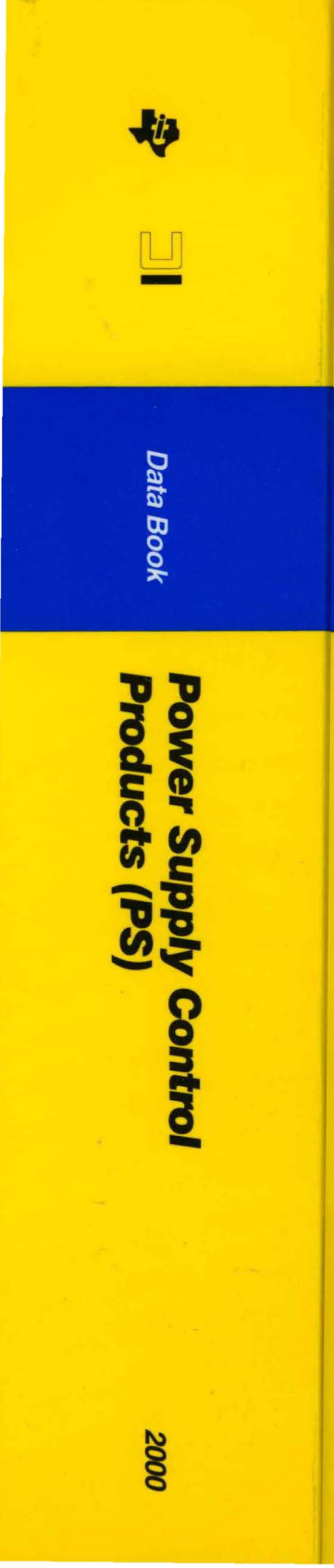


Power Supply Control Products (PS)

Data Book

2000

TEXAS INSTRUMENTS

Unitrode Products from Texas Instruments

Power Supply Control Products (PS)

Data Book

2000

Analog and Mixed-Signal

On October 15, 1999, Texas Instruments strengthened its ability to provide you with truly premier Power Management solutions. We are proud to announce the acquisition of Power Management expert Unitrode and Battery Management expert Benchmarq.

As you may know, Unitrode has a 40-year history of designing and supplying Power Management components and subsystems. Benchmarq, based in Dallas and acquired by Unitrode last year, has won multiple awards for its industry-leading Battery Management solutions.

TI's commitment to the Power Management marketplace is already evident in its growing portfolio of industry-leading low dropout regulators, supply voltage supervisors, low-power DC-DC converters, power distribution switches and processor power products. Now, with the combination of TI's and Unitrode's high-performance products and TI's leading-edge process technologies and packaging expertise, we are positioned to provide you with easy-to-use, high-performance Power Management solutions.

Unitrode brings a family of products that complements TI's existing portfolio. TI's worldwide network of service and support increases access to and support for the Unitrode and Benchmarq portfolios. Most important, Unitrode brings to this union hundreds of experienced employees dedicated to the Power Management market.

What's in this for you? TI and Unitrode designers are working together right now to develop next-generation Power and Battery Management solutions. Maybe you're looking for easy-to-design-in, turn-key solutions. Or perhaps you need high-performance products, and complete systems and applications knowledge so you can put a power system together yourself. Either way, TI is dedicated to satisfying all of your Power Management needs today and in the future.

The combined TI and Unitrode Power Management offering comprises a rich portfolio that we intend to build upon together. To find out more, including ordering samples, you can visit our website at **www.ti.com/sc/powerleader**, complete the enclosed reply card, or call us for more information, using the TI contact information found on the back cover of this book.

Using Unitrode Data Books

Data sheets and other information about Unitrode's products are organized, by business line, into four volumes: Interface (IF), Portable Power (PP), Power Supply Control (PP), and Nonvolatile SRAMs and Real-Time Clocks (NV).

Each book contains general information as well as sections devoted to the specific business line. Information in these books is referenced in several ways.

Information Source	Volume/ Page Location			
	IF	NV	PP	PS
Data Sheet Types	v	v	v	v
Table of Contents	vi	vi	vi	vi
Master Part Number Index	1-1	1-1	1-1	1-1
Master Application Note Index by Part Number	1-19	1-19	1-19	1-20
Master Application Note Index by Publication Number	1-24	1-24	1-24	1-25
Master Application Note Index by Subject	1-28	1-28	1-28	1-29
Unitrode Product Portfolio	7-1	10-1	6-1	10-1
Product Cross-Reference Tables (NV Book Only)	–	3-2 4-2 5-2	–	–
Ordering Information	2-1	2-1	2-1	2-1

Reading the Indices

The master indices, contained in all four data books, list the location of all data sheets. Each entry is preceded by one of the following 2-letter abbreviations:

- **IF** Interface
- **NV** Nonvolatile SRAMs and Real-Time Clocks
- **PP** Portable Power
- **PS** Power Supply Control

Unitrode's Products

Unitrode Corporation is a world leader in the design and manufacture of innovative, high-performance linear and mixed-signal ICs and modules. This data book introduces the Company's products designed for commercial, industrial, consumer, and military/aerospace applications.

Focused on power management, battery management, and high-speed data communications, products include:

- Off-line power management
- DC/DC power management
- Protection/supervisory circuits
- Portable power management
- Motion/motor controls
- High-speed interface
- Nonvolatile controllers and NVSRAMs
- Real-time clocks

Unitrode also offers an assortment of special function ICs, including fiber-to-curb ringers, CAN transceivers, IrDA transceivers, cellular power-management products and pager/PDA power controllers.

All Unitrode products are backed by design and applications teams that understand the interaction between the Company's products and rest of the power system/subsystem. Unitrode designs technically advanced products in response to customer needs and in anticipation of market trends.

Whatever the application—Power Management, Battery Management, or Ultrafast Data Communications—Unitrode is an innovative, dependable and customer-driven source for catalog, semi-custom, and custom linear/mixed-signal ICs and modules.

Worldwide Service

Unitrode serves its customers around the world from many locations:

- Design centers in New Hampshire, Texas, California, and North Carolina
- A facility in Dallas for assembly and manufacturing
- A facility in Singapore for testing, assembly subcontractor coordination, and customer service
- A worldwide network of manufacturers' representatives and distributors

Process Capabilities

Unitrode's bipolar process, optimized for both precision-analog and power functions, is constantly updated with the latest process options, such as:

- Operating-voltage ranges from 4–65V
- Schottky and integrated injection logic
- Ion implant
- Thin-film resistors for high accuracy
- Double-level metallization for high-density, high-current layouts and buried zener reference

The Company's BiCMOS process is ideal for high-density linear and mixed-mode designs, especially where speed and low power-consumption are of primary importance.

Options include:

- 3-, 2.5-, and 1-micron processes
- Up to 15V operation
- High-current, double-level metallization
- 125 fully isolated, vertical NPN transistors
- Thin-film resistors

This year, a new BCDMOS process offers all the options available with BiCMOS, as well as a lateral DMOS device with up to 35V operation for added power-handling capability.

An ISO9001 and 9002 Firm

Unitrode was one of the first U.S. linear/analog manufacturers to achieve IS/ISO 9001/EN29001 registration, and in 1998, the registrars completed recertification of the Merrimack and Singapore facilities and renewed the Company's registration to ISO 9001/9002-1994, respectively.

To be registered, the Company passed a rigorous examination of its quality systems—from product design through shipment. These registrations thus assure customers all over the world that Unitrode is adhering to very high, precisely defined standards.

Listening To Customers

To develop custom and semi-custom parts, Unitrode design engineers work very closely with customers, so all requirements are accurately understood, all possibilities are fully explored, and all products meet or exceed specified needs.

Unitrode also pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that satisfy them.

Important Notice

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Printed in U.S.A.
by Banta Book Group
Harrisonburg, Virginia

Product Production Status

The table below defines three types of data sheets issued at various stages of product development. Unitrode reserves the right to change products without notice to improve design performance, reliability, or manufacturability.

CLASSIFICATION	PRODUCT STAGE	DESCRIPTION
Advance Information Data Sheet	Formative or Design	This document contains the design specifications for product under development. Specifications may be changed in any manner without notice.
Preliminary Data Sheets	First Production	Supplementary data may be published at a later date. Unitrode reserves the right to make changes at any time without notice, in order to improve design and supply the best product possible.
No Classification Noted	Full Production	Product is in full production.


UNITRODE

Table of Contents

Power Factor Correction 4

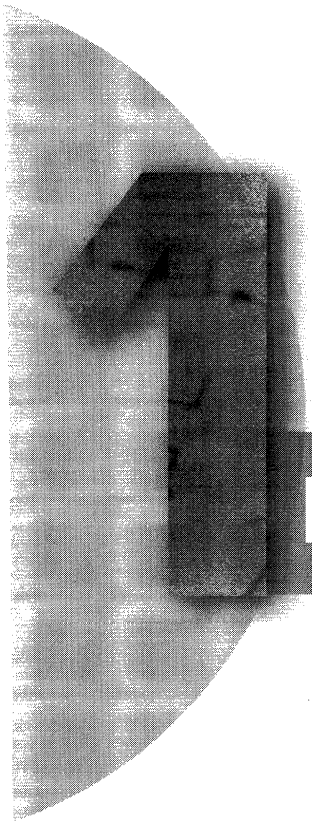
Linear Regulation 5

Power Drivers 6

Power Supply Support 7

Motion Control 8

INDEX



Master Part Number and Application Indices

Numeric Master Part Index

Part numbers are listed numerically, not by prefix (bq, DV, EV, UC, UCC).
*Products included in this book are listed in **bold**.*

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Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-19	A Simple Isolation Amplifier using the UC1901	UC3901	PS/7-64
DN-26	UC3842A - Low Cost Startup and Fault Protection Circuit	UC3842A/3A/4A/5A	PS/3-464
DN-27	UC1842/UC1842A Summary of Functional Differences	UC3842/3/4/5	PS/3-466
DN-28	UC3840/UC3841/UC3851 PWM Controllers - Summary of Functional Differences	UC3841	PS/3-467
DN-29	UC3842A Family Frequency Foldback Technique Provides Protection	UC3842A/3A/4A/5A	PS/3-468
DN-30	Programmable Electronic Circuit Breaker	UC3842A/3A/4A/5A	PS/3-469
DN-32	Optocoupler Feedback Drive Techniques	UC3832/3	PS/5-41
DN-33	Optocoupler Feedback Drive Techniques Using the UC3901 and UC3903	UC3903	PS/7-65
DN-35	IGBT Drive Using MOSFET Gate Drivers	UC3708	PS/6-85
DN-36	UC1525B/1527B Devices - Comparison Summary to UC1525A/1527A Devices	UC3525A/27A	PS/3-470
DN-38	Unique Converter for Low Power Bias Supplies	UC494/5A&C	PS/3-471
DN-39E	Optimizing Performance in UC3854 Power Factor Correction Applications	UCC3857	PS/4-76
DN-40	The Effects of Oscillator Discharge Current Variations on Maximum Duty Cycle and Frequency in UC3842 and UC3842A PWM ICs	UC3842/3/4/5	PS/3-473
DN-41	Extend Current Transformer Range	UC3854	PS/4-81
DN-42A	Design Considerations for Transitioning from UC3842 to the New UCC3802 Family	UCC3800/1-5	PS/3-476
DN-43	Simple Techniques to Generate a Negative Voltage Bias Supply from a Positive Input Voltage	UCC3800/1-5	PS/3-479
DN-44	UC3854A and UC3854B Advanced Power Factor Correction Control ICs	UC3854A/B	PS/4-83
DN-45	UC3846, UC3856 and UCC3806 Push-Pull PWM Current Mode Control ICs	UCC3806	PS/3-480
DN-45	UC3846, UC3856 and UCC3806 Push-Pull PWM Current Mode Control ICs	UC3856	PS/3-480
DN-46	Highly Efficient Low Power DC to DC Inverter Converts +5V Input to -3V Output	UCC3813	PS/3-482
DN-48	Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range	UCC3813	PS/3-484
DN-49	Easy Switcher Controls SEPIC Converter for Automotive Applications	UC2577	PS/3-487
DN-50	Simple Techniques for Isolating and Correcting Common Application Problems with UC3625 Brushless DC Motor Drives	UC3625	PS/8-111
DN-51	Programming the UCC3806 Features	UCC3806	PS/3-489
DN-52	Adjustable Electronic Load for Low Voltage DC Applications	UC39432	PS/7-76
DN-53A	Design Considerations for Synchronizing Multiple UC3637 PWMs	UC3637	PS/8-115
DN-54	Innovative Buck Regulator Uses High Side N-Channel Switch without Complex Gate Drive	UCC3813	PS/3-492
DN-56A	Single Switch Flyback Circuit Converts +5VDC to +/-12VDC for RS-232 and RS-422 Applications	UCC3800/1-5	PS/3-492
DN-57	Power Dissipation Considerations for the UC3726N/UC3727N IGBT Driver Pair	UC3726	PS/6-87
DN-58	UCC3912 Programmable Electronic Circuit Breaker - Performance Evaluation and Programming Information	UCC3912	IF/5-102
DN-59A	UCC3889 Bias Supply Controller Evaluation Kit - Schematic and List of Materials	UCC3888	PS/3-494
DN-60	UC3726/UC3727 IGBT Driver Pair Evaluation Kit Testing Procedure	UC3726	PS/6-90
DN-61	A High Performance Linear Regulator for Low Dropout Applications	UC3832/3	PS/5-42
DN-62	Switching Power Supply Topology: Voltage Mode vs. Current Mode	UCC35701	PS/3-496

*Publications included in this book are listed in **bold**.*

Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-63	The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters	UC3875/6/7/8	PS/3-499
DN-64	Inductorless Bias Supply for Synchronous Rectification and High Side Drive Applications	UCC3583	PS/3-502
DN-65	Considerations in Powering BiCMOS ICs	UCC3809-1,-2	PS/3-505
DN-66	Unitrode - UC3854A/B and UC3855A/B Provide Power Limiting with Sinusoidal Input Current for PFC Front Ends	UC3854A/B	PS/4-86
DN-67	UCC3913 Electronic Circuit Breaker for Negative Voltage Applications Evaluation Kit List of Materials for a -48V/1A Test Circuit	UCC3913	IF/5-105
DN-68	Parelling UCC3912 Electronic Circuit Breaker ICs	UCC3912	IF/5-106
DN-70	UC3573 Buck Regulator PWM Control IC	UC3573	PS/3-508
DN-72	Lamp Ignitor Circuit	UCC3305	PS/9-52
DN-73	UCC3941 One Volt Boost Converter Demonstration Kit - Schematic and List of Materials	UCC3941-3/5/ADJ	PP/7-101
DN-75	Using the UC3871 and UC3872 Resonant Fluorescent Lamp Drivers in Floating Lamp Applications	UC3872	PP/8-50
DN-76	Closed Loop Temperature Regulation Using the UC3638 H-Bridge Motor Controller and a Thermoelectric Cooler	UC3638	PS/8-118
DN-77	Overcurrent Shutdown with the UC3853	UC3853	PS/4-91
DN-78	High Power Factor Preregulator IC, Evaluation Board, Schematic and List of Materials	UC3853	PS/4-92
DN-79	UCC3750 Demonstration Board Operating Guidelines	UCC3750	PS/9-55
DN-81	UCC3911 Demo Board Information	UCC3911	PP/6-51
DN-82	UCC3958 Demonstration Board Schematic and Bill of Materials	UCC3958	PP/6-55
DN-83	UC3584 DW Secondary Side Post Regulator, Evaluation Board, Schematic, and List of Materials	UC3584	PS/3-511
DN-84	UCC3956 Switch Mode Lithium-Ion Battery Charger Controller Evaluation Board, Schematic and List of Materials	UCC3956	PP/3-413
DN-85	UCC3831 USB Power Controller IC, Evaluation Board – Schematic and List of Materials	UCC3831	IF/5-106
DN-86	UCC3954 Single Cell Lithium-Ion to +3.3V Converter Performance Evaluation Kit – Schematic and List of Materials	UCC3954	PP/7-103
DN-87	UCC3918 Low On-Resistance Hot Swap Power Manager Performance Evaluation Kit , Schematic and List of Materials	UCC3918	IF/5-113
DN-88	UCC5342 IrDA 115.2kbps Tranceiver Performance Evaluation Board – Schematic and List of Materials	UCC5342	PP/9-15
DN-89	Comparing the UC3842, UCC3802, and UCC3809 Primary-Side PWM Controllers	UC3842/3/4/5	PS/3-514
DN-90	UCC3858 "Energy Star" PFC Evaluation Board, Schematic and List of Materials	UCC3858	PS/4-94
DN-91	UCC3926DS ±20A Integrated Current Sensor Evaluation Board – Schematic and List of Materials	UCC3926	PS/9-58
DN-92	UCC5630 SCSI Multimode (LVD/SE) Evaluation Board and List of Materials	UCC5630	IF/3-122
DN-93	UCC3957, Three - Four Cell Lithium-Ion Protector Circuit, Evaluation Board and List of Materials	UCC3957	PP/6-57
DN-94	UCC5343, IrDA Transceiver with Encoder/Decoder, Evaluation Board and List of Materials	UCC5343	PP/9-19
DN-95	UCC3919 Hot Swap Power Manager Evaluation Circuit Board and Bill of Materials	UCC3919	IF/5-116
DN-96	UCC3952 Evaluation Board and List of Materials	UCC3952	PP/6-61

*Publications included in this book are listed in **bold**.*

Application/Design Notes by Publication Number

Pub.	Title	IC Featured	Volume/Page
DN-97	UCC39411 Low Power Synchronous Boost Converter Evaluation Kit, Schematic and Bill of Materials	UCC39411/2/3	PP/7-106
DN-98	UCC3917 Positive Floating Hot Swap Power Manager Evaluation Kit, Schematic and Bill of Materials	UCC3917	IF/5-120
DN-99	Pulse Edge Transmission (PET) circuit	UCC3961	PS/8-102
DN-501	Using RAM Clear Function with bq3285/bq3287A RTCs	bq3285/bq3287	NV/4-321
DN-502	High-Side Current Sensing with Benchmarq Portable Power Fast-Charge Control IC		PP/3-307
U-93	A New Integrated Circuit for Current Mode Control	UC3846/7	PS/3-518
U-94	The UC1901 Simplifies the Problem of Isolated Feedback in Switching Regulators	UC3901	PS/7-72
U-95	Versatile UC1834 Optimizes Linear Regulator Efficiency	UC3834	PS/5-49
U-97	Modeling, Analysis and Compensation of the Current Mode Converter	UCC3813	PS/3-526
U-99	UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor	UC3717	PS/8-118
U-100A	UC3842/3/4/5 Provides Low-Cost Current-Mode Control	UC3842/3/4/5	PS/3-532
U-102	UC1637/2637/3637 Switched Mode Controller for DC Motor Drive	UC3637	PS/8-126
U-104	Improved Charging Methods for Lead-Acid Batteries using the UC3906	UC3906	PP/3-388
U-110	1.5MHz Current Mode IC Controlled 50W Power Supply	UC3825	PS/3-546
U-111	Practical Considerations in Current Mode Power Supplies	UC3709	PS/3-558
U-112	A High Precision PWM Transconductance Amplifier for Microstepping using Unitrode's UC3637	UC3637	PS/8-137
U-113	Design Notes on Precision Phase Locked Speed Control for DC Motors	UC3634	PS/8-145
U-115	New Integrated Circuit Produces Robust, Noise Immune System for Brushless DC Motors	UC3625	PS/8-155
U-118	New Driver ICs Optimize High Speed Power MOSFET Switching Characterisitics	UC3709	PS/6-92
U-120	A Simplified Approach to DC Motor Modeling for Dynamic Stability Analysis	UC3638	PS/8-162
U-122	A New Family of Integrated Circuits Controls Resonant Mode Power Converters	UC3861-8	PS/3-576
U-127	Unique Chip Pair Simplifies High Side Switch Drive	UC3725	PS/6-107
U-128	The UC3823A,B & UC3825A,B Enhanced Generation of PWM Controllers	UC3823/5A/B/3	PS/3-585
U-129	UC3907 Load Share IC Simplifies Parallels Power Supply Design	UC3907	PS/7-84
U-130	Dedicated ICs Simplify Brushless DC Servo Amplifier Design	UC3625	PS/8-166
U-131	Simple Switchmode Lead-Acid Battery Charger	UC3906	PP/3-417
U-132	Power Factor Correction Using the UC3852 Controlled ON-Time Zero Current Switching Technique	UC3852	PS/4-98
U-133A	UCC3800/1-5 BiCMOS Current Mode Control ICs	UCC3800/1-5	PS/3-594
U-134	UC3854 Controlled Power Factor Correction Circuit Design	UC3854	PS/4-114
U-135	The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters	UC3848	PS/3-612
U-136A	Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller	UC3875/6/7/8	PS/3-623
U-137	Practical Considerations in High Performance MOSFET, IGBT & MCT Gate Drive Circuits	UC3709	PS/6-122
U-138	Zero Voltage Switching Resonant Power Conversion	UC3861-8	PS/3-637
U-140	Average Current Mode Control of Switching Power Supplies	UC3849	PS/3-664
U-141	Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution	UC3871	PP/8-27

*Publications included in this book are listed in **bold**.*

Application/Design Notes by Publication Number

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INTERFACE (IF)

Hot Swap Power Managers

SCSI

NONVOLATILE SRAMs AND REAL-TIME CLOCKS (NV)

Real-Time Clocks

PORTABLE POWER (PP)

Battery Charging

*Publications included in this book are listed in **bold**.*

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Frequency Foldback

Gate Drives

Isolation Amplifier

Leading Edge Blanking

Lighting Circuits

Linear Voltage Regulators

Load Sharing

Magnetics Design

*Publications included in this book are listed in **bold**.*

Publications included in this book are listed in ***bold****.*

Power Factor Correction

PWM Oscillators

Rectification

Resonant Converters

Ring Generator Controllers

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General Information

Ordering Information

(see Benchmarq ordering information page for "bq" prefix products)

UC	XXXXX	XX	XX	XXXX	general syntax
UC	17131 27131 37131	A	J	883B	example

PREFIX
"UC" ~ Linear Integrated Circuits
"UCC" ~ BiCMOS

PART NUMBER
First digit "1" ~ Military Temperature Range*
First digit "2" ~ Industrial Temperature Range*
First digit "3" ~ Commercial Temperature Range*
(*consult individual data sheets for specific temperature ranges on each part)

SCREEN/PROCESSING OPTIONS
"883" ~ MIL-STD-883
Class Q of MIL-PRF-38535

PACKAGE OPTIONS

OPTIONAL GRADES
A or B ~ Improved Version

Letter Designator	Package Type
D	Plastic Narrow Body (150 mil) SOIC
DW	Plastic Wide Body (300 mil) SOIC
DP	Plastic Narrow Body Power SOIC
DS	Plastic Narrow Body (150 mil) SOIC with Shunt Current Sense
DWP	Plastic Wide Body Power SOIC
FP	Power Plastic Metric Quad Flatpack (MQFP)
FQ	Power Low Profile Quad Flatpack (LQFP)
FQP	Power Plastic Low Profile Quad Flatpack (LQFP)
J	Ceramic Dual-in-Line (300 mil and 600 mil)
L	Ceramic Leadless Chip Carrier
LP	Power LCC
M	Quasi Shrink Small Outline (150 mil body, 0.635mm pitch)
MWP	Power Quasi Shrink Small Outline (300 mil body, 0.88mm pitch)
N	Plastic Dual-in-Line (300mil and 600 mil)
P	Mini SOIC
PW	Thin Shrink Small Outline (TSSOP)
PWP	Power TSSOP
Q	Plastic Leadless Chip Carrier (PLCC)
QP	Power (PLCC)
SP	Power Ceramic Dual-in-Line
T	Plastic TO-220
TD	Plastic TO-263 Power Surface Mount
Z	Zig-Zag In-Line Power Package

Quality and innovation characterize our products!

Our commitment begins with our Quality Assurance System. In October 1992, Unitrode Corporation became one of the first in our industry to achieve IS/ISO 9001/EN 29001 Registration. Currently, Unitrode's quality-assurance system exceeds the rigorous requirements of ISO 9001-1994 and MIL-PRF-38535. Quality Management Institute (QMI) has awarded Unitrode a Certificate of Registration (Number 003889) indicating compliance with ISO 9001, for the design and manufacture of analog integrated circuits. For its Singapore branch, Unitrode also holds an ISO 9002 Certificate of Registration (Number 93-2-0148) from the Singapore Productivity and Standards Board, for semiconductor IC manufacturing, factory inspection and testing, and wafer-probe testing.

In August 1996, the Defense Supply Center-Columbus (DSCC) granted Unitrode full Q-Level certification to MIL-PRF-38535 for listing on the Qualified Manufacturers List (QML). In addition, DSCC continued Unitrode's laboratory suitability by certifying that our test methods accord with MIL-STD-883.

All Unitrode products and manufacturing processes meet extensive qualification requirements. Qualification ensures that

- Customer and/or design requirements are translated efficiently into manufacturing requirements
- All groups are integrated, coordinated, and capable
- Our processes are manufacturable
- Our products meet or exceed the reliability requirements of our customers

Process Qualification

When a process qualification is required, Quality Assurance organizes a cross-functional team that prepares and completes a formal qualification plan according to QP 2515. Key requirements for major processes include

- Documented design rules and process specifications; process and device simulation with full SPICE models
- Completed process control plan with identified critical, significant, and non-critical characteristics
- Implemented process-control charts
- Demonstrated Cp, and Cpk for significant and critical characteristics
- Documented out-of-control action plans (OCAPs)
- Completed quality audit
- Process-acceptance criteria
- Gage R&R studies
- Construction analyses

Reliability Testing

Our extensive reliability requirements ensure that our new processes demonstrate, for commercial products under typical use conditions, a 200 FIT rate or better (failures in time calculated at 70°C, 0.7eV activation energy, 60% confidence) at the time of qualification, using a minimum of three wafer lots. Figure 1, on page 2-6, lists typical reliability tests performed for new major processes.

Package Qualification

Whenever a new package is introduced, in addition to qualifying the manufacturing process using requirements appropriate to assembly processing, Unitrode performs a complete battery of reliability tests.

Figure 2, on page 2-7, depicts typical requirements for plastic packages. Figure 3, on page 2-8, presents the requirements for hermetic packages.

Product Qualification

New products must be manufactured using qualified processes and packages. Unitrode's new product qualification consists of 2 major milestones: Release For Introduction (RFI) and Release to Production (RTP).

RFI is the term Unitrode uses to describe devices that

- Are built on a qualified process
- Meet the preliminary data sheet over the specified temperature range
- Demonstrate no infant mortality
- Have been verified in the appropriate application
- Have had ESD measured and classified
- Have a released preliminary test program

Devices that achieve RTP meet all the RFI requirements (plus additional requirements) and complete Unitrode's product qualification. Typical RTP requirements include

- Bench and temperature characterization
- Demonstrated compliance to all data-sheet parameters
- Cp, Cpk targets met for all untrimmed parameters in data sheet
- Test program complete and released to production
- Machine capability less than 5% of the device specification range
- Test schematic(s), test program(s), bonding diagram(s), and burn-in diagrams approved and released
- ESD measured and classified (human body model)
- Passed latch-up and HTOL test to 1000 hours
- Final data sheet approved and released.

Results

As a result of our comprehensive qualification procedures, we are able to report long-term device reliability of 4.0 FIT or lower for combined functional families. This figure is estimated from millions of hours of life-testing at accelerated temperatures.

Failure Analysis

If we do experience a failure during pre-production qualification, we have an extensive failure-analysis lab to determine and fix the root cause before the products reach our customers. We begin by verifying the failure to published specifications. We provide written failure-verification to our customers within 72 hours.

This notification is followed by failure-mode identification through laboratory analyses such as electrical measurements, optical and electron microscopy, radiography, device deprocessing, microsectioning, spectrometry, and cholesteric liquid-crystal analysis. Unitrode maintains a ten-day cycle to identify moderately complex failures from receipt of failed units.

If needed, closed-loop corrective action is managed through our Corrective Action Continuous Improvement Team using the 8D approach.

Customer Notification

Our continuous improvement requires an occasional product or process change. Unitrode notifies the customer (a 90-day notification whenever possible) when

- A waiver to a customer's or Unitrode's specification is required before shipment of material deemed suitable by Unitrode or our customer
- Any product, process or mask change requires a change to Unitrode's data sheet, SCD, purchase order, or customer specification
- Any product, process or mask change reduces ESD rating
- A change occurs in manufacturing location, including wafer fabrication, assembly, and test
- There is a change in wafer starting material, dieletric, passivation or metalization materials and certain assembly materials
- A major change occurs in manufacturing process on a critical or significant characteristic, according to our process control plan(s)
- A manufacturing process changes a characteristic that is a reliability concern
- Unitrode's operating procedures or quality systems change significantly

Total Business Excellence

Unitrode's policy of Total Business Excellence (TBE) goes well beyond the scope of Quality Assurance. A company demonstrating Total Business Excellence must have more rigorous business practices than industry standards and a supporting culture to enable and improve these practices.

TBE requires continuous improvement. It is a never-ending search for ways to improve everything we do, and a pledge to ultimately translate improvements into better products and services for our customers.

Our goals include improved designs that meet the broadest spectrum of application needs, improved translation of customer requirements into actual product performance characteristics, improved understanding of process capabilities to improve the product introduction process, higher productivity, less scrap and rework, and lower production costs.

For example, Unitrode internal qualification procedures now include rigorous qualification of our suppliers, subcontractors, and the wafer fabrication (both major new processes and unit processes). Each qualification is managed by a cross-functional quality team. Qualification requirements include detailed and advanced process control plans, out-of-control action plans (OCAPs), demonstrated process-capability, advanced statistical process-control techniques, and Gage R&R studies.

We've improved many of our internal practices: for example, shop floor control, document management, customer notification, and corrective action. We've replaced our old hardcopy system with electronically based systems using the best software systems and relational databases.

Total Business Excellence affects every department, activity, and product, from initial concept to end-user installation and operation.

For all of these reasons we deliver high-quality, reliable products. Our continuing quest to improve everything we do yields better and more reliable products and services for our customers. That is what earns customer loyalty!

Figure 1. Typical Reliability Tests for New Processes

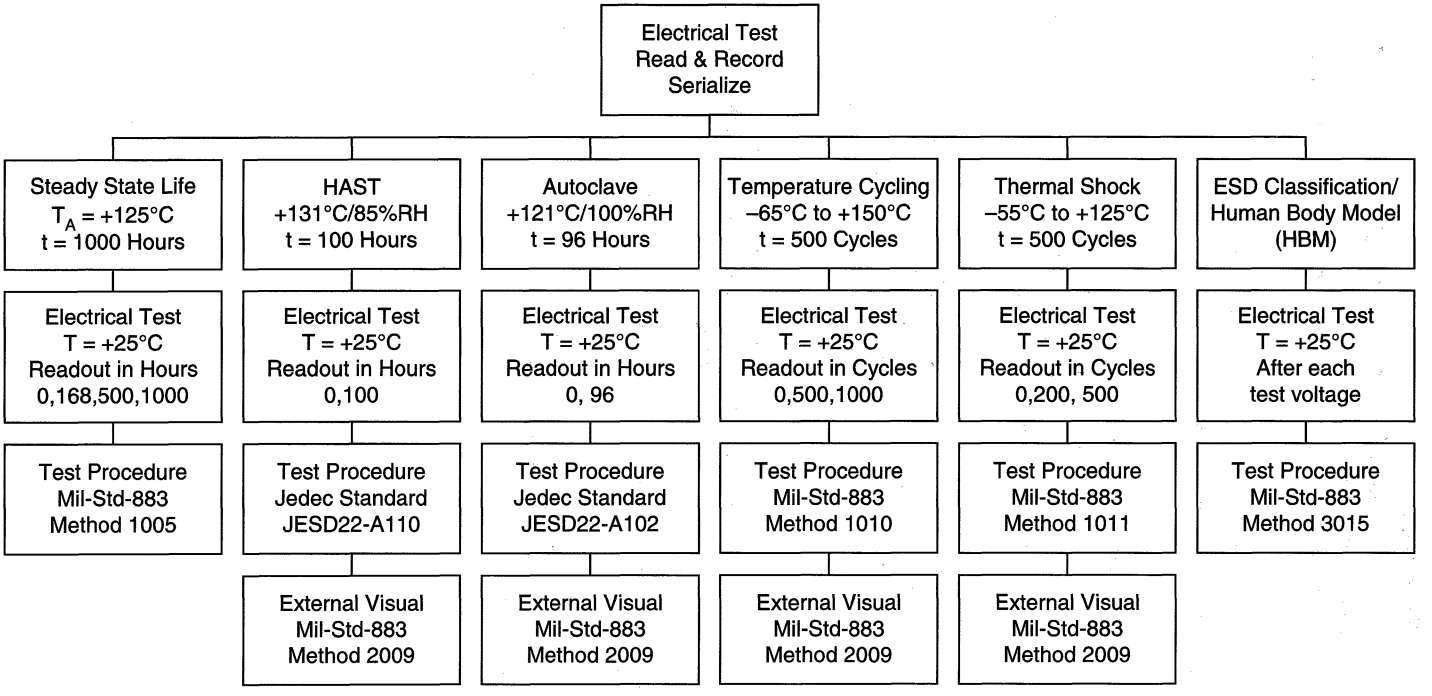
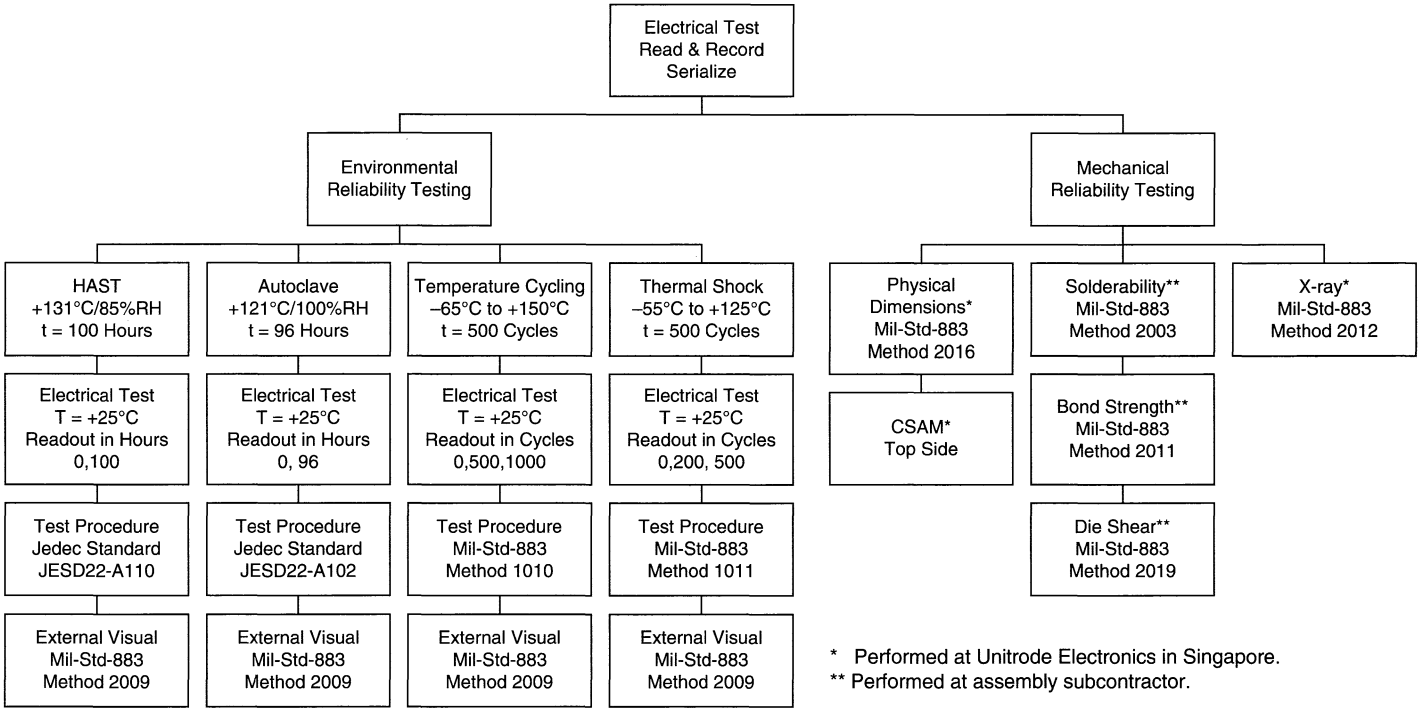
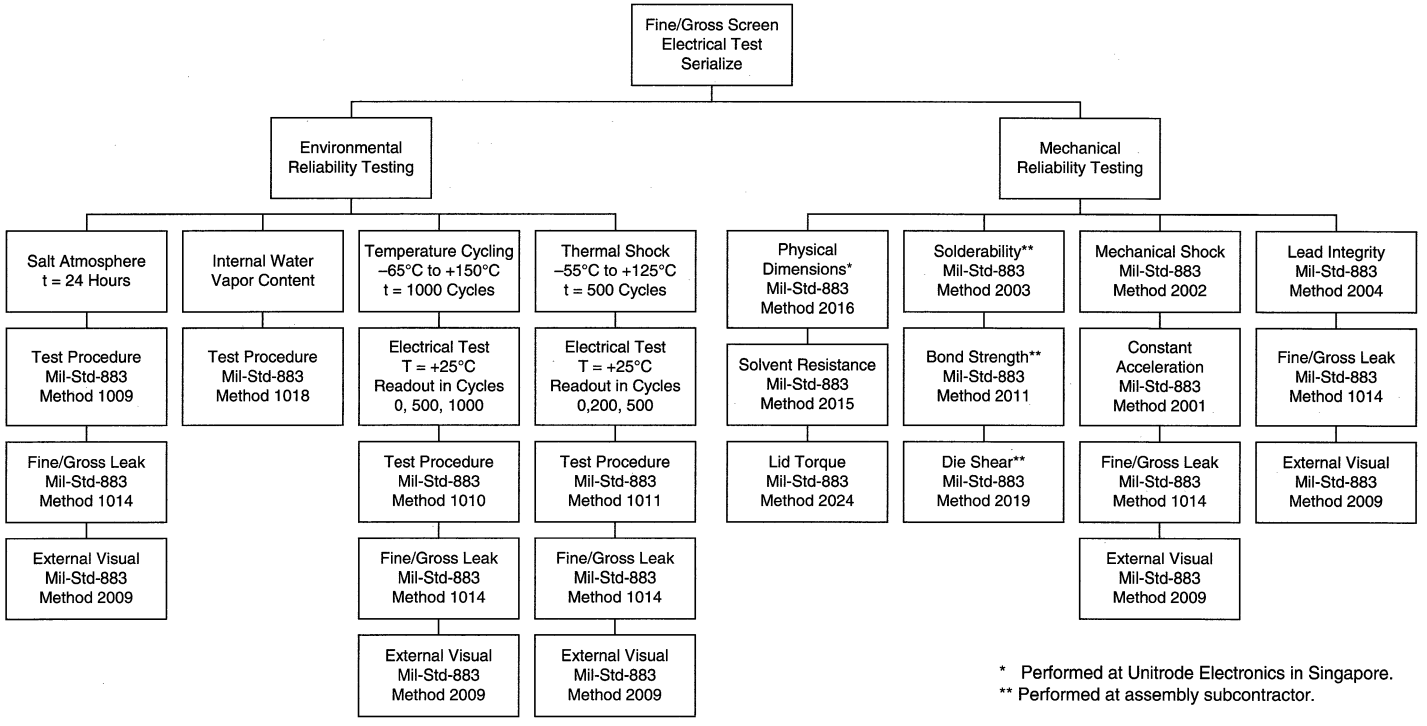


Figure 2. Typical Reliability Requirements for Plastic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Figure 3. Typical Reliability Requirements for Hermetic Packages



* Performed at Unitrode Electronics in Singapore.
** Performed at assembly subcontractor.

Description

Unitrode offers most of our products in die and/or wafer form through our die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques.Die thickness is either 12 mils or 15 mils, +/- 1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing

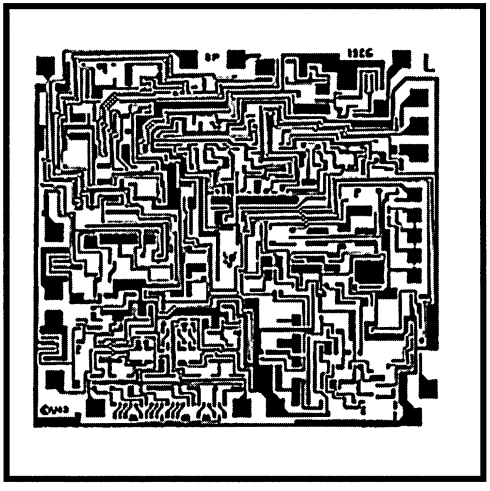
All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications, with the exception of some high power or high speed devices where production probe equipment limit the test environment.

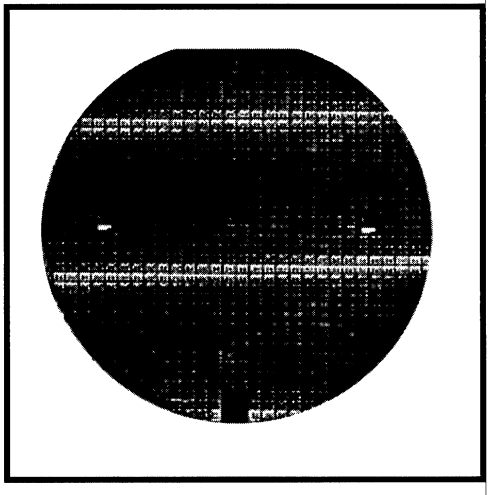
Inspection

Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering

Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.



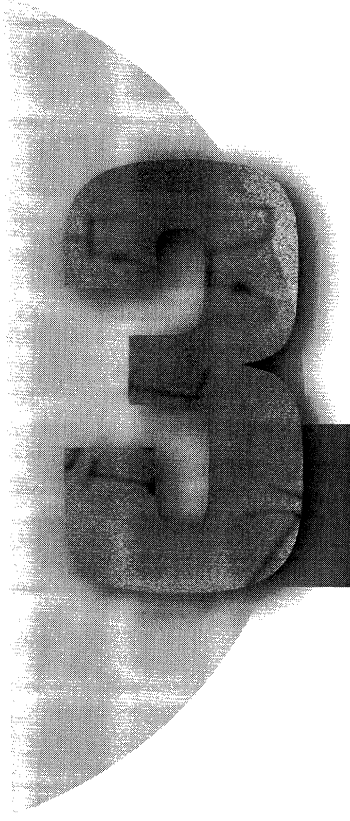


Small Computer Systems Interface (SCSI)

Bus Bias Generators

Hot Swap Power Manager™ ICs

Drivers/Receiver Transceivers



PWM Control

PWM Control

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3800	UCC3801	UCC3802	UCC3803	UCC3804
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count❖	8	8	8	8	8
Page Number	PS/3-173	PS/3-173	PS/3-173	PS/3-173	PS/3-173

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3805	UCC3806	UCC3807-1	UCC3807-2	UCC3807-3
Application	DC-DC and Battery	Isolated Output, Push-pull Controller	DC-DC	Off-line	DC-DC and Battery
Topology	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1.5%	1%	1.5%	1.5%	1.5%
Peak Output Current	1A	0.5A	1A	1A	1A
Under Voltage Lockout	4.1V / 3.6V	7.5V / 6.75V	7.2V / 6.9V	12.5V / 8.3V	4.3V / 4.1V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y		Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	50% / 50%	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal		Y			
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-45, DN-51, DN-65, U-97, U-110, U-144	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A
Pin Count❖	8	16	8	8	8
Page Number	PS/3-173	PS/3-180	PS/3-187	PS/3-187	PS/3-187

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3808-1	UCC3808-2	UCC3809-1	UCC3809-2	UCC3810
Application	Off-line	DC-DC and Battery	DC-DC	Off-line	Dual PWM Controller, Off-line, DC-DC
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	2%	2%	5%	5%	1.5%
Peak Output Current	0.5A Source, 1A Sink	0.5A Source, 1A Sink	0.4A Source, 0.8A Sink	0.4A Source, 0.8A Sink	1A
Under Voltage Lockout	12.5V / 8.3V	4.3V / 4.1V	10V / 8V	15V / 8V	11.3V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual, Totem Pole
Startup Current	130µA	130µA	100µA	100µA	150µA
Leading Edge Blanking					Y
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	50% / 50%	50% / 50%	90%	90%	50%
Separate Oscillator / Synchronization Terminal			N/A	N/A	Y
Application / Design Note	DN-65, U-97, U-110, U-170	DN-65, U-97, U-110, U-170	DN-65, DN-89, U-165, U-168	DN-65, DN-89, U-165, U-168	DN-65, U-97, U-110, U-133A
Pin Count❖	8	8	8	8	16
Page Number	PS/3-192	PS/3-192	PS/3-198	PS/3-198	PS/3-205

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-0	UCC3813-1	UCC3813-2	UCC3813-3	UCC3813-4
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count❖	8	8	8	8	8
Page Number	PS/3-212	PS/3-212	PS/3-212	PS/3-212	PS/3-212

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-5	UC3823	UC3823A	UC3823B	UC3824
Application	DC-DC and Battery	DC-DC	DC-DC	Off-line	Synchronous Rectifier, Forward Converter
Topology	Forward, Flyback	Buck, Boost	Buck, Boost	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1%	1%	1%	1%
Peak Output Current	1A	1.5A	2A	2A	1.5A
Under Voltage Lockout	4.1V / 3.6V	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	9.2V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Complementary, Totem Pole
Startup Current	100µA	1.1mA	0.1mA	0.1mA	1.1mA
Leading Edge Blanking	Y		Y	Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	100%	Programmable, <100%	Programmable, <100%	100%
Separate Oscillator / Synchronization Terminal		Y	Y	Y	Y
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	U-97, U-111, U-131	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-111
Pin Count❖	8	16	16	16	16
Page Number	PS/3-212	PS/3-219	PS/3-225	PS/3-225	PS/3-233

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3825	UC3825A	UC3825B	UC3826❍	UC3827-1
Application	DC-DC	DC-DC	Off-line	Secondary Side, Average Current Mode	Multiple Output or High Voltage Output DC-DC Converters
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Buck Current Fed Push-pull
Voltage Reference Tolerance	1%	1%	1%	1%	4%
Peak Output Current	1.5A	2A	2A	0.25A	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers
Under Voltage Lockout	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	8.4V / 8.0V	9V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Floating Buck, Push-pull
Startup Current	1.1mA	0.1mA	0.1mA		1mA
Leading Edge Blanking		Y	Y	N/A	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable, <50%	Programmable, <50%	90% for Buck Stage, 50% / 50% for Push-pull Stage
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	U-97, U-110, U-111	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-135, U-140	
Pin Count❖	16	16	16	24	24
Page Number	PS/3-240	PS/3-225	PS/3-225	PS/3-247	PS/3-257

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3827-2	UCC3830-4	UCC3830-5	UCC3830-6	UCC3839❍
Application	Multiple Output or High Voltage Output DC-DC Converters	Microprocessor Power	Microprocessor Power	Microprocessor Power	Secondary Side, Average Current Mode Control
Topology	Buck Voltage Fed Push-pull	Buck	Buck	Buck	Any Topology
Voltage Reference Tolerance	4%	1%*	1%*	1%*	1%
Peak Output Current	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers	1.5A	1.5A	1.5A	10mA to Drive Opto-coupler
Under Voltage Lockout	9V / 8.4V	10.5V / 10V	10.5V / 10V	10.5V / 10V	
Maximum Practical Operating Frequency	500kHz	100kHz	200kHz	400kHz	1MHz
Outputs	Floating Buck, Push-pull	Single	Single	Single	Opto-coupler Drive
Startup Current	1mA				
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	90% for Buck Stage, 50% / 50% for Push-pull Stage	95%	95%	95%	
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note					U-140
Pin Count❖	24	20	20	20	14
Page Number	PS/3-257	PS/3-263	PS/3-263	PS/3-263	PS/3-276

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3841	UC3842	UC3842A	UC3843	UC3843A
Application	Primary Side, Programmable, Off-line, DC-DC	Off-line	Off-line	DC-DC	DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout		16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Open Collector	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	4.5mA	1mA	0.5mA	1mA	0.5mA
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	Programmable	100%	100%	100%	100%
Separate Oscillator / Synchronization Terminal					
Special Features			Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current
Application / Design Note	DN-28	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111
Pin Count❖	18	8, 14	8, 14	8, 14	8, 14
Page Number	PS/3-281	PS/3-289	PS/3-296	PS/3-289	PS/3-296

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3844	UC3844A	UC3845	UC3845A	UC3846
Application	Off-line	Off-line	DC-DC	DC-DC	Off-line, DC-DC
Topology	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	0.5A
Under Voltage Lockout	16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V	7.7V / 6.95V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	1mA	0.5mA	1mA	0.5mA	
Leading Edge Blanking					
Soft Start					Y
Maximum Duty Cycle	50%	50%	50%	50%	50% / 50%
Separate Oscillator / Synchronization Terminal					Y
Special Features		Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current	
Application / Design Note	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-45, U-93, U-97, U-100A, U-111
Pin Count❖	8, 14	8, 14	8, 14	8, 14	16
Page Number	PS/3-289	PS/3-296	PS/3-289	PS/3-296	PS/3-302

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3847	UC3848❍	UC3849❍	UC3851	UC3856
Application	Off-line, DC-DC	Average Current Mode, Off-line, DC-DC	Secondary Side, Average Current Mode	Off-line, Programmable, Primary Side Controller	Isolated Output, Push-pull Controller
Topology	Push-pull, Full Bridge, Half Bridge	Forward, Flyback	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	0.5A	2A	0.25A	0.2A	1.5A
Under Voltage Lockout	7.7V / 6.95V	13V / 10V	8.3V / 7.9V		7.7V / 7.0V
Maximum Practical Operating Frequency	500kHz	1MHz	1MHz	500kHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current		500µA		4.5mA	
Leading Edge Blanking		N/A	N/A	Y	
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable	50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y		Y		Y
Application / Design Note	DN-45, U-93, U-97, U-100A, U-111	U-135, U-140	U-135, U-140	DN-28	DN-45, U-93, U-97, U-110
Pin Count❖	16	16	24	18	16
Page Number	PS/3-302	PS/3-309	PS/3-317	PS/3-327	PS/3-333

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3880-4	UCC3880-5	UCC3880-6	UCC3882	UCC3884
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power	Off-Line or DC-DC Frequency Foldback Controller
Topology	Buck	Buck	Buck	Synchronous Buck	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%*	1%*	1%*	1%*	2%
Peak Output Current	1.5A	1.5A	1.5A	1.5A	0.5A Source, 1A Sink
Under Voltage Lockout	10.5V / 10V	10.5V / 10V	10.5V / 10V	10.5V / 10V	8.9V / 8.3V
Maximum Practical Operating Frequency	100kHz	200kHz	400kHz	700kHz	750kHz
Outputs	Single	Single		Dual, N-FET Drive	Single
Startup Current					200µA
Leading Edge Blanking					
Average Current Mode	Y	Y		Y	
Foldback Current Limiting	Y	Y		Y	
Soft Start					Y
Maximum Duty Cycle	95%	95%		95%	80%
Separate Oscillator / Synchronization Terminal					Y
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	
Application / Design Note	U-140	U-140	U-140	U-140	DN-65, U-164
Pin Count❖	24	18	16	28	16
Page Number	PS/3-373	PS/3-373	PS/3-373	PS/3-380	PS/3-393

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
** Combined Reference, DAC, and Error Amplifier Tolerance.*
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3886				
Application	Microprocessor Power				
Topology	Buck				
Voltage Reference Tolerance	1.5%				
Peak Output Current	1.5A				
Under Voltage Lockout	10.3V / 10.05V				
Maximum Practical Operating Frequency	400kHz				
Outputs	Single				
Startup Current					
Leading Edge Blanking					
Average Current Mode					
Foldback Current Limiting					
Soft Start					
Maximum Duty Cycle	95%				
Separate Oscillator / Synchronization Terminal					
Special Features	External Reference Input, Use with UC3910				
Application / Design Note	U-140, U-156, U-157				
Pin Count❖	16				
Page Number	PS/3-400				

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UC2577-12	UC2577-15	UC2577-ADJ
Description	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator
Application	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications
Output Voltage	12V	15V	Adjustable
Special Features	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available
Application / Design Note	DN-47, DN-49	DN-47, DN-49	DN-49
Pin Count❖	5	5	5
Page Number	PS/3-31	PS/3-31	PS/3-36

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER				
	UC3572	UC3573	UC3578	UCC3585+	
Application	Low Power, High Efficiency, Spot Regulator	Low Power, High Efficiency, Spot Regulator	DC-DC	Low Input Voltage Synchronous Buck Regulator with Output Voltage Tracking	
Topology	Negative Output Flyback	Buck	Buck	Voltage Mode Synchronous Buck	
Voltage Reference Tolerance	2%	2%	2%	1%	
Peak Output Current	0.5A	0.5A	0.6A Source, 0.8A Sink	0.5A	
Maximum Practical Operating Frequency	300kHz	300kHz	100kHz Internal Oscillator	700kHz	
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Floating Totem Pole	P FET/N FET Synchronous	
Startup Current			N/A	2.3mA	
VoltageFeedforward				N	
Soft Start			Y	Y	
Maximum Duty Cycle	100%	100%	90%	100%	
Separate Oscillator / Synchronization Terminal				N	
Application / Design Note		DN-70	U-167		
Pin Count❖	8	8	16	16	
Page Number	PS/3-108	PS/3-112	PS/3-116	PS/3-154	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39401+	UCC3941	UCC39411/2/3+
Description	Low Voltage Boost Controller / Charger	1V Synchronous Boost Converter	1V Low Power Boost Controller
Application	Pager Power	High Efficiency Integrated Boost Converter	High Efficiency Low Power Synchronous Boost Conversion
Special Features	•High Efficiency Boost •1V Input •Battery Charger •Backup LDO	•Full Load Startup at 1V •Power Limit Control •Auxiliary 9V Supply •Output Disconnect •Shutdown Mode	•200mW Output Power with Battery Voltages as low as 0.8V •Power Limit Control •Adaptive Current Mode Control •Auxiliary 7V Supply •Shutdown Mode
Application / Design Note			
Pin Count❖	20	8	8
Page Number	PP/7-34	PP/7-45	PP/7-58

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39421/2+	UCC3954	
Description	Multimode HF PWM Controller	Single Cell Lithium-Ion to 3.3V Converter	
Application	High Efficiency Boost, Sepic Flyback Converter	High Efficiency Flyback Converter	
Special Features	•2mHz Operation •1.8V Input •Current Limit •Power-on Reset •Low Voltage Detect	•Fixed 3.3V Output •750mA Output Current •Low Battery Warning •Low Battery Disconnect •Shutdown Mode	
Application / Design Note			
Pin Count❖	16, 20	8	
Page Number	PP/7-66	PP/7-93	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3588+	UCC3830-4	UCC3830-5	UCC3830-6	UCC3880-4
Application	Synchronous Buck Regulator with 5 Bit DAC	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power
Topology	Voltage Mode Synchronous Buck	Buck	Buck	Buck	Buck
Voltage Reference Tolerance	1%	1%*	1%*	1%*	1%*
Peak Output Current	1A	1.5A	1.5A	1.5A	1.5A
Maximum Practical Operating Frequency	700kHz	100kHz	200kHz	400kHz	100kHz
Outputs	Dual NFET Synchronous	Single	Single	Single	Single
Soft Start	Y				
Average Current Mode		Y	Y	Y	Y
FoldbackCurrent Limiting		Y	Y	Y	Y
Maximum Duty Cycle	100%	95%	95%	95%	95%
Special Features		5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor
Application / Design Note					U-140
Pin Count❖	16	20	20	20	20
Page Number	PS/3-163	PS/3-263	PS/3-263	PS/3-263	PS/3-373

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3880-5	UCC3880-6	UCC3882		
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power		
Topology	Buck	Buck	Synchronous Buck		
Voltage Reference Tolerance	1%*	1%*	1%*		
Peak Output Current	1.5A	1.5A	1.5A		
Maximum Practical Operating Frequency	200kHz	400kHz	700kHz		
Outputs	Single	Single	Dual, N-FET Drive		
Soft Start					
Average Current Mode	Y	Y	Y		
FoldbackCurrent Limiting	Y	Y	Y		
Maximum Duty Cycle	95%	95%	95%		
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor		
Application / Design Note	U-140	U-140	U-140		
Pin Count❖	20	20	28		
Page Number	PS/3-373	PS/3-373	PS/3-380		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Support	UNITRODE PART NUMBER		
	UCC391+	UC3910	UCC3946
Description	5-Bit DAC 5V Operation	Reference, 4-bit DAC and Fault Monitor	Microprocessor Supervisor with Watchdog Timer
Application	Sets Control Voltage for UC3886 and other Precision PWMs	Sets Control Voltage for UC3886, UC3870 and other Precision PWMS	Accurate Microprocessor Supervision
Special Features	•5V Operation •1% Combined Reference and DAC Tolerance •Meets VID Code for Pentium II Processors	•4-bit DAC Sets Output Voltage of PWM, Meets Intel VID Code •1% Combined Reference and DAC Tolerance •Over and Under Voltage Monitoring and Protection	•Programmable Reset Period •Programmable Watchdog Period •1.5% Accurate Threshold •4mA IDD
Application / Design Note		U-157, U-158	
Pin Count❖	8	16	8
Page Number	PS/3-434	PS/3-437	PP/7-88

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Post Regulation Controllers	UNITRODE PART NUMBER				
	UCC3583	UC3584	UC3838A		
Application	Secondary Side Post Regulation	DC-DC Secondary Side Synchronous Post Regulator	Mag-Amp Controller		
Topology	Buck	Buck			
Voltage Reference Tolerance	1.5%	1%	1%		
Peak Output Current	1.5A Source, 0.5A Sink	1.5A Source and Sink	120mA Reset Current		
Maximum Practical Operating Frequency	500kHz	1MHz			
Undervoltage Lockout	9.0V / 8.4V	10.5V / 8.8V	N/A		
Outputs	Single, Totem Pole	Single, Totem Pole			
Startup Current	100µA	N/A			
Voltage Feedforward	N/A				
Soft Start	Y	Y			
Maximum Duty Cycle	95%	94%			
Separate Oscillator / Synchronization Terminal	Y	Y			
Special Features	•For Both Single Ended and Center Tapped Secondary Circuits •Operation From Floating Supply Referenced to Output	•Can Use Existing Windings •Internally Regulated 15V Boost Supply Bias for Low Voltage Applications •Short Circuit Protection with Programmable Delay	•Dual Op-Amps •–120V Reset Driver		
Application / Design Note	DN-64	DN-64, DN-83	DN-47		
Pin Count ❖	14	16	16, 20		
Page Number	PS/3-139	PS/3-148	PS/3-272		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Secondary Side PWM Control	UNITRODE PART NUMBER				
	UC3826	UCC3839❍	UC3849❍	UCC3960+	UCC3961+
Application	Secondary Side, Average Current Mode	Secondary Side, Average Current Mode Control	Secondary Side, Average Current Mode	Primary-Side Startup Control	Primary-Side Startup Control
Topology	Forward, Flyback, Buck, Boost	Any Topology	Forward, Flyback, Buck, Boost		
Voltage Reference Tolerance	1%	1%	1%	5%	5%
Peak Output Current	0.25A	10mA to Drive Opto-coupler	0.25A	1.5A	1.5A
Undervoltage Lockout	8.4V / 8V		8.3V / 7.9V	10V / 8V	10V / 8V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	400kHz Synchronizable Switching Frequency	400kHz Synchronizable Switching Frequency
Outputs	Single, Totem Pole	Opto-coupler Drive	Single, Totem Pole	Single	Single
Startup Current				150µA	150µA
Leading Edge Blanking	N/A		N/A	N/A	N/A
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	Programmable		Programmable		Programable V-S Clamp
Separate Oscillator / Synchronization Terminal	Y		Y		
Special Features					• Multimode OVC Protection, • Programable OV and UV, • Self Bias Regulation.
Application / Design Note	U-135, U-140	U-140	U-135, U-140	DN-99	DN-99
Pin Count ❖	24	14	24	8	14
Page Number	PS/3-247	PS/3-276	PS/3-317	PS/3-442	PS/3-450

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★	UC3860
Application	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Off-line, DC-DC, Zero Current Switching
Topology	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1%
Peak Output Current	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A	2A
Undervoltage Lockout	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V	17.3V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	2MHz
Outputs	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2	Dual Programmable, Totem Pole
Startup Current	50µA	50µA	50µA	50µA	300µA
Voltage Feedforward	Y	Y	Y	Y	
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	Programmable	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-65	DN-65	DN-65	DN-65	
Pin Count ❖	16	16	16	16	24, 28
Page Number	PS/3-122	PS/3-122	PS/3-122	PS/3-122	PS/3-341

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3861	UC3862	UC3863	UC3864	UC3865
Application	Off-line, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	Off-line, Zero Current Switching
Topology	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Undervoltage Lockout	16.5V / 10.5V	16.5V / 10.5V	8V / 7V	8V / 7V	16.5V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle	50% / 50%	100%	50% / 50%	100%	50% / 50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-349	PS/3-349

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3866	UC3867	UC3868	UC3875	UC3876
Application	Off-line, Zero Current Switching	DC-DC and Battery, Zero Current Switching	DC-DC and Battery, Zero Current Switching	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	2A	2A
Undervoltage Lockout	16.5V / 10.5V	8V / 7V	8V / 7V	10.75V / 9.5V	15.25V / 9.25V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Soft Start				Y	Y
Maximum Duty Cycle	100%	50% / 50%	100%	100%	100%
Separate Oscillator / Synchronization Terminal				Y	Y
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	DN-63, U-111, U-136A	DN-63, U-111, U-136A
Pin Count ❖	16	16	16	20, 28	20, 28
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-357	PS/3-357

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3877	UC3878	UC3879	UCC3895+	
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase, Shifted Bridge	
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	
Voltage Reference Tolerance	1%	1%	1%	1%	
Peak Output Current	2A	2A	0.1A	0.1A	
Undervoltage Lockout	10.75V / 9.5V	15.25V / 9.25V	Selectable 10.75V / 9.5V, 15.25V / 9.25V	11V / 9V	
Maximum Practical Operating Frequency	1MHz	1MHz	300kHz	1MHz	
Outputs	Quad, Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	
Startup Current	150µA	150µA	150µA	150µA	
Leading Edge Blanking					
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	100%	100%	100%	100%	
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	
Application / Design Note	DN-63, U-111, U-136A	DN-63, U-111, U-136A	DN-63, U-111, U-136A, U-154	DN-63, U-136A	
Pin Count ❖	20, 28	20, 28	20	20	
Page Number	PS/3-357	PS/3-357	PS/3-367	PS/3-425	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3524✣	UC3524A	UC3525A	UC3525B	UC3526
Application	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge
Voltage Reference Tolerance	4%	1%	1%	0.75%	1%
Peak Output Current	100mA	200mA	400mA	200mA	100mA
Undervoltage Lockout		7.5V / 7V	7V	7V	Y
Maximum Practical Operating Frequency	300kHz	500kHz	500kHz	500kHz	400kHz
Outputs	Dual Alternating, Uncommitted	Dual Alternating, Uncommitted	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current		4mA			
Voltage Feedforward					
Soft Start			Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	50% / 50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note			DN-36	DN-36	
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-43	PS/3-48	PS/3-54	PS/3-61	PS/3-68

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3526A	UC3527A	UC3527B	UC3548	UCC3570
Application	Fixed Frequency PWM Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Off-line, DC-DC	Wide Range, Off-line
Topology	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Flyback, Forward	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	1%	0.75%	1%	1%
Peak Output Current	100mA	400mA	200mA	2A	500mA
Undervoltage Lockout	Y	7V	7V	13V / 10V	13V / 9V
Maximum Practical Operating Frequency	550kHz	500kHz	500kHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current				500µA	85µA
Voltage Feedforward				Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	Programmable	100%
Separate Oscillator / Synchronization Terminal	Y	Y	Y		
Application / Design Note		DN-36	DN-36		DN-48, DN-62, DN-65, U-150
Pin Count ❖	18	16	16	16	14
Page Number	PS/3-75	PS/3-54	PS/3-61	PS/3-83	PS/3-91

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC35701+	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★
Application	Wide Range DC-DC and Off-line	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM
Topology	Forward, Flyback, Buck and Boost	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback
Voltage Reference Tolerance	1%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1.2A	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A
Undervoltage Lockout	13V / 9V	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V
Maximum Practical Operating Frequency	700kHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2
Startup Current	130µA	50µA	50µA	50µA	50µA
Voltage Feedforward	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-48, DN-62, DN-65, U-150	DN-65	DN-65	DN-65	DN-65
Pin Count ❖	14	16	16	16	16
Page Number	PS/3-99	PS/3-122	PS/3-122	PS/3-122	PS/3-122

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC3581	UCC3588+	UCC3888	UCC3889	UCC3890
Application	Off-line, Primary Side PWM for ISDN Applications	Synchronous Buck Regulator with 5 Bit DAC	Off-line Power Supply Controller	Off-line Power Supply Controller	Off-line Battery Charge Controller
Topology	Forward, Flyback	Voltage Mode Synchronous Buck	Flyback	Flyback	Flyback
Voltage Reference Tolerance	1.5%	1%	3%	3%	4%
Peak Output Current	1A	1A	0.15A	0.15A	0.15A
Undervoltage Lockout	7.3V / 6.8V	10.5V / 10V	8.4V / 6.3V	8.4V / 6.3V	8.6V / 6.3V
Maximum Practical Operating Frequency	100kHz	700kHz	250kHz	250kHz	250kHz
Outputs	Single, Totem Pole	Dual NFET Synchronous	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA		150µA	150µA	
Voltage Feedforward			Y	Y	Y
Soft Start	Y	Y			
Maximum Duty Cycle	Programmable	100%	55%	55%	N/A
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note	DN-48, DN65		DN-59A, U-149A	DN-59A, DN-65, U-149A	
Pin Count ❖	14	16	8	8	8
Page Number	PS/3-131	PS/3-163	PS/3-407	PS/3-412	PS/3-418

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.

❖The smallest available pin count for thru-hole and surface mount packages.

+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC494A/AC	UC495A/AC			
Application	DC-DC	DC-DC			
Topology	Buck, Boost, Push-Pull, Half Bridge	Buck, Boost, Push-Pull, Half Bridge			
Voltage Reference Tolerance	1%	1%			
Peak Output Current	200mA	200mA			
Undervoltage Lockout	5V / 4.7V	5V / 4.7V			
Maximum Practical Operating Frequency					
Outputs	Dual Floating	Dual Floating			
Startup Current	6mA	6mA			
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle					
Separate Oscillator / Synchronization Terminal					
Special Features		On Chip 39V Zener			
Application / Design Note	DN-38	DN-38			
Pin Count ❖	16	18			
Page Number	PS/3-460	PS/3-460			

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product


UNITRODE

Simple Step-Up Fixed Voltage Regulators

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, 65V(max)
- Extended Input Voltage Range: 3.0V to 40V
- Current Mode Operation for Improved Transient Response, Line Regulation, and Current Limiting
- Soft Start Function Provides Controlled Startup
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, UVLO and Thermal Shutdown
- Improved Replacement for LM2577 Series

DESCRIPTION

The UC2577 family of devices provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide fixed output voltages of 12V or 15V as step-up regulators.

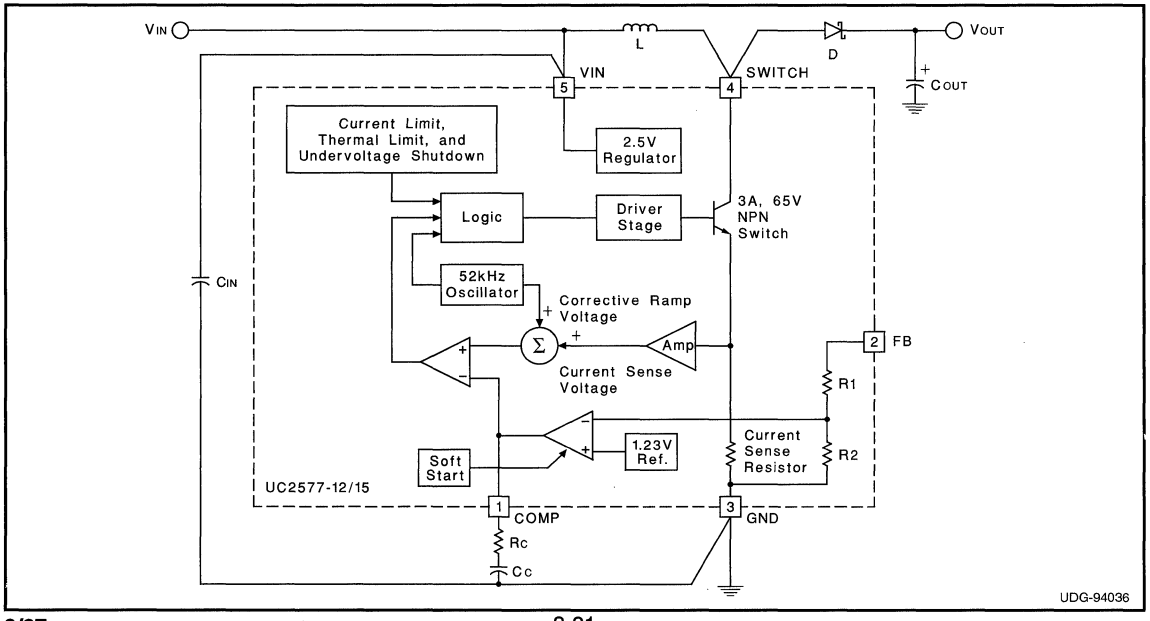
The UC2577 series features a wide input voltage range of 3.0V to 40V. An on-chip 3.0A NPN switch is included with undervoltage lockout, thermal protection circuitry, and current limiting, as well as soft start mode operation to reduce current during startup. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

For Applications Information, see the UC2577-ADJ data sheet, Design Note DN-48 "Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range", and Design Note DN-49 "UC2577 Easy Switcher Controls SEPIC Converter for Automotive Applications".

TYPICAL APPLICATIONS

- Simple Boost and Flyback Converters
- Transformer Coupled Forward Regulators
- SEPIC Topology Permits Input Voltage to be Higher or Lower than Output Voltage
- Multiple Output Designs

BLOCK DIAGRAM



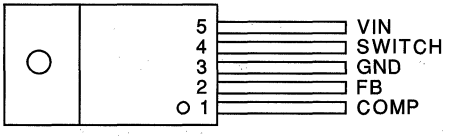
UC2577-12

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating (C = 100pF, R = 1.5kΩ) 2kV

CONNECTION DIAGRAM

5-Pin TO-220 (Top View)
T Package



Also available in TO-263 Package (TD).

RECOMMENDED OPERATING RANGE

Supply Voltage ..... 3.0V ≤ VIN ≤ 40V
Output Switch Voltage ..... 0V ≤ VSWITCH ≤ 60V
Output Switch Current ..... ISWITCH ≤ 3.0A
Junction Temperature Range ..... –40°C ≤ TJ ≤ +125°C

ORDERING INFORMATION

UC2577T-12	5 Pin TO-220 Plastic Package
UC2577T-15	5 Pin TO-220 Plastic Package
UC2577TD-12	5 Pin TO-263 Plastic Package
UC2577TD-15	5 Pin TO-263 Plastic Package

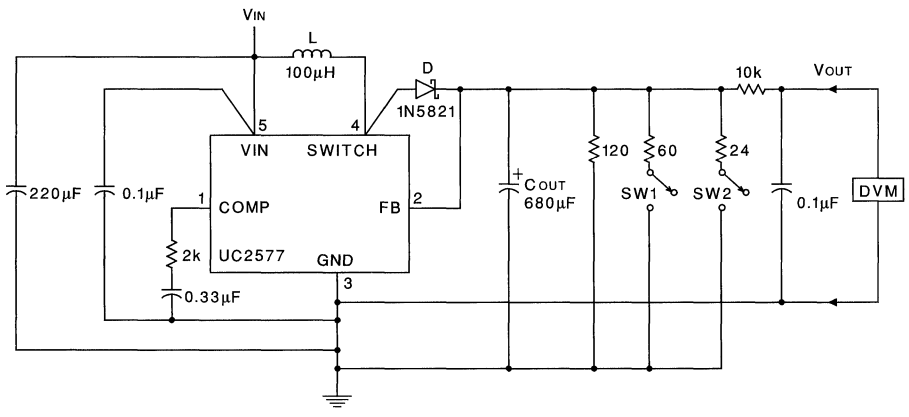
ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for TA = –40°C to +125°C, VIN = 5V, ISWITCH = 0, and TA = TJ.

		UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
System Parameters *Circuit Figure 1* (Note 3)					
Output Voltage	VIN = 5V to 10V, ILOAD = 100mA to 800mA	11.40	12.0	12.60	V
	TJ = 25°C	11.60		12.40	V
Line Regulation	VIN = 3.0V to 12V, ILOAD = 300mA		20	100	mV
	TJ = 25°C			50	mV
Load Regulation	VIN = 5V, ILOAD = 100mA to 800mA		20	100	mV
	TJ = 25°C			50	mV
Efficiency	VIN = 5V, ILOAD = 800mA		80		%
Device Parameters					
Input Supply Current	VFB = 14V (Switch Off)		7.5	14	mA
	TJ = 25°C			10	mA
	ISWITCH = 2.0A, VCOMP = 2.0V (Max Duty Cycle)		45	85	mA
	TJ = 25°C			70	mA
Input Supply UVLO	ISWITCH = 100mA		2.70	2.95	V
	TJ = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, ISWITCH = 100mA	42	52	62	kHz
	TJ = 25°C	48		56	kHz
Output Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, VCOMP = 1.0V	11.64	12	12.36	V
	TJ = 25°C	11.76		12.26	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		7		mV
FB Pin Input Resistance			9.7		kΩ
Error Amp Transconductance	ICOMP = –30μA to +30μA, VCOMP = 1.0V	145	370	615	μmho
	TJ = 25°C	225		515	μmho
Error Amp Voltage Gain	VCOMP = 0.8V to 1.6V, RCOMP = 1.0MΩ (Note 4)	25	80		V/V
	TJ = 25°C	50			V/V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, I_{SWITCH} = 0, and T_A = T_J.

		UC2577-12			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Device Parameters (cont.)					
Error Amplifier Output Swing	Upper Limit V_{FB} = 10.0V	2.0	2.4		V
	T_J = 25°C	2.2			V
	Lower Limit V_{FB} = 15.0V		0.3	0.55	V
	T_J = 25°C			0.40	V
Error Amp Output Current	V_{FB} = 10.0V to 15.0V, V_{COMP} = 10.0V	±90	±200	±400	µA
	T_J = 25°C	±130		±300	µA
Soft Start Current	V_{FB} = 10.0V, V_{COMP} = 0.5V	1.5	5.0	9.5	µA
	T_J = 25°C	2.5		7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V, I_{SWITCH} = 100mA	90	95		%
	T_J = 25°C	93			%
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA



L = 415-0930 (AIE) D = any manufacturer

Figure 1. Circuit Used to Specify System Parameters

UC2577-15

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating (C = 100pF, R = 1.5kΩ) 2kV

RECOMMENDED OPERATING RANGE

Supply Voltage ..... $3.0V \le V_{IN} \le 40V$
Output Switch Voltage ..... $0V \le V_{SWITCH} \le 60V$
Output Switch Current ..... $I_{SWITCH} \le 3.0A$
Junction Temperature Range ..... $-40°C \le T_J \le +125°C$

See Page 2 of this data sheet for Connection Diagram and Ordering Information.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, I_{SWITCH} = 0, and $T_A = T_J$.

		UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
System Parameters *Circuit Figure 2* (Note 3)					
Output Voltage	VIN = 5V to 12V, I_{LOAD} = 100mA to 600mA	14.25	15.0	15.75	V
	T_J = 25°C	14.50		15.50	V
Line Regulation	VIN = 3.0V to 12V, I_{LOAD} = 300mA		20	100	mV
	T_J = 25°C			50	mV
Load Regulation	VIN = 5V, I_{LOAD} = 100mA to 600mA		20	100	mV
	T_J = 25°C			50	mV
Efficiency	VIN = 5V, I_{LOAD} = 600mA		80		%
Device Parameters					
Input Supply Current	V_{FB} = 1.5V (Switch Off)		7.5	14	mA
	T_J = 25°C			10	mA
	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		45	85	mA
	T_J = 25°C			70	mA
Input Supply UVLO	I_{SWITCH} = 100mA		2.70	2.95	V
	T_J = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, I_{SWITCH} = 100mA	42	52	62	kHz
	T_J = 25°C	48		56	kHz
Output Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, V_{COMP} = 1.0V	14.55	15	15.44	V
	T_J = 25°C	14.70		15.30	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		10		mV
FB Pin Input Resistance			12.2		kΩ
Error Amp Transconductance	I_{COMP} = –30µA to +30µA, V_{COMP} = 1.0V	110	300	500	µmho
	T_J = 25°C	170		420	µmho
Error Amp Voltage Gain	V_{COMP} = 0.8V to 1.6V, R_{COMP} = 1.0MΩ (Note 4)	20	65		V/V
	T_J = 25°C	40			V/V
Error Amplifier Output Swing	Upper Limit V_{FB} = 12.0V	2.0	2.4		V
	T_J = 25°C	2.2			V
	Lower Limit V_{FB} = 18.0V		0.3	0.55	V
	T_J = 25°C			0.40	V
Error Amp Output Current	V_{FB} = 12.0V to 18.0V, V_{COMP} = 1.0V	±90	±200	±400	µA
	T_J = 25°C	±130		±300	µA
Soft Start Current	V_{FB} = 12.0V, V_{COMP} = 0.5V	1.5	5.0	9.5	µA
	T_J = 25°C	2.5		7.5	µA
Maximum Duty Cycle	V_{COMP} = 1.5V, I_{SWITCH} = 100mA	90	95		%
	T_J = 25°C	93			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, I_{SWITCH} = 0, and $T_A = T_J$.

		UC2577-15			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Device Parameters (cont.)					
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA

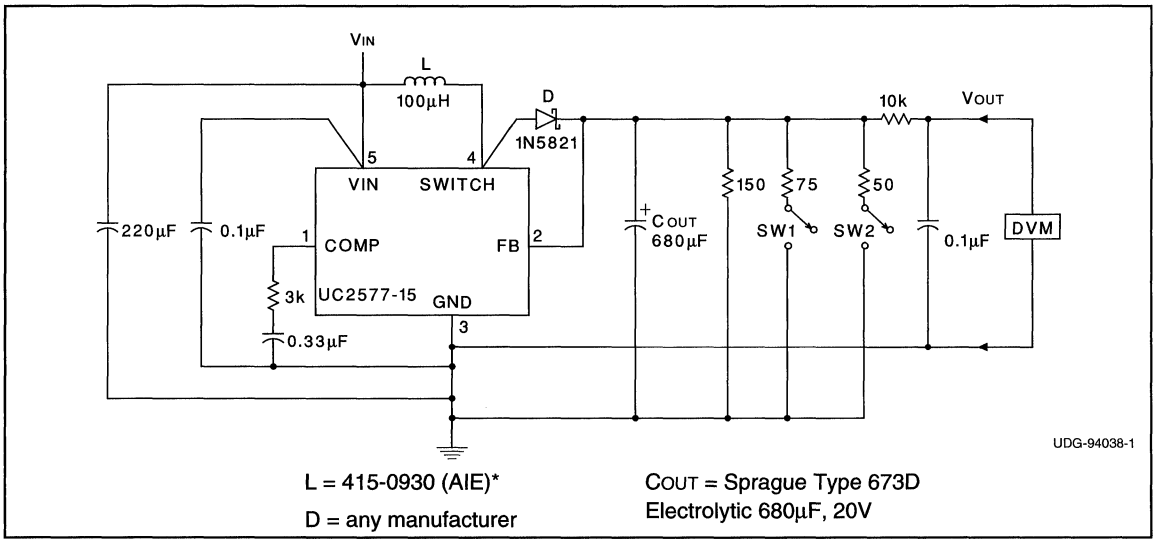


Figure 2. Circuit used to specify system parameters.

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions during which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Output current cannot be internally limited when the UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC2577 is used as a flyback or forward converter regulator.

Note 3. External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

Note 4: A 1.0MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring A_{VOL}. In actual applications, this pin's load resistance should be ≥10MΩ, resulting in AVOL that is typically twice the guaranteed minimum limit.

**(AIE) is AIE Magnetics, Div. Vernitron Corp., 2801 72nd Street North, St. Petersburg, FL 33710. Tel. (813) 347-2181*

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

Simple Step-Up Voltage Regulator

FEATURES

- Requires Few External Components
- NPN Output Switches 3.0A, 65V(max)
- Extended Input Voltage Range: 3.0V to 40V
- Current Mode Operation for Improved Transient Response, Line Regulation, and Current Limiting
- Soft Start Function Provides Controlled Startup
- 52kHz Internal Oscillator
- Output Switch Protected by Current Limit, Undervoltage Lockout and Thermal Shutdown
- Improved Replacement for LM2577-ADJ Series

TYPICAL APPLICATIONS

- Simple Boost and Flyback Converters
- SEPIC Topology Permits Input Voltage to be Higher or Lower than Output Voltage
- Transformer Coupled Forward Regulators
- Multiple Output Designs

DESCRIPTION

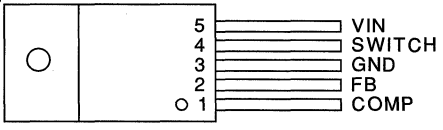
The UC2577-ADJ device provides all the active functions necessary to implement step-up (boost), flyback, and forward converter switching regulators. Requiring only a few components, these simple regulators efficiently provide up to 60V as a step-up regulator, and even higher voltages as a flyback or forward converter regulator.

The UC2577-ADJ features a wide input voltage range of 3.0V to 40V and an adjustable output voltage. An on-chip 3.0A NPN switch is included with undervoltage lockout, thermal protection circuitry, and current limiting, as well as soft start mode operation to reduce current during startup. Other features include a 52kHz fixed frequency on-chip oscillator with no external components and current mode control for better line and load regulation.

A standard series of inductors and capacitors are available from several manufacturers optimized for use with these regulators and are listed in this data sheet.

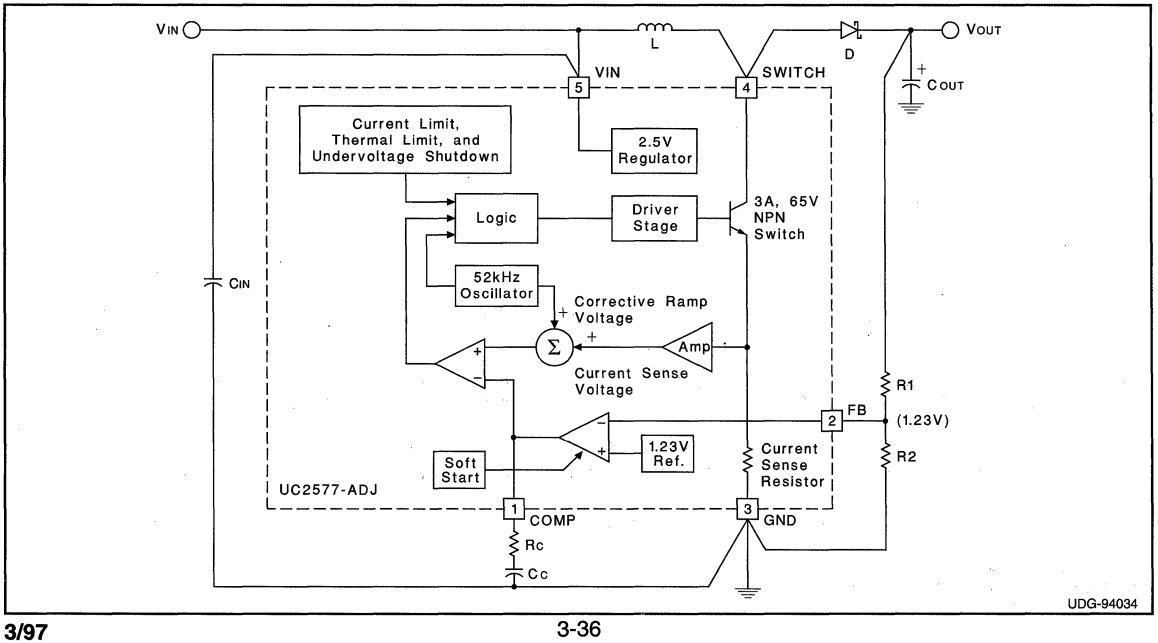
CONNECTION DIAGRAM

5-Pin TO-220 (Top View)
T Package



Also available in TO-263 Package (TD).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage 45V
Output Switch Voltage 65V
Output Switch Current (Note 2) 6.0A
Power Dissipation ..... Internally Limited
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Maximum Junction Temperature ..... 150°C
Minimum ESD Rating (C = 100pF, R = 15kΩ) 2kV

RECOMMENDED OPERATING RANGE

Supply Voltage ..... 3.0V ≤ VIN ≤ 40V
Output Switch Voltage ..... 0V ≤ VSWITCH ≤ 60V
Output Switch Current ..... ISWITCH ≤ 3.0A
Junction Temperature Range ..... –40°C ≤ TJ ≤ +125°C

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = –40°C to +125°C, VIN = 5V, VFB = VREF, ISWITCH = 0, and TA =TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
System Parameters *Circuit Figure 1* (Note 3)					
Output Voltage	VIN = 5V to 10V, ILOAD = 100mA to 800mA	11.40	12.0	12.60	V
	TJ = 25°C	11.60		12.40	V
Line Regulation	VIN = 3.0V to 10V, ILOAD = 300mA		20	100	mV
	TJ = 25°C			50	mV
Load Regulation	VIN = 5V, ILOAD = 100mA to 800mA		20	100	mV
	TJ = 25°C			50	mV
Efficiency	VIN = 5V, ILOAD = 800mA		80		%
Device Parameters					
Input Supply Current	VFB = 1.5V (Switch Off)		7.5	14	mA
	TJ = 25°C			10	mA
	ISWITCH = 2.0A, VCOMP = 2.0V (Max Duty Cycle)		45	85	mA
	TJ = 25°C			70	mA
Input Supply UVLO	ISWITCH = 100mA		2.70	2.95	V
	TJ = 25°C			2.85	V
Oscillator Frequency	Measured at SWITCH Pin, ISWITCH = 100mA	42	52	62	kHz
	TJ = 25°C	48		56	kHz
Reference Voltage	Measured at FB Pin, VIN = 3.0V to 40V, VCOMP = 1.0V	1.206	1.230	1.254	V
	TJ = 25°C	1.214		1.246	V
Reference Voltage Line Regulation	VIN = 3.0V to 40V		0.5		mV
Error Amp Input Bias Current	VCOMP = 1.0V		100	800	nA
	TJ = 25°C			300	nA
Error Amp Transconductance	ICOMP = –30µA to +30µA, VCOMP = 1.0V	1600	3700	5800	µmho
	TJ = 25°C	2400		4800	µmho
Error Amp Voltage Gain	VCOMP = 0.8V to 1.6V, RCOMP = 1.0MΩ (Note 4)	250	800		V/V
	TJ = 25°C	500			V/V
Error Amplifier Output Swing	Upper Limit VFB = 1.0V	2.0	2.4		V
	TJ = 25°C	2.2			V
	Lower Limit VFB = 1.5V		0.3	0.55	V
	TJ = 25°C			0.40	V
Error Amp Output Current	VFB = 1.0V to 1.5V, VCOMP = 1.0V	±90	±200	±400	µA
	TJ = 25°C	±130		±300	µA
Soft Start Current	VFB = 1.0V, VCOMP = 0.5V	1.5	5.0	9.5	µA
	TJ = 25°C	2.5		7.5	µA
Maximum Duty Cycle	VCOMP = 1.5V, ISWITCH = 100mA	90	95		%
	TJ = 25°C	93			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +125°C, VIN = 5V, V_{FB} = V_{REF}, I_{SWITCH} = 0, and T_A =T_J.

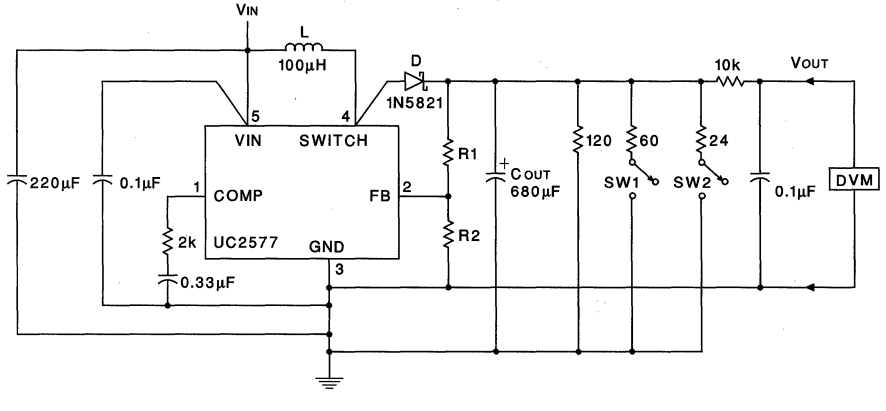
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Device Parameters (cont.)					
Switch Transconductance			12.5		A/V
Switch Leakage Current	V_{SWITCH} = 65V, V_{FB} = 1.5V (Switch Off)		10	600	µA
	T_J = 25°C			300	µA
Switch Saturation Voltage	I_{SWITCH} = 2.0A, V_{COMP} = 2.0V (Max Duty Cycle)		0.5	0.9	V
	T_J = 25°C			0.7	V
NPN Switch Current Limit	V_{COMP} = 2.0V	3.0	4.3	6.0	A
Thermal Resistance	Junction to Ambient		65		°C/W
	Junction to Case		2		°C/W
COMP Pin Current	V_{COMP} = 0		25	50	µA
	T_J = 25°C			40	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions during which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Output current cannot be internally limited when the UC2577 is used as a step-up regulator. To prevent damage to the switch, its current must be externally limited to 6.0A. However, output current is internally limited when the UC2577 is used as a flyback or forward converter regulator.

Note 3. External components such as the diode, inductor, input and output capacitors can affect switching regulator performance. When the UC2577 is used as shown in the Test Circuit, system performance will be as specified by the system parameters.

Note 4: A 1.0MΩ resistor is connected to the compensation pin (which is the error amplifier's output) to ensure accuracy in measuring AVOL. In actual applications, this pin's load resistance should be | 10MΩ, resulting in AVOL that is typically twice the guaranteed minimum limit.



L = 415-0930 (AIE)
D = any manufacturer

C_{OUT} = Sprague Type 673D
Electrolytic 680µF, 20V

R1 = 48.7k in series with 511Ω (1%)
R2 = 5.62k (1%)

Figure 1. Circuit used to specify system parameters.

APPLICATIONS INFORMATION

Step-up (Boost) Regulator

The Block Diagram shows a step-up switching regulator utilizing the UC2577. The regulator produces an output voltage higher than the input voltage. The UC2577 turns its switch on and off at a fixed frequency of 52kHz, thus storing energy in the inductor (L). When the NPN switch is on, the inductor current is charged at a rate of VIN/L. When the switch is off, the voltage at the SWITCH terminal of the inductor rises above VIN, discharging the stored current through the output diode (D) into the output capacitor (C_{OUT}) at a rate of (V_{OUT} - VIN)/L. The energy stored in the inductor is thus transferred to the output.

The output voltage is controlled by the amount of energy transferred, which is controlled by modulating the peak inductor current. This modulation is accomplished by feeding a portion of the output voltage to an error amplifier which amplifies the difference between the feedback voltage and an internal 1.23V precision reference voltage. The output of the error amplifier is then compared to a voltage proportional to the switch current, or the inductor current, during the switch on time. A comparator terminates the switch on time when the two voltages are equal and thus controls the peak switch current to maintain a constant output voltage. Figure 2 shows voltage and current waveforms for the circuit. Formulas for calculation are shown in Figure 3.

STEP-UP REGULATOR DESIGN PROCEDURE

(Refer to the block diagram) Given:

$V_{IN(min)}$ = Minimum input supply voltage

V_{OUT} = Regulated output voltage

$I_{LOAD(max)}$ = Maximum output load current

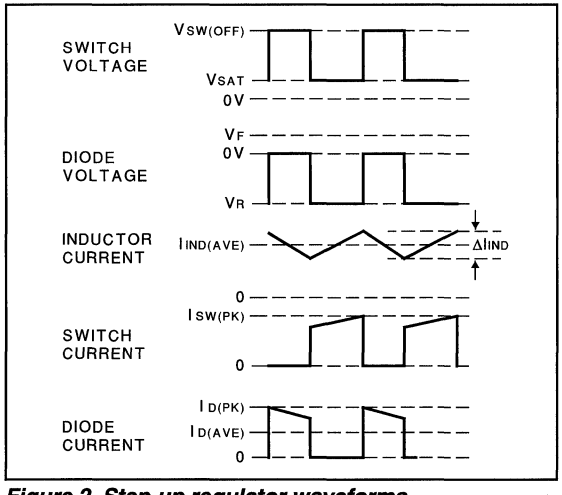


Figure 2. Step-up regulator waveforms.

Duty Cycle	D	$\frac{VOUT+VF-VIN}{VOUT+VF-VSAT}$, $\frac{VOUT-VIN}{VOUT}$
Avg. Inductor Current	$I_{IND(AVG)}$	$\frac{ILOAD}{1-D}$
Inductor Current Ripple	ΔI_{IND}	$\frac{VIN-VSAT}{L} \bullet \frac{D}{52{,}000}$
Peak Inductor Current	$I_{IND(PK)}$	$\frac{ILOAD}{1-D}+\frac{\Delta IIND}{2}$
Peak Switch Current	$I_{SW(PK)}$	$\frac{ILOAD}{1-D}+\frac{\Delta IIND}{2}$
Switch Voltage when Off	$V_{SW(OFF)}$	$V_{OUT} + V_F$
Diode Reverse Voltage	V_R	$V_{OUT} - V_{SAT}$
Avg. Diode Current	$I_{D(AVG)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$\frac{ILOAD}{1-D}+\frac{\Delta IIND}{2}$.
Power Dissipation	P_D	$0.25\Omega\left(\frac{ILOAD}{1-D}\right)^2 D+\frac{ILOAD \bullet D \bullet VIN}{50(1-D)}$
V_F = Forward Biased Diode Voltage, I_{LOAD} = Output Load Current.		

Figure 3. Step-up regulator formulas.

First, determine if the UC2577 can provide these values of V_{OUT} and $I_{LOADmax}$ when operating with the minimum value of V_{IN}. The upper limits for V_{OUT} and $I_{LOADmax}$ are given by the following equations.

$V_{OUT} \le 60V$ and

$V_{OUT} \le 10 \bullet V_{INmin}$

$$I_{LOADmax} \le \frac{2.1A \bullet VINmin}{VOUT}$$

These limits must be greater than or equal to the values specified in this application.

1. Output Voltage Section

Resistors R1 and R2 are used to select the desired output voltage. These resistors form a voltage divider and present a portion of the output voltage to the error amplifier which compares it to an internal 1.23V reference. Select R1 and R2 such that:

$$\frac{R1}{R2} = \frac{VOUT}{1.23V} - 1$$

APPLICATIONS INFORMATION (cont.)

2. Inductor Selection (L)

A. Preliminary Calculations

To select the inductor, the calculation of the following three parameters is necessary:

Dmax, the maximum switch duty cycle ($0 \le D \le 0.9$):

$$Dmax = \frac{VOUT + VF - VINmin}{VOUT + VF - 0.6V}$$

where typically V_F = 0.5V for Schottky diodes and V_F = 0.8V for fast recovery diodes.

E•T, the product of volts • time that charges the inductor:

$$E \bullet T = \frac{Dmax \bullet (VINmin - 0.6V)10^6}{52{,}000Hz} (V \bullet \mu s)$$

$I_{IND, DC}$, the average inductor current under full load:

$$IIND, DC = \frac{1.05 \bullet ILOADmax}{1 - Dmax}$$

B. Identify Inductor Value:

1. From Figure 4, identify the inductor code for the region indicated by the intersection of E•T and $I_{IND, DC}$. This code gives the inductor value in microhenries. The L or H prefix signifies whether the inductor is rated for a maximum E•T of 90Vμs (L) or 250Vμs (H).

2. If D < 0.85, go to step C. If D ≥ 0.85, calculate the minimum inductance needed to ensure the switching regulator's stability:

If L_{min} is smaller than the inductor values found in step B1, go on to step C. Otherwise, the inductor value found in step B1 is too low; an appropriate inductor code should be obtained from the graph as follows:

1.Find the lowest value inductor that is greater than Lmin.

2.Find where E•T intersects this inductor value to determine if it has an L or H prefix. If E•T intersects both the L and H regions, select the inductor with an H prefix.

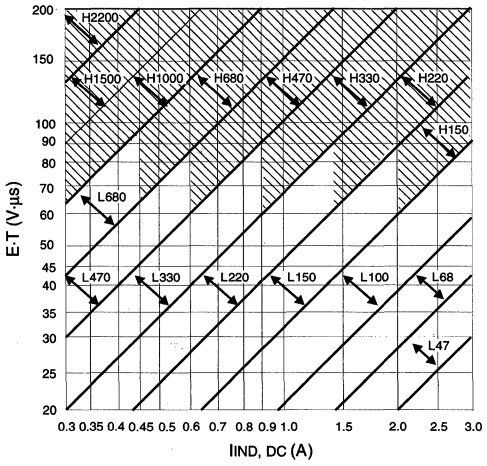
C. *Inductor Selection*

Select an inductor from the table of Figure 5 which cross references the inductor codes to the part numbers of the three different manufacturers. The inductors listed in this table have the following characteristics:

AIE (ferrite, pot-core inductors): Benefits of this type are low etectromagnetic interference (EMI), small physical size, and very low power dissipation (core loss).

Pulse (powdered iron, toroid core inductors): Benefits are low EMI and ability to withstand E•T and peak current above rated value better than ferrite cores.

Renco (ferrite, bobbin-core inductors): Benefits are low cost and best ability to withstand E•T and peak current above rated value. Be aware that these inductors generate more EMI than the other types, and this may interfere with signals sensitive to noise.



Note: This chart assumes that the inductor ripple current inductor is approximately 20% to 30% of the average inductor current (when the regulator is under full load). Greater ripple current causes higher peak switch currents and greater output ripple voltage. Lower ripple current is achieved with larger value inductors. The factor of 20% to 30% is chosen as a convenient balance between the two extremes.

Figure 4. Inductor Selection Graph

APPLICATIONS INFORMATION (cont.)

Inductor Code	Manufacturer's Part Number		
	AIE	Pulse	Renco
L47	415 - 0932	PE - 53112	RL2442
L68	415 - 0931	PE - 92114	RL2443
L100	415 - 0930	PE - 92108	RL2444
L150	415 - 0953	PE - 53113	RL1954
L220	415 - 0922	PE - 52626	RL1953
L330	415 - 0926	PE - 52627	RL1952
L470	415 - 0927	PE - 53114	RL1951
L680	415 - 0928	PE - 52629	RL1950
H150	415 - 0936	PE - 53115	RL2445
H220	430 - 0636	PE - 53116	RL2446
H330	430 - 0635	PE - 53117	RL2447
H470	430 - 0634	PE - 53118	RL1961
H680	415 - 0935	PE - 53119	RL1960
H1000	415 - 0934	PE - 53120	RL1959
H1500	415 - 0933	PE - 53121	RL1958
H2200	415 - 0945	PE - 53122	RL2448

AIE Magnetics, Div. Vernitron Corp., (813)347-2181
2801 72nd Street North, St. Petersburg, FL 33710
Pulse Engineering, (619)674-8100
12220 World Trade Drive, San Diego, CA 92128
Renco Electronics, Inc., (516)586-5566
60 Jeffryn Blvd. East, Deer Park, NY 11729

Figure 5. Table of standardized inductors and manufacturer's part numbers.

3. Compensation Network (RC, CC) and Output Capacitor (COUT) Selection

The compensation network consists of resistor RC and capacitor CC which form a simple pole-zero network and stabilize the regulator. The values of RC and CC depend upon the voltage gain of the regulator, ILOADmax, the inductor L, and output capacitance COUT. A procedure to calculate and select the values for RC, CC, and COUT which ensures stability is described below. It should be noted, however, that this may not result in optimum compensation. To guarantee optimum compensation a standard procedure for testing loop stability is recommended, such as measuring VOUT transient responses to pulsing ILOAD.

A. Calculate the maximum value for RC.

$$R_C \le \frac{750 \bullet ILOADmax \bullet VOUT^2}{VINmin^2}$$

Select a resistor less than or equal to this value, not to exceed 3kΩ.

B. Calculate the minimum value for COUT using the following two equations.

$$C_{OUT} \ge \frac{0.19 \bullet L \bullet RC \bullet ILOADmax}{VINmin \bullet VOUT} \quad \text{and}$$

$$C_{OUT} \ge \frac{VINmin \bullet RC \bullet (VINmin + (3.74 \bullet 10^5 \bullet L))}{487{,}800 \bullet VOUT^3}$$

The larger of these two values is the minimum value that ensures stability.

C. Calculate the minimum value of CC.

$$C_C \ge \frac{58.5 \bullet VOUT^2 \bullet COUT}{RC^2 \bullet VINmin}$$

The compensation capacitor is also used in the soft start function of the regulator. When the input voltage is applied to the part, the switch duty cycle is increased slowly at a rate defined by the compensation capacitor and the soft start current, thus eliminating high input currents. Without the soft start circuitry, the switch duty cycle would instantly rise to about 90% and draw large currents from the input supply. For proper soft starting, the value for CC should be equal or greater than 0.22μF.

Figure 6 lists several types of aluminum electrolytic capacitors which could be used for the output filter. Use the following parameters to select the capacitor.

Working Voltage (WVDC): Choose a capacitor with a working voltage at least 20% higher than the regulator output voltage.

Ripple Current: This is the maximum RMS value of current that charges the capacitor during each switching cycle. For step-up and flyback regulators, the formula for ripple current is:

$$I_{RIPPLE(rms)} = \frac{ILOADmax \bullet Dmax}{1 - Dmax}$$

Choose a capacitor that is rated at least 50% higher than this value at 52kHz.

Equivalent Series Resistance (ESR): This is the primary cause of output ripple voltage, and it also affects the values of RC and CC needed to stabilize the regulator. As a result, the preceding calculations for CC and RC are only valid if the ESR does not exceed the maximum value specified by the following equations.

$$ESR \le \frac{0.01 \bullet 15V}{I_{RIPPLE(P-P)}} \quad \text{and} \quad \le \frac{8.7 \bullet 10^{-3} \bullet VIN}{ILOADmax} \quad \text{where}$$

$$I_{RIPPLE(P-P)} = \frac{1.15 \bullet ILOADmax}{1 - Dmax}$$

APPLICATIONS INFORMATION (cont.)

Select a capacitor with an ESR, at 52kHz, that is less than or equal to the lower value calculated. Most electrolytic capacitors specify ESR at 120kHz which is 15% to 30% higher than at 52kHz. Also, note that ESR increases by a factor of 2 when operating at –20°C.

In general, low values of ESR are achieved by using large value capacitors (C ≥ 470µF), and capacitors with high WVDC, or by paralleling smaller value capacitors.

4. Input Capacitor Selection (C_{IN})

To reduce noise on the supply voltage caused by the switching action of a step-up regulator (ripple current noise), VIN should be bypassed to ground. A good quality 0.1µF capacitor with low ESR should provide sufficient decoupling. If the UC2577 is located far from the supply source filter capacitors, an additional electrolytic (47µF, for example) is required.

Nichicon - Types PF, PX, or PZ
927 East State Parkway, Schaumburg, IL 60173
(708) 843-7500

United Chemi-CON - Types LX, SXF, or SXJ
9801 West Higgens, Rosemont, IL 60018
(708) 696-2000

Figure 6. Aluminum electrolytic capacitors recommended for switching regulators.

5. Output Diode Selection (D)

In the step-up regulator, the switching diode must withstand a reverse voltage and be able to conduct the peak output current of the UC2577. Therefore a suitable diode must have a minimum reverse breakdown voltage greater than the circuit output voltage, and should also be rated for average and peak current greater than $I_{LOADmax}$ and I_{Dpk}. Because of their low forward voltage drop (and thus higher regulator efficiencies), Schottky barrier diodes are often used in switching regulators. Refer to Figure 7 for recommended part numbers and voltage ratings of 1A and 3A diodes.

V_{OUTmax}	Schottky		Fast Recovery	
	1A	3A	1A	3A
20V	1N5817 MBR120P	1N5820 MBR320P		
30V	1N5818 MBR130P 11DQ03	1N5821 MBR330P 31DQ03		
40V	1N5819 MBR140P 11DQ04	1N5822 MBR340P 31DQ04		
50V	MBR150 11DQ05	MBR350 31DQ05	1N4933 MUR105	
100V			1N4934 MUR110 10DL1	MR851 30DL1 MR831

MBRxxx and MURxxx are manufactured by Motorola.
1DDxxx, 11Cxx and 31Dxx are manufactured by International Rectifier

Figure 7. Diode Selection Chart

ORDERING INFORMATION

Unitrode Type Number

UC2577T-ADJ 5 Pin TO-220 Plastic Package
UC2577TD-ADJ 5 Pin TO-263 Plastic Package

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

UC1524
UC2524
UC3524

Advanced Regulating Pulse Width Modulators

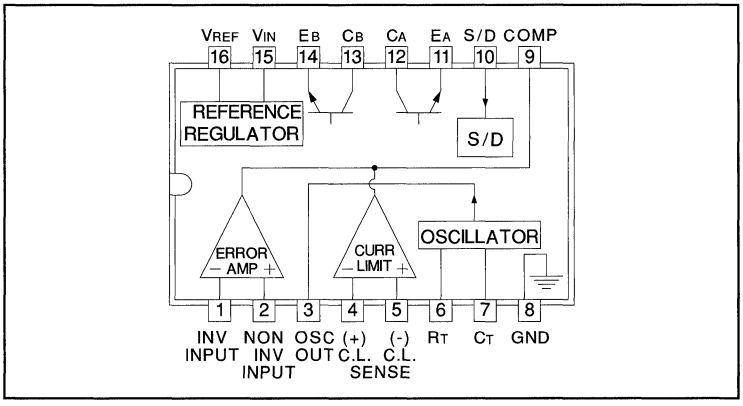
FEATURES

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for Single-ended or Push-pull Applications
- Low Standby Current...8mA Typical
- Interchangeable with SG1524, SG2524 and SG3524, Respectively

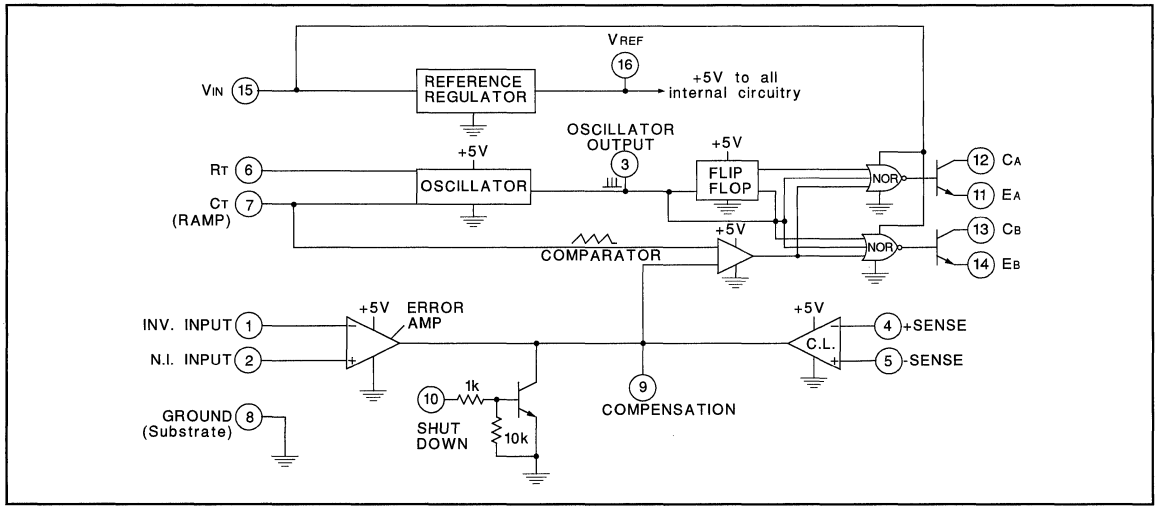
DESCRIPTION

The UC1524, UC2524 and UC3524 incorporate on a single monolithic chip all the functions required for the construction of regulating power supplies, inverters or switching regulators. They can also be used as the control element for high-power-output applications. The UC1524 family was designed for switching regulators of either polarity, transformer-coupled dc-to-dc converters, transformerless voltage doublers and polarity converter applications employing fixed-frequency, pulse-width modulation techniques. The dual alternating outputs allow either single-ended or push-pull applications. Each device includes an on-chip reference, error amplifier, programmable oscillator, pulse-steering flip-flop, two uncommitted output transistors, a high-gain comparator, and current-limiting and shut-down circuitry. The UC1524 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2524 and UC3524 are designed for operation from -25°C to +85°C and 0° to +70°C, respectively.

CONNECTION DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1524, –25°C to +85°C for the UC2524, and 0°C to +70°C for the UC3524, V_{IN} = 20V, and f = 20kHz, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1524/UC2524			UC3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Ripple Rejection	f = 120Hz, T_J = 25°C		66			66		dB
Short Circuit Current Limit	V_{REF} = 0, T_J = 25°C		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	T_J = 125°C, t = 1000 Hrs.		20			20		mV
Oscillator Section								
Maximum Frequency	C_T = .001mfd, R_T = 2kΩ		300			300		kHz
Initial Accuracy	R_T and C_T Constant		5			5		%
Voltage Stability	V_{IN} = 8 to 40V, T_J = 25°C			1			1	%
Temperature Stability	Over Operating Temperature Range			5			5	%
Output Amplitude	Pin 3, T_J = 25°C		3.5			3.5		V
Output Pulse Width	C_T = .01mfd, T_J = 25°C		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2.5V		0.5	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common Mode Voltage	T_J = 25°C	1.8		3.4	1.8		3.4	V
Common Mode Rejection Ratio	T_J = 25°C		70			70		dB
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		3			3		MHz
Output Voltage	T_J = 25°C	0.5		3.8	0.5		3.8	V
Comparator Section								
Duty-Cycle	% Each Output On	0		45	0		45	%
Input Threshold	Zero Duty-Cycle		1			1		V
	Maximum Duty-Cycle		3.5			3.5		V
Input Bias Current			1			1		µA
Current Limiting Section								
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Maximum Out, T_J = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common Mode Voltage		-1		+1	-1		+1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_{CE} = 40V		0.1	50		0.1	50	µA
Saturation Voltage	I_C = 50mA		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	17	18		17	18		V
Rise Time	R_C = 2k ohm, T_J = 25°C		0.2			0.2		µs
Fall Time	R_C = 2k ohm, T_J = 25°C		0.1			0.1		µs
Total Standby Current	V_{IN} = 40V		8	10		8	10	mA

ABSOLUTE MAXIMUM RATINGS (Note 1)

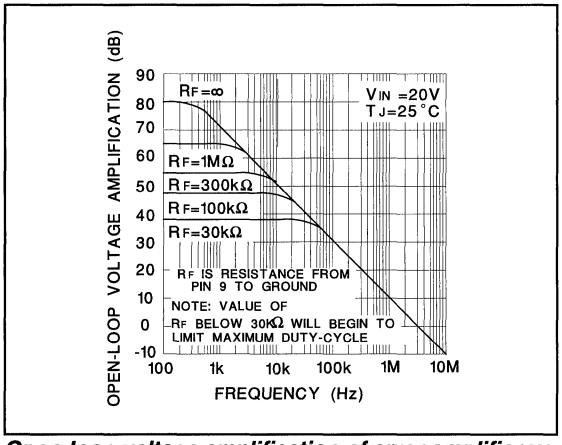
Supply Voltage, V_{CC} (Notes 2 and 3) 40V
Collector Output Current 100mA
Reference Output Current 50mA
Current Through C_T Terminal . . . . . –5mA
Power Dissipation at T_A = +25°C (Note 4) 1000mW
Power Dissipation at T_C = +25°C (Note 4) 2000mW
Operating Junction Temperature Range . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C

Note 1: Over operating free-air temperature range unless otherwise noted.
Note 2: All voltage values are with respect to the ground terminal, pin 8.
Note 3: The reference regulator may be bypassed for operation from a fixed 5V supply by connecting the V_{CC} and reference output pins both to the supply voltage. In this configuration the maximum supply voltage is 6V.
Note 4: Consult packaging section of databook for thermal limitations and considerations of package.

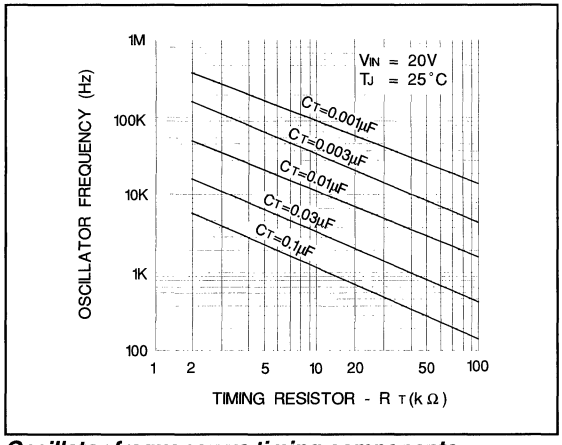
RECOMMENDED OPERATING CONDITIONS

Supply Voltage, V_{CC} . . . . . 8V to 40V
Reference Output Current . . . . . 0 to 20mA
Current through C_T Terminal . . . . . –0.03mA to –2mA
Timing Resistor, R_T . . . . . 1.8kΩ to 100kΩ
Timing Capacitor, C_T . . . . . 0.001µF to 0.1µF
Operating Ambient Temperature Range
UC1524 . . . . . –55°C to +125°C
UC2524 . . . . . –25°C to +85°C
UC3524 . . . . . 0°C to +70°C

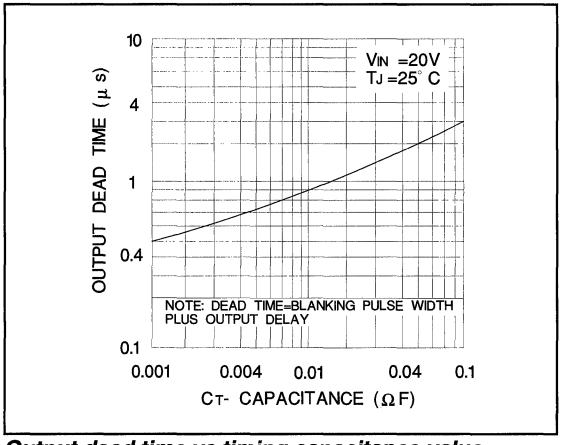
TYPICAL CHARACTERISTICS



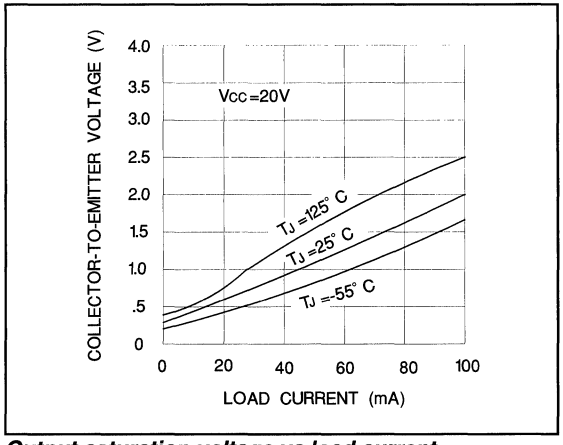
Open-loop voltage amplification of error amplifier vs frequency.



Oscillator frequency vs timing components.



Output dead time vs timing capacitance value.



Output saturation voltage vs load current.

PRINCIPLES OF OPERATION

The UC1524 is a fixed-frequency pulse-width-modulation voltage regulator control circuit. The regulator operates at a frequency that is programmed by one timing resistor (R_T), and one timing capacitor (C_T), R_T establishes a constant charging current for C_T. This results in a linear voltage ramp at C_T, which is fed to the comparator providing linear control of the output pulse width by the error amplifier. The UC1524 contains an on-board 5V regulator that serves as a reference as well as powering the UC1524's internal control circuitry and is also useful in supplying external support functions. This reference voltage is lowered externally by a resistor divider to provide a reference within the common-mode range of the error amplifier or an external reference may be used. The power supply output is sensed by a second resistor divider network to generate a feedback signal to the error amplifier. The amplifier output voltage is then compared to the linear voltage ramp at C_T. The resulting modulated pulse out of the high-gain comparator is then steered to the appropriate output pass transistor (Q_1 or Q_2) by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure both outputs are never on simultaneously during the transition times. The width of the blanking pulse is controlled by the valve of C_T. The outputs may be applied in a push-pull configuration in which their frequency is half that of the base oscillator, or paralleled for single-ended applications in which the frequency is equal to that of the oscillator. The output of the error amplifier shares a common input to the comparator with the current limiting and shutdown circuitry and can be overridden by signals from either of these inputs. This common point is also available externally and may be employed to control the gain of, or to compensate, the error amplifier or to provide additional control to the regulator.

TYPICAL APPLICATIONS DATA

Oscillator

The oscillator controls the frequency of the UC1524 and is programmed by R_T and C_T according to the approximate formula:

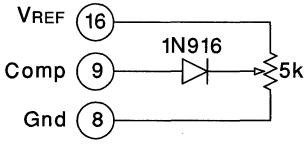
$$f \approx \frac{1.18}{RTCT}$$

where R_T is in kilohms
C_T is in microfarads
f is in kilohertz

Practical values of C_T fall between 0.001 and 0.1 microfarad. Practical values of R_T fall between 1.8 and 100 kilohms. This results in a frequency range typically from 120 hertz to 500 kilohertz.

Blanking

The output pulse of the oscillator is used as a blanking pulse at the output. This pulse width is controlled by the value of C_T. If small values of C_T are required for frequency control, the oscillator output pulse width may still be increased by applying a shunt capacitance of up to 100pF from pin 3 to ground. If still greater dead-time is required, it should be accomplished by limiting the maximum duty cycle by clamping the output of the error amplifier. This can easily be done with the circuit below:

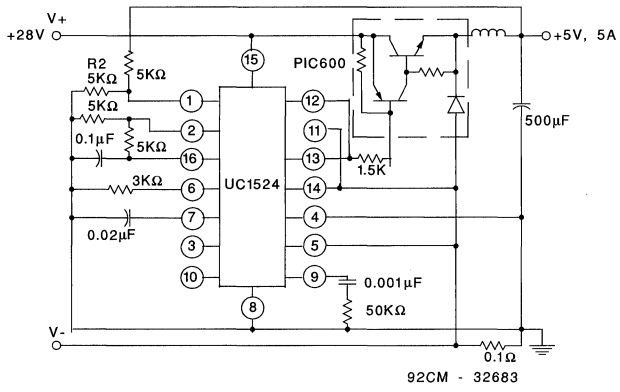


Synchronous Operation

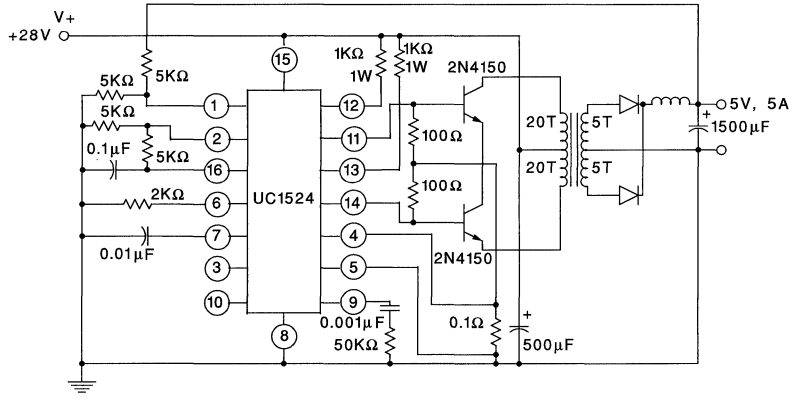
When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output terminal. The impedance to ground at this point is approximately 2 kilohms. In this configuration R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more UC1524 regulators are to operated synchronously, all oscillator output terminals should be tied together, all C_T terminals connected to single timing capacitor, and the timing resistor connected to a single R_T, terminal. The other R_T terminals can be left open or shorted to V_{REF}. Minimum lead lengths should be used between the C_T terminals.

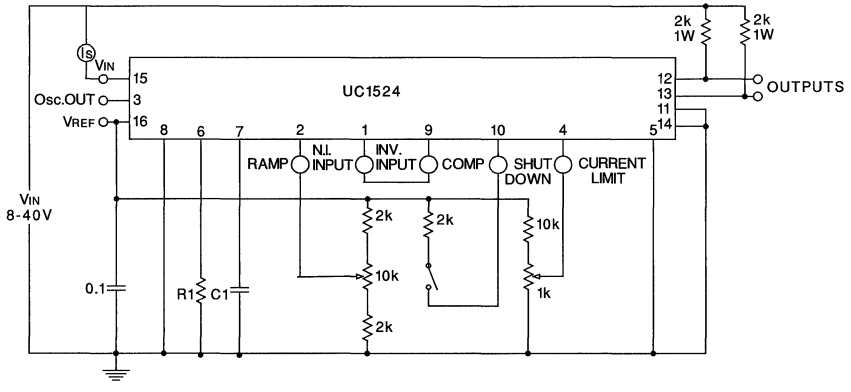
Single-Ended LC Switching Regulator Circuit



Push Pull Transformer Coupled Circuit



Open Loop Test Circuit



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Advanced Regulating Pulse Width Modulators

FEATURES

- Fully Interchangeable with Standard UC1524 Family
- Precision Reference Internally Trimmed to ±1%
- High-Performance Current Limit Function
- Under-Voltage Lockout with Hysteretic Turn-on
- Start-Up Supply Current Less Than 4mA
- Output Current to 200mA
- 60V Output Capability
- Wide Common-Mode Input Range for both Error and Current Limit Amplifiers
- PWM Latch Insures Single Pulse per Period
- Double Pulse Suppression Logic
- 200ns Shutdown through PWM Latch
- Guaranteed Frequency Accuracy
- Thermal Shutdown Protection

DESCRIPTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard UC1524 (SG1524) while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

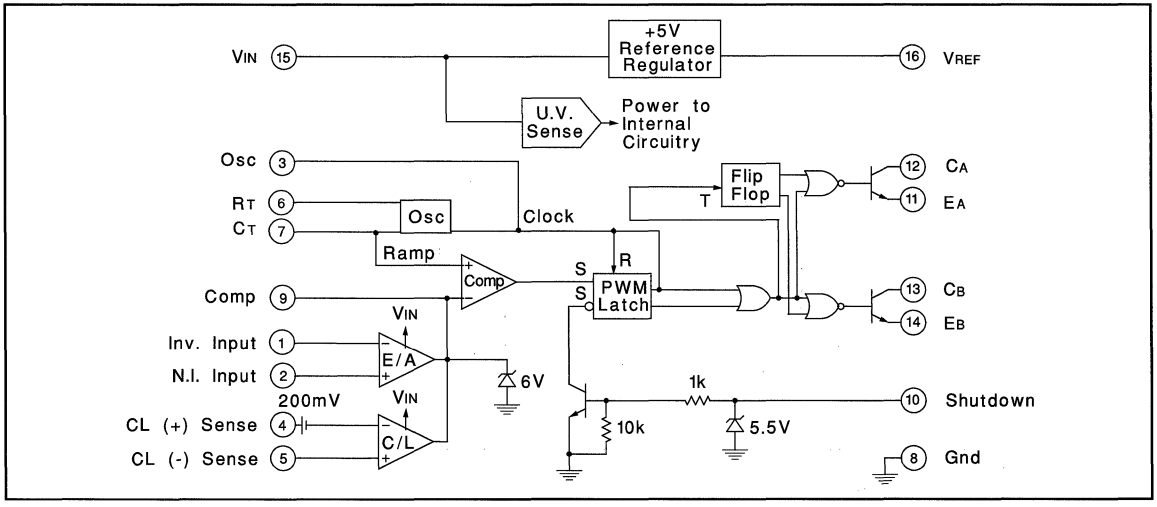
The UC1524A includes a precise 5V reference trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments; an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommitted transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter-free activation.

Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period, even in noisy environments, logic to eliminate double pulsing on a single output, a 200ns external shutdown capability, and automatic thermal protection from excessive chip temperature. The oscillator circuit of the UC1524A is usable beyond 500kHz and is now easier to synchronize with an external clock pulse.

The UC1524A is packaged in a hermetic 16-pin DIP and is rated for operation from -55°C to +125°C. The UC2524A and 3524A are available in either ceramic or plastic packages and are rated for operation from -25°C to +85°C and 0°C to 70°C, respectively. Surface mount devices are also available.

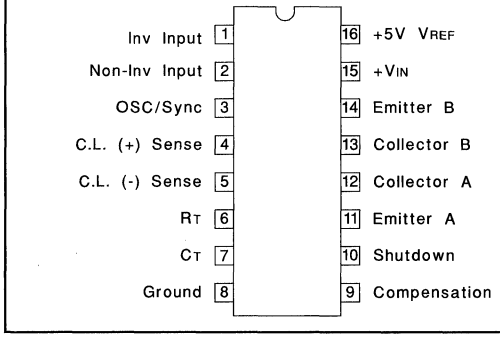
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

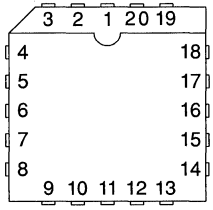
Supply Voltage (V_{IN}) 40V
Collector Supply Voltage (V_C) 60V
Output Current (each Output) 200mA
Maximum Forced Voltage (Pin 9, 10) . . . . . -3 to +5V
Maximum Forced Current (Pin 9, 10) . . . . . ±10mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature, (Soldering, 10 seconds) . . . . . +300°C
Note: Consult packaging section of Databook for thermal limitations and considerations of package.

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
Non-Inv. Input	3
OSC/SYNC	4
C.L. (+) sense	5
N/C	6
C.L. (-) sense	7
RT	8
CT	9
Ground	10
N/C	11
Compensation	12
Shutdown	13
Emitter A	14
Collector A	15
N/C	16
Collector B	17
Emitter B	18
+VIN	19
+5V VREF	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Input Voltage	Operating Range after Turn-on	8		40	8		40	V
Turn-on Threshold		6.5	7.5	8.5	6.5	7.5	8.5	V
Turn-on Current	V_{IN} = 6V		2.5	4		2.5	4	mA
Operating Current	V_{IN} = 8 to 40V		5	10		5	10	mA
Turn-on Hysteresis*			0.5			0.5		V
Reference Section								
Output Voltage	T_J = 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
	Over Operating Range	4.9		5.1	4.85		5.15	V
Line Regulation	V_{IN} = 10 to 40V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20 mA		20	25		20	35	mV
Temperature Stability*	Over Operating Range*		20	25		20	35	mV
Short Circuit Current	V_{REF} = 0, 25°C ≤ T_J ≤ 125°C		80	100		80	100	mA
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz, T_J =25°C		40			40		μVrms
Long Term Stability*	T_J =125°C, 1000 Hrs.		20	50		20	50	mV

** These parameters are guaranteed by design but not 100% tested in production.*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01 mfd)								
Initial Accuracy	T_J = 25°C	41	43	45	39	43	47	kHz
	Over Operating Range	40.2		45.9	38.2		47.9	kHz
Temperature Stability*	Over Operating Temperature Range		1	2		1	2	%
Minimum Frequency	R_T = 150kΩ, C_T = 0.1mfd			140			120	Hz
Maximum Frequency	R_T = 2.0kΩ, C_T = 470pF	500			500			kHz
Output Amplitude*		3	3.5		3	3.5		V
Output Pulse Width*		0.29	0.5	1.0	0.3	0.5	1.0	µs
Ramp Peak		3.3	3.5	3.7	3.3	3.5	3.7	V
Ramp Valley	T_J = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
Ramp Valley T.C.			-1.0			-1.0		mV/°C
Error Amplifier Section (Unless otherwise specified, V_{CM} = 2.5V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	5		1	10	µA
Input Offset Current			.05	1		0.5	1	µA
Common Mode Rejection Ratio	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	70	80		70	80		dB
Output Swing (Note 1)		5.0		0.5	5.0		0.5	V
Open Loop Voltage Gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	72	80		64	80		dB
Gain-Bandwidth*	T_J = 25°C, A_V = 0dB	1	3		1	3		MHz
DC Transconductance*§	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
P.W.M. Comparator (R_T = 2kΩ, C_T = 0.01mfd)								
Minimum Duty Cycle	V_{COMP} = 0.5V			0			0	%
Maximum Duty Cycle	V_{COMP} = 3.8V	45			45			%
Current Limit Amplifier (Unless otherwise specified, Pin 5 = 0V)								
Input Offset Voltage	T_J = 25°C, E/A Set for Maximum Output	190	200	210	180	200	220	mV
	Over Operating Temperature Range	180		220	170		230	mV
Input Bias Current			-1	-10		-1	-10	µA
Common Mode Rejection Ratio	$V_{(pin\ 5)}$ = -0.3V to + 5.5V	50	60		50	60		dB
Power Supply Rejection Ratio	V_{IN} = 10 to 40V	50	60		50	60		dB
Output Swing (Note 1)	Minimum Total Range	5.0		0.5	5.0		0.5	V
Open-Loop Voltage Gain	ΔV_O = 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
Delay Time*	Pin 4 to Pin 9, ΔV_{IN} = 300mV		300			300		ns
Output Section (Each Output)								
Collector Emitter Voltage	I_C = 100µA	60	80		60	80		V
Collector Leakage Current	V_{CE} = 50V		.1	20		.1	20	µA

** These parameters are guaranteed by design but not 100% tested in production.*

§ DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to the common mode voltage.

The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

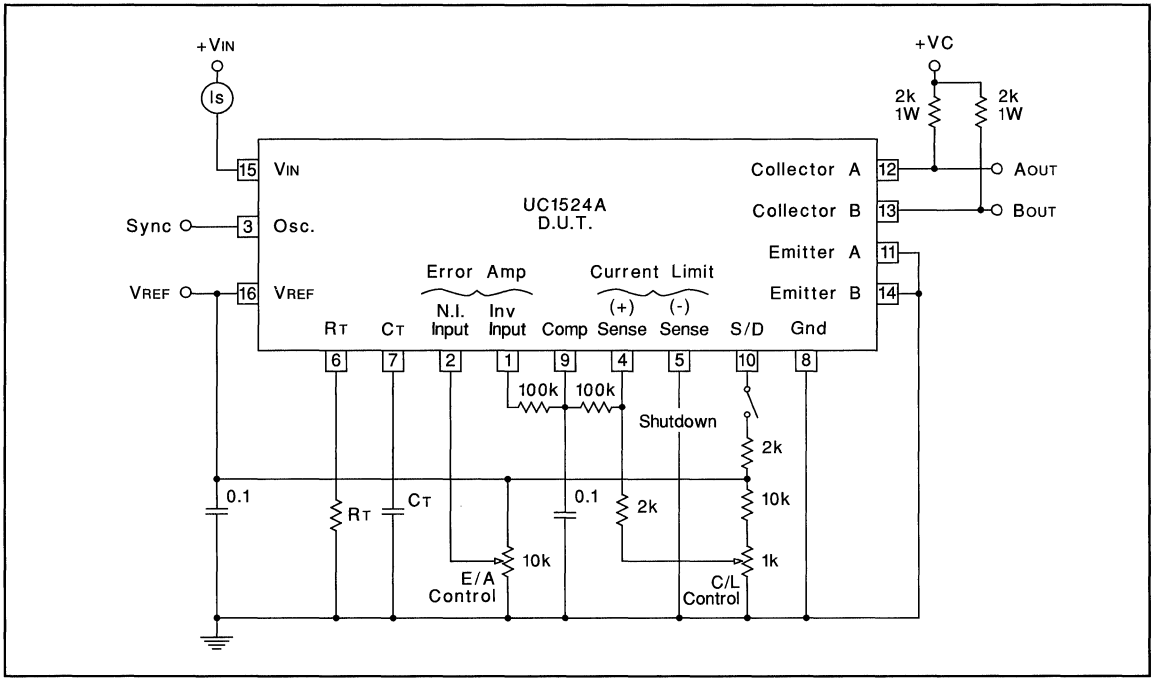
Note 1: Min Limit applies to output high level, max limit applies to output low level.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1524A, -25° to +85°C for the UC2524A, and 0°C to + 70°C for the UC3524A; V_{IN} = V_C = 20V. T_A = T_J.

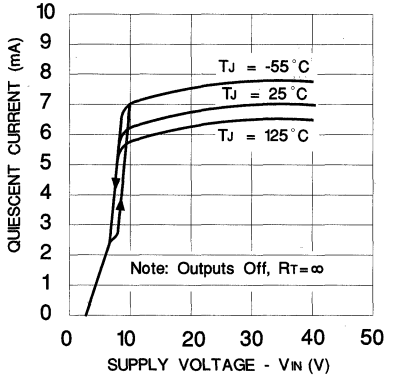
PARAMETER	TEST CONDITIONS	UC1524A / UC2524A			UC3524A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section (cont.) (Each Output)								
Saturation Voltage	I_C = 20mA		.2	.4		.2	.4	V
	I_C = 200mA		1	2.2		1	2.2	V
Emitter Output Voltage	I_E = 50mA	17	18		17	18		V
Rise Time*	T_J = 25°C, R = 2kΩ		120	400		120	400	ns
Fall Time*	T_J = 25°C, R = 2kΩ		25	200		25	200	ns
Comparator Delay*	T_J = 25°C, Pin 9 to output		300			300		ns
Shutdown Delay*	T_J = 25°C, Pin 10 to output		200			200		ns
Shutdown Threshold	T_J = 25°C, R_C = 2kΩ	0.6	.7	1.0	0.6	.7	1.0	V
S/D Threshold Over Temp.	Over Operating Temperature Range	0.4		1.2	0.4		1.0	V
Thermal Shutdown*			165			165		°C

** These parameters are guaranteed by design but not 100% tested in production.*

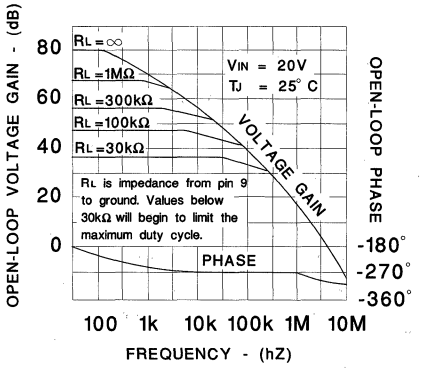
OPEN-LOOP CIRCUIT



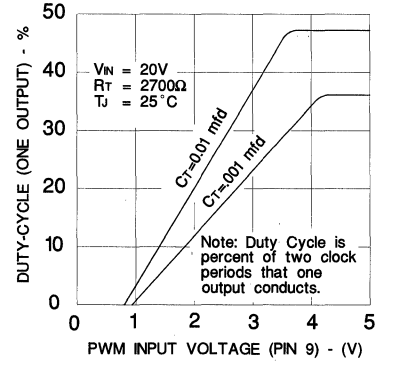
Supply Current vs Voltage



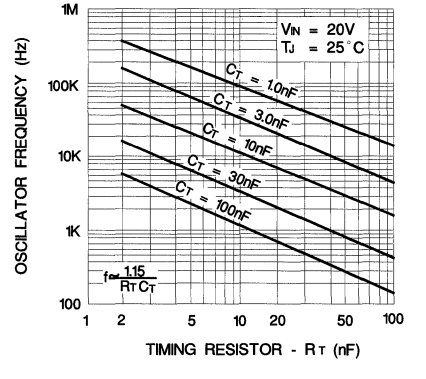
Error Amplifier Voltage Gain and Phase vs Frequency



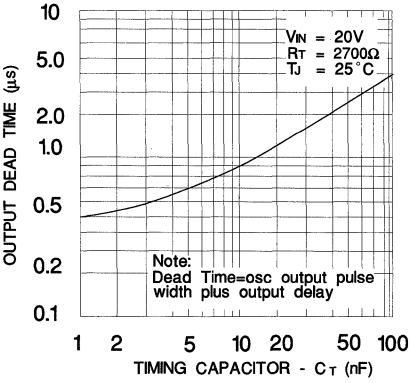
Pulse Width Modulator Transfer Function



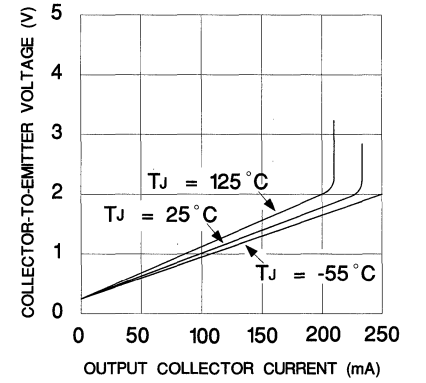
Oscillator Frequency vs Timing Components



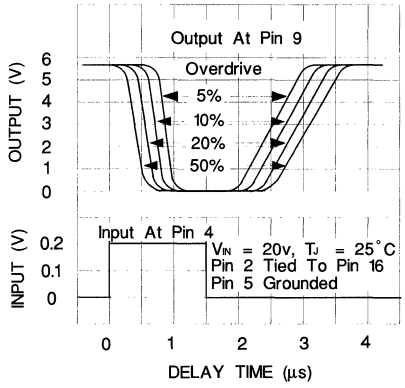
Output Dead Time vs Timing Capacitor Value



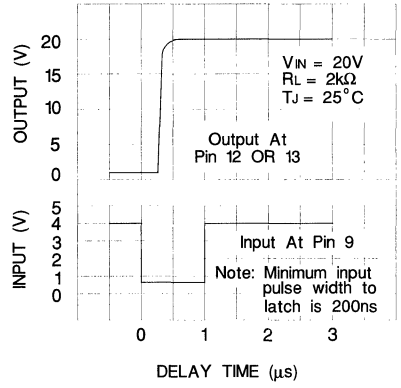
Output Saturation Voltage



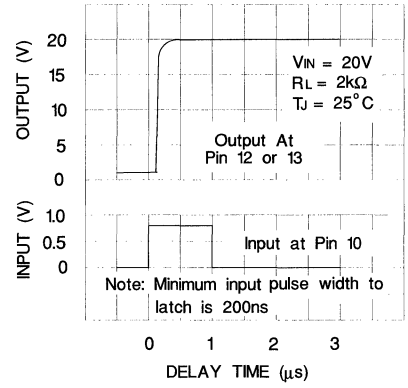
Current Limit Amplifier Delay



Shutdown Delay From PWM Comparator - Pin 9



Turn-Off Delay From Shutdown - Pin 10



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Regulating Pulse Width Modulators

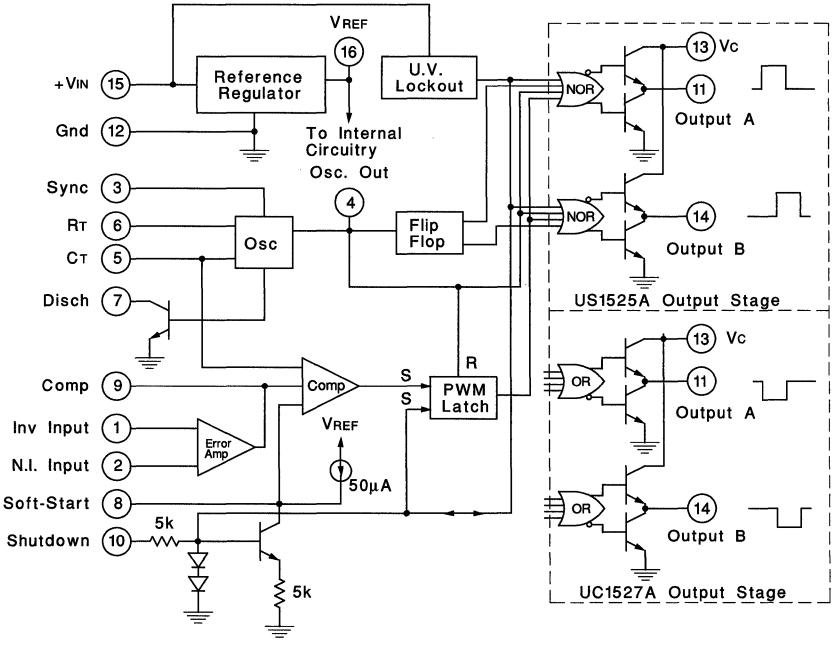
FEATURES

- 8 to 35V Operation
- 5.1V Reference Trimmed to ±1%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers

DESCRIPTION

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, (+V_{IN}) ..... +40V
Collector Supply Voltage (V_C) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +V_{IN}
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Power Dissipation at T_C = +25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.

Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

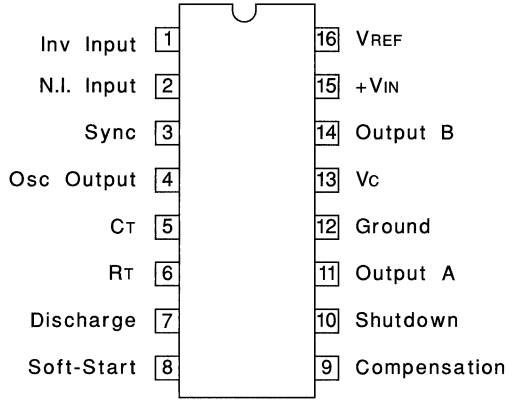
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage (+V_{IN}) ..... +8V to +35V
Collector Supply Voltage (V_C) ..... +4.5V to +35V
Sink/Source Load Current (steady state) ..... 0 to 100mA
Sink/Source Load Current (peak) ..... 0 to 400mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 100Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... .001μF to 0.1μF
Dead Time Resistor Range ..... 0 to 500Ω
Operating Ambient Temperature Range
UC1525A, UC1527A ..... -55°C to +125°C
UC2525A, UC2527A ..... -25°C to +85°C
UC3525A, UC3527A ..... 0°C to +70°C

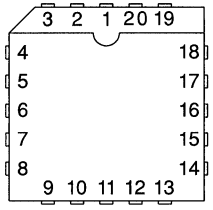
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Inv. Input	2
N.I. Input	3
SYNC	4
OSC. output	5
N/C	6
CT	7
RT	8
Discharge	9
Softstart	10
N/C	11
Compensation	12
Shutdown	13
Output A	14
Ground	15
N/C	16
VC	17
Output B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +V_{IN} = 20V, and over operating temperature, unless otherwise specified, $T_A = T_J$

PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN} = 8 to 35V		10	20		10	20	mV
Load Regulation	I_L = 0 to 20mA		20	50		20	50	mV
Temperature Stability (Note 5)	Over Operating Range		20	50		20	50	
Total Output Variation (Note 5)	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Shorter Circuit Current	V_{REF} = 0, T_J = 25°C		80	100		80	100	mA
Output Noise Voltage (Note 5)	10Hz ≤ 10kHz, T_J = 25°C		40	200		40	200	μVrms
Long Term Stability (Note 5)	T_J = 125°C		20	50		20	50	mV
Oscillator Section (Note 6)								
Initial Accuracy (Notes 5 & 6)	T_J = 25°C		± 2	± 6		± 2	± 6	%
Voltage Stability (Notes 5 & 6)	V_{IN} = 8 to 35V		± 0.3	± 1		± 1	± 2	%
Temperature Stability (Note 5)	Over Operating Range		± 3	± 6		± 3	± 6	%
Minimum Frequency	R_T = 200kΩ, C_T = 0.1μF			120			120	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 5 & 6)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 5 & 6)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (V_{CM} = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	μA
Input Offset Current				1			1	μA
DC Open Loop Gain	R_L ≥ 10MΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 5)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
DC Transconductance (Notes 5 & 7)	T_J = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.1	1.5		1.1	1.5		mS
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5 to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	V_{IN} = 8 to 35V	50	60		50	60		dB

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at f_{OSC} = 40kHz (R_T = 3.6kΩ, C_T = 0.01μF, R_D = 0Ω). Approximate oscillator frequency is defined by:

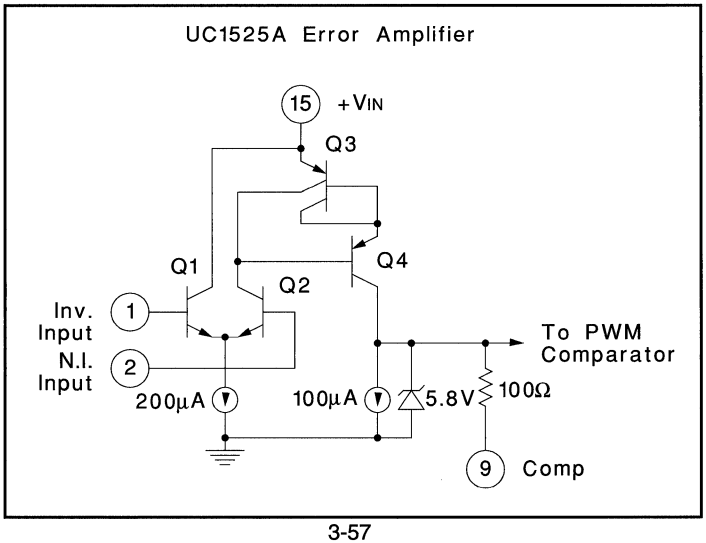
$$f = \frac{1}{C_T (0.7RT + 3R_D)}$$

Note 7: DC transconductance (g_M) relates to DC open-loop voltage gain (A_V) according to the following equation: $A_V = g_M R_L$ where R_L is the resistance from pin 9 to ground..
The minimum g_M specification is used to calculate minimum A_V when the error amplifier output is loaded.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 20V, and over operating temperature, unless otherwise specified, $T_A = T_J$

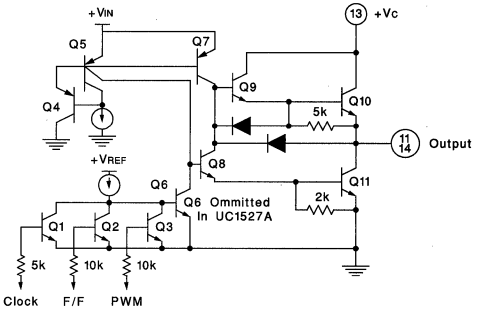
PARAMETER	TEST CONDITIONS	UC1525A/UC2525A UC1527A/UC2527A			UC3525A UC3527A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
PWM Comparator								
Minimum Duty-Cycle				0			0	%
Maximum Duty-Cycle		45	49		45	49		%
Input Threshold (Note 6)	Zero Duty-Cycle	0.7	0.9		0.7	0.9		V
	Maximum Duty-Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 5)			.05	1.0		.05	1.0	µA
Shutdown Section								
Soft Start Current	V_{SD} = 0V, V_{SS} = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	V_{SD} = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, V_{SS} = 5.1V, T_J = 25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	V_{SD} = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 5)	V_{SD} = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (V_C = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output High Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Under-Voltage Lockout	V_{COMP} and V_{SS} = High	6	7	8	6	7	8	V
V_C OFF Current (Note 7)	V_C = 35V			200			200	µA
Rise Time (Note 5)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 5)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Total Standby Current								
Supply Current	V_{IN} = 35V		14	20		14	20	mA

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 6: Tested at f_{OSC} = 40kHz (R_T = 3.6kΩ, C_T = 0.01µF, R_D = 0Ω).
Note 7: Collector off-state quiescent current measured at pin 13 with outputs low for UC1525A and high for UC1527A.

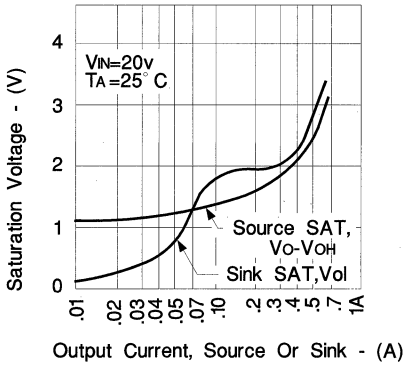


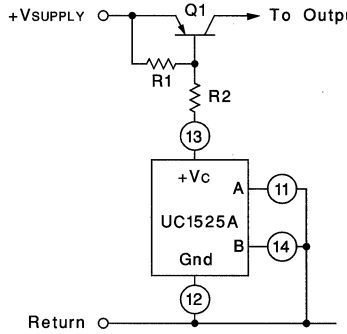
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525A Output Circuit (1/2 Circuit Shown)

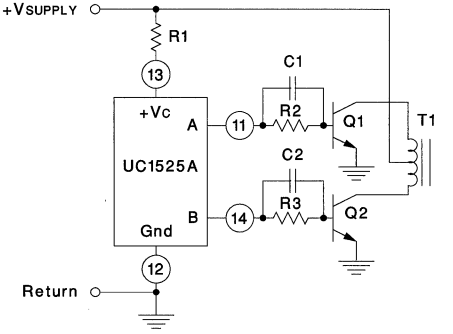


UC1525A Output Saturation Characteristics

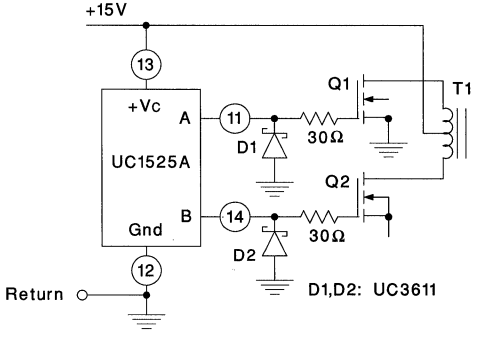




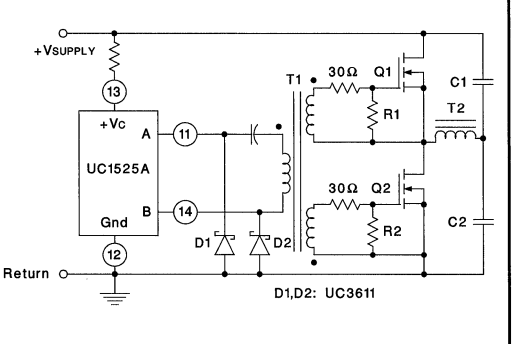
For single-ended supplies, the driver outputs are grounded. The Vc terminal is switched to ground by the totem-pole source transistors on alternate oscil-



In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with

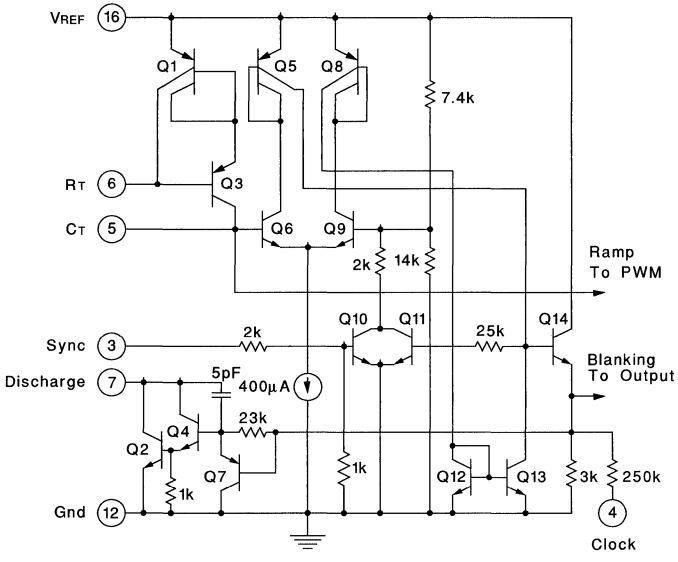


The low source impedance of the output drivers provides rapid charging of power FET Input capaci-



Low power transformers can be driven by the UC1525A. Automatic reset occurs during dead

UC1525A Oscillator Schematic



PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTIC SHUTDOWN OPTIONS

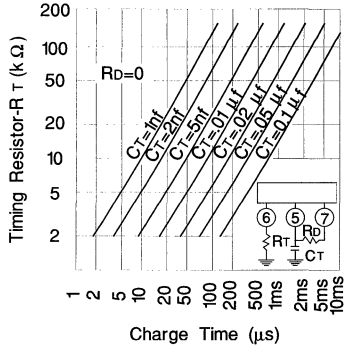
(See Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

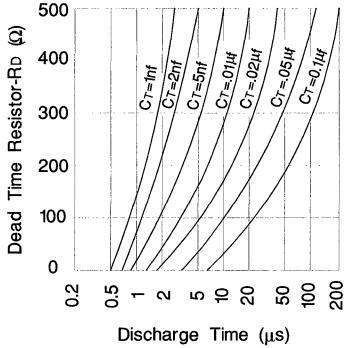
An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions; the PWM latch is immediately set providing the fastest turn-off signal to the outputs; and a 150µA-current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

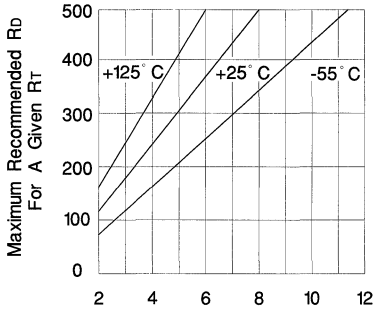
Oscillator Charge Time vs RT and CT



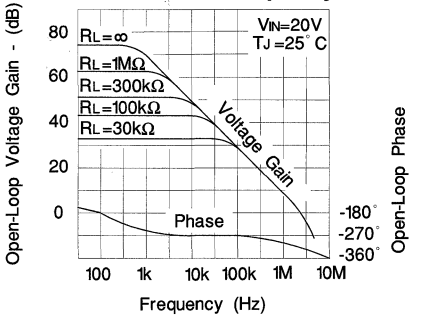
Oscillator Discharge Time vs RD and CT



Maximum Value RD vs Minimum Value RT

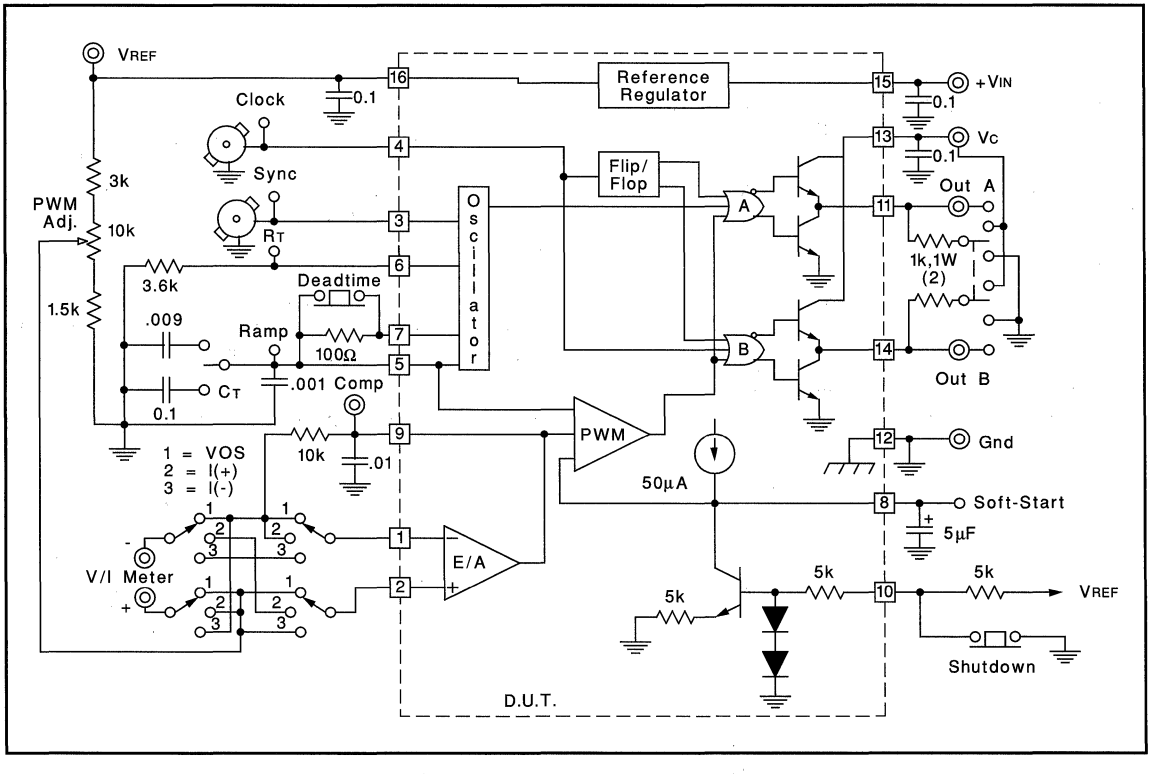


Error Amplifier Voltage Gain and Phase vs Frequency



RL is impedance from pin 9 to ground. Values below

LAB TEST FIXTURE



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application INFO available

UC1525B UC1527B
UC2525B UC2527B
UC3525B UC3527B

Regulating Pulse Width Modulators

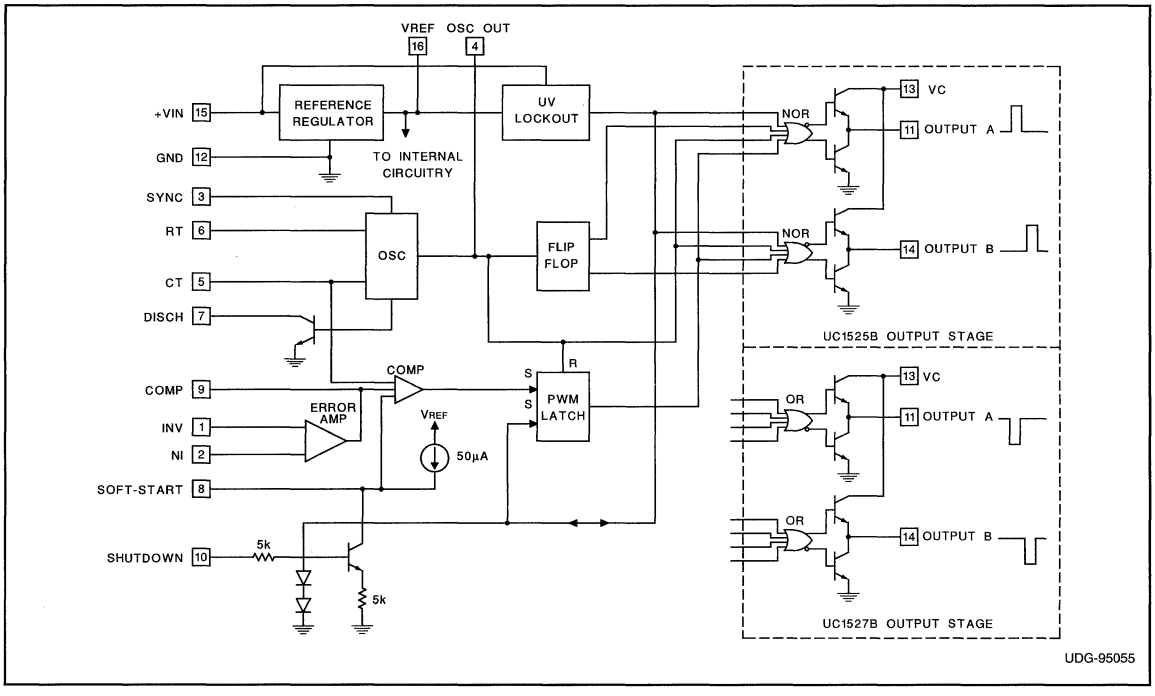
FEATURES

- 8 to 35V Operation
- 5.1V Buried Zener Reference Trimmed to ±0.75%
- 100Hz to 500kHz Oscillator Range
- Separate Oscillator Sync Terminal
- Adjustable Deadtime Control
- Internal Soft-Start
- Pulse-by-Pulse Shutdown
- Input Undervoltage Lockout with Hysteresis
- Latching PWM to Prevent Multiple Pulses
- Dual Source/Sink Output Drivers
- Low Cross Conduction Output Stage
- Tighter Reference Specifications

DESCRIPTION

The UC1525B/1527B series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V buried zener reference is trimmed to ±0.75% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state. The UC1527B utilizes OR logic which results in a HIGH output level when OFF.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, (+VIN) . . . . . +40V
Collector Supply Voltage (VC) . . . . . +40V
Logic Inputs . . . . . –0.3V to +5.5V
Analog Inputs . . . . . –0.3V to VIN
Output Current, Source or Sink 500mA
Reference Output Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at T_A = +25°C 1000mW
Power Dissipation at T_C = +25°C 2000mW
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

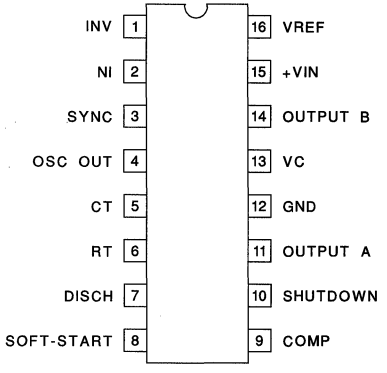
RECOMMENDED OPERATING CONDITIONS (Note 1)

Input Voltage (+VIN) . . . . . +8V to +35V
Collector Supply Voltage (VC) . . . . . +4.5V to +35V
Sink/Source Load Current (steady state) . . . . . 0 to 100mA
Sink/Source Load Current (peak) . . . . . 0 to 400mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 100Hz to 400kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 0.001µF to 0.1µF
Dead Time Resistor Range . . . . . 0Ω to 500Ω

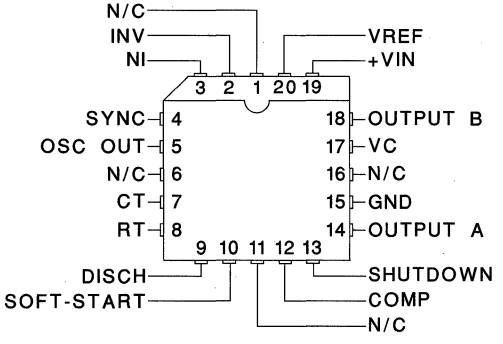
Note 1: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



LCC-20, PLCC-20 (Top View)
L, Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	5.062	5.10	5.138	5.036	5.10	5.164	V
Line Regulation	VIN = 8V to 35V		5	10		5	10	mV
Load Regulation	I_L = 0mA to 20mA		7	15		7	15	mV
Temperature Stability (Note 2)	Over Operating Range		10	50		10	50	mV
Total Output Variation	Line, Load, and Temperature	5.036		5.164	5.024		5.176	V
Short Circuit Current	VREF = 0, T_J =25°C		80	100		80	100	mA
Output Noise Voltage (Note 2)	10Hz ≤ f ≤10kHz, T_J = 25°C		40	200		40	200	µVrms
Long Term Stability (Note 2)	T_J = 125°C, 1000 Hrs.		3	10		3	10	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 3)								
Initial Accuracy (Notes 2 & 3)	T_J = 25°C		±2	±6		±2	±6	%
Voltage Stability (Notes 2 & 3)	VIN = 8V to 35V		±0.3	±1		±1	±2	%
Temperature Stability (Note 2)	Over Operating Range		±3	±6		±3	±6	%
Minimum Frequency	RT = 200kΩ, CT = 0.1µF			120			120	Hz
Maximum Frequency	RT = 2kΩ, CT = 470pF	400			400			kHz
Current Mirror	I_{RT} = 2mA	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude (Notes 2 & 3)		3.0	3.5		3.0	3.5		V
Clock Width (Notes 2 & 3)	T_J = 25°C	0.3	0.5	1.0	0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V		1.0	2.5		1.0	2.5	mA
Error Amplifier Section (VCM = 5.1V)								
Input Offset Voltage			0.5	5		2	10	mV
Input Bias Current			1	10		1	10	µA
Input Offset Current				1			1	µA
DC Open Loop Gain	RL ≥ 10 MegΩ	60	75		60	75		dB
Gain-Bandwidth Product (Note 2)	A_V = 0dB, T_J = 25°C	1	2		1	2		MHz
Output Low Level			0.2	0.5		0.2	0.5	V
Output High Level		3.8	5.6		3.8	5.6		V
Common Mode Rejection	V_{CM} = 1.5V to 5.2V	60	75		60	75		dB
Supply Voltage Rejection	VIN = 8V to 35V	50	60		50	60		dB
PWM Comparator								
Minimum Duty Cycle				0			0	%
Maximum Duty Cycle		45	49		45	49		%
Input Threshold (Note 3)	Zero Duty Cycle	0.7	0.9		0.7	0.9		V
Input Threshold (Note 3)	Maximum Duty Cycle		3.3	3.6		3.3	3.6	V
Input Bias Current (Note 2)			0.05	1.0		0.05	1.0	µA
Shutdown Section								
Soft Start Current	$V_{SHUTDOWN}$ = 0V, $V_{SOFTSTART}$ = 0V	25	50	80	25	50	80	µA
Soft Start Low Level	$V_{SHUTDOWN}$ = 2.5V		0.4	0.7		0.4	0.7	V
Shutdown Threshold	To outputs, $V_{SOFTSTART}$ = 5.1V, T_J =25°C	0.6	0.8	1.0	0.6	0.8	1.0	V
Shutdown Input Current	$V_{SHUTDOWN}$ = 2.5V		0.4	1.0		0.4	1.0	mA
Shutdown Delay (Note 2)	$V_{SHUTDOWN}$ = 2.5V, T_J = 25°C		0.2	0.5		0.2	0.5	µs
Output Drivers (Each Output) (Vc = 20V)								
Output Low Level	I_{SINK} = 20mA		0.2	0.4		0.2	0.4	V
	I_{SINK} = 100mA		1.0	2.0		1.0	2.0	V
Output HIgh Level	I_{SOURCE} = 20mA	18	19		18	19		V
	I_{SOURCE} = 100mA	17	18		17	18		V
Undervoltage Lockout	V_{COMP} and $V_{SOFTSTART}$ = High	6	7	8	6	7	8	V
Collector Leakage	VC = 35V			200			200	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1525B and UC1527B; –40°C to +85°C for the UC2525B and UC2527B; 0°C to +70°C for the UC3525B and UC3527B; +VIN = 20V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1525B/UC2525B UC1527B/UC2527B			UC3525B UC3527B			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Drivers (Each Output) (VC = 20V) (cont.)								
Rise Time (Note 2)	C_L = 1nF, T_J = 25°C		100	600		100	600	ns
Fall Time (Note 2)	C_L = 1nF, T_J = 25°C		50	300		50	300	ns
Cross conduction charge	Per cycle, T_J = 25°C		30			30		nc
Total Standby Current								
Supply Current	VIN = 35V		14	20		14	20	mA

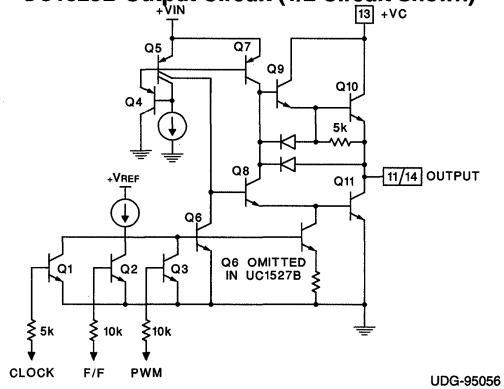
Note 2: Guaranteed by design. Not 100% tested in production.

Note 3: Tested at fosc= 40kHz (R_T = 3.6Ω, C_T = 0.01µF, R_D = 0Ω). Approximate oscillator frequency is defined by:

$$f = \frac{1}{C_T \bullet (0.7 \bullet R_T + 3R_D)}$$

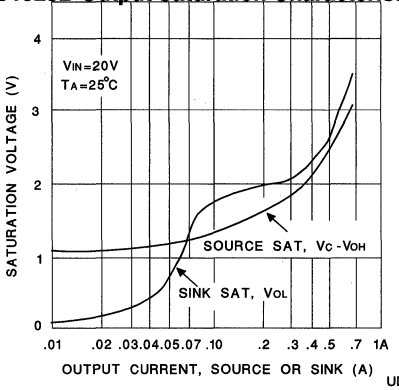
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

UC1525B Output Circuit (1/2 Circuit Shown)

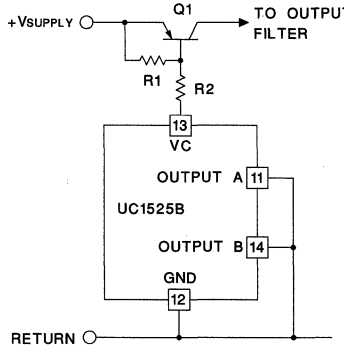


UDG-95056

UC1525B Output Saturation Characteristics

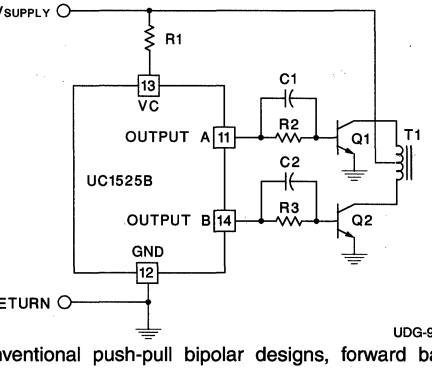


UDG-95057



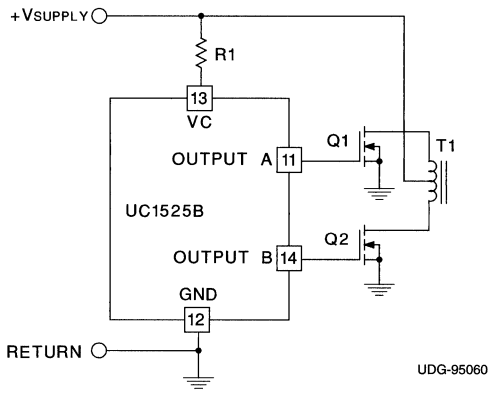
UDG-95058

For single-ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

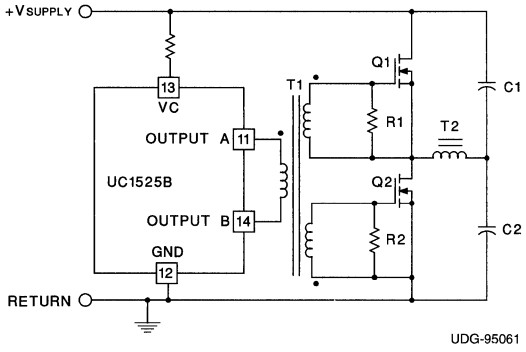


UDG-95059

In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C, and C2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

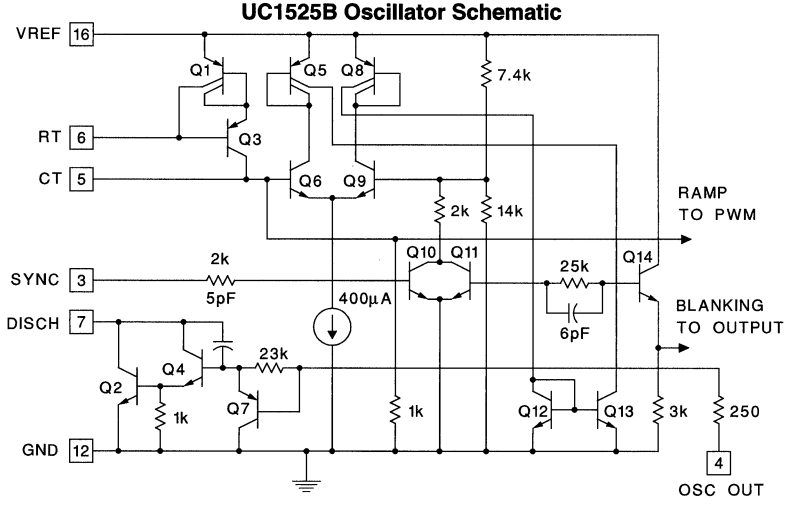
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

Shutdown Options (See Block Diagram)

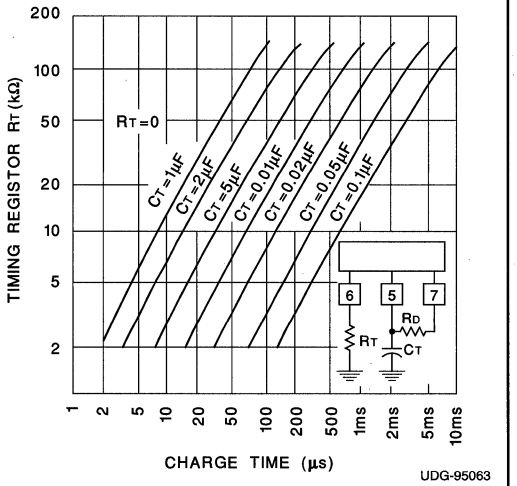
Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

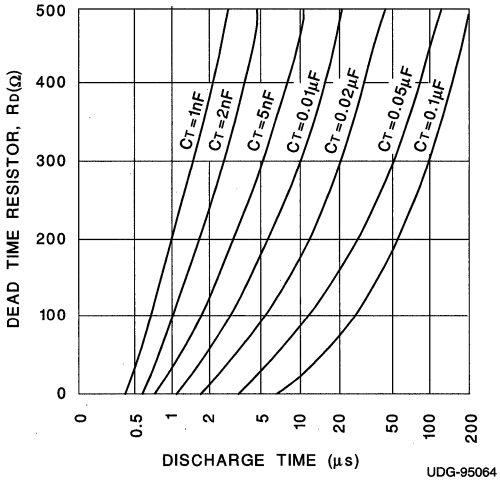
UC1525B Oscillator Schematic



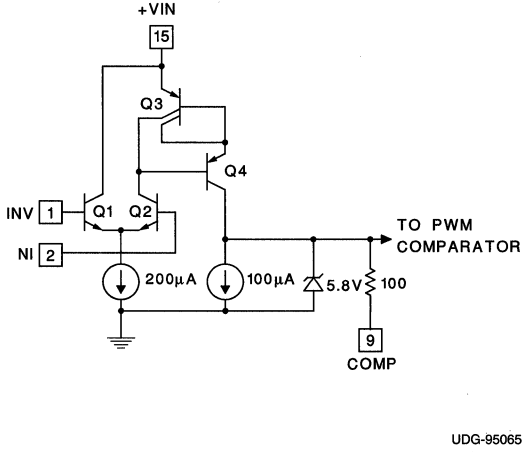
Oscillator Charge Time vs. R_T and C_T



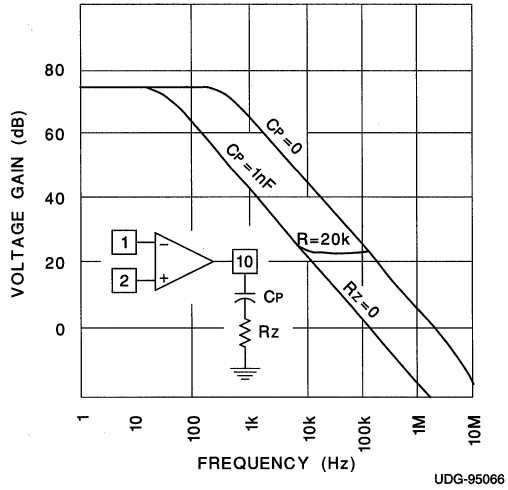
Oscillator Discharge Time vs. R_D and C_T



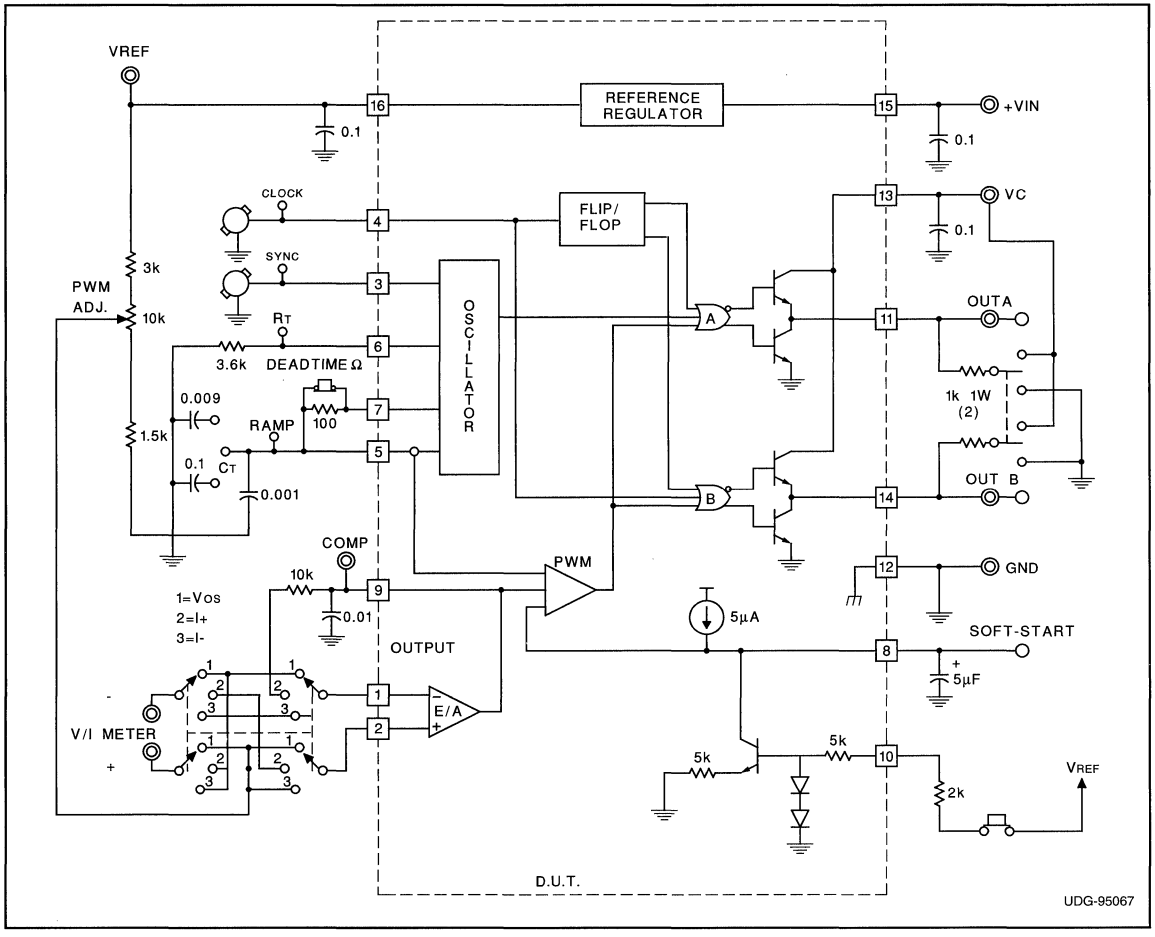
UC1525B Error Amplifier



Error Amplifier Open-Loop Frequency Response



LAB TEST FIXTURE



UNITRODE CORPORATION
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TEL. (603) 424-2410 • FAX (603) 424-3460

Regulating Pulse Width Modulator

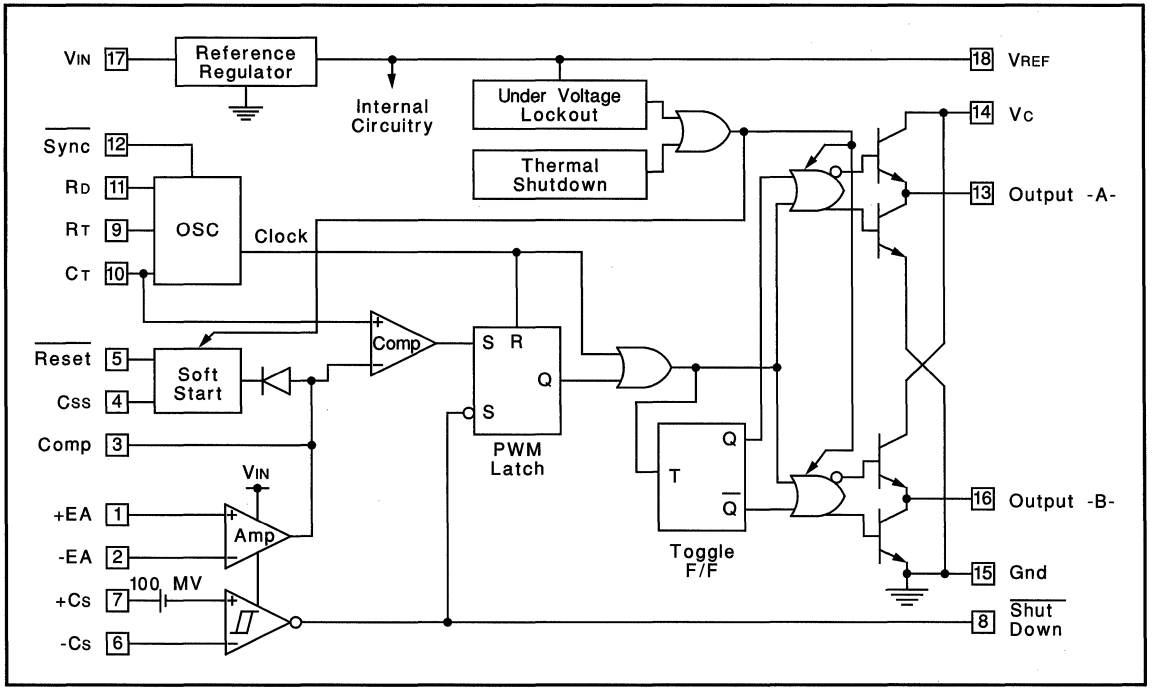
FEATURES

- 8 To 35V Operation
- 5V Reference Trimmed To ±1%
- 1Hz To 400kHz Oscillator Range
- Dual 100mA Source/Sink Outputs
- Digital Current Limiting
- Double Pulse Suppression
- Programmable Deadtime
- Under-Voltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- TTL/CMOS Compatible Logic Ports
- Symmetry Correction Capability
- Guaranteed 6 Unit Synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and setting logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2526 is characterized for operation from -25°C to +85°C, and the UC3526 is characterized for operation from 0° to +70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+VIN) ..... +40V
Collector Supply Voltage (+VC) ..... +40V
Logic Inputs ..... -0.3V to +5.5V
Analog Inputs ..... -0.3V to +VIN
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at TC = +25°C (Note 2) 3000mW
Operating Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging section of databook for thermal limitations and considerations of package.

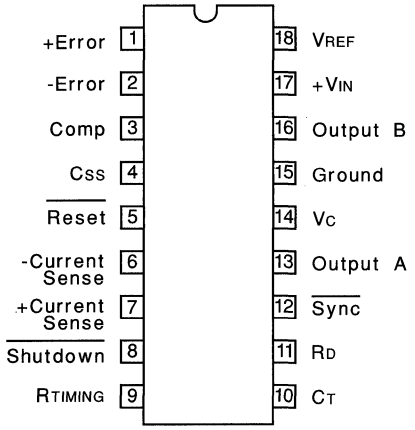
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage ..... +8V to +35V
Collector Supply Voltage ..... +4.5V to +35V
Sink/Source Load Current (each output) ..... 0 to 100mA
Reference Load Current ..... 0 to 20mA
Oscillator Frequency Range ..... 1Hz to 400kHz
Oscillator Timing Resistor ..... 2kΩ to 150kΩ
Oscillator Timing Capacitor ..... 1nF to 20µF
Available Deadtime Range at 40kHz ..... 3% to 50%
Operating Ambient Temperature Range
UC1526 ..... -55°C to +125°C
UC2526 ..... -25°C to +85°C
UC3526 ..... -0°C to +70°C

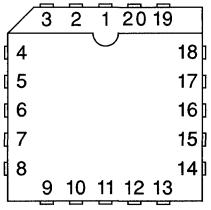
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+Error	2
-Error	3
Comp.	4
Css	5
Reset	6
- Current Sense	7
+ Current Sense	8
Shutdown	9
RTIMING	10
CT	11
RD	12
Sync	13
Output A	14
VC	15
N/C	16
Ground	17
Output B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	TJ = + 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+VIN = 8 to 35V		10	20		10	30	mV
Load Regulation	IL = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating TJ		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	VREF = 0V	25	50	100	25	50	100	mA
Under -Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	VREF = 3.8V		0.2	0.4		0.2	0.4	V
	VREF = 4.8V	2.4	4.8		2.4	4.8		V

Note 4: IL = 0mA.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 5)								
Initial Accuracy	T_J = + 25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20µF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 6)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	V_{PIN1}-V_{PIN2} ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V_{PIN2}-V_{PIN1} ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 12kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 5)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} =40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	µA
Current Limit Comparator (Note 7)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ =+2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 8)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
Power Consumption (Note 9)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		18	30		18	30	mA

Note 4: I_L = 0mA.
Note 5: F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.1µF ± 1%, R_D = 0Ω)
Note 6: V_{CM} = 0 to +5.2V
Note 8: V_C = +15V
Note 9: +V_{IN} = +35V, R_T = 4.12kΩ

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

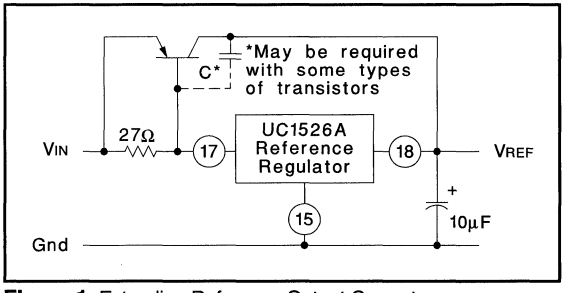


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

Soft-Start Circuit

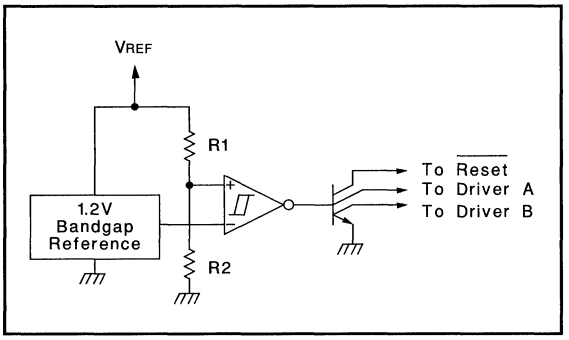


Figure 2. Under-Voltage Lockout Schematic

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100mA current source to charge CS. Q2 clamps the error amplifier output to 1VBE above the voltage on CS. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

Digital Control Ports

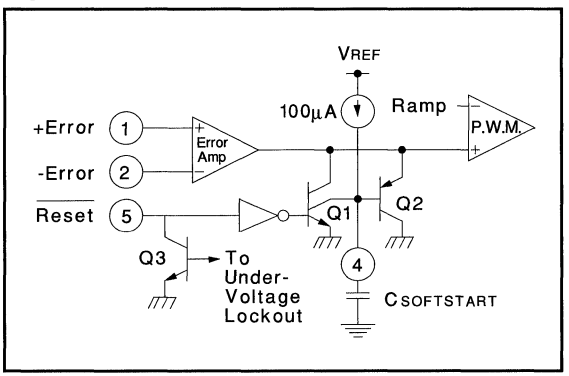


Figure 3. Soft-Start Circuit Schematic

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators

APPLICATIONS INFORMATION (cont.)

TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

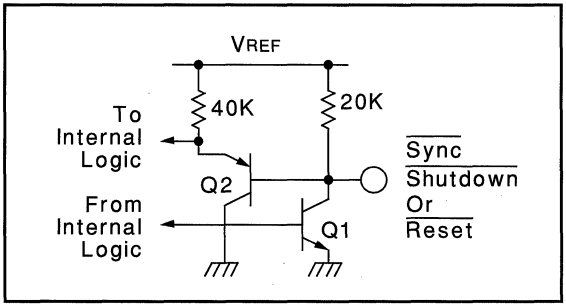


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD = 0 (pin 11 shorted to ground) select values for RT and CT from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +VC terminal is the same as the oscillator frequency.

2. If more dead time is required, select a large value of RD. At 40kHz dead time increases by 400ns/Ω .

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminals may be either left open or grounded.

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +VC, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +VC terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

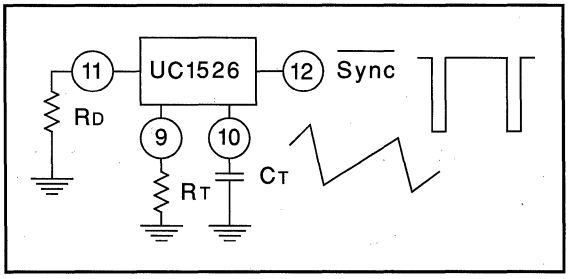


Figure 5. Oscillator Connections and Waveforms

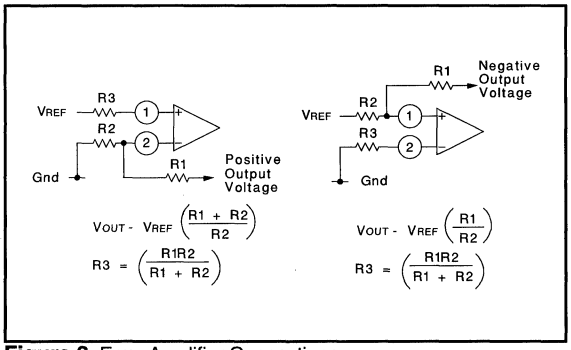


Figure 6. Error Amplifier Connections

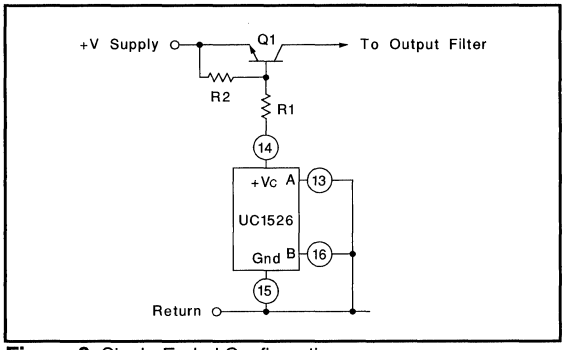


Figure 8. Single-Ended Configuration

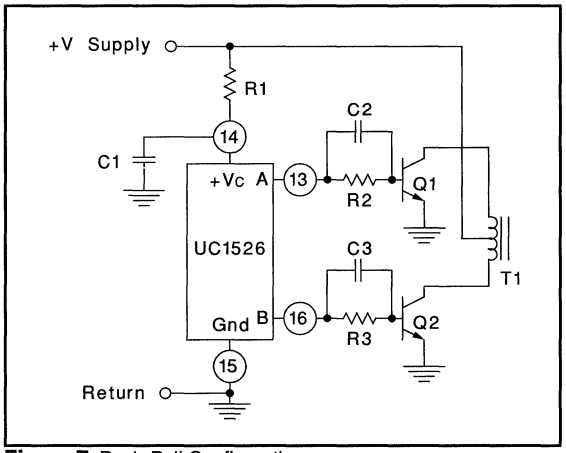


Figure 7. Push-Pull Configuration

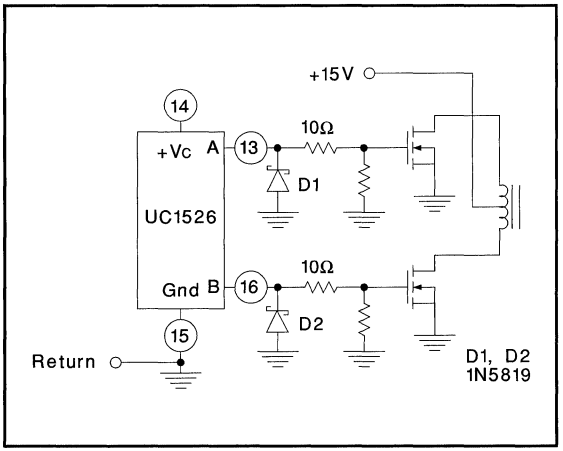
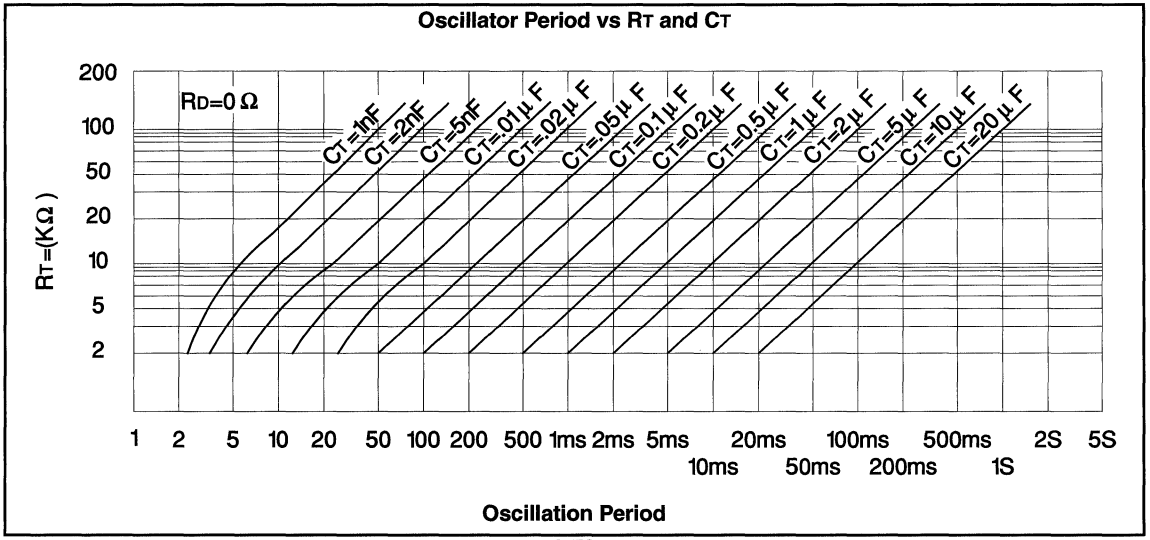


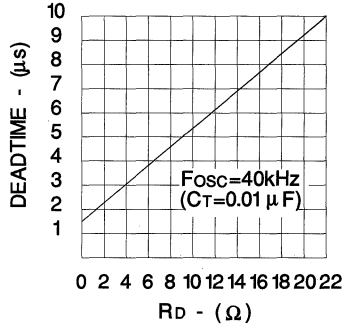
Figure 9. Driving N-channel Power Mosfets

TYPICAL CHARACTERISTICS

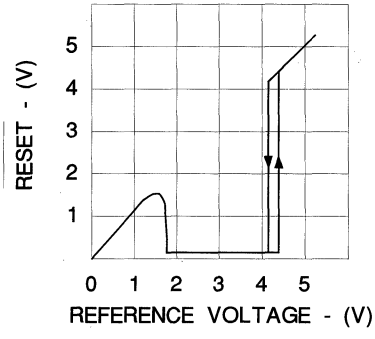


TYPICAL CHARACTERISTICS

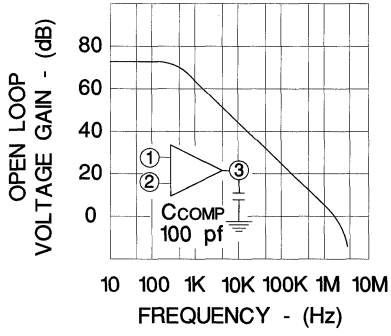
Output Driver Deadtime vs RD Value



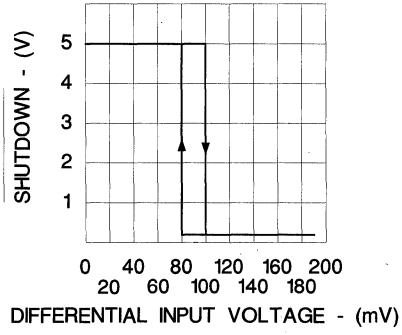
Under Voltage Lockout Characteristic



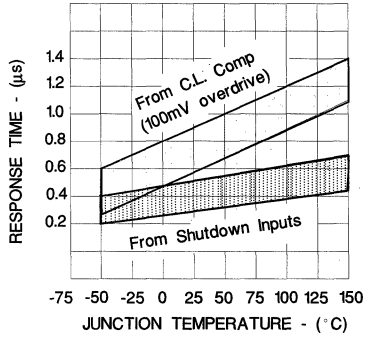
Error Amplifier Open Loop Gain vs Frequency



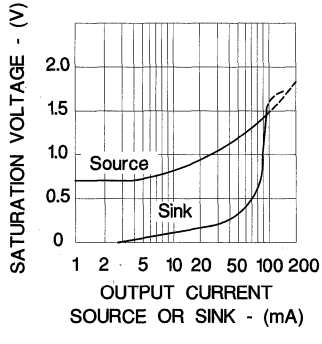
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



UNITRODE CORPORATION
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UNITRODE

UC1526A
UC2526A
UC3526A

Regulating Pulse Width Modulator

FEATURES

- Reduced Supply Current
- Oscillator Frequency to 600kHz
- Precision Band-Gap Reference
- 7 to 35V Operation
- Dual 200mA Source/Sink Outputs
- Minimum Output Cross-Conduction
- Double-Pulse Suppression Logic
- Under-Voltage Lockout
- Programmable Soft-Start
- Thermal Shutdown
- TTL/CMOS Compatible Logic Ports
- 5 Volt Operation (V_{IN} = V_C = V_{REF} = 5.0V)

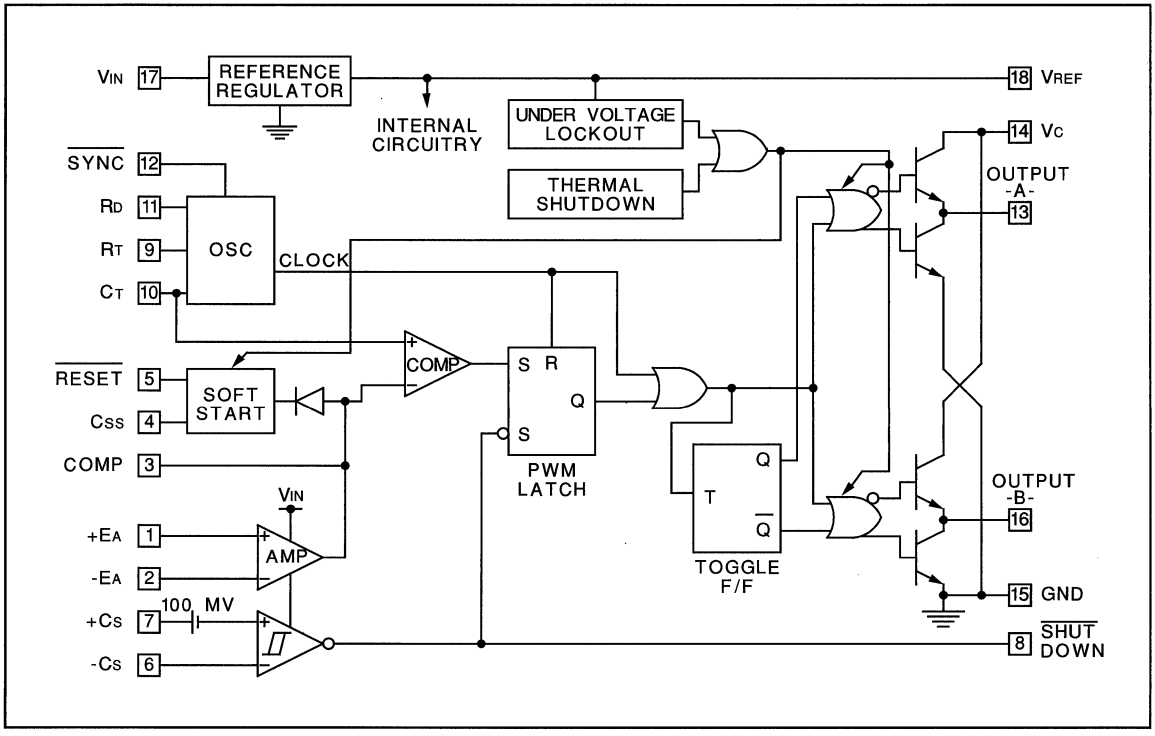
DESCRIPTION

The UC1526A Series are improved-performance pulse-width modulator circuits intended for direct replacement of equivalent non- "A" versions in all applications. Higher frequency operation has been enhanced by several significant improvements including: a more accurate oscillator with less minimum dead time, reduced circuit delays (particularly in current limiting), and an improved output stage with negligible cross-conduction current. Additional improvements include the incorporation of a precision, band-gap reference generator, reduced overall supply current, and the addition of thermal shutdown protection.

Along with these improvements, the UC1526A Series retains the protective features of under-voltage lockout, soft-start, digital current limiting, double pulse suppression logic, and adjustable deadtime. For ease of interfacing, all digital control ports are TTL compatible with active low logic.

Five volt (5V) operation is possible for "logic level" applications by connecting V_{IN}, V_C and V_{REF} to a precision 5V input supply. Consult factory for additional information.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+VIN) . . . . . +40V
Collector Supply Voltage (+VC) . . . . . +40V
Logic Inputs . . . . . -0.3V to +5.5V
Analog Inputs . . . . . -0.3V to +VIN
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at TA = +25°C (Note 2) 1000mW
Power Dissipation at TC = +25°C (Note 2) 3000mW
Operating Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging Section of Databook for thermal limitations and considerations of package.

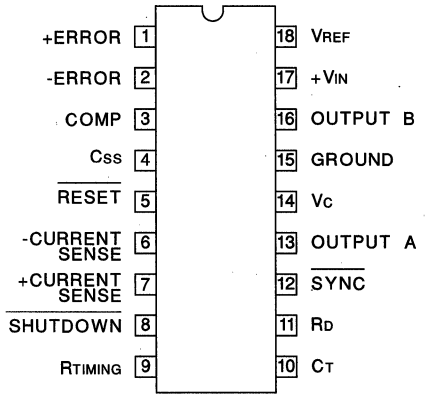
RECOMMENDED OPERATING CONDITIONS

(Note 3)
Input Voltage . . . . . +7V to +35V
Collector Supply Voltage . . . . . +4.5V to +35V
Sink/Source Load Current (each output) . . . . . 0 to 100mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 1Hz to 600kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 400pF to 20μF
Available Deadtime Range at 40kHz . . . . . 1% to 50%
Operating Ambient Temperature Range
UC1526A . . . . . -55°C to +125°C
UC2526A . . . . . -25°C to +85°C
UC3526A . . . . . 0°C to +70°C

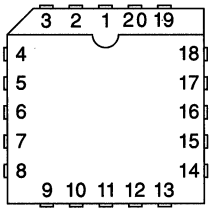
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+ERROR	2
-ERROR	3
COMP.	4
CSS	5
RESET	6
- CURRENT SENSE	7
+ CURRENT SENSE	8
SHUTDOWN	9
RTIMING	10
CT	11
RD	12
SYNC	13
OUTPUT A	14
VC	15
N/C	16
GROUND	17
OUTPUT B	18
+VIN	19
VREF	20

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1526A / UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	T_J = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 7 to 35V		2	10		2	15	mV
Load Regulation	I_L = 0 to 20mA		5	20		5	20	mV
Temperature Stability	Over Operating T_J (Note 5)		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under-Voltage Lockout								
$\overline{RESET}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
	V_{REF} = 4.7V	2.4	4.7		2.4	4.8		V
Oscillator Section (Note 6)								
Initial Accuracy	T_J = +25°C		±3	±8		±3	±8	%
Voltage Stability	+V_{IN} = 7 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J (Note 5)		2	6		1	3	%
Minimum Frequency	R_T = 150kΩ, C_T = 20µF (Note 5)			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 470pF	550			650			kHz
Sawtooth Peak Voltage	+V_{IN} = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	+V_{IN} =7V	0.5	1.0		0.5	1.0		V
$\overline{SYNC}$ Pulse Width	T_J = 25°C, R_L = 2.7kΩ to V_{REF}		1.1			1.1		µs
Error Amplifier Section (Note 7)								
Input Offset Voltage	R_S ≤ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	R_L ≥ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	$V_{PIN\ 1}$ - $V_{PIN\ 2}$ ≥ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	$V_{PIN\ 2}$ - $V_{PIN\ 1}$ ≥ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	R_S ≤ 2kΩ	70	94		70	94		dB
Supply Voltage Rejection	+V_{IN} = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 6)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{SYNC}$, $\overline{SHUTDOWN}$, and $\overline{RESET}$)								
HIGH Output Voltage	I_{SOURCE} = 40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	µA
Shutdown Delay	From Pin 8, T_J = 25°C		160			160		ns
Current Limit Comparator (Note 8)								
Sense Voltage	R_S ≤ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Shutdown Delay	From pin 7, 100mV Overdrive, T_J = 25°C		260			260		ns

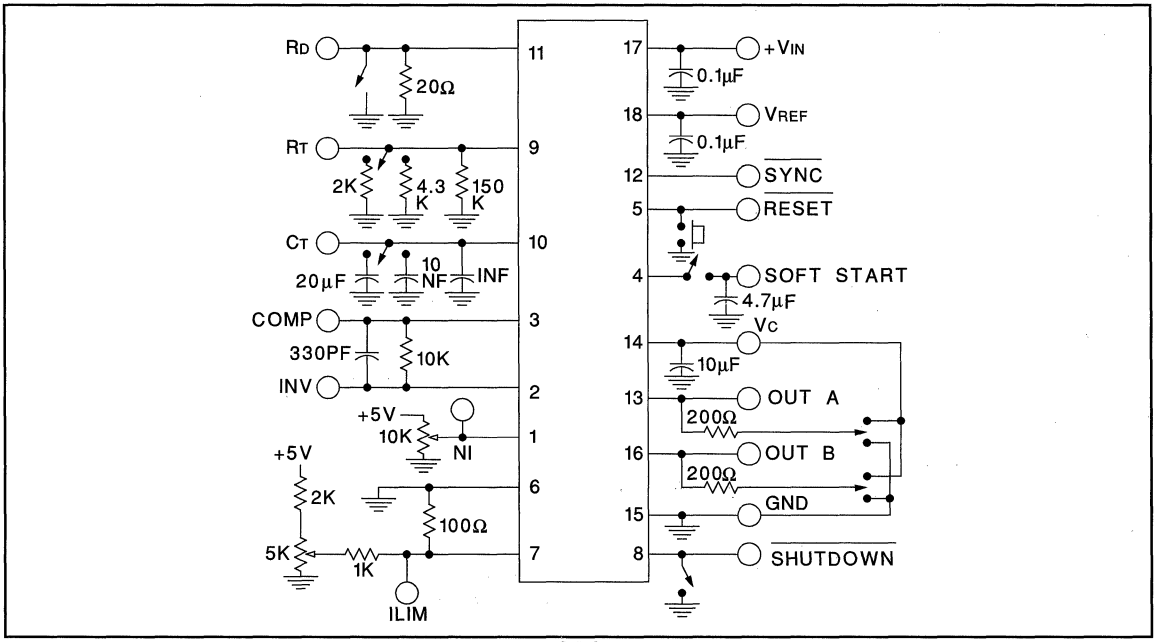
Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: F_{OSC} = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01µF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10: V_{IN} = +35V, R_T = 4.12kΩ.

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1526A UC2526A			UC3526A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Soft-Start Section								
Error Clamp Voltage	$\overline{RESET}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{RESET}$ = +2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 9)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF (Note 5)		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF (Note 5)		0.1	0.2		0.1	0.2	µs
Cross-Conduction Charge	Per cycle, T_J = 25°C		8			8		nC
Power Consumption (Note 10)								
Standby Current	$\overline{SHUTDOWN}$ = +0.4V		14	20		14	20	mA

Note 4: I_L = 0mA.
Note 5: Guaranteed by design, not 100% tested in production.
Note 6: F_{OSC} = 40kHz, (R_T = 4.12kΩ ± 1%, C_T = 0.01µF± 1%, R_D = 0 Ω).
Note 7: V_{CM} = 0 to +5.2V
Note 8: V_{CM} = 0 to +12V.
Note 9: V_C = +15V.
Note 10:

Open Loop Test Circuit UC1526A



APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526A is based on a precision band-gap reference, internally trimmed to ±1% accuracy. The circuitry is fully active at supply voltages above +7V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

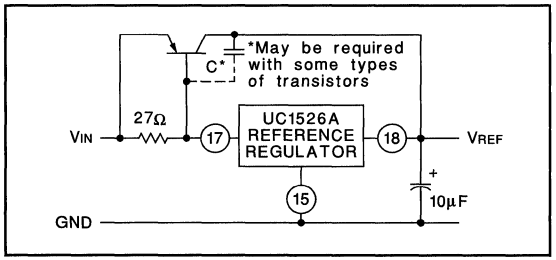


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526A and the power devices it controls from inadequate supply voltage, If +VIN is too low, the circuit disables the output drivers and holds the RESET pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to 3VBE or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the RESET pin, allowing a normal soft-start. The comparator has 350mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls RESET LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526A can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

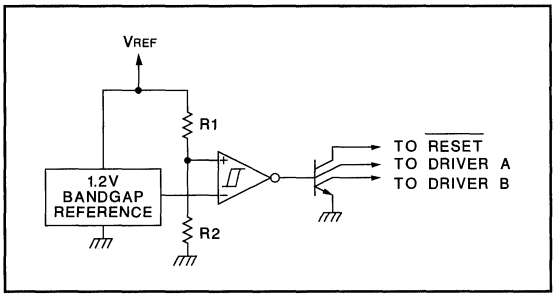


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526A, the under-voltage lockout circuit holds RESET LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, RESET will go HIGH. Q1 turns off, allowing the internal 100µA current source to charge CS. Q2 clamps the error amplifier output to 1VBE above the voltage on CS. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for

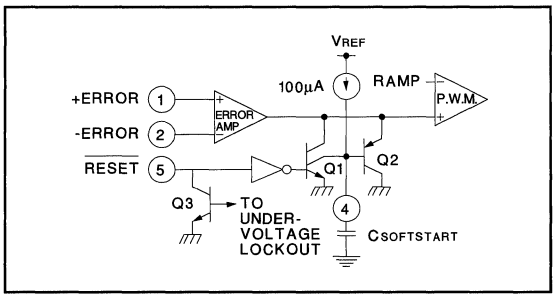


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526A are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving SYNC LOW initiates a discharge cycle in the oscillator. Pulling SHUTDOWN LOW immediately inhibits all PWM output pulses. Holding RESET LOW

APPLICATIONS INFORMATION (cont.)

capacitor. The logic threshold is +1.1V at +25⊃C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

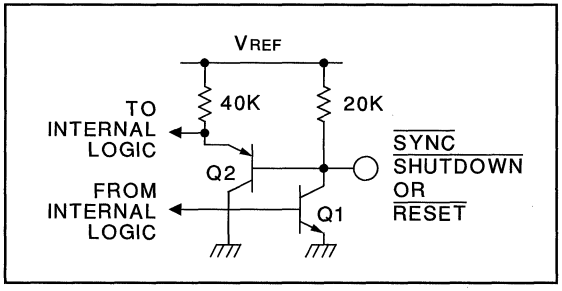


Figure 4. Digital Control Port Schematic

Oscillators

The oscillator is programmed for frequency and dead time with three components: RT, CT and RD. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With RD= 0Ω (pin 11 shorted to ground) select values for RT and CT from the graph on page 4 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +VC terminal is the same as the oscillator frequency.

2. If more dead time is required, select a larger value of RD. At 40kHz dead time increases by 400ns/Ω.

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of RT slightly to bring the frequency back to the nominal design value.

The UC1526A can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the SYNC frequency.

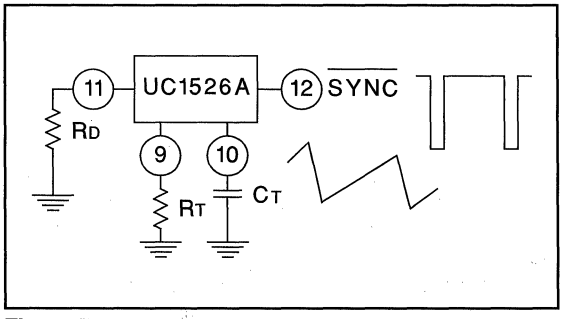


Figure 5. Oscillator Connections and Waveforms

the SYNC pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency, and then sharing its sawtooth and clock waveforms with the slave units. All CT terminals are connected to the CT pin of the master and all SYNC terminals are likewise connected to the SYNC pin of the master. Slave RT terminals are left open or connected to VREF. Slave RD terminal may be either left open or grounded.

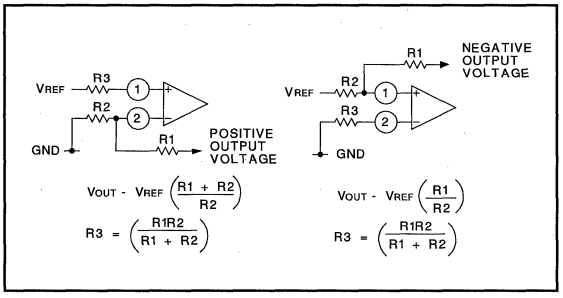


Figure 6. Error Amplifier Connections

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ. Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

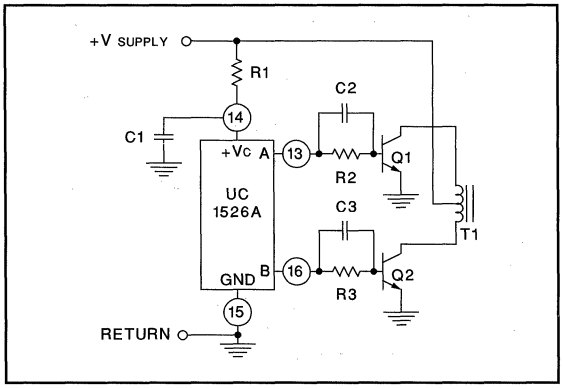


Figure 7. Push-Pull Configuration

APPLICATIONS INFORMATION (cont.)

Output Drivers

The totem pole output drivers of the UC1526A are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching; however, improved design has limited this cross-conduction period to less than 50ns. Capacitor decoupling at Vc is recommended and careful grounding of Pin 15 is needed to insure that high peak sink currents from a capacitive load do not cause ground transients.

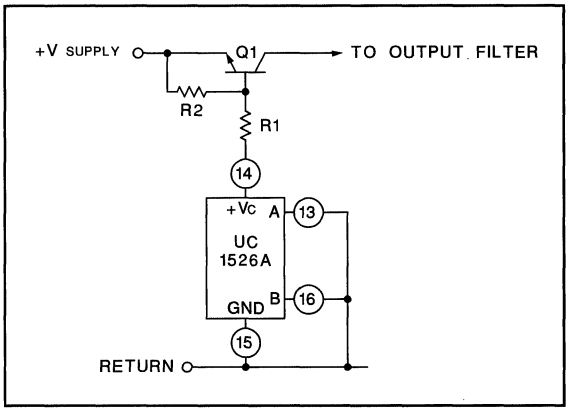


Figure 8. Single-Ended Configuration

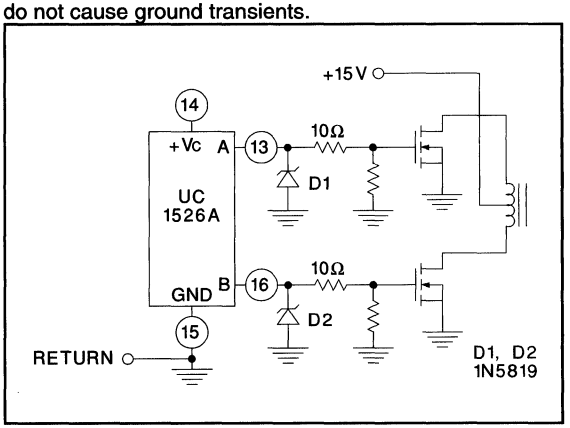
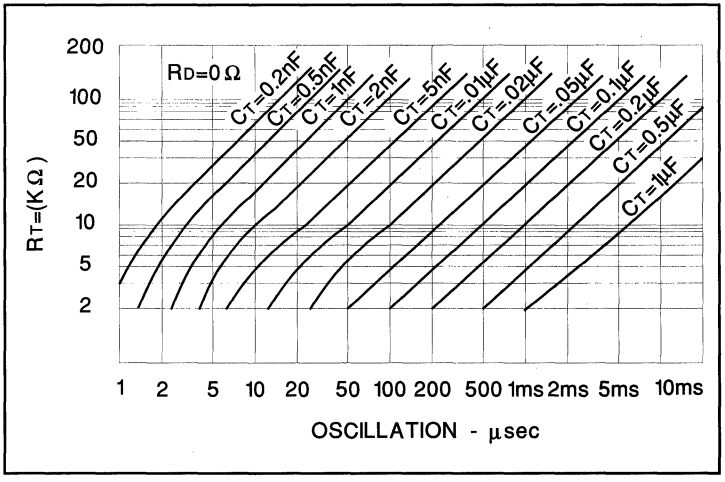


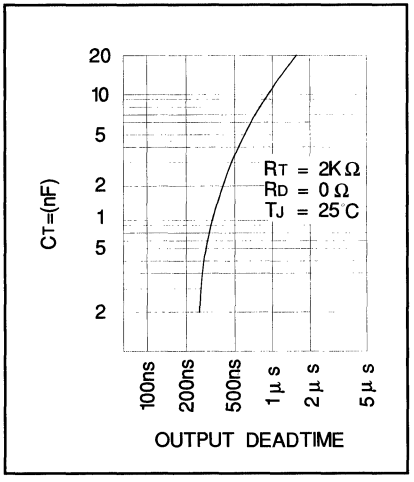
Figure 9. Driving N-Channel Power MOSFETs

TYPICAL CHARACTERISTICS

OSCILLATOR PERIOD vs RT and CT

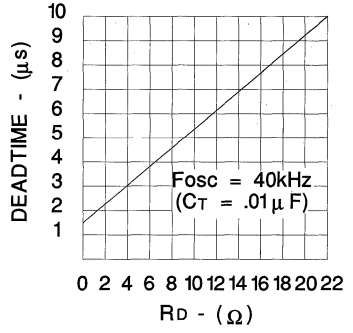


OUTPUT BLANKING

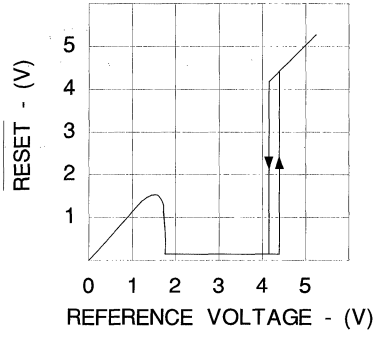


TYPICAL CHARACTERISTICS (Cont.)

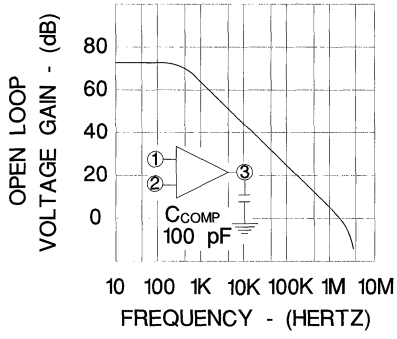
Output Driver Deadtime vs. RD Value



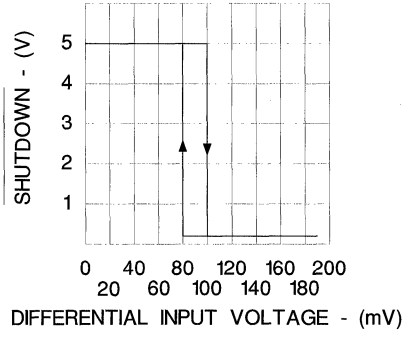
Under Voltage Lockout Characteristic



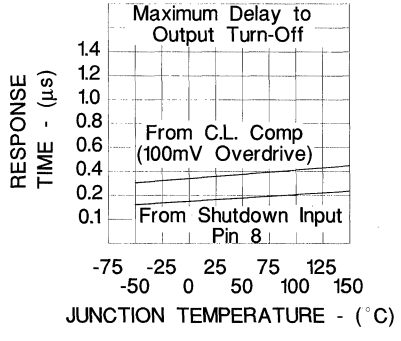
Error Amplifier Open Loop Gain vs. Frequency



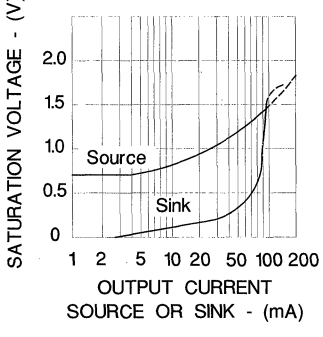
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



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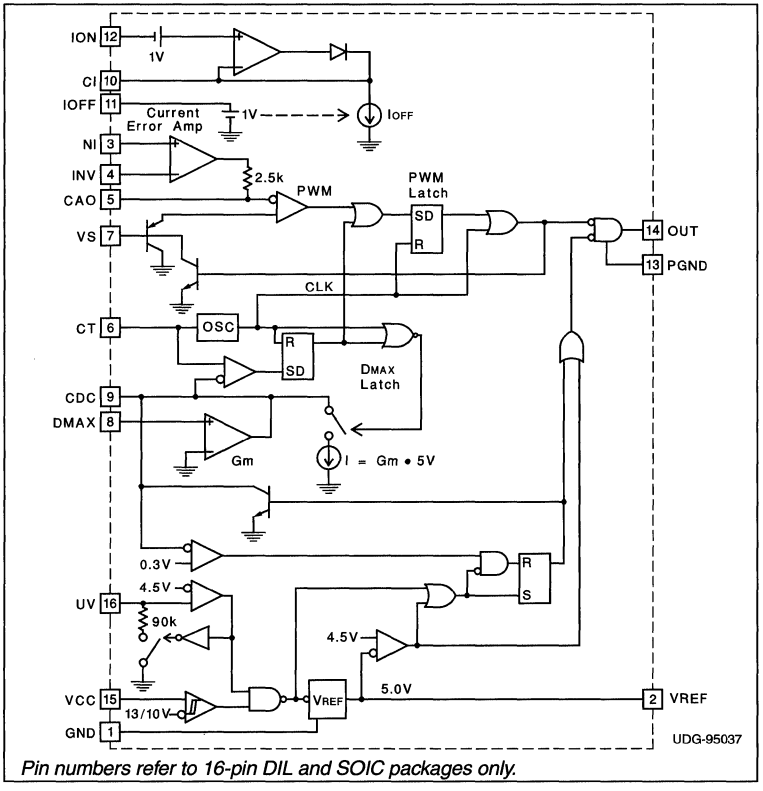
Primary Side PWM Controller

FEATURES

- Primary Side Voltage Feed-forward Control of Isolated Power Supplies
- Accurate DC Control of Secondary Side Short Circuit Current using Primary Side Average Current Mode Control
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Undervoltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Startup Current (500µA)

BLOCK DIAGRAM



Pin numbers refer to 16-pin DIL and SOIC packages only.

DESCRIPTION

The UC3548 family of PWM control ICs uses voltage feed-forward control to regulate the output voltage of isolated power supplies. The UC3548 resides on the primary side and has the necessary features to accurately control secondary side short circuit current with average current mode control techniques. The UC3548 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC3548 implements a patented technique of sensing secondary current from the primary side in an isolated buck derived converter. A current waveform synthesizer monitors switch current and simulates the inductor current downslope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side is used by an average current mode control circuit to accurately limit maximum output current.

The UC3548 circuitry includes a precision reference, a wide bandwidth error amplifier for average current control, an oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current output driver. The current error amplifier easily interfaces with an optoisolator from a secondary side voltage sensing circuit.

A full featured undervoltage lockout (UVLO) circuit is contained in the UC3548. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500µA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

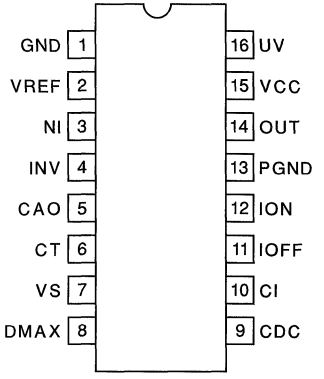
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15) 22V
Output Current, Source or Sink (Pin 14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground to Ground (Pin 1 to Pin 13) ..... ±0.2V
Analog Input Voltages
(Pins 3, 4, 7, 8, 12, 16) ..... -0.3 to 7V
Analog Input Currents, Source or Sink
(Pins 3, 4, 7, 8, 11, 12, 16) 1mA
Analog Output Currents, Source or Sink (Pins 5 & 10) ... 5mA
Power Dissipation at T_A = 60°C 1W
Storage Temperature Range..... –65°C to +150°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

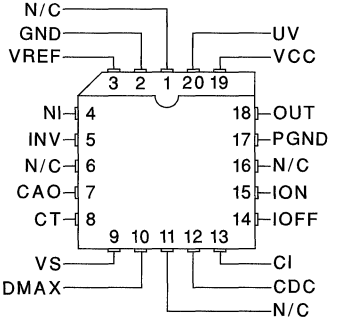
Notes: All voltages are with respect to ground (DIL and SOIC pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or DW Packages



PLCC-20 & LCC-20 (Top View)
Q & L Packages



ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the junction temperature range of –55°C to +125°C for the UC1548, –40°C to +85°C for the UC2548, and 0°C to +70°C for the UC3548. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/µs
Iib			-2	-20	µA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	100		dB
Vio	12V ≤ VCC ≤ 20V, 0V ≤ VCM ≤ 5V			10	mV
Iib			-0.5	-3	µA
Voh	Io = –200µA	3.1	3.3	3.5	V
Vol	Io = 200µA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/µs
Oscillator					
Frequency	T_A = 25°C	240	250	260	kHz
		235		265	kHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, all specifications are over the junction temperature range of –55°C to +125°C for the UC1548, –40°C to +85°C for the UC2548, and 0°C to +70°C for the UC3548. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Duty Cycle Clamp					
Max Duty Cycle	$V_{(DMAX)} = 0.75 \bullet V_{REF}$	73.5	76.5	79.5	%
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
$R_{HYSTERESIS}$	Vuv = 4.2V	77	90	103	kΩ
Reference					
VREF	$T_A = 25°C$	4.95	5	5.05	V
	0 < Io < 10mA, 12 < VCC < 20	4.93		5.07	V
Line Regulation	12V < Vcc < 20V		4	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit Current	$V_{REF} = 0V$	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	CI = 1nF		20	45	ns
Output Low Saturation	Io = 20mA		0.25	0.4	V
	Io = 200mA		1.2	2.2	V
Output High Saturation	Io = -200mA		2.0	3.0	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Icc					
I_{START}	VCC = 12V		0.2	0.4	mA
Icc (pre-start)	VCC = 15V, V(UV) = 0		0.5	1	mA
Icc (run)			22	26	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAO: Output of the current error amplifier. Also the resistor load for the collector of an optocoupler.

CDC: Connect a charge balance integration capacitor from CDC to GND to achieve an accurate duty cycle clamp. This capacitor also sets the soft start time.

CI: Output of the inductor current waveform synthesizer. Requires a capacitor to ground.

CT: A capacitor from CT to GND sets the oscillator frequency.

DMAX: Programs maximum duty cycle with a resistive divider from VREF to DMAX to GND.

GND: Signal ground.

INV: Inverting input of the current error amplifier.

IOFF: Programs the discharge slope of the capacitor on CI to emulate the down slope of the inductor current waveform.

ION: Input pin to inductor current waveform synthesizer. Apply a voltage proportional to switch current to this pin.

NI: Noninverting input of the current error amplifier.

OUT: Output driver for the gate of a power FET.

PGND: Power ground pin for the output driver. This ground circuit should be connected to GND at a single point.

UV: Line voltage sense pin to insure the chip only operates with sufficient line voltage. Program with a resistive divider from the converter input voltage to UV to GND.

VCC: Chip supply voltage. Bypass with a 1µF ceramic capacitor to PGND.

VREF: Precision voltage reference. Bypass with a 1µF ceramic capacitor to GND.

VS: Volt second clamp programming pin and feedforward ramp waveform for the pulse width modulator. Connect a resistor to the input line voltage and a capacitor to GND.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout block diagram is shown in Figure 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (<500µA) and the output is low.

The UV comparator monitors input line voltage (V_{IN}). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$V_{IN(on)} = 4.35V \bullet (1 + Rv1/Rv2')$ and

$V_{IN(off)} = 4.35V \bullet (1 + Rv1/Rv2)$ where

$Rv2' = Rv2 \| 90k$.

The resulting hysteresis is

$V_{IN(hys)} = 4.35V \bullet Rv1 / 90k$.

When the UV comparator is low, I_{CC} is low (<500µA) and the output is low.

When both the UV and VCC comparators are high, the internal bias circuitry for the remainder of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

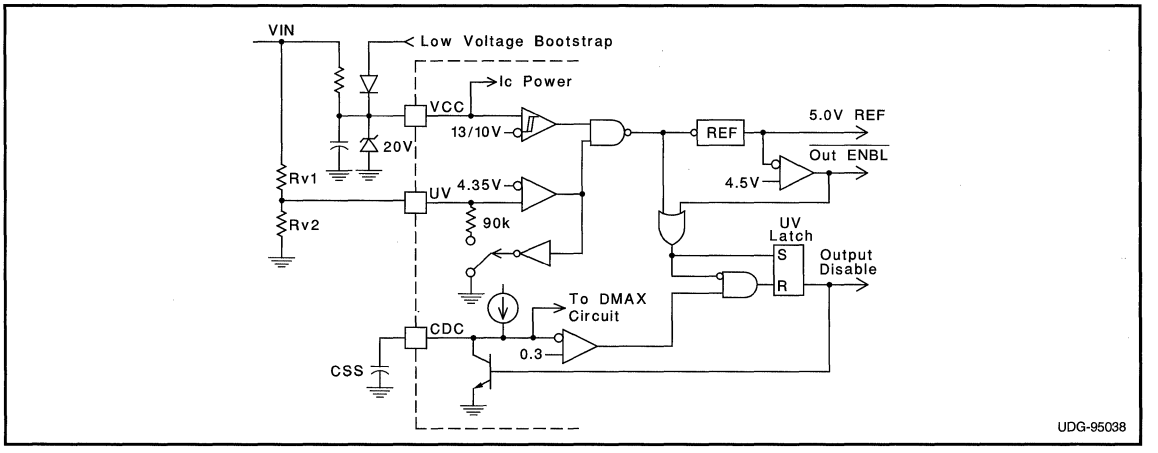


Figure 1: Undervoltage Lockout

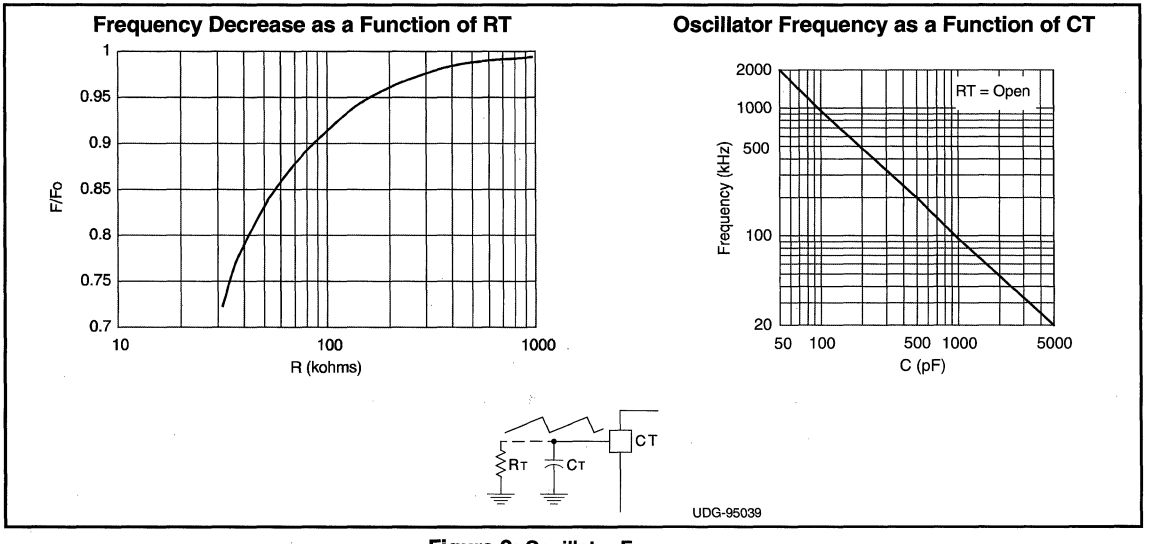


Figure 2: Oscillator Frequency

OSCILLATOR

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Figure 2. Frequency is determined by:

$$F = 1 / (10k \bullet CT).$$

The sawtooth wave shape is generated by a charging current of 200µA and a discharge current of 1800µA. The discharge time of the sawtooth is guaranteed dead time for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor RT from CT to ground can be used to adjust the oscillator frequency. RT should not be less than 40kohms. This will allow up to a 22% decrease in frequency.

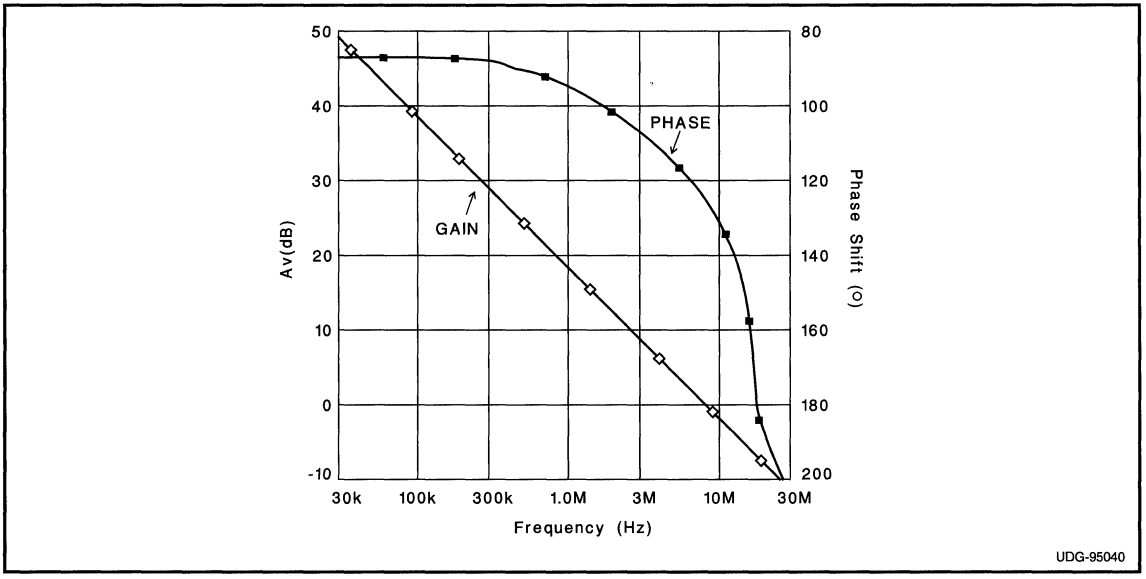


Figure 3: Error Amplifier Gain and Phase Response over Frequency

INDUCTOR CURRENT WAVEFORM SYNTHESIZER

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope dIL/dt = –Vo/L. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Figure 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. The best utilization of the UC3548 is to translate maximum average inductor current to a 4 volt signal level. Given N and Ns (the turns ratio of the power and current sense transformers respectively), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$Rs = 4V \bullet Ns \bullet N / IL(max).$$

Restated, the maximum average inductor current will be limited to:

$$IL(max) = 4V \bullet Ns \bullet N/Rs.$$

IOFF and CI need to be chosen so that the ratio of dV(CI)/dt to dIL/dt is the same during switch off time as on time. Recommended nominal off current is 100µA. This requires

$$CI = (100\mu A \bullet N \bullet Ns \bullet L) / (Rs \bullet Vo(nom))$$

where L is the output inductor value and Vo(nom) is the converter regulated output voltage.

INDUCTOR CURRENT WAVEFORM SYNTHESIZER (cont.)

There are several methods to program IOFF. If accurate maximum current control is required, IOFF must track output voltage. The method shown in Figure 4 derives a voltage proportional to VIN • D (where D = duty cycle). In a buck converter, output voltage is proportional to VIN • D. A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to VIN and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated Vo. A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI downslope.

If accurate system maximum current is not a critical requirement, Figure 5 shows the simplest method of downslope generation: a single resistor (ROFF = 40k) from IOFF to VREF. The discharge current is then 100µA. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor downslope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Figure 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, ROFF = Vo / 100µA. The 4 • ROFF resistor is added to compensate the one volt input level of the IOFF pin. Without this compensation, a minor current foldback behavior will be observed.

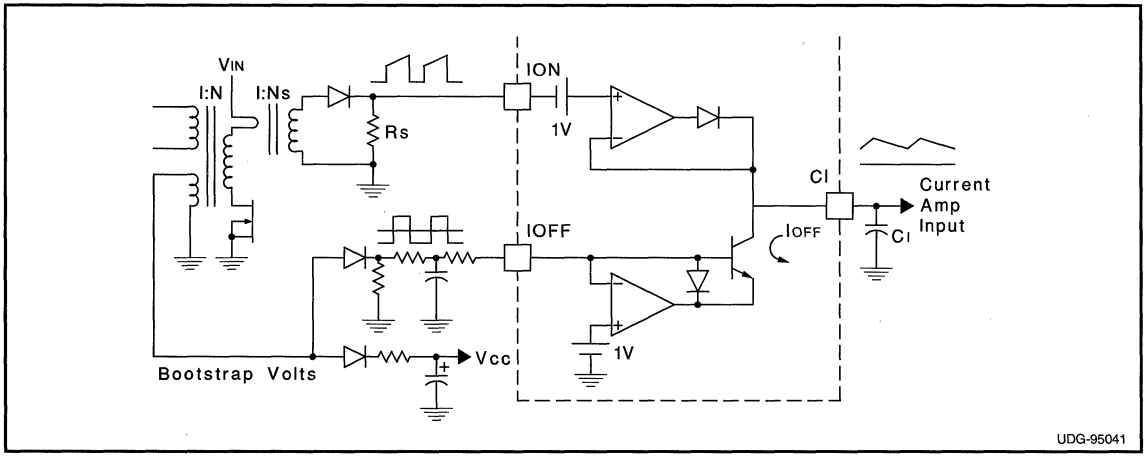


Figure 4: Inductor Current Waveform Synthesizer

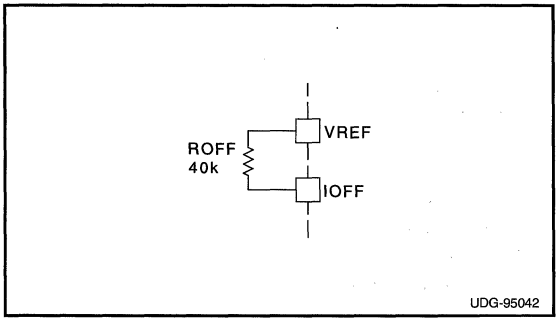


Figure 5: Fixed IOFF

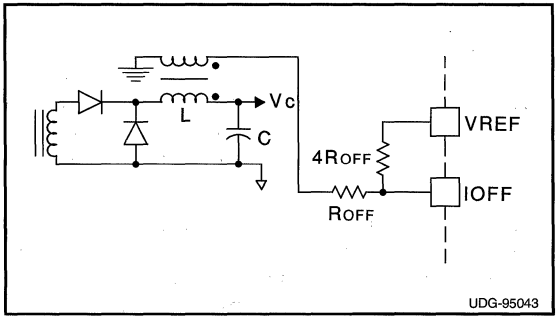


Figure 6: Second Inductor Winding Generation of IOFF

FEED FORWARD PULSE WIDTH MODULATION

Pulse width modulation is achieved by comparing the output of the current error amplifier to the feed forward ramp generated at VS (Figure 7). The charge slope of the ramp is determined by a resistor (RVS) from VS to VIN and a capacitor (CVS) from VS to GND. In the event that CAO is at its maximum voltage, typically 3.3V, the UC3548 will limit the power stage to a volt-second product of:

$$V_{IN} \bullet T_{ON}(max) = 3.3V \bullet Rvs \bullet Cvs.$$

An isolated voltage control loop can be implemented with a secondary side reference, error amplifier and an optoisolator. The optoisolator can be used to override the current amplifier output which is current limited by a 2.5k resistor. In overcurrent situations, the voltage loop turns the optoisolator off and the current error amplifier then assumes duty cycle control resulting in accurately limited maximum output current.

MAXIMUM DUTY CYCLE AND SOFT START

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Figure 7). The value programmed is:

$$D(max) = Rd1 / (Rd1 + Rd2).$$

For proper operation, the integrating capacitor, C_{DC}, should be larger than T(osc) / 80k, where T(osc) is the oscillator period. C_{DC} also sets the soft start time constant, so values of C_{DC} larger than minimum may be desired. The soft start time constant is approximately:

$$T(ss) = 20k \bullet C_{DC}.$$

GROUND PLANES

The output driver on the UC3548 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Figure 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which to PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The source of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, CI and VS should likewise be connected to the signal ground plane.

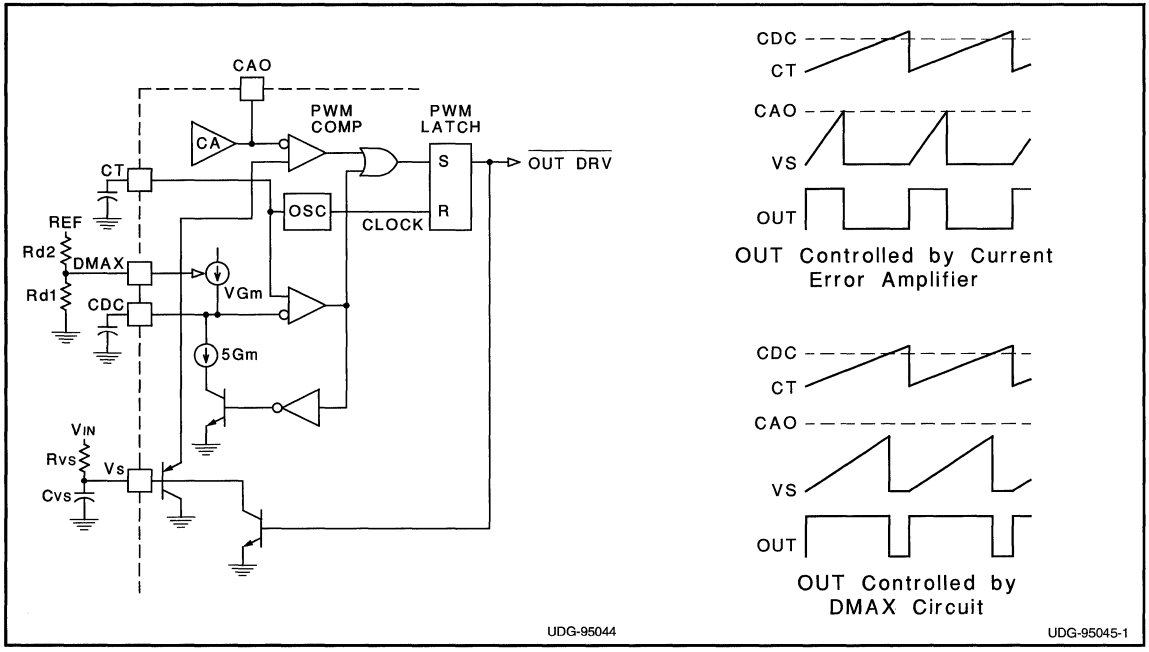


Figure 7: Duty Cycle Control

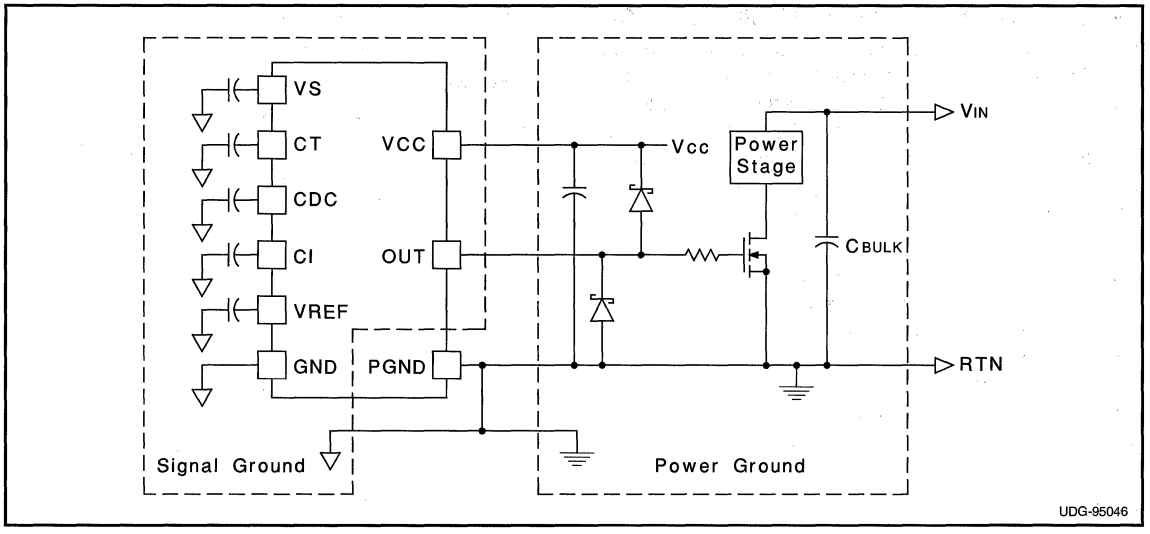


Figure 8: Ground Plane Considerations

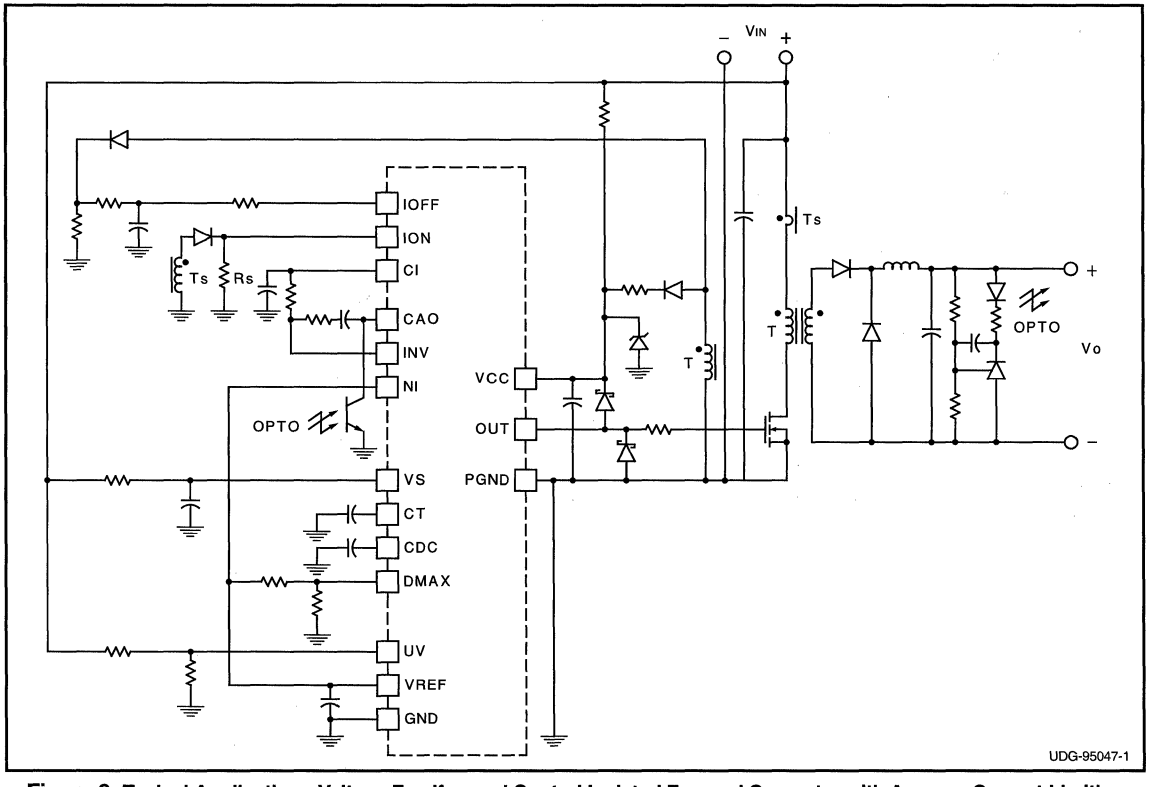


Figure 9: Typical Application - Voltage Feedforward Control Isolated Forward Converter with Average Current Limiting

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application INFO available

UCC1570
UCC2570
UCC3570

Low Power Pulse Width Modulator

FEATURES

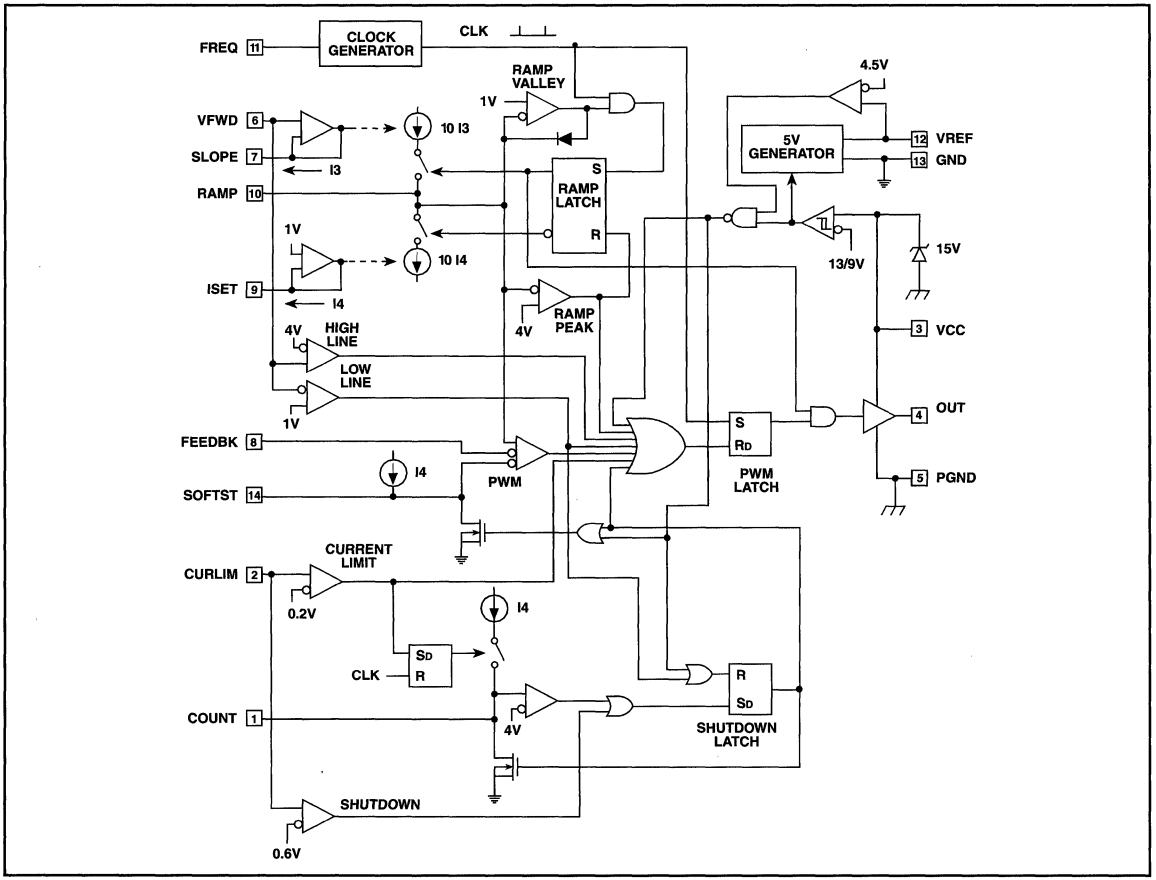
- Low Power BiCMOS Process
- 85µA Start-up Current
- 1mA Run Current
- 1A Peak Gate Drive Output
- Voltage Feed Forward
- Programmable Duty Cycle Clamp
- Optocoupler Interface
- 500kHz Operation
- Soft Start
- Fault Counting Shutdown
- Fault Latch Off or Automatic Restart

DESCRIPTION

The UCC1570 family of pulse width modulators is intended for application in isolated switching supplies using primary side control and a voltage mode feedback loop. Made with a BiCMOS process, these devices feature low startup current for efficient off-line starting with a bootstrapped low voltage supply. Operating current is also very low; yet these devices maintain the ability to drive a power MOSFET gate at frequencies above 500kHz.

Voltage feedforward provides fast and accurate response to wide line voltage variation without the noise sensitivity of current mode control. Fast current limiting is included with the ability to latch off after a programmable number of repetitive faults has occurred. This allows the power supply to ride through a temporary overload, while still shutting down in the event of a permanent fault. Additional versatility is provided with a maximum duty cycle clamp programmable within a 20% to 80% range and line voltage sensing with a programmable window of allowable operation.

BLOCK DIAGRAM

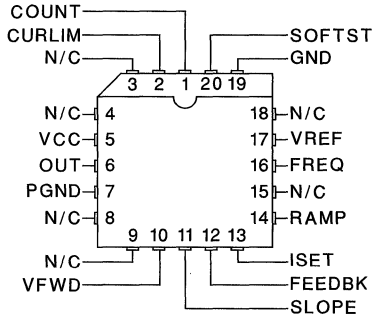


ABSOLUTE MAXIMUM RATINGS

Supply Voltage
(Limit Supply Current to 20mA) . . . . . Self Limiting at 15V
Supply Current . . . . . +20mA
Analog Inputs (CURLIM, VFWD, FEEBK) 6V
Programming Current I_{SLOPE}, I_{ISET} . . . . . –1mA
Output Current I_{OUT}
DC . . . . . ±180mA
Pulse (0.5ms) . . . . . ±1.2A

Note: *All voltages are with respect to GND. Currents are positive into the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.*

PLCC-20 (TOP VIEW)
Q Package

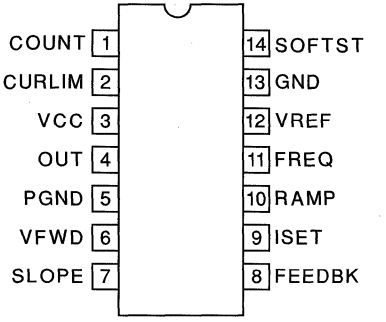


ORDERING INFORMATION

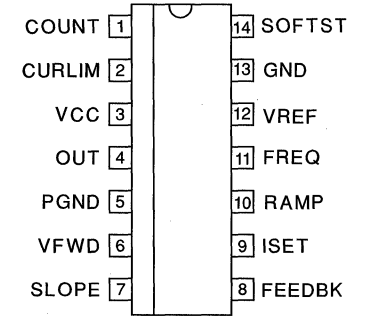
	Temperature Range	Package
UCC1570J	–55°C to +125°C	Ceramic Dip
UCC2570D	–40°C to +85°C	SOIC
UCC2750N		Plastic Dip
UCC3570D	0°C to +70°C	SOIC
UCC3570N		Plastic Dip
UCC3570Q		PLCC

CONNECTION DIAGRAMS

DIL-14 (TOP VIEW)
N or J Package



SOIC-14 (TOP VIEW)
D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= –40 to 85°C for the UCC2570, T_A=–55 to 125°C for the UCC1570, R_{ISET}=100k, R_{SLOPE}=121k, C_{FREQ}=180pF, C_{RAMP}=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Reference					
VREF	VCC =10 to 13V, I_{VREF} = 0 to 2mA	4.9	5	5.1	V
Line Regulation	VCC = 10 to 13V		2	10	mV
Load Regulation	I_{VREF} = 0 to 2mA		2	10	mV
Short Circuit Current	VREF = 0		10	50	mA
VCC					
Vth (On)		12	13		V
Vth (Off)		8	9	10	V
Hysteresis		3	4	5	V
VCC	I_{VCC} = 10mA	13.5	15	16	V
I_{VCC} Start	VCC = 11V, VCC Comparator Off		85	150	µA
$I_{VCC\ Run}$	VCC Comparator On		1	1.5	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0 to 70°C for the UCC3570, T_A= –40 to 85°C for the UCC2570, T_A=–55 to 125°C for the UCC1570, R_{ISET}=100k, R_{SLOPE}=121k, C_{FREQ}=180pF, C_{RAMP}=150pF, VCC=11V and T_A=T_J.

PARAMETER	TEST CONDITIONS	Min	Typ	Max	Units
Line Sense					
Vth High Line Comparator		3.9	4	4.1	V
Vth Low Line Comparator		0.96	1	1.04	V
Iib (VFWD)			0	±100	nA
Oscillator					
Frequency		90	100	110	kHz
Ramp Generator					
I_{RAMP}/I_{SLOPE}		9	10	11	A/A
$-I_{RAMP}/I_{ISET}$		9	10	11	A/A
Peak Ramp Voltage		3.8	4	4.2	V
Valley Ramp Voltage		0.95	1	1.05	V
ISET Voltage Level		0.95	1	1.05	V
Soft Start					
Saturation	VCC = 11V, VCC Comparator Off		25	100	mV
I_{SOFTST}/I_{ISET}		0.8	1	1.2	A/A
Pulse Width Modulator					
Iib(FEEDBK)			0	±100	n A
FEEDBK	Zero Duty Cycle	0.9	1	1.1	V
	Maximum Duty Cycle, (Note 1)	3.8	4	4.2	V
Current Limit					
Iib(CURLIM)			0	±100	nA
Vth Current Limit		180	200	220	mV
Vth Shutdown		500	600	700	mV
Fault Counter					
Vth		3.8	4	4.2	V
Vsat			0	100	mV
I_{COUNT}/I_{ISET}		0.8	1	1.2	A/A
Output Driver					
Vsat High	I_{OUT} = –100mA		0.4	1	V
Vsat Low	I_{OUT} = 100mA		0.4	1	V
Rise/Fall Time	C_{OUT} = 1nF, (Note 1)		20	100	ns

Note 1: *This parameter guaranteed by design but not 100% tested in production.*

PIN DESCRIPTIONS

VCC: Chip supply voltage pin. Bypass to PGND with a low ESL/ESR 0.1µF capacitor plus a capacitor for gate charge storage. Lead lengths must be minimum.

PGND: Ground pin for the output driver. Keep connections less than 2cm. Carefully maintain low impedance path for high current return.

OUT: Gate drive output pin. Connect to the gate of a power MOSFET with a resistor greater than 2Ω. Keep connection lengths under 2cm.

VFWD: Voltage Feed Forward and Line Sense pin. Connect to input DC line using a resistive divider.

SLOPE: Program the charging current for RAMP with a resistor from this pin to GND. This pin will follow VFWD.

FEEDBK: Input to the pulse width modulator comparator. Drive this pin with an optocoupler to GND and a resistor to VREF. Modulation input range is from 1V to 4V.

ISET: A resistor from this pin to GND programs RAMP discharge current, FREQ current, SOFTST current, and COUNT current.

PIN DESCRIPTIONS (cont.)

RAMP: Ramp Pin. Connect a capacitor to GND. Rising slope is programmed by current in SLOPE. This slope is compared to FEEDBK for pulse width modulation. The falling slope is programmed by the current in ISET and used to limit maximum duty cycle.

FREQ: Oscillator pin. Program the frequency with a capacitor to GND.

VREF: Precision 5V reference, and bypass point for internal circuitry. Bypass this pin with a 1µF minimum capacitor to GND.

GND: Analog ground. Connect to a low impedance ground plane containing all analog low current returns.

SOFTST: Soft start pin. Program with a capacitor to GND.

COUNT: Program the time that fault events will be tolerated before shutdown occurs with a capacitor and resistor to GND.

CURLIM: Current Limit Sense pin. Terminates OUT gate drive pulse for inputs over 0.2V. Enables fault counting function (COUNT). For inputs over 0.6V, the shutdown latch is activated.

APPLICATION INFORMATION

(Note: Refer to Typical Application for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.

Power Sequencing

VCC normally connects through a high impedance (R5) to the rectified line, with an additional path(R6) to a low voltage, bootstrap on the winding power transformer. VFWD normally connects to a divider (R1 and R2) from the rectified line. For circuit activation, all of the following considerations are required:

1. VFWD between 1V and 4V
2. VCC has been under 9V (to reset the shutdown latch)
3. VCC over 13V

At this time, the circuit will activate. I_{VCC} will increase from its start up value of 85µA to its run value of 1mA. The capacitor on SOFTST is charged with a current determined by:

$$-I_{SOFTST} = \frac{1V}{R4}.$$

When SOFTST rises above 1V, output pulses will begin and I_{VCC} will further rise to a level dictated by gate charge requirements as$I_{VCC} \approx$ 1mA + QTfs. With output pulses, the low voltage bootstrap winding should now power the controller. If VCC falls below 9V, the controller will turn off and the start sequence will reset and retry.

VCC Clamp

An internal shunt regulator clamps VCC so that it will not exceed 15V.

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and back low when RAMP either crosses FEEDBK or equals 4V. If, however, any of the following occur, OUT is immediately driven low for the remainder of the clock period:

1. VFWD is outside the range of 1V to 4V
2. CURLIM is greater than 0.2V
3. FEEDBK or SOFTST is less than 1V

Normal output pulses will not resume until the beginning of the next clock period in which none of the above conditions exist.

Current Limiting

CURLIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse overcurrent control for excessive loads. This comparator also causes C_F to be charged for the remainder of the clock cycle. The charging current is

$$-I_{COUNT} = \frac{1V}{R4}.$$

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than $\frac{(4 \bullet R4)}{(1 - D_{MAX})}$.

APPLICATION INFORMATION (cont.)

Latched Shutdown

If CURLIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SOFTST and COUNT, and reduce I_{VCC} to approximately 1mA. When, and if, VCC falls below 9V, the shutdown latch will reset and I_{VCC} will fall to 85µA, allowing the circuit to restart. If VCC remains above 9V, an alternate restart will occur if VFWD is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or CURLIM pins.

Deadtime Control

The voltage waveform on RAMP has independently controlled rising and falling edges. At the start of the clock period, RAMP is at 1V and rises to 4V. It then discharges back to 1V and awaits the next clock period. OUT can only be high during the rising part of the waveform, while it is positively blanked off during the falling portion. Setting the –dV/dt slope by R4 from ISET to GND establishes a minimum deadtime as:

$$td = 0.3 \bullet R4 \bullet C_R$$

Choose R4 between 20k and 200k and C_R greater than 50pF. In order to have a pulse at OUT in the next clock period, RAMP must fall to 1V prior to the end of the current period. If it does not, OUT will remain low for the entire next clock period.

Voltage Feedforward

The +dV/dt on RAMP is made proportional to line voltage. The slope is:

$$\frac{dV}{dt} = 10 \bullet \frac{VFWD}{(R3 \bullet C_R)}$$

where VFWD is line voltage scaled by R1 and R2. Therefore, a changing line voltage will accomplish an immediate proportionate pulse width change without any action from the feedback amplifier. This will result in constant volt-second drive to the power transformer providing both international voltage operation, and excellent dynamic line regulation. VFWD is intended to operate over a 4:1 range (1V to 4V) with undervoltage and overvoltage sensors designed to drive OUT low if this range is exceeded. Choose R3 between 20k and 200k.

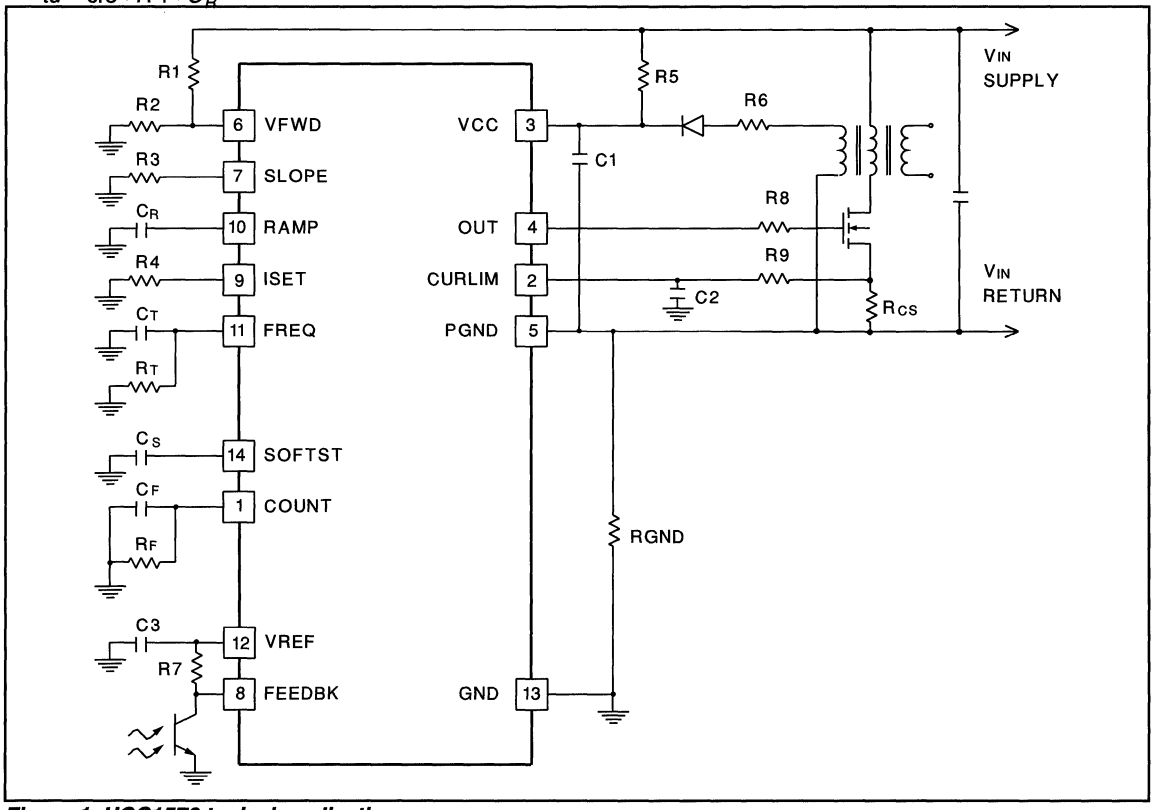


Figure 1. UCC1570 typical application.

APPLICATION INFORMATION (cont.)

Frequency Set

A capacitor from FREQ to GND will determine a constant clock frequency. Frequency is:

$$F = \frac{1.8}{(R4 \bullet C_T)}$$

If required, frequency can be trimmed down from the above equation by the addition of R_T from FREQ to GND. The reduction in frequency is a function of the ratio of $R_T/R4$. R_T should be greater than 2.4 • R4 for reliable operation.

External synchronization can be accomplished by coupling a narrow pulse to a resistor inserted in series with the ground side of C_T. The value should be less than R4/200 and the synchronizing pulse width should be less than 5% of the oscillator period.

External synchronization can also be accomplished by driving FREQ with an CMOS inverter. The inverter must be able to sink (4 • I4) with at a voltage less than the 3.5V upper threshold of the oscillator. It must also be able to source 36 • I4 at a voltage greater than the 1.5V lower threshold of the oscillator. As long as FREQ is held high, the output is guaranteed to be low.

Gate Drive Output

The UCC1570 is capable of 1A peak output current. Bypass VCC with at least 0.1µF directly to PGND. Use a capacitor with low equivalent series resistance and inductance. The connection from OUT to the MOSFET gate should have a 2Ω or greater damping resistor and the length should be minimized. A low impedance connection must be established between the MOSFET source (or the ground side of the current sense resistor), the VCC bypass capacitor and PGND. PGND should then be connected by a single path (shown as RGND in the application) to GND.

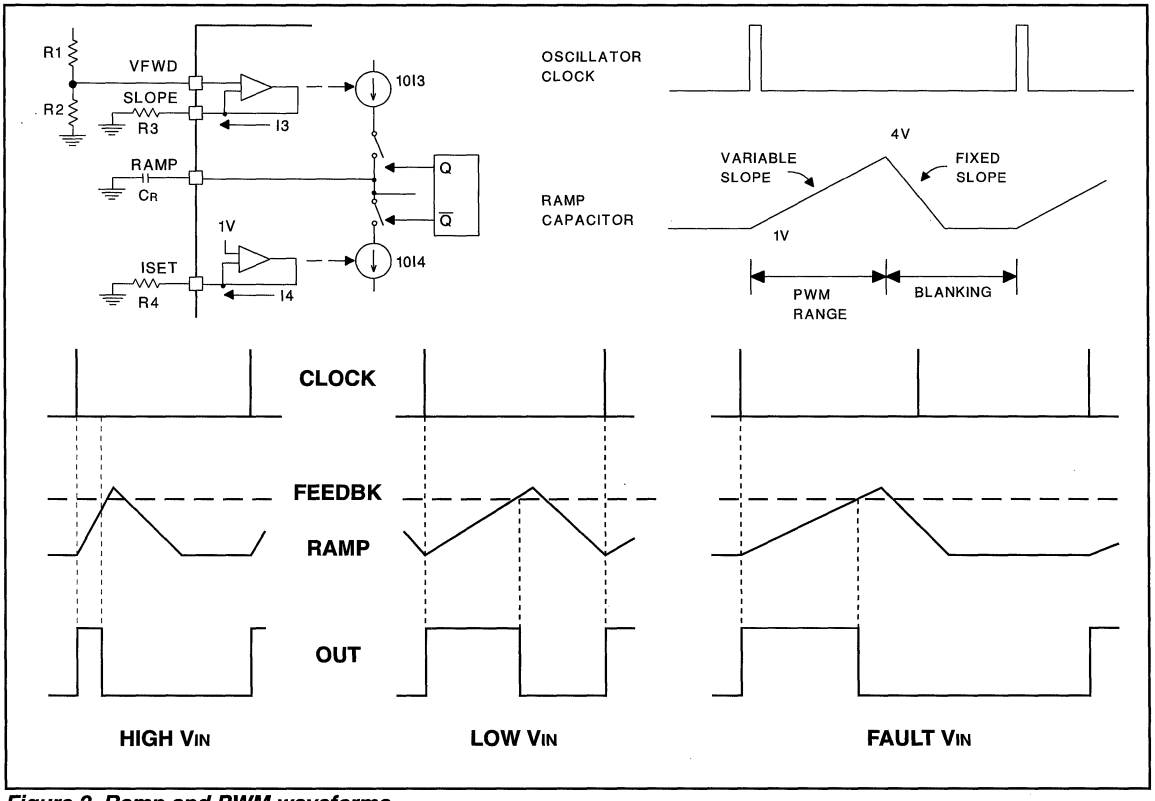


Figure 2. Ramp and PWM waveforms.

APPLICATION INFORMATION (cont.)

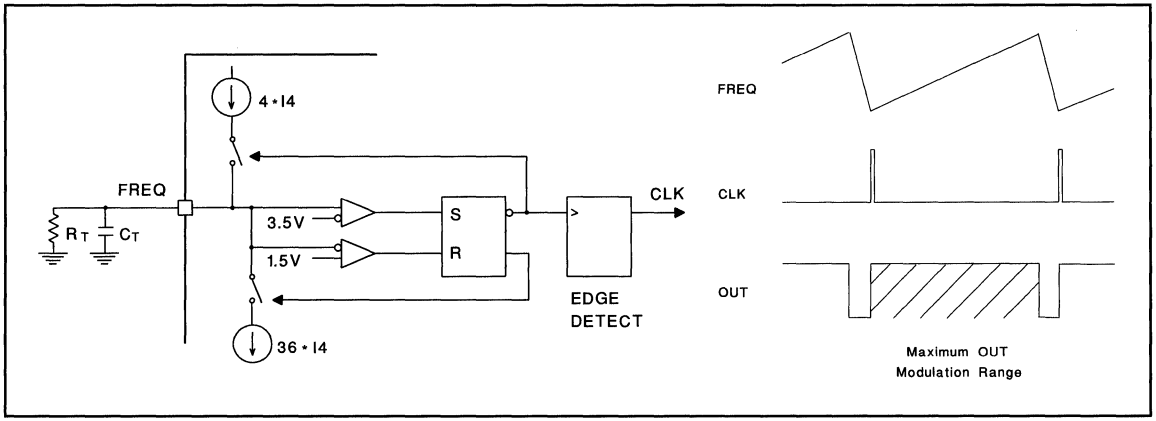


Figure 3. Clock generator.

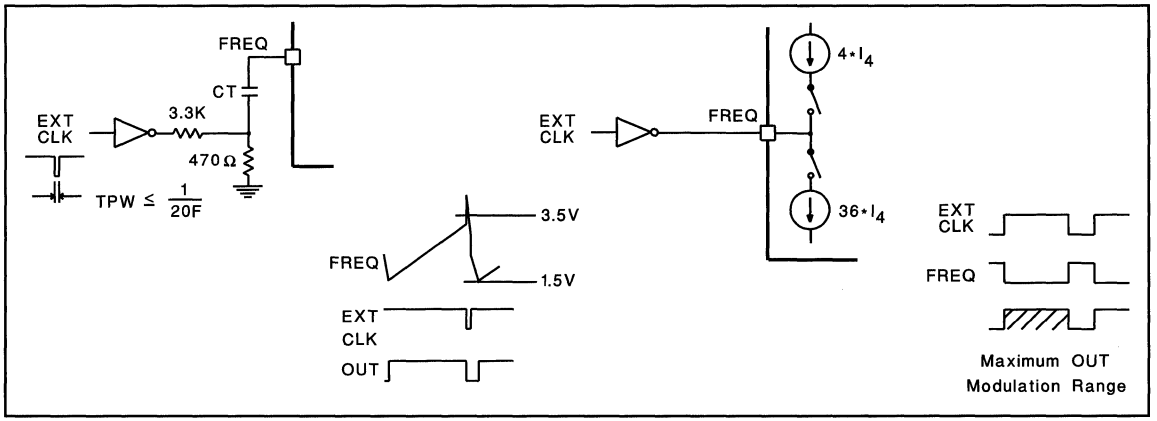


Figure 4. External clock synchronization.

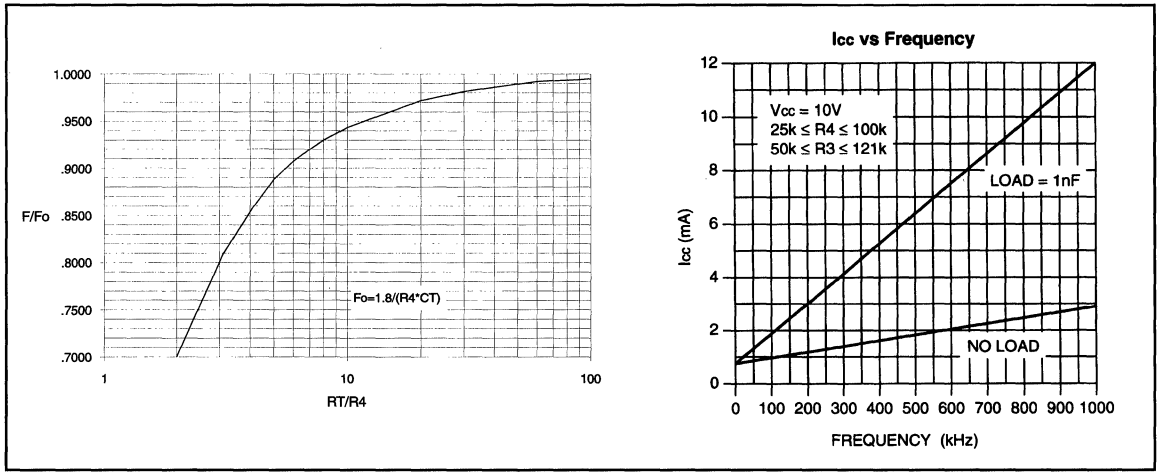
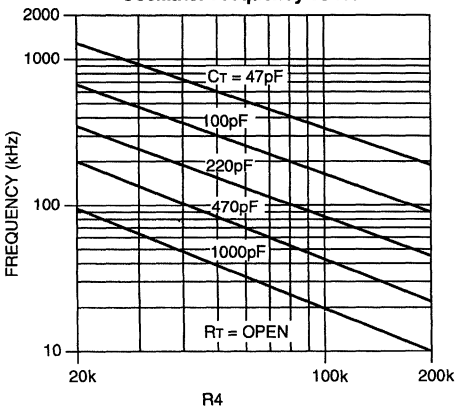


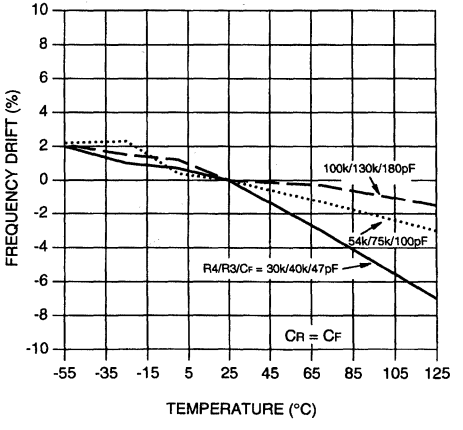
Figure 5. Frequency dependence on RT/ R4 ratio.

APPLICATION INFORMATION (cont.)

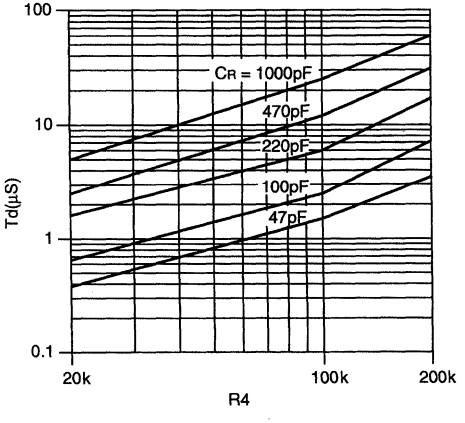
Oscillator Frequency vs R4



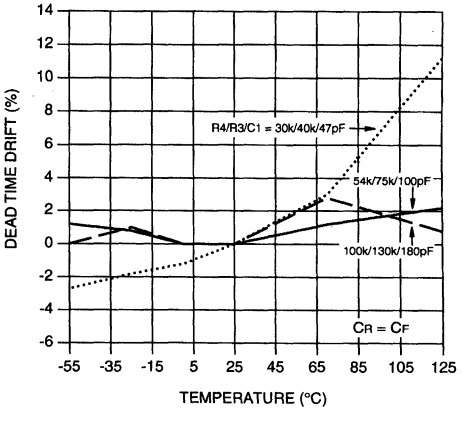
Oscillator Frequency Temperature Drift (%)



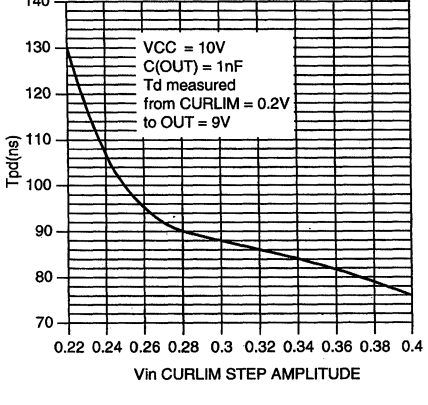
Minimum Dead Time vs R4



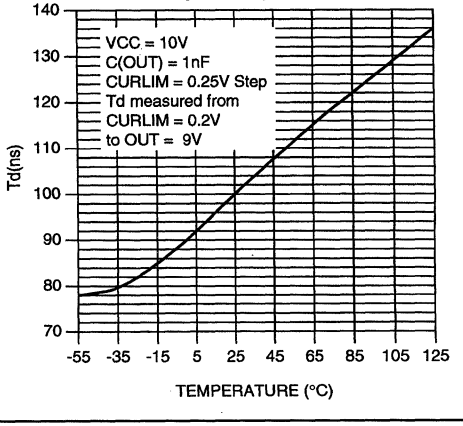
Minimum Dead Time Temperature Drift (%)



CURLIM to OUT Propagation Delay vs Overdrive



CURLIM to OUT Propagation Delay vs Temperature



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application INFO available

UCC15701/2
UCC25701/2
UCC35701/2

Advanced Voltage Mode Pulse Width Modulator

3

FEATURES

- 700kHz operation
- Integrated Oscillator/ Voltage Feed Forward Compensation
- Accuracte Duty Cycle Limit
- Accurate volt-second Clamp
- Optocoupler Interface
- Fault Counting Shutdown
- Fault Latch off or Automatic Shutdown
- 1A Peak Gate Drive Output
- 130µA Start-up Current
- 750µA Operating Current

DESCRIPTION

The UCC35701/UCC35702 family of pulse width modulators is intended for isolated switching power supplies using primary side control. They can be used for both off-line applications and DC/DC converter designs such as in a distributed power system architecture or as a telecom power source.

The devices feature low startup current, allowing for efficient off-line starting, yet have sufficient output drive to switch power MOSFETs in excess of 500kHz.

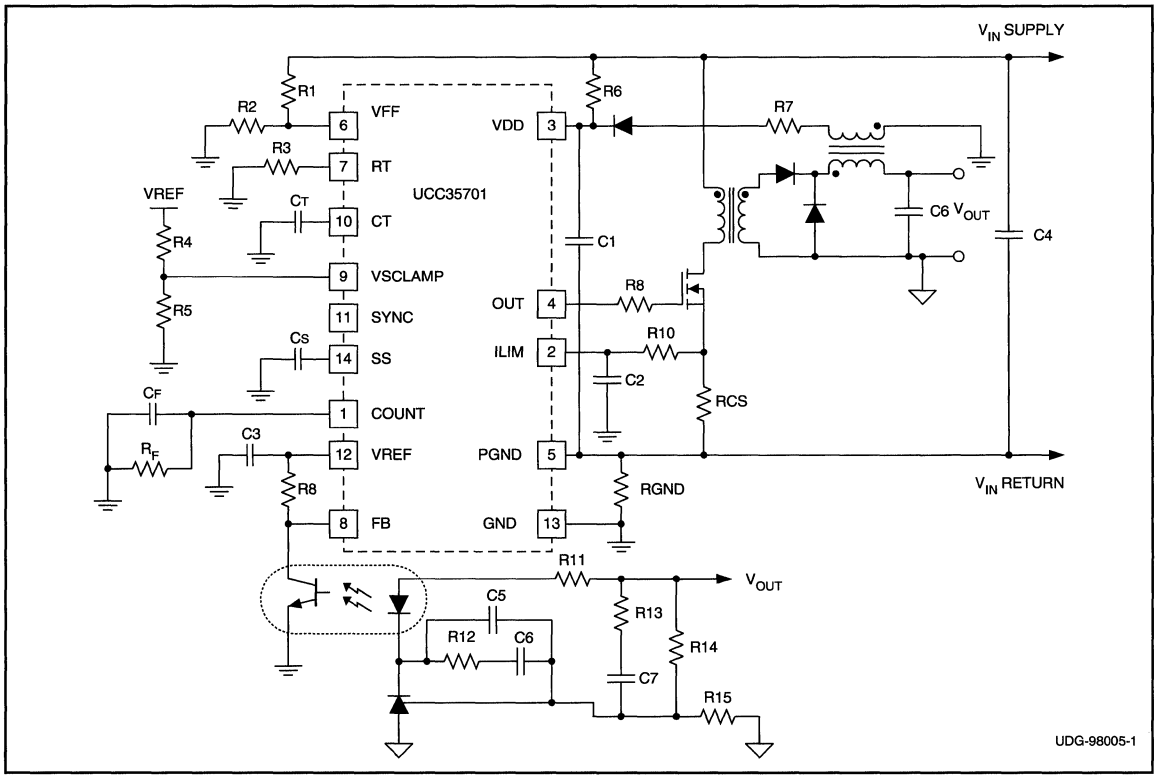
Voltage feed forward compensation provides fast and accurate response to input voltage changes over a 4:1 range. An accurate volt-second clamp and maximum duty cycle limit are also featured.

Fault protection is provided by pulse by pulse current limiting as well as the ability to latch off after a programmable number of repetitive faults has occurred.

Two UVLO options are offered. UCC35701 has turn-on and turn-off thresholds of 13V/9V and UCC35702 has thresholds of 9.9V/9.1V.

The UCC35701/2 and the UCC25701/2 are offered in the 14 pin SOIC (D), 14 pin PDIP (N) or in 14 pin TSSOP (PW) packages. The UCC15701 is offered in the 14 pin CDIP (J) package.

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltage (Supply current limited to 20mA) 15V
Supply Current..... 20mA
Input pins (ILIM,VFF,RT,CT,VSCLAMP,SYNC,SS) 6V
Output Current (OUT) DC ..... +/- 180mA
Output Current (OUT) Pulse (0.5ms)..... +/- 1.2A
Storage Temperature ..... -65°C to +150°C
Junction Temperature..... -55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

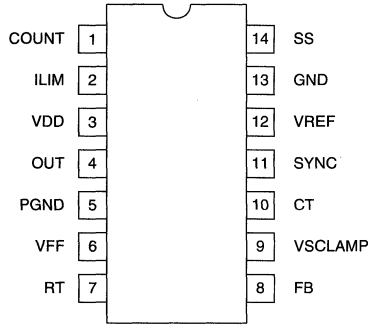
Note: *All voltages are with respect to GND. Currents are positive into the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.*

ORDERING INFORMATION

	$T_A = T_J$	UVLO Option	Package
UCC15701J	–55°C to +125°C	13V / 9V	CDIP-14
UCC15702J		9.9V / 9.1V	CDIP-14
UCC25701D	–40°C to +85°C	12.5V / 8.3V	SOIC-14
UCC25701N		12.5V / 8.3V	PDIP-14
UCC25701PW		12.5V / 8.3V	TSSOP-14
UCC25702D		9.9V / 9.1V	SOIC-14
UCC25702N		9.9V / 9.1V	PDIP-14
UCC25702PW		9.9V / 9.1V	TSSOP-14
UCC35701D	0°C to +70°C	12.5V / 8.3V	SOIC-14
UCC35701N		12.5V / 8.3V	PDIP-14
UCC35701PW		12.5V / 8.3V	TSSOP-14
UCC35702D		9.9V / 9.1V	SOIC-14
UCC35702N		9.9V / 9.1V	PDIP-14
UCC35702PW		9.9V / 9.1V	TSSOP-14

CONNECTION DIAGRAMS

DIL-14, SOIC-14, TSSOP-14 (TOP VIEW)
N or J, D, PW PACKAGE



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 11V, RT = 60.4k, C_T = 330pF, $C_{REF} = C_{VDD}$ = 0.1µF, V_{FF} = 2.0V, and no load on the outputs.

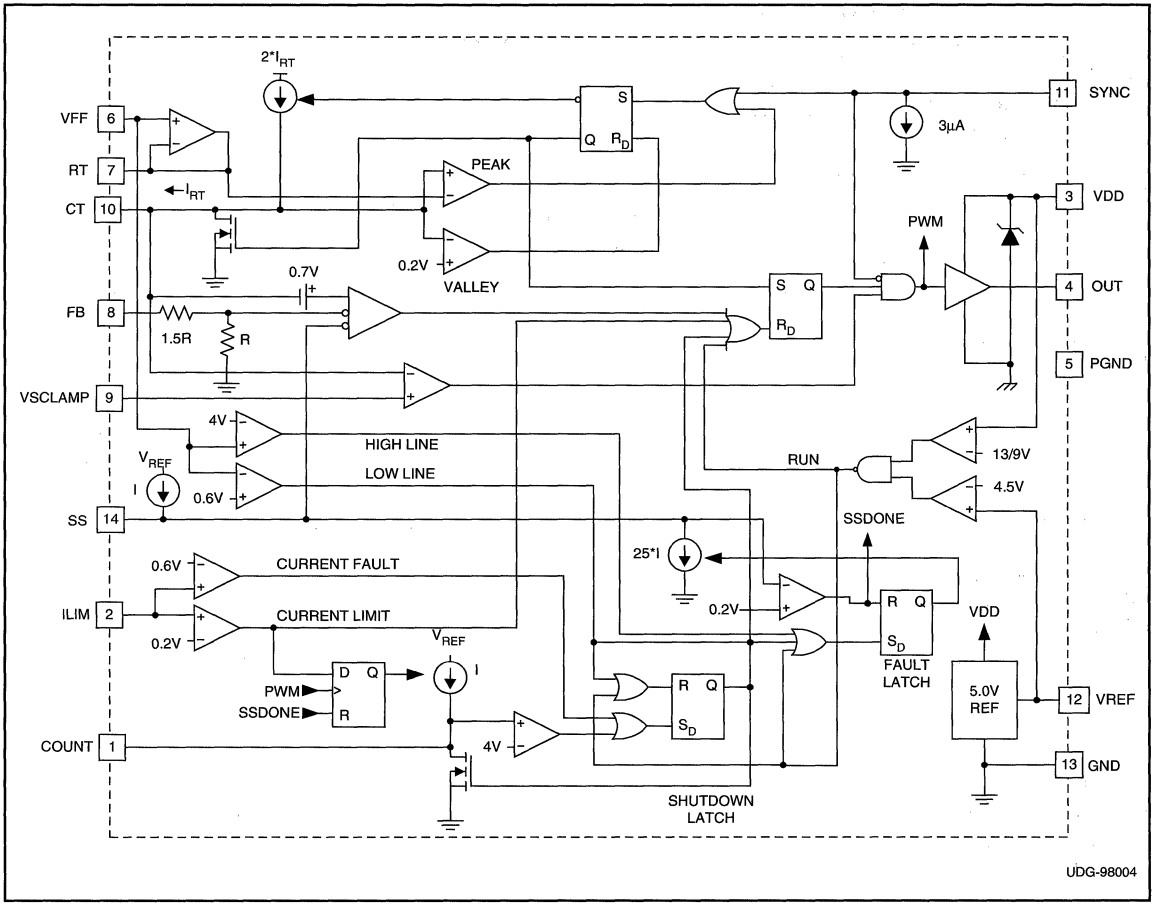
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
Start Threshold	(UCC35701)	12	13	14	V
	(UCC35702)	9.1	9.9	10.7	V
Stop Threshold	(UCC35701)	8	9	10	V
	(UCC35702)	8.5	9.1	9.9	V
	(UCC35701)	3	4	5	V
	(UCC35702)		0.8		V
Supply Current					
Start-up Current	(UCC35701) V_{DD} = 11V, V_{DD} Comparator Off		130	200	µA
	(UCC35702) V_{DD} = 8V, V_{DD} Comparator Off		120	190	µA
I_{DD} Active	V_{DD} Comparator On		0.75	1.5	mA
V_{DD} Clamp Voltage	I_{DD} = 10mA	13.5	14.3	15	V
V_{DD} Clamp – Start Threshold			1		V
Voltage Reference					
V_{REF}	V_{DD} = 10V to 13V, I_{VREF} = 0mA to 2mA	4.9	5	5.1	V
Line Regulation	V_{DD} = 10V to 13V		20		mV
Load Regulation	I_{VREF} = 0mA to 2mA		2		mV
Short Circuit Current	V_{REF} = 0V, TJ = 25°C		20	50	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, V_{DD} = 11V, RT = 60.4k, C_T = 330pF, C_{REF} = C_{VDD} = 0.1µF, V_{FF} = 2.0V, and no load on the outputs.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Line Sense					
Vth High Line Comparator		3.9	4	4.1	V
Vth Low Line Comparator		0.5	0.6	0.7	V
Input Bias Current		–100		100	nA
Oscillator Section					
Frequency	V_{FF} = 0.8V to 3.2V	90	100	110	kHz
Frequency	V_{FF} = 0.6V to 3.4V (Note 1)	90	100	110	kHz
SYNC VIH		2			V
SYNC VIL				0.8	V
SYNC Input Current	VSYNC = 2.0V		3	10	µA
RT Voltage	VFF = 0.4V	0.5	0.6	0.7	V
	VFF = 0.8V	0.75	0.8	0.85	V
	VFF = 2.0V	1.95	2.0	2.05	V
	VFF = 3.2V	3.15	3.2	3.25	V
	VFF = 3.6V	3.3	3.4	3.5	V
C_T Peak Voltage	VFF = 0.8V (Note 1)		0.8		V
	VFF = 3.2V (Note 1)		3.2		V
C_T Valley Voltage	(Note 1)		0		V
Soft Start/Shutdown/Duty Cycle Control Section					
I_{SS} Charging Current		10	18	30	µA
I_{SS} Discharging Current		300	500	750	µA
Saturation	V_{DD} = 11V, IC Off		25	100	mV
Fault Counter Section					
Threshold Voltage	VFF = 0.8V to 3.2V	3.8	4	4.2	V
Saturation Voltage	VFF = 0.8V to 3.2V			100	mV
Count Charging Current		10	18	30	µA
Current Limit Section					
Input Bias Current		–100	0	100	nA
Current Limit Threshold		180	200	220	mV
Shutdown Threshold		500	600	700	mV
Pulse Width Modulator Section					
FB Pin Input Impedance	VFB = 3V	30	50	100	kΩ
Minimum Duty Cycle	VFB <= 1V			0	%
Maximum Duty Cycle	VFB >= 4.5V, VSCLAMP >= 2.0V	95	99	100	%
PWM Gain	VFF = 0.8V	35	50	70	%/V
Volt Second Clamp Section					
Maximum Duty Cycle	VFF = 0.8V, VSCLAMP = 0.6V	69	74	79	%
Minimum Duty Cycle	VFF = 3.2V, VSCLAMP = 0.6V	17	19	21	%
Output Section					
VOH	I_{OUT} = –100mA, (V_{DD} – V_{OUT})		0.4	1	V
VOL	I_{OUT} = 100mA		0.4	1	V
Rise Time	C_{LOAD} = 1000pF		20	100	ns
Fall Time	C_{LOAD} = 1000pF		20	100	ns

Note 1: Guaranteed by design. Not 100% tested in production.

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

VDD: Power supply pin. A shunt regulator limits supply voltage to 14V typical at 10mA shunt current.

PGND: Power Ground. Ground return for output driver and currents.

GND: Analog Ground. Ground return for all other circuits. This pin must be connected directly to PGND on the board.

OUT: Gate drive output. Output resistance is 10Ω maximum.

VFF: Voltage feedforward pin. This pin connects to the power supply input voltage through a resistive divider and provides feedforward compensation over a 0.8V to 3.2V range. A voltage greater than 4.0V or less than 0.6V on this pin initiates a soft stop cycle.

RT: The voltage on this pin mirrors VFF over a 0.8V to 3.2V range. A resistor to ground sets the ramp capacitor charge current. The resistor value should be between 20k and 200k.

CT: A capacitor to ground provides the oscillator/ feedforward sawtooth waveform. Charge current is 2 • I_{RT}, resulting in a CT slope proportional to the input voltage. The ramp voltage range is GND to V_{RT}.

Period and oscillator frequency is given by:

$$T = \frac{V_{RT} \bullet C_T}{2 \bullet I_{RT}} + t_{DISCH} \approx 0.5 \bullet R_T \bullet C_T$$

$$F \approx \frac{2}{RT \bullet CT}$$

PIN DESCRIPTIONS (cont.)

VSCLAMP: Voltage at this pin is compared to the CT voltage, providing a constant volt-second limit. The comparator output terminates the PWM pulse when the ramp voltage exceeds VSCLAMP. The maximum on time is given by:

$$t_{ON} = \frac{V_{VSCLAMP} \bullet CT}{2 \bullet I_{RT}}$$

The maximum duty cycle limit is given by:

$$D_{MAX} = \frac{t_{ON}}{T} = \frac{V_{VSCLAMP}}{V_{RT}}$$

FB: Input to the PWM comparator. This pin is intended to be driven with an optocoupler circuit. Input impedance is 50kΩ. Typical modulation range is 1.6V to 3.6V.

SYNC: Level sensitive oscillator sync input. A high level forces the gate drive output low and resets the ramp capacitor. On-time starts at the negative edge the pulse. There is a 3µA pull down current on the pin, allowing it to be disconnected when not used.

VREF: 5.0V trimmed reference with 2% variation over line, load and temperature. Bypass with a minimum of 0.1µF to ground.

SS: Soft start pin. At power up, a capacitor to ground is charged with a nominal 15µA to V_{REF}. A soft start cycle is initiated either at power up or after a fault condition discharges the soft start capacitor with a controlled discharge current of ~450µA.

A low line, high line, UVLO, or a low V_{REF} fault will follow the soft stop with a soft start cycle as soon as all faults are cleared. A current fault (0.6V on ILIM) or COUNT fault will cause a latched soft stop. In this case, dropping V_{DD} below 9V, or VFF below 600mV will initiate a soft start cycle AFTER the voltage at SS is below 200mV.

ILIM: Provides a pulse by pulse current limit by terminating the PWM pulse when the input is above 200mV. An input over 600mV initiates a latched soft stop cycle.

COUNT: Capacitor to ground integrates current pulses generated when ILIM exceeds 200mV. A resistor to ground sets the discharge time constant. A voltage over 4V will initiate a latched soft stop cycle.

APPLICATION INFORMATION

*(**Note**: Refer to the Typical Application Diagram on the first page of this datasheet for external component names.) All the equations given below should be considered as first order approximations with final values determined empirically for a specific application.*

Power Sequencing

VDD is normally connected through a high impedance (R6) to the input line, with an additional path (R7) to a low voltage bootstrap winding on the power transformer. VFF is connected through a divider (R1/R2) to the input line.

For circuit activation, all of the following conditions are required:

1. VFF between 0.6V and 4.0V

2. VDD has been under 9V to reset the shutdown latch

3. VDD is over 13V for UCC35701/2 or over 9.9V for UCC35702.

The circuit will start at this point. I_{VDD} will increase from the start up value of 130µA to the run value of 1mA. The capacitor on SS is charged with a 15µA current. When the voltage on SS is greater than 0.8V, output pulses can begin, and supply current will increase to a level determined by the MOSFET gate charge requirements to I_{VDD} ~ 1mA + QT • fs. When the output is active, the bootstrap winding should be sourcing the supply current. If VDD falls below 9V, the controller will enter a shutdown sequence and turn the controller off, returning the start sequence to the initial condition.

VDD Clamp

An internal shunt regulator clamps VDD so the voltage does not exceed 14V. If the regulator is active, supply current must be limited to less than 20mA.

Output Inhibit

During normal operation, OUT is driven high at the start of a clock period and is driven low by voltages on CT, FB or VSCLAMP.

The following conditions cause the output to be immediately driven low until a clock period starts where none of the conditions are true:

1. $I_{LIM} > 0.2V$

2. FB or SS is less than 0.8V

Current Limiting

ILIM is monitored by two internal comparators. The current limit comparator threshold is 0.2V. If the current limit comparator is triggered, OUT is immediately driven low and held low for the remainder of the clock cycle, providing pulse-by-pulse over-current control for excessive

APPLICATION INFORMATION (cont.)

loads. This comparator also causes C_F to be charged for the remainder of the clock cycle.

If repetitive cycles are terminated by the current limit comparator causing COUNT to rise above 4V, the shutdown latch is set. The COUNT integration delay feature will be bypassed by the shutdown comparator which has a 0.6V threshold. The shutdown comparator immediately sets the shutdown latch. R_F in parallel with C_F resets the COUNT integrator following transient faults. R_F must be greater than $(4 \bullet R4) \bullet (1 - D_{MAX})$.

Latched Shutdown

If ILIM rises above 0.6V, or COUNT rises to 4V, the shutdown latch will be set. This will force OUT low, discharge SS and COUNT, and reduce I_{DD} to approximately 1mA. When, and if, V_{DD} falls below 9V, the shutdown latch will reset and I_{DD} will fall to 130µA, allowing the circuit to restart. If V_{DD} remains above 9V, an alternate restart will occur if VFF is momentarily reduced below 1V. External shutdown commands from any source may be added into either the COUNT or ILIM pins.

Voltage Feedforward

The voltage slope on CT is proportional to line voltage over a 4:1 range and equals 2•VFF/(RT•CT). The capacitor charging current is set by the voltage across R_T. V(RT) tracks VFF over a range of 0.8V to 3.2V. A changing line voltage will immediately change the slope of V(CT), changing the pulse width in a proportional manner without using the feedback loop, providing excellent dynamic line regulation.

VFF is intended to operate over a 4:1 range between 0.8V and 3.2V. Voltages at VFF below 0.6V or above 4.0V will initiate a soft stop cycle and a chip restart when the under/over voltage condition is removed.

Volt-Second Clamp

A constant volt-second clamp is formed by comparing the timing capacitor ramp voltage to a fixed voltage derived from the reference. Resistors R4 and R5 set the volt-second limit. For a volt-second product defined as $VIN \bullet t_{ON(max)}$, the required voltage at VSCLAMP is:

$$\frac{\left(\frac{R2}{R1+R2}\right) \bullet \left(V_{IN} \bullet t_{ON(max)}\right)}{R_T \bullet C_T}.$$

The duty cycle limit is then:

$$\frac{V_{VSCLAMP}}{V_{VFF}}, \text{ or } \frac{V_{VSCLAMP}}{V_{IN} \bullet \left(\frac{R2}{R1+R2}\right)}.$$

The maximum duty cycle is realized when the feedforward voltage is set at the low end of the operating range. The absolute maximum duty cycle is:

$$D_{MAX} = \frac{V_{VSCLAMP}}{0.8}$$

Frequency Set

The frequency is set by a resistor from RT to ground and a capacitor from CT to ground. The frequency is approximately: $F = \frac{2}{(R_T \bullet C_T)}$

TYPICAL WAVEFORMS

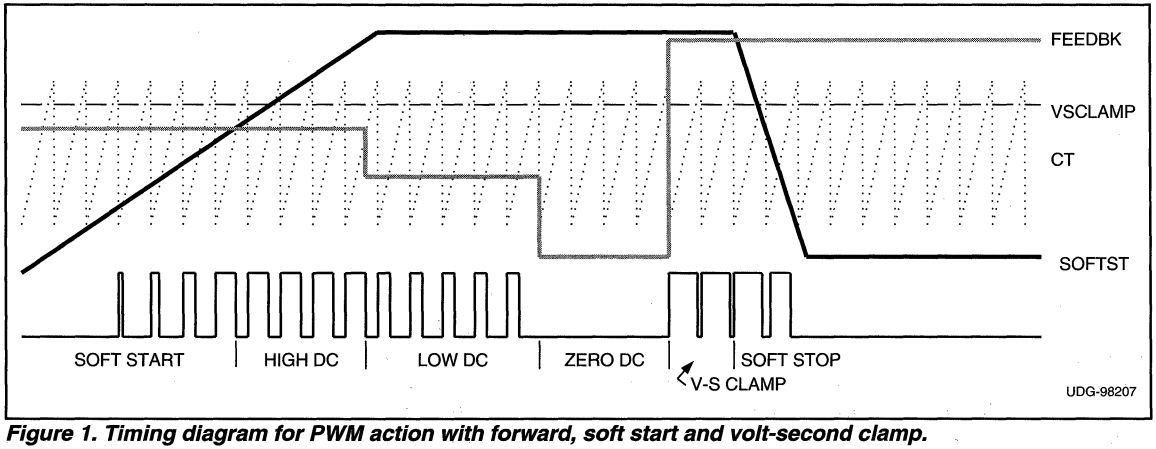


Figure 1. Timing diagram for PWM action with forward, soft start and volt-second clamp.

TYPICAL WAVEFORMS (cont.)

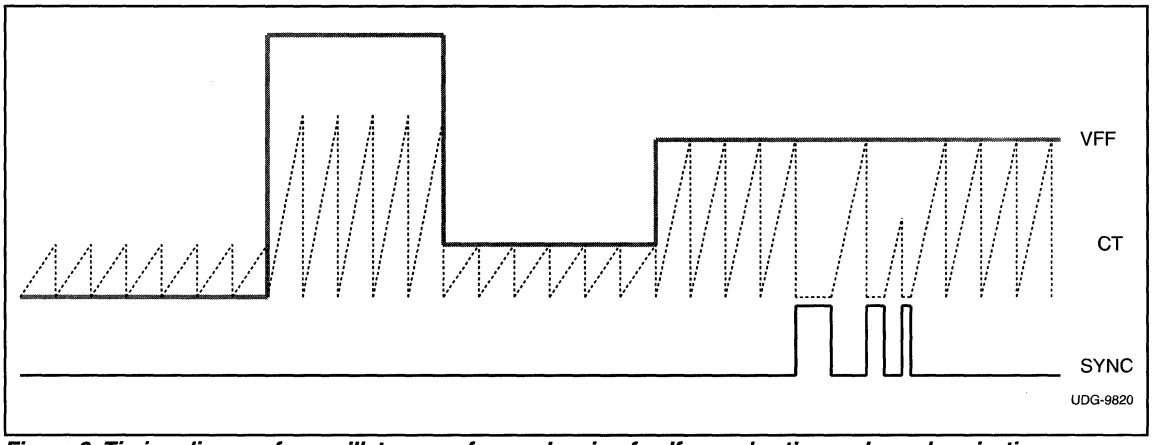


Figure 2. Timing diagram for oscillator waveforms showing feedforward action and synchronization.

TYPICAL CHARACTERISTIC CURVES

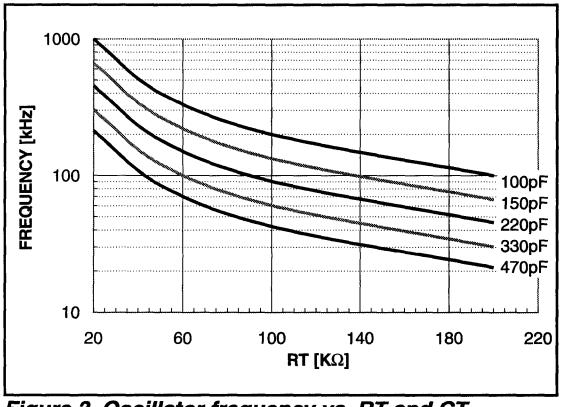


Figure 3. Oscillator frequency vs. RT and CT.

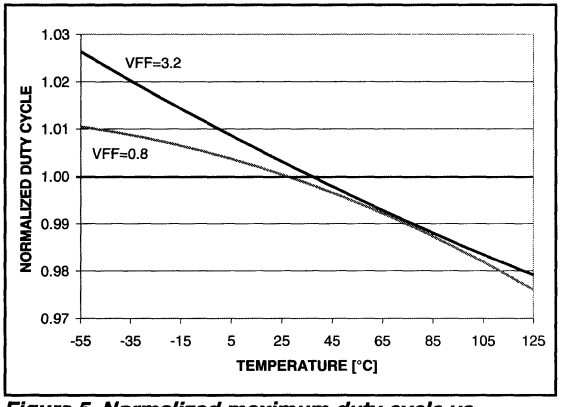


Figure 5. Normalized maximum duty cycle vs. temperature.

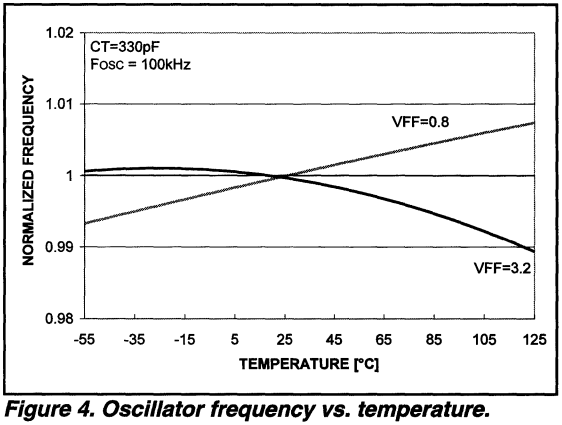


Figure 4. Oscillator frequency vs. temperature.

APPLICATION INFORMATION (cont.)

External synchronization is via the SYNC pin. The pin has a 1.5V threshold , making it compatible with 5V and 3.3V CMOS logic. The input is level sensitive, with a high input forcing the oscillator ramp low and the output low. An active pull down on the SYNC pin allows it to be unconnected when not used.

Gate Drive Output

The UCC35701/2 is capable of a 1A peak output current. Bypass V_{DD} with at least 0.1µF directly to PGND. The capacitor must have a low equivalent series resistance and inductance. The connection from OUT to the power MOSFET gate should have a 2Ω or greater damping resistor and the distance between chip and MOSFET should be minimized. A low impedance path must be established between the MOSFET source (or ground side of the current sense resistor), the V_{DD} capacitor and PGND. PGND should then be connected by a single path (shown as RGND) to GND.

Transitioning From UCC3570 To UCC35701

The UCC35701/2 is an advanced version of the popular, low power UCC3570 PWM. Significant improvements were made to the IC's oscillator and PWM control sections to enhance overall system performance. All of the key attributes and functional blocks of the UCC3570 were maintained in the UCC35701/2. A typical application using UCC3570 and UCC35701/2 is shown in Fig. 6 for comparison.

The advantages of the UCC35701/2 over the UCC3570 are as follows.

- Improved oscillator and PWM control section.
- A precise maximum volt-second clamp circuit. The UCC3570 has a dual time base between oscillator and feedforward circuitry. The integated time base in UCC35701/2 improves the duty cycle clamp accuracy, providing better than ± 5% accurate volt- second clamp over full temperature range.
- Separately programmable oscillator timing resistor (RT) and capacitor (CT) circuits provide a higher degree of versatility.
- An independent SYNC input pin for simple external synchronization.
- A smaller value filter capacitor (0.1µF) can be used with the enhanced reference voltage.

UCC35701/2 is pin to pin compatible to UCC3570 but is not a direct drop-in replacement for UCC3570 sockets. The changes required to the power supply printed circuit board of for existing UCC3570 designs are minimal. For conversion, only one extra resistor to set the volt-second clamp needs to be added to the existing PC board layouts. In addition, some component values will need to be changed due to the functionality change in of four of the IC pins.

The Pinout Changes from UCC3570 are as follows.

- Pin 7 was changed from SLOPE to RT (for timing resistor)
- Pin 8 was changed from ISET to VSCLAMP (requiring one additional resistor from pin 9 to VREF)
- Pin 10 was changed from RAMP to CT (single timing capacitor)
- Pin 11 was changed from FREQ to SYNC (input only)

Additional Information

Please refer to the following two Unitrode application topics for additional information. They are available in the Unitrode Applications Handbook.

[1] Application Note U-150, *Applying the UCC3570 Voltage-Mode PWM Controller to Both Off-line and DC/DC Converter Designs* by Robert A. Mammano

[2] Design Note DN-62, *Switching Power Supply Topology, Voltage Mode vs. Current Mode* by Robert Mammano

APPLICATION INFORMATION

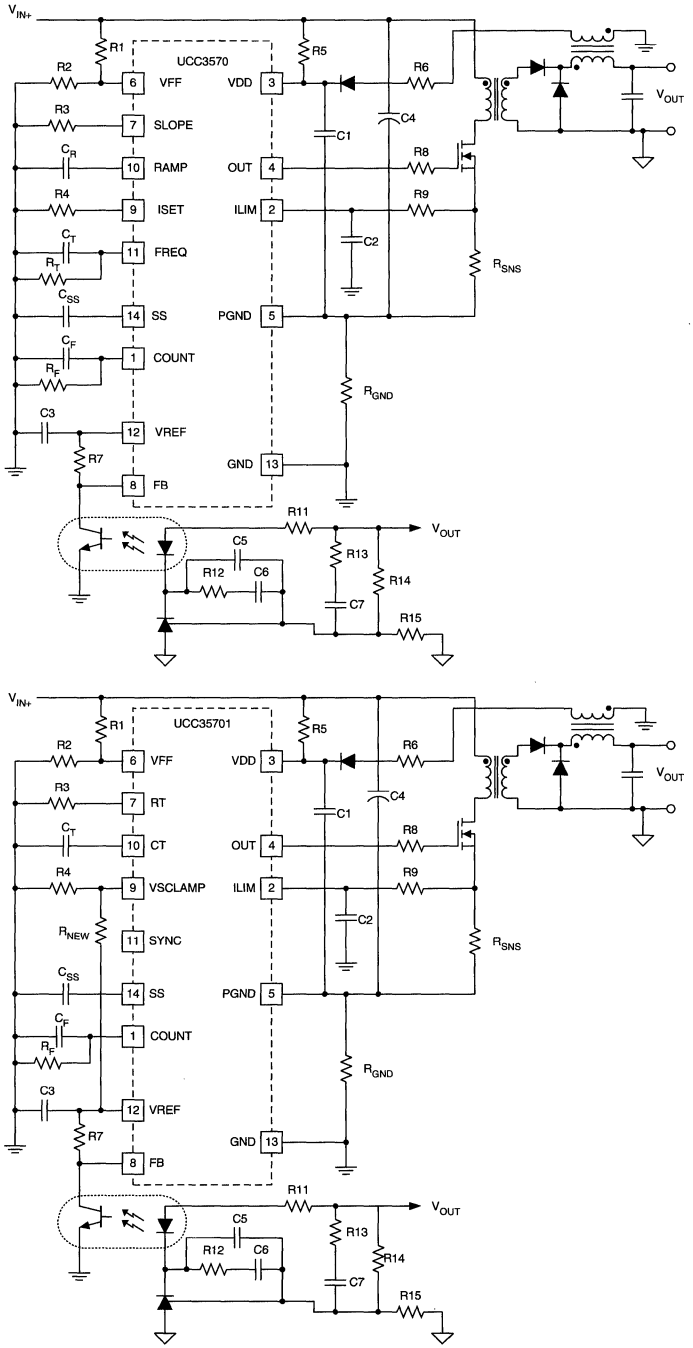


Figure 6. Single-ended forward circuit comparison between UCC3750 and UCC37501.

UNITRODE CORPORATION
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Negative Output Flyback Pulse Width Modulator

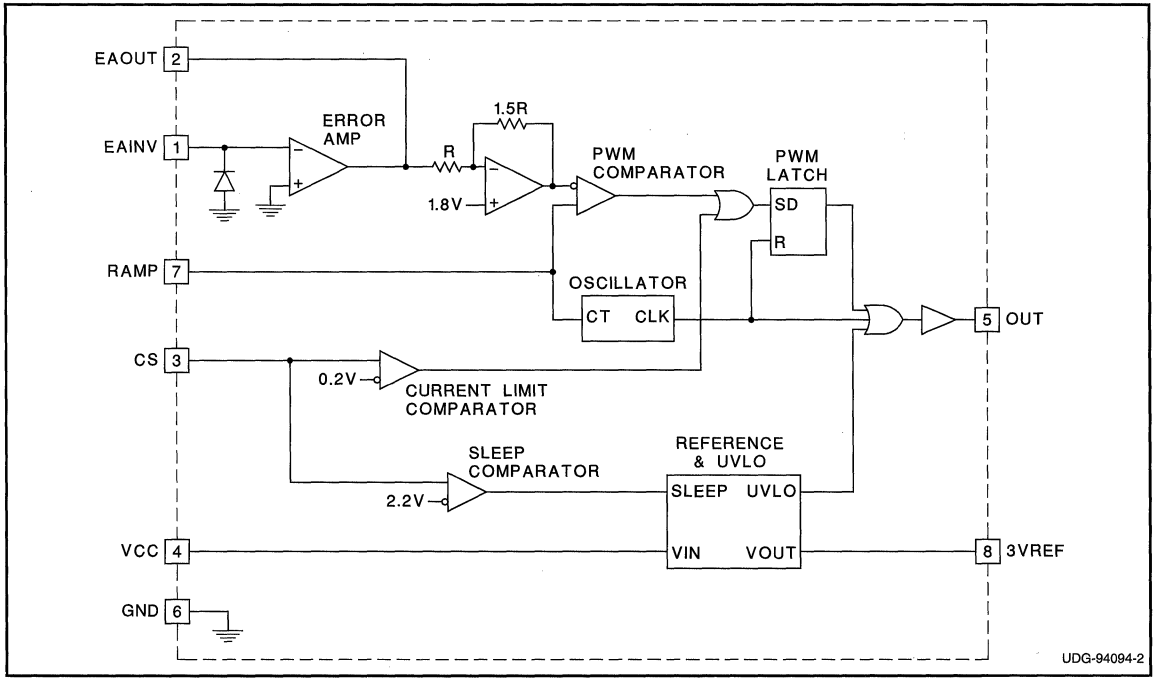
FEATURES

- Simple Single Inductor Flyback PWM for Negative Voltage Generation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50µA Sleep Mode Current

DESCRIPTION

The UC3572 is a negative output flyback pulse width modulator which converts a positive input voltage to a regulated negative output voltage. The chip is optimized for use in a single inductor negative flyback switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3572 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Output current can be sensed and limited to a user determined maximum value. The UVLO circuit turns the chip off when the input voltage is below the UVLO threshold. In addition, a sleep comparator interfaces to the UVLO circuit to turn the chip off. This reduces the supply current to only 50µA, making the UC3572 ideal for battery powered applications.

BLOCK DIAGRAM



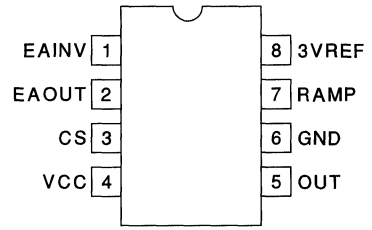
ABSOLUTE MAXIMUM RATINGS

VCC 35V
EAINV . . . . . -0.6V to VCC
I_{EAOUT} 25mA
RAMP . . . . . -0.3V to 4V
CS . . . . . -0.3V to VCC
Iout . . . . . -0.7A to 0.7A
I_{3VREF} . . . . . -15mA
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (TOP VIEW)
D, N or J Packages



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1572	–55°C to +125°C	J
UC2572	–40°C to +85°C	D, N or J
UC3572	0°C to +70°C	D or N

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I_{3VREF} = 0V to –5mA		1	10	mV
Oscillator Section					
Frequency	VCC = 5V to 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	–10	0	10	mV
	I_{EANV} = –1mA		–0.2	–0.9	V
I_{EAINV}	EAOUT = 2V		–0.2	–1.0	µA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = –100mV	3.6	4	4.4	V
EAOUT Low	EAINV = 100mV		0.1	0.2	V
I_{EAOUT}	EAINV = –100mV, EAOUT = 2V	–350	–500		µA
	EAINV = 100mV, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T_J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold		0.195	0.215	0.235	V
Input Bias Current	CS = 0		–0.4	–1	µA
CS Propogation Delay			300		nS
Gate Drive Output Section					
OUT High Saturation	I_{OUT} = 0		0	0.3	V
	I_{OUT} = –10mA		0.7	1.5	V
	I_{OUT} = –100mA		1.5	2.5	V
OUT Low Saturation	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	nS

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drive Output Section (cont.)					
Fall Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	nS
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = +100mV, VCC = 5V to 30V		92	96	%
Minimum Duty Cycle	EAINV = –100mV, VCC = 5V to 30V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	45	55	65	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
IVCC	VCC = 5V, 30V		9	12	mA
	VCC = 30, CS = 3V		50	150	µA

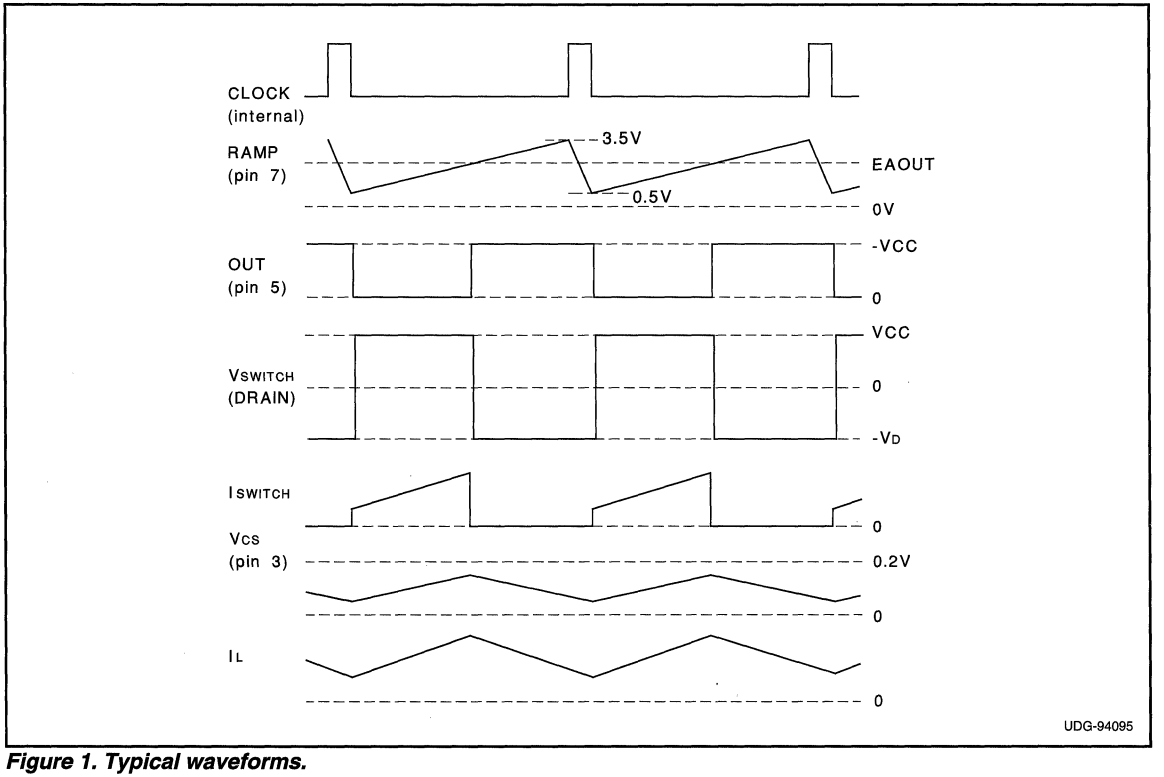


Figure 1. Typical waveforms.

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor to GND.

CS: Current limit sense pin. Connect to a ground referenced current sense resistor in series with the flyback inductor. OUT will be held high (PMOS switch off) if CS exceeds 0.2V.

EAINV: Inverting input to error amplifier. Summing junction for 3VREF and VOUT sense. The non-inverting input of the error amplifier is internally connected to GND. This pin will source a maximum of 1mA.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

OUT: Gate drive for external PMOS switch connected between V_{CC} and the flyback inductor. OUT drives the gate of the PMOS switch between V_{CC} and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \bullet C_{RAMP}}$$

Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75 to 30V. Bypass with a 1µF capacitor.

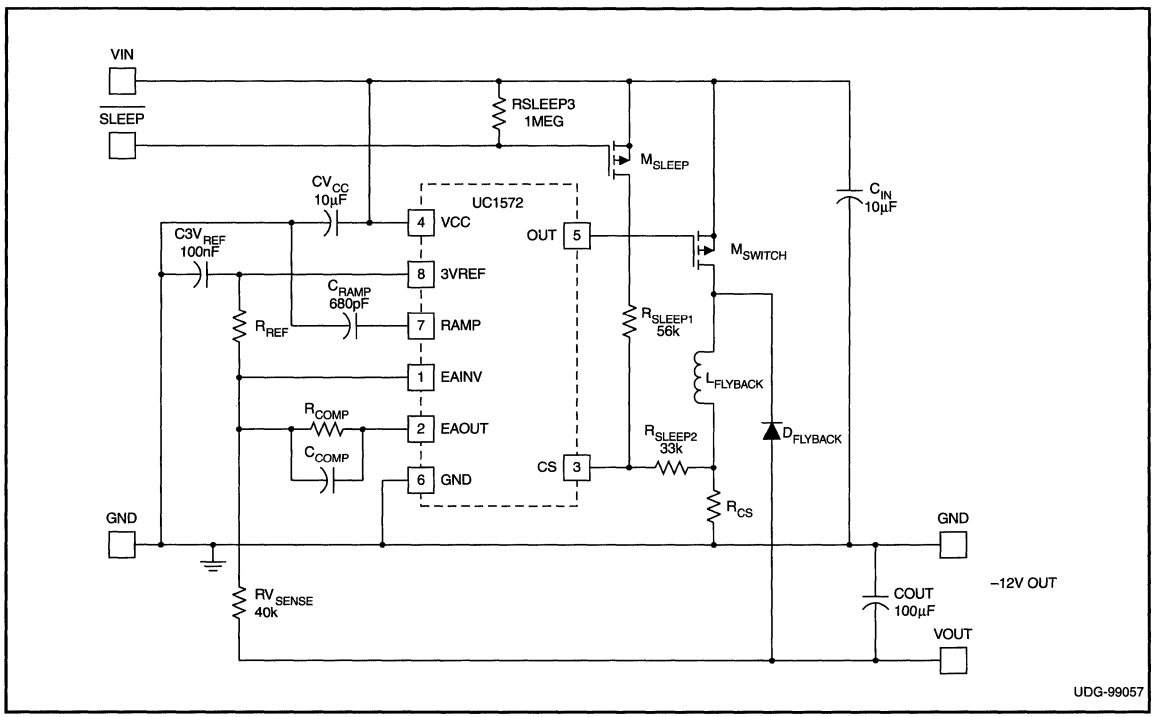


Figure 2. Typical application: +5V to –12V flyback converter.

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application INFO available

UC1573
UC2573
UC3573

Buck Pulse Width Modulator Stepdown Voltage Regulator

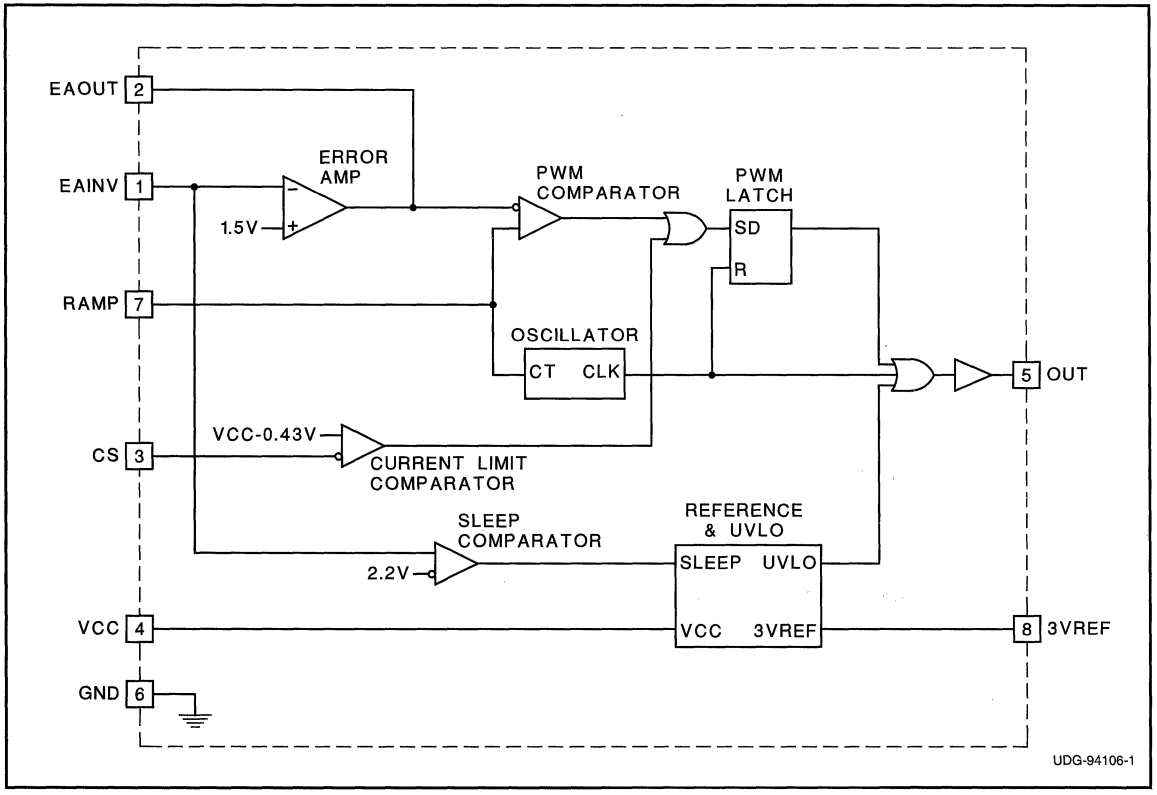
FEATURES

- Simple Single Inductor Buck PWM Stepdown Voltage Regulation
- Drives External PMOS Switch
- Contains UVLO Circuit
- Includes Pulse-by-Pulse Current Limit
- Low 50μA Sleep Mode Current

DESCRIPTION

The UC3573 is a Buck pulse width modulator which steps down and regulates a positive input voltage. The chip is optimized for use in a single inductor buck switching converter employing an external PMOS switch. The block diagram consists of a precision reference, an error amplifier configured for voltage mode operation, an oscillator, a PWM comparator with latching logic, and a 0.5A peak gate driver. The UC3573 includes an undervoltage lockout circuit to insure sufficient input supply voltage is present before any switching activity can occur, and a pulse-by-pulse current limit. Input current can be sensed and limited to a user determined maximum value. In addition, a sleep comparator interfaces to the UVLO circuit which turns the chip off when the input voltage is below the UVLO threshold. This reduces the supply current to only 50μA, making the UC3573 ideal for battery powered applications.

BLOCK DIAGRAM



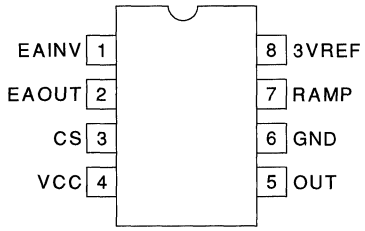
ABSOLUTE MAXIMUM RATINGS

VCC 35V
EAINV . . . . . –0.6V to VCC
I_{EAOUT} 25mA
RAMP . . . . . –0.3V to 4V
CS . . . . . –0.3V to VCC
I_{OUT} . . . . . –0.7A to 0.7A
I_{3VREF} . . . . . –15mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
J or N, D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these parameters apply for T_A = –55°C to +125°C for the UC1573, –40°C to +85°C for the UC2573, and 0°C to +70°C for the UC3573, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
3VREF		2.94	3	3.06	V
Line Regulation	VCC = 4.75 to 30V		1	10	mV
Load Regulation	I_{3VREF} = 0 to –5mA		1	10	mV
Oscillator Section					
Frequency	V_{CC} = 5V, 30V	85	100	115	kHz
Error Amp Section					
EAINV	EAOUT = 2V	1.45	1.5	1.55	V
I_{EAINV}	EAOUT = 2V		–0.2	–1	µA
AVOL	EAOUT = 0.5V to 3V	65	90		dB
EAOUT High	EAINV = 1.4V	3.6	4	4.4	V
EAOUT Low	EAINV = 1.6V		0.1	0.2	V
I_{EAOUT}	EAINV = 1.4V, EAOUT = 2V	–350	–500		µA
	EAINV = 1.6V, EAOUT = 2V	7	20		mA
Unity Gain Bandwidth	T_J = 25°C, F = 10kHz	0.6	1		MHz
Current Sense Comparator Section					
Threshold (referred to VCC)		–0.39	–0.43	–0.47	V
Input Bias Current	CS = VCC		150	800	nA
CS Propagation Delay			400		ns
Gate Drive Output Section					
OUT High Saturation	I_{OUT} = 0		0	0.3	V
	I_{OUT} = –10mA		0.7	1.5	V
	I_{OUT} = –100mA		1.5	2.5	V
OUT Low Saturation	I_{OUT} = 10mA		0.1	0.4	V
	I_{OUT} = 100mA		1.5	2.2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1nF + 3.3 Ohms		30	80	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV = 1.4V		92	96	%
Minimum Duty Cycle	EAINV = 1.6V			0	%
Modulator Gain	EAOUT = 1.5V to 2.5V	25	35	45	%/V
Undervoltage Lockout Section					
Start Threshold		3.5	4.2	4.5	V
Hysteresis		100	200	300	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these parameters apply for T_A = –55°C to +125°C for the UC1573, –40°C to +85°C for the UC2573, and 0°C to +70°C for the UC3573, VCC = 5V, CT = 680pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sleep Mode Section					
Threshold		1.8	2.2	2.6	V
Supply Current Section					
I_{VCC}	VCC = 30V		9	12	mA
I_{VCC}	VCC = 30V, EAINV = 3V		50	150	µA

PIN DESCRIPTIONS

3VREF: Precision 3V reference. Bypass with 100nF capacitor.

CS: Peak current limit sense pin. Senses the current across a current sense resistor placed between VCC and source of the PMOS Buck switch. OUT will be held high (PMOS buck switch off) if VCC – CS exceeds 0.4V.

EAINV: Inverting input to error amplifier. VOUT sense feedback connected to this pin. The non-inverting input of the error amplifier is internally connected to:

$$\frac{3VREF}{2} \quad Volts.$$

Connecting the EAINV pin to an external voltage greater than 2.6V commands the chip to go into a low current sleep mode.

EAOUT: Output of error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground.

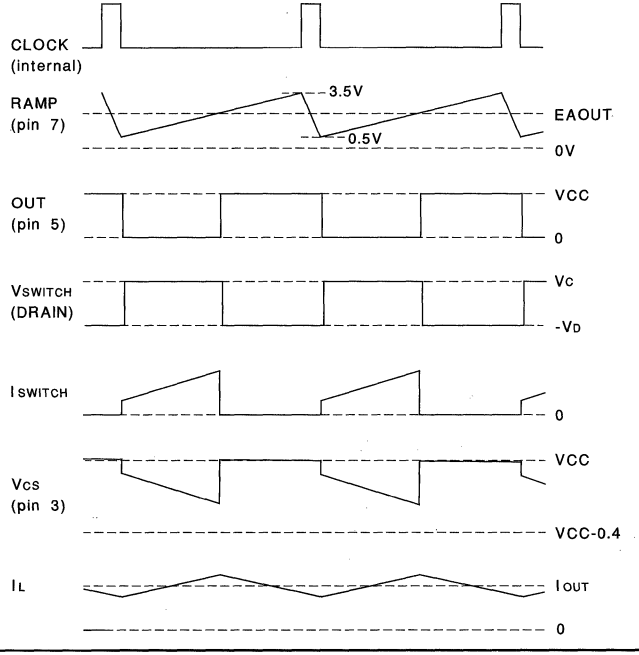
OUT: Gate drive for external PMOS switch connected between VCC and the flyback inductor. OUT drives the gate of the PMOS switch between VCC and GND.

RAMP: Oscillator and ramp for pulse width modulator. Frequency is set by a capacitor to GND by the equation

$$F = \frac{1}{15k \bullet C_{RAMP}}$$

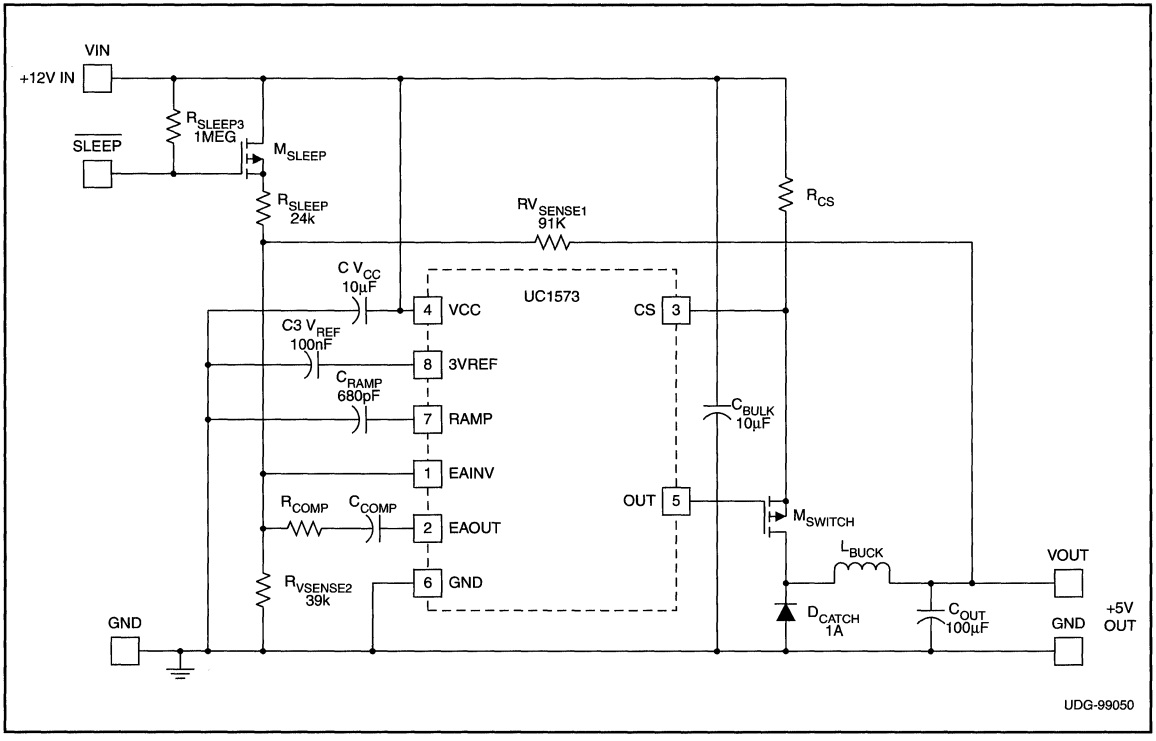
Recommended operating frequency range is 10kHz to 200kHz.

VCC: Input voltage supply to chip. Range is 4.75V to 30V. Bypass with a 1µF capacitor.



Typical Waveforms.

TYPICAL APPLICATION: 12V TO 5V BUCK CONVERTER



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Buck Pulse Width Modulator Stepdown Voltage Regulator

FEATURES

- Provides Simple Single Inductor Buck PWM Step-Down Voltage Regulation
- Drives External High Side NMOS Switch
- 14V to 72V Input Voltage Operating Range
- Contains 100kHz Internal Oscillator, 2V Reference and UVLO
- Soft Start on Power Up
- Overcurrent Shutdown Followed by Soft Start

DESCRIPTION

The UC3578 is a PWM controller with an integrated high side floating gate driver. It is used in buck step down converters and regulates a positive output voltage. Intended to be used in a distributed power system, the IC allows operation from 14V to 72V input voltage which range includes the prevalent telecomm bus voltages. The output duty cycle of the UC3578 can vary between 0% and 90% for operation over the wide input voltage and load conditions.

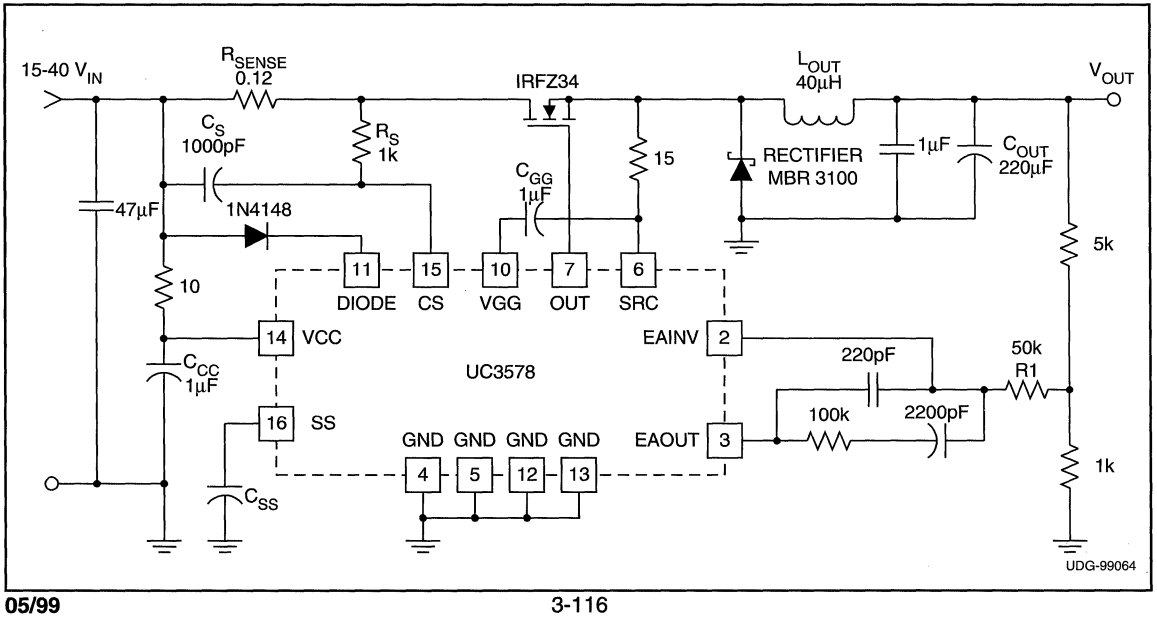
The UC3578 simplifies the design of the single switch PWM buck converter by incorporating a floating high side driver for an external N-channel MOSFET switch. It also features a 100kHz fixed frequency oscillator, an internal 2V precision reference, an error amplifier configured for voltage mode operation, and a PWM comparator with latching logic. Complementing the traditional voltage mode control block, the UC3578 incorporates an overcurrent shutdown circuit with full cycle soft re-start to limit the input current to a user defined maximum value during overload operation. Additional functions include an under voltage lockout circuit to insure that sufficient input supply voltage is present before any switching activity can occur.

The UC2578 and the UC3578 are both available in surface mount and thru-hole power packages.

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC2578DP	–40°C to +85°C	Power SOIC
UC2578N		Power PDIP
UC3578DP	0°C to +70°C	Power SOIC
UC3578N		Power PDIP

TYPICAL APPLICATION DIAGRAM



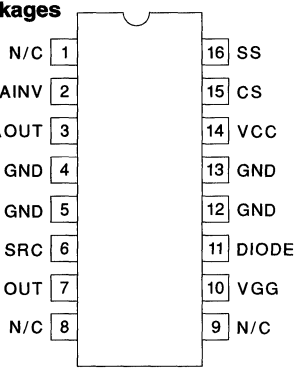
ABSOLUTE MAXIMUM RATINGS

VCC . . . . . +72V
EAINV . . . . . –0.3V to +10V
EAOUT . . . . . –0.3V to +10V
SS . . . . . –0.3V to +10V
DIODE . . . . . –0.3V to VCC
VGG . . . . . –0.3V to VCC +14V
CS . . . . . VCC – 5V to VCC +0.6V
I_{OUT} Pulsed . . . . . –0.8A to +0.6A
SRC . . . . . –0.6V to VCC
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N or DP Packages



Note: The four GND pins are internally connected.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified VCC = 14V, VGG = 14V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency	VCC = 14V to 72V, EAINV = 1.9V, T_J = 25°C	100	110	120	kHz
	VCC = 11V to 14V, Over Temperature	90		120	kHz
Error Amplifier Section					
EAINV	EAOUT = EAINV	1.97	2	2.03	V
I_{EAINV}	EAOUT = EAINV		100	300	nA
EAVOL	EAOUT/EAINV, 25°C	70	80		dB
EAOUT High	EAINV ≤ 1.9V, I_{EAOUT} = –100µA	5.5	6.2		V
EAOUT Low	EAINV ≥ 2.1V, I_{EAOUT} = 100µA		0.8	1.1	V
Unity Gain Bandwidth	T_J = 25°C, F = 100kHz	0.85	1		MHz
PSRR, EAOUT	EAOUT = EAINV, VCC = 14V	80	90		dB
Current Sense Comparator Section					
Threshold (Referred to VCC)		0.4	0.5	0.6	V
Input Bias Current	CS = VCC – 0.4V		0.2	1	µA
Propagation Delay	$V_{OVERDRIVE}$ = 250mV		0.7	1.2	µs
Blanking Time	$V_{OVERDRIVE}$ = 250mV	75	200	300	ns
Gate Drive Output Section					
VOH	I_{OUT} = –200mA	9.5	11		V
VOL	I_{OUT} = 20mA		0.2	0.36	V
	I_{OUT} = 200mA		1.5	2	V
Rise Time	T_J = 25°C, C_{LOAD} = 1nF		40	70	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1nF		40	70	ns
Pulse Width Modulator Section					
Maximum Duty Cycle	EAINV ≤ 1.9V	85	90		%
Minimum Duty Cycle	EAINV ≥ 2.1V		0		%
Modulator Gain	EAOUT = 2.5V to 3.5V		30		%/V
Undervoltage Lockout Section					
Start Threshold	OUT – SRC, EAINV ≤ 1.9V, SRC = 0V	10	11	12	V
UVLO Hysteresis		1.5	2	2.5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified VCC = 14V, VGG = 14V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VGG Regulator Section					
VGG – SRC	VCC = 72V, SRC = 0V, I_{VGG} = –7mA	14.5	15.25	17	V
	VCC = 50V, SRC = 0V, I_{VGG} = –7mA	14	14.75	16	V
	VCC = 15V, SRC = 0V, I_{VGG} = –7mA	13	13.75	14.5	V
	VCC = 11V, SRC = 0V, I_{VGG} = –7mA	9.5	10	10.5	V
Soft Start Ramp Section					
Soft Start Ramp Current		–30	–45		µA
Supply Current Section					
I_{VCC}	EAINV ≥ 2.1V, SRC = 0V		10	14	mA
I_{VGG}	EAINV ≥ 2.1V, SRC = 0V		7	10.5	mA

PIN DESCRIPTIONS

CS: Peak current limit sense pin. Senses the current across a current sense resistor placed between VCC and the drain of the NMOS buck switch. OUT will be held low (NMOS buck switch off) if VCC – CS exceeds 0.5V.

DIODE: An external small signal diode (1N4148 typical) is connected here, anode to VCC and cathode to DIODE, to implement the VGG regulator function.

EAINV: Inverting input to error amplifier. V_{OUT} sense feedback is connected to this pin. The non-inverting input of the error amplifier is internally connected to 2V.

EAOUT: Output of the error amplifier. Use EAOUT and EAINV for loop compensation components.

GND: Circuit Ground. The four ground pins are internally connected together by the fused leadframe of the package. They provide the primary thermal conduction path for dissipating junction heat.

OUT: Gate drive for the external NMOS switch connected between VCC and the buck inductor.

SRC: This pin is connected to the junction of the external NMOS switch source, the floating voltage source capacitor, the free-wheeling diode cathode, and buck inductor.

SS: The external soft start capacitor is connected to this pin.

VGG: An external capacitor connected from VGG to SRC completes the floating voltage source for the floating gate driver. A 1µF capacitor is recommended.

VCC: Input supply voltage. This pin supplies an internal ground referenced voltage regulator that supplies the IC and an on-chip regulated floating voltage source (VGG – SRC) used by the floating driver to drive the external NMOS buck switch. This pin should be bypassed with a high quality ceramic capacitor.

APPLICATION INFORMATION

The UC3578 Floating Buck Controller is a high frequency switching regulator with a floating driver which provides PWM control for non-isolated buck converters. The controller operates at a fixed 100 kHz switching frequency, and in voltage mode control. The duty cycle range of the PWM output is 0% to 90% allowing for a wide range of input voltages (14V minimum with transients to 72V). The regulator features an undervoltage lockout threshold of 11V with approximately 2V hysterisis as well as soft start capability. The typical application circuit shown is for a 15V to 40V input and a 12V at 3A output.

To ensure proper operation of the floating driver, an external capacitor (1µF ceramic) must be connected from VGG to SRC, and to the source of the external MOSFET through a small resistor, as shown in the typical application diagram and in Fig 2. This capacitor provides the energy for the high side driver. The gate drive voltage to the MOSFET is internally regulated to 14V. A diode (1N4148) is required from the input voltage to DIODE. This allows the floating drive capacitor to charge during conduction of the output rectifier but prevents its discharge back into the supply rail. A 1µF ceramic capacitor is recommended from VCC to ground to provide high frequency decoupling. Additional decoupling of this pin could be accomplished by a low value resistor between VCC and V_{IN} and a 1µF capacitor from VCC to GND as shown in the schematic.

APPLICATION INFORMATION (cont.)

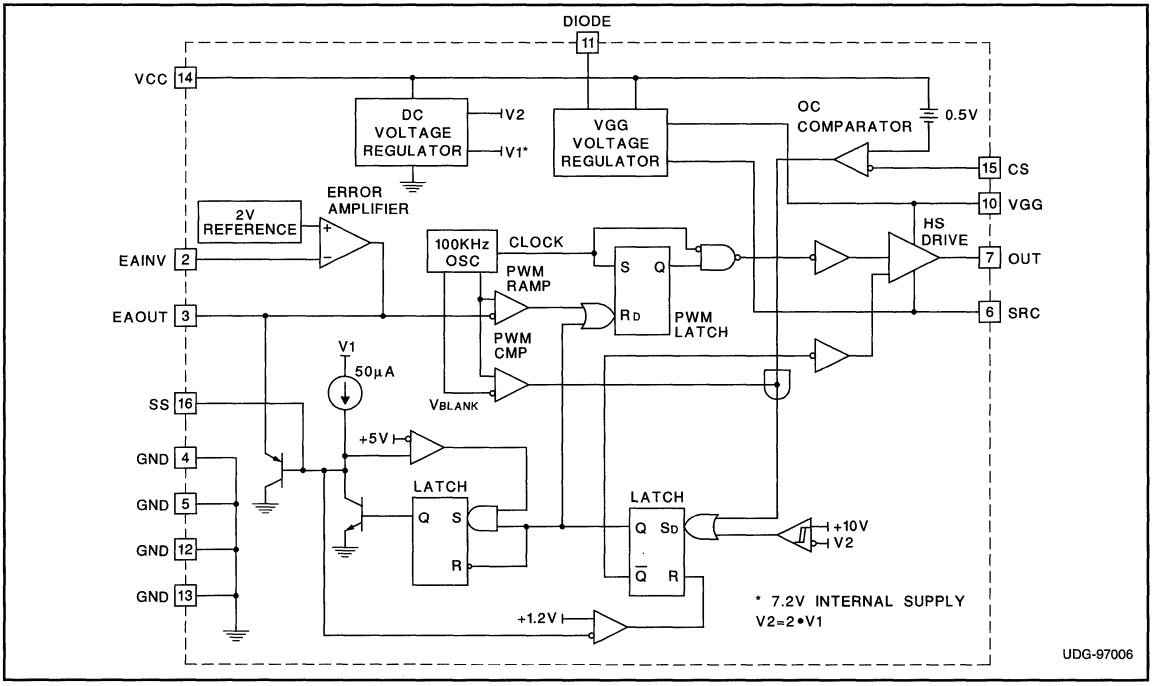


Figure 1. Block diagram.

Current Limit

The current sense pin provides overcurrent shutdown. As can be seen from the block diagram, the overcurrent comparator is wire ANDed with the oscillator after an internally set blanking time. The I_{LIMIT} threshold level is set by the current sense resistor from R_{SENSE}.

$$I_{LIMIT} = \frac{0.5V}{R_{SENSE}}$$

An optional filter can be added (R_SC_S) from the current sense resistor to CS to provide high frequency filtering of the current sense signal if necessary.

During a current limit condition, the soft start capacitor on SS is discharged until its voltage level reaches 1.2V. During this time, a duty cycle clamp is activated to approximately 0.6V above the voltage level on the SS capacitor. This condition persist until the SS capacitor is discharged to 1.2V, thus disabling the output driver. At this time, the SS capacitor is allowed to charge to 5V through the 50µA current source and normal operation resumes when the SS capacitor reaches 5V. During the condition described, the regulator enters a hiccup current limit mode of operation which limits the power dissipation in the MOSFET and output rectifier under a short circuit condition.

Error Amplifier

The onboard error amplifier of the UC3578 is a voltage amplifier with its non-inverting input tied to an internal 2V reference. As usual, loop compensation can be added from the inverting input of EAINV to the error amplifier output at EAOUT. Consideration must be given when choosing the values of the compensation components around the amplifier so that the output swing of the amplifier is not restricted. The output of the amplifier can source 100µA typically.

General

As in any buck converter, when the switch is off, the source flies low due to the conduction of the free-wheeling rectifier. The source (SRC) is pulled below ground by an amount determined by the forward voltage drop of the rectifier and by any transient voltage spike from inductance in this path. The occurrence of this condition could result in erratic operation of the IC during this period if the negative excursion is not limited. This is because of conduction of current in the substrate of the IC due to the source pin being pulled below ground and forward biasing the internal substrate PN junction. To limit this effect, a small resistor (15Ω) can be placed in series

APPLICATION INFORMATION (cont.)

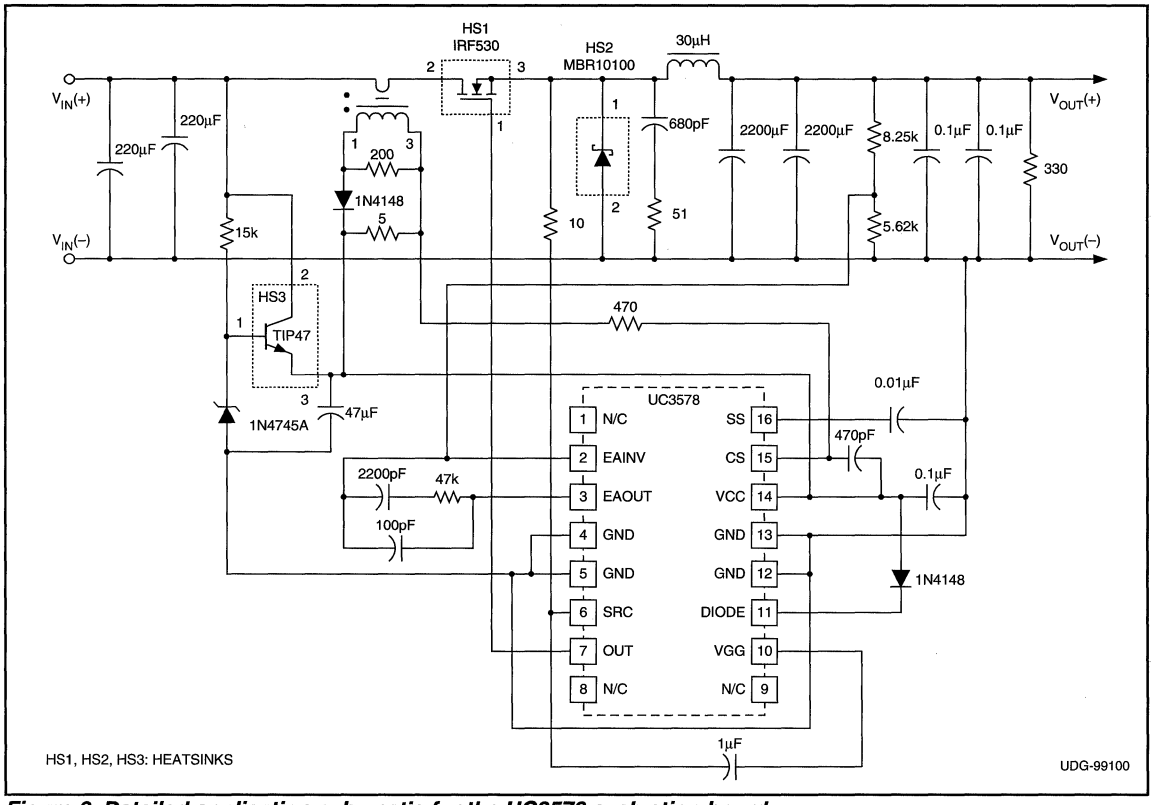


Figure 2. Detailed application schematic for the UC3578 evaluation board.

between the MOSFET source and the SRC pin as shown in Fig. 1. Too large a resistor will limit the drive to the MOSFET and result in startup problems with the regulator. A Schottky rectifier is used for the free-wheeling diode to limit the negative excursion of the source. This will also limit the reverse recovery current thus limiting the inductive voltage spike.

In applications where transient load excursions may result in a no load condition, it is necessary that the output of the regulator be loaded with a small load current (10mA to 15mA). This will prevent the output voltage from going unregulated at no load. This small load current is necessary for proper operation of the floating driver since the source must fly low to charge up the floating driver capacitance.

Thermal Considerations

For proper operation and reliability of the UC3578, proper thermal management is essential. It is important that the designer keep in mind that with surface mount packages, a significant amount of the heat that the device generates is conducted out through the lead frame. Because of this, the PCB design becomes a critical part of the thermal management system. Worst case junction-to-ambient thermal resistance for different package configurations are given in a table in the data book in the package information section.

The maximum ambient operating temperature is an important factor in determining what the maximum operating voltage can be for a particular application. For example, if we assume a maximum operating ambient temperature of 70°C we can determine what the maximum allowable input voltage can be given other parameters such as package thermal impedance and MOSFET total gate charge by following the procedure outlined below;

$$T_{J(max)} - T_A = 125°C - 70°C = 55°C. \quad (1)$$

$$Pd = \frac{55°C}{58°C/W} = 0.95W, \quad (2)$$

APPLICATION INFORMATION (cont.)

where 58°C/W is the worst case theta j-a for the 16 pin DP package and Pd is the package power dissipation.

$$Pd = (Qg \bullet 100kHz + 19mA) \bullet V_{IN}, \quad (3)$$

where Qg is the total MOSFET gate charge and 19mA is the maximum quiescent current for the UC3578 (I_{CC} + I_{GG}) from the data sheet. The switching frequency of the buck converter is 100kHz.

The gate charge can be determined from the MOSFET data sheet. As an example, for a IRFZ34 which has a total gate charge of 46nC, substituting for Pd in equation 3:

$$0.95W = (46nC \bullet 100kHz + 19mA) \bullet V_{IN}, \text{ and}$$

$$V_{IN(max)} = \frac{0.95W}{0.0236A} = 40V.$$

Therefore, at 70°C using a IRFZ34 MOSFET the maximum input voltage is limited to 40V to maintain a maximum junction temperature of 125°C in the 16 pin DP package.

Higher input voltages can be achieved by choosing a MOSFET with a lower total gate charge or by a reduced ambient operating temperature or by reducing the theta j-a of the package by improving the PCB mounting method. It is recommended that the four GND pins (4, 5, 12 and 13) be connected to a ground plane to provide a low resistance thermal path. If a ground plane is not available, a heat spreader on a double sided PC board is recommended.

Note: Thermal impedance number is based on device mounted to 5 square inch FR4 PC board with one ounce copper. From Unitrode 95-96 data book Table 1, page 9-8, when resistance range is given, lower thermal impedance values are for 5 square inch aluminum PC board.

ADDITIONAL INFORMATION

Please refer to the following Unitrode topic for additional application information.

[1] Application Note U-167, *Design and Evaluation of a 48V to 5V Telecom Buck Converter using the UC3578 Control IC* by Mark Dennis.

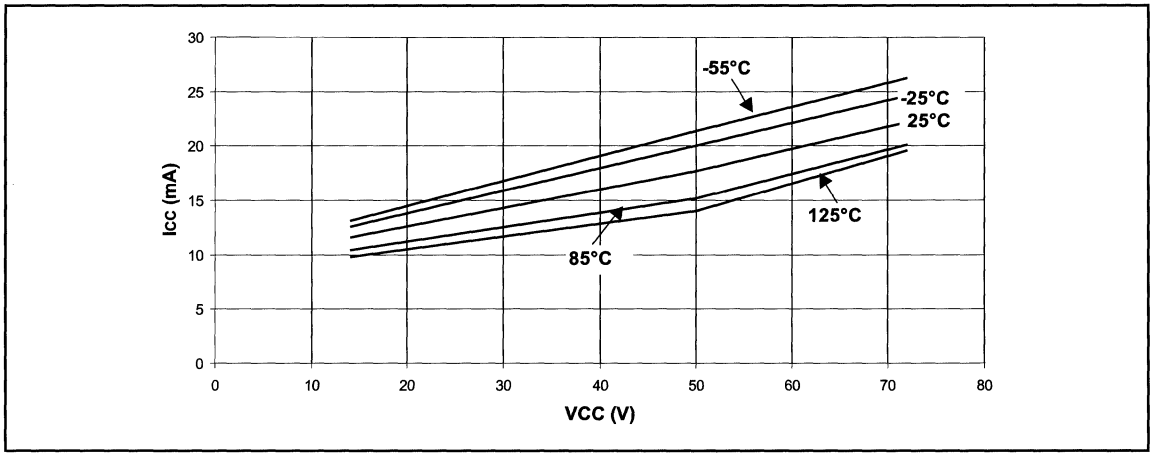


Figure 3. I_{CC} vs. VCC vs. temperature.

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Single Ended Active Clamp/Reset PWM

FEATURES

- Provides Auxiliary Switch Activation Complementary to Main Power Switch Drive
- Programmable deadtime (Turn-on Delay) Between Activation of Each Switch
- Voltage Mode Control with Feedforward Operation
- Programmable Limits for Both Transformer Volt- Second Product and PWM Duty Cycle
- High Current Gate Driver for Both Main and Auxiliary Outputs
- Multiple Protection Features with Latched Shutdown and Soft Restart
- Low Supply Current (100µA Startup, 1.5mA Operation)

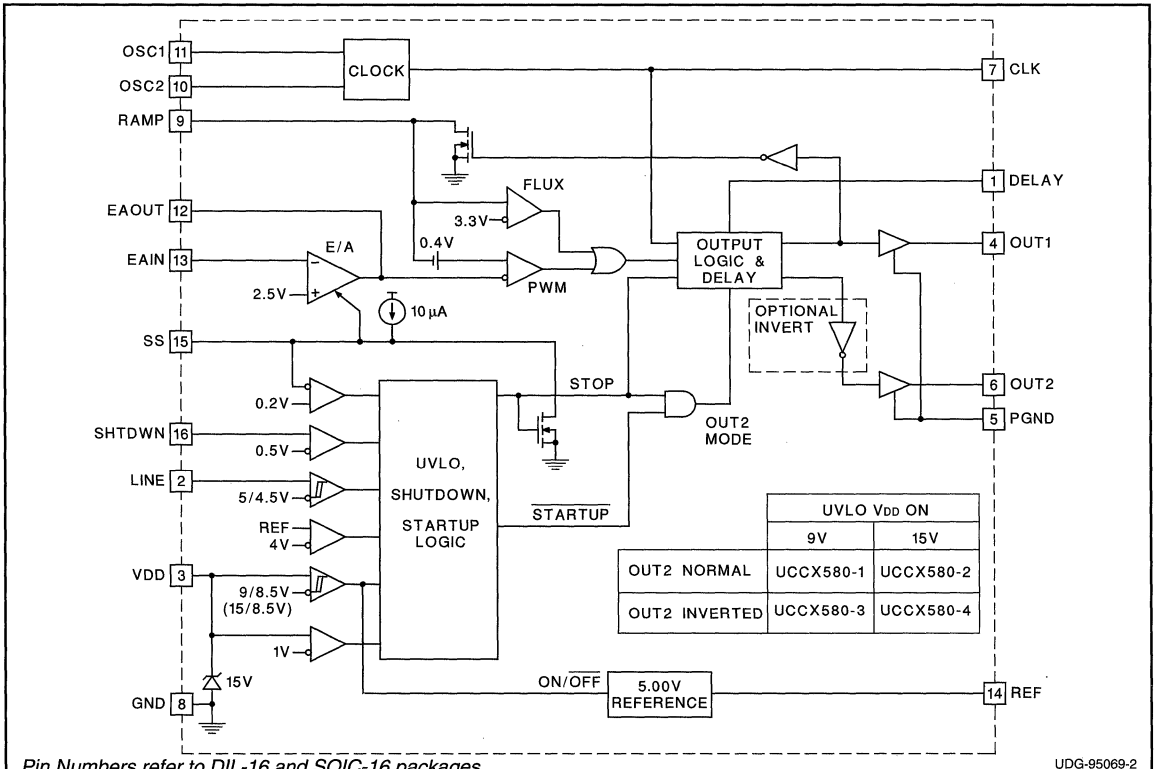
DESCRIPTION

The UCC3580 family of PWM controllers is designed to implement a variety of active clamp/reset and synchronous rectifier switching converter topologies. While containing all the necessary functions for fixed frequency, high performance pulse width modulation, the additional feature of this design is the inclusion of an auxiliary switch driver which complements the main power switch, and with a programmable deadtime or delay between each transition. The active clamp/reset technique allows operation of single ended converters beyond 50% duty cycle while reducing voltage stresses on the switches, and allows a greater flux swing for the power transformer. This approach also allows a reduction in switching losses by recovering energy stored in parasitic elements such as leakage inductance and switch capacitance.

The oscillator is programmed with two resistors and a capacitor to set switching frequency and maximum duty cycle. A separate synchronized ramp provides a voltage feedforward pulse width modulation and a programmed maximum volt-second limit. The generated clock from the oscillator contains both frequency and maximum duty cycle information.

(continued)

BLOCK DIAGRAM



Pin Numbers refer to DIL-16 and SOIC-16 packages

UDG-95069-2

DESCRIPTION (cont.)

The main gate drive output (OUT1) is controlled by the pulse width modulator. The second output (OUT2) is intended to activate an auxiliary switch during the off time of the main switch, except that between each transition there is deadtime where both switches are off, programmed by a single external resistor. This design offers two options for OUT2, normal and inverted. In the -1 and -2 versions, OUT2 is normal and can be used to drive PMOS FETs. In the -3 and -4 versions, OUT2 is inverted and can be used to drive NMOS FETs. In all versions, both the main and auxiliary switches are held off prior to startup and when the PWM command goes to zero duty cycle. During fault conditions, OUT1 is held off while OUT2 operates at maximum duty cycle with a guaranteed off time equal to the sum of the two deadtimes.

Undervoltage lockout monitors supply voltage (VDD), the precision reference (REF), input line voltage (LINE), and the shutdown comparator (SHTDWN). If after any of these four have sensed a fault condition, recovery to full operation is initiated with a soft start. VDD thresholds, on and off, are 15V and 8.5V for the -2 and -4 versions, 9V and 8.5V for the -1 and -3 versions.

The UCC1580-x is specified for operation over the military temperature range of –55°C to 125°C. The UCC2580-x is specified from –40°C to 85°C. The UCC3580-x is specified from 0°C to 70°C. Package options include 16-pin surface mount or dual in-line, and 20-pin plastic leadless chip carrier.

ABSOLUTE MAXIMUM RATINGS

VDD 16V
I_{VDD} 25mA
LINE, RAMP . . . . . –0.3V to VDD + 1V
I_{LINE}, I_{RAMP} 5mA
DELAY 5.3V
I_{DELAY} . . . . . –5mA
I_{OUT1} (tpw < 1µs and Duty Cycle < 10%) . . . . . –0.6A to 1.2A
I_{OUT2} (tpw < 1µs and Duty Cycle < 10%) . . . . . –0.4A to 0.4A
I_{CLK} . . . . . –100mA to 100mA
OSC1, OSC2, SS, SHTDWN, EAIN . . . . . –0.3V to REF + 0.3V
I_{EAOUT} . . . . . –5mA to 5mA
I_{REF} . . . . . –30mA
PGND . . . . . –0.2V to 0.2V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

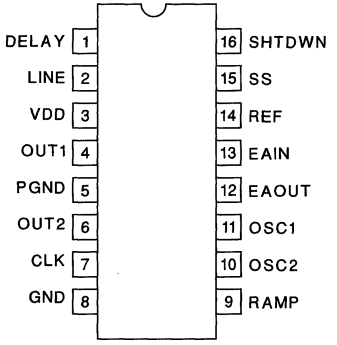
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ORDER INFORMATION

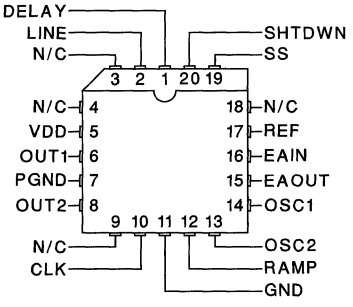
UCC☐580☐-☐
- ☐ — UVLO On Threshold/OUT2 Options
- ☐ — Package
- ☐ — Temperature Range

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



PLCC-20 (Top View)
Q Packages



ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2k, R2 = 4.41k, C_T = 100pF, R3 = 100k, C_{OUT1} = 0, C_{OUT2} = 0. T_A = 0°C to 70°C for the UCC3580, –40°C to 85°C for the UCC2580, –55°C to 125°C for the UCC1580, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Frequency		370	400	430	kHz
CLK Pulse Width		650	750	850	ns
CLK V_{OH}	I_{CLK} = –3mA	4.3	4.7		V
CLK V_{OL}	I_{CLK} = 3mA		0.3	0.5	V
Ramp Generator Section					
Ramp V_{OL}	I_{RAMP} = 100µA		50	100	mV
Flux Comparator Vth		3.16	3.33	3.50	V
Pulse Width Modulator Section					
Minimum Duty Cycle	OUT1, EAOUT = VOL			0	%
Maximum Duty Cycle	OUT1, EAIN = 2.6V	63	66	69	%
PWM Comparator Offset		0.1	0.4	0.9	V
Error Amplifier Section					
EAIN	EAOUT = EAIN	2.44	2.5	2.56	V
I_{EAIN}	EAOUT = EAIN		150	400	nA
EAOUT, VOL	EAIN = 2.6V, I_{EAOUT} = 100µA		0.3	0.5	V
EAOUT, VOH	EAIN = 2.4V, I_{EAOUT} = –100µA	4	5	5.5	V
AVOL		70	80		dB
Gain Bandwidth Product	f = 100kHz (Note 1)	2	6		MHz
Softstart/Shutdown Section					
Start Duty Cycle	EAIN = 2.4V		0		%
SS V_{OL}	I_{SS} = 100µA		100	350	mV
SS Restart Threshold			400	550	mV
I_{SS}			–20	–35	µA
SHTDWN V_{TH}		0.4	0.5	0.6	V
I_{SHTDWN}			50	150	nA
Undervoltage Lockout Section					
VDD On	UCC3580-2,-4	14	15	16	V
	UCC3580-1,-3	8	9	10	V
VDD Off		7.5	8.5	9.5	V
LINE On		4.7	5	5.3	V
LINE Off		4.2	4.5	4.8	V
I_{LINE}	LINE = 6V		50	150	nA
Supply Section					
VDD Clamp	I_{VDD} = 10mA	14	15	16	V
I_{VDD} Start	VDD < VDD On		160	250	µA
I_{VDD} Operating	No Load		2.5	3.5	mA
Output Drivers Section					
OUT1 V_{SAT} High	I_{OUT1} = –50mA		0.4	1.0	V
OUT1 V_{SAT} Low	I_{OUT1} =100mA		0.4	1.0	V
OUT2 V_{SAT} High	I_{OUT2} = –30mA		0.4	1.0	V
OUT2 V_{SAT} Low	I_{OUT2} = 30mA		0.4	1.0	V
OUT1 Fall Time	C_{OUT1} = 1nF, Rs = 3Ω		20	50	ns
OUT1 Rise Time	C_{OUT1} = 1nF, Rs = 3Ω		40	80	ns
OUT2 Fall Time	C_{OUT2} = 300pF, Rs = 10Ω		20	50	ns

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications are over the full temperature range, VDD = 12V, R1 = 18.2k, R2 = 4.41k, C_T = 100pF, R3 = 100k, C_{OUT1} = 0, C_{OUT2} = 0. T_A = 0°C to 70°C for the UCC3580, –40°C to 85°C for the UCC2580, –55°C to 125°C for the UCC1580, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Drivers Section (cont.)					
OUT2 Rise Time	C_{OUT2} = 300pF, R_S = 10Ω		20	40	ns
Delay 1 OUT2 to OUT1	R3 = 100k, $C_{OUT1} = C_{OUT2}$ = 15pF	90	120	160	ns
	$T_A = T_J$ = 25°C	100	120	140	ns
Delay 2 OUT1 to OUT2	R3 = 100k, $C_{OUT1} = C_{OUT2}$ = 15pF	110	170	250	ns
	$T_A = T_J$ = 25°C	140	170	200	ns
Reference Section					
REF	I_{REF} = 0	4.875	5	5.125	V
Load Regulation	I_{REF} = 0mA to 1mA		1	20	mV
Line Regulation	VDD = 10V to 14V		1	20	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLK: Oscillator clock output pin from a low impedance CMOS driver. CLK is high during guaranteed off time. CLK can be used to synchronized up to five other UCC3580 PWMs.

DELAY: A resistor from DELAY to GND programs the nonoverlap delay between OUT1 and OUT2. The delay times, Delay1 and Delay2, are shown in Figure 1 and are as follows:

$$Delay1 = 1.1pF \bullet R3$$

Delay2 is designed to be larger than Delay1 by a ratio shown in Figure 2.

EAIN: Inverting input to the error amplifier. The noninverting input of the error amplifier is internally set to 2.5V. EAIN is used for feedback and loop compensation.

EAOUT: Output of the error amplifier and input to the PWM comparator. Loop compensation components connect from EAOUT to EAIN.

GND: Signal Ground.

LINE: Hysteretic comparator input. Thresholds are 5.0V and 4.5V. Used to sense input line voltage and turn off OUT1 when the line is low.

OSC1 & OSC2: Oscillator programming pins. A resistor connects each pin to a timing capacitor. The resistor connected to OSC1 sets maximum on time. The resistor connected to OSC2 controls guaranteed off time. The combined total sets frequency with the timing capacitor. Frequency and maximum duty cycle are approximately given by:

$$\text{Frequency} = \frac{1}{(R1 + 1.25 \bullet R2) \bullet CT}$$

$$\text{Maximum Duty Cycle} = \frac{R1}{R1 + 1.25 \bullet R2}$$

Maximum Duty Cycle for OUT1 will be slightly less due to Delay1 which is programmed by R3.

OUT1: Gate drive output for the main switch capable of sourcing up to 0.5A and sinking 1A.

OUT2: Gate drive output for the auxiliary switch with ± 0.3A drive current capability.

PGND: Ground connection for the gate drivers. Connect PGND to GND at a single point so that no high frequency components of the output switching currents are in the ground plane on the circuit board.

RAMP: A resistor (R4) from RAMP to the input voltage and a capacitor (CR) from RAMP to GND programs the feedforward ramp signal. RAMP is discharged to GND when CLK is high and allowed to charge when CLK is low. RAMP is the line feedforward sawtooth signal for the PWM comparator. Assuming the input voltage is much greater than 3.3V, the ramp is very linear. A flux comparator compares the ramp signal to 3.3V to limit the maximum allowable volt-second product:

$$\text{Volt-Second Product Clamp} = 3.3 \bullet R4 \bullet CR.$$

REF: Precision 5.0V reference pin. REF can supply up to 5mA to external circuits. REF is off until VDD exceeds 9V (–1 and –3 versions) or activates the 15V clamp (–2 and –4 versions) and turns off again when VDD droops below 8.5V. Bypass REF to GND with a 1µF capacitor.

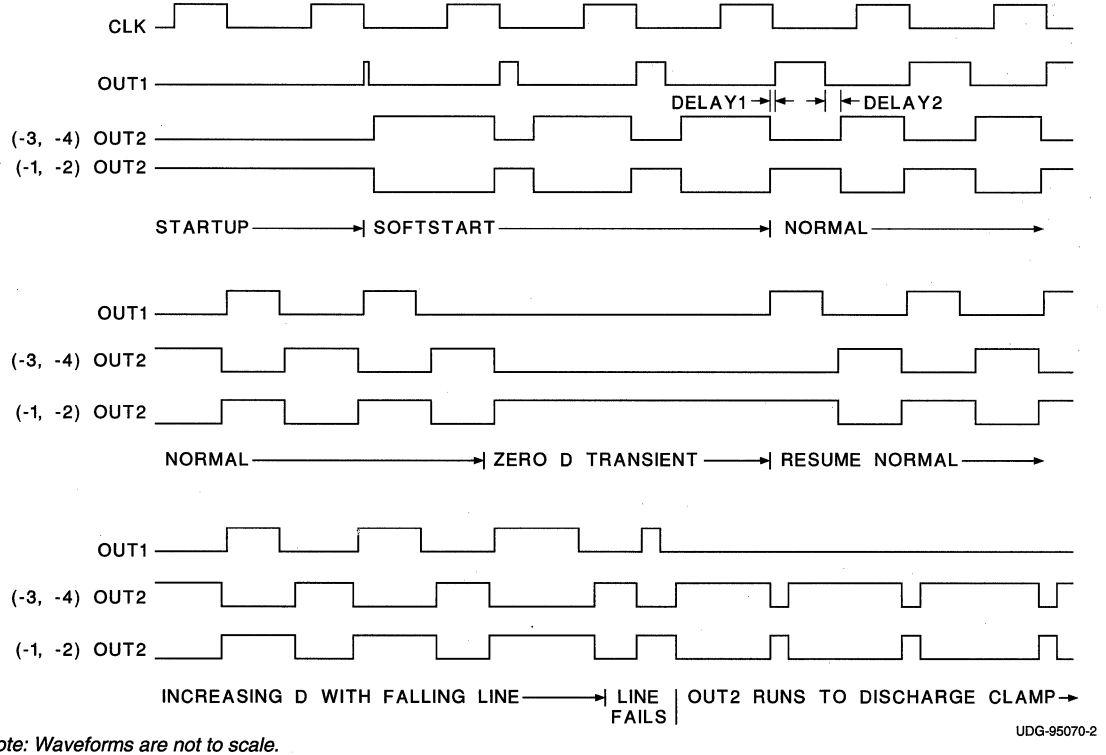
SHTDWN: Comparator input to stop the chip. The threshold is 0.5V. When the chip is stopped, OUT1 is low and OUT2 continues to oscillate with guaranteed off time equal to two non-overlap delay times.

PIN DESCRIPTIONS (cont.)

SS: A capacitor from SS to ground programs the soft start time. During soft start, EAOUT follows the amplitude of SS's slowly increasing waveform until regulation is achieved.

VDD: Chip power supply pin. VDD should be bypassed to PGND. The –1 and –3 versions require VDD to exceed 9V to start and remain above 8.5V to continue running. A shunt clamp from VDD to GND limits the supply voltage to 15V. The –2 and –4 versions do not start until the shunt clamp threshold is reached and operation continues as long as VDD is greater than 8.5V.

APPLICATION INFORMATION



Note: Waveforms are not to scale.

Figure 1. Output time relationships.

UVLO and Startup

For self biased off-line applications, -2 and -4 versions (UVLO on and off thresholds of 15V and 8.5V typical) are recommended. For all other applications, -1 and -3 versions provide the lower on threshold of 9V. The IC requires a low startup current of only 160µA when VDD is under the UVLO threshold, enabling use of a large trickle charge resistor (with corresponding low power dissipation) from the input voltage. VDD has an internal clamp at 15V which can sink up to 10mA. Measures should be taken not to exceed this current. For -2 and -4 versions, this clamp must be activated as an indication of reaching the UVLO on threshold. The internal reference (REF) is brought up when the UVLO on threshold is crossed. The startup logic ensures that LINE and REF are above and SHTDWN is below their respective thresholds before outputs are asserted. LINE input is useful for monitoring actual input voltage and shutting off the IC if it falls below a programmed value. A resistive divider should be used to connect the input voltage to the LINE input. This feature can protect the power supply from excessive currents at low line voltages.

APPLICATION INFORMATION (cont.)

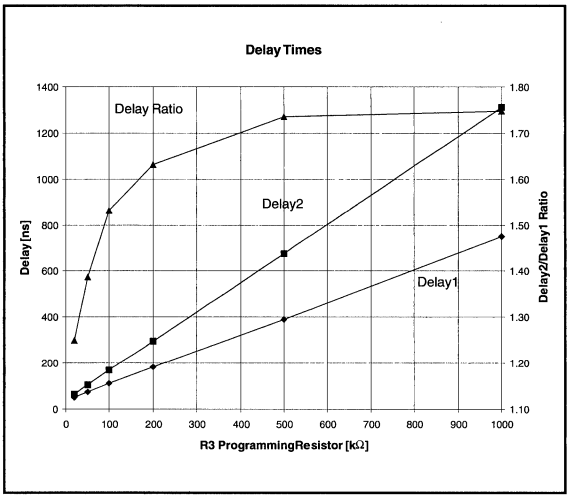


Figure 2. Delay times.

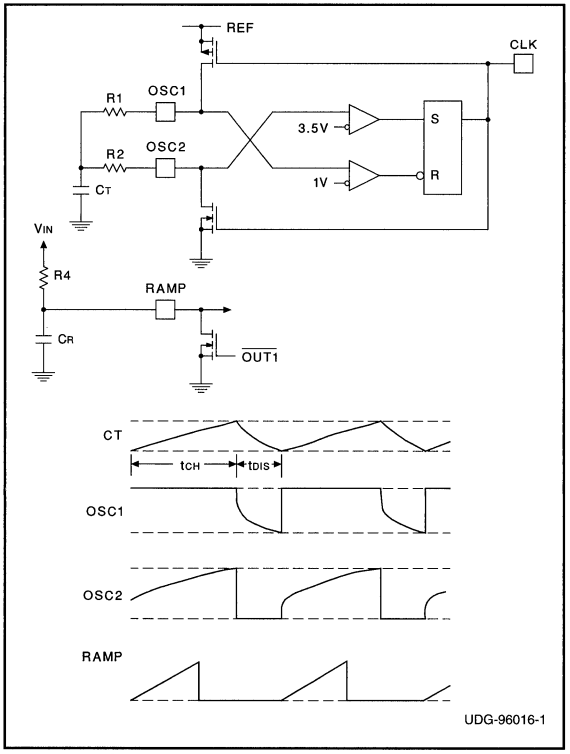


Figure 3. Oscillator and ramp circuits.

The soft start pin provides an effective means to start the IC in a controlled manner. An internal current of 20µA begins charging a capacitor connected to SS once the startup conditions listed above have been met. The voltage on SS effectively controls maximum duty cycle on OUT1 during the charging period. OUT2 is also controlled during this period (see Figure 1). Negation of any of the startup conditions causes SS to be immediately discharged. Internal circuitry ensures full discharge of SS (to 0.3V) before allowing charging to begin again, provided all the startup conditions are again met.

Oscillator

Simplified oscillator block diagram and waveforms are shown in Figure 3. OSC1 and OSC2 pins are used to program the frequency and maximum duty cycle. Capacitor CT is alternately charged through R1 and discharged through R2 between levels of 1V and 3.5V. The charging and discharging equations for CT are given by

$$VC(charge) = REF - 4.0 \bullet e^{-t/\tau_1}$$

$$VC(discharge) = 3.5 \bullet e^{-t/\tau_2}$$

where $\tau_1 = R1 \bullet CT$ and $\tau_2 = R2 \bullet CT$. The charge time and discharge time are given by

$$t_{CH} = R1 \bullet C_T \text{ and } t_{DIS} = 1.25 \bullet R2 \bullet C_T$$

The CLK output is high during the discharge period. It blanks the output to limit the maximum duty cycle of OUT1. The frequency and maximum duty cycle are given by

$$\text{Frequency} = \frac{1}{(R1 + 1.25 \bullet R2) \bullet CT}$$

$$\text{Maximum Duty Cycle} = \frac{R1}{R1 + 1.25 \bullet R2}$$

Maximum Duty Cycle for OUT1 will be slightly less due to Delay1 which is programmed by R3.

Voltage Feedforward and Volt-Second Clamp

UCC3580 has a provision for input voltage feedforward. As shown in Figure 3, the ramp slope is made proportional to input line voltage by converting it into a charging current for CR. This provides a first order cancellation of the effects of line voltage changes on converter performance. The maximum volt-second clamp is provided to protect against transient saturation of the transformer core. It terminates the OUT1 pulse when the RAMP voltage exceeds 3.3V. If the feedforward feature is not used, the ramp can be generated by tying R4 to REF. However, the linearity of ramp

APPLICATION INFORMATION (cont.)

suffers and in this case the maximum volt-second clamp is no longer available.

Output Configurations

The UCC3580 family of ICs is designed to provide control functions for single ended active clamp circuits. For different implementations of the active clamp approach, different drive waveforms for the two switches (main and auxiliary) are required. The -3 and -4 versions of the IC supply complementary non-overlapping waveforms (OUT1 and OUT2) with programmable delay which can be used to drive the main and auxiliary switches. Most active clamp configurations will require one of these outputs to be transformer coupled to drive a floating switch (e.g. Figure 5). The -1 and -2 versions have the phase of OUT2 inverted to give overlapping waveforms. This configuration is suitable for capacity coupled driving of a ground referenced p-channel auxiliary switch with the OUT2 drive while OUT1 is directly driving an n-channel main switch (e.g. Figure 4).

The programmable delay can be judiciously used to get zero voltage turn-on of both the main and auxiliary switches in the active clamp circuits. For the UCC3580, a single pin is used to program the delays between OUT1 and OUT2 on both sets of edges. Figure 1 shows the relationships between the outputs. Figure 2 gives the ratio between the two delays. During the transition from main to auxiliary switch, the delay is not very critical for ZVS turn-on. For the first half of OUT1 off-time, the body diode of the auxiliary switch conducts and OUT2 can be turned on any time. The transition from auxiliary to main switch is more critical. Energy stored in the parasitic inductance(s) at the end of the OUT2 pulse is used to discharge the parasitic capacitance across the main switch during the delay time. The delay (Delay 1) should be optimally programmed at 1/4 the resonant period determined by parasitic capacitance and the resonant inductor (transformer leakage and/or magnetizing inductances, depending on the topology). However, depending on other circuit parasitics, the resonant behavior can change, and in some cases, ZVS turn-on may not be ob-

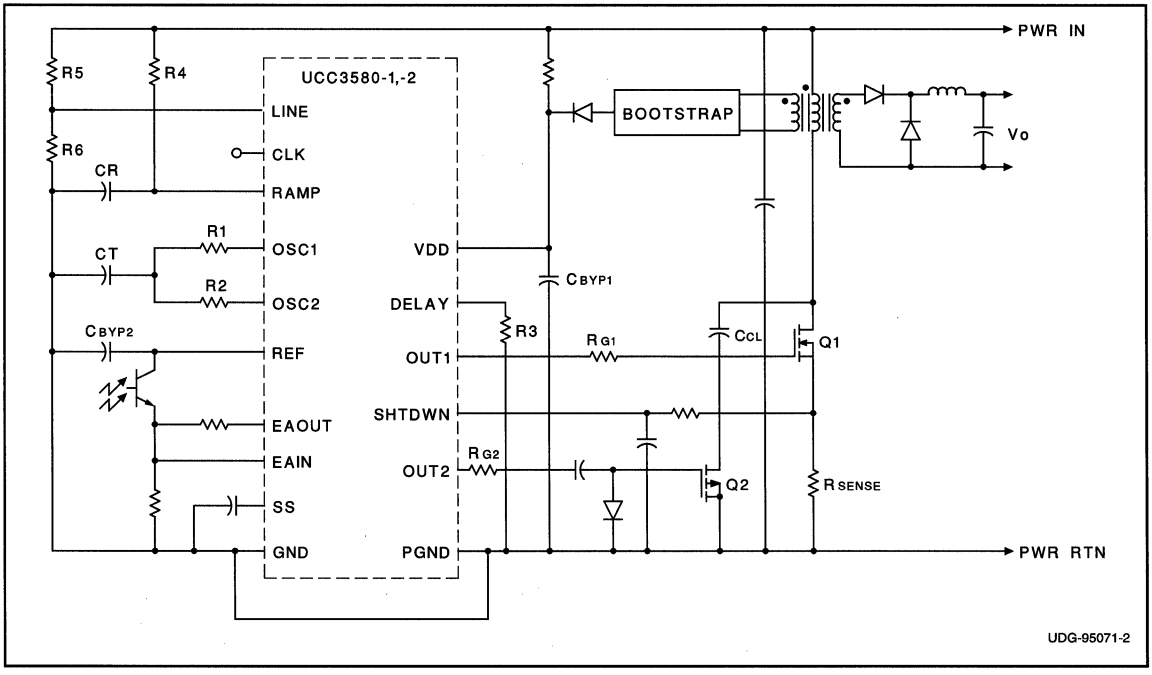


Figure 4. Active clamp forward converter.

Note that Vicor Corporation has claimed that the use of active reset in a forward converter topology is covered by their U.S. Patent No. 4,441,146. Unitrode is not suggesting or encouraging persons to infringe or use Vicor's patented technology absent a license from Vicor.

APPLICATION INFORMATION (cont.)

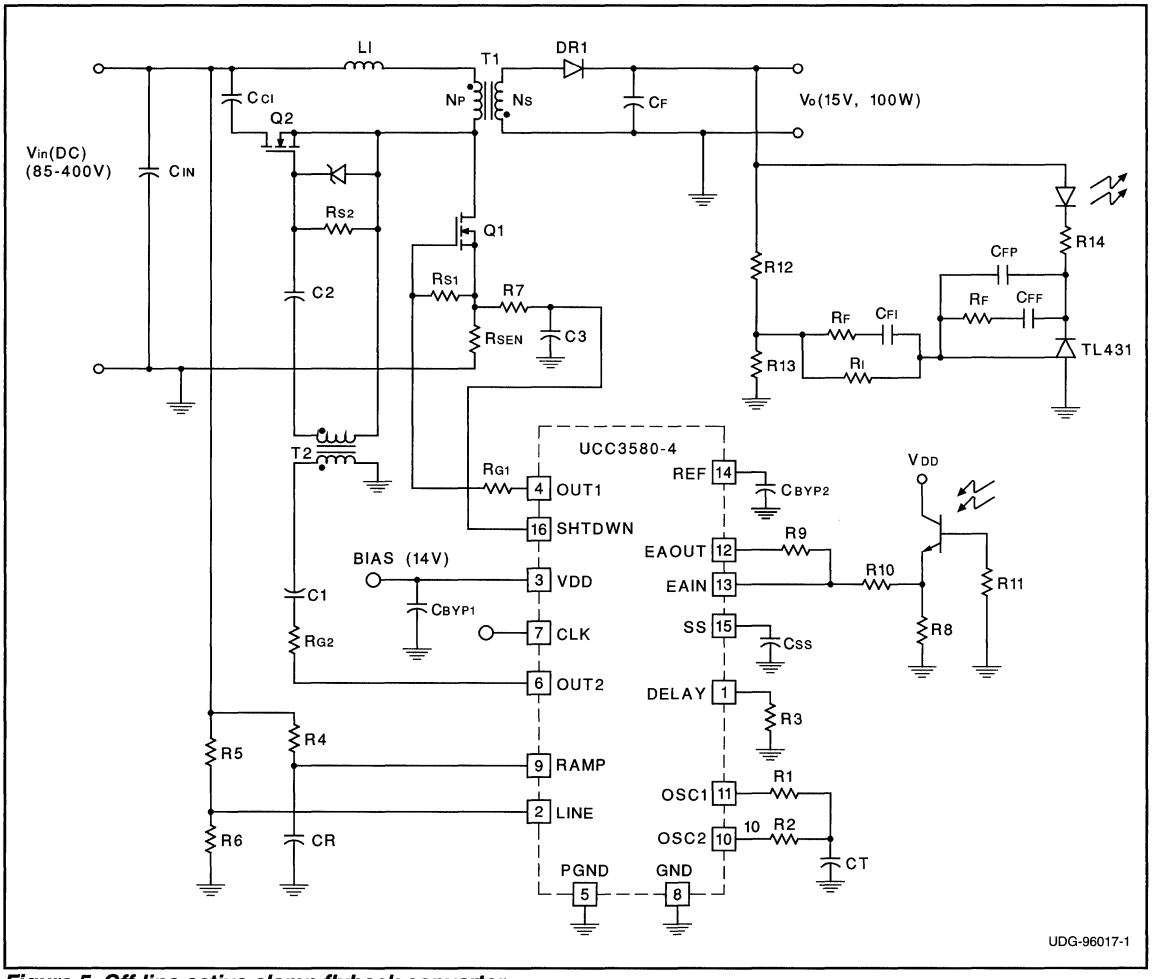


Figure 5. Off-line active clamp flyback converter.

The use of active reset in a flyback power converter topology may be covered by U.S. Patent No. 5,402,329 owned by Technical Witts, Inc., and for which Unitrode offers users a paid up license for application of the UCC1580 product family.

APPLICATION INFORMATION (cont.)

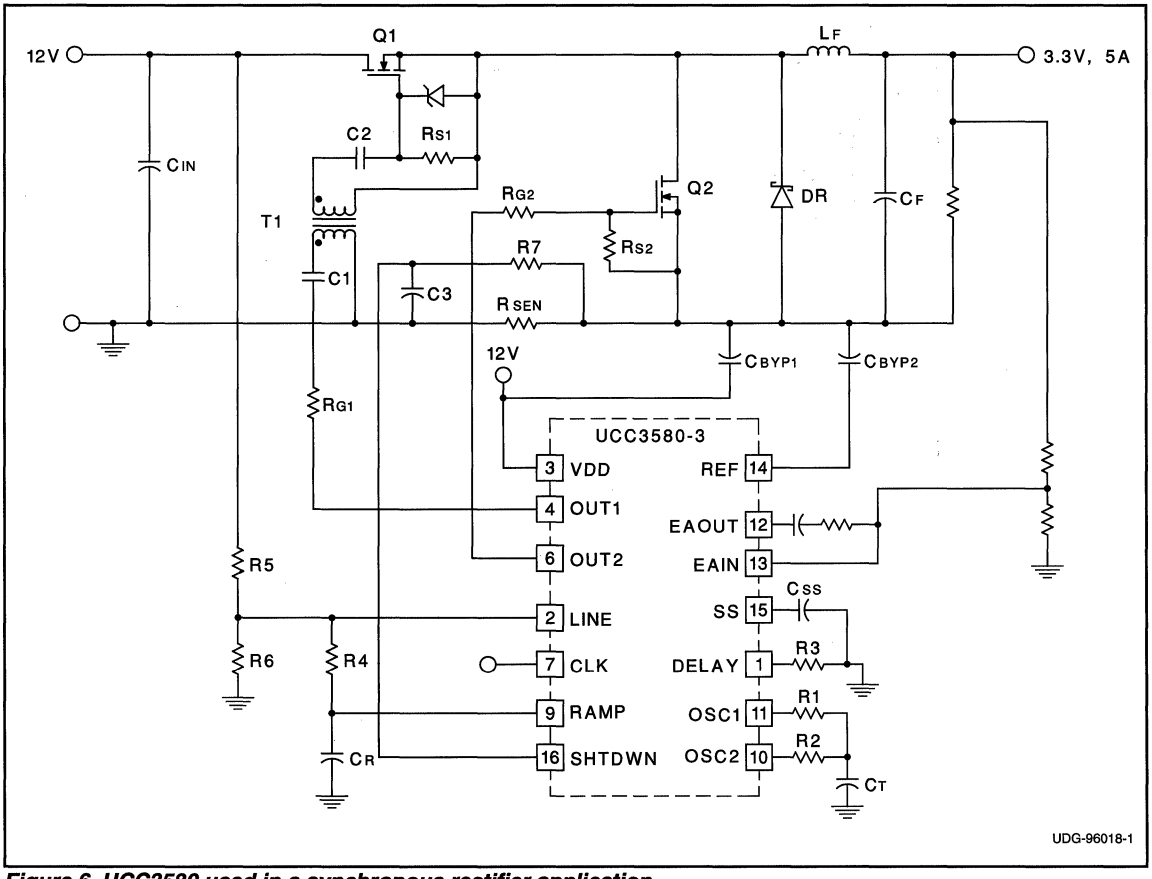


Figure 6. UCC3580 used in a synchronous rectifier application.

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UNITRODE

application INFO available

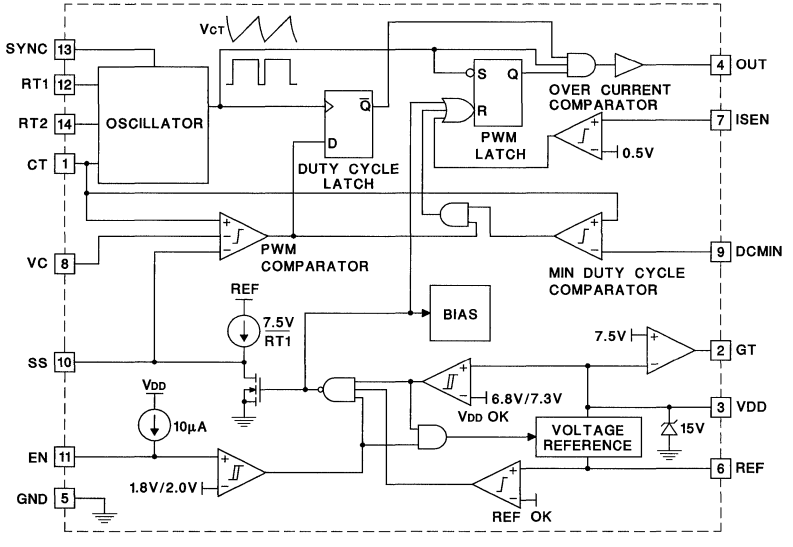
UCC1581
UCC2581
UCC3581

Micropower Voltage Mode PWM

FEATURES

- Low 85µA Startup Current
- Low 300µA Operating Current
- Automatically Disabled Startup Preregulator
- Programmable Minimum Duty Cycle with Cycle Skipping
- Programmable Maximum Duty Cycle
- Output Current 1A Peak Source and Sink
- Programmable Soft Start
- Programmable Oscillator Frequency
- External Oscillator Synchronization Capability

BLOCK DIAGRAM



Note: Pin Connection shown for 14-pin Package

UDG-95011-1

DESCRIPTION

The UCC3581 voltage mode pulse width modulator is designed to control low power isolated DC - DC converters in applications such as Subscriber Line Power (ISDN I.430). Primarily used for single switch forward and flyback converters, the UCC3581 features BiCMOS circuitry for low startup and operating current, while maintaining the ability to drive power MOSFETs at frequencies up to 100kHz. The UCC3581 oscillator allows the flexibility to program both the frequency and the maximum duty cycle with two resistors and a capacitor. A TTL level input is also provided to allow synchronization to an external frequency source.

The UCC3581 includes programmable soft start circuitry, overcurrent detection, a 7.5V linear preregulator to control chip V_{DD} during startup, and an on-board 4.0V logic supply.

The UCC3581 provides functions to maximize light load efficiency that are not normally found in PWM controllers.

A linear preregulator driver in conjunction with an external depletion mode N-MOSFET provides initial controller power. Once the bootstrap supply is functional, the preregulator is shut down to conserve power. During light load, power is saved by providing a programmable minimum duty cycle clamp. When a duty cycle below the minimum is called for, the modulator skips cycles to provide the correct average duty cycle required for output regulation. This effectively reduces the switching frequency, saving significant gate drive and power stage losses.

The UCC3581 is available in 14-pin plastic and ceramic dual-in-line packages and in a 14-pin narrow body small outline IC package (SOIC). The UCC1581 is specified for operation from –55°C to +125°C, the UCC2581 is specified for operation from –40°C to +85°C, and the UCC3581 is specified for operation from 0°C to +70°C.

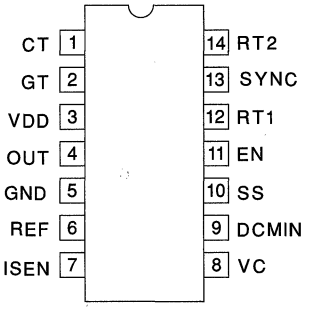
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($I_{DD} \leq 10mA$) 15V
Supply Current 30mA
V_{REF} Current . . . . . –10mA
OUT Current . . . . . ± 1A
Analog Inputs
EN . . . . . –0.3V to (VDD + 0.3V)
VC, ISEN, SYNC, DCMIN . . . . . –0.3V to (V_{REF} + 0.3V)
Power Dissipation at T_D = 25°C
(N, J, Q, L Package) 1W
(D Package) 0.65W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Unless otherwise specified, all voltages are with respect to Ground. Currents positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)
N or J, D Packages



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UCC1581J	–55°C to +125°C	CDIP
UCC2581D	–40°C to +85°C	SOIC
UCC2581N	–40°C to +85°C	PDIP
UCC3581D	0°C to +70°C	SOIC
UCC3581N	0°C to +70°C	PDIP

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VDD = 10V, 0.1µF capacitor from VDD to GND, 1.0µF capacitor from REF to GND, RT1 = 680kΩ, RT2 = 12kΩ, CT = 750pF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	I = –0.2mA	3.94	4.0	4.06	V
Load Regulation	–5.0mA < I < –0.2mA		10	30	mV
Undervoltage Lockout Section					
Start Threshold		6.7	7.3	7.9	V
Minimum Operating Voltage After Start		6.2	6.8	7.4	V
Hysteresis		0.2	0.5	0.8	V
Linear Preregulator Section					
Regulated VDD Voltage		7.0	7.5	8.0	V
Regulated VDD to UVLO Delta		100	230	600	mV
VDD Override Threshold				8.2	V
Oscillator Section					
Frequency	25°C	18	19.5	21	kHz
Temperature Stability	(Note 1)		3.0		%
CT Peak Voltage	(Note 1)		2.5		V
CT Valley Voltage	(Note 1)		1.0		V
SYNC VIH		1.9	2.1	2.3	V
SYNC VIL	(Note 1)		1.8		V
PWM SECTION					
Maximum Duty Cycle		80	83	86	%
Minimum Duty Cycle	(VC < 1.0V) DCMIN = 0V			0	%
	(VC > 1.0V at start of cycle) DCMIN = 1.18V	8	10.5	13	%
Input Bias Current	(DCMIN), (Note 1)	–150	20	150	nA
	(VC), (Note 1)	–150	20	150	nA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VDD = 10V, 0.1µF capacitor from VDD to GND, 1.0µF capacitor from REF to GND, RT1 = 680kΩ, RT2 = 12kΩ, CT = 750pF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
Input Bias Current		–150	20	150	nA
Overcurrent Threshold		0.4	0.5	0.6	V
Output Section					
OUT Low Level	I = 100mA		0.6	1.2	V
OUT High Level	I = –100mA, VDD – OUT		0.6	1.2	V
Rise/Fall Time	(Note 1)		20	100	ns
Soft start Section					
Soft start Current	SS = 2V	–9	–11.5	–14	µA
Chip Enable Section					
VIH		1.9	2.0	2.1	V
VIL		1.7	1.8	1.9	V
Hysteresis		180	230	280	mV
Source Current		5	10	15	µA
Overall Section					
Start-Up Current	VDD < Start Threshold		85	130	µA
Operating Supply Current	VC = 0V		300	600	µA
VDD Zener Shunt Voltage	I_{DD} = 10mA	13.5	15	16.5	V
I_{DD} Stand-by Shunt Voltage	EN = 0V		100	150	µA

Note 1: Guaranteed by design. Not 100% tested in production

PIN DESCRIPTIONS

CT: Oscillator timing capacitor pin. Minimum value is 100pF.

DCMIN: Input for programming minimum duty cycle where pulse skipping begins. This pin can be grounded to disable minimum duty cycle feature and pulse skipping.

EN: Enable input. This pin has an internal 10µA pull-up. A logic low input inhibits the PWM output and causes the soft start capacitor to be discharged.

GND: Circuit ground.

GT: Pin for controlling the gate of an external depletion mode N-MOSFET for the startup supply. The external N-MOSFET regulates VDD to 7.5V until the bootstrap supply comes up, then GT goes low.

ISEN: Input for overcurrent comparator. This function can be used for pulse-by-pulse current limiting. The threshold is 0.5V nominal.

OUT: Gate drive output to external N-MOSFET.

REF: 4.0V reference output. A minimum value bypass capacitor of 1.0µF is required for stability.

RT1: Resistor pin to program oscillator charging current. The oscillator charging current is $9.2 \bullet \left(\frac{2.0V}{RT1}\right)$.

See Application Diagram Fig. 1.

The current into this pin is $\left(\frac{2.0V}{RT1}\right)$.

The value of RT1 should be between 220k and 1MΩ.

RT2: Resistor pin to program oscillator discharge time. The minimum value of RT2 is 10kΩ. See Application Diagram Fig. 1.

SS: Soft start capacitor pin. The charging current out of SS is 3.75X the current in RT1.

SYNC: Oscillator synchronization pin. Rising edge triggered CMOS/TTL compatible input with a 2.1V threshold. SYNC should be grounded if not used. The minimum pulse width of the SYNC signal is 100ns.

VC: Control voltage input to PWM comparator. The nominal control range of VC is 1.0V to 2.5V.

VDD: Chip input power with an 15V internal clamp. VDD is regulated by startup FET to 7.5V until the bootstrap voltage comes up. VDD should be bypassed at the chip with a 0.1µF minimum capacitor.

APPLICATION INFORMATION

The UCC3581's oscillator allows the user the flexibility to program the frequency and the duty cycle by adjusting two resistors and a capacitor. Application Diagram Fig. 1 shows these components as RT1, RT2, and CT. RT1 programs the timing capacitor charging current which results in a linear ramp charging CT. Discharge of CT is accomplished though RT2 which results in a standard RC discharge waveform. The oscillator on-time (CT charging) is calculated by the formula

$$t_{ON} = 0.082 \bullet RT1 \bullet C_T.$$

The off-time (CT discharging) is calculated by the formula

$$t_{OFF} = 0.95 \bullet RT1 \bullet C_T.$$

Resistor RT1 programs the charging current. The current is

$$\frac{2.0V}{RT1}.$$

CT charging current is 9.2 times the current in RT1. RT1 can range from 220kΩ to 1MΩ. Minimum capacitor size is 100pF, and minimum RT2 size is 10k.

A Block Diagram of the Oscillator is shown in Fig. 2. The oscillator also has an external synchronization pin. When a low to high level is detected, and if the oscillator's output is in the high state (CT charging), the oscillator output immediately goes low and CT starts discharging. The sync input is rising edge sensitive and is ignored when the oscillator output is low.

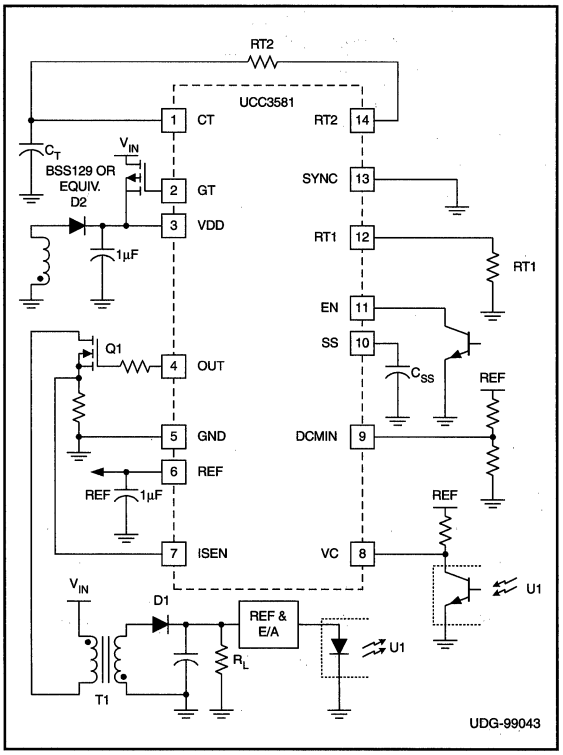


Figure 1. Application diagram.

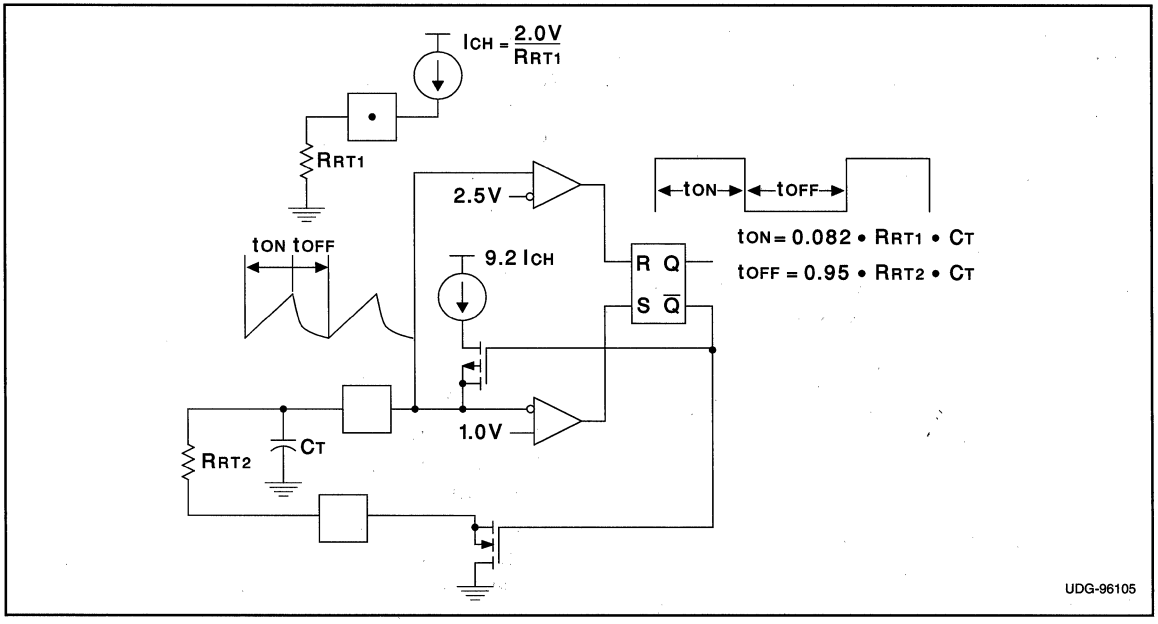


Figure 2. Oscillator.

APPLICATION INFORMATION (cont.)

The externally bypassed 4.0V reference is controlled by undervoltage lockout and chip enable circuitry. The enable input is internally tied to a 10μA current source which allows the pin to be driven by an open collector driver. The part is also enabled if EN floats. The UCC3581 has a soft start function which requires a user supplied external timing capacitor. When in soft start mode, the soft start capacitor, Css, is charged with a constant current source. The soft start current is 3.75X the current in RT1.

There is an on-chip control amplifier, which when driving the gate of an external depletion mode N-MOSFET, acts as a 7.5V linear preregulator supplying VDD directly from the primary input power line. The preregulator may subsequently be fully disabled by a tertiary bootstrap winding providing a minimum of 8.2V to the VDD pin.

Computation of DCMIN

DCMIN for a given duty cycle is calculated as follows.

$$\Delta V = i_{OSC} \bullet DC \bullet \frac{(t_{ON} + t_{OFF})}{C_T}$$

where

- i = oscillator charge current = 9.2 . (2.0V/RT1)
- DC = Duty Cycle, as a fraction of 1
- t_{ON} = 0.082 • RT1 • CT
- t_{OFF} = 0.95 • RT2 • CT
- C_T = Oscillator Capacitor

The CT pin ramp slews from 1V to 2.5V. Therefore, add ΔV to 1V to get DCMIN voltage.

Example: For 10% duty cycle with RT1 = 680kΩ, RT2 = 12kΩ, and CT = 705pF,

$$\Delta V = i_{OSC} \bullet DC \bullet \frac{(t_{ON} + t_{OFF})}{C_T}$$

$$= \frac{9.2 \bullet \left(\frac{2.0V}{680k}\right) \bullet (0.1) \bullet 4.182 \bullet 10^{-5}\ \text{sec} + 8.55 \bullet 10^{-6}\ \text{sec}}{750 \bullet 10^{-12}}$$

$$\Delta V = 0.18V$$

Therefore,

$$DCMIN = 1V + 0.18V = 1.18V$$

A Typical Micropower Application

The circuit shown in Fig. 3 illustrates the use of the UCC3581 in a micropower application. The isolated 5V flyback power supply uses a minimum of parts and operates over an 8:1 input voltage range (15VDC to 120VDC) while delivering a regulated 5V output with a load swing from 0W to 1W. It operates in the discontinuous mode at light load or high line, and continuous mode at heavier loads and lower line voltages. Higher input line voltages are possible by simply increasing the voltage ratings of C1, Q1, D1 and D2.

The most notable feature of the design is its efficiency. With a load of 1 watt, the typical efficiency is 82%, dropping to 70% around 50mW. With a load of only 12.5mW, the efficiency remains as high as 50%. At this load, with an input of 50V, the total input current is only 500μA. Note that the power supply can be disabled by pulling the UCC3581 enable pin low, in which case the input current drops to less than 150μA.

The UCC3581 achieves very low losses by means of low quiescent current and pulse skipping at light loads which reduces switching losses. The degree of pulse skipping is controlled by programming the minimum duty cycle. In this example, the frequency is 35kHz at maximum load and drops to <2kHz at 12.5mW load (minimum pulse width of around 6μsec, or 21% duty cycle at 35kHz). Another way losses are reduced is operating with a VDD of around 10V rather than the more common 12V to 16V. At such light primary currents, the MOSFET remains in full saturation with a gate drive voltage well below 10V.

Gate drive losses are minimized by choosing a MOSFET with low total gate charge, in this case only 8nC maximum. By choosing a large gate drive resistor, EMI is minimized by reducing peak currents. Due to pulse skipping, switching times are less critical for efficiency at light load.

The shunt regulator (LM3411) and optocoupler (MOC8100) are also key to the efficiency at such light loads, and were chosen for their low operating current. The LM3411 has a quiescent current of only 150μA maximum (compared to 1mA for the more common TL431). In addition, because it is not a three terminal device, the LM3411's quiescent current does not flow in the optocoupler LED. Since this bias current is not in the feedback control path, a higher value pull-up resistor can be used on the optocoupler output transistor, further reducing losses.

TYPICAL APPLICATION

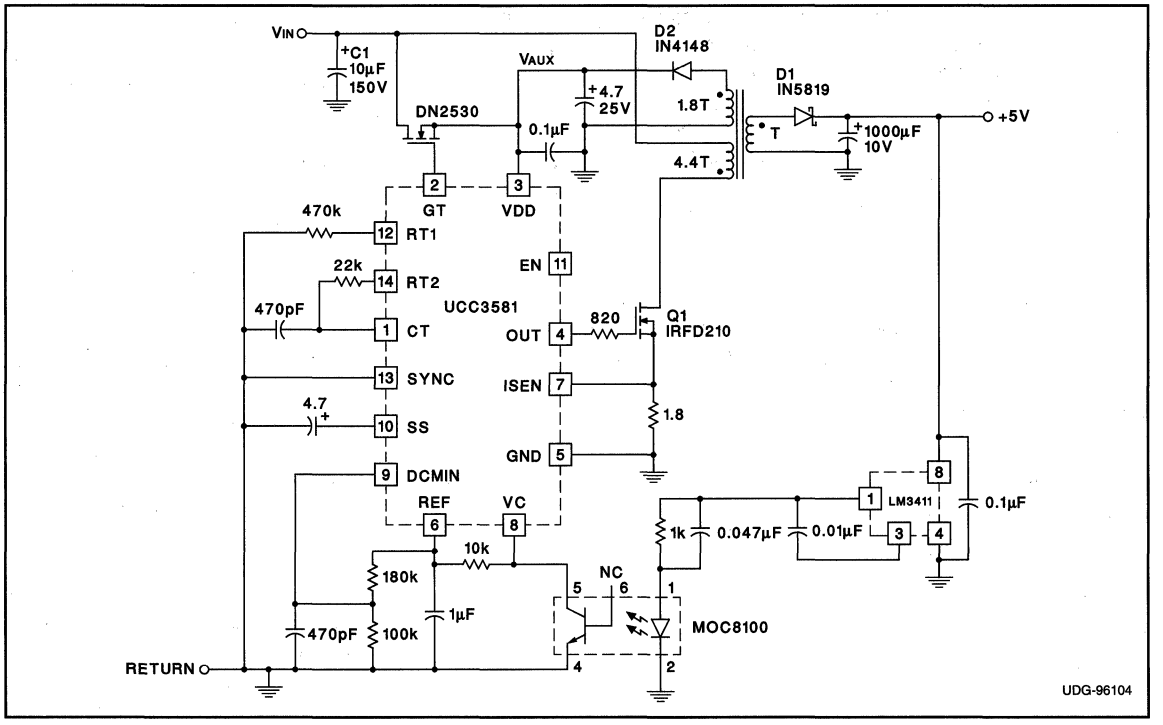


Figure 3. Micropower power supply with 50% efficiency at 12.5mW load.

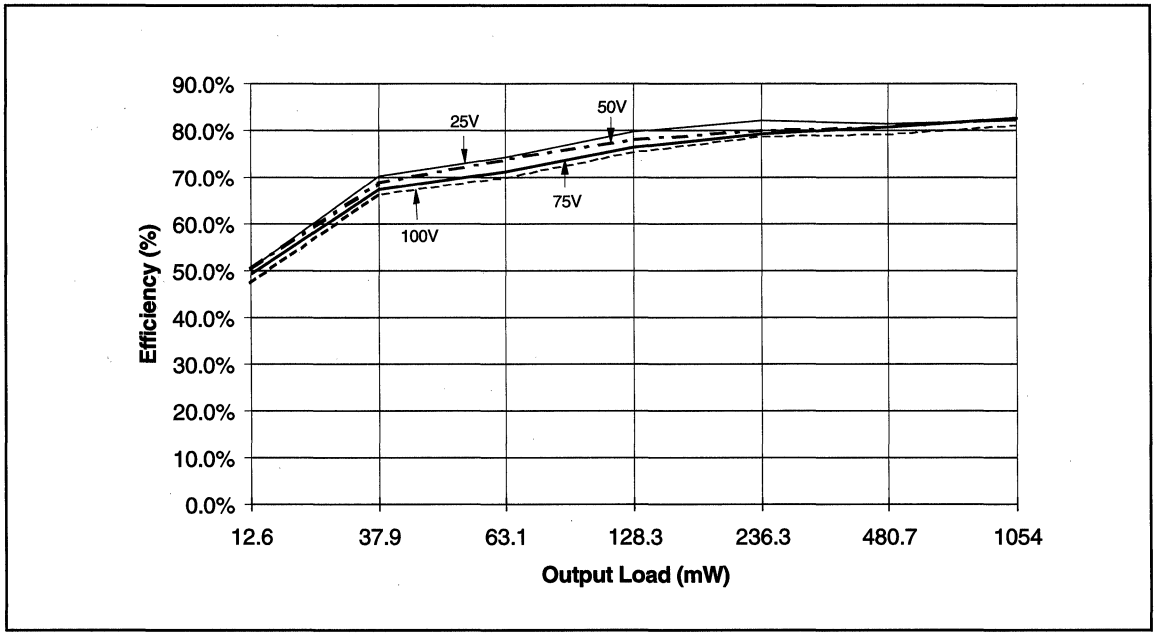


Figure 4. UCC3581 efficiency vs. line and load.

APPLICATION INFORMATION (cont.)

A rather large soft start capacitor was chosen to give a startup time of several hundred milliseconds, reducing the input surge current while the output is coming up.

Note that for stability, the UCC3581 V_{REF} bypass capacitor needs to be at least 1µF. The V_{DD} supply also needs some capacitance to hold it up between pulses at light load and high line, where the frequency may drop to less than 1kHz due to pulse skipping. Otherwise it may drop low enough for the startup MOSFET to be biased on, lowering efficiency.

If the sync input is used, it should not be left in a high impedance state where noise could cause false triggering. If unused, it should be grounded.

The transformer was designed with a standard Magnetics RM8 ferrite core using P material, gapped for an A_L of 1600mH/1000Turn^2. The primary consists of 44 turns, while the 5V secondary has 10 turns and the bootstrap winding 18 turns. For simplicity, all the windings can be #28 AWG. A two section bobbin was used to provide high primary to secondary isolation. A much smaller design, with reduced isolation, could have been done for this low power level.

TYPICAL CHARACTERISTIC CURVES

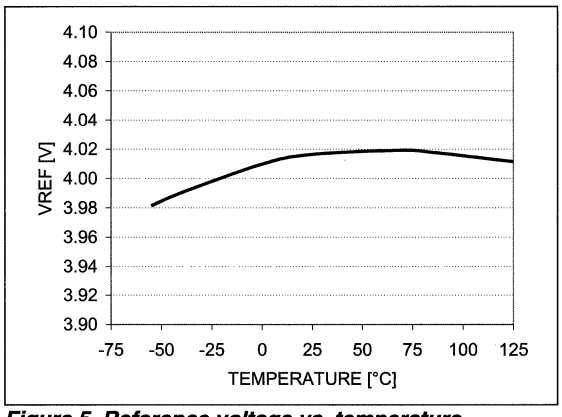


Figure 5. Reference voltage vs. temperature.

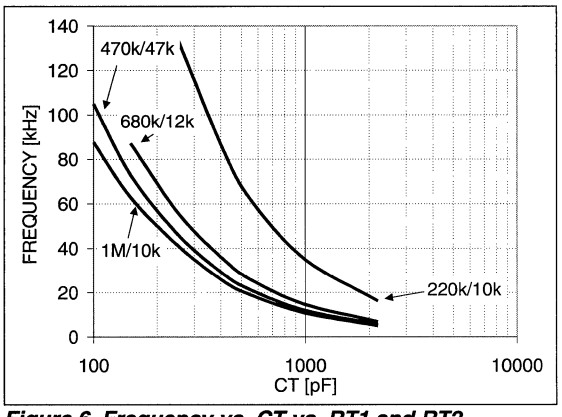


Figure 6. Frequency vs. CT vs. RT1 and RT2.

TYPICAL CHARACTERISTIC CURVES (cont.)

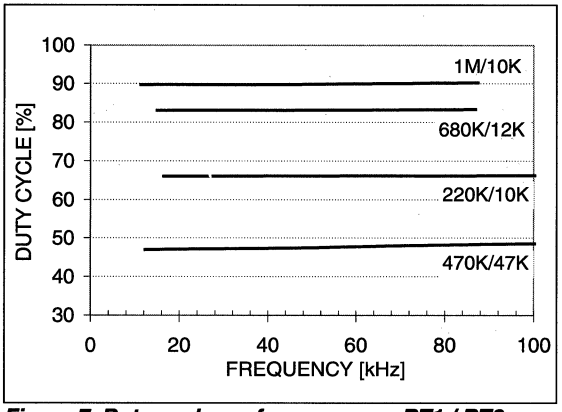


Figure 7. Duty cycle vs. frequency vs. RT1 / RT2.

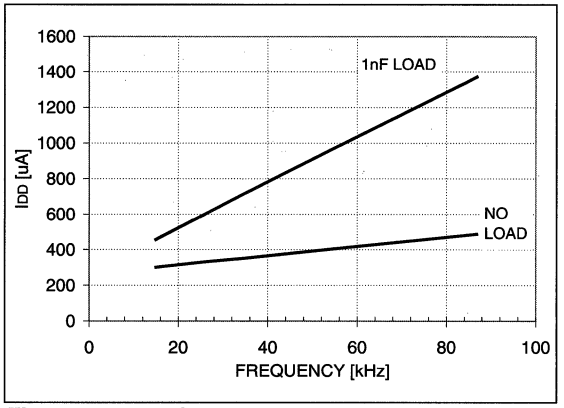


Figure 8. I_{DD} vs. frequency RT1 = 680k, RT2 = 12k.

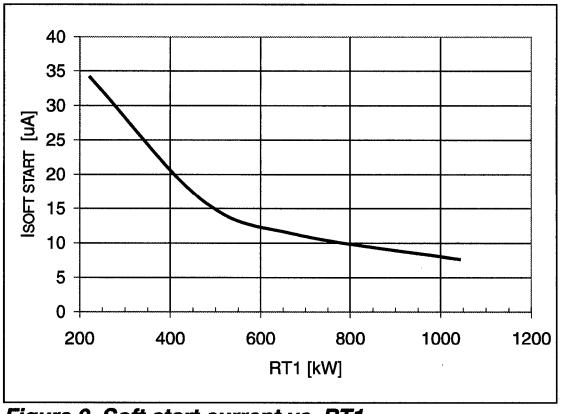


Figure 9. Soft start current vs. RT1.

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Switch Mode Secondary Side Post Regulator

FEATURES

- Precision Secondary Side Post Regulation for Multiple Output Power Supplies
- Useful for Both Single Ended and Center Tapped Secondary Circuits
- Ideal Replacement for Complex Magnetic Amplifier Regulated Circuits
- Leading Edge Modulation
- Does Not Require Gate Drive Transformer
- High Frequency (>500kHz) Operation
- Applicable for Wide Range of Output Voltages
- High Current Gate Driver (0.5A Sink/1.5A Source)
- Average Current Limiting Loop

DESCRIPTION

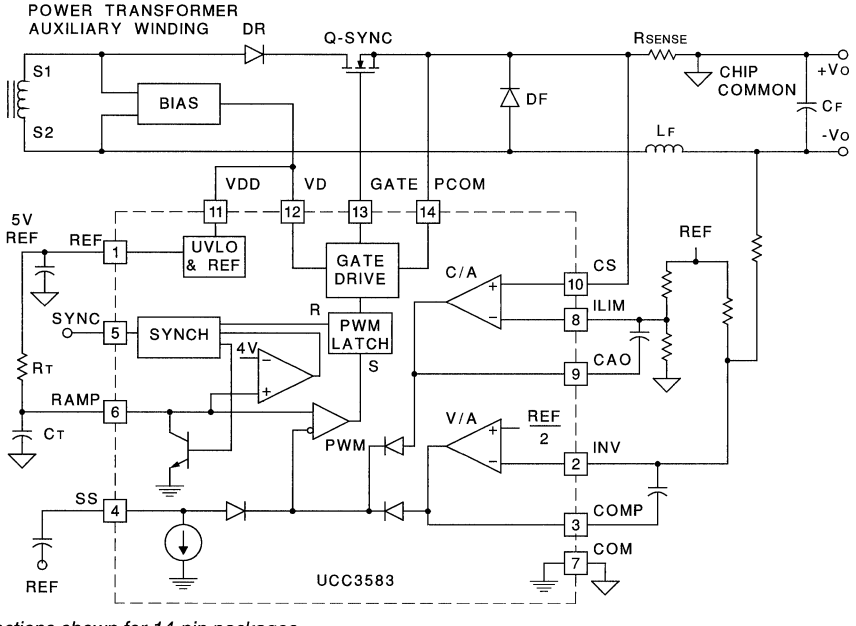
The UCC3583 is a synchronizable secondary side post regulator for precision regulation of the auxiliary outputs of multiple output power supplies. It contains a leading edge pulse width modulator, which generates the gate drive signal for a FET power switch connected in series with the rectifying diode. The turn-on of the power switch is delayed from the leading edge of the secondary power pulse to regulate the output voltage. The UCC3583 contains a ramp generator slaved to the secondary power pulse, a voltage error amplifier, a current error amplifier, a PWM comparator and associated logic, a gate driver, a precision reference, and protection circuitry.

The ramp discharge and termination of the gate drive signal are triggered by the synchronization pulse, typically derived from the falling edge of the transformer secondary voltage. The ramp starts charging again once its low threshold is reached. The gate drive signal is turned on when the ramp voltage exceeds the control voltage. This leading edge modulation technique prevents instability when the UCC3583 is used in peak current mode primary controlled systems.

The controller operates from a floating power supply referenced to the output voltage being controlled. It features an undervoltage lockout (UVLO) circuit, a soft start circuit, and an averaging current limit amplifier. The current limit can be programmed to be proportional to the output voltage, thus achieving foldback operation to minimize the dissipation under short circuit conditions.

(continued)

TYPICAL APPLICATION AND BLOCK DIAGRAM



Note: Pin connections shown for 14-pin packages.

UDG-96201-2

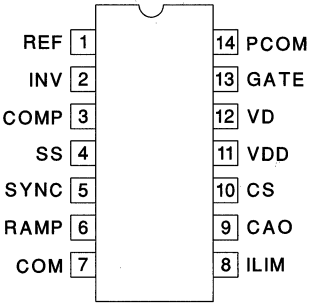
ABSOLUTE MAXIMUM RATINGS

V_{DD} 15V
I_{VDD} 15mA
RAMP ..... –0.3V to V_{DD} + 1V
I_{RAMP} 5mA
I_{REF} ..... –30mA
P_{COM} ..... –0.2V to 0.2V
I_{GATE} (twp < 1µS and Duty Cycle < 10%) ..... –0.8A to 1.8A
I_{COMP} ..... –5mA to 5mA
I_{CAO} ..... –5mA to 5mA
V_{SYNC} ..... –0.6V to V_{REF} +0.3V
I_{SYNC} ..... –05mA to 5mA
INV, SS, ILIM, ISENSE..... –0.3V to VREF + 0.3V
Storage Temperature ..... –65°C to +150°C
Junction Temperature..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.)..... +300°C

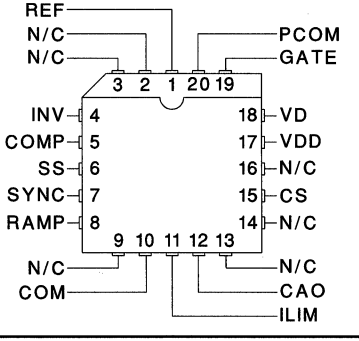
All voltages are with respect to the COM terminal unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)
J, N, or D Packages



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1583, –40°C to 85°C for UCC2583, and 0°C to 70°C for UCC3583; VDD = 12V, R_T = 60k, C_T = 200pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ramp Generation and Synchronization					
Maximum Input Operating Frequency	For input with 5% to 90% duty cycle (Note 1)	500			kHz
Ramp Frequency, Free Running		95	100	105	kHz
Ramp Discharge Current	V_{RAMP} = 0.5V	2.0	3.6		mA
Low Threshold Voltage	No min, no max, 0=TYP		0		V
High Threshold Voltage		3.75	4	4.25	V
Synchronizing Threshold Voltage (On)	(Note 1)		1		V
Synchronizing Comparator Hysteresis			1		V
Output Duty Cycle					
Minimum Duty Cycle	Output D/C = Output PW / Input PW			0	%
Maximum Duty Cycle	Output D/C = Output PW / Input PW	100			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for UCC1583, –40°C to 85°C for UCC2583, and 0°C to 70°C for UCC3583; VDD = 12V, R_T = 60k, C_T = 200pF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier					
V_{INV}	V_{COMP} = V_{INV}, 0°C to 70°C (UCC3583)	2.462	2.5	2.538	V
	V_{COMP} = V_{INV}, All Other Temperature Ranges	2.45	2.5	2.55	V
I_{INV}	V_{COMP} = V_{INV}		300	500	nA
V_{COMP} Low	V_{INV} = 2.6V, I_{COMP} = 100µA		450	700	mV
V_{COMP} High	V_{INV} = 2.4V, I_{COMP} = –100µA	5.0	5.5	6.0	V
AVOL	No Load	70	90		dB
GBW Product	At f = 100kHz, T_A = 25°C (Note 1)	3	5		MHz
Current Error Amplifier					
Input Offset Voltage				10	mV
Input CM Low	Common Mode for CS and ILIM (Note 1)			0	V
Input CM High	Common Mode for CS and ILIM (Note 1)	2			V
V_{CAO} Low	V_{+IN} = 0V, V_{-IN} = 0.1V, I_{CAO} = 100µA		250	500	mV
V_{CAO} High	V_{+IN} = 0V, V_{-IN} = 0.1V, I_{CAO} = –100µA	5.0	5.5	6.0	V
Input Current (ILIM and CS Pins)		–50	0	50	nA
AVOL	No Load	70	90		dB
GBW Product	At f = 100kHz, T_A = 25°C	2	4		MHz
Soft Start Current			10	25	µA
UVLO					
VDD On Threshold Voltage		8.5	9.0	9.5	V
VDD Off Threshold Voltage		7.9	8.4	8.9	V
UVLO Hysteresis		0.3	0.6	0.9	V
Bias Supply					
Supply Clamp Voltage		13	14	15	V
Supply Current (VDD)	f = 100kHz With No Gate Output Load		3	5	mA
Output Driver					
V_{SAT} High	I_{GATE} = –150mA		0.6	1.0	V
V_{SAT} Low	I_{GATE} = 50mA		0.4	0.75	V
Rise Time	C_{GATE} = 1nF		50	75	ns
Fall Time	C_{GATE} = 330pF		20	40	ns
Reference					
V_{REF}	I_{REF} = 0, 0°C to 70°C (UCC3583)	4.925	5	5.075	V
	I_{REF} = 0, All Other Temperature Ranges	4.900	5	5.100	V
Line Regulation	VDD = 10V to 14V		2	30	mV
Load Regulation	I_{REF} = 0mA to 2mA		1	20	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAO: Output of the current error amplifier. Averaging of the sensed current signal is provided by connecting an integrating capacitor between ILIM and CAO. CAO feeds into the PWM comparator input and controls the loop when its voltage is higher than the voltage at COMP (output of the voltage error amplifier).

COM: Signal ground for the chip. It is connected to the positive terminal of the output voltage being regulated by the IC.

COMP: Output of the voltage error amplifier fed into the PWM comparator. Loop compensation components are connected between COMP and INV.

CS: Non-inverting input of the current error amplifier. The sensed current signal from the current sense resistor is connected to this pin. By making the signal at CS proportional to the output voltage, effective current foldback limiting can be provided.

GATE: Gate drive output for the power switch FET. The drive pin has a 0.5A sink/1.5A source capability and very low output off-state impedance.

ILIM: Inverting input of the current error amplifier. It sets the DC limit for the output current.

INV: Inverting input of the voltage error amplifier. The feedback signal is connected to this pin using a resistive divider between REF and –Vo.

PCOM: Power ground for the chip. It is connected to the source terminal of the MOSFET being regulated by the IC.

RAMP: This pin is the input to the PWM comparator and provides a ramp signal for generation of the PWM signal. A capacitor to COM and a resistor to REF set the charging rate for the ramp. An internal current source of 1mA discharges RAMP when synchronization signal appears or when RAMP crosses a 4V threshold. In the intended mode of operation, the switching frequency is determined by the secondary power pulse. The RC components at RAMP should be selected to give an appropriately sized ramp signal. In the absence of a synchronizing pulse, these RC components determine the free running frequency of the controller.

REF: Precision 5V reference pin. REF stays off until VDD exceeds 9V and turns off again when VDD drops below 8.4V. Bypass REF to COM.

SS: This pin provides a soft start function. A capacitor to REF programs the soft start time. During soft start, the PWM comparator is controlled by the soft start voltage resulting in a slow increase in output duty cycle. Once the soft start capacitor is discharged, output control is dictated by the larger of the output at CAO or COMP.

SYNC: Synchronization input pin. It is connected to a signal representative of the secondary power pulse. One possible implementation is to use a resistive divider between terminal S2 of the secondary winding shown in Figure 1 and REF for generating the input to the SYNC pin. The synchronizing comparator is referenced to 0.5V and has ±500mV of hysteresis. The trip levels are approximate 1.0V and 0.0V. The designer should prevent the SYNC pin from exceeding 0.3V below ground as this will turn on the ESD diode.

VD: Power supply for the output driver. VD should be tied to VDD in the application.

VDD: Power supply for the chip. VDD should be bypassed to COM. VDD has to be 9V for the IC to start and 8.4V for it to remain operational. A shunt clamp from VDD to COM limits the supply voltage to 14V.

APPLICATION INFORMATION

Power Stage Circuit Configuration

The UCC3583 is designed for use in a post regulator application for tightly regulating auxiliary outputs in a multiple output converter. The post regulation is applied to the secondary side power pulse of a power transformer where the power pulse is controlled by the feedback signal from the main output. In order to simplify the application of the UCC3583, it is required that the IC be referenced to the positive output terminal and the output filter inductor be placed in the return path. The placement of the inductor in the return path facilitates better EMI performance, in addition to making magnetic designs and terminations easier to implement. Typical set-up and circuit waveforms of the UCC3583 system application are shown in Figure 1. Figure 2 shows waveforms for a single ended output rectifier application of the UCC3583 shown on page 1. The UCC3583 can also be used in half bridge rectifier applications as shown by the circuit and waveforms depicted in Figures 3 and 4. Referencing the IC to the positive output terminal creates a requirement for a floating bias voltage for the IC which can be referenced to the same positive voltage terminal. Possible implementations of deriving the floating bias voltage are shown in Figure 5.

APPLICATION INFORMATION (cont.)

For the circuit shown in Figure 5a, CC1 is charged when the transformer voltage is positive and the synchronous switch is on. During the off period of Q-SYNC, the charge is transferred to CC2 through diode DC2. Diode DC3 charges CC2 during the blocking interval of Q-SYNC. This method is preferable when the transformer positive voltage is high enough to generate the required bias voltage. For the circuit shown in Figure 5b, CC1 is charged during the period when reverse (reset) voltage appears across the secondary. The charge on CC1 is transferred to CC2 through DC2 when Q-SYNC turns on. This method is preferable when the reverse voltage is high enough to generate the required bias voltage. The series resistor should be chosen to handle the required voltage drop at full IC operating current when the zener clamp across VDD and COM is activated.

The following is a description of the major functional blocks of the UCC3583. Refer to Figure 6 (Typical Application Circuit) for component designations.

UVLO and Start Up

The UCC3583 has an internal undervoltage lockout circuit which keeps the internal circuitry inactive until VDD exceeds the upper threshold (9V). Once the chip is activated, VDD has to be above the lower UVLO threshold (8.4V) for it to remain functional. The IC requires a low startup current of only 100µA when VDD is under the UVLO threshold. VDD has an internal clamp of 14V which can sink up to 10mA. Measures must be taken not to exceed this current. The internal reference (REF) is brought up when the UVLO on threshold is exceeded.

The soft start pin provides an effective means to start the IC in a controlled manner. An internal current of 10µA starts discharging a capacitor connected to SS when the UVLO conditions have been removed. The voltage on SS controls the duty cycle of the output during the discharge period.

Synchronizing Circuit and Oscillator

UCC3583 is primarily intended for synchronizable operation where its switching frequency is determined by the secondary pulse of the power transformer. However, it has an internal oscillator which allows it to operate in free-running mode when an external synchronization pulse is not available. The switching frequency is determined by resistor RT connected between REF and RAMP and capacitor CT connected from RAMP to GND. The frequency is given by:

$$freq = \frac{1}{t_{CH} + t_{DIS}} \quad where \; t_{CH} = 1.56 \bullet R_T \bullet C_T$$

and

$$t_{DIS} = \frac{C_T \bullet V_{RAMP(p-p)}}{I_{RAMP(dis)}} \approx 3000 \bullet C_T$$

The values of RT and CT are also dictated by the fact that the ramp is discharged through an internal impedance of 2k. The value of RT needs to be at least 50k to ensure that the internal discharge current is the current through RT during the entire discharge period. This results in making the value of CT relatively small for a desired frequency of operation.

When the synchronizing signal is available, the oscillator frequency should be programmed to be lower than the synchronizing frequency to ensure proper operation. A large difference in self-running and synchronizing frequencies leads to smaller ramp amplitude and higher noise sensitivity. The ramp capacitor is discharged when the synchronization signal arrives and begins charging when the low threshold is crossed.

There are two methods to synchronize to the secondary pulse. One method is to use the rising edge of the secondary pulse, which reduces the maximum duty cycle available. Subsequently, the post regulator switch cannot be turned on during the CT discharge time. The other method is to use the falling edge of the secondary pulse for synchronization. This method is preferable because it allows a slower discharge of the ramp capacitor without affecting the maximum available duty cycle of the post regulator. The UCC3583 SYNC input needs to reach a fixed threshold (1.0V typical) for synchronization to take effect. Hence the IC is usable with either method of synchronization. However, the UCC3583 oscillator configuration is better suited for synchronization to the falling edge. A recommended method to implement the synchronization is shown in Figure 6. By connecting SYNC to a resistive divider between REF and the secondary terminal S2, the synchronization is achieved whenever the voltage on S2 goes from a negative value to zero. R_A and R_B should be selected so that the voltage on the SYNC pin varies from 0V to 1V. Placement of a Schottky diode from SYNC to COM prevents the voltage at SYNC from going negative. The internal hysteretic SYNC comparator has an inverting input set to 0.5V with about ±0.5V hysteresis.

PWM Comparator

The UCC3583 uses a leading edge PWM scheme. In a leading edge PWM, the output pulse (gate signal) is turned on when the error amplifier crosses the PWM ramp and turned off by the clock/oscillator. Leading edge modulation is naturally provided by magamp type post regulators and is an essential feature for post regulators. Without the leading edge modulation in a multiple output

APPLICATION INFORMATION (cont.)

converter with post regulation on one or more outputs, the primary current shape does not remain monotonic and can lead to instability when the primary current is used for current mode control or current limiting. When compared to conventional trailing edge PWMs, the leading edge modulation leads to a phase inversion that needs to be accounted for in the feedback loop. For the UCC3583, this inversion is automatically provided since the sensed voltage at the power supply output negative terminal has a negative polarity with respect to the chip common. Thus, UCC3583 does not require inverting buffers which would otherwise be needed.

Error Signal Generation and Current Limiting

The PWM comparator in the UCC3583 is controlled by three parallel loops with only one of them in effect at a time. During normal operation, the voltage error amplifier output is fed to the PWM comparator. The voltage error amplifier can be compensated using commonly used feedback techniques to achieve the desired dynamic performance. The ouput drive capability of the voltage amplifier is limited to 100µA, so appropriately high impedances should be used to utilize the full output swing of the amplifier. During startup, the soft start capacitor controls the pulse width. The third control loop is provided by the average current amplifier. By sensing the instantaneous inductor current and filtering/averaging it with the current error amplifier, accurate current limiting is achieved. This loop is in effect only during the overcurrent mode and provides a more accurate and noise free control of the maximum output current compared to conventional peak current limiting circuits. The current limit is set by programming the voltage at ILIM based on the current sense resistor chosen. In addition, the current limit can be made proportional to the output voltage in order to limit the power dissipation under short circuit conditions. This is implemented by inserting a bias voltage on CS which is proportional to the output voltage.

Gate Drive Circuit

The gate drive circuit of the UCC3583 provides high current drive capability and is very easy to implement as a result of tying the chip common to the source of the switching device. Turn on current is higher (1.5A) as fast turn on is essential for low losses and effective operation. During the turn off, the drain voltage disappears, so turn off time can be slower without increasing switching losses.

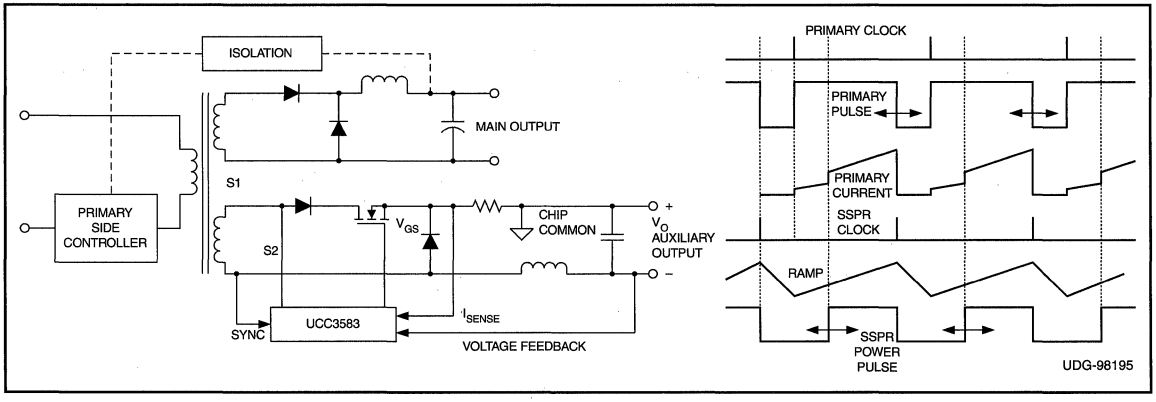
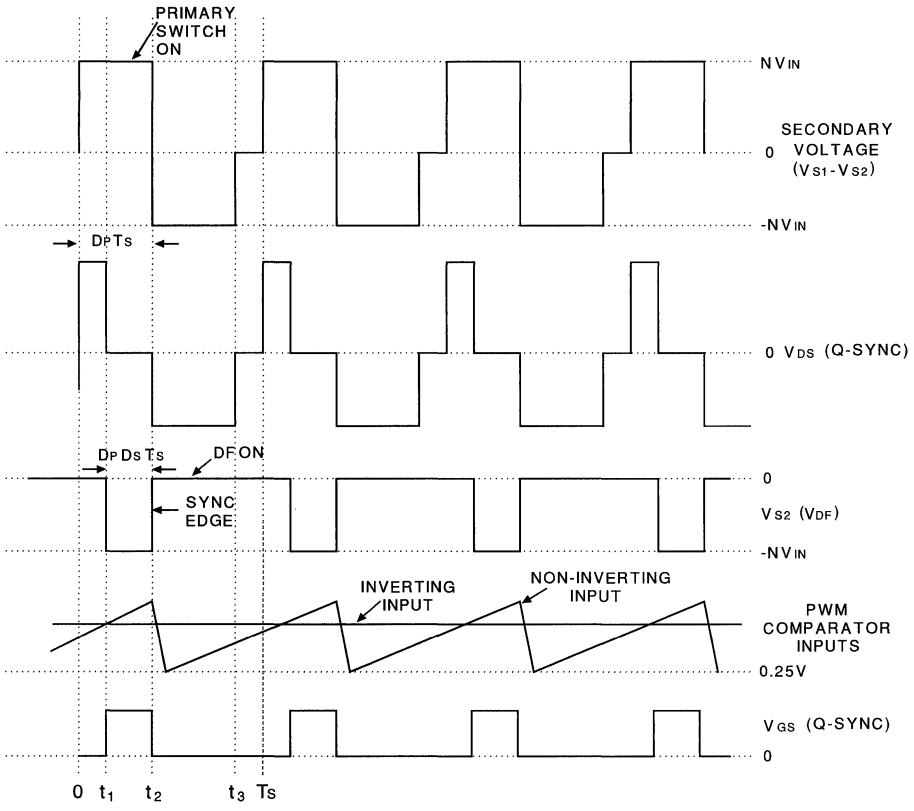


Figure 1. UCC3583 SSPR system application and typical waveforms.

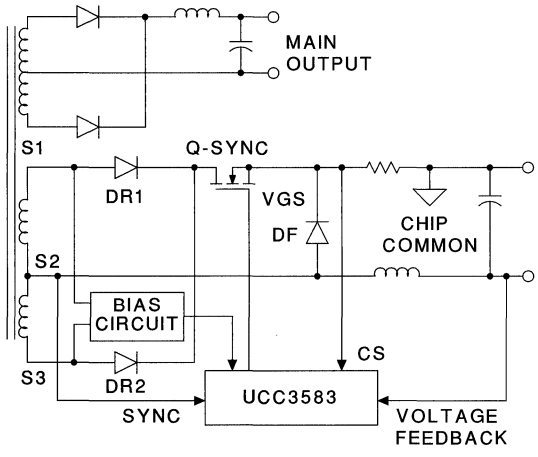
APPLICATION INFORMATION (cont.)



Note: All waveforms are referenced to chip common.

UDG-96141-1

Figure 2. Single ended post regulator waveforms.



UDG-96142-1

Figure 3. Half-bridge synchronous post regulator application.

APPLICATION INFORMATION (cont.)

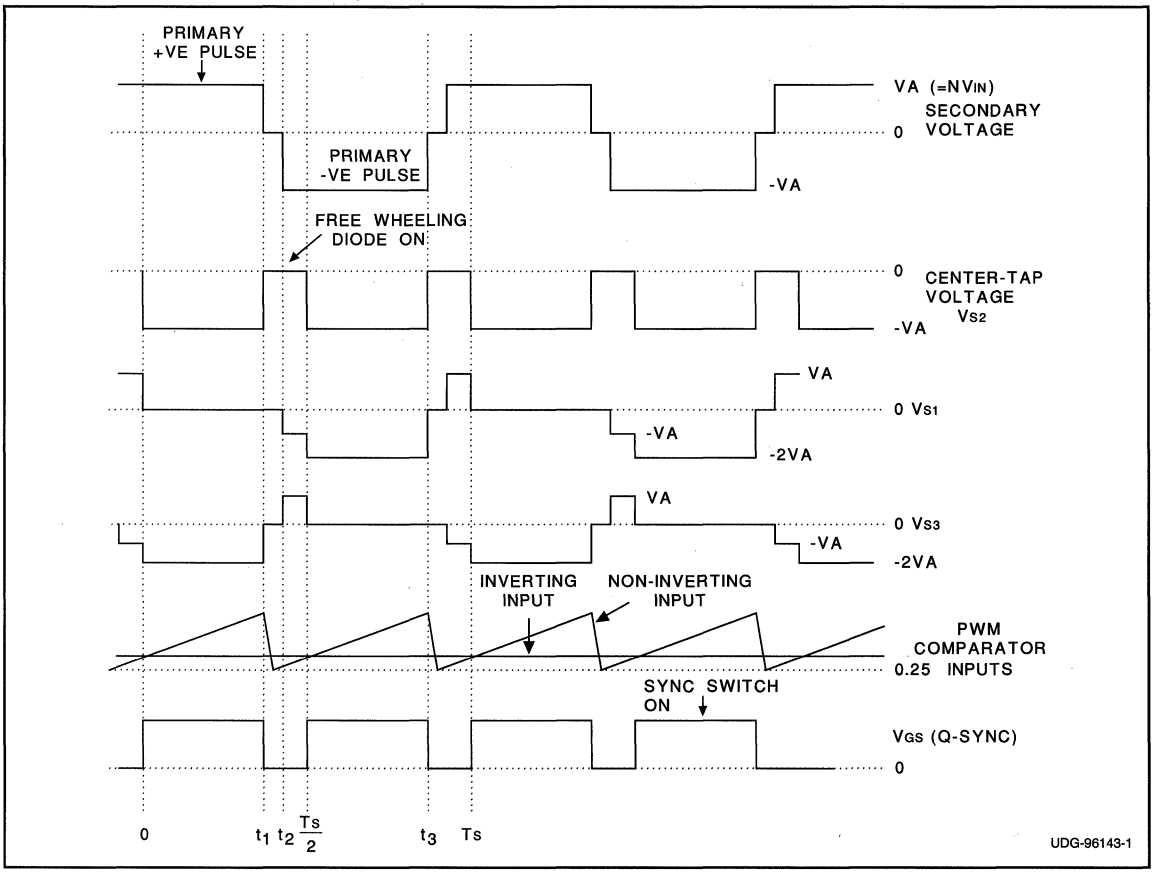


Figure 4. Half-bridge synchronous post regulator to waveforms.

APPLICATION INFORMATION (cont.)

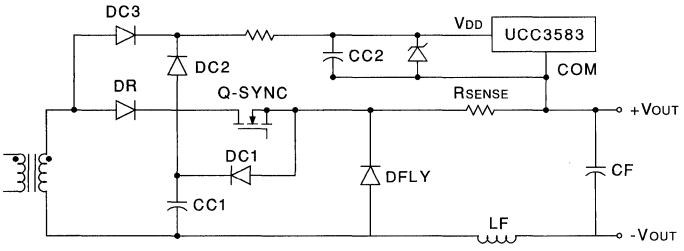


Figure 5a

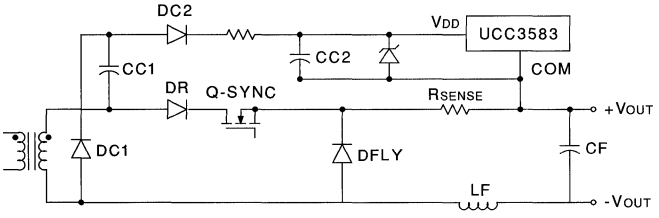
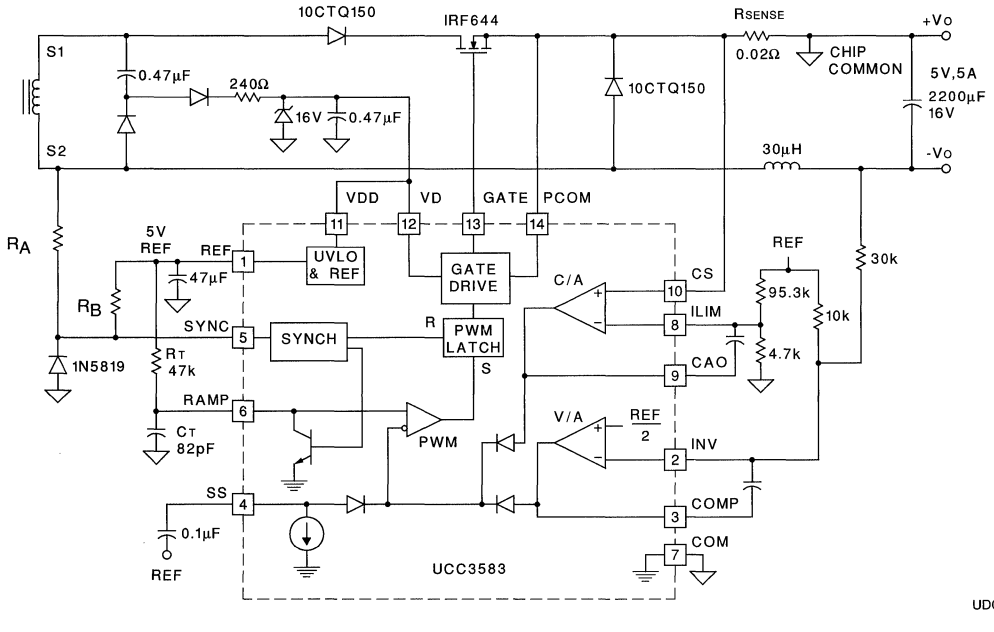


Figure 5b

UDG-96175-1

Figure 5. Possible implementation for floating bias voltage generation.



UDG-96072-2

Figure 6. Typical application circuit.

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application INFO available

UC1584
UC2584
UC3584

Secondary Side Synchronous Post Regulator

FEATURES

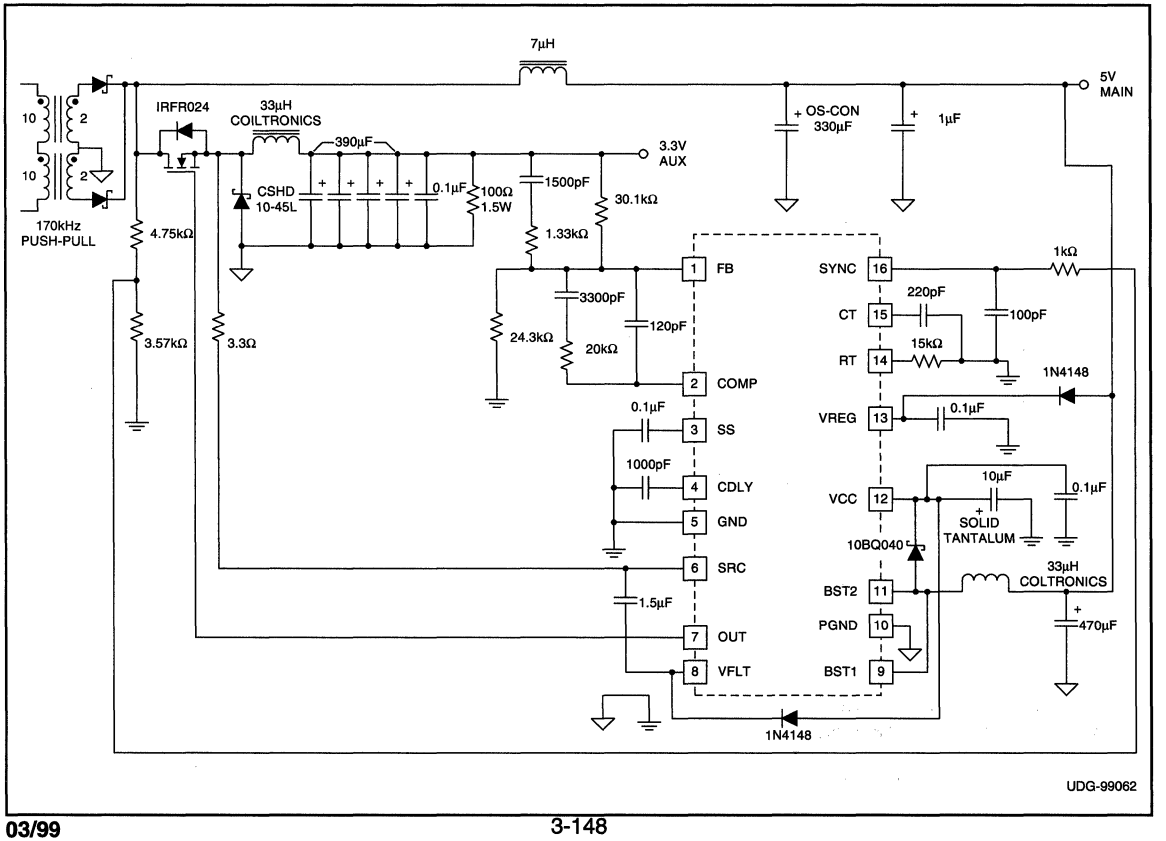
- Practical Operation at Switching Frequencies up to 1MHz
- Wide Band Error Amplifier
- Undervoltage Lockout with Hysteresis
- Output Active Low During UVLO
- Soft Start/Maximum Duty Cycle Control
- Trimmed Bandgap Reference
- Internally Regulated 15V Boost Supply
- Short Circuit Protection with Programmable Delay

DESCRIPTION

The UC3584 is a low voltage, Secondary Side Synchronous Post Regulator. It is intended to be used for auxiliary output voltage regulation in single secondary winding, multiple output power supplies (for more details refer to the Application Section of this Data sheet). The UC3584 is most suited for systems where the main output is regulated between 5V and 14V. Output voltages regulated by the UC3584 can range from virtually 0V up to the output voltage of the main output.

Auxiliary output voltage regulation with the UC3584 uses leading edge modulation making it compatible to primary side peak current or voltage mode control. The UC3584 clock circuit is synchronized to the switching frequency utilizing the falling edge of the transformer's secondary winding waveform.

TYPICAL APPLICATION DIAGRAM.



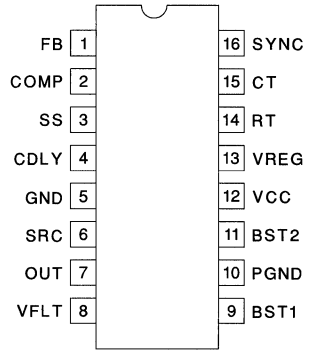
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
V_{FLT} Voltage . . . . . 50V, 30V at 2A
Supply Current 50mA
Analog Inputs . . . . . –0.3 to 20V
SYNC Maximum Sink Current 600µA
PWM Driver, I_{OUT} . . . . . ± 300mA
PWM Driver, I_{OUT} (Peak) . . . . . ± 1.5A
Maximum Operating Frequency 1MHz

Power Dissipation at T_A = 60°C 1W
Storage Temperature . . . . . –65°C to 150°C
Junction Temperature . . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . . 300°C
Currents are positive into, negative out of specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1584J	–55°C to +125°C	CDIP
UC2584DW	–40°C to +85°C	SOIC-Wide
UC2584N		PDIP
UC3584DW	0°C to +70°C	SOIC-Wide
UC3584N		PDIP

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3584, –40°C to 85°C for the UC2584, and –55°C to 125°C for the UC1584, VCC = 15V. $T_A = T_J$.

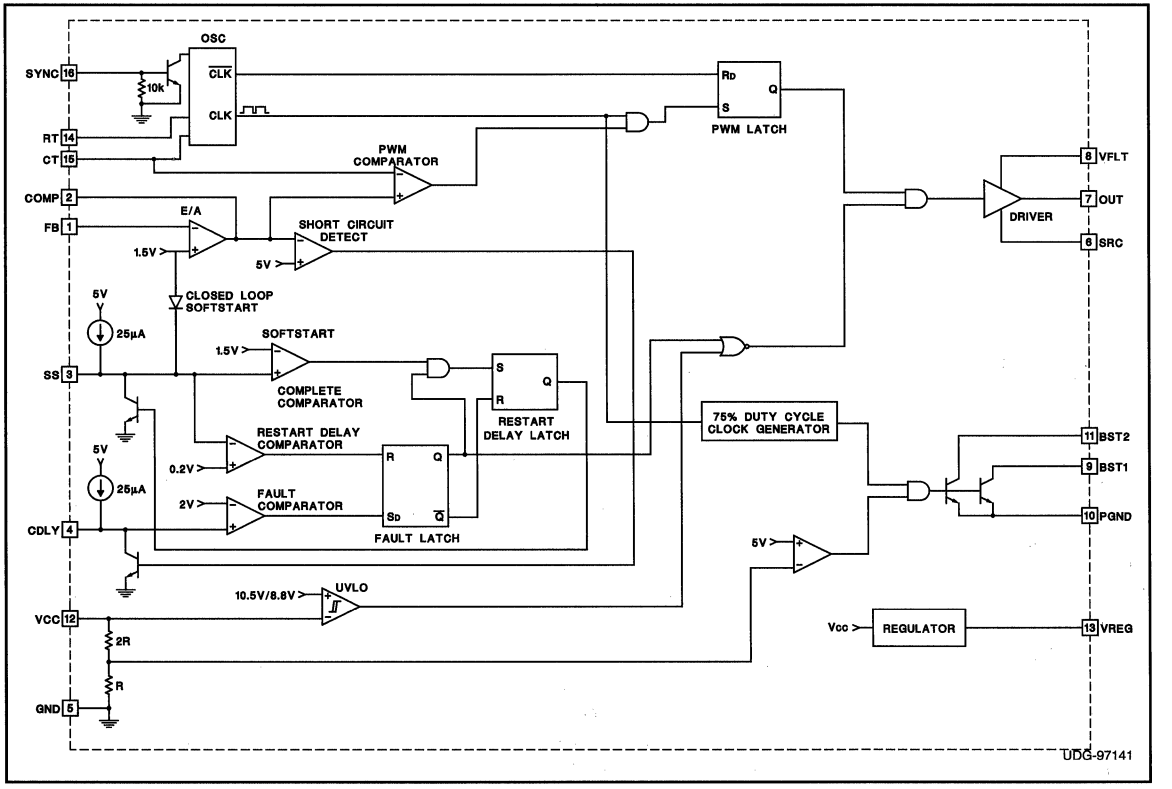
PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
Error Amplifier					
FB	COMP = FB	1.468	1.5	1.532	V
I_{FB}	$V_{COMP} = V_{FB}$	150	300	450	nA
COMP V_{OL}	FB = 1.6V, I_{COMP} = 200µA		50	400	mV
COMP V_{OH}	FB = 1.4V, I_{COMP} = –200µA	5.1	5.5	7	V
AVOL		60	80		dB
PSRR (COMP)	COMP = FB, VCC = 14V to 16V	60			dB
GBW Product	F = 100kHz	5	10		MHz
Oscillator					
Frequency	R_T = 3.75k, C_T = 400pF, No Synchronization		500		kHz
Ramp Low	R_T = 3.75k, C_T = 400pF, No Synchronization		1.75		V
Ramp High	R_T = 3.75k, C_T = 400pF, No Synchronization		3.5		V
Ramp Amplitude	R_T = 3.75k, C_T = 400pF, No Synchronization		1.75		V
PWM					
Maximum Duty Cycle	COMP = 4.5V	90			%
Minimum Duty Cycle	COMP = 0V			0	%
PWM DRIVER					
V_{SAT} High	$V_{FLT} - V_{OUT}$, I_{OUT} = –100mA		2.5	3	V
V_{SAT} Low	$V_{OUT} - V_{SRC}$, I_{OUT} = 50mA		0.8	2.2	V
T_{RISE}	Load = 1nF, SRC = 0V, Measure V_{OUT} 1V to 9V		75	100	ns
T_{FALL}	Load = 1nF, SRC = 0V, Measure V_{OUT} 9V to 1V		25	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UC3584, –40°C to 85°C for the UC2584, and –55°C to 125°C for the UC1584, VCC = 15V. $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYPE	MAX	UNITS
Soft Start					
Charge Current			30		µA
Discharge Current			1		mA
SS Delay	C_{SS} = 500nF		50		ms
Fault Latch					
Charge Current			30		µA
Discharge Current			5		mA
Fault Latch Delay	CDLY = 500nF		50		ms
UVLO					
VCC On			10.5		V
Hysteresis			1.7		V
Regulated Voltage					
V_{REG}	I_{REG} = 0mA to 1mA	4.8		5.2	V
VCC Regulator					
VCC	Boost inductor connected to 5V	14	15	16	V
I_{CC}	No Load, Boost Circuitry Inactive		12	40	mA
	No Load, Boost Circuitry Active (Note 1)		55		mA

Note 1: Guaranteed by design. Not 100% tested in production.

BLOCK DIAGRAM



PIN DESCRIPTIONS

BST1: Collector of the boost switch. This is the connection point of the external boost inductor and boost diode. The boost converter generates the bias supply for the UC3584 from the regulated 5V output.

BST2: See BST1. BST2 must be connected externally to BST1 pin.

CDLY: Delay Set. External CDLY capacitor sets the delay from the time Short Circuit condition is detected and Fault Condition is asserted.

COMP: Output of the Voltage Error Amplifier.

CT: Connect the Timing Capacitor between CT and GND.

FB: Inverting Input of the Voltage Error Amplifier.

GND: Analog System Ground.

OUT: Output of the floating driver for an external, N-channel MOSFET.

PGND: Power Ground. This is the reference node for the boost bias supply regulator. PGND and GND must be connected externally.

RT: A Timing Resistor connected between RT and GND sets the discharge current of the timing capacitor.

SRC: Source connection of the floating driver to the external switch.

SS: Soft Start. An external capacitor is connected between SS and GND to set the duration of the Soft Start cycle.

SYNC: Synchronization Pin. The UC3584 is synchronized from the falling edge of the transformer's secondary winding. Voltage must exceed 1V at minimum input line.

VCC: Bias supply of the chip, approximately 15V. This is also the output of the boost regulator. The VCC pin must be decoupled to PGND.

VFLT: Positive rail of the floating driver's bias supply. Decouple to SRC using a high frequency (ceramic) capacitor.

VREG: Output of the internal 5V regulated supply. Must be decoupled to GND.

APPLICATION INFORMATION

Biasing the UC3584

Bias supply for the UC3584 is generated from the main output of the power supply by a boost regulator. The inductor, diode and capacitor of the boost converter are external components, while the boost switch is internal to the chip. The boost converter operates in a burst mode with a built-in hysteresis of approximately 1V centered at 15V. This is a bang-bang controller and when enabled has a fixed duty cycle of 75%.

Undervoltage Detection

The UVLO circuit of the UC3584 monitors the voltage on VCC. During power up and power down, the pulse width modulator and the output driver are disabled and OUT is held active low. Operation is enabled when VCC reaches 10.5V. The UVLO circuitry has a built-in hysteresis of 1.7V (10.5V to 8.8V) thus VCC must drop below 8.8V in order to assert UVLO again.

Precision Reference

An internal precision bandgap reference provides accurate voltages to the error amplifier and other control sections of the IC. A buffered 5V regulated voltage is also available for external circuitry on the VREG pin. This pin must be decoupled to the signal GND connection by a good quality high frequency capacitor.

Oscillator and Trailing Edge Synchronization

The UC3584 is outfitted with a synchronizable oscillator which also generates a ramp signal across the CT capacitor for the PWM comparator. For easy implementation of the leading edge pulse width modulation technique, the oscillator has an inverted ramp waveform as shown in Fig. 1. The free running oscillator frequency is determined by the timing components, RT and CT, according to the following approximate equations:

$$R_T = \left(\frac{9.3}{1 - D_{MAX}}\right)^{1.7}$$

$$f_{OSC} = \frac{2 - \left(8.2 \times 10^8 \bullet C_T\right)}{\left(R_T \bullet C_T\right)^{0.9}}$$

where

R_T is the timing resistor, its value should be between 1kΩ and 100kΩ,

C_T is the timing capacitor,

D_{MAX} is the desired maximum duty cycle, and

f_{OSC} is the free running oscillator frequency.

APPLICATION INFORMATION (cont.)

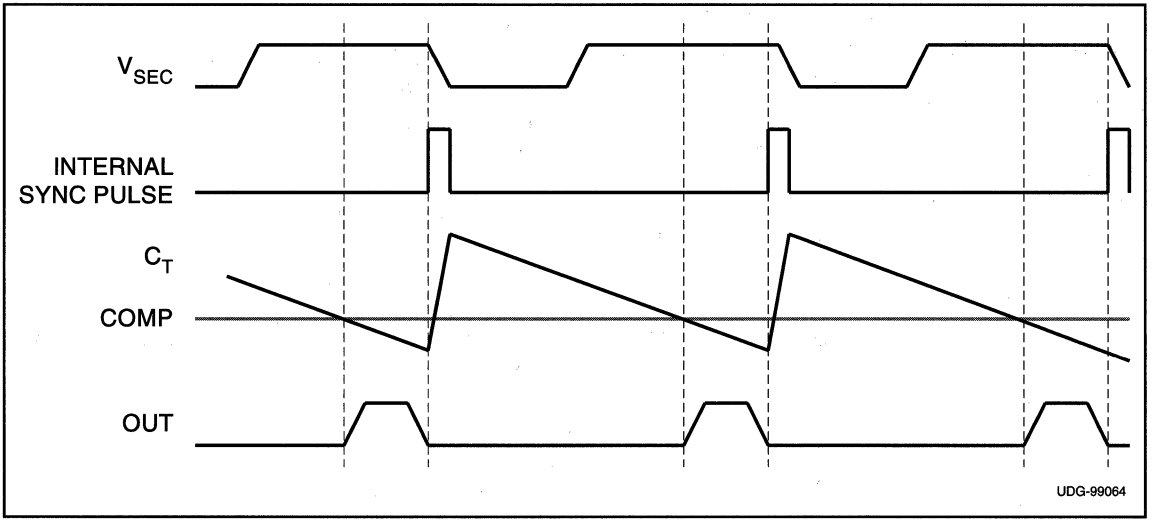


Figure 1. Trailing edge synchronization, leading edge modulation.

Figure 2 graphically depicts the measured frequency data.

Edge Modulation

During normal operation the oscillator must be synchronized to the falling edge of the transformer secondary waveform. Synchronization is achieved by connecting SYNC to the secondary winding via a resistor divider. The resistor divider must be chosen to provide a SYNC pin voltage in excess of 1V at the lowest operating voltage on the transformer secondary winding. The UC3584 will generate a narrow internal synchronization pulse which will synchronize the oscillator to the switching frequency of the main converter.

PWM and Output Driver

The UC3584 employs leading edge modulation technique to set the required on time of its output. Leading edge modulation is preferred for secondary side regulation in multiple output converters to prevent ambiguity in the primary current waveform. In fact, this is the only feasible technique to preserve compatibility with primary side peak current mode control.

As Fig. 1 depicts the UC3584 utilizes voltage mode control to regulate output voltage. The output pulse width (the on-time of the MOSFET switch) is determined on a cycle-by-cycle basis by comparing the output of the voltage error amplifier and the ramp waveforms across the timing capacitor. OUT is asserted when the voltage on COMP exceeds the voltage on CT. There are three more conditions which must be satisfied to obtain an active high on the OUT pin. These conditions are:

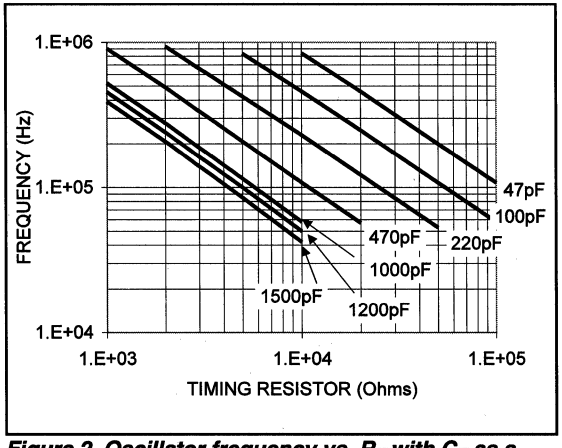


Figure 2. Oscillator frequency vs. R_T with C_T as a parameter.

APPLICATION INFORMATION (cont.)

1. VCC within normal range (UVLO is inactive),
2. No fault condition is detected,
3. C_T is discharging.

During the fast charging time of the C_T capacitor is held low.

Ultimately, the output of the PWM circuitry controls the conduction interval of an external N-channel MOSFET switch in the power supply. The UC3584 employs an on-board, floating gate driver circuit to interface to the external switch. An external capacitor connected between VFLT and SRC acts as a floating power supply for the driver during the on-time of the switch. Charge is being replenished to the bootstrap capacitor during the off-time of the switch through the bootstrap diode connected between VCC and VFLT as shown in the typical application diagram.

Soft Start

The UC3584 Soft Start circuitry is designed to implement closed loop startup of the power supply output. During Soft Start, the reference to the noninverting input of the error amplifier is controlled by the voltage across the soft start capacitor on SS. As this voltage rises, it provides an increasing reference to the error amplifier. Once the soft start capacitor charges above the 1.5V precision reference of the error amplifier, SS gets disconnected from the noninverting input of the error amplifier. This technique allows the error amplifier to stay in its linear mode and to regulate the output voltage of the power supply according to the gradually increasing reference voltage on its noninverting input. Further advantage of the closed loop start up scheme is the absence of output voltage overshoot during power up of the power supply output.

Fault Detection

Fault Detection feature is implemented to detect excessive overload conditions. Under these conditions the error amplifier output goes high to command the maximum duty cycle. As soon as the error amplifier's output exceeds 5V, the fault delay capacitor connected to the CDLY pin starts charging. If C_{DLY} capacitor voltage reaches 2V before the error amplifier output falls back below 5V, a fault condition is declared, the PWM output is disabled and soft start cycle is initiated. Under persistent fault conditions the UC3584 will continuously cycle through soft start sequence, attempting to bring the output to its regulated, nominal voltage. The value of C_{DLY} capacitor should be chosen large enough to delay the activation of the fault sequence in case of load transients which can also cause the error amplifier output to go high temporarily.

Error Amplifier

The Error Amplifier of the UC3584 is used to regulate the voltage of an auxiliary output in a power supply. The noninverting input of the error amplifier is connected to an internal, 1.5V reference. The inverting input (FB pin) is tied to an output voltage divider. The compensation network of the negative feedback loop is connected between the amplifier's output (COMP pin) and FB. The noninverting input of the error amplifier is also connected to the SS node through a diode. This arrangement allows closed loop soft start for the output of a power supply regulated by the UC3584. Closed loop soft start assures that the error amplifier is kept in active mode and the output voltage of the converter follows the reference voltage on its noninverting input as it ramps up (following the SS node). If a fault condition is detected, SS node gets pulled to ground, forcing the error amplifier's reference low. Consequently, the error amplifier's output voltage goes low and duty cycle is reduced.

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Low Voltage Synchronous Buck Controller

FEATURES

- Resistor Programmable 1.25V to 4.5V V_{OUT}
- 2.5V to 6V Input Supply Range
- 1% DC Accuracy
- High Efficiency Synchronous Switching
- Drives P-channel (High Side) and N-channel (Low Side) MOSFETs
- Lossless Programmable Current Limit
- Logic Compatible Shutdown
- Programmable Frequency
- Start-up Voltage Tracking Protects Dual Rail Microprocessors

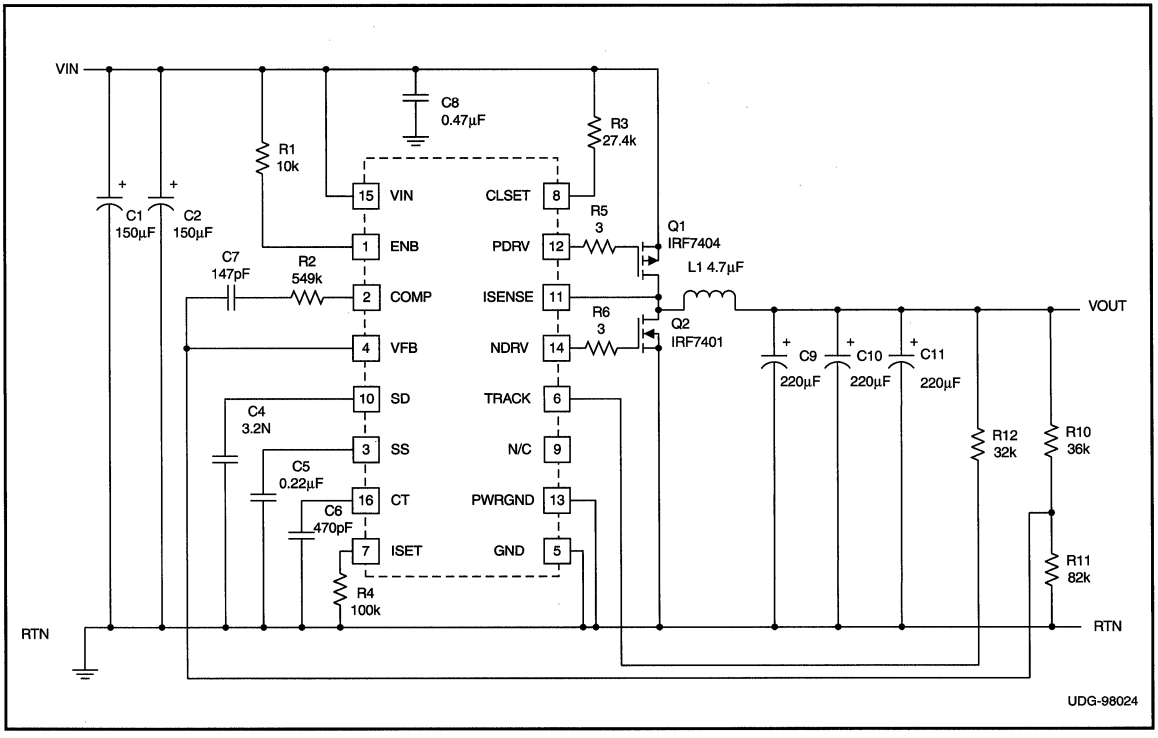
DESCRIPTION

The UCC2585/UCC3585 synchronous Buck controller provides flexible high efficiency power conversion for output voltages as low as 1.25V with guaranteed ±1% DC accuracy. Output currents are only limited by the choice of external logic level MOSFETs. With an input voltage range of 2.5V to 6.0V it is the ideal choice for 3.3V only, battery input, or other low voltage systems. Applications include local microprocessor core voltage power supplies for desktop and Notebook computers, and high speed GTL bus regulation. Its fixed frequency oscillator is capable of providing practical PWM operation to 700kHz.

With its low voltage capability and inherent "always on" operation, the UCC2585/UCC3585 causes VOUT to track VIN once VIN has exceeded the threshold voltage of the external P channel MOSFET. Tracking can be tailored for any application with a single resistor or disabled by connecting TRACK to VIN. For dual supply rail microprocessors this feature negates the need for external diodes to insure supply voltage tracking between the +3.3V and lower voltage microprocessor core supplies.

(continued)

TYPICAL APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Analog Pins
  Minimum and Maximum Forced Voltage
  (Reference to GND) ..... –0.3V to +6.3V
Digital Pins
  Minimum and Maximum Forced Voltage
  (Reference to GND) ..... –0.3V to 6.3V
Power Driver Output Pins
Maximum forced current ..... ±1.0A
Operating Junction Temperature ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C

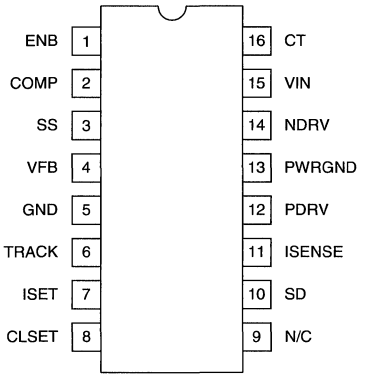
Note: *Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns.*

APPLICATIONS

- Low Voltage Microprocessor Power such as PowerPC 603 and 604
- High Power 5V or 3.3V to 1.25V–4.5V Regulators
- GTL Bus Termination

CONNECTION DIAGRAMS

DIL-16, SOIC-16, SSOP-16 (TOP VIEW)
J, N, D, and M Packages



DESCRIPTION (cont.)

The UCC2585/UCC3585 drives a complementary pair of power MOSFET transistors, P-channel on the high side, and N-channel on the low side to step down the input voltage at up to 90% efficiency.

A programmable two-level current limiting function is provided by sensing the voltage drop across the high side P channel MOSFET. This circuit can be configured to provide pulse-by-pulse limiting, timed shutdown after 7 consecutive faults, or latch-off after fault detection, allowing maximum application flexibility. The current limit threshold is programmed with a single resistor selected to match system MOSFET characteristics.

The UCC2585/UCC3585 also includes undervoltage lockout, a logic controlled enable, and softstart functions. The UCC2585/UCC3585 is offered in the 16 pin surface mount and through hole packages.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3585, and T_A = –40°C to 85°C for the UCC2585. T_A = T_J. VIN = 3.3V, ENB, I_{SENSE} = V_{IN}, V_{FB} = 1.25V, COMP = 1.5V, C_T = 330pF, R_{ISET} = 100k, RTRACK = 10k, RCLSET = 10k.

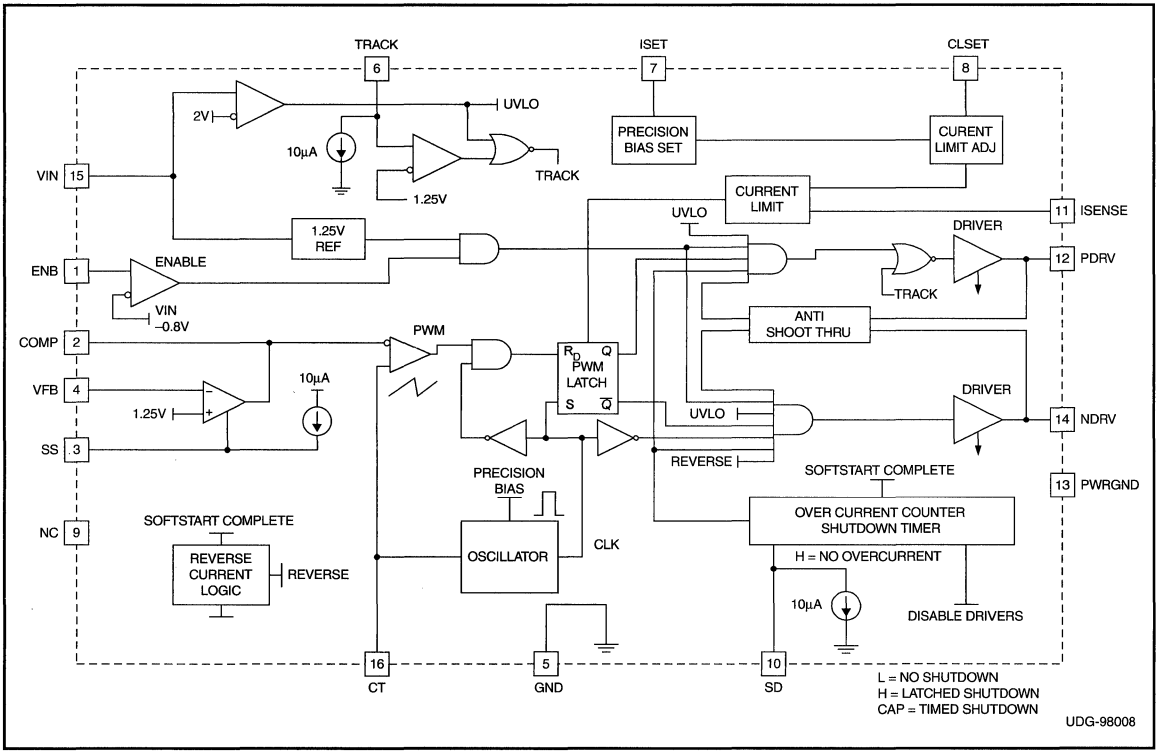
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Section					
Supply Current – Total (Active)			2.3	3.5	mA
Supply Current – Shutdown	ENABLE = 0V		10	25	µA
VIN Turn On Threshold (UVLO)			2.35	2.60	V
VIN Turn On Hysteresis			450	550	mV
Voltage Amplifier Section					
Input Voltage (Internal Reference)	T_A = 0°C to 70°C, VIN = 3.0V to 3.6V, Note 1	1.238	1.250	1.262	V
Input Voltage (Internal Reference)	VIN = 3.0V to 3.6V, IND/MIL Temp, Note 1	1.228	1.250	1.273	V
Open Loop Gain	COMP = 0.5 to 2.5V	65	80		dB
Output Voltage High	I(COMP) = –50µA	3.00	3.25		V
Output Voltage Low	I(COMP) = 50µA		0.10	0.25	V
Output Source Current		–100	–175		µA
Output Sink Current		0.4	1.0		mA
Oscillator/PWM Section					
Initial Accuracy	T_J = 25°C	405	450	495	kHz
Initial Accuracy	Over Temperature	390	450	510	kHz
CT Ramp Peak to Valley		1.8	2.1	2.4	V
CT Ramp Valley Voltage		0.3	0.4		V
PWM Maximum Duty Cycle	COMP = 3V, Measured on PDRV	100			%
PWM Minimum Duty Cycle	COMP = 0.2V, Measured on PDRV			0	%
PWM Delay to Outputs	COMP = 2.5V		45		ns
Tracking Current	Measured on TRACK, V_{TRACK} = 1.6V	10	12	15	µA
Enable High Threshold	Measured on ENABLE (Note 3)		2.8		V
Enable Low Threshold	Measured on ENABLE		0.5		V
Softstart Charge Current	SS = 0V	–10	–14	–18	µA
Current Limit Section					
Pulse to Pulse Threshold	Measured Between V_{IN} and I_{SENSE}	100	125	150	mV
CLSET Current		11	14	16	µA
SD Sink Current	SD = 2V	8	13	18	µA
SD Source Current	SD = 2V		–100	–140	µA
Restart Threshold	Measured on SDOWN	0.40	0.55	0.90	V
Output Driver Section (PDRV, NDRV)					
Pull Up Resistance	–100mA (Source) T_A = 25°C		6		Ω
Pull Down Resistance	100mA (Sink) T_A = 25°C		4		Ω
Deadtime Delay	Note 2	150	200	250	ns

Note 1. Measured on COMP with the Error Amp in a Unity Gain (voltage follower) configuration.

Note 2. 50% point of PDRV Rise to NDRV Rise and 50% point of NDRV Fall to PDRV Fall.

Note 3. Enable High Threshold = V_{IN} –0.5.

BLOCK DIAGRAM



PIN DESCRIPTIONS

CLSET: CLSET is used to program the pulse by pulse and overcurrent shutdown levels for the UCC1585. A resistor is connected between CLSET and VIN to set the thresholds. The threshold follows the following relationship:

$$Icl = \frac{\frac{1.25}{R_{ISET}} \bullet R_{CLSET}}{RDS(on)}$$

COMP: Output of the Voltage type error amplifier. Loop compensation components are connected between COMP and VFB.

CT: A high quality ceramic capacitor connected between this pin and ground sets the PWM oscillator frequency by the following relationship:

$$F = \frac{1}{(6700 \bullet CT)}$$

Use capacitor values greater than 100pF in order to minimize the effects of stray capacitance. The oscillator is capable of reliable operation in excess of 1MHz.

ENB: A LOGIC1 (V_{IN}–0.5V) on this input will activate the Output drivers. A logic zero (0.5V) will prevent switching of the output drivers. Do not allow ENB to remain between these levels steady state.

GND: Reference level for the IC. All voltages and currents are with respect to GND.

ISENSE: ISENSE performs two functions. The first is to monitor the voltage dropped across the high side P channel MOSFET switch while it is conducting. This information is used to detect over current conditions by the current limit circuitry. The second function of ISENSE is to measure current through the lowside N-channel MOSFET. When the current flow through this MOSFET is drain to source, (i.e. reversed), this FET is turned off for the remainder of the switching cycle.

PIN DESCRIPTIONS (cont.)

ISET: A resistor is connected between ISET and ground to program a precision bias for many of the UCC2585/UCC3585 circuit blocks. Allowable resistor values are 90kΩ to 110kΩ. 1.25V is provided to ISET via a buffered version the internal bandgap voltage reference. The resultant current is 1.25V / R_{ISET}.This current is mirrored directly over to CLSET to program the over current thresholds. A second use for this current is to set a basis for the charging current of the oscillator.

PDRV: High current driver output for the high side P channel MOSFET switch. A 3Ω to 10Ω series resistor between PDRV and the MOSFET gate may be inserted to reduce ringing on this pin. In some layout situations, a low V_F diode may be required from this pin to ground to keep the pin from ringing more than 0.5V below ground.

PWRGND: High current return path for the MOSFET drivers. PWRGND and GND should be terminated together as close to the IC package as possible.

SD: This pin can configure current limit to operate in any one of three different ways.

1) A forced voltage of less than 250mV on SD inhibits the shutdown function causing pulse by pulse limiting.

2) A capacitor from SD to GND provides a controller-converter shutdown timeout after 7 consecutive overcurrent signals are received by the current limit circuitry. An interval 10μA (typ) current source discharges the SD capacitor to the 0.5V (typ) restart threshold. The shutdown time is given by:

$$T_{SHUT} = \frac{[C_{SD} \bullet (V_{IN} - 0.5)]}{10\mu A},$$

where C_{SD} is the value of the capacitor from SD to GND, and VIN is the chip supply voltage (on pin 15). At this point, a softstart cycle is initiated, and a 100μA current (typ) quickly recharges SD to VIN. During softstart, pulse by pulse limiting is enabled, and the 7 cycle count is delayed until softstart is complete (i.e. charged to approximately VIN volts).

3) A forced voltage of greater than 1V on SD will cause the UCC2585/UCC3585 to latch OFF after 7 overcurrent signals are received. After the controller is latched off, SD must drop below 250mV to restart the controller.

SS: A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor will slowly charge on start-up via an internal current source. The output of the Voltage error amplifier (COMP) tracks this voltage thereby limiting the controller duty ratio.

NDRV: High current driver output for the low side MOSFET switch. A 3Ω to 10Ω series resistor between NDRV and the MOSFET gate may be inserted to reduce ringing on this pin. In some layout situations, a low V_F diode may be required from this pin to ground to keep the pin from ringing more than 0.5V below ground.

TRACK: A resistor is connected between TRACK and output voltage of the converter to set the start-up profile of the power converter. Certain dual supply rail microprocessors require that a maximum voltage differential between the supply rails is not exceeded. Failure to do so results in large currents in the microprocessor through the ESD (electrostatic discharge) protection devices. This can result in chip failure. The UCC2585/UCC3585 is designed such that it is "normally on" before V_{IN} reaches the 2.0V (nom.) UVLO threshold. That is, the high side P channel MOSFET switch driver output is actively held low allowing the MOSFET to conduct current to the output as soon as V_{IN} is high enough to exceed the gate turn on threshold. The resistor from TRACK to V_{OUT} sets the voltage level on VOUT at which the P channel MOSFET is turned off. The tracking cutoff voltage follows the following relationship:

$$V_{OUT}(\max) = 1.25V + 12\mu A \bullet (R_{TRACK})$$

This is necessary for very low output voltage applications (< 2.0V), where overvoltage may occur if the Pchannel MOSFET is not disabled before the UVLO threshold is reached. For applications with V_{OUT} greater than 2.0V, TRACK can be disabled by tying TRACK to V_{IN}.

VFB: Inverting input to the Voltage type error amplifier. The common mode input range for VFB extends from GND to 1.5V.

VIN: Supply voltage for the UCC2585/UCC3585.Bypass with a 0.1μF ceramic capacitor (minimum) to supply the switching transient currents required by the external MOSFET switches.

APPLICATION INFORMATION

Some of today's microprocessors require very low operating voltages. In some cases, as low as 1.8V of supply voltage are required in addition to already available 3.3V system voltage. Following is an illustration of a design using the UCC3585 as the power controller.

The design criteria are as follows:

- Input Voltage (V_{IN}) 3.3V DC
- Output Voltage (V_{OUT}) 1.8V DC
- Output Ripple Voltage (V_{OUT}) 18mV
- Output Current (I_{OUT}) 3.5A DC

Other features include

- Output Tracking
- Switching Frequency (F_S) 350kHz
- 100% Surface Mount

The first few steps in the design are to define the power stage (Schematic Fig. 1).

1) The normal operating duty cycle (δ) of the regulator is approximately

$$\delta = \frac{V_{OUT}}{V_{IN}} = \frac{1.8}{3.3} = 0.545$$

2) Select the output inductor to meet ripple current requirements. For this design, the allowable ripple current in the output inductor is selected to be 10% of the full load output current.

$$L1 = \frac{(V_{IN} - V_{OUT}) \bullet \delta}{F_S \bullet 0.1 \bullet I_{OUT}} = 4.6\,\mu H$$

A Pulse Engineering SMT inductor (PE-53682) is 4.7µH has a DC resistance (R_{L1}) of 8.3mΩ and will dissipate 0.1W under full load operation.

The resulting ΔI_{OUT} is now:

$$\Delta I_{OUT} = \frac{(V_{IN} - V_{OUT})}{4.7 \bullet 10^{-6}} \bullet \frac{\delta}{Fs} = 0.5\,A$$

3) Next, the output capacitors are determined based upon the output ripple criteria. Assuming the ripple is limited by the equivalent series resistance, or ESR, of the capacitors and not the impedance of the capacitors at the switching frequency, then the output capacitor selection is based upon ESR, size and voltage considerations.

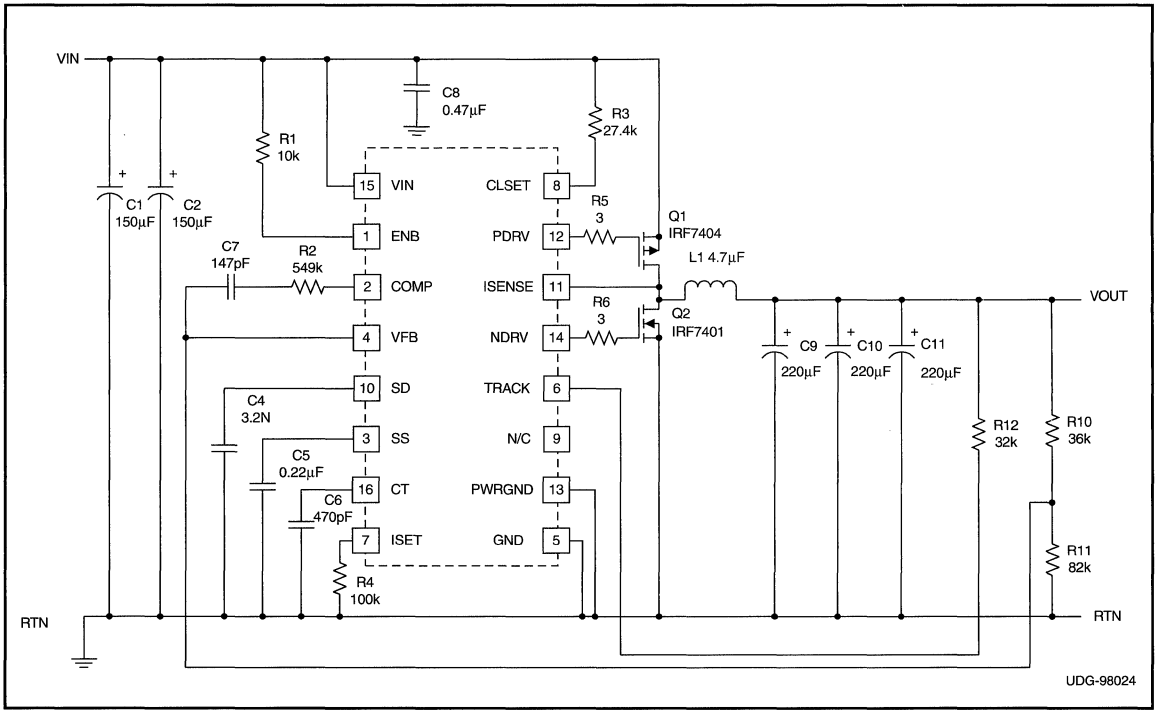


Figure 1. Application circuit schematic.

APPLICATION INFORMATION (cont.)

$$ESR = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{0.018}{0.5} = 0.026\,\Omega$$

A 220µF, 6.3V Sprague 594D capacitor has an ESR of 75mΩ. Three of these in parallel will result in an overall ESR of 25mΩ. (C9, C10, and C11 in Fig. 1). Since the output ripple current is so low, the capacitor's ripple current rating of 1.45A is not a concern.

To check the assumption that the capacitor's impedance at the switching frequency is dominated by the ESR and not the capacitor's capacitance value, calculate the impedance and compare it to the ESR.

$$Zc = \frac{1}{2\pi \bullet Fs \bullet C} = \frac{1}{2\pi \bullet 350k \bullet 220\mu} = 2m\Omega$$

The ESR of the capacitor is 37 times that of the impedance of the capacitor at the switching frequency, so the earlier assumption was valid.

4) Before selecting the switching MOSFETs, the current that will be flowing through them must first be determined.

$$I_{D_{PK}} = I_{OUT} + \frac{\Delta I_{OUT}}{2} = 3.8A$$

The RMS of this current in Q1 is

$$I_D Q1_{RMS} = I_{D_{PK}} \sqrt{\delta} = 2.8A$$

And in Q2

$$I_D Q2_{RMS} = I_{D_{PK}} \sqrt{1-\delta} = 2.5A$$

5) Since this regulator must be able to operate from a 3.3V source, the MOSFETs used must have a gate threshold level of no more than 2V.

For Q1, an IRF7404 is selected. It has an $R_{DS(on)}$ of 0.04Ω, a total gate charge (Q_G1) of 50nC, and a turn OFF ($t_{OFF}1$) time of 65ns. The conduction loss in Q1 will be:

$$P_D Q1_{ON} = I_D Q1_{RMS}{}^2 \bullet R_{DS_{ON}} Q1 = 0.593W$$

The gate drive losses will be

$$P_D Q1_{GATE} = Q_{G_1} \bullet V_{IN} \bullet F_S = 58mW$$

And finally the turn OFF losses are estimated

$$P_D Q1_{OFF} = \frac{1}{2} \bullet V_{IN} \bullet I_D Q1_{PK} \bullet T_{OFF1} \bullet F_S = 0.14W$$

The total power loss for Q1 is the sum of these three:

$$P_D Q1_{TOTAL} = 0.5W$$

6) Q2 has been selected to be an IRF7401, which has an $R_{DS(ON)}$ of 0.03Ω, and a total gate charge (Q_G2) of 48nC and a body diode turn OFF switching time ($t_{OFF}2$) of 59ns. In this topology, the N Channel MOSFET, Q2, is turned OFF prior to the turn ON of Q1, so when Q2 is turned OFF, current is being re-routed from the channel of the device into the intrinsic body diode. Therefore Q2's intrinsic body diode incurs switching loss during the turn OFF interval.

The conduction loss in Q2 is:

$$P_D Q2_{ON} = I_D Q2_{RMS}{}^2 \bullet R_{DS_{ON}} Q2 = 0.2W$$

The gate drive losses will be

$$P_D Q2_{GATE} = Q_{G_2} \bullet V_{IN} \bullet F_S = 55mW$$

And the body diode turn OFF loss:

$$P_D Q2_{D\_OFF} = \frac{1}{2} \bullet V_{IN} \bullet I_{D_{PK}} \bullet T_{OFF2} \bullet F_S = 0.13W$$

The total power loss for Q2 is the sum of these three:

$$P_D Q2_{TOTAL} = 0.4W$$

7) Thus far the power loss in the two MOSFETs and the output inductor total 1.0W. The average input current is:

$$I_{IN_{AVG}} = \frac{V_{OUT} \bullet I_{OUT} + P_{LOSS}}{V_{IN}} = 2.2A$$

The peak to peak ripple in the input capacitors is the peak current less the average input current during Q1's ON time, and equal to the average input current during Q1's OFF time. The RMS value of this current is then:

$$I_{IN\_CAP_{RMS}} = \sqrt{(I_{D_{PK}} - I_{IN_{AVG}})^2 \bullet \delta + (I_{IN_{AVG}})^2 \bullet (1-\delta)} = 1.9A$$

8) After the input capacitor's input ripple current is known, select the input capacitors. Again, Sprague 594D Solid Tantalum capacitors are chosen. A single 150µF, 10V capacitor has a ripple current rating of 1.35A RMS. Two in parallel (C1 and C2) will have a combined capability of 2.7A, and a total ESR of 40mΩ. The losses in the capacitors are:

$$P_{DIN\_CAP} = I_{IN\_CAP_{RMS}}{}^2 \bullet ESR = 0.14W$$

Adding the capacitor loss to that previously found, the total losses are now 2.1W.

9) The overall efficiency of the power train is then

$$E_{FF} = \frac{V_{OUT} \bullet I_{OUT}}{V_{OUT} \bullet I_{OUT} + 2.1} = 0.84$$

APPLICATION INFORMATION (cont.)

The losses are dominated by the MOSFETs Q1 and Q2. One way to improve the efficiency would be to reduce the conduction loss in Q1, either by choosing a device with a lower $R_{DS(on)}$ or by paralleling it with another MOSFET. The conduction losses in Q2 may be improved by the same technique, but will prove detrimental in switching losses. To lower the switching losses, Q2 may be paralleled with a Schottky diode. In this manner, the switching loss may be absorbed by the Schottky, instead of the MOSFET.

10) After the power stage design is completed, attention is given to the feedback loop. The LC filter gain is described by the equation (10A) below: (where $\omega = j2\pi f$)

Where C_{OUT} is the combined capacitance of C9, C10, and C11 and R_{ESR} is the ESR of the capacitors.

There will be a double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L1 \bullet C_{OUT}}} = 2.8\,kHz$$

and a zero at the point where the impedance of the output capacitors equals the ESR:

$$F_Z = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} = 9.6\,kHz$$

The modulator gain is given by

$$K_{PWM} = \frac{V_{IN}}{V_{RAMP}} = 1.65$$

where V_{RAMP} is the peak to peak amplitude of the oscillator ramp found on the CT pin. The overall open loop gain is shown in Fig. 2.

11) The voltage divider is next determined to give us the proper output voltage. First select one of the divider resistors R11 = 82k. The other resistor becomes:

$$R10 = R11 \bullet \frac{V_{OUT}}{V_{REF}} - R11 = 36\,k$$

12) The equation for the error amplifier in this configuration is:

$$K_{EA} = \frac{\frac{1}{j2\pi \bullet f \bullet C7} + R2}{R10}$$

For a gain of 5 and a zero at 2kHz

$$R2 = 15 \bullet R10 = 180\,k$$

and

$$C7 = \frac{1}{2\pi \bullet fp \bullet R2} = 440\,pF$$

The overall voltage loop gain now has a crossover at 34kHz with a phase margin of about 73 degrees.

13) Select the R_{ISET} resistor, R3, to be 100k. (The range of value should be between 90k and 110k.) Then choosing the current limit trip point to be 130% of I_{OUT}, the current limit set resistor is then found by the relationship

$$R3 = \frac{1.3 \bullet I_{OUT}}{1.25} \bullet R_{DS(on)}Q1 \bullet R_{ISET} = 27.2k$$

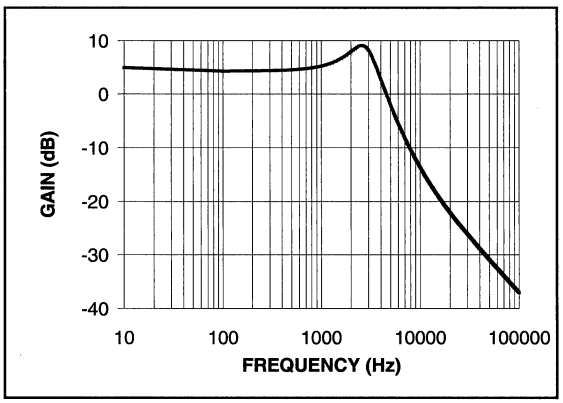


Figure 2. Modulator and filter frequency response.

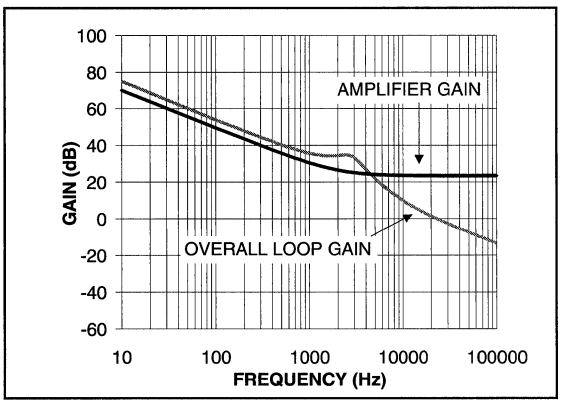


Figure 3. Error amp and closed loop frequency response.

$$(10A)\quad KLC = \frac{1 + \omega \bullet R_{ESR} \bullet C_{OUT}}{1 + \omega^2 \bullet L1 \bullet C_{OUT} + \omega\left(R_{L1} \bullet C_{OUT} + R_{ESR} \bullet C_{OUT} + \frac{L1}{R_{LOAD}}\right)}$$

APPLICATION INFORMATION (cont.)

Note that the $R_{DS(on)}$ value used should include the effects of temperature.

14) During normal power on of the UCC3585, the gate of Q1 is held low (Q1 turned ON) until the V_{CC} input to the IC reaches the 2V Under Voltage Lockout (UVLO) voltage. At UVLO, the UCC3585 wakes up and switching begins on Q1 and Q2. With a 1.8V output however, the output will reach 2V before regulation begins! This is where the tracking function comes into use. By selecting an appropriate resistive divider from the output, we can select the point below UVLO at which Q1 will be shut off. Upon reaching UVLO, the UCC3585 will then begin to regulate normally.

With a 1.8V nominal output voltage, select the tracking turn off point to be 1.6V.

$$R3 = \frac{1.6 - 1.25}{12\mu} = 29k\,\Omega$$

Note that the tracking function ONLY makes a difference below UVLO. If V_{OUT} were to be 2V or above, then the tracking pin should be tied to V_{IN}.

15) A capacitor on the SD pin will allow the converter to shutdown in the event seven consecutive over current pulses occur. If a timing shutdown interval of 1ms is chosen as the shutdown time, T_{SD}, then the value of the capacitor is:

$$C4 = \frac{T_{SD}}{(V_{IN} - 0.5) \bullet \left(\frac{1}{I_{CHG}} + \frac{1}{I_{DICHG}} \right)} = 3.2nF$$

Where I_{CHG} and I_{DISCHG} are 100µA and 10µA respectfully.

16) The next step is to find the value of timing capacitor.

$$C6 = \frac{T_S}{6000} = 476pF$$

A 470pF capacitor will result in a switching frequency of 354kHz.

17) The softstart capacitor is selected for a 5ms startup time. Knowing that a 10µA current source will charge the capacitor to 2.5V, the softstart capacitor is given by:

$$C5 = \frac{T_{SS} \bullet I_{CHG}}{V_{SS}} = \frac{5m \bullet 10\mu}{2.5} = 20nF$$

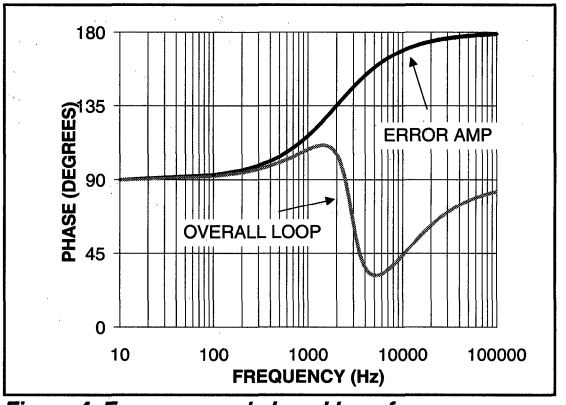


Figure 4. Error amp and closed loop frequency response.

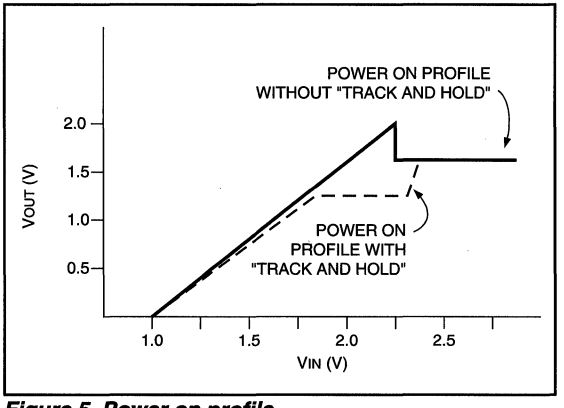


Figure 5. Power on profile.

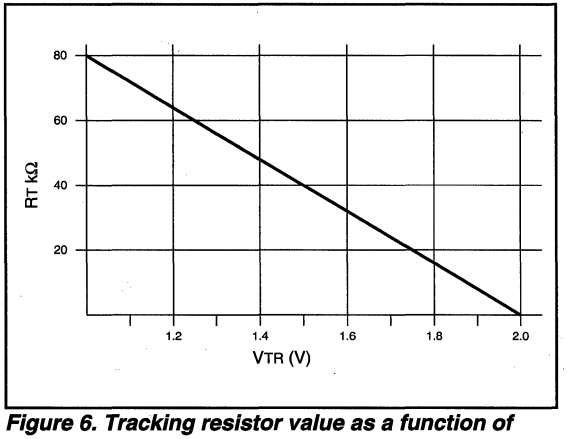


Figure 6. Tracking resistor value as a function of turn off voltage.

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- Power Good OV / UV / OVP Voltage Monitor
- Undervoltage Lockout and Softstart Functions
- Short Circuit Protection
- Low Impedance MOSFET Drivers
- Chip Disable

DESCRIPTION

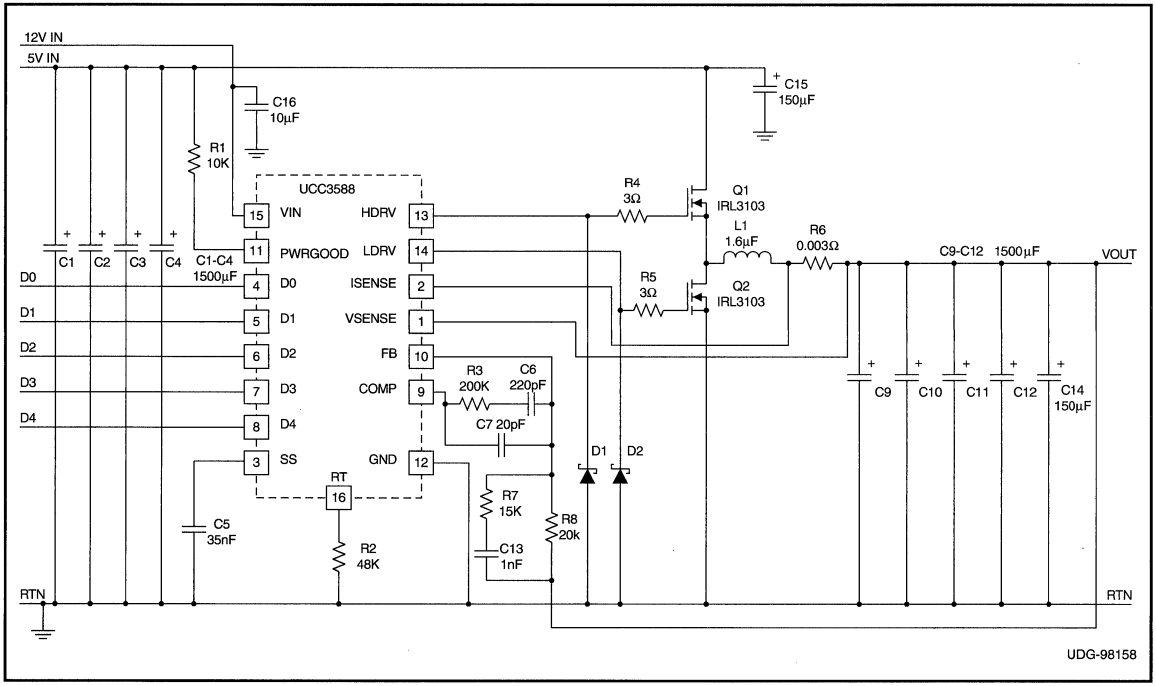
The UCC1588 synchronous step-down (Buck) regulator provides accurate high efficiency power conversion. Using few external components, the UCC1588 converts 5V to an adjustable output ranging from 3.5VDC to 2.1VDC in 100mV steps and 2.05VDC to 1.8VDC in 50mV steps (1.75VDC to 1.3VDC in 50mV steps, –1 only) with 1% DC system accuracy. A high level of integration and novel design allow this 16-pin controller to provide a complete control solution for todays demanding microcontroller power requirements. Typical applications include on board or VRM based power conversion for Intel Pentium II™ microprocessors, as well as other processors from a variety of manufacturers. High efficiency is obtained through the use of synchronous rectification.

The softstart function provides a controlled ramp up of the system output voltage. Overcurrent circuitry detects a hard (or soft) short on the system output voltage and invokes a timed softstart/shutdown cycle to reduce the PWM controller on time to 5%.

The oscillator frequency is externally programmed with RT and operates over a range of 50kHz to 800kHz. The gate drivers are low impedance totem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated by fixed delay times between turn off and turn on of the external high side and synchronous MOSFETs. The chip includes undervoltage lockout circuitry which assures the correct logic states at the outputs during power up and power down.

APPLICATION DIAGRAM

(continued)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 15V
Gate Drive Current, 50% Duty Cycle 1A
Input Voltage, V_{SENSE}, V_{FB}, SS, COMMAND, COMP 5V
Input Voltage, D0, D1, D2, D3, D4 ..... 6V
Input Current, RT, COMP 5mA

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

THERMAL DATA

Plastic DIP Package
Thermal Resistance Junction to Leads, θjc ..... 45°C/W
Thermal Resistance Junction to Ambient, θja ..... 90°C/W
Ceramic DIP Package
Thermal Resistance Junction to Leads, θjc ..... 28°C/W
Thermal Resistance Junction to Ambient, θja ..... 120°C/W
Standard Surface Mount Package
Thermal Resistance Junction to Leads, θjc ..... 35°C/W
Thermal Resistance Junction to Ambient, θja ..... 120°C/W

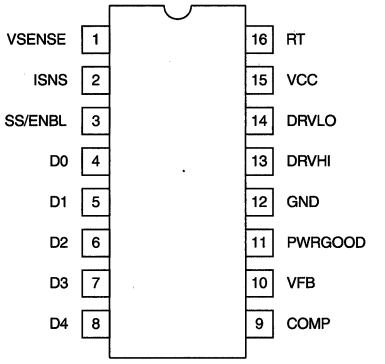
Note: *The above numbers for θja and θjc are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device and PC-board system. All of the above numbers assume no ambient airflow, see the packaging section of Unitrode Product Data Handbook for more details.*

DESCRIPTION (cont.)

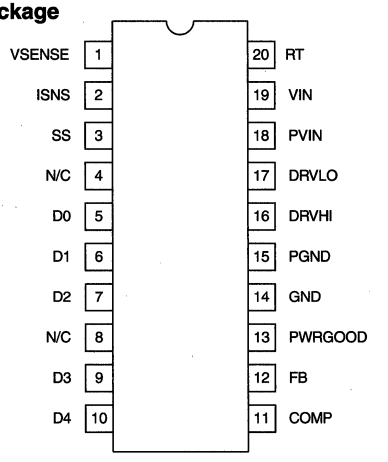
This device is available in 16- pin surface mount, plastic and ceramic DIP, TSSOP packages, and 20 pin surface mount. The UCC1588 is specified for operation from –55°C to +125°C, the UCC2588 is specified for operation from –25°C to +85°C, and the UCC3588 is specified for operation from 0°C to +70°C.

CONNECTION DIAGRAMS

DIP-16, SOIC-16, TSSOP-16 (TOP VIEW)
N, J, D and PW Packages



SOIC-20 (TOP VIEW)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A = T_J$. V_{CC} = 12V, RT = 49k.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, On	V_{CC} = 12V		4.5		mA
UVLO Section					
VCC UVLO Turn-On Threshold			10.5	10.80	V
UVLO Threshold Hysteresis			500		mV
Voltage Error Amplifier Section					
Input Bias Current	V_{CM} = 2.0V		–0.02	0	µA
Open Loop Gain	0.6 < V_{COMP} < 2.5		90		dB
Output Voltage High	I_{COMP} = –500µA		3.4		V
Output Voltage Low	I_{COMP} = +500µA		0.2	0.5	V
Output Source Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–500		µA
Output Sink Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V		10		mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A = T_J$. V_{CC} = 12V, RT = 49k.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator/PWM Section					
Initial Accuracy	T_A = 25°C	240	300	360	kHz
	0°C < T_A < 70°C	220	300	380	kHz
	–25°C < T_A < 85°C	210	300	390	kHz
	–55°C < T_A < 150°C	200	300	400	kHz
Voltage Stability	V_{CC} = 10.8V to 13.2V		1		%
Ramp Amplitude (p–p)			1.85		V
Ramp Valley Voltage			0.65		V
PWM Max Duty Cycle	COMP = 3V		95		%
PWM Min Duty Cycle	COMP = 0. 3V		0		%
PWM Delay to Outputs (High to Low)	COMP = 1.5V		150		ns
PWM Delay to Outputs (Low to High)	COMP = 1.5V		150		ns
Transient Window Comparator Section					
Detection Range High (Duty Cycle = 0)	% Over $V_{COMMAND}$, (Note 1)	1	3	5	%
Detection Range Low (Duty Cycle = 1)	% Under $V_{COMMAND}$, (Note 1)	–1	–3	–5	%
Propogation Delay (V_{SENSE} to Outputs)			150		nS
Soft Start/ Shutdown Section					
SS Charge Current (Normal Start Up)	Measured on SS		–10		µA
SS Charge Current (Short Circuit Fault Condition)	Measured on SS		–100		µA
SS Discharge Current (During Timeout Sequence)	Measured on SS		2.5		µA
Shutdown Threshold	Measured on SS		4.2		V
Restart Threshold	Measured on SS	0.4	0.5		V
Soft Start Complete Threshold (Normal Start-Up)	Measured on SS		3.7		V
DAC / Reference Section					
COMMAND Voltage Accuracy	10.8V < V_{IN} < 13.2V, measured on COMP, 0°C < T_A < +70°C, (Note 2)	–1.00		1.00	%
	10.8V < V_{IN} < 13.2V, measured on COMP, –25°C < T_A < +85°C, (Note 2)	–1.10		1.10	%
D0–D4 Voltage High			6		V
D0–D4 Voltage Threshold			3		V
D0–D4 Voltage Input Bias Current	V(D4,...,D0) < 0.5V		–90	–20	µA
Overvoltage Comparator Section					
Trip Point	% Over $V_{COMMAND}$, (Note 1)	5.00	8.60	12.00	%
Hysteresis		10	20	30	mV
Undervoltage Comparator Section					
Trip Point	% Under $V_{COMMAND}$, (Note 1)	–12.00	–8.60	–5.00	%
Hysteresis		10	20	30	mV
PWRGOOD Signal Section					
Output Impedance	V_{IN} = 12V, $I_{PWRGOOD}$ = 1mA			470	Ω
Overvoltage Protection Section					
Trip Point	% Over $V_{COMMAND}$, (Note 1)	10	17.50	25.00	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined		–10		µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3588, –25°C to +85°C for the UCC2588, and –55°C to +125°C for the UCC1588, $T_A = T_J$. V_{CC} = 12V, RT = 49k.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Drivers (DRVHI, DRVLO) Section					
Output High Voltage	I_{GATE} = 100mA, V_{IN} = 12V		11.5		V
Output Low Voltage	I_{GATE} =– 100mA, V_{IN} = 12V		0.5		V
Driver Non-overlap Time (DRVHI– to DRVLO+)	(Note 3)		100		nS
Driver Non-overlap Time (DRVLO– to DRVHI+)	(Note 3)		50		nS
Driver Rise Time (3nF Capacitive Load)			80		nS
Driver Fall Time (3nF Capacitive Load)			80		nS
Current Limit Section					
Current Limit Detect to Softstart Quick Charge	$V_{ISNS} = V_{SENSE}$ + 75mV		170		nS
Start of Quick Charge to Shutdown Threshold	$V_{ISNS} = V_{SENSE}$ + 75mV, C_{SS} = 10nF, (Note 4)		1.6		µS
Current Limit Threshold Voltage	$V_{THRESHOLD} = V_{ISNS} - V_{VSENSE}$	50	54	58	mV
ISNS Input Bias Current			–10		µA

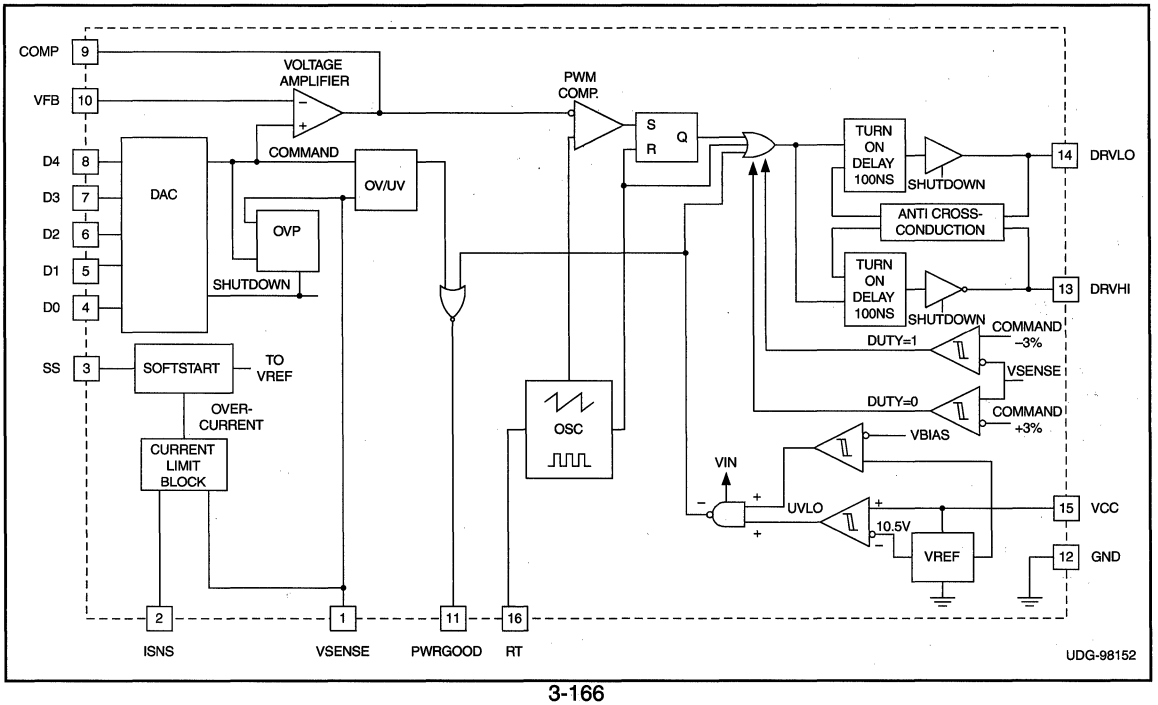
Note 1: *This percentage is measured with respect to the ideal command voltage programmed by the V_{ID} (D0 to D4) pins and applies to all DAC codes from 1.8 to 3.5V.*

Note 2: *Reference and error amplifier offset trimmed while the voltage amp is set in unity gain mode.*

Note 3: *Deadtime delay is measured from the 50% point of DRVHI falling to the 50% point of DRVLO rising, and vice-verse.*

Note 4: *This time is dependent on the value of C_{SS}.*

BLOCK DIAGRAM



PIN DESCRIPTION

COMP: (Voltage Amplifier Output) The system voltage compensation network is applied between COMP and VFB.

D0, D1, D2, D3, D4: These are the digital input control codes for the DAC. The DAC is comprised of two ranges set by D4, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected the pin to GND; a bit is set high by floating the pin. Each control pin is pulled up to approximately 6V by an internal pull-up. If one of the low voltage codes is commanded on the DAC inputs, the outputs will be disabled. The outputs will also be disabled for all 1's, the NO CPU command.

DRVHI: (PWM Output, MOSFET Driver) This output provides a low Impedance totem pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVHI from ringing below GND. DRVHI is disabled during UVLO conditions. DRVHI has a typical output impedance of 5Ω for a V_{IN} voltage of 12V.

DRVLO: (synchronous rectifier output, MOSFET driver) This output provides a low Impedance totem pole driver to drive the low-side synchronous external MOSFET. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot. Minimize circuit trace length to prevent DRVLO from ringing below GND. DRVLO is disabled during UVLO conditions. DRVLO has a typical output impedance of 5Ω for a V_{IN} voltage of 12V. Please see the "Typical Curves" section to determine the driver output impedance as a function of V_{IN} Voltage.

GND: (Ground) All voltages measured with respect to ground. Vcc should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing to GND should be as short and direct as possible.

ISNS: (Current Limit Sense Input) A resistance connected between this sense connection and Vsense sets up the current limit threshold (54mV typical voltage threshold).

PWRGOOD: This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 8.5%(typ). The on resistance of the open-drain switch is no higher than 470Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1mA or less.

RT: (Oscillator Charging Current) This pin is a low impedance voltage source set at ~1.25V. A resistor from RT to GND is used to program the internal PWM oscillator frequency. The equation for R_T follows:

$$R_T = \left(\frac{1}{(f \bullet 67.2pF)}\right) - 800 \qquad (1)$$

SS/SD: (Soft Start/Shut Down) A low leakage capacitor connected between SS and GND will provide a softstart function for the converter. The voltage on this capacitor will slowly charge on start-up via an internal current source (10µA typ.) and ultimately clamp at approximately 3.7V. The output of the voltage error amplifier (COMP) tracks this voltage thereby limiting the controller duty ratio. If a short circuit is detected, the clamp is released and the cap on SS charges with a 100µA (typ) current source. If the SS voltage exceeds 4.2V, the converter shuts down, and the 100µA current source is switched off. The SS cap will then be discharged with a 2.5µA (typ) current sink. When the voltage on SS falls below 0.5V, a new SS cycle is started. The equation for soft-start time follows:

$$T_{SS} = 3.7\left(\frac{C_{SS}}{10\,\mu A}\right). \qquad (2)$$

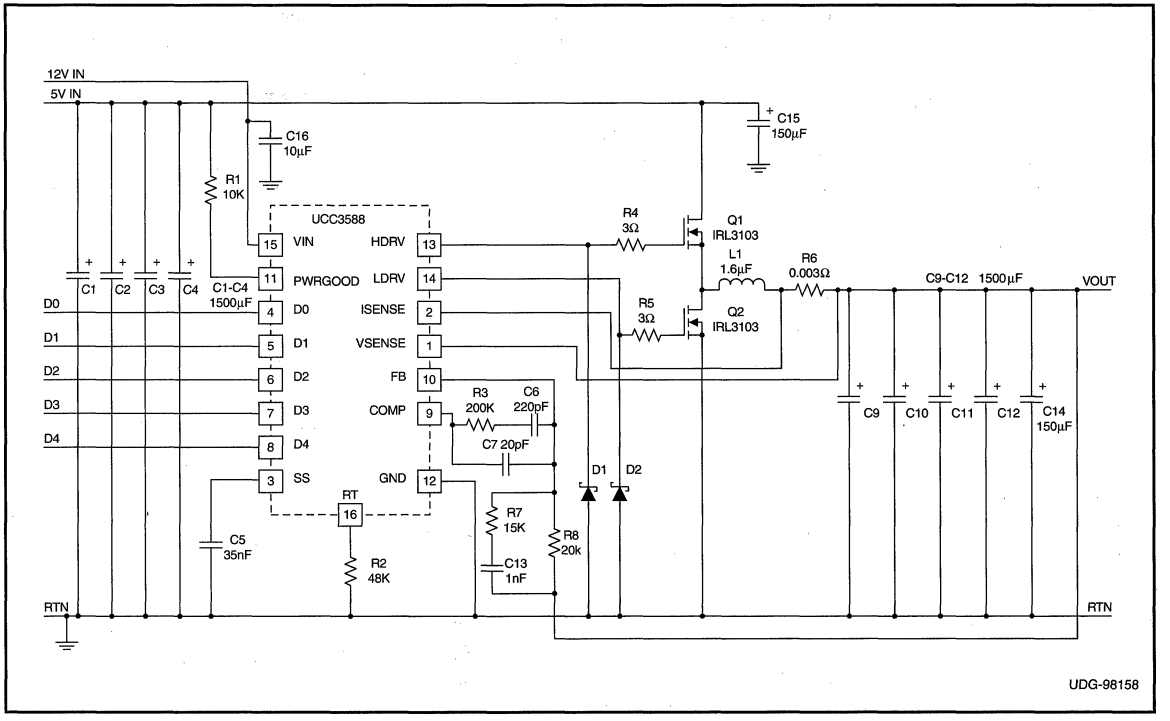
Shutdown is accomplished by pulling SS/SD below 0.5V.

VCC: (Positive Supply Voltage) This pin is normally connected to a 12V ±10% system voltage. The UCC1588 will commence normal operation when the voltage on VCC exceeds 10.5V (typ). Bypass V_{CC} directly to GND with a 0.1µF (minimum) ceramic capacitor to supply current spikes required to charge external MOSFET gate capacitances.

VFB: (Voltage Amplifier Inverting Input) This is normally connected to a compensation network and to the power converter output through a divider network.

VSENSE: (Direct Output Voltage Connection) This pin is a direct kelvin connection to the output voltage used for over voltage, under voltage, and current sensing.

APPLICATION DIAGRAM



APPLICATION INFORMATION

Figure 1 shows a synchronous regulator using the UCC3588. It accepts +5V and +12V as input, and delivers a regulated DC output voltage. The value of the output voltage is programmable via a 5-bit DAC code to a value between 1.8Vand 3.5V. The example given here is for a 12A regulator, running from a 10% tolerance source, and operating at 300kHz.

The design of the power stage is straightforward buck regulator design. Assuming an output noise requirement of 50mV, and an output ripple current of 20% of full load, the value of the output inductor should be calculated at the highest input voltage and lowest output voltage that the regulator is likely to see. This insures that the ripple current will decrease as the input voltage and output voltage differential decreases. The minimum duty cycle, δ_{min}, should also be calculated under this condition.

1) The current sense resistor is chosen to allow current limit to occur at 1.4 times the full load current.

$$R6 = \frac{V_{TRIP}}{(1.4 \bullet I_{OUT})} = \frac{50\,mV}{16.8A} = 3m\Omega \qquad (3)$$

2) To properly approximate the full load duty cycle operating range, assumptions are made regarding the MOSFETs' Rds_{ON}, and the output inductor's DC resistance. Q1 and Q2 are IRF3103s, each with an Rds_{ON} of 0.014Ω. The output inductor is allowed to dissipate one watt under full load, giving a DC resistance of 6.9mΩ, and R6 is 3mΩ. The resulting duty cycle at the operating extremes is then:

$$\delta_{min} = \frac{V_{OUT(lo)} + I_{OUT} \bullet (R6 + Rds_{ON} + R\ell)}{V_{IN(hi)}} \qquad (4)$$

$$= \frac{1.8 + (12 \bullet 0.024)}{5.5} = 0.379$$

$$\delta_{max} = \frac{V_{OUT(hi)} + I_{OUT} \bullet (R6 + Rds_{ON} + R\ell)}{V_{IN(lo)}} \qquad (5)$$

$$= \frac{3.5 + (12 \bullet 0.024)}{4.5} = 0.842$$

3) The value of the output inductor is chosen at the worst case ripple current point.

APPLICATION INFORMATION (cont.)

$$L = \frac{V_{IN(hi)} - V_{OUT(lo)} \bullet \delta_{min} T_S}{\Delta I_{OUT}} = \frac{(5.5 - 1.8) \bullet 0.379 \bullet 3.333\mu}{2.4} = 1.9\mu H \quad (6)$$

Four turns of #16 on a micrometals T51-52C core has an inductance of 1.9µH, has a DC resistance of 6.6mΩ, and will dissipate about 1W under full load conditions. With an output inductor value of 1.9µH, the ripple current will be 1750mA under the low-input-high-output condition.

4) To meet the output noise voltage requirement, the output capacitor(s) must be chosen so that the ripple voltage induced across the ESR of the capacitors by the output ripple current is less than 50mv.

$$ESR < \frac{50\,mV}{\Delta I_{OUT}} = 42\,m\Omega \quad (7)$$

Additionally, to meet output load transient response requirements, the capacitors' ESL and ESR must be low enough to avoid excessive voltage transient spikes. (See Application Note U-157 for a discussion of how to determine the amount and type of load capacitance.) For this example, four Sanyo MV-GX 1500µf, 6.3 V capacitors will be used. The ESR of each capacitor is approximately 44mΩ so the parallel combination of four results in an equivalent ESR of 11mΩ.

5) Q1 and Q2 are chosen to be IRF3103 N-Channel MOSFETs. Each MOSFET has an Rds_{ON} of approximately 0.014Ω, a gate charge requirement of 50nC, and a turn OFF time of approximately 54ns.

To calculate the losses in the upper MOSFET, Q1, first calculate the RMS current it will be conducting.

$$I(Q1_{RMS}) = \sqrt{\delta\left(I_{OUT}^2 + \frac{\Delta I_{OUT}^2}{12}\right)} \quad (8)$$

Notice that with a higher output voltage, the duty cycle increases, and therefore so does the RMS current. Any heat sink design should take into account the worst case power dissipation the device will experience.

With the highest programmable output voltage of 3.5 volts and the lowest possible input voltage of 4.5V, the RMS current Q1 will conduct is 10.5 amps, and the conduction loss is

$$P_{CON}\,Q1 = (I_{Q1RMS})^2 \bullet Rds_{ON} = 1.5W \quad (9)$$

Next, the gate drive losses are found.

$$P_{GATE}\,Q1 = Q_G \bullet V_{IN(hi)} \bullet F_S = 0.08W \quad (10)$$

And the Turn OFF losses are estimated as

$$P_{T(OFF)}Q1 = \tfrac{1}{2} V_{IN(hi)} \bullet I_{D(pk)} \bullet tf \bullet F_S = 0.56W \quad (11)$$

The total loss in Q1is the sum of the three components, or about 2.1 watts.

The gate drive losses in Q2 will be the same as in Q1, but the turn OFF losses will be associated with the reverse recovery of the body diode, instead of the turn OFF of the channel. This is due to the UCC3588's delay built into the switching of the upper and lower MOSFET's drive. For example, when Q1 is turned OFF, the turn ON of Q2 is delayed for about 100ns, insuring that the circuit has time to commutate and that current has begun to flow in the body diode of Q2. When Q2 is turned OFF, current is diverted from the channel of Q2 into the body diode of Q2, resulting in virtually no power dissipation. When Q1 is turned ON 100ns later however, the circuit is forced to commutate again. This time causing reverse recovery loss in the body diode of Q2 as its polarity is reversed. The loss in the diode is expressed as:

$$P_{RR}Q2 = \tfrac{1}{2} \bullet Q_{RR} \bullet V_{IN(hi)} \bullet F_S = 0.26W \quad (12)$$

Where Q_{RR}, the reverse recovery of the body diode, is 310nC.

100ns before the turn ON of Q2, and 100ns after the turn OFF of Q2, current flows through Q2's intrinsic body diode. The power dissipation during this interval is:

$$P_{COM}Q2_{DIODE} = I_{OUT} \bullet V_{DIODE} \bullet \frac{200\,ns}{3.33\mu s} = 12 \bullet 1.4 \bullet 0.06 = 1W \quad (13)$$

During the ON period of Q2, current flows through the Rds_{ON} of the device. Where the highest RMS current in Q1 was at the low-input-and-high-output condition, the highest RMS current in Q2 is found when the input is at its highest, and the output is at its lowest. The equation for the RMS current in Q2 is:

$$I(Q2_{RMS}) = \sqrt{\left(1 - \delta_{min} - \frac{200\,ns}{3.33\mu s}\right) \bullet \left(I_{OUT}^2 + \frac{\Delta I_{OUT}^2}{12}\right)} = 8.7A \quad (14)$$

$$P_{CON}Q2 = I\left(Q2_{RMS}^2\right) \bullet Rds_{ON} = 1.06W \quad (15)$$

The worst case loss in Q2 comes to about 2.4 watts.

6) Repeating the preceding procedure for various input and output voltage combinations yields a table of operating conditions.

APPLICATION INFORMATION (cont.)

Table 1. Regulator Operating Conditions

	V_{IN}= 4.5	5.0	5.5
V_{OUT}=3.5			
Pd Q1	2.2	2.1	2
Pd Q2	1.5	1.6	1.8
Pd L	0.95	0.95	0.95
Pd Total	5.1	5.2	5.4
Average Input	10.50	9.5	8.70
Duty Cycle	0.84	0.76	0.69
V_{OUT}=1.8			
Pd Q1	1.5	1.4	1.4
Pd Q2	2.3	2.4	2.5
Pd L	0.95	0.95	0.95
Pd Total	5.2	5.3	5.4
Average Input	6.00	5.40	4.96
Duty Cycle	0.46	0.42	0.38

7) Assuming the converter's input current is DC, the remaining switching current drawn by Q1 must come from the input capacitors. The next step then, is to find the worst case RMS current the capacitors will experience. (Equation 16). Where I_{IN}(avg) is the average input current.

Repeating the above calculation over the operating range of the regulator (see Table 2.) reveals that the worst case capacitor ripple current is found at low input, and at low output voltage. A Sanyo MV-GX, 1500µF, 6.3V capacitor is rated to handle 1.25 amps at 105°C. Derating the design to 70°C allows the use of four capacitors, each one experiencing one fourth of the total ripple current.

Table 2. Regulator Operating Conditions

	V_{IN}= 4.5	5.0	5.5
V_{OUT}= 3.5			
Total Input Cap RMS Current	4.4	5.2	5.6
Total Input Cap Power Dissipation	0.21	0.29	0.34
Total Power Dissipation	5.1	5.3	5.4
Power Train Efficiency	0.89	0.88	0.87
V_{OUT}=1.8			
Total Input Cap RMS Current	6	5.9	5.8
Total Input Cap Power Dissipation	0.39	0.39	0.37
Total Power Dissipation	5.2	5.3	5.4
Power Train Efficiency	0.81	0.8	0.8

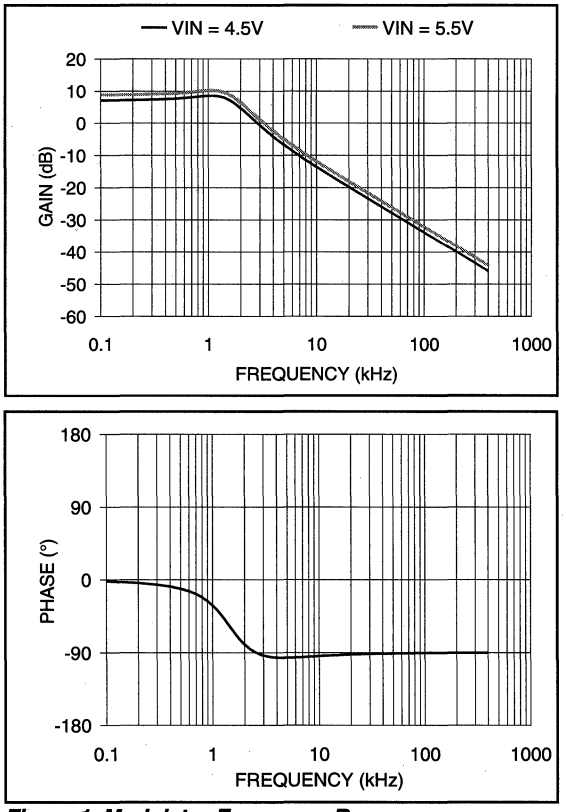


Figure 1. Modulator Frequency Response

8) The voltage feedback loop is next. The gain and frequency response of the PWM and LC filter is shown in Equation 17.

To compensate the loop with as high a bandwidth as practical, additional gain is added to the loop with the voltage error amplifier.

$$I_{CAP_{RMS}} = \sqrt{\delta\left((I_{OUT} - I_{IN\,avg})^2 + \frac{\Delta I_{OUT}{}^2}{12}\right) + (1-\delta)\bullet(I_{IN\,avg})^2} \quad (16)$$

APPLICATION INFORMATION (cont.)

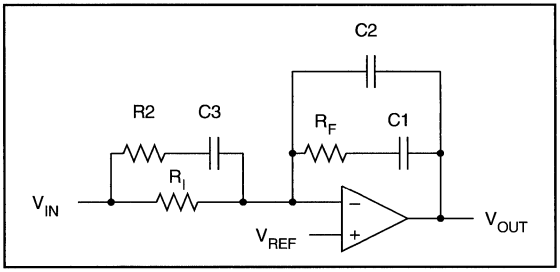


Figure 3. Voltage error amplifier configuration.

The equation for the gain of the voltage amplifier in this configuration is:

$$K_{EA} = \frac{(1+s(C1Rf)) \bullet (1+s(C3(R_I+R2)))}{R_I\left(s^2C1C2Rf + s(C1+C2)\right) \bullet (1+s(C3R2))} \quad (18)$$

For good transient response, select the R_F-C1 zero at 5kHz. Add additional phase margin by placing the R_I-C3 zero also at 5kHz. To roll off the gain at high frequency, selece the R2-C3 pole to be at 10kHz, and the final C2-R_F pole at 40kHz. Results are R_I=20k, R_F=200k, R2=15k, C1=220nf, C2=20pF, C3=1000pf. The Gain-Phase plots of the voltage error amplifier and the overall loop are plotted below.

9) The value of RT is given by:

$$RT = \left(\frac{1}{F_S \bullet 67.2pF}\right) - 800 = 48k\,\Omega \quad (19)$$

10) The value of the soft start capacitor is given by:

$$C_{SS} = 10\mu \bullet \frac{t_{SS}}{3.7V} \quad (20)$$

Where t_{SS} is the desired soft start time.

To insure that soft start is long enough so that the converter does not enter current limit during startup, the minimum value of soft start may be determined by:

$$C_{SS} \geq \frac{C_{OUT} \bullet I_{CH}}{\left(\frac{V_{LIM}}{R_{SENSE}}\right) - I_{OUT}} \bullet \frac{V_{IN}}{V_{RAMP}} \quad (21)$$

Where C_{OUT} is the output capacitance, Ich is the soft start charging current (10µa typ), V_{LIM} is the current limit trip voltage (54mV typ), I_{OUT} is the load current, V_{IN} is the 5V supply, and V_{RAMP} is the internal oscillator ramp voltage (1.85V typ). For this example, C_{SS} must be greater than 35nF, and the resulting soft start time will be 13ms.

11) The output of the regulator is adjustable by programming the following codes into the D0 - D4 pins according to the table below. To program a logic zero, ground the pin. To program a logic 1, then leave the pin floating. Do not tie the pin to an external voltage source.

12) A series resistor should be placed in series with the gate of each MOSFET to prevent excessive ringing due to parasitic effects. A value of 3Ω to 5Ω is usually

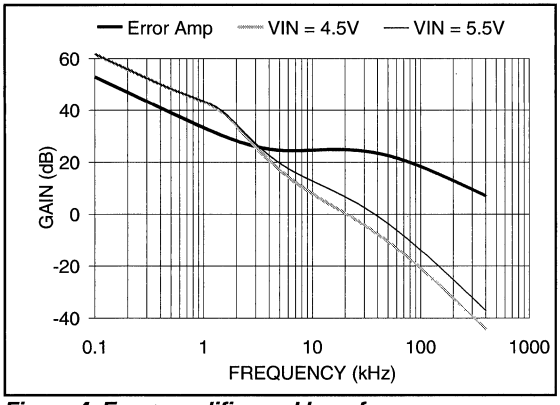


Figure 4. Error amplifier and loop frequency response.

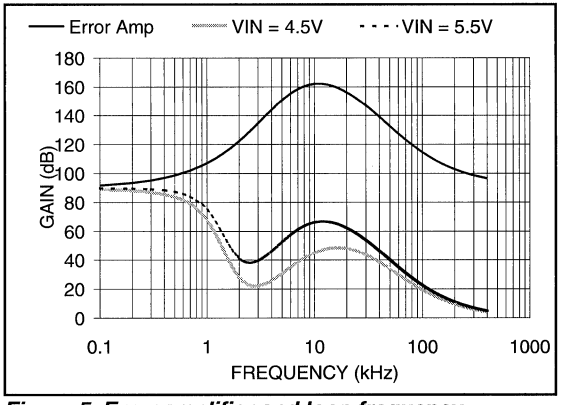


Figure 5. Error amplifier and loop frequency response.

APPLICATION INFORMATION (cont.)

Table 3.
VID Codes and Resulting Regulator Output Voltage

D4	D3	D2	D1	D0	V_{OUT}
For -1 Parts Only					
0	1	1	1	1	1.3
0	1	1	1	0	1.35
0	1	1	0	1	1.4
0	1	1	0	0	1.45
0	1	0	1	1	1.5
0	1	0	1	0	1.55
0	1	0	0	1	1.6
0	1	0	0	0	1.65
0	0	1	1	1	1.7
0	0	1	1	0	1.75
For all parts					
0	0	1	0	1	1.8
0	0	1	0	0	1.85
0	0	0	1	1	1.9
0	0	0	1	0	1.95
0	0	0	0	1	2
0	0	0	0	0	2.05
1	1	1	1	1	No outputs
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4

sufficient in most cases. Additionally, to prevent pins 13 and 14 from ringing more than 0.5V below ground, a clamp schottky rectifier placed as close as possible to the IC is also recommended.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

application INFO available

UCC1800/1/2/3/4/5
UCC2800/1/2/3/4/5
UCC3800/1/2/3/4/5

Low-Power BiCMOS Current-Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 500µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UC3842 and UC3842A

DESCRIPTION

The UCC1800/1/2/3/4/5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

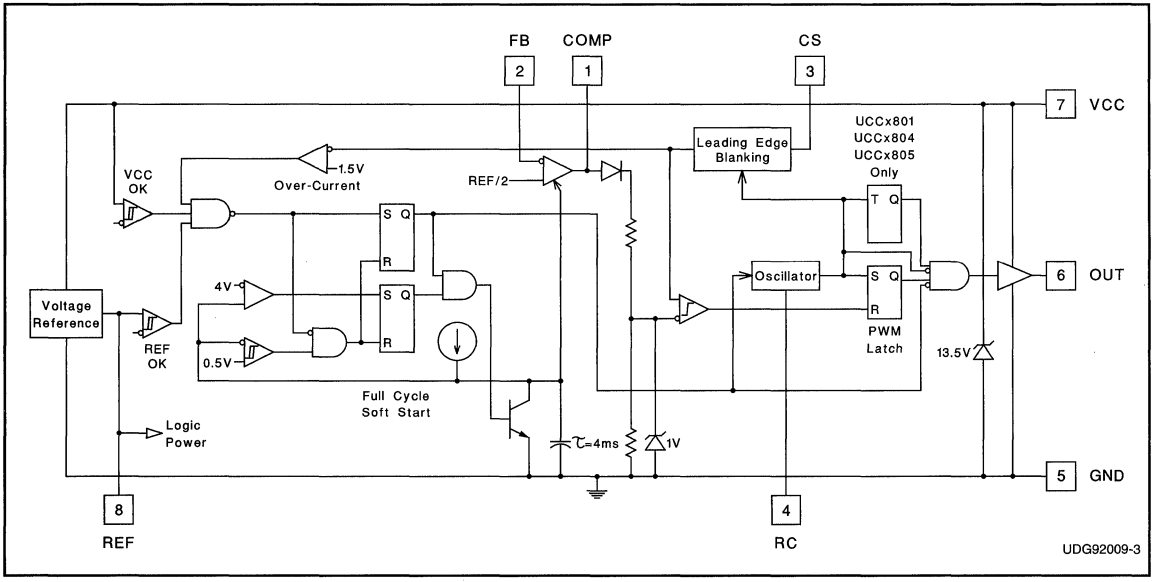
These devices have the same pin configuration as the UC1842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

The UCC1800/1/2/3/4/5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC1803 and UCC1805 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC1802 and UCC1804 make these ideal choices for use in off-line power supplies.

The UCC180x series is specified for operation from –55°C to +125°C, the UCC280x series is specified for operation from –40°C to +85°C, and the UCC380x series is specified for operation from 0°C to +70°C.

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx800	100%	5V	7.2V	6.9V
UCCx801	50%	5V	9.4V	7.4V
UCCx802	100%	5V	12.5V	8.3V
UCCx803	100%	4V	4.1V	3.6V
UCCx804	50%	5V	12.5V	8.3V
UCCx805	50%	4V	4.1V	3.6V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} Voltage (Note 2) 12.0V
V_{CC} Current 30.0mA
OUT Current . . . . . ±1.0A
OUT Energy (Capacitive Load) 20.0µJ
Analog Inputs (FB, CS) . . . . . –0.3V to 6.3V
Power Dissipation at T_A < +25°C (N or J Package) 1.0W
Power Dissipation at T_A < +25°C (D Package) 0.65W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitrode databook for information regarding thermal specifications and limitations of packages.

Note 2: In normal operation V_{CC} is powered through a current limiting resistor. Absolute maximum of 12V applies when V_{CC} is driven from a low impedance source such that I_{CC} does not exceed 30mA.

TEMPERATURE AND PACKAGE SELECTION

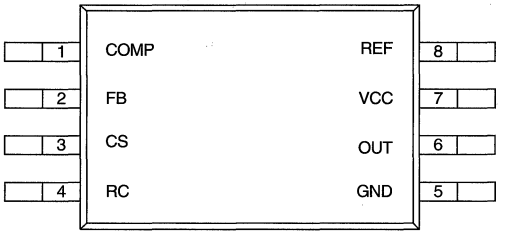
	Temperature Range	Available Packages
UCC1800	–55°C to +125°C	J
UCC2800	–40°C to +85°C	N, D, PW
UCC3800	0°C to +70°C	N, D, PW

ORDERING INFORMATION

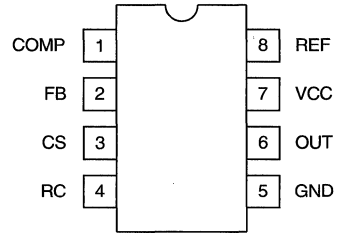
UCC☐80☐☐
- ☐☐ — PACKAGE
- ☐ — PRODUCT OPTION
- ☐ — TEMPERATURE RANGE

CONNECTION DIAGRAMS

TSSOP-8 (Top View)
PW Package



DIL-8, SOIC-8 (Top View)
J or N, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ +125°C for UCC180x; –40°C ≤ T_A ≤ +85°C for UCC280x; 0°C ≤ T_A ≤ +70°C for UCC380x; V_{CC}=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from V_{CC} to GND; 0.1µF capacitor from V_{REF} to GND. T_A=T_J.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J=+25°C, I=0.2mA, UCCx800/1/2/4	4.925	5.00	5.075	4.925	5.00	5.075	V
	T_J=+25°C, I=0.2mA, UCCx803/5	3.94	4.00	4.06	3.94	4.00	4.06	
Load Regulation	0.2mA<I<5mA		10	30		10	25	mV
Total Variation	UCCx800/1/2/4 (Note 7)	4.88	5.00	5.10	4.88	5.00	5.10	V
	UCCx803/5 (Note 7)	3.90	4.00	4.08	3.90	4.00	4.08	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J=+25°C (Note 9)		130			130		µV
Long Term Stability	T_A=+125°C, 1000 Hours (Note 9)		5			5		mV
Output Short Circuit		–5		–35	–5		–35	mA
Oscillator Section								
Oscillator Frequency	UCCx800/1/2/4 (Note 4)	40	46	52	40	46	52	kHz
	UCCx803/5 (Note 4)	26	31	36	26	31	36	kHz
Temperature Stability	(Note 9)		2.5			2.5		%
Amplitude peak-to-peak		2.25	2.40	2.55	2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45			2.45		V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $-55°C \le T_A \le +125°C$ for UCC180x; $-40°C \le T_A \le +85°C$ for UCC280x; $0°C \le T_A \le +70°C$ for UCC380x; V_{CC}=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from V_{CC} to GND; 0.1µF capacitor from V_{REF} to GND. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
Error Amplifier Section								
Input Voltage	COMP=2.5V; UCCx800/1/2/4	2.44	2.50	2.56	2.44	2.50	2.56	V
	COMP=2.0V; UCCx803/5	1.95	2.0	2.05	1.95	2.0	2.05	
Input Bias Current		–1		1	–1		1	µA
Open Loop Voltage Gain		60	80		60	80		dB
COMP Sink Current	FB=2.7V, COMP=1.1V	0.3		3.5	0.4		2.5	mA
COMP Source Current	FB=1.8V, COMP=REF–1.2V	–0.2	–0.5	–0.8	–0.2	–0.5	–0.8	mA
Gain Bandwidth Product	(Note 9)		2			2		MHz
PWM Section								
Maximum Duty Cycle	UCCx800/2/3	97	99	100	97	99	100	%
	UCCx801/4/5	48	49	50	48	49	50	
Minimum Duty Cycle	COMP=0V			0			0	%
Current Sense Section								
Gain	(Note 5)	1.10	1.65	1.80	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP=5V (Note 6)	0.9	1.0	1.1	0.9	1.0	1.1	V
Input Bias Current		–200		200	–200		200	nA
CS Blank Time		50	100	150	50	100	150	ns
Over-Current Threshold		1.42	1.55	1.68	1.42	1.55	1.68	V
COMP to CS Offset	CS=0V	0.45	0.90	1.35	0.45	0.90	1.35	V
Output Section								
OUT Low Level	I=20mA, all parts		0.1	0.4		0.1	0.4	V
	I=200mA, all parts		0.35	0.90		0.35	0.90	V
	I=50mA, VCC=5V, UCCx803/5		0.15	0.40		0.15	0.40	V
	I=20mA, VCC=0V, all parts		0.7	1.2		0.7	1.2	V
OUT High V_{SAT} (V_{CC}-OUT)	I=–20mA, all parts		0.15	0.40		0.15	0.40	V
	I=–200mA, all parts		1.0	1.9		1.0	1.9	V
	I=–50mA,VCC=5V, UCCx803/5		0.4	0.9		0.4	0.9	V
Rise Time	C_L=1nF		41	70		41	70	ns
Fall Time	C_L=1nF		44	75		44	75	ns
Undervoltage Lockout Section								
Start Threshold (Note 8)	UCCx800	6.6	7.2	7.8	6.6	7.2	7.8	V
	UCCx801	8.6	9.4	10.2	8.6	9.4	10.2	V
	UCCx802/4	11.5	12.5	13.5	11.5	12.5	13.5	V
	UCCx803/5	3.7	4.1	4.5	3.7	4.1	4.5	V
Stop Threshold (Note 8)	UCCx1800	6.3	6.9	7.5	6.3	6.9	7.5	V
	UCCx1801	6.8	7.4	8.0	6.8	7.4	8.0	V
	UCCx802/4	7.6	8.3	9.0	7.6	8.3	9.0	V
	UCCx803/5	3.2	3.6	4.0	3.2	3.6	4.0	V
Start to Stop Hysteresis	UCCx800	0.12	0.3	0.48	0.12	0.3	0.48	V
	UCCx801	1.6	2	2.4	1.6	2	2.4	V
	UCCx802/4	3.5	4.2	5.1	3.5	4.2	5.1	V
	UCCx803/5	0.2	0.5	0.8	0.2	0.5	0.8	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for $-55°C \le T_A \le +125°C$ for UCC180x; $-40°C \le T_A \le +85°C$ for UCC280x; $0°C \le T_A \le +70°C$ for UCC380x; V_{CC}=10V (Note 3); RT=100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from V_{CC} to GND; 0.1µF capacitor from V_{REF} to GND. $T_A=T_J$.

PARAMETER	TEST CONDITIONS	UCC180X UCC280X			UCC380X			UNITS
Soft Start Section								
COMP Rise Time	FB=1.8V, Rise from 0.5V to REF–1V		4	10		4	10	ms
Overall Section								
Start-up Current	V_{CC} < Start Threshold		0.1	0.2		0.1	0.2	mA
Operating Supply Current	FB=0V, CS=0V		0.5	1.0		0.5	1.0	mA
VCC Internal Zener Voltage	I_{CC}=10mA (Note 8)	12	13.5	15	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx802/4	0.5	1.0		0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.
Note 4: Oscillator frequency for the UCCx800, UCCx802 and UCCx803 is the output frequency.
Oscillator frequency for the UCCx801, UCCx804 and UCCx805 is twice the output frequency.
Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.
Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.
Note 7: Total Variation includes temperature stability and load regulation.
Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.
Note 9: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3800 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3800 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

CS: CS is the input to the current sense comparators. The UCC3800 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3800 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ± 750mA. OUT is actively held low when V_{CC} is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to V_{CC}. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

PIN DESCRIPTIONS (cont.)

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

The frequency of oscillation can be estimated with the following equations:

$$\text{UCCx800/1/2/4:}\quad F = \frac{1.5}{R \bullet C}$$

$$\text{UCCx803, UCCx805:}\quad F = \frac{1.0}{R \bullet C}$$

where frequency is in Hz, resistance is in ohms, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

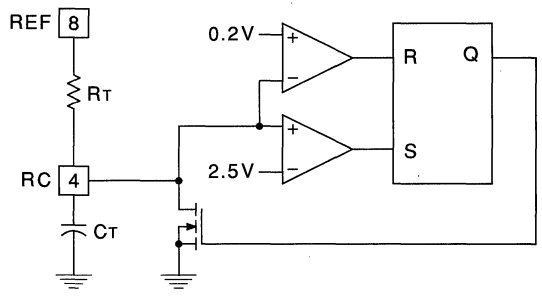
REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When V_{CC} is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5k ohm resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

VCC: V_{CC} is the power input connection for this device. In normal operation V_{CC} is powered through a current limiting resistor. Although quiescent V_{CC} current is very low, total supply current will be higher, depending on OUT current. Total V_{CC} current is the sum of quiescent V_{CC} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \times F.$$



The UCC3800/1/2/3/4/5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of RT and CT. The fall time is set by CT and an internal transistor on-resistance of approximately 125Ω. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

Figure 1. Oscillator.

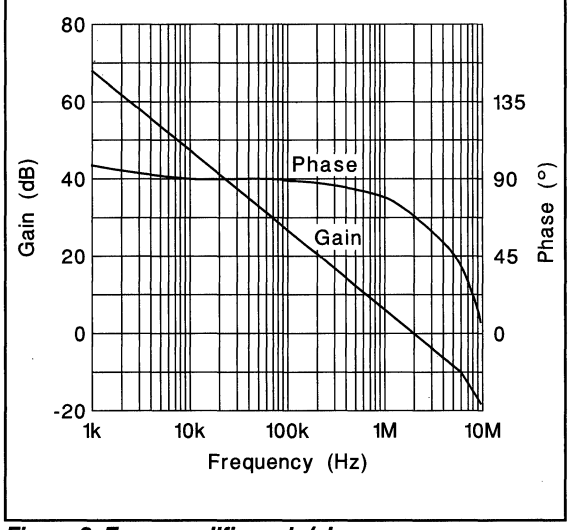


Figure 2. Error amplifier gain/phase response.

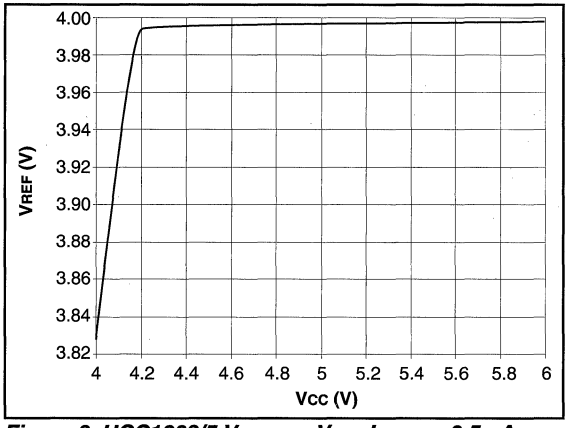


Figure 3. UCC1803/5 V_{REF} vs. V_{CC}; I_{LOAD} = 0.5mA.

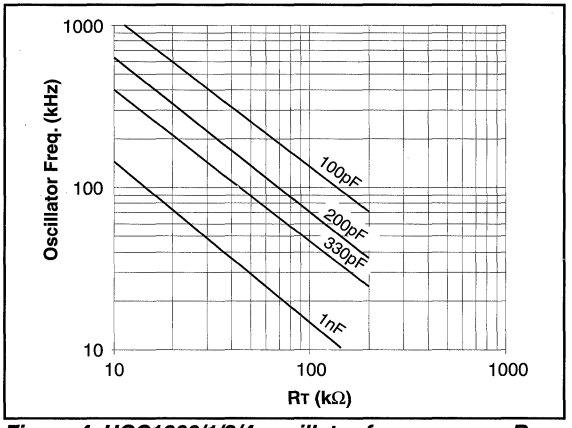


Figure 4. UCC1800/1/2/4 oscillator frequency vs. R_T and C_T.

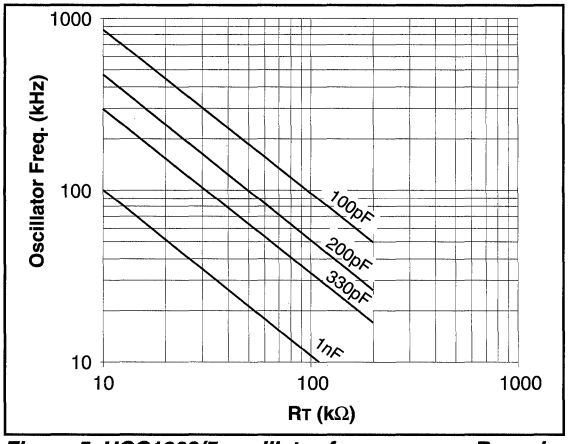


Figure 5. UCC1803/5 oscillator frequency vs. R_T and C_T.

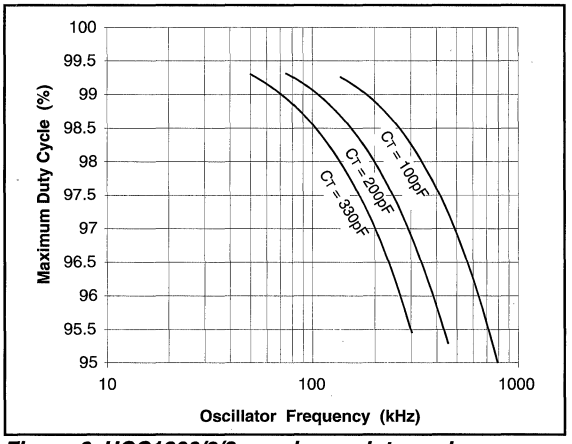


Figure 6. UCC1800/2/3 maximum duty cycle vs. oscillator frequency.

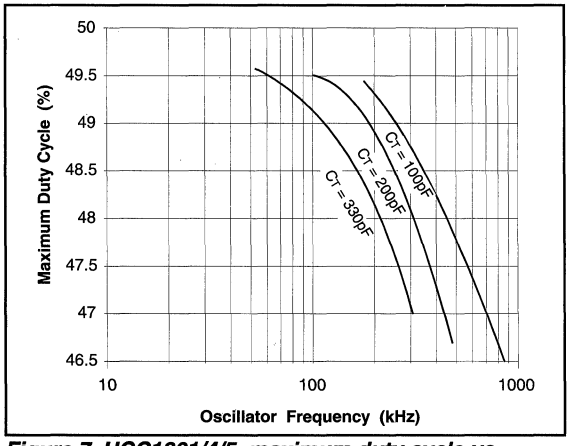


Figure 7. UCC1801/4/5 maximum duty cycle vs. oscillator frequency.

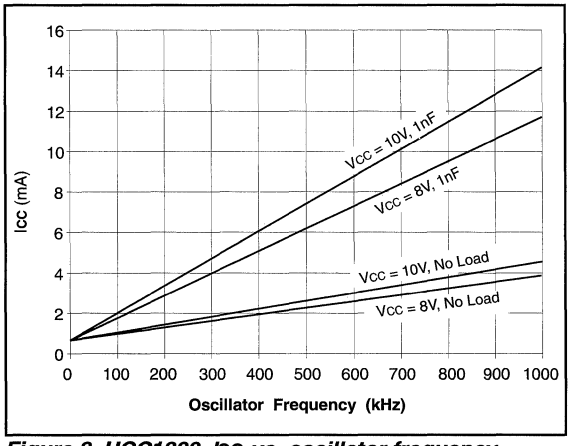


Figure 8. UCC1800 I_{CC} vs. oscillator frequency.

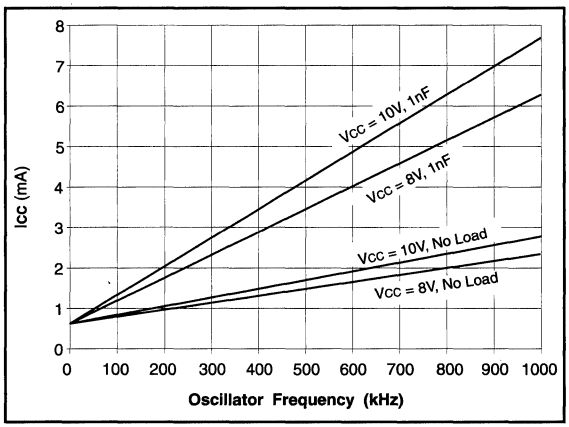


Figure 8. UCC1805 ICC vs. oscillator frequency.

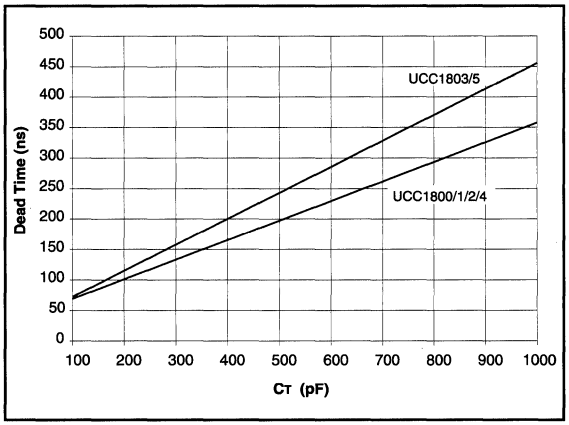


Figure 9. Dead time vs. C_T, R_T = 100k.

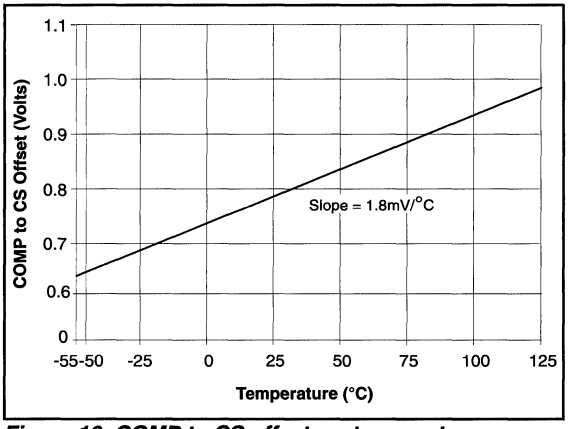


Figure 10. COMP to CS offset vs. temperature, CS = 0V.

UNITRODE

application INFO available

UCC1806
UCC2806
UCC3806

Low Power, Dual Output, Current Mode PWM Controller

FEATURES

- BiCMOS Version of UC1846 Families
- 1.4mA Maximum Operating Current
- 100µA Maximum Startup Current
- 1.0A Peak Output Current
- 125nsec Circuit Delay
- Easier Parallelability
- Improved Benefits of Current Mode Control

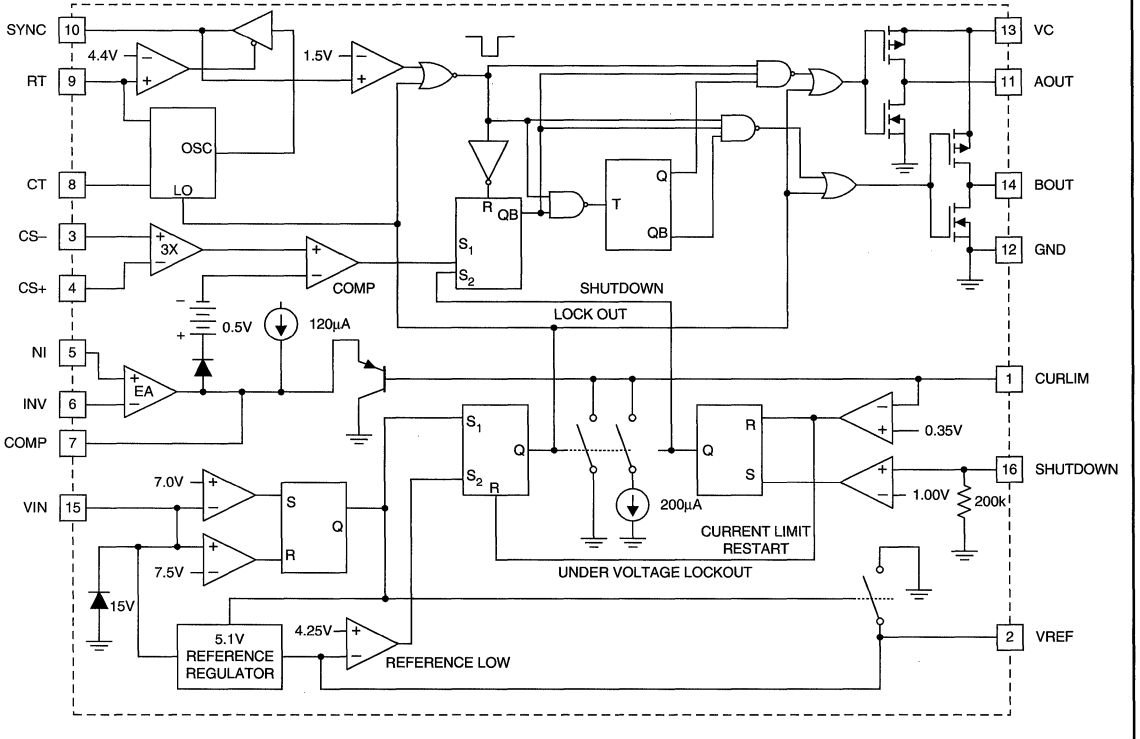
DESCRIPTION

The UCC1806 family of BiCMOS PWM controllers offers exceptionally improved performance with a familiar architecture. With the same block diagram and pinout of the popular UC1846 series, the UCC1806 line features increased switching frequency capability while greatly reducing the bias current used within the device. With a typical startup current of 50µA and a well defined voltage threshold for turn-on, these devices are favored for applications ranging from off-line power supplies to battery operated portable equipment. Dual high current, FET driving outputs and a fast current sense loop further enhance device versatility.

All the benefits of current mode control including simpler loop closing, voltage feed-forward, parallelability with current sharing, pulse-by-pulse current limiting, and push-pull symmetry correction are readily achievable with the UCC1806 series.

(continued)

BLOCK DIAGRAM



Pin numbers refer to DIL-16 package.

UDG-99035

02/99

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, Low Impedance (Pin 15) . . . . . +15V
Supply Current, High Impedance (Pin 15) . . . . . +25mA
Output Supply Voltage (Pin 13) . . . . . +18V
Output Current, Continuous Source or Sink . . . . . ±200mA
Output Current, Gate Drive . . . . . ±500mA
Analog Input Voltage (Pin 3, 4, 5, 6, 16) . . –0.3V to +V_{IN} +0.3V
Sync Output Current (Pin 10) . . . . . ±30mA
Error Amplifier Output Current (Pin 7) . +10mA/– (Self Limiting)
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Storage Temperature Range . . . . . 65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Note 1. All voltages are with respect to Ground, Pin 12.

Note 2. Currents are positive into, negative out of the specified terminal.

Note 3. Consult packaging section of databook for thermal limitations and considerations of package.

Note 4. Pin numbers refer to DIL-16 package.

DESCRIPTION (continued)

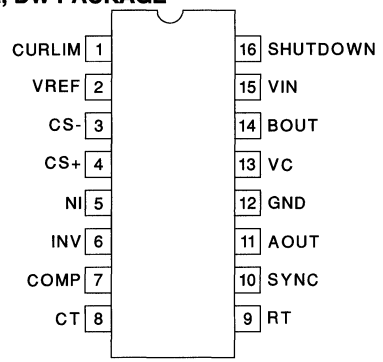
These devices are available with multiple package options for both through-hole and surface mount applications; and in commercial, industrial, and military temperature ranges. Contact factory for availability.

The UCC1806 is specified for operation from –55°C to +125°C, the UCC2806 is specified for operation from –40°C to +85°C, and the UCC3806 is specified for operation from 0°C to +70°C. The part is available in DIP and SOIC packages.

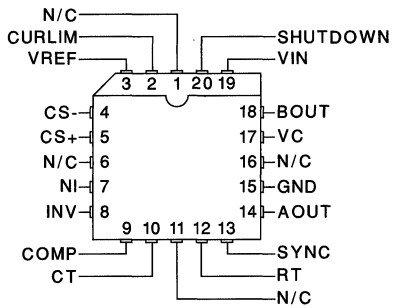
3

CONNECTION DIAGRAMS

DIL-16 (Top View)
J or N, DW PACKAGE



PLCC-20, LCC-20 (Top View)
Q, L PACKAGE



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 0.2mA	5.02	5.10	5.17	5.00	5.10	5.20	V
Load Regulation	0.2mA < I_O < 5mA		3	25		3	25	mV
Temperature Stability	(Note 5)		0.2	0.6		0.2	0.6	mV/°C
Total Output Variation	Line, Load, Temperature (Note 7)	–150		150	–150		150	mV
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note 5)		70			70		µV
Long Term Stability	T_A = 125°C, 1000 Hours (Note 5)		5	25		5	25	mV
Output Short Circuit		–10		–30	–10		–30	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, $T_A = T_J$.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section								
Initial Accuracy	T_J = 25°C	42	47	52	42	47	52	kHz
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 5)		2			2		%
Amplitude			2.35			2.35		V
SYNC Delay to Outputs	Pin 8 = 0V, Pin 9 = V_{REF}, V_{SYNC} = 0.8V to 2.0V		50	125		50	100	ns
Discharge Current	T_J = 25°C, $V_{PIN\ 8}$ = 2.0V		2			2		mA
SYNC, V_{OL}	I_{OUT} = +1mA			0.4			0.4	V
SYNC, V_{OH}	I_{OUT} = –4mA	2.4			2.4			V
SYNC, V_{IL}	Pin 8 = 0V, Pin 9 = V_{REF}			0.8			0.8	V
SYNC, V_{IH}	Pin 8 = 0V, Pin 9 = V_{REF}	2.0			2.0			V
SYNC Input Current		–1		+1	–1		+1	µA
Error Amplifier Section								
Input Offset Voltage				5			10	mV
Input Bias Current				–1			–1	µA
Input Offset Current				500			500	nA
Common Mode Range		0		V_{IN}-2	0		V_{IN}-2	V
Open Loop Gain	V_O = 1.0 to 4.0	80	100		80	100		dB
Unity Gain Bandwidth		1			1			MHz
Output Sink Current	V_{ID} < –20mV, $V_{PIN\ 7}$ = 1.0V	1			1			mA
Output Source Current	V_{ID} < 20mV, $V_{PIN\ 7}$ = 3.0V	–80	–120		–80	–120		µA
Output High Level	V_{ID} = –50mV	4.5			4.5			V
Output Low Level	V_{ID} = –50mV			0.5			0.5	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$ = 0V, $V_{PIN\ 1} = V_{REF}$ (Notes 3,4)	2.75	3	3.35	2.75	3	3.35	V/V
Maximum Differential Input Signal ($V_{PIN\ 4}$ - $V_{PIN\ 3}$)	$V_{PIN\ 1} = V_{REF}$, $V_{PIN\ 5} = V_{REF}$, $V_{PIN\ 6}$ = 0V	1.1			1.1			V
Input Offset Voltage	$V_{PIN\ 1}$ = 0.5V, $V_{PIN\ 7}$ = OPEN		10	30		10	50	mV
CMRR	V_{CM} = 0 to V_{IN} – 3.5	60			60			dB
PSRR		56			56			dB
Input Bias Current	$V_{PIN\ 1}$ = 0.5V, PIN 7 OPEN (Note 3)			–1			–1	µA
Input Offset Current	$V_{PIN\ 1}$ = 0.5V, PIN 7 OPEN (Note 3)			1			1	µA
Delay to Outputs	$V_{PIN\ 5} = V_{REF}$, PIN 6 = 0, PIN 1 = 2.75V, PIN 4 – PIN 3 = 0 to 1.5V step (Note 6)		125	175		125	175	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$ = 0, $V_{PIN\ 4}$ = 0, PIN 7 = open	0.40	0.50	0.60	0.40	0.50	0.60	V
Input Bias Current				1			1	µA
Minimum Latching Current		300	200		300	200		µA
Maximum Non-Latching Current			200	80		200	80	µA
Shutdown Terminal Section								
Threshold Voltage		0.94	1.00	1.06	0.9	1.0	1.1	V
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Delay to Outputs	$V_{PIN\ 16}$ = 0 to 1.3V		75	150		75	150	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = –55°C to +125°C for the UCC1806, –40°C to +85°C for the UCC2806, and 0°C to +70°C for the UCC3806; V_{IN} = 12V, R_T = 33k, C_T = 330pF, C_{BYPASS} on V_{REF} = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITION	UCC1806 / UCC2806			UCC3806			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Supply Voltage		2.5		15	2.5		15	V
Output Low Level	I_{SINK} = 20mA		100	300		100	200	mV
	I_{SINK} = 100mA		0.40	1.1		0.40	1.1	V
Output High Level	I_{SOURCE} = –20mA	11.6	11.9		11.6	11.9		V
	I_{SOURCE} = –100mA	11	11.6		11	11.6		V
Rise Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns
Fall Time	T_J = 25°C, C_{LOAD} = 1000pF		35	65		35	65	ns
Under Voltage Lockout Section								
Startup Current	V_{IN} < Start Threshold		50	100		50	100	µA
Operating Supply Current			1	1.4		1	1.4	mA
V_{IN} Shunt Voltage	I_{VIN} = 10mA	15		17.5	15		17.5	V
Startup Threshold		6.5	7.5	8	6.5	7.5	8	V
Threshold Hysteresis			0.75			0.75		V

Note 1: All voltages are with respect to Ground, Pin 12.

Note 2: Currents are positive into, negative out of the specified terminal.

Note 3: Parameters measured at trip point of latch with $V_{PIN\ 5}$ = V_{REF}, $V_{PIN\ 6}$ = 0V.

Note 4: Amplifier gain defined as: G = delta change at Pin 7/delta change forced at Pin 4 delta voltage at Pin 4 = 0 to 1V.

Note 5: Guaranteed by design. Not 100% tested in production.

Note 6: Current Sense Amp output is slew rate limited to provide noise immunity.

Note 7: Line Range = 10V to 15V, Load Range = 0.2mA to 5mA.

PIN DESCRIPTIONS

AOUT and BOUT: AOUT and BOUT provide alternating high current gate drive for the external MOSFETs. Duty cycle can be varied from 0 to 50% where minimum dead time is a function of CT. Both outputs use MOS transistor switches with inherent anti-parallel body diodes to clamp voltage swings to the supply rails, allowing operation without the use of clamp diodes.

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier is a low output impedance, 2MHz operational amplifier which allows sinking or sourcing of current at the COMP pin. The error amplifier is internally current limited, so that zero duty cycle can be commanded by externally forcing COMP to GND.

CS–: CS- is the inverting input of the 3X, differential current sense amplifier.

CS+: CS+ is the non-inverting input of the 3X, differential current sense amplifier.

CT: CT is the oscillator timing capacitor connection point, which is charged by the current set by RT. CT is discharged to GND through a 2.6mA current sink. This causes a linear discharge of CT to zero volts which then initiates the next switching cycle. Dead time occurs during the discharge of CT, forcing AOUT and BOUT low. Switching frequency (fs) and dead time (td) are approximated by:

$$fs = \frac{1}{2 \bullet RT \bullet CT + td} \text{ and } td = 961 \bullet CT$$

CURLIM: CURLIM programs the primary current limit threshold and determines whether the device will latch off or retry after an overcurrent condition. When a shutdown signal is generated, a 200µA current source to ground pulls down on CURLIM. If the voltage on the pin remains above 350mV the device remains latched and the power must be cycled to restart. If the voltage on the pin falls below 350mV, the device attempts a restart. The voltage threshold is typically set by a resistor divider from

PIN DESCRIPTIONS (continued)

V_{REF} to ground. To calculate the current limit adjust voltage threshold the following equations can be used;

Current Limit Adjust Latching Mode Voltage:

$$V = \frac{V_{REF} - (R1 \bullet 300\,\mu A)}{1 + \frac{R1}{R2}} > 350mV$$

Current Limit Adjust Non-Latching Mode Voltage:

$$V = \frac{V_{REF} - (R1 \bullet 80\,\mu A)}{1 + \frac{R1}{R2}} > 350mV$$

where R1 is the resistance from the V_{REF} to CURLIM and R2 is the resistance from CURLIM to GND.

GND: GND is the reference ground and power ground for all functions of this part. Bypass and timing capacitors should be connected as close as possible to GND.

INV: INV is the inverting input of the error amplifier and has a common mode range from 0V to V_{IN} –2V.

NI: NI is the non-inverting input of the error amplifier and has a common mode range from 0V to V_{IN} –2V.

RT: RT is the connection point for the oscillator timing resistor. It has a low impedance input and is nominally at 1.25V. The current through RT is mirrored to the timing capacitor pin, CT. This causes a linear charging of CT from 0V to 2.35V. Note that the current mirror is limited to a maximum of 100µA so RT must be greater than 12.5k.

SHUTDOWN: The SHUTDOWN pin is provided for enhanced protection. When SHUTDOWN is driven above 1V, AOUT and BOUT are forced low.

SYNC: SYNC is a bi-directional pin, allowing or providing external synchronization with TTL compatible thresholds. In a typical application RT is connected through a timing resistor to GND which allows the internal oscillator to free run. In this mode SYNC outputs a TTL compatible pulse during the oscillator dead time (when CT is being discharged). If RT is forced above 4.4V, SYNC acts as an input with TTL compatible thresholds and the internal oscillator is disabled. When SYNC is high, greater than 2V the outputs are held active low. When SYNC returns low, the outputs may be high until the on-time is terminated by the normal peak current signal, a fault seen at SHUTDOWN or the next high assertion of SYNC. Multiple UCC3806s can be synchronized by a single master UCC3806 or external clock.

VC: VC is the input supply connection for the FET drive outputs and has an input range of 2.5V to 15V. VC should be capacitively bypassed for proper operation.

V_{IN}: V_{IN} is the input supply connection for this device. The UCC1806 has a maximum startup threshold of 8V and internally limited by means of a 15V shunt regulator. The shunted supply current must be limited to 2.5mA. For proper operation, VIN must be bypassed to GND with at least a 0.01µF ceramic capacitor.

V_{REF}: V_{REF} is a 5.1V ±1% trimmed reference output with a 5mA maximum available current. V_{REF} must be bypassed to GND with at least a 0.1µF ceramic capacitor for proper operation.

TYPICAL CHARACTERISTICS

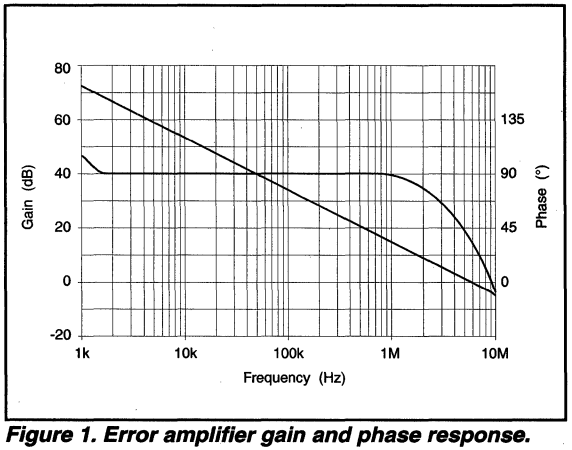


Figure 1. Error amplifier gain and phase response.

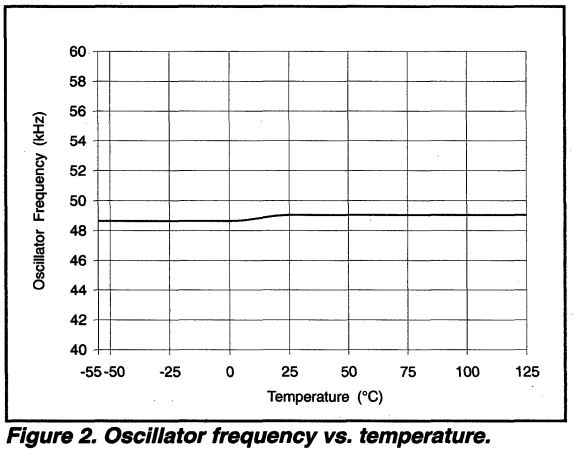


Figure 2. Oscillator frequency vs. temperature.

TYPICAL CHARACTERISTICS (continued)

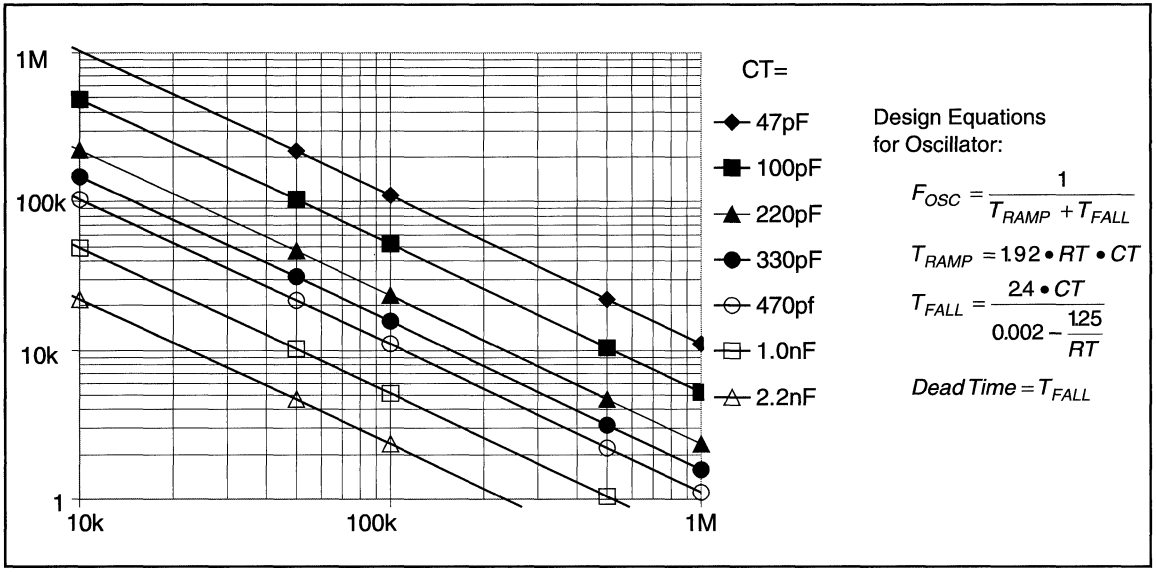


Figure 3. Oscillator frequency vs. RT and CT.

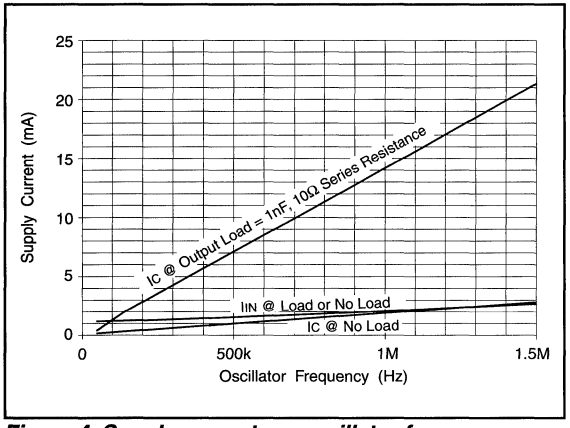


Figure 4. Supply current vs. oscillator frequency.

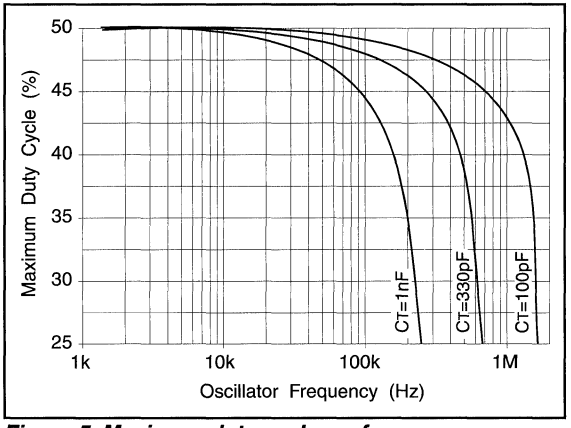
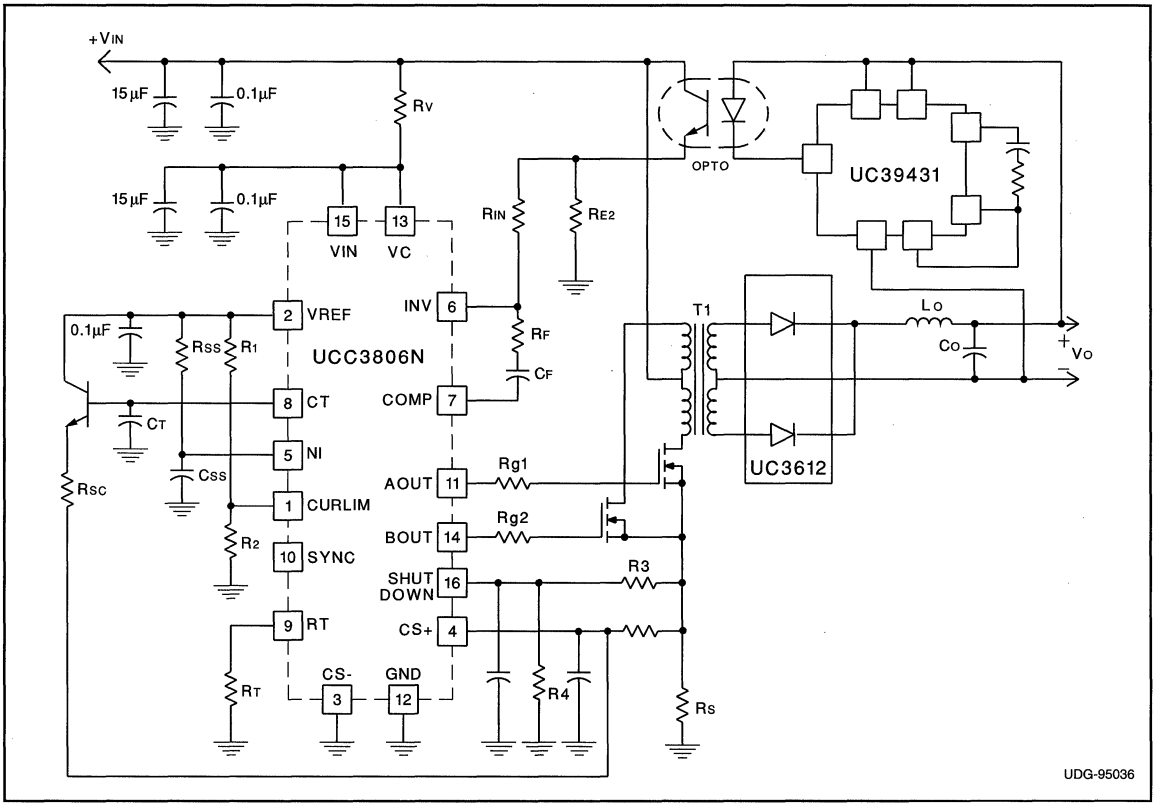


Figure 5. Maximum duty cycle vs. frequency.

TYPICAL APPLICATION



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application INFO available

UCC1807-1/-2/-3
UCC2807-1/-2/-3
UCC3807-1/-2/-3

Programmable Maximum Duty Cycle PWM Controller

FEATURES

- User Programmable Maximum PWM Duty Cycle
- 100µA Startup Current
- Operation to 1MHz
- Internal Full Cycle Soft Start
- Internal Leading Edge Blanking of Current Sense Signal
- 1A Totem Pole Output

DESCRIPTION

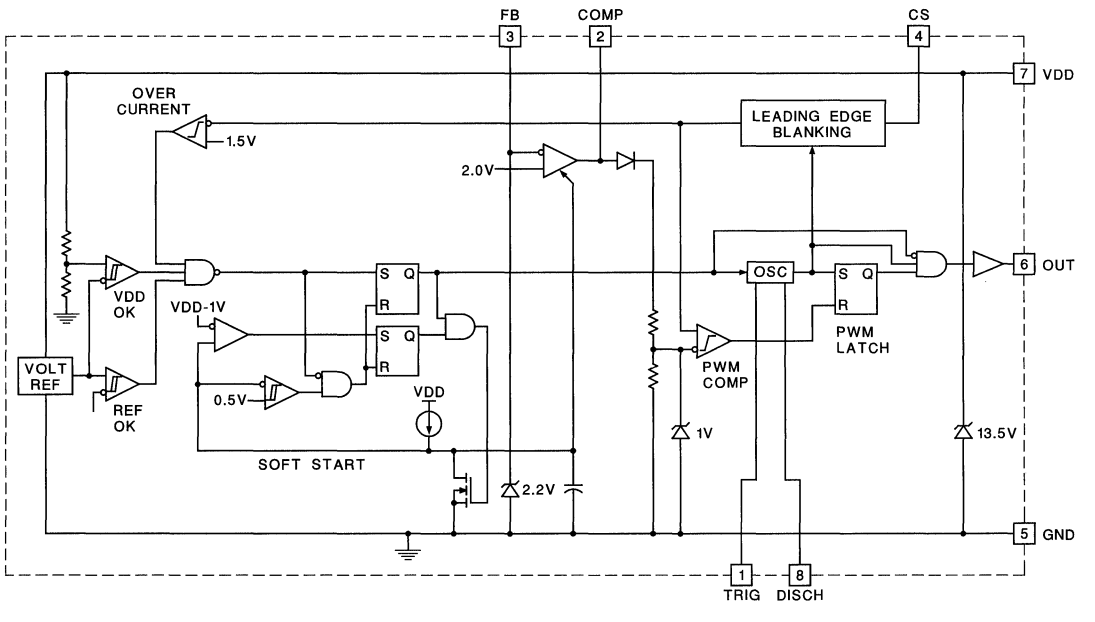
The UCC3807 family of high speed, low power integrated circuits contains all of the control and drive circuitry required for off-line and DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count.

These devices are similar to the UCC3800 family, but with the added feature of a user programmable maximum duty cycle. Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3807 family also features internal full cycle soft start and internal leading edge blanking of the current sense input.

The UCC3807 family offers a variety of package options, temperature range options, and choice of critical voltage levels. The family has UVLO thresholds and hysteresis levels for off-line and battery powered systems. Thresholds are shown in the table below.

Part Number	Turn-on Threshold	Turn-off Threshold
UCCx807-1	7.2V	6.9V
UCCx807-2	12.5V	8.3V
UCCx807-3	4.3V	4.1V

BLOCK DIAGRAM



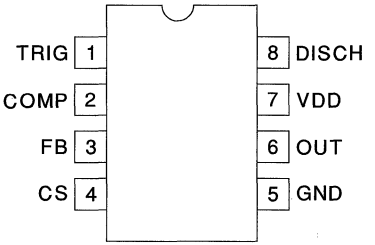
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (I_{DD} ≤10mA) 13.5V
Supply Current 30mA
OUT Current . . . . . ±1A
Analog Inputs (FB, CS) . . . . . –0.3V to (VDD + 0.3V)
Power Dissipation at T_A +25°C (N or J packages) 1W
Power Dissipation at T_A +25°C (D package) 0.65W
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

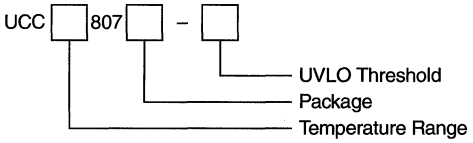
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8, (Top View)
J or N, D Packages



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1807-1/-2/-3; –40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V (Note 6), R_A = 12kΩ, R_B = 4.7kΩ, CT = 330pF, 1.0µF capacitor from VDD to GND, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section Section					
Frequency		175	202	228	kHz
Temperature Stability	(Note 5)		2.5		%
Amplitude	(Note 1)		1/3VDD		V
Error Amplifier Section					
Input Voltage	COMP = 2.0V	1.95	2.00	2.05	V
Input Bias Current		–1		1	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1.0V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 4.0V	–0.2	–0.5		mA
PWM Section					
Maximum Duty Cycle		75	78	81	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 2)	1.1	1.65	1.8	V/V
Maximum Input Signal	COMP = 5.0V (Note 3)	0.9	1.0	1.1	V
Input Bias Current		–200		200	nA
CS Blank Time		50	100	150	ns
Overcurrent Threshold		1.4	1.5	1.6	V
COMP to CS Offset	CS = 0V	0.55	1.1	1.65	V
Output Section					
OUT Low Level	I = 100mA		0.4	1	V
OUT High Level	I = –100mA, VDD - OUT		0.4	1	V
Rise/Fall Time	CL = 1nF (Note 5)		20	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1807-1/-2/-3; –40°C to +85°C for UCC2807-1/-2/-3; and 0°C to +70°C for UCC3807-1/-2/-3; VDD = 10V (Note 6), R_A = 12kΩ, R_B = 4.7kΩ, CT = 330pF, 1.0µF capacitor from VDD to GND, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold	UCCx807-1 (Note 4)	6.6	7.2	7.8	V
	UCCx807-2	11.5	12.5	13.5	V
	UCCx807-3	4.1	4.3	4.5	V
Minimum Operating Voltage After Start	UCCx807-1 (Note 4)	6.3	6.9	7.5	V
	UCCx807-2	7.6	8.3	9.0	V
	UCCx807-3	3.9	4.1	4.3	V
Hysteresis	UCCx807-1	0.1	0.3	0.5	V
	UCCx807-2	3.5	4.2	5.1	V
	UCCx807-3	0.1	0.2	0.3	V
Soft Start Section					
COMP Rise Time	FB = 1.8V, From 0.5V to 4.0V		4		ms
Overall Section					
Startup Current	VDD < Start Threshold (UCCx807-1,-3)		0.1	0.2	mA
	VDD < Start Threshold (UCCx807-2)		0.15	0.25	mA
Operating Supply Current	FB = 0V, CS = 0V, No Load (Note 7)		1.3	2.1	mA
VDD Zener Shunt Voltage	I_{DD} = 10mA	12.0	13.5	15.0	V
Shunt to Start Difference		0.5	1.0		V

Note 1: Measured at TRIG; signal minimum = 1/3 VDD, maximum = 2/3 VDD.

Note 2: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.8V$

Note 3: Parameter measured at trip point of latch with FB at 0V.
Note 4: Start Threshold and Zener Shunt thresholds track one another.
Note 5: Guaranteed by design. Not 100% tested in production.
Note 6: Adjust VDD above the start threshold before setting at 10V for UCC3807-2.
Note 7: Does not include current in external timing RC network.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3807 is a low output impedance, 2MHz operational amplifier. COMP can both source and sink current. The error amplifier is internally current limited, which allows zero duty cycle by externally forcing COMP to GND.

The UCC3807 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: Current sense input. There are two current sense comparators on the chip, the PWM comparator and an overcurrent comparator.

The UCC3807 also contains a leading edge blanking circuit, which disconnects the external CS signal from the current sense comparator during the 100ns interval immediately following the rising edge of the signal at the OUT pin. In most applications, no analog filtering is required on CS. Compared to an external RC filtering technique, leading edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero on-time of the OUT signal is directly affected by the leading edge blanking and the CS to OUT propagation delay.

The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold causes a soft start cycle.

FB: The inverting input to the error amplifier. For best stability, keep connections to FB as short as possible and stray capacitance as small as possible.

GND: Reference ground and power ground for all functions of the part.

OUT: The output of a high current power driver capable of driving the gate of a power MOSFET with peak currents exceeding 1A. OUT is actively held low when VDD is below the UVLO threshold.

The high current power driver consists of MOSFET output devices in a totem pole configuration. This allows the output to switch from VDD to GND. The output stage also provides a very low impedance which minimizes overshoot and undershoot. In most cases, external Schottky clamp diodes are not required.

PIN DESCRIPTIONS (cont.)

TRIG/DISCH: Oscillator control pins. Trig is the oscillator timing input, which has an RC-type charge/discharge signal controlling the chip's internal oscillator. DISCH is the pin which provides the low impedance discharge path for the external RC network during normal operation. Oscillator frequency and maximum duty cycle are computed as follows:

$$frequency \approx \frac{1.4}{(R_A + 2R_B)C_T}$$

$$duty\ cycle \approx \frac{R_A + R_B}{R_A + 2R_B}$$

as shown in Figure 1.

For best performance, keep the lead from C_T to GND as short as possible. A separate ground connection for C_T is desirable. The minimum value of R_A is 10kΩ, the minimum value of R_B is 2.2kΩ, and the minimum value of C_T is 47pF.

VDD: The power input connection for this device. Total VDD current is the sum of quiescent current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

$I_{OUT} = Qg \bullet F$, where F is frequency.

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible in parallel with an electrolytic capacitor.

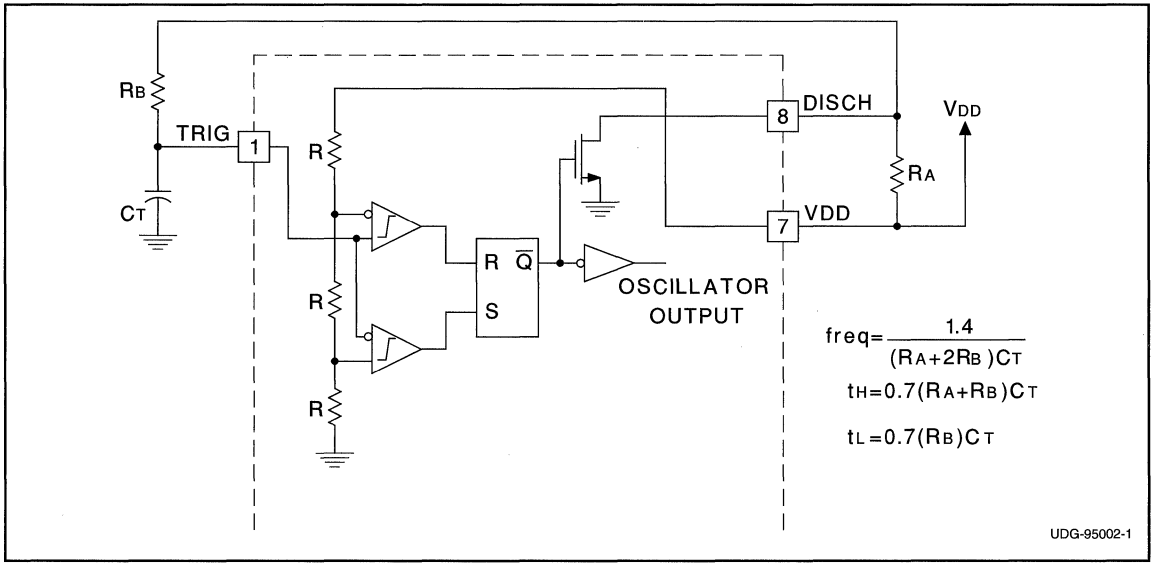


Figure 1. Oscillator Block Diagram

APPLICATIONS INFORMATION

The circuit shown in Fig. 2 illustrates the use of the UCC3807 in a typical off-line application. The 100W, 200kHz, universal input forward converter produces a regulated 12VDC at 8 Amps. The programmable maximum duty cycle of the UCC3807 allows operation down to 80VRMS and up to 265VRMS with a simple RCD clamp to limit the MOSFET voltage and provide core reset. In this application the maximum duty cycle is set to about 65%. Another feature of the design is the use of a flyback winding on the output filter choke for both bootstrapping and voltage regulation. This method of loop closure eliminates the optocoupler and secondary side regulator, common to most off-line designs, while providing good line and load regulation.

T1:	
Core	Magnetics Inc. #P-42625-UG (ungapped)
Primary:	28 turns of 2x #26AWG
Secondary:	6 turns of 50x0.2mm Litz wire
L1:	
Core:	Magnetics Inc. #P-42625-SG-37 (0.020" gap)
Main Winding:	13 turns of 2x #18AWG
Second Winding:	11 turns of #26AWG
Magnetics Inc.	
900 E. Butler Road P.O. Box 391 Butler, PA 16003 Tel: (412) 282-8282 Fax: (412) 282-6955	

APPLICATIONS INFORMATION (cont.)

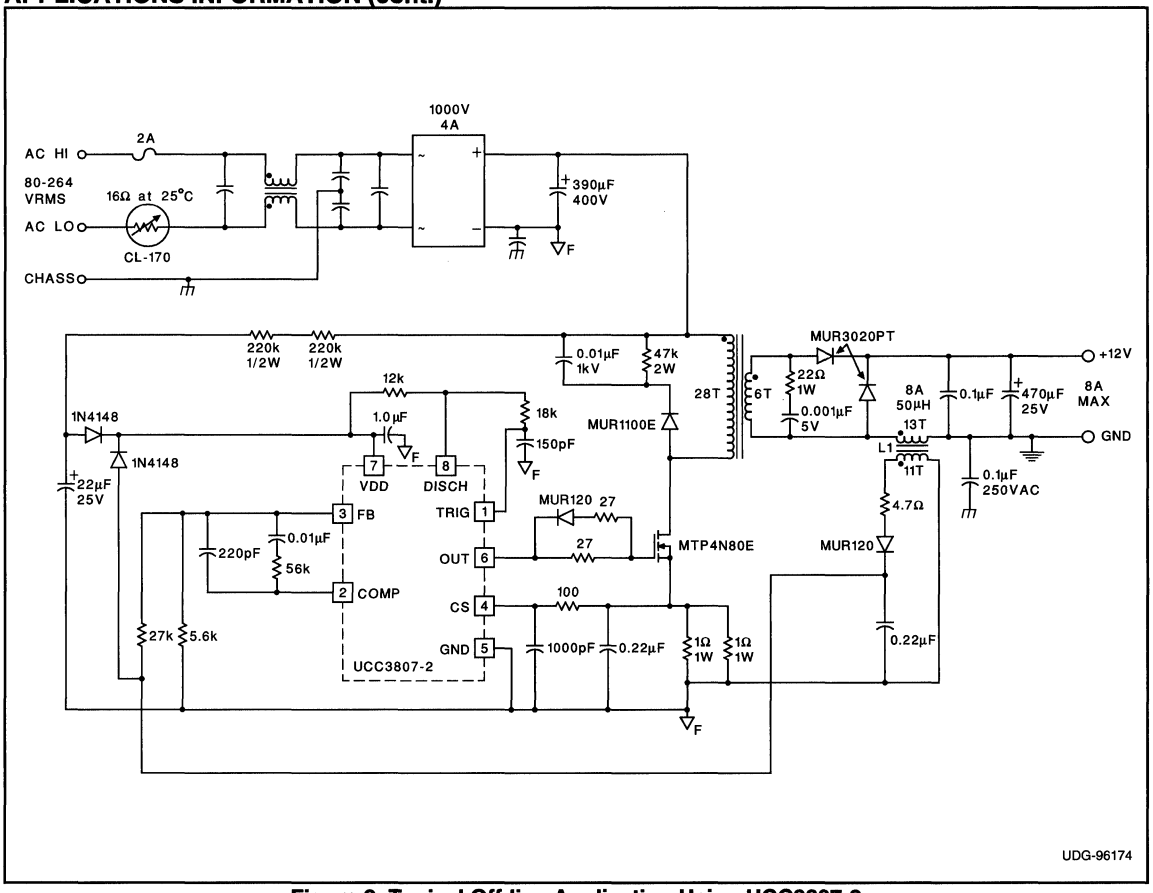


Figure 2. Typical Off-line Application Using UCC3807-2

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UNITRODE

application INFO available

UCC1808-1/-2
UCC2808-1/-2
UCC3808-1/-2

Low Power Current Mode Push-Pull PWM

FEATURES

- 130µA Typical Starting Current
- 1mA Typical Run Current
- Operation to 1MHz
- Internal Soft Start
- On Chip Error Amplifier With 2MHz Gain Bandwidth Product
- On Chip VDD Clamping
- Dual Output Drive Stages In Push-Pull Configuration
- Output Drive Stages Capable Of 500mA Peak Source Current, 1A Peak Sink Current

DESCRIPTION

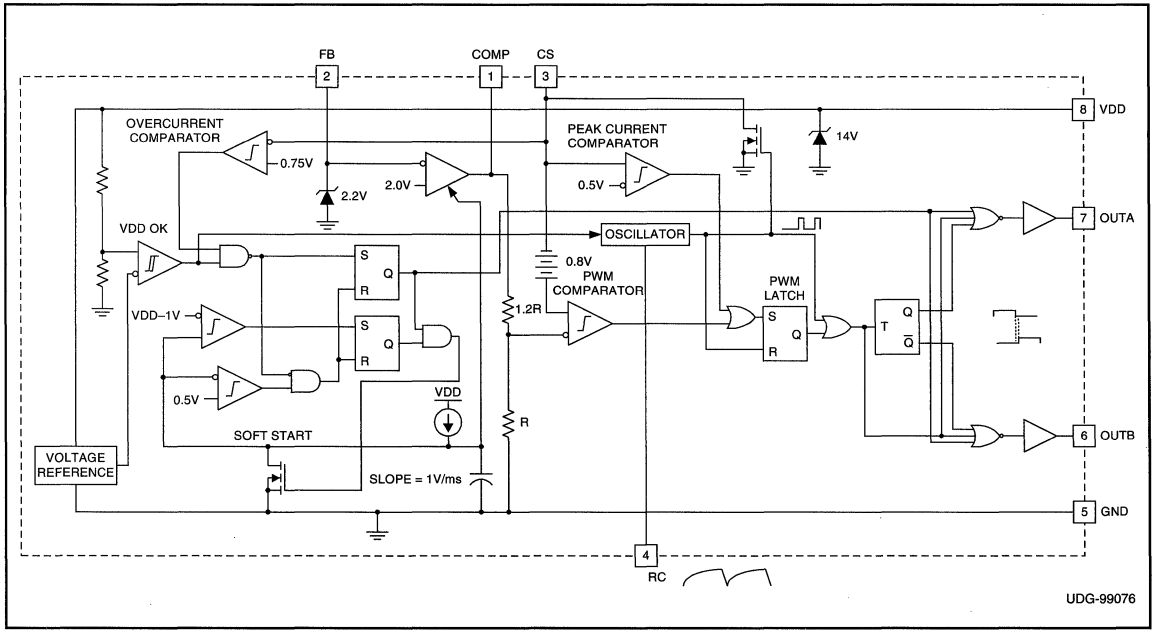
The UCC3808 is a family of BiCMOS push-pull, high-speed, low power, pulse width modulators. The UCC3808 contains all of the control and drive circuitry required for off-line or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

The UCC3808 dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60ns to 200ns depending on the values of the timing capacitor and resistors, thus limits each output stage duty cycle to less than 50%.

The UCC3808 family offers a variety of package options temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for off-line and battery powered systems. Thresholds are shown in the table below.

Part Number	Turn on Threshold	Turn off Threshold
UCCx808-1	12.5V	8.3V
UCCx808-2	4.3V	4.1V

BLOCK DIAGRAM



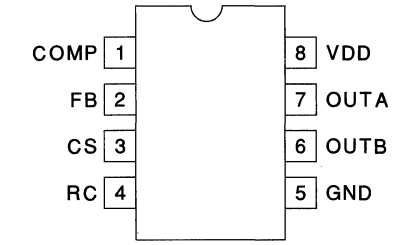
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IDD ≤10mA) 15V
Supply Current 20mA
OUTA/OUTB Source Current (peak) . . . . . –0.5A
OUTA/OUTB Sink Current (peak) 1.0A
Analog Inputs (FB, CS) . –0.3V to VDD+0.3V, not to exceed 6V
Power Dissipation at T_A = 25°C (N Package) 1W
Power Dissipation at T_A = 25°C (D Package) 650mW
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ORDER INFORMATION

UCC ☐ 808 ☐ - ☐
- ☐ — UVLO THRESHOLD
- ☐ — PACKAGE
- ☐ — TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS:

Unless otherwise specified, T_A = 0°C to 70°C for the UCC3808-X, –40°C to 85°C for the UCC2808-X and –55°C to 125°C for the UCC1808-X, VDD = 10V (Note 6), 1µF capacitor from VDD to GND, R = 22kΩ, C = 330pF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Oscillator Frequency		175	194	213	kHz
Oscillator Amplitude/VDD	(Note 1)	0.44	0.5	0.56	V/V
Error Amplifier Section					
Input Voltage	COMP = 2V	1.95	2	2.05	V
Input Bias Current		–1		1	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.2V, COMP = 1V	0.3	2.5		mA
COMP Source Current	FB = 1.3V, COMP = 3.5V	–0.2	–0.5		mA
PWM Section					
Maximum Duty Cycle	Measured at OUTA or OUTB	48	49	50	%
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 2)	1.9	2.2	2.5	V/V
Maximum Input Signal	COMP = 5V (Note 3)	0.45	0.5	0.55	V
CS to Output Delay	COMP = 3.5V, CS from 0 to 600mV		100	200	ns
CS Source Current		–200			nA
CS Sink Current	CS = 0.5V, RC = 5.5V (Note 7)	5	10		mA
Over Current Threshold		0.7	0.75	0.8	V
COMP to CS Offset	CS = 0V	0.35	0.8	1.2	V
Output Section					
OUT Low Level	I = 100mA		0.5	1	V
OUT High Level	I = –50mA, VDD – OUT		0.5	1	V
Rise Time	C_L = 1nF		25	60	ns
Fall Time	C_L = 1nF		25	60	ns
Undervoltage Lockout Section					
Start Threshold	UCCx808-1 (Note 6)	11.5	12.5	13.5	V
	UCCx808-2	4.1	4.3	4.5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C for the UCC3808-X, –40°C to 85°C for the UCC2808-X and –55°C to 125°C for the UCC1808-X, VDD = 10V (Note 6), 1µF capacitor from VDD to GND, R = 22kΩ, C = 330pF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section (cont.)					
Minimum Operating Voltage After Start	UCCx808-1	7.6	8.3	9	V
	UCCx808-2	3.9	4.1	4.3	V
Hysteresis	UCCx808-1	3.5	4.2	5.1	V
	UCCx808-2	0.1	0.2	0.3	V
Soft Start Section					
COMP Rise Time	FB = 1.8V, Rise from 0.5V to 4V		3.5	20	ms
Overall Section					
Startup Current	VDD < Start Threshold		130	260	µA
Operating Supply Current	FB = 0V, CS = 0V (Note 5 and 6)		1	2	mA
VDD Zener Shunt Voltage	IDD = 10mA (Note 4)	13	14	15	V

Note 1: Measured at RC. Signal amplitude tracks VDD.

Note 2: Gain is defined by $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$, $0 \le V_{CS} \le 0.4V$.

Note 3: Parameter measured at trip point of latch with FB at 0V.

Note 4: Start threshold and Zener Shunt threshold track one another.

Note 5: Does not include current in the external oscillator network.

Note 6: For UCCx808-1, set VDD above the start threshold before setting at 10V.

Note 7: The internal current sink on the CS pin is designed to discharge an external filter capacitor. It is not intended to be a DC sink path.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft start. Soft start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft start cycle. An internal MOSFET discharges the current sense filter capacitor to improve dynamic performance of the power converter.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC3808, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500mA peak source current, and 1A peak sink current.

The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This "dead time" between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60ns to 200ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: The oscillator programming pin. The UCC3808's oscillator tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Fig. 1 shows the oscillator block diagram.

Only two components are required to program the oscillator, a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula:

PIN DESCRIPTIONS (cont.)

$$f_{OSCILLATOR} = \frac{1.41}{RC}$$

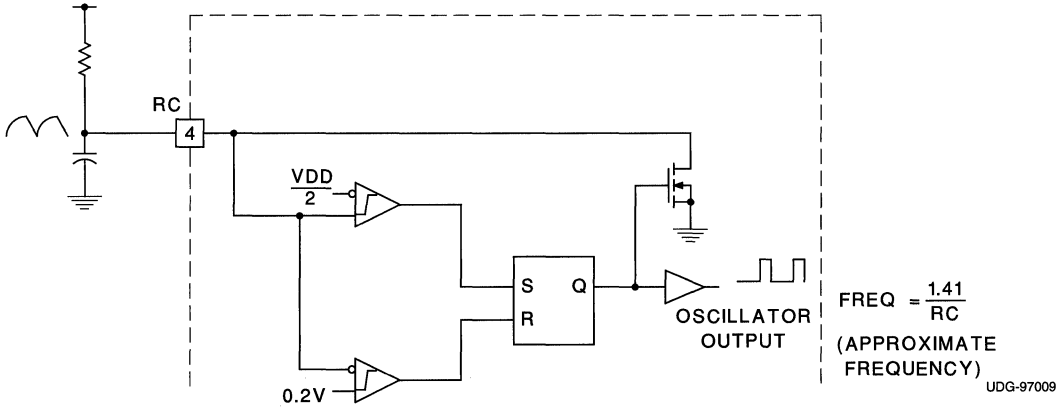
where frequency is in Hertz, resistance in Ohms, and capacitance in Farads. The recommended range of timing resistors is between 10kΩ and 200kΩ and range of timing capacitors is between 100pF and 1000pF. Timing resistors less than 10kΩ should be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from

$I_{OUT} = Qg \bullet F$, where F is frequency.

To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. A 1µF decoupling capacitor is recommended.



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch a ½ the oscillator frequency, with guaranteed duty cycle of < 50% for both outputs.

Figure 1. Block diagram for oscillator.

APPLICATION INFORMATION

A 200kHz push-pull application circuit with a full wave rectifier is shown in Fig. 2. The output, V_O, provides 5V at 75W maximum and is electrically isolated from the input. Since the UCC3808 is a peak current mode controller the 2N2222A emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller and a 1µF is suggested as close to the IC as possible. The controller supply is a series RC for startup, paralleled with a bias winding on the output inductor used in steady state operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the UC3965 Precision Reference with Low Offset Error Amplifier. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanically strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer is a low profile design, EFD size 25, using Magnetics Inc. P material which is a good choice at this frequency and temperature. The input voltage may range from 36V dc to 72V dc. Refer to application note U-170 for addition design information.

APPLICATION INFORMATION (cont.)

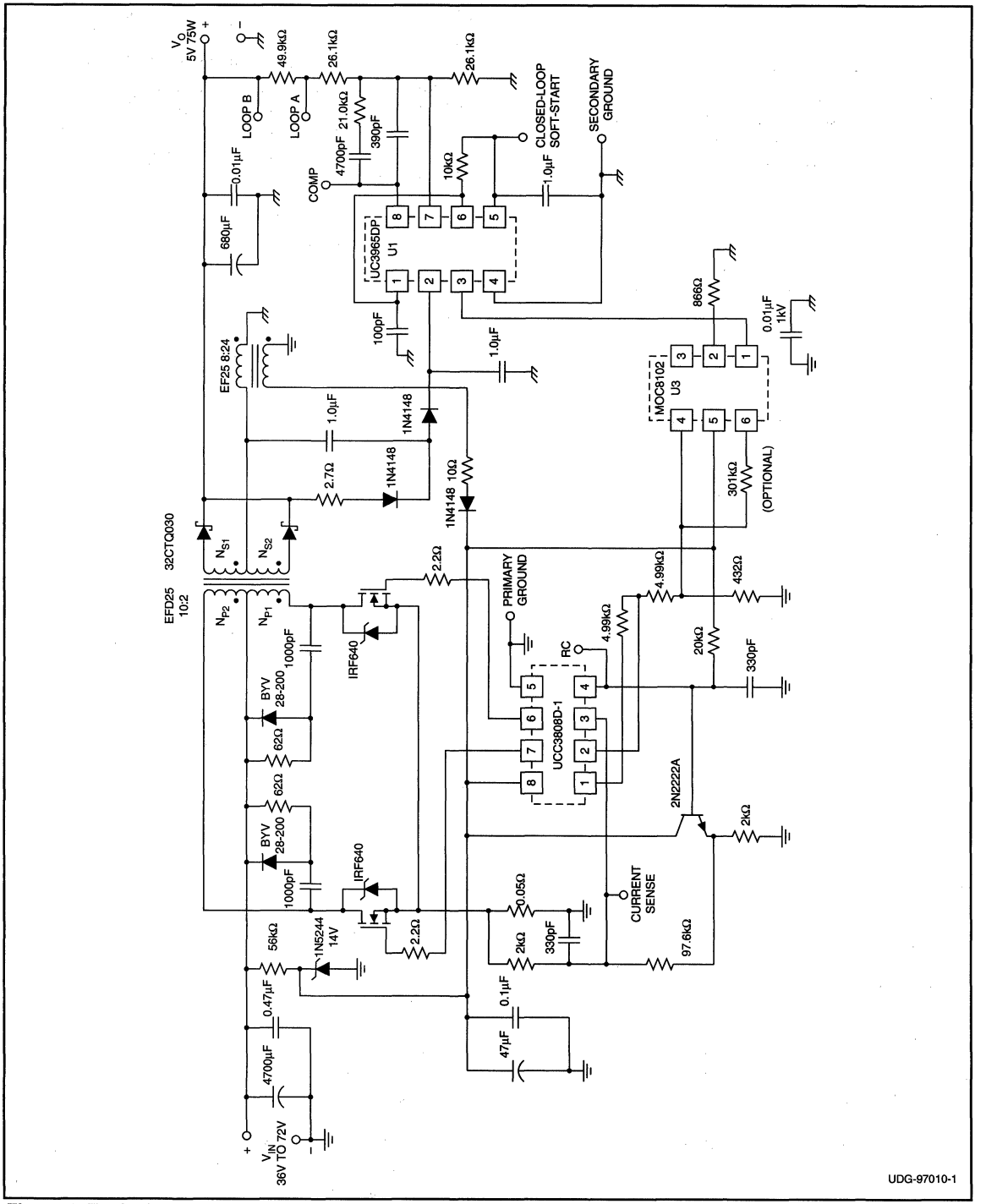


Figure 2. Typical application diagram.

TYPICAL CHARACTERISTIC CURVES

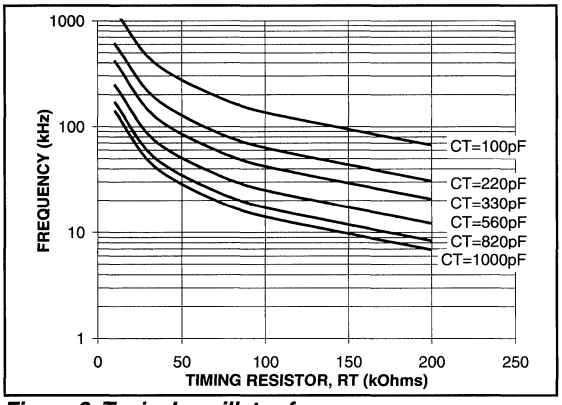


Figure 3. Typical oscillator frequency.

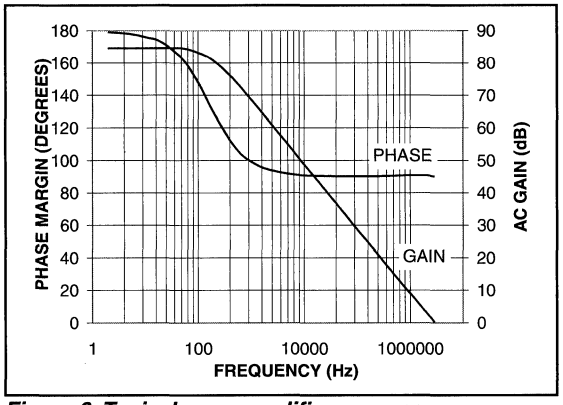


Figure 6. Typical error amplifier response.

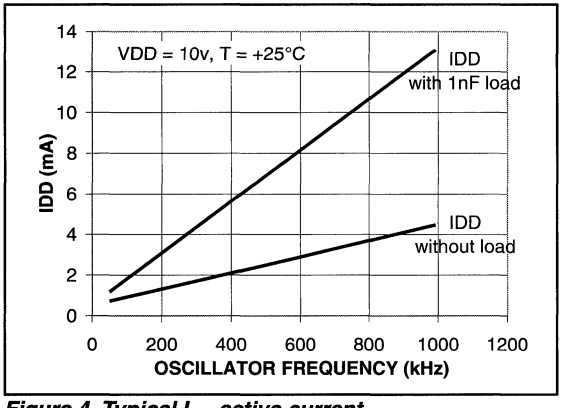


Figure 4. Typical I_{DD} active current.

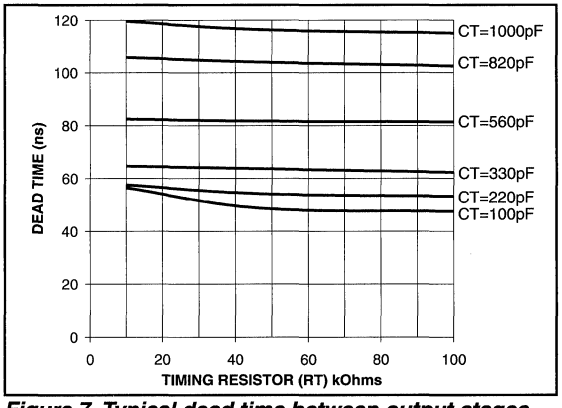


Figure 7. Typical dead time between output stages.

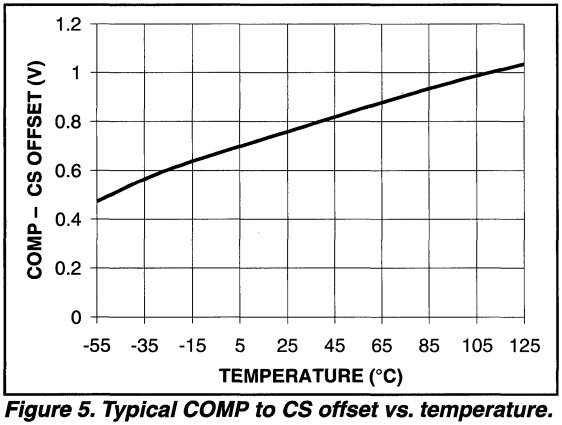


Figure 5. Typical COMP to CS offset vs. temperature.

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UNITRODE

application INFO available

UCC1809-1/-2
UCC2809-1/-2
UCC3809-1/-2

Economy Primary Side Controller

FEATURES

- User Programmable Soft Start With Active Low Shutdown
- User Programmable Maximum Duty Cycle
- Accessible 5V Reference
- Undervoltage Lockout
- Operation to 1MHz
- 0.4A Source/0.8A Sink FET Driver
- Low 100µA Startup Current

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCX809-1	10V	8V
UCCX809-2	15V	8V

DESCRIPTION

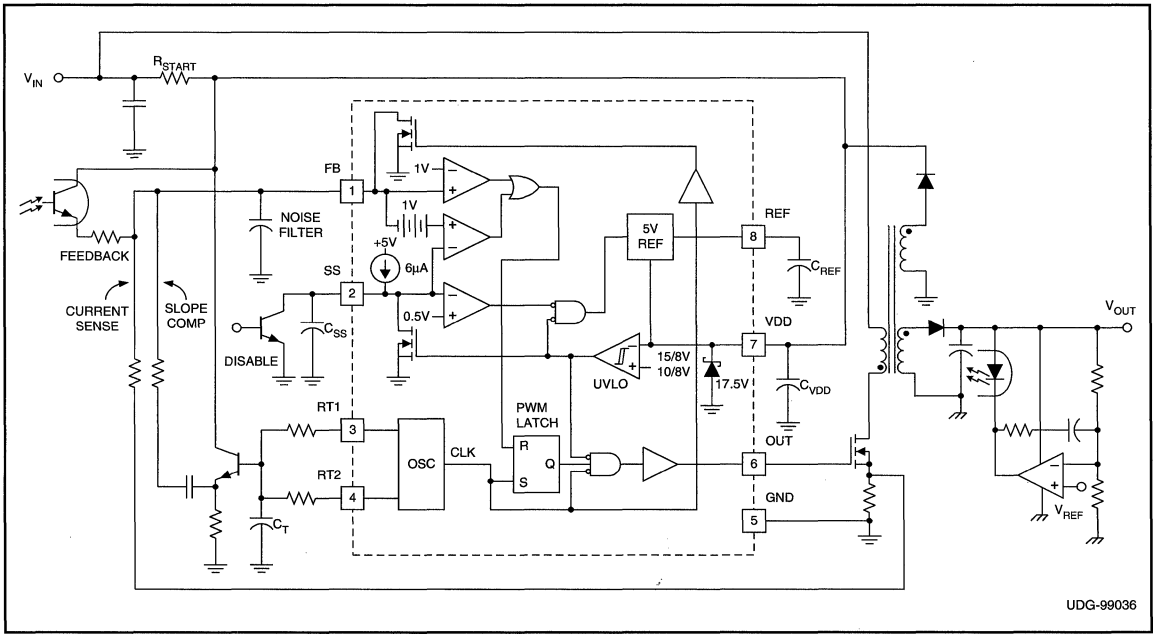
The UCC3809 family of BCDMOS economy low power integrated circuits contains all the control and drive circuitry required for off-line and isolated DC-to-DC fixed frequency current mode switching power supplies with minimal external parts count. Internally implemented circuits include undervoltage lockout featuring startup current less than 100µA, a user accessible voltage reference, logic to ensure latched operation, a PWM comparator, and a totem pole output stage to sink or source peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state.

Oscillator frequency and maximum duty cycle are programmed with two resistors and a capacitor. The UCC3809 family also features full cycle soft start.

The family has UVLO thresholds and hysteresis levels for off-line and DC-to-DC systems as shown in the table to the left.

The UCC3809 and the UCC2809 are offered in the 8 pin SOIC (D), PDIP (N), TSSOP (PW), and MSOP (P) packages. The small TSSOP and MSOP packages make the device ideal for applications where board space and height are at a premium.

TYPICAL APPLICATION DIAGRAM



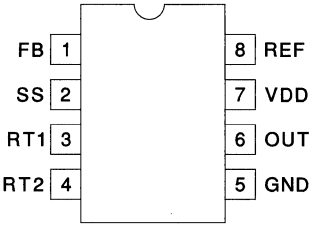
ABSOLUTE MAXIMUM RATINGS

VDD 19V
I_{VDD} 25mA
I_{OUT} (tpw < 1µs and Duty Cycle < 10%) . . . . . –0.4A to 0.8A
RT1, RT2, SS . . . . . –0.3V to REF + 0.3V
I_{REF} . . . . . –15mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

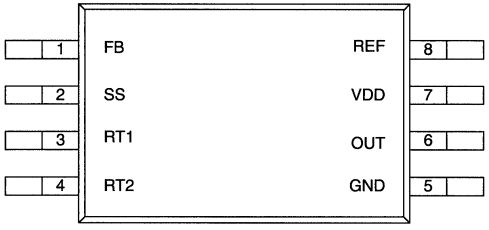
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

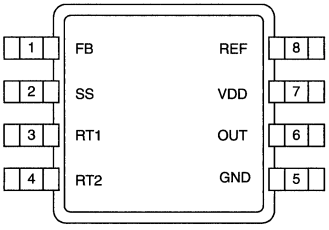
SOIC-8, DIL-8 (Top View)
D, N and J Packages



TSSOP-8 (Top View)
PW Package



MSOP-8 (Top View)
P Package



	Temperature Range	Available Packages
UCC1809-X	–55°C to +125°C	J
UCC2809-X	–40°C to +85°C	N, D, P, PW
UCC3809-X	0°C to +70°C	N, D, P, PW

ORDERING INFORMATION

UCC□ 809□ –□

- UVLO OPTION
- PACKAGE
- TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Section					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD}	No Load		600	900	µA
I_{VDD} Starting				100	µA
Undervoltage Lockout Section					
Start Threshold (UCCx809-1)		9.4		10.4	V
UVLO Hysteresis (UCCx809-1)		1.65			V
Start Threshold (UCCx809-2)		14.0		15.6	V
UVLO Hysteresis (UCCx809-2)		6.2			V
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA	4.75	5	5.25	V
Line Regulation	VDD = 10V to 15V		2		mV
Load Regulation	I_{REF} = 0mA to 5mA		2		mV
Comparator Section					
I_{FB}	Output Off		–100		nA
Comparator Threshold		0.9	0.95	1	V
OUT Propagation Delay (No Load)	V_{FB} = 0.8V to 1.2V at T_R = 10ns		50	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD = 12V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft Start Section					
I_{SS}	VDD = 16V, V_{SS} = 0V	–3	–6	–16	µA
V_{SS} Low	VDD = 7.5V, I_{SS} = 200µA			0.2	V
Shutdown Threshold		0.44	0.48	0.52	V
Oscillator Section					
Frequency	RT1 = 10k, RT2 = 4.32k, CT = 820pF	90	100	110	kHz
Frequency Change with Voltage	VDD = 10V to 15V		0.1		%/V
C_T Peak Voltage			3.33		V
C_T Valley Voltage			1.67		V
C_T Peak to Peak Voltage		1.54	1.67	1.80	V
Output Section					
Output V_{SAT} Low	I_{OUT} = 80mA (dc)		0.8	1.5	V
Output V_{SAT} High	I_{OUT} = –40mA (dc), VDD – OUT		0.8	1.5	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc)			1.5	V
Minimum Duty Cycle	V_{FB} = 2V		0		%
Maximum Duty Cycle			70		%
Rise Time	C_{OUT} = 1nF		35		ns
Fall Time	C_{OUT} = 1nF		18		ns

PIN DESCRIPTIONS

FB: This pin is the summing node for current sense feedback, voltage sense feedback (by optocoupler) and slope compensation. Slope compensation is derived from the rising voltage at the timing capacitor and can be buffered with an external small signal NPN transistor. External high frequency filter capacitance applied from this node to GND is discharged by an internal 250Ω on resistance NMOS FET during PWM off time and offers effective leading edge blanking set by the RC time constant of the feedback resistance from current sense resistor to FB input and the high frequency filter capacitor capacitance at this node to GND.

GND: Reference ground and power ground for all functions.

OUT: This pin is the high current power driver output.

REF: The internal 5V reference output. This reference is buffered and is available on the REF pin. REF should be bypassed with a 0.47µF ceramic capacitor.

RT1: This pin connects to timing resistor RT1 and controls the positive ramp time of the internal oscillator (Tr = 0.74 • (C_T + 27pF) • RT1). The positive threshold of the internal oscillator is sensed through inactive timing resistor RT2 which connects to pin RT2 and timing capacitor C_T.

RT2: This pin connects to timing resistor RT2 and controls the negative ramp time of the internal oscillator (Tf = 0.74 • (C_T + 27pF) • RT2). The negative threshold of the internal oscillator is sensed through inactive timing resistor RT1 which connects to pin RT1 and timing capacitor C_T.

SS: This pin serves two functions. The soft start timing capacitor connects to SS and is charged by an internal 6µA current source. Under normal soft start SS is discharged to at least 0.4V and then ramps positive to 1V during which time the output driver is held low. As SS charges from 1V to 2V soft start is implemented by an increasing output duty cycle. If SS is taken below 0.5V, the output driver is inhibited and held low. The user accessible 5V voltage reference also goes low and I_{VDD} < 100µA.

VDD: The power input connection for this device. This pin is shunt regulated at 17.5V which is sufficiently below the voltage rating of the DMOS output driver stage. VDD should be bypassed with a 1µF ceramic capacitor.

APPLICATION INFORMATION

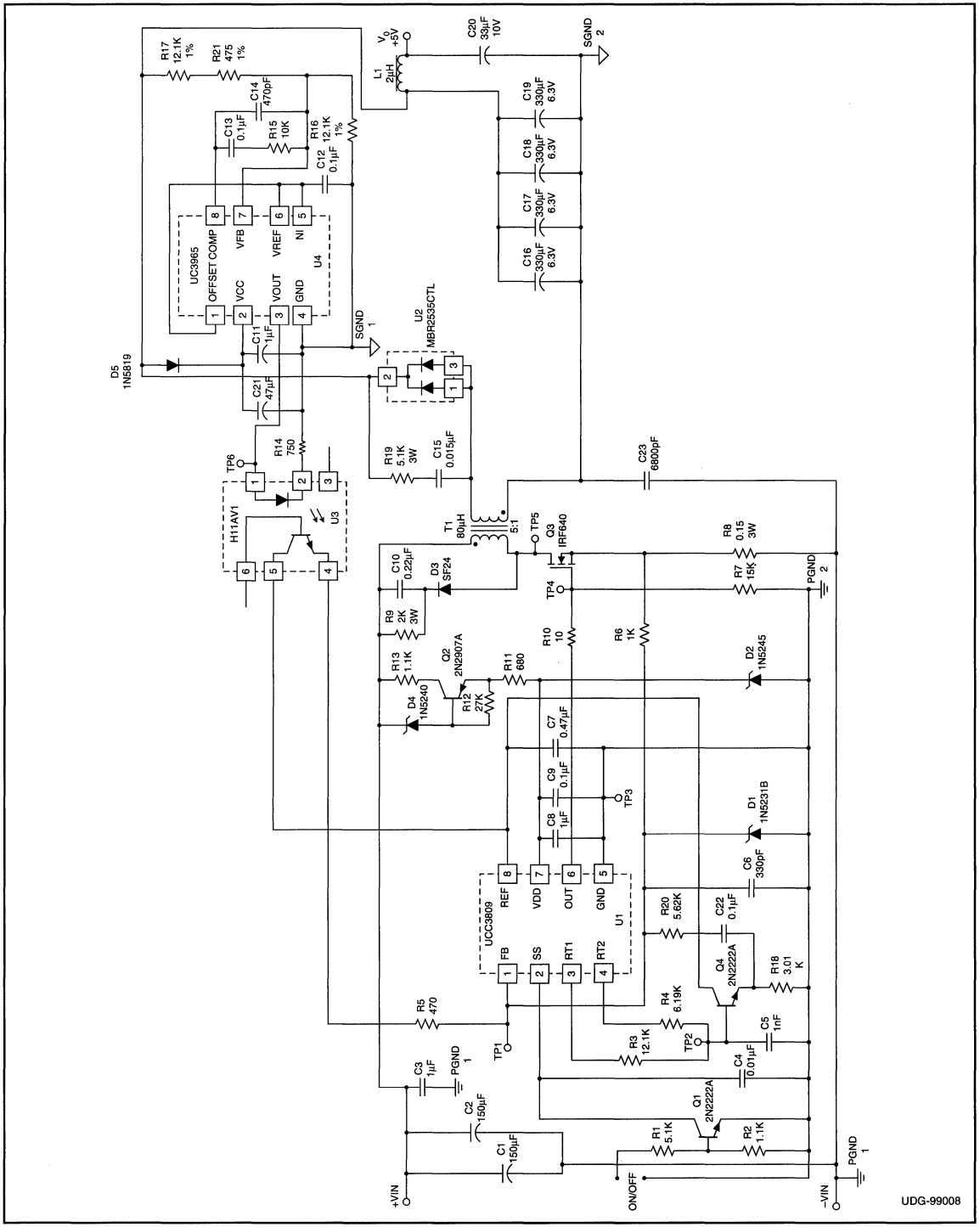


Figure 1. Detailed application diagram: –48V to +5V flyback converter.

APPLICATION INFORMATION (cont.)

The Typical Application Diagram shows an isolated flyback converter utilizing the UCC3809. Note that the capacitors C_{REF} and C_{VDD} are local decoupling capacitors for the reference and IC input voltage, respectively. Both capacitors should be low ESR and ESL ceramic, placed as close to the IC pins as possible, and returned directly to the ground pin of the chip for best stability. REF provides the internal bias to many of the IC functions and C_{REF} should be at least 0.47µF to prevent REF from drooping.

FB Pin

The basic premise of the UCC3809 is that the voltage sense feedback signal originates from an optocoupler that is modulated by an external error amplifier located on the secondary side. This signal is summed with the current sense signal and any slope compensation at the FB pin and compared to a 1V threshold, as shown in the Typical Application Diagram. Crossing this 1V threshold resets the PWM latch and modulates the output driver on-time much like the current sense comparator used in the UC3842. In the absence of a FB signal, the output will follow the programmed maximum on-time of the oscillator.

When adding slope compensation, it is important to use a small capacitor to AC couple the oscillator waveform before summing this signal into the FB pin. By correctly selecting the emitter resistor of the optocoupler, the voltage sense signal can force the FB node to exceed the 1V threshold when the output that is being compared exceeds a desired level. Doing so drives the UCC3809 to zero percent duty cycle.

Oscillator

The following equation sets the oscillator frequency:

$$F_{OSC} = [0.74 \bullet (CT + 27pF) \bullet (RT1 + RT2)]^{-1}$$

$$D_{MAX} = 0.74 \bullet RT1 \bullet (CT + 27pF) \bullet F_{OSC}$$

Referring to Figure 2 and the waveforms in Figure 3, when Q1is on, CT charges via the $R_{DS(on)}$ of Q1 and RT1. During this charging process, the voltage of CT is sensed through RT2. The S input of the oscillator latch, S(OSC), is level sensitive, so crossing the upper threshold (set at 2/3 VREF or 3.33V for a typical 5.0V reference) sets the Q output (CLK signal) of the oscillator latch high. A high CLK signal results in turning off Q1 and turning on Q2. CT now discharges through RT2 and the $R_{DS(on)}$ of Q2. CT discharges from 3.33V to the lower threshold (set at 1/3 VREF or 1.67V for a typical 5.0V reference) sensed through RT1. The R input to the oscillator latch, R(OSC), is also level sensitive and resets the CLK signal low when CT crosses the 1.67V threshold, turning off Q2 and turning on Q1, initiating another charging cycle.

Figure 3 shows the waveforms associated with the oscillator latch and the PWM latch (shown in the Typical Application Diagram). A high CLK signal not only initiates a discharge cycle for CT, it also turns on the internal NMOS FET on the FB pin causing any external capacitance used for leading edge blanking connected to this pin to be discharged to ground. By discharging any external capacitor completely to ground during the external switch's off-time, the noise immunity of the converter is enhanced allowing the user to design in smaller RC components for leading edge blanking. A high CLK signal also sets the level sensitive S input of the PWM latch, S(PWM), high, resulting in a high output, Q(PWM), as shown in Figure 3. This Q(PWM) signal will remain high until a reset signal, R(PWM) is received. A high R(PWM) signal results from the FB signal crossing the 1V threshold, or during soft start or if the SS pin is disabled.

Assuming the UVLO threshold is satisfied, the OUT signal of the IC will be high as long as Q(PWM) is high and S(PWM), also referred to as CLK, is low. The OUT signal will be dominated by the FB signal as long as the FB signal trips the 1V threshold while CLK is low. If the FB signal does not cross the 1V threshold while CLK is low, the OUT signal will be dominated by the maximum duty cycle programmed by the user. Figure 3 illustrates the various waveforms for a design set up for a maximum duty cycle of 70%.

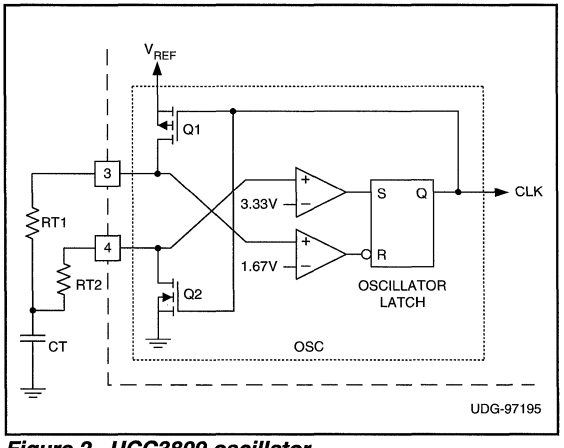


Figure 2. UCC3809 oscillator.

APPLICATION INFORMATION (cont.)

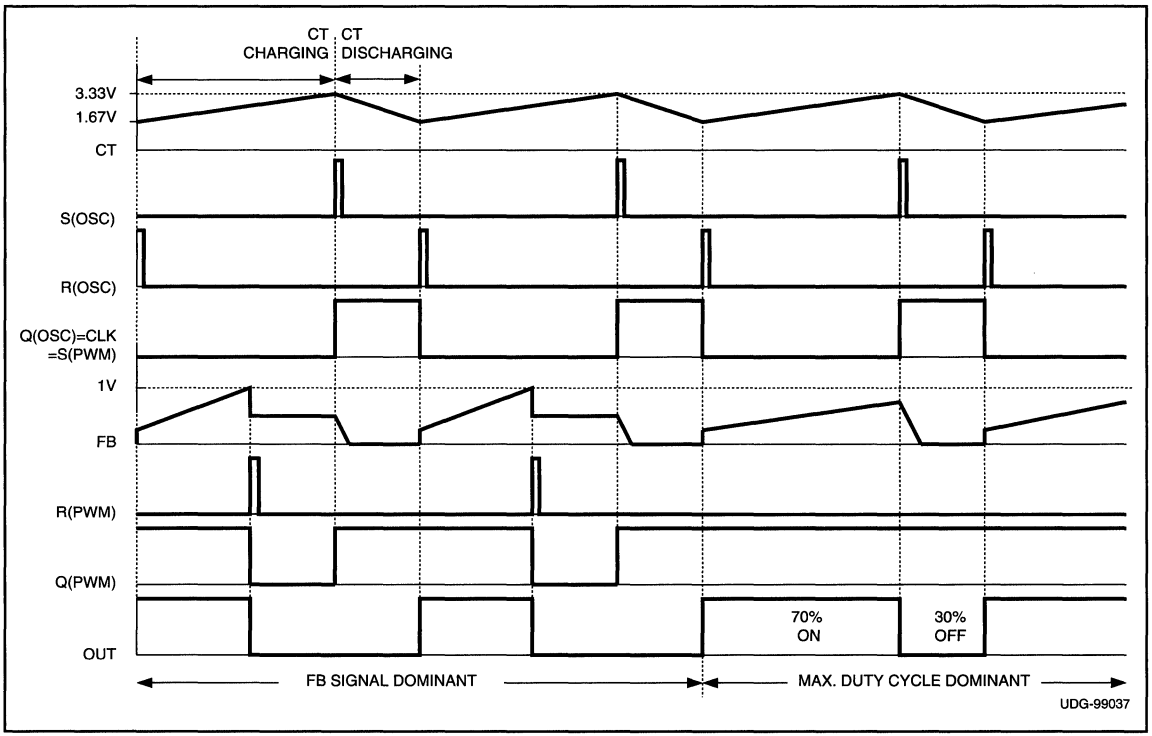


Figure 3. Waveforms associated with the oscillator latch and the PWM latch.

The recommended value for CT is 1nF for frequencies in the 100 kHz or less range and smaller CT for higher frequencies. The minimum recommended values of RT1 and RT2 are 10kΩ and 4.32kΩ, respectively. Using these values maintains a ratio of at least 20:1 between the $R_{DS(on)}$ of the internal FETs and the external timing resistors, resulting in minimal change in frequency over temperature. Because of the oscillator's susceptibility to capacitive coupling, examine the oscillator frequency by looking at the common RT1-RT2-CT node on the circuit board as opposed to looking at pins 3 and 4 directly. For good noise immunity, RT1 and RT2 should be placed as close to pins 3 and 4 of the IC as possible. CT should be returned directly to the ground pin of the IC with minimal stray inductance and capacitance.

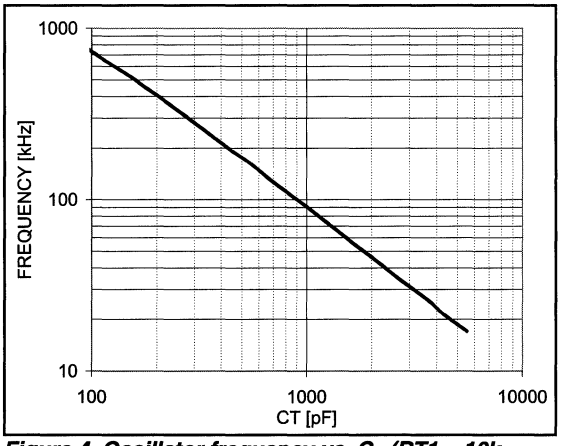


Figure 4. Oscillator frequency vs. C_T (RT1 = 10k, RT2 = 4.32k)

APPLICATION INFORMATION (cont.)

Synchronization

Both of the synchronization schemes shown in Figure 5 can be successfully implemented with the internal oscillator of the UCC3809. Both schemes allow access to the timing ramp needed for slope compensation and have minimal impact on the programmed maximum duty cycle. In the absence of a sync pulse, the PWM controller will run independently at the frequency set by RT1, RT2, and CT. This free running frequency must be approximately 15 to 20% lower than the sync pulse frequency to insure the free running oscillator does not cross the comparator threshold before the desired sync pulse.

Option I uses the synchronization pulse to pull pin 3 low, triggering the internal 1.67V comparator to reset the RS latch and initiate a charging cycle. The valley voltage of the CT waveform is higher when synchronized using this configuration, decreasing the ramp charge and discharge times, thereby increasing the operating frequency; otherwise the overall shape of the CT voltage waveform is unchanged.

Option II uses the synchronization pulse to superimpose the sync voltage onto the peak of the CT waveform. This triggers the internal 3.33V comparator, initiating a discharge cycle. The sync pulse is summed with the free running oscillator waveform at the CT node, resulting in a spike on top of the CT peak voltage.

ADDITIONAL INFORMATION

Please refer to the following Unitrode application topics for additional information.

[1] Application Note U-165, *Design Review: Isolated 50W Flyback Converter with the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier* by Lisa Dinwoodie.

[2] Design Note DN-89, *Comparing the UC3842, UCC3802, and UCC3809 Primary Side PWM Controllers* by Lisa Dinwoodie.

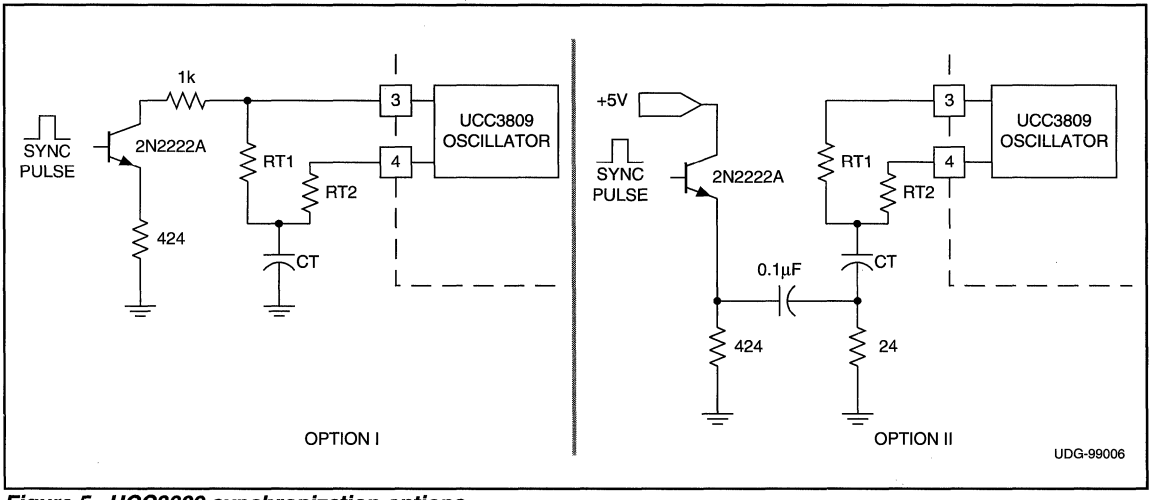


Figure 5. UCC3809 synchronization options.

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UNITRODE

application INFO available

UCC1810
UCC2810
UCC3810

Dual Channel Synchronized Current Mode PWM

FEATURES

- Single Oscillator Synchronizes Two PWMs
- 150µA Startup Supply Current
- 2mA Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Full-Cycle Fault Restart
- Internal Leading Edge Blanking of the Current Sense Signal
- 1 Amp Totem Pole Outputs
- 75ns Typical Response from Current Sense to Output
- 1.5% Tolerance Voltage Reference

DESCRIPTION

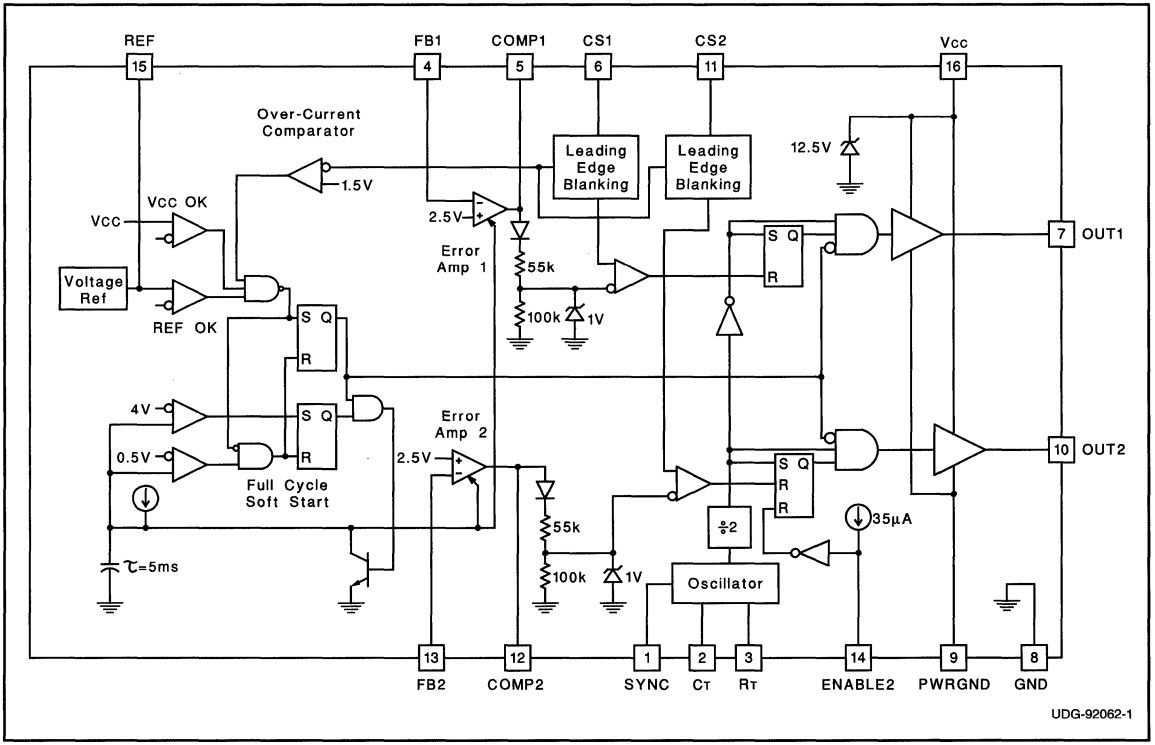
The UCC3810 is a high-speed BiCMOS integrated circuit which implements two synchronized pulse width modulators for use in off-line and DC-to-DC power supplies.

The UCC3810 provides perfect synchronization between two PWMs by using the same oscillator. The oscillator's sawtooth waveform can be used for slope compensation if required.

Using a toggle flip flop to alternate between modulators, the UCC3810 ensures that one PWM will not slave, interfere, or otherwise affect the other PWM. This toggle flip flop also ensures that each PWM will be limited to 50% maximum duty cycle, insuring adequate off-time to reset magnetic elements.

This IC contains many of the same elements of the UC3842 current mode controller family, combined with the enhancements of the UCC3802. This minimizes power supply parts count. Enhancements include leading edge blanking of the current sense signals, full cycle fault restart, CMOS output drivers, and outputs which remain low even when the supply voltage is removed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC} Voltage (Note 3) 11V
V_{CC} Current 20mA
OUT1, OUT2 Current, Peak, 5% Duty Cycle. . . . . ±1A
OUT1, OUT2 Energy (Capacitive Load) 20µJ
Analog Inputs (FB1, FB2, CS1, CS2, SYNC). . . . –0.3V to 6.3V
Operating Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

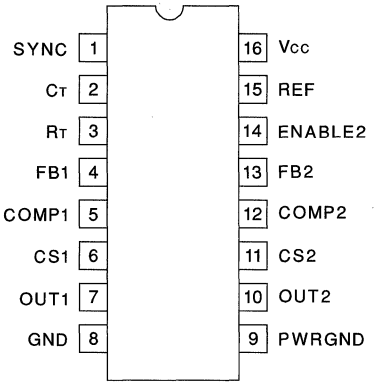
Note 1: *All voltages are with respect to GND. All currents are positive into the specified terminals.*

Note 2: *Consult Unitrode Integrated Circuits Product & Applications Handbook for information regarding thermal specifications and limitations of packages.*

Note 3: *In normal operation, V_{CC} is powered through a current limiting resistor. Absolute maximum of 11V applies when driven from a low impedance such that the V_{CC} current does not exceed 20mA.*

CONNECTION DIAGRAM

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55^{\circ}C \le T_A \le 125^{\circ}C$ for UCC1810; $-40^{\circ}C \le T_A \le 85^{\circ}C$ for UCC2810; $0^{\circ}C \le T_A \le 70^{\circ}C$ for UCC3810; V_{CC} = 10V (Note 4); R_T = 150k; C_T = 120pF; No Load; $T_A = T_J$. All parameters are the same for both channels.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C	4.925	5.000	5.075	V
Load Regulation	0mA < I_{REF} < 5mA		5	25	mV
Line Regulation	UVLO Stop Threshold Voltage +0.5V < V_{CC} < Shunt Voltage		12		mV
Output Voltage	Full temperature range, 0mA < I_{REF} < 5mA	4.85	5.00	5.10	V
Output Noise Voltage	10Hz < f < 10kHz, T_J = +25°C (Note 10)		235		µV
Long Term Stability	T_A = +125°C, 1000 Hours (Note 10)		5		mV
Output Short Circuit Current			–8	–25	mA
Oscillator Section					
Oscillator Frequency	R_T = 30k, C_T = 120pF (Note 5)	840	940	1040	kHz
Oscillator Frequency	R_T = 150k, C_T = 120pF (Note 5)	200	220	240	kHz
Temperature Stability	(Note 10)		2.5		%
Peak Voltage			2.5		V
Valley Voltage			0.05		V
Peak-to-Peak Amplitude		2.25	2.45	2.65	V
SYNC Threshold		0.80	1.65	2.2	V
SYNC Input Current	SYNC = 5V		30		µA
Error Amplifier Section					
FB Input Voltage	COMP = 2.5V	2.44	2.50	2.56	V
FB Input Bias Current				±1	µA
Open Loop Voltage Gain		60	73		dB
Unity Gain Bandwidth	(Note 10)		2		MHz
COMP Sink Current	FB = 2.7V, COMP = 1V	0.3	1.4	3.5	mA
COMP Source Current	FB = 1.8V, COMP = 4V	–0.2	–0.5	–0.8	mA
Minimum Duty Cycle	COMP = 0V			0	%
COMP Soft Start Rise Time	FB = 1.8V, Rise from 0.5V to REF–1.5V		5		ms

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55^{\circ}C \le T_A \le 125^{\circ}C$ for UCC1810; $-40^{\circ}C \le T_A \le 85^{\circ}C$ for UCC2810; $0^{\circ}C \le T_A \le 70^{\circ}C$ for UCC3810; V_{CC} = 10V (Note 4); R_T = 150k; C_T = 120pF; No Load; $T_A = T_J$. All parameters are the same for both channels.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
Gain	(Note 6)	1.20	1.55	1.80	V/V
Maximum Input Signal	COMP = 5V (Note 7)	0.9	1.0	1.1	V
CS Input Bias Current				± 200	nA
CS to OUT Propagation Delay	CS steps from 0V to 1.2V, COMP = 2.5V		75		ns
CS Blank Time	(Note 8)		55		ns
CS Overcurrent Threshold		1.35	1.55	1.85	V
COMP to CS Offset	CS = 0V	0.65	0.95	1.4	V
PWM Section					
Maximum Duty Cycle	R_T = 150k, C_T = 120pF (Note 10)	45	49	50	%
Maximum Duty Cycle	R_T = 30k, C_T = 120pF (Note 10)	40	45	48	%
Minimum On Time	CS =1.2V, COMP = 5V		130		ns
Output Section					
OUT Low Level	I_{OUT} = 20mA		0.12	0.42	V
	I_{OUT} = 200mA		0.48	1.10	V
	I_{OUT} = 20mA, V_{CC} = 0V		0.7	1.20	V
OUT High Level (V_{CC} - OUT)	I_{OUT} = –20mA		0.15	0.42	V
	I_{OUT} = –200mA		1.20	2.30	V
OUT Rise Time	C_{OUT} = 1nF		20	50	ns
OUT Fall Time	C_{OUT} = 1nF		30	60	ns
Undervoltage Lockout Section					
Start Threshold		9.9	11.3	13.2	V
Stop Threshold		7.5	8.3	9.5	V
Start to Stop Hysteresis		1.7	3.0	4.7	V
ENABLE2 Input Bias Current	ENABLE2 = 0V	–20	–35	–55	µA
ENABLE2 Input Threshold Voltage		0.80	1.53	2.00	V
Overall Section					
Startup Current	V_{CC} < Start Threshold Voltage		0.15	0.25	mA
Operating Supply Current, Outputs Off	V_{CC} = 10V, FB = 2.75V		2.0	3.0	mA
Operating Supply Current, Outputs On	V_{CC} = 10V, FB = 0V, CS = 0V, R_T = 150k		3.2	5.1	mA
Operating Supply Current, Outputs On	V_{CC} = 10V, FB = 0V, CS = 0V, R_T = 30k		8.5	14.5	mA
V_{CC} Internal Zener Voltage	I_{CC} = 10mA (Note 9)	11.0	12.9	14.0	V
V_{CC} Internal Zener Voltage Minus Start Threshold Voltage		0.4	1.2		V

Note 4: Adjust V_{CC} above the start threshold before setting at 10V.

Note 5: Oscillator frequency is twice the output frequency. $F_{OSC} \approx \dfrac{4}{RT \times CT}$

Note 6: Current Sense Gain A is defined by: $A = \dfrac{\Delta VCOMP}{\Delta VCS}$ $0 \le VCS \le 0.8V$.

Note 7: Parameter measured at trip point of latch with FB = 0V.
Note 8: CS Blank Time is measured as the difference between the minimum non-zero on-time and the CS to OUT delay.
Note 9: Start Threshold Voltage and V_{CC} Internal Zener Voltage track each other.
Note 10: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP1, COMP2: The low impedance outputs of the error amplifiers.

CS1, CS2: The current sense inputs to the PWM comparators. These inputs have leading edge blanking. For most applications, no input filtering is required. Leading edge blanking disconnects the CS inputs from all internal circuits for the first 55ns of each PWM cycle. When used with very slow diodes or in other applications where the current sense signal is unusually noisy, a small current sense RC filter may be required.

CT: The timing capacitor of the oscillator. Recommended values of C_T are between 100pF and 1nF. Connect the timing capacitor directly across C_T and GND.

ENABLE2: A logic input which disables PWM 2 when low. This input has no effect on PWM 1. This input is internally pulled high. In most applications it can be left floating. In unusually noisy applications, the input should be bypassed with a 1nF ceramic capacitor. This input has TTL compatible thresholds.

FB1, FB2: The high impedance inverting inputs of the error amplifiers.

GND: To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together. However, use care to avoid coupling noise into GND.

OUT1, OUT2: The high current push-pull outputs of the PWM are intended to drive power MOSFET gates through a small resistor. This resistor acts as both a current limiting resistor and as a damping impedance to minimize ringing and overshoot.

PWRGND: To separate noise from the critical control circuits, this part has two different ground connections: GND and PWRGND. GND and PWRGND must be electrically connected together.

REF: The output of the 5V reference. Bypass REF to GND with a ceramic capacitor ≥0.01µF for best performance.

RT: The oscillator charging current is set by the value of the resistor connected from R_T to GND. This pin is regulated to 1V, but the actual charging current is 10V/R_T. Recommended values of R_T are between 10k and 470k. For a given frequency, higher timing resistors give higher maximum duty cycle and slightly lower overall power consumption. Supply current decreases with increased R_T by the relationship:

$$\Delta ICC = \frac{11V}{RT}$$

For more information, see the detailed oscillator block diagram.

SYNC: This logic input can be used to synchronize the oscillator to a free running oscillator in another part. This pin is edge triggered with TTL thresholds, and requires at least a 10ns wide pulse. If unused, this pin can be grounded, open circuited, or connected to REF.

VCC: The power input to the IC. This pin supplies current to all functions including the high current output stages and the precision reference. Therefore, it is critical that V_{CC} be directly bypassed to PWRGND with an 0.1µF ceramic capacitor.

APPLICATION INFORMATION

Leading Edge Blanking and Current Sense

Figure 1. shows how an external power stage is connected to the UCC3810. The gate of an external power N-channel MOSFET is connected to OUT through a small current limiting resistor. For most applications, a 10Ω resistor is adequate to limit peak current and also practical at damping resonances between the gate driver and the MOSFET input reactance. Long gate lead length increases gate capacitance and mandates a higher series gate resistor to damp the RLC tank formed by the lead, the MOSFET input reactance, and the UCC3810 driver output resistance.

The UCC3810 features internal leading edge blanking of the current sense signal on both current sense inputs. The blank time starts when OUT rises and continues for 55ns. During that 55ns period, the signal on CS is ignored. For most PWM applications, this means that the CS input can be connected to the current sense resistor as shown above. However, high speed grounding practices and short lead lengths are still required for good performance.

APPLICATION INFORMATION (cont.)

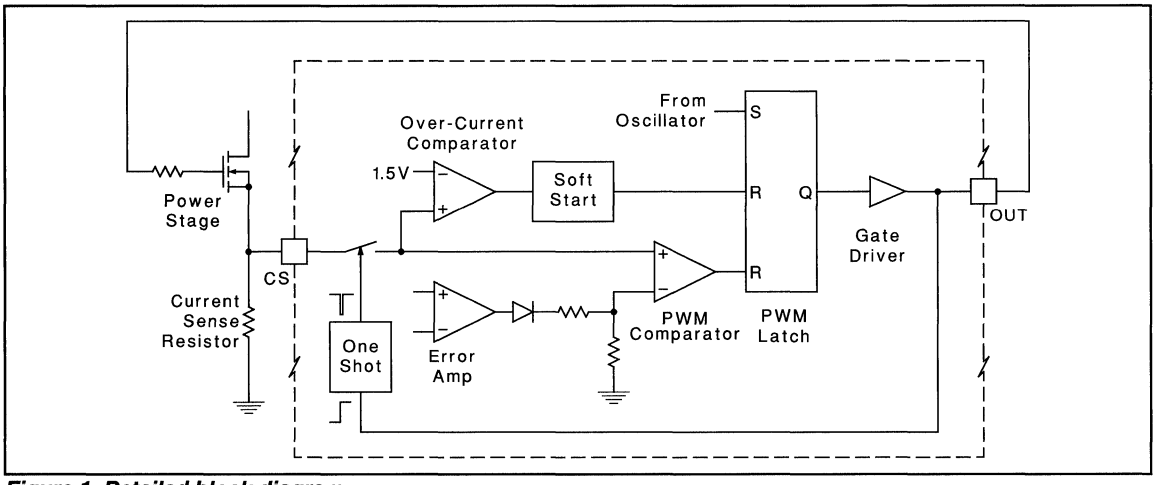


Figure 1. Detailed block diagram.

Oscillator

The UCC3810 oscillator generates a sawtooth wave at CT. The sawtooth rise time is set by the resistor from RT to GND. Since RT is biased at 1V, the current in RT is 1V/RT. The actual charging current is 10 times higher. The fall time is set by an internal transistor on-resistance of approximately 100Ω. During the fall time, all outputs are off and the maximum duty cycle is reduced below 50%. Larger timing capacitors increase the discharge time and reduce frequency. However, the percentage maximum duty cycle is only a function of the timing resistor RT and the internal 100Ω discharge resistance.

Error Amp Output Stage

The UCC3810 error amplifiers are operational amplifiers with low output resistance and high input resistance. The output stage of one error amplifier is shown above. This output stage allows the error amplifier output to swing close to GND and as high as one diode drop below 5V with little loss in amplifier performance.

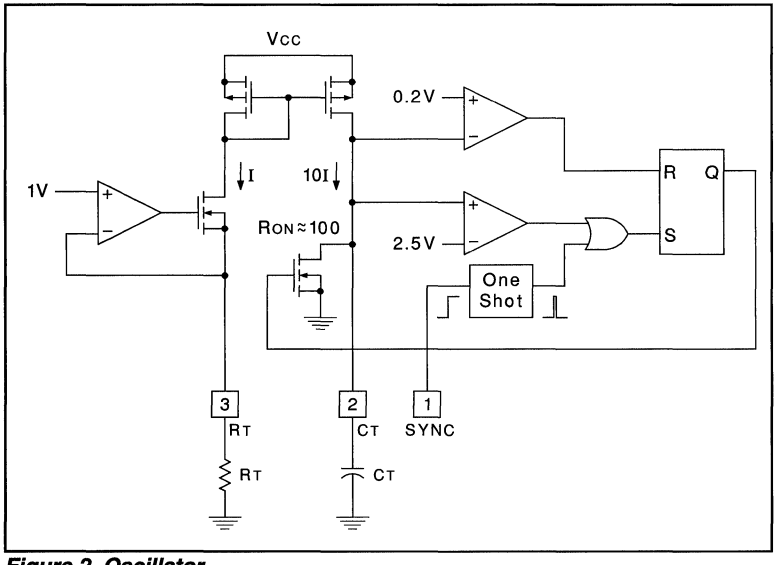


Figure 2. Oscillator.

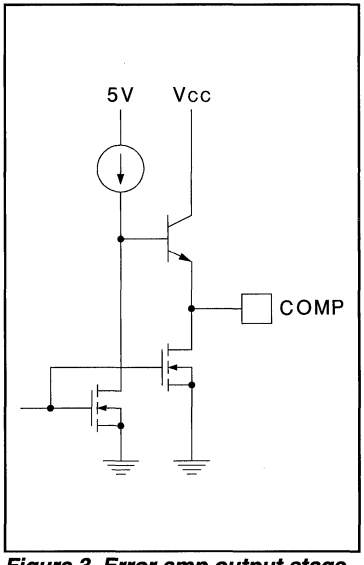


Figure 3. Error amp output stage.

TYPICAL CHARACTERISTICS

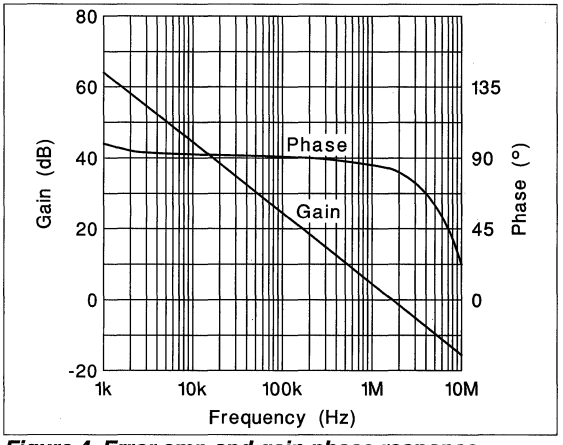


Figure 4. Error amp and gain phase response.

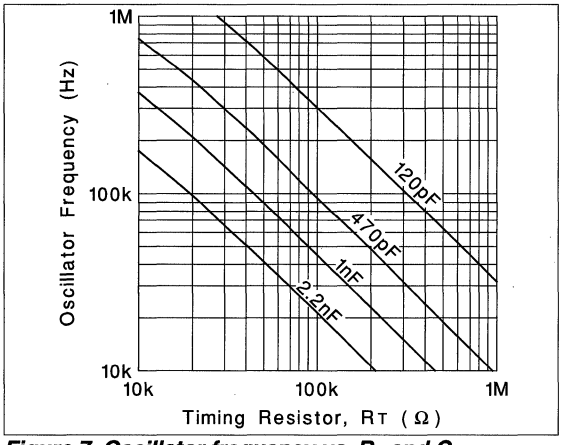


Figure 7. Oscillator frequency vs. R_T and C_T.

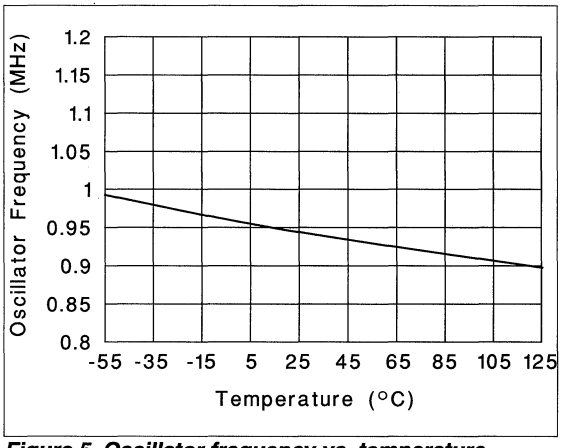


Figure 5. Oscillator frequency vs. temperature.

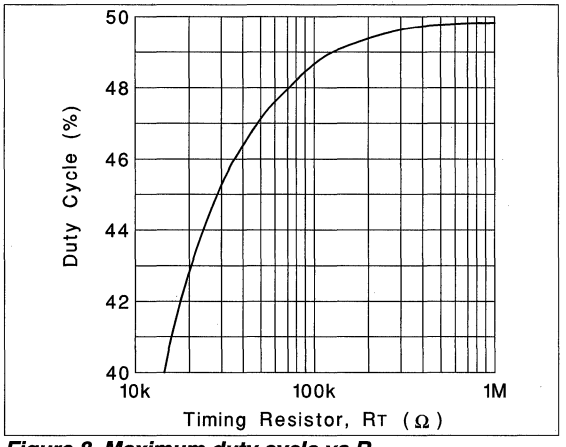


Figure 8. Maximum duty cycle vs R_T.

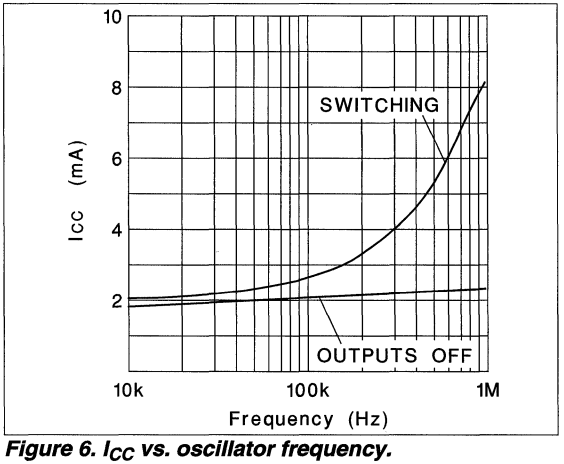


Figure 6. I_{CC} vs. oscillator frequency.

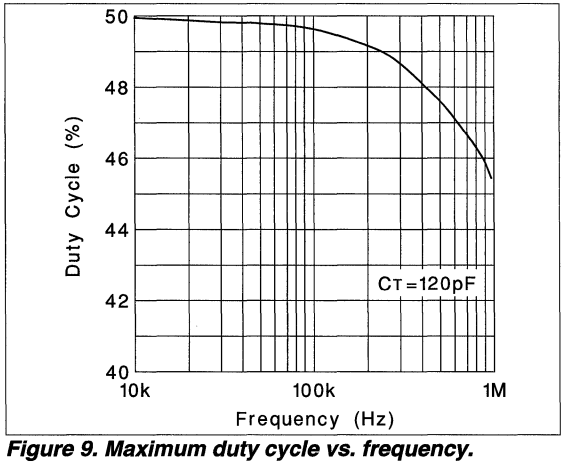


Figure 9. Maximum duty cycle vs. frequency.

APPLICATION INFORMATION (cont.)

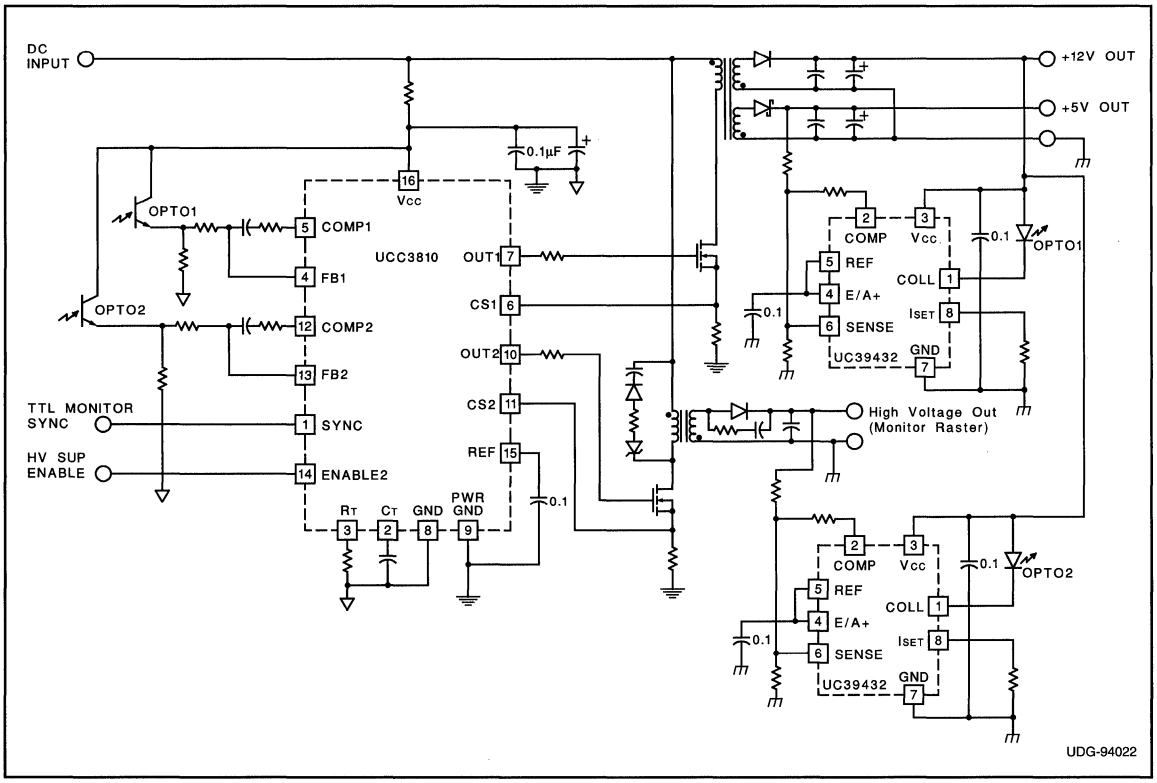


Figure 10. Typical application.

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application INFO available

UCC2813-0/-1/-2/-3/-4/-5
UCC3813-0/-1/-2/-3/-4/-5

Low Power Economy BiCMOS Current Mode PWM

FEATURES

- 100µA Typical Starting Supply Current
- 500µA Typical Operating Supply Current
- Operation to 1MHz
- Internal Soft Start
- Internal Fault Soft Start
- Internal Leading-Edge Blanking of the Current Sense Signal
- 1 Amp Totem-Pole Output
- 70ns Typical Response from Current-Sense to Gate Drive Output
- 1.5% Tolerance Voltage Reference
- Same Pinout as UCC3802, UC3842, and UC3842A

DESCRIPTION

The UCC3813-0/-1/-2/-3/-4/-5 family of high-speed, low-power integrated circuits contain all of the control and drive components required for off-line and DC-to-DC fixed frequency current-mode switching power supplies with minimal parts count.

These devices have the same pin configuration as the UC3842/3/4/5 family, and also offer the added features of internal full-cycle soft start and internal leading-edge blanking of the current-sense input.

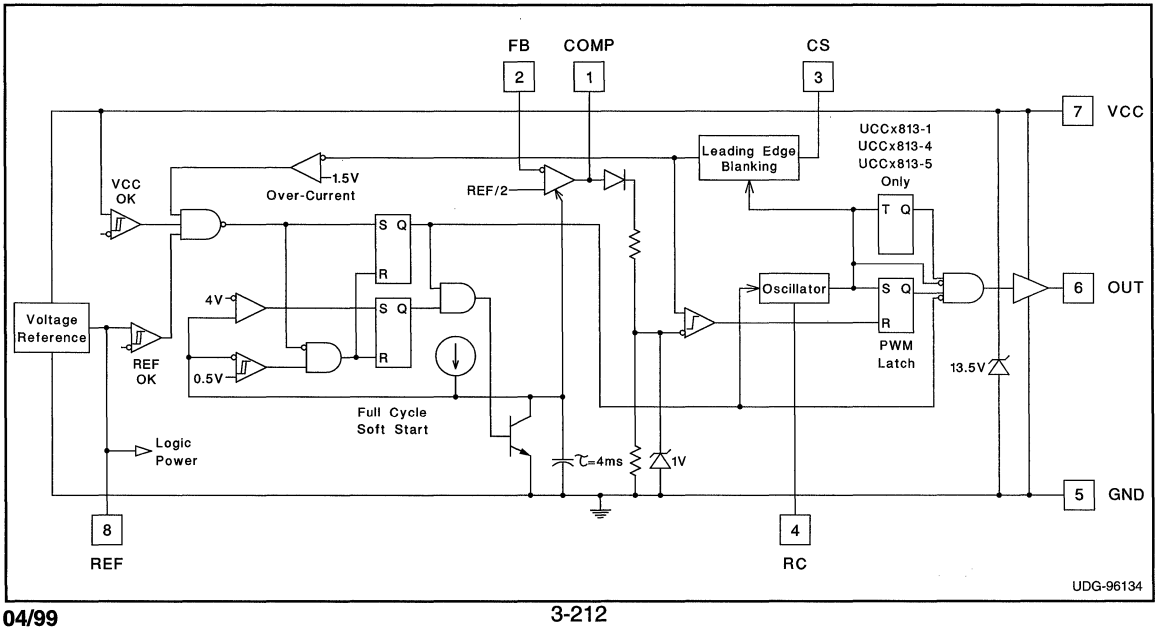
The UCC3813-0/-1/-2/-3/-4/-5 family offers a variety of package options, temperature range options, choice of maximum duty cycle, and choice of critical voltage levels. Lower reference parts such as the UCC3813-3 and UCC3813-5 fit best into battery operated systems, while the higher reference and the higher UVLO hysteresis of the UCC3813-2 and UCC3813-4 make these ideal choices for use in off-line power supplies.

The UCC2813-x series is specified for operation from –40°C to +85°C and the UCC3813-x series is specified for operation from 0°C to +70°C.

ORDERING INFORMATION

Part Number	Maximum Duty Cycle	Reference Voltage	Turn-On Threshold	Turn-Off Threshold
UCCx813-0	100%	5V	7.2V	6.9V
UCCx813-1	50%	5V	9.4V	7.4V
UCCx813-2	100%	5V	12.5V	8.3V
UCCx813-3	100%	4V	4.1V	3.6V
UCCx813-4	50%	5V	12.5V	8.3V
UCCx813-5	50%	4V	4.1V	3.6V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

VCC Voltage (Note 2) 12.0V
VCC Current 30.0mA
OUT Current ..... ±1.0A
OUT Energy (Capacitive Load) 20.0µJ
Analog Inputs (FB, CS) ..... –0.3V to 6.3V
Power Dissipation at T_A < +25°C (N Package) 1.0W
Power Dissipation at T_A < +25°C (D Package) 0.65W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages are with respect to GND. All currents are positive into the specified terminal. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

Note 2: In normal operation VCC is powered through a current limiting resistor. Absolute maximum of 12V applies when VCC is driven from a low impedance source such that ICC does not exceed 30mA.

	TEMPERATURE RANGE	PACKAGES
UCC2813	–40°C TO +85°C	N, D, PW
UCC3813	0°C TO +70°C	N, D, PW

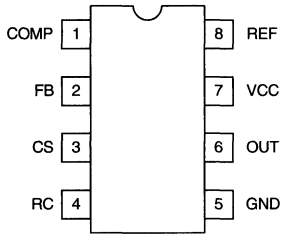
ORDERING INFORMATION

UCC□813□-□

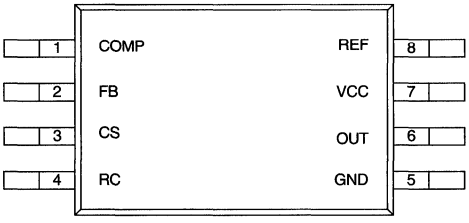
- PRODUCT OPTION
- PACKAGE
- TEMPERATURE RANGE

CONNECTION DIAGRAMS

DIL-8 or SOIC-8 (TOP VIEW)
N or D PACKAGE



TSSOP-8 (TOP VIEW)
PW PACKAGE



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. T_A = T_J.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
Reference Section					
Output Voltage	T_J = +25°C, I = 0.2mA, UCCx813-0/-1/-2/-4	4.925	5.00	5.075	V
	T_J = +25°C, I = 0.2mA, UCCx813-5	3.94	4.00	4.06	V
Load Regulation	0.2mA < I < 5mA		10	30	mV
Total Variation	UCCx813 -0-1/-2/-4 (Note 7)	4.84	5.00	5.10	V
	UCCx813-5 (Note 7)	3.84	4.00	4.08	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = +25°C (Note 9)		70		µV
Long Term Stability	T_A = +125°C, 1000 Hours (Note 9)		5		mV
Output Short Circuit		–5		–35	mA
Oscillator Section					
Oscillator Frequency	UCCx813-0/-1/-2/-4 (Note 4)	40	46	52	kHz
	UCCx813-5 (Note 4)	26	31	36	kHz
Temperature Stability	(Note 9)		2.5		%
Amplitude Peak-to-Peak		2.25	2.40	2.55	V
Oscillator Peak Voltage			2.45		V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1µF capacitor from VCC to GND; 0.1µF capacitor from VREF to GND. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
Error Amplifier Section					
Input Voltage	COMP = 2.5V; UCCx813-0/-1/-2/-4	2.42	2.50	2.56	V
	COMP = 2.0V; UCCx813-3/-5	1.92	2.0	2.05	V
Input Bias Current		–2		2	µA
Open Loop Voltage Gain		60	80		dB
COMP Sink Current	FB = 2.7V, COMP = 1.1V	0.4		2.5	mA
COMP Source Current	FB = 1.8V, COMP = REF – 1.2V	–0.2	–0.5	–0.8	mA
Gain Bandwidth Product	(Note 9)		2		MHz
PWM Section					
Maximum Duty Cycle	UCCx813-0/-2/-3	97	99	100	%
	UCCx813-1/-4/-5	48	49	50	
Minimum Duty Cycle	COMP = 0V			0	%
Current Sense Section					
Gain	(Note 5)	1.10	1.65	1.80	V/V
Maximum Input Signal	COMP = 5V (Note 6)	0.9	1.0	1.1	V
Input Bias Current		–200		200	nA
CS Blank Time		50	100	150	ns
Over-Current Threshold		1.32	1.55	1.70	V
COMP to CS Offset	CS = 0V	0.45	0.90	1.35	V
Output Section					
OUT Low Level	I = 20mA, all parts		0.1	0.4	V
	I = 200mA, all parts		0.35	0.90	V
	I = 50mA, VCC = 5V, UCCx813-3/-5		0.15	0.40	V
	I = 20mA, VCC = 0V, all parts		0.7	1.2	V
OUT High V_{SAT} (V_{CC}-OUT)	I = –20mA, all parts		0.15	0.40	V
	I = –200mA, all parts		1.0	1.9	V
	I = –50mA,VCC = 5V, UCCx813-3/-5		0.4	0.9	V
Rise Time	C_L = 1nF		41	70	ns
Fall Time	C_L = 1nF		44	75	ns
Undervoltage Lockout Section					
Start Threshold (Note 8)	UCCx813-0	6.6	7.2	7.8	V
	UCCx813-1	8.6	9.4	10.2	V
	UCCx813-2/-4	11.5	12.5	13.5	V
	UCCx813-3/-5	3.7	4.1	4.5	V
Stop Threshold (Note 8)	UCC1813-0	6.3	6.9	7.5	V
	UCC1813-1	6.8	7.4	8.0	V
	UCCx813-2/-4	7.6	8.3	9.0	V
	UCCx813-3/-5	3.2	3.6	4.0	V
Start to Stop Hysteresis	UCCx813-0	0.12	0.3	0.48	V
	UCCx813-1	1.6	2	2.4	V
	UCCx813-2/-4	3.5	4.2	5.1	V
	UCCx813-3/-5	0.2	0.5	0.8	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for –40°C ≤ T_A ≤ +85°C for UCC2813-x; 0°C ≤ T_A ≤ +70°C for UCC3813-x; VCC = 10V (Note 3); RT = 100k from REF to RC; CT=330pF from RC to GND; 0.1μF capacitor from VCC to GND; 0.1μF capacitor from VREF to GND. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UCC2813-x UCC3813-x			UNITS
		MIN	TYP	MAX	
Soft Start Section					
COMP Rise Time	FB = 1.8V, Rise from 0.5V to REF–1V		4		ms
Overall Section					
Start-up Current	VCC < Start Threshold		0.1	0.23	mA
Operating Supply Current	FB = 0V, CS = 0V, RC = 0V		0.5	1.2	mA
VCC Internal Zener Voltage	ICC = 10mA (Note 8)	12	13.5	15	V
VCC Internal Zener Voltage Minus Start Threshold Voltage	UCCx813-2/-4	0.5	1.0		V

Note 3: Adjust VCC above the start threshold before setting at 10V.

Note 4: Oscillator frequency for the UCCx813-0, UCCx813-2 and UCCx813-3 is the output frequency. Oscillator frequency for the UCCx813-1, UCCx813-4 and UCCx813-5 is twice the output frequency.

Note 5: Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}$ $0 \le V_{CS} \le 0.8V$.

Note 6: Parameter measured at trip point of latch with Pin 2 at 0V.

Note 7: Total Variation includes temperature stability and load regulation.

Note 8: Start Threshold, Stop Threshold and Zener Shunt Thresholds track one another.

Note 9: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator.

Unlike other devices, the error amplifier in the UCC3813 family is a true, low output-impedance, 2MHz operational amplifier. As such, the COMP terminal can both source and sink current. However, the error amplifier is internally current limited, so that you can command zero duty cycle by externally forcing COMP to GND.

The UCC3813 family features built-in full cycle Soft Start. Soft Start is implemented as a clamp on the maximum COMP voltage.

FB: FB is the inverting input of the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

CS: CS is the input to the current sense comparators. The UCC3813 family has two different current sense comparators: the PWM comparator and an over-current comparator.

The UCC3813 family contains digital current sense filtering, which disconnects the CS terminal from the current sense comparator during the 100ns interval immediately following the rising edge of the OUT pin. This digital filtering, also called leading-edge blanking, means that in most applications, no analog filtering (RC filter) is required on CS. Compared to an external RC filter technique, the leading-edge blanking provides a smaller effective CS to OUT propagation delay. Note, however, that the minimum non-zero On-Time of the OUT signal is directly affected by the leading-edge-blanking and the CS to OUT propagation delay.

The over-current comparator is only intended for fault sensing, and exceeding the over-current threshold will cause a soft start cycle.

RC: RC is the oscillator timing pin. For fixed frequency operation, set timing capacitor charging current by connecting a resistor from REF to RC. Set frequency by connecting a timing capacitor from RC to GND. For best performance, keep the timing capacitor lead to GND as short and direct as possible. If possible, use separate ground traces for the timing capacitor and all other functions.

PIN DESCRIPTIONS (cont.)

The frequency of oscillation can be estimated with the following equations:

$$\text{UCCx813-0/-1/-2/-4:}\quad F = \frac{1.5}{R \bullet C}$$

$$\text{UCCx813-3, UCCx813-5:}\quad F = \frac{1.0}{R \bullet C}$$

where frequency is in Hz, resistance is in Ω, and capacitance is in farads. The recommended range of timing resistors is between 10k and 200k and timing capacitor is 100pF to 1000pF. Never use a timing resistor less than 10k.

GND: GND is reference ground and power ground for all functions on this part.

OUT: OUT is the output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±750mA. OUT is actively held low when VCC is below the UVLO threshold.

The high-current power driver consists of FET output devices, which can switch all of the way to GND and all of the way to VCC. The output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

VCC: VCC is the power input connection for this device. In normal operation VCC is powered through a current limiting resistor. Although quiescent VCC current is very low, total supply current will be higher, depending on OUT current. Total VCC current is the sum of quiescent VCC current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g \bullet F.$$

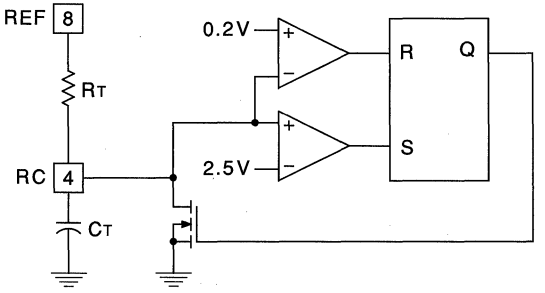
To prevent noise problems, bypass VCC to GND with a ceramic capacitor as close to the VCC pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor.

REF: REF is the voltage reference for the error amplifier and also for many other functions on the IC. REF is also used as the logic power supply for high speed switching logic on the IC.

When VCC is greater than 1V and less than the UVLO threshold, REF is pulled to ground through a 5kΩ resistor. This means that REF can be used as a logic output indicating power system status. It is important for reference stability that REF is bypassed to GND with a ceramic capacitor as close to the pin as possible. An electrolytic capacitor may also be used in addition to the ceramic capacitor. A minimum of 0.1µF ceramic is required. Additional REF bypassing is required for external loads greater than 2.5mA on the reference.

To prevent noise problems with high speed switching transients, bypass REF to ground with a ceramic capacitor very close to the IC package.

APPLICATION INFORMATION



The UCC3813-0/-1/-2/-3/-4/-5 oscillator generates a sawtooth waveform on RC. The rise time is set by the time constant of R_T and C_T. The fall time is set by CT and an internal transistor on-resistance of approximately 125Ω. During the fall time, the output is off and the maximum duty cycle is reduced below 50% or 100% depending on the part number. Larger timing capacitors increase the discharge time and reduce the maximum duty cycle and frequency.

Figure 1. Oscillator.

APPLICATION INFORMATION (cont.)

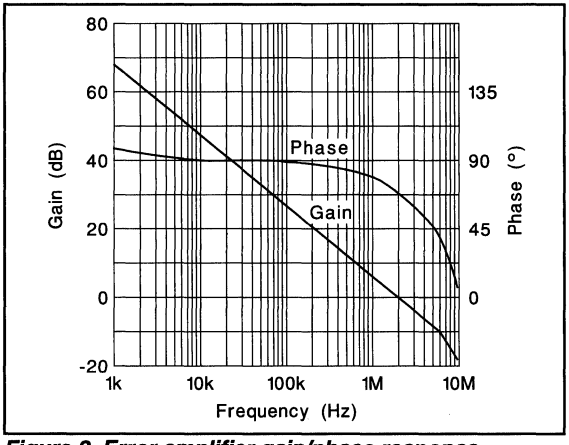


Figure 2. Error amplifier gain/phase response.

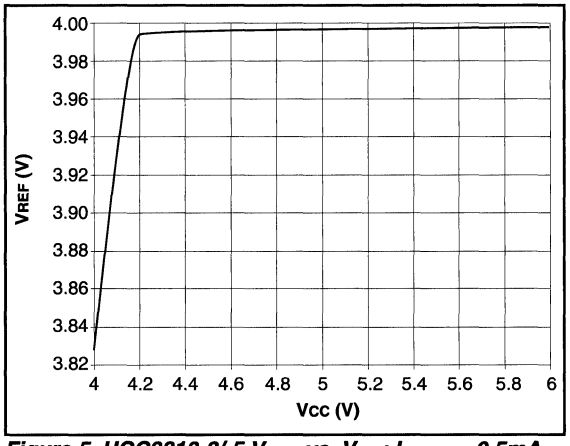


Figure 5. UCC3813-3/-5 V_{REF} vs. V_{CC}; I_{LOAD} = 0.5mA.

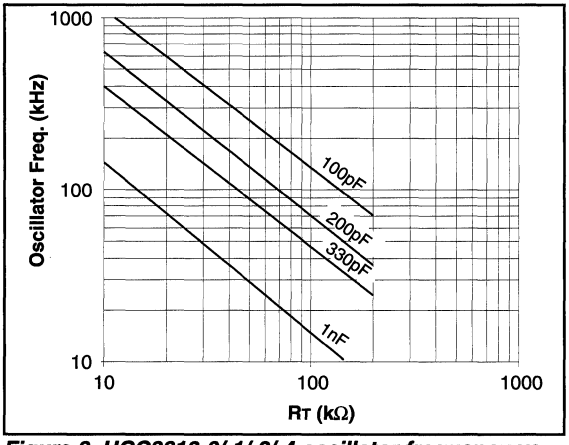


Figure 3. UCC3813-0/-1/-2/-4 oscillator frequency vs. R_T and C_T.

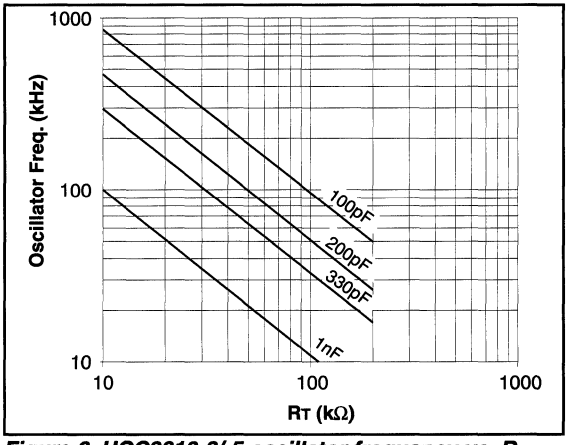


Figure 6. UCC3813-3/-5 oscillator frequency vs. R_T and C_T.

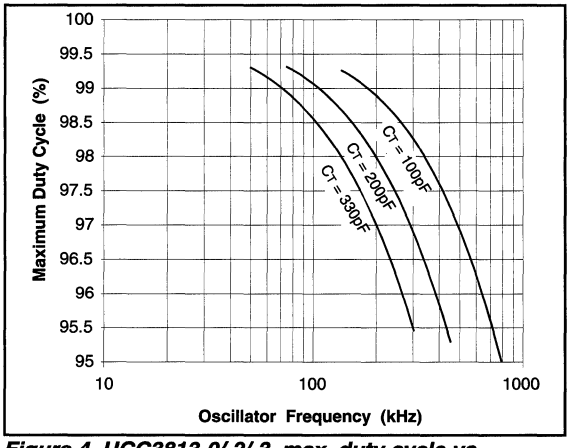


Figure 4. UCC3813-0/-2/-3 max. duty cycle vs. oscillator frequency.

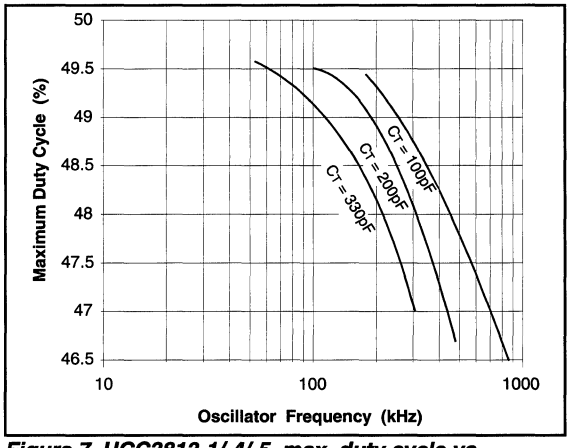


Figure 7. UCC3813-1/-4/-5 max. duty cycle vs. oscillator frequency.

APPLICATION INFORMATION (cont.)

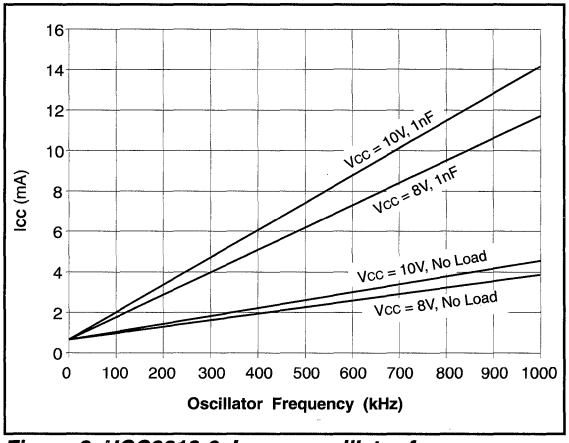


Figure 8. UCC3813-0 I_{CC} vs. oscillator frequency.

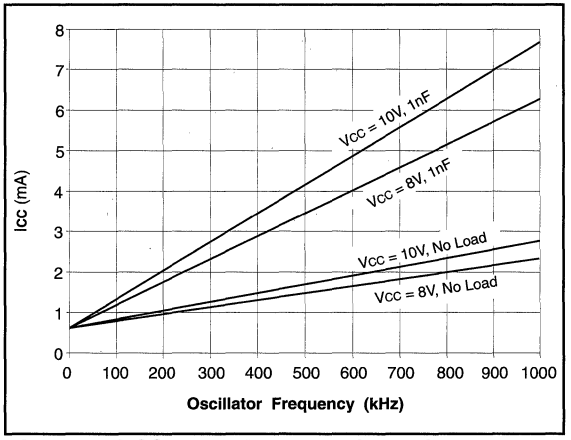


Figure 10. UCC3813-5 I_{CC} vs. oscillator frequency.

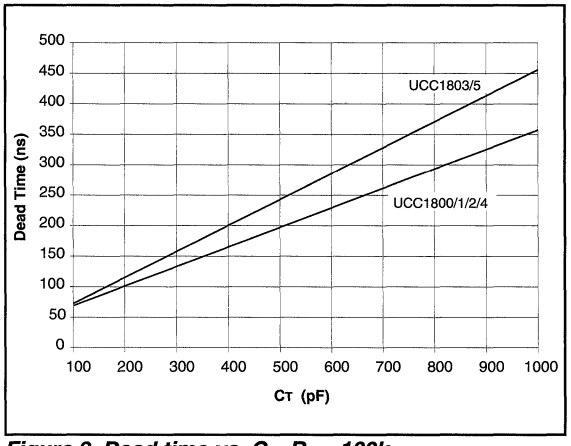


Figure 9. Dead time vs. C_T, R_T = 100k.

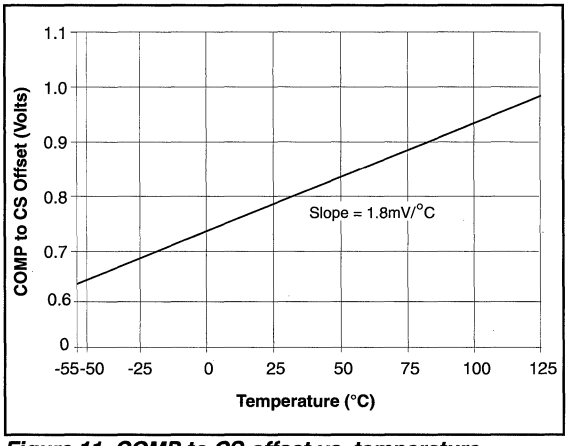


Figure 11. COMP to CS offset vs. temperature, CS = 0V.

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UNITRODE

application INFO available

UC1823
UC2823
UC3823

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current-Mode Topologies
- Practical Operation @ Switching Frequencies to 1.0MHz
- 50ns Propagation Delay to Output
- High Current Totem Pole Output (1.5A peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start/Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)
- Trimmed Bandgap Reference (5.1V ±1%)

DESCRIPTION

The UC1823 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage-mode systems with the capability for input voltage feed-forward.

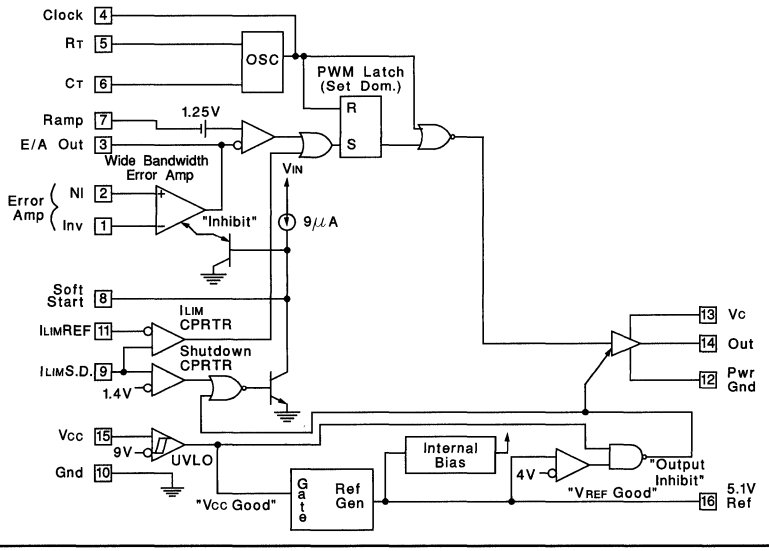
Protection circuitry includes a current limit comparator, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at the output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the output is high impedance. The current limit reference (pin 11) is a DC input voltage to the current limit comparator. Consult specifications for details.

These devices feature a totem pole output designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is defined as a high level.

ABSOLUTE MAXIMUM RATINGS

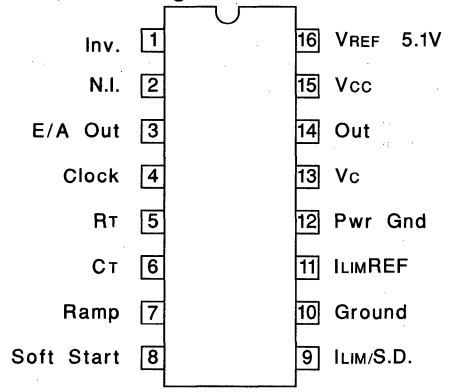
Supply Voltage (Pins 15, 13) 30V
Output Current, Source or Sink (Pin14)
  DC 0.5A
  Pulse (0.5µs) 2.0A
Analog Inputs (Pins 1, 2, 7, 8, 9, 11) . . . . . –0.3V to +6V
Clock Output Current (Pin 4) . . . . . –5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . . –5mA
Power Dissipation at T_A = 60 °C 1W
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C
Note: All voltages are with respect to ground, Pin 10.
Currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations

BLOCK DIAGRAM

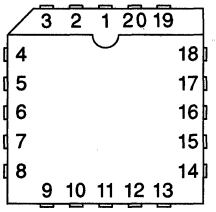


CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
Inv.	2
N.I.	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft start	10
N/C	11
ILIM/S.D.	12
Ground	13
ILIM REF	14
PWR Gnd	15
N/C	16
VC	17
OUT	18
VCC	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10 < V_{CC} < 30V		2	20		2	20	mV
Load Regulation	1 < I_O < 10mA		5	20		5	20	mV
Temperature Stability*	T_{MIN} < T_A < T_{MAX}		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temp.	5.00		5.20	4.95		5.25	
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	T_J = 125°C, 1000 hrs.		5	25		5	25	mV
Short Circuit Current	V_{REF}=0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	T_J=25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10 < V_{CC} < 30V		0.2	2		0.2	2	%
Temperature Stability*	T_{MIN} <T_A < T_{MAX}		5			5		%
Total Variation*	Line, Temp.	340		460	340		460	kHz
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V

ELECTRICAL CHARACTERISTICS: Unless otherwise noted, these specifications apply for R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, 0°C < T_A < +70°C for the UC3823, -25°C < T_A < +85°C for the UC2823, and -55°C < T_A < +125°C for the UC1823, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1823 UC2823			UC3823			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1 < V_O < 4V	60	95		60	95		dB
CMRR	1.5 < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10 < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ =1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0.5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µS
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero D.C. Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit/Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			±10			±10	µA
Current Limit Offset	$V_{PIN\ 11}$ = 1.1V			15			15	mV
Current Limit Common Mode Range ($V_{PIN\ 11}$)		1.0		1.25	1.0		1.25	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output*			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		100	500	µA
Rise/Fall Time*	C_L = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
I_{CC}	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ =0V, $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

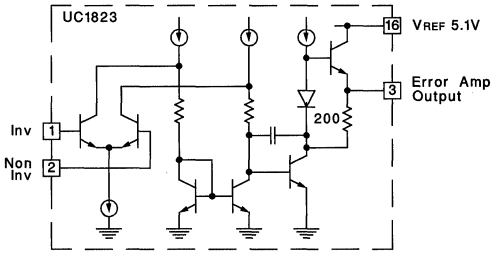
* These parameters are guaranteed by design but not 100% tested in production.

UC1823 PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

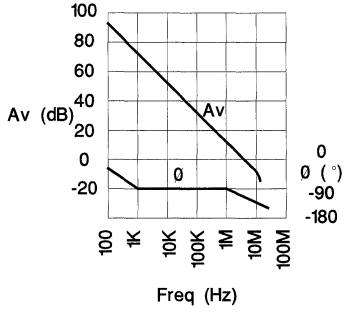
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1823, follow these rules. 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFET. Don't allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass V_{CC}, V_C, and V_{REF}. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, C_T, like a bypass capacitor.

ERROR AMPLIFIER CIRCUIT

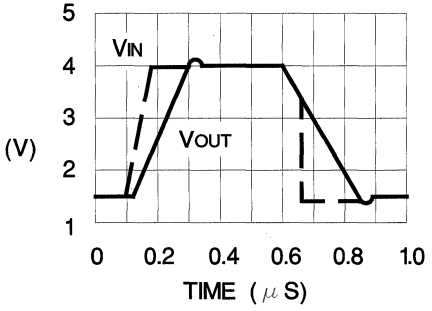
Simplified Schematic



Open Loop Frequency Response

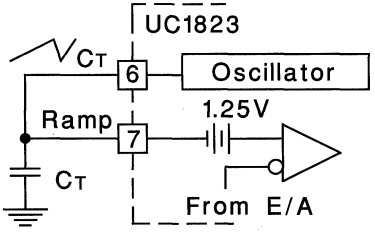


Unity Gain Slew Rate

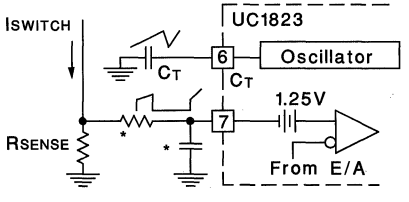


PWM APPLICATIONS

Conventional (Voltage Mode)

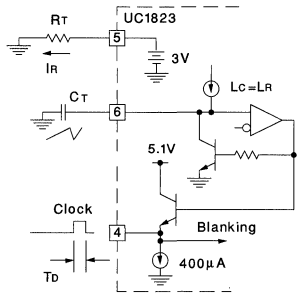


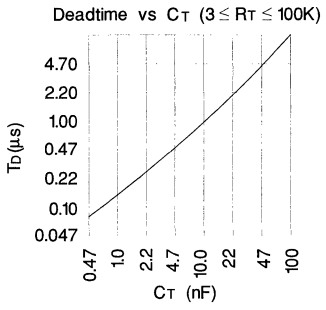
Current-Mode

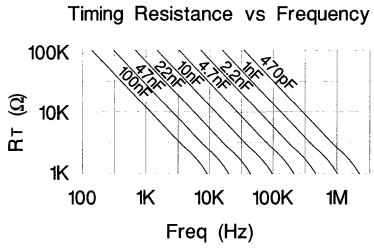


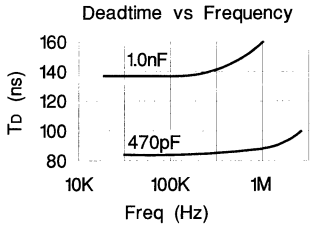
* A small filter may be required to suppress switch noise

OSCILLATOR CIRCUIT



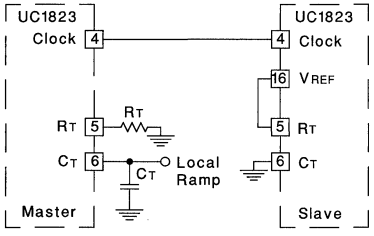




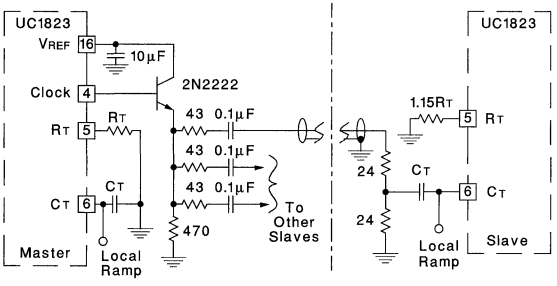


SYNCHRONIZED OPERATION

Two Units in Close Proximity

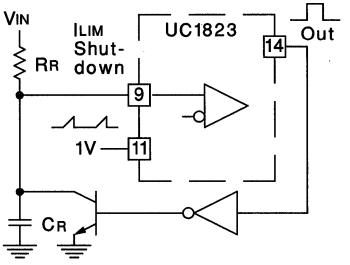


Generalized Synchronization

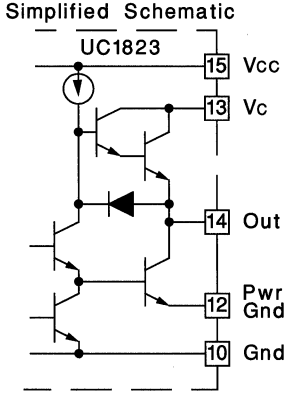


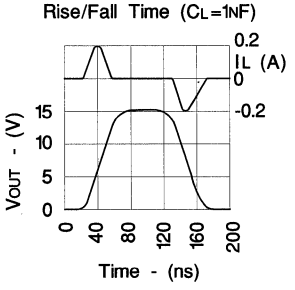
CONSTANT VOLT-SECOND CLAMP CIRCUIT

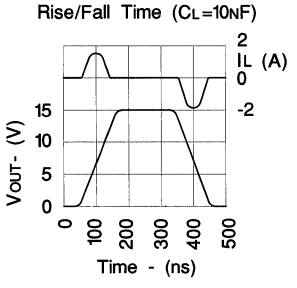
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the inverter must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

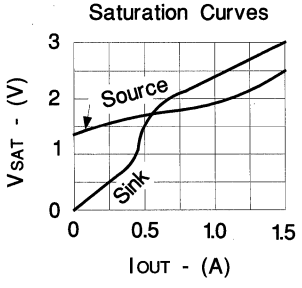


OUTPUT SECTION

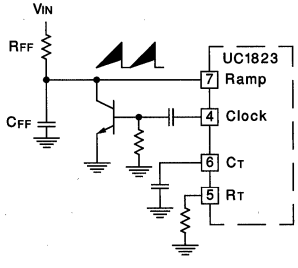








FEED FORWARD TECHNIQUE FOR OFF-LINE VOLTAGE MODE APPLICATION



UNITRODE CORPORATION
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UNITRODE

application INFO available

UC1823A,B/1825A,B
UC2823A,B/2825A,B
UC3823A,B/3825A,B

High Speed PWM Controller

FEATURES

- Improved versions of the UC3823/UC3825 PWMs
- Compatible with Voltage or Current-Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (2A Peak)
- Trimmed Oscillator Discharge Current
- Low 100µA Startup Current
- Pulse-by-Pulse Current Limiting Comparator
- Latched Overcurrent Comparator With Full Cycle Restart

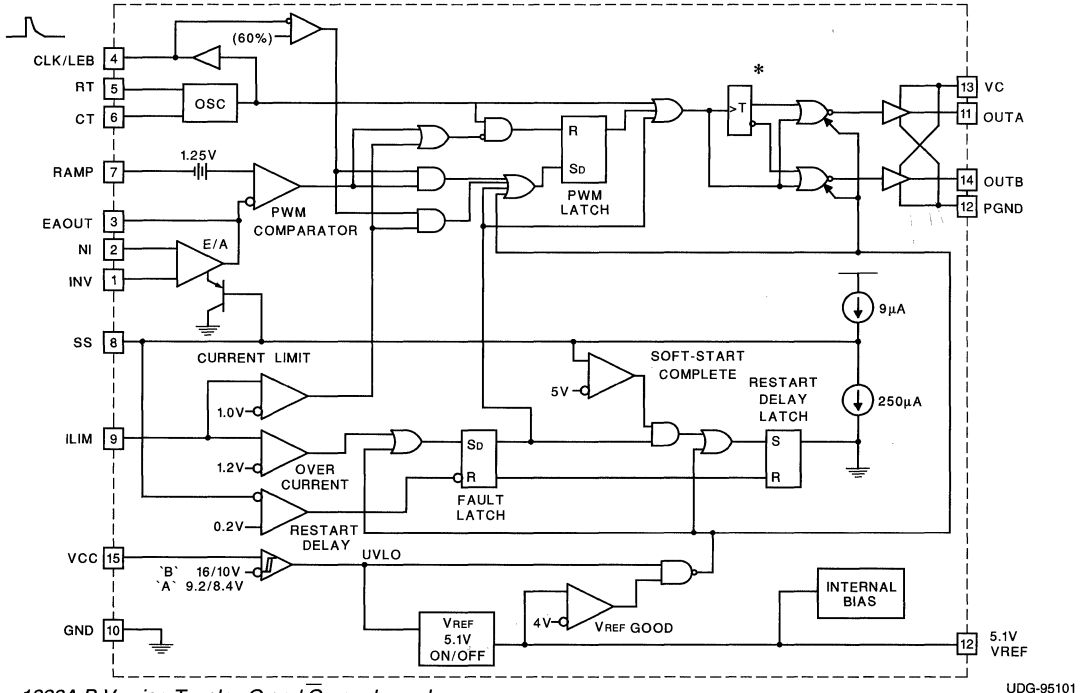
DESCRIPTION

The UC3823A & B and the UC3825A & B family of PWM control ICs are improved versions of the standard UC3823 & UC3825 family. Performance enhancements have been made to several of the circuit blocks. Error amplifier gain bandwidth product is 12MHz while input offset voltage is 2mV. Current limit threshold is guaranteed to a tolerance of 5%. Oscillator discharge current is specified at 10mA for accurate dead time control. Frequency accuracy is improved to 6%. Startup supply current, typically 100µA, is ideal for off-line applications. The output drivers are redesigned to actively sink current during UVLO at no expense to the startup current specification. In addition each output is capable of 2A peak currents during transitions.

Functional improvements have also been implemented in this family. The UC3825 shutdown comparator is now a high-speed overcurrent comparator with a threshold of 1.2V. The overcurrent comparator sets a latch that ensures full discharge of the soft start capacitor before allowing a restart. While the fault latch is set, the outputs are in the low state. In the event of continuous faults, the soft start capacitor is fully charged before discharge to insure that the fault frequency does not exceed the designed soft start period. The UC3825 Clock pin has become CLK/LEB. This pin combines the functions of clock output and leading edge blanking adjustment and has been buffered for easier interfacing.

(continued)

BLOCK DIAGRAM



** Note: 1823A,B Version Toggles Q and $\overline{Q}$ are always low*

UDG-95101

DESCRIPTION (cont.)

The UC3825A,B has dual alternating outputs and the same pin configuration of the UC3825. The UC3823A,B outputs operate in phase with duty cycles from zero to less than 100%. The pin configuration of the UC3823A,B is the same as the UC3823 except pin 11 is now an output pin instead of the reference pin to the current limit comparator. "A" version parts have UVLO thresholds identical to the original UC3823/25. The "B" versions have UVLO thresholds of 16 and 10V, intended for ease of use in off-line applications.

Consult Application Note U-128 for detailed technical and applications information. Contact the factory for further packaging and availability information.

Device	UVLO	Dmax
UC3823A	9.2V/8.4V	< 100%
UC3823B	16V/10V	< 100%
UC3825A	9.2V/8.4V	< 50%
UC3825B	16V/10V	< 50%

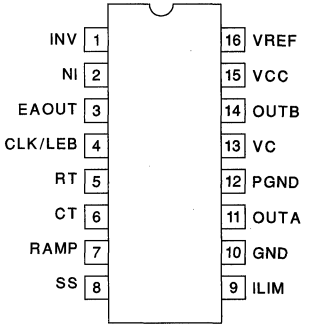
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VCC) 22V
Output Current, Source or Sink (Pins OUTA, OUTB)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground (PGND) ..... ±0.2V
Analog Inputs
(INV, NI, RAMP) ..... –0.3V to 7V
(ILIM, SS) ..... –0.3V to 6V
Clock Output Current (CLK/LEB) ..... –5mA
Error Amplifier Output Current (EAOUT) 5mA
Soft Start Sink Current (SS) 20mA
Oscillator Charging Current (RT) ..... –5mA
Power Dissipation at T_A = 60°C 1W
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

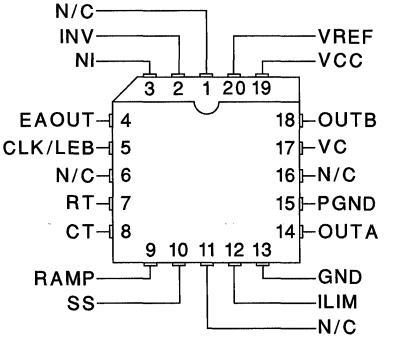
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16, (Top View)
J or N Package; DW Package



PLCC-20, LCC-20, (Top View)
Q, L Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_J = 25°C, Io = 1mA	5.05	5.1	5.15	V
Line Regulation	12 < VCC < 20V		2	15	mV
Load Regulation	1mA < I_O < 10mA		5	20	mV
Total Output Variation	Line, Load, Temp	5.03		5.17	V
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 1)		0.2	0.4	mV/°C
Output Noise Voltage	10Hz < f < 10kHz (Note 1)		50		µVRMS
Long Term Stability	T_J = 125°C, 1000 hours (Note 1)		5	25	mV
Short Circuit Current	VREF = 0V	30	60	90	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
Initial Accuracy	T_J = 25°C (Note 1)	375	400	425	kHz
Total Variation	Line, Temperature (Note 1)	350		450	kHz
Voltage Stability	12V < VCC < 20V			1	%
Temperature Stability	$T_{MIN} < T_A < T_{MAX}$ (Note 1)		5		%
Initial Accuracy	RT = 6.6k, CT = 220pF, T_A = 25°C (Note 1)	0.9	1	1.1	MHz
Total Variation	RT = 6.6k, CT = 220pF (Note 1)	0.85		1.15	MHz
Clock Out High		3.7	4		V
Clock Out Low			0	0.2	V
Ramp Peak		2.6	2.8	3	V
Ramp Valley		0.7	1	1.25	V
Ramp Valley to Peak		1.6	1.8	2	V
Oscillator Discharge Current	RT = Open, V_{CT} = 2V	9	10	11	mA
Error Amplifier Section					
Input Offset Voltage			2	10	mV
Input Bias Current			0.6	3	µA
Input Offset Current			0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	12V < VCC < 20V	85	110		dB
Output Sink Current	V_{EAOUT} = 1V	1	2.5		mA
Output Source Current	V_{EAOUT} = 4V	–0.5	–1.3		mA
Output High Voltage	I_{EAOUT} = –0.5mA	4.5	4.7	5	V
Output Low Voltage	I_{EAOUT} = 1mA	0	0.5	1	V
Gain Bandwidth Product	F = 200kHz	6	12		MHz
Slew Rate	(Note 1)	6	9		V/µs
PWM Comparator					
RAMP Bias Current	V_{RAMP} = 0V		–1	–8	µA
Minimum Duty Cycle				0	%
Maximum Duty Cycle		85			%
Leading Edge Blanking	R = 2k, C = 470pF	300	375	450	ns
LEB Resistor	$V_{CLK/LEB}$ = 3V	8.5	10	11.5	kohm
EAOUT Zero D.C. Threshold	V_{RAMP} = 0V	1.1	1.25	1.4	V
Delay to Output	V_{EAOUT} = 2.1V, V_{RAMP} = 0 to 2V Step (Note 1)		50	80	ns
Current Limit/Start Sequence/Fault Section					
Soft Start Charge Current	V_{SS} = 2.5V	8	14	20	µA
Full Soft Start Threshold		4.3	5		V
Restart Discharge Current	V_{SS} = 2.5V	100	250	350	µA
Restart Threshold			0.3	0.5	V
ILIM Bias Current	0 < V_{ILIM} < 2V			15	µA
Current Limit Threshold		0.95	1	1.05	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1823A,B and UC1825A,B; –40°C to +85°C for the UC2823A,B and UC2825A,B; 0°C to +70°C for the UC3823A,B and UC3825A,B; RT = 3.65k, CT = 1nF, VCC = 12V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit/Start Sequence/Fault Section (cont.)					
Over Current Threshold		1.14	1.2	1.26	V
ILIM Delay to Output	V_{ILIM} = 0 to 2V Step (Note 1)		50	80	ns
Output Section					
Output Low Saturation	I_{OUT} = 20mA		0.25	0.4	V
	I_{OUT} = 200mA		1.2	2.2	V
Output High Saturation	I_{OUT} = 20mA		1.9	2.9	V
	I_{OUT} = 200mA		2	3	V
UVLO Output Low Saturation	I_O = 20mA		0.8	1.2	V
Rise/Fall Time	C_L = 1nF (Note 1)		20	45	ns
UnderVoltage Lockout					
Start Threshold	UCX823B and X825B only		16	17	V
Stop Threshold	UCX823B and X825B only	9	10		V
UVLO Hysteresis	UCX823B and X825B only	5	6	7	V
Start Threshold	UCX823A and X825A only	8.4	9.2	9.6	V
UVLO Hysteresis	UCX823A and X825A only	0.4	0.8	1.2	V
Supply Current					
Startup Current	VC = VCC = V_{TH}(start) –0.5V		100	300	µA
Icc			28	36	mA

Note 1:Guaranteed by design. Not 100% tested in production.

APPLICATIONS INFORMATION

OSCILLATOR

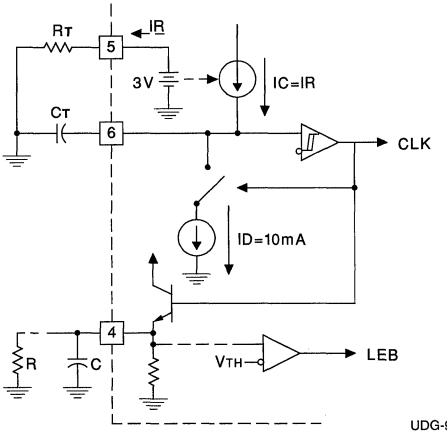
The UC3823A,B/3825A,B oscillator is a saw tooth. The rising edge is governed by a current controlled by the RT pin and value of capacitance at the CT pin. The falling edge of the sawtooth sets dead time for the outputs. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on desired frequency, RT, and D_{MAX}. The design equations are:

$$RT = \frac{3V}{(10mA)(1 - D_{MAX})}$$

$$CT = \frac{(1.6 \bullet D_{MAX})}{(RT \bullet F)}$$

Recommended values for RT range from 1k to 100k. Control of D_{MAX} less than 70% is not recommended.

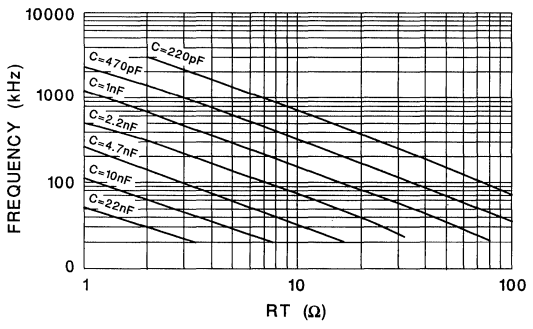
Oscillator



APPLICATIONS INFORMATION (cont.)

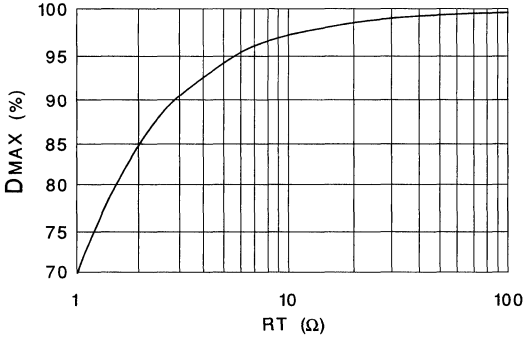
OSCILLATOR (cont.)

Oscillator Frequency vs. R_T and C_T Curve



UDG-95103

Maximum Duty Cycle vs R_T Curve



UDG-95104

LEADING EDGE BLANKING

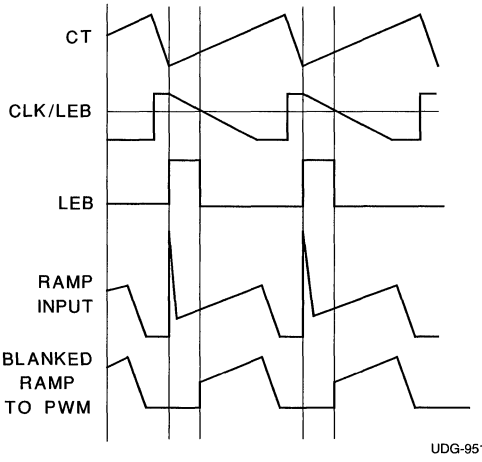
The UC3823A,B/3825A,B performs fixed frequency pulse width modulation control. The UC3823A,B outputs operate together at the switching frequency and can vary from 0 to some value less than 100%. The UC3825A,B outputs are alternately controlled. During every other cycle, one output will be off. Each output then, switches at one-half the oscillator frequency, varying in duty cycle from 0 to less than 50%.

To limit maximum duty cycle, the internal clock pulse blanks both outputs low during the discharge time of the oscillator. On the falling edge of the clock, the appropriate output(s) is driven high. The end of the pulse is controlled by the PWM comparator, current limit comparator, or the overcurrent comparator.

Normally the PWM comparator will sense a ramp crossing a control voltage (error amp output) and terminate the pulse. Leading edge blanking (LEB) causes the PWM comparator to be ignored for a fixed amount of time after the start of the pulse. This allows noise inherent with switched mode power conversion to be rejected. The PWM ramp input may not require any filtering as result of leading edge blanking.

To program a Leading Edge Blanking period, connect a capacitor, C, to CLK/LEB. The discharge time set by C and the internal 10k resistor will determine the blanked interval. The 10k resistor has a 10% tolerance. For more accuracy, an external 2k 1% resistor, R, can be added, resulting in an equivalent resistance of 1.66k with a tolerance of 2.4%. The design equation is:

LEB Operational Waveforms



UDG-95105

$t_{LEB} = 0.5 \bullet (R \mid\mid 10k) \bullet C.$

Values of R less than 2k should not be used

Leading edge blanking is also applied to the current limit comparator. After LEB, if the ILIM pin exceeds the one volt threshold, the pulse is terminated. The over current comparator, however, is not blanked. It will catch catastrophic over current faults without a blanking delay. Any time the ILIM pin exceeds 1.2V, the fault latch will be set and the outputs driven low. For this reason, some noise filtering may be required on the ILIM pin.

APPLICATIONS INFORMATION (cont.)

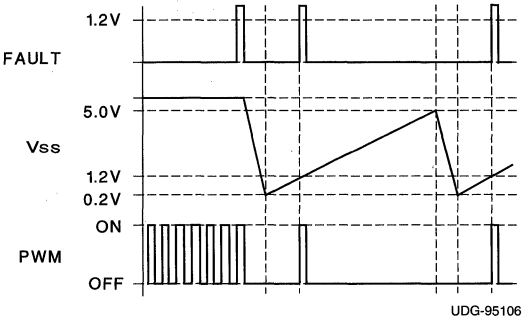
UVLO, SOFT START AND FAULT MANAGEMENT

Soft start is programmed by a capacitor on the SS pin. At power up, SS is discharged. When SS is low, the error amp output is also forced low. As the internal 9µA source charges the SS pin, the error amp output follows until closed loop regulation takes over.

Anytime ILIM exceeds 1.2V, the fault latch will be set and the output pins will be driven low. The soft start cap is then discharged by a 250µA current sink. No more output pulses are allowed until soft start is fully discharged, and ILIM is below 1.2V. At this point the fault latch will be reset and the chip will execute a soft start.

Should the fault latch be set during soft start, the outputs will be immediately terminated, but the soft start cap will not be discharged until it has been fully charged. This results in a controlled hiccup interval for continuous fault conditions.

Soft Start and Fault Waveforms

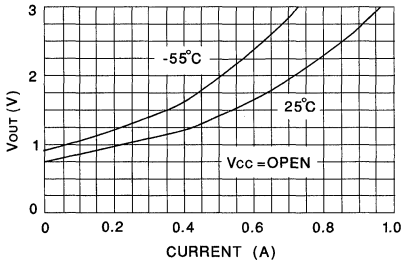


UDG-95106

ACTIVE LOW OUTPUTS DURING UVLO

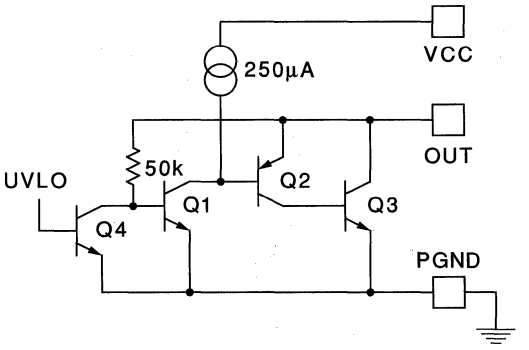
The UVLO function forces the outputs to be low and considers both VCC and VREF before allowing the chip to operate.

Simplified Schematic



UDG-95108

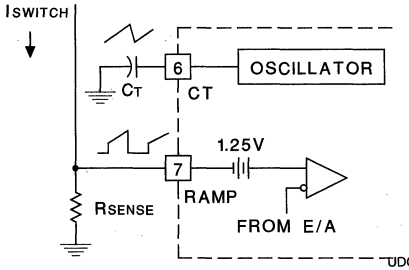
Output V and I During UVLO



UDG-95107

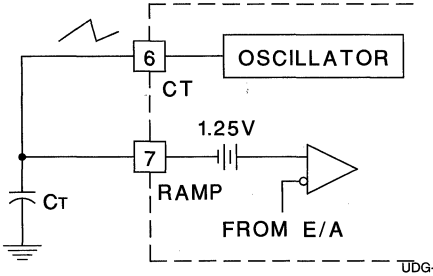
PWM APPLICATIONS

Current Mode



UDG-95109

Voltage Mode



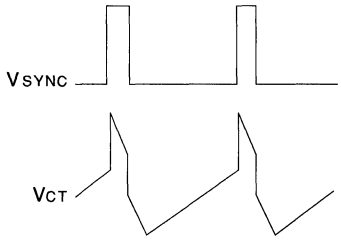
UDG-95110

APPLICATIONS INFORMATION (cont.)

SYNCHRONIZATION

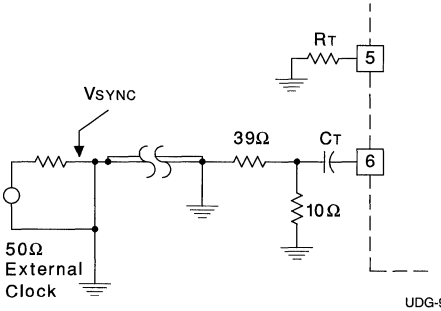
The oscillator can be synchronized by an external pulse inserted in series with the timing capacitor. Program the free running frequency of the oscillator to be 10 to 15% slower than the desired synchronous frequency. The pulse width should be greater than 10ns and less than half the discharge time of the oscillator. The rising edge of the CLK/LEB pin can be used to generate a synchronizing pulse for other chips. Note that, the CLK/LEB pin will no longer accept an incoming synchronizing signal.

Operational Waveforms



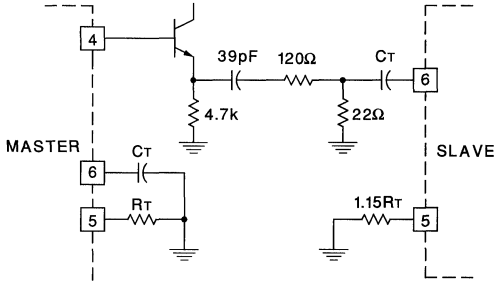
UDG-95112

General Oscillator Synchronization



UDG-95111

Two Units



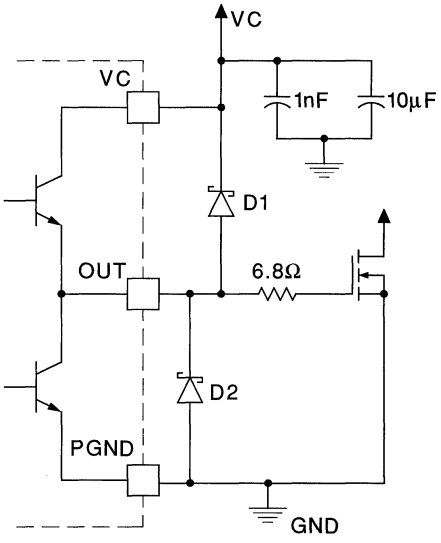
UDG-95113

HIGH CURRENT OUTPUTS

Each totem pole output of the UC3823A,B and UC3825A,B can deliver a 2 amp peak current into a capacitive load. The output can slew a 1000pF capacitor 15 volts in approximately 20 nanoseconds. Separate collector supply (VC) and power ground (PGND) pins help decouple the IC's analog circuitry from the high power gate drive noise. The use of 3 Amp Schottky diodes (1N5120, USD245 or equivalent) as shown in the figure from each output to both VC and PGND are recommended. The diodes clamp the output swing to the supply rails, necessary with any type of inductive/capacitive load, typical of a MOSFET gate. Schottky diodes must be used because a low forward voltage drop is required. DO NOT USE standard silicon diodes.

Although a "single ended" device, two output drivers are available on the UC3823A,B devices. These can be "paralleled" by the use of a one-half ohm (noninductive) resistor connected in series with each output for a combined peak current of 4 amps.

Power MOSFET Drive Circuit



D1, D2 = 1N5820

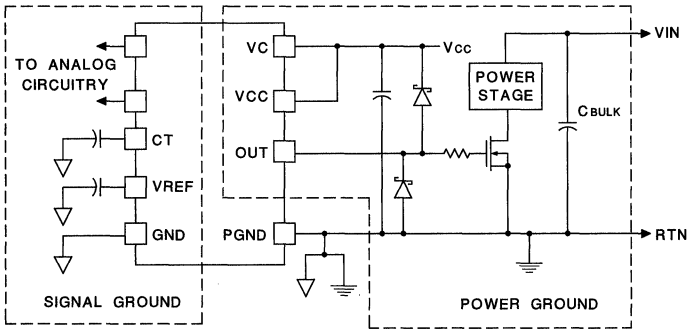
UDG-95114

APPLICATIONS INFORMATION (cont.)

GROUND PLANES

Each output driver of these devices is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stages. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

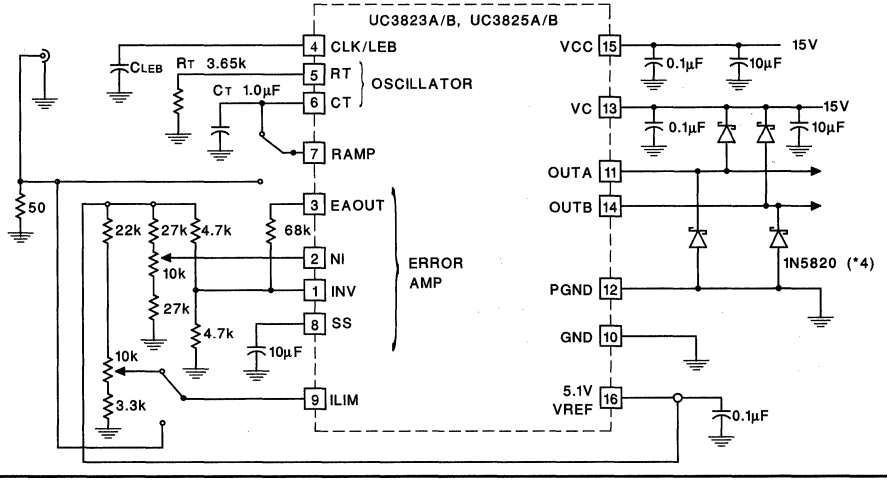
VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low ESR/ESL ceramic 1µF capacitors are recommended for both VCC and VREF. All analog circuitry should likewise be bypassed to the signal ground plane.



UDG-95115

Open Loop Test Circuit

This test fixture is useful for exercising many of the UC3823A,B, UC3825A,B functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.



UDG-95116

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Speed PWM Controller

FEATURES

- Complementary Outputs
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V ± 1%)

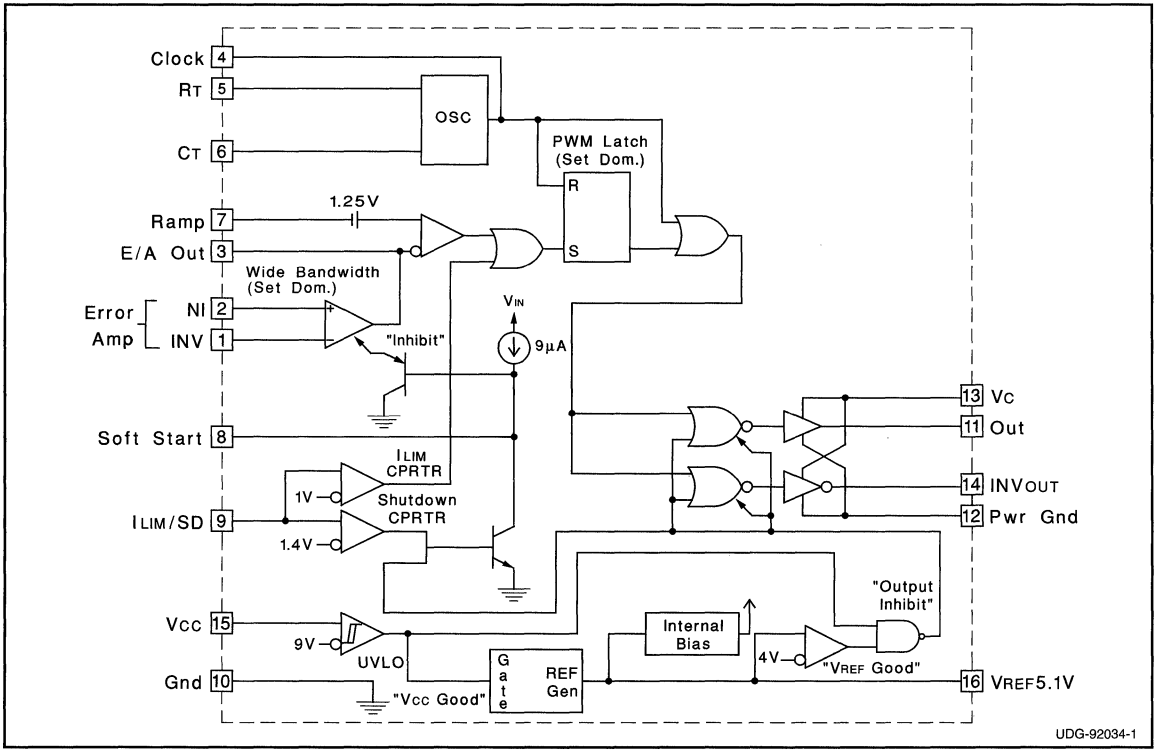
DESCRIPTION

The UC1824 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM

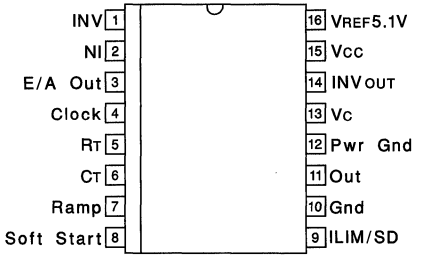


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 7) ..... -0.3V to 7V
(Pin 8, 9) ..... -0.3V to 6V
Clock Output Current (Pin 4) ..... -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) ..... -5mA
Power Dissipation 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

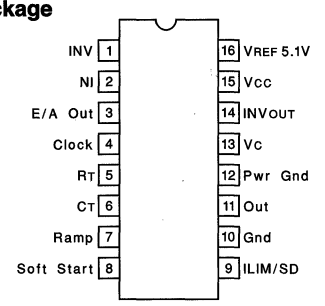
Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package

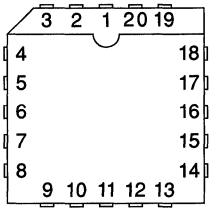


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
VC	17
INVOUT	18
VCC	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated,these specifications apply for , RT = 3.65k, CT = 1nF, VCC = 15V, -55°C<TA<125°C for the UC1824, –40°C<TA<85°C for the UC2824, and 0°C<TA<70°C for the UC3824, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, IO = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < VCC < 30V		2	20		2	20	mV
Load Regulation	1mA < IO < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	TJ = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 25⊃C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < VCC < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1824, –40°C<T_A<85°C for the UC2824, and 0°C<T_A<70°C for the UC3824, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1824 UC2824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Total Variation*	Line, Temperature	340		460	340		460	kHz
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA

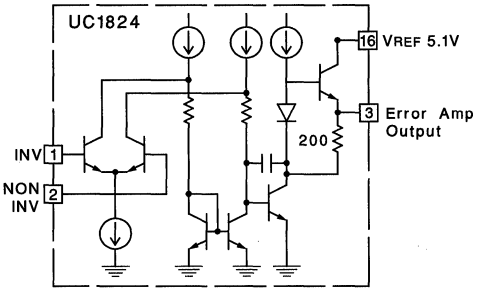
** This parameter not 100% tested in production but guaranteed by design.*

UC1824 Printed Circuit Board Layout Considerations

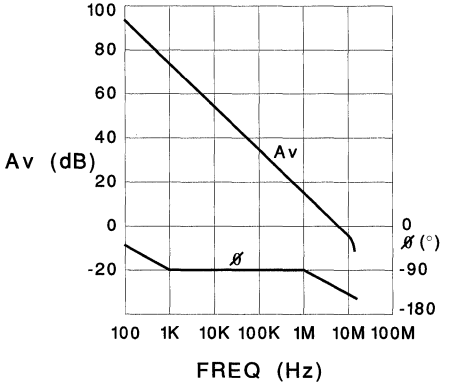
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1mF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

Error Amplifier Circuit

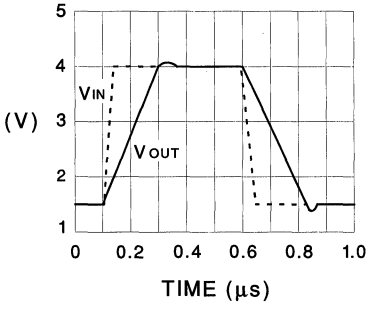
Simplified Schematic



Open Loop Frequency Response

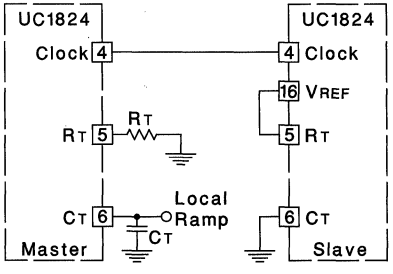


Unity Gain Slew Rate

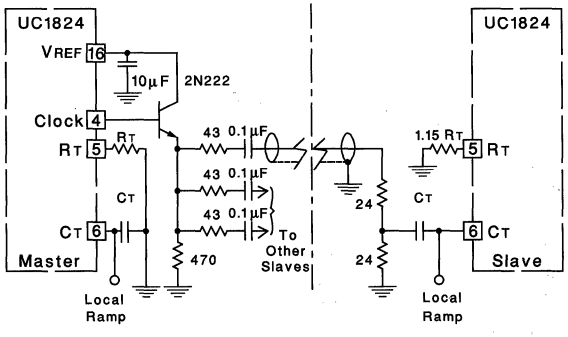


Synchronized Operation

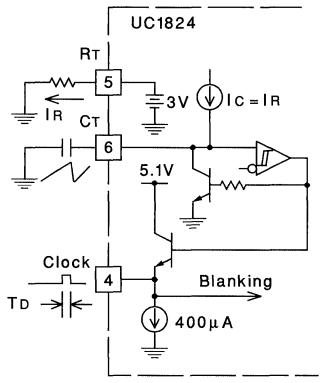
Two Units in Close Proximity



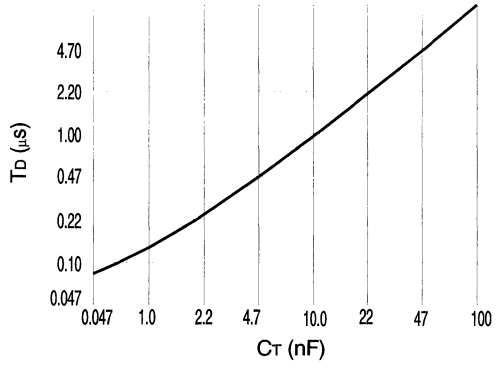
Generalized Synchronization



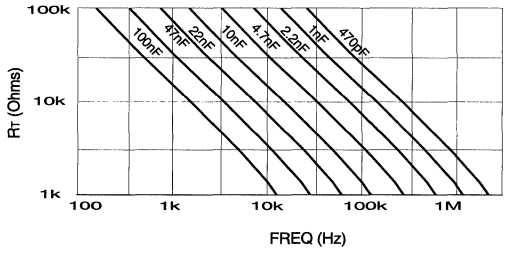
Oscillator Circuit



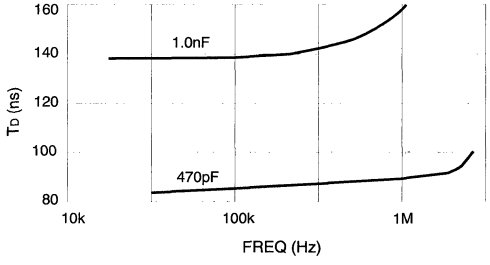
Primary Output Deadtime vs CT (3k ® RT ® 100k)



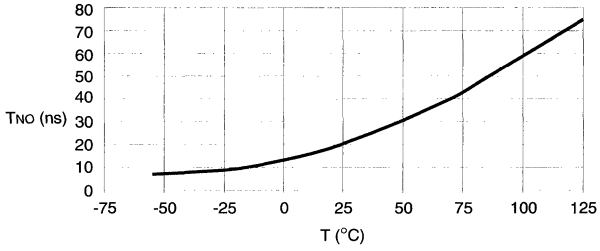
Timing Resistance vs Frequency



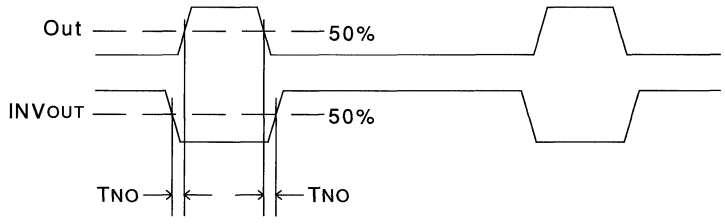
Primary Output Deadtime vs Frequency



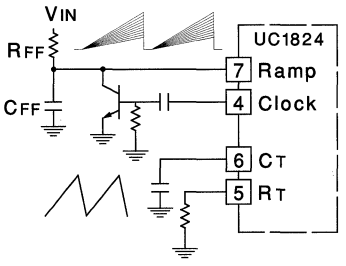
Typical Non-Overlap Time (TNO) Over Temperature



Non-Overlap Time (TNO)

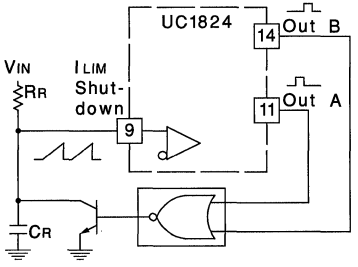


Forward Technique for Off-Line Voltage Mode Application



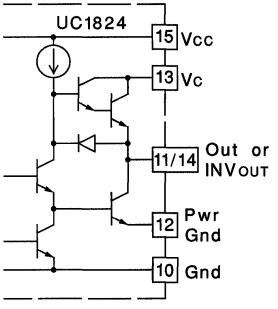
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

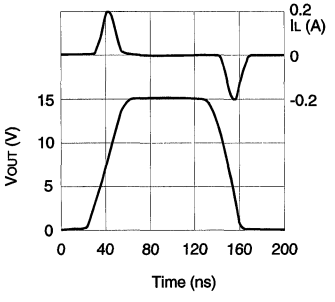


Output Section

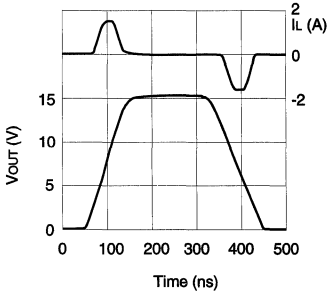
Simplified Schematic



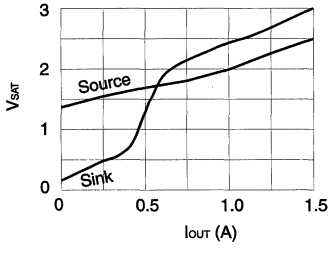
Rise/Fall Time (CL=1nF)



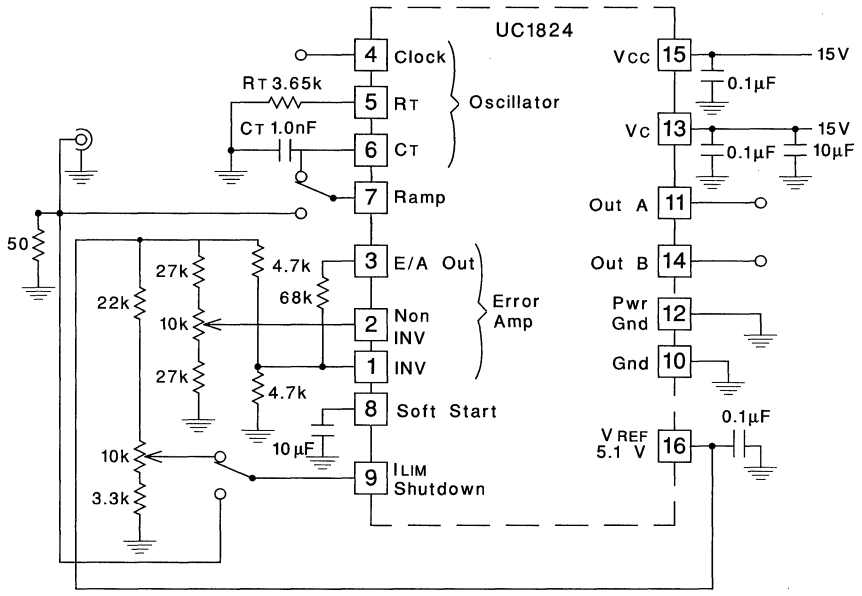
Rise/Fall Time (CL=10nF)



Saturation Curves



Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications. As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

UNITRODE CORPORATION
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UNITRODE

application INFO available

UC1825
UC2825
UC3825

High Speed PWM Controller

FEATURES

- Compatible with Voltage or Current Mode Topologies
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1mA)

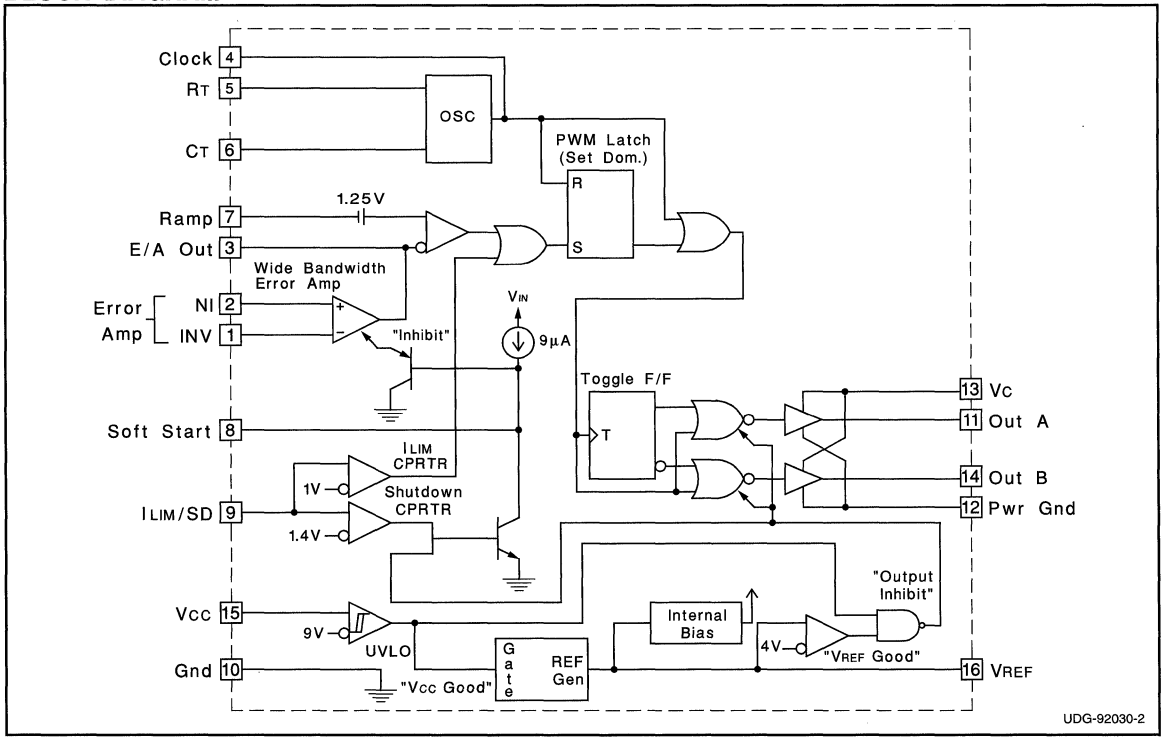
DESCRIPTION

The UC1825 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM



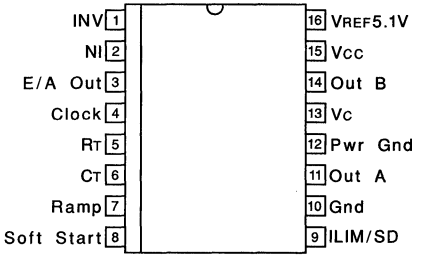
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15) 30V
Output Current, Source or Sink (Pins 11, 14)
DC 0.5A
Pulse (0.5µs) 2.0A
Analog Inputs
(Pins 1, 2, 7) . . . . . -0.3V to 7V
(Pin 8, 9) . . . . . -0.3V to 6V
Clock Output Current (Pin 4) . . . . . -5mA
Error Amplifier Output Current (Pin 3) 5mA
Soft Start Sink Current (Pin 8) 20mA
Oscillator Charging Current (Pin 5) . . . . . -5mA
Power Dissipation 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

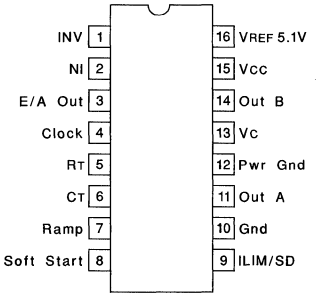
Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)

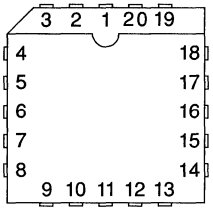


CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-20 & LCC-20 (Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out A	14
Pwr Gnd	15
N/C	16
VC	17
Out B	18
VCC	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for , RT = 3.65k, CT = 1nF, VCC = 15V, -55 C<TA<125 C for the UC1825, –40 C<TA<85 C for the UC2825, and 0 C<TA<70 C for the UC3825, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25 C, Io = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < VCC < 30V		2	20		2	20	mV
Load Regulation	1mA < Io < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/ C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		µV
Long Term Stability*	TJ = 125 C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 2 C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < VCC < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated,these specifications apply for , R_T = 3.65k, C_T = 1nF, V_{CC} = 15V, -55°C<T_A<125°C for the UC1825, –40°C<T_A<85°C for the UC2825, and 0°C<T_A<70°C for the UC3825, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1825 UC2825			UC3825			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Clock Out High		3.9	4.5		3.9	4.5		V
Clock Out Low			2.3	2.9		2.3	2.9	V
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V
Error Amplifier Section								
Input Offset Voltage				10			15	mV
Input Bias Current			0.6	3		0.6	3	µA
Input Offset Current			0.1	1		0.1	1	µA
Open Loop Gain	1V < V_O < 4V	60	95		60	95		dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		75	95		dB
PSRR	10V < V_{CC} < 30V	85	110		85	110		dB
Output Sink Current	$V_{PIN\ 3}$ = 1V	1	2.5		1	2.5		mA
Output Source Current	$V_{PIN\ 3}$ = 4V	-0.5	-1.3		-0.5	-1.3		mA
Output High Voltage	$I_{PIN\ 3}$ = -0.5mA	4.0	4.7	5.0	4.0	4.7	5.0	V
Output Low Voltage	$I_{PIN\ 3}$ = 1mA	0	0 .5	1.0	0	0.5	1.0	V
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz
Slew Rate*		6	12		6	12		V/µs
PWM Comparator Section								
Pin 7 Bias Current	$V_{PIN\ 7}$ = 0V		-1	-5		-1	-5	µA
Duty Cycle Range		0		80	0		85	%
Pin 3 Zero DC Threshold	$V_{PIN\ 7}$ = 0V	1.1	1.25		1.1	1.25		V
Delay to Output*			50	80		50	80	ns
Soft-Start Section								
Charge Current	$V_{PIN\ 8}$ = 0.5V	3	9	20	3	9	20	µA
Discharge Current	$V_{PIN\ 8}$ = 1V	1			1			mA
Current Limit / Shutdown Section								
Pin 9 Bias Current	0 < $V_{PIN\ 9}$ < 4V			15			10	µA
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V
Delay to Output			50	80		50	80	ns
Output Section								
Output Low Level	I_{OUT} = 20mA		0.25	0.40		0.25	0.40	V
	I_{OUT} = 200mA		1.2	2.2		1.2	2.2	V
Output High Level	I_{OUT} = -20mA	13.0	13.5		13.0	13.5		V
	I_{OUT} = -200mA	12.0	13.0		12.0	13.0		V
Collector Leakage	V_C = 30V		100	500		10	500	µA
Rise/Fall Time*	CL = 1nF		30	60		30	60	ns
Under-Voltage Lockout Section								
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V
Supply Current Section								
Start Up Current	V_{CC} = 8V		1.1	2.5		1.1	2.5	mA
ICC	$V_{PIN\ 1}$, $V_{PIN\ 7}$, $V_{PIN\ 9}$ = 0V; $V_{PIN\ 2}$ = 1V		22	33		22	33	mA

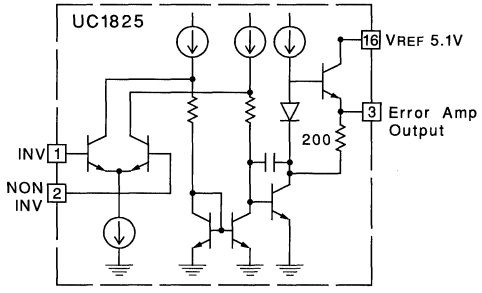
** This parameter not 100% tested in production but guaranteed by design.*

Printed Circuit Board Layout Considerations

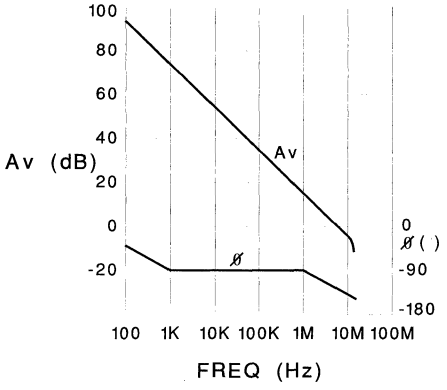
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1825 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3) Bypass VCC, VC, and VREF. Use 0.1µF monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

Error Amplifier Circuit

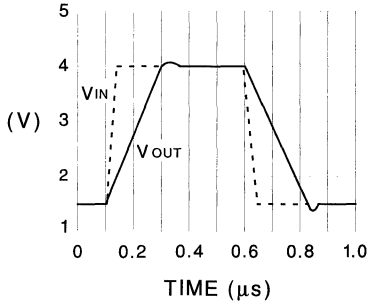
Simplified Schematic



Open Loop Frequency Response

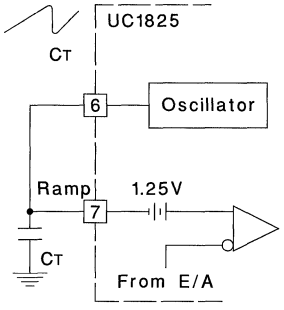


Unity Gain Slew Rate

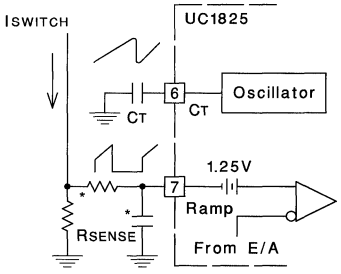


PWM Applications

Conventional (Voltage Mode)

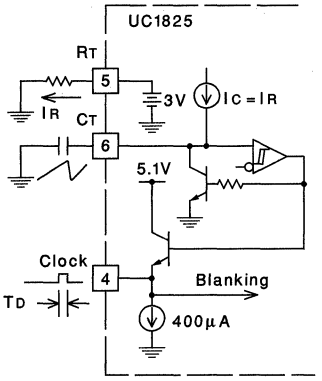


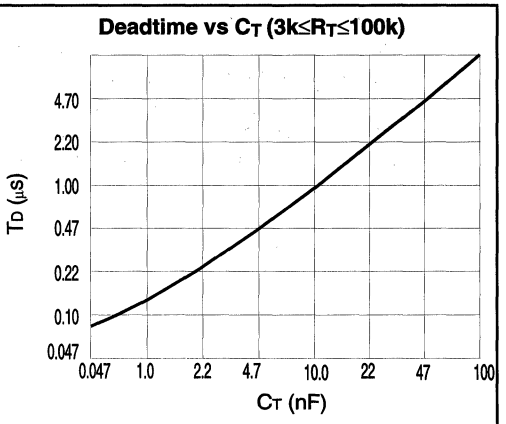
Current-Mode

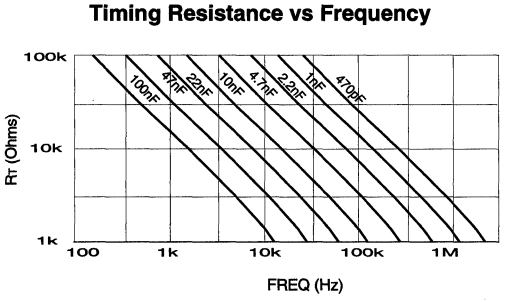


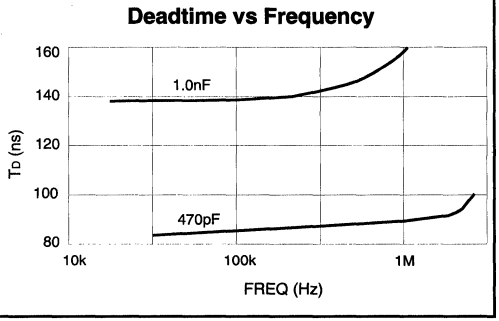
* A small filter may be required to suppress switch noise.

Oscillator Circuit



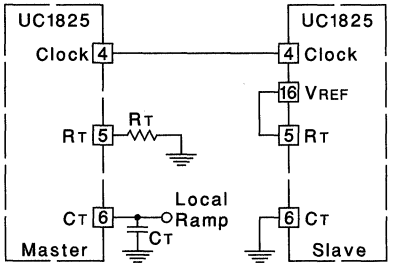




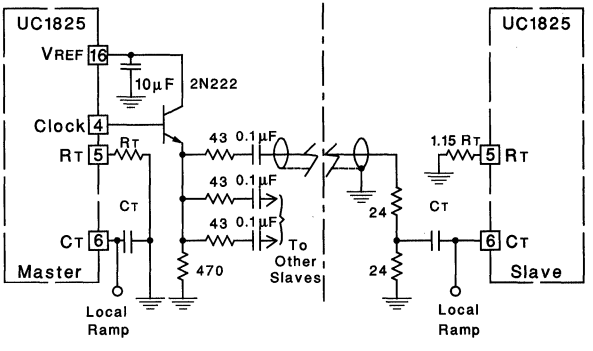


Synchronized Operation

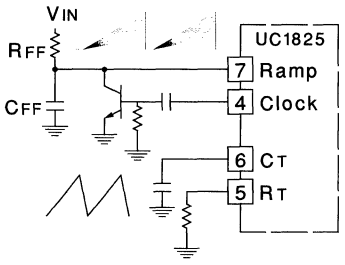
Two Units in Close Proximity



Generalized Synchronization

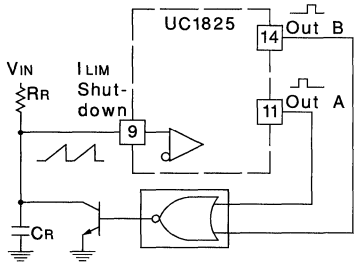


Forward Technique for Off-Line Voltage Mode Application



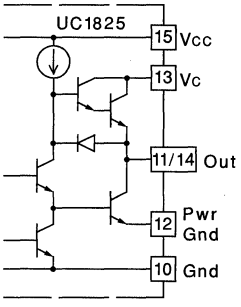
Constant Volt-Second Clamp Circuit

The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, RT and CR are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.

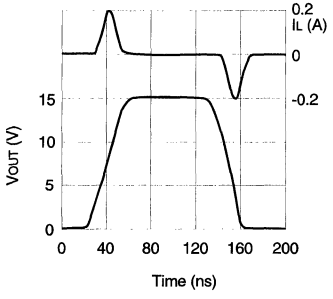


Output Section

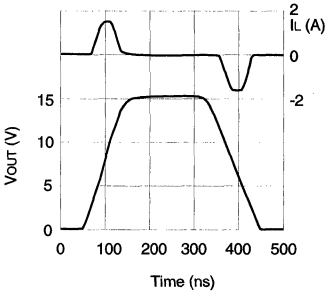
Simplified Schematic



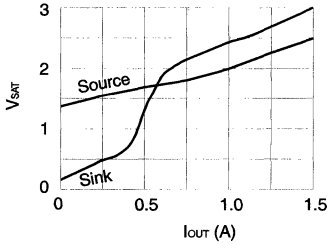
Rise/Fall Time (CL=1nF)



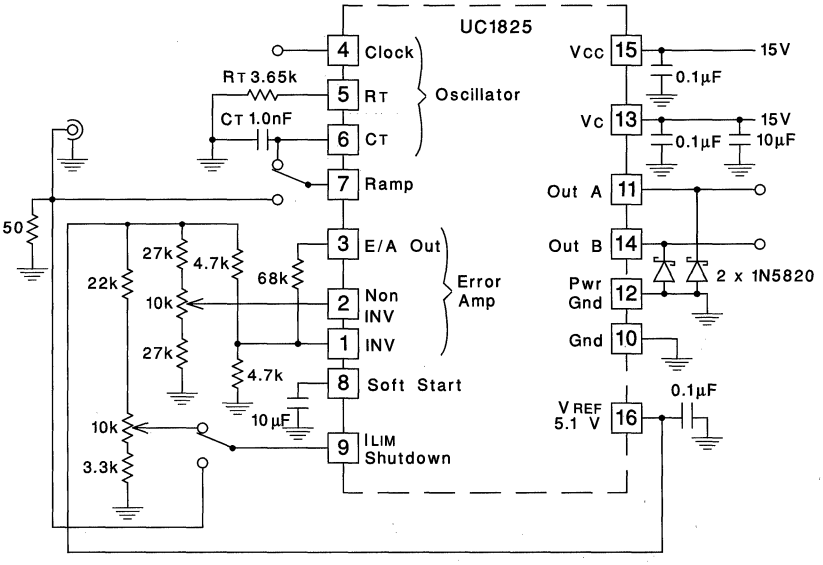
Rise/Fall Time (CL=10nF)



Saturation Curves



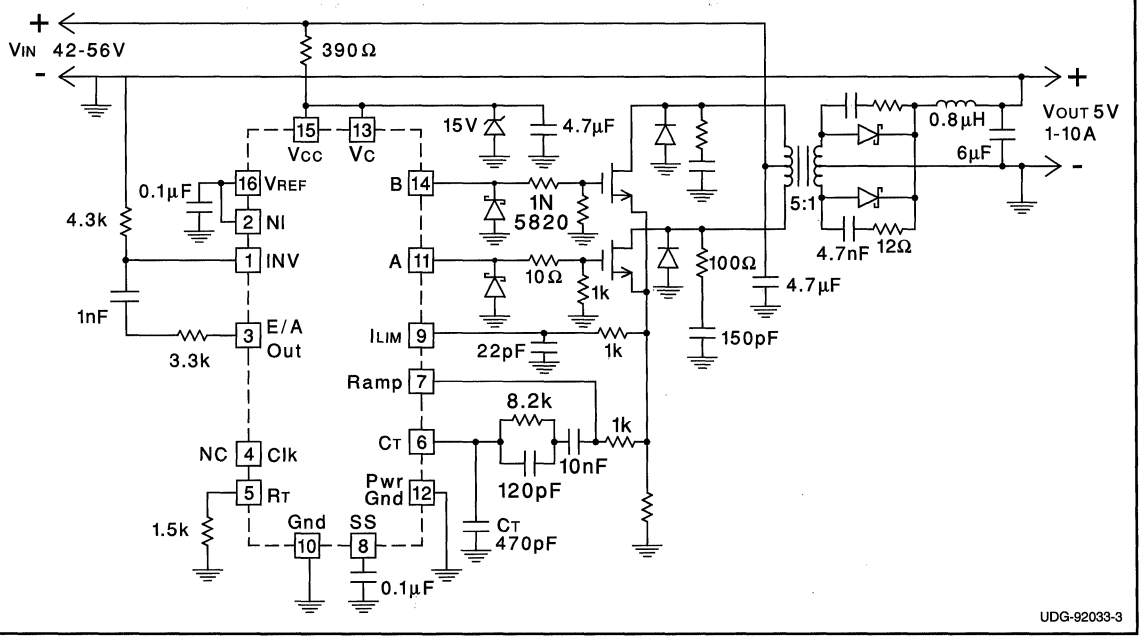
Open Loop Laboratory Test Fixture



This test fixture is useful for exercising many of the UC1825's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

Design Example: 50W, 48V to 5V DC to DC Converter - 1.5MHz Clock Frequency



UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

Secondary Side Average Current Mode Controller

FEATURES

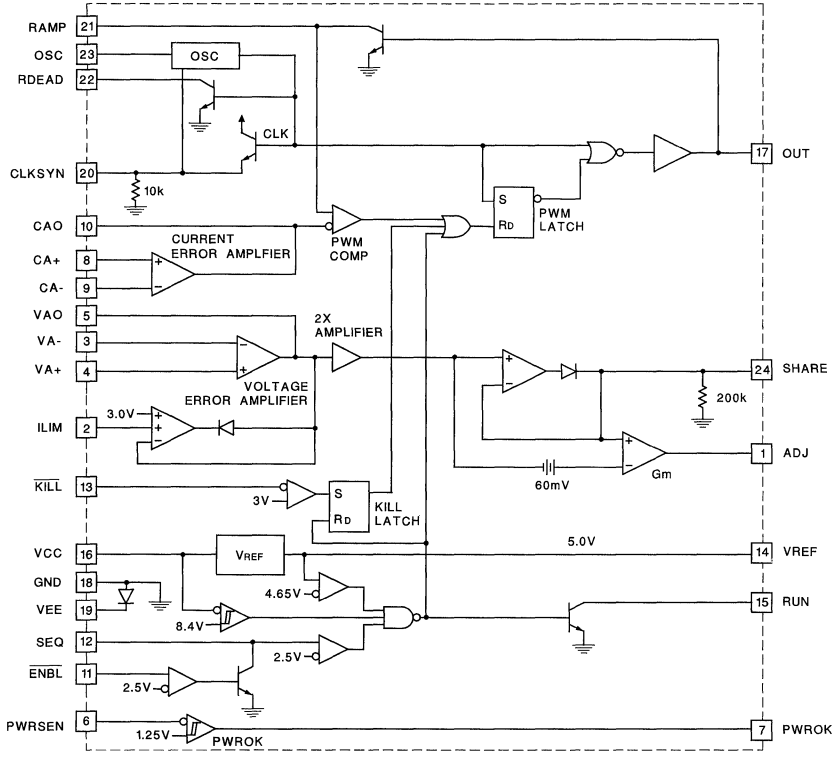
- Practical Secondary Side Control of Isolated Power Supplies
- 1MHz Operation
- Tailored Loop Bandwidth Provides Excellent Noise Immunity
- Voltage Feedforward Provides Superior Transient Response
- Accurate Programmable Maximum Duty Cycle
- Multiple Chips Can be Synchronized to Fastest Oscillator
- Wide Gain Bandwidth Product (70MHz, Acl>10) Current Error Amplifier
- Up to Ten Devices Can Easily Share a Common Load

DESCRIPTION

The UC1826 family of average current mode controllers accurately accomplishes secondary side average current mode control. The secondary side output voltage is regulated by sensing the output voltage and differentially sensing the AC switching current. The sensed output voltage drives a voltage error amplifier. The AC switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current error amplifier. The output of the voltage error amplifier can be used to drive the current amplifier which filters the measured inductor current. Fast transient response is accomplished by utilizing voltage feedforward in generating the PWM ramp.

The UC1826 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC1826 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. With its tailored bandwidth, the UC1826 provides excellent noise immunity and is an ideal controller to achieve high power, secondary side average current mode control.

BLOCK DIAGRAM



Pin Numbers refer to 24-pin packages.

UDG-95013

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 20V
Output Current Source or Sink 0.3A
Analog Input Voltages . . . . . –0.3V to 7V
ILIM, KILL, SEQ, ENBL, RUN, PWRSEN, PWROK –0.3V to 7V
CLKSYN Current Source 20mA
RUN Current Sink 20mA
SEQ Current Sink 20mA
RDEAD Current Sink 20mA
RAMP Current Sink 20mA
Share Bus Voltage (voltage with respect to GND) . . 0V to 6.2V
ADJ Voltage (voltage with respect to GND) . . . . . 0.9V to 6.3V
VEE (voltage with respect to GND) . . . . . –1.5V

Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

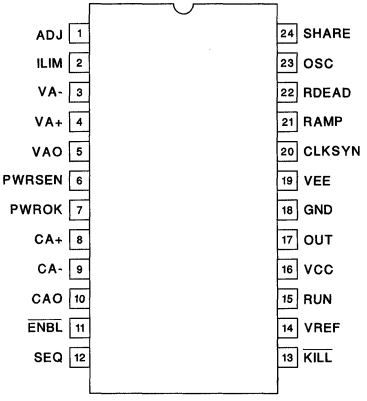
All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

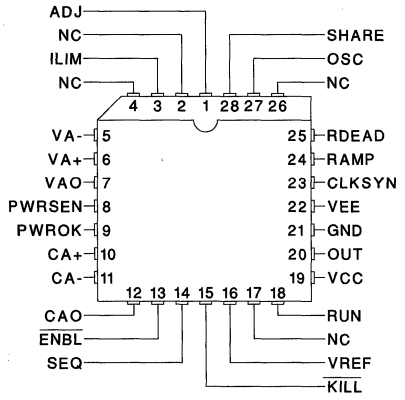
Input Voltage . . . . . 8V to 20V
Sink/Source Output Current 250mA
Timing Resistor R_T . . . . . 1k to 200k
Timing Capacitor C_T . . . . . 75pF to 2nF

CONNECTION DIAGRAMS

DIL-24, SOIC-24, TSSOP-24 (Top View)
J or N, DW, PW Packages



PLCC-28 (Top View)
Q Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier					
Ib			0.5	3	µA
Vio	T_A = +25°C		0.75	3	mV
	Over Temperature			5	mV
Avo		60	90		dB
GBW (Note 2)	Acl = 10, R_{IN} = 1k, CC = 15pF, f = 200kHz (Note 1)	45	70		MHz
Vol	I_O = 1mA, Voltage above VEE		0.5		V
Voh	I_O = 0mA		3.8		V
	I_O = –1mA		3.5		V
Voltage Error Amplifier					
Ib			0.5	3	µA
Vio				5	mV
Avo		60	90		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Error Amplifier (cont.)					
GBW (Note 2)	f = 200kHz		7		MHz
Vol	I_O = 175mA, Volts above VEE			0.6	V
Voh	ILIM = 3V	2.85	3	3.15	V
Voh-ILIM	Tested ILIM = 0.5V, 1.0V, 2.0V	–100		100	mV
2X Amplifier and Share Amplifier					
V offset (b; y = mx + b)				20	mV
GAIN (m; y = mx + b)	Slope with AV_{OUT} = 1V and 2V	1.98		2.02	V
GBW (Note 2)			100		kHZ
R_{SHARE}	VCC = 0, $V_{SHARE/ISHARE}$		200		kΩ
Total Offset	Negative supply is VEE, GND Open,VAO = GND	–75	0	75	mV
Vol	VAO = Voltage Amp Vol, Volts above VEE	0.2	0.45	0.6	V
Voh	I_O = 0mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
	I_O = –1mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
Adjust Amplifier					
Vio		40	60	80	mV
gm	I_O = –2μA to 2μA, C_{ADJ} = 0.1μF		–0.1	–0.3	mS
Vol	I_{OUT} = 0	0.9	1	1.1	v
	I_{OUT} = 2μA	0.85	1	1.15	V
Voh	I_{OUT} = 0, V_{SHARE} = 6.5V	5.7	6	6.3	V
	I_{OUT} = –2μA, V_{SHARE} = 6.5V	5.7	6	6.3	V
Oscillator					
Frequency		450	500	550	kHz
Max Duty Cycle		72	76	80	%
OSC Ramp Amplitude		2	2.2	2.4	V
Ramp Saturation	I_O = 10mA, OSC = 0V		0.44	0.8	V
Clock Driver/SYNC (CLKSYN)					
Vol			0.02	0.2	V
Voh			3.6		V
	R_{CLKSYN} = 200Ω		3.5		V
I_{SOURCE}			25		mA
R_{CLKSYN}	VCC = 0, V_{CLKSYN}/I_{CLKSYN}		10		k
V_{TH}			1.5		V
VREF Comparator					
Turn-on Threshold			4.65		V
Hysteresis			0.4		V
VCC Comparator					
Turn-on Threshold		7.9	8.4	8.9	V
Hysteresis			0.4		V
PWR Sense Comparator					
Voltage Threshold			1.25		V
Vol	I_O = 1mA		0.3	0.4	V
Voh	I_O = –100μA		4		V
$\overline{\text{KILL}}$ Comparator					
Voltage Threshold			3		V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1826; –40°C to +85°C for UC2826; and 0°C to +70°C for UC3826; VCC = 12V, VEE = GND, Output no load, C_T = 345pF, R_T = 4kΩ, RDEAD = 1000Ω, C_{RAMP} = 345pF, R_{RAMP} = 35.2kΩ, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sequence Comparator					
Voltage Threshold			2.5		V
SEQ SAT	I_O = 10mA		0.25		V
Enable Comparator					
Voltage Threshold			2.5		V
RUN SAT	I_O = 10mA		0.2		V
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	VCC = 15V	4.9		5.1	V
Line Regulation	10 < VCC < 20		3	15	mV
Load Regulation	0 < I_O < 10mA		3	15	mV
Short Circuit I	VREF = 0V	30	60	90	mA
Output Stage					
Rise Time	C_L = 100pF		10	20	ns
Fall Time	C_L = 100pF		10	20	ns
Voh	VCC > 11V, I_O =–10mA	8.0	8.	8.8	V
	I_O = –200mA	7.8			V
Vol	I_O = 200mA			3.0	V
	I_O = 10mA			0.5	V
Virtual Ground					
V_{GND}-VEE	VEE is externally supplied, GND is floating and used as Signal GND.	0.2	0.75		V
Icc					
Icc (run)			21	30	mA

Note 1: Guaranteed by design. not 100% tested in production.
Note 2: Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

PIN DESCRIPTIONS

ADJ: The output of the transconductance (gm = –0.1mS) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6V) its control voltage (VA+) until its load current is equal to the master. The 60mV input offset on the gm amplifier guarantees that the unit sensing the highest load current is chosen as the master. The 60mV offset is guaranteed by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30mV. The total current sense gain is the current amplifier gain. This pin needs a 0.1μF capacitor to compensate the amplifier.

CA–, CA+: The inverting and non-inverting inputs to the current error amplifier. This amplifier needs a capacitor between CA– and CAO to set its dominant pole.

CAO: The output of the current error amplifier which is internally clamped to 4V. It is internally connected to the inverting input of the PWM comparator.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The CLKSYN voltage is 3.6V when the oscillator capacitor C_T is being discharged, otherwise it is 0V.

PIN DESCRIPTIONS (cont.)

ENBL: The active low input with a 2.5V threshold enables the output to switch. SEQ and RUN are driven low when ENBL is above its 2.5V threshold.

GND: The signal ground used for the voltage sense amplifier, current error amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

KILL: The active low input with a 3.0V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving KILL above 3.0V and either resetting the power to the chip (VCC) or resetting the ENBL signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0V. A voltage less than 3.0V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp (not to be confused with PWM ramp) pin has a capacitor C_T to ground and two resistors in series R_T and R_{DEAD} to VREF. The total resistance of R_T and R_{DEAD} divided by VREF – V_{OSC} sets exponential charge current. The oscillator charges from 1.2V to 3.4V until the output transitions low. At this time an open collector transistor is turned on and discharges the C_T capacitor through RDEAD.

The charge time is approximately $T_{CHARGE} = 2(R_T + R_{DEAD}) \bullet C_T$ when the R_{DEAD} resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \bullet R_{DEAD} \bullet C_T$.

$$(1)\ Frequency \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}}$$

$$(2)\ Maximum Duty Cycle \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}}$$

The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5V. The peak current sink and source are 250mA. All UVLO, SEQ, ENBL, and KILL logic either enable or disable the output driver.

PWRSEN: This pin is the input to the PWROK comparator.

PWROK: The output pin from the PWROK comparator. It has a 300μA current source output when driven high.

RAMP: An open collector that can sink 20mA to discharge the oscillator capacitor. An RC is tied between VCC and GND to accomplish feedforward. The PWM output drives this pin. When the output is high, the transistor is off enabling the charging of the RAMP capacitor. When the output transitions low, the transistor is turned on discharging the RAMP capacitor. The voltage at RAMP rises from 0.2V to near 4V at maximum duty cycle. Although this is an exponential ramp at high VCC voltage the ramp appears linear.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is $2 \bullet R_{DEAD} \bullet C_T$. The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4V, VREF is greater than 4.65V, SEQ is greater than 2.5V, and KILL lower than 3.0V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND create a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly DC voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA–, VA+: The inverting and non-inverting inputs to the voltage error amplifier.

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

VCC: The input voltage to the chip. The chip is operational between 8.4V and 20V.

VEE: The negative supply voltage to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0V.

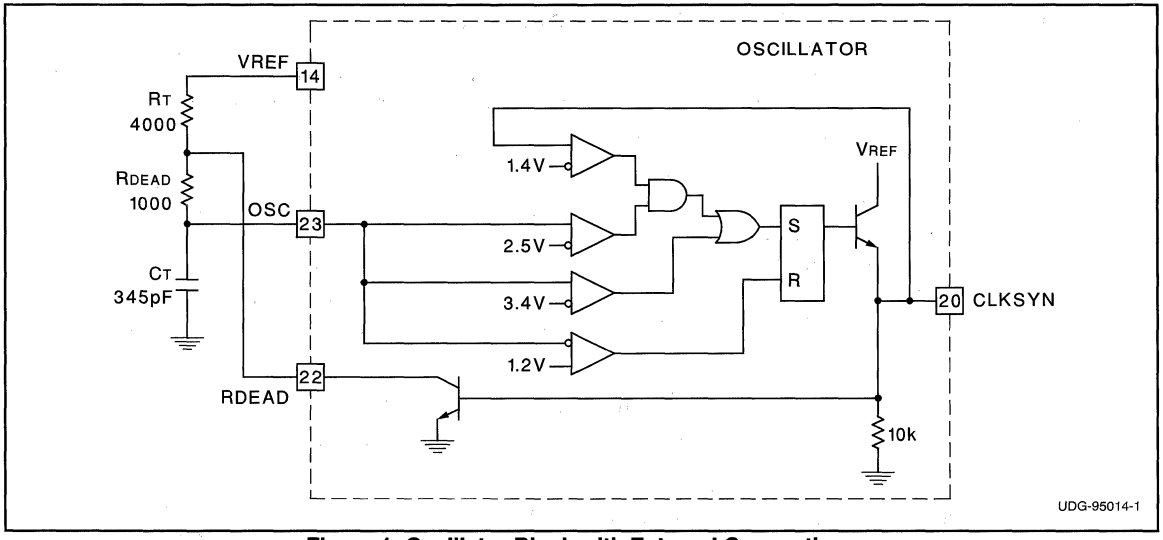


Figure 1. Oscillator Block with External Connections

CIRCUIT DESCRIPTION:

PWM Oscillator: The chip has two pins that set RC time constants. The resistor and capacitor tied to RAMP create the ramp used as the input to the PWM comparator. When the output pin OUT is high, RAMP charges until it passes the PWM comparator threshold. The output is then driven low and RAMP is discharged. The resistors and capacitor on the OSC pin are used to set the PWM operating frequency and its maximum duty cycle.

The oscillator block diagram with external wiring is shown in Figure 1. OSC has a capacitor (C_T) to ground and two resistors in series (R_T and R_{DEAD}) to VREF. The total resistance of R_T and R_{DEAD} divided by VREF - V_{OSC} sets the exponential charge current. The oscillator charges from 1.2V to a 3.4V threshold with an RC time delay of 2 • C_T • (R_{DEAD} + R_T). After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. At this time an open collector transistor is turned on and discharges C_T capacitor through RDEAD with a RC time delay of 2 • C_T • R_{DEAD}. The oscillator and ramp waveforms are shown in Figure 2. Equations to attain frequency and maximum duty cycle are listed under the OSC pin description.

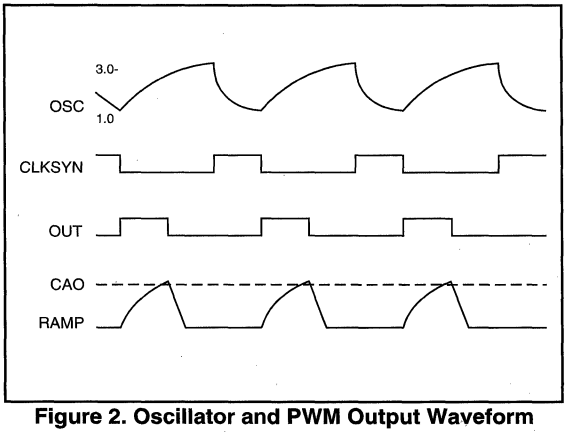


Figure 2. Oscillator and PWM Output Waveform

As shown in Figure 3, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure 1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to guarantee synchronization.

Grounds, Voltage Sensing and Current Sensing: The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 4, the

CIRCUIT BLOCK DESCRIPTION (cont.)

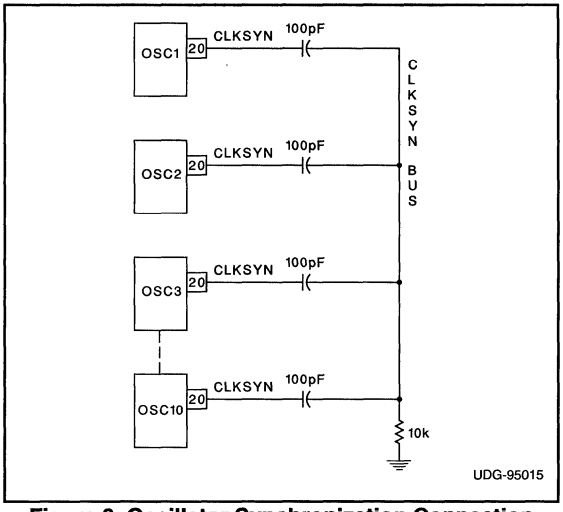


Figure 3. Oscillator Synchronization Connection Diagram

positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA–), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, R_S. The voltage across the shunt resistor is level shifted up so that the maximum voltage across R_S corresponds to the voltage error amplifier Voh.

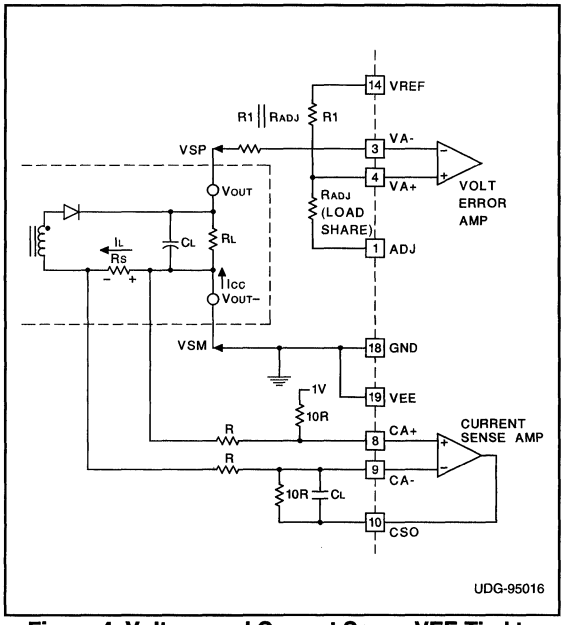


Figure 4. Voltage and Current Sense VEE Tied to GND

Figure 4 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7V below ground. The resistor R_{ADJ} is used for load sharing. The unit which is the master will force V_{ADJ} to 1.0V. Therefore, the regulated voltage being sensed is actually

$$VSP - VSM = (VREF - V_{ADJ}) \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}} \right) + V_{ADJ}$$

$$VSM = 0V, V_{ADJ} = 1V\,(master), VREF = 5V$$

$$VSP = 4 \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}} \right) + 1V$$

The voltage at ADJ on the slave chips will increase forcing their load currents to increase to match the master.

The AC frequency response of the voltage error amplifier is shown in Figure 5.

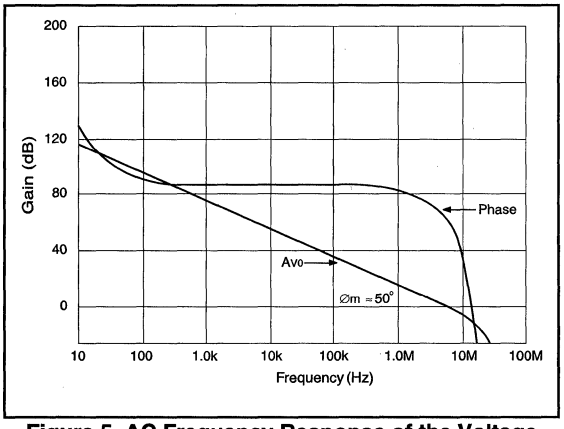


Figure 5. AC Frequency Response of the Voltage Error Amplifier

Startup and Shutdown: Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC1826 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it will command zero load current, guaranteeing a soft start. The undervoltage lockout (UVLO) is a logical AND of $\overline{ENBL}$ < 2.5V, SEQ > 2.5V, VCC > 8.4V and

CIRCUIT BLOCK DESCRIPTION (cont.)

VREF > 4.65V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the $\overline{ENBL}$ pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4V. The $\overline{KILL}$ input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after $\overline{KILL}$ has been initiated, the chip must be powered down and then back up. A pulse on the $\overline{ENBL}$ pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing: Load sharing is accomplished similarly to the UC1907 except it has the added constraint of using the sensed current for average current mode control. The sensed current for the UC1826 has an AC component that is amplified and then averaged. The voltage error amplifier represents this average current. The voltage error amplifier output is the current command signal and its voltage represents the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The IC with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60mV input offset guarantees that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) ICs to adjust their respective references high in order to balance each IC's load current. The master's ADJ pin will be at its 1.0V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0V.

VREF can be adjusted 150mV to 300mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} will typically be 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1V ±100mV by a factor of 10 to 30, contributing only a 3mV to 10mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop: The current error amplifier (CEA) needs its loop compensated externally. The zero crossing can be calculated with Equation 3.

$$(3)\quad Frequency(0dB) = \frac{1}{2\pi R_{INV} \bullet C_{COMP}}$$

R_{INV} is the input resistance at the inverting terminal CA– C_{COMP} is the capacitance between C_A– and CAO.

Although it is only unity gain stable for a BW of 7MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate with sufficient phase margin at a GBW of 70MHz. A closed loop gain of 10 attenuates the output by 20.8dB

$$20.8 = 20\log \bullet \frac{1}{11}$$

to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity at 7MHz, where the phase margin begins to roll off. See Figure 6 for a typical Bode plot.

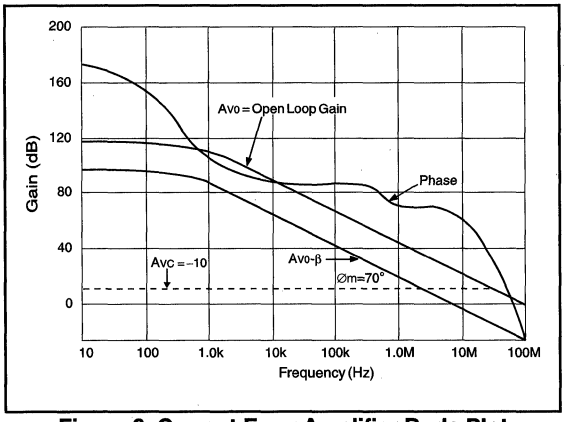


Figure 6. Current Error Amplifier Bode Plot

The current error amplifier bandwidth is rolled off and controlled by the voltage error amplifier output. The maximum load current is limited to approximately the maximum voltage across the shunt resistor (maximum of 200mV) divided by R_S:

$$(4)\quad I_{MAX(LOAD)} = \frac{V_{R(S)}}{R_S}$$

ILIM sets the maximum current limit by setting the Voh clamp on the voltage error amplifier. If ILIM is not set to limit the Voh to be equal to the maximum voltage across R_S, VAO must be attenuated to match the maximum voltage V_{RS} across the shunt resistor. By attenuating the

CIRCUIT BLOCK DESCRIPTION (cont.)

maximum voltage at VAO to be equal to V_{RS}, the current control loop keeps the load from exceeding its current limit. If the ILIM pin is connected to VREF, the Voh is set at 3.0V. The maximum current limit clamp can be reduced by reducing the voltage on ILIM to less than 3.0V as described in the ILIM pin description.

Design Example: Figure 7 is an open loop test that lets the user test the circuit blocks discussed without having to build an entire control loop. The pulse width can be varied by either the V_{ADJ} or the VI_{SENSE} inputs. Figure 8 shows an isolated power supply using the UC1826 secondary side average current mode controller.

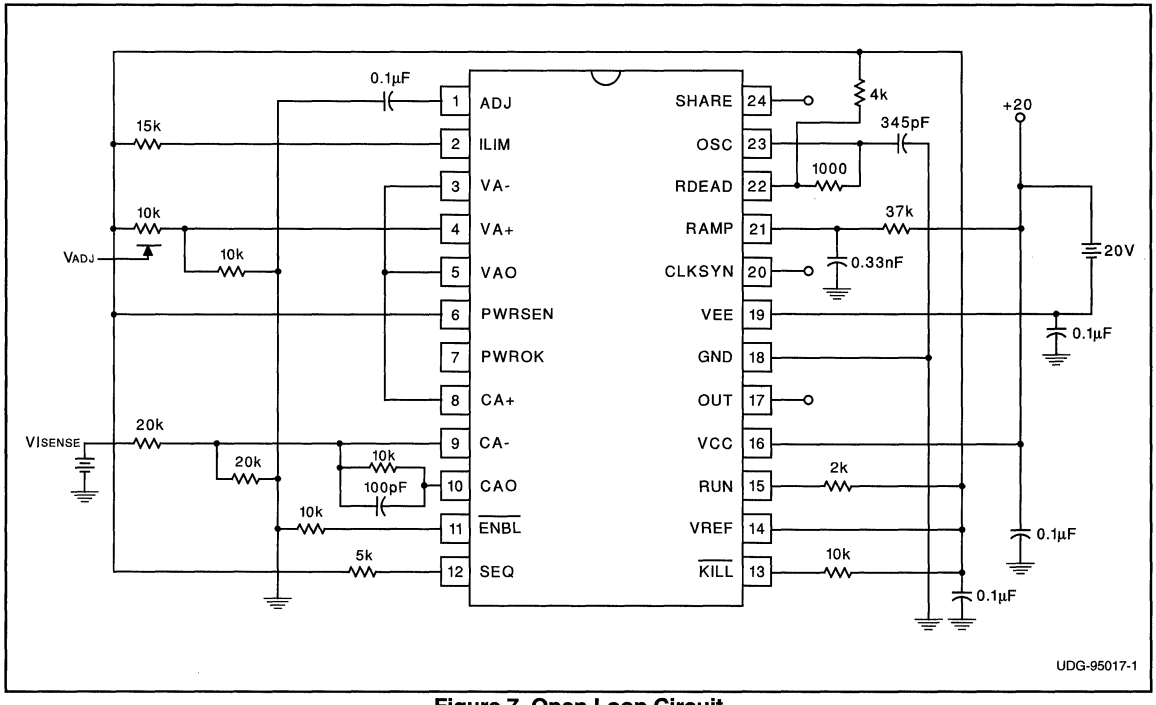


Figure 7. Open Loop Circuit

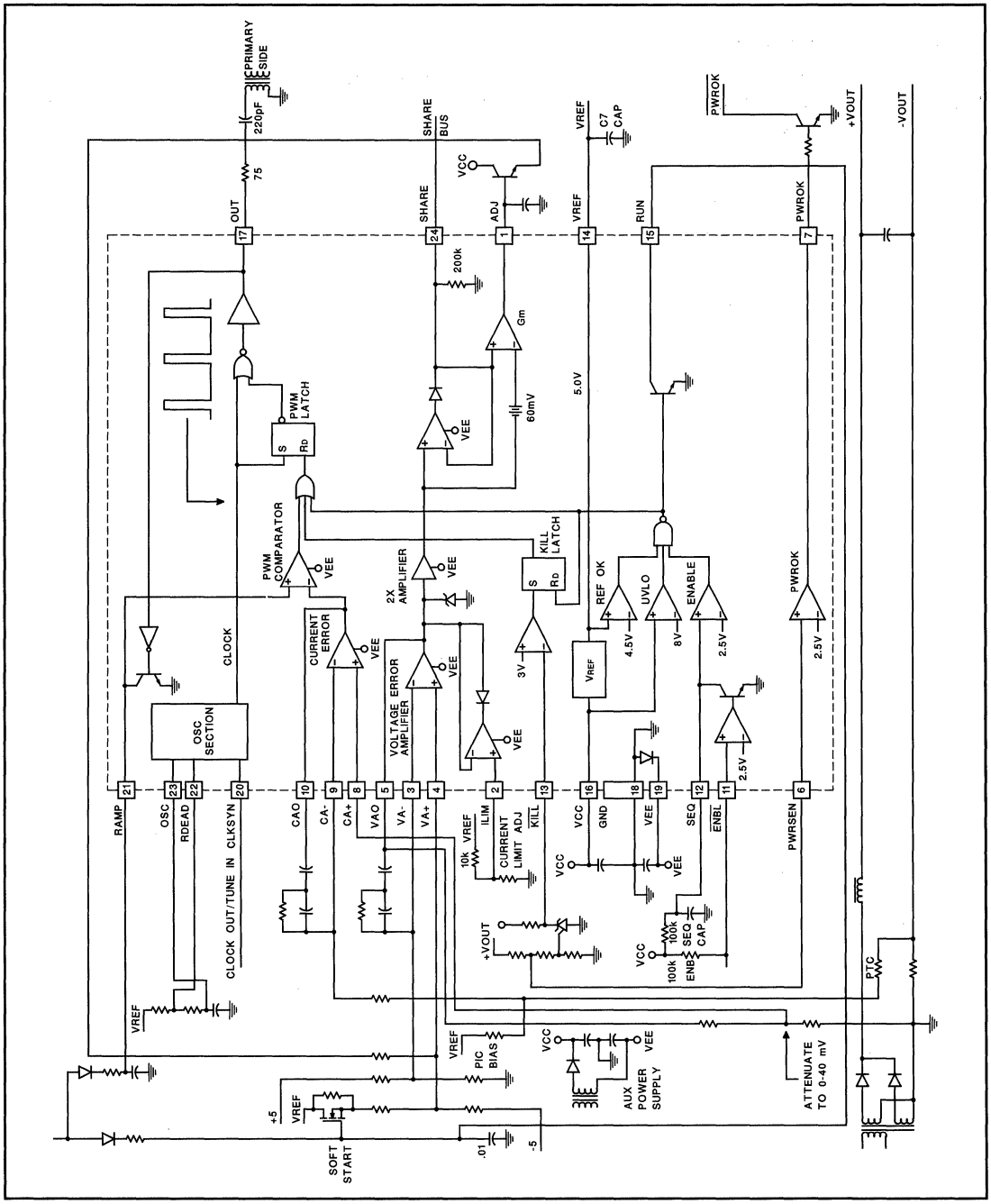


Figure 8. UC1826 Application Diagram

UNITRODE CORPORATION
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Buck Current/Voltage Fed Push-Pull PWM Controllers

FEATURES

- Ideal for Multiple Output and/or High Voltage Output Voltage Converters
- Up to 500kHz Operation
- High Voltage, High Current Floating Driver for Buck Converter Stage
- UC3827-1 Current Fed Controller has Push-Pull Drivers with Overlapping Conduction Periods
- UC3827-2 Voltage Fed Controller has Push-Pull Drivers with Non-overlapping Conduction Periods
- Average Current Mode, Peak Current Mode or Voltage Mode with Input Voltage Feedforward Control for Buck Power Stage
- Wide Bandwidth, Low Offset, Differential Current Sense Amplifier
- Precise Short Circuit Current Control

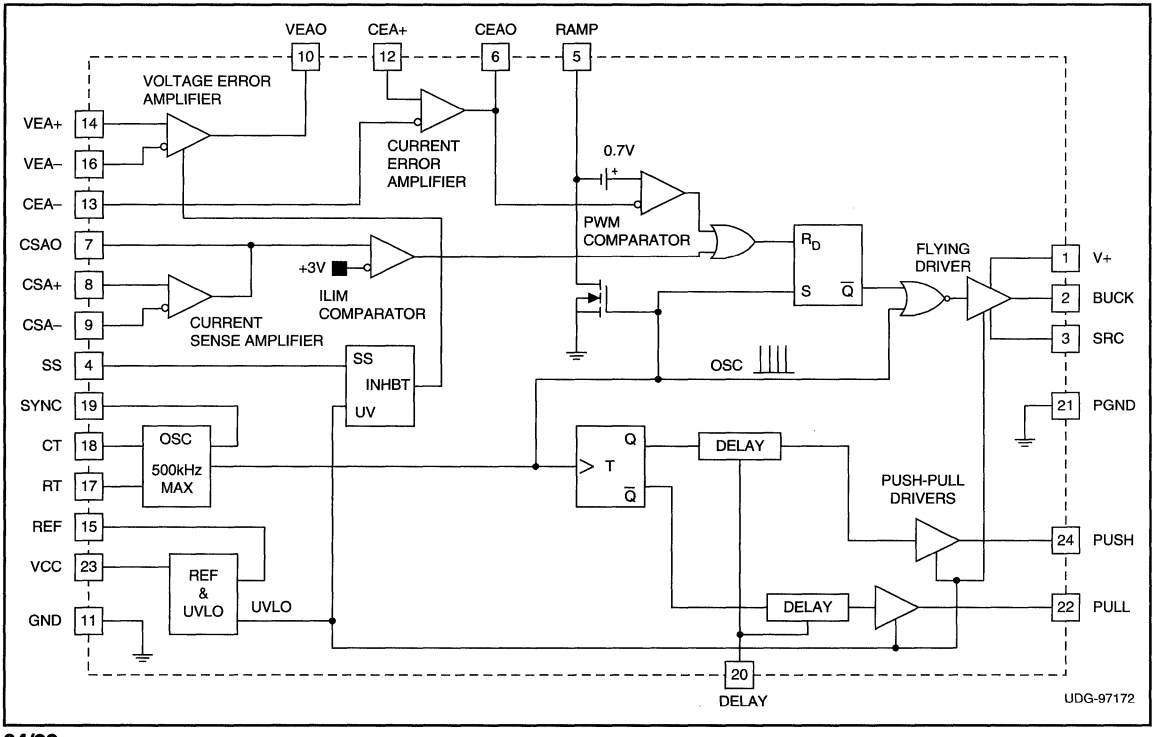
DESCRIPTION

The UC3827 family of controller ICs provides an integrated control solution for cascaded buck and push-pull converters. These converters are known as current fed or voltage fed push-pull converters and are ideally suited for multiple output and/or high voltage output applications. In both current fed and voltage fed modes, the push-pull switches are driven at 50% nominal duty cycles and at one half the switching frequency of the buck stage. In the current fed mode, the two switches are driven with a guaranteed overlap period to prevent ringing and voltage stress on the devices. In the voltage fed mode, the two switches are driven with a guaranteed gap time between the switches to prevent shorting the transformer across the energy storage capacitor and to prohibit excessive currents flowing through the devices.

The converter's output voltage is regulated by pulse width modulation of the buck switch. The UC3827 contains complete protection and PWM control functions for the buck converter. Easy control of the floating switch is accomplished by the floating drive circuitry. The gate drive waveform is level shifted to support an input voltage up to 72Vdc.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

The UC3827 can be set up in traditional voltage mode control using input voltage feedforward technique or in current mode control. Using current mode control prevents potential core saturation of the push-pull transformer due to mismatches in timing and in component tolerances. With average current mode control, precise control of the inductor current feeding the push-pull stage is possible without the noise sensitivity associated with peak current mode control. The UC3827 average current mode loop can also be connected in parallel with the voltage regulation loop to assist only in fault conditions.

Other valuable features of the UC3827 include bidirectional synchronization capability, user programmable overlap time (UC3827-1), user programmable gap time (UC3827-2), a high bandwidth differential current sense amplifier, and soft start circuitry.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VCC 20V
Input Voltage Range
  For all pins except V+, BUCK, SRC . . . . . –0.3V to 5V
  For V+ and BUCK 90V
  For SRC 90V–VCC
BUCK Driver
  IO Continuous . . . . . ± 250mA
  IO Peak . . . . . ± 1A
PUSH/PULL Driver
  IO Continuous . . . . . ± 200mA
  IO Peak . . . . . ± 0.8A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Voltages are referenced to ground. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

TEMPERATURE AND PACKAGE SELECTION GUIDE

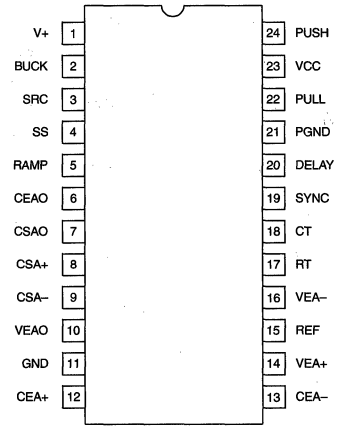
	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1827-X	–55°C to +125°C	J
UC2827-X	–40°C to +85°C	N, DW, Q
UC3827-X	0°C to +70°C	N, DW, Q

PART VERSION GUIDE

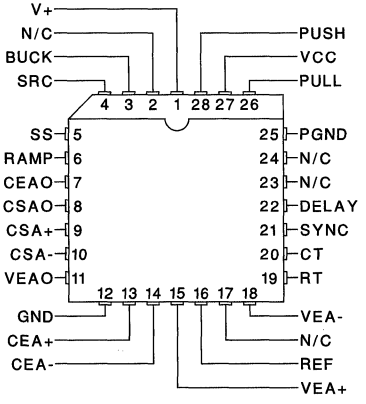
PART NUMBER	TOPOLOGY
UCX827-1	Current Fed Push-Pull
UCX827-2	Voltage Fed Push-Pull

CONNECTION DIAGRAMS

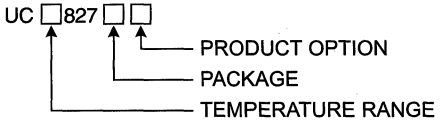
DIL-24 (Top View)
N or J, DW Packages



PLCC-28 (Top View)
Q Package



ORDERING INFORMATION



ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 15V, V+ = 14.3V, CT = 340pF, RT = 10K, R_{DELAY} = 24.3k, SRC = GND, BUCK, PUSH and PULL outputs no load. $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply					
VCC UVLO, Turn-On		8.3	8.8	9.5	V
Hysteresis		0.9	1.2	1.5	V
I_{VCC} Start	VCC = 8V			1000	µA
I_{VCC} Run			32	45	mA
V+ UVLO, Turn-On		7.1	7.5	8.3	V
V+ Hysteresis		0.2	0.4	0.9	V
I_{V+} Buck High		0.2	1	2	mA
Voltage Error Amplifier					
IB			0.5	3	µA
VIO				10	mV
AVOL		80	95		dB
GBW	(Note 7)	1	4		MHz
VOL	I_{VEAO} = 0µA (No Load)		0.3	0.5	V
VOH	I_{VEAO} = 0µA (No Load)	2.85	3	3.20	V
Current Sense Amplifier					
IB			–1	–5	uA
VIO				5	mV
AVOL		80	110		dB
GBW	(Note 7)	15	29		MHz
VOL	I_{CEAO} = 0µA (No Load)		0.25	0.5	V
VOH	I_{CEAO} = 0µA (No Load)	3	3.3		V
Common Mode Range	(Note 7)	0		2	V
Current Error Amplifier					
IB			–1	–5	µA
VIO				10	mV
AVOL		80	110		dB
GBW	At 100kHz, Measure Gain	2	4.5		MHz
VOL	I_{CEAO} = 0µA (No Load)		0.25	0.5	V
VOH	I_{CEAO} = 0µA (No Load)	3.3	3.5		V
Common Mode Range	(Note 7)	0		5	V
Oscillator Section					
Frequency		180	220	250	kHz
CT Discharge Current	3.5V at CT when CT removed	5			mA
PWM Comparator					
Minimum Duty Cycle	200kHz			0	%
Maximum Duty Cycle	200kHz	85	91	95	%
Buck Output Stage					
Rise Time	1nF Load, (Note 3)		40	100	ns
Fall Time	1nF, Load		30	80	ns
VOH	I_{BUCK} = –15mA , V+ –BUCK (Note 4)		1.5	2.5	V
	I_{BUCK} = –150mA, V+ – BUCK (Note 4)		2	2.5	V
VOL	I_{BUCK} = 15mA (Note 5)		0.2	0.4	V
	I_{BUCK} = 150mA (Note 5)		0.7	1.2	V

ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 15V, V+ = 14.3V, CT = 340pF, RT = 10K, RDELAY = 24.3k, SRC = GND, BUCK, PUSH and PULL outputs no load. TJ = TA.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Push/Pull Output Stages					
Rise Time	1nF Load		50	100	ns
Fall Time	1nF Load		35	100	ns
Overlap Time, -1 Only	1nF loads (Note 1)	100	250	400	ns
Non-Overlapping Time, -2 Only	(Note 2)	100	250	500	ns
VOH	IPUSH/PULL = –10mA, VCC – PUSH (Note 6)		2	3	V
	IPUSH/PULL = –100mA, VCC – PUSH (Note 6)		2.5	3	V
VOL	IPUSH/PULL = 10mA (Note 6)		0.2	0.8	V
	IPUSH/PULL = 100mA (Note 6)		0.6	1.2	V
Reference					
REF Voltage		4.8	5	5.2	V
Short Circuit Current	REF = 0V	–35	–50	–65	mA
Line Regulation	9.5V < VCC < 20V		5	20	mV
Load Regulation	0mA < IO < 10mA		8	20	mV
Soft Start					
VOL, Saturation	VCC = 7V		250	500	mV
Iss		–5	–12	–25	µA

Note 1: The overlap time is measured from the point at which the rising edge of PUSH/PULL crosses 5V until the falling edge of PULL/PUSH crosses 5V.

Note 2: The non-overlap time is measured from the point at which the falling edge of PUSH/PULL crosses 5V until the rising edge of PULL/PUSH crosses 5V.

Note 3: Measure the rise time from when BUCK crosses 1V until it crosses 9V.

Note 4: To force BUCK high, force CSAO=2.5V, CEAO = 2.5V, a 25k pulldown resistor form RAMP to ground, and CT = 0.5V.

Note 5: To force BUCK low, force CSAO = 2.5V, CEAO = 2.5V, a 10k pulldown resistor from RAMP to ground, and CT = 3.5V.

Note 6: To toggle PUSH or PULL into a desired state, pulse CT from 0.5V to 3.5V. PUSH and PULL toggle on the rising edge of CT.

Note 7: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

BUCK: Output of the buck PWM controller. The BUCK output is a floating driver, optimized for controlling the gate of an N-channel MOSFET. The peak sink and source currents are 1A. Any undervoltage faults will disable BUCK to an off condition (low).

CEA+: The non-inverting input of the current error amplifier.

CEA–: The inverting input of the current error amplifier.

CEAO: The output of the current error amplifier and the inverting input of the PWM comparator of the buck converter.

CSA+: The noninverting input of the current sense amplifier.

CSA–: The inverting input of the current sense amplifier.

CSAO: The output of the current sense amplifier and the noninverting input of the current limit comparator. When the signal level on this pin exceeds the 3V threshold of the current limit comparator, the buck gate drive pulse is terminated. This feature is useful to implement cycle-by-cycle current limiting for the buck converter.

CT: This pin is provided for the timing capacitor which is connected between CT and GND. The oscillator frequency is set by CT and a resistor RT, connected between pin RT and GND. The CT discharge current is approximately 40X the bias current through the resistor connected to RT. A practical maximum value for the discharge current is 20mA. The frequency of the oscillator is given by:

$$fOSC = \frac{0.77}{RT \bullet CT}$$

PIN DESCRIPTIONS (cont.)

DELAY: A resistor to GND programs the overlap time of the PUSH and PULL outputs of the UC3827-1 and the dead time of the PUSH and PULL outputs of the UC3827-2. The minimum value of the resistor, RDELAY, is 18kΩ. The delay or overlap time is given by:

$$TDELAY = \frac{RDELAY}{200\Omega} \bullet 10^{-9} \text{ sec.}$$

GND: This pin is the ground reference for all sensitive setup components not related to driving the outputs. They include all timing, voltage sense, current sense, and bypass components.

PGND: Ground connection for the PUSH and PULL outputs. PGND must be connected to GND at a single point on the printed circuit board. This is imperative to prevent large, high frequency switching currents flowing through the ground metalization inside the IC.

PULL: Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults will disable PULL to an off condition (low).

PUSH: Ground referenced output to drive an N-channel MOSFET. The PULL and the PUSH outputs are driving the two switches of the push-pull converter with complementary signals at close to a 50% duty cycle. Any undervoltage faults will disable PUSH to an off condition (low).

RAMP: The RAMP voltage, after a 700mV internal level shift, is fed to the noninverting input of the buck PWM comparator. A resistor to Vin and a capacitor to GND provide an input voltage feedforward signal for the buck controller in voltage mode control. In peak current mode control, the RAMP pin receives the current signal of the buck converter. In an average current mode setup, the RAMP pin has a linearly increasing ramp signal. This waveform may be generated either by connecting RAMP directly to CT, or by connecting both a resistor from VCC to RAMP and a capacitor from RAMP to GND.

REF: The output of the +5V on board reference. Bypass this pin with a capacitor to GND. The reference is off when the chip is in undervoltage lockout mode.

RT: A resistor to GND programs the charge current of the timing capacitor connected to CT. The charge current approximately equals:

$$\frac{REF}{2 \bullet RT}$$

The charge current should be less than 500μA to keep CT's discharge peak current less than 20mA, which is CT's maximum practical discharge value. The discharge time, which sets the maximum duty cycle, is set internally and is influenced by the charge current.

SRC: The source connection for the floating buck switch. The voltage on the SRC pin can exceed VCC but must be lower than 90V-VCC. Also, during turn-off transients of the buck switch, the voltage at SRC can go to –2V.

SS: The soft start pin requires a capacitor to GND. During soft start the output of the voltage error amplifier is clamped to the soft start capacitor voltage which is slowly charged by an internal current source. In UVLO, SS is held low.

SYNC: SYNC is a bidirectional pin for the oscillator. This pin can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The SYNC voltage is 3.6V when the oscillator capacitor, CT, is discharged. Otherwise it is 0V. If the recommended synchronization circuit is not used, a 1k or lower value resistor from SYNC to GND may be needed to increase the fall time of the signal at SYNC.

VCC: A voltage source connected to this pin supplies the power for the UC3827. It is recommended to bypass this pin to both GND and PGND ground connections with good quality high frequency capacitors.

VEA+: The non-inverting input of the voltage error amplifier.

VEA–: The inverting input of the voltage error amplifier.

VEAO: The output of the voltage error amplifier.

V+: Supply voltage for the buck output. The floating driver of the UC3827 uses the bootstrap technique which requires a reservoir capacitor to store the required energy for the on time of the buck switch. A diode must be connected from VCC to V+ to charge the reservoir capacitor. This diode must be able to withstand Vin. The reservoir capacitor must be connected between V+ and SRC and its voltage is monitored directly by the undervoltage lockout circuitry of the buck driver.

APPLICATION INFORMATION

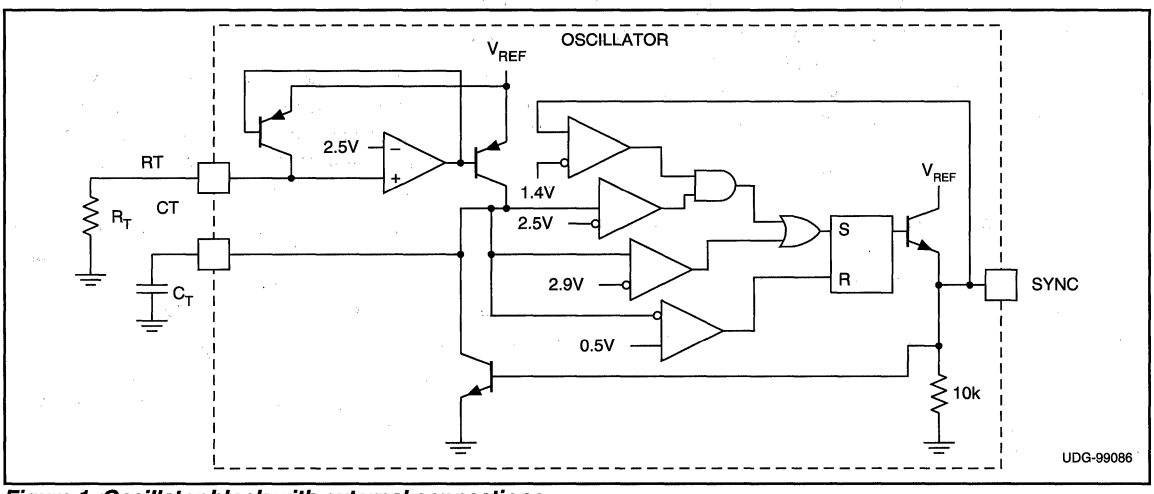


Figure 1. Oscillator block with external connections.

CIRCUIT BLOCK DESCRIPTION

PWM Oscillator. The oscillator block diagram with external connections is shown in Fig. 1. A resistor (R_T) connected to pin RT sets the linear charge current:

$$I_{RT} \approx \frac{2.5V}{R_T}$$

The timing capacitor (C_T) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4V threshold. After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. CT continues to discharge until it reaches a 0.5V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Fig. 2.

As shown in Fig. 3, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Fig. 1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 17% of each other to guarantee synchronization.

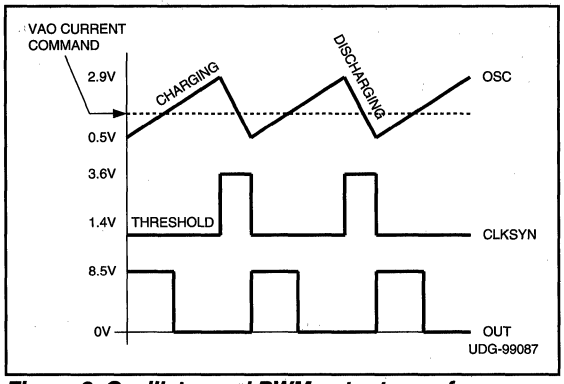


Figure 2. Oscillator and PWM output waveform.

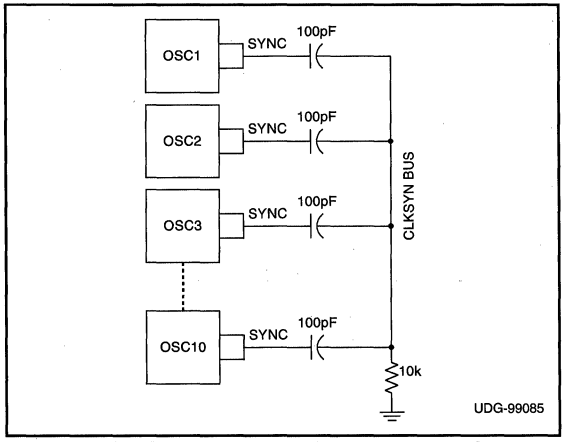


Figure 3. Oscillator synchronization connection diagram.

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UNITRODE

5-Bit Microprocessor Power Supply Controller

FEATURES

- 5-Bit Digital-to-Analog Converter (DAC)
- Supports 4-Bit and 5-Bit Microprocessor VID Codes
- Combined DAC/Voltage Monitor and PWM Functions
- 1% DAC/Reference
- Current Sharing
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 4Ω Totem Pole Output
- Chip Disable Function

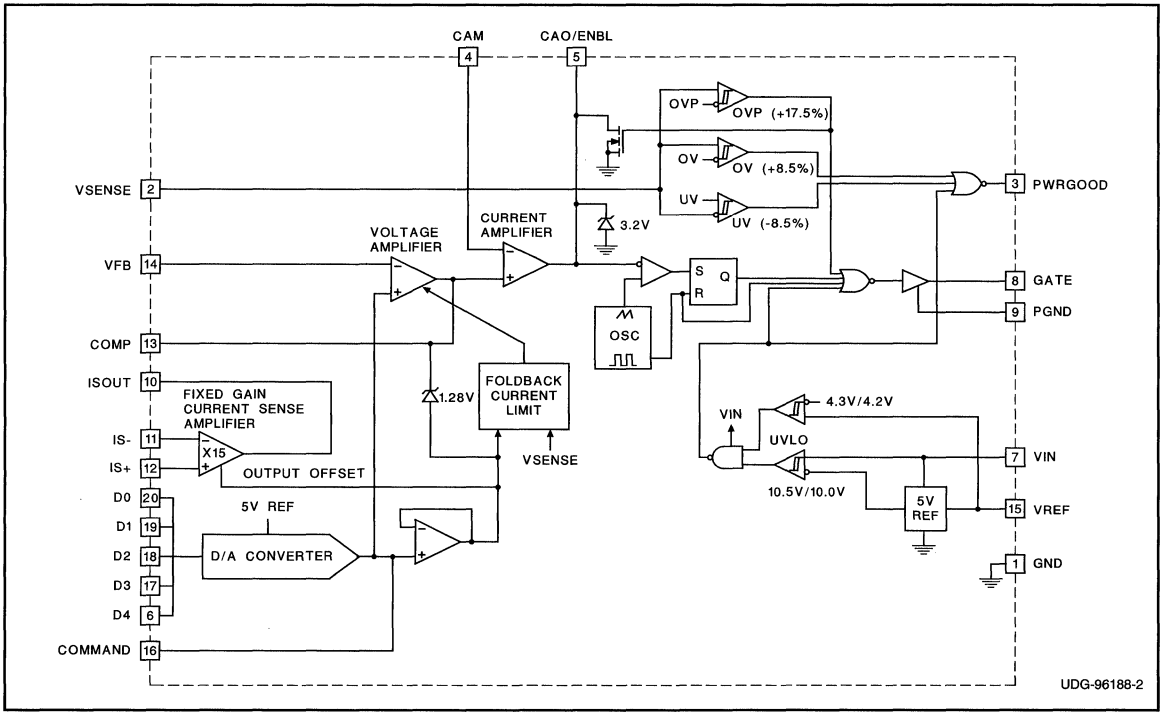
DESCRIPTION

The UCC3830-4/-5/-6 is a fully integrated single chip solution ideal for powering high performance microprocessors. The chip includes an average current mode PWM controller, has a fully integrated 5-Bit DAC, and includes an on-board precision reference and voltage monitor circuitry. The UCC3830-x converts 5VDC to an adjustable output, ranging from 3.5VDC down to 1.8VDC with 1% DC system accuracy (see Table 1). The UCC3830-x fully supports Intel's 4-bit Pentium® Pro and 5-bit Pentium® II VID codes.

The accuracy of the DAC/reference combination is 1%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 8.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 17.5%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8V.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

The voltage and current amplifiers have a 3MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz, depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 4Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC3830-x is specified for operation from 0°C to 70°C.

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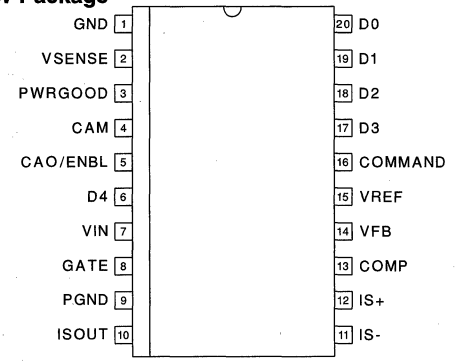
CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



ABSOLUTE MAXIMUM RATING

Input Supply Voltage VIN 15V
D0, D1, D2, D3, D4, VSENSE, VFB, IS+, IS–, CAM Inputs
Maximum Forced Voltage ..... –0.3V to 5.3V
PWRGOOD Output Maximum Voltage 5.5V
COMMAND Ouput Maximum Current ..... Internally Limited
Reference Output Current ..... Internally Limited
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into negative out of the specified terminal. Pulse is defined as a less than 10% duty cycle with a maximum duration of 500 µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

ORDERING INFORMATION

UCC3830□-□
- SEE FREQUENCY TABLE
- PACKAGE

***Note**: Consult factory for temperature range or package options not shown.*

FREQUENCY TABLE

	Frequency		
	100kHz	200kHz	400kHz
UCC3830-4	X		
UCC3830-5		X	
UCC3830-6			X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis		200	500	700	mV
Supply Current					
I_{IN}	D0 through D4 = Open		7.5	13.5	mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{VREF} = 0mA, 0°C < T_A < 70°C	–1		1	%
D0-D4 Voltage High	DX Pin Floating	4	5	5.2	V
D0-D4 Input Bias Current	DX Pin Tied to GND	–100	–70	–20	µA
OVP Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	10	17.5	25	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined	–0.5	–0.1	0.5	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VD0 = VD1 = VD2 = VD3 = VD4 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	5	8.5	12	%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	VSENSE = 2.0V			470	Ω
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1), D0 = D1 = D2 = D4 = Open, D3 = GND	–12	–8.5	–5	%
Hysteresis			20	30	mV
Voltage Error Amplifier					
Input Bias Current	V_{CM} = 3.0V	–0.5	–0.02	0.5	µA
Open Loop Gain	1.5V < V_{COMP} < 2.5V, D4 = D3 = D2 = D1 = GND, D0 = Open		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.5	–0.3	mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V	0.5	1		mA
Current Sense Amplifier					
Gain		14.25		15.25	V/V
Input Resistance			3		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.5	–0.3	mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V	5	8		mA
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V	–12		12	mV
Input Bias Current	V_{CM} = 3.0V		–0.1		µA
Open Loop Gain	1V < $V_{CAO/ENBL}$ < 2.5V		80		dB
Output Voltage High	V_{COMP} = 3V, V_{CAM} = 2.5V		3.2		V
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V		–1	–0.5	mA
Output Sinking Current	V_{CAM} = 3V, $V_{CAO/ENBL}$ = V_{COMP} = 2.5V	3	5		mA
Oscillator					
Frequency (-4)		85	100	115	kHz
Frequency (-5)		170	200	230	kHz
Frequency (-6)		340	400	460	kHz
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.2		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	70	ns
Fall Time	C_{GATE} = 3.3nF		15	70	ns
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; V_{SENSE} = $V_{COMMAND}$ = 3V		4.28		V
	$V_{COMMAND}$ = 3V, V_{SENSE} = 0		3.64		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D4 pins.

PIN DESCRIPTIONS

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO/ENBL below).

CAO/ENBL (Current Amplifier Output/Chip Enable): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO/ENBL exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO/ENBL voltage from rising excessively past the oscillator peak voltage for excellent transient response. The user can force this pin below 0.8V externally with an open collector, disabling the GATE drive.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 5-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. This voltage ranges from 1.8V to 3.5V as programmed by the 5-bit DAC according to Table 1. The GATE output is disabled when all 1s or illegal codes are presented at the 5 Bit DAC. The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D4 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D4, the most significant bit (MSB) as shown in Table 1. A bit is set low by being connected to GND. A bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

GATE (PWM Output, MOSFET Driver): This output provides a 4Ω totem pole driver. Use a series resistor between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS– (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + G_{CSA} • I • R_{SENSE}), where COMMAND is the voltage on the COMMAND pin, G_{CSA} is the fixed gain of the current sense amplifier, equal to 15, I is the current through the sense resistor, and R_{SENSE} is the value of the average current sensing resistor.

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor ≤ 0.10µF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 8.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

PIN DESCRIPTIONS (cont.)

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 8.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 17.5%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

TYPICAL PERFORMANCE CURVES

The curves shown in Figures 1 and 2 depict the typical high gain-bandwidth products for the UCC3830-x Voltage Amplifier, Current Amplifier and Current Sense Amplifiers. These high gain-bandwidth devices help achieve an excellent transient response to load and line changes.

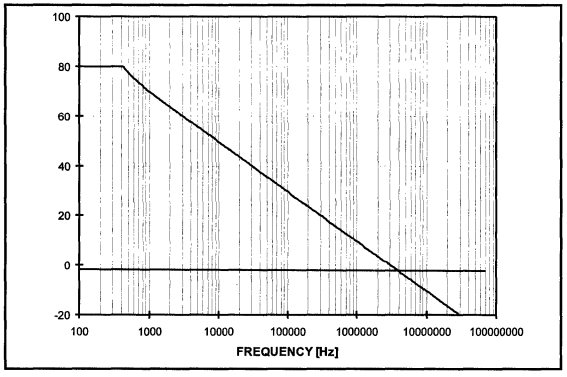


Figure 1. Open loop gain for UCC3830 voltage and current amplifier.

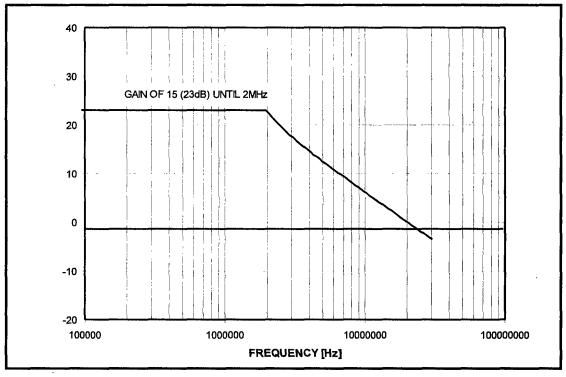


Figure 2. Current sense amplifier gain vs frequency.

APPLICATION INFORMATION

Short Circuit Current Limit

The short circuit current limit, ISC, is set according to:

$$ISC = \frac{1.28V}{RSENSE \bullet GCSA}$$

where RSENSE is the average current sense resistor and GCSA is the current sense amplifier gain. GCSA equals 15.

Example: Choose RSENSE to set the short circuit limit at 17A using the UCC3830-5

$$RSENSE = \frac{1.28V}{17A \bullet 15} = 0.005\Omega.$$

A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the load current.

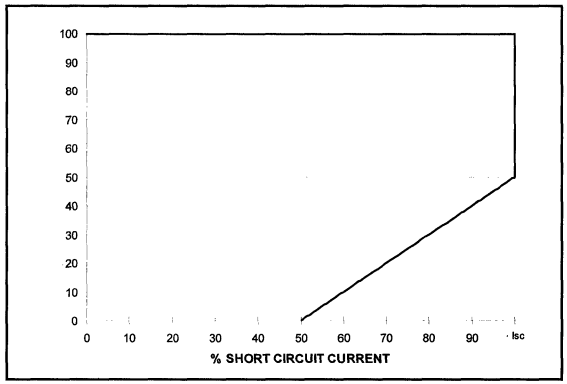


Figure 3. Short circuit foldback reduces stress on circuit components by reducing short circuit current.

APPLICATION INFORMATION (cont.)

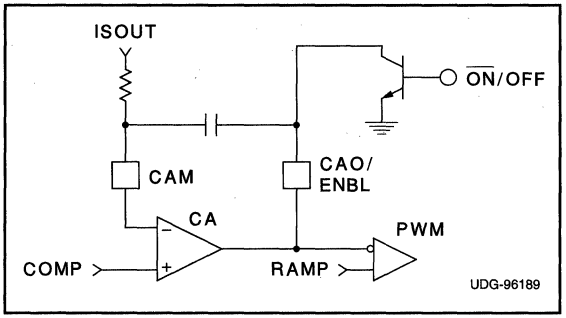


Figure 4. Disabling the UCC3830-x.

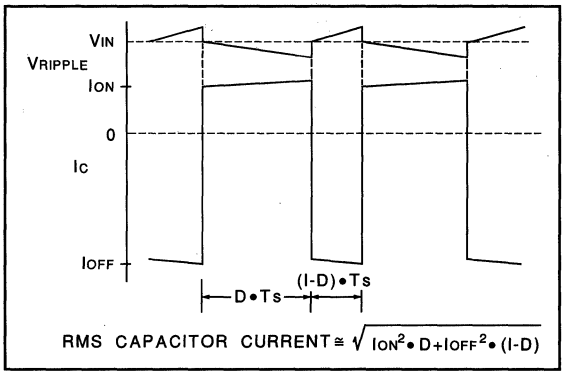


Figure 5. Input capacitors current waveform.

The UCC3830-x incorporates short circuit current foldback, as shown in Figure 3. When the output of the power supply is short circuited, the output voltage falls. When the output voltage reaches 1/2 of its nominal voltage (COMMAND/2) then the output current is reduced. This feature reduces the amount of current in the MOSFET, diode and capacitors, and insures high reliability.

Enabling/Disabling the UCC3830-x Gate Drive

The CAO/ENBL pin can be used to disable the UCC3830 gate drive by forcing this pin below 0.8V, as shown in Figure 4. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effectively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.

Setting the Output Voltage Using the DAC

The 5-bit Digital-to-Analog Converter (DAC) is programmed according to Table 1. The COMMAND voltage is always active as long as the UCC3830 VIN pin is above the undervoltage lockout voltage. The output gate drive, GATE, is disabled at certain DAC codes, as shown in Table 1. Disabling the gate drive disables the power supply.

Operating the 5-Bit Controller with Intel's 4-Bit Pentium Pro

The UCC3830-x 5-Bit Controller is completely backward compatible. When the fifth bit, D4 is left open (4-Bit Processor in circuit), the UCC3830-x acts as a 4-Bit controller with the COMMAND voltage fully compatible with Intel's 4-Bit Pentium® Pro family.

Table 1. Programming the command voltage for the UCC3830-x.

Digital Command					Command	GATEHI/GATELO	Digital Command					Command	GATEHI/GATELO
D4	D3	D2	D1	D0	Voltage	Status	D4	D3	D2	D1	D0	Voltage	Status
0	1	1	1	1	1.300	Note 1	1	1	1	1	1	2.000	Note 1
0	1	1	1	0	1.350	Note 1	1	1	1	1	0	2.100	Enabled
0	1	1	0	1	1.400	Note 1	1	1	1	0	1	2.200	Enabled
0	1	1	0	0	1.450	Note 1	1	1	1	0	0	2.300	Enabled
0	1	0	1	1	1.500	Note 1	1	1	0	1	1	2.400	Enabled
0	1	0	1	0	1.550	Note 1	1	1	0	1	0	2.500	Enabled
0	1	0	0	1	1.600	Note 1	1	1	0	0	1	2.600	Enabled
0	1	0	0	0	1.650	Note 1	1	1	0	0	0	2.700	Enabled
0	0	1	1	1	1.700	Note 1	1	0	1	1	1	2.800	Enabled
0	0	1	1	0	1.750	Note 1	1	0	1	1	0	2.900	Enabled
0	0	1	0	1	1.800	Enabled	1	0	1	0	1	3.000	Enabled
0	0	1	0	0	1.850	Enabled	1	0	1	0	0	3.100	Enabled
0	0	0	1	1	1.900	Enabled	1	0	0	1	1	3.200	Enabled
0	0	0	1	0	1.950	Enabled	1	0	0	1	0	3.300	Enabled
0	0	0	0	1	2.000	Enabled	1	0	0	0	1	3.400	Enabled
0	0	0	0	0	2.050	Enabled	1	0	0	0	0	3.500	Enabled

APPLICATION INFORMATION (cont.)

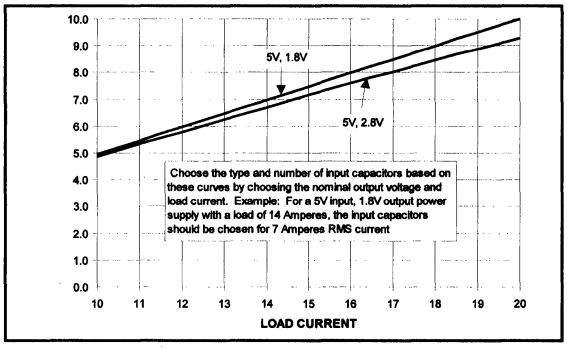


Figure 6. Load current vs RMS current for input capacitors.

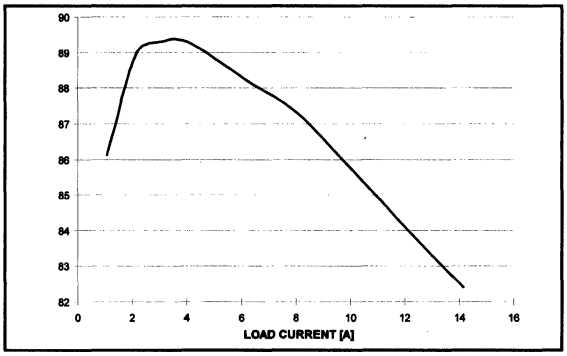


Figure 7. Efficiency of UCC3830-5 200kHz demo kit at 2.8V ouput.

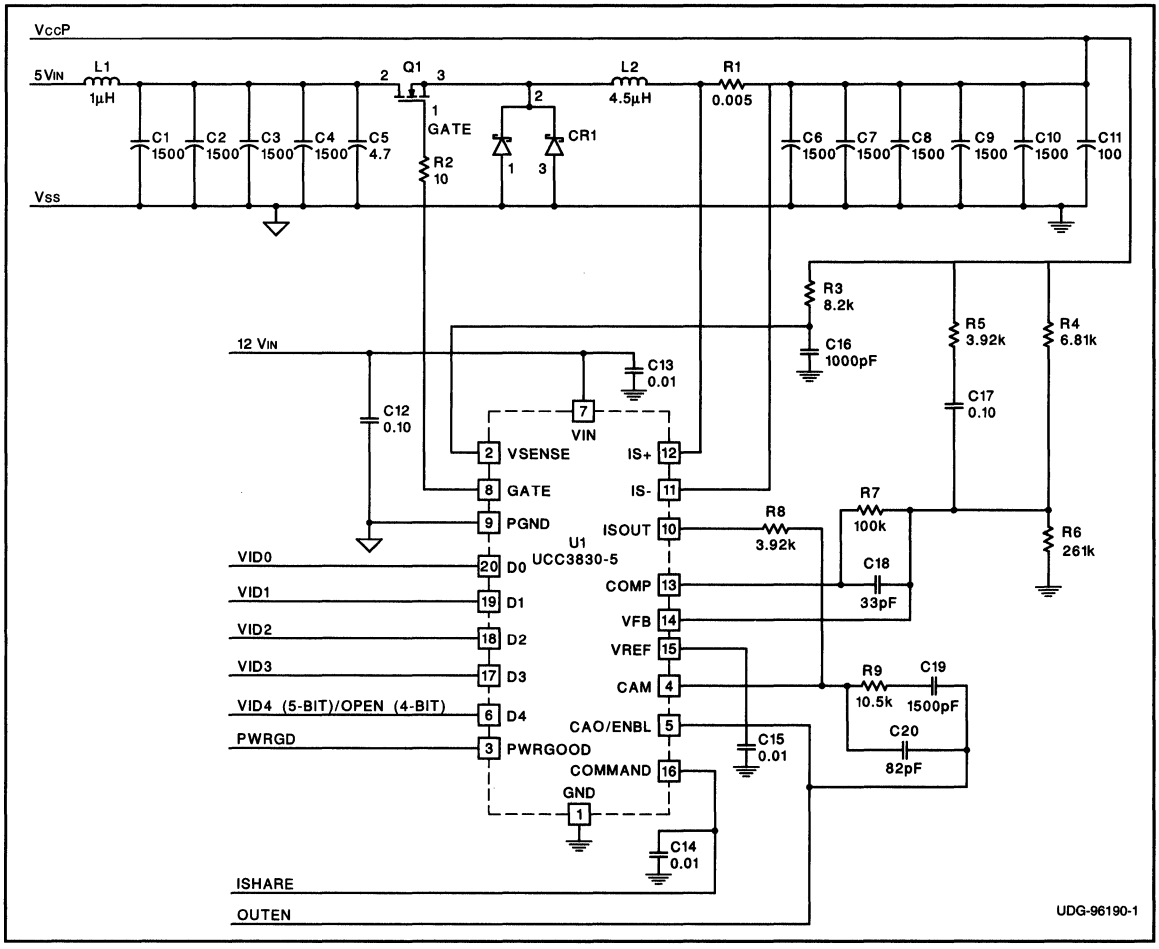


Figure 8. UCC3830 configured for 4-bit or 5-bit operation.

APPLICATION INFORMATION (cont.)

Choosing the Input Capacitor

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability and their voltage rating. The input capacitors must handle virtually all of the RMS current at the switching frequency, even if the circuit does not have an input inductor. The switching current in the input capacitors appears as shown in Figure 5.

The amount of RMS current in an Aluminum Electrolytic capacitor has a strong impact on the reliability and lifetime of the capacitor. Other factors which affect the life of an input capacitor are internal heat rise, external airflow, the amount of time that the circuit operates at maximum current and the operating voltage. The curves in Figure 6 show the RMS current handled by the total input capacitance in typical VRM circuits delivering 1.8V to 2.8V and powered from 5V.

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

Typical Application

The UCC3830-x is ideal for converting the 5.0V system bus into the required Pentium® Pro bus voltage. The 3.3V system bus can also be converted using the UCC3830-x when the Pentium® Pro requires lower bus voltages.

Table II. Parts list.

REFERENCE DESIGNATOR	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD
C12	0.10µF Ceramic	1206 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.01µF Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10µF Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10µF Ceramic	1206 SMD
C22	0.10µF Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB

Table II. Parts list. (cont.)

REFERENCE DESIGNATOR	DESCRIPTION	PACKAGE
R1	Dale/Vishay WSR-2 0.005Ω 1%	SMD Power Package
R2	10Ω, 5%, 1/16 Watt	0603 SMD
R3	8.2kΩ, 5%, 1/16 Watt	0603 SMD
R4	6.81kΩ, 1%, 1/16 Watt	0603 SMD
R5	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R6	261kΩ, 1%, 1/16 Watt	0603 SMD
R7	100kΩ, 1%, 1/16 Watt	0603 SMD
R8	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R9	10.5kΩ, 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

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application INFO available

UC1838A
UC2838A
UC3838A

Magnetic Amplifier Controller

FEATURES

- Independent 1% Reference
- Two Uncommitted, Identical Operational Amplifiers
- 100mA Reset Current Source with –120V Capability
- 5V to 40V Analog Operation
- 5W DIL Package

DESCRIPTION

The UC1838A family of magnetic amplifier controllers contains the circuitry to generate and amplify a low-level analog error signal along with a high voltage-compliant current source. This source will provide the reset current necessary to enable a magnetic amplifier to regulate and control a power supply output in the range of 2A to 20A.

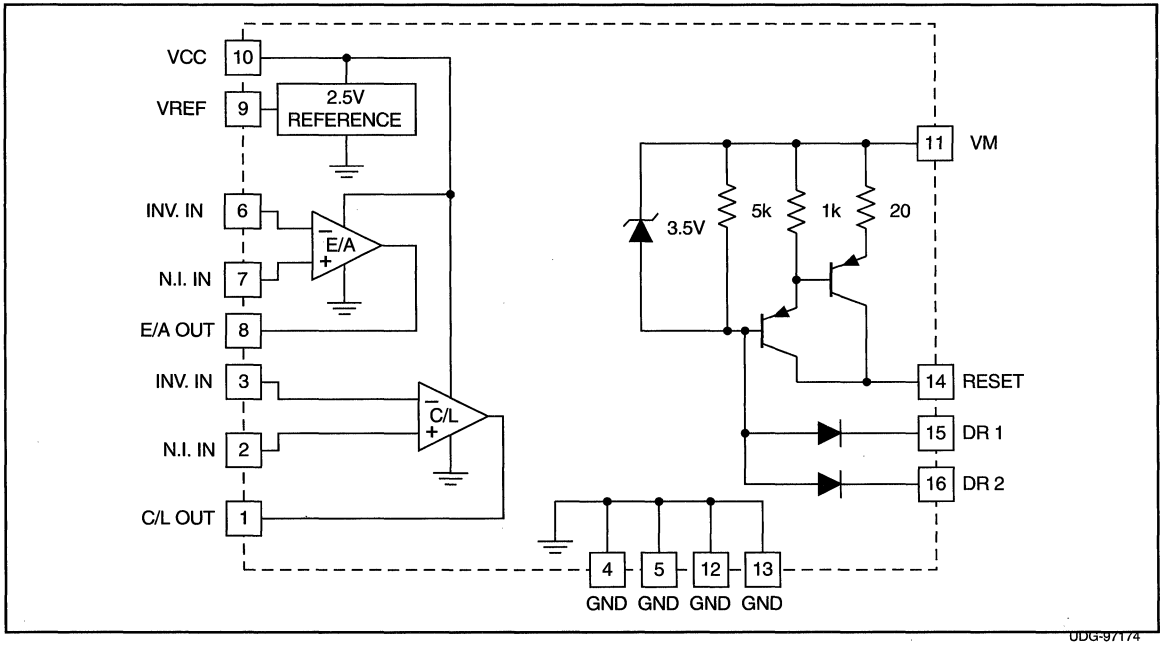
By controlling the reset current to a magnetic amplifier, this device will define the amount of volt-seconds the magnetic amplifier will block before switching to the conducting state. Magnetic amplifiers are ideal for post-regulators for multiple-output power supplies where each output can be independently controlled with efficiencies up to 99%. With a square or pulse-width-modulated input voltage, a magnetic amplifier will block a portion of this input waveform, allowing just enough to pass to provide a regulated output. With the UC1838A, only the magnetic amplifier coil, three diodes, and an output L-C filter are necessary to implement a complete closed-loop regulator.

The UC1838A contains a precision 2.5V reference, two uncommitted high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of magnetic amplifier reset current and with –120 volt capability.

These devices are available in a plastic "bat-wing" DIP for operation over a –20°C to +85°C temperature range and, with reduced power, in a hermetically sealed cerdip for –55°C to +125°C operation. Surface mount versions are also available.

This improved "A" version replaced the non "A" version formerly introduced.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 40V
Magnetic Amp. Source Voltage, V_M 40V
Reset Output Voltage, V_R ..... –120V
Total Current Source Voltage, $V_M - V_R$ ..... –140V
Amplifier Input Range ..... –0.3V to V_{CC}
Reset Input Current, I_{DR} ..... –10mA
Power Dissipation at T_A = 25°C
  Q, N, DP Package 2W
  J, L Package 1W
Power Dissipation at T (leads/case) = 25°C
  Q, N, DP Package 5W
  J, L Package 2W
Operating Temperature Range ..... –55°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

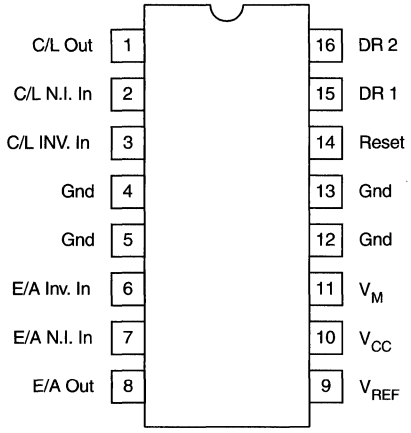
Note: All voltages are with respect to ground pins. All currents are positive into the specified terminal. Consult Packaging section of Databook for thermal limitations and considerations of package.

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1838AJ	–55°C to +125°C	Ceramic Dip
UC1838AL		CLCC
UC2838ADP	–20°C to +85°C	Power SOIC
UC2838AN		Plastic Dip
UC2838AQ		PLCC
UC3838ADP	0°C to +70°C	Power SOIC
UC3838AN		Plastic Dip
UC3838AQ		PLCC

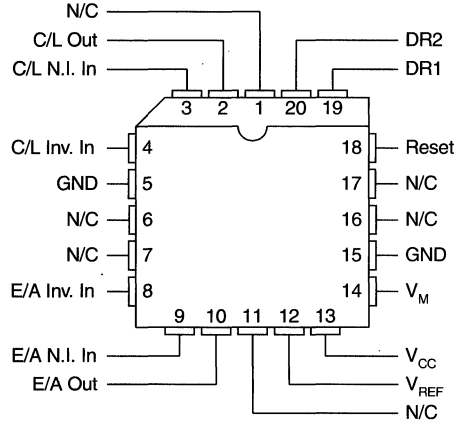
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DP Package



Note: All four ground pins must be connected to a common ground

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages

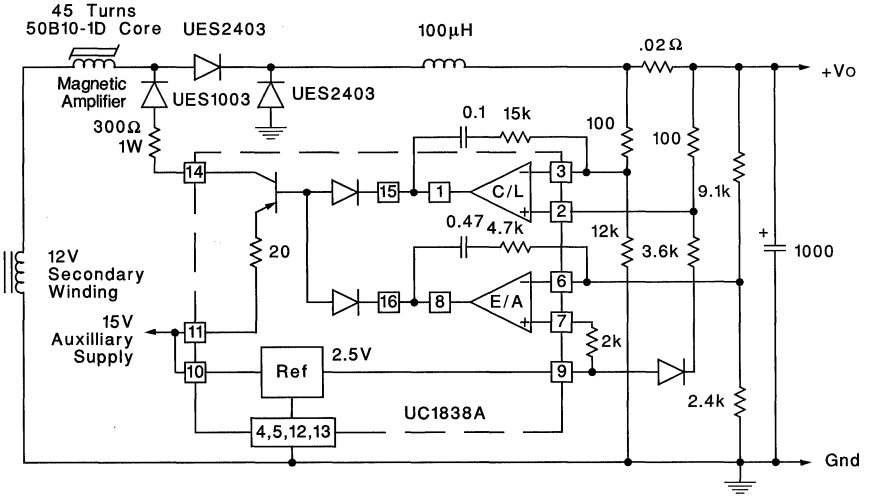


ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1838A, –20°C to +85°C for the UC2838A, and 0°C to +70°C for the UC3838A, V_{CC} = 20V, V_M = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1838A / UC2838A			UC3838A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Supply Current	V_{CC} = V_M = 40V		4	8		4	8	mA
Reference Output	T_A = 25°C	2.47	2.5	2.53	2.45	2.5	2.55	V
Line Regulation	V_{CC} = 5 to 30V		1	5		1	10	mV
Load Regulation	I_O = 0 to –2mA		5	20		5	20	mV
Short Circuit Current	V_{REF} = 0V		–30	–60		–30	–60	mA
Temperature Stability*	Over Operating Temp. Range		15	25		10	25	mV
Amplifier Section (Each Amplifier)								
Offset Voltage	V_{CM} = 2.5V			5			10	mV
Input Bias Current	V_{IN} = 0V			–1			–1	µA
Input Offset Current				100			100	nA
Minimum Output Swing		0.4		18	0.4		18	V
Output Sink Current	V_O = 5V	1	10	30	1	10	30	mA
Output Source Current	V_O = 0V	–1	–10	–20	–1	–10	–20	mA
A_{VOL}	V_O = 1 to 11V	100	120		100	120		dB
C_{MRR}	V_{IN} = 1 to 11V	70	80		70	80		dB
P_{SRR}	V_{CC} = 10 to 20V	70	100		70	100		dB
Gain Bandwidth*		0.6	0.8		0.6	0.8		MHz
Reset Drive Section								
Input Leakage	V_{DR} = 40V			10			10	µA
Output Leakage	V_R = –120V			–100			–100	µA
Input Current	I_R = –50mA		–1	–2		–1	–2	mA
Maximum Reset Current	I_{DR} = –3mA	–100	–120	–200	–100	–120	–200	mA
Transconductance	I_R = –10 to –50mA	.03	.042	.055	.03	.042	.055	A/V

** These parameters are guaranteed by design but not 100% tested in production.*

TYPICAL APPLICATION



+12V, 4A output with switching frequency = 50 kHz.

APPLICATION INFORMATION

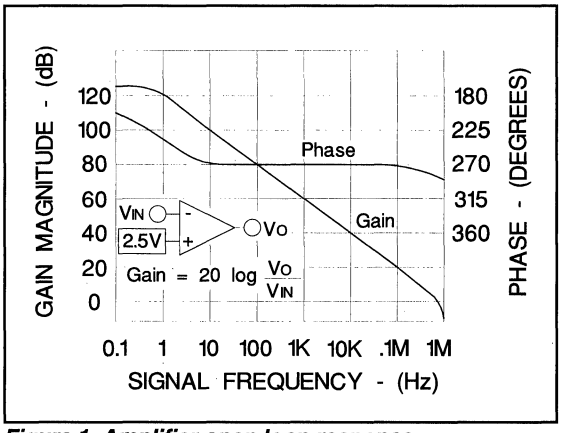


Figure 1. Amplifier open loop response.

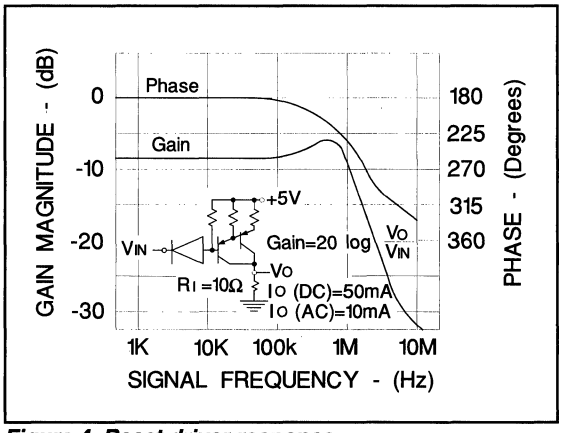


Figure 4. Reset driver response.

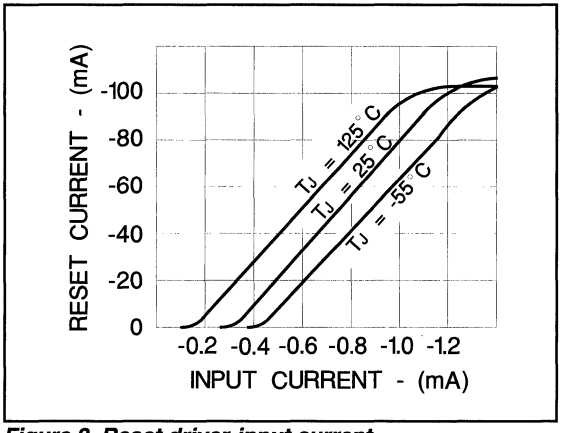


Figure 2. Reset driver-input current.

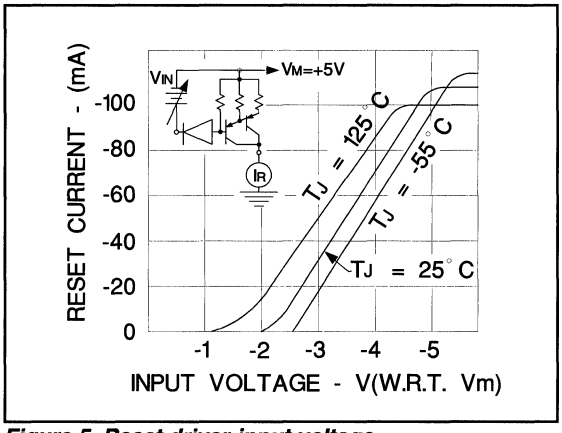


Figure 5. Reset driver-input voltage.

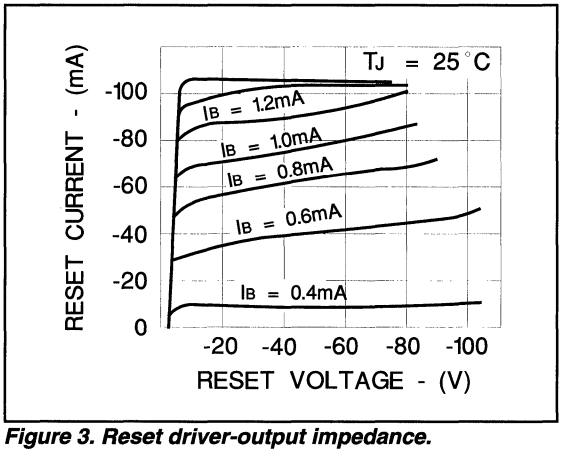


Figure 3. Reset driver-output impedance.

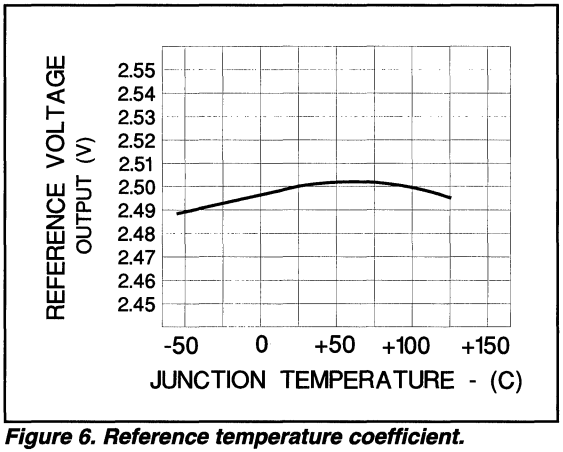


Figure 6. Reference temperature coefficient.

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Secondary Side Average Current Mode Controller

FEATURES

- Practical Secondary Side Control of Isolated Power Supplies
- Provides a Self Regulating Bias Supply From a High Input Voltage Using an External N-Channel Depletion Mode FET
- Onboard Precision, Fixed Gain, Differential Current Sense Amplifier
- Wide Bandwidth Current Error Amplifier
- 5V Reference
- High Current, Programmable Gm Amplifier Optimized to Drive Opto-couplers

DESCRIPTION

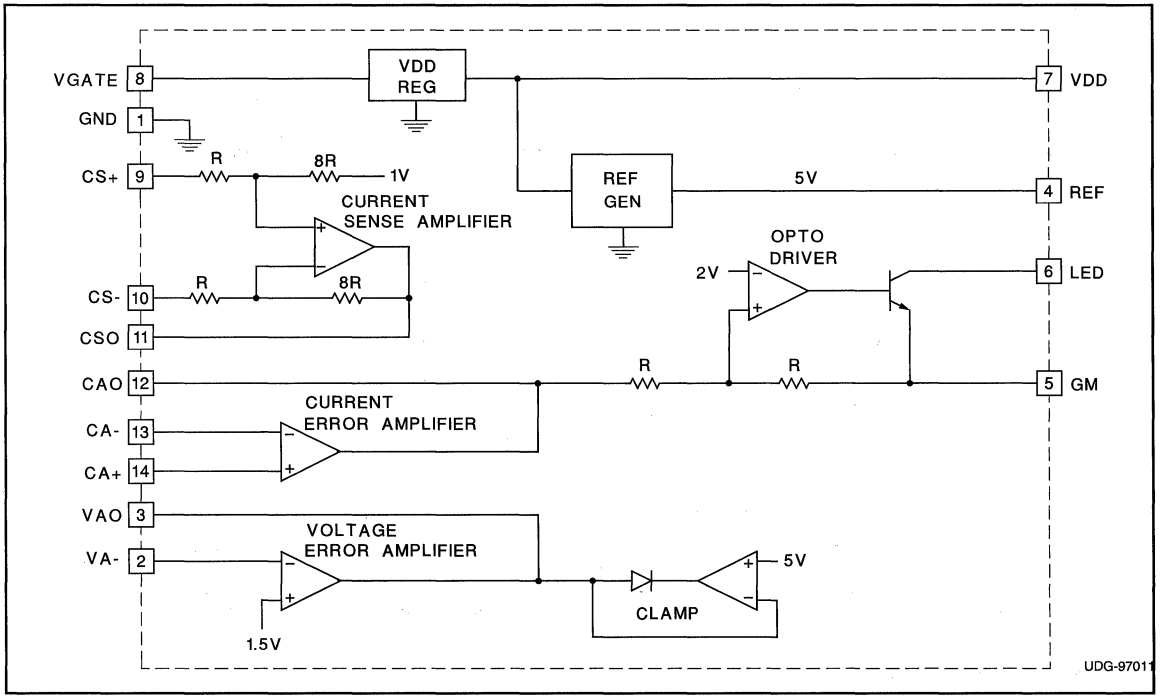
The UCC3839 provides the control functions for secondary side average current mode control in isolated power supplies. Start up, pulse width modulation and MOSFET drive must be accomplished independently on the primary side. Communication from secondary to primary side is anticipated through an opto-isolator.

Accordingly, the UCC3839 contains a fixed gain current sense amplifier, voltage and current error amplifiers, and a Gm type buffer/driver amplifier for the opto-isolator. Additional housekeeping functions include a precision 5V reference and a bias supply regulator.

Power for the UCC3839 can be generated by peak rectifying the voltage of the secondary winding of the isolation transformer. From this unregulated voltage, the UCC3839's bias supply regulator will generate its own 7.5V bias supply using an external, N-channel, depletion mode FET.

The UCC3839 can be configured for traditional average current mode control where the output of the voltage error amplifier commands the current error amplifier. It can also be configured for output voltage regulation with average current mode short circuit current limiting, employing two parallel control loops regulating the output voltage and output current independently.

BLOCK DIAGRAM



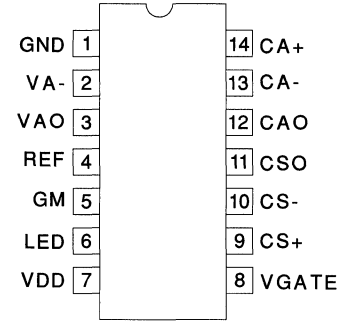
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Supply Current
(LED not connected) 2mA
(LED connected) 14mA
Analog Inputs ..... –0.3V to 15V
Power Dissipation at T_A = 60°C
(LED not connected) 20mW
(LED connected) 55mW
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-14, SOIC-14 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839 and –55°C to 125°C for the UCC1839. V_{LINE} = 10V, RG = 400Ω. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier					
VIO				10	mV
AVOL		60			dB
CMRR	V_{CM} = 0.5V to 5.5V	60			dB
PSRR	V_{LINE} = 10V to 20V	60			dB
CAO High	CA– = 1V, CA+ = 1.1V, I_{CAO} = –100µA	4.8		7	V
I_{CAO}	CA– = 1V, CA+ = 1.1V, CAO = 0.5V	–500		–250	µA
CAO Low	CA– = 1V, CA+ = 0.9V, I_{CAO} = 500µA		0.2	0.4	V
GBW	F = 100kHz, T_A = 25°C	3	5		MHz
Voltage Error Amplifier					
VA–		1.475	1.5	1.525	V
AVOL		60			dB
PSRR	V_{LINE} = 10V to 20V	60			dB
VAO High	I_{VAO} = –100µA to 100µA	4.8	5	5.2	V
I_{VAO}	VA– = 1.45V, VAO = 0.5V	–500		–250	µA
VAO Low	VA– = 1.55V, VAO = 0.5V, I_{VAO} = 500µA		0.2	0.4	V
GBW	(Note 1)	3	5		MHz
Current Sense Amplifier					
CSO Zero	CS+ = CS– = –0.3V to 5.5V, I_{CSO} = –100µA to 100µA	0.95	1	1.05	V
AV	CS+ = 0, CS– = 0mV to –200mV	7.8	8	8.2	V/V
Current Sense Amplifier (cont.)					
Slew Rate	CS+ = 0, CS– = 0mV to –0.5V	2	4		V/µs
CSO	CS+ = –200mV, CS– = –700mV	4.8	5	5.2	V
LED Driver					
I_{LED}	LED = 5.5V, CA– = 1V, CA+ = 1.1V, RG = 400		0	10	µA
	LED = 5.5V, CA– = 1V, CA+ = 0.9V, RG = 400	9	10	11	mA
Gm	LED = 5.5V, CAO = 1V to 3V, RG = 400	2.25	2.5	2.75	mS
Slew Rate	CAO = 2V to 2.5V, LED = 400Ω to 5.5V, RG = 400	2	4		V/µs

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, 0°C to 70°C for the UCC3839, –40°C to 85° for the UCC2839 and –55°C to 125°C for the UCC1839. V_{LINE} = 10V, RG = 400Ω. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Precision Reference					
REF	T_J = 25°C	4.95	5	5.05	V
	I_{REF} = 0mA to 1mA, V_{LINE} = 10V to 20V	4.9		5.1	V
VA+/REF		0.298	0.3	0.302	V/V
VDD Regulator					
VDD	IDD = 0mA to –15mA, V_{LINE} = 10V to 40V	7	7.5	8	V
I_{VDD}	V_{LINE} = 10V to 40V, CA– = 0V, CA+ = 1V, VA– = 2.9V, CS+ = CS– = 0, I_{REF} = 0		1.3	2	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CA–: Current Error Amplifier Negative Input.

CAO: Current Error Amplifier Output. Output source current is limited, and output sink current is guaranteed to be greater than the VAO output source current. Current loop compensation components are generally connected to CAO and CA–.

CA+: Current Error Amplifier Positive Input.

CS–: Current Sense Amplifier Negative Input.

CSO: Current Sense Amplifier Output. Internally set gain V_{OUT}/V_{IN} = 8 V_{IN} = 0V results in CSO = 1V.

CS+: Current Sense Amplifier Positive Input.

GM: Gm (transconductance) Programming Pin. Resistor R_{GM} = 400Ω to GND.

GND: Chip Ground.

LED: Output of LED Driver. Connect LED from VDD pin to LED.

REF: 5V Precision Reference Buffer Output. Minimum Decoupling Capacitance = 0.01µF

VA–: Voltage Error Amplifier Negative Input. Voltage Error Amplifier is internally referenced to 1.5V

VAO: Voltage Error Amplifier Output. In a two loop average current mode control configuration, VAO is connected to CA+ and is the current command signal. VAO is internally clamped not to exceed 5V for short circuit control. In a single loop voltage mode control configuration with a parallel average short circuit current control loop, VAO is connected directly to CAO. Output source current is limited, and output sink current is guaranteed to be greater than the CAO output source current.

VDD: 7.5V Regulator output. Supply for most of the chip. Minimum Decoupling Capacitance = 0.01µF

VGATE: External FET Gate Control Voltage.

APPLICATION INFORMATION

Fig. 1 shows a typical secondary side average current mode controller configuration using the UCC3839. In this configuration, output voltage is sensed and regulated by the voltage error amplifier. Its output, VAO provides the reference for the current error amplifier at the CA+ pin. VAO can be connected to CA+ directly or through a resistive divider depending on the particular application requirements.

Average current mode control needs accurate output current information which is provided by a low value current sense resistor. The voltage proportional to the converter's output current is sensed and amplified by the precision current sense amplifier of the chip. The onboard current sense amplifier has a gain of 8 and is intended for differential sensing of the shunt voltage with a common mode voltage range from 0V up to 5V. The output of the current sense amplifier, CSO is 1V for zero input which guarantees that the circuit can control currents down to 0A.

The CSO signal is fed to the CA– input of the current error amplifier through a resistor. The current error amplifier takes the VAO and CSO signals and generates the error signal for the pulse width modulator.

APPLICATION INFORMATION (cont.)

Since the PWM function is located on the primary side of the power converter the CAO signal must be sent across the safety isolation boundary. The UCC3839 anticipates an opto-coupler to provide isolation between primary and secondary. Therefore, CAO drives a transconductance amplifier that controls LED current in an opto-isolator. During start up and when CAO exceeds 4V, the current in the LED drops to zero. Maximum LED current is obtained during normal operation as CAO reaches its lowest potential. Its value is determined by the programming resistor value from the GM pin to circuit GND.

An alternative secondary side controller configuration is introduced in Fig. 2. In this circuit, the voltage and current control loops of the UCC3839 are connected parallel. It can be achieved by connecting the VAO and CAO pins together. The error amplifier with the lower output voltage controls the current in the opto-coupler providing the feedback signal for the PWM section on the primary side. Voltage regulation is still maintained by the voltage error amplifier until a user programmable output current is reached. At this time CAO will take control over the Gm amplifier and the output current of the converter will be regulated while the output voltage falls below its nominal value. This current level is set at the CA+ input by a resistive divider from the 5V reference of the chip.

Since the chip is powered from a peak rectifier which maintains the bias supply for the UCC3839 even under short circuit conditions, both of these techniques can be used to eliminate the short circuit runaway problem in isolated power supplies using peak current mode control on the primary side.

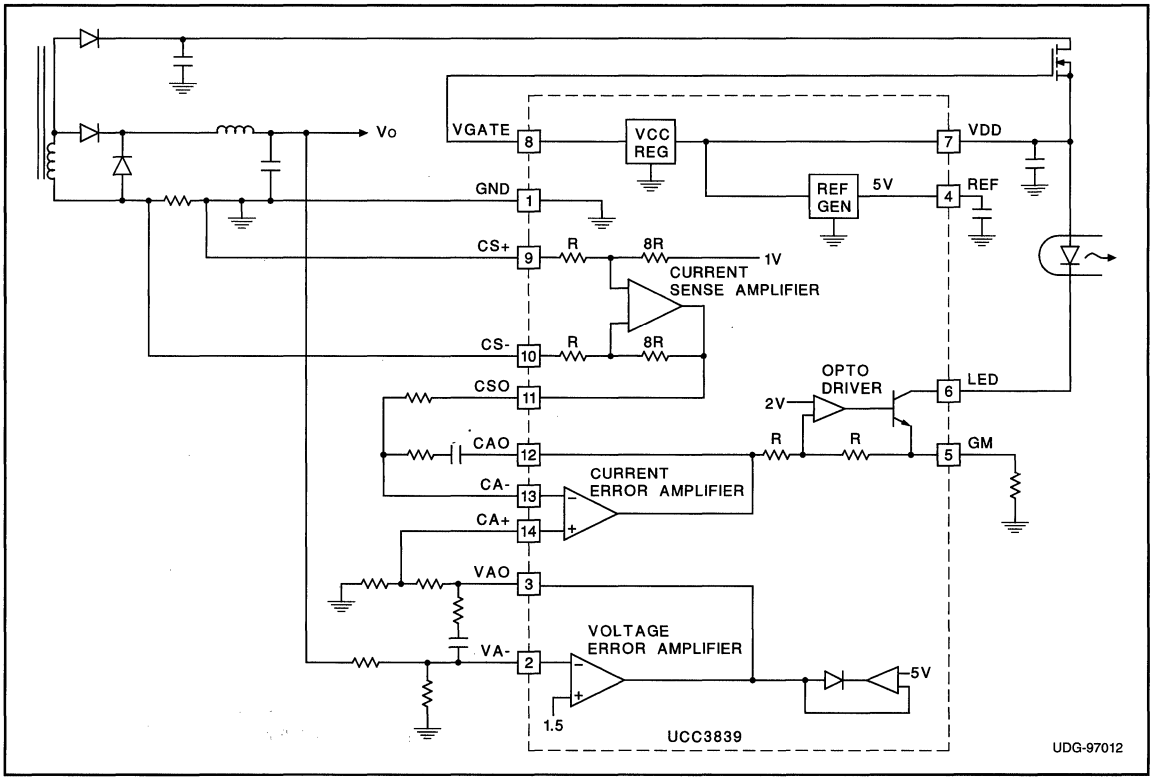


Figure 1. Secondary side average current mode controller.

APPLICATION INFORMATION (cont.)

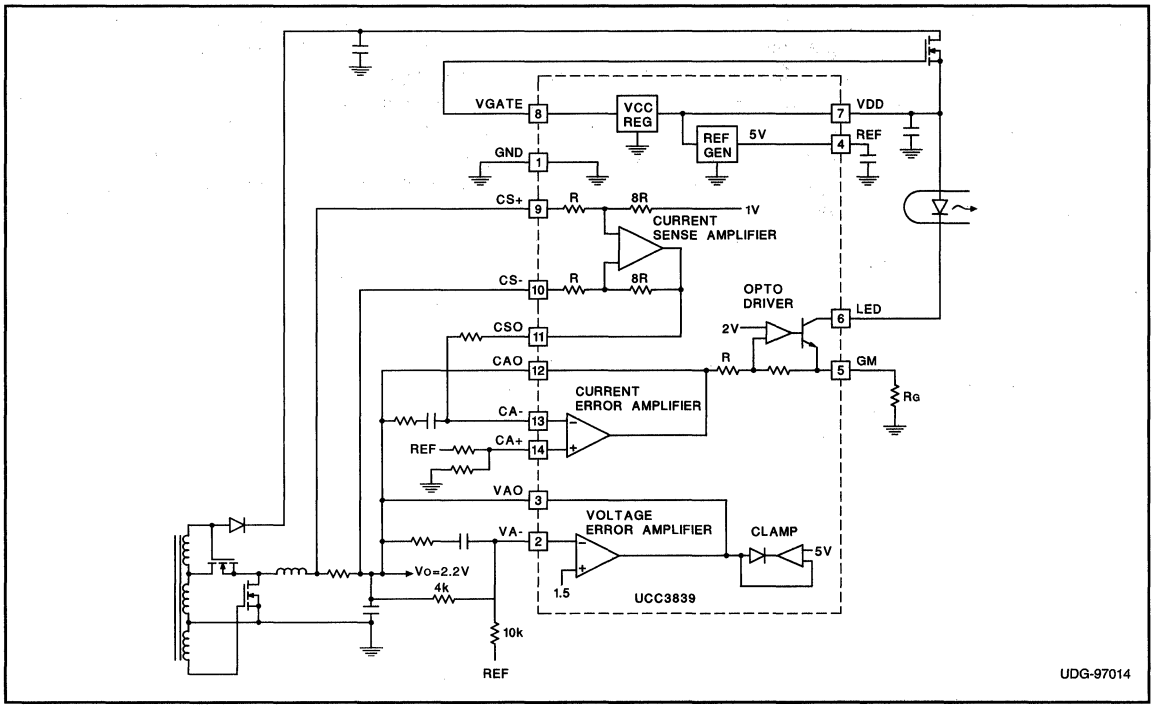


Figure 2. Voltage mode with average current short circuit limit.

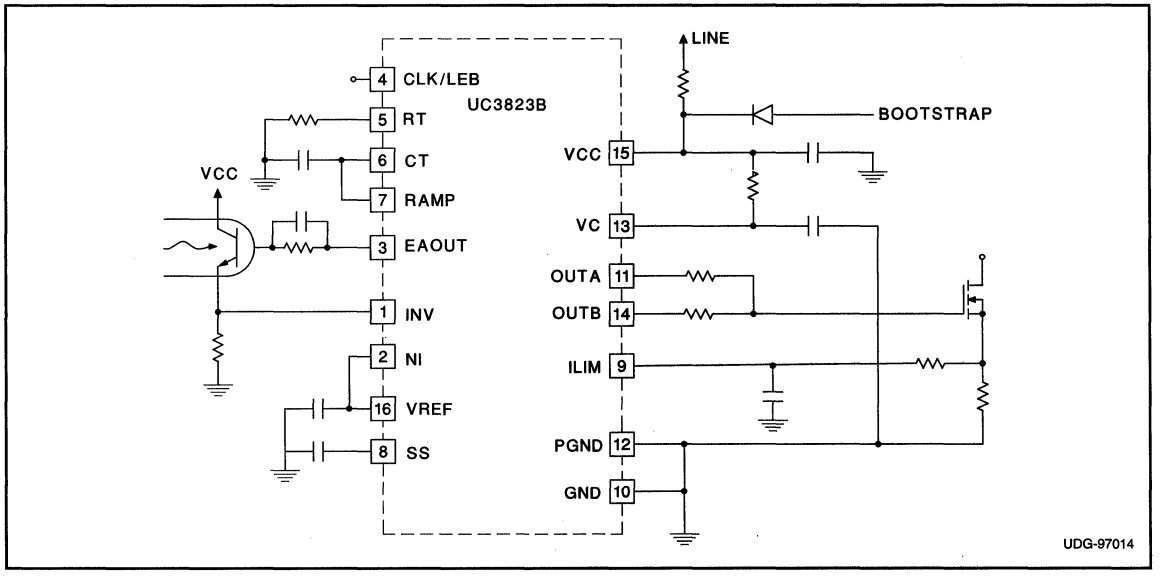


Figure 3. Typical primary side circuit for use with secondary side average current mode controller.

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UNITRODE

application INFO available

UC1841
UC2841
UC3841

Programmable, Off-Line, PWM Controller

3

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-current, Off-line Start Circuit
- Voltage Feed Forward or Current Mode Control
- Guaranteed Duty Cycle Clamp
- PWM Latch for Single Pulse per Period
- Pulse-by-Pulse Current Limiting Plus Shutdown for Over-Current Fault
- No Start-up or Shutdown Transients
- Slow Turn-on Both Initially and After Fault Shutdown
- Shutdown Upon Over- or Under-Voltage Sensing
- Latch Off or Continuous Retry After Fault
- PWM Output Switch Usable to 1A Peak Current
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL Package

DESCRIPTION

The UC1841 family of PWM controllers has been designed to increase the level of versatility while retaining all of the performance features of the earlier UC1840 devices. While still optimized for highly-efficient bootstrapped primary-side operation in forward or flyback power converters, the UC1841 is equally adept in implementing both low and high voltage input DC to DC converters. Important performance features include a low-current starting circuit, linear feed-forward for constant volt-second operation, and compatibility with either voltage or current mode topologies.

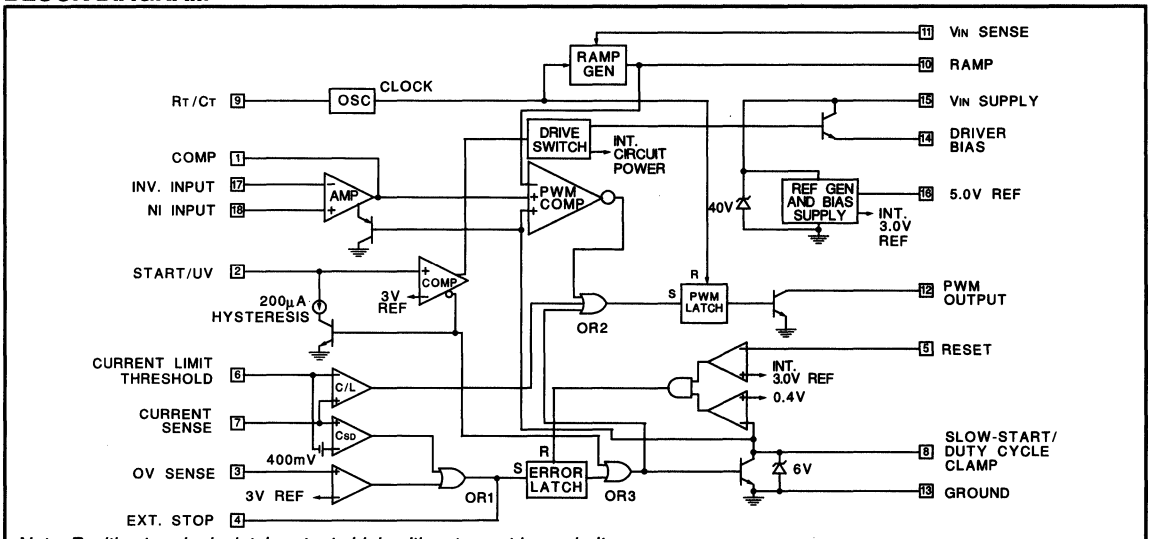
In addition to start-up and normal regulating PWM functions, these devices include built in protection from over-voltage, under-voltage, and over-current fault conditions with the option for either latch-off or automatic restart.

While pin compatible with the UC1840 in all respects except that the polarity of the External Stop has been reversed, the UC1841 offers the following improvements:

1. Fault latch reset is accomplished with slow start discharge rather than recycling the input voltage to the chip.
2. The External Stop input can be used for a fault delay to resist shutdown from short duration transients.
3. The duty-cycle clamping function has been characterized and specified.

The UC1841 is characterized for -55°C to +125°C operation while the UC2841 and UC3841 are designed for -25°C to +85°C and 0°to +70°C, respectively.

BLOCK DIAGRAM



Note: Positive true logic, latch outputs high with set, reset has priority.

6/93

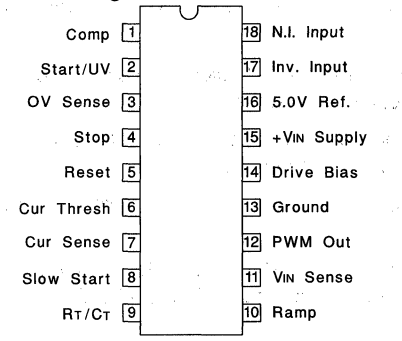
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, +V_{IN} (Pin 15) (Note 2)
  Voltage Driven ..... +32V
  Current Driven, 100mA maximum ..... Self-limiting
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Stop Input (Pin 4) ..... -0.3 to +5.5V
Comparator Inputs
  (Pins 1, 7, 9-11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

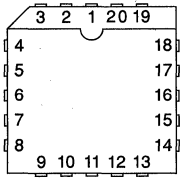
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal.
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



PACKAGE PIN FUNCTIONS	
FUNCTION	**PIN**
Comp	1
Start/UV	2
OV Sense	3
Stop	4
Reset	5
CUR Thresh	7
CUR Sense	8
Slow Start	9
RT/CT	10
Ramp	11
VIN Sense	12
PWM Out	13
Ground	14
Drive Bias	15
+VIN Supply	17
5.0V REF	18
Inv. Input	19
N.I. Input	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		10	14		10	14	mA
Supply OV Clamp	I_{IN} = 20mA	33	40	45	33	40	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Temperature Stability	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Temperature Stability	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1841, -25°C to +85°C for the UC2841, and 0°C to +70°C for the UC3841; V_{IN} = 20V, R_T = 20kΩ, C_T = .001mfd, R_R = 10kΩ, C_R = .001mfd, Current Limit Threshold = 200mV, T_A = T_J.

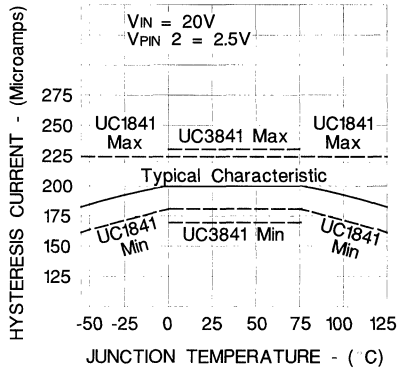
PARAMETER	TEST CONDITIONS	UC1841 / UC2841			UC3841			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = -10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O= 1 to 3V	60	66		60	66		dB
Output Swing (Max. Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth*	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate*	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range* (other than zero)	Minimum Total Continuous Range, Ramp Peak < 4.2V	4		95	4		95	%
50% Duty Cycle Clamp	R_{SENSE} to V_{REF} = 10k	42	47	52	42	47	52	%
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Output Leakage	V_{OUT} = 40V		0.1	10		0.1	10	µA
Comparator Delay*	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN} - V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range*		-0.4		3.0	-0.4		3.0	V
Current Limit Delay*	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

** These parameters are guaranteed by design but not 100% tested in production.*

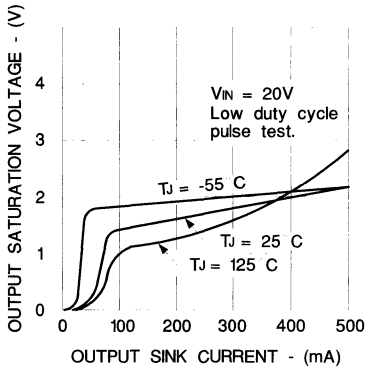
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first order correction factor $\approx 0.3 \log (C_T \times 10^{12})$.
2. Ramp Generator	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$ C_R is normally selected $\leq C_T$ and its value will have some effect upon valley voltage. Limiting the minimum value for I_{SENSE} will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ± 2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch	Transistor capable of sinking current to ground which is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400mA saturated with peak capacitance discharge in excess of one amp.
SEQUENCING FUNCTIONS	
1. Start/UV Sense	With an increasing voltage, it generates a turn-on signal and releases the slow-start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias	Supplies drive current to external power switch to provide turn-on bias.
4. Slow Start	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (typically 3V) b. Stop > 2.4V (typically 1.6V) c. Current Sense 400mV over threshold (typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin 5 < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop	A voltage over 1.2V will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a typical delay of 13ms/µF.

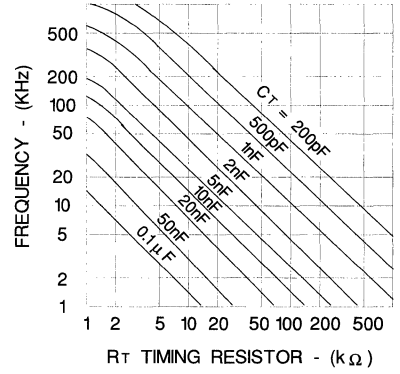
Start/UV Hysteresis



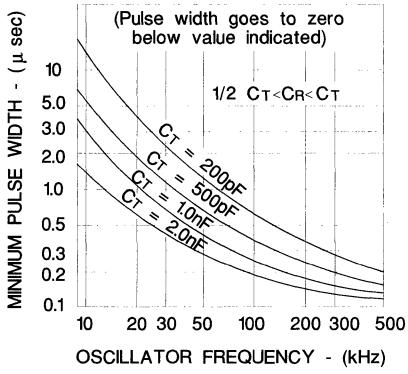
PWM Output-Saturation Voltage



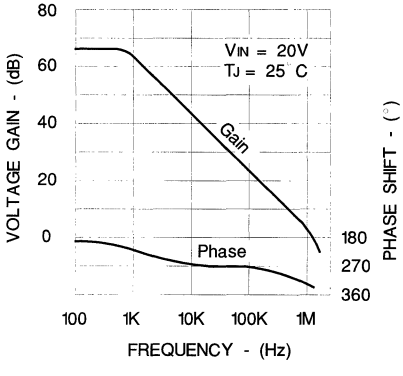
Oscillator Frequency



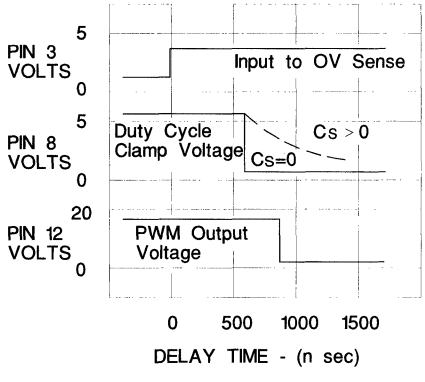
PWM Output Minimum Pulse Width



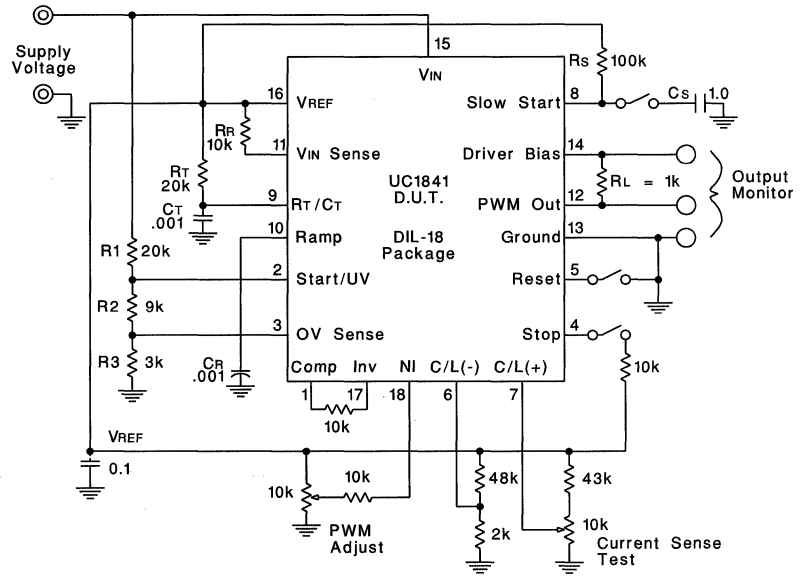
Error Amplifier Open Loop Gain and Phase



Shutdown Timing



OPEN-LOOP TEST CIRCUIT



Nominal Frequency $= \frac{1}{R_T C_T} = 50\ \text{kHz}$

Start Voltage $= 3\left(\frac{R1+R2+R3}{R2+R3}\right) + 0.2R1 = 12\text{V}$

UV Fault Voltage $= 3\left(\frac{R1+R2+R3}{R2+R3}\right) = 8\text{V}$

OV Fault Voltage $= 3\left(\frac{R1+R2+R3}{R3}\right) = 32\text{V}$

Current Limit = 200mV

Current Fault Voltage = 600mV

Duty Cycle Clamp = 50%

FLYBACK APPLICATION (A)

In this application (see Figure A, next page), complete control is maintained on the primary side. Control power is provided by RIN and CIN during start-up, and by a primary-referenced low voltage winding, N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling – a task made even easier with the UC1841's feed–forward line regulation.

An extension to this application for more precise regulation would be the use of the UC1901 Isolated Feedback Generator for direct closed-loop control to an output.

Not shown, are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application; however, one example of power transistor interfacing is provided on the following page.

REGULATOR APPLICATION (B)

With the addition of a level shifting transistor, Q1, the UC1841 is an ideal control circuit for DC to DC converters such as the buck regulator shown in Figure B opposite. In addition to providing constant current drive pulses to the PIC661 power switch, this circuit has full fault protection and high speed dynamic line regulation due to its feed-forward capability. An additional feature is the ability to work with high input line voltages – in this case, up to 60V – with internal protective clamping.

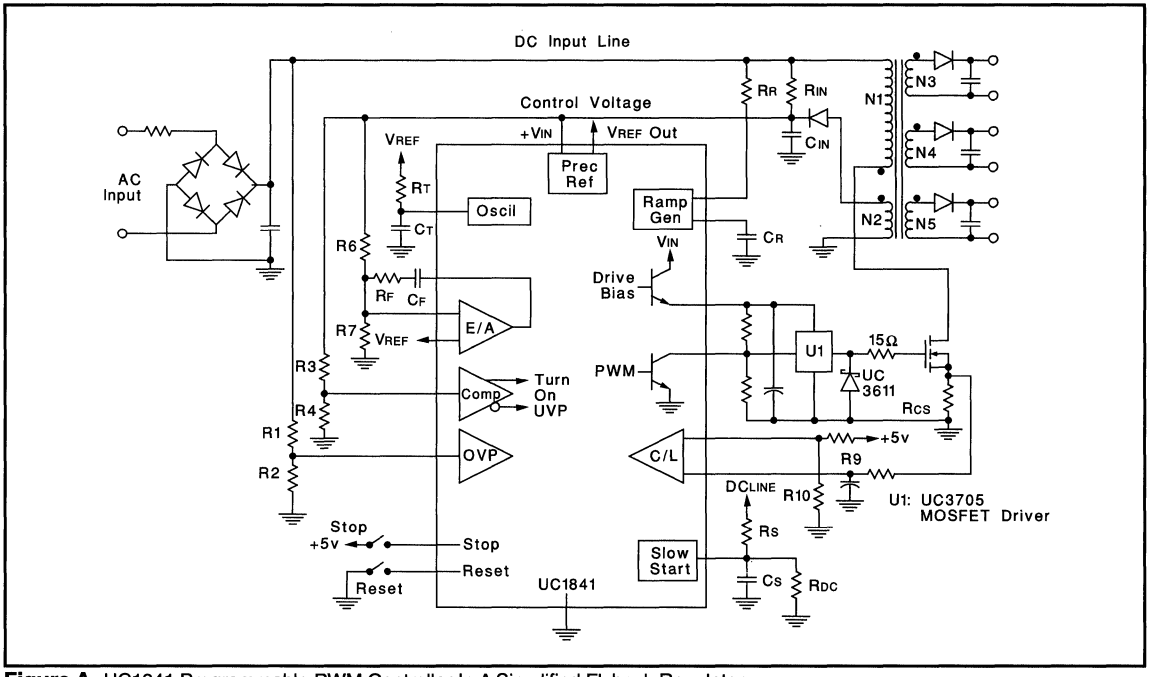


Figure A. UC1841 Programmable PWM Controller In A Simplified Flyback Regulator

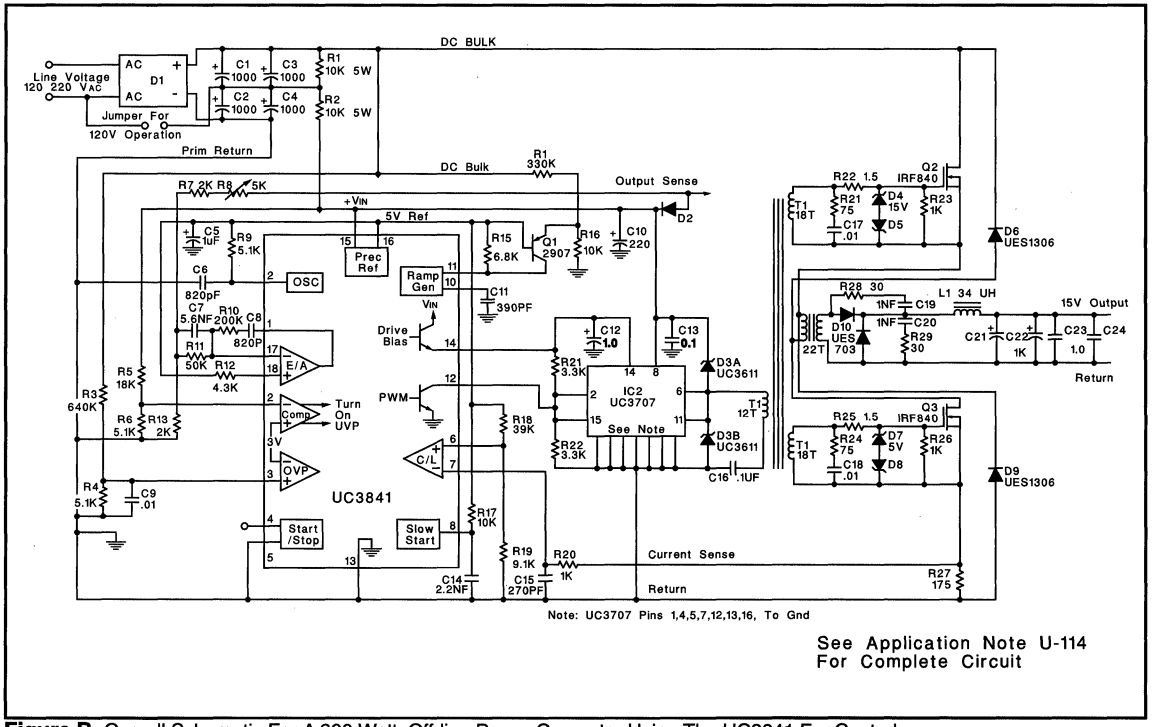
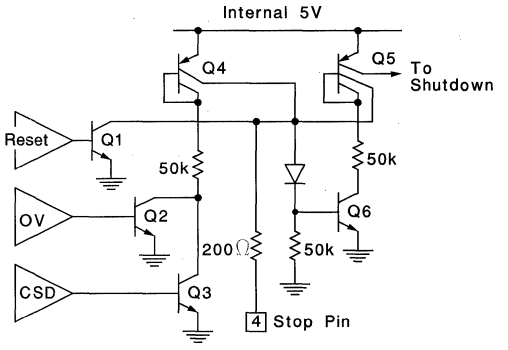


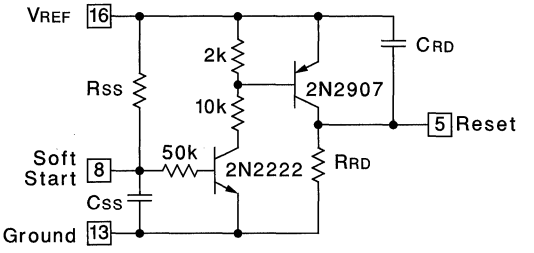
Figure B. Overall Schematic For A 300 Watt, Off-line Power Converter Using The UC3841 For Control

ERROR LATCH INTERNAL CIRCUITRY

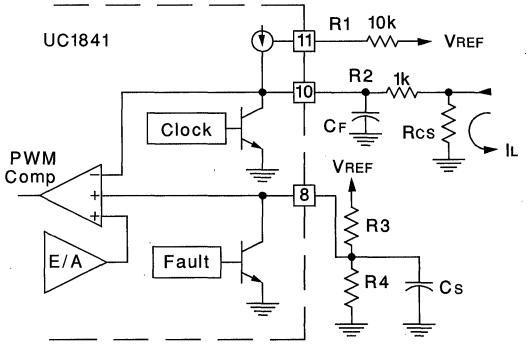


The Error Latch consists of Q5 and Q6 which, when both on, turns off the PWM Output and pulls the Slow-Start pin low. This latch is set by either the Over-Voltage or Current Shutdown comparators, or by a high signal on Pin 4. Reset is accomplished by either the Reset comparator or a low signal on Pin 4. An activation time delay can be provided with an external capacitor on Pin 4 in conjunction with the ≈ 100µA collector current from Q4.

PROGRAMMABLE SOFT START AND RESTART DELAY CIRCUIT

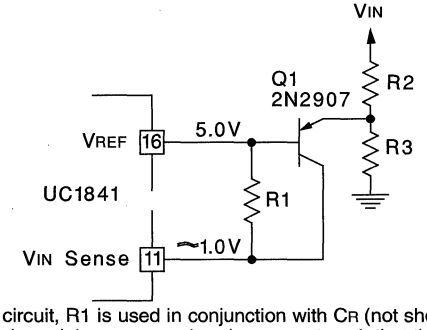


Restart Delay = (.51)(RRD)(CRD)



Since Pin 10 is a direct input to the PWM comparator, this point can also serve as a current sense port for current mode control. In this application, current sensing is ground referenced through RCS. Resistor R1 sets a 400mV offset across R2 (assuming R2 > RCS) so that both the Error Amplifier and Fault Shutdown can force the current completely to zero. R2 is also used along with CF as a small filter to attenuate leading-edge spikes on the load current waveform. In this mode, current limiting can be accomplished by divider R3/R4 which forms a clamp overriding the output of the Error Amplifier.

CURRENT MODE CONTROL



In this circuit, R1 is used in conjunction with CR (not shown) to establish a minimum ramp charging current such that the ramp voltage reaches 4.2V at the required maximum output pulse width.

The purpose of Q1 is to provide an increasing ramp current above a threshold established by R2 and R3 such that the duty cycle is further reduced with increasing VIN.

The minimum ramp current is:

$$I_{R(MIN)} = \frac{V_{REF} - V_{IN\ SENSE}}{R1} \approx \frac{4V}{R1}$$

The threshold where VIN begins to add extra ramp current is:

$$V_{IN} \approx 5.6V\left(\frac{R2 + R3}{R3}\right)$$

Above the threshold, the ramp current will be:

$$I_R\ (VARIAB) \approx \frac{4}{R1} + \frac{V_{IN} - 5.6}{R2} - \frac{5.6}{R3}$$

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UNITRODE

application INFO available

UC1842/3/4/5
UC2842/3/4/5
UC3842/3/4/5

Current Mode PWM Controller

FEATURES

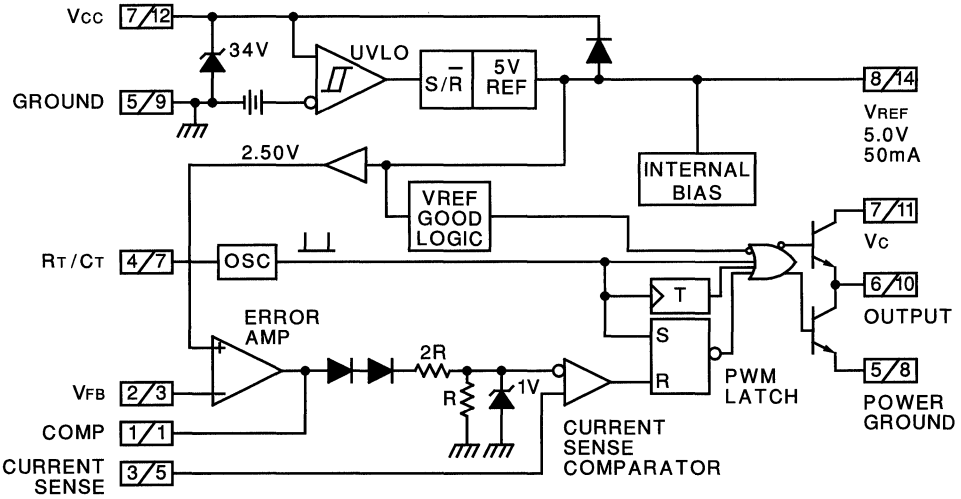
- Optimized For Off-line And DC To DC Converters
- Low Start Up Current (<1mA)
- Automatic Feed Forward Compensation
- Pulse-by-pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500khz Operation
- Low RO Error Amp

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N Channel MOSFETs, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.4V and 7.6V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to 50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flop which blanks the output off every other clock cycle.

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844 and 1845.

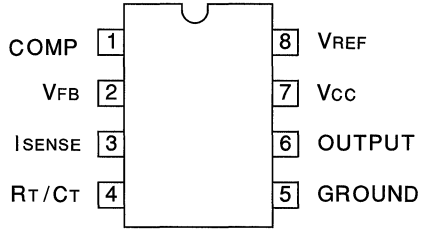
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (Icc <30mA) . . . . . Self Limiting
Output Current . . . . . ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) . . . . . -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SOIC-14) 725mW
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

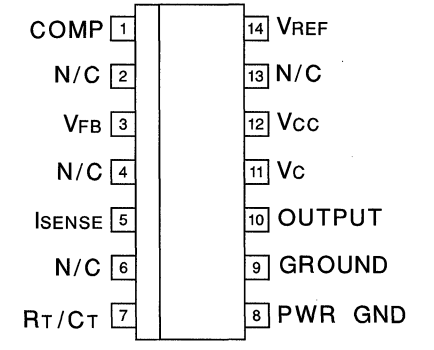
Note 1: All voltages are with respect to Pin 5.
All currents are positive into the specified terminal.
Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

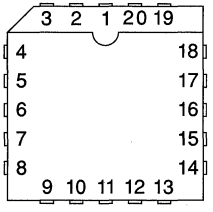
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D8 Package



SOIC-14 (TOP VIEW)
D Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
COMP	2
N/C	3
N/C	4
VFB	5
N/C	6
ISENSE	7
N/C	8
N/C	9
RT/CT	10
N/C	11
PWR GND	12
GROUND	13
N/C	14
OUTPUT	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for -55°C ≤ T_A ≤ 125°C for the UC184X; -40°C ≤ T_A ≤ 85°C for the UC284X; 0°C ≤ T_A ≤ 70°C for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T =3.3nF, T_A=T_J.

PARAMETER	TEST CONDITIONS	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2) (Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp. (Note 2)	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = 25°C (Note2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\,4}$ peak to peak (Note 2)		1.7			1.7		V
Error Amp Section								
Input Voltage	$V_{PIN\,1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	(Note 2) T_J = 25°C	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\,2}$ = 2.7V, $V_{PIN\,1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\,2}$ = 2.3V, $V_{PIN\,1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\,2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\,2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Notes 3 and 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\,1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3) (Note 2)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	$V_{PIN\,3}$ = 0 to 2V (Note 2)		150	300		150	300	ns

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\,2}$ = 0.
Note 4: Gain defined as

$$A = \frac{\Delta\, VPIN\,1}{\Delta\, VPIN\,3},\ 0 \le VPIN3 \le 0.8V$$

Note 5: Adjust V_{CC} above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843.
Output frequency is one half oscillator frequency for the UC1844 and UC1845.
Note 7: Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$Temp\ Stability = \frac{V_{REF}(max) - VREF(min)}{TJ(max) - TJ(min)}$$

V_{REF} (max) and V_{REF} (min) are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $-55°C \le T_A \le 125°C$ for the UC184X; $-40°C \le T_A \le 85°C$ for the UC284X; $0°C \le T_A \le 70°C$ for the 384X; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF, $T_A = T_J$.

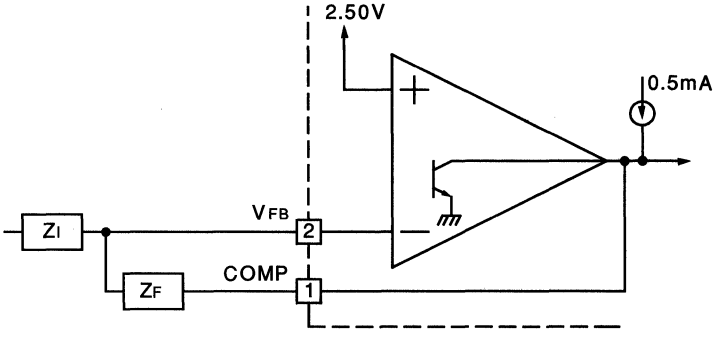
PARAMETER	TEST CONDITION	UC1842/3/4/5 UC2842/3/4/5			UC3842/3/4/5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Under-voltage Lockout Section								
Start Threshold	X842/4	15	16	17	14.5	16	17.5	V
	X843/5	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operating Voltage After Turn On	X842/4	9	10	11	8.5	10	11.5	V
	X843/5	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	X842/3	95	97	100	95	97	100	%
	X844/5	46	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.5	1		0.5	1	mA
Operating Supply Current	$V_{PIN\,2} = V_{PIN\,3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: These parameters, although guaranteed, are not 100% tested in production.
Note 3: Parameter measured at trip point of latch with $V_{PIN\,2}$ = 0.
Note 4: Gain defined as:

$$A = \frac{\Delta\, VPIN\,1}{\Delta\, VPIN\,3};\ 0 \le VPIN\,3 \le 0.8V.$$

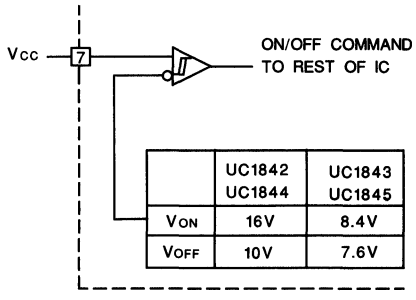
Note 5: Adjust V_{CC} above the start threshold before setting at 15V.
Note 6: Output frequency equals oscillator frequency for the UC1842 and UC1843. Output frequency is one half oscillator frequency for the UC1844 and UC1845.

ERROR AMP CONFIGURATION

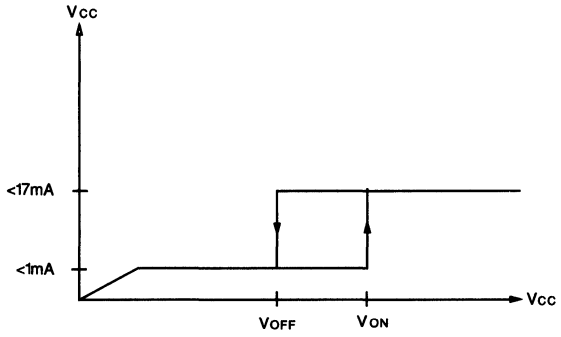


Error Amp can Source or Sink up to 0.5mA

UNDER-VOLTAGE LOCKOUT

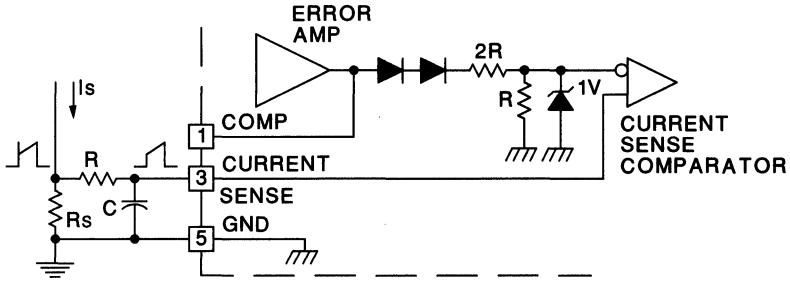


	UC1842 UC1844	UC1843 UC1845
VON	16V	8.4V
VOFF	10V	7.6V



During under-voltage lock-out, the output driver is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

CURRENT SENSE CIRCUIT

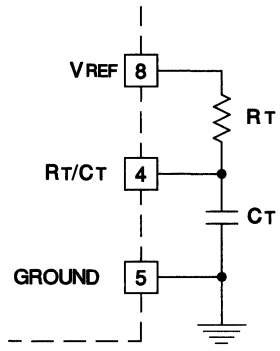


Peak Current (Is) is Determined By The Formula

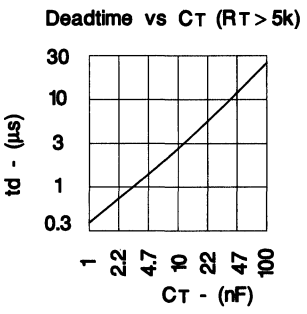
$$I_{SMAX} \approx \frac{1.0V}{R_S}$$

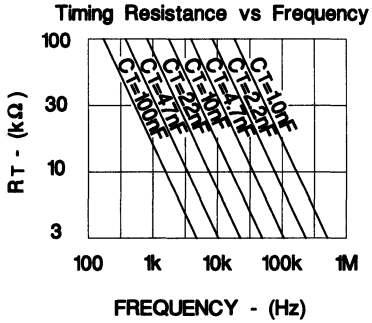
A small RC filter may be required to suppress switch transients.

OSCILLATOR SECTION

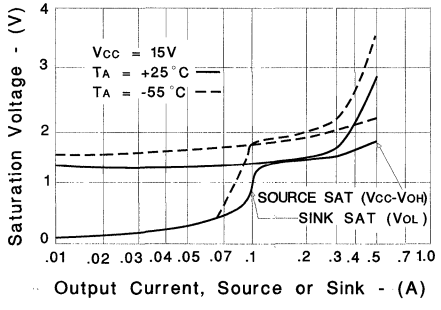


For $R_T > 5k$ $f \sim \frac{1.72}{R_T C_T}$

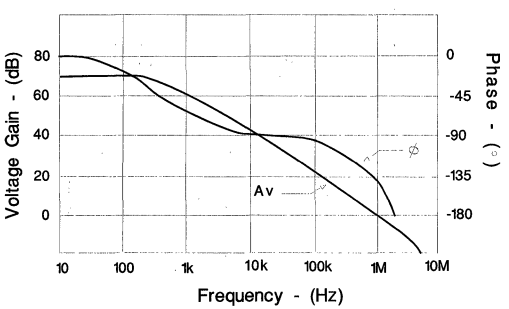




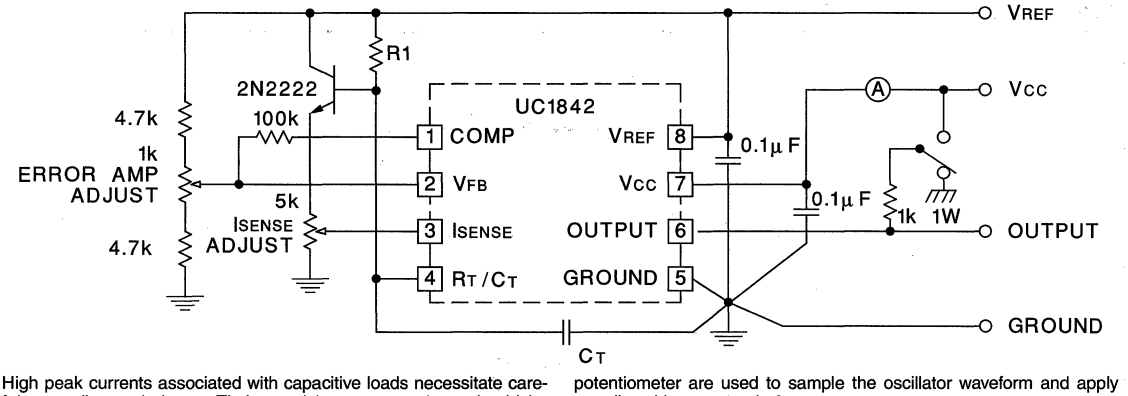
OUTPUT SATURATION CHARACTERISTICS



ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE

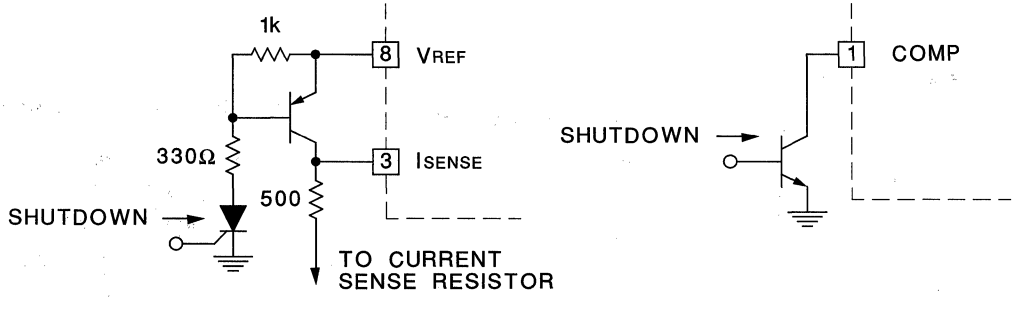


OPEN-LOOP LABORATORY FIXTURE



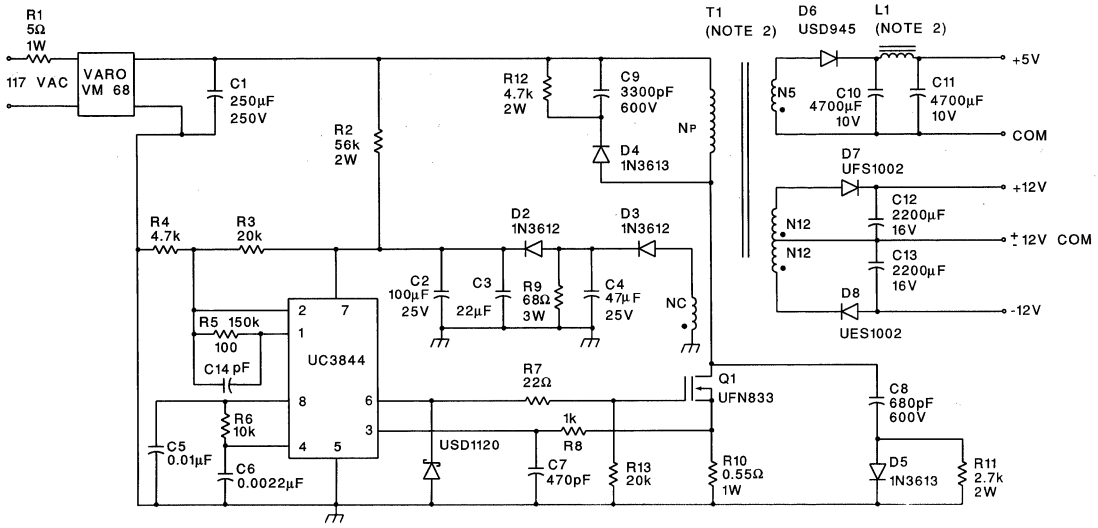
High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

SHUT DOWN TECHNIQUES



Shutdown of the UC1842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling Vcc below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

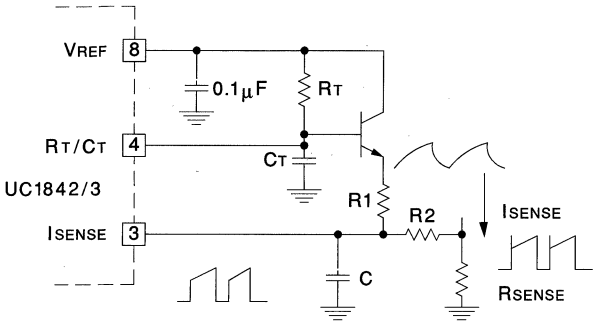
OFFLINE FLYBACK REGULATOR



Power Supply Specifications

1. Input Voltage95VAC to 130VA (50 Hz/60Hz)
2. Line Isolation3750V
3. Switching Frequency40kHz
4. Efficiency @ Full Load70%
5. Output Voltage:
   A. +5V, ±5%; 1A to 4A load
   Ripple voltage: 50mV P-P Max

SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.

Note that capacitor, C forms a filter with R2 to suppress the leading edge switch spikes.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

application INFO available

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low RO Error Amp

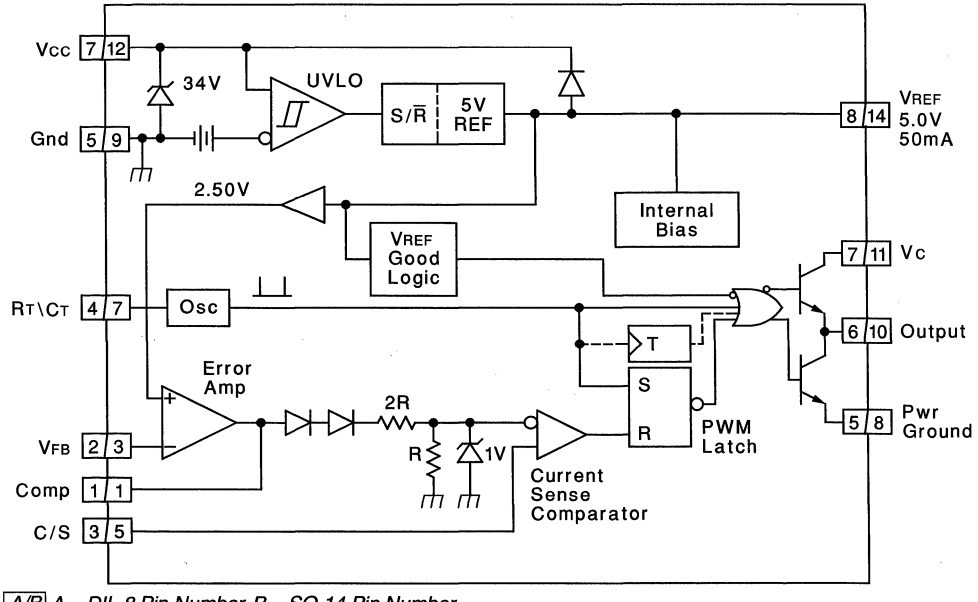
DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for VCC over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM



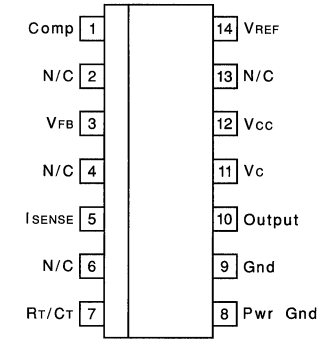
Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (ICC mA) ..... Self Limiting
Output Current ..... ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) ..... -0.3V to +6.3V
Error Amp Output Sink Current 10mA
Power Dissipation at TA ≤ 25°C (DIL-8) 1W
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

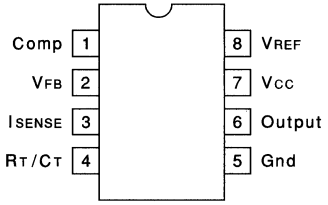
Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only.

SOIC-14 (TOP VIEW)
D Package

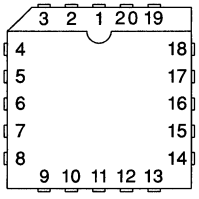


CONNECTION DIAGRAMS

DIL-8, SOIC-8 (TOP VIEW)
J or N, D8 Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
VFB	5
N/C	6
ISENSE	7
N/C	8-9
RT/CT	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
VC	17
VCC	18
N/C	19
VREF	20

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; VCC = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	TJ = 25°C, IO = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ VIN ≤ 25V		6	20		6	20	mV
Load Regulation	1 ≤ IO ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz TJ = 25°C (Note 2)		50			50		µV
Long Term Stability	TA = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	TJ = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ VCC ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	TMIN ≤ TA ≤ TMAX (Note 2)		5			5		%
Amplitude	VPIN 4 peak to peak (Note 2)		1.7			1.7		V
Discharge Current	TJ = 25°C, VPIN 4 = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, these specifications apply for -55°C ≤ TA ≤ 125°C for the UC184xA; -40°C ≤ TA ≤ 85°C for the UC284xA; 0 ≤ TA ≤ 70°C for the UC384xA; VCC = 15V (Note 5); RT = 10k; CT = 3.3nF; TA = TJ; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
	VPIN 4 = 2V (Note 8)	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	VPIN 1 = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
AVOL	2 ≤ VO ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	TJ = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ VCC ≤ 25V	60	70		60	70		dB
Output Sink Current	VPIN 2 = 2.7V, VPIN 1 = 1.1V	2	6		2	6		mA
Output Source Current	VPIN 2 = 2.3V, VPIN 1 = 5V	-0.5	-0.8		-0.5	-0.8		mA
VOUT High	VPIN 2 = 2.3V, RL = 15k to ground	5	6		5	6		V
VOUT Low	VPIN 2 = 2.7V, RL = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	VPIN 1 = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ VCC ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	VPIN 3 = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	ISINK = 20mA		0.1	0.4		0.1	0.4	V
	ISINK = 200mA		15	2.2		15	2.2	V
Output High Level	ISOURCE = 20mA	13	13.5		13	13.5		V
	ISOURCE = 200mA	12	13.5		12	13.5		V
Rise Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
Fall Time	TJ = 25°C, CL = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	VCC = 5V, ISINK = 10mA		0.7	1.2		0.7	1.2	V
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
Turn On	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA

Note 2: These parameters, although guaranteed, are not 100% tested in production.

Note 3: Parameter measured at trip point of latch with VPIN2 = 0.

Note 4: Gain defined as: $A = \frac{\Delta V_{PIN\,1}}{\Delta V_{PIN\,3}}$; $0 \le V_{PIN\,3} \le 0.8V$.

Note 5: Adjust VCC above the start threshold before setting at 15V.

Note 6: Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.

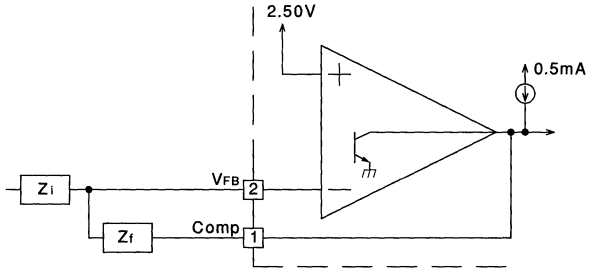
Note 7: "Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF}(max) - V_{REF}(min)}{T_J(max) - T_J(min)}.$$

VREF (max) and VREF (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."

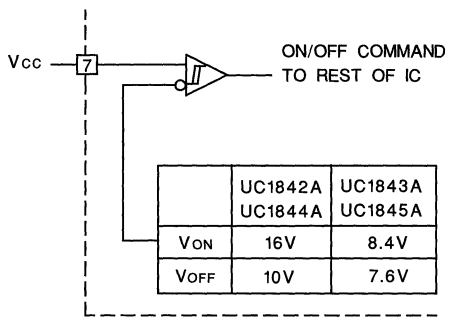
Note 8: This parameter is measured with RT = 10kΩ to VREF. This contributes approximately 300µA of current to the measurement. The total current flowing into the RT/CT pin will be approximately 300µA higher than the measured value.

Error Amp Configuration

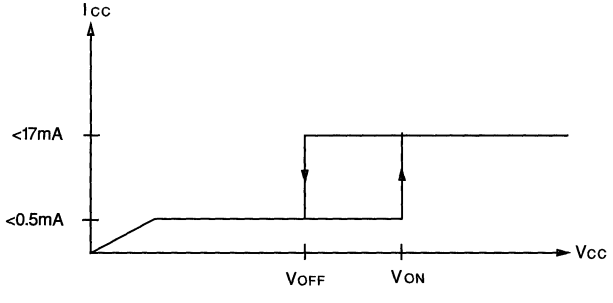


Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

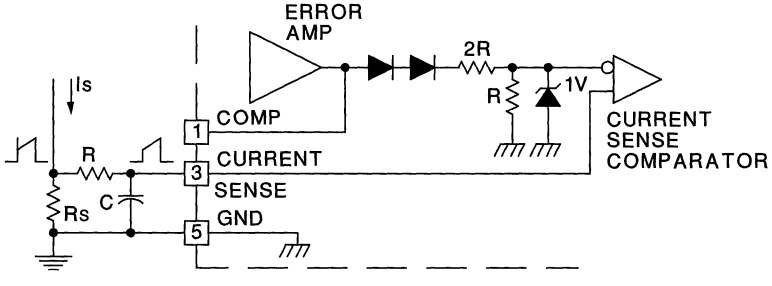


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

Current Sense Circuit



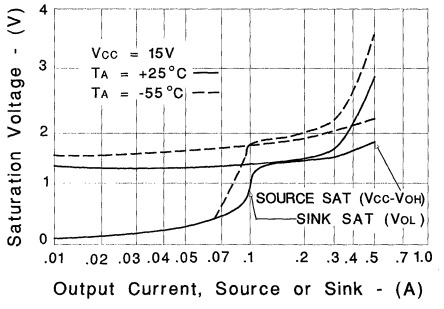
Peak Current (Is) is Determined By The Formula

$$I_{SMAX} \approx \frac{1.0V}{R_S}$$

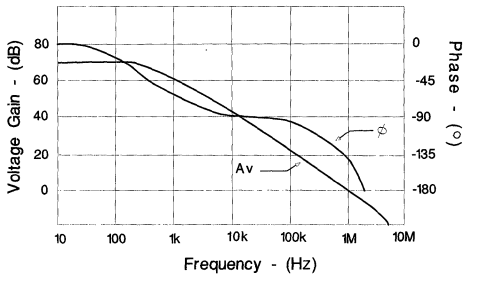
A small RC filter may be required to suppress switch transients.

APPLICATIONS DATA (cont.)

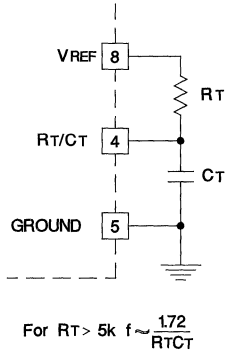
Output Saturation Characteristics



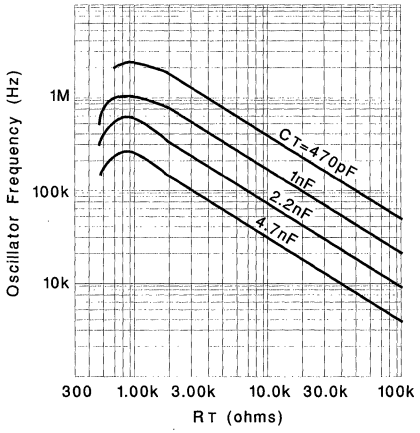
Error Amplifier Open-Loop Frequency Response



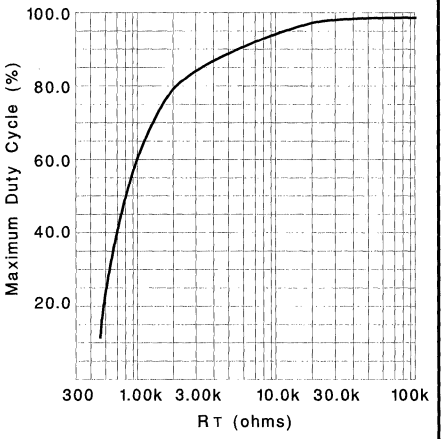
Oscillator Section



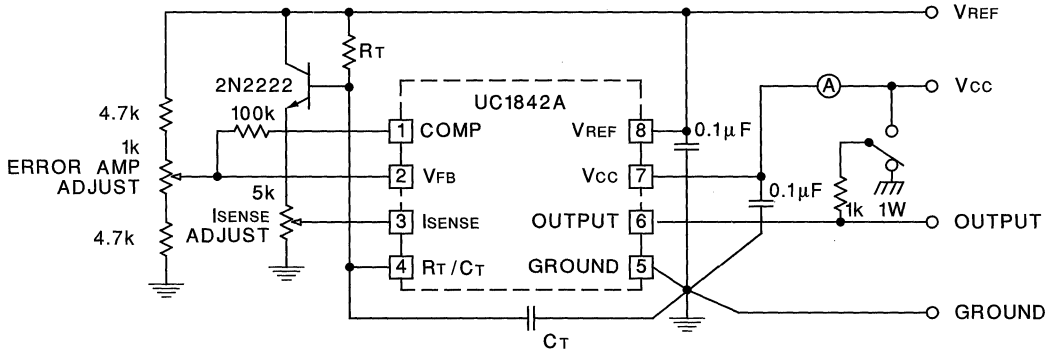
Oscillator Frequency vs Timing Resistor



Maximum Duty Cycle vs Timing Resistor



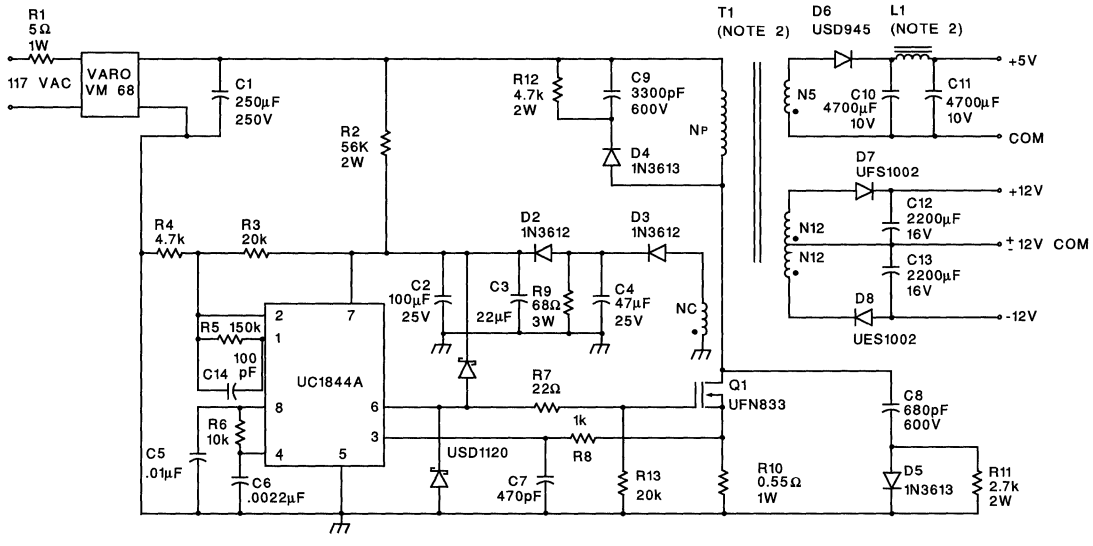
Open-Loop Laboratory Test Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

APPLICATIONS DATA (cont.)

Off-line Flyback Regulator

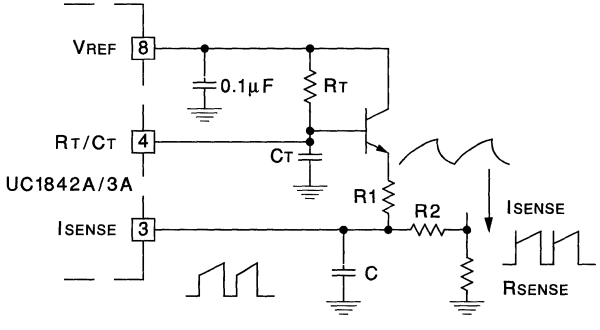


Power Supply Specifications

1. Input Voltage	*95VAC to 130VA (50 Hz/60Hz)*
2. Line Isolation	*3750V*
3. Switching Frequency	*40kHz*
4. Efficiency @ Full Load	*70%*

5. Output Voltage:
A. +5V, ±5%; 1A to 4A load
Ripple voltage: 50mV P-P Max
B. +12V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
C. -12V ,±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max

Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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UNITRODE

application INFO available

UC1846/7
UC2846/7
UC3846/7

Current Mode PWM Controller

FEATURES

- Automatic Feed Forward Compensation
- Programmable Pulse-by-Pulse Current Limiting
- Automatic Symmetry Correction in Push-pull Configuration
- Enhanced Load Response Characteristics
- Parallel Operation Capability for Modular Power Systems
- Differential Current Sense Amplifier with Wide Common Mode Range
- Double Pulse Suppression
- 500mA (Peak) Totem-pole Outputs
- ±1% Bandgap Reference
- Under-voltage Lockout
- Soft Start Capability
- Shutdown Terminal
- 500kHZ Operation

DESCRIPTION

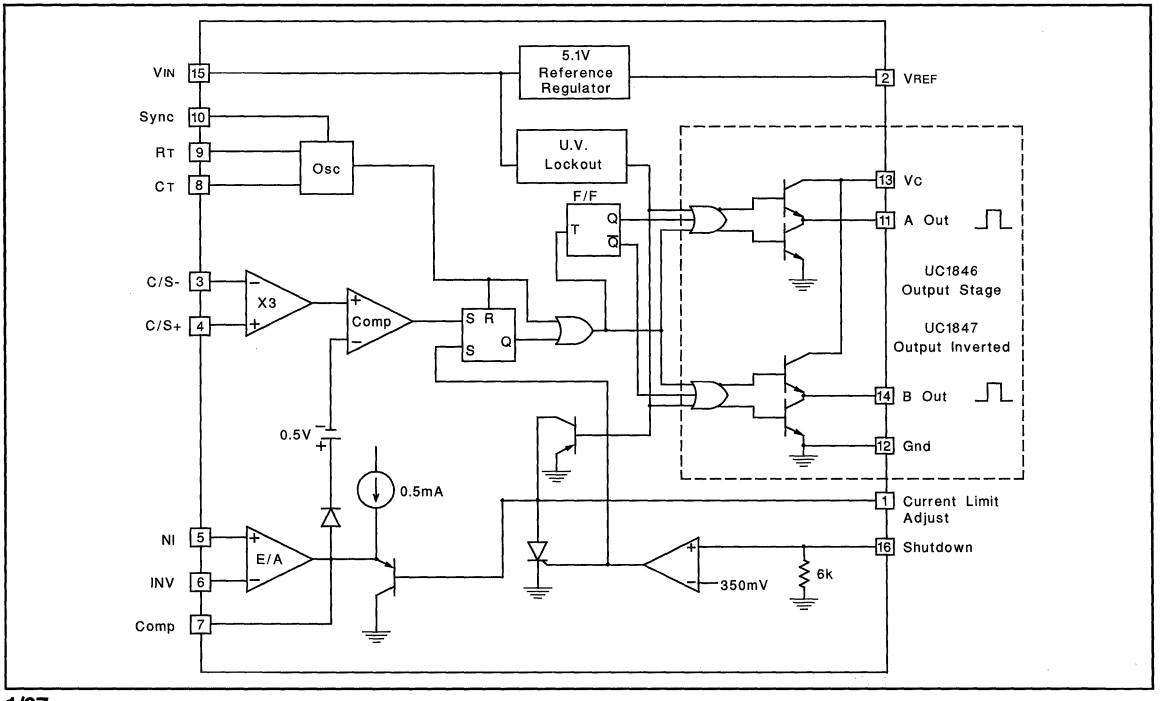
The UC1846/7 family of control ICs provides all of the necessary features to implement fixed frequency, current mode control schemes while maintaining a minimum external parts count. The superior performance of this technique can be measured in improved line regulation, enhanced load response characteristics, and a simpler, easier-to-design control loop. Topological advantages include inherent pulse-by-pulse current limiting capability, automatic symmetry correction for push-pull converters, and the ability to parallel "power modules" while maintaining equal current sharing.

Protection circuitry includes built-in under-voltage lockout and programmable current limit in addition to soft start capability. A shutdown function is also available which can initiate either a complete shutdown with automatic restart or latch the supply off.

Other features include fully latched operation, double pulse suppression, deadline adjust capability, and a ±1% trimmed bandgap reference.

The UC1846 features low outputs in the OFF state, while the UC1847 features high outputs in the OFF state.

BLOCK DIAGRAM



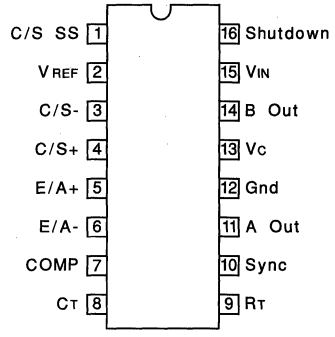
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pin 15) . . . . . +40V
Collector Supply Voltage (Pin 13) . . . . . +40V
Output Current, Source or Sink (Pins 11, 14) 500mA
Analog Inputs (Pins 3, 4, 5, 6, 16) . . . . . -0.3V to +V_{IN}
Reference Output Current (Pin 2) . . . . . -30mA
Sync Output Current (Pin 10) . . . . . -5mA
Error Amplifier Output Current (Pin 7) . . . . . -5mA
Soft Start Sink Current (Pin 1) 50mA
Oscillator Charging Current (Pin 9) 5mA
Power Dissipation at T_A=25°C 1000mW
Power Dissipation at T_C=25°C 2000mW
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

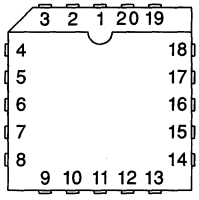
Note 1. All voltages are with respect to Ground, Pin 13. Currents are positive into, negative out of the speficied terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL and SOIC packages only.

CONNECTION DIAGRAMS

DIL-16, SOIC-16
(TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
C/L SS	2
V_{REF}	3
C/S-	4
C/S+	5
N/C	6
E/A+	7
E/A-	8
Comp	9
C_T	10
N/C	11
R_T	12
Sync	13
A Out	14
Gnd	15
N/C	16
Vc	17
B Out	18
V_{IN}	19
Shutdown	20

ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J=25°C, I_O=1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	V_{IN}=8V to 40V		5	20		5	20	mV
Load Regulation	I_L=1mA to 10mA		3	15		3	15	mV
Temperature Stability	Over Operating Range, (Note 2)		0.4			0.4		mV/°C
Total Output Variation	Line, Load, and Temperature (Note 2)	5.00		5.20	4.95		5.25	V
Output Noise Voltage	10Hz ≤ f ≤10kHz, T_J=25°C (Note 2)		100			100		µV
Long Term Stability	T_J=125°C, 1000 Hrs. (Note 2)		5			5		mV
Short Circuit Output Current	V_{REF}=0V	-10	-45		-10	-45		mA

ELECTRICAL CHARACTERISTICS (cont.) (Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Oscillator Section								
Initial Accuracy	T_J=25°C	39	43	47	39	43	47	kHz
Voltage Stability	V_{IN}=8V to 40V		-1	2		-1	2	%
Temperature Stability	Over Operating Range (Note 2)		-1			-1		%
Sync Output High Level		3.9	4.35		3.9	4.35		V
Sync Output Low Level			2.3	2.5		2.3	2.5	V
Sync Input High Level	Pin 8=0V	3.9			3.9			V
Sync Input Low Level	Pin 8=0V			2.5			2.5	V
Sync Input Current	Sync Voltage=3.9V, Pin 8=0V		1.3	1.5		1.3	1.5	mA
Error Amp Section								
Input Offset Voltage			0.5	5		0.5	10	mV
Input Bias Current			-0.6	-1		-0.6	-2	µA
Input Offset Current			40	250		40	250	nA
Common Mode Range	V_{IN}=8V to 40V	0		V_{IN}-2V	0		V_{IN}-2V	V
Open Loop Voltage Gain	ΔV_O=1.2 to 3V, V_{CM}=2V	80	105		80	105		dB
Unity Gain Bandwidth	T_J=25°C (Note 2)	0.7	1.0		0.7	1.0		MHz
CMRR	V_{CM}=0V to 38V, V_{IN}=40V	75	100		75	100		dB
PSRR	V_{IN}=8V to 40V	80	105		80	105		dB
Output Sink Current	V_{ID}=-15mV to -5V, $V_{PIN\ 7}$=1.2V	2	6		2	6		mA
Output Source Current	V_{ID}=15mV to 5V, $V_{PIN\ 7}$=2.5V	-0.4	-0.5		-0.4	-0.5		mA
High Level Output Voltage	R_L=(Pin 7) 15kΩ	4.3	4.6		4.3	4.6		V
Low Level Output Voltage			0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	$V_{PIN\ 3}$=0V, Pin 1 Open (Notes 3 & 4)	2.5	2.75	3.0	2.5	2.75	3.0	V
Maximum Differential Input Signal ($V_{PIN\ 4}$-$V_{PIN\ 3}$)	Pin 1 Open (Note 3) R_L (Pin 7)=15kW	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		5	25		5	25	mV
CMRR	V_{CM}=1V to 12V	60	83		60	83		dB
PSRR	V_{IN}=8V to 40V	60	84		60	84		dB
Input Bias Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		-2.5	-10		-2.5	-10	µA
Input Offset Current	$V_{PIN\ 1}$=0.5V, Pin 7 Open (Note 3)		0.08	1		0.08	1	µA
Input Common Mode Range		0		V_{IN}-3	0		V_{IN}-3	V
Delay to Outputs	T_J=25°C, (Note 2)		200	500		200	500	ns
Current Limit Adjust Section								
Current Limit Offset	$V_{PIN\ 3}$=0V, $V_{PIN\ 4}$=0V, Pin 7 Open (Note 3)	0.45	0.5	0.55	0.45	0.5	0.55	V
Input Bias Current	$V_{PIN\ 5}$=V_{REF}, $V_{PIN\ 6}$=0V		-10	-30		-10	-30	µA
Shutdown Terminal Section								
Threshold Voltage		250	350	400	250	350	400	mV
Input Voltage Range		0		V_{IN}	0		V_{IN}	V
Minimum Latching Current ($I_{PIN\ 1}$)	(Note 6)	3.0	1.5		3.0	1.5		mA

ELECTRICAL CHARACTERISTICS (cont.)

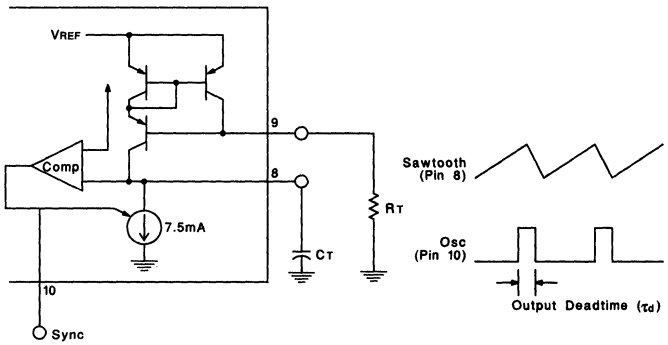
(Unless otherwise stated, these specifications apply for T_A=-55°C to +125°C for UC1846/7; -40°C to +85°C for the UC2846/7; and 0°C to +70°C for the UC3846/7; V_{IN}=15V, R_T=10k, C_T=4.7nF, T_A=T_J.)

PARAMETER	TEST CONDITIONS	UC1846/UC1847 UC2846/UC2847			UC3846/UC3847			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Shutdown Terminal Section (cont.)								
Maximum Non-Latching Current ($I_{PIN\ 1}$)	(Note 7)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	T_J=25°C (Note 2)		300	600		300	600	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	V_C=40V (Note 5)			200			200	µA
Output Low Level	I_{SINK}=20mA		0.1	0.4		0.1	0.4	V
	I_{SINK}=100mA		0.4	2.1		0.4	2.1	V
Output High Level	I_{SOURCE}=20mA	13	13.5		13	13.5		V
	I_{SOURCE}=100mA	12	13.5		12	13.5		V
Rise Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Fall Time	C_L=1nF, T_J=25°C (Note 2)		50	300		50	300	ns
Under-Voltage Lockout Section								
Start-Up Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysteresis			0.75			0.75		V
Total Standby Current								
Supply Current			17	21		17	21	mA

Note 2. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with VPIN 5 = VREF, VPIN 6 = 0V.
Note 4. Amplifier gain defined as: $G = \frac{\Delta V_{PIN7}}{\Delta V_{PIN4}}$; ΔV_{PIN4} = 0 to 1.0V
Note 5. Applies to UC1846/UC2846/UC3846 only due to polarity of outputs.
Note 6. Current into Pin 1 guaranteed to latch circuit in shutdown state.
Note 7. Current into Pin 1 guaranteed not to latch circuit in shutdown state.

APPLICATIONS DATA

Oscillator Circuit



Output deadtime is determined by the external capacitor, C_T, according to the formula: $\tau d\ (\mu s) = 145 CT\ (\mu f) \left(\frac{ID}{ID - \frac{3.6}{RT\ (k\Omega)}} \right)$.

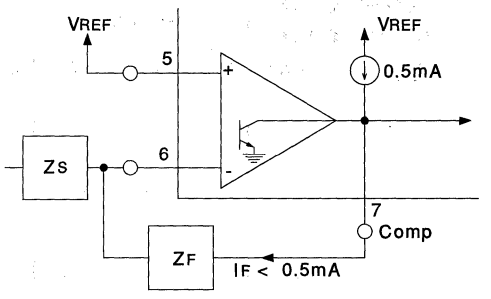
I_D = Oscillator discharge current at 25°C is typically 7.5.

For large values of R_T: $\tau d\ (\mu s) \approx 145 CT\ (\mu f)$.

Oscillator frequency is approximated by the formula: $fT\ (kHz) \approx \frac{2.2}{RT\ (k\Omega) \bullet CT\ (\mu f)}$.

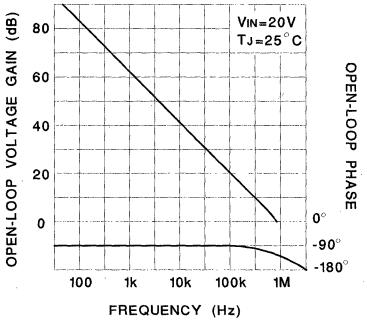
APPLICATIONS DATA (cont.)

Error Amp Output Configuration

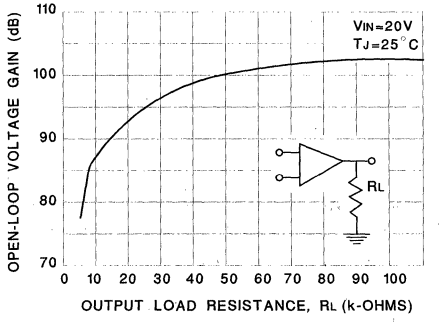


Error Amplifier can source up to 0.5mA.

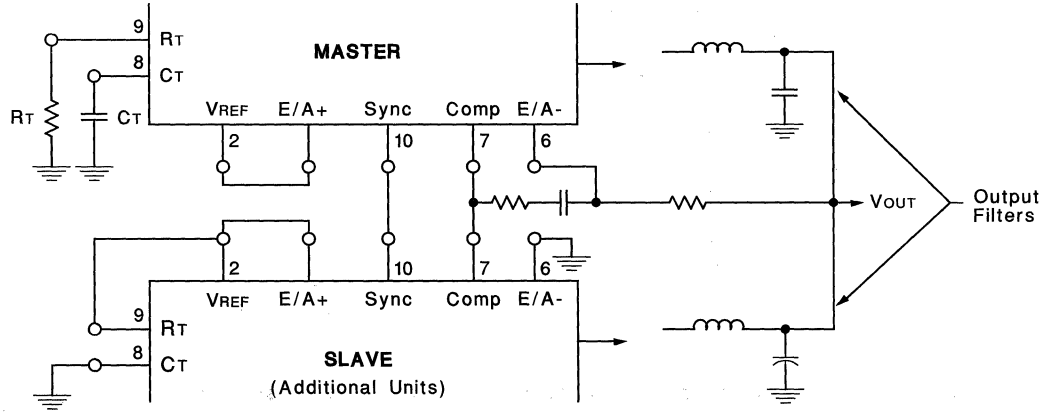
Error Amp Gain and Phase vs Frequency



Error Amp Open-Logic D.C. Gain vs Load Resistance



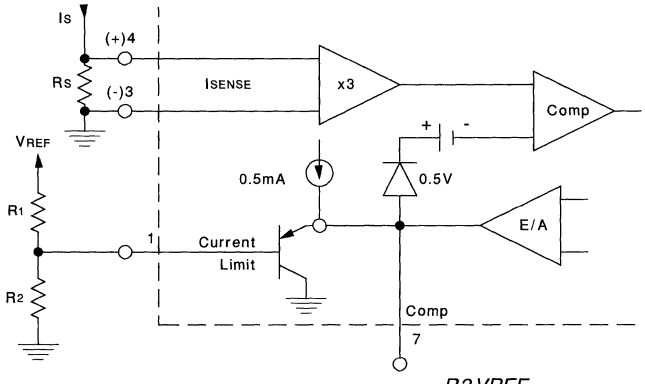
Parallel Operation



Slaving allows parallel operation of two or more units with equal current sharing.

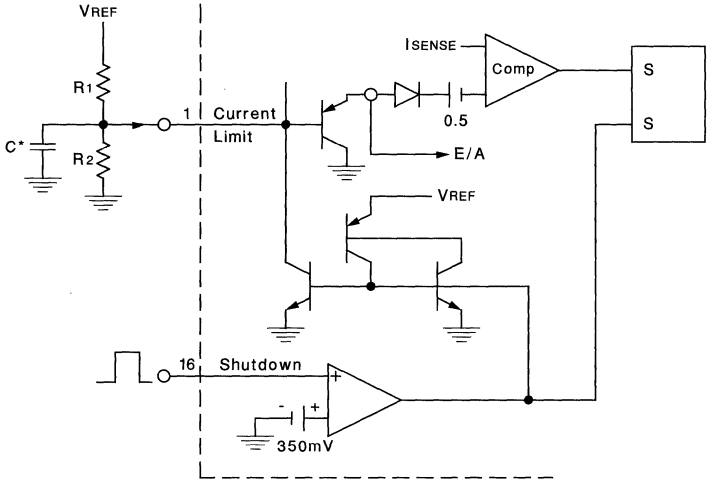
APPLICATIONS DATA (cont.)

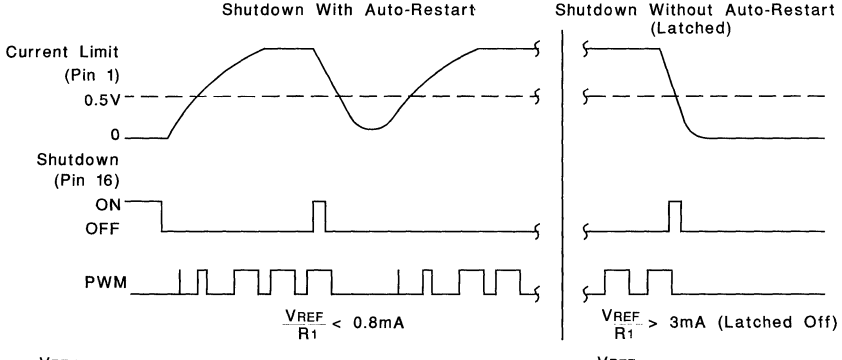
Pulse by Pulse Current Limiting



Peak Current (Is) is determined by the formula: $IS = \dfrac{\dfrac{R2\,VREF}{R1+R2} - 0.5}{3RS}$

Soft Start and Shutdown /Restart Functions



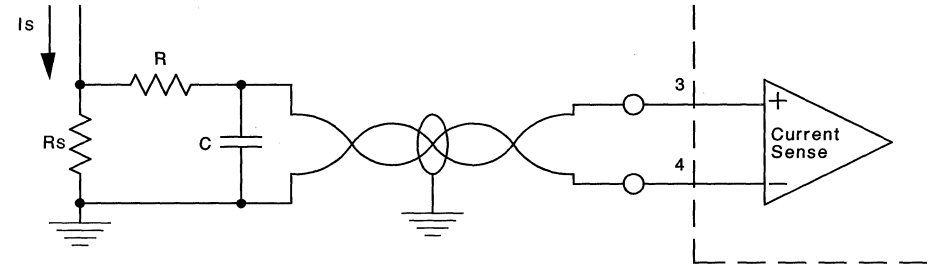


If $\frac{VREF}{R1}$ < 0.8mA, the shutdown latch will commutate when Iss = 0.8mA and a restart cycle will be initiated.

If $\frac{VREF}{R1}$ > 3mA, the device will latch off until power is recycled.

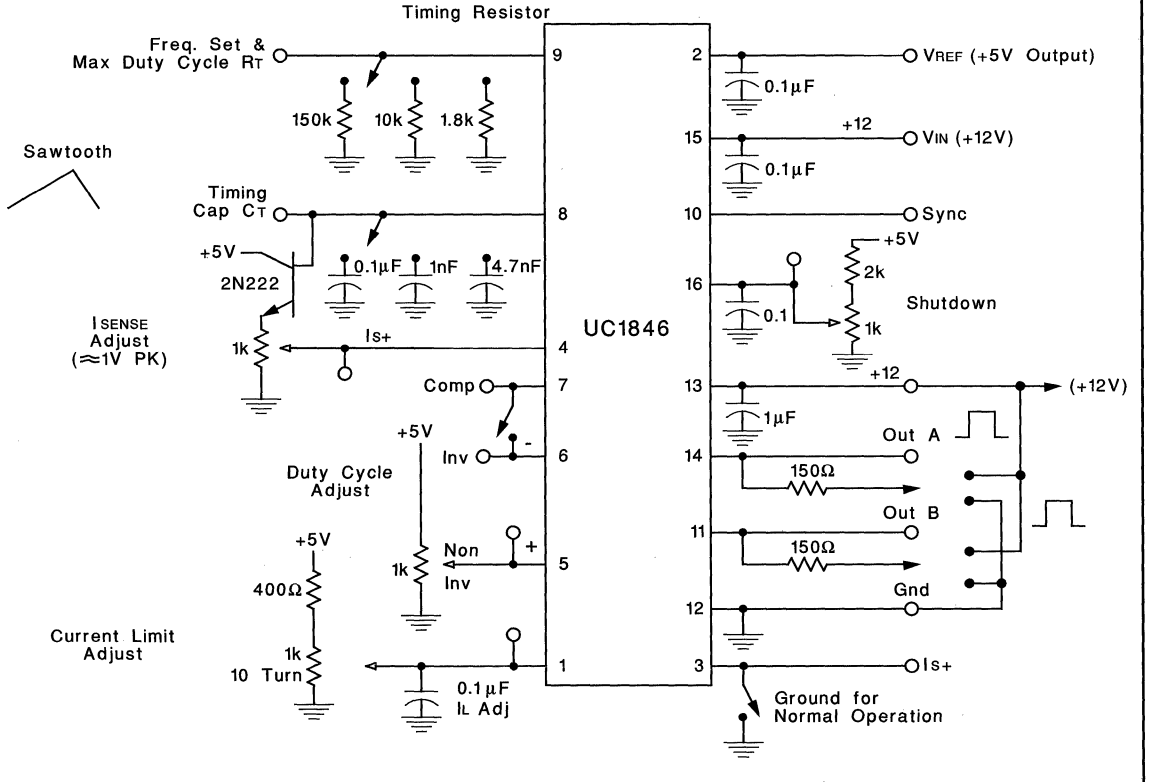
APPLICATIONS DATA (cont.)

Current Sense Amp Connection



A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise free sensing.

UC1846 Open Loop Test Circuit



-Bypass Caps Should Be Low ESR & ESL Type
-Short Pins 6 & 7 for Unity Gain Testing

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UNITRODE

application INFO available

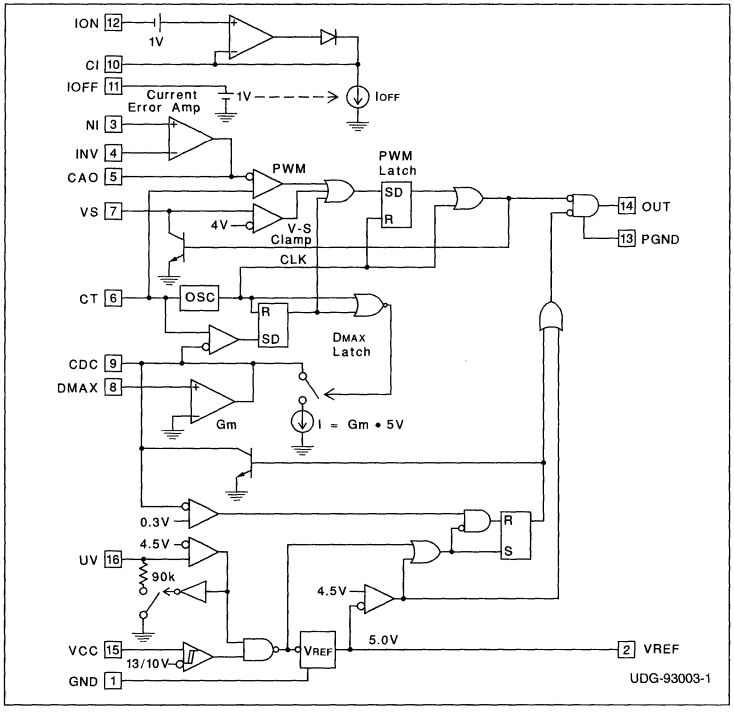
UC1848
UC2848
UC3848

Average Current Mode PWM Controller

FEATURES

- Practical Primary Side Control of Isolated Power Supplies with DC Control of Secondary Side Current
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Under Voltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Startup Current (500µA)
- Precision 5V Reference (1%)

BLOCK DIAGRAM



DESCRIPTION

The UC3848 family of PWM control ICs makes primary side average current mode control practical for isolated switching converters. Average current mode control insures that both cycle by cycle peak switch current and maximum average inductor current are well defined and will not run away in a short circuit situation. The UC3848 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC3848 implements a patented technique of sensing secondary current in an isolated buck derived converter from the primary side. A current waveform synthesizer monitors switch current and simulates the inductor current down slope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side allows for full DC control of output current.

The UC3848 circuitry includes a precision reference, a wide bandwidth error amplifier for average current control, an oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current output driver. The current error amplifier easily interfaces with an optoisolator from a secondary side voltage sensing circuit.

A full featured undervoltage lockout (UVLO) circuit is contained in the UC3848. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500µA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

Patents embodied in the UC3848 belong to Lambda Electronics Incorporated and are licensed for use in applications employing these devices.

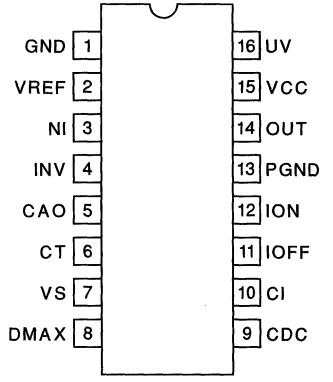
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15) 22V
Output Current, Source or Sink (Pin 14)
DC 0.5A
Pulse (0.5µs) 2.2A
Power Ground to Ground (Pin 1 to Pin 13) . . . . . ±0.2V
Analog Input Voltages
(Pins 3, 4, 7, 8, 12, 16) . . . . . –0.3 to 7V
Analog Input Currents, Source or Sink
(Pins 3, 4, 7, 8, 11, 12, 16) 1mA
Analog Output Currents, Source or Sink (Pins 5 & 10) . . . 5mA
Power Dissipation at TA = 60°C 1W
Storage Temperature Range . . . . . -65°C to +150° C
Lead Temperature (Soldering 10 seconds) . . . . . +300° C

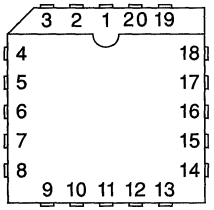
Notes: All voltages are with respect to ground (DIL and SOIC Pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N, or DW Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
GND	2
VREF	3
NI	4
INV	5
N/C	6
CAO	7
CT	8
VS	9
DMAX	10
N/C	11
CDC	12
CI	13
IOFF	14
ION	15
N/C	16
PGND	17
OUT	18
VCC	19
UV	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications are over the junction temperature range of -55° C to +125° C for the UC1848, -40° C to +85° C for the UC2848, and 0° C to +70° C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/µs
Iib			-2	-20	µA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
AVOL		60	100		dB
Vio	12V ≤VCC ≤20V, 0V ≤VCM ≤5V			10	mV
Iib			-0.5	-3	µA
Voh	Io = -200µA	3	3.3		V
Vol	Io = 200µA		0.3	0.6	V
Source Current	Vo = 1V	1.4	1.6	2.0	mA
GBW Product	f = 200kHz	5	8		MHz
Slew Rate (Note 1)		8	10		V/µs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications are over the junction temperature range of -55° C to +125° C for the UC1848, -40° C to +85° C for the UC2848, and 0° C to +70° C for the UC3848. Test conditions are: VCC = 12V, CT = 400pF, CI = 100pF, IOFF = 100µA, CDC = 100nF, Cvs = 100pF, and Ivs = 400µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency	T_A = 25°C	240	250	260	kHz
		235		265	kHz
Ramp Amplitude		1.5	1.65	1.8	V
Duty Cycle Clamp					
Max Duty Cycle	V(DMAX) = 0.75 • VREF	73.5	76.5	79.5	%
Volt Second Clamp					
Max On Time		900		1100	ns
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
RHYSTERESIS	Vuv = 4.2V	77	90	103	kΩ
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
	0 < Io < 10mA, 12 < VCC < 20	4.93		5.07	V
Line Regulation	12 < Vcc < 20V		4	15	mV
Load Regulation	0 < Io < 10mA		3	15	mV
Short Circuit Current	VREF = 0V	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	CI = 1nF		20	45	ns
Output Low Saturation	Io = 20mA		0.25	0.4	V
	Io = 200mA		1.2	2.2	V
Output High Saturation	Io = -200mA		2.0	3.0	V
UVLO Output Low Saturation	Io = 20mA		0.8	1.2	V
Icc					
ISTART	VCC = 12V		0.2	0.4	mA
Icc (pre-start)	VCC = 15V, V(UV) = 0		0.5	1	mA
Icc (run)			22	26	mA

Note 1: Guaranteed by design.

APPLICATION INFORMATION

Under Voltage Lockout

The Under Voltage Lockout block diagram is shown in Fig 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, ICC is low (<500µA) and the output is low.

The UV comparator monitors input line voltage (V_{IN}). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

V_{IN}(on) = 4.35V • (1 + Rv1/Rv2′) and

V_{IN}(off) = 4.35V • (1 + Rv1/Rv2) where

Rv2′ = Rv2|| 90k.

The resulting hysteresis is

V_{IN}(hys) = 4.35V • Rv1 / 90k.

When the UV comparator is low, I_{CC} is low (500µA) and the output is low.

APPLICATION INFORMATION (cont.)

When both the UV and VCC comparators are high, the internal bias circuitry for the rest of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

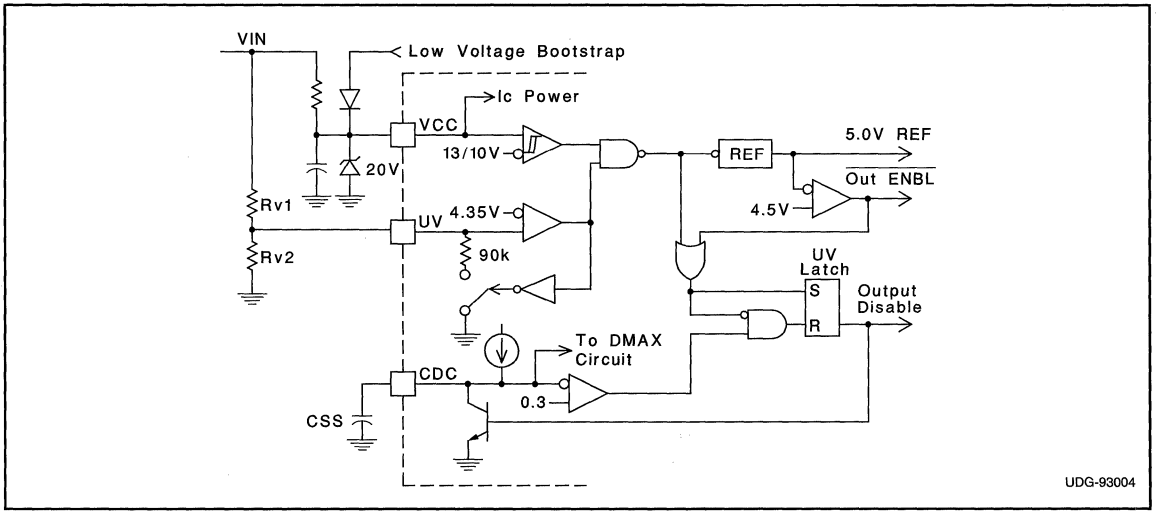


Figure 1: Under voltage lockout.

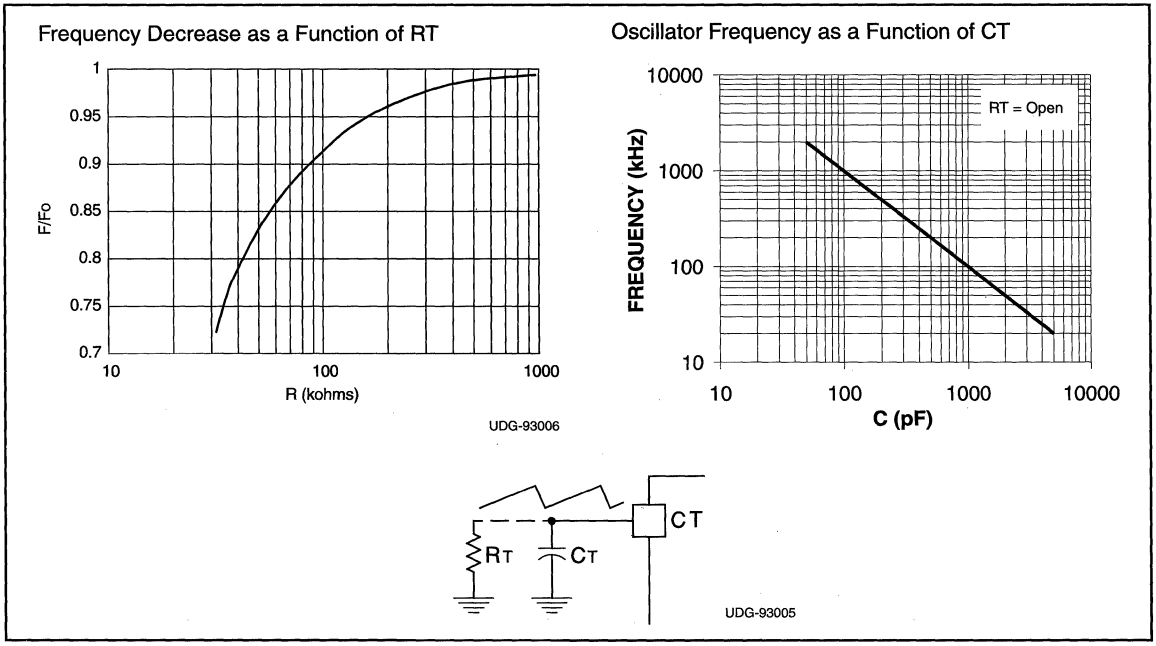


Figure 2: Oscillator frequency.

APPLICATION INFORMATION (cont.)

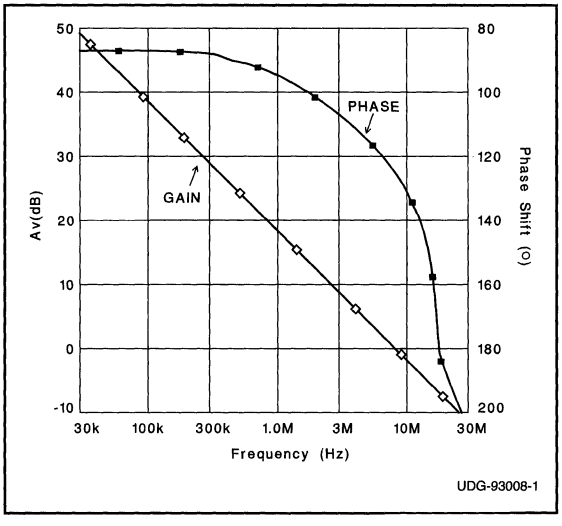


Figure 3: Error amplifier gain and phase response over frequency.

Oscillator

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Fig. 2. Frequency is determined by:

$$F = 1 / (10k \bullet CT).$$

The sawtooth wave shape is generated by a charging current of 200µA and a discharge current of 1800µA. The discharge time of the sawtooth is guaranteed dead time for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor RT from CT to Ground can be used to adjust the oscillator frequency. RT should not be less than 40kΩ. This will allow up to a 22% decrease in frequency.

Inductor Current Waveform Synthesizer

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope $dIL/dt = -V_O/L$. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Fig. 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. The best utilization of the UC3848 is to translate maximum average inductor current to a 4V signal level. Given N and Ns (the turns ratio of the power and current sense transformers), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$Rs = 4V \bullet Ns \bullet N / IL(max).$$

Restated, the maximum average inductor current will be limited to:

$$IL(max) = 4V \bullet Ns \bullet N/Rs.$$

IOFF and CI need to be chosen so that the ratio of dV(CI)/dt to dIL/dt is the same during switch off time as on time. Recommended nominal off current is 100µA. This requires

$$CI = (100\mu A \bullet N \bullet Ns \bullet L) / (Rs \bullet V_O(nom))$$

where L is the output inductor value and V_O(nom) is the converter regulated output voltage.

There are several methods to program IOFF. If accurate average current control is required during short circuit operation, IOFF must track output voltage. The method shown in Fig. 4 derives a voltage proportional to $V_{IN} \bullet D$ (Duty Cycle). (In a buck converter, output voltage is proportional to VIN • D.) A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to VIN and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated V_O. A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI down slope.

APPLICATION INFORMATION (cont.)

If the system is not sensitive to short circuit requirements, Figure 5 shows the simplest method of downslope generation: a single resistor (ROFF = 40k) from IOFF to VREF. The discharge current is then 100µA. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor down slope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating IOFF is to add a second winding to the output inductor core (Fig. 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, ROFF = V_O / 100µA. The 4 • ROFF resistor is added to compensate the one volt input level of the IOFF pin. Without this compensation, a minor current foldback behavior will be observed.

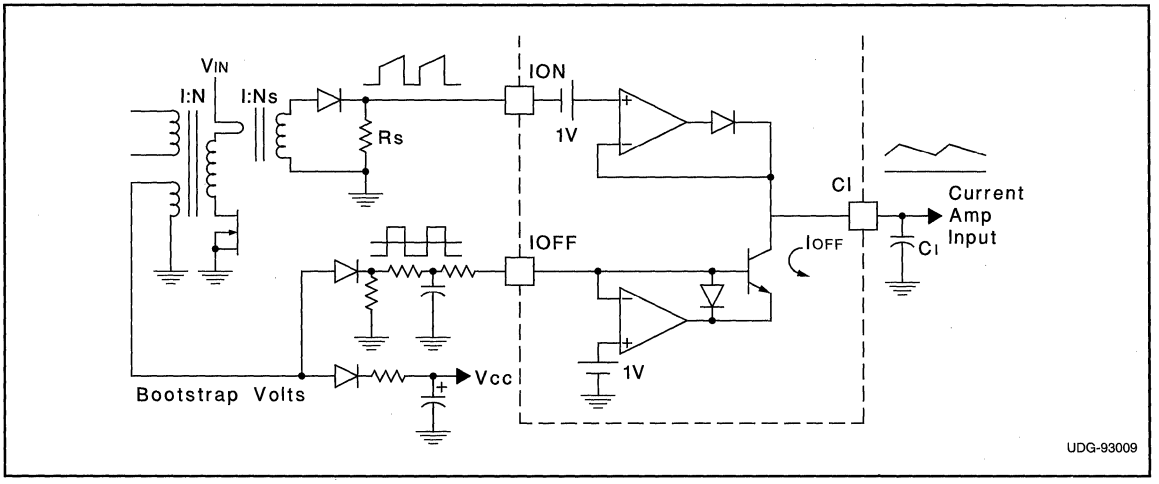


Figure 4: Inductor current waveform synthesizer.

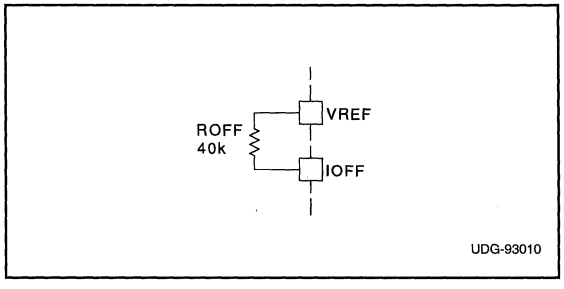


Figure 5: Fixed IOFF.

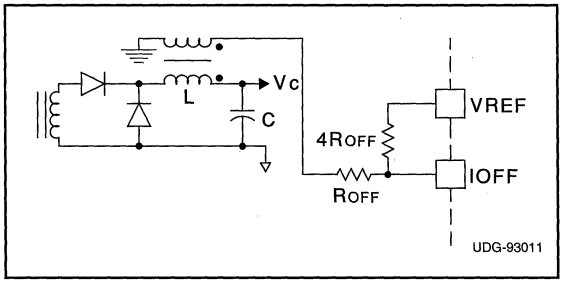


Figure 6: Second inductor winding generation of IOFF.

APPLICATION INFORMATION (cont.)

Maximum Volt-Second Circuit

A maximum volt-second product can be programmed by a resistor (Rvs) from VS to VIN and a capacitor (Cvs) from VS to ground (Figure 7). VS is discharged while the switch is off. When the output turns on, VS is allowed to charge. Since the threshold of the VS comparator is much less than VIN, the charging profile at Vs will be essentially linear. If VS crosses the 4.0V threshold before the PWM turns the output off, the VS comparator will turn the output off for the remainder of the cycle. The maximum volt-second product is

$$V_{IN} \bullet T_{ON}(max) = 4.0V \bullet Rvs \bullet Cvs.$$

Maximum Duty Cycle And Soft Start

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from VREF to DMAX (Fig. 7). The value programmed is:

$$D(max) = Rd1 / (Rd1 + Rd2).$$

For proper operation, the integrating capacitor, C_{DC}, should be larger than $C_{DC}(min) > T(osc) / 80k$, where T(osc) is the oscillator period. C_{DC} also sets the soft start time constant, so values of C_{DC} larger than minimum may be desired. The soft start time constant is approximately:

$$T(ss) = 20k \bullet C_{DC}.$$

Ground Planes

The output driver on the UC3848 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Fig. 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which to PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. VCC should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both VCC and PGND. Nothing else should be connected to power ground.

VREF should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low esr/esl ceramic 1µF capacitors are recommended for both VCC and VREF. The capacitors from CT, CDC, and CI should likewise be connected to the signal ground plane.

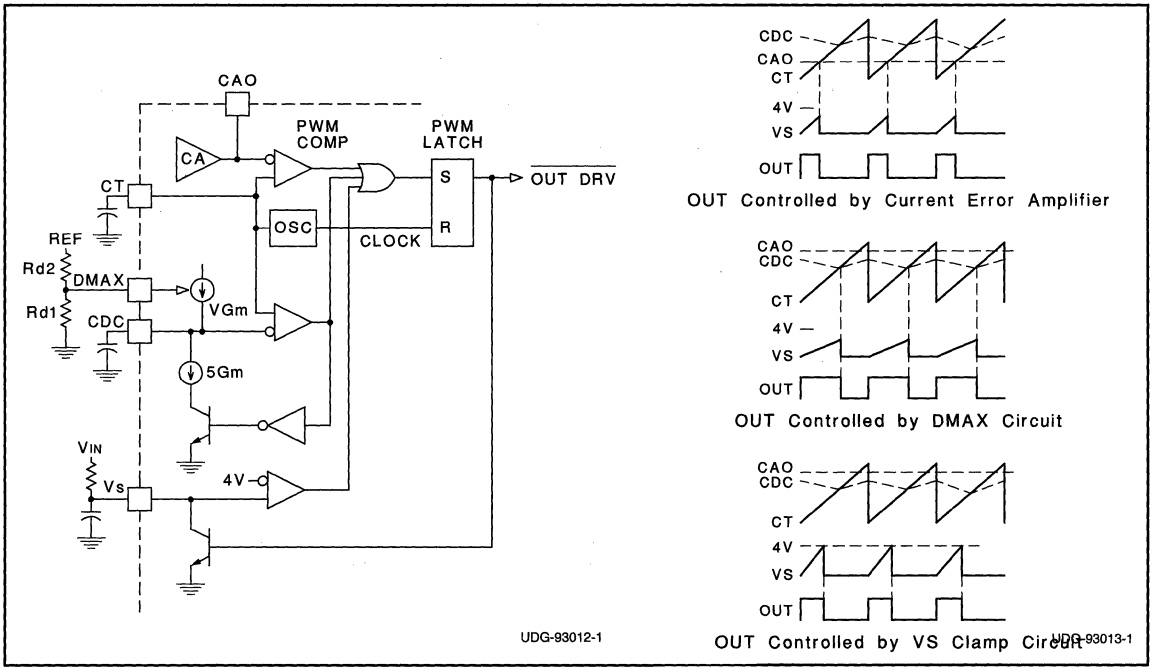


Figure 7: Duty cycle control.

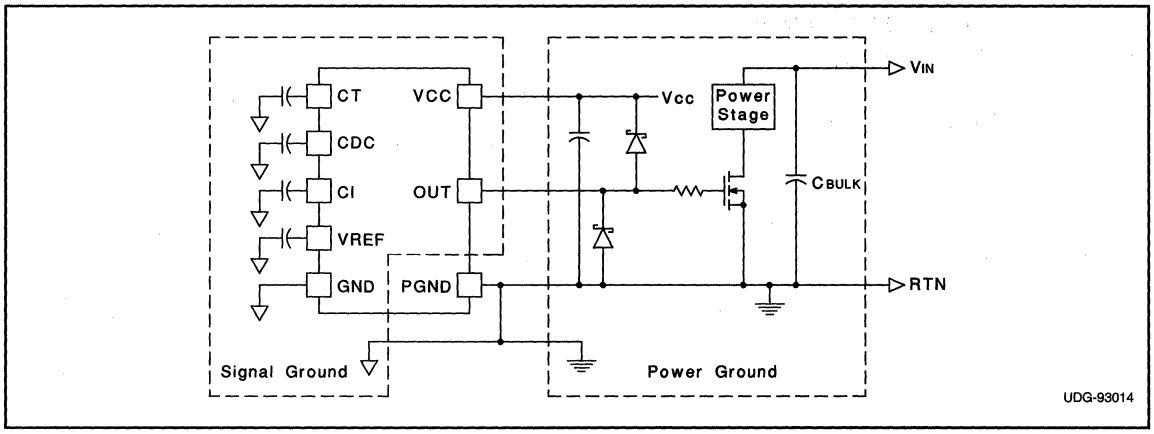


Figure 8: Ground plane considerations.

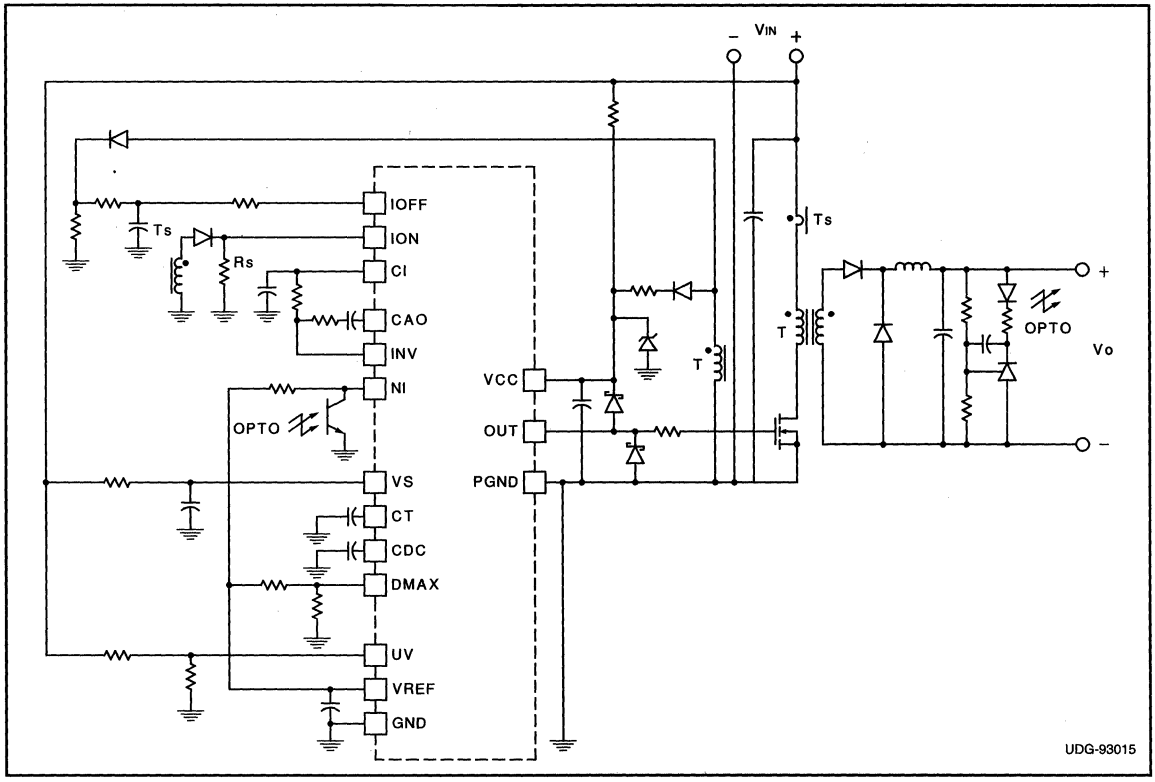


Figure 9: Typical application - an average current-mode isolated forward converter.

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Secondary Side Average Current Mode Controller

FEATURES

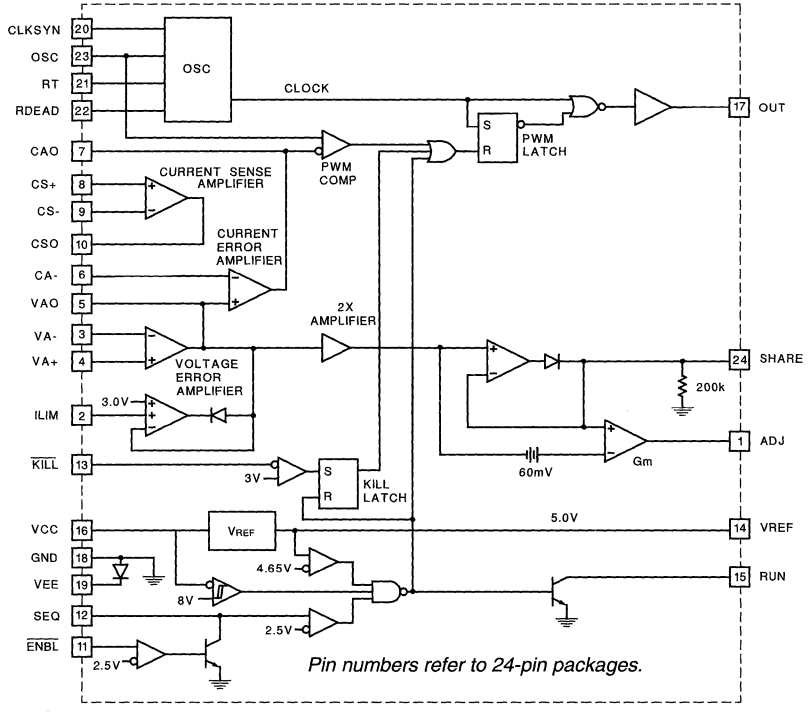
- Practical Secondary Side Control of Isolated Power Supplies
- 1MHz Operation
- Differential AC Switching Current Sensing
- Accurate Programmable Maximum Duty Cycle
- Multiple Chips Can be Synchronized to Fastest Oscillator
- Wide Gain Bandwidth Product (70MHz, Acl>10) Current Error and Current Sense Amplifiers
- Up to Ten Devices Can Easily Share a Common Load

DESCRIPTION

The UC1849 family of average current mode controllers accurately accomplishes secondary side average current mode control. The secondary side output voltage is regulated by sensing the output voltage and differentially sensing the AC switching current. The sensed output voltage drives a voltage error amplifier. The AC switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current sense amplifier. The outputs of the voltage error amplifier and current sense amplifier differentially drive a high bandwidth, integrating current error amplifier. The sawtooth waveform at the current error amplifier output is the amplified and inverted inductor current sensed through the resistor. This inductor current down-slope compared to the PWM ramp achieves slope compensation, which gives an accurate and inherent fast transient response to changes in load.

The UC1849 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC1849 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. The UC1849 is an ideal controller to achieve high power, secondary side average current mode control.

BLOCK DIAGRAM



UDG-94110

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 20V
Output Current Source or Sink 0.3A
Analog Input Voltages . . . . . –0.3V to 7V
ILIM, KILL, SEQ, ENBL, RUN . . . . . –0.3V to 7 V
CLKSYN Current Source 12mA
RUN Current Sink 15mA
SEQ Current Sink 20mA
RDEAD Current Sink 20mA
Share Bus Voltage (voltage with respect to GND) . . 0V to 6.2V
ADJ Voltage (voltage with respect to GND) . . . . . 0.9V to 6.3V
VEE (voltage with respect to GND) . . . . . –1.5V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

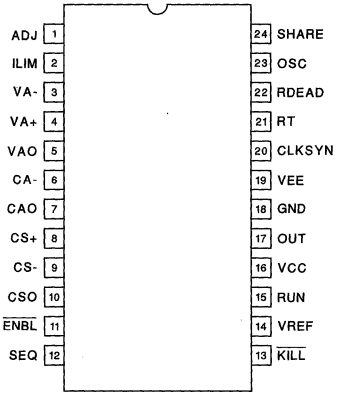
All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

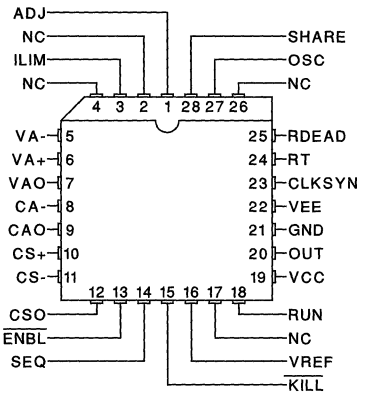
Input Voltage . . . . . 8V to 20V
Sink/Source Output Current 250mA
Timing Resistor (RT) . . . . . 1k to 200k
Timing Capacitor (CT) . . . . . 75pF to 2nF

CONNECTION DIAGRAMS

DIL-24, SOIC-24, TSSOP-24 (Top View)
J or N, DW, PW Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Ib			0.5	3	µA
Vio	T_A = +25°C			3	mV
	Over Temperature			5	mV
Avo		60	90		dB
GBW (Note 2)	Acl = 1, R_{IN} = 1k, CC = 15pF, f = 200kHz (Note 1)	4.5	7		MHz
Vol	I_O = 1mA, Voltage above VEE		0.5		V
Voh	I_O = 0mA		3.8		V
	I_O = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Current Error Amplifier					
Ib			0.5	3	µA
Vio			3	20	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Error Amplifier (cont.)					
Avo		60	90		dB
GBW (Note 2)	Acl = 1, R_{IN} = 1k, CC=15pF, f=200kHz (Note 1)	4.5	7		MHz
Vol	I_O = 1mA, Voltage above VEE		0.5		V
Voh	I_O = 0mA		3.8		V
	I_O = –1mA		3.5		V
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
Voltage Error Amplifier					
Ib			0.5	3	µA
Vio			2	5	mV
Avo		60	90		dB
GBW (Note 2)	f = 200kHz	4.5	7		MHz
Vol	I_O = 175µA, Volts above VEE		0.3	0.6	V
Voh	ILIM > 3V	2.85	3	3.15	V
Voh - ILIM	Tested ILIM = 0.5V, 1.0V, 2.0V	–100		100	mV
CMRR	–0.2 < Vcm < 8V		80		dB
PSRR	10V < VCC < 20V		80		dB
2X Amplifier and Share Amplifier					
V offset (b; y = mx + b)				20	mV
GAIN (m; y = mx + b)	Slope with AV_{OUT} = 1V and 2V	1.98		2.02	V
GBW (Note 2)			100		kHZ
R_{SHARE}	VCC = 0, V_{SHARE}/I_{SHARE}		200		k
Total Offset	Negative supply is VEE, GND Open, VAO = GND	–75	0	75	mV
Vol	VAO = Voltage Amplifier Vol, Volts above VEE	0.2	0.45	0.6	V
Voh	I_O = 0mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
	I_O = –1mA, ILIM = 3V, VAO = Voltage Amp Voh	5.7	6	6.3	V
Adjust Amplifier					
Vio		40	60	80	mV
gm	I_{OUT}= –10µA to 10µA, V_{OUT} = 3.5V, C_{ADJ} = 1µF		–1		mS
Vol	I_{OUT} = 0	0.9	1	1.1	V
	I_{OUT} = 50µA	0.85	1	1.15	V
Voh	I_{OUT} = 0, V_{SHARE} = 6.5V	5.7	6	6.3	V
	I_{OUT} = –50µA, V_{SHARE} = 6.5V	5.7	6	6.3	V
Oscillator					
Frequency		450	500	550	kHz
Max Duty Cycle		80	85	90	%
OSC Ramp Amplitude		2	2.5	2.8	V
Clock Driver/SYNC (CLKSYN)					
Vol			0.02	0.2	V
Voh			3.6		V
	R_{CLKSYN} = 200Ω		3.2		V
I_{SOURCE}			25		mA
R_{CLKSYN}	VCC = 0, $V_{CLKSYN/ICLKSYN}$		10		k
V_{TH}			1.5		V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1849; –40°C to +85°C for UC2849; and 0°C to +70°C for UC3849; VCC = 12V, VEE = GND, Output no load, CT = 345pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1k, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VREF Comparator					
Turn-on threshold			4.65		V
Hysteresis			0.4		V
VCC Comparator					
Turn-on Threshold		7.9	8.3	8.7	V
Hysteresis			0.4		V
$\overline{\text{KILL}}$ Comparator					
Voltage Threshold			3		V
Sequence Comparator					
Voltage Threshold			2.5		V
SEQ SAT	I_O = 10mA		0.25		V
Enable Comparator					
Voltage Threshold			2.5		V
RUN SAT	I_O = 10mA		0.25		V
Reference					
VREF	T_A = 25°C	4.95	5	5.05	V
VREF	VCC = 15V	4.9		5.1	V
Line Regulation	10 < VCC < 20		3	15	mV
Load Regulation	0 < I_O < 10mA		3	15	mV
Short Circuit I	VREF = 0V	30	60	90	mA
Output Stage					
Rise Time	C_L = 100pF		10	20	ns
Fall Time	C_L = 100pF		10	20	ns
Voh	VCC > 11V, I_O = –10mA	8.0	8.4	8.8	V
	I_O = –200mA	7.8			V
Vol	I_O = 200mA			3.0	V
	I_O = 10mA			0.5	V
Virtual Ground					
V_{GND}-VEE	VEE is externally supplied, GND is floating and used as Signal GND.	0.2	0.75		V
Icc					
Icc (run)			21	30	mA

Note 1: If a closed loop gain greater than 1 is used, the possible GBW will increase by a factor of ACL + 10; where ACL is the closed loop gain.

Note 2: Guaranteed by design. not 100% tested in production.

Note 3: Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

PIN DESCRIPTIONS

ADJ: The output of the transconductance (gm = –1mS) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6V) its control voltage (VA+) until its load current is equal to the master. The 60mV input offset on the gm amplifier guarantees that the unit sensing the highest load current is chosen as the master. The 60mV offset guarantees by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30mV. This pin needs a 1μF capacitor to compensate the amplifier.

PIN DESCRIPTIONS (cont.)

CA–: The inverting input to the current error amplifier. This amplifier needs a capacitor between CA– and CAO to set its dominant pole.

CAO: The output of the current error amplifier which is internally clamped to 4V. It is internally connected to the inverting input of the PWM comparator.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier is not internally compensated so the user must compensate externally to attain the highest GBW for the application.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4V. The CLKSYN voltage is 3.6V when the oscillator capacitor (CT) is being discharged, otherwise it is 0V. If the recommended synchronization circuit is not used, a 1k or lower value resistor from CLKSYN to GND may be needed to increase fall time on CLKSYN pin.

CSO: The output of the current sense amplifier which is internally clamped to 4V.

$\overline{\text{ENBL}}$: The active low input with a 2.5V threshold enables the output to switch. SEQ and RUN are driven low when $\overline{\text{ENBL}}$ is above its 2.5V threshold.

GND: The signal ground used for the voltage sense amplifier, current sense amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

$\overline{\text{KILL}}$: The active low input with a 3.0V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving $\overline{\text{KILL}}$ above 3.0V and either resetting the power to the chip (VCC) or resetting the $\overline{\text{ENBL}}$ signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0V. A voltage less than 3.0V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp pin which has a capacitor (CT) to ground and a resistor (RDEAD) to the RDEAD pin programs its maximum duty cycle by programming a minimum dead time. The ramp oscillates between 1.2V to 3.4V when an RDEAD resistor is used. The maximum duty cycle can be increased by connecting RDEAD to OSC which changes the oscillator ramp to vary between 0.2V and 3.5V. In order to guarantee zero duty cycle in this configuration VEE should not be connected to GND.

The charge time is approximately $T_{CHARGE} = R_T \bullet C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \bullet RDEAD \bullet C_T$.

$$(1)\ Frequency \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}}$$

$$(2)\ Maximum Duty\ Cycle \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}}$$

The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5V. The peak current sink and source are 250mA. All UVLO, SEQ, $\overline{\text{ENBL}}$, and $\overline{\text{KILL}}$ logic either enable or disable the output driver.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is $2 \bullet RDEAD \bullet C_T$. The C_T capacitance should be increased by approximately 40pF to account for parasitic capacitance.

RT: This pin programs the charge time of the oscillator ramp. The charge current is

$$\frac{VREF}{2 \bullet R_T}$$

The charge time is approximately $T_{CHARGE} \approx R_T \bullet C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} \approx 2 \bullet RDEAD \bullet C_T$.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4V, VREF is greater than 4.65V, SEQ is greater than 2.5V, and $\overline{\text{KILL}}$ lower than 3.0V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND creates a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly DC voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA+, VA–: The inverting and non-inverting inputs to the voltage error amplifier.

PIN DESCRIPTIONS (cont.)

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

VCC: The input voltage of the chip. The chip is operational between 8.4V and 20V.

VEE: The negative supply to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0V.

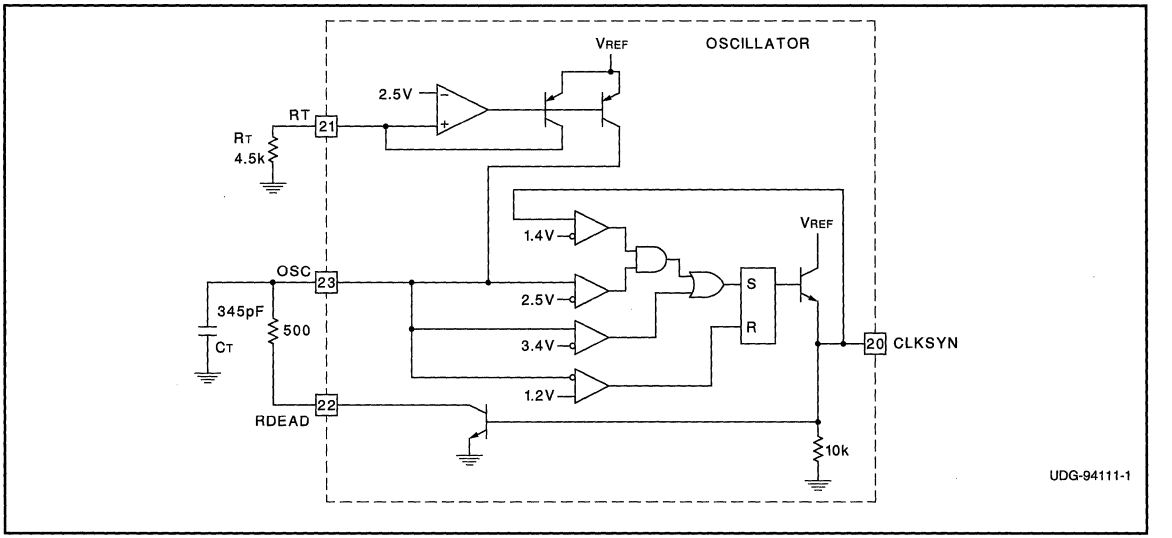


Figure 1. Oscillator Block with External Connections

CIRCUIT BLOCK DESCRIPTION:

PWM Oscillator: The oscillator block diagram with external connections is shown in Figure 1. A resistor (R_T) connected to pin RT sets the linear charge current;

$$I_{RT} \approx \frac{2.5V}{R_T}$$

The timing capacitor (C_T) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4V threshold. After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. This discharge time with the RC time delay of 2 • C_T • RDEAD is the minimum output low time. OSC continues to discharge until it reaches a 1.2V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Figure 2. Equations to approximate frequency and maximum duty cycle are listed under the OSC pin description. Figure 3 and 4 graphs show measured variation of frequency and maximum duty cycle with varying RT, CT, and RDEAD component values.

As shown in Figure 5, several oscillators are synchronized to the highest free running frequency by connecting 100pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10k. Referring to Figure 1, the synchronization threshold is 1.4V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5V. This allows units, once they discharge below 2.5V, to continue through the

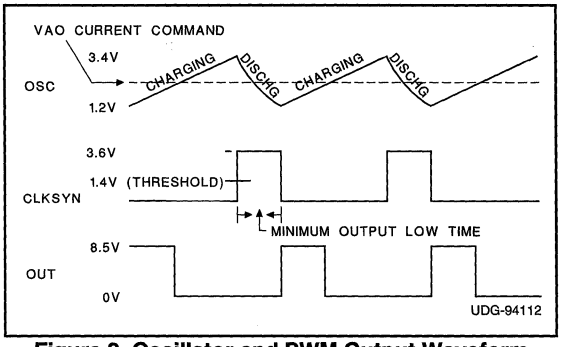


Figure 2. Oscillator and PWM Output Waveform

CIRCUIT BLOCK DESCRIPTION (cont.)

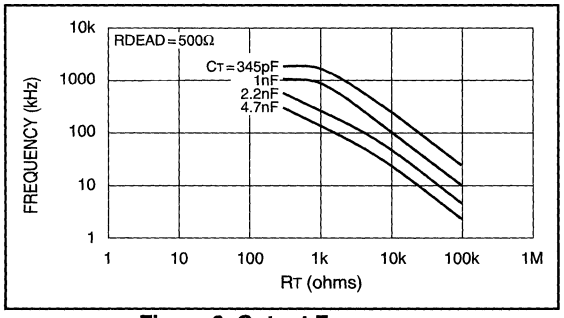


Figure 3. Output Frequency

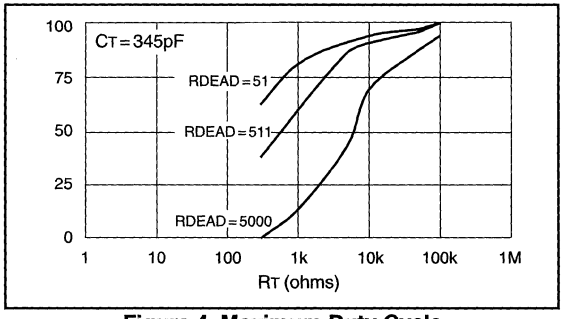


Figure 4. Maximum Duty Cycle

current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to guarantee synchronization.

Grounds, Voltage Sensing and Current Sensing: The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 6, the positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA–), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, R_S.

Figure 6 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. The voltage offset on the current sense amplifier is not needed if VEE is separated from GND. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7V below ground. The resistor R_{ADJ} is used for load sharing. The unit which is the

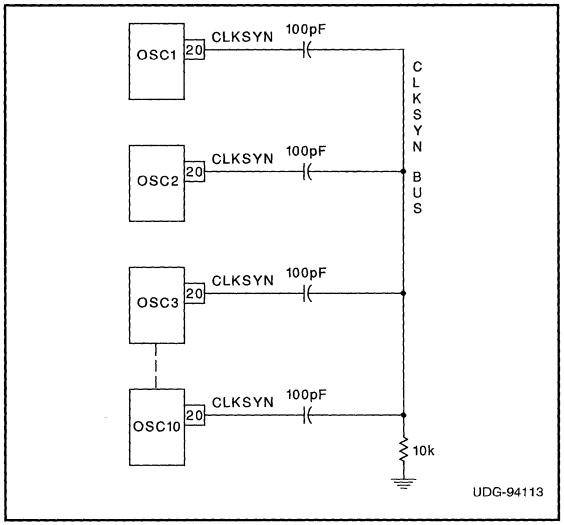


Figure 5. Oscillator Synchronization Connection Diagram

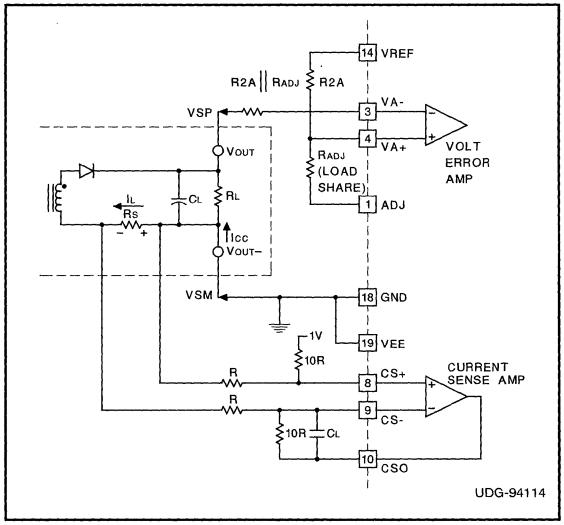


Figure 6. Voltage and Current Sense VEE Tied to GND

master will force V_{ADJ} to 1.0V. Therefore, the regulated voltage being sensed is actually:

$$VSP - VSM = (VREF - V_{ADJ}) \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}} \right) + V_{ADJ}$$

$$VSM = 0V, V_{ADJ} = 1V\,(master), VREF = 5V$$

CIRCUIT BLOCK DESCRIPTION (cont.)

$$VSP = 4 \bullet \left(\frac{R_{ADJ}}{R1 + R_{ADJ}} \right) + 1V$$

The ADJ pin voltage on the slave chips will increase forc-

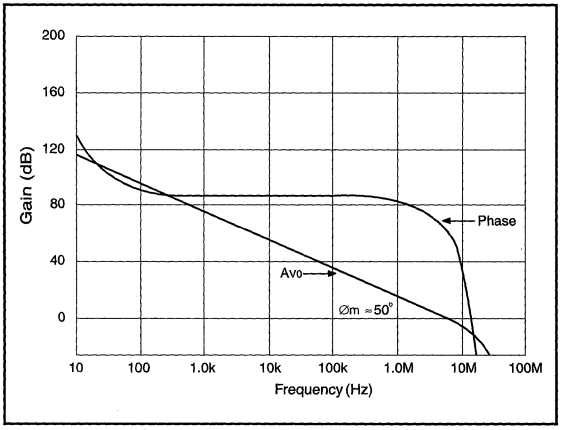


Figure 7. AC Frequency Response of the Voltage Error Amplifier

ing their load currents to increase to match the master.

The AC frequency response of the voltage error amplifier is shown in Figure 7.

Startup and Shutdown: Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC1849 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it will command zero load current, guaranteeing a soft start. The undervoltage lockout (UVLO) is a logical AND of $\overline{ENBL}$ < 2.5V, SEQ > 2.5V, VCC > 8.4V and VREF > 4.65V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the $\overline{ENBL}$ pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4V. The $\overline{KILL}$ input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after $\overline{KILL}$ has been initiated, the chip must be powered down and then back up. A pulse on the $\overline{ENBL}$ pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing: Load sharing is accomplished similar to the UC1907. The sensed current for the UC1849 has an AC component that is amplified and then averaged. The voltage error amplifier output is the current command signal representing the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The IC with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60mV input offset guarantees that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) ICs to adjust their respective references high in order to balance each IC's load current. The master's ADJ pin will be at its 1.0V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0V.

VREF can be adjusted 150mV to 300mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} will typically be 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1V ±100mV by a factor of 10 to 30, contributing only a 3mV to 10mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop: The current sense amplifier (CSA) is designed specifically for the task of sensing and amplifying the inductor ripple current at frequencies up to 1MHz. The CSA's input offset voltage (VIO) is trimmed to less than 1mV to minimize error of the average current signal. This amplifier is not internally compensated allowing the user to optimally choose the zero crossing bandwidth.

$$(3)\quad Frequency\,(0dB) = \frac{1}{2\pi R_{INV} \bullet C_{COMP}}$$

R_{INV} is the input resistance at the inverting terminal CS–
C_{COMP} is the capacitance between C_S– and CSO.

Although it is only unity gain stable for a GBW of 7MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate at 70MHz with sufficient phase margin. A closed loop gain of 10 attenuates the output by 20.8dB.

CIRCUIT BLOCK DESCRIPTION (cont.)

$$20.8 = 20 \log \bullet \frac{1}{11}$$

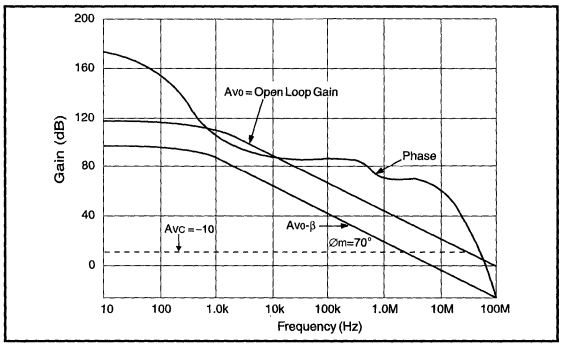


Figure 8. Current Sense Amplifier and Current Error Amplifier Bode Plot

to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity at 7MHz, where the phase margin begins to roll off. See Figure 8 for typical Bode plot.

The gain of the differential current sense amplifier (CS_{GAIN}) is calculated by knowing the maximum load current. The maximum voltage across the shunt resistor (R_S) divided by R_S is the maximum load current. By amplifying the voltage across RS, V_{RS}, to be equal to the voltage error amplifier Voh, the current control loop keeps the load from exceeding its current limit. Voh is set at 3.0V if ILIM is connected to VREF. The maximum current limit clamp can be reduced by reducing the voltage at ILIM to less than 3.0V as described in the ILIM pin description.

$$(4) \qquad R_S = \frac{V_{RS}}{Max\, I_{LOAD}}$$

$$(5) \qquad CS_{GAIN} = \frac{V_{ILIM}}{V_{RS}}$$

The current error amplifier (CEA) also needs its loop compensated by the user with the same criteria as the current sense amplifier. This amplifier is essentially the same wide bandwidth amplifier without the input offset voltage trim. The zero crossing can also be approximately calculated with Equation 3. The gain bandwidth of the current loop is optimized by matching the inductor downslope (V_O/L) to the oscillator ramp slope ($V_S \bullet f_S$). Subharmonic oscillation problems are avoided by keeping the amplified inductor downslope less than the oscillator ramp slope.

The following equation determines the current error amplifier gain (GCA):

$$(6) \qquad GCA = \frac{V_S \bullet f_S}{(V_O / L) \bullet R_S \bullet CS_{GAIN}};$$

where CS_{GAIN} and R_S are defined by equations 4 and 5,

Vs is the oscillator peak to peak voltage,

fs is the oscillator frequency,

V_O is the output voltage,

and L is the inductance.

Additional Information about average current mode control can be found in Unitrode Application Note U-140.

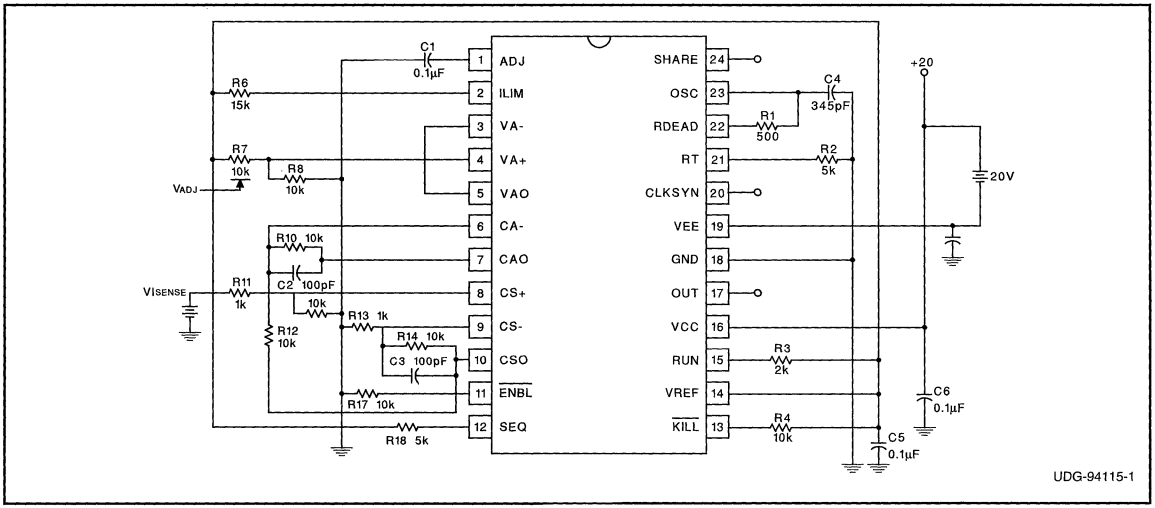


Figure 9. Open Loop Circuit

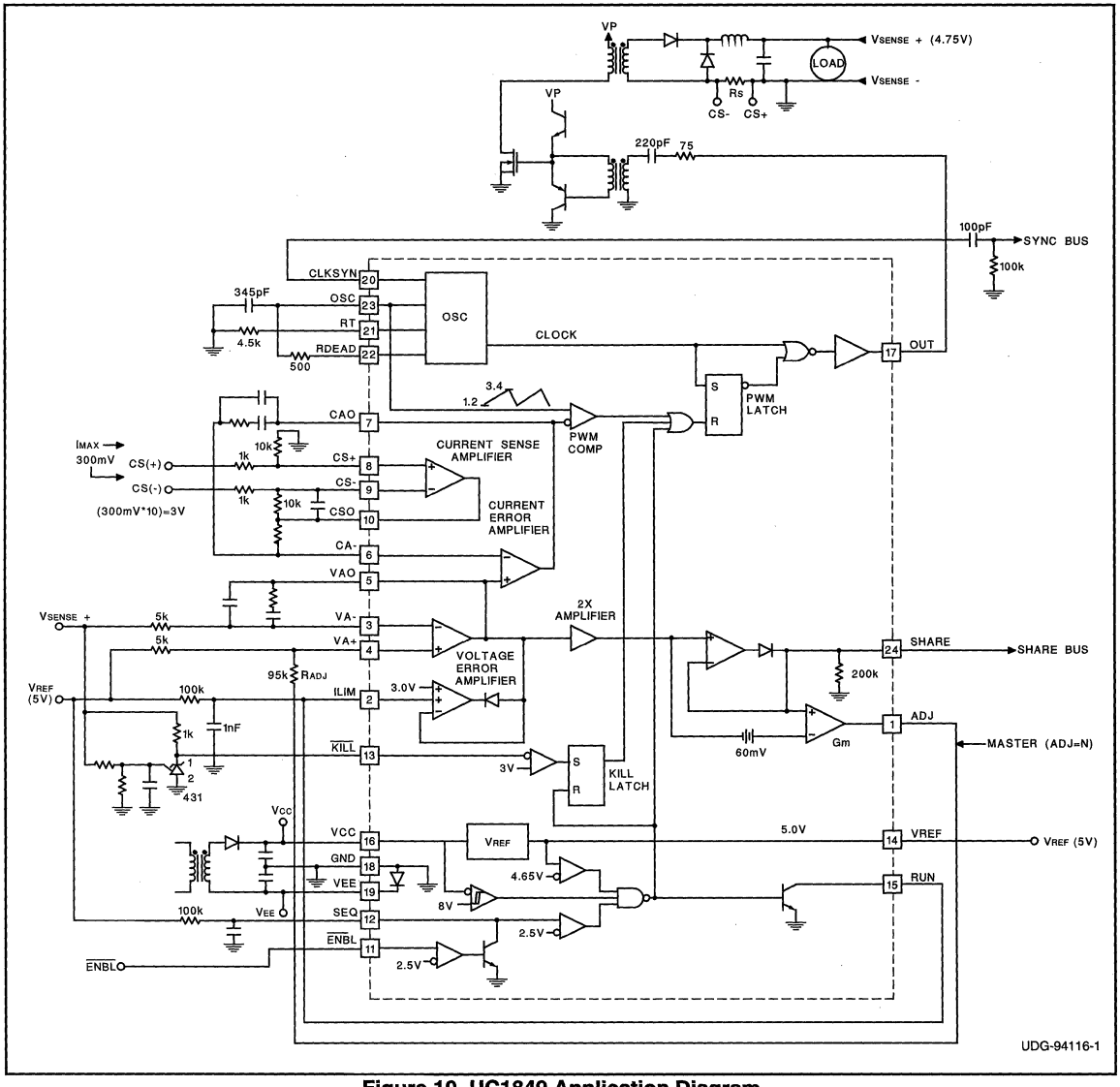


Figure 10. UC1849 Application Diagram

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UNITRODE

application INFO available

UC1851
UC2851
UC3851

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

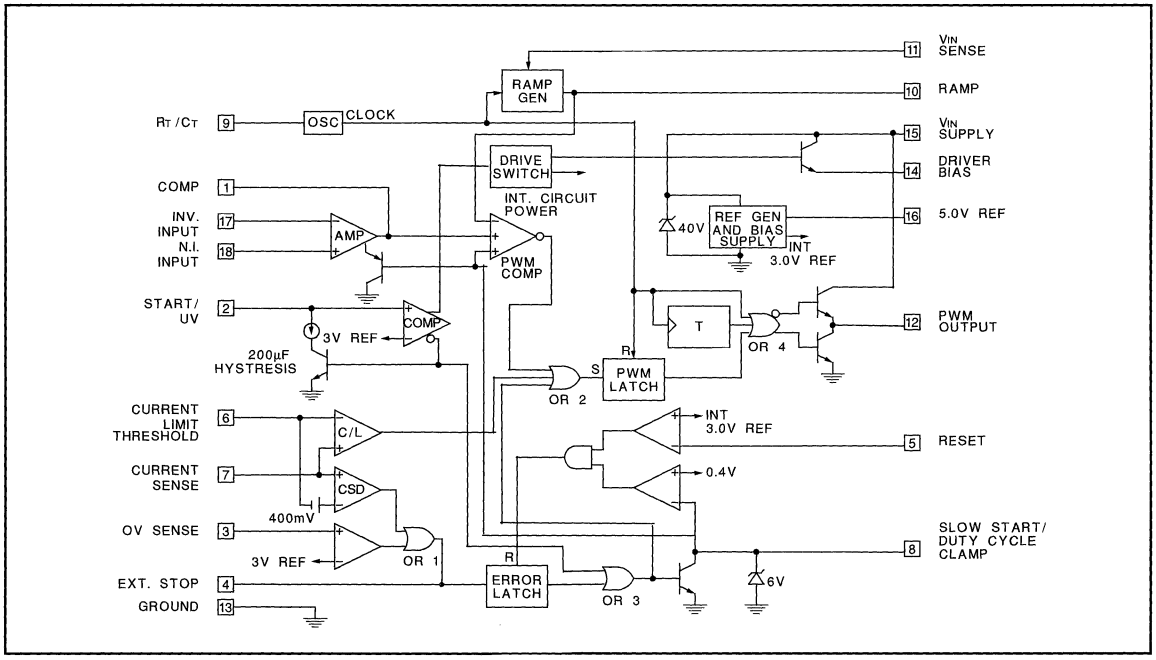
DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +VIN (Pin 15)
- Voltage Driven ..... +32V
- Current Driven, 100mA maximum ..... Self-limiting

PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) ..... -200mA
Reference Output Current (Pin 16) ..... -50mA
Slow-Start Sink Current (Pin 8) 20mA
VIN Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) ..... -0.5 to +5.5V
Stop Input (Pin 4) ..... -0.3 to +5.5V
Comparator Inputs (Pins 1–7, 9–11, 16) ..... Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C

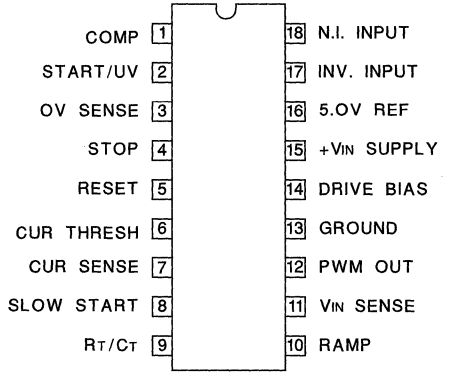
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal

Note 2: All pin numbers are referenced to DIL-18 package.

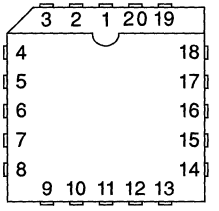
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L PACKAGE



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
COMP	1
START/UV	2
OV SENSE	3
STOP	4
RESET	5
CUR THRESH	7
CUR SENSE	8
SLOW START	9
RT/CT	10
RAMP	11
VIN SENSE	12
PWM OUT	13
GROUND	14
DRIVE BIAS	15
+VIN SUPPLY	17
5.0V REF	18
INV. INPUT	19
N.I. INPUT	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; VIN = 20V, RT = 20kΩ, CT = .001 mfd, RR = 10kΩ, CR = .001mfd. Current Limit Threshold = 200mV, TA = TJ.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	VIN = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	VIN = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	VIN = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	TJ = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	VIN = 8 to 30V		10	15		10	20	mV
Load Regulation	IL = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	VREF = 0, TJ = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	TJ = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	VIN = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	RT = 2kΩ, CT = 330pF	500			500			kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

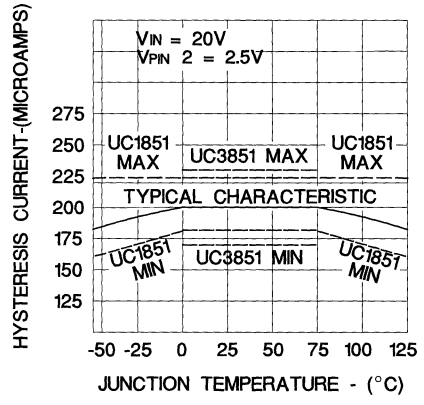
PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = –10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max Output ® Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 1)	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate (Note 1)	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	I_{SOURCE} = 20mA	18	18.5		18	18.5		V
	I_{SOURCE} = 200mA	17	18.5		17	18.5		V
Rise Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Fall Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Comparator Delay (Note 1)	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN}-V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 1)	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

Note 1:Guaranteed by design. Not 100% tested in production.

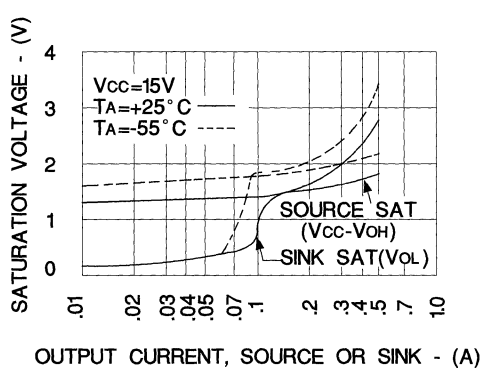
FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external RT and CT. Frequency = $\frac{K_C}{R_T C_T}$ where KC is a first-order correction factor ≈ 0.3 log (CT x 10^{12}).
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{d_V}{d_T} = \frac{\text{sense voltage}}{R_R C_R}$. CR is normally selected ≤ CT and its value will have some effect upon valley duty cycle. Limiting the minimum value for ISENSE into pin 11 will establish a maximum duty cycle clamp. CR terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by RsCs for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/µF.

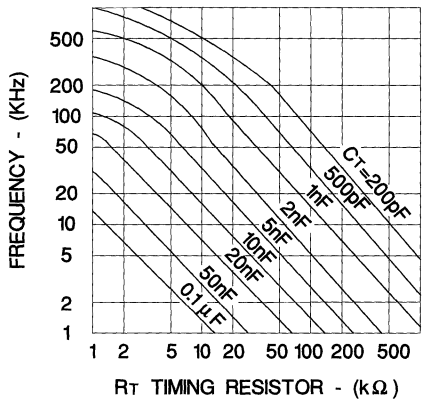
Start/UV Hysteresis Current



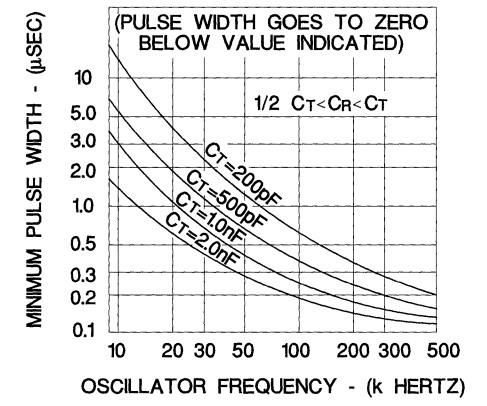
Output Saturation Characteristics



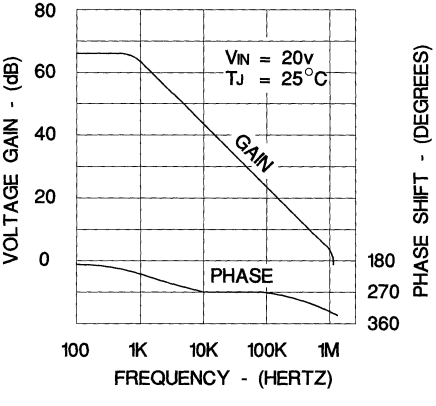
Oscillator Frequency



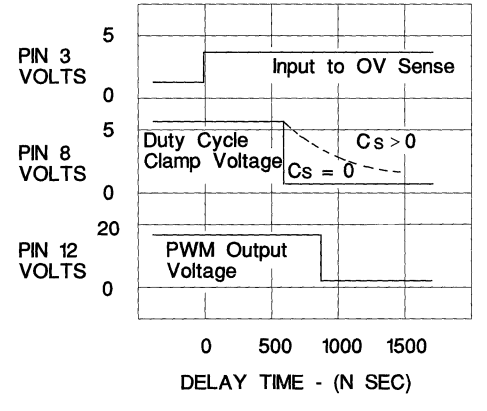
PWM Output Minimum Pulse Width



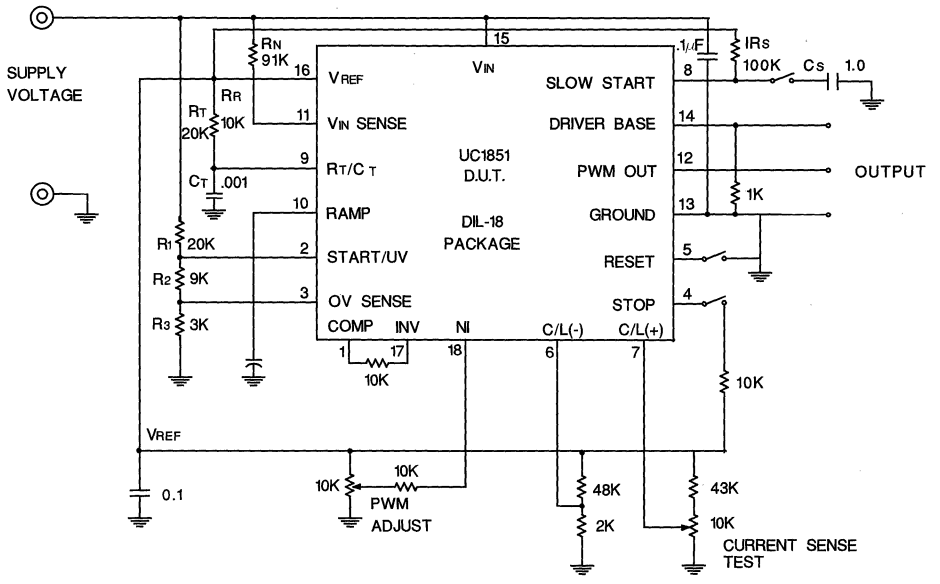
Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



OPEN-LOOP CIRCUIT



$$\text{Nominal Frequency} = \frac{1}{RTCT} = 50kHz$$

$$\text{Start Voltage} = 3\left(\frac{R1+R2+R3}{R2+R3}\right) + 0.2R1 = 12V$$

$$\text{UV Fault Voltage} = 3\left(\frac{R1+R2+R3}{R2+R3}\right) = 8V$$

$$\text{OV Fault Voltage} = 3\left(\frac{R1+R2+R3}{R3}\right) = 32V$$

Current Limit = 200mV

Current Fault Voltage = 600mV

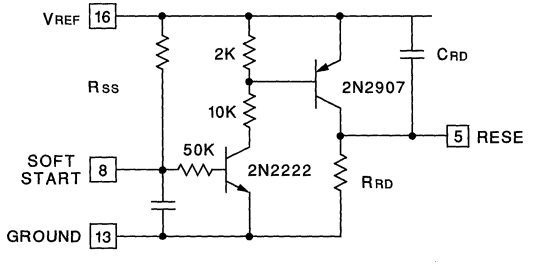
Duty Cycle Clamp = 50%

@VIN = 15V, Duty Cycle = 48%

@VIN = 30V, Duty Cycle = 24%

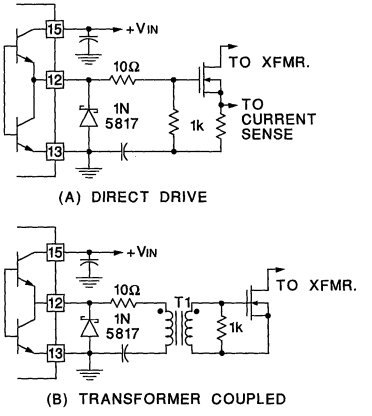
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Programmable Soft Start and Restart Delay Circuit



For further application information see UC1840/UC1841 Data Sheets

UC1851 Power MOSFET Drive Interface



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UNITRODE

application INFO available

UC1856
UC2856
UC3856

Improved Current Mode PWM Controller

FEATURES

- Pin-for-Pin Compatible With the UC3846
- 65ns Typical Delay From Shutdown to Outputs, and 50ns Typical Delay From Sync to Outputs
- Improved Current Sense Amplifier With Reduced Noise Sensitivity
- Differential Current Sense with 3V Common Mode Range
- Trimmed Oscillator Discharge Current for Accurate Deadband Control
- Accurate 1V Shutdown Threshold
- High Current Dual Totem Pole Outputs (1.5A peak)
- TTL Compatible Oscillator SYNC Pin Thresholds
- 4kV ESD Protection

DESCRIPTION

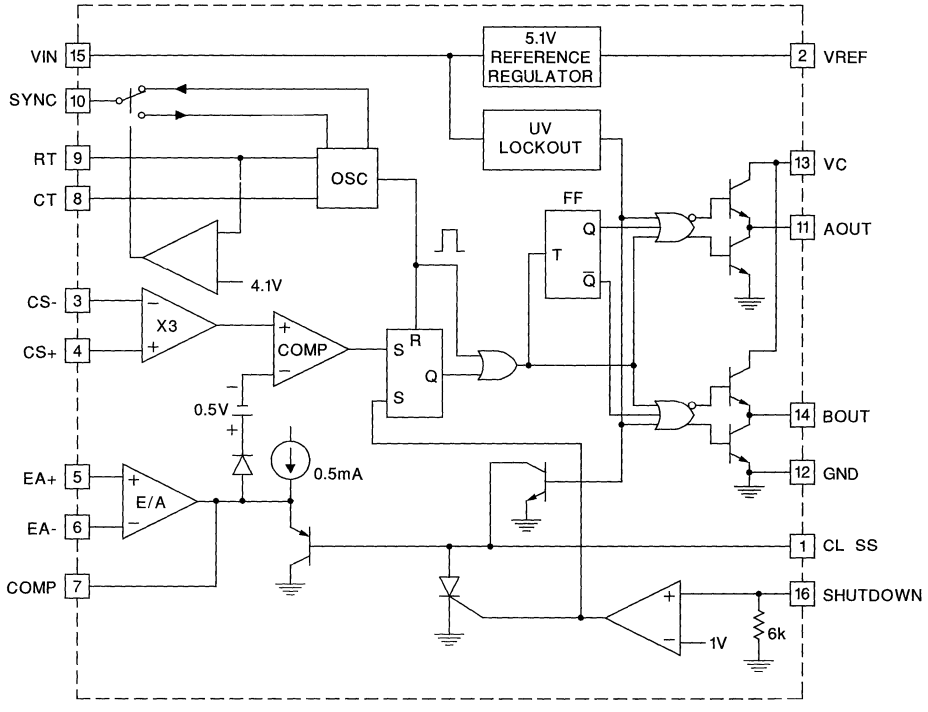
The UC3856 is a high performance version of the popular UC3846 series of current mode controllers, and is intended for both design upgrades and new applications where speed and accuracy are important. All input to output delays have been minimized, and the current sense output is slew rate limited to reduce noise sensitivity. Fast 1.5A peak output stages have been added to allow rapid switching of power FETs.

A low impedance TTL compatible sync output has been implemented with a tri-state function when used as a sync input.

Internal chip grounding has been improved to minimize internal "noise" caused when driving large capacitive loads. This, in conjunction with the improved differential current sense amplifier results in enhanced noise immunity.

Other features include a trimmed oscillator current (8%) for accurate frequency and dead time control; a 1V, 5% shutdown threshold; and 4kV minimum ESD protection on all pins.

BLOCK DIAGRAM



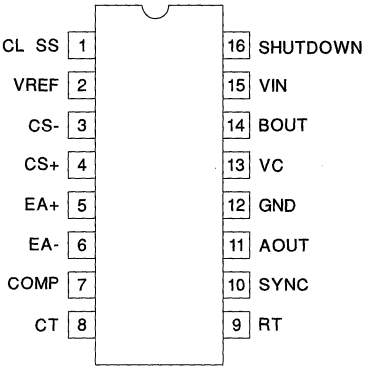
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +40V
Collector Supply Voltage . . . . . +40V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 2.0A
Error Amp Inputs . . . . . $-0.3V$ to $+V_{IN}$
Shutdown Input . . . . . $-0.3V$ to $+10V$
Current Sense Inputs . . . . . $-0.3V$ to $+3V$
SYNC Output Current . . . . . ±10mA
Error Amplifier Output Current . . . . . –5mA
Soft Start Sink Current 50mA
Oscillator Charging Current 5mA
Power Dissipation at $T_A = 25°C$ (Note 2) 1000mW
Power Dissipation at $T_C = 25°C$ (Note 2) 2000mW
Junction Temperature . . . . . –55°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

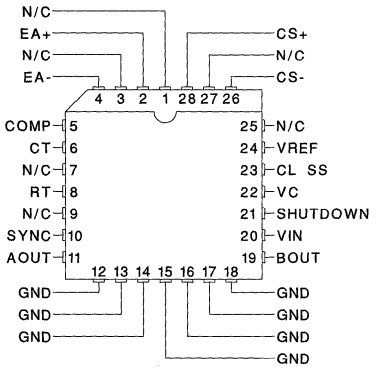
All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

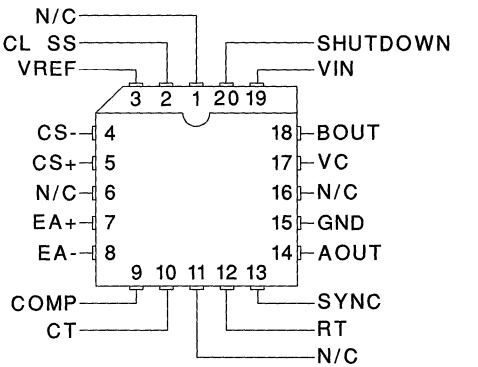
DIL–16, SOIC-16 (Top View)
J or N, DW PACKAGE



PLCC-28 (Top View)
QP PACKAGE



PLCC-20 (Top View)
Q PACKAGE



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for UC1856; $-40°C$ to $+85°C$ for the UC2856; and $0°C$ to $+70°C$ for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	$T_J = 25°C$, $I_O = 1mA$	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	VIN = 8V to 40V			20			20	mV
Load Regulation	$I_O = -1mA$ to $-10mA$			15			15	mV
Total Output Variation	Line, Load, and Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage	$10Hz < f < 10kHz$, $T_J = 25°C$		50			50		µV
Long Term Stability	$T_J = 125°C$, 1000 Hrs (Note 2)		5	25		5	25	mV
Short Circuit Current	VREF = 0V	–25	–45	–65	–25	–45	–65	mA
Oscillator Section								
Initial Accuracy	$T_J = 25°C$	180	200	220	180	200	220	kHz
	Over Operating Range	170		230	170		230	kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for UC1856; –40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (cont.)								
Voltage Stability	VIN = 8V to 40V			2			2	%
Discharge Current	T_J = 25°C, V_{CT} = 2V	7.5	8.0	8.8	7.5	8.0	8.8	mA
	V_{CT} = 2V	6.7	8.0	8.8	6.7	8.0	8.8	mA
Sync Output High Level	I_O = –1mA	2.4	3.6		2.4	3.6		V
Sync Output Low Level	I_O = +1mA		0.2	0.4		0.2	0.4	V
Sync Input High Level	CT = 0V, RT = VREF	2.0	1.5		2.0	1.5		V
Sync Input Low Level	CT = 0V, RT = VREF		1.5	0.8		1.5	0.8	V
Sync Input Current	CT = 0V, RT = VREF V_{SYNC} = 5V		1	10		1	10	µA
Sync Delay to Outputs	CT = 0V, RT = VREF V_{SYNC} = 0.8V to 2V		50	100		50	100	ns
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 2V			5			10	mV
Input Bias Current				–1			–1	µA
Input Offset Current				500			500	nA
Common Mode Range	VIN = 8V to 40V	0		VIN-2	0		VIN-2	V
Open Loop Gain	V_O = 1.2V to 3V	80	100		80	100		dB
Unity Gain Bandwidth	T_J = 25°C	1	1.5		1	1.5		MHz
CMRR	V_{CM} = 0V to 38V, VIN = 40V	75	100		75	100		dB
PSRR	VIN = 8V to 40V	80	100		80	100		dB
Output Sink Current	V_{ID} = –15mV, V_{COMP} = 1.2V	5	10		5	10		mA
Output Source Current	V_{ID} = 15mV, V_{COMP} = 2.5V	–0.4	–0.5		–0.4	–0.5		mA
Output High Level	V_{ID} = 50mV, R_L (COMP) = 15k	4.3	4.6	4.9	4.3	4.6	4.9	V
Output Low Level	V_{ID} = –50mV, R_L (COMP) = 15k		0.7	1		0.7	1	V
Current Sense Amplifier Section								
Amplifier Gain	V_{CS} – = 0V, CL SS Open (Notes 3,4)	2.5	2.75	3.0	2.5	2.75	3.0	V/V
Maximum Differential Input Signal (V_{CS}+ - V_{CS}–)	CL SS Open (Note 3) R_L (COMP) = 15k	1.1	1.2		1.1	1.2		V
Input Offset Voltage	$V_{CL\ SS}$ = 0.5VCOMP Open (Note 3)		5	35		5	35	mV
CMRR	V_{CM} = 0V to 3V	60			60			dB
PSRR	VIN = 8V to 40V	60			60			dB
Input Bias Current	$V_{CL\ SS}$ = 0.5V, COMP Open (Note 3)			–1	–3	–1	–3	µA
Input Offset Current	$V_{CL\ SS}$ = 0.5V, COMP Open (Note 3)			1			1	mA
Input Common Mode Range		0		3	0		3	V
Delay to Outputs	V_{EA}+ = VREF, EA– = 0V CS+ – CS– = 0V to 1.5V		120	250		120	250	ns
Current Limit Adjust Section								
Current Limit Offset	V_{CS}– = 0V V_{CS}+ = 0V, COMP = Open (Note 3)	0.43	0.5	0.57	0.43	0.5	0.57	V
Input Bias Current	V_{EA}+ = VREF, V_{EA}– = 0V		–10	–30		–10	–30	µA
Shutdown Terminal Section								
Threshold Voltage		0.95	1.00	1.05	0.95	1.00	1.05	V
Input Voltage Range		0		5	0		5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for UC1856; –40°C to +85°C for the UC2856; and 0°C to +70°C for the UC3856, VIN = 15V, RT = 10k, CT = 1nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1856/UC2856			UC3856			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Shutdown Terminal Section (cont.)								
Minimum Latching Current ($I_{CL\ SS}$)	(Note 5)	3	1.5		3	1.5		mA
Maximum Non-Latching Current ($I_{CL\ SS}$)	(Note 6)		1.5	0.8		1.5	0.8	mA
Delay to Outputs	$V_{SHUTDOWN}$ = 0 to 1.3V		65	110		65	110	ns
Output Section								
Collector-Emitter Voltage		40			40			V
Off-State Bias Current	VC = 40V			250			250	µA
Output Low Level	I_{OUT} = 20mA		0.1	0.5		0.1	0.5	V
	I_{OUT} = 200mA		0.5	2.6		0.5	2.6	V
Output High Level	I_{OUT} = –20mA	12.5	13.2		12.5	13.2		V
	I_{OUT} = –200mA	12	13.1		12	13.1		V
Rise Time	C1 = 1nF		40	80		40	80	ns
Fall Time	C1 = 1nF		40	80		40	80	ns
UVLO Low Saturation	VIN = 0V, I_{OUT} = 20mA		0.8	1.5		0.8	1.5	V
PWM Section								
Maximum Duty Cycle		45	47	50	45	47	50	%
Minimum Duty Cycle				0			0	%
Undervoltage Lockout Section								
Startup Threshold			7.7	8.0		7.7	8.0	V
Threshold Hysterisis			0.7			0.7		V
Total Standby Current								
Supply Current			18	23		18	23	mA

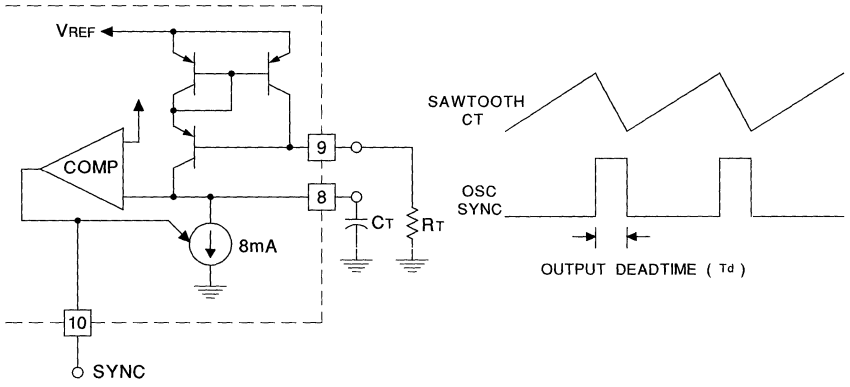
Note 1: All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
Note 2: This parameter, although guaranteed over the recommended operating conditions is not 100% tested in production.
Note 3: Parameter measured at trip point of latch with V_{EA}+ = VREF, V_{EA}– = 0V.
Note 4: Amplifier gain defined as:

$$G = \frac{\Delta V_{COMP}}{\Delta V_{CS}+}; \quad \Delta V_{CS} - = 0V\ TO\ 1.0V$$

Note 5: Current into CL SS guaranteed to latch circuit into shutdown state.
Note 6: Current into CL SS guaranteed not to latch circuit into shutdown state.

APPLICATIONS INFORMATION

Oscillator Circuit



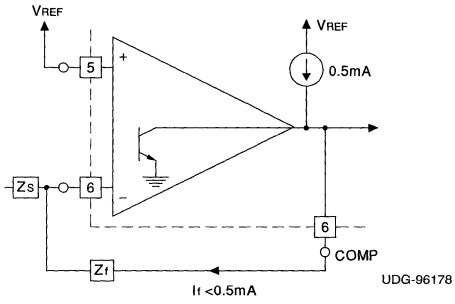
Output deadtime is determined by size of the external capacitor, C_T, according to the formula: $Td = \frac{2C_T}{8mA - \frac{3.6}{R_T}}$

For large values of R_T: $Td = 250C_T$

Oscillator frequency is approximated by the formula: $f_T = \frac{2}{R_T C_T}$

UDG-96177

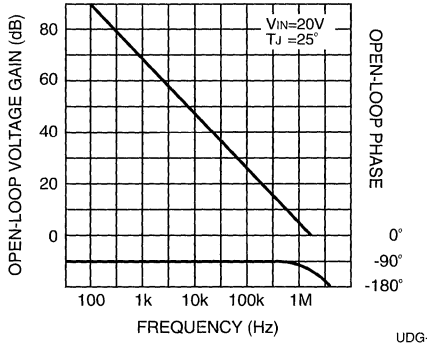
Error Amplifier Output Configuration



UDG-96178

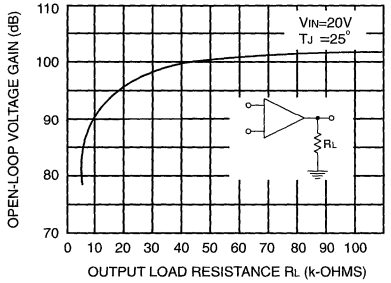
Error Amplifier can source up to 0.5mA.

Error Amplifier Gain and Phase vs Frequency



UDG-96179

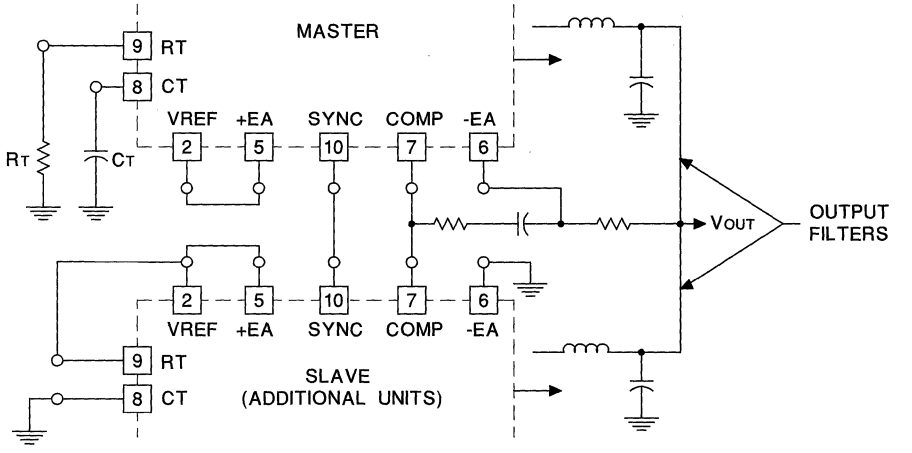
Error Amplifier Open-Loop D.C. Gain vs Load Resistance



UDG-96180

APPLICATIONS INFORMATION (cont.)

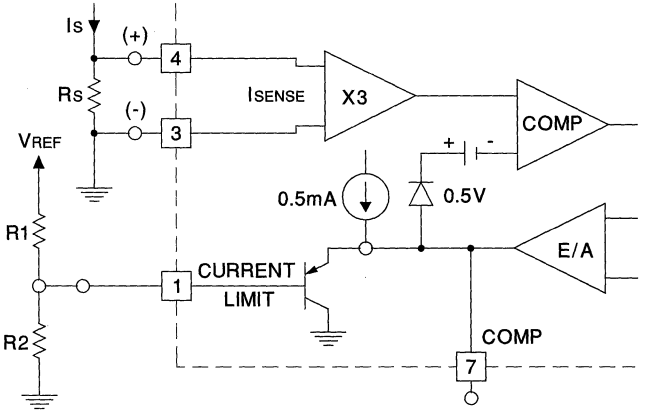
Parallel Operation



UDG-96181

Slaving allows parallel operation of two or more units with equal current sharing.

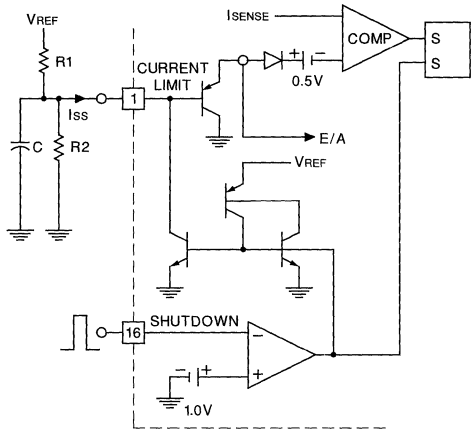
Pulse by Pulse Current Limiting



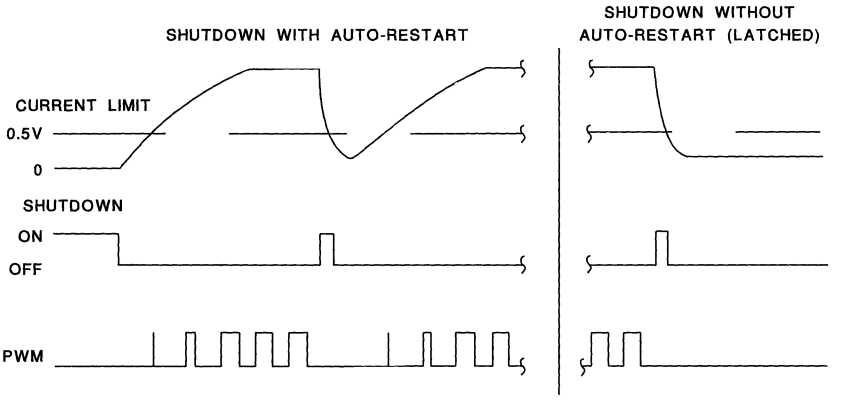
UDG-96182

Peak current (Is) is determined by the formula: $Is = \dfrac{\left(\dfrac{R2V_{REF}}{R1+R2}\right) - 0.5}{3R_S}$

APPLICATIONS INFORMATION (cont.)



UDG-96183

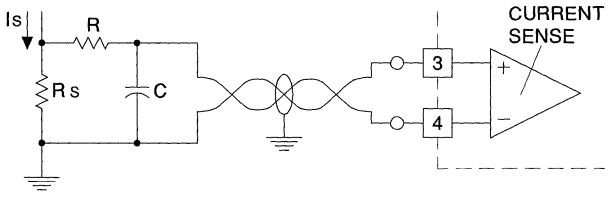


UDG-96184

If $\frac{V_{REF}}{R1}$ < 0.8mA, the shutdown latch will commutate when I_{SS} = 0.8mA and a restart cycle will be initiated.

If $\frac{V_{REF}}{R1}$ < 3mA, the device will latch off until power is recycled.

Current Sense Amplifier Connections

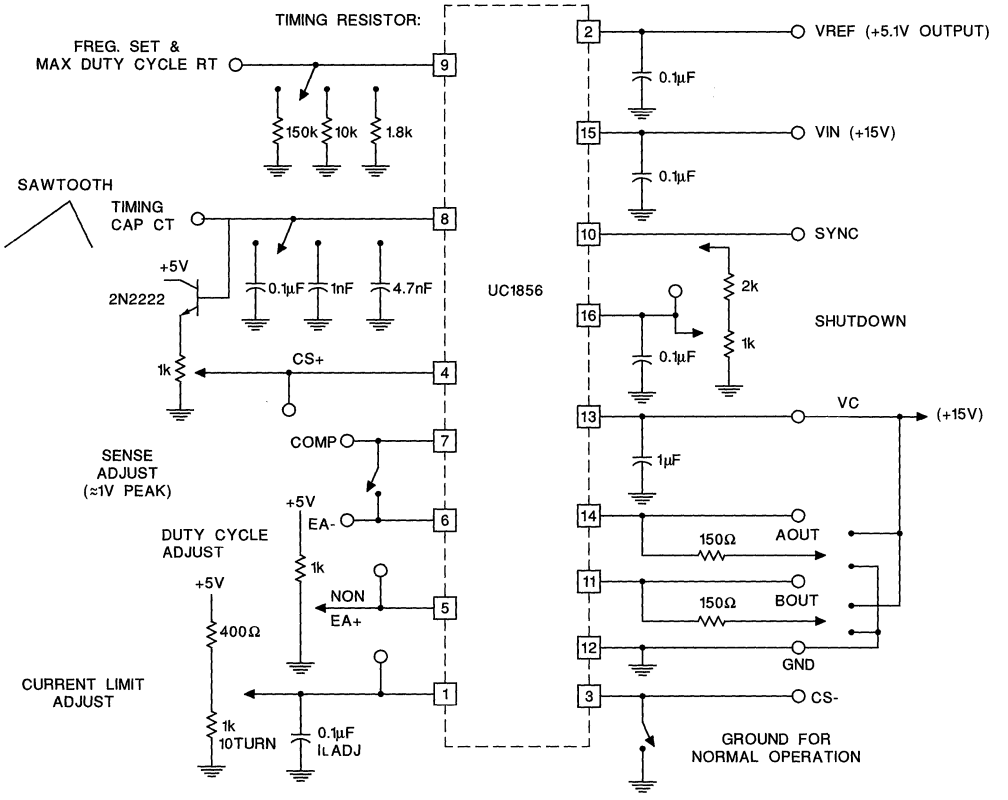


UDG-96185

A small RC filter may be required in some applications to reduce switch transients. Differential input allows remote, noise sensing.

APPLICATIONS INFORMATION (cont.)

UC1856 Open Loop Test Circuit



- BYPASS CAPS SHOULD BE LOW ESR & ESL TYPE
- SHORT E/A- & COMP FOR UNITY GAIN TESTING

THE USE OF A GROUND PLANE IS HIGHLY RECOMMENDED

UDG-96186

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

application INFO available

UC1860
UC2860
UC3860

Resonant Mode Power Supply Controller

FEATURES

- 3MHz VFO Linear over 100:1 Range
- 5MHz Error Amplifier with Controlled Output Swing
- Programmable One Shot Timer—Down to 100ns
- Precision 5V Reference
- Dual 2A Peak Totem Pole Outputs
- Programmable Output Sequence
- Programmable Under Voltage Lockout
- Very Low Start Up Current
- Programmable Fault Management & Restart Delay
- Uncommitted Comparator

DESCRIPTION

The UC1860 family of control ICs is a versatile system for resonant mode power supply control. This device easily implements frequency modulated fixed-on-time control schemes as well as a number of other power supply control schemes with its various dedicated and programmable features.

The UC1860 includes a precision voltage reference, a wide-bandwidth error amplifier, a variable frequency oscillator operable to beyond 3MHz, an oscillator-triggered one-shot, dual high-current totem-pole output drivers, and a programmable toggle flip-flop. The output mode is easily programmed for various sequences such as A, off, B, off; A & B, off; or A, B, off. The error amplifier contains precision output clamps that allow programming of minimum and maximum frequency.

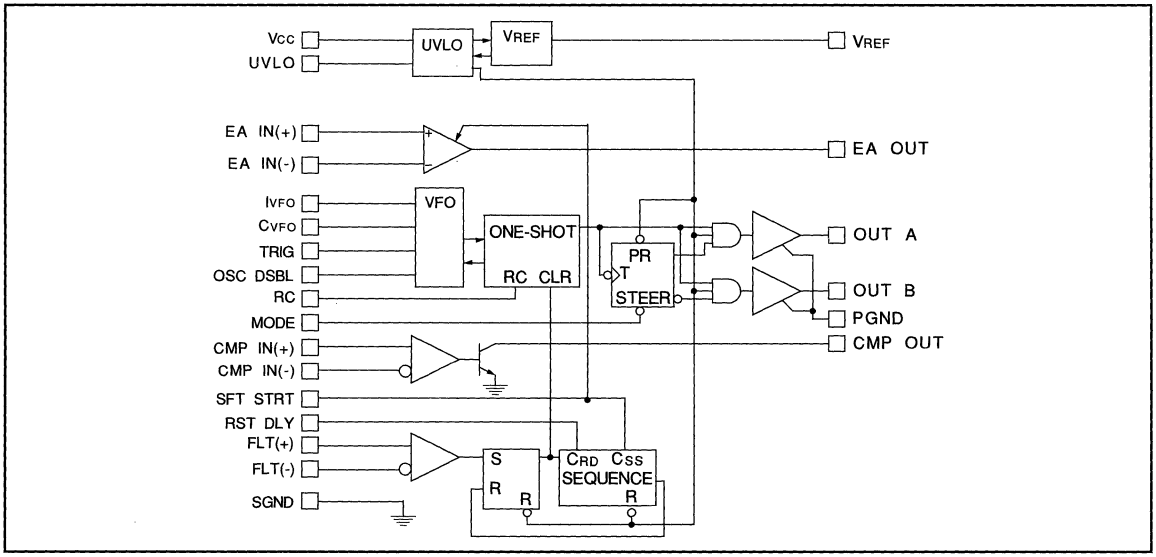
The device also contains an uncommitted comparator, a fast comparator for fault sensing, programmable soft start circuitry, and a programmable restart delay. Hic-up style response to faults is easily achieved. In addition, the UC1860 contains programmable under voltage lockout circuitry that forces the output stages low and minimizes supply current during start-up conditions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 19) 20V
Output Current, Source or Sink (pins 17 & 20)
  DC 0.8A
  Pulse (0.5µs) 3.0A
Power Ground Voltage . . . . . ±0.2V
Inputs (pins 1, 2, 3, 4, 8, 9, 11, 12,
  13, 14, 21, 22, 23 & 24) . . . . . –0.4 to 6V
Error Amp Output Current, Source or Sink (pin 5) 2mA
I_{VFO} Current (pin 7) 2mA
Comparator Output Current (pin 15) 5mA
Comparator Output Voltage (pin 15) 15V
Soft Start or Restart Delay Sink Current (pins 22 & 23) . . . 5mA
Power Dissipation at T_A = 50°C (DIP) 1.25W
Power Dissipation at T_A = 50°C (PLCC) 1W
Lead Temperature (Soldering, 10 seconds) . . . . . 300°C

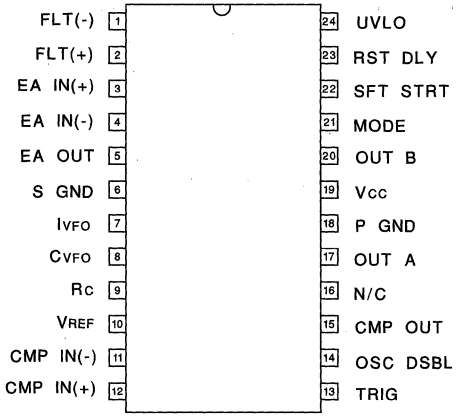
Note: All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the DIP. Refer to Packaging Section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

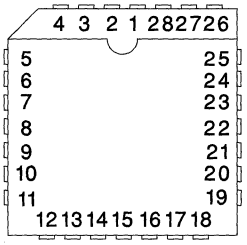


CONNECTION DIAGRAMS

DIL - 24 (TOP VIEW)
J or N Package



PLCC-28, LCC-28
(TOP VIEW)
Q or L Package



PIN PACKAGE FUNCTION	
FUNCTION	PIN
S GND	1
IVFO	2
CVFO	3
RC	4
VREF	5
CMP IN (-)	6
CMP IN (+)	7
TRIG	8
OSC DSBL	9
CMP OUT	10
N/C	11, 12
OUT A	13
PGND	14
N/C	15
VCC	16
OUT B	17
N/C	18, 19
MODE	20
SFT STRT	21
RST DLY	22
UVLO	23
FLT (-)	24
FLT (+)	25
EA IN (+)	26
EA IN (-)	27
EA OUT	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, all specifications apply for -55°C ≤ T_A ≤ 125°C for the UC1860, -25°C ≤ T_A ≤ 85°C for the UC2860, 0 ≤ T_A ≤ 70°C for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_A = 25°C, I_O = 0	4.95	5.00	5.05	V
	I_O = 0, Over Temp	4.93		5.07	V
Line Regulation	10 ≤ V_{CC} ≤ 20V		2	15	mV
Load Regulation	0 ≤ I_O ≤ 10mA		2	25	mV
Output Noise Voltage*	10Hz ≤ f ≤ 10kHz		50		μVRMS
Short Circuit Current	V_{REF} = 0V	-150		-15	mA
Error Amplifier Section					
Input Offset Voltage	2.8 ≤ V_{CM} ≤ 4.5V		1	8	mV
Input Bias Current			50	500	nA
Open Loop Gain	dVO = 1.5V	60	80		dB
PSRR	10 ≤ V_{CC} ≤ 20V	70	100		dB
Output Low (VO-V_{IVFO})	-0.1 ≤ I_O ≤ 0.1mA	-8	0	8	mV
Output High (VO-V_{IVFO})	-0.5 ≤ I_O ≤ 0.5mA	1.9	2	2.1	V
Unity Gain Bandwidth*	R_{IN} = 2k	4	5		MHz
Oscillator Section					
Nominal Frequency*		1.0	1.5	2.0	MHz
dF/dIosc*	100 ≤ I_{VFO} ≤ 500μA	2	3	4	GHz/A

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications apply for –55°C ≤ T_A ≤ 125°C for the UC1860, -25° ≤ T_A ≤ 85°C for the UC2860, 0 ≤ T_A ≤ 70°C for the UC3860, V_{CC} = 12V, C_{VFO} = 330pF, I_{VFO} = 0.5mA, C = 330pF, and R = 2.7k, T_A = T_J.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section (cont'd)					
Trig in Threshold		1.0	1.4	1.8	V
Trig in Open Circuit Voltage		0.7	0.9	1.1	V
Trig in Delta (V_{TH}-V_{OC})		0.3	0.5	0.7	V
Trig in Input Resistance	dV $_{TRIG}$ = V_{OC} to V_{TH}	5	12	25	kΩ
Minimum Trig in Pulse Width*			3	10	ns
Osc. Disable Threshold		1.0	1.4	1.8	V
One Shot Timer					
On Time*		150	200	250	ns
Clamp Frequency*	I_{VFO} = 1.5mA	2.8	3.7	4.6	MHz
Dead Time*	I_{VFO} =1.5mA	35	70	100	ns
Output Stage					
Output Low Saturation	20mA		0.2	0.4	V
	200mA		0.5	2.2	V
Output High Saturation	–20mA		1.5	2.0	V
	–200mA		1.7	2.5	V
Rise/Fall Time*	C_{LOAD} = 1nF		15	30	ns
UVLO Low Saturation	20mA		0.8	1.5	V
Output Mode Low Input				0.4	V
Output Mode High Input		2.0			V
Under Voltage Lockout Section					
V_{CC} Comparator Threshold	On	16	17.3	18.5	V
	Off	9.5	10.5	12	V
UVLO Comparator Threshold	On	3.6	4.2	4.8	V
	Hysteresis	0.2	0.4	0.6	V
UVLO Input Resistance	UVLO = 4/V_{CC} = 8	10	23	50	kΩ
V_{REF} Comparator Threshold	V_{CC} = UVLO = V_{REF}		4.5	4.9	V
Supply Current					
I_{CC}	V_{CC} = 12V, V_{OSC} DSBL = 3V		30	40	mA
I_{START}	UVLO pin open V_{CC} = V_{CC} (on) -0.3V		0.3	0.5	mA
Fault Comparator					
Input Offset Voltage	–0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Propagation Delay To Output*	±50mV input		100	150	ns
Uncommitted Comparator					
Input Offset Voltage	–0.3 ≤ V_{CM} ≤ 3V		2	10	mV
Input Bias Current	V_{CM} = 0V		100	200	µA
Input Offset Current	V_{CM} = 0V		10	30	µA
Output Low Voltage	I_O = 2mA		0.3	0.5	V
Propagation Delay To Sat*	±50mV input, 2.5k load to 5V		50	100	ns
Soft Start/Restart Control Section					
Saturation Voltage (2 pins)	I_{SINK} = 100µA		0.2	0.5	V
Charge Current (2 pins)		2	5	10	µA
Restart Delay Threshold		2.8	3.0	3.2	V

**Guaranteed by design but not 100% tested.*

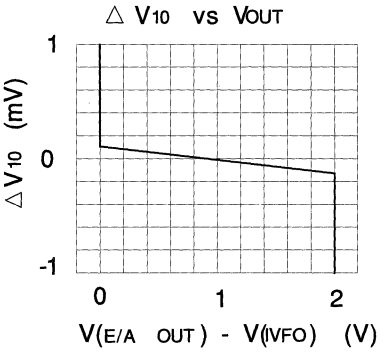
ERROR AMPLIFIER

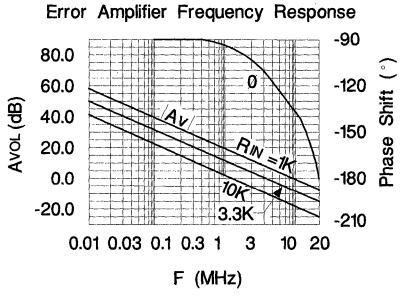
The error amplifier is a high gain, low offset, high bandwidth design with precise limits on its output swing. The bandwidth of the amplifier is externally determined by the resistance seen at the inverting input. Unity gain bandwidth is approximately:

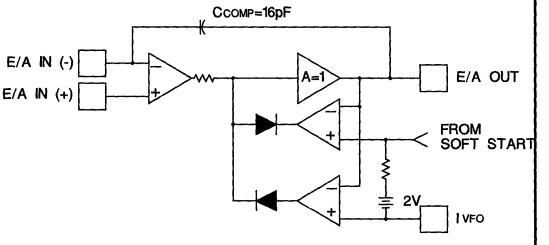
Frequency (0dB) = $1/(2\pi \bullet R_{IN}(-) \bullet C_{COMP})$

The input common mode range of the amplifier is from 2.8 to 4.5V. As long as one pin is within this range, the other can go as low as zero.

The output swing with respect to the IVFO pin is limited from zero to 2V. Note that pulling Sft Strt (soft start) low will lower the reference of the upper clamp. The lower clamp, however, will dominate should the upper clamp reference drop below the lower reference.





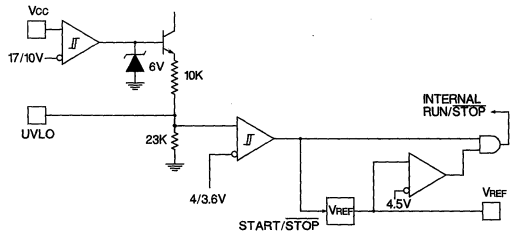


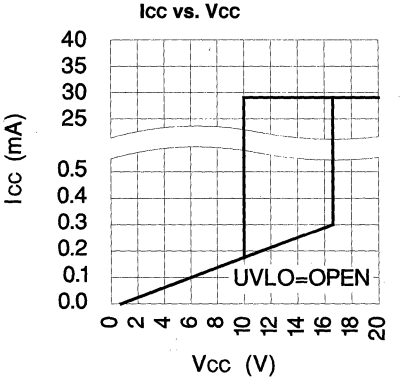
UNDER VOLTAGE LOCKOUT SECTION

The under voltage lockout consists of three comparators that monitor VCC, UVLO and VREF. The VREF comparator makes sure that the reference voltage is sufficiently high before operation begins. When the UVLO comparator is low, the outputs are driven low, the fault latch is reset, the soft start pin is discharged, and the toggle flip-flop is loaded for output A.

The VCC comparator is used for off-line applications by leaving the UVLO pin open. In this application the supply current is typically less than 0.3mA during start-up.

The UVLO comparator is used for DC to DC applications or to gate the chip on and off. To utilize its hysteretic threshold by an external resistive divider, the internal impedance of the pin must be accounted for. To run from a 5V external supply, UVLO, VCC, and VREF are tied together.





VARIABLE FREQUENCY OSCILLATOR

The VFO block is controlled through 4 pins: C_{VFO}, I_{VFO}, Osc Dsbl (oscillator disable), and Trig (trigger input). Oscillator frequency is approximately:

$$Frequency = I_{VFO}\,(C_{VFO} \bullet 1V)$$

With a fixed capacitor and low voltage applied to Trig and Osc Dsbl, frequency is linearly modulated by varying the current into the I_{VFO} pin.

The Trig and Osc Dsbl inputs are used to modify VFO operation. If Osc Dsbl is held high, the oscillator will complete the current cycle but wait until Osc Dsbl is returned low to initiate a new cycle. If a pulse is applied to Trig during a cycle, the oscillator will immediately initiate a new cycle. Osc Dsbl has priority over Trig, but if a trigger pulse is received while Osc Dsbl is high, the VFO will remember the trigger pulse and start a new cycle as soon as Osc Dsbl goes low.

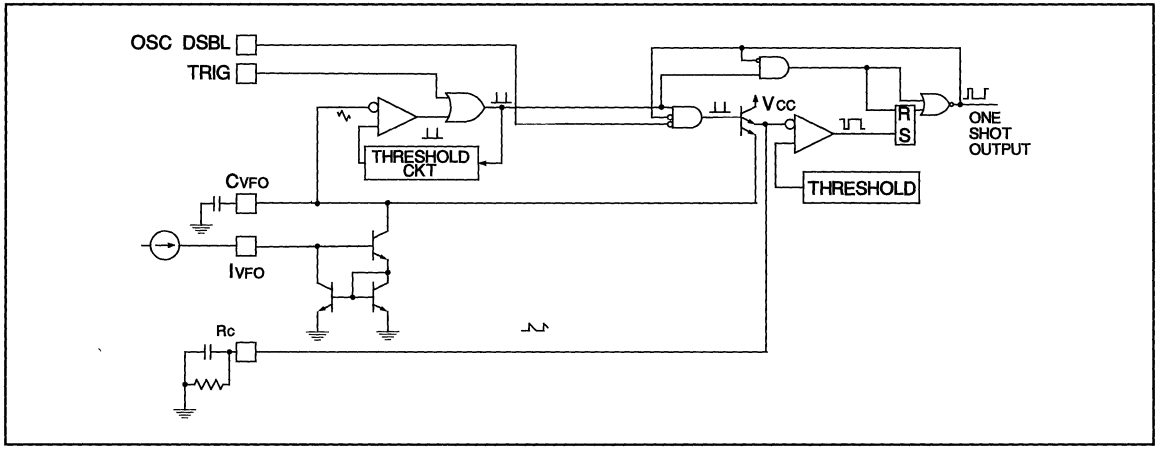
Normally low trigger pulses are used to synchronize the oscillator to a faster clock. Normally high trigger pulses can also be used to synchronize to a slower clock.

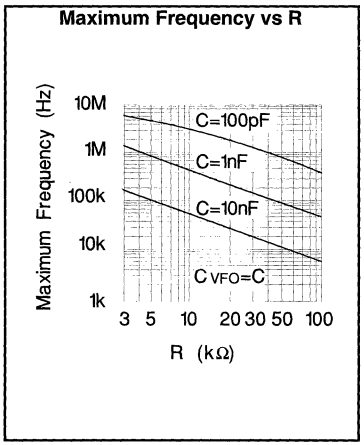
ONE SHOT TIMER

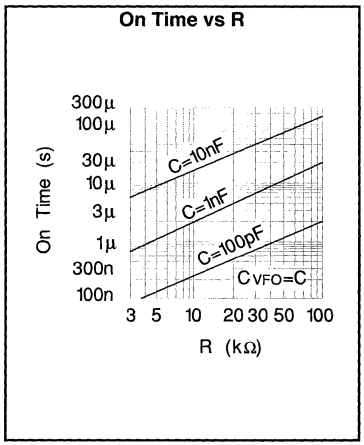
The one shot timer performs three functions and is programmed by the RC pin. The first function is to control output driver pulse width. Secondly, it clocks the toggle flip-flop. Thirdly, it establishes the maximum allowable frequency for the VFO. One shot operation is initiated at the beginning of each oscillator cycle. The RC pin, programmed by an external resistor and capacitor to ground, is charged to approximately 4.3V and then allowed to discharge. The lower threshold is approximately 80% of the peak. On time is approximately:

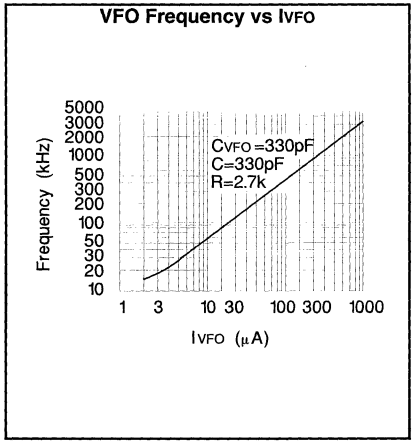
$$t_{ON} = 0.2 \bullet R \bullet C.$$

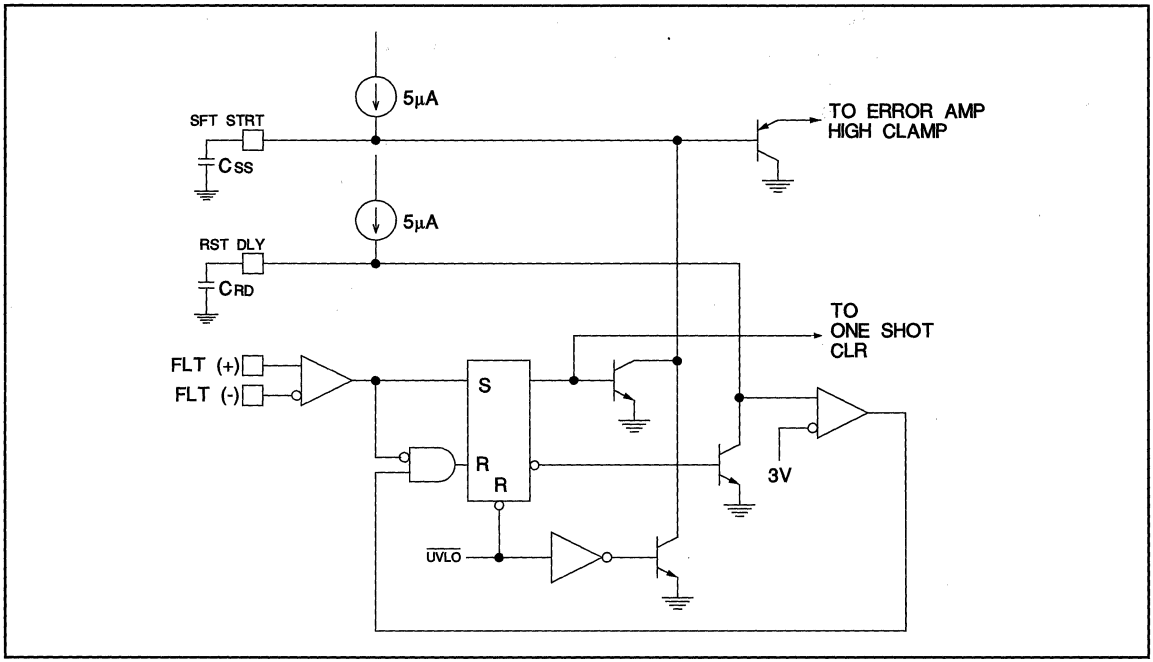
After crossing the lower threshold, the resistor continues to discharge the capacitor to approximately 3V, where it waits for the next oscillator cycle.











FAULT MANAGEMENT SECTION

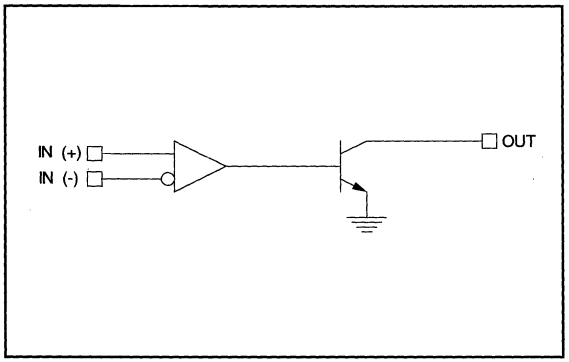
During UVLO, the fault management section is initialized. The latch is reset, and both Sft Strt (soft start) and Rst Dly (restart delay) are pulled low. When Sft Strt is low, it lowers the upper clamp of the error amplifier. As Sft Strt increases in voltage, the upper clamp increases from a value equal to the lower clamp until it is 2V more positive. A capacitor to ground from the Sft Strt pin will control the start rate.

UNCOMMITTED COMPARATOR

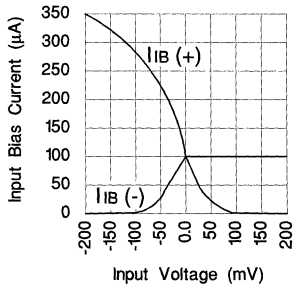
The uncommitted comparator, biased from the reference voltage, operates independently from the rest of the chip. The open collector output is capable of sinking 2mA. The inputs are valid in the common mode range of -0.3 to 3.0V. As long as one of the inputs is within this range, the other can be as high as 5V.

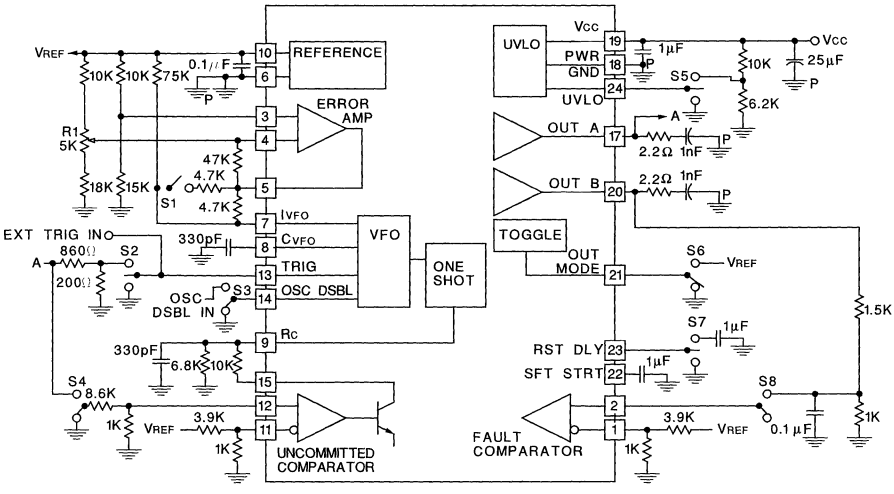
The high speed fault comparator will work over the input common mode range of -0.3 to 3.0V. When a fault is sensed, the one shot is immediately terminated, Sft Strt is pulled low, and Rst Dly is allowed to go high. Three modes of fault disposition can easily be implemented. If Rst Dly is externally held low, then a detected fault will shut the chip down permanently. If the Rst Dly pin is left open, a fault will simply cause an interruption of operation. If a capacitor is connected from Rst Dly to ground, then hic-up operation is implemented. The hic-up time is:

$$t_{OFF} = 600\,k\,\Omega \bullet C \bullet (Rst\,Dly).$$



Input Bias Current Input Voltage





OPEN LOOP LABORATORY TEST FIXTURE

The open loop laboratory test fixture is designed to allow familiarization with the operating characteristics of the UC3860. Note the pin numbers apply to the DIP.

To get started, preset all the options as follows:

Adjust the error amplifier variable resistor pot (R1) so the wiper is at a high potential.

Open the I_{VFO} resistor switch (S1).

Throw the Trig switch (S2) to ground.

Throw the Osc Dsbl switch (S3) to ground.

Throw the uncommitted comparator switch (S4) to ground.

Throw the UVLO switch (S5) to the resistive divider.

Throw the Out Mode switch (S6) to ground.

Open the restart delay switch (S7).

Throw the fault switch (S8)to ground.

In this configuration, the chip will operate for V_{CC} greater than 12V. Adjustment of the following controls allows examination of specific features.

R1 adjusts the output of the error amp. Notice the voltage at pin 5 is limited from 0V to 2V above the voltage at pin 7.

S1 changes the error amp output to VFO gain. With S1 open, the maximum frequency is determined by the error amp output. With S1 closed, the one shot will set the maximum frequency.

S2 demonstrates the trigger. An external trigger signal may be applied. When the switch is set to the resistive divider, the chip will operate in consecutive mode (ie: A,B, off...)

S3 allows input of an external logic signal to disable the oscillator.

S4 demonstrates the uncommitted comparator. When set to output A, the comparator will accelerate the discharge of pin 9, shortening the output pulse.

S5 shorted to ground will disable the chip and the outputs will be low. If the switch is open, the V_{CC} start and stop thresholds are 17V and 10V. Switched to the resistive divider, the thresholds are approximately 12V and 10V.

S6 sets the mode of the toggle flip-flop. When grounded, the outputs operate alternately. Switched to 5V, the outputs switch in unison. (Note: If S6 and S2 are set for unison operation and triggered consecutive outputs, the chip will free run at the maximum frequency determined by the one shot.)

S7 open allows the chip to restart immediately after a fault sense has been removed. When grounded, it causes the chip to latch off indefinitely. This state can be reset by UVLO, V_{CC}, or opening the switch. Connected to 1µF programs a hic-up delay time of 600 ms.

S8 allows the simulation of a fault state. When flipped to the RC network, the comparator monitors scaled average voltage of output B. Adjusting frequency will cause the comparator to sense a 'fault' and the chip will enter fault sequence.

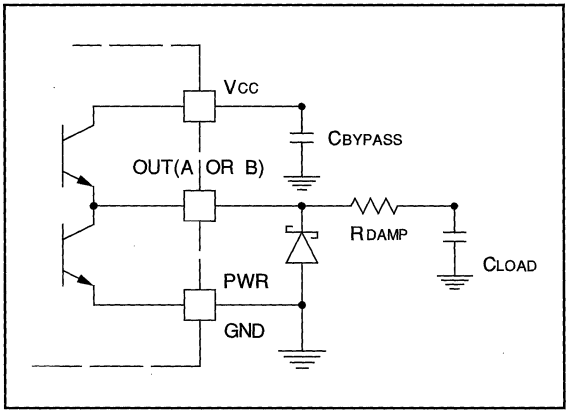
OUTPUT STAGE

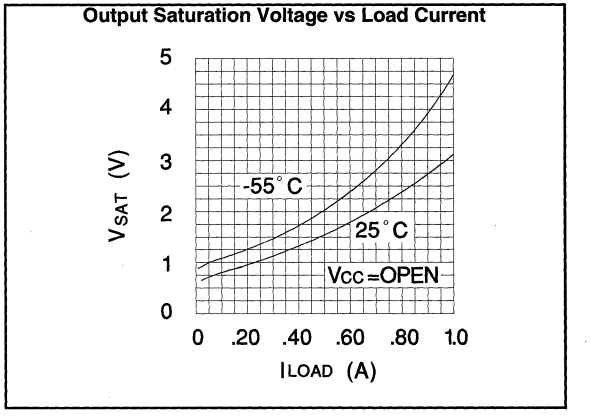
The two totem pole output stages can be programmed by Mode to operate alternately or in unison. When Mode is low the outputs alternate. During UVLO, the outputs are low.

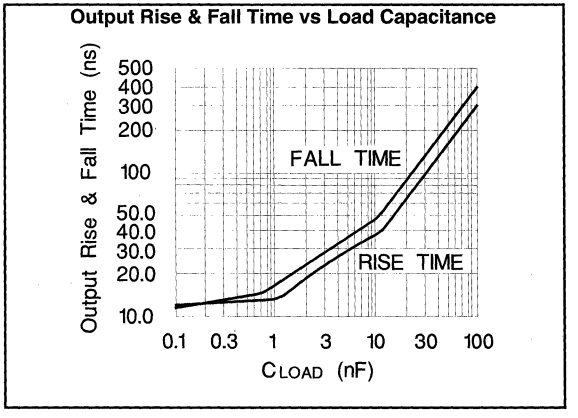
Extreme care needs to be exercised in the application of these outputs. Each output can source and sink transient currents of 2A or more and is designed for high values of dI/dt. This dictates the use of a ground plane, shielded interconnect cables, Schottky diode clamps from the output pins to Pwr Gnd (power ground), and some series resistance to provide damping. Pwr Gnd should not exceed ±0.2V from signal ground.

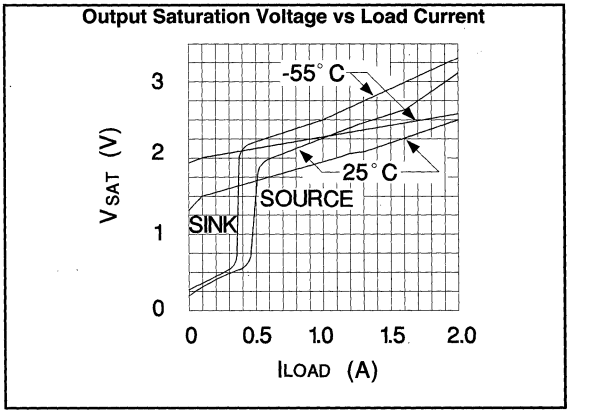
BYPASS NOTE

The reference should be bypassed with a 0.1µF ceramic capacitor from the VREF pin directly to the ground plane near the Signal Ground pin. The timing capacitors on CVFO and RC should be treated likewise. VCC, however, should be bypassed with a ceramic capacitor from the VCC pin to the section of ground plane that is connected to Power Ground. Any required bulk reservoir capacitor should parallel this one. The two ground plane sections can then be joined at a single point to optimize noise rejection and minimize DC drops.









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UNITRODE

application INFO available

UC1861-1868
UC2861-2868
UC3861-3868

Resonant-Mode Power Supply Controllers

FEATURES

- Controls Zero Current Switched (ZCS) or Zero Voltage Switched (ZVS) Quasi-Resonant Converters
- Zero-Crossing Terminated One-Shot Timer
- Precision 1%, Soft-Started 5V Reference
- Programmable Restart Delay Following Fault
- Voltage-Controlled Oscillator (VCO) with Programmable Minimum and Maximum Frequencies from 10kHz to 1MHz
- Low Start-Up Current (150µA typical)
- Dual 1 Amp Peak FET Drivers
- UVLO Option for Off-Line or DC/DC Applications

DESCRIPTION

The UC1861-1868 family of ICs is optimized for the control of Zero Current Switched and Zero Voltage Switched quasi-resonant converters. Differences between members of this device family result from the various combinations of UVLO thresholds and output options. Additionally, the one-shot pulse steering logic is configured to program either on-time for ZCS systems (UC1865-1868), or off-time for ZVS applications (UC1861-1864).

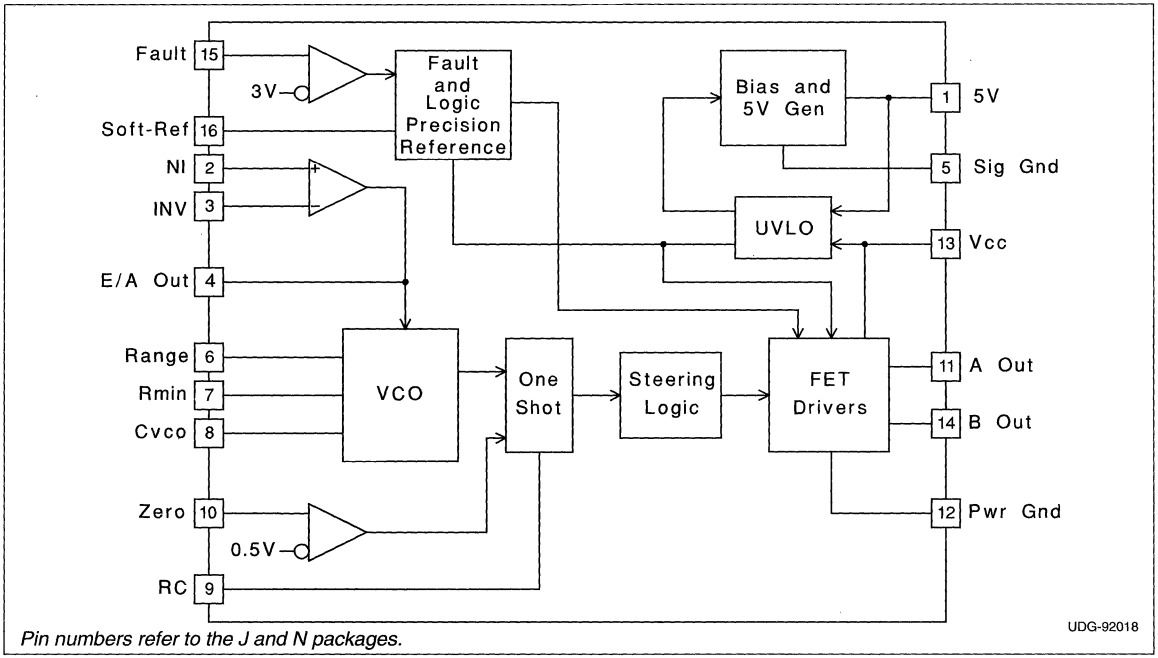
The primary control blocks implemented include an error amplifier to compensate the overall system loop and to drive a voltage controlled oscillator (VCO), featuring programmable minimum and maximum frequencies. Triggered by the VCO, the one-shot generates pulses of a programmed maximum width, which can be modulated by the Zero Detection comparator. This circuit facilitates "true" zero current or voltage switching over various line, load, and temperature changes, and is also able to accommodate the resonant components' initial tolerances.

Under-Voltage Lockout is incorporated to facilitate safe starts upon power-up. The supply current during the under-voltage lockout period is typically less than 150µA, and the outputs are actively forced to the low state.

(continued)

Device	1861	1862	1863	1864	1865	1866	1867	1868
UVLO	16.5/10.5	16.5/10.5	36014	36014	16.5/10.5	16.5/10.5	36014	36014
Outputs	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel	Alternating	Parallel
"Fixed"	Off Time	Off Time	Off Time	Off Time	On Time	On Time	On Time	On Time

BLOCK DIAGRAM



Pin numbers refer to the J and N packages.

DESCRIPTION (cont.)

UVLO thresholds for the UC1861/62/65/66 are 16.5V (ON) and 10.5V (OFF), whereas the UC1863/64/67/68 thresholds are 8V (ON) and 7V (OFF). After V_{CC} exceeds the UVLO threshold, a 5V generator is enabled which provides bias for the internal circuits and up to 10mA for external usage.

A Fault comparator serves to detect fault conditions and set a latch while forcing the output drivers low. The Soft-Ref pin serves three functions: providing soft start, restart delay, and the internal system reference.

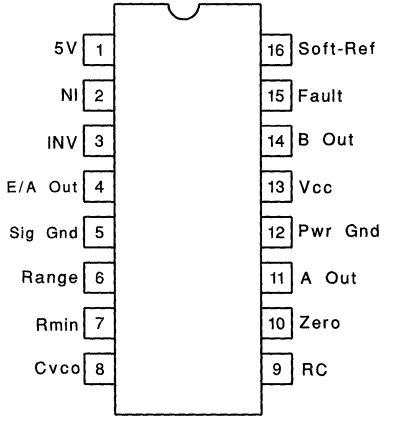
Each device features dual 1 Amp peak totem pole output drivers for direct interface to power MOSFETS. The outputs are programmed to alternate in the UC1861/63/65/67 devices. The UC1862/64/66/68 outputs operate in unison alllowing a 2 Amp peak current.

ABSOLUTE MAXIMUM RATINGS

V_{CC} 22V
Output Current
  Source or Sink (Pins 11 & 14) 0.5A
  DC Pulse (0.5µs) 1.5A
Power Ground Voltage ..... ±0.2V
Inputs (Pins 2, 3, 10, & 15) ..... –0.4 to 7V
Error Amp Output Current ..... ±2mA
Power Dissipation 1W
Junction Temperature (Operating) ..... 150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

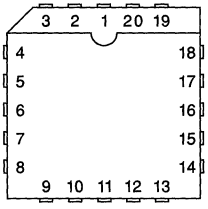
All voltages are with respect to signal ground and all currents are positive into the specified terminal. Pin numbers refer to the J and N packages. Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

DIL-16, SOIC-16 (Top View)
J or N, DW Packages



CONNNECTION DIAGRAMS

PLCC-20 & LCC-20 (Top View)
Q & L Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
Soft Ref	1
5V	2
NI	3
INV	4
E/A Out	5
Sig Gnd	6
Range	7
RMIN	8
CVCO	9
RC	10
Zero	11
NC	12
NC	13
A Out	14
Pwr Gnd	15
Pwr Gnd	16
VCC	17
B Out	18
NC	19

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for $-55°C \le T_A \le 125°C$ for the UC186x, $-25°C \le T_A \le 85°C$ for the UC286x, and $0°C \le T_A \le 70°C$ for the UC386x, V_{CC}=12V, C_{VCO}=1nF, Range=7.15k, R_{MIN}=86.6k, C=200pF, R=4.02k, and Csr=0.1µF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Generator					
Output Voltage	12V ≤ Vcc ≤ 20V, –10mA ≤ Io ≤ 0mA	4.8	5.0	5.2	V
Short Circuit Current	Vo = 0V	–150		–15	mA
Soft-Reference					
Restart Delay Current	V = 2V	10	20	35	µA
Soft Start Current	V = 2V	–650	–500	–350	µA
Reference Voltage	T_J = 25°C, Io = 0A	4.95	5.00	5.05	V
	12V ≤ Vcc ≤ 20V, –200µA ≤ Io ≤ 200µA	4.85		5.15	V
Line Regulation	12V ≤ Vcc ≤ 20V		2	20	mV
Load Regulation	–200µA ≤ Io ≤ 200µA		10	30	mV
Error Amplifier (Note 3)					
Input Offset Voltage	V_{CM} = 5V, Vo = 2V, Io = 0A	–10		10	mV
Input Bias Current	V_{CM} = 0V	–2.0	–0.3		µA
Voltage Gain	Vcm = 5V, 0.5V ≤ Vo ≤ 3.7V, Io = 0A	70	100		dB
Power Supply Rejection Ratio	Vcm = 5V, Vo = 2V, 12V ≤ Vcc ≤ 20V	70	100		dB
Error Amplifier (Note 3) (cont.)					
Common Mode Rejection Ratio	0V ≤ Vcm ≤ 6V, Vo = 2V	65	100		dB
V_{OUT} Low	V_{ID} = –100mV, Io = 200µA		0.17	0.25	V
V_{OUT} High	V_{ID} = 100mV, Io = –200µA	3.9	4.2		V
Unity Gain Bandwidth	(Note 4)	0.5	0.8		MHz
Voltage Controlled Oscillator					
Maximum Frequency	V_{ID} (Error Amp) = 100mV, T_J = 25°C	450	500	550	kHz
	V_{ID} (Error Amp) = 100mV	425		575	kHz
Minimum Frequency	V_{ID} (Error Amp) = –100mV, T_J = 25°C	45	50	55	kHz
	V_{ID} (Error Amp) = –100mV	42		58	kHz
One Shot					
Zero Comparator Vth		0.45	0.50	0.55	V
Propagation Delay	(Note 4)		120	200	ns
Maximum Pulse Width	V_{ZERO} = 1V	850	1000	1150	ns
Maximum to Minimum Pulse Width Ratio	V_{ZERO} = 0V UCx861 – UCx864	2.5	4	5.5	
	V_{ZERO} = 0V UCx865 – UCx868. –55°C to +85°C	4	5.5	7	
	V_{ZERO} = 0V UCx865 – UCx868, +125°C	3.8	5.5	7	
Output Stage					
Rise and Fall Time	C_{LOAD} = 1nF (Note 4)		25	45	ns
Output Low Saturation	Io = 20mA		0.2	0.5	V
	Io = 200mA		0.5	2.2	V
Output High Saturation	Io = –200mA, down from Vcc		1.7	2.5	V
UVLO Low Saturation	Io = 20mA		0.8	1.5	V
Fault Comparator					
Fault Comparator Vth		2.85	3.00	3.15	V
Delay to Output	(Note 4) (Note 5)		100	200	ns

ELECTRICAL CHARACTERISTICS Unless otherwise stated, all specifications apply for –55°C≤TA≤125°C for the UC186x, –25°C≤TA≤85°C for the UC286x, and 0°C≤TA≤70°C for the UC386x, VCC=12V, CVCO=1nF, Range=7.15k, RMIN=86.6k, C=200pF, R=4.02k, and CSR=0.1µF. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO					
Vcc Turn-on Threshold	UCx861, UCx862, UCx865, UCx866	15	16.5	18	V
	UCx863, UCx864, UCx867, UCx868	7	8.0	9	V
Vcc Turn-off Threshold	UCx861, UCx862, UCx865, UCx866	9.5	10.5	11.5	V
	UCx863, UCx864, UCx867, UCx868	6	7.0	8	V
Icc Start	VCC = VCC(on) – 0.3V		150	300	µA
Icc Run	VID = 100mV		25	32	mA

Note 1: Currents are defined as positive into the pin.
Note 2: Pulse measurement techniques are used to insure that TJ = TA.
Note 3: VID = V(NI) – V(INV).
Note 4: This parameter is not 100% tested in production but guaranteed by design.
Note 5: Vi = 0 to 4V tr(Vi) ≤ 10ns tpd = t(Vo = 6V) – t(Vi = 3V)

APPLICATION INFORMATION

UVLO & 5V GENERATOR (See Figure 1): When power is applied to the chip and Vcc is less than the upper UVLO threshold, Icc will be less than 300µA, the 5V generator will be off, and the outputs will be actively held low.

When Vcc exceeds the upper UVLO threshold, the 5V generator turns on. Until the 5V pin exceeds 4.9V, the outputs will still remain low.

The 5V pin should be bypassed to signal ground with a 0.1µF capacitor. The capacitor should have low equivalent series resistance and inductance.

FAULT AND SOFT-REFERENCE (See Figure 1): The Soft-Ref pin serves three functions: system reference, restart delay, and soft-start. Designed to source or sink 200µA, this pin should be used as the input reference for the error amplifier circuit. This pin requires a bypass capacitor of at least 0.1µF. This yields a minimum soft-start time of 1ms.

Under-Voltage Lockout sets both the fault and restart delay latches. This holds the outputs low and discharges the Soft-Ref pin. After UVLO, the fault latch is reset by the low voltage on the Soft-Ref pin. The reset fault latch resets the delay latch and Soft-Ref charges via the 0.5mA current source.

The fault pin is input to a high speed comparator with a threshold of 3V. In the event of a detected fault, the fault latch is set and the outputs are driven low. If Soft-Ref is above 4V, the delay latch is set. Restart delay is timed as Soft-Ref is discharged by 20µA. When Soft-Ref is fully discharged, the fault latch is reset if the fault input signal is low. The Fault pin can be used as a system shutdown pin.

If a fault is detected during soft-start, the fault latch is set and the outputs are driven low. The delay latch will remain reset until Soft-Ref charges to 4V. This sets the delay latch, and restart delay is timed. Note that restart delay for a single fault event is longer than for recurring faults since Soft-Ref must be discharged from 5V instead of 4V.

The restart delay to soft-start time ratio is 24:1 for a fault occurring during normal operation and 19:1 for faults occurring during soft-start. Shorter ratios can be programmed down to a limit of approximately 3:1 by the addition of a 20kΩ or larger resistor from Soft-Ref to ground.

A 100kΩ resistor from Soft-Ref to 5V will have the effect of permanent shut down after a fault since the internal 20µA current source can't pull Soft-Ref low. This feature can be used to require recycling Vcc after a fault. Care must be taken to insure Soft-Ref is indeed low at start up, or the fault latch will never be reset.

APPLICATION INFORMATION

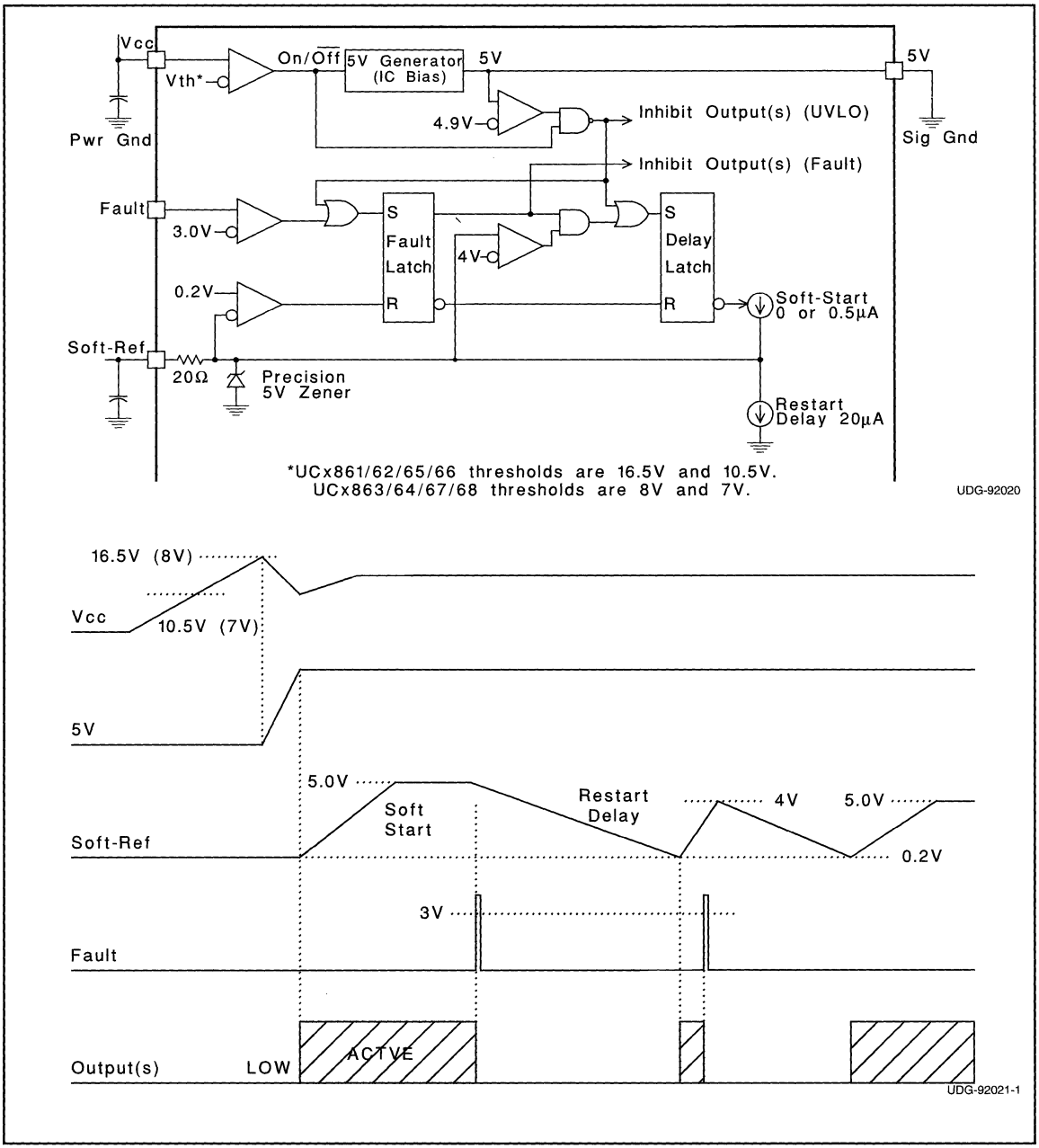
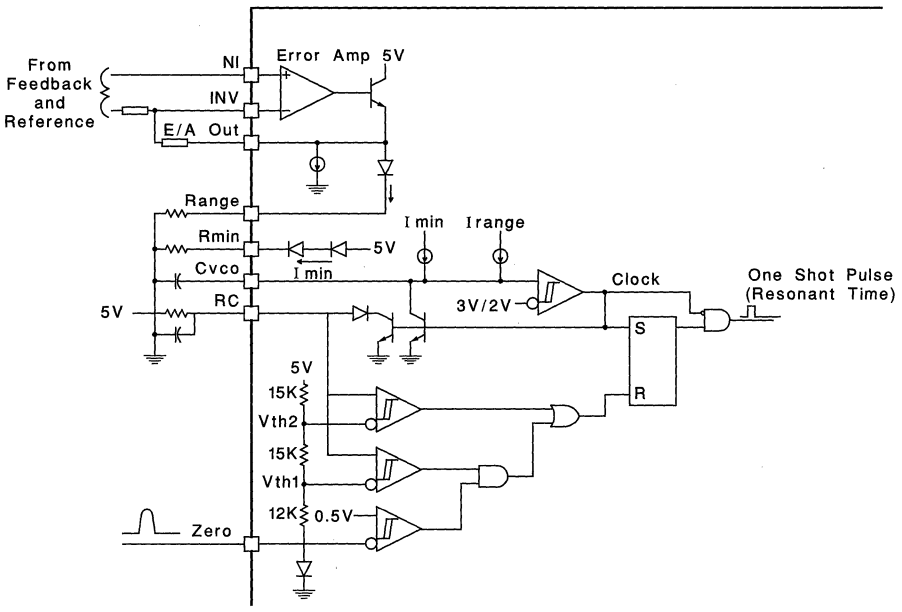


Figure 1. UVLO, 5V, fault and soft-ref.



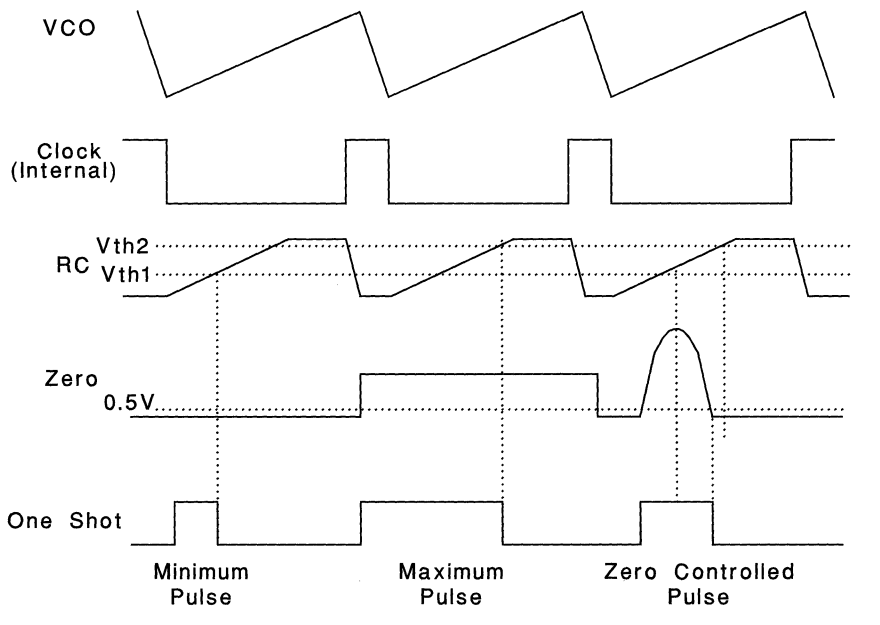


Figure 2. Error Amp, Voltage Controlled Oscillator, and One Shot

APPLICATION INFORMATION

Minimum oscillator frequency is set by Rmin and Cvco. The minimum frequency is approximately given by the equation:

$$F_{MIN} \cong \frac{4.3}{R_{MIN} \bullet C_{VCO}}$$

Maximum oscillator frequency is set by Rmin, Range & Cvco. The maximum frequency is approximately given by the equation:

$$F_{MAX} \cong \frac{3.3}{(R_{MIN} \,//\, Range) \bullet C_{VCO}}$$

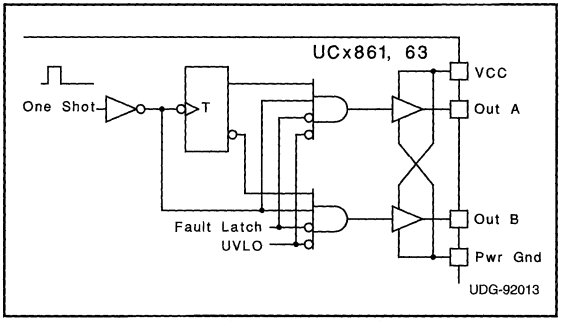
The Error Amplifier directly controls the oscillator frequency. E/A output low corresponds to minimum frequency and output high corresponds to maximum frequency. At the end of each oscillator cycle, the RC pin is discharged to one diode drop above ground. At the beginning of the oscillator cycle, V(RC) is less than Vth1 and so the output of the zero detect comparator is ignored. After V(RC) exceeds Vth1, the one shot pulse will be terminated as soon as the zero pin falls below 0.5V or V(RC) exceeds Vth2. The minimum one shot pulse width is approximately given by the equation:

$$Tpw(min) \cong 0.3 \bullet R \bullet C.$$

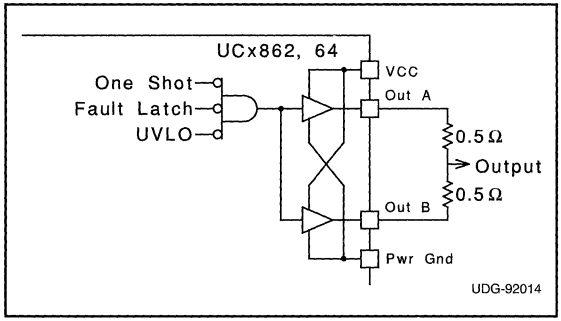
The maximum pulse width is approximately given by:

$$Tpw(max) \cong 1.2 \bullet R \bullet C.$$

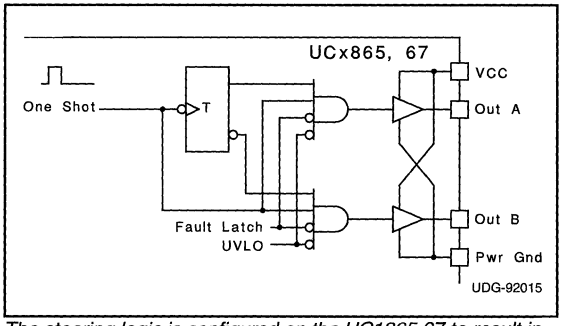
STEERING LOGIC



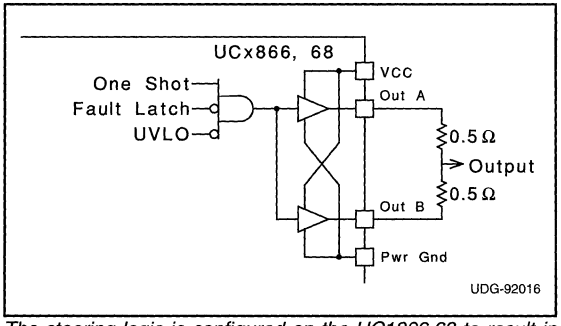
The steering logic is configured on the UC1861,63 to result in dual non-overlapping square waves at outputs A & B. This is suited to drive dual switch ZVS systems.



The steering logic is configured on the UC1862,64 to result in inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZVS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.



The steering logic is configured on the UC1865,67 to result in alternating pulse trains at outputs A & B. This is suited to drive dual switch ZCS systems.



The steering logic is configured on the UC1866,68 to result in non-inverted pulse trains occurring identically at both output pins. This is suited to drive single switch ZCS systems. Both outputs are available to drive the same MOSFET gate. It is advisable to join the pins with 0.5 ohm resistors.

APPLICATION INFORMATION (cont.)

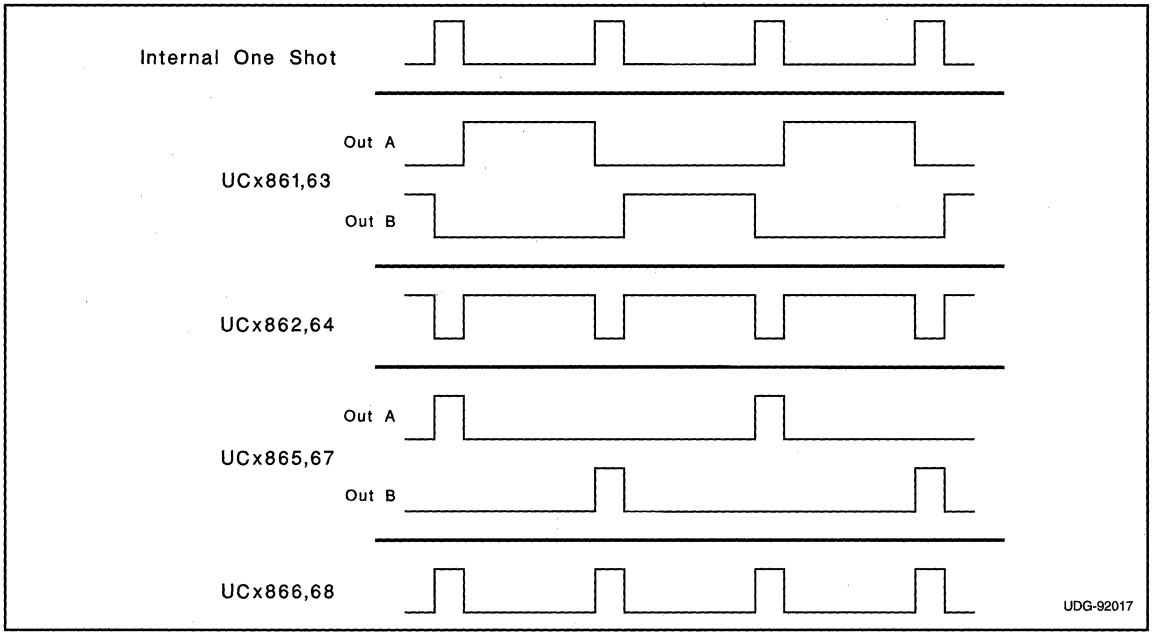


Figure 3. Current waveforms.

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Phase Shift Resonant Controller

FEATURES

- Zero to 100% Duty Cycle Control
- Programmable Output Turn-On Delay
- Compatible with Voltage or Current Mode Topologies
- Practical Operation at Switching Frequencies to 1MHz
- Four 2A Totem Pole Outputs
- 10MHz Error Amplifier
- Undervoltage Lockout
- Low Startup Current –150µA
- Outputs Active Low During UVLO
- Soft-Start Control
- Latched Over-Current Comparator With Full Cycle Restart
- Trimmed Reference

DESCRIPTION

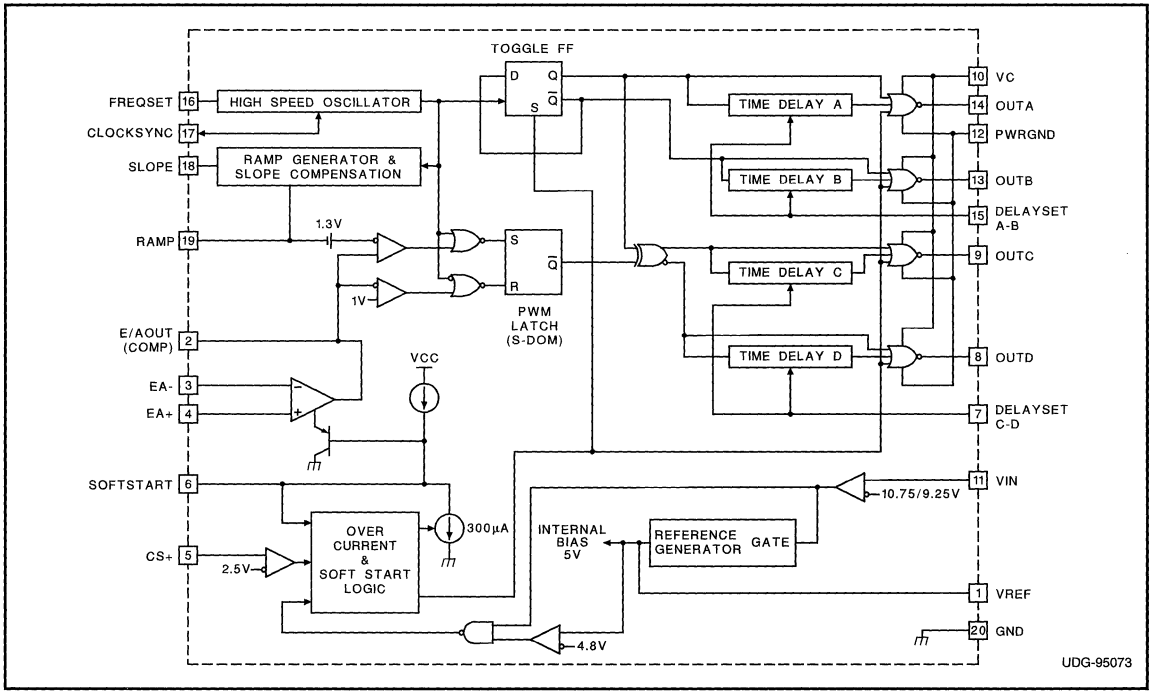
The UC1875 family of integrated circuits implements control of a bridge power stage by phase-shifting the switching of one half-bridge with respect to the other, allowing constant frequency pulse-width modulation in combination with resonant, zero-voltage switching for high efficiency performance at high frequencies. This family of circuits may be configured to provide control in either voltage or current mode operation, with a separate over-current shutdown for fast fault protection.

A programmable time delay is provided to insert a dead-time at the turn-on of each output stage. This delay, providing time to allow the resonant switching action, is independently controllable for each output pair (A-B, C-D).

With the oscillator capable of operation at frequencies in excess of 2MHz, overall switching frequencies to 1MHz are practical. In addition to the standard free running mode, with the CLOCKSYNC pin, the user may configure these devices to accept an external clock synchronization signal, or may lock together up to 5 units with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout which maintains all outputs in an active-low state until the supply reaches a 10.75V threshold. 1.5V hysteresis is built in for reliable, boot-strapped chip supply. Over-current protection is provided, and will latch the outputs in the OFF state within 70nsec of a fault. The current-fault circuitry implements full-cycle restart operation. **(continued)**

BLOCK DIAGRAM



DESCRIPTION (cont.)

Additional features include an error amplifier with bandwidth in excess of 7MHz, a 5V reference, provisions for soft-starting, and flexible ramp generation and slope compensation circuitry.

These devices are available in 20-pin DIP, 28-pin "bat-wing" SOIC and 28 lead power PLCC plastic packages for operation over both 0°C to 70°C and –25°C to +85°C temperature ranges; and in hermetically sealed cerdip, and surface mount packages for –55°C to +125°C operation.

Device	UVLO Turn-On	UVLO Turn-Off	Delay Set
UC1875	10.75	9.25V	Yes
UC1876	15.25V	9.25V	Yes
UC1877	10.75V	9.25V	No
UC1878	15.25V	9.25V	No

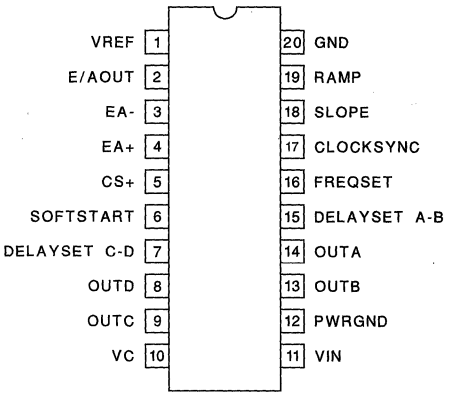
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VIN) 20V
Output Current, Source or Sink
DC 0.5A
Pulse (0.5µs) 3A
Analog I/Os
(Pins 1, 2, 3, 4, 5, 6, 7, 15, 16, 17, 18, 19) . . . . –0.3 to 5.3V
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

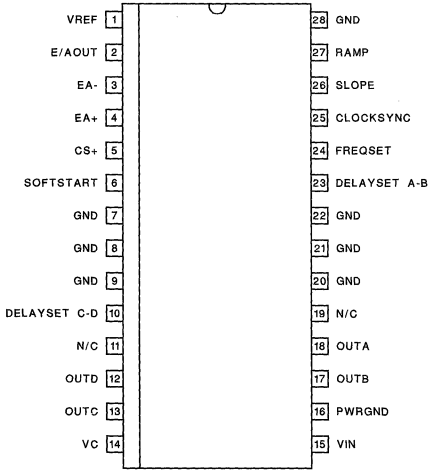
Note: Pin references are to 20 pin packages. All voltages are with respect to ground. Currents are positive into, negative out of, device terminals. Consult Unitrode databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

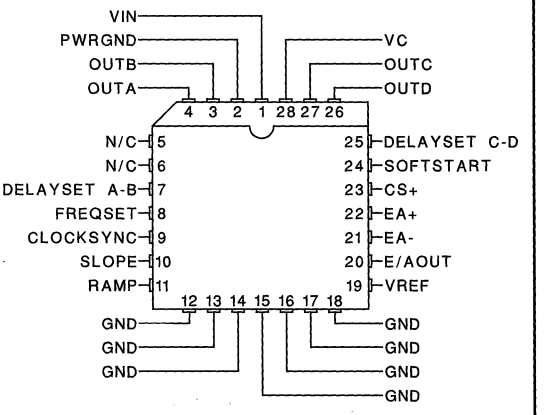
Dil-20 (Top View)
J or N Package



SOIC-28, (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, –55°C < T_A < 125°C for the UC1875/6/7/8, –25°C < T_A < 85°C for the UC2875/6/7/8 and 0°C < T_A < 70°C for the UC3875/6/7/8, VC = VIN = 12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAYSET\ A\text{-}B}$ = $C_{DELAYSET\ C\text{-}D}$ = 0.01μF, $I_{DELAYSET\ A\text{-}B}$ = $I_{DELAYSET\ C\text{-}D}$ = –500μA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start Threshold	UC1875/UC1877		10.75	11.75	V
	UC1876/UC1878		15.25		V
UVLO Hysteresis	UC1875/UC1877	0.5	1.25	2.0	V
	UC1876/UC1878		6.0		V
Supply Current					
I_{IN} Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		150	600	μA
I_C Startup	VIN = 8V, VC = 20V, R_{SLOPE} open, I_{DELAY} = 0		10	100	μA
I_{IN}			30	40	mA
I_C			15	30	mA
Voltage Reference					
Output Voltage	T_J = +25°C	4.92	5	5.08	V
Line Regulation	11 < VIN < 20V		1	10	mV
Load Regulation	I_{VREF} = –10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.9		5.1	V
Noise Voltage	10Hz to 10kHz		50		μVrms
Long Term Stability	T_J = 125°C, 1000 hours		2.5		mV
Short Circuit Current	VREF = 0V, T_J = 25°C		60		mA
Error Amplifier					
Offset Voltage			5	15	mV
Input Bias Current			0.6	3	μA
AVOL	1V < $V_{E/AOUT}$ < 4V		60	90	dB
CMRR	1.5V < V_{CM} < 5.5V	75	95		dB
PSRR	11V < VIN < 20V	85	100		dB
Output Sink Current	$V_{E/AOUT}$ = 1V	1	2.5		mA
Output Source Current	$V_{E/AOUT}$ = 4V		–1.3	–0.5	mA
Output Voltage High	$I_{E/AOUT}$ = –0.5mA	4	4.7	5	V
Output Voltage Low	$I_{E/AOUT}$ = 1mA	0	0.5	1	V
Unity Gain BW		7	11		MHz
Slew Rate		6	11		V/μsec
PWM Comparator					
Ramp Offset Voltage	T_J = 25°C (Note 3)		1.3		V
Zero Phase Shift Voltage	(Note 4)	0.55	0.9		V
PWM Phase Shift (Note1)	$V_{E/AOUT}$ > (Ramp Peak + Ramp Offset)	98	99.5	102	%
	$V_{E/AOUT}$ < Zero Phase Shift Voltage	0	0.5	2	%
Output Skew (Note 1)	$V_{E/AOUT}$ < 1V		5	±20	nsec
Ramp to Output Delay	UC3875/6/7/8 (Note 6)		65	100	nsec
	UC1875/6/7/8, UC2875/6/7/8 (Note 6)		65	125	nsec
Oscillator					
Initial Accuracy	T_J = 25°C	0.85	1	1.15	MHz
Voltage Stability	11V < VIN < 20V		0.2	2	%
Total Variation	Line, Temperature	0.80		1.20	MHz
Sync Pin Threshold	T_J = 25°C		3.8		V
Clock Out Peak	T_J = 25°C		4.3		V
Clock Out Low	T_J = 25°C		3.3		V
Clock Out Pulse Width	$R_{CLOCKSYNC}$ = 3.9kΩ		30	100	nsec

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, $-55°C < T_A < 125°C$ for the UC1875/6/7/8, $-25°C < T_A < 85°C$ for the UC2875/6/7/8 and $0°C < T_A < 70°C$ for the UC3875/6/7/8, VC = VIN = 12V, $R_{FREQSET}$ = 12kΩ, $C_{FREQSET}$ = 330pF, R_{SLOPE} = 12kΩ, C_{RAMP} = 200pF, $C_{DELAYSET\ A\text{-}B}$ = $C_{DELAYSET\ C\text{-}D}$ = 0.01µF, $I_{DELAYSET\ A\text{-}B}$ = $I_{DELAYSET\ C\text{-}D}$ = −500µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Frequency	$R_{FREQSET}$ = 5kΩ	2			MHz
Ramp Generator/Slope Compensation					
Ramp Current, Minimum	I_{SLOPE} = 10µA, $V_{FREQSET}$ = VREF		−11	−14	µA
Ramp Current, Maximum	I_{SLOPE} = 1mA, $V_{FREQSET}$ = VREF	−0.8	−0.95		mA
Ramp Valley			0		V
Ramp Peak - Clamping Level	$R_{FREQSET}$ = 100kΩ		3.8	4.1	V
Current Limit					
Input Bias	V_{CS}+ = 3V		2	5	µA
Threshold Voltage		2.4	2.5	2.6	V
Delay to Output	UC3875/6/7/8		85	125	nsec
	UC1875/6/7/8, UC2875/6/7/8		85	150	nsec
Soft-Start/Reset Delay					
Charge Current	$V_{SOFTSTART}$ = 0.5V	−20	−9	−3	µA
Discharge Current	$V_{SOFTSTART}$ = 1V	120	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	I_{OUT} = 50mA		0.2	0.4	V
	I_{OUT} = 500mA		1.2	2.6	V
Output High Level	I_{OUT} = −50mA		1.5	2.5	V
	I_{OUT} = −500mA		1.7	2.6	V
Delay Set (UC1875 and UC1876 only)					
Delay Set Voltage	I_{DELAY} = −500µA	2.3	2.4	2.6	V
Delay Time	I_{DELAY} = −250µA (Note 5) (UC3875/6/7/8, UC2875/6/7/8)	150	250	400	nsec
	I_{DELAY} = −250µA (Note 5) (UC1875/6/7/8)	150	250	600	nsec

Note 1: Phase shift percentage (0% = 0°, 100% = 180°) is defined as $\theta = \frac{200}{T}\Phi\%$, *where* θ *is the phase shift, and* Φ *and T are defined in Figure 1. At 0% phase shift,* Φ *is the output skew.*

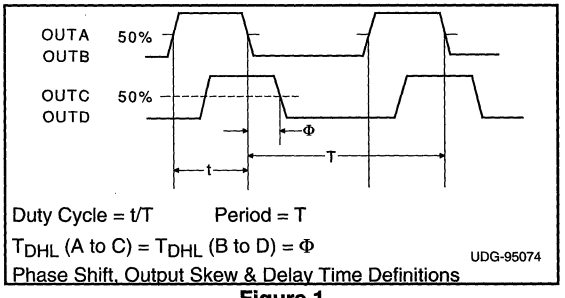
Note 2: Delay time is defined as delay = T (1/2−(duty cycle)), where T is defined in Fig. 1.

Note 3: Ramp offset voltage has a temperature coefficient of about −4mV/°C.

Note 4: Zero phase shift voltage has a temperature coefficient of about −2mV/°C.

Note 5: Delay time can be programmed via resistors from the delay set pins to ground. Delay time $\cong \frac{62.5 \bullet 10^{-12}}{I_{DELAY}}$ *sec. Where* $I_{DELAY} = \frac{Delay\ set\ voltage}{R_{DELAY}}$ *The recommended range for* I_{DELAY} *is* $25\mu A \le I_{DELAY} \le 1mA$

Note 6: Ramp delay to output time is defined in Fig. 2.



Phase Shift, Output Skew & Delay Time Definitions

Figure 1

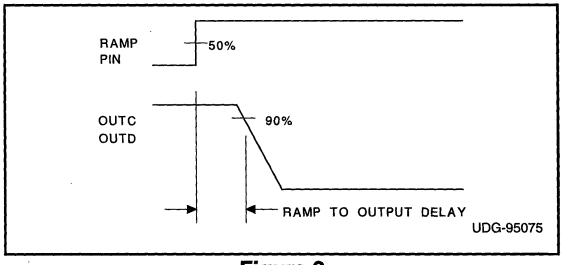


Figure 2

PIN DESCRIPTIONS

CLOCKSYNC (bi-directional clock and synchronization pin): Used as an output, this pin provides a clock signal. As an input, this pin provides a synchronization point. In its simplest usage, multiple devices, each with their own local oscillator frequency, may be connected together by the CLOCKSYNC pin and will synchronize on the fastest oscillator. This pin may also be used to synchronize the device to an external clock, provided the external signal is of higher frequency than the local oscillator. A resistor load may be needed on this pin to minimize the clock pulse width.

E/AOUT (error amplifier output): This is is the gain stage for overall feedback control. Error amplifier output voltage levels below 1 volt will force 0° phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving with a sufficiently low impedance source.

CS+ (current sense): The non-inverting input to the current-fault comparator whose reference is set internally to a fixed 2.5V (separate from VREF). When the voltage at this pin exceeds 2.5V the current-fault latch is set, the outputs are forced OFF and a SOFT-START cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled from switching and held in a low state until the CS+ pin is brought below 2.5V. The outputs may begin switching at 0 degrees phase shift before the SOFTSTART pin begins to rise -- this condition will not prematurely deliver power to the load.

FREQSET (oscillator frequency set pin): A resistor and a capacitor from FREQSET to GND will set the oscillator frequency.

DELAYSET A-B, DELAYSET C-D (output delay control): The user programmed current flowing from these pins to GND set the turn-on delay for the corresponding output pair. This delay is introduced between turn-off of one switch and turn-on of another in the same leg of the bridge to provide a dead time in which the resonant switching of the external power switches takes place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA– (error amplifier inverting input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level.

EA+ (error amplifier non-inverting input): This is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the EA+ pin.

GND (signal ground): All voltages are measured with respect to GND. The timing capacitor, on the FREQSET pin, any bypass capacitor on the VREF pin, bypass capacitors on VIN and the ramp capacitor, on the RAMP pin, should be connected directly to the ground plane near the signal ground pin.

OUTA-OUTD (outputs A-D): The outputs are 2A totem-pole drivers optimized for both MOSFET gates and level-shifting transformers. The outputs operate as pairs with a nominal 50% duty-cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is syncronized with the clock waveform. The C-D pair will drive the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (power ground): VC should be bypassed with a ceramic capacitor from the VC pin to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should parallel this one. Power ground and signal ground may be joined at a single point to optimize noise rejection and minimize DC drops.

RAMP (voltage ramp): This pin is the input to the PWM comparator. Connect a capacitor from here to GND. A voltage ramp is developed at this pin with a slope:

$$\frac{dV}{dT} = \frac{Sense Voltage}{R_{SLOPE} \bullet C_{RAMP}}$$

Current mode control may be achieved with a minimum amount of external circuitry, in which case this pin provides slope compensation.

Because of the 1.3V offset between the ramp input and the PWM comparator, the error amplifier output voltage can not exceed the effective ramp peak voltage and duty cycle clamping is easily achievable with appropriate values of R_{SLOPE} and C_{RAMP}.

SLOPE (set ramp slope/slope compensation): A resistor from this pin to VCC will set the current used to generate the ramp. Connecting this resistor to the DC input line voltage will provide voltage feed-forward.

SOFTSTART (soft start): SOFTSTART will remain at GND as long as VIN is below the UVLO threshold. SOFTSTART will be pulled up to about 4.8V by an internal 9μA current source when VIN becomes valid (assuming a non-fault condition). In the event of a current-fault (CS+ voltage exceeding 2.5V), SOFTSTART will be pulled to GND and them ramp to 4.8V. If a fault occurs during the SOFTSTART cycle, the outputs will be immediately disabled and SOFTSTART must charge fully prior to resetting the fault latch.

For paralleled controllers, the SOFTSTART pins may be paralled to a single capacitor, but the charge currents will be additive.

PIN DESCRIPTIONS (cont.)

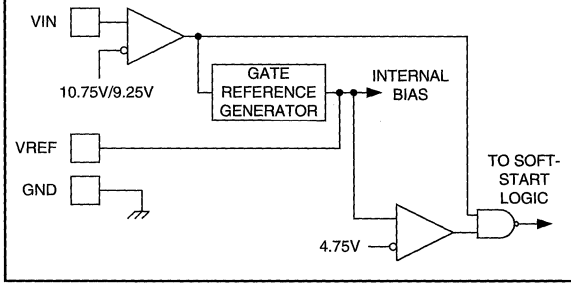
VC (output switch supply voltage): This pin supplies power to the output drivers and their associated bias circuitry. Connect VC to a stable source above 3V for normal operation, above 12V for best performance. This supply should be bypassed directly to the PWRGND pin with low ESR, low ESL capacitors.

VIN (primary chip supply voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12V for normal operation. To ensure proper chip functionality, these devices will be inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should by bypassed directly to the GND pin with low ESR, low ESL capacitors.

NOTE: When VIN exceeds the UVLO threshold the supply current (I_{IN}) will jump from about 100µA to a current in excess of 20µA. If the UC1875 is not connected to a well bypassed supply, it may immediately enter UVLO again.

VREF: This pin is an accurate 5V voltage reference. This output is capable of delivering about 60mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled while VIN is low enough to force the chip into UVLO. The circuit is also in UVLO until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1µF, low ESR, low ESL, capacitor to the GND pin.

APPLICATION INFORMATION
Undervoltage Lockout Section

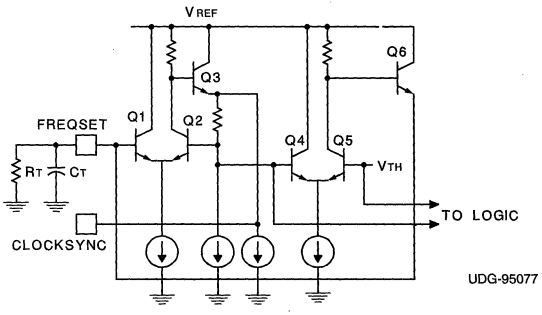


When power is applied to the circuit and VIN is below the upper UVLO threshold, I_{IN} will be below 600µA, the reference generator will be off, the fault latch is reset, the soft-start pin is discharged, and the outputs are actively held low. When VIN exceeds the upper UVLO threshold, the reference generator turns on. All else remains in the shut-down mode until the output of the reference, VREF, exceeds 4.75V.

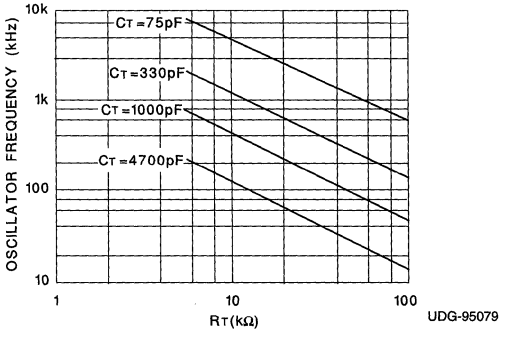
UDG-99136

The high frequency oscillator may be either free-running or externally synchronized. For free-running operation, the frequency is set via an external resistor and capacitor to ground from the FREQSET pin.

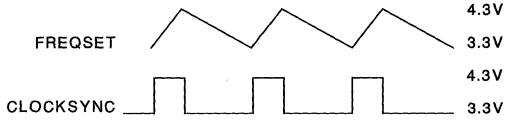
Simplified Oscillator Schematic



UDG-95077



UDG-95079



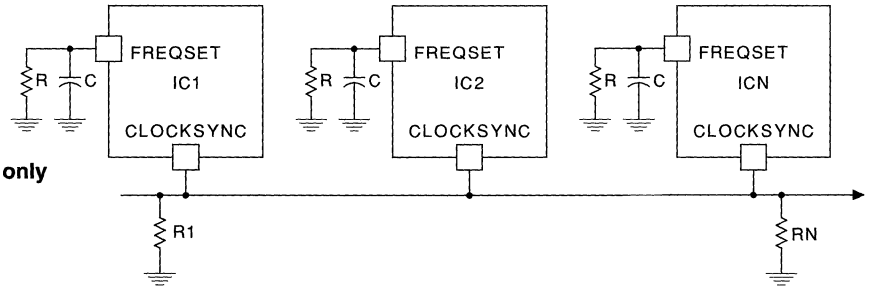
UDG-95078

APPLICATION INFORMATION (cont.)

Synchronizing The Oscillator

The CLOCKSYNC pin of the oscillator may be used to synchronize multiple UC1875 devices simply by connecting the CLOCKSYNC of each UC1875 to the others:

1875/6/7/8s only



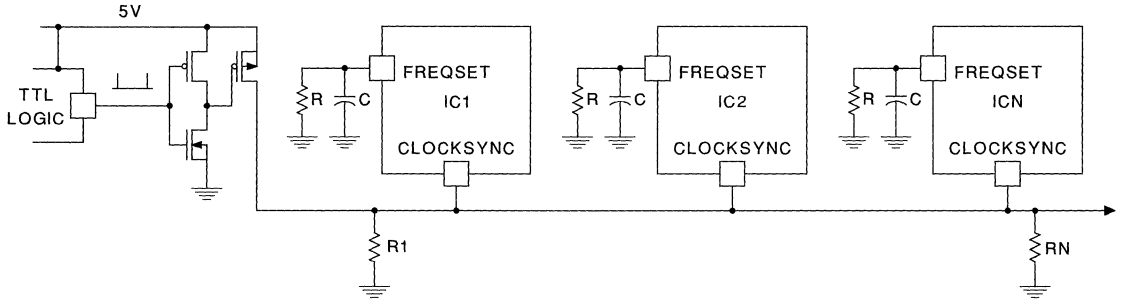
UDG-95080

All ICs will sync to chip with the fastest local oscillator.

R1 & RN *may* be needed to keep sync pulse narrow due to capacitance on line.

R1 & RN *may* also be needed to properly terminate R_{SYNC} line.

Syncing to external TTL/CMOS



UDG-95081

ICs will sync to fastest chip or TTL clock if it is higher frequency.

R & RN *may* be needed for same reasons as above

Although each UC1875/6/7/8 has a local oscillator frequency, the group of devices will synchronize to the fastest oscillator driving the CLOCKSYNC pin. This arrangement allows the synchronizing connection between ICs to be broken without any local loss of functionality.

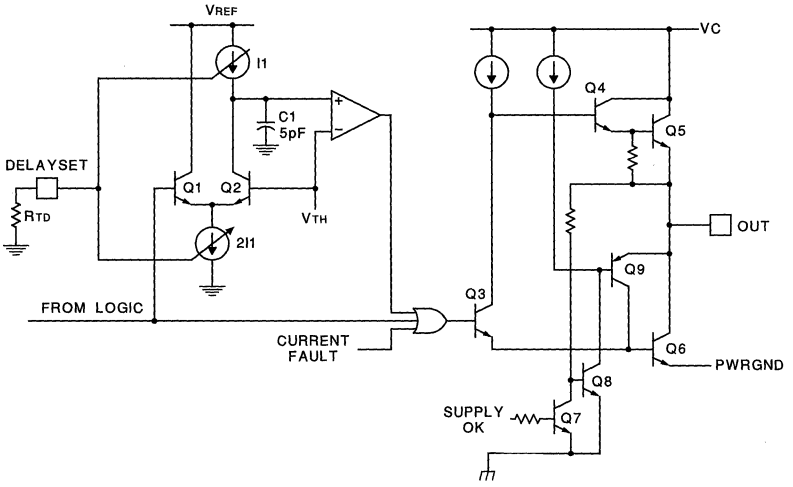
Synchronizing the device to an external clock signal may be accomplished with a minimum of external circuitry, as shown in the previous figure.

Capacitive loading on the CLOCKSYNC pin will increase the clock pulse width, and may adversely effect system performance. Therefore, a resistor to ground from the CLOCKSYNC pin is optional, but may be required to offset capacitive loading on this pin. These resistors are shown in the oscillator schematics as R1, RN.

APPLICATION INFORMATION (cont.)

Delay Blocks And Output Stages

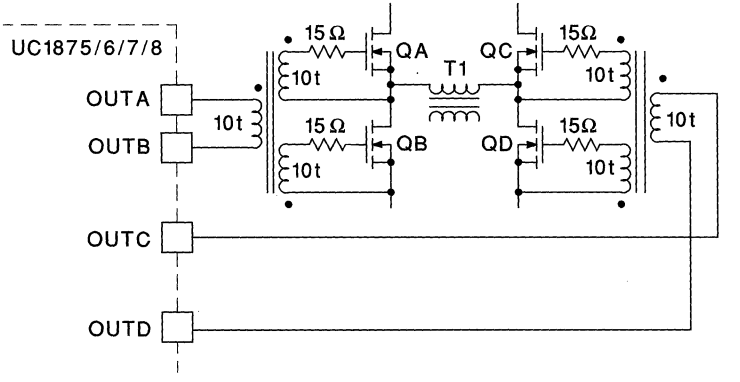
In each of the output stages, transistors Q3 through Q6 form a high-speed totem-pole driver which will source or sink more than one amp peak with a total delay of approximately 30 nanoseconds. To ensure a low output level prior to turn-on, transistors Q7 through Q9 form a self-biased driver to hold Q6 on prior to the supply reaching its turn-on threshold. This circuit is operable when the chip supply is zero. Q6 is also turned on and held low with a signal from the fault logic portion of the chip.



The delay providing the dead-time is accomplished with C1 which must discharge to V_{TH} before the output can go high. The time is defined by the current sources, I1, which is programmed by an external resistor, R_{TD}. The voltage on the Delay Set pins is internally regulated to 2.5V and the range of dead time control is from 50 to 200 nanoseconds. NOTE: There is no way to disable the delay circuitry, and the delay time must be programmed.

Output Switch Orientation

The four outputs of the UC1875/6/7/8 interface to the full bridge converter switches as shown below:



3 Winding Bifilar, AWG 30 Kynar Insulation

APPLICATION INFORMATION (cont.)

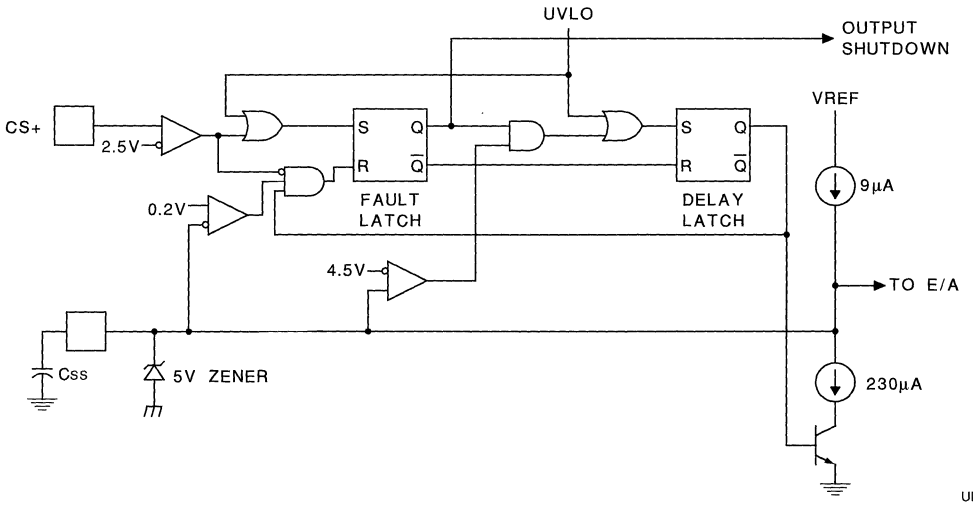
Fault/Soft-Start

The fault control circuitry provides two forms of power shutdown:

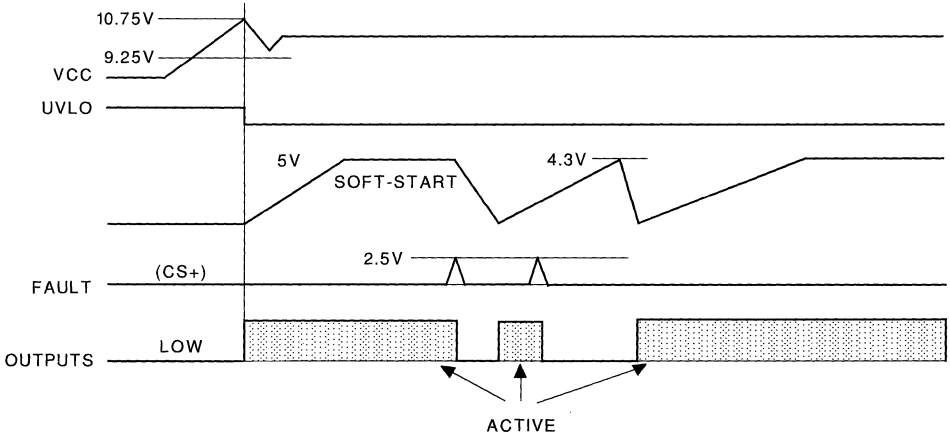
- Complete turn-off of all four output power stages.
- Clamping the phase shift command to zero.

Complete turn-off is ordered for an over-current fault or a low supply voltage. When the SOFTSTART pin reaches its low threshold, switching is allowed to proceed while the phase-shift is advanced from zero to its nominal value with the time constant of the SOFT-START capacitor.

The fault logic insures that a continuous fault will institute a low frequency "hiccup" retry cycle by forcing the SOFT-START capacitor to charge through its full cycle between each restart attempt.



UDG-95084



UDG-95085

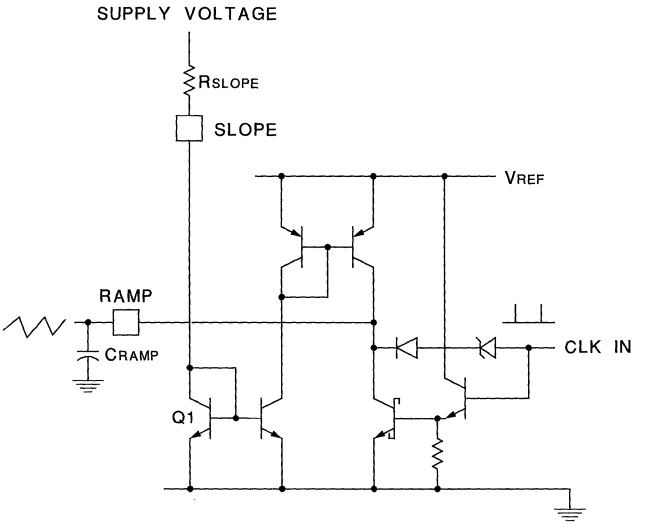
APPLICATIONS INFORMATION (cont.)
Slope/Ramp Pins

The ramp generator may be configured for the following control methods:

- Voltage Mode
- Voltage Feedforward
- Current Mode
- Current Mode with Slope Compensation

The figure below shows a voltage-mode configuration. With R_{SLOPE} tied to a stable voltage source, the waveform on C_{RAMP} will be a constant-slope ramp, providing conventional voltage-mode control. If R_{SLOPE} is connected to the power supply input voltage, a variable-slope ramp will provide voltage feedforward.

Voltage Mode Operation



UDG-95086

1. Simple voltage mode operation achieved by placing R_{SLOPE} between VIN and SLOPE.

2. Voltage Feedforward achieved by placing R_{SLOPE} between supply voltage and SLOPE pin of UC1875.

RAMP

$$\frac{dV}{dT} \approx \frac{V_{Rslope}}{R_{SLOPE} \bullet C_{RAMP}}$$

For current-mode control the ramp generator may be disabled by grounding the slope pin and using the ramp pin as a direct current sense input to the PWM comparator.

UNITRODE CORPORATION
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UNITRODE

application INFO available

UC1879
UC2879
UC3879

Phase Shift Resonant Controller

FEATURES

- Programmable Output Turn On Delay; Zero Delay Available
- Compatible with Voltage Mode or Current Mode Topologies
- Practical Operation at Switching Frequencies to 300kHz
- Four 100mA Totem Pole Outputs
- 10MHz Error Amplifier
- Pin Programmable Undervoltage Lockout
- Low Startup Current - 150µA
- Soft Start Control
- Outputs Active Low During UVLO

DESCRIPTION

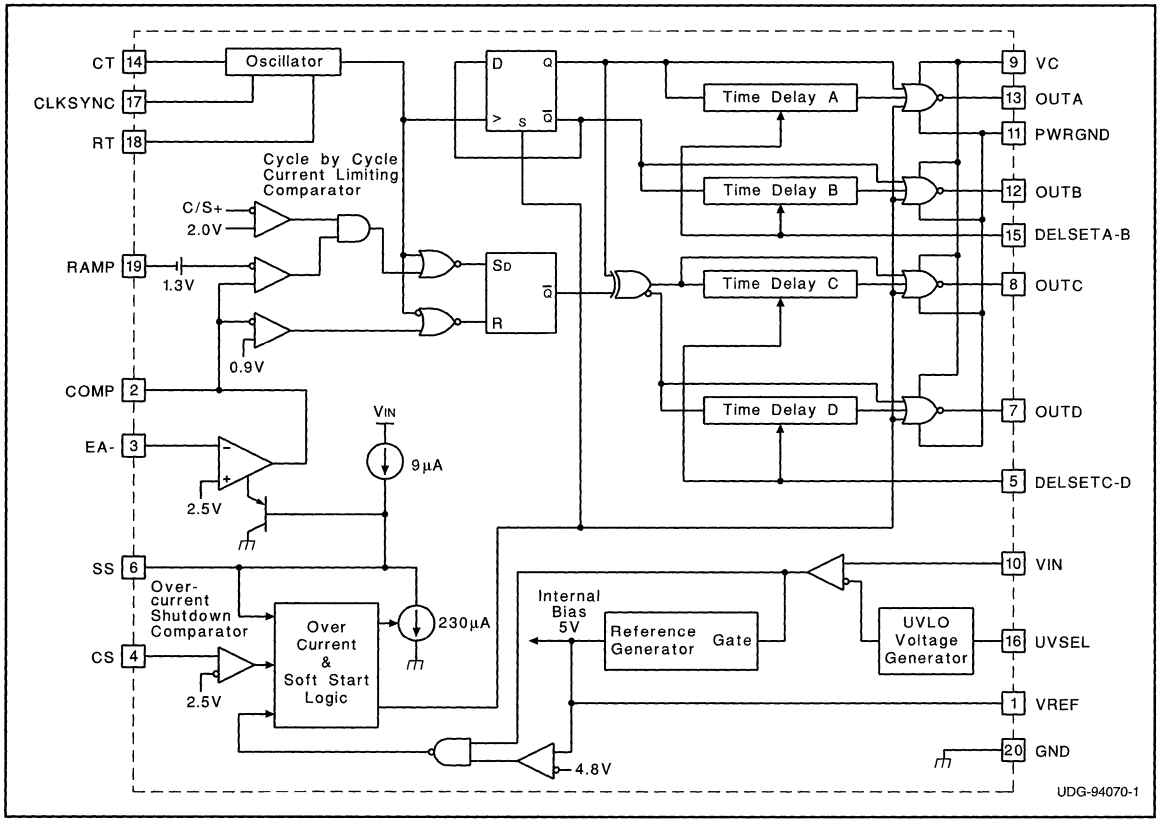
The UC3879 controls a bridge power stage by phase shifting the switching of one half-bridge with respect to the other. This allows constant frequency pulse width modulation in combination with resonant, zero-voltage switching for high efficiency performance. The UC3879 can be configured to provide control in either voltage mode or current mode operation, with overcurrent shutdown for fast fault protection.

Independently programmable time delays provide dead-time at the turn-on of each output stage, allowing time for each resonant switching interval.

With the oscillator capable of operating in excess of 600kHz, overall output switching frequencies to 300kHz are practical. In addition to the standard free running mode, with the CLKSYNC pin, the user may configure the UC3879 to accept an external clock synchronization signal. Alternatively, up to three units can be locked together with the operational frequency determined by the fastest device.

Protective features include an undervoltage lockout and overcurrent protection. Additional features include a 10MHz error amplifier, a 5V precision reference, and soft start. The UC3879 is available in 20 pin N, J, DW, and Q and 28 pin L packages.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VC, VIN) 20V
Output Current, Source or Sink, DC 20mA
Analog I/0s
(Pins 1, 2, 3, 4, 5, 6, 14, 15, 17, 18, 19) . . . . . –0.3 to 5.3V
(Pin 16) . . . . . –.03V to VIN
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Notes: *Pin references are to 20 pin DIL and SOIC packages. All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

CLCC-28 (Top View)
L Package

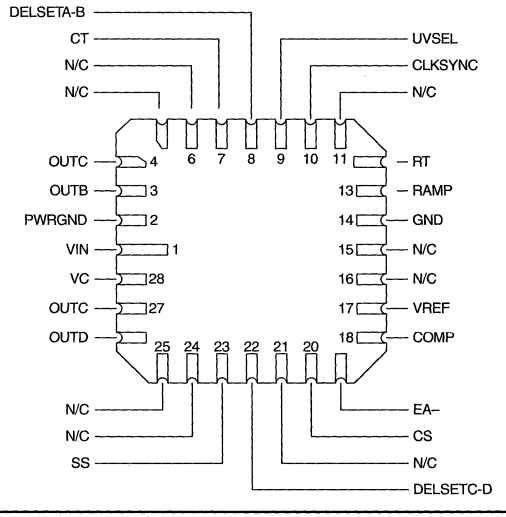
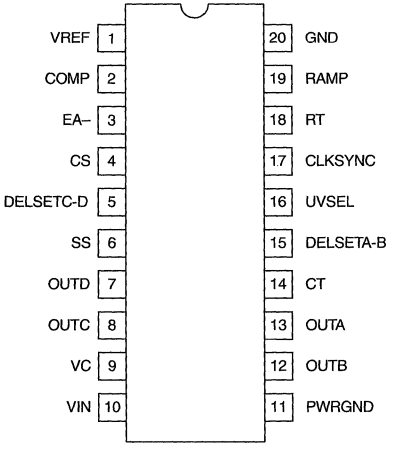


Table I. Product Selection Guide

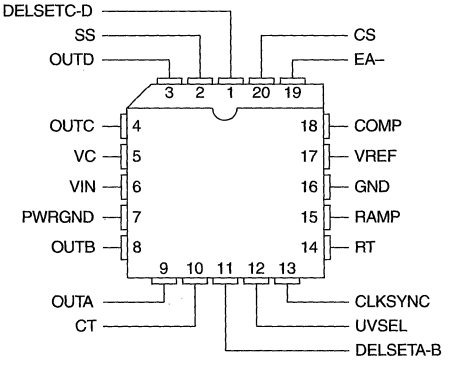
	TEMPERATURE RANGE	AVAILABLE PACKAGES
UCC1879	– 55°C to +125°C	J, L
UCC2879	– 40°C to +85°C	N, DW, Q, J, L
UCC3879	0°C to +70°C	N, DW, Q

CONNECTION DIAGRAMS

DIL-20, SOIC-20 (Top View)
J or N Package, DW Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS Unless specified; VC = VIN = V_{UVSEL} =12V, CT = 470pF, RT = 9.53k, $R_{DELSETA-B}$ = $R_{DELSEC-D}$ = 4.8k, $C_{DELSETA-B}$ = $C_{DELSETC-D}$ = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
Start Threshold	V_{UVSEL} = VIN	9	10.75	12.5	V
	V_{UVSEL} = Open	12.5	15.25	16.5	V
UVLO Hysteresis	V_{UVSEL} = VIN	1.15	1.75	2.15	V
	V_{UVSEL} = Open	5.2	6	7.4	V
Input Bias, UVSEL Pin	V_{UVSEL} = VIN = 8V		30		µA
Supply Current					
I_{VIN} Startup	VIN = V_{UVSEL} = 8V, VC = 18V, $I_{DELSETA-B}$ = $I_{DELSETC-D}$ = 0		150	600	µA
I_{VC} Startup	VIN = V_{UVSEL} = 8V, VC = 18V, $I_{DELSETA-B}$ = $I_{DELSETC-D}$ = 0		10	100	µA
I_{VIN} Operating	UC3879, UC2879		23	33	mA
	UC1879		23	36	mA
I_{VC} Operating			4	8	mA
Voltage Reference					
Output Voltage	T_J = +25°C	4.92	5	5.08	V
Line Regulation	11V < VIN < 18V		1	10	mV
Load Regulation	I_{VREF} = –10mA		5	20	mV
Total Variation	Line, Load, Temperature	4.875		5.125	V
Short Circuit Current	VREF = 0V, T_J = 25°C		–60	–15	mA
Error Amplifier					
Error Amplifier Input Voltage		2.4	2.5	2.6	V
Input Bias Current			0.6	3	µA
AVOL	1V < V_{COMP} < 4V	60	90		dB
PSRR	11V < VIN < 18V	85	100		dB
Output Sink Current	V_{COMP} = 1V	1	2.5		mA
Output Source Current	V_{COMP} = 4V		–1.3	–0.5	mA
Output Voltage High	I_{COMP} = –0.5mA	4	4.7	5	V
Output Voltage Low	I_{COMP} = 1mA	0	0.5	1	V
Slew Rate	T_A = +25°C	6	11		V/µs
PWM Comparator					
RAMP Offset Voltage	T_J = 25°C, Note 3	1.1	1.25	1.4	V
PWM Phase Shift,	V_{COMP} > $V_{RAMPpeak}$ + $V_{RAMPoffset}$	98	99.7	102	%
$T_{DELSETA-B}$, $T_{DELSETC-D}$ = 0, Note 1	V_{COMP} < Zero Phase Shift Voltage	0	0.3	2	%
Output Skew,	V_{COMP} > $V_{RAMPpeak}$ + $V_{RAMPoffset}$		10		ns
$T_{DELSETA-B}$, $T_{DELSETC-D}$ = 0, Note 1	V_{COMP} < Zero Phase Shift Voltage		10		ns
Ramp to Output Delay, $T_{DELSETA-B}$ = 0,	UC3879, UC2879		115	250	ns
$T_{DELSETC-D}$ = 0	UC1879		115	300	ns
Oscillator					
Initial Accuracy	T_A = 25°C	180	200	220	kHz
Voltage Stability	11V < VIN < 18V		1	2	%
Total Variation	Line, Temperature	160	200	240	kHz
CLKSYNC Threshold		2.3	2.5	2.7	V
Clock Out High		2.8	4		V
Clock Out Low		0.5	1	1.5	V
Clock Out Pulse Width			400	600	ns
Ramp Valley Voltage			0.2	0.4	V

ELECTRICAL CHARACTERISTICS Unless specified; VC = VIN = V_{UVSEL} =12V, CT = 470pF, RT = 9.53k, $R_{DELSETA-B}$ = $R_{DELSEC-D}$ = 4.8k, $C_{DELSETA-B}$ = $C_{DELSETC-D}$ = 0.01µF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Ramp Peak Voltage		2.8	2.9	3.2	V
Current Limit					
Input Bias	V_{CS} = 3.0V		2	10	µA
Threshold Voltage		2.35	2.5	2.65	V
Delay to OUTA, B, C, D			160	300	ns
Cycle-by-Cycle Current Limit					
Input Bias	V_{CS} = 2.2V		2	10	µA
Threshold Voltage		1.85	2	2.15	V
Delay to Output Zero Phase			110	300	ns
Soft Start/Reset Delay					
Charge Current	V_{SS} = 0.5V	–20	–9	–3	µA
Discharge Current	V_{SS} = 1V	120	230		µA
Restart Threshold		4.3	4.7		V
Discharge Level			300		mV
Output Drivers					
Output Low Level	I_{OUT} = 10mA		0.3	0.4	V
Output High Level	I_{OUT} = –10mA, Referenced to VC		2.2	3	V
Delay Set (Note 5)					
Delay Time	$R_{DELSETA-B}$ = $R_{DELSETC-D}$ = 4.8k	300	430	600	ns
Delay Time	$R_{DELSETA-B}$ = $R_{DELSETC-D}$= 1.9k	130	170	250	ns
Zero Delay	$V_{DELSETA-B}$ = $V_{DELSETC-D}$ = 5V		5		ns

Note 1. *Phase shift percentage (0% = 0°, 100% = 180°) is defined as* $\theta = \frac{200}{T}\Phi$ %

where θ *is the phase shift, and* Φ *and T are defined in Figure 1. At 0% phase shift,* Φ *is the output skew.*

Note 2. *Delay time is defined as:*

$$delay = T \bullet \left(\frac{1}{2} - duty\ cycle\right)$$

where T is defined in Figure 1.

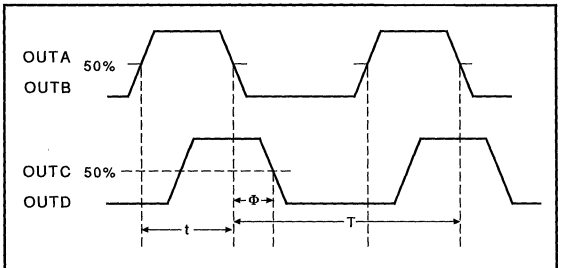
Note 3. *Ramp offset voltage has a temperature coeffecient of about –4mV/°C.*

Note 4. *The zero phase shift voltage is the voltage measured at COMP which forces zero phase shift. This condition corresponds to zero effective output power. Zero phase shift voltage has a temperature coeffecient of about –2mV/°C.*

Note 5. *Delay time can be programmed via resistors from the delay set pins to ground.*

$$Delay\ Time = \left(0.89 \bullet 10^{-10} \bullet R_{DELAY}\right) \text{sec}$$

The recommended range for R_{DELAY} *is 1.9k to 10k.*



$Duty\ Cycle = \frac{t}{T}$

$Period = T$

$T_{DHL}(A\ to\ C) = T_{DHL}(B\ to\ D) = \Phi$

Figure 1. Phase Shift, Output Skew & Delay Time Definitions

PIN DESCRIPTIONS

CLKSYNC (Bi-directional Clock and Synchronization): Used as an output, CLKSYNC provides a clock signal. As an input, this pin provides a synchronization point. Multiple UC3879s, each with their own local oscillator frequency, may be connected together by the CLKSYNC pin, and they will synchronize to the fastest oscillator. This pin may also be used to synchronize the UC3879 to an external clock, provided the frequency of the external signal is higher than the frequency of the local oscillator. CLKSYNC is internally connected to an emitter follower pull-up and a current source pull-down (300µA typical). Therefore an external resistor to GND can be used to improve the CLKSYNC pin's ability to drive capacitive loads.

COMP (Error Amplifier Output): This pin is the output of the gain stage for overall feedback control. Error amplifier output voltage levels below 0.9 volt forces zero phase shift. Since the error amplifier has a relatively low current drive capability, the output may be overridden by driving it with a sufficiently low impedance source.

CT (Oscillator Frequency Set): After choosing RT to set the required upper end of the linear duty cycle range, the timing capacitor (CT) value is calculated to set the oscillator frequency as follows:

$$CT = \frac{Dlin}{1.08 \bullet RT \bullet f}$$

Connect the timing capacitor directly between CT and GND. Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 600kHz.

CS (Current Sense): This pin is the non-inverting input to the two current fault comparators whose references are set internally to fixed values of 2.0V and 2.5V. When the voltage at this pin exceeds 2.0V, and the error amplifier output voltage exceeds the voltage on the ramp input, the phase shift limiting overcurrent comparator will limit the phase shifting on a cycle-by-cycle basis. When the voltage at this pin exceeds 2.5V, the current fault latch is set, the outputs are forced OFF, and a soft start cycle is initiated. If a constant voltage above 2.5V is applied to this pin the outputs are disabled and held low. When CS is brought below 2.5V, the outputs will begin switching at 0 degrees phase shift before the SS pin begins to rise. This condition will not prematurely deliver power to the load.

DELSETA-B, DELSETC-D (Output Delay Control): The user programmed currents from these pins to GND set the turn on delay for the corresponding output pair. This delay is introduced between the turn off of one switch and the turn on of another in the same leg of the bridge to allow resonant switching to take place. Separate delays are provided for the two half-bridges to accommodate differences in the resonant capacitor charging currents.

EA– (Error Amplifier Inverting Input): This is normally connected to the voltage divider resistors which sense the power supply output voltage level. The loop compensation components are connected between this pin and COMP.

GND (Signal Ground): All voltages are measured with respect to GND. The timing capacitor on CT, and bypass capacitors on VREF and VIN should be connected directly to the ground plane near GND.

OUTA – OUTD (Outputs A-D): The outputs are 100mA totem pole output drivers optimized to drive FET driver ICs. The outputs operate as pairs with a nominal 50% duty cycle. The A-B pair is intended to drive one half-bridge in the external power stage and is synchronized to the clock waveform. The C-D pair drives the other half-bridge with switching phase shifted with respect to the A-B outputs.

PWRGND (Power Ground): VC should be bypassed with a ceramic capacitor from VC to the section of the ground plane that is connected to PWRGND. Any required bulk reservoir capacitor should be connected in parallel. PWRGND and GND should be connected at a single point near the chip to optimize noise rejection and minimize DC voltage drops.

RAMP (Voltage Ramp): This pin is the input to the PWM comparator. Connect it to CT for voltage mode control. For current mode control, connect RAMP to CS and also to the output of the current sense transformer circuit. Slope compensation can be achieved by injecting a portion of the ramp voltage from CT to RAMP.

PIN DESCRIPTIONS (cont.)

RT (Clock/Sync Duty Cycle Set Pin): The UC3879 oscillator produces a sawtooth waveform. The rising edge is generated by connecting a resistor from RT to GND and a capacitor from CT to GND (see CT pin description). During the rising edge, the modulator has linear control of the duty cycle. The duty cycle jumps to 100% when the voltage on COMP exceeds the oscillator peak voltage. Selection of RT should be done first, based on the required upper end of the linear duty cycle range (Dlin) as follows:

$$RT = \frac{2.5}{10mA \bullet (1 - Dlin)}$$

Recommended values for RT range from 2.5k to 100k.

SS: Connect a capacitor between this pin and GND to set the soft start time. The voltage at SS will remain near zero volts as long as VIN is below the UVLO threshold. Soft start will be pulled up to about 4.8V by an internal 9µA current source when VIN and VREF become valid (assuming a non-fault condition). In the event of a current fault (CS voltage exceeding 2.5V), soft start will be pulled to GND and then ramp to 4.8V. If a fault occurs during the soft start cycle, the outputs will be immediately disabled and soft start must fully charge prior to resetting the fault latch. For paralleled controllers, the soft start pins may be paralleled to a single capacitor, but the charge currents will be additive.

UVSEL: Connecting this pin to VIN sets a turn on voltage of 10.75V with 1.5V of UVLO hysteresis. Leaving the pin open-circuited programs a turn on voltage of 15.25V with 6.0V of hysteresis.

VC (Output Switch Supply Voltage): This pin supplies power to the output drivers and their associated bias circuitry. The difference between the output high drive and VC is typically 2.1V. This supply should be bypassed directly to PWRGND with a low ESR/ESL capacitor.

VIN (Primary Chip Supply Voltage): This pin supplies power to the logic and analog circuitry on the integrated circuit that is not directly associated with driving the output stages. Connect VIN to a stable source above 12V for normal operation. To ensure proper functionality, the UC3879 is inactive until VIN exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND with a low ESR/ESL capacitor.

NOTE: *When VIN exceeds the UVLO threshold the supply current (I_{IN}) jumps from about 100µA to greater than 20mA. If the UC3879 is not connected to a well bypassed supply, it may immediately enter the UVLO state again. Therefore, sufficient bypass capacity must be added to ensure reliable startup.*

VREF: This pin provides an accurate 5V voltage reference. It is internally short circuit current limited. VREF is disabled while VIN is below the UVLO threshold. The circuit is also disabled until VREF reaches approximately 4.75V. For best results bypass VREF with a 0.1µF, low ESR/ESL capacitor.

ADDITIONAL INFORMATION

Please refer to the following Unitrode publications for additional information. The following three topics are available in the Applications Handbook.

[1] Application Note U-154, *The New UC3879 Phase-Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters* by Laszlo Balogh.

[2] Application Note U-136, *Phase Shifted, Zero Voltage Transition Design Considerations and the UC3875 PWM Controller* by Bill Andreycak.

Design Note DN-63, *The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters* by Laszlo Balogh.

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Pentium® Pro Controller

PRELIMINARY

FEATURES

- Combined DAC/Voltage Monitor and PWM Functions
- 4-Bit Digital-to-Analog Converter (DAC)
- 1.0% DAC/Reference
- Low Offset X20 Current Sense Amplifier
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 2Ω Totem Pole Output
- Chip Disable Function

DESCRIPTION

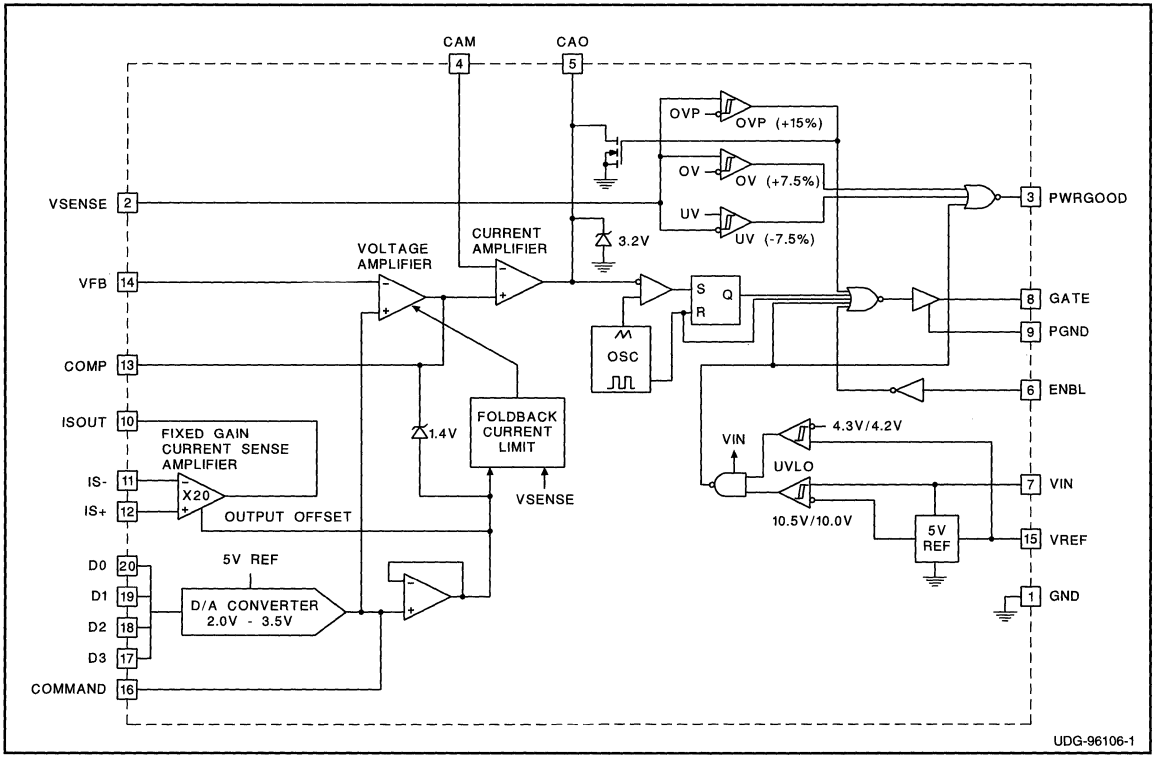
The UCC3880-4/-5/-6 combines high precision reference and voltage monitoring circuitry with average current mode PWM controller circuitry to power Intel Pentium Pro and other high-end microprocessors with a minimum of external components. The UCC3880-x converts 5VDC to an adjustable output, ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The chip includes a precision 5V reference which is capable of sourcing current to an external load. The output voltage of the DAC is derived from this reference, and is programmed directly by Intel's VID pins (Table 1).

The accuracy of the DAC/reference combination is 1.0%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 7.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 15%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. Grounding the ENABLE pin forces the GATE output low.

(continued)

BLOCK DIAGRAM



DESCRIPTION (cont.)

The voltage and current amplifiers have a 4MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz, depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 2Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC2880-x is specified for operation from –25°C to 85°C, and the UCC3880-x is specified for operation from 0°C to 70°C.

Pentium® Pro is a registered trademark of Intel Corporation.

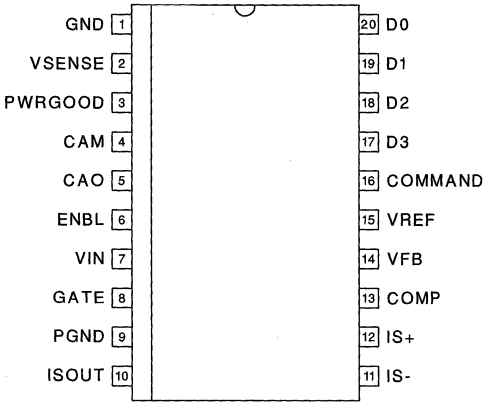
ORDERING INFORMATION

UCC □ 880 □ - □
- □ — See Frequency Gain Table
- □ — Package
- □ — Temperature Range

Consult factory for temperature range or package options not shown.

CONNECTION DIAGRAM

SOIC-20 (Top View)
DW Package



Frequency Gain Table

	Frequency		
	100kHz	200kHz	400kHz
UCC3880-4	X		
UCC3880-5		X	
UCC3880-6			X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
I_{IN}			3.5		mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, I_{VREF} = 0mA	–1		1	%
D0-D3 Voltage High	DX Pin Floating		5		V
D0-D3 Input Bias Current	DX Pin Tied to GND		–70	–20	µA
VREF Output Voltage		4.975	5	5.025	V
VREF Load Regulation	I_{VREF} = 0mA to 5mA	–10	0		mV
VREF Sourcing Current	VREF = 0V		10		mA
OVP Comparator					
Trip Point	% Over COMMAND Voltage	10	15	20	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined		–0.1		µA
Propagation Delay			1		µs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)		7.6	10	%
Return Point	% Over COMMAND Voltage (Note 1)	5	7.4		%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	VSENSE = 2.0V			470	Ω
Propagation Delay			1		µs
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)	–10	–7.6		%
Return Point	% Over COMMAND Voltage (Note 1)		–7.4	–5	%
Hysteresis			20	30	mV
Propagation Delay			1		µs
Enable Pin					
Pull-up Current	V_{ENBL} = 2.5V		–50	–20	µA
Voltage Error Amplifier					
Input Offset Voltage	V_{COMP} = 3.5V		0.0		mV
Input Bias Current	V_{CM} = 3.0V		–0.02	0	µA
Open Loop Gain	1V < V_{COMP} < 4V		90		dB
Common Mode Rejection Ratio	2V < V_{COMP} < 3.5V		90		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	V_{VFB} = 2V, $V_{COMMAND}$ = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{VFB} = 3V, $V_{COMMAND}$ = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3		MHz
Current Sense Amplifier					
Gain			20		V/V
Input Resistance			5		kΩ
Common Mode Rejection Ratio	0V < V_{CM} < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{IS-} = 2V, V_{ISOUT} = V_{IS+} = 2.5V		–0.5		mA
Output Sinking Current	V_{IS-} = 3V, V_{ISOUT} = V_{IS+} = 2.5V		6.0		mA
–3dB Frequency	At GAIN = 20		1.75		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V			10	mV
Input Bias Current	V_{CM} = 3.0V		0.15		µA
Open Loop Gain	1V < V_{CAO} < 3V		90		dB
Output Voltage High	V_{COMP} = 3V, V_{CAM} = 2.5V		3.2		V
Common Mode Rejection Ratio	1.5V < V_{CM} < 4.9V		80		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	V_{CAM} = 2V, V_{CAO} = V_{COMP} = 2.5V		–0.5		mA
Output Sinking Current	V_{CAM} = 3V, V_{CAO} = V_{COMP} = 2.5V		2.0		mA
Gain Bandwidth Product	F = 100kHz		3.5		MHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, V_{ENBL} = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < T_A < 70°C, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency (–4)		85	100	115	kHz
Frequency (–5)			200		kHz
Frequency (–6)			400		kHz
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	I_{GATE} = –100mA		0.20		V
Output High Voltage	I_{GATE} = 100mA		11.8		V
Rise Time	C_{GATE} = 3.3nF		20	80	ns
Fall Time	C_{GATE} = 3.3nF		15	80	ns
Output Impedance	I_{GATE} = 100mA		2		Ω
	I_{GATE} = –100mA		2		Ω
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; V_{SENSE} = $V_{COMMAND}$ = 3V		4.4		V
	$V_{COMMAND}$ = 3V, V_{SENSE} = 0		3.7		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D3 pins.

PIN DESCRIPTIONS

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO (Current Amplifier Output): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage for excellent transient response.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. Setting all input control codes low produces 3.5V at COMMAND; setting all codes high produces 2.0V at COMMAND. The DAC LSB step size (i.e. resolution) is 100mV (See Table 1). The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01μF, low ESR, low ESL capacitor for best circuit noise immunity.

Decimal Code	D3	D2	D1	D0	COMMAND Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

Table 1. Programming the COMMAND Voltage

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing

PIN DESCRIPTIONS (cont.)

the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND. A bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

ENBL (Chip Enable Pin): This input is used to disable the GATE and PWRGOOD outputs. Grounding this pin causes the GATE output to be held low; floating the pin or pulling it up to 5V ensures normal operation. ENBL is pulled up to 5V internally.

GATE (PWM Output, MOSFET Driver): This output provides a 2Ω totem pole driver. Use a series resistor of at least 5Ω between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS– (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is (COMMAND + G_{CSA} • I • R_{SENSE}), where COMMAND is the voltage on the COMMAND pin, G_{CSA} is the fixed gain of the current sense amplifier, equal to 20, I is the current through the sense resistor, and R_{SENSE} is the value of the average current sensing resistor.

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor ≥ 0.10µF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 7.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 7.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 15%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

APPLICATION INFORMATION

Current Limit

The short circuit current limit, I_{SC}, is set according to:

$$ISC = \frac{1.4V}{R_{SENSE} \bullet G_{CSA}}$$

where R_{SENSE} is the average current sense resistor and G_{CSA} is the current sense amplifier gain, where G_{CSA} equals 20. Example: Choose R_{SENSE} to set the short circuit current limit at 16A using the UCC3880-5

$$R_{SENSE} = \frac{1.4V}{16A \bullet 20} = 4.4m\Omega$$

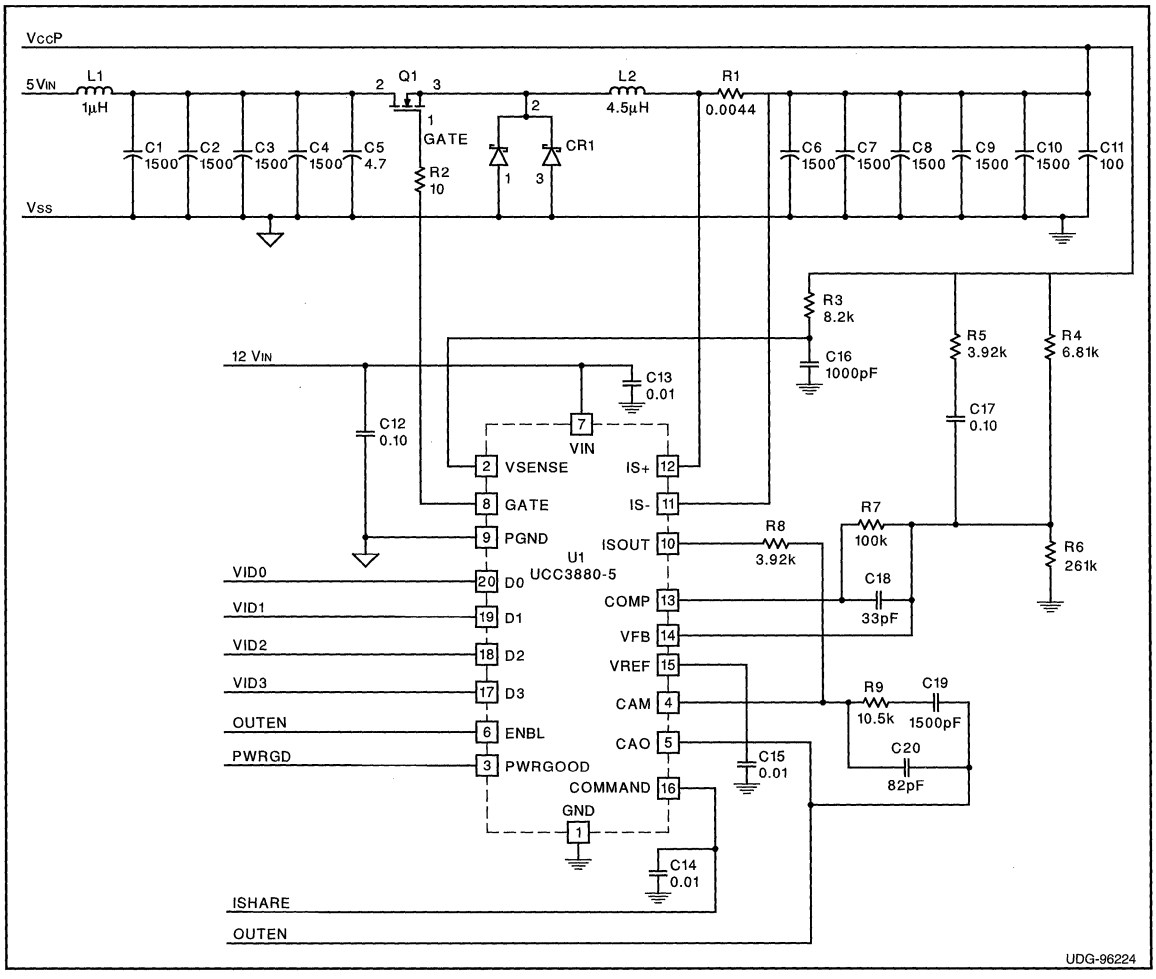
A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the full load current.

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

TYPICAL APPLICATION

The UCC3880-x is ideal for converting the 5.0V system bus into the required Pentium® Pro bus voltage.



UCC3880 Configured for Powering the Pentium® Pro

PARTS LIST

REF.	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD
C12	0.10µF Ceramic	1206 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.01µF Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10µF Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10µF Ceramic	1206 SMD
C22	0.10µF Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB
R1	Dale/Vishay WSR-2 0.005Ω 1%	SMD Power Package
R2	10Ω, 5%, 1/16 Watt	0603 SMD
R3	8.2kΩ, 5%, 1/16 Watt	0603 SMD
R4	6.81kΩ, 1%, 1/16 Watt	0603 SMD
R5	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R6	261kΩ, 1%, 1/16 Watt	0603 SMD
R7	100kΩ, 1%, 1/16 Watt	0603 SMD
R8	3.92kΩ, 1%, 1/16 Watt	0603 SMD
R9	10.5kΩ, 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

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Average Current Mode Synchronous Controller With 5-Bit DAC

FEATURES

- Combined DAC/Voltage Monitor and PWM with Synchronous Rectification Functions
- 5-Bit Digital-to-Analog (DAC) Converter
- 1% DAC/Reference Combined Accuracy
- Compatible with 5V and 12V Systems and 12V-only Systems
- Low Offset Current Sense Amplifier
- Programmable Oscillator Frequency Practical to 700kHz
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- 2Ω Totem Pole Outputs with Programmable Dead Times to Eliminate Cross-Conduction
- Chip Disable Function

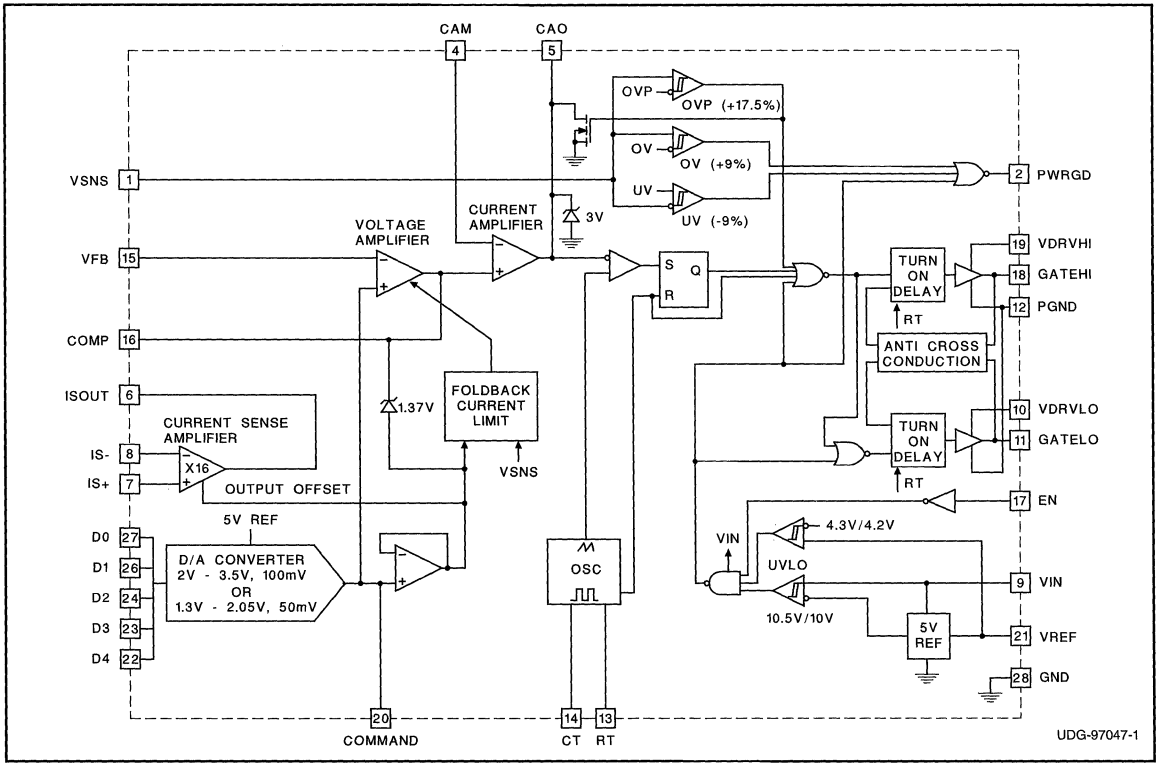
DESCRIPTION

The UCC3882 combines high precision reference and voltage monitoring circuitry with average current mode PWM synchronous rectification controller circuitry to power high-end microprocessors with a minimum of external components. The UCC3882 converts 5V or 12V to an adjustable output ranging from 1.8VDC to 2.05VDC in 50mV steps and 2.1VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The DAC output voltage is directly compatible with Intel's 5-bit VID code (Table 1) which covers 1.3V to 2.05V in 50mV steps and 2.1V to 3.5V in 100mV steps. The accuracy of the DAC/reference combination is better than 1%. Undervoltage lockout circuitry assures the correct logic states at the outputs during power up and power down. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its designed value by more than 9%. A second overvoltage comparator digitally forces GATEHI off and GATELO on when the system output voltage exceeds its designed value by more than 17.5%.

(continued)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

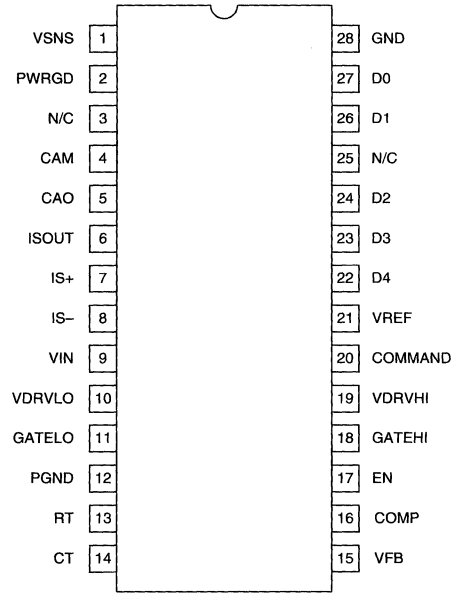
VDRVHI, GATEHI (Note 1) . . . . . –0.3V to 20V
VDRVLO, GATELO. . . . . –0.3V to 15V
All other pins referenced to GND . . . . . –0.3V to 5.3V
VIN. . . . . +15V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature. . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

Note 1: 20V at no load. Derate to 18.5V when used with capacitive loads of greater than 1000pF in series with less than 20 Ω.

CONNECTION DIAGRAM

DIL-28, SOIC-28 (Top View)
N, DW or PW Packages



DESCRIPTION (continued)

For all of the parts, grounding the EN pin disables the GATEHI and GATELO outputs, shutting down the power supply. For the 2882 and 3882 only, programming a DAC output voltage below 1.8V, or programming all of the VID pins high also disables the GATEHI and GATELO outputs. For the "–1" option parts, the GATEHI and GATELO outputs are switching, and the power supply output voltage regulates at the programmed DAC output voltage for all VID codes.

The voltage and current amplifiers have 2.5MHz gain-bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is externally programmed with RT and CT. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short-circuited, minimizing component stress and dissipation during abnormal conditions. The gate drivers are low impedance totem pole output stages capable of driving large external MOSFETs. Cross conduction is eliminated internally by programming the dead time between turn-off and turn on of the external high side and synchronous MOSFETs.

This device is available in a 28-pin wide body surface mount package. The UCC2882 is specified for operation from –25°C to +85°C and the UCC3882 is specified for operation from 0°C to 70°C.

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12V, VSNS = 3.5V, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V$, R_T = 13k, C_T = 1.8nF, EN = Open, 0°C < T_A < 70°C, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis		300	500	700	mV
Supply Current					
I_{IN}	EN = 0V		7	12	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12V, VSNS = 3.5V, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V$, $R_T = 13k$, $C_T = 1.8nF$, EN = Open, $0°C < T_A < 70°C$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, IREF = 0mA (Note 1)	–1		1	%
D0-D4 Voltage High	DX Pin Floating		5	5.2	V
D0-D4 Input Bias Current	DX Pin Tied to GND	–120	–70	–20	µA
OVP Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)	10	17	25	%
Hysteresis			20		mV
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)	5	9	12	%
Hysteresis			20		mV
PWRGD On Resistance				470	Ω
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 2)	–12	–9	–5	%
Hysteresis			20		mV
Enable Pin					
Pull Up Current	VEN = 2.5V	–80	–50	–20	µA
Voltage Error Amplifier					
Input Offset Voltage	VCM = 3V	–10	0	10	mV
Input Bias Current	VCM = 3V	–0.5		0.5	µA
Open Loop Gain	2.05V < VCOMP < 3.05V		90		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		85		dB
Output Sourcing Current	VVFB = 2V, VCOMMAND = VCOMP = 2.5V		–1.6	–0.8	mA
Output Sinking Current	VVFB = 3V, VCOMMAND = VCOMP = 2.5V		1		mA
Current Sense Amplifier					
Gain		15	16	17	V/V
Common Mode Rejection Ratio	0V < VCM < 4.5V		60		dB
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	VIS– = 2V, VISOUT = VIS+ = 2.5V		–4	–3	mA
Output Sinking Current	VIS– = 3V, VISOUT = VIS+ = 2.5V	3	4		mA
Current Amplifier					
Input Offset Voltage	VCM = 3V		1		mV
Input Bias Current	VCM = 3V		–0.1		µA
Open Loop Gain	1V < VCAO < 2.5V		90		dB
Output Voltage High			3		V
Power Supply Rejection Ratio	10.8V < VIN < 15V		80		dB
Output Sourcing Current	VCAM = 2V, VCAO = VCOMP = 2.5V		–7		mA
Output Sinking Current	VCAM = 3V, VCAO = VCOMP = 2.5V		17		mA
Oscillator					
Initial Accuracy	TA = 25°C	324	360	396	kHz
	0°C < TA < 70°C	300	360	420	kHz
Valley to Peak Voltage			1.67		V
Frequency Change With Voltage	10.8V < VIN < 15V		1		%
Output Section (GATEHI and GATELO)					
Output Low Voltage	IGATE = –100mA		0.2		V
Output High Voltage	IGATE = 100mA		11.8		V
Rise Time	CGATE = 3.3nF, RSERIES = 10Ω		20	80	ns
Fall Time	CGATE = 3.3nF, RSERIES = 10Ω		15	80	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = VDRVHI = VDRVLO = 12V, VSNS = 3.5V, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = V_{D4} = 0V$, $R_T = 13k$, $C_T = 1.8nF$, EN = Open, $0°C < T_A < 70°C$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Turn On Delay					
GATEHI Turn Off to GATELO Turn On			150		ns
GATELO Turn Off to GATEHI Turn On			135		ns
Foldback Current Limit					
Clamp Level	$V_{COMMAND} = V_{SNS}$ $V_{FB} = V_{COMMAND} - 100mV$ (Note 3)		1.37		V
	$V_{SNS} = 0$ $V_{FB} = V_{COMMAND} - 100mV$ (Note 3)		0.71		V
System Short Circuit Current Limit	$V_{COMMAND} = 2.3V$ $V_{FB} = 0V$ (Note 4)	14.4	17	22	A

Note 1: This test measures the combined errors of the COMMAND voltage and the voltage amplifier offset voltage. Applies to all DAC codes from 1.8V to 3.5V.

Note 2: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D4 pins.

Note 3: This voltage is measured with respect to the COMMAND voltage.

Note 4: The calculation of this parameter assumes an offchip sense resistor value of 0.005Ω. This test encompasses all sources of error from the IC.

PIN DESCRIPTIONS

CAM: This pin is the inverting input to the current amplifier. The average load current feedback from the ISOUT pin is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO: This pin is the current amplifier output. The current loop compensation network is connected between this pin and the CAM pin. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The voltage at this output ranges from below 0.5V (forcing 0% duty cycle) to above 2.5V forcing maximum duty cycle. A 3V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage, for excellent transient response.

COMP: This pin is the voltage error amplifier output voltage. The system voltage compensation network is applied between COMP and VFB. A 1.37V clamp above COMMAND is used to force the power supply into current limit mode when the output is short circuited. See the Applications Section for programming current limit.

COMMAND: This pin is the output of the 5-bit digital-to-analog (DAC) converter and is the non-inverting input of the voltage error amplifier. The voltage on this pin sets the switching regulator output voltage. The COMMAND voltage is set by the DAC input pins D0-D4, according to Table 1. The COMMAND source impedance is typically 1.2kΩ and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01μF, low ESR, low ESL capacitor for best circuit noise immunity.

CT: This pin is used with RT to program the internal PWM oscillator frequency. Use a high quality capacitor for best oscillator accuracy. See the Applications Section for programming the oscillator.

D0-D4: These are the digital input control codes for the DAC (See Table 1). The DAC is comprised of two ranges set by D4 and with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal pull up.

EN: This input is used to disable the GATEHI and GATELO outputs, resulting in disabling the power supply. Pulling EN to GND causes the GATEHI and GATELO outputs to be held low, while floating the pin or pulling it up to 5V ensures normal operation. EN is pulled up to 5V internally.

GATEHI: This output provides a low impedance totem pole driver to drive the high-side external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATEHI from ringing more than 0.3V below PGND. The VDRVHI pin provides the power for the GATEHI pin. GATEHI is disabled during UVLO and overvoltage conditions. For the 2882/3882 only, GATEHI is also disabled when the COMMAND voltage is programmed between 1.3 and 1.75V, or where the D0-D4 pins are all logic high levels, indicating no processor present.

PIN DESCRIPTIONS (continued)

GATELO: This output provides a low impedance totem pole driver to drive the low-side synchronous external MOSFET. A series resistor between this pin and the gate of the external MOSFET is recommended to prevent gate drive ringing and overshoot. Good layout techniques should be used to prevent GATELO from ringing more than 0.3V below PGND. The VDRVLO pin provides the power for GATELO. GATELO is disabled during UVLO conditions. For the 2882/3882 only, GATELO is also disabled when the COMMAND voltage is programmed between 1.3 and 1.75V, or where the D0-D4 pins are all logic high levels, indicating no processor present.

GND: Ground reference for the device. All voltages, with the exception of the GATE voltages, are measured with respect to GND. Bypass capacitors on VIN, VREF, VSNS and COMMAND should be connected directly to the ground plane near GND.

IS-: This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+: This pin is the non-inverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT: This pin is the output of the current sense amplifier. The voltage on this pin is equal to the voltage across the sense resistor multiplied by 16 and biased up by the COMMAND voltage. This voltage is used for Average Current mode control and for current limiting.

PGND: This pin provides a dedicated ground for the output gate drivers. The GND and PGND pins should be connected externally using a short PC board trace or plane. Decouple VDRVHI and VDRVLO to PGND with low ESR capacitor of at least 0.1µF.

PWRGD: This pin is an open drain output which is driven low to reset the microprocessor when VSNS rises above or falls below its nominal value by 9%. The on resistance of the open-drain switch will be no higher than 470Ω. This output should be pulled up to a logic level voltage and should be programmed to sink 1mA or less.

RT: This pin is used with CT to program the internal PWM oscillator frequency. It is also used to program the delay times between the external MOSFET turn on and turn off periods, which eliminates cross conduction in those MOSFETs. See the Applications Section for programming the oscillator and for controlling cross conduction.

VDRVHI: This pin supplies power to the high side output driver, GATEHI. Connect VDRVHI to an 18V or lower source for power supplies converting 12VDC to lower voltages, and to a 12V source for systems for power supplies converting 5VDC. This pin should be bypassed directly to PGND using a low ESR capacitor.

VDRVLO: This pin supplies power to the low side output driver, GATELO. VDRVLO is typically connected to a 12V source, but may be connected to a 5V source for driving logic level MOSFETs. This pin should be bypassed directly to PGND using a low ESR capacitor.

VIN: This pin supplies power to the chip. Connect VIN to a stable voltage source that is at least 10.8V above GND. The GATEHI, GATELO and PWRGD outputs will be held low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to GND.

VFB: This pin is the inverting input to the error amplifier. This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF: This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A Converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSNS: This pin is connected to the system output voltage through a low pass R-C filter. When the voltage on VSNS rises above or falls below the COMMAND voltage by 9%, the PWRGD output is driven low to reset the microprocessor. When the voltage on VSNS rises above the COMMAND voltage by 17.5%, the OVP comparator disables the GATEHI output and enables the GATELO output, forcing 0% duty cycle on the power supply. This pin is also used by the foldback current limiting circuitry to indicate when the output voltage has been short circuited. VSNS should be decoupled very closely to the IC with a capacitor to GND. The OV and UV comparators' hysteresis is typically 20mV, requiring good layout and filtering techniques to insure that noise and ground-bounce do not inadvertently trip the OV and UV comparators. It is recommended that an R-C filter set to approximately Fs/10 be used to filter noise from the system output, where Fs is the oscillator frequency.

DAC INFORMATION

The 5-bit Digital-to-Analog Converter (DAC) is programmed according to Table 1.The COMMAND voltage is always active as long as the UCC3882 VIN pin is above the undervoltage lockout voltage. For the 2882/3882 only, the output gate drives GATEHI and GATELO are disabled at certain DAC codes, as shown in Table 1. Disabling the gate drives disables the power supply. For the 2882 -1 and 3882 -1, the GATEHI and GATELO drives are enabled for all DAC codes. For a given code, the power supply output regulates at the corresponding COMMAND voltage.

Digital Command					Command	GATEHI/GATELO	Digital Command					Command	GATEHI/GATELO
D4	D3	D2	D1	D0	Voltage	Status	D4	D3	D2	D1	D0	Voltage	Status
0	1	1	1	1	1.300	Note 1	1	1	1	1	1	2.000	Note 1
0	1	1	1	0	1.350	Note 1	1	1	1	1	0	2.100	Enabled
0	1	1	0	1	1.400	Note 1	1	1	1	0	1	2.200	Enabled
0	1	1	0	0	1.450	Note 1	1	1	1	0	0	2.300	Enabled
0	1	0	1	1	1.500	Note 1	1	1	0	1	1	2.400	Enabled
0	1	0	1	0	1.550	Note 1	1	1	0	1	0	2.500	Enabled
0	1	0	0	1	1.600	Note 1	1	1	0	0	1	2.600	Enabled
0	1	0	0	0	1.650	Note 1	1	1	0	0	0	2.700	Enabled
0	0	1	1	1	1.700	Note 1	1	0	1	1	1	2.800	Enabled
0	0	1	1	0	1.750	Note 1	1	0	1	1	0	2.900	Enabled
0	0	1	0	1	1.800	Enabled	1	0	1	0	1	3.000	Enabled
0	0	1	0	0	1.850	Enabled	1	0	1	0	0	3.100	Enabled
0	0	0	1	1	1.900	Enabled	1	0	0	1	1	3.200	Enabled
0	0	0	1	0	1.950	Enabled	1	0	0	1	0	3.300	Enabled
0	0	0	0	1	2.000	Enabled	1	0	0	0	1	3.400	Enabled
0	0	0	0	0	2.050	Enabled	1	0	0	0	0	3.500	Enabled

Table 1. Programming the Command Voltage for the UCC3882

APPLICATION INFORMATION

This IC is intended to be used in a high performance power supply to power the Pentium® II or a similar processor. Figure 1 shows a typical power supply application circuit which converts +5V to lower voltages required by the Pentium® II Processor.

Synchronous Switching Delay Time

Figure 2 shows that the fundamental difference between a Buck and a Synchronous Buck regulator is the use of a MOSFET rather than a Schottky diode as the low side or free-wheeling switch.

In order to maintain safe and efficient operation of a Synchronous Buck regulator, both MOSFETs, Q1 and Q2, should never be turned on at the same time. Having both MOSFETs on at the same time results in cross conduction, which can result in excessively high power dissipation in one or both MOSFETs. The UCC3882 has a built in delay between the turn OFF of one MOSFET and the turn ON of the other MOSFET. This delay is a controlled delay between the GATEHI and GATELO drive outputs and is programmable by the selection of the resistor R_T. Controlling the delay between the gate drive outputs is only part of the solution. The power supply designer must also understand intrinsic delays involving MOSFET turn on, turn off, rise and fall times in order to insure that there is no cross conduction.

It is recommended that a value between 10kΩ and 15kΩ be used for R_T, which minimizes the delay and can result in the highest efficiency operation. A higher value of R_T will result in a larger delay between the MOSFET Gate transitions. R_T should be between 10kΩ minimum and 50kΩ maximum.

Programming the Oscillator

The first step in programming the oscillator is choosing the value of R_T as described above. The second step is to program the frequency according to the curves shown in Figure 3, by choosing the appropriate capacitor value.

For convenience, values are shown in Table 1 for nominal frequencies from 100kHz to 700kHz using standards resistors and capacitor values.

APPLICATION INFORMATION (continued)

FREQUENCY	RT	CT
(kHz)	(kΩ)	(pF)
100	14.7	5600
200	11.0	3900
300	10.5	2700
400	11.3	1800
500	12.7	1200
600	10.7	1200
700	11.0	1000

Table 2. Programming Standard Frequencies

An excessively long delay time between gate drive signals, or a delay time that is too small, will result in a inefficient power supply design. The third step in programming the oscillator is to observe the actual circuit waveforms to insure that the delay is optimal. The designer should vary RT and CT accordingly to adjust the delay time and to program the proper oscillator frequency.

Using an External Schottky Diode in Parallel With the Low Side MOSFET

The purpose of using a synchronous buck regulator is to substitute a low voltage drop MOSFET in place of a Schottky diode as the low side switch. An external Schottky diode may still be required however, in order to reduce the losses due to the reverse recovery of the low-side MOSFET body diode. Figure 4 illustrates the effects on power losses due to the non-ideal nature of a typical MOSFET body diode. IRM is the peak recovery current of the body diode of Q2 and ILOUT is the current of the output inductor. Using a parallel Schottky diode can reduce these losses and increase circuit efficiency. The size of the diode should be increased as a function of load current, input voltage, and operating frequency. The diode should be as close to the lower MOSFET, Q2, as possible, to reduce stray inductance.

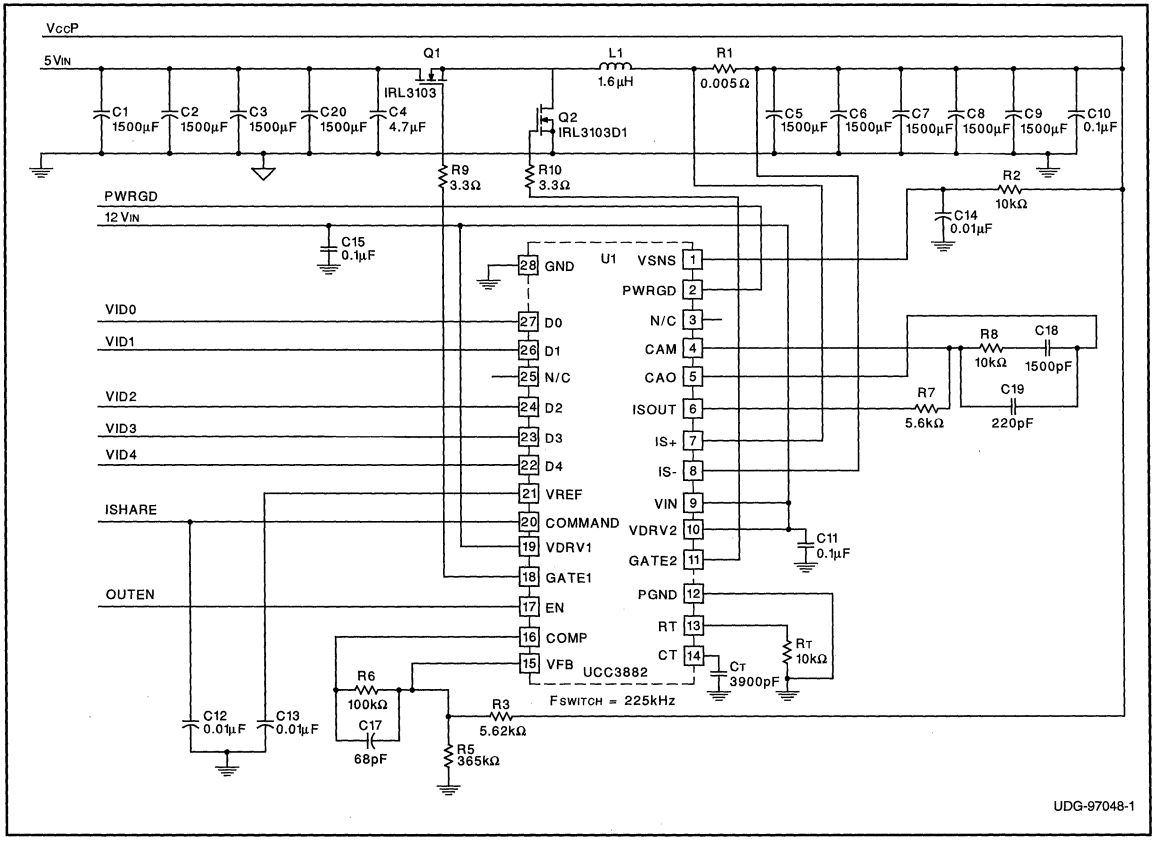


Figure 1. Application circuit - Pentium® II power supply.

APPLICATION INFORMATION

Choosing RSENSE to Set the Current Limit

RSENSE is chosen to limit the maximum (short circuit) current of the power supply. The short circuit current equation for the UCC3882 is:

$$ISC = \frac{1.37V}{RSENSE \bullet 16}$$

and therefore, the value of the sense resistor, for a chosen short circuit current is:

$$RSENSE = \frac{1.37V}{ISC \bullet 16}$$

The short circuit current limit does vary slightly as a function of the switching regulator's output inductor value and operating frequency because a high value of ripple current will reduce the average short circuit current limit. Figure 5 shows the variation in Isc given common values for the UCC3882. The UCC3882 is nominally configured so that a 0.005mΩ resistor will set the current limit to approximately 17A.

The UCC3882 incorporates short circuit current foldback, as shown in Figure 6. When the output of the power supply is short circuited, the output voltage falls. When the output voltage reaches 1/2 of its nominal voltage (COMMAND/2) then the output current is reduced. This feature reduces the amount of current in the MOSFETs and capacitors, and insures high reliability.

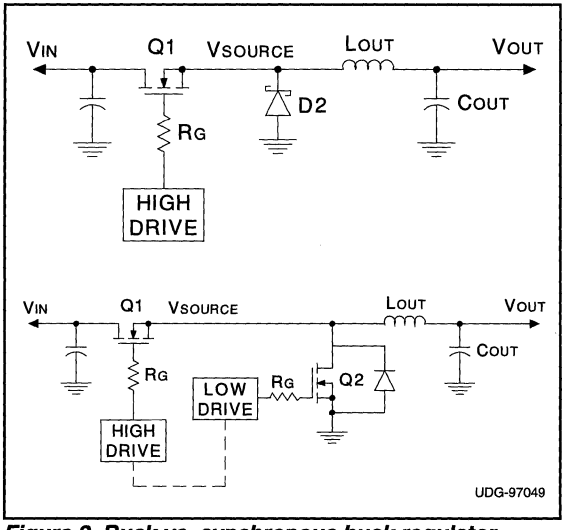


Figure 2. Buck vs. synchronous buck regulator.

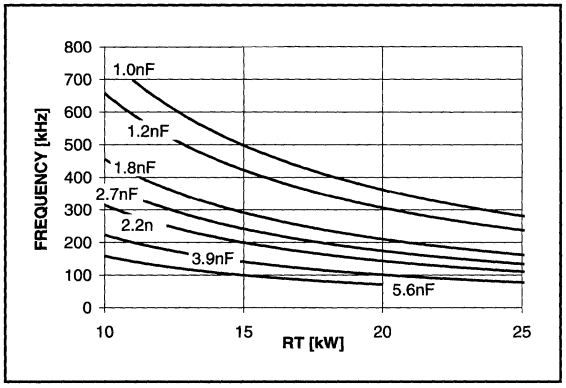


Figure 3. Programming UCC3882 oscillator frequency.

Choosing VDRVLO, VDRVHI and VIN

The UCC3882 requires a nominal 12V input supplied at VIN. VDRVLO and VDRVHI can be set to any voltage less than 18.5V, and may be set individually. A power supply deriving its power from +5V should use +12V at the VDRVHI pin, but may use either +5V or +12V depending on the drive requirements of the synchronous low-side MOSFET. A power supply deriving its power from +12V should use +18V at VDRVHI in order to provide adequate voltage (6V) gate drive to the high-side MOSFET. VIN must be less than +15V.

Input Capacitors

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability and their voltage rating. The input capacitors must handle virtually all of the RMS current at the switching frequency, even if the circuit does not have an input inductor. The switching current in the input capacitors appears as shown in Figure 7.

Aluminum or tantalum capacitors can be used. The amount of RMS current in an Electrolytic capacitor has a strong impact on the reliability and lifetime of the capacitor. Other factors which affect the life of an input capacitor are internal heat rise, external airflow, the amount of time that the circuit operates at maximum current and the operating voltage. The curves in Figure 8 show the RMS current handled by the total input capacitance in typical VRM circuits powered from 5V or from 12V.

APPLICATION INFORMATION (continued)

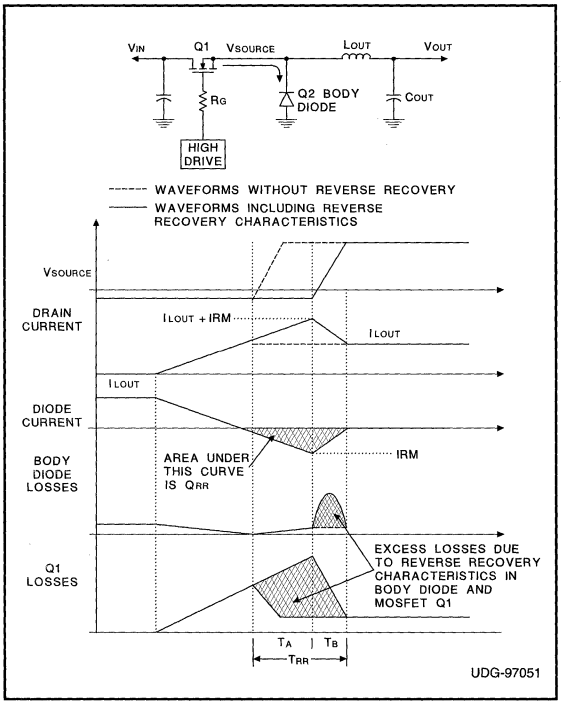


Figure 4. Effects of reverse recovery in a synchronous rectifier.

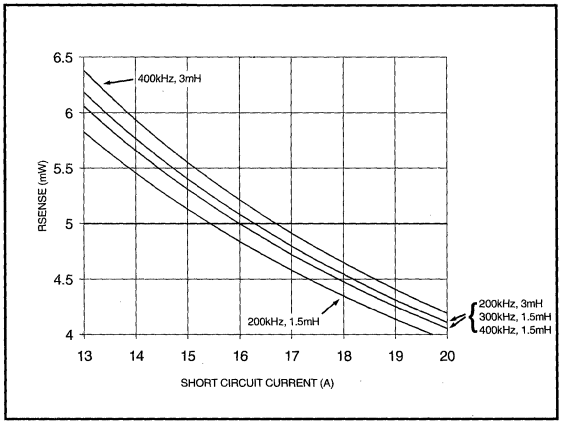


Figure 5. Short circuit current limit vs. RSENSE for various frequency and inductor values.

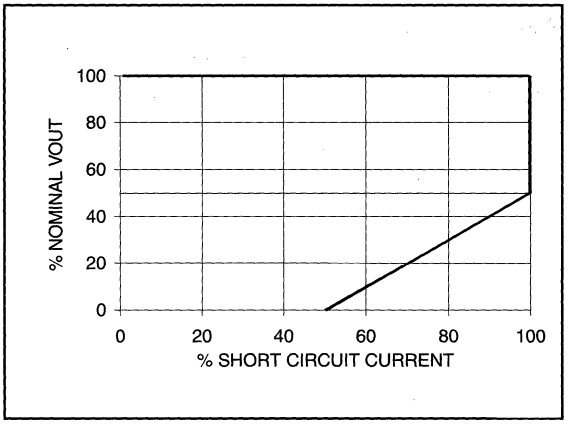


Figure 6. Short circuit foldback reduces stress on circuit components by reducing short circuit current.

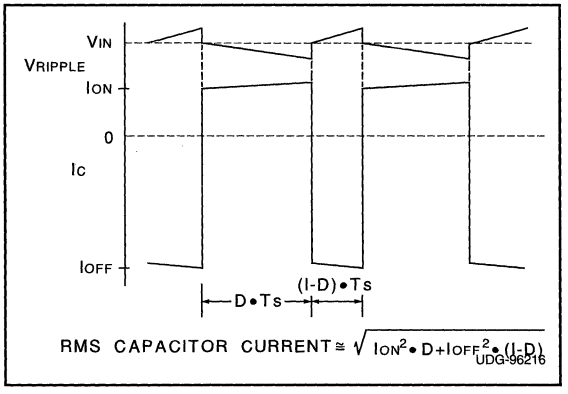


Figure 7. Input capacitors current waveform.

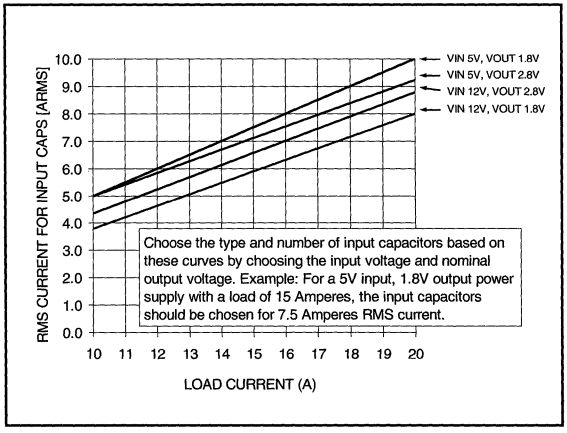


Figure 8. Load current vs RMS current for input capacitors - Pentium® II Family.

APPLICATION INFORMATION (continued)

Demonstration Kit Design and Performance

A demonstration circuit was built based on the UCC3882 and utilizing an Intel VRM 8.1 form factor connector. The schematic is shown in Figure 9 and the Bill of Materials in Table 3. The circuit is configured for the following operating parameters:

- Switching Frequency = 225kHz
- Rated Output Current = 15A
- Short Circuit Current = 17A Nominal
- Output Voltage: 1.8V to 2.8V Configured by VID Code
- Airflow: 100 LFM
- Temperature: 0 to 60°C
- Regulation: Per Intel VRM 8.1 DC-DC Converter Design Guidelines

Figures 12 - 14 show the performance of the circuit.

REF	DESCRIPTION	PACKAGE
U1	Unitrode UCC3882 DAC/PWM	SOIC-28 WIDE
C01	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C02	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C03	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C04	Sprague/Vishay 595D475X0016A2B, 4.7uF 16V Tantalum	SPRAGUE Size A
C05	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C06	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C07	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C08	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C09	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	0.10µF Ceramic	1206 SMD
C11	0.10µF Ceramic	1206 SMD
C12	0.01µF Ceramic	0603 SMD
C13	0.01µF Ceramic	0603 SMD
C14	0.01µF Ceramic	0603 SMD
C15	0.10µF Ceramic	1206 SMD
C17	68pF NPO Ceramic	0603 SMD
C18	1000pF Ceramic	0603 SMD
C19	220pF NPO Ceramic	0603 SMD
C20	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
CT	3900pF Ceramic	0603 SMD
J1	AMP 532956-7 40 Pin Connector	40 Pin
L1	Toroid T51-52C, 5 Turns #16AWG, 1.6µH	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB, layed down
Q2	International Rectifier IRL3103D1, 30V, 56A	TO-220AB, layed down
R01	5mΩ, PCB Resistor	Copper Trace
R02	10kΩ, 5%, 1/16 Watt	0603 SMD
R03	5.62kΩ, 1%, 1/16 Watt	0603 SMD
R05	365kΩ, 1%, 1/16 Watt	0603 SMD
R06	100kΩ, 5%, 1/16 Watt	0603 SMD
R07	5.6kΩ, 5%, 1/16 Watt	0603 SMD
R08	10kΩ, 5%, 1/16 Watt	0603 SMD
R09	3.3Ω, 5%, 1/16 Watt	0603 SMD
R10	3.3Ω, 5%, 1/16 Watt	0603 SMD

Table 3. Bill of materials.

APPLICATION INFORMATION (continued)

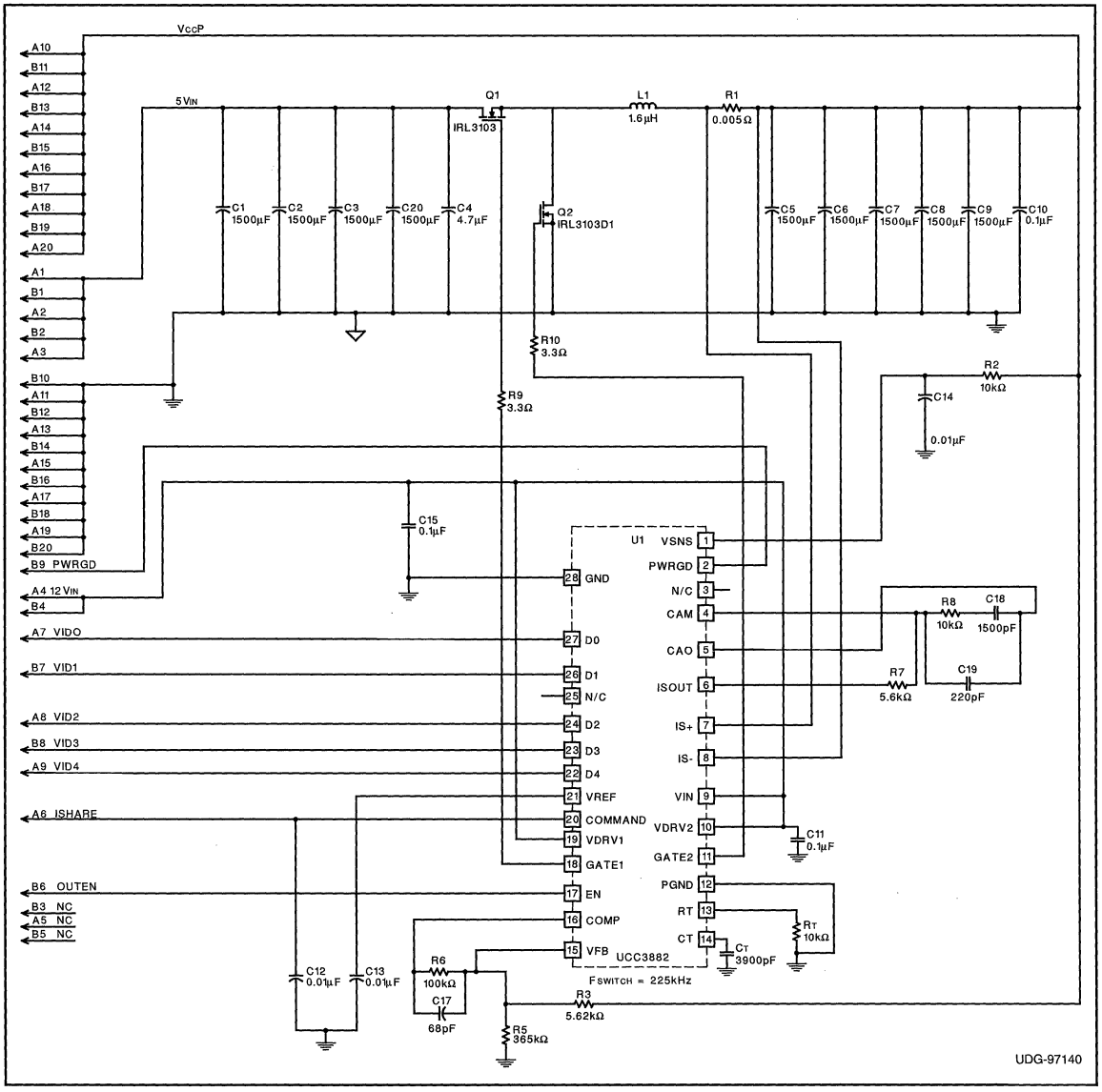


Figure 9. Reference design - UCC3882 5-bit synchronous rectifier PWM controller for the Intel Pentium®II processor.

APPLICATION INFORMATION (continued)

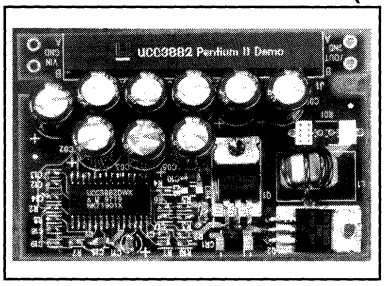


Figure 10. Demo board.

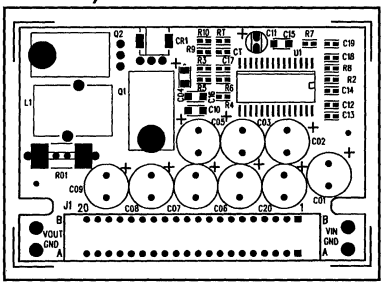


Figure 11a. COMP silkscreen.

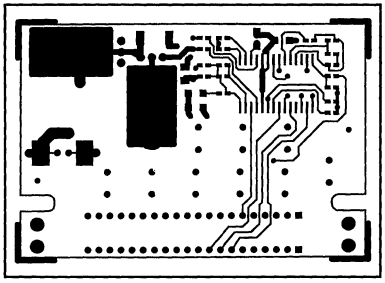


Figure 11b. COMP side.

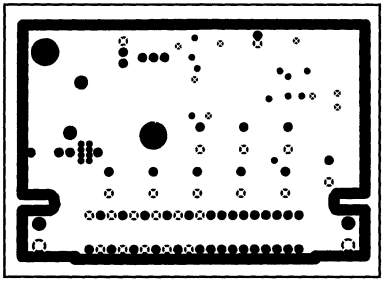


Figure 11c. GND layer.

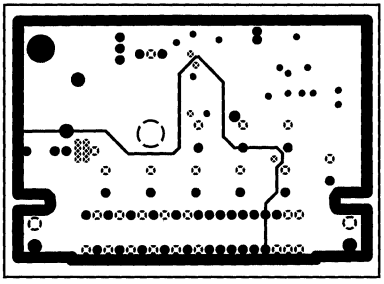


Figure 11d. PWR layer.

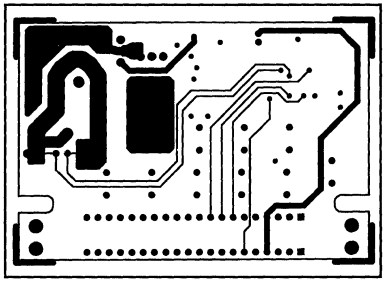
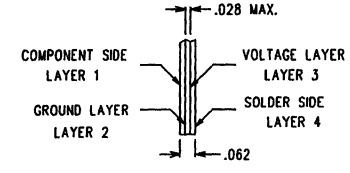
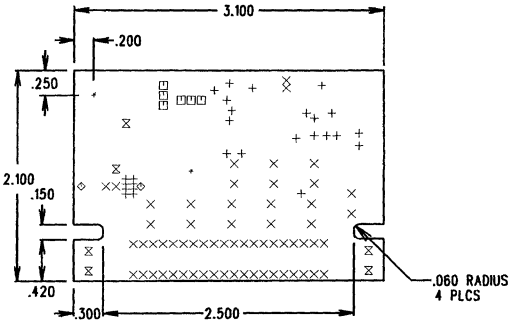


Figure 11e. Solder side.



1 OZ. CU. INNER LAYERS, 1 OZ. CU. OUTER LAYERS



DRILL DRAWING
UCC3882 BOARD

NOTES:

1. MAT'L: .062 THK. FR4 COPPERCLAD LAMINATE
2. ALL HOLES TO BE PLATED THRU WITH A MINIMUM WALL THICKNESS OF .001 AND A SOLDER COATING OF .0003.
3. BOARDS TO BE SOLDERMASKED BOTH SIDES LPI OBC.
4. BOARDS TO BE SILKSCREENED ON BOTH SIDES WITH PERMANENT, WHITE EPOXY (CHEMICAL AND SCRATCH RESISTANT).
5. BOARDS SHALL BE MADE FROM UNDERWRITER LABORATORY RECOGNIZED MATERIAL AND THE FINISHED BOARD MUST CARRY THE VENDER'S U.L. LOGO.
6. ALL DRAWINGS AND FILMS VIEWED FROM COMPONENT SIDE.

DRILL CHART			
SYMBOL	SIZE	QTY	PLATED TYPE
+	.016	27	PLATED
×	.037	62	PLATED
□	.045	6	PLATED
◇	.050	2	PLATED
⧖	.070	6	PLATED
A	.156	2	PLATED

Figure 11f. Drill drawing.

APPLICATION INFORMATION (cont.)

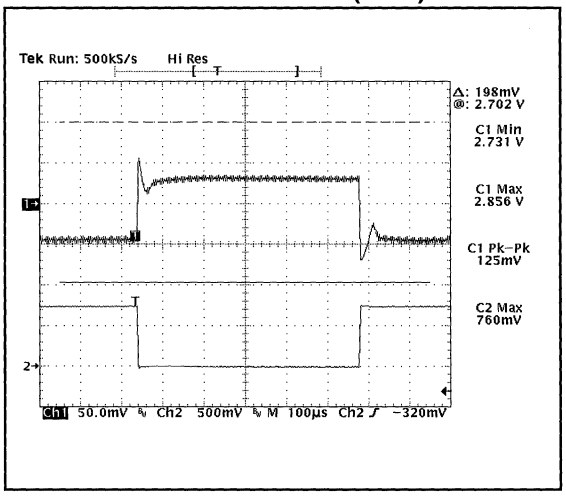


Figure 12. Transient response to 15.2A step load channel 2 scale is 50mV/A.

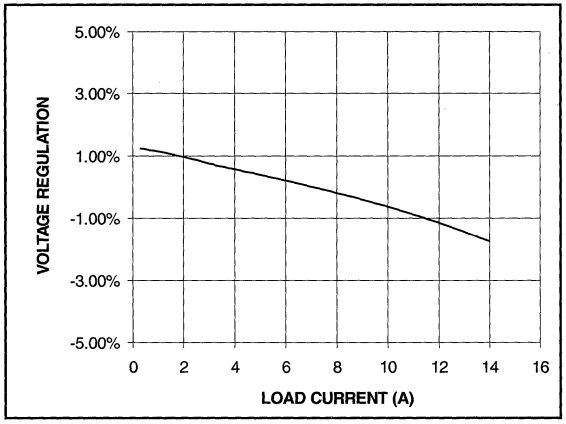


Figure 14. Load regulation.

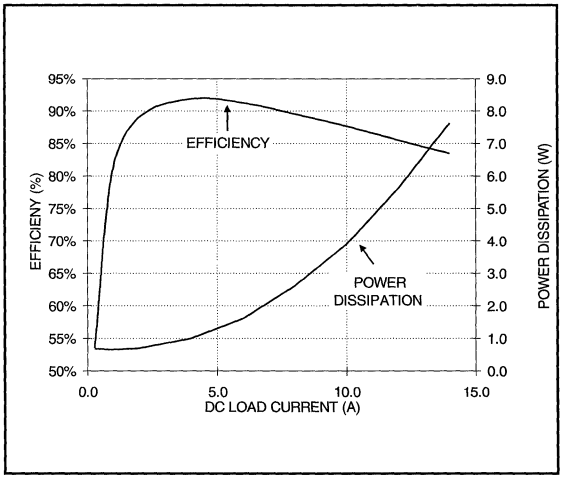


Figure 13. UCC3882 demo kit efficiency.

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UNITRODE

application INFO available

UCC1884
UCC2884
UCC3884
PRELIMINARY

Frequency Foldback Current Mode PWM Controller

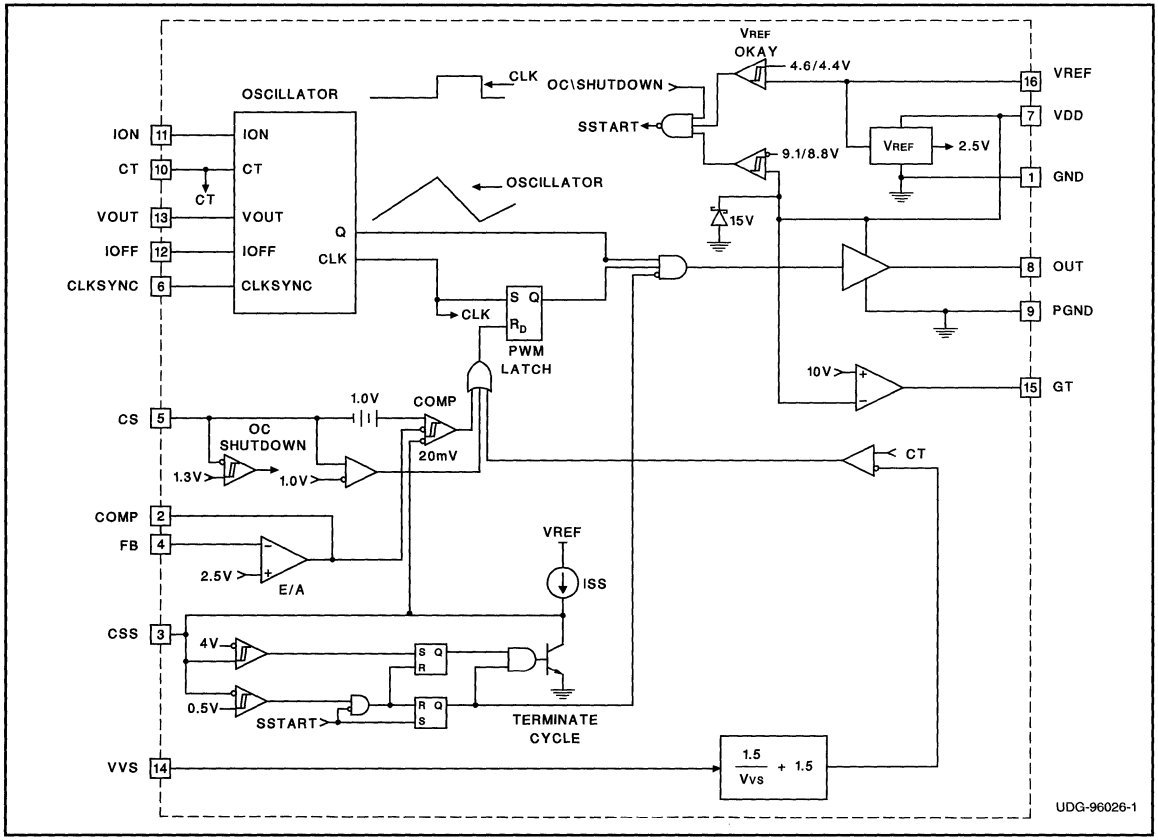
FEATURES

- Frequency Foldback Reduces Operating Frequency Under Fault Conditions
- Accurate Programmable Volt-Second Clamp
- Programmable Maximum Duty Cycle Clamp
- Oscillator Synchronization
- Overcurrent Protection
- Shutdown with Full Soft Start
- Wide Gain Bandwidth Amplifier (GBW > 2.5MHz)
- Current Mode Operation
- Precision 5V Reference

DESCRIPTION

The UCC3884 is a high performance current mode PWM controller intended for single ended switch mode power supplies. The chip implements a frequency foldback scheme that decreases the oscillator frequency as the output voltage falls below a programmed value. This technique decreases the average output current sourced into a low impedance load which can occur during an output short circuit or overload condition. Excessive short circuit current is more prevalent in high frequency converters where the propagation delay and switch turn-off time forces a minimum attainable duty cycle. An accurate volt-second clamp limits the duty cycle during line or load transient conditions which could otherwise saturate the transformer. The volt-second clamp may also be used with an external overvoltage protection circuit to handle fault conditions such as current sense disconnect or current transformer saturation. The frequency foldback, volt-second clamp, cycle-by-cycle current limit, and overcurrent shutdown provide a rich set of protection features for use in peak current mode pulse width modulators.

BLOCK DIAGRAM

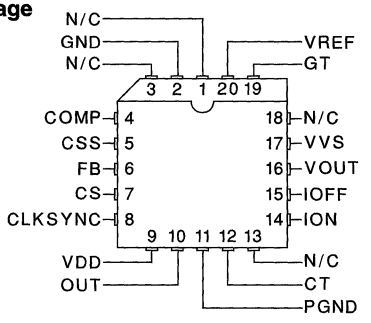


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 15V
Output Sink Current 1A
Output Source Current 0.5A
All Other Pins 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

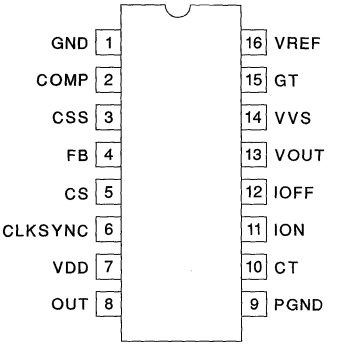
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

PLCC-20 (Top View)
Q Package



CONNECTION DIAGRAMS

DIL-16, SOIC-16 (Top View)
J, N or D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications apply for T_A = –55°C to 125°C for the UCC1884, –40°C to 85°C for the UCC2884, and 0°C to 70°C for the UCC3884, CT = 220pF, R_{ON} = 53k, R_{OFF} = 38k, VOUT = VREF, VVS = 0V, CSS = 2.5nF, VDD = 11V, Output no load, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
5V Reference Section					
VREF	I_{REF} = 0mA	4.86	5	5.14	V
Line Regulation	VDD = 10V to 12V		1	10	mV
Load Regulation	0 < I_{REF} < 5mA		1	20	mV
Short Circuit I	VREF = 0V		15	45	mA
Oscillator Section					
Accuracy	$V_{OUT} = V_{REF}$	360	400	440	kHz
Foldback Frequency	VOUT = 0.75V	200	230	260	kHz
CLKSYNC Output High		4.8	5	5.2	V
CLKSYNC Output Low			0.0	0.4	V
CLKSYNC Sink Current	CLKSYNC = 1V	1.2	2.2		mA
CLKSYNC Source Current	CLKSYNC = 3V		–0.2	–0.1	mA
CLKSYNC Input Threshold	CLKSYNC from 5V to 0V (Edge Detect)	2.5	3.0	3.5	V
Error Amplifier Section					
I_B	Total Bias Current; Regulating Level	–1		1	µA
FB Voltage	FB = COMP	2.43	2.5	2.57	V
Avo		50	90		dB
GBW	F = 100kHz (Note 1)	2.5	5		MHz
Output Source Current	FB = 2.3V, COMP = 2.5V	–0.6	–1.2		mA
Output Sink Current	FB = 2.7V, V_{COMP} = 1V	0.250	1.5		mA
V_{OL}	I_O = 100µA		0.3	0.9	V
V_{OH}	I_O = –100µA	2.7	3.1	3.5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications apply for T_A = –55°C to 125°C for the UCC1884, –40°C to 85°C for the UCC2884, and 0°C to 70°C for the UCC3884, CT = 220pF, R_{ON} = 53k, R_{OFF} = 38k, VOUT = VREF, VVS = 0V, CSS = 2.5nF, VDD = 11V, Output no load, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Section					
Minimum Duty Cycle	FB = 3V, CS = 0V			0	%
Maximum Duty Cycle	FB = 0V, CS = 0V	75	78	81	%
Current Sense Section					
Input Bias Current (CS)				3.0	µA
CS Shutdown Threshold		1.235	1.3	1.365	V
CS Shutdown Hysteresis			20		mV
CS Over Current Threshold		0.95	1	1.05	V
Current/Fault Section					
Soft Start Charge Current		–10	–20	–30	µA
Soft Start Discharge Current		10	20	30	µA
V_{OL}			0	50	mV
Soft Start Complete Threshold		3.6	4	4.4	V
Soft Start Restart Threshold		0.4	0.5	0.6	V
Volt Second Clamp					
Duty Cycle	VVS = 1.4V, T_A = 0°C to 70°C	53.8	56.8	59.8	%
	VVS = 3.6V, T_A = –55°C to 125°C	19.8	22	25.8	%
	VVS = 3.6V, T_A = –40°C to 85°C	20.9	22	24.5	%
	VVS = 3.6V, T_A = 0°C to 70°C	21	22	23	%
I_B	VVS = 3.7V	–1		+1	µA
Output Stage					
Output Low Saturation	I_{OUT} = 100mA		0.5	0.9	V
Output High Saturation	I_{OUT} = –50mA		0.5	0.9	V
	I_{OUT} = –200mA			1.9	V
UVLO Output Low Saturation	I_{OUT} = 20mA, VDD = 0V		0.7	1.2	V
Rise Time	CL = 1nF		50	70	ns
Fall Time	CL = 1nF		30	50	ns
Undervoltage Lockout					
Turn-On Threshold Voltage		8.4	8.9	9.4	V
Hysteresis		200	600	1000	mV
Startup Regulator					
Regulated VDD Voltage		9.5	10	10.5	V
VDD Override Threshold				10.7	V
Overall					
V_{DD} Range				14.5	V
I_{DD} (run)	f = 400kHz	2	5	10	mA
I_{DD} Startup Current	VDD = 5.4V			250	µA
VDD Clamp	IDD = 10mA	12	13.5	15	V

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLKSYNC: An edge triggered active low TTL signal to this pin synchronizes the oscillator to an external clock. When VOUT decreases below 3.0V, the frequency foldback circuit is activated and the controller becomes unsynchronized. When VOUT exceeds 3.0V, the controller resynchronizes to the external clock.

COMP: The output of the voltage error amplifier used for compensation. The output is clamped to 3.0V minimum.

CS: Current sense input. This pin accepts a voltage proportional to converter inductor current. The voltage at CS is compared to the output of the compensated error amplifier to control the on-time of the switch. Voltage mode control can be realized by driving this pin with a fixed sawtooth ramp. Voltage feedforward is achieved by making the peak of this ramp proportional to the input voltage.

CSS: A capacitor, C_{SS}, to ground programs the soft start time for the power up sequence. This function is also used when an overcurrent fault occurs. As CSS is charged, the PWM comparator uses the lowest of either the voltage at CSS or the error amplifier output voltage to determine the duty cycle. The duty cycle, therefore, slowly increases during the soft start cycle. The faults that cause CSS to discharge and shutdown the controller are the logical OR of VREF below 4.4V or VDD below 8.8V. If a fault is still present when CSS is discharged below 0.5V, the supply remains off until the fault is cleared. The soft start time is determined by:

$$T_{SS} = 3.5 \bullet \frac{C_{SS}}{I_{SS}}$$

where I_{SS} is 20µA. A current limit terminates the present cycle. It does not generate a soft start cycle.

CT: A capacitor, C_T to ground, is charged and discharged creating the oscillator waveform. This waveform varies between 1.5V and 3.5V. The operating frequency is determined by:

$$f = \frac{4.4}{C_T \bullet \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5} \right)}$$

The ratio of the time duration of the positive sloped portion of the CT voltage waveform to the period gives the maximum duty cycle.

FB: The inverting input of the voltage amplifier used to sense the output voltage. The non-inverting input of the error amplifier is internally connected to 2.5V.

GND: The ground pin internally used for all the amplifiers and as the return for all resistor and capacitor connections to the UCC3884.

GT: Used to drive an external depletion-mode MOSFET for the housekeeping power supply. The MOSFET is turned off when the bootstrap winding voltage exceeds 10V. There is 300mV of hysteresis around the 10V turn-off voltage to prevent oscillation. See Typical Application.

IOFF: A resistor, R_{OFF}, to ground, programs the discharge current of the timing capacitor C_T. This is a variable discharge current which determines the negative slope of the oscillator voltage waveform at CT. The discharge time is dependent on the voltage at the VOUT pin. The discharge current is given by I_{OFF} = VOUT/R_{OFF}. The VOUT pin is internally clamped to 3.5V maximum.

ION: A resistor, R_{ON}, to ground programs the charge current of the timing capacitor, C_T, which generates the positive slope of the oscillator waveform. The charge time is constant and corresponds to the maximum output on-time at OUT. The charge current equation is I_{ON} = 1.5V/R_{ON}. When required the linear positive slope of the C_T voltage could be buffered and used to provide slope compensation into the CS pin.

OUT: The output of the controller. The peak source current is 0.5A and the peak sink current is 1.0A. The faults listed under the CSS description turn off this output.

PGND: The power ground pin is used as the return for the output transistor drive stage.

VDD: The input voltage of the chip. A low ESR and ESL ceramic capacitor from this pin to GND should be used to bypass internal switching transients.

VOUT: This pin accomplishes frequency foldback by controlling the discharge current for the oscillator C_T capacitor. A dc voltage proportional to the output voltage is connected to this pin. To startup with zero output voltage the user should tie a resistor between VREF and VOUT. The value depends on the lowest desired operating frequency. When VOUT decreases below 3.5V the frequency decreases by reducing the discharge current I_{OFF}. When VOUT increases, the frequency increases by increasing the discharge current. The maximum operating frequency occurs when VOUT = 3.5V. The C_T charge time is constant to guarantee a maximum output duty cycle. This pin must be above 3.0V to allow synchronization to occur.

PIN DESCRIPTIONS (cont.)

VREF: This pin is the output of the 5V regulated reference. Bypass this pin with a low ESR and ESL ceramic capacitor (e.g., 0.47µF).

VVS: Provides a programmable duty cycle clamp which is dependent upon the input voltage. A resistor divider network reduces the input voltage supplied to VVS. The IC determines the reciprocal of the voltage at VVS and scales the result. The voltage is then compared to the oscillator waveform to clamp the duty cycle. The purpose of this clamp is to reduce the likelihood of saturating the isolation transformer during unusual line or load conditions.

APPLICATION INFORMATION

Theory of Operation

The UCC3884 current mode PWM controller contains a programmable oscillator which includes the ability to synchronize multiple PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT), have time intervals that are set by external resistors at ION and IOFF. The operating frequency is inversely proportional to the timing capacitor. The negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. The power supply output voltage and the voltage from VREF are fed back to VOUT. When the output voltage decreases, the voltage at VOUT also decreases. As VOUT decreases below 3.5V, the operating frequency decreases. This reduction in frequency allows the duty cycle to decrease below what the CS to OUT delay would otherwise permit. This is referred to as frequency foldback. An output short circuit or overload causes the converter to enter the frequency foldback mode. Synchronization to other controllers can only occur during normal operation, that is, when VOUT is greater than 3.0V.

GT is provided to turn off an external depletion-mode MOSFET after startup when the bootstrap winding exceeds 10V. This depletion-mode MOSFET is used in the housekeeping section of the converter to simplify startup biasing circuitry. The amplifier that drives this MOSFET has 300mV of hysteresis to avoid oscillation during power up.

An accurate programmable volt-second technique clamps the duty cycle. The duty cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, under closed loop control, the operating duty cycle is a fixed value. The volt-second clamp duty cycle may then be set somewhat higher than this operating duty cycle. For other input voltages, the volt-second clamp will still exceed the steady state operating duty cycle. This allows normal closed loop operation of the converter. It is during a load transient (a fault such as a momentary short circuit) as the error amplifier increases the duty cycle, that when the volt-second clamp accurately limits the maximum volt-seconds. This ensures that the transformer does not saturate during a fault which can fail the power supply. After the fault is removed the converter resumes closed loop control.

CSS is provided which allows the UCC3884 to be disabled with an external transistor. The increasing pulse width at OUT during soft start should be programmed to be less than the pulse width of the duty cycle limit that the frequency foldback circuitry creates. The frequency foldback circuit will be in effect during soft start since the output voltage fed back to VOUT is less than 3.5V. Designing the circuit in this fashion allows a proper startup sequence.

The current sense feedback pin has an overcurrent protection feature which forces a soft start cycle only if the IC is not currently in a soft start cycle. A 1V bias at the PWM comparator's non-inverting input and a reset dominant PWM latch permit zero duty cycle operation.

The error amplifier has a wide gain-bandwidth product and its non-inverting input is internally set to 2.5VDC.

Oscillator

The oscillator has charge and discharge currents programmed with resistors to ground from ION and IOFF respectively, as seen on the Oscillator Block Diagram (Fig. 1). This generates a linear sawtooth waveform on CT. Frequency foldback is accomplished by the level shifted output voltage controlling the VOUT voltage which decreases the discharge current and the frequency.

Synchronization is accomplished by coupling the fastest oscillator CLKSYNC signal as shown on the Oscillator Synchronization Diagram (Fig. 2). The fastest (master) CLKSYNC pin will couple a negative pulse into the slower (slave) CLKSYNC pins forcing the slaves' CT pins to quickly discharge as shown on the Oscillator Waveform diagram (Fig. 3).

APPLICATION INFORMATION (cont.)

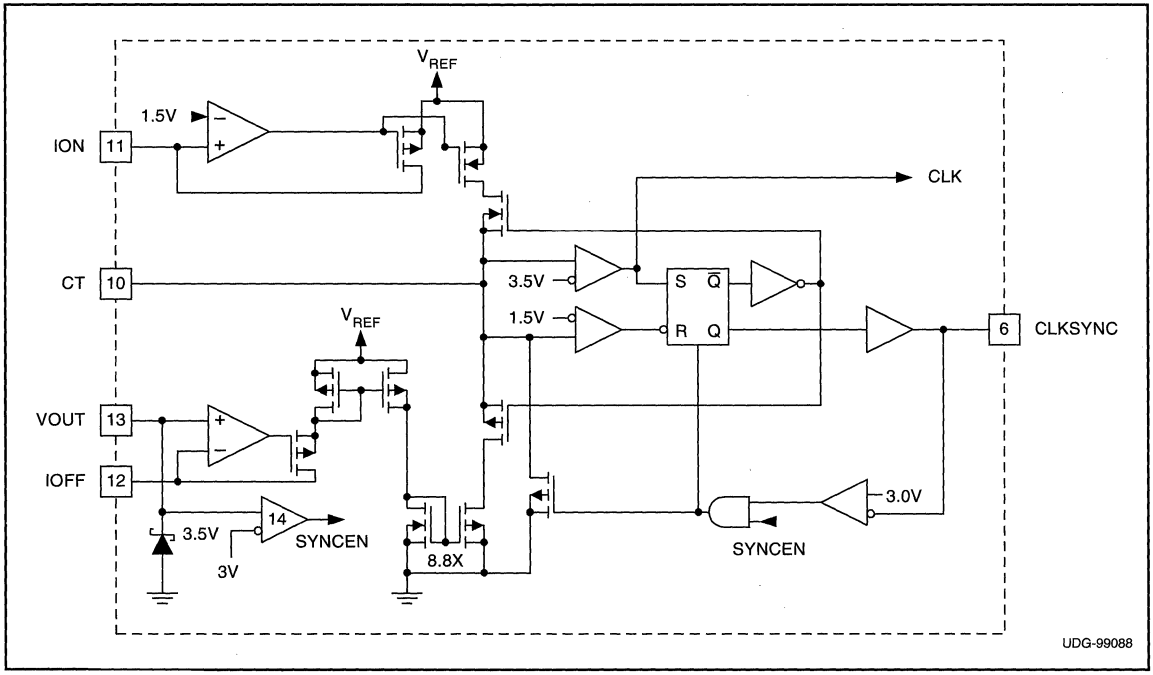


Figure 1. UCC3884 oscillator.

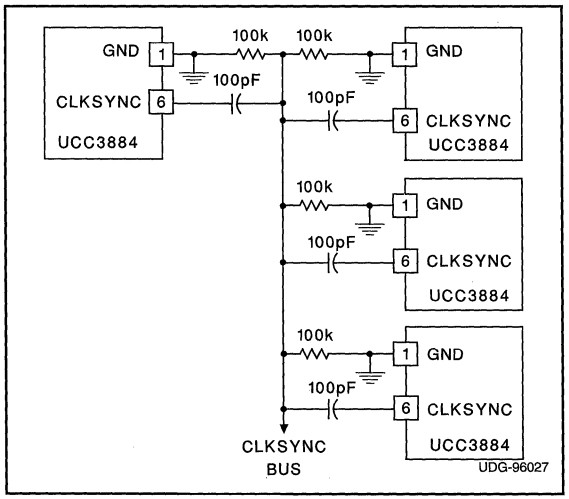


Figure 2. Oscillator synchonization connection diagram.

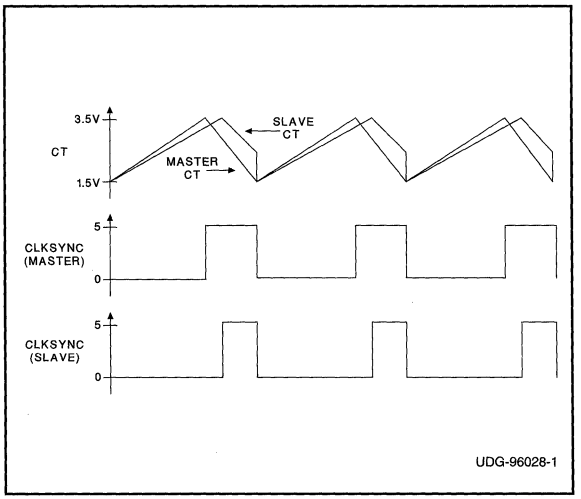


Figure 3. Oscillator waveforms.

APPLICATION INFORMATION (cont.)

The following explains two synchronization techniques:

1. If the user does not care which unit is the master, then the oscillator frequencies are designed as accurate as necessary and one unit will become the master and synchronize the remaining units. The user will never know exactly which unit will be themaster upon power up.
2. If the user does care which unit is the master, a unit should be identified as the master, and the frequency and maximum duty cycle clamp should be programmed accordingly. The ROFF resistor which programs the slave units oscillator discharge ramp should be between 50% and 100% of the ROFF resistor which programs the master. This guarantees that if a slave unit tries to synchronize the master, the master frequency will still be faster than the slave frequency and the master will synchronize all the remaining units.

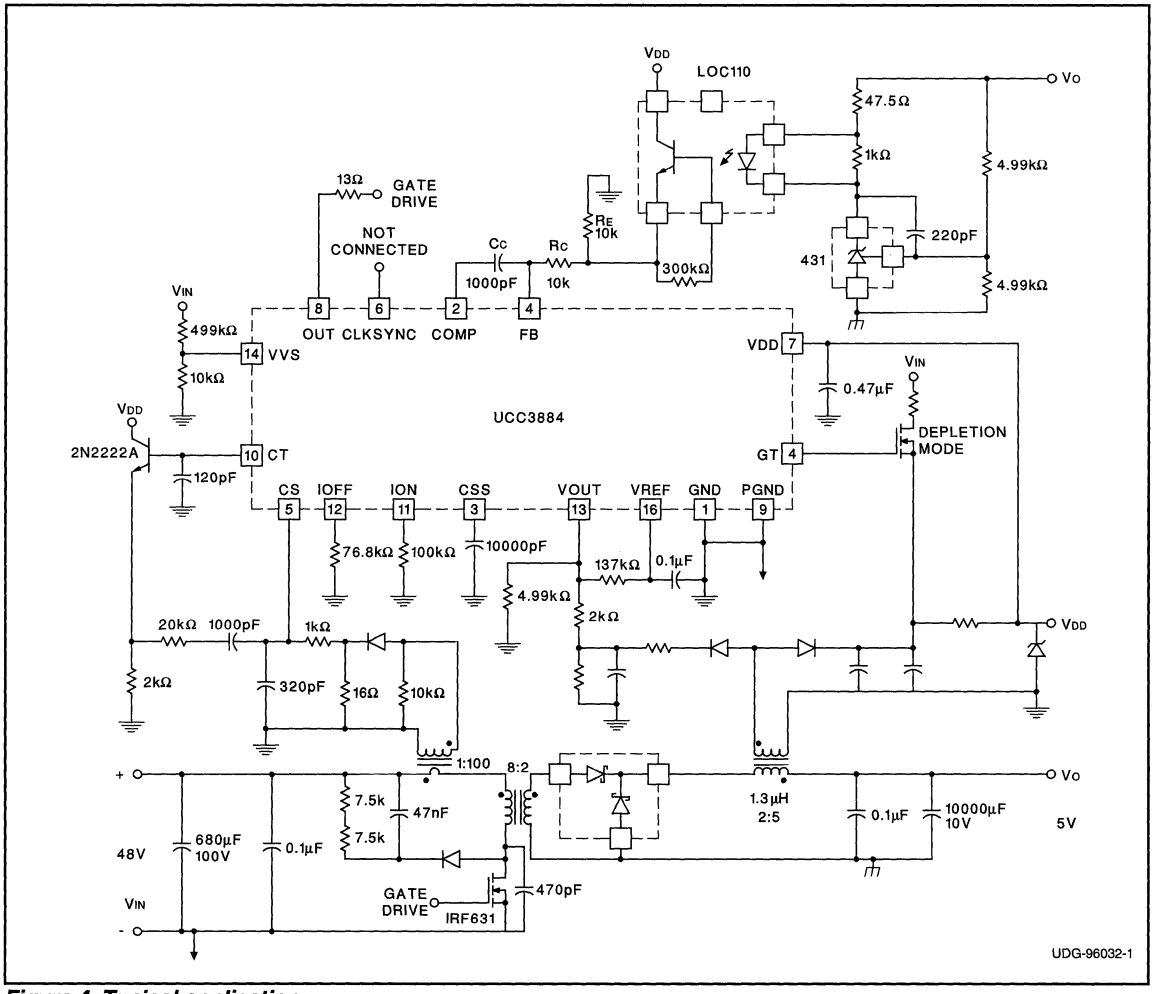


Figure 4. Typical application.

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UNITRODE

application INFO available

UC1886
UC2886
UC3886

Average Current Mode PWM Controller IC

FEATURES

- 10.3V - 20V Operating Range
- Low Offset Voltage Amplifier
- High Bandwidth Current and Voltage Amplifiers
- Low Offset Current Sense Amplifier
- Undervoltage Lockout
- Trimmed 5 Volt Reference
- Externally Programmable Oscillator Charge Current
- 1.5A Peak Totem Pole Output
- Available in 16-pin DIL or SOIC Packages

DESCRIPTION

The UC3886 family of PWM controller ICs is designed for DC-to-DC converters with average current mode control. It is designed for use in conjunction with the UC3910 4-bit DAC and Voltage Monitor. The UC3886 drives an external N-channel MOSFET and can be used to power the Intel Pentium® Pro and other high-end microprocessors.

The UC3886 in conjunction with the UC3910 converts 5VDC to an adjustable output ranging from 2.0V to 3.5V in 100mV steps with 35mV DC system accuracy.

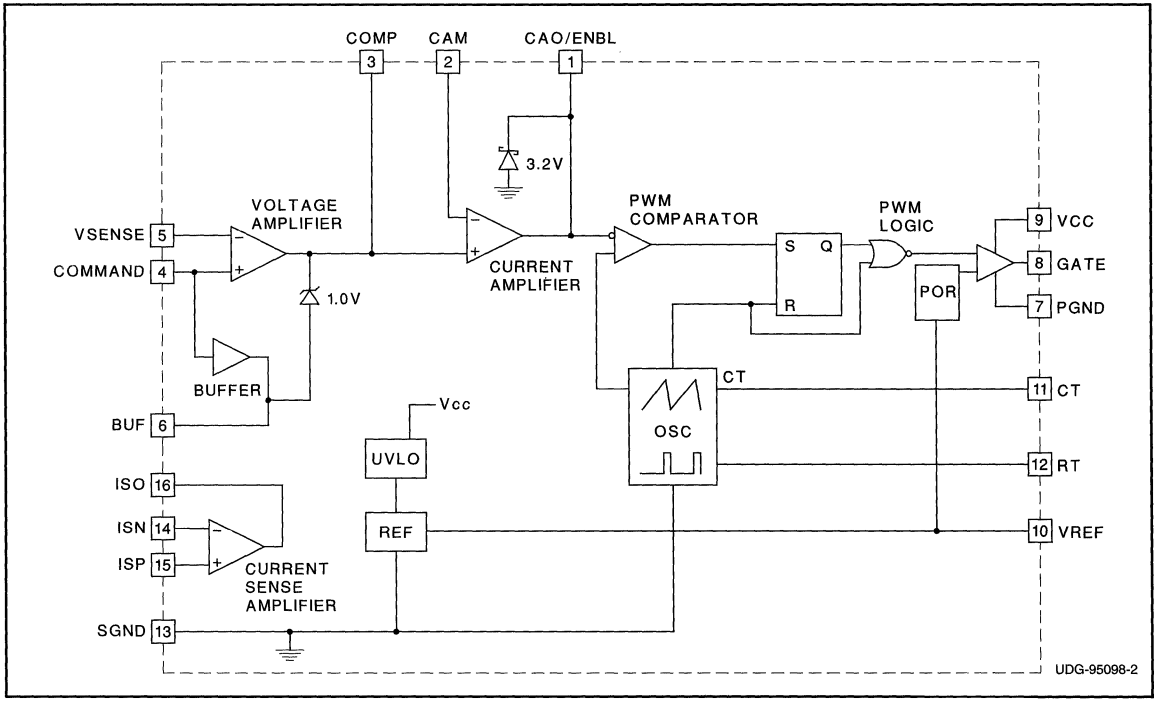
The oscillator is programmed by the user's selection of an external resistor and capacitor, and is designed for 300kHz typical operation.

The voltage and current amplifiers have 3.5MHz gain-bandwidth product to satisfy high performance system requirements.

The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. It has inputs and outputs accessible to allow user-selection of gain-setting resistors, and is internally compensated for a gain of 5 and above. The command voltage input is buffered and provided for use as the reference for the current sense amplifier.

The output of the voltage amplifier (input to the current amplifier) is clamped to 1 volt above the command voltage to serve as a current limit. The gate output can be disabled by bringing the CAO/ENBL pin to below 0.8 volts.

BLOCK DIAGRAM



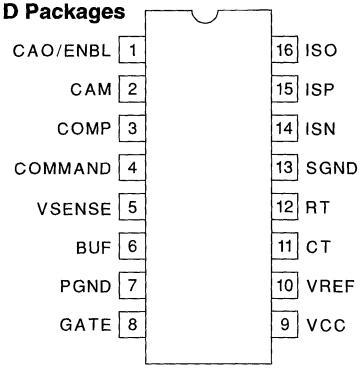
ABSOLUTE MAXIMUM RATINGS

Supply Voltage 20V
Output Current
CAM, COMMAND, VSENSE, ISN, ISP . . . . . ± 1A
Analog Input . . . . . –0.3V to 7V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperatue (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VCC = 12V, $V_{COMMAND}$ = 3.0V, CT = 1nF, RT = 10k, $T_A = T_J$ = 0°C < T_A < 70°C for the UC3886. (Note: –25°C < T_A < 85°C for the UC2886, and –55°C < T_A < 125°C for the UC1886)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current	VCC = 11V, Gate Open		10	15	mA
	VCC = 9.3V			5	mA
Undervoltage Lockout					
Start Threshold		9.7	10.3	10.8	V
UVLO Hysteresis			0.25	0.4	V
Voltage Error Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			4	mV
	V_{CM} = 3.0V (UC2886, UC1886)			15	mV
Input Bias Current	V_{CM} = 3.0V			–2	µA
Input Offset Current	V_{CM} = 3.0V (UC3886)			0.01	µA
	V_{CM} = 3.0V (UC2886, UC1886)			0.1	µA
Open Loop Gain	2.5V < V_{COMP} < 3.5V	60	85		dB
Common-Mode Rejection Ratio	2V < V_{COMP} < 4V	60	85		dB
Power Supply Rejection Ratio	11V < VCC < 15V	60	85		dB
Output High Voltage (Clamp)	I_{COMP} = –100µA (UC3886)	3.95	4	4.05	V
	I_{COMP} = –100µA (UC2886, UC1886)	3.9		4.1	V
Output Low Voltage (Clamp)	I_{COMP} = 100µA	1.9		2.7	V
Output Sink Current	V_{COMP} = 3.7V	0.9			mA
Output Source Current	V_{COMP} = 2.8V	–0.15	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
5.0V Reference					
Output Voltage	I_{VREF} = 1.0mA	4.9	5	5.1	V
Total Variation	Line, Load, Temperature	4.825		5.175	V
Line Regulation	11V < VCC < 15V			10	mV
Load Regulation	0 < I_{VREF} < 2mA			15	mV
Short Circuit Current		–10		–40	mA

ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 12V, $V_{COMMAND}$ = 3.0V, CT = 1nF, RT = 10k, $T_A = T_J = 0°C < T_A < 70°C$ for the UC3886. (Note: $-25°C < T_A < 85°C$ for the UC2886, and $-55°C < T_A < 125°C$ for the UC1886)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Buffer					
Gain	I_{BUF} = ± 500µA (UC3886)	0.98	1	1.02	V/V
	I_{BUF} = ± 500µA (UC2886, UC1886)	0.95		1.05	V/V
Current-Sense Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			2	mV
	V_{CM} = 3.0V (UC2886, UC1886)			6	mV
Input Bias Current	V_{CM} = 3.0V			-1	µA
Input Offset Current	V_{CM} = 3.0V			0.2	µA
Open Loop Gain	$2V < V_{ISO} < 6V$	60	85		dB
CMRR	$0V < V_{CM} < 4.5V$	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{ISO} = –100µA	5			V
Output Low Voltage	I_{ISO} = 1mA			1	V
Output Source Current	V_{ISO} = 2V	–0.2			mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Current Amplifier					
Input Offset Voltage	V_{CM} = 3.0V (UC3886)			13	mV
	V_{CM} = 3.0V (UC2886, UC1886)			18	mV
Input Bias Current	V_{CM} = 3.0V			1	µA
Open Loop Gain	$1V < V_{CAO} < 3V$	60	85		dB
CMRR	$1.5V < V_{CM} < 4.5V$	60	85		dB
PSRR	11V < VCC < 15V	60	85		dB
Output High Voltage	I_{CAO} = –100µA	3		3.3	V
Output Low Voltage	I_{CAO} = 100µA			1	V
Output Source Current	V_{CAO} =1V	–0.1	–0.25		mA
Gain-Bandwidth Product	F = 100kHz	2	3.5		MHz
Oscillator					
Frequency	RT = 10k, CT = 1nF (UC3886)	90	100	110	kHz
	RT = 10k, CT = 1nF (UC2886, UC1886)	85		115	kHz
Frequency Change With Voltage	11V > VCC > 15V			1	%
CT Peak Voltage		2.6	2.8		V
CT Valley Voltage			1	1.2	V
CT Peak-to-Peak Voltage		1.6	1.8	2.0	V
Output Section					
Output Low Voltage	I_{GATE} = 200mA		1.6	2.2	V
Output High Voltage	I_{GATE} = –200mA	9	10.3		V
Output Low Voltage	$5V < VCC < 9V$, I_{GATE} = 10mA			0.5	V
	$V_{CAO} < 0.8V$, I_{GATE} = 10mA			0.5	V
Rise/Fall Time	C_L = 1nF			150	ns
Maximum Duty Cycle	(UC3886)	90			%
	(UC2886, UC1886)	85			%

PIN DESCRIPTIONS

BUF: (Buffer Output) The voltage on COMMAND pin is buffered and presented to the user here. This voltage is used to provide the operating bias point for the current sense amplifier by connecting a resistor between BUF and ISP. Decouple BUF with 0.01µF or greater to SGND.

CAM: (Current Amplifier Minus Input) The average load current feedback from ISO is typically applied through a resistor here.

CAO/ENBL: (Current Amplifier Output/Chip Enable) The current loop compensation network is connected between CAO/ENBL and CAM, the inverting input of the current amplifier. The voltage at CAO/ENBL is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage at this pin exceeds 1.0 volts, allowing the PWM to force zero duty cycle when necessary. The user can force this pin below 0.8 volts externally with an open collector, disabling the GATE drive.

COMMAND: (Voltage Amplifier Non-Inverting Input) This input to the voltage amplifier is connected to a command voltage, such as the output of a DAC. This voltage sets the switching regulator output voltage.

COMP: (Compensation, Voltage Amplifier Output) The system voltage compensation network is applied between COMP and VSENSE. The voltage at COMP is clamped to prevent it from going more than 1V above the COMMAND voltage. This is used to provide an accurate average current limit. The voltage on COMP is also clamped to 0.7V below the voltage on COMMAND. This is done to avoid applying a full charge to capacitors in the compensation network during transients, allowing quick recovery time and little overshoot.

CT: (Oscillator Timing Capacitor) A capacitor from CT to SGND along with the resistor on RT, sets the PWM frequency and maximum duty cycle according to these formulas:

$$D_{MAX} = 1 - \frac{2.0V}{RT \bullet 4.0mA}$$

where D_{MAX} is the maximum operating duty cycle, and RT is in ohms.

$$F_{OSC} = \frac{2.0V \bullet ((4.0mA \bullet RT) - 2.0V)}{CT \bullet 1.8V \bullet RT^2 \bullet 4.0mA}$$

where F_{OSC} is the UC3886 oscillator switching frequency in Hz, RT is in ohms, and CT is in farads.

GATE: (PWM Output) The output is a 1A totem pole driver. Use a series resistor of at least 5Ω to prevent interaction between the gate impedance and the output driver that might cause excessive overshoot.

ISN: (Current Sense Amplifier Inverting Input) A resistor to the low side of the average current sense resistor and a resistor to ISO are applied to this pin to make a differential sensing amplifier.

ISO: (Current Sense Amplifier Output) A feedback resistor to ISN is connected here to make a differential sensing amplifier. The voltage at this pin is equal to (V_{BUF} + A • I_{AVG} • R_{SENSE}) where A is the user determined gain of the differential amplifier, I_{AVG} is the average load current of the system, and R_{SENSE} is the average current sensing resistor. For stability, A must be greater than 5. Set A such that A • I_{SC} • R_{SENSE} = 1.0V where ISC is the user-determined short circuit current limit.

ISP: (Current Sense Amplifier Non-Inverting Input) A resistor to the high side of the average current sense resistor and a resistor to BUF are connected to this pin to make a differential sensing amplifier.

PGND: (Power Ground) The PWM output current returns to ground through this pin. This is separated from SGND to avoid on-chip ground noise generated by the output current.

RT: (Oscillator Charging Current) This pin is held at 2V. Resistor RT from this pin to SGND sets the oscillator charging current. Use 5k < RT < 100k.

SGND: (Signal Ground) For better noise immunity, signal ground is provided at this pin.

VCC: (Positive Supply Voltage) This pin supplies power to the chip and to the gate drive output. Decouple to PGND and separately to SGND for best noise immunity. The reference (VREF), GATE output, oscillator, and amplifiers are disabled until VCC exceeds 10.3V.

VREF: (Voltage Reference Output) An accurate 5V reference as provided at this pin. The output can deliver 2mA to external circuitry, and is internally short circuit current limited. VREF is disabled if VCC is below UVLO. Bypass 5V REF to SGND with an 0.01µF or larger capacitor for best stability.

VSENSE: (Voltage Sense Input) This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

APPLICATION INFORMATION

OSCILLATOR

The UC3886 oscillator is a saw tooth. The rising edge is governed by a current controlled by RT flowing into the capacitor CT. The falling edge of the sawtooth sets the dead time for the output. Selection of RT should be done first, based on desired maximum duty cycle. CT can then be chosen based on the desired frequency, FS, and the value of RT. The design equations are:

$$D_{MAX} = 1 - \frac{2.0V}{RT \bullet 4.0\,mA}$$

$$F_{OSC} = \frac{2.0V \bullet ((4.0\,mA \bullet RT) - 2.0V)}{CT \bullet 1.8V \bullet RT^2 \bullet 4.0\,mA}$$

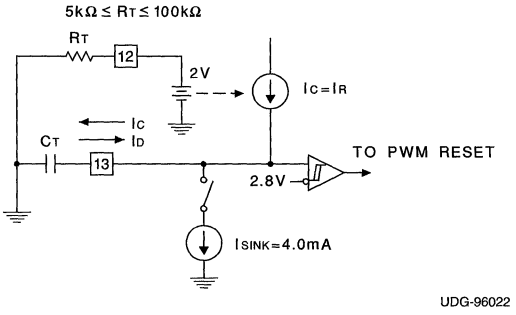


Figure 1. Oscillator

Configuring the Current Sense Amplifier

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, R_{SENSE}. This amplifier must be set up as a differential amplifier as shown.

The Current Sense Amplifier gain, G_{CSA}, is given by the ratio of R2/R1. The output of the Current Sense Amplifier at the ISO pin is given by

$$V_{ISO} = V_{BUF} + V_{SENSE} \bullet \frac{R2}{R1}$$

The Current Sense Amplifier gain, G_{CSA}, must be programmed to be greater than or equal to 5.0 (14dB), as this amplifier is not stable with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore G_{CSA} must be programmed between

$G_{CSA\_MIN} = 5.0$ and $G_{CSA\_MAX} = 2.5MHz/F_{SWITCH}$

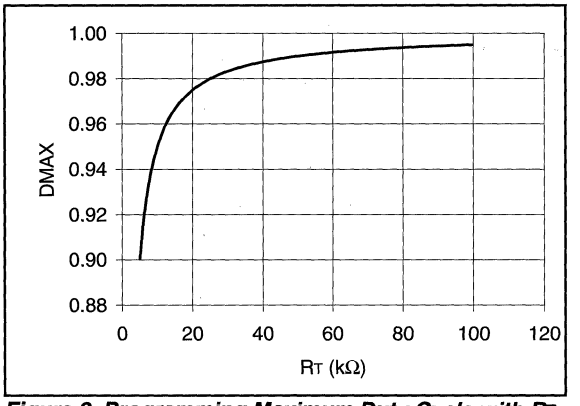


Figure 2. Programming Maximum Duty Cycle with RT

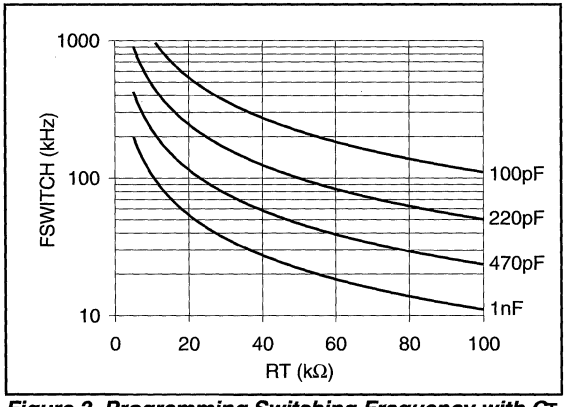


Figure 3. Programming Switching Frequency with CT

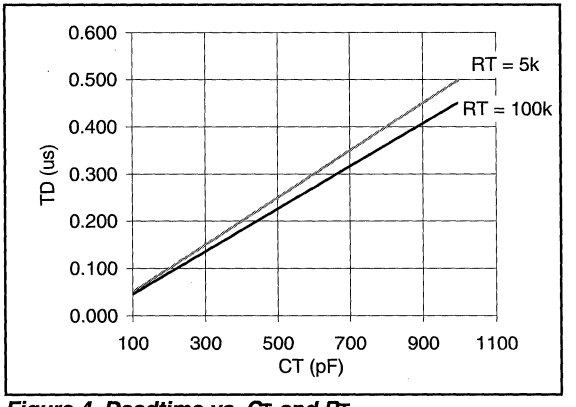


Figure 4. Deadtime vs. CT and RT

APPLICATION INFORMATION (cont.)

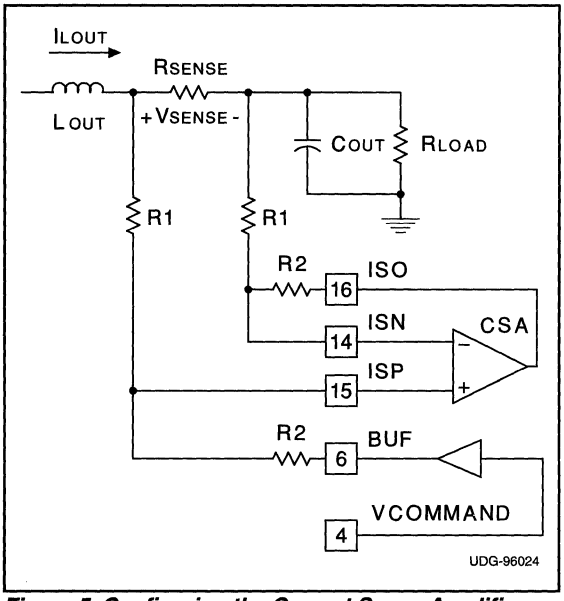


Figure 5. Configuring the Current Sense Amplifier

Enabling/Disabling the UC3886 Gate Drive

The CAO/ENBL pin can be used to Disable the UC3886 gate drive by forcing this pin below 0.8V, as shown. Bringing the voltage below the valley of the PWM oscillator ramp will insure a 0% duty cycle, effectively disabling the gate drive. A low noise open collector signal should be used as an Enable/Disable command.

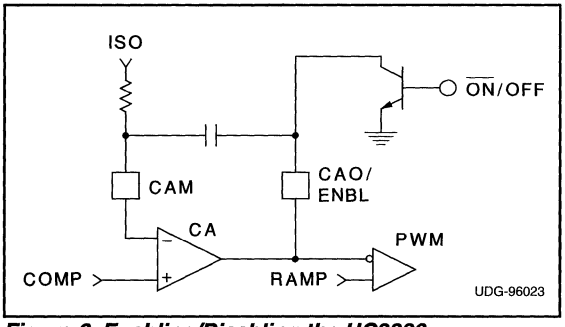


Figure 6. Enabling/Disabling the UC3886

TYPICAL APPLICATIONS

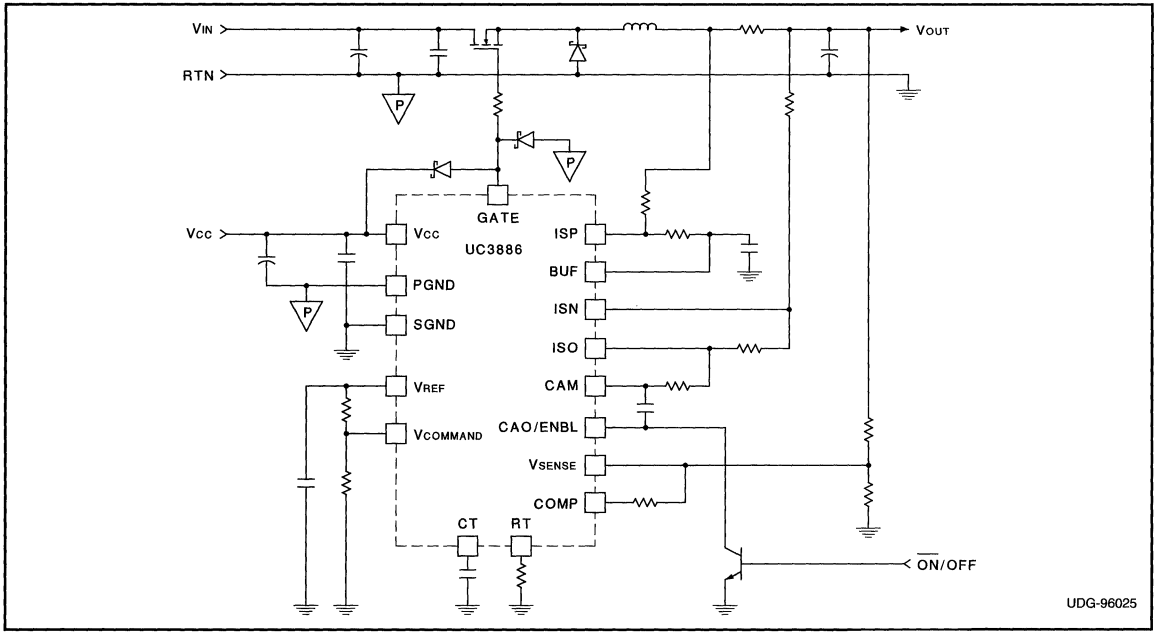


Figure 7. The UC3886 Configured in a Buck Regulator

TYPICAL APPLICATIONS (cont.)

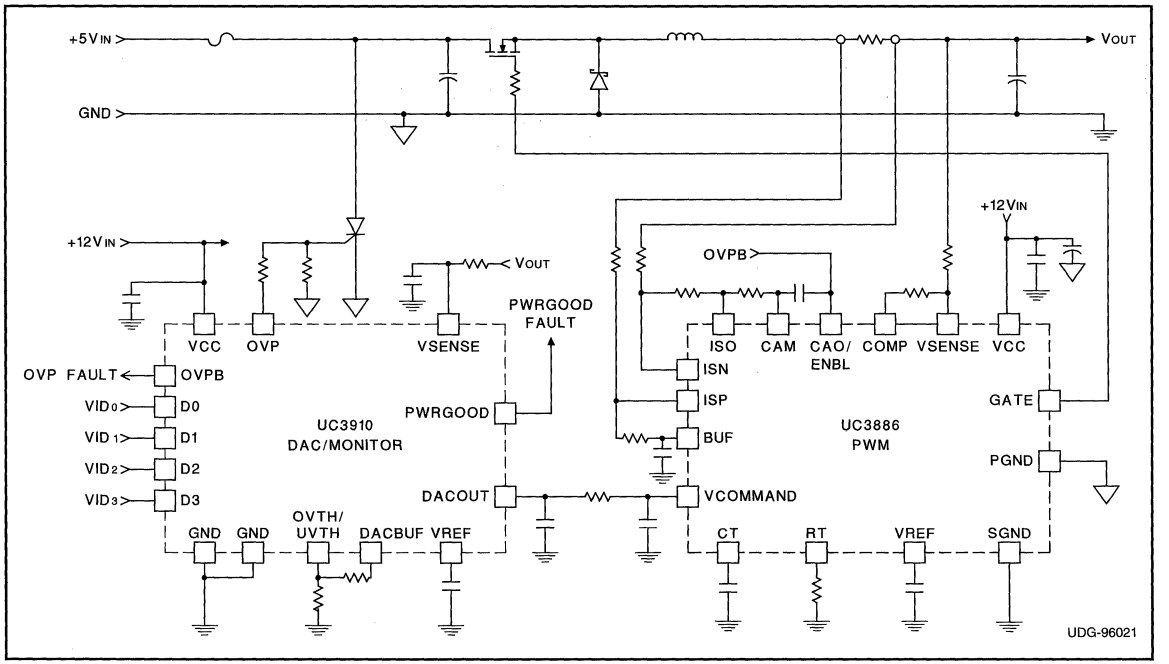


Figure 8. UC3886 Configured with the UC3910 for a Pentium® Pro DC/DC Converter

UNITRODE CORPORATION
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UNITRODE

application INFO available

UCC1888
UCC2888
UCC3888

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Power Supply
- Wide 100VDC to 400VDC Allowable Input Range
- Fixed 5VDC or Adjustable Low Voltage Output
- Output Sinks 200mA, Sources 150mA Into a MOSFET Gate
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC3888 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios as high as 400V to 2.7V with no transformer and low internal losses.

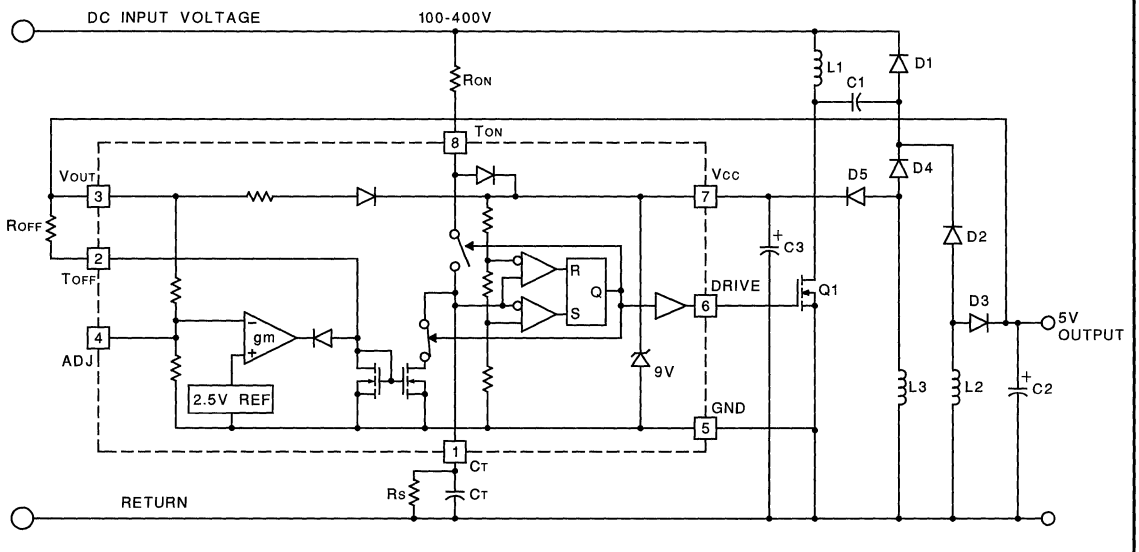
The control algorithm utilized by the UCC3888 sets the switch on time inversely proportional to the input line voltage and sets the switch off time inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 2.7V to be achieved with a switch duty cycle of 7.6%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage is set internally to 5V. It can be programmed for other output voltages with two external resistors. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the current through RON into TON is directed to VCC where it charges the external capacitor, C3, connected to VCC. As voltage builds on VCC, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until VCC reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into TON to the timing capacitor, CT. CT charges to a fixed threshold with a current ICHG=0.8 • (VIN - 4.5V)/RON. Since DRIVE will only be high for as long as CT charges, the power switch on time will be inversely proportional to line voltage. This provides a constant (line voltage) • (switch on time) product.

TYPICAL APPLICATION



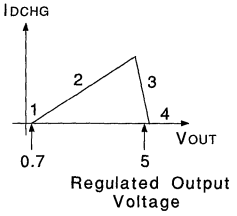
Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-96013

OPERATION (cont.)

At the end of the on time, Q1 is turned off and the current through RON is again diverted to VCC. Thus the current through RON, which charges CT during the on time, contributes to supplying power to the chip during the off time.

The power switch off time is controlled by the discharge of CT which, in turn, is programmed by the regulated output voltage. The relationship between CT discharge current, IDCHG, and output voltage is illustrated as follows:



Region 1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.

Region 2. As VOUT rises above approximately 0.7V to its regulated value, IDCHG is defined by ROFF, and is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As VOUT increases, IDCHG increases reducing off time. The operating frequency increases and VOUT rises quickly to its regulated value.

Region 3. In this region, a transconductance amplifier reduces IDCHG in order to maintain a regulated VOUT.

Region 4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\ (\text{max}) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

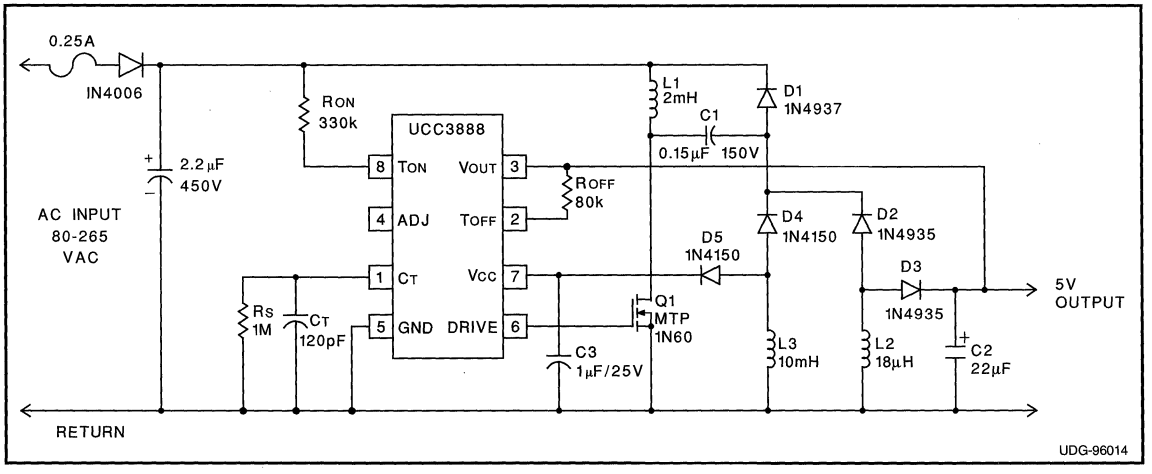
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V\ /(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of RS which have a minimal impact on TOFF.

The above equations assume that VCC equals 9V. The voltage at TON increases from approximately 2.5V to 6.5V while CT is charging. To take this into account, VIN is adjusted by 4.5V in the calculation of TON. The voltage at TOFF is approximately 0.7V.

DESIGN EXAMPLE

The UCC3888 regulates a 5 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.2 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.

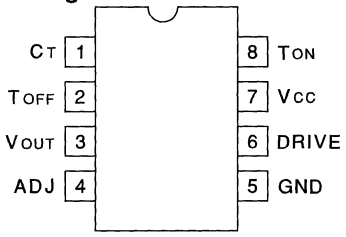


ABSOLUTE MAXIMUM RATINGS

ICC 8mA
Current into TON Pin 1.5mA
Voltage on VOUT Pin 20V
Current into TOFF Pin 250µA
Storage Temperature ..... -65°C to +150°C
Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for TA = 0°C to 70°C for the UCC3888, -40°C to +85°C for the UCC2888, and -55°C to +125°C for the UCC1888. No load at DRIVE pin (CLOAD=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC Zener Voltage	ICC < 1.5mA	8.6	9.0	9.3	V
Startup Current	VOUT = 0		150	250	µA
Operating Current I(VCC)	VCC = VCC(zener) – 100mV, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	VOUT = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	VOUT = 0	6.0	6.3	6.6	V
Hysteresis	VOUT = 0	1.8			V
Oscillator					
Amplitude	VCC = 9V	3.5	3.7	3.9	V
CT to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
CT to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, VCC = 9V		0.15	0.4	V
	I = 100mA, VCC = 9V		0.7	1.8	V
VOH	I = –20mA, VCC = 9V	8.5	8.8		V
	I = –100mA, VCC = 9V	6.1	7.8		V
Rise Time	CLOAD = 1nF		35	70	ns
Fall Time	CLOAD = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: ICHG / I(TON)	VCT = 3V, DRIVE = High, I(TON) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	RON = 330k	60	80	100	V
Minimum Current I(TON) for Fault	RON = 330k		220		µA
On Time During Fault	CT = 150pF, VLINE = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
VOUT Error Amp					
VOUT Regulated 5V (ADJ Open)	VCC = 9V, IDCHG = I(TOFF)/2	4.5	5.0	5.5	V
Discharge Ratio: IDCHG / I(TOFF)	I(TOFF) = 50µA	0.95	1.01	1.07	
Voltage at TOFF	I(TOFF) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max IDCHG = 50µA		2.4		mA/V
	Max IDCHG = 125µA	1.9	4.1	7.0	mA/V

Note 1: gm is defined as $\frac{\Delta IDCHG}{\Delta VOUT}$ *for the values of VOUT when VOUT is in regulation. The two points used to calculate gm are for IDCHG at 65% and 35% of its maximum value.*

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 5V regulated supply without additional external components. Other output voltages can be obtained by connecting a resistor divider between VOUT, ADJ and GND. Use the formula

$$V_{OUT} = 2.5V \bullet \frac{R1 + R2}{R2}$$

where R1 is connected between VOUT and ADJ, and R2 is connected between ADJ and GND. R1 || R2 should be less than 1kΩ to minimize the effect of the temperature coefficient of the internal 30k resistors which also connect to VOUT, ADJ, and GND. See Block Diagram.

CT (timing capacitor): The signal voltage at CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage at CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

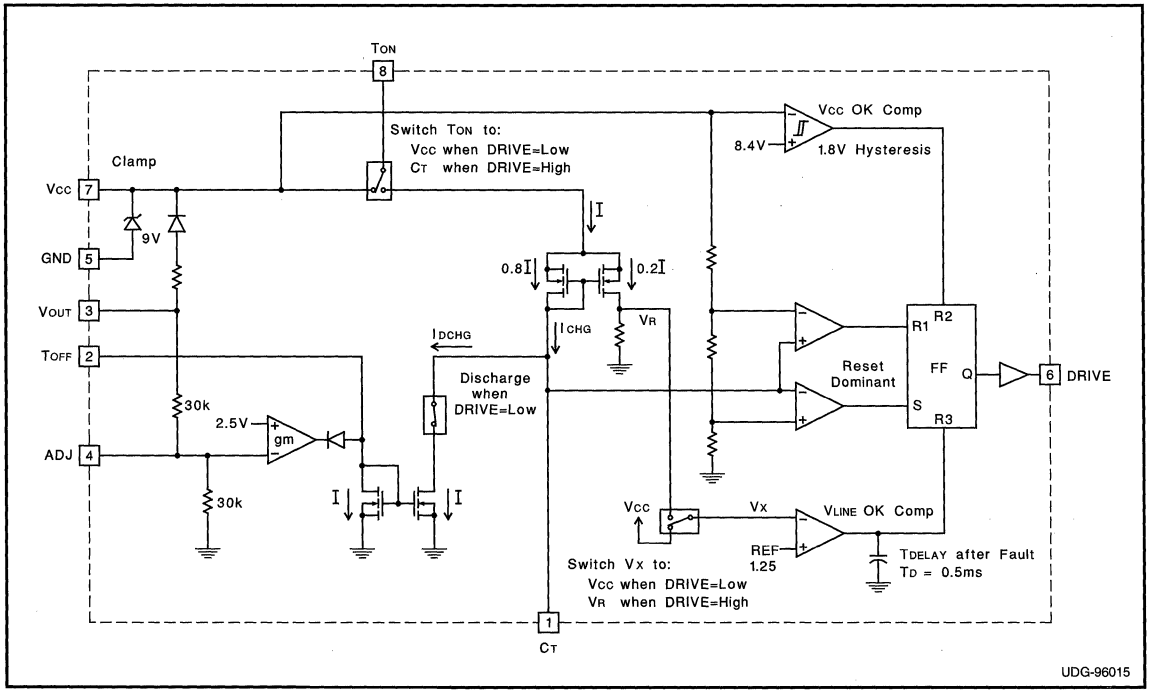
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from 2.5V to 6.5V.

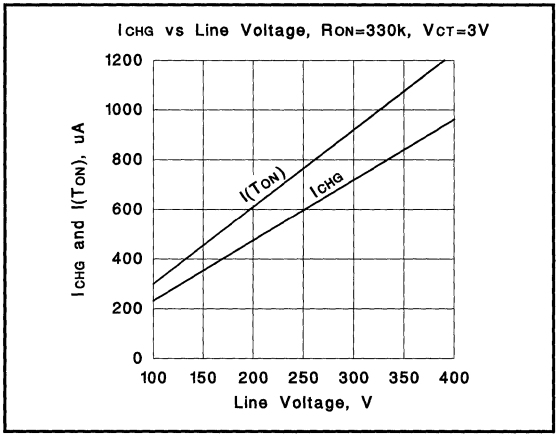
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. The device needs an external supply, from a source such as the rectified AC line or derived from the switching circuit. Precautions must be taken to ensure that total ICC does not exceed 8mA.

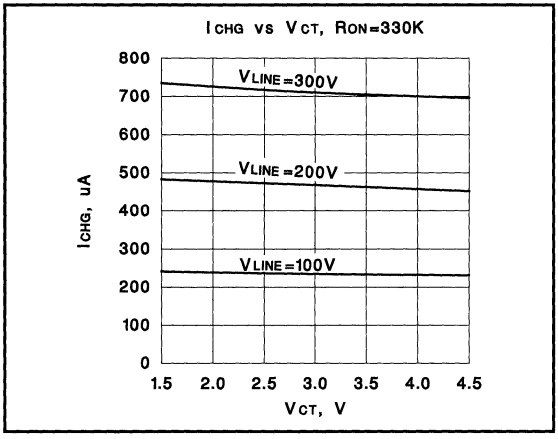
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS CURVES





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application INFO available

UCC1889
UCC2889
UCC3889

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Applications
- Ideal Primary-side Bias Supply
- Efficient BiCMOS Design
- Wide Input Range
- Fixed or Adjustable Low Voltage Output
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC1889 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios of 400V to 12V with no transformer and low internal losses.

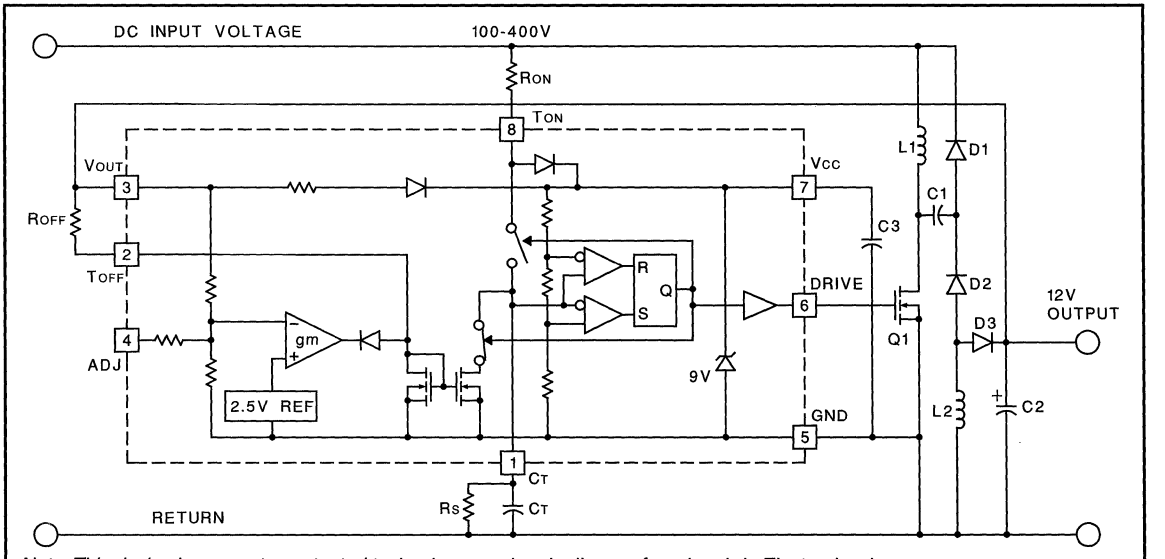
The control algorithm utilized by the UCC1889 is to force the switch on time to be inversely proportional to the input line voltage while the switch off time is made inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 12V to be achieved with a switch duty cycle greater than 10%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage can be easily set to 12V or 18V. Moreover, it can be programmed for other output voltages less than 18V with a few additional components. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the RON current into TON is directed to VCC where it charges the external capacitor, C3, connected to VCC. As voltage builds on VCC, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until VCC reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into TON to the timing capacitor, CT. CT charges to a fixed threshold with a current $I_{CHG}=0.8 \bullet (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as CT charges, the power switch on time will be inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

TYPICAL APPLICATION



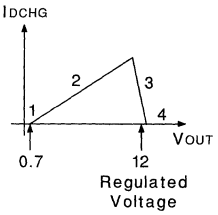
Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-93060-1

OPERATION (cont.)

At the end of the on time, Q1 is turned off and the RON current into TON is again diverted to VCC. Thus the current through RON, which charges CT during the on time, contributes to supplying control power during the off time.

The power switch off time is controlled by the discharge of CT which, in turn, is programmed by the regulated output voltage. The relationship between CT discharge current, IDCHG, and output voltage is illustrated as follows:



1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.
2. As VOUT rises above approximately 0.7V to its regulated value, IDCHG is defined by ROFF, and therefore is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As VOUT increases, IDCHG increases resulting in the reduction of off time. The frequency of operation increases and VOUT rises quickly to its regulated value.

3. In this region, a transconductance amplifier reduces IDCHG in order to maintain VOUT in regulation.
4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\ (\text{max}) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

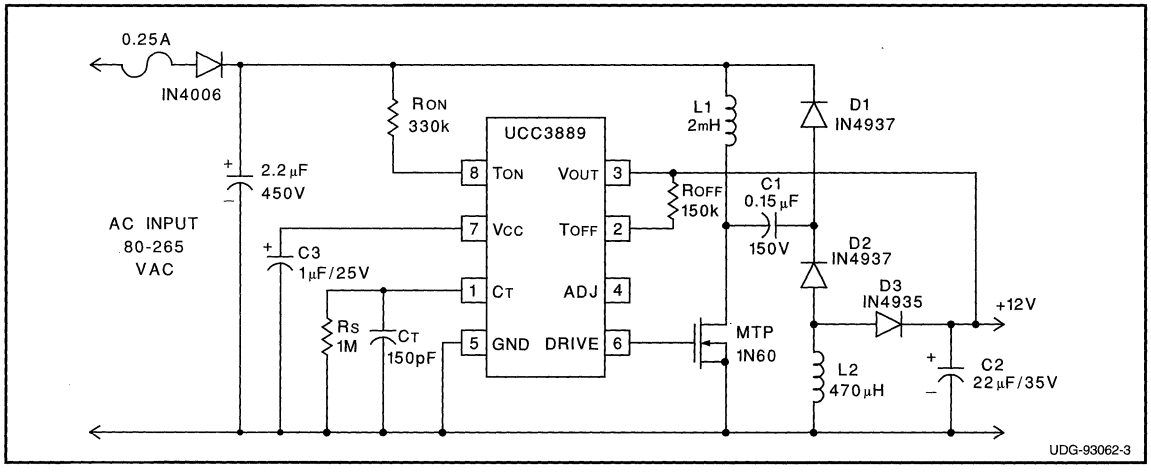
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V/(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of RS which have a minimal impact on TOFF.

The above equations assume that VCC equals 9V. The voltage at TON increases from approximately 2.5V to 6.5V while CT is charging. To take this into account, VIN is adjusted by 4.5V in the calculation of TON. The voltage at TOFF is approximately 0.7V.

DESIGN EXAMPLE

The UCC3889 regulates a 12 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.4 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.

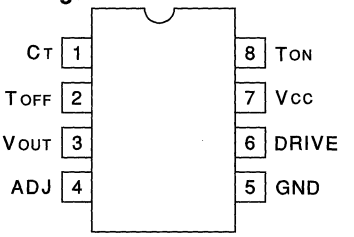


ABSOLUTE MAXIMUM RATINGS

ICC 5mA
Current into TON Pin 1.5mA
Voltage on VOUT Pin 20V
Current into TOFF Pin 250µA
Storage Temperature ..... -65°C to +150°C
Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for TA = 0°C to 70°C for the UCC3889, -40°C to +85°C for the UCC2889, and -55°C to +125°C for the UCC1889. No load at DRIVE pin (CLOAD=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC Zener Voltage	ICC < 1.5mA	8.6	9.0	9.3	V
Startup Current	VOUT = 0		150	250	µA
Operating Current I(VOUT)	VOUT = 11V, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	VOUT = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	VOUT = 0	6.0	6.3	6.6	V
Hysteresis	VOUT = 0	1.8			V
Oscillator					
Amplitude	VCC = 9V	3.5	3.7	3.9	V
CT to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
CT to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, VCC = 9V		0.15	0.4	V
	I = 100mA, VCC = 9V		0.7	1.8	V
VOH	I = –20mA, VCC = 9V	8.5	8.8		V
	I = –100mA, VCC = 9V	6.1	7.8		V
Rise Time	CLOAD = 1nF		35	70	ns
Fall Time	CLOAD = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: ICHG / I(TON)	VCT = 3V, DRIVE = High, I(TON) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	RON = 330k	60	80	100	V
Minimum Current I(TON) for Fault	RON = 330k		220		µA
On Time During Fault	CT = 150pF, VLINE = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
VOUT Error Amp					
VOUT Regulated 12V (ADJ Open)	VCC = 9V, IDCHG = I(TOFF)/2	11.2	11.9	12.8	V
VOUT Regulated 18V (ADJ = 0V)	VCC = 9V, IDCHG = I(TOFF)/2	16.5	17.5	19.5	V
Discharge Ratio: IDCHG / I(TOFF)	I(TOFF) = 50µA	0.95	1.01	1.07	
Voltage at TOFF	I(TOFF) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max IDCHG = 50µA		1.0		mA/V
	Max IDCHG = 125µA	0.8	1.7	2.9	mA/V

Note 1: gm is defined as $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ *for the values of VOUT when VOUT is in regulation. The two points used to calculate gm are for IDCHG at 65% and 35% of its maximum value.*

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 12V or an 18V regulated supply without additional external components. To select the 12V option, ADJ pin is left open. To select the 18V option, ADJ pin must be grounded. For other output voltages less than 18V, a resistor divider between VOUT, ADJ and GND is needed. Note, however, that for output voltages less than VCC, the device needs additional bootstrapping to VCC from an external source such as the line voltage. If so, precautions must be taken to ensure that total ICC does not exceed 5mA.

CT (timing capacitor): The signal voltage across CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage on CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

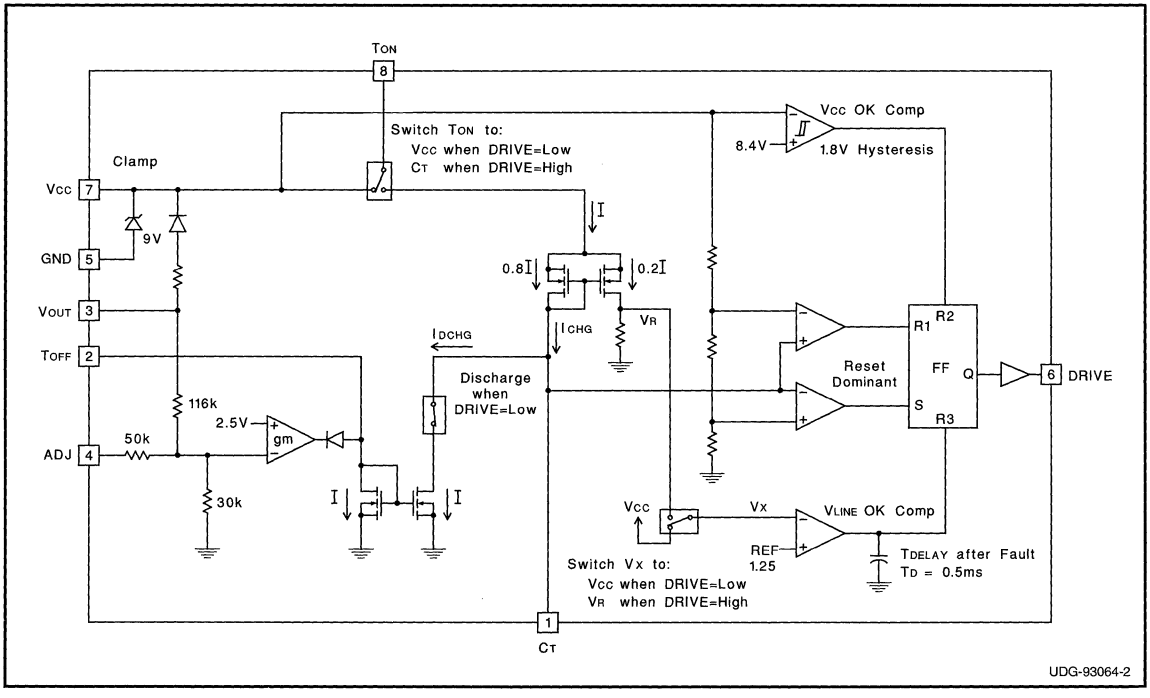
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from approximately 2.5V to 6.5V.

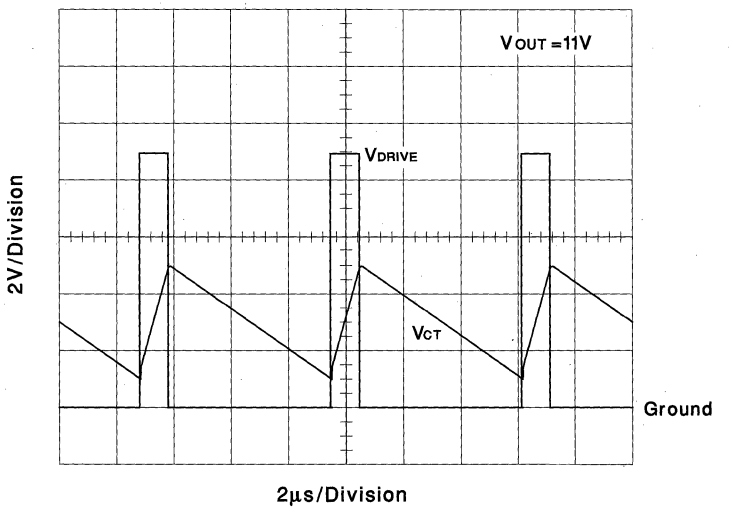
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. Normally, VCC is not directly powered from an external voltage source such as the line voltage. In the event that VCC is directly connected to a voltage source for additional bootstrapping, precautions must be taken to ensure that total ICC does not exceed 5mA.

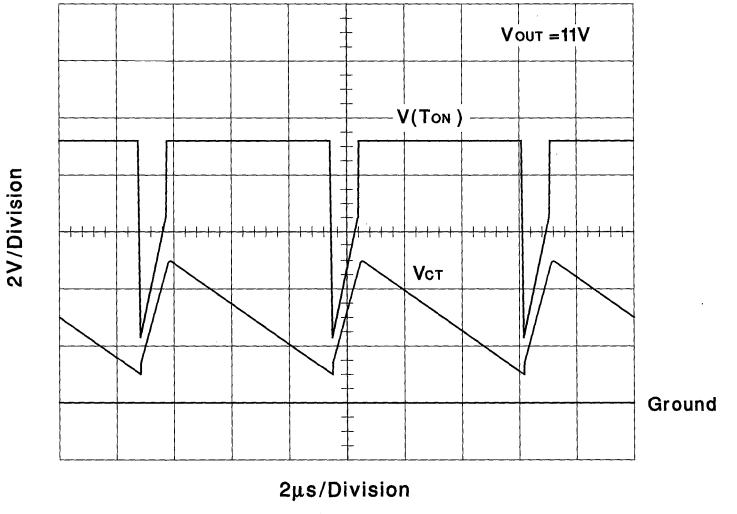
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

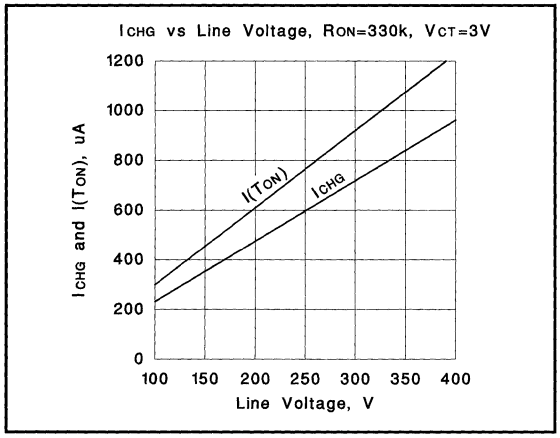
BLOCK DIAGRAM

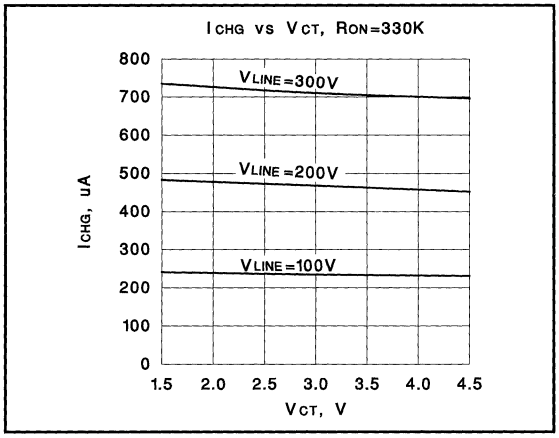


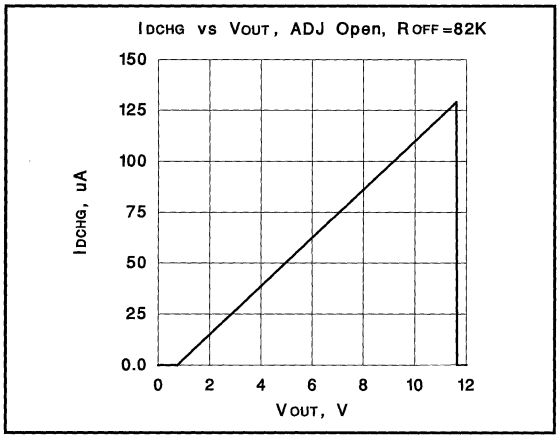
TYPICAL WAVEFORMS

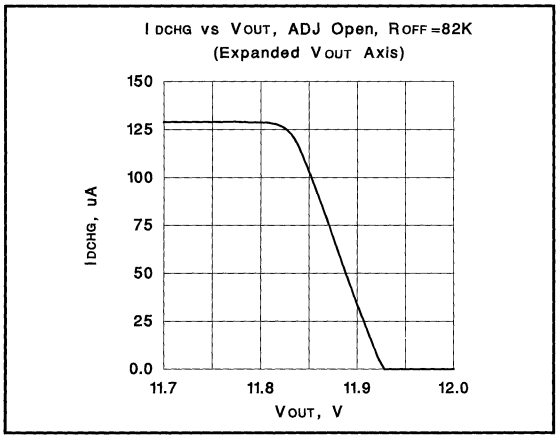


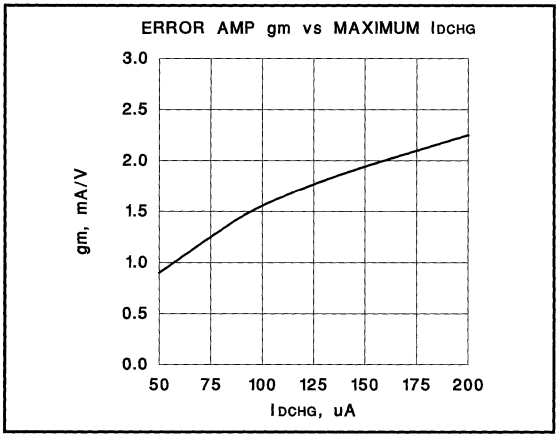


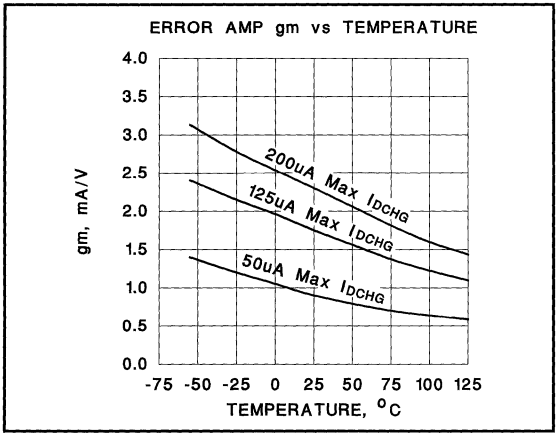












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application INFO available

UCC1890
UCC2890
UCC3890

Off-Line Battery Charger Circuit

FEATURES

- Transformerless Off-Line Operation
- Low Voltage Operation to 0.8V
- Ideal for Battery Trickle Charger Applications
- Current Mode Operation With 100mV Shunt
- Voltage Mode Operation With Fixed 1.25V Output or Resistor Adjustable Output
- Efficient BiCMOS Design
- Inherent Short Circuit Protection

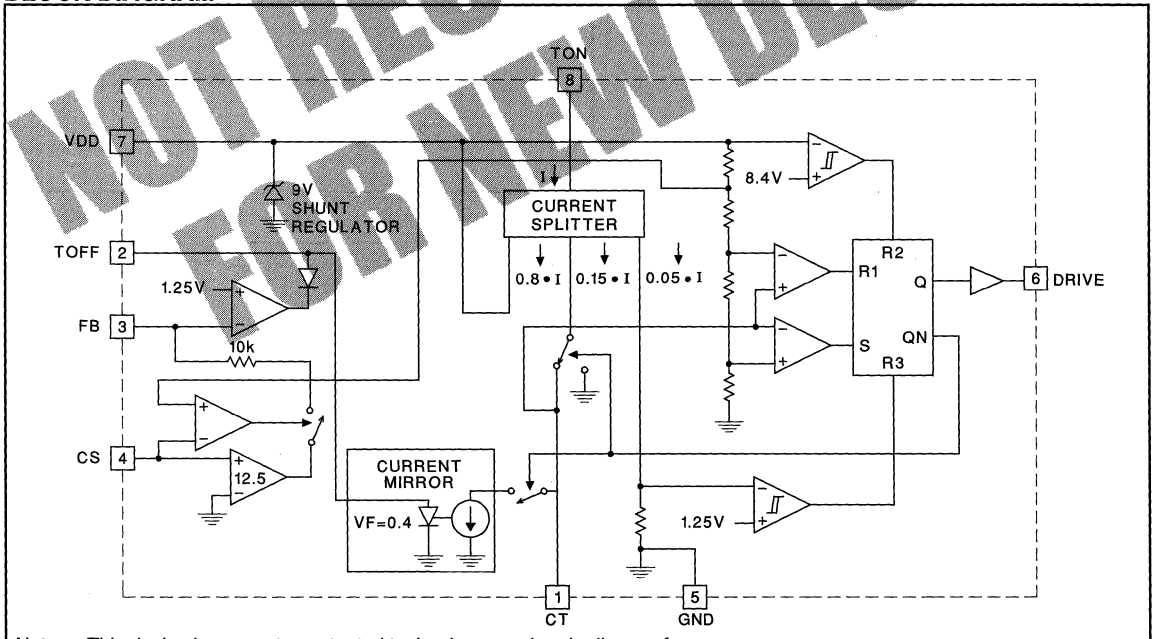
DESCRIPTION

The UCC3890 controller is optimized for use as an off-line, low power, low voltage, regulated current supply, ideally suited for battery trickle charger applications. The unique circuit topology used in this device can be visualized as two cascaded flyback converters; each operating in the discontinuous mode, and both driven from a single external power switch. The significant benefit of this approach is the ability to charge low voltage batteries in off-line applications with no transformer, and low internal losses.

The control algorithm used by the UCC3890 forces a switch on time inversely proportional to the input line voltage, while the switch off time is inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a large voltage conversion ratio with reasonable switch duty cycle.

While the UCC3890 is ideally suited for control of constant current battery chargers, provision is also made to operate as a fixed 1.25V regulated supply, or to use a resistor voltage divider to obtain output voltages higher than 1.25V.

BLOCK DIAGRAM



Note: This device incorporates patented technology used under license from Lambda Electronics, Inc.

UDG-96052

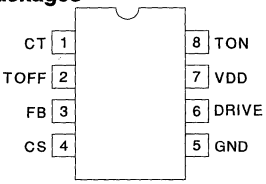
ABSOLUTE MAXIMUM RATINGS

IDD 7.5mA
Current into TON 7.5mA
Voltage on VOUT 20V
Current into TOFF 250µA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for TA = –55°C to 125°C for UCC1890, –40°C to 85°C for the UCC2890, and 0°C to 70°C for the UCC3890. No load at DRIVE pin (CLOAD = 0), TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VDD Zener Voltage	IDD = 4.75mA, ITON = 0mA	8.3	9.0	9.4	V
Minimum Operating Current ITON	IDD = –1mA, F = 150kHz		1.65	2.0	mA
Undervoltage Lockout					
Minimum Voltage to Start	FB = 0	7.8	8.6	9.2	V
Minimum Voltage after Start	FB = 0	5.75	6.3	6.65	V
Hysteresis	FB = 0	1.8	2.3	2.6	V
VDD – VSTART	FB = 0	0.2	0.4	0.7	V
Oscillator					
Amplitude	ITON = 3mA; ITOFF = 50µA; VFB = 0V CT = 100pF	3.1	3.4	3.7	V
CT to DRIVE High Delay	Overdrive = 200mV		80	200	ns
CT to DRIVE Low Delay	Overdrive = 200mV		50	100	ns
Charge Coefficient ICT/ITON	ITON = 3mA; VCT = 3.0V	0.135	0.15	0.165	µA/µA
Discharge Coefficent ICT/ITOFF	ITOFF = 50µA; VCT = 3.0V	0.95	1.00	1.05	µA/µA
Driver					
VOL	I = 100mA (Note 1)		0.7	1.8	V
VOH	I = –100mA referred to VDD (Note 1)	–2.9	–1.5		V
Rise Time	CL = 1nF		35	70	ns
Fall Time	CL = 1nF		30	60	ns
Line Voltage Detection					
Minimum ITON for Fault		1.0	1.5	2.0	mA
ITON Detector Hysteresis			110		µA
On Time During Fault			0.5		µs
VOUT Error Amplifier					
Reference Level	ITOFF = 50µA, ICT = 25µA, TJ = 25°C	1.20	1.25	1.30	V
	ITOFF = 50µA, ICT = 25µA, Over Temperature	1.15	1.25	1.35	V
Voltage at TOFF	ITOFF = 50µA	0.3	0.4	0.5	V
Regulation gm	ITOFF = 50µA (Note 2)	2.0	4.0	7.7	mA/V
Current Sense Amplifier					
Gain	VCS = 90 – 110mV	11.8	12.5	13.0	V/V
Input Offset Voltage	VCS = 90 – 110mV	–5	0	5	mV
Input Voltage for CS Amplifier Enabled	ITON = 3mA, Referred to VDD	–1.5	–0.8		V
Input Voltage for CS Amplifier Disabled	ITON = 3mA, Referred to VDD		–0.8	–0.3	V

Note 1: VDD forced to 100mV below VDD Zener Voltage

Note 2: gm is defined as $\frac{\Delta ICT}{\Delta VFB}$ *for the values of VFB where the error amp is in regulation. The two points used to calculate gm are for ICT at 65% amd 35% of its maximum value.*

PIN DESCRIPTIONS

CS: The high side of the current sense shunt is connected to this pin. Short CS to VDD for voltage feedback operation.

CT: Oscillator timing capacitor is connected to this pin.

DRIVE: Gate drive to external power switch.

FB: Output of current sense amplifier. This pin can be used for direct output voltage feedback if the current sense amp input pin CS is shorted to the VDD pin.

GND: Ground pin.

TOFF: Resistor ROFF connects from voltage output to this pin to provide a maximum capacitor discharge current proportional to output voltage.

TON: Resistor RON connects from line input to this pin to provide capacitor charge current proportional to line voltage. The current in RON also provides power for the 9V shunt regulator at VDD.

VDD: Output of 9V shunt regulator.

APPLICATION INFORMATION

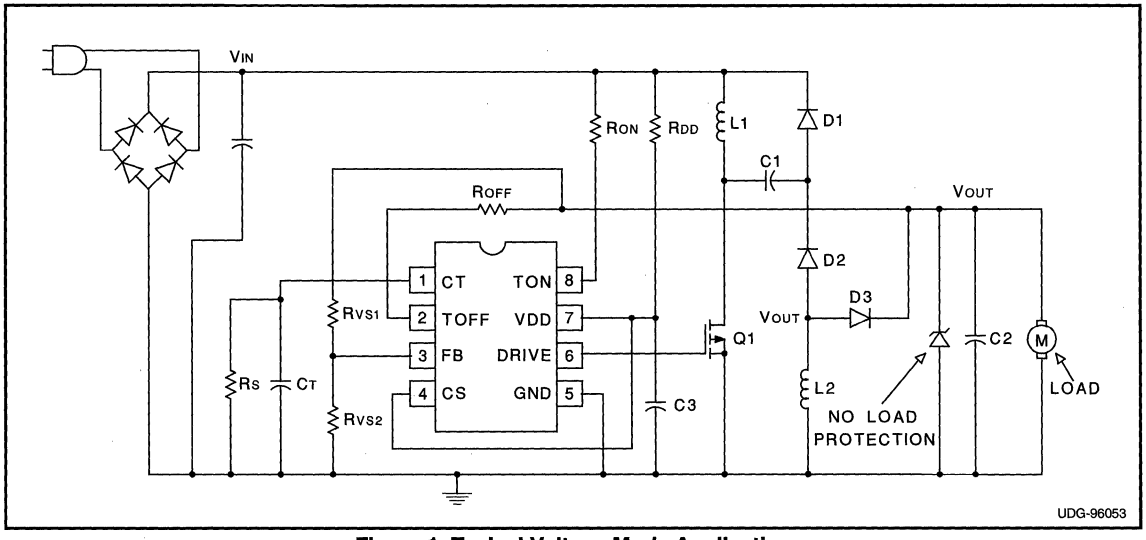


Figure 1. Typical Voltage Mode Application

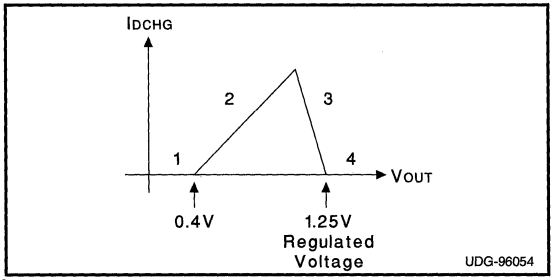
OPERATION (VOLTAGE OUTPUT)

Figure 1 shows a typical voltage mode application. When input voltage is first applied, all of the current through RDD and 80% of the current through RON, charge the external capacitor C3 connected to VDD. As the voltage builds on VDD, undervoltage lockout holds the circuit off and the output DRIVE low until VDD reaches 8.4V. At this time, DRIVE goes high, turning on the external power switch Q1, and 15% of the current into TON is directed to the timing capacitor CT. The voltage at TON is fixed at approximately 11V, so CT charges to a fixed threshold with current

$$I = 0.2 \bullet \frac{V_{IN} - 11V}{R_{ON}}$$

Since the input line is much greater than 11V, the charge current is approximately proportional to the input line voltage. DRIVE is only high while CT is charging, so the power switch on time is inversely proportional to line voltage. This provides a constant line voltage-switch on time product.

At the end of the switch on time, Q1 is turned off, and the 15% of the RON current which was charging CT is diverted to ground. The power switch off time is controlled by discharge of CT, which is determined by the outut voltage as described here:



APPLICATION INFORMATION (cont.)

1. When VOUT = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, RS, is placed in parallel with CT to establish a minimum switching frequency.

2. As VOUT rises above approximately 0.4V, IDCHG is set by ROFF, and is defined by

$$I_{DCHG} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

As VOUT increases, IDCHG increases resulting in the reduction of off time. The frequency of operation increases and VOUT rises quickly to its regulated value.

3. In this region, a transconductance amplifier reduces IDCHG in order to maintain VOUT in regulation. The input to the transconductance amplifier is the pin FB. (In this mode the pin CS should be shorted to VDD.) FB can either be connected directly to VOUT to regulate at nominal VOUT = 1.25V or to be connected to VOUT through a resistor divider RVS1/RVS2 to regulate at nominal

$$V_{OUT} = \frac{1.25V \bullet (R_{VS1} + R_{VS2})}{R_{VS2}}$$

4. If VOUT should rise above its regulation range, IDCHG falls to zero and the circuit returns to the minimum frequency established by RS and CT.

The range of switching frequencies is established by RON, ROFF, RS, and CT as follows:

$$\text{Frequency} = \frac{1}{TON + TOFF}$$

$$TON = \frac{C_T \bullet 3.4V \bullet 0.15 \bullet R_{ON}}{V_{IN} - 11V}$$

$$TOFF_{(MAX)} = 1.5 \bullet R_S \bullet C_T \text{ (regions1 and 4)}$$

$$TOFF = \frac{C_T \bullet 3.4V \bullet R_{OFF}}{V_{OUT} - 0.4V} \text{ (region 2)}$$

The above equations assume VDD = 9, the voltage at TON = 11V, the voltage at TOFF = 0.4V.

OPERATION (CURRENT OUTPUT)

Figure 2 shows a typical current mode application. In current mode, operation is the same as in voltage mode, except that in region 3 the transconductance amplifier is controlled by the current sense amplifier which senses the voltage across a shunt resistor RSH. The circuit then regulates the current in the shunt to the nominal value

$$I_{SH} = \frac{100mV}{R_{SH}}$$

The circuit shown in this schematic would be suitable for an application which trickle charges a battery at a low current, (e.g. C/10), and has a battery load which draws a high current, (e.g. C), when turned on. In that case, RSH1 value is chosen so that

$$\frac{100mV}{R_{SH1}} = \frac{C}{10}$$

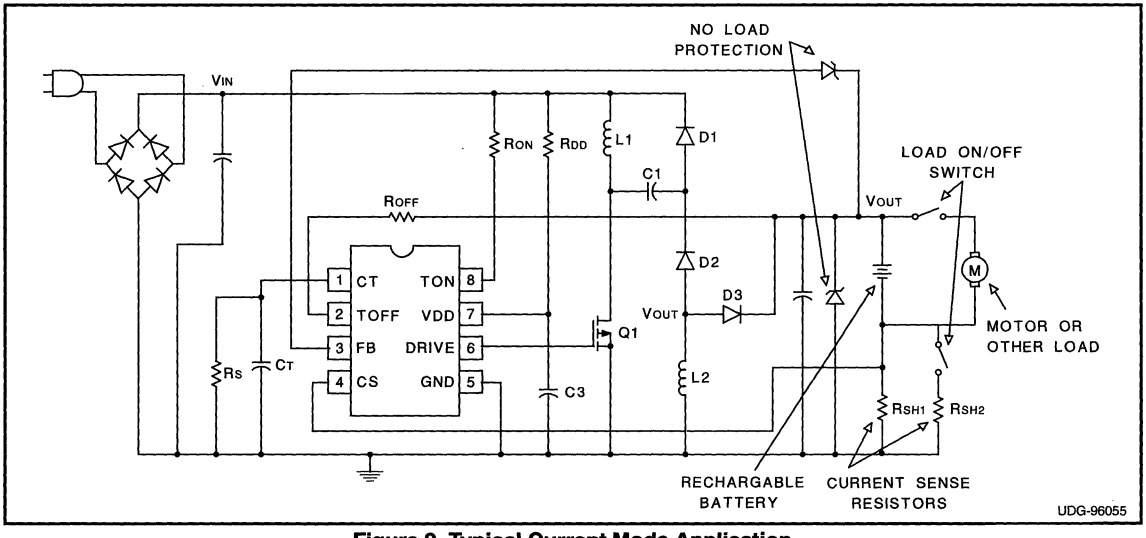


Figure 2. Typical Current Mode Application

APPLICATION INFORMATION (cont.)

If R_{SH2} is chosen so that

$$\frac{100mV}{R_{SH2}} = C$$

then the regulator output will assist the battery, minimizing or eliminating battery output current.

DESIGN EXAMPLE

A typical design has the following requirements:

V_{IN}	=	80 to 132 VAC or 100 to 180 VDC
V_{OUT}	=	1.25V
$V_{OUT'}$	=	2.0V (assumes 1.25 V_{OUT} with 750mV forward drop in D3)
I_{LOAD}	=	500mADC max
$F_{SWITCHING}$	=	100kHz
η (eff.)	=	50% (excluding efficiency losses in D3 which will be very large due to the low output voltage. Losses in D3 are accounted for by using $V_{OUT'}$ in the calculations).

Component values are indicated in Figure 3. The explanation for the choices in component values follows.

First calculate the maximum duty cycle, d(max). To calculate this assume that at maximum load/minimum line conditions, the converter will be at the continuous conduction boundary and there will be no idle time after the inductors are discharged. For all other load/line conditions, the UCC3890 will stretch the off time, to create an idle time after the inductors are discharged, in order to maintain a constant output voltage. For a single flyback stage at continuous conduction boundary

$$d = \frac{1}{1 + \frac{V_{IN}}{V_{OUT}}}$$

For the cascaded flyback stages of the UCC3890 topology, the corresponding equation is

$$d(max) = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT'}}}}$$

in this case

$$d(max) = \frac{1}{1 + \sqrt{\frac{100V}{2V}}} = 0.125$$

Next using the operating frequency and the maximum duty cycle to calculate the maximum on time

$$TON(max) = \frac{d(max)}{F_{SWITCHING}}$$

in this case

$$TON(max) = \frac{0.125}{100kHz} = 1.25\mu s$$

correspondingly

$$TOFF(min) = \frac{1 - 0.125}{100kHz} = 8.75\mu s$$

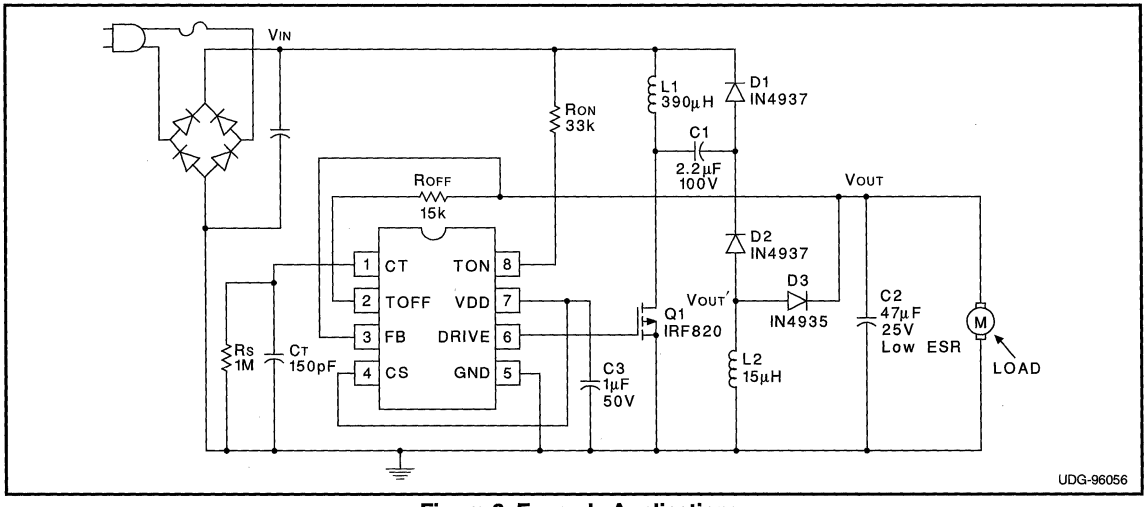


Figure 3. Example Application

APPLICATION INFORMATION (cont.)

The average input current at minimum line and maximum load will be

$$I_{IN} = \frac{I_{OUT}}{\eta} \bullet \frac{V_{OUT}'}{V_{IN}}$$

in this case

$$I_{IN} = \frac{500mA}{0.5} \bullet \frac{2V}{100V} = 20mA$$

Knowing that input current is drawn from the line only during TON, calculate the peak current in L1 to be

$$I_{L1}(pk) = 2 \bullet I_{IN} \bullet \frac{TON + TOFF}{TON}$$

in this case

$$I_{L1}(pk) = 2 \bullet 20mA \bullet \frac{1.25\mu s + 8.75\mu s}{1.25\mu s} = 320mA$$

Now calculate the value for L1

$$L_1 = V_{IN} \bullet \frac{TON}{I_{L1}(pk)}$$

in this case

$$L_1 = 100V \bullet \frac{1.25\mu s}{320mA} = 390\mu H$$

The output voltage of the first flyback stage is

$$V_{C1} = V_{IN} \bullet \frac{TON}{TOFF}$$

in this case

$$V_{C1} = 100V \bullet \frac{1.25\mu s}{8.75\mu s} = 14.3V$$

Knowing that output current is provided to the load only during TOFF, calculate the peak current in L2 to be

$$I_{L2}(pk) = 2 \bullet I_{OUT} \bullet \frac{TON + TOFF}{TOFF}$$

in this case

$$I_{L2}(pk) = 2 \bullet 0.5A \bullet \frac{1.25\mu s + 8.75\mu s}{8.75\mu s} = 1.14A$$

Now calculate the value of L2

$$L_2 = V_{OUT}' \bullet \frac{TOFF}{I_{L2}(pk)}$$

in this case

$$L_2 = 2V \bullet \frac{8.75\mu s}{1.14A} = 15\mu H$$

For all of the calculations so far only the maximum load/minimum line condition have been considered. The entire range of operation must be considered to choose values for the rest of the components.

Under all normal operating conditions the current ITON, (which is the current in RON), should be greater than 2mA and less than 7.5mA. In this case set RON to give ITON = 2.8mA at low line. The voltage at TON will be about 11V so

$$R_{ON} = \frac{100V - 11V}{2.8mA} = 33k\Omega$$

With RON = 33k, ITON at high line will be

$$I_{TON} = \frac{180V - 11V}{33k} = 5.1mA$$

At high line, the power dissipation in RON will be

$$P(R_{ON}) = (180V - 11V) \bullet 5.1mA = 860mW$$

RON will need to be at least a 1W resistor. Alternately it could be four 1/4W 8.2kΩ resistors in series.

Once RON is set, CT can be chosen. The charge current for CT is nominally 15% of ITON, and the nominal oscillator amplitude is 3.4V, so

$$TON = \frac{CT \bullet 3.4V}{0.15 \bullet I_{TON}}$$

solving for CT

$$CT = \frac{TON \bullet 0.15 \bullet I_{TON}}{3.4V}$$

ITON at low line is 2.8mA, and the target TON at low line is 1.25µs, so in this case

$$CT = \frac{1.25\mu s \bullet 0.15 \bullet 2.8mA}{3.4V} = 150pF$$

The final component to be chosen is ROFF, which determines the minimum value of TOFF. When the output voltage is below the regulation point, the discharge current for CT is equal to ITOFF (the current in ROFF). Under that condition

$$TOFF = \frac{CT \bullet 3.4V}{I_{TOFF}}$$

since the voltage at the TOFF pin = 0.4V

$$I_{TOFF} = \frac{V_{OUT} - 0.4V}{R_{OFF}}$$

substituting and solving for ROFF

$$R_{OFF} = \frac{T_{OFF} \bullet (V_{OUT} - 0.4V)}{CT \bullet 3.4V}$$

The largest discharge current, and hence the minimum off time, will occur when the output is about 10mV be-

APPLICATION INFORMATION (cont.)

low the regulation point of 1.25V. The minimum value for TOFF is 8.75µs. So in this case

$$R_{OFF} = \frac{8.75\mu s \bullet (1.24V - 0.4V)}{150pF \bullet 3.4V} = 15k$$

OTHER APPLICATION CONSIDERATIONS

Output Capacitor: For best regulation of the output voltage or current, the output capacitor should be a low ESR type. This is especially true when operating in current sense mode with a non-linear load such as a battery. If a low ESR capacitor cannot be used, excellent regulation can also be achieved by placing a low pass R/C filter between the current shunt and the CS input.

No Load Operation: The UCC3890 is inherently protected for short circuits, but not for open circuits. If the load is removed, the output voltage will quickly rise up to the regulation point. Once the output is above the regulation voltage, the oscillator will drop to the minimum frequency set by RS/CT. With no load on the output, even at this low frequency the output voltage can quickly rise to a dangerous level. To protect against this, it is recommended that a zener or other voltage clamp always be connected across the output. The clamp should be chosen to be above the normal range of output voltage, but low enough to protect the output capacitor. In current sense operation, removal of the load will also break the regulation loop, in which case a simple clamp on the output may not be adequate. In current sense mode it is recommended that a second zener be connected from the output to the FB pin, the breakdown voltage of this clamp chosen to be high enough so that it will not conduct during normal operation, but will conduct at least 2V lower than the breakdown voltage of the other clamp.

Gate Drive for the External FET: The UCC3890 is guaranteed to be able to deliver at least 1mA of steady state current to the gate of the external FET at ITON = 2mA. If ITON is higher than 2mA, 80% of the additional current is available to drive the FET gate. If, as in the design example above, a moderate sized FET such as the IRF820 is used, the operating frequency is 100kHz, and the minimum ITON at low line is 2.8mA, then the available gate drive current may be adequate. The IRF820 needs about 13nC to charge the gate on each cycle. At 100kHz, this is equivalent to 1.3mA steady state; below the minimum 1.64mA available. In some combinations of a larger FET, and/or higher frequency operation, the current available for driving the gate may not be adequate. In that case extra current may be provided by connecting a resistor RDD from the line input to the VDD pin. This resistor should be sized so that under all conditions the current input to VDD is below the 7.5mA absolute maximum limit. RDD will likely need to be a power resistor.

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application INFO available

UCC1895
UCC2895
UCC3895
PRELIMINARY

BiCMOS Advanced Phase Shift PWM Controller

FEATURES

- Programmable Output Turn-on Delay
- Adaptive Delay Set
- Bidirectional Oscillator Synchronization
- Capability for Voltage Mode or Current Mode Control
- Programmable Soft Start/Soft Stop and Chip Disable via a Single Pin
- 0% to 100% Duty Cycle Control
- 6.5MHz Error Amplifier
- Operation to 1MHz
- Low Active Current Consumption (5mA Typical @ 500kHz)
- Very Low Current Consumption During Undervoltage Lock-out (150µA typical)

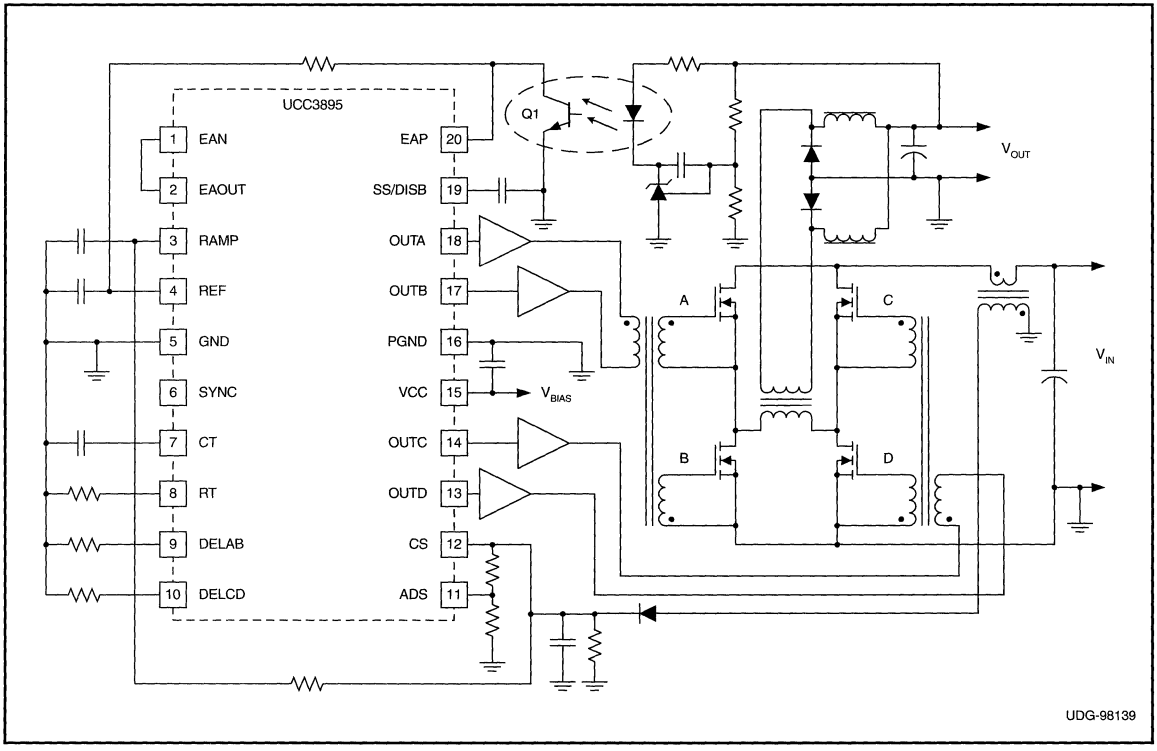
DESCRIPTION

The UCC3895 is a phase shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage mode or current mode controller.

While the UCC3895 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Since it is built in BCDMOS, it operates with dramatically less supply current than it's bipolar counterparts. The UCC3895 can operate with a maximum clock frequency of 1MHz.

The UCC3895 and UCC2895 are offered in the 20 pin SOIC (DW) package, 20 pin PDIP (N) package, 20 pin TSSOP (PW) package, and 20 pin PLCC (Q). The UCC1895 is offered in the 20 pin CDIP (J) package, and 20 pin CLCC package (L).

SIMPLIFIED APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (IDD < 10mA) 17V
Supply Current 30mA
REF current 15mA
OUT Current 100mA
Analog inputs
(EAP, EAN, EAOUT, RAMP,
SYNC, ADS, CS, SS/DISB) . . . . . –0.3V to REF+0.3V
Power Dissipation at T_A=+25°C (N Package) 1W
Power Dissipation at T_A=+25°C (D Package) 650mW
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +125°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

TEMPERATURE & PACKAGE SELECTION TABLE

	TEMPERATURE RANGE	PACKAGE SUFFIX
UCC1895	–55°C to +125°C	J, L
UCC2895	–40°C to +85°C	DW, N, PW, Q
UCC3895	0°C to +70°C	DW, N, PW, Q

ORDERING INFORMATION

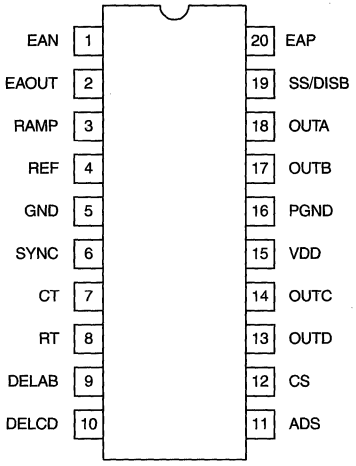
UCC□895 □

PACKAGE SUFFIX

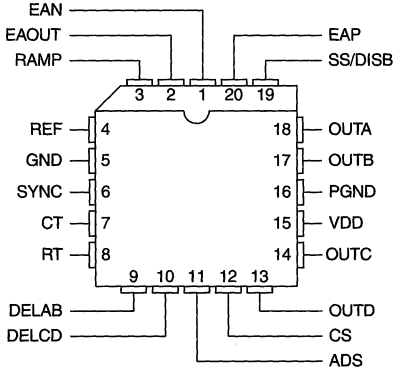
TEMPERATURE RANGE

CONNECTION DIAGRAMS

DIL-20,c SOIC-20, TSSOP-20 (TOP VIEW)
J or N Package, DW Package, PW Package



PLCC-20, CLCC-20 (TOP VIEW)
Q Package, L Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD=12V, RT=82k, CT=220pF, RDELAB=10k, RDELCD=10k, C_{REF}=0.1µF, C_{VDD}=1.0µF, no load at outputs. $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, –40°C to +85°C for UCC2895x, and –55°C to +125°C for UCC1895x.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
Start Threshold			11		V
Stop Threshold			9		V
Hysteresis			2		V
Supply Current					
Start-up Current	VDD = 8V		150	300	µA
I_{DD} Active			5		mA
VDD Clamp Voltage	IDD = 10mA		17.5		V
Voltage Reference Section					
Output Voltage	T_J = 25°C	4.95	5	5.05	V
	9V < VDD < 17.5V, 0mA < IREF < 5mA, Temperature	4.85	5	5.15	V
Short Circuit Current	REF = 0V, T_J = 25°C		20		mA
Error Amplifier Section					
Common Mode Input Voltage Range		–0.1		3.6	V
Offset Voltage		–5		5	mV
Input Bias Current (EAP, EAN)		–2		2	µA
EAOUT VOH	EAP–EAN = 500mV, I_{EAOUT}= –0.5mA	3.6	4	5	V
EAOUT VOL	EAP–EAN = –500mV, I_{EAOUT}= 0.5mA	0	0.3	0.4	V
EAOUT Source Current	EAP–EAN = 500mV, EAOUT= 2.5V	0.7	1		mA
EAOUT Sink Current	EAP–EAN = –500mV, EAOUT= 2.5V	2.5	3		mA
Open Loop DC Gain		70	80		dB
Unity Gain Bandwidth			6.5		MHz
Slew Rate	EAN from 1V to 0V, EAP = 500mV, EAOUT from 0.5V to 3.0V		2		V/µs
No Load Comparator Turn-Off Threshold			0.5		V
No Load Comparator Turn-On Threshold			0.6		V
Oscillator Section					
Frequency	T_J = 25°C	484	511	538	kHz
Total Variation	Line, Temperature		2.5	5	%
SYNC VIH			2.1		V
SYNC VIL			1.9		V
SYNC VOH	I_{SYNC} = –400µA, CT = 2.6V	4	4.3		V
SYNC VOL	I_{SYNC} = 100µA, CT = 2.6V		0.7	1	V
SYNC Output Pulse Width	SYNC Load = 1MEG and 10pF in parallel		75	125	ns
RT Voltage		2.9	3	3.1	V
CT Peak Voltage		2.45	2.5	2.55	V
CT Valley Voltage		0	0.1	0.2	V
PWM Comparator Section					
EAOUT to RAMP Input Offset Voltage	RAMP = 0V, DELAB = DELCD = REF	0.7	0.8	0.95	V
Minimum Phase Shift (OUTA to OUTC, OUTB to OUTD)	RAMP = 0V, EAOUT = 650mV (Note 1)	0	0.6		%
RAMP to OUTC/OUTD Delay	RAMP from 0V to 2.5V, EAOUT = 1.2V, DELAB = DELCD = REF (Note 2)		75		ns
RAMP Bias Current	0V < RAMP < 5V, SYNC = 0V to REF, CT = 0V	–5		50	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD=12V, RT=82k, CT=220pF, RDELAB=10k, RDELCD=10k, C_{REF}=0.1µF, C_{VDD}=1.0µF, no load at outputs. $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, –40°C to +85°C for UCC2895x, and –55°C to +125°C for UCC1895x.

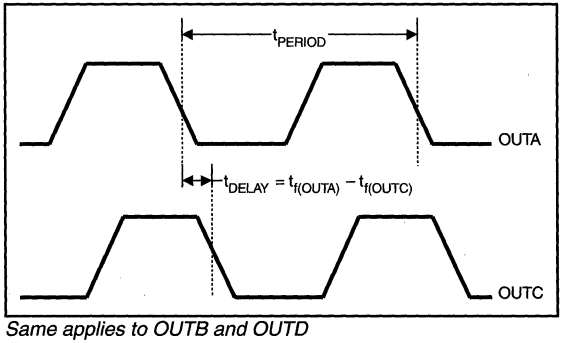
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
CS Bias Current	0 < CS , 2.5V, 0 < ADS < 2.5V	–3		20	µA
Peak Current Threshold			2		V
Overcurrent Threshold			2.5		V
CS to Output Delay	CS from 0 to 2.3V, DELAB = DELCD = REF		75		ns
Soft Start/Shutdown Section					
Soft Start Current	SS/DISB = 3.0V, CS < 1.9V		–37		µA
Soft Stop Current	SS/DISB = 3.0V, CS > 2.6V		370		µA
Soft Start/Disable Comparator Threshold			0.5		V
Delay Set Section					
DELAB/DELCD Output Voltage	ADS = CS = 0V		0.5		V
	ADS = 0V, CS = 2.0V		2.0.		V
Output Delay	ADS = CS = 0V (Note 2)		500		ns
ADS Bias Current	0V < ADS < 2.5V, 0V < CS < 2.5V	–20		20	µA
Output Section					
VOH (all outputs)	IOUT = –10mA, VDD to Output		250	350	mV
VOL (all outputs)	IOUT = 10mA		150	250	mV
Rise TIme	C_{LOAD} = 100pF		30		ns
Fall Time	C_{LOAD} = 100pF		20		ns

Note 1: Minimum phase shift is defined as followed:

$$\Phi = 200 \bullet \frac{t_{f(OUTA)} - t_{f(OUTC)}}{t_{PERIOD}} \quad Or$$

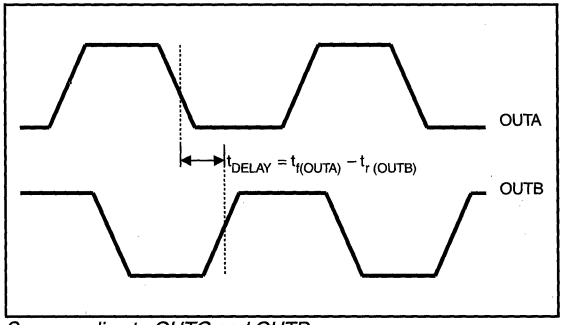
$$\Phi = 200 \bullet \frac{t_{f(OUTB)} - t_{f(OUTD)}}{t_{PERIOD}} \quad where$$

$t_{f(OUTA)}$ = *falling edge of OUTA signal*
$t_{f(OUTB)}$ = *falling edge of OUTB signal*
$t_{f(OUTC)}$ = *falling edge of OUTC signal*
$t_{f(OUTD)}$ = *falling edge of OUTD signal*
$t_{(PERIOD)}$ = *period of OUTA or OUTB signal*



Same applies to OUTB and OUTD

Note 2. Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is defined as shown below, where:
$t_{f(OUTA)}$ = *falling edge of OUTA signal*
$t_{r(OUTB)}$ = *rising edge of OUTB signal*



Same applies to OUTC and OUTD

PIN DESCRIPTIONS

ADS: Adaptive Delay Set. This function sets the ratio between the maximum and minimum programmed output delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2.0V (the Peak Current threshold), ADS changes the output voltage on the delay pins DELAB and DELCD by the following formula:

$$V_{DEL} = [0.75 \bullet (V_{CS} - V_{ADS})] + 0.5V$$

where V_{CS} and V_{ADS} are in Volts. ADS must be limited to between 0V and 2.5V.

EAOUT: Error Amplifier Output. It is also connected internally to the non-inverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500mV, and allows the outputs to turn-on again when EAOUT rises above 600mV.

CT: Oscillator Timing Capacitor. (Refer to Fig. 1, Oscillator Block Diagram) The UCC3895's oscillator charges CT via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.5V. The approximate oscillator period is calculated by the following formula:

$$t_{OSC} = \frac{5 \bullet R_T \bullet C_T}{48} + 75ns$$

where C_T is in Farads, and R_T is in Ohms and t_{OSC} is in seconds. C_T can range from 100pF to 880pF. Please note that a large C_T and a small R_T combination will result in extended fall times on the C_T waveform. The increased fall time will increase the SYNC pulse width, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter.

CS: Current Sense. This is the inverting input of the Current Sense comparator and the non-inverting input of the Over-current comparator, and the ADS amplifier. The current sense signal is used for cycle-by-cycle current limiting in peak current mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called "soft stop", with full soft start.

DELAB, DELCD: Delay Programming Between Complementary Outputs. DELAB programs the dead time between switching of outputs A and B, and DELCD programs the dead time between output C and D. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC3895 allows the user to select the delay, in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half-bridges to accommodate differences in resonant capacitor charging currents. The delay in each stage is set according to the following formula:

$$t_{DELAY} = \frac{(25 \bullet 10^{-12}) \bullet R_{DEL}}{V_{DEL}}$$

where V_{DEL} is in Volts, and R_{DEL} is in Ohms and t_{DELAY} is in seconds. DELAB and DELCD can source about 1mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay can be defeated by tying DELAB and/or DELCD to REF. For an optimum performance keep stray capacitance on these pins at <10pF.

EAP: The non-inverting input to the error amplifier.

EAN: The inverting input to the error amplifier.

GND: Chip ground for all circuits except the output stages.

OUTA–OUTD: The 4 outputs are 100mA complementary MOS drivers, and are optimized to drive FET driver circuits. Output A and B are fully complementary, always operate up to 50% duty cycle and one-half the oscillator frequency. A and B outputs are intended to drive one half-bridge circuit in an external power stage. Outputs C and D will drive the other half-bridge and will have the same characteristics as OUTA and OUTB. Output C is phase shifted with respect to Output A, and Output D is phase shifted with respect to Output B. Note that changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

PGND: Output Stage Ground. To keep output switching noise from critical analog circuits, the UCC3895 has 2 different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, since PGND carries high current, board traces must be low impedance.

PIN DESCRIPTIONS (cont.)

RAMP: The Inverting Input of the PWM Comparator. This pin receives either the CT waveform in voltage and average current mode controls, or the current signal (plus slope compensation) in peak current mode control.

RT: Oscillator Timing Resistor. (Refer to Fig. 1, Oscillator Block Diagram) The oscillator in the UCC3895 operates by charging an external timing capacitor, CT, with a fixed current programmed by R_T. R_T current is calculated as follows:

$$I_{RT} = \frac{3.0V}{R_T}$$

where R_T is in Ohms and I_{RT} is in Amperes. R_T can range from 40kΩ to 120kΩ Soft start charging and discharging current are also programmed by I_{RT} .

SS/DISB: Soft Start/Disable. This pin combines the 2 independent functions.

Disable Mode: A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5V, externally forcing REF below 4V, or if VDD drops below the undervoltage lockout threshold. In the case of REF being pulled below 4V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

Note that if externally forcing SS/DISB below 0.5V, the pin will start to source current equal to I_{RT}.

If an overcurrent fault is sensed (CS ≥ 2.5V), a "soft stop" is initiated. In this mode, SS/DISB will sink a constant current of (10 • I_{RT}). The soft stop will continue until SS/DISB falls below 0.5V. When any of these faults are detected, all outputs are forced to ground immediately. Note that the only time the part switches into low I_{DD} current mode, though, is when the part is in undervoltage lockout.

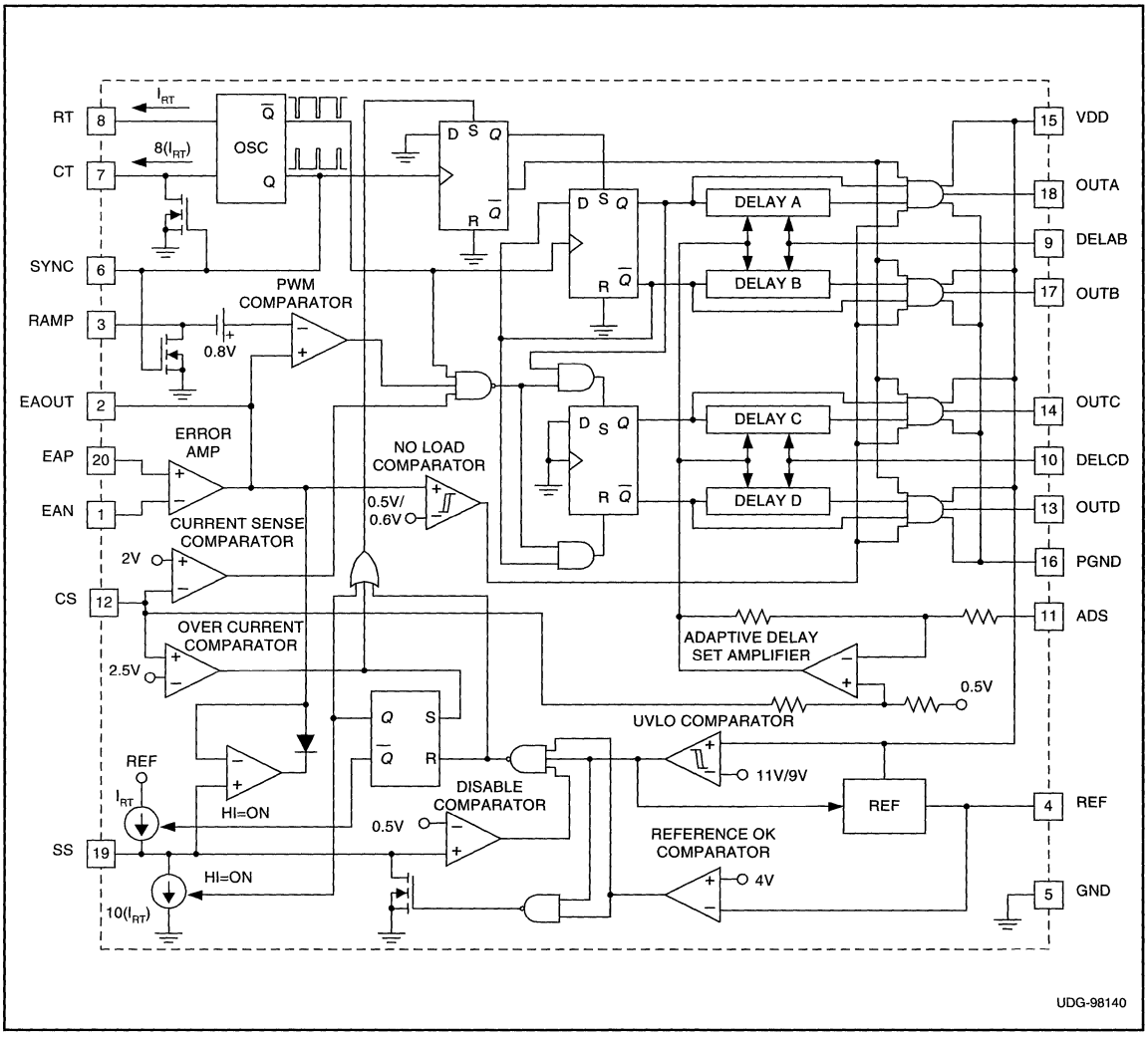
Soft Start Mode: After a fault or disable condition has passed, VDD is above the start threshold, and/or SS/DISB falls below 0.5V during a soft stop, SS/DISB will switch to a soft start mode. The pin will now source current, equal to I_{RT}. A user selected resistor/capacitor combination on SS/DISB determines the soft start time constant. Note that SS/DISB will actively clamp the EAOUT pin voltage to approximately the SS/DISB pin voltage during both soft start, soft stop, and disable conditions.

SYNC: Oscillator Synchronization. (Refer to Fig. 1, Oscillator Block Diagram) This pin is bidirectional. When used as an output, SYNC can be used as a clock, which is the same as the chip's internal clock. When used as an input, SYNC will override the chip's internal oscillator and act as it's clock signal. This bidirectional feature allows synchronization of multiple power supplies. The SYNC signal will also internally discharge the CT capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level sensitive, with an input low threshold of 1.9V, and an input high threshold of 2.1V.

VDD: Power Supply. VDD must be bypassed with a minimum of a 1.0µF low ESR, low ESL capacitor to ground.

REF: 5V, ±2% voltage reference. The reference supplies power to internal circuitry, and can also supply up to 5mA to external loads. The reference is shut down during undervoltage lock-out but is operational during all other disable modes. For best performance, bypass with a 0.1µF low ESR, low ESL capacitor to ground

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

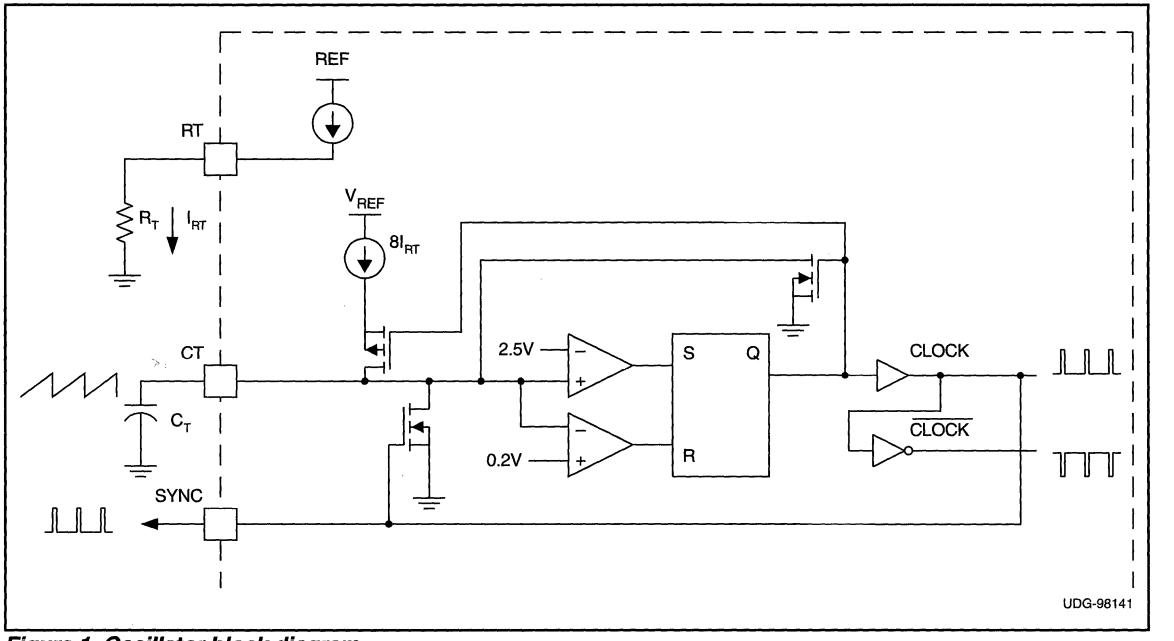


Figure 1. Oscillator block diagram.

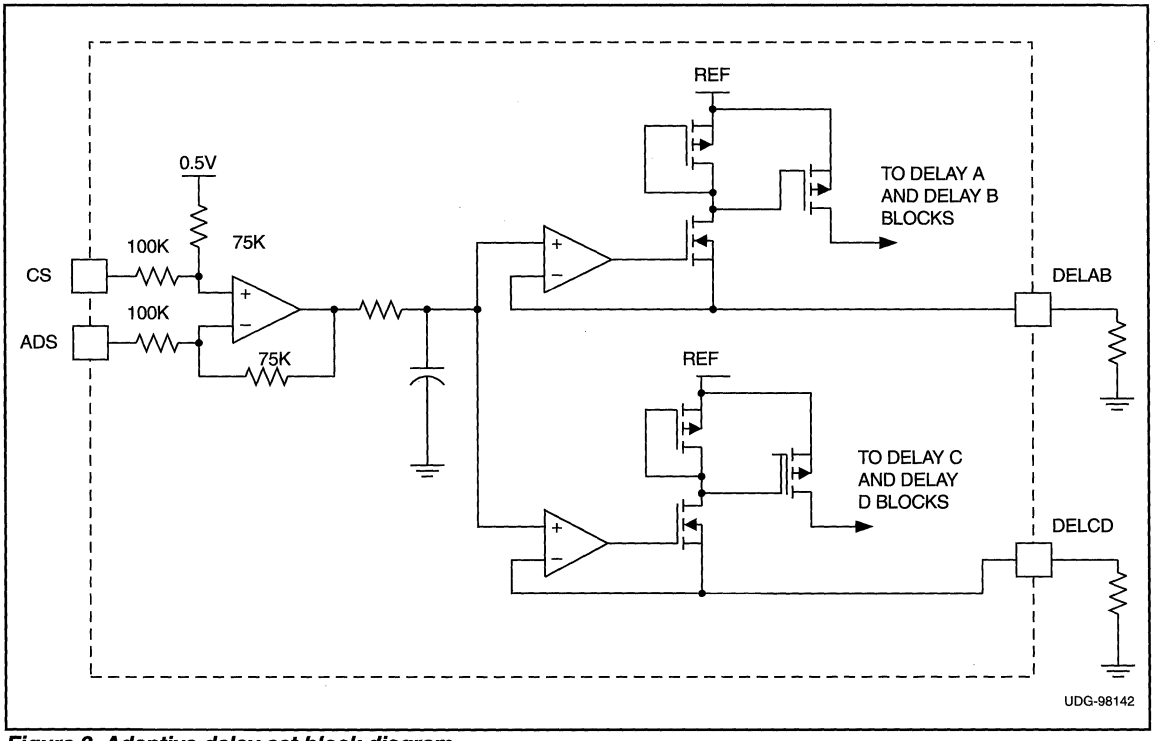


Figure 2. Adaptive delay set block diagram.

CIRCUIT DESCRIPTION (cont.)

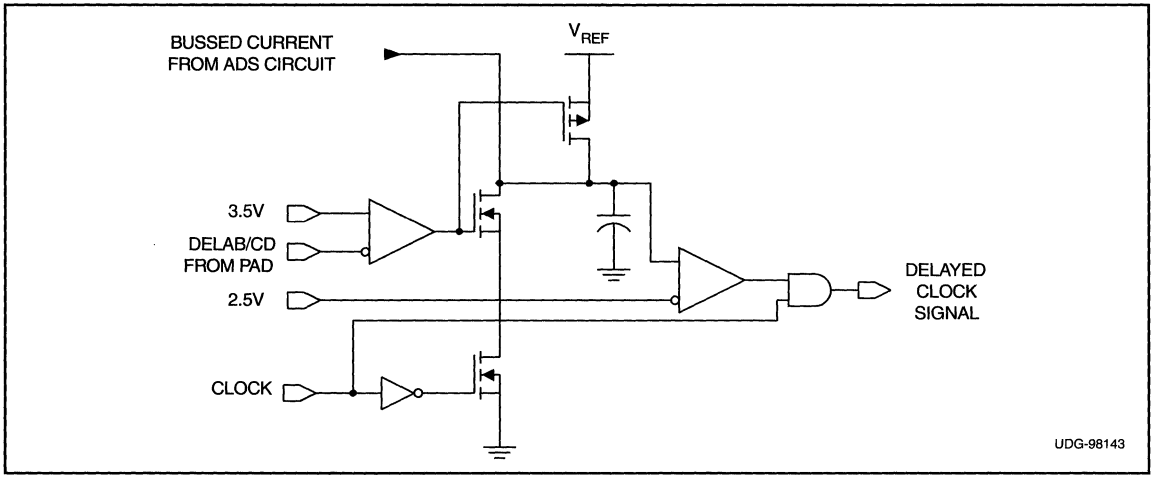


Figure 3. Delay block diagram (one delay block per output).

APPLICATION INFORMATION

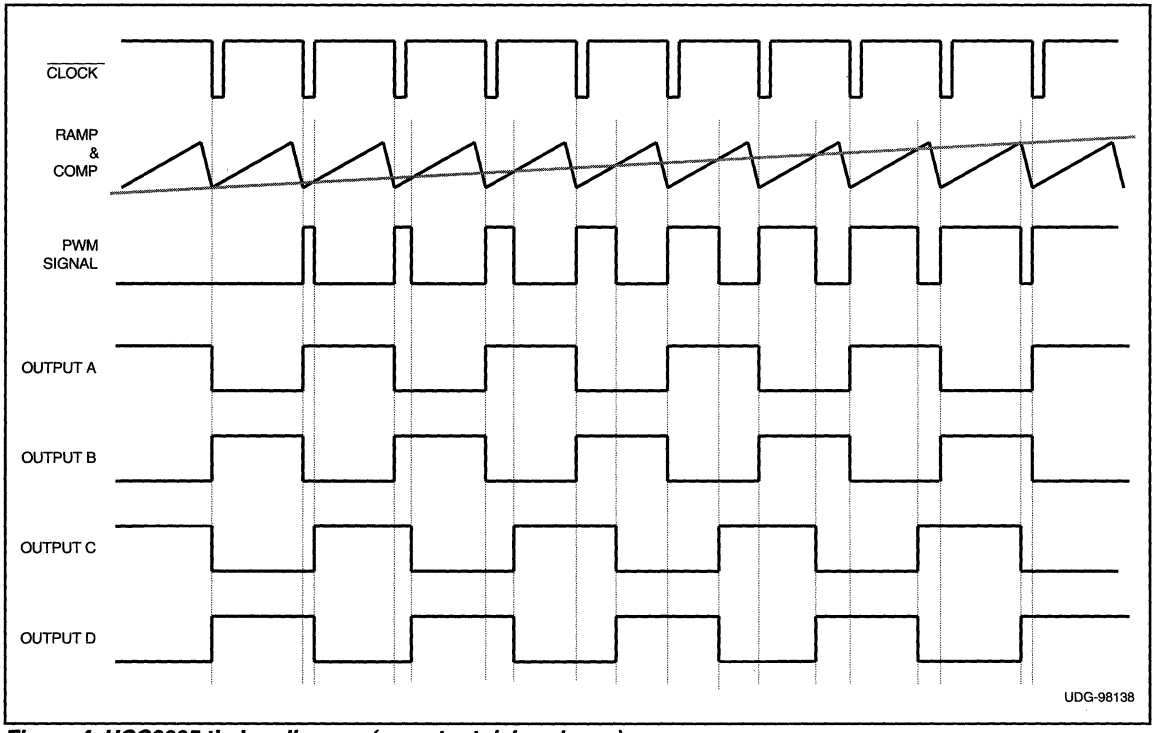


Figure 4. UCC3895 timing diagram (no output delay shown).

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ADVANCE INFORMATION

5-Bit Programmable Output BiCMOS Precision Voltage Reference

FEATURES

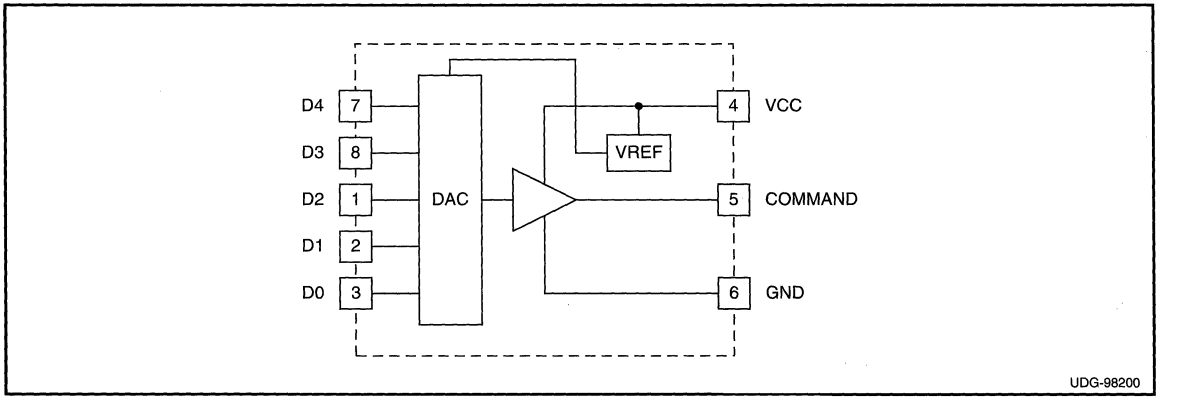
- 5 - Bit Digital-to-Analog Converter (DAC) supports Intel Pentium II™ Microprocessor VID Codes
- Compatible with 5V Systems
- 1% Output Voltage Accuracy Guaranteed

DESCRIPTION

The UCC391 provides an accurate reference, programmable by a 5-bit DAC, in a tiny 8 pin package. Using few external components, the UCC391 converts 5V to an adjustable output ranging from 3.5VDC to 2.1VDC in 100mV steps and 2.05VDC to 1.3VDC in 50mV steps with 1% DC system accuracy.

This device is available in and 8 pin surface mount (150mm SOIC) and TSSOP packages and is specified for operation from 0°C to 70°C.

BLOCK DIAGRAM



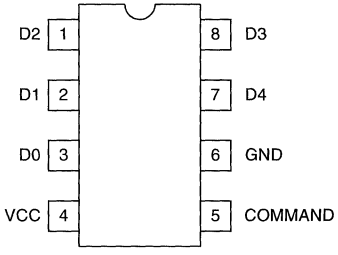
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 8V
Input Voltage, D0, D1, D2, D3, D4 . . . . . 8V

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

MSOP-8, TSSOP-8 (TOP VIEW)
P, PW Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A = 0°C to 70°C for the UCC391, $T_A = T_J$. V_{CC} = 5V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, On	V_{CC} = 5V		1.8		mA
DAC Reference Section					
COMMAND Voltage Accuracy	4.5V < V_{IN} < 5.5V, measured on COMMAND, 0°C < T_A < 70°C (Note 1)	–1.00		1.00	%
D0 – D4 Voltage High		4.5	5	5.5	V
D0 – D4 Voltage Threshold			2.5		V
D0 – D4 Input Bias Current	V(D4, D3, D2, D1, D0) < 0.5V		–90	–20	µA
Output Current (Maximum Load)	I_{OUT} ($V_{COMMAND}$)	0		150	µA

***Note 1**: Reference and output amplifier offsets are trimmed out before packaging.*

PIN DESCRIPTIONS

GND: (Ground) All voltages measured with respect to ground. VCC should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor.

VCC: (Positive supply voltage) This pin is normally connected to a 5V ± 10% system voltage. Bypass VCC directly to GND with a 0.1µF (minimum) ceramic capacitor.

COMMAND: This pin is the output of the IC. It is controlled by the 5-bit input word (D0:D4). This output will have a ±1% system accuracy over temperature, process, and input voltage.

D0, D1, D2, D3, D4: These are the digital input control codes for the DAC. The DAC is comprised of two ranges set by D4, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND; a bit is set high by floating the pin. Each control pin is pulled up to approximately 5V by an internal pull-up. If all ones are commanded on the DAC inputs (no CPU command), the output will be disabled.

APPLICATION INFORMATION

D4	D3	D2	D1	D0	V_{OUT}
0	1	1	1	1	1.3
0	1	1	1	0	1.35
0	1	1	0	1	1.4
0	1	1	0	0	1.45
0	1	0	1	1	1.5
0	1	0	1	0	1.55
0	1	0	0	1	1.6
0	1	0	0	0	1.65
0	0	1	1	1	1.7
0	0	1	1	0	1.75
0	0	1	0	1	1.8
0	0	1	0	0	1.85
0	0	0	1	1	1.9
0	0	0	1	0	1.95
0	0	0	0	1	2
0	0	0	0	0	2.05
1	1	1	1	1	NO OUTPUT
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table I. VID Codes and Resulting Regulator Output Voltage

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application INFO available

UC1910
UC2910
UC3910

4-Bit DAC and Voltage Monitor

FEATURES

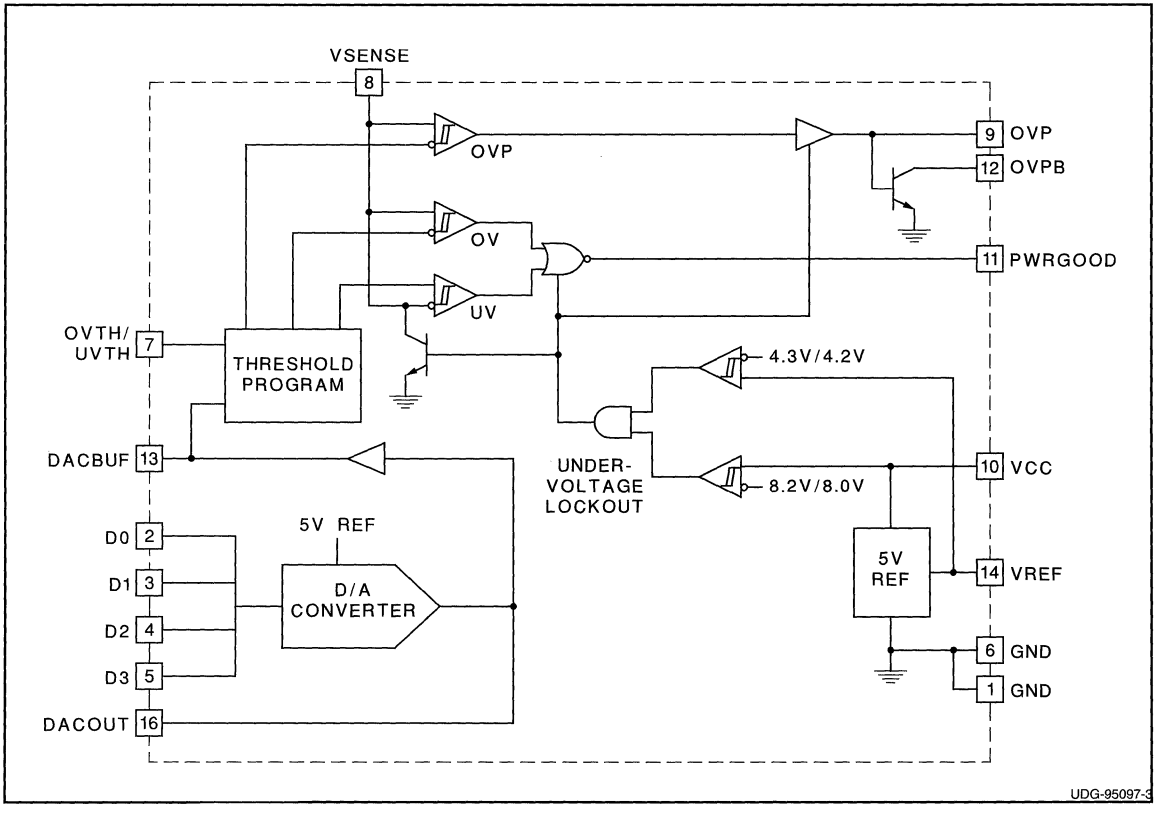
- Precision 5V Reference
- 4-Bit Digital-to-Analog (DAC) Converter
- 0.5% DAC/Reference Combined Error
- Programmable Undervoltage and Overvoltage Fault Windows
- Overvoltage Comparator with Complementary SCR Driver and Open Collector Outputs
- Undervoltage Lockout

DESCRIPTION

The UC3910 is a complete precision reference and voltage monitor circuit for Intel Pentium® Pro and other high-end microprocessor power supplies. It is designed for use in conjunction with the UC3886 PWM. The UC3910 together with the UC3886 converts 5VDC to an adjustable output ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

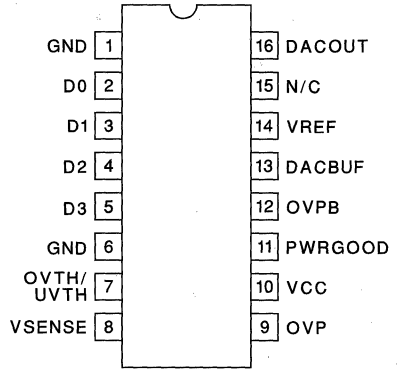
The UC3910 utilizes thin film resistors to ensure high accuracy and stability of its precision circuits. The chip includes a precision 5V voltage reference which is capable of sourcing 10mA to external circuitry. The output voltage of the DAC is derived from this reference, and the accuracy of the DAC/reference combination is 0.5%. Programmable window comparators monitor the supply voltage to indicate that it is within acceptable limits. The window is programmed as a percentage centered around the DAC output. An overvoltage protection comparator is set at a percentage 2 times larger than the programmed lower overvoltage level and drives an external SCR as well as provides an open collector output. Undervoltage lockout protection assures the correct logic states at the outputs during power-up and power-down.

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J, N, or D Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
V_{IN} UVLO Turn-on Threshold		7	8	9	V
UVLO Threshold Hysteresis		50	200	500	mV
Supply Current					
I_{IN} Startup	VCC = 5V		2	3.5	mA
I_{IN}	VCC = 12V		10	12	mA
DAC/Reference					
DACOUT Voltage Accuracy	Line, Load, 0°C < T_A < 70°C (Note 1)	–0.9		0.9	%
	Line, Load, –55°C < T_A < 125°C	–1.5		1.5	%
D0-D3 Voltage High	Dx Pin Floating	4.6	4.85		V
D0-D3 Input Bias Current	Dx Pin Tied to GND	–140	–105		µA
VREF Output Voltage	I_{VREF} = 0mA, 0°C < T_A < 70°C	4.97	5	5.03	V
VREF Total Variation	Line, Load, 0°C < T_A < 70°C (Note 1)	4.96	5	5.04	V
	Line, Load, –55°C < T_A < 125°C	4.925	5	5.075	V
VREF Sourcing Current	VREF = 0V	10			mA
DAC Buffer					
Input Offset Voltage	I_{DACBUF} = –1mA, 0°C < T_A < 70°C	–25		25	mV
Output Sourcing Current		–12		–1	mA
Monitor Circuitry (Note 2)					
VSENSE UV Threshold Voltage	Code 0, Ratio = 0.45 (Note 3)	3.174	3.237	3.3	V
	Code 0, Ratio = 0.9	2.87	2.975	3.08	V
	Code 15, Ratio = 0.45	1.816	1.85	1.884	V
	Code 15, Ratio = 0.9	1.635	1.7	1.765	V
VSENSE OV Threshold Voltage	Code 0, Ratio = 0.45	3.7	3.763	3.826	V
	Code 0, Ratio = 0.9	3.92	4.025	4.13	V
	Code 15, Ratio = 0.45	2.116	2.15	2.184	V
	Code 15, Ratio = 0.9	1.635	2.3	2.365	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VCC = 12V, VSENSE = 3.5V, $V_{OVTH/UVTH}$ = 1.26V, $V_{D0} = V_{D1} = V_{D2} = V_{D3}$ = 0V, 0°C < T_A < 70°C for the UC3910, –25°C < T_A < 80°C for the UC2910, –55°C < T_A < 125°C for the UC1910 $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Monitor Circuitry (Note 2) (cont.)					
VSENSE OVP Threshold Voltage	Code 0, Ratio = 0.45	3.937	4.025	4.113	V
	Code 0, Ratio = 0.9	4.41	4.55	4.69	V
	Code 15, Ratio = 0.45	2.235	2.3	2.365	V
	Code 15, Ratio = 0.9	2.505	2.6	2.695	V
OV, UV Comparator Hysteresis	Code 0, Ratio = 0.9	70	88	120	mV
	Code 15, Ratio = 0.45	15	25	40	mV
OVP Comparator Hysteresis	Code 0, Ratio = 0.9	160	218	300	mV
	Code 15, Ratio = 0.45	40	62	85	mV
Input Common Mode Range	OV, UV, OVP Comparators	0		5	V
Propagation Delay	OV, UV Comparators			5	µs
	OVP Comparator			5	µs
PWRGOOD, OVP, OVPB Outputs					
PWRGOOD Voltage Low	$I_{PWRGOOD}$ = 10mA			0.4	V
OVP Sourcing Current	V_{OVP} = 1.4V	65			mA
OVPB Voltage Low	I_{OVPB} = 1mA			0.4	V

Note 1: "Line, Load" implies that the parameter is tested at all combinations of the conditions: 10.8V < VCC < 13.2V, –2mA < I_{VREF} < 0mA.

Note 2: These are the actual voltages on VSENSE which will cause the OVPB and PWRGOOD outputs to switch, assuming the DACOUT voltage is perfect. These limits apply for 0°C < T_A < 70°C.

Note 3: "Code 0" means pins D0 - D4 are all low; "Code 15" means they are all floating or high (See Table 1). "Ratio" is the divider ratio of the resistor string between DACBUF and OVTH/UVTH (See Figure 1).

PIN DESCRIPTIONS

D0-D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB) (See Table 1). A bit is set low by being connected to GND; a bit is set high by floating it, or connecting it to a 3V to 5V voltage source. Each control pin is pulled up to approximately 4.8V by an internal 40µA current source.

DACBUF (Buffered DACOUT Voltage): This pin provides a buffered version of the DACOUT voltage to allow external programming of the OV/UV thresholds (see OVTH/UVTH below).

DACOUT (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital to analog (DAC) converter. Setting all input control codes low produces 3.5V at DACOUT; setting all codes high produces 2.0V at DACOUT. The LSB step size (i.e. resolution) is 100mV (See Table 1). The DACOUT source impedance is typically 3kΩ and must therefore drive a high impedance input. Bypass DACOUT at the driven input with a 0.01µF, low ESR, low ESL capacitor for best circuit noise immunity.

Table 1. Programming the DACOUT Voltage

Decimal Code	D3	D2	D1	D0	DACOUT Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

PIN DESCRIPTIONS (cont.)

GND (Signal Ground): All voltages are measured with respect to GND. The two GND pins are connected together internally but should also be connected externally using a short PC board trace. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near one of the signal ground pins.

OVP (Overvoltage Comparator Output): This output pin drives an external SCR circuit with up to 65mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below). The OVP comparator hysteresis is a function of both the DACBUF voltage and the OV/UV percentage programmed.

OVPB (Overvoltage Comparator Complementary Output): This output is a complement to the OVP output (see above) and provides an open collector capable of sinking 1mA when the voltage on VSENSE rises above its nominal value by a percentage set by the voltage on the OVTH/UVTH pin (see below).

OVTH/UVTH (Undervoltage and Lower Overvoltage Threshold Input): This pin is used to program the window thresholds for the OV and UV comparators. The OV-UV window is centered around the DACBUF voltage and can be programmed from ±5% to ±15% about DACBUF. Connect a resistor divider between DACBUF and GND to set the percentage. The threshold for the OVP comparator is internally set to a percentage 2 times larger than the programmed OV percentage; therefore, its range extends from 10% to 30% above DACBUF.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open collector output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by a percentage programmed by OVTH/UVTH. The OV and UV comparators' hysteresis is a function of the DACBUF voltage and the OV/UV programmed percentage.

VCC (Positive Supply Voltage): This pin supplies power to the chip. Connect VCC to a stable voltage source of at least 9V and capable of sourcing at least 15mA. The OVP and PWRGOOD outputs are held low, the OVPB output is in a high impedance state, and the VSENSE pin is pulled low until VCC exceeds the upper undervoltage lockout threshold. This pin should be bypassed directly to the GND pin with a 0.1µF low ESR, low ESL capacitor.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference, capable of delivering up to 10mA to external circuitry, and is internally short circuit current limited. For best reference stability, bypass VREF directly to the GND pin with a 0.1µF, low ESR, low ESL capacitor.

VSENSE (Output Voltage Sensing Input): This pin is the input to the OVP and PWRGOOD comparators and is connected to the system output voltage through a lowpass filter. When choosing the resistor value for this filter, make sure that no more than 500µA will flow through the resistor when VSENSE is grounded.

APPLICATION INFORMATION

The Overvoltage (OV), Undervoltage (UV) and Overvoltage Protection Voltage (OVP) threshold detections voltages are programmed as a percentage about the nominal DAC output voltage, DACOUT. Figure 1 illustrates how to program the UC3910 by setting a voltage divider, R_{DIV}, at the OVTH/UVTH pin. The voltage divider ration is defined as:

$$R_{DIV} = \frac{RS1}{RS1 + RS2}$$

The UC3910 allows a ratio R_{DIV} at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Fig. 2.

The OV, UV and OVP percentage thresholds are given by:

$$\%V_{OV} = R_{DIV} \bullet 16.7$$
$$\%V_{UV} = -(R_{DIV} \bullet 16.7)$$
$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

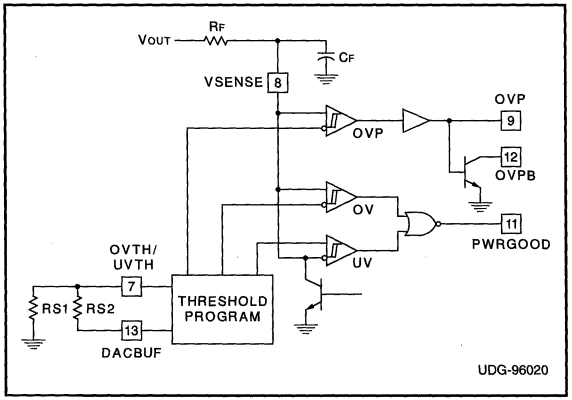


Fig 1. Setting the OV/UV/OVP threshold percentages.

APPLICATION INFORMATION (cont.)

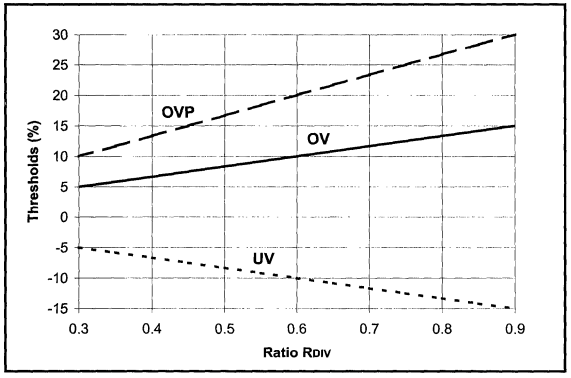


Figure 2. OV, UV and OVP percentage thresholds as a function of the divider ratio R_{DIV}.

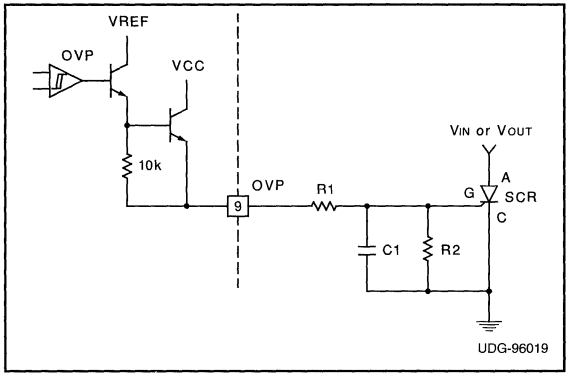


Figure 3. Driving and SCR using the UC3910 OVP signal.

An R-C filter is added to the VSENSE pin to filter noise and ripple at the comparator inputs. An R-C filter frequency of $F_{SWITCH}/10$ is recommended. Choose the value of R_F therefore such that it limits the current into VSENSE to ≤ 0.5mA.

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet \left(\frac{F_{SWITCH}}{10}\right)}, \qquad R_F \geq \frac{V_{OUT}}{0.5mA}$$

The Overvoltage Protection output, OVP, can be used to directly drive a crowbarring SCR, as shown in Figure 3.

A typical application is shown in Figure 4 using the UC3910 together with the UC3886 Average Current Mode PWM Controller for IC for a power supply to drive Intel's Pentium® Pro processor.

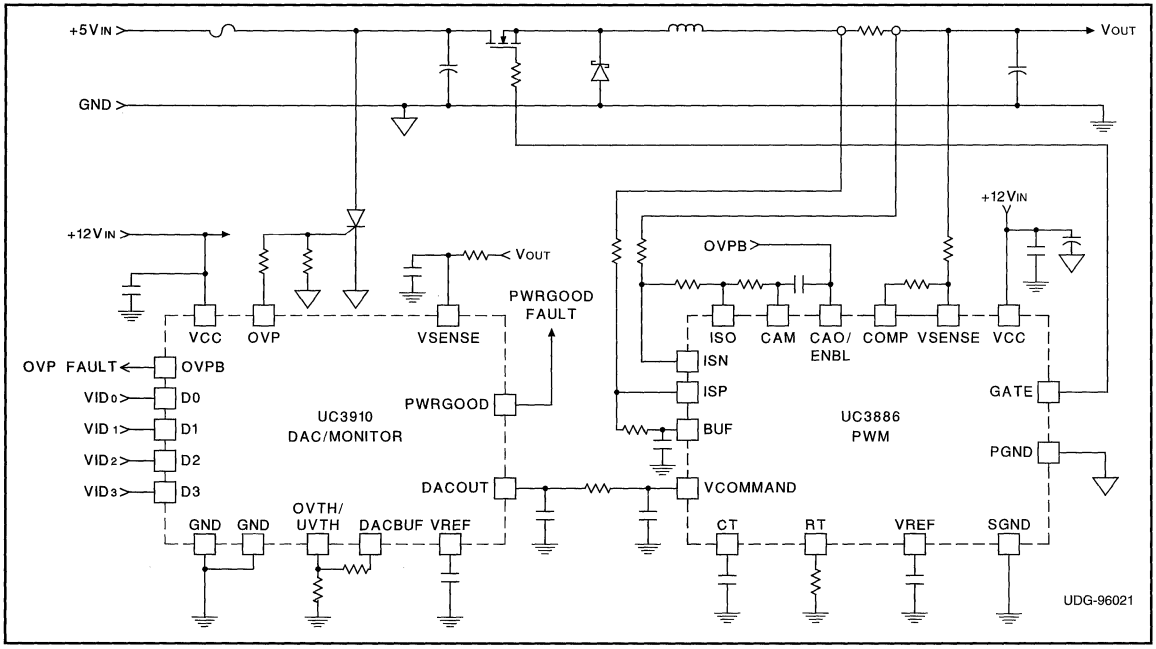


Figure 4. UC3910 Configured with the UC3886 for a Pentium® Pro DC/DC Converter

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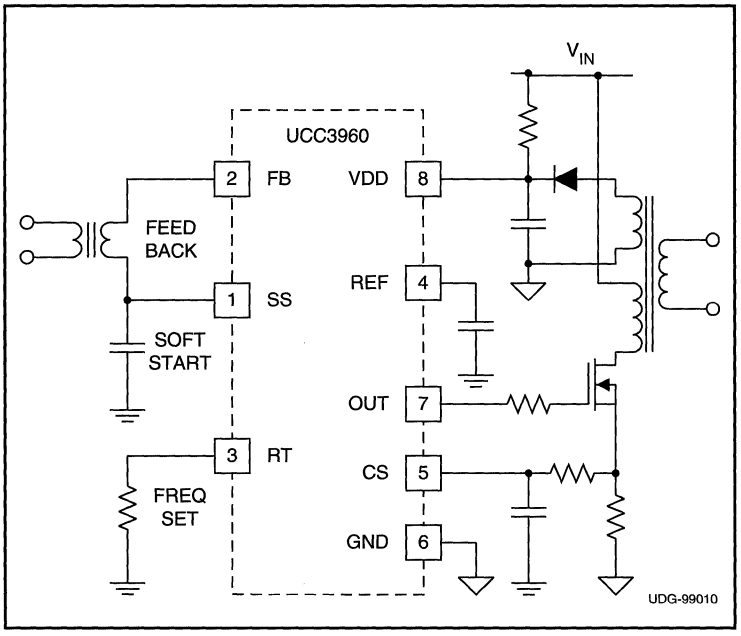
UCC1960
UCC2960
UCC3960
ADVANCE INFORMATION

Primary-Side Startup Controller

FEATURES

- Operates with Secondary-Side PWM Control
- Isolated PWM Command through a Pulse Transformer
- Initial Free-running Soft Startup with Duty-Cycle Clamping
- Up to 400kHz Synchronizable Switching Frequency
- High current FET drive (1.5A sink, 0.75A source)
- Overcurrent Protection
- Under Voltage LockOut with 2V hysteresis
- Low-Current Startup

TYPICAL APPLICATION DIAGRAM



DESCRIPTION

The UCC3960 Primary-Side Startup Controller is a unique solution which provides all the primary-side functions required for a single-ended, isolated off-line, switch-mode power converter which utilizes secondary-side PWM control. It is usable with a wide range of secondary circuits and is especially well suitable for systems where sophisticated handling of overload conditions is required.

Secondary-side control assumes that output voltage and current measurements are interfaced directly to an output ground-referenced PWM stage which develops the power switch command for the supply. This digital PWM command can then be transmitted to the primary-side power switch through a simple and low-cost isolating pulse transformer. With secondary-side control, it is much easier to monitor and control the system load with tightly coupled analog control loops. Load oriented features such as output current sharing and synchronous rectification are implemented more easily. The UCC3960 additionally allows the use of an extremely small and low-cost pulse transformer for higher converter bandwidth. This eliminates the loop gain variations due to initial accuracy and aging of an opto-coupler feedback element or the size penalty of a gate transformer.

UCC3960 provides all the circuitry required on the primary side of a secondary-side controlled power supply. The UCC3960 features low current startup (100µA) with active low during UVLO, under-voltage lockout with 2V hysteresis, soft-start capability, a 5V reference, high current power output for driving N-Channel MOSFETs, a free running 360kHz to 60kHz oscillator which is synchronizable to the secondary side PWM signal, and the ability to accept start/stop PWM commands from an isolating pulse transformer.

In a non-typical use, the UCC3960 can accommodate an analog feedback signal through an opto-isolator where it can operate in voltage mode control mode with primary side peak current limiting.

The UCC3960 and the UCC2960 are available in the 8 pin SOIC (D) and PDIP (N) packages. The UCC1960 is available in 8 pin CDIP (J) package. A full feature version is available in a 14 pin package as UCC3961 which includes multimode over-current protection, volt-second clamp, programmable over and under voltage sense lines and the self bias regulator.

ABSOLUTE MAXIMUM RATINGS

VDD
- Voltage Driven 19V
- Current Driven 25mA

I_{OUT} 4nF load with 4Ω series resistor . . . . . –1.5A/2A
I_{REF} . . . . . –7.5mA
SS, RT, REF, CS . . . . . –0.3V to VDD+0.3V
FB . . . . . –6.0V to VDD+0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

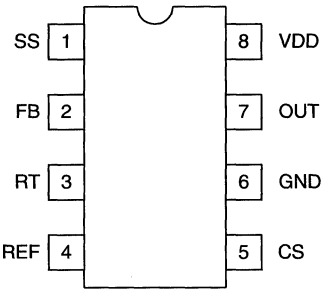
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and specification of packages.

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UCC1960J	–55°C to +125°C	CDIP
UCC2960D	–40°C to +85°C	SOIC
UCC2960N		PDIP
UCC3960D	0°C to +70°C	SOIC
UCC3960N		PDIP

CONNECTION DIAGRAMS

SOIC-8, DIL-8 (Top View)
D, N and J Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated these parameters apply for VDD = 12V, RT=56.3k, C_{VDD} = 1µF, C_{REF} = 0.1µF, C_{SS} = 0.01µF, R_{OUT} = 4Ω, C_{OUT} = 1nF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section (VDD)					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD} Operating	No load	1.8	2.3	2.8	mA
I_{VDD} Starting	V_{DD} = 7.5V	100	150	200	µA
Undervoltage Lockout Section					
UVLO Start Threshold		9.5	10	10.5	V
UVLO Hysteresis		1.9	2	2.1	V
Voltage Reference Section (REF)					
VREF		4.75	5.0	5.25	V
Load Regulation	I_{REF} = 0mA to –2.5mA		4		mV
Line Regulation	V_{DD} = 10V to 12V		4		mV
Short Circuit Current			10	15	mV
Soft Start Section (SS)					
SS Discharge Current	SD = 4.5V Pulsed		6		µA
SS Charge Current	SD = 4.5V Pulsed		–6		µA
V_{SS} Low Threshold			1		V
V_{SS} Clamp Threshold			5		V
R_{SS} ON	V_{DD} = 7.5V	600	700	800	Ω
Current Sense Section (CS)					
CS Threshold	Pulse-by-Pulse	0.92	1	1.08	V
	Immediate	1.26	1.37	1.49	V
CS Input Bias	CS = 1.1V Pulsed			0.1	µA
CS to OUT Delay		50	75	100	ns
R_{CS} ON		600	700	800	Ω

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for VDD = 12V, RT=56.3k, C_{VDD} = 1µF, C_{REF} = 0.1µF, C_{SS} = 0.01µF, R_{OUT} = 4Ω, C_{OUT} = 1nF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Section					
OUT Frequency		127.5	150	172.5	kHz
OUT Frequency Charge with Voltage	V_{DD} = 10V to 12V		0.1		%/V
OUT Minimum Duty Cycle			0		%
OUT Maximum Duty Cycle		63	70	70	%
Output Section (OUT)					
Output V_{SAT} Low	I_{OUT} = 100mA (dc) (Note 1)		0.7	1.0	V
Output V_{SAT} High (VDD-OUT)	I_{OUT} = –40mA (dc) (Note 2)		0.56	1.0	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc), V_{DD} = 7.5V			1.5	V
Rise Time			30	60	ns
Fall Time	RT = 133.3k		15	30	ns
Feedback Section (FB)					
FB-SS, Positive Differential Voltage	FB-SS Pulsed, FB = SS	2	2.5	7	V
FB-SS, Negative Differential Voltage	FB-SS Pulsed, FB = SS	–2	–2.5	–7	V
Input Bias Current	FB = 4.5V, SS = 0V			0.1	µA
FB Negative Compliance	I_{FB} = –100µA, SS = 0V	–6.8	–7.2	–7.6	V
Rising Edge FB-SS to OUT Delay	FB-SS Pulsed = 2V, FB = SS	50	75	100	ns
Falling Edge FB-SS to OUT Delay	FB-SS Pulsed = 2V, FB = SS	100	125	150	ns

Note 1: OUT Low, nominal of 0.7V reflects the 3Ω DMOS ON resistance plus 4Ω R_{SERIES}.

Note 2: OUT High (VDD-OUT), nominal of 0.56V reflects the 10Ω HVPMOS ON resistance plus 4Ω R_{SERIES}.

PIN DESCRIPTIONS

GND: This pin is the reference point for grounding all analog functions and must be kept as clean as possible from all switching noise. It should be closely bypassed to VDD.

CS: This is the pulse-by-pulse and shutdown over-current sense input pin. This Current Sense pin will trigger a pulse-by-pulse termination anytime a 1.0V threshold is exceeded while a signal in excess of 1.375V on this pin will initiate a complete shutdown. Since the CS pin can be noise sensitive, it is good practice to insert a small low-pass RC filter between this pin and the current sensor.

FB: This is the control input for the signal from a secondary-side PWM controller whose pulse-width command has been differentiated by the feedback pulse edge transformer into positive "start" and negative "stop" pulses. These signals are used to turn on and off the primary power switch and must have an amplitude of at least ±2.0V (4V peak-to-peak).

OUT: This is the drive pin for the MOSFET power switch and will both sink (1.5A) and source (0.75A) fast, high-current gate drive pulses. During shutdown, this pin is self-biased to an active low state. A minimum of 4Ω should be added in series with the output to ensure that the on chip driver safe operating area is not exceeded. (Data from the IRF820/830/840 family of MOSFETs, commonly available in the TO-220 package, is used to derive this value. The gate charge needed to provide full enhancement was used to establish an equivalent capacitance of up to 4000pF.)

RT: A resistor from this pin to GND establishes a current, $I_{SET} = \frac{2V}{RT}$ which is mirrored internally for several functions. It establishes the free-running startup switching frequency with an internal capacitor according to the relationship, $fs = \frac{8.0 \times 10^9}{RT}$. The startup oscillator has a rise and fall time set to limit the duty-cycle of the power switch to a maximum of 70%, a limit which is maintained even after the feedback signal takes command.

PIN DESCRIPTIONS

REF: This is a 5V output usable with external loads of up to 10mA. This voltage is also the source for all internal analog threshold settings and should be bypassed with a minimum of 0.1µF capacitance to GND.

SS: The pin implements the primary side soft start function. This is the connection point for an external capacitor which determines the rate of increase in commanded pulse width for the power switch at startup. It also serves as the AC ground return for the feedback pulse transformer to provide a tracking bias for the FB input.

VDD: This is the power input connection for all the control circuitry and, in addition, conducts all the gate charge current for the power FET. It should be closely bypassed with at least 1.0µF to GND. This pin is internally shunt regulated to clamp at 17.5V to protect the internal components so if a voltage source above this value is possible, external current limiting must be provided.

BLOCK DIAGRAM

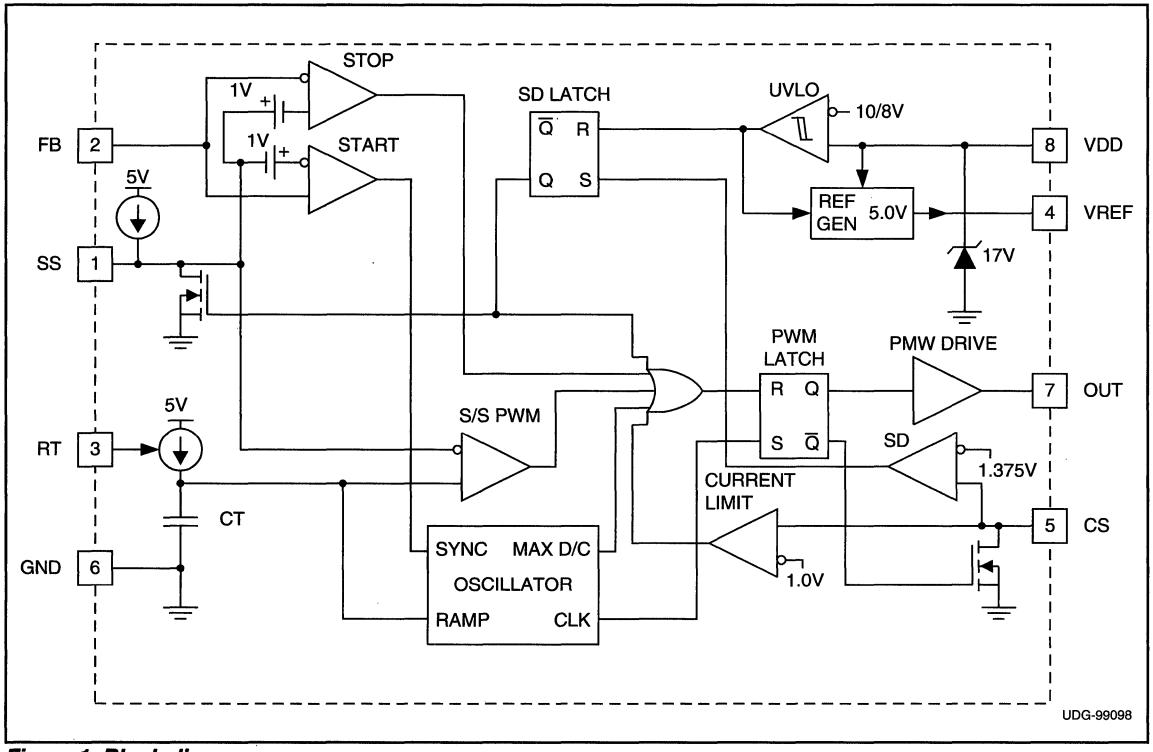


Figure 1. Block diagram.

CIRCUIT DESCRIPTION

Start-up Oscillator Section

The RT pin is connected to an internal 2.0V nominal, unity gain closed loop amplifier which is referenced to a voltage divider off the 5.0V reference. When a 22.22kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 90μA internal current is realized which charges the internal oscillator capacitor, approximately 58pF. I_{RT} = 90μA produces a maximum free running oscillator frequency of 360KHz at a 70% duty cycle. When a 133.33kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 15μA internal current is realized which produces a minimum free running oscillator frequency of 60KHz at a 70% duty cycle. The approximately 70% maximum duty cycle is setup by on chip MOSFET current mirrors which are not programmable.

Any frequency between these two limits (6:1 maximum to minimum frequency) is obtainable by linearly scaling the RT resistance between the minimum 22.22kΩ and maximum 133.33kΩ values. The secondary side PWM frequency should be fixed at (1 / 0.9) or 1.11 times the user programmed primary side free running oscillator frequency for proper primary side synchronization. Therefore, in all cases the recommended secondary side synchronization frequency shall be 1.11 times higher than the selected primary side free running start up frequency. Taking into consideration the two extreme limits for primary side free running start up frequency, the secondary side operating frequency should be set between 400kHz and 67kHz.

Soft Start Section

The Soft Start section contains all the circuitry required to produce a user programmable slowly increasing PWM duty cycle, starting from 0% to a maximum of 70%. The Soft Start cycle is triggered either by the initial primary side Start-up procedure or after any one of three user programmable fault conditions and one fixed fault condition. The PWM duty cycle increases according to the charge rate of an user selectable external Soft Start capacitor, connected from the SS pin to GND. The SS capacitor is charged by a nominal 6uA internal current source.

Voltage comparators referenced to a 4.0V threshold monitor the OVS pin, SD pin and the UVS pin and trigger a Soft Start cycle when a fault condition is detected on any of these pins. Should the CS pin rise in voltage above 1.375V a Soft Start cycle will also be triggered. The Soft Start cycle disables the output driver OUT and holds it in the low state until the capacitor connected from the SS pin to GND is discharged below 1.0V by an internal 6μA current sink. After this discharge period the PMW output OUT is enabled and the duty cycle is allowed to slowly increase as before.

Synchronization Section

The SS pin and the FB pin accepts the secondary side of a small signal synchronization transformer. A series blocking capacitor inserted in the primary side of the synchronization transformer is intended to differentiate the square wave gate drive output of the secondary side PWM controller while preventing the transformer from saturation. The SS capacitor also provides an AC GND at the SS pin or the synchronization transformer secondary. The small signal synchronization transformer provides galvanic isolation between primary and secondary side and must have adequate voltage breakdown rating between the primary and secondary windings.

Two comparators, with an approximate 1.0V offset each, are connected to the FB pin to provide plus and minus differential voltage comparison with a 2.0V deadband between the FB and SS pins. The 2.0V deadband prevents inductive backswing of the small signal transformer from giving false secondary side pulse edge detection.

Enough energy must be coupled into the comparator differential inputs to ensure reliable comparator switching. This requires sufficient voltage overdrive above the 1.0V comparator threshold and a specified transformer circuit time constant to provide a minimum synchronization pulse width.

On receiving the first recognizable negative going voltage pulse (turn-off command) generated from the falling edge of the differentiated square wave gate drive signal on the secondary side, the PWM latch is RESET and a synchronization latch is SET. After this event all primary side PMW driver output is slaved to the secondary side driver output in both frequency and duty cycle. The triggering of a Soft Start cycle by a fault condition will RESET the synchronization latch to again allow the internal Start-up oscillator to control the PWM latch.

PWM Section

The PWM section consists of a reset dominant SR latch with necessary logical gating on the SET input to allow control from the free running Start-up Oscillator until feedback from the secondary side PWM gate drive output is detected. After the occurrence of detectable feedback from the secondary side gate driver, the control of the primary side PWM latch is handed off to the secondary side PWM controller. A nine input OR gate on the PWM latch reset dominant input allows the numerous fault conditions to RESET the PWM latch and control from either the Start-up oscillator or feedback from the secondary side PWM output driver.

CIRCUIT DESCRIPTION (cont.)

UVLO & REF Sections

The under voltage lockout (UVLO) circuit will enable normal operation after VDD exceeds the 10.0V turn-on threshold and permits operation until VDD falls below the 8V turn-off threshold. While activated, the UVLO circuit holds the PWM gate driver output (OUT) and the internal reference buffer amplifier output REF low. To insure proper Soft Start, internal NMOS FET switches discharge external capacitor connected to the SS pin during under voltage conditions.

The 5V internal reference is connected to the REF pin and must be bypassed using a good quality, high frequency capacitor. This 5V reference is not available externally while the chip is disabled by the under voltage lockout circuit.

CS Section

The Current Sense (CS) circuit monitors the voltage across a ground referenced current sense resistor, connected between the source of the external power MOSFET and GND. The signal amplitude at the CS pin is compared to two, a 1.0V and a 1.375V, thresholds by two independent voltage comparators.

A voltage level greater than 1.0V, but less than 1.375V, will SET the reset dominant Shut Down latch and RESET the PWM latch. The SD latch is RESET by the Start-up oscillator arriving at it's 4.0V compare threshold.

During the OFF period of the PWM latch any capacitance connected to the CS pin is discharged to GND potential by an internal 700Ω device.

VDD Clamp Section

To insure that the absolute maximum voltage ratings of internal devices are not violated, an internal shunt voltage regulator is provided to clamp the VDD pin at a nominal 17.5V maximum voltage. Similarly to other shunt or zener like voltage regulator circuits the current through the internal VDD clamp must be limited below the maximum current level indicated in the datasheet. In addition to limiting the current through the clamp circuit, the maximum power dissipation capability of the particular package used in the application has to be considered.

OUT Driver Section

An internal output driver OUT is provided to drive the gate of an external N-channel power MOSFET. The output driver consists of a nominal 4.0Ω ON resistance PMOS FET for turn-on, and a nominal 2.0Ω ON resistance DMOS FET utilized during the turn-off of the external MOSFET transistor. An external series gate resistance is specified to maintain an acceptable SOA (Safe Operating Area) for the DMOS device of the internal output driver. As discussed in the UVLO section before, the under voltage lockout (UVLO) circuit holds the PWM gate driver output low while UVLO conditions exists.

APPLICATION INFORMATION

The evaluation circuit of UCC3960 as the primary side startup circuit and UC3845 as the secondary side controller is shown in Fig. 2.

Pulse Edge Transmission Circuit

The UCC3960 uses a Pulse Edge Transmission (PET) circuit to transmit isolated gate pulse information from the secondary side controller. It is important for the PET circuit to have proper frequency response and adequately high damping (low Q factor) in order to prevent excessive overshoot. The circuit is shown below.

The pulse width measured at the FB pin must be between 25nsec wide and 200nsec wide, measured at 1 Volt above and at 1 Volt below the Soft Start voltage. The FB voltage must not be overdriven by more than 5V above or 5V below the Soft Start voltage. In order to prevent false triggering, the FB voltage must not ring pelloast the Soft Start voltage by more than ±0.9V. This can be met if the Pulse Edge Transmission circuit has a resonant frequency of 880kHz and a Q of 0.25. For further details, refer to Design Note DN-99, *Pulse Edge Transmission Circuit*. The following values will meet those specifications for a 12 Volt Secondary Gate Pulse signal, over the full range of UCC3960 operating frequencies.

T1 1:1 turns ratio, L_M=5.4µH, Feronics 11-622J, N1 = N2 = 4 turns

R1 300Ω

C1 2700pF

R2 200Ω

APPLICATION INFORMATION

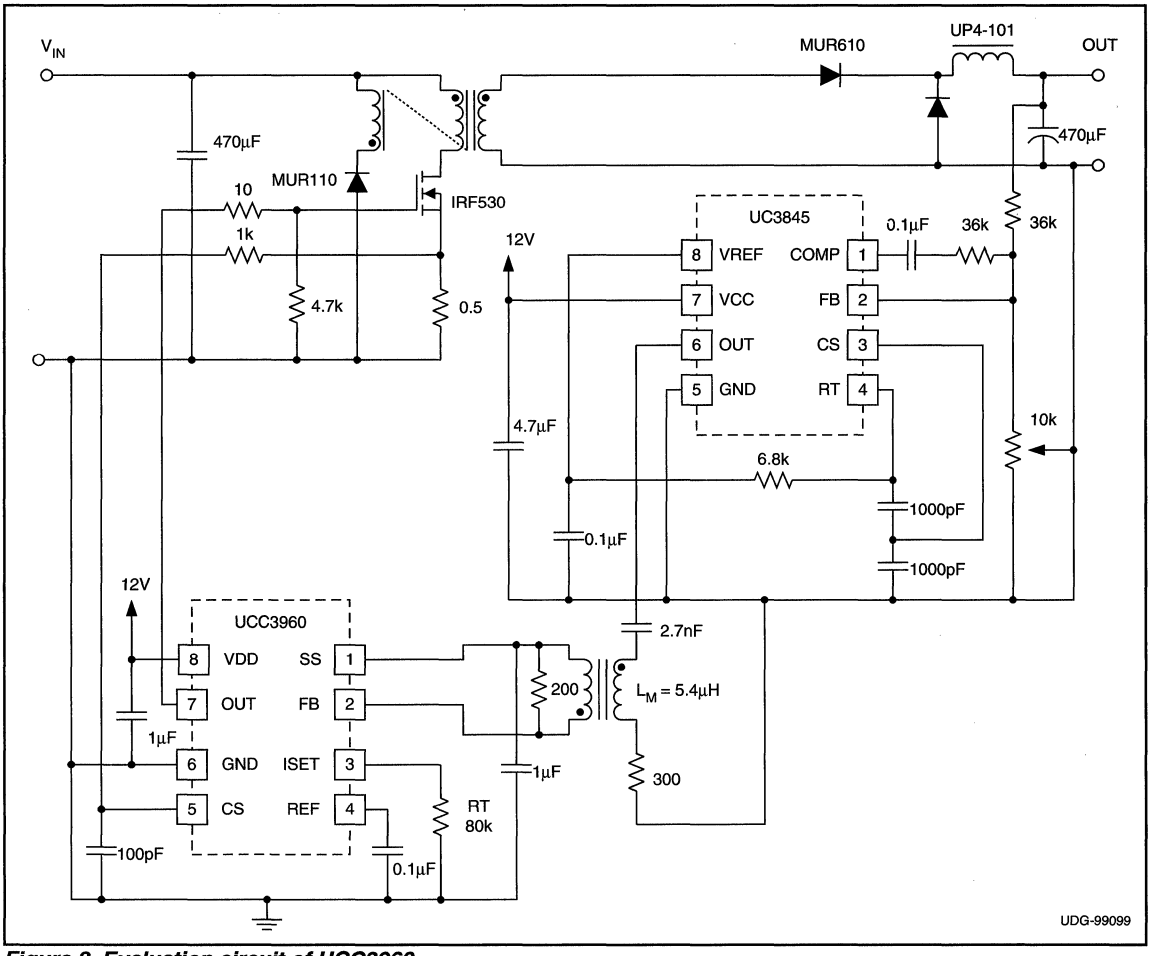


Figure 2. Evaluation circuit of UCC3960.

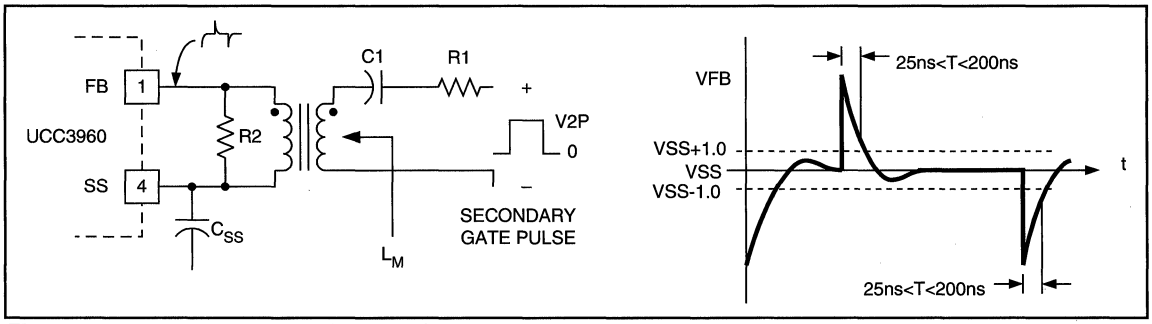


Figure 3. Pulse edge transmission circuit.

TYPICAL WAVEFORMS

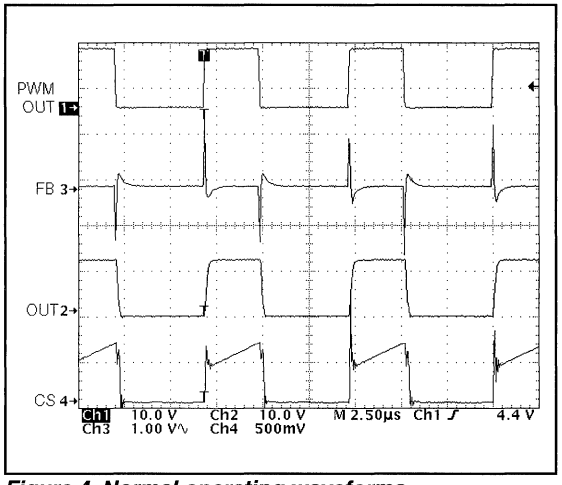


Figure 4. Normal operating waveforms.

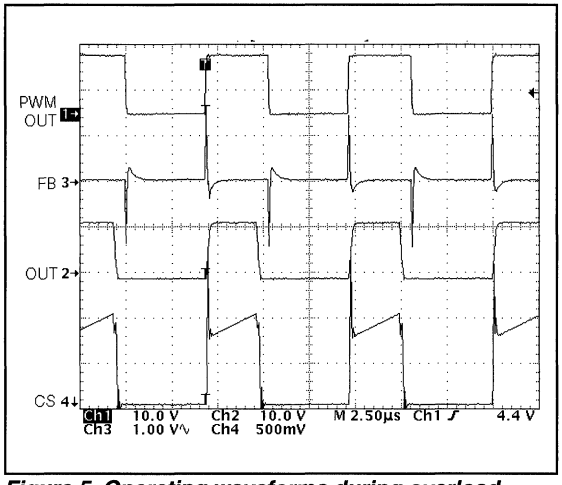


Figure 5. Operating waveforms during overload.

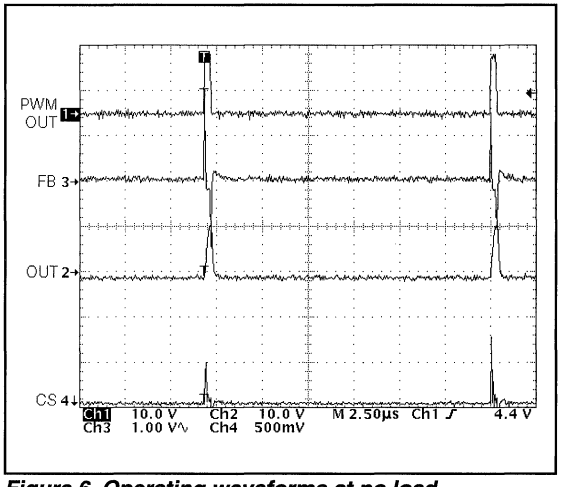


Figure 6. Operating waveforms at no load.

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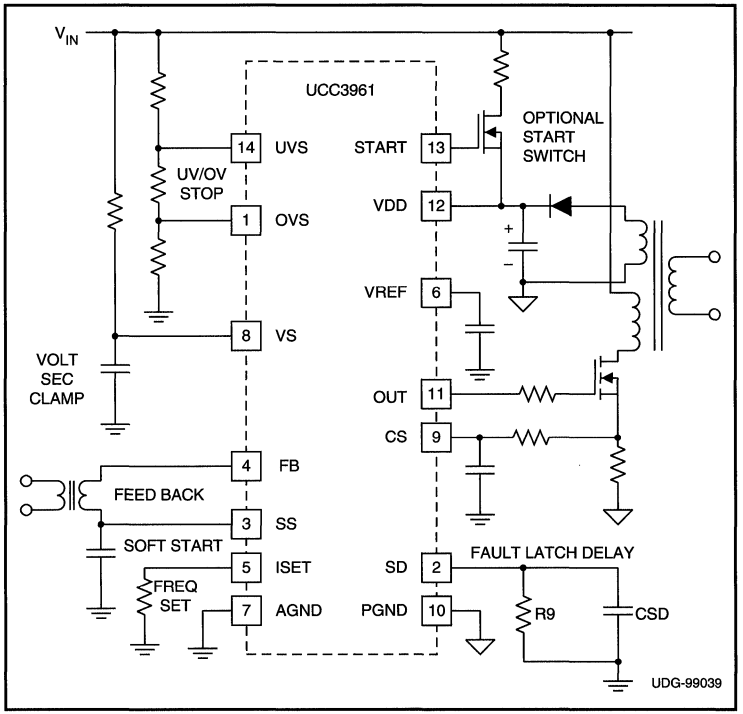
UCC2961
UCC3961
ADVANCE INFORMATION

Advanced Primary-Side Startup Controller

FEATURES

- Operates with Secondary-Side PWM Control
- Isolated PWM Command through a Pulse Transformer
- Initial Free-running Soft Startup with Duty-Cycle Clamping
- Up to 400kHz Synchronizable Switching Frequency
- High current FET drive (1.5A sink, 0.75A source)
- Multi-Mode Over-Current Protection with Restart, Latching, or Cycle-by-Cycle Current Limiting
- Programmable Volt-Second Clamp for Transformer Reset
- Under Voltage LockOut with 2V hysteresis
- Low-Current Startup with Optional Disconnect
- Programmable Over- and Under-Voltage Protection

TYPICAL APPLICATION DIAGRAM



DESCRIPTION

The UCC3961 Advanced Primary-Side Startup Controller is a unique solution which provides all the primary-side functions required for a single-ended, isolated off-line, switch-mode power converter which utilizes secondary-side PWM control. It is usable with a wide range of secondary circuits and is especially well suitable for systems where sophisticated handling of overload conditions is required.

Secondary-side control assumes that output voltage and current measurements are interfaced directly to an output ground-referenced PWM stage which develops the power switch command for the supply. This digital PWM command can then be transmitted to the primary-side power switch through a simple and low-cost isolating pulse transformer. The advantages of secondary-side control are tightly coupled analog control loops, monitoring and control functions that easily interfaces to the system load, incorporation of output current sharing, generation of drive signals for synchronous rectification, and the use of a low-cost pulse transformer instead of opto-couplers which also allows higher converter bandwidth and eliminates the loop gain variations caused by the aging and initial accuracy of the optical feedback element.

UCC3961 provides all the circuitry required on the primary side of a secondary-side controlled power supply. The IC allows implementation of initial startup with optional high voltage disconnect after starting, input voltage monitoring with turn-off for either under- or over-voltage, primary power switch current protection, pulse-by-pulse current limiting plus shutdown after a programmable delay, and continuous input volt-second clamping to insure protection from transformer saturation. UCC3961 also features a multi purpose, bi-directional shutdown pin which can be used to modify the converter's behavior in overload conditions. The possible configurations include continuous peak current limiting, delayed or immediate shutdown with full cycle soft restart or fully latched overcurrent shutdown.

The UCC3961 and the UCC2961 are available in the 14 pin SOIC (D) and PDIP (N) packages. The UCC1961 is available in 14 pin CDIP (J) package. For applications where only startup and control are desired, a simplified version of this product is offered in an 8-pin package as the UCC3960.

(continued)

DESCRIPTION (cont.)

The additional features of the UCC3961 include low current startup (100μA) with active low during UVLO, under-voltage lockout with 2V hysteresis, soft-start capability, a 5V reference, high current power output for driving N-Channel MOSFETs, a free running 360kHz to 60kHz oscillator which is synchronizable to the secondary side PWM signal, and the ability to accept start/stop PWM commands from an isolating pulse transformer.

In a non-typical use, the UCC3961 can accommodate an analog feedback signal through an opto-isolator where the UCC3961 then can operate in voltage mode control mode with primary side peak current limiting.

ABSOLUTE MAXIMUM RATINGS

VDD
- Voltage Driven 19V
- Current Driven 25mA

I_{OUT} 4nF load with 4Ω series resistor . . . . . –1.5A/2A
I_{REF} . . . . . –7.5mA
OVS, SD, SS, RT, REF, VS, CS, START, UVS . . . . . –0.3V to VDD+0.3V
FB . . . . . –6.0V to VDD+0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

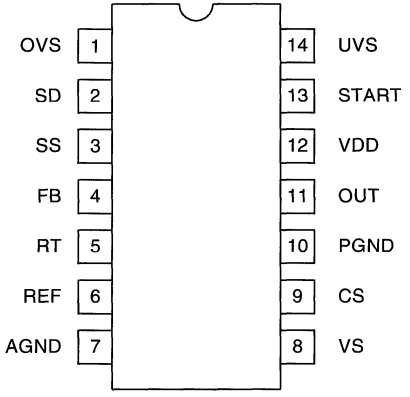
All voltages are with respect to ground unless otherwise stated. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and specification of packages.

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UCC1961J	–55°C to +125°C	CDIP
UCC2961D	–40°C to +85°C	SOIC
UCC2961N	–40°C to +85°C	PDIP
UCC3961D	0°C to +70°C	SOIC
UCC3961N	0°C to +70°C	PDIP

CONNECTION DIAGRAMS

SOIC-14, DIL-14 (Top View)
D, N and J Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated these parameters apply for VDD = 12V, RT=56.3k, C_{VDD} = 1μF, C_{REF} = 0.1μF, C_{SS} = 0.01μF, R_{OUT} = 4Ω, C_{OUT} = 1nF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section (VDD)					
VDD Clamp	I_{VDD} = 10mA	16	17.5	19	V
I_{VDD} Operating	No load	1.8	2.3	2.8	mA
I_{VDD} Starting	V_{DD} = 7.5V	100	150	200	μA
Undervoltage Lockout Section					
UVLO Start Threshold		9.5	10	10.5	V
UVLO Hysteresis		1.9	2	2.1	V
Voltage Reference Section (REF)					
VREF		4.75	5.0	5.25	V
Load Regulation	I_{REF} = 0mA to –2.5mA		4		mV
Line Regulation	V_{DD} = 10V to 12V		4		mV
Short Circuit Current			10	15	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for VDD = 12V, RT=56.3k, C_{VDD} = 1µF, C_{REF} = 0.1µF, C_{SS} = 0.01µF, R_{OUT} = 4Ω, C_{OUT} = 1nF and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Sense Section (OVS)					
OVS Threshold		3.68	4	4.32	V
OVS Input Bias Current				0.1	µA
Undervoltage Sense Section (UVS)					
UVS Threshold		3.68	4	4.32	V
UVS Input Bias Current				0.1	µA
Soft Start Section (SS)					
SS Discharge Current	SD = 4.5V Pulsed		6		µA
SS Charge Current	SD = 4.5V Pulsed		–6		µA
V_{SS} Low Threshold			1		V
V_{SS} Clamp Threshold			5		V
R_{SS} ON	V_{DD} = 7.5V	600	700	800	Ω
Shutdown Section (SD)					
SD Threshold		3.68	4	4.32	V
SD Discharge Current			0.63		µA
SD Charge Current			–6.3		µA
R_{SD} ON	V_{DD} = 7.5V	600	700	800	Ω
Current Sense Section (CS)					
CS Threshold	Pulse-by-Pulse	0.92	1	1.08	V
	Immediate	1.26	1.37	1.49	V
CS Input Bias	CS = 1.1V Pulsed			0.1	µA
CS to OUT Delay		50	75	100	ns
R_{CS} ON		600	700	800	Ω
Oscillator Section					
OUT Frequency		127.5	150	172.5	kHz
OUT Frequency Charge with Voltage	V_{DD} = 10V to 12V		0.1		%/V
OUT Minimum Duty Cycle			0		%
OUT Maximum Duty Cycle		63	70	70	%
Volt*Second Section (VS)					
VS Threshold		3.68	4	4.32	V
VS Input Bias				0.1	%/V
R_{VS} ON		600	700	800	Ω
Output Section (OUT)					
Output V_{SAT} Low	I_{OUT} = 100mA (dc) (Note 1)		0.7	1.0	V
Output V_{SAT} High (VDD-OUT)	I_{OUT} = –40mA (dc) (Note 2)		0.56	1.0	V
Output Low Voltage During UVLO	I_{OUT} = 20mA (dc), V_{DD} = 7.5V			1.5	V
Rise Time			30	60	ns
Fall Time	RT = 133.3k		15	30	ns
Bias Regulator Section (START)					
Bias Regulator	V_{DD} – START = 0.5V	11.6	11.8	12	V
VDD Override Voltage	V_{DD} – START = 1.0V	12.2	12.4	12.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these parameters apply for VDD = 12V, RT=56.3k, C_{VDD} = 1µF, C_{REF} = 0.1µF, C_{SS} = 0.01µF, R_{OUT} = 4Ω, C_{OUT} = 1nF and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Section (FB)					
FB-SS, Positive Differential Voltage	FB-SS Pulsed, FB = SS	2	2.5	7	V
FB-SS, Negative Differential Voltage	FB-SS Pulsed, FB = SS	–2	–2.5	–7	V
Input Bias Current	FB = 4.5V, SS = 0V			0.1	µA
FB Negative Compliance	I_{FB} = –100µA, SS = 0V	–6.8	–7.2	–7.6	V
Rising Edge FB-SS to OUT Delay	FB-SS Pulsed = 2V, FB = SS	50	75	100	ns
Falling Edge FB-SS to OUT Delay	FB-SS Pulsed = 2V, FB = SS	100	125	150	ns

Note 1: OUT Low, nominal of 0.7V reflects the 3Ω DMOS ON resistance plus 4Ω R_{SERIES}.

Note 2: OUT High (VDD-OUT), nominal of 0.56V reflects the 10Ω HVPMOS ON resistance plus 4Ω R_{SERIES}.

PIN DESCRIPTIONS

AGND: This pin is the reference point for grounding all analog functions and must be kept as clean as possible from all switching noise. It should be connected to PGND in only one location as close to the IC as practical.

CS: This is the pulse-by-pulse and shutdown over-current sense input pin. This Current Sense pin will trigger a pulse-by-pulse termination anytime a 1.0V threshold is exceeded while a signal in excess of 1.375V on this pin will initiate a complete shutdown. Each activation of pulse-by-pulse termination also sends a current pulse to the SD pin where an external capacitor can be used to provide a delayed shutdown. Since the CS pin can be noise sensitive, it is good practice to insert a small low-pass RC filter between this pin and the current sensor.

FB: This is the control input for the signal from a secondary-side PWM controller whose pulse-width command has been differentiated by the feedback pulse edge transformer into positive "start" and negative "stop" pulses. These signals are used to turn on and off the primary power switch and must have an amplitude of at least ±2.0V (4V peak-to-peak).

OUT: This is the drive pin for the MOSFET power switch and will both sink (1.5A) and source (0.75A) fast, high-current gate drive pulses. During shutdown, this pin is self-biased to an active low state. A minimum of 4Ω should be added in series with the output to ensure that the on chip driver safe operating area is not exceeded. (Data from the IRF820/830/840 family of MOSFETs, commonly available in the TO-220 package, is used to derive this value. The gate charge needed to provide full enhancement was used to establish an equivalent capacitance of up to 4000pF.)

OVS: This pin is used with an external resistor divider of V_{IN} to terminate operation if a voltage is sensed above the internal 4V threshold. Activation sets the Shutdown Latch which requires recycling the voltage on VDD to restart.

PGND: This is the power ground for the PWM output stage and conducts any current transients from the power switch gate drive. It should be closely bypassed to VDD and connected to AGND in only one location as close to the IC as possible.

RT: A resistor from this pin to AGND establishes a current, I_{SET} = 2V / RT, which is mirrored internally for several functions. It establishes the free-running startup switching frequency with an internal capacitor according to the relationship, fs = 8.0 x 10^9 / RT. The startup oscillator has a rise and fall time set to limit the duty-cycle of the power switch to a maximum of 70%, a limit which is maintained even after the feedback signal takes command.

REF: This is a 5V output usable with external loads of up to 10mA. This voltage is also the source for all internal analog threshold settings and should be bypassed with a minimum of 0.1µF capacitance to AGND.

SD: This pin is the input to the shutdown circuit. Like OVS, this pin also sets the Shutdown Latch when a threshold above 4V is exceeded. The primary intent of this input is to allow the use of an external capacitor to program a delay between the onset of current limiting and the issuance of a Shutdown command by integrating current pulses which appear on this pin with each activation of the CS input. This pin is pulled low with a current sink of 0.33/RT when there is no CS signal. The shutdown function can be disabled by connecting SD pin to AGND.

PIN DESCRIPTIONS

SS: The pin implements the primary side soft start function. This is the connection point for an external capacitor which determines the rate of increase in commanded pulse width for the power switch at startup. It also serves as the AC ground return for the feedback pulse transformer to provide a tracking bias for the FB input.

START: In conjunction with an external depletion-mode NFET, such as the Supertex DN2530, this pin can be used to develop a regulated 12V at VDD and thereby minimize or eliminate continuous current drain when starting from a variable high voltage source. If this function is unused, this pin can be left open.

UVS: This pin is used with an external resistor divider of Vin to terminate operation if a voltage is sensed below the internal 4V threshold. Activation maintains the circuit in shutdown with the soft-start capacitor clamped low.

VDD: This is the power input connection for all the control circuitry and, in addition, conducts all the gate charge current for the power FET. It should be closely bypassed with at least 1.0 uF to PGND and 0.1 uF to AGND. This pin is internally shunt regulated to clamp at 17.5V to protect the internal components so if a voltage source above this value is possible, external current limiting must be provided.

VS: This pin provides a volt-second clamp for the operation of the transformer-driving power switch with the aid of an external capacitor to ground and a high value resistor to the transformer's voltage source (Vin). With the initiation of each power pulse, the circuit will release an internal grounding clamp across the capacitor allowing it to charge with a current from the resistor proportional to the input voltage. If this pin reaches 4V prior to output termination from other control functions, then this will end the power pulse.

$$T_{VS} = 1.61 \bullet R_{VS} \bullet C_{VS},\ R_{VS} > 100\Omega$$

BLOCK DIAGRAM

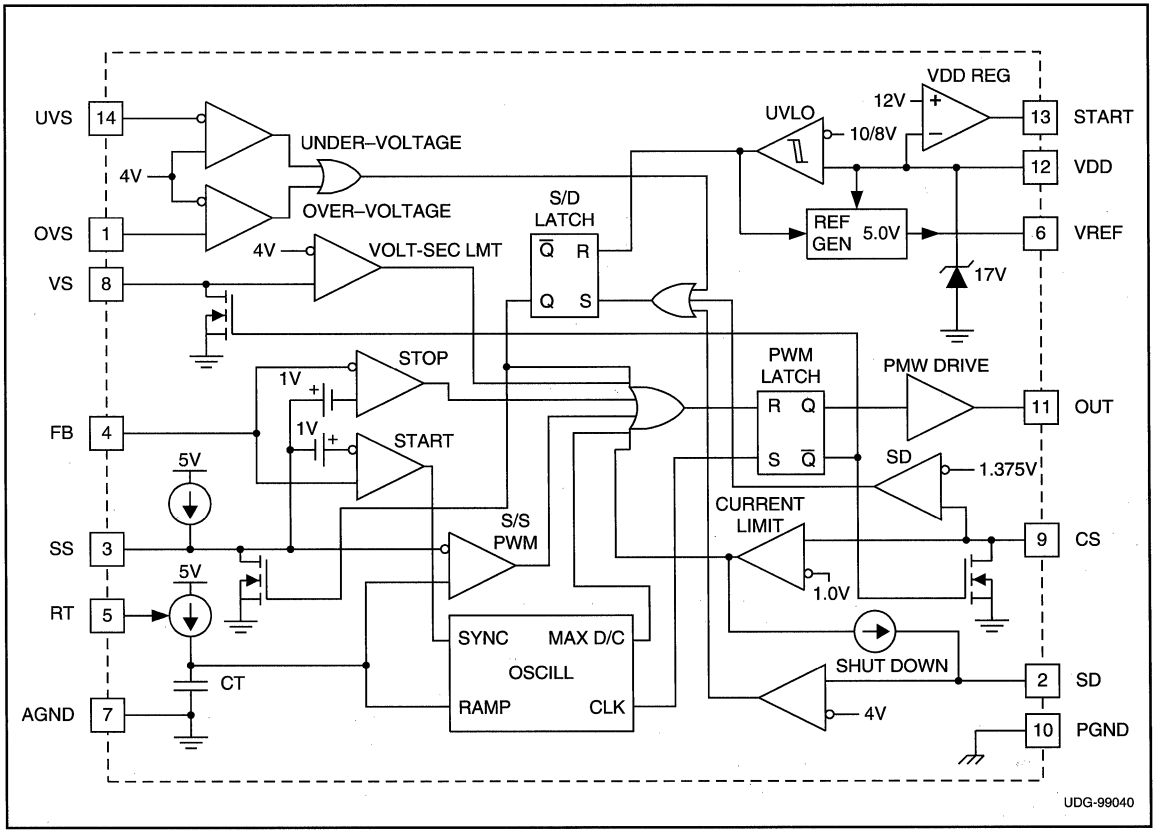


Figure 1. Block diagram.

CIRCUIT DESCRIPTION

Start-up Oscillator Section

The RT pin is connected to an internal 2.0V nominal, unity gain closed loop amplifier which is referenced to a voltage divider off the 5.0V reference. When a 22.22kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 90μA internal current is realized which charges the internal oscillator capacitor, approximately 58pF. I_{RT} = 90μA produces a maximum free running oscillator frequency of 360KHz at a 70% duty cycle. When a 133.33kΩ resistor is connected from the RT pin to GND an approximate I_{RT} = 15μA internal current is realized which produces a minimum free running oscillator frequency of 60KHz at a 70% duty cycle. The approximately 70% maximum duty cycle is setup by on chip MOSFET current mirrors which are not programmable.

Any frequency between these two limits (6:1 maximum to minimum frequency) is obtainable by linearly scaling the RT resistance between the minimum 22.22kΩ and maximum 133.33kΩ values. The secondary side PWM frequency should be fixed at (1 / 0.9) or 1.11 times the user programmed primary side free running oscillator frequency for proper primary side synchronization. Therefore, in all cases the recommended secondary side synchronization frequency shall be 1.11 times higher than the selected primary side free running start up frequency. Taking into consideration the two extreme limits for primary side free running start up frequency, the secondary side operating frequency should be set between 400kHz and 67kHz.

Soft Start Section

The Soft Start section contains all the circuitry required to produce a user programmable slowly increasing PWM duty cycle, starting from 0% to a maximum of 70%. The Soft Start cycle is triggered either by the initial primary side Start-up procedure or after any one of three user programmable fault conditions and one fixed fault condition. The PWM duty cycle increases according to the charge rate of an user selectable external Soft Start capacitor, connected from the SS pin to GND. The SS capacitor is charged by a nominal 6uA internal current source.

Voltage comparators referenced to a 4.0V threshold monitor the OVS pin, SD pin and the UVS pin and trigger a Soft Start cycle when a fault condition is detected on any of these pins. Should the CS pin rise in voltage above 1.375V a Soft Start cycle will also be triggered. The Soft Start cycle disables the output driver OUT and holds it in the low state until the capacitor connected from the SS pin to GND is discharged below 1.0V by an internal 6μA current sink. After this discharge period the PMW output OUT is enabled and the duty cycle is allowed to slowly increase as before.

Synchronization Section

The SS pin and the FB pin accepts the secondary side of a small signal synchronization transformer. A series blocking capacitor inserted in the primary side of the synchronization transformer is intended to differentiate the square wave gate drive output of the secondary side PWM controller while preventing the transformer from saturation. The SS capacitor also provides an AC GND at the SS pin or the synchronization transformer secondary. The small signal synchronization transformer provides galvanic isolation between primary and secondary side and must have adequate voltage breakdown rating between the primary and secondary windings.

Two comparators, with an approximate 1.0V offset each, are connected to the FB pin to provide plus and minus differential voltage comparison with a 2.0V deadband between the FB and SS pins. The 2.0V deadband prevents inductive backswing of the small signal transformer from giving false secondary side pulse edge detection.

Enough energy must be coupled into the comparator differential inputs to ensure reliable comparator switching. This requires sufficient voltage overdrive above the 1.0V comparator threshold and a specified transformer circuit time constant to provide a minimum synchronization pulse width.

On receiving the first recognizable negative going voltage pulse (turn-off command) generated from the falling edge of the differentiated square wave gate drive signal on the secondary side, the PWM latch is RESET and a synchronization latch is SET. After this event all primary side PMW driver output is slaved to the secondary side driver output in both frequency and duty cycle. The triggering of a Soft Start cycle by a fault condition will RESET the synchronization latch to again allow the internal Start-up oscillator to control the PWM latch.

PWM Section

The PWM section consists of a reset dominant SR latch with necessary logical gating on the SET input to allow control from the free running Start-up Oscillator until feedback from the secondary side PWM gate drive output is detected. After the occurrence of detectable feedback from the secondary side gate driver, the control of the primary side PWM latch is handed off to the secondary side PWM controller. A nine input OR gate on the PWM latch reset dominant input allows the numerous fault conditions to RESET the PWM latch and control from either the Start-up oscillator or feedback from the secondary side PWM output driver.

CIRCUIT DESCRIPTION (cont.)

UVLO & REF Sections

The under voltage lockout (UVLO) circuit will enable normal operation after VDD exceeds the 10.0V turn-on threshold and permits operation until VDD falls below the 8V turn-off threshold. While activated, the UVLO circuit holds the PWM gate driver output (OUT) and the internal reference buffer amplifier output REF low. To insure proper Soft Start and to prevent false SD detection, internal NMOS FET switches discharge external capacitors connected to the SS and SD pins during under voltage conditions.

The 5V internal reference is connected to the REF pin and must be bypassed using a good quality, high frequency capacitor. This 5V reference is not available externally while the chip is disabled by the under voltage lockout circuit.

CS and VS Section

The Current Sense (CS) circuit monitors the voltage across a ground referenced current sense resistor, connected between the source of the external power MOSFET and GND. The signal amplitude at the CS pin is compared to two, a 1.0V and a 1.375V, thresholds by two independent voltage comparators.

A voltage level greater than 1.0V, but less than 1.375V, will SET the reset dominant Shut Down latch and RESET the PWM latch. The SD latch is RESET by the Start-up oscillator arriving at it's 4.0V compare threshold. When the SD latch is SET a scaled current, I_{SD} = -(1/6)*(I_{RT}), charges an user selectable external capacitor connected between the SD pin and GND. When the SD latch is RESET a scaled current I_{SD} = (1/10)*(1/6)*(I_{RT}), discharges the user selectable capacitor connected between the SD pin and GND.

A current sense voltage greater than 1.375V will immediately trigger a SD event and also RESET the PWM latch. During the OFF period of the PWM latch any capacitance connected to the CS pin is discharged to GND potential by an internal 700Ω device.

The Volt*Second (VS) clamp circuit monitors the voltage at the VS pin produced by an external series RC circuit. The resistor is connected from the HV primary side power input, that is derived from the rectified line voltage, to the VS pin. The capacitor is from the VS pin to GND and being charged by the resistor during the ON time of the OUT driver. The resulting exponential voltage at the VS pin is monitored by a voltage comparator with a 4.0V threshold. Should the voltage at the VS pin exceed 4.0V, the PWM latch is RESET thus the output drive signal is terminated. This RC circuit can be tailored to prevent the power transformer from saturation by effectively limiting the applied maximum Volt*Second product across the primary winding. During the OFF period of the PWM output driver the VS capacitor is discharged to GND potential by an internal switch with 800Ω ON resistance.

START Regulator and VDD Clamp Sections

To facilitate the primary side Start-up a VDD = 12V voltage regulator may be implemented by using an external depletion mode FET. The gate of this device is than connected to the START pin, the Source terminal is attached to the VDD pin, and the Drain is tied to the HV primary side power input that is derived from the rectified line voltage. An auxiliary bootstrap winding off the main power transformer might be used to generate a bias voltage greater than 12V, which will effectively shutdown the 12V regulator and increase the efficiency of the biasing solution during normal operation.

To insure that the absolute maximum voltage ratings of internal devices are not violated, an internal shunt voltage regulator is provided to clamp the VDD pin at a nominal 17.5V maximum voltage. Similarly to other shunt or zener like voltage regulator circuits the current through the internal VDD clamp must be limited below the maximum current level indicated in the datasheet. In addition to limiting the current through the clamp circuit, the maximum power dissipation capability of the particular package used in the application has to be considered.

OUT Driver Section

An internal output driver OUT is provided to drive the gate of an external N-channel power MOSFET. The output driver consists of a nominal 4.0Ω ON resistance PMOS FET for turn-on, and a nominal 2.0Ω ON resistance DMOS FET utilized during the turn-off of the external MOSFET transistor. An external series gate resistance is specified to maintain an acceptable SOA (Safe Operating Area) for the DMOS device of the internal output driver. As discussed in the UVLO section before, the under voltage lockout (UVLO) circuit holds the PWM gate driver output low while UVLO conditions exists.

APPLICATION INFORMATION

The evaluation circuit of UCC3961 as the primary side startup circuit and UC3845 as the secondary side controller is shown in Fig. 2.

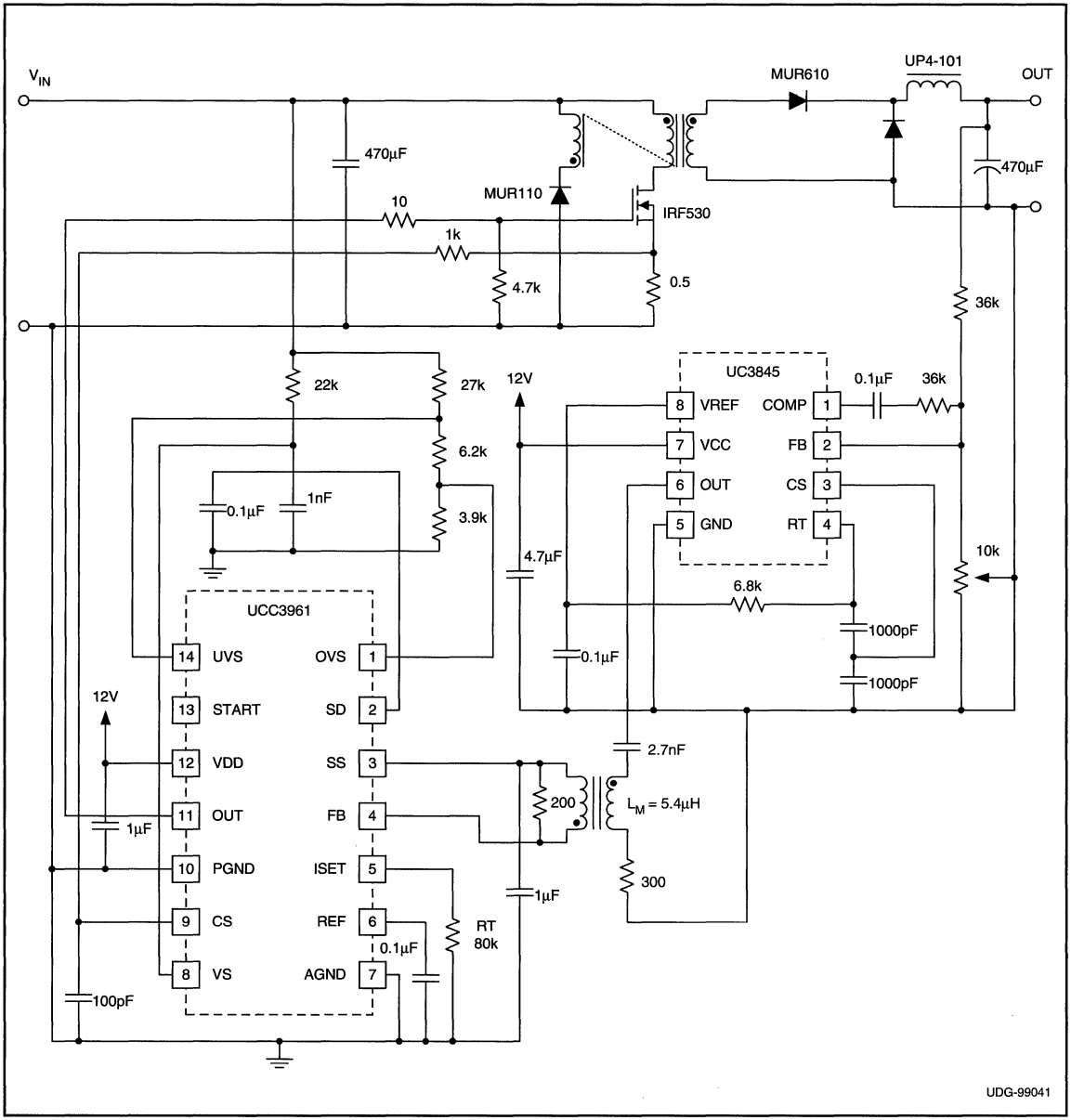


Figure 2. Evaluation circuit of UCC3961.

APPLICATION INFORMATION (cont.)

Pulse Edge Transmission Circuit

The UCC3961 uses a Pulse Edge Transmission (PET) circuit to transmit isolated gate pulse information from the secondary side controller. It is important for the PET circuit to have proper frequency response and adequately high damping (low Q factor) in order to prevent excessive overshoot. The circuit is shown below.

The pulse width measured at the FB pin must be between 25nsec wide and 200nsec wide, measured at 1 Volt above and at 1 Volt below the Soft Start voltage. The FB voltage must not be overdriven by more than 5V above or 5V below the Soft Start voltage. In order to prevent false triggering, the FB voltage must not ring pelloast the Soft Start voltage by more than ±0.9V. This can be met if the Pulse Edge Transmission circuit has a resonant frequency of 880kHz and a Q of 0.25. For further details, refer to Design Note DN-99, *Pulse Edge Transmission Circuit*. The following values will meet the specifications for a 12 Volt Secondary Gate Pulse signal, over the full range of UCC3961 operating frequencies.

T1 1:1 turns ratio, L_M=5.4µH, Feronics 11-622J, N1 = N2 = 4 turns

R1 300Ω

C1 2700pF

R2 200Ω

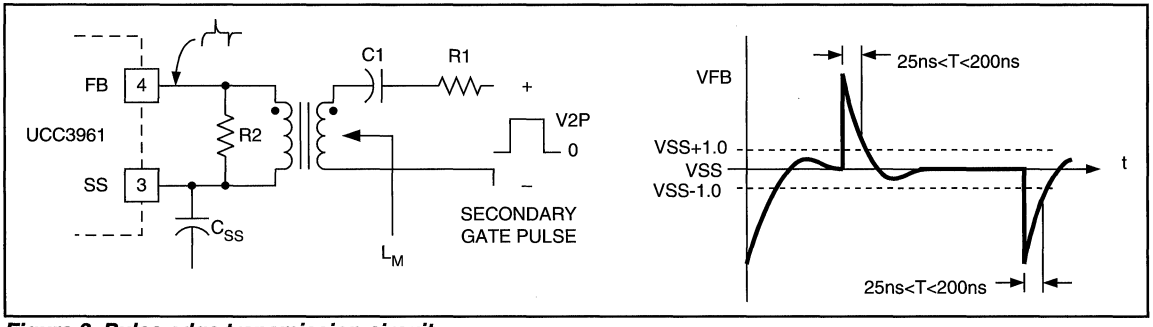


Figure 3. Pulse edge transmission circuit.

TYPICAL WAVEFORMS

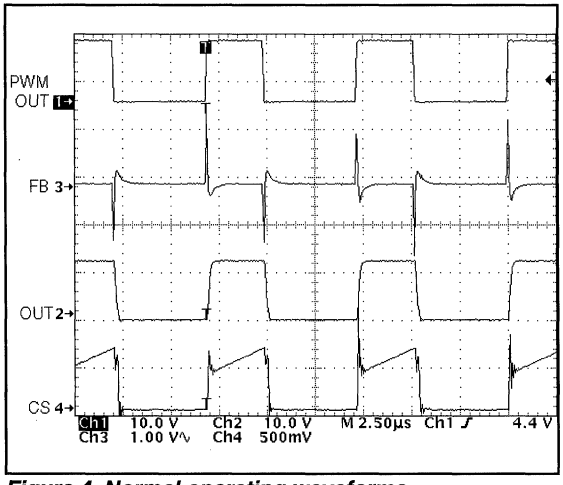


Figure 4. Normal operating waveforms.

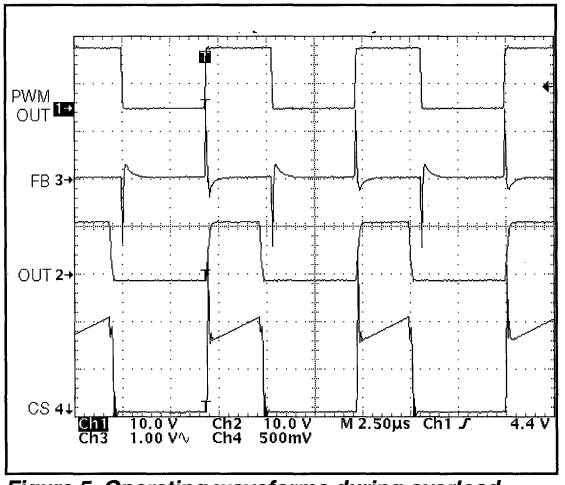


Figure 5. Operating waveforms during overload.

TYPICAL WAVEFORMS (cont.)

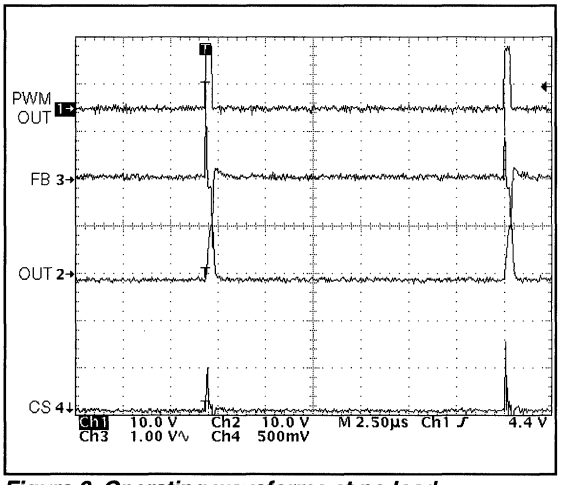


Figure 6. Operating waveforms at no load.

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UNITRODE

application INFO available

UC494A/AC
UC495A/AC

Advanced Regulating Pulse Width Modulators

FEATURES

- Dual Uncommitted 40V, 200mA Output Transistors
- 1% Accurate 5V Reference
- Dual Error Amplifiers
- Wide Range, Variable Deadtime
- Single-ended or Push-pull Operation
- Under-voltage Lockout With Hysteresis
- Double Pulse Protection
- Master or Slave Oscillator Operation
- UC495A: Internal 39V Zener Diode
- UC495A: Buffered Steering Control

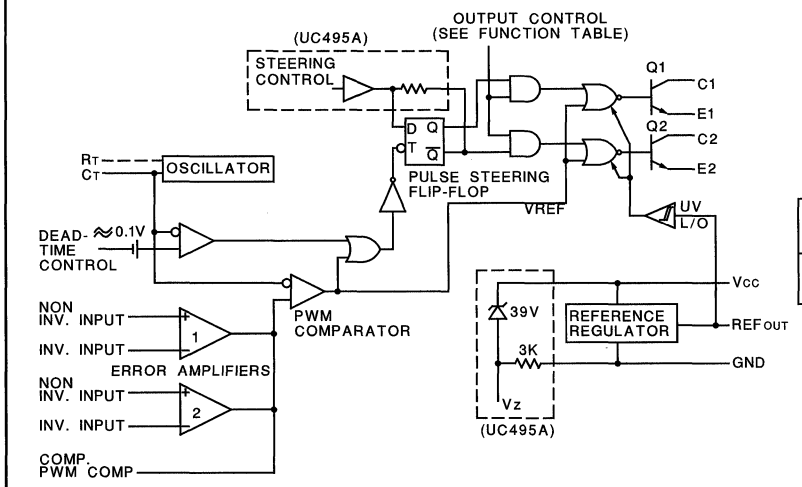
DESCRIPTION

This entire series of PWM modulators each provide a complete pulse width modulation system in a single monolithic integrated circuit. These devices include a 5V reference accurate to ±1%, two independent amplifiers usable for both voltage and current sensing, an externally synchronizable oscillator with its linear ramp generator, and two uncommitted transistor output switches. These two outputs may be operated either in parallel for single-ended operation or alternating for push-pull applications with an externally controlled dead-band. These units are internally protected against double-pulsing of a single output or from extraneous output signals when the input supply voltage is below minimum.

The UC495A contains an on-chip 39V zener diode for high-voltage applications where V_{CC} would be greater than 40V, and a buffered output steering control that overrides the internal control of the pulse steering flip-flop.

The UC494A is packaged in a 16-pin DIP, while the UC495A is packaged in an 18 pin DIP. The UC494A, UC495A are specified for operation over the full military temperature range of -55°C to +125°C, while the UC494AC, UC495AC are designed for industrial applications from 0°C to +70°C.

BLOCK DIAGRAM



FUNCTION TABLE	
Output Control Connected to:	Output Function
Ground	Single-Ended or Parallel Operation
V_{REF}	Push-Pull Alternating Outputs

UC495A

Steering Control (Output Control at V_{REF})	Output Function
V_S < 0.4V	PWM Output at Q1
V_S > 2.4V	PWM Output at Q2

ABSOLUTE MAXIMUM RATINGS (Note 1, 2, 3)

Supply Voltage, V_{CC} (Note 2) 45V
Amplifier Input Voltages . . . . . V_{CC} + 0.3V
Collector Output Voltage 41V
Collector Output Current 250mA
Continuous Total Dissipation 1000mW
@ (or below) 25°C free air temperature range (Note 3)
Storage Temperature Range . . . . . -65° to +150°C
Lead Temperature 1/16" (1.6mm) from case for 60 seconds,
J Package . . . . . 300°C
Lead Temperature 1/16" (1.6mm) from case for 10 seconds,
N Package . . . . . 260°C

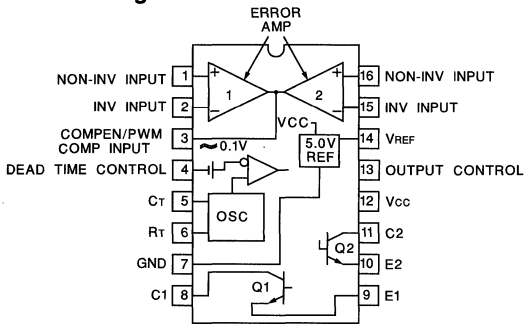
Note 1: Over operating free air temperature range unless otherwise noted.
Note 2: All voltage values are with respect to network ground terminal 3.
Note 3: Consult Packaging Section of Databook regarding thermal specifications and limitations of packages.

RECOMMENDED OPERATING CONDITIONS

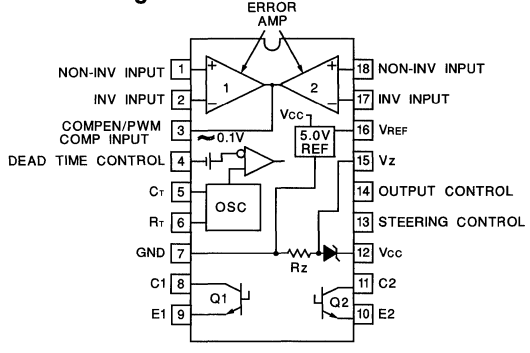
Supply Voltage V_{CC} . . . . . 7V to 40V
Error Amplifier Input Voltages . . . . . -0.3V to V_{CC}-2V
Collector Output Voltage 40V
Collector Output Current (each transistor) 200mA
Current into Feedback Terminal 0.3mA
Timing Capacitor, C_T . . . . . 0.47nF to 10,000nF
Timing Resistor, R_T . . . . . 1.8kΩ to 500kΩ
Oscillator Frequency . . . . . 1kHz to 300kHz
Operating Free Air Temperature
UC494A, UC495A . . . . . -55°C to +125°C
UC494AC, UC495AC . . . . . 0°C to +70°C

CONNECTION DIAGRAMS

DIL-18 (TOP VIEW) **UC494A/AC**
J or N Package



DIL-18 (TOP VIEW) **UC495A/AC**
J or N Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage V_{REF}	I_O = 1mA, T_A = 25°C	4.95	5	5.05	V
Input Regulation	V_{CC} = 7V to 40V		2	25	mV
Output Regulation	I_O = 1mA to 10mA		1	15	mV
Output Voltage Over Temperature	ΔT_A = Min. to Max.	4.90		5.10	V
Short Circuit Output Current	V_{REF} = 0, T_A = 25°C (Note 1)	10	35	50	mA
Oscillator Section					
Frequency (Note 2)	C_T = 0.01μF, R_T = 12kΩ		10		kHz
Standard Deviation Of Frequency (Note 3)	All Values of V_{CC}, C_T, R_T, T_A Constant		10		%
Frequency Change With Voltage	V_{CC} = 7V to 40V, T_A = 25°C		0.1		%
Frequency Change With Temperature	C_T = 0.01μF, R_T = 12kΩ, ΔT_A = Min. to Max.			2	%
Deadtime Control Section (Output Control Connected to V_{REF})					
Input Bias Current (Pin 4)	$V_{(PIN\ 4)}$ = 0V to 5.25V		-2	-10	μA
Maximum Duty-Cycle (Each Output)	$V_{(PIN\ 4)}$ = 0V	45			%

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, over recommended operating free-air temperature range, V_{CC} = 15V, f = 10kHz, $T_A = T_J$.

PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNITS
Deadtime Control Section (cont.) (Output Control Connected to V_{REF})						
Input Threshold Voltage (Pin 4)	Zero Duty-Cycle			3	3.3	V
	Maximum Duty-Cycle		0			V
Amplifier Section						
Input Offset Voltage	$V_{O\ (PIN\ 3)}$ = 2.5V			2	10	mV
Input Offset Current	$V_{O\ (PIN\ 3)}$ = 2.5V			25	250	nA
Input Bias Current	$V_{O\ (PIN\ 3)}$ = 2.5V			-0.2	-1	µA
Common-Mode Input Voltage Range	V_{CC} = 7V to 40V		.03 to V_{CC} -2			V
Open Loop Voltage Gain	ΔV_O = 3V, V_O = 0.5V to 3.5 V		70	95		dB
Unity Gain Bandwidth				800		kHz
Common-Mode Rejection Ratio	V_{CC} = 40V, T_A = 25°C		65	80		dB
Output Sink Current (Pin 3)	V_{ID} = -15mV to -5V, $V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Output Source Current (Pin 3)	V_{ID} = 15mV to 5V, $V_{(PIN\ 3)}$ = 3.5V		-2			mA
Output Section						
Collector Off-State Current	V_{CE} = 40V, V_{CC} = 40V			2	100	µA
Emitter Off-State Current	V_{CC} = V_C = 40V, V_E = 0				-100	µA
Collector - Emitter Saturation Voltage — Common-Emitter	V_E = 0, I_C = 200mA			1.1	1.3	V
Collector - Emitter Saturation Voltage — Emitter-Follower	V_C = 15V, I_E = -200mA			1.5	2.5	V
Output Control Input Current	V_I = V_{REF}				3.5	mA
PWM Comparator Section						
Input Threshold Voltage (Pin 3)	Zero Duty-Cycle			4	4.5	V
Input Sink Current (Pin 3)	$V_{(PIN\ 3)}$ = 0.7V		0.3	0.7		mA
Steering Control (UC495A, See Function Table)						
Input Current	$V_{(PIN\ 13)}$ = 0.4V, Q_1 ACTIVE				-200	µA
	$V_{(PIN\ 13)}$ = 2.4V, Q_2 ACTIVE				300	µA
Deadband				500		mV
Zener Diode Circuit (UC495A)						
Breakdown Voltage	V_{CC} = 45V, I_Z = 2mA		36	39	45	V
Sink Current	$V_{(PIN\ 15)}$ = 1V		0.2	0.3	0.6	mA
Total Device						
Standby Supply Current	Pin 6 at V_{REF}, All other inputs and outputs open	V_{CC} = 15V		6	10	mA
		V_{CC} = 40V		9	15	mA
Under Voltage Lockout			3.5		6.5	V
Hysteresis				300		mV
Switching Characteristics (T_A = 25°C)						
Output Voltage Rise Time	Common-Emitter Configuration			100	200	ns
Output Voltage Fall Time	R_L = 68Ω, C_L = 15pF			25	100	ns
Output Voltage Rise Time	Emitter-Follower Configuration			100	200	ns
Output Voltage Fall Time	R_L = 68Ω, C_L=15pF			40	100	ns

Note 1: Duration of the short circuit should not exceed one second.

Note 2: Frequency for other values of C_T and R_T is approximately $f = \frac{1.1}{R_T \bullet C_T}$

Note 3: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula: $\sigma = \sqrt{\frac{\sum_{n=1}^{n} (X_n - X)^2}{n-1}}$

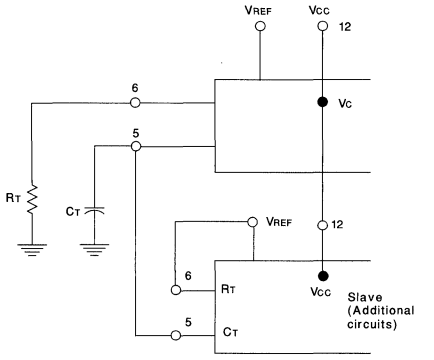


Figure 1. Slaving two or more control circuits.

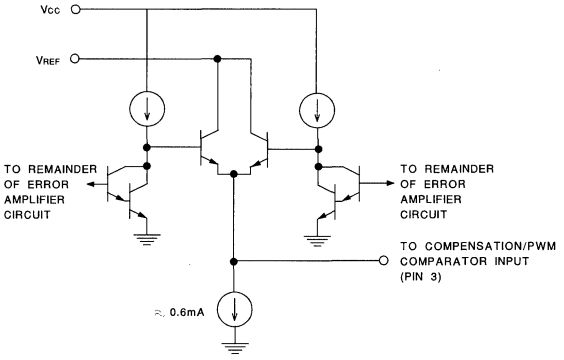
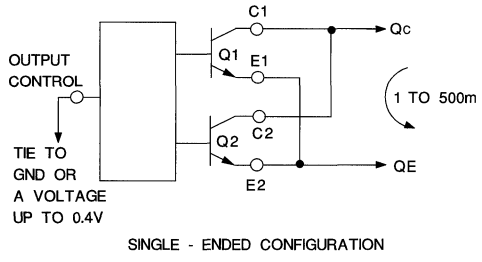


Figure 2. Output circuit of error amplifiers.



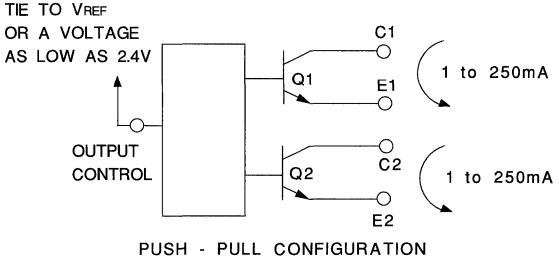


Figure 3. Output connections for single-ended and push-pull configurations.

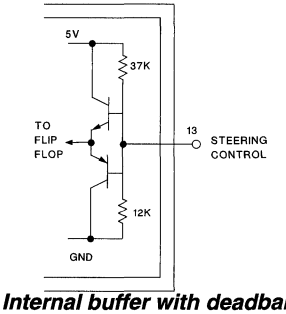


Figure 4. Internal buffer with deadband for steering control on UC495A.

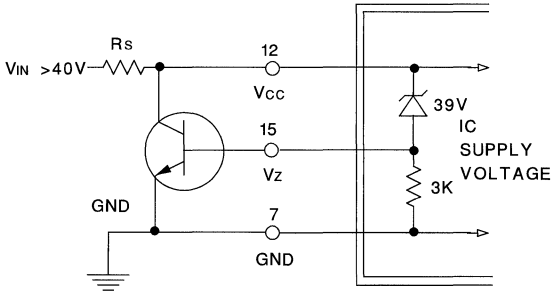


Figure 5. Operation with V_{IN} > 40V using internal zener.

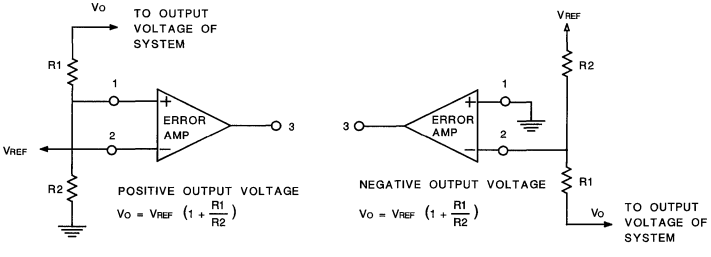


Figure 6. Error amplifier sensing techniques.

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UNITRODE
Design Note

UC3842A
LOW COST START-UP AND FAULT PROTECTION CIRCUIT

This circuit optimizes control circuit performance to include:

- **Low Start-up Current, Less Than 0.5 ma**
- **MOSFET Compatible Undervoltage Lockout Thresholds 16V Turn-on, 10V Turn-off**
- **Programmable Restart Delay HICCUP Fault Protection**
- **Auxiliary 5V Precision Reference**
- **Overvoltage/Overtemperature Protection**

CIRCUIT DESCRIPTION AND OPERATION:

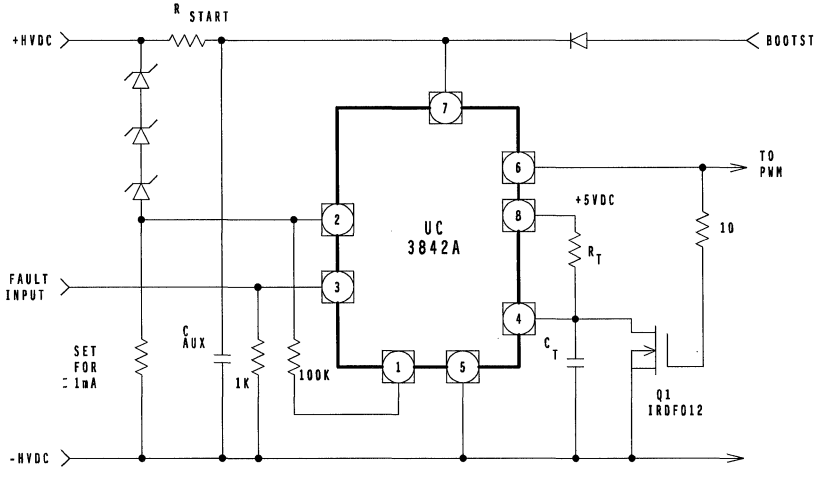
The UC3842A Controller is featured in this design ***NOT*** as the power supply control IC, but in a supervisory function to assist the principal PWM. It will be utilized to facilitate a low current start-up of less than 0.5 milliamp from the high voltage bulk supply. Additionally, the UC3842A features 16 volt turn-on and 10 volt turn-off thresholds, ideally suited for power mosfet gate drive circuits. The 1 amp output of the UC3842A is used to switch the auxiliary supply voltage to the principal PWM controller, a UC3825 or UC3846 for example.

The oscillator of the UC3842A is configured to generate a constant off time, corresponding to the desired restart delay interval. At the beginning of its operation, the UV initiates a clock cycle and the PWM output at pin 6 goes high. This is fed to transistor Q_1 which pulls the R_t/C_t input at pin 4 low, thus "freezing" the oscillator, while keeping the PWM output high. Once a valid fault (greater than 1 volt) is received at the current sense input (pin 3), the output at pin 6 will go low. Transistor Q_1 is then turned off, and the oscillator generates an off period, or delay as programmed by the R_t/C_t components. This procedure will repeat as often as dictated by the fault conditions, but significantly reduces the average short circuit currents and power dissipation.

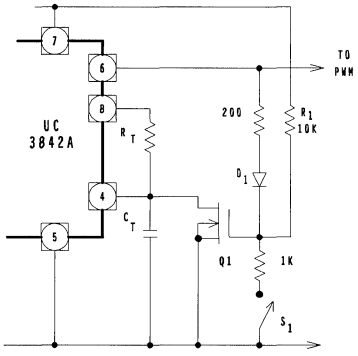
The UC3842A's current sense node is used as the fault input, and can be configured to provide numerous safeguards. Primary overvoltage protection is accomplished by using a simple resistor divider network or series string of zener diodes to the high voltage rail. Overtemperature protection is possible by including the UC3730 Precision Thermal Monitor IC, or a variable impedance thermistor. In a simple configuration, the fault circuit is designed to deliver a 1 volt input to pin 3 of the UC3842A when a fault response is necessary. The error amplifier can also be biased to accept lower amplitudes of valid fault inputs at the current sense input. A precision five volt auxiliary supply is made available at the IC's reference output, pin 8 and can supply 20 milliamps maximum.

UC3842A Supervisory Function Circuits

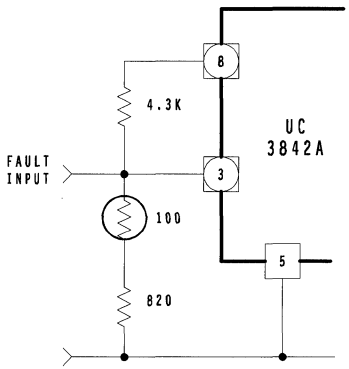
LOW COST START-UP and FAULT PROTECTION CIRCUIT



COMBINED LATCH/RESET/HICCUP FUNCTIONS
General Circuit



OVER-TEMPERATURE PROTECTION
using 50 to 100Ω thermocouples



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UNITRODE
Design Note

UC1842/UC1842A FAMILY
SUMMARY OF FUNCTIONAL DIFFERENCES

The industry standard series of UC1842/43/44/45 devices has been improved for higher frequency, off-line power supplies. This new "A" series of controllers, UC1842A/43A/44A/45A, feature three major advantages over their predecessors as shown in the summary below.

Start Up Current

	UC1842/45	UC1842A/45A
Typical (T_J = 25°C)	0.5ma	0.3ma
Maximum (T_J = 25°C)	1.0ma	0.5ma

Oscillator Discharge Current

	UC1842/45			**UC1842A/45A**		
	MIN	TYP	MAX	MIN	TYP	MAX
At T_J = 25°C (mA)	7	10	13	7.8	8.3	8.8
Overtemp. Range	6	—	14	7.5	—	8.8

Output Saturation

	UC1842/45	UC1842/45A
During UVLO	1V @ 0.2ma	1V @ 10ma

The reduced start-up current is of particular concern in offline supplies where the IC is "powered-up" from the high voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Lowering this by 50% in the "A" version family will reduce the resistors power loss by the same percentage.

Precision operation at high frequencies with an accurate maximum duty cycle can now be obtained with the "A" family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or deadtime.

Another significant improvement has been made in the output section, specifically to the lower totem-pole transistor's operation during undervoltage lockout. The "A" series of devices prevent the power MOSFETs from parasitically turning-on at powerup due to the "Miller" effect. This new technique allows the IC to sink higher currents at lower saturation voltages than it's predecessors.

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UC3840/UC3841/UC3851 PWM CONTROLLERS SUMMARY OF FUNCTIONS AND DIFFERENCES

The UC3840/UC3841 and UC3851 PWM controllers incorporate numerous protection features for switch mode power supplies. The list includes programmable undervoltage lockout thresholds, programmable current limit thresholds, overvoltage protection, soft-start and external stop/reset capability. While these controllers are similar in concept, there are subtle differences amongst them in the operation of the error latch circuitry, specifically, the external stop and reset inputs. The UC3841 and UC3851 ICs feature an improved circuit design which simplifies the interface to the internal protection circuitry. A summary of the functions and modes of operation is listed below.

EXTERNAL STOP

	UC3840	UC3841/51
Low (<0.8V)	Stop	Defeat E/L Operation
High	Normal	Stop
Open	Normal	Normal
Cap. to GND During Power-up	Not Recommended	Delay E/L Operation at ≈ 13msec/μF

E/L= Error Latch

RESET

	UC3840	UC3841/51
High (>3.2V)	Latch	Latch
Low (<2.8V)	Requires UV Cycle to Reset	Reset

SOFT START

	UC3840	UC3841/51
After UV or Reset	Unlatched	Latched ($V_{SS} \leq 0.40V$)

The UC3851 controller incorporates two additional features, a toggle flip-flop for an accurate 50% maximum duty cycle clamp, and a 1 amp peak totem-pole output for driving power MOSFETs. Maximum duty cycles and output configurations for each device is shown below.

MAXIMUM DUTY CYCLE (T_J = 25°C)

	UC3840/41	UC3851
R_T = 20k, C_T = 1nF	0-95%	0-46%

PWM OUTPUT

	UC3840/41	UC3851
1A (PK)	Open Collector Active Low	Totem Pole Active High

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UC3842A FAMILY
FREQUENCY FOLDBACK TECHNIQUE PROVIDES PROTECTION

Excessive power dissipation in switching devices can occur during start-up and overload conditions in many switchmode power supplies. Many sophisticated PWM controllers provide the means for protection against these conditions; however, simple low-cost controllers will require additional circuitry. The circuit described below utilizes only one additional resistor and transistor to enhance the performance of the UC3842A family of controllers.

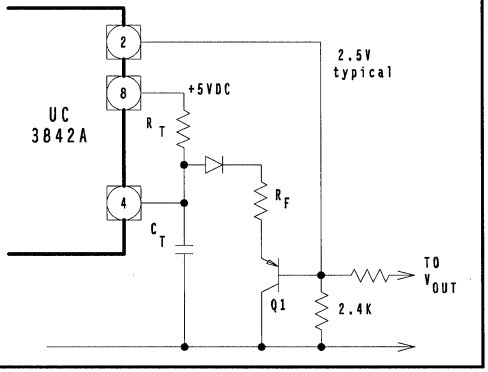
The power supply output voltage is fed to the error amplifier inverting input (pin 2) at a 2.5 volt amplitude under normal operating conditions. During start-up or overload, however, this voltage can drop to zero. The circuit shown uses this feedback voltage to divert normal charging current from the IC's timing capacitor to ground whenever the feedback voltage is below the 2.5 volt nominal. A linear three-to-one reduction of oscillator frequency is obtainable for most applications. This technique lengthens the potential maximum on-time and reduces the programmed deadtime. In many circuits, however, the peak current limit threshold is reached early in the cycle under these overload conditions, and this is not a problem. For most applications, the foldback resistor value (R_F) should equal that of the timing resistor (R_T).

EXAMPLE:

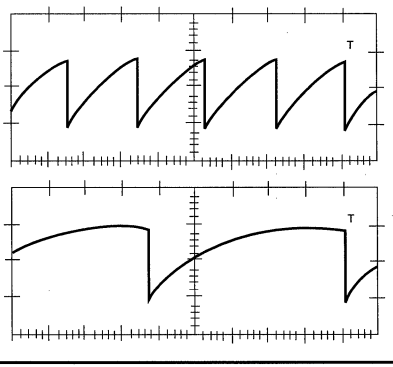
100 kHz operation, R_T = 15k, C_T = 1 nF, R_F = 15k, Q_1 = 2N2907A

OPERATING MODE	NORMAL	OVERLOAD
$V_{E/A}$ - (pin 2)	2.50V	0.00V
Oscillator Freq.	105 kHz	36 kHz

FREQUENCY FOLDBACK TECHNIQUE CIRCUIT



OSCILLATOR FREQUENCY



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PROGRAMMABLE ELECTRONIC CIRCUIT BREAKER

The design of a programmable electronic circuit breaker is shown below which utilizes the UC3843A control IC to facilitate a high speed turn-off following an overcurrent condition. This low cost, industry standard IC contains the required protection features and drive capability in a single 8 pin device.

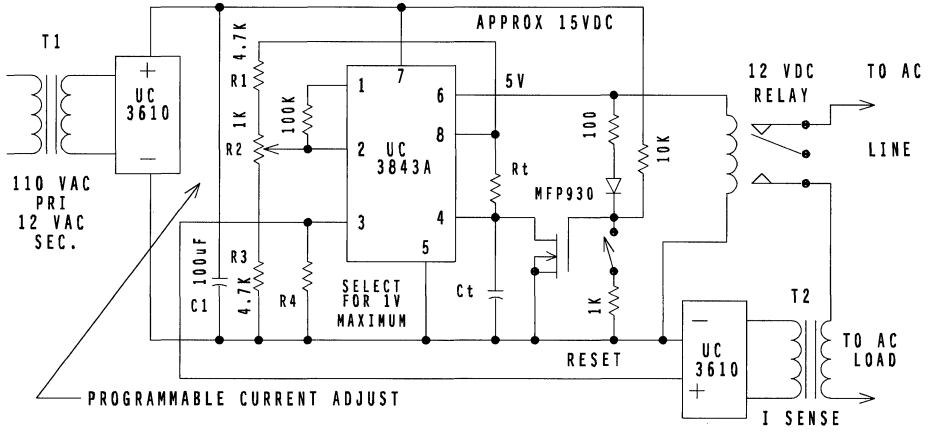
CIRCUIT OPERATION

Power to the controller is provided by a simple, low cost 60Hz transformer from the AC line which delivers 12 VAC at the secondary. The output current is determined primarily by the relay used with an additional 10 milliamps, or so, drawn by the IC. Undervoltage lockout prevents any operation until 10 VDC is obtained across capacitor C1, when the UC3843A will turn on. The PWM output at pin 6 goes high which drives the relay ON and switches the load across its respective power source. The load current is sensed by the current transformer T2, multiplied by its turns ration(N) and develops a voltage across the sense resistor R4. This resistor is scaled to delivery 1 volt maximum at the full load current and is one input to the PWM comparator.

While the output at pin six is high transistor Q1 is also turned ON which disables the ICs oscillator, locking the output high until toggles by the PWM. A 10k resistor (R5) to the supply voltage (pin 7) supplies bias to Q1 after the output has gone low, providing a latched OFF condition. This can easily be reset by pulling Q1's gate low through 1k ohms to ground as shown.

SCHEMATIC DIAGRAM

ELECTRONIC CIRCUIT BREAKER FEATURES HIGH SPEED CURRENT LIMITING



The other input to the PWM comparator is represented by the voltage at pin 1, the error amplifier output which can be adjusted by resistor R2. Internally, this voltage is reduced by two diode drops then attenuated to one-third its amplitude. The PWM circuitry compares this voltage with that of the current sense input at pin 3. When the current sense input exceeds the threshold set by resistor R2, the comparator is tripped and the ouptput at pin 6 is latched OFF.

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UC1525B/UC1527B DEVICES

Comparison Summary to UC1525A/27A Devices

The UC1525B and UC1527B devices are enhanced versions of the previous generation of UC1525A and UC1527A devices. They are pin-for-pin compatible and direct replacements for the "A" versions in almost all applications. Significnt improvements have been made in the 5.1 V reference voltage and the output drivers as itemized in the tables below.

PARAMETER	NEW: UC1515B/27B	OLD: UC1525A/27A
REFERENCE VOLTAGE		
V_{REF} (min)	5.062 V	5.05 v
V_{REF} (max)	5.138 V	5.15 v
Line Regulation (max)	+/- 10 mV	+/-20 mV
Load Regulation (max)	+/-15 mV	+/-50 mV
Temperature Stability (max)	+/-30 mV	+/-50 mV
Total Output Variation (max)	5.036 V to 5.164 V	5.00 V to 5.20V
Long Term Stability (max)	+/-10 mV	+/-50 mV
Temperature Coefficient (typ)	8 ppm/deg. C	
PWM OUTPUT SECTION		
Minimum On-Time (typ)	350 nS	600 nS
Cross Conduction	30 nC	150 nC
SUPPLY CURRENT		
ICC Increase (40 kHz to 400 kHz)	15 mA (max)	40 mA (typ)
ESD PROTECTION		
Discharge Withstand Voltage (typ)	2 kV (typ all pins)	no protection

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UNIQUE "CHEAP AND DIRTY" CONVERTER FOR LOW POWER BIAS SUPPLIES

Bill Andreycak

Regulated output voltage is obtained - regardless of input voltage

Most power supply designs use PWM controller ICs and MOSFET switches which require 10 to 15 volt bias supplies for proper operation. A common application problem is to first generate an auxiliary supply within this range. Although simple in many applications, developing this supply with a variable low voltage input can be challenging especially when the input amplitude goes both below and above the desired output voltage. The circuit shown below is a unique, inexpensive solution to this problem.

Basically, the topology is a two transistor flyback (buck-boost) converter which provides a noninverting output polarity. By varying the duty cycle, the output voltage can be either higher or lower than the input amplitude. This attribute makes this approach ideally suited for many widerange input or automotive applications. Likewise, this technique is equally applicable to power factor correction applications. Additionally, the inductor can be operated in either the continuous or discontinuous current modes.

BUCK-BOOST CONVERTER (2 XTOR)

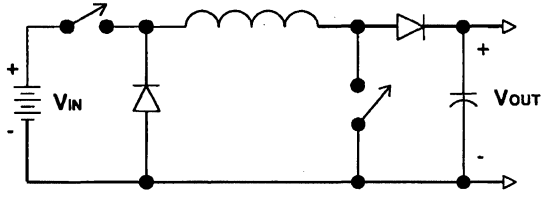

Figure 1.

Implementation of this technique will require a "high side" switch connected to the input voltage (VIN) and a low side switch to ground. Both of these are activated together, placing the inductor across the input supply while the switches are on. At turn off, the inductor is placed across the output capacitor and the two diodes conduct until the current reaches zero (discontinuous mode) or the next switching cycle is initiated (continuous mode). Inductor voltage and current waveforms are shown at maximum duty cycle for clarity.

INDUCTOR VOLTAGE AND CURRENT

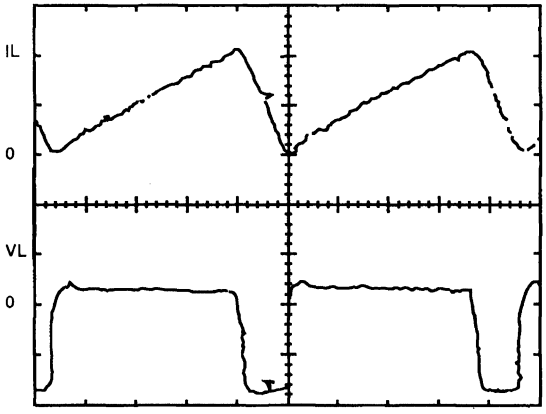

Figure 2.

At first, most PWM controllers may seem to be likely candidates for implementation of this technique. However, only one PWM features the ability to simultaneously switch both outputs together. The UC494A provides this operational mode by grounding its output control (O/C) input. Also limiting the IC selection is the fact that one IC output must go high and the other low each cycle. This is accomplished by connecting each of the UC494A's output collectors and emitters as required.

Switching at 200kHz in this application, the UC494A is programmed by a 9.1 K timing resistor (RT) and 470 pF capacitor (CT). High frequency conversion facilitates the use of a small (surface mount) inductor and output storage capacitor. Output voltage is regulated by using the ICs "A" amplifier as the voltage error amplifier. The 15 volt output is divided

down to 5 volts across the 15 K ohm resistor at pin 1 and compared to the reference voltage at pin 14. The 30K ohm resistor to Vout can be changed to provide different output voltages if required. Amplifier "B" is not used, but can be configured to provide overcurrent or overvoltage protection if desired. Schottky (1N5820) diodes are used in the power stage to maximize efficiency. Standard silicon diodes can be substituted in cost sensitive applications with some performance degradation. Efficiency for the 400 mW converter shown in figure 3 is approximately 50% for inputs between 7 and 16 volts and decreases slightly at higher and lower inputs. Consult Unitrode Design Note DN-37 for further information about 5 volt PWM operation.

BUCK BOOST CONVERTER USING THE UC 494A PWM CONTROLLER

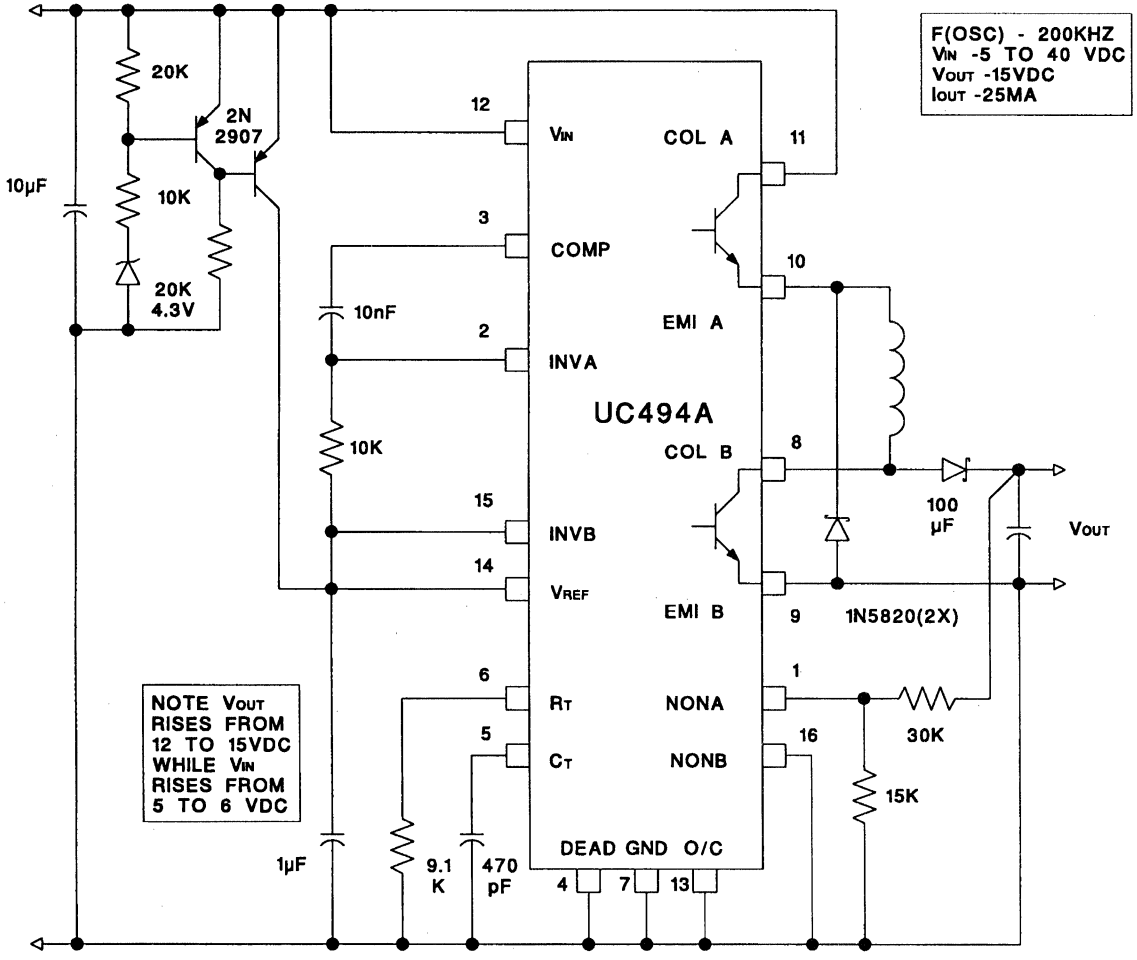

Figure 3.

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THE EFFECTS OF OSCILLATOR DISCHARGE CURRENT VARIATIONS ON MAXIMUM DUTY CYCLE AND FREQUENCY IN UC3842 AND UC3842–"A" PWM ICs

by YEAM CHONG HOCK

Many designers try to program a precise maximum duty cycle and operating frequency by careful selection of the oscillator timing components, Rt and Ct. Because of the variations in oscillator discharge current, very accurate programming is not easily obtainable. However, it is possible with ICs which contain a "trimmed" discharge current which has specified limits. This Design Note will detail programming frequency and maximum duty cycle with both types of oscillators. Simplified equations will be used to develop obtainable ranges for these parameters over IC tolerances.

ON-TIME

Maximum on-time directly corresponds to the maximum charging time of the timing capacitor. Charging time (TC) is determined by the timing capacitor value (Ct), the charging current (IRt) and the voltage amplitude between the upper and lower oscillator thresholds.

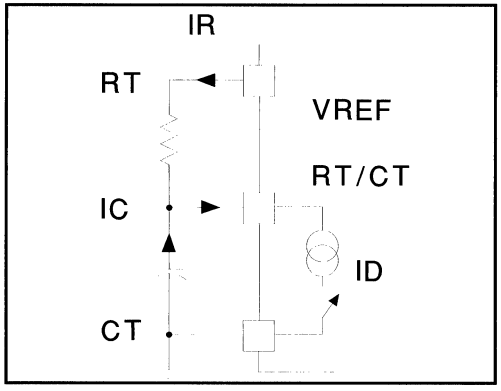

Figure 1: Basic UC3842 Oscillator Circuit

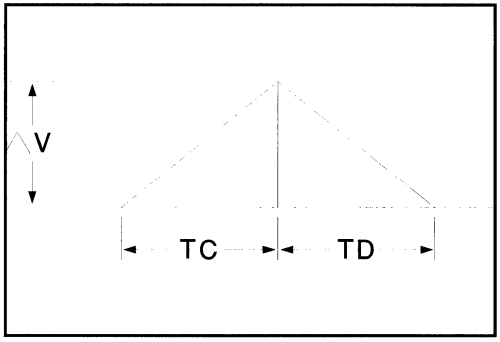

Figure 2: Timing Waveforms and Design Equations

OFF-TIME (DEADTIME)

The off-time occurs while the timing capacitor is discharged from the oscillator upper threshold to its lower threshold. The discharge current actually sinks two currents to ground. One current is flowing from the discharging timing capacitor. Another current flows from the timing resistor (Rt) pulling to Vref. Therefore, the effective timing capacitor discharge current (ICt) is the ICs discharge current (Id) minus the timing resistor charging current (IRt). Maximum duty cycle and switching frequency can

be controlled by accurately setting the ratio of these currents and capacitor value. The related equations are listed below.

CHARGING:

$$ICt = C \times \frac{dV}{Tc} ICt = C \times dV / Tc$$

$$ICt = \frac{5V}{Rt} (approximation)$$

$$TC = c \times \frac{dV}{IRt}$$

DISCHARGING:

$$ICt = Id - IRt$$

$$Td = c \times \frac{dv}{(IRt - Id)}$$

$$Td = \frac{(Id - IRt)}{Id}$$

DUTY CYCLE:

$$D = \frac{Tc}{(Tc + Td)}$$

$$D = \frac{(Id - Rt)}{Id}$$

SWITCHING FREQUENCY:

$$F = \frac{1}{Tper} = \frac{1}{(Tc + Td)}$$

$$F = \frac{(Id - IRt)}{(Id \times Tc)}$$

EXAMPLE 1:

This example will calculate the potential variations in maximum duty cycle and frequency using a standard UC3842 device. A ten milliamp internal discharge current (Id = 10mA) will be used for initial programming. The worst case limits of 6 and 14 milliamp discharge currents will be used to analyze the possible variations. A target of 100kHz at 60% duty cycle will be used.

$Id = 10mA (typical)$

$Id(\min) = 6mA, Id(\max) = 14mA$

$F(typ) = 100kHz$

$D = 0.60 (60\%)$

Based on the 10mA discharging current and the equations previously mentioned;

$IRt = 4mA$, and $Tc = 6us$

Using the same Rt and Ct values with a discharge current of 6mA results in:

$Dmax = 0.33 (30\%)$

$F = 55kHz$

When the highest discharge current of 14mA is used, the results are:

$Dmax = 0.71 (71\%)$

$F = 118kHz$

Therefore, the total possible range due to discharge current variations in maximum duty cycle and frequency is:

$Dmax = 33\ 71\ percent$

$Frequency = 55\ 118kHz$

In most applications this range is far too wide to use in a high volume production environment. One technique to minimize the effects of the discharge current is to have the ICs sorted into different groups. Each group can have a tight distribution or tolerance and will use a specific timing resistor and capacitor to achieve the desired frequency and duty cycle. Each other group will also need a specific Rt and Ct for that group. Keeping these groups separated can create problems in some production situations. One alternative is to have the ICs measured and "binned" at the factory. Another way is to use only ICs within one distribution group, for example, 10mA +/- 1mA. Listed below is a general procedure to follow with grouped parts.

1. Sort ICs by discharge current range
ex: 7mA +/- 1mA (6-8mA total)

2. Select Rt and Ct using previous equations and worst case conditions.

Table 1 shows the results of selecting ICs by discharge current. The oscillator was programmed not to exceed 100kHz and 60% maximum duty cycle.

I Discharge (+/- 1mA)	Rt (k)	Ct (nF)	Minimum Duty%	Maximum Duty%	Minimum Freq (kHz)	Maximum Freq (kHz)
7mA	1.56	11.3	47	60	77.8	100
9mA	1.25	14.1	50	60	83.3	100
11mA	1.04	16.9	52	60	86.7	100

TRIMMED DISCHARGE CURRENT:

Very repeatable and predictable high volume production can be rescued from these variations by using the right IC, one with a trimmed discharge current. The UC3842A, UC3843A, UC3844A and UC3845A devices have an internal factory trimmed discharge current with a tight distribution. This is set at 8.3mA typically, and can only vary between a low of 7.5mA and a high of 8.8mA. Programming these ICs for a 50% maximum duty cycle and 100kHz switching frequency will result in worst case variations of:

$D(\min) = 56\%$

$D(\max) = 62\%$

$F(\min) = 92.9kHz$

$F(\max) = 103.8kHz$

This is a significant improvement over the non "A: version devices. The accuracy of these ICs will improve when these ICs are used at wider maximum duty cycles, for example 65 to 85 percent. The UC3844A and UC3845A are intended for 50% maximum duty cycle applications and contain a flip flop to insure that 50% D(max) is never exceeded. The UC3842A and UC3843A have maximum duty cycles near 100% and can be adjusted lower using the appropriate Rt and Ct components.

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DESIGN CONSIDERATIONS FOR TRANSITIONING FROM UC3842 TO THE NEW UCC3802 FAMILY

John Gaumont

In an attempt to stay abreast of trends in the power supply marketplace, the Power Supply Design Engineer is perpetually seeking methods of improving upon existing designs. Requirements such as lower power for battery operated equipment, higher switching frequencies for reduced magnetics size, higher levels of circuit integration for improved reliability and lower cost have become necessities for survival.

The UCC3802 offers numerous advantages which allow the Power Supply Design Engineer to meet these challenging requirements. Features include:

- BI-CMOS Process
- Low Starting Supply Current: typically 100µA
- Low Operating Supply Current: typically 500µA
- Pin out Compatible with UC3842 and UC3842A families
- 5 Volt Operation (UCC3803, UCC3805)
- Leading Edge Blanking of Current Sense Signal
- On-Chip Soft Start
- Internal Full Cycle Restart Delay
- 1% Voltage Reference
- Up to 1 MHz Oscillator
- Self-Biasing Output Low During UVLO
- Very Few External Components Required
- 70ns Response from Current Sense to Output
- Available in Surface Mount or DIP Package

The UCC3802 family of devices are pin out compatible with the UC3842 and UC3842A families however, they are **NOT PLUG-IN COMPATIBLE**. In general, the UCC3802 requires fewer external components and consumes less operating current. The following UCC3802 family attributes should be considered **BEFORE** inserting the device into a UC3842/42A family socket:

1. Maximum supply voltage
2. Turn-on and Turn-off thresholds
3. Oscillator Rt, Ct values
4. Schottky diodes may not be required on output
5. No current sense filter required
6. No soft start circuitry required
7. Auxiliary power (bootstrap winding) may not be required

Detailed Pin By Pin Description

PIN 1 COMP--The UCC3802 has a true low output impedance error amplifier which both sources and sinks current. The error amplifier associated with the UC3842 family is an open collector in parallel with a current source. The UCC3802 has power-up soft start and fault soft start built on-chip with a fixed COMP rise time to 5V in 5ms. Therefore, **NO EXTERNAL SOFT START CIRCUITRY IS REQUIRED** saving 1 resistor, 1 capacitor, and 1 PNP transistor.

PIN 2 FB--The UCC3802 features a 2 MHz bandwidth error amplifier versus 1 MHz on the UC3842. Feedback techniques are identical to the UC3842 family. Stray capacitance on FB should be kept as small as possible, and the lead length as short as possible to achieve best stability.

PIN 3 CS--The UCC3802 current sense is significantly different from its predecessor. The UC3842 current sense input connects to only the PWM comparator. The UCC3802 Current Sense input connects to two comparators; the PWM comparator and the over-current comparator. Internal leading edge blanking masks the first 100ns of the current sense signal. This **MAY ELIMINATE THE NEED FOR AN RC CURRENT SENSE FILTER AND PREVENT FALSE TRIGGERING** due to leading edge noise. Connect CS directly to MOSFET source current sense resistor. The gain of the current sense amplifier on the UCC3802 family is typically 1.65 V/V versus typically 3 V/V with the UC3842 family.

PIN 4 RC--The UCC3802's oscillator allows for operation to 1 MHz versus 500KHz with the UC3842. Both devices make use of an external resistor to set the charging current for the capacitor which determines the oscillator frequency. For the UCC3802 and UCC3804

$$F_{Hz} = \frac{1.5}{R_{OHMS} \bullet C_F}$$

For the UCC3803 and UCC3805

$$F_{Hz} = \frac{1.0}{R_{OHMS} \bullet C_F}$$

The two equations are different due to different reference voltages. The recommended range of timing resistor values is between 10K and 200K; the recommended range of timing capacitor values is between 100pF and 1000pF. The peak to peak amplitude of the oscillator waveform is 2.45 Volts versus 1.7 Volts. For best performance, keep the timing capacitor lead to GND as short as possible. Separate ground traces for the timing capacitor and all other pins are recommended. The maximum duty cycle for the UCC3802/03 is approximately 99%; the maximum duty cycle for the UCC3803/04 is approximately 49%. The duty cycle **CANNOT** be easily modified by adjusting RT and CT, unlike the UC3842A family. The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor RT and the internal oscillator discharge transistor on-resistance, like the UC3842. However, maximum duty cycle limits less than 90% for the UCC3802/03 and less than 45% for the UCC3804/05 can not reliably be set in this manner. For better control of maximum duty cycle, consider using the UCC3807.

PIN 5 GND--Both devices same.

PIN 6 OUT--The output of the UCC3802 is a CMOS output versus a Bipolar output on the UC3842. Peak output current remains the same +/- 1 Amp. The CMOS output provides very smooth rising and falling waveforms, with virtually no overshoot or undershoot. Additionally, the CMOS output provides a low resistance to the supply in response to overshoot, and a low resistance to ground in response to undershoot. Because of this, **SCHOTTKY DIODES MAY NOT BE NECESSARY** on the output. Furthermore, the UCC3802 has a self-biasing, active low output during UVLO. This feature **ELIMINATES THE GATE TO SOURCE**

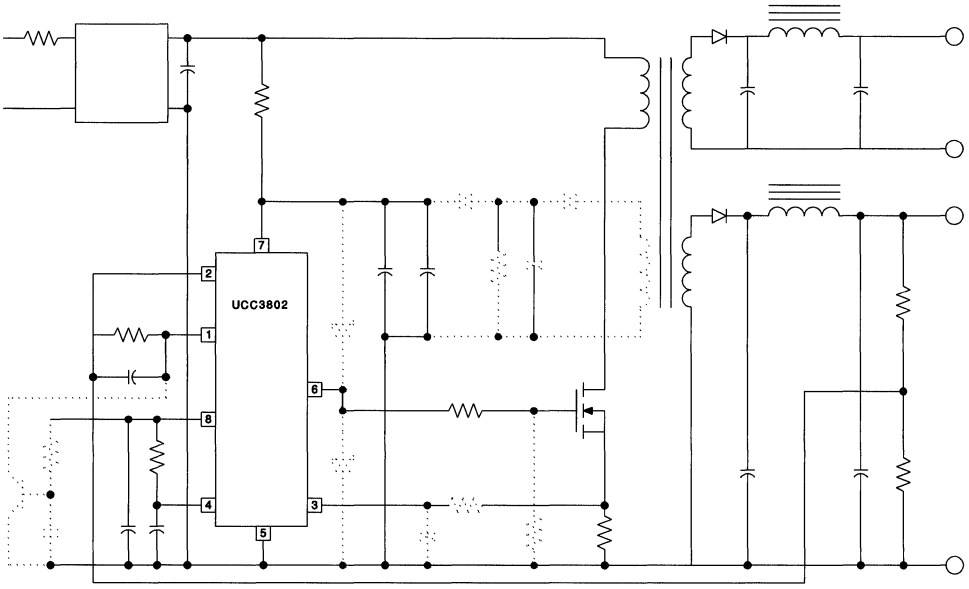

Figure 1

Figure 1 illustrates a nonisolated off-line flyback. Dotted components may be eliminated using the UCC3802 family.

"BLEEDER" RESISTOR associated with the MOSFET gate drive. Finally, **NO MOSFET GATE VOLTAGE CLAMP** is necessary with the UCC3802 as the on-chip zener diode automatically clamps the output to VCC.

PIN 7 VCC--The UCC3802 has a lower VCC (supply voltage) clamp of 13.5 Volts typical versus 30 Volts on the UC3842. For applications which require a higher VCC voltage, a resistor must be placed in series with VCC to increase the source impedance. The maximum value of this resistor

$$Rmax = \frac{VIN(min) - VCC(max)}{ICC + Qgate \bullet F}$$

Additionally, the UCC3802 has an on-chip zener diode to regulate VCC to 13.5 Volts. The turn-on and turn-off thresholds for the UCC3802 family are significantly different: 12.5V and 8V for the UCC3802 and UCC3804; 4.1 V and 3.6V for the UCC3803 and UCC3805. 5 Volt PWM operation is now possible. To ensure against noise related problems, filter VCC with an electrolytic and bypass with a ceramic capacitor to ground. Keep the capacitors close to the IC pins.

PIN 8 REF--The UCC3802 and UCC3804 have a 5 Volt reference. The UCC3803 and UCC3805 have a 4 Volt reference; both +/- 1% versus +/- 2% on the UC3842 family. The output short circuit current is lower...5mA versus 30mA. REF must be bypassed to ground with a ceramic capacitor to prevent oscillation and noise problems. REF can be used as a logic output; as when VCC is lower than the UVLO threshold, REF is held low.

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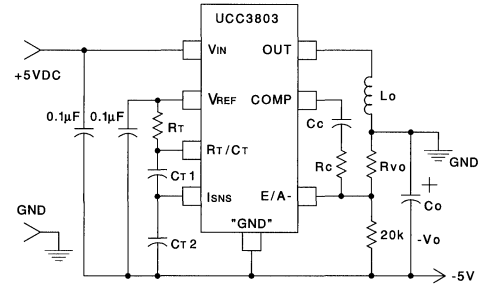
Simple Techniques to Generate a Negative Voltage Bias Supply from a Positive Input Voltage

by Bill Andreycak

Developing a low power negative supply voltage from a positive input supply can be accomplished using some very common PWM control ICs. Typical applications include generating a negative five through twelve volt (-5V to -12V) supply for analog function ICs (OP amps), RS-232 communication circuits, and MOSFET or IGBT gate drives at power levels below a few Watts.

Many PWM ICs contain a high current totem pole output which goes high during the device's ON-time or pulse width. The exact pulse width is modulated to regulate a converter's output voltage during changes in input voltage and output current. The IC's totem pole output can also be used as the main switch in low power applications. One example of this is a Flyback converter configured as shown in Figure 1.

Figure 1: Low Power Negative Output Voltage +5V to -5V Inverter



With this arrangement, the inductor (L) charges when the IC output is high and discharges or flies-back when the IC output goes low. Energy stored during the inductors charging time is transferred to the output capacitor (Cout) during the flyback, or OFF portion of the cycle. When a BiCMOS PWM control IC is used, the external diode can be replaced by the MOS channel and body diode of the IC's lower totem pole transistor thus saving one component. Reverse recovery characteristics are not a concern since current also flows through the MOS transistor channel in parallel with the body diode.

The circuit can be designed for either continuous or discontinuous inductor current operation, depending on the application. Discontinuous mode is generally preferred at lower power levels to minimize inductor size. Continuous inductor current operation is more applicable with higher load currents. High frequency switching and surface mount packaging options minimize overall size.

Conventional duty cycle control (voltage mode) is less complex to implement as the control technique than current mode control. The principal difficulty is sensing the inductor current which is not referenced to the IC's return connection, -Vout instead of ground. Adding a current sense transformer is possible, but will increase cost and complexity. Overcurrent protection is obtained by using the IC's internal maximum current limit at the switch.

Note that the BiCMOS UCC3803 device used in the example circuit of Figure 1. has a maximum low impedance input supply voltage rating of 12VDC. This limits it's applications to less than negative seven volts outputs (-7V max) with a +5V DC input. Higher voltage outputs, for example -12V to -15V, can be obtained by using a UC3843 with a higher maximum input voltage (30VDC). Here too there are some limitations. These fully bipolar ICs draw higher supply current and have higher undervoltage lockout (UVLO) thresholds, but are acceptable choices for some applications.

The IC datasheet should be referred to for additional information. Application Notes within the IC databook contain general information about the design of the Flyback converter, and others. For further assistance contact a Unitrode Field Application Engineer or the factory.

8/93

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UC3846, UC3856 and UCC3806
Push Pull PWM Current Mode Control ICs

by Jack Palczynski

The UC3856 is a pin for pin compatible high performance bipolar version of the industry standard UC3846. It can replace the UC3846 with few circuit modifications and features increased speed, higher gate drive current and reduced propagation delays. The UCC3806 is a BiCMOS pin for pin compatible ultra low power version ideal for battery, low power and high speed applications. The UCC3806 may also replace the UC3846 with few circuit changes.

Specification Differences :

	UC3846	UC3856	UCC3806
Process	**40V Bipolar**	**40V Bipolar**	**18V BiCMOS**
General:			
Startup Current (max)	21mA	23mA	100µA
Operating Current	21mA	23mA	1.4mA
Output Section:			
Supply Vc (max)	40V	40V	15V
Drive Voltage Supply	40V (max)	40V (max)	18V (max)
Rise and Fall Time	300ns (max)	80ns (max)	65ns (max)
Peak Output Current	0.5A	1.5A	0.5A
Oscillator Section:			
Oscillator Discharge I	---------	6.7 to 8.8mA	2.2 to 2.9mA
Initial Accuracy	43kHz ±9.3%	200kHz ±15%	49kHz ±22%
Sync V_{OH} (min)	3.9V	2.4V	2.4V
Sync V_{OL} (max)	2.5V	0.4V	0.4V
Sync V_{IH} (min)	3.9V	2.0V	2.0V
Sync V_{IL} (max)	2.5V	0.8V	0.8V
Sync I_{INPUT} (max)	1.5mA	10µA	1µA
Sync I_{OUTPUT} (max)	-5mA	±10mA	±30mA
Error Amp Section:			
Input I_{OFFSET}(max)	250nA	500nA	500nA
Open Loop Gain	105dB (typ)	100dB (typ)	100dB (typ)
Unity Gain BW	1MHz (typ)	1.5MHz (typ)	3MHz (typ)
PSRR (typ)	105dB	100dB	100dB
Current Sense Amp Section:			
Input CM Range	0V to (V_{IN} - 3V)	0V to 3V	0V to (V_{IN} - 3.5V)
Shutdown Terminal Section:			
Threshold Voltage	0.35V (typ)	1V (typ)	1V (typ)
Input Voltage Range	0V to V_{IN}	0V to 5V	0V to V_{IN}
Delays:			
I_{SENSE} amp to Output	500ns (max)	250ns (max)	175ns (max)
Shutdown to Output	600ns (max)	110ns (max)	100ns (max)
Sync Delay to Output	300ns (typ)	50ns (typ)	50ns (typ)

8/93

Applications Information:

When replacing the UC3846 with a **UC3856**, extra care must be taken to decouple V_{IN}, V_C and V_{REF} with ceramic capacitors close to the leads of the IC. In applications where high output currents are seen, very fast rise and fall times can cause source ripple which can induce problems for PWM ICs which are not properly decoupled. Note also that the shutdown voltage changes from 350mV to 1V. Oscillator frequency is calculated differently, however similar mechanisms generate the oscillator frequency and dead times. As with any bipolar PWM IC, outputs should be protected from negatively biasing the substrate. This is typically done by using Schottky diodes from ground to each output. Failure to do this could cause spurious interruption and restart of the oscillator, dropping of output pulses and a significant increase in propagation delays. The input of the current sense amplifier is slew rate limited allowing lower values of filter capacitors to be used to eliminate leading edge noise. As with the UC3846, the UC3856 uses a differential current sense amplifier which can eliminate ground loop problems and increase noise immunity.

When replacing the UC3846 with the **UCC3806**,output Schottky diodes can be eliminated because the totem pole output is made of MOSFETs which may conduct current in either direction. As with any MOS device, higher impedances require proper decoupling with ceramic capacitors close to the IC. V_{IN}, V_C and V_{REF} should all be properly decoupled. Note that the UCC3806 has a limiting regulator to limit V_{IN} to 15V and the shunted current must be limited to 10mA. To determine oscillator frequency; a 1.25V source through R_T (min 12.5k) creates a current which is mirrored to C_T. This current charges C_T from zero to 2.5V, at which point the outputs are turned off. Both outputs remain low while C_T discharges to zero volts from a 2.6mA current sink. The Shutdown threshold voltage (pin 16) is 1V. The specific Shutdown mode is determined by a switched internal 190µA sink between pin 1 and ground, turned on when a shutdown is triggered. If the Shutdown voltage falls below 350mV, a restart is triggered. Otherwise, the oscillator remains latched off. As with the UC3856, the UCC3806 current sense amplifier is slew rate limited allowing less leading edge filtering to be used. This amplifier is also fully differential, eliminating ground loop problems associated with noisy environments. For additional information consult Application Note U-144 or contact a Unitrode Field Applications Engineer.

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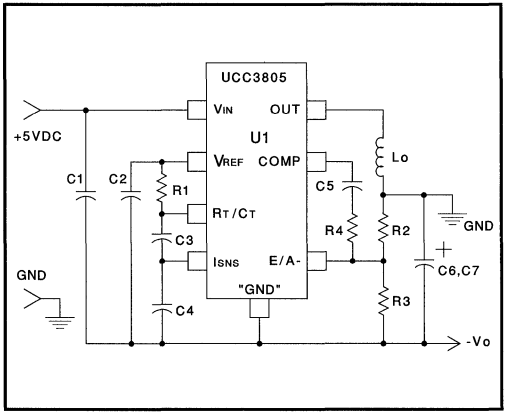
Highly Efficient Low Power DC to DC Inverter Converts +5V Input to -3V Output

* Achieves 73% Efficiency at 0.2 Watt

by Bill Andreycak

Operational Notes : The UCC3805 PWM control IC is used in this Flyback inverter application to perform three functions; control, switching and output rectification. During the PWM ON-time, the upper totem pole switch of the IC's output is turned on applying the 5 volt input across the inductor (Lo) which stores energy. The PWM output goes low when the correct duty cycle is achieved to regulate the output voltage, Vo. This turns off the upper totem pole switch and turns on the lower one, connecting the inductor to the output voltage (-3V) rail. The lower totem pole switch acts as a synchronous rectifier in parallel with the internal MOS body diode. This condition necessitates discontinuous inductor current operation at all times to avoid high cross-conduction currents in the IC output stage.

Circuit Schematic



The duty cycle is controlled using conventional voltage mode operation. The IC's oscillator timing waveform (R_T/C_T) is capacitively divided down to the appropriate amplitude (1V max) and fed into the I_{SNS} pin. A regulated output is obtained by resistively dividing down the output to 2.0 volts above the IC's "ground" (which is at -3V) and input to the error amplifier's inverting input (E/A-). A 400kHz oscillator frequency results in 200kHz switchmode power conversion due to the IC's internal divide-by-two toggle flip-flop. This is done to limit the maximum duty cycle to below 50% while maintaining the benefits of high frequency operation.

A 200 milliwatt converter was constructed to deliver -3.0 volts at approximately 65 milliamps from a +5 volt input supply. Peak efficiency at full load measured 73% with V_{IN} = +5.5V, 69% with +5.0V and 60% at +4.75V input.

Higher switching frequencies are a practical choice to reduce the inductor volume, although some degradation in efficiency is to be expected. The use of surface mount components results in a very compact DC to DC converter, suitable for "on-card" regulators and distributed power applications.

List of Materials

C1	0.1µF / 16V
C2	0.1µF / 16V
C3	100pF / 6V
C4	270pF / 6V
*C5	1nF / 6V
C6	1.0µF / 6V
C7	100µF / 6V
SPRAGUE	#592D-107X06R3R2
L1	150µH / 0.4µJ
COILCRAFT	# DT3316-154
R1	30k / 0.1W
R2	11.0k / 0.1W
R3	20.0k / 0.1W
*R4	100k / 0.1W
U1	UCC3805 PWM

Other Applications:

+5V to -2V : A minus two volt (-2V) output can be obtained with the same circuit by simply replacing resistor R2 with a short circuit. The inductor value may need to be modified depending on the desired output current.

+5V to -5V : A minus five volt (-5V) output is obtained by using a 30k ohm value for resistor R2. Note that the UCC3803 device is recommended (without the toggle flip flop) to achieve a higher maximum duty cycle. The inductor value needs to be calculated based upon output current and switching frequency. Higher overall efficiency can be obtained than in the -3V application due to the higher output voltage (-5V).

Consult Unitrode Design Note DN-43 for other simple DC-DC inverter applications, or contact a Unitrode Field Applications Engineer.

* Coilcraft telephone number: 1-800-322-COIL

* Sprague telephone number: 1-207-324-4140

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Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range

by Jack Palczynski

Much attention has been given to the Single Ended Primary Inductor Converter (SEPIC) topology recently because output voltage may be either higher or lower than input voltage. The output is also not inverted as is the case in a flyback or Cuk topology. Voltage conversion is accomplished without transformers, instead using low cost inductors to transfer energy. The input and output voltages are DC isolated by a coupling capacitor. This design note illustrates an application for a 5V, 100mA output converter for battery powered and Automotive applications. It makes use of a UCC3803 BiCMOS current mode controller to provide a 5V output at full load of 100mA from an input of 2.5V to 13.5V after an initial start-up at 5 volts.

This SEPIC converter uses current mode control to simplify stabilization of the control loop. Peak current in the FET is limited by the pulse by pulse current limiting of the UCC3803. Switching frequency is 500kHz, allowing low output current handling and low output ripple with small inductors and capacitors while remaining in the continuous inductor current mode (CCM). Once started, the low voltage operation of the UCC3803 is extended by bootstrapping from the output through a UC3612 Schottky diode. By including slope compensation (Q2, R3), the duty cycle may exceed 50% without experiencing subharmonic oscillations.

This topology places higher stresses on both the switch and the diode than with other PWM topologies. Peak switch and diode stresses are both $V_{IN}+V_{OUT}$ and $I_{IN} + I_{OUT}$. Peak to peak ripple current in the coupling capacitor is $I_{IN} + I_{OUT}$.

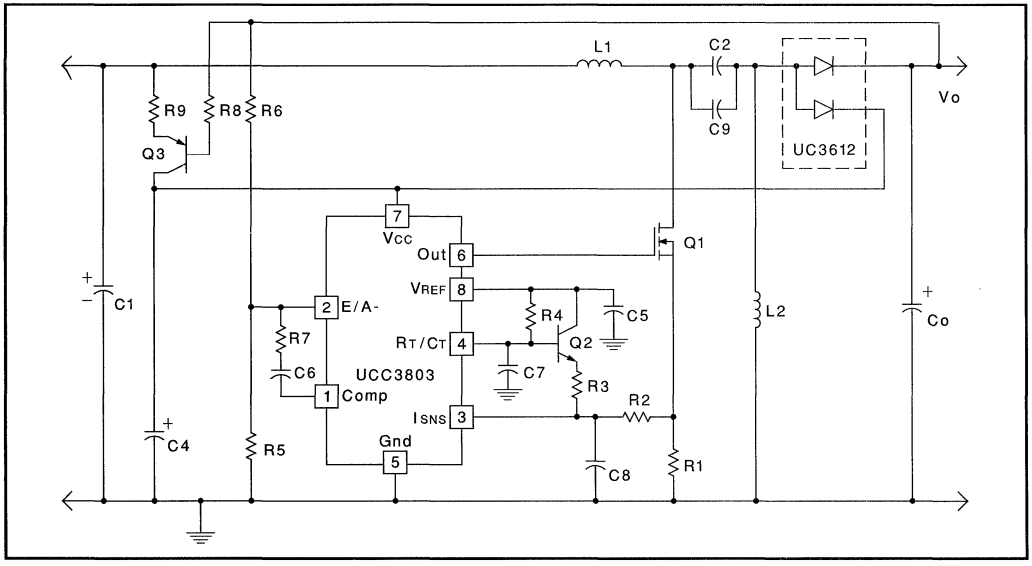


Figure 1. UCC3803 Controlled SEPIC Converter

Specifications :

VIN (initial start-up) 5V
VIN ..... 2.5V to 13.5V
IOUT ..... 45mA to 100mA
Switching Frequency 500kHz
Output Regulation ..... ±3%
Output Ripple ..... 150mV (max)

SEPIC Converter Design Guide:

1. Choose a switching frequency, fs.

$fs = 500kHz$

2. Calculate minimum duty cycle (DMIN):

$$DMIN = \frac{Vo}{Vo + VIN(max)}$$

$$DMIN = \frac{5V}{(5V + 13.5V)} = 0.27$$

3. Calculate maximum duty cycle (DMAX):

$$DMAX = \frac{Vo}{Vo + VIN(min)}$$

$$DMAX = \frac{5V}{(5V + 2.5V)} = 0.67$$

4. Find an appropriate inductor so that IDIODE is not less than zero (note that this value should be used for both inductors):

$$L > \frac{VIN(max) \bullet DMIN}{fs \bullet Io(min)\left(\frac{Vo}{VIN(max)} + 1\right)}$$

$$L1 = L2 > \frac{13.5V \bullet 0.27}{500kHz \bullet 45mA\left(\frac{5}{13.5} + 1\right)} = 118\mu H$$

Note that the COILCRAFT inductor selected is specified at twice this value of inductance at light load, and decreases at high loads.

5. Calculate IIN(max) at maximum output current:

$$IIN(max) = \frac{Io(max) \bullet D(max)}{1 - D(max)}$$

$$IIN(max) = \frac{0.1 \bullet 0.67}{1 - 0.67} = 202mA$$

6. Find RMS current ripple and choose an appropriate Ccc:

$$\sqrt{Io(max)^2 \bullet D(max) + IIN(max)^2 \bullet (1 - D(max))}$$

$$\sqrt{0.1^2 \bullet 0.67 + 0.2^2 \bullet (1 - 0.67)} = 141mA$$

Select a capacitor to handle this ripple current.

7. Choose an output capacitor for ripple voltage:

$$dIO(max) = IIN(max) + \frac{VIN(max) \bullet D(max)}{2Lfs}$$

$$dIO(max) = 202mA + \frac{2.5V \bullet 0.67}{2 \bullet 220\mu H \bullet 500kHz} = 209mA$$

then, ripple voltage

$$dV > dIo(max)\left(\frac{1}{2\pi fs \bullet C} + ESR\right)$$

$$150mV > 209mA\left(\frac{1}{2\pi \bullet 500kHz \bullet 33\mu F} + 0.7\right) = 148mV$$

Some iterations with different capacitors will yield an acceptable voltage ripple.

It may become necessary to run the converter in discontinuous inductor current mode (DCM) when minimum load is a very small percentage of the maximum load. D will become dependent on output load and output voltage regulation will vary more than in CCM. The CCM system double pole occurs at

$$fdp = \frac{1}{\sqrt{2} \bullet \pi (L1 + L2)Ccc}$$

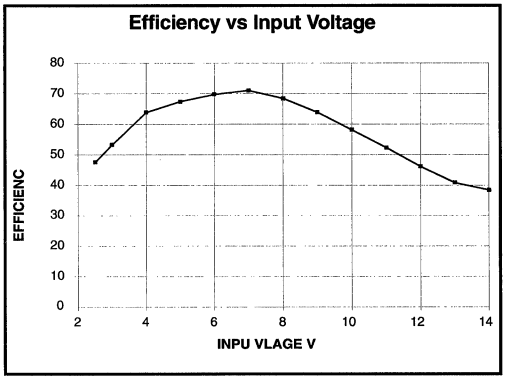
and the ESR zero occurs at

$$fz = \frac{1}{2 \bullet \pi \bullet ESR \bullet Co}.$$

A plot of efficiency is shown below for the range of input voltage. Efficiency may be increased by using lower switching frequencies at a cost of larger components. This might be desirable in equipment with small batteries that demand lower power consumption for extended life.

The SEPIC converter may be used for a wide range of output voltages over a range of input voltages.

Other outputs tested were 3V and 12V with circuits similar to that of this design note. As output current increases, conduction losses in the switch and output diode begin to degrade efficiency and ripple current in the coupling capacitor may be excessive. In high power applications, a transformer isolated converter or cascaded stages may be more practical.



Parts List:

D1, D2	Unitrode UC3612D Dual Schottky phone # (603) 429-8610
C1-3, C9	33µF 25V Sprague 293D336X0025E2T phone # (207) 324-4140
C4,C5,C6	0.1µF Ceramic
C8	150pF Ceramic
L1, L2	220µH COILCRAFT DT3316-102-224 phone # (708) 639-1469
Q1	Siliconix Si9410DY phone # (800) 554-5565
Q2	2N2222S
Q3	2N2907AS
R1	1 ohm 1/4W
R2	1k 1/8W
R3, R6	10k 1/8W
R4	30k 1/8W
R5, R7	6.2k 1/8W
R8,R9	50 ohm 1/8W
U1	Unitrode UCC3803D BiCMOS PWM IC

REFERENCES:

[1] W. Andreycak U-133 "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Application Note

[2] L. Dixon "High Power Factor Preregulator Using the SEPIC Converter" Unitrode Seminar SEM-900 pp. 6.1-6.12

[3] L. Dixon "Control Loop Design SEPIC Preregulator Example" Unitrode Seminar SEM-900 pp. 7.1-7-6

[4] U-97 "Modeling, Analysis and Compensation of the Current-Mode Converter" Unitrode Applications Handbook A-100 pp. 260-266

[5] U-100 "UC3842 Provides Low-Cost Current-Mode Control" Unitrode Applications Handbook A-100 pp.278-291

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UC2577 Controls SEPIC Converter for Automotive Applications

by Jack Palczynski

The Single Ended Primary Inductance Converter (SEPIC) can convert an input voltage to an output voltage that is higher, lower or equal to the input. Conversion is performed without the use of expensive transformers, making this a good choice for low cost, non-isolated applications. The UC2577 provides the switch and control to take advantage of this topology with a minimum of additional parts.

The circuit shown in Figure 1 was designed to provide a 5V or 12V output from an input voltage ranging between 3V and 40V. The coupling capacitor is chosen to handle the high ripple current seen in this topology, with a peak-to-peak current of approximately $I_{IN} + I_{OUT}$. The converter switches at 52kHz and operates in both continuous inductor current mode (CCM) and discontinuous inductor current mode (DCM). Note that both the diode and the switch have a peak voltage stress of approximately $V_{IN} + V_{OUT}$, and peak current stress of approximately $I_{IN} + I_{OUT}$. Note that when the converter is in CCM, the ratio of $V_{OUT}/V_{IN} = D/(1-D)$ where D is the duty ratio. To calculate components for other inputs and outputs, assume CCM as a starting point and use about 1/2 max output current as a min value. For further details, consult Unitrode Design Note DN-48.

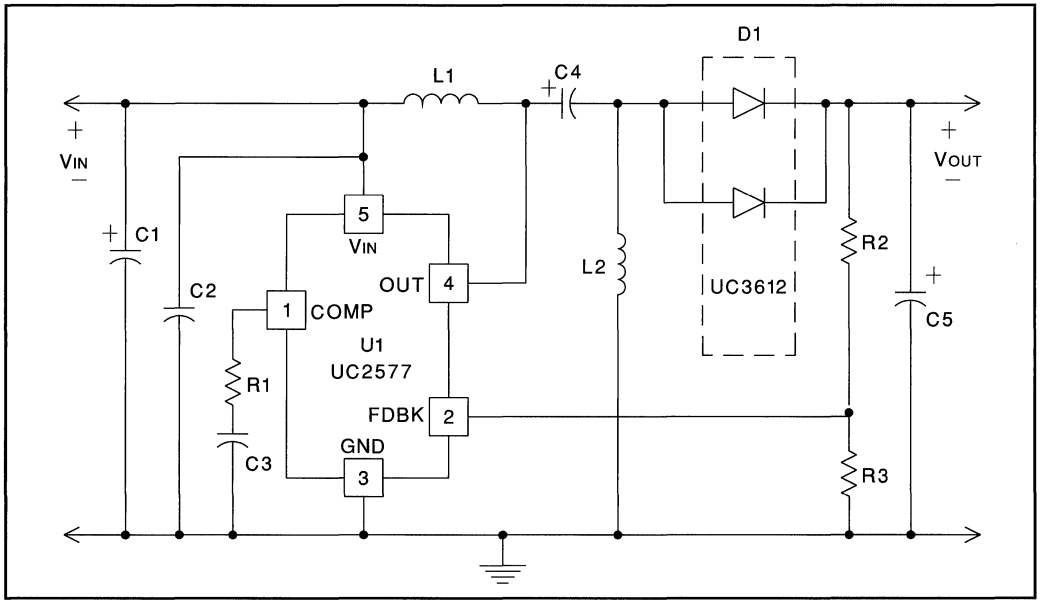

Figure 1. Easy SEPIC Converter Schematic

Parts List:

U1	UC2577
D1	UC3612 Dual Schottky
L1,L2	100µH ECI # M1088 phone (413) 562-7684
C1	47µF/50V Sprague 515D476M050AA6A phone (207) 324-4140
C2	0.1µF ceramic
C3	0.47µF ceramic
C4	220µF/50V Sprague 515D227M050CD6A
C5	220µF/6V Sprague 595D227X9006D7 (5V output)
* C5	12V output only, use four 68µF/16V Sprague 293D686X0016D2T
R1	100 ohm 1/8W
R2	3.01k 1/8W
R3	1k 1/8W (5V output)
* R3	330 ohms 1/8W (12V output)
* D2,3	UC3612 Dual Schottky (Extended Operating Range)

Efficiency was measured for the 5V (Figure 2) and 12V (Figure 3) output at two power levels for the full range of Automotive input voltages.

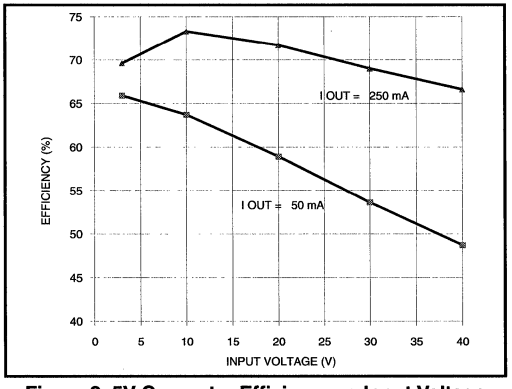

Figure 2: 5V Converter Efficiency vs Input Voltage

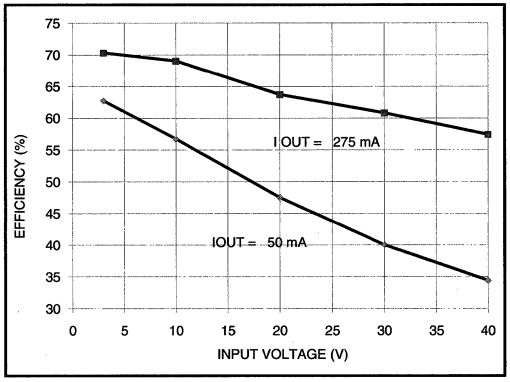

Figure 3: 12V Converter Efficiency vs Input Voltage

As seen in Figure one, a simple design is used to convert power for automotive applications. If longer hold up times are needed or operation at low input voltages demanded, the circuit in Figure 4 may become useful. By adding two diodes, the output voltage bootstraps the IC and allows operation even after the input voltage drops below the operating range of the IC.

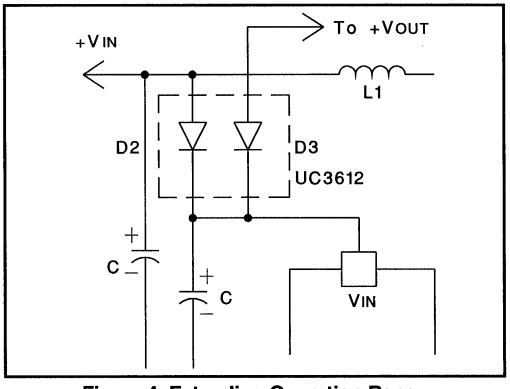

Figure 4: Extending Operation Range

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Programming the UCC3806 Features

by Jack Palczynski

INTRODUCTION

The UCC3806 is a pin for pin compatible BiCMOS replacement for the UC3846 and UC3856. Some functions in the UCC3806 are programmed differently and these methods are explained here. In particular, the CUR LIM ADJ pin programs the maximum peak current for the current sense amplifier. This function is completely compatible with previous ICs. The second function on this pin is the latch/non-latch feature for the shutdown pin. Programming latch or non-latch mode differs from the UC3846 and UC3856 and these changes will be explained here.

Current Limit Adjust

To review, the CUR LIM ADJ pin adjusts the maximum current peak on the current sense amplifier (pin 4 to 3) by the formula: Vcl=1/3 * [(R2*VREF)/(R1+R2) -0.5] . This can be verified by carefully following the path from the current sense amplifier to the CUR LIM ADJ pin. A second function is for shutdown mode programming. When the shutdown pin voltage exceeds 1V, the UCC3806 outputs shut down. At this point, a 190µA (typ) current sink pulls current from the CUR LIM ADJ pin to ground. If the voltage at the CUR LIM ADJ is above

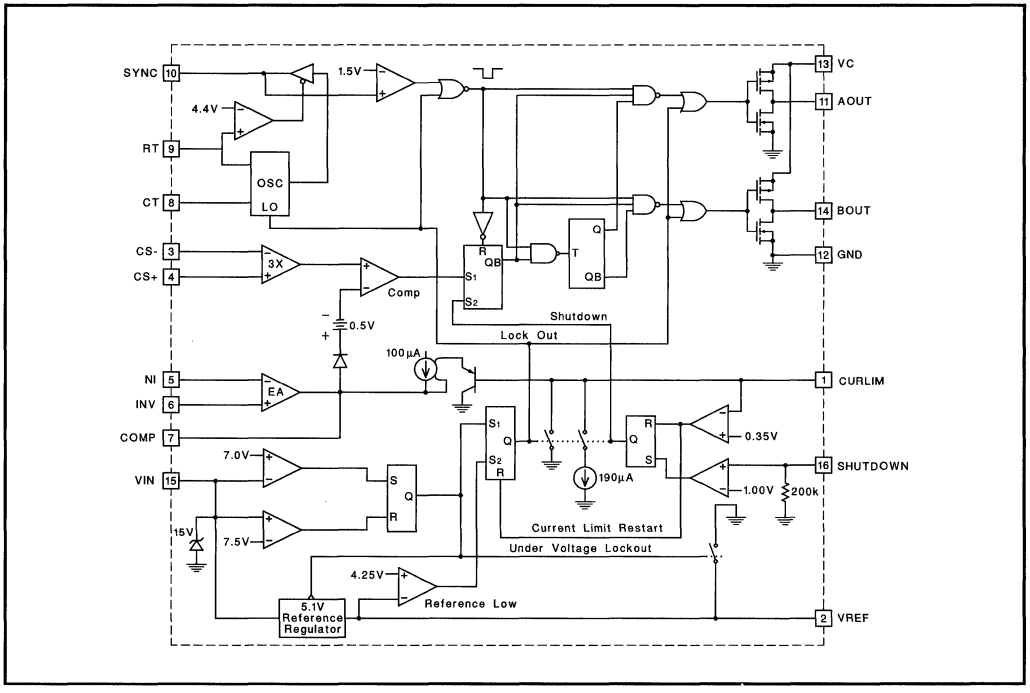

Figure 1: UCC3806 BiCMOS Current Mode PWM Block Diagram

350mV (typ), then the IC remains latched off. If this voltage falls below 350mV at any time, the shutdown is unlatched and the IC restarts. Calculating the actual voltage on the CUR LIM ADJ pin is a simple, two source superposition problem.

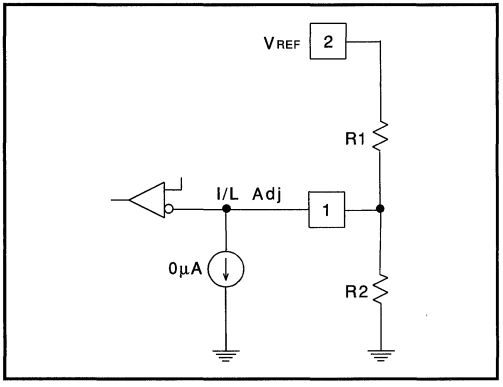

Figure 2: Superposition with current sink = 0

$V = (V_{REF} * R2)/(R1+R2)$

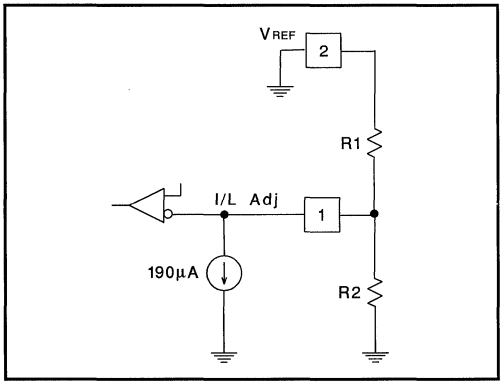

Figure 3: Superposition with V_{REF} = 0

$V=[-190\mu A*(R1*R2)]/(R1+R2)$

Combining equations:

$V=(V_{REF}-R1*190\mu A)/[1+R1/R2)]$

The internal current sink is specified to be between 80µA to 300µA. This is the dominant source for error for this application, thus worst case values are inserted into the above equation to determine latch and non-latch modes.

I LIM ADJ Latching Mode Voltage:

$V=(V_{REF}-R1*300\mu A)/[1+R1/R2)]$ >350mV

I LIM ADJ Non-Latching Mode Voltage:

$V=(V_{REF}-R1*80\mu A)/[1+R1/R2)]$ <350mV

Solving either of these equations and solving the equation for a desired current limit pin voltage simultaneously gives closed form solutions for R1 and R2. Some solutions are shown below.

Table of Approximate Resistor Value:

Latching Mode:			
V (pin 4)	**R1**	**R2**	**V (pin 1)**
1.0	16.5k	38.3k	0.1
0.77	15k	18.2k	0.3
0.5	14.7k	9.76k	0.3

Non-Latching Mode:			
V (pin 4)	**R1**	**R2**	**V (pin 1)**
1.0	54.9k	130k	0.5
0.77	54.9k	66.5k	0.4
0.5	51.1k	34k	0.4

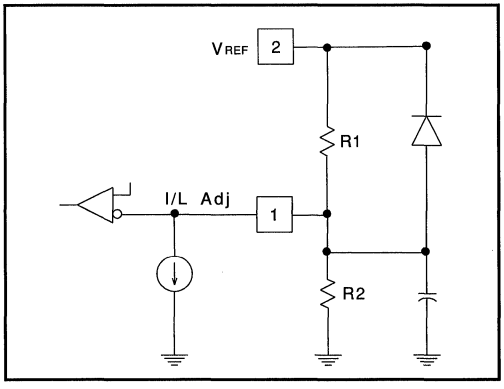

Figure 4: Soft starting the current

Softstart

The CUR LIM ADJ may also be used as a convenient soft start point. By adding a capacitor across R2, maximum current sense ramps up as the soft start capacitor charges. A diode may be added to force a quick discharge of the capacitor when IC power is removed.

SUMMARY

With a systematic approach, one may achieve a variety of maximum current peak levels and the desired shutdown mode. In addition, the UCC3806 allows for a programmed softstart by adding a capacitor to the CUR LIM ADJ pin. By understanding the internal workings of the UCC3806, designers will find many features which can be of great help in reducing parts count and current requirements.

REFERENCES

(1) W. Andreycak, "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Integrated Circuits Corporation U-133, Unitrode Product & Applications Handbook '93-'94, pp. 9-344 to 9-361.

(2) J. Palczynski, "UCC BiCMOS Current Mode Control IC" Unitrode Integrated Circuits Corporation Applications Note U-144.

(3) W. Andreycak, "Practical Considerations in Current Mode Power Supplies" Unitrode Integrated Circuits Applications Note U-111, Unitrode Product & Applications Handbook '93-'94, pp. 9-134 to 9-151.

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Innovative Buck Regulator Uses High Side N-Channel Switch Without Complex Gate Drive

Converts +5 VDC to +3.3 VDC (or others) and draws only 40 microamps in standby mode

by Bill Andreycak

Obtaining very high efficiency in a voltage step-down (Buck regulator) application often requires the use of N channel, low on-resistance MOSFET switches. The difficulty in driving these enhancement mode devices on the high side of a converter is that they require a gate voltage above the input supply to turn-on. This necessity demands an additional supply voltage solely for the high side gate drive. Although P channel devices are a viable alternative for the sake of gate drive simplicity, their associated cost and higher on resistance limits the number of applications. Typically, P channel FETs are used in Buck regulators with output currents below 4 amps, or so. However, the demand of many 1.8 volt through 3.3 volt logic systems is often in the neighborhood of 10 amps, forcing the use of N channel devices.

The circuit shown in Figure 1. incorporates the UCC3803 BiCMOS PWM controller in a conventional voltage mode controlled Buck regulator application. Normally, the IC needs to be supplied with a separate 12 volt supply from the input to the Buck converter. As the MOSFET is switched on, it's source approaches it's drain voltage (5V) and the gate is driven seven volts higher to the IC's 12 volt supply. Logic level MOSFETs are required for this application which become fully enhanced with only five (or so) volts gate to source in comparison to standard devices which require about ten volts. When Q1 is turned off, the gate is driven to ground by the IC's output and diode DO then conducts the full output current of the regulator.

What's unique about this circuit configuration is the way in which VCC is supplied to the IC. Diode D1 is used to route the initial power to the UCC3803's VCC pin from the 5 volt input. Notice

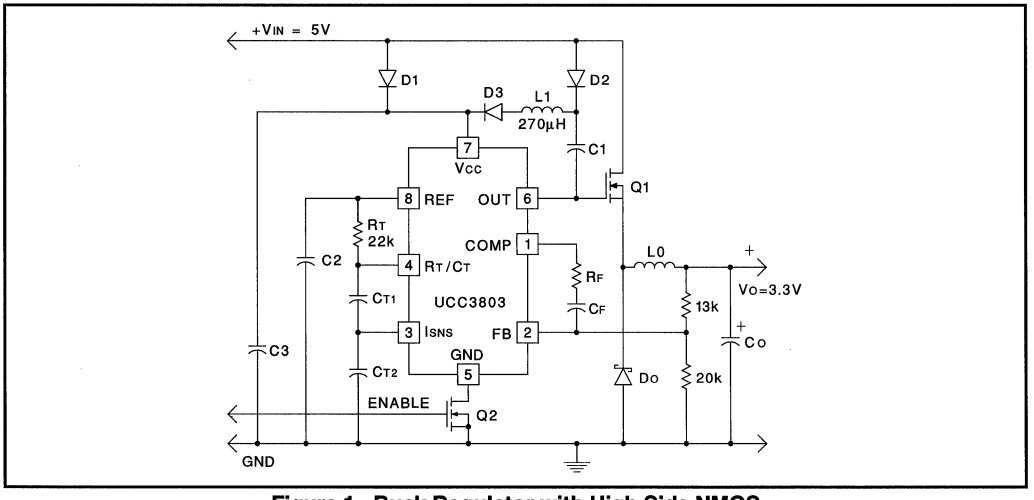

Figure 1. Buck Regulator with High Side NMOS

that diode D2 and capacitor C1 are connected between V_{IN} and the IC's output, pin 6. While the IC is off, it's output is low and capacitor C1 is charged to V_{IN}, or 5 volts. Once the 4.1 volt undervoltage lockout threshold of the IC is crossed, it's PWM output begins switching and goes high. The upper totem-pole transistor within the IC forces the lower end of capacitor C1 (connected to pin 6) up towards the IC's supply voltage, V_{CC}. The initial charge stored by the 5V across C1 is then directed to V_{CC} through diode D3. Essentially, a quasi-resonant tank circuit is formed by the following components; the UCC3803's output, C1, L1 and D3. This simple circuit configuration replenishes the supply voltage (V_{CC}) each time the PWM output switches. After a few initial switching cycles, the ICs supply voltage (V_{CC}) is increased to approximately twice V_{IN}, or about 10 volts. This is a sufficient amplitude to properly drive Logic Level N Channel FETs on the high side of a Buck Regulator. The UCC3803's internal 12 volt supply clamp can also be used to supply a better regulated supply voltage, however any excess current will be shunted to ground. This will reduce overall efficiency slightly, but will immunize the supply voltage from any duty cycle related variations.

The ideal value of inductor L1 is determined by several operating conditions. The critical ones are switching frequency, duty cycle, IC supply current and the current required to supply the MOSFET's gate charge (Q_g) demand. For most high frequency applications, the inductance is in the range of about 50 to 300 microHenries. Note that small, inexpensive surface mount or axial thruhole components the size of a half-watt resistor are ideal candidates. A one time "tweaking" of the exact value during the prototype stage may be required to deliver the best performance over all line and load conditions. Once the best value is established, an adequate supply voltage will obtained over all specified operating conditions.

Operating at 500kHz, the UCC3803 and bootstrap circuit will collectively draw 8 milliamps from the 5 volt input while boosting the supply voltage to approximately 9 volts. Input current rises to around 12mA in order to raise the supply voltage to 11.5 volts. This amplitude is just below the V_{CC} supply clamp voltage threshold of the UCC3803 IC. In most applications, the DC current from the 5 volt input source required to charge the MOSFET gate will be around 20mA, which adds to the IC and bootstrap circuit demands. Typical consumption of the entire working control circuit will be in the 30 to 50mA range, depending on frequency and MOSFET selections.

A low current standby mode can be obtained by using a small logic level MOSFET to switch the IC's ground connection in and out of circuit. When disabled, the entire circuit draws approximately 40 microamps from a 5 volt input. Other adaptations are possible, as shown in Application Note U-133 of the Unitrode IC databook.

Circuit Modifications:

Other output voltages (2.0, 2.2, 2.5, 2.75, 3.0 VDC) :

Any desired output voltage between 2.0V and V_{IN} can be developed using the exact circuit schematic of Figure 1. The modifications required are only to the component values used in the Buck regulator section (L_{OUT}, C_{OUT} and R1), although some adjustment of L1 may also be needed.

High current output:

A high current output can also be achieved using the schematic of Figure 1. by selecting the components appropriately for the higher output power.

Component List:

C1, C2	0.01µF/16 VDC
C3	1µF/16 VDC
C_{T1}	150pF/10VDC
C_{T2}	270pF/10 VDC
D1, D2, D3	1N4148
U1	UCC3803

NOTE : All other components and values depend upon the exact application.

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Design Note

UCC3889 Bias Supply Controller Evaluation Kit – Schematic and Lists of Materials

by Bill Andreycak

Evaluation Kits facilitate a quick measurement of new IC performance in typical application circuits without a lengthy investment of time and resources. The schematic for the UCC3889 Off-Line Bias Supply Controller IC Evaluation Kit is shown below in Figure 1 with a photograph of the top side layout in Figure 2. Notice that this board is designed to accept both conventional "through-hole" or leaded components as well as their surface mount counterparts. An additional prototyping area allows engineers to further customize these units to address their projects' specific needs. Component lists for two popular 1 Watt (output power) applications are also provided, and complete design details are available in Unitrode Application Note U-149: "Elegantly Simple Off-Line Bias Supply for Very Low Power Applications".

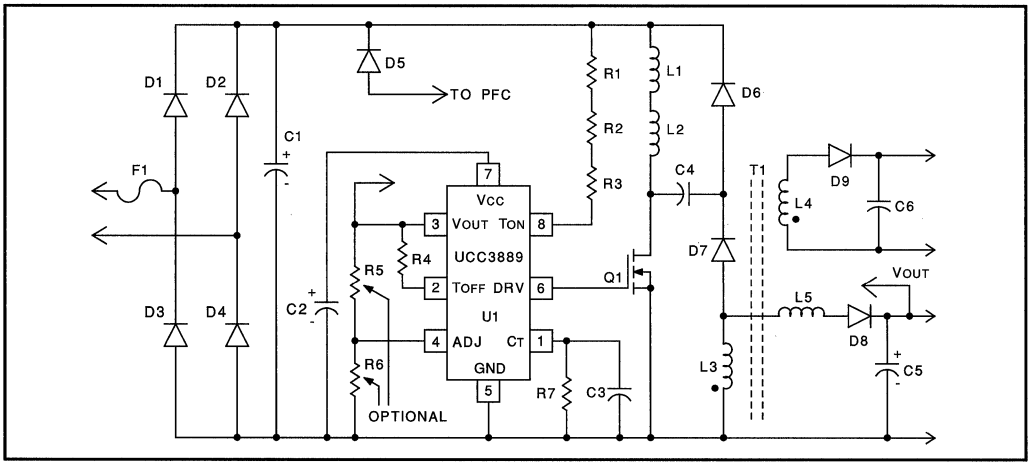

Figure 1. UCC3889 Evaluation Kit Schematic

Nonisolated 85 to 265VAC Universal Input, 12VDC / 1 Watt Converter

C1 = 2.2µF/450 VDC Electrolytic
C2 = 2.2µF/35 VDC Electrolytic
C3 = 150pF/16 VDC Ceramic Disc
C4 = 0.1µF/100 VDC Polyester foil
C5 = 33µF/25VDC Electrolytic (low ESR)
D1-D4 = 1A/800V Rectifier (1N4006)
D6,D7 = 1A/600V Fast Recovery Rectifier (1N4937)
D8 = 1A/200VDC Fast Recovery Rectifier (1N4935)
F1 = 0.2 ADC/250VAC Fuse
L1,L2 = 1mH (each) Inductor, 200 mA peak, 250 VDC rating
L3 = 390µH Inductor, 250mA peak
L5 = Jumper Wire, AWG#20 (short circuit)
Q1 = 600V/2A MOSFET, (MTP1N60 or IRFBC10)
R1,2,3 = 110k, 1/2W, 5%, 150VDC rating each (three used)
R4 = 150k, 1/4W, 5%
R7 = 2 Meg, 1/4W, 5%
U1 = UCC3889 Control IC

Components **NOT USED** in this design:
C6, D5, D9, L4, R5, R6

Optional component list:
D5 = 1A/800V DIODE (1N4006) - used with DC input from PFC or UPS
R5,R6 = 1/4W, 5% resistors - used to program other output voltages

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Transformer Isolated 85 to 265VAC Universal Input, 12VDC / 1 Watt Converter

C1 = 2.2µF/450 VDC Electrolytic
C2 = 1µF/35 VDC Electrolytic
C3 = 150pF/16 VDC Ceramic
C4 = 0.1µF/150 VDC Polyester foil
C5,6 = 33µF/25VDC Electrolytic (low ESR)
D1-4 = 1A/800V Rectifier (1N4006)
D6,7 = 1A/600V Fast Recovery Rectifier (1N4937)
D8,9 = 1A/200VDC Fast Recovery Rectifier (1N4935)
F1 = 0.2ADC/250VAC Fuse
L1,2 = 1mH (each) Inductor, 200mA peak, 250VDC rating
L4 = Transformer; 1:1 Turns ratio, 300µH (Coilcraft # E3497A)
L5 = 10µH, 750mA peak
Q1 = 600V/2A MOSFET, (MTP1N60 or IRFBC10)
R1,2,3 = 110k, 1/2W, 5%, 150VDC rating each (three used)
R4 = 150k, 1/4W, 5%
R7 = 2 Meg, 1/4W, 5%
U1 = UCC3889 CONTROL IC

Components **NOT USED** in this design:
D5, L3, R5, R6

Optional component list:
D5 = 1A/800V DIODE (1N4006) - used with DC input from PFC or UPS
R5,R6 = 1/4W, 5% resistors - used to program other output voltages

Note that the control technique and cascade Flyback configuration used in these examples can be extended to higher power levels and a variety of applications. This is accomplished by selecting the converter's power components accordingly. Higher current ratings for the power MOSFET, rectifiers and inductors, along with lower inductance values are usually all that's required. Other topologies, for example, the simple (non-cascaded) flyback, forward and boost converters can be controlled by the UCC3889 IC. Many distributed DC power and DC to DC converters make likely candidates for this control technique. Power Factor Correction (PFC) can also be achieved with this IC when used in a discontinuous inductor current boost configuration. Consult Unitrode Application Note U-132 for information on the controlled on-time, variable off-time PFC control technique which can be implemented with the UCC3889 without the need for current sensing. For further information, contact a local Unitrode representative or Field Application Engineer.

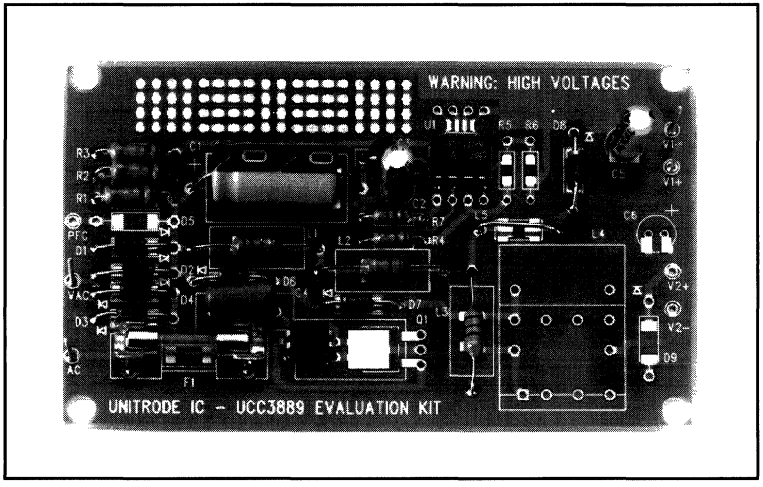

Figure 2. Top Side PC Board Photo

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Design Note

Switching Power Supply Topology Voltage Mode vs. Current Mode

by: Robert Mammano

Unitrode IC Corporation has, since its inception, been active in the development of leading-edge control circuits to implement state-of-the-art progressions in power supply technology. Over the years many new products have been introduced to allow designers to readily apply new innovations in circuit topologies. Since each of these new topologies purports to offer improvements over that which was previously available, it is reasonable to expect some confusion to be generated with the introduction of the UCC3570 - a new voltage-mode controller introduced almost 10 years after we told the world that current-mode was such a superior approach.

The truth, however, is that there is no single topology which is optimum for all applications. Moreover, voltage-mode control - if updated with modern circuit and process developments - has much to offer designers of today's high-performance supplies and is a viable contender for the power supply designer's attention.

To answer the question as to which circuit topology is best for a specific application, one must start with a knowledge of both the advantages and disadvantages of each approach. The following discussion attempts to do this in a consistent way for these two power supply control algorithms.

Voltage Mode Control

This was the approach used for the first switching regulator designs and it served the industry well for many years. The basic voltage mode configuration is shown in Figure 1.

The major characteristics of this design are that there is a single voltage feedback path, with pulse-width modulation performed by comparing the voltage error signal with a constant ramp waveform. Current limiting must be done separately.

The advantages of voltage-mode control are:

1. A single feedback loop is easier to design and analyze.

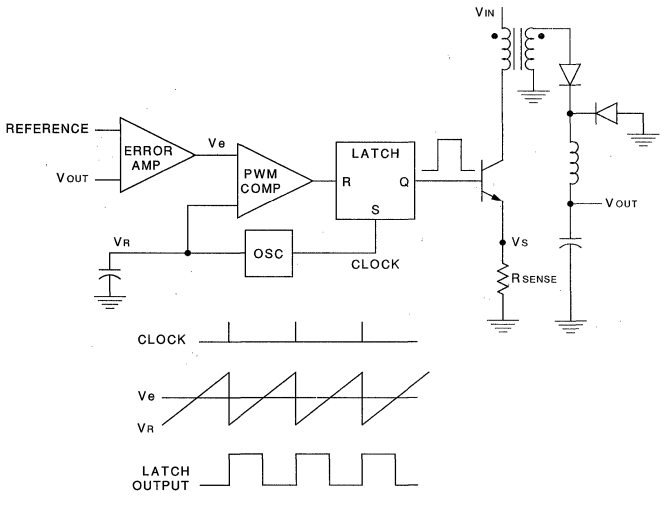

FIGURE 1. VOLTAGE MODE CONTROL

Figure 1. Voltage Mode Control

2. A large-amplitude ramp waveform provides good noise margin for a stable modulation process.
3. A low-impedance power output provides better cross-regulation for multiple output supplies.

Voltage-mode's disadvantages can be listed as:

1. Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response.
2. The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation.
3. Compensation is further complicated by the fact that the loop gain varies with input voltage.

Current Mode Control

The above disadvantages are relatively significant and since all are alleviated with current-mode control, designers were highly motivated to consider this topology upon its introduction. As can be seen from the diagram of Figure 2, basic current-mode control uses the oscillator only as a fixed-frequency clock and the ramp waveform is replaced with a signal derived from output inductor current.

The advantages which this control technique offers include the following:

1. Since inductor current rises with a slope determined by Vin-Vo, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
2. Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop (at least in the normal region of interest). This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.
3. Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the Error Amplifier, and the ease of providing load sharing when multiple power units are paralleled.

While the improvements offered by current-mode are impressive, this technology also comes with its own unique set of problems which must be solved in the design process. A listing of some of these is outlined below:

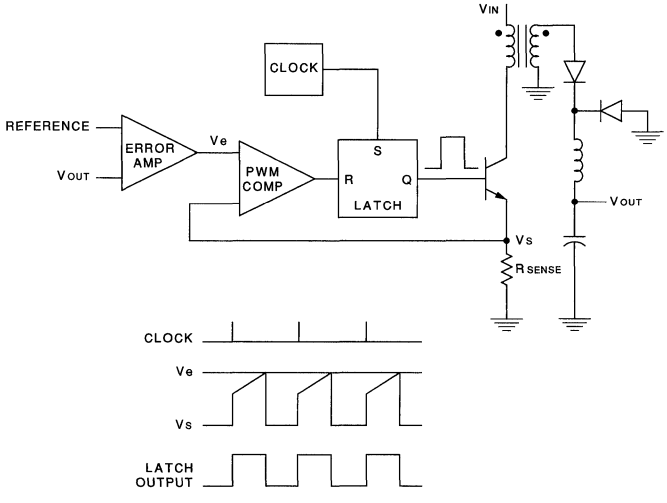

FIGURE 2. CURRENT MODE CONTROL

Figure 2. Current Mode Control

1. There are now two feedback loops, making circuit analysis more difficult.
2. The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.
3. Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop.
4. A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
5. With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross-regulation with multiple outputs.

So from the above we can conclude that while current-mode control will ease many of the limitations of voltage-mode, it also contributes a new set of challenges to the designer. However, with the knowledge gained from more recent developments in power control technology, a re-evaluation of voltage-mode control indicated that there were alternative ways to correct its major weaknesses and the result was the UCC3570.

Voltage-Mode Revisited

The two major improvements to voltage-mode control offered by the UCC3570 are voltage feed-forward to eliminate the effects of line voltage variations, and higher frequency capability which allow the poles of the output filter to be placed above the range of normal control loop bandwidth.

Voltage feed-forward is accomplished by making the slope of the ramp waveform proportional to input voltage. This provides a corresponding and correcting duty cycle modulation with no action needed by the feedback loop. The result is a constant control loop gain and instantaneous response to line voltage changes. The higher frequency capability is accomplished through the use of BiCMOS processing for this IC which yields smaller parasitic capacitance and lower circuit delays. Thus many of the problems of voltage-mode have been alleviated without incurring the difficulties of current-mode.

Choosing Circuit Topologies

None of the above discussion should leave the impression that there is no longer a place for current-mode control - only that both topologies are viable choices in today's environment. There are considerations which could point to one or the other as more optimum for each particular application. Some of these are outlined below:

Consider the use of current-mode if:

1. The power supply output is to be a current source or very high output voltage.
2. The fastest dynamic response is needed with a given switching frequency.
3. The application is for a DC/DC converter where the input voltage variation is relatively constrained.
4. Modular applications where parallelability with load sharing is required.
5. In push-pull circuits where transformer flux balancing is important.
6. In low-cost applications requiring the absolute fewest components.

Consider voltage-mode (with feed-forward) if:

1. There are wide input line and/or output load variations possible.
2. Particularly with low line - light load conditions where the current ramp slope is too shallow for stable PWM operation.
3. High power and/or noisy applications where noise on the current waveform would be difficult to control.
4. Multiple output voltages are needed with relatively good cross-regulation.
5. Saturable reactor controllers are to be used as auxiliary secondary-side regulators.
6. Applications where the complexities of dual feedback loops and/or slope compensation is to be avoided.

In line with these considerations, the UCC3570 has been optimized for low-to-medium power, off-line, primary-side control applications with isolated feedback. It features many performance enhancements for this task in addition to the control characteristics described above but, since that is not the purpose of this document, the reader is referred to the product data sheet for further information.

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Design Note

The Current-Doubler Rectifier: An Alternative Rectification Technique For Push-Pull And Bridge Converters

by Laszlo Balogh

This design note describes an alternative rectification method which offers simpler structure and better utilization of the isolation transformers in push-pull, half-bridge and bridge power stages where usually full-wave rectification is required on the secondary side of the transformers. Converters using the current-doubler rectifier can achieve lower and better distributed power dissipation and smaller size in the magnetic components.

The common property of the push-pull, half-bridge and bridge topologies which makes the full-wave rectification necessary is that they utilize bipolar voltage across the secondary side of the transformer.

Figure 1 illustrates the commonly used circuit arrangement for full-wave rectification. For proper operation the secondary winding has to be center-tapped with one terminal connected to the reference potential (ground) of the circuit. The center-tapping splits the secondary winding into two inductors which are coupled strongly but not perfectly within one magnetic structure.

This design note assumes a full-bridge power converter using the phase-shifted control method. Consequently, the primary of the isolation transformer is short circuited in the free-wheeling mode which has a profound effect on the current distribution in the secondary windings during that period. In all other aspects, the operation of the push-pull, half-bridge and the conventional full-bridge converters are identical to the description below.

Based on the polarities and signal names of Figure 1, operation is as follows:

During the first active period when energy is transferred from the primary to the secondary side, the voltage across TR1 is positive. D1 is forward biased while the negative voltage appearing across TR2 keeps D2 reverse biased. The current of the output inductor, LO, is forced to flow through TR1 while TR2 carries no current. During the free-wheeling period, the voltages across TR1 and TR2 become zero. In theory the output current is evenly distributed between the secondary windings TR1 and TR2. In practice, because of leakage inductance

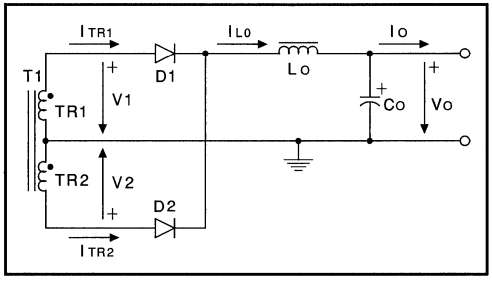

Figure 1. Full-Wave Rectifier

associated with real magnetic structures, the output current is not shared evenly. TR1 still conducts most of the output inductor current while the current slowly builds up in TR2 depending on the value of the leakage inductance and the available voltage across it. In the next active interval, V2 is positive, in which case TR2 and D2 carries all the current of LO while D1 is reverse biased by TR1 having no current through them. In the next period V1 and V2 are zero again and similarly to the previous free-wheeling period the output inductor current will keep flowing in TR2.

Figure 2 shows the most important waveforms of operation.

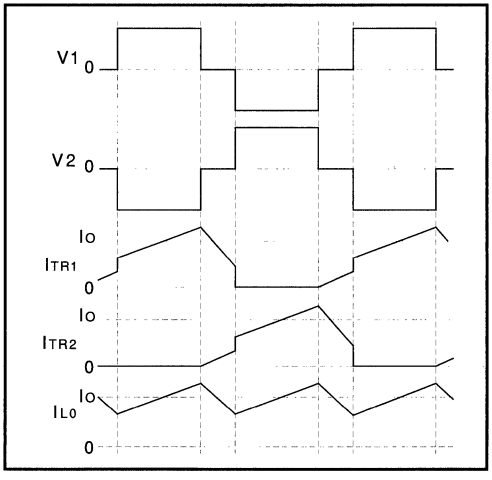

Figure 2. Waveforms of the Full-Wave Rectifier

The proposed current-doubler rectifier is presented in Figure 3. It is composed of the secondary winding of the isolation transformer which is not center-tapped now, the same two rectifier diodes, two individual but identical filter inductors and an equal output capacitor to the one of the full-wave rectifier circuit.

Using the symbols and signal polarities introduced in Figure 3 the operation of the rectifier is described below:

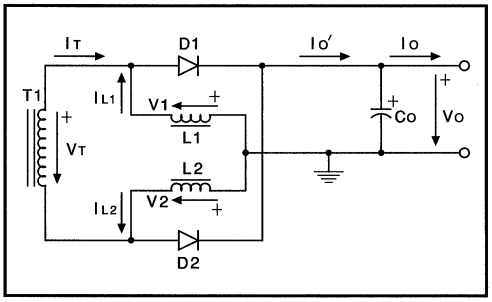

Figure 3. Current-Doubler Rectifier

Starting at the first active period the voltage across the secondary winding of the transformer, V_T is positive. Current flows in positive direction in both filter inductors, L1 and L2. During this period D1 is forward biased while D2 is kept off by V_T. It means that the current path for L1 runs through D1 and the output capacitor, basically kept away from the secondary winding of the transformer. The current of the second filter inductor L2 flows through the transformer winding and D1, closing the loop through the output capacitor. Hence the output current is the sum of the DC components of the two filter inductor currents, the transformer sees only half of the load current during the active time interval. During this time, the voltage across L1 is negative and equals the output voltage causing the current in L1 to decrease. On the other hand, V2 across L2 is positive, causing the current in L2 to increase. The active period is followed by a free-wheeling interval. V_T is not forced across the secondary winding of the transformer any longer. The voltage across L2 becomes negative, and equal to the output voltage amplitude, producing a negative slope in the current through L2. As in the full-wave case, theory would suggest that the current of L2 goes through D2 instead of the transformer winding, but in practice this current will continue, due to flow in the transformers secondary. The conditions for L1 do not change. At the beginning of the consecutive active interval, a negative voltage appears on the output of the transformer. D1 turns off while D2 is forward biased. The current rapidly changes direction in the transformer winding, and is equal to the current of L1. The current of L2 is not flowing through the transformer any longer and keeps decreasing by the rate determined by the inductance value and the output voltage. Having a positive voltage across L1, the current starts building up in the inductor. The full operating cycle is completed by another free-wheeling period when V_T becomes zero, $-V_O$ appears on L1 causing its current to decrease and there is no change in the condition of L2.

The essential waveforms of the current-doubler rectifier are indicated in Figure 4.

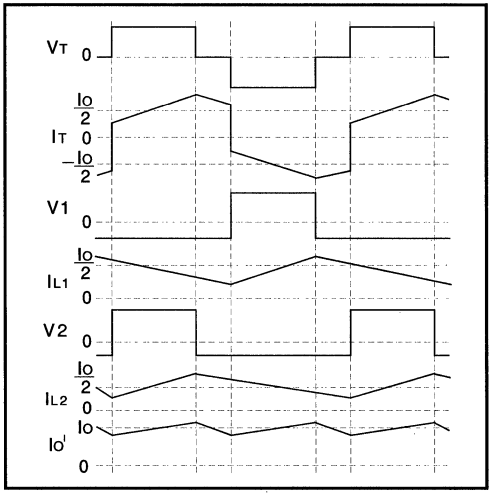

Figure 4. Waveforms of the Current Doubler Rectifier

Summarizing the most important properties of the current-doubler rectifier as revealed by the circuit diagram, the description of operation and the different waveforms, the following conclusions can be drawn:

- there is no need for center-tapping
- finer steps in turns ratio are possible
- transformer structure is simpler
- transformer carries approximately half of the output current (only the secondary winding)
- operation on the primary side, including duty-cycle is unchanged

- diode and output capacitor stresses are identical to the full-wave technique
- additional filter inductor required
- each filter inductor carries only half of the DC output current
- ripple currents cancel on common output capacitor
- requires current-mode control to ensure equal currents in the filter inductors

In order to correctly judge the merit of this rectification technique for practical applications, a quantitative comparison is presented. Assume, that two converters operate with a clock frequency of fs, have the same input and output voltages, equal load currents and equal ripple currents in the output capacitors. For these cases, the most important design parameters are given in an easy to use form in Table 1. For simplicity, the current values are not reflecting the effect of the AC components of the inductor currents.

Table 1. Comparison of Full-Wave and Current-Doubler Rectifiers

Technique >	**Full-Wave**			**Current-Doubler**		
Magnetics>	**TR1**	**TR2**	**Lo**	**Tr**	**L1**	**L2**
Transformer Operating Frequency	$\frac{fs}{2}$			$\frac{fs}{2}$		
Transformer Primary Number of Turns	N			N		
Transformer Secondary Number of Turns	1	1	-	2	-	-
Transformer Secondary Current (DC average; multiplier is the duty-cycle of the secondaries)	$Io \bullet 0.5$	$Io \bullet 0.5$	-	$\frac{Io}{2} \bullet 1$	-	-
Secondary current reflected to the primary (DC average)	$Io \bullet \frac{1}{N} \bullet D$			$\frac{Io}{2} \bullet \frac{2}{N} \bullet D$		
D1; D2 Breakdown Voltage (minimum)	$V_{IN} \bullet \frac{1+1}{N}$			$V_{IN} \bullet \frac{2}{N}$		
Output Inductor Operating Frequency	-	-	fs	-	$\frac{fs}{2}$	$\frac{fs}{2}$
Output Inductor Current (DC Average)	-	-	Io	-	$\frac{Io}{2}$	$\frac{Io}{2}$
Output Inductance (minimum) ** function of duty-cycle*	-	-	Lo	-	≤Lo*	≤Lo*

Summary: the presented current-doubler rectifier provides an alternative rectification technique for converters employing push-pull, half-bridge or bridge topologies. The method simplifies the power transformer and adds one more filter inductor to the circuit. Depending on the particular application, the total volume of the two filter inductors might be equal or smaller than the choke of the full-wave rectifier due to their lower operating frequency and lower current rating.

Further trade-offs can be made in order to reduce inductor sizes by lowering the inductance value and relying more strongly on the ripple current cancellation of the two inductors. Additionally, the current-doubler rectifier offers the potential benefit of better distributed power dissipation which might become a vital benefit in densely packed power supplies. Because of its added circuit complexity, this solution could probably be justified in medium to higher power and/or high output current applications.

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Design Note

Inductorless Bias Supply Design for Synchronous Rectification and High Side Drive Applications

by Bill Andreycak

Developing a bias supply which is higher than a power supply's input voltage is usually required in high side switch applications. Two such examples are Buck regulators and Synchronous Switch converters using N-channel MOSFETs as the switching device. Independent of the specific application, there are numerous requirements for cost effective bias supplies without the added complexity of inductors, switches, transformer windings or even an independent power supply. The circuit shown in Figure 1 exemplifies the need in a transformer coupled, Synchronous Switch application in a Forward converter.

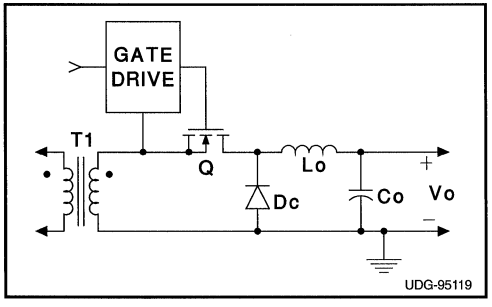

Figure 1. Synchronous Switch

A number of more demanding applications than the conventional Synchronous Switch examples exist, all with similar high side bias supply needs. For example, adding an overcurrent limit or circuit breaker function to the output will require a more sophisticated detection and gate drive circuit than the previous examples. A further extension would be the need to completely regulate the output voltage by pulse width modulating the switch. Note, however, that each of these will require the MOSFET switch to be "reversed" from that found in the Synchronous Switch example. This is necessary so that the MOSFET body diode does not always conduct while the input is greater than the output voltage. With this adaptation, its "channel" can be switched "on" to perform rectification only when required. Furthermore, this allows for the gate drive to be pulse width modulated to regulate the output voltage or to control output current. A diode, placed in series with the switch is required to prevent the MOSFET body diode from conducting when the transformer secondary voltage reverses. The basic circuit is shown in Figure 2.

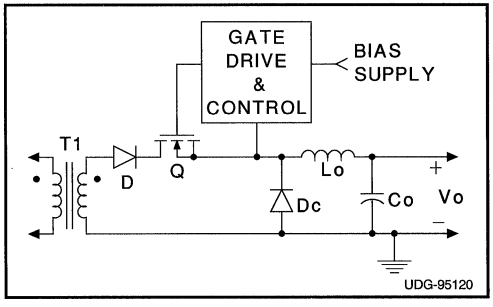

Figure 2. Controlled Switch with Series Diode

One problem with the configuration shown in Figure 2 is that the control circuit is "floating" and all control signals will require isolation which adds unnecessary complexity. An improved arrangement, shown in Figure 3, references the control circuit and gate drive to the supply's positive output rail. Note that the output filter stage consisting of the commutating diode (Dc), output filter capacitor (Co) and output inductor (Lo) has been reconfigured yet performs the same task. For simplicity, the output inductor has been moved to the lower (return) rail for two reasons. First, it enables the gate drive and control circuitry to be solidly referenced to the positive output voltage. Secondly, it eliminates the need for a "floating" gate drive which would have been required if the inductor were left in the positive output rail. Additional noise immunity in the control logic is generally gained with this configuration since its

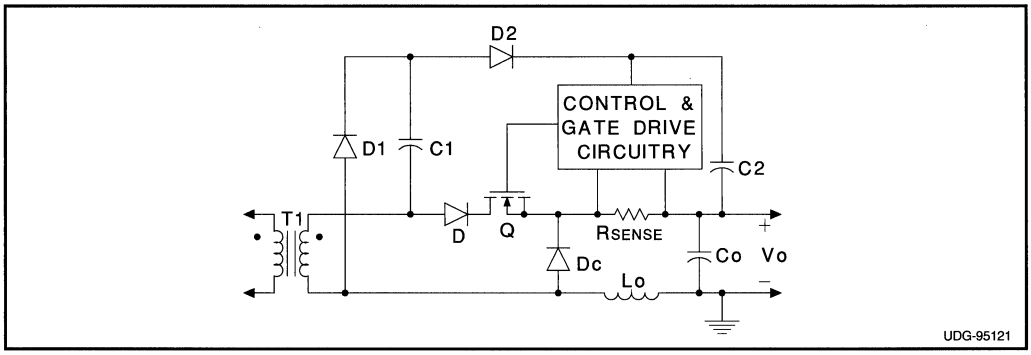

Figure 3. Improved Circuit Configuration

common mode range is reduced. Note that a direct measurement of output current is also available for overcurrent protection purposes or current mode control by using a sense resistor in series with the positive output.

Operation of the basic charge pump circuitry used to develop the high side bias is as follows. The sequence begins at turn-off of the main power supply switch on the transformer's primary side which causes the secondary voltage waveform to collapse. Power is transferred to the bias supply during the transformer's resetting or "backstroke". As the voltage across the secondary winding reverses, capacitor C1 is charged through diode D1 to the peak amplitude of the secondary reset voltage. Note that these components are "isolated" from the bias supply capacitor (C2) by diode D2 while C1 swings below the positive output rail and charges. During the normal transfer of power to the output stage the secondary transformer voltage is positive. As this occurs, Diode D1 is reversed biased and turns off while capacitor C1 is lifted along with the positive secondary transformer voltage. When the voltage across capacitor C1 exceeds that across the bias supply capacitor (C2), diode D2 conducts. Note that this takes place whether or not the power switch and diode are conducting. Charge stored in C1 is delivered to C2 beginning with the rise of secondary transformer voltage, replenishing C2. Eventually, diode D2 will discontinue conducting as C1's voltage drops below that of C2. The entire cycle is repeated beginning at the reset of T1 when the secondary voltage goes negative, starting the charge of C1 again. One noteworthy additional benefit of this circuit is that it may snub some of the parasitic energy across the transformer during its transient reset which can reduce the peak reverse voltage of the output (power) diode.

In center tapped transformer secondary applications, for example push-pull, half and full bridge topologies, the circuit can be replicated to accommodate the second high side switch and drive circuitry, as shown in Figure 4. This arrangement will provide power to the bias supply from both windings of the secondary. At first glance, the lower side circuitry may seem unnecessary, or even wrong. But when the time comes for it to transfer power to the output, this lower side becomes the upper side of the schematic and the need for it becomes apparent.

Many other arrangements of the basic diode and capacitor charge pump circuit are possible - without using inductors and/or additional switches for these low power applications. For more demanding ones, a linear or switchmode integrated circuit regulator can be considered to deliver a precisely regulated bias voltage.

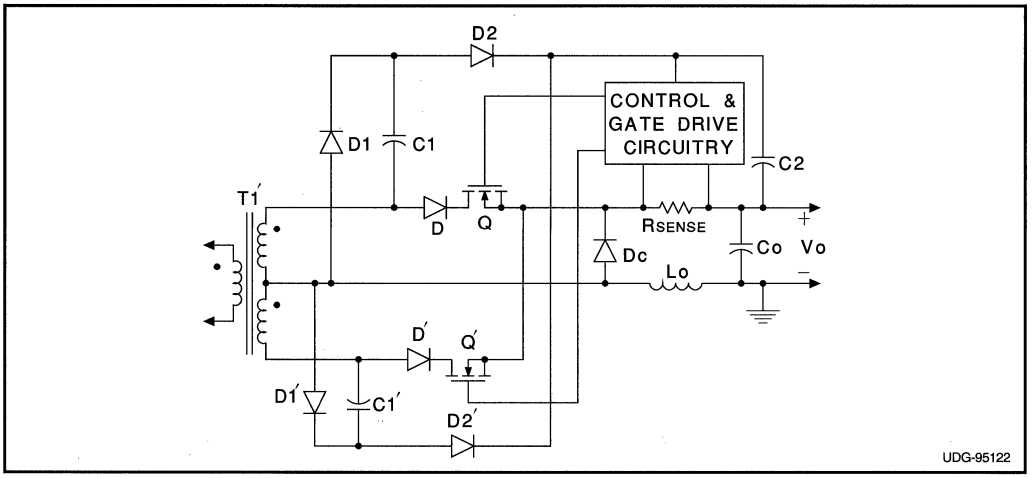

Figure 4. Center Tapped Application of Improved Circuitry

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Considerations in Powering BiCMOS ICs

by Jack Palczynski

Bipolar linear integrated circuits have been with us for years in the form of PWM and PFC controllers, supervisory circuits and others. Since these devices have traditionally been built using relatively high voltage (35V) Bipolar processes, powering considerations were typically never a concern. In addition, many of these ICs contained high current protection zeners to keep higher voltages from damaging the device. With a number of new BiCMOS ICs now replacing traditional Bipolars, more consideration needs to be given to powering these low voltage controllers. This Design Note will provide more details regarding the device specifications and help simplify the powering and use of these energy saving devices.

The most prolific of PWM ICs are those of the UC3842 family which are easy to use and to power. The V_{CC} supply can be as high as 34V and an on-chip zener can sink up to 30mA of current. It consumes significantly more power in comparison to the replacement series of Unitrode UCC3802 BiCMOS PWMs. Requiring only about 10% of the current used by the UC3842, these BiCMOS parts are a logical replacement for previous UC3842 based designs. The tradeoff is that the maximum voltage is 13.5V. With these specifications in mind, several power methodologies will be described.

Upon first review of the UCC3802 data sheet, several seemingly contradictory specifications could be noted. The UVLO start threshold has a range of 11.5V to 13.5V, while the protection zener voltage can vary from 12.0V to 15.0V. However, the absolute maximum supply voltage of the IC is specified at 12.0V. This absolute maximum is defined as the lowest possible zener voltage when driven from a low impedance (voltage) source. Note, however, that the zener voltage is always higher than the UVLO start voltage. These two parameters track each other and the chip is tested to guarantee that the zener voltage will never be below that of the start voltage.

For low cost, off-line applications, these newly introduced control ICs offer savings in overall cost and power in comparison to their predecessors. For example, the UCC3802 PWM consumes only 1mA (approximate) for full operation – which can eliminate the need for a bias supply in many instances. To this 1mA, add estimates for the other currents consumed by the control circuitry (gate drive, slope compensation, etc.). Working backwards, calculate the resistor value for the circuit of Figure 1 to deliver this current from the rectified, filtered line voltage. Typically, the AC input voltage will range from $85V_{RMS}$ to $264V_{RMS}$, or about a 3:1 ratio. The corresponding DC input will vary accordingly from 124VDC to 374VDC. Calculate R1 to provide supply current at the lowest input voltage. 3mA minimum supply current is used for this example.

$$\frac{124VDC - 12VDC}{3mA} = 37.3k\Omega \text{ (use 36k).}$$

At high line, this current will increase to

$$\frac{374VDC - 12VDC}{36k} = 10.1mA$$

and dissipate more power. The resistor will guarantee that the ICs zener clamp will not be subjected to overcurrent since it shunts only 7.1mA, the other 3mA are consumed for operation. This configuration is generally referred to as a "current source" power supply. Before the IC starts, it only draws 100µA and C1 is charged with nearly the full supply current. Once C1 reaches the UVLO start threshold of about 13.5V, the UC3802 starts and then uses 1mA for itself, and an additional 2mA (this example) to power the gate drive and other functions.

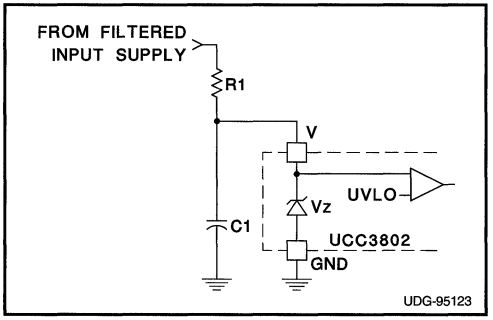

Figure 1. Off-line Current Source Power

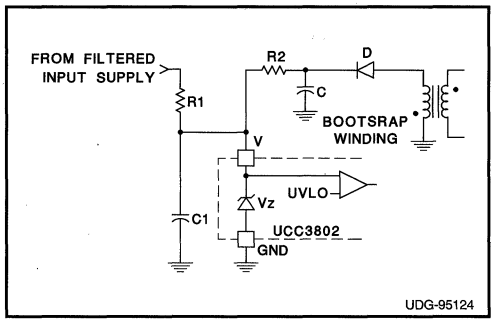

Figure 2. Adding a Bootstrap Supply

A drawback to the above circuit is that a good percentage of power is dissipated in R1. If the input voltage range is very wide, or if a high frequency is used or a FET with high gate charge is used, it may not be possible to guarantee that the zener current is limited to 30mA at high line while still being able to provide enough current to run at low line. To create a more efficient input supply, a few alternatives are demonstrated. Figure 2 shows a typical bias supply with modifications for the BiCMOS IC. R1 limits current while the IC is in standby mode so that zener current is not exceeded as in the last example. In this case, the resistor may be made much larger since it will not be the major power source once the supply has started. Resistor R2 is placed in series with the bias supply coming from the transformer in order to again limit the zener current to 10mA. This circuit will result in a higher efficiency than that of the first - at the cost of additional components and a bias winding on the transformer. During start up, C1 again charges through R1 until the turn on threshold of the IC is reached. If R1 is very large, then the UVLO hysteresis of the UCC3802 allows the controller to continue running until it reaches its lower threshold. During this time, the bias supply starts supplying current and should take over as the primary IC power supply before the lower UVLO threshold is reached.

A third solution is to use the Unitrode UCC3889 bias supply control circuitry as seen in Figure 3. This patented control technology will provide a fully regulated supply from a high input voltage without the use of transformers. As with the last circuit, a series resistor from an 18V input to Vcc

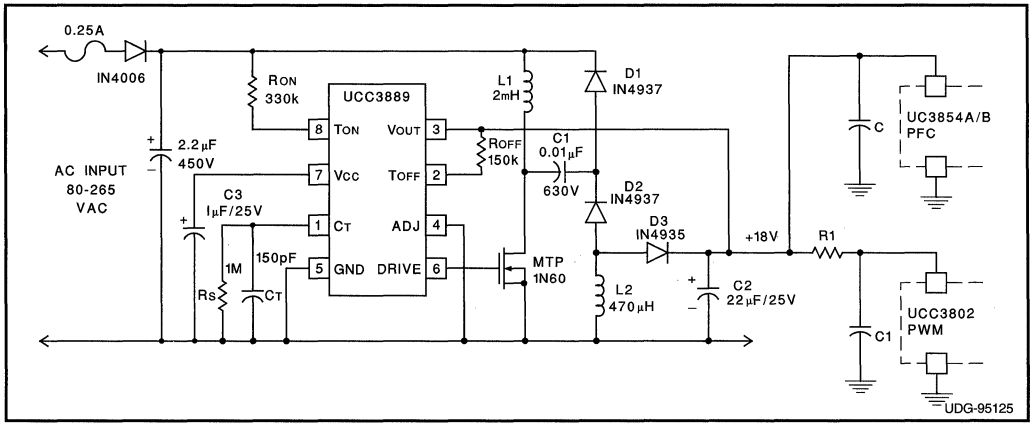

Figure 3. UCC3889 Powers Other Circuits

will limit current. With the UCC3889 IC, an input Power Factor Correction IC or other primary side PWM circuit may also be easily powered.

The UCC3802 and the entire family of Unitrode BiCMOS integrated circuits can provide added efficiency, higher speed, FET totempole output drivers (which eliminate the need for protection Schottky diodes) and other added features. With some care, input power can easily be designed to meet the ICs power requirements, and assist in designing new, more efficient switching power supplies.

References:

[1] W. Andreycak, "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Applications Note U-132.

[2] J. Palczynski, "UCC3806 BiCMOS Current Mode Control IC" Unitrode Applications Note U-144

[3] W. Andreycak, "Elegantly Simple Off-Line Bias Supply for Very Low Power Applications" Unitrode Applications Note U-149

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UC3573 Buck Regulator PWM Control IC

Typical Application Circuit for +12VDC Input to +5VDC/1A Output
Also : Demonstration Kit Circuit Schematic and List of Materials

by Chuck Melchin and Bill Andreycak

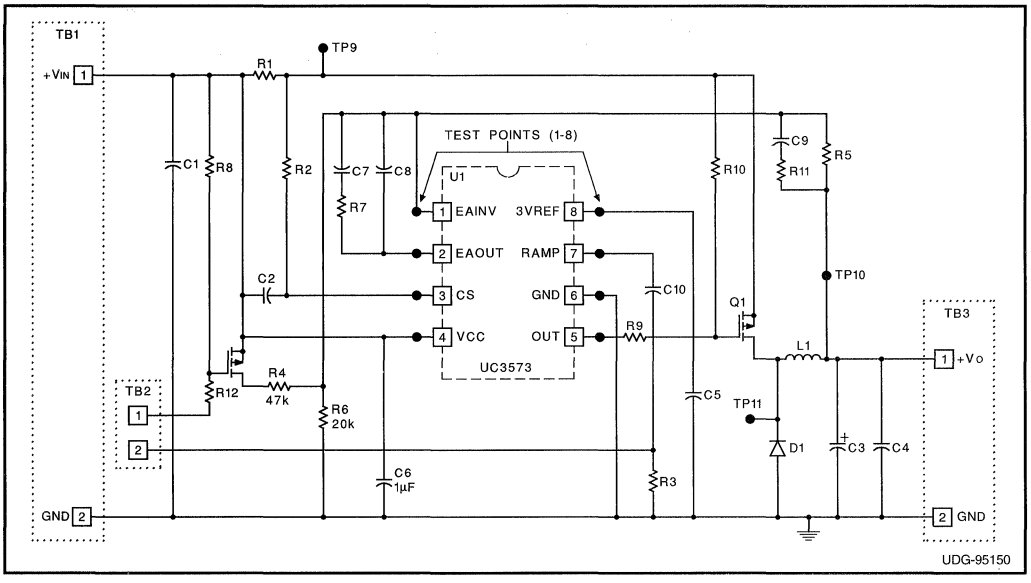

Figure 1. UC3573 Application Circuit Schematic

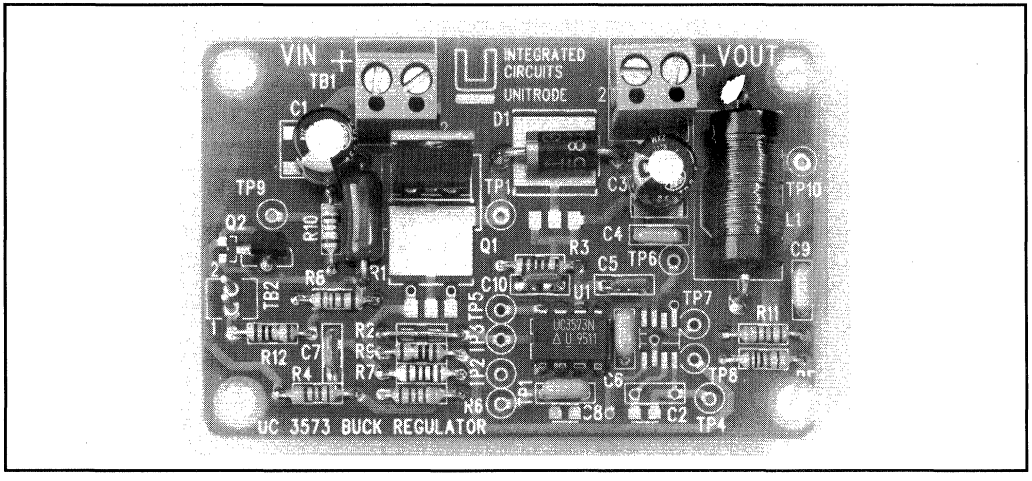

Figure 2. Photo of UC3573 Demo Kit

List of Materials:

Reference	Value and Type
C1,C3	CAP 82µF/25V Electrolytic, ESR < 0.25Ω@100kHz (Panasonic HFQ or FA series)
C2	Not Used - Open Circuit
C4,C5	CAP 0.1µF/50V Ceramic
C6	CAP 0.47µF/50V Ceramic
C7	CAP 2.2nF/50V Ceramic NPO Type
C8	CAP 27pF/50V Ceramic NPO Type
C9	CAP 1.8nF/50V Ceramic
C10	CAP 680pF/50V Ceramic
D1	1N5820 3A/20V Schottky Diode
H1*	Heatsink for Q1
L1	220µH/2A : Coilcraft PCH-45 Series
Q1	IRF9Z30 P-Channel Power MOSFET, –50V, 0.2Ω RDS(on)
Q2	BS250P P-Channel Signal MOSFET, –45V, 100 ohm RDS(on)
R1	0.27Ω/1 Watt
R2	Short Circuit - Use AWG#22 Wire
R3, R9	20Ω, 1/4W
R4	47k, 1/4W
R5	47k, 1/4W, 1%
R6	20k, 1/4W, 1%
R7	130k, 1/4W
R8, R10	100k, 1/4W
R11	7.5k, 1/4W
R12	200k 1/4W
TB1, TB3	Terminal Block
U1	UC3573 PWM

* = Optional

Test Equipment needed:

Power supply +12VDC/2A max.
Adjustable load for 5VDC/2A max.
Digital Multimeter 100Ω, 1 Watt load resistor Oscilloscope.

Testing Procedure

1. Before applying power to the UC3573 Demo Kit, connect A 100Ω preload resistor across the UC3573 output terminals at TB3. This places a minimum load of 50 milliamps on the +5VDC output of the converter to keep the Buck regulator inductor current continuous. Also connect the adjustable electronic or resistive load across the same output terminals. Set the load to draw no current and observe correct ± polarity when using an electronic load. Pin 1 of TB3 is the positive output (+) and pin 2 is the negative (-) terminal, or ground. Also connect the digital multimeter to the output terminals to measure the output voltage.
2. Connect the 12VDC/2A power supply to the UC3573 Demo Kit input terminal block observing the correct polarity. Pin 1 of TB1 is the positive input (+12VDC) and pin 2 is the return connection (-) and ground.
3. The oscilloscope and digital multimeter can be used to observe and measure signals at numerous nodes in the Buck converter. Test points TP1 through TP8 correspond directly to the respective pins of the UC3573 IC; ie. TP1 is the voltage at the UC3573's pin 1 with respect to ground. The various waveforms and amplitudes of the IC pins can be monitored over the operating ranges of input voltage and output current. Test points TP9 through TP11 are for further probing of the power stage.
4. Once all of the connections to the UC3573 demo kit have been verified, the +12VDC input can be applied. The output voltage of the Demo Kit should be approximately 5.0 VDC (4.8 to 5.2 VDC worst case) initially. Note that 1% tolerance resistors are used in the voltage divider network to the IC's error amplifier and the IC's internal reference voltage (Pin 8) has an initial tolerance of ±2%.
5. Gradually increase the load on the UC3573 Demo Kit output until the output voltage decreases to 4.5VDC or lower. Load current will be limited to approximately 1.3ADC, and decreasing the load resistance will only lower the output voltage, and not cause a significant increase in the converter's output current. This is a typical exhibition of the overcurrent protection feature of the IC. Each switching cycle, the pulse width output of the IC is turned off early (before the normal pulse width is reached) to reduce the input power drawn. This feature reduces the MOSFET switch power dissipation and provides protection from a short circuited or severely overloaded output condition. Once the fault has been removed, the output voltage will automat-

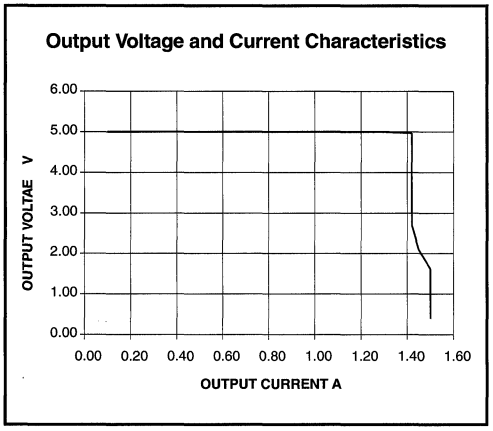

Figure 3. Converter Output Voltage Versus Current

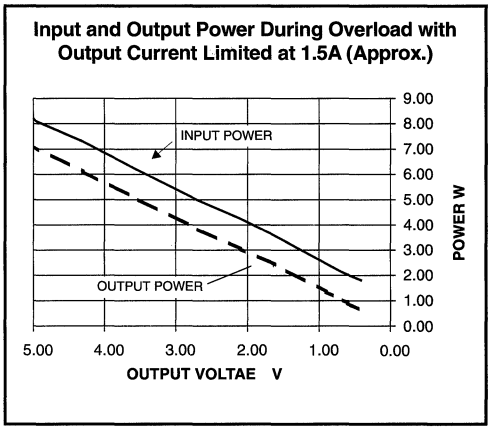

Figure 4. Converter Input and Output Power During Overload

ically return to the normal 5VDC amplitude. The exact profiles of output voltage versus output current is shown in Figure 3. and input power versus output power during overload conditions is shown in Figure 4.

Optional Features

Synchronization: Terminal block TB2 is for optional external synchronization of the UC3573 and for remote shutdown of the UC3573 Demo Kit. The required SYNC pulse input to TB2 (pin 2) is a brief pulse of approximately 1 volt amplitude. This adds to the IC's normal oscillator timing sawtooth waveform (RAMP, pin 7) to force the total waveform above the oscillator's internal upper threshold. Doing this will terminate the immediate switching cycle and initiate the next clock cycle. It is necessary that the synchronization frequency is higher than the UC3573 programmed oscillator frequency in order for this to work properly. Note that a low impedance, fairly high current drive circuit is required to force synchronization. More complete details can be found in Unitrode Application Note U-111 in the "Synchronization" section.

Remote Shutdown: The UC3573 controller can be placed into a low current (50μA typical) standby mode by forcing the error amplifier inverting input above 2.6VDC. The circuitry used to facilitate this on the Demo Kit consists of transistor Q2, resistors R4, R6 and R12. When pin 1 of terminal block TB2 is pulled low, a voltage divider to the gate of Q2 is formed between resistors R8 and R4. This drives the gate to source voltage of the P-channel MOSFET switch below its threshold causing it to turn on. Its drain voltage, connected to resistor R4 approaches that of the FET source node which is connected to the positive input voltage (+VIN). Now a voltage divider is activated between the input voltage and ground via R4 and R6 which forces the error amplifier inverting input voltage to rise above the 2.6VDC shutdown threshold, placing the device into its low current standby mode.

Other Applications

Many other voltage step down applications are addressable by the UC3573 Buck Regulator PWM Controller. Following a brief design exercise, the UC3573 Demonstration Kit can be repopulated with the exact components to evaluate other DC to DC converter designs. Consult the UC3573 Datasheet for additional information.

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Design Note

UC3584DW Secondary Side Post Regulator, Evaluation Board, Schematic, and List of Materials

By Phil Cooke

Introduction

The operation of the UC3584 Secondary Side Post Regulator can quickly be evaluated in a given system by using this separate board containing a fully functional auxiliary converter. This controller provides a semiconductor solution for regulating auxiliary outputs in transformer isolated power supplies where magnetic amplifiers (magamps) where previously used. Circuit operation is synchronized to the main power converter and is based on leading edge modulation. This technique is compatible with both primary side current-mode and voltage-mode controls employed by the main converter.

Circuit Description

As shown in Fig. 1, a buck power stage produces the regulated auxiliary output at the AUX OUT connector. The input power is provided at V_{IN} and can be connected to a variety of single and double ended buck-derived converters. One such case is shown in Fig. 2 for a push-pull converter. This power connection is made at the common cathode of the main output node just before the main filter inductor. Connection at this node affords both synchronization to the primary controller and power transfer. Note that the oscillator is set at approximately 150kHz to make synchronization to a 170kHz converter possible. To guarantee synchronization, the free running oscillator frequency should be set to less than the main frequency by adjusting R11 and C10.

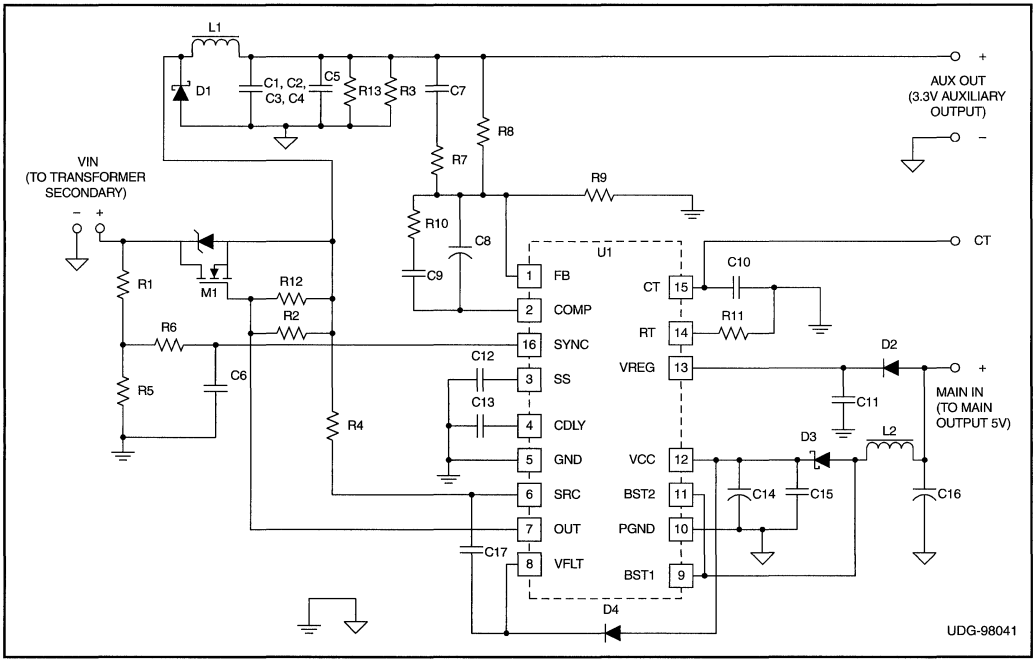

Figure 1. Evaluation board schematic.

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The auxiliary circuit is designed to interface to a 5.0V main output and its output is set to 3.3V at 10W. Other configurations are possible with minor changes to R7, C7, R8, R9, C8, C9 and R10. The surface mount design permits the use of the lowest thermal impedance package (UC3584DW) and minimizes required circuit board area. Compensation of the auxiliary circuit uses a lead-lag network providing the most flexibility for other designs. Power to the IC (U1) is generated by the boost circuit consisting primarily of L2, D3, C14 and an internal boost switch. The boost circuit can be replaced if desired, by a simple voltage doubler attached to the main transformer secondary winding.

For more complete information, pin descriptions and specifications for the UC3584DW Secondary Side Post Regulator, please refer to the UC3584, UCC3583 and the UCC3808 data sheet or contact your Unitrode Field Applications Engineer.

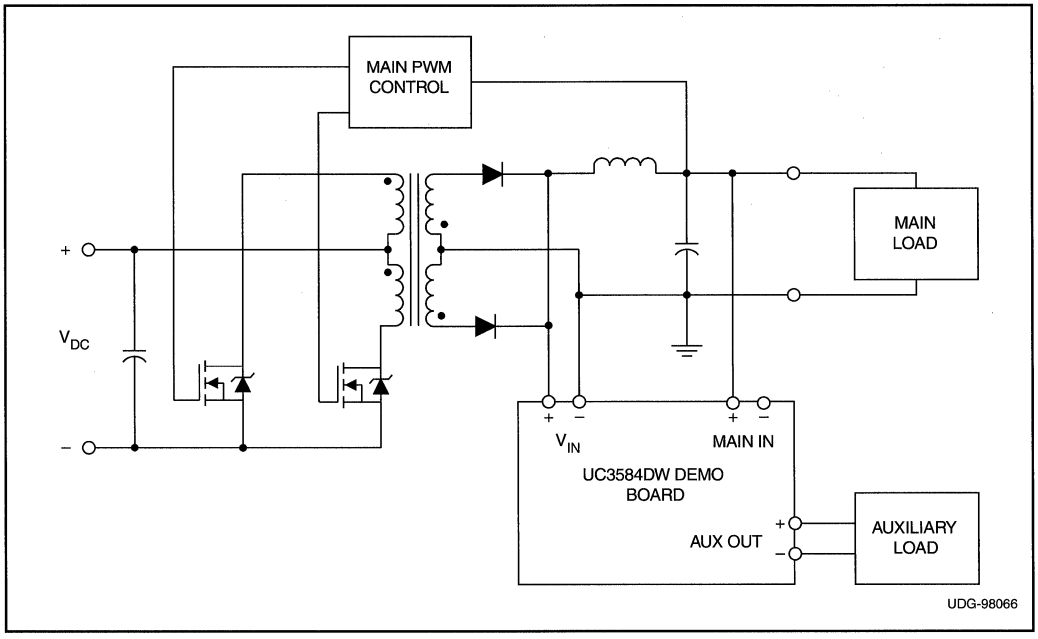

Figure 2. Connections between push-pull power stage and UC3584DW evaluation board.

Reference Designator	Description	Manufacturer	Part Number
C1, C2, C3, C4	390µF, 6.3V, R Case Code, Solid Tantalum	Sprague, Newark	595D397X06R3R2T
C5,C11, C12, C15	0.1 µF, 50V, 1206, X7R, ±10%	Xicon, Mouser	140-CC502B104K
C6	100 pF, 50V, 1206, NPO, ±5%	Xicon, Mouser	140-CC502N101J
C7	4700 pF, 50V, 1206, X7R, ±10%	Xicon, Mouser	140-CC502B472K
C8	120 pF, 50V, 1206, NPO, ±5%	Xicon, Mouser	140-CC502N121J
C9	0.01 µF, 50V, 1206, X7R, ±10%	Xicon, Mouser	140-CC502B103K
C10	220 pF, 50V, 1206, NPO, ±5%	Xicon, Mouser	140-CC502N221J
C13	1000 pF, 50V, 1206, X7R, ±10%	Xicon, Mouser	140-CC502B102K
C14	10 µF, 25V, 7343, Tantalum, ±20%	Kemet, Newark	T491D106M025AS

Table 1. Evaluation board list of materials.

Reference Designator	Description	Manufacturer	Part Number
C16	470 µF, 6V, 7343H, Tantalum, ±20%	Kemet	T510X477M006AS
C17	1.5 µF, 25V, Tantalum, ±20%	Panasonic, Digikey	ECS-H1EX155R
D1	Schottky, 10A, 45V	Central Semiconductor	CSHD10-45L
D2, D4	1N4148	Diodes Inc.	1N4148
D3	Schottky, 1.0A, 40V	IR	10BQ040
L1	33µH, 3.7A rms, 52mΩ	Coiltronics	UP4-330
L2	33µH, 2.4A rms, 98.9mΩ	Coiltronics	UP2-330
M1	MOSFET, 60V, 0.10Ω, 14A	IR	IRFR024
R1	4.75kΩ, 1206, 1/8W	Panasonic, Digikey	P4.75KFCT-ND
R2, R12	2kΩ, 1206, 1/8W	Panasonic, Digikey	P2.0KFCT-ND
R3, R13	243Ω, 1206, 1/8W	Panasonic, Digikey	P243FCT-ND
R4	3.3Ω, 1206, 1/8W	Panasonic, Digikey	P3.3RCT-ND
R5	3.57kΩ, 1206, 1/8W	Panasonic, Digikey	P3.57KFCT-ND
R6	1kΩ, 1206, 1/8W	Panasonic, Digikey	P1.0KFCT-ND
R7	13.3kΩ, 1206, 1/8W	Panasonic, Digikey	P13.3KFCT-ND
R8	68.1kΩ, 1206, 1/8W	Panasonic, Digikey	P68.1KFCT-ND
R9	57.6kΩ, 1206, 1/8W	Panasonic, Digikey	P57.6KFCT-ND
R10	17.8kΩ, 1206, 1/8W	Panasonic, Digikey	P17.8KFCT-ND
R11	15kΩ, 1206, 1/8W	Panasonic, Digikey	P15.0KFCT-ND
V_{IN}, AUX OUT, MAIN IN	Terminal Board Connectors	RDI/Mouser	506-2SV-02
COMP, CT	Test Points, SMT	Components Corp.	TP-108-02
U1	Secondary Side Synchronous Post Regulator	Unitrode	UC3584DW

Table 1. Evaluation board list of materials (continued).

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Design Note

Comparing the UC3842, UCC3802, and UCC3809 Primary Side PWM Controllers

by Lisa Dinwoodie

Introduction

Despite the fact that the UC3842 and the UCC3802 are pin for pin compatible, they are not drop in replacements for each other. Designed as the next generation '42, the UCC3809 also has differences that prevent a simple drop in substitute. Table 1 identifies the most notable features and functional differences between the three controllers. This Design Note will help the user transition from either the UC3842 or the UCC3802 to the UCC3809 in an existing design.

Figures 1, 2, and 3 all show the same basic isolated flyback converter utilizing a different primary side controller chip. Each converter uses identical component types and circuit traces. Careful attention must be paid to the components and circuit traces that are drawn with dotted lines. The dotted lines indicate unused components in that particular design and these designations would be left open. The secondary side of each figure consists of an error amplifier and voltage reference to compare the output voltage and drive an optocoupler. The primary side of each figure consists of a MOSFET switch, PWM controller IC, and supporting circuitry to perform soft start, leading edge blanking, slope compensation, and current limiting. Table 2 lists each component and the function it supports in each design.

Soft-Start and Shutdown

The UC3842 requires an external PNP, resistor, and capacitor in order to have full cycle soft start. The UCC3802 has built in soft start fixed at 1V/ms. The UCC3809 has user programmable soft start by selecting a single capacitor. The shut down circuitry is the same in all three designs except that the UCC3809 uses this circuitry to pull the SS pin low instead of pulling the COMP pin low as in the UC3842 and the UCC3802.

Bias

The BiCMOS design of the UCC3802 and the UCC3809 result in lower start up and operating currents as compared to the bipolar UC3842. As an added feature, the '09 has two versions with different under voltage lockout levels for off-line or dc to dc systems.

Table 1. Feature comparison of the three controllers.

FEATURES	UC3842	UCC3802	UCC3809
Operating Current	11mA	0.5mA	0.6mA
Undervoltage Lockout/Hysteresis	16V / 6V	12.5V / 4.2V	10V / 2V (–1 Version) 15V / 7V (– 2 Version)
Max. Frequency	500 kHz	1 MHz	1 MHz
Soft Start	External Circuit Required	Internal	User Programmable
Leading Edge Blanking	External	Internal	External
Output Drive	± 1A	± 1A	0.4A Source / 0.8A Sink
Reference Voltage	5V ± 2%	5V ± 2%	5V ± 5%
Maximum Duty Cycle Limit	Not User Programmable	Less Than 90% Not Recommended	User Programmable Up To 70%
Slope Compensation	External	External	External
Error Amplifier	Internal	Internal	External
Shut Down	External	External	External

Outputs

Only the UC3842 requires Schottky diodes from the output to ground in order to prevent the substrate from becoming negatively biased. The CMOS output stage of the UCC3802 and UCC3809 make these Schottkies unnecessary.

Oscillator

Both the UC3842 and the UCC3802 use a single resistor and capacitor to set the oscillator frequency. Both oscillators have a valley voltage of approximately zero. This is evident in Figures 1 and 2 where R_{T2} is not used (shorted) and the AC coupling capacitor in the slope compensation circuitry, C_{SC}, is also shorted. Although requiring fewer parts, setting a maximum duty cycle is difficult if not impossible. Because the UC3842 and the UCC3802 do not have trimmed discharge currents, the maximum duty cycle can only be set by trial and error on every device. The UCC3809 uses two resistors and a capacitor (and two pins) to set its oscillator frequency. The user can reliably set the maximum duty cycle by programming the positive ramp time of the oscillator through the selection of R_{T1} and C_T. Because the valley voltage of the oscillator is greater than zero, the AC coupling capacitor is required in the slope compensation circuitry of the UCC3809. The UCC3802 and the UCC3809 can be used in systems with switching frequencies as high as 1MHz, the UC3842 is limited to 500kHz operation.

Feedback

Because the flyback design shown in the figures requires isolation, an external error amplifier is used on the secondary side to sense the output voltage. The internal error amplifiers in the UC3842 and the UCC3802 are configured for unity gain and are essentially not used. The UCC3809 was designed without an internal error amplifier, greatly reducing its silicon size and cost. A single pin (FB) sums the current sense signal, the voltage feedback signal, and any added slope compensation. The UC3842 and the UCC3802 require three pins to perform these functions.

Current Sense

To reduce the effects of noise pulses on the leading edge of the current sense signal, the UC3842 and the UCC3809 designs both use an RC filter. Thanks to an internal discharging FET on the FB pin in the UCC3809, this device has better noise immunity and requires a smaller external RC filter than the UC3842. These components are not required with the UCC3802 because this chip has on-board current sense filtering that blanks out the first 100ns of the rising edge of the OUT pin.

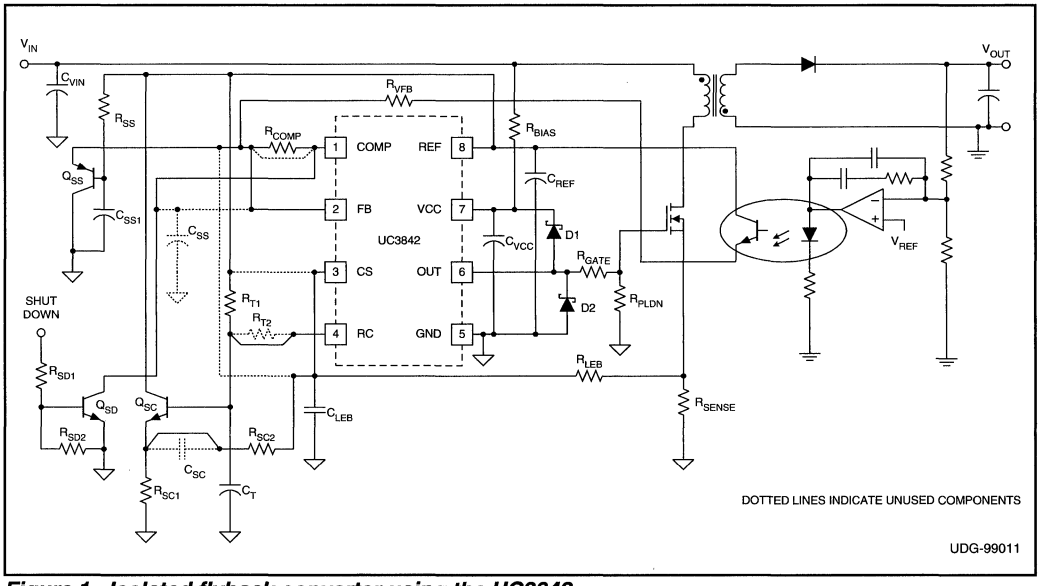

Figure 1. Isolated flyback converter using the UC3842.

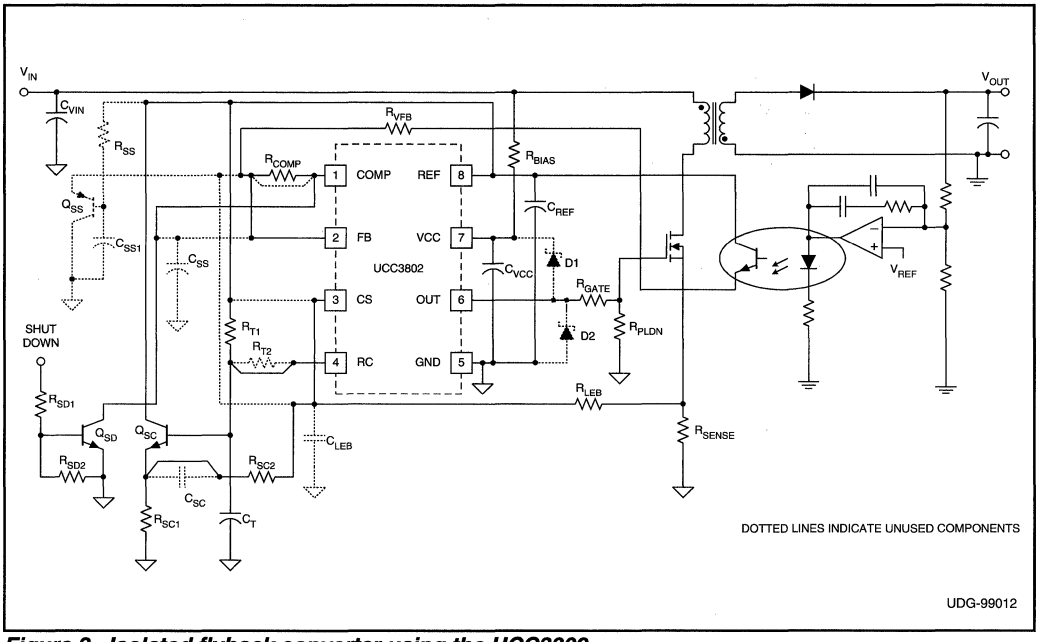

Figure 2. Isolated flyback converter using the UCC3802.

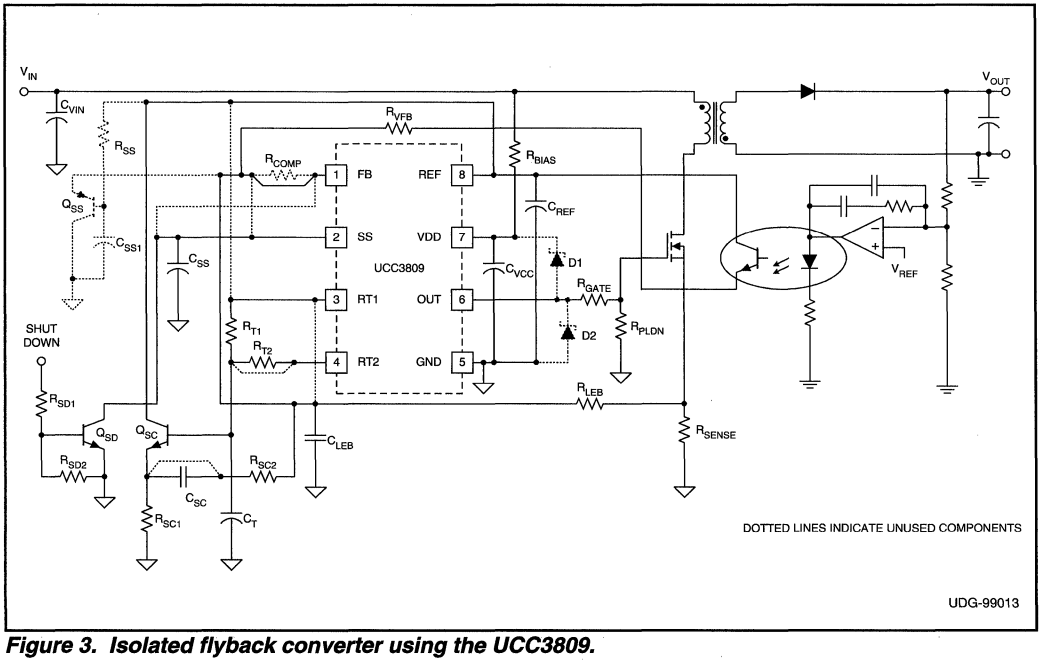

Figure 3. Isolated flyback converter using the UCC3809.

Table II. Component function and requirement comparison for Figures 1, 2, and 3.

COMPONENT	FUNCTION	UC3842	UCC3802	UCC3809
R_{BIAS}	IC Operating Current, UVLO/Hysteresis	Required	Required	Required
C_{REF}	VREF Decoupling	Required	Required	Required
C_{VCC}	Input Voltage Decoupling	Required	Required	Required
D1	Gate Drive Clamp	Required	Not Used	Not Used
D2	Gate Drive Clamp	Required	Not Used	Not Used
R_{GATE}	Gate Drive	Required	Required	Required
R_{PLDN}	Gate Drive	Required	Required	Required
R_{T1}	Oscillator	Required	Required	Required
R_{T2}	Oscillator	Not Used	Not Used	Required
C_T	Oscillator	Required	Required	Required
C_{SS}	Soft Start	Not Used	Not Used	Required
Q_{SS}	Soft Start	Required	Not Used	Not Used
C_{SS1}	Soft Start	Required	Not Used	Not Used
R_{SS}	Soft Start	Required	Not Used	Not Used
R_{LEB}	Leading Edge Blanking, Slope Compensation	Required	Required	Required
C_{LEB}	Leading Edge Blanking	Required	Not Used	Required
Q_{SC}	Slope Compensation	Required	Required	Required
R_{SC1}	Slope Compensation	Required	Required	Required
C_{SC}	Slope Compensation	Not Used	Not Used	Required
R_{SC2}	Slope Compensation	Required	Required	Required
R_{VFB}	Voltage Feedback	Required	Required	Required
R_{COMP}	Voltage Feedback	Required	Required	Not Used
Q_{SD}	Shutdown	Required	Required	Required
R_{SD1}	Shutdown	Required	Required	Required
R_{SD2}	Shutdown	Required	Required	Required
R_{SENSE}	Current Limit	Required	Required	Required

Packaging

In systems where board space and height are at a premium, the UCC3809 is the optimum choice because it is available in the new MSOP package, which is approximately two-thirds the footprint of the TSSOP package. The MSOP measures only 1mm in height as compared to 1.2mm for the TSSOP. The TSSOP is the smallest package available for the UCC3802 and the 14 pin SOIC D package is the smallest package that will accommodate the UC3842.

Summary

Although not directly a drop in replacement, existing designs utilizing the UC3842 or the UCC3802 can be easily transitioned to the UCC3809. By doing so, the user will enjoy the added benefits of programmable soft-start, maximum duty cycle clamp, smaller profile, and better noise immunity without a redundant, unused error amplifier on the primary side resulting in a more cost effective, efficient design.

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A NEW INTEGRATED CIRCUIT FOR CURRENT MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

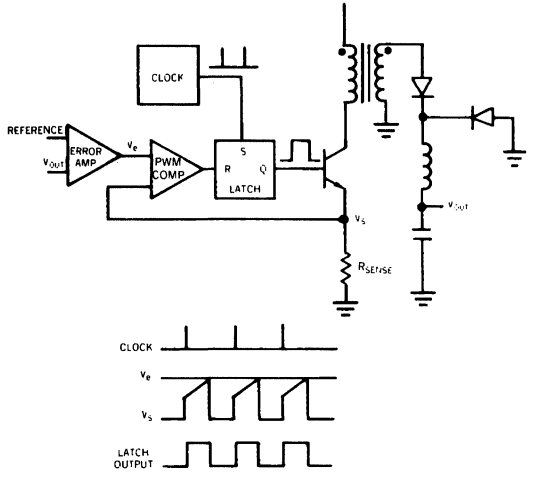


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

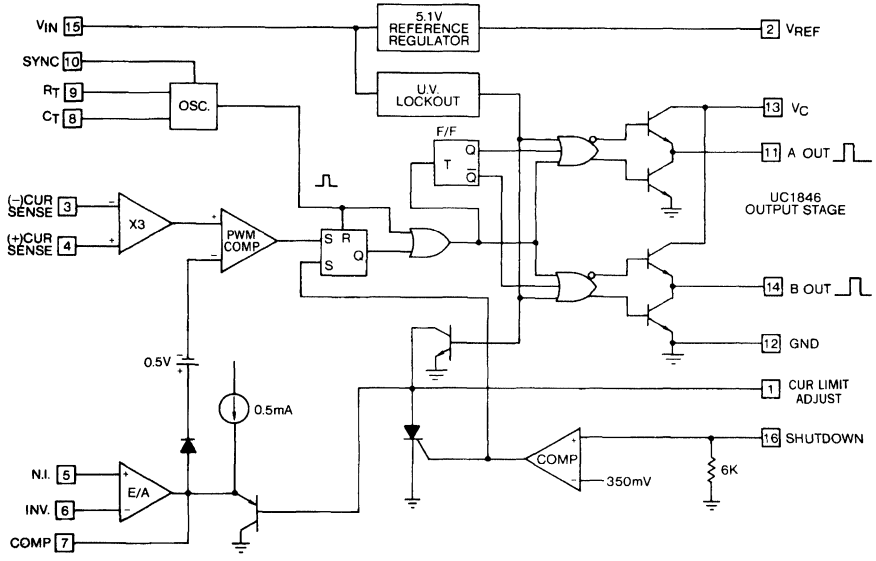


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1 MHz.
- An error amplifier with common mode range from ground to V_{cc}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

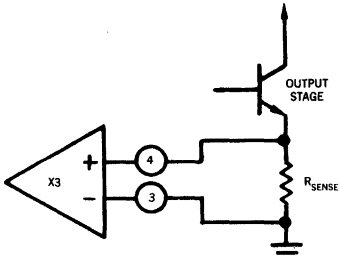
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

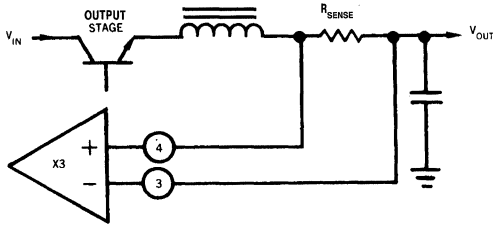
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

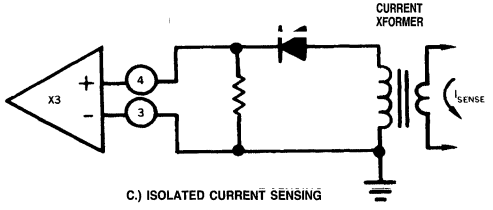
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

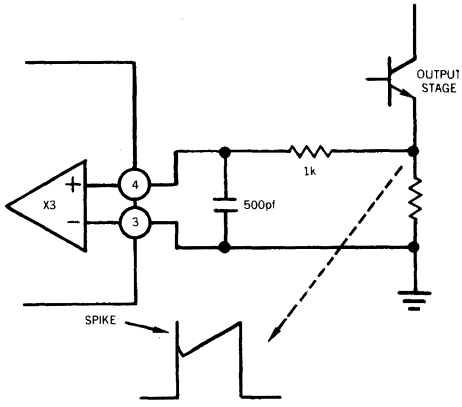


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t= 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stabillity and waveform clarity at frequencies in excess of 1MHz.

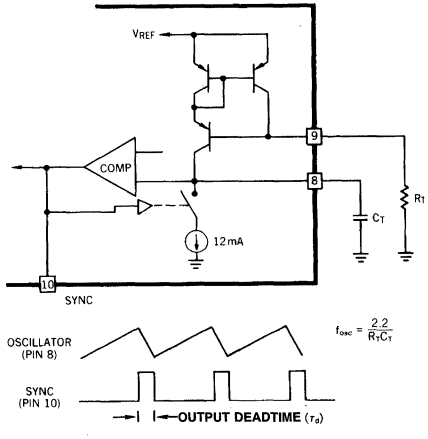


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T\ C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

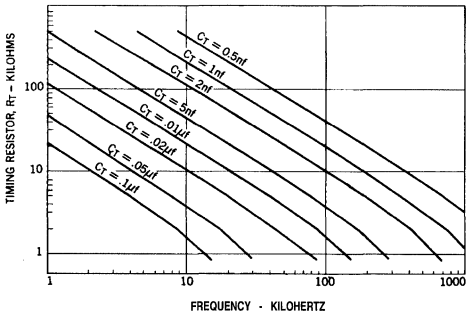


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

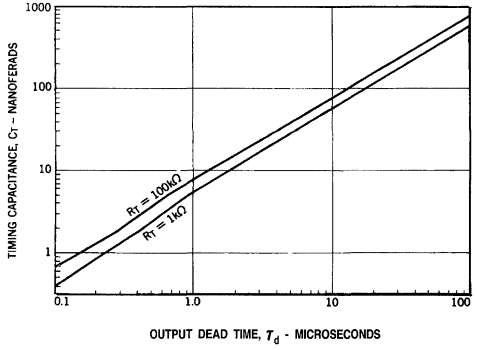


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus CT for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

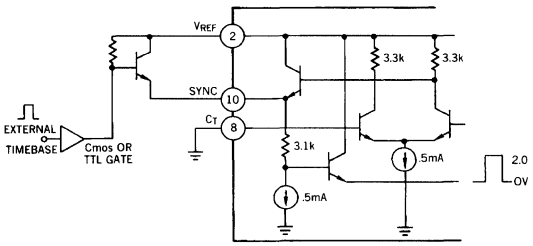


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

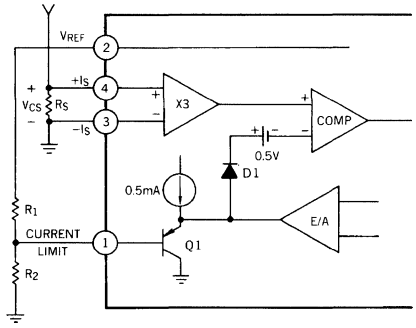


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ -0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2\,(V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

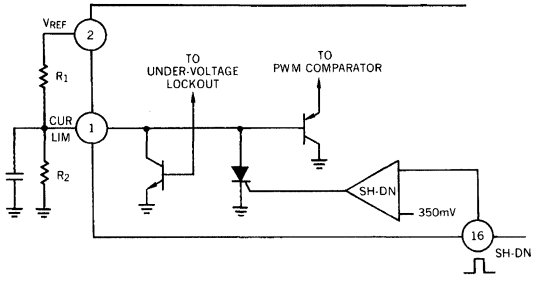


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

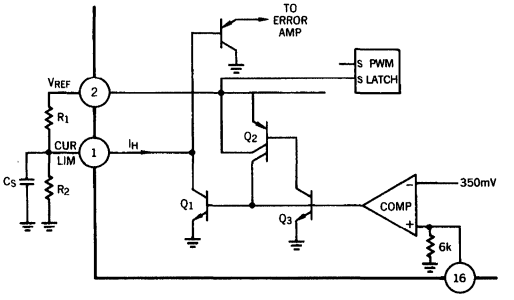


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

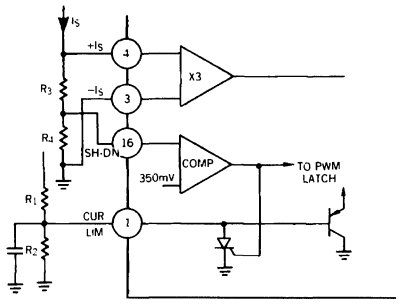


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN - SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads - such as the gates of power FETS - are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz - a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to OdB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4-8]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

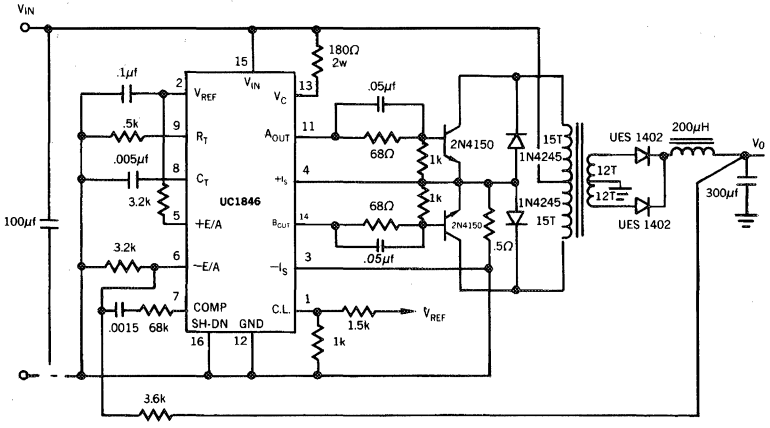
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation - important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, -E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

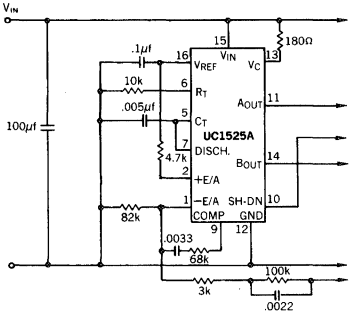
Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response - 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A - with identical output transistors - shows phase B driving the core close to saturation with 50% more current than phase A.

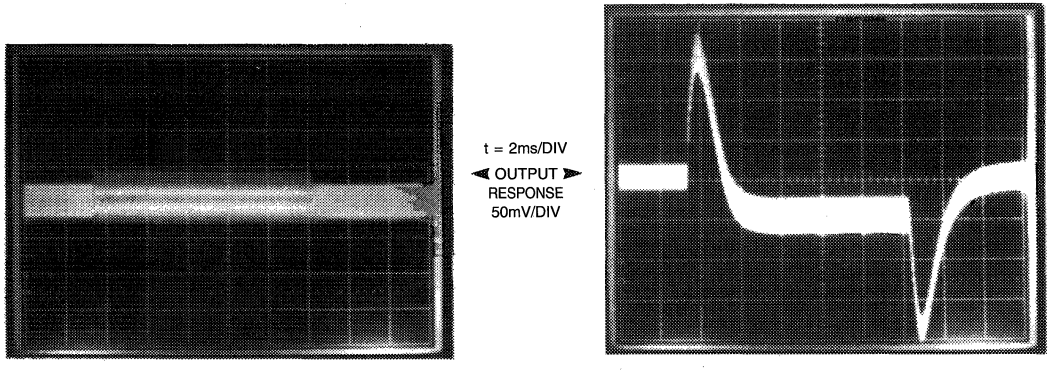


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR



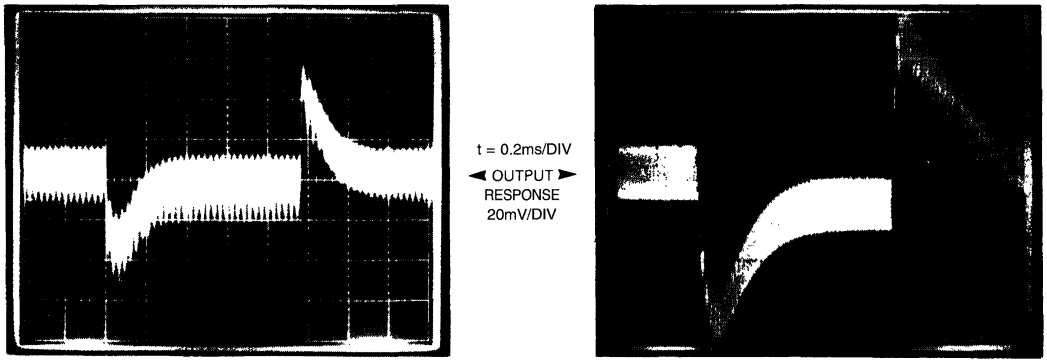
(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



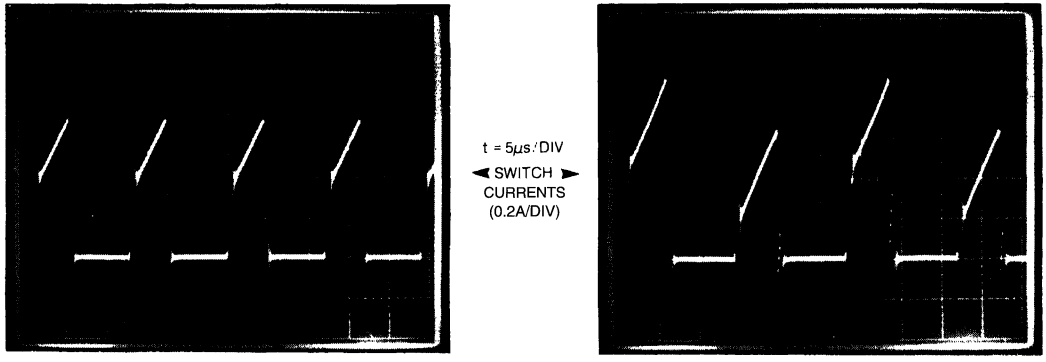
(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS



(A) (B)

FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS



(A) (B)

FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated[1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation - usually a single resistor - adds to its attractiveness. However, this introduces a new problem - that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from yet containing elements of each. Although this has been addressed in part by several authors[1,2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

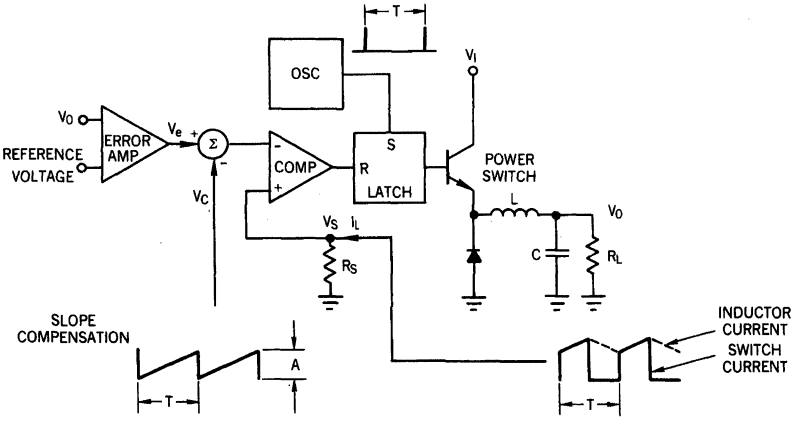


FIGURE 1 - A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in (1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle - regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

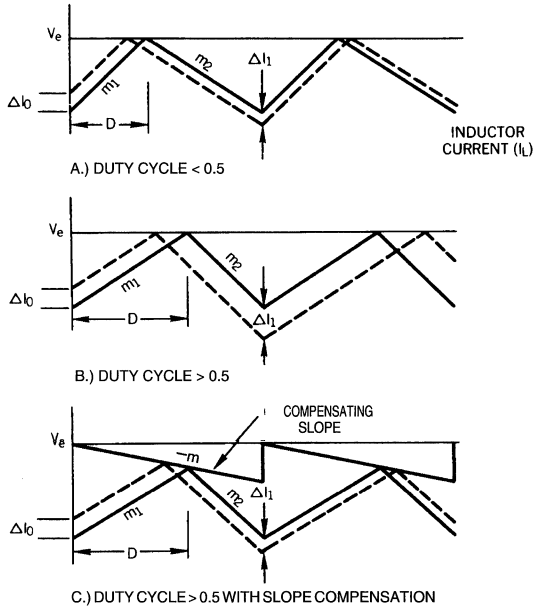


FIGURE 2 - DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for D < 0.5 (Figure 2A), and increase with time for D > 0.5 (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope -m as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

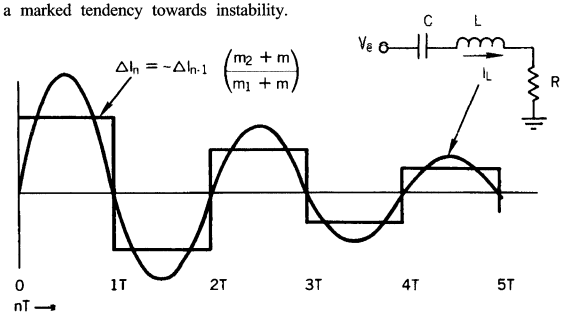


FIGURE 3 - ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

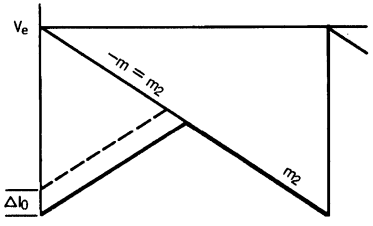


FIGURE 4 - FOR THE CASE OF m = - m2, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and - because of excess phase shift in the modulator - can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

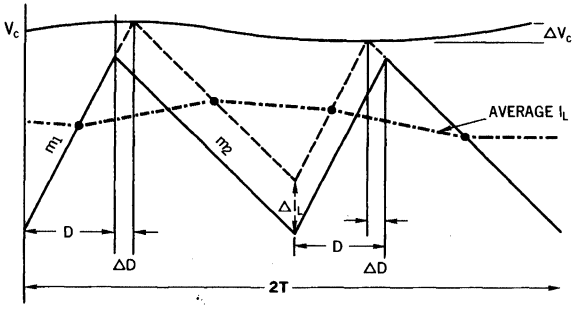


FIGURE 5- CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \quad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \quad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \quad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \quad (7)$$

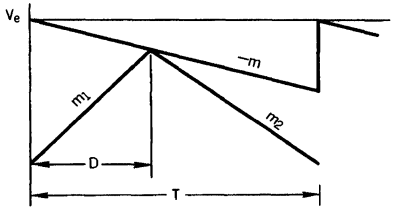


FIGURE 6- ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \quad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \quad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \quad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = \frac{1}{2} f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \quad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = \frac{1}{2} f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \quad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = \frac{1}{2} f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \quad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = \frac{1}{2} f_S$, then for the case of m = 0 (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -\frac{1}{2} m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

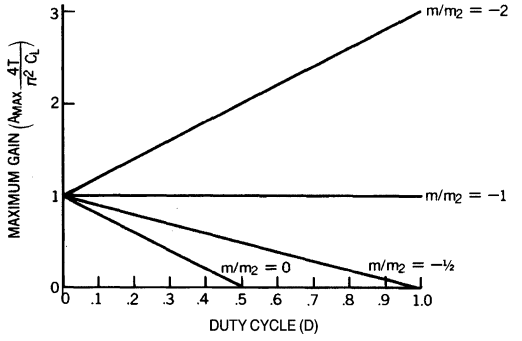


FIGURE 7 - MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase **m**, we reach a point, $m = -m_2$, where the maximum. gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage - in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output - or feedforward characteristics. If we choose to add slope compensation equal to $m = -½\ m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -½\ m_2$.

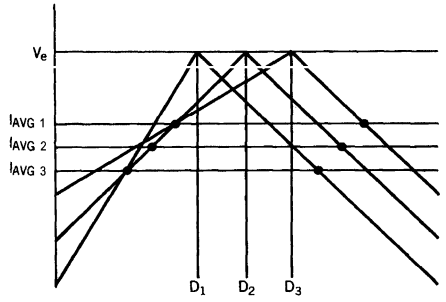


FIGURE 8 - PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

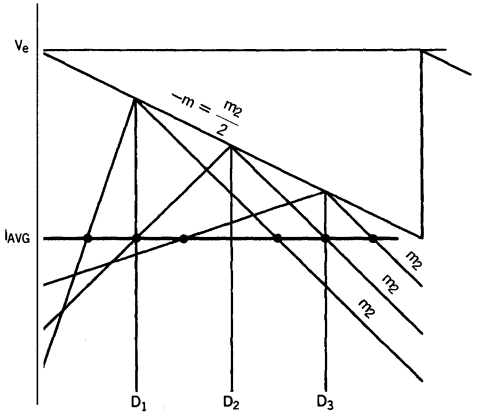


FIGURE 9 - AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUN CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -½\ m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons - reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current - not just the ripple current This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -½\ m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

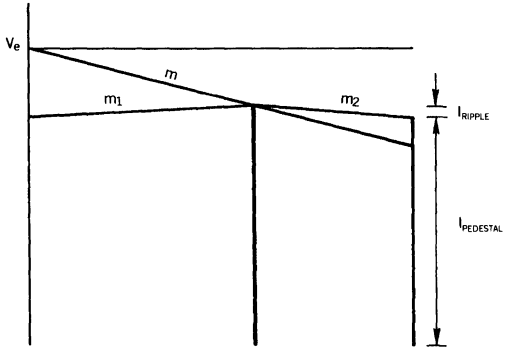


FIGURE 10 - A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11 a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

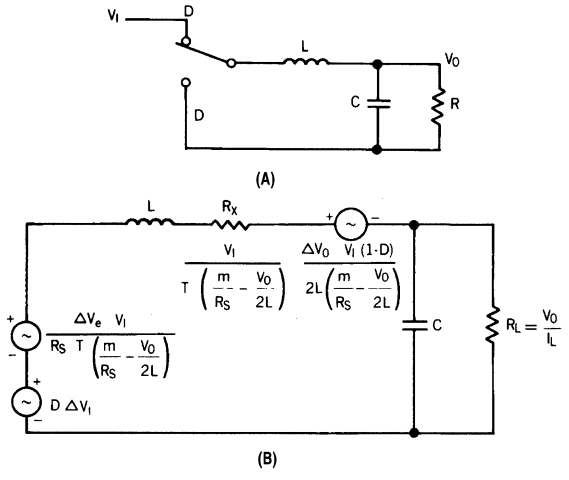


FIGURE 11- BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations - that in substitute $V_I + \Delta V_I, V_0 + \Delta V_0, D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables - and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_0}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (17)$$

A third equation - the control equation - relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\, V_0\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1-D)\,\Delta V_0 \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state space equations

(20)

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e\, V_I}{R_S\, LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0\, V_I\,(1-D)}{2L^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)}$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed In most cases, the dependent source between R_X and C can be ignored

If R_X is much greater than L, as is the case for little or no compensation (m = 0), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to L $\left(m \gg \frac{R_S V_0}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S V_0}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S V_0}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_0 = 12V
V_I = 25V
L = 200 µH
C = 300µf
T = 20µS
R = .5Ω
RL = 1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced ripple rejection slowly degrades to that of a voltage-mode converter (-6.4dB for this example).

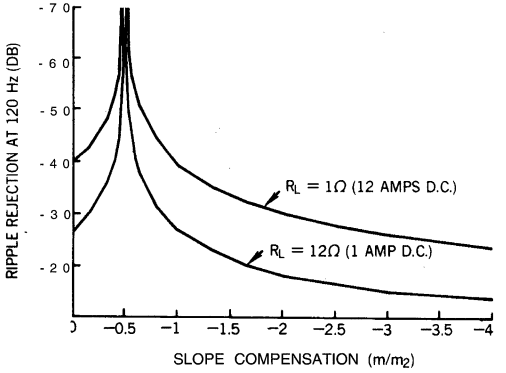


FIGURE 12 - RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used. as is the case for R_L = 1 ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}m_2$, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used. the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift

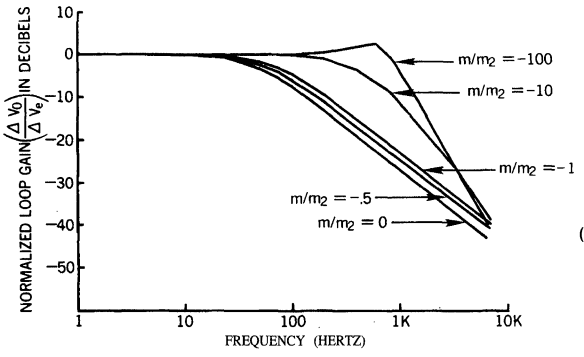
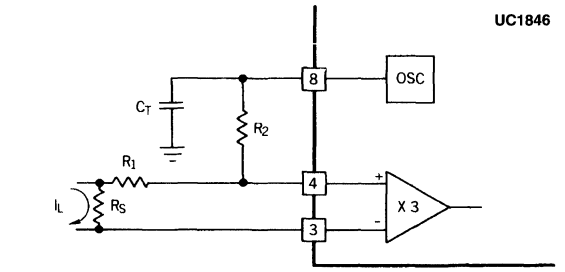
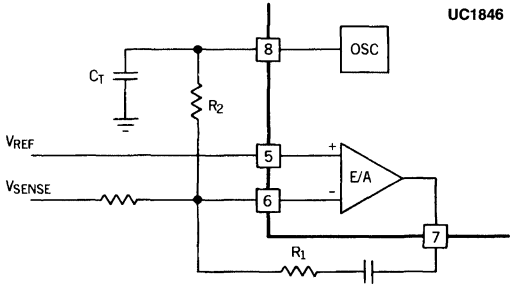


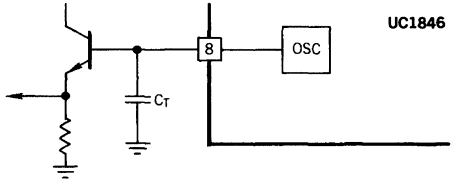
FIGURE 13 - NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 - ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

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UC3842/3/4/5 PROVIDES LOW-COST CURRENT-MODE CONTROL

INTRODUCTION

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845 Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

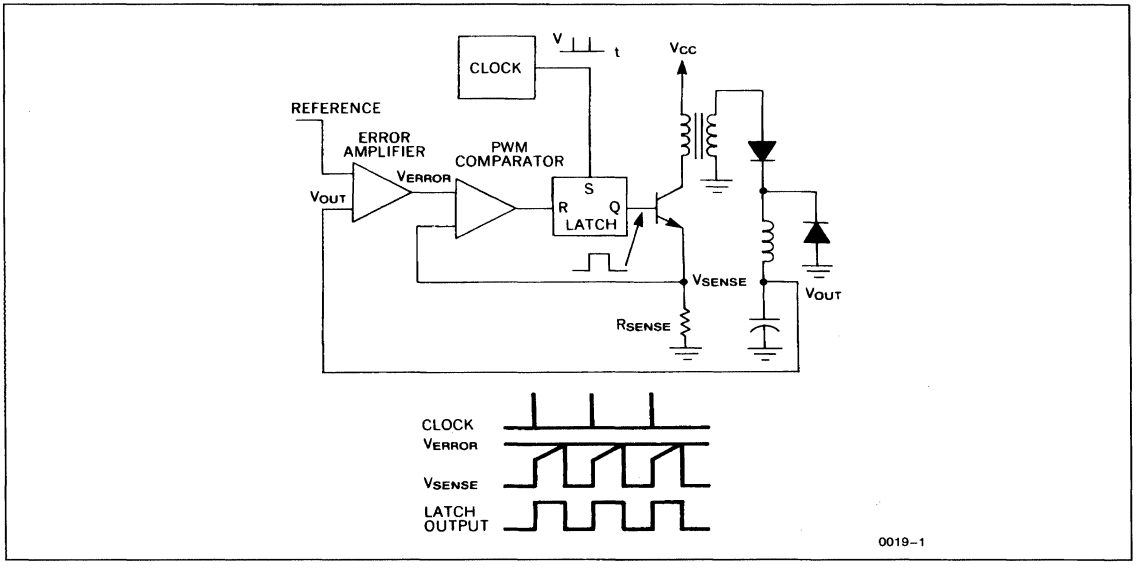


Figure 1. Two-Loop Current-Mode Control System

error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustrated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

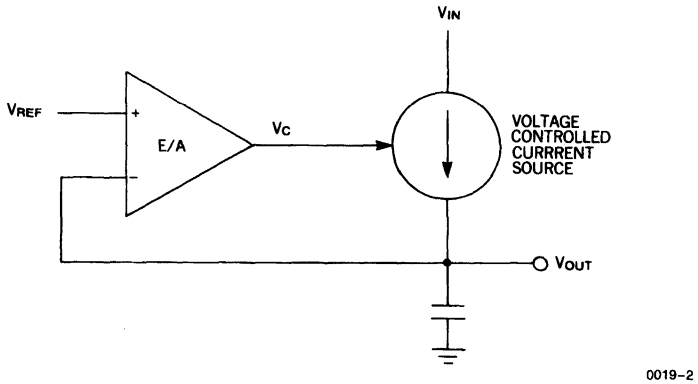
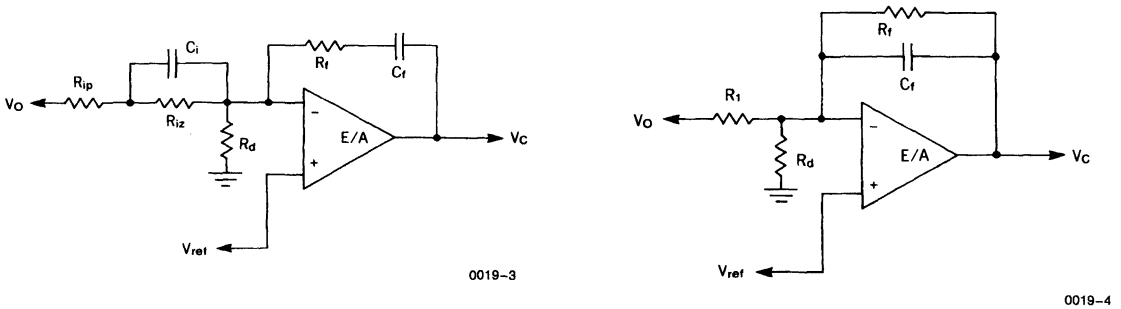


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control **B) Current Mode Control**

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

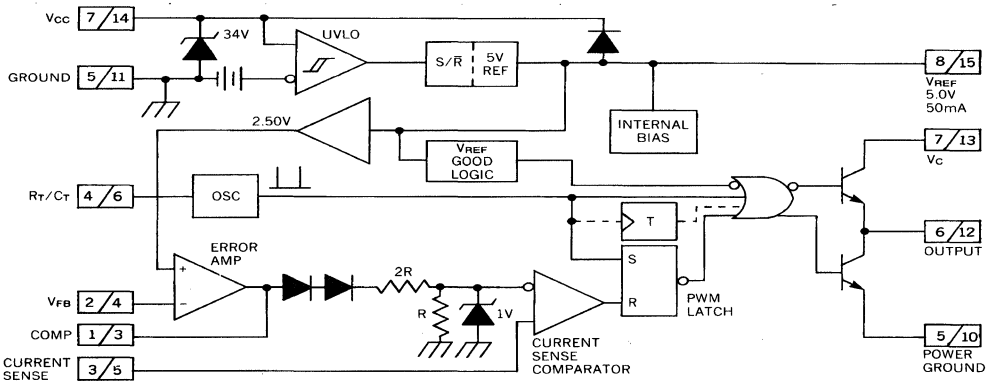
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (< 1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



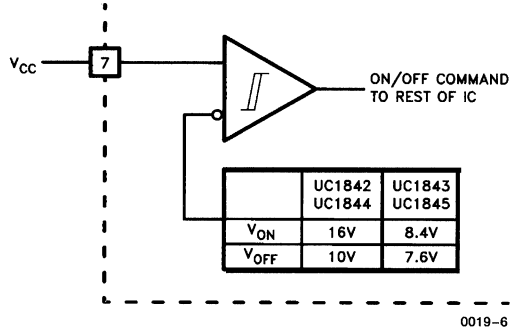
Note: 1. A/B A= DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

Figure 4

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge GIN when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.



	UC1842 UC1844	UC1843 UC1845
V_{ON}	16V	8.4V
V_{OFF}	10V	7.6V

Figure 5

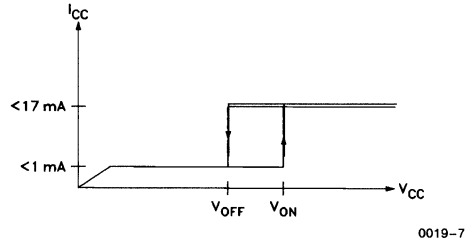


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor CT is charged from V_{REF} (5V) through the timing resistor R_T, and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of CT for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72\ /\ (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

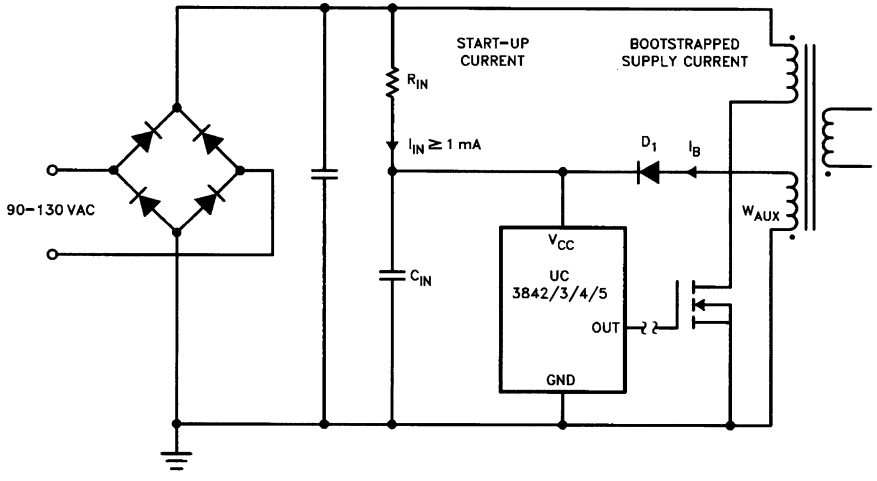


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

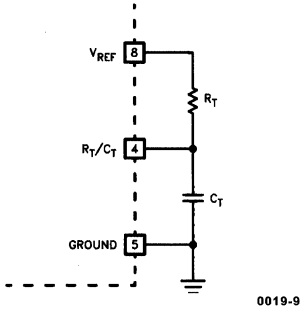


Figure 8

Deadtime vs C_T (R_T > 5k)

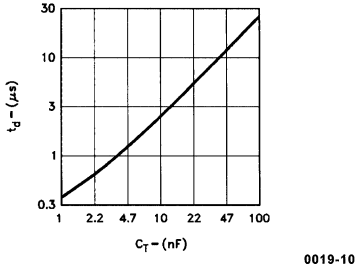


Figure 9

Timing Resistance vs Frequency

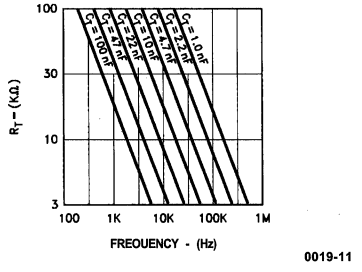


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as Figure 11 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_s}$$

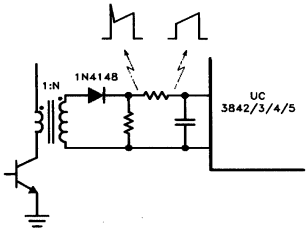


Figure 11. Transformer-Coupled Current Sensing

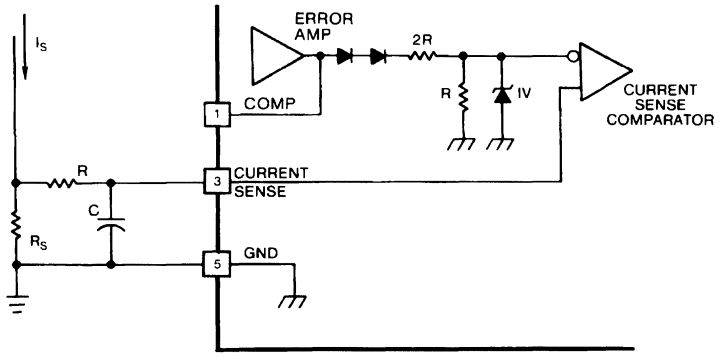


Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = 1/2\pi R_F C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

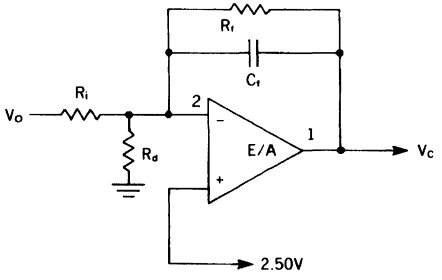


Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

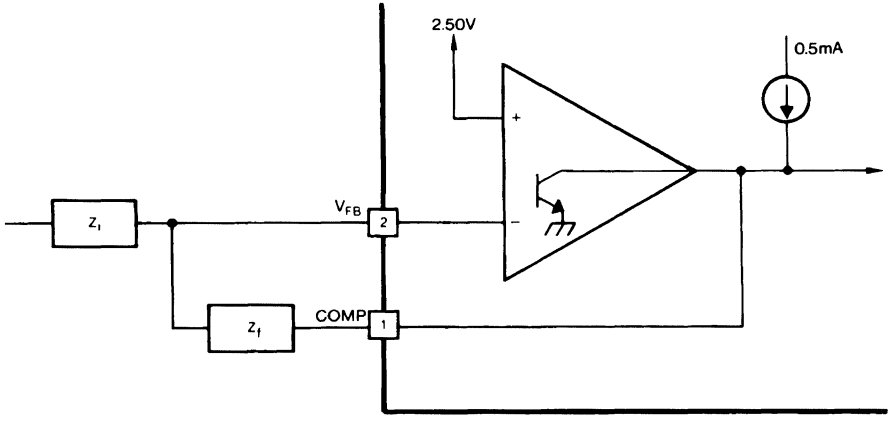


Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I, resulting in a DC error in output voltage (V_O) given by:

$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I$,

It is therefore desirable to keep the value of R_I, as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~ 10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ± 1 amp peak for driving MOSFET gates, and a + 200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most I- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

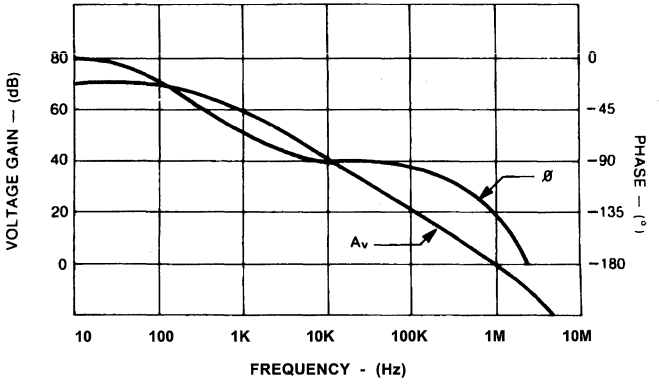


Figure 15. Error Amplifier Open-Loop Frequency Response

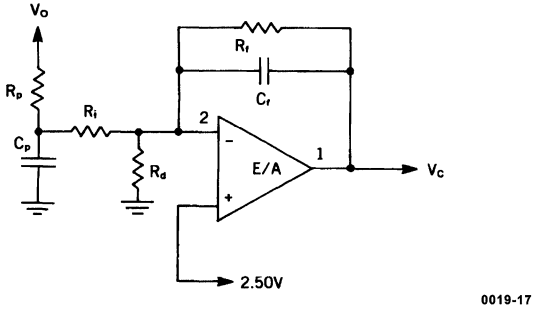


Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ± 1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

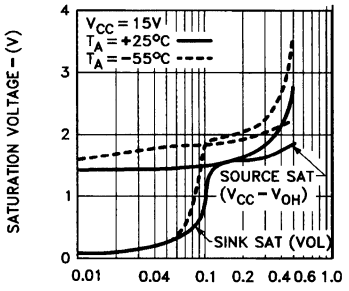


Figure 17. Output Saturation Characteristics

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

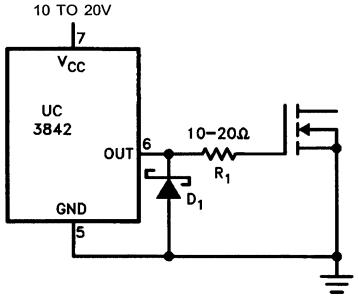


Figure 18. Direct MOSFET Drive

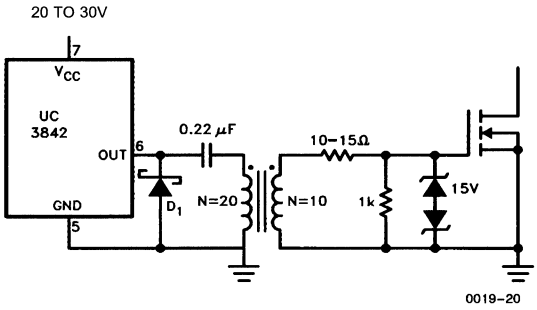


Figure 19. Isolated MOSFET Drive

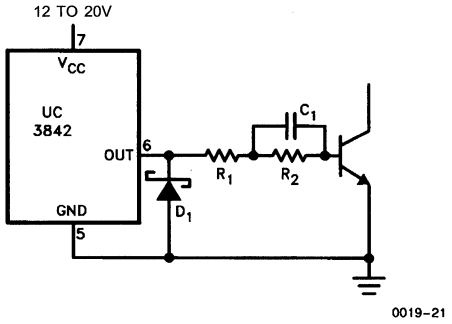


Figure 20. Bipolar Drive with Negative Turn-Off Bias

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 21 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~ 2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~ 1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 31 results in an R_T/C_T waveform like that of Figure 21B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

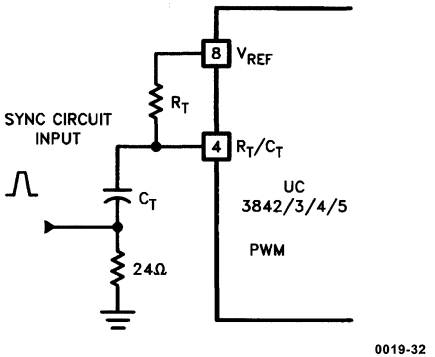


Figure 22. Sync Circuit Implementation

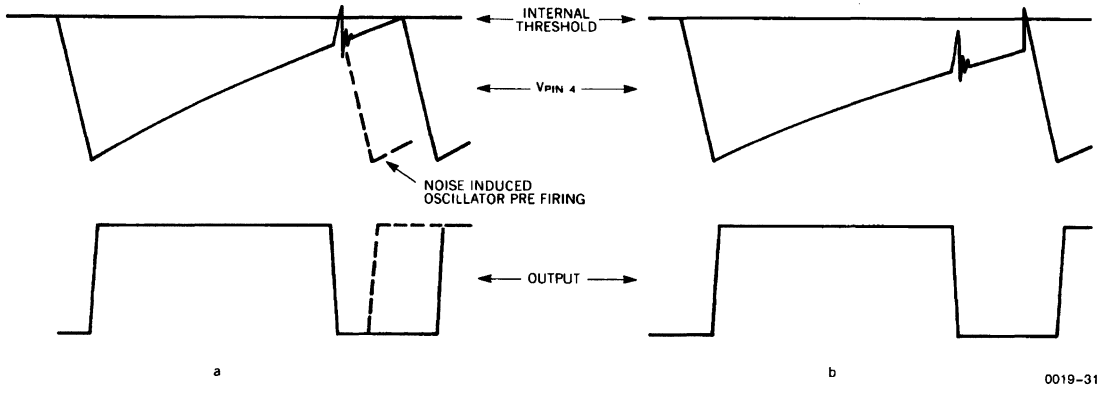


Figure 21. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

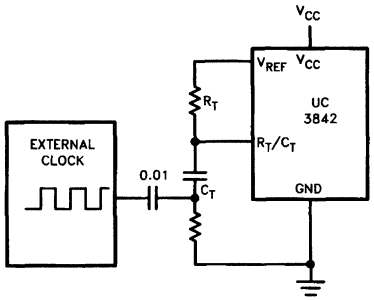
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in "Practical Considerations in Current Mode Power Supplies" listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 23.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a "dead" or off time for the output.

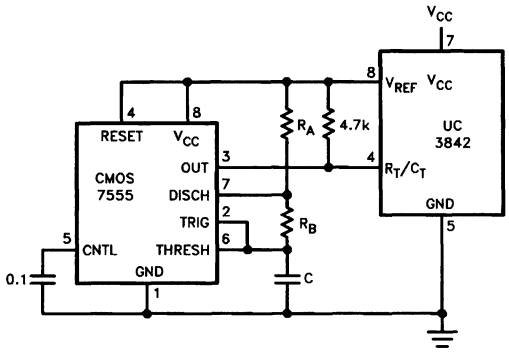
A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



0019-34

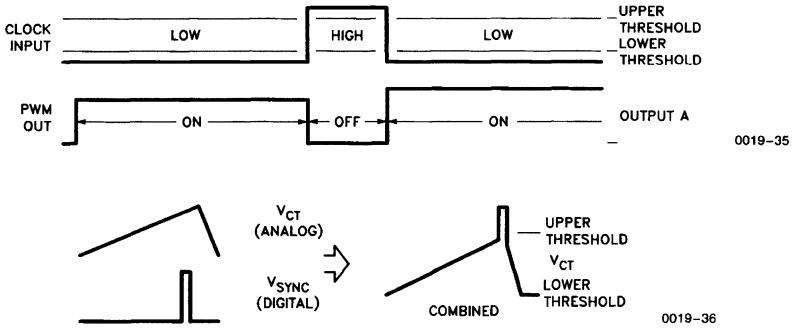
$D_{Max} = t_L (t_H + t_L)$
$t_H = 0.693 (R_A + R_B) C$
$t_L = 0.693 R_B C$



0019-33

Figure 23

Synchronization to an External Clock



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0019-36

Figure 24

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 25 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave(s). The photos shown in Figures 26 and 27 depict the circuit waveforms of interest.

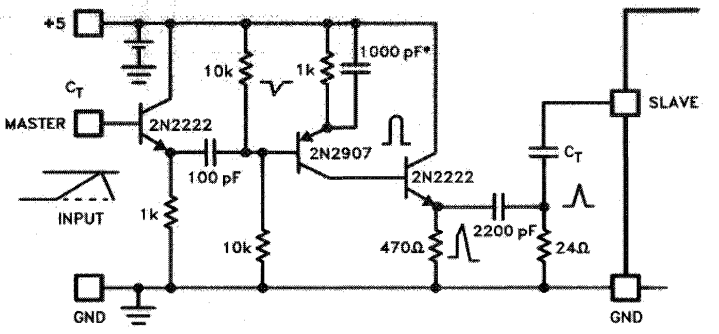
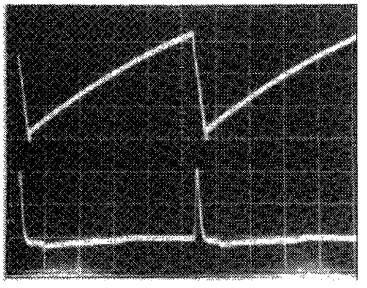


Figure 25. Sync Pulse Generator Circuit



Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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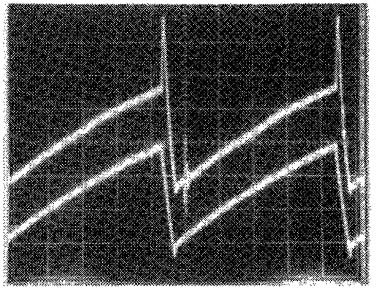
0019-38

Figure 26. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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0019-39

Figure 27. Master/Slave Sync Waveforms at C_T

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up
$V_O \approx 2 \times V_{IN}$

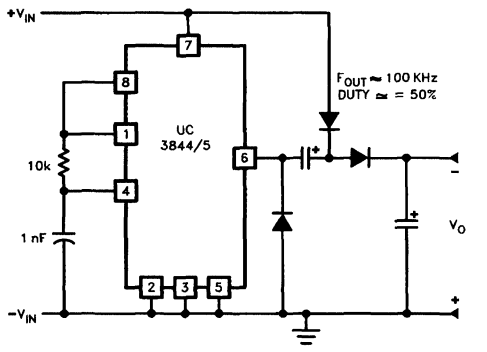


Figure 28

Inverting
$V_O \approx -V_{IN}$

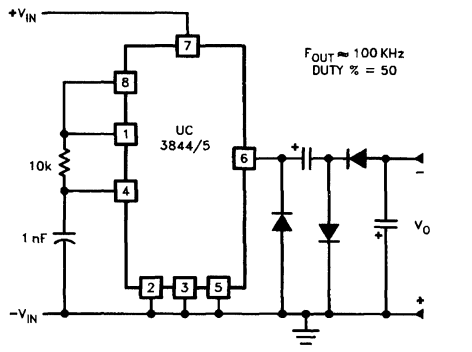


Figure 29

Low Power Buck Regulator-Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see "Closing The Feedback Loop", Buck Topology.

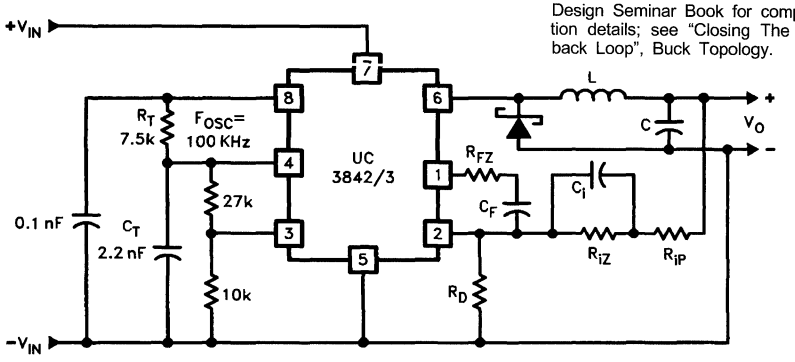


Figure 30

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 31 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

Also consult UNITRODE application note U-96 in the applications handbook.

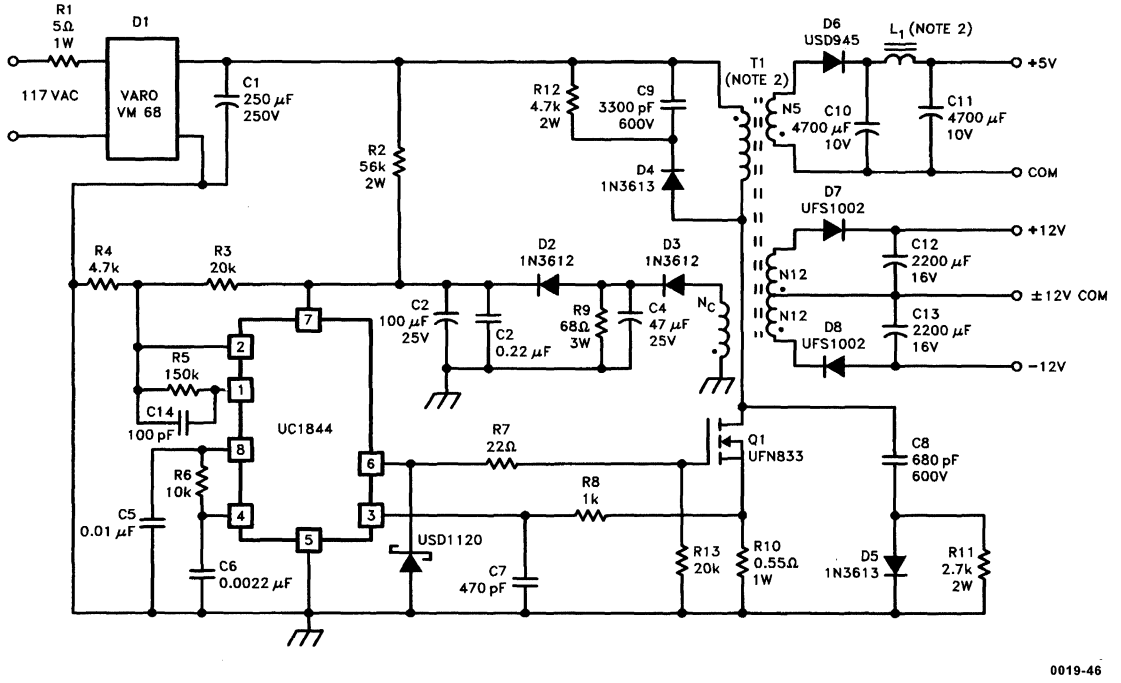
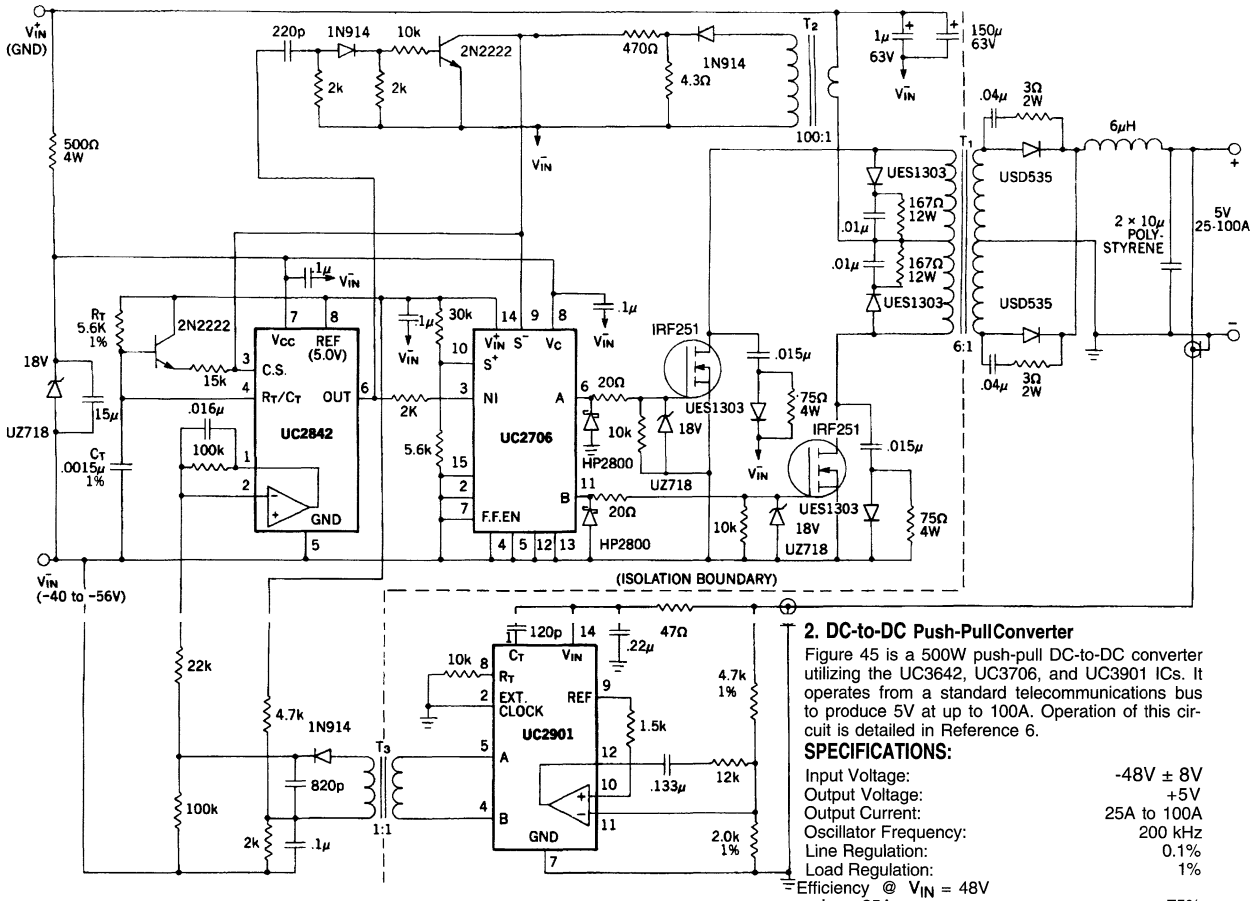


Figure 31

Power Supply Specifications

1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   A. + 5V, ± 5%: 1A to 4A load
   Ripple voltage: 50 mV P-P Max.
   6. +12V, ±3% 0.1A to 0.3A load
   Ripple voltage: 100 mV P-P Max.
   C. -12V ±3%, 0.1A to 0.3A load
   Ripple voltage: 100 mV P-P Max.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460



2. DC-to-DC Push-Pull Converter

Figure 45 is a 500W push-pull DC-to-DC converter utilizing the UC3642, UC3706, and UC3901 ICs. It operates from a standard telecommunications bus to produce 5V at up to 100A. Operation of this circuit is detailed in Reference 6.

SPECIFICATIONS:

Input Voltage:	-48V ± 8V
Output Voltage:	+5V
Output Current:	25A to 100A
Oscillator Frequency:	200 kHz
Line Regulation:	0.1%
Load Regulation:	1%
Efficiency @ V_{IN} = 48V	
I_O = 25A:	75%
I_O = 50A:	80%
Output Ripple Voltage:	200 mV P-P

Also consult application note U-101 in the Unitrode Applications Handbook.

0019-48

Figure 32. 500W Push-Pull DC-to-DC Converter

UNITRODE
APPLICATION NOTE

1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

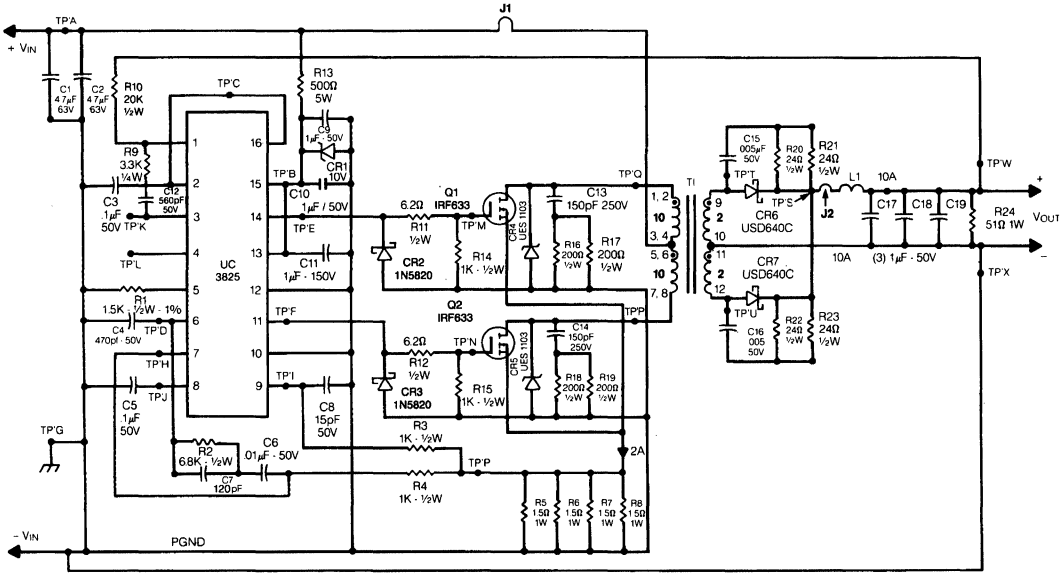
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825 Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.[1]

Figure 1. Schematic Diagram



II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2-10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

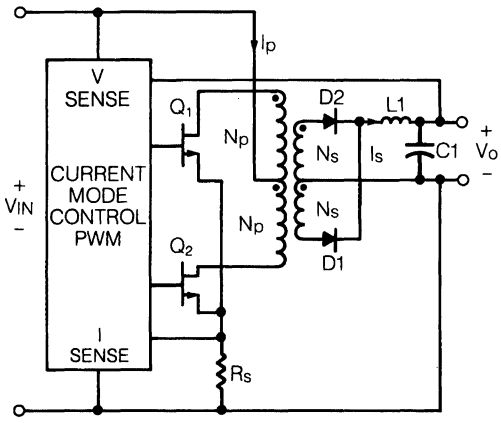


Figure 2. Basic Diagram - Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_s. Simultaneously, diode D1 conducts current $I_p \times N_p/N_s$ in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

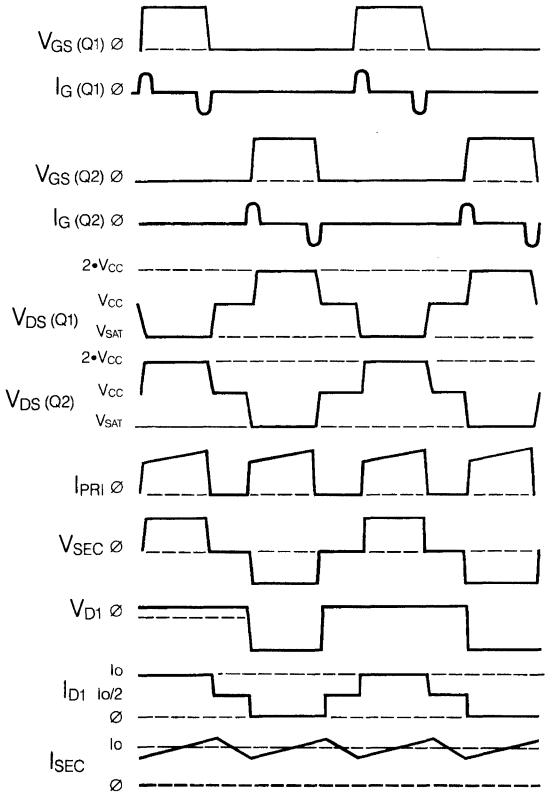


Figure 3. Basic Push-Pull Waveforms

IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{CC} and V_C (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures are used for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} \quad \frac{68\text{ watts}}{42\text{ volts}}$$

The primary current during the transistor on time is:

$$\text{I(p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \le \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload: V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

$$\text{P dc} = \text{I dc}^2\ \text{Rds max} \cdot \text{duty}$$
$$= 2^2 \cdot 0.8 \cdot 0.85/2 = 1.35\text{ watts}$$

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 -150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) - V xtor (max) - V (Rs) max

V p (min) = 42 v - 2.0 v - 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)

V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \bullet Duty\ (max) \bullet 10^4}{2 \bullet Freq. \bullet N\ (p) \bullet \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared2 and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \bullet Np = \frac{V\ pri \bullet D\ max \bullet 10^4}{2 \bullet F \bullet \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \bullet 0.85 \bullet 10^4}{2 \bullet 750{,}000 \bullet 10 \bullet 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise?

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

d pen = 7.5/ (frequencyo5) (cm)

At 750 kHz, this corresponds to $8.66 \bullet 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm*

Primary area (Axp) = 1.24A / 450A / cm² = $2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$I_{rms(sec)} = \frac{I_{sec}^2 (\text{duty on}) + I_{sec}^2 \frac{(2 \cdot \text{duty off})}{2}}{2}$$

$$I_{rms(sec)} = \frac{102 (.425) + 5^2 \frac{(2 \cdot ,075)}{2}}{2}$$

I rms (sec) = 4.81A

Secondary Area (Axs) = 4.81A / 450A I cm*
= $1.07 \cdot 10^{-2}$ cm²

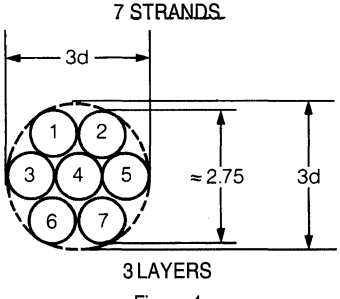


Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\#\ \text{conductors}} = \frac{\text{Axp}}{7} = \frac{2.75\ 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ \text{cm}^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07\ 10^{-2}\ \text{cm}}{1.40\ \text{cm}} = 7.64 \cdot 10^{-3}\ \text{cm}$$

This corresponds to 0.003" thick foil, a standard value. In practice, slightly thicker foil (0.004" to 0.005") may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

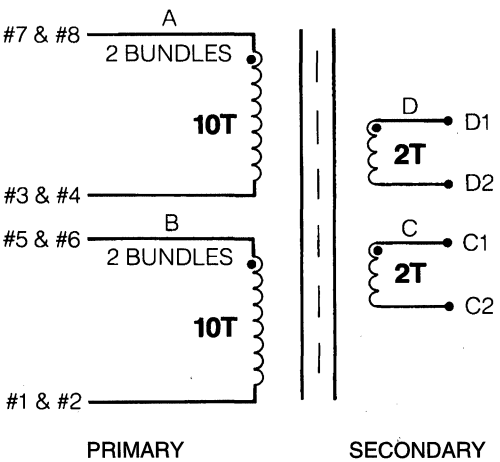


Figure 5. Transformer Schematic

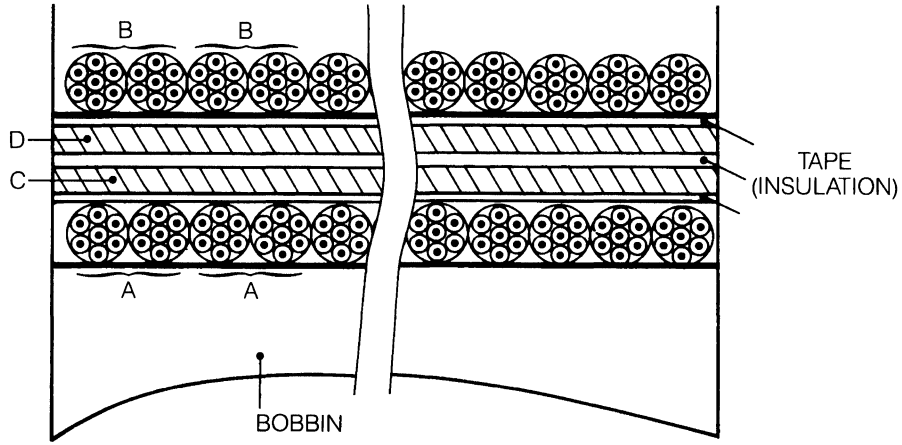


Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of 1.82 $\cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$R_{pri} = \frac{R_{wire} \cdot M.L.T. \cdot \#turns}{\#wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586 \text{ ohm}$$

Voltage drop and power loss in each half winding can be also calculated:

$V(R_{pri}) = I_{pri} \cdot R_{pri} = 2.0 \cdot 0.58 = 0.116$ volt (negligible)

$P(R_{pri}) = R_{pri} \cdot I_{pri}^2 \cdot duty = 0.0586\ 0\ 4\ 0\ 0.425$
$= 0.0996$ watts

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec $= 1.58 \cdot 10^{-4}$ ohms/cm.

$R_{sec} = R_{foil} \cdot M.L.T. \cdot \#\text{ turns} = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2$
$= 0.00143$ ohm

$V(R_{sec}) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143$ volt (negligible)

$P(R_{sec}) = R_{sec}((I_{dc}^2 \cdot D \text{ on}) + (\cdot 2 \cdot D \text{ off}))$

$P(R_{sec}) = 0.00143\,((10^2 \cdot 0.425) + (5^2 \cdot 0.15)) =$
0.066 watts

Transformer Power Losses

The total copper losses for two windings are then:

$P_{cu} = P(R_{pri}) + P(R_{sec}) = 2 \cdot (0.066 + 0.0996)$
$= 0.332$ watts

Estimated eddy current losses are approximately 50% of the copper losses. $P_{cu} \approx 0.50$ watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$P_{core} = 3.327 \cdot 0.15 = 0.50$ watt

The total power lost is a summation of the copper and ferrite losses:

$P_{xfmr} = P_{cu} + P_{core} = 0.50 + 0.50 = 1.00$ watts

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\,di}{dt} \quad L = \frac{V\,dt}{di} = \frac{5.9\text{ v } (350)\ 10^{-9}\text{ s}}{3.0\text{ A}} = 690 \text{ nanohenries}$$

Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \cdot N^2 \cdot D\ (in),\ N = (L/F \cdot D)^1\ (turns)$

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690\ /0.0173 \cdot 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \cdot 10^2 \cdot 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \cdot \frac{T\ period}{2} \cdot \frac{I}{2},\ Delta\ Q = I\ p\text{-}p\ /\ 8 \cdot F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p\ /\ 8 \cdot F \cdot dV = 3\ /\ 8 \cdot 1.5 \cdot 10^6 \cdot 0.10 = 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit/Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section – slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information.

Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability5

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7) that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

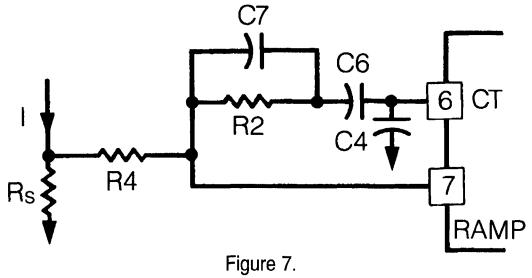


Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

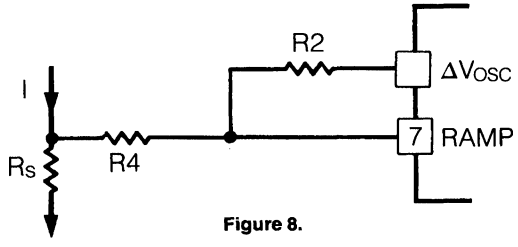


Figure 8.

STEP 1. Calculate Inductor Downslope
S(L) = di/dt = V sec / L = 5.9 V/ .740 pH = 8.0 A/μs (1)

STEP 2. Calculate Reflected Downslope to Primary
S(L)' = S(L) / N (turns ratio) = 8.0/5 = 1.6 A/ $S (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage
V S(L)' = S(L)' • Rsense = 1.6 • 0.375 = 0.600 V/μs (3)

STEP 4. Calculate Oscillator Slope
VS(osc) = d(V osc) / T on = 1.8V / 570 ns = 3.15V/ fi((4)

STEP 5. Generate the Ramp Equations
Using superpostion, the circuit can be configured as:

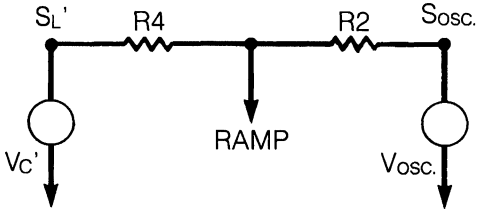


Figure 9.

$$V(ramp) = \frac{V\,S(L)' \cdot R2}{R2 + R4} = \frac{V\,S(osc) \cdot R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,

$$V(ramp) = V\,S(L)'' + V\,S(comp) \quad (6)$$

WHERE

$$V\,S(comp) = \frac{V\,S(osc) \cdot R4}{R2 + R4}; \quad V\,S(L)'' = \frac{V\,S(L)' \cdot R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation

$$V\,S(comp) = m \cdot S(L)'' \quad (7)$$

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S(osc) \cdot R4}{R2 + R4} = \frac{m \cdot V\,S(L)' \cdot R2}{R2 + R4}$$

SOLVING FOR R2:

$$R2 = R4 \cdot \frac{V\,S(osc)}{V\,S(L)' \cdot m} = R4 \cdot \frac{3.15}{0.600 \cdot 0.75} \quad (9)$$

USING CIRCUIT VALUES,

$$R2 = 7.05 \cdot R4$$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency.[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\pi$ R (load) C (output)

$F_z = 1/2\pi$ R (esr) C (output)

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min - 0.300 max

For three capacitors in parallel, ESR = 0.016 - 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

F_p (2A) = $1 / (2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

F_p (10A) = $1 / (2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

F_z (high) = $1 / (2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

F_z (low) = $1 / (2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V(\text{output})}{V(\text{control})} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V(\text{control})} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76. \ 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of -16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = $1 / (2 \cdot \pi \cdot R9 \cdot C12)$

therefore, $C12 = 1 / (2 \cdot \pi \cdot R9 \cdot F \text{ zero})$

$C12 = 1 / (2 \cdot 3.14 \cdot 3300 \cdot 100.000) = 480$ pF (use 560 pF)

R10 / R9 = approx -16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

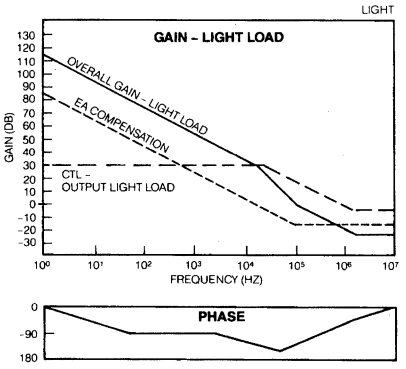


Figure 11.

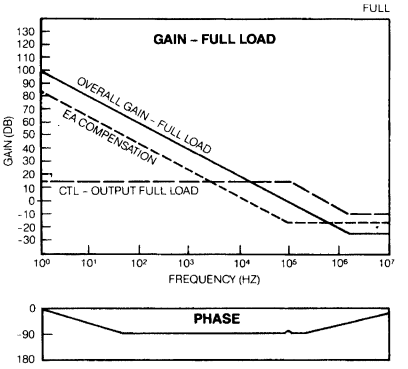


Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13,14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2,3	USD1140	40 V, 1 Amp Schottky
CR4,5	UES1105	150 V, 2.5 Amp Ultrafast
CR6,7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1,2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1K, 1/2 W, 5%	
R5-8	1.5 R, 1W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink-Mosfets (AAALL #5786B)	
H2	Heatsink-Diodes (AAALL #5299B)	

Efficiency Measurements

v (In)	I (In)	p (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

v (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg.
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses	
Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 w
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

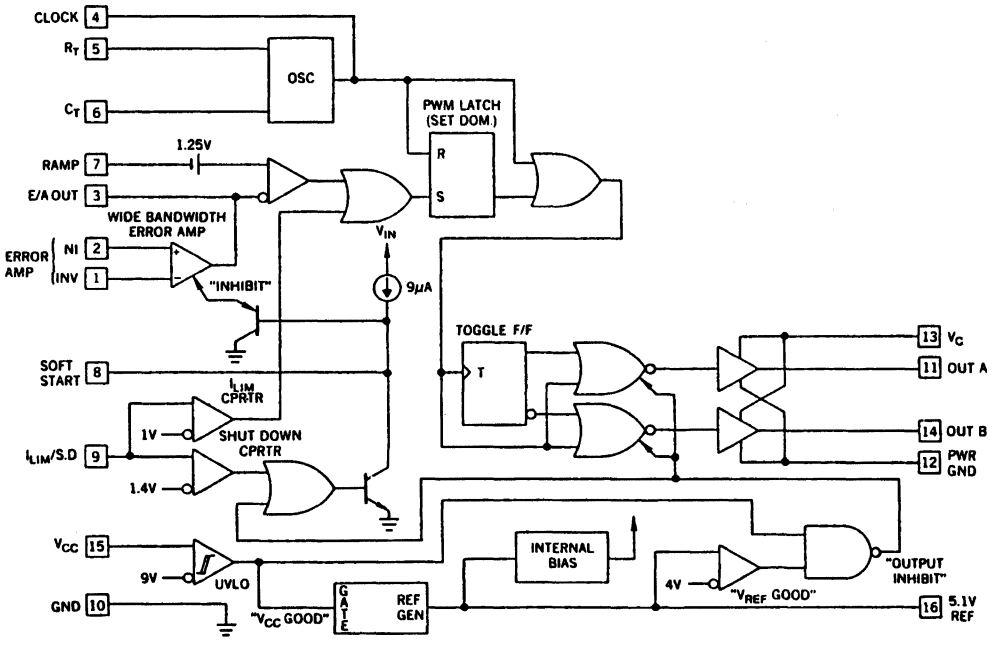
If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

Summary
The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

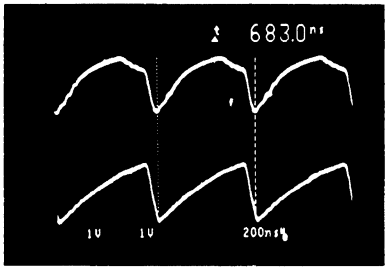
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section CI — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



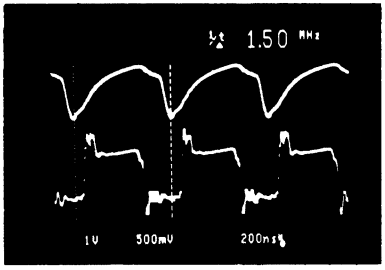
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H' 1 v/cm

Bottom Trace
CT Waveform.
TP 'D' 1 v/cm

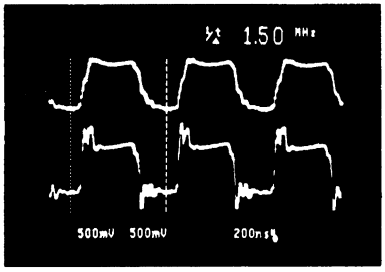
RAMP VOLTAGE



Top Trace
Filtered Ip with
Slope Compensation
TP 'H' 1 v/cm

Bottom Trace
Unfiltered Ip
TP 'P' .5 v/cm

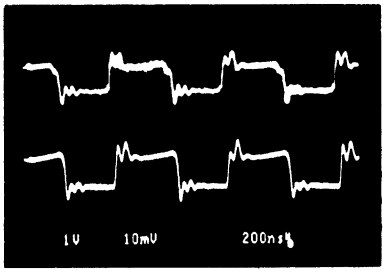
PRIMARY CURRENT



Top Trace
Filtered Ip
TP 'I' .5 v/cm

Bottom Trace
Unfiltered I_P
TP 'P' .5 v/cm

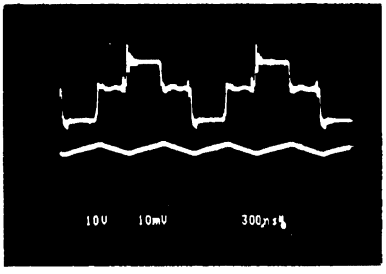
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P' 1 v/cm

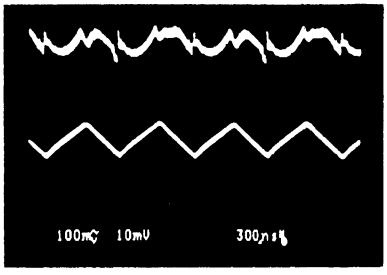
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T' 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W' 100 mv/cm

Bottom Trace
AC Output Current
J2 2 A/cm

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UNITRODE
APPLICATION NOTE

PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant $V_{OUT} L_{SEC}$.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current II, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

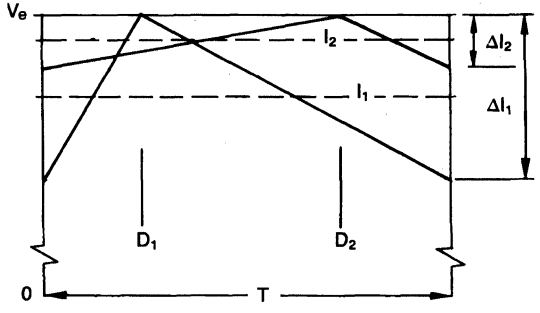


Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

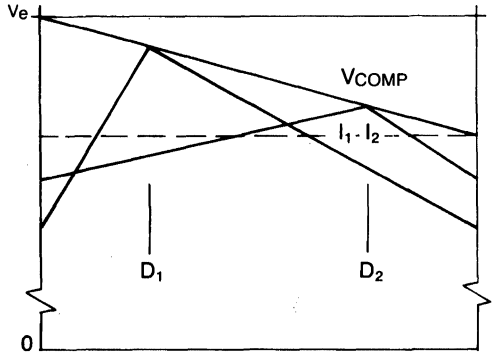


Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator ΔV Oscillator (PK-PK Ramp Amplitude) I Sense Threshold (Max)
Output	V Secondary (Min) L output I AC Secondary (Secondary Ripple Current)
General	R Sense (Current Sensing Resistor) M (Amount of Slope Compensation) N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

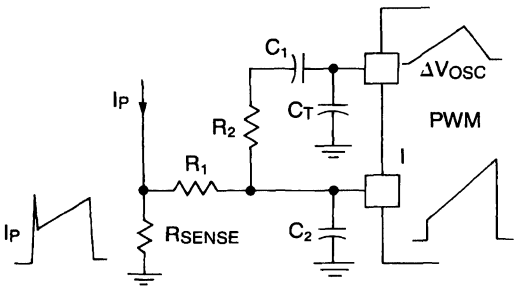


Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

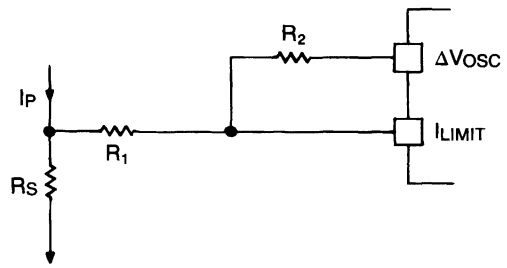


Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope

$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary

$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp

$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope

$V\,S_{(OSC)} = d\,(V_{OSC}) / T\,on$ (Volts/Second)

Step 5. Generate the Ramp Equations

Using superposition, the circuit can be illustrated as:

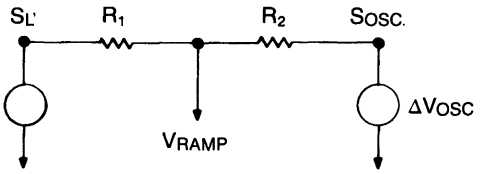


Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} \quad \text{simplifying,}$$

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)} \quad \text{where}$$

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}\ , \text{and } V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation

$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of downslope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

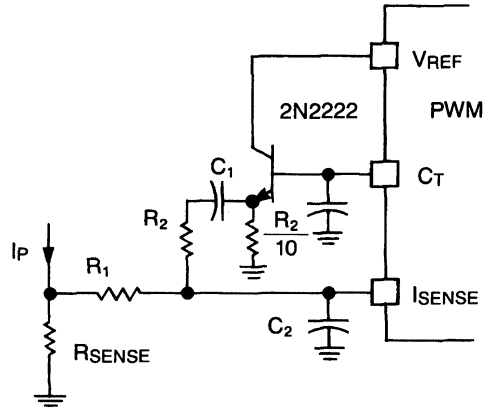


Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 µS
T Deadtime: 500 ns, T on Max = 4.5 µS
Turns Ratio: 15/1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<l0% I DC)
L Output: 5.16 µh

1. Calculate the Inductor Downslope on the Secondary Side

S (L) = di/dt = V_{SEC}/L_{SEC} = 6 v/5.16 µh = 1.16 A/μs

2. Calculate the Transformed Inductor Slope to the Primary Side

S (L)' = S (L) • Ns/Np = 1.16 • 1/15 = 0.0775 A/µS

3. Calculate the Transformed Slope Voltage at Sense Resistor

V S(L)' = S (L)' • Rsense = 7.72 • $1O^{-2}$ • 0.250 = $1.94 \bullet 10^{-2}$ V/μS

4. Calculate the Oscillator Slope at the Timing Capacitor

$S_{(OSC)}$ = d V osc/T on max = 1.8/4.5 = 0.400 V/µS

5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \cdot \frac{V\,S_{(OSC)}}{V\,S(L)' \cdot M} \; ; \; R2 = \frac{1\,K \cdot 0.400}{0.0192 \cdot 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

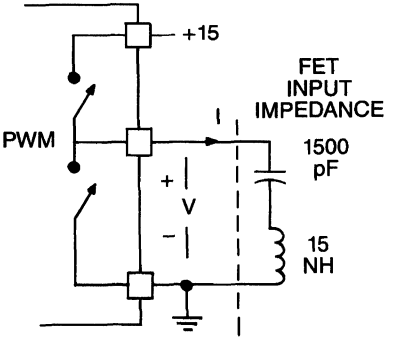


Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

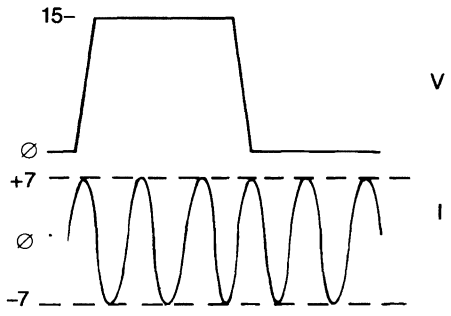


Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (V_C) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

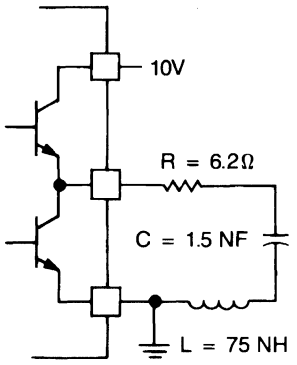


Figure 9. Circuit Parameters

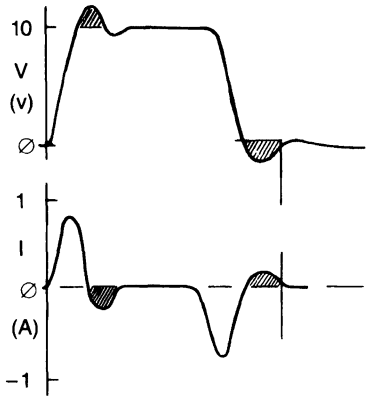


Figure 10. Circuit Response

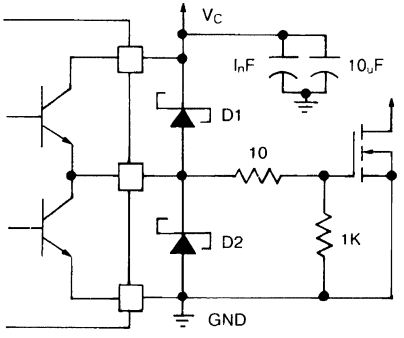
The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$$R\ (\text{gate}) \geq 2 \cdot \sqrt{L/C}$$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS - highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure 10 when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

Power MOSFET Drive Circuit

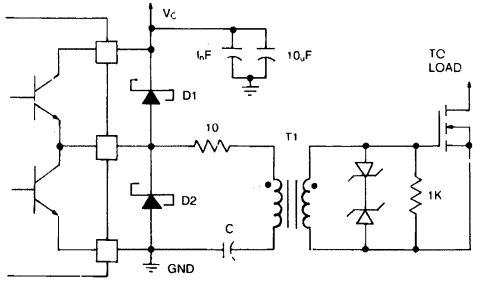


D1.D2: UC3611 Schottky Diodes

Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage

Transformer Coupled MOSFET Drive Circuit



D1 .D2: UC3611 Schottky Diode Array

Figure 12.

inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Transformer Coupled Push-Pull MOSFET Drive Circuit

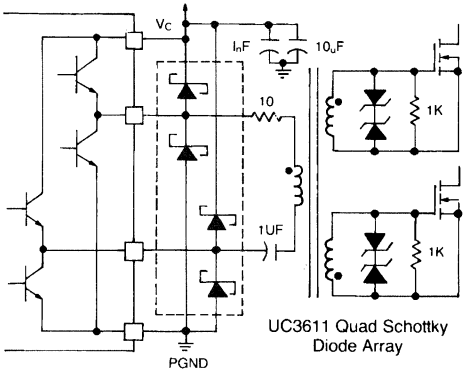


Figure 13.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1 .0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET high speed applications. SEE APPLICATION NOTE U-118

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resulting in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

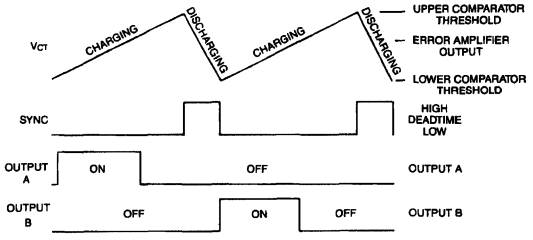


Figure 14. Voltage Mode Control – Normal Operation

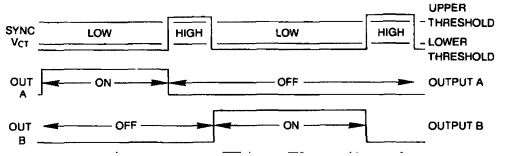


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

- Sync any PWM to/from any other PWM
- Sync any PWM to/from any number of other PWMs
- Sync from digital levels for simple system integration
- Bidirectional sync signal
- Any PWM can be master or slave with no modifications
- Each control circuit will start and run independently of sync if sync signal is not present
- Localized ramp at Ct for slope compensation
- No critical frequency settings on each module
- High speed - minimum delays
- High noise immunity
- Low power requirements
- Remote off capability
- Minimal effect on frequency, duty cycle, and dead time
- Low cost and component count
- Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

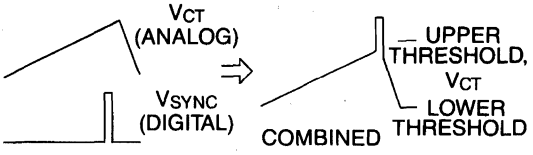


Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

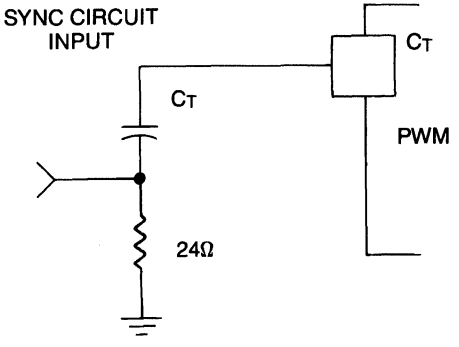


Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail .)

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

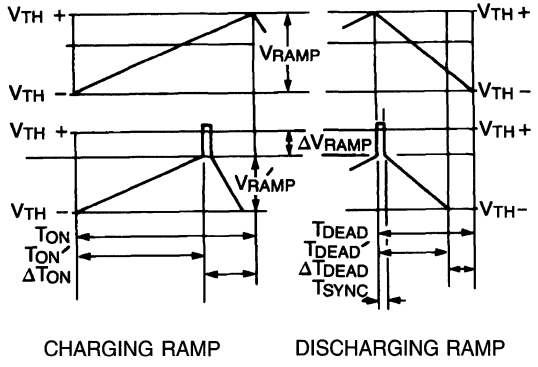


Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\,osc = \frac{1}{Ct}\int I\,chg\,dT = \frac{I\,chg}{Ct}\Big]_{0}^{t} \quad T$$

$$T\,chg = \{\,\Delta V\,osc \bullet Ct\,\} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\,osc = Vth\ upper - Vth\ lower$$

$$\Delta V\,osc' = \Delta V\,osc\,\frac{(tchg')}{t\,chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\,chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\,chg'}{T\,chg(o)} = \frac{T\,sync}{T\,orig} = \frac{F\,orig}{F\,sync} = P\ \text{"relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\,chg' = T\,chg(o) \bullet P = 0.85\ T\,chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta\,[Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\,[Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) - ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\,dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\,dchg' = T\,dchg(o) - T\ loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\,dchg(o) \bullet [\Delta V\,dchg' / \Delta Vosc(o)]$$

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

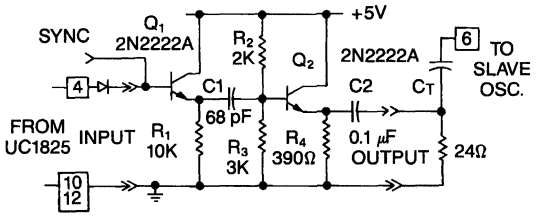


Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor Cl, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master This high speed pulse amplifier circuit adds a minimum of delay (≈ 50 ns) between the master to slave timing relationship.

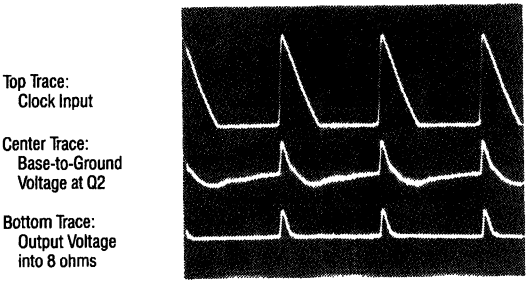


Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.

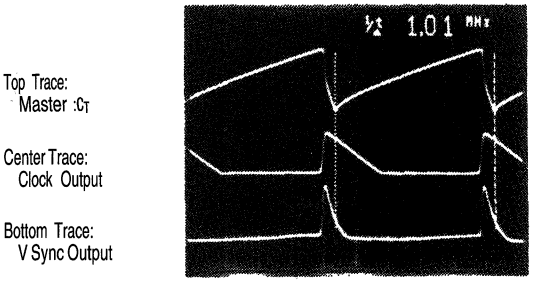


Figure 21. Circuit Timing Waveforms

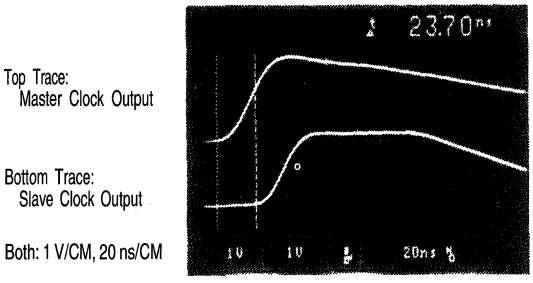


Figure 22. Sync Circuit Delay; Input to Output

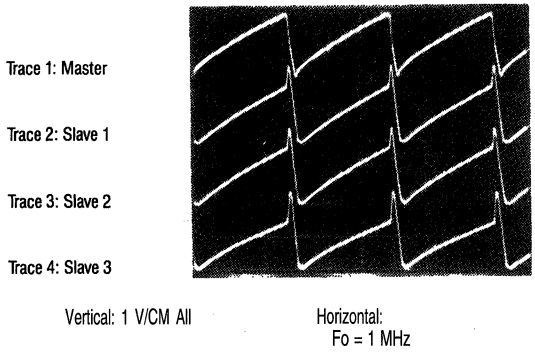


Figure 23. Oscillator Waveforms: Master and Slaves

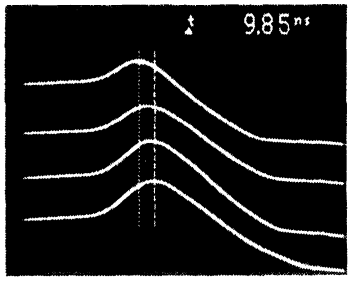


Figure 24. Typical Sync Delay at CT: Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator In this instance, the sync pulse forces synchronization at alternate cycles to the master.

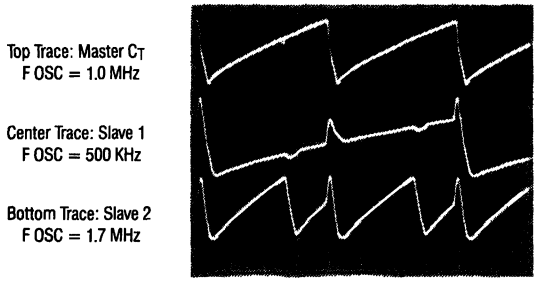


Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

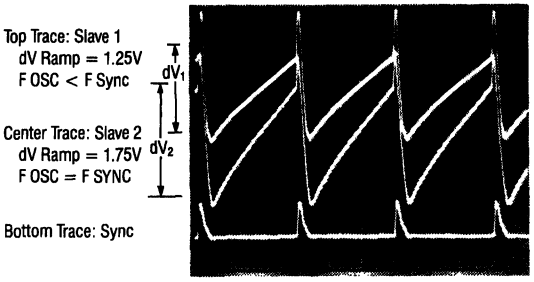


Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

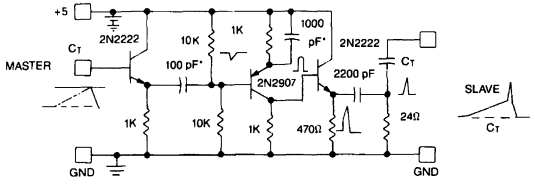


Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

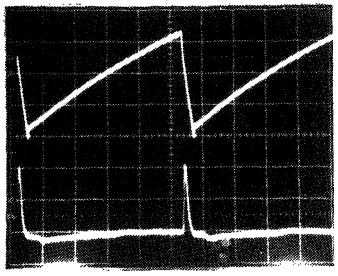


Figure 28. Operating Waveforms at 500 KHz

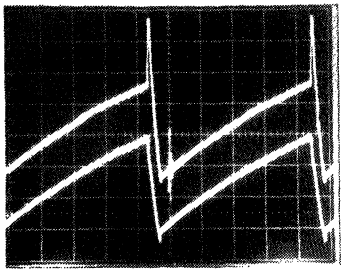


Figure 29. Master/Slave Sync Waveforms at CT

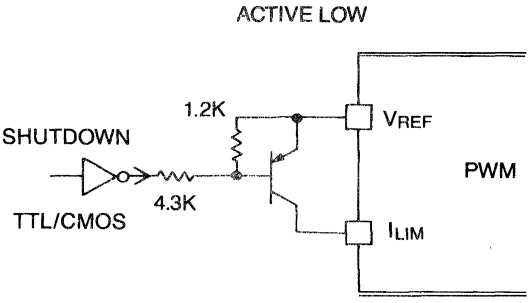
IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

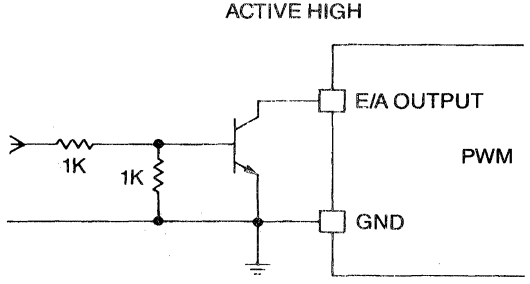
One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.



A. NONLATCHING

Figure 30. PWM Shutdown Circuits

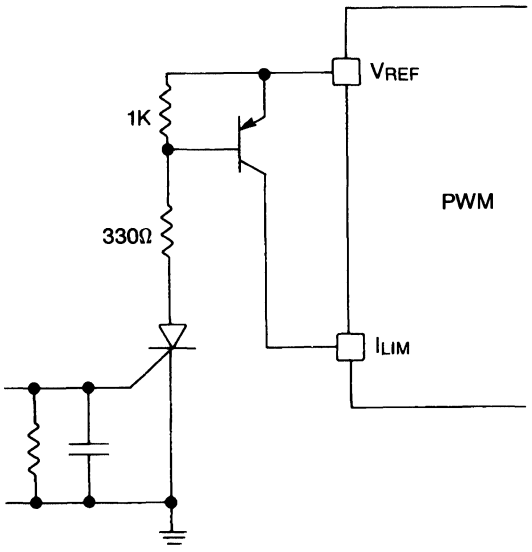


B. NONLATCHING

Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

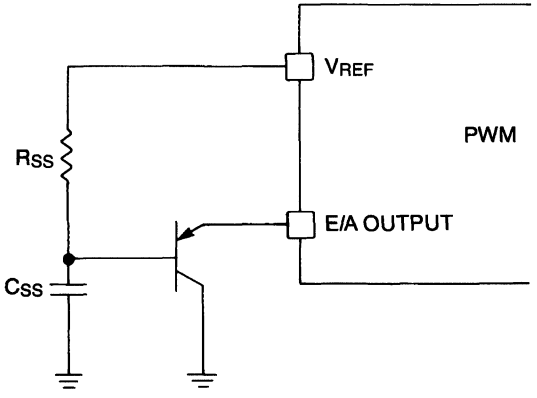


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

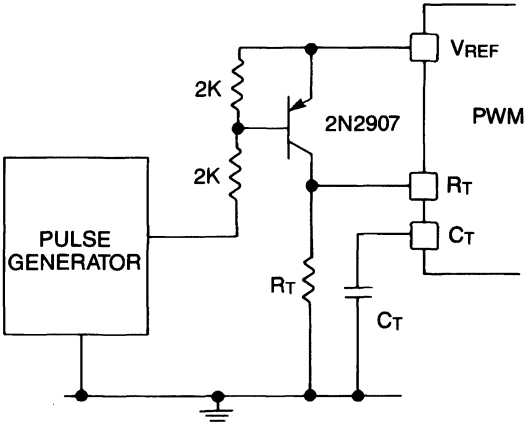
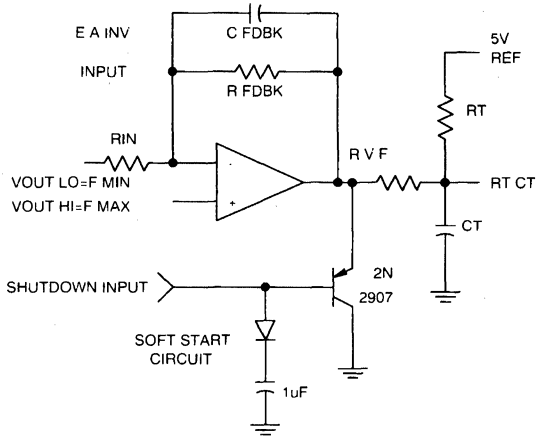


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

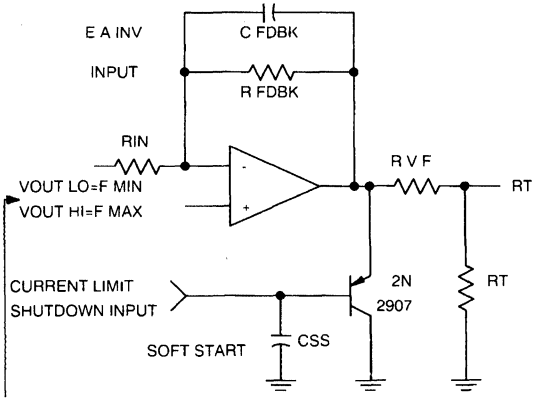
VOLTAGE CONTROLLED OSCILLATOR GENERAL CONFIGURATION

VARIABLE FREQUENCY OPERATION
FIXED 50% DUTY CYCLE
OSCILLATORS WITH SINGLE PIN PROGRAMMING



UC3851 / UC3844A / UC3845A
*GROUND RAMP OR CURRENT SENSE INPUT

OSCILLATORS WITH SEPARATE RT & CT PINS



UC3823 / UC3825 / UC3847
*GROUND RAMP OR CURRENT SENSE INPUT
USE NONINV E/a INPUT FOR REVERSE V/F OPERATION

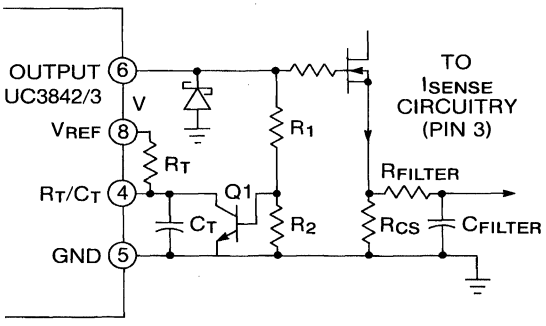
Fixed "Off -Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

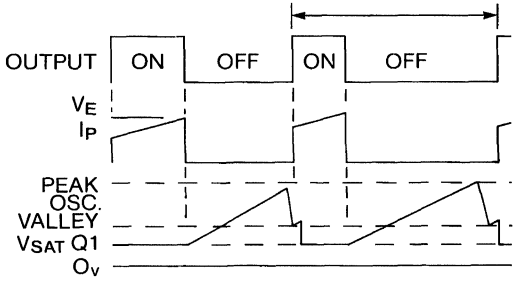
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold.The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator"charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

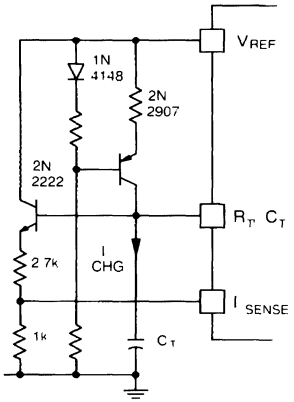


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

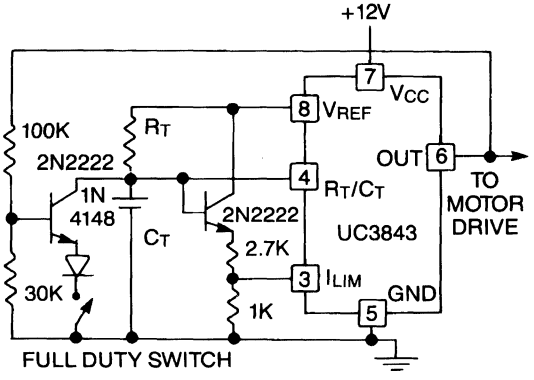


Figure 37. Full Duty Cycle Implementation

VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (< 35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

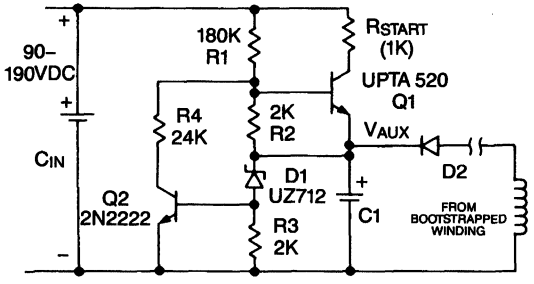


Figure 38. NPN Switches

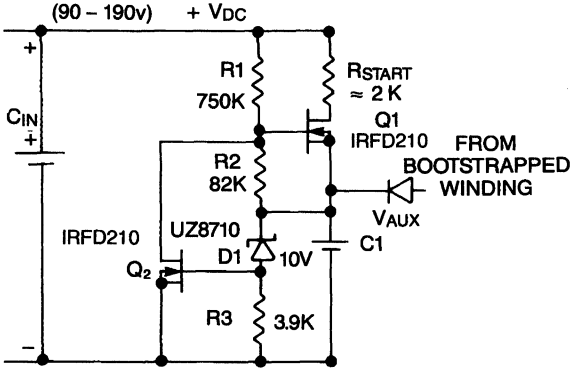


Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor CI is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to CI from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and CI is charged through R start-up from the high voltage DC, as during start-up.

NOTE: SEE DESIGN NOTE DN-26 FOR ADDITIONAL CIRCUITS.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

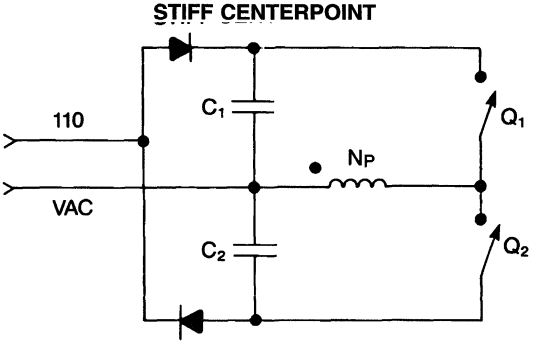


Figure 40.

SOFT CENTERPOINT

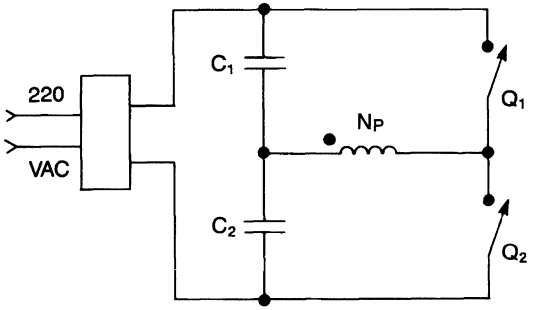


Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

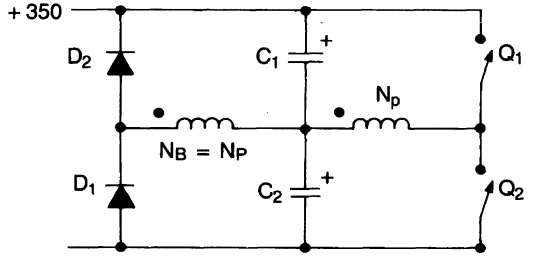


Figure 42. Schematic - Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

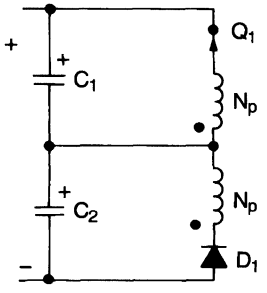


Figure 43. Transistor Q1 On

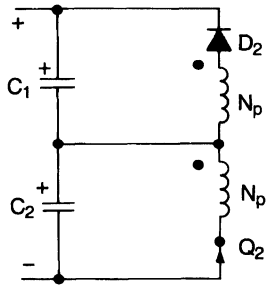


Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

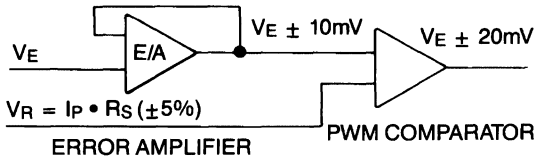


Figure 45. PWM Diagram

In reality, small offets of ± 10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ± 20 millivolt offset represents a ± 2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ± 20 millivolts introduces only ± 0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ± 5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (± 2%) / Rs (± 5%); therefore Ip' = Ip (± 7%) The primary currents (hence output currents) will share within ± seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

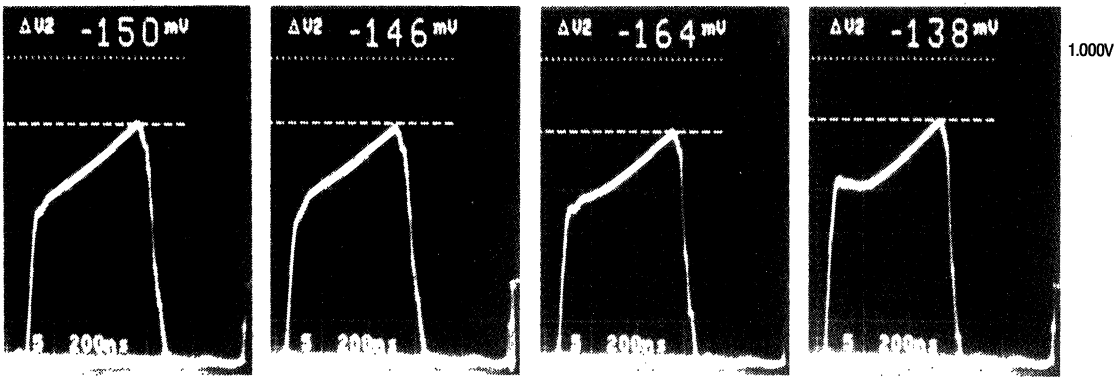


Figure 46. Primary Currents - Parallel Operation

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.

Top Trace:
V_E: Error Voltage with Noise

Lower Trace:
V_R: Primary Current

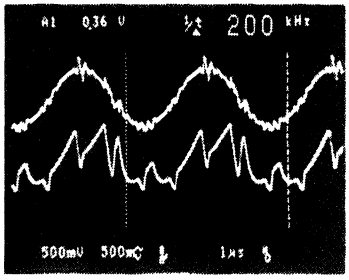


Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter.

Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

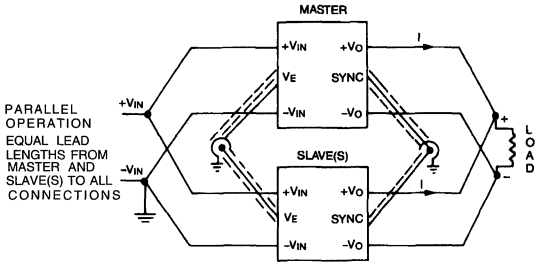


Figure 48.

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APPLICATION NOTE

A NEW FAMILY OF INTEGRATED CIRCUITS CONTROLS RESONANT MODE POWER CONVERTERS

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ABSTRACT

A new family of integrated circuits is introduced. Devices from this family implement the necessary architecture to control a broad range of resonant mode converters. Key features in the areas of switch timing, fault management, and soft-start technique arc unique to this family. Individual devices arc customized to handle off-line or DC to DC. single-ended or dual-switch, zero-voltage-or-current-switched configurations. Specific application to three different resonant mode converters is mentioned.

SURVEY OF EXISTING CONTROL INTEGRATED CIRCUITS

Since 1986, interest in resonant mode power conversion has exploded in the technical conferences. IC makers have been quick to respond with offerings of control ICs. Table 1 is a list of chips available at the present time. To simplify thinking, the first three parts listed are essentially the same design as arc the last two. There arc significant differences in features and performance levels between the three groups. However, a common operational philosophy is shared by all: fixed-pulse-width variable-frequency. This approach has been applied to zero-current-switched (ZCS), quasi-resonant mode converters with reported success.

Table 1. List of Resonant Mode Control ICs

LD405
GP605
CS3805
- - - - - -
UC3860
- - - - - -
MC34066
CS360

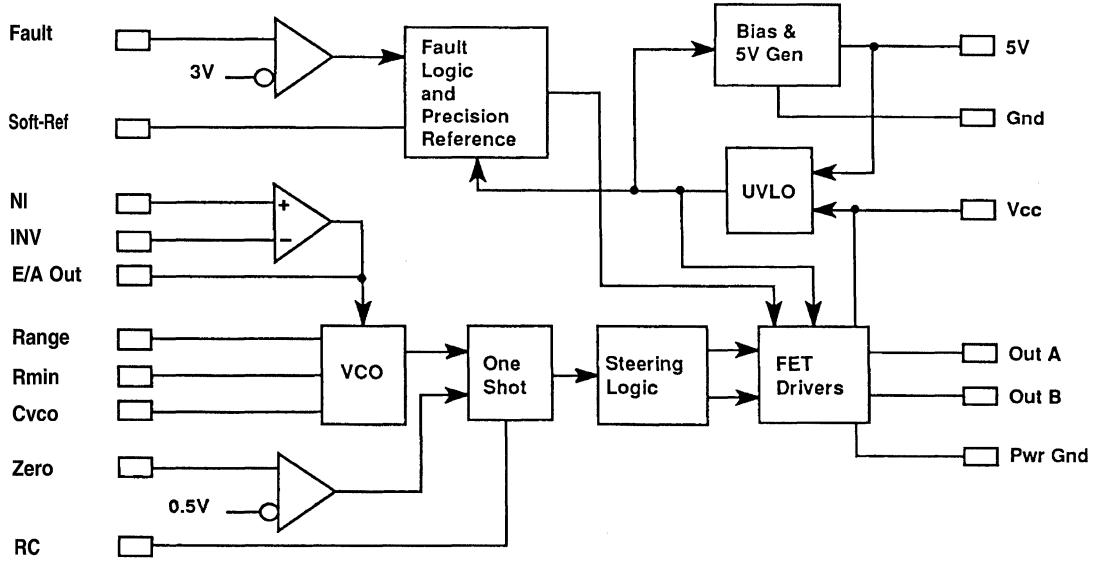

Figure 1. Controller Block Diagram

NEW FAMILY OF RESONANT MODE CONTROL INTEGRATED CIRCUITS

As the discipline is maturing, the advantage of some feature changes has become apparent. Versatility to control both ZCS and zero-voltage-switched (ZVS) converters is needed. The ability to control proper switch times (on or off) with changing line, load, or component values is needed. To address these needs, a family of controllers based on a common silicon die has been developed. Three members of the family, the UC1861, UC1864, and UC1865 will be covered in detail.

The common block diagram of the family is illustrated in figure 1. These parts feature an error amplifier (E/A), voltage controlled oscillator (VCO), one shot timing generator with a zero wave-crossing detection comparator, steering logic to two output drivers, a 5V bias generator, and under voltage lockout (UVLO). A latched fault management scheme provides soft start, restart delay, and a precision reference.

Die options can be produced that give different UVLO levels, as well as different output properties. There arc two UVLO options. The first, suited for off-1ine operation has thresholds of 16 and 10V. While UVLO is active, Icc is less than 0.3mA. The other option is 8 and 7V, to accommodate lower input voltage DC/DC converters.

The flavor of the outputs required by different resonant mode topologies requires the steering logic to be configured specially for each application. The basic options that can be built allow for single or dual switch drive, and controlled on or off times. Zero-current-switching applications require controlled switch on times while zero-voltage-switching applications require controlled switch off times. Figure 2 shows these options.

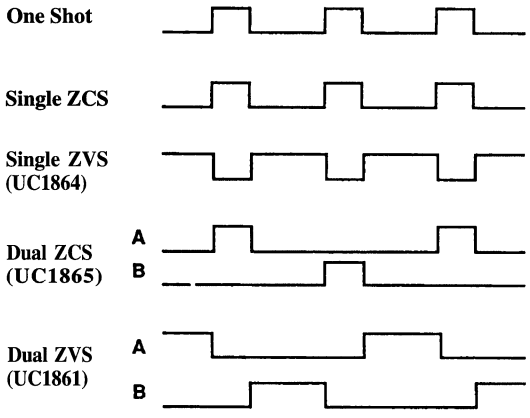

Figure 2. Output Drive For Different Converters

Table 2 details the options implemented in the 1861, '64, and '65. Other options can be built from the same die.

Table 2. Implemented Options in the 1861, '64, '65.

Device	UVLO Vth	Outputs	Zero-(?)-Switching
UC1861	16/10V	Dual	Voltage
UC1864	8/7V	Single	Voltage
UC1865	16/10V	Dual	Current

PRIMARY CONTROL BLOCKS

The fundamental control blocks essential for a majority of resonant mode converters arc an error amplifier. VCO, one shot timing generator, and output stage to drive power mosfets.

ERROR AMP & VOLTAGE CONTROLLED OSCILLATOR

Figure 3 details the E/A and VCO. The E/A output directly controls the VCO via the Irange generator. The VCO has inputs for two resistors, R_{ange} and R_{min} and one capacitor, C_{vco}. R_{min} and C_{vco} determine minimum frequency.

$$F_{min} = \frac{3.6}{(R_{min} * C_{vco})} \quad (1)$$

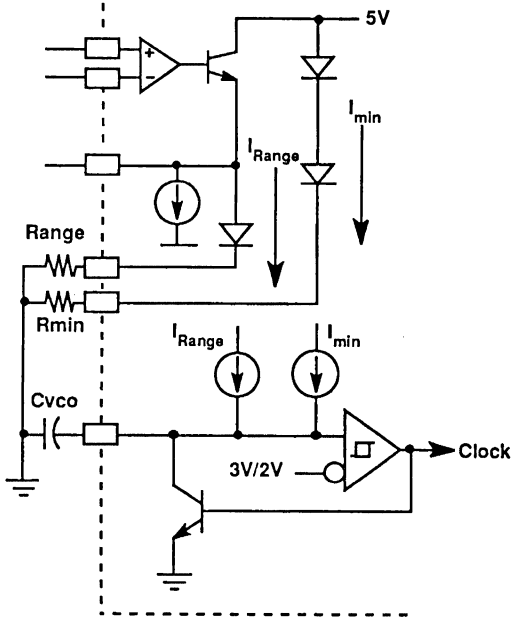

Figure 3. Error Amplifier and Voltage Controlled Oscillator

When the output of the E/A is less than or equal to one diode drop above ground, the VCO operates at minimum frequency. The E/A output can go as high as one diode drop below 5V. When at this potential, the VCO frequency is at its maximum.

$$F_{max} = \frac{3.6}{(R_{ange} \| R_{min}) * C_{vco}} \quad (2)$$

Usable maximum frequency tops out around 1.5MHz. The Frequency range is the difference in equations 2 and 1.

$$\Delta F = \frac{3.6}{R_{ange} * C_{vco}} \quad (3)$$

Since the nominal E/A output swing is approximately 3.6V for full variation in VCO frequency, the gain of the VCO block is

$$dF/dV = \frac{1}{R_{ange} * C_{vco}} \quad (4)$$

In ZCS power supplies, an increase in frequency will corrcspond to an increase in the converter's output voltage. For these applications the E/A non-inverting input is connected to a reference voltage while the output voltage sense is fed back to the inverting input. For ZVS power supplies, a decrease in frequency corresponds to an increase in output voltage. For these systems, the input to the E/A are exchanged.

The common mode range of the E/A is from zero to 6V. This feature allows zero volts to be a valid reference voltage applied to the E/A. Soft start, covered later. takes advantage of this feature.

ONE SHOT TIMING REQUIREMENTS

The basic premise in resonant mode conversion is packets of energy delivered at varying repetition rates. Each energy packet dictates a basic switch on or off time, hence the one shot timer. In ZCS systems the switch is on. In ZVS systems the switch is off. The timer, then, should force the switch to conform to the resonant timing of the tank circuit. It is this conformance that achieves zero stress switching.

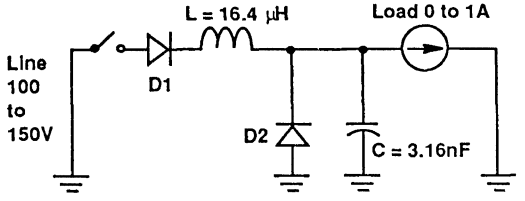

Figure 4. ZCS Resonant Tank Example

For purposes of convenience, a simplified ZCS resonant tank is presented to illustrate the timing requirements of resonant converters in general. This is an example, not a rigorous theoretical presentation. It does, however, demonstratc the problems to overcome in properly controlling a resonant mode converter. The circuit of figure 4 is designed to operate from line input of 100 to 150V and 0 to 1A load current. The tank frequency is arbitrarily selected to be 700kHz. A reasonable first guess for tank impedance is determined by

$$Z_o = \frac{V_{lowline}}{I_{max} * 1.386} \quad (5)$$

$$= 72 \text{ ohms.}$$

From the equations governing resonant tank natural frequency and impedance, L and C can be calculated.

(6)

$$F_o = \frac{1}{2\pi\sqrt{LC}} = 700\text{kHz}$$

(7)

$$Z_o = \sqrt{\frac{L}{C}} = 72 \text{ ohms}$$

$$L = \frac{Z_o}{2\pi F_o} = 16.4\ \mu\text{H} \quad (8)$$

$$C = \frac{1}{2\pi Z_o F_o} = 3.16\text{nF} \quad (9)$$

Figure 5 shows the pertinent current and voltage waveforms for the case of 125V input and 0.8A output. When the switch closes at zero time, the current starts to build linearly. Once the current reaches 0.8A, then load current is completely supplied through the inductor and D2 carries no current. At this point in time the L and C resonate together until inductor current returns to zero. At this time the switch is allowed to turn off, but it doesn't necessarily have to. D1 prevents reverse current in the switch. It isn't necessary to open the switch until the capacitor voltage decays to line voltage. It is acceptablc to open the switch any time during this "switch window". If it is opened too soon, the circuit will suffer severe switching losses. If it is not opened, the tank will resume resonating, as shown by the dashed curves. If the switch is opened later than the switch window, not only will the circuit suffer switching losses, but the transfer function becomes overly complex.

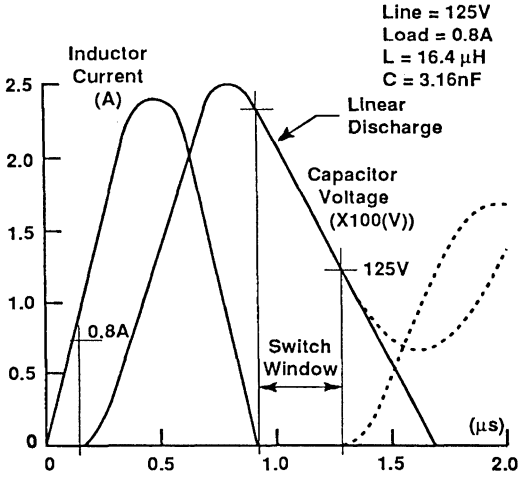

Figure 5. Typical Resonant Tank Waveforms

The graph in figure 6 plots the switch window as a function of load current for both high and low line voltage. For example, at a load current of 0.5A and high line, the switch must be closed for at least 0.80us and need not be opened until 1.61us. Examination reveals the most stringent switch window, 1.03 to 1.21us, occurs at low line and full load. Furthermore, this window is a subset of all other windows. This might lead to choosing a fixed on-time of 1.12us under the assumption that it is relatively easy to build a fixed time one-shot circuit with total variations less than +/-8%. However, further consideration will lead to a different conclusion.

In order to insure that the example in question can be produced, the variations of the resonant components and the possibility of output overload must also be examined. This example continues by assuming total variations for the capacitor are under 10% while under 20% for the inductor. A 20% overload is also allowed.

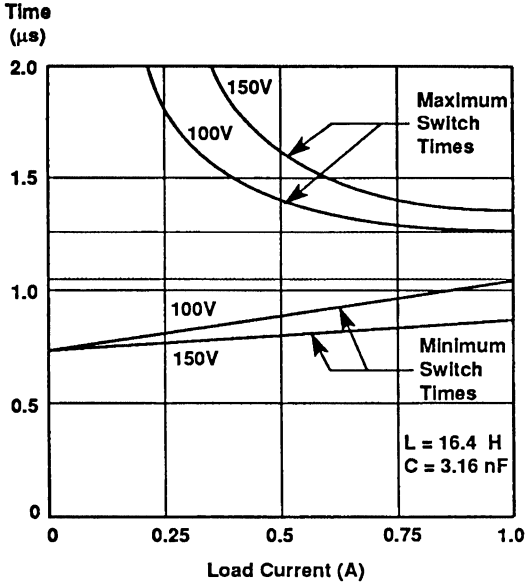

Figure 6. MinimumlMaximum Switch Time vs Load Current

Figure 7 shows the valid switch windows at 1.2A and 100V for nominal component values as well as the four tolerance comers. Several observations can be made. Firstly, the window for the case of +20% inductor and -10% capacitor variations has zero tolerance.

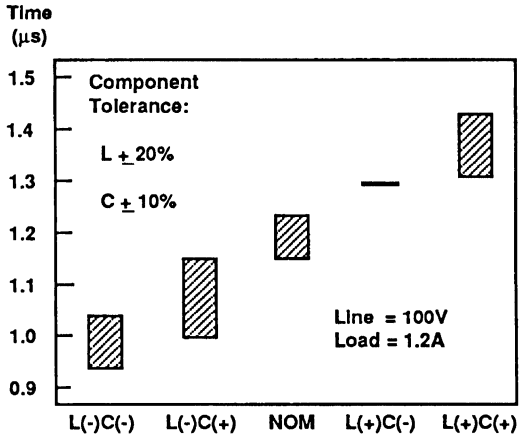

Figure 7. Switch Window vs Component Value

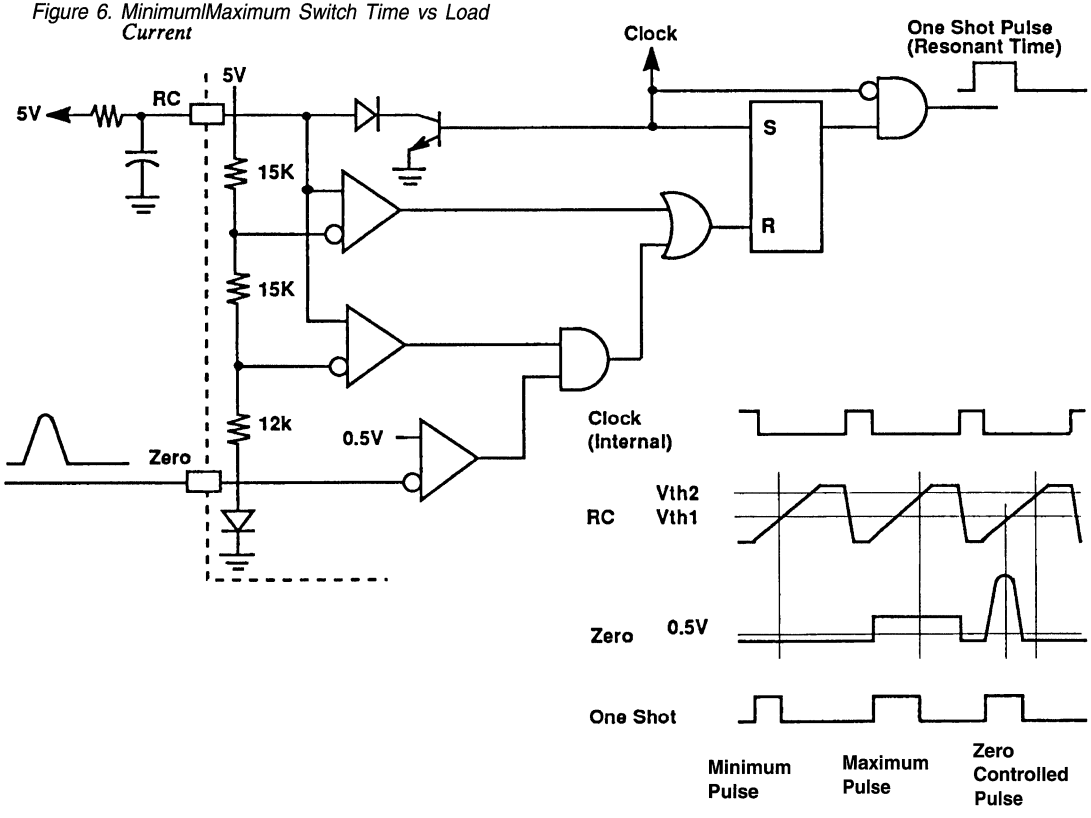

Figure 8. One Shot Timer.

The switch must turn off at 1.30us. This is because the tank impedance is exactly the ratio of low line voltage to overload current for these component values. This is the source of the 1.386 factor in equation 5. Secondly, and the point of the illustration, there is no possible value of fixed switch time that accommodates component variation.

ONE SHOT TIMING GENERATOR

In figure 8, details of the one shot timer arc seen. The clock signal from the VCO sets the latch, blanks the output, and causes the RC timing pin to be discharged. The timing pin determines the minimum and maximum times the one shot output will be high.

$$T_{max} = R * C \quad (10)$$

$$T_{min} = 0.3 * T_{max} \quad (11)$$

Between these two limits, the zero detect comparator will terminate the one shot pulse whenever the Zero pin goes below 0.5V. By sensing the zero crossing of the resonant waveform, the one shot adapts to different resonant component values and varying line/load conditions. The switch time will properly track the resonant tank assuring zero stress switching.

STEERING LOGIC & OUTPUT STAGE

Figures 9, 10, and 11, are block diagrams of the steering logic and output stages. Each output stage is a totem pole driver optimized for driving power mosfet gates. Gate currents of 1A can be obtained from each driver. Note the 1864 single driver is actually both drivers on the chip paralleled. Sample waveforms for the three configurations were shown in figure 2.

Fault and UVLO response of the three configurations is identical. These indications always force both drivers to the low state. During UVLO, the outputs can easily sink 20mA irrespective of Vcc.

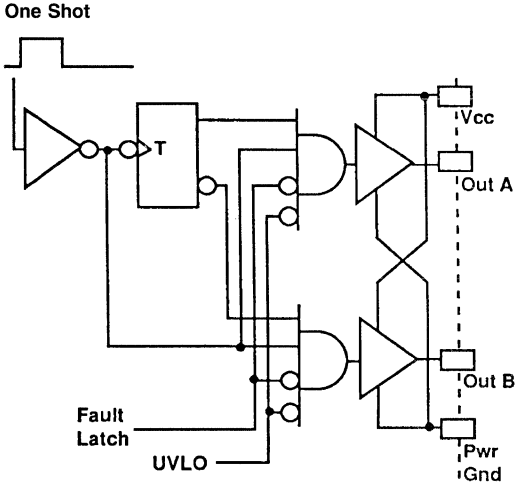

Figure 9. UC1861 Steering Logic

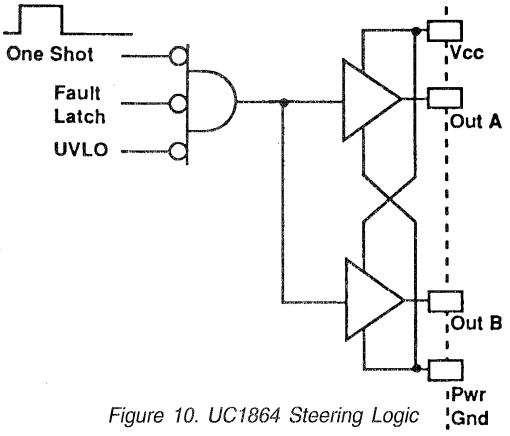

Figure 10. UC1864 Steering Logic

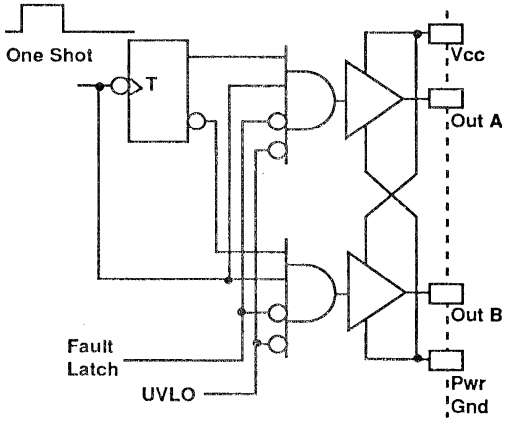

Figure 11. UC1865 Steering Logic

SECONDARY BLOCKS

The secondary blocks on board are UVLO, a 5V bias generator, and fault management with a precision reference. The purpose of the 5V generator is to provide a stable bias environment for internal circuits and up to 10mA of current for external loads. The one shot timing resistor connects to 5V.

UVLO senses both Vcc and 5V. It doesn't allow operation of the chip until both are above preset values. When Vcc is below the UVLO threshold, the 5V generator is off, the outputs are actively pulled low, the fault latch is set, and supply current is less than 300uA.

SOFT START, RESTART DELAY, PRECISION REFERENCE

A novel combination fault management and precision reference is shown in figure 12. One pin is dedicated to a fault sense comparator with a 3V threshold. A second pin does triple duty providing soft start, restart delay, and precision system reference. UVLO initializes the latches. forcing the chip output(s) to be low and the Soft-Ref pin to be discharged. After UVLO, Soft-Ref is charged by an internal 0.5mA current source until is it clamped at

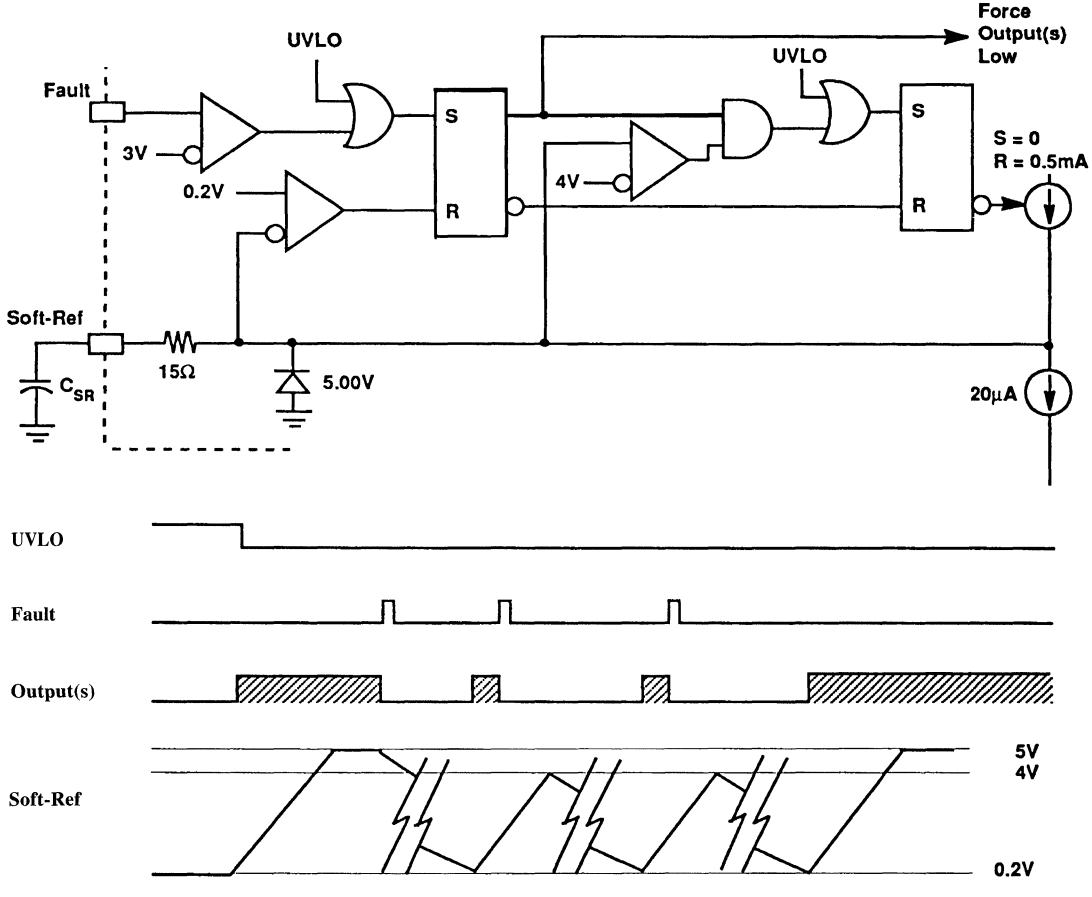

Figure 12. Fault Comparator, Soft Start, Restart Delay And Precision Reference

5V. The soft start time is approximately given by:

$$T_{softstart} = C_{sr} * 10kohms. \quad (12)$$

The recognition of a fault causes the outputs to be driven low and the Soft-Ref pin to be discharged with a 20uA current source. This is the restart delay period. When Soft-Ref reaches 0.2V, the outputs are enabled and the pin is recharged by the 0.5mA current. If a fault should occur before completion of the charge cycle, the outputs are immediately driven low, but the Soft-Ref pin is charged to 4 Volts before the 20uA restart delay current discharges the pin. The restart delay time during continuous fault operation is:

$$T_{restart} = C_{sr} * 190kohms. \quad (13)$$

The ratio of restart delay to soft start is 19:1. If shorter restart delay times are desired, a resistor of 20k or larger can be added from Soft-Ref to ground. The timing equations then become:

$$T_{softstart} = R_{sr} * C_{sr} * \ln\left(\frac{(0.48mA * Rsr) - 0.2}{(0.48mA * Rsr) - 5}\right) \quad (14)$$

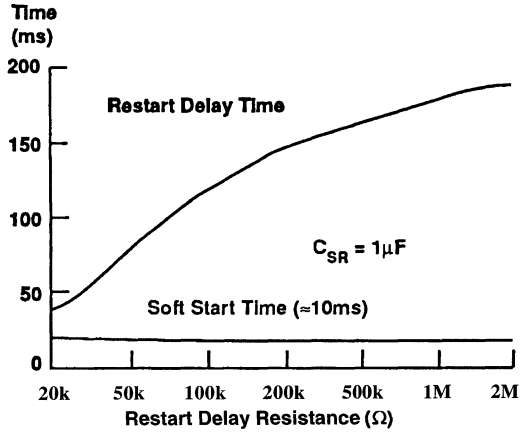

Figure 13. Soft Start And Restart Delay Times

$$T_{restart} = R_{sr} * C_{sr} * \ln\left(\frac{(20uA * Rsr) + 4}{(20uA * Rsr) + 0.2}\right) \quad (15)$$

Soft and restart times are plotted in figure 13 for C_{sr} = 1uF.

The restart feature can be defeated by the addition of a 100k resistor from Soft-Ref to 5V. In this configuration, a fault detection will permanently shut down the converter until either Vcc is recycled and UVLO resets the fault circuit, the 100k resistor is opened or Soft-Ref is externally pulled to ground. The soft start time becomes:

$$T_{softstart} = C_{sr} * 9.2kohm. \quad (16)$$

The Soft-Ref pin is the system reference pin. By ramping the reference from zero during soft start, the converter output will follow the ramp up under closed loop control. This technique allows controlled starts for both ZCS and ZVS systems with no significant overshoot.

The reference characteristic of the Soft-Rcf pin is due to a trimmed 5V zener-type clamp circuit. Fifteen ohms resistance separates the Soft-Ref pin from the clamp to eliminate zener oscillations for any external capacitance value. The clamp zener is designed to tolerate loading of +/- 200uA without degradation of reference accuracy. Loading, however, will alter the soft start and restart delay times, and could even preclude restart delay action unless care is taken in the design.

DC/DC ZVS SINGLE ENDED FORWARD CONVERTER APPLICATION

A ZVS multi-resonant forward converter based on previously reported (ref. 4) work is shown in figure 14. An 1864 is used to control the converter. A 22k resistor from the input line is used to start the circuit, which boot-straps power from the output to the chip after start-up. Before start-up, the chip draws less than 300uA and starts operating when Vcc rcachcs 8V. After start-up, the 22k resistor dissipates 70mW.

The switch voltage V_s is sampled with a 100k/5.1k divider network. The chip anticipates zero crossing when V_s = 10V. In this power converter, switch voltages of 200 to 300V are to be expected. A pnp is used to clamp the zero voltage, Vz to prevent damage to the chip. The 100k resistor represents an insignificant load to the resonant circuit.

The paralleled outputs are connected, as good practice dictates, to the mosfct gate with a small-valued resistor. A schottky diode parallels the output pins to protect the chip from negative voltage spikes that might result from parasitic ringing in the gate circuit.

This power stage was demonstrated to have excellent short circuit tolerance when the minimum switching frequency is well controlled. For this reason, the fault input is not used.

Sensed output voltage is scaled & presented to the non-inverting pin of the E/A. The inverting input is DC referenced to the Soft-Ref

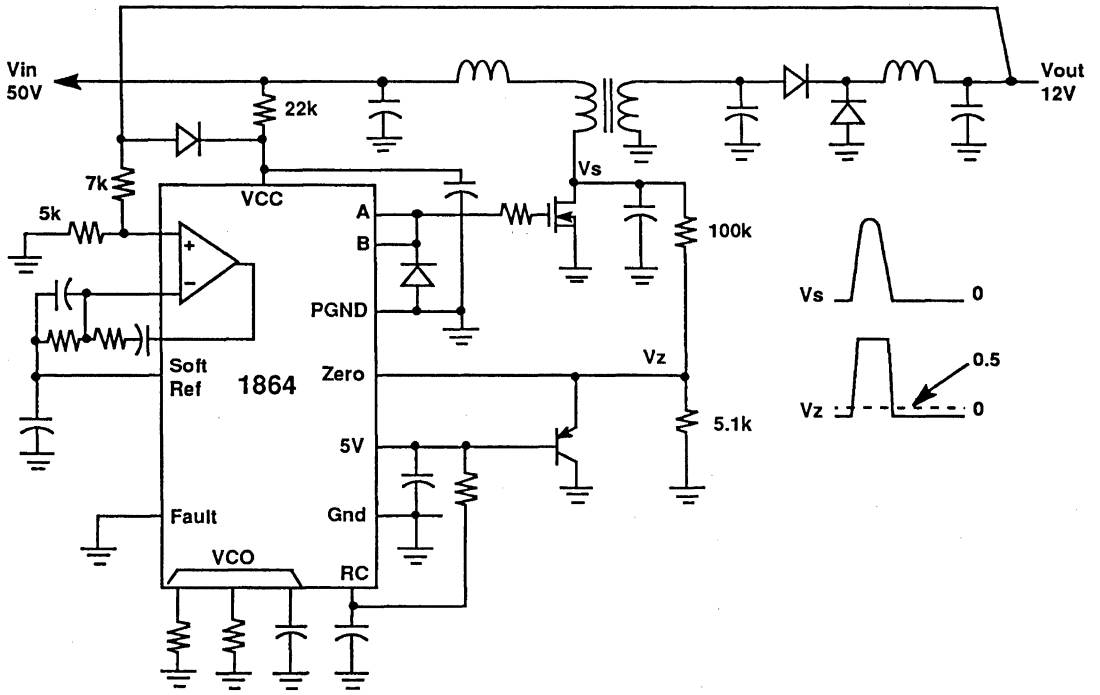

Figure 14. ZVS-MR Forward Converter Controlled By UC1864.

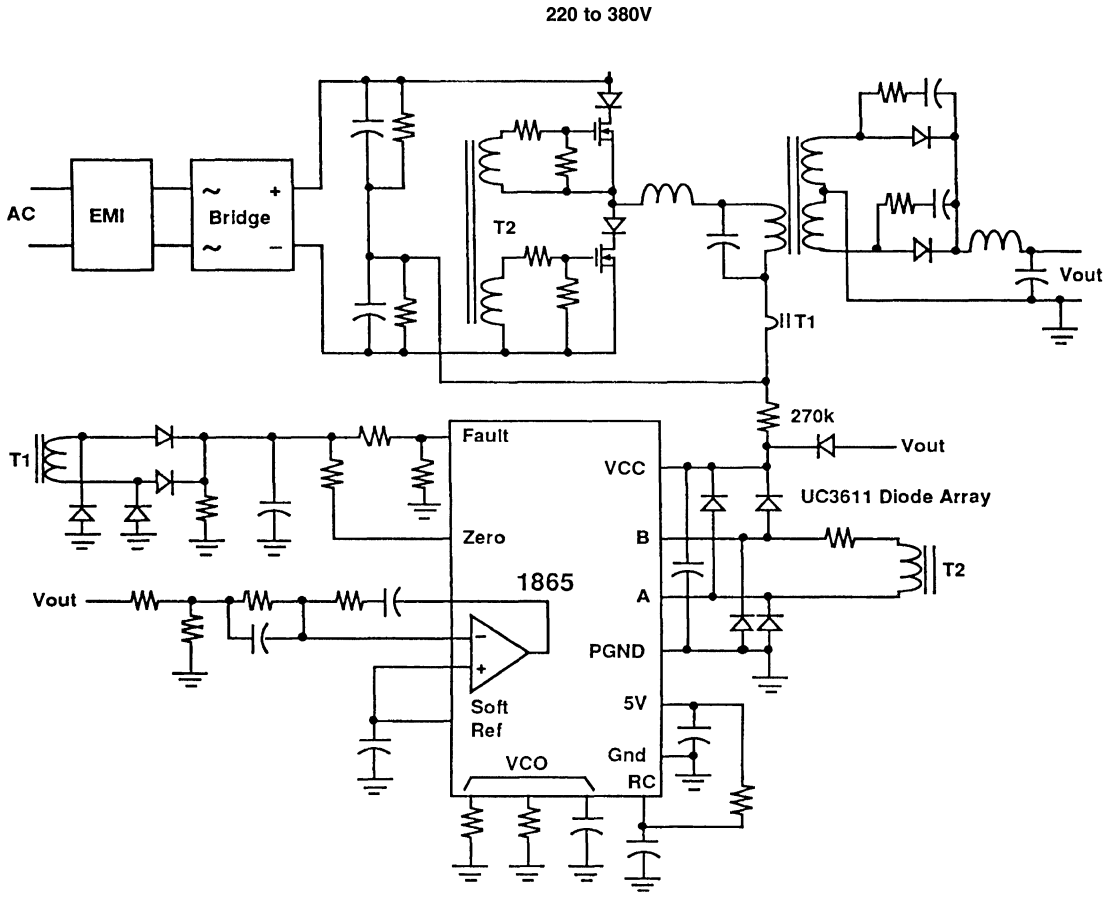

Figure 15. ZCS Off-Line Half-Bridge Converter With UC1865

pin, 5V. The compensation network shown represents zero DC load to the Soft-Ref pin. As long as C_{sr} is much larger than the feedback capacitor, then soft start behavior will be essentially as described in equation 12.

OFF-LINE ZCS HALF-BRIDGE CONVERTER APPLICATION

AZCS off-line half-bridge converter (ref. 1) with an 1865 control IC is shown in figure 15. Irrelevant details in the converter have been simplified. The wide UVLO hysteresis and low start current of the chip have been used in start-up. A single resistor from the high voltage bus is used to start the circuit which then sustains itself from output voltage.

This circuit samples resonant current with transformer T1. Rectified secondary current, converted to an analog voltage, is applied to the fault and zero inputs of the 1865. Excessive current in the resonant tank will effect a shutdown and restart. The resistor between current sense transformer and the zero pin is to limit

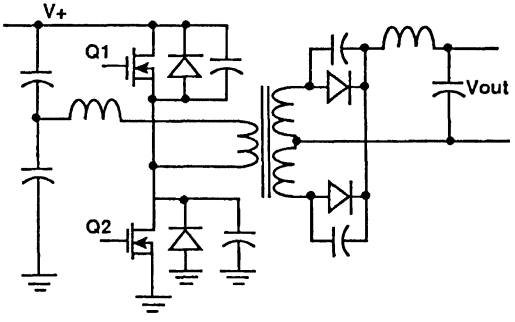

Figure 16. ZVS Half-Bridge Converter

current when the signal is at a high value. The allowable voltage range at the zero pin is zero to 9V, and resistive current limiting to less than 1mA is sufficient.

The half bridge power mosfets arc transformer driven from the differentially connected output drivers of the 1865. A UC3611 schottky diode array has been used to prevent the outputs from being forced too far above Vcc or below ground.

The E/A non-inverting input is directly connected to the Soft-Rcf pin to take advantage of all three features of the pin. This emphasizes the simplicity of application of the 1865 to this converter.

OFF-LINE ZVS HALF-BRIDGE CONVERTER APPLICATION

An off-line ZVS half-bridge converter (ref. 3) is shown in figure 16. An 1861 controls this converter in much the same manner as the two previous examples and is not shown here. The error amp configuration matches the ZVS example while the output stage is configured like the ZCS example.

This application does, however, present a difficulty in sensing zero voltage to control the one shot. In the first ZVS example, the voltage waveform was ground referenced and unipolar. The ZCS cxample had bipolar current, but a transformer and diode bridge conditioned the signal for the chip. In this example, zero switch voltage needs to be sensed for both Q1 and Q2. This poses no real problem for Q2. Q1 is another story. Some form of external circuitry must be employed to sense Q1 and translate the information to the ground referenced chip.

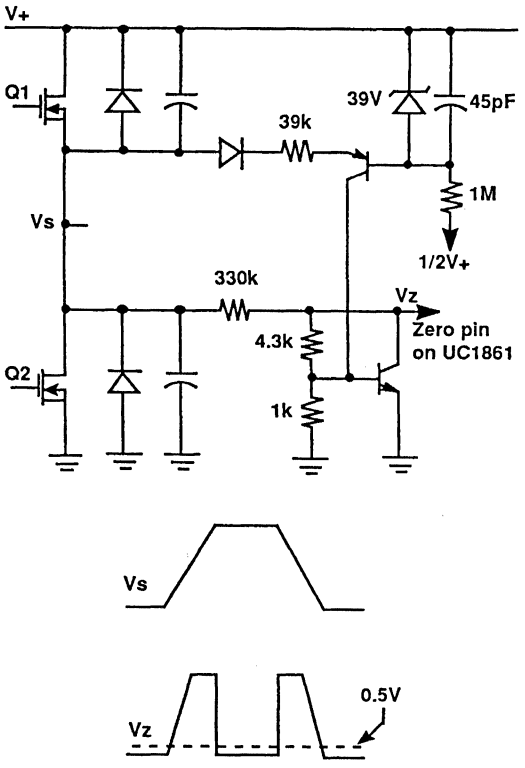

Figure 17. Zero Voltage Sensing Scheme For ZVS Half-Bridge Converter

An easily implemented high voltage comparator circuit is shown in figure 17. The pnp and diode are the only high voltage components used. The circuit dissipates only 300mW. The output of this circuit is applied directly to the zero input of the 1861.

CONCLUSION

A new family of integrated circuits to control resonant mode converters has been introduced that provides several improved features over those previously available. This family has parts that are suited not only to zero-current-switching, but also to zero-voltage-switching converters. The 1861, 1863. and 1865 are suited to off-line ZVS, DC/DC single ended ZVS, and off-line ZCS systems. Controllers for other specific converters can be built from this family. Adaptive control for resonant tank component variations as well as varying line and load conditions is inherent in the chip due to its zero crossing detect circuitry. A unique one pin approach to soft start, restart delay, and system reference provides adjustable restart delay to soft start time ratios as well as closed loop control during soft starts. Relative ease of application to three previously reported converters was discussed.

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APPLICATION NOTE

THE UC3823A,B AND UC3825A,B ENHANCED GENERATION OF PWM CONTROLLERS

BILL ANDREYCAK

ABSTRACT

This application note will highlight the enhancements incorporated in four new PWM control ICs, the UC3823A, UC3823B, UC3825A and UC3825B devices. Based upon the industry standard UC3823 and UC3825 controllers, this advanced generation features several key improvements in protection and performance over their predecessors. Newly developed techniques such as leading edge blanking of the current sense input and full cycle soft start protection following a fault have been incorporated into the design. Numerous enhancements to existing standard functions and features have also been made.

INTRODUCTION

Higher degrees of integrated functions within PWM IC controllers are necessary to remain in pace with todays advancing power supply technology Many external features, used almost universally by designers, have been built into this new generation of UC3823A,B and UC3825A,B PWM controllers. These control enhancements can be classified as either a performance or protection improvement, and an itemized description of each will be presented. The new features are:

PERFORMANCE IMPROVEMENTS

- Lower startup current
- Accurate oscillator frequency
- Leading Edge Blanking
- Higher current totempole outputs
- Higher G.B.W. Error Amplifier

PROTECTION ENHANCEMENTS

- Active Low outputs during UVLO
- Advanced undervoltage lockout
- Latched fault logic
- Full-cycle soft start
- Restart delay after fault

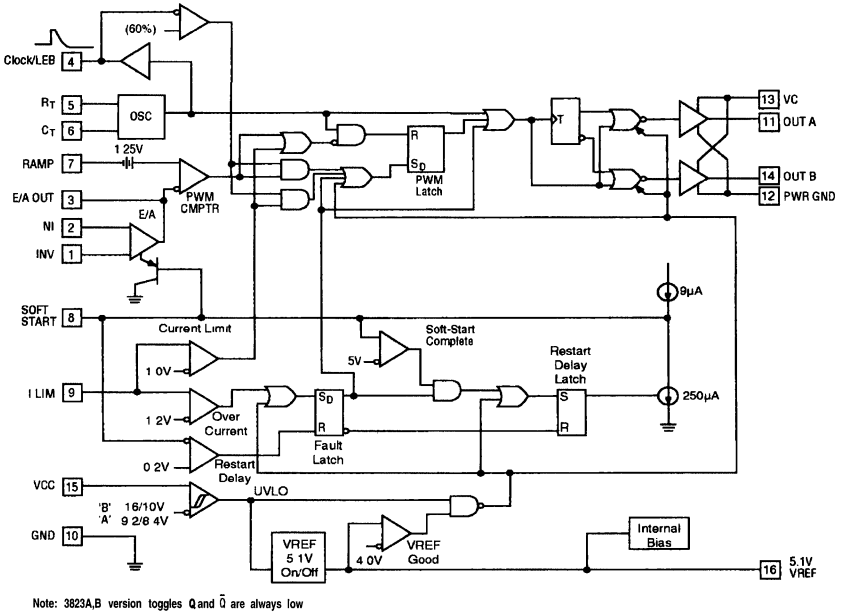

Figure 1- UC3823A,B and UC3825A,B Block Diagram

UC3823A,B AND UC3825A,B FEATURES PREVIEW AND APPLICATIONS GUIDE

In most applications, the UC3823A and UC3825A devices are enhanced drop-in replacements for the UC3823 and UC3825 high speed PWMs. The "A" suffix versions (UC3823A and UC3825A) feature similar undervoltage lockout (UVLO) thresholds to the preceding generation which turn on at 9.2 volts and turn off at 8.4 volts. Off-line power supplies can benefit from the wider UVLO hysteresis of the "B" version devices (UC3823B and UC3825B) which turn on at 16 volts and off at 10 volts. This, in conjunction with the lower startup current of 100 microamps can streamline the IC's power supply and minimize startup circuitry power loss.

One significant difference will be found on the UC3823A and UC3823B controllers. Formerly, the UC3823 (non A or B version) provided access to the current limit comparator's threshold at pin 11. This could be accurately set by the user within the range of 1.0 to 1.25 volts with an external reference voltage. The UC3823A and UC3823B devices use pin 11 as a high current totempole output, identical to that found on pin 14. These outputs can be paralleled - effectively doubling the peak output current capability to 4 amps. No access to the previous current limit reference (I LIM REF) comparator is provided as this threshold is internally set to 1.0 volts with a +/- 5% accuracy over all operating conditions. Existing applications can incorporate the UC3823A or UC3823B devices by simply removing any of the former external biasing components to pin 11.

One other major difference to the prior generation of PWMs is the reduced maximum operating supply (Vcc) and collector supply (Vc) voltages of 22 volts versus 30 volts. This characteristic is a principal consideration when determining the IC power supply, as nearly all applications utilize a supply voltage between 10 and 15 volts. Typical supply current is higher; 28 mA versus the former 22 mA, however the maximum Icc is unchanged at 33 mA.

Since many of the enhancements in this new family of PWMs are executed using internal circuitry, most applications require no additional components externally to realize a performance or protection advantage. The list of improvements which includes latched fault protection and full cycle soft start should not require any PC board changes. The leading edge blanking feature, however, will require one capacitor from the CLOCK/LEB (pin4) to ground to facilitate programming.

The improved oscillator section can be optimally programmed for the correct frequency and maximum duty cycle combination. No changes to the timing component values of Rt and Ct are necessary. Additionally, high frequency current mode applications can benefit from the high gain bandwidth error amplifier (12 MHz). Unity gain bandwidth is also up from 5.5 MHz to 9 MHz. This should not require changes to the PC board layout unless the compensation circuit design relied upon the older 5.5 MHz UGBW for high frequency roll-off.

STARTUP FEATURES

Since a majority of PWM applications are off-line converters, a low startup current is desirable. This attribute minimizes the complexity and power loss of the startup power supply once normal operation is attained. Every milliamp of additional startup current drawn by the controller results in a power loss of approximately 385 milliwatts in a power factor corrected application. Heat, PC board real estate and additional cost are unnecessary extras which can be eliminated with a lower startup current controller.

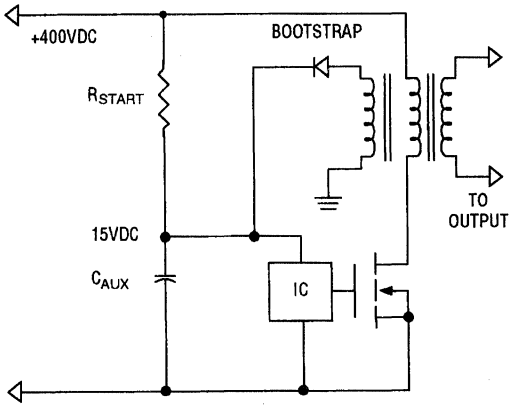

Figure 2 - Startup/Bootstrap Circuit

This new generation of UC3823A,B and UC3825A,B control ICs minimizes the startup current to 100uA typically. Once the IC crosses its undervoltage lockout threshold, the current drawn will increase to the typical running current.

In an off-line converter, two things are necessary to get the main converter up and running when the control IC turns on. First, the IC should contain wide undervoltage lockout hysteresis. Second, the bootstrap supply should come up and into regulation very quickly before the auxiliary capacitor voltage drops below the ICs lower (turn-off) undervoltage lockout threshold.

Undervoltage lockout thresholds are primarily determined by the allowable MOSFET gate voltage range. Operation with gate-to-source voltages above sixteen volts can cause over-stress to the device, and voltages lower than about nine volts can cause linear FET operation. The "B" suffix designator (UC3823B and UC3825B) is used to define devices which exhibit typical undervoltage lockout thresholds of

16V (turn-on) and 10V (turn-off) for off-line applications. The "A" suffix parts (UC3823A and UC3825A) incorporate 9.2V (turn-on) and 8.4V (turn-off) thresholds for DC to DC converter applications, and are compatible with existing UC3823 and UC3825 (non A,B) UVLO thresholds.

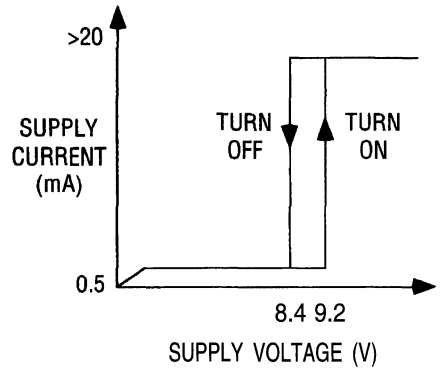

Figure 3 - 9.2/8.4V UVLO Thresholds-DC/DC Converters

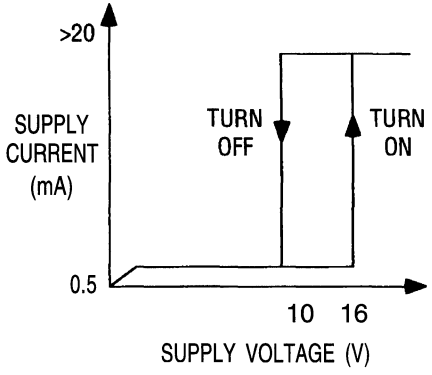

Figure 4 - 16/10V UVLO Thresholds-Off Line Power Supplies

SELF BIASING, ACTIVE LOW OUTPUTS DURING UV LOCKOUT

Another enhancement to the new UC3823A,B and UC3825A,B controllers is found in the output stages. During undervoltage lockout almost all internal functions of the control IC are disabled, primarily to obtain a low startup current. Generally, this would result in little or no available bias to actively keep the outputs low during this power-up condition, when it's needed the most. Outputs are in a high impedance state which is typically about 1 megohm. As the DC (bulk) high voltage rises, a capacitive divider is formed at the MOSFET switch between the drain-to-gate and the gate-to-source capacitances. A quickly rising bulk supply can couple a problematic gate drive command to any FET driven without a gate pull down circuit. Since the control IC is below its turn on threshold, the unbiased output drivers of older PWMs cannot prevent the switch from turning on under these circumstances.

One solution to prevent this parasitic turn-on during undervoltage lockout is to incorporate an active low, self biasing totem-pole design in the driver output. As shown in figure 5, a PNP drive transistor (Q2) is connected between the output pin of the IC and the lower NPN output transistor (Q3). As the output voltage rises, transistor Q1 is biased on through the 50K ohm resistance. This causes the base of Q2 to go low, turning Q2 on. The output pin supplies drive bias to the main totem-pole transistor, Q3, directly through the saturated PNP. Increasing voltage on the output pin provides more drive to transistors Q1, Q2 and Q3. The saturation voltage of this circuit at moderate currents (10mA) is well below the turn on thresholds of the power switching MOSFETs. This circuit is removed from operation once the undervoltage lockout requirements have been satisfied. Transistor Q4 is turned on with a valid UVLO which voids the possibility of transistor Q1 from ever turning on during normal operation. Additionally, a 250 microamp current source from Vcc keeps the PNP predriver (Q2) off after UVLO.

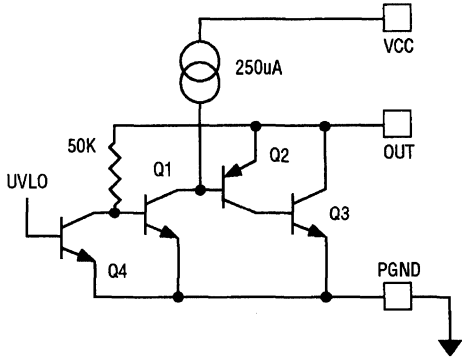

Figure 5 - UVLO Self Biasing Outputs

Another benefit of this technique is obtained during power down. As the IC crosses below its lower UVLO threshold, the self biasing circuitry is enabled. Any residual voltage on the output will similarly turn the totempole stage on which actively pulls the output low. This feature insures correct gate drive operation regardless of the turn off sequence.

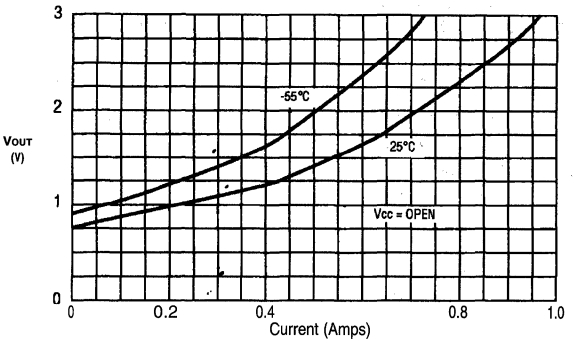

Figure 6 - Output V and I During UVLO

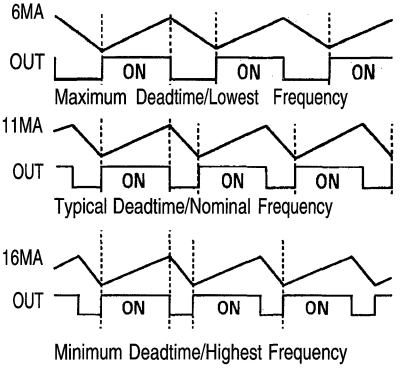

Figure 7 - Frequency and Deadtime Variations vs. Discharge Current Tolerances

OSCILLATOR ACCURACY

Fundamental to the design of any switchmode converter is maintaining an accurate switching frequency. The UC3823A/B and UC3825A/B ICs utilize two pins for the sawtooth oscillator; one each for the timing resistor (Rt) and timing capacitor (Ct). The resistor programs the charging current to the timing capacitor via an internal current mirror with high accuracy. Maximum switch on-time is determined by the rising capacitor voltage whereas deadtime, the programmed switch off time is determined by the timing capacitors discharge.

Considerable improvement has been made to the accuracy of the oscillator discharge current. The previous generation of UC3823/25 devices endured variations of plus or minus forty percent (+/- 40%) over the full military temperature range and production tolerances. This new generation of UC3823A/B and UC3825A/B PWM controllers features a well controlled oscillator discharge current which is "trimmed" at wafer probe testing to +/- 1 milliamp. Oscillator initial accuracy (400 KHz nominal) has been tightened to 375 KHz minimum and 425 KHz maximum. Total variation over all line and temperature ranges is limited to 350 and 450 KHz. A new specification for 1 MHz accuracy has been added, demonstrating a plus or minus fifteen percent total frequency variation at high frequency.

CLOCK OUTPUT

The UC3823A,B and UC3825A,B controllers also feature a TTL/CMOS compatible CLOCK output pin. Specified amplitudes are 3.7 volts in the high (off) state and 0.2 volts during its low state. Additionally, this pin is also used for programming of the leading edge blanking function. Notice that unlike their non A,B predecessors, these enhanced versions cannot be externally synchronized by an input to the clock pin. Synchronization is obtained by forcing a SYNC pulse across a resistor in series with the timing capacitor.

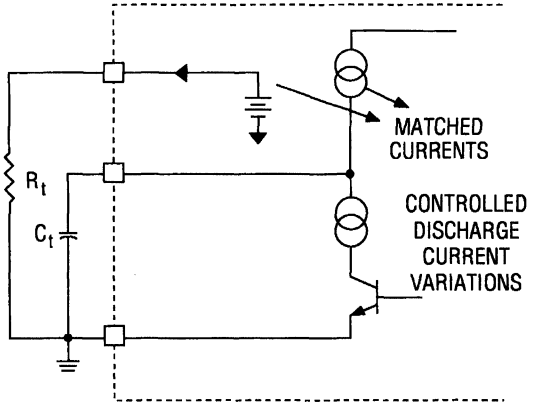

Figure 8 - Controlled Discharge Current

LEADING EDGE NOISE IN THE CURRENT SENSING CIRCUIT

One of the most difficult tasks with peak current mode control is sensing the inductor current. Instead, switch current is generally sensed by means of either a series resistor or current sense transformer. There is some difficulty with using this technique accurately, especially at light current levels. As the switch turns on, circuit parasitics in the power stage, output rectifier reverse recovery characteristics and high current gate drive pulses can create significant noise pulses on the leading edge of the current sense signal. Traditionally, this problem has been overcome by adding a small R-C noise filter between the current sense resistor and the PWM controllers current sense input. At low operating frequencies and high output current levels this R/C filtering technique will generally deliver satisfactory results. However, at higher switching frequencies, and almost always at lighter load currents the leading edge spike amplitude can greatly exceed the peak current sense signal.

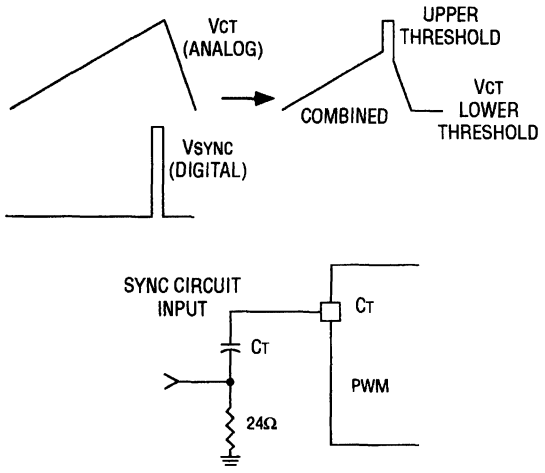

Figure 9 - Synchronization

The leading edge current sense noise shown in figure 10 will cause a premature, false triggering of the pulse width modulator. Additionally, this will lead to instability of the converter by causing the voltage loop to oscillate at light loads. When the PWM is triggered by the noise spike instead of the true current signal - a smaller (minimum) pulse width is delivered to the main switch. The power supply's output voltage subsequently falls which causes the voltage amplifier to command for a higher inductor (switch) current. Eventually this continues until the amplitude is sufficient to rise above the leading edge noise spike.

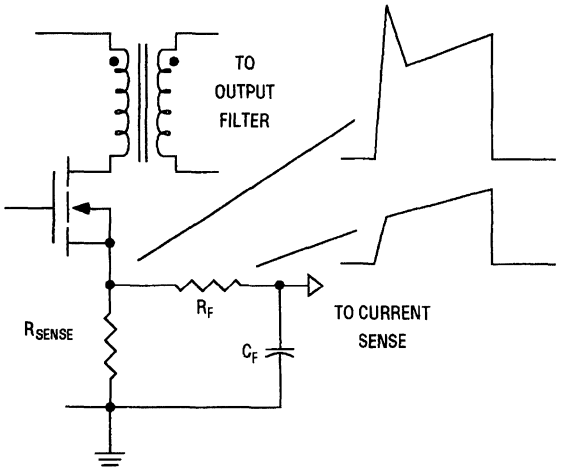

Figure 10 - Current Sensing Technique

Pulse widths too wide for proper operation are now delivered and the output voltage climbs until the voltage amplifier commands less current. This oscillatory process continues at a rate determined by several factors. Noteworthy is that this has nothing at all to do with the instability caused by inadequate slope compensation, or peak-to-average current error. The cause is leading edge noise, and even optimal loop compensation cannot protect against this problem.

LEADING EDGE BLANKING

The RC filter shown in figure 10 can be tailored to work well over a limited range of applications and power levels. Another technique, known as Leading Edge Blanking (LEB) essentially blindfolds (blanks) the PWM comparator for a specific amount of time during the beginning of the cycle. The blanking duration is user programmable and should correspond to the width of the leading edge noise spike. This eliminates the need for filtering of the current sense signal in peak current mode controlled circuits.

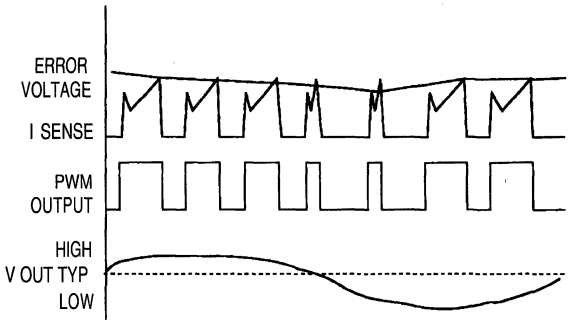

Figure 11- Instablity Caused By Leading Edge Noise Triggering

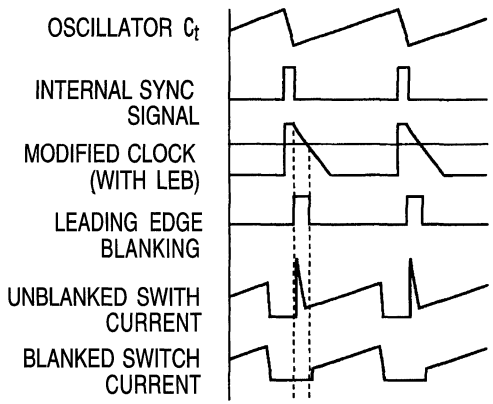

Figure 12 - Leading Edge Blanking Operational Waveforms

LEB IMPLEMENTATION

The focal point of any fixed frequency PWM controller is its clock. Used to accurately program the switching frequency and maximum duty cycle, the clock serves as the trigger source for the leading edge blanking circuitry. A digital representation of the timing capacitor charge/discharge status is developed by internal logic. This is made available at the PWMs CLOCK pin for external purposes. The UC3823A,B and UC3825A,B all use a high output to indicate the OFF period of the switching cycle, and a low to indicate the maximum ON time. These levels will be incorporated into the design of the leading edge blanking circuitry.

The clock output of the UC3823A,B and UC3825A,B is pulled high during the oscillator deadtime to approximately 4 volts. A capacitor added to the CLOCK output pin programs the leading edge blanking duration. An internal comparator with an accurate threshold set at 60% of the peak clock amplitude has been added. The LEB programming capacitor is discharged by an internal 10K ohm resistance to ground. The LEB interval is defined by the time required for the capacitance to discharge from 4 volts to the 60% threshold. Once the LEB capacitor discharges below this threshold, the PWM operates normally without any blanking. Programming should accommodate the worst case of leading edge noise. With no programming capacitor added, the ICs function similarly to their predecessors and provide no blanking.

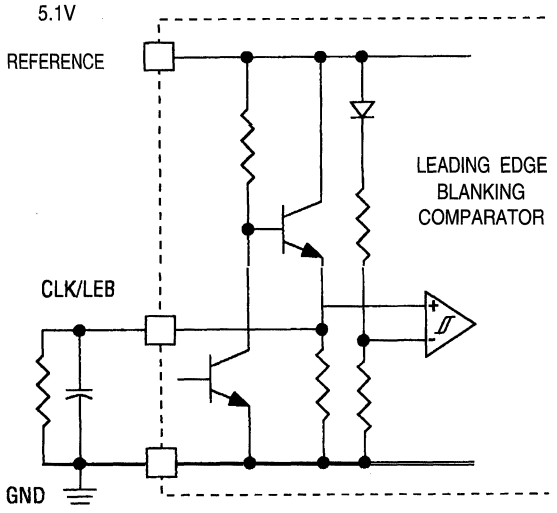

Figure 13 - LEB Circuitry

Because of the leading edge blanking, the PWM outputs will exhibit a minimum ON time in normal operation. The duration corresponds directly to that of the LEB programming, so a minimum duty cycle has also been established. Resolution between zero duty cycle and this minimum duty cycle cannot be obtained - which should also be taken into account when programming the LEB circuitry.

Zero duty cycle is a valid operating condition which can be achieved by one of two methods. The most obvious technique is to bias the error amplifier such that its output is driven below the PWM zero duty cycle threshold of 1.1V. The ICs error amplifier can easily accomplish this while sinking current up to 1 mA, worst case. The second technique utilizes the current limiting feature (ILIM) at pin 9. An ILIM input held above the 1.2V (typ) FAULT threshold will force the PWM's on-time and duty cycle to zero. More details of the interface between the PWM and fault circuitry will be found in the following fault protection section.

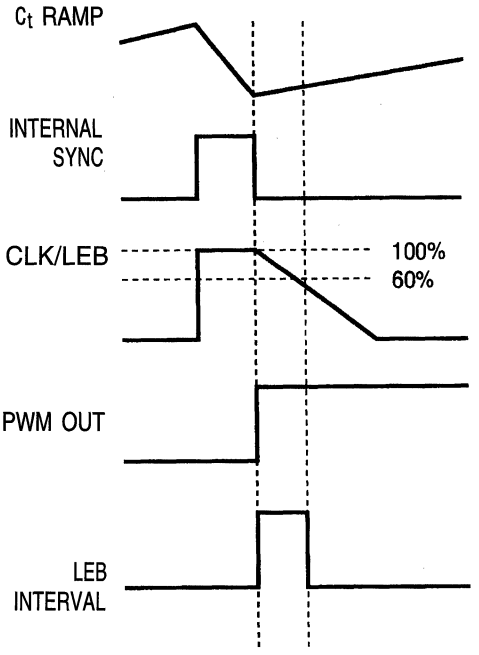

Figure 14 - Blanking Waveforms

LATCHED FAULT PROTECTION

While the previous generation of control ICs offered fault protection circuitry, they did not feature a fully latched shutdown after detecting a fault. The unlatched technique only

discharges the soft start capacitor during the duration of the fault - a duration which can be very brief with a high speed controller. As a result, the duty cycle is not significantly reduced, and the IC continues delivering output pulses at the the switching frequency. Typically, the switching components can easily be dangerously overstressed while also dissipating a significant amount of power.

The new UC3823A,B and UC3825A,B controllers feature a latched fault protection circuit as shown in figure 15. Two comparators are used to offer two stage protection - depending on the amplitude of the fault. The first comparator has a one volt threshold for cycle-by-cycle current limiting. In normal operation this terminates the immediate switch drive pulse but does not trigger the latching fault logic. One volt has been selected as the peak amplitude of the current sense signal for normal operation and slight overloads to accommodate transients.

The second comparator has a slightly higher threshold of 1.20 volts, indicative of a twenty percent overload or fault. When this comparator is tripped, the fault latch is turned on and the soft start capacitor begins discharging. The present output pulse had already been terminated by the one volt comparator circuity while the signal was rising to cross the 1.20 volt level. The over- current latch insures that the PWM latch is held off for an extended period of time, approximately equal to the soft start time constant.

Once this overcurrent latch is set, a second "restart" latch is triggered which insures the proper restart of the control logic. First, a current sink (typically 200 uA) is turned on by the restart latch output which overpowers the 9 uA charging current source and begins discharging the soft start capacitor. The capacitor voltage is monitored by a restart comparator, looking for a decay to the threshold level of 0.2 volts. Once this occurs, the restart comparator resets the overcurrent comparator which sequentially resets the restart latch.

The restart latch can only be set with the right set of conditions as shown in the block diagram. First, undervoltage lockout must be satisfied to insure proper operation during initial power-up. Secondly, the overcurrent (1.2 V) comparator must be triggered, indicative of a valid fault. Last, and most important, is that a full soft start cycle must be completed before the restart latch can be retriggered. A fourth comparator insures that the soft start capacitor voltage has charged to a 5 volt threshold. This indicates that a complete discharge followed by a complete charge has occurred.

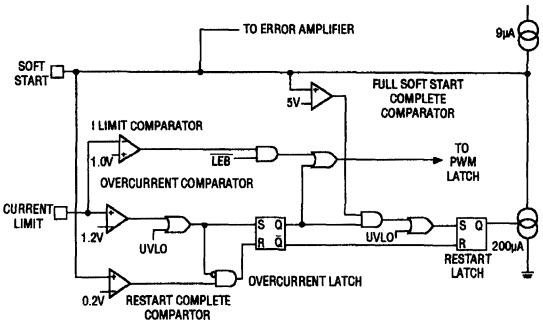

Figure 15 - Latched Fault And Full Cycle Soft Start Protection Circuitry

FULL CYCLE / CONTINUOUS FAULTS

During a fault, many designers prefer to reduce the repetition rate at which the switch is driven rather than to continue at the normal switching frequency. Often called "hiccup", this delayed restart will significantly reduce the overstress and power dissipated during abnormal conditions. Implementation of the latched fault technology results in significantly lower power dissipation during a continuous fault or shorted output stage. Instead of delivering minimum duty cycle pulses at the oscillator frequency, the retry sequence occurs at a repetition rate approximately equal to the soft start period with a continuous fault.

In the worst case, two PWM outputs can occur in a time less than the soft start time constant, but this happens only once with a 'true" fault input (>1.2 V). For example, assume that the converter is in normal operation when a fault is detected. The first valid fault immediately turns off the output and triggers the latching overcurrent circuitry. Since the soft start capacitor was fully charged (above 5 volts), the "full soft start complete" comparator allows the overcurrent latch to set the restart latch. Discharge begins and continues until the restart complete comparator is tripped at a soft start capacitor voltage of 0.2 volts. The restart latch is reset, and the soft start capacitor begins charging.

Note that a well defined time is required between this instant and the time when the first output pulse can next occur. The capacitor begins at 0.2 volts and the error amplifier output is internally clamped to the soft start capacitor voltage. Back at the PWM comparator, however, there is a 1.25 volt offset on the ramp pin to facilitate zero duty cycle. Therefore, the soft start capacitor must charge from 0.2 volts to 1.25 volts before the PWM comparator is active.

This provides a slight interval between the worst case of successive output pulses into a shorted load. From this point on, the soft start capacitor must fully charge up to the five volt threshold of the "full soft start complete" comparator. Once in this mode, only one PWM output per soft start period can be obtained into a fault as shown in figure 16.

LEB AND FAULT DETECTION

The leading edge blanking circuitry is interfaced to also blank some of the fault detection circuitry. While numerous arrangements are possible, only one configuration offers a reasonable compromise between quick response and noise immunity. As demonstrated in figure 12, leading edge blanking does inhibit the one volt, cycle-by-cycle current limit comparator during the programmed interval. However, the blanking does not disable the 1.2 volt overcurrent comparator and fault logic. This adaptation will accommodate a moderate amount of leading edge noise without having to significantly filter the current sense, and fault signals. Even if a moderate amount of filtering is required, the latched full cycle shutdown protection minimizes the power dissipation.

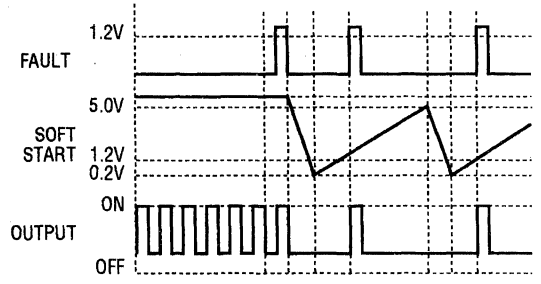

Figure 16 - Full Cycle Soft Start - Operational Waveforms

TIGHTER FAULT THRESHOLDS

This latest generation of IC controllers utilizes a thin film resistor process which provides improved control of the tolerance. These resistors are used to generate accurate voltage thresholds by dividing down the IC's reference voltage internally. Both of the current limiting comparator thresholds have been tightened in the "A" and "B" versions of controllers. The cycle-by-cycle current limit threshold range has been tightened to +/- 5% from its previous +/- 10% specification. The new limits are 0.95V minimum, 1.05V maximum with the center remaining at the previous 1.0 volts.

The overcurrent (fault) threshold, however, has been centered at 1.2 volts instead of the 1.4 volt midpoint of the non A,B versions. The new specifications are 1.14 volts minimum to 1.26 volts maximum. Applications converting to the newer controllers may need to adjust the current sense resistor value accordingly. Typical propagation delay is unchanged at 50 ns typical, and 80 ns maximum.

HIGHER GAIN BANDWIDTH ERROR AMPLIFIER

Many of the critical UC3823/25 error amplifier specifications have been improved. The characteristics which significantly differ are: input offset voltage - reduced from 10 to 7 mV, unity gain bandwidth - increased from 5.5 MHz to 9 MHz, typical slew rate - reduced from 12 to 9 V/us. Notice that the minimum slew rate is unchanged at 6 V/us.

HIGH POWER OUTPUTS

The industry need for higher switching frequencies and improved efficiency has directly effected the design of the totem-pole output drivers. Many of the capacitive loads (MOSFETS) placed directly on the PWM outputs require high peak currents to obtain adequate switching transitions. The high speed UC3823A,B and UC3825A,B controllers feature peak current ratings of 2 amps, and are capable of slewing 15 volts in 35 nanoseconds into 1000pF Separate collector supply (Vc) and power ground connections (PGND) help decouple the analog circuitry from the high power gate drive noise.

TYPICAL APPLICATION

The 1.5 MHz, 50 Watt push-pull converter detailed in Application Note U-110 was redesigned to accept the UC3825"B" device. The basic power stage remained similar while an emphasis was placed on control circuit improvements. These enhancements included Leading Edge Blanking of the current sense signal and Restart Delay following a fault. Also, a current sense transformer was installed which not only reduced losses but allowed amplification of the current sense signal to approximately 2.5 volts, thus enhancing noise immunity.

Improvements to the power section of the converter include the use of larger MOSFETS (IRF640's) and the addition of a bootstrap winding for the auxiliary bias supply. The startup resistor from the input supply was increased since the UC3825"B" device features a wide UVLO hysterisis of six volts.

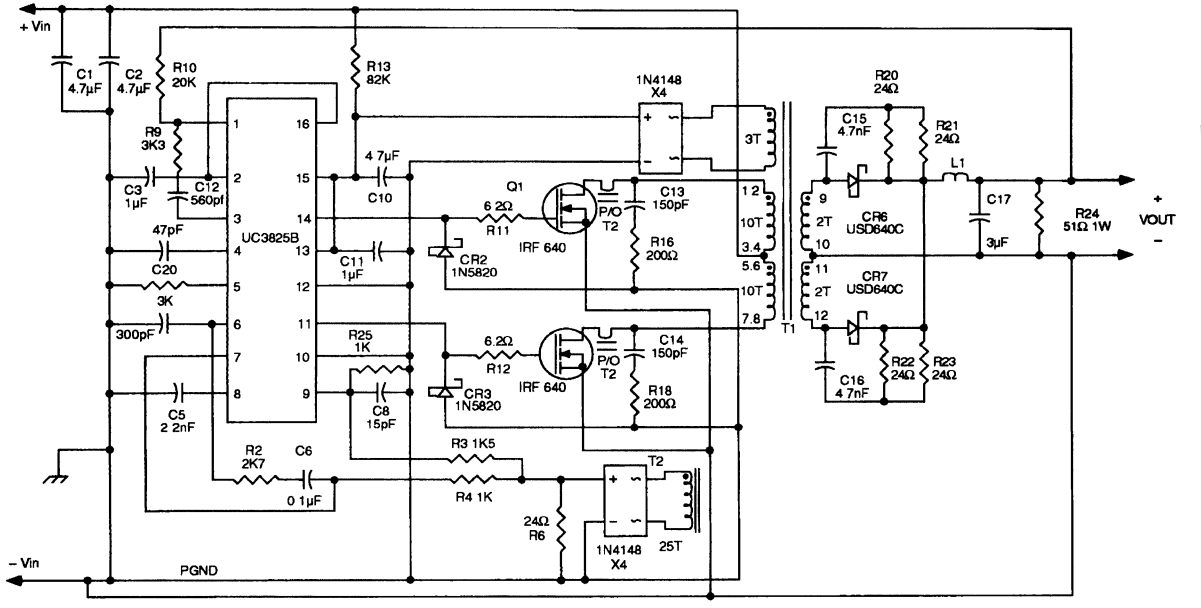

Figure 17 UC3825B Controlled 1.5 MHz Push Pull Converter

CONVERTER PERFORMANCE

The redesigned converter exhibited similar line, load and transient response to the original converter, which was excellent due to the high conversion frequency. A significant improvement was made in the short circuit performance by comparison. While operating into a continuous short circuited output, the UC3825"B" controlled version reduced the converter input power (and dissipation) to approximately one-hundredth of the original design. Featuring the programmable Restart Delay circuitry, the redesigned 50 Watt converter draws only one-quarter of a Watt (1/4 W) of input power with a shorted circuited output.

SUMMARY

This new generation of UC3823A,B and UC3825A,B PWM controllers features a multitude of performance advantages over its predecessors. Higher precision, increased protection and programmable new functions are just a few of the benefits obtainable with these enhanced versions of PWMs. And as the level of sophistication in todays power supplies increases, so too must that of its components - especially control ICs. Containing an expanded list of integrated features, this new era of enhanced UC3823A,B and UC3825A,B controllers overcomes the challenges of the power supply industry for higher levels of power, protection and performance.

ADDITIONAL INFORMATION AND REFERENCES

1. New Pulse Width Modulator Chip Controls 1 MHz Switchers; UNITRODE Application Note # U-107
2. 1.5 MegaHertz Current Mode IC Controlled 50 Watt Power Supply; UNITRODE IC Databook, Application Note # U-110
3. "Practical Considerations in Current Mode Power Supplies"; UNITRODE IC Databook, Application Note # U-111

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UCC 3800/1/2/3/4/5 BiCMOS CURRENT MODE CONTROL ICs

BILL ANDREYCAK

INTRODUCTION

Power supply design has become increasingly more challenging as engineers confront the difficulties of obtaining higher power density, improved performance and lower cost. The control for many of these switchmode supplies was revolutionized with two significant introductions; an advance technique known as current mode control, and a novel PWM solution, the UC3842 controller. This IC contained several innovative features for general purpose current mode controlled applications. Included were high speed circuitry, undervoltage lockout, an op-amp type error amplifier, fast overcurrrent protection, a precision reference and a high current totem-pole output.

The popular UC3842 control circuit architecture has been recently improved upon to deliver even higher levels of protection and performance. Advanced circuitry such as leading edge blanking of the current sense signal, soft-start and full cycle restart have been built-in to minimize external parts count. Additionally, these integrated circuits have been developed on a BiCMOS wafer fabrication process geared to virtually eliminate supply power and propagation delays in comparison to the bipolar UC3842 devices. These sophisticated new BiCMOS controllers, the UCC3800 through UCC3805 pulse width modulators address the challenges presented by the upcoming generations of power supply designs. This application note will highlight the features incoporated into this new generation of PWM controllers in addition to realizeable enhancements in typical applications. The specific differences between members of the UCC3800/1/2/3/4/5 family are reflective of their maximum duty cycle, undervoltage lockout thresholds and reference voltage which are summarized in the following table.

Unitrode Part #	Max Duty Cycle	VRef (V)	UVLO Turn-On	UVLO Turn-Off
UCC3800	100%	5.0	7.2	6.9
UCC3801	50%	5.0	9.4	7.4
UCC3802	100%	5.0	12.5	8.4
UCC3803	100%	4.0	4.1	3.6
UCC3804	50%	5.0	12.5	8.4
UCC3805	50%	4.0	4.1	3.6

UCC3800/1/2/3/4/5 PWM FEATURES

A. Low start-up current
B. Undervoltage lockout
C. Low operating current
D. Internal soft start
E. Self biasing output during UVLO
F. Leading Edge Blanking
G. Self regulating Vcc supply
H. Full cycle restart after fault
I. Clamped gate drive amplitude
J. Reduced propagation delays
K. 5 Volt operation (UCC3803 & 05)

IN-CIRCUIT ADVANTAGES vs. UC3842

- Greatly reduced power requirements
- Eliminates bootstrap supply
- Fewer external components
- Lower junction temperature
- Reduced stress during faults
- No current sense R/C filter network
- Faster response to fault
- Higher frequency operation
- Higher maximum duty cycles

UCC3800/1/2/3/4/5 DEVICE OVERVIEW

The BiCMOS UCC3800/1/2/3/4/5 devices have similar standard features and pinouts to the bipolar UC3842/3/4/5 PWMs and are enhanced replacements in many applications. There are a few important differences however which may require minor modifications to existing applications.

APPLICATION DIFFERENCES

1. Maximum supply voltage from a low impedance source: 12V versus 30V
2. Undervoltage lockout thresholds
3. Start-up current
4. Operating current
5. Oscillator timing component values
6. Reference voltage (UCC3803 and 05)
7. Vcc supply self clamping zener voltage
8. Internal soft start
9. Internal full cycle restart
10. Clamped gate drive voltage
11. Current loop gain
12. E/A reference voltage ('03 & '05)

UCC3800/1/2/3/4/5 BLOCK DIAGRAM

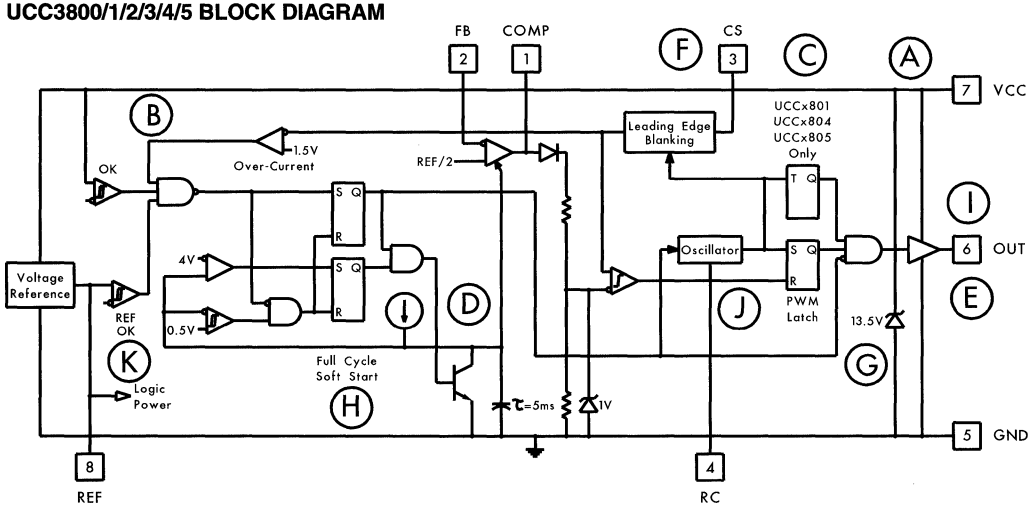

Figure 1.

SUPPLYING POWER

An internal Vcc shunt regulator is incorporated in each member of the UCC3800/1/2/3/4/5 PWMs to regulate the supply voltage at approximately 13.5 volts. A series resistor from Vcc to the input supply source is required with inputs above 12 volts to limit the shunt regulator current as shown in figure 2. A maximum of 10 milliamps can be shunted to ground by the internal regulator.

The internal regulator in conjunction with the device's low startup and operating current can greatly simplify powering the device and may eliminate the need for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and needs no external zener diode or regulator protection with a current limited input supply. The UVLO start-up threshold is 1.0 volts below the shunt regulator level on the '02 and '04 devices to guarantee start-up.

It is important to bypass the ICs supply (Vcc) and reference voltage (Vref) pins with a 0.1uF to 1uF ceramic capacitor to ground. The capacitors should be located as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in off-line applications to hold the supply voltage (Vcc) above the UVLO turn-off threshold during start-up.

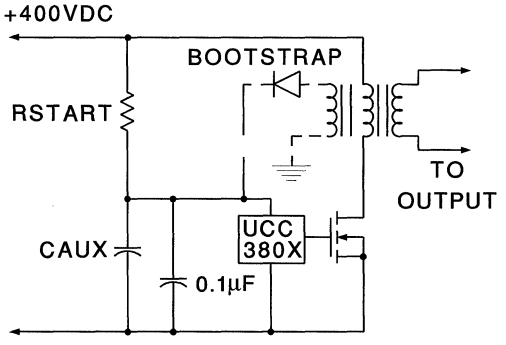

Figure 2. Powering the UCC3802.

UNDERVOLTAGE LOCKOUT

The UCC3800/1/2/3/4/5 devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (Vcc) and the reference voltage (Vref) are monitored by the UVLO circuitry. An active low, self biasing totem pole output during UVLO design is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCC 3802/3/4/5 devices are different from the previous generation of UC3842/3/4/5 PWMs. Basically, the thresholds are optimized for two groups of applications; off-line power supplies and DC-DC converters. The UCC3802 and UCC3804 feature typical UVLO thresholds of 12.5V for turn-on and 8.3V for turn-off, providing 4.3V of hysteresis. For low voltage inputs which include battery and 5V applications, the UCC3803 and UCC3805 turn on at 4.1V and turn off at 3.6V with 0.5V of hysteresis. The UCC3800 and UCC3801 have UVLO thresholds optimized for automotive and battery applications.

During UVLO the IC draws approximately 100 microamps of supply current. Once crossing the turn-on threshold the IC supply current increases typically to about 500 microamps, over an order of magnitude lower than bipolar counterparts.

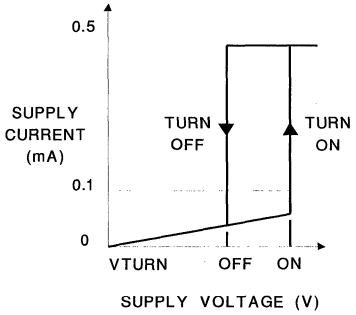

Figure 3. During Undervoltage Lockout

Device	Vton	Vtoff
UCC3800	7.2	6.9
UCC3801	9.4	7.4
UCC3802, 4	12.5	8.3
UCC3803, 5	4.1	3.6

SELF BIASING, ACTIVE LOW OUTPUT

The self biasing, active low clamp circuit shown eliminates the potential for problematic MOSFET turn on. As the PWM output voltage rises while in UVLO, the P device drives the larger N type switch ON which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the ICs supply voltage during undervoltage lockout.

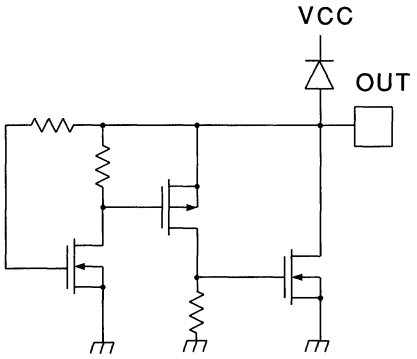

Figure 4: Internal circuit which holds output low during UVLO.

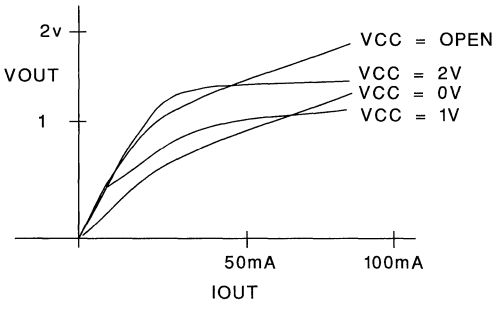

Figure 5: Output voltage vs. output current during UVLO.

REFERENCE VOLTAGE

The traditional 5.0V amplitude bandgap reference voltage of the UC3842 family can be also found on the UCC3800,1,2 and UCC3804 devices. However, the reference voltage of the UCC3803 and UCC3805 device is 4.0 volts. This change was necessary to facilitate operation with input supply voltages below five volts. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO which can be used as a UVLO status indication.

REFERENCE DIFFERENCES

Note that the 4V reference voltage on the UCC3803 and UCC3805 is derived from the supply voltage (Vcc) and requires about 0.5V of headroom to maintain regulation. Whenever Vcc is below approximately 4.5V, the reference voltage also will drop outside of its specified range for normal operation. The relationship between Vcc and Vref during this excursion is shown in Figure 7.

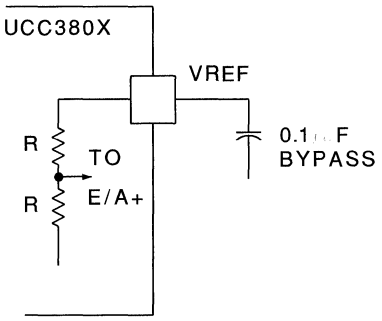

Figure 6: Required reference bypass.

The noninverting input to the error amplifier is tied to one-half of the PWMs reference voltage, Vref. Note that this input is 2.0V on the UCC3803 and UCC3805 and 2.5V on the higher reference voltage parts, the UCC3800, UCC3801, UCC3802 and UCC3804.

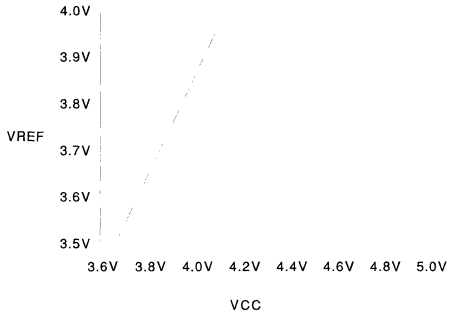

Figure 7: UCC3803 VREF output vs. VCC.

OSCILLATOR SECTION

The oscillator section of the UCC3800 through UCC3805 BiCMOS devices has few similarities to the UC3842 type — other than single pin programming. It does still utilize a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values will need to be changed since a much lower charging current is desirable for low power operation.

Several characteristics of the oscillator have been optimized for high speed, noise immune operation. The oscillator peak to peak amplitude has been increased to 2.45V typical versus 1.7V on the UC 3842 family. The lower oscillator threshold has been dropped to approximately 0.2 volts while the upper threshold remains fairly close to the original 2.8 volts at approximately 2.65V.

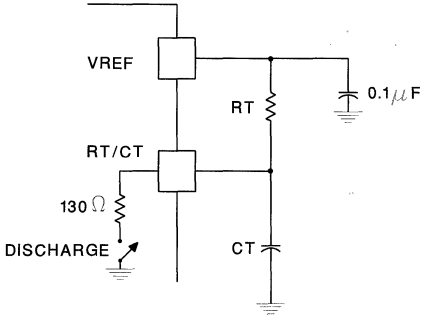

Figure 8: Oscillator equivalent circuit.

Discharge current of the timing capacitor has been increased to nearly 20 milliamps peak as opposed to roughly 8mA. As shown, this can be represented by approximately 130 ohms in series with the discharge switch to ground. A higher current was necessary to achieve brief deadtimes and high duty cycles with high frequency operation. Practical applications can utilize these new ICs to a 1 MHz switching frequency.

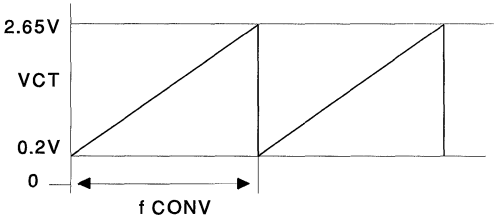

Figure 9: OSC Waveform

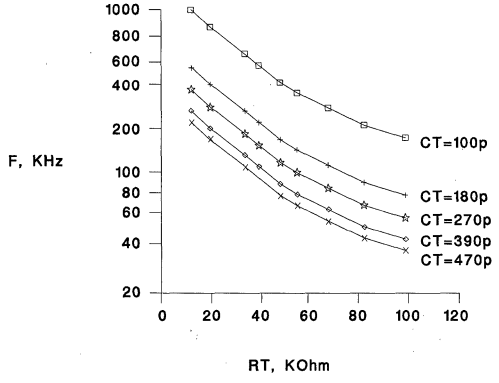

Figure 10: Oscillator frequency vs. RT for several CT.

SYNCHRONIZATION

Synchronization of these PWM controllers is best obtained by the universal technique shown in figure 12. The ICs oscillator is programmed to free run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the 50Ω resistor to force synchronization. Typically, a one volt amplitude pulse of 100 nanoseconds width is sufficient for most applications.

The ICs can also be synchronized to a pulse train input directly to the oscillator Rt/Ct pin. Note that the IC will internally pull low at this node once the upper oscillator threshold is crossed. This 130 ohm impedance to ground remains active until the pin is lowered to approximately 0.2 V. External synchronization circuits should accommodate these conditions.

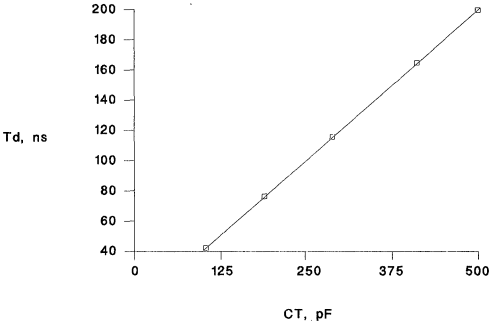

Figure 11: Minimum dead time vs. CT.

PWM SECTION : MAXIMUM DUTY CYCLE

Maximum duty cycle is higher for these devices than for their UC3842/3/4/5 predecessors. This is primarily due to the higher ratio of timing capacitor discharge to charge current which can exceed one-hundred to one in a typical BiCMOS application. **Attempts to program the oscillator maximum duty cycle much below the specified range by adjusting the timing component values of Rt and Ct should be avoided.** There are two reasons to refrain from this design practice. First, the ICs high discharge current would necessitate higher charging currents than necessary for programming,

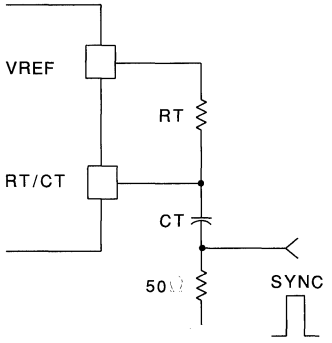

Figure 12: Synchronizing the oscillator.

defeating the purpose of low power operation. Secondly, a low value timing resistor will prevent the capacitor from discharging to the lower threshold and initiating the next switching cycle.

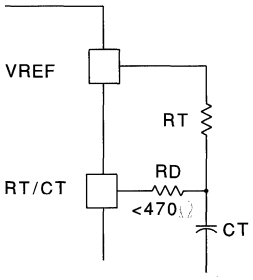

Figure 13: Circuit to produce controlled maximum duty cycle.

DEADTIME CONTROL

Deadtime is the term used to describe the guaranteed OFF time of the PWM output during each oscillator cycle. It is used to insure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation.

The deadtime of the UCC380x PWM family is determined by the internal 130 Ohm discharge impedance and the timing capacitor value. Larger capacitance values extend the deadtime whereas smaller values will result in higher maximum duty cycles for the same operating frequency. A curve for deadtime versus timing capacitor values is provided in figure 11.

Increasing the deadtime is possible by adding a resistor between the Rt/Ct pin of the IC and the timing components. The deadtime increases with the discharge resistor value to about 470 Ohms as indicated from the curve. Higher resistances should be avoided as they can decrease the deadtime and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing Rt will "freeze" the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V.

Reducing the maximum duty cycle can be accomplished by adding a discharge resistor (below 470 Ohms) between the ICs Rt/Ct pin and the actual Rt/Ct components. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge – but not the charging portion of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude.

Because of the reduced peak-to-peak amplitude, the exact value of Ct may need to be adjusted from UC3842 type designs to obtain the correct initial oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values since these are readily available in finer numerical increments.

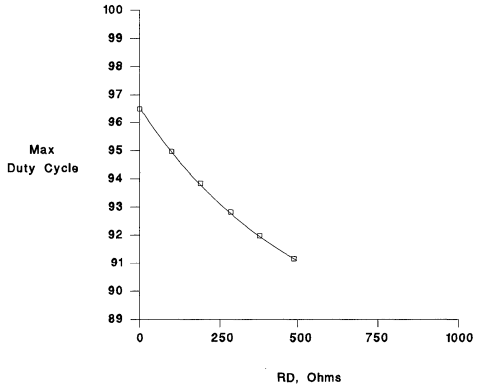

Figure 14: Maximum duty cycle vs. RD for RT = 20k.

LEADING EDGE BLANKING

A 100 nanosecond leading edge blanking interval is applied to the current sense input circuitry of the UCC3800/1/2/3/4/5 devices. This internal feature has been incorporated to eliminate the need for an external resistor-capacitor filter network to sup-

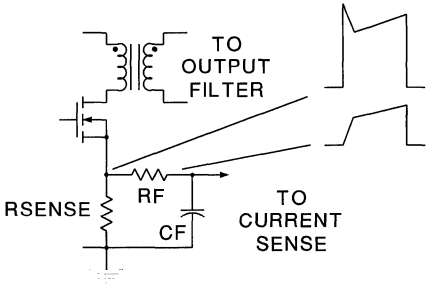

Figure 15: Current sense filter required with older PWM ICs.

press the switching spike associated with turn-on of the power MOSFET. This 100 nanosecond period should be adequate for most switchmode designs but can be lengthened by adding an external R/C filter.

Note that the 100 ns leading edge blanking is also applied to the cycle-by-cycle current limiting function in addition to the overcurrent fault comparator.

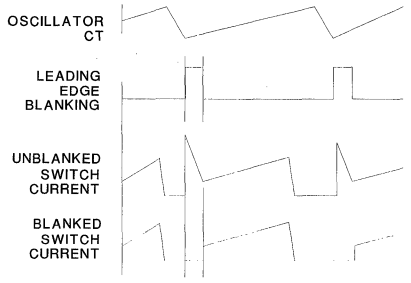

Figure 16: Current sense waveforms with leading edge blanking.

MINIMUM PULSE WIDTH

The leading edge blanking circuitry can lead to a minimum pulse width equal to the blanking interval under certain conditions. This will occur when the error amplifier output voltage (minus a diode drop and divided by 1.65) is lower than the current sense input. However, the amplifier output voltage must also be higher than a diode forward voltage drop of about 0.5V. It is only during these conditions that a minimum output pulse width equal to the blanking duration can be obtained.

Note that the PWM comparator has two inputs; one is from the current sense input. The other PWM input is the error amplifier output which has a diode and two resistors in series to ground. The diode in this network is used to guarantee that zero duty cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, along with pulse width.

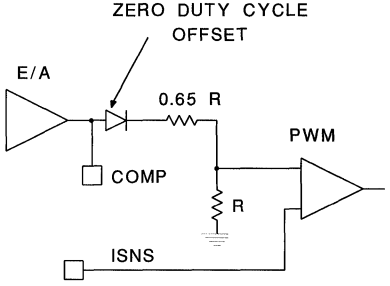

Figure 17.

Zero duty cycle is achievable by forcing the error amplifier output below the zero duty cycle threshold of one diode voltage drop.

PROTECTION CIRCUITRY: CURRENT LIMITING

A 1.0 volt (typical) cycle-by-cycle current limit threshold is incorporated into the UCC3800 family. Note that the 100 nanosecond leading edge blanking pulse is applied to this current limiting circuitry. The blanking overrides the current limit comparator output to prevent the leading edge switch noise from triggering a current limit function.

Propagation delay from the current limit comparator to the output is typically 70 nanoseconds. This high speed path minimizes power semiconductor dissipation during an overload by abbreviating the on time.

CURRENT SENSE OFFSET CIRCUITRY

For increased efficiency in the current sense circuitry, the circuit shown in figure 18 can be used. Resistors RA and RB bias the actual current sense resistor voltage up, allowing a small current sense amplitude to be used. This circuitry provides current limiting protection with lower power loss current sensing.

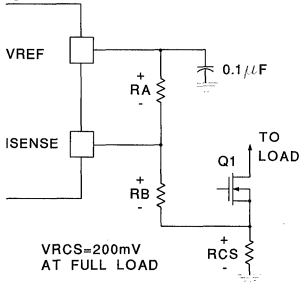

Figure 18: Biasing Isense for lower current sense voltage.

The example shown uses a 200 millivolt full scale signal at the current sense resistor. Resistor Rb biases this up by approximately 700 mV to mate with the 0.9V minimum specification of the current limit comparator of the IC. The value of resistor Ra changes with the specific IC used, due to the different reference voltages. The resistor values should be selected for minimal power loss. For example, a 50 uA bias sets Rb = 13k ohms, Ra=75 k ohms (UCC3800,1,2,4) or Ra=56k ohms with the UCC3803 and UCC3805 devices.

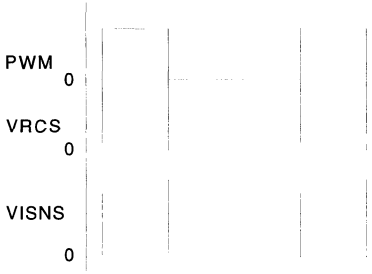

Figure 19.

OVERCURRENT PROTECTION AND FULL CYCLE RESTART

A separate overcurrent comparator within the UCC 3800/1/2/3/4/5 devices handles operation into a short circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5 volt threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft start capacitor to generate a delay before retry is attempted. Often referred to as "hiccup", this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components.

Full Cycle Soft Start insures that there is a predictable delay of greater than 3 milliseconds between successive attempts to operate during fault. The circuit shown in figure 20 and the timing diagram in figure 21 show how the IC responds to a severe fault, such as a saturated inductor. When the fault is first detected, the internal soft start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. When the fault clears, the capacitor will slowly charge and will allow the error amp output (COMP) to rise. When COMP gets high enough to enable the ouput, another fault occurs, latching off the PWM output, but the soft start capacitor still continues to rise to 4V before being discharged and permitting start of a new cycle. This means that for a severe fault, sucessive retries will be spaced by the time required to fully charge the soft start capacitor.

Low leakage transformer designs are recommended in high frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the overcurrent comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short circuit power dissipation of the converter.

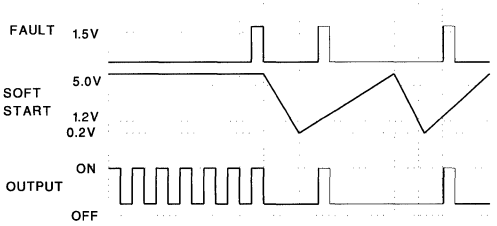

Figure 21.

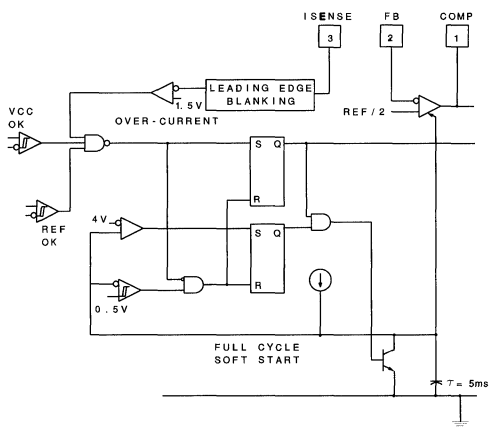

Figure 20.

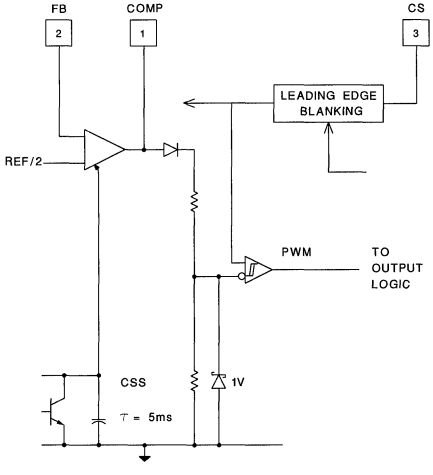

Figure 22.

SOFT START

Internal soft starting of the PWM output is accomplished by gradually increasing error amplifier (E/A) output voltage. When used in current mode control, this implementation slowly raises the peak switch

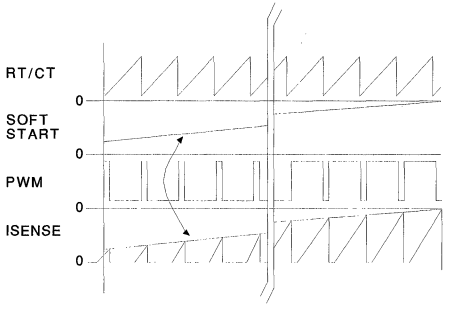

Figure 23.

current each PWM cycle in comparison, forcing a controlled start-up. In voltage mode (duty cycle) control, this feature continually widens the pulse width.

The soft start capacitor (Css) is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of Css occurs whenever the overcurrent protection comparator is triggered by a fault.

Soft start is performed within the UCC3800/-1/2/3/4/5 devices by clamping the E/A amplifier output to an internal soft start capacitor (Css) which is charged by a current source. The soft start clamp circuitry is overridden once Css charges above the voltage commanded by the error amplifier for normal PWM operation.

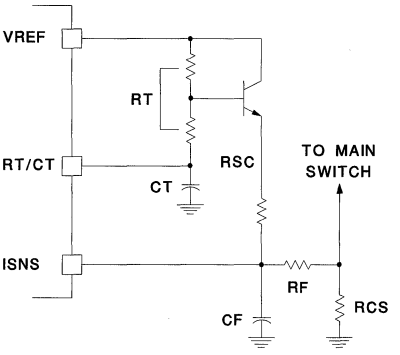

Figure 24: Adding slope compensation.

APPLICATIONS SECTION: CURRENT MODE CONTROL

Peak current mode control is obtained by feeding the converters switch current waveform into the current sense (Isens) input of a UCC3800/1/2/3/4/5 device. The sense resistor should be selected to develop a 0.9 V peak amplitude at full load, including slope compensation. Because of the internal 100 ns typical leading edge blanking, the traditional resistor-capacitor (Rf/Cf) filter to suppress the turn-on noise spike may not be needed.

SLOPE COMPENSATION

Slope compensation can be added in all current mode control applications to cancel the peak to average current error. Slope compensation is neces-

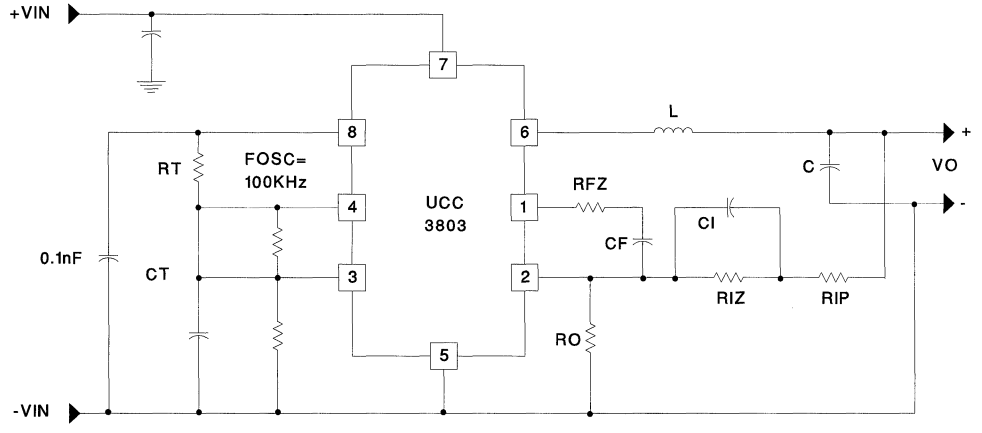

Figure 27: Low-power buck PWM example using on-chip power FETs.

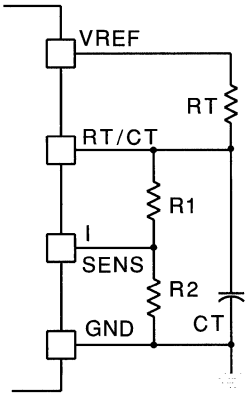

Figure 25: Connecting UCC3802 for voltage mode.

sary with applications with duty cycles exceeding 50%, but also improves performance in those below 50%.

Primary current is sensed using resistor Rcs in series with the converter switch. The timing resistor can be broken up into two series resistors to bias up the NPN follower. This is needed to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous current converters. A NPN voltage follower drives the slope compensating programming resistor (Rsc) to provide a slope compensating current into Cf.

VOLTAGE MODE OPERATION

Any current mode control IC can be used as a direct duty cycle control (voltage mode) by applying a sawtooth ramp to the current sense input. The exponential charging of the timing capacitor (Ct) is used as an approximation of a sawtooth.

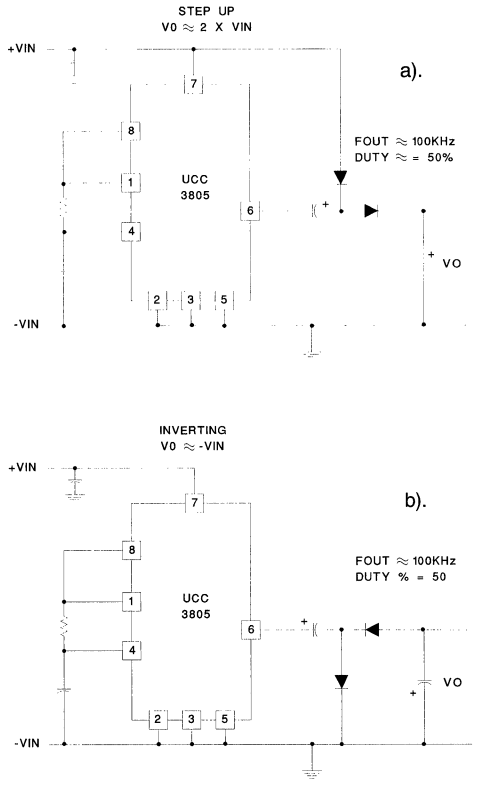

Figure 26: a) Using the UCC3805 to double VIN.
b). Using the UCC3805 to create Vo = –VIN.

The oscillator waveform is resistively divided down by R1 and R2 to a 0.9V maximum amplitude and fed into the current sense input for duty cycle control. A small capacitor across R1 might be necessary to completely bring the current sense input to

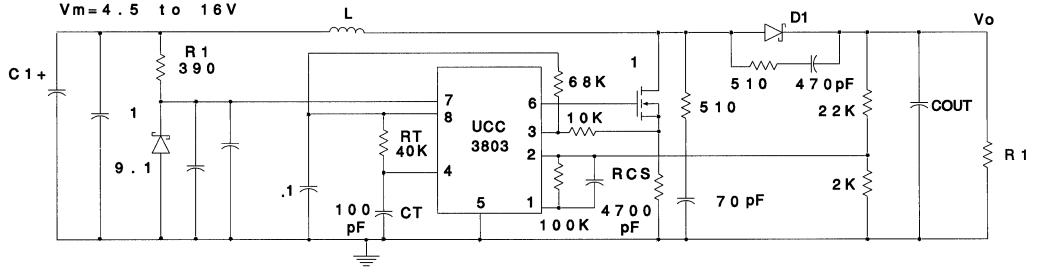

Figure 28: A practical boost PWM example.

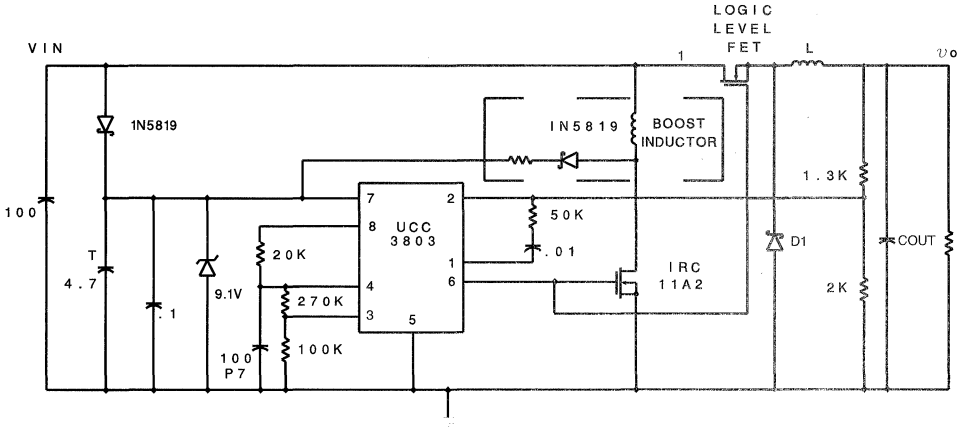

Figure 29: A practical buck PWM that runs with VIN ≥ 4.1V.

zero volts at the beginning of each PWM cycle. Current in the divider network should be kept around 50 microamps, a compromise between low power consumption and good noise immunity. A 15K ohm and 30 K ohm are used in the example.

This circuit can also be used to program the PWM maximum duty cycle. Values should be calculated to attain the 0.9V current sense voltage at the desired maximum duty cycle.

LOW POWER DC/DC CONVERTERS CHARGE PUMP CONVERTERS

Charge pump converters are popular for simple, low power applications. The two basic applications are free running step-up and inverting switchers which use few external components as shown in figure 26.

LOW POWER BUCK REGULATOR

For voltage step down applications, the UCC 380x totem pole output can be used as both the switch and commutating diode of the buck regulator (see figure 27). Power dissipation and the one amp peak current rating of the IC's output stage limit the range of applications to less than 1 amp of output current. High frequency operation permits the use of small and inexpensive surface mount components.

BUCK-BOOST CONVERTER for VOLTAGE STEP-UP and/or STEP-DOWN APPLICATIONS

A two-switch buck-boost converter can be controlled by the UCC380x family of PWMs. This specific

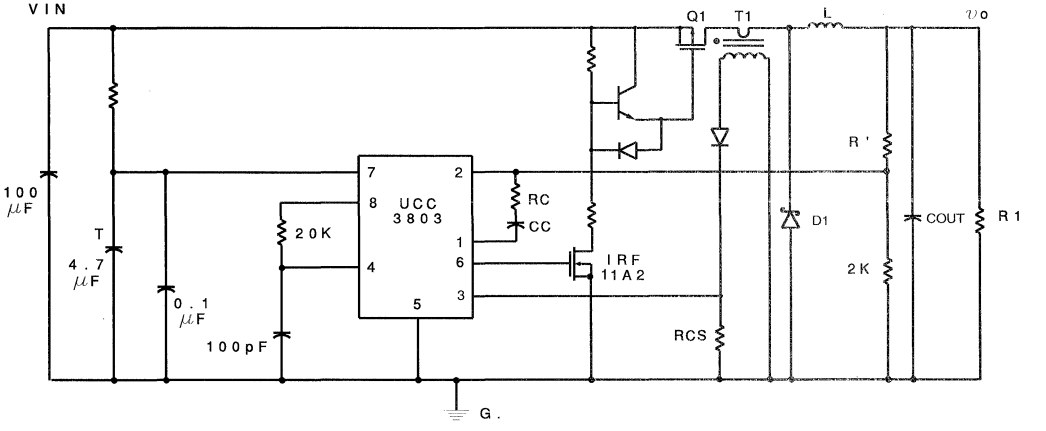

Figure 30: Buck PWM using a PMOS high-side switch.

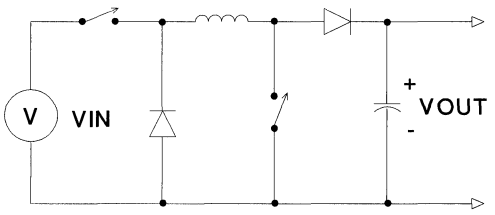

Figure 31. Simplified two switch buck/boost converter drive switches together.

converter is useful in applications where the input voltage can be both higher and lower than the desired output voltage. Implementation combines the voltage step-down characteristic of the buck regulator with the voltage step-up of the boost converter. Both switches are driven simultaneously with this adaptation to simplify the control algorithm. Note that the PWM output of the IC will be used directly for the high side switch in a low power application thus requiring only one external switch. Also, the body diode of the lower side totem-pole output is used as one of the commutating rectifiers, further reducing complexity. As shown in figure 31, this approach is ideal for low voltage, low power DC to DC applications. Higher voltage and higher power applications will require the use of discrete semiconductors for the high side switch and lower diode.

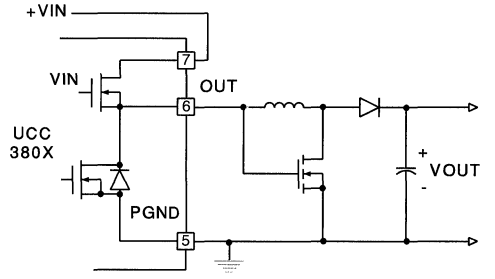

Figure 32. Buck/boost PWM for low power systems.

Duty cycle is varied with input line voltage to provide a regulated output. This non isolated buck-boost converter can be operated in either the discontinuous and continuous inductor current modes. High frequency switching permits the use of very small and inexpensive surface mount inductors for most low power applications. The converter can be controlled by duty cycle modulation (voltage mode) or current mode control, and with or without overcurrent protection.

BOOST CONVERTERS

The UCC 3803 and UCC 3805 devices are fully operational from a 4.5 volt input supply and are ideally suited for 5VDC and battery input PWM boost converter applications. MOSFETs featuring "logic level" gate thresholds are the most likely candidates for the PWM switch as opposed to using standard devices which typically require a gate voltage near 12 volts to be fully on. Currently, many popular N channel MOSFETs are available with logic level gate inputs as an option. Note that many logic level FETs have maximum gate voltage ratings of +/- 10V as opposed to +/- 20V for most conventional FETs which limits their application. Also note that the UCC 380x devices will require a current limited supply when used above 12 volts from a low impedance source.

A basic current mode controlled boost converter application circuit is shown in figure 28. Typical component values for 250 kHz operation are listed in the following tables for a 12V and 24V output applications. The boost converter design equations are summarized below.

BOOST DESIGN SUMMARY:

(Discontinuous inductor current)

$$Vout = Vin \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Iin = Iout \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Ip = 2 \times Iin \times \{ \frac{t(period)}{t(on)}$$

$$Ip = \frac{2 \times t(period) \times Iout \times (t(on) + t(off))}{[t(on) \times t(off)]}$$

$$where\ t(period) = \frac{1}{F(switching}$$

$$L = \frac{Vout\ minus\ Vin(min) \times t(off)]}{Ip}$$

$$C\ out = \frac{(Ip \times t(off))\ max}{2 \times dVout}$$

$$ESR(max) = \frac{dVout}{Ip}$$

BOOST CONVERTER DESIGN TABLE 1

VIN = 4.5 to 10 VDC

VOUT = 12 VDC

IOUT = 0.2, 0.4, 1 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	1.8uH
PCH-	27-123	27-682	27-182
Cout	100uF	300uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 2

VIN = 4.5 to 10 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	3.9uH
PCH-	27-123	27-682	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	8A/50V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 3

VIN = 10 to 18 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	22uH	12uH	3.9uH
PCH-	27-223	27-123	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.2	0.1	0.066
Q1*	3A/60V IRFF113	3A/60V IRFF113	IRFF133

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

BUCK REGULATOR

The buck regulator is a more difficult design challenge than the boost converter due to the high side switch. A transformer coupled gate drive is typically required to deliver drive pulses to the switch, which requires about ten volts above the input voltage for proper drive. Current mode control further complicates the design by requiring a current transformer to level shift the high side current sense signal down to the ground based input of the IC. In many applications, direct duty cycle control (voltage mode) can be used to simplify the design although overcurrent protection is lost with common ground applications.

Several examples of common buck regulator application circuits are shown in figures 29 and 30. Direct duty cycle control is used for simplicity, however current mode control can be easily adapted as shown in the example. Tables listing component values and typical part numbers have been included.

DESIGN EQUATIONS:

$Vout = Vin * D$ (duty cycle)

$$\text{where } D = \frac{T(on)}{T(period)}$$

$$L = Vout \times \frac{t(off)}{d\,Io}$$

where: Delta Io is the inductor ripple current and equal to one-half of the minimum output current. Minimum output current has been selected as 10% of the full load current

$$Ipk = Io + \frac{d\,Io}{2}$$

$Iin(DC) = Iout * D$

$$Cout = \frac{d\,Io}{(8 \times F \times d\,Vout)}$$

where F is the switching frequency and Δ Vout is the output ripple voltage

BUCK REGULATOR DESIGN TABLES

TABLE 4

VIN = 4.5 to 10 VDC

VOUT = 3.3 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/20V 1N5820	6A/40V 6TQ045	12A/45V 12TQ045
L	39uH	22uH	6.8uH
PCH-	27-393	45-223	45-682
Cout	2uF	4.7uF	10uF
Q1*	8A/60V IRLZ14	8A/60V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 5

VIN = 10 to 18 VDC

VOUT = 5 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	120uH	39uH	22uH
PCH-	27-1243	45-393	45-223
Cout	2uF	5uF	10uF
Q1*	4A/50V IRF9Z12	8A/50V IRF9Z22	12A/50V IRF9Z30

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 6

VIN = 10 to 18 VDC

VOUT = 9 VDC

IOUT = 1, 3, 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	39uH	12uH	6.9uH
PCH-	27-293	27-123	27-682
Cout	1uF	3uF	5uF

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

OFF-LINE APPLICATIONS: FORWARD AND FLYBACK CONVERTERS

Several benefits can be realized in off-line applications by using the low current, UC380x BiCMOS PWM controllers. First, the IC can be powered from a resistor to the rectified input voltage source, eliminating the bootstrap winding. This applies to most low frequency applications (50kHz) where the DC supply current required for the gate drive is low. Soft start of the power supply and delayed restart following a fault requires no external parts. The in-

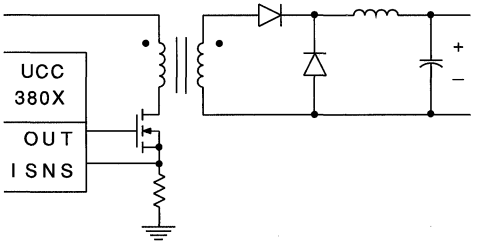

Figure 33. Forward Converter

ternal leading edge blanking eliminates filtering of the current sense signal. Also, the ICs undervoltage lockout thresholds, internal Vcc shunt regulator and active low totem pole output eliminate any problematic gate drive operation.

The basic schematic of a forward converter is shown in figure 33, and a flyback is shown in figure 34. In each, the UCC3804 limits the maximum duty cycle to 50% by internal logic, allowing time for the main transformer to reset. Applications which utilize higher maximum duty cycles, for example 65%, should use the UCC 3802 device without the internal toggle flip flop.

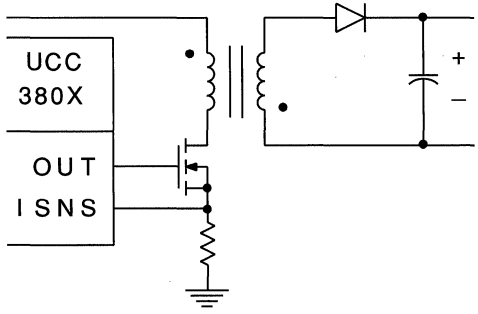

Figure 34. Flyback Converter

UCC380X OTHER APPLICATIONS: UNIVERSAL SYNC GENERATOR

The UCC3803 can be used as a synchronization (SYNC) pulse generator and driver for a variety of applications. Basically, one circuit shown uses the leading edge blanking duration as the SYNC output pulse width. The current limit input is biased at 1.25 volts to terminate the output pulse immediately after the ICs internal blanking pulse width.

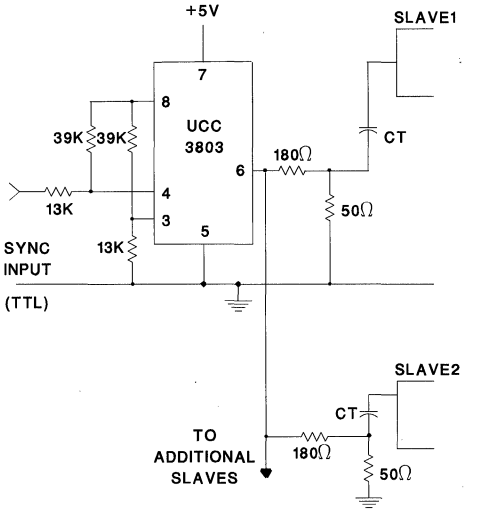

Figure 35. Synchronization Circuit

The oscillator is resistively programmed to a DC level of 1.25 volts also, midway between its upper and lower thresholds. When a TTL compatible SYNC pulse is injected, the amplitude at the oscillator input is raised above its upper threshold. This turns on the internal discharge circuitry which pulls the pin to about 0.2 volts, crossing the lower oscillator threshold. Once this occurs, the discharge transistor is turned off and the ICs output is turned on, generating the SYNC pulse. Note that the current sense input is biased to turn the ICs output off following the leading edge blanking duration, which is used to program the SYNC output pulse width. This 100 nanosecond duration is ideal for synchronizing most PWMs used today with the technique shown.

This circuit can be adapted to generate other width pulses with minor modifications. A capacitor can be added across the lower resistor in the divider network to the current sense input for extending the pulse width. Note that the voltage must be limited below 1.4 volts or a full cycle soft start will be incurred. Also, this capacitor must be discharged before the beginning of each pulse for proper timing

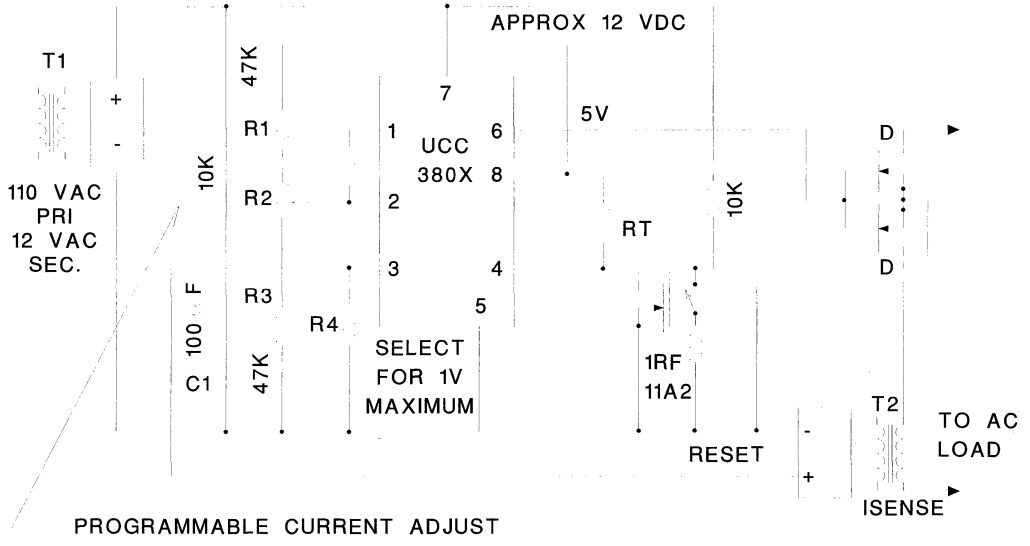

Figure 36. Electronic circuit breaker application.

to occur. One recommendation is to diode couple the current sense input to the oscillator Rt/Ct pin. External circuits can also be used for more precise programming.

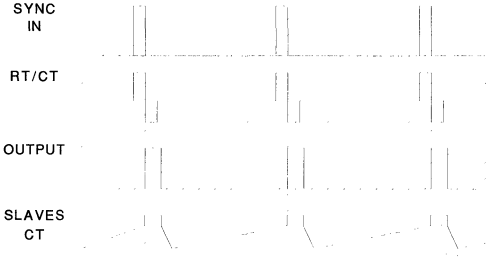

Figure 37. Synchronization Circuit Waveforms

VFO APPLICATIONS

Members of the UCC380x family of devices are adaptable for use in variable frequency applications. The most direct means of accomplishing this is to vary the charging current to the oscillator timing capacitor. Note that the minimum compliance voltage of the current source must exceed the upper oscillator threshold of approximately 2.7 volts. The VFO current source can be generated by an external op-amp for general purpose applications as shown.

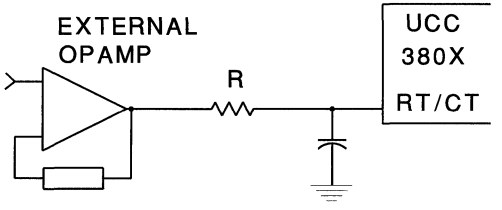

Figure 38. Using UCC380x as a VFO.

Some VFO applications can utilize the ICs internal error amplifier to vary the frequency over a programmed minimum and maximum frequency range. This is done by programming the minimum frequency by a resistor to Vref. Another current sink/source is formed by a resistor to the E/A output. This arrangement performs frequency modulation as the E/A output voltage is varied. Applications which require a fixed 50% duty cycle at varying frequencies, electronic ballasts, for ex-

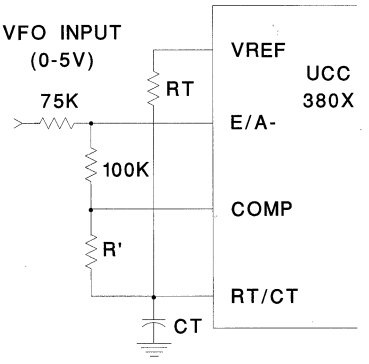

Figure 39: Using the error amplifier to make a simple VFO.

ample, should use the UCC3804 or UCC3805 devices. Output frequency from these will be one-half of the ICs oscillator due to the internal divide-by-two gating circuitry.

FIXED OFF-TIME APPLICATIONS

Obtaining a fixed off-time, variable on-time control technique is easily implemented with the UCC380x family. The oscillator Rt/Ct timing components are used to generate the off-time rather than the operating frequency. Implementation is shown in the corresponding figure 40.

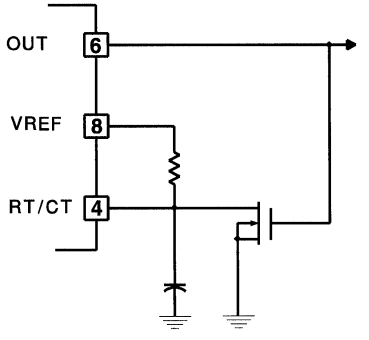

Figure 40: Fixed off-time control.

FULL DUTY CYCLE APPLICATIONS

Any of the UCC380x PWM controllers can be used at full (100%) duty cycle. This mode of operation may be required in certain applications, including DC switch drivers. Implementation requires "freezing" the oscillator so that the output stays high until it is time to turn off. Switch Q1 insures that the PWM output is high when switch Q2 is activated to stop the oscillator. Current limiting can still be accomplished by using the current sense feature of the IC, in addition to modulating the peak current via the error amplifier.

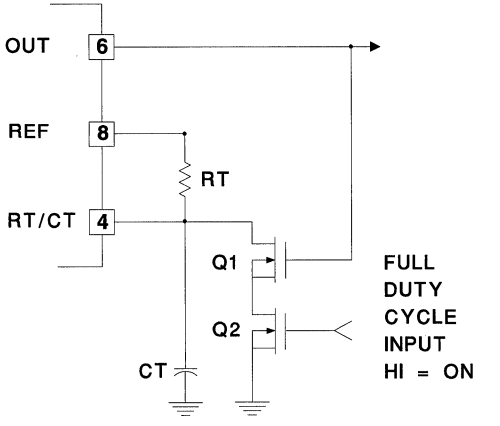

Figure 41. 100% Duty Cycle Circuit

HIGH SPEED, PROGRAMABLE ELECTRONIC CIRCUIT BREAKER

A high speed, programmable electronic circuit breaker can be built using the UCC380x family to perform the control and MOSFET drive functions. Basically, back-to-back power MOSFETS are used as the switching element although an SCR, TRIAC or bipolar switch can also be used. The MOSFETS are connected with the sources tied together to simplify the gate drive while providing a blocking path to current in either direction. Current limiting for an AC supply requires a current transformer, also shown, which can be simplified to a resistor for use in DC input applications. The current sense input to the IC can either be biased up for lower power loss in the current sense network, or programmed by adjusting the error amplifier output voltage to yield a similar result.

SWITCHING COMPONENT NOTES: P CHANNEL MOSFET SWITCHES

Logic level P channel MOSFETs are unavailable today which limits the use of P channel MOSFETs to those with input voltages greater than about ten volts for proper gate drive. The P channel switch will also require a small N channel device to invert its gate drive command, due to the active high output of the PWM (figure 30). High speed PNP transistors are also a suitable choice for some applications.

N CHANNEL MOSFET SWITCHES

Proper gate drive for N channel high side switches will require a supply voltage which is several volts above the input voltage. This is not a problem in five volt input applications using logic level FETs if a nine volt (or higher) supply is also available. If not, one option is to construct a very low power boost converter to generate the nine volt supply to power the IC and gate drive. The boost converter switch can be driven from the UCC380x output which is switching the main output (figure 29). Small, inexpensive surface mount inductors, switches and diodes are readily available. Another possibility is to build a charge pump circuit driven from the PWM output, provided that only a few volts of headroom are required.

GATE DRIVE TRANSFORMER

Higher input voltage applications using high-side switches will require a gate drive transformer due to 12 volt maximum supply rating of the UCC 380x IC family. A small ferrite toroid with two windings and minimal insulation is typically used. A capacitor is placed in series with the primary and is needed for proper reset of the core. The DC offset introduced by the capacitor will effect the primary to secondary turns ratio of the transformer which is dependant on the application. A PULSE Engineering (phone 619-268-2400) model PE-64973 can be employed in most Buck regulator designs.

CURRENT SENSE TRANSFORMER

A current sense transformer is required in the buck regulator application for current mode control. This transformer is used to level shift the current signal from the high side input supply to the ground referenced PWM circuitry. A high turns ratio should be incorporated to reduce power dissipation. Parasitic noise can be minimized by inserting the transformer in series with the drain of the power switch as opposed to its source. A PULSE Engineering (phone 619-268-2400) model PE-64978 current transformer with a one turn primary and 50 turn secondary can be used in most applications.

ADDITIONAL INFORMATION

1. UNITRODE Application Note U-100A;
" The UC3842/3/4/5 Series of Current Mode PWM ICs" :
   - UC3842/3/4/5 PWMs
   - Applications Information

2. UNITRODE Application Note U-111;
" Practical Considerations in Current Mode Power Supplies" ;
   - Fixed OFF-Time Implementation
   - Full Duty Cycle
   - Paralleling Power Supplies
   - Shutdown Techniques
   - Slope Compensation (implementation)
   - Soft Start
   - Synchronization
   - Variable Frequency Operation
   - Voltage Mode Operation

3. UNITRODE Application Note U-96A
"A 25 Watt Off-Line Flyback Switching Regulator":
   - Flyback Converter Design

4. UNITRODE Application Note U-97
"Modelling, Analysis and Compensation of the Current Mode Converter "
   - Current Mode Control
   - Slope Compensation

5. UNITRODE Design Note DN-42
"Design Considerations for Transitioning from UC3842 to the New UCC3802 Family"

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The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters

by JOHN A. O'CONNOR

ABSTRACT

This application note describes the UC3848 average current mode PWM controller. The unique features of this controller are discussed, which make primary side average current mode control practical for isolated converters. The UC3848 employs a current waveform synthesizer which monitors switch current and simulates the inductor current down slope, generating a complete current waveform without actual secondary side measurement. Primarily intended for single ended converters, several additional features such as accurate duty-cycle and volt-second limiting allow maximum transformer and switch utilization. A three output, 200 watt off-line design example is presented which also features planar magnetics and a coupled output inductor.

INTRODUCTION

The UC3848 represents a significant advance in the control of single switch forward converters. Generally considered simple and reliable, but non-optimum in transformer and switch utilization, the single switch forward has previously been reserved for less demanding applications. Upon careful examination however, it is apparent that many of the perceived limitations actually result from the control circuitry rather than the converter topology itself.

The advantages that an inner current loop brings to power supply design and performance are well known [1]. Current mode control is usually preferred over direct duty cycle control because of the superior input supply rejection and simplified voltage loop closure. Average current feedback provides additional advantages over the more common peak current feedback. Major benefits include inherent slope compensation, better noise rejection, and the ability to operate with both continuous and discontinuous inductor current. Additionally, average current feedback provides significantly better closed current loop accuracy. This further improves input supply rejection and current limit accuracy. Average current feedback is detailed in the references [2,3,4].

Maximum power component utilization requires carefully defined and controlled operating mode boundaries. While this can be said of many converter topologies, it is particularly critical with the single switch forward because of the transformer reset mechanism. Energy in the transformer leakage and magnetizing inductance must be removed after each energy transfer cycle. Above all, the control circuit must insure that this condition is achieved. Total losses are generally minimized by bringing the peak power transfer as close to the average as possible. This indicates that improvements in efficiency and component utilization are obtainable by maximizing duty-cycle. Unfortunately, maximizing duty-cycle conflicts with assuring transformer reset, traditionally requiring an overly conservative design to assure reliability.

Previously, these characteristics have limited the single switch converter to low-power, low-end applications. The UC3848 Average Current Mode PWM Controller allows operation beyond conventional limitations by employing highly accurate circuitry to provide programmable operating boundaries, and by implementing an inner average current feedback loop for improved control characteristics and accuracy. This control circuit advance capitalizes on unique, patented circuitry, and the precision achievable with Unitrode's thin-film resistor process.

The UC3848 Average Current Mode PWM Controller

The block diagram of the UC3848 shown in figure 1, illustrates a number of unique functions. Although the IC can certainly be used for flyback,

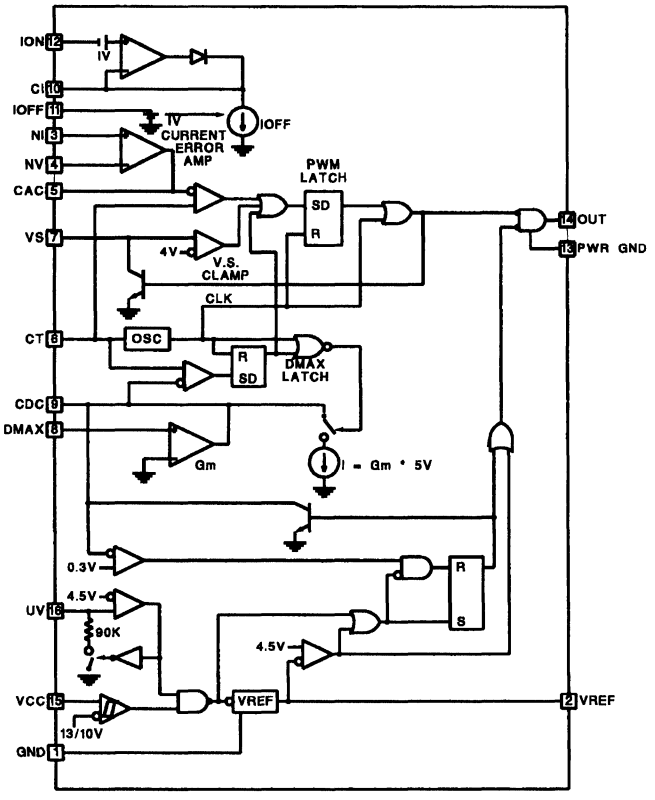

Figure 1

UC3848 Average Current Mode PWM Controller

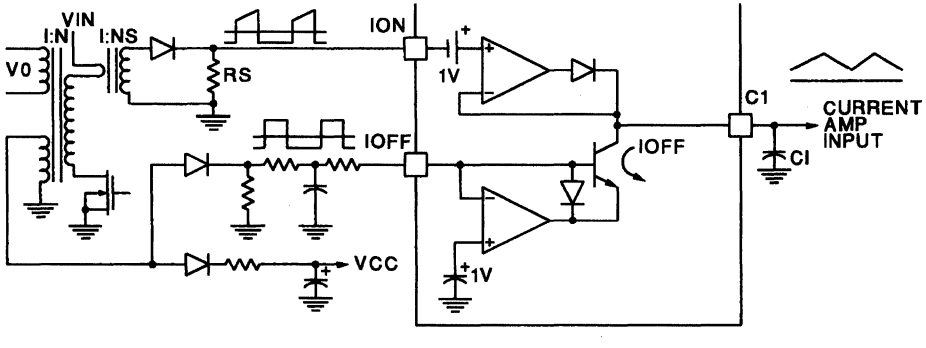

Figure 2

Inductor Current Waveform Synthesizer

boost, as well as other buck derived converters [4], the UC3848 has been optimized for forward converter use. The UC3848s precision functions bring switching power supply control to a new level:

- Average Current Mode Control
- Average Current Sense Signal Synthesizer
- Programmable Maximum Duty-Cycle and Volt-Second Control
- Under Voltage Lockout (UVLO) monitors Vcc, Vin, and Vref
- 2 Amp peak MOSFET Driver with Active Low During UVLO
- 8MHz gain-bandwidth Current Error Amplifier
- Latched PWM comparator
- Practical Operation up to 1 MHz
- Low Start-Up Current (500uA)
- Precision Reference (1% @ 5V)

The sophistication and performance of the UC3848 may at first appear contradictory to simple forward converter design. A truly simple implementation however, is best achieved by maintaining simple power circuitry, and p/acing the complexity and precision in the control circuitry where it can be integrated into a single IC.

Average Current Mode Control

Average current loop implementation first requires an average current signal for the control variable. This immediately presents a problem with isolated converters since this signal is entirely on the secondary side. A current sense transformer cannot be used to directly sense output inductor current with buck derived converters since the inductor normally has a continuous DC component. A potentially complex and expensive solution is avoided with the realization that output inductor current is directly reflected to the primary during the switch on time. Simply scaling the switch current by the transformer turns ratio provides the rising portion of the inductor current waveform. When the switch is off, the inductor current decays at V_{OUT}/L. This information can be used to synthesize an analog of the actual output inductor current without any secondary connections.

Inductor current is synthesized by the UC3848 with a circuit that behaves similar to a track and hold amplifier, as shown in figure 2. While the switch is on, a unity gain buffer charges an external capacitor (C_I), essentially following the rising input current waveform. A one volt offset is also added to provide sufficient headroom for the buffer's output stage. When the switch turns off, a programmable current sink discharges the capacitor, simulating the actual inductor current decay. Several techniques are available for setting the discharge current, depending on the required accuracy of the current sense signal. If good short-circuit accuracy is required, an analog of the output voltage is required to control the synthesizer capacitor discharge rate. There are two simple ways to derive this signal on the primary side.

The first method uses a transformer bootstrap winding voltage as shown in figure 2. The average value of the rectified output and bootstrap winding voltages are directly proportional. By adding a separate rectifier and filter to this winding, the capacitor discharge current can be programmed to track V_{OUT}. Typically, a bootstrap winding is employed with off-line converters to power the control circuitry after initial start-up, so the raw signal is usually present at no additional cost. Note that an error is present during transients since the filter creates a lag between the output and the filtered bootstrap voltages.

If the transient error is unacceptable, the technique shown in figure 3 can be used. A secondary winding on the output inductor provides a voltage directly proportional to the output without filtering. While the switch is off, V_{OUT} is across the output inductor. Any other winding on the inductor will have a voltage proportional to V_{OUT} by the turns

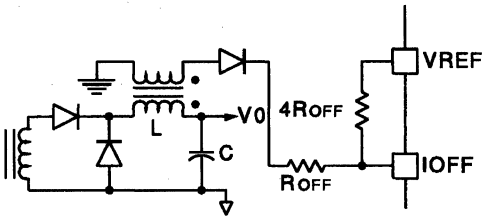

Figure 3
IOFF Generation using
Second Inductor Winding

ratio of the two windings. The sense winding rectifier drop cancels the output rectifier drop when the turns ratio is 1 : 1, yielding excellent signal accuracy. While this approach is simple and accurate, it does come at additional expense since this winding is not normally required. Additionally, high voltage agency approved isolation is required for off-line converters, adding further cost and manufacturing complexity to the inductor.

With either of these techniques, an offset current may be added to compensate for the synthesizer's

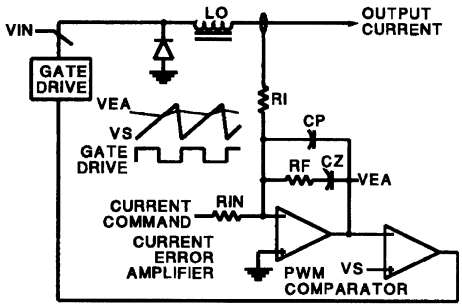

FIGURE 4. AVERAGE CURRENT FEEDBACK LOOP

Figure 4

Average Current Feedback Loop

one volt offset. Connecting a resistor with a value four times the I_{OFF} input resistor between the V_{REF} and I_{OFF} pins cancels the offset.

Often, a fixed discharge current is acceptable. This is programmed by connecting a resistor between the V_{REF} and I_{OFF} pins. The synthesized current waveform is quite accurate when the output voltage is near the regulating value, however an error exists during start-up and output short-circuit. During a short, the current decays much slower since V_{OUT} is only the output rectifier and circuit resistance voltage drops. The current ripple also becomes a small fraction of its value at the regulating voltage. The synthesizer however, discharges the capacitor as if the output were not shorted, and therefore underestimates the output inductor current. The short-circuit current will then exceed the programmed limit by almost one-half of the normal peak-to-peak ripple current. Typically, the inductor ripple current is 20% to 30% of the maximum DC value, corresponding to a short circuit current 10% to 15% higher than the maximum output current available at normal output voltage.

The current error amplifier has sufficient gain to use a current sense resistor directly in most applications. A current sense transformer however, results in better performance by allowing a larger amplitude, lower noise signal. Ideally, the current sense signal is scaled to 4 volts at the maximum current level. The current transformer load resistance is then:

$$R_S = 4V \times N \times \frac{N_S}{I_L} \qquad (1)$$

where N = transformer turns ratio
N_s = current transformer ratio
I_L = maximum load current

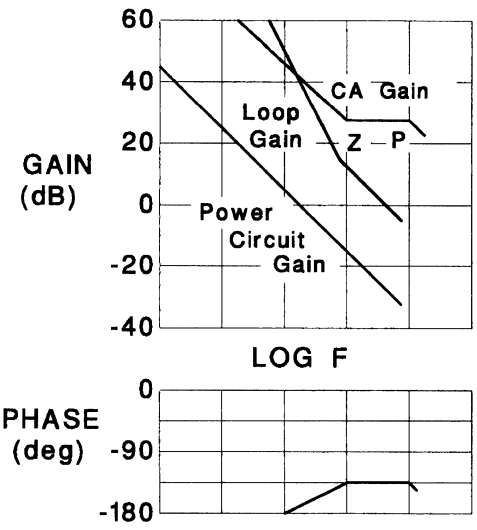

Figure 5

Open Current Loop Response

With multiple secondaries, normalize all other loads to the main output through the turns ratio directly. Note that for these calculations, output inductors and their effect on ripple current is not considered, since the UC3848 controls average, not peak current. Output inductances must be normalized to the main output through the turns ratio squared however, when calculating peak current and current ripple.

The recommended nominal I_{OFF} current is 100µ A, leaving C_I the remaining current synthesizer component.

$$C_I = \frac{(100\mu A \times N \times N_S \times L_{NORM})}{(Rs \times V_{OUT}(nom))} \qquad (2)$$

where L_{NORM} = normalized output inductance

Figure 4 shows the average current feedback loop. This inner loop is analogous to direct duty-cycle or voltage-mode control except that the control variable is output inductor current rather than output voltage. Properly compensated, the open loop gain is comparable to peak current-mode's at high frequency, and becomes orders of magnitude higher as frequency decreases. The open current loop response shown in figure 5 illustrates this behavior. This high open loop gain translates into high

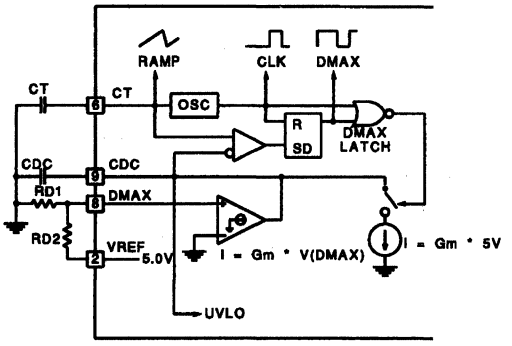

Figure 6

Duty-Cycle Limit Programming

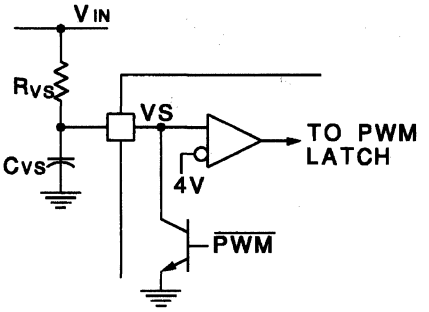

Figure 7

Volt-Second Clamp

closed loop accuracy. In comparison, peak current mode relies entirely on its transfer function accuracy, and has no means by which to reduce errors. This characteristic difference from peak current-mode is attributed to the current error amplifier's compensation, and is key to the resulting performance enhancements.

The increased gain at low frequency provides excellent closed current loop accuracy, even when the inductor current becomes discontinuous. High open loop gain also allows greater filtering of the current sense signal with no degradation in closed loop accuracy. It is this characteristic, along with the larger amplitude signals that provides significantly reduced noise susceptibility in comparison to peak current-mode control.

PWM Oscillator

Oscillator programming is simplified by providing internally set charge and discharge currents. Excellent initial accuracy and temperature stability are assured by precision thin-film resistors. Since only a timing capacitor (C_T) is required to set the frequency, external component error contribution is minimal. The precision high speed oscillator combined with short propagation delay through the PWM circuitry allows practical operation up to 1MHz.

A 200µA charge current and a 1800µA discharge current generates a sawtooth waveform with a well defined rise/fall relationship and accurate frequency. During discharge, the output driver is disabled, limiting the maximum duty-cycle to 90%. Note that this maximum can be reduced by the accurate, duty-cycle limit and the volt-second product limit circuits, which are explained in following sections. Oscillator frequency is programmed by:

$$F = \frac{1}{(10k \times C_T)} \qquad (3)$$

If greater frequency accuracy is required, a trim resistor in parallel with C_T can be added to lower the frequency. The trim resistor should not be less than 40kΩ, limiting the maximum trim range to 25% below nominal. Frequency decrease as a function of trim resistance is shown on the UC3848 data sheet.

Duty-Cycle Limiting and Soft Start

The conventional single switch forward converter design usually limits the maximum duty-cycle to 50%. This limit however, is only required if a one-to-one clamp winding is employed to facilitate transformer core reset. While some designers still use this technique, a resistor/capacitor/diode (RCD) clamp has become more prevalent. The RCD clamp eliminates a transformer winding and potentially offers a wider duty-cycle range. Currently, a 50% duty-cycle limit is primarily used because it can be accurately derived from a toggle flip-flop. To exploit a wider duty-cycle, an accurate, programmable duty-cycle clamp is required.

The UC3848 employs a unique, patented technique to limit the maximum duty-cycle to a value programmed by a resistive divider. The circuit utilizes a capacitor (C_{DC}) for integration only, and does not rely on its absolute value for maximum duty-cycle accuracy. The absolute value of C_{DC} does set the soft-start time constant, although high precision is not normally required for this function.

Internally, the UC3848 capitalizes on the excellent matching characteristics achievable on an IC to implement a charge balanced loop. A matched transconductance source and sink form a precision integrator circuit, as shown in figure 6. The current

source is externally programmed to Gm x V_{DMAX} and is on continually. The current sink is internally set at Gm x 5V, and is switched on and off. The resulting discharge current is Gm(5V - $_{DMAX}$). The current source and sink charge and discharge C_{DC}, while its voltage is compared with the oscillator voltage.

The current sink discharges C_{DC} from the time that the switch is turned on until the oscillator voltage becomes greater than C_{DC}'s voltage. For the remainder of the period, C_{DC} is charged by the current source. Note that C_{DC}'s voltage is essentially a DC level with a very small ripple component unless it is a particularly small value. C_{DC} maintains a constant voltage only if the average applied charge is zero. The charge balanced loop therefore forces $I_{DISCHARGE}$ x $T_{ON(max)}$ to equal I_{CHARGE} x $T_{OFF(min)}$. A large offset voltage between C_T and C_{DC} may be observed when measuring an actual circuit. This offset contributes negligible error since high DC loop gain reduces its effect by several orders of magnitude.

While the circuit's operation may seem complicated, it couldn't be easier to apply. A voltage divider from V_{REF} to D_{MAX} as shown if figure 6 sets the maximum duty-cycle. The circuit inherently provides soft-start at initial power-up as C_{DC} charges to it's steady state value. Increasing C_{DC} extends the loop settling time, and hence the soft-start time constant, with no effect on the programmed maximum duty-cycle. Note that the single pole loop response avoids overshoot, regardless of the integrating capacitor value. Soft-start after fault is explained in the under-voltage lockout section. Maximum duty-cycle and soft-start are programmed by the following relationships:

$$D_{MAX} = \frac{R_{D1}}{(R_{D1} + R_{D2})} \quad (4)$$

$$\tau_{ss} = 20k \times C_{DC} \quad (5)$$

Volt-Second Product Limit

During transients it may be desirable to limit the duty-cycle below the programmed maximum value. For example, active transformer reset circuits vary the clamp voltage inversely proportional to the input supply voltage [5]. During steady state operation the peak MOSFET voltage varies much less than with passive clamp circuits. Unless the input voltage range is large, the peak MOSFET voltage will be fairly constant. This occurs because the applied volt-second product remains constant over the entire operating duty-cycle range during steady state. Thus as the input voltage goes up and the duty-cycle decreases, the clamp voltage goes down as the reset time increases.

If during a transient the duty-cycle is allowed to increase excessively, the MOSFET will be subjected to significantly higher voltages. This assumes that the reset circuit's clamp voltage can slew rapidly. If it cannot, the magnetizing current will ratchet up, possibly saturating the transformer. Both scenarios are easily prevented by simply limiting the maximum applied volt-second product.

The UC3848 generates a voltage proportional to the volt-second product with the circuit shown in figure 7. A current directly proportional to the supply voltage (V_{IN}/R_{VS}) charges a capacitor (C_{VS}) while the MOSFET is on. When the MOSFET is turned off, the capacitor is discharged. Volt-second limiting is accomplished by comparing the capacitor's voltage to a 4 volt reference, and terminating the pulse width for the remainder of the switching period. Normally, the worst case MOSFET voltage occurs during maximum input voltage at the volt-second limited duty-cycle. However, high turns ratio designs which allow a very wide duty-cycle may actually generate the highest MOSFET voltage during low-line at the volt-second limited duty-cycle.

Since the volt-second product is constant it can be calculated at any input voltage. The effectiveness

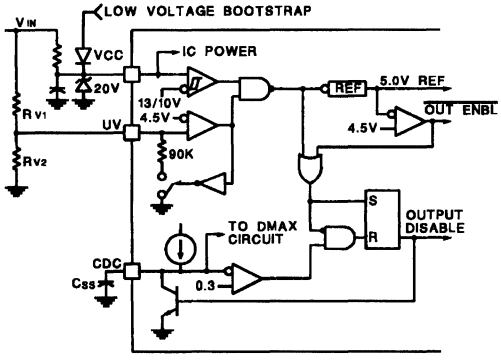

Figure 8

Under Voltage Lockout

of the volt-second limit however, should be analyzed at minimum and maximum input voltage, in addition to a few more typical voltages. The volt-second product clamp is programmed by:

$$V_{IN} \times T_{ON} = 4.0V \times R_{VS} \times C_{VS} \quad (6)$$

Under Voltage Lockout

Programmable under voltage lockout (UVLO) further defines operating mode boundaries. V_{CC}, V_{IN},

and V_{REF} are monitored to insure that the chip supply, main input supply, and reference are within specification before enabling the output stage. Figure 8 shows the block diagram of the UVLO circuitry.

The V_{CC} comparator monitors the chip supply voltage. Hysteretic thresholds at 13V and 10V insure that sufficient voltage is available to power the chip and fully turn on the MOSFET. The V_{IN} comparator monitors the input supply through a resistive divider. A small capacitor from UV to ground is usually required to filter noise from this high impedance node. Both the thresholds and the hysteresis are programmed by the divider values with the relationships:

$$V_{IN(ON)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2'}}\right) \quad (7)$$

$$V_{IN(OFF)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2}}\right) \quad (8)$$

where $R_{V2'} = R_{V2} \parallel 90k$

$$V_{IN(HYS)} = 4.5V \times \frac{R_{V1}}{90k} \quad (9)$$

When either the V_{CC} or the V_{IN} comparator are low, the bias circuitry to the rest of the chip is off. The quiescent current (Ioo) is nominally 500µ A to facilitate off-line applications. Once both V_{CC} and V_{IN} are within specification, the bias circuitry for the rest of the chip is activated. The output driver and C_{DC} pin are still held low until V_{REF} exceeds the 4.5V threshold of the V_{REF} comparator. When the V_{REF} comparator goes high, control of the output driver transfers to the PWM circuitry and C_{DC} is allowed to charge, soft-starting the supply.

If any of the three monitored voltages falls below their threshold during start-up or normal operation, the UVLO latch is set, the output driver is held low, and C_{DC} is discharged. This state is maintained until C_{DC} is fully discharged, at which point operation is as described above.

Output Driver

High current transistors enable the output driver to deliver 2 amps peak allowing direct interface to any MOSFET typically used in single ended converters. The driver also incorporates self-biasing circuitry that maintains a low impedance to ground during UVLO. This assures that high dv/dt at V_{IN} during power-up cannot inadvertently turn on the MOSFET through its miller capacitance.

The combination of high peak current, stray circuit inductance, and capacitive gate load result in reflections back to the driver, which if left unclamped, will cause erratic chip behavior. External schottky diodes from the output to V_{CC} and ground will divert the reflected current and assure reliable operation. A well designed layout with typical circuit values will normally require 1A, 20V schottky clamp diodes. Looser layouts, longer gate drive traces, and lower gate resistor values all place greater demand on the output clamping circuit, and may necessitate higher current diodes.

Voltage Reference and Error Amplifier

Since the UC3848 is intended for primary side control, the voltage reference (V_{REF}) does not affect output voltage stability. It does however, affect current limiting and the other precision circuits previously mentioned, and has therefore been designed for good initial accuracy and temperature drift. The reference should be capacitively bypassed to reduce high frequency output impedance and noise susceptibility.

To facilitate wide bandwidth current loops, the error amplifier has an 8Mhz gain bandwidth product. Even with small current feedback signals such as from a current sense resistor, loop bandwidth will almost always be limited by external circuit characteristics rather than error amplifier limitations. The amplifier's 8 V/s slew rate assures that even during large signal transients, external components will determine circuit behavior.

Design Example

A 200 watt off-line supply utilizing the UC3848 is shown in figure 9. It delivers a regulated +5V at 20A, and a semi-regulated +/-15V at 3.3A. The conversion frequency is 260kHz, which was determined to be a reasonable compromise between size and efficiency. A coupled output inductor improves dynamic cross regulation and steers some of the +5V ripple current to the +/-15V filter capacitors [9]. This results in minimal total output capacitor volume. A bridge/doubler input rectifier allows operation over an input range of 85 to 265VAC. For simplicity and cost, an RCD clamp is employed to facilitate transformer reset. This common configuration is typical of many commercial applications.

The transformer turns ratio is selected to minimize MOSFET stress. Ideally, the maximum duty-cycle should be as large as possible, allowing the highest turns ratio and lowest reflected load current. This must be balanced against the peak MOSFET voltage developed during transformer reset.

Since the UC3848 can accurately define operating mode boundaries, any practical duty-cycle range can be used. This allows maximum utilization of both current and voltage capability of a particular

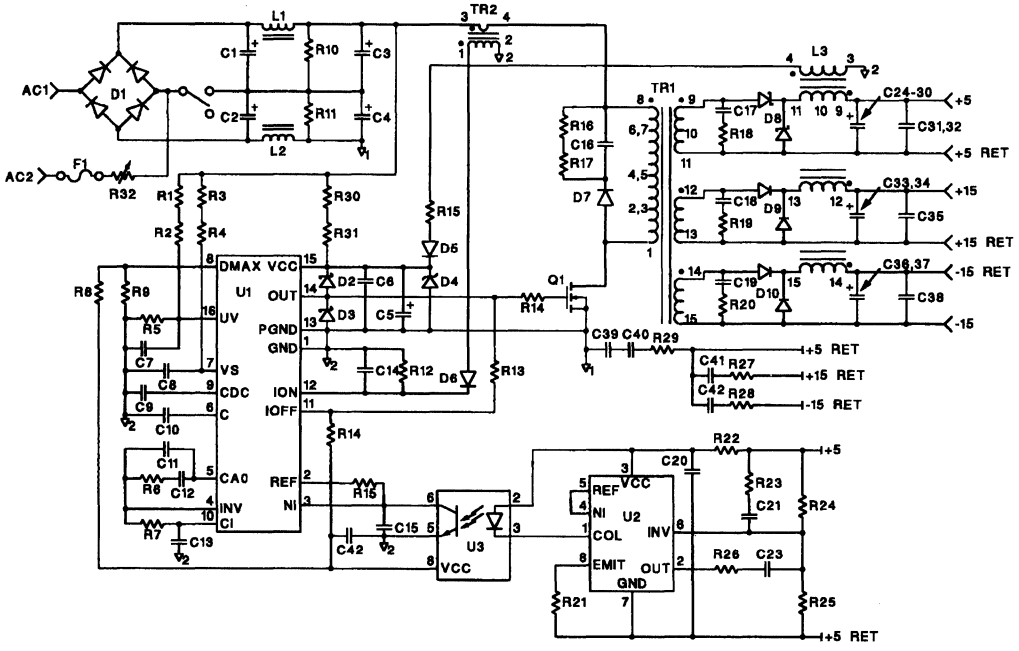

Figure 9

200W 3 OUTPUT FORWARD CONVERTER

MOSFET. The RCD clamp allows some trade-off in dissipation versus peak MOSFET voltage. Turns ratio and clamp optimization requires a good estimation of leakage inductance, switch capacitance, and transformer interwinding capacitance, since energy stored in these parasitics will be transferred or dissipated each switching cycle. RCD clamp optimization is covered in detail in reference [6].

The design example transformer uses a 16:1 turns ratio (primary to 5 volt), allowing a wide input supply range and reliable use of an 800V MOSFET. The MOSFET, an APT801R2BN from Advanced Power Technology [7], is rated at 800V and has 1.2Ω maximum on resistance at 25°C. A planar transformer and coupled output inductor from Signal Transformer Co. [8] are used, which offer several advantages over custom wound components. Planar construction provides tighter parameter tolerance. Compact, low profile magnetics help achieve high power density. Their standard design provides agency approved insulation and known performance characteristics, greatly reducing the number of iterations to produce a good power supply design.

The duty-cycle is limited to 0.6, maintaining regulation down to approximately 160 VDC in. With the switching frequency programmed for 260 kHz, the nominal volt-second product is 345 Vs. The volt-second clamp is programmed to 425 Vs to allow for tolerances and large signal transients.

A current transformer senses switch current resulting in minimal loss and good signal quality. A 1000pF capacitor shunts the high frequency turn-on spike before feeding the current sense signal to the UC3848s current waveform synthesizer. A fixed I_{OFF} value renders an acceptable short circuit current for this application. Average short circuit losses are kept low by the hiccup action which occurs as the boot-strap supply collapses and the supply restarts. Highly accurate short circuit current is most advantageous when a continuous supply is available for the control circuit such as in low voltage DC to DC converter applications.

When the MOSFET is on, the current synthesizer's I_{OFF} current is increased through a resistor connected to the gate driver output (R13). This allows C_I's voltage to better follow rectifier reverse recovery spikes present in the current waveform. This technique allows minimal filtering of the current

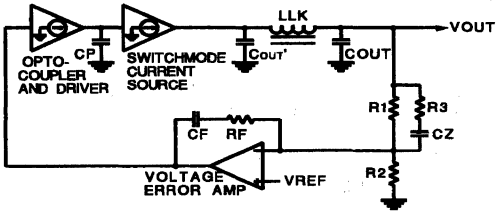

Figure 10

Voltage Feedback Loop

sense signal, and thus preserves accuracy.

The coupled output inductor provides good dynamic cross regulation, and steers some of the 5 volt ripple current to the +/-15 volt outputs where it is more efficiently filtered. Although this technique minimizes size and complexity, it does negate two major advantages of average current mode control. The average current loop maintains excellent regulation down to zero load for the fully regulated output. Unfortunately, the semi-regulated outputs will degrade quickly as the inductor current becomes discontinuous, forcing minimum loads for reasonable output voltage tolerance. Also, stray and leakage inductance between the secondary circuits introduces parasitic tank circuits, which if underdamped, will cause output ringing and instability. Generally, electrolytic output capacitors, low coupled inductor leakage inductance, and tight layout will allow successful implementation, although loop bandwidth must usually be compromised to maintain stability. Coupled output inductor design and application is detailed in reference [9].

Without the additional output circuitry parasitics, a single output supply with average current feedback has excellent regulation and transient response from zero to full load. There is also much less restriction on output capacitor type, allowing small ceramic or film capacitors in many applications. Although the design example's closed loop bandwidth is not as high as would be achievable with a single output, the electrolytic output capacitors store enough energy to provide good transient response and low output impedance.

Control Loops

A block diagram of the voltage feedback loop is shown in figure 10. For clarity, the inner average current feedback loop is shown as a transconductance amplifier, and is identical to figure 4. Current loop compensation is best described in the references [2,3], as a number of subtleties must be considered for optimal performance. The basic approach is easily summarized:

To avoid subharmonic oscillation of a single pole system, the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This puts an upper limit on the current amplifier gain, and indirectly sets the loop gain crossover frequency. As derived in [2], the resulting unity gain crossover frequency will be:

$$f_C = \frac{(f_S V_{IN})}{(2\pi V_{OUT})} = \frac{f_S}{(2\pi D)} \quad (10)$$

The crossover frequency must be reduced in a practical system to account for tolerances and additional waveform slope injected by output voltage ripple through the voltage error amplifier. For the design example, f_C is approximately 50kHz at the maximum duty-cycle.

At the switching frequency, the average current loop's behavior is similar to peak current mode control. Placing a zero at one-half the crossover frequency increases the loop gain with decreasing frequency, providing high closed current loop accuracy. To further reduce noise susceptibility, a pole is placed at the switching frequency. While such a low frequency filter is completely unacceptable with peak sensing, the high gain at low frequency assures accurate current limiting. It is these fundamental differences from peak current mode which provide the performance enhancements.

The voltage loop reference and error amplifier reside on the secondary side as typically configured in off-line power supplies. A UC19432 incorporates a high precision reference, voltage error amplifier, and programmable transconductance amplifier for accurate opto-coupled feedback. Voltage loop compensation is normally the same as with peak current mode control and is described in detail in the references [2,9,10]. As previously noted, an additional LC pole resulting from leakage and stray inductance requires additional compensation. Ultimately, this parasitic restricts the bandwidth of this coupled inductor design example, although transient response is still quite good. The same control configuration with a single output supply provides optimal performance and allows simpler compensation.

Summary

The UC3848 clearly demonstrates the next level of switching power supply control achievable with improved techniques and precision circuitry. High

performance and high power density objectives coupled with the need for simplicity and low cost have called for further refinement of single switch conversion. The UC3848 answers that call combining precision circuitry, average current mode control and function flexibility, allowing optimal power component utilization and performance.

References:

[1] V. Holland, "Modelling, Analysis and Compensation of the Current-Mode Converter" Unitrode application note U-97

[2] L. Dixon, "Control Loop Design", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800,1991

[3] L. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode application note U-140

[4] B. Mammano, "Average Current-Mode Control Provides Enhanced Performance for a Broad Range of Power Topologies", PCIM conference proceedings, 1992

[5] B. Carsten, "Design Techniques for Transformer Active Reset Circuits at High Frequencies and Power Levels", High Frequency Power Conversion conference proceedings, 1990

[6] C.S. Leu, G.C. Hua, F.C. Lee, C. Zhou, "Analysis and Design of RCD Clamp Forward Converter", Virginia Power Electronics Center seminar proceedings, 1992

[7] Planar Magnetics data sheet, Signal Transformer Co., Inwood, NY, 516-239-5777

[8] APT801R2BN data sheet, Advanced Power Technology, Bend, OR, 503-382-8028

[9] L. Dixon, "Coupled Filter Inductors in Multi-Output Buck Regulators", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800,1991

[10] L. Dixon, "Closing the Feedback Loop", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM700,1990

Unitrode Data Sheets:

UC3848
UC1 9432

PARTS LIST FOR **200W** CONVERTER

R1, 2	825k	1%
R3, 4	243k	1%
R5	42.2k	1%
R6, 7	10k	
R8	10.0k	1%
R9	15.0k	1%
R10, 11	62k	1w
R12	68	
R13	36k	
R14	39k	
R15,23	2k	
R16, 17	15k	3w
R18	10	2w
R19, 20	33	1/2w
R21	33	
R22	200	
R24	18.7k	1%
R25	6.49k	1%
R26	1k	
R27, 28	20	
R29	100	
R30, 31	120k	1/2w
R32	5ΩNTC	thermistor

C1-C4	390µF	20%	200V
C5	100µF	20%	25V
C6, 20, 31, 32, 35, 38	1µF		
C7, 14	1nF		
C8	220pF	5%	
C9	47nF		
C10	390pF	5%	
C11	22pF		
C12	330pF		
C13	220pF		
C15	10nF		
C16	2.2nF		
C17	4.7nF		100V
C18, 19	470pF		500V
C21, 23	3.3nF		
C24-C30	1000µF	20%	10V
C32, 33, 36, 37	330µF	20%	25V
C39, 40	2.2nF	20%	500V
	class x/y		
C41, 42	100nF	20%	100V

D1	MB106-ND	(Diodes, Inc.)
D2, 3	1N5820	
D3	1N4745A	
D4, 5	1N4148	
D6	10DF8	(International Recifier)
D7	40CPQ060	(International Recifier)
D9, 10	10CTF20	(International Recifier)
Q1	APT801R2BN	(Advanced Power Technology)
L1, 2	RL-1160-1.0	(Renco)
L3	SHFI-2515	(Signal Transformer Co.)
TR1	SHF-2525-16	(Signal Transformer Co.)
TR2	PE64978	(Pulse Engineering)
U1	UC3848	
U2	UC19432	

NOTE: All resistors 5%, 1/4 watt unless noted
All capacitors 10%, 50V unless noted

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UNITRODE

APPLICATION NOTE

PHASE SHIFTED, ZERO VOLTAGE TRANSITION DESIGN CONSIDERATIONS and the UC3875 PWM CONTROLLER

BILL ANDREYCAK

ABSTRACT

This Application Note will highlight the design considerations incurred in a high frequency power supply using the Phase Shifted Resonant PWM control technique. An overview of this switching technique including comparisons to existing fixed frequency non-resonant and variable frequency Zero Voltage Switching is included. Numerous design equations and associated voltage, current and timing waveforms supporting this technique will be highlighted. A general purpose Phase Shifted converter design guide and procedure will be introduced to assist in weighing the various design tradeoffs. An experimental 500 Watt, 48 volt at 10.5 amp power supply design operating from a preregulated 400 volt DC input will be presented as an example. Considerations will be given to the details of the magnetic, power switching and control circuitry areas. A summary of comparative advantages, differences and tradeoffs to other conversion alternatives is included.

UC3875 CONTROL CIRCUIT SCHEMATIC

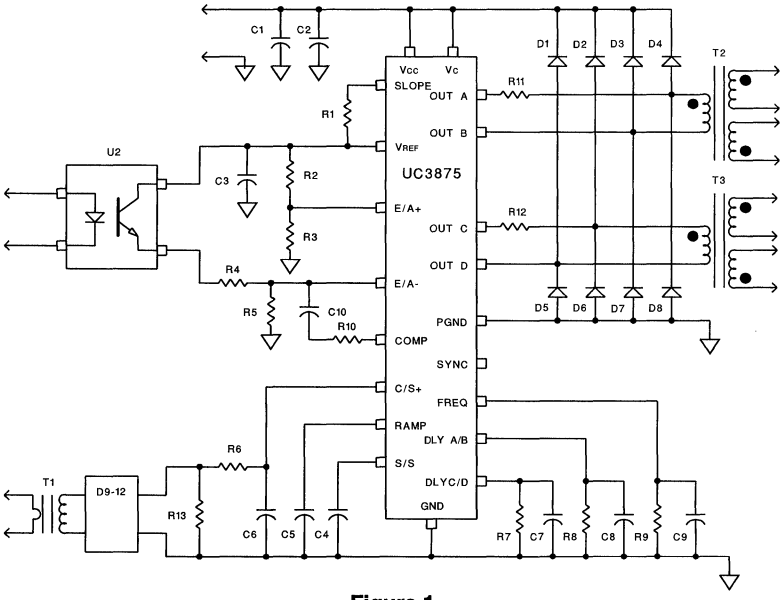

Figure 1

INTRODUCTION

The merits of lossless transitions using Zero Voltage Switching techniques have already been established in power management applications. [1-5] Effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique. The full bridge topology as shown in figure 2. will be the specific focus of this presentation, with an emphasis placed on the fixed frequency, phase shifted mode of operation.

Full Bridge Topology - General Circuit

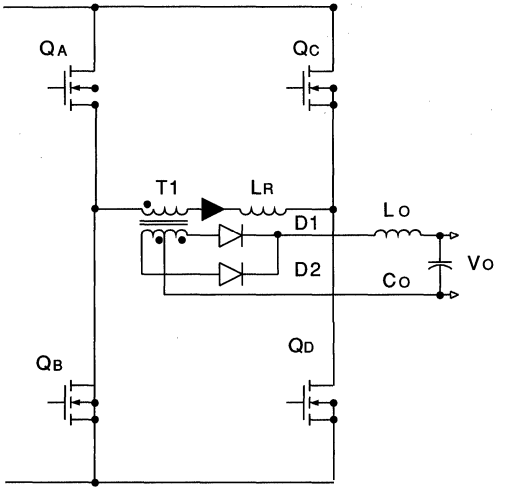

Figure 2

SWITCH DRIVE COMMANDS

The diagonal bridge switches are driven together in a conventional full bridge converter which alternately places the transformer primary across the input supply, Vin, for some period of time, t(on) as shown in figure 3.

Power is only transferred to the output section during the ON times of the switches which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Conventional Full Bridge PWM Waveforms

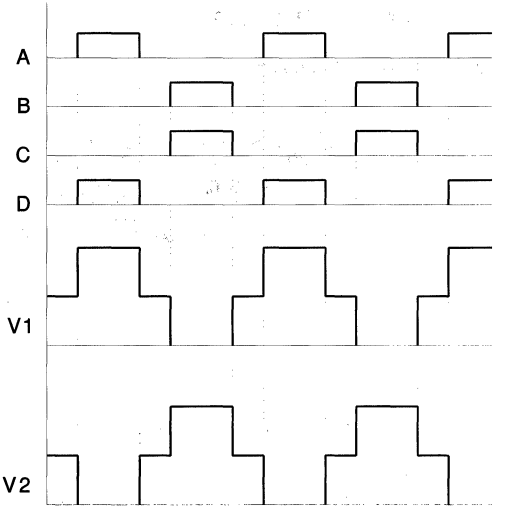

Figure 3

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in figure 4.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (Coss) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge "leg" with zero voltage across it enabling Zero Voltage Switching upon its turn ON.

Phase Shifted PWM Control Waveforms

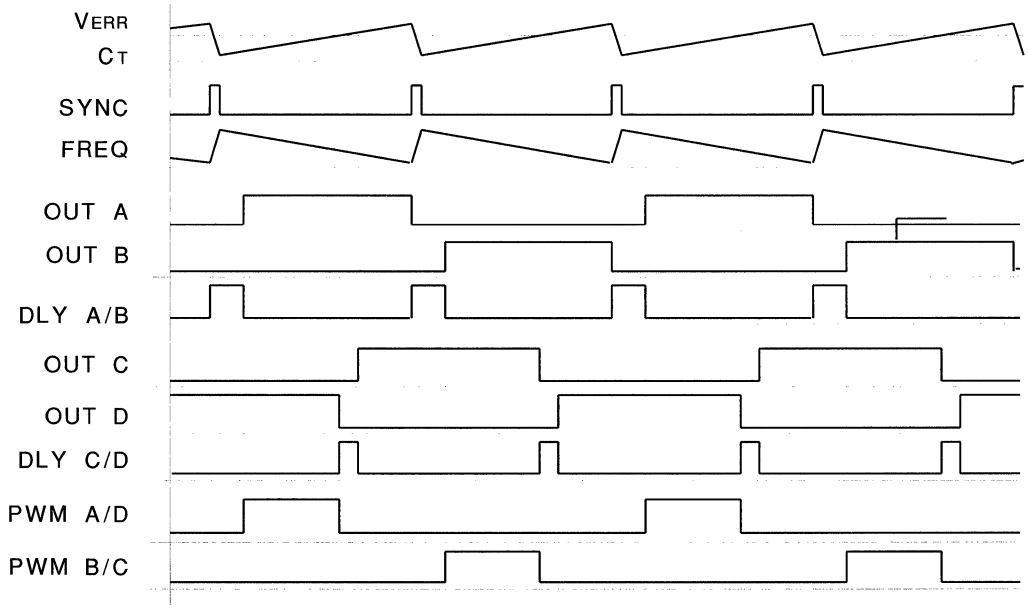

Figure 4

ZVS FUNDAMENTALS

An intentional dead-time can be introduced in the power conversion cycle whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather then turn the switch on instantly when zero voltage is attained, the switch is held off while the primary current circulates into the shorted primary through the body diode and the opposite leg switch, which is still on. This off time is used to fill in the voids between the point where zero voltage has been reached where the switch needs to turned on to achieve fixed frequency operation.

Fixed frequency operation is obtainable over an identified range of input voltages and output currents. For reference purposes, the variable frequency ZVS technique has similar limitations for proper operation which occur at minimum output load and maximum input line as shown in figure 5.

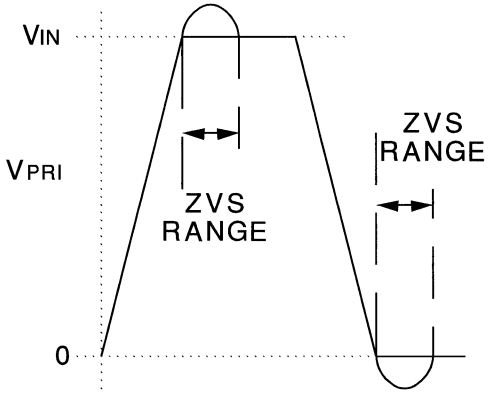

Figure 5

ZVS Limitations

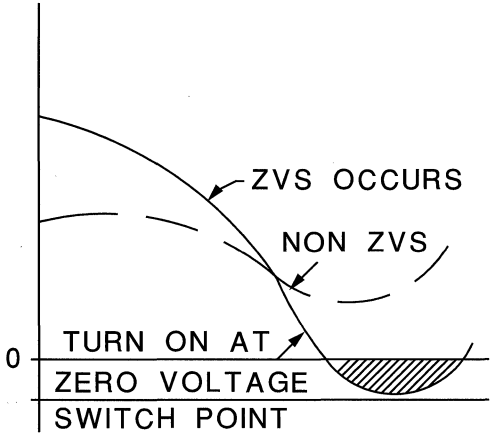

Figure 6

Phase Shifted PWM Switch Orientation

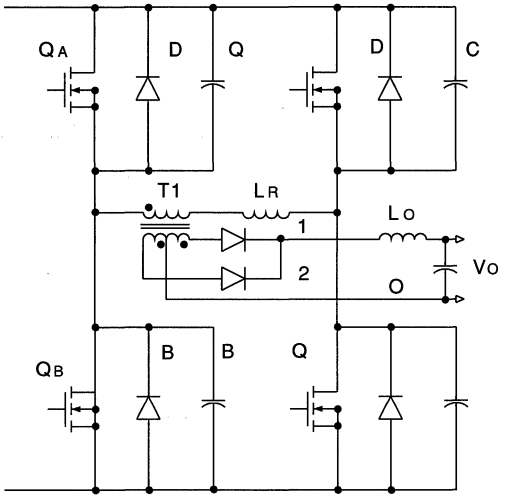

Figure 7

PHASE SHIFTED FUNDAMENTALS

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its nonresonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's constructuin. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

CIRCUIT SCHEMATIC AND DESCRIPTION

Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in figure 7. including voltage and current designations.

The basic circuit is comprised of four switches labeled QA through QD and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (IP) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also accounted for by multiplying the output inductance by the turns ratio squared (N^2), or dividing the secondary AC ripple current Isec(ac) by the turns ratio (N) as shown in figure 8.

Primary Magnetic Components

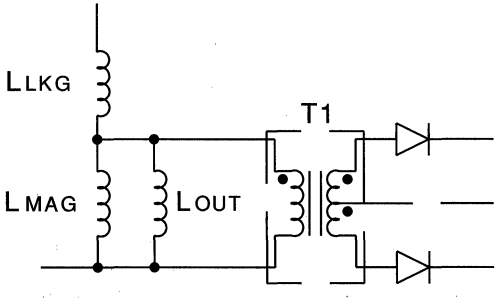

Figure 8

INITIAL CONDITIONS : t = t(0)

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as Ip(t(0)).

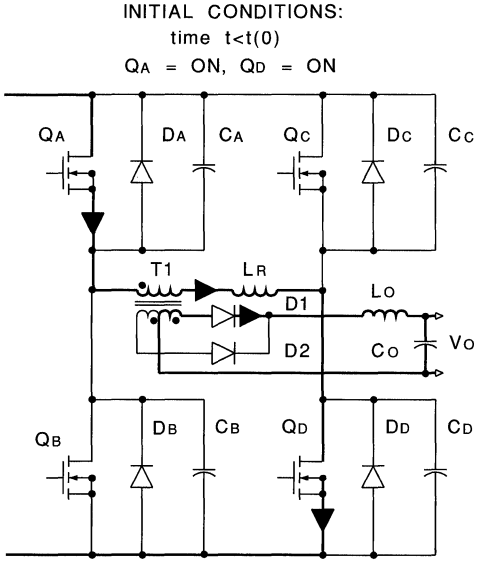

Figure 9

RIGHT LEG RESONANT TRANSITION : INTERVAL: t(0) <t <t(1)

The primary current flowing at time t(0) is equal to Ip(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right. Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at Ip(t(0)) by the resonant inductance (Lp(res)) of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, Lr. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external "shim" inductor to control the accuracy. It's also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.

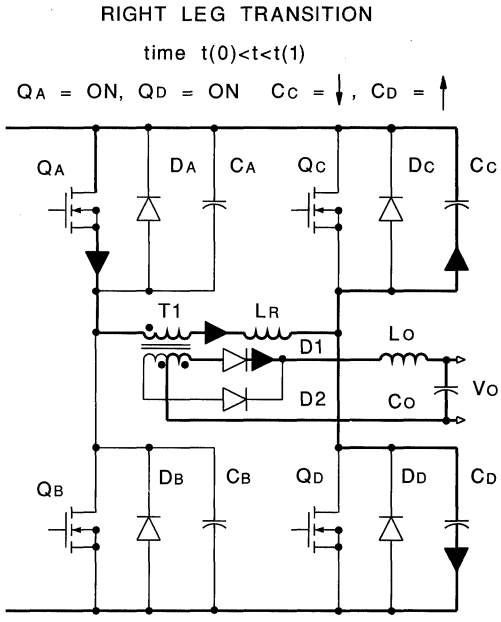

Figure 10

With switch QD turned off, the primary current continues to flow using the switch output capacitance, Coss to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, Vin+. Simultaneously, the transformer capacitance (Cxfmr) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased fom Vin to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, Vout*N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt.

previously turned ON and switch QA will now be turned OFF. The primary current will continue to

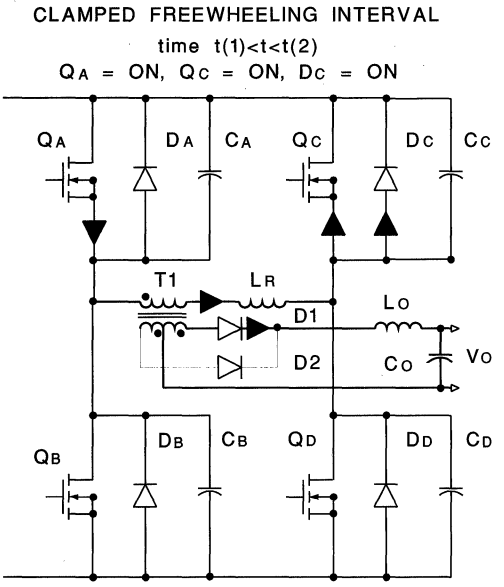

Figure 11

CLAMPED FREEWHEELING INTERVAL
Time t(1) <t <t(2)

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode.

LEFT LEG TRANSITION :
Time t(2) <t <t(3)

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been

flow but the path has changed to the output capacitance (Coss) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation.

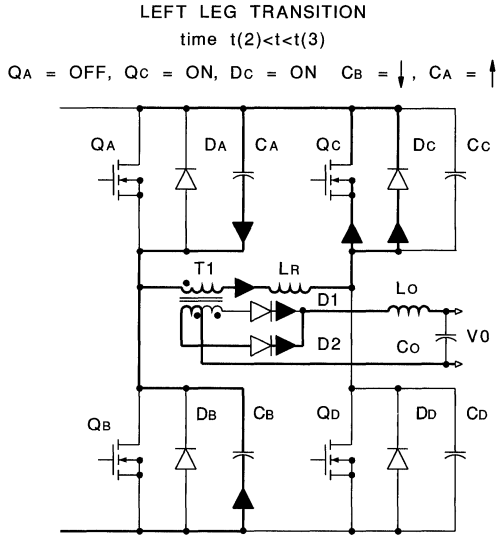

Figure 12

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial (IP(t(0)) value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

POWER TRANSFER INTERVAL

Time t(3) <t <t(4)

This interval of the phase shifted cycle is basically identical to that of conventional square wave power convesion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by Vin and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, Iout/N. The two time variant contributors to primary current are the magnetizing current (Imag) and the output inductor magnetizing contribution reflected to the primary, Lout/N^2. The exact switch ON time is a function of Vin, Vout and N the transformer turns ratio, just as with conventional converters.

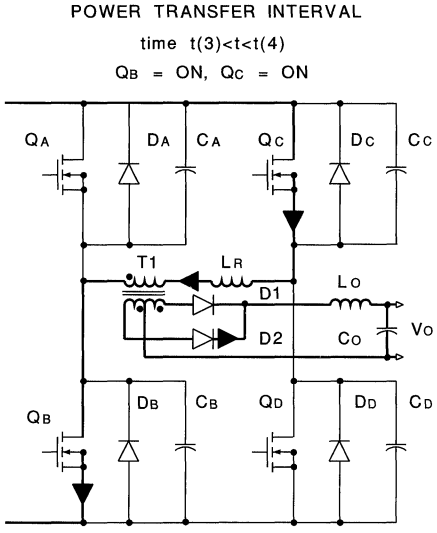

Figure 13

SWITCH TURN OFF; TIME t(4)

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, Coss. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, Vin. The output capacitance of the lower switch in the left hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage.

The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set QA and QD.

OPERATIONAL WAVE FORMS

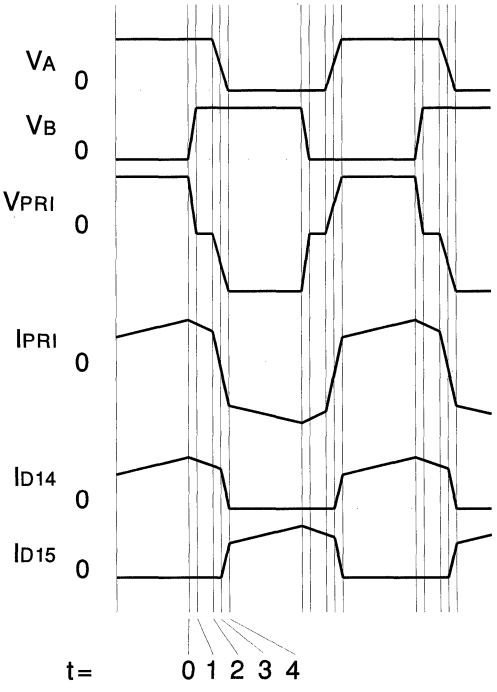

Figure 14

RESONANT TANK CONSIDERATIONS

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.

RESONANT CIRCUIT LIMITATIONS

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (Wr) of the tank circuit. Elements of this tank are the the resonant inductor (Lr) and capacitor (Cr), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance Cxfmr. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, Wr :

$$Wr = \frac{1}{(Lr \times Cr)\ \hat{}\ 0.5}$$

$$t(max)\ transition = \frac{\pi}{2 \times Wr}$$

Coss, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 * Coss. Transformer capacitance (Cxfmr) must also be added as it is **NOT** negligible in many high frequency applications.

The resonant capacitance, Cr :

$$Cr = [\,(\frac{8}{3}\,C_{oss)+}\,Cxfmr\,]$$

The capacitive energy required to complete the transition , W(Cr) is:

$$W(\,Cr) = \frac{1}{2} \times Cr \times VPri\text{^}2$$

This energy can also be expressed as:

$$W(\,Cr) = [\,(\frac{4}{3} \times Coss) + Cxfmr\,] \times Vin\text{^}2$$

STORED INDUCTIVE ENERGY

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, Lr:

$$W(Lr) = \frac{1}{2}\,x\,Lr\,x\,Ipri\text{^}2$$

RESONANT CIRCUIT SUMMARY

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships.

The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t(max) at light load.

$$Tres = 4 \times t(\,\max)$$

$$Fres = \frac{1}{T(\,res)}\;or$$

$$where\;\; Wr = 2 \times \pi \times Fres$$

$$Wr = \frac{2 \times \pi}{T(\,res)}$$

Reorganizing and combining these relationships;

$$Wr = \left[\frac{(2 \times \pi)}{(4 \times t(\,\max))}\right]$$

$$Wr = \frac{\pi}{(2 \times t(\,\max))}$$

The resonant radian frequency (Wr) is related to the resonant components by the equation:

$$Wr = \frac{1}{(\,Lr \times Cr)\text{^}2}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$Lr = \frac{1}{(\,Wr\text{^}2 \times Cr)}$$

Previously outlined relationships for Wr and Cr can be introduced to result in the following specific equation.

$$Lr = \frac{1}{\left[\frac{\pi}{(2 \times t(\,\max)}\right]\text{^}2 \times \left[(\frac{8}{3} \times Coss) + Cxfmr\right]}$$

Note that this figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.

$$\frac{d\,IPri}{dt} = \frac{Vin}{Lr}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

STORED ENERGY REQUIREMENTS

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times Lr \times IPri(\,\min)\text{^}2 \;>\; \frac{1}{2} \times Cr \times Vin(\,\max)\text{^}2,\; or$$

$$Lr \times IPri(min)\text{^}2 \;>\; Cr \times Vin(\,\max)\text{^}2$$

Since Cr and Vin are known or can be estimated for a given application, this term becomes a constant and Lr has been quantified.

MINIMUM PRIMARY CURRENT

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$IPri(\min) = \left[\frac{(Cr \times Vin\hat{}2)}{Lr}\right]\hat{}0.5$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower that IP(min) it can be used as a confirmation of the mathematics.

$$IR(average) = Cr \times \frac{Vin}{t(\max)}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually cores loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

PHASE SHIFTED PWM CONTROL CIRCUITRY

Probably the most critical control aspect in the phase shifted PWM technique is the ability to span the full 0 to 180 degree phase shift range. Falling short of performance on either end of the spectrum can place unnecessary burdens on the fault protection circuitry or primary switches. Loss of control at either extreme will result in catastrophic consequences by simultaneously turning on both transistors in a given "leg" of the converter. The UC3875 Phase Shifted controller features the required circuitry to deliver both zero and effectively full duty cycle - effortlessly. Additionally, the UC3875 controller is utilized to perform the necessary control, decoding, protection and drive functions for this application. Peak current mode control is implemented for this example although the IC is equally suited for conventional voltage mode control, with or without input voltage feed forward. When used in current mode, the IC accepts a zero to 2.7 volt amplitude maximum current senses input and makes adding slope compensation a simple function.

UC3875 Block Diagram

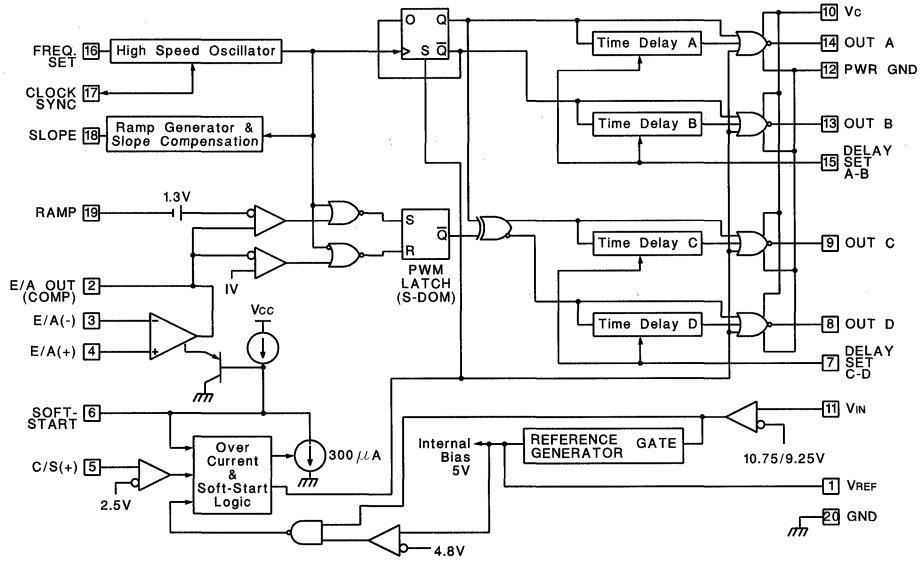

Figure 16

UNITRODE UC3875 PHASE SHIFTED PWM CONTROL IC - BLOCK DIAGRAM

A synchronizable oscillator is programmed by a resistor capacitor network from the frequency set pin to ground. Synchronization is performed by driving the SYNC pin from another UC3875 or external circuitry. The precision 5.0 volt bandgap reference is available to program the noninverting input of the error amplifier as well as optional external functions. Output regulation is achieved using the 7 MHz gain-band width on-board error amplifier which feeds the high speed PWM circuitry. Soft starting is accomplished with a capacitor to ground which gradually increases the error amplifier output, corresponding to pulse width, phase shift or peak current, depending on the exact implementation. This signal is compared to the Ramp input of the IC having a usable input range from zero to 2.7 volts.

Delays between the output drive commands to facilitate Zero Voltage Switching are programmed at the Delay Set inputs. One unique feature of the UC3875 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different primary currents during one switching cycle which cause and result in different resonant transition times between the leading and falling edges. Inability to program each of these durations will generally result in lossy, non-zero voltage switching of the full bridge converters switches under some operating conditions.

The four UC3875 output totem poles can each deliver a two amp peak gate drive current, more than adequate in a high frequency transformer coupled gate drive application. To minimize noise transmitted back to the analog circuitry, the output section features its own collector power supply (Vc) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply further enhances performance.

Fault protection is established by the programmable current limit circuitry. Full cycle restart corresponding to the time programmed by the soft start interval minimizes power dissipation in a short circuited output.

TYPICAL APPLICATION CIRCUIT SCHEMATIC SUMMARY

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. switching losses due to the simultaneous overlapof voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage acvantageously. For most applications, there is little reason to consider the traditional square wave counterpart of theis phase shifted PWM technique for future designs.

Very high frequency operation of this technique, beyond 500 KHz, is probable above the optimal operating point. Transition times quickly erode the usable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and repower loss in the switches. Any incremental gains in cost or power density by reducting the size of the output filter are probably nullified by the needs for larger MOSFETs and heatsinks. This phase shifted PWM technique does excel in the overall majority of mid to high power, off-line applications. Peak efficiency will be obtained in applications with moderate load ranges, however excellent results can also be obtained in most designs with load ranges of ten-to one. A subgroup of applications may exist where non ZVS operation extremely light loads is acceptable, especially when the advantages under all other operating conditions are considered. Additionally, the Unitrode UC3875 Phase Shifted Controlller IC has been introduced to simplify the control circuit design challenge. Features of the UC3875 include 2 MHz operation and four 2 amp peak totem-pole output drivers for high frequency applications. Separate programming of the different AD and BC leg transition intervals has made available to optimize converter performance.

Finally, the flexible control logic permits current mode or voltage mode control, with or without input voltage feed forward. The complexity of control, drive and protection of the fixed frequency phase shifted converter has been fully addressed in a single integrated solution.

UC3875 Phase Shifted PWM Converter
Control and Output Circuit Schematic

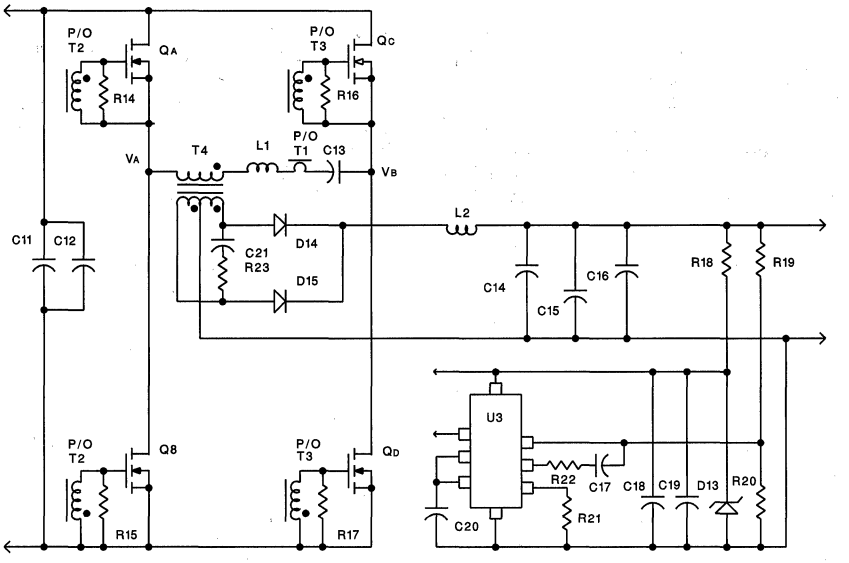

Figure 17

UC 3875 Phase Shifted PWM Converter
Control and Drive Circuit Schematic

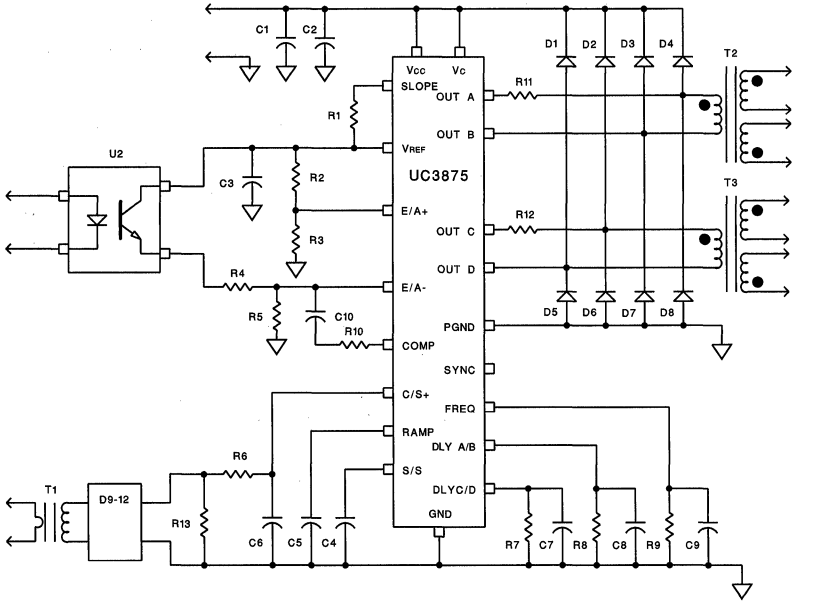

Figure 18

UC3875 F.B.P.S. CONVERTER

LIST OF MATERIALS

CAPACITORS

All are 20 VDC Ceramic Monolithic or Multilayer UNLESS "*" indicated.

C1= 1 µF
C2= 47 µF/25V ELECTROLYTIC
C3= 1 µF
C4= 1 µF
C5= 75 pF/16V POLYSTYRENE
C6= 0.001 µF
C7, 8= 0.01 µF
C9= 470 pF
C10= 0.1 µF
C11= 1 µF/450VDC POLY
C12= 47µ/450VDC ELECTROLYTIC
C13= 1.2µF/450 VDC POLY
C14= 1µF/100VDC
C15, 16= 220µF/63VDC ELECTROLITIC
C17= TBD
C18= 1µF
C19= 22 µF/25VDC ELECTROLITIC
C20= 1 µF
C21= 2.7 nF/200V POLY/low ESL&ESR

DIODES
D1-8= 1N5820 3A/20V SCHOTTKY
D9-12= 1N4148
D13= 12V 3W ZENER
D14, 15= 15A/200V FAST RECOVERY

INDUCTORS
L1= 47µH/3A
L2= 100µH/15A

MOSFET TRANSISTORS
QA-D=IRF840 NMOS

Bill Andreycak / UICC
2/24/93

RESISTORS

All are 1/2 Watt, 1%, Metal Film UNLESS "*" indicated

R1= 75K
R2= 2K
R3= 3K
R4= 470 Ohm
R5= 3K
R6= 100 Ohm
R7, 8= 6.8K
R9= 43K
R10= 150K
R11, 12= 10 Ohm
R13= 20 Ohm
R14-17= 10K
R18= 3.6K, 1WATT
R19= 36K
R20= 1K
R21= TBD
R22= TBD
R23= 110 Ohms/5W Carbon

TRANSFORMER
T1= 1 SENSE
T2, 3= GATE DRIVERS
T4= MAIN XFMR

INTEGRATED CIRCUITS
U1= UC3875 PMW
U2= OPTO
U3= UC19432

One Switching Cycle

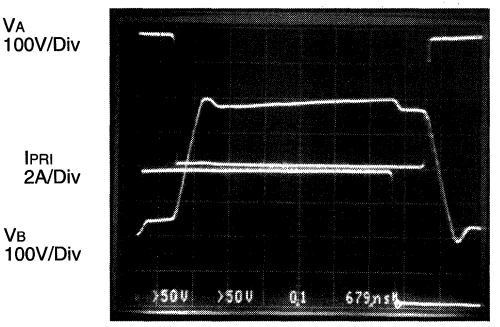

Figure 19

Primary Waveforms

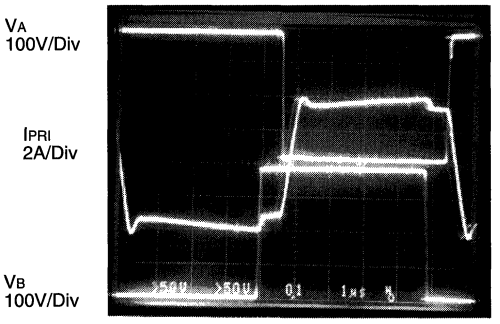

Figure 20

Secondary Waveforms

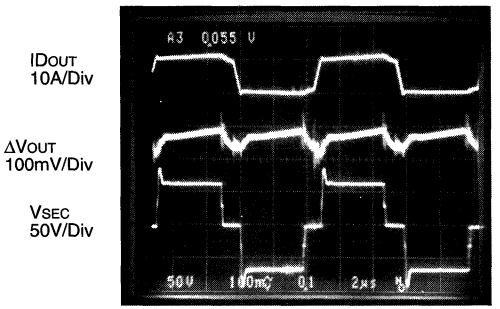

Figure 21

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Zero Voltage Switching Resonant Power Conversion

Bill Andreycak

Abstract

The technique of zero voltage switching in modern power conversion is explored. Several ZVS topologies and applications, limitations of the ZVS technique, and a generalized design procedure are featured. Two design examples are presented: a 50 Watt DC/DC converter, and an off-line 300 Watt multiple output power supply. This topic concludes with a performance comparison of ZVS converters to their square wave counterparts, and a summary of typical applications.

Introduction

Advances in resonant and quasi-resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Currently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals and relevant voltage and current waveforms.

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicized by another at various power conferences [2,3]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters [4,5,6,7,8]. In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the MOSFET output capacitance (C_{OSS}) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique [9,IO].

Zero Voltage Switching Overview

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.

Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly

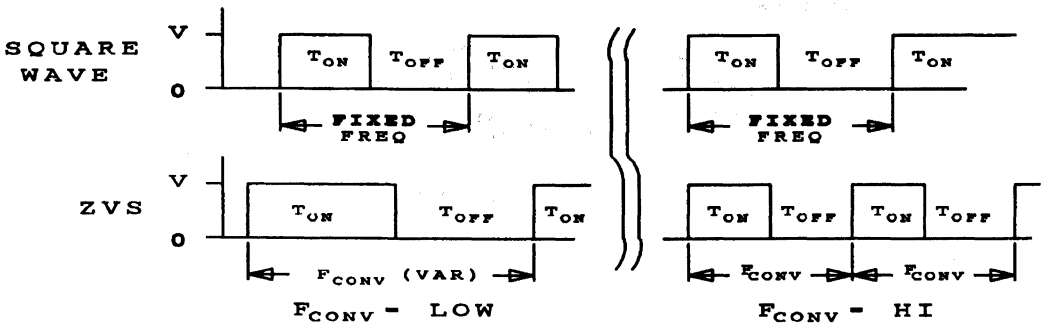


Fig. 1 - Zero Voltage Switching vs. Conventional Square Wave

unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (C_{OSS}) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V_{DS} equals zero.

The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, however a list of references describing the others has been included in the appendix.

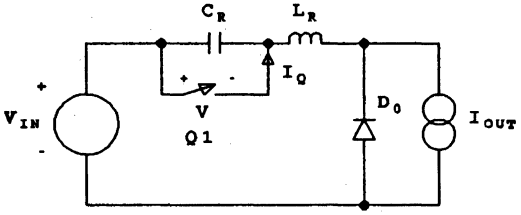


Fig. 2 - Resonant Switch Implementation

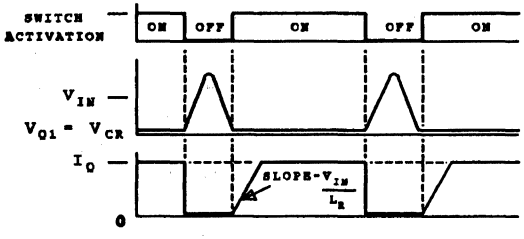


Fig. 3 - General Waveforms

ZVS Benefits

- Zero power "Lossless" switching transitions
- Reduced EMI / RFI at transitions
- No power loss due to discharging C_{OSS}
- No higher peak currents, (ie. ZCS) same as square wave systems
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and component ***L & C***

- Reduced gate drive requirements (no "Miller" effects)

Short circuit tolerant

ZVS Differences:

- Variable frequency operation (in general)
- Higher off-state voltages in single switch, unclamped topologies
- Relatively new technology - users must climb the learning curve
- Conversion frequency is inversely proportional to load current
- A more sophisticated control circuit may be required

ZVS Design Equations

A zero voltage switched Buck regulator will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevant polarities are shown in Fig. 4.

Typical design procedure guidelines and "shortcuts" will be employed during the analysis' for the purpose of brevity. At the onset, all components will be treated as though they were ideal which simplifies the generation of the basic equations and relationships. As this section progresses, losses and non-ideal characteristics of the components will be added to the formulas. The timing summary will expound upon the equations for a precise analysis.

Another valid assumption is that the output filter section consisting of output inductor L_o and capacitor C_o has a time constant several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value L_R and the magnetizing current ΔI_{Lo} as well as the inductor's DC resistance is negligible. In addition, both the input voltage V_{IN} and output voltage V_O are purely DC, and do not vary during a given conversion cycle. Last, the converter is operating in a closed loop configuration which regulates the output voltage V_O.

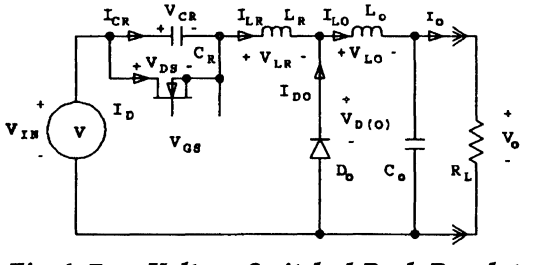


Fig. 4 -Zero Voltage Switched Buck Regulator

Initial Conditions: Time interval < t_0

Before analyzing the individual time intervals, the initial conditions of the circuit must be defined. The analysis will begin with switch Q_1 on, conducting a drain current I_D equal to the output current I_o, and $V_{DS} = V_{CR} = 0$ (ideal). In series with the switch Q_1 is the resonant inductor L_R and the output inductor L_O which also conduct the output current I_O. It has been established that the output inductance L_O is large in comparison to the resonant inductor L_R and all components are ideal. Therefore, the voltage across the output inductor V_{Lo} equals the input to output voltage differential; $V_{Lo} = V_{IN} - V_O$. The output filter section catch diode D_o is not conducting and sees a reverse voltage equal to the input voltage; $V_{Do} = V_1$, observing the polarity shown in Figure 4.

Table I - INITIAL CONDITIONS

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=V_{CR}=0$; $I_D=I_{LR}=I_{LO}=I_O$
D_O	OFF	$V_{DO}=V_{IN}$; $I_{DO}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
L_O		$V_{LO}=V_{IN}-V_O$; $I_{LO}=0$

Capacitor Charging State: t_0 - t_1

The conversion period is initiated at time t_0 when switch Q_1 is turned OFF. Since the current through resonant inductor L_R and output inductor L_O cannot change instantaneously, and no drain current flows in Q_1 while

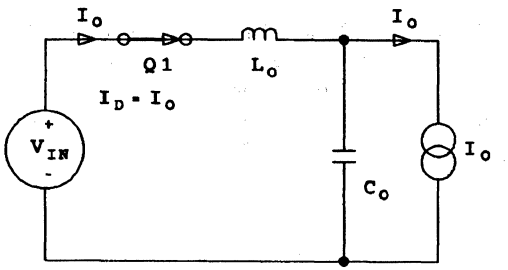


Fig. 5 - Simplified Model

$$V_{CR}(t) = \frac{I_O t}{C_R} \quad ; \quad t_{01} = \frac{C_R V_{IN}}{I_O}$$

$$I_{CR} = I_O \qquad for\ t_0 < t < t_1$$

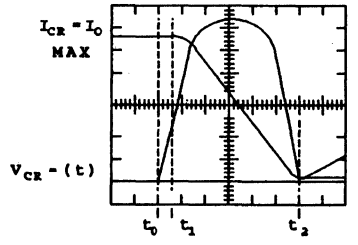


Fig. 6 - Resonant Capacitor Waveforms

it is off, the current is diverted around the switch through the resonant capacitor C_R. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage ($V_{CR} = V_{IN}$). ***Since*** the current is not changing, neither is the voltage across resonant inductor L_R.

At time t_0 the switch current I_D "instantly" drops from I_O to zero. Simultaneously, the resonant capacitor current I_{CR} snaps from zero to I,, while the resonant inductor current I_{LR} and output inductor current I_{LO} are constant and also equal to I_O during interval t_{01}. Voltage across output inductor L_O and output catch diode D_O linearly decreases during this interval due to the linearly increasing voltage across resonant capacitor C_R. At time t_1, V_{CR} equals V_{IN}, and D_O starts to conduct.

Table II - CAPACITOR CHARGING: $t_0 - t_1$

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$I_D = 0$; $V_{DS(t)} = V_{CR(t)}$
C_R	Charging	$I_{CR} = 0$; $V_{CR(t)}$ RISES LINEARLY $V_{CR(t0)} = 0$; $V_{CR(t1)} = V_{IN}$
L_R		$I_{LR(t)} = I_O$; $V_{LR} = 0$
D_O	OFF	$V_{DO(t0)} = V_{IN}$; $V_{DO(t1)} = 0$; DECREASES LINEARLY
L_O		$V_{LO(t0)} = V_{IN} - V_O$; $V_{LO(t1)} = -V_O$ DECREASES LINEARLY ; $I_{LO} = I_O$

Resonant State: $t_1 - t_2$

The resonant portion of the conversion cycle begins at t_1 when the voltage across resonant capacitor V_{CR} equals the input voltage V_{IN}, and the output catch diode begins conducting. At t_1, current through the resonant components I_{CR} and I_{LR} equals the output current I_O.

The stimulus for this series resonant L-C circuit is output current I_O flowing through the resonant inductor prior to time t_1. The ensuing resonant tank current follows a cosine function beginning at time t_1, and ending at time t_2. At the natural resonant frequency ω_R, each of the ***L-C*** tank components exhibit an impedance equal to the tank impedance, Z_R. Therefore, the peak voltage across C_R and switch Q_1 are a function of Z_R and I_O.

The instantaneous voltage across C_R and Q_1 can be evaluated over the resonant time interval using the following relationships:

$$V_{CR(t)} = V_{CR(t1)} + \frac{I_O}{\omega_R C_R} \sin[\omega_R (t - t_1)]_{t_1}^{t_2}$$

$$Z_R = 1/\omega_R C_R \quad ; \quad V_{CR(t1)} = V_{IN}$$

$$\therefore \quad V_{CR(t)} = V_{IN} + I_O Z_R \sin[\omega_R (t - t_1)]_{t_1}^{t_2}$$

Of greater importance is the ability to solve the equations for the precise off-time of the switch. This off-time will vary with line and load changes and the control circuit must respond in order to facilitate true zero ***voltage*** switching. While some allowance does exist for a fixed off time technique, the degree of lati-

tude is insufficient to accommodate typical input and output variations, The exact time is obtained by solving the resonant capacitor voltage equations for the condition when zero voltage is attained.

$$Let\ V_{CR(t)} = 0\ ;\ I_O Z_R\ SIN(\omega_R(t-t_1)) = -V_{IN}$$

The equation can be further simplified by extracting the half cycle (180 degrees) of conduction which is a constant for a given resonant frequency, and equal to π/ω_R.

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin \left[\frac{V_{IN}}{I_O Z_R}\right]_{t_1}^{t_2}$$

The resonant component current ($I_{CR} = I_{LR}$) is a cosine function between time t_1 and t_2, described as:

$$I_{CR(t)} = I_O \cos\left[\omega_R(t-t_1)\right]_{t_1}^{t_2}$$

The absolute maximum duration for this interval occurs when 270 degrees ($3\pi/2\omega_R$) of resonant operation is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line voltage are approached.

Contributions of line and load influences on the resonant time interval t_{12} can be analyzed individually as shown in Figs. 7 and 8.

Prior to time t_1, the catch diode D_O was not conducting. Its voltage, V_{DO}, was linearly decreasing from V_{IN} at time t_0 to zero at t_1 while input source V_{IN} was supplying full output current, I_O. At time t_1, however, this situation changes as the resonant capacitor initiates resonance, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage, V_{DO}, changes polarity as it begins to conduct, supplementing the decreasing resonant inductor current with diode current I', extracted from stored energy in output inductor L_O. The diode current waveshape follows a cosine function during this interval, equalling I_O minus $I_{CR}(t)$.

Also occurring at time t_1, the output filter inductor L_O releases the stored energy required

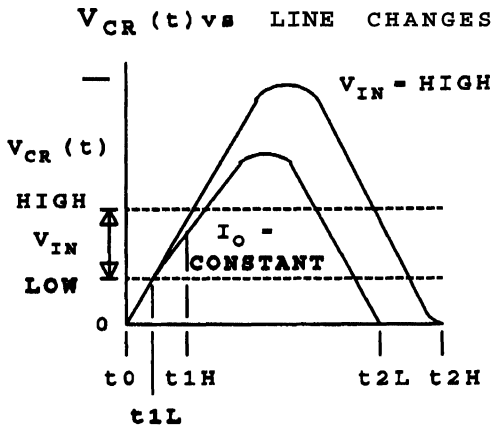


Fig. 7 -- Resonant Capacitor Voltage vs. Line

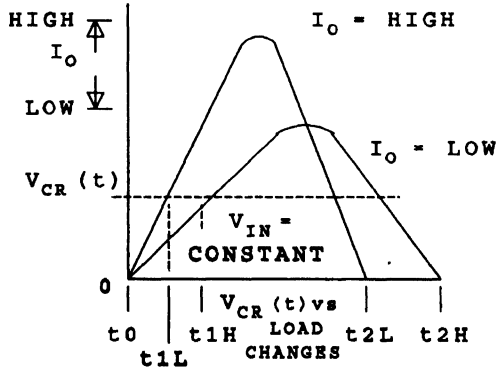


Fig. 8 -- Resonant Capacitor Voltage vs. Load

to maintain a constant output current I_O. Its reverse voltage is clamped to the output voltage V_O minus the diode voltage drop V_{DO} by the convention followed by Figure 4.

Table III - RESONANT INTERVAL: $t_1 - t_2$

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$V_{DS(t)} = V_{CR(t)}$
C_R	Resonant	$V_{CR(t)} = V_{IN} + (I_O Z_R \sin(\omega_R(t-t_1)))$ $I_{CR(t)} = I_O \cos(\omega_R(t-t_1))$
L_R	Resonant	$V_{LR(t)} = [I_O Z_R \sin(\omega_R(t-t_1))$ $I_{LR(t)} = I_{CR(t)}$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$

Inductor Charging State: t_2 - t_3

To facilitate zero voltage switching, switch Q_1 is activated once the voltage V_{DS} across Q_1 and resonant capacitor V_{CR} has reached zero, occurring at time t_2. During this inductor charging interval t_{23}, resonant inductor current I_{LR} is linearly returned from its negative peak of minus I_O to its positive level of plus I_O.

The output catch diode D_O conducts during the t_{23} interval. It continues to freewheel the full output current I_O, clamping one end of the resonant inductor to ground through D_O. There is a constant voltage, $V_{IN} - V_{DO}$, across the resonant inductor. As a result, I_{LR} rises linearly, I_{DO} decreases linearly. Energy stored in output inductor L_O continues to be delivered to the load during this time period.

A noteworthy peculiarity during this **time**-span can be seen in the switch dram current waveform. At time t_2, when the switch is turned on, current is actually returning from the resonant tank to the input source, V_{IN}. This indicates the requirement for a reverse polarity diode across the switch to accommodate the bi-directional current. An interesting result is that the switch can be turned on at any time during the first half of the t_{23} interval without affecting normal operation. A separate time interval could be used to identify this region if desired.

$$\frac{dI_R}{dt} = \frac{V_{IN}}{L_R} \; ; \; dt = dI_R L_R / V_{IN}$$

$$\therefore \; t_{23} = \frac{L_R \Delta I_R}{V_{IN}}$$

$$\text{where } \Delta I_R = -I_O \text{ to } +I_O = 2I_O$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}} \quad \text{and varies with } V_{IN} \text{ and } V_O$$

Power Transfer State: t_3 - t_4

Once the resonant inductor current I_{LR} has reached I_O at time t_3, the zero voltage switched converter resembles a conventional square wave power processor. During the remainder of the conversion period, most of the pertinent waveforms approach DC conditions.

Table IV - INDUCTOR CHARGING: t_2 - t_3

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$I_{D(t)} = -I_O + ((V_{IN} + V_{DO})/L_R)t$
C_R		$V_{CR} = 0$
L_R	Charging	$V_{LR} = V_{IN} + V_{DO}$ $I_{LR(t)} = -I_O + (V_{LR}/L_R)(t-t2)$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O		$I_{LO} = I_O$; $V_{LO} = -(V_O + V_{DO})$

Assuming ideal components, with Q_1 closed, the input source supplies output current , and the output filter inductor voltage V_{LO} equals $V_{IN} - V_O$. The switch current and resonant inductor current are both equal to I_O, and their respective voltage drops are zero ($V_{DS} = V_{LR} = 0$). Catch diode voltage V_{DO} equals V_{IN}, and $I_{DO} = 0$.

In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the t_{34} interval. Variable frequency operation is actually the result of modulating the on-time as dictated by line and load conditions. Increasing the time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter. For example, if the output voltage were to drop in response to an increased load, the conversion frequency would decrease in order to raise the effective ON period. Conversely, at light loads where little energy is drawn from the output capacitor, the control circuit would adjust to minimize the t_{34} duration by increasing the conversion frequency. In summary, the conversion frequency is inversely proportional to the power delivered to the load.

$$V_O = \frac{V_{IN} t_{34}}{t_{01} + t_{12} + t_{23} + t_{34}} = \frac{V_{IN} t_{34}}{t_{03} + t_{34}}$$

$$t_{34} = \frac{V_O t_{03}}{V_{IN} - V_O}$$

Table V - POWER TRANSFER: t_3-t_4

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=I_O R_{DS(ON)}$; $I_D=I_O$
C_R		$V_{CR}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
D_O	OFF	$V_{DO}=V_{IN}$
L_O	Charging	$V_{LO}=V_{IN}-V_O$; $I_{LO}=I_O$

V_{IN} = 18 V
V_O = 5 V
I_O = 5 A

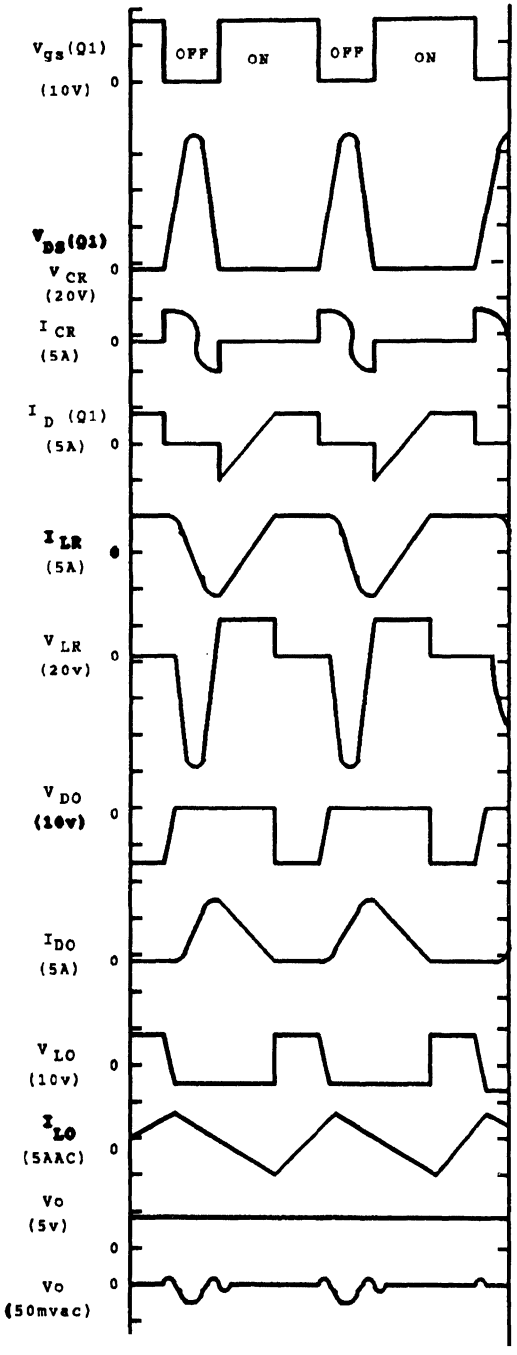


Fig. 9 -- ZVS Buck Regulator Waveforms

ZVS Converter Limitations:

In a ZVS converter operating under ideal conditions, the on-time of the switch ($t_{23}+t_{34}$) approaches zero, and the converter will operate at maximum frequency and deliver zero output voltage. In a practical design , however, the switch on-time cannot go to zero for several reasons.

First of all, the resonant tank components are selected based on the maximum input voltage V_{INmax} and minimum output current I_{Omin} for the circuit to remain resonant over all operating conditions of line and load. If the circuit is to remain zero voltage switched, then the resonant tank current cannot be allowed to go to zero. It can, however, reach I_{Omin}.

There is a finite switch on-time associated with the inductor charging interval t_{23} where the resonant inductor current linearly increases from $-I_O$ to $+I_O$. As the on-time in the power transfer interval t_{34} approaches zero, so will the converter output voltage. Therefore, the minimum on-time and the maximum conversion frequency can be calculated based upon the limitation of I_{Omin} and zero output voltage.

The limits of the four zero voltage switched time intervals will be analyzed when I_O *goes* to I_O minimum. Each solution will be retained in terms of the resonant tank frequency ω_R for generalization.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{O\min}}{V_{INmax}\omega_R}$$

$$\therefore t_{01\max} = \frac{C_R V_{INmax}}{I_{O\min}} = 1/\omega_R$$

$$t_{12\max} = \frac{3\pi}{2\omega_R} = \frac{1.5\pi}{\omega_R}$$

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax}}{I_{O\min}\omega_R}$$

$$\therefore t_{23} = \frac{2L_R I_{O\min}}{V_{INmax}} = \frac{2}{\omega_R}$$

$$t_{34\min} = 0$$

Both the minimum on-time and maximum off-time have been described in terms of the resonant tank frequency , ω_R. Taking this one step further will result in the maximum conversion frequency $f_{CONVmax}$, also as a function of the resonant tank frequency.

Minimum On-Time:

$$t_{23\min} = \frac{2}{\omega_R} = \frac{1}{\pi f_R} = \frac{0.318}{f_R}$$

Maximum Off-Time:

$$t_{01}+t_{12\min} = \frac{1+1.5\pi}{\omega_R} = \frac{0.909}{f_R}$$

The maximum conversion frequency corresponds to the minimum conversion period, $T_{CONVmin}$, which is the sum of the minimum on-time and maximum off-time:

$T_{CONVmin}$:

$$t_{01}+t_{12\min}+t_{23} = \frac{0.909+0.308}{f_R} = \frac{1.227}{f_R}$$

The maximum conversion frequency, $f_{CONVmax} = 1/T_{CONVmin}$, equals

$$F_{CONV\max} = \frac{1}{T_{CONV(\min)}} = \frac{f_R}{1.227}$$

The ratio of the maximum conversion frequency to that of the resonant tank frequency can be expressed as a topology coefficient, K_T. For this zero voltage switched Buck regulator and its derivatives, K_{Tmax} equals:

$$K_{T\max} = \frac{F_{CONVmax}}{f_R} = \frac{f_R/1.227}{f_R} = 0.815$$

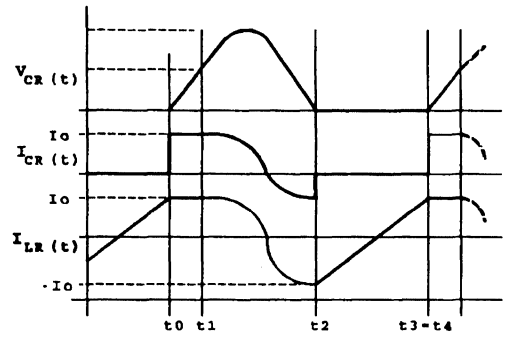


Fig. IO -- Waveforms a $F_{CONV} = K_T \cdot f_R$

In a realistic application, the output voltage of the power supply is held in regulation at V_O which stipulates that the on-time in the power processing state, t_{34}, cannot go to zero as in the example above. The volt-second product requirements of the output must be satisfied during this period, just as in any square wave converter design. Analogous to minimum duty cycle, the minimum on-time for a given design will be a function of V_{IN}, V_O and the resonant tank frequency, ω_R.

Although small, a specific amount of energy is transferred from the input to the output during the capacitor charging interval t_{01}. The voltage into the output filter section linearly decreases from V_{IN} at time t_0 to zero at t_1, equal to an average value of $V_{IN}/2$. In addition, a constant current equal to the output current I_O was being supplied from the input source. The average energy transferred during this interval is defined as:

$$W_{IN} = \frac{1}{2} V_{IN} I_O t_{01} = \frac{V_{IN} I_O}{2} \frac{C_R V_{IN}}{I_O} = \frac{V_{IN}^2 C_R}{2}$$

The equation can be reorganized in terms of C_R and ω_R as:

$$W_{IN} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

This minimum energy can be equated to minimum output watts by dividing it by its conversion period where t_{34} equals zero. **Topology** coefficient K-r will be incorporated to define the ratio of the maximum conversion frequency (minimum conversion period) to that of the resonant tank frequency, ω_R.

$$W_{IN} = P_O T_{CONV} \quad , \quad Where \; T_{CONV} = \frac{7.71}{\omega_R}$$

$$W_{IN} = P_{O\min} \frac{7.71}{\omega_R} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

$$P_{O\min} = V_O I_{O\min} = \frac{V_{IN}^2 I_{O\min}}{2(7.71) V_{IN\max}}$$

This demonstrates that a zero power output is **unobtainable** in reality. The same is true for the ability to obtain zero output voltage. The equation can be rewritten as:

$$V_{O\min} = \frac{V_{IN}^2}{2(7.71) V_{IN\max}} = \frac{0.065\, V_{IN}^2}{V_{IN\max}}$$

Solving for the highest minimum output voltage, the worst case for occurs when I_O equals I_{Omin} and V_{IN} is at its maximum, V_{INmax}.

$$V_{O\min} = 0.065\, V_{IN\max} \; ; \quad \approx 6.5\%\; V_{IN\max}$$

$$P_{O\min} = 0.065\, V_{IN\max} I_{O\min} \; ; \quad \approx 6.5\%\; P_{IN\min}$$

Under normal circumstances the circuit will be operating far above this minimum requirement. In most applications, the amount of power transferred during the capacitor charging interval t_{01} can be neglected as it represents less than seven percent (7%) of the **minimum** input power. This corresponds to less than one percent of the total input power assuming a **10:1** load range.

ZVS Effective Duty Cycles:

A valid assumption is that a negligible amount of power is delivered to the load during the capacitor charging interval t_{01}. **Also,** no power is transferred during the resonant period from t_{12}. Although the switch is on during period t_{23}, it is only recharging the

resonant and output inductors to maintain the minimum output current, I_{Omin}. In summary, NO output power is derived from V_{IN} during interval t_{03}.

The power required to support V_O at its current of I_O is obtained from the input source during the power transfer period t_{34}. Therefore, an effective "duty cycle" can be used to describe the power transfer interval t_{34} to that of the entire switching period, t_{04}, or T_{CONV}.

ZVS - Effective Duty Cycle Calculations:

$$\text{"Duty Cycle"} = \frac{V_O}{V_{IN}} = \frac{t_{34}}{t_{04}}$$

$$\text{"Duty Cycle"} = \frac{t_{34}}{t_{01}+t_{12}+t_{23}+t_{34}}$$

And can be analyzed over line and load ranges using previous equations for each interval.

Accommodating Losses in the Design Equations:

Equations for zero voltage switching using ideal components and circuit parameters have been generated, primarily to understand each of the intervals in addition to computer modeling purposes. The next logical progression is to modify the equations to accommodate voltage drops across the components due to series impedance, like $R_{DS(on)}$, and the catch diode forward voltage drop. These two represent the most significant loss contributions in the buck regulator model. Later, the same equations will be adapted for the buck derived topologies which incorporate a transformer in the power stage.

The procedure to modify the equations is straightforward. Wherever V_{IN} appears in the equations while the switch is on it will be replaced by $V_{IN}-V_{DS(on)}$, the latter being a function of the load current I_O. The equations can be further adjusted to accept changes of $R_{DS(on)}$ and V_F, etc. with the device junction temperatures. Resonant component initial tolerances, and temperature variations likewise could optionally be evaluated.

A computer program to calculate the numerous time intervals and conversion frequencies as a function of line and load can simplify the design process, if not prove to be indispensable. Listed in the Appendix of this section is a BASIC language program which can be used to initiate the design procedure.

To summarize: When the switch is on, replace V_{IN} with $(V_{IN}-V_{DS(on)}) = (V_{IN}-I_O \cdot R_{DS(on)})$. When the free-wheeling diode is on, replace V_O with (V_O+V_F).

$$t_{01} = \frac{C_R(V_{IN}-I_O R_{DS(on)})}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R}\arcsin\left[\frac{V_{IN}-I_O R_{DS(on)}}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}-I_O R_{DS(on)}}$$

$$t_{34} = \frac{(V_O+V_F)(t_{01}+t_{12}+t_{23})}{(V_{IN}-I_O R_{DS(on)})-(V_O+V_F)}$$

$$Z_R = \frac{V_{INmax}-R_{DS(on)} I_{O\,min}}{I_{O\,min}}$$

Transformer Coupled Circuit Equations:

The general design equations for the Buck topology also apply for its derivates; namely the forward, half-bridge, full-bridge and push-pull converters. Listed below are the modifications and circuit specifics to apply the previous equations to transformer coupled circuits.

General Transformer Coupled Circuits. Maintaining the resonant tank components on the primary side of the transformer isolation boundary is probably the most common and simplest of configurations. The design procedure begins by transforming the output voltage and current to the primary side through the turns ratio, N. The prime (') designator will be used to signify the translated variables as seen by the primary side circuitry.

$$N = \frac{Primary\ Turns}{Secondary\ Turns}$$

$I_O' = I_O/N$; $V_O' = V_O \cdot N$; and $Z_O' = Z_O \cdot N^2$

To satisfy the condition for resonance, $I_R < I_O'$

$$I_R \le I_O' = I_O/N \ ; \ Z_R \le \frac{V_{INmax}}{I_{O'\,min}} = \frac{V_{INmax} N}{I_O}$$

The resonant tank component equations now become:

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax} N}{I_{Omin} \omega_R}$$

Note: the calculated resonant inductance value does not include any series inductance, typical of the transformer leakage and wiring inductances.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{Omin}}{N V_{INmax} \omega_R}$$

Note: the calculated resonant capacitor value does not include any parallel capacitance, typical of a MOSFET output capacitance, C_{OSS}, in shunt. Multi-transistor variations of the buck topology should accommodate all switch capacitances in the analysis.

Timing Equations (including N):

$$t_{01} = \frac{C_R V_{IN} N}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin \left[\frac{V_{IN} N}{I_O Z_R} \right]_{t1}^{t2}$$

$$t_{23} = \frac{2 L_R I_O}{V_{IN} N}$$

$$t_{34} = \frac{N V_O (t_{01} + t_{12} + t_{23})}{V_{IN} - N V_O}$$

$$T_{CONV} = t_{01} + t_{12} + t_{23} + t_{34}$$

Determining Transformer Turns Ratio (N): The transformer turns ratio is derived from the equations used to define the power transfer interval t_{34} in addition to the maximum off-time, t_{03}. While this may first seem like an iterative process, it simplifies to the volt-second product relationship described. The general equations are listed below.

The turns ratio N is derived by substituting $N \cdot V_O$ for the output voltage V_O in the power transfer interval t_{34} equation. Solving for N results in the relationship:

$$N V_O / V_{IN} = t_{34} / (t_{01} + t_{12} + t_{23} + t_{34})$$

$$N = \frac{V_{IN\,min} t_{34}}{V_O t_{04}}$$

The transformer magnetizing and leakage inductance is part of the resonant inductance. This requires adjustment of the resonant inductor value, or both the resonant tank impedance Z_R and frequency ω_R will be off-target. One

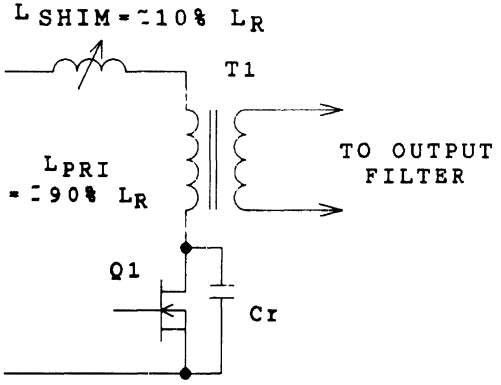


Fig. 11 -- Transformer Inductance "Shim"

option is to design the transformer inductance to be exactly the required resonant inductance, thus eliminating one component. For precision applications, the transformer inductance should be made slightly smaller than required, and "shimmed" up with a small inductor.

Expanding ZVS to Other Topologies

ZVS Forward Converter - Single Ended: The single ended forward converter can easily be configured for zero voltage switching with the addition of a resonant capacitor across the switch. Like the buck regulator, there is a high voltage excursion in the off state due to resonance, the amplitude of which varies with line and load. The transformer can be designed so that its magnetizing and leakage inductance equals the required resonant inductance. This simplifies transformer reset and eliminates one component. A general circuit diagram is shown in Fig. 12 below. The associated waveforms for when L_{PRI} equals L_R are shown in Fig. 13.

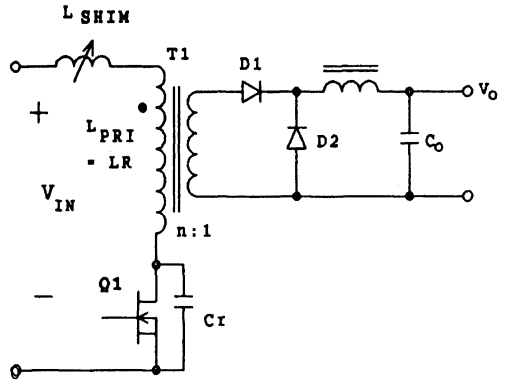
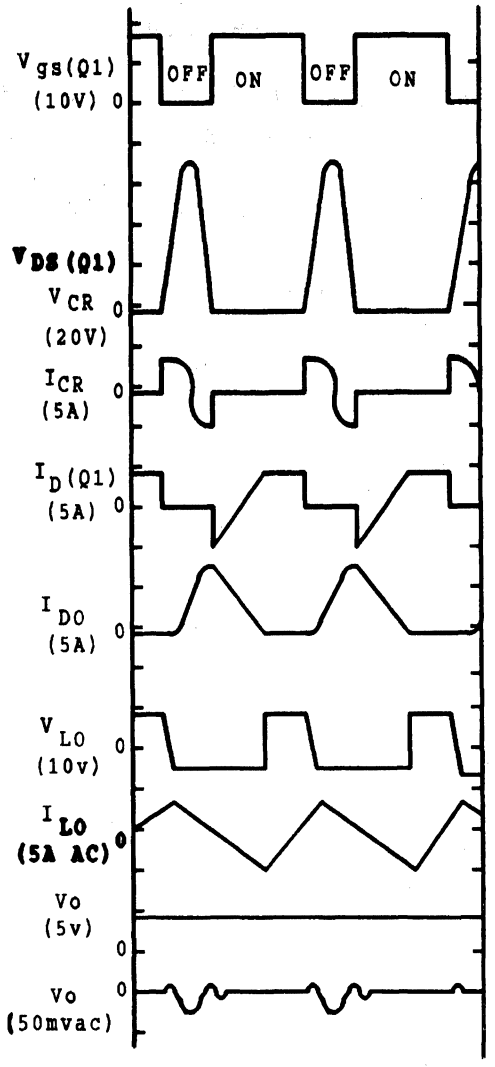


Fig. 12 -- ZVS Forward Converter



ZVS Clamped Configurations -- Half and Full Bridge Topologies: Zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains similar, there is a difference in the resonant t_{12} interval.

While single switch converters have high off-state voltage, the bridge circuits clamp the switch peak voltages to the DC input rails, reducing the switch voltage stress. This alters the duration of the off segment of the resonant interval, since the opposite switch(es) must be activated long before the resonant cycle is completed. In fact, the opposite switch(es) should be turned on immediately after their voltage is clamped to the rails, where their drain to source voltage equals zero. If not, the resonant tank will continue to ring and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes.

Examples of this are demonstrated in Figs. 14 and 15. To guarantee true zero voltage switching, it is recommended that the necessary sense circuitry be incorporated.

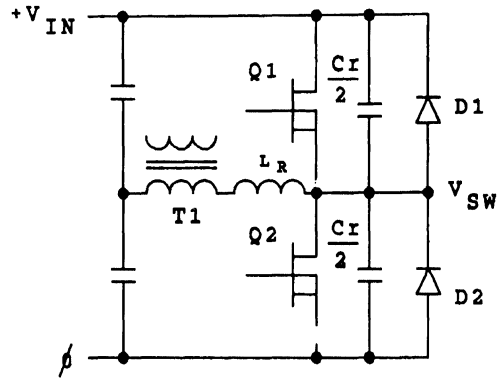


Fig. 14 -- Clamped ZVS Configuration

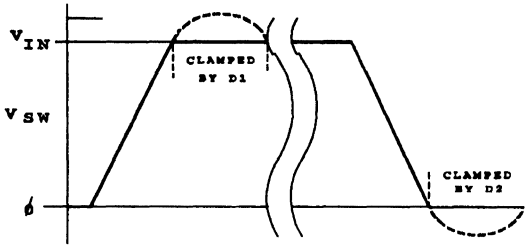


Fig. 15 -- Clamped ZVS Waveforms

ZVS Half Bridge: The same turns ratio, N, relationship applies to the half bridge topology when V_{IN} in the previous equations is considered to be one-half of the bulk rail-to-rail voltage. V_{IN} is the voltage across the transformer primary when either switch is on.

Refer to the circuit and waveforms of Figs. 14 and 15. C_R, the resonant capacitor becomes the parallel combination of the two resonant capacitors, the ones across each switch. Although the resonant inductor value is unaffected, all series leakage and wiring inductance must be taken into account.

The off state voltages of the switches will try to exceed the input bulk voltage during the resonant stages. **Automatic** clamping to the input bulk rails occurs by the MOSFET body diode, which can be externally shunted with a higher performance variety. Unlike the forward converter which requires a core reset equal to the applied volt second product, the bidirectional switching of the **half** (and full) bridge topology facilitate automatic core reset during consecutive switching cycles [11,12].

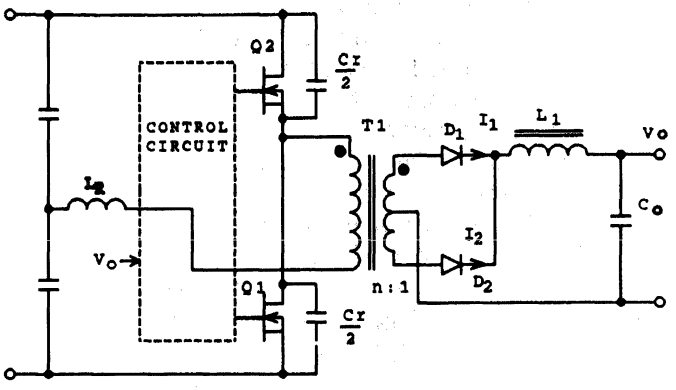


Fig. 16 -- ZVS Half Bridge Circuit

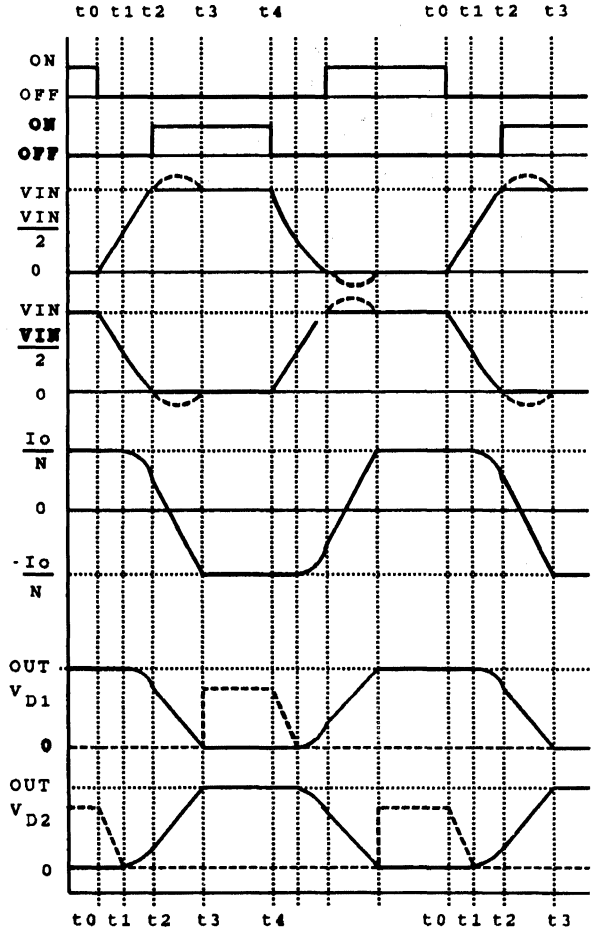


Fig. 17 -- ZVS Half Bridge Wavefoms

ZVS Full Bridge: The equations represented for the forward topology apply equally well for one conversion cycle of the full bridge topology, including the transformer turns ratio. Since the resonant capacitors located at each switch are "in-circuit" at all times, the values should be adjusted accordingly. As with the half bridge converter, the resonant capacitors' voltage will exceed the bulk rails, and clamping via the FET body diodes or external diodes to the rails is common [13].

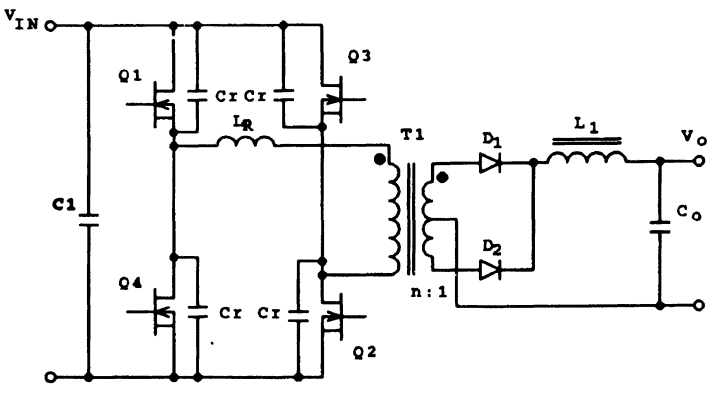


Fig. 18 -- ZVS Full Bridge Circuit

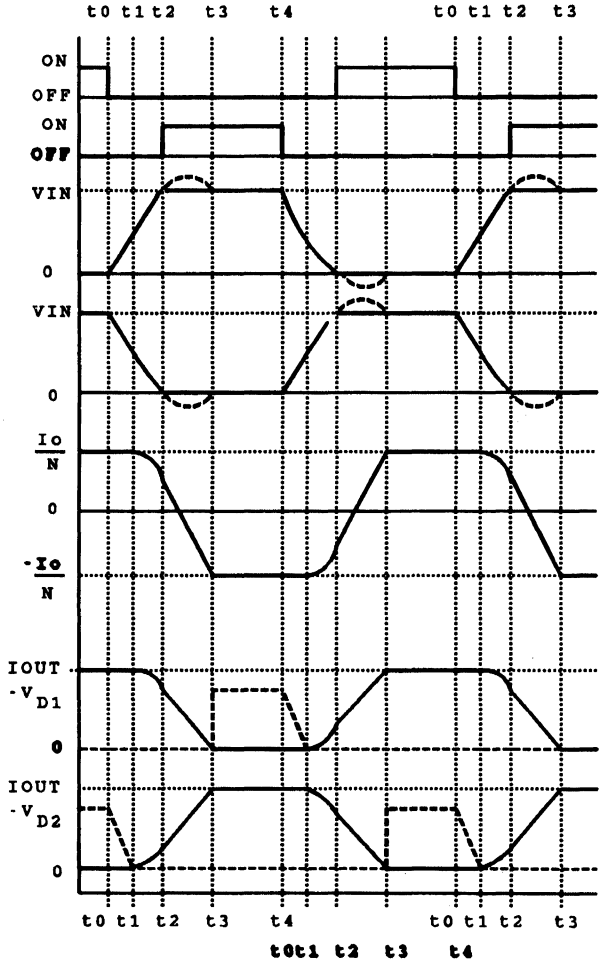


Fig. 19 -- ZVS Full Bridge Wavefoms

ZVS Design Procedure

Buck Derived Topologies -- Continuous output Current:

1. List all input/output specs and ranges.

   V_{IN} min & max ; Vo ; I_O min & max

2. Estimate the maximum switch voltages. For unclamped applications (buck and forward):

   $V_{DSmax} = V_{INmax}(1 + (I_{Omax}/I_{Omin})$

   Note: Increase I_{Omin} *if* V_{DSmax} is too high if possible).

   For clamped applications (bridges): $V_{DSmax} = V_{INmax}$

3. Select a resonant tank frequency, ω_R (HINT: $\omega_R = 2\pi f_R$).

4. Calculate the resonant tank impedance and component values.

5. Calculate each of the interval durations (t_{01} thru t_{34}) and their ranges as a function of all line and load combinations.
   (See Appendix for a sample computer program written in BASIC)

   Additionally, summarize the results to establish the range of conversion frequencies, peak voltages and currents, etc.

6. **Analyze the results.** Determine if the frequency range is suitable for the application. If not, a recommendation is to limit the load range by raising I_{Omin} and start the design procedure again. Verify also that the design is feasible with existing technology and components.

7. Finalize the circuit specifics and details.

- ☐ Derive the transformer turns ratio. (non-buck applications)
- ☐ Design the output filter section based upon the lowest conversion frequency and output ripple **current,I_O(ac).**
- ☐ Select applicable components; diode, MOSFET etc.

8. Breadboard the circuit **carefully** using RF techniques wherever possible. Remember -- parasitic inductances and capacitances prefer to resonate upon stimulation, and quite often, **unfavorably.**

9. Debug and modify the circuit as required to accommodate component parasitics, layout concerns or packaging considerations.

Avoiding Parasitics

Ringing of the catch diode junction capacitance with circuit inductance (and package leads) will significantly degrade the circuit performance. Probably the most common solution to this everyday occurrance in square wave converters is to shunt the diode with an R-C snubber. Although somewhat dissipative, a compromise can be established between snubber losses and parasitic overshoot caused by the ringing. Unsnubbed examples of various applicable diodes are shown in Fig. 20 below.

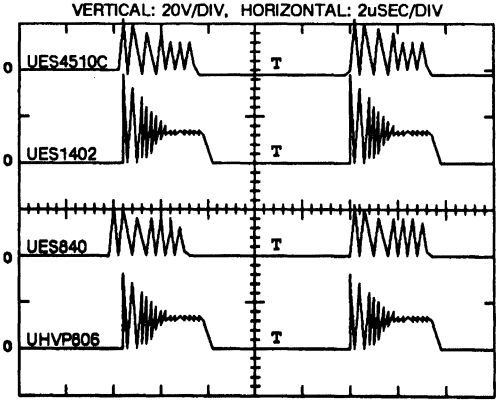


Fig. 20 -- Catch Diode Ringing

Multiresonant ZVS Conversion

Another technique to avoid the parasitic resonance involving the catch diode capacitance is to shunt it with a capacitor much larger than the junction capacitance. Labelled C_D, this element introduces favorable switching characteristics for both the switch and catch diode. The general circuit diagram and associated waveforms are shown below, but will not be explored further in this presentation [14,15].

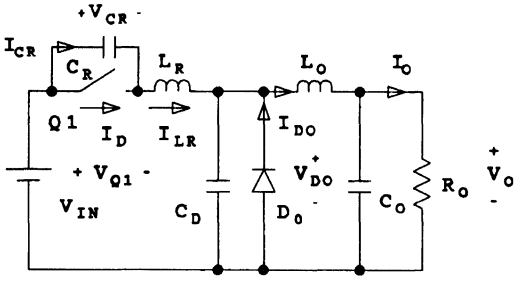


Fig. 21 -- Multiresonant ZVS Circuit

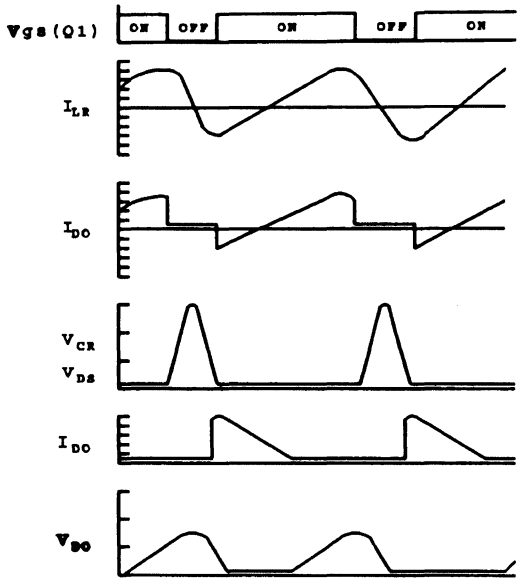


Fig. 22 -- Multiresonant Waveforms

Current Mode Controlled ZVS Conversion

Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise ON time of the power switch -- an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

Principles of operation. Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry. When the resonant capacitor voltage crosses zero, the UC3864 output goes high. This turns ON the power switch and recycles the UC3843A to initiate the next current mode controlled period. The UC3864 fault circuitry functions, but its error amplifier and VCO are not used.

ZVS Forward Converter -- Design Example

1. List circuit specifications:

V_{IN} = 18 to 26 V
V_O = 5.0 V ; I_O = 2.5 to 10 A

2. Estimate the maximum voltage across the switch:

$V_{DSmax} = V_{INmax}(1 + (I_{Omax}/I_{Omin}))$
$=26\cdot(1+(10/2.5)) = 26\cdot5 = 130$ V

3. Select a resonant tank frequency, ω_R.

A resonant tank period frequency of 500KHz will be used. It was selected as a compromise between high frequency operation and low parasitic effects of the components and layout.

f_R = 500KHz ; $\omega_R = 3.14 \cdot 10^6$ radians/sec

4. Calculate the resonant tank impedance and component values.

Resonant tank impedance, $Z_R > V_{INmax}/I_{Omin}$

To accommodate the voltage drop across the MOSFET, calculate $V_{DS(on)min}$, which equals $R_{DS(on)}I_{Omin} = 0.8 \cdot 2.5 = 2V$

$Z_R = (V_{INmax} - V_{DSmin})/I_{Omin}$

$Z_R = (26-2)/2.5 = 10\ \Omega$

$C_R = 1/(Z_R\omega_R) = 1/(10 \cdot 3.14 \cdot 10^6) = 32nF$

$L_R = Z_R/\omega_R = 10/3.34 \cdot 10^6 = 3.18\mu H$

5. Calculate each of the interval durations (t_{01} thru t_{34}) and ranges as they vary with line and load changes.

The zero voltage switched buck converter "gain" in kiloHertz per volt of V_{IN} and kHz per amp of I_O can be evaluated over the specified ranges. A summary of these follows:

Table VI - Interval Durations vs. Line & Load

	V_{IN}=18 I_O=2.5	V_{IN}=18 I_O=10	V_{IN}=26 I_O=2.5	V_{IN}=26 I_O=10
t_{10}	0.217	0.055	0.314	0.078
t_{12}	1.29	1.06	1.49	1.08
t_{23}	0.93	3.72	0.64	2.58
t_{34}	1.39	6.68	0.78	1.78
T_{CONV}	3.83	11.51	3.23	5.52
f_{CONV}	261kHz	87kHz	310kHz	181kHz
Transistor Switch Durations:				
t_{ON}	2.32	10.4	1.42	4.36
t_{OFF}	1.51	1.11	1.80	1.16

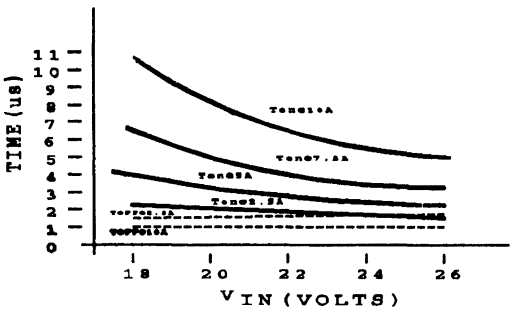


Fig. 23 - Switch Times vs. Line & Load

df_{CONV}/dV_{IN} vs I_O					
I_O =	2.5A	5A	7.5A	10A	avg
df/dV =	6.1	11.2	11.9	11.7	10.2

Highest "gain" (11.9 kHz/V) occurs near full load.

df_{CONV}/dI_O vs V_{IN}						
V_{IN} =	18	20	22	24	26	avg
df/dV =	23.3	22.1	20.5	18.8	17.3	20.4

Highest "gain" (23.3 kHz/A) occurs at V_{INmin}.

It may be necessary to use the highest gain values to design the control loop compensation for stability over all operating conditions. While this may not optimize the loop transient response for all operating loads, it will guarantee stability over the extremes of line and load.

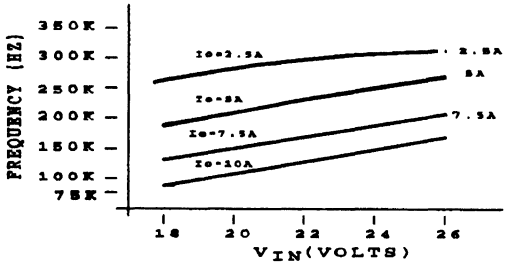


Fig. 24 - Conversion Freq. vs. Line & Load

6. Analyze the results.

The resonant component values, range of conversion frequencies, peak voltage and current ratings seem well within the practical limits of existing components and technology.

7. Finalize the circuit specifics and details based on the information obtained above.

A. Output Filter Section: Select L_O and C_O for operation at the lowest conversion frequency and designed ripple current.

B. Heatsink Requirements: An estimate of the worst case power dissipation of the power switch and output catch diode can be made over line and load ranges.

C. Control Circuit: The UC3861-64 series of controllers will be examined and programmed per the design requirements.

Programming the Control Circuit

One-shot= Accommodating Off-time Variations. The switch off-time varies with line and load by ≈ ± 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects results in an much wider excursion. For all practical purposes, a true fixed off-time technique will ***not*** work.

Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-

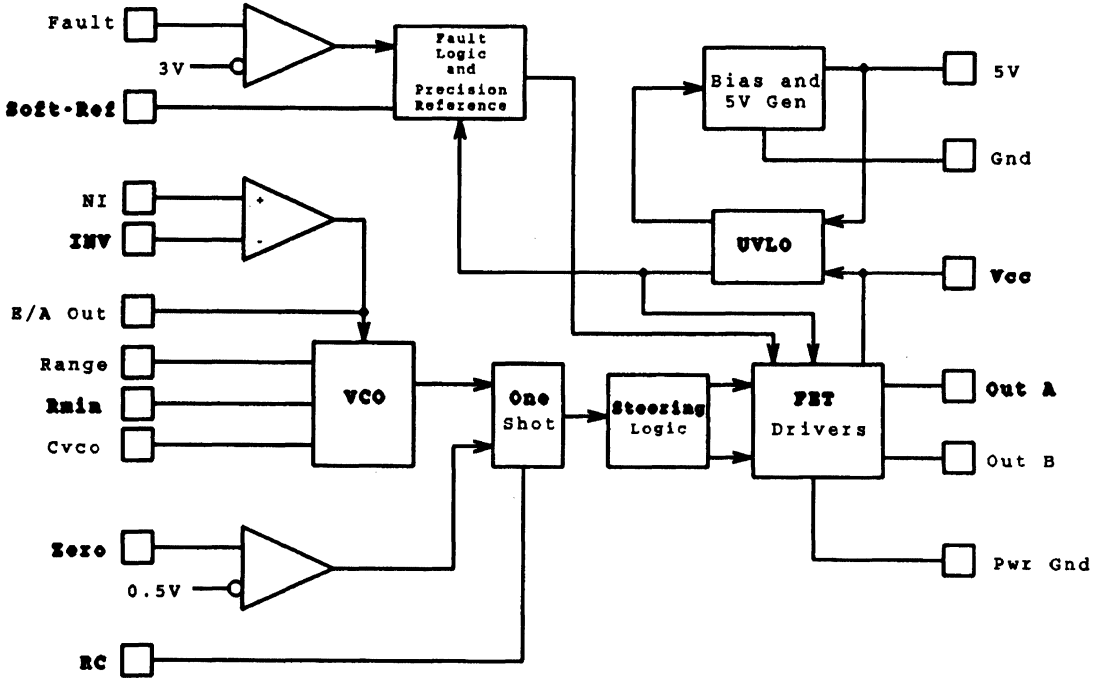


Fig. 25 -- The UC3861-64 ZVS Controllers -- Block Diagram

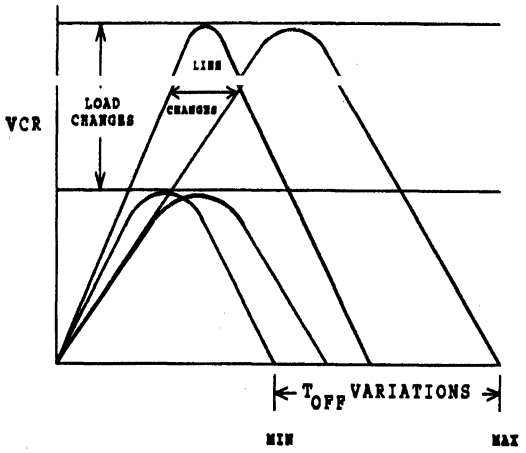


Fig. 26 -- C_R Volts & Off-time vs. Line & Load

time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

Referring to Fig. 26, in this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a 3:1 range capability and will be programmed for 2.2 uS (max), controllable down to 0.75 uS. Programming of the one-shot requires a single R-C time constant, and is straightforward using the design information and equations from the data sheet. Implementation of this feature is shown in the control circuit schematic.

Programming the VCO. The calculated range of conversion frequencies spans 87 to 310 kHz. These values will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences.

First, a minimum f_C of 75 kHz has been selected and programmed according to the following equation:

$$F_{VCOmin} = 3.6/(R_{min}C_{VCO})$$

The **maximum** f_C of 350 kHZ is programmed by:

$$F_{VCOmax} = 3.6/(R_{min} \parallel R_{range}) \cdot C_{VCO}$$

Numerous values of R_{min} and C_{VCO} will satisfy the equations. The procedure can be simplified by letting R_{min} equal 100K.

$$C_{VCO}\ (\mu F) = 0.036/f_{min}\ (\text{kHz})$$

$$R_{RANGE}\ (\text{k}\Omega) = 100/(f_{CONVmax}/f_{CONVmin} - 1)$$

where $R_{min} = 100\text{K}$, $C_{VCO} = 470\text{pF}$, $R_{RANGE} = 27\text{K}$

The VCO gain in frequency per volt from the error amplifier output is approximated by:

$$dF/dV = 1/(R_{RANGE}C_{VCO}) = 78.2\ \text{kHz/V}$$

with an approximate 3.6 volt delta from the error amplifier.

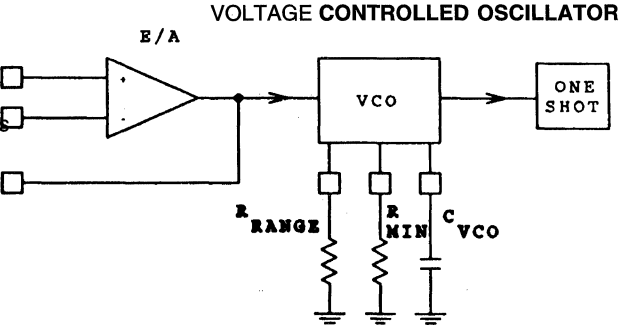


Fig. 27 -- E/A - VCO Block Diagram

Fault Protection - Soft Start & Restart Delay One of the unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latch off following fault, etc) with a single resistor.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 ms and a restart delay of approximately 200 ms. The preprogrammed ratio of 19:I (restart delay to soft start) will be utilized, however the relevant equations and relationships have also been provided for other applications. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short circuit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold.

Optional Programming of T_{SS} and T_{RD} :

Soft Start: $T_{SS} = C_{SR} \bullet$ 10K

Restart Delay: $T_{RD} = C_{SR} \bullet$ 19OK

Timing Ratio: $T_{RD}:T_{SS}$ = 19:I

Gate Drive: Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem pole outputs shows 30 ns rise and fall times into **1nF.**

Loop Compensation -- General Information. The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unlike the dual loop system of current mode control, the ZVS output filter section exhibits

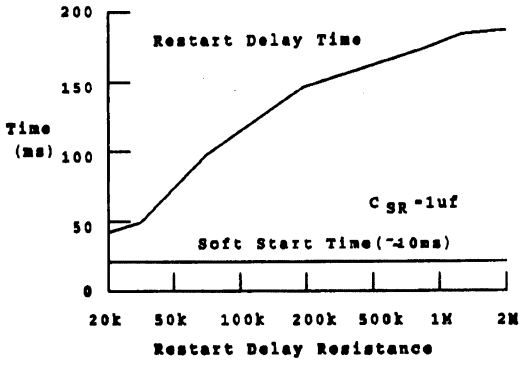


Fig. 28 -- Programming T_{SS} and T_{RD}

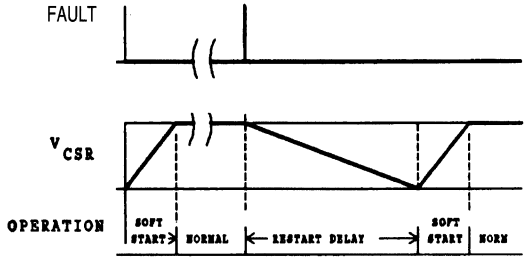


Fig. 29 -- Fault Operational Waveforms

a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for the highest low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filter's two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

A noteworthy alternative is the use of a two loop approach which is similar to current mode control, eliminating one of the output poles. One technique known as Multi-Loop Control for Quasi-Resonant Converters [18] has been

developed. Another, called Average Current Mode Control is also a suitable candidate,

$$\omega_{P1} = \frac{1}{R_{FP}C_F} \quad ; \quad \omega_{Z1} = \frac{1}{(R_{FP} \| R_{FZ})C_F}$$

$$\omega_{Z2} = \frac{1}{(R_{IP}+R_{IZ})C_I} \quad ; \quad \omega_{P2} = \frac{1}{R_{IP}C_I}$$

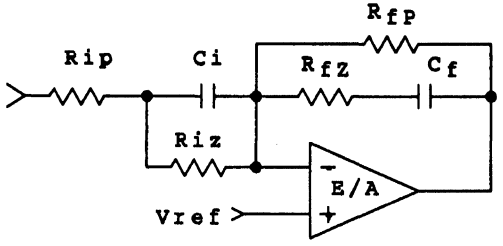


Fig. 30 - Error Amplifier Compensation

Summary

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the MOSFET output capacitance can be significant at high switching frequencies, impairing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [14,15] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of

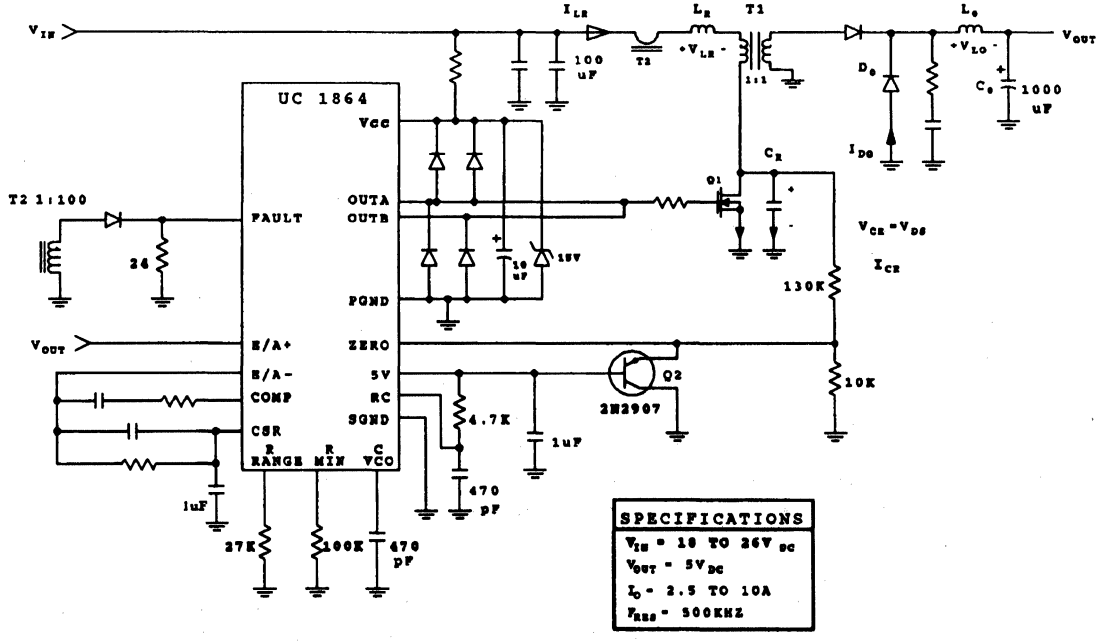


Fig. 31 - Zero Voltage Switched Forward Converter

the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detrimental parasitic generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

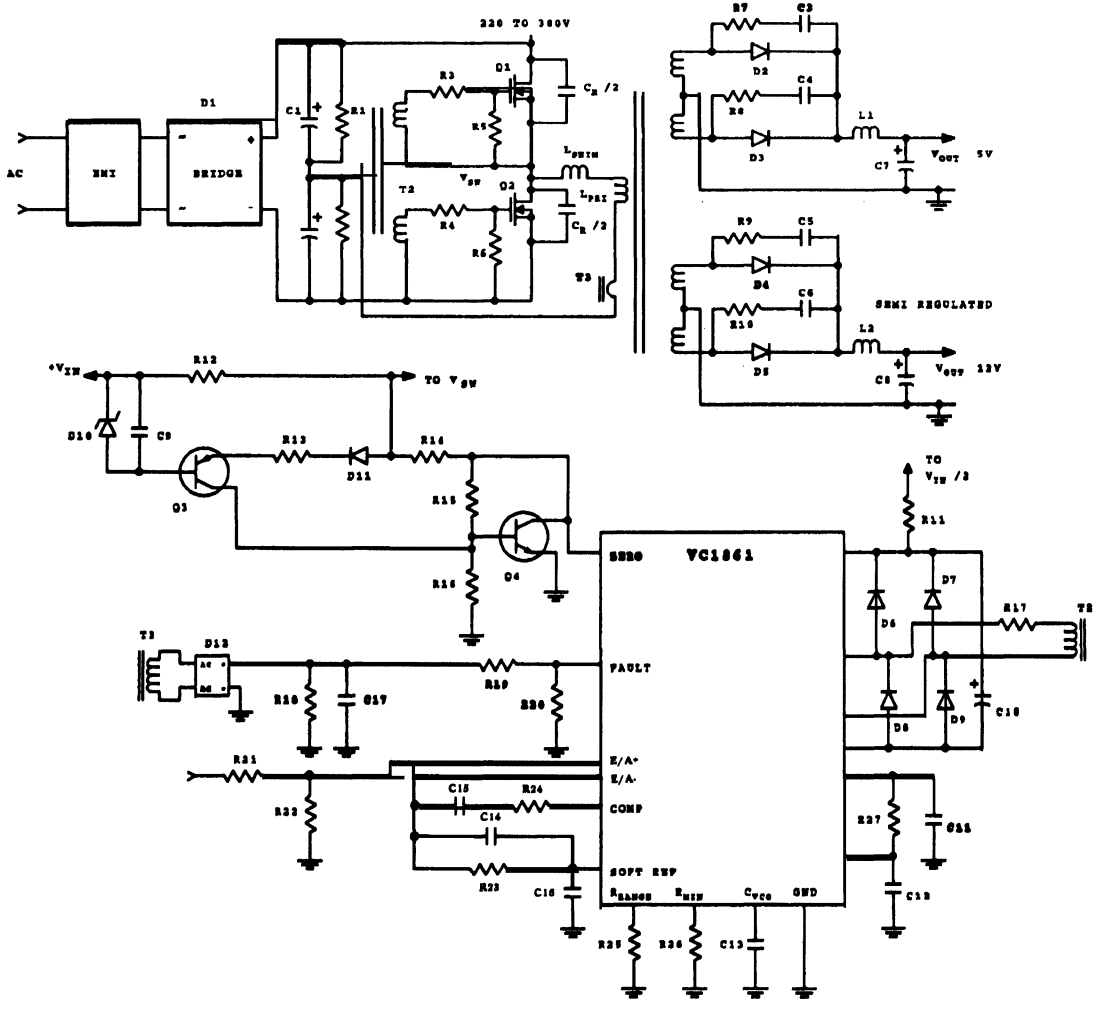


Fig. 32 -- Zero Voltage Switched Half-Bridge Converter

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```
10 ' Zero Voltage Switching Calculations and Equations
20 ' Using the Continuous Current Buck Topology
30 ' in a Typical DC/DC Converter Power Supply Application
40 '
50 PRINTER$ = "lptl:": ' Printer at parallel port #l **********
60 '
70 ' Summary of Variables and Abbreviations
80 '
90 ' Cr = Resonant Capacitor
100 ' Lr = Resonant Inductor
110 ' Zr = Resonant Tank Impedance
120 ' Fres = Resonant Tank Frequency (Hz)
130 '
140 ' VImin = Minimum DC Input Voltage
150 ' VImax = Maximum DC Input Voltage
160 ' Vdson = Mosfet On Voltage = Io*Rds
170 ' Rds = Mosfet On Resistance
180 ' Vdsmax = Peak MOSFET Off State Voltage
190 ' Vo = DC Output Voltage
200 ' Vdo = Output Diode Voltage Drop
210 ' Iomax = Maximum Output Current
220 ' Iomin = Minimum Output Current
230 '
240 ' Start with parameters for low voltage dc/dc buck regulator
250 '
260 ' ****Define 5 Vi and 5 Io data points ranging from min to max*****
270 ' (Suggestion: With broad ranges, use logarithmic spread)
280 DATA 18,20,22,24,27 : 'Vi data
290 DATA 2.5,4,6,8,10 : 'Io data
300 FRES = 500000!
310 VO = 5!
320 VDO = .8
330 RDS = .8
340 SAFT = .95
350 '
360 FOR J = 1 TO 5: READ VI(J): NEXT
370 FOR K = 1 TO 5: READ IO(K): NEXT
380 CLS
390 PRINT "For output to screen, enter 'S' or 'S'."
400 INPUT "Otherwise output will be sent to printer : ", K$
410 IF K$ = "S" OR K$ = "s" THEN K$ = "scrn:" ELSE K$ = PRINTER$
420 OPEN K$ FOR OUTPUT AS #1: CLS
430 PRINT #1, "================================================="
440 PRINT #1, "Zero Voltage Switching Times (uSec) vs. Vi, Io"
450 PRINT #1,"============================================================"
460 '
```

```
470 ' '========HERE GOES========
480 '
490 VIMAX = VI(5): IOMIN = IO(1): IOMAX = IO(5)
500 ZR = (VIMAX - (RDS * IOMIN)) / (IOMIN * SAFT)
510 WR = 6.28 * FRES
520 CR = 1 / (ZR * WR)
530 LR = ZR / WR
540 '
550 FOR J = 1 TO 5: VI = VI(J)
560    PRINT #I, USING "                    Input Voltage = ###.## V"; VI
570    FOR K = 1 TO 5: IO = IO(K)
580       RSIN = (VI / (IO * ZR)):     VDSON = RDS * IO
590 '
600       D(0, K) = IO * .00000I:   ' Compensate for later mult. by 10^6
610       D(I, K) = (CR * VI) / IO: 'dtO1
620       D(2, K) = (3.14 / WR) + (1 / WR) * ATN(RSIN / (1 - RSIN ^ 2)): 'dt12
630       D(3, K) = (2 * LR * IO) / VI: 'dt23
640       D(6, K) = D(1,  K) + D(2, K) + D(3, K): ' dt03
650       D(4, K) = ((VO + VDO) * D(6, K)) / ((VI - VDSON) - (VO + VDO)): 'dt34
660       D(5, K) = D(1  K) + D(2, K) + D(3, K) + D(4, K): 'Tconv
670 NEXT K
680 '
690 PAR$(0) = "Io (A) ="
700  PAR$(I)  =  "dt01  ="
710  PAR$(2)  =  "dt12  ="
720  PAR$(3)  =  "dt23  ="
730  PAR$(4)  =  "dt34  ="
740 PAR$(5) = "Tconv ="
750  PAR$(6)  =  "dt03  ="
760 '
770    FOR P = 0 TO 6
780       PRINT #1, PAR$(P);
790       FOR K = 1 TO 5
800          PRINT #I, USING " ####.###"; D(P, K) * I000000!;
810       NEXT K: PRINT #I,
820    NEXT P
830 PRINT #I,
840 NEXT J
850 '
860 PRINT #I, "Additional  Information:"
870  PRINT  #I, "Zr(Ohms) ="; INT(I000! * ZR) / 1000
880 PRINT #I, "wR(KRads)="; INT(WR / 1000)
890 PRINT #I. "Cr(nF)     ="; INT((I000 * CR) / 10 ^ -9) / 1000
900 PRINT #I, "Lr(uH)     ="; INT((1000 * LR) / 10 ^ -6) / 1000
910 PRINT #I, "Vdsmax     ="; VIMAX * (1 + IOMAX / IOMIN)
920 END
```

	Input Voltage = 18.00 V				
Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.218	0.136	0.091	0.068	0.054
dt12 =	1.290	1.153	1.096	1.070	1.056
dt23 =	0.931	1.490	2.235	2.980	3.725
dt34 =	1.387	1.791	2.682	4.118	6.677
Tconv =	3.825	4.571	6.103	8.236	11.511
dt03 =	2.439	2.780	3.421	4.118	4.835

	Input Voltage = 20.00 V				
Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.242	0.151	0.101	0.076	0.061
dt12 =	1.339	1.175	1.108	1.079	1.062
dt23 =	0.838	1.341	2.011	2.682	3.352
dt34 =	1.150	1.406	1.987	2.852	4.186
Tconv =	3.569	4.074	5.207	6.688	8.661
dt03 =	2.419	2.667	3.220	3.836	4.475

	Input Voltage = 22.00 V				
Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.266	0.166	0.111	0.083	0.067
dt12 =	1.390	1.198	1.120	1.087	1.069
dt23 =	0.762	1.219	1.829	2.438	3.048
dt34 =	0.988	1.153	1.557	2.136	2.958
Tconv =	3.406	3.737	4.616	5.744	7.141
dt03 =	2.418	2.584	3.060	3.608	4.183

	Input Voltage = 24.00 V				
Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.290	0.182	0.121	0.091	0.073
dt12 =	1.442	1.223	1.133	1.096	1.075
dt23 =	0.698	1.117	1.676	2.235	2.794
dt34 =	0.870	0.975	1.268	1.682	2.241
Tconv =	3.301	3.498	4.199	5.103	6.183
dt03 =	2.431	2.522	2.930	3.421	3.941

	Input Voltage = 27.00 V				
Io (A) =	2.500	4.000	6.000	8.000	10.000
dt01 =	0.327	0.204	0.136	0.102	0.082
dt12 =	0.516	1.264	1.153	1.109	1.085
dt23 =	0.621	0.993	1.490	1.987	2.483
dt34 =	0.442	0.793	0.983	1.253	1.604
Tconv =	1.906	3.254	3.763	4.451	5.254
dt03 =	1.464	2.461	2.780	3.198	3.650

Additional Information:
Zr(Ohms) = 10.526
wR(KRads)= 3140
Cr(nF) = 30.254
Lr(uH) = 3.352
Vdsmax = 135

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Average Current Mode Control of Switching Power Supplies

Lloyd Dixon

Abstract

Current mode control as usually implemented in switching power supplies actually senses and controls peak inductor current. This gives rise to many serious problems, including poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain cannot correct. Average current mode control eliminates these problems and may be used effectively to control currents other than inductor current, allowing a much broader range of topological application.

General Perspective

Current mode control is a two-loop system as shown in the simple example of Fig. 1. The switching power supply inductor is "hidden" within the inner current control loop. This simplifies the design of the outer voltage control loop and improves power supply performance in many ways, including better dynamics. The objective of this inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control. (Switch current --equal to inductor current during the "on" time--is often sensed.) If the inductor ripple current is small, peak inductor current control is nearly equivalent to average inductor current control.

In a conventional switching power supply employing a buck derived topology, the inductor is in the output. Current mode control then is actually output current control, resulting in many performance advantages. On the other hand, in a high power factor preregulator using the boost topology, the inductor is in the input. Current mode control then controls input current, allowing it to be easily conformed to the desired sinusoidal waveshape.

Peak Current Mode Control Problems

Poor noise immunity. The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop-see Fig. 1. The comparator turns the power switch off when the instantaneous current reaches the desired level. The current ramp is usually quite small compared to the programming level, especially when V_{IN} is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a subharmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

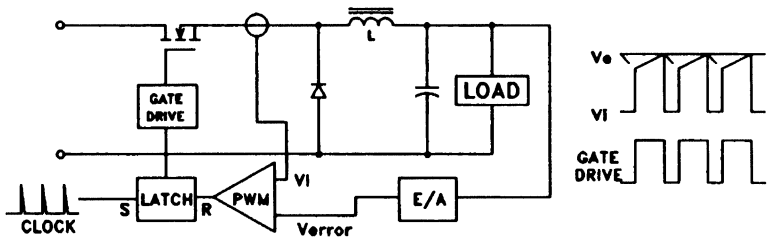

Fig. 1 - Peak Current Mode Control Circuit and Waveforms

Slope compensation required. The peak current mode control method is inherently unstable at duty ratios exceeding 0.5,

resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability. In a buck regulator the inductor current downslope equals V_O/L. With V_O constant, as it usually is, the compensating ramp is fixed and easy to calculate-but it does complicate the design. With a boost regulator in a high power factor application, the downslope of inductor current equals $(V_{IN}-V_O)/L$ and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

Peak to average current error. The peak to average current error inherent in the peak method of inductor current control is usually not a serious problem in conventional buck-derived power supplies. This is because inductor ripple current is usually much smaller than the average full load inductor current, and because the outer voltage control loop soon eliminates this error.

In high power factor boost preregulators the peak/avg error is very serious because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor current ramp makes the already poor noise immunity much worse.

Topology problems. Conventional peak current mode control actually controls inductor current. As normally used for output current control, it is most effective when applied to a buck regulator where the inductor is in the output. But for flyback or boost topologies the inductor is not in the output, the *wrong* current is controlled, and much of the advantage of current mode control is lost.

Likewise, the boost topology with its inductor at the input is well suited for input current control in a high power factor preregulator, but buck and flyback topologies are not well suited because the inductor is not in the input and the wrong current is controlled.

Average Current Mode Control

Peak current mode control operates by directly comparing the actual inductor current waveform to the current program level (set by the outer loop) at the two inputs of the PWM comparator. This current loop has low gain and so cannot correct for the deficiencies noted above.

Referring to Fig. 2, the technique of average current mode control overcomes these problems by introducing a high gain integrating current error amplifier *(CA)* into the current loop. A voltage across R_P (set by the outer loop) represents the desired current program level. The voltage across current sense resistor R_S represents actual inductor current. The difference, or current error, is amplified and compared to a large amplitude sawtooth (oscillator ramp) at the PWM comparator inputs.

The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the *CA*. Compared with peak current mode control, the current loop gain crossover frequency, f_c, can be made approximately the same, but the gain will be much greater at lower frequencies.

The result is:

1) Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor preregulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

2) Slope compensation is not required, but

there is a limit to loop gain at the switching frequency in order to achieve stability.

3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, volts away from the corresponding current error level at the input of the PWM comparator.

4) The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.

Designing the Optimum Control Loop

Gain Limitation at f_s: Switching power supply control circuits all exhibit subharmonic oscillation problems if the slopes of the waveforms applied to the two inputs of the PWM comparator are inappropriately related.

With peak current mode control, slope compensation prevents this instability.

Average current mode control has a very similar problem, but a better solution. The oscillator ramp effectively provides a great amount of slope compensation. One criterion applies in a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion puts an upper limit on the current amplifier gain at the switching frequency, indirectly establishing the maximum current loop gain crossover frequency, f_C. It is the first thing that needs to be considered in optimizing the average current mode control loop.

In the following examples, we assume that the power circuit design has been completed, and only the *CA* compensation remains to be worked out.

Example 1: Buck Regulator Output Current. The simple buck regulator shown in Fig. 2 has the following operating parameters:

Switching Frequency, f_S = 100 kHz
Input Voltage, V_{IN} = 15 - 30V
Output Voltage, V_0 = 12V
Output Current, I_O = 5A (6A O.L.)
Inductance, L = 60 μH
max. ΔI_O @ 30V (100 kHz) = 1.2A
Sense Resistance, R_S = 0.10

C_{FP} is temporarily omitted. Zero $R_F C_{FZ}$ is well below the switching frequency. Near f_s, the amplifier gain is flat. The overall current loop has only one active pole (from the inductor).

The inductor current is sensed through R_S. (How this is accomplished will be discussed later.) The inductor current waveform with its sawtooth ripple component is amplified and inverted through the CA and applied to the comparator. The inductor current downslope (while the switch is off) becomes an upslope, as shown in Fig. 2. To avoid subharmonic oscillation, this off-time CA output slope must not exceed the oscillator ramp slope. In Fig. 2, the off-time CA output slope is much less than the oscillator ramp slope, indicating that the CA gain is less than optimum.

Calculating the slopes:

Inductor Current Downslope = Vo/L
Oscillator Ramp Slope = Vs/Ts = Vsf$_s$

Where V_s is the oscillator ramp p-p voltage, T_S and f_s are the switching period and frequency.

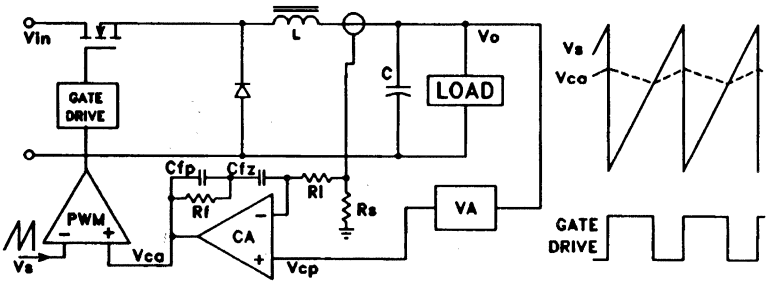

Fig. 2 - Average Current Mode Control Circuit and Waveforms

The inductor current downslope is translated into a voltage across current sense resistor R_S and multiplied by the *CA* gain, G_{CA}. This is set equal to the oscillator ramp slope to determine the *CA* gain allowed at f_S:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max\ G_{CA} = \frac{v_{CA}}{v_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (1)$$

Applying the values given in the example, and with V_S of 5Vpp, the maximum G_{CA} at the switching frequency is 25 (28dB). The current error amplifier gain at f_S is set to this optimum value by making the ratio $R_F/R_I = 25$.

The small-signal control-to-output gain of the buck regulator current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\frac{V_{IN}}{sL} = \frac{1590}{f} \quad (@30V) \qquad (2)$$

The overall open loop gain of the current loop is found by multiplying (1) and (2). The result is set equal to 1 to solve for the loop gain crossover frequency, f_c:

$$\frac{R_S}{V_S}\frac{V_{IN}}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S V_{IN}}{2\pi V_O} = \frac{f_S}{2\pi D} \qquad (3)$$

Setting the CA gain at the limit found in (1), the crossover frequency will never be less than one sixth of the switching frequency. (This is exactly the same result reported by Middlebrook [1] for peak current mode control with recommended slope compensation.) In this example, f_c is 20 kHz with V_{IN} at 15V (D= .8), and 40 kHz when V_{IN} at 30V (D= .4).

If the error amplifier had a flat gain characteristic, the phase margin at crossover would be 90° -much more than required-and the gain at lower frequencies wouldn't be much better than with peak current mode control. But zero $R_F C_{FZ}$ placed at 10 kHz, below the minimum crossover frequency, reduces the phase margin to 63°, and boosts the low frequency gain dramatically, with an integrator gain of 250K/f. It is this characteristic which causes the current loop to rapidly and accurately home in on the average current called for by the outer loop. Even though the comparator actually turns off the power switch when a *peak* inductor current is reached, this peak current level is adjusted by the current amplifier so that the average current is correct.

Fig. 3 shows the start-up waveforms of the voltages at the PWM comparator inputs and the inductor current with V_{IN} at 30V and full load. Note how the amplified and inverted inductor current downslope virtually coincides with the oscillator ramp, because the CA gain was set at the optimum level according to Equation (1). Note also that if the CA gain is increased further, not only will the off-time slope exceed the oscillator ramp slope, but the positive excursion may reach the CA compliance limit, clipping or clamping the waveform.

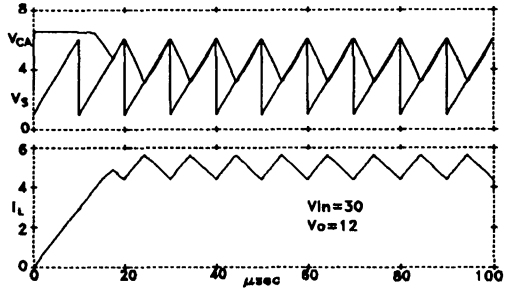

Fig. 3 - Buck Waveforms, Optimized Gain

Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at switching frequency f_s(100 kHz). This pole has one purpose-to eliminate noise spikes riding on the current waveform, the nemesis of peak current mode control. The sawtooth CA output waveform is also diminished, especially the higher order harmonics, and shifted in phase as shown in Fig. 4. The pole-zero pair (at 100 kHz and 10 kHz) reduces the phase margin at crossover to a very acceptable 45° -see Fig. 5.

The reduced amplitude and slopes of the CA waveform resulting from the 100 kHz pole might suggest that the CA gain could be in-

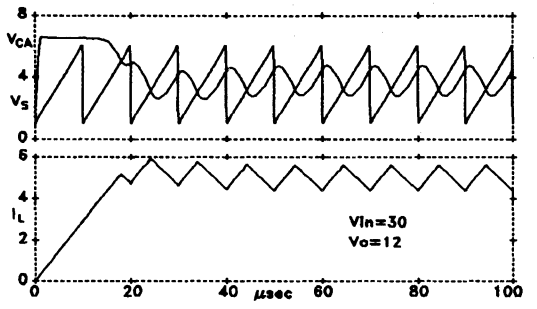

Fig. 4 - Buck with Additional Pole at f_S

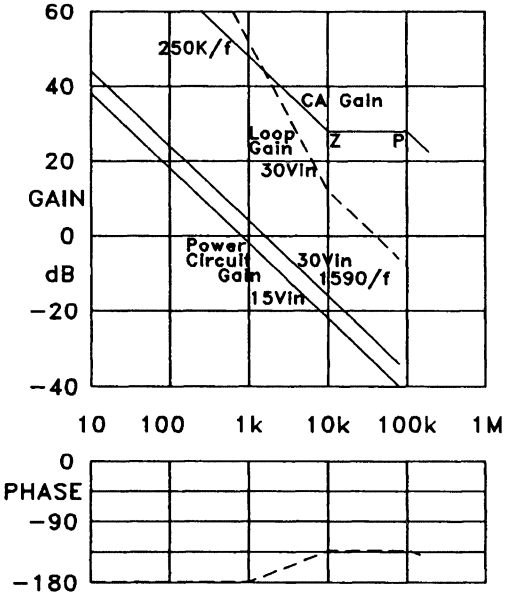

Fig. 5 - Buck Regulator Bode Plot

creased beyond the maximum value from Equation (1), but beware-Eq. (1) is valid only for a system with a single pole response at f_s, but with C_{FP} added there are now two active poles at f_s. Experimentally, increasing G_{CA} may incur subharmonic oscillation.

Discontinuous Operation. When the load current I_O becomes small, the inductor current becomes discontinuous. The current level at the continuous/discontinuous mode boundary is:

$$I_O = I_L = \frac{V_O(V_{IN}-V_O)}{V_{IN}2f_SL} \qquad (4)$$

Worst case is at max V_{IN} , when ripple current is greatest. In this example, the mode boundary occurs at $I_O(=I_L)$ of 0.2A when V_{IN} is 15V, and at 0.6A when V_{IN} is 30V.

In the discontinuous mode, below the mode boundary, changes in I_O require large duty cycle changes. In other words, the power circuit gain suddenly becomes very low. Also, the single pole characteristic of continuous mode operation with its 90° phase lag disappears, so the power circuit gain is flat-independent of frequency. The current loop becomes more stable, but much less responsive.

With peak current mode control in the discontinuous mode, peak/avg current error becomes unacceptably huge. But with average current mode control, the high gain of the current error amplifier easily provides the large duty cycle changes necessary to accommodate changes in load current, thereby maintaining good average current regulation.

Referring to Fig. 2, when the current loop is closed, the voltage across current sense resistor V_{RS} equals the current programming voltage V_{CP} (from the voltage error amplifier) at frequencies below f_S. The transconductance of the closed current loop is a part of the outer voltage control loop:

$$g = \frac{\hat{i}_L}{\hat{v}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{CP}} = \frac{1}{R_S} \qquad (5)$$

The closed loop transconductance rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

Example 2: Boost Regulator Input Current. A 1 kW off-line preregulator (Fig 6) operates with the following parameters:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
output Volts, V_O = 380Vdc
Max. O.L. I_{IN}(@90V) = 12A rms, 17A pk
L = 0.25mH
$\Delta I_L, \Delta I_{IN}$ @90V = 3.4A
R_S = 0.05Ω

The max. overload line current at min. V_{IN} corresponds to 1080W input. The max. peak overload 60Hz line current (17A) should-by design-correspond to a limit on the current programming signal, I_{CP}. The max peak 100kHz current through the switch and rectifier is 17A plus one-half ΔI_L: 17 + 3.4/2 = 18.7A

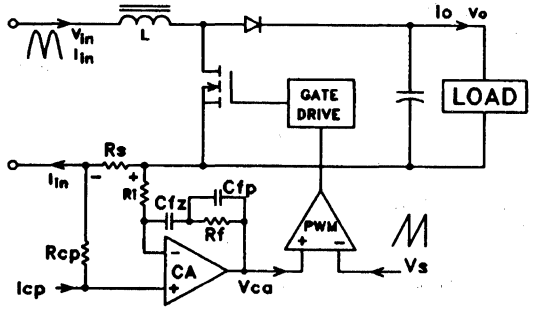

Fig. 6 - Boost Preregulator Circuit

The current downslope occurs when the power switch is off:

$$\text{Inductor Current Downslope} = (V_O - V_{IN})/L$$
$$\text{Worst case when } V_{IN} = V_O/L$$
$$\text{Oscillator Ramp Slope} = Vs/Ts = Vs\, f_s$$

Multiply the downslope by R_S and *CA* gain and set equal to the oscillator ramp slope, then solve for maximum *CA* gain:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max\ G_{CA} = \frac{v_{CA}}{v_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (6)$$

Note the form of Equation (6) is identical to the buck regulator in (1). Using the values for this application, the maximum G_{CA} is 6.58, accomplished by making R_F/R_I = 6.58.

The small-signal control-to-input gain of the current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\frac{V_O}{sL} = \frac{2420}{f} \qquad (7)$$

Note that (7) is nearly identical to (2) for the buck regulator, except the gain depends on V_O (which is constant), rather than V_{IN}.

The overall current loop gain is found by multiplying (6) and (7). The result is set equal to 1 to solve for the crossover frequency, f_C:

$$\frac{R_S}{V_S}\frac{V_O}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S}{2\pi} \qquad (8)$$

With the *CA* gain at the limit found in (6), the current loop f_C is *fixed* at $f_S/6$ (16.7 kHz).

As with the earlier example, with a flat gain error amplifier the phase margin at crossover is 90° — larger than necessary. So zero $R_F C_{FZ}$ is set at 1/2 of the minimum crossover frequency ($f_C/2 = f_S/12$ 8.33=kHz), providing a low frequency boost with an integrator gain of 55K/f. Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at 6 times the zero frequency (50 kHz) to eliminate noise spikes. Together, the zero at 8.33 kHz and the pole at 50 kHz leave a phase margin at crossover of 40°. Startup waveforms are shown in Fig. 7, and the Bode plot in Fig. 8.

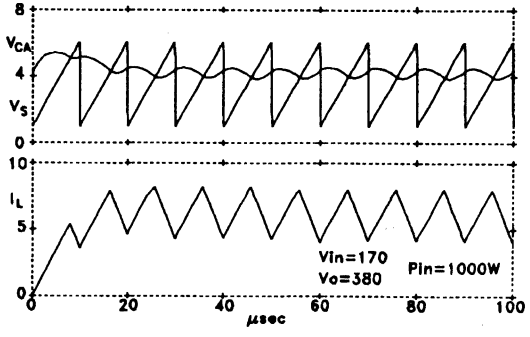

Fig. 7 - Boost Regulator Waveforms

Referring back to Fig. 6 — when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. In this case, programmed with a current source I_{CP}, the current gain of the closed current loop is:

$$G = \frac{i_L}{i_{CP}} = \frac{v_{RS}/R_S}{v_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (9)$$

The closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

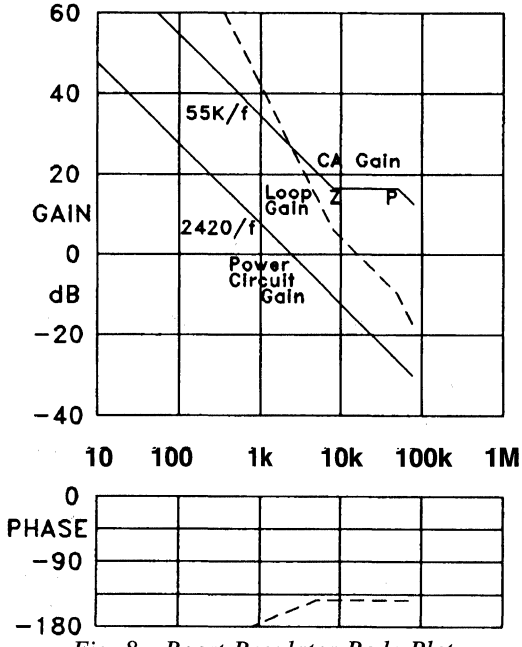

Fig. 8 - Boost Regulator Bode Plot

In a high power factor preregulator application, the current is programmed to follow the rectified line voltage. As the rectified sine wave voltage and current approaches the cusp at zero, the inductor current becomes discontinuous. Discontinuous operation can occur over a substantial portion of the line cycle, especially when line current is low at high line voltage and/or low power input. With peak current mode control, discontinuous operation results in a large peak/average current error. A large inductance is required to make ripple current small and put the mode boundary at a low current level. However, average current mode control eliminates the peak/average error. A small inductance can and should be used to reduce cost, size and weight and improve current loop bandwidth.

Figure 9 shows a boost preregulator programmed to follow a 60 Hz (rectified) sine wave input. The lower waveforms show the programmed and actual line current waveforms. (The programmed waveform has been increased by 5% to make the two waveforms visible. The actual waveform leads the programmed waveform by a small amount and has less than 0.5% 3rd harmonic distortion! The upper waveforms show the duty cycles of the switch and diode throughout the line cycle. The inductor current is continuous when the current is high, and the switch and diode duty cycles add up to 1. But as the current approaches zero crossing, operation becomes discontinuous as shown by the appearance of "dead" time (when neither the switch, the diode, or the inductor are conducting).

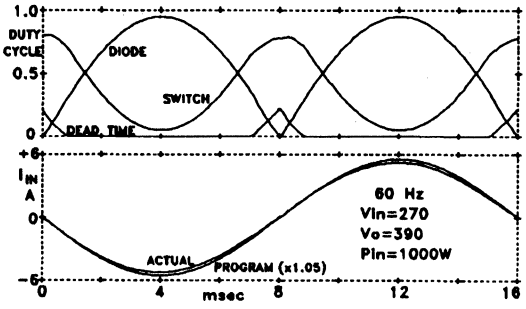

Fig. 9 - Boost 60Hz Sine Wave Input Current

Note that the switch duty cycle does not change as much when operation becomes discontinuous. With the boost (and flyback) topology in the discontinuous mode, average input current tends to follow input voltage at a constant duty cycle. Even though plenty of CA gain is available to change the duty cycle, little change is required for perfect tracking.

Figure 10 shows how the actual input current sine wave tracks the programming signal at 400 Hz. The distortion is worse -- 4.5% 3rd harmonic. This is for two reasons:

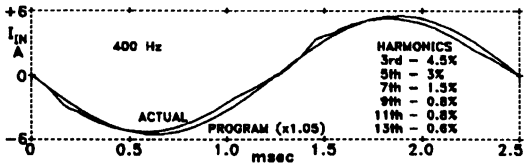

Fig. 10 - Boost 400Hz Sine Wave Input Current

1. The harmonic components of the rectified 400 Hz waveform are at higher frequencies and closer to the current loop crossover frequency where the loop gain is less, compared with the 50 or 60 Hz harmonics.
2. The inductor current has difficulty rising off zero because the input voltage is so very low at that point. So the inductor current lags coming off zero, then catches up and overshoots the programmed level. (This effect is much worse with peak current mode control because of the large inductor required.)

Controlling Average Switch Current

In the previous examples, average current mode control was applied to controlling inductor current (buck output current and boost input current). This is relatively easy because the inductor current is mostly DC with only a small amount of ripple to deal with. But if it is desired to use a buck or flyback topology to control input current in a high power factor application, then the chopped current waveform through the power switch must be averaged, a more difficult task.

Example 3: Flyback Regulator Input Current: A 1000 W off-line preregulator uses a flyback circuit in order to achieve a standard 300V output bus even though the input voltage ranges above and below 300V (Figs. 11,12).

The flyback converter could be designed to operate in the discontinuous inductor current mode in this application. The discontinuous flyback converter is not difficult to control (crudely) by fixing the duty cycle during each line half-cycle, but the peak currents through the power switch and rectifier are nearly twice as high as with continuous mode operation.

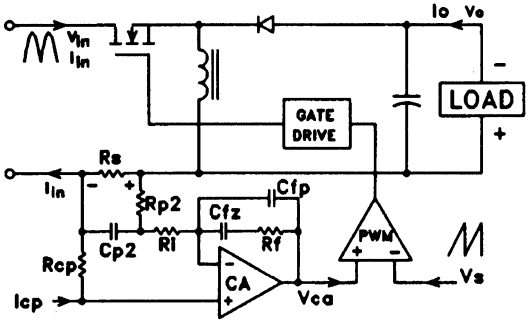

Fig. 11 - Flyback Preregulator Circuit

The high peak current lowers efficiency and requires devices with higher current ratings.

Continuous mode operation suffers the problem that the boundary is crossed into the discontinuous mode at light loads and high input voltage, unless a large filter inductor is used, which hurts the frequency response and the power factor as well as the pocketbook.

This dilemma disappears with average current mode control because it functions well in the discontinuous as well as the continuous mode, enabling the use of a small inductance value. In this example, the flyback converter operates in the continuous mode when it is important do so--at high current levels, to keep the maximum peak current to half that of a strictly discontinuous flyback converter. The operating parameters are:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
Output Volts, V_O = 300V dc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
ΔI_L @9OV = 3.6A
R_S = 0.025Ω

The max. overload rms line current at min. V_{IN} equates to 1080W input (2160Wpk 60Hz). The max. overload peak 60 Hz line current (17A) should be made to correspond to a limit on the current programming input, I_{CP}. Unlike the boost converter, the flyback input current is chopped, so the peak 100kHz current through

the switch, the inductor, and the rectifier are much greater than the 60 Hz peak current-see Fig. 12. The worst case, at low line and max. overload input current is:

$$I_{PK(100kHz)} = \frac{I_{PK(60Hz)}}{D} = \frac{17}{.702} = 24.2A$$

Add to this one-half ΔI_L to obtain the absolute max. peak current through the switch, inductor, and rectifier: 24.2 + 3.6/2 = 26A.

Compared to the boost converter, the flyback topology requires higher current and higher voltage devices and generates a lot more input noise because of the chopped waveform. In its favor, the flyback converter can operate with any input/output voltage ratio, can provide current limiting, and input/output isolation.

As discussed in the previous example, the boost converter amplifier gain at f_S was limited only by the criteria that the inductor current downslope must not exceed the oscillator ramp slope. The power circuit control-to-input current gain had a simple -1 slope from zero to f_S, making it very easy to compensate.

But with the flyback converter, the chopped switch current waveform will be averaged. This results in a lower crossover frequency, f_C, and lower gain-bandwidth for two reasons:

1. The large amplitude chopped current waveform must be integrated by the CA. The upslope of the resulting triangular waveform at the CA output must not exceed the oscillator ramp slope. (The inductor current downslope is not relevant.)
2. There is a zero (conventional left half-plane) in the control-to-input current gain characteristic. This zero moves with output current level. Loop gain crossover cannot be much higher than the lowest zero frequency.

The small-signal control-to-input gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS} , the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left[I_L + \frac{V_O}{sL}\right] \qquad (10)$$

This is the characteristic of a "normal" zero-a -1 slope with 90° phase lag below f_Z and flat gain with no phase shift above f_Z. The zero frequency may be calculated:

$$f_Z = \frac{V_O}{2\pi L I_L} \qquad (11)$$

Note that the zero moves inversely with inductor current and inductance value. This zero has a big effect on loop compensation. To obtain the best loop response, it is important that f_{Zmin} be as high as possible, by making the inductance small. Fortunately, with average current mode control, there is no need to worry about crossing into discontinuous operation. The limit on making the inductance too small is when the inductor ripple current becomes too large, increasing peak switch and rectifier currents an undesirable amount.

Using the specific values of this example, the power circuit gain is:

$$\frac{v_{RS}}{v_{CA}} = \frac{I_L}{200} - j\frac{960}{f}$$

The minimum zero frequency is 8 kHz, which occurs at 24.2A, the max. overload *inductor* current at 90V low line. The gain above f_Z is 0.12 (-18.4dB). The power circuit gain is shown in the Bode plot of Fig. 13.

Turning now to the current error amplifier (Fig. 11), the chopped input (switch) current waveform shown in Fig. 12 flows through R_S. The average value of this waveform, chopped at 100 kHz, is compared to the current program level across $R_{CP}$and amplified. Assume for the moment that C_{P2} is zero and C_{FZ} is shorted. The CA gain in the vicinity of 100 kHz is determined by integrator $(R_I+R_{P2})C_{FP}$. Averaging is accomplished because the DC gain is high, but the 100 kHz rectangular waveform with its harmonics is amplified relatively little. The rectangular waveform is converted into a triangular wave as shown in Fig. 12.

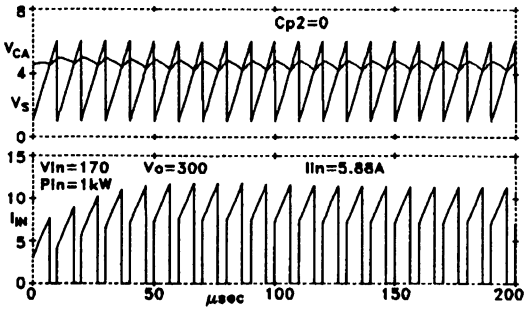

Fig. 12 - Flyback Regulator Waveforms

The optimum CA integtator gain at 100 kHz is the gain at which the maximum CA output upslope equals the oscillator ramp slope. This is the same principle used in the previous two examples, but in those cases the inductor (whose current was being controlled) did most of the averaging. The inductor did the integration to provide the triangular ripple current waveform and the CA gain was flat in the vicinity of f_S. But in this flyback preregulator example, the chopped *switch* current is being controlled so the averaging and the triangular waveshape are achieved by an integrating amplifier.

The upslope of the CA output occurs when the switch is off and the 100 kHz current waveform is at zero. The CA inputs are both at program voltage V_{CP} . V_{CPmax} equates to the max. overload peak 60Hz input current (17A) through R_S. Therefore, during the switch "off" time, the maximum current through $R = (R_I+R_{P2})$ is :

$$I_{RImax} = \frac{V_{CPmax}}{R} = \frac{I_{INpk} R_S}{R}$$

The upslope of the CA output is determined by the current through R_I charging C_{FP}:

$$\text{max } CA \text{ Upslope} = \frac{I_{RImax}}{C_{FP}} = \frac{I_{INpk} R_S}{C_{FP} R_I}$$

$$\text{Oscillator Ramp Slope} = V_s/T_s = V_s f_S$$

Equating the slopes and solving for C_{FP}:

$$\frac{I_{INpk} R_S}{C_{FP} R} = V_S f_S$$

$$C_{FP} = \frac{I_{INpk} R_S}{V_S f_S R} \qquad (12)$$

Using the values from this example, and assuming R = 10K (R_I=9K, R_{P2}=1K) :

$$C_{FP} = \frac{17 \times .025}{5 \times 0.1 \times 10^6 \times 10K} = 85\,pF$$

The CA integrator gain may now be calculated and entered in the Bode plot:

$$G_{CA} = \frac{1}{2\pi f R C_{FP}} = \frac{187{,}000}{f} \qquad (13)$$

The compensation circuit as designed so far (with C_{P2} zero and C_{FZ} open) has high loop gain and is very stable only when the inductor current is high, maintaining the power circuit zero near the position shown in Fig. 13, so that its gain is flat at f_C. At lower current levels, the power circuit zero slides down to the right and

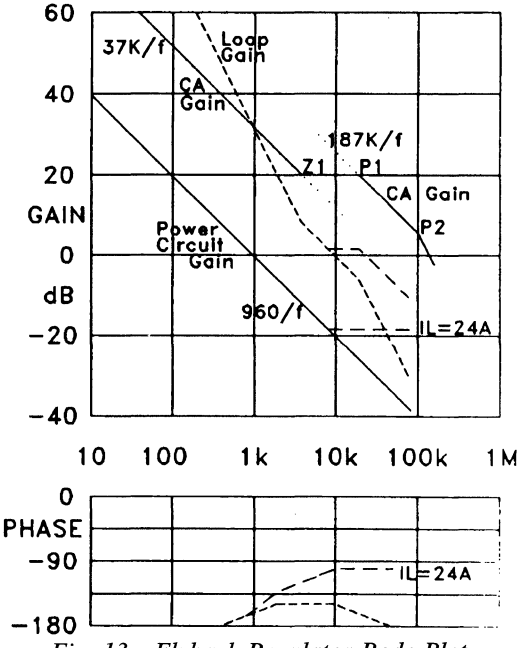

Fig. 13 - Flyback Regulator Bode Plot

the power circuit gain at f_c has a -1 slope. With the -1 slope of the CA gain, the overall current loop gain has a slope of -2 at crossover, and will ring excessively. It is necessary to add a pole-zero pair to the CA gain to reduce the slope to -1 in the vicinity of f_C. Offsetting the integrator gain by a factor of 5, as shown in the Bode plot, provides a phase bump which increases the actual phase margin to 42°, a slightly underdamped condition (the Bode *approximation* is 31°, as shown).

The offset factor of 5 is provided by $C_{FZ} = 4 \cdot C_{FP}$ = 340pF. C_{FZ} and C_{FP} in parallel set the integrator gain at low frequencies to 37,000/f.

The location of the flat portion of the CA gain characteristic is determined by R_F. It is easiest to solve this graphically using the Bode plot. Ideally, Z1 and P1 should bracket the crossover frequency. *Simply slide the flat portion up and down between the integrator slopes until its gain is equal (but opposite in sign) to the power circuit gain at the same frequency as the center of the flat potion.* That frequency is the crossover frequency, f_C. In Fig 13, the CA gain in the flat portion is 10 (20dB). This is accomplished by:

$$R_F = 10R = 10(R_1 + R_{P2}) = 100K \quad (14)$$

The precise value of R_F (and f_C) is not at all critical. The phase bump is broad, and the loop response is really determined by the integrator gain below f_C (37,000/f).

Finally, an additional pole $R_{P2}C_{P2}$ is placed at 100kHz to filter out noise spikes. This pole frequency is too high to significantly affect phase margin at crossover.

Referring back to Fig. 11 — when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. Programmed with a current source I_{CP}, the current gain of the closed current loop is identical to Eq. 9:

$$G = \frac{\hat{i}_L}{\hat{i}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (15)$$

Just as in the previous examples, the closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S. The moving zero of the flyback power circuit is hidden within the inner current loop, and is invisible to the outer voltage control loop. In fact-regardless of the power circuit topology-with average current mode control, the external characteristics of the current loops are identical: flat gain, rolling off with a single pole characteristic above the open loop crossover frequency.

Example 4: Buck Regulator Input Current: The buck regulator is sometimes used in high power factor preregulator applications. It can only function when V_O is less than V_{IN}, so the output bus voltage must be low. Normally, a low output voltage should be avoided, because the bus filter capacitor becomes large and expensive, but in applications such as telephone or battery charging this is not a problem and/or there is no choice. With 120V line input and 48 volt output bus, the input current will drop to zero for a substantial portion of each line cycle, each time the instantaneous line voltage goes below 48V. Third harmonic distortion will be 7 - 8% at low line, but the power factor of 0.99 is good enough for most applications.

Although the flyback topology might be used in the same low voltage output application, the buck topology operates with lower inductor current and lower peak current through the switch and rectifier. Peak voltages on the switch and rectifier are also much lower. But the flyback topology can provide line isolation in the preregulator by using a flyback transformer instead of simple inductor.

The buck circuit can be almost the same as the flyback circuit of Fig. 11, interchanging the inductor and the rectifier (cathode up).

The control loop design procedure is the same as for the flyback in Example 3. The buck regulator has the same left half-plane zero. In fact, the power circuit control-to-input gain equation is identical to Eq. 10 for the flyback circuit.

Controlling Average Rectifier Current

Peak current mode control has been used with great success in conventional power supplies using buck-derived topologies. It works well because peak current mode control actually controls inductor current, and the inductor is located in the output of all buck topologies. When boost or flyback topologies are used, peak current mode control functions poorly, because the wrong current is controlled-the inductor current is not in the output. Although peak current mode control eliminates the inductor from the small-signal characteristic of the outer loop, the right half-plane zero present in boost and flyback outputs remains to plague outer loop compensation.

In boost or flyback circuits, the diode is in the output side, and ideally the diode current should be controlled, not inductor current. This is no problem for average current mode control. Its integrating current error amplifier can average the rectangular diode current waveform in the same way that it averages the switch current in the input of the buck or flyback preregulators discussed earlier. The right half-plane zero forces a lower current loop crossover frequency, but the RHP zero is "buried" within the current loop. The outer voltage control loop sees only a flat gain characteristic with a single pole roll-off at the crossover frequency-just the same as all the other topologies previously discussed. A flyback circuit using average current mode control is shown in Figure 14.

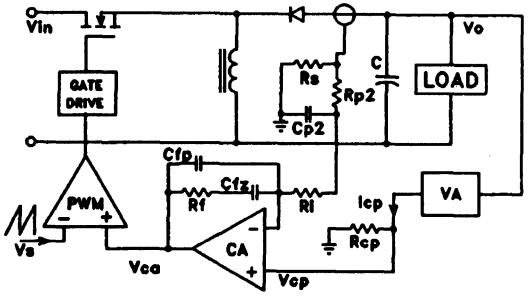

Fig. 14 - Flyback Output Current Control

The circuit is almost identical to the flyback preregulator of Fig. 11, except output current is sensed and controlled.

The small-signal control-to-output gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left(\frac{V_O}{sL} - I_L\right) \qquad (16)$$

The same equation applies to controlling the output current of a boost circuit. Note the similarity with Eq. 10 for flyback or buck input current control. In Eq. 16, low frequency gain depends on V_{IN} rather than V_O, but more importantly, the inductor current I_L has a minus sign, which represents 180° phase lag above the zero frequency. This is the characteristic of a right half-plane zero, and it makes the loop compensation much more difficult. It is usually necessary to cross over at a frequency one half to one fourth of the RHP zero frequency in order to cross over with adequate phase margin. This results in lower closed loop bandwidth for the current loop than the previous examples. However, once this is accomplished, the RHP zero does not appear in the outer loop.

It is very important to make the inductance small to achieve the highest possible RHP zero frequency. Fortunately, average current mode control allows the mode boundary to be crossed. This permits a much smaller inductance than with peak current mode control, resulting in a much higher RHP zero frequency and higher crossover frequency.

Current Sensing

One important advantage of having a high gain current error amplifier is that it permits a very small current sense resistor value resulting in low power dissipation. The CA can make up for the gain lost with the small resistor.

In many applications, however, using a current sense resistor in the direct path of the current to be measured is not practical. The tiny R_S value may be difficult to implement, and the power dissipation in a practical sense

resistor is too great. Often, the R_S circuit location is at a large potential difference from the control circuit. This is especially a concern when current must be sensed on the other side of the isolation boundary.

A current sense transformer (C.T.) can provide the necessary dielectric isolation and eliminate the need for an extreme low-value resistor. As shown in Fig. 15, this technique

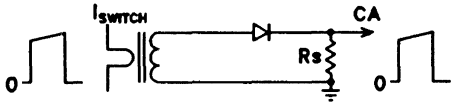

Fig. 15

works well for average current mode control when the current to be sensed and averaged is a pulse which returns to zero within each switching period-such as switch current (buck or flyback input current) or diode current (boost or flyback output current). Although "transformers can't couple DC", a C.T. does couple the entire instantaneous current waveform including its DC component if the core is reset to zero baseline each time the pulse goes to zero.

Total reset requires the same volt-seconds (of opposite sign) that were applied to "set" the core. At duty cycles approaching 1.0-which can occur temporarily with most topologies-the time available for reset may be only a tiny fraction of the switching period. Achieving total reset in a short time requires a large backswing of voltage across the C.T., so don't use low voltage diodes to couple the C.T. to R_S.

With a boost converter controlling input current in a high power factor preregulator application, a current sense resistor easily ties in directly with the control circuit, as shown in Fig. 6. Nevertheless, many designers would prefer to use a current transformer to minimize power loss and allow the use of a much higher R_S value. However, since the input current of a boost converter *is* the inductor current, the input current never goes to zero when operating in the continuous mode. Therefore, a C.T.. can't be used to sense input current of a boost converter because the DC value is lost, and the C.T. cannot reset-it will saturate. The same problem occurs in a buck regulator circuit, where the C.T. can't directly sense average output (inductor) current.

The answer to this problem is to use *two* C.T.s–one sensing switch current, the other sensing diode current. By summing their outputs as shown in Fig. 16, the true inductor current is reconstituted. Each C.T. has plenty of time to reset.

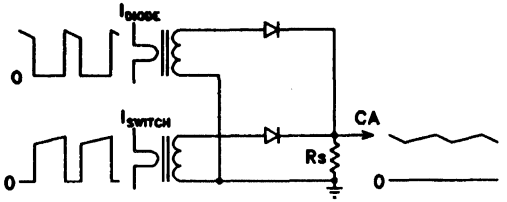

Fig. 16

Using Current Sense Transformers:
It is not difficult to achieve excellent results using low cost commercially available pulse transformers. A current sense "inductor" such as Pulse Engineering 51688 is a toroidal core wound with 200 secondary turns for a secondary inductance of 80 mH. A 0.18" hole is provided to slip the primary wire through.

The pulse voltage across the windings of a current transformer generates a magnetizing current which starts at zero and increases fairly linearly with time. The magnetizing current subtracts from the pulse current delivered to the secondary. Initially, the current through R_S is precisely I_{PRI}/N, but as time passes, the secondary current drops off more rapidly than it should, This effect is called "droop". It is usually not a problem if certain precautions are observed. The amount of current droop through the current sense resistor can be calculated:

$$\Delta I_{PRI(droop)} = \frac{N_S}{N_P}\frac{V_S}{L_S}\Delta t \qquad (17)$$

where N is the turns ratio, V_S the voltage across the secondary, L_S the secondary inductance and Δt is the max. pulse width. As the

equation shows, droop is minimized by maximizing secondary inductance-use the largest you can get. Don't use a large R_S value to obtain a large secondary voltage-its not necessary and makes reset more difficult. Make the turns ratio as low as possible by using two or three primary turns if space allows. Don't reduce the turns ratio by reducing the secondary turns-this is counter-productive because the inductance goes down with the turns *squared.*

For example, consider the flyback input current preregulator of Fig. 11, using a current transformer in series with switch instead of the 0.025Ω sense resistor shown. Using the Pulse Engineering #51688 current sense inductor with one turn primary, the turns ratio is 1:200. Secondary inductance is 80 mH. The 24A max. overload pulse current becomes a 0.12A current pulse on the secondary side. A 10Ω sense resistor will have a max. voltage of 1.3V sent to the CA, and the max. secondary voltage including diode forward drop is 2.0V. The maximum pulse width is 7.02μsec.

Applying these values to Eq. 17:

$$\Delta I_{PRI(droop)} = \frac{200}{1}\,\frac{2.0}{80\times10^{-3}}\,7\times10^{-6} = .035A$$

Only 35mA droop out of 24A isn't bad!

When two C.T.s are used-one on either side of isolation boundary-their turns ratios must be proportioned the same as the power transformer pri/sec turns ratio so that currents through R_S will be equalized.

All of the equations containing R_S given earlier in this paper assume the sense resistor is measuring current directly. When using a current sense transformer, reflect the actual R_S on the C.T. secondary side into the primary by substituting $R_S N_P/N_S$.

References:

[1] S. Hsu, A. Brown, L. Rensink, R.D. Middlebrook, "Modelling and Analysis of Switching DC-to-DC Converters in Constant Frequency Current Programmed Mode, *"IEEE PESC Proceedings,* 1979

[2] R.D. Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming" *IEEE PESC Proceedings,* June 1985

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UCC3806 BiCMOS CURRENT MODE CONTROL IC

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Abstract

Space and cost constraints have forced power supply designs into smaller spaces and demanded more efficient designs with higher switching frequencies. With the introduction of the UCC3806 BiCMOS current mode controller, a designer has the advantages of reduced current consumption, power loss and propagation delays within the IC. The UCC3806 is pin-for-pin compatible with the popular UC3846 and UC3856 controllers. With minimal part changes, this device may be suitable for retrofit into many existing designs where higher power consumption and propagation delays posed problems in the past. An ideal application for the UCC3806 is in battery operated equipment where low power consumption is critical to extended operation.

INTRODUCTION

As power supply requirements are demanding higher switching frequencies and lower power consumption, bipolar PWM IC's may limit design flexibility. The versatile UC3846 consumes relatively low power but is slow by today's standards. The UC3856 fulfills the high speed requirements but uses significantly more power to accomplish the task. Unitrode's BiCMOS process produces fast, low power BiCMOS control ICs with the high power capabilities of bipolar devices, a prime example being the UCC3806.

The UCC3806 features slew rate limiting of the current sense amplifier input voltage. This allows direct injection of the primary current sense signal without the need to filter the inductive leading edge spike. The propagation delay from current sense to output is reduced to 125ns and rise and fall times of the gate drive outputs are only 65ns. Gate drive current remains high at ±500mA from the dual totem pole MOSFET drivers. The low undervoltage lockout thresholds make this IC ideal for many battery and automotive applications. Most features will be familiar to the designer acquainted with the UC3846. The one volt pulse by pulse current limiting remains, along with programmable latched or non-latched shutdown modes triggered via the Shutdown pin.

This Application Note highlights retrofit applications of the UCC3806 and provides a step by step process to accomplish this. Several new applications will be introduced with a review of some popular applications. Unitrode Application Note U-93 describing the UC3846 should be reviewed for background and additional information.

UCC3806 BiCMOS Current Mode PWM Control IC Features

- 100µA startup current
- 1.4mA operating current
- Pin-for-pin compatible with UC3846 and UC3856
- Operating frequency to 1MHz
- ±500mA MOSFET output stage
- 65ns output rise and fall times
- 125ns current amp to output delay
- Current Sense Slew Rate Limiting
- Undervoltage Lockout

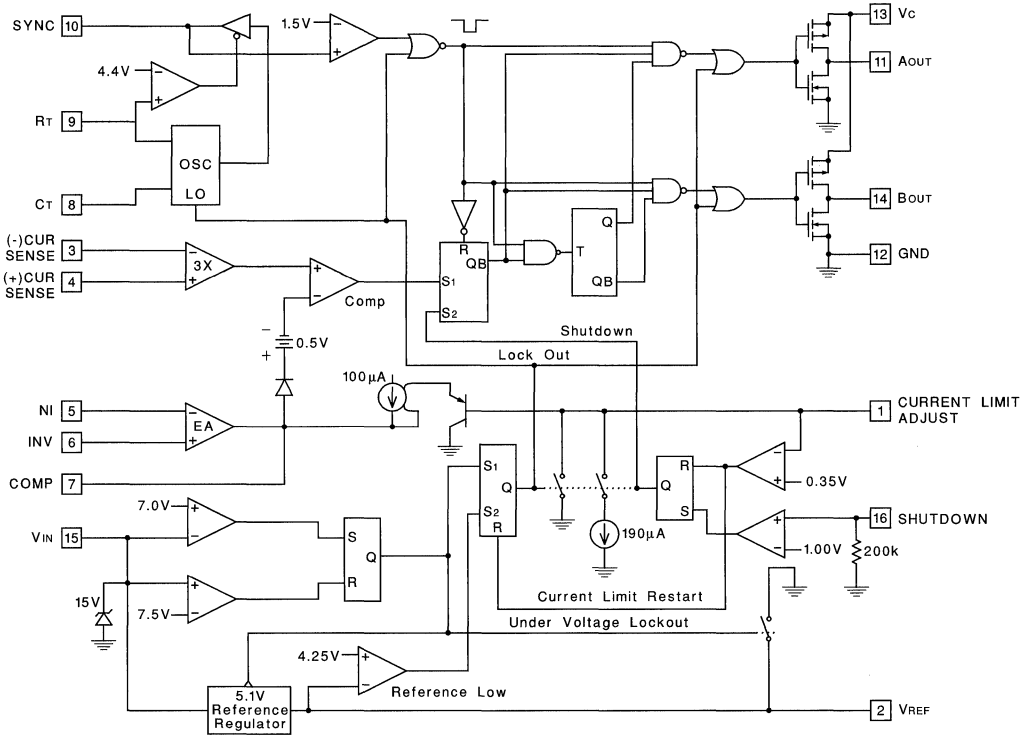
DEVICE DIFFERENCES

For designers familiar with the UC3846 or UC3856 devices, this section will provide a quick overview of necessary design changes to incorporate the UCC3806.

1) **UVLO**: Three parameters should be observed here. The start up voltage threshold is 8.0V with an operating hysteresis of 0.75V. The absolute maximum voltage for V_{IN} (pin 15, IC power) is 15V and for V_C (pin 13, gate drive voltage), 18V.

2) **DEAD TIME** (t_d) is determined by the timing capacitor (C_T).

$t_d = 961C_T$ (approximately)



UCC1806 Block Diagram

3) **SWITCHING FREQUENCY** (fs) may be found by using the equation

$$f_S = \frac{1}{2R_TC_T + t_d}$$

4) **SHUTDOWN** threshold voltage on pin 16 has been raised to 1.0V.

5) **GATE DRIVES**: The maximum gate drive current is ±500mA.

6) **CURRENT LIMIT**: As in the UC3846 and UC3856, R1 and R2 (see Figure 5) program the threshold for primary current limit and determine whether the IC will latch off or retry. When a shutdown signal is generated, a 190µA current source to ground pulls down on pin 1. If the voltage on the current limit adjust pin (pin 1) remains above 350mV the IC will remain latched and power must be cycled to restart. If the voltage on the current limit adjust pin falls below 350mV, then the IC will attempt a re-start.

DESCRIPTION

SUPPLYING POWER

Power can be applied to the UCC3806 by a single source or by two separate sources, one for the IC supply and another for the FET drive outputs. In either case, adequate local capacitive bypassing is required. The IC supply voltage is internally limited by a 15 volt shunt regulator circuit. This is advantageous in off-line applications where the IC is powered-up by a resistor to the high voltage input. Shunted supply current in the IC must be limited to 10mA maximum. The IC's ground should be separated from any high current or noisy ground paths, but at the same electrical potential. This is best done by routing a local ground for the UCC3806 circuitry and then connecting this to a single point system ground.

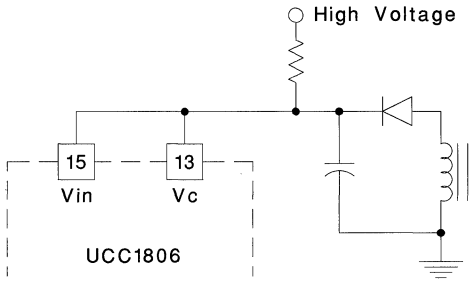


Figure 1. Supplying Power

UNDER VOLTAGE LOCKOUT (UVLO)

A minimum of 8V is needed to start the UCC3806, and once operational, the IC operates down to 7.25V. Below this level the UCC3806 will turn off and again require at least 8V to re-start. Care must be taken to be sure that the voltage source can supply adequate current to maintain operation or the IC will cross its turn-off undervoltage lockout threshold and shut down. The most obvious symptom where this problem occurs is when the entire power supply pulses on and off. Depending on the storage capacitor size and bias supply circuitry, the supply may eventually continue to run or may simply hiccup. A good design will include a large capacitor across the IC power inputs to store energy long enough to avoid UVLO. Note that the gate drive requirements of most power MOSFETs will usually use more current than the IC draws by itself, and must not be overlooked. Please refer to application note U-93 and U-137 for more details.

SELF-BIASING, ACTIVE LOW OUTPUTS DURING UNDER VOLTAGE LOCKOUT.

During any undervoltage lockout the UCC3806 outputs are actively held low to eliminate problems caused by a power MOSFET switch device inadvertently turning on. As with other Unitrode PWM IC's, gate drive outputs cannot pull high until the IC has been properly turned on. This self-biasing circuitry derives its power from the MOSFET gate voltage which is attempting to rise. Note that this protection feature is also activated when the supply voltage falls below the UVLO point, causing the IC to turn off.

REFERENCE VOLTAGE

The UCC3806 provides a 5.1V ± 1% reference output. Bypass capacitors with low impedance (ESL and ESR) and good high frequency response should be used. Generally, a ceramic monolithic or MLC capacitor with short leads to the IC ground pin is required even if the reference is not externally used. Note that the maximum current available from the reference pin is 10mA. Erratic operation can be caused by exceeding the maximum current or from connecting very noisy loads to the V_{REF} pin without adequate bypassing and filtering.

OSCILLATOR

The oscillator timing section of the UCC3806 is similar to it's predecessors yet uses different voltage thresholds throughout. Frequency is programmed by selecting the values of two timing components; C_T, the timing capacitor and R_T, the timing resistor. Current flowing from the internal 1.25V reference at the R_T pin divided by the value of R_T is mirrored to the timing capacitor pin (C_T). This causes a linear charging of C_T from 0V to 2.5V, the lower and upper oscillator thresholds. Note that the current mirror is limited to a maximum of 100µA so R_T must be greater than 12.5k.

Oscillator discharge is facilitated by switching on a 2.6mA current sink from C_T to ground. This causes a linear discharge of C_T to zero and then initiates the next switching cycle. Dead time occurs during the discharge time of the capacitor during which time both outputs are active low. Subjecting other IC pins to excessive noise or pulling some points below ground may reset the oscillator or cause periodic termination. f_s and t_d may be approximated by:

$$f_s = \frac{1}{2R_TC_T + t_d} \qquad t_d = 961\ C_T$$

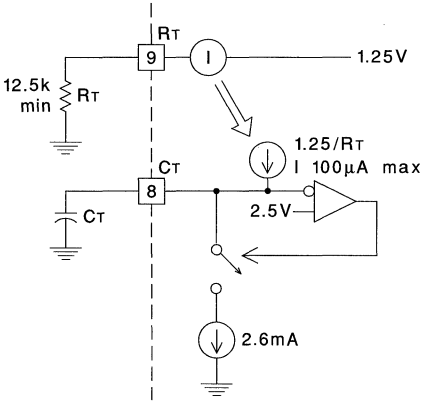


Figure 2. Frequency and Deadtime Programming

SYNCHRONIZATION

The SYNC pin allows external synchronization of the UCC3806 to an outside control signal with TTL compatible thresholds. The oscillator C_T pin must be grounded in order to use the SYNC input feature. The internal clock is reset and a deadtime generated by applying a voltage greater than 2V (high) to the SYNC pin. Returning this input to a voltage less than 0.8V toggles the output flip-flop and initiates a new switching cycle.

External synchronization may be sourced from the SYNC pin. The oscillator output goes to the SYNC pin and affects the outputs as described above. Another UCC3806 may be connected to the SYNC pin in order to match the frequency of the master device. Other circuits or devices may use the characteristics of the SYNC pin. A high output state is at least 2.4V with 5mA current sourced and low output state 0.4V maximum with a 1mA sink.

OUTPUT DRIVER SECTION

The two UCC3806 alternating outputs consist of totem-pole MOSFET pairs. Duty cycle may be varied from 0 to 98% where minimum dead time is determined by the timing capacitor value. Both outputs use MOS transistor switches with inherent anti parallel body diodes to clamp voltage swings to the supply rails. This may allow operation without the use of clamp Schottky diodes on each gate drive as recommended with all bipolar ICs. Drive currents of ±500mA peak with rise and fall times of 65ns are typical performance specifications.

CURRENT AMPLIFIER SECTION

Slew rate limiting on the current sense amplifier output is featured in the UCC3806 device. This allows direct connection to the current sense resistor or current transformer with minimal filtering. Parasitic leading edge inductive spikes can cause false triggering in most PWM IC's and thus require significant filtering.

As with other current mode PWM's, the UCC3806 can be configured for a variety of control techniques. The more common examples are peak current mode control, direct duty cycle control (voltage mode), and gaining popularity is average current mode control. Slope compensation can be added by dividing down the oscillator sawtooth waveform and summing a portion of it to the peak switch current signal.

High efficiency current sensing can be obtained by developing a small amplitude current sense signal, well below the 1 volt maximum of the IC. A DC pedestal can be added to raise the current signal, gaining noise immunity. One easy method of achieving this is to add resistors from output A and output B to the positive current sense input in a system where the negative current sense pin is grounded. Note that this pedestal will vary with changes in the IC collector supply voltage, VC. Another method to add a DC level to the current sense input or the current limit input is to use a resistive divider from VREF.

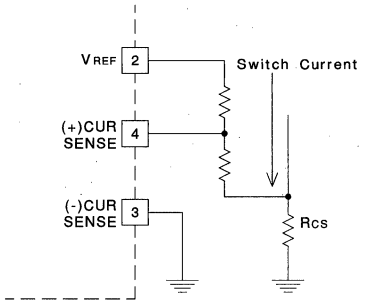


Figure 3A. Level Shifted Current Sense

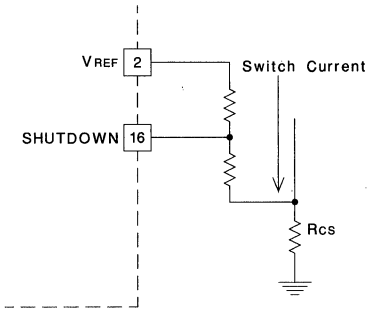


Figure 3B. Level Shifted Shutdown

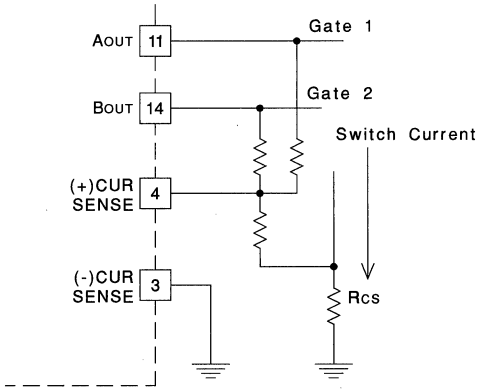


Figure 3C. Adding a Pedestal from Gate Drives

PROTECTION CIRCUITRY

By adjusting the pulse-by-pulse current limiting, a converter can be protected against short circuit conditions. The UCC3806 terminates the PWM output protecting the switching device and other power components when sensed switch current reaches the 1 volt current limit threshold. The ratio of this signal to actual switch current is determined by the current sense resistor value. Additionally, the

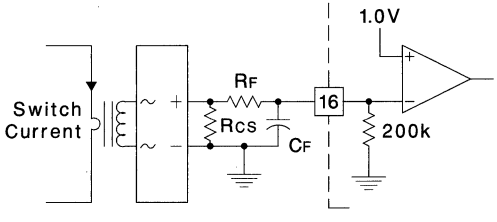


Figure 4. Overcurrent Shutdown

SHUTDOWN feature can be incorporated for further protection as shown in Figure 4.

The pulse-by-pulse current sense amplifier allows differential voltage sensing for ungrounded sense resistors. The current amplifier will terminate the ON-time when it's differential voltage reaches that set at the current limit input. Pulse by pulse current limiting is programmed by two resistors at the current limit. These resistors also set the shutdown mode to either latching or non-latching shutdown. To choose Values of R1 and R2:

$$V_{CS} = (V_{pin1} - 0.5)/3$$

$$I_{CL} = \left(\left(\frac{R_2 \bullet V_{REF}}{R_1 + R_2}\right) - 0.5\right) / 3R_S$$

During Shutdown:

$$V_{pin1} = \frac{V_{REF} - 190(10^{-6})R_1}{1 + \frac{R_1}{R_2}}$$

Latch Mode: $V_{pin1} > 350mV$

Non-Latch Mode: $V_{pin1} < 350mV$

A SHUTDOWN pin is provided for enhanced protection. Pin 16 can be programmed to force a shutdown when it's voltage exceeds 1V, and latching or non-latching modes are programmable options. When a shutdown is triggered, a 190µA current sink is connected to the current limit pin. If the voltage on pin 1 remains above 350mV, then the IC remains latched and outputs are held actively low. If the voltage is allowed to fall below 350mV, then the IC will reset and initiate a re-start. Of course, a wider margin is recommended to guarantee that resistor tolerances and external noise do not affect this mode selection. Again, a bypass capacitor from pin 1 to ground can also help eliminate problems from external noise.

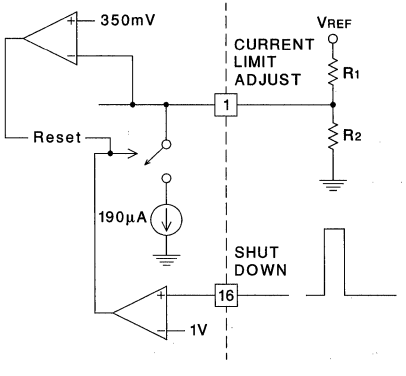


Figure 5. Shutdown Mode Programming

SOFT START

Several methods of soft starting of a converter are possible with the UCC3806, and two common examples are shown. In the first example, an R/C network isolated by a PNP transistor sinks current from the output of the error amplifier. In the second, an R/C network alone is used on the error amplifier non-inverting (E/A+) input. This ramps up the non-inverting input of the op-amp to reduce the slew of output voltages and delivers true closed loop controlled start-up. In both cases, the diode provides automatic capacitor discharge when the VREF turns off, typical of a power-up or shutdown condition.

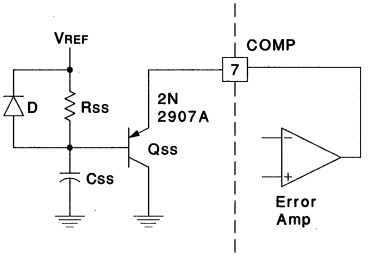


Figure 6. Buffered Soft Start

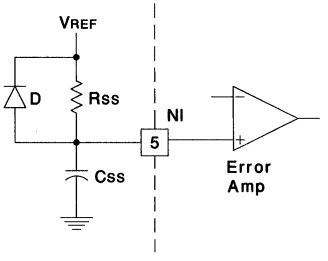


Figure 7. Closed Loop Soft Start

APPLICATIONS

Push-Pull Converter

One of the most common uses for the UCC3806 is in an isolated Push-Pull configuration utilizing current mode control. A summation of the components and their functions follows.

Resistors Rg1 and Rg2 limit the output current to 0.5A. Rv limits current to the IC to 10mA. RT and CT set frequency and dead time. Note that oscillator waveforms may become non-linear at higher frequencies and so RT and CT should be selected to obtain the desired frequency. Rss and Css are used to ramp up the reference on the error amp so the output voltage comes up in an orderly manner. R1 and R2 program the pulse by pulse current limit for primary peak current. R3 and R4 set a shutdown triggered by excessive primary current. These levels should be set to assure that a shut-

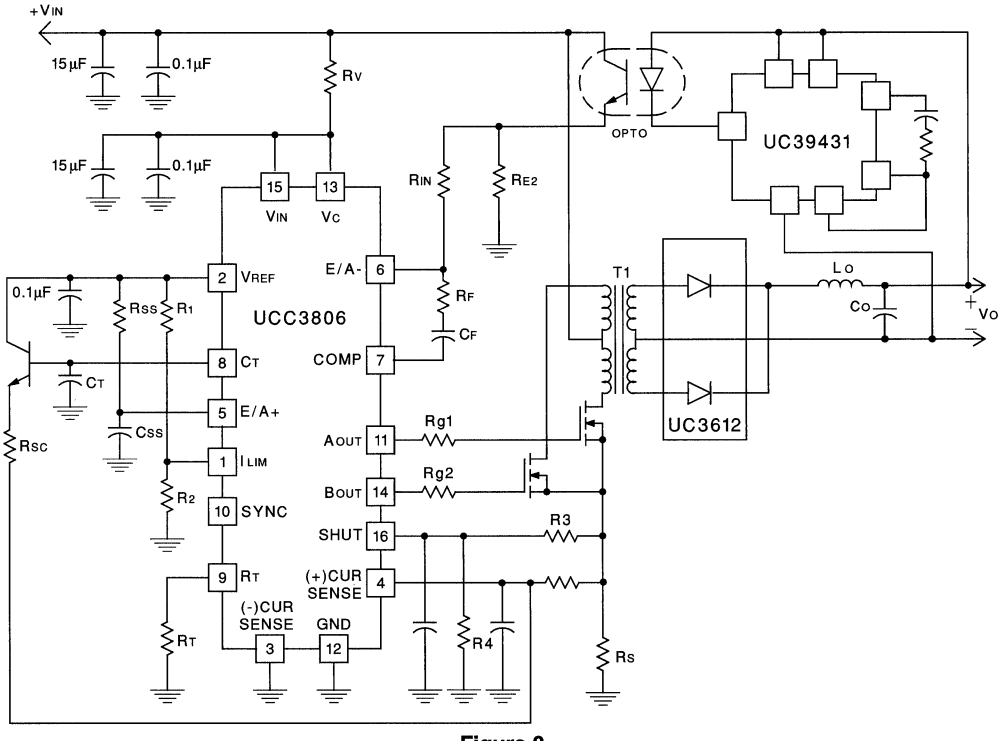


Figure 8

down will be triggered before the pulse by pulse current limit threshold is reached. R1 and R2 determine latched or non-latched shutdown once shutdown is tripped. Slope compensation is shown and may be necessary in order to avoid sub-harmonic oscillations when duty cycles greater than 50% occur. Note that bypass capacitors are used in several locations to filter noise around the UCC3806 circuitry. The value of these capacitors will vary depending on input and output variables, layout, and power level.

Non-Isolated Autotransformer Converter

When isolation is not needed but a voltage step up desired, a simple push-pull configuration may be used with a non-isolated transformer to step up the input to output voltage. Figure 9 shows how a UCC3806 may be used to achieve a very efficient converter ideal for battery applications. Because of the voltage step up, output regulation is maintained even when input voltage falls below output voltage. Notice that the UCC3806 is otherwise used in a very conventional application here. Circuit set up follows the same simple rules as a conventional transformer isolated converter. Efficiencies over 90% can be realized for low power converters similar to this example.

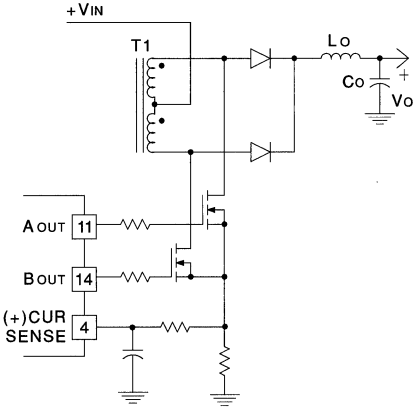


Figure 9. Autotransformer Converter

Self Contained Low Power Converter

A non-isolated converter of Figure 10 demonstrates the versatility of the UCC3806 FET output stage. In this application, the lower drive FET of each output totem pole is used as a synchronous rectifier along with the parasitic body diode, and no external diodes or switches are used. Interleaved inductors are incorporated and operated in the continuous current mode. Inductor current must not

become discontinuous, or current will reverse direction and circulate into the IC. When this occurs, the other inductor circulates current into the lower output FET creating excessive heating and forcing the IC to overcome backwards current when turning on again.

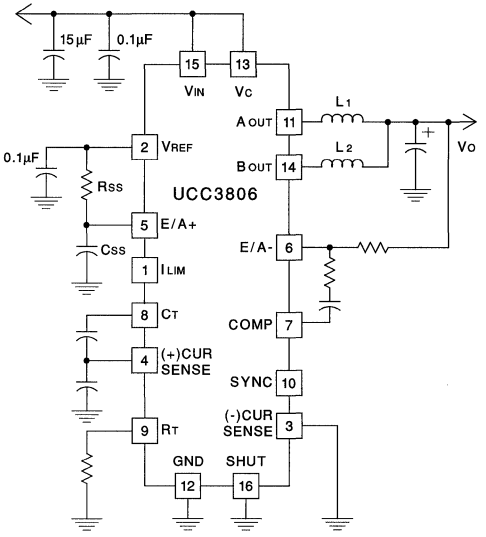


Figure 10

Summary

BiCMOS technology in the UCC3806 has added a new dimension to PWM IC's available today. This IC enables the designer to optimize circuits by allowing higher switch frequencies and decreasing IC delays. This breakthrough in technology brings a dramatic reduction in IC operating current and the ability to use larger resistor values in support circuitry which further cuts power loss. Less parts can be used by eliminating Schottky diodes which protect Bipolar IC's as well as the possible elimination of current sense filtering. The UCC3806 remains pin for pin compatible with the familiar UC3846 and possesses all of the desirable functions found in that popular PWM control IC. These features include a 500mA output drive capability, current mode control, fully differential current sense amplifier, pulse by pulse current limiting under voltage lock out and built in shutdown circuitry.

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ELEGANTLY SIMPLE OFF-LINE BIAS SUPPLY FOR VERY LOW POWER APPLICATIONS

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INTRODUCTION

Generating a low power, low voltage bias supply in an off-line application may not seem like a major design challenge – at first glance. However, obtaining an efficient, cost effective and compact 1 Watt supply can be a frustrating ordeal as the various approaches are evaluated. A simple transformerless technique, like the Buck regulator, requires a rather complex high side switch which can be difficult to drive. Narrow duty cycles are another inescapable problem with a significant step down in input to output voltage.

The Flyback converter can provide a relatively simple solution for this low power application, but it requires more costly coupled windings instead of a single inductor to perform the voltage conversion. Other topologies too, have their own unique sets of problems. For example, the SEPIC Converter is a viable option, but needs a high voltage blocking capacitor and two inductors, in addition to the high voltage switch. It will also require current mode control for stability as opposed to simpler control techniques. Charge pump circuits are another possibility, but are generally much noisier, deliver poor efficiency and often use a high side switch. This Application Note will present a novel conversion technique to achieve the desired low voltage, low power bias supply while meeting the design goal of low cost with minimal complexity.

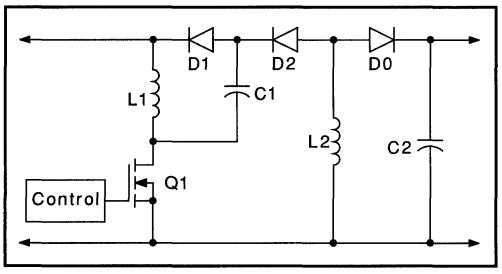

Figure 1. Cascaded Flybacks

Approach : The basic converter shown in Figure 1 is a cascaded Flyback Converter operated in the discontinuous current mode. Two flyback stages are placed in a series configuration to complete the voltage transformation. Inductor L1 of the first stage is switched across the input voltage when MOSFET (Q1) turns on. Energy is stored in L1 as its current rises linearly until the switch is turned off. When this occurs, inductor L1 discharges its energy into capacitor C1, and diode D1 is conducting. In steady state operation the switching action develops a net DC voltage across C1, the "output" capacitor of the first Flyback converter, C1.

The inductor of the second stage (L2) is also switched across capacitor C1 while the MOSFET is on. Although the voltage across inductor L2 is negative with respect to ground, energy is stored in L2 as the current linearly rises. When the switch is turned off, inductor L2 discharges to the output capacitor of this second Flyback stage, C2. A regulated DC output voltage is obtained across C2 and controlled by varying the ON-time of switch Q1. Voltage and current waveforms for this converter are shown in Figure 2 for completeness.

This cascaded Flyback converter can be controlled by a number of popular techniques which include Duty Cycle (Voltage Mode) Control or Current Mode Control, and can be operated in either fixed or variable frequency modes. A novel control technique will be introduced to greatly simplify the circuit complexity, and is implemented in the UCC3889 Bias Control IC with complete details to follow.

CONVERTER DESIGN EQUATIONS

Circuit components are primarily determined by several key factors; switching frequency, output power, efficiency and duty cycle. First, the voltage conversion relationship for the Flyback topology is reviewed.

Duty Cycle :

Duty cycle (d) = $\frac{t_{ON}}{t_{PERIOD}}$

where $t_{PERIOD} = t_{ON} + t_{OFF}$, or $\frac{1}{f_{SWITCHING}}$

For the Flyback topology, the duty cycle can be approximated by the following relationship:

$$V_{OUT} = V_{IN} \bullet \frac{d}{1-d}$$

The cascaded Flyback conversion technique utilizes the output of the first Flyback converter as the input to the second stage. The voltage transformation of the two Flyback converters in series can be approximated by :

$$V_{OUT} = V_{IN}\left(\frac{d}{1-d}\right)^2$$

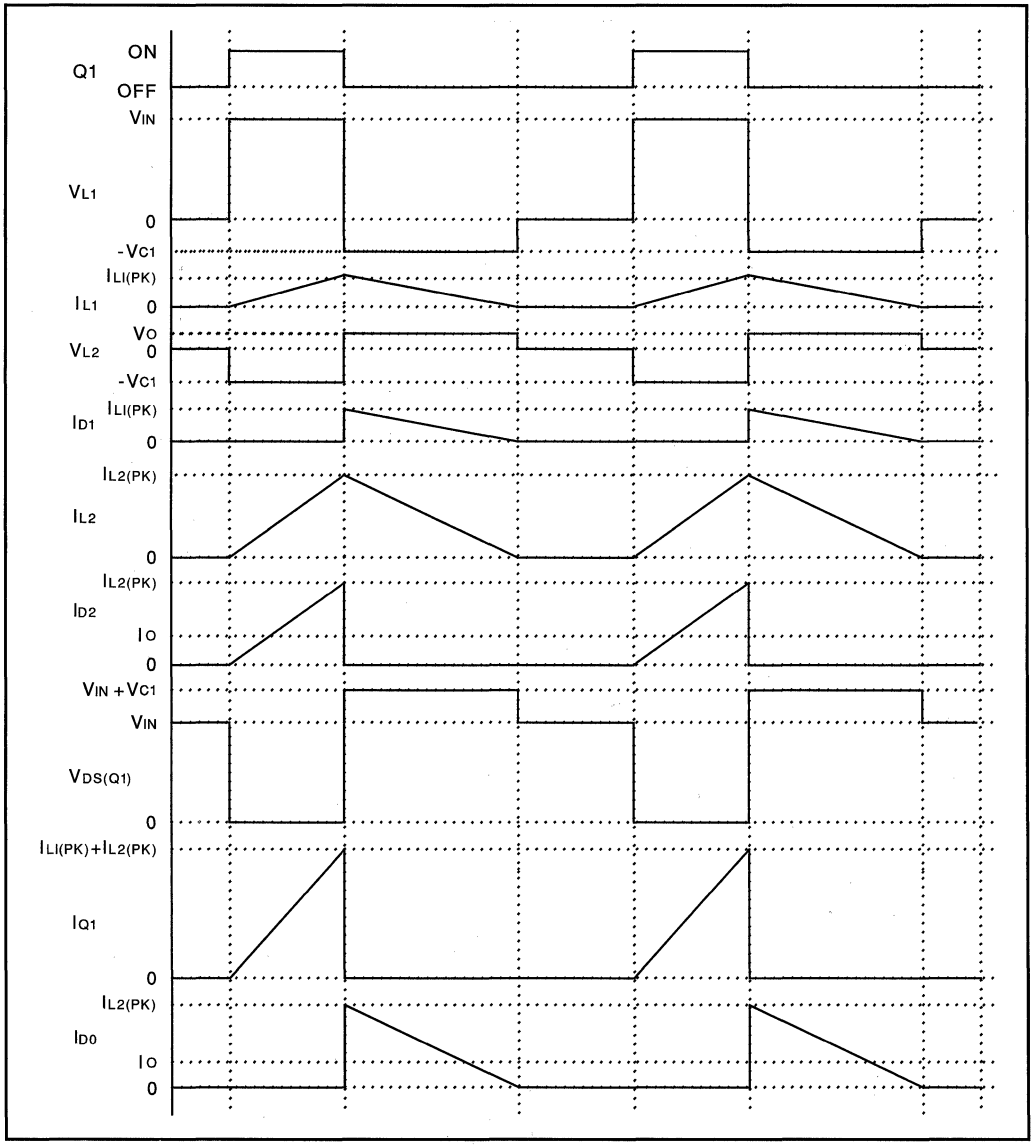

Figure 2. Converter Waveforms

This equation can be rearranged to solve for the duty cycle with respect to VIN and **VOUT** as:

$$\text{duty cycle} = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

Input Power :

$$P_{IN} = \frac{P_{IN}}{n}\ ;\ \text{where}\ \ n = \text{efficiency}$$

Input Current :

$$I_{IN} = \frac{P_{IN}}{V_{IN}}\ ;\ \text{or}\ I_{IN} = \frac{P_{OUT}}{(V_{IN} \bullet n)}$$

Peak Inductor Current :

The peak inductor current changes with line and load conditions according to the following relationship :

$$I_{LPK} = \frac{2 \bullet I_{IN}}{d}$$

Inductor Value :

The inductor values are obtained from the equation :

$$L = \frac{V \bullet \Delta t}{\Delta I}$$

Any set of operating conditions can be used to solve this, and other equations. It is often easiest to standardize on using low line, full load conditions when the inductor (L1) is charging during the switch ON-time.

$$L = V_{INmin} \bullet \frac{t_{ON}}{I_{LPK}}$$

The second Flyback inductor value (L2) is obtained using this equation but by substituting the output voltage of the first converter (**VOUT**1) for VIN.

OTHER COMPONENTS

Capacitors are selected to adequately provide a filtered DC voltage with little ripple, and to handle the ripple current without excessive self heating. Similarly, diode selection is based upon the maximum reverse voltage, forward current and acceptable recovery times for this application. The main switch (Q1) must withstand the high flyback voltage of the first converter and exhibit low conduction loss. Most 600V MOSFET's with less than 10 ohms of on-resistance (Rds on) are good candidates for this low power application.

CONTROL SECTION

The block diagram of the UCC3889 Off-line Power Supply Controller is shown in Figure 3. This IC incorporates several innovative features to reduce external circuitry and complexity while providing control to regulate the output voltage. A variable ON-time and variable OFF-time control algorithm is used to perform regulation. The switch ON-time is

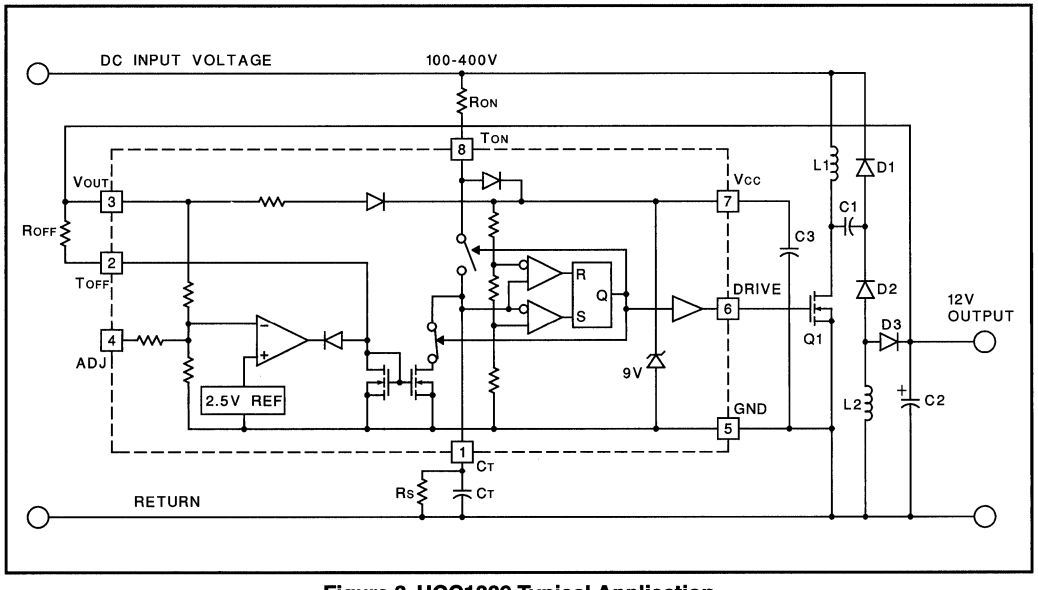

Figure 3. UCC1889 Typical Application

varied inversely with the supply input voltage, whereas the OFF-time is varied inversely with the supply's output voltage. This results in inherent short circuit protection, input voltage feedforward and a greatly simplified control technique. Operation and programming of these key features will be explored in more thorough detail.

POWERING THE UCC3889 CONTROLLER

Note that the UCC3889 is powered by connecting a resistor from the IC's TON pin to the high voltage supply, and not from the VCC connection. An internal switch directs the current from TON to either VCC or to a current mirror used for a timing function, and further details are presented in the TIMING section. Prior to turn-on, this switch is positioned to connect TON to VCC, steering the current into the VCC supply capacitor.

This BiCMOS Control IC consumes less than 250 microamps from the input supply while **VCC** is below it's 8.5 volt undervoltage lockout (UVLO) turn-on threshold. Once on, the IC typically draws only 1.5 milliamps from **VOUT**, and has a UVLO turn-off threshold of 6.3 volts. The **VCC** supply capacitor, CVcc, must maintain the IC supply voltage within it's 2.2 volt UVLO hysteresis region during the start-up of the converter.

Additionally, the minimum line voltage to begin operation of the converter can be programmed. RON, the timing circuit programming resistor also functions to program a current indicative of the AC input line voltage. Turn on occurs when this current reaches 220µA typically, so select the value of RON accordingly. This protection feature therefore will require a minimum current drawn by the IC from the line at all times, so the worst case power dissipation for RON will be at high line.

Two other noteworthy features are the IC's internal 9V zener clamp diode between **VCC** and ground, and the switched current source and diode from **VOUT** to **VCC**. The zener eliminates the need for external overvoltage protection when powered from a current source (resistor) to a high voltage supply, typical of an off-line converter. It also clamps the supply voltage when normally powered from the converter's output voltage. When **VOUT** rises above **VCC**, a switched internal current source is enabled thus limiting the current shunted to ground by the zener clamp diode. This helps minimize wasted power which would otherwise reduce overall efficiency and raise the IC's junction temperature. The series diode also prevents **VCC** from powering **VOUT** during start-up and short circuited output conditions.

GATE DRIVE OUTPUT

A CMOS totempole output stage is incorporated in this IC which provides a rail-to-rail voltage swing of the DRIVE output. A 200mA peak sink current and a 150mA peak source current will adequately drive MOSFETs gates for this low power application. Typical rise and fall times into a 1 nanoFarad load are 35 and 25 nanoseconds respectively.

Schottky clamp diodes to protect the IC's gate drive output from swings below ground and above VCC are NOT needed. The internal body diodes of the CMOS output stage transistors provide sufficient clamping.

OSCILLATOR AND TIMING FUNCTIONS

Programming begins with a selection of the highest operating frequency which will typically occur at low line and full load. As either the load is decreased, or input line increased, the switching frequency will adjust to regulate the output voltage. Therefore, the first parameter to determine is the switching frequency, FS. A good first approximation is 100kHz which will be used for this example.

Fs = 100kHz at low line, full load

The switching frequency selection will determine the exact values of the converter inductors (L1 and L2) in addition to the exact ON-time and OFF-time. Once the inductor values are calculated, the IC can be programmed to deliver the specific control timing functions, **TON** and TOFF. Likewise, the selected ON and OFF times can be used to determine the exact inductor values needed to facilitate the power conversion.

Switch ON-time is developed by charging a timing capacitor from a constant current source. The exact charging current is varied directly with the converter input voltage to deliver a constant volt-second charging of the timing capacitor. This characteristic will exhibit input voltage feedforward and immunize the output from changes in line voltage.

During the charging period of the timing capacitor, the voltage at TON is approximately 4.5 volts. Note that only eighty percent (80%) of the current into the TON pin is used to charge the timing capacitor. The other twenty percent is diverted to the minimum line voltage detection circuitry which is described in the Protection Circuits portion of this Application Note. The exact timing capacitor charging current is therefore :

$$I(CT+) = 0.8 \bullet \frac{(VIN - 4.5)}{RtON}$$

The timing capacitor has a peak to peak amplitude of approximately 3.7 volts for high noise immunity. It begins charging from a lower threshold of 1.3 volts to it's upper threshold of 5.0 volts. While the timing capacitor is charging, the IC's output is high and the converter switch is on. The control circuit ON-time is programmed according to the following formula:

$$t_{ON} = \frac{C_T \bullet 3.7}{I(C_T+)}$$

This can also be expressed as :

$$t_{ON} = \frac{4.6 \bullet C_T \bullet R_{TON}}{V_{IN} - 4.5}$$

The ON-time must correspond to the time required to charge the inductors to a peak current value necessary to maintain regulation of the output voltage for any given set of line and load conditions. Note that the exact voltage at TON will rise from about 2.5 to 6.5 volts while the timing capacitor is charging, so these equations are approximations.

Once the timing capacitor crosses the upper oscillator threshold, the IC output goes low and the main switch is turned off. The timing capacitor is then discharged by a current programmed at the TOFF pin. This discharge current is varied as a function of the converter's output voltage to perform regulation, facilitate startup and provide protection against overload and short circuit conditions. Discharge current is programmed by a resistor (ROFF) from the TOFF pin to ground according to the following equation:

$$I(C_T-) = \frac{V_{OUT} - 0.7}{R_{OFF}}$$

The OFF-time is expressed as :

$$t_{OFF} = \frac{3.7 \bullet C_T \bullet R_{OFF}}{V_{OUT} - 0.7}$$

The total conversion period is a sum of the ON-time and OFF-time for a given set of operating conditions. Combining equations, this can be stated as:

$$t_{PERIOD} = 3.7 \bullet C_T \bullet \left(\frac{R_{TON}}{0.8 \bullet (V_{IN} - 4.5)} + \frac{R_{TOFF}}{V_{OUT} - 0.7} \right)$$

Since one percent resistors are more readily available than capacitors with such a tight tolerance, it is advisable to first select the timing capacitor. Also, resistor values should be kept as high as possible to minimize oscillator currents to attain high overall efficiency, especially in a low power application. A good first approximation is to use 150pF for the timing capacitor value which will "home-in" on timing resistor values between 200k and 2meg ohms for approximately 100kHz operation.

C_T = 150pF (first approximation)

REGULATING THE OUTPUT VOLTAGE

The converter output voltage can be regulated in two different modes, depending on the application. In it's simplest configuration, the output voltage is connected to the IC's VOUT pin and the ADJ pin is unused. An internal 116k/30k ohm resistor network is used to divide the output voltage down for comparison to a precision 2.5 volt reference at the transconductance (gm) amplifier. It's output alters the timing capacitor discharge current to adjust the Off-time in response to any changes in the converter output voltage. In this configuration with the ADJ pin "floating", the output voltage is regulated at 12 volts. This level was selected for general purposes and is compatible with many applications.

Another simple configuration of this control circuit is to ground the ADJ pin. An additional 50kΩ is then placed in parallel with the 30kΩ internal divider resistor thus lowering the impedance to about 18.75kΩ. Grounding the ADJ pin will regulate the converter output voltage at approximately 18 volts instead of 12 volts, as with the ADJ pin floating. This amplitude was selected for use with many popular off-line PWMs as this converters principal load which utilize a 16 volt turn-on threshold. After accommodating their UVLO tolerances, eighteen volts was selected to fulfill nearly all PWM undervoltage lockout requirements.

The converter output voltage can be programmed for any level above 2.5 volts with two parts. An external resistive divider network between VOUT, ADJ and GND is all that's needed. This should be a lower impedance than the IC's internal divider network to null out any inaccuracies due to initial tolerance. By proper IC layout design and procedures, resistor ratios within the device will be maintained quite accurately although their exact values can vary significantly. For this reason, best results are obtained by using lower impedances externally than the 116k, 30k and 50k used within the UCC3889.

CLOSING THE FEEDBACK LOOP

An internal transconductance amplifier (gm type) is used to maintain regulation of the output voltage. The converter's output voltage is divided down by the 116k and 30k ohm resistor network and fed to the inverting input of the error amplifier. This statement applies for the simple configuration where the ADJ pin is unused and left floating. For all other applications which utilize the ADJ pin for programming the output voltage, then the 50k ohm series resistance must be accommodated in the design

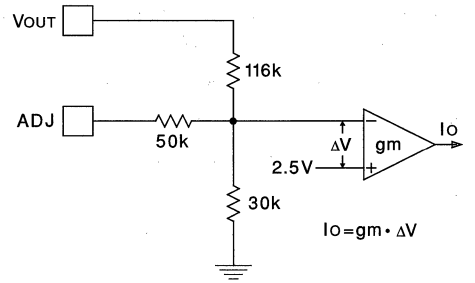

Figure 4. Adjust Pin Details

equations, as shown in Figure 4. For either case, the noninverting error amplifier input is internally tied to a precise 2.5 volt reference. The corresponding amplifier output current is the transconductance of the amplifier (gm) multiplied by the difference in amplifier input voltages (ΔV) and is expressed as:

$$I(E/A)_{OUT} = gm \bullet \Delta V, \text{ where } gm = 1mA/V$$

The error amplifier output current is used to modulate the discharge current of the timing capacitor and perform regulation. This current is subtracted from the capacitor's maximum discharge current which is programmed by ROFF, as shown in Figure 5. Note that the maximum discharge current is limited to 225 microamps within the IC, so a value below this should be used.

When the converter output voltage is low, the timing capacitor discharge current is also low. This is typical of start-up and short circuit conditions. Low discharge current indicates a long discharge time, or OFF-time for CT, corresponding to a low duty cycle. This feature delivers excellent protection under either of these conditions. As the output voltage increases, so does the discharge current. This has the effect of widening the duty cycle in response to the output voltage being lower than it's ideal setpoint. More energy is transferred as the duty cycle widens which continues to raise the output voltage.

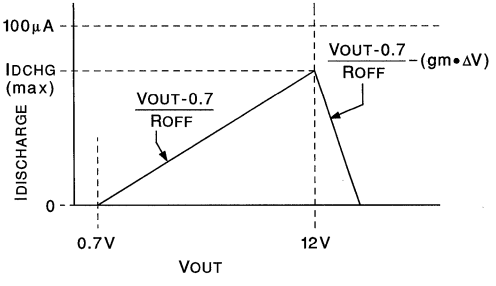

Figure 5. Discharge I vs. VOUT

As the exact point of regulation is reached, the timing capacitor discharge current will decrease as shown in Figure 5. This has the effect of reducing the effective duty cycle in response to the output voltage getting above the ideal threshold. If the output voltage continues to climb, then the discharge current is reduced even further. This will result in a longer OFF-time, or further reduced duty cycle, thus bringing the output voltage back to it's set point. Note that this operational mode also provides overvoltage protection.

PROTECTION CIRCUITRY

For an eight pin device, this UCC3889 features a number of internal protection features. As highlighted in previous sections, the IC has a 9V zener clamp on its supply rail. There is also a diode isolating VCC from the normal power source (VOUT) to keep the IC alive in case of a shorted output or overload condition. A switched current source also protects the zener from the low impedance present at VOUT.

Undervoltage lockout guarantees that the IC does not turn on until all internal circuits are properly biased for normal operation. It also insures an adequate gate drive amplitude is present to the main switch. This is performed by the "VCC OK" comparator as indicated in the UCC3889 block diagram, Figure 3.

Low line lockout protection is also contained within the IC to prevent operation during brown-out conditions and at power down. This eliminates the potential for excessively low frequency operation which can cause saturation of the inductors and abnormally high currents within the power stage. One-fifth of the current flowing into TON is used in conjunction with the "V LINE OK" comparator to detect this situation. Note that this conditional test is performed at every oscillator clock cycle during the charging of the timing capacitor. To further reduce power consumption, the current used for detection of low line, in addition to CT's charging current are switched off while the oscillator discharges each cycle.

Once a low line fault triggers the "V LINE OK" comparator, a 0.5 millisecond fault delay period begins. During this time the IC output is held off regardless of the oscillator operation. This delay limits the converter's retry rate during a brownout to around 2 kilohertz which is a significant reduction in comparison to the switching frequency. In addition, the ON-time of the converter is reduced to 600ns independent of the input line voltage.

Further details and specifications can be obtained on the device's datasheet.

DESIGN EXAMPLE

V_{IN} = 80 to 132VAC, or 100 to 180VDC

V_{OUT} = 12VDC

P_{OUT} = 1 Watt maximum

$F_{SWITCHING}$ = 100kHz

Efficiency = 50% (estimate)

Low line, full load condition will be used to begin the design procedure.

Step 1. Calculate Maximum Duty Cycle

$$\text{DutyCycle (d)} = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

$$d(max) = \frac{1}{1+\sqrt{\frac{100}{12}}} = \frac{1}{3.887} =$$

d(max) = 0.257 (roughly 26%)

Step 2. Calculate $t_{ON}(max)$

$$F_{SWITCHING} = \frac{1}{t_{PERIOD}} = \frac{1}{10\mu s} = 100kHz$$

$$t_{ON}(max) = \frac{d(max)}{F_{SWITCHING}}$$

$$t_{ON}(max) = \frac{0.257}{100kHz} = 2.57\mu s$$

Step 3. Calculate $t_{OFF}(min)$

$t_{OFF}(min) = t_{PERIOD} - t_{ON}(max)$

$t_{OFF}(min) = 10\mu s - 2.57\mu s = 7.43\mu s$

Step 4. Calculate the Maximum Input Power

$$P_{IN}(max) = \frac{P_{OUT}}{n(efficiency)} = \frac{1W}{0.5} = 2W$$

Step 5. Calculate the Input Current at Low Line

$$I_{IN} = \frac{P_{IN}}{V_{IN}(min)}$$

$$I_{IN} = \frac{2W}{100V} = 0.020A$$

Step 6. Calculate the Peak Inductor Current, $I_{L1}(pk)$

$$I_{L1}(pk) = 2 \bullet \frac{I_{IN}}{d} = 2 \bullet \frac{0.020}{0.257} = 0.156A$$

Step 7. Calculate the First Inductor Value (L1)

$$L1 = \frac{V_{IN} \bullet t_{ON}(max)}{I_{L1}(pk)} = 100 \bullet 2.57 \bullet \frac{10^{-6}}{0.156} = 1.67mH$$

Step 8. Calculate the Output Voltage of the First Flyback Stage

Since the volt-second products of the ON-time and OFF-time must balance for any inductor, then $V_{IN} \bullet t_{ON} = V_{OUT} \bullet t_{OFF}$, where V_{OUT} is VC1.

$$VC1 = V_{IN} \bullet \frac{t_{ON}}{t_{OFF}} = 100 \bullet \frac{2.57\mu s}{7.43\mu s} = 34.6V$$

Note that the second inductor (L2) is switched across this voltage while the main switch is on, so VC1 is the applied voltage to the second Flyback stage. Although this capacitor is switched between the lower and upper supply rails, the voltage rating of C1 is much lower than the input. The worst case can be easily calculated using the previous equation for VC1, but note that the IC will adjust the duty cycle to minimize this voltage change over line and load ranges. Specifically, the switching frequency will adjust, so a high voltage capacitor is not needed for normal operation.

Step 9. Calculate the Peak Current in the Second Inductor (L2)

$$I_{L2}(pk) = 2 \bullet \frac{I_{OUT}}{1 - d}$$

$$\text{where } I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{1W}{12V} = 0.083A$$

$$I_{L2}(pk) = \frac{2 \bullet I_{OUT}}{d} = \frac{2 \bullet 0.083}{1 - 0.257} = 0.223A$$

Step 10. Calculate the Second Inductor Value (L2) using the Output Voltage of the First Stage, ON-time and Required Peak Current of L2.

$$L2 = VC1 \bullet \frac{t_{ON}}{I_{L2}(pk)} = \frac{34.6 \bullet 2.57 \bullet 10^{-6}}{0.223} = 398\mu H$$

Step 11. Verify the Estimated Output Voltage, V_{OUT}

$$V_{OUT} = \frac{V_{IN}(stage\ 2) \bullet d}{1 - d}$$

$$V_{OUT} = \frac{34.6 \bullet 0.257}{0.743} \approx 12.0V$$

Note that this is an approximation and does not account for the output rectifier voltage drop nor any other losses. The control circuit will adjust for these losses since it is operating closed loop and modify the OFF-time, hence duty cycle, accordingly.

PROGRAMMING THE UCC3889 FUNCTIONS

The timing functions of the IC will be programmed according to the timing intervals which

have been calculated for 100kHz operation. A 150pF timing capacitor has been selected as a starting point to simplify the design process. The specific ON-time and OFF-time programming resistors are obtained from the previous equations by inserting the appropriate times and capacitor value.

Step 12. Calculate RtON

$$RtON = \frac{tON \bullet (VIN - 4.5)}{4.6 \bullet CT}$$

$$RtON = \frac{2.57 \bullet 10^{-6} \bullet (100 - 4.5)}{4.6 \bullet 150 \bullet 10^{-12}}$$

RtON = 348.9k (use 330kΩ)

Step 13. Calculate ROFF

$$ROFF = \frac{tOFF \bullet (VOUT - 0.7)}{3.7 \bullet CT}$$

$$ROFF = \frac{7.43 \bullet 10^{-6} \bullet (12 - 0.7)}{3.7 \bullet 150 \bullet 10^{-12}}$$

ROFF = 149.3k (use 150k)

Step 14. Calculate RDCHG

A resistor placed in parallel with the timing capacitor is used to discharge CT when the converter output voltage goes to zero. This also sets the maximum OFF-time of the switch and is used to program the minimum frequency for startup and short circuit protection. A one millisecond (1ms) duration will be used for this example.

$$RDCHG \approx \frac{tOFFmax}{3.7 \bullet CT}$$

RDCHG = 1.78 meg (use 1.8 or 2 meg)

PROGRAMMING THE OTHER PINS

An output voltage of 12VDC has been selected which does not require a resistor divider for feedback. The IC's ADJ pin is open for this application. Also, the MOSFET gate will be directly connected to the IC's output and no gate drive resistor is needed. Typical 0.1µF bypassing will be used at the IC's supply voltage, VCC. A tight prototype layout is also recommended as good design practice.

PROTOTYPE ASSEMBLY

The entire 1 Watt off-line power supply can be built with as few as 16 parts for a 110VAC only input as shown in Figure 6. Using surface mount assembly techniques and a tight PC board layout, the completed assembly requires about one square inch (1" sq.of area). A performance evaluation for this example is summarized below.

UNIVERSAL INPUT VOLTAGE (80 to 265VAC)

Due to the higher voltage input (373Vpk), L1 and RtON will be broken-up into series components which can conservatively handle the applied voltage. For example, three identical 1/4W resistors will be used as RtON due to the maximum voltage rating of 200 volts each. Inductor L1 is divided into two very inexpensive axial type inductors also placed in series to withstand the high voltage. All other lower voltage components are similar to the 110VAC only application, and are readily available, standard types used in the industry.

The bulk input capacitor should be conservatively rated for 450VDC, and the input diodes are 800V types. Since the circuit operates in the discontinuous inductor current mode, diode switching speed is not very critical. However, diodes should have recovery times below a quarter of a microsecond (trr < 250ns) for efficient high frequency operation, and rated for the proper reverse voltage. Standard

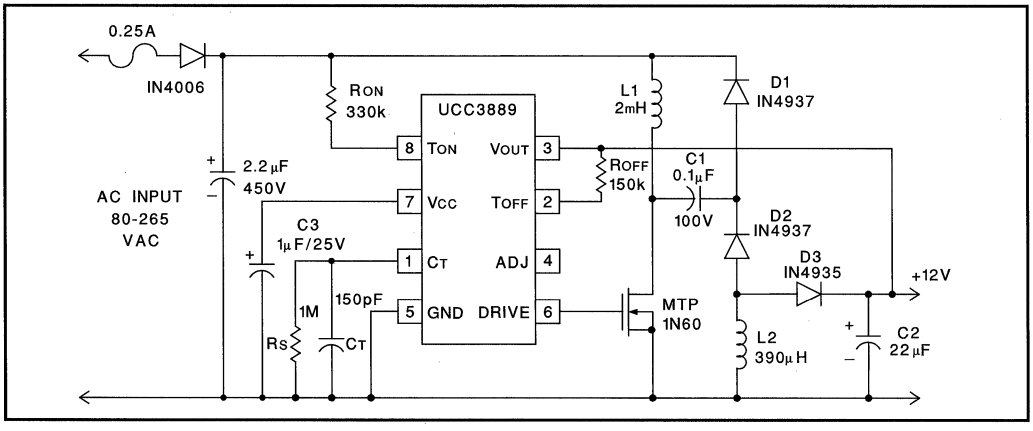

Figure 6. Design Example

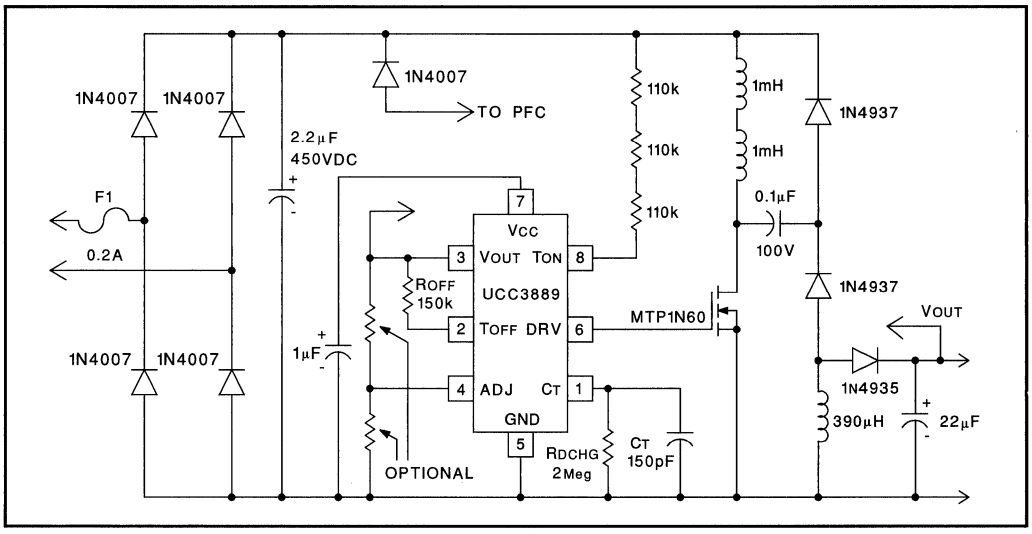

Figure 7. Typical 110/220VAC Application

1N4937 type 600V diodes can be used in the high voltage switching sections, and a lower voltage 1N4935 is a good selection for the output diode. To simplify manufacturing, 1N4937s can be used for all three rectifier applications. The complete schematic and list of components is shown in figure 7. Measured performance is indicated above.

UCC3889 Application Circuit Performance Measurements

110VAC (only) and 110/220 Universal AC input Nonisolated models

VIN (VAC)	VOUT (VDC)	POUT (W)	EFFCY (approx)
78 (both)	12.16	0.58	45%
	12.15	0.81	47%
	12.11	1.00	47%
128 (both)	12.22	0.59	45%
	12.23	0.82	45%
	12.24	1.02	44%
170 (110/220 only)	12.24	0.59	44%
	12.25	0.82	44%
	12.26	1.03	44%
264 (110/220 only)	12.24	0.59	40%
	12.26	0.82	42%
	12.28	1.034	43%

VOUT nominal = 12.195V, ±0.7% (±85mV)
Efficiency nominal = 44%

ISOLATING THE OUTPUT VOLTAGE

An isolated output voltage is obtainable with this UCC3889 controlled cascaded Flyback conversion technique. While several possibilities exist, one of the easiest places to attain isolation is at the inductor used in the second power conversion stage, as shown in Figure 8. Due to its lower inductance than the first stage, fewer turns are required and generally a smaller core can be utilized. Note, however, that the core size could be predominantly determined by the isolation requirements and not the stored energy requirements of the system. Designers are encouraged to pursue various core geometry options depending on the specific isolation voltage, safety agency and creepage/clearance distance requirements.

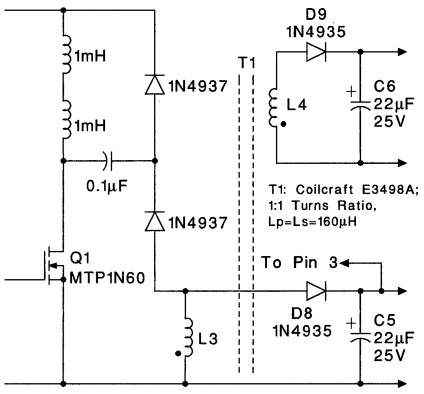

Figure 8. Isolated Output

One rather quick, inexpensive and effective way to provide an isolated output is to use an "off-the-shelf" isolation transformer which meets the design specifications. Many standard "Common Mode Line Chokes" used for EMI filters and suppression meet the appropriate voltage isolation requirements. One example of this is the Coilcraft "EE Style" series of line chokes. Specifically, their E3496A through E3498A coupled chokes have inductances between 168µH and 468µH, and can handle currents from 2.5 to 4 amps. As stated previously, there are a variety of other manufacturers, core styles and ratings to choose from, in addition to designing one's own.

REGULATING THE ISOLATED OUTPUT

Maintaining adequate regulation of the isolated output voltage over all line and load conditions without any feedback path to the IC via optocoupler (etc.) is possible. If both windings of the isolating inductor were perfectly coupled then the voltages of each would look identical regardless of which one was being loaded. As is always the case, truly perfect magnetic coupling cannot be obtained, resulting in detrimental series, leakage inductance. This detracts from the ability for one winding to perfectly track the other which will degrade output voltage regulation. These effects are minimized by a low leakage inductance design, but some finite leakage is to be expected, especially with high voltage isolation between windings.

Preloading of the "feedback" winding which powers the UCC3889 IC and provides the voltage feedback information will improve regulation of the isolated output over all load conditions. While this does reduce overall efficiency, the small penalty

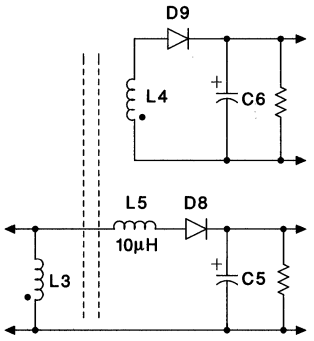

Figure 9. Adding Series Inductance to Improve Cross Regulation

may be an acceptable compromise for the improvement in regulation.

The best option to improve regulation is to add some series inductance to the "feedback" winding as shown in Figure 9. Note that when placed as shown, the inductance is not part of the circuit while the coupled inductor is charging, but only during the discharge. This additional inductance has the effect of steering all ripple current (hence stored energy) to the isolated output which is more heavily loaded. Energy is transferred to where it is needed most, at the load, and not to the control circuit. By varying the series inductance and preloading of each output, excellent regulation of the isolated output voltage can be achieved without requiring a separate feedback path.

An isolated version of the universal input range application circuit of Figure 10 was constructed and

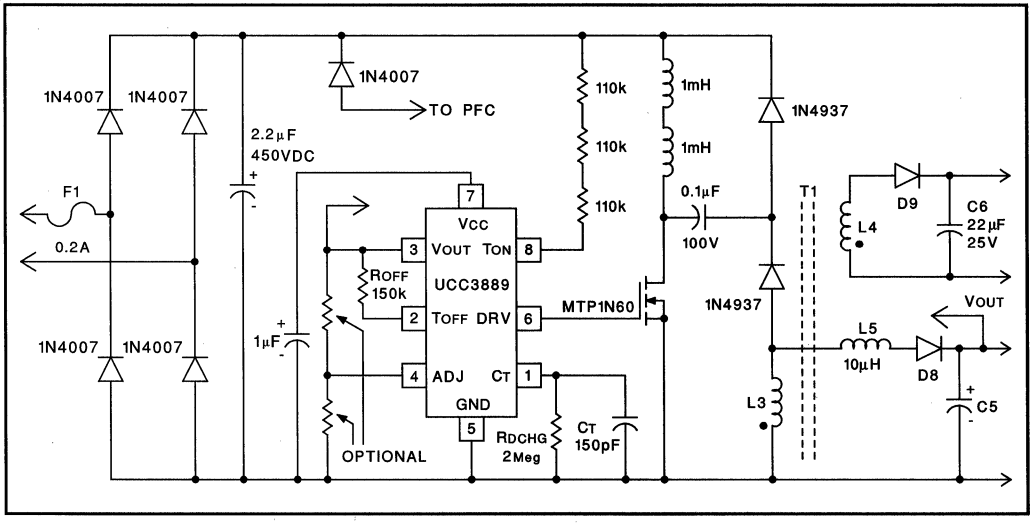

Figure 10. Isolated Output with Universal AC Input Range

tested. Performance results are shown below for comparison to the nonisolated version.

UCC3889 Application Circuit Performance Measurements

110/220 Universal AC Input with Isolated Output

VIN (VAC)	VNONISO (VDC)	VISO (VDC)	POUT (W)	EFFCY (approx)
78	12.37	12.07	0.41	45%
	12.31	11.85	0.63	46%
	12.26	11.63	0.82	47%
	12.26	11.33	0.99	51%
156	12.39	12.14	0.42	44%
	12.36	12.00	0.64	45%
	12.37	11.80	0.85	46%
	12.37	11.72	1.06	44%
195	12.42	11.77	0.39	43%
	12.39	11.59	0.60	44%
	12.36	11.33	0.78	44%
	12.33	11.42	1.00	45%
240	12.43	11.819	0.39	39%
	12.41	11.697	0.61	42%
	12.39	11.605	0.81	43%
	12.38	11.626	1.04	43%

Nonisolated VOUT nominal = 12.349V, ±0.7% (±85mV)
Isolated VOUT nominal = 11.74V, ±3.4% (±400mV)
Efficiency nominal = 45%
Main Transformer = COILCRAFT E3498A "Common Mode EMI Filter Choke", Turns Ratio = 1:1, Lp = Ls = 160µH (approx), 3750VAC Isolation

EFFICIENCY

The efficiency measurements indicate the overall ratio of output power divided by the input power, and are typically around 45%. Note that this figure includes the power lost in the timing resistor (RTON) **connecting the input supply voltage to the UCC3889 for initial startup and continuous input line voltage detection. The power consumed to perform this function is approximately 30 milliwatts at low line, but nearly 400 milliwatts at high line. Once this loss is accounted for, the remaining losses demonstrate that this converter runs between 51% and 63% efficiency at high line, depending on load. It is clear that this cascaded flyback conversion technique is a highly efficient solution to low power applications, especially with a high voltage input.**

OTHER APPLICATIONS

Although primarily designed for off-line applications, the UCC3889 Bias Supply Controller and the cascaded Flyback Conversion technique are equally applicable for low power DC/DC converters. Typical usages are to generate a bias supply for the main PWM controller, or to deliver a regulated, low power output supply. The simple implementation of this control technique is further applicable to numerous other topologies including conventional Flyback, Forward and other single switch converters.

SUMMARY

The task of generating a low power, low voltage bias supply can be greatly simplified using this novel cascaded Flyback converter technique. Inexpensive, readily available standard components can be used in cost sensitive applications, while miniature surface mount devices are best suited where size is a premium. Furthermore, this approach can be utilized to generate an isolated low power supply without the complexity of voltage feedback circuitry. Finally, a sophisticated 8 pin IC, the UCC3889 Bias Supply Controller has been introduced to minimize external components while providing complete protection of the converter and regulation of the output voltage.

NOTES

1. The control technique implemented by the UCC3889 Control IC is used under agreement from Lambda Electronics and is patent pending. Designs incorporating this control technique are not in violation of this patent provided that the UCC3889 is used as the control device.

2. COILCRAFT's phone number is : 1-800-322-2645 (U.S.).

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APPLYING THE UCC3570 VOLTAGE-MODE PWM CONTROLLER TO BOTH OFF-LINE AND DC/DC CONVERTER DESIGNS

By Robert A. Mammano
Vice President
Advanced Technology

Abstract

BiCMOS processing provides the key to a new integrated PWM controller which offers higher switching frequencies at lower quiescent current drain while including new innovations in both performance and protection features. Its versatility is demonstrated with the description of a 50W, wide input voltage range, off-line inverter and a 48-to-5V isolated DC/DC converter, both of which feature efficiencies in the range of 80 percent.

INTRODUCTION

Over the years, our industry continues to see a steady evolution in power control technologies as new circuit topologies offer performance improvements over those achievable with older designs. For instance, current-mode control has become today's dominant control algorithm as its introduction brought such benefits as:

- Instant response to line variation
- Inherent pulse-by-pulse current limiting
- Faster loop response

These characteristics were quite significant when compared to the voltage-mode circuits built with the technology of the early 1980's when current-mode IC's were first introduced. However, both circuit design and IC process developments during the intervening years have shown that these capabilities are not necessarily limited to current-mode control. And along with the benefits of current-mode control have come several difficulties which have notably complicated the power supply designer's tasks. Among these are:

- Dealing with the current waveform's leading-edge spike
- Eliminating the effects of ringing or other noise sources
- Adding the appropriate amount of slope compensation
- Analyzing circuit performance with two feedback loops
- Providing good regulation with multiple outputs
- Stabilizing PWM operation with low amplitude ramp waveforms

Although solutions can and have been found for all the above issues, these difficulties have inspired a re-evaluation of voltage-mode control in the light of today's technology. In particular, it seemed desirable to incorporate some newer circuit concepts - such as voltage feed-forward, programmable duty-cycle limiting, and sophisticated fault protection - into a design which could also benefit from low-current BiCMOS processing. These circuit and process innovations have resulted in a new IC controller equally at home in wide voltage range off-line inverters and highly efficient isolated DC/DC converters.

INTRODUCING THE UCC3570

The overall block diagram for the UCC3570 is shown in Figure 1. While this architecture may look relatively complex, it is not because of the pulse-width modulation circuitry. Although this may be the heart of the controller, it is implemented with only the comparator, OR-gate, latch, and output driver shown across the center of the diagram. Since the UCC3570 is intended for isolated applications, there is no error amplifier, anticipating that this function will be on the opposite side of the isolation boundary.

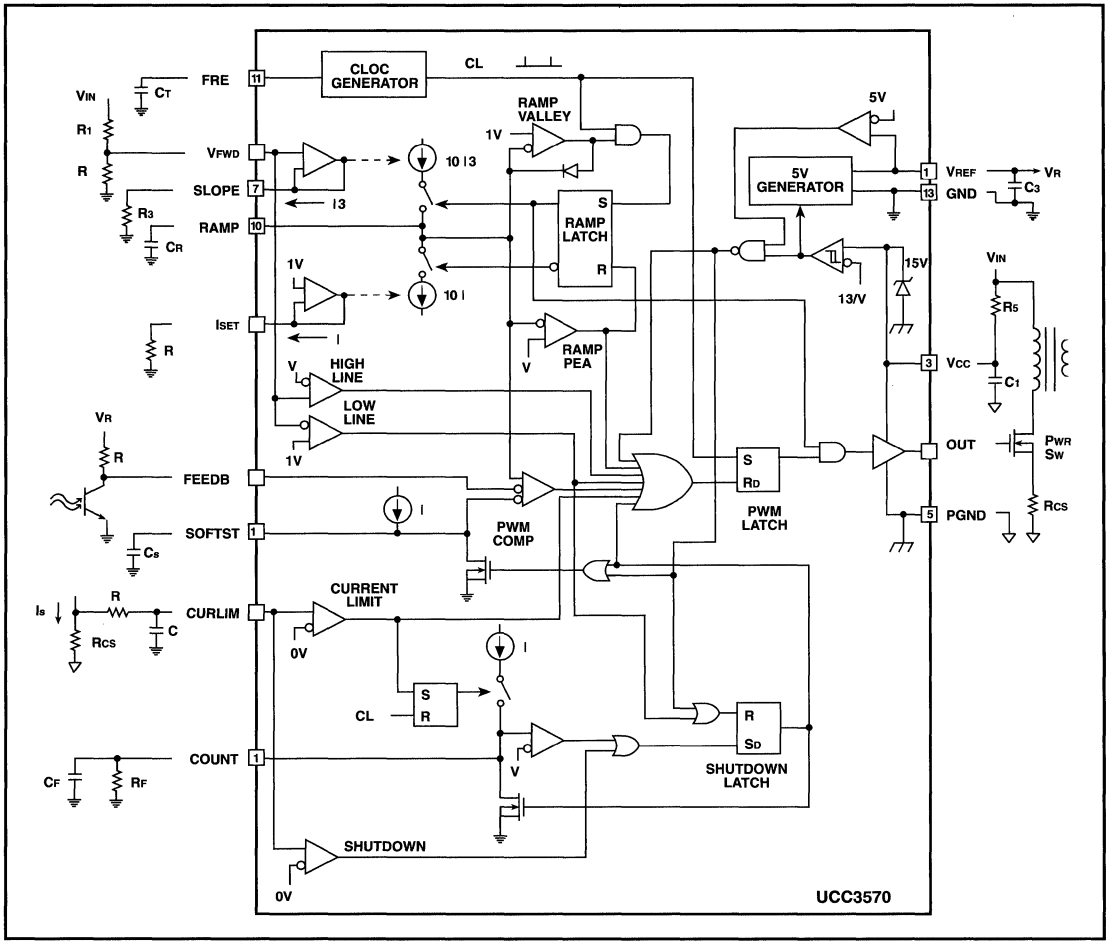

Figure 1. The overall block diagram of the UCC3570 showing connections to typical external components.

The emphasis given to programming and protection is indicated by the multiple-input OR-gate in the PWM path. This gate will terminate or prevent an output pulse if any of its inputs are high. The input signals to this gate are derived from the remainder of the circuitry. These other circuits can be divided into three sections which are described below: Ramp generation, Power sequencing, and Fault protection.

RAMP GENERATION CIRCUITRY

An important circuit feature incorporated into the design of the UCC3570 is a unique PWM ramp generator which combines voltage feed-forward, duty-cycle clamping, and fixed frequency operation. While all of these characteristics have individually been used before, combining them into a control which will automatically and linearly provide an open-loop PWM correction for large input voltage variations, and allow a maximum duty-cycle clamp to be user-set over a 20%-to-80% range, while maintaining constant switching frequency, was a challenge met with the circuitry shown separately in Figure 2.

The ramp voltage waveform is formed by charging an external capacitor with a current source made proportional to the input line voltage, and discharging it with a programmable current sink which determines the minimum deadtime. Switching between the charging and discharging currents is commanded by a flip-flop which is set with a constant-frequency clock signal, and reset when the ramp reaches four volts. To insure constant ramp amplitude, the bottom of the ramp is held at one volt while awaiting the clock command to start the next charge cycle. If the ramp discharge has not returned to one volt at the end of the period, the clock is blocked, forcing the circuit to wait through the next period before charging again by accepting the following clock signal.

These relationships are shown in Figure 3 which compares the ramp waveform with three different levels of input voltage.

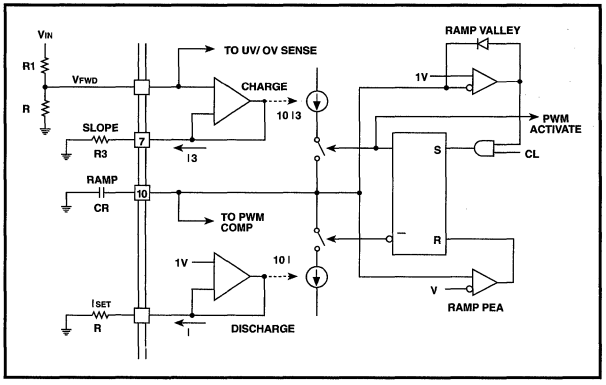

Figure 2. The ramp generation portion of the UCC3570 with independent rise-time, fall-time, and frequency control.

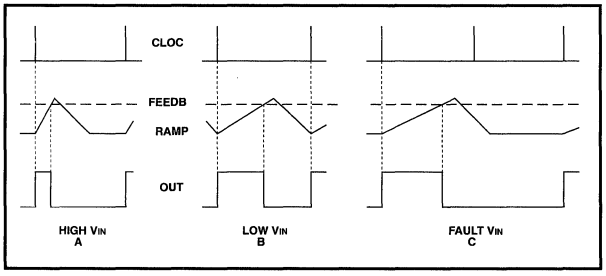

Figure 3. Effects of line voltage on the ramp waveform showing a variable slope rise, constant fall, and guaranteed minimum off-time.

PROGRAMMING AND PROTECTION

The power sequencing features of the UCC3570 are highly optimized for off-line operation beginning with the fact that the BiCMOS process yields very low operating currents for this device - one milliamp to run and less than 100 microamps prior to starting. In addition, there are two pins which sense the line voltage and provide turn-on/turn-off functions. VCC provides chip power and has a UVLO circuit which sets turn-on at 13 volts with a 4-volt hysteresis. VFWD is primarily intended to provide voltage feed-forward by adjusting the ramp slope, but this pin is also monitored by over and under-voltage sensing comparators which terminate output pulses if the line voltage is outside its defined operating range. Because VCC will normally require an energy storage capacitor, it will respond more slowly than VFWD and since both must be above a minimum for operation, turn-on will typically be initiated by VCC while a collapsing voltage on VFWD will provide a faster turn-off. Turn-on is further controlled by a Soft-Start circuit which minimizes both starting currents and output voltage overshoot.

Another valuable circuit feature is an over-current fault protection technique which provides fast pulse-by-pulse current limiting with the ability to accept a definable period of over-current operation and then shut the system down if the fault is continuous. Referring again to Figure 1, the Current Limit pin is shown monitored by two comparators with thresholds of 0.2 and 0.6 volts. (It might be noted that noise filtering here has no impact on the feedback control loop as it would with current-mode control.) When the 0.2V threshold is exceeded, the output is commanded off within 100nsec. In addition, each time this occurs, an increment of charge is added to the capacitor on the COUNT pin and should the voltage on this pin rise to 4V, a Shutdown Latch is activated. This latch is also triggered immediately if the current limit signal crosses the 0.6V threshold. Reset of the Shutdown Latch occurs when either VCC or VFWD falls below its lower threshold which allow a variety of options for either manual or automatic restart but, in either case, reset initiates a normal soft-start.

WARNING

Off-line AC power supplies are intrinsically hazardous!!!

The power supply described herein contains dangerous voltages!

Never allow human contact with any part of the input circuitry of any power supply, including the input ground connections, if it is not connected through an isolation transformer, whether the supply is turned on or off.

The supply described herein uses and can produce voltages which are potentially lethal! It should be serviced or tested only by experienced, qualified personnel, with proper techniques and equipment!

WARNING

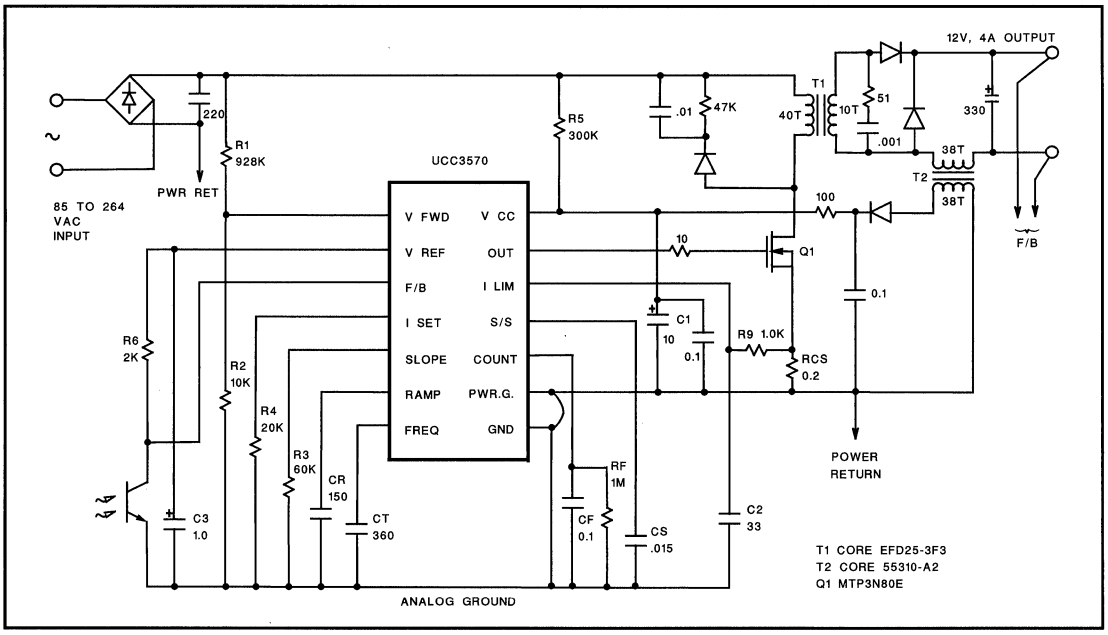

Figure 4. A simplified schematic for a 50 Watt, off-line power converter with full fault protection applicable to worldwide line voltages.

AN OFF-LINE APPLICATION

The 50 Watt off-line supply shown in Figure 4 is presented to illustrate a typical use for this controller. This application is intended for highly cost-sensitive markets requiring operation over world-wide line voltages. Its forward topology provides good regulation with low output ripple and it takes advantage of the low current requirement of the UCC3570 to allow simple interfacing to the high voltage line with minimal power loss. The switching frequency is 225kHz with the allowable duty-cycle range set to a maximum of 67% - a value which keeps the peak switch current low while still insuring a finite reset time for the transformer. The design steps which follow, while perhaps less rigorous than some might wish, should still provide a check list of items for the designer to consider when applying the UCC3570, regardless of the specific application.

TRANSFORMER RESET

In any single-ended power stage design, the plan for transformer reset is one of the first design decisions needed. In providing a power pulse to the output, the transformer is driven in one polarity for a finite number of volt-seconds. To prevent saturation, the same number of volt-seconds must be provided in the opposite polarity between the termination of one power pulse and the beginning of the next one. Since it is the volt-second product which must be met, many compromises can be made between the amount of reset voltage allowed and the time allocated. The UCC3570 simplifies this analysis to the extent that the worst case situation will always be at the lowest operating voltage. This is because, when properly set up, the voltage feed-forward feature will automatically increase the minimum off-time as the input voltage increases.

While most single-ended converters allocate 50% of the switching period for transformer reset, in the interests of allowing a lower peak input current, the maximum duty-cycle for this application was extended to 67%, allowing only one-third of the period for reset. This precluded using a reset winding on the power transformer with a 1-to-1 turns ratio. While a higher turns ratio could have been used, that would have offered the choice of either recycling the reset energy to the source and thereby requiring a much higher voltage power switch, or wasting all the reset energy in a lower voltage clamping circuit.

Since neither choice was particularly attractive - and to save the cost of a separate reset winding on the transformer - the solution for this design was to use an R-C-D snubber for reset. This passive resistor-capacitor-diode network will generate a variable clamp voltage - high at minimum V_{IN} since the capacitor has less time when it is not charging, and lower at high V_{IN} since the shorter on-time provides more discharge time for the capacitor. An obvious benefit of this solution is simplicity - only three passive components and no reset winding on the transformer. The disadvantage is that there is some reset energy lost in the resistor but in this case it was only approximately 0.5W. Using this R-C-D clamp

allowed setting the maximum duty cycle at 67% at low line, while still clamping the maximum drain voltage of the switch to 500 volts under high line conditions. These drain voltage waveforms are shown in Figure 5.

TRANSFORMER DESIGN

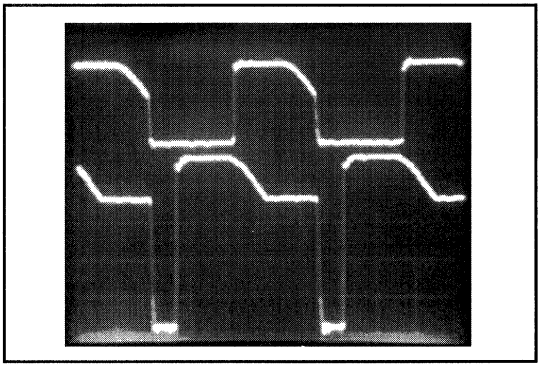

Figure 5. FET drain voltage at full load with VIN = 85 VAC (top trace) and VIN = 264 VAC (lower trace) V = 100V/div, H = 1.0µs/div.

Since this power supply is intended for world-wide operation, the line voltage range was established as 85-264 VAC. This means the peak rectified DC input voltage could be assumed to range from 120 to 373 VDC, but allowing 25 volts of ripple at low line brings the lower limit down to 95 volts. With a switching frequency of 225kHz, the maximum on-time would be 67% of 4.44µsec, or 2.9µsec at the lowest input voltage.

For reasons of cost and size, a Philips EFD-25 ferrite core (3F3 material) was selected through an iterative process of determining a flux swing from the high-frequency core loss characteristics of an assumed core size, using Faraday's law to calculate the number of turns, and then verifying that these turns would fit onto that core size. The EFD-25 core structure is shown in Figure 6 and its size yields a core area of 0.58cm^2 and a volume of 3.3cm^3. If the flux swing is less than 1.25kG at 225kHz, the core loss should be less than 0.25 Watt. The number of turns are calculated from

$$V_{IN} = \frac{N \Delta B Ae}{T_{ON}\, 10^8} \quad \text{or}$$

$$N = \frac{95V \bullet 2.9\mu s \bullet 10^8}{1250G \bullet 0.58cm^2} = 38t$$

which was rounded up to 40 turns.

The number of secondary turns is calculated from

$$V_O = [V_{IN} \bullet \frac{Nsec}{Npri} - Rect\ drop] \bullet Duty\ Cycle, \text{ or}$$

$$12 = [95 \bullet \frac{Nsec}{40} - 1.0V]\ 0.67, \text{ which yields}$$

Nsec = 8 turns. (10 turns was used in this example to provide added operating margin.)

The final transformer design, which is illustrated in Figure 7, incorporated 40 turns of #24 wire wound in two sections to sandwich the secondary, which consisted of 10 turns of four strands of #26 wire. The DC resistance of the primary calculated 0.16 Ohm while the secondary amounted to 0.016 Ohm. Using these values and the core loss curves, the total power loss was calculated as:

Primary loss	=	153mW
Secondary loss	=	243mW
Core loss	=	165mW
Total loss	=	561mW

which, in consideration of the transformer's volume of approximately four cm^3, should experience a maximum temperature rise of less than 20°C.

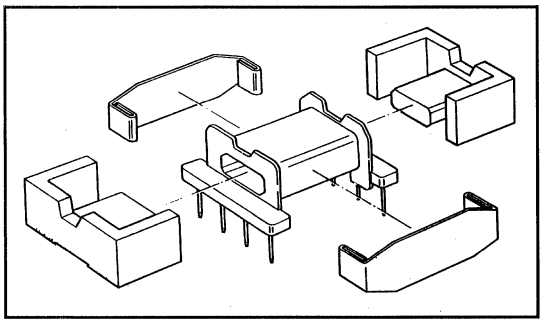

Figure 6. The Philips EFD core assembly optimized for low board profile.

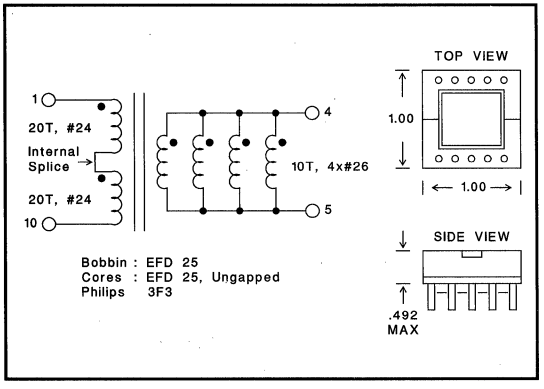

Figure 7. Power transformer schematic and physical dimensions.

OUTPUT INDUCTOR DESIGN

The output inductor must be designed to handle the maximum DC load current without saturating while maintaining continuous conduction at the minimum load. This minimum load was arbitrarily set at 5% of the full 4 Amp load. The worst-case light-load condition occurs at high line where the duty-cycle is calculated to be 0.13 which gives an off-time of 3.9µsec. The minimum value of inductance can then be calculated as

$$L = V\ dt/di, \text{ or } \frac{13V \bullet 3.9\mu s}{0.4A} = 127\mu H$$

The number of turns is calculated from the core characteristics, picking a core large enough to retain adequate inductance at maximum load. In this case, these goals were met with a Mag Inc toroidal 55310-A2 core and 38 turns of #20 wire. Since the control bootstrap voltage and the output can be equal in this case, a second 38 turns of #34 wire powers the control circuit. Power lost in the inductor is calculated as 92mW in the core and 630mW in the wire resistance for a total of approximately 0.75 Watt.

CONTROL CIRCUIT POWER

Another early question to be answered in the design of an off-line power supply is the method used to power the control circuit. Two obvious possibilities are often ruled out: using a separate 60Hz step-down transformer is costly overhead in a low power application; and powering the primary circuitry directly from the high bulk voltage will require a series dropping resistor whose power dissipation is usually unacceptable. While BiCMOS control circuits require very little quiescent current, the determining factor is now usually the power MOSFET gate drive energy. The average gate current for a power MOSFET can be approximated by

$$Ig(ave) = Qt \bullet f$$

where Qt is the total gate charge and f is the switching frequency. Note that this current is relatively unaffected by input voltage, duty-cycle, or output loading. Therefore, I_{CC} for the UCC3570 can be assumed to have three distinct fixed values: pre-startup, active but with no output switching, and operating the power switch.

The most common method for supplying primary control power is the use of a low voltage "bootstrap" winding from the high frequency power transformer. Since this power source is only active when the circuit is switching, start-up energy must still come from the bulk voltage and it must be recognized that anything which stops the switching will cause the control circuit to lose power. When using a separate winding on the transformer with a forward topology, the peak voltage will vary with input voltage which could result in some power loss if the control voltage must be clamped. This application solves that problem by taking power from a second winding in the output inductor. The polarity is such that this winding conducts during flyback when it has the output voltage (times the turns ratio) across it.

POWER MOSFET SELECTION

While the choice of power switch is primarily determined by the input voltage and current, secondary considerations must include the balancing of conductive losses - determined by $R_{DS}(on)$ - against the switching losses which are largely related to the gate charge requirements and the capability of the drive circuitry. The device selected for this supply is the Motorola MTP4N80E which has the following key specifications:

Drain-source voltage.....800 Volts

Continuous drain current .....3 Amps

$R_{DS}(on)$ at 25°C.....1.95 Typ, 3.0 Max Ohms

Total gate charge .....36 Typ, 80 Max nC

Drain-source capacitance 200pF

With a 40:10 transformer turns ratio, the input current will be approximately one Amp. The conductive loss is calculated from the input current (adding a factor to account for less than 100% efficiency), the drain-source resistance (accounting for its positive temperature coefficient), and the maximum duty cycle.

The switching losses are best determined empirically but they can be estimated with a knowledge of the switching times, calculated from the total gate charge divided by the peak gate current. These times are typically less than 50nsec since the UCC3570 can deliver up to one Amp of gate current.

In this design, the total power loss estimates for the MOSFET are

Conductive loss..... 2.0 Watts

Switching losses ..... 4.7 Watts

With a total of 6.7W, this device will have the highest dissipation within the supply and heatsinking the TO-220 package will be required.

UCC3570 PROGRAMMING

Establishing the operating parameters for the UCC3570 requires a very straight-forward series of independent calculations which are well described in the data sheet for this device. The following is merely a simple overview, listing the recommended sequence of calculations. The block diagram of Figure 1 should be referenced for all component designations and it should be assumed that all equations are first-order approximations with more exact values to be defined empirically.

1. Set chip operating current : $I_{SET} = 1V / R4 = I4$

2. Set switching frequency : $fs = 1.8 / (R4 \bullet C_T)$

3. Set minimum deadtime : $td = 0.3 \bullet R4 \bullet C_R$

4.Set feed-forward range : The UCC3570 establishes this range as 4:1 by the 4V and 1V limits set for V_{FWD}. Therefore,

$V_{IN}(Max) = 4 \bullet (R1 + R2) / R2$, and
$V_{IN}(Min) = 1 \bullet (R1 + R2) / R2$.

Note that if a greater range is required, or a voltage range different from that of the duty cycle, it can be accommodated by raising R2 and R3 off ground by a small bias voltage, $0 < Vb < 1V$, or by using the equivalent circuit shown in Figure 8.

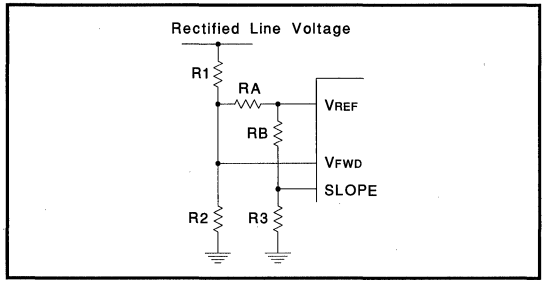

Figure 8. Modifying the 4:1 the input voltage ratio. RA works with R2 to increase the voltage range and RB works with R3 to change the feed-forward gain.

5.Set feed-forward slope : The up-slope of the ramp waveform is

$dV / dt = 10 \bullet V_{FWD} / (R3 \bullet C_R)$.

This can be used to define

$t_{ON}(Max) = 0.3 \bullet R3 \bullet C_R / 1V$, and
$t_{ON}(Min) = 0.3 \bullet R3 \bullet C_R / 4V$.

6.Set current fault parameters : The value for the current sensing resistor is established by the 200mV threshold for the CURLIM pin. Shutdown will occur when the circuit is operating in current limit mode for a time determined by

Time to S/D = $4V \bullet C_F \bullet R4 \bullet (T / t_{OFF})$

Note that this time will be extended by the current which is drained away from C_F by the action of R_F.

The total schematic and parts list for this application are given in Appendix A (see page 10) and some representative waveform photographs of its performance are shown in Figures 9 through 12. While this converter design could find many practical applications as shown, many additional options are possible. For example, reducing the value of the start-up resistor (R5 in Figure 1) such that V_{CC} will not fall below 9 volts after shutdown interrupts the bootstrap voltage, will provide a positive latch-off from a fault. Output over-voltage shutdown can easily be added by a sensing circuit on the secondary driving the COUNT pin through a second optocoupler. And, of course, it should be easy to reconfigure this design to further optimize efficiency, size, cost, or power level to meet a different set of priorities.

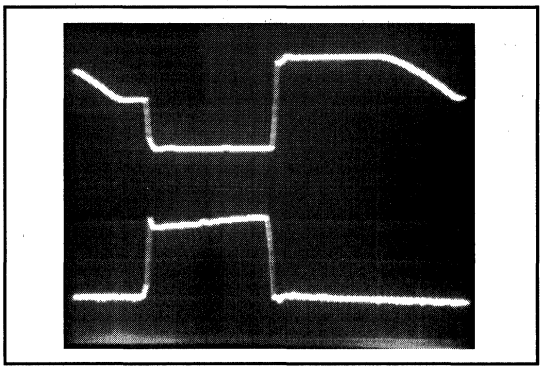

Figure 9. Drain voltage and current at 115VAC and full load. V1 = 100V/div, V2 = 0.5A/div, H = 0.5µsec/div.

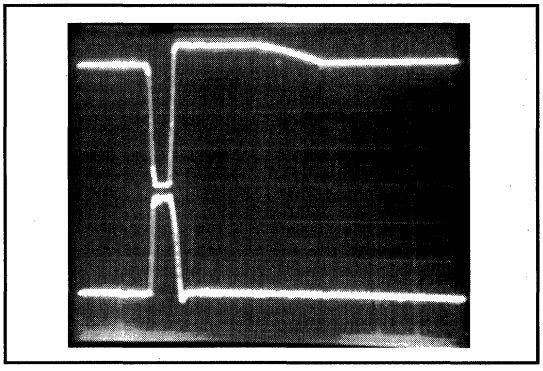

Figure 10. Drain voltage and current under short circuit conditions at 264VAC input. V1 = 100V/div, V2 = 0.5A/div, H= 0.5µsec/div.

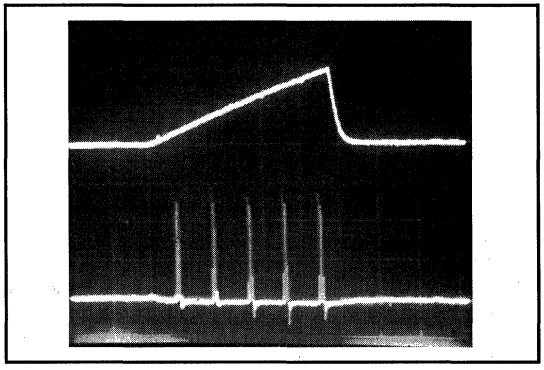

Figure 11. Count voltage with a continuous short circuit (current waveform is aliased) V = 2V/div, H = 2msec/div.

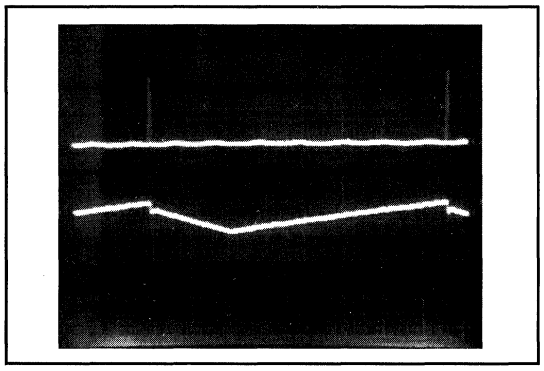

Figure 12. Auto recycle with the output shorted. V1 is count waveform at 2V/div, V2 is VCC at 5V/div, H = 0.2 seconds/div.

A SIMPLE DC/DC CONVERTER

A second application for the UCC3570 illustrates its use in an isolated DC-to-DC converter designed for a load module in a distributed power system architecture or as a telecom power source. This 20 Watt design, as shown in Figure 13, will accept an input voltage from 30V to 60V while maintaining a constant 5V output. A unique element of this design is the controller's ability to get its supply current from only the input voltage, eliminating the need for a low-voltage bootstrap supply driven from the power transformer. This is made practical by both the low operating current of the UCC3570 and by driving a low-gate charge FET at less than maximum frequency. The IRF630 has a total gate charge requirement of only 30nC maximum which, at 100kHz, means only 3mA of average gate current. Add 1mA for the IC, another for miscellaneous programming resistors, and 5mA is all that is needed for the total primary circuitry. This can readily be taken directly from the input voltage but, for improved efficiency, a simple current source has been added to keep this current constant with changing input voltage levels.

Without a bootstrap voltage source to collapse and recycle VCC after a fault-activated shutdown, this design would normally require a manual restart; however, several other options are possible. For example, adding a diode from the VFWD to Soft-Start pins will provide a hiccup operating mode but with a relatively short off-time. For a low duty-cycle mode, a delayed restart can

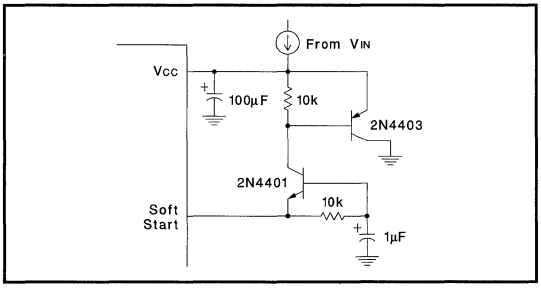

Figure 14. Two transistors will provide an external auto-restart by recycling VCC when Soft-Start is reset.

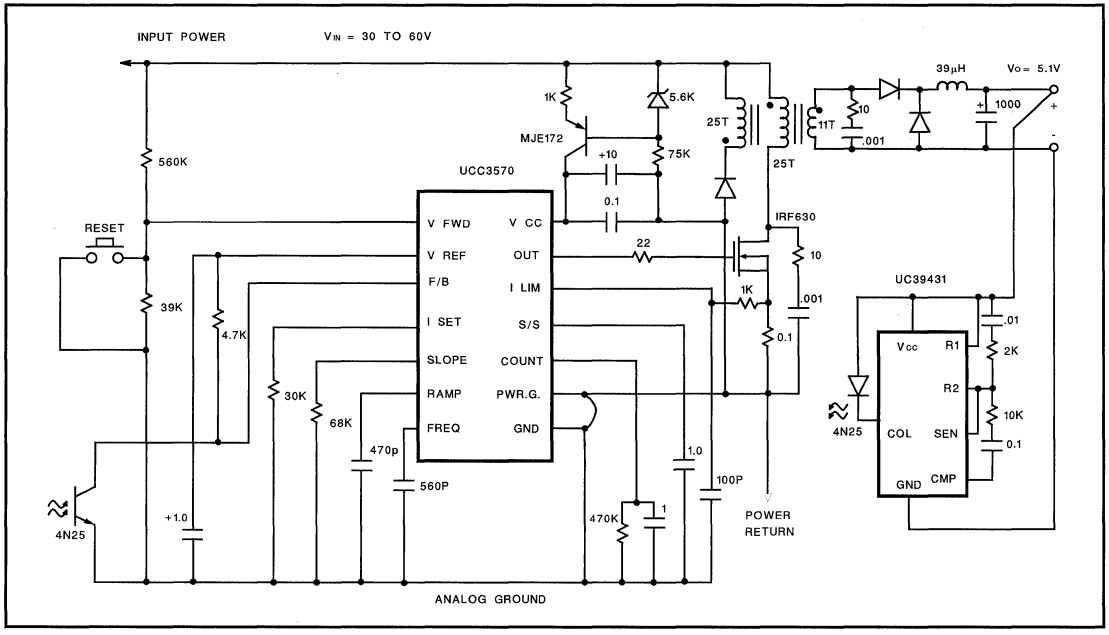

Figure 13. An isolated 25W, 48V to 5V converter including the UC39431 as an optocoupled feedback generator.

be accomplished with the two-transistor circuit shown in Figure 14. This circuit uses the energy in the soft-start capacitor to discharge the VCC capacitor which gives a turn-on delay equivalent to normal start up. The operation of this circuit is illustrated in Figure 15.

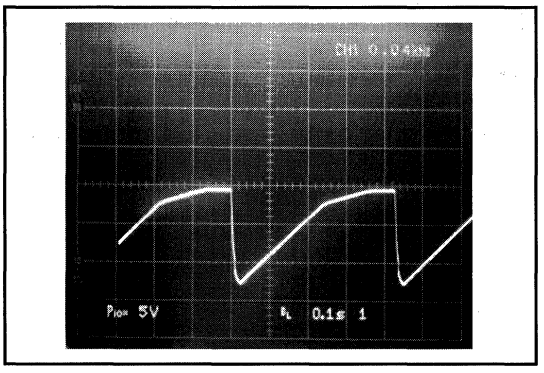

Figure 15. With auto re-start, a shorted output recycles VCC with a 0.4 second delay.

Another option for eliminating a latched shutdown is to simply short the COUNT pin to ground which will prevent activation of the Shutdown Latch unless the Current Limit threshold of 600mV is exceeded - an unlikely event considering the 80nsec response of the pulse-by-pulse current protection. Figure 16 shows operation in this mode with a continuous shorted output.

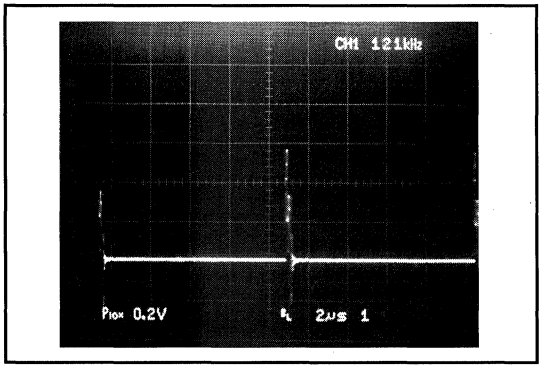

Figure 16. With the Fault Count function disabled, a shorted output reduces the current pulse width such that the peak across RCS remains below shutdown threshold.

This converter design illustrates another characteristic of the UCC3570 which provides both added safety and better utilization of the transformer magnetics. With an input voltage range specified as 30 to 60 Volts, If the OV clamp is set for 60V, the controller will continue to operate down to 15V (1/4 of 60V). However, if the maximum duty-cycle clamp is set for 50% at 30V, the ramp waveform will cause the output to skip pulses at voltages less than 30V insuring against saturation of the power transformer.

The rest of the circuit details for this application can be deduced from the information presented above and the complete schematic and parts list given in Appendix B (see page 12).

SUMMARY

With the minimal need for additional external components and support functions which these two quite different applications have shown, the versatility of the UCC3570 has been demonstrated. Not shown, but equally important is this device's ability to provide the same protection and programmability with power stages scaled up to several hundred Watts, and to efficiently operate at switching frequencies above 500kHz. Thus, once again it has been demonstrated that one can never close the door to "older" technologies and, in this case, revisiting voltage-mode control has yielded a new controller combining efficient operation, stable performance, and ease of application highly attuned to meeting today's stringent requirements for cost-effective power systems.

REFERENCES

Leu, Hua, Lee, and Zhou, "Analysis and Design of R-C-D Clamp Forward Converter" VPEC, Virginia Tech and Delta Power Electronics Lab, Blacksburg, VA.

ACKNOWLEDGMENTS

The author acknowledges and appreciates the help in the design of these examples provided by:

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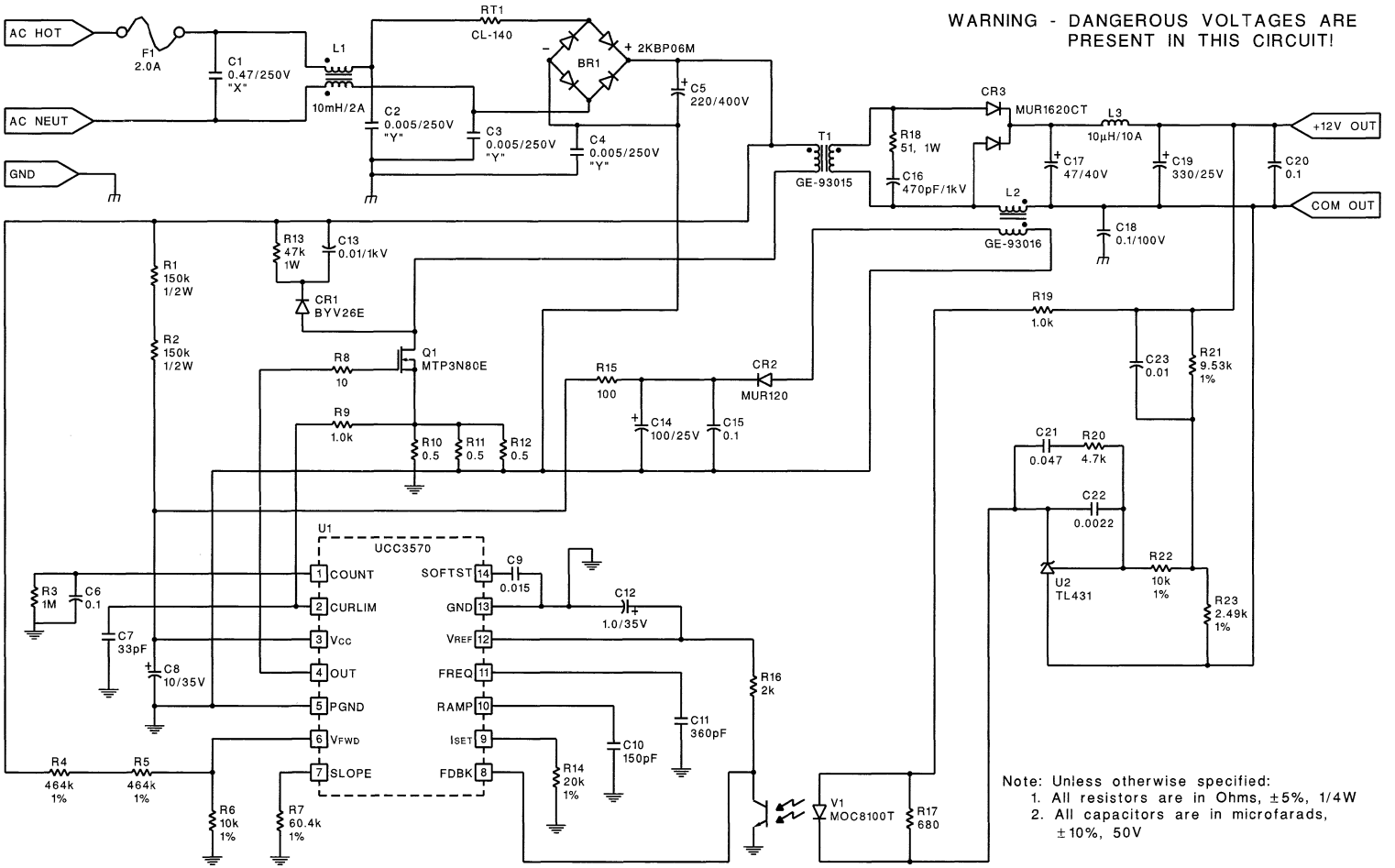
APPENDIX - A
12 VOLT, 50 WATT POWER SUPPLY

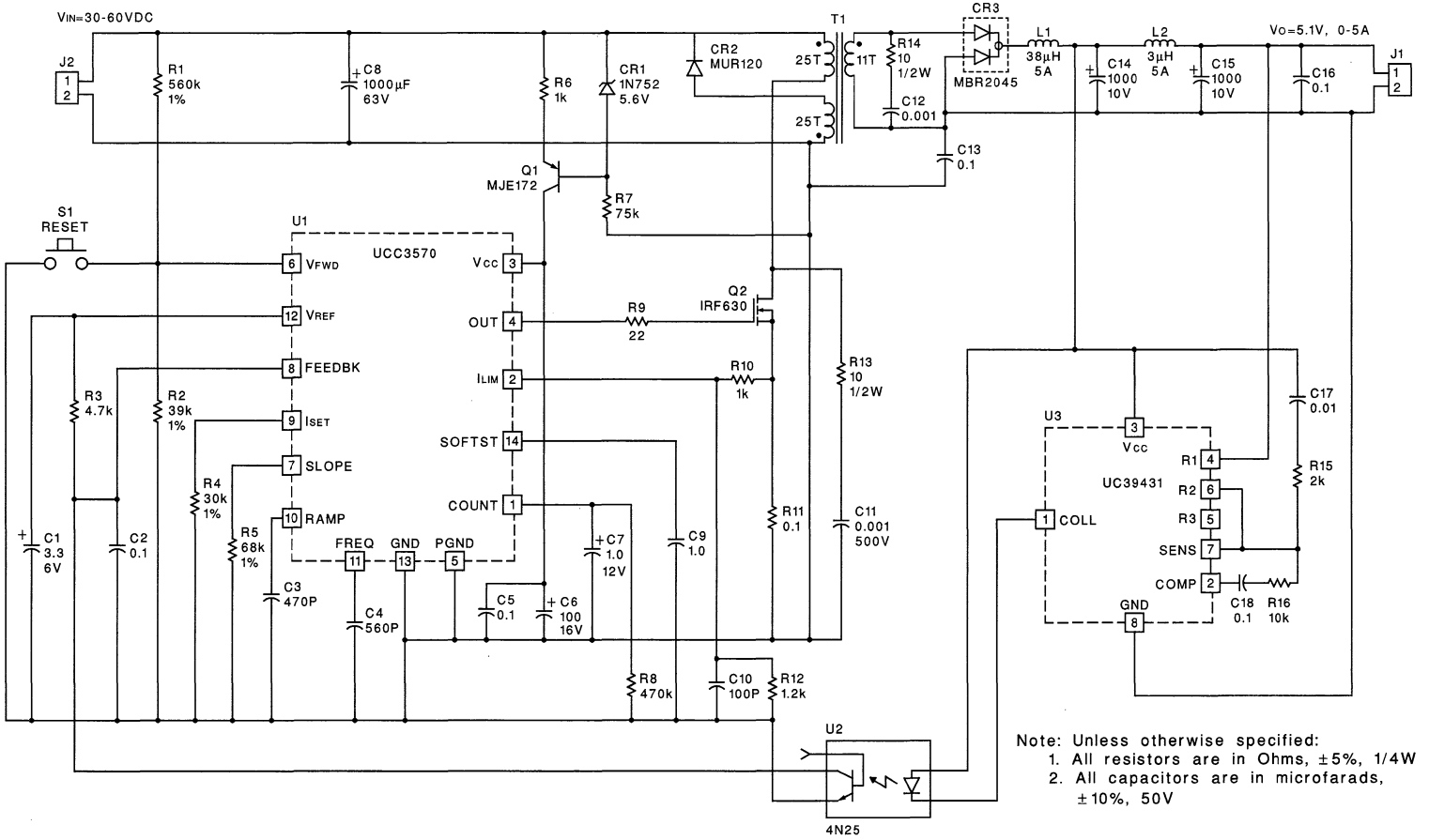


12 VOLT, 50 WATT POWER SUPPLY
BILL OF MATERIALS

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
1	1	BR1	2KBP06M	General Inst.
2	1	CR1	BYV26E	Philips
3	1	CR2	MUR120	Motorola
4	1	CR3	MUR1620CT	Motorola
5	1	Q1	MTP3N80E	Motorola
6	1	V1	MOC8100T	Motorola
7	1	U1	UCC3570N	Unitrode
8	1	U2	TL431	
9	1	T1	GE-93015	GFS Mfg.
10	1	L1	10mH/2A	Coilcraft
11	1	L2	GE-93016	GFS Mfg.
12	1	L3	10µH/10A	Coiltronics
13	1	F1	2.0A Fuse	
14	1	C1	0.47µF, 250V, "X"	Roederstein
15	1	C2	.005µF, 250V, "Y"	Roederstein
16	1	C3	.005µF, 250V, "Y"	Roederstein
17	1	C4	.005µF, 250V, "Y"	Roederstein
18	1	C5	220µF/400V	Panasonic
19	1	C6	0.1µF/50V	Polyester
20	1	C7	33pF/100V	Ceramic NPO
21	1	C8	10µF/35V	Solid Tantalum
22	1	C9	0.015/50V	Ceramic X7R
23	1	C10	150pF/100V	Ceramic NPO
24	1	C11	360pF/100V	Ceramic NPO
25	1	C12	1.0µF/35V	Solid Tantalum
26	1	C13	0.01µF/1kV	Ceramic X5F
27	1	C14	100µF/25V	Aluminum
28	1	C15	0.1µF/100V	Polyester

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
29	1	C16	470pF/1kV	Ceramic YSF
30	1	C17	47µF/40V	Aluminum
31	1	C18	0.1µF/100V	Polyester
32	2	C19	330µF/25V	Aluminum
33	1	C20	0.1µF/100V	Polyester
34	1	C21	0.047µF/100V	Ceramic X7R
35	1	C22	.0022µF/100V	Ceramic X7R
36	1	C23	0.01µF/100V	Ceramic X7R
37	1	RT1	CL-140	Keystone
38	2	R1, R2	150k, 1/2W	
39	1	R3	1M	
40	2	R4, R5	464k, 1%	RN55D
41	1	R6	10k, 1%	RN55D
42	1	R7	60.4k, 1%	RN55D
43	1	R8	10Ω	
44	1	R9	1.0k	
45	3	R10,11,12	0.5Ω	Carbon Film
46	1	R13	47k, 1W	
47	1	R14	20k, 1%	RN55D
48	1	R15	100Ω	
49	1	R16	2.0k	
50	1	R17	680Ω	
51	1	R18	51Ω, 1W	
52	1	R19	1.0k	
53	1	R20	4.7k	
54	1	R21	9.53k, 1%	RN55D
55	1	R22	10k, 1%	RN55D
56	1	R23	2.49k, 1%	RN55D

APPENDIX - B
48V - 5V, 20W DC/DC CONVERTER



Note: Unless otherwise specified:
1. All resistors are in Ohms, ±5%, 1/4W
2. All capacitors are in microfarads, ±10%, 50V

48V - 5V, 20W DC/DC CONVERTER
BILL OF MATERIALS

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
1	1	CR1	1N752, 5.6V	
2	1	CR2	MUR120	Motorola
3	1	CR3	MBR2045	Motorola
4	1	Q1	MJE172	Motorola
5	1	Q2	IRF630	Int. Rect.
6	1	U1	UCC3570	Unitrode
7	1	U2	4N25	
8	1	U3	UC39431	Unitrode
9	1	T1	Transformer	Custom
10	1	L1	38µH, 5A	Custom
11	1	L2	3µH, 5A	Toko
12	1	C1	3.3µF, 6V	Solid Tantalum
13	4	C2, 5, 16, 18	0.1	
14	1	C3	470pF	
15	1	C4	560pF	
16	1	C6	100µF, 16V	Solid Tantalum
17	1	C7	1.0µF, 12V	Solid Tantalum
18	1	C8	1000µF, 63V	
19	1	C9	1.0µF	
20	1	C10	100pF	

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
21	1	C11	.001µF, 500V	
22	1	C12	.001µF	
23	1	C13	0.1µF, 100V	
24	2	C14, 15	1000µF, 10V	
25	1	C17	.01µF	
26	1	R1	560k, 1%	
27	1	R2	39k, 1%	
28	1	R3	4.7k	
29	1	R4	30k,1%	
30	1	R5	68k, 1%	
31	1	R6	1.0k	
32	1	R7	75k	
33	1	R8	470k	
34	1	R9	22Ω	
35	1	R10	1.0k	
36	1	R11	0.1Ω	
37	1	R12	1.2k	
38	2	R13, 14	10Ω, 1/2W	
39	1	R15	2k	
40	1	R16	10k	

Magnetics Winding Information

T1:
Core: EI187-3C80 (Philips)
Primary: 25 Turns Bifilar = 26AWG
Reset: 25 Turns = 31AWG (Wound with Primary)
Secondary: 11 Turns Quadfilar = 25AWG

L1:
Core: T68-52D (Micrometals)
Winding: 21 Turns = 20AWG

L2:
Toko 262LYF-0077M

THE NEW UC3879 PHASE-SHIFTED PWM CONTROLLER SIMPLIFIES THE DESIGN OF ZERO VOLTAGE TRANSITION FULL-BRIDGE CONVERTERS

by Laszlo Balogh

INTRODUCTION

This Application Note will introduce the UC3879 integrated circuit and compare its performance to its predecessors, the UC3875/6/7/8 controller family. These integrated circuits provide all necessary control, decoding, protection and drive functions to successfully manage the operation of the full-bridge converter with phase-shifted control. This integrated solution greatly simplifies the design procedure and offers significant savings in development time and printed circuit board real-estate for the designer.

Using the conventional full-bridge topology with phase-shifted control technique has already demonstrated its superiority in medium to high power, DC-to-DC power conversion. This control method provides well controlled dv/dt values and zero-voltage switching of all primary side semiconductors in the power stage over nearly all operating conditions. Several publications [1-8] discussed the details of operation including equivalent circuits for the resonant transitions for both legs of the bridge converter, conditions for zero-voltage switching and describing further improvement possibilities. The major benefits offered by this approach are a simpler power stage than its hard switched counterpart, utilizing circuit parasitics instead of being penalized by them, improved efficiency and lower EMI level. These significant advantages are realized with a slightly more complex control algorithm.

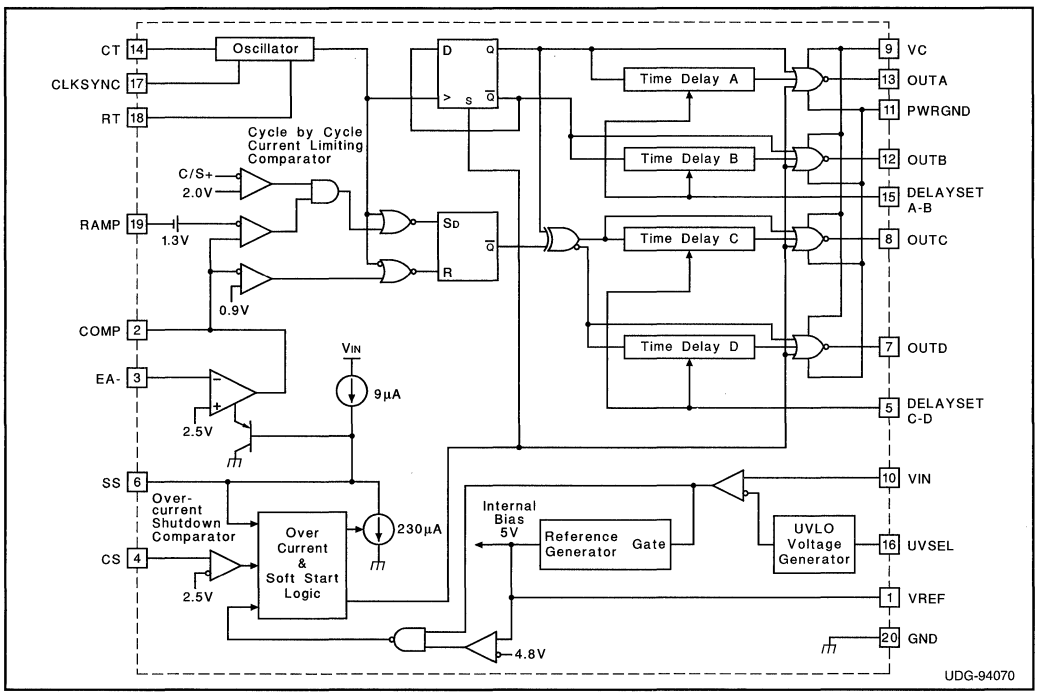


Figure 1. UC3879 Block Diagram

UNITRODE UC3879 PHASE-SHIFT PWM CONTROL IC - BLOCK DIAGRAM

The UC3879 is an improved version of the previously introduced UC3875 controller family. The internal architecture of the IC is shown in Figure 1.

The undervoltage lockout level of the UC3879 is user selectable by the UVSEL pin. Two predefined thresholds are available. If the UVSEL pin is floating, the chip starts running when the supply voltage exceeds 15.25V on the VIN pin. In case the UVSEL pin is externally connected to the VIN pin, operation starts at 10.75V. Independent of the selected start up option, the UC3879 goes to an undervoltage lockout mode when the input voltage falls below approximately 9.25V. The threshold levels reflect the two most commonly used auxiliary power generation methods; bootstrap or off-line.

The operating frequency of the synchronizable oscillator is programmed by two external components. The resistor from the RT pin to ground defines the charge current of the timing capacitor while the discharge current is internally fixed at 10mA. This way, the duty-cycle (D_{OSC}) of the oscillator, which corresponds to the duty ratio of the signal appearing on the CLKSYNC output of the IC, can be set accurately based on the relationship:

$$RT = \frac{2.5V}{0.01A \bullet D_{OSC}}$$

The minimum recommended pulse width for reliable operation is around 250nsec and for all practical applications it should not exceed 500nsec. Hence, D_{OSC} shall be determined based on the clock frequency as:

$$D_{OSC} = (250nsec...500nsec) \bullet f_{CLOCK}$$

The timing capacitor, connected between the CT pin and ground, in combination with the already defined RT value determines the clock frequency (f_{CLOCK}) by the following formula:

$$CT = \frac{(1 - D_{OSC})}{1.08 \bullet RT \bullet f_{CLOCK}}$$

In practice, the selection of proper capacitance values are much more difficult than those of the resistors. Therefore, one might first select the appropriate capacitor value to fulfill the requirement based on the following simple table:

Frequency Range	Capacitance
f_{CLOCK} < 30kHz	2.2nF
30kHz < f_{CLOCK} < 100kHz	680pF
100kHz < f_{CLOCK}	220pF

After choosing the value of the timing capacitor, the required resistance can be calculated as:

$$RT \cong \frac{0.47 + 0.07 \bullet \sqrt{47.17 - 5 \bullet 10^4 \bullet CT \bullet f_{CLOCK}}}{CT \bullet f_{CLOCK}}$$

Figure 2 shows the solution of the timing equations for the most commonly used frequency range. It offers a quick guide to estimate the required resistor value.

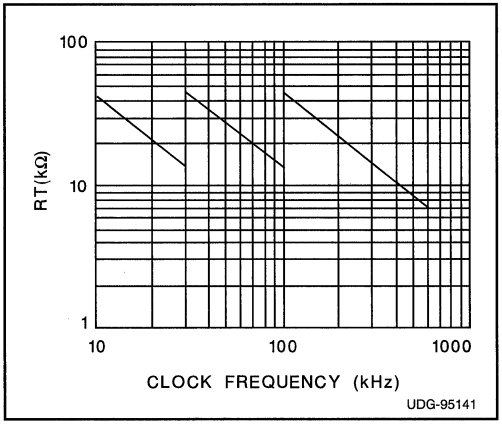


Figure 2. Timing Resistor (RT) vs. Oscillator Frequency

During free-running operation the capacitor voltage changes between nearly 0V and 2.9V linearly. Typical operating waveforms for free-running and synchronized operation are demonstrated in Figure 3.

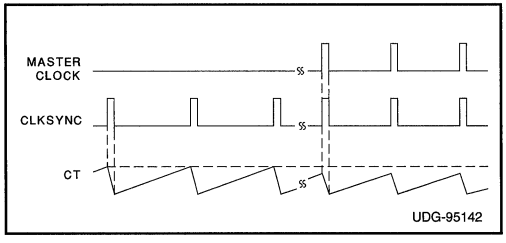


Figure 3. Oscillator Waveforms
a) Free-running; b) Synchronized Operation

Synchronization can be attained by driving the CLKSYNC pin from another UC3879 or by external circuitry as shown in Figure 4.

In both cases, all ICs will synchronize to the IC or external clock signal with the highest free-running frequency. The resistors R1 to Rn may be needed to properly terminate the synchronization bus and to keep the sync pulse narrow due to capacitance loading the line.

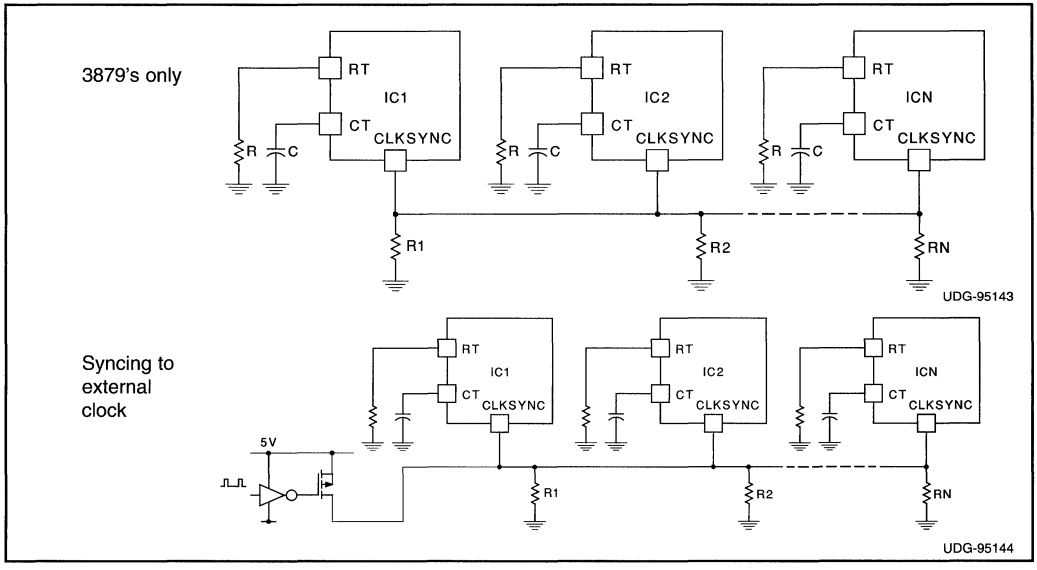


Figure 4. Typical Synchronization Schemes

An additional benefit of using local timing components for each individual oscillator is that it allows the synchronizing connections among the ICs to be broken without any local loss of functionality.

Output regulation is achieved using the 10MHz gain bandwidth on-board error amplifier. The noninverting input of the error amplifier is internally connected to a 2.5V reference. The inverting input (E/A–) and the output of the amplifier (E/A OUT) are accessible for feedback and compensation purposes. The output of the error amplifier is utilized to command the high speed PWM circuit. This signal is compared to the RAMP input of the IC having a usable input voltage range from zero to 2.9V.

Soft-start is accomplished with a capacitor from the soft-start pin (SS) to ground. During the soft-start period, the soft-start output of the error amplifier is clamped to the capacitor voltage which is gradually increased from zero to about 4.8V. It corresponds to pulse width, phase shift or peak current limiting

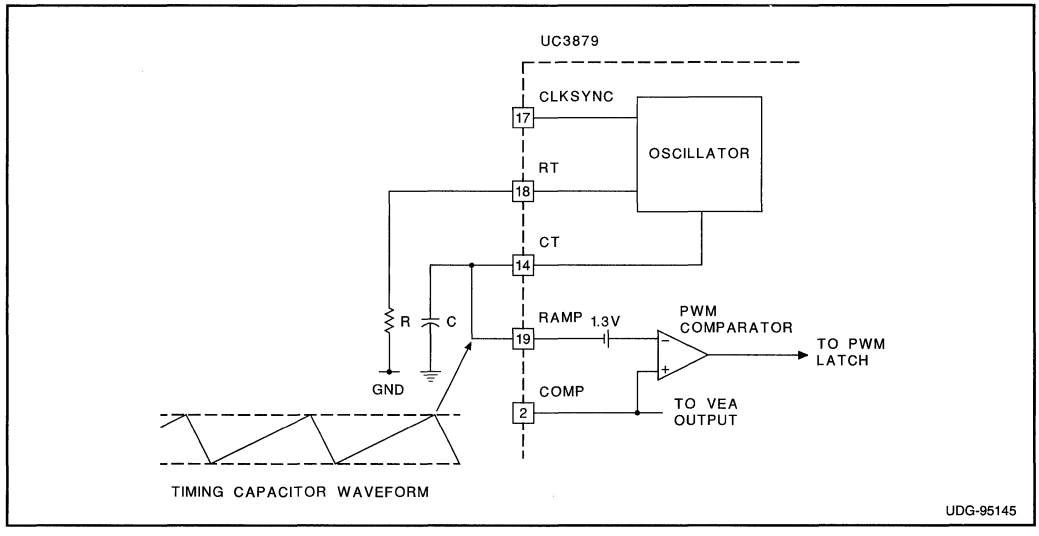


Figure 5. UC3879 with Voltage Mode Control

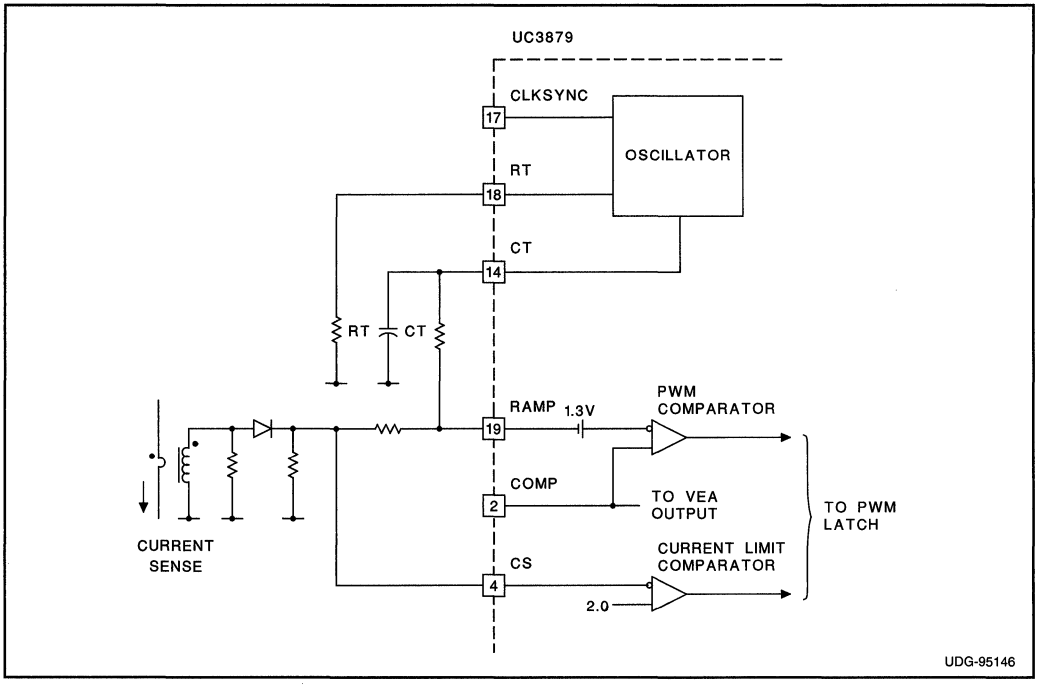


Figure 6. UC3879 with Peak Current Mode Control

depending on the exact implementation.

The UC3879 is equally suited for conventional voltage mode control or for peak current mode control. When used in voltage mode, the CT signal is directly fed to the RAMP terminal as indicated in Figure 5.

In current mode operation, the RAMP signal is the sum of the current sense signal and the slope compensation, derived from the voltage across the timing capacitor as it is shown in Figure 6.

Fault protection is established by two independent current limiting circuits which accept a 0V to 2.5V amplitude maximum current sense signal on their CS input pin. They provide cycle-by-cycle and shutdown type current limit protection in both voltage or

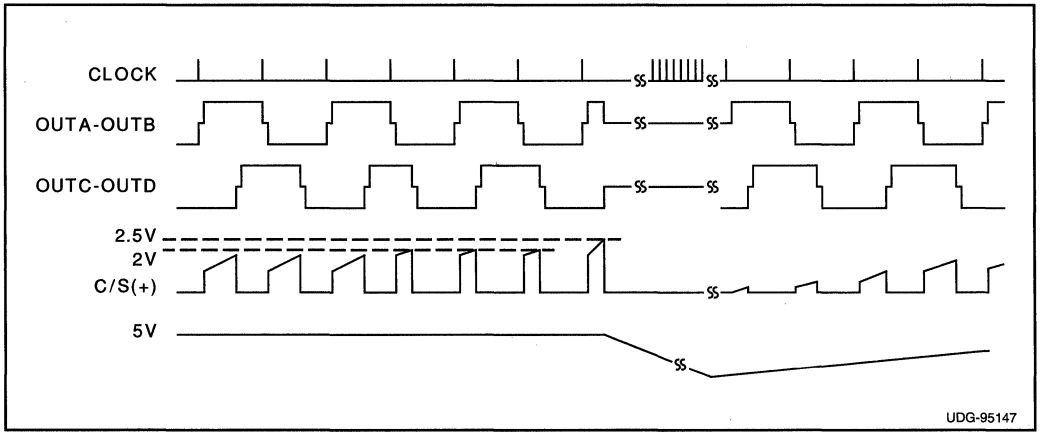


Figure 7. Operation of the Current Limiting Circuits (typical waveforms)

current mode operation. The characteristic waveforms are presented in Figure 7.

The fault protection circuits are inactive until the instantaneous voltage on the CS pin remains below the first threshold of 2V. When the signal on the CS pin exceeds 2V the existing output pulse is terminated. This first level of overload protection provides an effective defense mechanism to protect the primary side semiconductors against excessive current stress and to establish a rough input power limitation for the converter based on cycle-by-cycle current limit action.

At more severe overload conditions, this protection method is not adequate. For these cases, the UC3879 offers a second level of security. When the current sense signal on the CS pin would exceed, even momentarily, the 2.5V maximum value, the IC will initiate a full soft-start cycle to prevent catastrophic failure. If the load conditions do not change, hiccup mode will be established to reduce component stresses and to limit average power dissipation to a fail safe level.

The four totem pole OUTputs of the UC3879 can each deliver 100mA peak drive current. These outputs are intended to drive external gate drive circuits. This enhances the robustness of the overall design. To further reduce the noise transmitted back to the analog circuitry, the output section features its own collector power supply (VC) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply improves performance even more.

The steady state timing relations for the four outputs are shown in Figure 8.

Delays between the output drive commands to facilitate Zero Voltage Switching operation are programmed at the DELAYSET inputs. Delay time is determined by the current flowing from the delay set pin to ground through a resistor, R_{delay}. Timing accuracy will improve by using a current sink connected to the delay set pins in place of the resistors. The delay time can be calculated by the following equations:

$$t_{delay} = \frac{249.6 \cdot 10^{-12}}{I_{delay}} \text{ [sec.]}$$

where

$$I_{delay} = \frac{V_{delayset}}{R_{delay}};$$

$V_{delayset}$ = delay set pin voltage (2.4V typ.);

R_{delay} = resistor value from delay set pin to GND.

One unique feature of the UC3879 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different energy levels available for the resonant transitions of the leading and trailing legs of the bridge circuit [7-9]. Inability to optimize each of these durations will generally result in loosing zero voltage switching of the full-bridge converter switches under some operating conditions.

The optimum delay time, on the cycle-by-cycle basis, is the function of the actual current flowing in the primary winding of the transformer. This current

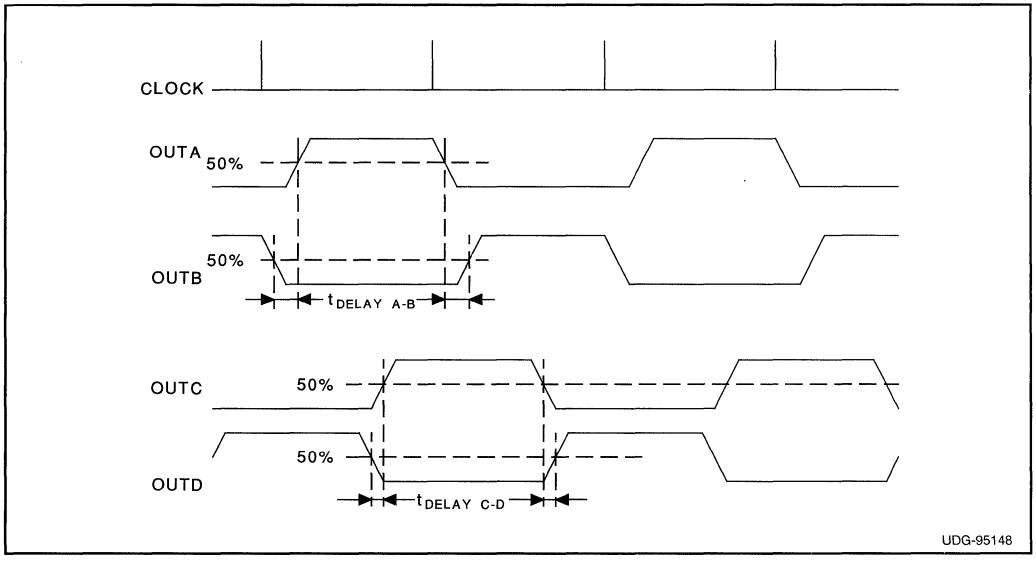


Figure 8. Output Timing Diagram for Steady State Operation

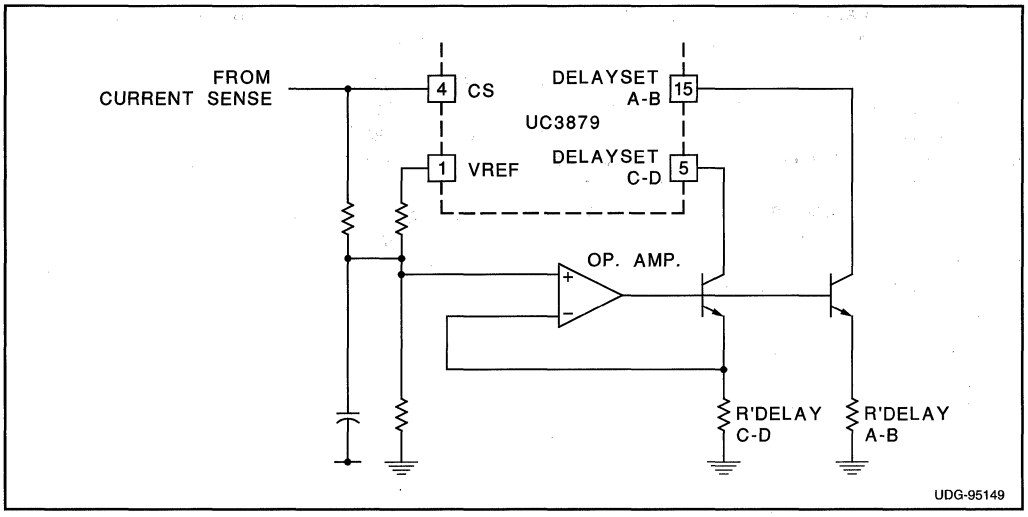


Figure 9. Adaptive Control of Delay Times

value can easily change by a factor of 10 to even 100 depending on load conditions. This causes a large variation in the required delay time, thus adaptive programming of delays might be desirable for certain applications.

Figure 9 introduces a simple external circuit to achieve variable delay times based on the momentary value of the sensed current.

The resistor network connected to the positive input of the operational amplifier determines the ratio of the minimum and the maximum delay times. The actual values of $t_{delayA-B}$ and $t_{delayC-D}$ can be scaled by the resistors between the emitters of the respective transistors and ground.

As these delays can be realized in several ways along the external gate drive circuits, setting zero delay is also offered by simply connecting the delay set inputs to the IC's 5.0V reference.

The precision, short circuit protected 5.0V bandgap reference is available for external functions as well.

UC3879 VS. UC3875/6/7/8

Although the UC3879 retained the operating principle and the basic architecture of the UC3875, it is still important to draw attention to the enhanced and added features of the new IC. The differences between the two controllers are summarized in Table 1. Their consequences for the circuit design will also be highlighted.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit utilizes a logic input (UVSEL) to select between the two available turn-on voltages (15.25V/10.75V). The advantage of this solution is that it can configure the undervoltage lockout threshold without external components. The UC3879 provides the same undervoltage lockout

Features	UC3875/6/7/8	UC3879
Undervoltage Lockout	Fixed at 15.25V/10.75V	Selectable
Supply Current	45mA typ.	27mA typ.
Oscillator Section	up to 2MHz operation	up to 600kHz operation
Error Amplifier	noninverting input accessible	noninverting input tied to 2.5V
Cycle-by-cycle Current Limiting	not available	implemented
Time Delay Circuits	60ns minimum delay	0 delay available
Output Drivers	4 x 2A totem-pole	4 x 100mA totem-pole

Table 1. Comparison of Unitrode's Phase-Shifted PWM Control ICs

levels that were offered by multiple part numbers in the UC3875/6/7/8 family.

SUPPLY CURRENT

The supply current demand (I_{IN}) of the UC3879 has been significantly reduced. While the startup current stayed the same, approximately 150µA, the operating supply current of the circuit decreased from 45mA to about 27mA. The gain was achieved by reducing internal bias currents. As a result, the maximum operating frequency has been lowered and the gate drive philosophy is revised. The UC3879 expects a high current gate drive device connected to its outputs opposed to the direct drive capability of the UC3875 family.

OSCILLATOR SECTION

The UC3879 features a completely redesigned oscillator circuit offering better noise immunity, temperature stability, and linearity. The charge current of the timing capacitor is constant, producing a linear, positive slope on the timing capacitor during the conduction period. The voltage level is tailored to provide ramp signal for voltage mode control directly. Likewise, slope compensation can be effortlessly accomplished using the voltage of the timing capacitor in case of peak current mode control. The operating frequency is programmed by the combination of RT and CT, which are connected to their separate pins.

ERROR AMPLIFIER

Both integrated circuits make use of a 10MHz gain bandwidth amplifier to regulate the output voltage. The noninverting input of the UC3879 error amplifier is internally wired to a 2.5V reference opposed to the UC3875 family where the reference is to be provided externally.

In constant output voltage applications, the UC3879 will save those components related to generating the reference for the feedback amplifier. Conversely, it will require more components and more elaborate solution if the programming of the output voltage, thus the reference, is required. Systems with isolation between the primary and secondary side controllers will not experience any difference in the design since the error amplifier of the control IC is usually configured as a voltage follower processing the error signal transmitted from the secondary side of the converter.

CYCLE-BY-CYCLE CURRENT LIMITING

This new feature is implemented only in the UC3879 controller. It provides exact, cycle-by-cycle current protection for the primary side switches during over-load conditions. The fast comparator utilized for cycle-by-cycle current limiting will terminate the active interval in every switching period when the current sense signal exceeds the internally set 2V reference value. This first level of overload protection is suitable to limit the maximum power to be handled by the power stage and will not result in a hiccup type of operation.

DELAY CIRCUITS

As previously described, the time between turning off one switch and turning on the other in the same leg of the bridge has a profound effect on circuit performance. Note that the programmed delay times should accommodate any delays introduced by the high current gate circuits and transformer.

Allowing zero delay between the outputs of the UC3879 provides greater freedom to the designer to implement those delays as desired. Possible other points to program the necessary delays are the inputs of the high current gate drivers or the secondary sides of the gate drive transformers. All these solutions have their pros and cons, and require careful considerations in sight of the actual application.

OUTPUT DRIVERS

The output totem pole drivers of both controllers have identical structures. They feature their own power rail connections and they are kept active low during undervoltage lockout. However, output current ratings are remarkably different. With its 2A peak current capability, the UC3875 family is prepared for direct drive of the gates or gate drive transformers of the most commonly used power switches. Yet, with the continuously increasing die sizes, separate driver chips can be advantageous to eliminate undesired power dissipation and noise generation from the sensitive analog control sections. In this regard, the UC3879 is designed to work with external high current gate drive circuits. Its fast outputs, with 100mA peak current capability, are especially appropriate to drive the TTL or MOSFET input stages of those devices.

Undervoltage Lockout		Delay Times		UC3879	UVSEL pin		DELAYSET pins	
Turn-ON	Turn-OFF	$\tau_D > 0$	$\tau_D = 0$	Old Part #	Float	$\rightarrow V_{CC}$	$\rightarrow V_{REF}$	R_{SET}
10.75V	9.25V	X		**UC3875**		X		X
15.25V	9.25V	X		**UC3876**	X			X
10.75V	9.25V		X	**UC3877**		X	X	
15.25V	9.25V		X	**UC3878**	X		X	

Table 2. Providing UC3875/6/7/8 functionality through the setup options of the UC3879 control IC.

UC3879 DESIGN FLEXIBILITY

Besides the several improved features and added functions, the UC3879 offers the greatest degree of design flexibility with the minimum number of external components. Table 2 shows the different setup possibilities to achieve the same functionality offered by four different part numbers in the UC3875 family.

SUMMARY

As demonstrated, the UC3875/6/7/8 and the UC3879 integrated circuits are dedicated to eliminate most of the difficulties associated with implementing the numerous auxiliary functions and the tedious control algorithm of the full bridge converters with phase-shifted control. The single chip solution with its carefully optimized signal levels and minimum number of external components provide the fast track in the controller design for one of today's most promising power conversion techniques.

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THE UC3886 PWM CONTROLLER USES AVERAGE CURRENT MODE CONTROL TO MEET THE TRANSIENT REGULATION PERFORMANCE OF HIGH END PROCESSORS

by Larry Spaziani
Applications Engineer

ABSTRACT

The continuing development of high performance processors is imposing stringent requirements on their respective power systems. Intel's Pentium®Pro power system specification, for instance, demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. To meet these requirements, the UC3886 Average Current Mode PWM Controller is introduced. This application note highlights the features of the UC3886 and details how this IC is ideal for creating the optimal switching regulator for low voltage processor applications.

UC3886 FEATURES AND BENEFITS

- Average Current Mode Control direct from a sense resistor
  - No slope compensation networks required
- High Gain-Bandwidth Amplifiers for a fast transient response
- Programmable Current Sense Amplifier
  - Interfaces to a low power sense resistor
  - Accurate Over Current Protection
- On-board Reference for Standalone operation
- Direct Drive for Buck regulator NMOS high side switch
  - Eliminates need for separate Driver IC

INTRODUCTION

The Intel Pentium®Pro microprocessor specifications underscore an ongoing trend in high end digital systems. Clock frequencies are increasing for improved throughput and the number of transistors is increasing as manufacturing technology improves. Power management both within the processor and power to the processor has been elevated to a significant architectural design consideration.

The consequence of these advances for the power system is requirements that strike fear in the most hardy power supply designers. Load current increases as the number of transistors and the clock frequency increase whereas operating voltage decreases to limit the power dissipation on the processor. Noise immunity decreases as well under these conditions resulting in much tighter regulation requirements. High efficiency must be maintained even though currents are increasing and output voltages are decreasing. Load current transients become exceedingly fast as the processor goes into and out of sleep modes of operation. Operating voltage is no longer a standard but must be programmable for variations from supplier to supplier, or even within a product line, such as with the Intel Pentium®Pro. Of course, simplicity must be maintained in order to keep parts count low and cost down.

The UC3886 Average Current Mode PWM Controller has been created to meet these requirements. The UC3886 is a full featured PWM controller which offers excellent performance, yet can be configured as a basic Buck regulator with a low external parts count. Excellent regulation accuracy can be realized through the high gain of Average Current Mode Control and by the very low offset voltage and current amplifiers used in the UC3886, which contribute negligible error to the output voltage. High efficiency is maintained by providing a direct drive to an efficient, low $R_{DS(ON)}$ N-MOSFET. A variable output voltage power supply can be controlled simply by supplying a command voltage to the UC3886 from a programmable reference, such as the UC3910 4-Bit DAC and Voltage Monitor IC.

The high gain of Average Current Mode control offers several advantages which help the designer to meet the regulation requirements of a widely varying load current as well as the extremely fast transient requirements. High current loop gain can be maintained at low operating currents with a regulator in continuous or discontinuous modes of operation. Average Current Mode control also allows optimal high bandwidth loop compensation which can maintain regulation during high current transients. The UC3886 obtains this current information from a low value resistor, and requires no transformers or slope compensation circuitry. The highly accurate current limiting of the UC3886 reduces the need to electrically and thermally overdesign the power components for short circuit fault considerations.

THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER IC

A block diagram of the UC3886 is shown in Figure 1.

The UC3886 Average Current Mode PWM Controller is ideally suited for a basic Buck regulator configuration, as shown in Figure 2, where a low processor voltage is generated from +5V typically. Appendix 1 provides a review of the operation of the typical Buck regulator shown in Figure 2.

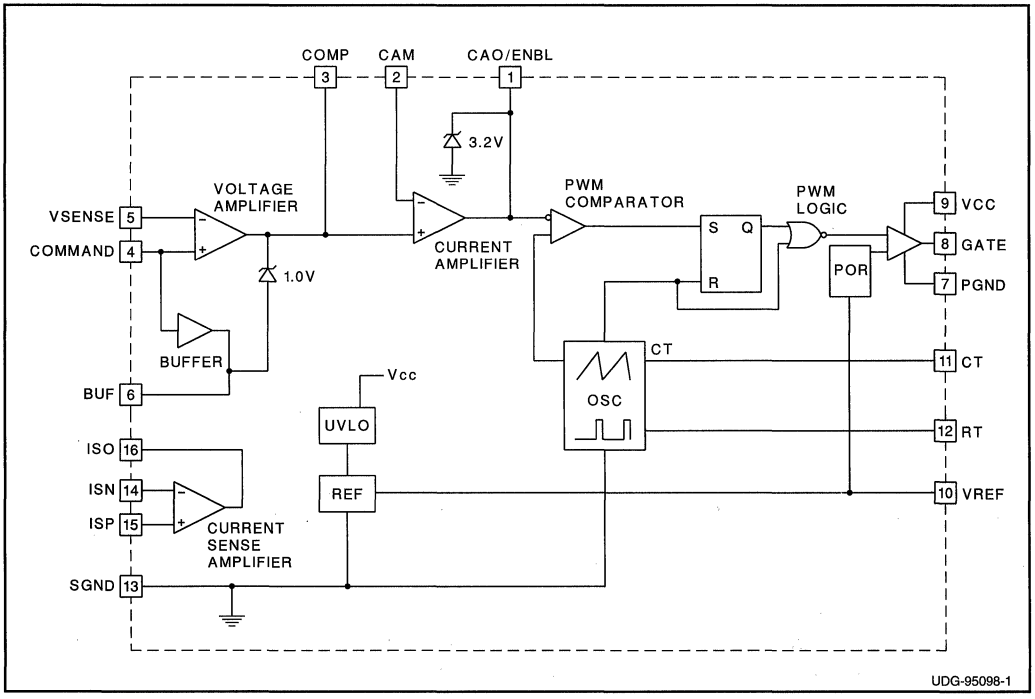

Figure 1. UC3886 Average Current Mode PWM Controller

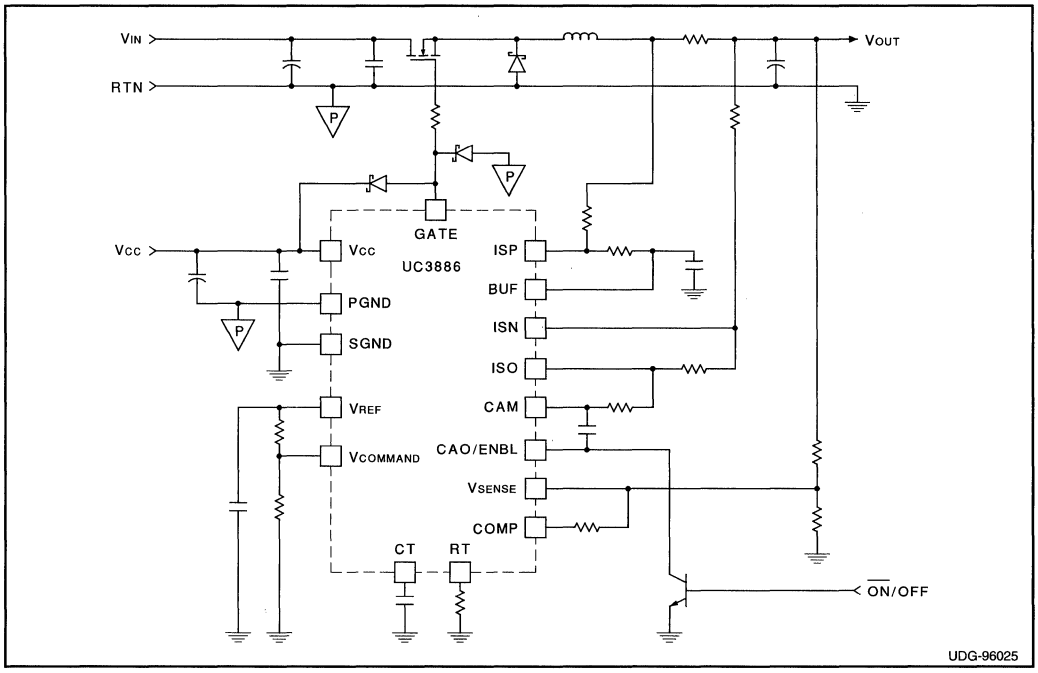

Figure 2. UC3886 Configured in a Typical Buck Regulator

UC3886 - SUPPLYING POWER

The UC3886 is constructed using a bipolar process allowing V_{CC} to be as high as 20V, however, the circuitry is optimized for a supply voltage of 12V. Minimum operating voltage is 10.3 volts. The supply voltage provides power directly to the reference voltage and the Gate Drive circuitry. It is also used to create an internal 7.3V bias voltage that supplies power to the Buffer, Voltage Amplifier, Current Amplifier, Current Sense Amplifier and the PWM comparator. The reference voltage is used to provide power directly to the PWM logic and to the Oscillator. Figure 3 shows the power distribution scheme within the UC3886.

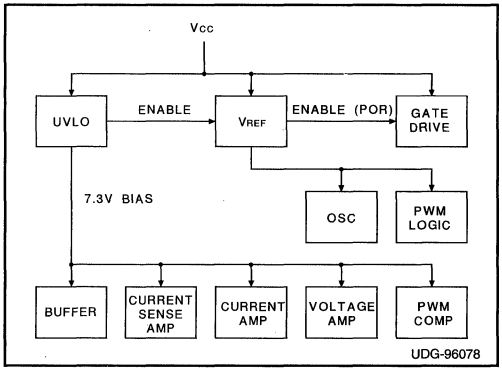

Figure 3. - Power Distribution within the UC3886

VCC should be decoupled to PGND closely to the IC with a low ESR capacitor to provide holdup during the gate pulses. Also add a 0.01µF to 0.1µF monolithic ceramic capacitor from VCC to SGND to provide high frequency signal decoupling.

UNDERVOLTAGE LOCKOUT

The UC3886 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 4 shows typical V_{CC} thresholds of the UC3886 UVLO circuitry.

During UVLO, V_{REF} is kept off, which disables the oscillator, the PWM logic, and the Gate Drive. The

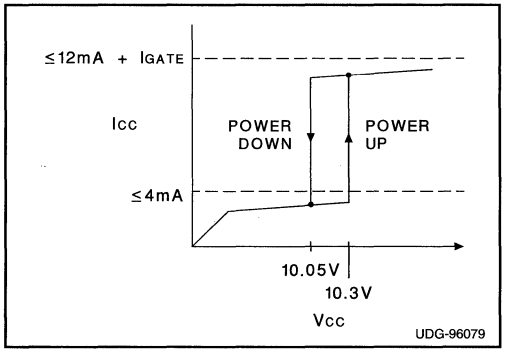

Figure 4. UC3886 UVLO Typical Values

buffers and amplifiers are also disabled. An internal signal called Power On Reset (POR) is created by monitoring the reference voltage, V_{REF}. The POR signal is held low until the reference voltage is high, at which time the Gate Drive output is enabled.

The total current drawn from the VCC source will include the IC supply current, I_{CC}, which provides bias power to the UC3886 as well as the average gate drive current, I_{GATE}, used to drive the N-channel MOSFET of the Buck regulator (see Appendix 2). The supply current is typically less than 4.0mA during UVLO and is typically less than 12mA (excluding gate drive current) when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}.

The 0.25V UVLO hysteresis prevents V_{CC} oscillations during the power up and power down sequences and also allows enough headroom for ripple voltage due to large gate drive current pulses.

Self Biasing, Active Low Output During UV Lockout

During UVLO, all chip functions are disabled in order to keep operating current at a minimum. The Gate Drive output, however, cannot be allowed to "float" high during this condition, because the Buck regulator N-channel MOSFET may inadvertently turn on.

An active low, self biasing totem-pole design is incorporated into the UC3886 Gate Drive output, which is very similar to that used in the UC3823A and is described in detail in U-128 [1]. The result of the self biased output is that during UVLO, the Gate Drive output is held low without drawing power from the supply voltage. No supply current is drawn because the self biasing output derives its power from the MOSFET gate voltage which is attempting to rise. This feature also negates the need for a gate-to-source resistor to keep the N-channel MOSFET biased off.

VREF

The UC3886 contains a 5.0V trimmed bandgap reference, similar to that used on many other Unitrode ICs. Figure 5 shows how the reference voltage, V_{REF}, can be used to create a Buck regulator command voltage ($V_{COMMAND}$) at the non-inverting input to the error amplifier, which sets the output voltage of the Buck regulator.

VREF can also be used to bias external circuitry, such as logic pull-ups and bias currents, so long as the total load current does not exceed 2.0mA. Short circuit protection on VREF protects the IC at a minimum of 10mA. A 0.01µF to 0.1µF monlithic ceramic decoupling capacitor from VREF to SGND should be located close to the IC.

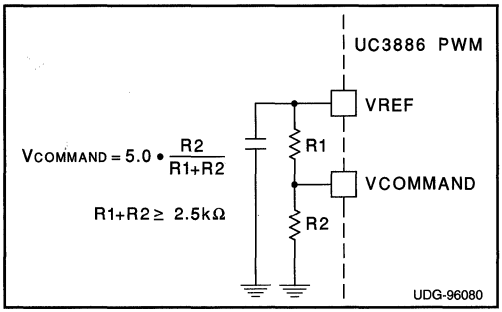

Figure 5. Setting VCOMMAND using VREF

HIGH POWER GATE DRIVE OUTPUT

The UC3886 features a single totem-pole output capable of directly driving an N-channel MOSFET and is similar to that of the UC3823A PWM IC. It features a 1.5A peak, 200mA average drive stage, ample capability to drive a size 6 FET [2] at several hundred kiloHertz.

The circuit of Figure 6 illustrates how the UC3886 Gate signal is used to drive a MOSFET for a low output voltage BUCK regulator.

Grounding with PGND and SGND

The PGND pin is a dedicated ground pin for the UC3886 output drive stage. The UC3886 Gate signal provides the high current gate pulses required during the MOSFET turn-on and turn-off times. These high current pulses should be decoupled by a low ESR capacitor placed closely to the IC as shown in Figure 6.

The current path for the gate pulses originates from the decoupling capacitor, passes through the totem-pole output of the UC3886 and enters the MOSFET gate. In a Buck regulator configuration, the inductor blocks the gate drive current, and therefore the gate current pulses exit the MOSFET DRAIN. The input capacitors decouple the gate current to ground and back to the V_{CC} decoupling capacitor, completing the loop. The PGND pin should be connected with the shortest possible path to power stage ground, to minimize loop inductance.

The SGND pin of the UC3886 is the reference voltage for all internal circuitry other than the output stage. SGND should have a direct path to the circuit ground, as shown in Figure 6, and should NOT be grounded at the PWM to PGND, since the gate pulses will result in some dv/dt in the PGND path. Differential voltage between SGND and PGND should not exceed 50mV.

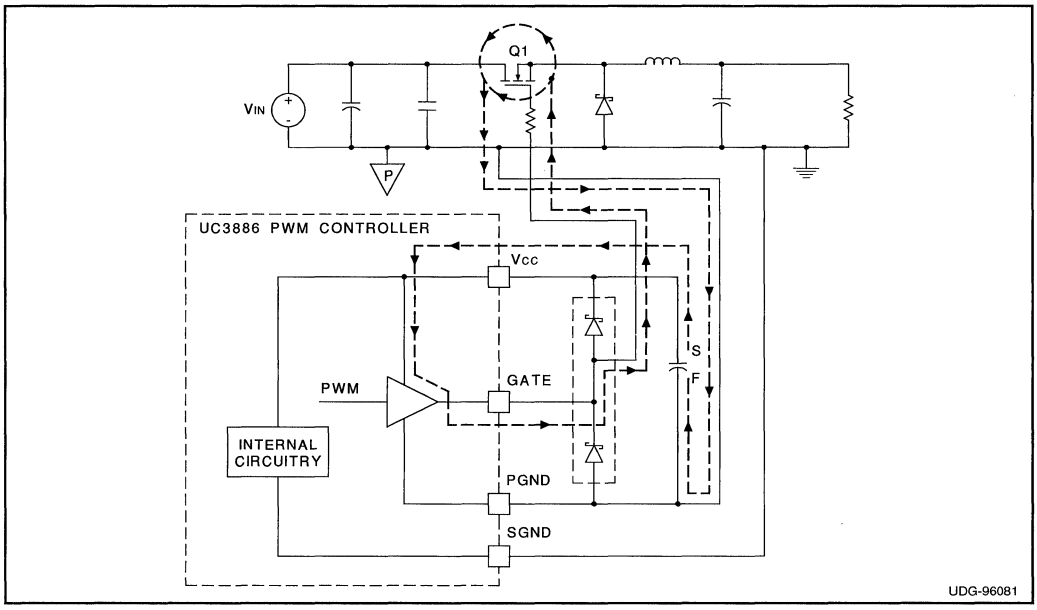

Figure 6. Driving a BUCK MOSFET with the UC3886

Schottky Clamping Diodes

The high di/dt characteristics of the gate drive pulse can cause undesirable ringing in the gate circuit, due to circuit trace inductance. A detailed explanation of why this occurs is available in Unitrode Application Note U-111 [2].

The use of low voltage schottky clamps, as shown in Figure 6, will protect the circuit from these effects. Use of 1N5821, 3A schottky diodes is recommended. The UC3612 is a dual schottky diode made specifically for this purpose and is available in an 8-pin DIP or SOIC package.

OSCILLATOR

The UC3886 oscillator is a sawtooth oscillator that is externally programmable (R_T, C_T) as shown in Figure 7. The oscillator switching period, T_S, consists of a charge time, T_C, and a discharge time or deadtime, T_D, such that

$$T_S = T_C + T_D \text{ [seconds]}$$

as shown in sawtooth waveform of Figure 7.

Oscillator equations presented below use the following units:

Resistance in ohms
Capacitance in farads
Currents in amperes
Time in seconds
Frequency in Hertz

The oscillator switching frequency, F_S, is given by

$$F_S = \frac{1}{T_S}$$

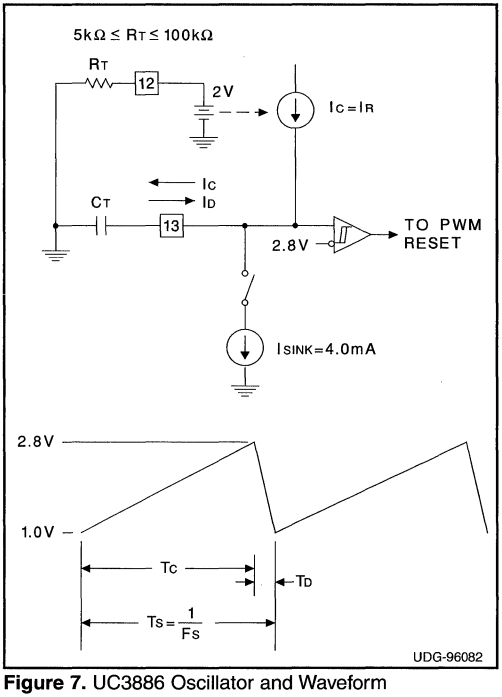

Figure 7. UC3886 Oscillator and Waveform

The sawtooth waveform charging current is programmed by the value of R_T. R_T should be a minimum of 5kW and a maximum of 100kW. Values of R_T outside this range will result in nonlinearity and are not recommended. The charge time is defined as the amount of time it takes the charge current to linearly charge C_T from 1.0V to 2.8V (DV = 1.8V), and is given by

$$T_C = \frac{C_T \bullet 1.8V}{(2.0V/R_T)}$$

The charge current is not switched off at the end of the charge time. The discharge current is therefore equal to

$$I_D = I_{SINK} - I_C = I_{SINK} - \frac{2.0V}{R_T}$$

where I_{SINK} is set internally in the UC3886 to 4.0mA.

The dead time is determined by

$$T_D = \frac{C_T \bullet 1.8V}{4.0mA - (2.0V/R_T)}$$

Programming the Oscillator

The first step in programming the oscillator is to choose a maximum operating duty cycle, D_{MAX}, given by

$$D_{MAX} = \frac{T_C}{T_C + T_D} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)}$$

D_{MAX} is programmable from 90% to 100%. Although a typical Buck regulator may only operate at 60% to 70% in steady state conditions, during a large transient load step condition, a higher duty cycle is required to "build" the inductor current. Programming D_{MAX} below 90% is not recommended. Figure 8 shows Dmax as a function of the timing resistor, R_T.

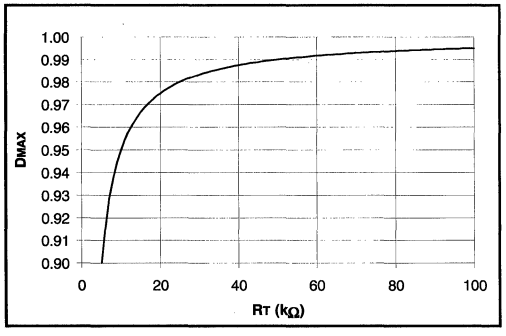

Figure 8. Programming Maximum Duty Cycle with R_T

The oscillator (switching) frequency can be programmed once the value of R_T is determined. The oscillator frequency is given by

$$F_S = \frac{2.0V \bullet [(4.0mA \bullet R_T) - 2.0V]}{C_T \bullet 1.8V \bullet R_T^2 \bullet 4.0mA}$$

which is plotted for several standard capacitor values in Figure 9.

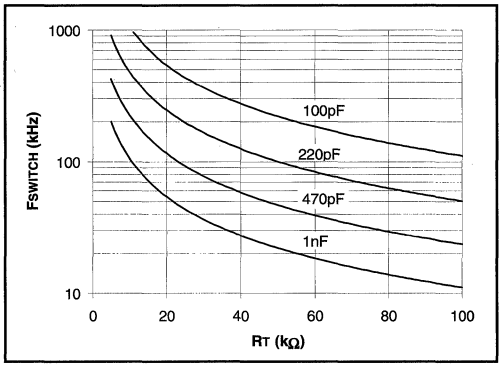

Figure 9. Programming Switching Frequency with C_T

Programming the oscillator frequency above 300kHz should be made with consideration for the Average Current Mode control amplifiers of the UC3886, which have an optimal Gain-Bandwidth product for operation below 300kHz.

The deadtime is plotted in Figure 10 as a function of R_T and C_T.

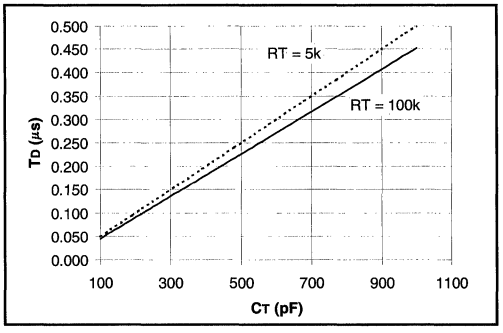

Figure 10. Deadtime vs C_T, R_T

Synchronizing the UC3886

Synchronizing the UC3886 can be achieved by superimposing a narrow voltage pulse on the PWM Ramp signal, as shown in Figure 11. The UC3886 oscillator should be programmed to freerun approximately 15% lower than that of the synchronizing frequency. A 1.0V amplitude pulse with a rise time of £ 10ns and a duration between 10ns and $T_D/2$ is recommended. Note that when synchronized, the dead time is the sum of the synchronizing pulse width and the oscillator discharge time. An excessively wide synchronizing pulse will result in less usable duty cycle, which may be required for large signal response. A very slow rising edge on the syn-

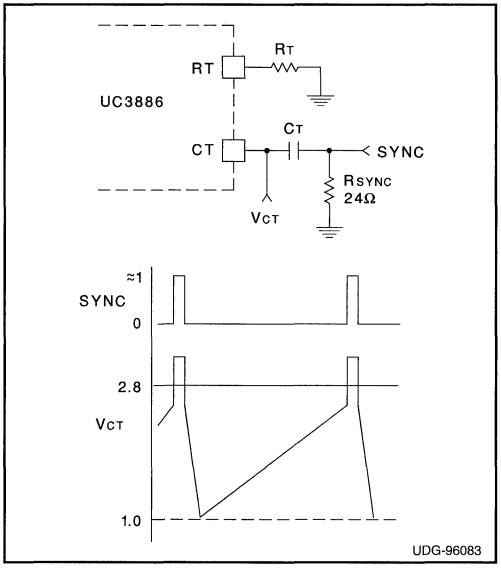

Figure 11. Synchronizing the UC3886

chronizing pulse should be avoided as well, as the PWM gain may be reduced.

Details of PWM oscillator operation, waveforms and synchronization is covered extensively in U-111 [2]. Synchronizing multiple UC3886 PWM controllers can be implemented using the UC3803 circuit as detailed in U-133A [3].

UC3886 - AVERAGE CURRENT MODE CIRCUIT BLOCK DESCRIPTION

The UC3886 Average Current Mode circuit blocks consist of the Voltage Amplifier, Buffer, Current Sense Amplifier, Current Amplifier and PWM Comparator. These blocks are shown in Figure 12 configured for Average Current Mode control in a Buck regulator.

The Dynamics of Average Current Mode Control with the UC3886

An understanding of the dynamics of Average Current Mode control as shown in Figure 12 is necessary to better understand the individual blocks which make up the system.

A simple but important fact must be understood up front; the ***load*** current of the Buck regulator is not the same as the ***inductor*** current of the Buck regulator. The ***load*** current is made up of the ***inductor*** current plus the current from the output capacitance. Average current mode control programs the ***inductor*** current. This is especially important when considering transient behavior and the dynamics involved.

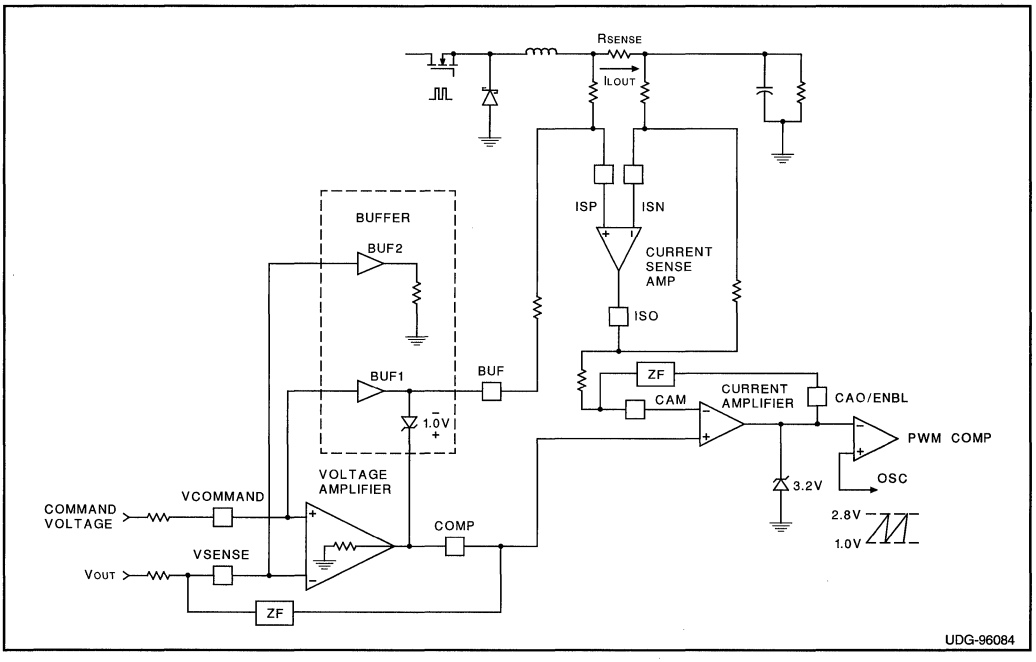

Figure 12. Configuring the UC3886 in Average Current Mode Control

The purpose of Average Current Mode Control is to program the Buck regulator (output inductor) to supply an average current to the load, such that the proper output voltage is maintained. The proper output voltage is programmed by the VCOMMAND pin on the UC3886.

A change in the load current of the Buck regulator will change the output voltage incrementally, which in turn will change the output of the Voltage Amplifier, COMP. Changing COMP will change the output of the Current Amplifier, CAO/ENBL, which is a direct input to the PWM comparator. Duty cycle will change as a result of CAO/ENBL changing. Note that at this point, the average inductor current has not changed yet, only the LOAD current. This means that until this point, the output capacitor has supplied the change in load current.

A duty cycle change will cause the average current to change through the inductor. The inductor current is converted to a voltage signal by the sense resistor, and is then amplified by the Current Sense Amplifier and is seen at the inverting input of the Current Amplifier, CAM. When the amplified current signal of the Current Amplifier's non-inverting input is equal to the COMP pin, the circuit settles into a steady state condition, where the average current into the load results in the proper output voltage.

BUFFER

The UC3886 Buffer block performs three functions:

- Buffers VCOMMAND to create a bias voltage for the Current Sense Amplifier output ISO.
- Clamps the COMP output of the Voltage Amplifier to:
  - 1.0 volt above the command voltage for use in current limiting.
  - 0.7 volts below the command voltage to limit large signal swing.
- Buffers V_{SENSE} for the sole purpose of minimizing the offset voltage at the Voltage Amplifier (BUF2 in Figure 12).

The Buffer has a gain accuracy of 1.0 ±0.05 V/V. A decoupling capacitor of 0.1µF located close to the IC is recommended in order to reduce noise in the current loop and to insure the unity gain stability of the Buffer.

VOLTAGE AMPLIFIER

The UC3886 Voltage Amplifier is used to create an error voltage based on the difference between the non-inverting (VCOMMAND) and inverting (VSENSE) inputs to the Voltage Amplifier. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB.

The Voltage Amplifier is optimized to provide excellent DC accuracy in a closed loop system by providing low offset voltage (±2.0mV) and very low input offset current (±0.01uA). The second buffer, BUF2, which buffers the VSENSE line, also improves DC accuracy by insuring that its bias current is closely matched to the bias current of BUF1 (i.e., very low offset current between BUF1 and BUF2). By matching the impedances at the Voltage Amplifier inputs, as shown in Figure 13, the low Voltage Amplifier and Buffer bias currents will cancel, minimizing DC error. Reducing the values of the resistors will minimize this small offset error.

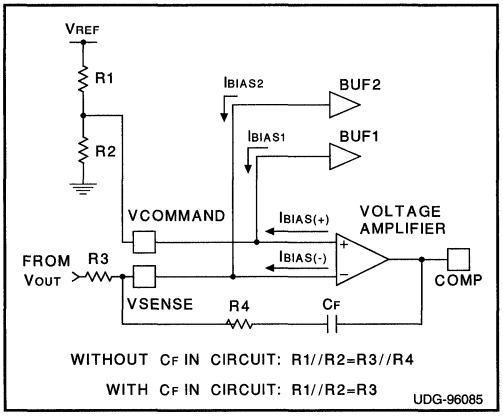

Figure 13. Minimizing DC Offsets at the Voltage Amplifier

The Voltage Amplifier is also optimized for large signal transient performance. A large signal (step) load change in a Buck regulator will result in a rapidly changing output voltage, which in turn will cause the Voltage Amplifier's output (COMP) to change. The COMP pin is clamped by the buffer to V_{BUF} +1.0V on the high side and to V_{BUF} -0.7V on the low side, where V_{BUF} is the voltage at the BUF pin. This insures that large signal transitions at the COMP pin will be limited to just outside its steady state control range (V_{BUF} to V_{BUF} +1.0V). Feedback capacitors will not have to be charged up and discharged from "rail to rail", and therefore the Voltage Amplifier will react much more quickly to transients, reducing reaction time and overshoot. Using low feedback capacitance will allow the Voltage Amplifier to rapidly slew from one level to another, insuring excellent transient response.

The use of non-integrating feedback around the Voltage Amplifier can optimize the transient performance of a converter by minimizing the amount of

capacitance on the COMP pin, and by intentionally limiting DC voltage regulation. Non-integrating compensation is discussed in Appendix 3.

CURRENT SENSE AMPLIFIER

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, R_{SENSE}. It features a 2.5MHz Gain-Bandwidth product and an open loop gain of 85dB. This amplifier must be set up as a differential amplifier as shown in Figure 14. A differential amplifier configuration will amplify only the difference voltage across the sense resistor, R_{SENSE}, and will not amplify or carry common-mode information.

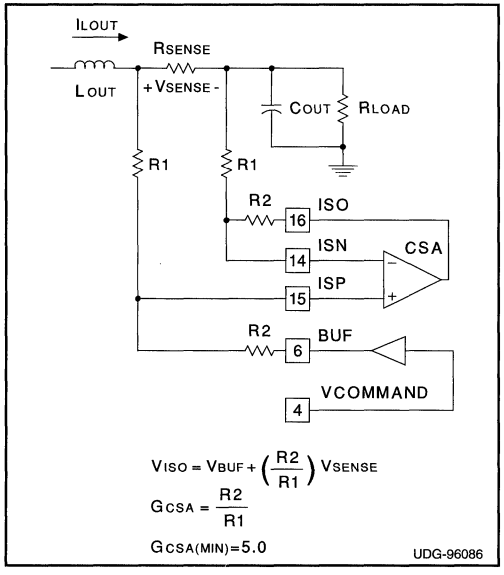

Figure 14 . Configuring the Current Sense Amplifier of the UC3886

The Current Sense Amplifier gain must be programmed (by external resistors) to be greater than or equal to 5.0 (14dB), as this amplifier ***is not stable*** with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore, the gain of the Current Sense Amplifier, G_{CSA}, must be programmed between

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX} = 2.5MHz/F_{SWITCH}$$

where F_{SWITCH} is the oscillator switching frequency.

Equations governing a Differential Amplifier are contained in Appendix 4.

R_{SENSE}, the current sense resistor, is used to measure the output inductor current, which is necessary for the proper operation of Average Current Mode Control. The Current Sense Amplifier features a common mode input range from 0.0 to 4.5Vdc. This allows the current sense resistor to be placed directly in series after the output inductor in low output voltage converters.

R_{SENSE} should not be placed before the output inductor because the current sense signal will be outside the common mode range of the Current Sense Amplifier. Likewise, R_{SENSE} should not be placed in the return path unless a ground difference can exist between the UC3886 and the load, which may be detrimental to voltage regulation. Figure 15 illustrates these points.

CURRENT AMPLIFIER AND PWM COMPARATOR

The Current Amplifier is used to create a current error voltage based on the difference between the amplified inductor current and the Voltage Amplifier output, COMP. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB. Using an integrating feedback compensating network around the Current Amplifier presents two advantages of Average Current Mode control over Peak Current Mode Control [4]. Higher DC gain is the first advantage. The second is the ability to compensate the loop, whereas Peak Current Mode Control has a fixed gain.

The output of the Current Amplifier, CAO/ENBL, is compared to the PWM ramp with the result being a duty cycle varying as a function of the inductor current and the commanded voltage. Ideal PWM comparator waveforms are shown in Figure 16. By observing the waveforms of Figure 16, the noise immunity advantage of Average Current Mode control over Peak Current Mode control can be seen. At the beginning of each switching cycle, the Ramp signal is at its lowest point, and therefore the PWM comparator is less susceptible to turn on spikes. Also, since an Average Current Mode control system samples the Inductor current, and not the switch current, there are no parasitic turn on spikes to compensate for or filter.

The Current Amplifier output, CAO/ENBL, is compared to the ramp waveform generated at the timing capacitor, C_T, at the high speed PWM Comparator. The ramp waveform is a fixed frequency ramp ranging from 1.0V to 2.8V. Figure 16 shows that the output of the Current Amplifier is clamped to approximately 3.2V, which is above the steady state range of the PWM comparator (2.8V). Large signal transient conditions may cause the Current Amplifier output to swing high and clamp to this upper limit. Clamping the Current Amplifier output allows a fast transient response, as the feedback

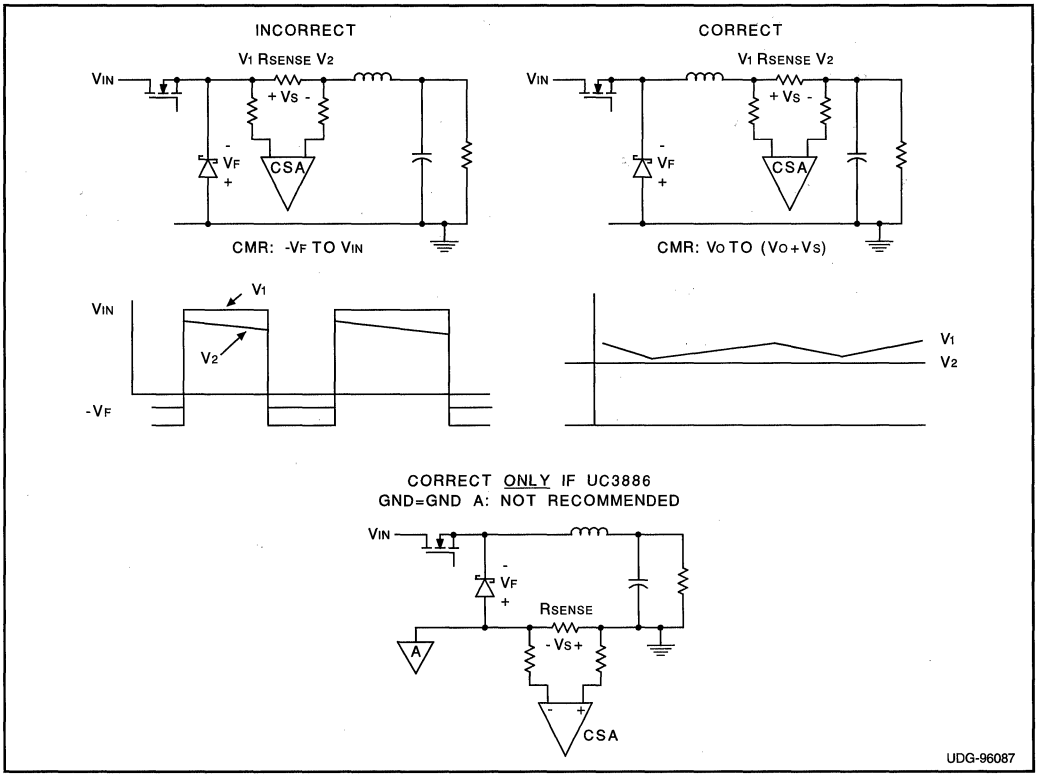

Figure 15. Sense Current AFTER the Inductor to Insure the Signal is within the Current Sense Amplifier's Common Mode Range

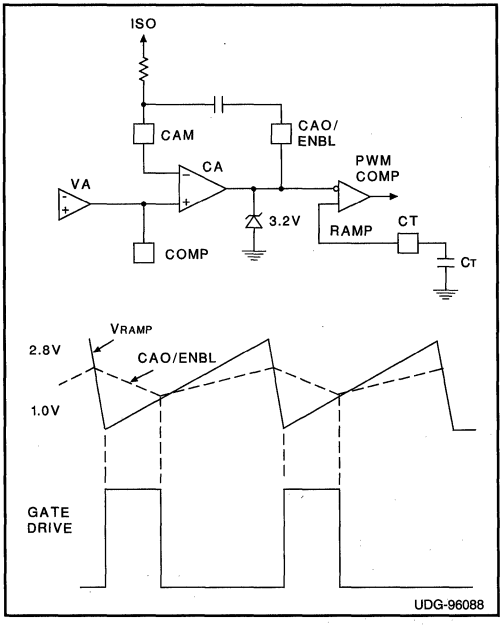

Figure 16. The Current Amplifier Output is compared to the PWM Ramp Signal

capacitors do not swing over a large voltage range and cause substantial transient overshoots or delays.

Disabling the UC3886 Gate Output with CAO/ENBL

The UC3886 can be disabled by bringing the CAO/ENBL pin below 0.8V, as shown in Figure 17. The CAO/ENBL pin is one input to the PWM comparator, and the oscillator ramp waveform is the other. Bringing the CAO/ENBL pin below 0.8V will force the Gate Drive duty cycle to 0%.

The CAO/ENBL is the output of the Current Amplifier and will be compensated for loop control. The signal to the CAO/ENBL pin must therefore be a true open collector so that during the HIGH (open) state, there is no effect on the amplifier's performance. The open collector signal must be capable of sinking [3] 250µA and remain below 0.8V. Figure 17 shows R1 which is recommended if the enable signal is located at a significant distance from the power supply. A long circuit board signal run can couple noise into the current loop if it resides close to noisy signals. R1 acts as a high impedance block to noise signals. R1 should be

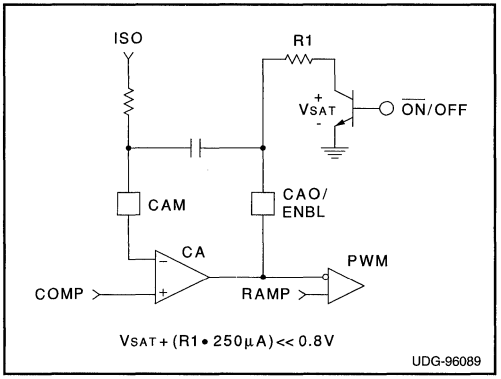

Figure 17. Disabling the UC3886

small enough however to insure that the disabling signal at CAO/ENBL is less than 0.8V. A 1kW resistor is recommended.

No features of the UC3886 are powered down during the disabled output state other than the Gate Drive output.

CLOSING THE LOOP WITH AVERAGE CURRENT MODE CONTROL

The fundamental principles of Average Current Mode Control are presented in Unitrode Application Note U-140 [4]. Compensating both the current loop and voltage loop is further detailed in Unitrode Seminar Topic "Switching Power Supply Control Loop Design" [5].

Figure 18 is a modification of the models presented in the two referenced application notes where the addition of the Current Sense Amplifier is the fundamental change.

Closing the Loop in a Variable Output Power Supply

The above mentioned references on closing the loop using Average Current Mode control show a critical limitation on the inductor current slope during the switch OFF time. A variable output power supply must consider the maximum operating output voltage, where the inductor current OFF time slope is maximized. The result will be less than optimal gain at the lower operating voltages.

CURRENT LIMITING WITH THE UC3886

The output of the Current Sense Amplifier, ISO, is determined by the differential gain equation (see Appendix 4) and is biased by the voltage at the BUF pin, V_{BUF}, as shown in Figure 14, such that

$$ISO = V_{BUF} + V_{SENSE} \bullet G_{CSA} \text{ [Volts]}$$

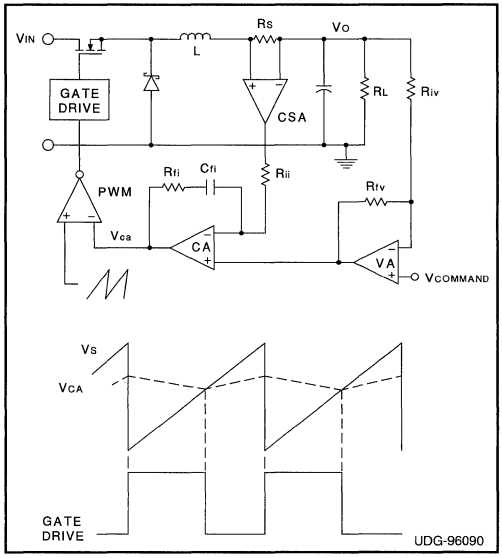

Figure 18. Average Current Mode Control Circuit and Waveforms for the UC3886 ACM Controller

where

$$V_{SENSE} = I_{LOUT} \bullet R_{SENSE} \text{ and}$$

$$G_{CSA} = \frac{R2}{R1} \text{ as shown in Figure 14.}$$

An increase in load current will force the power supply output voltage to decrease as the output capacitor discharges. This will force the Voltage Amplifier output (COMP) upward, the Current Amplifier output (CAO/ENBL) higher, will increase the duty cycle and thus will increase the inductor current.

COMP is clamped to V_{BUF} + 1.0V by the buffer. As the average output inductor current continues to rise, to raise the output voltage, the output of the Current Sense Amplifier, ISO, exceeds the value of COMP. This occurs when

$$I_{SC} \bullet R_{SENSE} \bullet G_{CSA} = 1.0 \text{ Volt}$$

or at a short circuit current limit, I_{SC}, of

$$I_{SC} = \frac{1.0 \text{ Volt}}{R_{SENSE} \bullet G_{CSA}} \text{ [Amperes]}$$

When ISO exceeds the value of COMP, the Current Amplifier, configured for high DC gain, swings to its minimum value, resulting in a lower short circuit duty cycle, D_{SC}. D_{SC} is high enough only to maintain the average current through the inductor.

Figure 19 graphically represents the dynamics of a short circuit placed across the output of the Buck regulator of Figure 12 at time t_1.

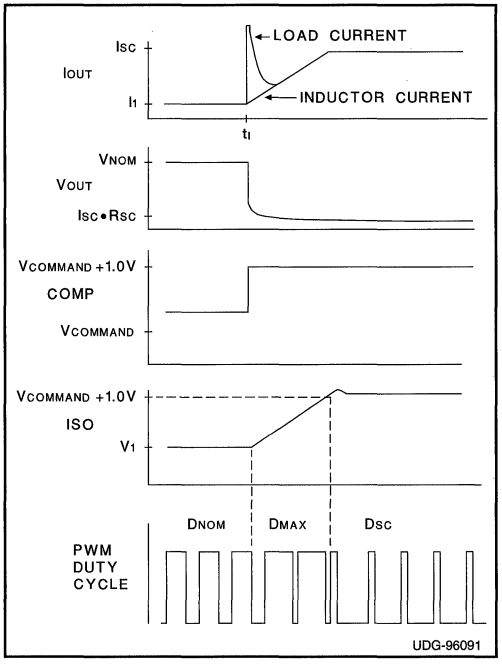

Figure 19. Dynamics of Short Circuit Protection with the UC3886

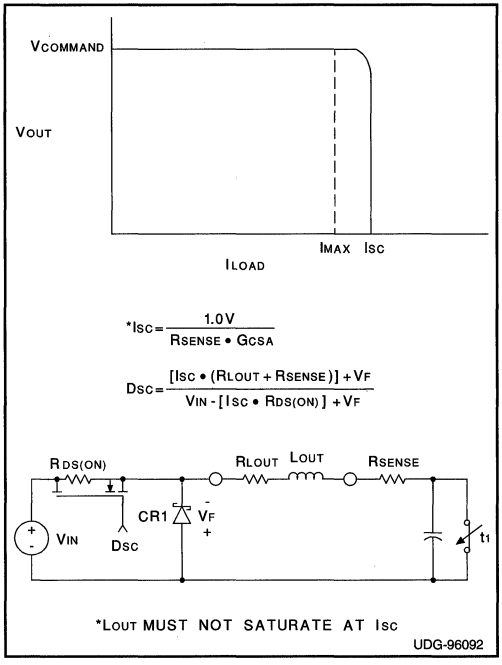

Figure 20. UC3886 Current Limit Load Line in a Buck Regulator

Current Limit Load Line

Current limiting in the UC3886 follows a "square knee" load line, where current is not disabled or folded back. Figure 20 shows this load line.

The voltage at the output of the Buck regulator of Figure 20 falls proportionally to the value of the short circuit, usually measured in milliohms. Many regulators, under a short circuit of extremely low resistance, will demonstrate a condition where Ipeak can be much larger than I_{SC}, often referred to as "tail-out". Safety and reliability issues may arise should the value of Ipeak not be well understood and controlled.

The simplified Buck regulator shown in Figure 20 shows several key parasitic elements, along with the value of R_{SENSE}, which limit the current to I_{SC}, preventing tail-out. See Appendix 5 for a detailed example of programming the current limit using the UC3886 ACM Controller.

AVERAGE CURRENT MODE CONTROL IN DISCONTINUOUS MODE

Average current mode control offers the advantage of being able to function while the regulator is running in a discontinuous mode of operation where the output inductor, and therefore the current signal, runs dry.

With peak current mode control, during discontinuous mode, the peak/average current error becomes unacceptably large, a result of the fixed and limited gain in peak current mode control. The high gain of the Current Amplifier used in Average Current Mode control allows the large changes in duty cycle required for load changes. The Average Current Mode gain, however, is limited.

> There is a slope limitation criteria of Average Current Mode control (U-140 [4]) which is: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This slope criteria directly limits the amount of gain obtainable in the Current Amplifier at the switching frequency.

The criteria mentioned above can be equated as

$$\frac{V_O + V_F}{L_{OUT}} \bullet R_S \bullet G_{CSA} \bullet G_{CA} \pounds \frac{V_S}{T_S - T_D}$$

where, in the model of Figure 18

V_S = Oscillator Ramp [V]

T_S = Switching Period [s]

T_D = Oscillator Deadtime [s]

V_O = Output Voltage [V]

V_F = Freewheeling Diode Forward Voltage [V]

L_{OUT} = Output inductor [H]

R_S = Sense Resistor [W]

G_{CSA} = Gain of the Current Sense Amplifier

G_{CA} = Gain of the Current Amplifier at the switching Frequency.

It can be shown from the above equation that the Current Amplifier gain is directly proportional to the Inductor value, and is constant at a given output voltage.

$$\frac{G_{CA}}{L_{OUT}} = \frac{V_S}{T_S - T_D} \bullet \frac{1}{R_S \bullet G_{CSA}} \bullet \frac{1}{V_O + V_F} = K$$

Decreasing L_{OUT} must result in a decrease in G_{CA}, and therefore the Average Current Mode gain. This lower current gain will adversely effect large signal response of the circuit, although a smaller inductor value will improve large signal response. Even with this limitation on the gain G_{CA}, Average Current Mode Control can achieve much higher gains than Peak Current Mode control.

STARTUP AND SOFT STARTING WITH THE UC3886

Soft starting a power supply is defined as bringing the output voltage up to its specified value in a slow, controlled manner. Typical power supplies soft start in 10ms to 100ms.

The need for soft starting a power supply is often associated with overshoot. The output voltage of a power supply will often ring over its specified value when the power supply is "snapped" on, as the control loop often lags the rise of the output voltage. The overshoot can be destructive if it is not clamped or controlled. Slowly ramping up the output voltage will minimize the overshoot.

The fast transient response of the UC3886 Average Current Mode controller helps eliminate the need for soft starting the DC/DC converter. At startup, the Average Current Mode control directly controls the inductor current. As long as the output voltage is less than the required voltage, the current loop forces the UC3886 to supply current limited to I_{SC}, the short circuit limit. Once the proper output voltage is reached, the very fast transient response of the UC3886 Voltage and Current Amplifiers will cut back on the duty cycle, thus eliminating the voltage overshoot associated with a slow loop response. A large output capacitance on the DC/DC converter will insure that a slight overshoot in inductor current results in negligible overshoot in the output voltage.

A soft start capacitor can be added to the VCOMMAND pin as shown in the circuit of Figure 21, should a slow, controlled start up be required. The values or resistors R1 and R2 should be chosen to (a) create the proper voltage at VCOMMAND, (b) draw less than 2.0mA from VREF and (c) equal the impedance seen by the inverting input of the UC3886 Voltage Amplifier, V_{SENSE}, to cancel bias current effects. Once the resistors are chosen, then C_{SS} should be chosen for the proper time constant.

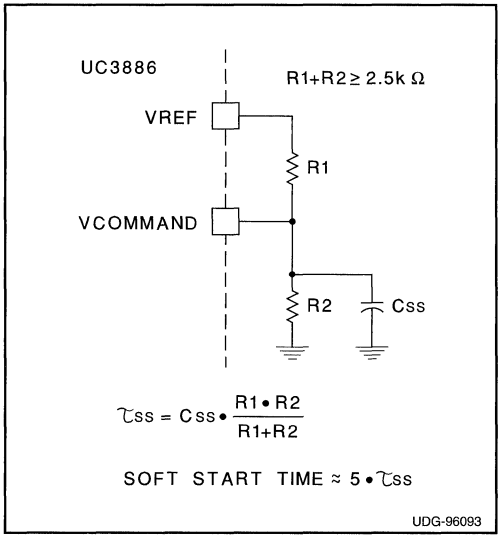

Figure 21. Soft Starting the UC3886

DRIVING A HIGH SIDE N-CHANNEL MOSFET WITH THE UC3886

The UC3886 is designed to drive an N-Channel MOSFET in a Buck configuration, as shown in Figure 6. There are circuit and MOSFET factors to be considered in order to properly drive the MOSFET. The circuit factors include the values of V_{IN}, V_{CC}, UVLO, the UC3886 totem-pole gate voltage and ringing voltages on the Gate and Source nodes. The MOSFET factors include V_{GSmin}, V_{GSmax}, R_{DSon} vs V_{GS}, and the type of MOSFET used, standard or Logic Level. A MOSFET's on and off characteristics are controlled by the gate-to-source voltage, V_{GS}.

There are many sources of literature [6, 7, 8, 9] which discuss MOSFET drive circuits and parameters. This application note will highlight several considerations in using the UC3886 GATE output in dri-

ving standard and Logic Level MOSFETs in a Buck regulator.

Standard MOSFET

1) Given a 5 volt input and a 12 volt V_{CC} source to the UC3886 (Figure 6), V_{GS} is only 7 volts nominally. R_{DSon} for standard MOSFETs is often specified with V_{GS} = 10V. A survey of several 60 volt low R_{DSon} MOSFETs shows that R_{DSon} is higher by a factor of approximately 1.35 when these MOSFETs are driven with only 7 volts V_{GS}. Specific data sheets and curves should be reviewed for exact figures.

2) The UVLO threshold at startup for the UC3886 is 10.3 volts. Although the PWM will start switching when UVLO is disabled, there may not be enough gate-to-source voltage for the MOSFET to carry the full load current. This characteristic can effect the amount of time to reach full load current at startup.

3) Turn on time for standard MOSFETs is often specified with V_{GS} = 10V, whereas the initial gate-to-source voltage from the UC3886 may be less than 10V. The resulting turn on time may be longer than specified in the device data sheets.

Logic Level MOSFET

1) Many modern, low voltage, low R_{DSon} Logic Level MOSFETs have a maximum V_{GS} rating of ±10V. Excessive gate voltage may damage or seriously degrade the reliability of these MOSFETs.

In the Buck regulator of Figure 6, the source voltage is rising from $-V_F$ to $+V_{IN}$ during turn on. At the beginning of the cycle, the gate-to-source voltage, V_{GS}, is equal to $V_{GATE}+V_F$, which may be well in excess of 10V. At the end of the cycle, V_{GS} is less, as the source voltage has risen to approximately the input voltage. The gate-to-source voltage dynamic characteristics are dependent on the value of series gate resistance, R_{GATE}, as well as circuit load characteristics. R_{GATE} can be increased to insure that during the turn-on pulse, the source voltage has risen to the input voltage well in advance of V_{GS} reaching its maximum value. The cost of this approach may be in switching power losses.

A gate-to-source zener diode can be used as shown in Figure 22 to insure that excessive V_{GS} is not reached.

Low R_{DSon} - Low Voltage MOSFETs

Several MOSFET processes have increased the density of MOSFET cells in order to optimize R_{DSon} and current handling capabilities. One result of this is the reduction of a good Gate metal path to individual cells. The result of this is higher internal gate resistance and inductance, which effects the switching performance of the MOSFET.

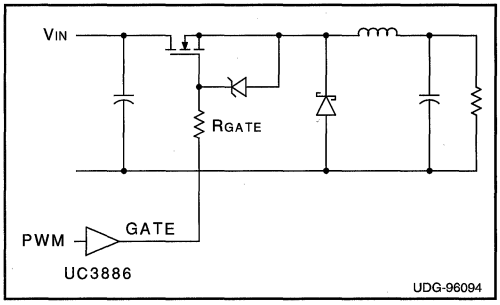

Figure 22. Clamping V_{GS} with a Zener Diode

A noticeable effect of these parasitics is the difference between the Turn-On delay and the Turn-Off delay. At turn-on, as soon as a small number of cells are turned on, drain current begins to conduct. At turn-off however, the gate charge must be removed from all MOSFET cells, resulting in a substantial delay in turning off the drain current, as illustrated in Figure 23. MOSFET Turn-on and Turn-off delays will vary based on supplier processes. Supplier data sheets should be consulted.

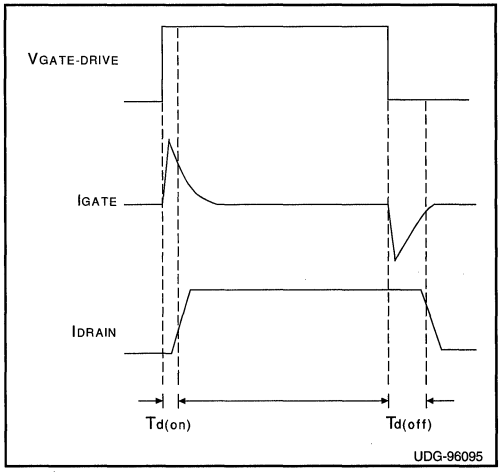

Figure 23. MOSFET Turn-On and Turn-Off Delays

USING THE UC3886 WITH THE UC3910 FOR A COMPLETE Pentium®Pro SOLUTION

The UC3886/UC3910 Chip Pair is shown in Figure 24 as configured in a typical Buck regulator. The programmable DAC output of the UC3910 is simply fed into the VCOMMAND pin of the UC3886 to provide a programmable PWM controlled power supply.

Using this chip pair offers significant benefits when providing power to today's microprocessors. The two IC's can be configured, as shown in Figure 24, to provide all functions required to interface with,

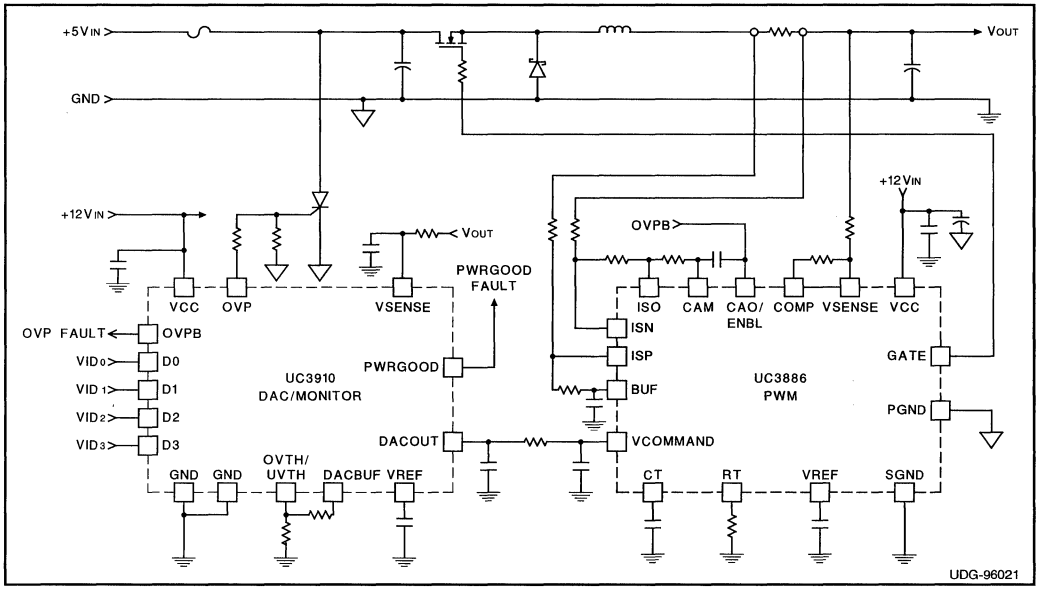

Figure 24. UC3886/UC3910 Interconnection Diagram

control, and monitor the performance of the Intel Pentium®Pro and other high end processors. Together, the chip pair meets the critical requirements of the Pentium®Pro with a simple, accurate and efficient switching regulator which meets the difficult transient regulation requirements with Average Current Mode Control.

For additional information on the UC3910 4-BIT DAC and Voltage Monitor IC, refer to application note U-158 [10]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [11].

Features of the UC3886/UC3910 Chip Pair

Simplicity

The UC3886/UC3910 is configured to drive a basic Buck regulator. The ICs integrate all control and monitoring functions, so that external parts count is reduced. Circuit boards can use fewer layers, fewer interconnects and fewer components.

The UC3886 features a direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.

The programmable voltage feature of the UC3910 allows system designers to directly interface with Intel's Pentium®Pro to create one power supply that will meet all voltage requirements, and thus reducing all the logistics associated with single output power supplies.

The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. The UC3910's tracking fault windows are simply programmable with two external resistors.

The UC3886 can directly monitor the inductor current through a low value resistor, eliminating the need for a current transformer or complicated waveform synthesis circuitry.

The accuracy and true "square-knee" characteristic of the UC3886 over current limit programming eliminates the need to over-design the power components for operation in an indefinite short circuit.

Accuracy

The typical ±0.5% accuracy of the UC3910 is not corrupted by the UC3886, as the UC3886 uses a very low offset Voltage Amplifier, has very low bias currents, and offsets the bias currents within the IC. The combined system accuracy is ±1%. This high DC accuracy negates the need for trimming the power supply output voltage in manufacturing.

Efficiency

The high current drive of the UC3886 allows the use a high end low R_{DSon} N-channel MOSFET. Full

load efficiencies of 80% can be met with a minimal cost and parts count.

Severe Transient Loading

The UC3886 Average Current Mode Control features allow optimization of both the voltage and current loops. High gain in the current loop can be achieved with Average Current Mode control. The UC3886 features very fast amplifiers for optimal large signal performance. The voltage and Current Amplifiers are internally clamped to reduce their dynamic range, which prevent large overshoot and respond faster to changes in load current. The UC3910 high accuracy allows a tightly regulated DC voltage which allows a wider voltage swing under load transient conditions.

SUMMARY

Power supply requirements for low voltage, high end processors are particularly difficult to meet with regard to tight regulation and fast transient response. The UC3886 contains all the features required to meet these requirements while maintaining high efficiency and a low external parts count. Average current mode control offers excellent regulation and fast transient response, accurate current limiting reduces electrical and thermal overdesign, and high side N-MOSFET drive helps create a simple and high efficiency power circuit.

REFERENCES

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[8] Unitrode Application Note U-118, New Driver ICs Optimize High Speed Power MOSFET Switching Characteristics, Bill Andreycak

[9] Unitrode Application Note U-137, Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits, Bill Andreycak

[10] Unitrode Application Note U-158, The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies, Larry Spaziani

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APPENDIX 1: BUCK REGULATOR BASICS

A schematic of a basic Buck regulator power stage is shown in Figure 1A . Several parasitic elements are included for the reasons described below.

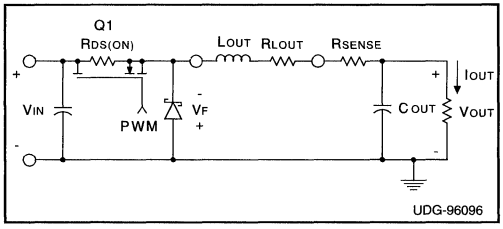

Figure 1A - Buck Regulator Power Stage

The transfer function of a Buck regulator is often simplified as

$$V_{OUT} = V_{IN} - D \qquad \text{Simple Approximation}$$

where D is the duty cycle of the Pulse Width Modulator (PWM).

Parasitic elements such as series resistance and even the diode drop, V_F, are often assumed to be negligible, especially when the output voltage is large compared to these voltage drops, and current is low.

For a low voltage, high current Buck regulator, a more exact transfer function is necessary to insure proper operation.

The basic operation of a Buck regulator with PWM control is this: a PWM controlled rectangular waveform is created by the switch, Q1, and is averaged by the output LC power stage. The inductor must balance volt-seconds during both the ON time and the OFF time in order for this averaging function to occur. Volt-seconds is defined as the product of the voltage across the inductor and the time which that voltage is present.

The equation for the volt-second product across the inductor during the ON and OFF times are given by:

$$VOLT\_SEC\_ON = (V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON}$$

$$VOLT\_SEC\_OFF = (V_{OUT} + I_{OUT} \bullet (R_{LOUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Equating the volt seconds gives

$$(V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON} = (V_{OUT} + I_{OUT} \bullet (RL_{OUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Duty cycle D is defined as T_{ON}/T, where T is the switching period. Therefore, T_{OFF}/T can be defined as 1-D, resulting in

$$\frac{T_{ON}}{T_{OFF}} = \frac{D \bullet T}{(1\text{-}D) \bullet T} =$$

$$\frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - [I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE})] - V_{OUT}}$$

giving the governing equation for the output voltage

$$V_{OUT} = (D \bullet V_{IN}) - (D \bullet I_{OUT} \bullet R_{DSON}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1 - D)]$$

and the governing equation for duty cycle

$$D = \frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - (I_{OUT} \bullet R_{DSON}) + V_F}$$

Duty Cycle for Buck Regulator

Example:

V_{IN} = 5.0V

V_{OUT} = 3.1V

R_{LOUT} = 0.010W

R_{SENSE} = 0.010W

R_{DSON} = 0.025W

I_{OUT} = 1A min to 10A max

V_F = 0.4V @ 1A, 0.5V @ 10A

Estimate Duty cycle based on the simple duty cycle approximation:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{3.1V}{5.0V} = 62\%$$

Calculate Duty cycle based on the complete equation:

$$D = \frac{3.1V + [10A \bullet (0.01W + 0.01W)] + 0.5V}{}$$

$$= 72.4\%@10A$$

$$D = \frac{3.1V + [1A \bullet (0.01W + 0.01W)] + 0.4V}{5.0V - (110A \bullet 0.025W) + 0.4V}$$

$$= 65.5\%@1A$$

The results show that simplifying the transfer function can result in a substantial error when low voltages and high currents are considered.

APPENDIX 2: CALCULATING AVERAGE GATE DRIVE CURRENT, I_{GATE}

A MOSFET gate requires a total gate charge, Q_G, which is specified in the manufacturer's data sheet, in order to effectively turn on. Understanding gate drive requirements and dynamics is discussed in detail in U-118 [8] and in U-137 [9]. The MOSFET gate is charged up at turn-on by a peak current waveform, often limited by the driver output impedance as well as series resistance. Over many cycles, the peaks of current can be averaged. This average current must be supplied to the UC3886 from the V_{CC} source.

Figure 2A shows an N-channel MOSFET in a Buck regulator configuration. The input voltage is 5V, and the gate driver is powered from 12V. The effective Gate-to-Source voltage is therefore 7V.

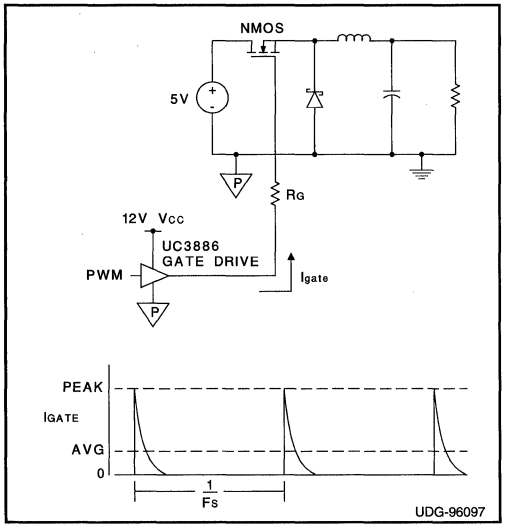

Figure 2A. Calculating Average Gate Current

Figure 2B is a generic example of a manufacturer's "Gate-Source Voltage vs Gate Charge" curve, found in most MOSFET data sheets. The charge required is a direct function of the Gate-to-Source voltage which drives the MOSFET. Using this curve, the required gate charge for the circuit in Figure 2A can be read off of the curve.

Gate charge and current are related by

$$Q_G = I_{GATE} \bullet T_S$$

where I_{GATE} is the AVERAGE gate current and T_S is $1/F_S$ or one switching period.

Average gate current, I_{GATE}, can therefore be calculated by using

$$I_{GATE} = Q_G / T_S = Q_G \bullet F_S.$$

As an example, an IRFZ48 MOSFET requires approximately 50 nanocoulombs total gate charge (Q_G) with 7 volts V_{GS} drive. The average current drawn by the gate at an operating frequency of 200kHz is therefore

$$I_{GATE} = 50nC \bullet 200kHz = 10 \text{ milliamps.}$$

The total current drawn by the UC3886 under these operating conditions, would therefore be

$$I_{CC} = I_{BIAS} + I_{GATE} = 10mA + 10mA$$
$$= 20mA \text{ total.}$$

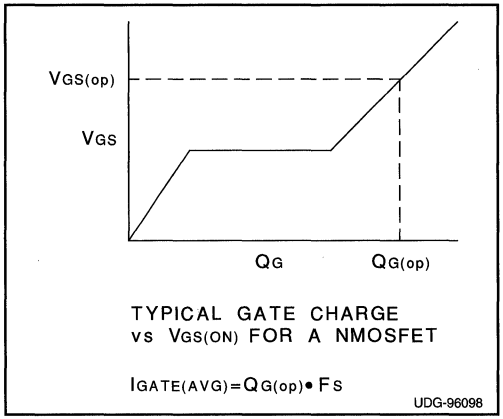

Figure 2B. Using Total Gate Charge to Calculate Gate Current

APPENDIX 3: MANAGING REGULATION AT THE LOAD WITH NON-INTEGRATING GAIN

A model of an Average Current Mode controlled Buck regulator is shown in Figure 3A. The Average Current Mode control loop can be modeled as a simple transconductance amplifier, which converts the Voltage Amplifier's error voltage into the required average output current.

The parasitic resistive and inductive elements shown in the circuit will have the following effects:

- The resistive elements will cause a steady state load regulation error proportional to resistance and load current
- The resistive elements will cause a transient voltage drop proportional to resistance and amplitude of the change in load current
- The inductive elements will cause a transient voltage drop proportional to inductance and the rate of change, di/dt.

Sensitive loads, such as high end Processor ICs, require regulation at the load to be extremely tight under load variations. Load regulation specifica-

tions can consist of a window of voltage regulation which includes variations of steady state load current, load transient conditions, voltage ripple and DC regulation tolerances.

The allowed transient voltage deviation, when considering low voltage processors with very fast transients rates, can be extremely difficult to meet, and may require an excessive amount of output capacitance in order to keep the total capacitor's ESR and ESL low enough to meet the regulation requirements. Excess capacitance is bulky and expensive.

Managing the regulation at the load can be summarized by the following goals and methods to meet the goals.

Goals

1. Meet ±5% regulation at the load under all operating conditions
2. Minimize the amount of output capacitance required at the power supply output in order to minimize cost and size

Methods

1. Use parallel, low impedance pins at the power supply connector.
2. Use power and ground planes from the power supply to the load.
3. Maximize local decoupling at the load.
4. Minimize ripple to maximize use of the regulation window.
5. Compensate for the I • R voltage drop to the load with positive DC offset at the power supply output.
6. Maximize allowable transient voltage swing by providing positive DC offset at the power supply output when operating at the minimum load, and providing negative DC offset at the power supply output when operating at the maximum load. This can be accomplished by using Non integrating gain (resistive, not capacitive feed back) about the Voltage Amplifier.

Methods 1 through 4 consist of good electronic layout and filtering practices. Methods 5 and 6 are steps which can be taken at the power supply, and are discussed below.

Figure 3B illustrates the output voltage effects resulting from load transients when integrating and non-integrating feedback is utilized as well as the effects of a DC offset voltage.

Integrating gain utilizes a DC blocking capacitor in the feedback, and therefore results in a very high

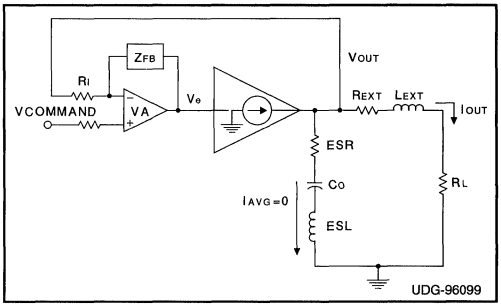

Figure 3A. Average Current Mode Controlled Regulator Output Model

DC gain. The result is excellent load regulation, where the output voltage is nominally equal to the command voltage. This is typical of most power supplies.

Non-integrating gain utilizes a resistive feedback path instead of capacitive. The result is that the output voltage will decrease as the load current increases. This provides an INTENTIONAL negative load regulation characteristic.

The use of the DC offset, achieved simply by the voltage divider formed by R_I and R_D of Figure 3B, centers the output voltage at nominal load.

These points are best shown by an example.

EXAMPLE

Buck regulator using UC3886/UC3910 Chip Pair

V_{OUT} = 2.4V to 3.4V.

Regulation window = ±5% including load, line, ripple and transient conditions.

Ripple = ±1%

DC Regulation Tolerance plus Line Regulation = ±1%

I • R Voltage Drop from power supply to load = -1% at Imax

Imin = 0.5A = Minimum normal operating current

Imax = 10A = Maximum normal operating current

I_Limit = 12A = Short circuit current limit

Goal: Determine and set V_{OUT} vs I_{OUT} such that the ±5% Regulation requirement is met with maximum allowed transient voltage swings (minimum output capacitance).

Step 1: Establish a regulation goal.

The specified window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%,

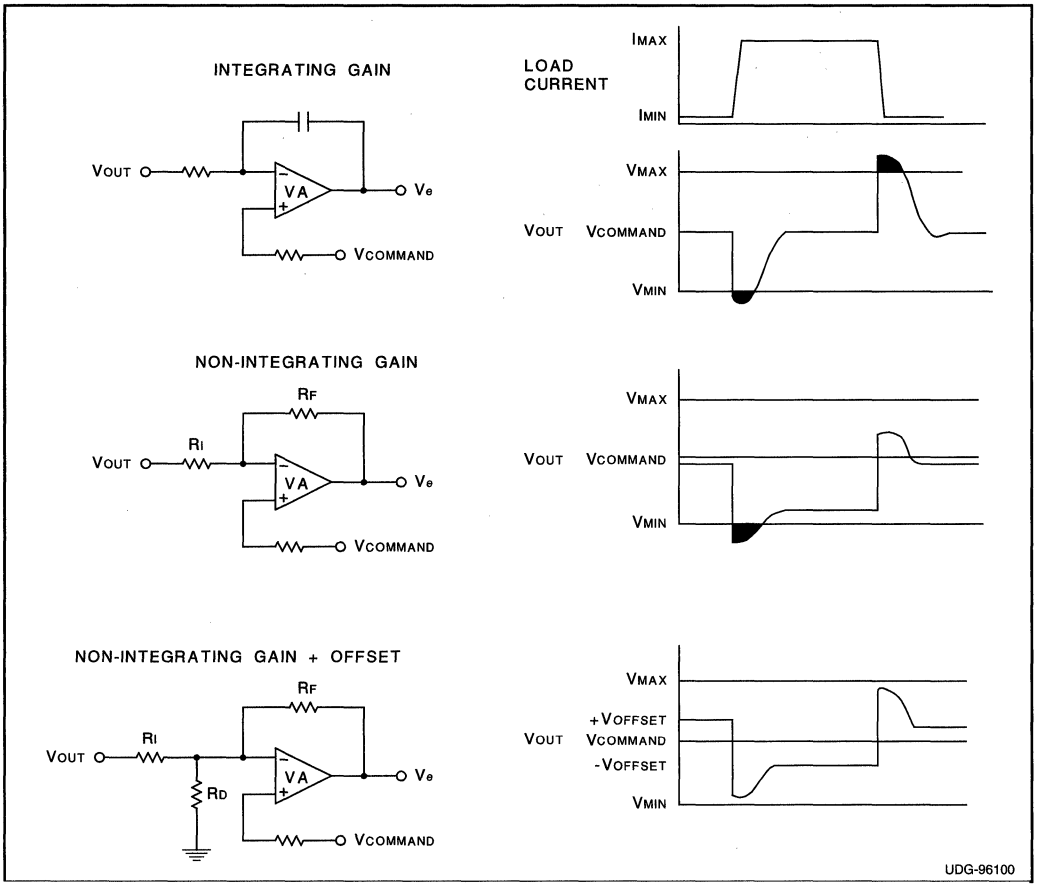

Figure 3B. Integrating vs Non-Integrating Gain in the Voltage Error Amplifier of the UC3886

reserve ±2% of the specified window. This leaves ±3% of the window for load regulation.

Figure 3C illustrates the regulation window.

Based on the regulation of integrating gain, a load step from Imin to Imax may only cause a -3% voltage excursion and still insure that the ±5% window requirement is met. The load regulation set as a goal will double the allowed voltage excursion from -3% to -6%.

Step 2: Determine the voltage-to-current gain of the closed loop Average Current Mode circuit.

The UC3886 error voltage, COMP, swings from Vcommand at 0.0 amperes load current, to $V_{COMMAND}$ +1.0V at the short circuit current limit point, I_Limit, set by the Current Sense Amplifier gain. The voltage-to-current gain is therefore equal to

$$V\_to\_I\_Gain = \frac{I\_Limit}{DVe} = \frac{12\ A}{1.0\ V} = 12$$

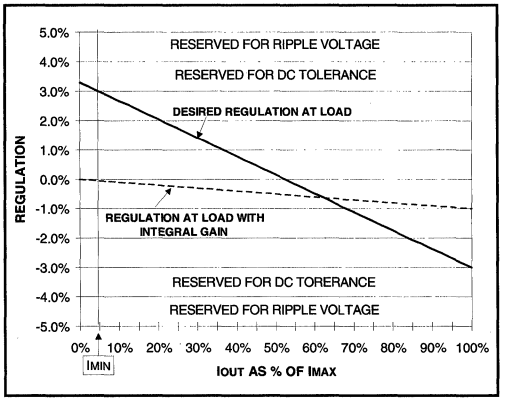

Figure 3C. Load Regulation for Example Circuit

Step 3: Determine the swing in the UC3886 error voltage, COMP, at Imax.

$$DVe = \frac{Imax}{I\_Limit} \bullet 1.0 = \frac{10.0\ A}{12\ A} \bullet 1.0$$

$$= 0.833\ Volts$$

From the desired load regulation curve, determine the swing in output voltage associated with the change from 0 Amps (Not Imin in this case) to Imax. Subtract the I • R drop intrinsic to the circuit.

The desired regulation swing is -6.3% - (-1.0%) = -5.3% from 0A to Imax. At the lowest operating output voltage, this is equivalent to:

$$DV_{OUT} = 2.4V \bullet 5.3\% = 0.127\ Volts$$

Step 4: Determine the gain around the Voltage Amplifier to achieve the desired voltage swing over the operating load range.

$$DVout = \frac{DVe}{Gain} = \frac{DVe}{R_F/R_I}$$

$$\text{and therefore } R_F/R_I = \frac{0.833V}{0.127V} = 6.56$$

Where R_F is the feedback resistor and R_I is the input resistor, as in Figure 3B. Let R_F = 20.0kW, then R_I = 3.09kW and the gain about the Voltage Amplifier = 6.47.

Step 5: Determine the DC offset required from the Resistive Divider and calculate the value of R_D.

The resistive divider must offset the output voltage by the desired offset at 0.0 Amps of +3.3%.

Using a voltage divider resistor, R_D with R_I, as shown in Figure 3B:

$$\frac{R_D}{R_I + R_D} = 1 - 0.033 \text{ so}$$

$$R_D = \frac{R_I \bullet (1-0.033)}{0.033} = 90.9kW$$

Figure 3D illustrates the resulting load regulation at the output of the power supply and at the load.

Step 6: Determine the effects of a variable output voltage

The DC offset fixed by the voltage divider of R_I and R_D is setting an offset percentage, which is constant at 3.3%.

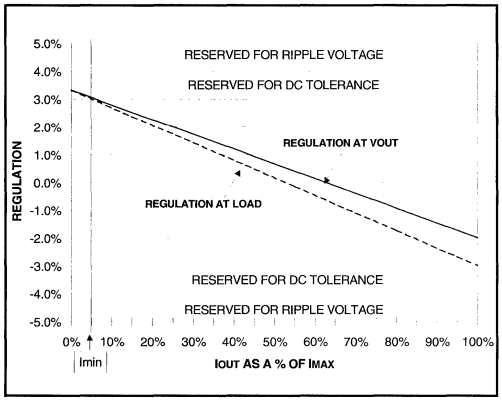

Figure 3D. Load Regulation for Example Circuit -2.4V Output

Therefore, at 0.0A all output voltages will start at +3.3% offset.

The gain of the Voltage Amplifier, set by R_F and R_I, is also fixed, and will therefore have a smaller effect at output voltages larger then 2.4V. At 3.4V, the change in output voltage is fixed at -0.127 Volts, which is only -3.74% of the nominal output. The higher voltages will therefore operate within a narrower voltage regulation window than 2.4V and the voltage regulation requirements will be met.

APPENDIX 4: DIFFERENTIAL AMPLIFIER EQUATIONS

The amplifier shown in Figure 4A is configured as a differential amplifier, with a DC bias. The output voltage of this configuration is given by

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

This result can be derived from the principal of superposition, by adding the portion of the output voltage due to each input voltage, V1, V2 and V_{BIAS}.

V1 term: Set V_{BIAS} and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier V(+) is derived from the voltage divider of R2 and R1, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V1 \bullet \left(\frac{R2}{R1+R2}\right)$$

$$V_{OUTV1} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

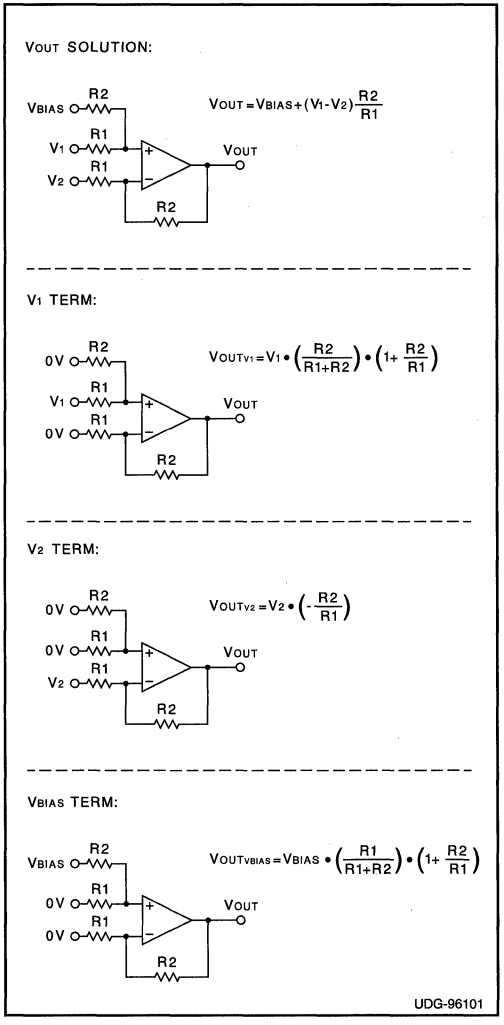

Figure 4A. Differential Amplifier Configuration with DC Bias

V2 term: Set V_{BIAS} and V1 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is 0 volts. The configuration is therefore a standard inverting op-amp configuration which gives

$$V_{OUTV2} = V2 \bullet \left(-\frac{R2}{R1}\right)$$

V_{BIAS} term: Set V1 and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is derived from the voltage divider of R1 and R2, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right)$$

$$V_{OUTVBIAS} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

when factored gives

$$V_{OUTVBIAS} = V_{BIAS}$$

V_{OUT} Solution: Sum the 3 terms together

$$V_{OUT} = V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$+ V2 \bullet \left(-\frac{R2}{R1}\right) + V_{BIAS}$$

which yields

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

The DC Bias is the value of V_{BIAS}, and the gain of the differential amplifier which multiplies the difference voltage (V1 - V2) is given by

$$\text{Gain} = \frac{R2}{R1}$$

APPENDIX 5: PROGRAMMING THE SHORT CIRCUIT LIMIT

From the short circuit current equation

$$I_{SC} = \frac{1.0 \text{ volt}}{R_{SENSE} \bullet G_{CSA}}$$

it can be seen that the product of the sense resistor and the gain of the Current Sense Amplifier must be

$$R_{SENSE} \bullet G_{CSA} = \frac{1.0 \text{ Volt}}{I_{SC}}$$

The value of G_{CSA} is bounded to

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX} = \frac{2.5MHz}{F_{SWITCH}}$$

which in turn, bounds the value of R_{SENSE}, since the product is a constant.

Several considerations must be used to select R_{SENSE}:

- Type - 2 Wire vs 4 Wire: With very low value sense resistors, as the UC3886 allows, the resistance of the solder joint becomes a major contributor to resistance. A 4 wire Kelvin connection removes the error due to the solder joint. A 2 wire is more cost effective. A compromise may be in using a surface mount 2 wire resistor and splitting the pads to simulate a 4 wire connection. Beware that paralleling 4 wire

resistors for reduced power dissipation can result in an imbalance between the resistors.

- Value - Minimum and Maximum possible values: The upper value is limited by the minimum G_{CSA} value, and the lower value by the maximum G_{CSA} value. Higher values dissipate more power. Lower values typically have a higher temperature coefficient, resulting in less accuracy over temperature and have a higher cost factor.
- Efficiency and Power Dissipation: The lower the value of R_{SENSE}, the less power dissipation and the higher the regulator's efficiency. Power dissipation must be considered under both normal maximum operating current, Imax, as well as under short circuit conditions, I_{SC}.
- Operating Voltages and Duty Cycle: Given a low input voltage and an output voltage close to V_{IN}, such as 3.3V input, 2.9V output, the operating duty cycle can be quite high. A large voltage drop across R_{SENSE} may be unacceptable.
- Self-Inductance: A low inductance type of resistor should be used. Inductance of the resistor will result in an inductive "step" voltage superimposed on the ramp voltage. The step voltage will not contribute to error as the average current measurement is not effected, but may contribute to instability due to the very high slope of the inductive step. Refer to Unitrode Application Note U-140 [4] regarding slope limitations in Average Current Mode Control.

The following example illustrates the selection process in choosing R_{SENSE} and in setting the value of G_{CSA}.

F_{SWITCH}: 200kHz

Imax: 10.0A

I_{RIPPLE}: 1.0Ap-p

R_{LOUT} 0.01W

V_F 0.5V @ 12A

V_{IN} 5.0V

$R_{DS(on)}$ 0.025W

Step 1: Find the bounds of the Current Sense Amplifier gain G_{CSA}.

Minimum gain = 5.0 By specification

$$\text{Maximum gain} = \frac{2.5\text{MHz}}{200\text{kHz}} = 12.5$$

Step 2: Choose the short circuit limit. This limit should insure that tolerances and ripple current do not inadvertently trip the over current threshold.

Figure 5A illustrates the limitations on the sense resistor based on the bounds of the gain. Choosing a value of Isc as low as possible will limit the power dissipation in the sense resistor.

Select I_{SC} = 12.0 Amps.

Step 3: Choose a value of R_{SENSE}

From Figure 5A, a 12.0A I_{SC} implies that Rsense must lie between 0.007W and 0.017W. Choose 0.010W as the lowest standard value.

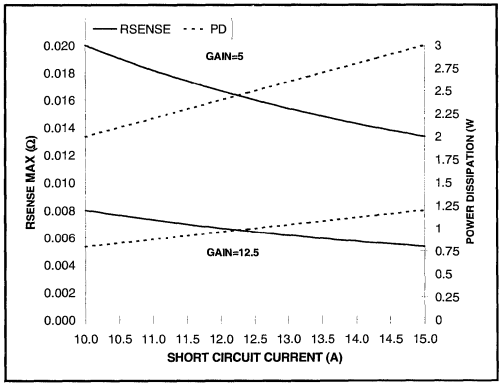

Figure 5A. R_{SENSE} and Power Dissipation Boundaries

Step 4: Program the gain of the Current Sense Amplifier.

$$G_{CSA} = \frac{1.0\text{ Volt}}{I_{SC} \bullet R_{SENSE}}$$

$$= \frac{1.0\text{ Volt}}{12.0\text{A} \bullet 0.01\text{W}} = 8.33$$

Choose large enough resistors so as not to load down the output of the Current Sense Amplifier. Refer to Figure 14 of this application note to configure the Current Sense Amplifier.

Select R2 = 36.5kW

$$R1 = \frac{36.5\text{kW}}{8.33} = 4.42\text{kW}$$ (closest 1% value)

$$G_{CSA} = \frac{36.5}{4.42} = 8.25$$

Step 5: Solve for the minimum AVERAGE short circuit current limit.

The tolerance of the UC3886 current limit

clamping mechanism is 1.0V ±0.05V. Assume R_{SENSE} and G_{CSA} each have a tolerance of ±2% over temperature and life. 1/2 of I_{RIPPLE} will add to the AVERAGE current value of I_{SC}, and should not cause the UC3886 to clamp into over current.

Then

$$I_{SC(min)} + \frac{I_{RIP}}{2} = \frac{0.95\ Volt}{R_{SENSE} \bullet 1.02 \bullet G_{CSA} \bullet 1.02}$$

which gives

$$I_{SC(min)} = \frac{0.95\ Volt}{0.010W \bullet 1.02 \bullet 8.25 \bullet 1.02} - \frac{1.0A}{2} = 10.57\ Amperes$$

which is above the maximum operating current of 10.0 amperes

Step 6: Calculate the power dissipation in R_{SENSE} during normal and short circuit conditions.

Normal: $Pd = Imax^2 \bullet R_{SENSE}$

$= 10^2 \bullet 0.010W = 1.0$ Watt

Short Circuit: $Pd = I_{SC}^2 \bullet R_{SENSE}$

$= 12^2 \bullet 0.010W = 1.44$ Watt

Calculating the Short Circuit Duty Cycle

During a short circuit condition in a Buck regulator, the duty cycle becomes small and the free-wheeling diode conducts current for most of each switching cycle. The free-wheeling diode's average current is almost equivalent to the short circuit current in this condition, resulting in much higher power dissipation.

To calculate the power dissipated in the diode, the short circuit duty cycle, D_{SC}, must be calculated.

The governing equation of the Buck regulator is derived in Appendix 1, where the output voltage is given by

$$V_{OUT} = D \bullet (V_{IN} - I_{OUT} \bullet (R_{DSon}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1-D)]$$

where D is the operating duty cycle. Under a true (0.0W) short circuit condition, the output voltage is 0.0 volts and the operating duty cycle will be D_{SC}. Using 0.0V in the formula above and solving for I_{SC} and D_{SC} gives

$$I_{SC} = \frac{D_{SC} \bullet (V_{IN} + V_F) - V_F}{D_{SC} \bullet R_{DSon} + R_{LOUT} + R_{SENSE}}$$

and $$D_{SC} = \frac{I_{SC} \bullet (R_{LOUT} + R_{SENSE}) + V_F}{V_{IN} - I_{SC} \bullet R_{DSon} + V_F}$$

Continuing from the above example, the short circuit duty cycle is

$$Dsc = \frac{12A \bullet (0.01W + 0.01W) + 0.5V}{5.0V - 12A \bullet 0.025W + 0.5V} = 12\%$$

The resulting diode average current is therefore

$I_{DIODE} = (100\%-12\%) \bullet 12A = 10.56$ Amperes.

The output inductor, L_{OUT}, must be designed not to saturate at the short circuit current. Should L_{OUT} saturate, excessive current can result which is only limited only by the parasitic resistances, which can result in reliability or safety problems.

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FUELING THE MEGAPROCESSOR - A DC/DC CONVERTER DESIGN REVIEW FEATURING THE UC3886 AND UC3910

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ABSTRACT

This application note provides a detailed account of design tradeoffs and procedures for the development of a Voltage Regulator Module (VRM) for the Intel Pentium®Pro processor. This voltage regulator features Unitrode's UC3886 Average Current Mode PWM Controller and UC3910 4-BIT DAC and Voltage Monitor ICs configured in a Buck Regulator. Test results and waveforms are provided which show how the VRM power supply meets stringent requirements imposed by Intel.

INTRODUCTION

Intel's Pentium®Pro power system specification demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. Meeting these requirements demands the most of both the power stage and the control system of the power supply. Unitrode's UC3886 and UC3910 are specifically designed for optimizing the control loop, the dynamic response and the DC accuracy required by the Pentium®Pro. The power stage inductor and capacitors are critical as well in meeting the extremely tight voltage regulation during a Pentium®Pro load transient.

This application note will detail the design of a complete VRM power supply. This design review will detail the critical VRM specifications, power supply architecture tradeoffs, power stage design details and equations and finally design specifics used to configure the UC3886 and UC3910. The complete current and voltage loops will then be closed, and performance results of the power supply will be shown.

This design review will reveal the many advantages of using the UC3886 and UC3910, which include:

- Direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.
- High DC accuracy negates the need for voltage trimming and insures the overall regulation will be met.
- Direct interface with INTEL's PENTIUM™ PRO VID programming codes.
- The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver.
- Accurate and true "square-knee" current limiting eliminates the need to over-design the power components for operation in an indefinite short circuit.
- Optimization of the loop performance due to large signal changes due to transient loading effects.

The Unitrode VRM demonstration kit is shown in Figure 1. The VRM's schematic is shown in Figure 2 and the parts are described in Table 1.

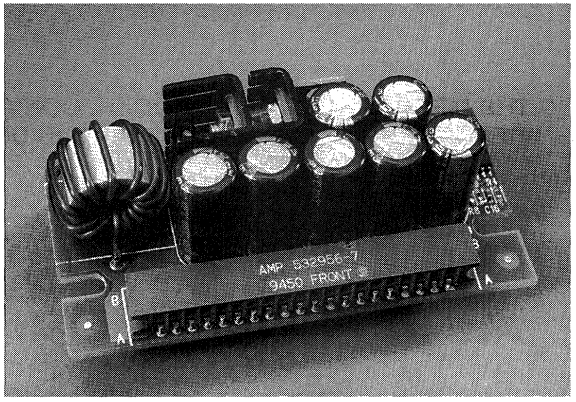

Figure 1. Unitrode's VRM Demonstration Kit

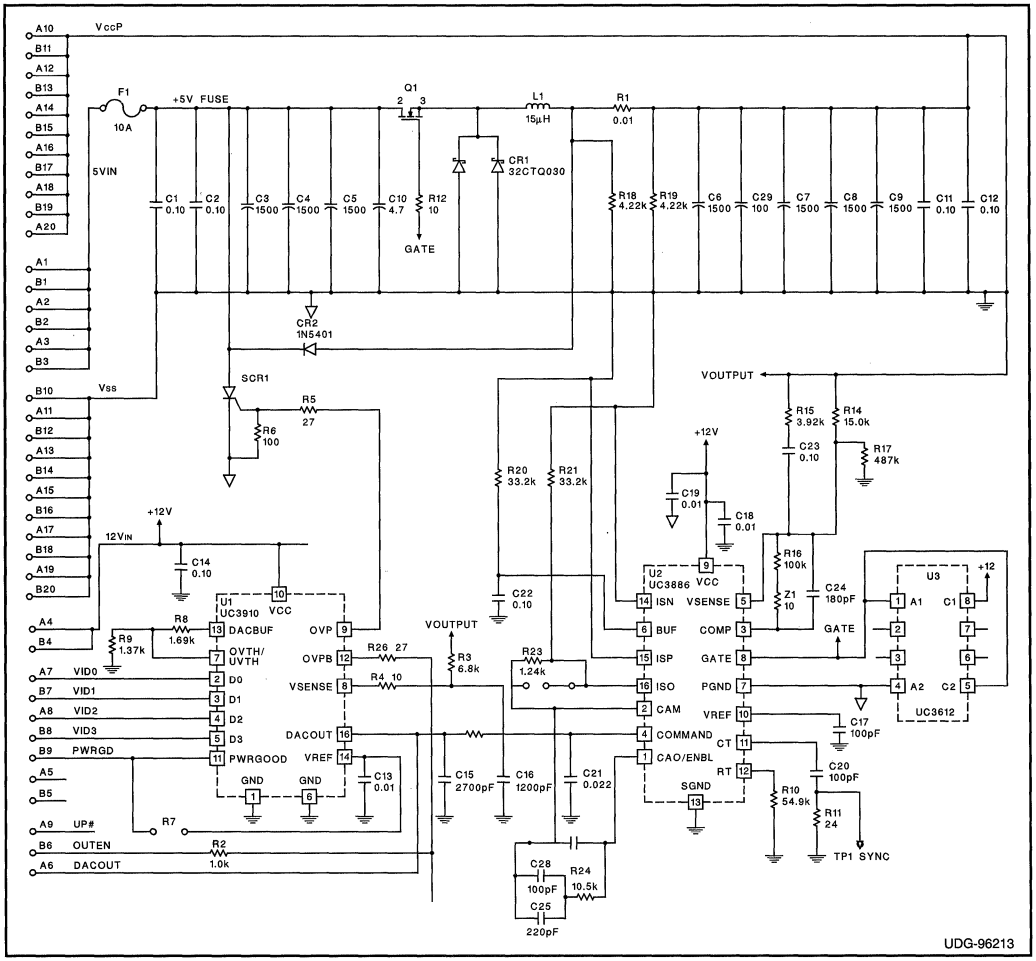

Figure 2. Schematic Diagram

POWER SUPPLY SPECIFICATIONS

The requirements for the DC/DC converter which will provide power to Intel Pentium®Pro are contained in Intel's application note AP-523 [1], Section 10. These power supply requirements consist of required specifications, expected specifications and design guidelines, some of which are summarized below.

Input Voltages: 5.00V ±5%
12.00V ±5%

Output Voltage: Variable from 2.4V to 3.4V programmable per INTEL VID codes, 100mV increments.

Minimum Current: 0.3A

Maximum Current: 11.2A

Regulation: ±5% Including initial tolerance, setpoints, drift, transients and ripple/noise.

Load Transient: Minimum to maximum or maximum to minimum current at a rate ≤30.3A/µs.

Input Current Rate: ±0.1A/µs maximum during a load transient.

Power-Good: Open Collector output LOW signal when the output voltage is not within ±10% of nominal.

Output Enable: Open Collector input signal with a LOW state disabling the DC/DC converter.

Ripple/Noise: ±1% to 20MHz.

Overshoot: ≤10% above the initial setpoint at application or removal of input power.

Efficiency: ≥80% at maximum current, ≥40% at minimum current

Temperature: +10°C to +60°C, ≥100 LFM air cooling along connector axis.

Over Voltage: Self shut down when the output exceeds 10% to 20% of nominal.

Short Circuit: Continuous short circuit mode-without damage or overstress to the unit.

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS

UNITRODE PENTIUM®PRO VRM DEMONSTRATION KIT			
REF.DES.	**DESCRIPTION**	**PACKAGE**	**NOTES**
U1	Unitrode UC3910DP 4-BIT DAC and Voltage Monitor	SOIC-16	
U2	Unitrode UC3886DP ACM PWM Controller	SOIC-16	
U3	Unitrode UC3612DP Dual Schottky Diode	SOIC-8	
C01	0.10µF Ceramic	1206 SMD	
C02	0.10µF Ceramic	1206 SMD	
C03	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C04	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C05	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C06	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C07	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C08	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C09	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C10	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A	
C11	0.10µF Ceramic	1206 SMD	
C12	0.10µF Ceramic	1206 SMD	
C13	0.10µF Ceramic	1206 SMD	
C14	0.10µF Ceramic	1206 SMD	
C15	2700pF Ceramic	0603 SMD	
C16	1200pF Ceramic	0603 SMD	
C17	1000pF Ceramic	0603 SMD	
C18	0.01µF Ceramic	0603 SMD	
C19	0.10µF Ceramic	1206 SMD	
C20	100pF NPO Ceramic	0603 SMD	
C21	0.022uF Ceramic	0603 SMD	
C22	0.10µF Ceramic	1206 SMD	
C23	0.10µF Ceramic	1206 SMD	

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS (cont.)

REF.DES.	DESCRIPTION	PACKAGE	NOTES
C24	180pF NPO Ceramic	0603 SMD	
C25	220pF NPO Ceramic	0603 SMD	
C26	NOT USED	0603 SMD1	
C27	180pF NPO Ceramic	0603 SMD	
C28	1000pF NPO Ceramic	0805 SMD	
C29	Sprague/Vishay 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD	
SCR1	Motorola MCR12D, 12A SCR	TO-220AB	2
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB	
CR1-HS	AAVID 577002 TO-220 Heat Sink		
CR2	1N5401CT, 3A 100V Diode	DO-201AD	2
F1	Littlefuse R451010, 10A Fast Blow	SMD Square	2
J1	AMP 532956-7 40 Pin Connector		
L1	Coilcraft S6030-B, 10µH to 20µH	Radial Toroid	
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB	
Q1-HS	AAVID 577202 TO-220 Heat Sink		
R01	Dale/Vishay WSR-2 0.01W 1%	SMD Power Package	3
R02	1.00kW, 1%, 1/16 Watt	0603 SMD	
R03	6.8kW, 5%, 1/16 Watt	0603 SMD	
R04	10W, 5%, 1/16 Watt	0603 SMD	4
R05	27W, 5%, 1/16 Watt	0603 SMD	2
R06	100W, 5%, 1/16 Watt	0603 SMD	2
R07	NOT USED	0603 SMD	5
R08	1.69kW, 1%, 1/16 Watt	0603 SMD	
R09	1.37kW, 1%, 1/16 Watt	0603 SMD	
R10	54.9kW, 1%, 1/16 Watt	0603 SMD	
R11	24W, 5%, 1/16 Watt	0603 SMD	8
R12	10W, 5%, 1/16 Watt	0603 SMD	
R13	10kW, 5%, 1/16 Watt	0603 SMD	
R14	15.0kW, 1%, 1/16 Watt	0603 SMD	
R15	3.92kW, 1%, 1/16 Watt	0603 SMD	
R16	100kW, 1%, 1/16 Watt	0603 SMD	
R17	487kW, 1%, 1/16 Watt	0603 SMD	
R18	4.22kW, 1%, 1/16 Watt	0603 SMD	
R19	4.22kW, 1%, 1/16 Watt	0603 SMD	
R20	33.2kW, 1%, 1/16 Watt	0603 SMD	
R21	33.2kW, 1%, 1/16 Watt	0603 SMD	
R22	NOT USED	0603 SMD	1
R23	1.24kW, 1%, 1/16 Watt	0603 SMD	
R24	10.5kW, 1%, 1/16 Watt	0603 SMD	
R25	NOT USED	0603 SMD	
R26	27W, 5%, 1/16 Watt	0603 SMD	6
Z1	10W, 5%, 1/16 Watt	0603 SMD	7

Notes:
1) R22 and C26 are not required. These parts can be used for alternative compensation schemes.
2) These parts are related to the overvoltage protection SCR firing circuit.
3) Simulate a "4 wire" connection using PCB etch for best results.
4) R04 used for debug purposes. R04 is not required in a production unit.
5) R07 can be used to pull up the PWRGOOD signal internally to the VRM
6) R26 is not required for proper operation. R26 is used as a "jumper".
7) Z1 used for debug purposes. Z1 can be used for alternative compensation, or shorted in a production unit.
8) R24 is not required for production unless synchronization is used.

POWER CONVERSION ARCHITECTURE

Topology: Single Switch Buck Regulator

Power conversion from either +5 volts or +12 volts to the lower voltages required by the Pentium®Pro can be accomplished by either a linear regulator or by a myriad of switching converter topologies. Linear regulation is not appropriate because of its inherently poor efficiency. Transformer coupled switching topologies are not required, and not desired, because of the common input and output grounding system. Either a single switch or a synchronous rectifier (two switch) buck regulator are the most appropriate choices for this application. Higher efficiency can be achieved with synchronous rectification, but is not required in this application because the efficiency goal is 80%. The added cost and complexity of a second N-MOSFET is therefore not justified.

Input Voltage: +5 Volts Provides Power, +12 Volts provides Bias and Drive

Either the +5 volt or the +12 volt power bus can be used for this single switch Buck regulator. An N-channel MOSFET is chosen as the switch because of the efficiency of low R_{DSon} N-MOSFETs. The +12 volt bus can be used to drive the N-MOSFET in a +5V input Buck regulator, whereas a +12V input Buck regulator would require a higher voltage (17-20 volts) to provide drive to the switch. Several other considerations are made in choosing the input voltage, including:

- +12V input would require a larger output inductor for a given ripple current.
- +5V input operates at higher duty cycles, reducing power in the freewheeling diode, whereas +12V input operates at lower duty cycles, reducing power in the MOSFET.
- The combined power dissipated of the freewheeling diode plus the MOSFET is less with a +5V input than with a +12V input.
- +5V typically has better power distribution on a motherboard, and within a system, even considering the higher DC currents involved when converting power from +5V.
- The input capacitors will see the same RMS switching current at either voltage.
- +5V has six dedicated input pins whereas +12V has only two. Using +5V as an input voltage will result in fewer amps/pin and a lower impedance path to the source.
- +12V busses can often withstand larger voltage deviations due to the loading effects of the Pentium®Pro.

Control Method - Average Current Mode Control Using the UC3886

Average Current Mode control, as implemented with the UC3886, offers the advantages of optimization of the control loop, very fast amplifiers for a fast transient response, and accurate current limiting. Application Note U-140 [2] discusses the many advantages of Average Current Mode control over both Peak Current Mode control and Voltage Mode control.

Switching Frequency - 200kHz

Several considerations in choosing 200kHz as the switching frequency are:

1. An upper bound on frequency is derived from the gain required by the UC3886 Average Current Mode control current sense amplifier. This upper bound will be shown to be 312kHz.
2. A high switching frequency is desired for
   - Minimum output inductor size
   - Maximum control loop bandwidth
3. A low switching frequency is desired for
   - Keeping switching losses low, although switching losses in the semiconductors is not a significant factor in this application because the input voltage (+5V) is very low.
   - Reducing noise when using a 2-layer printed circuit board.
4. The use of Aluminum Electrolytic capacitors is favored for both input and output capacitors in this application because of the height allowed, their high Capacitance-to-ESR and Capacitance-to-ESL ratios and their ripple current capabilities. Surveying several suppliers of Aluminum Electrolytic capacitors revealed that they have significantly low impedance and optimal ripple current handling at 100kHz to 200kHz, where ESR is minimal.

POWER STAGE COMPONENT SELECTION

The power stage components consist of the input and output capacitors, switch, freewheeling diode, output inductor and sense resistor, and are chosen to be leaded devices for the most part because of the height allowed in this design. The semiconductors are first chosen to meet a full load efficiency goal of 80% and to provide reliable operation at full load. The output inductor is then chosen to provide low output current ripple into the capacitors and for continuous mode operation of the

Buck regulator. The output capacitors are chosen to provide an extremely low output impedance for low voltage ripple and low voltage droop during and output load transient. Finally, the input capacitors are chosen to handle the high level of ripple current demanded by the Buck regulator and to heavily filter the input voltage from both high and low load transients.

Efficiency/Power Dissipation Budget

The desired efficiency goal of ≥80% at full load operation will govern how many of the power stage components are selected. Efficiency goals are set at a nominal input voltage of +5.00V, an output voltage of 3.1V, +25°C ambient temperature and at a maximum load current of 11.2A.

The nominal output power of the power supply is equal to 3.1V • 11.2A = 34.72 Watts. From the desired efficiency, the input power at full load is

$$P_{IN} = \frac{P_{OUT}}{0.8} = \frac{34.72W}{0.8} = 43.4 \text{ Watts}$$

The power dissipated is 8.68 Watts, at full load. An example efficiency budget is shown in Table 2.

Power Stage Component Design Details

Freewheeling Diode: CR1

International Rectifier 32CTQ030 or equivalent, 2 legs paralleled

$V_F \approx 0.35V$ @ $T_J = 115°C$

$T_{Jmax} = 150°C$

Heat Sink = AAVID P/N 577002 or equivalent

Low voltage schottky technology is chosen to maximize the efficiency of the power supply, based on its lower forward voltage and lack of reverse recovery losses.

The operating duty cycle for this Buck converter is derived based on the equation[3]

$$D = \frac{V_O + I_O \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_O \bullet R_{DSon}) + V_F}$$

Likewise, the short circuit operating duty cycle is given by

$$D_{SC} = \frac{0.0V + I_{SC} \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_{SC} \bullet R_{DSon}) + V_F}$$

Given R_{SENSE} = 0.01

R_{LOUT} = 0.012 at 25°C, full load current

V_F = 0.35V at full load, 0.25 at minimum load

I_{SC} = 12.5A Nominal Short Circuit Current

V_{IN} = 5.00V Nominal

R_{DSon} = 0.025 at 110°C

V_O = 3.10V Nominal

Then typical duty cycles will be approximately:

Operating: ≈ 73% at Full load, 25°C T_A

≈ 64% at minimum load, 25°C T_A

Short Circuit: ≈ 13%

The maximum operating power dissipation at the diode's maximum operating junction temperature of 110°C is given by

$$P_{Dmax} = V_F \bullet I_{Omax} \bullet (1 - D_{max})$$
$$= 0.35V \bullet 11.2A \bullet (1 - 0.73) = 1.06W$$

The power dissipation under short circuit conditions, however, is substantially larger

$$P_{Dsc} = V_F \bullet I_{sc} \bullet (1 - D_{sc}) = 0.35V \bullet 1.12A \bullet (1 \bullet 0.73) = 1.06W$$

Let T_{Jmax} = 115°C under operating conditions and 150°C under short circuit conditions (Rated T_{Jmax} for device)

The two governing formulas defining the heat sink requirements (thermal impedance RθHS) are

115°C = 50°C + 1.06W • (3.0 + RθHS),
RθHS = 58°C/W

150°C = 50°C +3.80W • (3.0 + RθHS),
RθHS = 23.3°C/W

The short circuit operation must be used to choose the heat sink. AAVID P/N 577002 with 100LFM of airflow meets the heat sink requirement of ≤23°C/W. Note that the accurate current limit set

TABLE 2 - POWER DISSIPATION BUDGET

Description	Power Dissipated [W]	Budget Remaining [W]
Budgeted Power		8.68
Estimated 3% Power Distribution (I^2R) Losses	1.1	7.58
Diode Losses	1.1	6.48
Sense Resistor	1.25	5.23
Output Inductor (I^2R)	1.3	3.93
Output Inductor (Core)	0.1	3.83
Input Capacitance Ripple Current Losses	0.5	3.33
UC3886 + UC3910 + Bias loads	0.3	3.03
MOSFET (Switching, Conduction, Gate Drive)	3.03	0.00

point achieved by the UC3886 allows for a minimum heat sink solution.

MOSFET Switch: Q1

International Rectifier IRL3103

$R_{DSon} \approx 0.025\Omega$ Estimated at $V_{GS} = 7V$, $T_J = 115°C$

Q_G (Total Gate Charge) ≈ 50nC estimated at $V_{GS} = 7V$

Heat Sink ≈ AAVID P/N 577202 or equivalent

From the power budget, the MOSFET should be chosen to achieve the desired losses, including the gate drive losses. Choosing a Logic Level MOSFET or a standard threshold voltage MOSFET is discussed in U-156 [3]. This application will utilize a Generation 5 MOSFET from International Rectifier because of its combination of low R_{DSon} at low V_{GS} as well as rated V_{GS} of ±20V.

The power dissipation of the MOSFET consists of 4 components; (a) Gate drive, (b) C_{OSS}, (c) Crossover losses, and (d) Conduction losses

a) Gate Drive losses are given by

$$P_{GATE} = I_{GATEavg} \bullet V_{GS}$$

From the IRL3103 charge curve, with $V_{GS} = 7$ volts, the required total charge, Q_G, is estimated to be 50nC. The average current is given by

$$I_{GATEavg} = Q_G \bullet F_S = 50nC \bullet 200kHz = 10mA$$

$$P_{GATE} = 0.010 \text{ Amps} \bullet 12 \text{ Volts} = 0.12 \text{ Watts}$$

b) Coss losses are due to the discharge of the energy stored in the capacitance Coss each cycle, equivalent to

$$P_{COSS} = 0.5 \bullet Coss \bullet (V_{IN} + V_F)^2 \bullet F_S$$

From the IRL3103 capacitance curve, Coss is estimated to be 2400pF. Therefore,

$$P_{COSS} = 0.5 \bullet 2400pF \bullet (5.35V)^2 \bullet 200kHz = 0.007W.$$

c) Crossover (turn-on and turn-off) losses can be estimated as

$$P_{CROSSOVER} = \frac{1}{6} \bullet (V_{IN} + V_F) \bullet I_O \bullet \frac{T_{RISE/FALL}}{T_S}$$

where $T_{RISE/FALL}$ is the MOSFET current rise and fall time, estimated to be approximately 150ns, and T_S is the switching period. This loss occurs once at turn-on, and once at turn-off, and therefore, for this application

$$P_{CROSSOVER} = 2 \bullet \frac{1}{6} \bullet 5.35V \bullet 11.2A \bullet \frac{150ns}{5\mu s} = 0.6 \text{ Watts}$$

d) Conduction losses are determined by

$$P_{COND} = I_O^2 \bullet R_{DSon} \bullet D_{MAX}$$

and are worst at the maximum operating junction temperature, where R_{DSon} is highest. For the IRL3103, this loss is

$$P_{COND} = 11.2^2 \bullet 0.025\Omega \bullet 0.73 = 2.29 \text{ Watts}$$

$$Pd\_Total\_FET = 2.29W + 0.6W + 0.007W + 0.12W = 3.02W$$

The MOSFET heat sink requirements are determined from

$$115°C = 50°C + 3.02W \bullet (2.0 + R_{\theta HS}),$$
$$R_{\theta HS} = 19.5°C/W$$

AAVID P/N 577202 with 100LFM of airflow provides ≤14°C/W, exceeding the heat sink requirement.

Output Inductor: L1

Coilcraft P/N S6030-B

20µH @ 0 Adc

10µH @11.2 Adc

13 Turns, # 16AWG on Micrometals T60-52D Core

$R_{DC} \leq 0.008\Omega$ max, 20°C Ambient

$T_{RISE} \approx 40°C$ at maximum load

The output inductor of a Buck regulator is often chosen to maintain continuous current in the inductor under minimum load conditions. The ripple current in the inductor under minimum DC current conditions is equal to $2 \bullet I_{MIN}$ for this rule to apply. For this power supply, L_{OUT} is determined by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT}) \bullet Duty}{2 \bullet I_{MIN} \bullet F_S} = \frac{(5V - 3.1V) \bullet 0.64}{2 \bullet 0.3A \bullet 200kHz} = 10.1\mu H \text{ @ Low Load}$$

A second condition for choosing the output inductor value is to limit the input current to the power supply during a step change in current from I_{MIN} to I_{MAX}. After a step change in load current, the duty cycle of the Buck regulator responds by assuming a maximum duty cycle of 100%. The input current therefore equals the output inductor current. To limit the input current rate to the required 0.1A/µs, the output inductor is chosen by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT})}{di/dt} = \frac{(5V - 3.1V)}{0.1A/\mu s} = 19\mu H$$

A toroidal inductor design is used to meet these needs. The form factor allows a component height of 0.800", thus allowing a sizable inductor that can be designed for low cost and simple winding techniques. The inductance vs DC current is shown in Figure 3. The inductor must not saturate with DC

current equal to the power supply short circuit current limit, or the current limiting will not be effective.

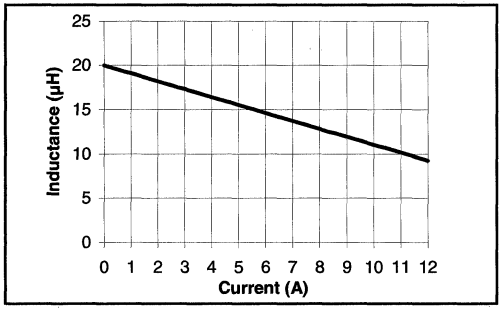

Figure 3. Output Inductor Performance vs DC Current - No AC Flux

The in-circuit inductance will tend to be higher due to the AC Flux imposed by the volt-seconds product of the Buck regulator. Micrometals -52 material's permeability increases substantially with AC Flux. This same effect of AC Flux on the permeability of the -52 material plays a major role during the transient load response of the power supply. During a transient load response, the voltage differential across the output inductor is approximately V_{IN}-V_{OUT}. The duration of the transient response, in excess of 100µs, means that the AC Flux on the core for this time is given by

$$\Delta B_{AC} = \frac{(V_{IN} - V_{OUT}) \bullet T_{LOUT} \bullet 10^8}{N \bullet Ae}$$

$$= \frac{(5V - 3.1V) \bullet 100\mu s \bullet 10^8}{13Turns \bullet 0.374\ cm^2}$$

$$= 3908\ Gauss$$

which, according to Micrometals [3] results in multiplying the output capacitance by approximately 260%. This results in a dynamic inductance, during a load step, of approximately 26µH. This feature will play an important role in the selection of the output capacitors to meet the transient load performance.

Output Capacitors: C06-C09, C11, C12, C29

SANYO - 6MV1500GX - 4 in Parallel
C = 1500µF
Form Factor = 10x20mm, Radial
ESR = 0.044Ω
ESL ≈ 4nH (Estimated)
Ripple Current Rating = 1.25A @ 105°C, 100kHz

Choosing the output capacitors for this regulator may be the single most important decision with regards to meeting the transient load behavior of the Pentium®Pro. The transient load step of the Pentium®Pro is so large and so fast that there is no control loop which can respond quickly enough and maintain regulation. Capacitance, providing a low impedance output, is therefore the best solution to maintaining the proper output voltage.

Understanding the Response to a Step Load

During a step load change from minimum to maximum current, the output of the power supply can be modeled as shown in Figure 4. Prior to the change in load current, the average current in the output inductor is I_{MIN} and the average current in the output capacitor is 0 amperes. Once the load current changes from Imin to I_{MAX}, the parasitic components shown in Figure 4 have a large affect on the output voltage.

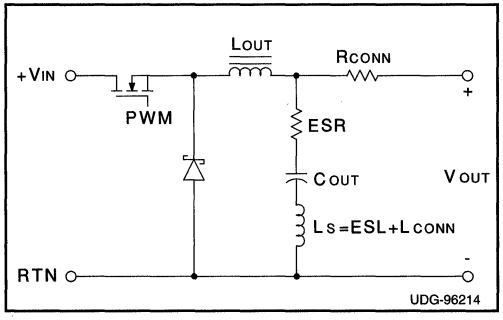

Figure 4. Large Signal Transient Model of Power Supply Output Stage

The VRM connector pins have parasitic resistance and inductance termed R_{CONN} and L_{CONN}. The parasitic inductance of the connector and the output capacitors (ESL) are summed together as L_S. ESR and R_{CONN} cannot be combined in the capacitor path as this would result in a DC load regulation error.

Figure 5 below illustrates the complexity of the output voltage waveform during a step in the output load current. A power supply with excellent load regulation is assumed for the purposes of understanding these dynamics. Reducing the load regulation through non-integrating [3] voltage loop gain will be discussed later in this application note. The output voltage responds to the load current step in four distinct phases, T_{STEP}, T_{LOOP}, T_{LOUT} and T_{CHARGE}.

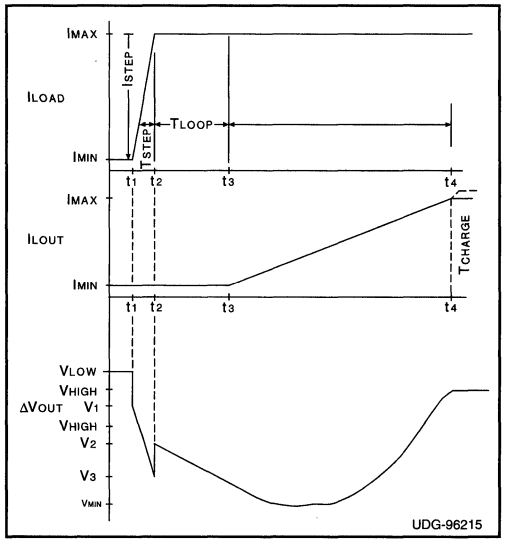

Figure 5. Dynamics of a Step Load

Phase 1, the step current phase from t_1 to t_2 (T_{STEP}), is characterized by a specified change in current and rise time. The response of the output voltage consists of:

a) A voltage step proportional to the parasitic circuit inductance, L_S.
b) A ramp in voltage proportional to the parasitic circuit resistance, R_S, where $R_S = R_{CONN} + ESR$.
c) A droop in voltage proportional to the power supply output capacitance.

The response of the output voltage during the time t_1 to t_2 is therefore given by

$$\Delta V_{OUT} = L_S \bullet \frac{\Delta I}{\Delta T} + i(t) \bullet R_S + \frac{1}{C_{OUT}} \int_{t_1}^{t_2} i(t)dt$$

which, at the end of T_{STEP}, is equal to

$$\Delta V_{OUT} = I_{STEP} \bullet \left(\frac{L_S}{T_{STEP}} + \frac{T_{STEP}}{2 \bullet C_{OUT}} + R_S \right)$$

Phase 2, from t_2 to t_3 (T_{LOOP}), is the time where the load current has settled at its maximum value, I_{MAX}, but the power supply loop has not yet responded. The inductor current is therefore still set at I_{MIN} and the response of the output voltage is therefore determined by

a) A voltage proportional to R_S.
b) A droop in voltage proportional to the power supply output capacitance.

There is an initial discharge of the capacitor at the end of Phase 1 which is the initial condition for Phase 2, determined by

$$\Delta V\_Phase1 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt$$

$$= \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}}$$

The response of the output voltage during the time t_2 to t_3 is therefore given by

$$\Delta V_{OUT} = \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}} + \frac{1}{C_{OUT}} \int_{t_2}^{t_3} i(t)dt + R_S \bullet$$

$$I_{STEP} = I_{STEP} \bullet \left(\frac{T_{STEP}}{2 \bullet C_{OUT}} + \frac{T_{LOOP}}{C_{OUT}} + R_S \right)$$

T_{LOOP}, for the UC3886 Average Current Mode Controller and the compensation components shown in Figure 2, is less than one switching cycle.

Phase 3, from t_3 to t_4 (T_{LOUT}), is the time when control loop has forced the Buck regulator to the maximum duty cycle (100% for the UC3886) and the inductor current is ramping from I_{MIN} to I_{MAX}. The output inductor current during this phase is given by

$$iL_{OUT(t)} = \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

Since the inductor current is ramping up during Phase 3, the capacitor current is ramping down, and is given by

$$iC_{OUT(t)} = I_{STEP} - IL_{OUT(t)}$$

$$= I_{STEP} - \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

The change in output voltage during Phase 3 consists of

a) A voltage drop proportional to ESR and R_{CONN}.
b) A droop in voltage proportional to the output capacitance.

During Phase 3, the voltage drop due to the ESR and the capacitance is changing because the capacitor current decreases. The voltage drop due to R_{CONN} is constant, as it is set by the constant value of R_{CONN} and the maximum load current, I_{STEP}. There is an initial discharge of the capacitor at the end of Phase 2 which is the initial condition for Phase 3, determined by

$$\Delta V\_Phase2 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt + \frac{1}{Cout}$$

$$\int_{t_2}^{t_3} I_{STEP} \, dt = \left(\frac{Istep}{2} \right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}} \right)$$

The change in output voltage during Phase 3 is given by

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{2}\right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}}\right) + \frac{1}{C_{OUT}} \int_{t_3}^{t_4} iC_{OUT(t)}dt + iC_{OUT(t)} \bullet ESR + I_{STEP} \bullet R_{CONN}$$

Which yields

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{C_{OUT}}\right) \bullet \left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) + I_{STEP} \bullet \left(EST - \frac{ESR \bullet t}{T_{LOUT}} R_{CONN}\right)$$

T_{LOUT} is defined as the time it takes for the inductor current to equal the change in load current, I_{STEP}.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

Phase 4, T_{CHARGE}, is the time when the inductor current overshoots to reach the programmed short circuit current limit in order to replace charge lost by the output capacitor. At the end of phase 4, the output voltage drop settles to

$$\Delta V_{OUT} = I_{STEP} \bullet R_{CONN}$$

The duration of phase 4 is determined by

$$I_{Cout} = C_{OUT} \bullet \frac{dv}{dt}$$ which yields a time of

$$T_{CHARGE} = \frac{C_{OUT} \bullet \Delta V\_Phase3}{(I_{SC} - I_{MAX})}$$

where I_{SC} is the programmed short circuit current limit, and ΔV_Phase3 is the voltage at the end of phase 3, determined by

$$\Delta V\_Phase3 = \frac{I_{STEP}}{C_{OUT}} \bullet \left(\frac{T_{LOUT}}{2} - \frac{T_{STEP}}{2} + T_{LOOP}\right)$$

Procedure for Determining the Required Output Capacitor(s)

Step 1: Determine the parasitic values of R_{CONN} and L_{CONN}. The following are estimates based on the connector pair used and the printed circuit board.

Resistance per pin ≈ 10mΩ

Resistance per mated pin set ≈ 20mΩ

Inductance per mated pin set ≈ 4.28nH

Number of output pins = 11 pairs in parallel

Resistance of printed circuit board to the connector ≈ 0.2mΩ

Inductance of printed circuit board to the connector ≈ 0.2nH

$$R_{CONN} = \frac{20m\Omega}{11} + 0.2m\Omega = 2.02m\Omega$$

$$L_{CONN} = \frac{4.28nH}{11} + 0.2nH = 0.59nH$$

Step 2: Establish an allowable maximum voltage drop, ΔV_{OUT}, at the output.

Application Note U-156 [3] discusses the use of non-integrating gain which allows a larger voltage deviation during a load transient. Set the minimum load regulation to be V_{NOM} +3% ±1%. Therefore, a -7% voltage deviation is allowed on the output voltage while still meeting a minimum overall voltage of -5%. Voltage ripple is not considered during this transient response as the duty cycle is effectively 100%, and there is no voltage ripple. These limits are illustrated in Figure 6.

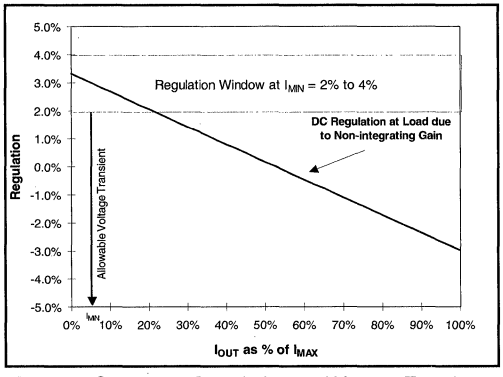

Figure 6. Setting the Regulation and Voltage Transient Requirements

$$\Delta V_{OUT} = 0.07 \bullet 3.1V = 0.217 \text{ volts}$$

Step 3: Estimate the total parasitic inductance, L_S, in order to derive a required value of R_S from the voltage step at the end of Phase 1. Aluminum electrolytic capacitors, size 10mm x 20mm, are estimated to have an ESL of approximately 4.0nH. Size 1206 ceramic chip capacitors are estimated to

have an ESL of approximately 1.9nH [1]. Assume that the combined ESL will be less than 0.51nH, for a total parasitic inductance

$L_S = 1.10nH$

This value must be insured to maintain overall regulation limits during the first phase, T_{STEP}.

Step 4: Equate the voltage deviation at the end of Phase 1 to the allowed voltage step. Assume that the change in voltage due to capacitive discharge is less than 1% of the overall change.

Therefore, the minimum value of C_{OUT} is equal to

$$C_{OUTmin} = \frac{10.9A \bullet 360ns}{2 \bullet 0.217V \bullet 0.01} = 904\mu F$$

Solving for the maximum value of R_S for a step of 11.2A – 0.3A = 10.9A yields,

$$R_S = \frac{(0.217V \bullet 0.99) - \left(10.9A \bullet \frac{1.1nH}{360ns}\right)}{10.9A}$$

$$= 16.6m\Omega$$

Step 5: Equate the voltage deviation at the end of Phase 2 to the allowed voltage step, from which a minimum value of C_{OUT} can be obtained

$$0.217V = \left(\frac{10.9A}{2}\right) \bullet \left(\frac{2 \bullet 5.0\mu s - 360ns}{C_{OUTmin}}\right) + (13.8m\Omega \bullet 10.9A)$$

$$C_{OUTmin} = \frac{\frac{10.9A}{2}(2.5\mu s \bullet 360ns)}{0.217V - (16.6m\Omega \bullet 10.9A)}$$

$$= 1457\mu F$$

Step 6: Choose a capacitor type, manufacturer(s) and values. Determine the number of capacitors required to meet the ESR requirements from Step 4 and the minimum capacitance requirements from Step 5. Add 20% margin for variations in ESR from 20°C down to 10°C (minimum operating temperature).

Radial, high frequency aluminum electrolytic capacitors are chosen based on the height allowed for this power supply VRM as well as their inherently low ESR and ESL. Many manufacturers offer 6.3V low ESR devices rated for 100kHz - 200kHz operation. Sanyo's MV-GX series of aluminum electrolytic capacitors are chosen based on their lower ESR specifications.

ESR Required = 16.6mΩ • 0.8 = 13.3mΩ

Sanyo MV-GX 1500µF, 10mm x 20mm, 6.3V device has a rated maximum ESR of 44mΩ. 4 devices are required, using 400mm² of board area. Sanyo MV-GX 1000µF, 8mm x 20mm, 6.3V device has a rated maximum ESR of 64mΩ. 6 devices are required, using 384mm² of board area. The 1500µF device is chosen to reduce the total parts count. The solution is:

$C_{OUT} = 1500\mu F \bullet 4 = 6000\mu F$

$ESR = 44m\Omega / 4 = 11.0m\Omega$

$ESL \approx 4nH / 4 = 1.0nH$

Step 7: Determine the voltage waveform at the output given this solution of output capacitors.

The current in the capacitor, during a transient, ramps up (or down) in a time determined by the output inductor. The output inductor, during a transient load step, is approximately 26µH.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

$$= \left(\frac{10.9A}{(5.0V - 3.1V)}\right) \bullet 26\mu H = 149\mu s$$

The capacitor current is defined as

$$iC_{OUTt} = I_{STEP} - \frac{I_{STEP}}{T_{LOUT}} \bullet t$$

The voltage drop at the output of the power supply, during Phase 3 (T_{LOUT}) of the load transition, is determined by

$$\Delta V_{OUT} = \frac{I_{STEP}}{C_{OUT}} \bullet \left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) + I_{STEP} \bullet \left(ESR - \frac{ESR \bullet t}{T_{LOUT}} + R_{CONN}\right)$$

The entire voltage response is plotted in Figure 7. Ceramic and tantalum capacitors (C11, C12, C29) are added in parallel to the aluminum output capacitors to reduce the overall ESL to less than the required

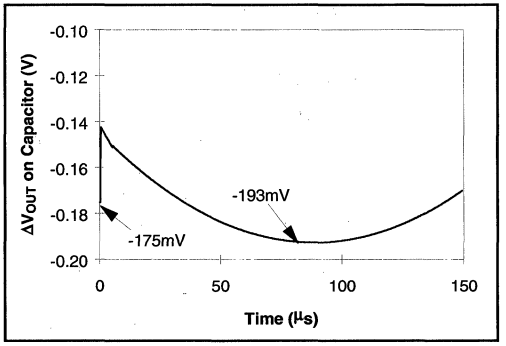

Figure 7. Voltage Droop on Power Supply Output during Load Transient

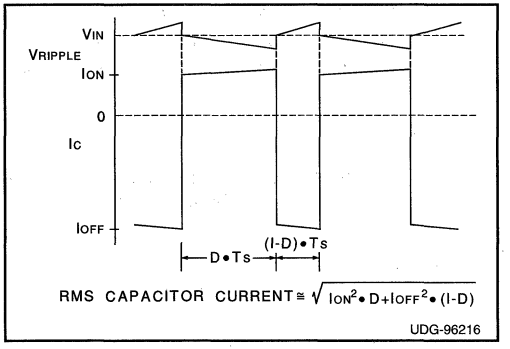

Figure 8. Input Capacitor(s) Current Waveform

0.51nH and to reduce high frequency noise to meet the ripple requirement of ≤2% peak-to-peak.

Input Capacitors: C01-C05

SANYO - 6MV1500GX - 3 in Parallel

C = 1500µF

Form Factor = 10 x 20mm, Radial

ESR = 0.044Ω

ESL ≈ 4nH (Estimated)

Ripple Current Rating = 1.25A @ 105°C, 100kHz

The input capacitance for a Buck regulator is chosen based on several criteria:

a) Ripple Current Handling at F_{SWITCH}
b) Ripple voltage at F_{SWITCH}
c) Maintaining Input voltage during load transients

The resulting solution must present a very low impedance to the input supply and to the Buck Regulator, resulting in a need for low ESR, large value capacitors.

Ripple Current and Voltage

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability. With just 10's of nanohenries parasitic input inductance the input capacitors must handle virtually all of the 200kHz switching current.

Figure 8 shows the switching waveforms in the input capacitor(s). The average VRM power supply input current is calculated based on the maximum load of the power supply and the efficiency at maximum load.

$$I_{AVG} = \frac{P_{INPUTmax}}{V_{INPUT}} = \frac{I_{Omax} \bullet V_{OUT}}{Efficiency \bullet V_{INPUT}}$$

$$= \frac{11.2A \bullet 3.1V}{0.80 \bullet 5.0V} = 8.68A$$

During the MOSFET ON time, the input capacitors must provide the difference between the load current and the input current. During the MOSFET OFF time, the capacitor current is the complete input average current. Therefore,

$$I_{ON} = I_{Omax} - I_{AVG} = 11.2A - 8.68A = 2.52A$$
$$I_{OFF} = -I_{AVG} = -8.68A$$

The duty cycle at the maximum operating current is approximately 73%, and therefore the RMS current in the capacitors, assuming a rectangular waveform since the current ramp is very small, is given by

$$I_{RMS} = \sqrt{I_{OFF}^2 \bullet (1 - Duty) + I_{ON}^2 \bullet Duty}$$
$$= 5.0\ A_{RMS}$$

Three (3) Sanyo capacitors are chosen to maintain reliable operation while operating at this RMS current level.

Given the current waveform of Figure 8, the input voltage ripple will be proportional to the input capacitance and ESR, as shown in the voltage waveform of Figure 8. Low ESR and high capacitance will keep the ripple voltage low.

C01 and C02 ceramic capacitors are added to filter high frequency noise from the switching power supply from the +5V input power bus.

Filtering V_{INPUT} During Load Transients

During a low-to-high output load transient, the duty cycle goes to 100% until the output inductor current is equal to the load current, and the output inductor limits di/dt of the input current. During a high-to-low output load transient, however, there is no output

inductor limiting the input current rate because the input switch is opened (0% duty cycle). The result is the +5V bulk power supply will continue to source high current into this power supply for some time. Figure 9 illustrates the difference in the circuits between a low-to-high and a high-to-low load transient.

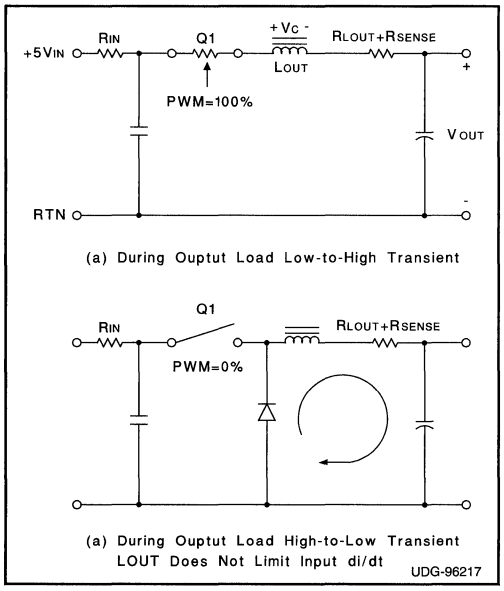

Figure 9. Lout limits the input current only on a low-to-high output current transient

Figure 10 shows typical current waveforms during a high-to-low load transient. The output current abruptly stops but the +5V bulk power supply takes a finite time to react to this change in load current, therefore sourcing energy into the input capacitors. Intel specifies that this input current must not change at a rate faster than 0.1A/µs.

The input capacitor(s) are chosen to limit the voltage surge on the input capacitors to less then 0.15

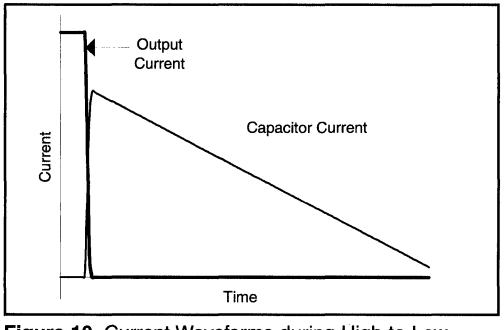

Figure 10. Current Waveforms during High-to-Low Output Transient

volts (3% of V_{IN}) during a high-to-low load transient. The current in the capacitor(s) is defined as

$$iC_{IN(t)} = I_{AVG} - I_{In\_Rate} \bullet t$$
$$= 8.68A - (0.1A/\mu s) \bullet t$$

where I_{In_Rate} is defined as the rate at which the input current decays based on the +5V bulk power supply, assumed here to be 0.1A/µs, therefore decaying to 0.0A in 86.8µs.

The voltage surge on the input capacitance during this time is

$$vC_{IN(t)} = \frac{1}{C_{IN}} \int_0^{86.8\mu s} = iC_{IN(t)} + (ESR_{IN} \bullet iC_{IN(t)}) =$$

$$\left(\frac{8.68}{Cin} - (10^5 \bullet ESR)\right) \bullet t - \left(\frac{10^5 \bullet t^2}{2 \bullet C_{IN}}\right) + 8.68 \bullet ESR$$

which is plotted in Figure 11 for 3 Sanyo MV-GX type 1500µF, 0.044Ω Aluminum Electrolytic Capacitors.

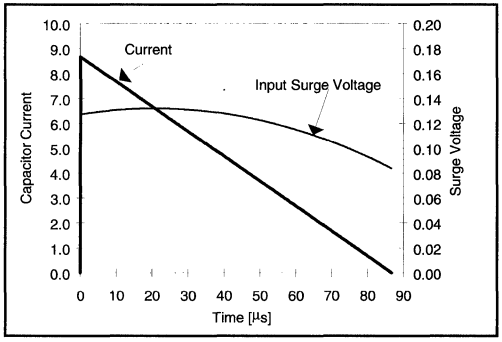

Figure 11. Input Capacitor Current and Surge Voltage During a High-to-Low Load Transient

Sense Resistor: R01

Dale P/N WSR-2 0.01Ω 1%

10mΩ, 2.0 watt 2 wire SMD sense resistor, ±75ppm TCR

The sense resistor is chosen by the criteria discussed in U-156, Appendix 5 [3]. R_{SENSE} is a 2-wire, 2 watt surface mount power product with very low inductance. The 2 watt rating (to ambient temperatures of 75°C) allows for 50% derating at the typical maximum current of 9.9 Amperes [1].

A short circuit current, I_{SC}, is chosen at a nominal 12.5 Amperes, more than 10% over the maximum current. The value of the UC3886 Current Amplifier's gain, G_{CSA}, is bounded to

$$G_{CSA\_MIN} = 5.0 \text{ and } G_{CSA\_MAX} = 2.5MHz/200kHz$$

From

$$G_{CSA} \bullet R_{SENSE} = \frac{1.0\ Volt}{I_{SC}}$$

A 12.5A limit implies that Rsense must lie between 0.0064Ω and 0.016Ω. Choose 0.010Ω as the lowest standard value.

The power dissipation in R_{SENSE} during normal and short circuit conditions is

Normal:

$$P_D = I_{AVG}^2 \bullet R_{SENSE} = 9.9^2 \bullet 0.010\Omega$$
$$= 0.98\ Watt = 49\%\ of\ rated$$

Short Circuit:

$$P_D = I_{SC}^2 \bullet R_{SENSE} = 12.5^2 \bullet 0.010\Omega$$
$$= 1.56\ Watt = 78\%\ of\ rated$$

CONFIGURING THE UC3910 4-BIT DAC AND VOLTAGE MONITOR AND THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

With the power stage chosen, the UC3910 and UC3886 are ready to be programmed for the proper operation. Figure 12 and Figure 13 show block diagrams for the UC3886 and the UC3910 ICs.

Grounding

The UC3886 signal ground (SGND) pin as well as the UC3910's two ground pins are referenced to the output voltage return path for best regulation and noise immunity. The PGND pin of the UC3886 is referenced to the input voltage return path, as discussed in U-156 [4], for best gate drive performance.

Decoupling

High frequency decoupling is provided at the VCC power pins (C14, C18) and the VREF pins (C13, C17) of both ICs. VCC is decoupled to PGND on the UC3886 additionally with a low ESR 0.1μF capacitor (C19) to provide a low impedance gate drive source.

Set the UC3886 Oscillator Frequency to 200kHz

During a load transient, a very high duty cycle is desired. Therefore, set the maximum duty cycle to 99%. From the UC3886 Data Sheet:

$$D_{MAX} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)} = 0.99 \rightarrow$$

$$R_T = \frac{2.0V}{(1 - D_{MAX}) \bullet 4.0mA} = 50k\Omega$$

$$C_T = \frac{2.0V \bullet ((4.0mA \bullet R_T) - 2.0V]}{F_S \bullet 1.8V \bullet R_T^2 \bullet 4.0mA} = 110pF$$

Choose C_T = 100pF (C20)
R_T = 54.9kΩ (R10)

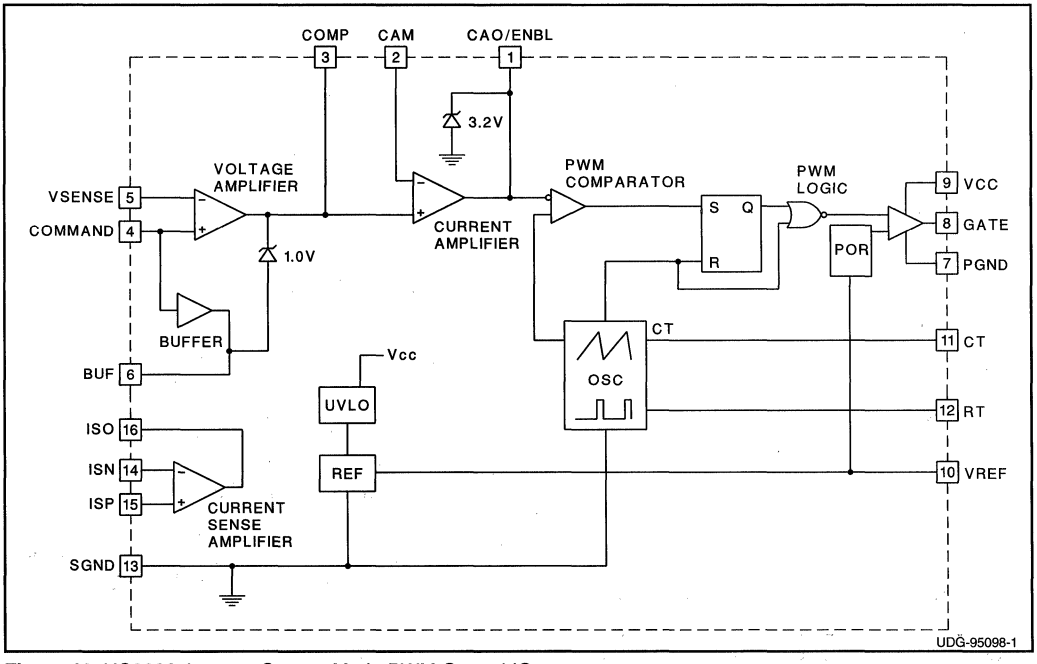

Figure 12. UC3886 Average Current Mode PWM Control IC

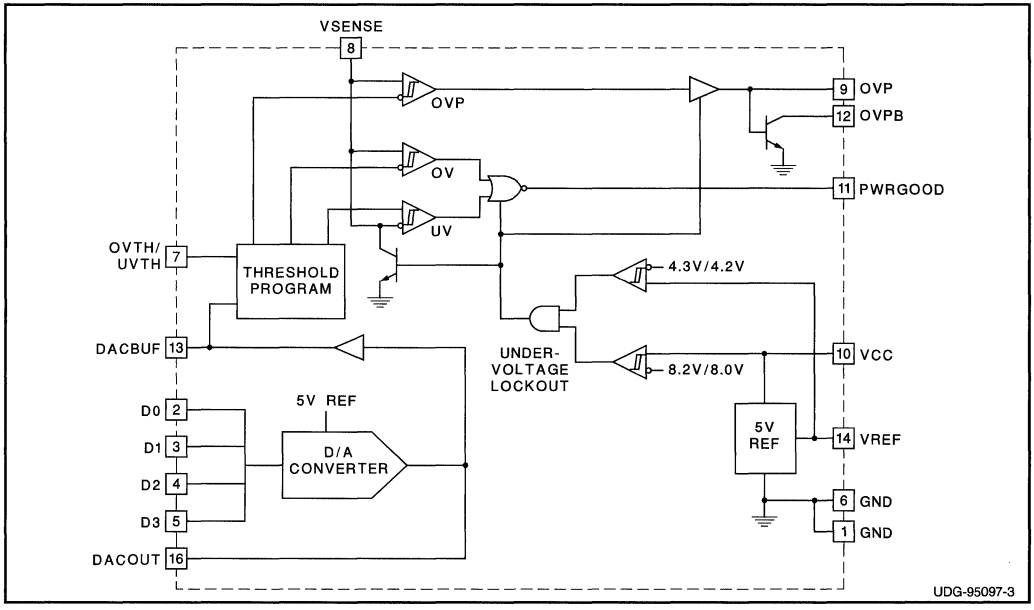

Figure 13. UC3910 4-BIT DAC and Voltage Monitor IC

Note that internal capacitance on the UC3886 CT pin adds approximately 10 to 15pF of capacitance. When using a capacitor as low as 100pF, a substantial frequency shift can result.

A 24Ω resistor and Test Point 1 (R11 and TP1) are provided to allow external synchronization of the unit from a narrow synchronizing pulse [3]. This resistor is not required unless external synchronization is desired.

Driving the MOSFET Gate from the UC3886 Gate Drive Output

A 10Ω gate drive resistor (R12) is placed close to the MOSFET gate. The 10Ω resistor limits the peak current and provides damping at the MOSFET gate to prevent oscillations. The power dissipation in this resistor is approximately 1.0mW based on an average current of 10mA.

Figure 14 shows that the current path for a gate drive signal originates from C19, a low decoupling capacitor located closely to the UC3886 GATE pin. C10 is added from the input voltage to the Power Ground (PGND) to decouple the high frequency current spike which exits the MOSFET from the DRAIN and must find a path back to PGND. C10 should be located as closely as possible to the MOSFET to prevent high frequency ringing at the MOSFET.

U3, the UC3612 dual schottky diode, is added to protect the UC3886 from inductive spikes above V_{CC} and below ground which may occur due to high gate drive spikes and parasitic inductance.

External Enable Signal

Intel specifies [1] that the Pentium®Pro power supply be enabled by an open collector, active high signal, OUTEN.

The UC3886 CAO/ENBL is connected to the input of the UC3886 PWM comparator (Figure 12), with the other side of the comparator attached to the oscillator ramp. The oscillator ramp is nominally a 1.0V to 2.8V peak ramp signal. The UC3886 gate drive is disabled by bringing the CAO/ENBL signal to a level below the oscillator ramp signal.

The external OUTEN signal is connected to the UC3886 CAO/ENBL signal through a 1.0kΩ resistor, R2. A 1.0kΩ resistor is recommended to provide a high impedance buffer between external noise and the output of the UC3886 Current Amplifier Output, to insure noise does not couple into the control loop. The CAO/ENBL pin may source up to 400μA. Using a 1.0kΩ resistor will result in a 400mV drop. A reasonable open collector output stage will be able to sink 400μA and maintain a saturation voltage less than 400mV, keeping the LOW level voltage at CAO/ENBL to less than 800mV.

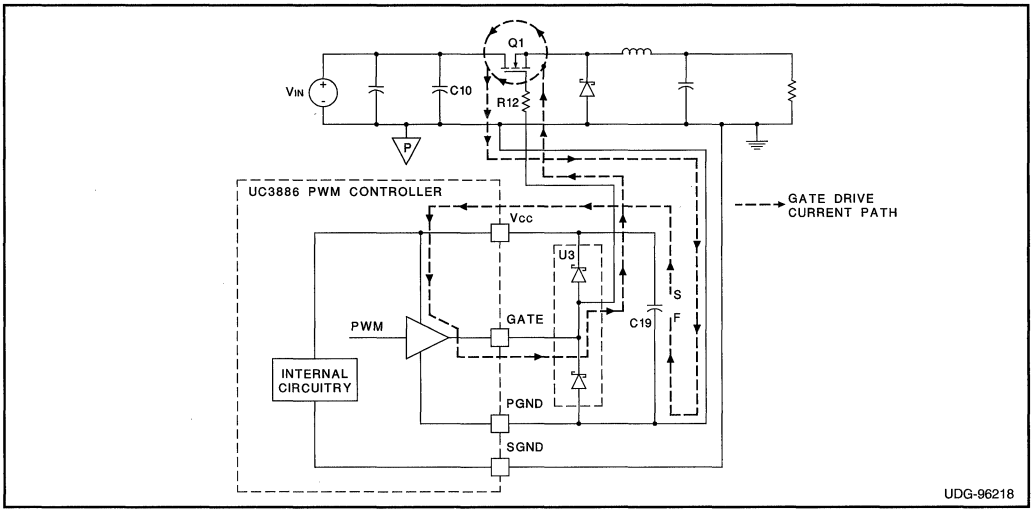

Figure 14. Driving Q1 with the UC3886

External Signal UP#

Intel specifies [1] that the UP# signal be used to disable the power supply if it is not capable of supporting an upgraded processor, either by varying the voltage or by supporting the higher load currents. The UP# signal is also an open collector signal, normally high, but pulled low when an Upgrade Processor is in place. By inserting a 0Ω jumper resistor for R25, the power supply will be disabled in the case of an upgrade processor.

> THE UNITRODE DEMONSTRATION KIT IS SHIPPED WITHOUT R25. UPGRADE PROCESSORS MAY EXCEED THE 12.5A CURRENT LIMIT OF THE DEMONSTRATION KIT. INSERT A 0Ω 0603 SMD JUMPER RESISTOR FOR R25 TO DISABLE THE POWER SUPPLY IN AN UPGRADE PROCESSOR APPLICATION

CONFIGURING THE UC3910 VOLTAGE MONITORING AND PROTECTION FEATURES

The regulation requirements for this power supply are set at ±5%. The PWRGD requirement is set to signal a voltage regulation failure when the output voltage is outside of the range of ±10%. The UC3910 Undervoltage and Overvoltage (UV, OV) thresholds are therefore chosen at midrange to be nominally ±7.5%.

The equations for setting the Voltage Monitoring thresholds (see U-158 [7]) are

$$\%V_{UV} = -\left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega}\right) \bullet 100 = -(R_{DIV} \bullet 16.7)$$

$$\%Vov = R_{DIV} \bullet 16.7$$

$$\%Vovp = R_{DIV} \bullet 33.4 = \%Vov \bullet 2.0$$

Setting $\%V_{UV}$ and $\%V_{OV}$ to ±7.55 yields a divider ratio R_{DIV} of 0.45.

R8 and R9 act as a voltage divider between the UC3910's DACBUF pin and OVTH/UVTH pin. R8 and R9 are chosen to draw approximately 1.0mA.

$R8 = 1.69k\Omega$, $R9 = 1.34k\Omega$, $R_{DIV} = 0.448$

The nominal thresholds are

Overvoltage Threshold	= +7.48%
Undervoltage Threshold	= –7.48%
Overvoltage Protection Threshold	= +14.96%

PWRGD Signal:

Intel requires [1] the PWRGD signal to be an open collector active HIGH signal when the voltage is within specification. R7 is a 4.7kΩ resistor which can be added internally to the demonstration kit power supply for evaluation purposes. See the schematic of Figure 2.

> R7 IS NOT INSTALLED ON UNITRODE'S DEMONSTRATION KIT. USE A 4.7kΩ 1/10W 0603 SMD RESISTOR IF INTERNAL PULLUP IS DESIRED.

Overvoltage Protection:

The UC3910 provides both OVP and OVPB pins for protection in the case of overvoltage. OVP is capable of driving an SCR to perform a crowbar func-

tion. OVPB is an open collector, active low signal which is designed to pull down on the UC3886 CAO/ENBL signal to disable the UC3886 gate drive.

The Overvoltage Protection circuit consists of F1, SCR1, CR2, R05 and R06. Fuse F1 serves to protect the circuit under two circumstances: a MOSFET short circuit failure and when the crowbar SCR is fired. The fuse is chosen based on the maximum operating power and efficiency.

$$P_{OUTmax} = 3.4 \text{ Volts} \bullet 11.2 \text{ Amps} = 38 \text{ Watts}$$

$$I_{INmax} = \frac{38 \text{ Watts}}{0.80 \bullet 5.0V} = 9.5 \text{ Amperes}$$

A 10 Ampere SMD fuse is chosen.

Characterizing SCR's for Crowbar Applications is discussed extensively in Motorola's Thyristor Device Data book [5]. SCR1 is chosen based on its low gate trigger current, its On-State RMS current rating, and because it has to discharge a substantial amount of low ESR aluminum capacitors, its Peak Non-repetitive surge current rating.

SCR1 by itself will not protect the Pentium®Pro processor against an overvoltage except by causing the fuse F1 to open, which can take a substantial amount of time. CR2 provides an additional path to discharge the output capacitors directly in order to clamp the output voltage and protect the processor immediately. CR2 is connected before the sense resistor, R1, in order to use R1 as a current limiting resistor when the crowbar is fired. CR2 has a rated surge current of 200 Amperes.

Connecting an SCR as a crowbar to the output voltage may appear to be the best way to protect the Pentium®Pro processor in the case of an overvoltage failure. However, the UC3886 provides a current limiting mechanism, which would cause the SCR to sink the programmed current limit. An input fuse would not open under these circumstances because of the low output power being delivered. The SCR on the output would most likely fail thermally and open, thus defeating the protection mechanism.

Resistor R6 from the SCR gate to ground is chosen to protect the SCR against false firing due to dv/dt conditions. R6 will draw approximately 15mA when the SCR is fired, as the gate voltage is approximately 1.5 volts. R5 is chosen to limit the current from the UC3910 while insuring that the SCR gate trigger current is sufficient down to 10°C. The UC3910 will source at least 65mA when activated. R5 limits the current preventing excessive droop on VCC when the SCR is fired.

The open collector signal OVPB is also triggered during an overvoltage protection fault. This signal can be used to disable the UC3886 gate drive by connecting it directly to the UC3886 CAO/ENBL signal. R26 is installed in Unitrode's demonstration kit as a "jumper" only, to enable or disable this feature. Normal applications will directly connect the UC3886 CAO/ENBL pin to the UC3910 OVPB pin. Note that the OVPB signal is an open collector signal and therefore may be "OR';d" with the external open collector OUTEN and UP# signals.

Setting the RC Filters at VSENSE and DACOUT of the UC3910

The UC3910 VSENSE pin requires an R-C filter to isolate the pin from the power supply output [6]. The resistor acts both as part of an R-C filter and to limit the current into the VSENSE pin. During UVLO of the UC3910, VSENSE is actively pulled low in order to prevent false overvoltage protection signals.

The filter resistor R3 is chosen to limit the input current to ≤500µA under the maximum programmable voltage for the Pentium®Pro.

$$R3 \quad \frac{3.4V}{500\mu A} = 6.8k\Omega$$

The filter capacitor C16 is chosen to set the filter corner frequency at approximately $F_{SWITCH}/10$ in order to reduce the switching frequency ripple by 20dB.

$$C16 = \frac{1}{R3 \bullet 2 \bullet \pi \bullet (200kHz/10)} = 1170pF$$

Use R3 = 6.8kΩ

C16 = 1200pF as standard values

The filter capacitor at the output of DACOUT, C15, is chosen to insure that DACOUT rises at a faster rate than VSENSE. This prevents false OVP signals during V_{CC} brownout or glitch conditions.

$$R3 \bullet C16 > 3k\Omega \bullet C15 \rightarrow$$

$$C15 \leq \frac{R3 \bullet C16}{3k\Omega} \quad 2720pF$$

Use C15 = 2700pF as a standard value

Note that resistor R4 connected to the UC3910 VSENSE pin is used for debug purposes only and is not required for normal operation.

Programming the Current Limit with the Current Sense Amplifier of the UC3886

A nominal current limit of 12.5 Amperes is desired to protect the power supply under short circuit con-

ditions. Accurate current limiting is advantageous in this Buck regulator as it limits the power dissipated in the freewheeling diode under short circuit conditions.

The gain of the current sense amplifier, G_{CSA}, is set based on the desired current limit and the value of the sense resistor [4], using:

$$G_{CSA} \bullet R_{SENSE} = \frac{1.0\ Volt}{I_{SC}} \rightarrow$$

$$G_{CSA} = \frac{1.0\ Volt}{12.5A \bullet 0.01\Omega} = 8.0$$

The current sense amplifier is configured as a differential amplifier using four external resistors, R18, R19, R20 and R21, with the gain equal to

$$G_{CSA} = 8.0 = \frac{R20}{R18} = \frac{R21}{R19}$$

R20 and R21 should not load down the UC3886 Current Sense Amplifier, and are chosen as 33.2kΩ. Therefore

Use R20 = R21 = 33.2kΩ
R18 = R19 = 4.22kΩ resulting in
G_{CSA} = 7.87 and a nominal short circuit current limit, I_{SC}, of 12.7 Amperes.

The BUF signal at pin 6 of the UC3886 must be filtered by C22 to insure a noise free bias voltage for the current sense signal ISO.

Programming the Non-Integrating Gain for the Voltage Amplifier of the UC3886

Managing the voltage regulation at the load, and maintaining regulation of ±5% involves the use of non-integrating gain about the UC3886 voltage amplifier. Without non-integrating gain, the number of output capacitors must increase. Application note U-156 [4], Appendix 3, details the goals and requirements for programming non-integrating gain.

The specified regulation window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%, reserve ±2% of the specified window. This leaves ±3% of the window for load regulation. The desired regulation performance, versus load current, is shown in Figure 15. Setting the low load regulation to +3% nominally will allow the maximum voltage excursion during a load transient.

The UC3886 error voltage, COMP, will vary with load current from 0.0A to I_{SC} = 12.7A. The change in the error voltage will be

$$\Delta Ve = \frac{I_{MAX}}{I_{SC}} \bullet 0.95V = \frac{11.2\ Amps}{12.7\ Amps} \bullet 0.95V$$

$$= 0.834\ Volts$$

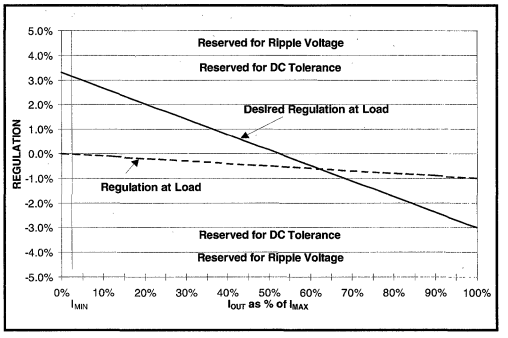

Figure 15. Load Regulation

A change in COMP of 0.95 volts is used because the change is 1.0V ±50mV, and under worst case the regulation window must be held.

Figure 15 shows that the load regulation due to parasitic resistances is –1% from no load to maximum load. From the desired load regulation curve, the swing in output voltage associated with the change from 0 Amps (Not I_{MIN} in this case) to I_{MAX} is determined to be –6.3%. The I • R drop intrinsic to the circuit is then subtracted and the desired regulation swing is set at –5.3%. From the lowest operating voltage, the change in the output voltage is

$$\Delta V_{OUT} = 2.4\ V \bullet 5.3\% = 0.127\ Volts$$

The gain around the Voltage Amplifier determined by the ratio of R16 to R14 is chosen to achieve the desired voltage swing over the operating load range.

$$\Delta V_{OUT} = \frac{\Delta V_E}{Gain} = \frac{\Delta V_E}{R16/R14} \text{ and}$$

$$\text{therefore } R16/R14 = \frac{0.88V}{0.127V} = 6.57$$

The feedback resistor is chosen very large to insure that there are no loading effects on the voltage amplifier output.

Use R16 = 100kΩ
R14 = 15kΩ resulting in the gain about the Voltage Amplifier of 6.67.

Non-Integrating gain has a negative regulation slope with regards to load current, and must be shifted up in order to swing ±3% about the nominal voltage. A DC offset is created by the resistive divider of R14 and R17 which shifts the regulation window up by +3.1%. R17 is chosen by

$$(V_{NOM} + 3\%) \bullet \frac{R17}{R14 + R17} = V_{NOM}$$

and therefore

$$\frac{R17}{R14 + R17} = \frac{1}{1.03}$$ yielding R17 = 487kΩ.

Filtering and Canceling Offset Current at the Command Pin of the UC3886

It is recommended that the decoupling capacitor, C21 be placed very close to the COMMAND pin of the UC3886, as this voltage is the voltage which commands the power supply output, and noise will directly couple to the power supply output. R13 is added in series between the UC3910 DACOUT pin and the UC3886 COMMAND pin in order to minimize DC errors due to offset currents in the UC3886 voltage amplifier. R13 is chosen to match the impedance at the V_{SENSE} input to the UC3886 voltage amplifier. Remember that the UC3910 DACOUT pin has an internal 3kΩ resistor. Therefore

$$R13 = \frac{1}{\frac{1}{R16}+\frac{1}{R14}+\frac{1}{R17}} - R_{DAC} =$$

$$= \frac{1}{\frac{1}{100k\Omega}+\frac{1}{15k\Omega}+\frac{1}{487k\Omega}} - 3k\Omega = 9.7k\Omega$$

Use R13 = 10kΩ

CLOSING THE LOOP WITH THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

The basis for closing the Average Current and the Voltage loops of this circuit is found in Unitrode Application Note U-140 [2] and in the Unitrode Seminar Topic "Switching Power Supply Control Loop Design" [7]. This application note presents a step-by-step methodology solving for the loop compensation components found in Figure 2. The current loop is completed first with the voltage loop to follow.

The goal in closing the loops for this power supply is to obtain a stable closed loop response for the current and voltage loops, with an overall closed loop crossover frequency between 10kHz and

$$\frac{F_S}{2\pi} = 32kHz.$$

Closing the Current Loop

Step 1: Calculate the Oscillator Ramp as seen at the PWM Comparator input. From U-140, it is known that "The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input".

From the oscillator timing equations, the ramp slope is

$$T_S = \frac{1}{F_S} = 5.0\mu s$$

$T_D \approx 50ns$ (Deadtime of oscillator)

Ramp = 2.8V – 1.0V = 1.8Vp-p

$$\text{Ramp Slope} = \frac{\text{Ramp}}{T_S - T_D} = \frac{1.8V}{4.95\mu s}$$

= 0.364 Volts/μs

Step 2: Calculate the inductor current downslope. The downslope occurs during the Buck regulator switch OFF time.

The inductor downslope is maximum at the maximum output voltage and with the minimum output inductance, which occurs at maximum load and maximum output voltage.

The diode forward voltage of CR1 is approximately 0.35V at 11.2A

$V_{OUTmax} = 3.4V$

L_{OUT} at the maximum operating current = 12μH

$$\text{Inductor di/dt} = \frac{3.4V + 0.35V}{12.0\mu H} = 0.313A/\mu s$$

Step 3: Convert the inductor current downslope to a voltage downslope as seen at the output of the Current Sense Amplifier.

Inductor dv/dt = 0.313A/μs • 0.01Ω •

$$\frac{33.2k\Omega}{4.22k\Omega} = 24.6mV/\mu s$$

Step 4: Set the gain from the Current Amplifier to meet the slope criteria. Reduce G_{CAmax} by 25% to account for amplified voltage ripple due to the ESR of the output capacitors. Reduce the gain by 15% more to account for Inductor and Oscillator variations.

The oscillator Ramp Slope = 0.364V/μs ≥ G_{CA} • Inductor dv/dt

where G_{CA} = The gain of the Current Amplifier at the switching frequency

Therefore:

$$G_{CA} \text{ at } F_{SWITCH} = \frac{364mV/ms}{24.6mV/ms} \bullet 0.60 = 8.9$$

Resistors R23 and R24 set the inverting

gain about the UC3886 Current Amplifier. Pick R24 to limit the loading on the Current Amplifier output. Then set R23 and R24 to program the Current Amplifier's inverting gain at F_{SWITCH}.

Use

R24 = 10.5kΩ

R23 = 1.24kΩ

as standard values

G_{CA} = 8.47

The GBW product for the UC3886 Current Amplifier is 3.5MHz and therefore a gain of 8.47 at 200kHz is within the device's GBW.

Step 5: Find the crossover frequency of the current loop gain by first finding the small signal control-to-output gain, G_P, of the buck regulator current loop power section. Consider the fact that the inductor, L_{OUT}, plays a key role in the equation for G_P, and that since L_{OUT} swings significantly with load current, so does G_P.

The small signal control-to-output gain is defined in U-140 from the CA output, V_{CA}, to the voltage across the sense resistor, V_{RS}. The UC3886 application however must add a gain stage factor for the Current Sense Amplifier gain. G_P is determined by

$$\frac{V_{RS}}{V_{CA}} = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet G_{CSA}$$

$$= G_P$$

The change in duty cycle to change in Current Amplifier output is 100%/V_S, or

$$\frac{Duty}{V_{CA}} = \frac{1}{V_S}$$

where

V_S = The peak-to-peak voltage change of the oscillator ramp

The change in the resistor voltage to change in the inductor current is simply the value of the sense resistor, R_S (R_S = R1 in Figure 2).

$$\frac{V_{RS}}{I_{Lout}} = Rs$$

The change in inductor current per the change in duty cycle is a function of the input voltage. The small signal voltage applied at the inductor is simply the small signal changes in V_{IN} • Duty. The change in inductor current per the change in applied inductor voltage (small signal) is given by:

$$\frac{i}{v} = \frac{1}{Z_{OUT}} \text{ where } v = V_{IN} \bullet Duty$$

and therefore $$\frac{I_{Lout}}{Duty \bullet V_{IN}} = \frac{1}{Z_{OUT}}$$

which leads to the transfer function of

$$\frac{I_{Lout}}{Duty} = \frac{V_{IN}}{Z_{OUT}}$$

Z_{OUT} is dominated by the output inductor at frequencies above the L • C resonant frequency, and results in a single pole rolloff due to that inductor, which is what is shown in U-140 as the "$V_{IN/S}$ • L_{OUT}" term. The complete impedance function includes the output Inductor, Capacitor, Sense Resistor, Inductor Resistance, ESR, ESL and Load Resistance. The parasitic resistances will help dampen the response at the resonant frequency and should not be ignored.

The output impedance is given by:

$$Z_{OUT} = s \bullet L_{OUT} + R_S + RLout + \frac{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) \bullet RL}{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) + RL}$$

where

R_{Lout} = DC Resistance of output inductor

C = Output capacitance

ESR = Output capacitance ESR

ESL = Output capacitance ESL

R_L = Load Resistance

Now, solving for the control-to-output gain, G_P (of the Current Loop only),

$$G_p = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet GCSA$$

can be simplified as

$$G_P = \left(\frac{1}{V_A}\right) \bullet (R_{SENSE}) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet G_{CSA}$$

U-140 states to multiply the control-to-output power loop gain, Gp, by the gain of the Current Amplifier to achieve the overall current loop gain.

$$Loop = G_P \bullet G_{CA} = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S\text{-}T_D) \bullet R_S \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Equating the current loop gain to 1 will yield the loop crossover frequency, F_C.

$$1 = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z(2 \bullet \pi \bullet F_C)}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S\text{-}T_D) \bullet R \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Z_{OUT} is dominated by the output inductor in the region of the crossover frequency, and therefore $Z_{OUT(fc)}$ can be replaced by $s \bullet L_{OUT}$

Solving for F_C and simplifying yields:

$$F_C = \frac{V_{IN}}{2 \bullet \pi \bullet (V_O + V_F) \bullet (T_S\text{-}T_D)}$$

Notice that L_{OUT} falls out of the equation, and therefore the only "Load" dependency is in the value of Vf. This is true ONLY if Lout is Constant with load current. If a swinging choke is used, then Lout cannot drop out of the equation.

The crossover frequency of the current loop can therefore be determined by

$$\frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet F_C \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA} = 1$$

and therefore

$$F_C = \frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA}$$

The crossover frequency of the current loop will therefore vary as a function of load, with the minimum crossover frequency at the maximum input voltage and maximum value of L_{OUT}, or at minimum load.

Solving for the crossover frequency:

$$F_{Cmax} = \frac{V_{Imax} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmin}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{5.25V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 120mH} \bullet 7.87 \bullet 8.47$$

$$= 25\ .8kHz$$

$$F_{Cmin} = \frac{V_{Imin} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmax}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{4.75V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 24.0\mu H} \bullet 7.87 \bullet 8.47$$

$$= 11.7kHz$$

where the input voltage is +5V ±5%

Step 6: Add the pole-zero compensation into the Current Amplifier by solving for C_{ZERO} (C25 + C28) and C_{POLE} (C27), and solve for the current loop transfer function.

The zero should be placed at or below the minimum current loop crossover frequency, F_{Cmin}. The value of C_{ZERO} is determined by

$$Czero = \frac{1}{2 \bullet \pi \bullet F_{Cmin} \bullet R24}$$

$$= \frac{1}{2 \bullet \pi \bullet 11.7kHz \bullet 10.5k\Omega}$$

$$= 1296pF$$

Use C_{ZERO} = C25 + C28 = 1220pF (2 capacitors are used to allow tuning of this frequency)

The pole should be placed at $F_S/2$. The value of C_{POLE} is determined by

$$C_{POLE} = \frac{C_{ZERO}}{(2 \bullet \pi \bullet F_S/2 \bullet R24 \bullet C_{ZERO}) - 1}$$

$$= \frac{1220pF}{(2 \bullet \pi \bullet = 200kHz/2 \bullet 10.5k\Omega \bullet 1220pF) - 1}$$

$$= 173pF$$

Use C_{POLE} = C27 = 180pF

The transfer function of the compensated current amplifier is

$$G_{CAs} = \frac{R24 \bullet (C_{POLE} + C_{ZERO}) \bullet s + 1}{s \bullet (C_{ZERO} \bullet R23 \bullet (R24 \bullet s \bullet C_{POLE} + 1)}$$

and the overall current loop is determined by multiplying the control-to-output transfer function by the current amplifier transfer function, or

$$Loop = G_P \bullet G_{CAs} = \left(\frac{1}{V_S} \bullet \frac{V_{IN}}{Z_{OUTs}} \bullet R_S \bullet G_{CSA} \right) \bullet G_{CAs}$$

which is plotted in Figure 16.

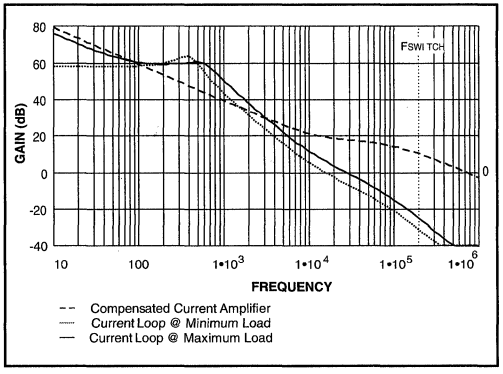

Figure 16. Current Amplifier and Current Loop Bode Plot - Minimum and Maximum Loads

The lower crossover frequency is above the estimated range of 11.7kHz because the gain of the compensated Current Amplifier is not a flat gain of 8.47 but is slightly higher due to the integrating feedback of the Current Amplifier.

The changes in loop gain at low frequencies is dominated by the changes in load resistance, while the variation at and around the crossover frequency is a function of the change in inductance vs current.

Closing the Voltage Loop:

The voltage loop must now be closed according to the guidelines in Unitrode Seminar Topic [7] "Switching Power Supply Control Loop Design". The compensation around the voltage amplifier of this circuit will differ from the seminar topic however by utilizing non-integrating gain [4].

Step 7: Generate a model for the closed current loop transconductance.

The small signal current loop can be modeled as a fixed gain at low frequencies equal the transconductance forced by the current loop, and having a pole at the current loop crossover frequency, f_{CI}, as shown in Figure 17 below.

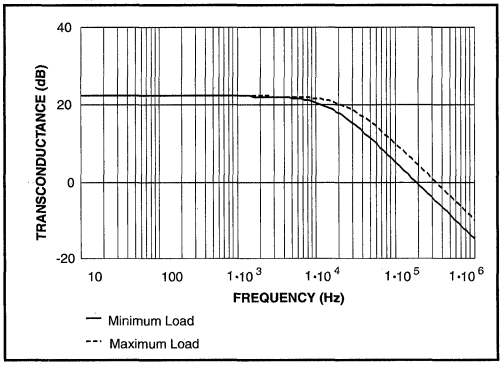

Figure 17. Small Signal Current Loop Transfer Function – Min and Max Loads

where the transconductance, TC(s) is determined by

$$T_{C(s)} = \frac{1}{R_S \bullet G_{CSA}} \bullet \left(\frac{1}{1 + \frac{s}{2 \bullet \pi \bullet f_{CL}}} \right)$$

The low frequency gain is the transconductance (remember, transconductance units is Ω^{-1})

$$Gain = \frac{1}{R_S \bullet G_{CSA}} = \frac{1}{0.01\Omega \bullet 7.87} = \frac{22.1dB}{\Omega}$$

Step 8: Determine the output impedance and power circuit gain, G_{Vs}.

The output impedance is determined by the output capacitance, its parasitics, and the load resistance.

$$Z_{Vout(s)} = \frac{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) \bullet R_{LOAD}}{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) + R_{LOAD}}$$

The power circuit gain equals the current loop transconductance times the output impedance, or

$$G_{Vs} = T_{C(s)} \bullet Z_{Vout(s)}$$

Step 9: Determine the gain required by the compensated voltage amplifier. Insure that gain at the switching frequency does not increase the PWM slope above the required amount due to ESR.

The resistors R14 and R16 around the voltage amplifier were determined by the requirements for non-integrating gain and are

$R14 = 15.0k\Omega$

$R16 = 100k\Omega$

The inductor current di/dt rate is known to be a maximum of 0.313A/µs. This inductor current ramp times the ESR of the output capacitor is multiplied by the gain of the voltage and current amplifiers and is seen at the PWM Comparator. The total contribution of ESR ripple contributed to the ramp at the PWM comparator is the limiting factor for the gain of the voltage amplifier, G_{VA}. Step 4 reduced G_{CAmax} by 25% to account for this factor. The gain of the Current Amplifier at the switching frequency, from Figure 16, is 3.3.

Therefore, from Step 4, and with an equivalent ESR of the output capacitors being 11.0mΩ

$$0.313A/\mu s \bullet ESR \bullet (1+G_{CA(Fs)}) \bullet G_{VAmax(Fs)} = 0.25 \bullet 0364V/\mu s$$

and therefore

$$G_{VAmax(Fs)} \quad \frac{0.25 \bullet 0364V/\mu s}{0.313A/\mu s \bullet 0.011 \bullet (1 + 3.3)}$$

$= 6.15$

Since R16 and R14 set an inverting gain of 100kΩ/15kΩ = 6.67, then the voltage amplifier gain must be rolled off (add a pole) prior to the switching frequency to reduce the gain to less than $G_{VAmax(Fs)}$.

Step 10: Compensate the Voltage Amplifier to achieve desired loop gain and phase and to reduce the voltage amplifier gain at the switching frequency to below $G_{VAmax(Fs)}$.

The voltage loop gain is obtained by multiplying the power circuit gain, G_{VS} by the Voltage Amplifier gain, G_{VAS}.

$$LoopV_S = G_{VAS} \bullet G_{VS} = G_{VAS} \bullet T_{C(s)} \bullet \left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) \bullet R_{LOAD}$$

$$\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) + R_{LOAD}$$

The voltage amplifier gain, without compensation, is simply R16/R14 = 6.67. The voltage loop gain is plotted in Figure 18, showing a very low crossover frequency.

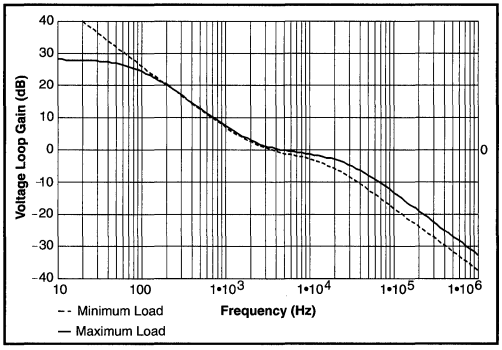

Figure 18. Voltage Loop Gain without Additional Voltage Amplifier Compensation

The voltage amplifier gain is compensated by adding a low frequency pole-zero pair in order to boost low frequency gain. Note however, that DC gain cannot be increased as it is limited by the requirements of non-integrating gain. Secondly, a high frequency pole is added to achieve the desired crossover frequency and to reduce the gain of the voltage amplifier beyond the crossover frequency.

Add C23 and R15 to add a low frequency pole-zero pair in order to boost low frequency (but NOT DC) gain, and therefore boost the crossover frequency. Set the zero at approximately 100Hz and the pole at approximately 400Hz.

The equations for the pole and zero are

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C23 \bullet R15} \quad \text{and}$$

$$F_{ZERO} = \frac{1}{2 \bullet \pi \bullet C23 \bullet (R15 + R14)}$$

Set C23 to 0.1µF. Then

$$R15 = \frac{1}{2 \bullet \pi \bullet C23 \bullet F_{POLE}}$$

$$= \frac{1}{2 \bullet \pi \bullet 0.01\mu F \bullet 400} = 3.98k\Omega$$

Use R15 = 3.92kΩ as a standard value. The results are:

F_{POLE} = 406Hz
F_{ZERO} = 84Hz

Add C24 to add another pole to roll off the gain to obtain the desired crossover frequency and reduce the gain of the voltage amplifier at the switching frequency.

Set C24 to 180pF to obtain a pole frequency at

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet R16 \bullet C24}$$

$$= \frac{1}{2 \bullet \pi \bullet 100k\Omega \bullet 180pF}$$

$$= 8.84kHz$$

The transfer function for the compensated voltage amplifier is

$$GVA(s) = \frac{R16}{R14} \bullet \frac{s \bullet C23 \bullet (R14 + R15) + 1}{(s \bullet R16 \bullet C24 + 1) \bullet (s \bullet R15 \bullet C23 + 1)}$$

With this compensation, the voltage amplifier gain and the loop response for the Voltage Loop are plotted in Figure 19.

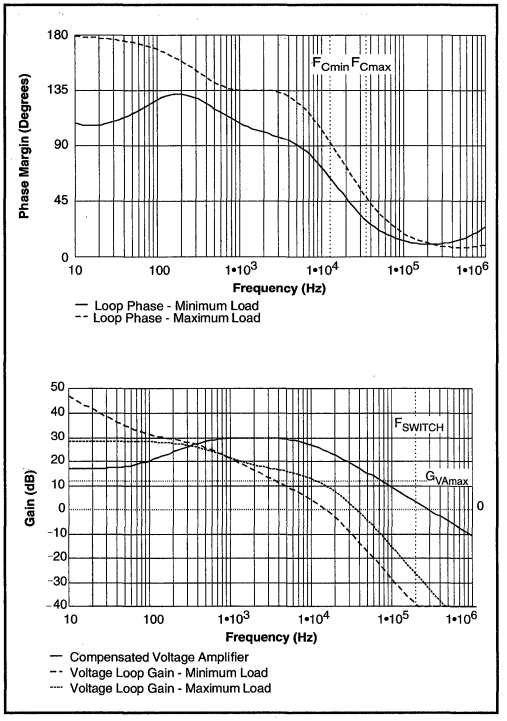

Figure 19. Final Voltage Loop Gain and Phase Plots

MEASURED RESULTS FROM THE VRM DEMONSTRATION KIT

Figure 20 provides the measured open loop response bode plots for the VRM power supply under a nominal 3.1V output at I_{Omax} = 11.2 Amperes.

Figure 21 shows the DC regulation measured at the load in a test configuration, with the nominal output voltage set to 3.100V. The measured test configuration DC impedance from the output of the connector to the resistive load is 1.50mΩ, which accounts for 17mV (0.54%) drop at full load. The load regulation curve matches the predicted non-integrating regulation curve.

Figure 22 shows the measured efficiency and power dissipation of the VRM in a test configuration, with the nominal output voltage set to 3.100V. The input voltage is fixed at 5.00V. The test board

COMPONENTS Z1, R22 AND C26 CAN BE USED FOR VARIATIONS IN THE COMPENSATION SCHEME. THE VRM DEMONSTRATION KIT IS SHIPPED WITH Z1=10Ω AND WITHOUT R22 AND C26.

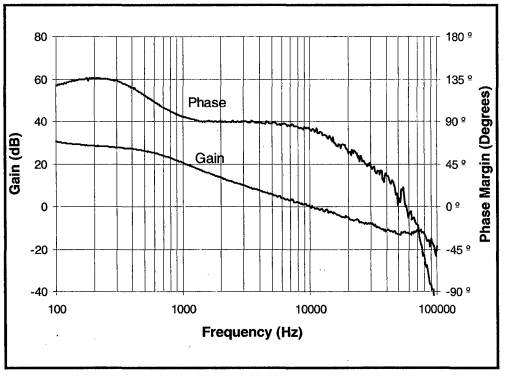

Figure 20. Open Loop Response with V_{OUT} = 3.1V, I_{OUT} = 11.2A

is subjected to 100LFM airflow at approximately 25°C ambient temperature. The full load efficiency is 83.6%.

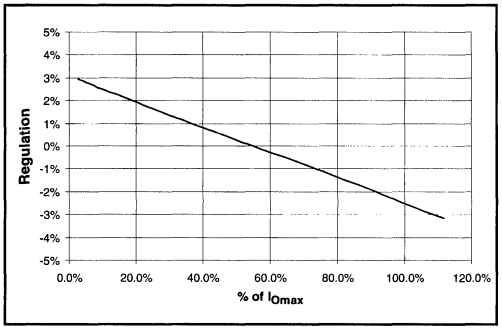

Figure 21. DC Regulation at V_{OUT} = 3.1V for VRM - Measured At Load

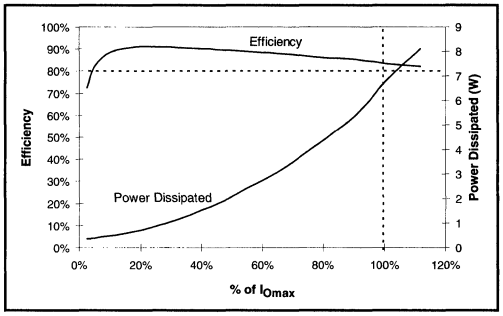

Figure 22. Efficiency and Power Dissipation vs Load for VRM Module with 3.100V nominal Output

The measured efficiency includes the power dissipated by the 12V bias power supply. The +12V current, I_{CC}, is measured to be 25.0mA during normal operation, and is fixed with varying load. With the OUTEN signal disabling the power supply, I_{CC} is measured at 18.5mA, supplying current only for the UC3886 and UC3910, but no gate drive. The average gate drive current is measured at 6.50mA.

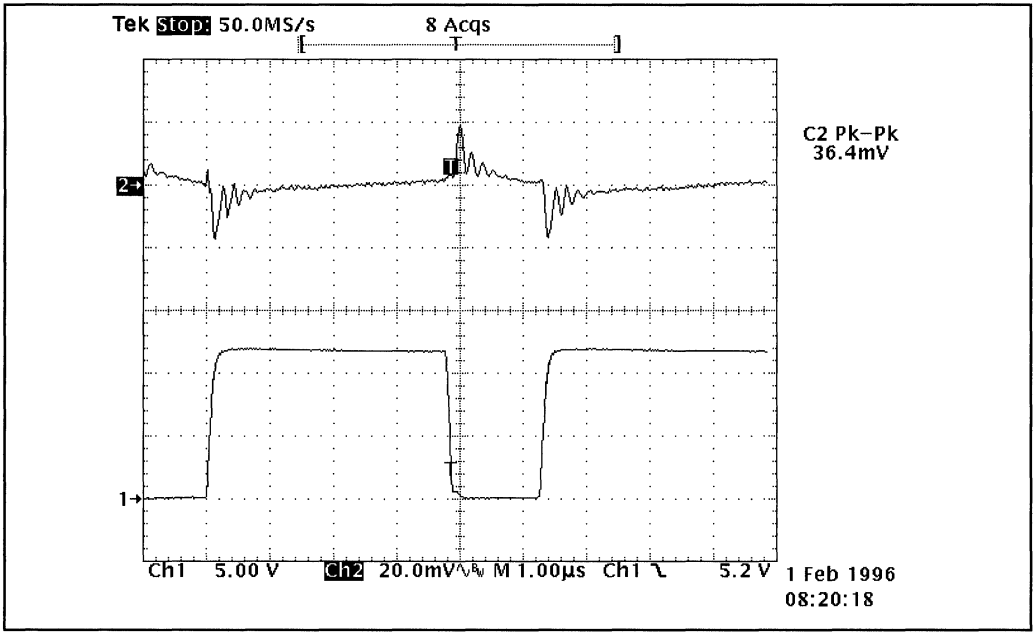

Figure 23. Ripple Voltage and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A.

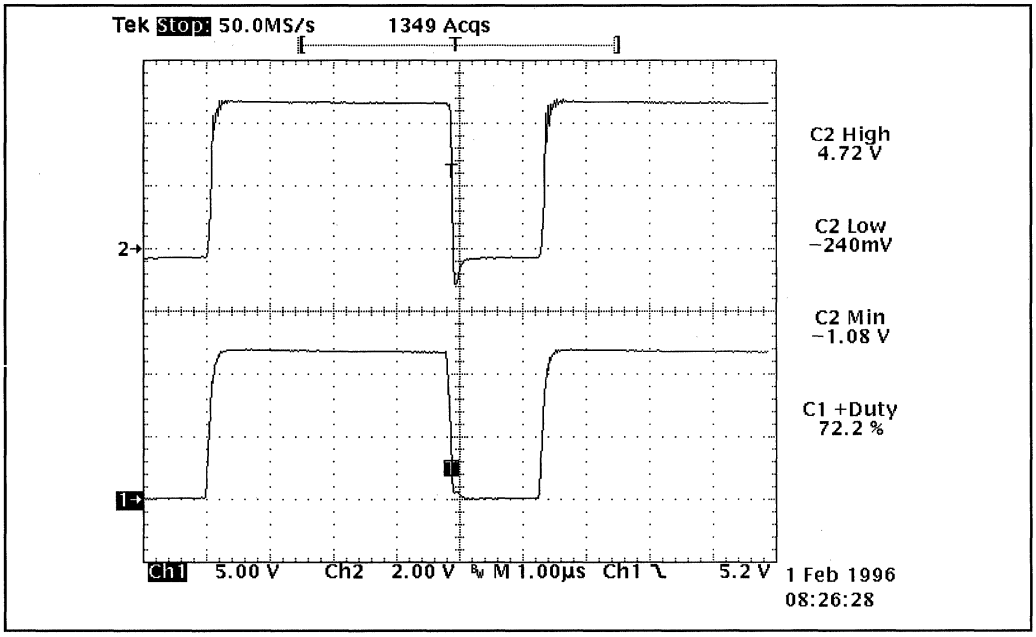

Figure 24. Source Voltage (Top) and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A

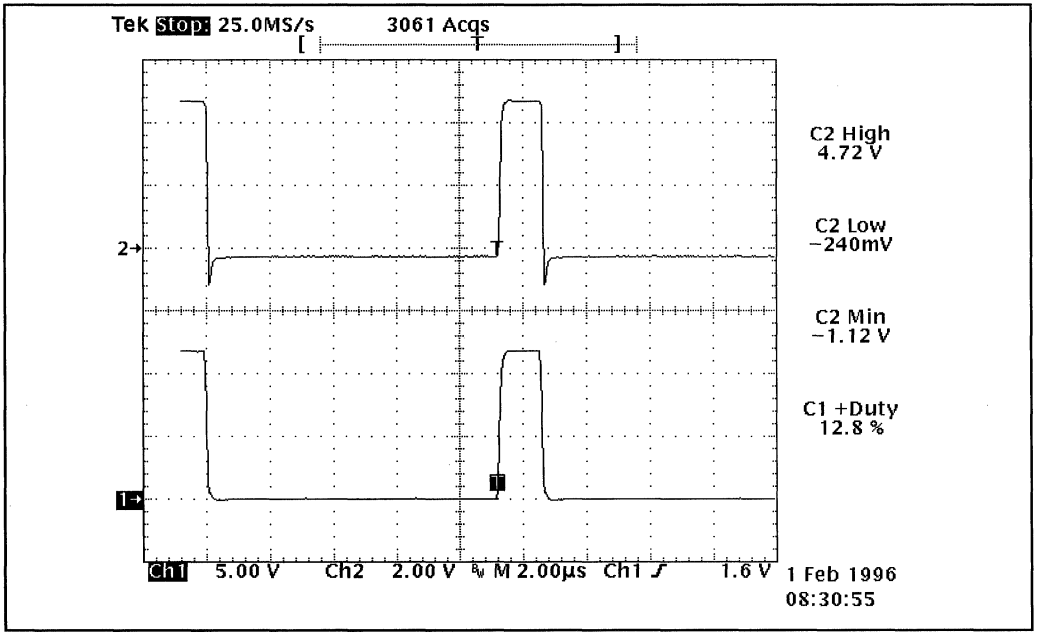

Figure 25. Short Circuit Source Voltage (Top) and Gate Voltage. V_{OUT} = 0.06V. The UC3886 skips cycles to maintain an accurate current limit.

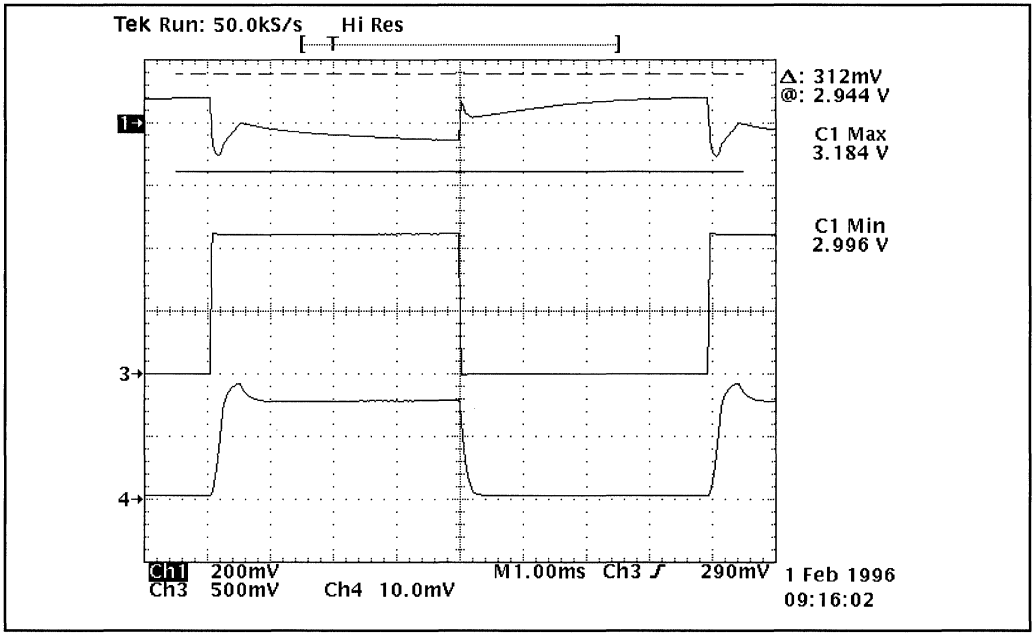

Figure 26. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V, between ±5% cursors. Load current (Middle) @ 2A/div varies at 30A/µs. Input current (Bottom) @ 5A/div. overshoots to charge input and output caps after a load step.

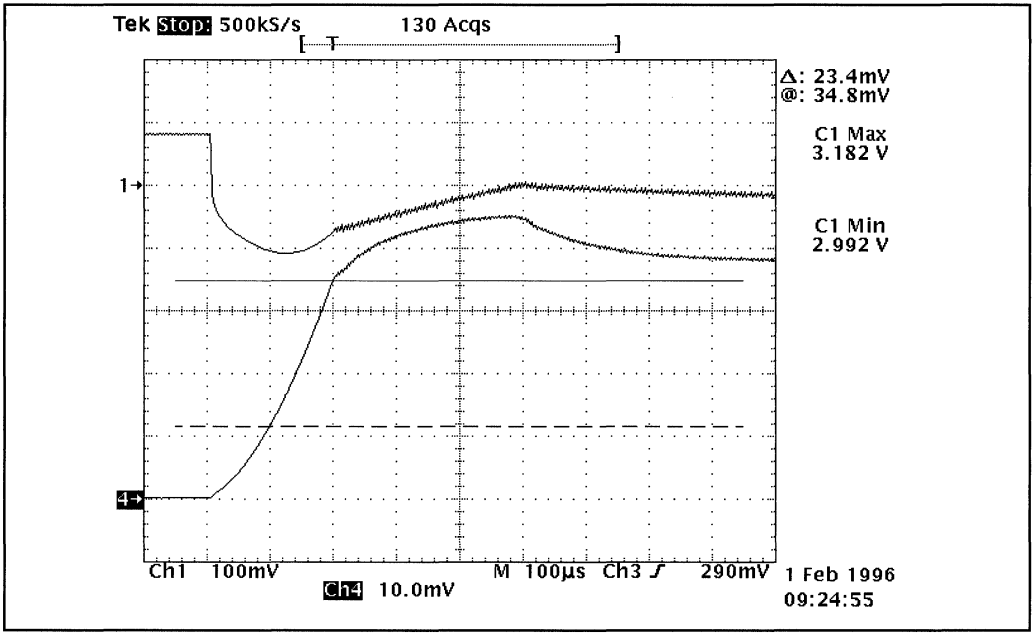

Figure 27. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Input current (Bottom, 2A/div) rises at 0.047A/µs during the load step.

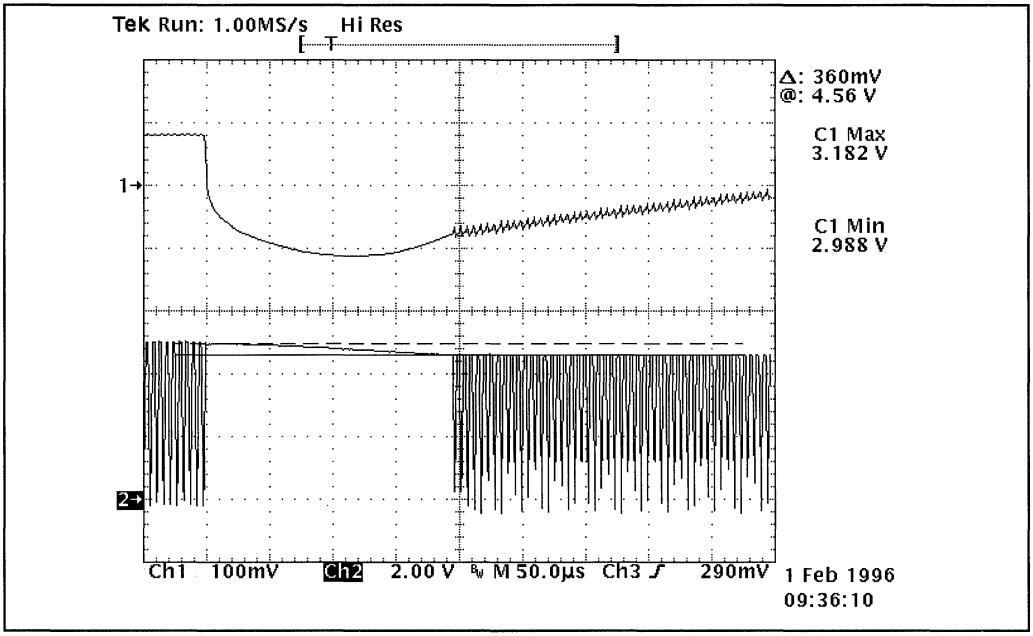

Figure 28. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Q1 Source (Bottom) shows 100% duty cycle as inductor current ramps to full load current. Slope in Source is due to Q1 R_{DSon}.

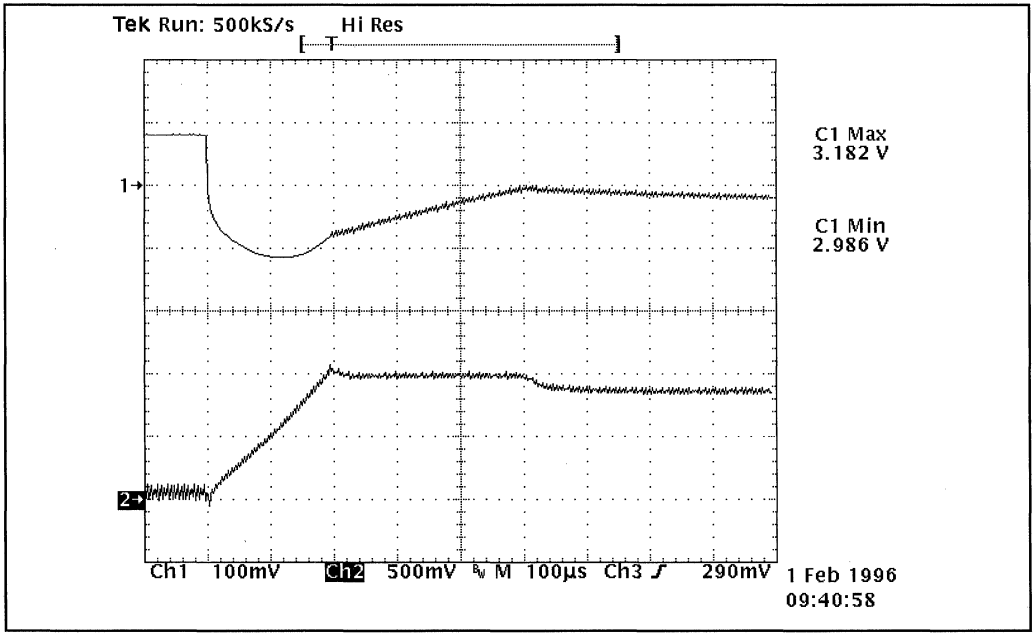

Figure 29. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. ISO, UC3886 Pin 16 (Bottom) swings from 3.10V (Marker 2) to 4.10V at a measured 12.6A short circuit current. The output inductor is calculated to be 27µH during this swing due to high AC Flux.

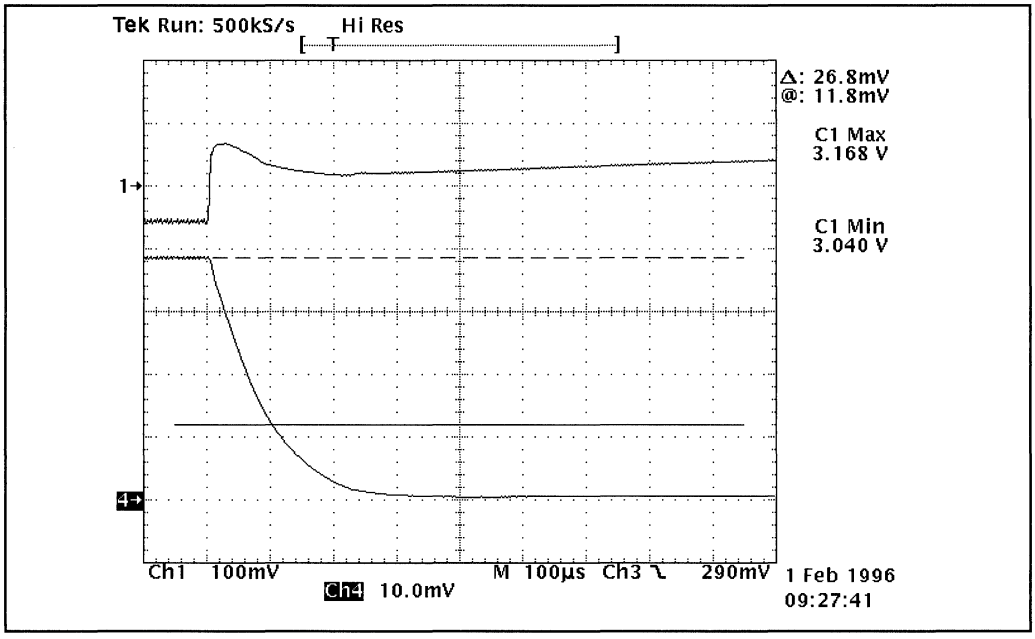

Figure 30. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. Input current (Bottom, 2A/div) falls at 0.054A/µs during the load step.

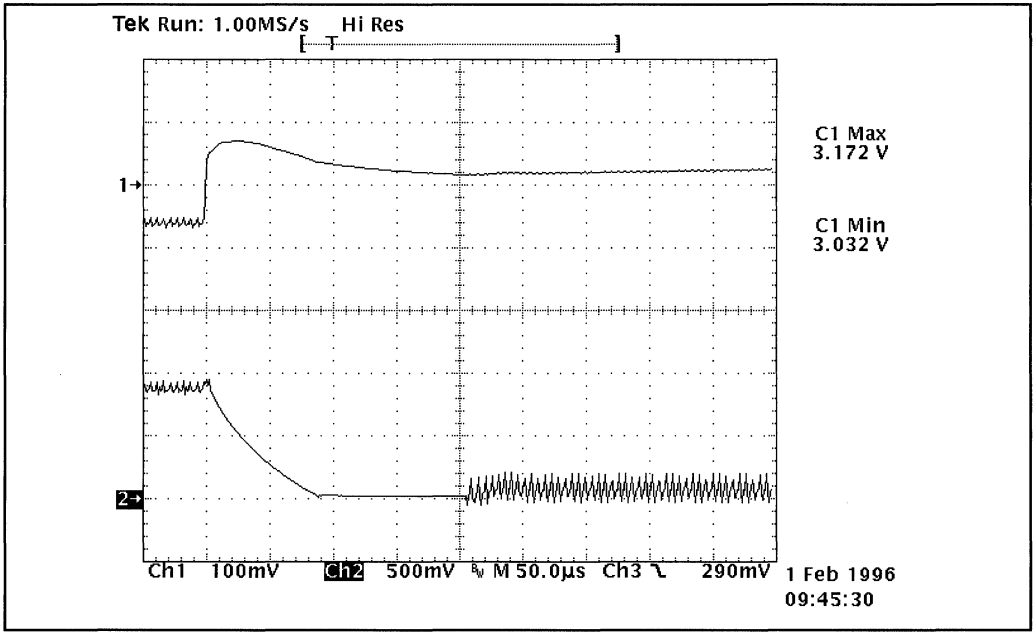

Figure 31. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. ISO, UC3886 Pin 16 (Bottom) swings from 4.00V (Marker 2) to 3.10V. The output inductor is calculated to be 28uH during this swing due to high AC Flux.

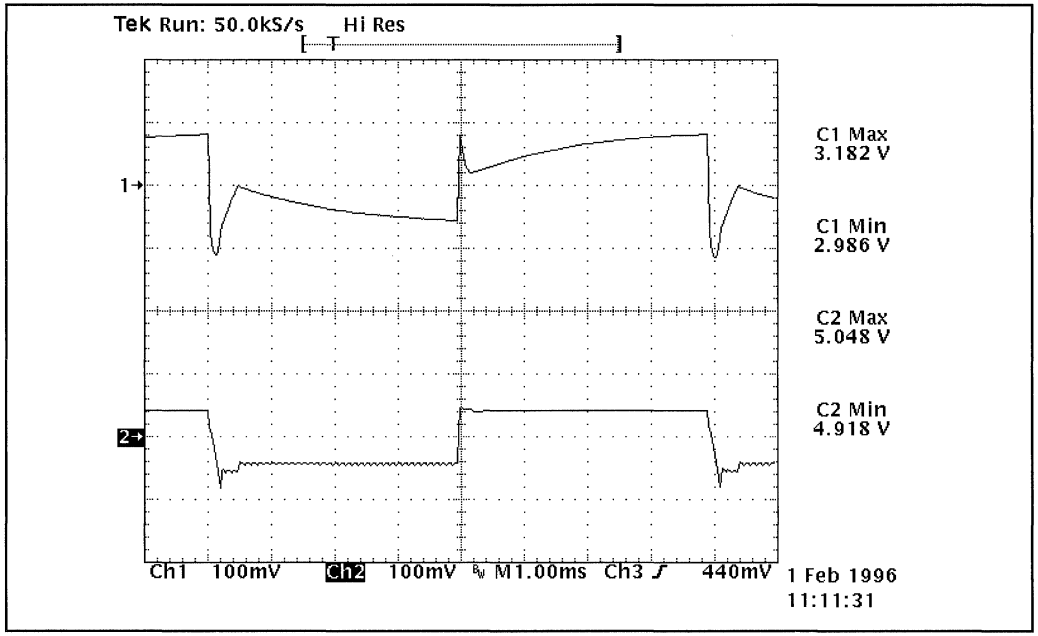

Figure 32. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V. Input voltage (Bottom) shows only 130mV deviation during load steps without input inductor, due to low impedance VRM input capacitors.

CONCLUSION

A highly accurate VRM power supply has been demonstrated which uses Unitrode's UC3886 and UC3910 ICs. This VRM meets the Intel VRM power supply specifications, has excellent regulation, transient response, and efficiency. It has been demonstrated that a single output inductor can allow continuous mode operation, meet the stringent transient response of the Pentium®Pro, and limit the input current rate as well. The use of non-integrating voltage loop regulation has been proven to use fewer output capacitors because of the larger transient voltage swing allowed by this technique.

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2. Unitrode Application Note U-140, Average Current Mode Control of Switching Power Supplies, Lloyd Dixon
3. Micrometals, Anaheim, CA, Iron Powder Cores Catalog 4, Issue G, Power Conversion & Line Filter Applications, Percent Initial Permeability vs Peak AC Flux Density Curve.
4. Unitrode Application Note U-156, The UC3886 PWM Controller Uses Average Current Mode Control to Meet the Transient Regulation Performance of High End Processors, Larry Spaziani
5. Motorola Thyristor Device Data Book, DL137/D Rev 6, Motorola Inc. Phoenix, Arizona
6. Unitrode Application Note U-158, The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies, Larry Spaziani
7. Unitrode Power Supply Design Seminar SEM-800, Switching Power Supply Control Loop Design, Lloyd Dixon. Reprinted in SEM-900 and SEM-1000.

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THE UC3910 COMBINES PROGRAMMABILITY, ACCURACY AND INTEGRATED FUNCTIONS TO CONTROL AND MONITOR HIGH END PROCESSOR POWER SUPPLIES

by Larry Spaziani

ABSTRACT

As high performance processors continue to develop, their respective power supply requirements become more stringent, often requiring low, custom voltages and increasingly tighter regulation. Intel's Pentium®Pro power system specification, for instance, demonstrates the need for tight regulation, programmable power supply voltage and programmable voltage monitoring for status reporting to the processor. To help meet these requirements, the UC3910 4-BIT DAC and Voltage Monitor IC is introduced. This application note discusses the architecture and features of the UC3910 and details how this IC is used for an optimal Pentium®Pro power supply solution.

UC3910 4-BIT DAC AND VOLTAGE MONITOR

- High Precision Reference for tight regulation
  0.5% Typical combined DAC/Reference precision
- 4-BIT DAC directly compatible with Intel's Pentium®Pro VID function
  Sixteen steps from 2.0V to 3.5V in 100mV increments
- Undervoltage and Overvoltage Fault Windows
  User programmed with 2 external resistors
  Proportional to DAC programmed voltage over the entire operating range
- Overvoltage Protection Comparator
  Proportional to DAC programmed voltage over the entire operating range
  Directly drives an external SCR
- Undervoltage Lockout

INTRODUCTION

The UC3910 4-BIT DAC and Voltage Monitor IC contains a 4-BIT Digital to Analog converter which is used to program a precise DC voltage for use in commanding a power supply voltage. The actual power supply voltage is compared against user programmable thresholds, with the comparators providing logic status to the system or protecting the power supply with a crowbar SCR. This IC has been developed to interface with Intel's Pentium® Pro processor, but has widespread uses where precise control and monitoring of a power supply voltage is required.

The high DC accuracy of the UC3910 reference and DAC, typically ±0.5%, makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Tight regulation of power supplies can be met without adjusting the power supply voltage at manufacturing. The programmable output can also be used to digitally adjust a power supply voltage in test or manufacturing, allowing a single power supply design to accommodate multiple uses.

The UC3910 offers substantial advantages over discrete solutions when meeting Intel's Pentium®Pro power supply requirements. Its 4-BIT Digital-to-Analog Converter output voltage varies from 2.0V to 3.5V in 100mV increments for direct

compatibility with Intel's VID codes. The many integrated features and the programmability of the UC3910 allow power supply designers to replace discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. Tight regulation can be met directly because of the excellent DC accuracy of the UC3910 combined DAC and reference voltages.

THE UC3910 4-BIT DAC AND VOLTAGE MONITOR

A block diagram of the UC3910 is shown in Figure 1.

The UC3910 is ideally suited to create a programmable, precision system reference for low voltage power supplies. Figure 2 shows the UC3910 configured with the UC3886 Average Current Mode PWM Controller IC to provide a solution for the

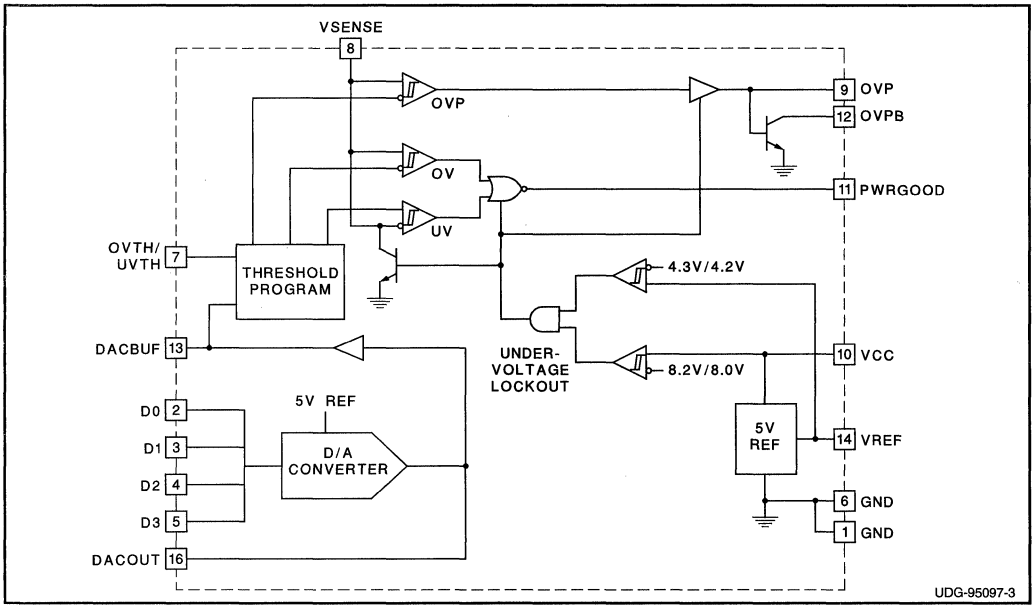

Figure 1. UC3910 4-BIT DAC and Voltage Monitor

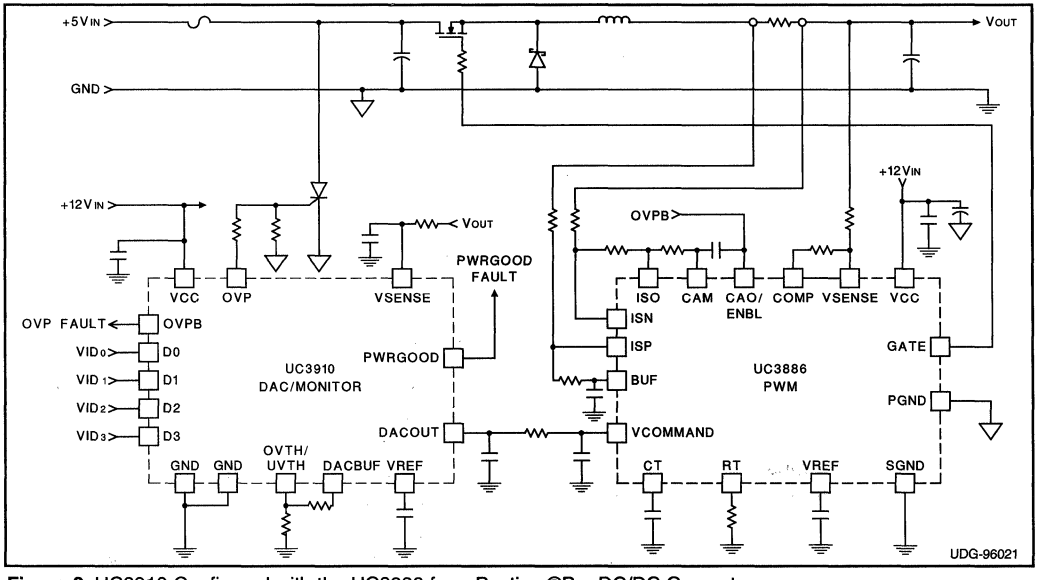

Figure 2. UC3910 Configured with the UC3886 for a Pentium®Pro DC/DC Converter

complex power system requirements of Intel's Pentium®Pro processor. The UC3910 is directly compatible with Intel's Voltage Identification (VID) code as shown in Figure 2.

UC3910 - SUPPLYING POWER

The UC3910 is constructed using a bipolar process allowing the input supply voltage, V_{CC}, to be as high as 20V. Minimum operating voltage is 8.2 volts. The supply voltage provides internal biasing of all circuit blocks including the high precision reference voltage, V_{REF}, which provides a precision reference voltage for the Digital to Analog Converter (DAC). VCC should be decoupled to ground with a 0.1µF to 1.0µF ceramic capacitor located in close proximity to the IC.

Grounding the UC3910

The UC3910 utilizes two ground pins to optimize the layout of the high precision DAC and Reference circuitry. Both ground pins must be connected to ground close to the IC and to each other.

UNDERVOLTAGE LOCKOUT

The UC3910 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 3 shows typical V_{CC} thresholds of the UC3910 UVLO circuitry.

The supply current, I_{CC}, is typically less than 3mA during UVLO and is typically less than 10mA when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}. The 0.2V hysteresis prevents V_{CC} oscillations during the power up and power down sequences.

During UVLO, V_{REF} and the DAC output, DACOUT, are disabled, the threshold circuitry is disabled and the sense pin, VSENSE, is actively held low. The PWRGOOD signal is actively held LOW, the OVPB signal is forced HIGH (open) and the OVP signal's drive is disabled to insure no false control signals are generated during power up and power down sequencing.

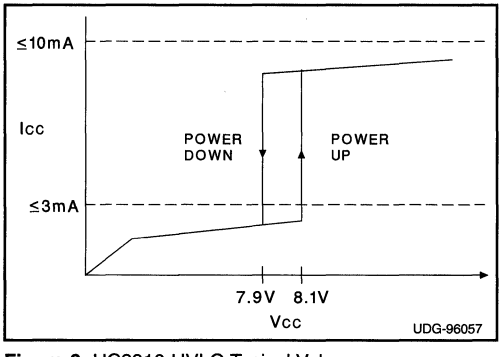

Figure 3. UC3910 UVLO Typical Values

VREF

The UC3910 contains a 5.0V precision trimmed bandgap reference, based on similar technology as that used on many other Unitrode ICs, but is enhanced by the use of precision thin film resistors. Thin film resistors exhibit excellent performance with voltage and temperature variations, and don't shift in value due to packaging stresses. These enhancements result in a reference voltage tolerance of ±0.5% from 0°C to 70°C. V_{REF} provides bias directly to the DAC circuitry, and plays a major role in the precision of the DAC output.

The reference can be used to bias external circuitry, can source up to 10mA and has internal short circuit protection. VREF should be decoupled with a 0.1µF to 1.0µF monolithic ceramic capacitor located close to the IC. Load circuits with high noise content should be avoided, or decoupled very well, as noise on V_{REF} will directly couple to the DACOUT pin.

VREF COMPARATOR

The reference voltage is internally monitored as shown in Figure 4. The 0.1V hysteresis prevents V_{REF} oscillations during the V_{REF} power up and power down sequences. While the reference voltage is below the V_{REF} threshold, VSENSE, PWRGOOD, OVP and OVPB are disabled in the same manner as they are during undervoltage lockout.

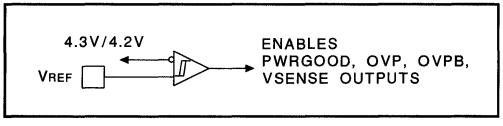

Figure 4. UC3910 V_{REF} Comparator

A typical power up sequence is shown in Figure 5. The voltage monitoring outputs are not enabled until time t_1 at which time V_{CC} and V_{REF} are above their respective thresholds.

PROGRAMMABLE DIGITAL-TO-ANALOG CONVERTER

The UC3910 contains a 4-Bit Digital to Analog Converter with an architecture shown in Figure 6. The DAC output (DACOUT) is a high impedance precision output programmed by the 4 programming pins, D0 (LSB) through D3 (MSB). Each programming bit pin controls a current source which is precisely trimmed to achieve the proper output voltage.

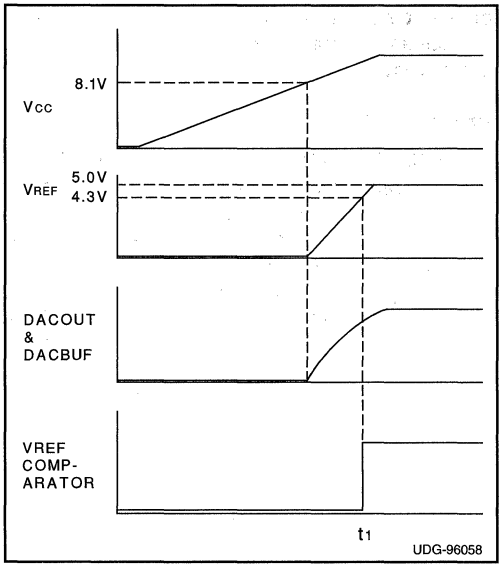

Figure 5. Power Up Sequence

DACOUT

The accuracy of the DACOUT pin, including the tolerance of the reference voltage, V_{REF} (combined accuracy), is typically ±0.5% and is ±0.9% from 0°C to 70°C worst case. DACOUT cannot be loaded externally since it is a high impedance (3kΩ) output. It should be decoupled locally with a 0.01µF to 0.1µF monolithic ceramic capacitor. A larger capacitor can be used to control the rise rate of the DACOUT voltage, where the internal 3kΩ resistor and the external decoupling capacitor form an RC time constant.

DACBUF

The DACBUF pin is a low impedance, buffered output of the DACOUT pin with a total gain/offset error of ±25mV. This pin is used by the UC3910 to set the overvoltage, undervoltage and overvoltage protection comparator threshold voltages. DACOUT cannot be used for this function since the threshold circuitry requires current and DACOUT cannot be loaded. The buffer is internally compensated for unity gain and cannot be decoupled externally. Good decoupling of the DACOUT and VCC pins will insure that the DACBUF signal is not corrupted by noise. DACBUF is internally clamped to 1 diode drop above ground during undervoltage lockout.

PROGRAMMING THE DAC

The DACOUT voltage is directly compatible with Intel's Pentium®Pro coding requirements, as shown in Table 1. The D0-D3 pins are directly equivalent to Intel's VID0 - VID3 signals. Intel requires programmable steps from 2.4V to 3.4V in 100mV increments, whereas the values of 2.0V to 2.3V and 3.5V are optional. The UC3910 DAC is programmable in 100mV increments, from 2.0V to 3.5V, where each decreasing bit represents a 100mV step, as shown Table 1.

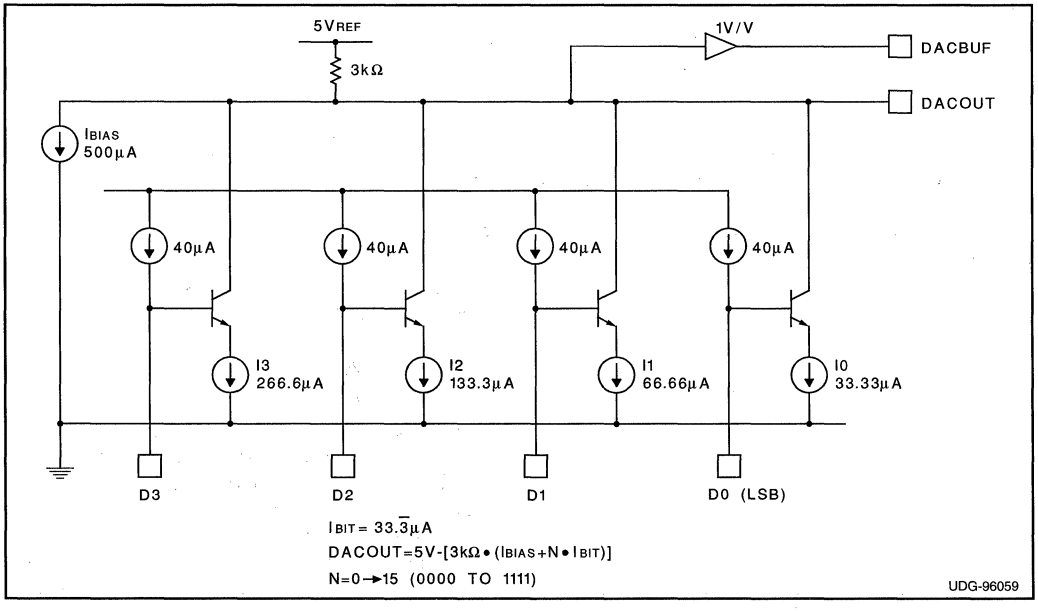

Figure 6. UC3910 Digital to Analog Converter (DAC) Architecture

Decimal Code	D3	D2	D1	D0	DACOUT Voltage	Pentium®Pro Specification	
15	1	1	1	1	2.0	No Processor	
14	1	1	1	0	2.1	2.1	
13	1	1	0	1	2.2	2.2	
12	1	1	0	0	2.3	2.3	
11	1	0	1	1	2.4	2.4	Intel's
10	1	0	1	0	2.5	2.5	I
9	1	0	0	1	2.6	2.6	I
8	1	0	0	0	2.7	2.7	I
7	0	1	1	1	2.8	2.8	↓
6	0	1	1	0	2.9	2.9	Operating
5	0	1	0	1	3.0	3.0	I
4	0	1	0	0	3.1	3.1	I
3	0	0	1	1	3.2	3.2	I
2	0	0	1	0	3.3	3.3	↓
1	0	0	0	1	3.4	3.4	Region
0	0	0	0	0	3.5	3.5	

Table 1. Programming the DACOUT Voltage

Figure 6 shows that each decimal code (0 through 15) represents an addition of 33.33µA of current through the 3kΩ resistor, which results in 100mV steps for each bit. A bias current of 500µA is used to set DACOUT to 3.5V when all four bits are 0s.

Programming pins D0-D3 are designed to accept OPEN = Logic 1 and SHORT = Logic 0 levels, as required by Intel, and will also accept open collector logic inputs. Each bit is pulled up internally to approximately 4.8V by a 40µA current source, as shown in Figure 6.

Some systems may want to control the D0-D3 pins from standard logic gates rather than open collector logic. The UC3910 will accept logic level inputs to the D0-D3 programming pins only if the logic HIGH level is ≥ 3.0 volts. The logic family should be well understood to insure that the driver can sink 40µA even when it is a logic HIGH.

Intel's specification for the Pentium®Pro processor includes all "1s" as an indicator that no processor is present. The UC3910 generates 2.0V on the DACOUT pin when all "1s" are present, thus insuring a safe low voltage level is present in a system should the programming pins be opened for any reason.

Dynamically Programming the DAC

The UC3910 is designed to accept the 4 bits as hardwired inputs prior to or at the same time power is applied to the UC3910. Dynamically changing the 4 bits is not recommended, as the characteristics (response time, overshoot, etc.) of the UC3910 DAC output under these conditions is highly dependent on external components. The time constant of the internal 3kΩ resistor and the DACOUT decoupling capacitor directly affect the rate at which DACOUT can dynamically change.

Changing the DAC Voltage Increments/Range

The UC3910 is designed to meet the Intel Pentium®Pro specification which requires programmable voltages from 2.4V to 3.4V in 100mV steps. Some systems may require exact power supply voltage outputs in ranges or increments other than those above in order to compensate for losses or to fine tune performance.

Upon inspection of Figure 6, a designer may opt to place an external resistor from DACOUT to VREF or to GND to adjust the DACOUT voltage up or down, respectively, as shown in Figure 7. This method, however, is NOT recommended. The UC3910 DAC is precisely trimmed to achieve it's accuracy, but the internal 3kΩ resistor IS NOT a precision resistor, and may be only accurate to ±20%. Designing an offset based on this internal resistor may therefore result in large errors. Should this method be used, the programmed voltage increment is no longer 100mV, but is proportional to the value of the external resistor used.

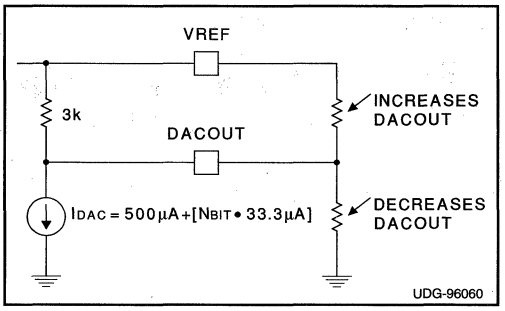

Figure 7. Using External Resistors to Adjust DACOUT is NOT recommended

A power supply's output voltage, controlled by the UC3910, may be adjusted when used in conjunction with the UC3886 PWM controller, as shown in Figures 8 (a) and (b). Increasing the voltage as shown in Figure 8 (a) can be accomplished with good accuracy by using precision resistors. Decreasing the voltage, as shown in Figure 8 (b) however, results in less accuracy, as the DACBUF buffered output includes gain/offset error of ±25mV (DACBUF = DACOUT ±25mV).

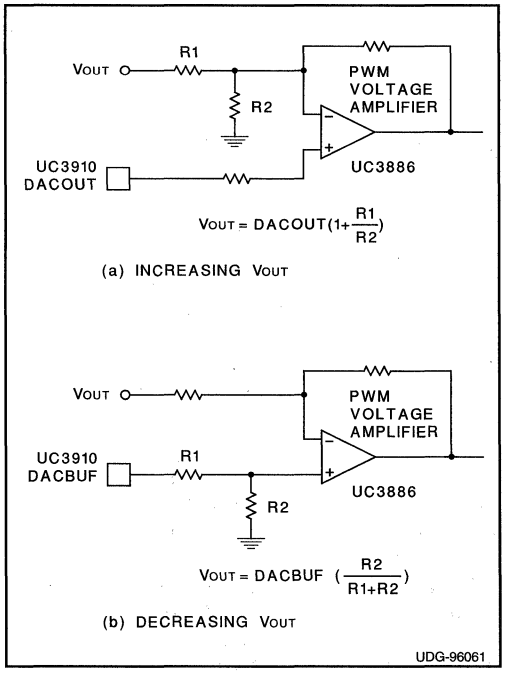

Figure 8. Recommended Methods for Adjusting a Power Supply's Output Voltage

VOLTAGE MONITORING SECTION

The UC3910's voltage monitoring section contains programmable window comparators which enable a power supply's output voltage to be closely monitored. The power supply's output voltage, as seen at the UC3910 VSENSE pin, is compared to three programmable thresholds; undervoltage, overvoltage, and overvoltage protection. The undervoltage and overvoltage comparators control the PWRGOOD signal to indicate that the output voltage is within a specified operating range. The overvoltage protection comparator controls the OVPB and OVP signals, which can be used to disable the power supply or to fire an external crowbar SCR.

The undervoltage, overvoltage, and overvoltage protection thresholds are programmed as a percentage above and below the programmed output (DACOUT), so that as the UC3910 DAC output voltage varies (various Pentium®Pro voltages for instance), so do the thresholds as a percentage of the DACOUT voltage.

Figure 9 shows a simplified schematic of the internal voltage monitor section. The voltage monitor section is programmable by the external resistors RS1 and RS2 at the threshold programming pin, OVTH/UVTH. RS1 and RS2 set the internal voltage thresholds which become inputs to the overvoltage, undervoltage and overvoltage protection comparators. The buffered DAC output, DACBUF, is used as the reference for the voltage monitoring thresholds.

VSENSE

The sense pin, VSENSE, is one input to the overvoltage, undervoltage and overvoltage protection comparators (OV, UV and OVP) which is compared to the set thresholds, as shown in Figure 9. VSENSE is typically connected to the output of the power supply which is controlled by the UC3910's precision output, DACOUT.

The hysteresis levels on the voltage monitor comparators can be as low as 20mV. VSENSE should be filtered externally with an RC filter, as shown in Figure 9, to insure that noise and ripple voltage does not cause false signals at the PWRGOOD and OVP pins. A filter frequency of 1/10th the power supply switching frequency is recommended, to reduce switching ripple by 20dB. The filter resistor and capacitor product is therefore

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

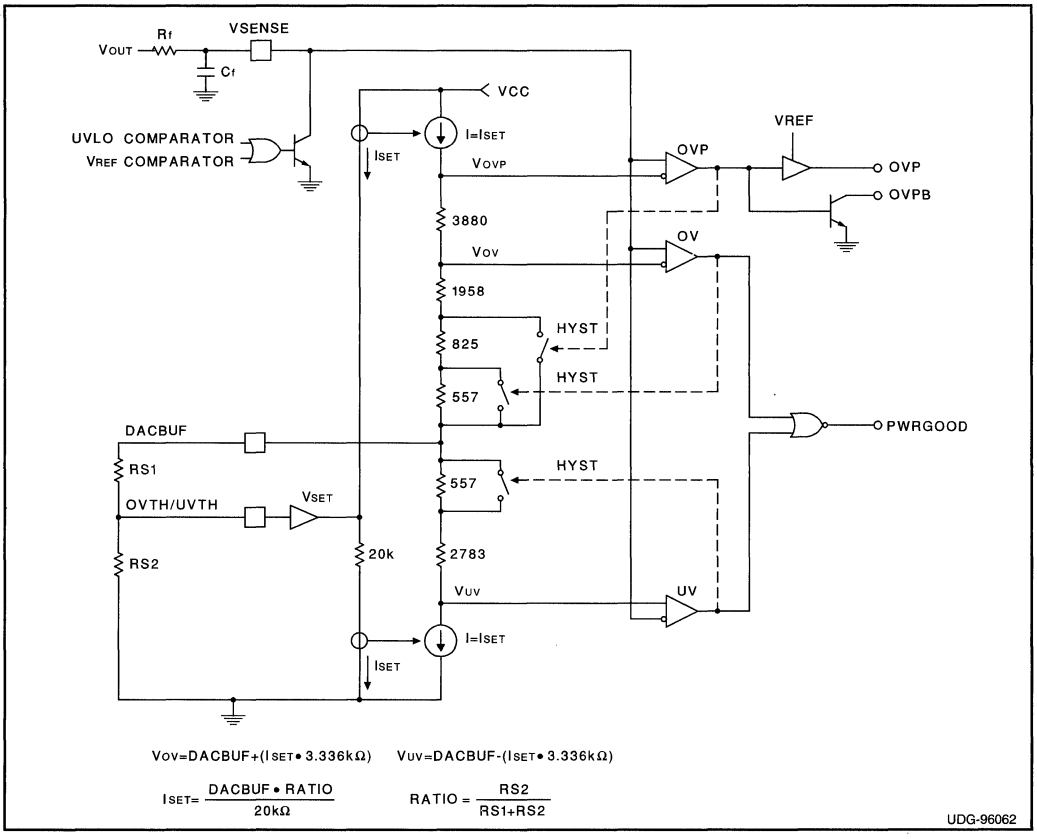

Figure 9. Voltage Monitor Section

VSENSE During UVLO - Protecting Against False OVP Signals

The UC3910 is designed to actively pull down VSENSE until V_{CC} and V_{REF} are above their respective thresholds during startup of the UC3910. This feature insures that during V_{CC} "brown-out" conditions, or when power supplies are powered up onto a live output bus, that the value of VSENSE will be below the DAC voltage, and will not trigger a false overvoltage protection signal. A V_{CC} "brown-out" situation is illustrated in Figure 10.

VSENSE can actively sink up to 500µA. The external filter resistor must therefore limit the current into VSENSE, such that

$$R_F \geq \frac{V_{OUT}}{500\mu A}$$

To insure that VSENSE does not falsely trigger an OVP condition, DACOUT must rise to its programmed level faster than VSENSE can rise. This restriction governs the two time constants on the VSENSE and the DACOUT pins. The DACOUT time constant is determined by the internal 3kΩ resistor and the DACOUT decoupling capacitor,

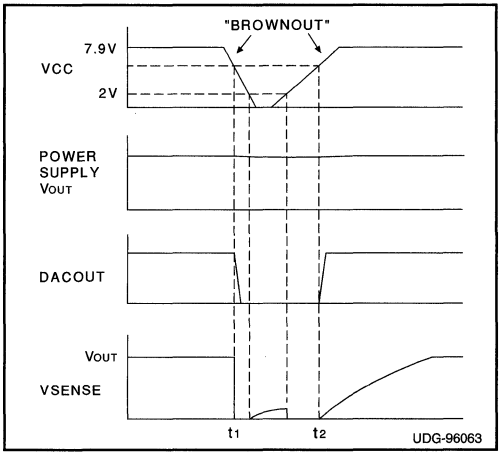

Figure 10. VSENSE is Pulled Low During UVLO Insuring that no False OVP Conditions Occur

whereas the VSENSE time constant is controlled by the external filter components R_F and C_F. From Figure 11, it can be seen that

$$R_F \bullet C_F > 3k\Omega \bullet C_{DACOUT}$$

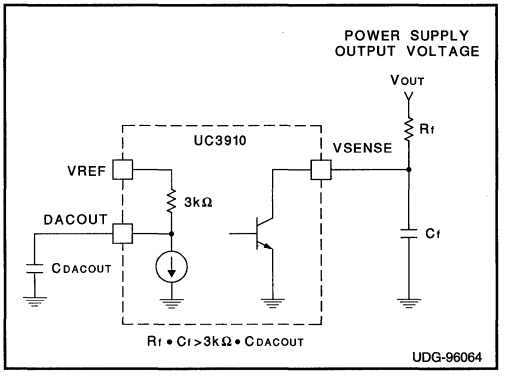

Figure 11. DACOUT Must Rise Faster than VSENSE

OVTH/UVTH Pin: Programming the OV, UV and OVP Thresholds

The UC3910 percentage thresholds are set above or below the nominal DAC output voltage, and are programmed by the ratio of the external resistors RS1 and RS2, R_{DIV}, where R_{DIV} is defined as

$$R_{DIV} = \frac{RS2}{RS1 + RS2}$$

The UC3910 allows a ratio R_{DIV} at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Figure 12.

The undervoltage, overvoltage and overvoltage protection (UV, OV and OVP) percentage thresholds are given by

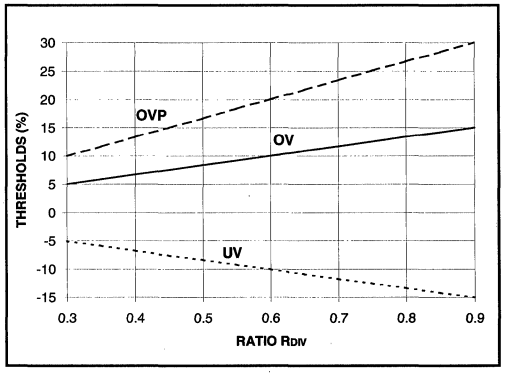

Figure 12. OV, UV and OVP Percentage Thresholds as a Function of the Divider Ratio R_{DIV}

$$\%V_{OV} = R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega} \bullet 100 = R_{DIV} \bullet 16.7$$

$$\%V_{UV} = -\%V_{OV} = -(R_{DIV} \bullet 16.7)$$

$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

Refer to Figure 9 for the following derivation of how these UC3910 thresholds are set.

The voltage at the OVTH/UVTH pin, V_{SET}, is obtained by dividing DACBUF using RS1 and RS2, such that

$$V_{SET} = DACBUF \bullet \left[\frac{RS2}{RS1+RS}\right]$$

$$= DACBUF \bullet R_{DIV}$$

V_{SET} is internally buffered and then fed to a 20kΩ resistor to set the current I_{SET}, giving

$$I_{SET} = \frac{V_{SET}}{20k\Omega}$$

I_{SET} is then mirrored to the overvoltage and undervoltage resistive chains shown in Figure 9. The total resistance in the overvoltage and undervoltage chains is 3.34kΩ, whereas the total resistance in the overvoltage protection chain is 6.663kΩ. DACBUF is internally tied to the "center" point of the resistive chains as a reference voltage for the thresholds. The UV, OV, and OVP threshold voltages, at their respective comparators, are therefore given by:

$$V_{OV} = DACBUF + I_{SET} \bullet 3.34k\Omega$$

$$V_{UV} = DACBUF - I_{SET} \bullet 3.34k\Omega$$

$$V_{OVP} = DACBUF + I_{SET} \bullet 6.663k\Omega$$

These threshold voltages can be expressed in terms of percentages above or below the nominal DACBUF voltage since they are all biased by the programmed DACBUF voltage. The overvoltage percentage is determined by

$$\%V_{OV} = \left(\frac{V_{OV} - DACBUF}{DACBUF}\right) \bullet 100$$

which can be simplified to

$$\%V_{OV} = \left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega}\right) \bullet 100 = R_{DIV} \bullet 16.7$$

Likewise, the undervoltage and overvoltage protection percentage thresholds can be expressed as

$$\%V_{UV} = -(R_{DIV} \bullet 16.7) \text{ and}$$

$$\%V_{OVP} = R_{DIV} \bullet 33.4 = \%V_{OV} \bullet 2.0$$

(The OVP threshold percentage is 2.0 times the OV threshold percentage)

These percentage thresholds are shown graphically in Figure 12.

Hysteresis and Tolerances in the OV, UV and OVP Thresholds:

Each of the UV, OV and OVP threshold circuits in the resistive chain of Figure 9 contains a hysteresis resistor, which is switched in or out by the output of the respective comparator. The result is that the threshold voltages change (in voltage, not percent) by

$$UV_{HYS} = -(I_{SET} \bullet 557\Omega)$$

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

I_{SET} is proportional to both the programmed DAC voltage DACBUF as well as the ratio R_{DIV} which sets the thresholds. For an Intel Pentium®Pro application with voltages ranging from 2.4V to 3.4V and R_{DIV} ranging from 0.3 to 0.9, the hysteresis can range from 20mV to 85mV on OV and UV and from 50mV to 211mV on OVP. The effects of hysteresis are shown graphically in Figure 13.

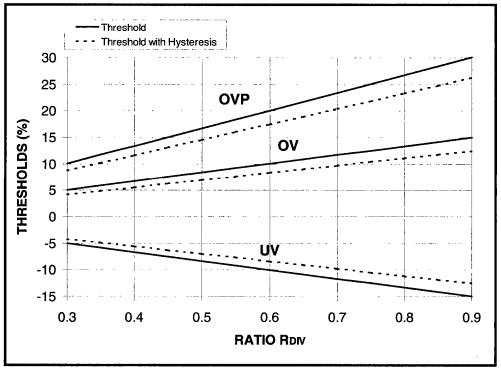

Figure 13. OV/UV and OVP Thresholds Including Hysteresis

There are tolerance factors that a circuit designer should consider when programming the voltage monitor threshold percentages. They are:

- UC3910 DACBUF error of ± 25mV
- UC3910 OV, UV and OVP Comparator off set voltages of ±10mV
- UC3910 Bias current from the OVTH/UVTH pins of ±30% of the value Iset
- UC3910 Threshold detection tolerance of ±10% of the percentage set
- External Resistor tolerances
- Non-ideal External resistor Values (The perfect divider ratio may not be achievable)

The designer can reduce the error due to external resistors by using precision values. Errors due to bias current from the OVTH/UVTH pin can also be minimized by using external values which draw approximately 1.0mA from DACBUF (presents a low impedance to the leakage current source), or

$$\frac{DACBUF}{RS1 + RS2} \approx 1.0mA$$

Unitrode has performed a Worst Case and an Root Sum Square (RSS) error analysis including all the abovementioned factors, for a set Ratio of R_{DIV}=0.45 (7.5% OV/UV thresholds), and using 1% resistors, with the results shown in Figure 14.

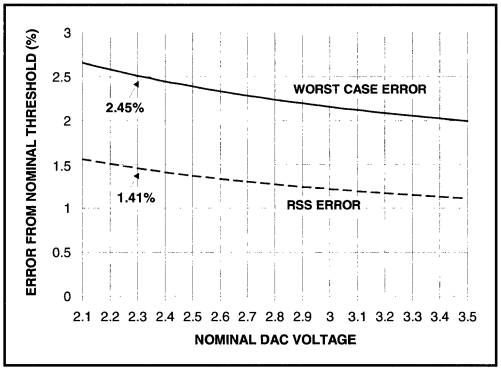

Figure 14. Error Analysis for a Nominal 7.5% OV/UV Threshold Setting - Varies with V_{OUT}

Should higher accuracy be required for the thresholds, the stability of the offset voltages and bias currents of the UC3910 with life and temperature is such that a voltage divider, RS1 and RS2, can be set up at manufacturing to set the thresholds very precisely, with little drift expected over the life of the power supply.

PWRGOOD

The PWRGOOD signal is an open collector logic level that is HIGH when the voltage at the UC3910 VSENSE pin is above the UV threshold and below the OV threshold, as indicated in Figure 9. The PWRGOOD signal must be pulled up externally to a voltage less than V_{CC}(max) and can sink 10mA.

Figure 15 illustrates the PWRGOOD comparator and drive stage. PWRGOOD is held low until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 15.

The PWRGOOD comparator output, during power up and power down sequencing, gets "smart" with V_{CC} at approximately 2.0 volts. Until V_{CC} reaches this level, there is not enough bias current (Figure 15, I1) to keep the PWRGOOD signal held in its low state. In most systems, where the PWRGOOD signal will act as the reset for the processor, this will

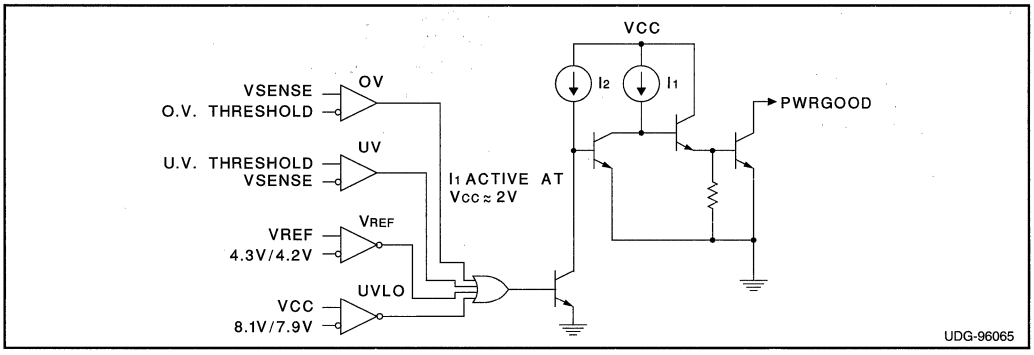

Figure 15. PWRGOOD Comparator and Drive

not matter since the processor itself will have no power during the time V_{CC} is lower than 2.0 volts.

Resistor R2 shown in Figure 16 can be used to pull down the PWRGOOD signal, thus insuring that even with VCC at 0 volts, the PWRGOOD signal will not provide an erroneous signal. R2 should be chosen such that it can sink a small amount of leakage current from the logic receiving circuit and still maintain logic low level. R1 must be chosen to limit the current into PWRGOOD to less than 10mA, and also to provide the proper level HIGH voltage. V_{REF} is disabled during UVLO, thus insuring there will be no pull-up voltage. Low voltage logic families can also be accommodated by using the circuit of Figure 16.

The PWRGOOD signal may be used as a reset signal to processor which is controlled by the UC3910 itself. A reset delay may be added to allow the processor to boot some time after the PWRGOOD signal. A typical reset circuit is shown in Figure 17.

OVP and OVPB Overvoltage Protection Signals

The OVP output signal is designed to directly trigger a silicon controlled rectifier (SCR) thyristor when a severe overvoltage condition occurs. OVPB is an open collector signal designed to go LOW under the same conditions, which can be used to disable a PWM such as the UC3886. The OVP comparator (see Figure 9) is tripped when the output voltage has reached a voltage equal to two times the programmed overvoltage threshold.

Figure 18 illustrates the OVP comparator and drive stage. The OVP and OVPB signals are disabled until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 18, by removing the bias current from the drive stage.

The OVP output drive, during power up and power down sequencing, gets "smart" with V_{CC} at approximately 2.0 volts. A minor amount of drive current can leak through to the OVP output while V_{CC} is lower than 2.0V. It is recommended that a 1kΩ maximum resistor be connected from OVP to ground, to insure that this leakage current does not charge an external SCR gate.

Figure 19 shows the UC3910 driving an external SCR. The UC3910 OVP signal, when high, will source a minimum of 65mA. Many SCRs require a

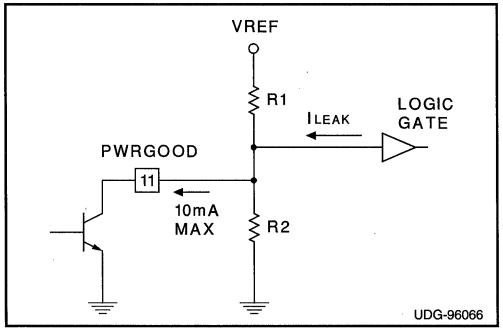

Figure 16. Add a Pull-down Resistor to PWRGOOD to Insure Proper Signal at $V_{CC} \leq 2$ Volts

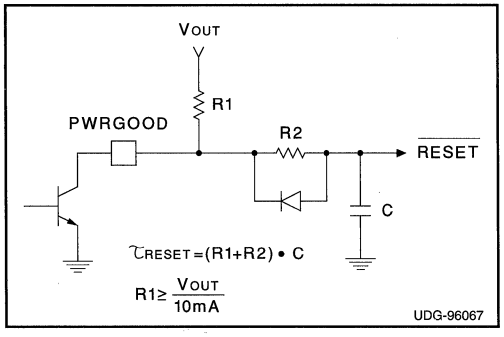

Figure 17. Using PWRGOOD to Reset the Processor

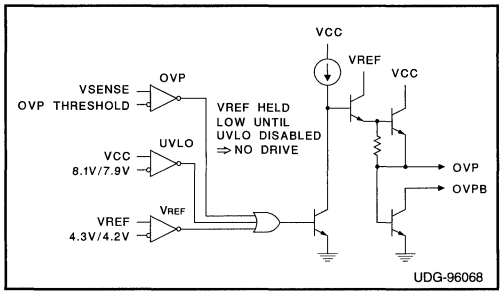

Figure 18. OVP Comparator and Drive

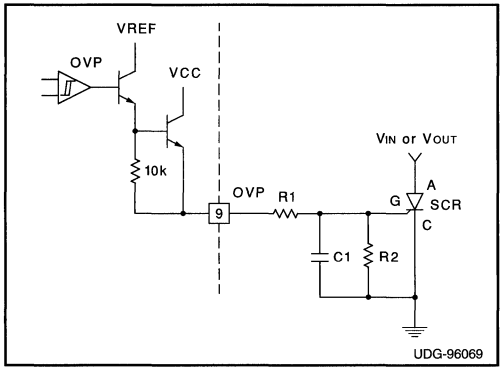

Figure 19. Driving an SCR using the UC3910 OVP Signal

gate trigger current (IGT) between 30mA and 50mA. The output high voltage will be approximately 4.3V maximum. The OVP signal is not pulled low internally to the UC3910.

Resistor R1 in Figure 19 is chosen to limit the gate current to minimize current draw on V_{CC} while insuring that the rated gate current is met. Resistor R2 is required to insure that the SCR is not inadvertently fired due to dc leakage currents or parasitic dv/dt effects through the SCR itself. C1 can be used to provide additional gate filtering, but should not be so large that the SCR gate signal is significantly delayed.

There are many tradeoffs to consider when choosing which SCR to use and where to use it to best protect critical electronics. SCR theory and various crowbar circuits are discussed extensively in literature [1] and in device data books [2].

The OVPB signal can be used to disable a power supply through a logic disable signal. This is easily accomplished when the UC3910 is used in conjunction with the UC3886 PWM controller IC, as demonstrated in Figure 20.

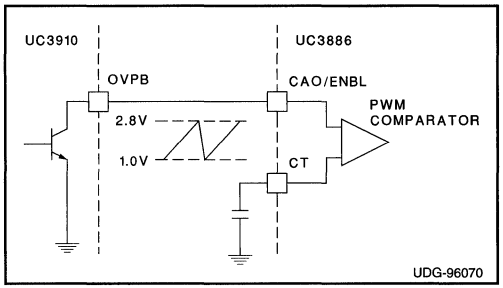

Figure 20. Disabling the UC3886 Switching Using the OVPB Signal

Circuit Example - Programming the Voltage Monitor Thresholds

Refer to Figure 9 and Figure 11, and program the UC3910 Voltage Monitor Section for the following requirements:

V_{OUTPUT} ranges from 2.4V to 3.4V (i.e., Pentium®Pro application)

F_{SWITCH} = 200kHz

Ripple voltage = 2% peak-to-peak

OV and UV Thresholds must be ±5% MINIMUM

OVP is to be set at 20% Maximum

Step 1: Choose to set the nominal overvoltage and undervoltage thresholds at 7.5% to insure that the ±5% thresholds are met.

Step 2: Calculate the ratio R_{DIV}, based on the desired 7.5%:

$R_{DIV} = 7.5/16.7 = 0.45$

Step 3: Find nominal values for RS1 and RS2

Let RS1 + RS2 draw ≈ 1.0mA at the maximum DACBUF voltage. Therefore

$$RS1+RS2 \approx \frac{3.4V}{1.0mA} \approx 3.4k\Omega$$

$$R_{DIV} = 0.45 = \frac{RS2}{RS1+RS2}$$

$RS2 = 1.54k\Omega$ $RS1 = 1.91k\Omega$

$RS1+RS2 = 3.45k\Omega$ $R_{DIV} = 0.446$

Step 4: Find the hysteresis in terms of percentage, over the 2.4V to 3.4V range:

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{557\Omega}{20k\Omega}$$

$$UV_{HYS} = -OV_{HYS}$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{1382\Omega}{20k\Omega}$$

The OV and UV hysteresis is 30mV @ 2.4V and 42mV @ 3.4V

The OVP hysteresis is 74mV @ 2.4V and 105mV @ 3.4V

Hysteresis on the OV and UV is ± 1.25%, and on the OVP is ± 3.1%

Step 5: Find V_{SENSE} filter components and calculate effective ripple at the VSENSE pin.

$$R_F \geq \frac{V_{OUTmax}}{500\mu A} \geq \frac{3.4V}{500\mu A} \geq 6.8k\Omega$$

Let $R_F = 6.8k\Omega$ as a standard 5% value.

$$C_F \geq \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

$$\geq \frac{1}{2 \bullet \pi \bullet (200kHz/10) \bullet 6.8k\Omega}$$

$$\geq 1170pF$$

Let $C_F = 1200pF$ as a standard value, giving a filter corner frequency of < 20kHz.

V_{RIPPLE} = 2% peak-to-peak • 1/10 = 4.8mV to 6.8mV peak to peak. This is well below the hysteresis ranges found in step 4.

Step 6: Solve for the thresholds. Use Figure 14 to estimate tolerances.

Nominal: $UV = -R_{DIV} \bullet 16.7 = -7.45\%$

$OV = R_{DIV} \bullet 16.7 = 7.45\%$

$OVP = OV \bullet 2.0 = 14.9\%$

Minimum OV/UV 7.45% - 2.45% = 5.00%

Maximum OV/UV 7.45% + 2.45% = 9.90%

Maximum OVP: 14.9% + 2.45% =17.35%

Step 7: Insure the time constant on VSENSE is slower than that on DACOUT

$$C_{DACOUT} \leq \frac{R_F \bullet C_F}{3k\Omega}$$

$$\leq \frac{6.8k\Omega \bullet 1200pF}{3k\Omega}$$

$$\leq 2720pF$$

Let C_{DACOUT} = 2700pF as a standard value.

SUMMARY

The UC3910 contains all the features required to command power supplies requiring custom voltages, precise regulation, programmable voltage monitoring and circuit protection. The high DC accuracy of the UC3910 reference and DAC makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Multiple discrete precision components can be replaced by the many integrated functions of the UC3910. Voltage programming is directly compatible with Intel's Pentium®Pro processor and voltage monitor threshold programming is precisely controlled with only two external resistors. Protecting the load against overvoltage can be performed with a logical shutdown or by driving a crowbar SCR.

Together with the UC3886 Average Current Mode PWM Controller IC, an optimal power supply can be designed to meet the stringent requirements of the Intel Pentium®Pro processor. For additional information on the UC3886 Average Current Mode PWM Controller IC, refer to application note U-156 [3]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [4].

REFERENCES

[1] Abraham I. Pressman, "Switching and Linear Power Supply, Power Converter Design" Switchtronix Press, 1987

[2] Thyristor Device Data Book, Motorola, Phoenix, Arizona.

[3] U-156 The UC3886 PWM Controller Uses Average Current Mode Control to Meet the Transient Regulation Performance of High End Processors, L. Spaziani

[4] U-157 Fueling the Megaprocessor - A DC/DC Converter Design Review Featuring the UC3886 and UC3910, L. Spaziani

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The UCC3884 Frequency Foldback Pulse Width Modulator

by Philip Cooke

ABSTRACT

This application note focuses on the UCC3884 frequency foldback peak current mode controller. The UCC3884 provides a solution to the current tail problem often seen in high frequency converters under overload fault conditions. Intended primarily for single-ended converters, other features such as a maximum duty-cycle clamp and an accurate volt-second clamp are also included. The block diagram and the main features of the UCC3884 will be presented in the theory of operation section. Following that a derivation of the oscillator, frequency foldback, and volt-second clamp equations are given. Finally, design details and test results for an example RCD clamp forward converter operating at 400kHz are shown.

INTRODUCTION

The output VI characteristic of high frequency, buck-derived, peak current mode converters can exhibit a current tail during current overload conditions. This overload may be caused by a short circuit condition or a low impedance at the power stage output. The current tail is actually a gradual increase in the average output current as the average output voltage decreases toward zero. The peak current limit in a PWM controller commands the power stage switch off during overcurrent conditions which should limit the maximum average output current. However, the propagation delay inherent in the controller and in the power switch during turn-off limits the minimum attainable duty cycle [1]. This minimum duty cycle limit can produce a current tail during overloads. Upon close inspection one finds that this propagation delay exists collectively between the current sense (CS pin) and the output (OUT pin) of the integrated circuit (IC) and the turn-off delay of the power stage switch. The reduction of the propagation delays for a given IC and power stage design can help, but tends to increase system cost. An alternate method is needed to reduce the delays and thus the excessive currents during a fault. One possible technique is implemented in the oscillator section of the UCC3884. During a fault condition as the output voltage approaches zero the operating frequency also decreases. By reducing the frequency during overload conditions the duty-cycle is permitted to decrease below the value previously limited by propagation delay in the constant frequency converter. The UCC3884 reduces the frequency smoothly as the load impedance approaches a short circuit, thus preventing possible latch-up with nonlinear loads [1]. This effectively diminishes the current tail in the output VI characteristic.

The UCC3884 is intended for high performance, peak current mode, single-ended applications that can benefit from frequency foldback. This frequency reduction only operates when the output voltage is below a user programmable value. More specifically, the oscillator runs at constant frequency and only folds back when the output voltage drops below a given value (e.g., 4.2V for a 5V output). A volt-second clamp circuit is also included that allows accurate duty-cycle clamping under transient line and load conditions providing an extra level of circuit protection from transformer saturation. For example, if a sudden increase in load power occurs while the input voltage increases, the applied volt-seconds could be enough to saturate the transformer, which could cause the power switch to fail. In this case, the volt-second clamp circuit could be used to prevent the failure of the power switch by overriding the control loop and limiting the applied volt-seconds. This controller also features a depletion-mode n-channel MOSFET gate drive intended to be used in the bias supply during start up. A reduction in both the size of the start up storage capacitor and turn-on time can be achieved by using an external depletion-mode device.

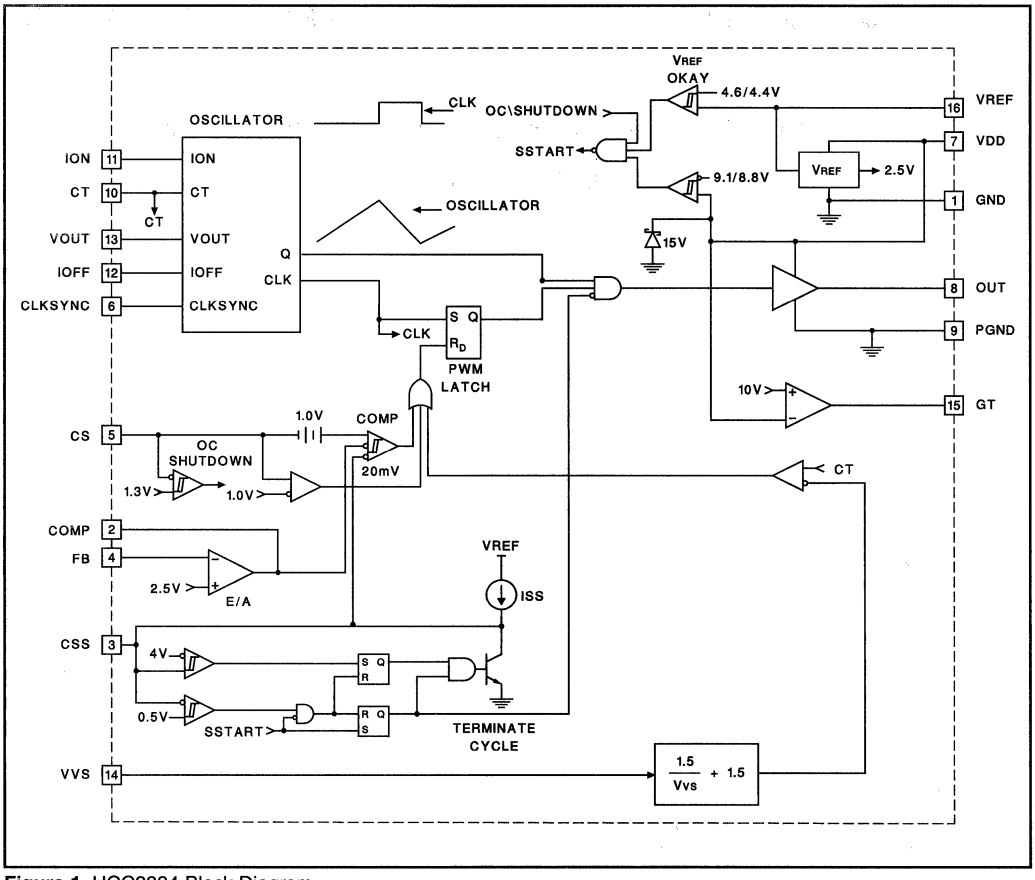

Figure 1. UCC3884 Block Diagram

THEORY OF OPERATION

The UCC3884 current mode controller, shown in Figure 1, contains a programmable oscillator section which includes the ability to synchronize multiply PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT, the connection point for the timing capacitor) have time intervals that are set by external resistors at ION and IOFF as shown in Figure 2. The nominal operating frequency is determined by the timing capacitor during non-frequency foldback conditions, that is, with the output voltage at its regulated value. The positive sloped portion of the oscillator waveform has a fixed time duration and is set by a resistor connected to ION. In a similar fashion the off-time is set by a resistor at IOFF. However, the negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. When the voltage at VOUT decreases below 3.5V, due to an output short circuit, the operating period increases and the IC is in frequency foldback operation. It should be emphasized that normal converter operation, except during start up, is at a fixed frequency.

The power supply output voltage and the voltage from VREF can be fed back into VOUT with summing resistors. This ensures a minimum frequency at startup and during short circuit conditions when the output voltage is zero. Figure 3 shows computer simulated VI curves for a 417kHz forward converter, one with frequency foldback and one without frequency foldback. The total propagation delay was set to 150ns in this computer model of a forward converter with 48V input (8:2 turns ratio). Power stage component values were L = 1.3µH with a DCR of 0.01Ω and C = 10000µF with an ESR of 70mΩ [1]. It can be seen that the current tail is reduced with frequency foldback. Figure 4 further details the effect of the propagation delay. Two simulations were done at the same operating frequency both without frequency foldback. The simulation with the current tail approaching 22A had a 150ns delay and the other

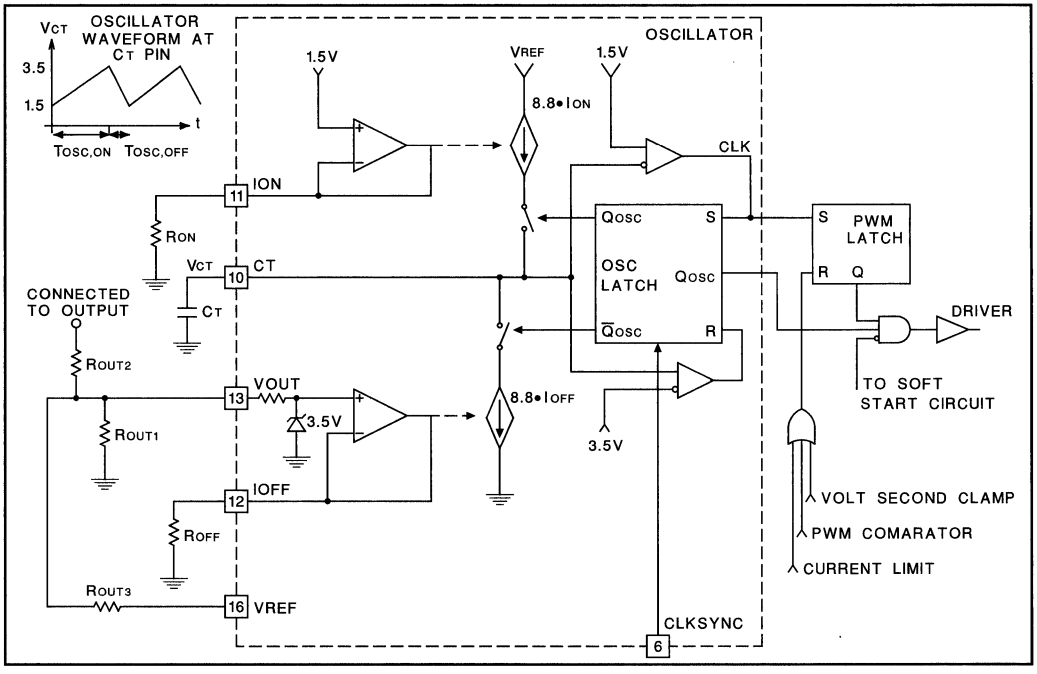

Figure 2. Functional Block Diagram of the UCC3884 Oscillator

had an unrealistic, nearly zero, 1.0ns delay. It is clear that the propagation delay can cause significant overcurrents and frequency foldback is a practical way to reduce the current tail effect.

Another feature included in the UCC3884 is an interface to drive an external depletion-mode MOSFET during power supply startup until the bootstrap winding exceeds a 10V threshold. At which time the depletion-mode MOSFET is turned-off. The internal amplifier controlling this MOSFET has 300mV of hysteresis to avoid oscillation during power-up.

An accurate programmable volt-second method to clamp the duty-cycle is implemented. It is configured so that the duty-cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, assuming regulation, the operating duty-cycle is a fixed value. The volt-second clamp duty-cycle may then be set somewhat higher than this operating duty-cycle. Since the volt-second duty-cycle limit is inversely proportional to V_{IN} at any other constant input voltage level, the volt-second clamp will still exceed

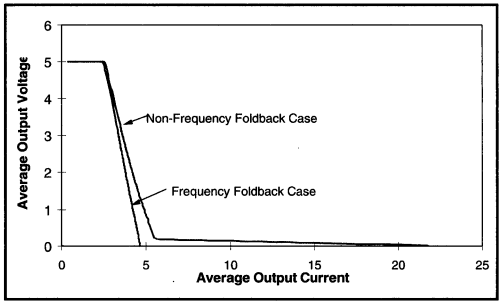

Figure 3. Frequency and Non-Frequency Foldback Comparision

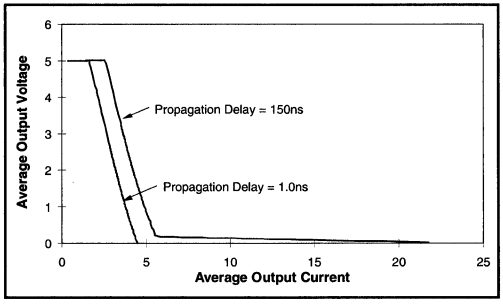

Figure 4. Non-Frequency Foldback with 1.0ns and 150ns Propagation Delays

the steady state operating duty-cycle as shown in Figure 5. This allows normal current-programmed closed-loop operation of the converter without the volt-second duty-cycle limit interfering with the control. For example, during a load transient and possibly an input voltage transient the volt-second clamp can accurately limit the maximum applied volt-seconds by limiting the duty-cycle. This ensures that the transformer does not saturate during a fault which could otherwise fail the power supply. After the fault passes the converter will go back into regulation.

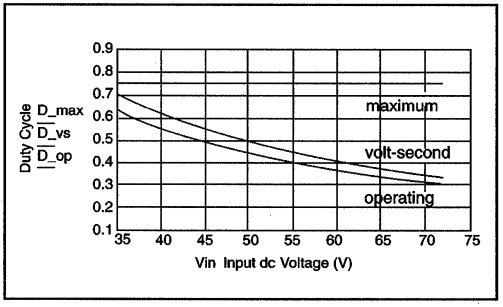

Figure 5. Various Duty Cycles

An external capacitor may be connected to CSS which provides for a soft-start and also allows the IC to be disabled with an external transistor. The frequency foldback and the soft-start functions will both be in effect during power-up since the output voltage fed back to the VOUT pin is less than 3.5V and the voltage on CSS is less than 4V. The increasing on-time at the OUT pin during soft-start is controlled by C_{SS} and the period is controlled by the frequency foldback circuitry. When an overload or short circuit occurs the frequency foldback circuit and possibly the volt-second clamp circuit is activated (assuming the overcurrent is not triggered). In each design the steady state VI characteristic produced by the frequency foldback circuit should be compared to the load VI curve to be certain that the converter will start under load.

The current sense feedback pin has an over current protection feature which forces a soft-start cycle only if the IC is not currently in a soft-start cycle. A voltage bias of 1.0V is added to the voltage sensed on the CS pin in order to facilitate zero duty-cycle when the error amplifier's output is less than 1.0V. The PWM latch is reset dominant so that if the error amplifier output is below 1.0V the output of the latch is not driven high.

The error amplifier is unity gain stable and has a wide gain-bandwidth product for accuracy. Its non-inverting input is internally set to 2.5V.

DETAILED DESCRIPTION AND DESIGN EQUATIONS

A description of the UCC3884 BiCMOS pulse width modulator and design equations will be presented followed by an example RCD Clamped Forward Converter design using the UCC3884 peak current mode controller [2,3,4].

Oscillator and Frequency Foldback Section:

The oscillator section has an independently programmable frequency and a maximum duty-cycle clamp. A single resistor sets the timing capacitor (CT) charge current which creates the positive slope portion of the oscillator waveform. A second resistor sets the timing capacitor discharge time. With reference to Figure 2 the oscillator waveform increases linearly from 1.5V to 3.5V and decreases linearly back to 1.5V completing one cycle. If T_{OSCon} represents the charge time and T_{OSCoff} is the discharge time then the frequency of the converter is given by

$$f = \frac{1}{T_{OSCon} + T_{OSCoff}} . \quad (1)$$

The output of the modulator can only be asserted during the positive slope portion of the oscillator waveform. With this limitation the maximum duty-cycle is given by the ratio of T_{OSCon} to $T_{OSCon} + T_{OSCoff}$;

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} . \quad (2)$$

The oscillator off-time is a function of the main output voltage only if the VOUT pin drops below 3.5V. The VOUT pin may exceed 3.5V in which case the off-time is calculated using 3.5V. Note that the IC does not internally clamp this voltage to 3.5V. If the output is short circuited or a low impedance load is applied the feedback voltage to the VOUT pin decreases which causes T_{OSCoff} to increase. This will increase the period and therefore decrease the frequency.

Recall that the oscillator on-time (T_{OSCon}) is constant and does not vary with output voltage. Under nominal operating conditions the frequency is constant and equation 1 can be expanded to

$$f = \frac{1}{\frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} + \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{OFF}}} = \quad (3)$$

$$\frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} =$$

$$\frac{4.4}{C_T \bullet \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5}\right)}$$

where C_T is the timing capacitor, R_{ON} sets the value of the C_T charging current, (8.8 • I_{ON}), and R_{OFF} sets the value of the C_T discharging current, (8.8 • I_{OFF}). The maximum current sourced from the ION and IOFF pins is limited to approximately 800µA.

To avoid start up problems, a resistor can be added from VREF to VOUT which provides a voltage bias to VOUT even when the output voltage is zero. The choice of value also sets the minimum operating frequency during frequency foldback, as will be reviewed in the example design section below.

Designs using an isolation transformer can derive a dc voltage level proportional to the output by using a peak detector circuit off of the bootstrap winding of the power transformer (Figure 8). This bias supply is normally required for isolated converters and therefore requires only a minimum of components.

Figure 6 shows the oscillator and frequency foldback portions of the UCC3884, where V_X is found by assuming no limiting action within the VOUT pin (see also Figure 2). V_X is given as

$$V_X = \frac{R_{OUT1} \parallel R_{OUT2}}{R_{OUT1} \parallel R_{OUT2} + R_{OUT3}} \bullet V_{REF} + \frac{R_{OUT1} \parallel R_{OUT3}}{R_{OUT1} \parallel R_{OUT3} + R_{OUT2}} \bullet V_O \quad (4)$$

where V_{REF} = 5V, V_O is the output voltage, and || represents parallel resistors. If equation 4 yields a V_X greater than 3.5V it would then be replaced with 3.5V. One possible design approach would be to ignore the loading of R_{OUT3} and set V_X slightly below the output voltage minus one-half of the maximum ripple voltage. With R_{OUT1} and R_{OUT2} known, set V_O = 0 and R_{OUT3} may be calculated based upon the minimum operating frequency desired.

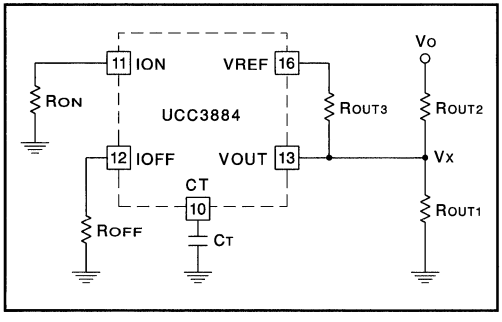

Figure 6. Oscillator and Frequency Foldback Connections to the UCC3884

Synchronization of Multiple ICs:

A CLKSYNC pin is provided which is used to synchronize two or more UCC3884 ICs. Multiple ICs are synchronized in frequency by connecting their CLKSYNC pins with capacitors to the CLKSYNC bus as shown in Figure 7. Each free running oscillator is designed with the same base frequency and the same maximum duty-cycle and is connected to the CLKSYNC bus with a capacitor and a pull-down resistor. A negative edged pulse from any IC will initialize all the ICs to start the upslope of their oscillator waveforms. For a given oscillator on the down-slope, if it receives a negative synchronization pulse before it reaches the 1.5V threshold, an internal MOS switch will quickly discharge its C_T down to 1.5V. After soft-start synchronization for each controller may take one or two cycles to come into lock. During frequency foldback under an output fault condition, the synchronization in the overloaded IC is inhibited and the converters can become unlocked. This is necessary since the overloaded ICs frequency is in foldback. The oscillators will resynchronize when the fault is removed. Due to tolerances, each free running oscillator frequency may be slightly different; therefore the CLKSYNC bus synchronizes to the highest frequency. For multiple PWM converters, synchronization to other controllers is only possible when the VOUT pin is greater than 3V.

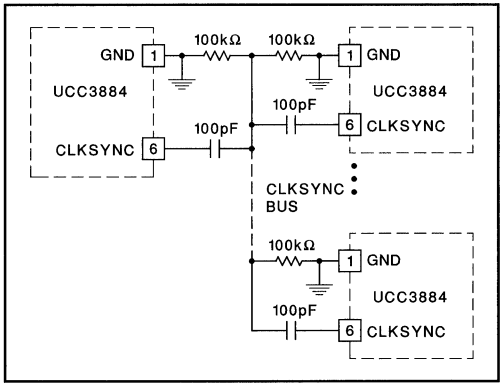

Figure 7. Oscillator Synchronization Connection Diagram

Volt-Second Clamp:

The volt-second duty-cycle clamp operates by taking the reciprocal of the voltage on VVS (see Figure 1) which is directly proportional to the input voltage and uses this signal to limit the duty-cycle. As V_{IN} increases, to maintain constant operating volt-seconds for a forward converter, the duty-cycle

decreases based upon

$$D_{OP} = \frac{V_O + V_D}{(V_{IN} - V_{DSon}) \bullet \frac{N_S}{N_P}}; \quad (5)$$

where D_{OP} is the operating duty-cycle, V_{DSon} is the on-state drain-to-source primary switch voltage, N_S is the secondary turns, N_P is the primary turns, and V_D is the voltage drop of the secondary rectifier diode [5]. In a similar fashion, the maximum duty-cycle clamp due to this volt-second function will also decrease and is given by

$$D_{VS} = \frac{K}{V_{VS}} \bullet \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} \quad (6)$$

$$= 1.1 \bullet \frac{D_{MAX}}{V_{VS}}$$

where D_{VS} is the duty-cycle clamp based upon applied volt-seconds to the transformer, V_{VS} is the voltage on the VVS pin, and K was calculated from

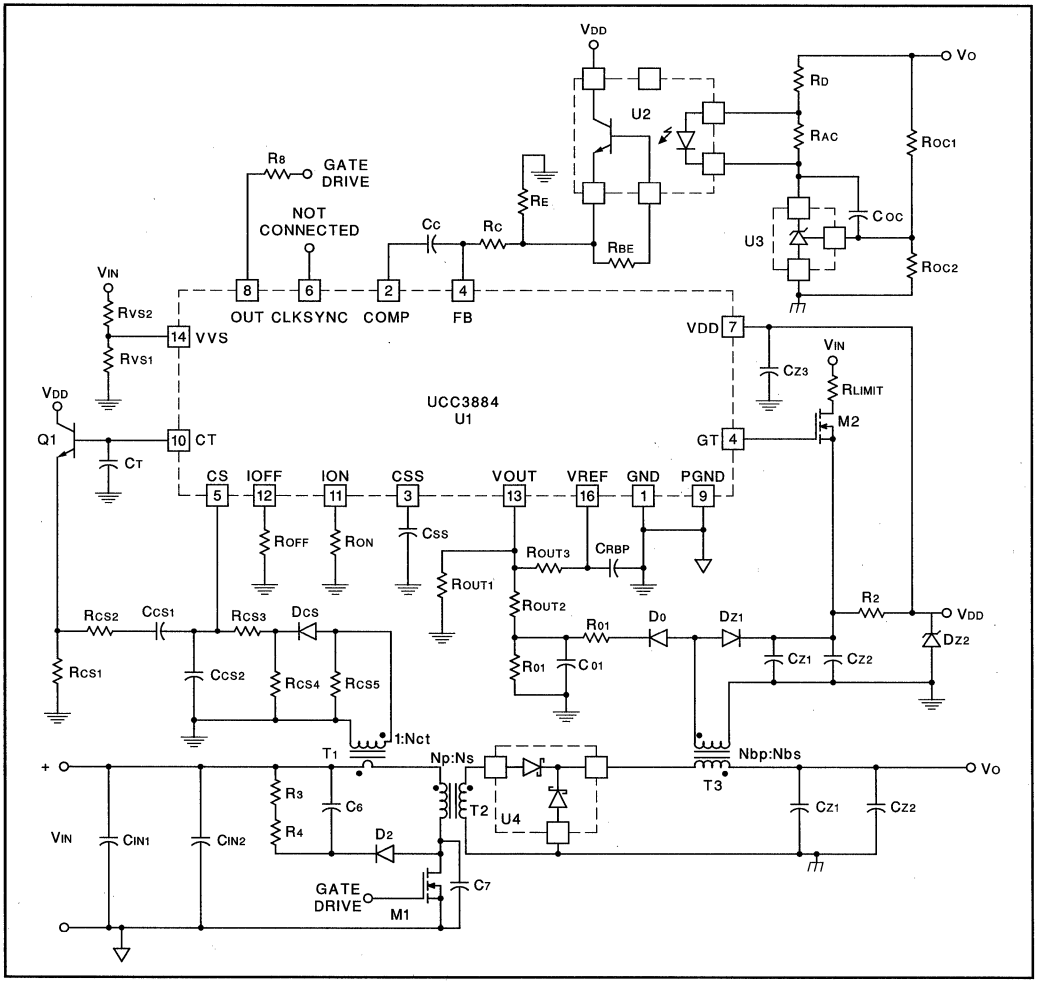

Figure 8. RCD Clamp Forward Converter with Frequency Foldback

the UCC3884 data sheet. The volt-second clamp is set by an external resistor divider network from the input voltage to the VVS pin. Normally, D_{VS} is chosen to exceed D_{OP} by some fixed percentage, say 10%. It may be necessary to put a small ceramic capacitor at the VVS pin to filter switching noise.

This feature allows for an accurate volt-second clamp within the input voltage range under load transient conditions. It is accurate since the timing capacitor tolerance does not effect equation 6. The voltage at VVS can be provided by 1% resistors and the internal accuracy is maintained to 3% (for the 0°C to 70°C temperature range). To limit the on-time at the minimum input voltage the maximum possible duty-cycle is clamped by D_{MAX}. The converters' actual duty-cycle can be limited by either the volt-second clamp or the maximum programmable duty-cycle clamp depending on operating conditions.

Soft-Start Operation:

A constant current source ISS, set internally to 20µA, charges C_{SS} to a clamped voltage level of typically 5.0V. The soft-start time is given by $3.5 \bullet C_{SS}/I_{SS}$. During start up the PWM comparator selects the minimum of either the error amplifier output or the soft-start capacitor voltage. The output duty-cycle is therefore slowly increased as the voltage at CSS increases. At some point the error amplifier voltage is lower and the voltage loop is closed. An overcurrent fault will initiate a soft-start cycle by first discharging C_{SS} and then slowly recharging the capacitor until the voltage returns to 4V. Soft-start discharge can only be activated when the voltage at C_{SS} exceeds about 4V.

Under Voltage Lockout Features:

The converter is disabled until VREF exceeds 4.6V and VDD exceeds 9.1V. Once these levels are reached the converter will begin the soft-start sequence. If VREF falls below 4.4V or VDD decreases below 8.8V the converter will immediately discharge C_{SS} and then start up again when VREF exceeds 4.6V and VDD exceeds 9.1V.

DESIGN EXAMPLE

A forward converter with an RCD clamp and a maximum of 75% duty-cycle at 400kHz was designed as shown in Figure 8 [1,2,3,4,6]. The input voltage range is 35V to 72Vdc with a 5V output. The highest operating duty-cycle is set to about 65% and will occur at the minimum input voltage during normal conditions. A maximum duty-cycle limit ensures reset of the transformer at low line.

Power Circuit Design:

A high frequency forward converter topology is often used in telecommunications applications requiring battery input from 35V to 72V DC with 48V nominal. A common output voltage is 5V and in this design a large capacitor, 10000µF, will be used to smooth the low frequency ripple components in order to more accurately measure average load currents during overload conditions. The output inductor was selected to be 1.3µH with a coupled winding for the bootstrap circuit (5:2 turns ratio). The transformer primary to secondary turns ratio is 8:2 and a RCD clamp is used to reset the transformer during the switch off-time. The laboratory prototype was built using higher rated components than necessary (maximum of 178W). This was done since constant measurement of short circuit fault currents without frequency foldback could cause excessive power dissipation.

Oscillator Design:

The oscillator on-time can be found, assuming D_{MAX} and f is known, by solving

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} = T_{OSCon} \bullet f \quad (7)$$

for T_{OSCon} yielding

$$T_{OSCon} = \frac{D_{MAX}}{f} = \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} = \frac{C_T}{4.4 \bullet I_{ON}} . \quad (8)$$

From equation 1, T_{OSCoff} becomes

$$T_{OSCoff} = \frac{1}{f} - T_{OSCon} \quad (9)$$

The oscillator operating frequency is given by

$$f = \frac{1}{2 \bullet 10^4 \bullet C_T} . \quad (10)$$

Solving for C_T yields

$$C_T = \frac{1}{2 \bullet 10^4 \bullet f} . \quad (11)$$

With T_{OSCon} and C_T known, I_{ON} may be found from equation 8

$$I_{ON} = \frac{C_T}{4.4 \bullet T_{OSCon}} . \quad (12)$$

Now R_{ON} is given by

$$R_{ON} = \frac{1.5}{I_{ON}} . \quad (13)$$

The next step is to calculate the maximum value of I_{OFF} which occurs during non-frequency foldback conditions. A portion of equation 3, repeated below,

$$f = \frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} \quad (14)$$

may be solved for I_{OFF} yielding

$$I_{OFF} = \frac{0.227 \bullet C_T \bullet f \bullet I_{ON}}{I_{ON} - 0.227 \bullet C_T \bullet f} . \quad (15)$$

Finally, the R_{OFF} resistor value is

$$R_{OFF} = \frac{3.5}{I_{OFF}} \quad (16)$$

These equations are used in a Mathcad spreadsheet listed in Appendix I [7].

Frequency Foldback Design:

The three resistors associated with frequency foldback may now be calculated. A useful approach is to first ignore the loading from the VOUT pin and ignore the R_{OUT3} connection. To allow for a small decrease in the output voltage before frequency foldback kicks in (this is not a requirement, but can be used to guarantee constant frequency operation under the expected output voltage ripple) set $V_X = 4V$ and from Figure 6 one can write

$$V_X = 4 \approx \frac{R_{OUT1}}{R_{OUT1} + R_{OUT2}} \bullet V_O \quad (17)$$

where V_O is the actual output voltage. By arbitrarily selecting R_{OUT1}, the value of R_{OUT2} can be determined. Now, the selection of R_{OUT3} determines the minimum frequency of operation. Rewriting equation 16 for the general case (when the VOUT pin is less than 3.5V)

$$V_X = R_{OFF} \bullet I_{OFF} . \quad (18)$$

Setting V_O equal zero in equation 4 one solves

$$V_X = \frac{R_{OUT1} \,||\, R_{OUT2}}{R_{OUT1} \,||\, R_{OUT2} + R_{OUT3}} \bullet V_{REF} \quad (19)$$

for R_{OUT3}. With R_{OUT1}, R_{OUT2}, and R_{OUT3} known, equation 4 can be used in a Mathcad spreadsheet to plot operating frequency of the converter as a function of the output voltage. Listed in Appendix I is an example of the spreadsheet which includes the calculations and graphs of the steady state volt-second clamp and frequency foldback characteristics.

Volt-Second Clamp Design:

The voltage at the VVS pin is given by

$$V_{VS} = \frac{R_{VS1}}{R_{VS1} + R_{VS2}} \bullet V_{IN} \quad (20)$$

once R_{VS1} is selected R_{VS2} can be solved for after D_{VS} is chosen. From equation 6

$$V_{VS} = K \bullet \frac{D_{MAX}}{D_{VS}} \quad (21)$$

as an example D_{VS} may be set to 110% of D_{OP}. For this case, after solving for R_{VS2} in equation 20 with V_{VS} replaced using equation 21, one finds

$$R_{VS2} = R_{VS1} \bullet (V_{IN} \bullet \frac{D_{OP}}{D_{MAX}} - 1) . \quad (22)$$

Control Loop Component Calculations:

The concentration of this application note is to show the characteristics of the frequency foldback and volt-second clamp features of the UCC3884. Details of the small-signal modeling of the modulator and power circuit can be found in [8] and [9]. Integral compensation was used to set the crossover frequency to 9kHz with a gain of about 7dB needed at this frequency.

EXPERIMENTAL RESULTS

The RCD clamp forward converter was prototyped in the laboratory and relevant results are presented in the following section.

Frequency Foldback Data:

The primary current sense resistor in Figure 8 was increased to 32Ω from 16Ω (16Ω was used in the computer model that generated Figures 3 and 4) in order to limit the average load currents to reasonable values for easy measurement. The previous simulation results showed the basic phenomena of the current tail with and without frequency foldback. Due to effects not included in the computer model the experimental data differs from the simulated data. The computer model is a powerful tool to gain a fundamental understanding of the large signal VI characteristics as shown in Figures 3 and 4. It may be possible to take into account ignored complications so that the simulated results match

more closely the experimental data. It is thought that some of these effects could be the saturation of the magnetics (output inductor), errors in estimating the finite turn-off time of the MOSFET power stage switch and possible saturation of the primary current sense transformer. Despite these measurement inaccuracies the frequency foldback operation does reduce the current tail as compared to non-frequency foldback operation and this can be seen in the simulation results and the actual circuit measurement data.

Figure 9 shows normal operation at constant frequency with about a 4A average load current. The top waveform is the output voltage (5V, channel 3) followed by the oscillator waveform measured at

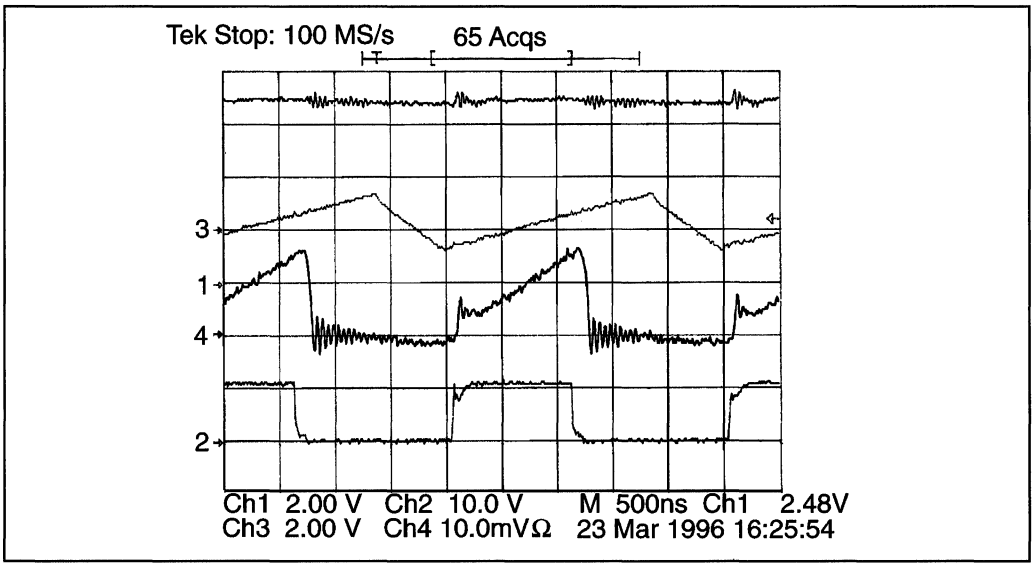

Figure 9. Converter Output Voltage, Oscillator Waveform, Primary Side Current During Normal Operation, and MOSFET Gate Voltage

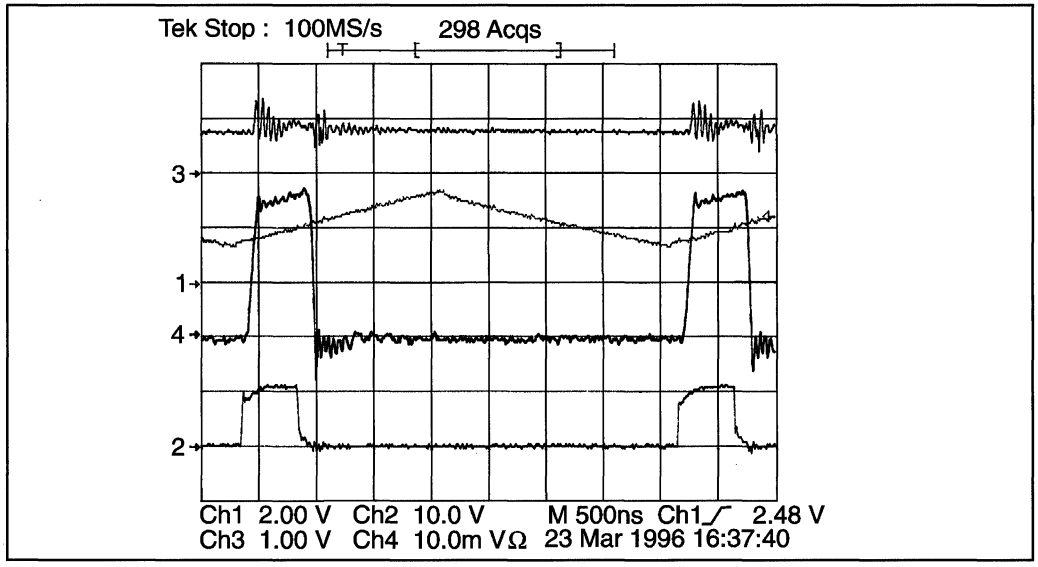

Figure 10. Converter Output Voltage, Oscillator Waveform, Primary Side Current During a Low Impedance Load Fault, and MOSFET Gate Voltage

pin 10 (CT, channel 1). Note that for small values of C_T the scope probe capacitance on pin 10 can decrease the frequency. The third from the top is the primary side current at 1A/div (channel 4). Note that there is a 470pF capacitor in parallel with the MOSFET primary switch to reduce clamp loss [2]. The bottom trace is the gate voltage at pin 8 (OUT, channel 2) which drives an IRF630 through a 13Ω resistor.

A low impedance load was applied and the resulting converter waveforms are shown in Figure 10 with the same scales as used in Figure 9 except the output voltage scale was decreased and the primary current scale on the AM503B was increased from 1A/div to 2A/div (channel 4). The average load current was 17.4A and the frequency was reduced from 403kHz to 267kHz. The output voltage decreased from 5.016V to 0.880V.

A toggle switch was used to change from frequency foldback to non-frequency foldback operation. This allowed direct comparison between frequency foldback and non-frequency foldback operation as the load resistance decreased. Figure 11 shows the data taken under the same conditions with and without frequency foldback. It was found that a fan was helpful in keeping the sense resistors cool in order to avoid drift during current measurement. The shape of the curves in Figure 11 differ from Figure 3, obviously the computer model has not taken into account all of the parasitic and saturation effects. The value of R_{OUT3} calculated in Appendix I was increased to 33.1k to generate the frequency foldback curve shown in Figure 11. The actual measured frequency versus output voltage is shown in Figure 12.

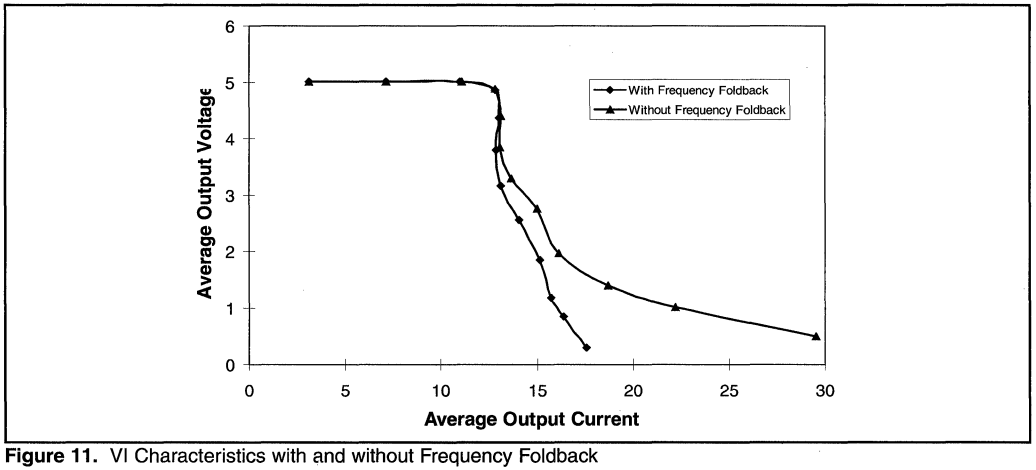

Figure 11. VI Characteristics with and without Frequency Foldback

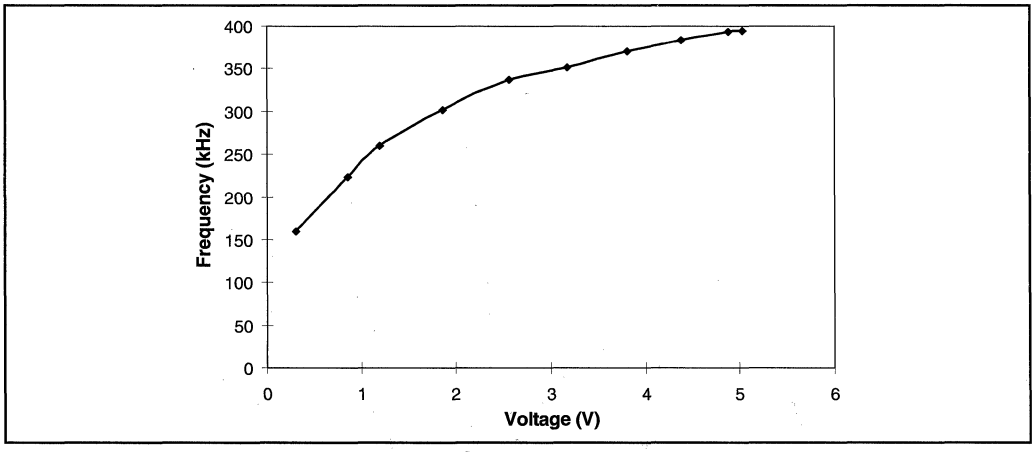

Figure 12. Measured Frequency versus Measured Output Voltage

SUMMARY

The UCC3884 peak current mode controller provides the designer a frequency foldback scheme to reduce the current tail often seen in high frequency buck derived converters. A possible practical design approach in the prototype circuit is to set the minimum frequency to about 1/3 of the nominal frequency and to use the simplified analysis outlined above to give first pass circuit values for the frequency foldback resistors R_{OUT1}, R_{OUT2}, and R_{OUT3}. During testing of the power converter low impedance loads can be applied for final adjustment of the frequency foldback resistors and to verify desired operation. The maximum duty-cycle clamp and volt-second clamp may be used to enhance performance and reliability of the power converter system. The undervoltage lockout, clock synchronization, depletion-mode MOSFET driver, and soft-start functions are all provided to complete a feature rich peak current mode controller within a 16 pin DIL package.

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Appendix I: Oscillator and Volt-Second Calculations

High Performance UCC3884 PWM with Frequency Foldback and Volt-Second Clamp
Mathcad design worksheet. by Philip Cooke

Specifications:

Input Votage	35V<Vin<72V
Output voltage	5V dc
Operating frequency	400 kHz

$f := 400 \cdot 10^3$ Estimated operating frequency (for non-frequency foldback conditions).

$D\_max := 0.75$ Maximum duty-cycle.

$N := \frac{8}{2}$ Primary transformer turns ratio.

$Vt := 3.5$ Peak oscillator voltage.

$Vb := 1.5$ Minimum oscillator voltage.

$Vd := 0.5$ Estimated voltage drop on secondary forward diode.

$Kon := 8.8$ Ion multiplier to charge Ct.

$Koff := 8.8$ Ioff multiplier to discharge Ct.

$K := 1.1$ Volt-second constant.

$Vds\_on := 0.15$ Approximate voltage drop of primary switch.

$Vout := 5$ Output dc voltage.

$Vref := 5$ Output of on-board UCC3884 regulator.

$Vin\_min := 35$ Minimum input voltage.

$Vin\_max := 72$ Maximum input voltage.

Oscillator Calculations:

Calculate the timing capacitor from the frequency:

$Ct := \frac{1}{2 \cdot 10^4 \cdot f}$ which gives $Ct = 1.25 \cdot 10^{-10}$ select $Ct := 120 \cdot 10^{-12}$

Recalculate operating frequency, $f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ so that $f = 4.167 \cdot 10^5$

The oscillator on time is given by equation 8 $Tosc\_on := \frac{D\_max}{f}$ $Tosc\_on = 1.8 \cdot 10^{-6}$

Now from equation 12, calculate Ion

$Ion := \frac{Ct}{4.4 \cdot Tosc\_on}$ so that $Ron := \frac{Vb}{Ion}$ $Ron = 9.9 \cdot 10^{4}$

Ioff is found from equation 15 $Ioff := \frac{0.2273 \cdot Ct \cdot f \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot f}$ $Ioff = 4.548 \cdot 10^{-5}$

Finally, Roff is $Roff := \frac{Vt}{Ioff}$ $Roff = 7.696 \cdot 10^{4}$

Checking the Kon*Ion and Koff*Ioff values to be sure they don't exceed 800 mA:

$Kon \cdot Ion = 1.333 \cdot 10^{-4}$

$Koff \cdot Ioff = 4.002 \cdot 10^{-4}$

Frequency Foldback Calculations:

Set Rout1 to 4.99 kW. $Rout1 := 4.99 \cdot 10^{3}$

Rearranging equation 17 to solve for Rout2: $Rout2 := \frac{Rout1}{4} \cdot Vout - Rout1$ $Rout2 = 1.248 \cdot 10^{3}$

The minimum frequency is selected to be 1/3.3 of the nominal frequency; now Ioff minimum can be calculated from equation 15:

$$Ioff := \frac{0.2273 \cdot Ct \cdot \frac{f}{3.3} \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot \frac{f}{3.3}} \qquad Ioff = 4.457 \cdot 10^{-6}$$

With Ioff equation 18 is used to find the minium value of Vx

$Vx := Roff \cdot Ioff$

With $Vx = 0.343$ V Rout3 is given by (equation 19):

$$Rout3 := \frac{Rout1 \cdot Rout2}{Rout1 + Rout2} \cdot \left(\frac{Vref}{Vx} - 1 \right) \qquad Rout3 = 1.355 \cdot 10^{4}$$

Volt-Second Calculations:

Choose 10 kW for Rvs1 and set D_vs = 1.467*D_max; $Rvs1 := 10 \cdot 10^3$

Calculate the operating duty-cycle at Vin_min. $Dop := \frac{Vout + Vd}{(Vin\_min - Vds\_on) \cdot \frac{1}{N}}$

From equation 22 $Rvs2 := Rvs1 \cdot \left(\frac{Vin\_min \cdot Dop}{D\_max} - 1 \right)$ $Rvs2 = 2.846 \cdot 10^5$

Final Selection of Components:

$Rout1 := 4.99 \cdot 10^3$ $Rout2 := 2.00 \cdot 10^3$ $Ron := 100 \cdot 10^3$ $Roff := 76.8 \cdot 10^3$

$Rout3 := 13.7 \cdot 10^3$ $Ct := 120 \cdot 10^{-12}$ $Rvs1 := 10 \cdot 10^3$ $Rvs2 := 287 \cdot 10^3$

Recalculate Ion, Ioff, f, Tosc_on, and Tosc_off:

$Ion := \frac{Vb}{Ron}$ $Ion = 1.5 \cdot 10^{-5}$ $Kon \cdot Ion = 1.32 \cdot 10^{-4}$

$Ioff := \frac{Vt}{Roff}$ $Ioff = 4.557 \cdot 10^{-5}$ $Koff \cdot Ioff = 4.01 \cdot 10^{-4}$

$f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ $f = 4.167 \cdot 10^5$

$Tosc\_on := \frac{Ct}{4.4 \cdot Ion}$ $Tosc\_on = 1.818 \cdot 10^{-6}$

$Tosc\_off := \frac{1}{f} - Tosc\_on$ $Tosc\_off = 5.818 \cdot 10^{-7}$

Derive Equations to Plot:

$i := 0, 1 .. 100$ Set up a range variable.

$Vin_i := Vin\_min + \left(\frac{Vin\_max - Vin\_min}{100} \right) \cdot i$ Use i as a parameter to vary Vin.

$$Vo_i := Vout \cdot \left(1 - \frac{i}{100}\right)$$

Vary Vo parametry with i.

$$D\_op_i := \frac{Vout + Vd}{\left(Vin_i - Vds\_on\right) \cdot \frac{1}{N}}$$

Calculate the steady state operating duty-cycle as a function of input voltage.

The Vx voltage is calculated assuming no clamp or load of the VOUT pin:

$$Vx_i := \frac{\frac{Rout1 \cdot Rout3}{Rout1 + Rout3}}{\left(\frac{Rout1 \cdot Rout3}{Rout1 + Rout3} + Rout2\right)} \cdot Vo_i + \frac{\frac{Rout1 \cdot Rout2}{Rout1 + Rout2}}{\left(\frac{Rout1 \cdot Rout2}{Rout1 + Rout2} + Rout3\right)} \cdot Vref$$

Next, the 3.5V limit is taking care of by the Mathcad conditional if statement:

$$Vout_i := if\left(Vx_i > 3.5, 3.5, Vx_i\right)$$

Now the Ct discharge current, Tosc_off, and f can be found as a function of Vout;

$$Ioff_i := \frac{Vout_i}{Roff} \qquad Tosc\_off_i := \frac{(Vt - Vb) \cdot Ct}{Koff \cdot Ioff_i} \qquad f_i := \frac{1}{Tosc\_on + Tosc\_off_i}$$

A temporary variable is used to calculate the voltage at the VVS pin as the input voltage varies. Stop gaps of 0.6V and 4.5V are assumed.

$$Vtemp_i := \frac{Rvs1}{Rvs1 + Rvs2} \cdot Vin_i$$

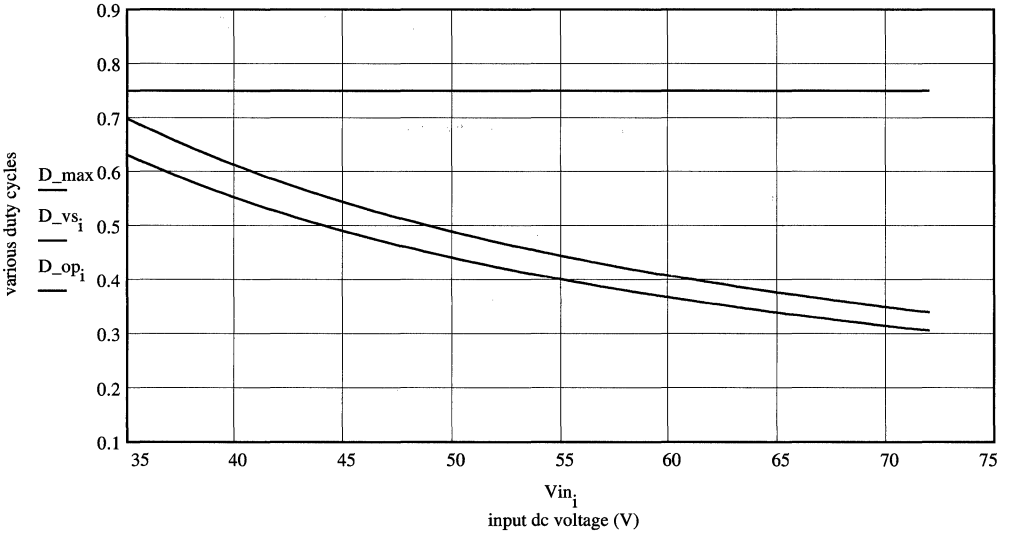
$$Vvs_i := if\left(Vtemp_i < 0.6, 0.6, if\left(Vtemp_i > 4.5, 4.5, Vtemp_i\right)\right)$$

Finally, the effective volt-second duty-cycle clamp is calculated;

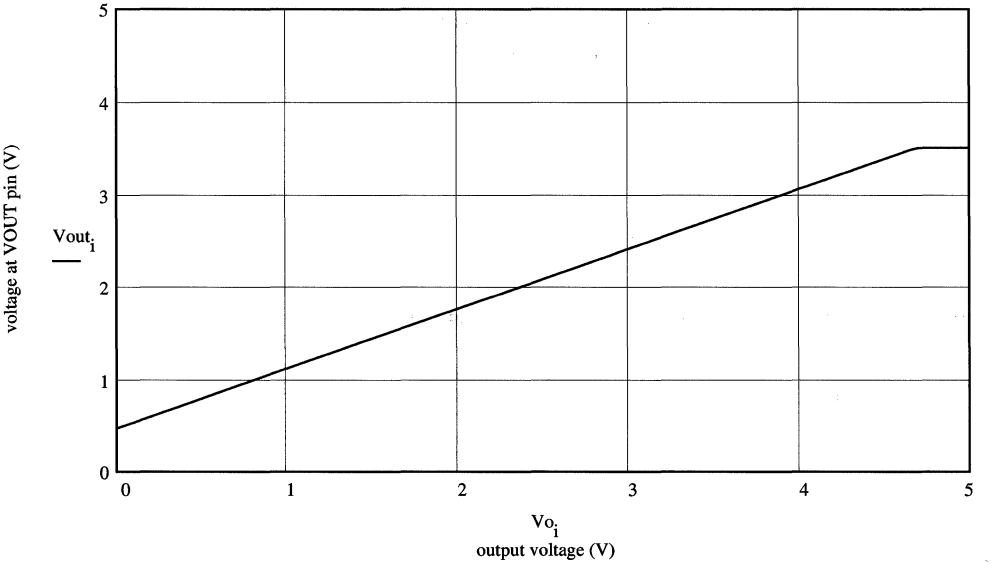
$$D\_vs_i := K \cdot \frac{D\_max}{Vvs_i}$$

Plot Expected Results:

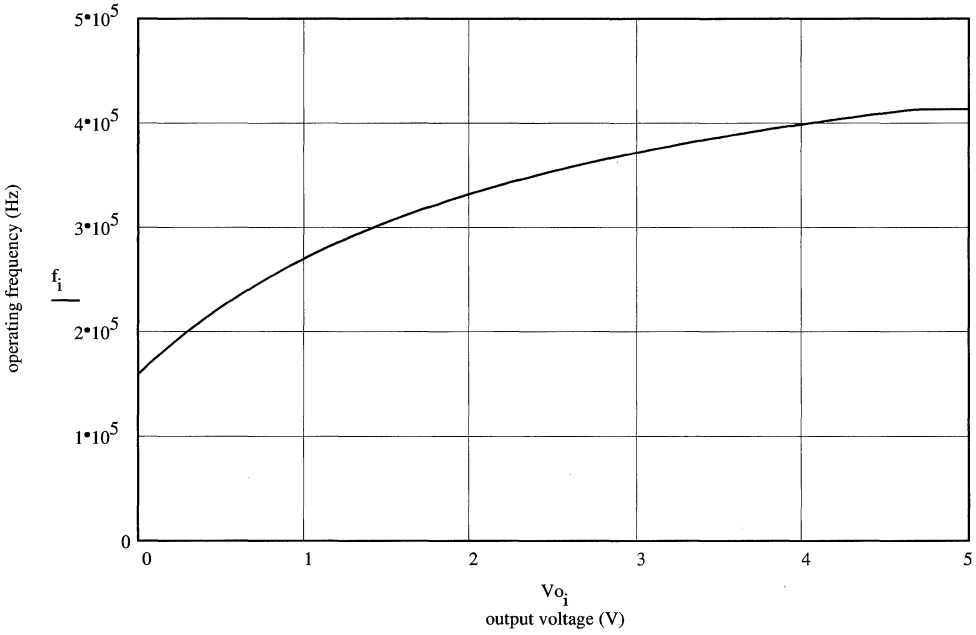
Waveforms from top to bottom; maximum duty cycle, volt-second clamp, and operating duty cycle



Voltage at the VOUT pin as the actual output voltage varies.



Frequency foldback characteristics: as the output voltage decreases the converters operating frequency decreases.



Design Review: Isolated 50 Watt Flyback Converter Using the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier

By Lisa Dinwoodie

ABSTRACT

The flyback power stage is a popular choice for single and multiple output dc-to-dc converters at power levels of 150 Watts or less. Without the output inductor required in buck derived topologies, such as the forward or push-pull converter, the component count and cost are reduced. This application note will review the design procedure for the power stage and control electronics of a flyback converter. In these isolated converters, the error signal from the secondary still needs to cross the isolation boundary to achieve regulation. By using the UC3965 Precision Reference with Low Offset Error Amplifier on the secondary side to drive an optocoupler and the UCC3809 Economy Primary Side Controller on the primary side, a simple and low cost 50 Watt isolated power supply is realized.

INTRODUCTION

The flyback converter reviewed in this application note, and available as a demonstration board ("demo board"), is specifically designed to interface with the voltage ranges used in the telecommunications industry. The primary goal of this 5V, 50 Watt power supply is an efficient design which meets all the specifications while maintaining low cost. This goal is achieved by using the UCC3809 on the primary side for fixed frequency current mode control and using the error amplifier and precision reference of the UC3965 on the secondary side. Each of these 8-pin integrated circuits requires minimal external parts resulting in an economical yet effective design. The demo board schematic is shown in Figure 1 and the list of materials is tabulated on page 17.

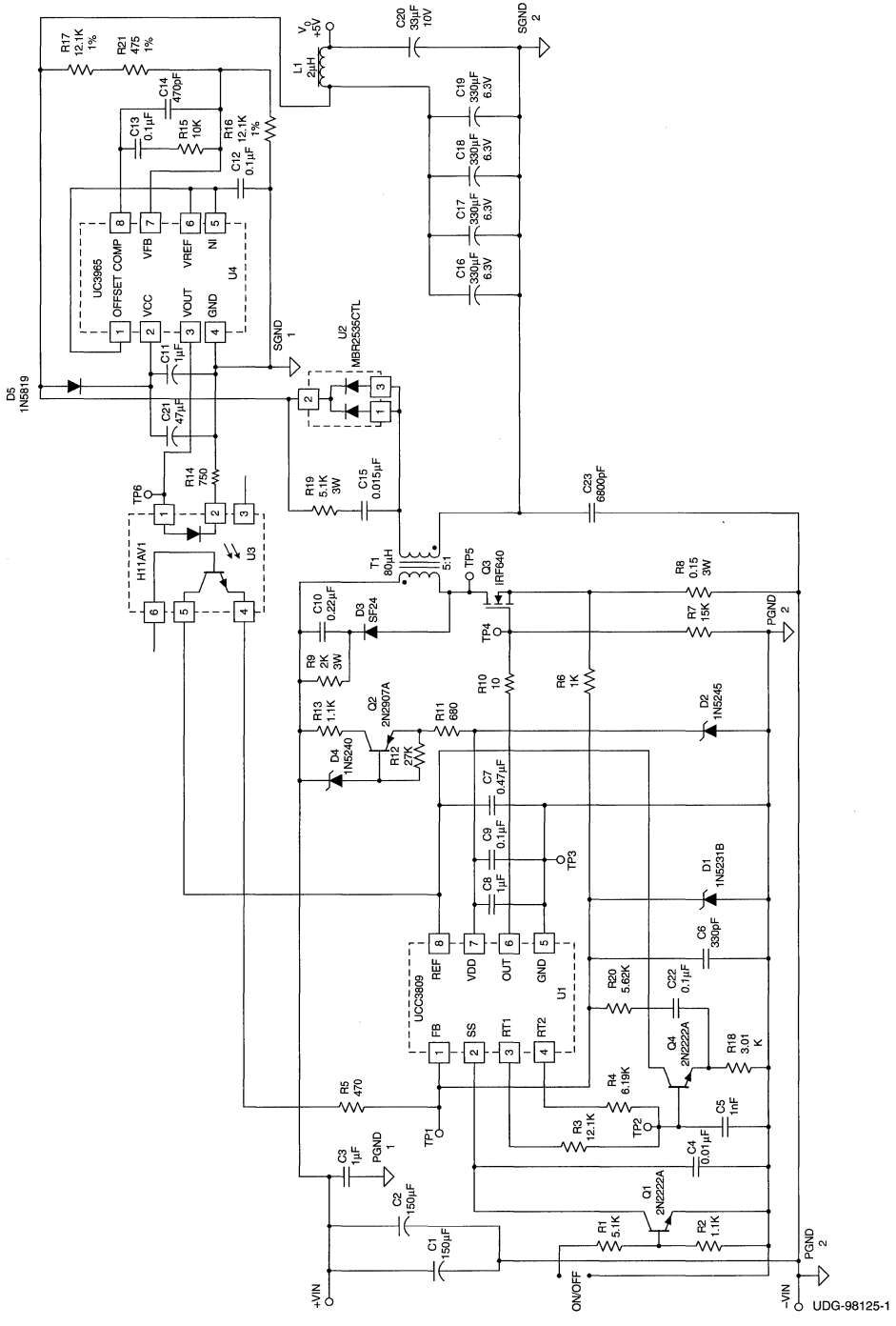


Figure 1. Schematic diagram of the –48V to +5V flyback converter available as a demo board.

POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	–72VDC to –32VDC (–48VDC nominal)
Output Voltage:	+5VDC
Load:	0A to 10A
Regulation:	±2% Over Load, Line, and Temperature
Isolation:	1500VRMS

DESIGNING THE POWER STAGE

Flyback Topology

There are many standard power converter topologies available to choose from, each with its advantages and disadvantages [1]. After careful consideration, taking into account factors such as low power, simplicity, isolation, input and output ripple currents, and low cost, the flyback configuration was chosen. The basic flyback converter topology is shown in Figure 2.

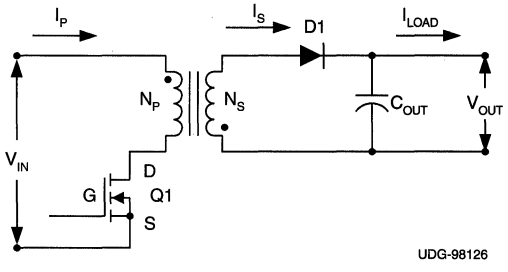


Figure 2. Flyback converter circuit configuration.

Control Method

Voltage mode control was past over in favor of current mode control because current mode control responds immediately to line voltage changes and provides inherent over current protection for the switching device. Traditional peak current mode control compares the amplified output voltage error with the primary inductor current signal. Using the UCC3809 pulse width modulator (PWM) as the controller, the amplified output voltage error and the primary inductor current ramp are summed and compared to a 1V threshold. The inner current control loop contains a small current sense resistor which senses the primary inductor current. The resistor transforms this current waveform into a voltage signal that is fed directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. The outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of the secondary side error amplifier. This divided down output voltage drives the inverting input to the error amplifier in the UC3965 which then drives an internal inverting output buffer. The resulting output then drives an optocoupler. The optocoupler output is also fed directly into the primary side PWM comparator. As the output voltage increases above the desired level, the optocoupler is driven harder on, forcing the PWM comparator to shut off the gate drive to the switching element. This outer loop determines the response to load changes.

Peak current mode control requires simpler compensation, has pulse-by-pulse current limiting, and has better load current regulation. Because the secondary currents are already quite large, continuous conduction mode (CCM) was chosen. Primary and secondary RMS currents can be up to two times higher for discontinuous mode than for CCM. Discontinuous conduction mode would require using a transistor with a higher current rating. Because the output ripple current is less than it would be if discontinuous mode were used, the output capacitors are smaller.

Continuous conduction mode has the disadvantage of requiring a higher magnetizing inductance to stay in CCM throughout the entire operating range and a right-half-plane zero in its transfer function. Feedback loop stabilization will be discussed in a later section.

Maximum Duty Cycle and Turns Ratio

Now that the topology (flyback) and control method (peak current mode control) have been decided upon, the next decision to be made is what the maximum duty cycle, D_{max}, should be. The duty cycle is the ratio of on-time of Q1, Figure 2, to total period, or $D = t_{on}/T$. In a CCM flyback converter the maximum duty cycle will determine the turns ratio of the transformer and impact the maximum voltage stress on the switching element. For this design, a maximum duty cycle of 45% was selected. Limiting the duty cycle increases the number of controller ICs to chose from because many available today have maximum duty cycle limitations of 50%.

The DC transfer function of a CCM flyback converter is:

$$\frac{V_O + V_D}{V_{IN(min)} - V_{Rds(on)}} = \frac{1}{N} \bullet \left(\frac{D_{max}}{1 - D_{max}} \right) \quad (1)$$

where V_O equals the output voltage, 5V,

V_D = forward voltage drop across rectifier D1, assumed to be 0.8V,

V_{IN} = 32 to 72V, $V_{IN(min)}$ = 32V,

$V_{Rds(on)}$ = on voltage drop across MOSFET Q1, equal to $R_{ds(on)} \bullet I_{RMS(primary)}$, assumed to be 1V,

N = turns ratio, equal to N_P/N_S,

N_S = number of transformer secondary turns,

N_P = number of transformer primary turns,

D = duty cycle.

Maximum duty cycle, 0.45, occurs at minimum input voltage. Substituting these values into (1) gives us a turns ratio of 4.37. The turns ratio is inversely proportional to the peak primary current, I_{PEAK}, but directly proportional to the voltage stress on the switching element. So the peak currents will not become unreasonably high and the voltage stress on the MOSFET will be kept as low as possible, the turns ratio is rounded up only to the next integer value, 5, or simply five primary turns for every one secondary turn. Recalculating equation (1) results in an actual D_{max} of 48%.

Switching Frequency

Because the magnetic components and filters will be smaller, the tendency is to have as high a switching frequency as possible. Unfortunately, the decision is not quite that clear cut. Core losses, gate charge currents, and switching losses increase with higher switching frequencies; peak currents and, consequently, I^2R losses increase with lower switching frequencies. A compromise must be reached between component size, current levels, and acceptable losses. Synchronization with other systems and backward compatibility may also be deciding factors. For this design, a fixed frequency (f_{sw}) of 70kHz was chosen. At D_{max} equal to 48%, $t_{on(max)}$ becomes 6.9µs.

Transformer Design [2]

The transformer in a flyback converter is actually a coupled inductor with multiple windings. Transformers provide coupling and isolation whereas inductors provide energy storage. The energy stored in the air gap of the inductor is equal to:

$$E = \frac{L_P \bullet (I_{PEAK})^2}{2} \quad (2)$$

where E is in Joules, L_P is the primary inductance in Henries, and I_{PEAK} is the peak primary current in Amperes. When the switch is on, D1 (from Figure 2) is reverse biased due to the dot configuration of the transformer. No current flows in the secondary windings and the current in the primary winding ramps up at a rate of:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_{IN(min)} - V_{Rds(on)}}{L_P} \quad (3)$$

where $V_{IN(min)}$ and $V_{Rds(on)}$ were defined previously and Δt is equal to $t_{on(max)}$ at $V_{IN(min)}$. The output capacitor, C_{OUT}, supplies all of the load current at this time. Because the converter is operating in the continuous conduction mode, ΔI_L is the change in the inductor current which appears as a positive slope ramp on a step. The step is present because there is still current left in the secondary windings when the primary turns on. When the switch turns off, current flows through the secondary winding and D1 as a negative ramp on a step, replenishing C_{OUT} and supplying current directly to the load.

Based on (3), the primary inductance can be calculated given an acceptable current ripple, ΔI_L. For the demo board design, ΔI_L was set to equal one-half the peak primary current. For a CCM flyback design, the peak primary current is calculated based upon (4).

$$I_{PEAK} = \left(\frac{I_{OUT(max)}}{N} \right) \bullet \left(\frac{1}{1 - D_{max}} \right) + \frac{\Delta I_L}{2} \quad (4)$$

By replacing ΔI_L with ½(I_{PEAK}), $I_{OUT(max)}$ with 10A, D_{max} with 0.48, and N with 5 as detailed earlier, the peak primary current is calculated to be 5.16A and ΔI_L calculates to 2.58A. The root mean square, RMS, current of a ramp on a step waveform is defined in (5) and calculates to be 2.74A for this application.

$$I_{rms} = \sqrt{\frac{t_{on(max)}}{T} \bullet \left((I_{PEAK})^2 - \Delta I_L \bullet I_{PEAK} + \frac{(\Delta I_L)^2}{3} \right)} \quad (5)$$

Using (3), L_P calculates to approximately 80µH. Due to cost considerations and a switching frequency of 70kHz, the core material was chosen to

be manganese zinc ferrite 3C85 from Philips. Because the inductor (a.k.a. the flyback transformer) is driven in one quadrant of the B-H plane only, a larger core is required in a flyback design. Because this converter is operating in the continuous conduction mode at a relatively low frequency, the maximum peak flux density, B_{max}, is limited by the saturation flux density, B_{sat}. Taking all this into consideration, the minimum core size is determined by (6).

$$AP = \left(\frac{L_P \bullet I_{PEAK} \bullet I_{rms} \bullet 10^4}{420 \bullet k \bullet B_{max}} \right)^{1.31} \quad (6)$$

where AP = the core area product in cm^4,

k = winding factor, equal to 0.2 for a continuous mode flyback,

$B_{max} \approx B_{sat}$, or 0.33 Telsa for 3C85 material at 100°C.

The result of (6) is compared to the product of the winding area, Aw (cm^2), and effective core area, Ae (cm^2), listed in the core manufacturer's data sheet. For this design, a Philips EFD30 core met the minimum criteria.

The minimum number of primary turns is determined by:

$$N_P = \frac{L_P \bullet I_{PEAK} \bullet 10^4}{B_{max} \bullet Ae} \quad (7)$$

Based upon this result and the predetermined turns ratio, the number of secondary turns is established. With a turns ratio of 5 and N_P equal to 20, N_S is calculated to be 4.

The energy stored in the flyback transformer is actually stored in an air gap in the core.This is because the high permeability of the ferrite material can't store much energy without saturating first. By adding an air gap, the hysteresis curve of the magnetic material is actually tilted, requiring a much higher field strength to saturate the core. The size of the air gap is calculated using (8).

$$gap = \frac{\mu_O \bullet \mu_r \bullet (N_P)^2 \bullet Ae \bullet 10^{-2}}{L_P} \quad (8)$$

In (8), the gap is measured in centimeters, μ_o is the permeability of free space equal to $4\pi \bullet 10^{-7}$ H/m, and μ_r is equal to the relative permeability of the gap material (in this case the gap material is air, μ_r =1). This gap is calculated to be 0.043cm and is evenly distributed between the center post and two outer legs of the EFD30 core.

The primary windings are two strands of 21AWG magnet wire in parallel, the first layer wound closest to the core, the second layer over the secondary windings. The secondary windings consist of four strands of 18AWG magnet wire in parallel, filling a single layer for maximum coupling.

Using a primary inductance of 80µH and a maximum duty cycle of 48% means the converter will not stay in continuous mode control over the entire operating range because of the relationship expressed in (9).

$$P_{O(min)} = \frac{\left(V_{IN(min)} - V_D\right) \bullet V_{IN(min)} \bullet \left(t_{on(max)}\right)^2}{2.5 \bullet T \bullet L_P} \quad (9)$$

According to (9), at the 32V minimum input voltage the converter will enter discontinuous mode at an output load current of less than 3.33A. To remain in CCM would require a much larger transformer, 264.5µH at 48% duty cycle. Increasing the primary inductor value requires a much larger core, such as the E41/17/2 core set from Philips. This would require 60% more circuit board space than the present core.

Another approach to guarantee remaining in continuous mode is to reduce the maximum duty cycle to approximately 26% and continue to use an 80µH flyback inductor.Unfortunately, the result of this would be considerably higher peak currents. Higher peak currents result in an increase of all the I^2R losses, and a larger core would be needed anyway to satisfy the core area product limit which is dependent upon the peak primary current as expressed in (6).

It is far better to design for continuous mode and to transition into discontinuous mode than the other way around. Discontinuous mode is actually unavoidable at zero load. A continuous mode feedback control loop has the ability to maintain stability while in discontinuous mode. However, a control loop designed for discontinuous operation does not take into account the already eluded to right-half-plane zero present in continuous mode. The existing demo board design has the fortuitous advantage of showing the user waveforms for both operating modes dependent upon input voltage and load current (see Figures 16 and 17).

MOSFET Selection

The switching element in a flyback converter must have a voltage rating high enough to handle the maximum input voltage and the reflected secondary voltage, not to mention any leakage inductance induced spike that is inevitably present. Approximate the required voltage rating of the MOSFET using (10).

$$V_{ds} = \left[\left(V_{IN(max)} + V_L\right) + \left(\frac{N_P}{N_S}\right) \bullet \left(V_O + V_D\right)\right] \bullet 1.3 \quad (10)$$

where V_{ds} = the required drain to source voltage rating of the MOSFET,

V_L = the voltage spike due to the leakage inductance of the transformer, estimated to be thirty percent of $V_{IN(max)}$,

and the additional 1.3 factor includes an overall thirty percent margin.

For the flyback converter presented, the required minimum voltage rating of the MOSFET calculates to be 160V. An IRF640 N-channel power MOSFET was chosen. This device has a voltage rating of 200V, a continuous DC current rating of 18A, and an $R_{ds(on)}$ of only 0.18Ω. By consulting the typical gate charge vs. gate-to-source voltage waveform in the manufacturer's data book, calculating the average current required to drive the gate capacitor of the FET is possible:

$$I_{gate} = Q_{max} \bullet f_{sw} \quad (11)$$

Q_{max} is the total gate charge in Coulombs, estimated to be 70nC based upon a gate to source voltage of 15V and a drain to source voltage of 160V. According to (11), the average supply current of the controller, I_{VDD}, needs to increase by 4.9mA to switch the gate at the selected operating frequency.

This FET will experience both switching and conduction losses. The conduction losses will be equal to the I^2R losses, as shown by (12).

$$P_{cond} = (I_{rms})^2 \bullet R_{ds(on)} \quad (12)$$

Switching losses are the result of overlapping drain current and drain to source voltage at turn on and turn off [3]. At turn on the drain current begins to flow through the FET device when the gate voltage has reached the V_{gs} threshold. This drain current will continue to rise until reaching its final value. Meanwhile, the drain to source voltage will remain at V_{ds}, calculated earlier in (10). This voltage starts to fall only after the "Miller" capacitor begins to charge. The charging time, t_{ch}, for the "Miller" capacitor is a function of the gate resistor, R_g (R10 in Figure 1), and the gate to drain "Miller" charge, Q_{gd}, as shown in (13).

$$t_{ch} = \frac{Q_{gd} \bullet R_g}{VDD - V_{gs(th)}} \quad (13)$$

In (13), VDD is the bias voltage of the UCC3809 and $V_{gs(th)}$ is the gate threshold voltage of the FET. The whole process repeats itself in reverse at turn off. The power dissipation of the FET's output capacitance, C_{oss}, also contributes to the switching losses in the form of $\frac{1}{2}CV^2f$. The total switching losses are estimated based on equation (14).

$$P_{SW} = \frac{C_{oss} \bullet (V_{ds})^2 \bullet f_{sw}}{2} + V_{ds} \bullet I_{PEAK} \bullet t_{ch} \bullet f_{sw} \quad (14)$$

The total FET losses are the sum of the conduction losses (12) and the switching losses (14), calculated to be 3.3W for the IRF640 FET used on the demo board. Without appropriate heatsinking, this device would have a junction to ambient thermal resistance of 62°C/W, resulting in a junction temperature rise of 206°C above ambient. Heat sinking is obviously required to prevent the junction temperature, T_j, from exceeding 150°C and avert device failure due to excessive heating. The IRF640 has a junction to case thermal resistance, θ_{jc}, of 1°C/W, using a silicone elastomer heat sink pad provides a case to heat sink thermal resistance, θ_{cs}, of 1.26°C/W. A heat sink which provides a maximum thermal resistance, θ_{sa}, of 35°C/W must be chosen for a use in an ambient temperature, T_a, of 25°C, as shown in (15a) and (15b).

$$T_j = (P_{cond} + P_{sw}) \bullet \left(\Theta_{jc} + \Theta_{cs} + \Theta_{sa}\right) + T_a \quad (15a)$$

$$\Theta_{sa} = \frac{T_j - T_a}{P_{cond} + P_{sw}} - \left(\Theta_{jc} + \Theta_{cs}\right) \quad (15b)$$

Diode Selection

Schottky rectifiers have a lower forward voltage drop than typical PN devices, making it the rectifier of choice when considering reducing converter losses and improving overall efficiency. Selecting the appropriate Schottky for a specific application depends mainly on the working peak reverse voltage rating, the peak repetitive forward current, and

the average forward current rating of the device. If the maximum working peak reverse voltage is exceeded the reverse leakage current will rise above its specified limit. The peak reverse voltage that the device will be subjected to is equal to the reflected maximum input voltage minus the voltage drop across the FET added to the output voltage. The maximum average forward current rating of the device must not be exceeded if the junction temperature of the device is to remain within its safe operating range. Because all current to the output capacitor and load must flow through the diode, the average forward diode current is equal to the steady-state load current. The peak repetitive forward current is equal to the reflected primary peak current. An MBR2535CTL Schottky rectifier from Motorola met the requirements for the demo board design. This device is a common cathode dual Schottky with a forward voltage drop of 0.47V and a working peak reverse voltage rating of 35V, exceeding the 20V requirement of the demo board design. The average rectified forward current rating is specified at 12.5A per leg, 25A total, and the peak repetitive forward current is rated for 25A per leg, or a total of 50A. The demo board requirement is 10A total average forward current and 26A total peak repetitive forward current.

Power loss in the Schotty is the summation of conduction losses and the reverse leakage losses. Conduction losses are calculated using the forward voltage drop and the average forward current. The MBR2535CTL will have conduction losses equal to 4.7W. Reverse leakage losses, which are dependent upon the reverse leakage current, the blocking voltage, and the on-time of the FET, are calculated to be 0.05W. Heat sink selection is once again based upon the required thermal resistance of the heat sink to air interface in order to maintain a junction temperture of less than 125°C.

Input and Output Capacitors

The input capacitors are chosen based upon their ripple current rating and their rated voltage. The input current waveform is shown in Figure 3. The shaded regions represent the current actually supplied by the input capacitors during the switch's on- and off-times. The RMS value of this ripple current is calculated by adding the RMS current of the ramp on a step shaded waveform during t_{ON} with the RMS value of the average input current during t_{OFF}. Because this example uses a duty cycle that is very close to 50%, this RMS current is almost equal to the primary RMS current calculated in (5).The actual capacitor value is not that critical as long as the minimum capacitance gives an acceptable ripple voltage determined by the following equation:

$$C_{min} = \frac{I_{rms}}{8 \bullet f_{sw} \bullet \Delta V} \qquad (16)$$

In (16), I_{rms} is equal to the RMS current, calculated from Figure 3, and ΔV is equal to the acceptable ripple voltage. Two United Chemi-Con SXE series 150µF capacitors in parallel met the requirements for the demo board design when derated for ambient temperature and frequency. The small 1µF ceramic capacitor is added at the converter input to provide a shorter path for high frequency ripple.

The output capacitors are also chosen based upon their low equivalent series resistance (ESR), ripple current and voltage ratings, and (16). The ripple current that the output capacitor experiences is a result of supplying the load current during the FET conduction time and its charging current during the FET off-time, as illustrated by the shaded regions in Figure 4. During the conduction time of the FET, the secondary windings of the transformer are not conducting. The discharging of the output capacitor supplies the 10A load current. During the FET

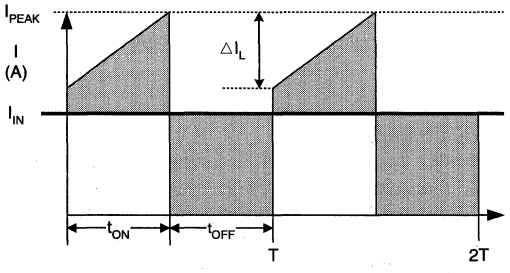


Figure 3. Input capacitor current waveform.

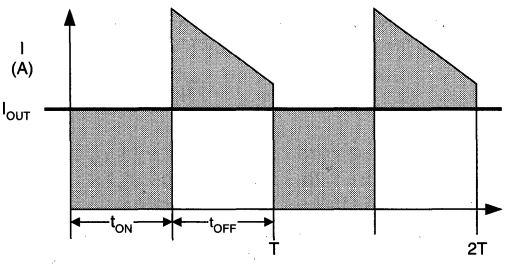


Figure 4. Output capacitor current waveform.

off-time, the secondary windings are conducting and the secondary peak current is charging the output capacitor and delivering the 10A current to the load. The RMS current is calculated to be approximately 14A. Four Sanyo OSCON 6SH330M 330µF capacitors in parallel met the requirements for the demo board design when derated for ambient temperature and frequency.

SETTING UP THE UCC3809

The UCC3809 was selected as the primary side controller for this application because of its flexibility, low cost, and built in features such as programmable maximum duty cycle, full cycle programmable soft start, undervoltage lockout, and low operating current.

VDD Bias/UVLO

The employment of a constant current biasing scheme, as shown in Figure 5, minimizes transformer design costs by eliminating the need for a bootstrap winding. It also avoids any high power dissipation that would be present in a single bias resistor. This is especially true with a wide input voltage range, such as seen in the telecommunications industry. The current biasing scheme supplies enough current for the gate drive, determined by (11), in addition to the maximum I_{VDD} current required to operate the internal functions of the IC.

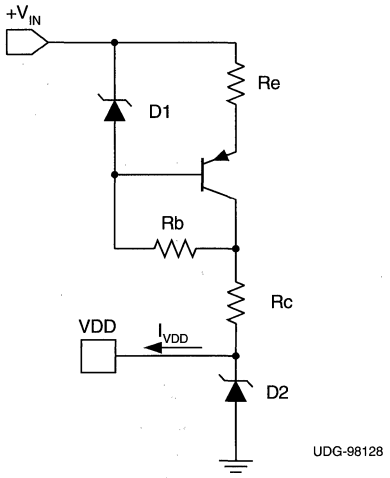


Figure 5. Constant current biasing.

The zener diode, D1, minus the V_{BE} drop of the small signal PNP transistor, sets up a constant voltage across the emitter resistor, Re, resulting in a constant emitter current. The selection of the collector resistor, Rc, ensures the transistor remains in the active mode throughout the entire range of V_{IN} while maintaining VDD above the under voltage lockout level. All of these components have minimal power dissipation and are surface-mountable if desired. Although the internal shunt regulator can sink up to 25mA, D2 was added to minimize the power dissipation in the IC.

The UCC3809 is available with two different undervoltage lockout (UVLO) levels and hysteresis options. Off-line users can take advantage of the wider hysteresis option available in the –2 device while the tighter hysteresis of the –1 is optimized for dc-to-dc converter use. UVLO insures that the IC bias is within specification before enabling the output stage. This guarantees the output drive is capable to fully turn on the MOSFET once the UVLO threshold has been reached. The output drive and reference voltage are actively held low during power-up and the I_{VDD} starting current is less than 100µA until VDD crosses the turn-on threshold. As VDD crosses the turn-off threshold during power-down, REF and the output drive are pulled low.

Decoupling

Both VDD and REF should be decoupled with good quality, low ESR/ESL, ceramic capacitors placed as close to the VDD or REF pin as possible and returned directly to the GND pin for the best high frequency performance. Because the reference voltage provides the bias to many of the internal circuits of the IC, its decoupling capacitor should be at least 0.47µF for adequate filtering.

Soft Start and Shutdown

The soft start feature enables the IC to start up in a controlled manner. While the IC is in UVLO, the SS pin is held low. Once the UVLO threshold has been crossed, an internal 6µA current source charges the external soft start capacitor (C4, Figure 1). As the capacitor voltage ramps up from 1V to 2V, the output duty cycle linearly increases to a level required for output voltage regulation. The soft start capacitor is chosen so that there is a delay of approximately 3 milliseconds before VOUT ramps up to its full potential. Pulling the SS pin below 0.5V will shut down the output and pull REF low. This feature is easily implemented using a small signal NPN and a pull-down resistor to accept a logic level command signal.

Output Driver

The totem pole output stage of the UCC3809 has the ability to source 0.4A and sink 0.8A. Placing a small resistor (R10, Fig. 1) in series with the IC output and the gate of the FET will damp any oscillations caused by the parasitic wiring inductance and the FET's input capacitance. To insure the MOSFET gate does not get charged to its turn-on threshold during device start up, a pull-down resistor (R7, Fig. 1) is added to the gate drive. The output stage provides a low resistance during overshoot and undershoot, eliminating the need for Schottky diodes on the output.

Oscillator

The data sheet gives a complete description of the operation of the internal oscillator and optional synchronization schemes. The external RT1 resistor (R3, Fig. 1) and the internally generated voltage across it control the charge current of CT (C5, Figure 1). When the CT voltage is equal to 2/3 of the reference voltage, sensed through RT2 (R4, Figure 1), the oscillator initiates a discharge cycle. The discharge current is set by RT2 and the CT voltage is sensed through RT1. When CT has discharged to 1/3 of the reference voltage, the charging cycle begins again.

The demo board requires 48%, or 6.9µs, of unrestrained on-time during its full range of operation. The duty cycle clamp is set at 66%, or 9.5µs, so that within the range of normal operation, the output regulation is not sacrificed because of hitting the duty cycle clamp. This clamp will effectively prevent the transformer from saturating when the input voltage is less than the minimum operating range, such as during start-up, brown-outs, and shut down, without inhibiting normal operation. For 100kHz switching frequency, the recommended capacitor for CT is approximately 1nF, and the internal capacitance of the IC is estimated to be 27pF. Setting t_{on} of the duty cycle clamp to 9.5µs, and CT equal to 1nF, RT1 is determined by:

$$RT1 = \frac{t_{on}}{0.74 \bullet (CT + 27pF)} \quad (17)$$

RT2 is then selected to satisfy the switching frequency period. The oscillator frequency is approximated by the following equation:

$$f_{sw} = \frac{1}{0.74 \bullet (CT + 27pF) \bullet (RT1 + RT2)} \quad (18)$$

For good noise immunity, the timing components must be placed as close as possible to the IC pins. The CT-RT1-RT2 junction (TP2 on the demo board) should be used to look at the oscillator waveform instead of putting a probe directly onto pins 3 and 4 of the IC. The probe will add stray capacitance to the oscillator and alter the switching frequency if placed directly on the IC pins.

Current Limiting

Selection of the current sense resistor is accomplished by dividing the FB 1V threshold value by the peak primary current at the desired current limit point, typically 120% of I_{PEAK}.

$$R_{sense} = \frac{FB_{threshold}}{1.2 \bullet I_{PEAK}} \quad (19)$$

This ground-referenced resistor must be a low inductance type and have a rated power level to meet the $(I_{RMS})^2 \bullet R_{sense}$ requirement. The closest standard value resistor that meets this requirement is used. The UCC3809/UC3965 demo board uses a 0.15Ω resistor for current sensing. This value resistor equates to a maximum primary side current limit point of 6.67A. This would lead to a worst case short circuit output current, I_{sc}, of 12.9A as calculated using (4), substituting I_{sc} for $I_{OUT(max)}$. Upon crossing the PWM comparator threshold, the internal PWM latch is reset, turning off the output driver until the beginning of the next oscillator charge cycle.

Current spikes caused by the leakage inductance of the flyback transformer and the reverse recovery of the diode could trip the current sense latch and prematurely shut off the output. This unwanted spike can be suppressed by adding a small RC filter for effective leading edge blanking (Figure 6). Usually adding a few hundred nanoseconds of blanking time is enough to ignore (or "blank") any unwanted current spikes. An internal 250Ω NMOS FET discharges the high frequency capacitor used in this filter during the PWM off-time.

Slope Compensation [4]

Sensing peak inductor current instead of average inductor current results in a loop response that is less than ideal. Adding slope compensation to the current sense signal cancels this error by maintaining a constant average current independent of duty cycle. Slope compensation is required for open loop stability in a current mode system with 50% or greater duty cycles, but will benefit any current mode application at the cost of a few small parts.

The UCC3809 demo board resistively divides the oscillator sawtooth at the CT node and superimposes it onto the current sense signal using an emitter follower configuration as detailed in [4].

The first step in implementing slope compensation is to calculate the flyback inductor down slope on the secondary side in amps per second:

$$S(L) = \frac{di}{dt} = \frac{V_{sec}}{L_{sec}} \quad (20)$$

where $V_{sec} = V_O + V_D$ and $L_{sec} = L_P/N^2$. Then transform this slope to the primary side and calculate the equivalent slope voltage at the sense resistor in volts per second:

$$VS(L)' = \frac{S(L)}{N} R_{sense} \quad (21)$$

Next, calculate the oscillator slope at the timing capacitor, CT, in volts per second:

$$VS(osc) = \frac{\Delta V_{osc}}{t_{on(max)}} \quad (22)$$

ΔV_{osc} is equal to the CT peak to peak voltage, 1.67V for the UCC3809. Because the oscillator waveform has a valley voltage greater than zero, an AC coupling capacitor is required (Fig. 6). Using superpositioning and neglecting the coupling and LEB capacitors, the voltage ramp equation at the FB pin can be derived (23).

$$V(ramp) = \frac{VS(L)' \bullet R_{SC}}{R_{LEB} + R_{SC}} + \frac{VS(osc) \bullet R_{LEB}}{R_{LEB} + R_{SC}} \quad (23)$$

The value of the R_{SC} resistor (Figure 6) is dependent upon the amount of slope compensation to be added. By equating a portion (M) of the inductor downslope to the resistively divided oscillator charge slope, R_{SC} can be determined.

$$\frac{VS(osc) \bullet R_{LEB}}{R_{LEB} + R_{SC}} = M \bullet \left(\frac{VS(L)' \bullet R_{SC}}{R_{LEB} + R_{SC}} \right) \quad (24)$$

$$R_{SC} = \frac{R_{LEB} \bullet VS(osc)}{VS(L)' \bullet M} \ \Omega \quad (25)$$

To guarantee current loop stability at 100% duty cycle, a minimum compensation of ½ the inductor down slope (M = 0.5) must be added. By adding slope compensation equal to the down slope of the inductor current (M = 1), any current perturbation will be eliminated in one cycle. The demo board incorporates approximately 80% slope compensation by using 5.62KΩ and 1KΩ resistors for R_{SC} and R_{LEB}, respectively.

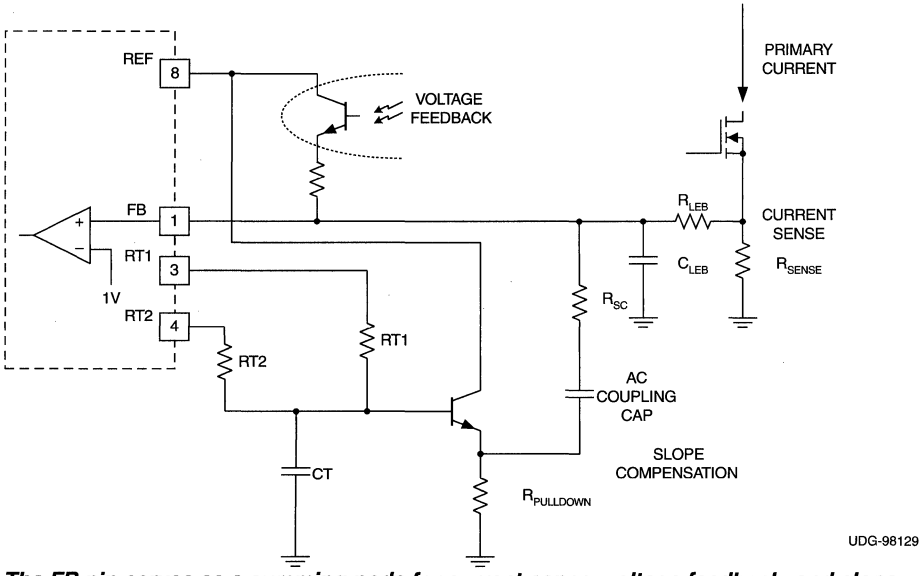


Figure 6. The FB pin serves as a summing node for current sense, voltage feedback, and slope compensation.

Voltage Feedback

The FB pin of the UCC3809 sums the voltage feedback signal to the current sense signal and any added slope compensation. The voltage feedback signal is from an optocoupler, which is driven from an error amplifier on the secondary side of the converter.The signal from the optocoupler is designed to trip the 1V threshold of the UCC3809 internal comparator when the output voltage exceeds its specified limit.

SETTING UP THE SECONDARY SIDE ERROR AMPLIFIER, UC3965

Because the flyback converter in this design is input-output isolated, the error amplifier needed to sense the output voltage is on the secondary side. The designers of the UCC3809 considered this when designing the circuit and omitted the error amplifier from this IC. Utilizing the UC3965 Precision Reference and Low Offset Error Amplifier satisfies the requirement for a secondary side error amplifier and has an on-board precision reference needed for accurate regulation.

Biasing, UVLO, and Decoupling

Because the UVLO threshold of the UC3965 is 4.1V, the secondary side IC can be biased from the 5V output bus. To prevent the ripple voltage from tripping the under voltage lockout, a 47µF decoupling capacitor is used. A Schottky diode in series with the input pin is required to prevent the decoupling capacitors from discharging with the output capacitors during the FET on-time.

Output Voltage Sensing

The precision reference of the UC3965 is tied to the non-inverting input of the device's internal error amplifier. The output voltage of the converter is resistively divided and compared to this reference at the inverting input. This error amplifier has a low 1mV input offset voltage that insures accurate regulation of V_O. The error amplifier drives the inverting input of an internal buffer whose output is then used to drive an optocoupler diode. As the output voltage increases beyond its desired value, the voltage difference at the error amplifier increases. This results in less drive at the inverting input of the internal buffer, increasing its output drive to the optocoupler. If the application does not require input-output isolation, this buffer could be used to drive the PWM directly.

Loop Compensation [5] [6]

As previously alluded to, a continuous current mode flyback will contain a right-half-plane (RHP) zero in its transfer function. What exactly does this mean? Basically, any increase in load current will require the primary peak inductor current to increase. The duty cycle must increase to accomplish this. In a flyback converter, the inductor current flows to the output only when the FET is off and the diode is conducting. Increasing the duty cycle increases the FET conduction time but decreases the diode conduction time. Ironically, the result of this is the average diode current, the current that supplies the load, actually decreases. This is a temporary situation; as the inductor current rises, the diode current eventually reaches its proper value. The condition where the average diode current must actually decrease before it can increase is referred to as a right-half-plane zero. To complicate matters, this zero contributes a phase lag, not a phase lead as a normal zero would. This zero moves in frequency as a function of load and input voltage, as shown in (26), making it impossible to cancel out by the insertion of a pole.

$$f_{RHPZERO} = \frac{N \bullet V_{IN}^{\,2}}{2 \bullet \pi \bullet R_{OUT} \bullet L_P \bullet (V_{IN} + N \bullet V_{OUT})} \qquad (26)$$

The easiest way to deal with a right-half-plane zero is to roll off the loop gain at a relatively low frequency using simple dominant pole compensation. Unfortunately, the result of this is poor dynamic response.

The primary goal of the compensation network is to provide good line and load regulation and dynamic response. These objectives are best met by providing high gain at low frequencies for good DC regulation and high bandwidth for good transient response. Optimum closed loop performance can only be achieved by first knowing what the transfer characteristic of the PWM and switching circuit looks like. Constructing a Bode plot of the known poles and zeroes in the power stage does this. Bode plots give a visual interpretation of the gain versus frequency and phase versus frequency characteristics of a system. In the gain plot, the gain shown at each frequency represents the amount by which the feedback loop will reduce a disturbance at that frequency.

Besides the RHP zero, the output capacitor and the load contribute a pole at a frequency determined by (27), and the output capacitor alone will contribute a zero based upon its ESR and capacitance as shown in (28).

$$f_{pole} = \frac{1+D}{2 \bullet \pi \bullet R_{OUT} \bullet C_{OUT}} \quad (27)$$

$$f_{zero} = \frac{1}{2\pi \bullet ESR \bullet C_{OUT}} \quad (28)$$

The control to output gain [7] is calculated using (29):

$$GAIN = 20 \bullet \log \bullet \left[\frac{I_{sc} \bullet R_{OUT} \bullet V_{IN}}{V_C \bullet (1-D) \bullet (2 \bullet N \bullet V_O + V_{IN})} \right] \quad (29)$$

In this equation, the output short circuit current, I_{sc}, was calculated previously. V_c is the control voltage, equal to 2.5V in the UC3965. In addition to the control to output gain, the optocoupler will also contribute a gain based upon its current transfer ratio and a phase lag due to its large collector to base capacitance. Because the optocoupler data sheet usually does not include any frequency dependent curves, the bandwidth was measured in the lab using a network analyzer. The gain contribution from the optocoupler averaged 7dB and the expected pole was not evident in scans run up to 60kHz. The closed loop gain of the inner current loop is equal to the inverse of the sense resistor, $1/R_{sense}$, or 16dB. By adding all of these factors together, a Bode plot of the uncompensated system can be realized.

Once the frequency response of the uncompensated system is determined, the next step is to determine what compensation is needed around the error amplifier for optimum performance. As stated earlier, optimum performance requires a high gain at low frequencies for good DC regulation and high bandwidth for good transient response. The crossover frequency, f_c, is the frequency at which the gain magnitude equals 0dB. High bandwidth is achieved by having the highest possible f_c. Because of the RHP zero, the highest possible crossover frequency is limited to $f_{RHPZERO}/\pi$.The phase margin, or the amount the phase lag measures at f_c less 180°, should be at least 45° for good transient response with little overshoot.The magnitude of the gain at the frequency where the phase plot measures –180° is referred to as the gain margin. If the slope of the gain plot is –2, or –40dB/decade, at low frequencies, it must transition to a –20dB/decade slope, also known as a –1 slope, one decade before crossing the 0dB point.If the slope remains at the –2 slope the resultant gain margin would be too small causing severe underdamped oscillations at f_c.

With all these tricks of the trade in mind, the compensation network is designed around the error amplifier.A certain amount of juggling is inevitable but, in general, the scheme shown in Figure 7 will handle most compensation requirements. There is a pole at the origin which contributes a –1 slope in the gain plot, a low frequency zero, f_{EAZERO} (30), flattens out the slope so the midrange gain is equal to R_f/R_i. A high frequency pole, f_{EAPOLE} (31), helps suppress any high frequency noise from propagating through the system. R_d forms a voltage divider with R_i and provides a DC offset.

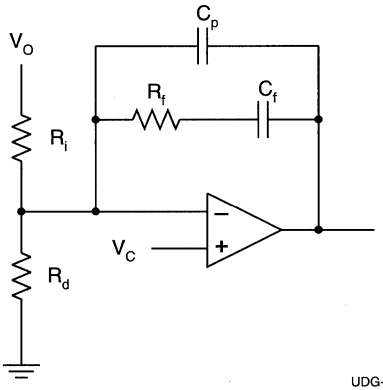


Figure 7. Error amplifier compensation network.

By combining the Bode plots of the PWM and power stage with the error amplifier compensation, a plot of the entire system is realized.

$$f_{EAZERO} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_f} \quad (30)$$

$$f_{EAPOLE} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p} \quad (31)$$

The following graphs show examples of Bode plots before and after compensation.

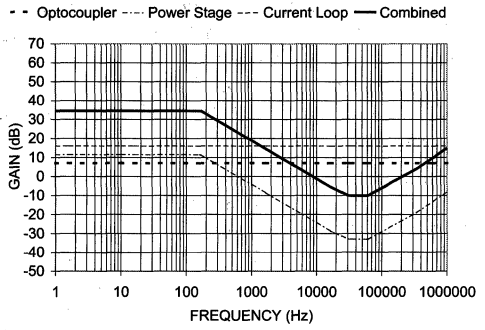


Figure 8. Gain Bode plot without compensation.

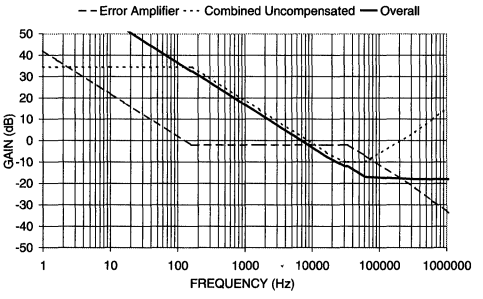


Figure 9. Gain Bode plot with compensation.

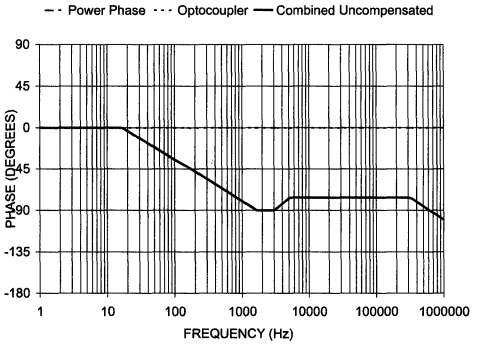


Figure 10. Phase Bode plot without compensation.

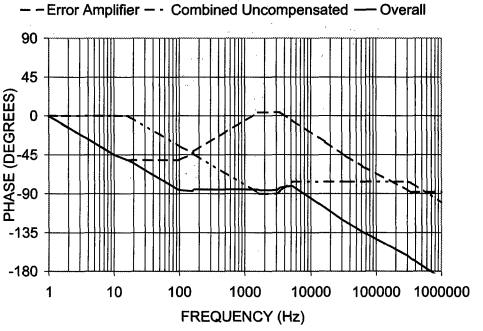


Figure 11. Phase bode plot with compensation.

SNUBBERS AND CLAMPS [7]

Transformer leakage inductance imposes high transients in the switch, requiring a switching device with an excessive voltage rating. The primary side of the demo board utilizes a passive polarized voltage clamp (Figure 12) to suppress the voltage overshoot during the turn-off transition of the FET. This circuit limits the peak switch voltage, reducing the power dissipation in the switching device. The total dissipated energy remains the same, but it is now divided between the clamp resistor and the FET.

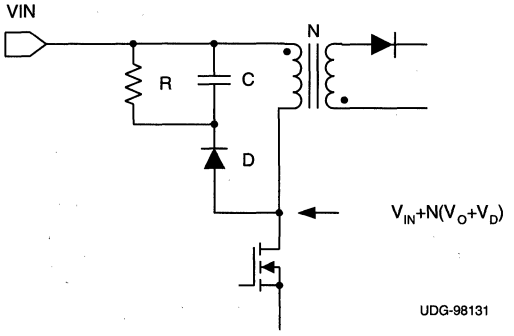


Figure 12. RCD clamp on the primary side suppresses voltage overshoot across the FET.

The parasitic inductance of the transformer is discharged into the capacitor during each switching cycle. The value of the capacitor is selected based upon the amount of energy that this leakage inductance stores plus the initial energy stored in the capacitor from the input voltage and the reflected output voltage. Equation 32 determines the minimum capacitor value.

$$C = \frac{L_L \bullet (I_{PEAK})^2}{\Delta V_c \bullet (\Delta V_c + 2V)} \quad (32)$$

In the above equation, ΔV_C is equal to the acceptable change of voltage across the capacitor, usually between 40 and 60V. L_L is equal to the leakage inductance of the transformer. I_{PEAK} is equal to the peak current in the inductor at the time of turn-off. V is equal to the DC bias across the capacitor. This DC bias is a result of the DC path through the resistor and diode and the secondary side voltage reflected to the primary:

$$V = N \bullet (V_O + V_D) \quad (33)$$

The resistor is selected such that the RC time constant is much longer than the switching period. This resistor must not only dissipate the energy stored in the leakage inductance, but also the voltage due to the DC bias of the capacitor:

$$P_R = \frac{L_L \bullet (I_{PEAK})^2 \bullet f_{sw}}{2} + \frac{V^2}{R} \quad (34)$$

The resistor used on the demo board must dissipate 2.4W of power. The diode is selected based upon the charging current of the capacitor.

The secondary side of the converter requires an RC snubber across the diode (Figure 13) to damp the high frequency ringing on the 5V bus due to the parasitic inductance of the transformer and parasitic capacitance of the Schottky.

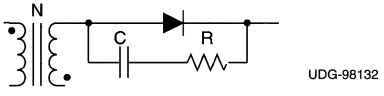


Figure 13. RC snubber on the secondary side dampens parasitic oscillations.

The capacitor is chosen such that, when placed across the Schottky, the oscillating frequency, f_{osc}, is reduced by approximately half. The leakage inductance, L_{SL} and parasitic capacitance, C_p can be determined by simultaneously solving (35a) and (35b).

$$f_{osc} = \frac{1}{2 \bullet \pi \bullet \sqrt{L_{SL} \bullet C_p}} \quad (35a)$$

$$\frac{f_{osc}}{2} = \frac{1}{2 \bullet \pi \bullet \sqrt{L_{SL} \bullet (C_p + C)}} \quad (35b)$$

In (35b), C is the capacitor that was added to reduce the oscillation frequency. The appropriate value of the resistor is selected to provide critical damping to the oscillation:

$$R = \sqrt{\frac{L_L}{(C_p + C)}} \quad (36)$$

Because the time constant of this RC snubber is much less than the switching period but much longer than the voltage rise time, the power dissipated by the resistor is dependent upon the energy stored in the capacitor. Since the capacitor charges and discharges each cycle, the power the resistor must dissipate is equal to:

$$P_R = C \bullet V^2 \bullet f_{sw} \quad (37)$$

In (37), C is the RC snubber capacitor value. V is equal to the drain to source voltage reflected to the secondary side added to the output voltage plus the voltage drop across the diode. This snubber circuit will prevent the anode of the diode from ringing below the reverse voltage rating of the Schottky device.

LC FILTER

The voltage ripple on the output will occur at the switching frequency and is required to be less than 50mV peak to peak. To meet the output noise specification, an LC filter was added to the converter output. The unfiltered ripple, V_R, will be equal to the peak secondary current multiplied by the ESR of the output capacitor bank. The amount of attenuation needed to filter the ripple, V_R, to an acceptable level is determined by (38)

$$ATTEN_{db} = -20 \bullet \log \bullet \left(\frac{V_R}{0.05} \right) \quad (38)$$

An LC filter will produce a gain plot with a –40dB/decade slope. The selected LC filter should have a pole that results in a minimum gain derived from (38) at the switching frequency. The pole frequency will occur at:

$$f_{pole} = \frac{1}{2 \bullet \pi \bullet \sqrt{LC}} \quad (39)$$

The demo board employs a 2µH iron powder toroid and a 33µF electrolytic capacitor for a pole frequency of 20kHz and a minimum gain of –8dB.

EXPERIMENTAL RESULTS

The oscilloscope traces refer to the test points (TP) indicated and are referenced to the appropriate ground, either primary or secondary.

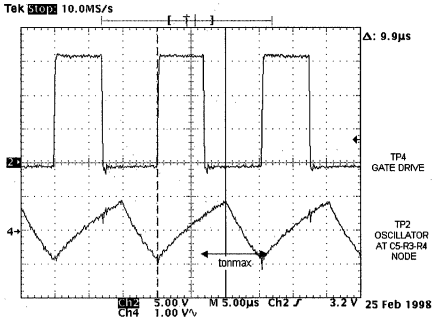


Figure 14. The UCC3809 gate drive and oscillator.

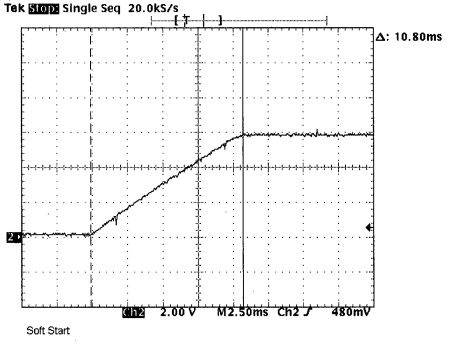


Figure 15. Soft start capacitor charging waveform.

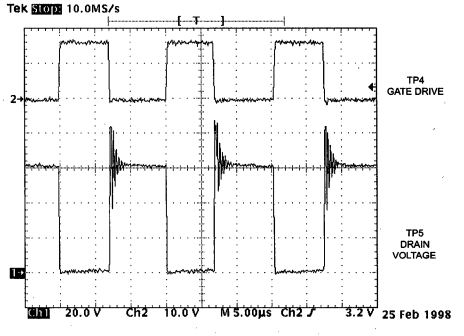


Figure 16. Gate and drain in continuous conduction mode.

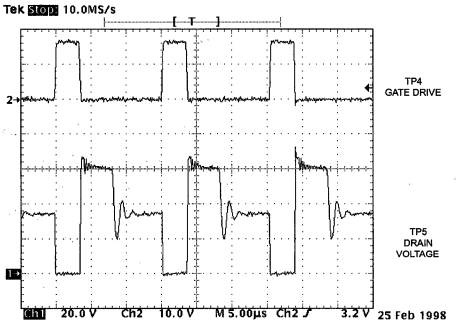


Figure 17. Gate and drain in discontinuous conduction mode.

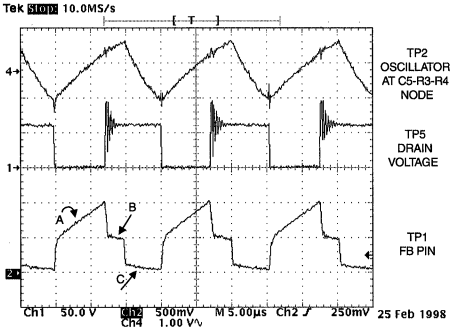


Figure 18. The FB pin in continuous conduction mode.

In Figure 18, the FB pin is shown in the bottom trace. Region A is the summation of the current sense and voltage feedback , at 1V the gate is turned off, resulting in the drain establishing a voltage with respect to the source. Region B results from the FB pin still sensing the voltage feedback during the remaining oscillator charge time. Region C is where the internal 250Ω on resistance FET is turned on during the PWM off time, discharging all external capacitance at that node.

Efficiency measurements performed yielded the following results.

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	n
31.763	1.830	58.126	5.019	9.211	46.225	0.795
31.954	1.809	57.805	5.014	9.178	46.022	0.796
48.014	1.178	56.560	5.017	9.202	46.168	0.816
48.073	1.172	56.342	5.015	9.185	46.060	0.818
72.038	0.780	56.190	5.015	9.187	46.071	0.820

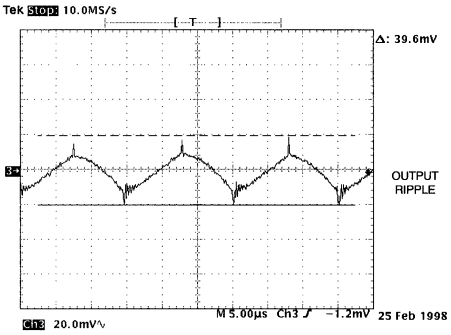


Figure 19. Output voltage ripple waveform.

ALTERNATE OUTPUT VOLTAGES

A user may require an output voltage different from the 5V discussed thus far. By working through this design review and substituting the required output voltage level, new peak currents and maximum duty cycles can be determined. These changes will be reflected in the selection of appropriate components such as the MOSFET, sense resistor, diode, and output capacitors. The transformer would be redesigned for the optimum turns ratio, wire sizes, and core requirements for the given design.

Table 1. Demonstration board parts list.

Reference Designator	Description	Manufacturer	Part Number
C1, C2	150mF, 80V, Aluminum Capacitor	United Chemi-Con	SXE80VB151M12X20LL
C3	1µF, 100V, Ceramic Capacitor	KEMET	C340C105K1R5CA
C4, C22	0.01µF, 50V, Ceramic Capacitor		
C5	1nF, 50V, Ceramic Capacitor		
C6	330pF, 50V, Ceramic Capacitor		
C7	0.47µF, 50V, Ceramic Capacitor		
C8	1µF, 50V, Ceramic Capacitor		
C9, C12	0.1µF, 50V, Ceramic Capacitor		
C10	0.22µF, 100V, Ceramic Capacitor	KEMET	C330C224K1R5CA
C11	1µF, 35V, Tantalum Capacitor		
C14	0.22µF, 50V, Ceramic Capacitor		
C15	0.015µF, 50V, Ceramic Capacitor		
C16, C17, C18, C19	330µF, 6.3V, Aluminum Capacitors	SANYO	OSCON 6SH330M
C20	33µF, 10V, Tantalum Capacitor		
C21	47µF, 25V, Aluminum Electrolytic	Panasonic	ECE-A1AFS470
C23	6800pF, 50V, Ceramic Capacitor		
D1	ZENER, 5.1V		1N5231
D2	ZENER, 15V		1N5245
D3	2A, 200V, Ultra Fast		SF24
D4	ZENER, 10V		1N5240
D5	1A Schottky		1N5819
L1	2.5µH, 11A	Coiltronics, Inc.	CTX08-14017
Q1, Q4	small signal NPN		MPS2222A
Q2	small signal PNP		MPS2907A
Q3	200V, 18A, N-Channel MOSFET	Motorola or IR	IRF640

Reference Designator	Description	Manufacturer	Part Number
R1	5.1K, ¼W, 5%		
R2, R13	1.1K, ¼W, 5%		
R3	12.1K, ¼W, 5%		
R4	6.19K, ¼W, 5%		
R5	470, ¼W, 5%		
R6	1.0K, ¼W, 5%		
R7	15K, ¼W, 5%		
R8	0.15, 3W, 5%	RCD	RSF2B0.15 ohm 5%
R9	2K, 3W, 5%	RCD	RSF2B2K ohm 5%
R10	10, ¼W, 5%		
R11	680, ¼W, 5%		
R12	27K, ¼W, 5%		
R14	750, ¼W, 5%		
R16, R17	12.1K, ¼W, 1%		
R18	3.01K, ¼W, 5%		
R19	5.1, 3W, 5%	RCD	RSF2B5.1 ohm 5%
R20	5.62K, ¼W, 5%		
R21	475, ¼W, 1%		
T1	80µH, N = 5	Coiltronics, Inc.	CTX08-13916
U1	PWM Controller	Unitrode	UCC3809
U2	25A, 35V Power Schottky Rectifier	Motorola	MBR2535CTL
U3	Optocoupler	Motorola	H11AV1
U4	Error Amplifier, Reference	Unitrode	UC3965
Heatsink	For TO-220	AAVID	529802 B 0 25 00

SUMMARY

The UCC3809/UC3965 demo board is an example of a 50 Watt continuous current mode flyback converter that includes features such as a duty cycle clamp, slope compensation, input to output isolation, and primary and secondary snubbers, just to name a few. A detailed step by step approach is given for power stage component selection, transformer design, loop compensation, and component power dissipation calculations. The features of the UCC3809 and the UC3965 offer design flexibility for a wide range of applications in simple to use 8-pin packages.

REFERENCES

[1] Abraham I. Pressman, *Switching Power Supply Design,* McGraw-Hill, Inc., 1991.

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[3] Bill Andreycak, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits,* Unitrode Application Note U-137, Unitrode Applications Handbook IC# 1051, 1997.

[4] Bill Andreycak, *Practical Considerations in Current Mode Power Supplies,* Unitrode Application Note U-111, Unitrode Applications Handbook IC# 1051, 1997.

[5] Lloyd H. Dixon, Jr., *Control Loop Cookbook,* Unitrode Power Supply Design Seminar Manual SEM-1100, 1996.

[6] Lloyd H. Dixon, Jr., *Closing the Feedback Loop,* Unitrode Power Supply Design Seminar Manual SEM-700, 1990.

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UC3578 TELECOM BUCK CONVERTER EVALUATION BOARD

By Mark Dennis
Unitrode Corporation

ABSTRACT

This application note describes a simple solution for a buck converter operating from an input of 15V to 72V with an N channel MOSFET switching transistor. Using this switch configuration requires a gate potential higher than the input source, generally requiring an auxiliary supply or a transformer. The UC3578 provides a regulated floating gate drive voltage for an N channel MOSFET that allows for cost-effective design of buck stepdown regulators with power levels in the tens of watts. A complete converter with schematic, bill of materials, and performance results is presented to produce a 5V, 35W output from a 48V source.

INTRODUCTION

Distributed power systems have come into widespread use in communications and related industries over the last decade. In these systems the electrical power distribution network has been changed from one central power supply with cables or busses to a number of smaller power processing units which are placed throughout the host system. The usual intent is to bring the power processing closer to the subsystems where the power will be used. The advantages of distributed power are delineated in [1], along with much information on distributed power architectures and applications.

The telecommunications industry has utilized –48V batteries as a power source for many years, and has selected 48Vdc as their bus voltage of choice. [1] Manufacturers have responded with 48Vdc input DC to DC converter modules with outputs from

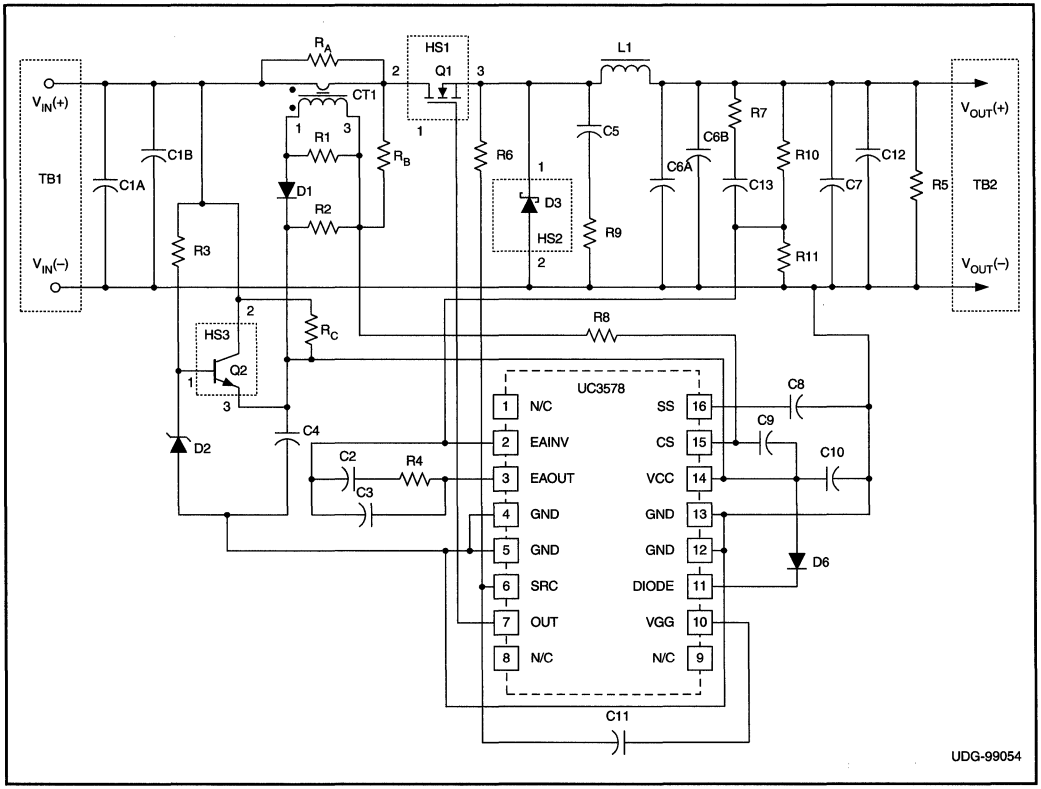

Figure 1. UC3578 evaluation board schematic.

under 1 watt to hundreds of watts, both isolated and non-isolated, with a wide range of features.

INTRODUCTION (cont.)

However, the cost of the modules has historically been relatively high compared to design solutions using discrete components. This Application Note will introduce the UC3578 integrated circuit and highlight its use in a 48V to 5V buck regulator. Utilizing this approach will result in a 35W converter that is a fraction of the cost of a comparable module.

This new IC is used to simplify the design of the single switch PWM buck converter by incorporating a floating high side driver that allows the use of an external N-channel MOSFET switch. A bipolar process is utilized which allows operation from the prevalent bus voltage of 48Vdc, with allowable inputs up to 72Vdc. Higher output current is possible because there is no preset internal switch current limit as used in control chips that incorporate an onboard switch. These options allow the user to configure a low cost high power buck regulator suitable for many applications.

UC3578 DEMONSTRATION CIRCUIT

Specifications. An evaluation board featuring the UC3578 has been developed to demonstrate the capabilities of this new controller. The demo board is targeted at the telecom converter market and has the following specifications:

- V_{IN} = 48V nominal
- 38.4V < V_{IN} < 57.6V
- V_{OUT} = 5V, ±2%
- Output ripple, <50mV at 100 kHz
- I_{OUT} = 7A
- P_{OUT} = 35W

SCHEMATIC

A schematic diagram for the telecom buck converter built to these specifications is shown in Fig. 1. The components Q1, D3, L1, and C6 perform the power handling tasks. C1 serves as a filter to handle the input ripple current. The UC3578 provides the control circuitry for orderly startup, switch protection, regulation, and high-side power MOSFET drive. These functions are discussed in detail in the following sections, along with selection of power components. Alternate components R_A, R_B, and R_C shown on the schematic are used to evaluate circuit options as described in the section *Resistive Current Sense Applications*. For further information on the device and specifications, consult the datasheet or contact a field applications engineer for assistance.

CIRCUIT DESCRIPTION

UC3578 Housekeeping and Control Circuits. Undervoltage lockout (UVLO) is employed to disable IC operation until V_{CC} reaches 11V, and exhibits a 2V hysteresis. After the UVLO threshold is exceeded a soft start cycle is initiated with 45µA charging current supplied to the capacitor on pin 16. When the soft start pin reaches approximately 1.2V the narrow soft start pulses begin to appear on the output, increasing in width until pin 16 is up to 5V. The internal oscillator is fixed at 100kHz, a frequency that has proven to be a good compromise between small size and efficiency. The internal architecture of the UC3578 is configured for voltage mode control. The onboard error amplifier is a voltage amplifier with the non-inverting input tied to an internal 2V reference. R10 and R11 form a voltage divider to provide feedback information to the inverting terminal, pin 2. Control loop compensation components R4, R7, C2, C3, and C13 are used to shape the overall closed loop response.

Gate Drive Circuit. Gate drive power for Q1 comes from a voltage V_{GG} on C11 which is charged through D6 when the switch Q1 is off and the freewheel diode D3 is conducting. Circuitry internal to the UC3578 regulates V_{GG} to 14Vdc. When V_{GG} is applied to the gate of Q1, turning it on, the source flies up close to V_{IN}, carrying the floating driver and V_{GG} with it. During the switch on-time D6 prevents V_{GG} from discharging into V_{IN}. Resistor R6 serves two purposes. First, it adds damping to the L-C circuit formed by trace inductance and switch gate-source capacitance. Second, it serves to limit current flow into the substrate of the IC when the SRC node (pin 6) is driven below ground when D3 begins conduction. It is essential that D3 is a Schottky diode so that the SRC pin is not pulled more than 0.6V below ground. A snubber consist-

ing of C5 and R9 is also placed across D3 to reduce high frequency ringing.

Current Limiting Circuitry. CT1 and associated circuitry R1, D1, and R2 sense input current between V_{IN} and the drain of switch Q1. In the UCC3578 the current sense input, pin 15, has a –0.5V threshold with respect to V_{CC}, pin 14. R2 is chosen to develop this signal when the current limit threshold is reached. Under full load conditions the input current during Q1 on time reaches a peak of 7Adc plus 1/2 ΔI, the ripple current. This normal peak current is 7A+0.875A = 7.875A. Headroom of at least 20% is allowed for transient conditions so the current limit trip point is set for a peak current of 10 amps. The selection of the burden resistor for the current transformer is calculated:

$$R2 = \frac{0.5V}{I_{PK}} \bullet \frac{N2}{N1} = \frac{0.5V}{10A} \bullet \frac{100}{1} = 5\Omega \qquad (1)$$

Circuit delays in the IC cause an effective LEB (leading edge blanking) period of approximately 150ns before the circuit will respond to an overcurrent condition. This allows suppression of leading edge spikes from rectifier ringing and/or inductive effects of the sensing circuit. When the desired current limit point is reached the UC3578 discharges the soft start capacitor on pin 16 and initiates a soft restart cycle to minimize fault power. R8 and C9 have been included to form a high frequency filter to reduce the switching noise that reaches the current limit comparator.

POWER CIRCUIT DESIGN

Power Switch Q1. The UC3578 integrated high-side driver allows the user to benefit from the low conduction losses and lower prices of the N-channel MOSFET as compared to a P-channel device. In the telecom buck converter Q1 must block the full input voltage in every cycle, so the voltage rating must be greater than 57.6V Since the ratings for MOSFETs generally step from 60V to 100V we will select a member of the IRF520, IRF530, IRF540 family which is rated for 100V. To do this requires estimation of the conduction and switching losses following the guidelines in reference [2].

Duty Cycle. In order to estimate the size of the heatsink required for Q1 the duty cycle must be determined. The simplified transfer function of an ideal buck regulator is given as:

$$D = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

where D is the duty cycle of the power switch Q1. Reference [3] presents a more detailed equation derived from the volt second balance across the output inductor during the switch ON and OFF times. Comparison between these two methods yields:

Table I. Duty cycle comparison.

	Low Line 38.4V	Nominal Line 48V	High Line 57.6V
Q1 ideal DC	13%	10.4%	8.7%
Q1 realistic DC	15.3%	12.2%	10%

These results show an error of approximately 15% between the two calculations.

IRF520, –530, –540 Comparison. [4] All three of the candidate MOSFETs could handle the peak and continuous current required by the buck telecom application. In order to choose the "best" fit for this example the total power loss was calculated following the procedures in [2] using the realistic duty cycles found above. Graphs are presented for Q1 Power Loss in Watts versus Switching Frequency for low, nominal, and high line conditions in Figs. 2, 3, and 4. In all three cases the IRF530 yielded the lowest approximate losses and is the best choice for the telecom converter. The IRF540 losses were higher in all cases because of the large switching losses. At low line the IRF520 losses grew because of increasing conduction losses.

There are several available heatsinks that have a 40°C rise with 3-4 watts of power dissipation. This choice is made depending on the form factor of the application and the availability or lack of forced air.

Diode D3. D3 is a Schottky diode used to carry the freewheeling current, and should have a voltage rating larger than the maximum input voltage with a safety margin. The power dissipation is approximately 3.7 watts [2]. Since V_{IN} may range up to 57.6Vdc in this application a 100V schottky di-

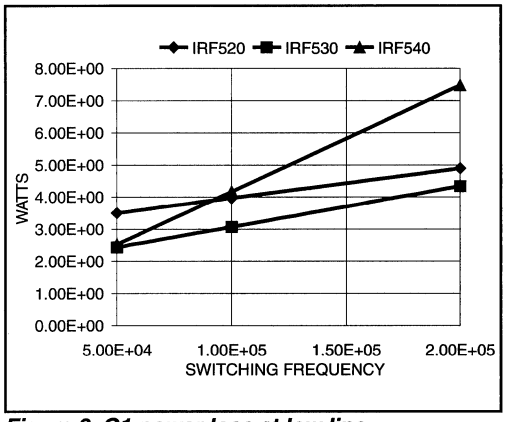

Figure 2. Q1 power loss at low line.

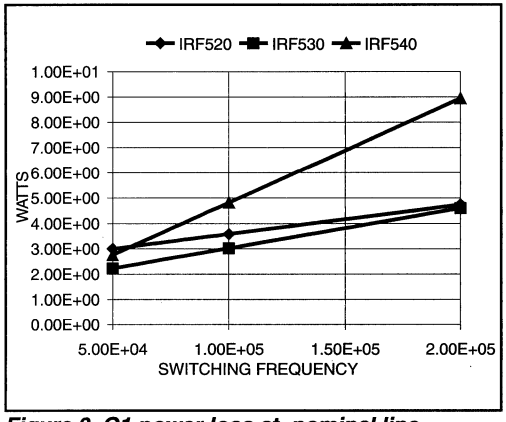

Figure 3. Q1 power loss at nominal line.

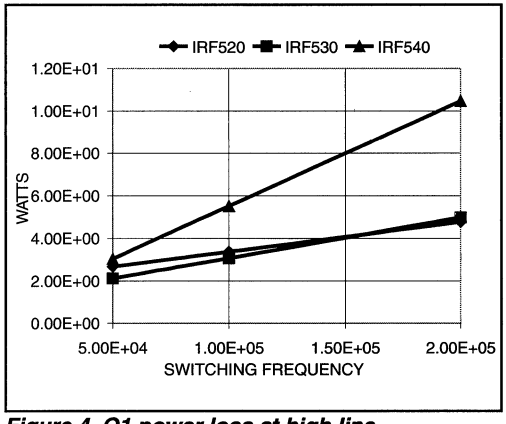

Figure 4. Q1 power loss at high line.

ode is specified, the MBR10100 [5]. The same heatsink specified for Q1 will also be used for D3.

OUTPUT INDUCTOR SELECTION

The output filter of the buck regulator can be optimized around many parameters. These include transient response, output ripple voltage, physical size, temperature rise, and other factors including availability and cost of parts. This design has been undertaken with the goal of obtaining good electrical performance using commercially available parts. Setting the ripple current in the circuit to 25% of the full load current results in a ripple current ΔI of 1.75A. Using the basic inductor equation:

$$V = L\frac{\Delta I}{\Delta T}, \tag{3}$$

which, when rearranged to find the inductance and substituting the appropriate values yields the minimum inductor value:

$$L = \frac{(V_{IN} - V_{Q1} - V_{OUT}) \bullet T_{ON}(\max)}{\Delta I} \tag{4}$$

$$= \frac{(38.2V - 1.7V - 5V) \bullet 1.44\,\mu\,\text{sec}}{1.75A} = 26\mu H$$

Several vendors list inductors in this range which are capable of handling 7A. In order to have an inductance over 26μH at full load the no load inductance may be considerably higher. Many available choices are based on low cost powdered iron that can have a "soft" saturation characteristic as their current is varied from minimum to maximum. In this case the inductor value decreases as the DC load current increases. The designer must insure that the full load inductor value is known to predict the ripple voltage on the output. The winding resistance of the inductor is generally given so the power loss can be calculated. part #CTX50-5-52, rated 50μH, was selected for use. It has a series resistance of 0.021Ω, with an inductance of at least 32.5μH at 10A.

CHOOSING THE OUTPUT CAPACITOR

The output capacitor choice can strongly affect the regulator size and cost. For the battery charger in [2] the output capacitor was chosen for its ability to handle the inductor ripple current and to provide filtering in the absence of the battery. Output ripple voltage and transient capability were not a major concern because the battery swamps out the effect

of the output filter capacitor. In buck regulators driving sensitive electronic loads the ripple voltage and transient capability now become major factors in choosing the output capacitors, along with ripple current capability. To ensure margin for specification compliance the output voltage ripple calculations are done using 37.5mV as a limit, which is 75% of the 50mV requirement.

Equation [5] from [6] allows calculation of the RMS ripple current flowing through the output capacitor.

$$I_{RIP} = \frac{\Delta I}{\sqrt{12}} = \frac{1.75A}{3.46} = 0.505A \quad (5)$$

If capacitors were ideal and had no parasitic resistance or inductance, the following equation from [6] would define the capacitance needed to carry the specified amount of ripple current with the stated voltage ripple at a fixed frequency:

$$C = \frac{\Delta I}{8 \bullet f \bullet \Delta V} = \frac{1.75A}{8 \bullet 100kHz \bullet 0.0375V} = 58.3\mu F \quad (6)$$

In real applications the capacitor ESR plays a major role in determining the output ripple voltage. In this example we want to calculate the maximum ESR allowed to stay within the ripple voltage specification using the ripple current calculated with an inductance of 32.5µH:

$$ESR = \frac{\Delta V}{\Delta I} = \frac{0.0375V}{1.4A} = 27m\Omega \quad (7)$$

The output capacitor chosen must have the following attributes:

A. voltage rating 20% greater than 5V

B. ripple current capability over 0.505A (5)

C. minimum value of 58.3µF (6)

D. ESR below 28mΩ at temperatures of interest (7)

The options available to the designer are as follows:

1) bulk capacitance: use one or more capacitors from one of the three applicable classes (Aluminum Electrolytic, Tantalum, or Organic Semiconductor) to meet the minimum capacitance and maximum ESR requirements.

2) fit capacitors to handle the inductor ripple current and then add a secondary L-C filter to meet the output voltage ripple requirements.

Table II. shows electrical parameters and normalized costs for the various capacitor technologies that are candidates for the output filter in this 100kHz buck converter. The cost figures were taken for a quantity of 1000 pieces through normal distribution channels. The total cost factor is based on the number of capacitors needed in parallel to reach the ESR goal of 27mΩ. In this example the Total Cost Factor of 1 is assigned to the use of two 2200µF aluminum electrolytic capacitors. The ripple current is over 1A for any one capacitor of the types mentioned, so the specific ratings are not given. It is evident that these choices present severe tradeoffs between cost and size of the buck converter. Option 2, incorporating a secondary L-C ripple filter, is not investigated in this presentation.

Another factor worthy of mention pertains to the transient loads the power supply may be subjected to in its application. Solutions that utilize the smaller capacitance values may have larger transient deviations because these load changes must propagate through the L1-C6 output filter. A larger capacitor would have more stored energy to supply the load while the inductor current climbs to the larger value of load current. The telecom buck converter incorporates two aluminum electrolytic output capacitors to minimize costs while providing a large value of reservoir capacity to handle load transients. For comparison, the design was also configured and stabilized with one capacitor to demonstrate the smallest practical size solution.

Table II. Capacitor technology comparison.

Manufacturer	Part Number	Type	Voltage	Value	ESR mΩ	No. Needed	Total Cost Factor
Panasonic	HFQ Series ECA-OJFQ222 [7]	Al El	6.3V	2200µF	0.042	2	1
Sanyo	SA Series 6SA330M [8]	OS	6.3V	330µF	0.025	1	1.45
AVX TPS	Series TPSE337M006R0100 [9]	Tantalum	6V	330µF	0.100	4	8.7

CONTROL LOOP STABILITY CONSIDERATIONS

Aluminum Electrolytics. In the UC3578 evaluation board the filter components have been chosen as follows:

Output Capacitors C6A,C6B:	total 4400µF, ESR approximately 0.021Ω
Output Inductor L1:	used 32.5µH for 10A rating

These values allow one to calculate the output corner frequency as:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{4400\mu F \bullet 32.5\mu H}} \quad (8)$$

$$= 421Hz$$

Due to the capacitor ESR, Fig. 5, the output filter capacitors contribute a power circuit zero at a frequency of:

$$F_Z = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}} \quad (9)$$

The gain falls with a –2 slope after the LC filter resonance, and this is converted to a –1 slope at the frequency where the capacitor ESR equals the capacitive impedance. This slope continues through the desired unity gain crossover frequency of 10kHz.

The UC3578 error amplifier should be tailored to have flat gain in this region to maintain the –1 slope for stable operation [10], and this can be achieved as shown in Fig.6 using an amplifier [11] with a zero-pole pair as shown below:

This amplifier configuration has been fully analyzed in [11] to yield a pole at the origin that sets the initial –1 slope, a zero at $1/2\pi$(R4C2), and a pole at $F_P=1/2\pi$(R4C3). The zero turns the gain slope from –1 to 0 before the unity gain crossover frequency of 10kHz is reached, and the pole turns the slope from 0 to –1 to roll off the gain at high fre-

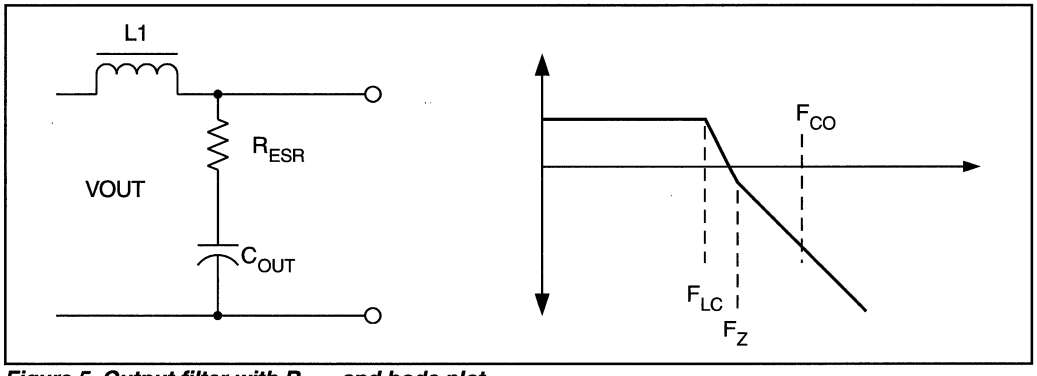

Figure 5. Output filter with R_{ESR} and bode plot.

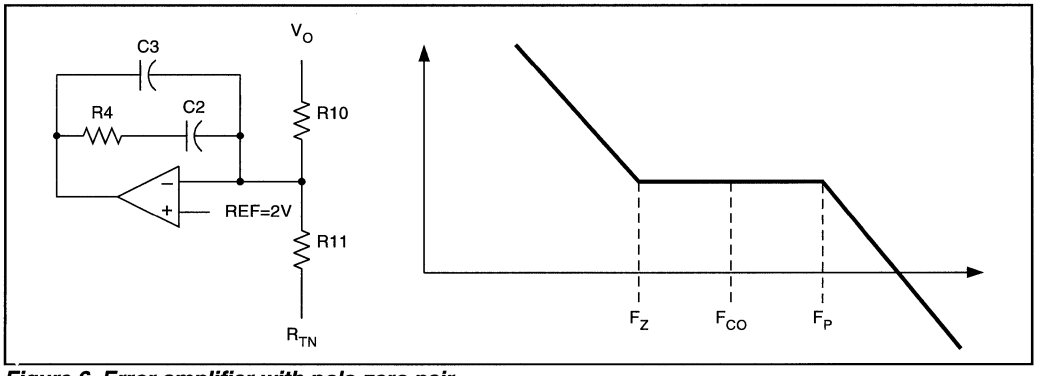

Figure 6. Error amplifier with pole-zero pair.

quencies. A summary of the demo board component selections is given in Table III.

OSCON Capacitors. The circuit was also built using the OSCON output capacitors.

Output Capacitor	330µF, ESR 0.025Ω
Output Inductor	32.5µH

This yielded a new output corner frequency of:

$$F_O = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{30\mu H \bullet 330\mu F}} \quad (10)$$
$$= 1.6\,kHz$$

In the OSCON capacitor circuit the ESR zero at 19.3kHz is beyond the crossover frequency of 12.5kHz, so the output filter characteristic exhibits a –2 slope throughout this region, as shown in Fig. 7.

For this situation the error amplifier must provide a +1 slope during the crossover region to convert the overall loop slope to –1. This requires an amplifier with two pole-zero pairs with the schematic and characteristic shown in Fig. 8.

Output Capacitor Summary. The Telecom Buck Regulator could be implemented with various output capacitor technologies. The aluminum provide the lowest cost solution with a good transient response due to the large bulk capacitance. The OSCON family provides the smallest solution with an acceptable transient response at a higher cost. Both versions may be implemented and stabilized on the demo board; it is left for the user to evaluate the best configuration for any particular application.

THERMAL CONSIDERATIONS IN HIGH VOLTAGE APPLICATIONS

The UC3578 voltage regulator is able to operate from an input voltage range of 14-72Vdc. However, in the Product Data Handbook pages 3-112 and 3-113 it is shown that thermal considerations play a limiting role in the application of the UC3578 integrated circuit as the supply voltage is increased. In the Data Handbook, Section 12, the package ratings for Unitrode parts are presented. This information allows calculation of the junction temperature rise for various power dissipation levels. For example, the 16 pin DP SOIC power lead frame has a thermal resistance Δja of 58°C/W on a 5 square inch FR4 PC board with one ounce copper. The maximum allowable power at 70°C is

$$P_D = \frac{(150°C - 70°C)}{58°C/W} = 1.38W. \quad (11)$$

For the 16 pin plastic batwing the allowable power is 1.6W at 70°C. Using this information we can derive a package derating as shown in Fig. 9. At 150°C no power dissipation is allowed, and at 70°C the differences between the two packages can be observed. Operation is only permitted to the left of the line representing a particular package; to the right the maximum junction temperature will be exceeded. Reliability is enhanced as the operating point is moved farther left from the line.

In the application using the DP package the input supply voltage is limited to approximately 40 Vdc because of power dissipation (approximately 1W) in the device package. It becomes obvious that the key to utilize the UC3578 in the 48Vdc input application is to find a way to dissipate the excess bias power external to the control IC. Methods to accomplish this are presented in this application note.

BIAS CURRENT COMPONENTS

At this point it is appropriate to discuss the three components of the bias currents feeding the circuit; namely I_{VCC}, I_{VGG}, and I_{GATE}. I_{VCC} is the quiescent current drawn to power the entire chip except for the floating gate driver V_{GG}. Current I_{VGG} supplies the driver section quiescent current through an external diode. The current needed to drive the external MOSFET, I_{GATE}, is supplied through the external diode and V_{GG} regulator. The power related to I_{VCC} and I_{VGG} is dissipated internally to the UC3578, however, this is not the case for I_{GATE}. The only power loss internal to the IC due to I_{GATE} comes from conduction of the totem pole driver section while the MOSFET gate is being charged and discharged.

I_{GATE} varies with the choice of the power MOSFET used as the buck switch. The IRF530 was selected to minimize the heatsink size needed in the circuit layout. The total gate charge, which must be supplied to drive this device, is 26nC [4]. This requires a current of

$$I_{GATE} = Q_G \bullet f_S = 26nC \bullet 100kHz = 2.6mA \quad (12)$$

At = 14V this represents a power loss of 36mW, and only a small portion of this is dissipated in the integrated circuit. This loss is small in comparison to that due to I_{VCC} and I_{VGG} and will not be in-

Table III. Control loop with aluminum electrolyte capacitors.

Filter cutoff	421Hz
ESR zero	1.81kHz
Modulator Gain	+23dB
Sampling Gain	–8dB
F_{CO} chosen	10kHz
E/A gain at F_{CO}	23dB
E/A zero frequency	1.54kHz
E/A pole frequency	40kHz
C2	2200pF
C3	85pF (used 100pF)
C13	Not used
R4	47k
R7	Not used
R10	8.25k

Table IV. Control loop with OSCON capacitors.

ESR zero	19.3kHz
Filter cutoff	1.6kHz
Sampling Gain	–8dB
F_{CO} chosen	12.5kHz
E/A 1st zero frequency	1.2kHz
E/A 2nd zero frequency	1.5kHz
E/A 1st pole	Origin
E/A 2nd pole	19.3kHz
E/A 3rd pole	50kHz
C2	6.8nF
C3	470pF
C13	1.5nF
R4	20k
R7	2.2k
R10	69.8k
R11	46.4k

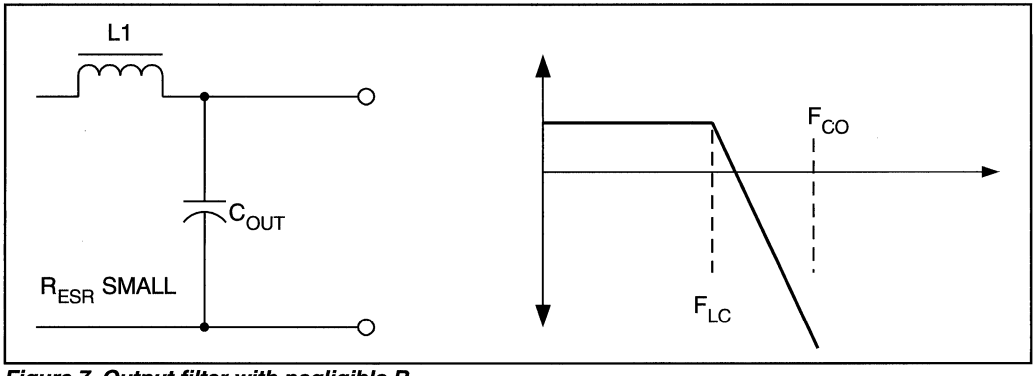

Figure 7. Output filter with negligible R_{ESR}.

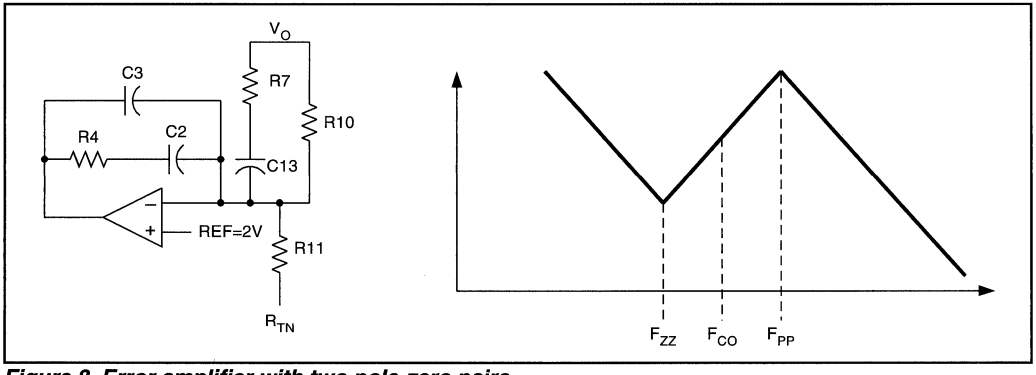

Figure 8. Error amplifier with two pole-zero pairs.

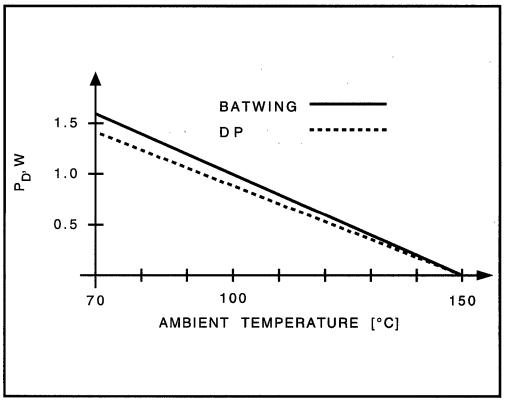

Figure 9. Allowable power disapation vs. ambient temperature.

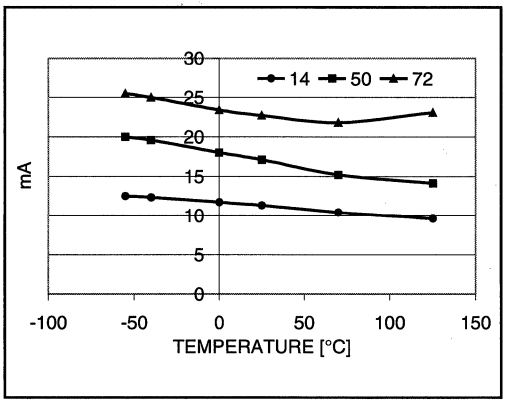

Figure 10. Variation of I_{CC} versus V_{CC} and temperature.

cluded in calculations for junction temperature for the IC.

Maximum specifications for I_{VCC} and I_{VGG} are given in the Product Data Handbook as I_{VCC}(max)=14mA and I_{VGG}(max)=10.5mA. I_{CC} varies with temperature and V_{CC} as given in Fig. 10. In the 48Vdc demo circuit our goal will be to regulate V_{CC} as V_{IN} increases. This will reduce the power dissipated in the UC3578 to levels which allow operation at V_{IN}=48Vdc with a reasonable T_J(max).

COMPARISON OF VCC SUPPLY METHODS

Two methods will be considered to limit the voltage available to supply bias power to the UC3578.

(1) Series dropping resistor

(2) VCC voltage regulator

The series resistor can be utilized in the lowest cost applications and works best when the supply voltage variation is relatively small. The resistor must be sized to allow the maximum required current at the minimum input voltage. In this case

$$R_{LIM} = \frac{(V_{IN}(\min) - V_{CC})}{(I_{VCC} + I_{VGG} + I_{GATE})} \quad (13)$$
$$= \frac{38.4V - 14V}{14mA + 10.5mA + 2.6mA} = 900\Omega$$

Note that was included because the associated voltage must be dropped on the resistor even though very little of this power is dissipated in the IC. As the input is increased to V_{IN}(max) = 57.6V the drop across R_{LIM} remains essentially constant because the I_{CC} increase seen with higher V_{CC} is offset by the I_{CC} decrease at higher junction temperature. Now,

$$V_R(\text{lim}) = 27.1mA \bullet 820\Omega = 22.2V, \quad (14)$$

and

$$V_{CC} = V_{IN}(\max) - V_R(\text{lim}) = 57.6V - 22.2V \quad (15)$$
$$= 35.4V$$

The UC3578 power dissipation is now

$$P_D = V_{CC} \bullet (I_{VCC} + I_{VGG}) \quad (16)$$
$$= 35.4V \bullet 24.5mA = 0.87W$$

At high V_{IN} calculate the UC3578 temperature rise is:

$$\Delta T_{JA} = \theta_{JA} \bullet P_D = 50°C/W \bullet 0.87W \quad (17)$$
$$= 43.5°C$$

This is a significant improvement over the databook example in which V_{CC} was limited to 40V.

VCC REGULATOR

The voltage regulator in Fig. 1 consists of Q2, R3, and D2. D2 is a 16V zener diode connected from base of Q2 to ground, so the bias voltage on the emitter of Q2 is regulated to one diode drop below the zener, or approximately 15V. R3 is selected to bring D2 into conduction and also provide base current to Q2. A power MOSFET could also be

used by increasing the zener diode value to offset the drop of the gate-source threshold voltage. A current regulator was not chosen for this application because the V_{CC} level supplied to the chip would vary as I_{CC} changes with temperature, possibly necessitating the addition of a second zener to clamp V_{CC} to a fixed level.

Under these conditions with V_{CC}=15V the power dissipated in the IC is:

$$P_D = V_{CC} \bullet (I_{VCC} + I_{VGG}) = 15V \bullet 24.5mA \quad (18)$$
$$= 0.37W$$

With this power dissipation we can find the junction temperature rise:

$$\Delta T_{JA} = \theta_{JA} \bullet P_D = 0.37W \bullet 50°C/W \quad (19)$$
$$= 18.5°C$$

This allows room to increase the maximum ambient temperature to the full industrial range or to raise the allowable V_{IN} range upward to 72Vdc(max), as long as the junction temperature and allowable power dissipation are monitored. Keep in mind that the bias voltage regulator should be sized to handle 1W of power at V_{IN} of 57.6V.

RESISTIVE CURRENT SENSE APPLICATIONS

Alternate circuits that utilize the UC3578 at lower input voltages and/or reduced ambient temperatures will often be able to fit a current sense resistor in place of the current transformer. In this case the filter formed by R8 and C9 is more critical to provide a clean waveform because there is no current transformer with associated filtering action to reduce the noise produced during the switching operation.

To use the demo board in a resistive current sense application, configure the circuit as follows:

Remove Components	Populate Components
CT1, R1, R2, D1, Q3, R3, D2	R_A, R_B, R_C

R_A is selected to produce 0.5V when input current limiting has reached the current limit activation level. R_B is a low value jumper (<=10Ω) to tie the current sense signal into the filter components R8 and C9. R_C is also a low value jumper (<=10Ω) to provide bias directly to the IC from V_{IN}.

OTHER CONSIDERATIONS

The UCC3578 is capable of operating at a duty cycle down to approximately 6%. Below this amount the controller will begin to skip pulses to maintain the output at the desired value. Fig. 11 gives an approximate V_O versus V_{IN} calculated using the ideal duty cycle equation. This is used to give a worst case estimate because it has been shown that the realistic duty cycle runs a little longer than the ideal duty cycle because of the effect of parasitic circuit components.

EVALUATION BOARD PERFORMANCE

The evaluation board was built and tested using the parts list given. Typical efficiencies are given in Table V. for the operating conditions listed.

A load transient from 2.5A to 5.0A was applied to the demo board to compare the two output capacitor configurations discussed in the stability section. Fig. 12 shows the transient response with two 2200µF aluminum electrolytic capacitors installed. It can be seen that the maximum undershoot is 70mV. In Fig. 13 a single 330µF OSCON capacitor was fitted in place of the aluminum electrolytics. Noting that the scales have changed, the maximum undershoot is now near 220mV. The importance of performance, cost, and size tradeoffs

Table V. Typical efficiencies for UC3578 evaluation board.

V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	W_{IN}	W_{OUT}	Efficiency
25V	0.61A	4.92V	2.5A	15.25W	12.30W	81%
35V	0.45A	4.92V	2.5A	15.75W	12.30W	78%
35V	0.91A	4.91V	5.0A	31.85W	24.55W	77%
48V	0.35A	4.91V	2.5A	16.80W	12.28W	73%
48V	0.69A	4.91V	5.0A	33.12W	24.55W	74%
48V	0.97A	4.91V	7.0A	46.56W	34.37W	74%

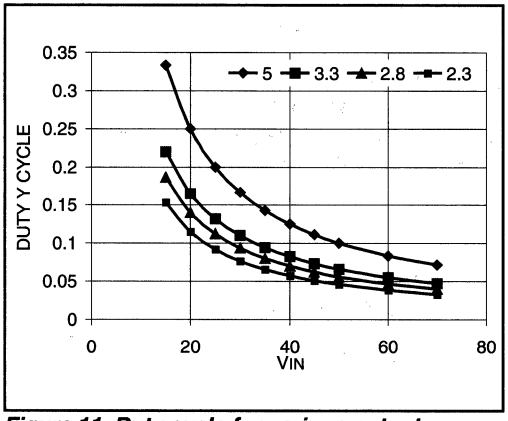

Figure 11. Duty cycle for various output voltages.

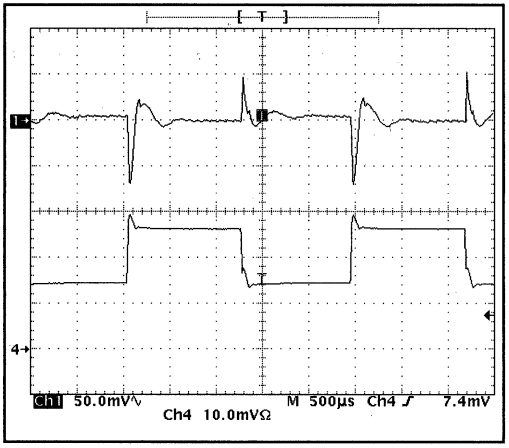

Figure 12. Transient response with two 2200uF aluminum electrolytic capacitors.

must be evaluated to make the most appropriate output capacitor selection.

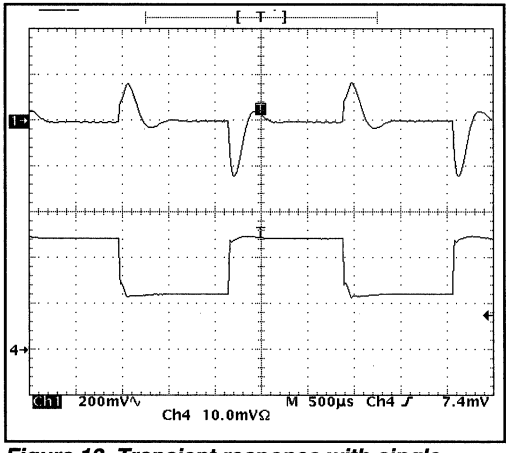

Figure 13. Transient response with single 330uF OSCON capacitor.

SUMMARY

The UC3578 Buck Stepdown Voltage Regulator provides the power supply designer with an integrated circuit controller that incorporates a floating high side driver capable of operating at input voltages up to 72Vdc. This application note explains the power losses associated with using this high voltage IC, and suggests circuit configurations to

Table VI. Evaluation board list of materials.

Reference Designator	Description	Manufacturer	Part #
C1A,B	220µF, 63V, Aluminum Capacitor	Panasonic	ECA-1JFQ221
C2	2200pF, 50V, Ceramic Capacitor		
C3	100pF, 50V, Ceramic Capacitor		
C4	47µF, 50V Aluminum Capacitor		
C5	680pF, 50V, Ceramic Capacitor		
C6A,C6B	2200µF, 6.3V, Aluminum Capacitor	Panasonic	ECA-OJFQ222
C7,C10,C12	0.1µF, 50V, Ceramic Capacitor		
C8	0.01µF, 50V, Ceramic Capacitor		
C9	470pF, 50V, Ceramic Capacitor		
C11	1µF, 50V, Ceramic Capacitor		
C13	See text for use		
CT1	Current transistor, 100:1	Magnetek Triad	CST306-2A
D1	75V, 200mA, Sw. Diode		1N4148
D2	16V Zener Diode, 1W		1N4745A
D3	100V, 10A Sch. Diode		MBR10100
D6	75V, 200mA, Sw. Diode		1N4148
HS1	Heatsink for Q1	Thermalloy	7020B-MT
HS2	Heatsink for D3	Thermalloy	7020B-MT
HS3	Heatsink for Q2	Aavid	579302B00000
L1	30µH, 10A Inductor	Coiltronics	CTX 50-5-52
R1	200Ω, 1/4W, 5% Resistor		
R2	5Ω, 1/4W, 1% Resistor		
R3	15k, 1/4W, 5% Resistor		
R4	47k, 1/4W, 5% Resistor		
R5	330Ω, 1/4W, 5% Resistor		
R6	10Ω, 1/4W 5% Resistor		
R7	See text for use		
R8	470Ω, 1/4W, 5% Resistor		
R9	51Ω, 1W, 5% Resistor		
R10	8.25k, 1/4W, 1% resistor		
R11	5.62k, 1/4W, 1% resistor		
RA	See text for use		
RB	See text for use		
RC	See text for use		
Q1	100V, 0.16Ω, N MOSFET	IR	IRF530
Q2	250V, 1A, NPN		TIP47
U1	Control IC	Unitrode	UC3578N
TB1, TB2	Terminal Block, 2 Pos., 5mm spacing		

relieve the thermal load. In addition, the demo board can be adapted to evaluate resistive current sense versions by making a few simple circuit changes.

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[1] Bob Mammano, *Distributed Power Systems*, Unitrode Power Supply Design Seminar SEM-900, Topic 1, 1993.

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[3] Larry Spaziani, *The UC3886 PWM Controller uses Average Current Mode Control to Meet the Transient Regulation Performance of High End Processors*, U-156 Application Note, Unitrode Applications Handbook, 1997, pp. 3-517 - 3-540.

[4] *HEXFET Power MOSFET Designer's Manual*, International Rectifier, 1993

[5] *Rectifier Device Data*, Motorola, Q1/95

[6] Unitrode SEM 700, *Magnetics Definitions and Equations*, p.M2-3, p. M7-8

[7] Digikey Catalog No. 975Q, Oct. - Dec. 1997, p244

[8] Sanyo OS-CON Technical Book, Ver. 5

[9] AVX TPS Tantalum Low ESR Capacitors Catalog

[10] L. H. Dixon, *Closing the Feedback Loop*, Unitrode Power Supply Design Seminar Manual SEM 700, 1990.

[11] H. Dean Venable and Stephen R. Foster, *Practical Techniques for Analyzing, Measuring, and Stabilizing Feedback Control Loops in Switching Regula-*

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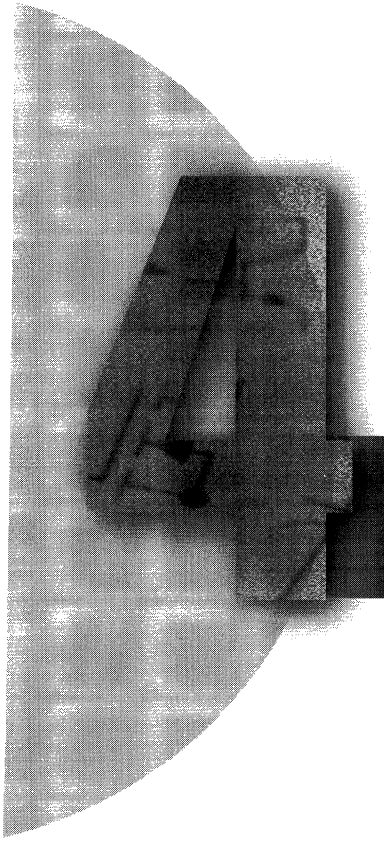

Power Factor Correction

Power Factor Correction

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC3817+	UCC3818+	UCC38500+	UCC38501+	UCC38502+
Soft Switching					
Maximum Practical Operating Frequency	250kHz	250kHz	250kHz	250kHz	250kHz
Current Error Amplifier Bandwidth	3MHz	3MHz	3MHz	3MHz	3MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1A	1A	1A	1A
Startup Current	0.1A	0.1A	0.1A	0.1A	0.1A
Undervoltage Lockout	16V / 10V	10.5V / 10V	16V / 10V	10.5V / 10V	16V / 10V
UVLO 2 Hysteresis			1.2V (300V Turn-off)	1.2V (300V Turn-off)	3V (200V Turn-off)
Overvoltage Protection	Y	Y	Y	Y	Y
Enable Input	Y (with OVP)	Y	Y	Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)
Special Features			DC / DC Controller Included	DC / DC Controller Included	DC / DC Controller Included
Application / Design Note	DN-39E	DN-39E	DN-39E		
Pin Count ❖	16	16	20	20	20
Page Number	PS/4-5	PS/4-5	PS/4-15	PS/4-15	PS/4-15

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC38503+	UC3852	UC3853	UC3854	UC3854A
Soft Switching		ZCT			
Maximum Practical Operating Frequency	250kHz	Variable	125kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	3MHz	N/A	1MHz	800kHz	5MHz
Average Current Mode	Y		Y	Y	Y
Worldwide AC Input Voltage Operation	Y		Y	Y	Y
Output Drive	1A	0.5A	1A	1A	1A
Startup Current	0.1A	1mA	0.25mA	1.5mA	0.3mA
Undervoltage Lockout	10.5V / 10V	16.3V / 11.5V	11.5V / 9.5V	16V / 10V	16V / 10V
UVLO 2 Hysteresis	3V (200V Turn-off)				
Overvoltage Protection	Y		Y		
Enable Input	Y			Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	N/A	Y	Y	Y
Special Features	DC / DC Controller Included				
Application / Design Note		DN-39E, U-132	DN-39E, DN-77, DN-78, U-159	DN-39E, DN-41, U-134	DN-39E, DN-44, DN-66
Pin Count ❖	20	8	8	16	16
Page Number	PS/4-15	PS/4-22	PS/4-27	PS/4-32	PS/4-42

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UC3854B	UC3855A	UC3855B	UCC3857	UCC3858
Soft Switching		ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	200kHz	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1.5A	1.5A	1A	0.5A
Startup Current	0.3mA	0.15mA	0.15mA	0.06mA	0.1mA
Undervoltage Lockout	10.5V / 10V	16V / 10V	10.5V / 10V	13.8V / 10V	13.8V / 10V
Overvoltage Protection		Y	Y		Y
Enable Input	Y	Y	Y		Y
Multiplier / Divider Feedforward	Y	Y	Y	Y (Faster Response)	Y (Faster Response)
Special Features		Current Synthesizer	Current Synthesizer	Single Stage Isolated Output	Improved Efficiency at Light Load
Application / Design Note	DN-39E, DN-44, DN-66	DN-39E, DN-66, U-153	DN-39E, DN-66, U-153	DN-39E	DN-39E, DN-90
Pin Count ❖	16	20	20	20	16
Page Number	PS/4-42	PS/4-48	PS/4-48	PS/4-56	PS/4-65

❖The smallest available pin count for thru-hole and surface mount packages.
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UNITRODE

BiCMOS Power Factor Preregulator

FEATURES

- Controls Boost Preregulator to near Unity Power Factor
- Limits Line Distortion
- World Wide Line Operation
- Over-voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- High Bandwidth, Low Offset Current Amplifier
- Improved Noise Immunity
- Improved Feedforward Line Regulation
- Leading Edge Modulation
- 150µA Start Up Current
- Low Power BiCMOS Operation
- 12V to 17V Operation

DESCRIPTION

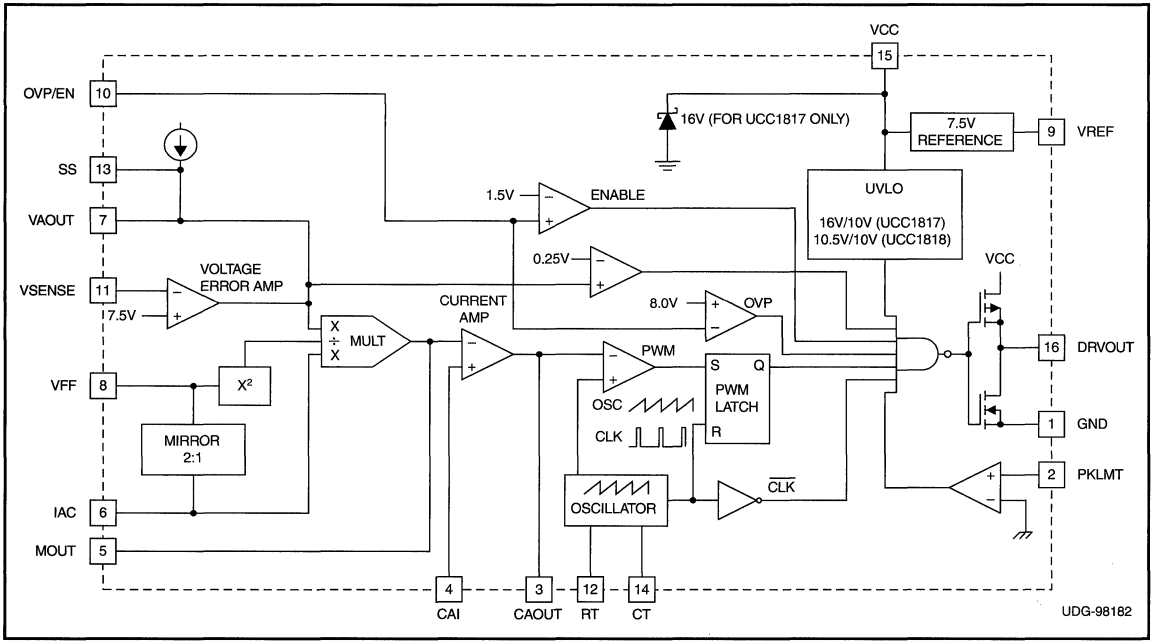
The UCC1817/UCC1818 provides all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to that of the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Unitrode's BiCMOS process, the UCC1817/UCC1818 offers new features such as lower start-up current (250µA MAX.), lower power dissipation, over-voltage protection, a shunt UVLO detect circuitry, a leading-edge modulation technique to improve ripple current in the bulk capacitor and an improved, low-offset (±2mV) current amplifier to reduce distortion at light load conditions.

UCC1817 offers an on-chip shunt regulator with low start-up current, suitable for applications utilizing a bootstrap supply. UCC1818 is intended for applications with a fixed supply (VCC.)

Available in the 16-pin N, D, DW and J and 20 pin L and Q packages.

BLOCK DIAGRAM

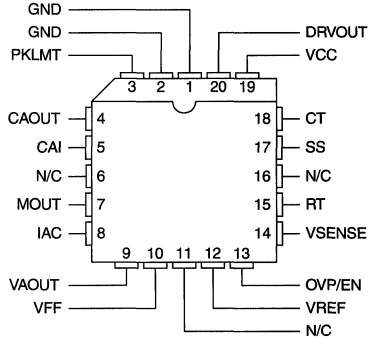


ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC 18V
Gate Drive Current,
  Continuous 0.2A
  50%Duty Cycle 1A
Input Voltage,
  CAI, MOUT 8V
  PKLMT 5V
  VSENSE, OVP/EN 10V
Input Current, RT, IAC, PKLMT 10mA
Maximum Negative Voltage, DRVOUT,PKLMT,MOUT . . –0.5V
Power Dissipation 1W

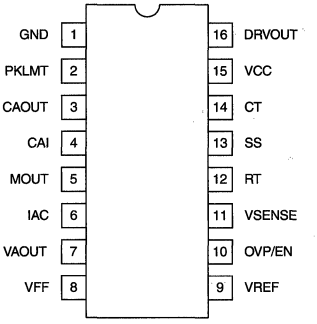
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



CONNECTION DIAGRAMS

SOIC-16, DIL-16 (TOP VIEW)
D, DW, N and J Packages



ORDERING INFORMATION

UCC □ 81 □ □
- PACKAGE
- PRODUCT OPTION
- TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3817, –40°C to +85°C for the UCC2817, and –55°C to +125°C for the UCC1817, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, Off	CAOUT, VAOUT = 0V, VCC = 15.5V		150	250	µA
Supply Current, On	VCC = 12V, No Load on DRVOUT		4	6	mA
UVLO Section					
VCC Turn-On		15.4	16	16.6	V
UVLO Hysteresis		5.8	6	6.2	V
Maximum Shunt Voltage	I_{VCC} = 10mA		17	17.5	V
VCC Turn-On Threshold (UCC1818)		10.2	10.5	10.8	V
UVLO Hysteresis (UCC1818)		0.4	0.5	0.6	V
Voltage Amplifier Section					
Input Voltage	T_A = 25°C	7.387	7.5	7.613	V
	T_A = –40°C to +85°C	7.369	7.5	7.631	V
	T_A = –55°C to 125°C	7.313	7.5	7.687	V
V_{SENSE} Bias Current	VSENSE = VREF, VAOUT = 2.5V		50		nA
Open Loop Gain	VAOUT = 2V to 5V		90		dB
V_{OUT} High	I_{LOAD} = –50µA	5.4	5.5	5.6	V
V_{OUT} Low	I_{LOAD} = 150µA		0.1	0.2	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3817, –40°C to +85°C for the UCC2817, and –55°C to +125°C for the UCC1817, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over Voltage Protection and Enable Section					
Over Voltage Reference		7.8	8	8.2	V
Hysteresis		400	500	600	mV
Enable Threshold			1.5	2	V
Current Amplifier Section					
Input Offset Voltage	V_{CM} = 0V, V_{CAOUT} = 3V	–2	0	2	mV
Input Bias Current	V_{CM} = 0V, V_{CAOUT} = 3V		–50		nA
Input Offset Current	V_{CM} = 0V, V_{CAOUT} = 3V		25		nA
Open Loop Gain	V_{CM} = 0V, V_{CAOUT} = 2V to 5V		90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAOUT} = 3V		80		dB
V_{OUT} High	I_{LOAD} = –150µA		7		V
V_{OUT} Low	I_{LOAD} = 1mA		0.2		V
Gain Bandwidth Product	Note 1	3	5		mHz
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.387	7.5	7.6	V
	Over Temperature (UCC38XX)	7.368	7.5	7.631	V
	Over Temperature (UCC28XX, UCC18XX)	7.313	7.5	7.687	V
Load Regulation	I_{REF} = 1mA to 2mA		3		mV
Line Regulation	V_{CC} = 10.8V to 15V		20		mV
Short Circuit Current	V_{REF} = 0V		35		mA
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	V_{CC} = 10.8V to 15V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Peak Voltage		4.5	5	5.5	V
Ramp Amplitude Voltage (peak to peak)			4		V
Peak Current Limit Section					
PKLMT Reference Voltage		–15		15	mV
PKLMT Propogation Delay			500		ns
Multiplier Section					
High Line, Low Power	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 1.25V		–6		µA
High Line, High Power	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 5V		–90		µA
Low Line, Low Power	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 1.25V		–19		µA
Low Line, High Power	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 5V		–300		µA
IAC Limited	I_{AC} = 150µA, V_{FF} = 1V, VA_{OUT} = 5V		–300		µA
Gain Constant	I_{AC} = 300µA, V_{FF} = 3V, VA_{OUT} = 2.5V		1		1/V
Zero Current	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 0.25V			–5	µA
	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 0.25V			–5	µA
Power Limit	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 5V		–300		µA
Feed-Forward Section					
VFF Output Current	I_{AC} = 300µA		–150		µA
Soft Start Section					
SS Charge Current			–10		µA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3817, –40°C to +85°C for the UCC2817, and –55°C to +125°C for the UCC1817, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver Section					
Pull Up Resistance	I_{OUT} = –100mA		5		Ω
Pull Down Resistance	I_{OUT} = 100mA		2		Ω
Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		10		ns
Zero Power Section					
Zero Power Comparator Threshold	Measured on VA_{OUT}		0.25		V

Note 1: Guaranteed by design, not 100% tested in production.

PIN DESCRIPTIONS

CAI: (current amplifier non-inverting input) This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: (current amplifier out) This is the output of a wide bandwidth op amp that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct current.

CT: (oscillator timing capacitor) A capacitor from CT to GND will set the PWM oscillator frequency according to:

$$f = \left[\frac{0.725}{(RT \bullet CT)}\right]$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on DRVOUT. Use a series gate resistor of at least 5Ω to prevent interaction between the gate impedance and the DRVOUT output driver that might cause the DRVOUT to overshoot excessively. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: (ground) All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor.

IAC: (input AC current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to multiplier output.

MOUT: (multiplier output and current sense inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is given by the equation:

$$I_{MULT} = \frac{(VAOUT - 1) \bullet I_{AC}}{{V_{FF}}^2 \bullet K} \;;$$

where K = 1 (multiplier gain constant.)

OVP/EN: (over voltage/enable) A window comparator input which will disable the output driver if the boost output is 5% above nominal or will disable both the PFC output driver and reset SS if pulled below 1.5V.

PKLMT: (PFC peak current limit) The threshold for pklimit is 0.0V. Use a resistor divider from the negative side of the current sense resistor to V_{REF} to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0V.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10kΩ and 100kΩ is recommended.

SS: (soft start) SS is at ground for either enable low or VCC too low conditions. When enabled, SS will charge an external capacitor with a current source. This voltage will be used as the voltage error signal during startup enabling the PWM duty cycle to increase slowly. In the event of a disable command or a V_{CC} dropout, SS will quickly discharge to disable the PWM.

VAOUT: (voltage amplifier out) This is the output of the opamp that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20mA between 10V and 17V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices will be inhibited unless VCC exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

PIN DESCRIPTIONS (cont.)

VFF: (feed-forward signal) RMS signal generated at this pin by mirroring I_{AC} into a single pole external filter.

$$R_{VFF} = \frac{VFF_{MAX}}{\sqrt{2} \bullet \frac{IAC_{MAX}}{2} \bullet 0.9}$$

VSENSE: (voltage amplifier inverting input) This is normally connected to a feedback network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when V_{CC} is below the UVLO threshold. Bypass VREF to GND with a 0.1µF or larger ceramic capacitor for best stability.

4

TYPICAL APPLICATION SCHEMATIC

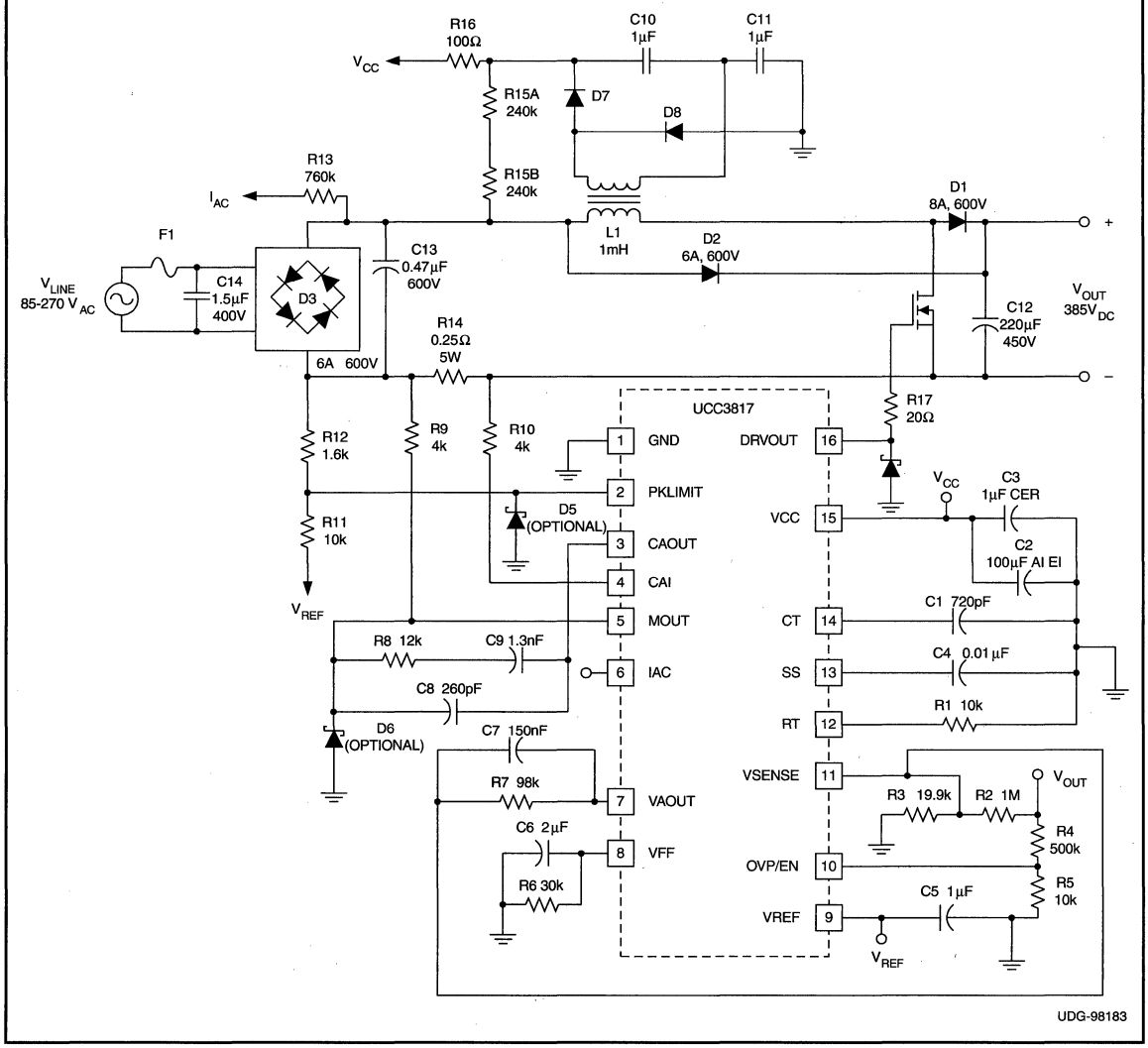


Figure 1. Typical application circuit.

APPLICATION INFORMATION

The UCC3817 is a BiCMOS average current mode boost controller for high power factor, high efficiency preregulator power supplies. Fig. 1 shows the UCC3817 in a 250W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform will have high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$$PF = \cos\Theta$$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with THD (total harmonic distortion) less than 3% are possible with a well-designed circuit. Following guidelines are provided to design PFC boost converters using the UCC3817.

Power Stage

L_{BOOST}: The boost inductor value is determined by multiplying the minimum input voltage by the maximum duty cycle and dividing this by the product of the switching frequency and the inductor ripple current allowed in the design. Ripple current is a function of L. Maximum ripple occurs at minimum input voltage:

$$L_{BOOST} = \frac{\left(V_{IN(\min)} \bullet D\right)}{(\Delta I \bullet f_S)}$$

For the example circuit a switching frequency of 100kHz, a ripple current of 875mA, a maximum duty cycle of 0.688 and a minimum input voltage of $85V_{RMS}$ gives us a boost inductor value of about 1µH.

C_{OUT}: Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the holdup time required for supporting the load after input AC voltage is removed. Hold up is the amount of time that the output stays in regulation after the input has dropped below the specified input range. For this circuit a 60Hz input voltage yields a hold up time of approximately 16ms. Expressing the capacitor value in terms of output power, output voltage, and hold up time gives the equation:

$$C_{OUT} = \frac{(2 \bullet P_{OUT} \bullet \Delta t)}{\left(V_{OUT}{}^2 - V_{OUT(\min)}{}^2\right)}$$

In practice the calculated minimum capacitor value may be inadequate because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often necessitates the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed can be determined by dividing the maximum specified output ripple voltage by the inductor ripple current.

In this design hold-up time was the dominant determining factor and a 220µF 450V capacitor was chosen for the output voltage level of 385VDC at 250W.

Power Switch Selection

As in any power supply design, tradeoffs between performance, cost, and size have to be made. When selecting a power switch it can be useful to calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C_{OSS} loss and turn-on and turn-off losses:

$$P_{GATE} = Q_{GATE} \bullet V_{GATE} \bullet fs$$

$$P_{COSS} = \frac{1}{2} \bullet C_{OSS} \bullet V^2{}_{OFF} \bullet fs$$

$$P_{ON} + P_{OFF} = \frac{1}{2} \bullet V_{OFF} \bullet I_L \bullet (t_{ON} + t_{OFF}) \bullet F_S$$

where Q_{GATE} is the total gate charge, V_{GATE} is the gate drive voltage, f_S is the clock frequency, C_{OSS} is the drain source capacitance of the MOSFET, T_{ON} and T_{OFF} are the switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH}) and V_{OFF} is the voltage across the switch during the off time, in this case $V_{OFF} = V_{OUT}$.

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \bullet K \bullet I^2{}_{RMS}$$

where K is the temperature factor found in the manufacturer's $R_{DS(on)}$ vs. junction temperature curves.

Calculating these losses and plotting against frequency gives a curve which enables the designer to determine either which manufacturer's device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. In this example the switch was chosen as the best trade off between performance, availability and cost. An excellent review of this procedure can be found in the Unitrode Power Supply Design Seminar SEM1200, Topic 6, Design Review: 140W, [*Multiple Output High Density DC/DC Converter*].

APPLICATION INFORMATION (cont.)

Multiplier

The output of the multiplier of the UCC3817 is a signal representing the desired input line current. It is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are V_{EA}, the voltage amplifier error signal, IAC, a representation of the input rectified AC line voltage, and an input voltage feedforward signal, V_{FF}. The output of the multiplier, I_{MO}, can be expressed:

$$I_{MO} = \frac{K \bullet I_{AC} \bullet (V_{EA} - 1)}{V_{FF}^{\,2}}$$

where K is a constant typically equal to 1.

The I_{AC} signal is obtained through a high value resistor connected between the rectified AC line and the IAC pin of the UCC3817. This resistor is sized to give the maximum I_{AC} current at high line. For this device the maximum I_{AC} current is about 500µA. A higher current than this can drive the multiplier out of its linear range. A smaller current level will be functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 to 270VAC gives a resistor value of 750kΩ. Because of voltage rating constraints of standard 1/4W resistors, use a combination of lower value resistors connected in series to give the 750kΩ value and distribute the high voltage across two or more resistors.

The current through the I_{AC} resistor is mirrored internally to the V_{FF} pin where it is filtered to produce a voltage feedforward signal proportional to line voltage and free of a 120Hz ripple component. This second harmonic ripple component at the V_{FF} pin is one of the major contributors to harmonic distortion in the system, so adequate filtering is crucial. Refer to Unitrode Power Supply Design Seminar, SEM-700 Topic 7, [*Optimizing the Design of a High Power Factor Preregulator.*] Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input AC line voltage, the amount of attenuation required by this filter is:

$$\frac{1.5\%}{66\%} \text{ or } .022$$

A ripple frequency (f_R)of 120Hz and an attenuation of .022 gives us a single pole filter with:

$$Fp = 120Hz * 0.022Hz \text{ or } 2.6Hz$$

The range of this input to the multiplier should be 0.5V to 5.5V over the line input range. Therefore the filter resistor should be sized accordingly. Maximum I_{AC} current is 500µA, mirrored 2:1 to V_{FF} becomes 250µA. The DC output is 90% of the RMS value of this half sine wave, or 159µA. So the filter resistor should be equal to the voltage swing of the input to the multiplier divided by the DC current or:

$$\frac{5V}{159\mu A} = 31.44k\Omega$$

Select 30kΩ for a standard value. Solving for the capacitor value:

$$C_f = \frac{1}{2\pi(30K)(2.6Hz)} = 2\mu F$$

This results in a single pole filter, which will adequately attenuate the harmonic distortion and also meet the DC requirement of the proper voltage swing across line conditions.

The R_{MO} resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or $I_{MO(max)}$, can be determined by the equation:

$$I_{MO(max)} = \frac{\left(K_M \bullet I_{AC}@LOWLINE \bullet \left(V_{EA(max)} - 1V\right)\right)}{V_{FF}^{\,2}(min)}$$

$I_{MO(max)}$ for this design is approximately 315µA. The R_{MO} resistor can then be determined by

$$R_{MO} = \frac{V_{RS}}{I_{MO(max)}}$$

In this example R_{MO} is equal to 3.91kΩ.

Voltage Loop

The second major source of harmonic distortion in an off-line converter is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier and appears as a 3rd harmonic ripple at the input to the multiplier. The voltage loop must be compensated not just for stability but also to attenuate the contribution of this ripple to the total harmonic distortion of the system. Refer to Fig. 2.

The gain of the voltage amplifier, G_{VA}, can be determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

$$V_{OPK} = \frac{P_{IN}}{(2\pi \bullet f_R \bullet C_{OUT} \bullet V_{OUT})}$$

APPLICATION INFORMATION (cont.)

In this example V_{OPK} is equal to 3.91V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the total harmonic distortion budget we set the gain equal to:

$$G_{VA} = \frac{(\Delta V_{AOUT} \bullet 1.5\%)}{V_{OPK}}$$

where V_{AOUT} is the effective output voltage range of the error amplifier (5V for the UCC3817). The network needed to realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_f and R_f. The value of R_{IN} is already determined because of its function as one half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case the value was chosen to be 1MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice the resistor value would be realized by the use of two 500kΩ resistors in series because of the voltage rating constraints of most standard 1/4W resistors. The value of C_f is determined by the equation:

$$C_f = \frac{1}{(2\pi \bullet f_R \bullet G_{VA} \bullet R_{IN})}$$

In this example C_f equals 65nF. Resistor R_f sets the DC gain of the error amplifier and thus determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^2 = \frac{P_{IN}}{(2\pi \bullet \Delta V_{AOUT} \bullet V_{OUT} \bullet R_{IN} \bullet C_{OUT} \bullet C_f)}$$

F_{VI} for this converter is 15Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1, [*A 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions*].

Solving for R_f becomes:

$$R_f = \frac{1}{(2\pi \bullet F_{VI} \bullet C_f)}$$

or R_f equals 150kΩ.

Current Loop

The gain of the power stage is:

$$G_{ID}(s) = \frac{(V_{OUT} \bullet R_{SENSE})}{(s \bullet L_{BOOST} \bullet V_P)}$$

R_{SENSE} has been chosen to give the desired differential voltage for the current sense amp at the desired current limit point. In this example a current limit of 4A and a reasonable differential voltage to the current amp of 1V gives a R_{SENSE} value of 0.25Ω. V_P in this equation is the voltage swing of the oscillator ramp, 4V for the UCC3817. Setting the crossover frequency of the system to 1/10th the switching frequency, or 10kHz, requires a power stage gain at that frequency of 0.383. In order for the system to have a gain of 1 at the crossover frequency, the current amplifier needs to have a gain of $1/G_{PS}$ at that frequency. G_{EA}, the current amp gain is then:

$$G_{EA} = \frac{1}{G_{PS}} = \frac{1}{0.383} = 2.611$$

Refer to Fig. 3. R_I is the R_{MO} resistor, previously calculated to be 3.9kΩ. The gain of the current amp is R_f/R_I, so multiplying R_I by G_{EA} gives the value of R_f, in this case approximately 10kΩ. Setting a zero at the crossover frequency and a pole at half the switching frequency completes the current loop compensation.

$$C_Z = \frac{1}{2 \bullet \pi \bullet R_f \bullet f_C}$$

$$C_P = \frac{1}{2 \bullet \pi \bullet R_f \bullet \frac{fs}{2}}$$

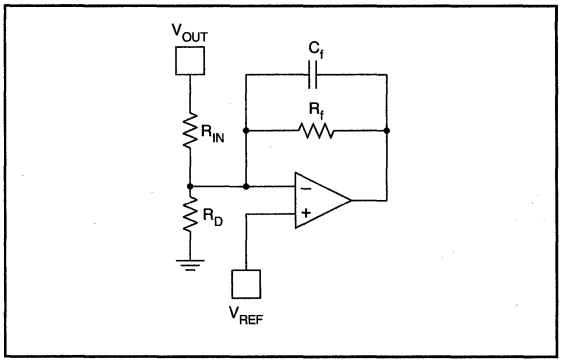


Figure 2: UCC3817 voltage amplifier configuration.

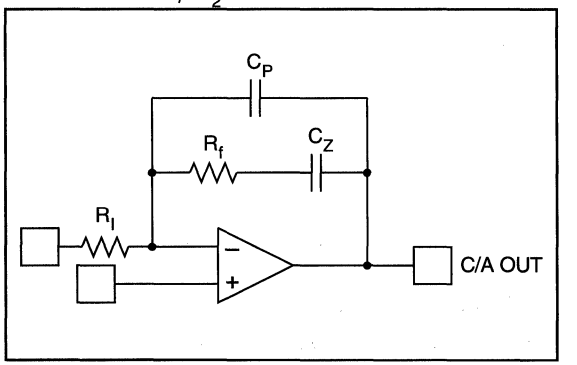


Figure 3. Current loop compensation.

APPLICATION INFORMATION (cont.)

The UCC3817 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous Unitrode PFC controllers improves noise immunity in the current amplifier. It also adds a phase inversion into the control loop. The UCC3817 takes advantage of this phase inversion to implement leading edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream DC to DC controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost, and reducing EMI. This is explained in greater detail in a following section. The UCC3817 current amplifier configuration is shown in Fig. 4.

Start Up Current

The UCC3818 version of the device is intended to have V_{CC} connected to a 12V supply voltage. The UCC3817 has an internal shunt regulator enabling the device to be powered from bootstrap circuitry as shown in the typical application circuit of Fig. 1. The current drawn by the UCC3817 during undervoltage lockout, or start up current, is typically 150µA. Once V_{CC} is above the UVLO threshold, the device is enabled and will draw 4mA typically. A resistor connected between the rectified AC line voltage and the VCC pin provides current to the shunt regulator during power up. Once the circuit is operational the bootstrap winding of the inductor will provide the V_{CC} voltage. Sizing of the startup resistor is determined by the startup time requirement of the system design.

$$I_{STARTUP} = C \bullet \frac{\Delta V}{\Delta t}$$

$$R = \frac{V_{RMS}}{I_{STARTUP}}$$

Where I is the startup current, C is the total capacitance at the VCC pin, V is the UVLO threshold and t is the allowed startup time.

Assuming a 1 second allowed startup time, a 16V UVLO threshold, and a total V_{CC} capacitance of 100µF, a resistor value of 75kΩ is required at a low line input voltage of $80V_{RMS}$. The IC start up current is sufficiently small as to be ignored in sizing the start up resistor.

Leading Edge Modulation

The UCC3817 uses leading edge modulation as opposed to traditional trailing edge modulation. Using leading edge modulation in a boost PFC front end being synchronized to a downstream buck converter using trailing edge modulation greatly diminishes the ripple current in the boost bulk capacitor. Refer to Fig. 5.

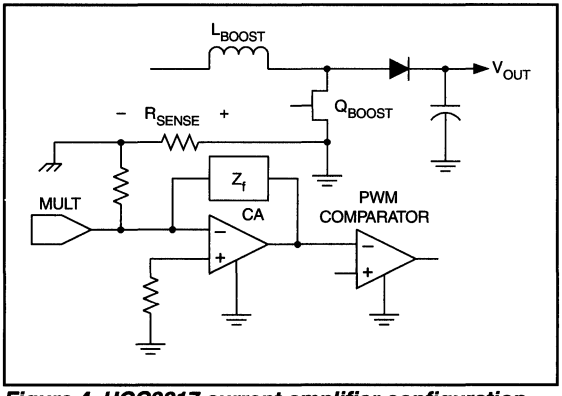


Figure 4. UCC3817 current amplifier configuration.

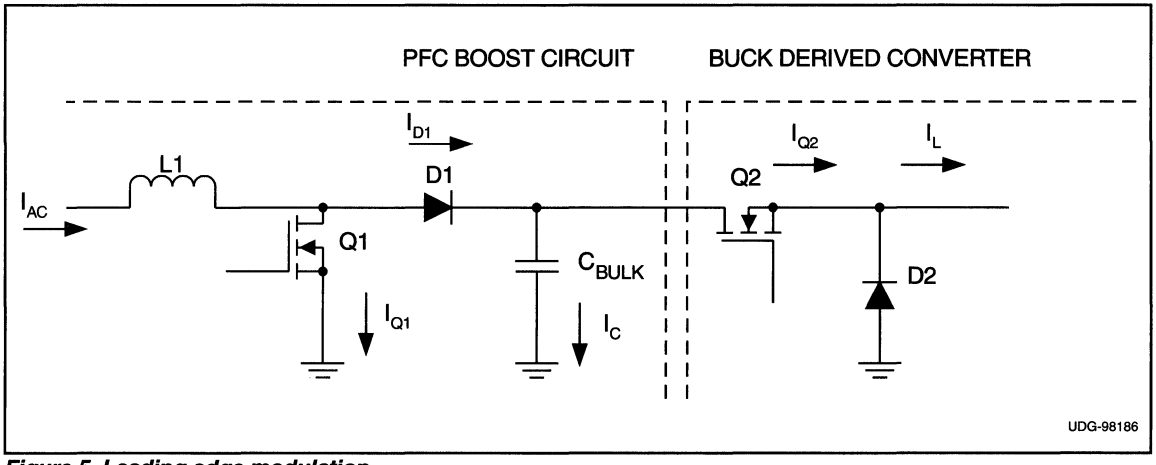


Figure 5. Leading edge modulation.

APPLICATION INFORMATION (cont.)

In a conventional synchronized system with both regulators utilizing trailing edge modulation, Q1 and Q2 would be turned on at the same time. All of the charging current for L1 would go to ground through Q1 and all of the output current would come from the bulk capacitor through Q2. Similarly, when both FETs are turned off, all the inductor current will flow into the bulk capacitor and all of the output current will be supplied by the freewheeling diode D2. By using leading edge modulation on the boost converter the FETs are turned on and off alternately. Refer to Fig. 6. When Q1 is off and Q2 is on, some of the output current is supplied through diode D1 by the boost inductor L1. When Q1 is on and Q2 off, the charge on the bulk capacitor is held up by the blocking action of Q2. It can be seen that the RMS current through the bulk capacitor is minimized when t1 and t3 are maximized with respect to t2 and t4. This greatly reduces the ripple current seen by the bulk capacitor, reducing stress and increasing reliability.

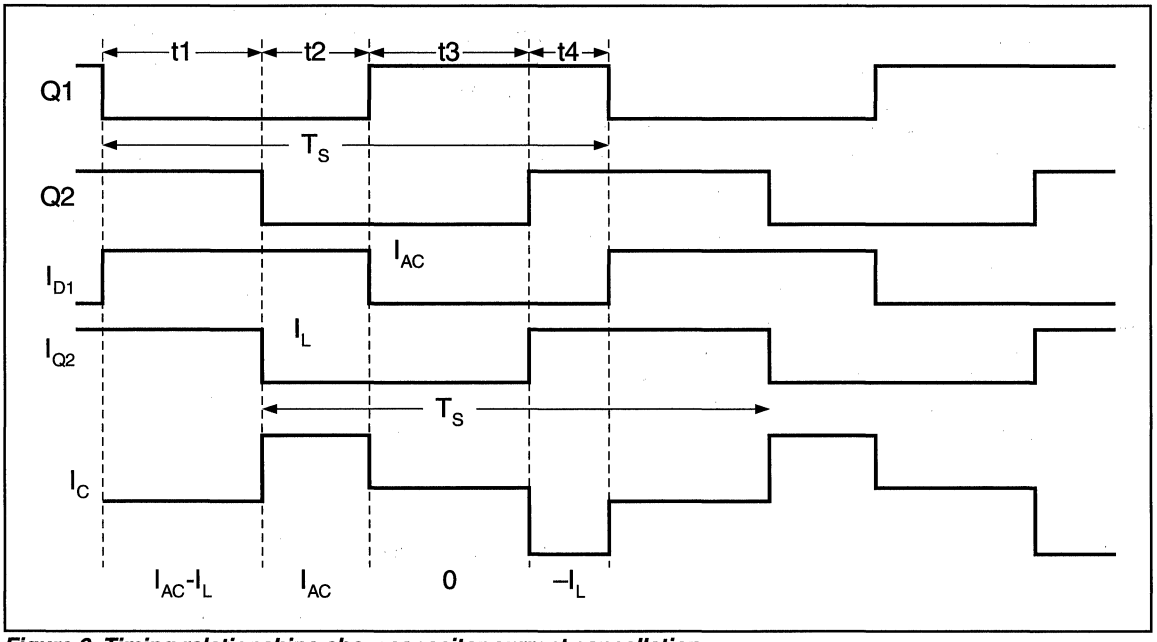


Figure 6. Timing relationships show capacitor current cancellation.

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FEATURES

- Combines PFC and 2nd Stage Down Converter Function
- Controls Boost PWM to near Unity Power Factor
- Accurate Power Limiting
- Average Current Mode Control in PFC Stage
- Peak Current Mode Control in Second Stage
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Programmable Oscillator
- Leading Edge/Trailing Edge Modulation for Reduced Output Ripple Using SmartSync™
- Low Startup Supply Current
- Synchronized Second Stage Start Up, with Programmable Soft Start
- Programmable Second Stage Shut Down

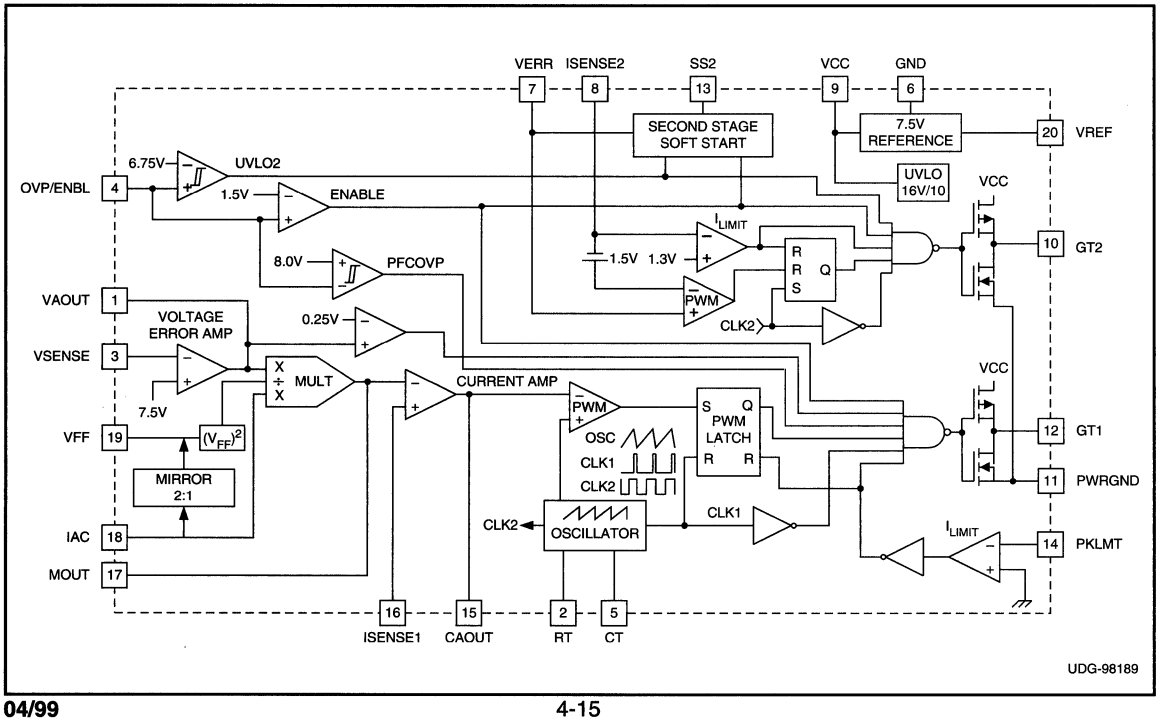
DESCRIPTION

The UCC18500 family provides all of the functions necessary for an active power factor corrected preregulator and a second stage forward converter. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage using average current mode control. The forward converter uses peak current mode control to perform the step down power conversion.

The PFC stage is leading edge modulation while the second stage is trailing edge synchronized to allow for minimum overlap between the boost and buck switches. This reduces ripple current in the bulk output capacitor.

In order to operate with a three to one range of input line voltages, a line feedforward (V_{FF}) in used to keep input power constant with varying input voltage. The multiplier then divides the line current by the square of the RMS value of the input line. Generation of V_{FF} is done using I_{AC} in conjunction with an external single pole filter. This not only reduces external parts count, but avoids the use of high voltage components offering a lower cost solution.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 18V
Gate Drive Current
  Continuous 0.2A
  50% Duty Cycle 1A
Input Voltage
  I_{SENSE1}, I_{SENSE2} MOUT, V_{SENSE}, OVP, ENBL. 11V
  PKLMT. 5V
Input Current, R_{SET}, I_{AC}, PKLMT, ENA 10mA
Power Dissipation 1W

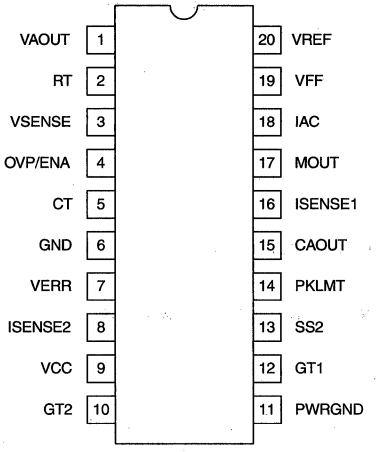
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

ORDERING INFORMATION

UCC □850□□
- PACKAGE
- PRODUCT OPTION
- TEMPERATURE RANGE

CONNECTION DIAGRAMS

DIL-20, SOIC-20 (TOP VIEW)
N, DW and J Packages



PACKAGE INFORMATION

	TEMPERATURE RANGE	PRODUCT OPTION UVLO	PRODUCT OPTION UVLO2 HYSTERESIS	PACKAGE
UCC18500	–55°C to +125°C	16	1.2	J-CDIP, N-PDIP, DW-SOIC
UCC18501		10.5	1.2	
UCC18502		16	3.0	
UCC18503		10.5	3.0	
UCC28500	–40°C to +85°C	16	1.2	N-PDIP, DW-SOIC
UCC28501		10.5	1.2	
UCC28502		16	3.0	
UCC28503		10.5	3.0	
UCC38500	0°C to +70°C	16	1.2	
UCC38501		10.5	1.2	
UCC38502		16	3.0	
UCC38503		10.5	3.0	

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3850X, –40°C to +85°C for the UCC2850X, and –55°C to +125°C for the UCC1850X, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Supply Current, Off	VCC = 12V		150	250	µA
Supply Current, On	VCC = 12V		4	6	mA
UVLO Section					
VCC Turn-On Threshold (UCCX8500/502)		15.4	16	16.6	V
UVLO Hysteresis (UCCX8500/502)		5.8	6	6.2	V
Shunt Voltage (UCCX8500/502)	I_{VCC} = 10mA		17	17.5	V
VCC Turn-On Threshold (UCCX8501/503)		10.2	10.5	10.8	V
UVLO Hysteresis (UCCX8501/503)		0.4	0.5	0.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3850X, –40°C to +85°C for the UCC2850X, and –55°C to +125°C for the UCC1850X, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Amplifier Section					
Input Voltage	T_A = 0°C to 70°C	7.388	7.500	7.613	V
	T_A = –40°C to 85°C	7.369	7.500	7.631	V
	T_A = –55°C to 125°C	7.313	7.5	7.687	V
V_{SENSE} Bias Current			50		nA
Open Loop Gain	V_{AOUT} = 2V to 5V		80		dB
V_{OUT} High	I_{LOAD} = –150µA	5.4	5.5	5.6	V
V_{OUT} Low	I_{LOAD} = 150µA		0.1	0.2	V
Over Voltage Protection and Enable Section					
Over Voltage Reference		7.8	8	8.2	V
Hysteresis		400	500	600	mV
Enable Threshold			1.5	2	V
Current Amplifier Section					
Input Offset Voltage	V_{CM} = 0V, V_{CAOUT} = 3V	–5	0	5	mV
Input Bias Current	V_{CM} = 0V, V_{CAOUT} = 3V		–50		nA
Input Offset Current	V_{CM} = 0V, V_{CAOUT} = 3V		25		nA
Open Loop Gain	V_{CM} = 0V, V_{CAOUT} = 2V to 5V		90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAOUT} = 3V		80		dB
V_{OUT} High	I_{LOAD} = –150µA		7		V
V_{OUT} Low	I_{LOAD} = 1mA		0.2		V
Gain Bandwidth Product		2.5	3.5		MHz
Voltage Reference Section					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.387	7.5	7.6	V
	Over Temperature (UCC3850X)	7.368	7.5	7.631	V
	Over Temperature (UCC2850X, UCC1850X)	7.313	7.5	7.687	V
Load Regulation	I_{REF} = 1mA to 2mA		5	10	mV
Line Regulation	VCC = 10.8V to 16V		10	20	mV
Short Circuit Current	V_{REF} = 0V		–35		mA
Oscillator Section					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	VCC = 10.8V to 15V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Peak Voltage		4.5	5	5.5	V
Ramp Amplitude Voltage (peak to peak)			4		V
Peak Current Limit Section					
PKLMT Reference Voltage		–15	0	15	mV
PKLMT Propogation Delay			500		ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, these specifications hold for T_A=0°C to 70°C for the UCC3850X, –40°C to +85°C for the UCC2850X, and –55°C to +125°C for the UCC1850X, $T_A = T_J$. V_{CC} = 12V, RT = 22k, CT = 330pF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier Section					
High Line, Low Power	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 1.25V		–6		µA
High Line, High Power	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 5V		–90		µA
Low Line, Low Power	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 1.25V		–19		µA
Low Line, High Power	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 5V		–300		µA
IAC Limited	I_{AC} = 150µA, V_{FF} = 1V, VA_{OUT} = 5V		–300		µA
Gain Constant (K)	I_{AC} = 300µA, V_{FF} = 2.8V, VA_{OUT} = 2.5V		1		1/V
Zero Current	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 0.25V	–5	0		µA
	I_{AC} = 500µA, V_{FF} = 4.7V, VA_{OUT} = 0.25V	–5	0		µA
Power Limit	I_{AC} = 150µA, V_{FF} = 1.4V, VA_{OUT} = 5V		–300		µA
Zero Power Section					
Zero Power Comparator Threshold	Measured on VAOUT		0.25	0.5	V
PFC Gate Driver Section					
GT1 Pull Up Resistance	I_{OUT} = –200mA		7		Ω
GT1 Pull Down Resistance	I_{OUT} = 100mA		3		Ω
GT1 Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
GT1 Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
Second Stage UVLO (UVLO2)					
PWM Turn-on Reference (UCCX8500/501)			6.75		V
Hysteresis (UCCX8500/501)			1.2		V
PWM Turn-on Reference (UCCX8502/503)			6.75		V
Hysteresis (UCCX8502/503)			3		V
Second Stage Soft Start Section					
SS2 Charge Current			–10		µA
SS2 Pulldown Current on VERR	VERR = 0.2V	2			mA
Second Stage Duty Cycle Clamp Section					
Maximum Duty Cycle		47		50	%
Second Stage Pulse by Pulse Current Sense Section					
Current Sense Comparator Threshold	VERR = 2.5V, Measured on ISENSE2		1		V
Second Stage Over Current Limit Section					
Peak Current Comparator Threshold			1.3		V
Input Bias Current			50		nA
Second Stage Gate Driver Section					
GT2 Pull Up Resistance	I_{OUT} = –200mA		7		Ω
GT2 Pull Down Resistance	I_{OUT} = 100mA		3		Ω
GT2 Output Rise Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns
GT2 Output Fall Time	C_{LOAD} = 1nF, R_{LOAD} = 10Ω		25		ns

Note 1: Guaranteed by design, not 100% tested in production.

PIN DESCRIPTIONS

CAOUT: (current amplifier out) This is the output of a wide bandwidth op amp that senses line current and commands the PFC pulse width modulator (PWM) to force the correct current. This output can swing close to gnd, allowing the PWM to force zero duty cycle when necessary.

CT: (Oscillator timing capacitor) A capacitor from CT to Gnd will set the oscillator frequency according to:

$$f = \frac{0.725}{(RT \bullet CT)}$$

GND: (ground) All voltages measured with respect to ground. VCC and VREF should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing to GND should be as short and direct as possible.

GT1: (gate drive) The output drive for the PFC stage is a totem pole MOSFET gate driver on GT1. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GT1 output driver that might cause the GT1 to overshoot excessively. Some overshoot of the GT1 output is always expected when driving a capacitive load.

GT2: (gate drive) Same as output GT1 for the second stage output drive. Limited to 50% maximum duty cycle.

IAC: (input ac current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to MOUT, so this is the only multiplier input which should be used for sensing instantaneous line voltage.

ISENSE1: (current sense) This is the inverting input to the current amplifier. This input and the non-inverting input MOUT remain functional down to and below GND.

ISENSE2: (current sense) A resistor from the source of the lower FET to ground generates the input signal for the peak limit control of the second stage. The oscillator ramp can also be summed into this pin.

MOUT: (multiplier output and current sense minus) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amp to reject ground noise. Multiplier output current is given by:

$$I_{MO} = \frac{(VAOUT - 1.0) \bullet I_{AC}}{K \bullet V_{FF}^{\,2}}$$

OVP/ENBL: (over voltage/enable) A window comparator input which will disable the PFC output driver if the boost output is 5% above nominal or will disable both the PFC and second stage output drivers and reset SS2 if pulled below 1.5V.

PKLMT: (PFC peak current limit) The threshold for pklimit is 0.0V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage corresponding to the desired overcurrent threshold across the current sense resistor.

PWRGND: Ground for totem pole output drivers.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10kΩ and 100kΩ is recommended.

SS2: (soft start for PWM) SS2 is at ground for either enable low or VCC below the UVLO threshold. When enabled, SS2 will charge an external capacitor with a current source. This voltage will be used as the voltage error signal during startup enabling the PWM duty cycle to increase slowly. In the event of a disable command or a VCC dropout, SS2 will quickly discharge to disable the PWM.

VAOUT: (voltage amplifier out) This is the output of the opamp that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20mA between 13V and 17V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate Gate Drive signals, the output devices will be inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

PIN DESCRIPTIONS

VERR: Voltage amp error signal for the second stage. The error signal is generated by an external amplifier which drives this pin.

VFF: (RMS feed forward signal) VFF signal generated at this pin by mirroring Iac into a single pole external filter.

$$R_{VFF} = \frac{VFF_{MAX}}{\sqrt{2} \bullet \frac{IAC_{MAX}}{2} \bullet 0.9}$$

VSENSE: (voltage amplifier inverting input) This is normally connected to a feedback network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when VCC is below the UVLO threshold. Bypass VREF to GND with a 0.1µF or larger ceramic capacitor for best stability.

APPLICATION INFORMATION

The UCC38500 is designed to incorporate all the control functions required for a power factor correction circuit and a second stage dc-dc converter. The PFC function is implemented as a full feature, average current mode controller Integrated Circuit for excellent performance. In addition, the input voltage feedforward function is implemented in a simplified manner. Current from IAC is mirrored over to the V_{FF} pin. By simply adding a resistor and capacitor (to attenuate 120Hz ripple) a voltage is developed which is proportional to line voltage. This eliminates several components normally connected to the line.

The UCC38500 uses leading edge modulation for the PFC stage and trailing edge modulation for the dc-dc stage. This reduces ripple current in the output capacitor by reducing the overlap in conduction time of the PFC and dc-dc switches. In addition to the reduced ripple current, noise immunity is improved through the current error amplifier implementation.

The UCC38500 is optimized to control a boost PFC stage operating in continuous conduction mode, followed by a dc-dc converter (typically a forward topology). It is usual that the dc-dc converter is transformer isolated and therefore its error amplifier will be located on the secondary side. The UCC38500 is configured without an internal error amplifier. The externally generated error signal is fed into the VERR pin.

The UCC38500 can be configured for voltage mode or current mode control of the second stage. The application figure shows a typical current mode configuration. For voltage mode control the ramp generated by CT is simply fed into the ISENSE2 pin.

One of the main system challenges in designing systems with a PFC front end is coordinating the turn-on and turn-off on the dc-dc converter. If the dc-dc converter is allowed to turn on before the boost converter is operational, it must operate at a much-reduced voltage and therefore can represent a large current draw to the boost converter. This start-up sequencing is handled internally by the UCC38500. The UCC38500 monitors the output voltage of the PFC converter and holds the dc-dc converter off until the output is within 10% of its regulation point. Once the trip point is reached the dc-dc section goes through a soft start sequence for a controlled, low stress start-up. Similarly if the output voltage drops too low (2 voltage options are available) the dc-dc converter shuts down thereby preventing overstress of the converter.

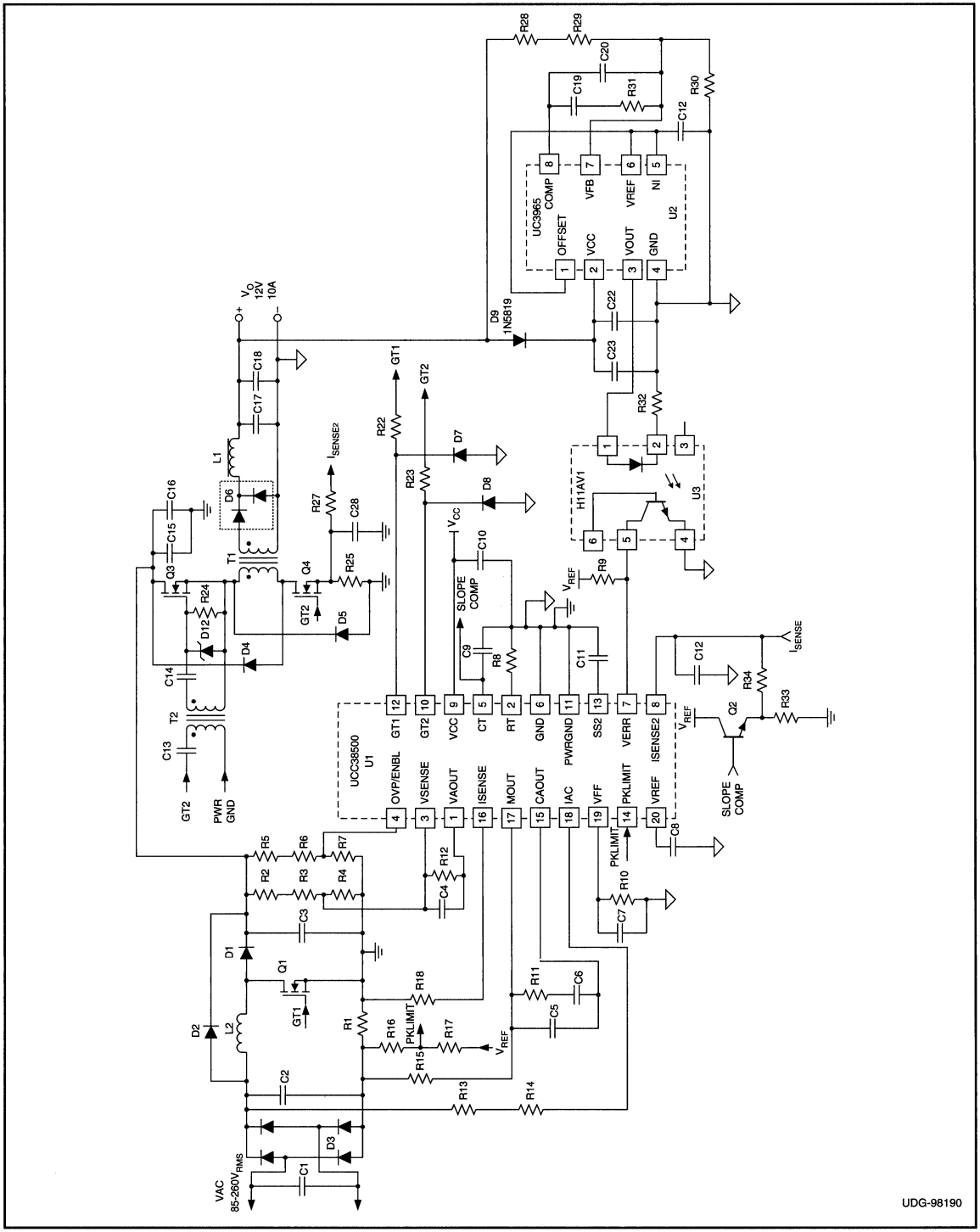
Design details of the PFC section can be found in several references shown below.

- UCC3817 data sheet
- High Power Factor Preregulator for Off-Line Power Supplies, SEM-800
- Optimizing the Design of a High Power Factor Switching Regulator, SEM-800

A design example for a 2 switch forward converter can be found in:

- 250W Off-Line Forward Converter Design Review, SEM-500

TYPICAL APPLICATION CIRCUIT



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application INFO available

UC1852
UC2852
UC3852

High Power-Factor Preregulator

FEATURES

- Low-Cost Power Factor Correction
- Power Factor Greater Than 0.99
- Few External Parts Required
- Controlled On-Time Boost PWM
- Zero-Current Switching
- Limited Peak Current
- Min and Max Frequency Limits
- Starting Current Less Than 1mA
- High-Current FET Drive Output
- Under-Voltage Lockout

DESCRIPTION

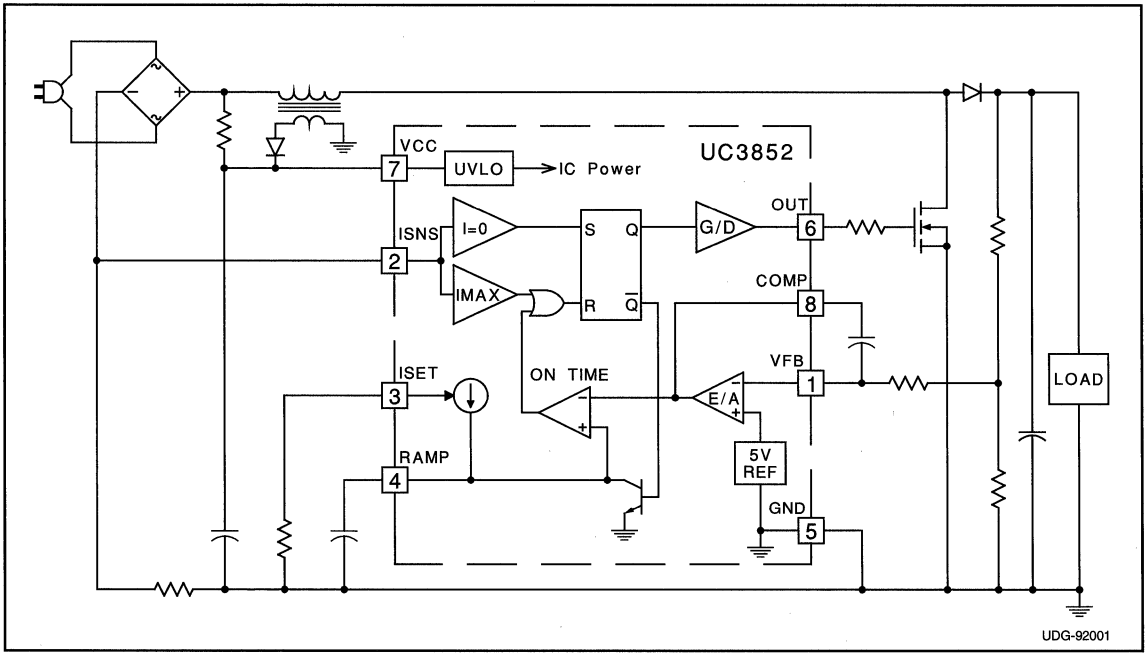
The UC1852 provides a low-cost solution to active power-factor correction (PFC) for systems that would otherwise draw high peak current pulses from AC power lines. This circuit implements zero-current switched boost conversion, producing sinusoidal input currents with a minimum of external components, while keeping peak current substantially below that of fully-discontinuous converters.

The UC1852 provides controlled switch on-time to regulate the output bulk DC voltage, an off-time defined by the boost inductor, and a zero-current sensing circuit to reactivate the switch cycle. Even though switching frequency varies with both load and instantaneous line voltage, it can be maintained within a reasonable range to minimize noise generation.

While allowing higher peak switch currents than continuous PFCs such as the UC1854, this device offers less external circuitry and smaller inductors, yet better performance and easier line-noise filtering than discontinuous current PFCs with no sacrifice in complexity or cost. The ability to obtain a power factor in excess of 0.99 makes the UC1852 an optimum choice for low-cost applications in the 50 to 500 watt power range. Protection features of these devices include under-voltage lockout, output clamping, peak-current limiting, and maximum-frequency clamping.

The UC1852 family is available in 8-pin plastic and ceramic dual in-line packages, and in the 8-pin small outline IC package (SOIC). The UC1852 is specified for operation from -55°C to +125°C, the UC2852 is specified for operation from -40°C to +85°C, and the UC3852 is specified for operation from 0°C to +70°C.

TYPICAL APPLICATION

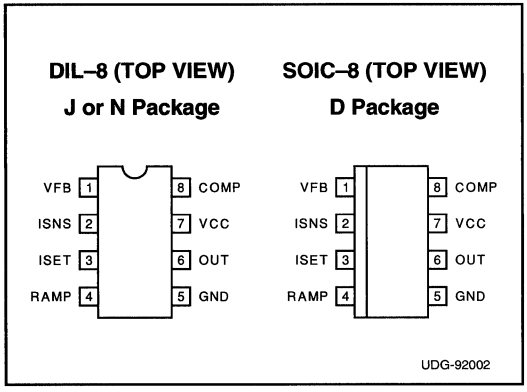


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low-impedance Source) 30.0V
Supply Current (High-impedance Source) 30.0mA
OUT Current, Peak ..... ±1.0A
OUT Energy, Capacitive Load 5.0µJ
Input Voltage, ISNS ..... ±5.0V
Input Voltage, VFB ..... –0.3V to +10.0V
COMP Current ..... ±10.0mA
ISET Current ..... –10.0mA
Power Dissipation at Ta≤25°C (Note 3) 1.0W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

Note 1: All voltages with respect to GND (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: Refers to DIL-8 Package. Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

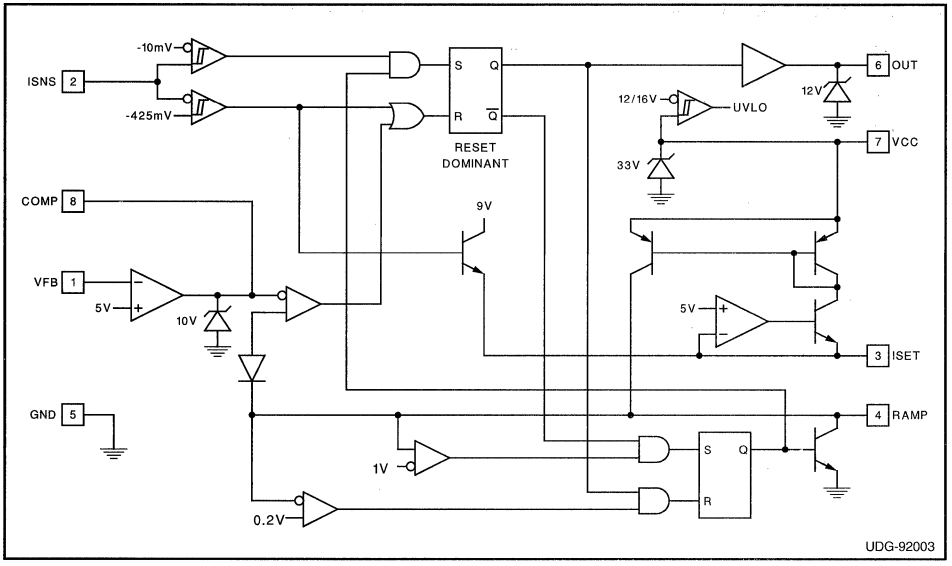


ELECTRICAL CHARACTERISTICS

Unless otherwise stated, VCC=24V, ISET=50kΩ to GND, RAMP=1nF to GND, ISNS= –0.1V, VFB connected to COMP, no load on OUT, –55°C<Ta<+125°C for the UC1852, –40°C<Ta<+85°C for the UC2852, and 0°C<Ta<+70°C for the UC3852, and Ta=Tj.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Timer Section					
ISET Voltage		4.5	5.0	5.5	V
RAMP Charge Current	RAMP=2.5V	88	98	108	µA
RAMP Discharge Current	ISNS= –1.0V, RAMP=1.0V	12	28	50	mA
RAMP Saturation Voltage	ISNS= –1.0V, I_{RAMP}=100µA		0.006	0.200	V
RAMP Threshold - Maximum Frequency	VFB=10V, COMP open	0.92	1.02	1.12	V
RAMP Threshold - PWM Comparator		3.9	4.3	4.8	V
Current Sense Comparator					
ISNS Restart Threshold		–18	–10	–4	mV
ISNS Fault Threshold		–550	–450	–350	mV
ISNS Input Current		–100	–30	100	µA
Error Amplifier Section					
VFB Input Voltage		4.6	5.0	5.3	V
VFB Input Bias Current		–5.00	–0.03	5.00	µA
COMP Sink Current	COMP=7.5V	10			mA
COMP Source Current	COMP=2.5V	–300	–175	–100	µA
COMP Clamp Voltage	VFB=0.0V, COMP open	9.2	10.0	10.6	V
OUT Output					
OUT Saturation Voltage High	VCC=13V, I_{OUT}= –200mA, RAMP=2V	0.5	1.7	2.5	V
OUT Saturation Voltage Low	I_{OUT}=200mA, ISNS= –1.0V	0.5	1.6	2.2	V
OUT Saturation Voltage Low @ 10mA	I_{OUT}=10mA, ISNS= –1.0V		0.05	0.40	V
OUT Clamp Voltage	I_{OUT}= –200mA, RAMP=2V	10.0	12.0	14.5	V
OUT Voltage during UVLO	I_{OUT}=100mA, VCC=0V	0.5	1.0	2.2	V
Overall Section					
Inactive Supply Current	VCC=10V	0.2	0.4	1.0	mA
Active Supply Current		3.0	6.0	10.0	mA
VCC Clamp Voltage	ICC=25mA	30	33	36	V
VCC Turn-On Threshold		14.5	16.3	17.5	V
VCC Turn-Off Threshold		10.5	11.5	13.0	V
VCC Threshold Hysteresis		3	5	7	V

DETAILED BLOCK DIAGRAM



PIN DESCRIPTIONS

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. To limit PWM on-time, this pin is clamped to approximately 10V. To implement soft start, the COMP pin can be pulled low and ramped up with a PNP transistor, a capacitor, and a resistor.

GND: Ground for all functions is through this pin.

ISET: The dominant function is of this pin is to program RAMP charging current. RAMP charging current is approximately 5V divided by the external resistor placed from ISET to ground. Resistors in the range of 10kΩ to 50kΩ are recommended, producing currents in the range of 100μA to 500μA.

A second function of ISET is as reference output. The ISET pin is normally regulated to 5V ±10%. It is critical that this pin only see the loading of the RAMP programming resistor, but a high input-impedance comparator or amplifier may be connected to this pin or to a tap on the RAMP programming resistor if required.

The third function of the ISET pin is as a FAULT output. In the event of an over-current fault, the ISET pin is forced to approximately 9V by the fault comparator. This can be used to trip an external protection circuit which can disable the load or start a fault restart cycle.

ISNS: This input to the zero and over current comparators is specially built to allow operation over a ±5V dynamic range. In noisy systems or systems with very high Q inductors, it is desirable to filter the signal entering the ISNS input to prevent premature restart or fault cycles. For best accuracy, ISNS should be connected to a current sense resistor through no more than 200 ohms.

OUT: The output of a high-current power driver capable of driving the gate of a power MOSFET with peak currents exceeding ±500mA. To prevent damage to the power MOSFET, the OUT pin is internally driven by a 12V supply. However, lead inductance between the OUT pin and the load can cause overshoot and ringing. External current boost transistors will increase this overshoot and ringing. If there is any significant distance between the IC and the MOSFET, external clamp diodes and/or series damping resistors may be required. OUT is actively held low when the VCC is below the UVLO threshold.

RAMP: A controlled on-time PWM requires a timer whose time can be modulated by an external voltage. The timer current is programmed by a resistor from ISET to GND. A capacitor from RAMP to GND sets the on time in conjunction with the voltage on COMP. Recommended values for the timer capacitors are between 100pF and 1nF.

VCC: VCC is the logic and control power connection for this device. VCC current is the sum of active device supply current and the average OUT current. Knowing the maximum operating frequency and the MOSFET gate charge (Qg), average OUT current can be estimated by:

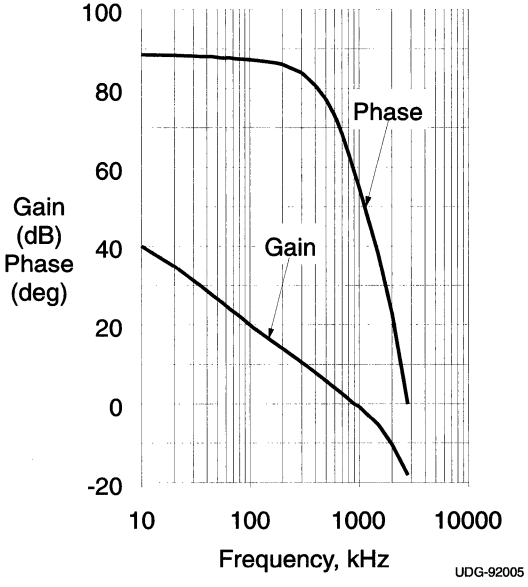
$$I_{OUT} = Q_g \times F$$

To prevent noise problems, bypass VCC to GND with both a ceramic and an electrolytic capacitor.

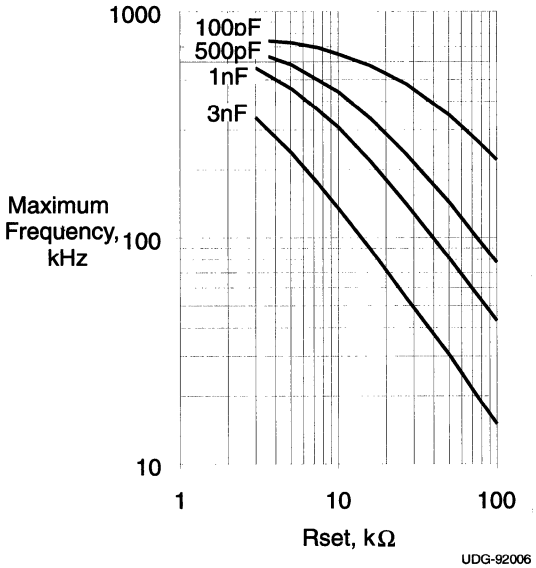
VFB: VFB is the error amplifier inverting input. This input serves as both the voltage sense input to the error amplifier

TYPICAL CHARACTERISTICS

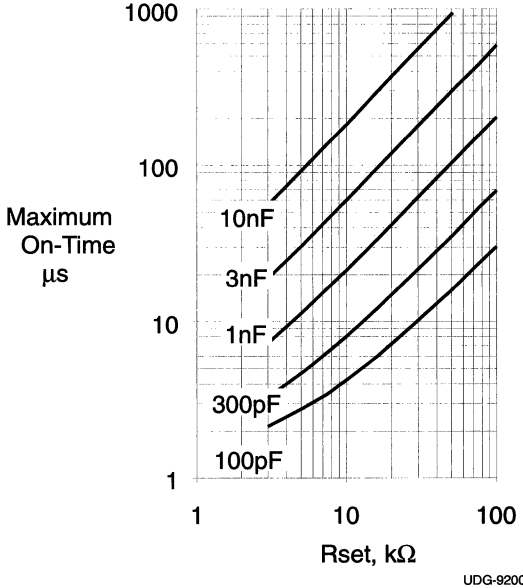
Error Amplifier Gain an Pase



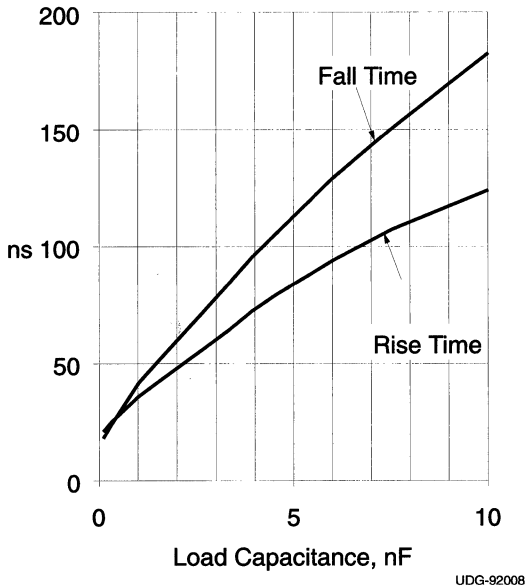
Ma Freuenc vs. Rset an Ct



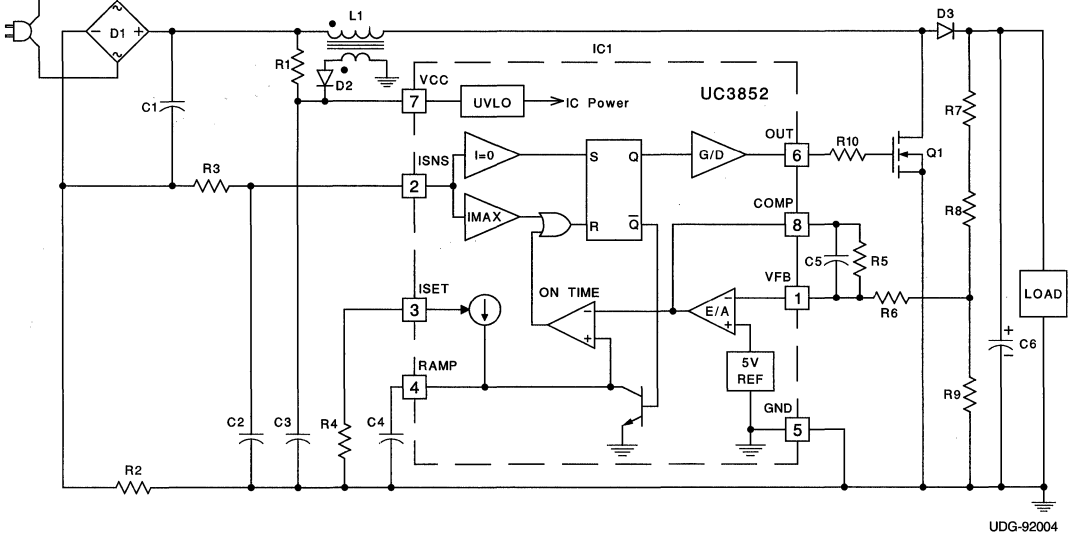
Ma OnT ime vs. Rset an Ct



OUT Rise an Fall T ime



APPLICATION INFORMATION: A 100 Watt Power Factor Preregulator



This circuit demonstrates a complete power factor preregulator based on the UC3852. This preregulator will supply up to 100 watts at 400VDC and exhibit power factor greater than 0.995 with less than 10% total harmonic distortion. Operating input range is 90V to 160V RMS at 50Hz to 60Hz.

This design is intentionally simple, yet fully functional. The UC3852 can also be used in designs featuring soft start, over-voltage protection, wide power-line voltage operation, and fault latching. For more information on applying the UC3852, refer to Unitrode Application Note U–132.

PARTS LIST

C1	0.47µF/250VAC X2 Class Polyester
C2	1nF/16V Ceramic
C3	68µF/35V Aluminum Electrolytic
C4	180pF/16V Ceramic
C5	0.1µF/16V Polyester or Ceramic
C6	82µF/450V Aluminum Electrolytic
D1	2A/500V Bridge Rectifier (Collmer KBPC106 or Powertex MB11A02V60)
D2	100mA/50V Switching Diode (1N4148)
D3	2A/500V 250ns Recovery-Time Rectifier (Motorola MR856)
IC1	UC3852N Power Factor Controller IC
Q1	IRF830 4.5A/500V 1.5Ω Power FET
L1	680µH (Renco RL3792 with 10 Turn 24 AWG Secondary)
R1	150kΩ, ¼W
R2	0.2Ω, ½W Carbon Composition
R3	10Ω, ¼W
R4	13.3kΩ, ¼W
R5	1MΩ, ¼W
R6	20kΩ, ¼W
R7	200kΩ, ½W
R8	200kΩ, ½W

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application INFO available

UC1853
UC2853
UC3853

High Power Factor Preregulator

FEATURES

- Complete 8-pin Power Factor Solution
- Reduced External Components
- RMS Line Voltage Compensation
- Precision Multiplier/Squarer/Divider
- Internal 75kHz Synchronizable Oscillator
- Average Current Mode PWM Control
- Overvoltage Protection Comparator
- High Current, Clamped Gate Driver

DESCRIPTION

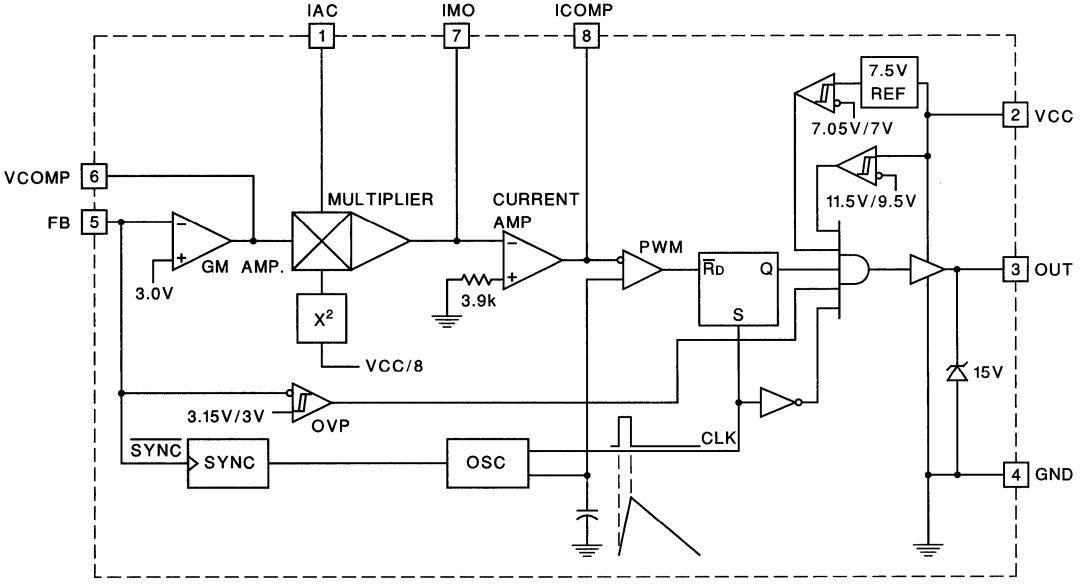
The UC3853 provides simple, yet high performance active power factor correction. Using the same control technique as the UC1854, this 8-pin device exploits a simplified architecture and an internal oscillator to minimize external component count. The UC3853 incorporates a precision multiplier/squarer/divider circuit, voltage and current loop error amplifiers, and a precision voltage reference to implement average current mode control with RMS line voltage compensation. This control technique maintains constant loop gain with changes in input voltage, which minimizes input line current distortion over the worldwide input voltage range.

The internal 75kHz oscillator includes an external clock input, allowing synchronization to downstream converters. Additionally, the device features an overvoltage protection comparator, a clamped MOSFET gate driver which self-biases low during undervoltage lockout, and low startup and supply current.

These devices are available in 8-pin plastic and ceramic dual in-line (DIP) packages, and 8-lead small outline (SOIC) packages. The UC1853 is specified for operation from –55°C to +125°C, the UC2853 is specified for operation from –25°C to +85°C, and the UC3853 is specified for operation from 0°C to +70°C.

4

BLOCK DIAGRAM



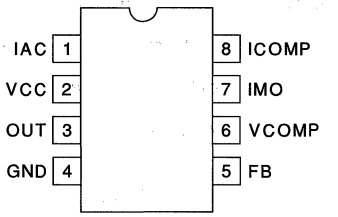
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) 40V
Output Drive Current,
  Continuous 0.125A
  Peak 0.5A
Output Minimum Voltage . . . . . –0.3V
IAC Maximum Input Current 1mA
IMO Maximum Output Current . . . . . –2mA
IMO Minimum Voltage . . . . . –0.3V
FB Maximum Input Voltage 5V
VCOMP Maximum Voltage 6.2V
ICOMP Sourcing Current . . . . . Self-Limiting
ICOMP Sinking Current 20mA
ICOMP Maximum Voltage 7.2V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, I_{AC} = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
VCC Turn-on Threshold	V_{VCOMP}, V_{ICOMP} Open		11.5	13	V
Hysteresis		1.5	1.8	2.1	V
Supply Current Section					
I_{VCC} Startup	V_{CC} = 8V, IAC = 100µA; V_{VCOMP}, V_{ICOMP} Open		250	500	µA
I_{VCC}	IAC = 0µA, V_{ICOMP} = 0V		10	15	mA
Voltage Loop Error Amplifier Section					
Transconductance	IOUT = ± 20µA 0-70C	300	450	575	µmho
	Temperature	135		640	µmho
Input Voltage	0-70C	2.925	3	3.075	V
	Temperature	2.9		3.1	V
AVOL	V_{VCOMP} = 1V – 4V	50	60		dB
Output Sink Current	V_{FB} = 3.2V, V_{VCOMP} = 3.75V	20	50		µA
Output Source Current	V_{FB} = 2.8V, V_{VCOMP} = 3.75V		–50	–20	µA
Output Voltage High		5.5	6		V
Output Voltage Low			0.6	0.9	V
Current Loop Error Amplifier Section					
Offset Voltage		0		6	mV
Voltage Gain	V_{ICOMP} = 1V – 4V		70		dB
Sink Current	V_{IMO} = 100mV, V_{ICOMP} = 3V	1			mA
Source Current	V_{IMO} = –0.1V, V_{ICOMP} = 3V		–150	–80	µA
Output High	I_{ICOMP} = –50mA	6	6.8		V
Output Low	I_{ICOMP} = 50µA		0.3	0.8	V
PWM Modulator Gain	V_{ICOMP} = 2V – 3V (Note 1)		20		%/V

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these parameters apply for T_A = –55°C to +125°C for the UC1853; –25°C to +85°C for the 2853; and 0°C to +70°C for the UC3853; VCC = 16V, V_{FB} = 3V, I_{AC} = 100µA, V_{VCOMP} = 3.75V, V_{ICOMP} = 3V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Multiplier Section					
Output Current – IAC Limited	VCC = 11V, V_{VCOMP} = 6V	–230	–200	–170	µA
Output Current – Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current – Power Limited	VCC = 12V, V_{VCOMP} = 5.5V	–236	–178	–168	µA
Output Current	VCC= 12V, V_{VCOMP} = 2V		–22		µA
	VCC= 12V, V_{VCOMP} = 5V		–156		µA
	VCC= 40V, V_{VCOMP} = 2V		–2		µA
	VCC= 40V, V_{VCOMP} = 5V		–14		µA
Multiplier Gain Constant	VCC= 12V, V_{VCOMP} = 5.5V (Note 2)	–1.05	–0.9	–0.75	V^{-1}
Oscillator Section					
Oscillator Initial Frequency	T_A = 25°C	67.5	75	82.5	kHz
Oscillator Frequency	Line, Load, Temperature	56	75	94	kHz
Synchronization Frequency Range				100	kHz
Synchronization Pulse Amplitude	Pulse slew rate = 100V/µsec (Note 3)		2		V
Output Driver Section					
Maximum Output Voltage	0mA load, VCC = 20V	12	15	17.5	V
Output High	0mA load, VCC = 12V, ref. to VCC	–2.7	–1.7		V
	–50mA load, VCC = 12V, ref. to VCC	–3	–2.2		V
Output Low (Device Inactive)	Vcc = 0V, 20mA load (Sinking)		0.9	2.0	V
Output Low (Device Active)	50mA load (Sinking)		0.5	1	V
OUT Rise Time	1nF from OUT to GND		55	100	ns
OUT Fall Time	1nF from OUT to GND		35	100	ns
OUT Maximum Duty Cycle	V_{ICOMP} = 0V	88	93		%
OVP Comparator Section					
Threshold Voltage	Volts Above EA Input V	90	150		mV
Hysteresis			80		mV

Note 1:

$$PWM\ modulator\ gain = \frac{\Delta DutyCycle}{\Delta V_{ICOMP}}$$

Note 2:

$$Gain\ constant\ (K) = \frac{IAC \bullet (VCOMP - 1.5V)}{IMO \bullet VCC \bullet \frac{VCC}{64}},\ VCC = 12V.$$

Note 3.
Synchronization is accomplished with a falling edge of 2V magnitude and 100V/µsec slew rate.

PIN DESCRIPTIONS

FB: Voltage Amplifier Inverting Input, Overvoltage Comparator Input, Sync Input. This pin serves three functions. FB accepts a fraction of the power factor corrected output voltage through a voltage divider, and is nominally regulated to 3V. FB voltages 5% greater than nominal will trip the overvoltage comparator, and shut down the output stage until the output voltage drops 5%. The internal oscillator can be synchronized through FB by injecting a 2V clock signal though a capacitor. To prevent false tripping of the overvoltage comparator, the clock signal must have a fast falling edge, but a slow rising edge. See Application Note U-159 for more information.

GND: Ground. All voltages are measured with respect to GND. The VCC bypass capacitor should be connected to ground as close to the GND pin as possible.

IAC: AC Waveform Input. This input provides voltage waveform information to the multiplier. The current loop will try to produce a current waveform with the same shape as the IAC signal. IAC is a low impedance input, nominally at 2V, which accepts a current proportional to the input voltage. Connect a resistor from the rectified input line to IAC which will conduct 500mA at maximum line voltage.

IMO: Multiplier Output and Current Sense Inverting Input. The output of the multiplier and the inverting input of the current amplifier are connected together at IMO. Avoid bringing this input below –0.5V to prevent the internal protection diode from conducting. The multiplier output is a current, making this a summing node and allowing a differential current error amplifier configuration to reject ground noise. The input resistance at this node should be 3.9k to minimize input bias current induced offset voltage. See the Applications section for the recommended circuit configuration.

OUT: Gate Driver Output. OUT provides high current gate drive for the external power MOSFET. A 15V clamp prevents excessive MOSFET gate-to-source voltage so that the UC3853 can be operated with VCC and high as 40V. A series gate resistor of at least 5 ohms should be used to minimize clamp voltage overshoot. In addition, a Schottky diode such as a 1N5818 connected between OUT and GND may be necessary to prevent parasitic substrate diode conduction.

ICOMP: Current Loop Error Amplifier Output. The current loop error amplifier is a conventional operational amplifier with a 150µA current source class A output stage. Compensate the current loop by placing an impedance between ICOMP and IMO. This output can swing above the oscillator peak voltage, allowing zero duty cycle when necessary.

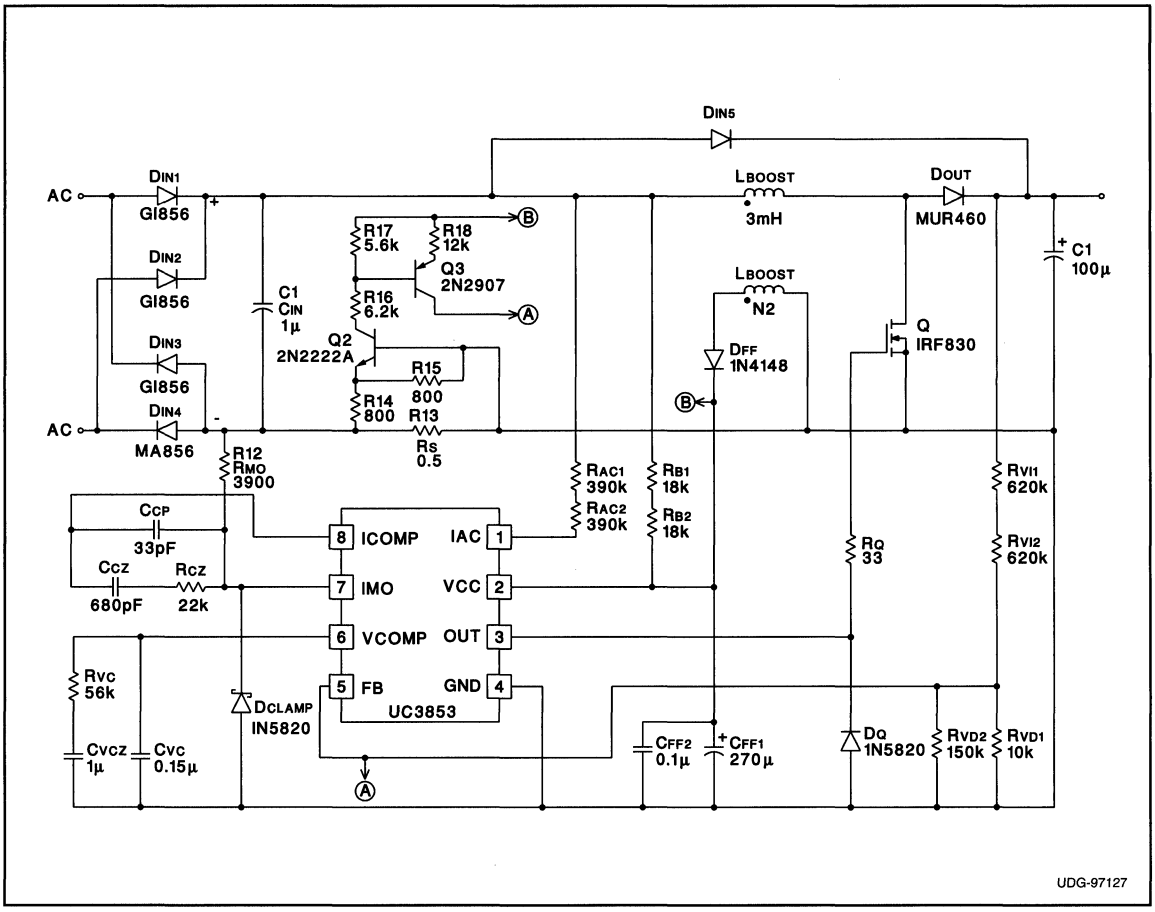
VCC: Input Supply Voltage. This pin serves two functions. It supplies power to the chip, and an input voltage level signal to the squarer circuit. When this input is connected to a DC voltage proportional to the AC input RMS voltage, the voltage loop gain is reduced by

$$\frac{64}{Vcc^2}.$$

This configuration maintains constant loop gain. The UC3853 input voltage range extends from 12V to 40V, allowing an AC supply voltage range in excess of 85VAC to 265VAC. Bypass VCC with at least a 0.1µF ceramic capacitor to ensure proper operation. See the Applications section for the recommended circuit configuration.

VCOMP: Voltage Loop Error Amplifier Output. The voltage loop error amplifier is a transconductance type operational amplifier. A feedback impedance between VCOMP and FB for loop compensation must be avoided to maintain proper operation of the overvoltage protection comparator. Instead, compensate the voltage loop with an impedance between VCOMP and GND. When VCOMP is below 1.5V, the multiplier output current is zero.

UC3853 TYPICAL APPLICATION



Note: the application circuit shown is a 100W, 75KHz design. Additional application information can be found in Application Note U–159 and Design Note DN–78.

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application INFO available

UC1854
UC2854
UC3854

High Power Factor Preregulator

FEATURES

- Control Boost PWM to 0.99 Power Factor
- Limit Line Current Distortion To <5%
- World-Wide Operation Without Switches
- Feed-Forward Line Regulation
- Average Current-Mode Control
- Low Noise Sensitivity
- Low Start-Up Supply Current
- Fixed-Frequency PWM Drive
- Low-Offset Analog Multiplier/Divider
- 1A Totem-Pole Gate Driver
- Precision Voltage Reference

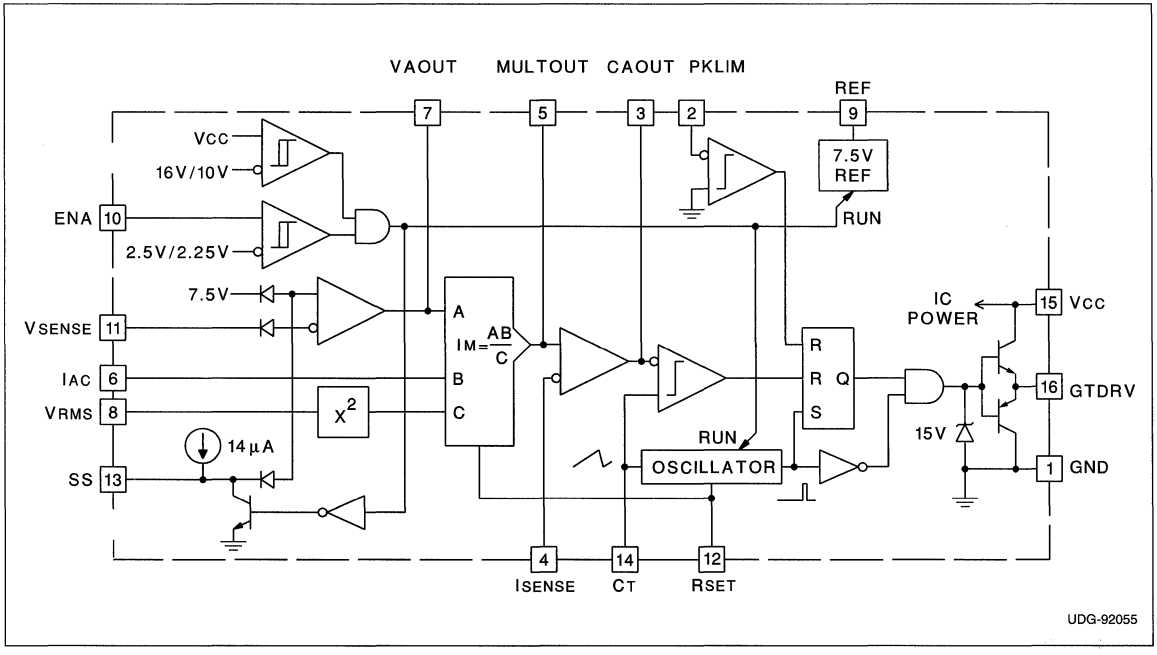
DESCRIPTION

The UC1854 provides active power factor correction for power systems that otherwise would draw non-sinusoidal current from sinusoidal power lines. This device implements all the control functions necessary to build a power supply capable of optimally using available power-line current while minimizing line-current distortion. To do this, the UC1854 contains a voltage amplifier, an analog multiplier/divider, a current amplifier, and a fixed-frequency PWM. In addition, the UC1854 contains a power MOSFET compatible gate driver, 7.5V reference, line anticipator, load-enable comparator, low-supply detector, and over-current comparator.

The UC1854 uses average current-mode control to accomplish fixed-frequency current control with stability and low distortion. Unlike peak current-mode, average current control accurately maintains sinusoidal line current without slope compensation and with minimal response to noise transients.

The UC1854's high reference voltage and high oscillator amplitude minimize noise sensitivity while fast PWM elements permit chopping frequencies above 200kHz. The UC1854 can be used in single and three phase systems with line voltages that vary from 75 to 275 volts and line frequencies across the 50Hz to 400Hz range. To reduce the burden on the circuitry that supplies power to this device, the UC1854 features low starting supply current.

BLOCK DIAGRAM

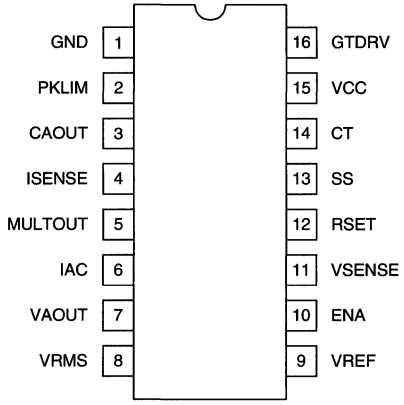


ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC 35V
GTDRV Current, Continuous 0.5A
GTDRV Current, 50% Duty Cycle 1.5A
Input Voltage, V_{SENSE}, V_{RMS} 11V
Input Voltage, I_{SENSE}, MULTOUT 11V
Input Voltage, PKLIM 5V
Input Current, R_{SET}, I_{AC}, PKLIM, ENA 10mA
Power Dissipation 1W
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... +300°C

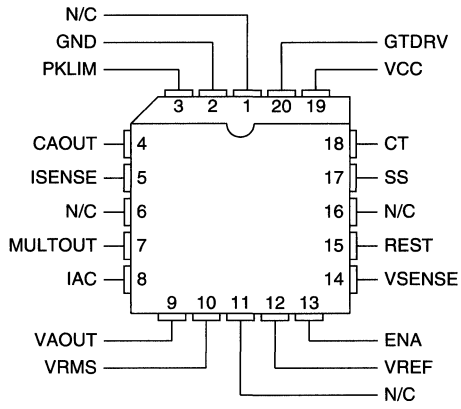
Note 1: All voltages with respect to GND (Pin 1).
Note 2: All currents are positive into the specified terminal.
Note 3: ENA input is internally clamped to approximately 14V.
Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

DIL–16 & SOIC-16 (Top View)
J, N & DW Packages



CONNECTION DIAGRAMS

PLCC-20 & LCC-20 (Top View)
Q & L Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLIM=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GTDRV, –55°C<T_A<125°C for the UC1854, –40°C<T_A<85°C for the UC2854, and 0°C<T_A<70°C for the UC3854, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	ENA=0V		1.5	2.0	mA
Supply Current, On			10	16	mA
V_{CC} Turn-On Threshold		14.5	16	17.5	V
V_{CC} Turn-Off Threshold		9	10	11	V
ENA Threshold, Rising		2.4	2.55	2.7	V
ENA Threshold Hysteresis		0.2	0.25	0.3	V
ENA Input Current	ENA=0V	–5.0	–0.2	5.0	µA
V_{RMS} Input Current	V_{RMS}=5V	–1.0	–.01	1.0	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLIM=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GTDRV, $-55^{\circ}C<T_A<125^{\circ}C$ for the UC1854, $-40^{\circ}C<T_A<85^{\circ}C$ for the UC2854, and $0^{\circ}C<T_A<70^{\circ}C$ for the UC3854, and $T_A=T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE AMPLIFIER					
Voltage Amp Offset Voltage	VA Out=5V	–8		8	mV
V_{SENSE} Bias Current		–500	–25	500	nA
Voltage Amp Gain		70	100		dB
Voltage Amp Output Swing			0.5 to 5.8		V
Voltage Amp Short Circuit Current	VA Out=0V	–36	–20	–5	mA
SS Current	SS=2.5V	–20	–14	–6	µA
CURRENT AMPLIFIER					
Current Amp Offset Voltage		–4		4	mV
I_{SENSE} Bias Current		–500	–120	500	nA
Input Range, I_{SENSE}, Mult Out		–0.3 to 2.5			V
Current Amp Gain		80	110		dB
Current Amp Output Swing			0.5 to 16		V
Current Amp Short Circuit Current	CA Out=0V	–36	–20	–5	mA
Current Amp Gain-BW Product	$T_A=25^{\circ}C$ (Note 6)	400	800		kHz
REFERENCE					
Reference Output Voltage	I_{REF}=0mA, $T_A=25^{\circ}C$	7.4	7.5	7.6	V
	I_{REF}=0mA, Over Temp.	7.35	7.5	7.65	V
V_{REF} Load Regulation	$-10mA<I_{REF}<0mA$	–15	5	15	mV
V_{REF} Line Regulation	$15V<V_{CC}<35V$	–10	2	10	mV
V_{REF} Short Circuit Current	REF=0V	–50	–28	–12	mA
MULTIPLIER					
Mult Out Current I_{AC} Limited	I_{AC}=100µA, R_{SET}=10k, V_{RMS}=1.25V	–220	–200	–180	µA
Mult Out Current Zero	I_{AC}=0µA, R_{SET}=15k	–2.0	–0.2	2.0	µA
Mult Out Current R_{SET} Limited	I_{AC}=450µA, R_{SET}=15k, V_{RMS}=1V, VA Out = 6V	–280	–255	–220	µA
Mult Out Current	I_{AC}=50µA, V_{RMS}=2V, VA=4V	–50	–42	–33	µA
	I_{AC}=100µA, V_{RMS}=2V, VA=2V	–38	–27	–12	µA
	I_{AC}=200µA, V_{RMS}=2V, VA=4V	–165	–150	–105	µA
	I_{AC}=300µA, V_{RMS}=1V, VA=2V	–250	–225	–150	µA
	I_{AC}=100µA, V_{RMS}=1V, VA=2V	–95	–80	–60	µA
Multiplier Gain Constant	(Note 5)		–1.0		V
OSCILLATOR					
Oscillator Frequency	R_{SET}=15k	46	55	62	kHz
	R_{SET}=8.2k	86	102	118	kHz
C_T Ramp Peak-to-Valley Amplitude		4.9	5.4	5.9	V
C_T Ramp Valley Voltage		0.8	1.1	1.3	V

Note 5: Multiplier Gain Constant (k) is defined by: $I_{MULTOUT} = \dfrac{k \times I_{AC} \times (VAOUT - 1)}{V_{RMS}^2}$

Note 6: Guaranteed by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC}=18V, R_{SET}=15k to ground, C_T=1.5nF to ground, PKLIM=1V, ENA=7.5V, V_{RMS}=1.5V, I_{AC}=100µA, I_{SENSE}=0V, CA Out=3.5V, VA Out=5V, V_{SENSE}=7.5V, no load on SS, CA Out, VA Out, REF, GTDRV, –55°C<T_A<125°C for the UC1854, –40°C<T_A<85°C for the UC2854, and 0°C<T_A<70°C for the UC3854, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER					
Maximum GTDRV Output Voltage	0mA load on GTDRV, 18V<V_{CC}<35V	13	14.5	18	V
GTDRV Output Voltage High	–200mA load on GTDRV, V_{CC}=15V	12	12.8		V
GTDRV Output Voltage Low, Off	V_{CC}=0V, 50mA load on GTDRV		0.9	1.5	V
GTDRV Output Voltage Low	200mA load on GTDRV		1.0	2.2	V
	10mA load on GTDRV		0.1	0.4	V
Peak GTDRV Current	10nF from GTDRV to GND		1.0		A
GTDRV Rise/Fall Time	1nF from GTDRV to GND		35		ns
GTDRV Maximum Duty Cycle	$V_{CA\ Out}$=7V		95		%
CURRENT LIMIT					
PKLIM Offset Voltage		–10		10	mV
PKLIM Input Current	PKLIM=–0.1V	–200	–100		µA
PKLIM to GTDRV Delay	PKLIM falling from 50mV to –50mV		175		ns

Note 5: Multiplier Gain Constant (k) is defined by: $I_{MULTOUT} = \frac{k \times I_{AC} \times (VAOUT - 1)}{V_{RMS}^2}$

Note 6: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CAOUT: Current Amplifier Output. This is the output of a wide-bandwidth op amp that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary. The current amplifier will remain active even if the IC is disabled. The current amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

CT: Oscillator Timing Capacitor. A capacitor from CT to GND will set the PWM oscillator frequency according to this relationship:

$$F = \frac{1.25}{R_{SET} \times C_T}$$

ENA: Enable. ENA is a logic input that will enable the PWM output, voltage reference, and oscillator. ENA also will release the soft start clamp, allowing SS to rise. When unused, connect ENA to a +5V supply or pull ENA high with a 22k resistor. The ENA pin is not intended to be used as a high speed shutdown to the PWM output.

GND: Ground. All voltages are measured with respect to GND. V_{CC} and REF should be bypassed directly to GND with an 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from the oscillator timing capacitor to GND should also be as short and as direct as possible.

GTDRV Gate Drive. The output of the PWM is a totem pole MOSFET gate driver on GTDRV. This output is internally clamped to 15V so that the IC can be operated with VCC as high as 35V. Use a series gate resistor of at least 5 ohms to prevent interaction between the gate impedance and the GTDRV output driver that might cause the GTDRV output to overshoot excessively. Some overshoot of the GTDRV output is always expected when driving a capacitive load.

IAC: Input AC Current. This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{AC}) to MULTOUT, so this is the only multiplier input that should be used for sensing instantaneous line voltage. The nominal voltage on I_{AC} is 6V, so in addition to a resistor from I_{AC} to rectified 60Hz, connect a resistor from I_{AC} to REF. If the resistor to REF is one fourth of the value of the resistor to the rectifier, then the 6V offset will be cancelled, and the line current will have minimal cross-over distortion.

PIN DESCRIPTIONS (continued)

ISENSE: Current sense minus. This is the inverting input to the current amplifier. This input and the non-inverting input MULTOUT remain functional down to and below GND. Care should be taken to avoid taking these inputs below –0.5V, because they are protected with diodes to GND.

MULTOUT: Multiplier output and current sense plus. The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MULTOUT. The cautions about taking I_{SENSE} below –0.5V also apply to MULTOUT. As the multiplier output is a current, this is a high impedance input similar to ISENSE, so the current amplifier can be configured as a differential amplifier to reject GND noise. Figure 12 shows an example of using the current amplifier differentially.

PKLIM: Peak Limit. The threshold for PKLIM is 0.0V. Connect this input to the negative voltage on the current sense resistor as shown in Figure 12. Use a resistor to REF to offset the negative current sense signal up to GND.

VAOUT: Voltage Amplifier Output. This is the output of the op amp that regulates output voltage. Like the current amplifier, the voltage amplifier will stay active even if the IC is disabled with either ENA or VCC. This means that large feedback capacitors across the amplifier will stay charged through momentary disable cycles. Voltage amplifier output levels below 1V will inhibit multiplier output. The voltage amplifier output is internally limited to approximately 5.8V to prevent overshoot. The voltage amplifier output stage is an NPN emitter follower pull-up and an 8k resistor to ground.

VRMS: RMS Line Voltage. The output of a boost PWM is proportional to the input voltage, so when the line voltage into a low-bandwidth boost PWM voltage regulator changes, the output will change immediately and slowly recover to the regulated level. For these devices, the VRMS input compensates for line voltage changes if it is connected to a voltage proportional to the RMS input line voltage. For best control, the VRMS voltage should stay between 1.5V and 3.5V.

REF: Voltage Reference Output. REF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and will remain at 0V when VCC is low or when ENA is low. Bypass REF to GND with an 0.1µF or larger ceramic capacitor for best stability.

VSENSE: Voltage Amplifier Inverting Input. This is normally connected to a feedback network and to the boost converter output through a divider network.

RSET: Oscillator Charging Current and Multiplier Limit Set. A resistor from RSET to ground will program oscillator charging current and maximum multiplier output. Multiplier output current will not exceed 3.75V divided by the resistor from RSET to ground.

SS: Soft Start. SS will remain at GND as long as the IC is disabled or VCC is too low. SS will pull up to over 8V by an internal 14µA current source when both VCC becomes valid and the IC is enabled. SS will act as the reference input to the voltage amplifier if SS is below REF. With a large capacitor from SS to GND, the reference to the voltage regulating amplifier will rise slowly, and increase the PWM duty cycle slowly. In the event of a disable command or a supply dropout, SS will quickly discharge to ground and disable the PWM.

VCC: Positive Supply Voltage. Connect VCC to a stable source of at least 20mA above 17V for normal operation. Also bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate GTDRV signals, these devices will be inhibited unless VCC exceeds the upper under-voltage lockout threshold and remains above the lower threshold.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

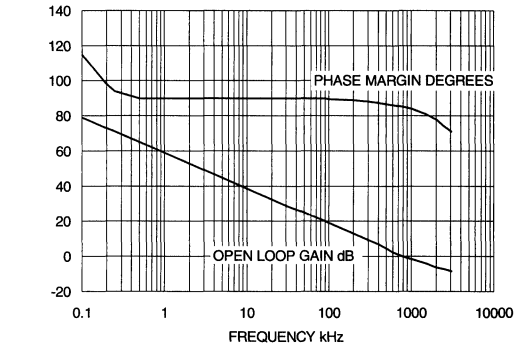


Figure 1. Current Amplifier Gain and Phase vs. Frequency

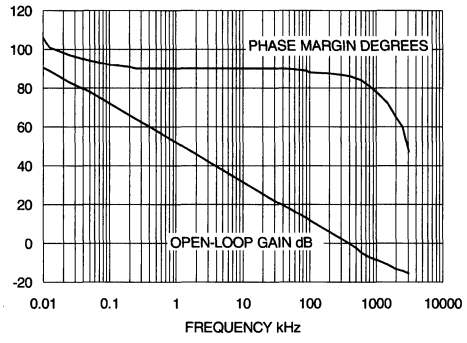


Figure 2. Voltage Amplifier Gain and Phase vs. Frequency

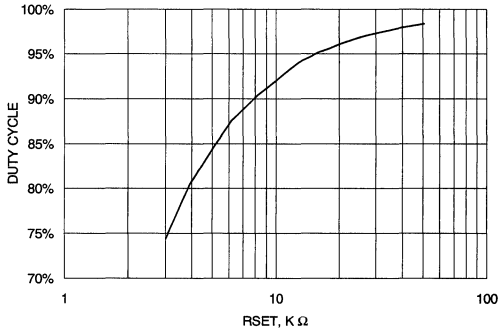


Figure 3. Gate Drive Maximum Duty Cycle

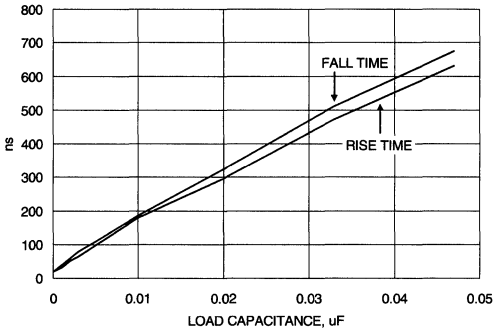


Figure 4. Gate Drive Rise and Fall Time

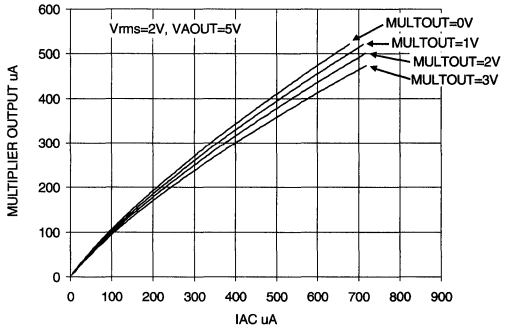


Figure 5. Multiplier Output vs. Voltage on MULTOUT

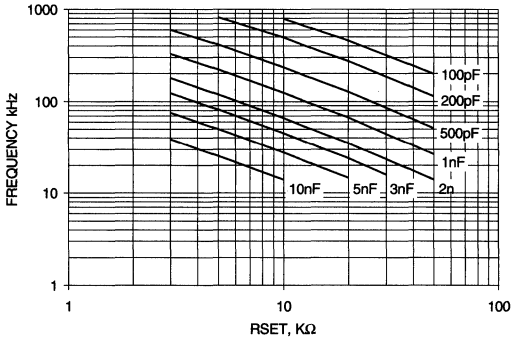


Figure 6. Oscillator Frequency vs. R_{SET} and CT

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$ (continued)

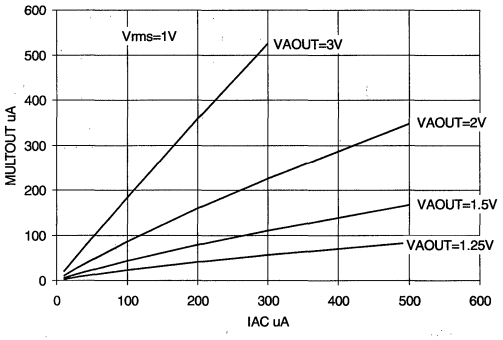


Figure 7. Multiplier Output vs Multiplier Inputs with MULTOUT=0V

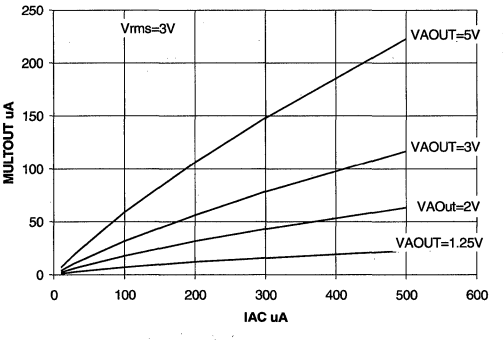


Figure 8. Multiplier Output vs Multiplier Inputs with MULTOUT=0

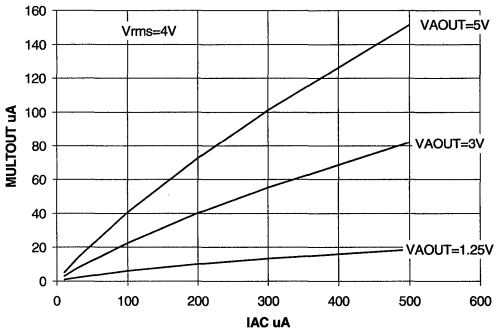


Figure 9. Multiplier Output vs Multiplier Inputs with MULTOUT=0

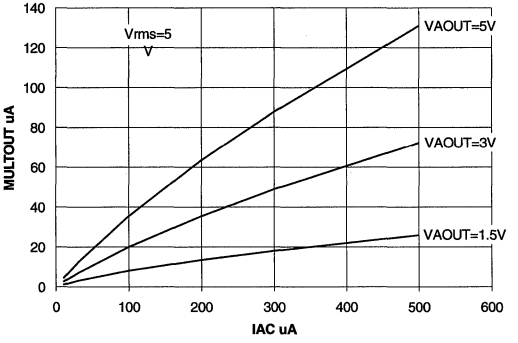


Figure 10. Multiplier Output vs Multiplier Inputs with MULTOUT=0

APPLICATION INFORMATION

A 250W PREREGULATOR

The circuit of Figure 12 shows a typical application of the UC3854 as a preregulator with high power factor and efficiency. The assembly consists of two distinct parts, the control circuit centering on the UC3854 and the power section.

The power section is a "boost" converter, with the inductor operating in the continuous mode. In this mode, the duty cycle is dependent on the ratio between input and output voltages; also, the input current has low switching frequency ripple, which means that the line noise is low. Furthermore, the output voltage must be higher than the peak value of the highest expected AC line voltage, and all components must be rated accordingly.

In the control section, the UC3854 provides PWM pulses (GTDRV, Pin 16) to the power MOSFET gate. The duty cycle of this output is simultaneously controlled by four separate inputs to the chip:

INPUT	PIN NO.	FUNCTION
VSENSE	11	Output DC Voltage
IAC	6	Line Voltage Waveform
ISENSE/MULTOUT	4/5	Line Current
VRMS	8	RMS Line Voltage

APPLICATION INFORMATION (continued)

Additional controls of an auxiliary nature are provided. They are intended to protect the switching power MOSFETS from certain transient conditions, as follows:

INPUT	PIN NO.	FUNCTION
ENA	10	Start-Up Delay
SS	13	Soft Start
PKLIM	2	Maximum Current Limit

PROTECTION INPUTS

ENA (Enable): The ENA input must reach 2.5 volts before the REF and GTDRV outputs are enabled. This provides a means to shut down the gate in case of trouble, or to add a time delay at power up. A hysteresis gap of 200mV is provided at this terminal to prevent erratic operation. Undervoltage protection is provided directly at pin 15, where the on/off thresholds are 16V and 10V. If the ENA input is unused, it should be pulled up to VCC through a current limiting resistor of 100k.

SS (Soft Start): The voltage at pin 13 (SS) can reduce the reference voltage used by the error amplifier to regulate the output DC voltage. With pin 13 open, the reference voltage is typically 7.5V. An internal current source delivers approximately −14μA from pin 13. Thus a capacitor connected between that pin and ground will charge linearly from zero to 7.5V in 0.54C seconds, with C expressed in microfarads.

PKLIM (Peak Current Limit): Use pin 2 to establish the highest value of current to be controlled by the power MOSFET. With the resistor divider values shown in Figure 12, the 0.0V threshold at pin 2 is reached when the voltage drop across the 0.25 ohm current sense resistor is 7.5V*2k/10k=1.5V, corresponding to 6A. A bypass capacitor from pin 2 to ground is recommended to filter out very high frequency noise.

CONTROL INPUTS

VSENSE (Output DC Voltage Sense): The threshold voltage for the VSENSE input is 7.5V and the input bias current is typically 50nA. The values shown in Figure 12 are for an output voltage of 400V DC. In this circuit, the voltage amplifier operates with a constant low frequency gain for minimum output excursions. The 47nF feedback capacitor places a 15Hz pole in the voltage loop that prevents 120Hz ripple from propagating to the input current.

IAC (Line Waveform): In order to force the line current waveshape to follow the line voltage, a sample of the power line voltage in waveform is introduced at pin 6. This signal is multiplied by the output of the voltage amplifier in the internal multiplier to generate a reference signal for the current control loop.

This input is not a voltage, but a current (hence IAC). It is set up by the 220k and 910k resistive divider (see Figure 12). The voltage at pin 6 is internally held at 6V, and the two resistors are chosen so that the current flowing into pin 6 varies from zero (at each zero crossing) to about 400μA at the peak of the waveshape. The following formulas were used to calculate these resistors:

$$R_{AC} = \frac{Vpk}{I_{AC}pk} = \frac{260V_{AC} \times \sqrt{2}}{400\,\mu A} = 910\,k$$

$$R_{REF} = \frac{R_{AC}}{4} = 220\,k$$

(where Vpk is the peak line voltage)

ISENSE/MULTOUT (Line Current): The voltage drop across the 0.25Ω current-sense resistor is applied to pins 4 and 5 as shown. The current-sense amplifier also operates with high low-frequency gain, but unlike the voltage amplifier, it is set up to give the current-control loop a very wide bandwidth. This enables the line current to follow the line voltage as closely as possible. In the present example, this amplifier has a zero at about 500Hz, and a gain of about 18dB thereafter.

VRMS (RMS Line Voltage): An important feature of the UC3854 preregulator is that it can operate with a three-to-one range of input line voltages, covering everything from low line in the US (85VAC) to high line in Europe (255VAC). This is done using line feedforward, which keeps the input power constant with varying input voltage (assuming constant load power). To do this, the multiplier divides the line current by the square of the RMS value of the line voltage. The voltage applied to pin 8, proportional to the average of the rectified line voltage (and proportional to the RMS value), is squared in the UC3854, and then used as a divisor by the multiplier block. The multiplier output, at pin 5, is a current that increases with the current at pin 6 and the voltage at pin 7, and decreases with the square of the voltage at pin 8.

PWM FREQUENCY: The PWM oscillator frequency in Figure 12 is 100kHz. This value is determined by CT at pin 14 and RSET at pin 12. RSET should be chosen first because it affects the maximum value of IMULT according to the equation:

APPLICATION INFORMATION (continued)

$$I_{MULT\,MAX} = \frac{-3.75V}{R_{SET}}$$

This effectively sets a maximum PWM-controlled current. With RSET=15k,

$$I_{MULT\,MAX} = \frac{-3.75V}{15k} = -250\,\mu A$$

Also note that the multiplier output current will never exceed twice IAC.

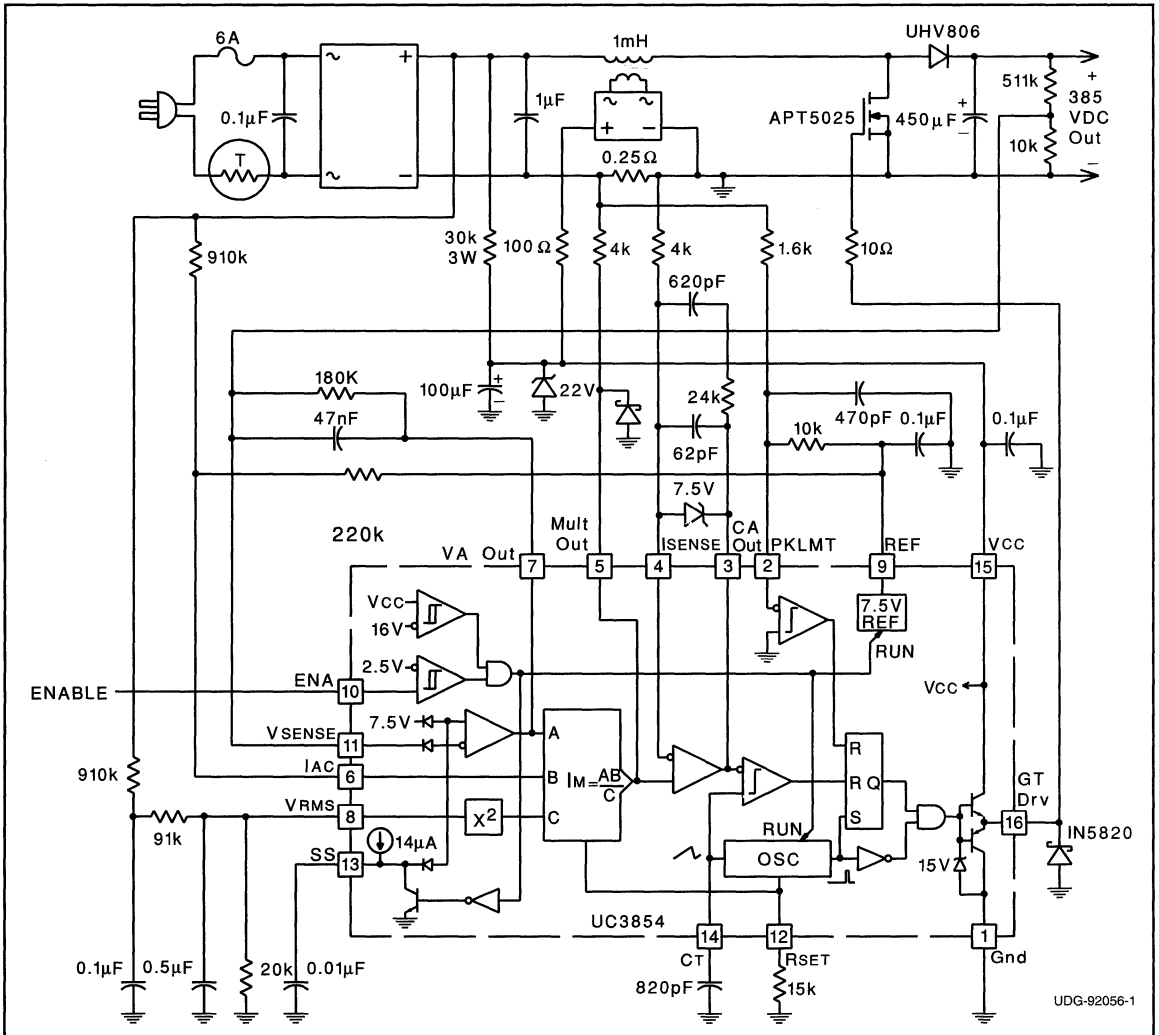
With the 4k resistor from MULTOUT to the 0.25 ohm current sense resistor, the maximum current in the current sense resistor will be

$$I_{MAX} = \frac{-I_{MULT\,MAX} \times 4k}{0.25\,\Omega} = -4A$$

Having thus selected RSET, the current sense resistor, and the resistor from MULTOUT to the current sense resistor, calculate CT for the desired PWM oscillator frequency from the equation

APPLICATION INFORMATION (continued)

This diagram depicts a complete 250 Watt Preregulator. At full load, this preregulator will exhibit a power factor of 0.99 at any power line voltage between 80 and 260 VRMS. This same circuit can be used at higher power levels with minor modifications to the power stage. See Design Note DN-39B and Application Note U-134 for further details.



NOTE: Boost inductor can be fabricated with ARNOLD MPP toroidal core part number A-438381-2, using a 55 turn primary and a 13 turn secondary.

Figure 12. Typical Application

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

application INFO available

UC1854A/B
UC2854A/B
UC3854A/B

Enhanced High Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Limits Line Current Distortion To <3%
- World-Wide Operation Without Switches
- Accurate Power Limiting
- Fixed Frequency Average Current Mode Control
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Integrated Current and Voltage Amp Output Clamps
- Multiplier Improvements: Linearity, 500mV VAC Offset (eliminates external resistor), 0-5V Multout Common Mode Range
- VREF "GOOD" Comparator
- Faster and Improved Accuracy ENABLE Comparator

DESCRIPTION

The UC1854A/B products are pin compatible enhanced versions of the UC1854. Like the UC1854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC1854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

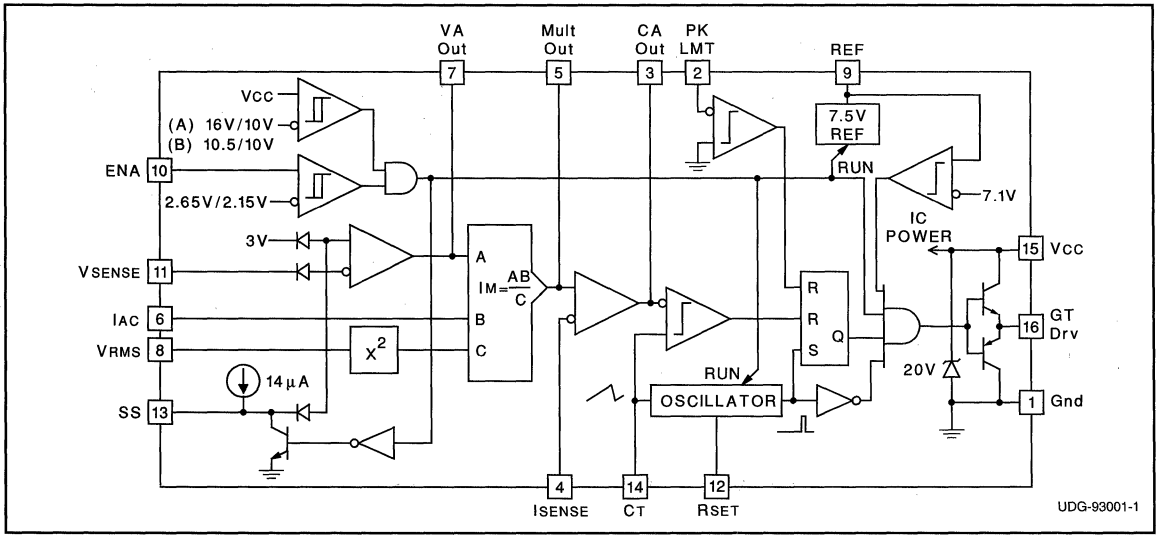
The UC1854A/B products improve upon the UC1854 by offering a wide bandwidth, low offset Current Amplifier, a faster responding and improved accuracy enable comparator, a VREF "good" comparator, UVLO threshold options (16/10V for offline, 10.5/10V for startup from an auxiliary 12V regulator), lower startup supply current, and an enhanced multiply/divide circuit. New features like the amplifier output clamps, improved amplifier current sinking capability, and low offset VAC pin reduce the external component count while improving performance. Improved common mode input range of the Multiplier output/Current Amp input allow the designer greater flexibility in choosing a method for current sensing. Unlike its predecessor, RSET controls only oscillator charging current and has no effect on clamping the maximum multiplier output current. This current is now clamped to a maximum of 2 • IAC at all times which simplifies the design process and provides foldback power limiting during brownout and extreme low line conditions.

A 1% 7.5V reference, fixed frequency oscillator, PWM, Voltage Amplifier with softstart, line voltage feedforward (V_{RMS} squarer), input supply voltage clamp, and over current comparator round out the list of features.

Available in the 16 pin N, DW, and J and 20 pin L and Q packages.

	UVLO Turn on	UVLO Turn off
UC1854A	16V	10V
UC1854B	10.5V	10V

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC 22V
GTDRV Current, Continuous 0.5A
GTDRV Current, 50% Duty Cycle 1.5A
Input Voltage, VSENSE, VRMS 11V
Input Voltage, ISENSE, MULTOUT. 11V
Input Voltage, PKLMT 5V
Input Current, RSET, IAC, PKLMT, ENA 10mA
Power Dissipation. 1W
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

Note 1: All voltages with respect to GND (Pin 1).

Note 2: All currents are positive into the specified terminal.

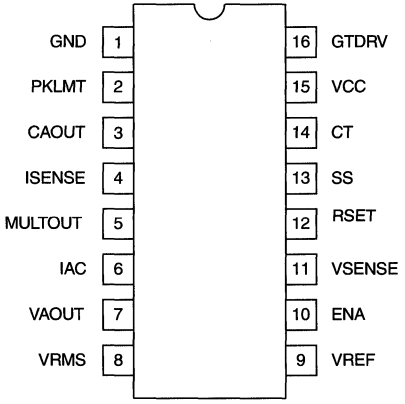
Note 3: ENA imput is internally clamped to approximately 10V.

Note 4: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

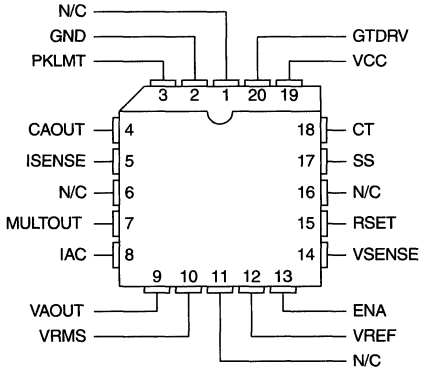
4

CONNECTION DIAGRAMS

DIL–16 & SOIC-16 (Top View)
J, N & DW Packages



PLCC-20 & LCC-20 (Top View)
Q & L Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 18V, R_T = 8.2k, C_T = 1.5nF, PKLMT = 1V, V_{RMS} = 1.5V, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, V_{SENSE} = 3V, –55°C < T_A< 125°C for the UC1854A/B, –40°C < T_A < 85°C for the UC2854A/B, and 0°C < T_A<70°C for the UC3854A/B, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERALL					
Supply Current, Off	CAO, VAO = 0V, V_{CC} = UVLO – 0.3V		250	400	µA
Supply Current, On			12	18	mA
V_{CC} Turn-On Threshold	UC1854A		16	17.5	V
	UC1854B		10.5	11.2	V
V_{CC} Turn-Off Threshold	UC1854A / B	9	10		V
V_{CC} Clamp	I(V_{CC}) = $I_{CC(on)}$ + 5mA	18	20	22	V
VOLTAGE AMPLIFIER					
Input Voltage		2.9	3.0	3.1	V
V_{SENSE} Bias Current		–500	ä25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	70	100		dB
V_{OUT} High	I_{LOAD} = –500µA		6		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3.5	mA
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)		1		mHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 18V, R_T = 8.2k, C_T = 1.5nF, PKLMT = 1V, V_{RMS} = 1.5V, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, V_{SENSE} = 3V, –55°C < T_A< 125°C for the UC1854A/B, –40°C < T_A < 85°C for the UC2854A/B, and 0°C < T_A<70°C for the UC3854A/B, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT AMPLIFIER					
Input Offset Voltage	V_{CM} = 0V	–4		0	mV
		–5.5		0	mV
Input Bias Current(sense)	V_{CM} = 0V	–500		500	nA
Open Loop Gain	V_{CM} = 0V, V_{OUT} = 2 to 6V	80	110		dB
V_{OUT} High	I_{LOAD} = –500µA		8		V
V_{OUT} Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1.5	3.5	mA
Common Mode Range		–0.3		5	V
Gain Bandwidth Product	Fin = 100kHz, 10mV p-p, (Note 1)	3	5		mHz
REFERENCE					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.4	7.5	7.6	V
	I_{REF} = 0mA	7.35	7.5	7.65	V
Load Regulation	I_{REF} = 1 to 10mA	0	8	20	mV
Line Regulation	V_{CC} = 12 to 18V	0	14	25	mV
Short Circuit Current	V_{REF} = 0V	25	35	60	mA
OSCILLATOR					
Initial Accuracy	T_A = 25°C	85	100	115	kHz
Voltage Stability	V_{CC} = 12 to 18V		1		%
Total Variation	Line, Temp	80		120	kHz
Ramp Amplitude (p-p)		4.9		5.9	V
Ramp Valley Voltage		0.8		1.3	V
ENABLE / SOFTSTART / CURRENT LIMIT					
Enable Threshold		2.35	2.55	2.8	V
Enable Hysteresis	V_{FAULT} = 2.5V		500	600	mV
Enable Input Bias Current	V_{ENABLE} = 0V		–2	–5	µA
Propagation Delay to Disable	Enable Overdrive = –100mV,(Note 1)		300		ns
SS Charge Current	$V_{SOFTSTART}$ = 2.5V	10	14	24	
PKLMT Offset Voltage		–15		15	mV
PKLMT Input Current	V_{PKLMT} = –0.1V	–200	–100		µA
PKLMT Propagation Delay	(Note 1)		150		ns
MULTIPLIER					
Output Current - I_{AC} Limited	I_{AC}=100µA, V_{RMS} = 1V, R_{SET} = 10k	–220	–200	–170	µA
Output Current - Zero	I_{AC}=0µA, R_{SET} = 10k	–2.0	–0.2	2.0	µA
Output Current - Power Limited	V_{RMS} = 1.5V, Va = 6V	–230	–200	–170	µA
Output Current	V_{RMS} = 1.5V, Va = 2V		ä22		µA
	V_{RMS} = 1.5V, Va = 5V		ä156		µA
	V_{RMS} = 5V, Va = 2V		ä2		µA
	V_{RMS} = 5V, Va = 5V		ä14		µA
Gain Constant	(Note 2) V_{RMS} = 1.5V, T_J = 25°C, Va = 6V	–1.1	–1.0	–0.9	A/A

Note 1. Guaranteed by design. Not 100% tested in production.

Note 2: Gain constant (K) $\dfrac{I_{AC} \bullet V_A - 1.5V}{V_{RMS}^2 \bullet I_{MO}}$

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 18V, R_T = 8.2k, C_T = 1.5nF, PKLMT = 1V, V_{RMS} = 1.5V, I_{AC} = 100µA, I_{SENSE} = 0V, CA_{OUT} = 3.5V, VA_{OUT} = 5V, V_{SENSE} = 3V, –55°C < T_A< 125°C for the UC1854A/B, –40°C < T_A < 85°C for the UC2854A/B, and 0°C < T_A<70°C for the UC3854A/B, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVER					
Output High Voltage	I_{OUT} = –200mA, V_{CC} = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V
Output Rise / Fall Time	C_{LOAD} = 1nF, (Note 1)		35		ns
Output Peak Current	C_{LOAD} = 10nF, (Note 1)		1.0		A

Note 1. Guaranteed by design. Not 100% tested in production.

Note 2: Gain constant (K) $\dfrac{I_{AC} \bullet V_A - 1.5V}{V_{RMS}^2 \bullet I_{MO}}$

FUNCTIONAL DESCRIPTION

Functional Description

The UC1854A/B products were designed as pin compatible upgrades to the industry standard UC1854 active Power Factor correction circuits. The circuit enhancements allow the user to eliminate in most cases several external components currently required to successfully apply the UC1854. In addition. linearity improvements to the Multiply, Square and Divide circuitry optimizes overall system performance. Detailed descriptions of the circuit enhancements are provided below. For in-depth design applications reference data refer to Unitrode application notes U-134 and DN-44.

Multiply/Square and Divide

The UC1854A/B Multiplier design maintains the same gain constant (K=-1) as the UC1854. The relationship between the inputs and output current is given as:

This is nearly the same as the UC1854, but circuit differences have improved the performance and application. The first difference is with the I_{AC} input. The UC1854A/B regulated this pin voltage to the nominal 500mV over the full operating temperature range, rather than the 6.0V used on the UC1854. The low offset voltage eliminates the need for a line zero crossing compensating resistor to V_{REF} from I_{AC} that UC1854 designs require. The maximum current at high line into IAC should be limited to 250µA for best performance. Therefore, if $V_{AC(max)}$= 270V, the R_{AC} = 270 (1.414)/250µA = 1.53MΩ.

The V_{RMS} pin linear operating range is improved with the UC1854A/B as well. The input range for V_{RMS} extends from 0V to 5.5V. Since the UC1854A squaring circuit employs an analog multiplier, rather than a linear approximation, accuracy is improved, and discontinuities are eliminated. The external divider network connected to V_{RMS} should produce 1.5V at low line (85V_{AC}). This will put 4.77V on V_{RMS} at high line (27V_{AC}) which is well within its operating range.

The Voltage Amplifier output forms the third input to the multiplier and is internally clamped to 6.0V. This eliminated an external zenerclamp often used in UC1854 designs. The offset voltage at this input to the Multiplier has been raised on the UC1854A/B to 1.5V.

The Multiplier output pin, which is also common to the Current Amplifier non-inverting input, has a –0.3V to 5.0V output range, compared to the –0.3V to 2.5V range of the UC1854. This improvement allows the UC1854A/B to be used in applications where the current sense signal amplitude is very large.

Voltage Amplifier

The UC1854 Voltage Amplifier design is essentially similar to the UC1854 with two exceptions. The first is with the internal connection/ The lower voltage reduces the amount of charge on the compensation capacitors, which provides improved recovery form large signal events, such as line dropouts, or power interruption. It also minimizes the DC current flowing through the feedback. The output of the Voltage amplifier is also changes. In addition to a 6.0V temperature compensated clamp, the output short circuit current has been lowered to 2mA typical, and an active pull down has replaced the passive pull down of the UC1854.

Current Amplifier

The Current Amplifier for an average current PFC controller needs a low offset voltage in order to minimize AC line current distortion. With this in mind, the UC1954A/B

FUNCTIONAL DESCRIPTION(continued)

Current Amplifier has improved the input offset voltage from (4mV to 0 to –3mV. The negative offset of the UC1854A/B guarantees that the PWM circuit will not drive the MOSFET is the current command is zero (both Current amplifier inputs zero.) Previous designs required an external offset cancellation network to implement this key feature. The bandwidth of the Current Amplifier has been improved as well to 5mHz typical. While this is not generally an issue at 50Hz or 60Hz inputs, it is essential for 400Hz input avionics applications.

Miscellaneous

Several other important enhancements have been implemented in the UC1854A/B. A V_{CC} supply voltage clamp at 20V allows the controller to be current fed if desired. The lower startup supply current (250μA typical), substantially reduces the power requirements of an offline startup resistor. The 10.5/10V UVLO option (UC1854B) enables the controller to be powered off of an auxiliary 12V supply.

The VREF "GOOD" comparator guarantees that the MOSFET driver output remains low if the supply of the 7.5V reference are not yet up. This improvement eliminates the need for external Schottky diodes on the PKL and CA+ pins that some UC1854 designs require. The propagation delay of the disable feature has been improved to 300ns typical. This delay was proportional to the size of the V_{REF} capacitor on the UC1854, and is typically several orders of magnitude slower.

TYPICAL CHARACTERISTICS at $T_A = T_J = 25°C$

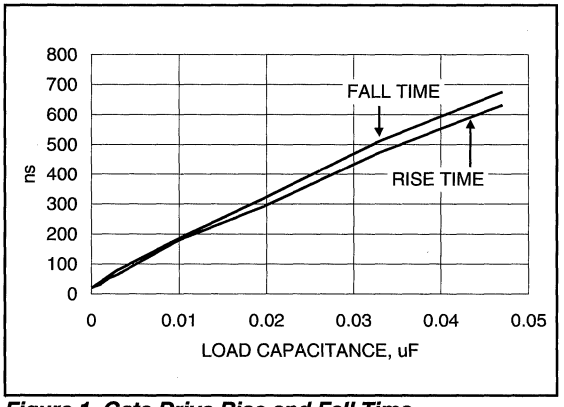


Figure 1. Gate Drive Rise and Fall Time

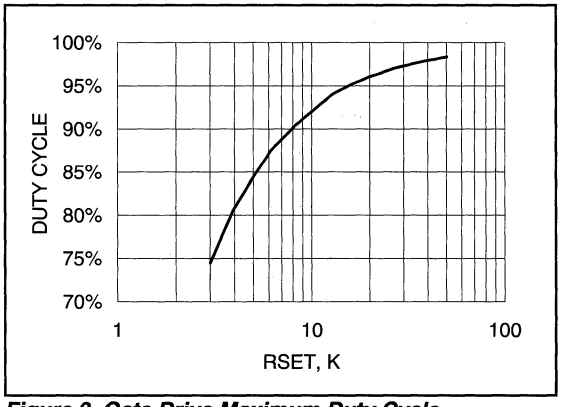


Figure 3. Gate Drive Maximum Duty Cycle

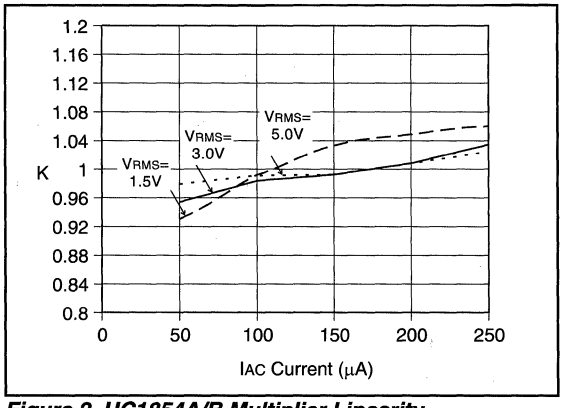


Figure 2. UC1854A/B Multiplier Linearity
VA_{OUT} = 3.5V

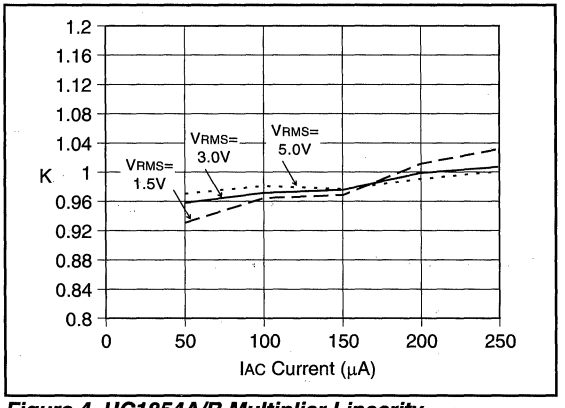


Figure 4. UC1854A/B Multiplier Linearity
VA_{OUT} = 5V

TYPICAL CHARACTERISTICS (cont.)

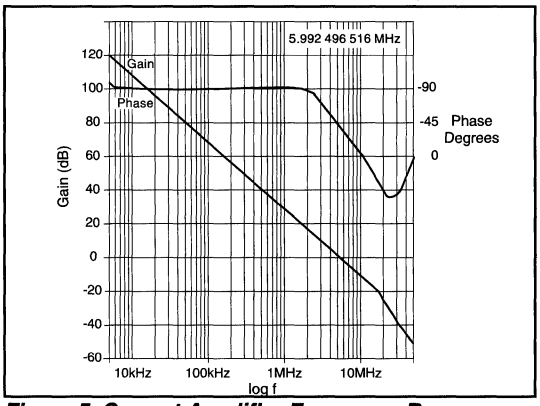


Figure 5. Current Amplifier Frequency Response

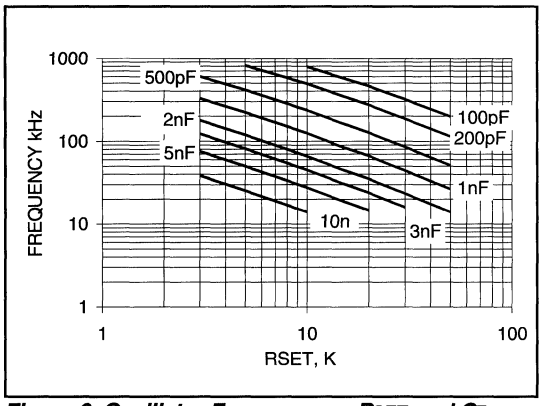


Figure 6. Oscillator Frequency vs RSET and CT

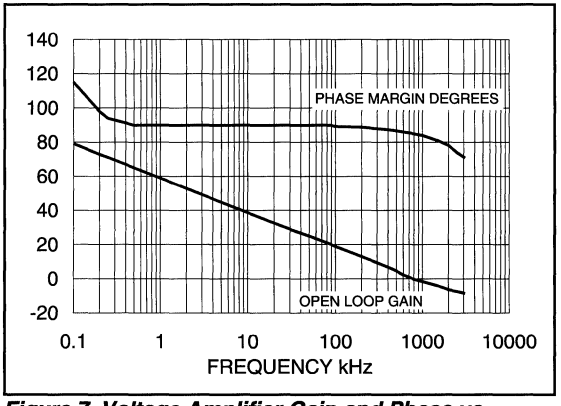


Figure 7. Voltage Amplifier Gain and Phase vs. Frequency

UNITRODE

application INFO available

UC1855A/B
UC2855A/B
UC3855A/B

High Performance Power Factor Preregulator

FEATURES

- Controls Boost PWM to Near Unity Power Factor
- Fixed Frequency Average Current Mode Control Minimizes Line Current Distortion
- Built-in Active Snubber (ZVT) allows Operation to 500kHz, improved EMI and Efficiency
- Inductor Current Synthesizer allows Single Current Transformer Current Sense for Improved Efficiency and Noise Margin
- Accurate Analog Multiplier with Line Compensator allows for Universal Input Voltage Operation
- High Bandwidth (5MHz), Low Offset Current Amplifier
- Overvoltage and Overcurrent protection
- Two UVLO Threshold Options
- 150µA Startup Supply Current Typical
- Precision 1% 7.5V Reference

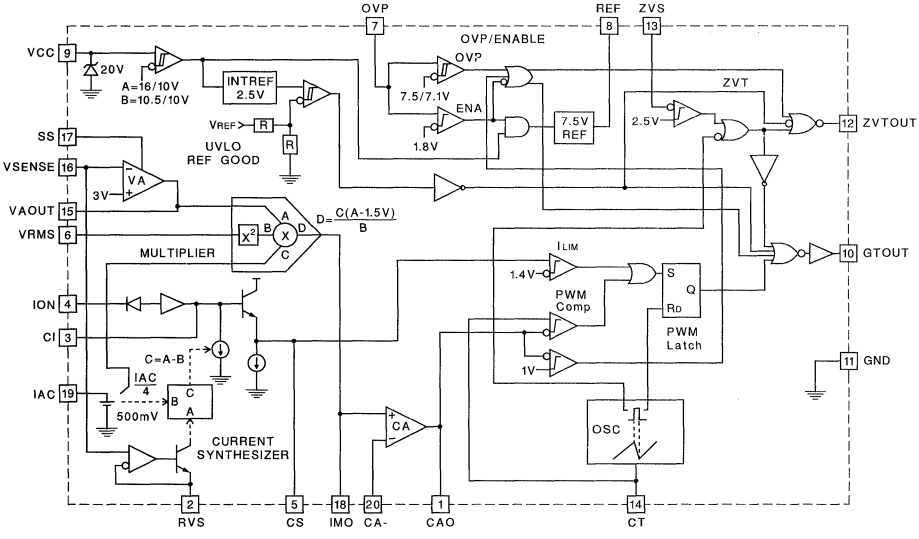
DESCRIPTION

The UC1855A/B provides all the control features necessary for high power, high frequency PFC boost converters. The average current mode control method allows for stable, low distortion AC line current programming without the need for slope compensation. In addition, the UC1855 utilizes an active snubbing or ZVT (Zero Voltage Transition technique) to dramatically reduce diode recovery and MOSFET turn-on losses, resulting in lower EMI emissions and higher efficiency. Boost converter switching frequencies up to 500kHz are now realizable, requiring only an additional small MOSFET, diode, and inductor to resonantly soft switch the boost diode and switch. Average current sensing can be employed using a simple resistive shunt or a current sense transformer. Using the current sense transformer method, the internal current synthesizer circuit buffers the inductor current during the switch on-time, and reconstructs the inductor current during the switch off-time. Improved signal to noise ratio and negligible current sensing losses make this an attractive solution for higher power applications.

The UC1855A/B also features a single quadrant multiplier, squarer, and divider circuit which provides the programming signal for the current loop. The internal multiplier current limit reduces output power during low line conditions. An overvoltage protection circuit disables both controller outputs in the event of a boost output OV condition.

Low startup supply current, UVLO with hysteresis, a 1% 7.5V reference, voltage amplifier with softstart, input supply voltage clamp, enable comparator, and overcurrent comparator complete the list of features. Available packages include: 20 pin N, DW, Q, J, and L.

BLOCK DIAGRAM



License Patent from Pioneer Magnetics. Pin numbers refer to DIL-20 J or N packages.

UDG-94001-2

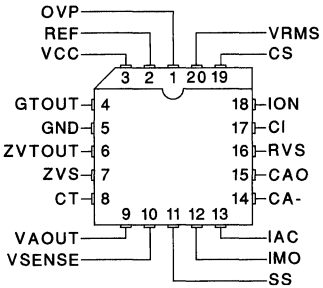
ABSOLUTE MAXIMUM RATINGS

Supply Voltage VCC ..... Internally Limited
VCC Supply Clamp Current 20mA
PFC Gate Driver Current (continuous) ..... ± 0.5A
PFC Gate Driver Current (peak) ..... ± 1.5A
ZVT Drive Current (continuous) ..... ± 0.25A
ZVT Drive Current (peak) ..... ± 0.75A
Input Current (IAC, RT, RVA) 5mA
Analog Inputs (except Peak Limit) ..... –0.3 to 10V
Peak Limit Input ..... –0.3 to 6.5V
Softstart Sinking Current 1.5mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

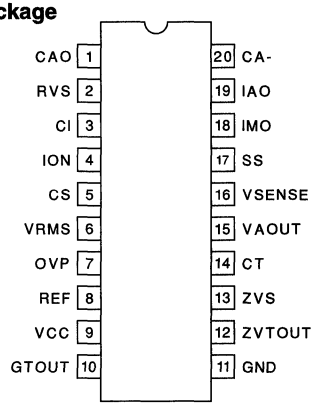
Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

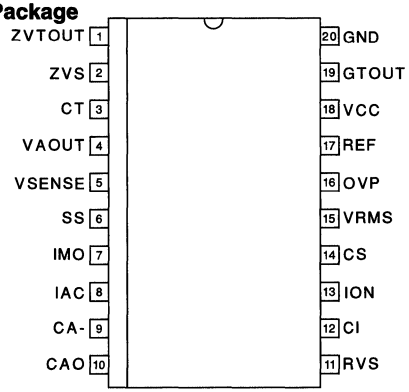
PLCC-20 & LCC-20 (Top View)
Q or L Package



DIL–20 (Top View)
J or N Package



SOIC-20 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, R_T = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I_{SENSE} = 0V, CA_{OUT} = 4V, VAOUT= 3.5V, VSENSE = 3V. $T_A = T_J$. T_A = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, OFF	CAO, VAOUT = 0V, VCC = UVLO –0.3V		150	500	µA
Supply Current, OPERATING			17	25	mA
VCC Turn-On Threshold	UC1855A		15.5	17.5	V
VCCTurn-Off Threshold	UC1855A,B	9	10		V
VCC Turn-On Threshold	UC1855B		10.5	10.8	V
VCC Clamp	I(VCC) = $I_{CC(on)}$ + 5mA	18	20	22	V
Voltage Amplifier					
Input Voltage		2.9		3.1	V
VSENSE Bias Current		–500	25	500	nA
Open Loop Gain	V_{OUT} = 2 to 5V	65	80		dB
V_{OUT} High	I_{LOAD} = –300µA	5.75	6	6.25	V
V_{OUT} Low	I_{LOAD} = 300µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		0.6	3	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, R_T = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I_{SENSE} = 0V, CA_{OUT} = 4V, VAOUT= 3.5V, VSENSE = 3V. T_A = T_J. T_A = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amplifier					
Input Offset Voltage	V_{CM} = – 2.5V	–4		4	mV
Input Bias Current (Sense)	V_{CM} = 2.5V	–500		500	nA
Open Loop Gain	V_{CM} = 2.5V, VOUT = 2 to 6V	80	110		dB
VOUT High	I_{LOAD} = –500µA		6		V
VOUT Low	I_{LOAD} = 500µA		0.3	0.5	V
Output Short Circuit Current	V_{OUT} = 0V		1	3	mA
Common Mode Range		–0.3		5	V
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV, P–P, T_A = 25°C	2.5	5		MHz
Reference					
Output Voltage	I_{REF} = 0mA, TA = 25°C	7.388	7.5	7.613	V
	I_{REF} = 0mA	7.313	7.5	7.688	V
Load Regulation	I_{REF} = 1 to 10 mA	–15		15	mV
Line Regulation	VCC = 15 to 35V	–10		10	mV
Short Circuit Current	REF = 0V	20	45	65	mA
Oscillator					
Initial Accuracy	T_A = 25°C	170	200	230	kHz
Voltage Stability	V_{CC} = 12 to 18V		1		%
Total Variation	Line, Temp.	160		240	kHz
Ramp Amplitude (P–P)		4.9		5.9	V
Ramp Valley Voltage		1.1		1.6	V
Enable/OVP/Current Limit					
Enable Threshold			1.8	2.2	V
OVP Threshold			7.5	7.66	V
OVP Hysteresis		200	400	600	mV
OVP Propagation Delay			200		ns
OVP Input Bias Current	V= 7.5V		1	10	µA
PKLIMIT Threshold		1.25	1.5	1.75	V
PKLIMIT Input Current	$V_{PKLIMIT}$ = 1.5V		100		µA
PKLIMIT Prop. Delay			100		ns
Multiplier					
Output Current - IAC Limited	IAC = 100µA, VRMS = 1V	–235	–205	–175	µA
Output Current - Zero	IAC = 0µA	–2	–0.2	2	µA
Output Current - Power Limited	VRMS = 1.5V, VAOUT = 5.5V	–250	–209	–160	µA
Output Current	VRMS = 1.5V, VAOUT = 2V		–26		µA
	VRMS = 1.5V VAOUT = 5V		–190		µA
	VRMS = 5V, VAOUT = 2V		–3		µA
	VRMS = 5V, VAOUT = 5V		–17		µA
Gain Constant	Refer to Note 1	–0.95	–0.85	–0.75	1/V
Gate Driver Output					
Output High Voltage	I_{OUT} = –200mA, VCC = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 200mA		1	2.2	V
Output Low Voltage	I_{OUT} = 10mA		300	500	mV
Output Low (UVLO)	I_{OUT} = 50mA, VCC = 0V		0.9	1.5	V
Output RISE/FALL Time	CLOAD = 1nF		35		ns
Output Peak Current	CLOAD = 10nF		1.5		A

ELECTRICAL CHARACTERISTICS: Unless otherwise specified: VCC = 18V, R_T = 15k, RVS = 23k, CT = 470pF, CI = 150pF, VRMS = 1.5V, IAC = 100µA, I_{SENSE} = 0V, CA_{OUT} = 4V, VAOUT= 3.5V, VSENSE = 3V. $T_A = T_J$. T_A = –55°C to 125°C (UC1855A/B), –40°C to 85°C (UC2855A/B), 0°C to 70°C (UC3855A/B).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ZVT					
Reset Threshold		2.3	2.6	2.9	V
Input Bias Current	V = 2.5V, V_{CT} = 0		6	20	µA
Propagation Delay	Measured at ZVTOUT		100		ns
Maximum Pulse Width			400		ns
Output High Voltage	I_{OUT} = –100mA, Vcc = 15V	12	12.8		V
Output Low Voltage	I_{OUT} = 100mA		1	2.2	V
	I_{OUT} = 10mA		300	900	mV
Output Low (UVLO)	I_{OUT} = 50mA, V_{CC} = 0V		0.9	1.5	V
Output RISE/FALL Time	C_{LOAD} = 1nF		35		ns
Output Peak Current	C_{LOAD} = 10nF		0.75		A
Current Synthesizer					
ION to CS Offset	VION = 0V		30	50	mV
CI Discharge Current	IAC = 50µA	105	118	140	µA
	IAC = 500µA		5		µA
IAC Offset Voltage		0.3	0.65	1.1	V
ION Buffer Slew Rate			10		V/µs
ION Input Bias Current	V_{ION} = 2V		2	15	µA
RVS Output Voltage	23k from RVS to GND	2.87	3	3.13	V

Note 1: Gain constant (K) $= \frac{IAC \bullet (VA_{OUT} - 1.5V)}{(V_{RMS}{}^2 \bullet IMO)}$ *at* $V_{RMS} = 1.5V$, $VA_{OUT} = 5.5V$.

PIN DESCRIPTIONS

CA–: This is the inverting input to the current amplifier. Connect the required compensation components between this pin and CAOUT. The common mode operating range for this input is between –0.3V and 5V.

CAO: This is the output of the wide bandwidth current amplifier and one of the inputs to the PWM duty cycle comparator. The output signal generated by this amplifier commands the PWM to force the correct input current. The output can swing from 0.1V to 7.5V.

CI: The level shifted current sense signal is impressed upon a capacitor connected between this pin and GND. The buffered current sense transformer signal charges the capacitor when the boost switch is on. When the switch is off, the current synthesizer discharges the capacitor at a rate proportional to the dI/dt of the boost inductor current. In this way, the discharge current is approximately equal to

$$\frac{3V}{RRVS} - \frac{IAC}{4}.$$

Discharging the CI capacitor in this fashion, a "reconstructed" version of the inductor current is generated using only one current sense transformer.

CS: The reconstructed inductor current waveform generated on the CI pin is level shifted down a diode drop to this pin. Connect the current amplifier input resistor between CS and the inverting input of the current amplifier. The waveform on this pin is compared to the multiplier output waveform through the average current sensing current amplifier. The input to the peak current limiting comparator is also connected to this pin. A voltage level greater than 1.5 volts on this pin will trip the comparator and disable the gate driver output.

CT: A capacitor from CT to GND sets the PWM oscillator frequency according to the following equation:

$$f \approx \frac{1}{11200 \bullet CT}.$$

Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscillator and PWM are designed to provide practical operation to 500kHz.

GND: All voltages are measured with respect to this pin. All bypass and timing capacitors connected to GND should have leads as short and direct as possible.

PIN DESCRIPTIONS (cont.)

GTOUT: The output of the PWM is a 1.5A peak totem pole MOSFET gate driver on GTOUT. A series resistor between GTOUT and the MOSFET gate of at least 10 ohms should be used to limit the overshoot on GTOUT. In addition, a low V_F Schottky diode should be connected between GTOUT and GND to limit undershoot and possible erratic operation.

IAC: This is a current input to the multiplier. The current into this pin should correspond to the instantaneous value of the rectified AC input line voltage. This is accomplished by connecting a resistor directly between IAC and the rectified input line voltage. The nominal 650mV level present on IAC negates the need for any additional compensating resistors to accommodate for the zero crossings of the line. A current equal to one fourth of the IAC current forms one of the inductor current synthesizer inputs.

IMO: This is the output of the multiplier, and the noninverting input of the current amplifier. Since this output is a current, connect a resistor between this pin and ground equal in value to the input resistor of the current amplifier. The common mode operating range for this pin is –0.3V to 5V.

ION: This pin is the current sensing input. It should be connected to the secondary side output of a current sensing transformer whose primary winding is in series with the boost switch. The resultant signal applied to this input is buffered and level shifted up a diode to the CI capacitor on the CI pin. The ION buffer has a source only output. Discharge of the CI cap is enabled through the current synthesizer circuitry. The current sense transformer termination resistor should be designed to obtain a 1V input signal amplitude at peak switch current.

OVP: This pin senses the boost output voltage through a voltage divider. The enable comparator input is TTL compatible and can be used as a remote shutdown port. A voltage level below 1.8V, disables V_{REF}, oscillator, and the PWM circuitry via the enable comparator. Between 1.8V and V_{REF} (7.5V) the UC1855 is enabled. Voltage levels above 7.5V will set the PWM latch via the hysteretic OVP comparator and disable both ZVTOUT and GTOUT until the OVP level has decayed by the nominal hysteresis of 400mV. If the voltage divider is designed to initiate an OVP fault at 5% of OV, the internal hysteresis enables normal operation again when the output voltage has reached its nominal regulation level. Both the OVP and enable comparators have direct logical connections to the PWM output and exhibit typical propagation delays of 200ns.

REF: REF is the output of the precision reference. The output is capable of supplying 25mA to peripheral circuitry and is internally short circuit current limited. REF is disabled and low whenever VCC is below the UVLO threshold, and when OVP is below 1.8V. A REF "GOOD" comparator senses REF and disables the stage until REF has attained approximately 90% of its nominal value. Bypass REF to GND with a 0.1µF or larger ceramic capacitor for best stability.

RVS: The nominal 3V signal present on the VSENSE pin is buffered and brought out to the RVS pin. A current proportional to the output voltage is generated by connecting a resistor between this pin and GND. This current forms the second input to the current synthesizer.

VAO: This is the output of the voltage amplifier. At a given input RMS voltage, the voltage on this pin will vary directly with the output load. The output swing is limited from approximately 100mV to 6V. Voltage levels below 1.5V on this pin will inhibit the multiplier output.

VCC: Positive supply rail for the IC. Bypass this pin to GND with a 1µF low ESL, ESR ceramic capacitor. This pin is internally clamped to 20V. Current into this clamp should be limited to less than 10mA. The UC1855A has a 15.5V (nominal) turn on threshold with 6 volts of hysteresis while the UC1855B turns on at 10.5V with 500mV of hysteresis.

VRMS: This pin is the feedforward line voltage compensation input to the multiplier. A voltage on VRMS proportional to the AC input RMS voltage commands the multiplier to alter the current command signal by $1/VRMS^2$ to maintain a constant power balance. The input to VRMS is generally derived from a two pole low pass filter/voltage divider connected to the rectified AC input voltage. This feature allows universal input supply voltage operation and faster response to input line fluctuations for the PFC boost preregulator. For most designs, a voltage level of 1.5V on this pin should correspond to low line, and 4.7V for high line. The input range for this pin extends from 0 to 5.5V.

VSENSE: This pin is the inverting input of the voltage amplifier and serves as the output voltage feedback point for the PFC boost converter. It senses the output voltage through a voltage divider which produces a nominal 3V. The voltage loop compensation is normally connected between this pin and VAO. The VSENSE pin must be above 1.5V at 25°C, (1.9V at –55°C) for the current synthesizer to work properly.

PIN DESCRIPTIONS (cont.)

ZVS: This pin senses when the drain voltage of the main MOSFET switch has reached approximately zero volts, and resets the ZVT latch via the ZVT comparator. A minimum and maximum ZVTOUT pulse width are programmable from this pin. To directly sense the ≈400V drain voltage of the main switch, a blocking diode is connected between ZVS and the high voltage drain. When the drain reaches 0V, the level on ZVS is ≈0.7V which is below the 2.6V ZVT comparator threshold. The maximum ZVTOUT pulse width is approximately equal to the oscillator blanking period time.

For more information see Unitrode Applications Note U-153.

ZVTOUT: The output of the ZVT block is a 750mA peak totem pole MOSFET gate driver on ZVTOUT. Since the ZVT MOSFET switch is typically 3X smaller than the main switch, less peak current is required from this output. Like GTOUT, a series gate resistor and Schottky diode to GND are recommended. This pin may also be used as a high current synchronization output driver.

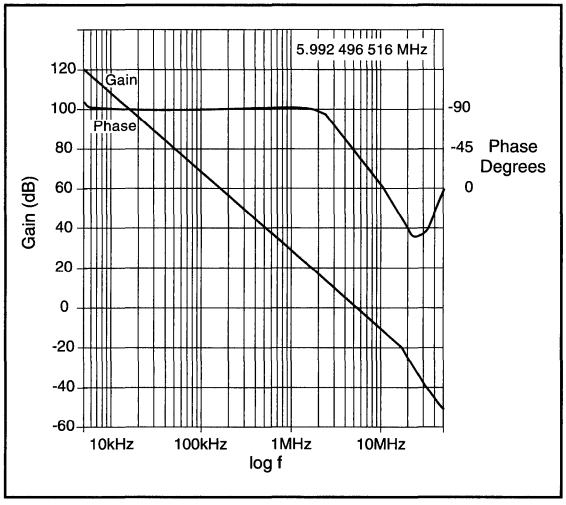


Figure 1. Current Amplifier Frequency Response

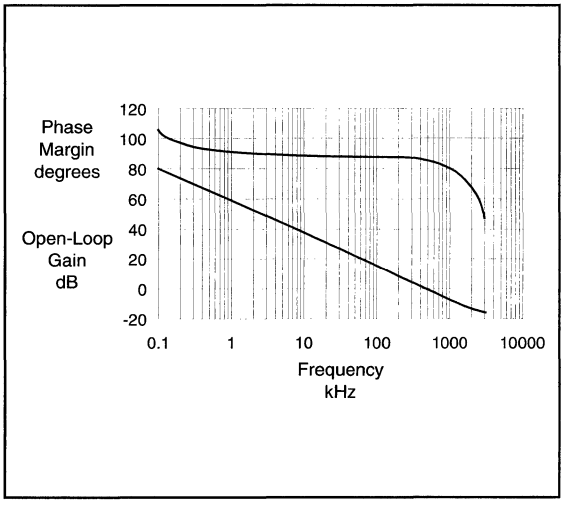


Figure 2. Voltage Amplifier Gain Phase vs Frequency

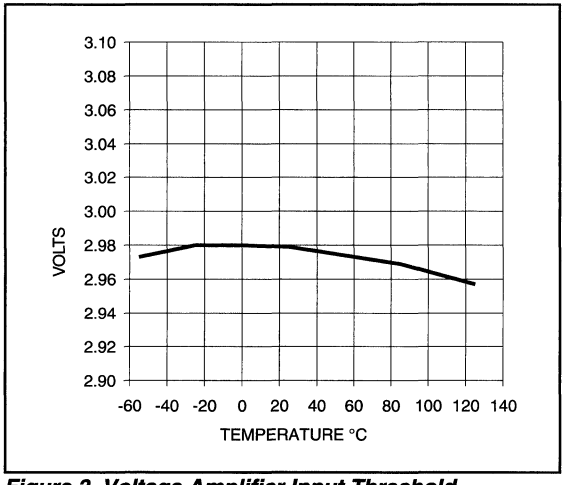


Figure 3. Voltage Amplifier Input Threshold

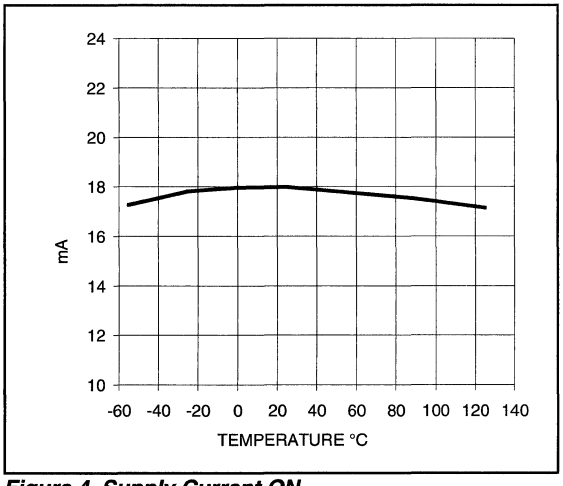


Figure 4. Supply Current ON

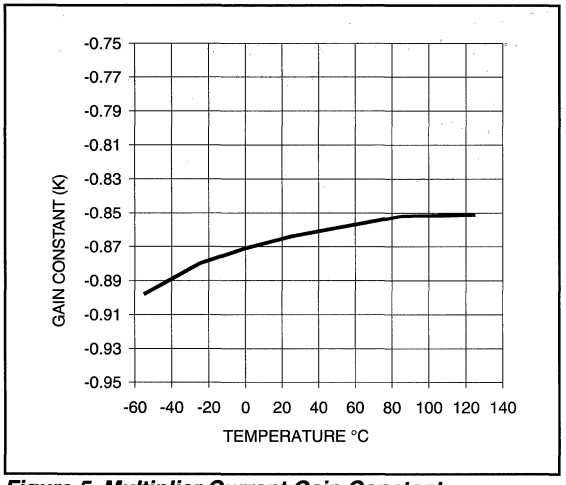


Figure 5. Multiplier Current Gain Constant

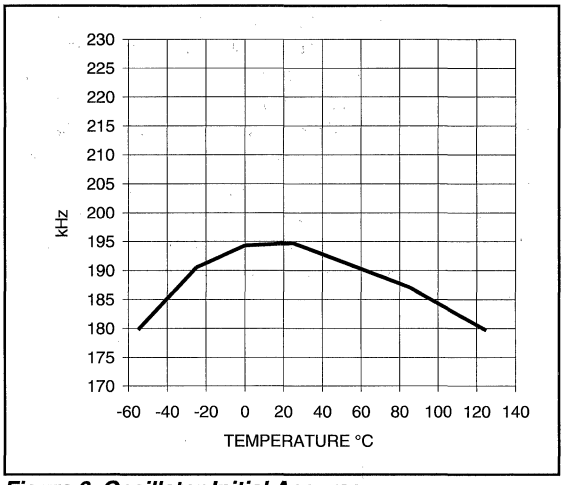


Figure 6. Oscillator Initial Accuracy

TYPICAL APPLICATION

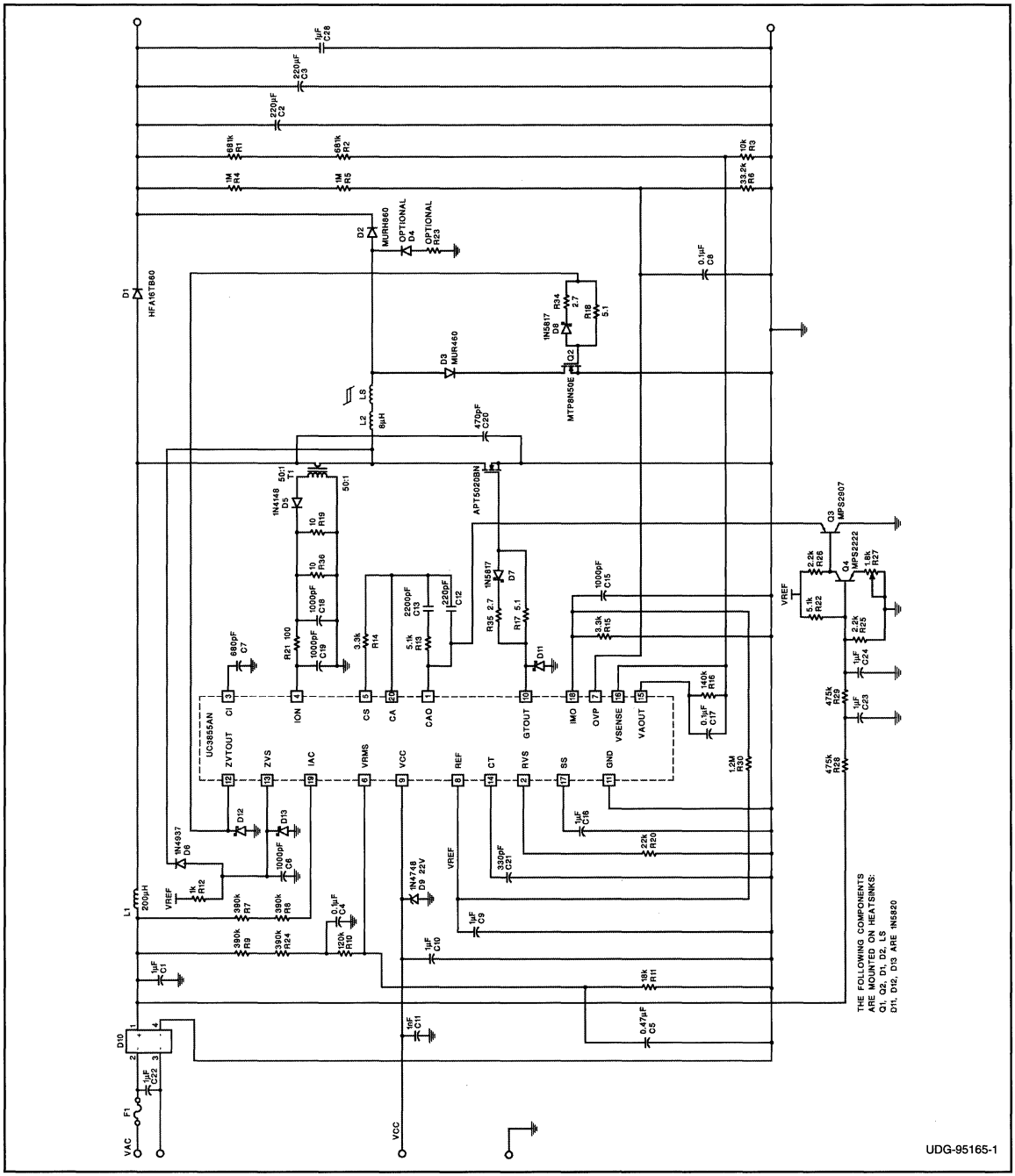


Figure 7. Typical Application

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

Isolated Boost PFC Preregulator Controller

FEATURES

- PFC With Isolation, $V_O < V_{IN}$
- Single Power Stage
- Zero Current Switched IGBT
- Programmable ZCS Time
- Corrects PF to >0.99
- Fixed Frequency, Average Current Control
- Improved RMS Feedforward
- Soft Start
- 9V to 18V Supply V Range
- 20-Pin DW, N, J, and L Packages

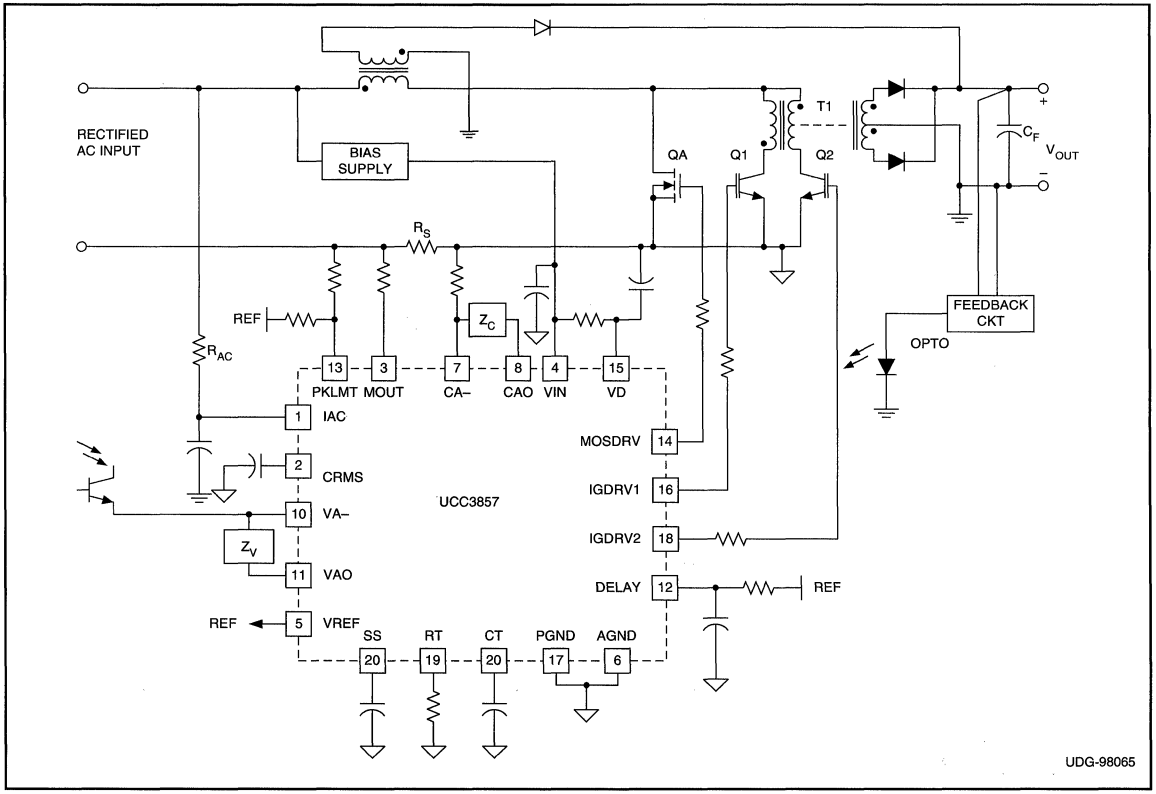
DESCRIPTION

The UCC3857 provides all of the control functions necessary for an Isolated Boost PFC Converter. These converters have the advantage of transformer isolation between primary and secondary, as well as an output bus voltage that is lower than the input voltage. By providing both power factor correction and down conversion in a single power processing stage, the UCC3857 is ideal for applications which require high efficiency, integration, and performance.

The UCC3857 brings together the control functions and drivers necessary to generate overlapping drive signals for external IGBT switches, and provides a separate output to drive an external power MOSFET which provides zero current switching (ZCS) for both the IGBTs. Full programmability is provided for the MOSFET driver delay time with an external RC network. ZCS for the IGBT switches alleviates the undesirable turn off losses typically associated with these devices. This allows for higher switching frequencies, smaller magnetic components and higher efficiency. The power factor correction (PFC) portion of the UCC3857 employs the familiar average current control scheme used in previous Unitrode controllers. Internal circuitry changes, however, have simplified the design of the PFC section and improved performance.

(continued)

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (VIN, VD) 18V
General Analog/Logic Inputs
(CRMS, MOUT, CA–, VA–, CT, RT, PKLMT)
(Maximum Forced Voltage) . . . . . –0.3V to 5V
IAC (Maximum Forced Current) 300µA
Reference Output Current . . . . . Internally Limited
Output Current (MOSDRV, IGDRV1, IGDRV2)
Pulsed 1A
Continuous 200mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

DESCRIPTION (continued)

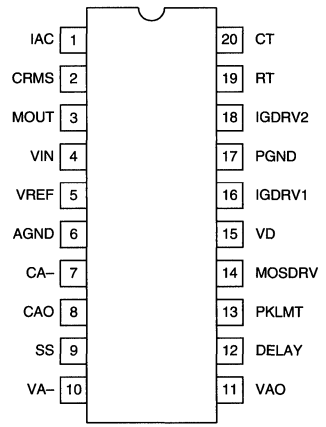
Controller improvements include an internal 6 bit A-D converter for RMS input line voltage detection, a zero load power circuit, and significantly lower quiescent operating current. The A-D converter eliminates an external 2 pole low pass filter for RMS detection.

This simplifies the converter design, eliminates 2nd harmonic ripple from the feedforward component, and provides an approximate 6 times improvement in input line transient response. The zero load power comparator prevents energy transfer during open load conditions without compromising power factor at light loads. Low startup and operating currents which are achieved through the use of Unitrode's BCDMOS process simplify the auxiliary bootstrap supply design.

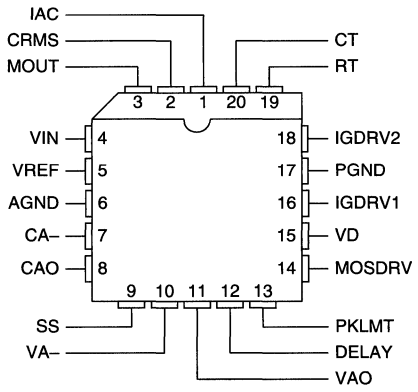
Additional features include: under voltage lockout for reliable off-line startup, a programmable over current shutdown, an auxiliary shutdown port, a precision 7.5V reference, a high amplitude oscillator ramp for improved noise immunity, softstart, and a low offset analog square, multiple and divide circuit. Like previous Unitrode PFC controllers, worldwide operation without range switches is easily implemented.

CONNECTION DIAGRAMS

DIL-20, SOIC- 20 (Top View)
J, N and DW Packages



PLCC-20 (Top View)
L Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, V_{VIN}, V_{VD} = 12V, R_T = 19.2K, C_T = 680pF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current, Active	No Load on Outputs, $V_{VD} = V_{VIN}$		3.5	5	mA
Supply Current, Startup	No Load on Outputs, $V_{VD} = V_{VIN}$		60	TBD	µA
VIN UVLO Threshold			13.75	15.5	V
UVLO Threshold Hysteresis		3	3.75	TBD	V
Reference					
Output Voltage (V_{VREF})	T_J = 25°C, I_{REF} = 1mA	7.387	7.5	7.613	V
	Over Temperature, UCC3857	7.368	7.5	7.631	V
	Over Temperature, UCC1857, UCC2857	7.313	7.5	7.687	V
Load Regulation	I_{REF} = 1mA to 10mA		2	10	mV
Line Regulation	$V_{VIN} = V_{VD}$ = 12V to 16V		2	15	mV
Short Circuit Current	V_{VREF} = 0V		–55	–30	mA
Current Amplifier					
Input Offset Voltage	(Note 1)	–3	0	3	mV
Input Bias Current	(Note 1)		–50		nA
Input Offset Current	(Note 1)		25		nA
CMRR	V_{CM} = 0V to 1.5V, V_{CAO} = 3V		80		dB
AVOL	V_{CM} = 0V, V_{CAO} = 2V to 5V	65	85		dB
VOH	Load on CAO = 50µA, V_{MOUT} = 1V, V_{CA-} = 0V	6	7		V
VOL	Load on CAO = 50µA, V_{MOUT} = 0V, V_{CA-} = 1V		0.2		V
Maximum Output Current	Source : V_{CA-} = 0V, V_{MOUT} = 1V, V_{CAO} = 3V		–150		µA
	Sink : V_{CA-} = 1V, V_{MOUT} = 0V, V_{CAO} = 3V	5	30	50	mA
Gain Bandwidth Product	f_{IN} = 100kHz, 10mV p – p	3	5		MHz
Voltage Amplifier					
Input Voltage	Measured on V_{VA-}, V_{VAO} = 3V	2.9	3	3.1	V
Input Bias Current	Measured on V_{VA-}, V_{VAO} = 3V		–50		nA
AVOL	V_{VAO} = 1V to 5V		75		dB
VOH	Load on V_{VAO}= –50µA, V_{VA-}= 2.8V	5.3	5.55	5.7	V
VOL	Load on V_{VAO}= 50µA, V_{VA-}= 3.2V		0.1	0.45	V
Maximum Output Current	Source: V_{VA-} = 2.8V, V_{VAO} = 3V	–20	–12	–5	mA
	Sink: V_{VA-} = 3.2V, V_{VAO}= 3V	5	20	30	mA
Oscillator					
Initial Accuracy	T_J = 25°C	42.5	50	57.5	kHz
		40	50	60	kHz
Voltage Stability	V_{VIN} = 12V to 18V		1		%
CT Ramp Peak-Valley Amplitude		4	4.5	5	V
CT Ramp Valley Voltage			1.5		V
Output Drivers					
VOH	IL = –100mA	9	10		V
VOL	IL = 100mA		0.1	0.5	V
Rise Time	C_{LOAD} = 1nF		25	TBD	ns
Fall Time	C_{LOAD} = 1nF		10	TBD	ns
Trailing Edge Delay					
Delay Time	R_D = 12k, C_D = 200pF, V_{VAO} = 4V	1.6	2	2.4	µs

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3857, –40°C to +85°C for the UCC2857, and –55°C to +125°C for the UCC1857, V_{VIN}, V_{VD} = 12V, R_T = 19.2K, C_T = 680pF. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Soft Start					
Charge Current			10		µA
Shutdown Comparator Threshold	Measured on SS	0		0.4	V
Multiplier					
Output Current, IAC Limited	I_{AC} = 100µA, V_{VAO} = 5.5V, V_{CRMS} = 0V		–200		µA
Output Current, Power Limited	I_{AC} = 100µA, V_{VAO} = 5.5V, V_{CRMS} = 1V		–200		µA
Output Current, Zero	I_{AC} = 0	–2	0	2	µA
Gain Constant			2.5		1/V
Zero Power, Peak Current					
Zero Power Comparator Threshold	Measured on VAO		0.5		V
Peak Current Limit Comparator Threshold	Measured on PKLMT		0		V

Note 1: Common mode voltages = 0V, V_{CAO} = 3V

PIN DESCRIPTIONS

AGND: Reference point of the internal reference and all thresholds, as well as the return for the remainder of the device except for the output drivers.

CA–: Inverting input of the inner current loop error amplifier.

CAO: Output of the inner current loop error amplifier. This output can swing between approximately 0.2V and 6V. It is one of the inputs to the PWM comparator.

VAO: This is the output of the voltage loop error amplifier. It is internally clamped to approximately 5.6V by the UCC3857 and can swing as low as approximately 0.1V. Voltages below 0.5V on VAO will disable the MOSDRV output and force the IGDRV1 and IGDRV2 outputs to a zero overlap condition.

CRMS: A capacitor is connected between CRMS and ground to average the AC line voltage over a half cycle. CRMS is internally connected to the RMS detection circuitry.

CT: A capacitor (low ESR, ESL) is tied between CT and ground to set the ramp generator switching frequency in conjunction with RT. The ramp generator frequency is approximately given by:

$$f_{SW} \approx \frac{0.67}{R_T \bullet C_T}.$$

DELAY: A resistor to VREF and a capacitor to AGND are connected to DELAY to set the overlap delay time for the MOSDRV output stage. The overlap delay function can be disabled by removing the capacitor to AGND.

IAC: A resistor is connected to the rectified AC input line voltage from IAC. This provides the internal multiplier and the RMS detector with instantaneous line voltage information.

IGDRV1: Driver output for one of the two external IGBT power switches.

IGDRV2: Driver output for one of the two external IGBT power switches.

MOSDRV: Driver output for the external power MOSFET switch.

MOUT: Output of the analog multiply and divide circuit. The output current from MOUT is fed into a resistor to the return leg of the input bridge. The resultant waveform forms the sine reference for the current error amplifier.

PKLMT: Inverting input of the peak current limit comparator. The threshold for this comparator is nominally set to 0V. The peak limit comparator terminates the MOSDRV, IGDRV1 and IGDRV2 outputs when tripped.

PGND: Return for all high level currents, internally tied to the output driver stages of the UCC3857.

RT: A resistor, R_T is tied between RT and ground to set the charging current for the internal ramp generator. The UCC3857 provides a temperature compensated 3.0V at RT. The oscillator charging current is therefore: 3.0V/R_T. Current out of RT should be limited to 250µA for best performance.

VA–: This is the feedback input for the outer voltage control loop. An external opto isolator circuit provides the

PIN DESCRIPTIONS (continued)

output voltage regulation information to VA– across the isolation barrier.

SS: A capacitor is connected between SS and GND to provide the UCC3857 soft start feature. The voltage on VAO, is clamped to approximately the same voltage as SS. An internal 10µA (nominal) current source is provided by the UCC3857 to charge the soft start capacitor.

VD: Positive supply rail for the three output driver stages. The voltage applied to VD must be limited to less than 18VDC. VD should be bypassed to PGND with a 0.1µF to 1.0µF low ESR, ESL capacitor for best results. VD and VIN can be isolated from each other with an RC lowpass filter for better supply noise rejection.

VIN: Input voltage supply to the UCC3857. This voltage must be limited to less than 18VDC. The UCC3857 is enabled when the voltage on VIN exceeds 13.75V (nominal).

VREF: Output of the precision 7.5V reference. A 0.01µF to 0.1µF low ESR, ESL bypass capacitor is recommended between VREF and AGND for best performance.

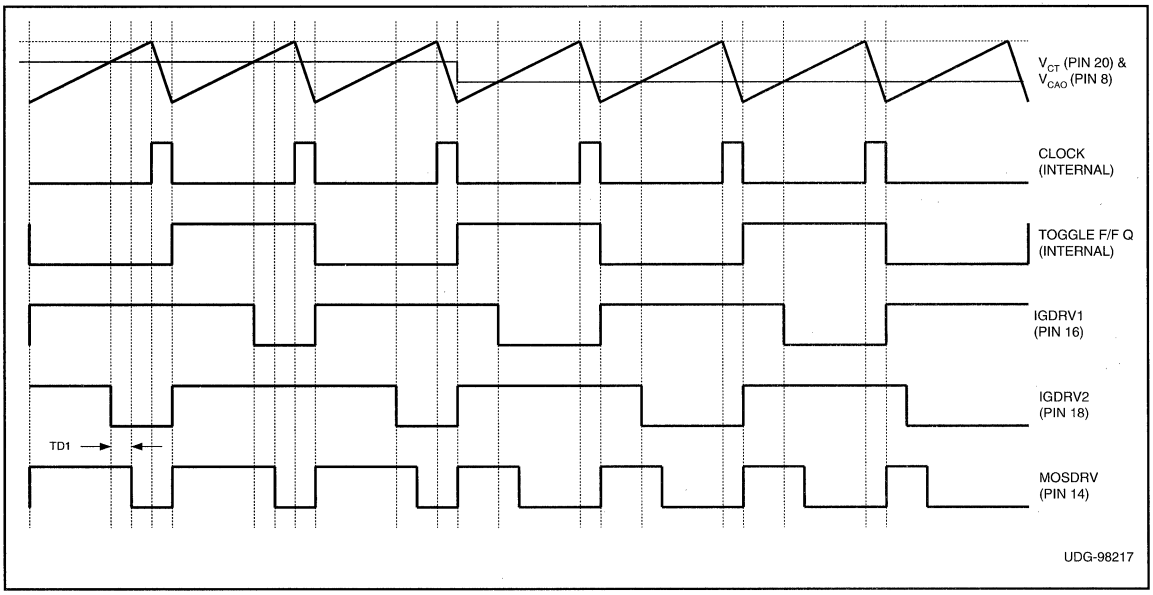


Figure 1. Typical control circuit timing diagram.

APPLICATION INFORMATION

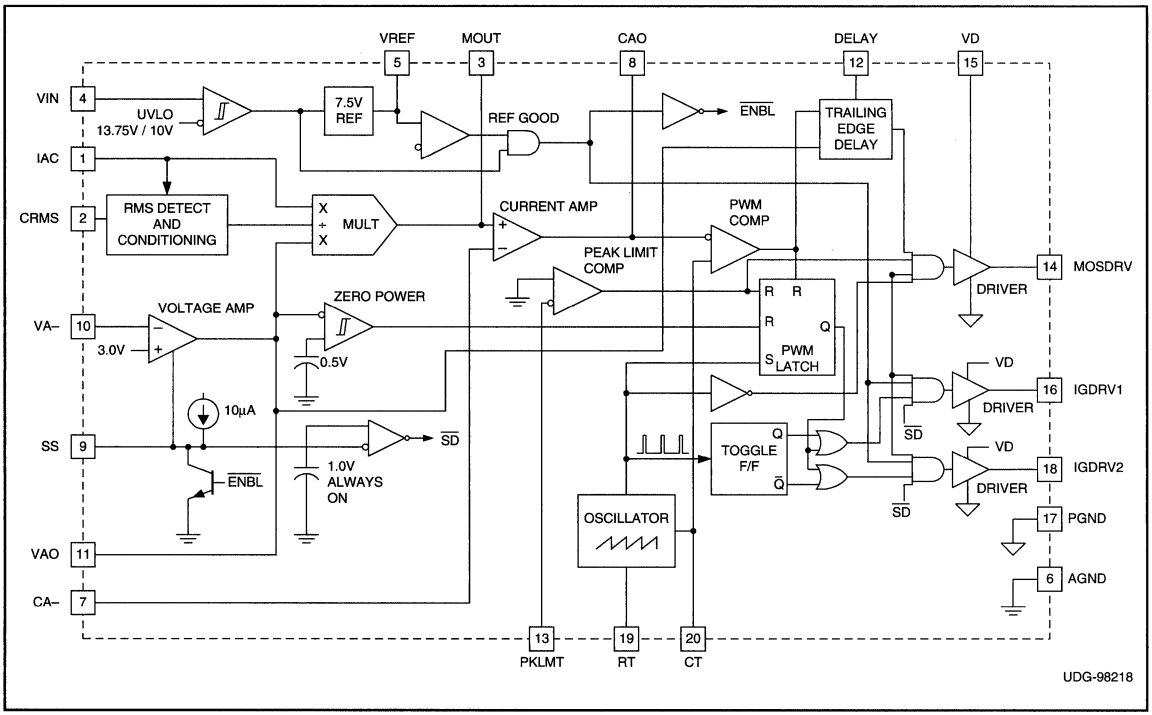
UCC3857 is designed to provide a solution for single stage power factor correction and step-down or step-up function, using an isolated boost converter. The Typical Application Circuit shows the implementation of a typical isolated boost converter using IGBTs as main switches in push-pull configuration and using a MOSFET as an auxiliary switch to accomplish soft-switching of IGBTs. Many variations of this implementation are possible including bridge-type circuits. The presense of low frequency ripple on the output makes this approach practical for distributed bus applications. It will not provide the highly regulated low ripple outputs typically required by logic level supplies.

The circuit shown in the Typical Application Circuit provides several advantages over a more conventional approach of deriving a DC bus voltage from AC line with power factor correction. The conventional approach uses two power conversion stages and has higher cost and complexity. With the use of UCC3857, the dual functionality of power factor correction and voltage step-down is combined into a single stage.

The power stage comprises a current-fed push-pull converter where the ON times of the push-pull switches (Q1 and Q2) are overlapped to provide effective duty cycle of a conventional PWM boost converter. When only one switch is on, the power is transferred to the output

APPLICATION INFORMATION (continued)

BLOCK DIAGRAM



through the transformer and the output rectifier. It can be seen that the ÷ operation on the primary side of the circuit is that of a boost converter and UCC3857 provides input current programming using average current mode control to achieve unity power factor. The transformer turns ratio can be used to get the required level of output voltage (higher or lower than the peak line voltage). The transformer also provides galvanic isolation for the output voltage.

Power stage optimization involves design and selection of components to meet the performance and cost objectives. These include the power switches, transformer and inductor design.

The choice of IGBTs is based on their advantage over MOSFETs at higher voltages. For universal line operation, the voltage stress on the push-pull switches can approach 1000V. However, the slow turn-off of IGBTs can contribute high switching losses and the use of MOSFET (QA) helps turn the IGBTs off with zero voltage across them (ZCS turn-off). This is accomplished by keeping QA on (beyond the turn-off of Q1 or Q2 – see Fig. 1 for waveforms) to allow the inductor current to divert from IGBT to MOSFET while the IGBT is turning off and still maintain zero volts. The MOSFET delay time (TD1) effectively adds to the boost inductor charge period. The voltage stress of the MOSFET is half the stress of the IGBTs under normal operating conditions. However, QA can see much higher voltage stress under start-up and short circuit conditions as the converter operates in a flyback mode then. For different operating requirements or constraints (e.g. single North American line operation), the choice of switching components may be different (e.g. MOSFETs for Q1 and Q2 and no QA) as the voltage stress is different. In that case, UCC3857 can still be used without using the MOSDRV output.

Transformer design is very critical in this topology. The push-pull transformer must have minimal leakage inductance between the primary and secondary windings. Similarly, the leakage between the two primary windings must be minimized. In practice, it is hard to achieve both targets without using sophisticated construction techniques such as interleaving, use of foils etc. In many cases, it may be beneficial to use a planar transformer to achieve these objectives. The effects of higher leakage inductance include higher voltage stresses, ringing, power losses and loss of available duty cycle. The high voltage levels make it difficult to design effective snubber circuits for this leakage induced ringing.

APPLICATION INFORMATION (cont.)

The design of the boost inductor is very similar to the conventional boost converter. However, as shown in the Typical Application Circuit, an additional winding connected to the output through a diode is required on the boost inductor. This winding must have the same turns ratio as the transformer and meet the isolation requirements. This winding is required to provide a discharge path for the inductor energy when the push-pull switches are both off. During start-up, when the output voltage is zero, the converter can see very high inrush currents. The overcurrent protection circuit of UCC3857 will shut down all the outputs when the set threshold is crossed. At that instance, the boost inductor auxiliary winding directs the energy to the output. This is a preferred manner of bringing the output voltage up to prevent the main switches from handling the high levels of inrush current. However, when the auxiliary winding is transferring the power to the output, the voltage stress across QA becomes input voltage plus the reflected output voltage–higher than its steady state value of reflected output voltage.

Chip Bias Supply and Start-up

UCC3857 is implemented using Unitrode's BCDMOS process which allows minimization of the start-up (60µA typical) and operating (3.5mA typical) supply currents. It results in significantly lower power consumption in the trickle charge resistor used to start-up the IC.

Oscillator Set-up

The oscillator of UCC3857 is designed to have a wide ramp amplitude (4.5V p–p) for higher noise immunity. The CT pin has the sawtooth waveshape and during the discharge time of C_T, a clock pulse is generated. During the discharge period, the effective internal impedance to GND is 600Ω. Based on this, the discharge time is given by $831 \bullet C_T$. As shown in the waveforms of Fig. 1, the internal clock pulse width is equal to the discharge time and that sets the minimum dead time between IGDRV1 and IGDRV2. The clock frequency is given by

$$f_{SW} = \frac{1}{(1.5 \bullet R_T + 831) \bullet C_T} \approx \frac{1}{(1.5 \bullet R_T \bullet C_T)} \quad (1)$$

The IGDRV1 and IGDRV2 outputs are switched at half the clock frequency while MOSDRV is switched at the clock frequency.

Reference Signal (I_{MULT}) generation

Like the UC3854 series, the UCC3857 has an analog computation unit (ACU) which generates a reference current signal for the current error amplifier. The inputs to the ACU are signals proportional to instantaneous line voltage, input voltage RMS information and the voltage error amplifier output. Unlike prior techniques of RMS voltage sensing, UCC3857 employs a patent pending technique to simplify the RMS voltage generation and eliminate performance degradation caused by the previous techniques. With the novel technique (shown in Fig. 3), need for external 2-pole filter for V_{RMS} generation is eliminated. Instead, the IAC current is mirrored and used to charge an external capacitor (C_{CRMS}) during a half cycle. The voltage on CRMS takes the integrated sinusoidal shape and is given by equation 2. At the end of the half-cycle, CRMS voltage is held and converted into a 6-bit digital word for further processing in the ACU. C_{CRMS} is discharged and readied for integration during next half cycle.

The advantage of this method is that the second harmonic ripple on the V_{RMS} signal is virtually eliminated. Such second harmonic ripple is unavoidable with the limited roll-off of a conventional 2-pole filter and results in 3rd harmonic distortion in the input current signal. The dynamic response to the input line variations is also improved as a new V_{RMS} signal is generated every cycle.

$$V_{CRMS} = \frac{I_{AC}(pk)}{2 \bullet \omega \bullet C_{CRMS}} (1 - \cos \omega t) \quad (2)$$

$$V_{CRMS}(pk) = \frac{I_{AC}(pk)}{\omega \bullet C_{CRMS}} \quad (2a)$$

For proper operation, $I_{AC}(pk)$ should be selected to be 100µA at peak line voltage. For universal input voltage with peak value of 265 VAC, this means R_{AC} = 3.6M. The noise sensitivity of the IC requires a small bypass capacitor for high frequency noise filtering. The value of this capacitor should be limited to 220nF maximum. The V_{CRMS} value should be approximately 1V at the peak of low line (80 VAC) to minimize any digitization errors. The peak value of V_{CRMS} at high line then becomes 3.5V. The desired C_{CRMS} can be calculated from equation 2 to be 75nF for 60Hz line.

The multiplier output current is given by equation (3) with K = 0.33.

$$I_{MULT} = \frac{(V_{VAO} - 0.5) \bullet I_{AC} \bullet K}{V_{CRMS}^2} \quad (3)$$

The multiplier peak current is limited to 200µA and the selected values for I_{AC} and V_{CRMS} should ensure that the current is within this range. Another limitation of the multiplier is that I_{MULT} can not exceed two times the IAC current, limiting the minimum voltage on V_{CRMS}.

The discrete nature of the RMS voltage feedforward means that there are regions of operation where the in-

APPLICATION INFORMATION (cont.)

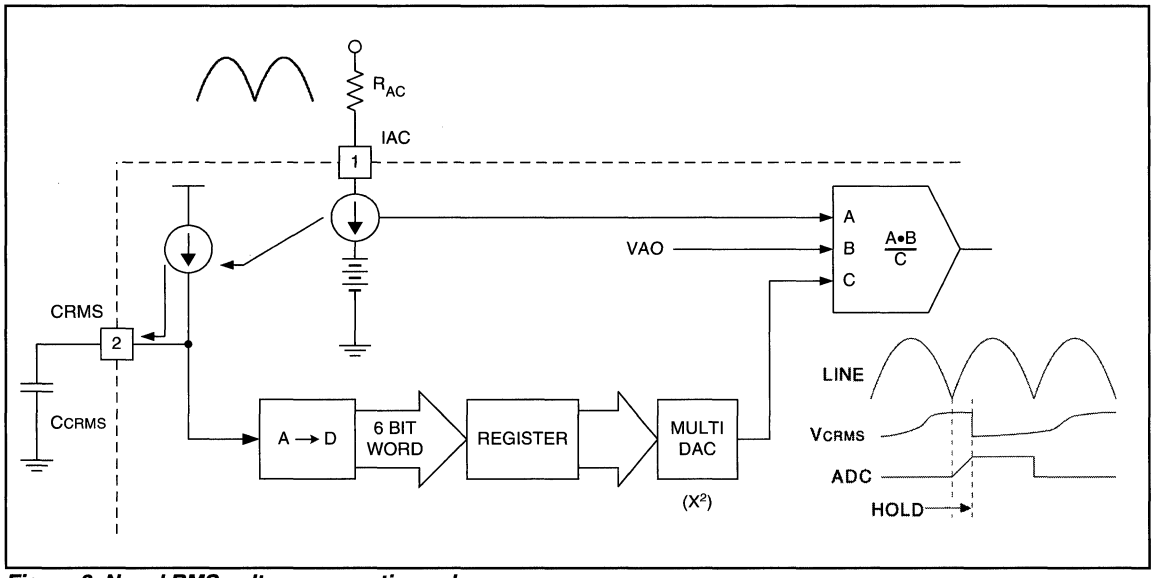


Figure 3. Novel RMS voltage generation scheme.

put voltage changes, but the V_{RMS} value fed into the multiplier does not change. The voltage error amplifier compensates for this by changing its output to maintain the required multiplier output current. When the output of the ADC changes, there is a jump in the output of the error amplifier. This has minimal impact on the overall converter operation.

Another key consideration with the RMS voltage scheme is that it relies on the zero-crossing of the Iac signal to be effective. At very light loads and high line conditions, the rectified AC does not quite reach zero if a large capacitor is being used for filtering on the rectified side of the bridge. In such instances, the feedforward effect does not take place and the controller functionality is compromised. For UCC3857, the I_{AC} current should go below 10µA for the zero crossing detection to take place. It is recommended that the capacitor value be kept low enough for light load operation or that the alternative scheme shown in Fig. 4 be used for I_{AC} sense.

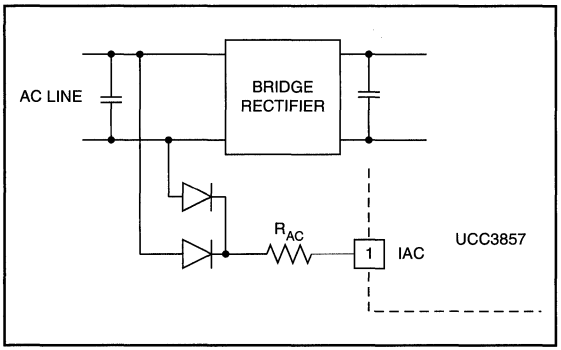


Figure 4. Alternative implementation for sensing I_{AC}.

Gate Drive Considerations

The gate drive circuits in UCC3857 are designed for high speed driving of the power switches. Each drive circuit consists of low impedance pull-up and pull-down DMOS output stages. The UCC3857 provides separate supply and ground pins (VD and PGND) for the driver stages. These pins allow better local bypassing of the driver circuits. VD can also be used to ensure that the SOA limits of the output stages are not violated when driving high peak current levels. For this, VD can be kept as low as possible (e.g. 10V) while VIN can go higher to handle the UVLO requirements.

Current Amplifier Set-up

Once the multiplier is set-up by choosing the V_{RMS} range, the current amplifier components can be designed. The maximum multiplier output is at low line, full load conditions. The inductor peak current also occurs at the same point. The multiplier terminating resistor can be determined using equation 4.

$$R_{MULT} = \frac{I_{L-PK} \bullet R_{SENSE}}{I_{MULT-PK}} \quad (4)$$

The current amplifier can be compensated using a previously presented techniques (U-134) summarized here. A simplified high frequency model for inductor current to duty cycle transfer function is given by

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{Vo}{sL} \quad (5)$$

The gain of the current feedback path at the frequency of interest (crossover) is given by

$$\frac{\hat{d}}{\hat{i}_L} = R_{SENSE} \bullet \frac{R_Z}{R_I} \bullet \frac{1}{V_{SE}} \quad (6)$$

Where VSE is the ramp amplitude (p-p) which is 4.5V for UCC3857. Combining equations. 5 and 6 yields the loop gain of the current loop and equating it to 1 at the desired crossover frequency can result in a design value for R_Z. The current loop crossover frequency should be limited to about 1/3 of the switching frequency of the converter to ensure stability. See Unitrode Application Note U-140 for further information.

Trailing Edge Delay

As shown in the waveforms of Fig. 1, the modified isolated boost converter requires drive signals for the two main (IGBT) switches and the auxiliary (MOSFET) switch with certain timing relationships. The delay between turn-off of an IGBT and turn-off of the MOSFET can be programmed for the UCC1857. In a PFC application, the input line varies from zero to the AC peak level, resulting in a wide range of required duty ratios. A fixed delay time will induce line current distortion at the peaks of the AC line under high line and/or light load conditions. This is caused by the minimum controllable duty ratio imposed on the modulator by the fixed delay. If the minimum controllable duty ratio is fixed, the inner current loop can exhibit a limit cycle oscillation at the line peaks, inducing line current distortion.

The UCC1857 has an adaptive MOSFET delay generator, which is directly modulated by load power demand. Referring to Fig. 5, this circuit directly varies the delay time based on the output level of the voltage error amplifier, which in an average current mode PFC converter with line feedforward is indicative of load power. The delay time is programmed with external components, R_D and C_D. The sequence of events starts when the internal CLK signal resets latch U2, causing PWMDEL to go high and the Q output to go low. C_D was discharged via M1 and is held low until the internal PWM signal goes low (indicating turn-off of either of the IGBT drives). At this point M1 turns off and C_D charges towards the 7.5V reference through R_D. A comparator U1 compares this voltage to the voltage error amplifier output (V_{VAO}). When the voltage on C_D is greater than V_{VAO}, the latch U2 is set causing PWMDEL to go low. PWMDEL is logically

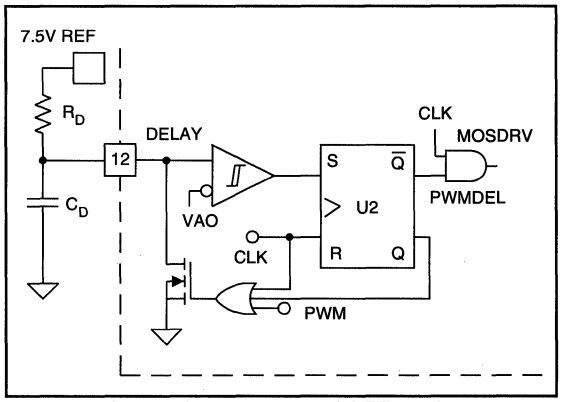


Figure 5. Circuit for adaptive MOSFET delay generation.

ANDed with $\overline{CLK}$ to produce the signal which commands the MOSFET driver output (MOSDRV). The delay time, TD1, is given by

$$TD1 = -R_D \bullet C_D \bullet \ell n\left(\frac{7.5 - V_{VAO}}{7.5}\right) \quad (7)$$

This technique reduces the overlap delay at light loads or high lines, but maintains a longer delay when the line voltage is low or the load is heavy. This by definition reduces the minimum controllable duty ratio to an acceptable level, and is programmable by the user. Reducing the delay time under light current conditions is acceptable since the IGBT current is directly proportional to load current. By providing programming flexibility with R_D and C_D, the delay times can be optimized for current and future classes of IGBT switches. The delay can also be set to zero by removing C_D from the circuit.

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application INFO available

UCC1858
UCC2858
UCC3858
PRELIMINARY

High Efficiency, High Power Factor Preregulator

FEATURES

- Programmable PWM Frequency Foldback for Higher Efficiency at Light Loads
- Leading Edge PWM for Reduced Output Capacitor Ripple Current
- Controls Boost PWM to Near Unity Power Factor
- World Wide Operation without Switches
- Accurate Power Limiting
- Synchronizable Oscillator
- 100µA Startup Supply Current
- Low Power BCDMOS
- 12V to 18V Operation

DESCRIPTION

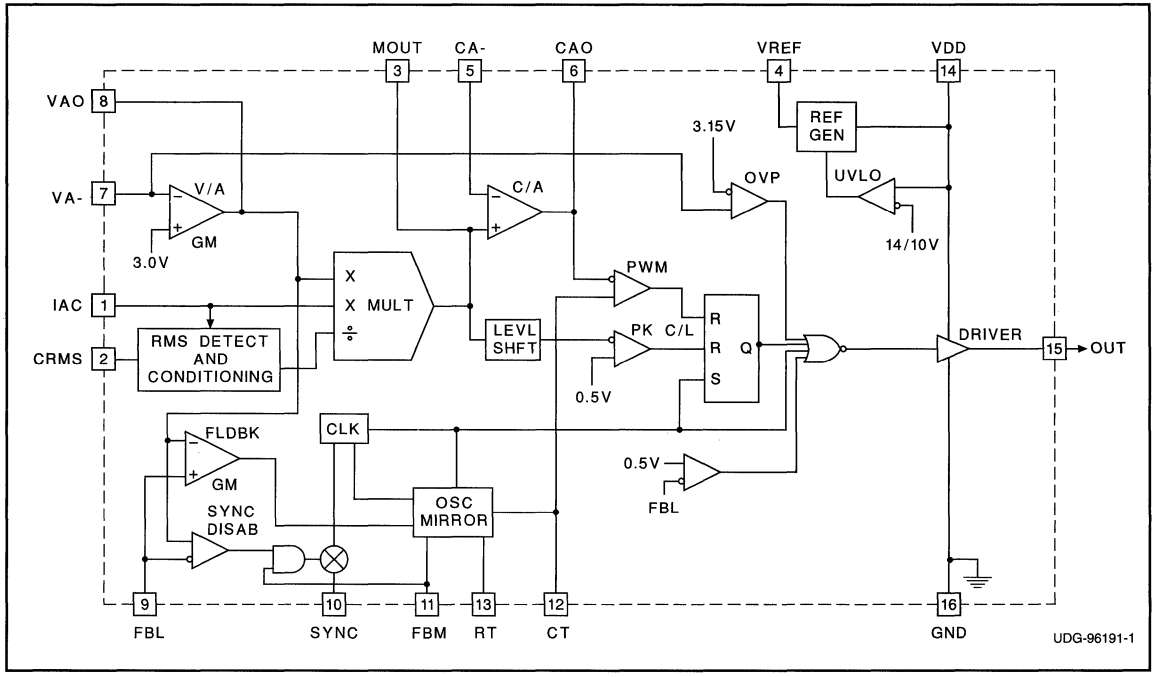
The UCC3858 provides all of the control functions necessary for active power factor corrected preregulators which require high efficiency at low power operation. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage using average current mode control.

The operation of the UCC3858 closely resembles that of previously designed Unitrode PFC parts with additional features to allow higher efficiency boost converter operation at light loads. This is accomplished by linearly scaling back the PWM frequency when the output of the voltage error amplifier drops below a predetermined user programmable level indicating a light load condition. The frequency is scaled back by reducing the charging current for the CT ramp (in proportion to the output power), and increasing the dead time. There is also an instantaneous reset input to pull the IC out of foldback mode quickly when the load comes back up.

The PWM technique used in the UCC3858 is leading edge modulation. When combined with the more conventional trailing edge modulation on the downstream converter, this scheme offers the benefit of reduced ripple current on the bulk storage capacitor. The oscillator is designed for easy synchronization to the downstream converter. A simple synchronization scheme can be implemented by connecting the PWM output of the downstream converter to the SYNC pin.

(continued)

BLOCK DIAGRAM



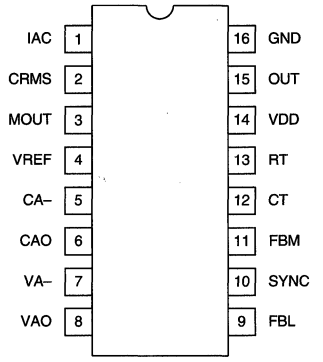
ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} 18V
Gate Drive Current
  Continuous 0.2A
  Pulsed 500mA
Input Current IAC 200mA
Power Dissipation 1W
Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... +300°C
Analog Inputs
  Maximum Forced Voltage ..... –0.3V to 11V

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIP-16, SOIC-16 (TOP VIEW)
J, N, DW Packages



DESCRIPTION (cont.)

Controller improvements include an onboard peak detector for the input line RMS voltage, an integrated overcurrent shutdown, overvoltage shutdown and significantly lower quiescent operating current. The peak detector eliminates an external 2-pole low pass filter for RMS detection. This simplifies the converter design as well as providing an approximate 6X improvement in input line transient response. The current signal is extracted from the current error amplifier input to provide a cycle-by-cycle peak current limit. Low startup and operating currents which are achieved through the use of Unitrode's BCDMOS process simplify the bootstrap supply design as well as minimize losses in the control circuit. A transconductance voltage error amplifier allows output voltage sensing for internal overvoltage protection.

Additional features include: undervoltage lockout for reliable off-line startup, a precision 7.5V reference, and a precision RMS detection and signal conditioning circuit. Chip shutdown can be attained by bringing the FBL pin below 0.5V.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3858, –40°C to +85°C for the UCC2858, and –55°C to +150°C for the UCC1858, V_{VDD} = 12V, R_T = 24k, C_T = 330pF, R_{FBM} = 96k, I_{IAC} = 100µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Off	V_{CAO}, V_{VAO} = 0V, V_{DD} = UVLO – 0.3V		100	250	µA
Supply Current, On	FBL = 0V	2	3.5	5	mA
VDD Turn-On Threshold		12	13.5	15.5	V
VDD Turn-Off Threshold			10		V
UVLO Hysteresis		3.2	3.5	3.8	V
Voltage Amplifier					
Input Voltage	T_A = 25°C	2.95	3	3.05	V
Over Voltage Protection	Volts Above VA– Input Voltage	0.12	0.14	0.16	V
VA– Bias Current			–0.5	–1	µA
Open Loop Gain	V_{OUT} = 2V to 5V	45	50		dB
VAO High	Load = –25µA	5.7	6	6.3	V
VAO Low	Load = 25µA		0.3	0.5	V
Output Source Current	$V_{VA–}$ = 2.8V			–50	µA
Output Sink Current	$V_{VA–}$ = 3.2V	50			µA
Transconductance	I_{OUT} = ± 50µA	400	600	1000	µS

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3858, –40°C to +85°C for the UCC2858, and –55°C to +150°C for the UCC1858, V_{VDD} = 12V, R_T = 24k, C_T = 330pF, R_{FBM} = 96k, I_{IAC} = 100µA, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Amplifier					
Input Offset Voltage	V_{CM} = 0V, V_{CAO} = 3V	–3	0	3	mV
Input Bias Current	V_{CM} = 0V, V_{CAO} = 3V	–6.5	–5		µA
Input Offset Current	V_{CM} = 0V, V_{CAO} = 3V	–0.5	0.0	0.5	µA
Open Loop Gain	V_{CM} = 0V, V_{CAO} = 2V to 5V	80	90		dB
CMRR	V_{CM} = 0V to 1.5V, V_{CAO} = 3V	65	80		dB
CAO High	V_{CA-} = 0V, V_{MOUT} = 1V, I_L = –50µA	6.5	7	7.5	V
CAO Low	V_{CA-} = 1V, V_{MOUT} = 0V, I_L = 1mA		0.2	0.3	V
Maximum Output Source Current		–130	–150		µA
Voltage Reference					
Output Voltage	I_{REF} = 0mA, T_A = 25°C	7.313	7.5	7.688	V
	Over Temperature, UCC3858	7.294	7.5	7.707	V
	Over Temperature, UCC2858, UCC1858	7.239	7.5	7.762	V
Load Regulation	I_{REF} = 0mA to 2mA		3	5	mV
Line Regulation	V_{DD} = 12V to 16V		30		mV
Short Circuit Current	V_{REF} = 0V		35	50	mA
Oscillator					
Initial Accuracy	T_A = 25°C	90	100	110	kHz
Voltage Stability	V_{DD} = 12V to 16V			1	%
Total Variation	Line, Temperature	80		120	kHz
Ramp Amplitude (p-p)	Oscillator Free Running, VAO = 5.5V	3.3	3.5	3.7	V
Ramp Peak Voltage	Oscillator Free Running, VAO = 5.5V	4.4	4.6	4.8	V
Peak Current Limit					
PKLMT Threshold Voltage	(V_{CA-})–V_{MOUT}	350	450	550	mV
PKLMT Hysteresis			100	200	mV
PKLMT Propagation Delay			1		µs
Multiplier Section					
High Line, Low Power	I_{AC} = 100µA, V_{CRMS} = 3.5V, VA_{OUT} = 1.25V		1		µA
High Line, High Power	I_{AC} = 100µA, V_{CRMS} = 3.5V, VA_{OUT} = 5.5V		15		µA
Low Line, Low Power	I_{AC} = 20µA, V_{CRMS} = 0.75V, VA_{OUT} = 1.25V		4		µA
Low Line, High Power	I_{AC} = 20µA, V_{CRMS} = 0.75V, VA_{OUT} = 5.5V		64		µA
IAC Limited	I_{AC} = 20µA, V_{CRMS} = 0.4V, VA_{OUT} = 5.5V		64		µA
Gain Constant	I_{AC} = 100µA, V_{CRMS} = 3.5V, VA_{OUT} = 5.5V		2.5		1/V
Zero Current	I_{AC} = 20µA, V_{CRMS} = 0.75V, VA_{OUT} = 5.5V (Note 1)		0		µA
	I_{AC} =100µA, V_{CRMS} = 3.5V, VA_{OUT} = 5.5V (Note 1)		0		µA
Power Limit (V_{CRMS} • I_{MO})	I_{AC} = 20µA, V_{CRMS} = 0.75V, VA_{OUT} = 5.5V		45		µW
PWM Frequency Foldback					
FBL Input Current		–500	–100		nA
FBL Output Disable			0.5		V
Foldback Minimum Frequency	R_{FBM} = 100k		25	30	kHz
FBM Foldback Override			1.5	1.75	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3858, –40°C to +85°C for the UCC2858, and –55°C to +150°C for the UCC1858, V_{VDD} = 12V, R_T = 24k, C_T = 330pF, R_{FBM} = 96k, I_{IAC} = 100µA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Driver					
Pull Up Resistance	I_{OUT} = 100mA		7		Ω
Pull Down Resistance	I_{OUT} = –100mA		3.5		Ω
Output Rise Time	C_{LOAD} = 1nF, R_S = 10Ω		25		ns
Output Fall Time	C_{LOAD} = 1nF, R_S = 10Ω		20		ns

Note1: M_{OUT} current with contributions form CA+ and peak limit level shift subtracted out.

PIN DESCRIPTIONS

CA–: (Current Amplifier Inverting Input) This input and the non-inverting input MOUT remain functional down to GND.

CAO: (Current Amplifier Ouput) Output of a wide bandwidth amplifier that senses line current and commands the pulse width modulator (PWM) to force the correct current. This output can swing close to GND, allowing the PWM to force zero duty cycle when necessary.

CRMS: (RMS Measurement Capacitor) A capacitor connected between CRMS and GND enables averaging of the AC line voltage over a half cycle. IAC current is internally mirrored to provide charging current for CRMS.

CT: (Oscillator Timing Capacitor) A capacitor from CT to GND will set the free-running PWM oscillator frequency according to:

$$f = \frac{0.814}{R_T \bullet C_T}$$

FBL: (Frequency Foldback Level Select) Selects the level of the voltage error amplifier output at which frequency foldback begins. A chip shutdown can be attained by bringing the foldback level pin to below 0.5V.

FBM: (Minimum Frequency Reference) A resistor between this pin and VREF is used to set the minimum frequency during foldback mode. Once the value of R_T and C_T are determined, use

$$R_{FBM} = \frac{0.857}{C_T \bullet f_{MIN}} - R_T$$

to find the value of R_{FBM} which will set the minimum foldback frequency to f_{MIN}. This pin also incorporates a foldback override which enables the part to return quickly to normal operating mode when the load comes back up. To override foldback mode, force this pin below 1.5V with an open collector.

GND: (Ground) All voltages measured with respect to ground. VDD and VREF should be bypassed directly to GND with a 0.1µF or larger ceramic capacitor. The timing capacitor discharge current also returns to this pin, so the lead from CT to GND should be as short and direct as possible.

IAC: (Input AC Current) This input to the analog multiplier is a current. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to MOUT. Requires some bypassing to GND for noise filtering (<470pF).

MOUT: (Multiplier Output) The output of the analog multiplier and the non-inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high impedance input so the amplifier can be configured as a differential amplifier to reject ground noise. The voltage at this pin is also used to implement peak current limiting.

OUT: (Gate Drive Output) The output of the PWM is a totem pole MOSFET gate driver. A series gate resistor of at least 5Ω is recommended to prevent interaction between the gate impedance and the output driver that might cause the gate drive to overshoot excessively.

RT: (Oscillator Timing Resistor) A resistor from RT to GND is used to program oscillator discharge current.

SYNC: (Oscillator Synchronization Input) Allows the PFC to be synchronized to a trailing edge modulator in the DC-DC stage. A synchronization pulse can be generated from the positive output edge of the downstream regulator and applied to this pin. The internal clock is reset (charged up) on the rising edge of the SYNC input.

VA–: (Voltage Amplifier Inverting Input) This pin is normally connected to the boost converter output through a divider network. It also is an input to the overvoltage comparator where by the output is terminated if this pin's voltage exceeds 3.15V.

VAO: (Voltage Amplifier Output) Output of the transconductance amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 6V for power limiting. It is also used to determine the frequency foldback mode. Compensation

PIN DESCRIPTIONS (cont.)

network is connected from this pin to GND.

VDD: (Positive Supply Voltage) Connect to a stable source of at least 20mA between 13V and 17V for normal operation. Bypass VDD directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitance. To prevent inadequate gate drive signals, the output devices will be inhibited unless V_{VDD} exceeds the upper undervoltage lockout voltage threshold and remains above the lower threshold.

VREF: (Reference Voltage) VREF is the output of an accurate 7.5V voltage reference. This output is capable of delivering 10mA to peripheral circuitry and is internally short circuit current limited. VREF is disabled and will remain at 0V when V_{VDD} is low. Bypass VREF to GND with

4

APPLICATION INFORMATION

The UCC3858 is designed to optimize the implementation of power factor corrected boost converters in low to medium power applications where light load efficiency is critical. While basic configuration of the UCC3858 is similar to the industry standard UC3854 series controllers, several distinguishing features have been added. A typical application circuit is shown along with a diagram showing how the UCC3858 can be used with the downstream converter to achieve optimum performance.

Chip Bias Supply and Startup

The UCC3858 is implemented using Unitrode's BCDMOS process allowing minimal startup (60µA typical) and operating (3.5mA typical) supply currents. This results in significantly lower power consumption in the trickle charge resistor used to startup the IC, increasing the system efficiency at light loads. Lower supply currents, coupled with the wide undervoltage lockout hysteresis (13.75V on, 10V off) provide the opportunity to operate both stages from the same startup and bootstrap supply as shown in the typical application drawing.

Oscillator and Frequency Foldback at Light Loads

The oscillator of the UCC3858 is set up to operate either synchronously with the downstream converter or as a stand alone oscillator. A simplified block diagram of the oscillator and associated circuitry is shown in Fig. 2 and the related waveforms are shown in Fig. 3a - 3c. A rising edge at the SYNC pin initiates the clock cycle by charging up the CT pin with a nominal internal current of I_{CHnom} (=19 •I_{DIS}). Once the high threshold of the ramp (4.5V) is crossed, the internal latch is set and the CT pin starts discharging at a rate (I_{DIS}=3/R_T) set by the resistor on the RT pin. In the absence of a SYNC pulse, C_T discharges all the way to the ramp low threshold (1V) and that sets the free running frequency of the oscillator as given by equation 1. In applications where synchronization is used, the R_T, C_T values should be chosen so that the free running frequency is always lower than the synchronization frequency.

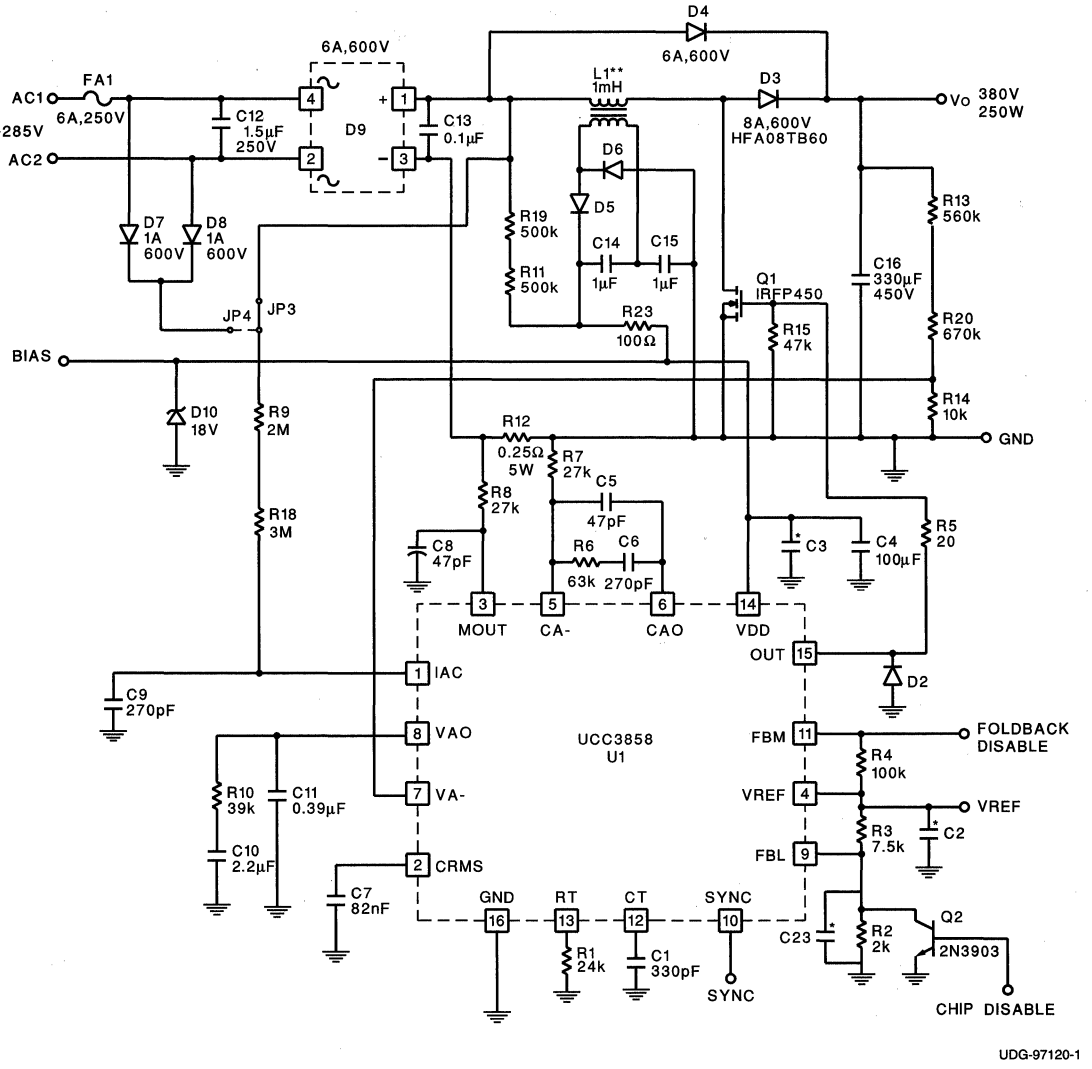
$$f = \frac{19}{20} \bullet \frac{3}{3.5} \bullet \frac{1}{R_T \bullet C_T} \qquad (1)$$

When VAO falls below the threshold level set by FBL, the oscillator goes into frequency foldback mode and disables synchronization. The frequency foldback is achieved by reducing the oscillator charging current as the power level (and VAO voltage) falls. As shown in Fig. 2, the difference between VAO and FBL regulates current I_{Csub} which subtracts the current available for charging C_T. The effective charge current into the capacitor is given by (I_{CHnom} - I_{Csub}). To avoid converter operation in the low frequency range (e.g. audio), the charge current should not be allowed to go very low. Minimum frequency of the controller is programmed by the current I_{MIN} flowing into pin FBM which sets the minimum charging current. The value of R_{FBM} to set the desired minimum frequency is given by:

$$R_{FBM} = \frac{3}{3.5} \bullet \frac{1}{f_{MIN} \bullet C_T} - R_T \qquad (2)$$

Fig. 4 shows the characteristic curves for the frequency foldback. When the converter comes out of the low power mode, the time taken to restore normal mode operation (return to nominal or synchronized frequency operation) must be minimized. Given that the voltage error amplifier response is very slow in PFC circuits, the VAO pin change is not the best indicator of change in load conditions. UCC3858 provides a solution where the normal mode can be restored instantaneously when FBM is pulled below 1.5V. A typical interface would involve the output of the error amplifier of the downstream converter (with proper buffering and filtering) driving an npn switch that pulls FBM down to GND. The buffer and filter should ensure that the switch is turned on only when the error amplifier of downstream converter is saturated high for a preset duration indicating a droop in output voltage from increased load. The FBM input can also be permanently pulled low to disable the frequency foldback mode completely, while still using the other features of UCC3858. FBL pin also acts as a chip disable input when it is brought below 0.5V.

APPLICATION INFORMATION (cont.)



** Pins 4, 9 and 14 need good bypassing to GND for noise immunity. Capacitors C2, C3 and C23 should each consist of a combination of ceramic (0.47µF) and tantalum (4.7µF) capacitors for best results.*

*** L1 can be fabricated with an Allied Signal Amorphous Core MP4510PFC, using a 100 turn (AWG 18) primary and 5 turn secondary. Alternatively, a gapped Ferrite Choke can be used. (Coiltronics CTX-08-13679)*

Figure 1. UCC3858 Typical application circuit.

APPLICATION INFORMATION (cont.)

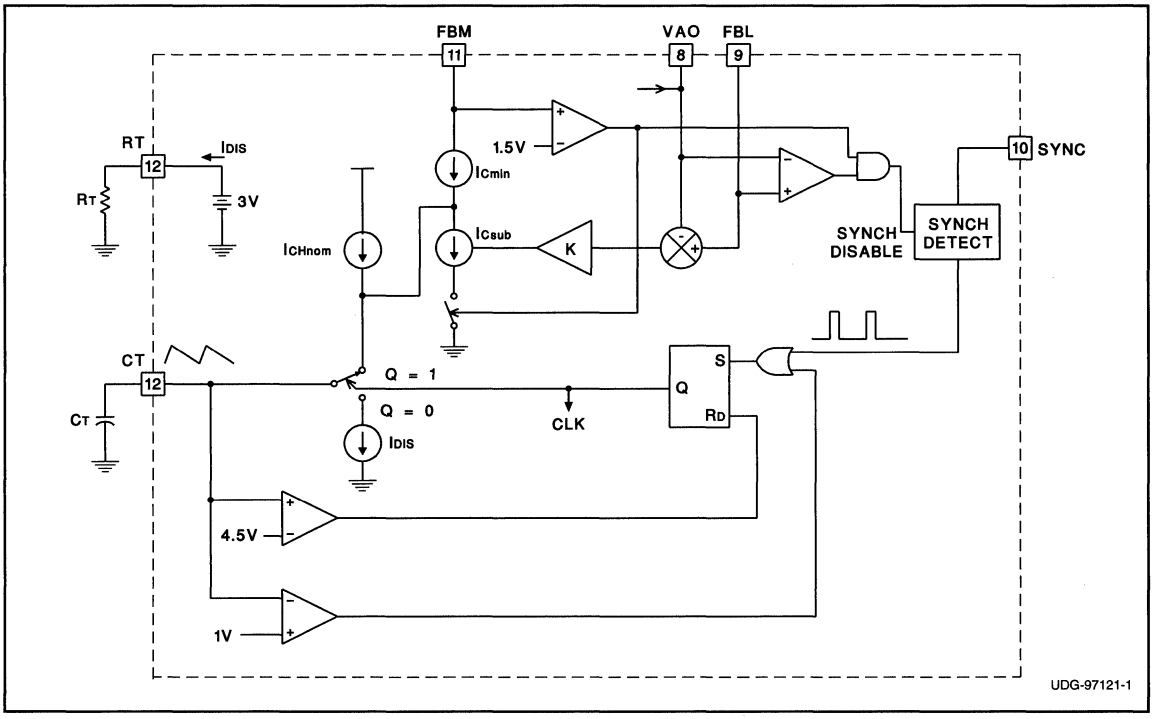


Figure 2. Oscillator block diagram.

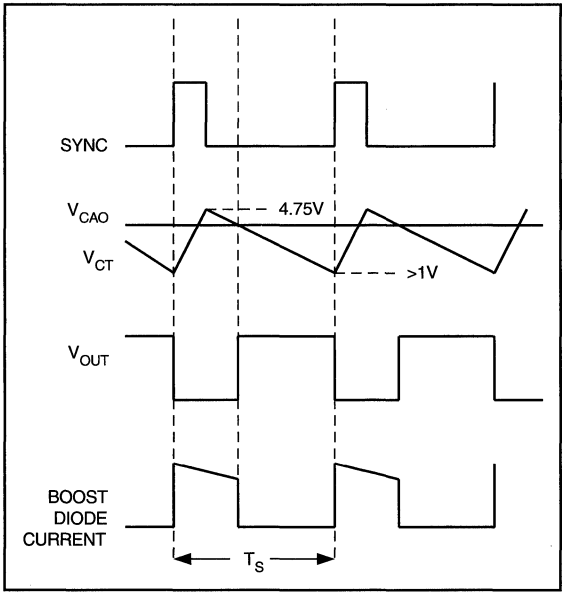


Figure 3a. Oscillator timing waveforms synchronized to buck (DC/DC) PWM.

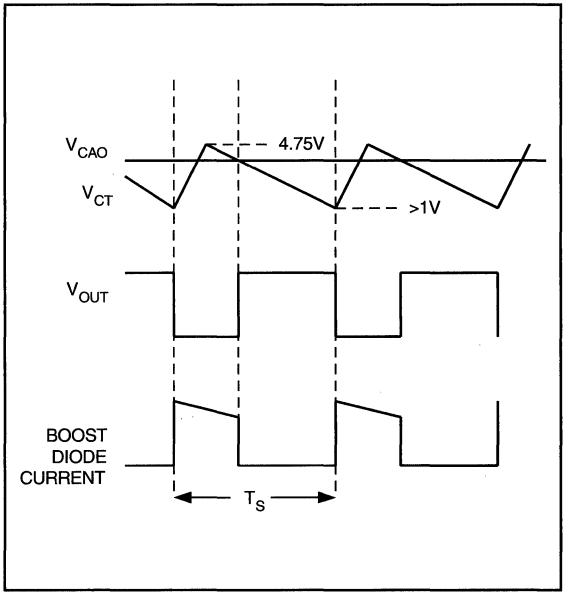


Figure 3b. Oscillator timing waveforms stand alone operation.

APPLICATION INFORMATION (cont.)

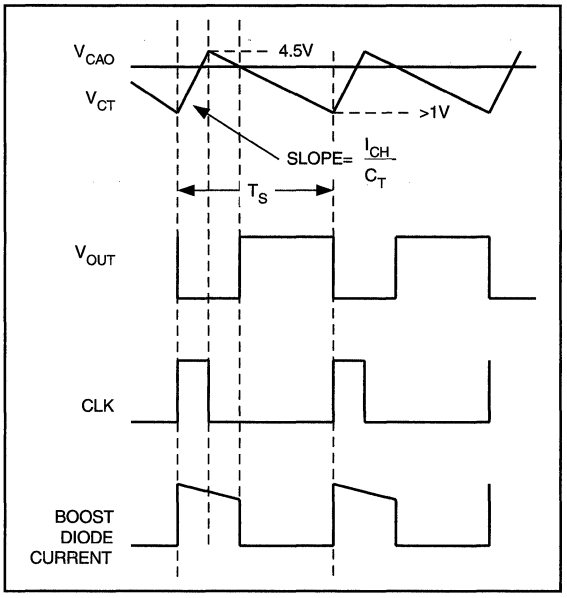


Figure 3c. Frequency foldback mode.

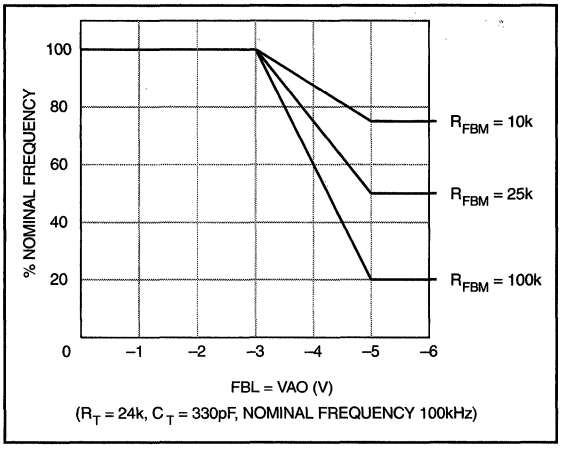


Figure 4. Frequency foldback characteristics.

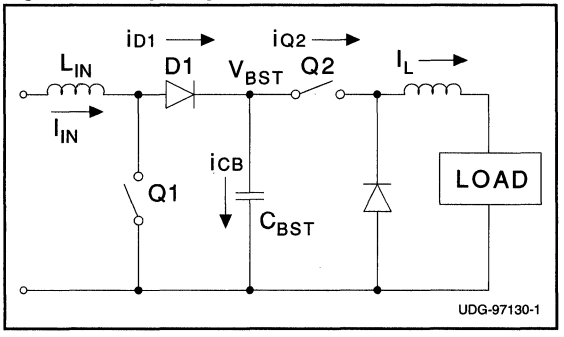


Figure 5. Simplified representation of a 2-stage PFC power supply.

Capacitor Ripple Reduction

For a power system where the PFC boost converter is followed by a DC-DC converter stage, there are benefits to synchronizing the two converters. In addition to the usual advantages such as noise reduction and stability, proper synchronization can significantly reduce the ripple currents in the boost circuit's output capacitor. Fig. 5 helps illustrate the impact of proper synchronization by showing a PFC boost converter together with the simplified input stage of a forward converter. The capacitor current during a single switching cycle depends on the status of the switches Q1 and Q2 and is shown in Fig. 6. It can be seen that with a synchronization scheme that maintains conventional trailing edge modulation on both converters, the capacitor current ripple is highest. The greatest ripple current cancellation is attained when the overlap of Q1 off-time and Q2 on-time is maximized. One method of achieving this is to synchronize the turn-on of the boost diode (D1) with the turn-on of Q2. This approach implies that the boost converter's leading edge is pulse width modulated while the forward converter is modulated with traditional trailing edge PWM. The UCC3858 is designed as a leading edge modulator with easy synchronization to the downstream converter to facilitate this advantage. Table 1 compares the I_{CBrms} for D1/Q2 synchronization as offered by UCC3858 vs. the $I_{CB_{rms}}$ for the other extreme of synchronizing the turn-on of Q1 and Q2 for a 200W power system with a V_{BST} of 385V.

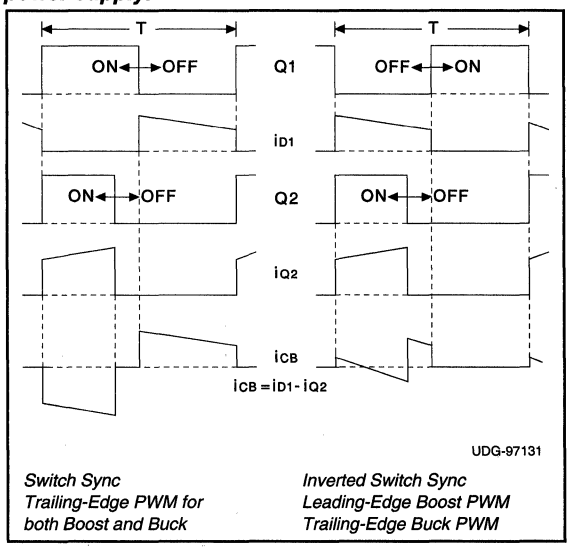


Figure 6. Timing waveforms for synchronization scheme.

APPLICATION INFORMATION (cont.)

Table I. Effects of Sychronization on Boost Capacitor Current

	V_{IN} = 85V		V_{IN} = 120V		V_{IN} = 240V	
D(Q2)	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
0.35	1.491A	0.835A	1.341A	0.663A	1.024A	0.731A
0.45	1.432A	0.93A	1.276A	0.664A	0.897A	0.614A

Table 1 illustrates that the boost capacitor ripple current can be reduced by about 50% at nominal line and about 30% at high line with the synchronization scheme facilitated by the UCC3858. The output capacitance value can be significantly reduced if its choice is dictated by ripple current or the capacitor life can be increased as a result. In cost sensitive designs where hold-up time is not critical, this is a significant advantage.

An alternative method of synchronization to achieve the same ripple reduction is possible. In this method, the turn-on of Q1 is synchronized to the turn-off of Q2. While this method yields almost identical ripple reduction and maintains trailing edge modulation on both converters, the synchronization is much more difficult to achieve and the circuit can become susceptible to noise as the synchronizing edge itself is being modulated.

Reference Signal (I_{MULT}) Generation

Like the UC3854 series, the UCC3858 has an Analog Computation Unit (ACU) which generates a reference current signal for the current error amplifier. The inputs to the ACU are (signals proportional to) instantaneous line voltage, input voltage RMS information and the voltage error amplifier output. Unlike prior techniques of RMS voltage sensing, UCC3858 employs a patent pending technique to simplify the RMS voltage generation and eliminate performance degradation caused by the prior techniques. With the novel technique (shown in Fig. 7), need for external two pole filter for V_{RMS} generation is eliminated. Instead, the IAC current is mirrored and used to charge an external capacitor (C_{RMS}) during a half cycle. The voltage on CRMS takes the integrated sinusoidal shape and is given by equation 3. At the end of the half- cycle, CRMS voltage is held and converted into a 4-bit digital word for further processing in the ACU. CRMS is discharged and readied for integration during the next half cycle. The advantage of this method is that the second harmonic ripple on the V_{RMS} signal is virtually eliminated. Such second harmonic ripple is unavoidable with the limited roll-off of a conventional 2-pole filter and results in a 3rd harmonic distortion in the input current signal. The dynamic response to the input line variations is also improved as a new V_{RMS} signal is generated every cycle.

$$V_{CRMS} = \frac{I_{AC\,pk}}{2 \bullet \omega \bullet C_{RMS}} \bullet (1 - \cos \omega t) \quad (3a)$$

$$V_{CRMS}(pk) = \frac{I_{AC\,pk}}{\omega \bullet C_{RMS}} \quad (3b)$$

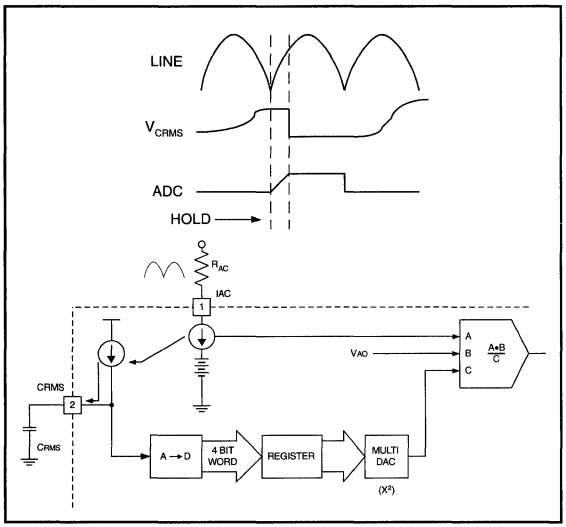


Figure 7. Novel circuit for RMS signal generation.

For proper operation, I_{ACpk} should be selected to be 100µA at peak line voltage. For universal input voltage with peak value of 265 VAC, this means R_{AC} = 3.6M. The noise sensitivity of the IC requires a small bypass capacitor for high frequency noise filtering. The value of this capacitor should be limited to 330pF maximum. The V_{CRMS} value should be approximately 1V at the peak of low line (80 VAC) to minimize any digitization errors. The peak value of V_{CRMS} at high line then becomes 3.5V. The desired C_{RMS} can be calculated from equation 3 to be 90nF for 50Hz line and 75nF for 60Hz line.

The multiplier output current is given by equation (4) with K=0.33.

$$I_{MULT} = \frac{(V_{VAO} - 1) \bullet I_{AC} \bullet K}{V_{CRMS}^{\,2}} \quad (4)$$

The multiplier peak current is limited to 200µA and the selected values for I_{AC} and V_{CRMS} should ensure that the current is within this range. Another limitation of the multiplier is that I_{MULT} can not exceed two times the I_{AC} current, limiting the minimum voltage on V_{CRMS}.

APPLICATION INFORMATION (cont.)

The discrete nature of the RMS voltage feedforward means that there are regions of operation where the input voltage changes, but the V_{RMS} value fed into the multiplier does not change. The voltage error amplifier compensates for this by changing its output to maintain the required multiplier output current. When the output of the ADC changes, there is a jump in the output of the error amplifier. There is a resultant shift in the foldback frequency if the converter is at light load. However, the impact of this change is minimal on the overall converter operation.

Another key consideration with the RMS voltage scheme is that it relies on the zero-crossing of the I_{AC} signal to be effective. At very light loads and high line conditions, the rectified AC does not quite reach zero if a large capacitor is being used for filtering on the rectified side of the bridge. In such instances, the feedforward effect does not take place and the controller functionality is lost. For UCC3858, the I_{AC} current should go below 10µA for the zero crossing detection to take place. It is recommended that the capacitor value be kept low enough for the light load operation or the feedforward be derived directly from the AC side of the input bridge as shown in the typical applications circuit.

Gate Drive Considerations

The gate drive circuit in UCC3858 is designed for high speed power switch drive. It consists of low impedance pull-up and pull-down DMOS output stages. When operating with high bias voltages, in order to stay within the SOA of the DMOS output stages, it is recommended that the gate drive current be limited to 0.5A peak with the use of external gate resistor. Please see the characteristic curve in Fig. 8 for determining the required external resistance.

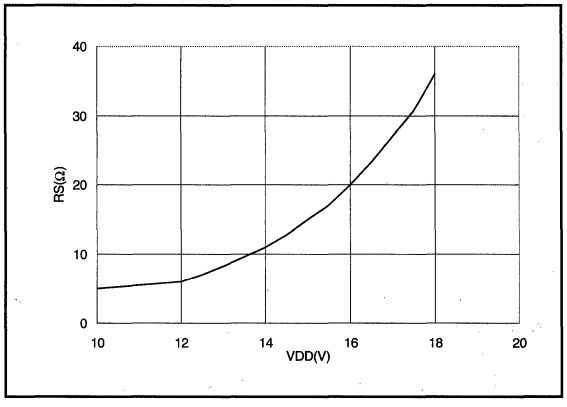


Figure 8. Required series gate resistance as a function of supply voltage.

Current Amplifier Set-up

The multiplier is set-up first by choosing the V_{RMS} range. The maximum multiplier output is at low line, full load conditions. The inductor peak current also occurs at the same point. The multiplier terminating resistor can be determined using equation 5.

$$R_{MULT} = \frac{IL_{PK} \bullet R_{SENSE}}{I_{MULT\,PK}} \quad (5)$$

The peak current limiting function provided by the UCC3858 is integrated into MOUT. The signal on MOUT is normally maintained at 0V as the ($I_{MULT} \bullet R_{MULT}$) cancels the voltage drop across the sense resistor with closed loop operation. During short circuit or transient startup conditions, the multiplier current can not fully cancel the voltage drop across RSENSE and the voltage at MOUT drops below 0V. The internal peak current limit is activated when MOUT drops below –0.5V. The peak current limit at any operating point is given by:

$$I_{LIM} = \frac{I_{MULT} \bullet R_{MULT} + 0.5}{R_{SENSE}} \quad (6)$$

The current amplifier can be compensated using previously presented techniques, (Application Note U- 134), summarized here. A simplified high frequency model for inductor current to duty cycle transfer function is given by:

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_O}{sL} \quad (7)$$

The gain of the current feedback path at the frequency of interest (crossover) is given by:

$$\frac{\hat{d}}{\hat{i}_L} = R_{SENSE} \bullet \frac{R_Z}{R_I} \bullet \frac{1}{V_{SE}} \quad (8)$$

Where V_{SE} is the ramp amplitude (p-p) which is 3.5V for UCC3858. Combining equations 7 and 8 yields the loop gain of the current loop and equating it to 1 at the desired crossover frequency can result in a design value for R_Z. The current loop crossover frequency selected using conventional trade offs. However, it should be ensured that the current-loop is stable at the minimum switching frequency under foldback conditions.

APPLICATION INFORMATION (cont.)

Voltage Amplifier Set-up

The voltage amplifier in UCC3858 is a transconductance type amplifier to allow output voltage monitoring for an overvoltage condition. The gain of the amplifier, given by $G_m \bullet Z_V$, should be chosen to achieve desired attenuation of the output second harmonic ripple (as described in previous Unitrode Application Notes U-134, U-159) while providing the best transient response.

APPLICATION INFORMATION (continued)

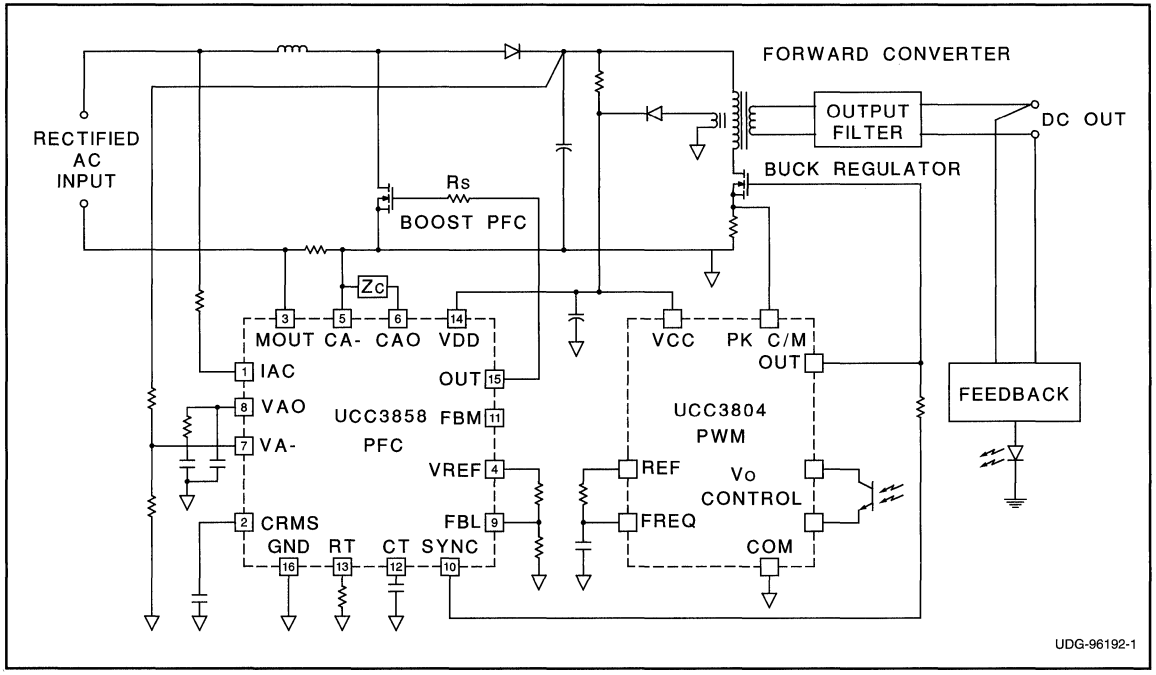


Figure 9. Use of the UCC3858 in a two stage converter to optimize performance.

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OPTIMIZING PERFORMANCE IN UC3854 POWER FACTOR CORRECTION APPLICATIONS

by Bill Andreycak

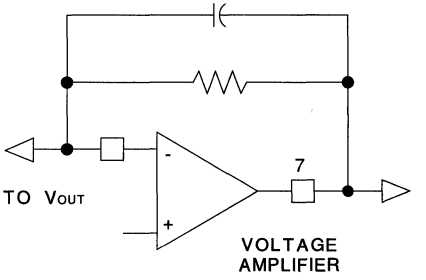
The performance of the UC3854 Power Factor Correction IC in the 250 watt application example has been evaluated using a precision PFC/THD instrument. The result was a power factor of 0.999 and Total Harmonic Distortion (THD) of 3.81%, measured to the 50th line frequency harmonic at nominal line and full load. Users should get similar results at these conditions. as well as over most line and load ranges. Summarized next are the circuit modifications which will improve the performance of most UC3854 PFC applications.

AMPLIFIER CLAMPS

There are a few ways to improve the obtainable power factor and performance in an application circuit. First, the current amplifier outputs should have a "clamp" circuit to limit the output voltage swing and prevent saturation of the amplifier. Without the clamps, overshoot of the current loop could result thus degrading optimal performance. The current amplifier should be clamped with a 7.5 volt zener diode from the output (pin3) back to the inverting input ISENSE(pin4). This example is shown in figure 1. Each amplifier is self protected with internal current limiting, however the IC power consumption may increase during this interval. This clamp is built in to the UC3854A.

CURRENT AMPLIFIER OFFSET VOLTAGE CANCELLATION

The current amplifier maximum input offset voltage is specified as +/- 4 millivolts. Failing to accommodate the offset voltage can causes a spike in the leading edge of the line current following the zero voltage crossing. The spike will occur until the current amplifier comes out of saturation and then resumes normal operation. The worst case offset voltage can be canceled by adding a small current to the biasing resistor (R3) located from I SENSE (pin 4) to ground. This cancellation current (1.1µA), when multiplied by the bias resistor value (3.9K) should be designed to provide the four millivolt offset.



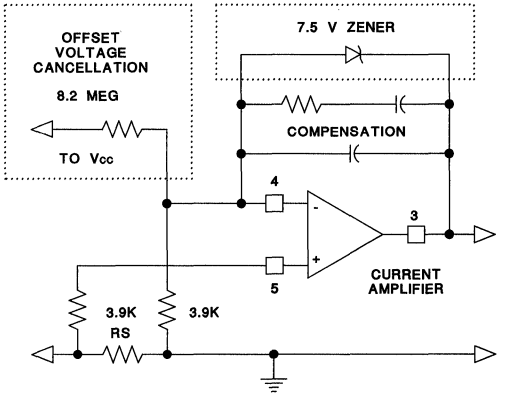


Figure 1.

This offset cancellation current should be obtained from the UC3854 supply voltage. Although a constant current source is optimal, a resistor from Vcc to the I SENSE input will provide acceptable results as shown also in figure 1. An 8.2 megohm resistor will develop a 1.1 microamp current into the 3.9 K ohm resistor used in the design example. This will generate a 4.28 millivolt offset at the worst case of operation where Vcc is 9 volts. It is adviseable to generate this bias from Vcc and not the UC3854 reference which is inactive until the undervoltage lockout threshold is reached. Bias cancellation circuits from the reference could cause the current amplifier to saturate before the devices crosses its UVLO turn-on threshold. This condition will increase the start-up current of the UC3854 above its 2 milliamp specification and may prevent start-up in certain off-line applications.

CURRENT SENSE AMPLITUDE

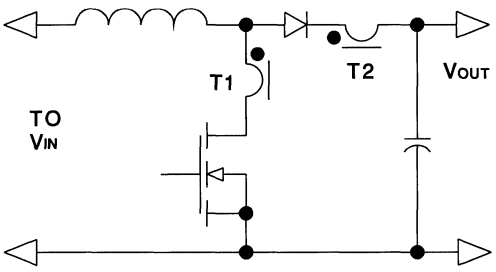
The current sense signal should be made as high as possible, and a one volt full scale signal is recommended. Since resistive sensing can cause high power loss many users elect to generate only 100 to 200 millivolts at full load. In comparison, ground noise and slight amplifier offset voltages represent a higher percentage of the total current sense signal. Best results are obtained with the one volt (max) input and lower performance could be incurred with lower current sense signals. especially at light loads and high line voltages. Alternatives to resistive current sense are given below .

CURRENT SENSE TECHNIQUES

An optional technique to resistive current sensing should be considered to reduce power loss in the current sense circuitry. Two current sense transformers can be installed to sum both the switch and diode currents which will recreate the actual inductor current as shown in figure 2. These transformers must be designed to operate over the full range of duty cycles for the PFC converter design which approaches 100% as the line voltages nears zero.

Another current sensing option is to use a DC current sense module or transformer which is typically Hall Effect based. Two application concerns are the cost and accuracy of this technique which may limit its usage to only specialized applications.

PFC BOOST CONVERTER



TRANSFORMER COUPLED CURRENT SENSE

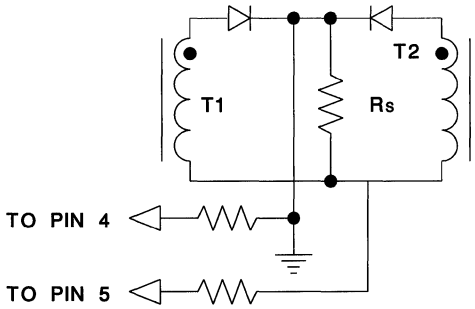
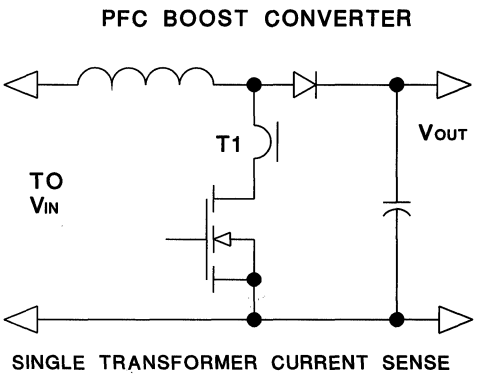


Figure 2.

A single current sense transformer in series with the PFC switch can also be used. This technique will require some additional circuitry to accurately reconstruct the primary current signal as shown in figure 3. Generating the inductor current signal while the switch is on is a simple task. The difficulty is in reconstructing the inductor current while the switch is off while no current is flowing in the current sense transformer.

Inductor current sensing can be simplified to use only one current sense transformer and a current sink circuit. The current sense signal is developed across resistor RI through diode DI while the switch is on. A second diode to the current sense transformer develops an identical voltage across capacitor CI as determined by the current sense resistor primary current and turns ratio. When the PFC switch turns off capacitor CI maintains the peak amplitude of the previous current sense signal.

Charge is removed by an ideal current sink circuit which lowers the capacitor voltage linearly during one switching cycle. The current is scaled to



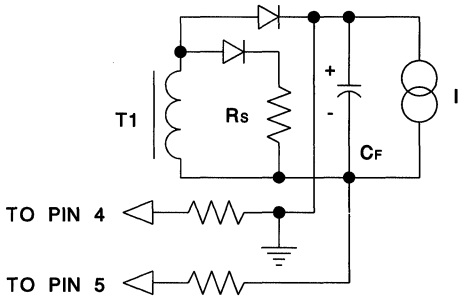


Figure 3.

discharge at the rate proportional to Vout minus Vin(t) divided by the inductor value, L. The input voltage (Vin) is constantly varying throughout the AC line cycle and so must the capacitor discharge current.

The circuitry shown in figure 4 will modulate the current sink inversely with the instantaneous line voltage. This will result in the correct discharge of capacitor C1 to reconstruct the actual inductor current. Polarity has been optimized for use with the UC3854 which requires a current sense signal below the ground reference. Another option is to develop a few volts of current sense signal to improve noise immunity and resistively divide this down to the one volt maximum input to the UC3854 controller.

Transistors QI through Q4 should be identical for best results. Transistors QI and Q3 are for temperature compensation of the base emitter junctions of Q2 and Q3. Emitter ballasting (50 to 100

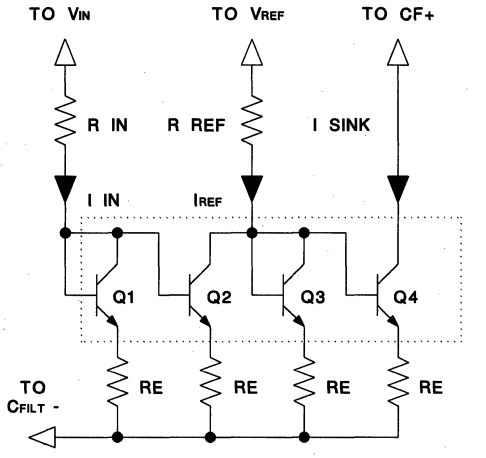
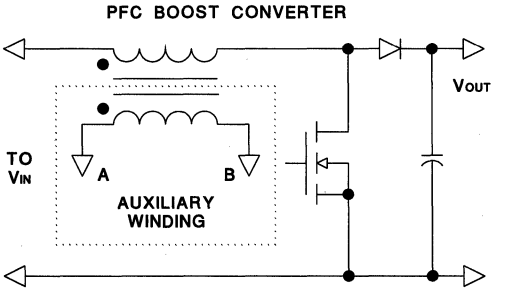


Figure 4.

mV) will also improve performance. The emitter currents of QI and Q2 should be similar and equal to Vin/Rin. This current is diverted away from the bases of Q3 and Q4 which limits the total range of sink current to the current sense filter capacitor, CFILT.

SCHOTTKY PROTECTION DIODES

Each pin of the UC3854 must be protected from negative voltages exceeding minus three hundred millivolts (-0.3V) maximum. In most applications, only three pins of the IC need external protection Schottky diodes. The gate drive output (pin 16) requires a 1N5820 3 amp Schottky diode to protect against parasitic inductive effects with high speed switching. The multiplier output (pin 5) and peak



current limit (pin 2) need Schottky diode protection during abnormal overcurrent conditions and during the initial inrush currents upon power-up. A 1N5817 Schottky diode will provide adequate clamping since

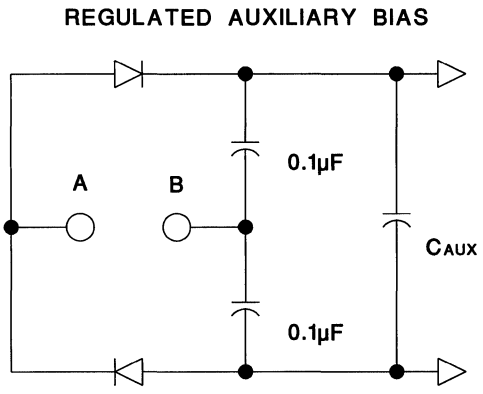


Figure 5.

the currents are low due to series resistors to the current sense circuitry.

REGULATED AUXILIARY SUPPLY

A secondary winding on the PFC boost inductor can be used to deliver a regulated auxiliary bias supply with few external components as shown in figure 5. Unlike more conventional and unregulated single diode or bridge rectifier techniques, this approach uses two diodes in a full wave configuration.

This arrangement develops two separate voltages across capacitors C1 and C2 each with 120 Hz components. However, when these two are summed at capacitor C3, the line variations are canceled, and a regulated auxiliary bias is obtained. The number of turns on the secondary winding will adjust the bias supply voltage. Additional windings on the boost inductor with similar rectification and filter circuitry can be used to deliver other semi-regulated isolated outputs.

UC 3854 POWER FACTOR CORRECTION EVALUATION KIT

LIST OF COMPONENTS

CAPACITORS (25 VDC)

C1 = 0.47 µF/250 VAC
C2 = 450 µF/450 VDC
C3 = 270 pF
C4 = 1 µF
C5 = NOT USED
C6 = 47 nF
C7 = 0.47 µF
C8 = NOT USED
C9 = 100 mF
C10 = 10 nF
C11 = 1 nF
C12 = 0.1 µF
C13 = 62 pF
C14 = NOT USED
C15 = 620 pF
C16 = 1 µF

DIODES

D1 =4 AMP/800VDC BRIDGE
D2 = UHVP806 FAST RECOVERY
D3 = 18 V ZENER
D4 = 1N5821 SCHOTTKY 3A
D5 = 1N4148
D6 = 1 AMP/100V BRIDGE
D7 = 1N5817 Schottky
D8 = 1N5817 Schottky

FUSE

F1 - 6A/250VAC FUSE

INDUCTOR

L1 = 1 milliHenry Inductor

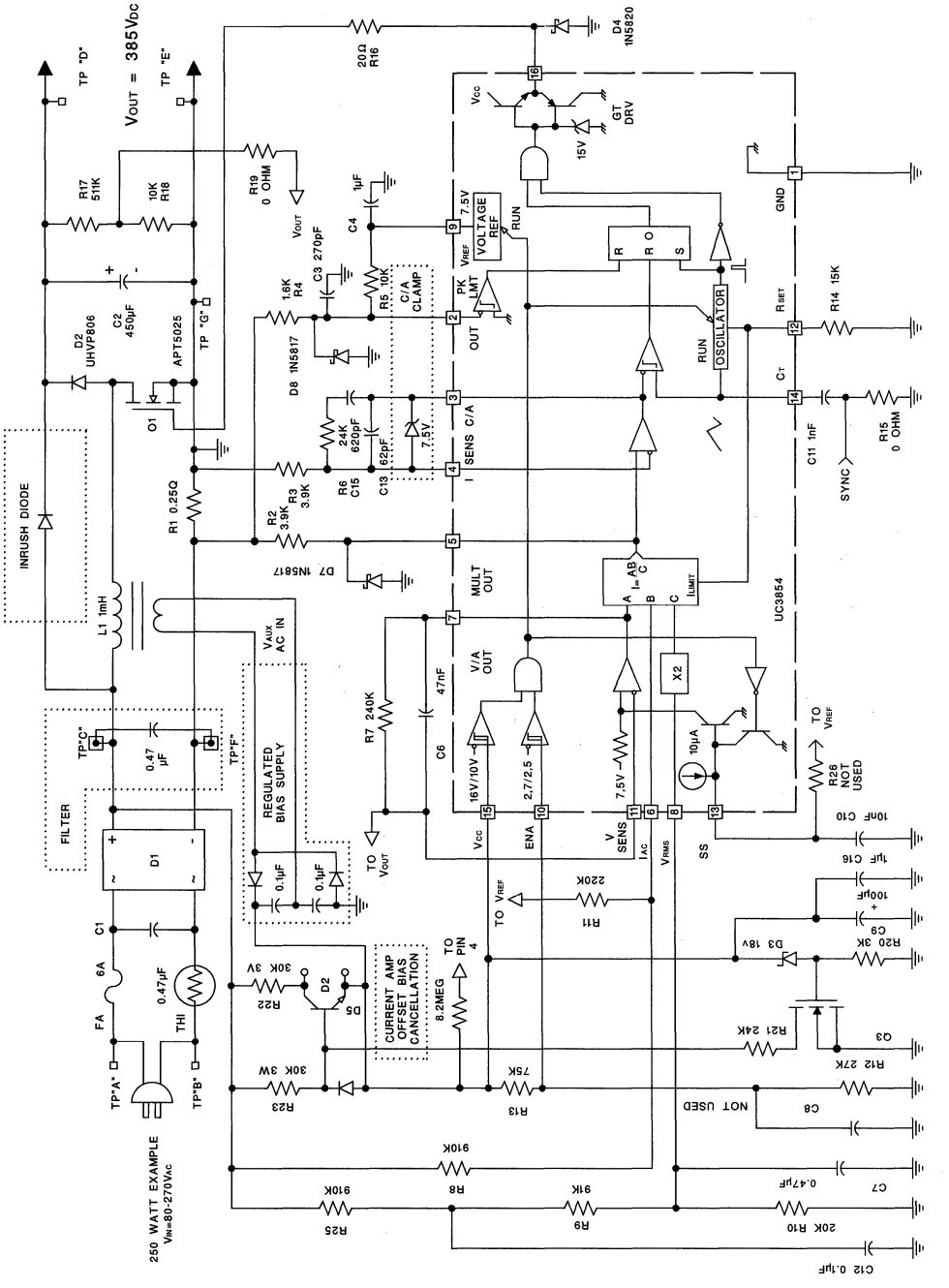
TRANSISTORS

Q1 = 500V/0.25 ohm NMOS FET
Q2 = 450V/0.5A NPN
Q3 = 50V/.5A NMOS FET

RESISTORS (1/2 WATT)

R1 - 0.25 ohm/5 WATT
R2 = 3.9 K
R3 = 3.9 K
R4 = 1.6 K
R5 = 10 K
R6 = 24 K
R7 =240 K
R8 = 910 K (400V)
R9 = 91 K
R10 = 20 K
R11 = 220 K
R12 = 27 K
R13 = 75 K
R15 = ZERO ohm
R20 = 3 K
R21 = 24 K
R22 = 30 K/3W
R23 = 470 K
R24 = USER SPECIFIED
R25 = 910 K (400V)
R26 = NOT USED (OPEN)

UC3854 Evaluation PC Board Schematic
250 Watt Power Factor Correction Application



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Design Note

EXTEND CURRENT TRANSFORMER RANGE

by PHILIP C. TODD

Transformers are used extensively for current sensing because they can monitor currents with very low power loss and they have wide bandwidth for good waveform fidelity. Current transformers perform well in applications with symmetrical AC currents such as push-pull or full bridge converter topologies. In single-ended applications, especially boost converters, problems can arise because of the need to accurately reproduce high duty factor, unipolar, waveforms. Unipolar pulses may saturate the current transformer and, if this happens, over current protection will be lost and, for current mode control, regulation will be lost and an over voltage condition will result.

The transformer core must be reset after each pulse so that the full range of the transformer will be available for the next pulse. Self reset of the current transformer is the most common techniques used but it has drawbacks. Self reset uses the energy stored in the current transformer core for reset and depends on the open circuit impedance of the current transformer to generate enough volt-seconds in a short period of time for reset. Current transformers operated above a 50% duty factor may not have enough stored energy to allow complete reset in the time available and this situation becomes worse as the duty factor approaches 100%.

The magnetizing inductance of the current transformer must be kept high because this determines the amount of droop the current waveform will exhibit over the pulse period. The higher the inductance the lower the droop will be. The waveform droop opposes slope compensation and should be kept to a minimum. High magnetizing inductance also means that the core stores very little energy which can be used to reset the core.

The current transformer turns ratio generally needs to be high to lower the power loss. The more turns put on the core, however, the greater the leakage inductance and the greater the parallel capacitance. The leakage inductance by itself is generally not a problem but it will limit the current rise and fall times. The parallel capacitance also limits the bandwidth of the current transformer but it is a greater problem during transformer reset. For the transformer to reset properly, all of the energy stored in the core must be removed. In self reset this energy must transfer from the magnetizing inductance to the parallel capacitance in a resonant manner. If the capacitance is too large, the resonant frequency will be too low and the magnetizing inductance will not be reset before the next pulse begins.

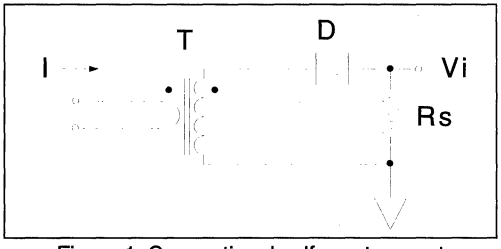

Figure 1: Conventional self-reset current transformer

Figure 1 shows a conventional current transformer circuit which uses self reset. The current I flowing in the primary, causes a current to flow through D and Rs to generate an output voltage proportional to Vc=IRs/N where N is the current transformer turns ratio. The problems discussed above occur during the reset interval when I=O. The core of T may not have enough energy to fully reset itself in the time available given the secondary capacitance of T plus the capacitance of D.

The problems with self reset of current transformers for unipolar pulse applications can be overcome with simple forced reset techniques derived from magnetic amplifiers. Duty factors above 90% are achievable with these techniques.

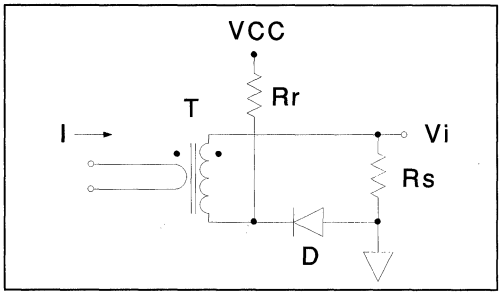

Figure 2: Current transformer with forced reset

Figure 2. shows the same circuit as Figure 1 configured for forced reset. The diode D has been moved from the high side of the transformer secondary winding to the ground side. This, of course, has no effect on the operation of the circuit and during the pulse this circuit behaves exactly as expected. During reset, however, Rr makes the circuit operation quite a bit different.

A current from Vcc through Rr can be much greater than the self reset current available from the magnetizing current of the transformer. This forcing current rapidly charges the parasitic capacitances and reverses the voltage on the secondary of the transformer. The applied volt-seconds can quickly reset the core so that high duty-factor operation is possible.

The forced reset may be high enough to drive the current transformer into saturation and this is an acceptable practice because the core will be saturated in the opposite direction (i.e. full reset) from the current pulse to be measured. This can be beneficial in some applications as it doubles the number of volt-seconds available from the transformer.

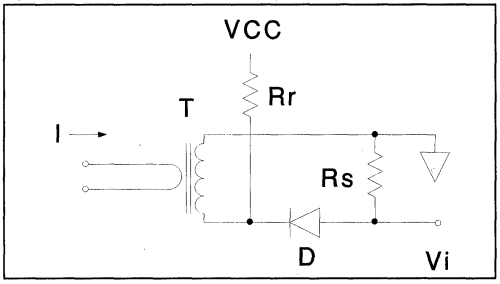

Figure 3: Negative output current sense

In some applications it may be desirable to generate a negative voltage from the current transformer. This can be accomplished without a negative voltage source to reset the transformer. Figure 3 shows the configuration. In this circuit there will be an error because the reset current subtracts from the sense current in Rs during the pulse. Care must be taken to minimize this effect.

There are other circuit configurations which are possible to force reset of the current transformer. Switches may be used to switch the reset current on and off. Additional windings or center tapped windings may be used also. Many circuits are possible and may provide a specific improvement at the expense of complexity. The circuits shown here are the simplest available and illustrate the basic concept.

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UC3854A and UC3854B Advanced Power Factor Correction Control ICs

by Bill Andreycak

The UC3854A and UC3854B Power Factor Correction (PFC) control ICs are advanced versions of the industry standard UC3854. The new devices are pin-for-pin compatible with the original version and feature numerous improvements. The UC3854A IC can be used in most existing UC3854 PFC designs with no modifications to the printed circuit board. New PFC preregulator designs and upgrades of existing ones can realize enhanced performance and reduced parts count with minimal design effort.

Specification Differences :

Parameter	UC3854	UC3854A	UC3854B
Supply Current, Off	2.0mA max.	400µA max.	400µA max.
Supply Voltage Vcc	35V max.	22V max.	22V max.
Vcc Turn-on threshold	16V typ.	16V typ.	10.5V typ.
Vcc UVLO hysteresis	6V typ.	6V typ.	0.5V typ.
Current Amplifier Bandwidth	1 MHz typ.	5 MHz typ.	5 MHz typ.
Current Amplifier offset	+4mV, -4mV max.	+0mV, -2mV max.	+0mV, -2mV max.
MULTOUT voltage (high)	2.5V typ.	5V typ.	5V typ.
Multiplier Gain tolerance	not specified	-0.9 to -1.1	-0.9 to -1.1
ENABLE propagation delay	not specified	300ns typ.	300ns typ.

Other Improvements and Changes - Non Specified:

VSENSE Input	7.5V	3.0V	3.0V
IAC voltage	6V typ.	0.5V typ.	0.5V typ.
Voltage Amplifier clamp	none	internal	internal
Current Amplifier clamp	none	internal	internal
VREF "good" circuitry	none	internal	internal

Application Information:

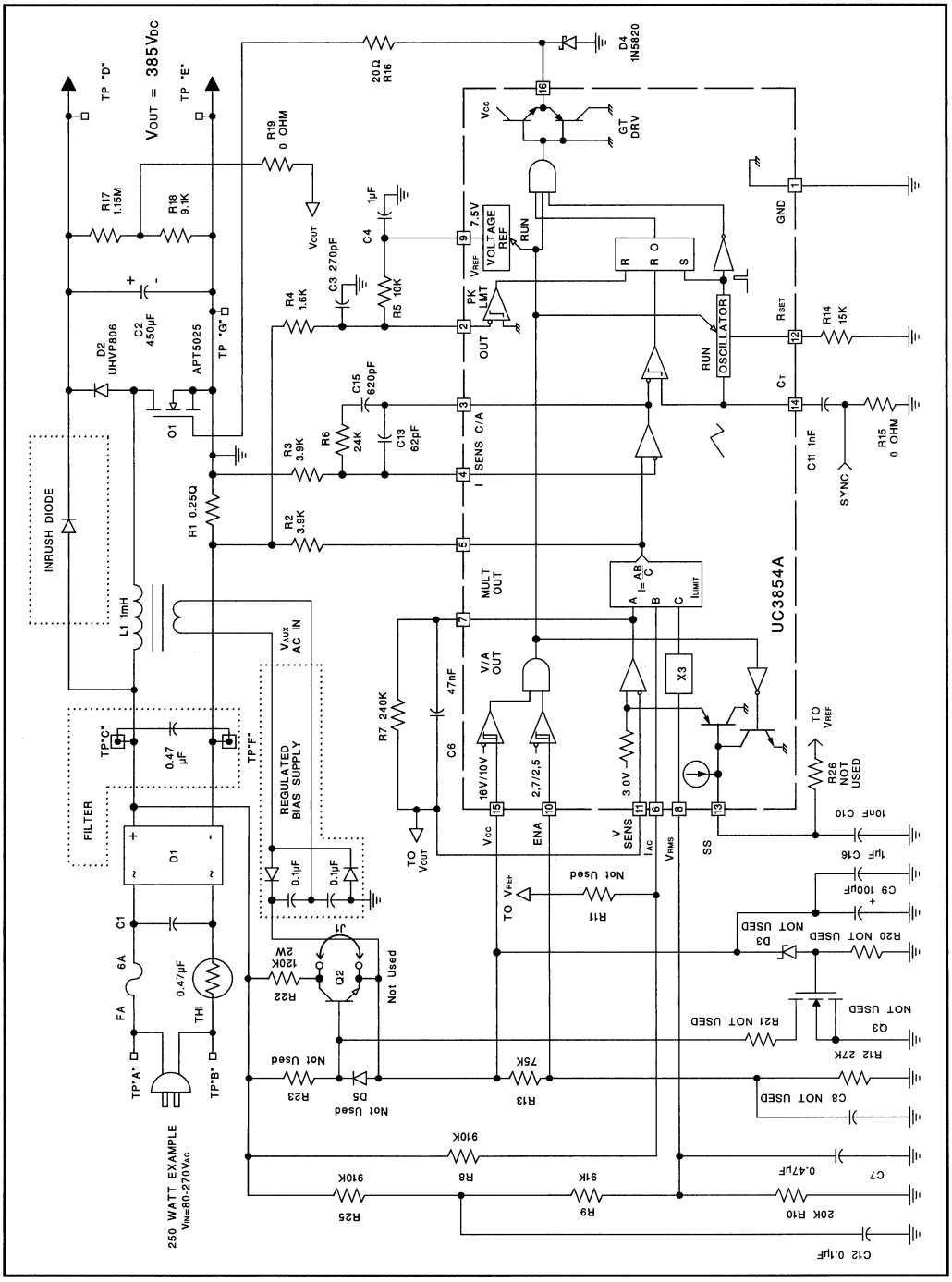
Converting an existing PFC design from the UC3854 to use the UC3854A or UC3854B device will eliminate five components from the control circuit. These are: one diode used to clamp the voltage amplifier output, a zener diode used to clamp the current amplifier output, one resistor to offset the bias current from the 6 volt amplitude of the IAC node, one resistor from Vcc to the current amplifier input to accommodate the worst case +4mV offset voltage, and a Schottky diode to clamp the overcurrent protection (PKLMT) input from going far below ground during power-up of the PFC preregulator. The output voltage divider feedback resistor value from VSENSE to ground must be lowered to accommodate the change in the amplifier's reference voltage from 7.5V to 3.0V. In most applications, existing production printed circuit boards do not have to be modified to take advantage of the newer devices. Locations used for the five components can remain on the boards but do not need to be populated.

For further application information consult Unitrode Application Note U-134 and Design Note DN-39D, or contact a Field Applications Engineer.

UC3854A EVALUATION BOARD LIST OF MATERIALS

C1	0.47µF / 300 VAC "X" TYPE
C2	450µF / 450 VDC ELECTROLYTIC
C3	270pF / 16 VDC
C4	1µF / 16 VDC CERAMIC
C6	0.047µF / 16 VDC CERAMIC
C7	0.47µF / 16 VDC CERAMIC
C9	100µF / 35 VDC ELECTROLYTIC
C10	0.01µF / 35 VDC CERAMIC
C11	1µF / 16 VDC CERAMIC
C12	0.1µF / 63 VDC POLY
C13	62pF / 16 VDC CERAMIC
C15	620pF / 16 VDC CERAMIC
C16	1µF / 35 VDC CERAMIC
C*	ADD A 0.47µF / 300VAC "X" CAP BETWEEN TP"C" AND TP"F"
D1	600 V / 6A BRIDGE RECTIFIER
D2	600 V / 8A VERY FAST RECOVERY RECTIFIER (trr35ns)
D4	20 V / 3A SCHOTTKY, 1N5820
D6	40 V / 1A BRIDGE RECTIFIER
F1	6A / 300 VAC FUSE
J1	JUMPER WIRE, AWG#22
L1	1mH INDUCTOR (SEE APPLICATION NOTE U-134)
Q1	500 V, 0.25 OHM N CHANNEL MOSFET / APT5025
R1	0.25 OHM, 5 WATT NON-INDUCTIVE
R2	3.9k, 1/2 W
R3	3.9k, 1/2 W
R4	1.6k, 1/2 W
R5	10k, 1/2 W
R6	24k, 1/2 W
R7	240k, 1/2 W
R8	1MEG, 1/2 W
R9	91k, 1/2 W
R10	20k, 1/2 W
R12	27k, 1/2 W
R13	75k, 1/2 W
R14	15k, 1/2 W
R15	JUMPER WIRE, AWG#22
R16	20 OHM, 1/2 W
R17	1.15 MEG, 1/2 W, 1% TOLERANCE
R18	9.1k, 1/2 W, 1% TOLERANCE
R19	JUMPER WIRE, AWG#22
R22	120k, 2 WATT
R23	910k, 1/2 W
R24	USER DETERMINED BY AUXILIARY SUPPLY WINDING
TH1	THRERMISTOR, N.T.C., 6 AMP / 500V RATING
U1	UC3854A PFC CONTROL IC
NOT USED : C5, C8, C14, D3, D5, Q2, Q3, R11, R20, R21, R23, R26	

UC3854A Evaluation PC Board Schematic 250 Watt Power Factor Correction Application



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Design Note

Unitrode - UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends

by Laszlo Balogh

This design note focuses on one of the major improvements introduced to the industry standard UC3854 high power factor boost controller. The new UC3854A/B versions eliminated the need for external components to clamp the voltage and current error amplifier outputs and optimized the voltage levels of some of the sense circuitry. All of these issues are already covered by DN-39 design note (present release is version E). The following aspects were expressed implicitly, in previous literature, and are now described in further details.

What makes intelligent power limiting possible with the UC3854A/B and with the newer UC3855A/B ZVS high power factor controllers, is that the maximum value of the multiplier output current is not directly related to the current of the R_{SET} resistor any more.

Instead, it is limited to be equal or smaller than twice the instantaneous value of the I_{AC} current. This new feature provides a very delicate and effective way to limit input power to the power factor corrector front-end while the converter still maintains a sinusoidal input current waveform. It has to be emphasized here that the power limiting scheme of the UC3854A/B does produce sinusoidal input current waveform even if the load is a negative impedance, like DC-DC converters. In these cases, special care has to be taken to guarantee that the output voltage of the boost power factor corrector is greater than the peak value of the input line voltage at all operating equilibrium. This can be insured by setting the power limiting of the DC-DC converter below the maximum power handling capability of the PFC stage.

In order to establish a straightforward design procedure for the multiplier setup, first a basic relationship should be shown. The ratio of the multiplier output current, (I_{MO}) and the I_{AC} current is constant within one cycle of the AC input because:

$$I_{AC}(t) = \frac{V_{RMS} \bullet \sqrt{2} \bullet \sin(\omega \bullet t)}{R_{AC}} \quad (1)$$

and

$$I_{MO}(t) = \frac{I_{AC}(t) \bullet (V_{EA} - 1.5)}{K \bullet (A \bullet V_{RMS})^2} \quad (2)$$

where,

V_{RMS} is the RMS value of the AC input voltage;

V_{EA} is the voltage error amplifier saturation voltage (V_{OH});

K is the multiplier constant (K = 1);

A is the divider ratio to the V_{RMS} pin of the IC.

The ratio of $I_{MO}(t)$ to $I_{AC}(t)$ is given as:

$$R = \frac{I_{MO}(t)}{I_{AC}(t)} = \frac{V_{EA} - 1.5}{K \bullet (A \bullet V_{RMS})^2} \quad (3)$$

which is determined only by the RMS value of the input voltage and stays constant within one line cycle.

In the case of a well executed design, the ratio will be equal to two - right at the minimum input voltage where the rated output power is still expected to be delivered. Figure 1 shows the optimal ratio of I_{MO} and I_{AC} as a function of the

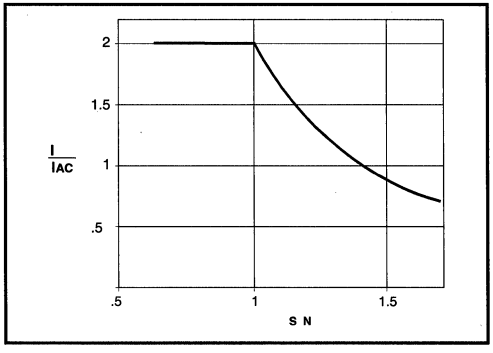

Figure 1. Ideal $\frac{I_{MO}}{I_{AC}}$ Ratio

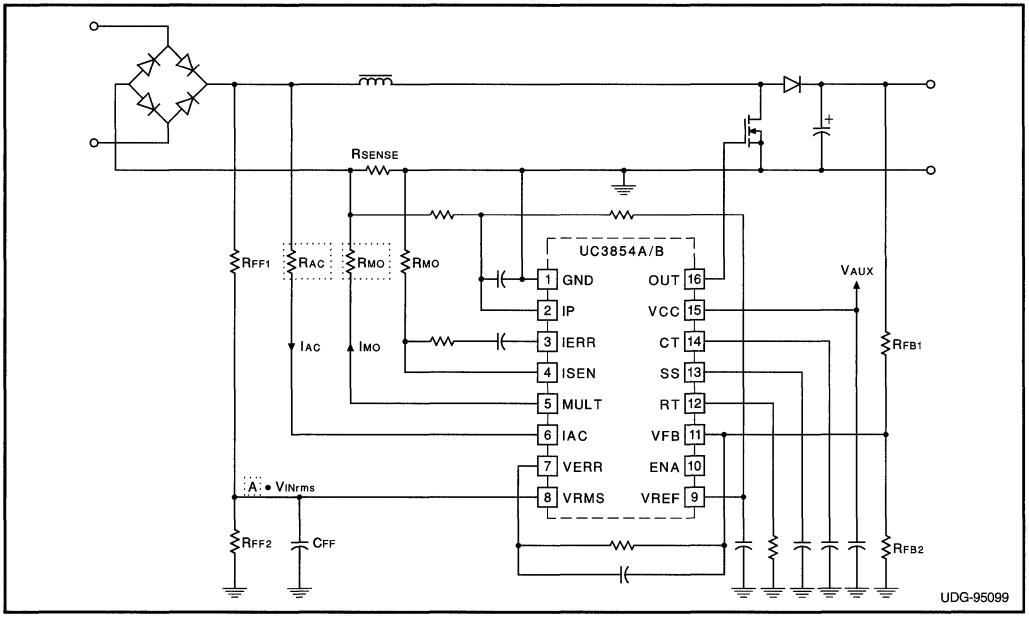

Figure 2. Multiplier Set Up Components in a Typical PFC Application

normalized input voltage. The horizontal axis of the graph is normalized for the minimum line voltage where full power can be obtained. For values below unity the converter will work in power limited mode.

To achieve precise power limiting the highlighted components of Figure 2 have to be calculated.

1. From the maximum peak input voltage and the highest allowable I_{AC} value calculate R_{AC}.

$$R_{AC} = \frac{V_{RMSmax} \bullet \sqrt{2}}{I_{ACmax}} \qquad (4)$$

where $I_{ACmax} \leq 600\mu A$ is given in the datasheet.

2. The factor "A" of equation (2) can be determined from the specified minimum input voltage value where the circuit has to supply full rated power. At that point, the voltage error amplifier output (V_{EA}) is about to saturate, and I_{MO} shall be at its theoretical maximum which is 2 • I_{ACmax}. The required value of "A" can be expressed from (3) using the conditions previously stated:

$$A = \frac{\sqrt{2.25}}{V_{RMSmin}} \qquad (5)$$

Now every parameter is given for equation (2), and I_{MO} is known for all operating conditions.

3. The next step is to calculate the peak value of the multiplier current (I_{MOmax}) at the minimum input voltage (V_{RMSmin}). From combining (2), (4) and (5),

$$I_{MOmax} = \frac{V_{RMSmin} \bullet \sqrt{2} \bullet (V_{EA} - 1.5)}{K \bullet R_{AC} \bullet 2.25} \qquad (6)$$

4. I_{MOmax} will define the maximum value of the input current (I_{INpeak}) which occurs at the peak of the minimum line voltage, (V_{RMSmin}) and at maximum load. The required peak input current is given as:

$$I_{INpeak} = \frac{P_{LIMIT}}{V_{RMSmin} \bullet \eta} \bullet \sqrt{2} \qquad (7)$$

The relation between I_{MOmax} and I_{INpeak} is defined by the two resistors R_{SENSE} and R_{MO} according to:

$$I_{INpeak} = I_{MOmax} \bullet \frac{R_{MO}}{R_{SENSE}} \quad (8)$$

5. The last parameter to be calculated is the value of R_{MO} from equations (6), (7) and (8), assuming that R_{SENSE} is already selected based on the allowed power dissipation of that resistor.

$$R_{MO} = \frac{2.25 \bullet K \bullet P_{LIMIT} \bullet R_{AC} \bullet R_{SENSE}}{V^2_{RMSmin} \bullet \eta \bullet (V_{EA} - 1.5)} \quad (9)$$

After all design parameters are defined, the normalized input RMS current values and the normalized input power can be calculated as the functions of the normalized input voltage.

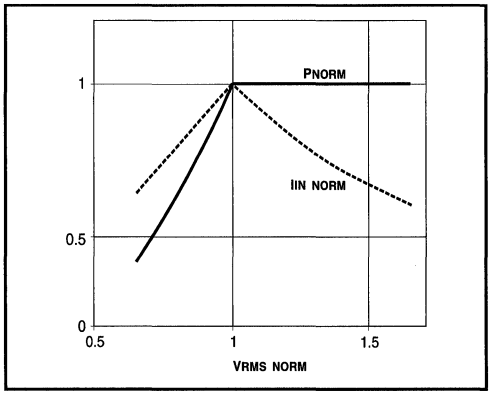

Figure 3. Power Limit and Maximum Input Current Values as a Function of Input Voltage (All Normalized)

As Figure 3 demonstrates, exact, and constant power limiting can be realized by the UC3854A/B high power factor controller ICs for the entire input voltage range. That is caused by the input voltage feedforward term in the multiplier equation, (2).

Design Example

The following example is to illustrate how to execute the procedure described above. The design example has the following start up parameters:

V_{IN} = 70 . . . 132 V_{ACRMS}	
V_{INmin} = 90 V_{ACRMS}	(where full output power still obtainable)
P_{OUT} = 250W	(power limit of the load converter)
P_{LIMIT} = 275W	(set PFC power limit 10% above load converter)
η = 0.95	(expected efficiency)

For optimum results follow the step-by-step design guide given below:

Step 1.

$$R_{AC} = \frac{132 \bullet \sqrt{2}}{600 \bullet 10^{-6}} = 311.1 \bullet 10^3$$

R_{AC} = 330kΩ

Step 2.

$$A = \frac{\sqrt{2.25}}{90} = 0.01667$$

A = 16.67mV/V_{RMS}

Step 3.

$$I_{MOmax} = \frac{90 \bullet \sqrt{2} \bullet (6 - 1.5)}{1 \bullet 330 \bullet 10^3 \bullet 2.25} = 771.4 \bullet 10^{-6}$$

I_{MOmax} = 771.4μA

Step 4.

$$I_{INpeak} = \frac{275}{90 \bullet 0.95} \bullet \sqrt{2} = 4.55$$

I_{INpeak} = 4.55A

Step 5.

Assume the maximum power dissipation of the current sense resistor P_{RS} = 0.5W, then:

$$R_{SENSE} = \frac{P_{RS} \bullet V_{INmin}^2 \bullet \eta^2}{P_{OUT}^2} \quad (10)$$

$$R_{SENSE} = \frac{0.5 \bullet 90^2 \bullet 0.95^2}{275^2} = 0.04833$$

R_{SENSE} = 47mΩ

Step 6.

$$R_{MO} = \frac{2.25 \bullet 1 \bullet 275 \bullet 330 \bullet 10^3 \bullet 47 \bullet 10^{-3}}{90^2 \bullet 0.95 \bullet (6 - 1.5)}$$

$$= 277.1$$

R_{MO} = 270Ω

The design just completed will exhibit the required power limiting characteristics for the entire operating input voltage range. The described calculations can be easily programmed as it is shown in the Mathcad® worksheet in the Appendix.

APPENDIX

This MathCAD file calculates the power limiting characteristic of the UC3854A/B and UC3855A/B high power factor controllers for wide input voltage range application.

INPUT PARAMETERS:

$V_{INmin} := 70$	Input voltage (RMS) value, where the controller starts operating.
$V_{INlim} := 90$	Minimum input voltage (RMS) where the circuit must deliver its rated output power.
$V_{INmax} := 270$	Maximum input voltage (RMS).
$P_{LIM} := 275$	110% of the load power requirements.
$\eta := 0.93$	Expected efficiency of the PFC stage.
$I_{ACmax} := 600 \cdot 10^{-6}$	Maximum value of the I_{AC} current as defined in the datasheet.
$V_{EAsat} := 6$	Output voltage of the voltage amplifier when it is saturated high.
$K := 1$	The multiplier constant as it is given in the datasheet.
$R_S := 0.047$	The current sense resistor value, defined previously based on the acceptable maximum power dissipation.

DESIGN PROCEDURE:

Step 1. Estimate R_{AC} resistance:

$$R_{ACest} = \frac{V_{INmax} \cdot \sqrt{2}}{I_{ACmax}} \qquad R_{ACest} = 6.364 \cdot 10^5$$

Pick the closest **higher** standard value:

$R_{AC} := 6.8 \cdot 10^5$

Step 2. Divider ratio of the input RMS voltage to the V_{RMS} pin (8) of the IC.

$$A := \frac{\sqrt{2.25}}{V_{INlim}} \qquad A = 0.017 \qquad [mV/V_{RMS}]$$

Step 3. Determine the maximum multiplier output current. It occurs at the peak of the mains cycle at the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{MOmaxpk} := \frac{V_{INlim} \cdot \sqrt{2} \cdot (V_{EAsat} - 1.5)}{K \cdot R_{AC} \cdot 2.25}$$

$I_{MOmaxpk} = 3.744 \cdot 10^{-4}$

Step 4. Calculate the highest peak input current value as defined by the rated output power and the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{INpk} := \frac{P_{lim} \cdot \sqrt{2}}{V_{INlim} \cdot \eta} \qquad I_{INpk} = 4.646$$

Step 5. Estimate R_{MO} resistance.

$$R_{MOest} := \frac{I_{INpk}}{I_{MOmaxpk}} \cdot R_S \qquad R_{MOest} = 583.367$$

Pick the closest **lower** standard value:

$R_{MO} := 560$

DESIGN VERIFICATION:

$Step := 20$ Number of points to calculate.

$i := 0..step$ Step variable.

Input voltage range definition:

$$V_{INRMS}(i) := V_{INmin} + \frac{V_{INmax} - V_{INmin}}{step} \cdot i$$

I_{AC} current as a function of the input voltage:

$$I_{ACRMS}(i) := \frac{V_{INRMS}(i)}{R_{AC}}$$

I_{MO} current as defined by the input voltage and applying the $I_{MO} < 2 \cdot I_{AC}$ limit.

$$I_{MORMSest}(i) := \frac{I_{ACRMS}(i) \cdot (V_{EAsat} - 1.5)}{K \cdot (A \cdot V_{INRMS}(i))^2}$$

$I_{MORMS}(i) := \text{if}(I_{MORMSest}(i) > 2 \bullet I_{ACRMS}(i), 2 \bullet I_{ACRMS}(i), I_{MORMSest}(i))$

Calculating the maximum input RMS current level limited by the multiplier output current.

$$I_{INRMS}(i) := I_{INRMS}(i) \bullet \frac{R_{MO}}{R_S}$$

The power limit of the power factor corrector.

$P_{INmax}(i) := V_{INRMS}(i) \bullet I_{INRMS}(i)$

Graphical representation of the obtained data:

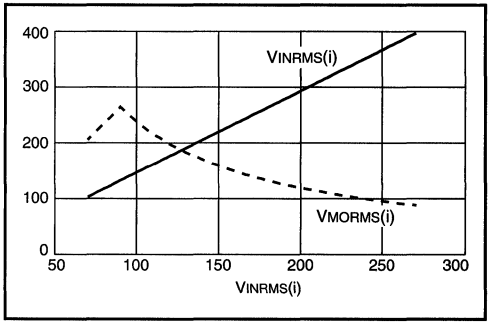

Figure 4. The I_{AC} and I_{MO} currents (in μAmps) as a function of the RMS input voltage.

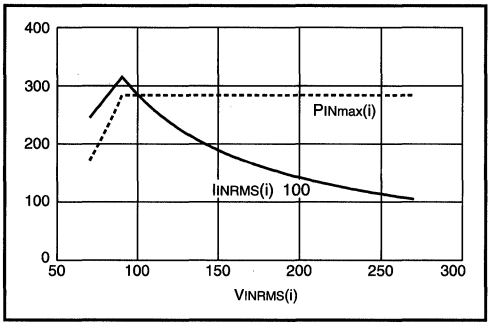

Figure 5. Input power [W] and input RMS current [A] (multiplied by 100 to fit the same scale) as a function of input RMS voltage.

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Overcurrent Shutdown with the UC3853

by James Noon

Boost converters are susceptible to large inrush currents at startup and with step changes in VLINE. This is due to the fact that the output capacitor is connected directly to the input through the boost diode. Therefore, controlling the boost MOSFET cannot limit the input current. However, the MOSFET can be protected from the large inrush or overcurrent by forcing the switch off when an overcurrent occurs. This is accomplished with the UC3853 by sensing when an overcurrent has occurred and forcing the FB pin high. Since the UC3853 incorporates a transconductance amplifier for the voltage loop, the FB pin has high input impedance and can easily be pulled up by external circuitry. The UC3853 uses this pin to both regulate the voltage loop and sense when an overvoltage occurs. If the FB pin is forced above 3.15V nominal, the gate drive will be terminated. By tying the overcurrent shutdown circuit into this pin, overcurrent protection can be achieved.

A circuit for providing overcurrent shutdown is shown below (the reference designators correspond with the demo board schematic). The circuit works by having R15 and R14 set the threshold level where the circuit is activated. For example, if R15 = R14, at approximately 1.4V across RSENSE Q2 will turn on. Once Q2 turns on, Q3 will be biased on. R17 and R16 set the bias for Q3 (we're assuming negligible drop across Q2 and R14 as a first approximation). Once Q3 turns on the FB pin will be driven high. R18 is sized so that at minimum Vcc the voltage divider formed by R18 and the RVD1 gives greater than 3.15V at the FB pin.

The current limit is set by adjusting the voltage divider formed by R14 and R15 such that for the voltage across RSENSE that corresponds to the shutdown current, there is 0.7V across R15.

For more information on the UC3853 please refer to U-159, or contact your Field Application Engineer.

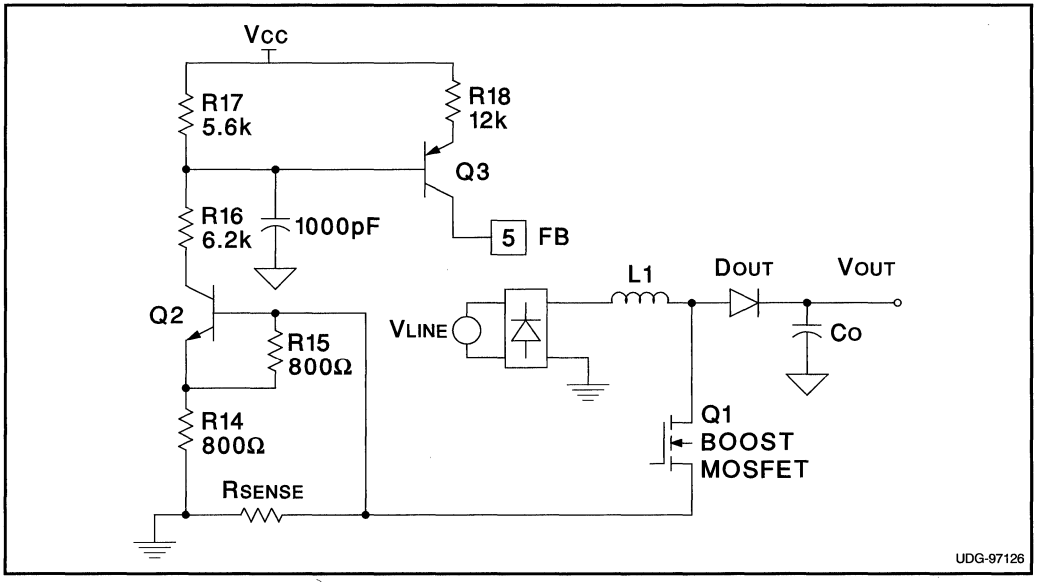

Figure 1.

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Design Note

UC3853 High Power Factor Preregulator IC, Evaluation Board, Schematic and List of Materials

by James Noon

Introduction

The UC3853 is an 8 pin, High Power Factor Preregulator Integrated Circuit. This demo board was designed for 100W, 75kHz operation over a universal input voltage range (80VAC to 270VAC). A complete explanation of the UC3853 operation as well as a detailed design procedure can be found in Unitrode Application Note U-159. A parts list and schematic diagram for the typical application circuit described in U-159 are shown below.

The power factor correction circuit is based on a boost circuit topology with average current mode control. The oscillator frequency is fixed internally to 75kHz. Although having only 8 pins, the UC3853 incorporates an inner average current loop along with input voltage feedforward and overvoltage shutdown.

AC Voltage Application

AC voltage should be applied across terminals P1. AC voltage should be applied only when some load is present across Vo and GND (P2).

Caution: *High voltage levels are present on the demo board whenever it is energized. Proper precautions must be taken when working with the board. The output capacitor has high levels of energy storage and it must be discharged before the load is removed.*

Reference Material

[1] Application Note U-159 *"Boost Power Factor Corrector Design With the UC3853"*

[2] Design Note DN-77 *"Over Current Shutdown with the UC3853"*

For more complete information, pin descriptions and specifications for the UCC3853 High Power Factor Preregulator IC, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

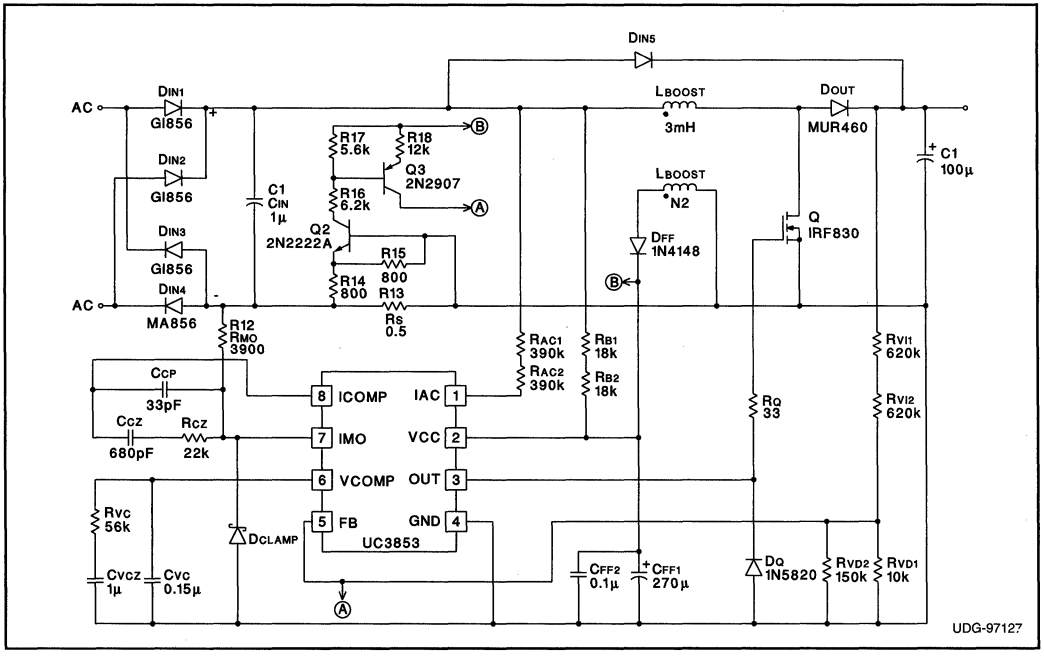

Figure 1. UCC3853 Evaluation Board Schematic

Reference Designator	Description	Manufacturer	Part Number
C_O	100µF, 450V, TSU Electrolytic Capacitor	Panasonic	
C_{IN}	1µF, 400V, Capacitor	Panasonic	ECQ-U2A105MV
C_{CZ}	680pF, 100V, Ceramic Capacitor		
C_{CP}	33pF, 100V N750, Ceramic Capacitor		
C_{VC}	0.15F, 100V, Ceramic Capacitor, X7R		
C_{VCZ}	1µF, 63V, Z5U, Ceramic Capacitor		
C_{FF1}	330µF, 50V, SU, Electrolytic Capacitor	Panasonic	
C_{FF2}	0.1µF, 63V, Z5U, Ceramic Capacitor		
D_{OUT}	600V, 8A, 19nS	International Rectifier	HFA08TB60
D_{OUT} (alternate)	600V, 8A, 28nS	Motorola	MURH860CT
D_{OUT} (alternate)	600V, 2.3A, 30nS	Philips	BYM26C
D_{IN}, D_{IN2}, D_{IN3}, D_{IN4}, D_{IN5}		General Instruments	GI856
D_{IN1}, D_{IN2}, D_{IN3}, D_{IN4}, D_{IN5} (Alternate)	600V, 3A, 200nS	Philips	BYW95C
D_Q, D_{IMO}	Schottky Rectifier, DO - 41		1N5819
D_{FF}	1A, 100V, 50nS, DO - 41, Rectifier		HER102
H_S	Heatsink	AAVID	529802B2500
F1	2AG submin. Fuse 3A		
F1	Fuse Clip		
L_{BOOST}	Inductor, with 220:25 turns, 3mH / 2A	Pulse Engineering	P0205
Q1	500V, N-Channel MOSFET	International Rectifier	IRF830
Q2	NPN General Purpose		MPS2222A
Q3	PNP General Purpose		MPS2907A
R_S	Wirewound , 0.5Ω/3W	Memcor-Truohm	SC3D
R_{AC1}, R_{AC2}	392k, 1% Metal Film		
R_{MO}	3.92k, 1% Metal Film		
R_{CZ}	22.1k, 1% Metal Film		
R_{VI1}, R_{VI2}	619k, 1% Metal Film		
R_{VD1}	10.0k, 1% Metal Film		
R_{VD2}	150k, 1% Metal Film	Yageo	
R_{B1}, R_{B2}	18k, 2W, Metal Film		
R_Q	33.2k, 1% Metal Film		
R14, R5	825k, 1% Metal Film		
R16	6.19k, 1% Metal Film		
R17	5.62k, 1% Metal Film		
R18	12.1k, 1% Metal Film		
R_{VC}	56.2k, 1% Metal Film		
P1, P2	Terminal Block		
U1	Unitrode 8-pin PFC controller	Unitrode	UC3853N

Table 1. UCC3853 Evaluation Board List of Materials

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UCC3858 "Energy Star" PFC Evaluation Board, Schematic, and List of Materials

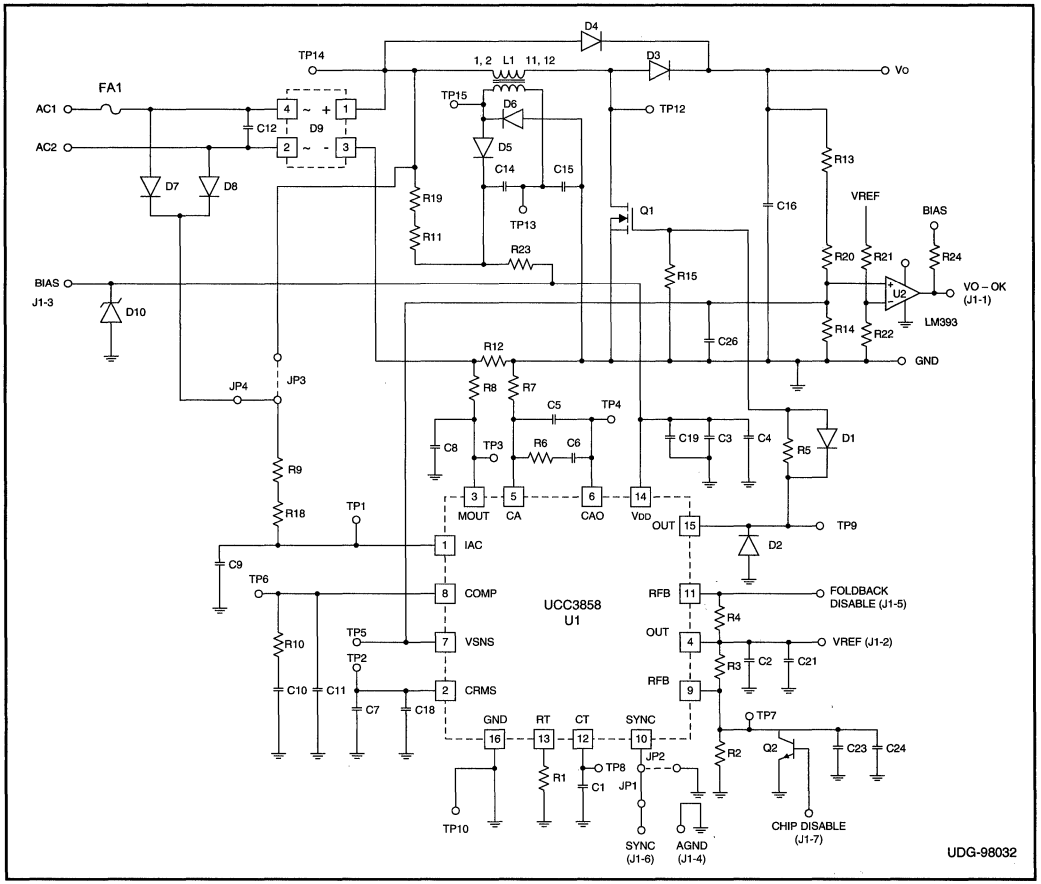
By Dhaval Dalal

Introduction

The UCC3858 provides all functions necessary for active power factor corrected preregulators which require high efficiency for low power operation. Its operation is similar to the previously designed Unitrode PFC preregulators with some added features. It has frequency foldback at light load operation for higher efficiency and leading edge modulation to allow better ripple cancellation on the boost output capacitor.

The UCC3858 demonstration board is designed to illustrate the performance of the IC in a 250W boost converter with power factor correction. The board is designed to handle a wide input operating voltage range (85-265 VAC) and a wide load range (5W-250W).

***Caution**: High voltage levels are present on the demo board whenever it is energized. Proper precautions must be taken when working with the board. The output capacitor has high levels of energy storage and it must be discharged before the load is removed.*



Operating Guidelines

The operating guidelines for the evaluation board are provided with reference to the schematic in Figure 1 and the parts list in Table 1.

Step 1. Bias Voltage Application

The demo board is shipped with self-biasing circuit enabled and bias voltage set at 16V. The board will become functional at approximately 90V RMS input when sufficient bias voltage develops. To use external bias voltage and remove self-biasing, R23 should be removed. The chip must be biased with a voltage between 10-18 V. On the demo board, the bias can be applied to J1-3 with respect to Ground (J1-4). For ideal performance ensure that VDD is maintained below 16V during the circuit operation.

For evaluating the demo board, apply external bias voltage first and ensure that the chip is operational. A valid VREF (7.5V) or a PWM signal on the Out pin (pin 15) can confirm the IC operation.

Step 2. Preset values and adjustments

If needed, the default settings of the board can be adjusted as follows.

The free running frequency of the oscillator is set at 92 kHz. If needed, the free running frequency can be adjusted by modifying R1 or C1.

Output voltage level is set at 375V nominal. It can be adjusted by changing R14.

The frequency foldback level is set to a load level of 75W and below. The foldback level can be altered by changing the resistive divider R3/R2.

The minimum switching frequency is set at 40 kHz, changing R4 will enable that to be adjusted.

If the foldback mode is not desired, pin 11 (J1-5) needs to be grounded.

Pulling J1-7 high can disable the chip operation. If not used, J1-7 should be held low to prevent noise susceptibility.

Vo-OK (J1-1) indicates that the output is above a set threshold (set by R21/R22).

Step 3. AC Voltage Application

AC voltage should be applied across terminals AC1 and AC2 after the chip operation has been verified. AC voltage should be applied only when some load is present across Vo and GND.

With the AC voltage within the input range, the output voltage should be regulated and the input current should track the input voltage shape with unity power factor. The operation of the circuit is verified over the line and load range and shows efficiency in 92% range. At lighter loads, there may be some distortion in the line current due to DCM operation. In the foldback mode, this distortion may be more pronounced as the available maximum duty cycle is reduced. At very light loads, the converter could go into pulse skipping mode - in the foldback mode, the pulse-skipping occurs at even lighter load.

Step 4. Synchronization

UCC3858 can be synchronized to a downstream converter for minimum ripple current on the bulk capacitor. A sync pulse can be applied to pin 10 of the IC (J1-6 on the board). To make synchronization work, move the jumper from JP2 position to JP1 position. The IC synchronizes to the leading edge of the incoming pulse and turns off the PWM output. PWM is turned on again when PWM comparator output goes high. This synchronized leading edge modulation scheme minimizes the ripple current on the bulk output capacitor (C16). Sync signal is TTL compatible, but can be as high as 14V. The sync frequency has to be higher than the free running frequency of the oscillator.

Debugging Hints

The demo board has been verified for operation over line and load range. However, the due to the complexity of the board some debugging may be required for a different operating environment/condition.

The Iac pin (pin 1) is sensitive to noise coupling. It has been adequately bypassed, but it may show irregular behavior if it is probed or is in a noisy environment. If this pin sees irregular behavior or current spikes near zero crossings, it can make the converter misbehave. Pin 2 can be monitored to detect if there are any missed or double pulses. It is essential that the IC be properly bypassed (VDD to GND) to minimize noise sensitivity. Putting the IC in a socket for evaluation or reducing the bypass capacitor C3 from 1μF could lead to irregular operation. In some situations, the sync pulse can inject noise into the system. In that case, it may help to slow down the rise time of the sync pulse. Other decoupling techniques (heavier bypassing on FBLVL pin) may also help.

While the demo board is primarily intended for use with an AC input, in some cases it may be necessary to evaluate it with DC input voltage. In these instances, the different RMS sensing scheme of the UCC3858 requires special handling. As described in the datasheet, the RMS sensing scheme requires a periodic zero crossing signal on the Iac pin (pin 1). With a DC input, Iac has to be manually pulsed to ground (at least twice) to clock in the voltage on Crms pin (pin 2) into the register for further processing. It also requires a resistive divider from the input voltage going into the Crms pin. With every change in input voltage, the Iac pulsing has to be repeated to ensure that the multiplier inputs are properly programmed.

Additional Information

For more information, pin description and specifications for the UCC3858 "Energy Star" PFC, please refer to the datasheet or contact your Unitrode Field Applications Engineer.

Reference Designator	Part Description	Manufacturer	Part Number
C1	330pF, 63V, Ceramic capacitor, CT		
C2	0.47μF, 50V, Film capacitor, bypass		
C3	1μF, 50V, Film Capacitor, bypass		
C4	100 μF, 25V, Aluminum Capacitor, bias		
C5	47pF, 100V, Ceramic Capacitor		
C6, C9	270pF, 63V, Ceramic Capacitor		
C7	82nF, 50V, Film Capacitor		
C8	47pF, 100V, Ceramic Capacitor		
C10	2.2μF, 63V, Z5U, Ceramic Capacitor		
C11	0.39μF, 50V, Film Capacitor		
C12	1.5 μF, 400V, Metal film Capacitor		
C14, C15	1μF, 50V, Film Capacitor		
C16	330μF, 450V, Output Aluminum Capacitor		
C18	82pF, 100V, Ceramic Capacitor		
C19, C21, C23	4.7μF, 25V, Tantalum Capacitor		
C24	.68μF, 50V, Film Capacitor		
C26	150 pF, 50V, Ceramic Capacitor		
C13, C17, C20, C22, C25	Not used		
D1	Not used		
D2, D5, D6	30V, 1A Schottky Diode		1N5818
D3	600V, 8A Ultrafast Diode	International Rectifier	HFA08TB60
D4	600V, 6A Diode - 400A Surge	General Instrument	GI756CT
D7, D8	600V, 1A, Fast Recovery Rectifier		1N4937
D9	6A, 600V Bridge Rectifier		PB66
D10	18V, 0.5W Zener		1N5248
FH1,FH2	Fuse Holders		
FA1	Fuse, 6A, 250VAC		F124
L1	1mH, 5.5A pk, Boost choke, 18:1 turns ratio	Coiltronics	CTX08-13679-02

Table 1. Parts List

Reference Designator	Part Description	Manufacturer	Part Number
Q1	500V, 0.4Ω MOSFET	International Rectifier	IRFP450
Q2	npn Transistor		2N3903
R1	24k (Note 1)		
R2	2k		
R3	7.5k		
R4	100k		
R5	20		
R6	63k		
R7, R8	27k		
R9	2M		
R10	39k		
R11,R19	51k, 3W (Note 2)		
R12	.25Ω, 5W		
R13	560k		
R14	10k		
R15	47k		
R18	3M		
R19	Not used		
R20	670k		
R21	33k		
R22	20k		
R23	Not used		
R24	51k		
U1	High Efficiency, High power factor preregulator	Unitrode	UCC3858
U2	Comparator		LM393
HS1	Heat Sink	Aavid	513201
J1	Connector, 8-pos. .156 center	AMP	A1969

Table 1. Parts List (continued)

Notes:
1. Unless otherwise specified, all resistors are ¼W , Metal Film, 5%.
2. One resistor to take the place of both R11 and R19

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APPLICATION NOTE

POWER FACTOR CORRECTION USING THE UC3852 CONTROLLED ON-TIME ZERO CURRENT SWITCHING TECHNIQUE

BILL ANDREYCAK

INTRODUCTION

The controlled on-time, zero current switching technique provides a simple and efficient solution to obtaining high power factor correction. This discontinuous inductor current approach essentially programs a constant switch on-time during one line half-cycle. It does not require any "complex" analog square, multiply and divide functions to control the instantaneous switch current as with other PFC techniques. Additionally, zero current switching limits the peak current to exactly twice that of the average inductor current over all line and load combinations. High efficiency operation is also achieved with no boost rectifier recovery concerns and power loss. In a typical 80 Watt application the UC3852 PFC technique delivers a power factor of 0.998 with 5.8% Total Harmonic Distortion at nearly 94% efficiency.

CIRCUIT SCHEMATIC

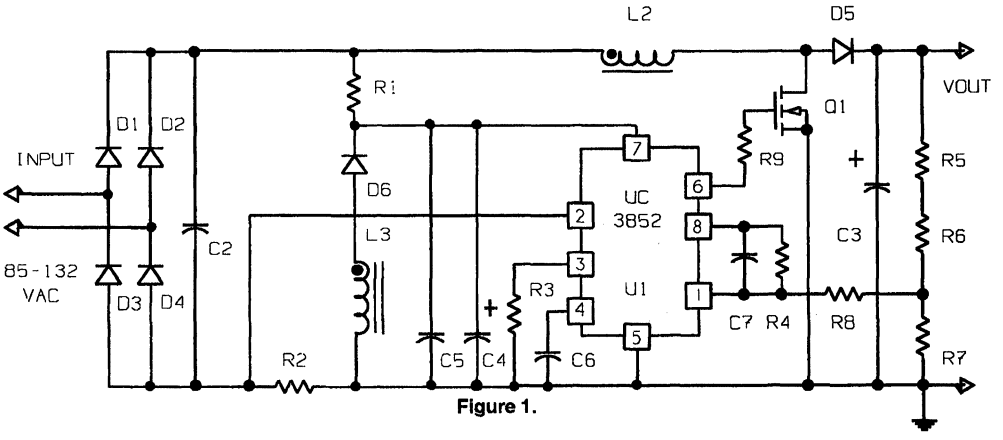


Figure 1.

UC3852 FEATURES

The UC3852 PFC controller contains several features which minimize external parts count while providing excellent performance and protection. Optimized for this off-line PFC application, the UC3852 delivers high power factor (0.997 typical) and a low cost overall solution.

OFF-LINE PROTECTION

- undervoltage lockout with hysteresis 16V turn-on, 11 V turn-off [1]
- clamped 12V gate drive output [2]
- active low, self biasing output [3]
- overcurrent protection [4]

CONTROL CIRCUIT ATTRIBUTES

- programmable maximum frequency [3, 5]
- programmable maximum on-time [3, 5]
- overcurrent indication output [7]

OPERATIONAL CHARACTERISTICS

- low operating current [8]
- low start-up current (0.4 mA) [1]
- few external required components
- 30 V maximum supply input [7]

CONTROL TECHNIQUE

- Zero Current Switching [9]
- controlled on-time [6]
- high noise immunity [6]

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

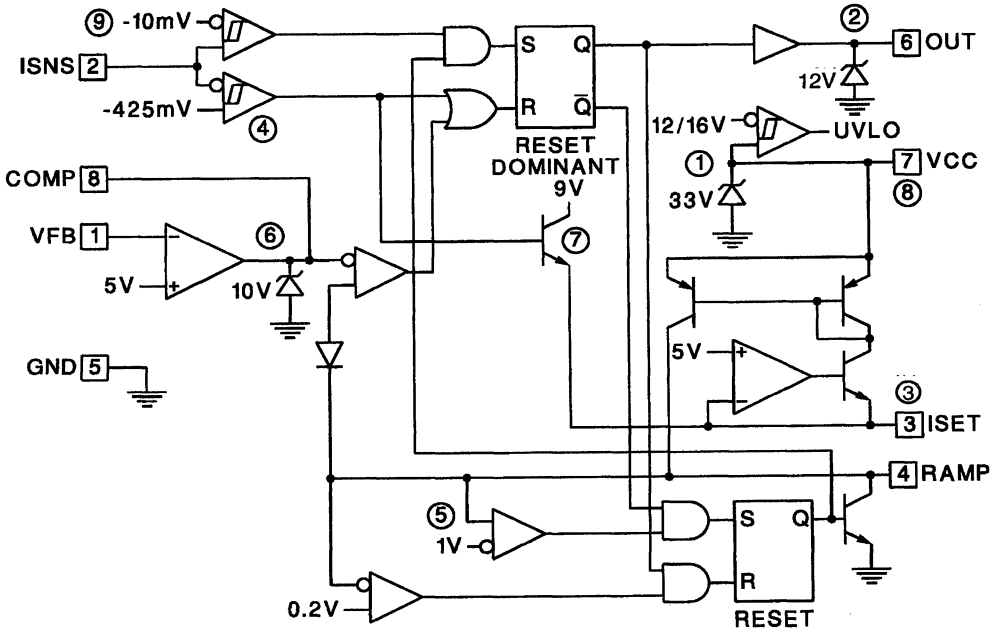


Figure 2.

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

PFC TECHNIQUE OVERVIEW

Most power factor correction techniques incorporate the boost topology which can be operated in either the continuous or discontinuous inductor current modes and switched at a fixed or variable frequency. Generally, the fixed frequency, continuous inductor current variety is preferred for higher power applications to minimize the peak current. Below about 500 Watts, the discontinuous inductor current version operated in a variable frequency mode offers several advantages. Benefits include reduced inductor size, minimal parts count and low cost of implementation. This paper will highlight the controlled on-time, zero current switched variety of discontinuous inductor current PFC operation.

FUNDAMENTALS

CONTROLLED ON-TIME

On-time of the PFC switch is controlled by the voltage error amplifier of the UC3852 which is compared to a sawtooth waveform generated at the ICs RAMP function at pin 4. The PFC switch on-time varies with line and load conditions but should be considered constant for one line half-cycle. A low frequency bandwidth is necessary in the voltage error amplifier loop compensation which is typically rolled off to cross zero dB below the line frequency.

ZERO CURRENT SWITCHING

Zero current switching facilitates three important advantages in this application. First, the inductor current must be zero before the next switching cycle is initiated inferring high efficiency and elimination of the boost rectifier recovery loss. Secondly, the change in inductor current (delta IL) is equal to the peak inductor current (IL(pk)) since current starts and returns to zero each cycle. The discontinuous boost converter current waveform has a triangular shape with an area (charge) equal to one-half of the product of its height (peak current) multiplied by its base (time). Since the timebase can be considered as a series of consecutive triangles, the peak current is therefore limited to exactly twice that of the average current. This is valid for both the steady state and instantaneous switching cycle relationships. The converter operates right on the border between continuous and discontinuous current modes which results in variable frequency operation.

The "fixed" on-time in conjunction with zero current switching provide automatic power factor correction of the input current. This can be demonstrated by analyzing the basic inductor waveform using specific attributes of this PFC technique for either charging and discharging of the inductor current. Since the inductor charging condition is being controlled by the UC3852 circuitry it will be used for the analysis.

INDUCTOR WAVEFORM

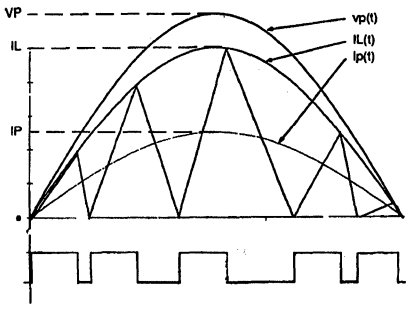


Figure 3.

1. $\frac{V}{L} = \frac{dI}{dt}$

For the PFC boost converter operation, V can be replaced by Vin(t), the instantaneous voltage across the inductor. Also, it is assumed that the inductance and the switch on-time is constant for the duration of one line-half cycle. The change in inductor current, delta I is actually the peak value of current (Ipk(t)) since the inductor always begins charging at zero current, as forced by zero current switching. Substituting these relationships into the inductor wave from equation will demonstrate the simplicity of this specific technique when used for power factor correction.

V = Vin(t)

L = constant

dI = Ipk(t)

dt = constant

2. Ipk(t) $\propto$ Vin(t)

This relationship demonstrates that the instantaneous line current will exactly track that of the instantaneous line voltage. Since the input voltage waveform is sinusoidal (Vin sin(wt)), then so is the input current (Ipk sin (wt)). This controlled on-time, zero current switched technique provides automatic power factor correction with very simple control circuitry.

PFC POWER STAGE DESIGN

It is advantageous to begin the power relationships from the AC line input of the preregulator and work towards the DC output section. The instantaneous primary voltage (VP(t)) is related to the steady state peak input (VP) by the following relationship:

3. $VP(t) = VP \sin(wt)$

where $VP = \sqrt{2} \times Vp$ (rms)

The amplitude of Vp(t) varies between zero and VP as sin(wt) goes from zero to one for one line half-cycle. Note that Vp(t) and VP are always positive with respect to the PFC circuit common due to the bridge rectification of the AC input waveform. The input current can similarly be expressed as:

4. $IP(t) = IP \sin(wt)$

where $IP = \sqrt{2} \times Ip$ (rms)}

Input power to the PFC converter is the Root Means Squared (RMS) component of the line voltage (Vp(RMS)) multiplied by the line current (Ip(RMS)). This can also be expressed using the peak terms of each waveform which is simpler for this application.

5. $Pin = \frac{VP}{\sqrt{2}} \times \frac{IP}{\sqrt{2}}$

$$Pin = \frac{(VP \times IP)}{2}$$

The average DC output current (Io) is determined by dividing the output power (Po) by the output voltage (Vo).

6. $Io = \frac{Po}{Vo}$

Converter efficiency (n) can also be factored into the design equations although it may typically be in the neighborhood of 94% at full load.

7. $Pin = \frac{Po}{n}$

or $Po = Pin \times n$

where $Pin = \frac{(VP \times IP)}{2}$

7A. $Po = \frac{(VP \times IP \times n)}{2}$

Equation 7A. can expressed with regard to primary current.

7B. $IP = \frac{(2 \times Po)}{(VP \times n)}$

It has been already established that the peak inductor current is exactly twice that of the average inductor current due to zero current switching.

8. $IL(pk) = 2 \times IL(avg)$

The average input current must be equal to the average inductor current since they are in series.

9. $Ipri\ (avg) = IL\ (avg)$

Combining equations yields the peak inductor current to the input current.

10. $Ipri\ (pk) = \frac{(4 \times Po)}{(VP \times n)}$

The inductor current can now be analyzed in its time variant form and over all line and load conditions.

11. $IL\ (t) = \frac{(4 \times Po \times \sin(wt))}{(VP \times n)}$

TIMING RELATIONSHIPS

Steady state conditions will be used to analyze the timing relationships of this controlled on-time PFC technique. The peak primary voltage (VP) will be used as the starting point for the calculations, so the input line must be specified.

The inductor relationship of equation 1. will be solved for the specific on-time required to charge the inductor to the correct peak current. This equation can be restated for a given set of operating conditions as:

12. $t(on) = IL\ (pk) \times \frac{L}{VP}$

Substituting equation 10. for IL(pk) into equation **12** results in:

12A. $t(on) = \frac{(4 \times Po \times L)}{(VP^2 \times n)}$

The instantaneous switch off-time varies not only with the line and load conditions, but also with the instantaneous line voltage. Off-time is analyzed by solving equation 1. for the inductor discharging where the voltage across the inductor is Vout minus Vin. This should be solved for the time required to discharge the current from its instantaneous peak to zero, which can be expressed as:

13. $t(off) = \frac{(IL(pk) \times L)}{(Vo - VP(\sin(wt)))}$

Substituting equation 11. for IL(pk) above will expand the off-time equation to:

13A. $t(off) = \frac{(4 \times Po \times L \times \sin(wt))}{VP \times (Vo - (VP \times \sin(wt)))}$

Due to the high efficiency during the boost inductor discharge and lack of rectifier recovery losses, the efficiency term (n) is essentially one. Loss can be ignored during the off-time since the boost diode forward voltage drop is very small in comparison to

the high voltage DC output, and resistive losses at these lower powers and currents are minimal.

CONVERSION PERIOD

The total time for one switching cycle is obtained by adding the on-time with the instantaneous off-time. Switching frequency is the reciprocal of the cyclical switching period which varies with line, load and instantaneous line voltage.

14. t(per) = t(on) + t(off)

$$t(per) = 4 \times Po \times L \times \left(\frac{1}{VP^2} + \frac{\sin(wt)}{VP \times [Vo - VP\sin(wt)]} \right)$$

SWITCHING FREQUENCY

15. f(conv) = 1 / t(per)

Switching frequency varies with the steady state line and load operating conditions along with the instantaneous input line voltage. Generally, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. Many applications can use thirty kiloHertz (30 kHz) as a good first approximation. Higher frequency operation should also be evaluated as this can significantly reduce the inductor size without negatively impacting efficiency or cost. In most applications, the minimum switching frequency will coincide with full load operation during the peak of the input voltage waveform at low line. In contrast, the highest frequency conversion occurs at light load and high line conditions, just as the input voltage waveform nears the zero crossing point. A plot of t(on), t(off), t(per) and switching frequency versus instantaneous line voltage is shown in figure 4 and for the specific application circuit of figure 1. Figure 5 demonstrates the typical changes incurred in conversion frequency from low to high line inputs.

SELECTING THE OUTPUT VOLTAGE

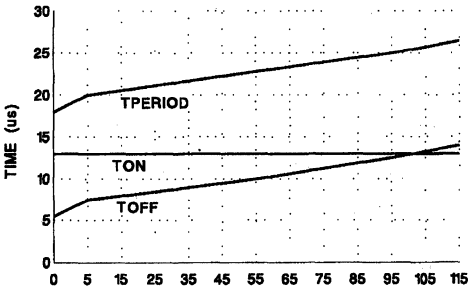
The boost converter output voltage should be designed to be at least thirty volts higher than the peak of the input voltage at high line. This will prevent long conversion cycles due to the small voltage across the discharging boost inductor. When this thirty volt margin is ignored, the minimum switching frequency will occur at the peak of high line operation and not at low line, but also at full load. This will require recalculation of the timing intervals.

INDUCTOR CONSIDERATIONS

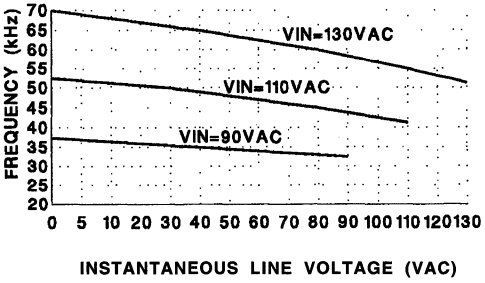
The exact inductor value can determined by solving equation 14 for the required inductance at the selected minimum operating frequency. Maximum on-time needs to be programmed into the UC3852 timing circuit. Both t(on)max and t(off)max will be individually calculated and added together to obtain the maximum conversion period, t(per)max. This is required to obtain the inductor value. Equations 12A and 13A will be solved for their respective maximums.

$$12B.\ t\ (on)\ max = \frac{4 \times L \times Po\ (max)}{VP\ (min)^2}$$

$$13B.\ t\ (off)\ max = \frac{4 \times L \times Po\ (max)}{[VP\ (min) \times (Vo - VP\ (min)]}$$



Conversion Times vs Instantaneous Line Nominal Line Voltage
Fig. 4



Conversion Frequency vs Instantaneous Line
Fig. 5.

14A. t(per)max = t(on)max + t(off)max

The minimum conversion frequency (F(conv)min) corresponds to the reciprocal of the maximum conversion period, t(per)max.

15A. F(conv)min = 1 / t(per)max

INDUCTOR VALUE

The inductance value necessary for an application can be obtained by substituting equations 12B and 13B into 15A. using the relationship of 14A.

$$16A.\ L = \frac{VP\ (min)^2 \times [Vo - VP\ (min)]}{4 \times Po\ (max) \times Vo \times F\ (conv)\ min}$$

This equation provides insight as to the possible ways to reduce the inductor value (size and cost) for a given set of design specifications. The most obvious approach is to increase the minimum conversion frequency above thirty kiloHertz if none of the other parameters (Vo, Po) can be varied.

INDUCTOR DESIGN SUMMARY

Generally, the size and cost of an inductor vary with its energy storage capacity, W(L). Although most of the energy is stored in the air gap (with a gapped ferrite design), the core set must support the necessary flux density (B) without saturating or exhibiting high core loss. The required energy storage of the boost inductor is:

17. W(L) = 0.5*L*IL(pk)^2

The number of turns required for a selected core size and material is:

18. N = L*IL(pk)*10^4 / (Bmax*Ae)

where Bmax is in Teslas and Ae is in square centimeters (cm^2)

The center leg gap to achieve the correct

inductance and storage is expressed by:

19. l(gap)={Uo*Ur*N^2*Ae*10^-2}/L (cm)

where Uo=4*Pi*10^-7(permitivity of free space), and Ur=1 (relative permeability of air)

OUTPUT CAPACITOR

The value of output capacitance is a generally determined by the required hold-up time or the acceptable output ripple voltage for a given application. It may also be governed by the specified ripple current rating or capacitor temperature rise. Typically, an approximation of one microFarad per Watt (1uF/W) is a good starting point. The exact value can later be changed depending on conversion frequency and other factors previously mentioned.

Electrolytic capacitors are typically used near 80% of their working voltage. This will necessitate a 500 VDC rating for use in a 264 VAC PFC application which may not be practical from a cost perspective. One option is to connect two lower voltage capacitors in series, each having the same value and a 250VDC rating.

SEMICONDUCTOR SELECTION

Peak currents and voltages must first be known over all operating conditions to select the proper MOSFET switch and boost rectifier. Standard design practice is to derate all semiconductors to about 75% of their maximum ratings, indicating the use of 500+ volt devices.

Low cost bipolar transistors are an acceptable alternative to MOSFETs if the conversion frequency is maintained fairly low. Inexpensive high voltage diodes with recovery times of 200 nanoseconds, or less should be used for the boost rectifier. Two popular devices are the 1N4937 and MUR160. Speed is not an issue with the input bridge rectifiers where 1N4004 to 1 N4006 types are acceptable. High frequency switching noise in the PFC converter should be well filtered before reaching the input bridge diodes due to their low speed characteristics. This is best accomplished by adding an UC filter between the bridge rectifier DC output and the boost converter.

CONTROL CIRCUIT DESIGN :

PROGRAMMING THE UC3852

STARTUP CIRCUITRY

The UC3852 design incorporates a low startup current feature and draws less than one milliamp (mA) from the Vcc bias supply. This minimizes the power loss due to with the startup resistor after the converter begins operation when a bootstrap winding supplies the full DC supply current. The UC3852 IC turns on when Vcc reaches approximately 16 volts, and IC supply current will increase to its operational level. Undervoltage lockout protection will turn the UC3852 device off when the supply voltage falls below the lower UVLO threshold of approximately 10 volts.

The startup circuitry for this off-line consists of a startup resistor from Vcc to the input supply voltage and a storage capacitor from Vcc to ground. Typically, select Rstart to supply around 1.5 milliamps (rms) of charging current (I(charge) at low line. The exact value can be obtained from the following approximations.

$$R(start) = \frac{VP(min) - V(turn\text{-}on)}{1.41 \times I(charge)}$$

The Vcc bias supply filter capacitor value is determined by several factors, but primarily by the UC3852 undervoltage lockout hysteresis. Implementation and phasing of this boost inductor winding in addition to soft start circuitry will also effect the capacitance.

$$C(Vcc) = \frac{(ICC - I(charge) \times t(boot)}{UVLO\ hysteresis}$$

For many applications, the following approximations can be used:

ICC = 10mA

I(charge) = 1.5 mA

t(boot) = 10 ms (one-half cycle at 50 Hz)

UVLO hysteresis = 5 volts

V(turn-on) = 15V

A standard 15 uF electrolytic with an adequate voltage rating (35V once derated) is used.

PROGRAMMING THE ON-TIME

The maximum switch on-time must be calculated to program the UC3852 oscillator. This maximum occurs when the line voltage, VP is at its minimum and the output power is at its maximum. This is more commonly known as the low line, full load condition.

t(on)max = 4*Pout(max)*L / Vp(min)^2

The UC3852 on-time is programmed by R/C components and uses two of the IC pins. A resistor from the ISET pin to ground programs the charging current into the RAMP pin. The Iset pin has an output voltage of approximately 5 volts, so the ISET is 5 volts divided by Rset. Typical charging current should range between 100 and 600 microamps.

The RAMP pin is used as one input to the Pulse Width Modulator of the UC3852. Internally, the RAMP voltage is compared to the error amplifier output (COMP) voltage to determine the exact on-time. The RAMP pin has a maximum amplitude of approximately 9 volts, and begins charging from approximately 0.2 volts, or an 8.8 volt swing.

The RAMP capacitor value is selected to program the maximum switch on-time as it charges from 0.2 to 9 volts by Iset. It can be calculated from the capacitor charge equation, shown below.

C = (I * dt) / dV

C(RAMP) = [Iset * t(on)max] / 8.8 V

The RAMP capacitor should be selected first from a list of standard values within the 100pF to 1nF range. The resulting ISET programming resistor selection is much easier as standard values with an initial tolerance of one percent (1%) are readily available.

$$RSET = \frac{5 \times t(on)max}{8.8 \times C(RAMP)}$$

or

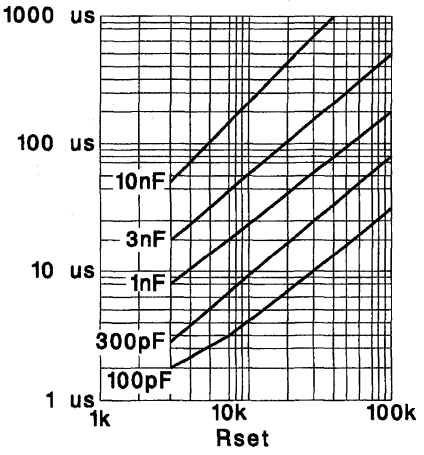
RSET = 0.568 * t(on)max / C(RAMP)

t(on)max = [RSET*C(RAMP)] / 0.568

UC3852 ON-TIME vs. RSET & C(RAMP)

ERROR AMPLIFIER COMPENSATION

Power Factor Correction using the ZCS controlled on-time technique requires a very low bandwidth voltage loop to deliver high power factor (). This is necessary to keep the switch on-time constant during any one line cycle. Other advantages to this approach are high noise immunity, and simplicity,



Max On-Time vs. Rset and Ct
Fig. 6

since no squarer, multiply or divide circuitry is needed.

Configuration of the compensation circuitry is shown in the UC3852 PFC application schematic. First, the PFC preregulator output voltage (Vout) is accurately divided down to 5.0 volts to interface with the error amplifier. Three standard one-half watt resistors are used to avoid needing more expensive, high voltage rated resistors for this application. This signal goes through a 20K ohm input resistor to the error amplifier inverting input. Feedback components are a 1 meg ohm resistor and a 0.1 uF capacitor in parallel from the E/A output to the inverting input.

This recommended amplifier compensation delivers one low frequency pole in the loop response at 1.6 Hz, as programmed by 1 meg ohm and 0.1 uF components. Low frequency gain is determined by the 20 K ohm input resistor, the output voltage divider resistance and the 5.0 reference voltage seen at the amplifiers (internal) noninverting input.

Many other compensation arrangements are possible.

Using this compensation network, a low frequency gain of approximately 34 dB is achieved. This rolls off with a single pole (-20 dB/decade) response centering at 1.6 Hz. The gain curve will intersect zero dB at about 120 Hz and result in excellent power factor correction. Better dynamic response and less overshoot of the output voltage can be obtained by adjusting the 20 K ohm input resistor to increase low frequency gain and move the zero dB crossing out to a higher frequency. Some slight degradation of the power factor is to be expected by increasing the loop response.

SOFT START

Soft starting of the output is optional, but recommended to minimize the output voltage overshoot upon power-up. This does not occur in applications which will always have some load on the output. However, most electronic ballast have either no load, or a very light load on the output at power-up and will see the overshoot. Soft start implementation requires only a diode and capacitor from the compensation pin to ground. Another diode from the capacitor to VCC discharges the soft start capacitor to the falling Vcc voltage when the AC line power is removed. This will guarantee that the circuit will always start up in soft start if the line is AC plug is removed for a few seconds. Again, this is an optional feature which depends on the application.

One "trick" to significantly reduce the size of the soft start capacitor is to replace the diode with a cheap PNP transistor. A capacitance multiplier can be obtained by connecting the PNP emitter to the error amplifier output and soft start capacitor from the base to ground. The collector of the transistor is connected to ground. This adaptation will scale the capacitance value up by beta of the transistor at the amplifier output. A 2N2907 or equivalent is a popular choice and will reduce the capacitance value by a factor of approximately 50.

A 1N914 or 1N4148 signal diode should be used from the base to emitter to prevent negative base-emitter voltages from damaging the transistor. Additionally, this transistor can easily be interfaced with any optional fault protection schemes to soft start the controller following a fault.

SOFT START IMPLEMENTATION

CURRENT SENSE

Current in the PFC design is sensed in the return line of the preregulator circuitry at the AC input bridge rectifiers. One side of the current sense resistor is referenced to the UC3852 "ground" connection. The other end of the resistor develops the current sense voltage which is equivalent to minus IL(t) * Rsense. The UC3852 zero current detection circuitry incorporates two comparators, one for zero current detection and another for over current protection.

ZERO CURRENT DETECTION

The zero current detection circuitry uses a negative 10 millivolt (-10mV) threshold as its reference. This negative threshold guarantees that there are no

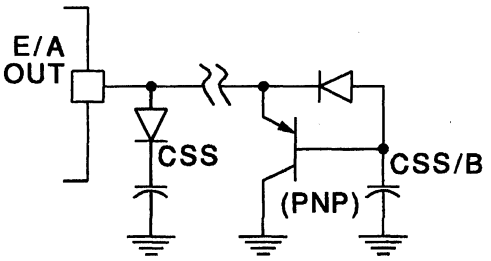


Figure 7.

startup problems since this input must be pulled below ground for normal operation. Whenever the zero detect input is raised above the minus ten millivolt threshold, the comparator is triggered and the next switching cycle begins.

Inductor current can be sensed by a current sense resistor which develops minus 400mV maximum during an overcurrent condition. This should only occur at a twenty percent overload, or 1.2 * IL(pk).

R(shunt) = 0.4 V / (1.2 * IL(pk))

Power dissipated in the shunt can be calculated by using the RMS component of the line current. The peak input current (IP) is one half of the peak inductor current (IL(max). The RMS component of the line current (IP(rms)) is obtained by dividing the peak line current (IP) by the square root of two (1.41).

IP(rms) = [IL(pk) / (2 * 1.414)

P (R(sense)) = IP(rms)^2 * R(sense)

Standard value, low resistance (1 ohm or less) one-eighth to one-quarter watt resistors can used alone or paralleled to obtain the exact value. Carbon composition or film resistors exhibit low series inductance and will work best.

A small R/C filter can be added in the current sense circuitry to filter out switching noise caused by circuit parasitics. This delay will minimally effect the precise two-to-one ratio of the peak to average

duce the amount of EMI/RFI filtering required by minimizing the rectifier recovery noise. For best results, the filter delay time should match the rectifiers recovery time. A ten ohm resistor and a one nanoFarad (1 nF) capacitor are good starting values.

OVERCURRENT FAULT PROTECTION

The UC3852 contains and overcurrent comparator (-400mV) which quickly terminates the PWM output. This comparator also drives circuitry connected to the ISET pin which raises its normal 5 volt amplitude to 9 volts during the overcurrent condition. In addition to programming the ramp capacitor charging current, the ISET pin can be used to drive external fault protection circuits. A resistor in series with a 5.6 volt zener diode to the ISET pin will develop approximately 3.4 volts across the resistor when an overcurrent fault is detected. This signal can be used to trigger external shutdown or hiccup circuitry.

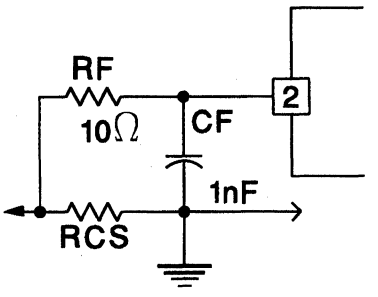


Figure 8.

GATE DRIVE

The UC3852 PWM output section is MOSFET compatible and rated for a one amp peak current. This totem pole design also features a twelve volt (12V) clamped output voltage to prevent excessive gate voltage when used with unregulated (Vcc) supply voltages. A twelve ohm resistor between the UC3852 and the MOSFET switch gate will limit the peak output current to its one amp maximum during normal operation.

Additionally, the UC3852 self biasing active low totem-pole design holds the MOSFET gate low during undervoltage lockout, preventing catastrophic problems at power-up and removal of the AC input.

inductor current and have an insignificant impact on power factor. However, this modification can re

ADVANCED PROTECTION CIRCUITRY

Certain applications of the UC3852 control IC may require sophisticated protection features. Some examples of these options are overvoltage protection and restart delay, soft start or latch-off following a fault. Each of these features can be added to the control circuit with a minimal amount of external parts, and often combined using shared components.

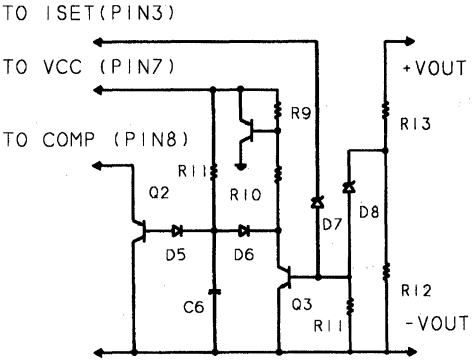


Figure 9.

LIST OF COMPONENTS

C6 = 1 uF, 35V
D5,6 = IN4148
D7= 6.2V ZENER
D8 = 40 V ZENER
Q2,4 = 2N2907
Q3 = 2N2222
R9,10=10K
R11 = 1 MEG
R12 = 24 K
R13 = Calculate for OVP
R14 = 1 K

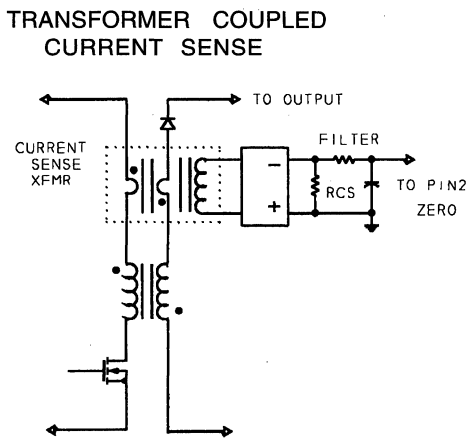


Figure 10.

Soft start is programmed by R11, C6 and the beta of Q2. Overcurrent protection starts at the UC3852 ISET pin which outputs a 9 V signal during a fault. This drives Q3 on through D7 and discharges C6 causing a soft start. Q4 also turns on with this arrangement which discharges Vcc causing a "hiccup". This is optional, and replacing Q3 with an SCR would latch the circuit off until power is reset. Overvoltage protection is attained via R11, R12, R13 and zener diode D8. When enough current flows through the zener (D8), R11 biases transistor Q3. Protection is similar to the overcurrent condition.

Regulated Auxiliary Bias Circuit

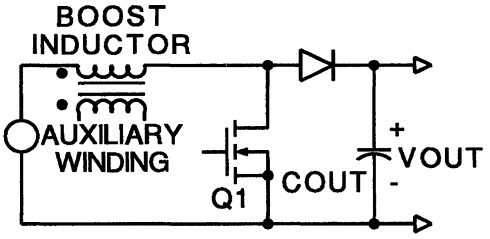


Figure 11.

CURRENT SENSE TRANSFORMERS

A transformer can be used to sense current in most of the UC3852 applications for higher efficiency. Two primary windings are needed to sense each component of the switched current. These may also be unequal in number of turns, depending on the input and output currents (or voltages). A single secondary winding and bridge rectification recreates the total inductor current. A small R/C filter network may be required to smoothen out spikes caused by the leakage inductance.

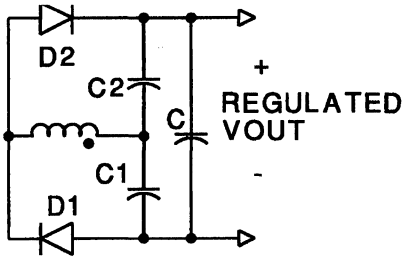


Fig. 12

Universal AC Input Feedforward Circuit

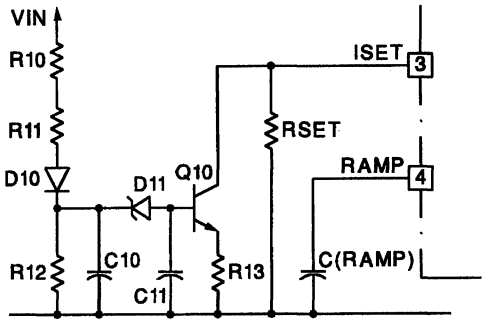


Figure 13.

REGULATED BOOTSTRAP SUPPLY

A regulated auxiliary supply is obtainable with a slight modification to the bootstrap interface and two inexpensive components. This circuit is advantageous in applications which incorporate other control ICs for the main converter or ballast drive sections. A regulated auxiliary voltage is NOT needed for the UC3852 which features a clamped twelve volt (typical) gate drive output voltage. This insures proper drive amplitude for power MOSFETs with an unregulated IC supply voltage to 30 volts.

Dual AC Input Range (110/220 VAC) Feedforward Circuit

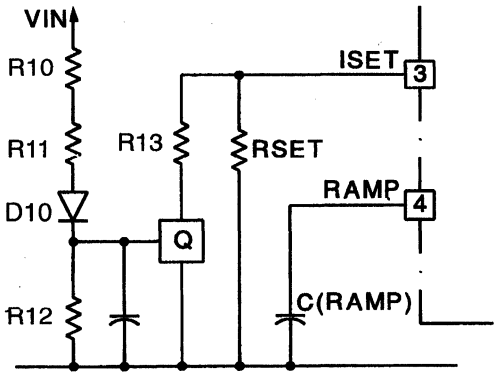


Figure 14.

OTHER PFC APPLICATIONS

The basic PFC schematic of Figure 1 can be used as a template for other PFC applications with different input voltage ranges and output power levels. A majority of the changes will be to accommodate higher (or lower) voltages and currents. Once familiar with the complete design procedure as outlined in this application note, designers are encouraged to recalculate the values for their applications using the same guidelines.

UNIVERSAL AC INPUT RANGE

The UC3852 controlled-on time, zero current switched PFC technique can be used to accommodate wide AC input voltages with the addition of a simple feedforward circuit. This external circuitry is required to cancel out the line dependent changes in the switch on-time over the three-to-one input range from 85 to 264 volts. Otherwise, the approximate nine-to-one control range of the UC3852 on-time would be fully used for line regulation allowing no accommodation for load changes.

CIRCUIT OPERATION

The rectified input voltage is applied across the network consisting of R10 through R12, D10 and C10. Capacitor C10 charges to the peak of the divided input voltage and is large enough to maintain this level over one line cycle. Diode D11 serves as an offset to bypass the range extender circuitry until a sufficient minimum line voltage has been established, typically 80 VAC. Capacitor C11, a small filter capacitor and the base of transistor Q10 reach a voltage of V(C10) minus the Zener forward voltage drop of diode D11. As this voltage rises, the emitter of Q10 and voltage across resistor R13 follows, offset by the base-emitter diode drop of Q10. This increasing bias pulls more current from the UC3852 ISET pin which sits at a fixed voltage. The current in both resistor R13 and resistor RSET is pulled from the UC3852 ISET output. Within the UC3852, the ISET current is mirrored to the RAMP capacitor (Cramp) which is compared to the error amplifier output to determine the ON-time. As the input voltage increases bias to Q10, more current is pulled from ISET thus increasing the RAMP charging current. For a fixed output load, this circuit performs the function of voltage feedforward and can keep the error amplifier output voltage fixed regardless of AC input voltage. This allows the full use of the ICs ON-time control range to accommodate load variations.

FEEDFORWARD CIRCUIT DESIGN

LOW LINE:

ISET = 5V/RSET

t(on)max=8.8*Cramp / ISET

HIGH LINE:

ISET = 5V/(RSET II RI3)

GENERAL:

V(C10) = 1.41*VIN*R12/(R10+R11+R12)

NOTE:V(C10)MAX=5V+Vzener

ISET(MIN)=5V/RSET

ISET(MAX)=ISET(MIN)+5V/R13

FEEDFORWARD BEGINS WHEN:

V(C10)-Vzener-Vbe(Q10) 0V

COMPONENTS:

C10=22uF/16V Q10=2N2222

C11=1nF/16V R10,11=100K

D10=1N4148 R12,13=5.1K

D11=1N5221(2.4V) RSET=51K

CONTINUOUS CURRENT PFC BOOST CONVERTER

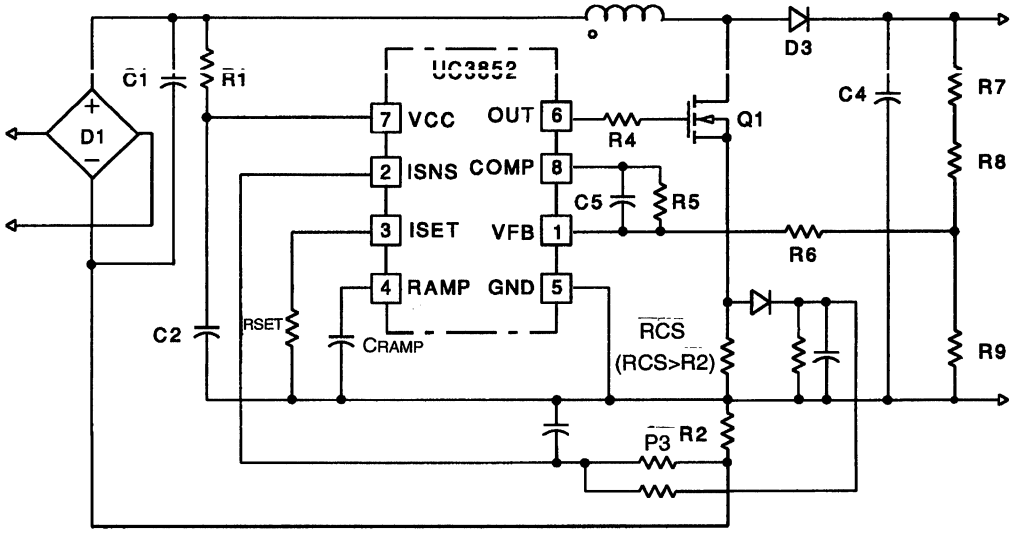


Figure 15.

CONTINUOUS PFC CURRENT IMPLEMENTATION

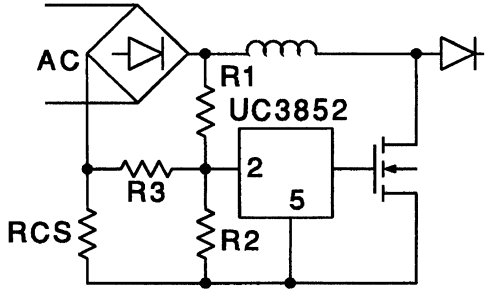


Figure 16.

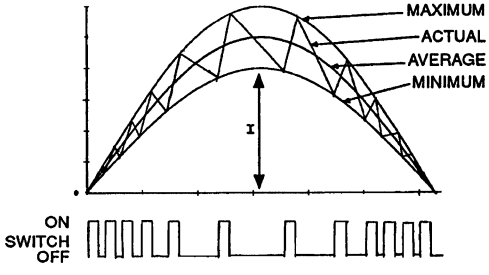


Figure 17.

UC3852 CONTROLLED PFC FLYBACK CONVERTER

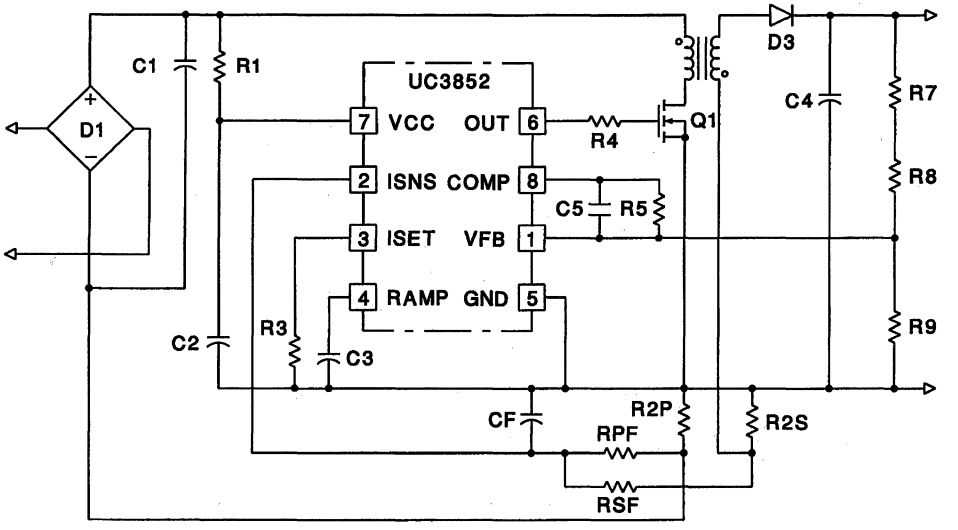


Figure 18.

UC3852 AS A CAPACITIVE DISCHARGE DRIVER

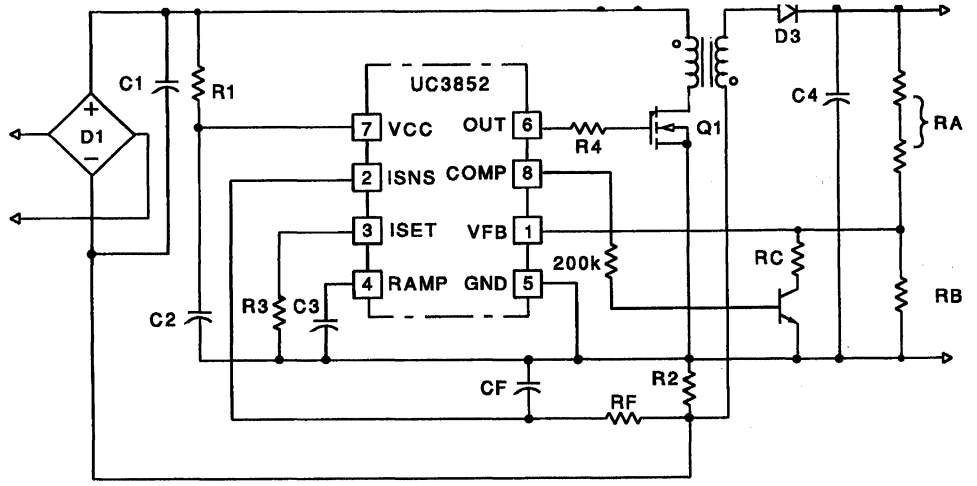


Figure 19.

AUTORANGE (110/220) VOLTAGE FEEDFORWARD CIRCUIT

Input line voltage feedforward can also be obtained with a simple circuit for dual AC input ranges with less demanding load variations. Shown below is a single step autorange circuit for use with the UC3852 timing circuitry. Basically, the TL431 is used as a comparator to switch in a second timing resistor (RSET') when the input voltage exceeds a preset threshold.

The AC input voltage is rectified by diode D20 and 'divided down by resistors R20 and R21. Capacitor C20 peak charges and filters this waveform to develop a DC voltage proportional to the input line. RSET is programming the initial charging current to the timing capacitor CRAMP. When the voltage across C20 exceeds the 2.5 V threshold of the TL431 comparator, its output goes low. This places

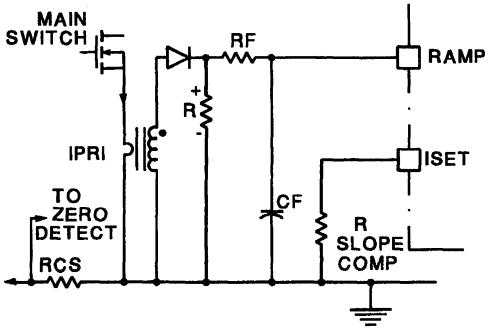


Figure 20.

a second timing resistor, RSET', in parallel with the original one thus increasing the current to CRAMP and performing line feedforward. Resistor values should be selected to switch in the feedforward compensation at approximately 155 VAC which is mid-range between high line of a 110 VAC input (130 VAC) and low line for a 220 VAC input (180 VAC). The value of RSET' must be selected to account for the TL431 output saturation voltage.

CONTINUOUS CURRENT PFC BOOST CONVERTER

The zero current switched PFC technique can also be modified to operate in the continuous inductor current mode. A positive amplitude, small offset signal is derived from the input voltage waveform. It gets added to the normal current sense signal which is negative with respect to ground. Summing these two signals to the ZERO input biases the actual inductor current sense more positive. Therefore, the zero current detection threshold is crossed before the inductor current is actually zero, and the PFC preregulator operates with continuous current. The exact amplitude of both parts of the inductor current can be determined by adjusting the inductance, on-time, and current sense resistor.

OTHER PFC TOPOLOGIES

The UC3852 can also perform power factor correction using the Flyback topology with a slight degradation to Power Factor. A Flyback topology is commonly used to generate a lower (or much higher) voltage output than the Boost converter. A nonisolated version of this is shown in Figure 18. for simplicity.

A resistor in series with the power return lead senses the inductor charging current while the switch is on, similar to that of the boost converter. However, the discharging current information is lost when the switch is off while the stored inductive energy is delivered to the output. A second current sense resistor is added in series with the secondary winding as shown to recover this information. A small amount of filtering may be necessary to smoothen out switching noise spikes while summing the current sense signals.

Good regulation of the output voltage will be obtained with this technique although some 120 Hz (2 x line frequency) ripple is to be expected. The flyback circuitry cannot fully transfer power when the input line voltage goes down near zero each cycle. This approach has numerous applications where a small amount of power supply ripple is acceptable. Post regulator circuits can be added to improve regulation if necessary.

CAPACITIVE DISCHARGE CIRCUITS

The UC3852 can also be used in capacitive discharge circuits, typical of photoflash and strobe applications. In fact, the circuit shown below will provide the minimum recharge time for a given peak input current. Zero current switching insures that the next switching cycle is initiated as soon as the inductor current discharges to zero. There is no deadtime between conversion cycles and the output is charged as quickly as possible for the programmed maximum inductor current.

Regulation is achieved by using a burst mode of operation where the UC3852 stops delivering output pulses when the output voltage setpoint is reached. Operation will begin again when the output voltage drops below the lower programmed threshold. Both of these thresholds are pro-

grammed by Ra, Rb and Rc according to the following formulas.

Vout(max) = (5*(Ra+Rx))/Rx

Vout(min) = (5*(Ra+Rb))/Rb

where Rx=(Rb*Rc)/(Rb+Rc)

NON PFC APPLICATIONS USING VARIABLE FREQUENCY OPERATION

Conventional PWM (non PFC) applications using a variable frequency control techniques can also be implemented with the UC3852. This applies to both current mode and variable ON-Time control methods. Typical examples of these are discontinuous current boost and flyback converters. Variable frequency operation is popular in numerous applications as it can minimize the peak current in comparison to fixed frequency designs. The zero current detection and switching technique of the UC3852 should be used in its standard configuration with current sensed below ground, although a current transformer can be introduced.

IMPLEMENTING CURRENT MODE

The ICs RAMP input will be used as the current sense input to be compared to the error amplifier output for current mode control. A current transformer is recommended to fully utilize the 9 volt compliance of this pin. This implementation allows for a wide load swing with maximum noise immunity. The RAMP pin gets discharged by internal IC logic to 0.2 V at the end of each ON-time. Therefore, some series impedance to the current sense resistor is recommended to keep load current outside of the IC. Any filter capacitor to suppress the switch leading edge noise spike will also get discharged. The ramp pin does not need a programming resistor, but one could be used to introduce optional slope compensation via the filter capacitor.

VARIABLE ON-TIME CONTROL

The switch ON-Time can also be controlled by comparing a sawtooth ramp to the error amplifier output. Configuration of this is basically identical to the standard PFC application using a RAMP capacitor and resistor to program the maximum ON-Time. Error amplifier compensation is likely to be much different and utilize a much higher loop crossover frequency than its PFC counterpart. The ICs error amplifier is similar to a '741 type general purpose OP-AMP and is programmed accordingly.

REFERENCES and ADDITIONAL INFORMATION:

1. ANDREYCAK, W. : "Controlled ON-Time, Zero Current Switched Power Factor Correction Technique"; UNITRODE Power Supply Design Manual SEM-800.

2. AHMED, SAEED, : "Controlled On-time Power Factor Correction Circuit with Input Filter"; Thesis, Virginia Polytechnic Institute.

3. MAMMANO, BOB and DIXON, LLOYD: "Designing High Power Factor Systems - Choosing the Optimum Circuit Topology", PCIM Magazine, March 1991.

PERFORMANCE EVALUATION

The UC3852 controlled PFC circuit shown in Figure 1 was constructed using the list of materials provided for this application. Power Factor and Total Harmonic Distortion to the 50th harmonic were measured using a VOLTEC PM- 3000 AC power analyzer. Test results indicated a power factor of 0.998 and T.H.D. below 6% at nominal line and full load. Very similar readings were obtained over the complete input voltage range and a moderate load change. Zero Current Switching (ZCS) facilitates high overall efficiency with this PFC technique.

UC3852 PFC TEST CIRCUIT

SPECIFICATIONS:

VIN = 85 TO 135 VAC

VOUT = 350 VDC

POUT = 86 W

MEASURED PERFORMANCE:

P.F. = 0.998

T.H.D. = 5.81%

TEST CONDITIONS;

(nominal line)

VIN = 115.7 VAC

IIN = 0.799 AAC

PIN = 92.13 W

VA IN = 91.84

INRUSH Ipk = 17.7 A

VOUT = 355.6 VDC

IOUT = 0.242 ADC

POUT = 86.1 W

EFFICIENCY = 93.45 %

C U R R E N T :

HARMONIC CONTENT

1st : 0.775 Amp

3rd : 3.91%

5th : 0.82%

7th : 0.38%

9th : 0.35%

11th: 1.30%

13th : 0.21%

LIST OF MATERIALS

CAPACITORS

C2 = **0.47** uF / 200 V

C3 = 82uF / 400 V

C4 = 22uF / 35 V

C5 = 0.1uF / 35V

C6 = 1nF / 16V

c7 = 0.1uF / 16V

DIODES

D1-4 = 1N4004, 1A / 400 V

D5 = 1N4937, 1A / 600 V

trr = 200ns

D6 = 1N4148, 0.2 A / 50 V

INDUCTORS

L2 = 1 mH Boost inductor

L3 = Several turns on L2 to provide 20 VDC supply voltage

RESISTORS

R1 = 100 k ohms 1 Watt

R2 = 0.1 ohm 1 W non-inductive

R3 = 18.2 k ohms 1% 1/2 W

R4 = 1 meg ohm 1/4 W

R5 = 330 k ohms 1% 1/2 W

R6 = 390 k ohms 1% 1/2 W

R7 = 10 k ohms 1% 1/4 W

R8 = 20 k ohms 1/4 W

R9 = 10 ohms 1/2 W non-inductive

TRANSISTOR

Q1 = IRF830 500 V / 4 A

INTEGRATED CIRCUIT

U1 = UC 3852

UNITRODE CORPORATION
7 CONTINENTAL BLVD. MERRIMACK. NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

APPLICATION NOTE

UC3854 Controlled Power Factor Correction Circuit Design

PHILIP C. TODD

ABSTRACT

This Application Note describes the concepts and design of a boost preregulator for power factor correction. This note covers the important specifications for power factor correction, the boost power circuit design and the UC3854 integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. This design procedure is directly applicable to the UC3854A/B as well as the UC3854. The recommendations in Unitrode Design Note DN-39 cover other areas of the circuit and, while not discussed here, must be considered in any design. This application note supersedes Application Note U- 125 "Power Factor Correction With the UC3854. "

INTRODUCTION

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor.

The most general definition of power factor is the ratio of real power to apparent power.

$$PF = \frac{P}{(Vrms \times Irms)} \quad \text{or} \quad PF = \frac{Watts}{V.A.}$$

Where P is the real input power and Vrms and Irms are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case. If the load is a pure resistance the real power and the product of the RMS voltage and current will be the same and the power factor will be 1.0. If the load is not a pure resistance the power factor will be below 1.0.

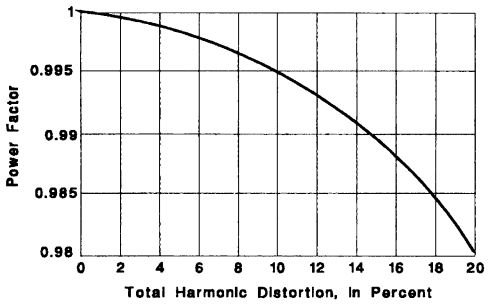
Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

$PF = \cos \theta$

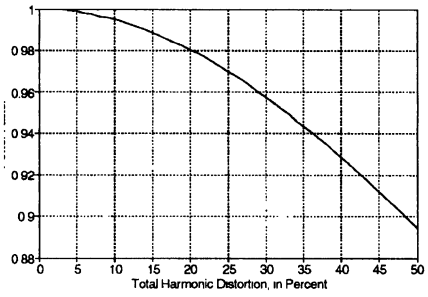
The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feedforward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current without increasing the total power being drawn. A non-linear load will therefore have a poor power factor because the RMS value of the current is high but the total power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from

Power Factor Versus Distortion



Power Factor Versus Distortion



Harmonic Order	Permissible current	Maximum permissible current
n	mA/W	A
Odd harmonics		
3	3.4	2.30
5	1.9	1.14
7	1.0	0.78
9	0.5	0.40
11	0.35	0.33
13	0.3	0.21
15 up	3.85/n	$0.15 \times \frac{15}{n}$
Even harmonics		
2	1.8	1.08
4	0.7	0.42
6	0.5	0.30
>8	$\frac{3}{n}$	$\frac{1.80}{n}$

Table 1

several sources: the feedforward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. But power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

The trend among the world standards organizations responsible for power quality is to specify maximum limits for the amount of current allowed at each of the harmonics of the line frequency. IEC 555-2 specifies each harmonic up through and beyond the 15th and the amount of current permissible at each. Table 1 lists the requirements for IEC 555-2 as of the time of this writing. There are two parts to the specification, a relative distortion and an absolute distortion maximum. Both limits apply to all equipment. This table is included here as an example of a line distortion specification. It is not intended to be used for design purposes. The IEC has not finalized the requirements of IEC 555 at this time and major changes are possible.

Active Power Factor Correction

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either

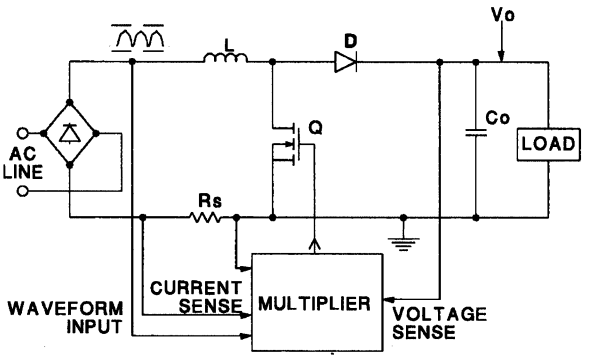


Figure 1

Basic Configuration of High Power Factor Control Circuit

peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854. Peak current mode control has a low gain, wide bandwidth current loop which generally makes it unsuitable for a high performance power factor corrector since there is a significant error between the programming signal and the current. This will produce distortion and a poor power factor.

Average current mode control is based on a simple concept. An amplifier is used in the feedback loop around the boost power stage so that input current tracks the programming signal with very little error. This is the advantage of average current mode control and it is what makes active power factor correction possible. Average current mode control is relatively easy to implement and is the method described here.

A block diagram of a boost power factor corrector circuit is shown in Figure 1. The power circuit of a

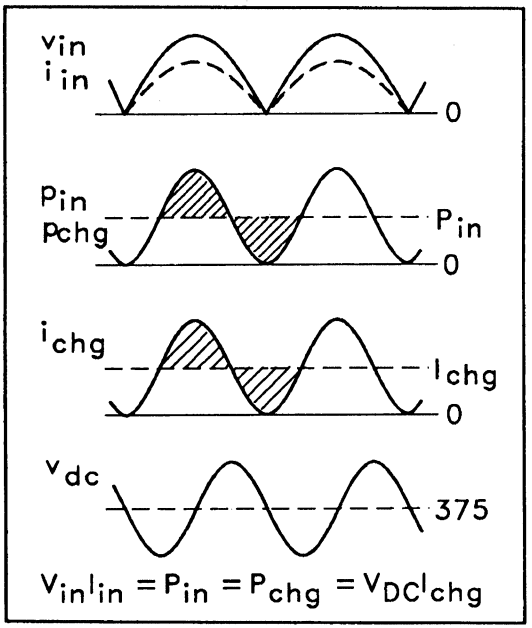


Figure 2. Preregulator Waveforms

boost power factor corrector is the same as that of a dc to dc boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.

The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. This is shown in Figure 2. The top waveform shows the voltage and the current into the power factor corrector and the second waveform shows the flow of energy into and out of the output capacitor. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow. The third waveform in Figure 2 shows the charging and discharging current. This current has a different shape from the input current and is almost entirely at the second harmonic of the AC line voltage. This flow of energy into and out of the capacitor results in ripple voltage at the second harmonic also and this is shown in the fourth waveform in Figure 2. Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

Control Circuits

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Figure 3 is a block diagram which shows the basic control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called Imo for multiplier output current. The multiplier input from the rectified line voltage is shown as a current in Figure 3 rather than as a voltage signal because this is the way it is done in the UC3854.

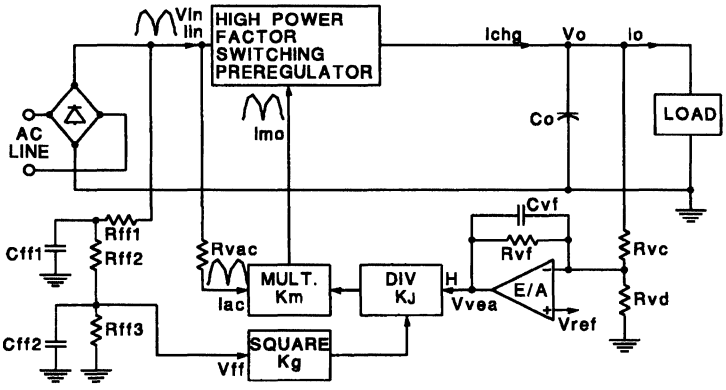


Figure 3. High Power Factor

Figure 3 shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feedforward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage (Vvea).

The current programming signal must match the rectified line voltage as closely as possible to maximize the power factor. If the voltage loop bandwidth were large it would modulate the input current to keep the output voltage constant and this would distort the input current horribly. Therefore the voltage loop bandwidth must be less than the input line frequency. But the output voltage transient response must be fast so the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keep the loop gain constant so the bandwidth can be as close as possible to the line frequency to minimize the transient response of the output voltage. This is especially important for wide input voltage ranges.

The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control. The output of the voltage error amplifier actually controls the power delivered to the load. This can be seen easily from an example. If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feedforward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector. This can be used to limit the maximum power which the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

Input Distortion Sources

The control circuits introduce both distortion and displacement into the input current waveform. These errors come from the input diode bridge, the multiplier circuits and ripple voltage, both on the output and on the feedforward voltage.

There are two modulation processes in an active power factor corrector. The first is the input diode bridge and the second is the multiplier, divider, squarer circuit. Each modulation process generates cross products, harmonics or sidebands between the two inputs. The description of these mathematically can be quite complex. Interestingly enough, however, the two modulators interact and one becomes a demodulator for the other so that the result is quite simple. As shown later, virtually all of the ripple voltages in an active power factor corrector are at the second harmonic of the line frequency. When these voltages go through the multiplier and get programmed into the input current and then go through the input diode bridge the second harmonic voltage amplitude results in two frequency components. One is at the third harmonic of the line frequency and the other is at the fundamental. Both of these components have an amplitude which is half of the amplitude of the original second harmonic voltage. They also have the same phase as the original second harmonic. If the ripple voltage is 10% of the line voltage amplitude and is phase shifted 90 degrees the input current will have a third harmonic which is 5% of the fundamental and is shifted 90 degrees and a fundamental component which is 5% of the line current and is displaced by 90 degrees.

The feedforward voltage comes from the rectified AC line which has a second harmonic component that is 66% of the amplitude of the average value. The filter capacitors of the feedforward voltage divider greatly attenuate the second harmonic and effectively remove all of the higher harmonics but some of the second harmonic is still present at the feedforward input. This ripple voltage is squared by the control circuits as shown in Figure 3. This doubles the amplitude of the ripple since it is riding on top of a large DC value. The divider process is transparent to the ripple voltage so it passes on to the multiplier and eventually becomes third harmonic distortion of the input current and a phase displacement. The doubling action of the squarer means that the amplitude of the input current distortion in percent is the same as the amplitude of the ripple voltage, in percent, at the feedforward input.

Needless to say, the feedforward ripple voltage must be kept small to achieve a low distortion input current. The ripple voltage could be made small with a single pole filter with a very low cutoff frequency. However, fast response to changes of the input voltage is also desirable so the response time of the filter must be fast. These two requirements are, of course, in conflict and a compromise must be found. A two pole filter on the feedforward input has a faster transient response than a single pole filter for the same amount of ripple attenuation. Another advantage of the two pole filter has is that the phase shift is twice that of the single pole filter. This results in 180 degrees of phase shift of the second harmonic and brings both the resulting third harmonic and the displacement component of the input current back in phase with the voltage. A second harmonic ripple voltage of 3% at the feedforward input results in a 0.97 power factor just from the displacement component if a single pole filter is used for the feedforward voltage. With a two pole filter there is no displacement component to the power factor because it is in

phase with the input current. The third harmonic component of the input current resulting from the second harmonic at the feedforward input will have the same amplitude as the second harmonic ripple voltage. If 3% second harmonic is present on the feedforward voltage the line current waveform will contain 3% third harmonic distortion.

The output voltage has ripple at the second harmonic due to the ripple current flowing through the output capacitor. This ripple voltage is fed back through the voltage error amplifier to the multiplier and, like the feedforward voltage, programs the input current and results in second harmonic distortion of the input current. Since this ripple voltage does not go through the squarer the amplitude of the distortion and displacement are each half of the amplitude of the ripple voltage. The ripple voltage at the output of the voltage error amplifier must be in phase with the line voltage for the displacement component to be in phase. The voltage error amplifier must shift the second harmonic by 90 degrees so that it will be in phase with the line voltage.

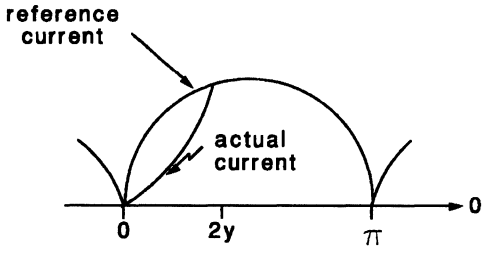


Figure 4. Cusp Distortion

The voltage loop of a boost converter with average current mode control has a control to output transfer function which has a single pole roll off characteristic so it could be compensated with a flat gain error amplifier. This produces a very stable loop with 90 degrees of phase margin. However, it provides less than optimum performance. The ripple voltage on the output capacitor is out of phase with the input current by 90 degrees. If the error amplifier has flat gain at the second harmonic frequency the distortion and displacement generated in the input current will be 90 degrees out of phase with the rectified AC line. The power factor can be improved by introducing phase shift into the voltage error amplifier response. This shifts the displacement component of the power factor back into alignment with the input voltage and increases the power factor. The amount of phase shift which can be added is determined by the need to keep the voltage loop stable. If the phase margin is reduced to 45 degrees the phase at the second harmonic will be very close to 90 degrees and this brings the displacement component back in phase with the input voltage.

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin.

Cusp Distortion

Cusp distortion occurs just after the AC line input has crossed zero volts. At this point the amount of current which is required by the programming signal exceeds the available current slew rate. When the input voltage is near zero there is very little voltage across the inductor when the switch is closed so the current cannot ramp up very quickly so the available slew rate is too low and the input current will lag behind the desired value for a short period of time. Once the input current matches the programmed value the control loop is back in operation and the input current will follow the programming signal. The length of time that the current does not track the programmed value is a function of the inductor value. The smaller the inductor value the better the tracking and the lower the distortion but the smaller inductor value will have higher ripple current. The amount of distortion generated by this condition is generally small and is mostly higher order harmonics. This problem is minimized by a sufficiently high switching frequency.

UC3854 Block Diagram

A block diagram of the UC3854 is shown in Figure 5 and is the same as the one in the device data sheet. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of Figure 5 contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsens. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

The output of the voltage error amplifier, Vvea, is available on pin 7 of the UC3854 and it is also an input to the multiplier. The other input to the multiplier is pin 6, Iac, and this is the input for the programming wave shape from the input rectifiers. This pin is held at 6.0 volts and is a current input. The feedforward input, Vff, is pin 8 and its value is squared before being fed into the divider input of the multiplier. The Iset current from pin 12 is also used in the multiplier to limit the maximum output current. The output current of the multiplier is Imo and it flows out of pin 5 which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin 4, the Isens pin. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin 14. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin 16. The output voltage is clamped internally to the UC3854 at 15 volts so that power MOSFETs will not have their gates over driven. An emergency peak current limit is provided on pin 2 and it will shut the output pulse off when it is pulled slightly below ground. The reference voltage output is connected to pin 9 and the input voltage is connected to pin 15.

DESIGN PROCESS

Power Stage Design

This analysis of the power stage design makes use of a 250W boost converter as an example. The control circuit for a boost power factor corrector does not change much with the power level of the converter. A 5000 watt power factor corrector will have almost the same control circuits as a 50 watt

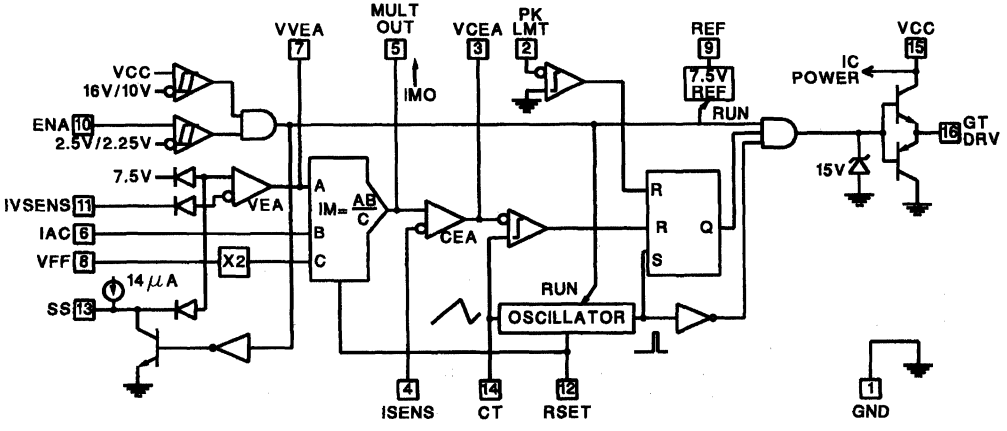


Figure 5. UC3854 Block Diagram

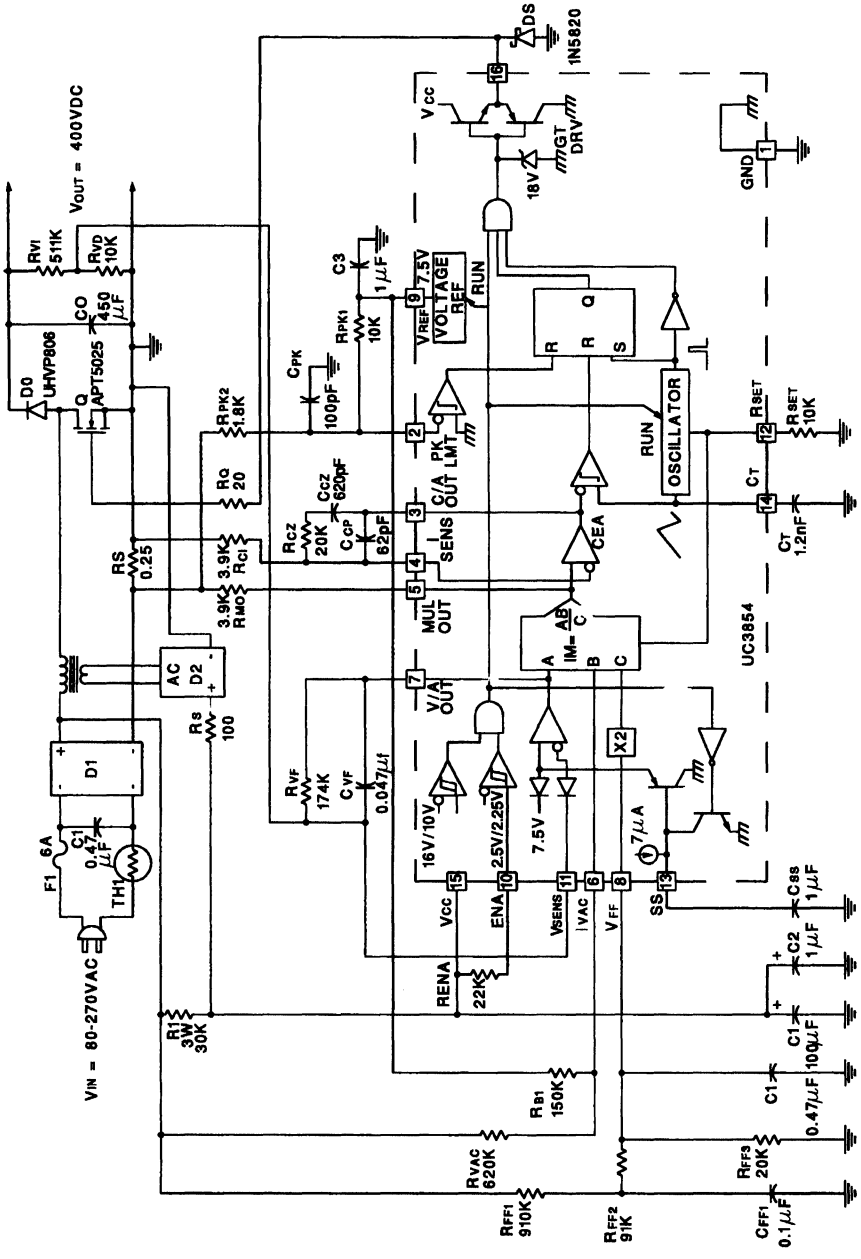


Figure 6.
Complete Schematic of 250W Power Factor Preregulator

corrector. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design process is the same and the power stage is scalable a 250 watt corrector serves well as an example and it can be readily scaled to higher or lower output levels. Figure 6 is the schematic diagram of the circuit. Please refer to this schematic in the discussion of the design process which follows.

Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

Maximum power output: 250W

Input voltage range: 80-27OVac

Line frequency range: 47-65Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20KHz to 300KHz proves to be an acceptable compromise. The example converter uses a switching frequency of l00KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak

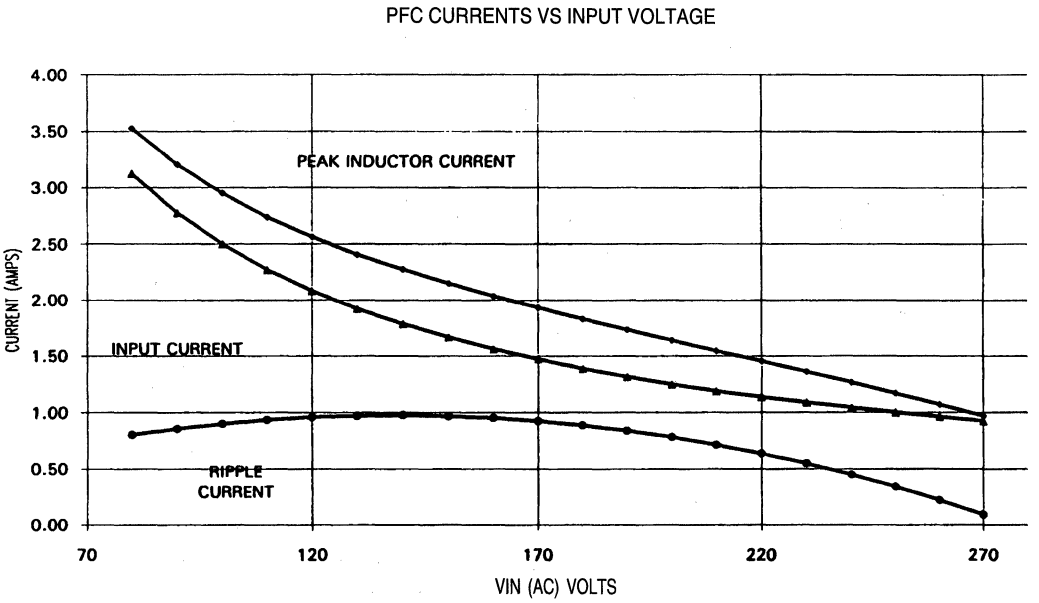


Figure 7

current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I\,line\,(pk) = \frac{\sqrt{2} \times P}{Vin\,(min)}$$

For the example converter the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 7 is a graph of the peak to peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{Vo - Vin}{Vo}$$

$$L = \frac{Vin \times D}{fs \times \Delta I}$$

Where ΔI is the peak-to-peak ripple current. In the example 250W converter D=0.71, ΔI=900ma, and L=0.89mH. For convenience the value of L is rounded up to 1.0mH.

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2μF per watt of output. In our 250W example the output capacitor is 450μF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2μF per watt, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capacitance value in terms of the hold-up time.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - Vo\,(min)^2}$$

Where Co is the output capacitor, Pout is the load power, Δt is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. For the example converter Pout is 250W, Δt is 64msec, Vo is 400V and Vo(min) is 300V so Co is 450μF.

Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation. The choice of these components is beyond the scope of this Application Note. The switch must have a current rating at least equal to the maximum peak current in

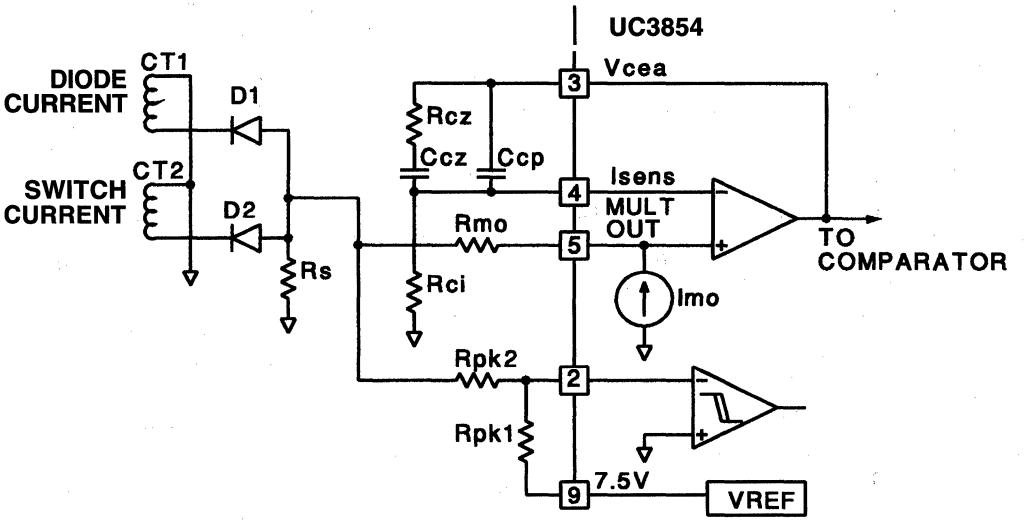


Figure 8.
Current Transformers Used
with Negative Output

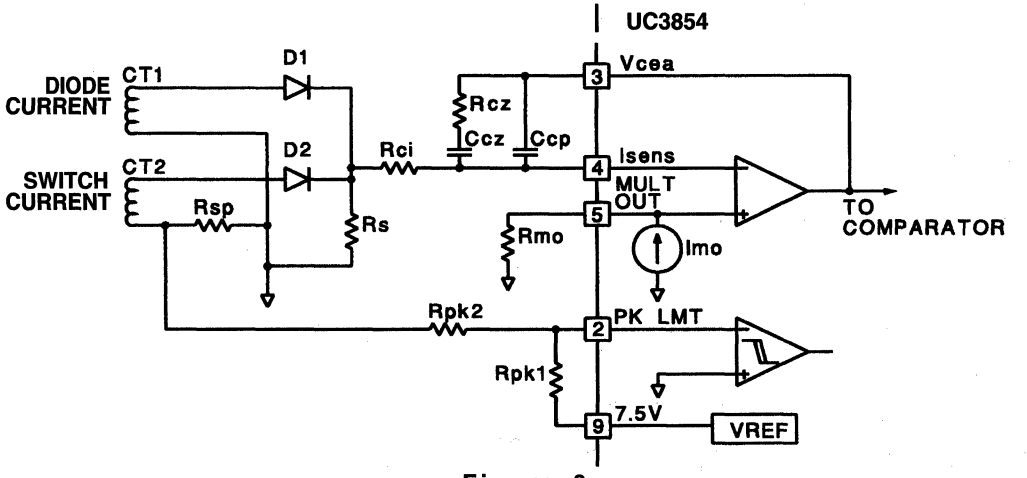


Figure 9.
Current Transformers Used
with Positive Output

the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the example circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 500Vdc breakdown and 23Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 8, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 9, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figures 8 and 9 respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 9) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 6) so the inverting input to the current error amplifier (pin 4) is connected to ground through Rci. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be zero. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor Rmo). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be zero because it is connected through Rci to ground.

The voltage across Rs, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 volt or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25 ohm resistor was chosen for Rs in the example converter and at the worst case peak current of 5.6 amps gives a maximum voltage of 1.40V peak.

Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor.

The equation for the voltage divider is given below:

$$Rpk2 = \frac{Vrs \times Rpk1}{Vref}$$

Where Rpk1 and Rpk2 are the resistors of the voltage divider, Vref is 7.5 volts on the UC3854, and Vrs is the voltage across the sense resistor Rs at the current limit point. The current through Rpk2 should be around 1 mA. The peak current limit in the example circuit is set at 5.4 amps with an Rpk1 of 10K and Rpk2 of 1.8K. A small capacitor, Cpk, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current Iac (pin 6) the feedforward voltage Vff from the input (pin 8) and the voltage error amplifier output voltage Vvea (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

Where Km is a constant in the multiplier and is equal to 1.0, Iac is the programming current from the rectified input voltage, Vvea is the output of the voltage error amplifier and Vff is the feedforward voltage.

Feedforward Voltage

Vff is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a Vff range of 1.4 to 4.5 volts. The UC3854 has an internal clamp which limits the effective value of Vff to 4.5 volts even if the input goes above that value. The voltage divider for the Vff input has three resistors (Rff1, Rff2 and Rff3 - see Figure 6) and two capacitors (Cff1 and Cff2) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270Vac the average value of a half sine will be 243Vdc and the peak will be 382V.

The Vff voltage divider has two DC conditions to meet. At high- input line voltage Vff should not be greater than 4.5 volts. At this voltage the Vff input clamps so the feedforward function is lost. The voltage divider should be set up so that Vff is equal to 1.414 volts when Vin is at its low line value and the upper node of the voltage divider, Vffc, should be about 7.5 volts. This allows Vff to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the Vff input goes below 1.414 volts. The Vff input should always be set up so that Vff is equal to 1.414 volts at the minimum input voltage. This may cause Vff to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have Vff clip at the high end rather than to have the multiplier output clip on the low end of the range. If Vff clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of Vff is 4.5 volts. If Rff1, the top resistor of the divider, is 910K and Rff2, the middle resistor, is 91 K and Rff3, the bottom resistor, is 20K the maximum value of Vff will be 4.76 volts when the input voltage is 270Vac RMS and the DC average value will be 243 volts. When the input voltage is 80Vac RMS the average value is 72 volts and Vff is 1.41Vdc. Also at Vin=80Vac the voltage at the upper node on the voltage divider, Vffc, will be 7.83 volts. Note that the high end of the range goes above 4.5 volts so that the low end of the range will not go below 1.41 volts.

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, Vvea, is clamped inside the UC3854 at 5.6 volts. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given Vvea voltage regardless of line voltage changes. If 5.0V is established as the maximum normal operating level then 5.6V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of Vff at 1.414 volts. This can be seen by plugging these values into the equation for the multiplier output current given above. When Vff is large the inherent errors of the multiplier are magnified because Vvea/Vff becomes small. If the application has a wide input voltage range and if a very low harmonic distortion

is required then Vff may be changed to the range of 0.7 to 3.5 volts. To do this an external clamp MUST be added to the voltage error amplifier to hold its output below 2.00 volts. In general, however, this is not a recommended practice.

Multiplier Input Current

The operating current for the multiplier comes from the input voltage through Rvac. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6mA. At high line the peak voltage for the example circuit is 382Vdc and the voltage on pin 6 of the UC3854 is 6.0Vdc. A 620K value for Rvac will give an Iac of 0.6mA maximum. For proper operation near the cusp of the input waveform when Vin=0 a bias current is needed because pin 6 is at 6.0Vdc. A resistor, Rb1, is connected from Vref to pin 6 to provide the small amount of bias current needed. Rb1 is equal to Rvac/4. In the example circuit a value of 150K for Rb1 will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for Imo, given above, for this condition. The peak value of Iac will be 182 microamps when Vin is at low line. Vvea will be 5.0 volts and Vff will be 2.0. Imo will then be 365 microamps maximum. Imo may not be greater than twice Iac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The Iset current places another limitation on the multiplier output current. Imo may not be larger than 3.75 / Rset. For the example circuit this gives Rset = 10.27K maximum so a value of 10K is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. Rmo, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be zero under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 amps in the example circuit and the current sense resistor is 0.25 ohms so the peak voltage across the sense resistor is 1.4 volts. The maximum multiplier output current is 365 microamps so the summing resistor, Rmo, must be 3.84K and a 3.9K resistor is chosen.

Oscillator Frequency

The oscillator charging current is Iset and is determined by the value of Rset and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$Ct = \frac{1.25}{Rset \times fs}$$

Where Ct is the value of the timing capacitor and fs is the switching frequency in Hertz. For the example converter fs is 100KHz and Rset is 10K so Ct is 0.00125µF.

Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (Rs) forming a low pass filter. The equation for the control to input current transfer function is:

$$\frac{Vrs}{Vcea} = \frac{Vout \times Rs}{Vs \times sL}$$

Where Vrs is the voltage across the input current sense resistor and Vcea is the output of the current error amplifier. Vout is the DC output voltage, Vs is the peak-to-peak amplitude of the oscillator ramp, sL is the impedance of the boost inductor (also jwL), and Rs is the sense resistor (with a current transformer it will be Rs/N). This equation is only valid for the region of interest between the resonant frequency of the filter (LCo) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (Vin=0) the inductor current is given by the ratio of the converter output voltage and the inductance (Vo/L). This current flows through the current sense resistor Rs and produces a voltage

with the slope VoRs/L (with current sense transformers it will be VoRs/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Where fci is the current loop crossover frequency and Rcz/Rci is the gain of the current error amplifier. This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400Vdc and the inductor is 1.0mH so the down slope of inductor current is 400mA per microsecond. The current sense resistor is 0.25 ohms so the input to the current error amplifier is 100mV per microsecond. The oscillator ramp of the UC3854 has a peak to peak value of 5.2V and the switching frequency is 100KHz so the ramp has a slope of 0.52 volts per microsecond. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (Rci) value of 3.9K the feedback resistance (Rcz) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9KHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45 degrees. If the zero is lower in frequency the phase margin will be greater. A 45 degree phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of Rcz. The equation is: Ccz = 1 / (2π x fci x Rcz). The example converter has Rcz=20K and fci=l5.9KHz so Ccz=500pF. A value of 620pF was chosen to give a little more phase margin.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62pF capacitor for Ccp which gives a pole at 128KHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62pF is adequate in this case.

Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90 degrees. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$Vopk = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), fr is the ripple frequency which is the second harmonic of the input line frequency, Co is the value of the output capacitance and Vo is the DC output voltage. The example converter has a peak ripple voltage of 1.84Vpk.

The amount of distortion which the ripple contributes to the input must be decided next. This deci-

sion is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range (ΔVvea) of 1.0 to 5.0 volts so the peak ripple voltage at the output of the voltage error amplifier is give by Vvea(pk) = %Ripple x ΔVvea. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, Gva, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter Gva is 0.0326.

The criteria for the choice of Rvi, the next step in the design process, are reasonably vague. The value must be low enough so that the opamp bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511 K resistor was chosen for Rvi and it will have power dissipation of about 300mW.

Cvf, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$Cvf = \frac{1}{2\pi fr \times Rvi \times Gva}$$

The example converter has a Cvf value of 0.08μF. If this value is rounded down to Cvf=0.047μF the phase margin will be a little better with only a little more distortion so this value was chosen.

The output voltage is set by the voltage divider Rvi and Rvd. The value of Rvi is already determined so Rvd is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example Rvd=l0K will give an output voltage of 390Vdc. This could be trimmed up to 400VDC with a 414K resistor in parallel with Rvd but for this application 390Vdc is acceptable. Rvd has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$Gbst = \frac{Pin \times Xco}{\Delta Vvea \times Vo}$$

Where Gbst is the gain of the boost stage including the multiplier, divider and squarer, Pin is the average input power, Xco is the impedance of the output capacitor, ΔVvea is the range of the voltage error amplifier output voltage (4 volts on the UC3854) and Vo is the DC output voltage.

The gain of the error amplifier above the pole in its frequency response is given by:

$$Gva = \frac{Xcf}{Rvi}$$

Where Gva is the gain of the voltage error amplifier, Xcf is the impedance of the feedback capacitance and Rvi is the input resistance.

The gain of the total voltage loop is the product of Gbst and Gva and is given by the this equation:

$$Gv = \frac{Pin \times Xco \times Xcf}{\Delta Vvea \times Vo \times Rvi}$$

Note that there are two terms which are dependent on f, Xco and Xcf. This function has a second order slope (-40dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set Gv equal to one and rearrange the equation to solve for fvi. Xco is replaced with 1/(2πfCo) and Xcf is replaced with 1/(2πfCvf).

The equation becomes:

$$fvi^2 = \frac{Pin}{\Delta Vvea \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Solving for fvi in the example converter gives fvi=19.14Hz. The value of Rvf can now be found by setting it equal to the impedance of Cvf at fvi. The equation is: Rvf=1 /(2πfviCvf).

In the example converter a value of 177K is calculated and 174K is used.

Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (Cff1 and Cff2) attenuate the ripple voltage from the rectified input voltage. The

second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the "gain" of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is Gff = 1.5 / 66.2 = 0.0227.

The recommended divider string impliments a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$fc = \sqrt{Gff} \times fr$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120Hz so the cutoff frequency is fc=0.15x120=18Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this applivation, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

In the example converter Rff2 is 91K and Rff3 is 20K; so,

Cff1=1/2πx18x91K=0.1μF;

Cff2=1/2πx18x20K=0.44μF;

so choose Cff2=0.47μF.

This completes the design of the major circuits of an active power factor corrector.

DESIGN PROCEDURE SUMMARY

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:

   Pout (max): 250W
   Vin range: 80-270Vac
   Line frequency range: 47-65Hz
   Output voltage: 400Vdc

2. Select switching frequency:

   Example:

   100KHz

3. Inductor selection:

   A. Maximum peak line current. Pin = Pout(max)

   $$Ipk = \frac{\sqrt{2} \times Pin}{Vin\ (min)}$$

   Example:

   Ipk=1.41 x250/80=4.42 amps

   B. Ripple current.

   $\Delta I = 0.2 \times Ipk$

   Example:

   ΔI=0.2x4.42= = 0.2x4.42 = 0.9 amps peak to peak

   C. Determine the duty factor at Ipk where Vin(peak) is the peak of the rectified line voltage at low line.

   $$D = \frac{Vo - Vin\ (peak)}{Vo}$$

   Example:

   D=(400-113)/400=0.71

   D. Calculate the inductance. fs is the switching frequency.

   $$L = \frac{Vin \times D}{fs \times \Delta I}$$

   Example:

   L=(113x.71)/(100,000x0.9)=0.89mH

   Round up to 1.0mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for Co are 1 μF to 2μF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. Δt is the hold-up time in seconds and V1 is the minimum output

capacitor voltage.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - V1^2}$$

Example:

Co=(2x250x34msec)/(400-350)=450µF

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0V is a typical value for Vrs.

   A. Find $Ipk(max) = Ipk + \frac{\Delta I}{2}$

   Example:

   Ipk(max)=4.42+0.45 ≈ 5.0amps peak

   B. Calculate sense resistor value.

   $$Rs = \frac{Vrs}{Ipk(max)}$$

   Example:

   Rs=1.0/5.0=0.20 ohms. Choose 0.25ohms

   C. Calculate the actual peak sense voltage.

   Vrs(pk)=Ipk(max)xRs

   Example:

   Vrs(pk)=5.0x0.25=1.25V

6. Set independent peak current limit. Rpk1 and Rpk2 are the resistors in the voltage divider. Choose a peak current overload value, Ipk(ovld). A typical value for Rpk1 is 10K.

   $Vrs(ovld) = Ipk(olvd) \times Rs$

   Example:

   Vrs(ovld)=5.6x0.25=1.4V

   $$Rpk2 = \frac{Vrs(ovld) \times Rpk1}{Vref}$$

   Example:

   Rpk2=(1.4x10K)/7.5=1.87K. Choose 1.8K

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, Km=1 , Iac is the multiplier input current, Vff is the feedforward voltage and Vvea is the output of the voltage error amplifier.

   $$Imo = \frac{Km \times Iac \times (Vvea - 1)}{vff^2}$$

   A. Feedforward voltage divider. Change Vin from RMS voltage to average voltage of the rectified input voltage. At Vin(min) the voltage at Vff should be 1.414 volts and the voltage at Vffc, the other divider node, should be about 7.5 volts. The average value of Vin is given by the following equation where Vin(min) is the RMS value of the AC input voltage:

   $Vin(av) = Vin(min) \times 0.9$

   The following two equations are used to find the values for the Vff divider string. A value of 1 Megohm is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

   $$vff = 1.414v = \frac{Vin(av) \times Rff3}{Rff1 + Rff2 + Rff3}$$

   $$Vnode \approx 7.5V = \frac{Vin(av) \times (Rff2 + Rff3)}{Rff1 + Rff2 + Rff3}$$

   Example:

   Rff1=910K, Rff2=91K, and Rff3=20K

   B. Rvac selection. Find the maximum peak line voltage.

   $Vpk(max) = \sqrt{2} \times Vin(max)$

   Example:

   Vpk(max)=1.414x270=382Vpk

   Divide by 600 microamps, the maximum multiplier input current.

   $$Rvac = \frac{Vpk(max)}{600E\text{-}6}$$

   Example:

   Rvac=(382)/6E-4=637K. Choose 620K

   C. Rb1 selection. This is the bias resistor. Treat this as a voltage divider with Vref and Rvac and then solve for Rb1. The equation becomes:

   Rb1 = 0.25 Rvac

   Example:

   Rb1=0.25Rvac=155K. Choose 150K

   D. Rset selection. Imo cannot be greater than twice the current through Rset. Find the multiplier input current, Iac, with Vin(min). Then calculate the value for Rset based on the value of Iac just calculated.

   $$Iac(min) = \frac{Vin(pk)}{Rvac}$$

   Example:

   Iac(

   $$Rset = \frac{3.75}{2 \times Iac(min)}$$

   Example:

Rset=3.75V/(2x182μA)=10.3Kohms.

Choose 10 Kohms

E. Rmo selection. The voltage across Rmo must be equal to the voltage across Rs at the peak current limit at low line input voltage.

$$Rmo = \frac{Vrs\ (pk)\ x\ 1.12}{2\ x\ Iac(min)}$$

Example:

Rmo=(l.25x1.12)/(2x182E-6)=3.84K.

Choose 3.9Kohms

8. Oscillator frequency. Calculate Ct to give the desired switching frequency.

$$Ct = \frac{1.25}{Rset \times fs}$$

Example:

Ct=1.25/(10K x 100K)=1.25nF.

9. Current error amplifier compensation.

A. Amplifier gain at the switching frequency. Calculate the voltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (Rs/N) for Rs. The equation is:

$$\Delta Vrs = \frac{Vo \times Rs}{L \times fs}$$

Example:

ΔVrs=(400x0.25)/(0.001 =(400x0.25)/(0.001 x100,000)=1.0Vpk

This voltage must equal the peak to peak amplitude of Vs, the voltage on the timing capacitor (5.2 volts). The gain of the error amplifier is therefore given by:

$$Gca = \frac{Vs}{\Delta Vrs}$$

Example:

Gca=5.2/1.0=5.2

B. Feedback resistors. Set Rci equal to Rmo.

Rci = Rmo

Rcz = Gca x Rci

Example:

Rcz=5.2x3.9K=20Kohms

C. Current loop crossover frequency.

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Example:

fci=(400x0.25x20K)/(5.2x2πx0.001

=15.7KHz

D. Ccz selection. Choose a 45 degree phase margin. Set the zero at the loop crossover frequency.

$$Ccz = \frac{1}{2\pi \times fci \times Rcz}$$

Example:

Ccz=1/(2πx15.7Kx20K)=507pF.

Choose 620pF

E. Ccp selection. The pole must be above fs/2.

$$Ccp = \frac{1}{2\pi \times fs \times Rcz}$$

Example:

Ccp=1/(2πx1 100Kx20K)=80pf.

Choose 62pF

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes 1/2% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, Vff, contributes 1% third harmonic to the input current for each 1% second harmonic at the Vff input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the Vff input and 0.75% is allocated to the output ripple voltage or 1.5% to Vvao. The remaining 0.75% is allocated to miscellaneous nonlinearities.

11. Voltage error amplifier compensation.

A. Output ripple voltage. The output ripple is given by the following equation where fr is the second harmonic ripple frequency:

$$Vo\ (pk) = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Example:

Vo(pk)=250/(2π120x450E-6x400)=1.84Vac

B. Amplifier output ripple voltage and gain. Vo(pk) must be reduced to the ripple voltage allowed at the output of the voltage error amplifier. This sets the gain of the voltage error amplifier at the second harmonic frequency. The equation is:

$$Gva = \frac{\Delta Vvao \times \%Ripple}{Vo\ (pk)}$$

For the UC3854 Vvao is 5-1=4V

Example:

Gva=(4x0.015)/1.84=0.0326

C. Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of Rvi is reasonably arbitrary.

Example:

Choose Rvi=511K

$$Cvf = \frac{1}{2\pi \times fr \times Rvi \times Gva}$$

Example:
Cvf=1/(2πx120x511Kx0.0326)=0.08μF.

Choose 0.047μF

D. Set DC output voltage.

$$Rvd = \frac{Rvi \times Vref}{Vo - Vref}$$

Example:

Rvd=(511Kx7.5)/(400-7.5)=9.76K.

Choose 10.0K

E. Find pole frequency. fvi = unity gain frequency of voltage loop.

$$fvi^2 = \frac{Pin}{\Delta Vvao \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Example:

$$fvi = \sqrt{(250/(4x400x511Kx450E-6x47E-9x39.5))} =$$

19.1 Hz

F. Find Rvf.

$$Rvf = \frac{1}{2\pi \times fvi \times Cvf}$$

Example:

Rvf=1/(2πx19.1 x47E-9)=177K. Choose 174K

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10 above.

$$Gff = \frac{\%THD}{66.2\%}$$

Example:

Gff=1.5/66.2=0.0227

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$fp = \sqrt{Gff} \times fr$$

Example:

fp=0.15xl20=18Hz

Select Cff1 and Cff2.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

Example:

Cff1=1/(2πx18x91K)=0.097μF. Choose 0.10μF

Cff2=1/(2πx18x20K)=0.44μF. Choose 0.47μF

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UC3855A/B HIGH PERFORMANCE POWER FACTOR PREREGULATOR

James P. Noon
New Product
Applications Engineer

INTRODUCTION

The trend in power converters is towards increasingly higher power densities. Usually, the method to achieve this is to increase the switching frequency, which allows a reduction in the filter component's size. Raising the switching frequency however, significantly increases the system switching losses which generally precludes operating at switching frequencies greater than 100kHz.

In order to increase the switching frequency while maintaining acceptable efficiency, several soft switching techniques have been developed [1,2,3]. Most of these resonant techniques increase the semiconductor current and/or voltage stress, leading to larger devices and increased conduction losses due to greater circulating current. A new class of converters has been developed [4], however, that allow an increase in switching frequency without the associated increase in switching losses, while overcoming most of the disadvantages of the resonant techniques. Zero voltage transition (ZVT) converters operate at a fixed frequency while achieving zero voltage turn-on of the main switch and zero current turn-off of the boost diode. This is accomplished by employing resonant operation only during switch transitions. During the rest of the cycle, the resonant network is essentially removed from the circuit and converter operation is identical to its nonresonant counterpart.

This technique allows a improvement in efficiency over the traditional boost converter, as well as operating the boost diode with reduced stress (due to controlled di/dt at turn-off). Soft-switching of the diode also reduces EMI, an important system consideration.

Active power factor correction programs the input current of the converter to follow the line voltage and power factors of 0.999 with THD of 3% are possible. The Unitrode UC3855A/B IC incorporates power factor correction control circuitry capable of providing high power factor with several enhancements relating to current sensing and ZVT operation of the power stage.

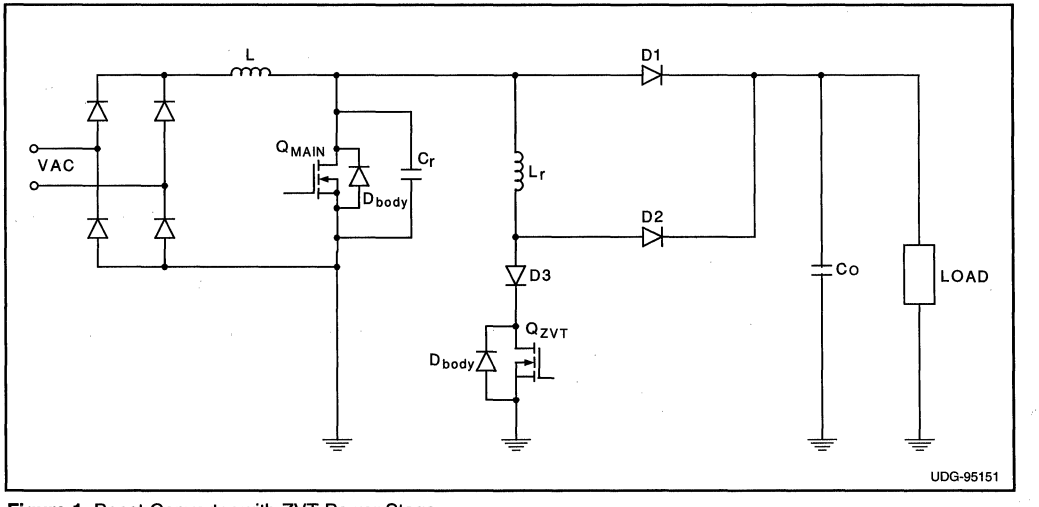


Figure 1. Boost Converter with ZVT Power Stage

The UC3855 incorporates all of the control functions required to design a ZVT power stage with average current mode control. Average current mode control has been chosen for its ability to accurately program the input current while avoiding the slope compensation and poor noise immunity of other methods [5,6].

ZVT TECHNIQUE

ZVT Boost Converter Power Stage

The ZVT boost converter operates the same as a conventional boost converter throughout its switching cycle except during the switch transitions. Figure 1 shows the ZVT boost power stage. The ZVT network, consisting of Q_{ZVT} , D2, L_r, and C_r, provides active snubbing of the boost diode and main switch. The ZVT circuit operation has been described in [4, 7, 8] and will be reviewed here for completeness. Referring to Figure 2, the following timing intervals can be defined:

ZVT Timing

t_0 - t_1 During the time prior to t_0, the main switch is off and diode D1 is conducting the full load current. At t_0, the auxiliary switch (Q_{ZVT}) is turned on. With the auxiliary switch on, the current in L_r ramps up linearly to I_{IN}. During this time the current in diode D1 is ramping down. When the diode current reaches zero the diode turns off (i.e. soft switching of D1). In the practical circuit some reverse recovery of the diode will occur since the diode needs time to remove the junction charge. The voltage across the ZVT inductor is V_O, and therefore the time required to ramp up to I_{in} is:

$$t_{01} = \frac{I_{IN}}{\left(\frac{V_O}{L_r}\right)}$$

t_1 - t_2 At t_1, the L_r current has reached I_{IN} and L_r and C_r will begin to resonate. This resonant cycle discharges C_r until its voltage equals zero. The dv/dt of the drain voltage is controlled by C_r (C_r is the combination of the external C_{DS} and C_{oss}). The current through L_r continues to increase while C_r discharges. The time required for the drain voltage to reach zero is 1/4 of the resonant period. At the end of this period the body diode of the main switch turns on.

$$t_{12} = \frac{\pi}{2} \bullet \sqrt{L_r C_r}$$

t_2 - t_3 At the beginning of this interval the switch drain voltage has reached 0V and the body diode is turned on. The current through the body diode is being driven by the ZVT inductor. The voltage

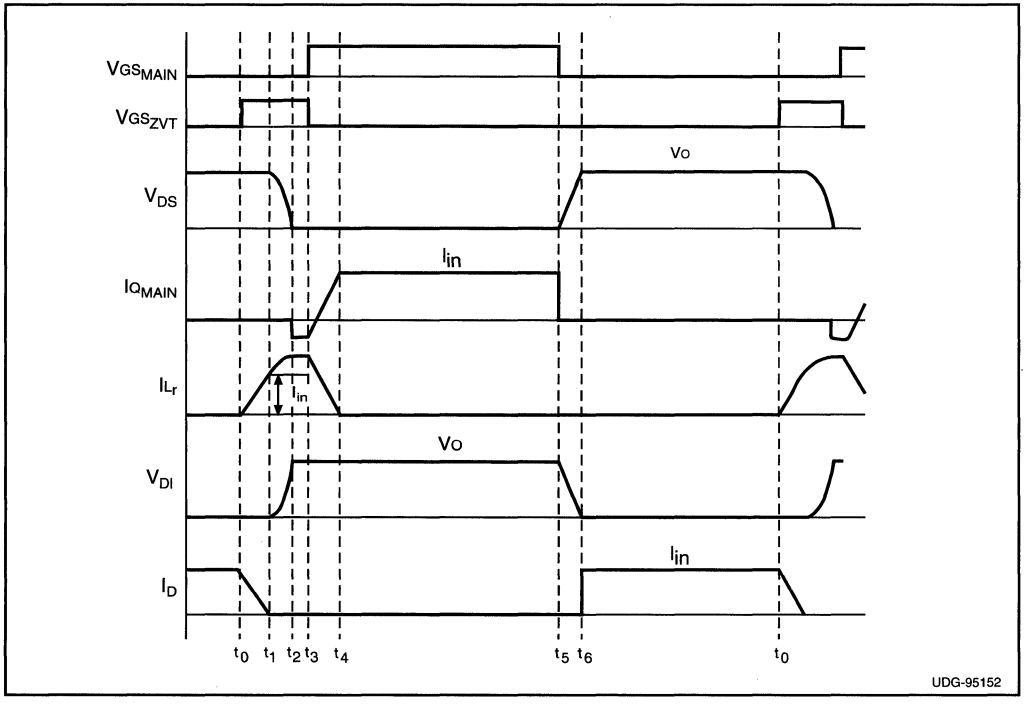


Figure 2. ZVT Timing Diagram

across the inductor is zero and therefore the current freewheels. At this time, the main switch can be turned on to achieve zero voltage switching.

t_3 - t_4 At t_3, the UC3855 senses that the drain voltage of Q_{MAIN} has fallen to zero and turns on the MAIN switch while turning off the ZVT switch. After the ZVT switch turns off, the energy in L_r is discharged linearly through D2 to the load.

t_4 - t_5 At t_4, the current in D2 goes to zero. When this occurs, the circuit is operating like a conventional boost converter. In a practical circuit however, L_r will resonate with C_{oss} of the ZVT switch driving the node at the anode of D1 negative (since the opposite end of L_r is clamped to zero). This effect will be discussed in the ZVT circuit design section.

t_5 - t_6 This stage is also exactly like a conventional boost converter. The main switch turns off. The Q_{MAIN} drain-to-source node capacitance charges to V_O and the main diode begins to supply current to the load. Since the node capacitance initially holds the drain voltage to zero, the turn off losses are significantly reduced.

It can be seen through the above description that the operation of the converter differs from the conventional boost only during the turn-on switch transitions. The main power stage components experience no more voltage or current stress than normal, and the switch and diode both experience soft switching transitions. Having significantly reduced the switching losses, the operating frequency can be increased without an efficiency penalty. The diode also operates with much lower losses and therefore will operate at a lower temperature, increasing reliability. The soft switching transitions also reduce EMI, primarily caused by hard turn-off of the boost diode.

Control Circuit Requirements

In order to maintain zero voltage switching for the main switch, the ZVT switch must be on until the voltage on C_r resonates to zero. This can be accomplished by using a fixed delay equal to t_{ZVT} at low line and maximum load.

$$t_{ZVT} = \frac{I_{INp} \bullet L_r}{V_O} + \frac{\pi}{2} \bullet \sqrt{L_r \bullet C_r}$$

However, this would give a longer than necessary delay at lighter load or higher line conditions, and therefore would increase the ZVT circuit conduction loss and increase the peak current stress. The UC3855 allows for a variable t_{ZVT} by sensing when the Q_{MAIN} drain voltage has fallen to zero. Once the voltage falls below the ZVS pin threshold voltage (2.5V), the ZVT gate drive signal is terminated and the main switch gate drive goes high. The control waveforms are shown in Figure 3. The switching period begins when the oscillator begins to discharge, and the ZVT gate drive goes high at the beginning of the discharge period. The ZVT signal will stay high until the ZVS pin senses the zero voltage condition or until the discharge period is over (the oscillator discharge time is the maximum ZVT pulse width). This allows the ZVT switch to be on only for as long as necessary.

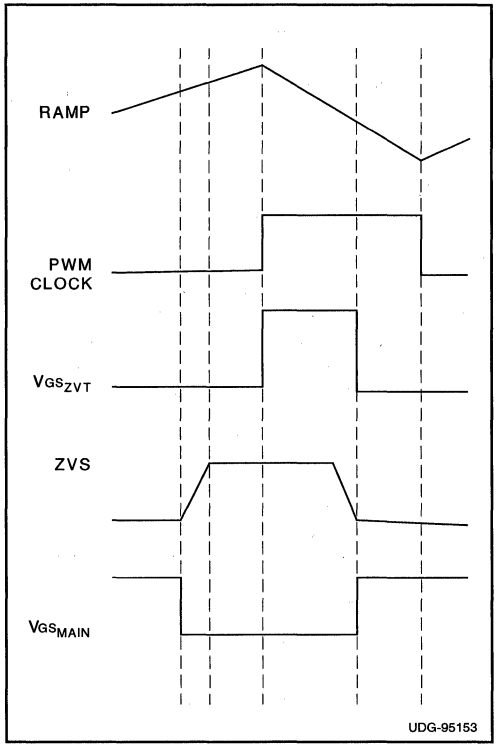
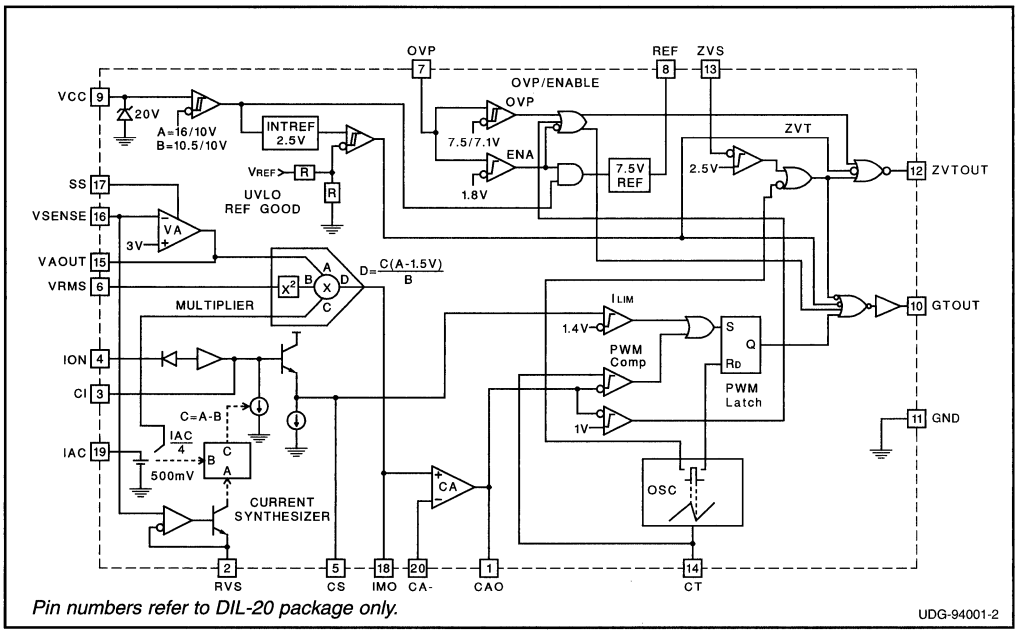


Figure 3. ZVT Control Waveforms

CONTROL CIRCUIT OPERATION AND DESIGN

Figure 4 shows the UC3855A/B block diagram (pin numbers correspond to DIL-20 packages). It shows a controller which incorporates the basic PFC circuitry, including average current mode control, and the drive circuitry to facilitate ZVT operation. The IC also has current waveform synthesizer circuitry to simplify current sensing, as well as overvoltage and overcurrent protection. In the following sections the control IC will be broken down into functional blocks and individually



Pin numbers refer to DIL-20 package only.

UDG-94001-2

Figure 4. UC3855 Controller Block Diagram

reviewed.

Comparison with UC3854A/B

The PFC section of the UC3855A/B is identical to the UC3854A/B. Several common design parameters are highlighted below to illustrate the similarities.

FUNCTION	UC3854A/B	UC3855A/B
Enable	Dedicated pin	Incorporated into OVP
Design Range for V_{RMS}	1.5V - 4.7V	1.5V - 4.7V
V_{REF} for VA	3V	3V
Max. VA Output Voltage	6V	6V
Offset Voltage at IAC	0.5V	0.7V
Multiplier Gain	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \bullet IMO}$	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \bullet IMO}$

New features incorporated into the UC3855A/B include:

ZVT control circuitry
Overvoltage protection
Current Synthesizer

Oscillator

The oscillator contains an internal current source and sink and therefore only requires an external timing capacitor (CT) to set the frequency. The nominal charge current is set to 500µA and the discharge current is 8mA. The discharge time is approximately 6% of the total period, which defines the maximum ZVT time. CT is calculated by:

$$CT = \frac{1}{11200 \bullet F_S}$$

ZVT Control Circuit

As stated in the ZVT Technique section, the UC3855A/B provides the control logic to ensure ZVT operation over all line and load conditions without using a fixed delay. The ZVS pin senses the MOSFET drain voltage and is an input to the ZVT drive comparator. The other comparator input is internally biased to 2.5V. When the ZVS input is above 2.5V (and the PWM clock signal is present) the ZVT drive signal can go high. Pulling the ZVS pin low will terminate the ZVT drive signal and turn on the main switch output (recall that the maximum ZVT output signal is equal to the oscillator dis-

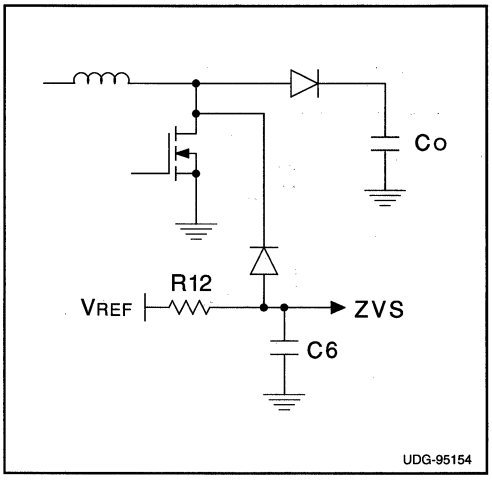


Figure 5. ZVS Sensing Circuit

charge time). The network used to sense the node voltage is shown in Figure 5. R12 pulls up the pin to a maximum of 7.5V, and C6 provides filtering. The RC time constant should be fast enough to reach 2.5V at maximum duty cycle. The drain voltage is limited by the node capacitance which slows down the dv/dt across the main MOSFET, which reduces the high speed requirement on the ZVS circuit. The maximum ZVS pin voltage should be limited to V_{REF}, otherwise the ZVS circuitry can become latched and will not operate properly.

An alternative method for ZVS operation, is to sense the drain voltage through a simple voltage divider. This voltage will still have to be filtered (and clamped) however, so as not to inject noise into the ZVS pin.

Refer back to Figure 3 for the timing waveforms.

GATE DRIVES

The main drive can source $1.5A_{PK}$ and the ZVT drive is $0.75A_{PK}$. The main switch drive impedance requirements are reduced due to ZVT operation. At turn-on the drain voltage is at zero volts and therefore the Miller capacitance effect is not an issue, and during turn-off, the dv/dt is limited by the resonant capacitor. Since the ZVT MOSFET is generally at least two die sizes smaller than the main switch, its drive requirements are met with a lower peak current capability.

Multiplier / Divider Circuit

The multiplier section of the UC3855A/B is identical to the UC3854A/B. It incorporates input voltage feedforward (through the VRMS input) to eliminate loop gain dependence on the input voltage. There are only three parameters (V_{VRMS}, I_{IAC}, and R_{IMO}) that need to be defined to properly set up the IC.

VRMS

The multiplier programs the line current and therefore effects the power drawn from the line. The VRMS pin is programmed by looking at the system power limits. Referring to the block diagram (Figure 4), the multiplier output equation is:

$$I_{IMO} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V^2_{VRMS}}$$

The power limit function is set by the maximum output voltage of the voltage loop error amplifier, V_{EA} (6V). The power limiting function is easily explained by looking at what happens for a given value of V_{EA}. If the AC line decreases by a factor of two, the feedforward voltage decreases by one fourth. This increases multiplier output current (and therefore line current) by two. The power drawn from the line has therefore remained constant. Conversely, if the load increases and the line stays constant, V_{EA} will increase, causing more line current to be drawn. It can be seen then, that V_{EA} is a voltage proportional to input power.

Normally the multiplier is set to limit maximum power at low line, corresponding to maximum error amplifier output voltage. The multiplier equation can be solved for the feedforward voltage that corresponds to maximum error amplifier voltage and maximum multiplier current (internally limited to 2 times I_{IAC}).

$$V^2_{VRMS} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{2 \bullet (I_{IAC})}$$

$$V_{VRMS} = 1.5V$$

Knowing the VRMS voltage at low line defines the voltage divider from the line to VRMS pin. This feedforward voltage must be relatively free of ripple in order to reduce the amount of second order harmonic that is present at the multiplier input (which in turn would cause 3rd order harmonics in the input current) [9]. The filtering will produce a dc voltage at the VRMS pin. Since the input voltage is defined in terms of its RMS value, the dc to RMS factor (0.9) must be taken into account [9]. For example, if the low line voltage is 85V, the attenuation required is:

$$\frac{85V_{RMS} \bullet (0.9)}{1.5 \bullet V_{DC}} = 51:1$$

At a high line of 270V, this will correspond to V_{VRMS} = 4.76V. The common mode range of the VRMS input is 0V to 5.5V. The calculated range is there-

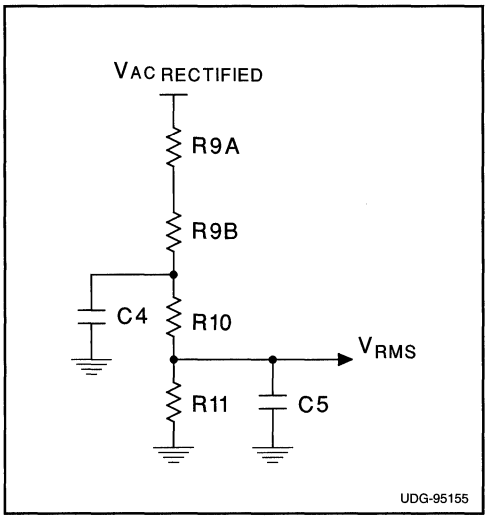


Figure 6. VRMS Circuit

fore within the accepted limits.

A two pole filter is recommended to provide adequate attenuation without degrading the feedforward transient response. A single pole filter will require a pole at too low of a frequency to still allow VRMS to respond quickly enough to changes in line voltage.

The filter poles can be calculated once the distortion contribution from V_{RMS} is determined. If the feedforward circuit's contribution to the total distortion is limited to 1.5%, the required attenuation of the filter can be calculated. Recall that the percentage of 2nd harmonic in a full wave rectified sinewave is approximately 66.7% of the dc value. The percentage of second harmonic will translate to the same percent 3rd harmonic distortion in the input current waveform [9]. Therefore, the filter attenuation required is:

$$\frac{1.5\%}{66.7\%} = 0.0025$$

The individual stages should have an attenuation of $\sqrt{0.0225}$ or 0.15. For a single stage filter:

$$A_V = \frac{f_c}{f} \Rightarrow f_c = 120Hz\ (0.15) = 18Hz$$

Referring to Figure 6 the components correspond to R9A = R9B = 390kΩ, R10 = 120kΩ, and R11 = 18kΩ with C4 = 0.082µF and C5 = 0.47µF.

I_{IAC}

The value of I_{IAC} is chosen to be 500µA at high line. This value is somewhat arbitrary, however it should be kept below 1mA to stay within the linear region of the multiplier. This corresponds to a total resistance of approximately 766kΩ from the line to IAC pin.

R_{IMO}

The multiplier output resistor can be calculated by recognizing that at low line and maximum load current, the multiplier output voltage will equal 1V (in order to stay below the undercurrent trip point). This will also correspond to the maximum sense voltage of the current transformer. The multiplier current under this condition is equal to 1V / R_{IMO}, and can be equated with the multiplier equation which yields:

$$\frac{1V}{R_{IMO}} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V^2_{VRMS}}$$

At low line I_{IAC} will equal 156µA (if low line = 85V and I_{IAC} was set to 500µA at 270V), V_{EA} will be at its maximum of 6V, and V_{VRMS} will be 1.5V. Therefore R_{IMO} equals 3.2kΩ.

Current Synthesizer

Current sensing is simplified due to the current synthesis function built into the UC3855A/B. Switch current is the same as inductor current when the switch is on and can be sensed using a single current transformer. The current synthesizer charges a capacitor (CI) with a current proportional to the switch current when the switch is on. During the switch off-time, the inductor current waveform is reconstructed by the controller. To get an accurate measure of the inductor current then, all that is required is to reconstruct the down slope of the inductor current, which is given by:

$$\frac{\Delta i}{\Delta t} = \frac{V_{OUT} - V_{AC}}{L}$$

Discharging CI with a current proportional to $V_{OUT} - V_{AC}$ will allow reconstruction of the inductor current waveform. The capacitor down slope is :

$$\frac{\Delta v}{\Delta t} = \frac{I_{DIS}}{CI}$$

The UC3855A/B develops I_{DIS} by subtracting $I_{IAC}/4$, from a current proportional to V_{OUT}. The voltage at the RVS pin is regulated at 3V and therefore picking the RVS resistor will set the current proportional to V_{OUT}.

$$I_{DIS} = \frac{3V}{R_{RVS}} - \frac{I_{IAC}}{4}$$

The ratio of the current in R_{RVS} to $I_{IAC}/4$ should

equal the ratio of V_{OUT} to V_{AC}. Therefore if I_{IAC} / 4 is 125µA, the current through R_{RVS} should be set to 130µA.

$$R_{RVS} = \frac{3V}{130\mu A} = 23k\Omega, \text{ use } 22k\Omega$$

Equating inductor current slope with capacitor voltage slope, and recognizing that maximum slope occurs when V_{AC} equals zero, CI can be solved for:

$$CI = \frac{3 \bullet L \bullet N}{R_{RVS} \bullet V_{OUT} \bullet R_S}$$

where N is the current transformer (CT) turns ratio, (Ns / Np) and R_S is the current sense resistor.

The current synthesizer has approximately 20mV of offset. This offset can cause distortion at the zero crossing of the line current. To null out this offset, a resistor can be connected between VREF and the IMO pin. The resistor value is calculated based on R_{IMO} and the offset at the output of the synthesizer. For a 20mV offset and R_{IMO} = 3.3k a resistor from VREF to IMO of 1.2MΩ will cancel the offset.

Current Sensing

Current Transformer

As was seen in the previous section, synthesizing inductor current with the UC3855A/B is quite simple. Only switch current needs to be sensed directly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation.

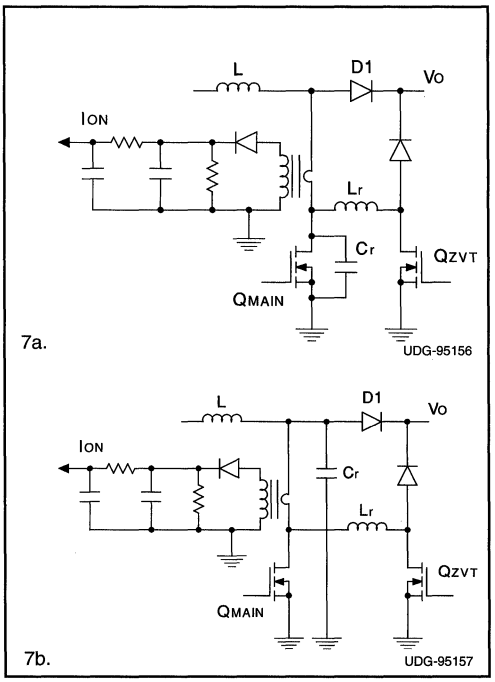


Figure 7. Current Transformer Sensing.

Several issues should be kept in mind when implementing the current transformer. At frequencies of a couple hundred kilohertz, core reset needs to be addressed. Contributing to the difficulty is the very high duty cycles inherent in a power factor correction circuit. In addition, the ZVT circuit can complicate the sensing/reset function. When the ZVT circuit turns on, it draws current from the line. In order to minimize line current distortion, this current should be measured. Placing the resonant inductor after the current transformer will ensure that the ZVT circuit current is measured. Similarly, when the main switch turns off, current will continue to flow into the resonant capacitor. While it is important to measure this current, if the capacitor is connected to the drain of the MOSFET, below the current transformer, this current will "eat" into the minimal reset time available at line zero crossings, where duty cycles are approaching 100%. This configuration is shown in Figure 7a. If the current transformer does not have enough time to reset, it can begin to saturate and lose accuracy, even if complete saturation is avoided, causing distortion at the zero crossings. A better configuration is shown in Figure 7b. In this circuit, the capacitor current will be measured when it discharges during the ZVT circuit on time. Since this occurs at the beginning of the switching cycle, the current transformer doesn't lose any of its reset time. Connecting C_r above the current transformer will not adversely affect the MOSFET dv/dt control. Since the IC is controlling average current, it doesn't matter whether the capacitor current is measured at the beginning or end of the switching cycle.

Figure 7 also shows that filtering is added to the transformer secondary in order to reduce noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.

In addition to position and reset considerations, actual current transformer construction must be considered. Using current transformers that have been designed and manufactured for operation at 20kHz will not give good performance at switching frequencies of 100kHz and greater. Low frequency designs generally have too much leakage inductance to be used for high frequency operation and can cause inaccurate sensing and/or noise problems.

Resistive Sensing

Resistive sensing is still possible with the UC3855A/B. Since both inputs to the current error

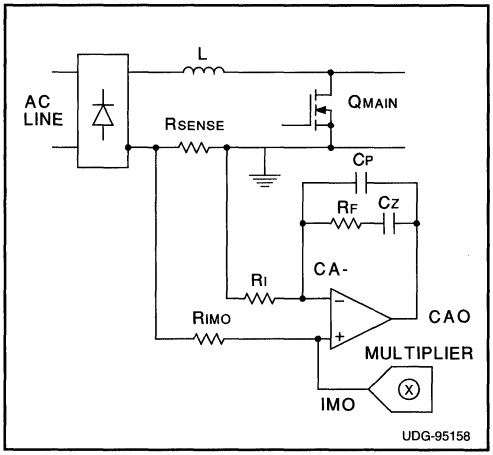


Figure 8. Resistive Sensing

amplifier are available to the user, resistive sensing is easy to implement. Figure 8 shows the typical configuration. The common mode range of the current error amplifier is –0.3V to 5.0V. The R_{IMO} value will remain the same as was calculated above if the maximum signal level remains at 1V. This will also allow the resistively sensed signal to be fed into ION and used for peak current limiting. It is recommended that the RVS resistor still be connected and a resistor connected from CS to ground in order to eliminate the possibility of noise being injected into these high impedance nodes.

Current Error Amplifier

The current error amplifier ensures that the input current drawn from the line follows the sinusoidal reference. The positive input to the amplifier is the multiplier output. The negative input is connected to the output of the current synthesizer (CS) through a resistor (usually the same value as R_{IMO}). The output of the current error amplifier is compared to the sawtooth waveform at the PWM comparator and terminates the duty cycle accordingly. At zero crossings of the line, the duty cycle will be at its maximum. Since the duty cycle is approaching 100%, proper reset of the current transformer will become increasingly difficult. Standard PWM controllers terminate the duty cycle during the oscillator discharge time, however, due to the ZVT operation, the UC3855A/B is capable of achieving 100% on-time. If the duty cycle is allowed to approach 100%, the current transformer will begin to saturate and cause the current error amplifier to "believe" that less current is being drawn from the line than is being commanded. This will cause the current amplifier to overcompensate, causing line current distortion at the zero crossings. In addition, if the current transformer saturates, the current limiting function will be lost. For these reasons it is recommended that the output of the current amplifier be clamped externally, to limit the maximum duty cycle. Figure 9 shows a typical clamp circuit.

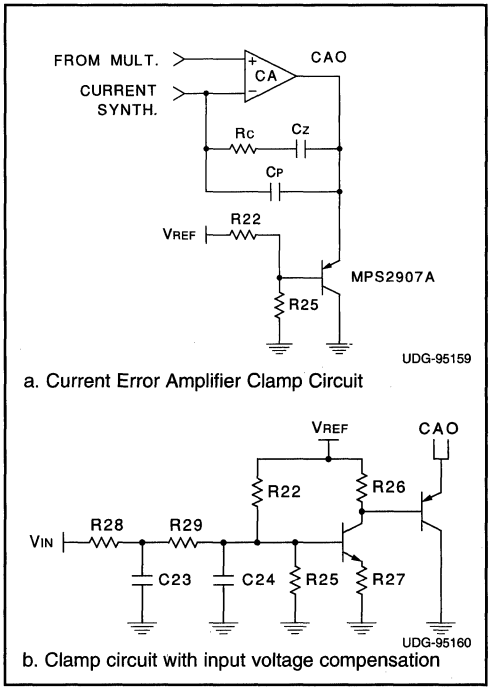


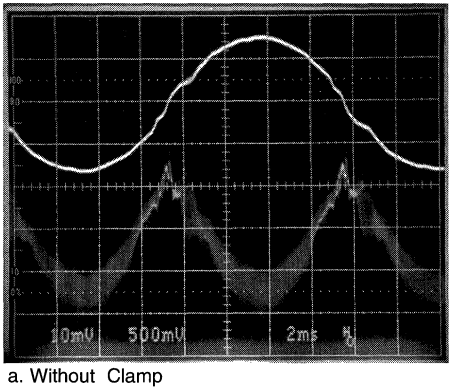
Figure 9. Clamp Circuit

The clamp circuit in Figure 9a will perform quite well (see Table 1), however if better performance is required, or if it's required to operate over a wide line range, the circuit in Figure 9b can be used. This circuit adjusts the clamp voltage to be inversely proportional to line voltage.

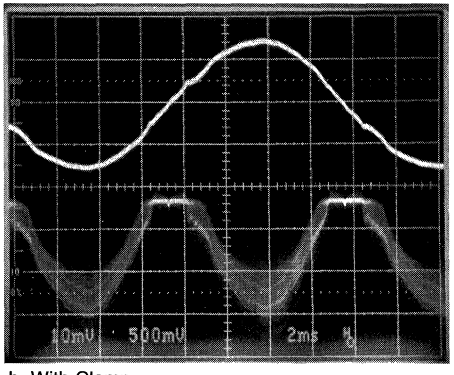
The procedure for setting the clamp voltage is quite easy. If during initial startup the current amplifier clamp is set to a relatively low value (≈ 4V) the system will operate but with excessive zero crossing distortion. Once the system is operating, the clamp voltage can be increased until the current transformer is not saturating, and line current has an acceptable level of THD. Once the clamp voltage is set, operation with other ICs will be repeatable. In the experimental breadboard built for universal line operation and 500W output, the single stage clamp was set to 5.6V (at low line and maximum load) and an acceptable level (< 10%) of THD was

measured over all line and load conditions. The clamp voltage is being set below the peak of the PWM comparator ramp (nominally 6.5V) to limit D_{MAX}. Setting the clamp voltage too low will cause excess zero crossing distortion due to the amplifier not being able to command enough line current.

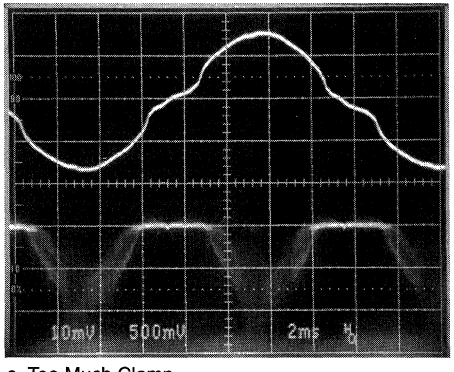
Figures 10a and 10b show the current amplifier operation with and without the clamp, while Figure 10c shows the effect of clamping the amplifier output voltage too low (top waveform is line current, bottom is V_{CAO}). Setting the clamp too high will have the same effect as having no clamp.



a. Without Clamp



b. With Clamp



c. Too Much Clamp

Figure 10. C/A Clamp Circuit Effects on I Line

The procedure for setting the two stage clamp circuit is the same except that the voltage contribution from the line must be factored in. The line voltage will only have to contribute 100mV to 200mV of clamp voltage for line compensation.

At very light or no load conditions, the average current drawn from the line is lower than can normally be commanded by the current error amplifier. To prevent an overvoltage condition from occurring, the IC goes into a pulse skipping mode if the output voltage of the error amplifier goes below ≈ 1V. Pulse skipping can also occur at high line and low load conditions. When C_{AO} goes below 1V, the pulse skipping comparator is activated. The output of the comparator goes to an input of an OR gate in the OVP/ENABLE circuit, causing the output of that OR gate to go high. This signal prevents the ZVT and main gate drives from going high.

The procedure for compensating the current error amplifier will be covered in the Design Procedure section (IV).

Voltage Error Amplifier

The output voltage is sensed by the VSENSE input to the voltage error amplifier and compared to an internally generated reference of 3V. The output of the amplifier, V_{EA}, (at a given input voltage) will vary proportionally with output power. The output voltage range for the voltage error amplifier is approximately 0.1V to 6V. The output of the amplifier is one of the multiplier inputs, and an input voltage below 1.5V will inhibit the multiplier output. The design procedure for compensating the voltage loop will be outlined in the Design Procedure section.

Protection Circuitry

OVP/ENABLE

The UC3855A/B combines the enable and OVP function into one pin. It requires a minimum of 1.8V to enable the IC, and below this voltage, the reference is held low and the oscillator is disabled. A voltage above 7.5V will interrupt the gate drive. The resistor divider should be sized for 7.5V when an over voltage condition is reached, this will allow startup at a reasonable line voltage. For example, if an overvoltage condition is defined as an output voltage exceeding 450V, then the voltage divider from V_{OUT} to the OVP pin is 60:1. This divider will allow startup at a line voltage of $76V_{RMS}$ ($108V_{PK}$).

Current Limit

The UC3855A/B has pulse by pulse current limiting. The multiplier power limit determines the maximum average power drawn from the line. However, during transients or overload conditions, a peak current limiting function is necessary. This function is implemented by sensing the switch current and feeding this value into ION, to a current limiting comparator that terminates the gate drive signal if the switch current signal exceeds 1.5V (nominal).

Soft Start

In order to ensure a smooth, controlled startup, the UC3855A/B provides a soft-start (SS) function. The SS pin sources 1.5µA into an external capacitor. This capacitor limits the supply voltage to the voltage loop error amplifier, which effectively limits the output voltage of the amplifier and therefore the maximum commanded output voltage. This allows the output voltage to ramp up in a controlled fashion.

Undervoltage Lockout

The UC3855A has a 15.5V (nominal) turn-on threshold with 6V of hysteresis while the UC3855B turns on at 10.5V with 0.5V of hysteresis.

TYPICAL APPLICATION

A typical application will be designed in order to illustrate the design procedure and highlight the design parameters that need to be defined. The design specifications are:

- V_{IN} = 85 - 270 VAC
- V_O = 410 VDC
- P_{omax} = 500W
- F_S = 250kHz
- Eff > 95%
- Pf > 0.993
- THD < 12%

The above specifications represent a common universal input voltage, medium power application. The switching frequency of 250kHz is now possible due to the soft switching, zero voltage transitions. The Pf and THD numbers correspond to achievable line correction with the UC3855.

Design Procedure

This design procedure is a summary of what was presented in [8]. However, several values have been changed in order to consolidate component values and/or specify more readily available parts.

1. Power Stage Design

Inductor Design

The power stage inductor design in a ZVT converter is identical to the conventional boost converter. The inductance required is determined by the amount of switching ripple desired, and allowing more ripple will reduce the inductor value. The worst case for peak current occurs at low line, maximum load. Peak power is equal to twice the average power and V_{PK} is $\sqrt{2}\ V_{RMS}$. To calculate input current, assume an efficiency of 95%.

$$I_{PK} = \frac{\sqrt{2} \bullet P_{IN}}{2 \bullet V_{INmin}} = \frac{\sqrt{2} \bullet \left(\frac{500}{0.95}\right)}{85}$$

$$= 8.7A \text{ (60Hz component)}$$

A good compromise between current ripple and peak current is to allow a 20% ripple to average ratio. This will also keep the peak switch current less than 10A.

$$\Delta I_L = 0.2 \bullet (8.7A) = 1.7A_{pp}$$

Rearranging the conversion ratio for the boost converter to solve for D yields :

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{410 - \sqrt{2} \bullet 85}{410} = 0.71$$

We can now calculate the required inductance.

$$L = \frac{V_{IN} \bullet D \bullet T_S}{\Delta I} = \frac{\sqrt{2} \bullet 85V \bullet (0.71 \bullet 4\mu s)}{1.7A}$$

$$= 200\mu H$$

Output Capacitor Selection

The value of output capacitor effects both hold-up time and output voltage ripple. If hold up time (t_H) is the main criteria, the following equation will give a value for C_O:

$$C_O = \frac{2 \bullet P_O \bullet t_H}{V_O^2 - V^2_{MIN}}$$

In this example a compromise between holdup time and capacitor size was made and a capacitor value of 440µF was selected. The capacitor bank consists of two 220µF, 450V DC capacitors in parallel.

Power MOSFET & Diode Selection

The main MOSFET selected is an Advanced

Power Technology's APT5020BN (or equivalent). This is a 500V, 23A device, with $R_{DS(on)}$ = 0.20Ω (25°C) and $C_{OSS} \approx$ 500pF in a TO-247 package. A 5.1Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn-on with a Schottky diode and 2.7Ω resistor in parallel with the resistor to speed up turn-off. A Schottky is also placed from GTOUT to ground to prevent the pin from being driven below ground, and should be placed as close to the IC as possible.

The boost diode selected is the International Rectifier HFA15TB60, a 15A, 600V ultrafast diode (or equivalent). Recall that a converter employing ZVT benefits from soft switching of the diode. With ZVT, the boost diode has a negligible impact on switching losses, and therefore a slower diode could potentially be used. However, there are still valid reasons for using an ultra fast diode in this application.

The ZVT inductor is sized according to the recovery time of the diode, and a slower diode will require a larger inductor. This will require a correspondingly longer Q_{ZVT} on-time, which increases conduction loss. A larger inductor will also require a longer time to discharge. To ensure complete discharge of the resonant inductor, the main switch minimum on-time should be approximately equal to the ZVT circuit on-time. This yields:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T}$$

D_{MIN} effects the minimum allowable output voltage for the boost converter to continue operating. The ZVT circuit on-time is a strong function of t_{rr}, and therefore choosing an ultra fast diode will keep the resonant circuit losses to a minimum and cause the least impact on the output voltage. The effective system duty cycle is primarily a function of the main switch on-time, since for a large portion of the resonant circuit's on-time, the voltage at the anode of the boost diode is held up by the resonant capacitor.

These considerations suggest a diode with a recovery time less than 75ns. Average output current in this design is less than 1.2A with a peak current of 9.2A. The conduction loss associated with the diode is approximately 2.2W.

While an ultra fast diode is being used, the diode is operating with significantly reduced switching losses. This will increase the overall system efficiency and reduce the peak stress of the diode.

2. ZVT Circuit Design

Resonant Inductor

The ZVT circuit design is straightforward. The circuit is performing an active snubber function and, as such, the inductor is designed to provide soft turn off of the diode. The ZVT capacitor is selected to provide soft switching of the MOSFET.

The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the ZVT switch turns on, the input current is diverted from the boost diode to the ZVT inductor. The inductor value can be calculated by determining how fast the diode can be turned off. The diode's turn-off time is given by its reverse recovery time. Calculating an exact value for L_r is difficult due to the variation in reverse recovery characteristics within the actual circuit as well as variations in how reverse recovery is specified from manufacturer to manufacturer. An example of circuit conditions effecting the reverse recovery is the natural snubbing action of the resonant capacitor, which limits the dv/dt at the anode of the diode. A good initial estimate is to allow the inductor current to ramp up to the diode current within three times the diode's specified reverse recovery time. One constraint on the maximum inductance value is its affect on the minimum duty cycle. As was shown in the diode selection section, the L-C time constant effects D_{MIN} and therefore V_{Omin}. Making L_r too large will also increase the conduction time of the ZVT MOSFET, increasing the resonant circuit conduction losses. As the value of L_r is reduced, the diode will experience more reverse recovery current, and the peak current through the inductor and ZVT MOSFET will increase. As the peak current is increased, the amount of energy stored in the inductor will also increase ($E = 1/2 \bullet L \bullet I^2$). This energy should be kept to a minimum in order to reduce the amount of parasitic ringing in this node at turn-off.

The reverse recovery of the diode is partially a function of its turn-off di/dt. If a controlled di/dt is assumed, the reverse recovery time of this diode can be estimated to be approximately 60ns. If the inductor limits the rise time to 180ns ($3 \bullet t_{rr}$), the inductance can be calculated.

$$\frac{di}{dt} = \frac{I_{INp}}{3 \bullet t_{rr}} = 53A/\mu s$$

$$I_{INp} = I_{pk} + \frac{\Delta I}{2}$$

$$L_r = \frac{V_O}{di/dt} = \frac{410V}{53A/\mu s} = 7.7\mu H$$

The inductor design is limited by core loss and resultant temperature rise, not saturating flux density. This is due to the high AC current component and the relatively high operating frequency. A good

design procedure is outlined in [10] and is beyond the scope of this review. Several points will be mentioned however. The core material should be a good high frequency, low loss material such as gapped ferrite or molypermalloy powder (MPP). Powder iron cores will generally not be acceptable in this application. The less expensive Magnetics Kool Mu material, although exhibiting higher losses than the MPP material, can also be used. The higher loss material will actually tend to damp the resonant ringing at the turn off of the ZVT switch. The inductor winding construction is also optimized by keeping interwinding capacitance to a minimum. This reduces the node capacitance at turn off and reduces the amount of damping required.

The inductor current can by found by analyzing the resonant circuit formed by L_r and C_r and recognizing that the resonant cycle begins when the current reaches I_{IN}.

$$I_{L_r} = I_{IN} + \frac{V_O}{Z_n} \bullet \sin\omega t$$

$$\text{where } Z_n = \sqrt{L_r / C_r} \quad , \omega = \sqrt{\frac{1}{L_r \bullet C_r}}$$

The peak current then is equal to I_{IN} plus the output voltage divided by the resonant circuit's characteristic impedance. Decreasing L_r or increasing C_r will increase the peak current. The inductor was designed using a Magnetics, Inc. MPP core 55209 with 33 turns for an inductance of 8µH. The inductor should be constructed with Litz wire or several strands of small magnet wire to minimize high frequency effects.

Resonant Capacitor

The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The APT5020BN has approximately 500pF of output capacitance, and an external capacitance of 500pF was added across the device. This capacitor limits the dv/dt at turn-off and consequently reduces the Miller effect. In addition, it reduces turn-off losses since the switch current is diverted to the capacitor. The capacitor must be a good high frequency capacitor, and low ESR and ESL are required. It must also be capable of handling the relatively large charging current at turn-off. Two good choices are polypropolene film or a ceramic material.

This combination of L and C yields a resonant quarter cycle of:

$$\frac{\pi}{2} \sqrt{L_r \bullet C_r} = 140\text{ns}$$

The resonant circuit's impact on the output voltage can now be calculated. Recall that to ensure discharge of the resonant inductor at high line:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T} \qquad (1)$$

and for a boost converter:

$$V_{OMIN} = \frac{V_{INpk}}{1 - D_{MIN}} \qquad (2)$$

Substituting (1) into (2) and solving for V_O produces:

$$V_{OMIN} = \frac{(L_r \bullet I_{INp} + V_{INp} \bullet T}{\left(T - t_{rr} - \frac{\pi}{2} \bullet \sqrt{L_r \bullet C_r}\right)} \qquad (3)$$

Equation (3) can be solved using the previously established values and yields a minimum output voltage of 405V. This suggests a design value of 410V for V_O.

ZVT Switch and Rectifier Selection

The ZVT switch also experiences minimal turn-on loss due to the discharge of its drain-to-source capacitance. However, it doesn't experience high current and voltage overlap since the turn-on current is limited by the resonant inductor. The switch does experience turn-off and conduction losses however. Although the peak switch current is actually higher than the main switch current, the duty cycle is small, keeping conduction losses low. The ZVT switch will be one or two die sizes smaller than the main switch due to the low average drain current. The ZVT switch on-time is :

$$t_{ZVT} = \frac{I_{INp} \bullet L_r}{V_O} + \frac{\pi}{2} \bullet \sqrt{L_r C_r}$$

The peak ZVT switch current is equal to the peak ZVT inductor current. A conservative approximation of the switch RMS current is made by assuming a square wave signal. The RMS of the current is approximated by:

$$I_{RMS} \approx I_{L_{rpk}} \bullet \sqrt{\frac{t_{ZVT}}{T}}$$

This corresponds to a peak of approximately 14A at maximum load and maximum ZVT on-time, however, the RMS is only 3.9A. An appropriate device in this application is the Motorola MTP8N50E, a 500V, 8A device with an $R_{DS(ON)}$ of 0.8Ω. As with the main MOSFET, a 5.1Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn on and a Schottky diode and resistor is placed in parallel with the resistor to speed up turn-off. A Schottky is also placed from ZVTOUT to ground to

prevent the pin from being driven below ground. This diode should be placed as close to the IC as possible.

The rectifiers needed for the ZVT circuit also experience relatively low RMS current. Diode D2 returns the energy stored in the resonant inductor during t_{ZVT} to the load. D2 should be an ultra-fast recovery diode and is usually chosen to be of similar speed as D1. The diode selected for D2 is a Motorola MURH860; a 600V device with a $t_{rr} \approx 35$ns.

Diode D3 blocks current from flowing up through the Q_{ZVT} body diode when the inductor resets, it sees the same peak and RMS current as Q_{ZVT}. D3 should be a fast recovery diode to decouple the drain to source capacitance of Q_{ZVT} from the resonant inductor. Energy stored in the D3 anode node capacitance will resonate with the ZVT inductor when the ZVT switch turns off. Minimizing this effect will reduce the amount of snubbing required at this node. The diode chosen here was the MUR460. This is a 600V, 4 amp device with $t_{rr} \approx 75$ns.

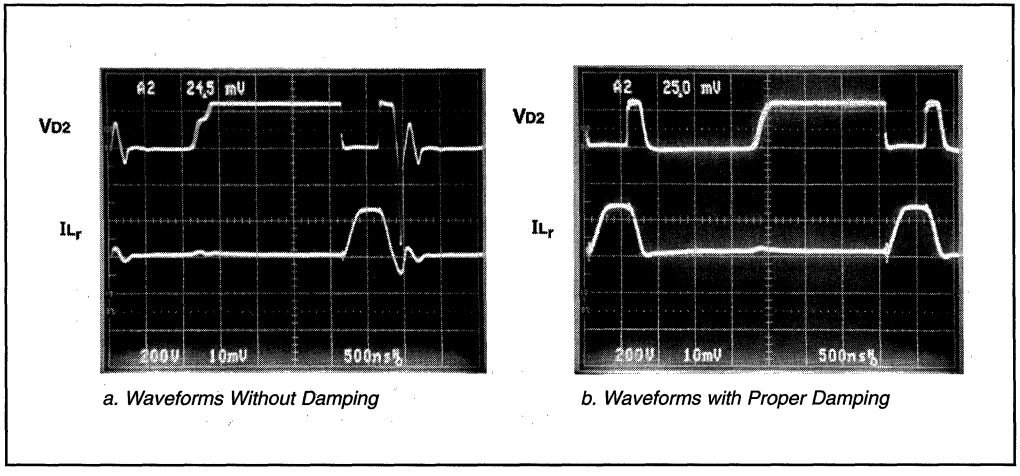
To summarize, both diodes in the ZVT circuit experience low RMS current. The main selection criteria in addition to the blocking voltage (in both cases equal to V_O) is reverse recovery time. Choosing devices with fast recovery times will reduce parasitic oscillations, losses, and EMI.

ZVT Snubber Circuit

The ZVT circuit requires some method for damping the parasitic oscillations that occur after the ZVT inductor current goes to zero. Figure 10a shows the ZVT inductor current and diode D2 anode voltage without adequate damping. The figure shows that as the inductor current begins to discharge (when Q_{ZVT} turns off) to the output, the anode voltage is at V_{OUT} (since D2 is conducting). As the inductor current passes through zero, the voltage rings negative since the opposite end of the inductor is clamped to 0V through the main switch body diode. The anode voltage can easily ring negatively to twice the output voltage. This increases the reverse voltage stress on the diode to three times the output voltage! Keeping the energy in the node capacitance to a minimum and using fast recovery diodes will reduce the ringing and improve the circuit performance.

Several methods of damping this oscillation have been proposed [4,7]. In this circuit two methods, the saturable reactor and resistive damping were investigated. A 51Ω, 10W noninductive resistor was connected through a diode from ground to the anode of D2. The saturable reactor was placed in series with the resonant inductor and implemented with 8 turns on a Toshiba saturable core SA 14 x 8 x 4.5. The resistive damping method prevents the node from oscillating. However, it does not prevent current from flowing in D2 while D1 is conducting (due to the dv/dt across L_r when Q_{MAIN} turns off). If current flows through D2 during this time it will experience reverse recovery current when Q_{ZVT} turns on. The saturable reactor prevents this current flow due to its high impedance. L_S also decouples L_r from the node capacitance, which prevents the node from oscillating.

The saturable reactor works well without the resistive damping and was the method chosen in this design. With the saturable reactor damping the circuit properly, the resistive damping can be eliminated. However, since L_S is designed to saturate each switching cycle, the core loss is largely material dependent and can cause significant temperature



a. Waveforms Without Damping

b. Waveforms with Proper Damping

Figure 11. ZVT Ringing Waveforms

rise of the core. In this circuit, heatsinking of the core was required. An alternative design was also tried using the larger MS 18 x 12 x 4.5 which ran cooler although it also required heatsinking. Optimization of this circuit can significantly reduce the losses in the ZVT circuit. In this design, damping network losses were approximately 2W. Figure 10b shows the same circuit condition with the node damped with L_S.

ZVS Circuit

The ZVS circuit components are chosen next. In this example, a 1kΩ resistor is used to pull up the ZVS pin. The capacitor chosen is 500pF. This combination will require approximately 200ns to charge up to the 2.5V threshold.

$$t = -R \bullet C \bullet ln\left(\frac{1-V_{THRESHOLD}}{V_{REF}}\right)$$

3. Oscillator Frequency

Calculate CT:

The switching frequency selected is 250kHz.

$$CT = \frac{1}{11200 \bullet 250kHz} = 357pF, \text{ use } 330pF$$

4. Multiplier/Divider Circuit

Calculate the VRMS resistor divider:

Set VRMS = 1.5V at low line ($85V_{RMS}$)

$$\text{divider} = \frac{85V_{RMS} \bullet 0.9}{1.5\ V_{DC}} = 51{:}1$$

The voltage divider can be solved if one of the resistors is defined (since there are two equations and three unknowns). Letting the lower resistor in the divider = 18kΩ:

$$R_{TOTAL} = 18k\Omega \bullet 51 = 918k\Omega$$

Letting R10 = 120kΩ, gives:

$$R9 = 918k\Omega - 120k\Omega - 18k\Omega = 780k\Omega$$

R9 is split into two resistors (each 390kΩ) to reduce their voltage stress.

Calculate the capacitor values to place the filter poles at 18Hz:

$$C5 = \frac{1}{2\pi \bullet f_P \bullet R11} = \frac{1}{2\pi \bullet 18Hz \bullet 18k\Omega}$$

$$= 0.49\mu F, \text{ use } 0.47\mu F$$

$$C4 = \frac{1}{2\pi \bullet f_P \bullet R_{eq}} = \frac{1}{2\pi \bullet 18Hz \bullet 117k\Omega}$$

$$= 75nF, \text{ use } 0.082\mu F$$

where $R_{eq} = R9||(R10 + R11) = 117k\Omega$

In order to consolidate capacitor values C4 could be chosen to be 0.1µF without degrading the system performance.

Calculate the IAC resistor:

Set I_{IAC} = 500µA at high line.

$$R = \frac{\sqrt{2} \bullet 270V}{500\mu A} = 764k\Omega$$

Use 2, 390kΩ resistors in series to reduce voltage stress.

Calculate R_{IMO}:

At low line I_{IAC} = 156µA and the output of the multiplier should equal 1V. With low line and maximum load, V_{EA} will be at its maximum of 6V, therefore, using the multiplier output equation:

$$\frac{1V}{R_{IMO}} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V_{VRMS}^2}$$

$$R_{IMO} = \frac{1.5^2}{156\mu A \bullet (6 - 1.5)} = 3.2k\Omega, \text{ use } 3.3k\Omega$$

A 1000pF capacitor is placed in parallel with R_{IMO} for noise filtering. Since the voltage across R_{IMO} is the output of the multiplier and is the reference for the current error amplifier, the RC pole frequency should be placed well above the 120Hz multiplier signal.

5. Current Synthesizer

First, chose a turns ratio for the current transformer. The current transformer is designed to produce 1V at peak input current. This allows sufficient margin before the current limit trip point (1.4V) is reached. If I_{PK} = 9.5A a turns ratio of 50 : 1 would be appropriate. This turns ratio will keep the sense network losses less than 150mW and allow the use of a 1/4 watt resistor. Solving for the sense resistor yields:

$$R_S = \frac{1V}{\frac{I_{sw}}{N}} = \frac{1V}{\frac{9.5}{50}} \approx 5.1\Omega$$

Recall from the previous current synthesizer section that R_{VS} = 22kΩ. The current synthesizer capacitor can now be calculated:

$$CI = \frac{3 \bullet L \bullet N}{R_{VS} \bullet V_{OUT} \bullet R_S}$$

$$= \frac{3 \bullet 200\mu H \bullet 50}{22k\Omega \bullet 410V \bullet 5.1\Omega} = 633pF, \text{ use } 680pF$$

6. Control Loop Design

Small Signal Model

The small signal model of the ZVT PFC boost converter is similar to the standard PFC boost converter model. The two converters operate exactly the

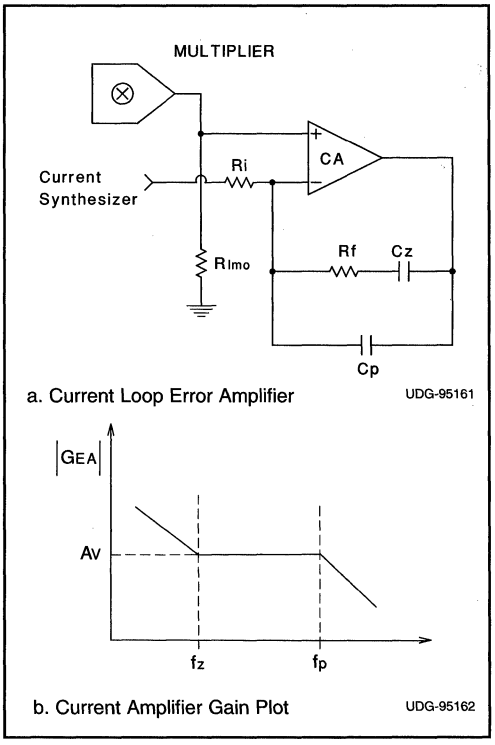


Figure 12. Current Error Amplifier Schematic

same throughout most of the switching cycle and only during the switching transitions is there any difference. This allows the design of the control loops to proceed following the standard techniques outlined in [9].

Current Loop Design

Excellent references on the current loop design are found in [5,9,11]. The design of the average current mode control loop begins with choosing a cross-over frequency. In this example the switching frequency is 250kHz, so the unity gain cross over frequency could be chosen to be as high as 40kHz (1/6 of the switching frequency). In this circuit however, the cross over is chosen to be 10kHz. Since the main job of the current loop is to track the line current, a 10kHz bandwidth is quite adequate for this application.

Once the cross over frequency (f_c) is known, the next thing to do is calculate the gain of the power stage. The small signal model of the power stage including the current sense network is given below. This model does not include the sampling effect at one half the switching frequency [12] but is a good approximation at the frequencies of interest.

$$G_{id}(s) = \frac{V_O \bullet R_{SENSE}}{s \bullet L \bullet V_{SE}}$$

The UC3855A/B has an oscillator ramp of $5.2V_{pp}$ (V_{SE}). The R_{SENSE} term, is the attenuation from actual input current to sensed current (i.e. it includes the current transformer turns ratio). Using the previously determined component values and solving for the power stage gain at f_c yields a gain of 0.63 at 10kHz. In order to have a gain of 1 at f_c, the error amplifier must have a gain of 1/0.63 at 10kHz. The error amplifier is shown in Figure 12a with the frequency response in Figure 12b. The resistor Ri is equal to 3.3kΩ so the feedback resistor is chosen to be 5.6kΩ. A zero is placed at the cross over frequency to give a phase margin of 45 degrees. To reduce switching noise a pole is placed at one-half the switching frequency. The following summarizes the design procedure.

1. $$|G_{id}(s)| = \frac{410V \bullet 0.10}{2 \bullet \pi \bullet 10kHz \bullet 200\mu H \bullet 5.2} = 0.63$$

2. $$G_{EA} = \frac{1}{|G_{id}(s)|} = 1.58 \Rightarrow Av = \frac{R_f}{R_i}$$

$$\therefore R_f = \frac{R_i}{|G_{id}(s)|} \approx 5.6k\Omega$$

3. $$f_z = f_c = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_z}$$

$$C_Z = \frac{1}{2 \bullet \pi \bullet 10kHz \bullet 5.6k\Omega} \approx 2200pF$$

4. $$f_p = \frac{1}{2 \bullet \pi \bullet R_f \left(\frac{C_z \bullet C_p}{C_z + C_p}\right)} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p}$$

$$C_p = \frac{1}{2 \bullet \pi \bullet 5.6k\Omega \bullet 125kHz} \approx 220pF$$

Voltage Loop Design

The design of the voltage loop follows the procedure given in [5]. The first step is to determine the amount of ripple on the output capacitor.

$$v_{Opk} = \frac{P_{IN} \bullet X_{Co}}{V_O}$$

$$V_{Opk} = \frac{525}{2 \bullet \pi \bullet 120 \bullet 410\mu \bullet 410} = 4.14V_{PK}$$
$$= 8.3V_{pp}$$

In order to meet the 3% THD specification, the distortion due to output ripple voltage feeding through the voltage error amplifier will be limited to 0.75%. This allows 1.5% from the multiplier and 0.75% from miscellaneous sources. A 1.5% second harmonic on the error amplifier will result in 0.75% 3 rd harmonic distortion at the input. At full load, the peak error amplifier ripple voltage allowed is:

$$V_{EApk} = \%\,ripple \bullet V_{VEA} = 0.015 \bullet (6 - 1)$$
$$= 0.075V$$

The error amplifier gain at 120Hz is the allowable error amplifier ripple voltage divided by the output ripple voltage, or 0.009 (–41 dB). The error amplifier input resistor was chosen to be 1.36MΩ to keep power dissipation low and allow a small value for the compensation capacitor. Two 681kΩ resistors in series are used to reduce the voltage stress. The voltage error amplifier schematic is shown in Figure 13, with the 120Hz gain determined by the integrator function of C_f and R_i. This network has a single pole role off and the capacitor value is easily found to give the desired gain at 120Hz.

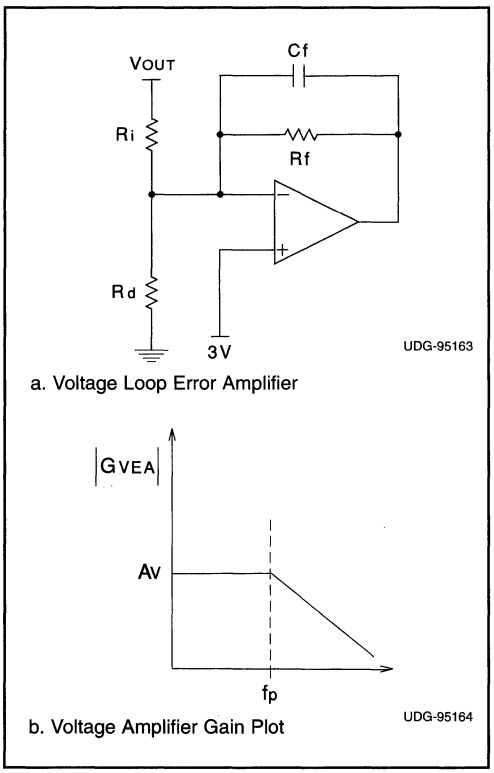


Figure 13. Voltage Error Amplifier

$$C_f = \frac{1}{2 \bullet \pi \bullet f \bullet G_{VEA} \bullet R_i}$$

$$C_f = \frac{1}{2 \bullet \pi \bullet 120Hz \bullet 0.009 \bullet 1.36M\Omega}$$
$$\approx 0.1\mu F$$

The crossover frequency can now be calculated recognizing that a pole (due to the combination of C_f and R_f) will be placed at the cross over frequency to provide adequate phase margin. The pole placement will determine the phase margin since the power stage has a single pole response with the associated 90 degree phase lag. If the error amplifier pole is placed at the crossover frequency, the overall loop gain will have a 45 degree phase margin. The power stage gain is given by:

$$G_{PS}(s) = \frac{V_o}{V_{VEA}} = \frac{P_{IN}}{\Delta V_{EA} \bullet V_o \bullet (s \bullet C_o)}$$

The voltage loop gain (T_V) is the product of the power stage gain and the error amplifier gain. To find the cross over frequency, solve for f and set equal to 1.

$$T_V = 1 = G_{PS}(s) \bullet G_{VEA}(s)$$

The error amplifier gain is:

$$G_{VEA} = \frac{-j}{2 \bullet \pi \bullet f \bullet R_i \bullet C_f} = \frac{-j \bullet 1.17}{f}$$

$$\therefore T_V = 1 = \frac{-j \bullet 92.6}{f} \bullet \left(\frac{-j \bullet 1.17}{f}\right) = \frac{108}{f^2}$$

The cross over frequency then is approximately 11Hz, so the resistor, R_f, can be calculated to place the pole at f_c.

$$R_f = \frac{1}{2 \bullet \pi \bullet 11Hz \bullet 0.1\mu F} \approx 140k\Omega$$

Finally, the resistor R_D (10kΩ) sets the DC output voltage to 410V.

7. OVP/ENABLE

An output voltage exceeding 450V is defined as an overvoltage condition. To trip the OVP comparator at 450V requires a divider of:

$$\frac{7.5V}{450V} = 60:1$$

Letting the lower resistor in the divider = 33kΩ, the top resistor then is 2MΩ, two 1MΩ resistors are

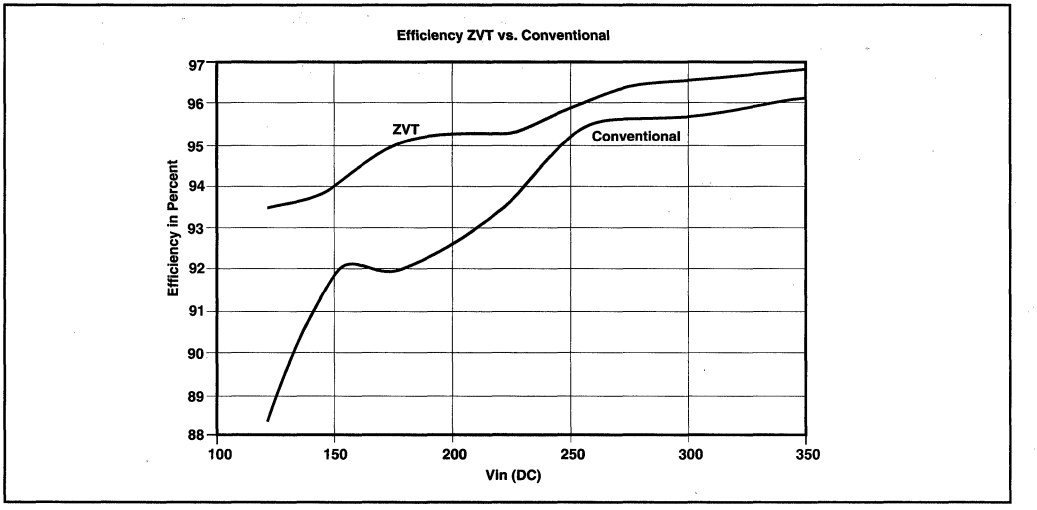


Figure 14. Efficiency Data

used in series to reduce the voltage stress. A 10nF capacitor is placed in parallel with the 33kΩ resistor for noise filtering.

With this divider the converter will start at $76V_{RMS}$, which will allow startup well below low line.

EXPERIMENTAL RESULTS

The example converter was constructed to demonstrate circuit performance. The circuit performed well and was tested over the full line and load ranges.

Figure 14 shows efficiency data for the ZVT vs. a conventional boost converter, which was derived by simply removing the ZVT components. The conventional circuit needed to be cooled with a fan in order to stabilize the power semiconductor temperatures. It can be seen from the data that the ZVT circuit has a significant advantage over the conventional converter at low line. At higher line voltages the advantage is reduced until the two power stages converge at high line. This is understandable and consistent with the other reported data [4,13]. At low line, the higher input current contributes to higher switching losses in the conventional converter. The ZVT converter however, does not experience increased switching losses (conduction losses increase for both converters at low line).

Figure 15 shows the ZVT and main switch gate drives as well as the main switch drain to source voltage. The ZVT gate drive goes high prior to the main switch and drives the drain voltage to zero before the main switch turns on. It should also be noted that the drain to source voltage waveform is very clean with no overshoot or ringing, which will reduce EMI and voltage stress on the device. The ZVT circuit waveforms are shown in Figure 16. Current in L_r is shown in the top trace. The wave-

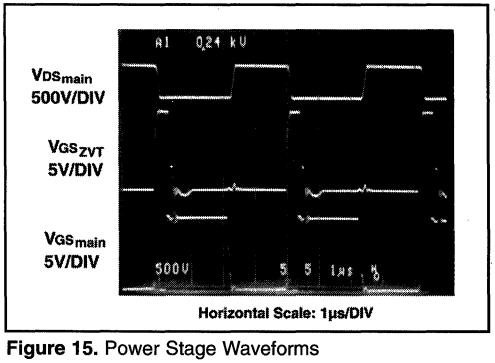


Figure 15. Power Stage Waveforms

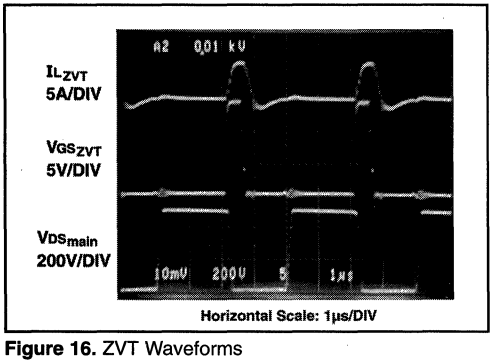


Figure 16. ZVT Waveforms

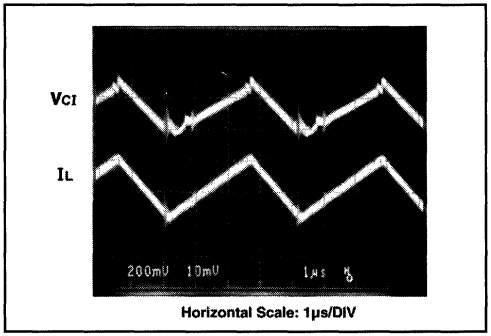


Figure 17. Current Synthesizer Waveforms

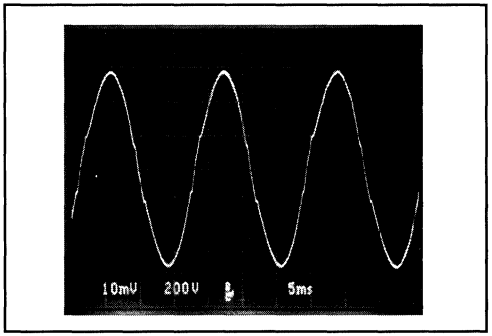


Figure 18. Line Current

forms are well damped with a peak current of approximately 6A. The current synthesizer waveforms are shown in Figure 17. The top waveform is the reconstructed waveform at CI and the bottom waveform is inductor current. The waveforms show good agreement. Any error between the reconstructed and actual waveform will be greatest at high line and is primarily caused by slight offset voltage errors in the synthesizer circuit.

Figure 18 shows the input line current at low line and maximum load, the THD and power factor are well within acceptable limits. Table 1 gives THD and pf measurements for several line and load conditions with the single stage current error amplifier clamp circuit. Table 2 shows THD and pf with the two stage clamp circuit shown in Figure 9B.

Line(VAC)	% THD	Pf
100	6.3	0.998
120	4.5	0.999
200	8.9	0.996
230	10	0.995

Table 1 THD and Pf vs. line, with single stage error amplifier clamp circuit.

Line(VAC)	% THD	Pf
100	4.95	0.999
120	5.30	0.998
200	5.45	0.998
230	5.83	0.998

Table 2 THD and Pf vs. line, with two stage error amplifier clamp circuit.

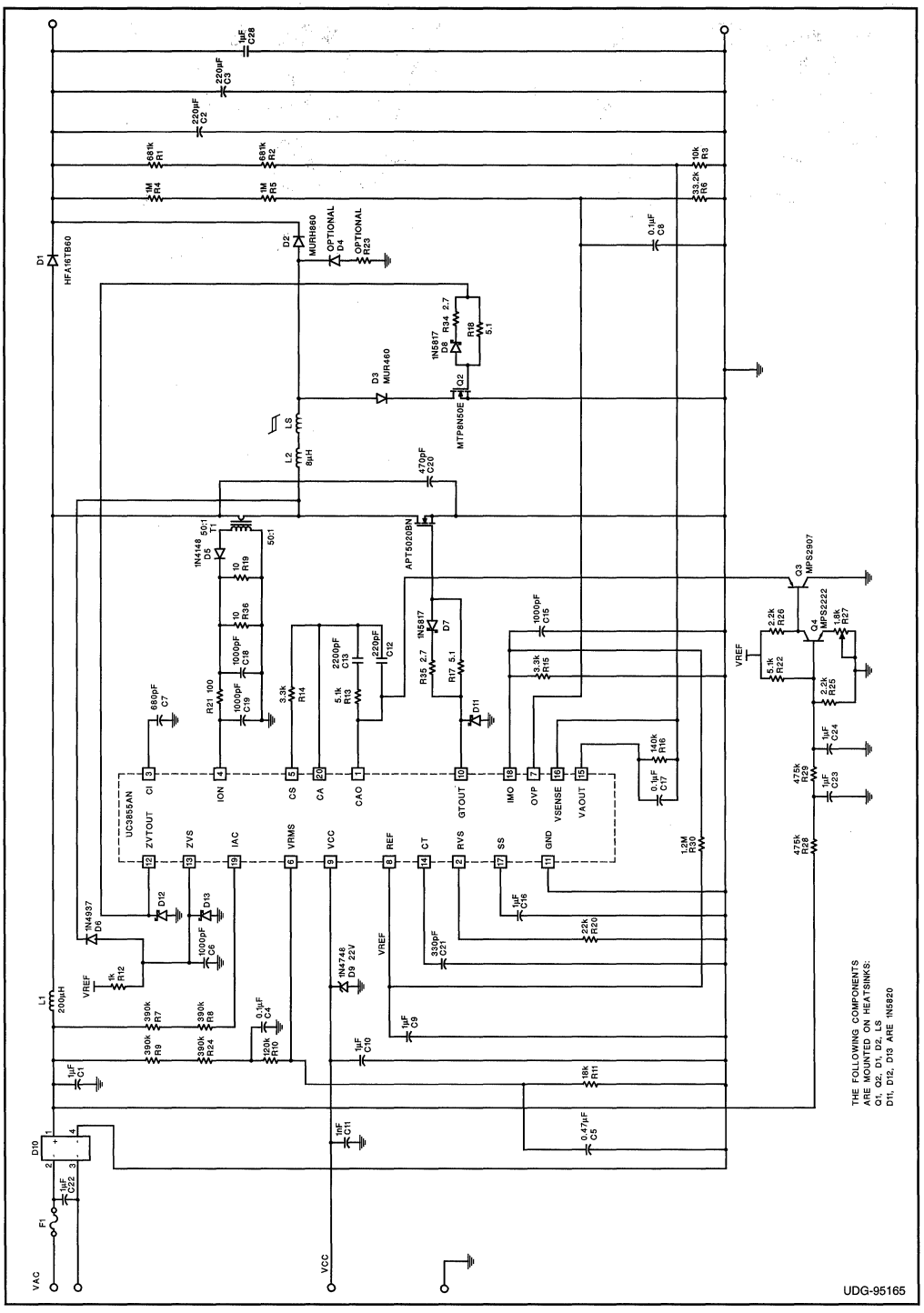


Figure 19. UC3855A/B Typical Application

POWER STAGE COMPONENT VENDORS

L1,L2	Magnetics, Butler, PA (412) 282-8282
Spike Killer	Toshiba, Westboro, MA (508) 836-3939
Q_{MAIN}	APT, Bend, OR (503) 382-8028
D1	International Rectifier, El Segundo, CA (310) 322-3331
Q_{ZVT}, D2, D3, D4	Motorola, Phoenix, AZ (602) 244-3550

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BOOST POWER FACTOR CORRECTOR DESIGN WITH THE UC3853

by Philip C. Todd

ABSTRACT

The UC3853 is designed to provide high performance power factor correction (PFC) for low to medium power applications with minimal complexity. It provides power supplies in the range of 10 to 200 watts with a low distortion, power factor corrected input current, a regulated output voltage and operation over a wide range of input voltages. The UC3853 uses average current mode control and works with either a boost or flyback converter. It was developed from the UC3854 family of PFC control circuits and has the same functionality in an 8-pin package. Much of the information available for the UC3854 family of integrated circuits is also applicable to the UC3853. In particular, Unitrode Application Note U-134 provides a good general introduction to power factor correction. U-134 contains an extended description of power factor correction, the boost PFC and the control circuits necessary to provide the correct programming of the current waveform. The reader is urged to review that note as well as this one before designing a boost power factor corrector.

This Application Note describes the features and functions of the UC3853 in detail. The design process for a boost power factor corrector is presented and the design details for a 100W output boost power factor corrector with a "universal" input voltage range of 80-270VAC are included. A table that extends the 100W boost converter example over the range of 25W to 200W is featured. A step-by-step summary of the design process is also provided so that the boost converter circuit may be customized for any application.

ABOUT THE UC3853 PFC CONTROLLER

The UC3853 has many similarities to the UC3854 based family of devices. It contains an average current mode control loop for a low distortion input current waveform, a multiplier to program an accurate current waveform and a voltage error amplifier to regulate the output voltage. The UC3853 also contains over-voltage protection for the output and has a fixed frequency internal oscillator which is synchronizable.

A block diagram of the UC3853 is shown in Figure 1. Due to its 8-pin simplicity, some pins serve more than one function and some functions are brought inside the chip altogether. The UC3853 begins operation when the voltage at the VCC pin is greater than 11.5V. An undervoltage lockout function (UVLO) keeps the device from operating before this voltage is reached. The UC3853 enters the UVLO state again when VCC drops below 9.5V. The hysteresis in the UVLO allows the device to be started from a capacitor which is trickle charged directly from the input voltage. When in UVLO, most of the internal circuits are not powered so the supply current is less than 500μA (250μA typical). The reference voltage in the UC3853 is internal to the device and is not brought out to a pin. The reference is divided down to 3.0V at the non-inverting input to the voltage error amplifier. The reference is trimmed to an accuracy of better than 2% at the FB pin of the voltage error amplifier so the reference voltage specification includes the offset of the amplifier. The total variation of the reference over temperature, including the set point accuracy, is 3.0V ±3.5%. For a typical 400V output the accuracy translates into an output variation of ±8V at room temperature, which is comparable to the ripple voltage amplitude on the output at full power.

The output of the UC3853 supplies 500mA peak current to the gate of the power MOSFET switch. A simplified schematic of the output driver is shown in Figure 2. The VCC pin provides the voltage feedforward signal needed by the multiplier/divider/squarer circuit and thus it has a wide input voltage range under normal operation. The output voltage

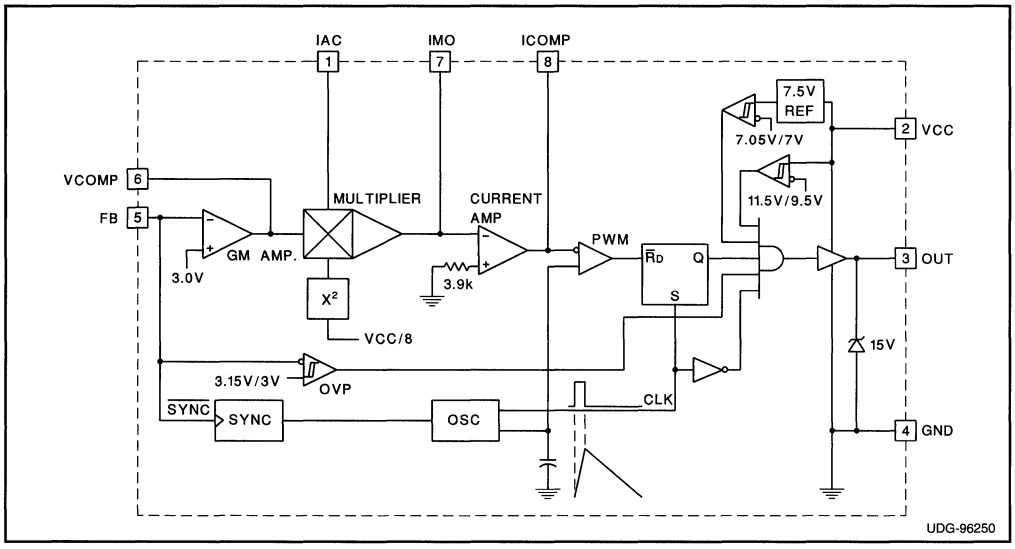

Figure 1. Block Diagram of UC3853

is therefore clamped near 15V to prevent the gate of the MOSFET switch from being driven beyond its breakdown voltage as VCC changes. When power is not applied to the device the output driver is self-biased to hold the output to within 1.5V of ground. When VCC is above the UVLO threshold the bias circuit is disabled and the output driver operates normally. This prevents the MOSFET from turning on when power is first applied to the converter. If the output were not held low, the gate to drain capacitance of the MOSFET would pull the gate high when power is applied and turn the device on, which often results in its destruction.

The PWM comparator uses the oscillator ramp and the output of the current amplifier to generate the gate drive output as shown in Figure 3. The output of the comparator is latched for the duration of the clock period to prevent false output pulses. The latch is set by the clock signal at the beginning of each clock period to drive the output high and is reset by the PWM comparator to drive the output low. The output is kept low by the status inputs to the AND gate that drives the output. The status inputs are the undervoltage lockout (UVLO), the reference valid and the output overvoltage status signal. The output is also held low during the clock interval.

The oscillator is internal to the UC3853, has a fixed 75kHz operating frequency and may be synchronized to an external source. The oscillator waveform is a reverse sawtooth because a negative slope ramp is required to provide the proper polarity for the PWM circuit and for the slope compensation of the average current loop. The current loop error amplifier inverts the current signal so the oscillator ramp must have a negative slope. The

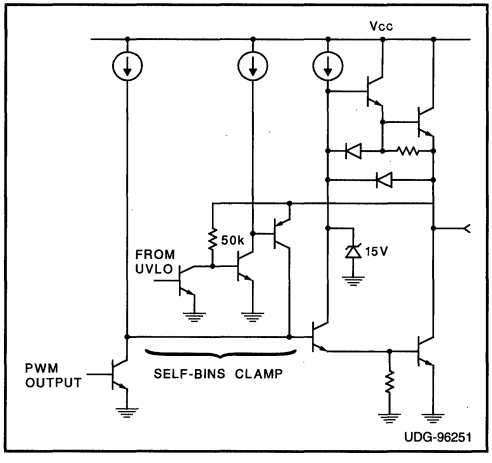

Figure 2. UC3853 Output Driver (Simplified Schematic)

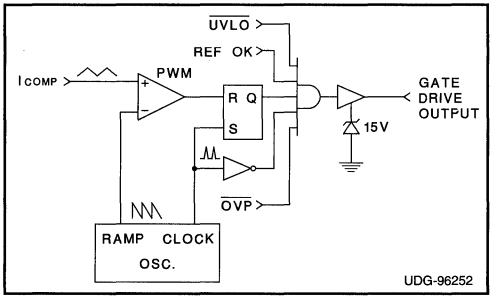

Figure 3. UC3853 PMW Circuit

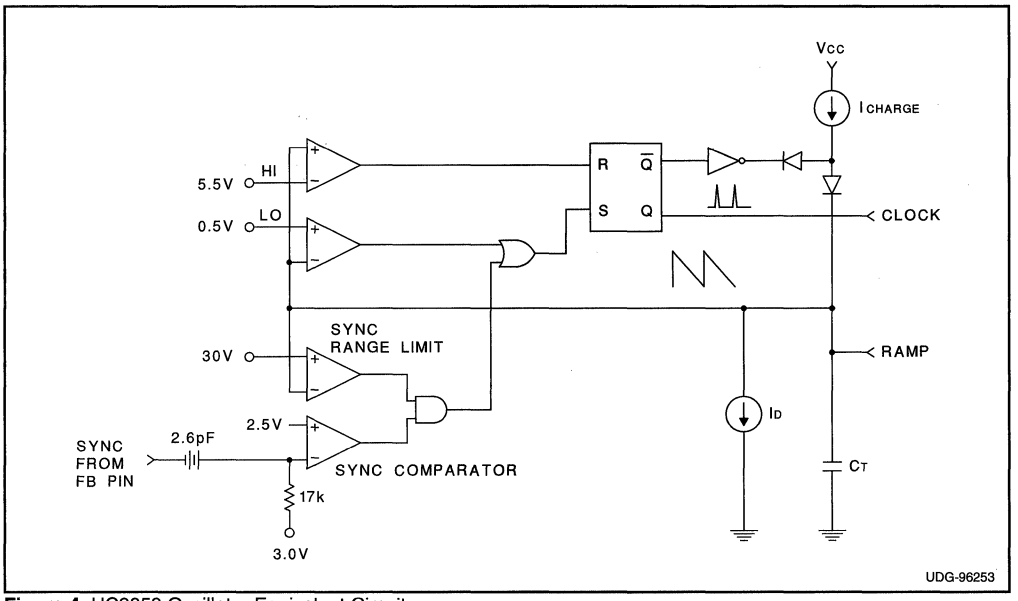

Figure 4. UC3853 Oscillator Equivalent Circuit

relative polarity of the two signals is therefore opposite, which is the correct orientation. This is all internal to the device. The width of the clock output pulse determines the minimum dead time of the output and is less than 1% of the clock period. An equivalent circuit for the oscillator and the sync circuit is shown in Figure 4.

The synchronizing pulse for the oscillator comes from the FB pin. The voltage feedback and the overvoltage protection are also connected to the FB pin. If the synchronizing signal is capacitively coupled into the FB pin it will not upset the DC output voltage value since the bandwidth of the amplifier is very small compared to the switching frequency. The compensation network on the output of the transconductance amplifier will eliminate the synchronizing signal from the output of the amplifier. The guaranteed synchronization frequency range is 95kHz to 115kHz. Circuits for synchronizing the oscillator are described later in this Application Note.

The voltage and current loop amplifiers, the squarer and the multiplier/divider circuits are shown in Figure 5. The current amplifier is a wideband operational amplifier and it has ground referenced inputs. The inverting input of the amplifier is a summing junction where the feedback, the input current signal and the current programming signal from the multiplier output come together. The current signal is negative and the output of the multiplier is positive so the current loop is adjusted to keep the voltage at the inverting input zero since the non-inverting input of the current amplifier is connected to ground through a 3.9kΩ resistor. This resistor provides DC balancing of the amplifier input bias currents. The amplifier has sufficient output drive capability to handle a wide range of feedback networks.

The squarer and multiplier/divider are the heart of the control circuit and are shown in Figure 5. This circuitry makes it possible to operate a boost PFC stage over a 3:1 input voltage range and still get excellent voltage loop bandwidth and fast response to input voltage variations. The multiplier/divider requires three inputs which are traditionally labeled A, B and C. The A input is the output of the voltage error amplifier which controls the average output voltage. The B input is the IAC signal which is a current from the input voltage and it is multiplied by the output of the voltage error amplifier to provide the current shape and amplitude needed to program the current loop. The C input is the divider input and it is the feed forward voltage that comes through the squarer. This input is proportional to the square of the average input voltage and it adjusts the gain of the multiplier to keep the gain of the voltage control loop constant. This is the secret to achieving a wide bandwidth control loop over a wide input voltage range. The squaring circuit takes its input from the VCC pin so the bias voltage for the UC3853 must be proportional to the input voltage for this feature to work properly.

The voltage error amplifier in the UC3853 is a transconductance amplifier and it has both a high input impedance and a high output impedance,

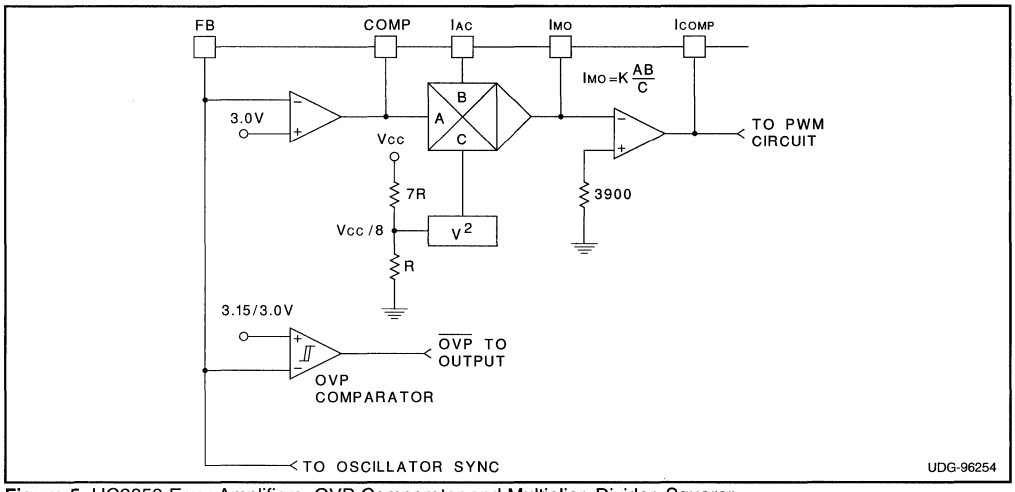

Figure 5. UC3853 Error Amplifiers, OVP Comparator and Multiplier, Divider, Squarer

which is a controlled current source output rather than the usual low impedance voltage source output. The gain of a transconductance amplifier is not given by the ratio of volts out to volts in. Instead it is given by the ratio of amperes out to volts in, which is a transconductance (the inverse of a resistance) and has the units of Siemens. The transconductance is a gain in this case and is often denoted by the symbol G_M. The gain of a transconductance amplifier can be changed into a voltage ratio by multiplying the transconductance gain by the load resistance. Hence, the voltage gain is set by an RC network to ground from the output of the amplifier. This allows the gain and frequency response of the amplifier to be determined by the load impedance without any components connected from the output of the amplifier to the input.

A transconductance amplifier was chosen to allow three functions to be combined on the FB pin. The oscillator sync input and the overvoltage comparator share the same input pin as the error amplifier so if a feedback network were connected around the amplifier the overvoltage comparator would be inaccurate. Since both the transconductance amplifier and the overvoltage comparator require only a simple voltage divider at their inputs for proper operation they can be combined into a single pin. The non-inverting input of the voltage amplifier is connected to a 3.0V DC reference which is the reference for the output voltage. The overvoltage comparator turns the output of the UC3853 off when the voltage at the FB pin exceeds 3.15V. The output turns back on when the voltage at the FB pin comes back to 3.0V.

BOOST PFC POWER STAGE DESIGN WITH THE UC3853

The circuit for a boost PFC is shown in Figure 6. The reference designators for the parts on the schematic match those in U-134 where the functions of the parts are the same. In all cases the reference designators are appropriate for the function of the device. A 100W boost power factor corrector is used as an example of the design process and this is the circuit that is shown in Figure 6. A table is provided at the end of this Application Note that extends the design over the range of 25W to 200W. The control circuits are the same whether at 25W or at 200W. The values of the control circuit components change only if the choices for circuit performance are different from those made here. The following design process allows the design to be modified to suit a wide variety of applications.

The design of a boost PFC begins with the specification for the system performance. The minimum and maximum input line voltages, the maximum output power, and the line frequency range must be specified. For the example circuit the specifications are:

- Maximum power output: 100 Watts
- Input line voltage range: 80-270VAC
- Line frequency range: 47-65Hz

The input line voltage and frequency range are a "universal" input range and allow this power factor corrector to operate from power lines anywhere in the world without switches or other adjustments.

The output voltage needs to be at least 5% higher than the peak voltage of the highest input line voltage. The peak of a 270VAC line will be about 380V

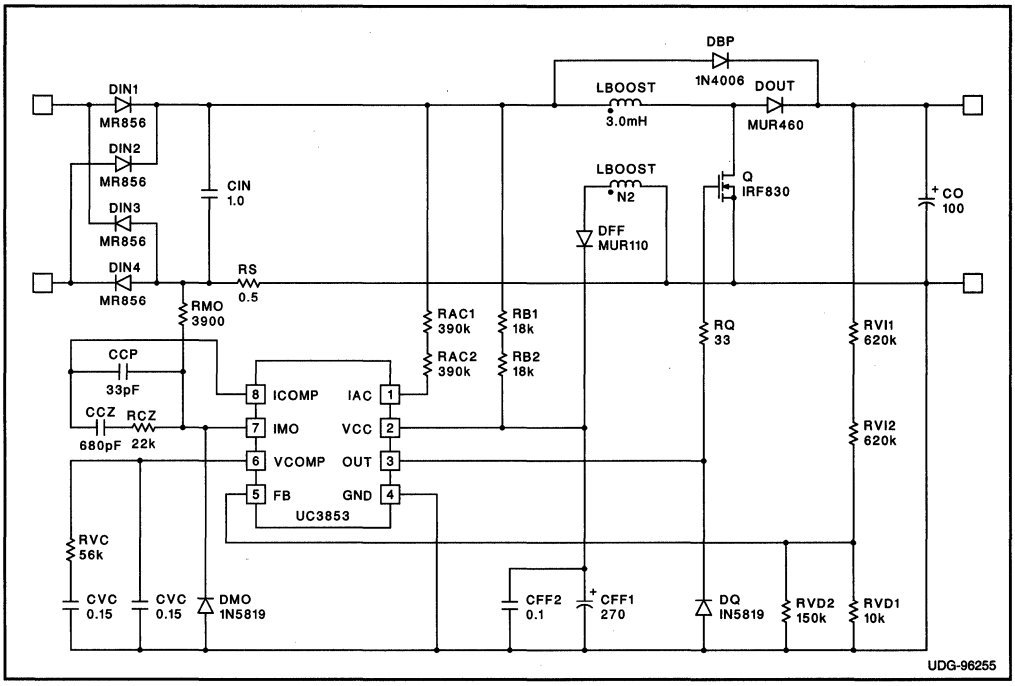

Figure 6. Schematic of a Boost Power Factor Corrector Using the UC3853

so 400V is chosen as the DC output voltage.

The switching frequency is an important consideration in the design process and the switching frequency is internally fixed in the UC3853 at 75kHz nominal and may be synchronized to an external 100kHz oscillator.

INDUCTOR SELECTION

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the peak high frequency ripple current. The peak line current is given by the following equation:

$$I_{LINEpk} = \frac{\sqrt{2} \bullet P}{V_{INmin}}$$

Where P is the maximum input power to the converter. Generally, using the output power is sufficiently accurate for this calculation since the efficiency of the converter should be greater than 90%. If greater accuracy in the design process is required, the design may be completed, the efficiency calculated and then the design process may be iterated using the calculated value for efficiency. For the example converter, the output power is 100W and V_{INmin} is 80VAC so I_{LINEpk} is 1.77A.

The high frequency ripple current, ΔI, must be kept reasonably small and is usually in the range of 15% to 25% of the peak line current given above. If the ripple current is too high the AC input filters required to filter out this noise become larger. If the ripple current is too low the value of the inductance is too large and the cusp distortion on the leading edge of the waveform will be large and the power factor will be low. For the example converter, the ripple current, ΔI, is chosen to be 20% of the peak line current or about 0.35A peak-to-peak. The peak current in the inductor, I_{Lpk}, is the sum of the peak line current and half of the peak-to-peak ripple current or 1.95A for the example converter.

The value of the inductor is determined by the peak current at low input line voltage, the duty factor, D, at that input voltage and the switching frequency. This value of the duty factor is given by the following equation:

$$D = \frac{V_O - \sqrt{2} \bullet V_{INmin}}{V_O}$$

Where V_{INmin} is the minimum RMS input line voltage and V_O is the DC output voltage. For the example converter V_{INmin} is 80V and V_O is 400V so D is 0.72.

The value of the inductor is given by the following equation:

$$L = \frac{\sqrt{2} \bullet V_{INmin} \bullet D}{\Delta I \bullet f_S}$$

Where V_{INmin} is the minimum RMS input voltage and D is given from the equation above. The switching frequency is fs and ΔI is the maximum peak-to-peak ripple current. For the example converter V_{IN} is 80V, D is 0.72, fs is 75kHz and ΔI is 0.35A peak-to-peak as determined above. This gives an inductance of 3.1mH. A value of 3.0mH nominal will be used.

Note that the ripple current changes with input voltage so it varies as the line voltage goes through its cycle. Under normal operation the ripple current can be significantly greater than the 20% specified here. The maximum ripple current occurs when the momentary value of the input voltage equals half the DC output voltage which corresponds to 50% duty ratio.

OUTPUT CAPACITOR SELECTION

C_O, the output capacitor generally falls in the range of 1 to 2μF per watt for typical 400V output applications. Since low cost is one of the targets of this converter, 1μF/W is chosen and thus a 100μF capacitor will be used for C_O. There are many factors that influence the value of the output capacitor. The output voltage hold-up time, the output ripple voltage, the loop transient response and the input current third harmonic distortion are all dependent to some degree on the value of the output capacitor and, in all cases except cost, a larger value of the output capacitance results in better performance. Nevertheless, a reasonable compromise can be reached with the 1μF/W value.

All power factor correction circuits have a large ripple current on their output at the second harmonic of the line current as highlighted in U-134. As the output capacitor becomes smaller, the output ripple voltage due to the second harmonic ripple current increases and the bandwidth of the voltage loop must be made smaller to keep the same level of distortion in the input current. A 1% second harmonic ripple voltage at the output of the voltage error amplifier becomes 0.5% third harmonic distortion of the input current. The only ways to reduce this source of distortion are to (1) increase the size of the output capacitor and (2) reduce the gain of the error amplifier at the second harmonic frequency by reducing the amplifier bandwidth. Reducing the loop bandwidth slows the transient response and increases its deviation.

The output capacitor may need to be larger for other reasons. If hold-up time is required, the capacitor may need to be larger than 1μF/W. The following equation may be used to calculate the size of the capacitor for a given hold-up time, power output and voltage change.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Where P is the rated power of the converter, Δt is the required hold-up time, V_O is the DC output voltage of the converter and V_{Omin} is the voltage to which the output decays at the end of the hold-up time. For the example converter, 100μF gives about 19 milliseconds of hold-up time for a 50V change in V_O or 35 milliseconds of hold-up for a 100V change.

CURRENT SENSE RESISTOR

R_S, the current sense resistor, is selected to provide 1.0V at the maximum current expected in the inductor. I_{LINEpk} plus half the peak-to-peak ripple current is the peak current through the inductor and was calculated above. The value of the current sense resistor is found from: $1.0V/I_{Lpk}$. For the example converter the peak current in the inductor is 2.0A maximum so the value of the sense resistor is 0.5Ω.

SWITCHES AND DIODES

The power switch must have a low R_{DSon} rating and a peak voltage rating greater than the output voltage of the converter with some margin for transient overshoot, ripple voltage on the output and appropriate levels of derating. A low R_{DSon} of the power switch will result in lower conduction losses but these devices also have high gate capacitances and may therefore have longer turn-on times, resulting in greater overall switch power dissipation. There is an optimum size switch for each application although the optima is rather broad. Suggestions for switches for a variety of power levels are contained in the table at the end of this application note. These are by no means the only possibilities and are simply generic choices. For the example converter an IRF830 was chosen.

The output diode must be rated for the peak output current and must be an incredibly fast diode. A reverse recovery time below 100 nanoseconds is strongly recommended and faster is much better. The reverse recovery time of the diode has a direct effect on the power dissipation in the switch. The switch must conduct full output current at full output voltage from the time it turns on until the diode turns off. For the example converter this will be 400V at 2.0A for a peak power of 800W. If this lasts for 100nsec the average power will be 6.0W at a 75kHz switching frequency. If a 35nsec recovery

diode is used the average power will be 2.1W. There are many diodes available that meet the requirements of this application. The temperature rise of the diode must be kept below maximum for the worst case conditions as well. The reverse recovery time of the diode becomes larger as the temperature increases and this increases the power dissipation of the switching transistor. Heat sinking of the diode may be required to control the maximum temperature. For the example converter either an MUR460 or a BYM26C is used.

INPUT DIODES

The input diodes are not particularly critical. They must have a current rating sufficient for the maximum current at low line and they must be held to a reasonable temperature rise. Fast recovery types generally prove to be a bit less noisy than standard recovery types. Avalanche breakdown types work better with noisy power lines. The exact choice of input diodes depends on many such factors as well as the amount of filtering present on the AC side of the bridge. For the example converter, MR856 or BYW95C diodes are used. Both are fast recovery types.

C_{IN} is part of the input filter even though it is after the input diodes. The value must be chosen in conjunction with the input filter and must be kept reasonably small. This capacitor carries most of the ripple current from the inductor so it needs to be a film type capacitor with a substantial high frequency ripple current capability. At light loads C_{IN} can have a large effect on the distortion of the input current because it is after the input diodes. At these low currents, especially near the input voltage zero crossing, the capacitor stores enough energy to maintain the output current and the input diodes turn off, thus introducing distortion into the input current. For the example converter, a 1.0µF capacitor was chosen to give less than 1V peak-to-peak ripple voltage at the switching frequency with 100W output.

CONTROL CIRCUIT DESIGN WITH THE UC3853

The heart of the UC3853 is the multiplier and it is quite easy to set the parameters for proper operation. The equation for the multiplier is given below and, even though it looks complex, it is quite straight forward.

$$I_{MO} = \frac{I_{AC} \bullet (V_{COMP} - 1.5)}{K_M \bullet \left(\frac{V_{CC}}{8}\right)^2}$$

I_{MO} is the output current from the multiplier. I_{AC} is the programming current that comes from the input through R_{AC} and is proportional to the input voltage. It tells the current loop what to do to maintain an input current which is proportional to the input voltage. V_{COMP} is the output of the voltage error amplifier and is the other input to the multiplier. K_M is the gain constant of the multiplier and is given in the data sheet for the UC3853. V_{CC} is the supply voltage to the UC3853 and it is divided by eight internally and then squared in the squaring circuit. This forms the divider input to the multiplier and is used to keep the gain of the voltage loop constant so that the loop bandwidth may be kept large and thus have a relatively fast transient response.

I_{AC} must be programmed to have a maximum value of 500µA when the AC line voltage is at its peak. The voltage at the IAC pin is 2.0V so it introduces very little error into the current if this voltage is ignored. For the example converter the maximum input voltage is 270VAC and this has a peak value of about 380V. A 760kΩ resistor will give 500µA. Most resistors are only rated to 250V so two resistors will be needed in series. The closest standard value is 390kΩ so this value is chosen for both R_{AC1} and R_{AC2}.

CURRENT LOOP COMPENSATION

The peak value of I_{MO} is about 250µA with the values of R_{AC} given above. If R_{MO} is made 3.9kΩ, the peak value of voltage across R_S will be 1.0V. This value of R_{MO} also matches the 3.9kΩ resistor internal to the UC3853 which is connected to ground from the non-inverting input of the current error amplifier. These two values provide the correct balance for the DC bias currents into the amplifier and give the correct input offset voltage. If the offset voltage is in the wrong direction the current loop could latch at zero output.

The PFC input current must track the current programming signal (I_{MO}) from the multiplier very closely to achieve a low distortion input current. Accurate tracking requires high gain in the current loop to minimize the errors. For the current loop to be stable, the frequency at which the gain of the loop is equal to one must be less than one thirds of the switching frequency and the gain must roll off with a single pole slope. The boost power stage has a single pole due to the main inductor and the current sense resistor. This L/R pole creates a stable loop with a fixed gain, wide bandwidth error amplifier. These two requirements can be accommodated by using pole zero compensation around the error amplifier. Pole zero compensation has

high gain at low frequencies and flat gain at high frequencies so that the input current tracks the programming signal accurately and is also stable at high frequencies. This is the essence of average current mode control and it is necessary for a low distortion PFC.

A block diagram of the current loop is shown in Figure 7. A bit of topological manipulation has been done to put the loop into this form. The switch, output diode and output capacitor have been moved to the other side of the inductor and lumped into the voltage source V_S, which is now a controlled source and is controlled by the duty factor d from the PWM circuit in the UC3853. The reason for showing the circuit model in this form is to highlight the source of the L/R pole in the current loop and to show how the pole zero compensation of the current error amplifier affects the loop.

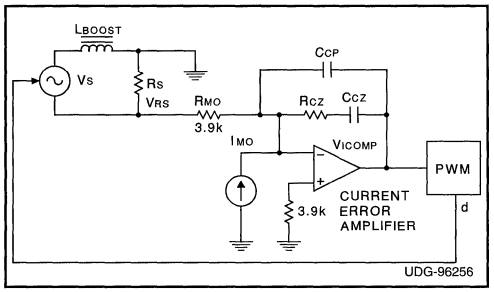

Figure 7. Simplified Block Diagram of a Boost PFC Current Loop

Figure 8 shows the control to output current gain of the current loop and the current amplifier compensation as well as the complete current loop gain. The graph ignores the double pole occurring at the switching frequency and the aliasing effects of the sampling system. The graph is based on a linear model to promote understanding of the loop dynamics and the compensation methods employed. The lower curve is the control to current transfer function of the boost stage and the pulse width modulator (V_{RS}/V_{Icomp}). The gain is moderate at low frequencies and shows the L/R corner frequency and single pole roll off up to half of the switching frequency. The pole zero compensation of the current error amplifier is shown along with the complete current loop response.

The design of the pole-zero compensation for the current loop begins with the equation for the control to output transfer function of the boost power stage. The control variables for this transfer function are the output of the current amplifier, V_{Icomp}, and the voltage across the current sense resistor, V_{RS}. The equation is:

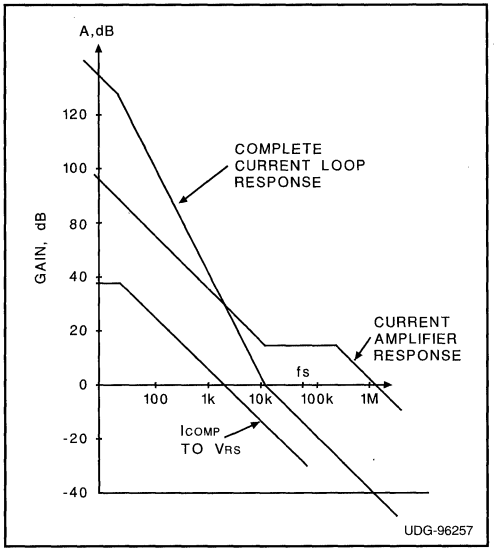

Figure 8. Current Loop Transfer Functions for 100W Example Boost Converter

$$\frac{V_{RS}}{V_{Icomp}} = \frac{V_O \bullet R_S}{V_{OSC} \bullet (R_S + X_L)}$$

Where V_O is the DC output voltage of the converter, R_S is the sense resistor value, V_{OSC} is the peak-to-peak amplitude of the oscillator ramp voltage and X_L is the impedance of the boost inductor ($2 \bullet \pi \bullet f \bullet L$).

The current loop is a very wide bandwidth loop and stability is achieved by adjusting the current amplifier gain so that the natural roll off from the L/R_S pole of the boost stage crosses 0dB gain at the appropriate frequency. Because the bandwidth is large, slope compensation must be added to the loop to compensate for the double pole which occurs at the switching frequency. In average current mode control the slope compensation is provided by the oscillator ramp, which is one of the inputs to the PWM comparator. If the gain of the error amplifier is correct, the amplitude of the oscillator ramp will introduce the correct amount of slope compensation. The procedure is to match the down slope of the inductor current with the slope of the oscillator ramp. That gives the correct value for the loop gain at the switching frequency to maintain stability. A capacitor is then added in series with the resistor for pole-zero compensation which gives the maximum amplifier gain at low frequencies.

The maximum down slope of the inductor current occurs when the input voltage is near zero. The equation for the inductor yields the slope of the current.

$$\frac{dI}{dt} = \frac{V_O}{L}$$

Where dI/dt is the slope of the inductor current in amperes per second, V_O is the DC output voltage of the converter and L is the value of the boost inductance. This current flows through the sense resistor and becomes a voltage so the equation is modified as follows:

$$\frac{dV}{dt} = \frac{V_O}{L} \bullet R_S$$

Where R_S is the sense resistor value. For the example converter the output voltage is 400VDC and the inductance is 3.0mH so the dI/dt is 0.133A/µsec, and R_S is 0.5Ω so dV/dt is 0.066V/µsec.

The oscillator in the UC3853 has a peak-to-peak amplitude of 5.0V and the period is 13.3µsec so the slope is 0.375V/µsec (the slope does not change with synchronization). The gain of the current amplifier at the switching frequency is determined by the ratio of the oscillator voltage slope divided by the current slope. The gain of the current amplifier at the switching frequency is the ratio of R_{CZ} to R_{MO}. For the example converter the current slope is 0.066V/µsec and the oscillator slope is 0.375V/µsec so the gain is 5.625. R_{MO} is 3.9kΩ so R_{CZ} is 22kΩ.

The value of the capacitor C_{CZ}, which introduces a zero into the current error amplifier response, is set by the current loop crossover frequency. The zero must be at or below that frequency to maintain the phase margin of the current loop. The equation for f_{CI} given below is simplified somewhat but is accurate over this frequency range.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{2 \bullet \pi \bullet L \bullet R_{MO} \bullet V_{OSC}}$$

Where V_O is the DC output voltage of the converter, R_S is the value of the current sense resistor and R_{CZ} is the current amplifier feedback resistance determined above. V_{OSC} is the peak-to-peak oscillator ramp voltage, L is the value of the boost inductor and R_{MO} is the current amplifier input resistance. For the example converter, V_O is 400VDC, R_S is 0.5Ω, R_{CZ} is 22kΩ, V_{OSC} is 5V, L is 3.0mH and R_{MO} is 3.9kΩ resulting in an f_{CI} of 12kHz.

C_{CZ} must have an impedance equal to or less than R_{CZ} at f_{CI}. This is easily found from:

$$C_{CZ} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

For the example converter, f_{CI} is 12kHz and R_{CZ} is 22kΩ so C_{CZ} must be greater than 600pF. A 680pF capacitor is chosen to give a bit of extra phase margin.

C_{CP} is included to suppress high frequency noise in the current amplifier and it must have an impedance of at least 2 • R_{CZ} at the switching frequency. Substituting f_S for f_{CI} into the equation above gives C_{CP}.

$$C_{CP} = \frac{1}{2 \bullet \pi \bullet f_S \bullet 2 \bullet R_{CZ}}$$

For the example converter C_{CP} must be less than 50pF. A value of 33pF is chosen to accommodate a 100kHz synchronization frequency.

A hard current limit is not necessary to protect the switch in an average current mode controlled system. The gain of the current amplifier is set so that the maximum change of current in the inductor results in at most a 20% change of the current during one clock period. This makes it impossible for the control circuit to cause the switch to be on long enough to enter an overcurrent condition. The current programming signal is also limited so the inductor current can not exceed this value.

HARMONIC DISTORTION BUDGET

Once the current loop is stable the next two tasks are setting the voltage loop compensation and the feedforward compensation. Both of these are determined by the amount of harmonic distortion each contributes to the input current. The voltage loop contributes 0.5% third harmonic distortion to the input current for each 1% ripple voltage at the output of the error amplifier. The feedforward compensation comes from the voltage supplied to the UC3853 and each 1% ripple on this input contributes 1% third harmonic distortion to the input current.

The choice of input current harmonic distortion limit and the allocation of this distortion to the two major sources is somewhat arbitrary. For the example converter, the THD will be limited to 5% of the input current. The voltage loop is allowed to contribute 2% of the distortion and the feedforward voltage is allowed to contribute 2% of the distortion. The remaining 1% will be allocated to other sources such as cusp distortion and possible multiplier nonlinearity. 5% THD gives a power factor of 0.99875.

VOLTAGE LOOP COMPENSATION

A simplified block diagram of the voltage loop is shown in Figure 9. Average current mode control turns the power stage of the boost converter into a voltage controlled current source driving a capaci-

tor, C_O, in parallel with the load resistance. The current loop therefore becomes a transconductance amplifier with a voltage input and current output. The voltage gain of the current loop is given by $G_{CL} \bullet Z_L$ where G_{CL} is the transconductance of the current loop and Z_L is the parallel combination of C_O and R_L, the load resistance. The frequency response of the current loop has a DC gain given by $G_{CL} \bullet R_L$ and a single pole roll off due to C_O and R_L within the frequency range of interest. Theoretically, if the voltage loop is closed around the current loop with a fixed gain error amplifier, the voltage loop will be stable because there is only a single pole from C_O and R_L within the loop. As the gain of the amplifier increases, the bandwidth of the voltage loop also increases. Although this solution is very appealing, it is not feasible with the UC3853 because the limited current capability of the voltage error amplifier. Therefore, the error amplifier compensation will have a zero below and

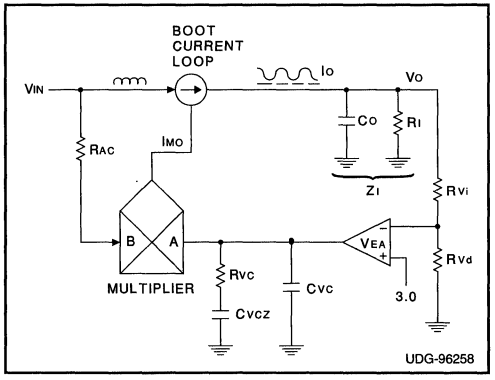

Figure 9. Simplified Block Diagram of a Boost PFC Voltage Loop

a pole at the crossover frequency of the voltage loop.

The multiplier in the voltage loop adds the current programming signal from the line frequency and it acts like a switching frequency. Therefore the bandwidth of the voltage loop must be kept below $(2 \bullet f_L/\pi)$ to maintain voltage loop stability where f_L is the line frequency. The gain of the error amplifier needs to be high to maintain wide bandwidth in the voltage loop and thus fast transient response but if it is too high the loop will go unstable due to the line frequency introduced by the programming signal in the multiplier. If the gain of the amplifier in the loop is set with a fixed gain to give maximum bandwidth, the DC gain of the loop is reasonable and the output voltage regulation is within a percent or two of the set point.

The relatively wide bandwidth of the loop gives good transient response but also gives little attenuation of the second harmonic ripple voltage on the output capacitor. This voltage modulates the input current so the harmonic distortion of the input current will be too high. Reducing the harmonic distortion requires reducing the gain of the loop at the second harmonic of the power line frequency, which is the ripple voltage frequency on the output capacitor. The bandwidth of the loop must also be kept as high as possible to maintain good transient response. If the loop is closed with an error amplifier having an extra pole just after the unity gain crossover frequency, it is possible to reduce the harmonic distortion and still maintain good loop bandwidth and adequate phase margin.

Figure 10 is a Bode diagram of the resulting loop response. The loop response has a pole at low frequency due to the load resistance and the output capacitance and then rolls off smoothly with a first order slope due to the output capacitor. Just after the gain of the loop crosses 0dB at f_{VI}, a second pole takes the slope to a second order roll off and this reduces the loop gain to the required level at the second harmonic of the line frequency. For greater DC regulation of the output voltage and because of the requirements of the voltage error

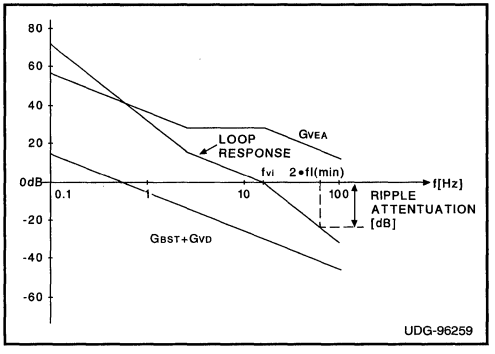

Figure 10. Transfer Functions of Voltage Loop

amplifier on the UC3853, a zero is added to the loop at low frequencies to compensate for the load resistance and output capacitance pole.

The design of the voltage loop compensation begins at the output capacitor. The voltage loop compensation reduces the amplitude of the ripple voltage from the output capacitor to a level, at the output of the voltage error amplifier, which is consistent with the harmonic distortion specification. The amount of ripple voltage on the output capacitor, C_O, is given by the following equation.

$$\Delta V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

Where P is the maximum input power of the con-

verter. Use of the input power in place of the output power is a reasonable compromise since the efficiency of the converter is high. The lowest power line frequency is f_{Lmin}, the output capacitor value is C_O and V_O is the DC output voltage. For the example converter, P (approximately P_{OUT}) is 100W, f_{Lmin} is 47Hz, C_O is 100µF and V_O is 400VDC. ΔV_{Opk} is therefore 4.2Vpk. Note that this is half the peak-to-peak value. Mathematically, this is the amplitude of the ripple voltage vector. At low line frequencies the ripple voltage is larger as is the gain of the error amplifier because of the loop compensation requirements. If performance is to be maintained over the range of line frequencies, then the lowest frequency must be used for the design.

The gain of the voltage error amplifier and the voltage divider preceding it are determined by the harmonic distortion budget for the voltage loop and the amount of ripple voltage on the output capacitor. The amount of ripple voltage allowed on the output of the voltage error amplifier is equal to twice the percentage of the distortion. Each 1% of second harmonic ripple voltage on the output of the amplifier results in 0.5% third harmonic current on the input. The %ripple on the output of the voltage error must be translated into an absolute voltage to find the gain of the voltage error amplifier and the voltage divider at the second harmonic of the line frequency. The %ripple is multiplied by the range of the output voltage (ΔV_{COMP}) to get the amplitude of the ripple voltage on the output of the amplifier. This is divided by the amplitude of the ripple voltage on the output capacitor to give the combined gain of the voltage error amplifier and the voltage divider. The equation for the gain is:

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{\Delta V_{Opk}}$$

Where G_V is the gain of the voltage divider and the voltage error amplifier, ΔV_{COMP} is the range of the voltage error amplifier output, %ripple is the percentage of ripple voltage allowed in the output of the voltage error amplifier and ΔV_{Opk} is given previously. For the example converter, ΔV_{COMP} is actually the active range of the input to the multiplier rather than the output range of the amplifier. On the UC3853 the active input range of the multiplier is between 1.5V and 6.0V so ΔV_{COMP} is 4.5V. The percent THD of the input current allowed from the voltage loop according to the harmonic distortion budget is 2% which results in 4% ripple voltage at the output of the voltage error amplifier. The numeric value of 0.04 must be used in the equation. The value of ΔV_{Opk} is 4.2V. Therefore:

$$G_V = \frac{4.5 \bullet 0.04}{4.2} = 0.043$$

The voltage divider is composed of R_{VI} and R_{VD} and is determined by the ratio of the DC output voltage to the internal reference voltage in the UC3853, which is 3.0V. The impedance of the voltage divider is somewhat arbitrary. For the example converter the output voltage is over 250V so two resistors are used in series to get the necessary voltage rating. 1.24MΩ is chosen as the divider impedance so two 620kΩ resistors are used for R_{VI}. R_{VD} is determined from the voltage divider equation and the value is just below 10kΩ so a 10kΩ resistor is used with a 150kΩ resistor in parallel. The gain of the voltage divider is given by the following equation:

$$G_{VD} = \frac{R_{VD}}{R_{VD} + R_{VI}}$$

The gain of the voltage divider, G_{VD}, is 0.0075 in the example. The gain of the divider and the voltage amplifier together must be 0.043. The gain of the amplifier at twice the line frequency (low line frequency is 47Hz) must be 5.7 for the example converter.

The gain of a transconductance amplifier is given by $A = G_M \bullet Z_A$. Where A is the voltage gain of the amplifier, G_M is the transconductance of the amplifier and Z_A is the load impedance from the V_{COMP} pin to ground. The transconductance of the amplifier in the UC3853 is 485µmhos. The gain needed for this application is 5.7, so the load impedance is 11.75kΩ. At the second harmonic of the line frequency, the gain of the amplifier is determined by C_{VC}, the voltage compensation capacitor. For the example converter, a capacitor with an impedance of 11.75kΩ at 94Hz has a value of 0.15µF and this is the value used.

The value of R_{VC} is found by extrapolating from the second harmonic frequency back to find the frequency at which the gain of the voltage loop is unity, f_{VI}. R_{VC} is then found by writing the equation for the gain of the loop, setting it to unity and solving the resulting equation for R_{VC}. The loop equation is the product of the gain of the current loop and load impedance, G_{BST}, the gain of the voltage amplifier, G_{VEA}, and the voltage divider, G_{VD}.

The gain of the boost stage is given by the following equation:

$$G_{BST} = \frac{P \bullet X_{CO}}{\Delta V_{COMP} \bullet V_O}$$

Where P is the input power and is here taken to be the output power because of the assumption of high efficiency. X_{CO} is the impedance of the output capacitor and varies with frequency. ΔV_{COMP} is the range of the voltage error amplifier output and is equal to 4.5V on the UC3853. V_O is the DC output voltage. By using the output power ($V_O \bullet I_O$) in the

equation, all of the terms that are associated with the multiplier and divider drop out of the equation.

The gain of the voltage divider, G_{VD}, is given above. The gain of the transconductance amplifier and its load are given by the following:

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the amplifier and X_{CVC} is the impedance of the compensation capacitor C_{VC}.

Finally, the equation for the loop can be written from these equations as:

$$G_V = \frac{P \bullet X_{CO} \bullet G_M \bullet X_{CVC} \bullet G_{VD}}{\Delta V_{COMP} \bullet V_O}$$

By setting $G_V = 1$ the equation can be solved for frequency since all other variables are known at this point. Note that there are two terms in the equation which vary with frequency, X_{CO} and X_{CVC}. The loop has a second order roll off at this point so the equation is solved for the square of the frequency. The unity gain crossover frequency, f_{VI}, is found from the following equation.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

For the example converter f_{VI} is 18.6Hz. The value of R_{VC}, which is what we have been trying to determine all along, is equal to the impedance of C_{VC} at f_{VI}. For the example converter, this is 57kΩ, so a 56kΩ standard value resistor is chosen.

The last step is the addition of a low frequency zero in the feedback loop. It is accomplished by adding C_{VCZ} in series with R_{VC} as shown in the schematic. From an operational standpoint, the effect of C_{VCZ} is to double the peak-to-peak variation of the output voltage during a step load transient. The overvoltage protection circuit built into the UC3853 will prevent the output voltage from exceeding the maximum value by turning the switch off until the output voltage is back within range. The undervoltage transient caused by a step load change will be unaffected.

The value of C_{VCZ} is not especially critical. However, since it adds both a pole and an zero to the loop gain, the zero must be far enough away in frequency from the C_{VC} and R_{VC} pole so that it does not contribute extra phase shift at the unity gain frequency, f_{VI}. This requires that the zero be at least two octaves below f_{VI}. For the example converter, the zero has been placed almost a full decade below f_{VI} and the value of C_{VCZ} is chosen as 1.0µF.

THE FEEDFORWARD VOLTAGE AND STARTUP CIRCUIT

The UC3853 makes use of a divider and squaring circuit to compensate the gain of the voltage loop for changes of the input voltage as shown in Figure 5. The input to the squarer and divider is the supply voltage to the UC3853 and is called V_{FF}. The function of the supply voltage, besides powering the chip, is to feed-forward information about the input voltage to the voltage loop. This means that V_{FF} must be proportional to the average value of the input voltage and must also have low ripple voltage because 1% ripple on this voltage will create 1% harmonic distortion on the input current.

The V_{FF} input is generated by a winding on the boost inductor that operates like a transformer. When the switch is turned on, the voltage across the inductor is equal to the input voltage. This voltage is tapped off by using an additional winding on the inductor to supply the control circuits. The current drain of the control circuits, I_{CC}, is typically about 15mA of which 10mA are allocated to the UC3853 and 5mA are allocated to the MOSFET gate drive current. These currents are constant and do not change appreciably with a change of the supply voltage.

The supply voltage range of the UC3853 is great enough to cover a 3:1 input voltage range. To provide the best utilization of the V_{FF} programming range the supply voltage to the UC3853 should be set to provide 10.5V when the input voltage is at low line. If a narrower range is being used for the input voltage than is used for this example, it may be desirable to set the minimum voltage slightly higher, in the range of 12V to 15V, to provide more voltage for the gate drive at lower line voltages and thus lower R_{DSon}. For the example converter, a turns ratio of 10:1 on the inductor will provide the correct value of V_{FF}. The minimum voltage is about 10.5V, with an input line voltage of 80VAC, after all of the diode drops have been taken into account. The UVLO threshold for turning the UC3853 off is 9.5V so a 10.5V minimum value of V_{FF} leaves some margin in the design for component variation.

The diode D_{FF} must block 80V, carry an average current of 15mA for the example converter and have a very fast recovery time. Small 100V diodes, such as BYD71B or MUR110 are suitable devices for this application.

The amount of harmonic distortion allocated to the V_{FF} input of the UC3853 is 2%, so the ripple voltage must be held to 2% of the minimum value of V_{FF}. For the example converter, the minimum voltage is 10.5V so the allowable ripple voltage is 0.21V. This is not the peak-to-peak value of the ripple but is the peak value of the second harmonic of

the line frequency. The peak-to-peak ripple voltage, ΔV_{FF}, is this value multiplied by π. For the example converter, ΔV_{FF} is therefore 0.66V peak-to-peak.

The value of C_{FF} can be found from the equation for a capacitor and the current drain of the control circuits, I_{CC}.

$$C_{FF} = \frac{I_{CC}}{\Delta V_{FF} \bullet 2 \bullet f_{Lmin}}$$

Where C_{FF} is the value of the V_{FF} bypass capacitor, I_{CC} is the current drain of the control circuits, ΔV_{FF} is the peak-to-peak ripple voltage on V_{FF} and f_{Lmin} is the minimum line frequency. For the example converter the value is 240µF. A standard value of 270µF is chosen and it is bypassed with a 0.1µF ceramic capacitor.

This value for C_{FF} also gives sufficient time to start the circuit since one half cycle of the input line frequency is needed to reach full operation. The turn-on threshold of the UC3853 is 11.5V and the turn-off threshold is 9.5V so there is more than sufficient energy stored to begin circuit operation.

$$\Delta t = \frac{C_{FF} \bullet (V_{TN} - V_{TF})}{I_{CC}}$$

Where Δt is the amount of time available for start-up, C_{FF} is the capacitance on V_{FF}, V_{TN} is the turn on threshold of the UC3853 (11.5V), V_{TF} is the turn off threshold (9.5V), and I_{CC} is the current drain of the control circuits. For the example converter Δt is 36 milliseconds.

Startup of the UC3853 is accomplished by charging V_{FF} to 11.5V through R_B. The value of R_B must be small enough to provide a reasonably short turn-on delay after power is applied and yet large enough to keep power dissipation low. The current through R_B at V_{INmin} must also be greater than the UC3853 startup current (500µA). For the example converter a 1 second delay at turn-on requires a bias current of approximately 3mA from the low input line voltage. The equivalent resistance is about 36kΩ. This resistance needs to be split into two equal resistors since the peak input voltage will exceed 250V so two 18kΩ resistors are used. At high line this gives about 6.8mA of bias current to V_{FF}. This is less than the current required by the UC3853 so this value of R_B is acceptable. If the current at high line were too great, V_{FF} would not accurately reflect the input voltage and performance would suffer. A larger value of R_B resulting in a longer turn-on delay is required in that case. At high line each of the 18kΩ resistors dissipates 0.82W. A 2W rating is specified.

The gate drive voltage of the UC3853 is limited to 15V by an internal clamp. This allows V_{FF} to change without causing the gate voltage to exceed the rating of the MOSFET. The UC3853 is designed to drive moderate size MOSFET switches, and the gate drive current is limited to 500mA(pk). This is more than sufficient to obtain the fast rise and fall times needed for high efficiency. R_Q is the resistor in series with the gate of the MOSFET. Its value of 33Ω is chosen to limit the peak gate current to about 350mA under normal operating conditions. In addition, this is the minimum value for which D_Q, the gate drive clamp, is NOT required under most circumstances. In general, if R_Q is made small there will not be sufficient damping of the resonance of the parasitic circuit inductances with the MOSFET gate capacitance, so the output of the UC3853 could be drawn below ground. Keeping R_Q in the range of 30Ω to 60Ω prevents this, eliminates the need for D_Q and at the same time provides ample output current for fast rise and fall times on the drain of the MOSFET. It is wise practice to leave room for D_Q on the circuit board until it can be verified in the laboratory that it is not needed.

OVER CURRENT PROTECTION

The boost converter is inherently unprotected against any overload situation. Because the switch is connected in parallel with the input source, the DC current path through the inductor, diode and the load impedance (parallel combination of C_O and R_L) can not be interrupted. The result is practically unlimited current flowing from the input to the output of the converter when the output voltage falls below the input voltage. This happens every instance when power is being applied to the converter at startup and when the load requires more power than the circuit was originally designed for. Unfortunately, these situations can not be avoided, but there are certain measures which can protect the circuit from a catastrophic failure.

The diode, D_{BP} in Figure 6 provides protection for the boost inductor and for the output rectifier, D_{OUT}. During the initial charging of the output capacitor at startup and in case of an overload, a high surge current flows from the input to the output of the converter. This high peak current would flow through the boost inductor and the very sensitive high speed epitaxial diode used for rectification. This high surge current can saturate the inductor and damage the diode causing a disastrous failure eventually. D_{BP} prevents the high current flowing in the inductor-diode path by providing a lower impedance direct path between the input and the output. The additional benefit of the D_{BP} diode is the protection against input voltage transients. When other high power loads are connected to the same distribution branch of the power line, their turn off generates huge inductive spikes

appearing at the input of the power factor corrector power supply. This can cause the input voltage of the boost converter to be higher than its output voltage even under normal operating conditions. The voltage spikes impose an increased voltage stress on the input rectifier diodes and it might cause the boost inductor to saturate depending on the duration and the amplitude of the line transient. The addition of the D_{BP} diode clamps the input voltage to the output capacitor voltage which will also absorb the transient energies without passing high current through the boost inductor and rectifier diode.

In normal circumstances D_{BP} has no effect on the circuit operation. Note that the diode D_{BP} can not prevent the circuit from developing high currents from the input to the output. It simply provides a safe passage for the high current to pass through the circuit. Once the high current is flowing, it has to go through the current sense resistor, R_S. Higher than nominal currents will develop negative voltage across R_S in excess of the 1V maximum value used in the design. Since the I_{MO} current is limited to $0.5 \bullet I_{AC}$, the IMO pin of the UC3853 will be pulled below ground. This could present a problem for the integrated circuit because of reverse biasing the substrate. When the IMO pin is pulled 0.3V below ground (to -0.3V), the OUT pin goes high turning on the main switch of the boost converter. Since the current can not be limited, the only way to avoid the parasitic turn on of the output is to limit the negative voltage on the IMO pin of the IC. It is accomplished by the Schottky diode, D_{MO} connected between the IMO pin of the UC3853 and circuit ground, as shown in Figure 6.

ABOUT SYNCHRONIZATION

Synchronization of the UC3853 oscillator requires a fast falling edge on the FB pin. The minimum requirements for the falling edge of the waveform are that it must have a slope of at least 20V/µsec and an amplitude of at least 1.0V. Faster fall times and greater amplitudes are strongly recommended. The amplitude of the sync signal must be kept below 3.0V so that the FB pin is not driven below ground. The sync signal must be capacitively coupled into the FB pin so that the DC feedback is not disturbed by the synchronization. The capacitor must be large enough so that it does not gain enough voltage during the pulse to trip the overvoltage comparator of the UC3853 on the rising edge of the sync waveform. These requirements are easily met with the circuit of Figure 11 as shown below.

In most applications the UC3853 will be synchronized to another PWM integrated circuit used to control the DC output voltage of the power supply. A few PWM integrated circuits, such as the UC3526A, have inverted pulse sync outputs and these can be interfaced to the UC3853 with just a small capacitor. Other PWM circuits have an output pulse which is positive and has a narrow pulse width. This signal needs to be inverted and conditioned to interface with the UC3853. If the pulse is more than 100nsec wide then the signal must be shortened as well. Some PWM integrated circuits do not have a sync output but these can still be synchronized with a little ingenuity and a few small parts.

A schematic of a generic sync circuit is shown in Figure 11. This circuit accepts a positive input pulse and provides the correct output pulse to the FB pin of the UC3853. The pulse is capacitively coupled to the FB pin through C_{SYNC}. The value of this capacitor is chosen so that the voltage change across it during a 2.5V pulse of 100 nanoseconds duration is about 100mV. This precludes the sync pulse having a significant effect on the UC3853 output voltage. If R_{VD} in Figure 6 is about 10kΩ then C_{SYNC} will be about 220pF. A larger value for C_{SYNC} may be used but the capacitor adds a pole to the feedback loop and the pole must be kept above the switching frequency. The voltage divider R_{SVD1} and R_{SVD2} reduce the effect of the pole by providing a compensating zero so their impedance must be relatively high. A value of 22kΩ was chosen to present a 10k impedance to the feedback network and thus keep the additional pole and zero relatively close together. The 5V source for the voltage divider is supplied from another PWM integrated circuit.

An NPN transistor is shown in Figure 11 to invert the input signal and drive the FB pin of the UC3853. Any fast general purpose small signal transistor will work in this application. The network chosen for the base of the transistor depends on the clock that it is being interfaced to. The base network shown in Figure 11 allows the circuit to work with a wide variety of inputs. C_{ST} and R_{ST} form a 100nsec time constant which will limit the width of

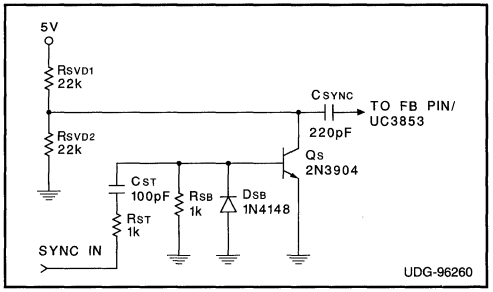

Figure 11. Synchronization Circuit for Positive Edge Sync Signals

the sync pulse output. The resistor R_{SB} and diode D_{SB} provide reset for the sync input time constant. A relatively fast rising edge on the input pulse is required for proper circuit operation.

As an example of synchronization, the sync circuit in Figure 11 may be used with the UC3525B by connecting the sync circuit input to the CLOCK output. The UC3525B has a positive going clock pulse whose width is equal to the discharge time of the timing capacitor. If the clock pulse width is small, below 100nsec, the input capacitor to the sync circuit, C_{ST}, may be eliminated.

Figure 12 shows a sync circuit for the UCC3802. This circuit may be modified for use with other PWM control circuits that do not have an oscillator sync output. The UCC3802 discharges the timing capacitor C_T with a 1.8mA current. The sync circuit is configured so that when C_T discharges, a negative voltage appears across R_{ST}. The emitter of Q_S is connected here and when the C_T is being discharged most of the current flows through Q_S and takes it into saturation. The collector of Q_S is connected to the FB pin of the UC3853 through the same network described above. The base of Q_S is biased above ground because the timing capacitor C_T will not discharge completely in this circuit due to the voltage offset of the emitter base junction of Q_S. This offset voltage changes the amplitude of the oscillator voltage and its frequency. By raising the base of Q_S above ground, the offset voltage is minimized. The offset voltage also has a temperature coefficient and D_S compensates for this so that the oscillator frequency drift over temperature will be reduced. All of the base components are optional but they do improve the performance of the sync circuit.

Further information about synchronization in general may be found in Unitrode Application Note U-111. Several of the circuits there may be adapted to the UC3853 synchronization circuits shown here.

LAYOUT CONSIDERATIONS

The UC3853 is a high speed circuit generally operating in a high noise environment. It requires careful layout and grounding to operate correctly. A ground plane extending at least 1 inch on each side of the device is recommended to control noise pickup. Do not let power currents in the ground plane run beneath the device. A split in the ground plane is acceptable to control the flow of current and divert it around the device if necessary. It is worthwhile to keep low level signals as far away from high noise signals, such as the output gate drive, as possible. Good bypassing of the VCC pin is essential. A 0.1µF ceramic capacitor connected between VCC and GND should be located within 0.5 inch of the UC3853 and connected with short, direct connections. The IMO pin and the FB pin are especially sensitive to noise because they are high impedance nodes. Keep the amount of printed circuit board trace connected to these pins as short as possible. The total length should be kept less than 1 inch. The general rule of thumb for printed circuit board layout is to place the UC3853 in the desired position and then to place the ceramic bypass capacitor as close to the VCC pin as possible. Then, and only then, proceed with placing the other components.

DISCONTINUOUS CONDUCTION MODE AND LIGHT LOAD OPERATION

The boost converter described in this Application Note normally runs in continuous inductor current mode but enters discontinuous conduction mode when the input voltage is low and when the load current is light. In discontinuous conduction mode

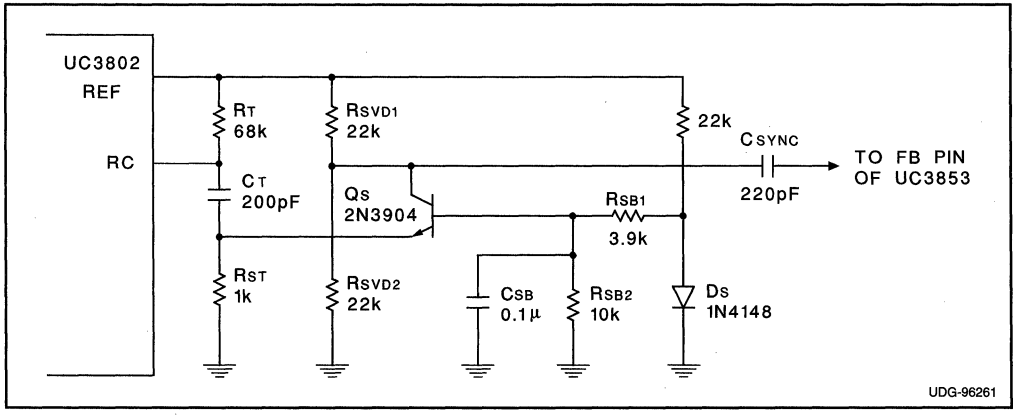

Figure 12. Synchronization Circuit for PMW Control Circuits Without a Clock Output

the gain of the boost power stage is reduced which can lead to reduced performance. The UC3853 uses an average current control technique where the boost power stage is embedded in a feedback loop that includes a high gain opamp which compensates for the changes in gain. The average current control loop regulates the input current in the converter and maintains the correct input current wave shape even though the current through the inductor is not continuous.

During operation of the converter at light loads, the input filters can contribute phase shift to the input current that reduces the power factor. Careful design is required to maintain high power factor at light loads. A capacitor, generally included after the input diodes as part of the input filter, is necessary to keep the high frequency ripple current from the boost converter out of the power lines. At light loads this capacitor holds charge as the input voltage goes through zero volts and turns the diode bridge off, introducing distortion into the input current. This is why the input capacitor value must be carefully selected.

It is possible to design a power factor corrector using the UC3853 which operates only in discontinuous inductor current mode. Such a converter will have good power factor and low distortion input current but it will also have high input ripple current which must be filtered out to pass EMI requirements. The design of a discontinuous conduction mode boost power factor corrector is not covered in this Application Note.

Another application of the UC3853 is with a flyback converter to produce a power factor corrected input current and a regulated and, optionally, isolated output voltage. Any power factor corrected converter produces a sinusoidal output current at the second harmonic of the input line frequency so a large amount of filtering or secondary regulation may be necessary to provide a useful output in most applications. The flyback converter may be operated in either continuous or discontinuous conduction modes. Both modes have large amounts of high frequency input current that must be filtered out to meet EMI requirements and the filter produces phase shift of the input current and reduces the power factor. The design of a flyback converter for power factor correction is not covered by this Application Note although the design is not particularly difficult.

DESIGN SUMMARY

This section summarizes the design process for a boost power factor corrector using the UC3853. The 100W design example with "universal" input voltage range used in the body of this Application Note is repeated here.

1. Specifications: Determine the operating requirements for the boost power factor corrector.

   Example:

   P_{OUTmax} = 100 Watts

   V_{OUT} = 400VDC

   Line voltage range = 80 to 270VAC

   Line frequency range = 47 to 65Hz

   Maximum THD = 5%

   Power Factor = 0.99

2. Switching frequency: The switching frequency is fixed at 75kHz but may be synchronized in the range of 95kHz to 115kHz. See the text for further information on synchronization.

3. Inductor selection:

   A. Find the maximum peak line current. Assume $P_{IN} = P_{OUT}$ and use P for the power rating.

   $$Ipk = \frac{2 \bullet P}{V_{INmin}}$$

   Example:

   $$Ipk = \frac{2 \bullet 100W}{80V} = 1.77Apk$$

   B. Find ΔI, the peak-to-peak high frequency ripple current. See the text for information on the selection of the ripple current. The typical range is 15 to 25% of Ipk.

   $$\Delta I = 0.2 \bullet Ipk$$

   Example:

   $\Delta I = 0.2 \bullet 1.77Apk = 0.35Apk\text{-}pk$

   C. Find the minimum duty factor, D, at $V_{INmin(pk)}$. This occurs at Ipk.

   $$D = \frac{V_O - 2 \bullet V_{INmin}}{V_O}$$

   Example:

   $$D = \frac{400V - 2 \bullet 80V}{400V} = 0.72$$

   D. Calculate the inductor value.

   $$L = \frac{2 \bullet V_{INmin} \bullet D}{f_S \bullet \Delta I}$$

   Example:

$$L = \frac{2 \bullet 80V \bullet 0.72}{75 \bullet 10^3Hz \bullet 0.35A} = 3.1mH$$

Round this value to 3.0mH.

4. Output capacitor selection: If hold-up time is important use the equation below. Typical values for a 400V output are 1µF to 2µF per Watt. If hold-up is not required, use the second harmonic ripple voltage and capacitor power dissipation to determine the minimum size of the capacitor. Δt is the hold-up time in seconds and V_{Omin} is the voltage to which the output decays at the end of the hold-up time.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Example: V_{Omin} is 350V and Δt is 19msec.

$$C_O = \frac{2 \bullet 100W \bullet 19 \bullet 10^{-3}sec}{(400V)^2 - (350V)^2} = 100\mu F$$

5. Current sense resistor selection: Select the current sense resistor to give 1.0V at the maximum peak input current.

$$R_S = \frac{1V}{Ipk + \frac{\Delta I}{2}}$$

Example:

$$R_S = \frac{1V}{1.77A + 0.5 \bullet 0.35A} = 0.5\Omega$$

6. Switch and diode selection: The switches and diodes may be selected from the table which follows this section or may be chosen by any other standard design criteria. The text discusses selection criteria.

   The output drive of the UC3853 provides about 500mA peak current. Choose R_Q to limit the current under normal operating conditions. A value of 33Ω or more will provide adequate control of the gate charge current, give good rise and fall times for small switches and eliminates the need for D_Q. If a lower value of R_Q is chosen, then D_Q is required.

7. Input diode and capacitor selection: Fast recovery rectifiers are recommended for D_{IN}. The faster the diode reverse recovery the lower the input current distortion will be. Choose a diode type rated for the maximum voltage at high line and for the maximum current at low line. It must also have adequate power dissipation capability.

   The choice of C_{IN} is a compromise between power factor and EMI performance. The value may not be too large or input distortion increases. The value may not be too small or EMI increases. Choose a device which will handle the full high frequency ripple current from the boost converter. A film or ceramic type is generally recommended. See the text for further selection information.

8. Multiplier set up: I_{AC} is 500µA maximum. R_{AC} is determined by Ohm's law.

$$R_{AC} = \frac{\sqrt{2} \bullet V_{INmax}}{0.5 \bullet 10^{-3}A}$$

Example:

$$R_{AC} = \frac{\sqrt{2} \bullet 270V}{0.5 \bullet 10^{-3}A} = 764k\Omega$$

Choose two standard value 390kΩ resistors in series to allow for voltage stress ratings.

9. Current amplifier gain at the switching frequency:

   A. Calculate ΔV_{RS}, the voltage change across the sense resistor due to the down slope of the inductor current if $V_{IN} = 0$ (at the zero crossing).

$$\Delta V_{RS} = \frac{V_O \bullet R_S}{L \bullet f_S}$$

Example:

$$\Delta V_{RS} = \frac{400V \bullet 0.5\Omega}{3 \bullet 10^{-3}H \bullet 75 \bullet 10^3Hz} = 0.89V$$

   B. The gain of the current amplifier at the switching frequency is the ratio of the oscillator voltage and ΔV_{RS}. The oscillator voltage in the UC3853 is 5.0Vpk-pk.

$$G_{CA} = \frac{V_{OSC}}{\Delta V_{RS}}$$

Example:

$$G_{CA} = \frac{5V}{0.89V} = 5.625\ (15.0dB)$$

10. Current amplifier compensation:

    A. R_{MO} selection: $R_{MO} = 3.9k\Omega$

    B. R_{CZ} selection: R_{CZ} sets the gain of the

amplifier at the switching frequency.

$R_{CZ} = G_{CA} \bullet R_{MO}$

Example:

$R_{CZ} = 5.625 \bullet 3.9k\Omega = 22k\Omega$

C. C_{CZ} selection: Calculate the unity gain crossover frequency of the current loop if C_{CZ} were not present.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{V_{OSC} \bullet 2 \bullet \pi \bullet L \bullet R_{MO}}$$

Example:

$$f_{CI} = \frac{400V \bullet 0.5\Omega \bullet 22 \bullet 10^3\Omega}{5V \bullet 2 \bullet \pi \bullet 3 \bullet 10^{-3}H \bullet 3.9 \bullet 10^3\Omega}$$

$$= 12 \bullet 10^3Hz$$

Choose the value of C_{CZ} to have an impedance equal to or less than R_{CZ} at f_{CI}.

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

Example:

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet 12 \bullet 10^3Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 600 \bullet 10^{-12}F$$

Choose a larger value of capacitance to increase the phase margin. $C_{CZ} = 680pF$.

D. C_{CP} selection: The C_{CP} and R_{CZ} pole must be greater than the switching frequency.

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet f_S \bullet R_{CZ}}$$

Example:

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet 75 \bullet 10^3Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 100 \bullet 10^{-12}F$$

Choose a smaller value of capacitance.

$C_{CP} = 68pF$

11. Harmonic Distortion Budget: The allocation of the allowed THD among the main error sources is somewhat arbitrary. The feedforward voltage contributes 1% third harmonic distortion for each 1% second harmonic on the bias supply to the UC3853. The voltage loop contributes 0.5% third harmonic distortion for each 1% second harmonic voltage on the output.

    Example: The specification is for 5% THD maximum. 2% is allocated to the feedforward voltage, 2% is allocated to the voltage control loop and 1% to miscellaneous sources.

12. Voltage amplifier: The voltage loop amplifier is a transconductance amplifier so its compensation is a bit different from other types of amplifiers.

    A. Voltage Divider: R_{VI} and R_{VD}. This voltage divider sets the DC output voltage. The UC3853 reference voltage is 3.0V. Choose a value for R_{VD} and calculate the value for R_{VI} from the equation.

    $$R_{VI} = R_{VD} \bullet \left(\frac{V_O}{V_{FB}} - 1\right)$$

    Example:

    Choose $R_{VD} = 10k\Omega$.

    $$R_{VI} = 10 \bullet 10^3\Omega \bullet \left(\frac{400V}{3V} - 1\right) = 1.3 \bullet 10^6\Omega$$

    Choose two standard value $620k\Omega$ resistors in series for R_{VI} to allow for the resistor voltage rating.

    Solve for a parallel resistance to R_{VD} to get correct output voltage.

    $$R_{VD} = \frac{R_{VI} \bullet V_{FB}}{V_O - V_{FB}}$$

    Example:

    $$R_{VD} = \frac{1.24 \bullet 10^6\Omega \bullet 3V}{400V - 3V} = 9.37 \bullet 10^3\Omega$$

    This is $10k\Omega$ in parallel with $150k\Omega$.

    B. Voltage divider gain: The gain of the voltage divider is given from the following equation:

    $$G_{VD} = \frac{V_{FB}}{V_O}$$

    Example:

    $$G_{VD} = \frac{3V}{400V} = 0.0075 \ (-42.5dB)$$

    C. Output ripple voltage: Output ripple voltage is given by the following equation where f_{Lmin} is the minimum line frequency. Low line frequency will give the greatest value of V_{Opk}.

    $$V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

    Example:

$$V_{Opk} = \frac{100W}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 100 \bullet 10^{-6}F \bullet 400V}$$

$$= 4.2V$$

D. Amplifier Gain: This gain calculation includes the gain of the voltage divider. The input range to the multiplier is the active range of the amplifier output voltage on the UC3853. ΔV_{COMP} is 4.5V on the UC3853. The %ripple used in the equation below is the amplitude of the ripple at the output of the voltage amplifier as a percentage of ΔV_{COMP} and the percentage is twice that specified for second harmonic voltage since the ripple is reduced by half in the power circuits. The equation uses %ripple in its numeric form.

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{V_{Opk}}$$

Example:

$$G_V = \frac{4.5V \bullet 0.04}{4.2V} = 0.043 \ (-27.3dB)$$

The gain of the voltage error amplifier alone is G_V divided by the gain of the voltage divider.

$$G_{VEA} = \frac{G_V}{G_{VD}}$$

Example:

$$G_{VEA} = \frac{0.043}{0.0075} = 5.73 \ (15.2dB)$$

E. Amplifier Compensation: A network connected from the output of a transconductance amplifier to ground determines its gain and frequency response. The gain of the amplifier is set for loop stability without regard to DC gain or THD. Those considerations come next. The gain of the amplifier is:.

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the UC3853 voltage amplifier as specified in the data sheet as 485µS. X_{CVC} is the impedance of C_{VC} at the second harmonic of the line frequency ($2 \bullet f_{Lmin}$). Solve the equation for X_{CVC} then convert the impedance to a capacitance value.

$$C_{VC} = \frac{G_M}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet G_{VEA}}$$

Example:

$$C_{VC} = \frac{485 \bullet 10^{-6}S}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 5.73} = 0.15 \bullet 10^{-6}F$$

F. Unity Gain Voltage Loop Crossover Frequency: The unity gain frequency of the now completed voltage control loop is found next. The following equation gives the frequency at which the loop gain is equal to one. Solve for f_{VI}.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

Example:

$$f_{VI} = \frac{1}{2 \bullet \pi} \bullet \sqrt{\frac{100W \bullet 485 \bullet 10^{-6}S \bullet 0.0075}{100 \bullet 10^{-6}F \bullet 0.15 \bullet 10^{-6}F \bullet 4.5V \bullet 400V}}$$

$$= 18.6Hz$$

G. R_{VC}: R_{VC} is added to the loop compensation to give a pole at f_{VI}. The value of R_{VC} is the resistance equal to the impedance of C_{VC} at f_{VI}. This gives approximately 45° of phase margin. A smaller value of R_{VC} will increase the phase margin at the expense of loop bandwidth.

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet f_{VI} \bullet C_{VC}}$$

Example

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet 18.6Hz \bullet 0.15 \bullet 10^{-6}F}$$

$$= 57 \bullet 10^3 \Omega$$

The closest standard value is 56kΩ.

H. C_{VCZ}: C_{VCZ} is added in series to R_{VC} to break the DC current path from the output of the voltage error amplifier to ground because the limited current capability of the transconductance amplifier stage. The zero added to the loop compensation increases the DC regulation of the output at the expense of increased peak-to-peak voltage excursions during transients. This zero introduced by C_{VCZ} must be set at least two octaves below f_{CI} to maintain a reasonable

phase margin. The value of C_{VCZ} must therefore be at least four times the value of C_{VC}.

$C_{VCZ} = 4 \bullet C_{VC}$

Example:

$C_{VCZmin} = 4 \bullet 0.15\mu F = 0.6\mu F$

Choose $C_{VCZ} = 1.0\mu F$ to give increased phase margin.

13. Voltage Feedforward: The feedforward voltage comes from the bias supply V_{FF}, which is supplied by a winding on the inductor. For the example converter, the turns ratio is set to give 10.5VDC with minimum input voltage after all parasitic losses are taken into account. The second harmonic ripple voltage must be held to 2% peak of V_{FFmin} according to the THD budget in step #10 above. The numeric value of THD is used in the equation. See the text for further information. The peak-to-peak ripple voltage is given by:

$V_R = \pi \bullet V_{FF} \bullet THD$

Example:

$V_R = \pi \bullet 10.5V \bullet 0.02 = 0.66Vpk\text{-}pk$

The current drawn by the control circuits is about 15mA. The value of C_{FF} is given by:

$$C_{FF} = \frac{I_{FF}}{V_R \bullet 2 \bullet f_{Lmin}}$$

Example:

$$C_{FF} = \frac{0.015A}{0.66V \bullet 2 \bullet 47Hz} = 242 \bullet 10^{-6}F$$

Choose a standard value of 270µF.

14. Starting Resistors: C_{FF} must be charged to 11.5V to start the UC3853 and it is trickle charged from V_{IN} by the current through R_B. The current through R_B at high line must not exceed the bias current of the UC3853 or V_{FF} will not track the input voltage and feedforward will be lost. The value of R_B may not be too large or the delay between the application of power and the start of the circuit will be too long. If the current through R_B is less than 500µA at low line the circuit will never start. A 1sec delay at low line is chosen as the maximum value. This is an arbitrary decision within the guidelines given.

$$R_B = \frac{t_{DELAY} \bullet \sqrt{2} \bullet V_{INmin}}{V_{FF} \bullet C_{FF}}$$

Example:

$$R_B = \frac{1sec \bullet \sqrt{2} \bullet 80V}{11.5V \bullet 270 \bullet 10^{-6}F} = 36 \bullet 10^3\Omega$$

Split this into two 18kΩ resistors because the voltage at high line is greater than 250V peak. At high line this gives 6.8mA of bias current which is less than I_{FF} (15mA) so this value is acceptable.

15. This completes the design of the boost power factor corrector.

DESIGN TABLE FOR "UNIVERSAL" INPUT VOLTAGE RANGE								
P_{OUT}	25	50	75	100	125	150	200	(Watts)
L	12	6.0	4.0	3.0	2.5	2.0	1.5	(mH)
C_O	25	50	75	100	125	150	200	(µF)
R_S	2.0	1.0	0.68	0.5	0.39	0.33	0.25	(Ω)
C_{IN}	0.22	0.5	0.68	1.0	1.0	1.0	1.0	(µF)
Q	IRF820 ----------> I RF830 ----------> I							
D_{OUT}	MUR160 --------> I		MUR460 -----> I		MUR860 ----------> I			
	BYV26C --------> I		BYM26C ------> I					
D_{IN}	1N4005 ---------> I MR856 ----------> I							
	1N4937 ---------> I BYW95C ----------> I							

Note: The values of the control circuit components remain the same and do not change with power output as long as the main component values are selected from the table. The control circuit components do change value under several circumstances: 1) The main component values are different from those given in the table. 2) The input voltage range or frequency range is different from that specified for the example converter. 3) The THD budget is different. 4) The output voltage is different.

INDUCTOR DESIGN

The 3.0mH inductor may be built as follows:

Core: Micrometals T157-8/90 — OD = 1.57in.
ID = 0.95in. Ht = 0.57in. m = 35
Main winding: 250 turns #20AWG
Auxiliary winding: 25 turns #28AWG

The core is an iron powder toroid. The two windings must be phased properly for correct operation of the converter. The main winding is best wound with bank or progressive winding rather than layer winding. Progressive or bank winding starts at one point on the core and winds progressively around the core until all the turns are in place. A small amount of backing up is required to get the wires to lay evenly on the core. The object is to get the turn-to-turn voltage to be as low as possible. This reduces the effective capacitance of the winding and increases the resonant frequency as well as eliminating the possibility of corona in the winding. The auxiliary winding needs to be insulated from the main winding and is wound outside the main winding.

HEAT SINK

The switch in the example converter dissipates approximately 8W at low line input. The heat sink is an Aavid 529802 and has a thermal resistance of 5°C/W.

REFERENCES

[1] P. C. Todd, "UC3854 Controlled Power Factor Correction Circuit Design," Unitrode Applications Note U-134.

[2] L. H. Dixon, "High Power Factor Preregulator for Off-Line Supplies," Unitrode Power Supply Design Seminar Manual SEM600, 1988. (Reprinted in subsequent editions of the Manual.)

[3] L. H. Dixon, "High Power Factor Switching Preregulator Design Optimization," Unitrode Power Supply Design Seminar Manual SEM700, 1990. (Reprinted in subsequent editions of the Manual.)

[4] L. H. Dixon, "Average Current Mode Control of Switching Power Supplies," Unitrode Applications Note U-140.

[5] W. Andreycak, "Practical Considerations in Current Mode Power Supplies," Unitrode Applications Note U-111.

[6] S. Freeland, "Input Current Shaping for Single Phase AC-DC Power Converters," Ph.D. Thesis, California Institute of Technology, 1988.

APPENDIX A: WHAT IS POWER FACTOR?

If a resistor is connected to a sinusoidal AC power line, the current will be sinusoidal and it will be in phase with the voltage. Any deviation from this ideal results in distortion of the current waveform. The apparent power delivered to the load is the sum of the real power and the distortion. The ratio of the apparent power delivered to the load and the real power delivered is the power factor and has a value between zero and one. The current through a purely resistive load has no phase shift and no harmonic distortion and so has a power factor of 1.0. Power factor is given by the following equation:

$$PF = \frac{\text{Real Power}}{V_{RMS} \bullet I_{RMS}}$$

The distortion of the input current has two components, a linear component which is the phase shift between the voltage and current and a non-linear component which is the harmonic distortion of the current waveform. The above equation for power factor may be solved for the phase distortion and the result becomes:

$$PF = \cos(\Theta)$$

Where Θ is the angle between the voltage sinusoid and the current sinusoid. This is the classic definition of power factor as used by electric utilities and it is the major form of distortion created by linear circuits such as motors.

The equation for power factor may also be solved for the harmonic distortion and the equation becomes:

$$PF = \frac{1}{1 + (THD)^2}$$

Where THD is the Total Harmonic Distortion of the current. This equation is the one with which we are most concerned in power electronics.

In a typical power electronics application the sinusoidal voltage from the power line is rectified and filtered to produce a high DC voltage which is then changed by a DC/DC converter to some other voltage which is useful to the system. The current from the rectifier and input filter generally has little phase shift but has much distortion. A choke input filter will produce a square wave input current with a power factor of about 0.9 and a THD near 50%. A capacitor input filter will produce a train of sharp current spikes with a power factor near 0.5 and THD over 100%. A power factor corrected input will produce a sinusoidal current which has a power factor of greater than 0.99 and harmonic distortion well below 5% at nominal load.

Power factor correction is required in much of the European Community for many electronic products. Power factor correction simplifies the distribution of electric power and thus reduces the cost to the consumer. It is expected that the requirement for power factor correction will grow in the future.

The boost power factor corrector is a boost converter whose control circuit programs the input cur-

UNITRODE CORPORATION
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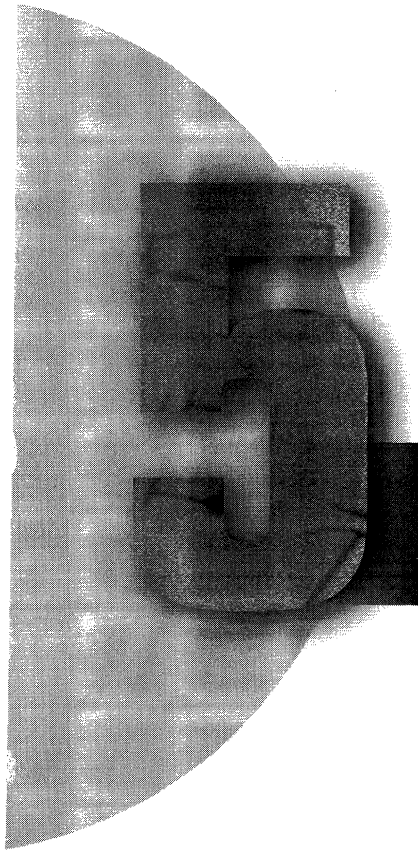


Linear Regulation

Linear Regulation

Linear Controllers	UNITRODE PART NUMBER				
	UC3832	UC3833	UC3834	UC3835	UC3836
Type of Output	Positive Adjustable	Positive Adjustable	Positive / Negative Adjustable	5V Fixed	Positive Adjustable
Maximum Input Voltage	36V	36V	40V	40V	40V
Minimum Output Voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V
Output Drive	300mA	300mA	350mA	500mA	500mA
Type of Short Circuit Limit	Duty Cycle	Duty Cycle	Foldback	Foldback	Foldback
Reference Voltage Accuracy	2%	2%	3% / 4%	2%	2%
Special Features	Multiple Pins Accessible	8 Pin Package		Built in Rsense	Built in Rsense
Application / Design Note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95		
Pin Count❖	14, 16	8, 16	16	8, 16	8, 16
Page Number	PS/5-11	PS/5-11	PS/5-18	PS/5-24	PS/5-24

Linear Controllers	UNITRODE PART NUMBER				
	UCC3837				
Type of Output	Positive Adjustable				
Maximum Input Voltage	12V				
Minimum Output Voltage	1.5V				
Output Drive	1.5mA				
Type of Short Circuit Limit	Duty Cycle				
Reference Voltage Accuracy	2%				
Special Features	• Internal Charge Pump • Direct N-FET Drive				
Application / Design Note					
Pin Count❖	8				
Page Number	PS/5-28				

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output Voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V / Adjustable
Dropout Voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output Voltage Accuracy	2.5%	1%	1%	1%	1%
Maximum Input Voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown Current	10µA				
Operating Current	400µA				
Line Regulation	0.01% / V				
Load Regulation	0.1%, I_{OUT} = 0 to 1A				
Special Features	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count❖	8	5	5	5	5
Page Number	PP/7-5	PS/5-5	PS/5-5	PS/5-5	PS/5-5

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC383	UC384	UC385-1	UC385-2	UC385-3
Output Voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout Voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output Voltage Accuracy	2.5%	2.5%	1%	1%	1%
Maximum Input Voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown Current	40µA	17µA			
Operating Current	400µA	240µA			
Line Regulation	0.01% / V	0.01% / V			
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA			
Special Features	Power Limit	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count❖	3	8	5	5	5
Page Number	PP/7-12	PP/7-19	PS/5-35	PS/5-35	PS/5-35

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC385-ADJ	UC386+	UC387+	UC388+	
Output Voltage	1.2V / Adjustable	3.3V	5V	Adjustable down to 1.25V	
Dropout Voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA	
Output Voltage Accuracy	1%	1.5%	1.5%	1.5%	
Maximum Input Voltage	7.5V	9V	9V	9V	
Shutdown Current		2µA	2µA	2µA	
Operating Current		10µA	10µA	10µA	
Line Regulation		25mV max	25mV max	25mV max	
Load Regulation		10mV max	10mV max	10mV max	
Special Features	Fast Transient Response	TSSOP	TSSOP	TSSOP	
Pin Count❖	5	8	8	8	
Page Number	PS/5-35	PP/7-29	PP/7-29	PP/7-29	

Special Functions Linear Regulators	UNITRODE PART NUMBER				
	UC560	UCC561+	UC563+		
Type of Output	Positive	Positive	Positive		
Application	Source / Sink Regulator for the 18 and 27 Line SCSI Termination	LVD SCSI Regulator for the 18 and 27 Line Termination	32 Line VME Bus Bias Generator		
Input Voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V		
Output Voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V		
Dropout Voltage	0.9V at 750mA				
Bus Standard	SCSI-1,2,3	SPI-2, 3	VME / VME64		
Sink / Source Current	300mA / –750mA	200mA / –200mA	475mA / –575mA		
Application / Design Note					
Pin Count❖	5, 8	16	3, 8		
Page Number	IF/4-3	IF/4-7	IF/4-10		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product


UNITRODE

UNITRODE

UC182-1,-2,-3,-ADJ
UC282-1,-2,-3,-ADJ
UC382-1,-2,-3,-ADJ

Fast LDO Linear Regulator

FEATURES

- Fast Transient Response
- 10mA to 3A Load Current
- Short Circuit Protection
- Maximum Dropout of 450mV at 3A Load Current
- Separate Bias and VIN Pins
- Available in Adjustable or Fixed Output Voltages
- 5 Pin Package allows Kelvin Sensing of Load Voltage
- Reverse Current Protection

DESCRIPTION

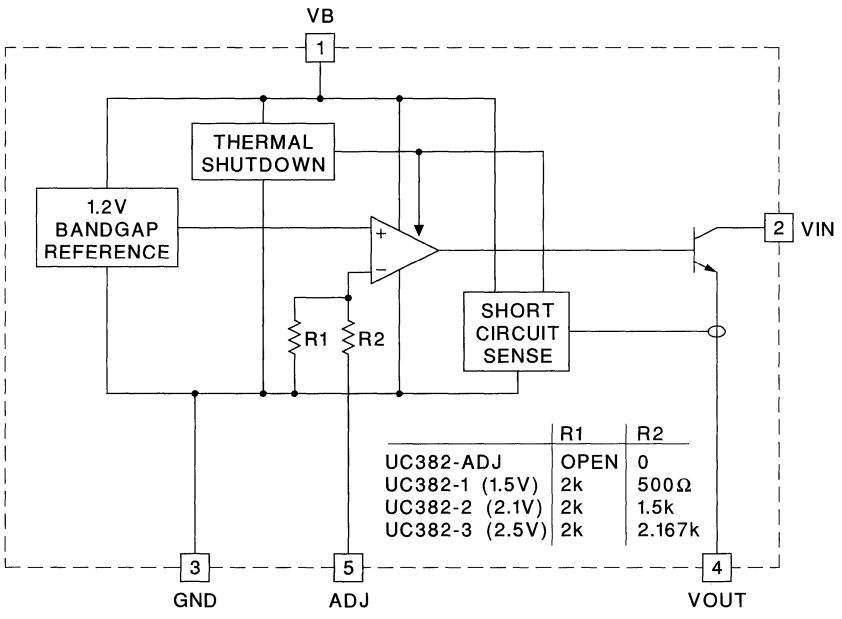
The UC382 is a low dropout linear regulator providing a quick response to fast load changes. Combined with its precision on-board reference, the UC382 excels at driving GTL and BTL buses. Due to its fast response to load transients, the total capacitance required to decouple the regulator's output can be significantly decreased when compared to standard LDO linear regulators.

Dropout voltage (VIN to VOUT) is only 450mV maximum at 100°C and 350mV typical at 3A load.

The on-board bandgap reference is stable with temperature and scaled for a 1.200V input to the internal power amplifier. The UC382 is available in fixed output voltages of 1.5V, 2.1V, or 2.5V. The output voltage of the adjustable version can be set with two external resistors. If the external resistors are omitted, the output voltage defaults to 1.2V.

5

BLOCK DIAGRAM



	R1	R2
UC382-ADJ	OPEN	0
UC382-1 (1.5V)	2k	500Ω
UC382-2 (2.1V)	2k	1.5k
UC382-3 (2.5V)	2k	2.167k

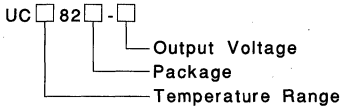
UDG-96037-1

ABSOLUTE MAXIMUM RATINGS

VB 13V
VIN . . . . . +7.5V
Output Voltage . . . . . +1.2V to 6.0V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

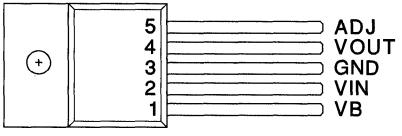
ORDERING INFORMATION



Temperature Range	Package	Output Voltage
1: –55°C to +125°C	T: TO-220	1: 1.5V
2: –25°C to +100°C	TD: TO-263	2: 2.1V
3: 0°C to +100°C		3: 2.5V
		ADJ: 1.2V or Adjustable

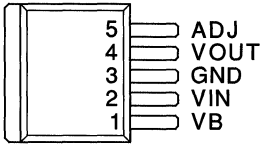
CONNECTION DIAGRAMS

5-Pin TO-220 (Top View)
T Package



Note: Tab tied to Pin 3.

5-Pin TO-263 (Top View)
TD Package



Note: Tab tied to Pin 3.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC182-X series, –25°C to +100°C for the UC282-X series and 0°C to +100°C for the UC382-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V for the UC382-ADJ, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UC382-3 Fixed 2.5V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-3	2.475	2.500	2.525	V
	UC282-3 and UC182-3	2.450	2.500	2.525	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB
VB PSSR		50	60		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, T_J = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-3		350	450	mV
	I_{VOUT} = 3A, UC282-3 and UC182-3		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-3		1.8	2.10	V
	I_{VOUT} = 3A, UC282-3		1.8	2.20	V
	I_{VOUT} = 3A, UC182-3		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	60	mA
VIN Current	I_{VOUT} = 3A	2.94	2.97		A
UC382-2 Fixed 2.1V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-2	2.079	2.100	2.121	V
	UC282-2 and UC182-2	2.058	2.100	2.121	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC182-X series, –25°C to +100°C for the UC282-X series and 0°C to +100°C for the UC382-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V for the UC382-ADJ, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UC382-2 Fixed 2.1V, 3A Family (cont.)					
VB PSSR		52	62		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, T_J = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-2		350	450	mV
	I_{VOUT} = 3A, UC282-2 and UC182-2		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-2		1.8	2.10	V
	I_{VOUT} = 3A, UC282-2		1.8	2.20	V
	I_{VOUT} = 3A, UC182-2		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	60	mA
VIN Current	I_{VOUT} = 3A	2.94	2.97		A
UC382-1 Fixed 1.5V, 3A Family					
Output Voltage (I_{VOUT} = 100mA)	UC382-1	1.485	1.500	1.515	V
	UC282-1 and UC182-1	1.470	1.500	1.515	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR		80	100		dB
VB PSSR		55	65		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, TJ = 25°C		350	425	mV
	I_{VOUT} = 3A, UC282-1		350	450	mV
	I_{VOUT} = 3A, UC282-2 and UC182-1		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-1		1.8	2.10	V
	I_{VOUT} = 3A, UC282-1		1.8	2.20	V
	I_{VOUT} = 3A, UC182-1		1.8	2.35	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	60	mA
VIN Current	I_{VOUT} = 3A	2.94	2.97		A
UC382-ADJ Adjustable, 3A Family					
ADJ Voltage (I_{VOUT} = 100 mA)	UC382-ADJ	1.188	1.200	1.212	V
	UC282-ADJ and UC182-ADJ	1.176	1.200	1.212	V
Load Regulation	I_{VOUT} = 10mA to 3A		0.5	4	mV
VIN PSSR	VOUT Programmed for 2.5V	80	100		dB
VB PSSR	VOUT Programmed for 2.5V	50	60		dB
VIN Dropout Voltage = VIN–VOUT	I_{VOUT} = 3A, T_J = 25°C		350	425	mV
	I_{VOUT} = 3A, UC382-ADJ		350	450	mV
	I_{VOUT} = 3A, UC282-ADJ and UC182-ADJ		350	500	mV
VB Dropout = VB–VOUT	I_{VOUT} = 3A, UC382-ADJ		1.8	2.10	V
	I_{VOUT} = 3A, UC282-ADJ		1.8	2.20	V
Short Circuit Current Limit		3.3		4.5	A
VB Current	I_{VOUT} = 10mA		6	9	mA
	I_{VOUT} = 3A		18	60	mA
VIN Current	I_{VOUT} = 3A	2.94	2.97		A

PIN DESCRIPTIONS

ADJ: In the adjustable version, the user programs the output voltage with two external resistors. The resistors should be 0.1% for high accuracy. The output amplifier is configured as a non-inverting operational amplifier. The resistors should meet the criteria of R3 || R4 < 100Ω. Connect ADJ to VOUT for an output voltage of 1.2V. Note that the point at which the feedback network is connected to the output is the Kelvin sense point.

GND: For accurate results, the GND pin should be referenced to the load ground.

VB: Supplies power to all circuits of the regulator except the collector of the output power transistor. The 2V headroom from VB to VOUT allows the use of a Darlington output stage for inherently low output impedance and fast response. (Dropout is derated for junction temperatures below 0°C.)

VIN: Supplies the current to the collector of the output power transistor only. The dropout (VIN-VOUT) is under 100mV for light loads; maximum dropout is 450mV at 3A for T_J = 0°C to +110°C. (Dropout is derated for junction temperatures over 110°C.) At full load, the majority of the VB current is going to the load.

VOUT: This pin should be connected to the load via a low impedance path. Avoid connectors which add significant inductance and resistance. Note that even though a Kelvin sense is available through a 5 pin package, care must be taken since voltage drops along wire traces add to the dropout voltage.

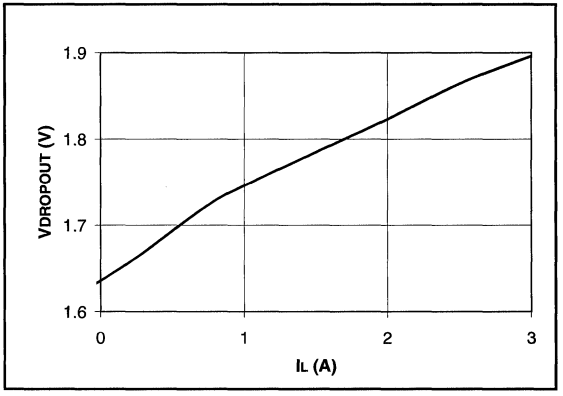


Figure 1. Typical Dropout (V_B - V_{OUT}), T_J = 27°C

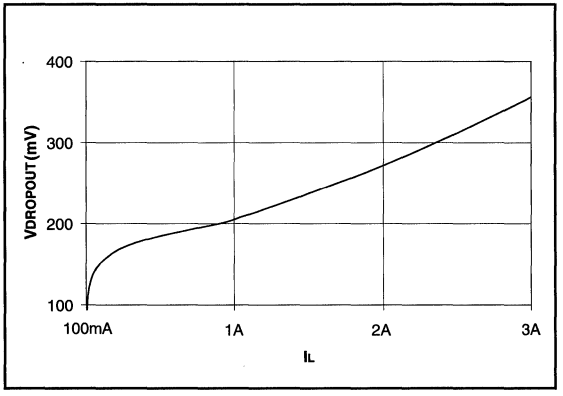


Figure 2. Typical Dropout (V_{IN} - V_{OUT}), T_J = 27°C

APPLICATION INFORMATION

The UC382 is easy to use. The adjustable version requires two 0.1% resistors to set the output voltage. The fixed versions of the UC382 require no external resistors. All versions of the UC382 require decoupling capacitors on the input and output. In a typical application, VB and VIN are driven from switching power supplies which may have large filter capacitors at their outputs. If the UC382 is further than 12 inches from the power supply, it is recommended to add local decoupling as close as possible to the linear regulator.

Decouple the output of the UC382 with at least 100µF of high quality tantalum or Sanyo OSCON capacitors close to the VOUT pin for maximum stability. Many applications involving ultra fast GTL or BTL applications require additional capacitance close to the load. The exact amount will vary according to speed and magnitude of the load transients and the tolerance allowed for transients on VOUT. When specifying the decoupling capacitors, the series resistance of the capacitor bank is an important factor in its ability to filter load transients.

The UC382 allows for Kelvin sensing the voltage at the load. This improves regulation performance and eliminates the voltage drops due to wire trace resistance. This voltage drop must be added to the headroom (VIN to VOUT and VB to VOUT). The dropout of 450mV is measured at the pins and does not include additional drops due to trace resistance. The minimum load current is 10mA.

Two or more UC382's may be used in parallel. While stable, this arrangement does degrade the transient response.

APPLICATION INFORMATION (cont.)

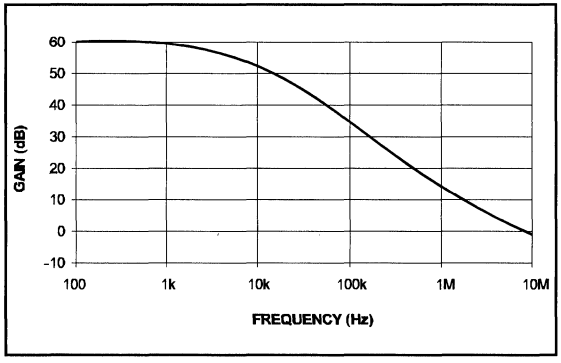


Figure 3. Open Loop Gain (100µF Output Capacitance, 1A Load).

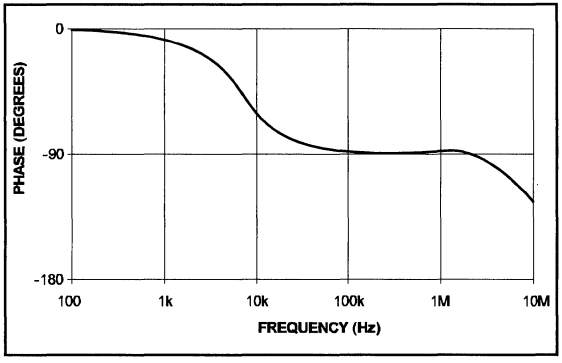


Figure 4. Open Loop Phase (100µF Output Capacitance, 1A Load).

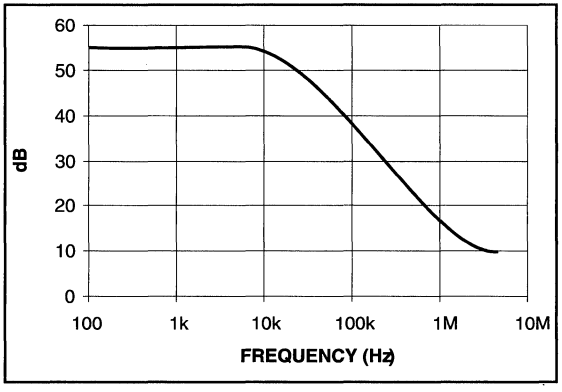


Figure 5. PSRR (V_B) 2.5V Out.

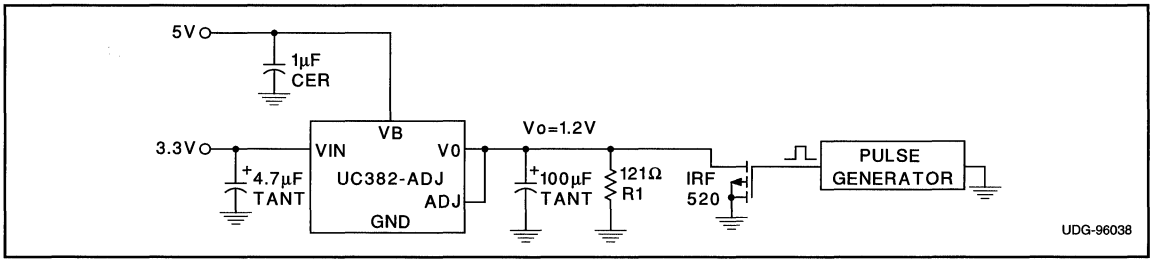


Figure 6. Transient test circuit.

APPLICATION INFORMATION (cont.)

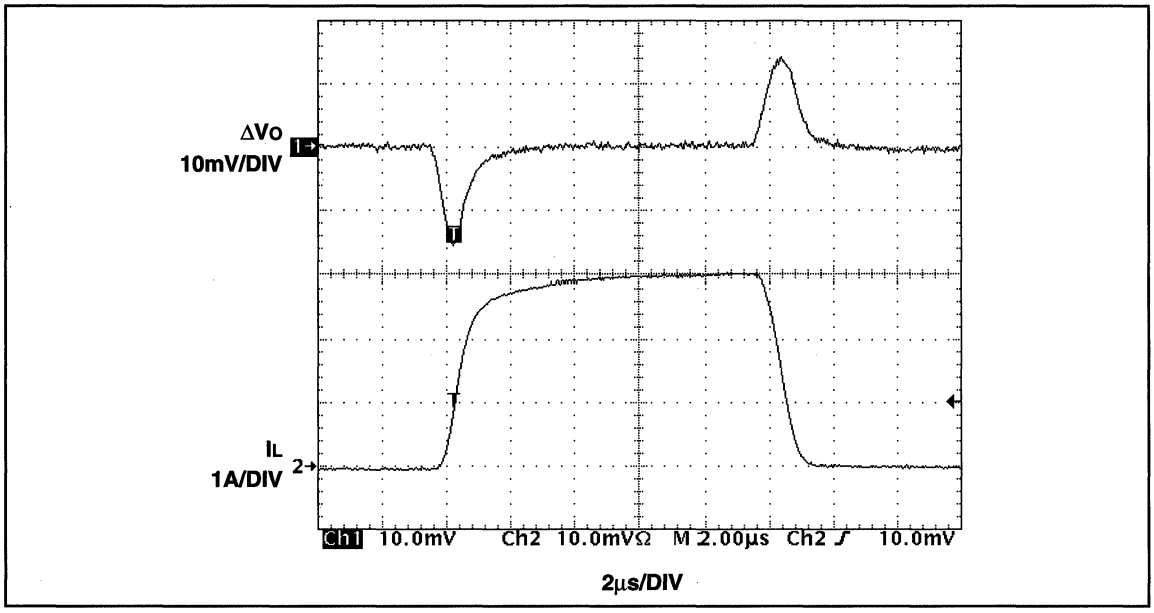


Figure 7. 10mA to 3A/µs load transient response.

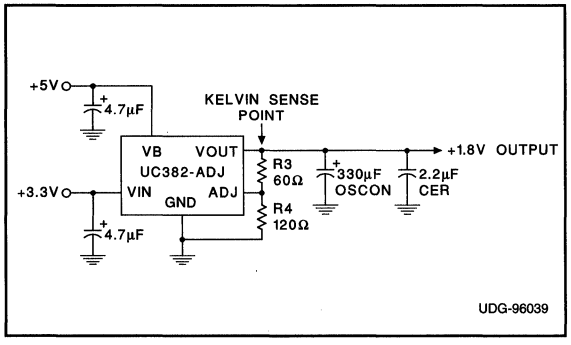


Figure 8. Typical UC382-ADJ application

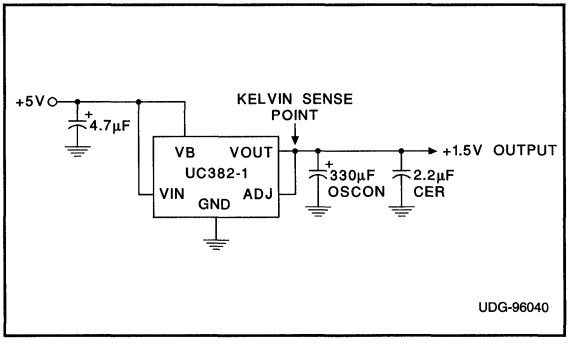


Figure 9. Typical UC382-1, -2, or -3 application

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

application INFO available

UC1832/3
UC2832/3
UC3832/3

Precision Low Dropout Linear Controllers

FEATURES

- Precision 1% Reference
- Over-Current Sense Threshold Accurate to 5%
- Programmable Duty-Ratio Over-Current Protection
- 4.5V to 36V Operation
- 100mA Output Drive, Source or Sink
- Under-Voltage Lockout

Additional Features of the UC1832 series:

- Adjustable Current Limit to Current Sense Ratio
- Separate +VIN terminal
- Programmable Driver Current Limit
- Access to V_{REF} and E/A(+)
- Logic-Level Disable Input

DESCRIPTION

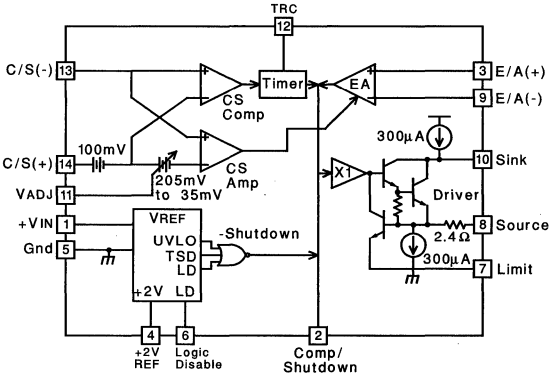
The UC1832 and UC1833 series of precision linear regulators include all the control functions required in the design of very low dropout linear regulators. Additionally, they feature an innovative duty-ratio current limiting technique which provides peak load capability while limiting the average power dissipation of the external pass transistor during fault conditions. When the load current reaches an accurately programmed threshold, a gated-astable timer is enabled, which switches the regulator's pass device off and on at an externally programmable duty-ratio. During the on-time of the pass element, the output current is limited to a value slightly higher than the trip threshold of the duty-ratio timer. The constant-current-limit is programmable on the UCx832 to allow higher peak current during the on-time of the pass device. With duty-ratio control, high initial load demands and short circuit protection may both be accommodated without extra heat sinking or foldback current limiting. Additionally, if the timer pin is grounded, the duty-ratio timer is disabled, and the IC operates in constant-voltage/constant-current regulating mode.

These IC's include a 2 Volt (±1%) reference, error amplifier, UVLO, and a high current driver that has both source and sink outputs, allowing the use of either NPN or PNP external pass transistors. Safe operation is assured by the inclusion of under-voltage lockout (UVLO) and thermal shutdown.

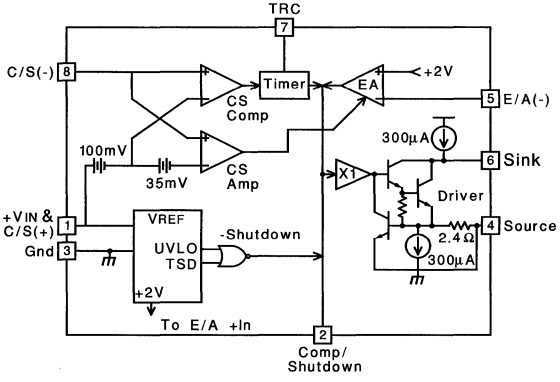
The UC1833 family includes the basic functions of this design in a low-cost, 8-pin mini-dip package, while the UC1832 series provides added versatility with the availability of 14 pins. Packaging options include plastic (N suffix), or ceramic (J suffix). Specified operating temperature ranges are: commercial (0°C to 70°C), order UC3832/3 (N or J); industrial (–25°C to 85°C), order UC2832/3 (N or J); and military (–55°C to 125°C), order UC1832/3J. Surface mount packaging is also available.

BLOCK DIAGRAMS

UCx832



UCx833



UDG-92040

ABSOLUTE MAXIMUM RATINGS

Supply Voltage +VIN 40V
Driver Output Current (Sink or Source) 450mA
Driver Sink to Source Voltage 40V
TRC Pin Voltage ..... –0.3V to 3.2V
Other Input Voltages ..... –0.3V to +VIN
Operating Junction Temperature (note 2). . . . –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

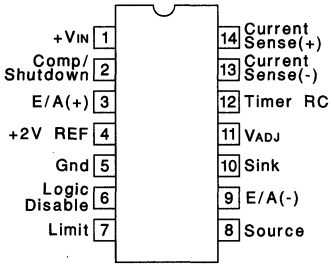
Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

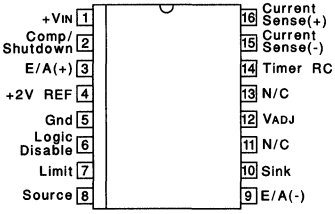
CONNECTION DIAGRAMS

UC1832

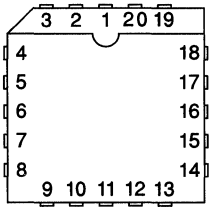
DIL-14 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



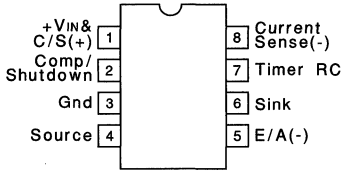
LCC-20 & PLCC-20
L & Q Package
(Top View)



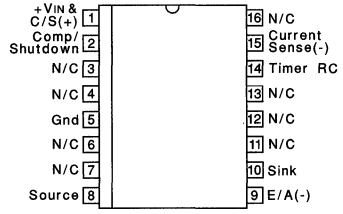
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
+VIN	2
Comp/Shutdown	3
E/A(+)	4
+2V REF	5
N/C	6
Gnd	7
Logic Disable	8
Limit	9
Source	10
N/C	11
E/A(-)	12
Sink	13
VADJ	14
N/C	15-17
Timer RC	18
Current Sense(-)	19
Current Sense(+)	20

UC1833

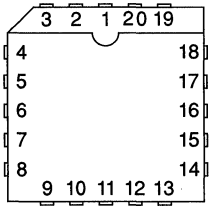
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



LCC-20 & PLCC-20
L & Q Package
(Top View)



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN & C/S(+)	1
N/C	2
N/C	3
N/C	4
Comp/Shutdown	5
Gnd	6
N/C	7
N/C	8
N/C	9
Source	10
N/C	11
E/A(-)	12
N/C	13
N/C	14
Sink	15
Timer RC	16
Current Sense(+)	17
N/C	18-20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, +V_{IN} = 15V, Driver sink = +V_{IN}, C/S(+) voltage = +V_{IN}. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	+V_{IN} = 6V		6.5	10	mA
	+V_{IN} = 36V		9.5	15	mA
	Logic Disable = 2V (UCx832 only)		3.3		mA
Reference Section					
Output Voltage (Note 3)	T_J = 25°C, I_{DRIVER} = 10mA	1.98	2.00	2.02	V
	over temperature, I_{DRIVER} = 10mA	1.96	2.00	2.04	V
Load Regulation (UCx832 only)	I_{OUT} = 0 to 10mA	-10	-5.0		mV
Line Regulation	+V_{IN} = 4.5 to 36V, I_{DRIVER} = 10mA		0.033	0.5	mV/V
Under-Voltage Lockout Threshold			3.6	4.5	V
Logic Disable Input (UCx832 only)					
Threshold Voltage		1.3	1.4	1.5	V
Input Bias Current	Logic Disable = 0V	-5.0	-1.0		µA
Current Sense Section					
Comparator Offset		95	100	105	mV
	Over Temperature	93	100	107	mV
Amplifier Offset (UCx833 only)		110	135	170	mV
Amplifier Offset (UCx832 only)	V_{ADJ} = Open	110	135	170	mV
	V_{ADJ} = 1V	180	235	290	mV
	V_{ADJ} = 0V	250	305	360	mV
Input Bias Current	V_{CM} = +V_{IN}	65	100	135	µA
Input Offset Current (UCx832 only)	V_{CM} = +V_{IN}	-10		10	µA
Amplifier CMRR (UCx832 only)	V_{CM} = 4.1V to +V_{IN}+0.3V		80		dB
Transconductance	I_{COMP} = ±100µA		65		mS
V_{ADJ} Input Current (UCx832 only)	V_{ADJ} = 0V	-10	-1		µA
Timer					
Inactive Leakage Current	C/S(+) = C/S(-) = +V_{IN}; TRC pin = 2V		0.25	1.0	µA
Active Pullup Current	C/S(+) = +V_{IN}, C/S(-) = +V_{IN} - 0.4V; TRC pin = 0V	-345	-270	-175	µA
Duty Ratio (note 4)	ontime/period, R_T = 200k, C_T = 0.27µF		4.8		%
Period (notes 4,5)	ontime + offtime, R_T = 200k, C_T = 0.27µF		36		ms
Upper Trip Threshold (Vu)			1.8		V
Lower Trip Threshold (Vl)			0.9		V
Trip Threshold Ratio	Vu/Vl		2.0		V/V
Error Amplifier					
Input Offset Voltage (UCx832 only)	V_{CM} = V_{COMP} = 2V	-8.0		8.0	mV
Input Bias Current	V_{CM} = V_{COMP} = 2V	-4.5	-1.1		µA
Input Offset Current (UCx832 only)	V_{CM} = V_{COMP} = 2V	-1.5		1.5	µA
AVOL	V_{COMP} = 1V to 13V	50	70		dB
CMRR (UCx832 only)	V_{CM} = 0V to +V_{IN} - 3V	60	80		dB
PSRR (UCx832 only)	V_{CM} = 2V, +V_{IN} = 4.5 to 36V		90		dB
Transconductance	I_{COMP} = ±10µA		4.3		mS
VOH	I_{COMP} = 0, Volts below +V_{IN}		.95	1.3	V
VOL	I_{COMP} = 0		.45	0.7	V
IOH	V_{COMP} = 2V	-700	-500	-100	µA

ELECTRICAL CHARACTERISTICS (cont.)

Unless otherwise stated, specifications hold for T_A = 0°C to 70°C for the UC3832/3, –25°C to 85°C for the UC2832/3, and –55°C to 125°C for the UC1832/3, +VIN = 15V, Driver sink = +VIN, C/S(+) voltage = +VIN. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier (cont.)					
IOL	VCOMP = 2V, C/S(-) = +VIN	100	500	700	µA
	VCOMP = 2V, C/S(-) = +VIN - 0.4V	2	6		mA
Driver					
Maximum Current	Driver Limit & Source pins common; TJ = 25°C	200	300	400	mA
	Over Temperature	100	300	450	mA
Limiting Voltage (UCx832 only)	Driver Limit to Source voltage at current limit, ISOURCE = -10mA; TJ = 25°C (Note 6)		.72		V
Internal Current Sense Resistance	TJ = 25°C (Note 6)		2.4		Ω
Pull-Up Current at Driver Sink	Compensation/Shutdown = 0.4V; Driver Sink = +VIN - 1V	-800	-300	-100	µA
	Compensation/Shutdown = 0.4V, +VIN = 36V; Driver Sink = 35V	-1000	-300	-75	µA
Pull-Down Current at Driver Source	Compensation/Shutdown = 0.4V; Driver Source = 1V	150	300	700	µA
Saturation Voltage Sink to Source	Driver Source = 0V; Driver Current = 100mA		1.5		V
Maximum Source Voltage	Driver Sink = +VIN, Driver Current = 100mA Volts below +VIN		3.0		V
UVLO Sink Leakage	+VIN = C/S(+) = C/S(-) = 2.5V, Driver Sink = 15V, Driver Source = 0V, TA = 25°C		25		µA
Maximum Reverse Source Voltage	Compensation/Shutdown = 0V; ISOURCE = 100µA, +VIN = 3V		1.6		V
Thermal Shutdown			160		°C

Note 3: *On the UCx833 this voltage is defined as the regulating level at the error amplifier inverting input, with the error amplifier driving V_{SOURCE} to 2V.*

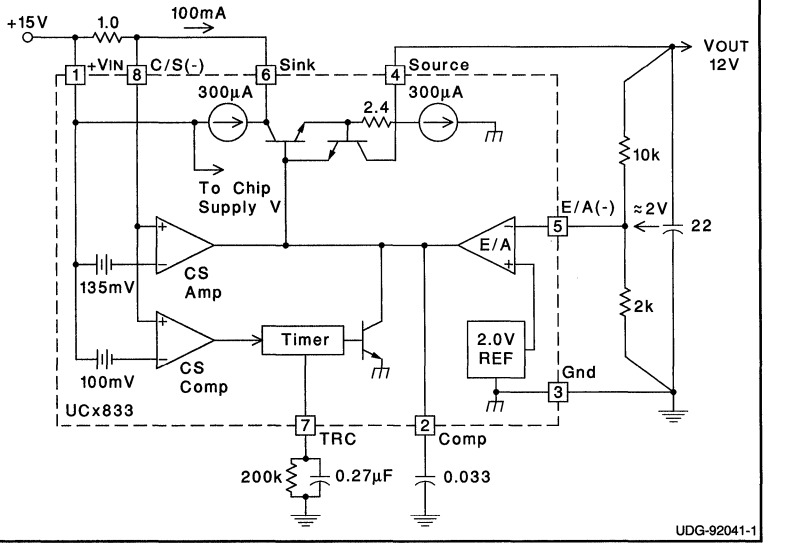
Note 4: *These parameters are first-order supply-independent, however both may vary with supply for $+V_{IN}$ less than about 4V. This supply variation will cause a slight change in the timer period and duty cycle, although a high off-time/on-time ratio will be maintained.*

Note 5: *With recommended R_T value of 200k, $T_{OFF} \bullet R_T C_T * ln(Vu/Vl) \pm 10\%$.*

Note 6: *The internal current limiting voltage has a temperature dependence of approximately -2.0mV/°C, or -2800ppm/°C. The internal 2.4 Ω sense resistor has a temperature dependance of approximately +1500ppm/°C.*

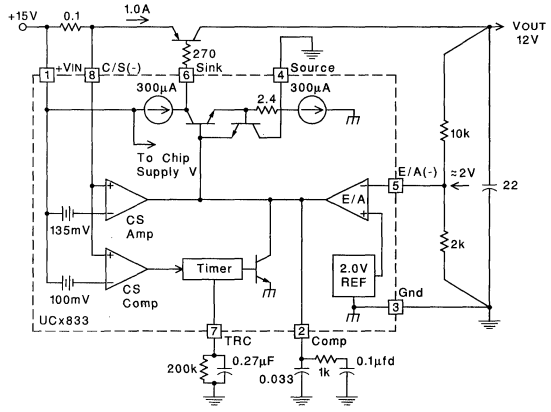
APPLICATION AND OPERATION INFORMATION

NPN Pass (Local 100mA Regulator) (UCx833)



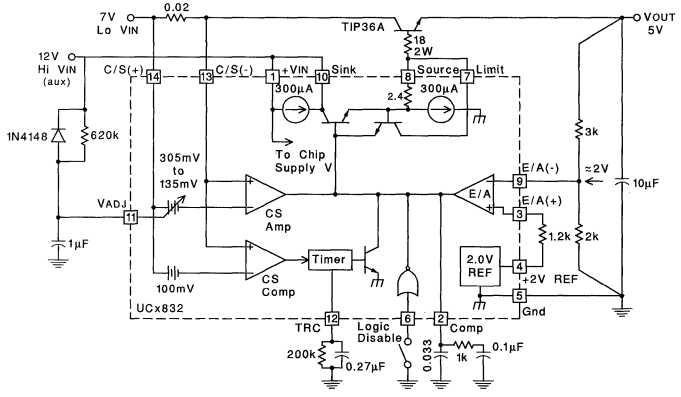
APPLICATION AND OPERATION INFORMATION (cont.)

PNP Pass (Low Drop-Out Regulator) (UCx833)



UDG-92042-1

NPN Pass (Medium Power, Low Drop-Out Regulator) (UCx832)



UDG-92043-1

Estimating Maximum Load Capacitance

For any power supply, the rate at which the total output capacitance can be charged depends on the maximum output current available and on the nature of the load. For a constant-current current-limited power supply, the output will come up if the load asks for less than the maximum available short-circuit limit current.

To guarantee recovery of a duty-ratio current-limited power supply from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit ON time. The design value of ON time can be adjusted by changing the timing capacitor. Nominally, $T_{ON} = 0.693 \times 10k \times C_T$.

Typically, the IC regulates output current to a maximum of $I_{MAX} = K \times I_{TH}$, where I_{TH} is the timer trip-point current,

and $K = \dfrac{Current\ Sense\ Amplifier\ Offset\ Voltage}{100mA}$

≈1.35 for UCx833, and is variable from 1.35 to 3.05 with V_{ADJ} for the UCx832.

For a worst-case constant-current load of value just less than I_{TH}, C_{MAX} can be estimated from:

$$C_{MAX} = ((K-1)I_{TH})\left(\frac{T_{ON}}{V_{OUT}}\right),$$

where V_{OUT} is the nominal regulator output voltage.

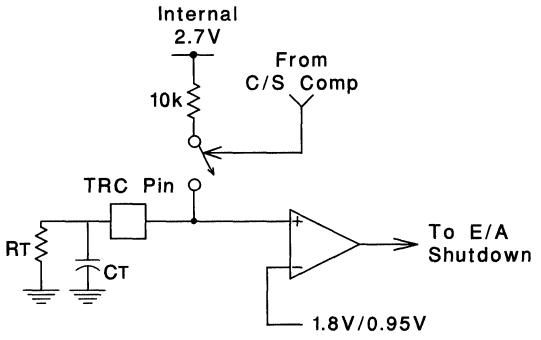
For a resistive load of value R_L, the value of C_{MAX} can be estimated from:

$$C_{MAX} = \frac{T_{ON}}{R_L} \bullet \frac{1}{I_N\left[\left(1 - \frac{V_{OUT}}{K \bullet I_{TH} \bullet R_L}\right)^{-1}\right]}$$

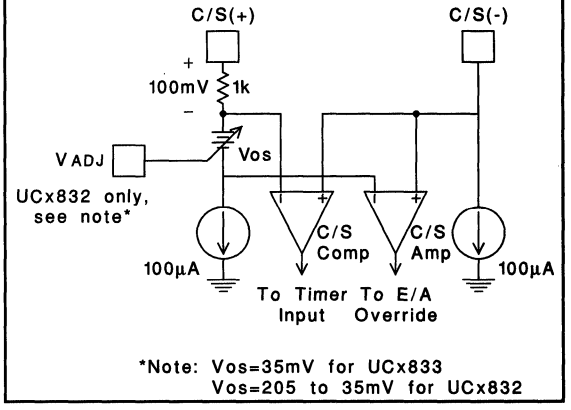
APPLICATION AND OPERATION INFORMATION (cont.)

Current Sense Amplifier Offset Voltage vs VADJ

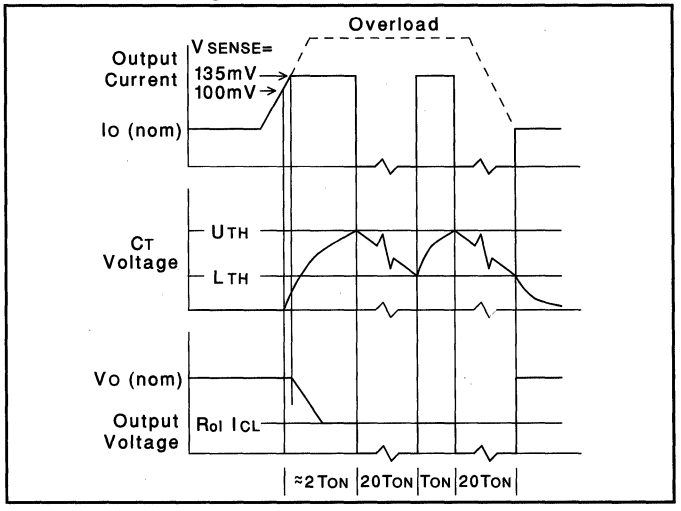
UCx832/33 Timer Function



UCx832/33 Current Sense Input Configuration



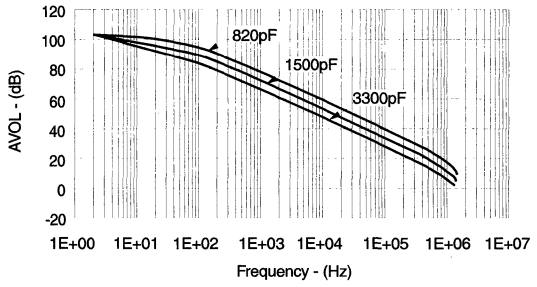
Load current, timing capacitor voltage, and output voltage of the regulator under fault conditions.



APPLICATION AND OPERATION INFORMATION (cont.)

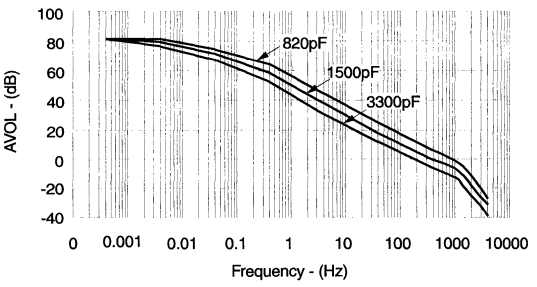
UCx832 Error Amplifier

AVOL vs Frequency and Cc



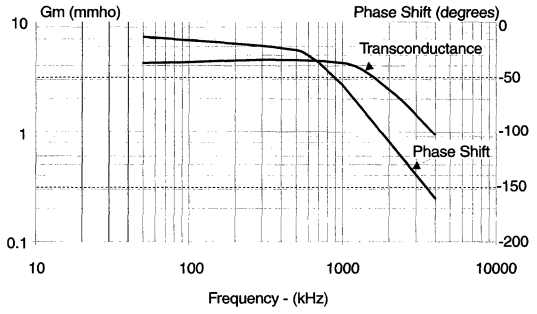
UCx832 Current Sense Amplifier

AVOL vs Frequency and Cc



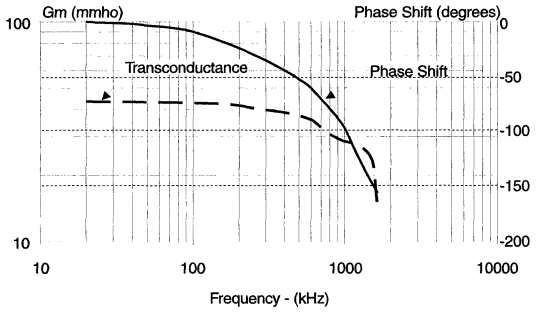
UCx832 Error Amplifier

Transconductance and Phase vs Frequency



UCx832 Current Sense Amplifier

Transconductance and Phase vs Frequency



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UNITRODE

application INFO available

UC1834
UC2834
UC3834

High Efficiency Linear Regulator

FEATURES

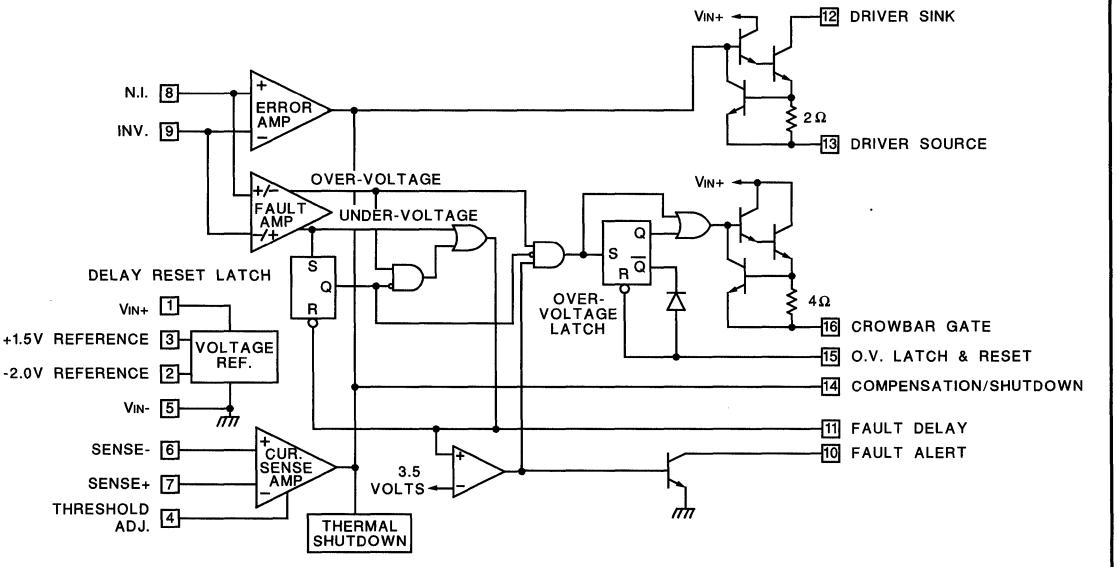
- Minimum VIN - VOUT Less Than 0.5V At 5A Load With External Pass Device
- Equally Usable For Either Positive or Negative Regulator Design
- Adjustable Low Threshold Current Sense Amplifier
- Under And Over-Voltage Fault Alert With Programmable Delay
- Over-Voltage Fault Latch With 100mA Crowbar Drive Output

DESCRIPTION

The UC1834 family of integrated circuits is optimized for the design of low input-output differential linear regulators. A high gain amplifier and 200mA sink or source drive outputs facilitate high output current designs which use an external pass device. With both positive and negative precision references, either polarity of regulator can be implemented. A current sense amplifier with a low, adjustable, threshold can be used to sense and limit currents in either the positive or negative supply lines.

In addition, this series of parts has a fault monitoring circuit which senses both under and over-voltage fault conditions. After a user defined delay for transient rejection, this circuitry provides a fault alert output for either fault condition. In the over-voltage case, a 100mA crowbar output is activated. An over-voltage latch will maintain the crowbar output and can be used to shutdown the driver outputs. System control to the device can be accommodated at a single input which will act as both a supply reset and remote shutdown terminal. These die are protected against excessive power dissipation by an internal thermal shutdown function.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, V_{IN} + ... 40V
Driver Current 400mA
Driver Source to Sink Voltage 40V
Crowbar Current ..... –200mA
+1.5V Reference Output Current ..... –10mA
Fault Alert Voltage 40V
Fault Alert Current 15mA
Error Amplifier Inputs ..... –0.5V to 35V
Current Sense Inputs ..... –0.5V to 40V
O.V. Latch Output Voltage ..... –0.5V to 40V
O.V. Latch Output Current 15mA

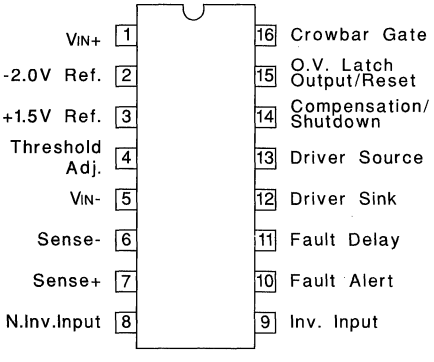
Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C 2000mW
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... 300°C

Note 1: Voltages are reference to V_{IN}–, Pin 5.
Currents are positive into, negative out of the specified terminals.
Consult Packaging section of Databook for thermal limitations and considerations of package.

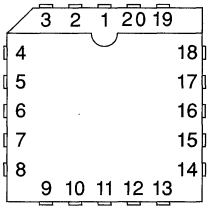
5

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
V_{IN} +	2
-2.0V REF	3
+1.5V REF	4
Threshold Adjust	5
N/C	6
V_{IN}–	7
Sense–	8
Sense+	9
N.Inv. Input	10
N/C	11
Inv. Input	12
Fault Alert	13
Fault Delay	14
Driver Sink	15
N/C	16
Driver Source	17
Compensation/ Shutdown	18
O.V. Latch Output/Reset	19
Crowbar Gate	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A=–55°C to +125°C for the UC1834, –40°C to +85°C for the UC2834, and 0°C to +70°C for the UC3834. V_{IN+} = 15V, V_{IN-} = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Turn-on Characteristics								
Standby Supply Current			5.5	7		5.5	10	mA
+1.5 Volt Reference								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	1.47		1.53	1.455		1.545	
Line Regulation	V_{IN+} = 5 to 35V		1	10		1	15	mV
Load Regulation	I_{OUT} = 0 to 2mA		1	10		1	15	mV
-2.0 Volt Reference (Note 2)								
Output Voltage (Referenced to V_{IN^+})	T_J = 25°C	–2.04	–2	–1.96	–2.06	–2	–1.94	V
	$T_{J(MIN)} \le T_J \le T_{J(MAX)}$	–2.06		–1.94	–2.08		–1.92	
Line Regulation	V_{IN+} = 5 to 35V		1.5	15		1.5	20	mV
Output Impedance			2.3			2.3		kΩ
Error Amplifier Section								
Input Offset Voltage	V_{CM} = 1.5V		1	6		1	10	mV
Input Bias Current	V_{CM} = 1.5V		–1	–4		–1	–8	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain	Output @ Pin 14, Pin 12 = V_{IN+} Pin 13, 20Ω to V_{IN-}	50	65		50	65		dB
CMRR	V_{CM} = 0.5 to 33V, V_{IN+} = 35V	60	80		60	80		dB
PSRR	V_{IN+} = 5 to 35V, V_{CM} = 1.5V	70	100		70	100		dB
Driver Section								
Maximum Output Current		200	350		200	350		mA
Saturation Voltage	I_{OUT} = 100mA		0.5	1.2		0.5	1.5	V
Output Leakage Current	Pin 12 = 35V, Pin 13 = V_{IN-}, Pin 14 = V_{IN-}		0.1	50		0.1	50	µA
Shutdown Input Voltage at Pin 14	$I_{OUT} \le$ 100µA, Pin 13 = V_{IN-}, Pin 12 = V_{IN+}	0.4	1		0.4	1		V
Shutdown Input Current at Pin 14	Pin 14 = V_{IN-}, Pin 12 = V_{IN+} $I_{OUT} \le$ 100µA, Pin 13 = V_{IN-}		–100	–150		–100	–150	µA
Thermal Shutdown (Note 3)			165			165		°C
Fault Amplifier Section								
Under- and Over-Voltage Fault Threshold	V_{CM} = 1.5V, @ E/A Inputs	120	150	180	110	150	190	mV
Common Mode Sensitivity	V_{IN+} = 35V, V_{CM} = 1.5 to 33V		–0.4	–0.8		–0.4	–1.0	%/v
Supply Sensitivity	V_{CM} = 1.5V, V_{IN+} = 5 to 35V		–0.5	–1.0		–0.5	–1.2	%/V
Fault Delay		30	45	60	30	45	60	ms/µF
Fault Alert Output Current		2	5		2	5		mA
Fault Alert Saturation Voltage	I_{OUT} = 1mA		0.2	0.5		0.2	0.5	V
O.V. Latch Output Current		2	4		2	4		mA
O.V. Latch Saturation Voltage	I_{OUT} = 1mA		1.0	1.3		1.0	1.3	V
O.V. Latch Output Reset Voltage		0.3	0.4	0.6	0.3	0.4	0.6	V
Crowbar Gate Current		–100	–175		–100	–175		mA
Crowbar Gate Leakage Current	V_{IN+} = 35V, Pin 16 = V_{IN-}		–0.5	–50		–0.5	–50	µA

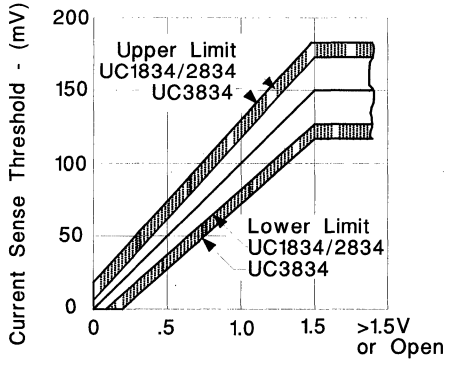
Note 2: When using both the 1.5V and –2.0V references the current out of pin 3 should be balanced by an equivalent current into Pin 2. The –2.0V output will change –2.3mV per µA of imbalance.

Note 3: Thermal shutdown turns off the driver. If Pin 15 (O.V. Latch Output) is tied to Pin 14 (Compensation/Shutdown) the O.V. Latch will be reset.

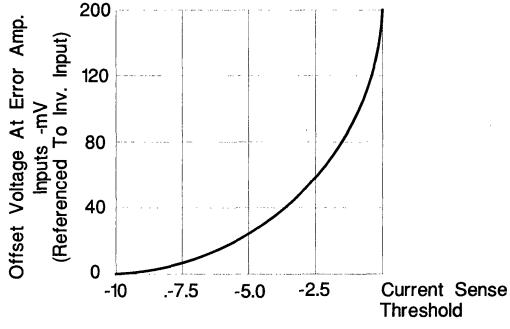
ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, these specifications apply for T_A=–55°C to +125°C for the UC1834, –40°C to +85°C for the UC2834, and 0°C to +70°C for the UC3834. V_{IN+} = 15V, V_{IN-} = 0V, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1834 UC2834			UC3834			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Current Sense Amplifier Section								
Threshold Voltage	Pin 4 Open, V_{CM} = V_{IN+} or V_{IN-}	130	150	170	120	150	180	mV
	Pin 4 = 0.5V, V_{CM} = V_{IN+} or V_{IN-}	40	50	60	30	50	70	
Threshold Supply Sensitivity	Pin 4 Open, V_{CM} = V_{IN-}, V_{IN+} = 5 to 35V		–0.1	–0.3		–0.1	–0.5	%/V
Adj. Input Current	Pin 4 = 0.5V		–2	–10		–2	–10	µA
Sense Input Bias Current	V_{CM} = V_{IN+}		100	200		100	200	µA
	V_{CM} = V_{IN-}		–100	–200		–100	–200	

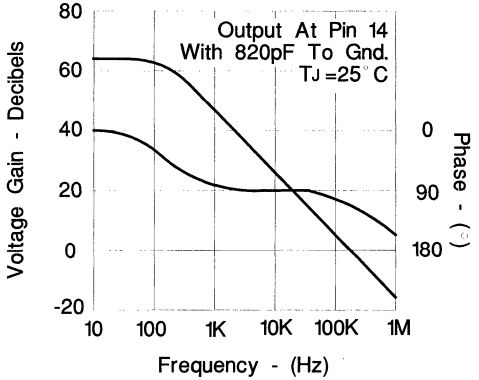
Current Sense Threshold Adjustment



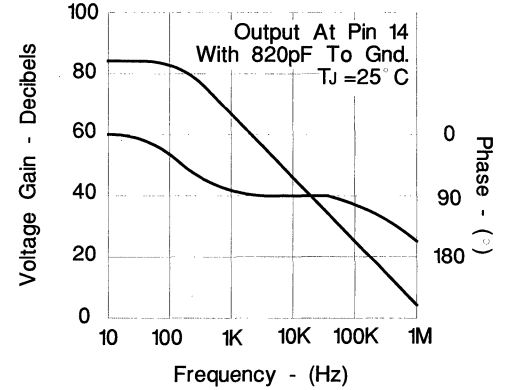
Current Limiting Knee Characteristics



Error Amplifier Gain and Phase Frequency Response

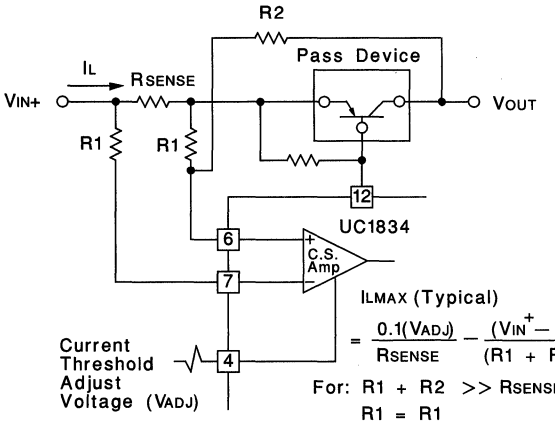


Current Sense Amplifier Gain and Phase Frequency Response



APPLICATION INFORMATION

Foldback Current Limiting



$$I_{LMAX}\ (Typical) = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN}^{+} - V_{OUT})\ R1}{(R1 + R2)\ R_{SENSE}},$$

For: $R1 + R2 >> R_{SENSE}$, $V_{ADJ} \leq 1.5V$, $R1 = R1$

Both the current sense and error amplifiers on the UC1834 are transconductance type amplifiers. As a result, their voltage gain is a direct function of the load impedance at their shared output pin, Pin 14. Their small signal voltage gain as a function of load and frequency is nominally given by;

$$A_{V\ E/A} = \frac{Z_L(f)}{700\Omega} \text{ and } A_{V\ C.S./A} = \frac{Z_L(f)}{70\Omega}$$

for: $f \leq 500kHz$ and $|Z_{L(f)}| \leq 1\ M\Omega$

Where:

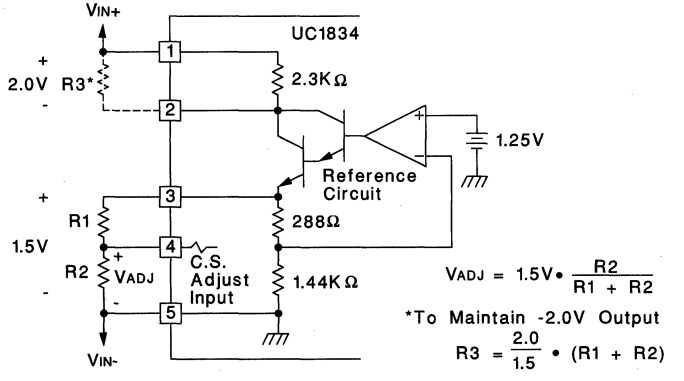
A_V=Small Signal Voltage Gain to pin 14.

$Z_L(f)$ = Load Impedance at Pin 14.

The UC1834 fault delay circuitry prevents the fault outputs from responding to transient fault conditions. The delay reset latch insures that the full, user defined, delay passes before an over-voltage fault response occurs. This prevents unnecessary crowbar, or latched-off conditions, from occurring following sharp under-voltage to over-voltage transients.

The crowbar output on the UC1834 is activated following a sustained over-voltage condition. The crowbar output remains high as long as the fault condition persists, or, as long as the over-voltage latch is set. The latch is set with an over-voltage fault if the voltage at Pin 15 is above the latch reset threshold, typically 0.4V. When the latch is set, its Q– output will pull Pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents Q– from pulling Pin 15 below the reset threshold. However, Pin 15 is pulled low enough to disable the driver outputs if Pins 15 and 14 are tied together. With Pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and Pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

Setting the Threshold Adjust Voltage (VADJ)



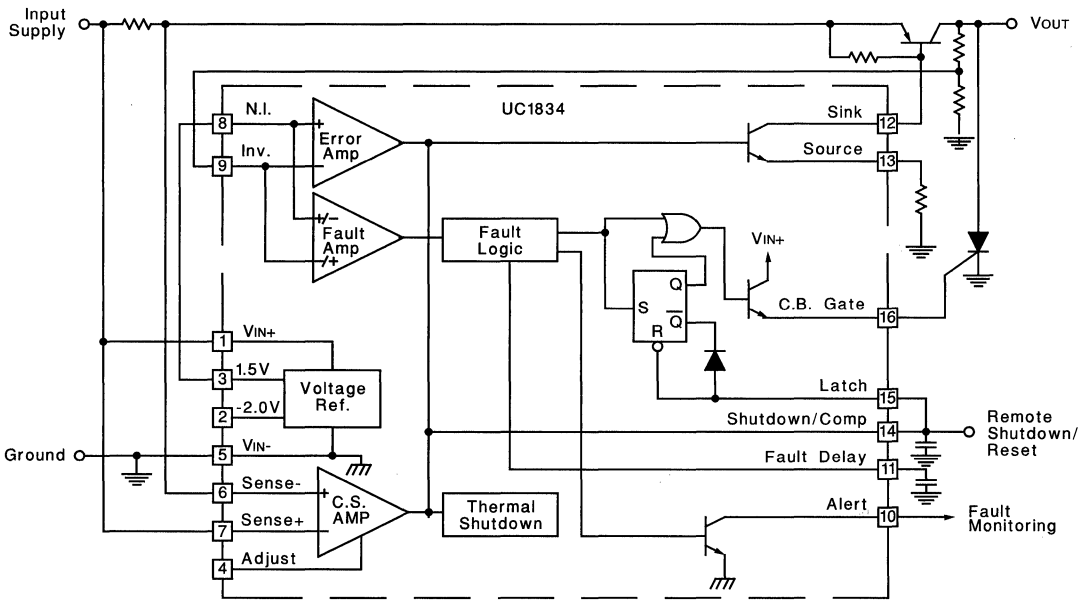
$$V_{ADJ} = 1.5V \bullet \frac{R2}{R1 + R2}$$

*To Maintain -2.0V Output

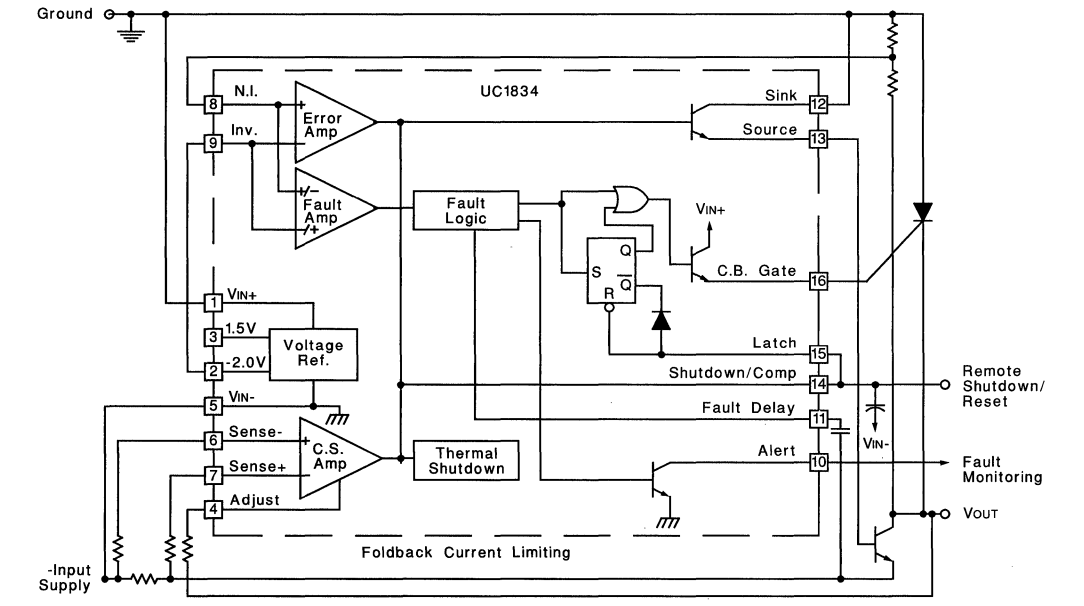
$$R3 = \frac{2.0}{1.5} \bullet (R1 + R2)$$

TYPICAL APPLICATIONS

5-10 Amp Positive Regulator



5-10 Amp Negative Regulator



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High Efficiency Regulator Controller

FEATURES

- Complete Control for a High Current, Low Dropout, Linear Regulator
- Fixed 5V or Adjustable Output Voltage
- Accurate 2.5A Current Limiting with Foldback
- Internal Current Sense Resistor
- Remote Sense for Improved Load Regulation
- External Shutdown
- Under-Voltage Lockout and Reverse Voltage Protection
- Thermal Shutdown Protection
- 8 Pin Mini-Dip Package (Surface Mount also Available)

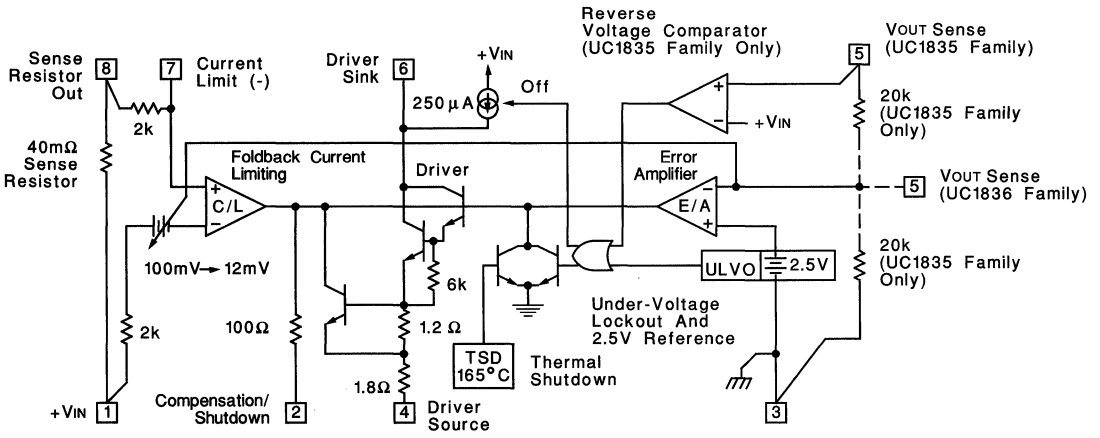
DESCRIPTION

The UC1835/6 families of linear controllers are optimized for the design of low cost, low dropout, linear regulators. Using an external pass element, dropout voltages of less than 0.5V are readily obtained. These devices contain a high gain error amplifier, a 250mA output driver, and a precision reference. In addition, current sense with foldback provides for a 2.5A peak output current dropping to less than 0.5A at short circuit.

These devices are available in fixed, 5V, (UC1835), or adjustable, (UC1836), versions. In the fixed 5 volt version, the only external parts required are an external pass element, an output capacitor, and a compensation capacitor. On the adjustable version the output voltage can be set anywhere from 2.5V to 35V with two external resistors.

Additional features of these devices include under-voltage lockout for predictable start-up, thermal shutdown and short circuit current limiting to protect the driver device. On the fixed voltage version, a reverse voltage comparator minimizes reverse load current in the event of a negative input to output differential.

BLOCK DIAGRAM



Note: Pin numbers refer to 8-Pin DIL Package

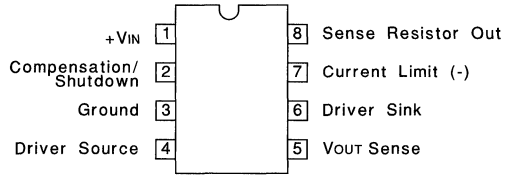
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (+VIN) . . . . . –1.0V to + 40V
Driver Output Current (Sink or Source) 600mA
Driver Source to Sink Voltage . . . . . + 40V
Maximum Current Through Sense Resistor. 4A
VOUT Sense Input Voltage . . . . . –.3V to + 40V
Power Dissipation at TA = 25°C (Note 2) 1000mW
Power Dissipation at TC = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

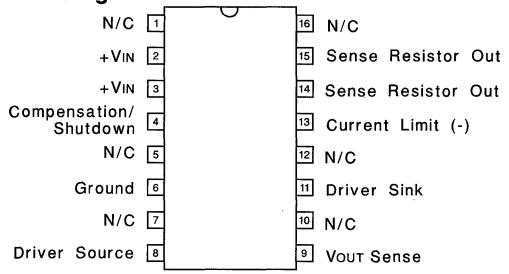
Note 1: Voltages are referenced to ground, (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal considerations and limitations of packages.

CONNECTION DIAGRAMS

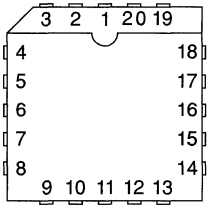
DIL-8, SOIC-8 (TOP VIEW)
N or J Package, D Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
+VIN	2
+VIN	3
N/C	4
Compensation/ Shutdown	5
N/C	6
Ground	7
N/C	8
N/C	9
Driver Source	10
N/C	11
VOUT Sense	12
N/C	13
N/C	14
Driver Sink	15
N/C	16
Current Limit (-)	17
N/C	18
Sense Resistor Out	19
Sense Resistor Out	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +VIN = 6V, Driver Source= 0V, Driver Sink = 5V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 6V		2.75	4.0	mA
	+VIN = 40V		3.75	6.0	mA
UVLO Threshold	+VIN Low to High, VOUT Sense = 0V	3.9	4.4	4.9	V
Threshold Hysteresis			0.1	0.35	V
Reverse Current	+VIN = -1.0V, Driver Sink Open		6.0	20	mA
Regulating Voltage and Error Amplifier (UC1835 Family Only)					
Regulating Level at VOUT Sense (VREG)	Driver Current = 10mA, TJ = 25°C	4.94	5.0	5.06	V
	Over Temperature	4.9		5.1	V
Line Regulation	+VIN = 5.2V + 35V		15	40	mV
Load Regulation	Driver Current = 0 to 250mA		6.0	25	mV
Bias Current at VOUT Sense	VOUT Sense = 5.0V	75	125	210	µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA

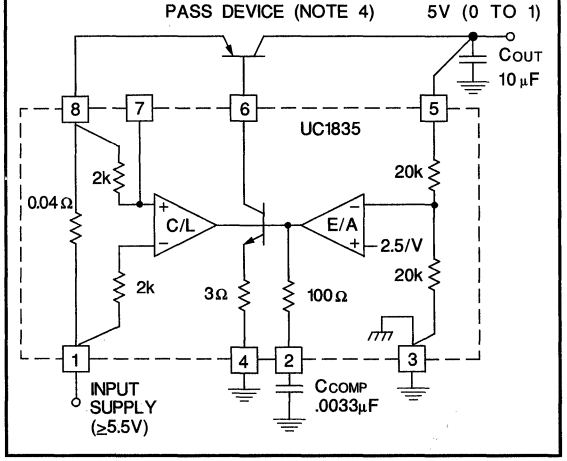
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to + 70°C for the UC3835/6, –25°C to + 85°C for the UC2835/6, and –55°C to +125°C for the UC1835/6, +V_{IN} = 6V, Driver Source= 0V, Driver Sink = 5V, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Regulating Voltage and Error Amplifier (UC1836 Family Only)					
Regulating Level at V_{OUT} Sense (V_{REG})	Driver Current = 10mA, T_J = 25°C	2.47	2.5	2.53	V
	Over Temperature	2.45		2.55	V
Line Regulation	+V_{IN} = 5.2V to 35V		6.0	20	mV
Load Regulation	Driver Current = 0 to 250mA		3.0	15	mV
Bias Current at V_{OUT} Sense	V_{OUT} Sense =2.5V	-1.0	-0.2		µA
Error Amp Transconductance	±100µA at Compensation/Shutdown Pin	0.8	1.3	2.0	mS
Maximum Compensation Output Current	Sink or Source, Driver Source Open	90	200	260	µA
Driver					
Maximum Current		250	500		mA
Saturation Voltage	Driver Current = 250mA, Driver Sink		2.0	2.8	V
Pull-Up Current at Driver Sink	Compensation/Shutdown=0.45V	140	250	300	µA
Driver Sink Leakage	In UVLO			10	µA
	In Reverse Voltage (UC1835 Family Only)			10	µA
Thermal Shutdown			165		°C
Foldback Current Limit					
Current Limit Levels at Sense Resistor Out	V_{OUT} Sense = (0.99) V_{REG}	2.2	2.5	2.8	A
	V_{OUT} Sense = (0.5) V_{REG}	1.3	1.5	1.7	A
	V_{OUT} Sense = 0V	0.25	0.4	0.55	A
Current Limit Amp Tansconductance	±100µA at Compensation/Shutdown, V_{OUT} Sense = (0.9) V_{REG}	12	24	42	mS
Limiting Voltage at Current Limit (-) (Note 2)	V_{OUT} Sense = (0.9) V_{REG} Volts Below +V_{IN}, T_J = 25°C	80	100	140	mV
Sense Resistor Value (Note 3)	V_{OUT} Sense = (0.9) V_{REG}, I_{OUT} = I_A, T_J = 25°C		40		mΩ

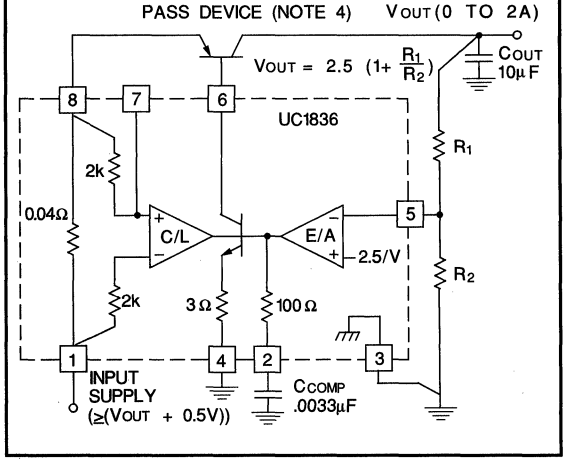
Note 2: This voltage has a positive temperature coefficient of approximately 3500ppm/°C.
Note 3: This resistance has a positive temperature coefficient of approximately 3500ppm/°C. The total resistance from Pin 1 to Pin 8 will include an additional 60 to 100mΩ of package resistance.

APPLICATION AND OPERATION INFORMATION

UC 1835 – Typical configurations for a 2A, Low Dropout 5V Regulator



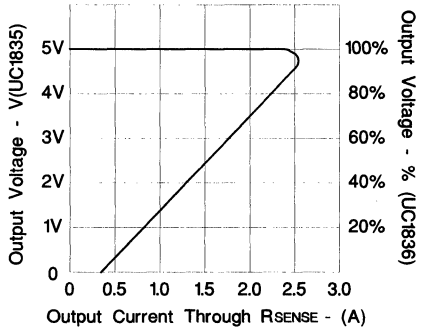
UC1836 – Typical Configuration for a 2A, Low Dropout Adjustable Regulator



Note 4: Suggested Pass devices are TIP 32B. (Dropout Voltage ≤0.75V) or, D45H, (Dropout Voltage ≤0.5V), or equivalents.

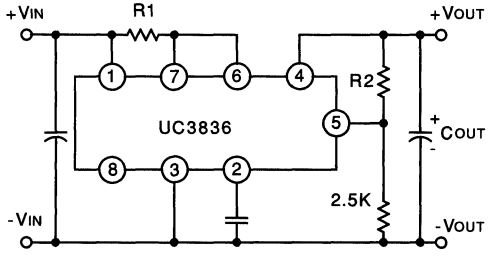
APPLICATION AND OPERATION INFORMATION (cont.)

UC1835/6 Foldback Current Limiting



UC3835/36 TYPICAL APPLICATIONS

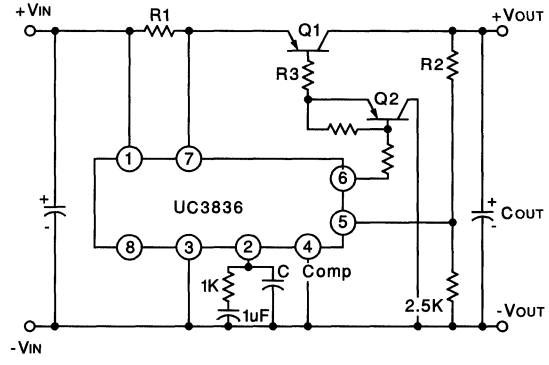
Low Current Application
using the UC3836 internal drive transistor



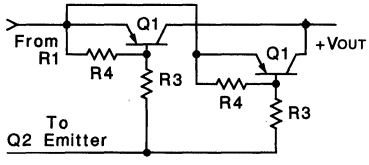
Typical Output Current vs VIN and VOUT
of the UC3836 internal drive transistor
for PDISS = 0.5W (approx.)

		VIN					
	Volts	5	9	12	15	18	24
VOUT	2	150	60	40	30	20	12
	5		105	55	35	25	15
	9			130	60	35	20
	12				120	55	25
	15	Current in mA				110	30

High Current Application
using drive transistor Q2 to increase Q1 base drive
and reduce UC3836 power dissipation



Parallel Pass Transistors
can be added for high current or
high power dissipation applications



EQUATIONS:
R1 = 0.100 V/IOUT (MAX)
R2 = (VOUT - 2.5V)/1mA
R3 = ((VIN - VBE - VSAT)*BETA(min))/IOUT (max)

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8-Pin N-FET Linear Regulator Controller

PRELIMINARY

FEATURES

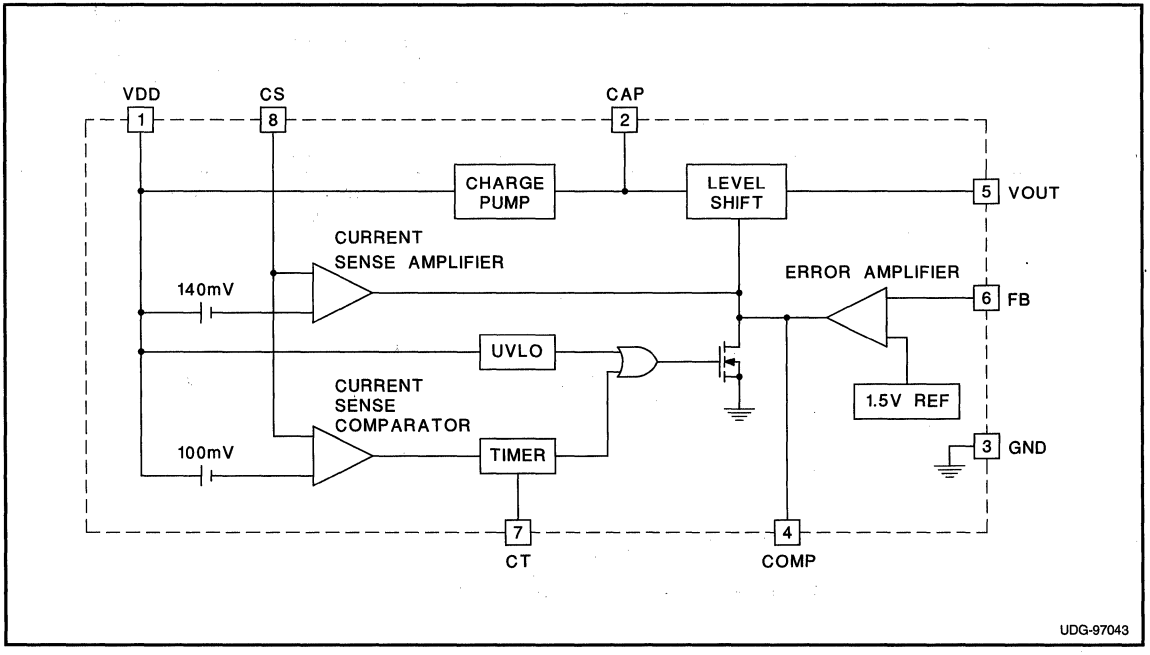
- On Board Charge Pump to Drive External N-MOSFET
- Input Voltage as Low as 3V
- Duty Ratio Mode Over Current Protection
- Extremely Low Dropout Voltage
- Low External Parts Count
- Output Voltages as Low as 1.5V

DESCRIPTION

The UCC3837 Linear Regulator Controller includes all the features required for an extremely low dropout linear regulator that uses an external N-channel MOSFET as the pass transistor. The device can operate from input voltages as low as 3V and can provide high current levels, thus providing an efficient linear solution for custom processor voltages, bus termination voltages, and other logic level voltages below 3V. The on board charge pump creates a gate drive voltage capable of driving an external N-MOSFET which is optimal for low dropout voltage and high efficiency. The wide versatility of this IC allows the user to optimize the setting of both current limit and output voltage for applications beyond or between standard 3-terminal linear regulator ranges.

This 8-pin controller IC features a duty ratio current limiting technique that provides peak transient loading capability while limiting the average power dissipation of the pass transistor during fault conditions. See the Application Section for detailed information.

BLOCK DIAGRAM



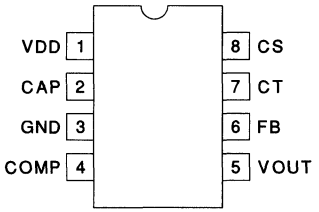
ABSOLUTE MAXIMUM RATINGS

All pins referenced to GND. . . . . –0.3V to +15V
CS, CT, FB . . . . . –0.3V to VDD + 0.3V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to 125°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current	VDD = 5V		1	1.5	mA
	VDD = 10V		1.2	2	mA
Under Voltage Lockout					
Minimum Voltage to Start		2.2	2.65	3	V
Minimum Voltage After Start		1.8	2.2	2.6	V
Hysteresis		0.25	0.45	0.65	V
Reference (Note 1)					
V_{REF}	25°C	1.485	1.5	1.515	V
	0°C to 70°C	1.470	1.5	1.530	V
	–55°C to 125°C	1.455	1.5	1.545	V
Current Sense					
Comparator Offset	0°C to 70°C	90	100	110	mV
Comparator Offset	–55°C to 125°C	85	100	115	mV
Amplifier Offset		120	140	160	mV
Input Bias Current	V_{CS} = 5V		0.5	5	µA
Current Fault Timer					
CT Charge Current	V_{CT} = 1V	16	36	56	µA
CT Discharge Current	V_{CT} = 1V	0.5	1.2	1.9	µA
CT Fault Low Threshold		0.4	0.5	0.6	V
CT Fault Hi Threshold		1.3	1.5	1.7	V
Fault Duty Cycle		2	3.3	5	%
Error Amplifier					
Input Bias Current			0.5	2	µA
Open Loop Gain		60	90		dB
Transconductance	–10µA to 10µA	2	5	8	mMho
Charge Current	V_{COMP} = 6V	20	40	60	µA
Discharge Current	V_{COMP} = 6V	10	25	40	µA
FET Driver					
Peak Output Current	V_{CAP} = 10V, VOUT = 1V	0.5	1.5	2.5	mA
Average Output Current	VOUT = 1V	25	100	175	µA
Max Output Voltage	V_{IN} = 4.5V, I_{OUT} = 0µA	8.4	9.7		V
	V_{IN} = 4.5V, I_{OUT} = 10µA, 0°C to 70°C	8	9		V
	V_{IN} = 4.5V, I_{OUT} = 10µA, –55°C to 125°C	7.5	9		V

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, T_A = –55°C to 12°C for the UCC1837, –25°C to 85°C for the UCC2837 and 0°C to 70°C for UCC3837; VDD = 5V, C_T = 10nF, C_{CAP} = 100nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump					
CAP Voltage	V_{IN} = 4.5V, C/S = 0V	11	12.5		V
	V_{IN} = 12V, C/S = 0V		15	16.5	V

Note 1: This is defined as the voltage on FB which results in a DC voltage of 8V on VOUT.

PIN DESCRIPTIONS

CAP: The output of the charge pump circuit. A capacitor is connected between this pin and GND to provide a floating bias voltage for an N-Channel MOSFET gate drive. A minimum of a 0.01µF ceramic capacitor is recommended. CAP can be directly connected to an external regulated source such as +12V, in which case the external voltage will be the source for driving the N-Channel MOSFET.

COMP: The output of the transconductance error amplifier and current sense amplifier. Used for compensating the small signal characteristics of the voltage loop (and current loop when Current Sense Amplifier is active in over curret mode).

CS: The negative current sense input signal. This pin should be connected through a low noise path to the low side of the current sense resistor.

CT: The input to the duty cycle timer circuit. A capacitor is connected from this pin to GND, setting the maximum ON time of the over current protection circuits. See the Application Section for programming instructions.

FB: The inverting terminal of the voltage error amplifier, used to feedback the output voltage for comparison with the internal reference voltage. The nominal DC operating voltage at this pin is 1.5V

GND: Ground reference for the device. For accurate output voltage regulation, GND should be referenced to the output load ground.

VDD: The system input voltage is connected to this point. VDD must be above 3V. VDD also acts as one side of the Current Sense Amplifier and Comparator.

VOUT: This pin directly drives the gate of the external N-MOSFET pass element. The typical output impedance of this pin is 6.5kΩ.

APPLICATION INFORMATION

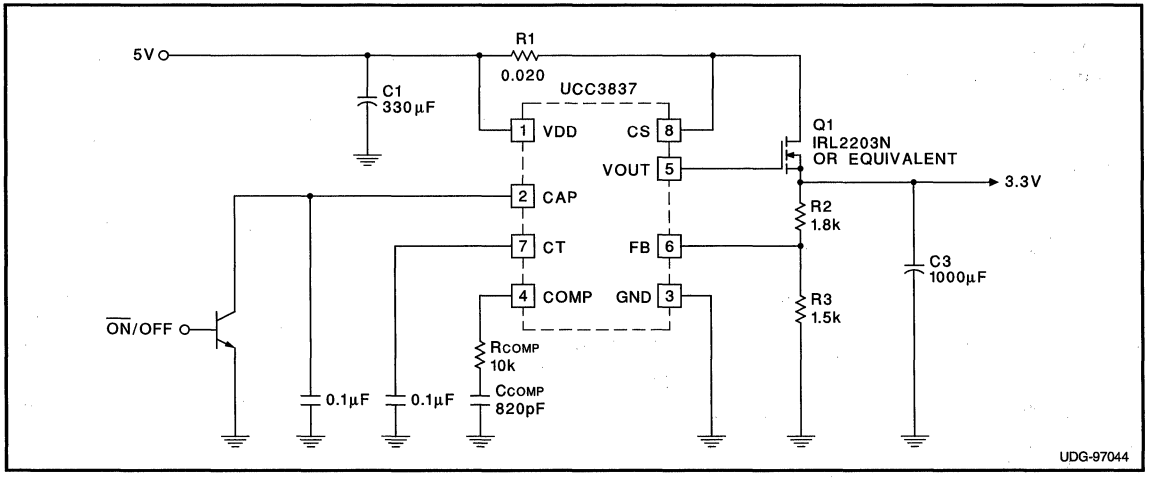


Figure 1. Typical Application 5V to 3.3V, 5A Regulator

Topology and General Operation

Unitrode Application Note U-152 is a detailed design of a low dropout linear regulator using an N-Channel MOSFET as a pass element, and should be used as a guide for understanding the operation of the circuit shown in Figure 1.

APPLICATION INFORMATION (cont.)

Charge Pump Operation

The internal charge pump of the UCC3837 is designed to create a voltage equal to 3 times the input VDD voltage at the CAP pin. There is an internal 5V clamp at the input of the charge pump however that insures the voltage at CAP does not exceed the ratings of the IC. This CAP voltage is used to provide gate drive current to the external pass element as well as bias current to internal sections of the UCC3837 itself. The charge pump output has a typical impedance of 80kΩ and therefore the loading of the IC and the external gate drive reduces the voltage from its ideal level. The UCC3837 can operate in several states including having the error amplifier disabled (shut down), in normal linear regulation mode, and in overdrive mode where the linear regulator is responding to a transient load or line condition. The maximum output voltage available at VOUT is shown in Figure 2 for these various modes of operation.

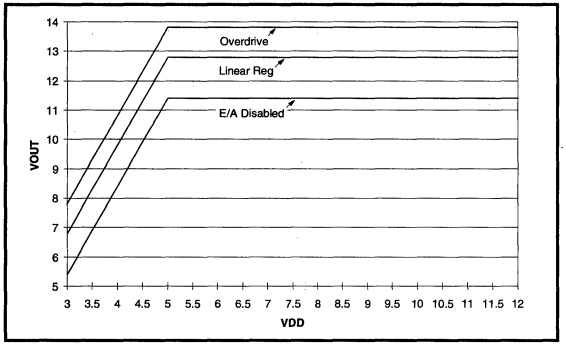


Figure 2. Typical V_{OUTMAX} vs. VDD

The charge pump output is designed to supply 10μA of average current to the load which is typically the MOSFET gate capacitance present at the VOUT pin. The capacitor value used at CAP is chosen to provide holdup of the CAP voltage should the external load exceed the average current, which occurs during load and line transient conditions. The value of CAP also determines the startup time of the linear regulator. The voltage at CAP charges up with a time constant determined by the charge pump output impedance (typically 80kΩ) and the value of the capacitor on CAP.

An external voltage such as +12V may be tied to the CAP pin directly to insure a higher value of VOUT, which may be useful when a standard level MOSFET is used or when VDD is very low and the resulting VOUT voltage may need to be higher. With an external source applied to CAP, the maximum voltage at VOUT will be approximately 1V below the external source. The external +12V source should be decoupled to GND using a minimum of a 0.01μF capacitor.

Choosing a Pass Element

The UCC3837 is designed for use with an N-Channel MOSFET pass element only. The designer may choose a logic level or standard gate level MOSFET depending on the input voltage, the required gate drive, and the available voltage at VOUT as discussed previously. MOSFET selection should be based on required dropout voltage and gate drive characteristics. A lower R_{DSON} MOSFET is used when low dropout is required, but this type of MOSFET will have higher gate capacitance which may result in a slower transient response.

A MOSFET used in linear regulation is typically operated at a gate voltage between the threshold voltage and the gate plateau voltage in order to maintain high gain. This mode of operation is linear, and therefore the channel resistance is higher than the manufacturer's published R_{DSON} value. The MOSFET should only be operated in the non-linear (switch) mode under transient conditions, when minimum dropout voltage is required.

Disabling the UCC3837

Grounding the CAP pin will remove the drive voltage and effectively disable the output voltage. The device used to short the output of CAP should have a very low leakage current when in the OPEN state, since even a few microamps will lower the charge pump voltage.

A second method of disabling the UCC3837 is to place a short circuit across C_{COMP}. This will have an advantage of a quicker restart time as the voltage at CAP will not be completely discharged. The charge pump will be loaded down by the typical 40μA charging current of the error amplifier with this configuration, resulting in a lower voltage at CAP.

Compensating the Error Amplifier

Using a MOSFET as an external pass element introduces a pole in the control loop that is a function of the UCC3837 output impedance, R_{OUT}, typically 6.5kΩ, and the MOSFET input gate capacitance. Figure 3 indicates that in the normal operation of a linear regulator using a MOSFET, the gate capacitance can be predicted directly from the MOSFET characteristic charge curve, using the relationship:

$$C_{IN} = \frac{\Delta Qgth}{\Delta Vgth}$$

This pole can be canceled by programming a zero frequency on the output of the UCC3837 error amplifier equal to the pole frequency. Therefore:

APPLICATION INFORMATION (cont.)

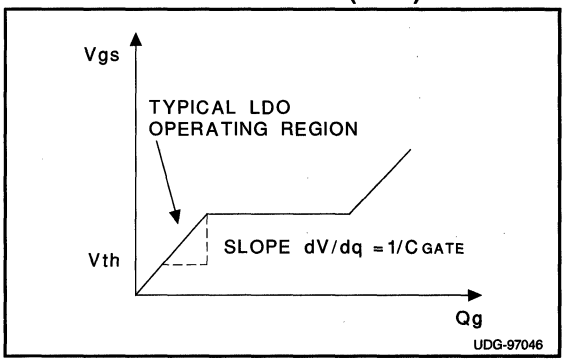


Figure 3.

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C_{IN} \bullet R_{OUT}}$$

$$F_{ZERO} = F_{POLE} = \frac{1}{2 \bullet \pi \bullet R_{COMP} \bullet C_{COMP}}$$

$$R_{COMP}C_{COMP} = \frac{1}{2 \bullet \pi \bullet F_{POLE}}$$

where CIN is the MOSFET input capacitance and ROUT is the output impedance of VOUT.

The value of CCOMP should be large enough that parasitics connected to COMP do not effect the zero frequency. A minimum of 220pF is recommended.

Transient Response

The transient performance of a linear regulator built using the UCC3837 can be predicted by understanding the dynamics of the transient event. Consider a load transient on the application circuit of Figure 1, where the output current steps from a low value to a high value. Initially, the output voltage will drop as a function of the output capacitors ESR times the load current change. In response to the decrease in feedback voltage at FB, the UCC3837 error amplifier will increase its charge current to a typical value of 40µA. The output of the amplifier will therefore respond by first stepping the voltage proportional to 40µA times RCOMP, and then ramping up proportional to 40µA and the value of CCOMP. Dynamic response can therefore be improved by increasing RCOMP and decreasing CCOMP.

The value of VOUT will increase the same amount as the increase in the error amplifier output. The UCC3837 output gate drive current, however, is internally limited to 1.5mA. The response of the voltage at the gate of the external pass element is therefore a function of the 1.5mA drive current and the external gate charge, as obtained from the MOSFET data sheet gate charge curve.

For the application circuit shown in Figure 1, the voltage at the error amplifier output will increase quickly by 400mV due to the 40µA current through RCOMP. The error amplifier will then slew at approximately 50mV per microsecond as the 40µA charges CCOMP.

From the IRL2203N data sheet, the typical required gate voltage at room temperature, to deliver 5A is 2.6V. The threshold for the device is approximately 1.5V. From the gate charge curve for the IRL2203N, approximately 7nC charge is required to change the gate voltage from 1.5V to 2.6V. With 1.5mA gate drive current, the required time to charge the gate is therefore 4.7µs.

Overcurrent Protection and Thermal Management:

Overcurrent protection is provided via the UCC3837's internal current amplifier and overcurrent comparator. If at any time the voltage across the current sense resistor crosses the comparator threshold, the UCC3837 begins to modulate the output driver at a 3% duty cycle. During the 3% on time, if the current forces 140mV across the sense amplifier, the UCC3837 will enter a constant output current mode. Figure 4 illustrates the cyclical retry of the UCC3837 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that

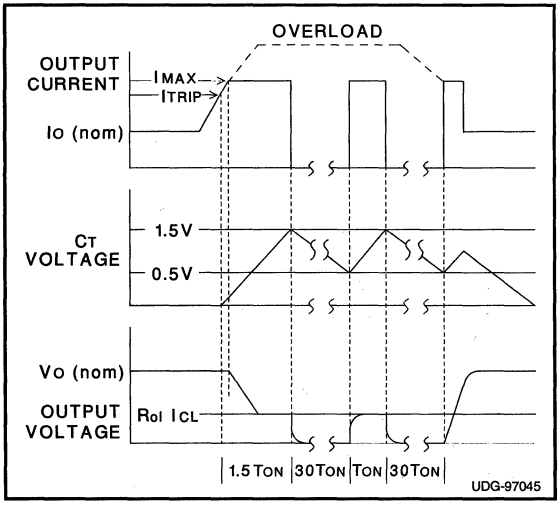


Figure 4. Load Current, Timing Capacitor Voltage and Output Voltage Under Fault Conditions

the timing capacitor is completely discharged and must initially charge to the reset threshold of 0.5V.

Fault time duration is controlled by the value of the timing capacitor, CT, according to the following equation:

APPLICATION INFORMATION (cont.)

$$t_{FAULT} = C_T \bullet \frac{\Delta V}{I} = C_T \bullet \frac{1.5 - 0.5}{36 \bullet 10^{-6}} = 27.8 \bullet 10^3 \bullet C_T \quad (1)$$

Figure 5 provides a plot of fault time vs. timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault. If not, the

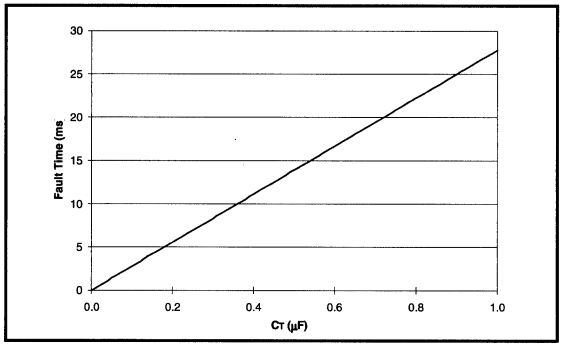


Figure 5. Fault Time vs. Timing Capacitance

charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on.

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and ITRIP values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$t_{FAULTmin} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}} \quad (2)$$

The minimum timing capacitor can be calculated by substituting equation (1) for tFAULT in equation (2) and solving for CT.

$$C_{Tmin} = \frac{C_{OUT} \bullet V_{OUT}}{27.8 \bullet 10^3 \bullet (I_{MAX} - I_{TRIP})} \quad (3)$$

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.25V input and a maximum output current of 5A, the power dissipated in the MOSFET is given by:

$$P = (V_{IN} - V_{RSENSE} - V_{OUT}) \bullet I_{OUT} \quad (4)$$

$$P = (5.25 - (5.002) - 3.3) \bullet 5 = 9.25W$$

Given that the thermal resistivity of the MOSFET is specified as 1°C/W for the TO-220 package style and assuming an ambient temperature of 50°C and a case to heat sink resistivity of Θ_{CS} = 0.3°C/W, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (5)$$

$$125 = 50 + 9.25 \bullet (1 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \leq 6.8° \text{ C/W}$$

Based on this analysis, any heatsink with a thermal resistivity of 6.8° C/W or less should suffice. The current in the circuit of Figure 1, under short circuit conditions, will be limited to 7A at a 3% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = [(V_{INmax} - I_{OUT} \bullet (R_{SENSE})) \bullet I_{OUT}] \bullet Duty \quad (6)$$

$$P = [(5.25 - 7 \bullet (0.02)) \bullet 7] \bullet 0.03 = 1.07W$$

Without switchmode protection, the short circuit power dissipation would be 35.8W, almost four times the nominal dissipation.

Using Printed Circuit Board Etch as a Sense Resistor

Unitrode Design Note 71 discusses the use of printed circuit board copper etch as a low ohm sense resistor. This technique can easily be applied when using the UCC3837. The application circuit shown in Figure 1 can be used as an example. This linear regulator is designed with a 5A average load current, demanding a 20mΩ sense resistor to result in a 100mV current sense comparator signal for the UCC3837. The maximum ambient temperature of the linear regulator is 70°C.

Using DN-71, a 1 ounce outer layer etch of 0.05 inches

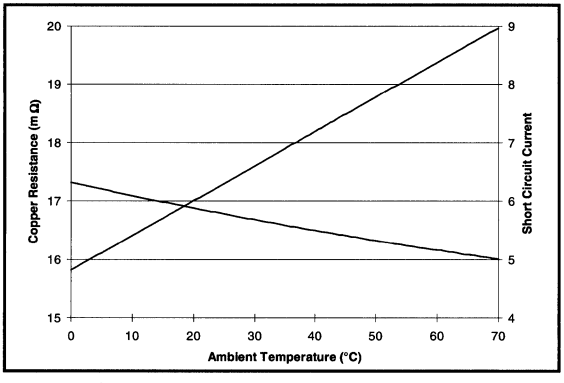


Figure 6. Copper Resistance and Short Circuit Limit for Example Resistor

APPLICATION INFORMATION (cont.)

wide and 1.57 inches long results in a resistance of 20mΩ at an ambient temperature of 70°C and an operating current of 5A. Because the resistivity of copper is a function of temperature, the current limit at lower temperatures will be higher, as shown in Figure 6.

Practical Considerations

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UCC3837 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation. Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100ns it takes the load current to slew from 200mA to 3A.

The dropout voltage of a linear regulator is often a key design parameter. Calculations of the dropout voltage of a linear regulator based on the UCC3837 Controller should consider all of the following:

- Sense resistor drop, including temperature and tolerance effects,
- Path resistance drops on both the input and output voltages,
- MOSFET resistance as a function of temperature and gate drive, including transient performance,
- Ground path drops.

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Fast LDO Linear Regulator

FEATURES

- Fast Transient Response
- 10mA to 5A Load Current
- Short Circuit Protection
- Maximum Dropout of 500mV at 5A Load Current
- Separate Bias and VIN Pins
- Available in Adjustable or Fixed Output Voltages
- 5 Pin Package allows Kelvin Sensing of Load Voltage
- Reverse Current Protection

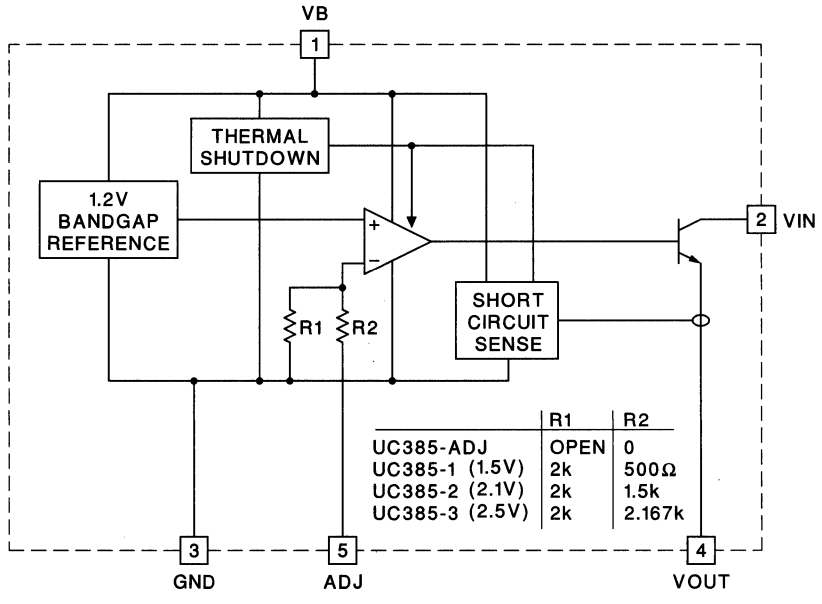
DESCRIPTION

The UC385 is a low dropout linear regulator providing a quick response to fast load changes. Combined with its precision on-board reference, the UC385 excels at driving GTL and BTL buses. Due to its fast response to load transients, the total capacitance required to decouple the regulator's output can be significantly decreased when compared to standard LDO linear regulators.

Dropout voltage (VIN to VOUT) is only 490mV maximum and 350mV typical at 5A load (–40°C to +100°C).

The on-board bandgap reference is stable with temperature and scaled for a 1.200V input to the internal power amplifier. The UC385 is available in fixed output voltages of 1.5V, 2.1V, or 2.5V. The output voltage of the adjustable version can be set with two external resistors. If the external resistors are omitted, the output voltage defaults to 1.2V.

BLOCK DIAGRAM



	R1	R2
UC385-ADJ	OPEN	0
UC385-1 (1.5V)	2k	500Ω
UC385-2 (2.1V)	2k	1.5k
UC385-3 (2.5V)	2k	2.167k

UDG-96193

ABSOLUTE MAXIMUM RATINGS

VIN . . . . . +7.5V
Output Voltage . . . . . +1.2V to 6.0V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

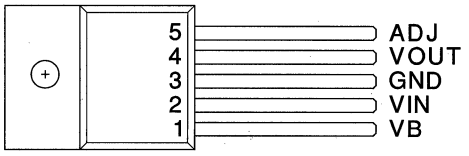
ORDERING INFORMATION

UC ☐ 85 ☐ - ☐
- ☐ Output Voltage
- ☐ Package
- ☐ Temperature Range

Temperature Range	Package	Output Voltage
1: –55°C to +125°C	T: TO-220	1: 1.5V
2: –40°C to +100°C	TD: TO-263	2: 2.1V
3: 0°C to + 100°C		3: 2.5V
		ADJ:1.2V or Adjustable

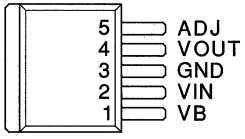
CONNECTION DIAGRAMS

5-Pin TO-220 (Top View)
T Package



Note: Tab = Ground

5-Pin TO-263 (Top View)
TD Package



Note: Tab = Ground

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC185-X series, –40°C to +100°C for the UC285-X series and 0°C to +100°C for the UC385-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V, $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
UC385-3 Fixed 2.5V, 5A Family					
Output Voltage (I_{VOUT} = 100mA)	UC385-3	2.475	2.5	2.525	V
	UC285-3 and UC185-3	2.45	2.5	2.525	V
Load Regulation	I_{VOUT} = 10mA to 5A		0.5	4	mV
VIN PSRR		80	110		dB
VB PSRR		50	65		dB
VIN Dropout Voltage = VIN– VOUT	I_{VOUT} = 5A, TJ = 25°C		350	425	mV
	I_{VOUT} = 5A, UC385-3		350	490	mV
	I_{VOUT} = 5A, UC285-3 and UC185-3		350	500	mV
VB Dropout = VB – VOUT	I_{VOUT} = 5A, UC385-3		1.9		V
	I_{VOUT} = 5A, UC285-3		1.9		V
	I_{VOUT} = 5A, UC185-3		1.9		V
Short Circuit Current Limit		5.3		6.5	A
VB Current	I_{VOUT} = 10A		8	11	mA
	I_{VOUT} = 5A		40	100	mA
VIN Current	I_{VOUT} = 5A	4.9	4.96		A
UC385-2 Fixed 2.1V, 5A Family					
Output Voltage (I_{VOUT} = 100mA)	UC385-2	2.079	2.1	2.121	V
	UC285-2 and UC185-2	2.058	2.1	2.121	V
Load Regulation	I_{VOUT} = 10mA to 5A		0.5	4	mV
VIN PSRR		80	110		dB
VB PSRR		50	67		dB
VIN Dropout Voltage = VIN – VOUT	I_{VOUT} = 5A, TJ = 25°C		350	425	mV
	I_{VOUT} = 5A, UC385-2		350	490	mV
	I_{VOUT} = 5A, UC285-2 and UC185-2		350	500	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these parameters apply for T_A = –55°C to 125°C for the UC185-X series, –40°C to +100°C for the UC285-X series and 0°C to +100°C for the UC385-X, VB = 5V; VIN = 3.3V, VOUT = 2.5V, $T_A = T_J$.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
UC385-2 Fixed 2.1V, 5A Family (cont.)					
VB Dropout = VB – VOUT	IVOUT = 5A, UC385-2		1.9		V
	IVOUT = 5A, UC285-2		1.9		V
	IVOUT = 5A, UC185-2		1.9		V
Short Circuit Current Limit		5.3		6.5	A
VB Current	IVOUT = 10mA		8	11	mA
	IVOUT = 5A		40	100	mA
VIN Current	IVOUT = 5A	4.9	4.96		A
UC385-1 Fixed 1.5V, 5A Family					
Output Voltage (IVOUT = 100mA)	UC385-1	1.485	1.5	1.515	V
	UC285-1 and UC185-1	1.470	1.5	1.515	V
Load Regulation	IVOUT = 10mA to 5A		0.5	4	mV
VIN PSRR		80	110		dB
VB PSRR		50	65		dB
VIN Dropout Voltage = VIN– VOUT	IVOUT = 5A, TJ = 25°C		350	425	mV
	IVOUT 5A, UC285-1		350	490	mV
	IVOUT = 5A, UC285-2 and UC185-1		350	500	mV
VB Dropout = VB – VOUT	IVOUT = 5A, UC385-1		1.9		V
	IVOUT = 5A, UC285-1		1.9		V
	IVOUT = 5A, UC185-1		1.9		V
Short Circuit Current Limit		5.3		6.5	A
VB Current	IVOUT = 10mA		8	11	mA
	IVOUT = 5A		40	100	mA
VIN = Current	IVOUT = 5A	4.9	4.96		A
UC385-ADJ Adjustable, 5A Family					
ADJ Voltage (IVOUT – 100mA)	UC385-ADJ	1.188	1.2	1.212	V
	UC285-ADJ and UC185-ADJ	1.176	1.2	1.212	V
Load Regulation	IVOUT = 10mA to 5A		0.5	4	mV
VIN PSRR	VOUT Programmed for 2.5V	80	110		dB
VB PSRR VOUT	Programmed for 2.5V	50	65		dB
VIN Dropout Voltage = VIN – VOUT	IVOUT = 5A, TJ = 25°C		350	425	mV
	IVOUT = 5A, UC385-ADJ		350	490	mV
	IVOUT = 5A, UC285-ADJ and UC185-ADJ		350	500	mV
VB Dropout = VB – VOUT	IVOUT = 5A, UC385-ADHJ		1.9		V
	IVOUT = 5A, UC285-ADJ		1.9		V
	IVOUT = 5A, UC185-ADJ		1.9		V
Short Circuit Current Limit		5.3		6.5	A
VB Current	IVOUT = 10mA		8	11	mA
	IVOUT = 5A		40	100	mA
VIN Current	IVOUT = 5A	4.9	4.96		A

PIN DESCRIPTIONS

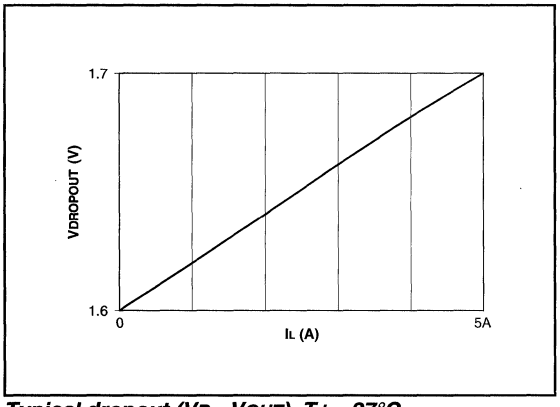
ADJ: In the adjustable version, the user programs the output voltage with two external resistors. The resistors should be 0.1% for high accuracy. The output amplifier is configured as a non-inverting operational amplifier. The resistors should meet the criteria of R3 || R4 < 100Ω. Connect ADJ to VOUT for an output voltage of 1.2V. Note that the point at which the feedback network is connected to the output is the Kelvin sense point.

GND: For accurate results, the GND pin should be referenced to the load ground.

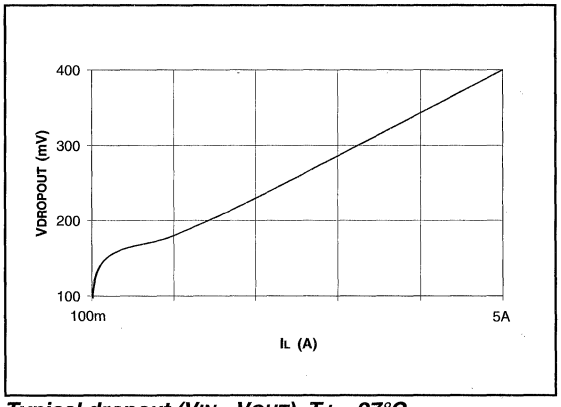
VB: Supplies power to all circuits of the regulator except the output power transistor. The 2V headroom from VB to VOUT allows the use of a Darlington output stage for inherently low output impedance and fast response. (Dropout is derated for junction temperatures below 0°C.)

VIN: Supplies the current to the collector of the output power transistor only. The dropout (VIN-VOUT) is under 100mV for light loads; maximum dropout is 490mV at 5A for T_J = 0°C to +110°C. (Dropout is derated for junction temperatures over 110°C.)

VOUT: This pin should be connected to the load via a low impedance path. Avoid connectors which add significant inductance and resistance. Note that even though a Kelvin sense is available through a 5 pin package, care must be taken since voltage drops along wire traces add to the dropout voltage.



Typical dropout (V_B - V_{OUT}), T_J = 27°C.



Typical dropout (V_{IN} - V_{OUT}), T_J = 27°C.

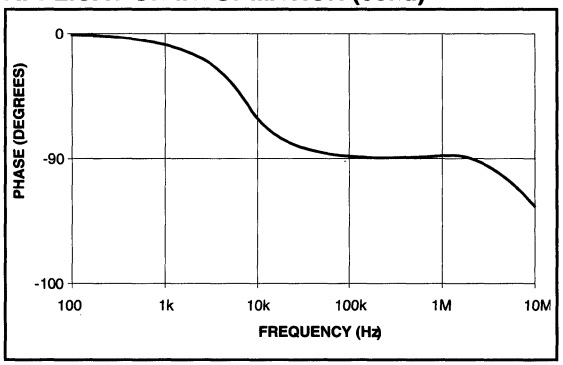
APPLICATION INFORMATION

The UC385 is easy to use. The adjustable version requires two resistors to set the output voltage. The fixed versions of the UC385 require no external resistors. All versions of the UC385 require decoupling capacitors on the input and output. In a typical application, VB and VIN are driven from switching power supplies which may have large filter capacitors at their outputs. If the UC385 is further than 12 inches from the power supply, it is recommended to add local decoupling as close as possible to the linear regulator.

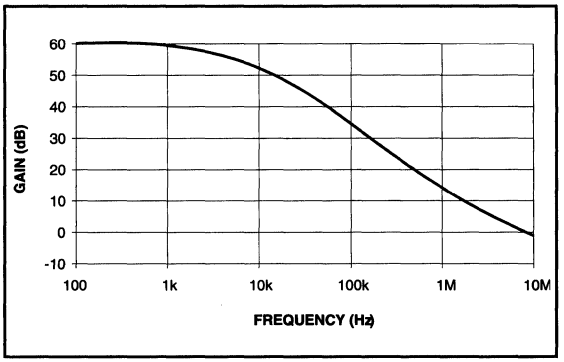
Decouple the output of the UC385 with at least 100μF of high quality tantalum or Sanyo OSCON capacitors close to the VOUT pin for maximum stability. Many applications involving ultra fast GTL or BTL applications require additional capacitance close to the load. The exact amount will vary according to speed and magnitude of the load transients and the tolerance allowed for transients on VOUT. When specifying the decoupling capacitors, the series resistance of the capacitor bank is an important factor in its ability to filter load transients.

The UC385 allows for Kelvin sensing the voltage at the load. This improves regulation performance and eliminates the voltage drops due to wire trace resistance. This voltage drop must be added to the headroom (VIN to VOUT and VB to VOUT). The dropout of 450mV is measured at the pins and does not include additional drops due to trace resistance.

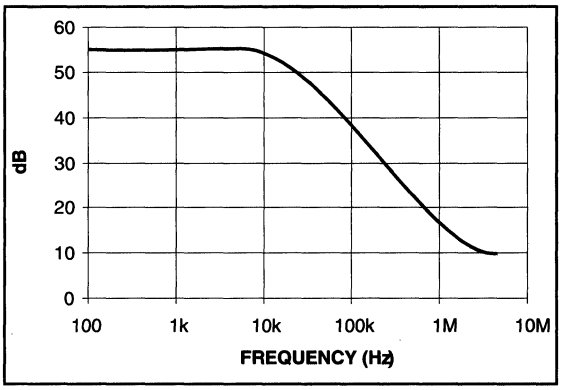
APPLICATION INFORMATION (cont.)



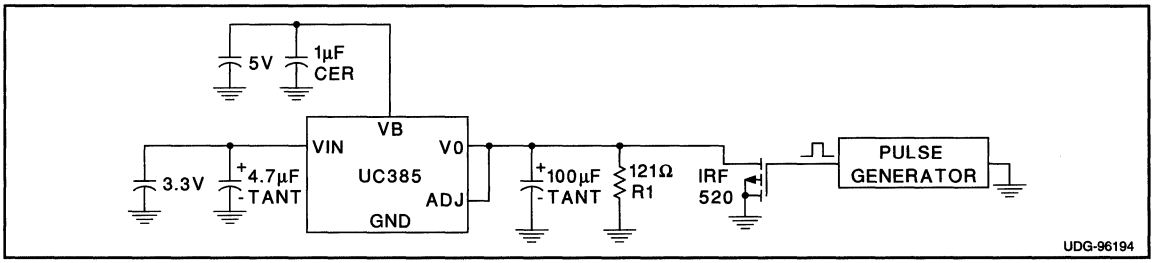
Open loop phase (100µf output capacitance, 1a load).



Open loop gain (100µf output capacitance, 1a load).

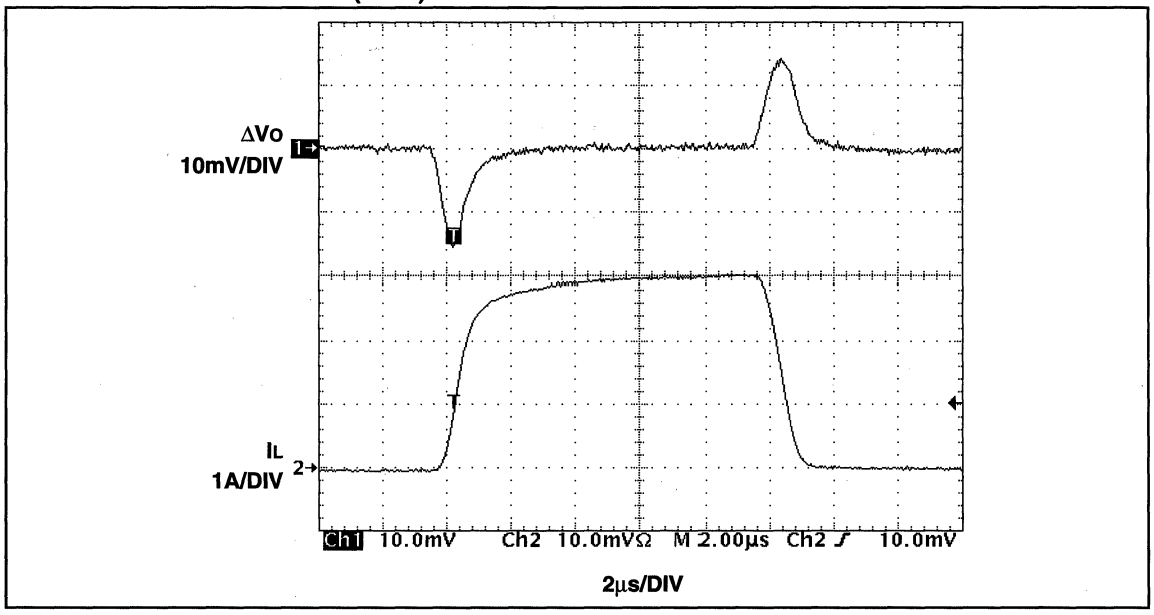


PSRR (V_B).

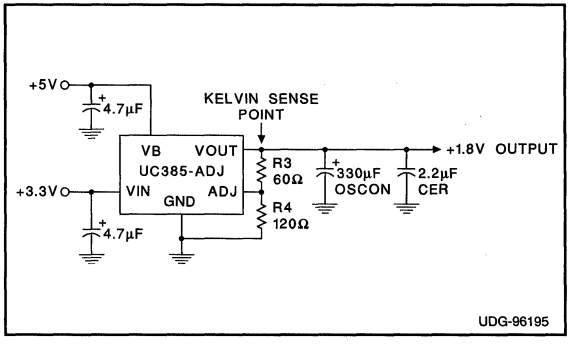


Transient test circuit.

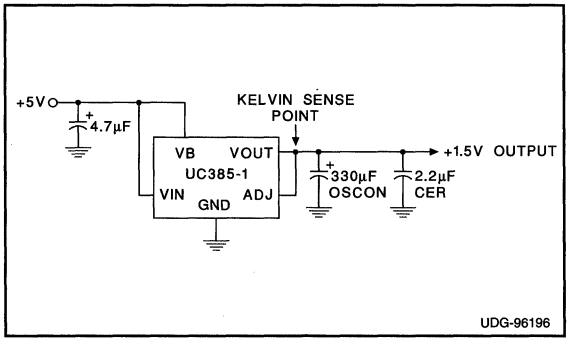
APPLICATION INFORMATION (cont.)



10mA to 3A/µs load transient response.



Typical UC385-ADJ application.



Typical UC385-1, -2, or -3 application.

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Design Note

OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES

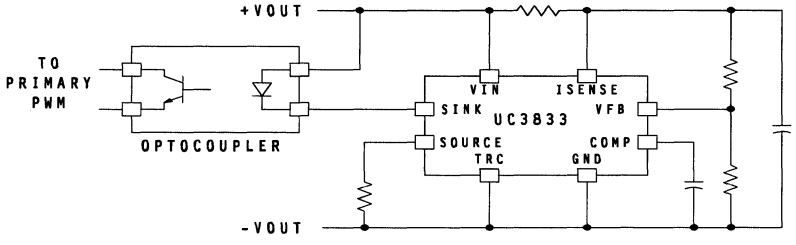
The use of optocouplers in the feedback path of switch-mode power supplies is probably one of the most common practices in the industry. Benefits of this method include low component cost, high voltage isolation and simplicity of design and implementation. Although adequate for many existing designs, the need for additional loop gain bandwidth occurs as switching frequencies are pushed towards the megahertz region.

One of the most popular ways to drive an optocoupler utilizes a TL431 Adjustable Shunt Regulator. It is configured on the output side of the power supply to modulate the optocoupler's photo diode current as a function of the power supply output voltage. Across its isolation boundary, the optocoupler transistor is connected to the PWM controller's error amplifier on the primary side of the power supply. Variations in the output voltage are optically transferred back to the error amplifier and control loop for correction. Providing additional features like over current protection or external shutdown require extra optocouplers and drive mechanisms, thus increasing the circuit complexity.

A linear regulator control IC, such as the UC3832, UC3833 or UC3836 can be substituted for the '431 while providing numerous additional features besides regulating the output. Overcurrent limiting and fault protection can be combined with the error voltage to drive the optocoupler and override it when necessary. Handshaking with external control logic, such as shutdown and sequencing is greatly simplified since the control IC is referred to the same ground. The most obvious benefit, however, is the introduction of the supplementary error amplifier in the feedback loop with programmable compensation.

Depending on the specific application, current limiting can be tailored to accommodate a programmable foldback characteristic, constant current or complete overcurrent shutdown. The UC3832 and UC3833 provide an addition level of versatility by offering a programmable duration event timer in the current limit circuitry. An adjustable trip threshold to accommodate varying load demands can be facilitated with the UC3832. For additional information, please consult application note U-116 and the respective device data sheets.

UC3833 LINEAR CONTROL IC DRIVES OPTOCOUPLED FEEDBACK



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A High Performance Linear Regulator for Low Dropout Applications

by Dave Zendzian

INTRODUCTION

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down and regulating the existing 5V system supply. To complicate matters further, the performance of these devices is directly related to supply voltage. This results in a need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. As of late, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design offers several desirable features including low output noise and wide bandwidth resulting in excellent transient load response.

This design note presents a linear regulator capable of maximizing the performance of these digital systems. The regulator is designed to meet the following system requirements:

V_{IN} = 5V ± 10%
V_{OUT} = 3.3V ± 5%
I_{OUT} = 3.5A typical, 4A maximum

Transient Response:
5% to 75% $I_{OUT(max)}$ in 100nsec, VREG = ± 5%

TOPOLOGY REVIEW

The regulator is implemented using a UC3833, precision linear controller. This IC includes all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier and an uncommitted output stage. Providing a driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. An innovative, switchmode current limiting technique is also implemented by the UC3833, significantly reducing power dissipation during fault conditions.

The crux of the design lies in the selection of a pass device. Requirements for the selected power device include operation under very low input/output differential voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage compared to a Darlington and simpler base drive than an NPN configuration. However, the gain of these devices is typically quite low, resulting in the need for significant base drive current. As the output requirements of the regulator increase the base current losses quickly become excessive, thereby decreasing the efficiency, along with the advantages of the linear regulator.

This leaves the P-channel MOSFET as the most likely candidate. While older generation P-channel devices are plagued with high on-resistance, recent advancements in high cell density technology have led to substantial reductions in RDSon. Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL is a 50A, 30V, logic level P-channel device with a maximum on-resistance of only 30mΩ. The maximum gate threshold voltage of 2.0V is necessary due to the 5V input requirement of this application. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in trans-conductance mode it can be biased with minimal drive current, further improving the efficiency of the regulator.

Bulk output capacitance is added to the design in order to help meet the 100nsec load transient requirement. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time charge is removed from the capacitor and its voltage correspondingly decreases until

the control loop can catch the error and correct for the increased load. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship I= CdV/dt. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected.

DESIGN DETAILS

Figure 1 illustrates the final design. Resistors R4 and R5 provide the bias for the pass transistor, Q1. By including emitter resistor R5, the UC3833 drive transistor's β is eliminated from the loop gain expression, thereby simplifying the compensation. Resistors R6 and R7 provide voltage feedback to the UC3833 while components R3, C2 and C3 compensate the voltage and current loops. Further compensation of the current loop is provided by the pole-zero pair introduced by R8, C7 and C8.

Current control is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the 100mV comparator threshold, the UC3833 begins to modulate the output driver. The duty cycle is approximately 5% with on and off-times set by timing components C1 and R2. During the on-time, the current sense amplifier provides constant output current by maintaining 135mV across R1. Duty cycle protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation, and not the full short circuit power.

Output capacitors were chosen based upon their ESR/ESL specifications and package style. The output capacitance is implemented using three surface mount, solid tantalum capacitors in parallel. This acts to reduce the equivalent ESR and ESL by 1/3, keeping the associated voltage transients within specification. Sprague 595D capacitors were used, providing an equivalent impedance of approximately 13mΩ typical and 60mΩ max at 100kHz. The surface mount package helps to further reduce the parasitic effects induced by component leads.

In order to achieve the expected performance, careful attention must be paid to circuit layout. The circuit should be laid out using a single point ground referenced to the return of the output capacitor. In addition, all high current carrying traces should be made as short and wide as possible in order to minimize the effects of parasitic resistance

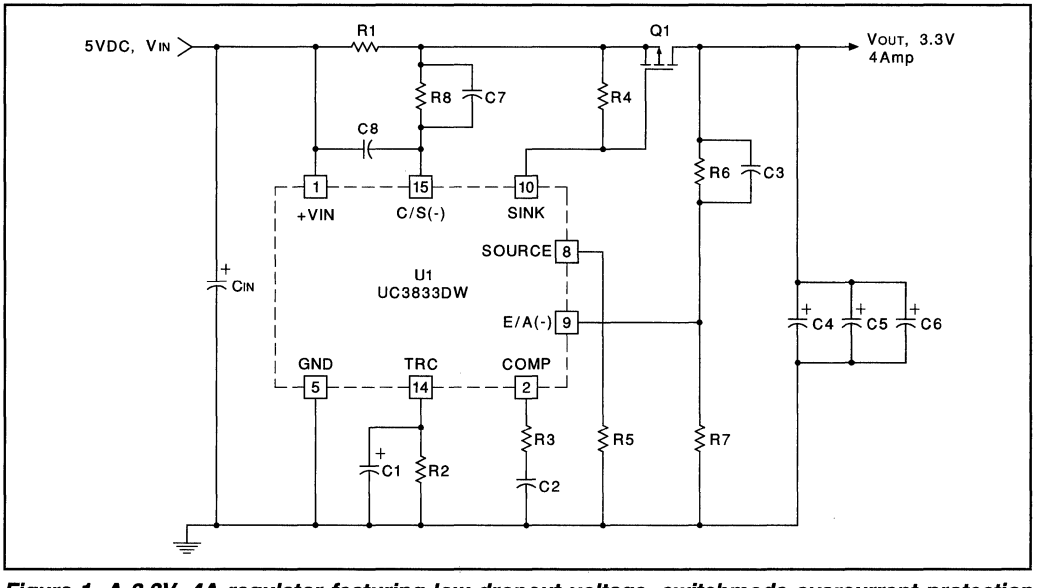

Figure 1. A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

and inductance. To illustrate the importance of these concepts, lets examine the effect of a 1.5" PCB trace located between the output capacitor and the UC3833 ground reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A. Each of these effects can be minimized by optimizing the layout and using generous amounts of copper on all high current runs.

Thermal control is provided by heatsinking the power MOSFET pass device. Any heatsink of 7.5°C/W or lower will keep the junction temperature of the MOSFET below 125°C at ambient temperatures up to 50°C and worst case operating conditions.

PERFORMANCE

In a typical application of 3A out with 5.0V in, the efficiency of the regulator is 65.5%. Under maximum load and worst case conditions the efficiency drops to 60%. During a short circuit, the regulator limits the peak output current to approximately 6A by design. At the 5% duty cycle set by C1 and R2, the average current is limited to 300mA, resulting in only 2W of power dissipated in the MOSFET as opposed to the potential dissipation of 32W in a constant current application!

Worst case DC regulation of ± 3% is accomplished using the UC3833 in conjunction with 1% feedback resistors. If a tighter tolerance is required the UC3832 can be substituted for the UC3833 along with 0.1% resistors. The UC3832 includes provisions for an external voltage reference, allowing increased performance over the UC3833's 1% internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 2 illustrates how the design behaves during the specified 100nsec load transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 2. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable

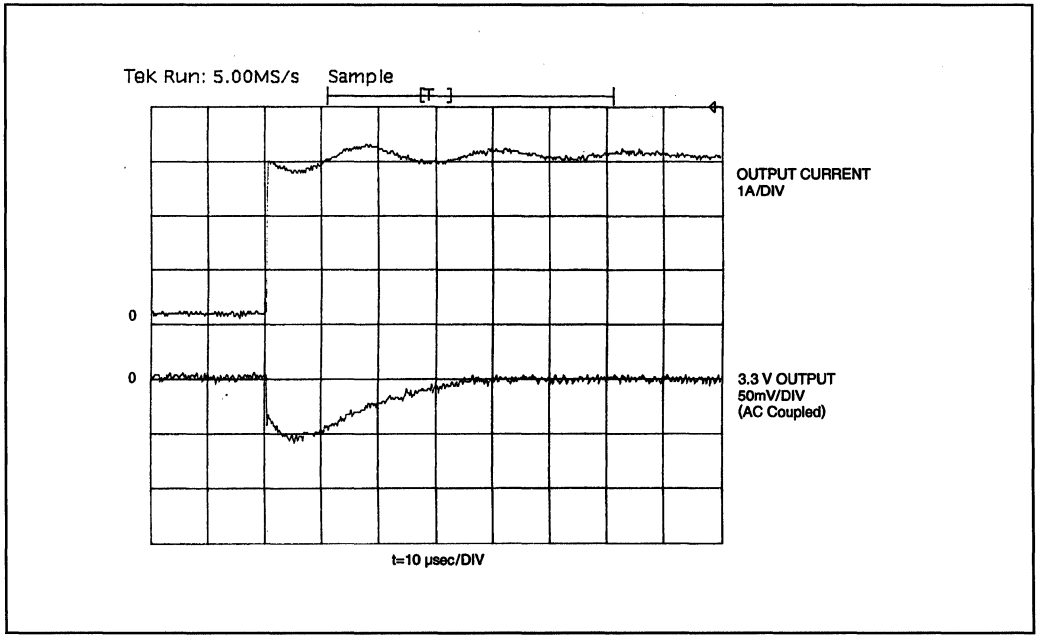

Figure 2. Transient response of the regulator illustrated in Figure 1 with a time base of 10µsec. The top trace is the load current on the output of the regulator. The bottom trace shows the transient recovery of the regulator's output when the load is stepped from 200mA to 3A.

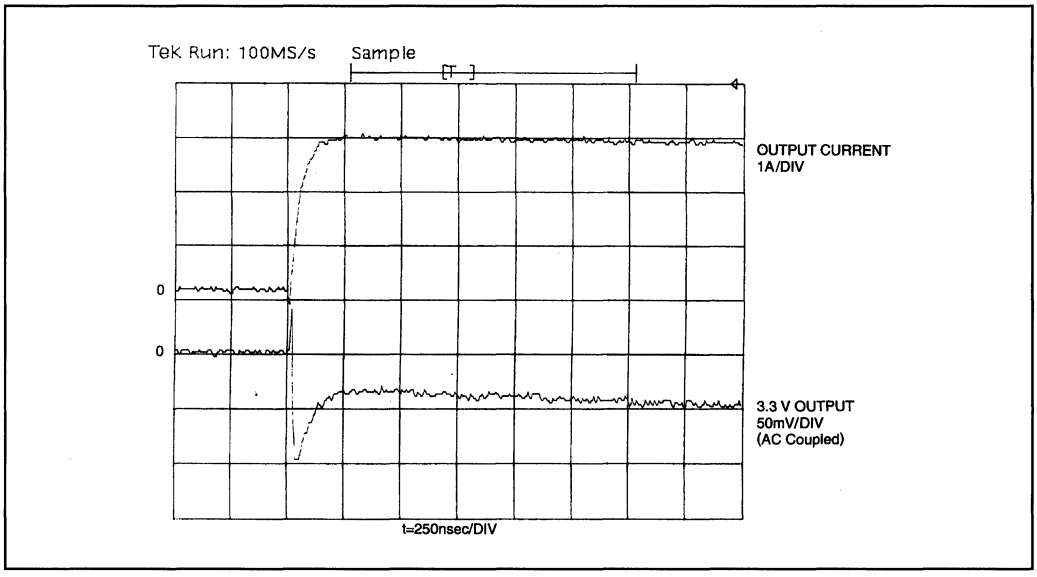

Figure 3. Transient response of the regulator illustrated in Figure 1 with a timebase of 250nsec. The top trace is the load current on the output of the regulator. The bottom trace shows the initial output transient resulting from the equivalent impedance of the output capacitor during a load step from 200mA to 3A.

state within 40µsec. Figure 3 shows the same response with a timebase expanded to 250nsec. In this plot the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

The circuit described in this design note can be easily modified to accommodate a variety of output voltage and current requirements. For additional information regarding the UC3832/3 linear controllers consult Unitrode application note U-116. Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectively.

Table 1. Parts list.

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1,C8 = 1µF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2,C3 = 0.1µF		
R3,R8 = 100Ω	C4,C5,C6 = 270µF		
R4 = 300Ω	C7 = 3300pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC 1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

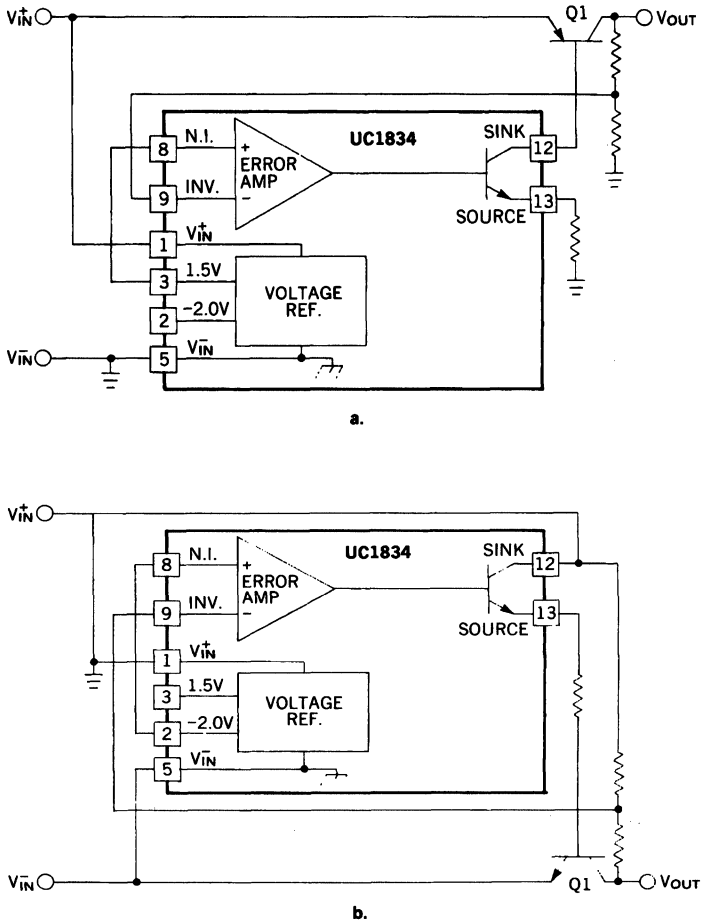


Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

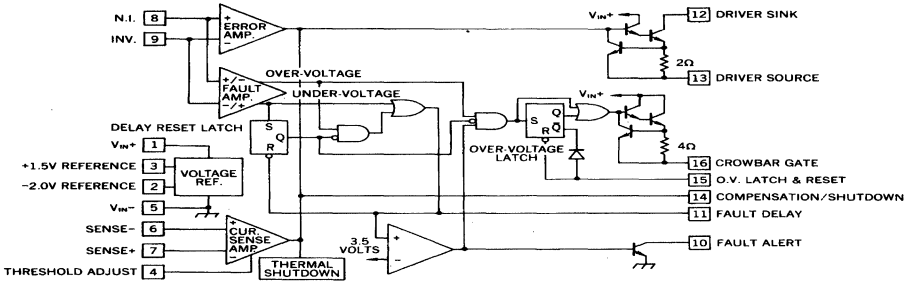


Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~ 30A) is possible with the Darlington pass elements of Figure 3d.

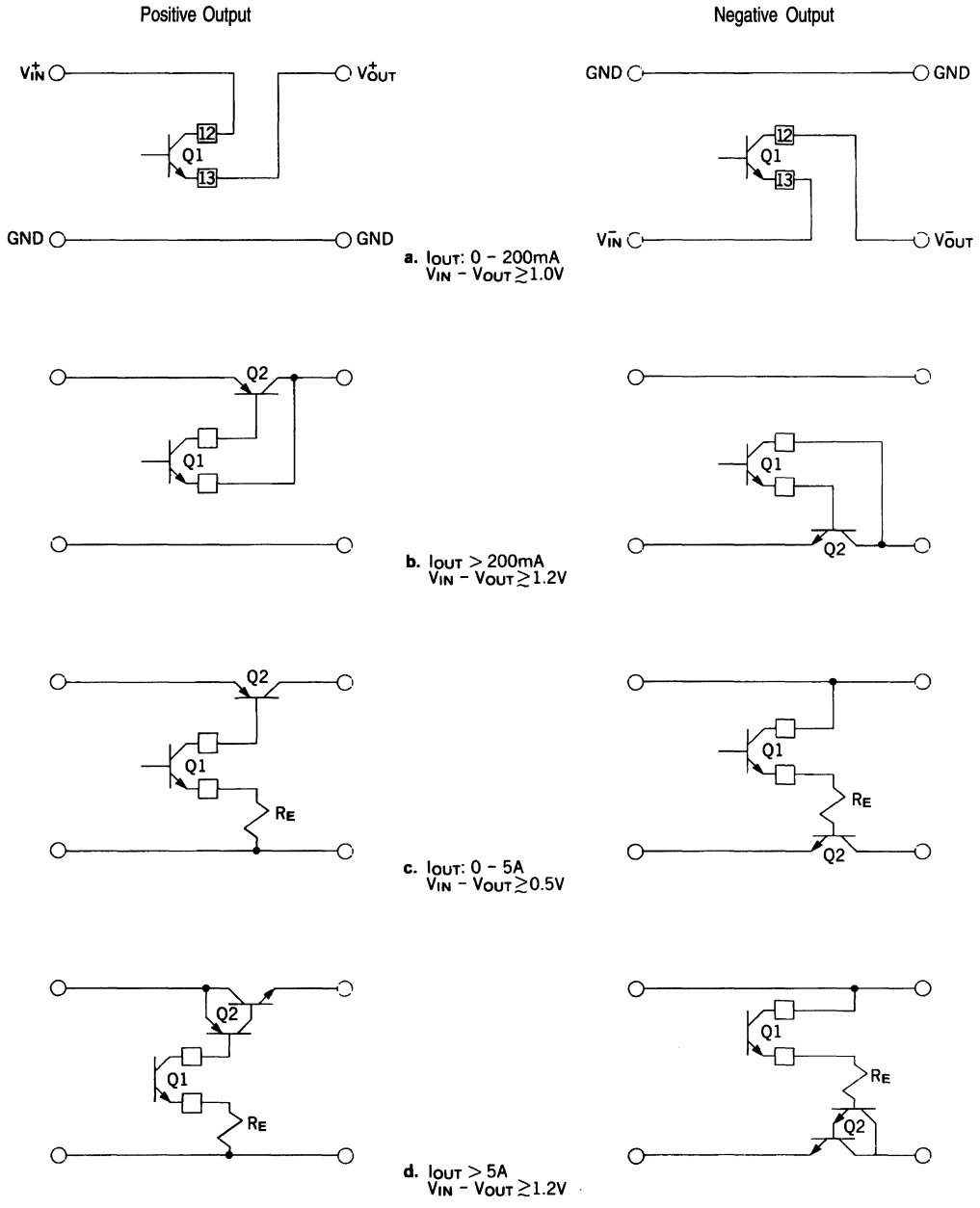


Figure 3. Pass Transistor Configurations

Current in the UC 1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

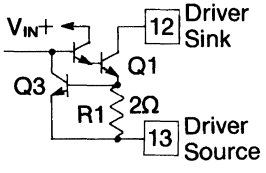
A resistor (is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

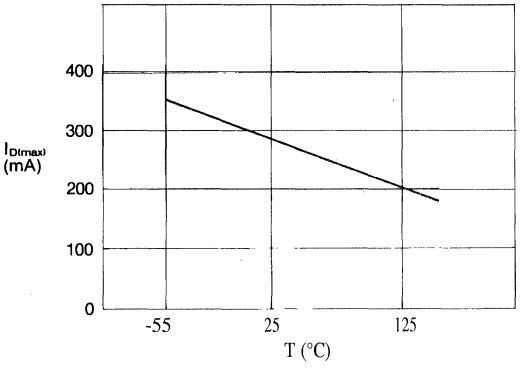
where: $V_{R_E\,(min)}$ is minimum voltage available to R_E
$I_{B(max)\,(Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)}\ q\ (V_{E/A\,out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC 1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

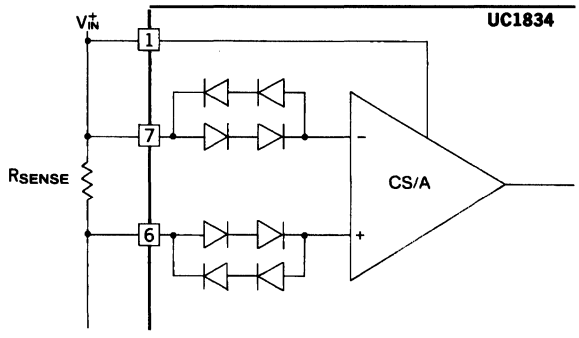


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \bullet V_{TH(d)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

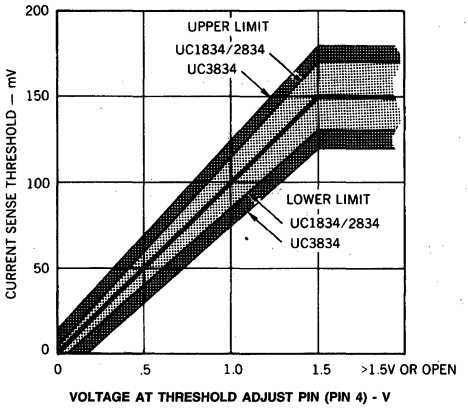


Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

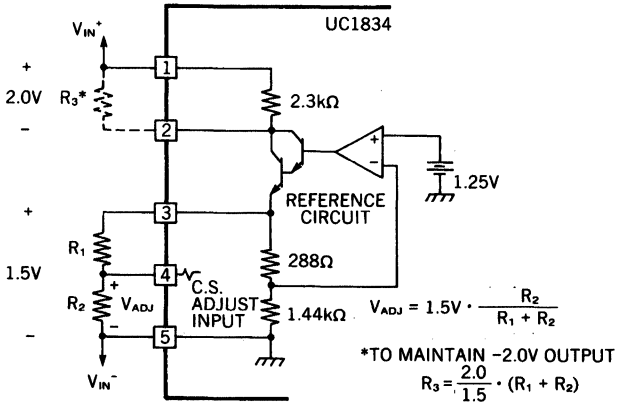


Figure 7. Setting the Current Threshold and Compensating the -2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage. The supply output voltage can decrease a proportional amount. When the CS/ input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/ and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

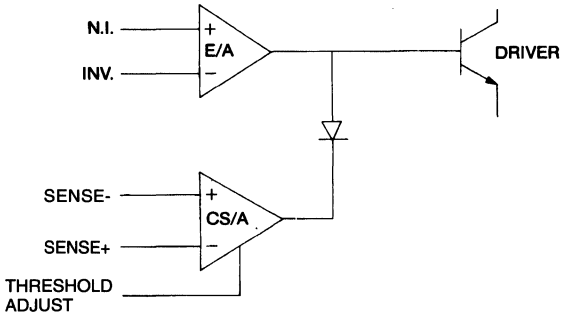


Figure 8. Current Sense Tied to E/A Output

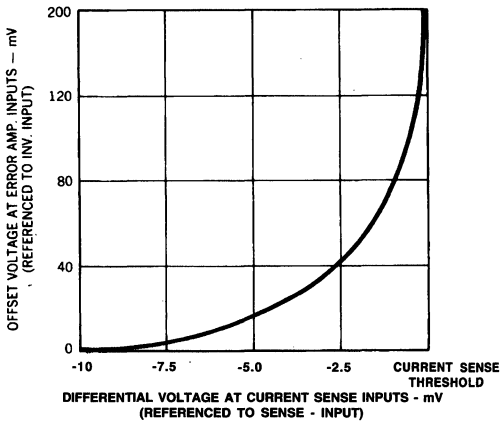


Figure 9. Current Limiting Knee Characteristic

FOLD BACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$I_{E(max)} \cdot V_{CE} \simeq K$ where **K** is a constant
or: $I_{E(max)} \simeq K/(V_{IN} - V_{OUT})$ (ignoring the sense resistor voltage drop).

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

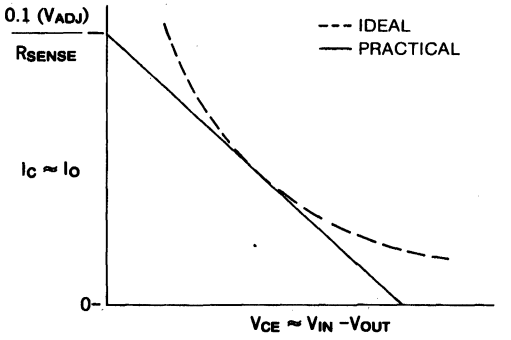


Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

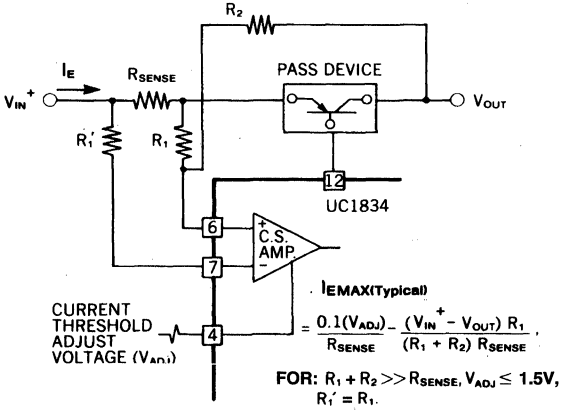


Figure 11. Foldback Current Limiting - Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

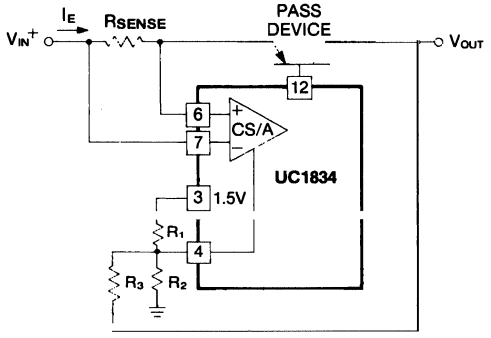


Figure 12. Foldback Current Limiting – Responds to Changes in V_{OUT} Only

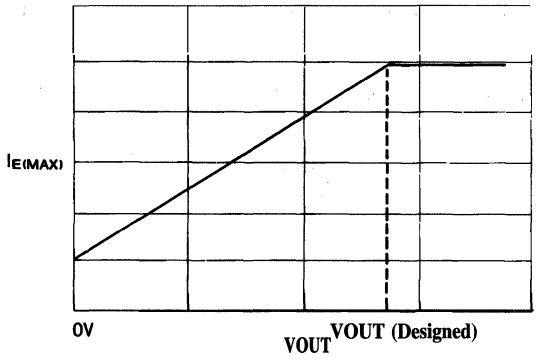


Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC 1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/ A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}|$ = 150mV. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/ μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\bar{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\bar{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

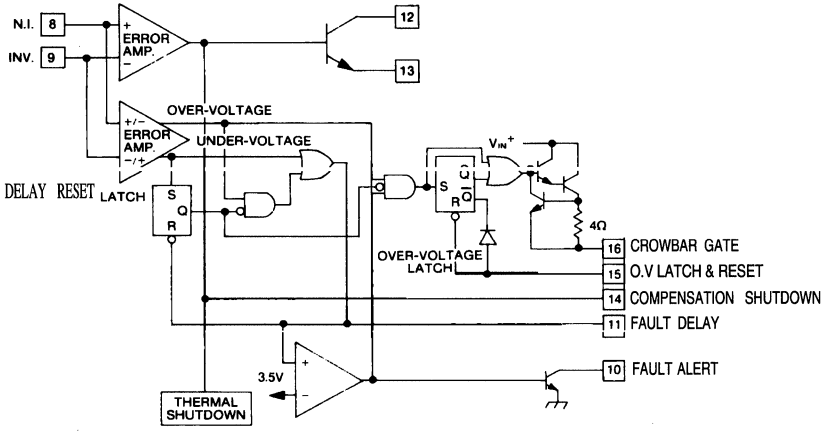


Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_C) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_C.

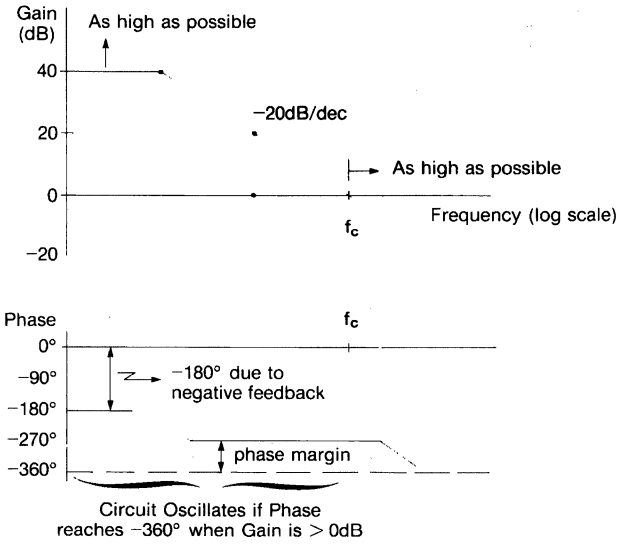


Figure 15. Desired Closed-Loop Response

Linear supplies using the UC 1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which, when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two. and can be treated in essentially the same ways.

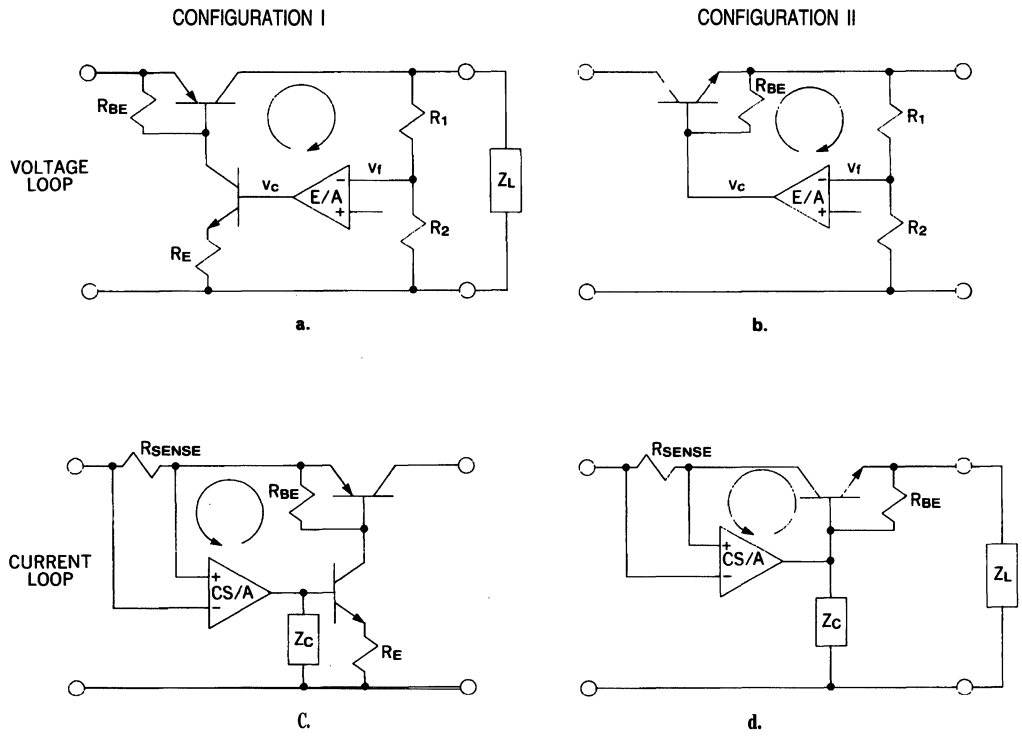


Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β q 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50MHz}{200} = 250kHz$$

Assuming a minimum load of 1A ($R_L = 5\Omega$), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51k\Omega}{(1.7 + 0.51)\,k\Omega} = 20 = 26dB.$$

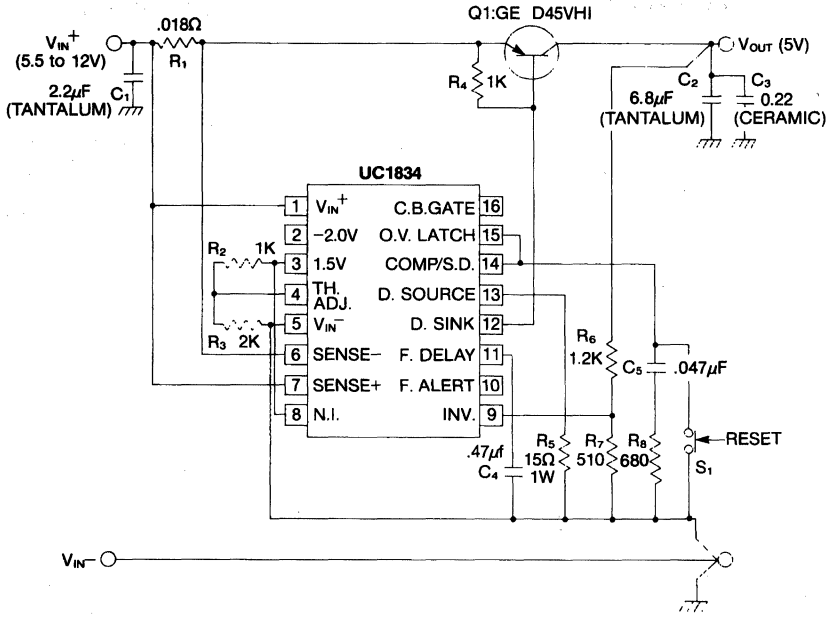


Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~ 0dBE/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

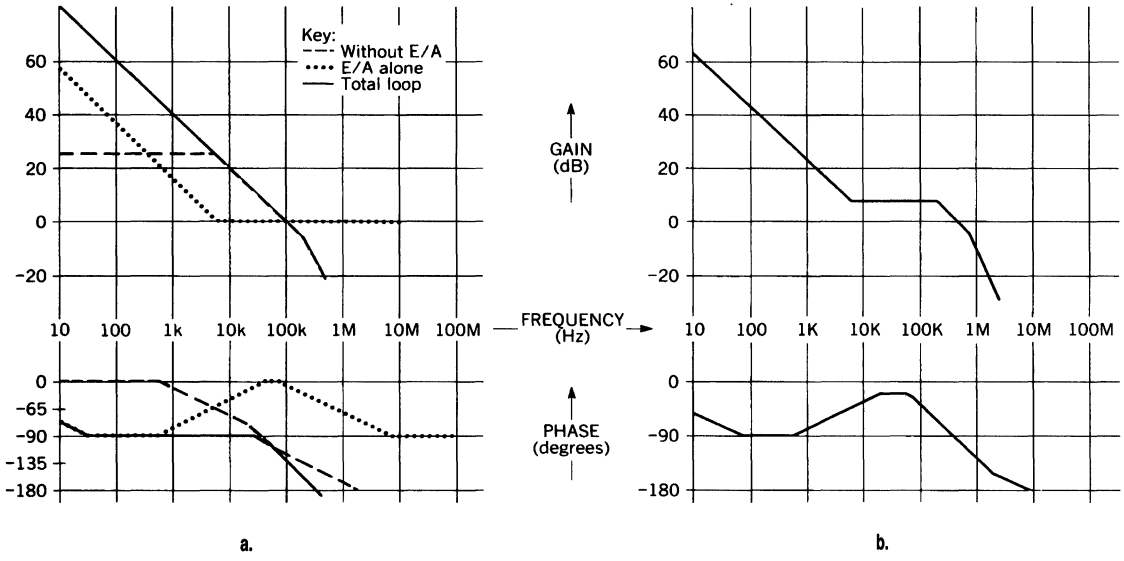


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

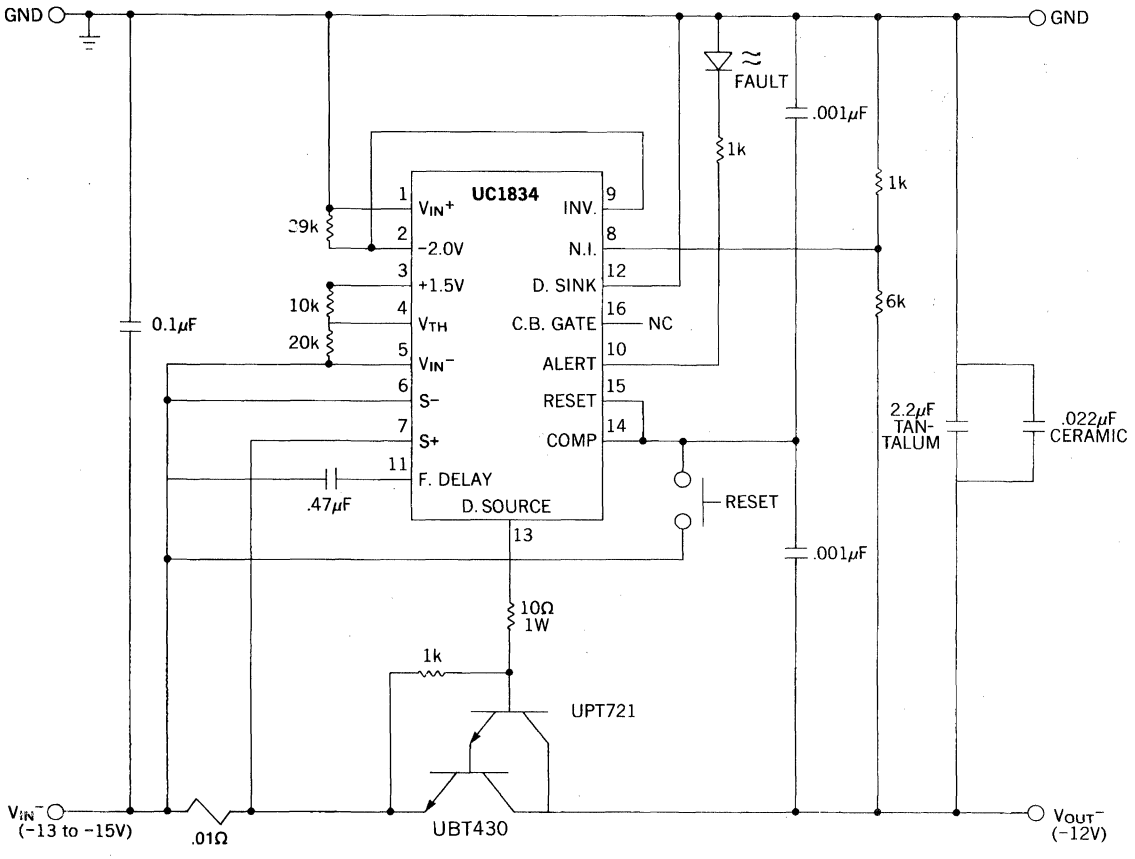


Figure 19. -12V, -10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of 1/

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at f_p=fr/P. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where:: $r_e = \frac{kT}{qI_C} = \frac{26mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1+R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right).$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

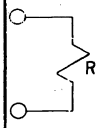
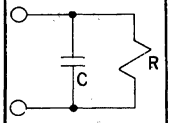
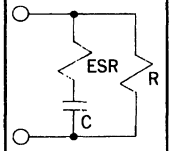
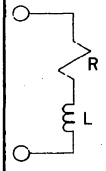
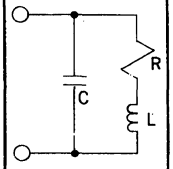
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0,\ \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_C \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

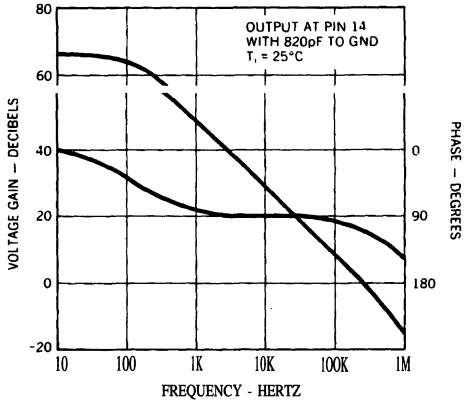


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is. to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

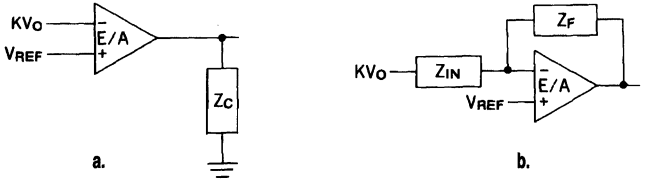


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

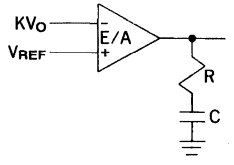
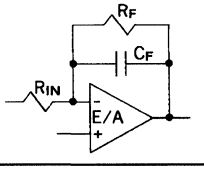
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s\,R_FC_F)}$	$\frac{1}{2\pi\,R_FC_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC 1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega$ = 14mS. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

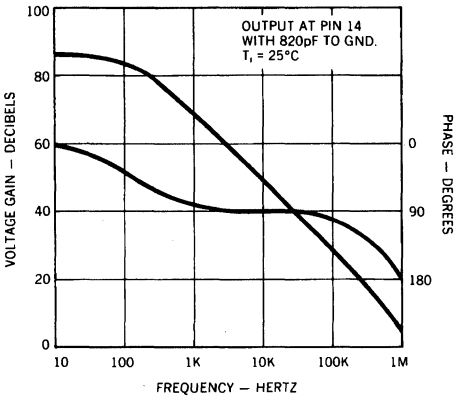


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d). Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right).$$

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A HIGH PERFORMANCE LINEAR REGULATOR FOR LOW DROPOUT APPLICATIONS

Dave Zendzian
Applications Engineer

INTRODUCTION

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down the existing 5V system supply. To complicate matters further, microprocessor performance is directly related to the quality of the supply voltage. This results in the need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. Recently, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design, on the other hand, offers several desirable features including low output noise and wide bandwidth, resulting in excellent transient load response. This application note presents a high performance linear regulator design capable of maximizing the performance of these digital systems.

LINEAR VS SWITCHER

Figure 1 illustrates the basic elements of both a linear and switching stepdown regulator. In the linear topology, the output is regulated by controlling the voltage drop across a power transistor biased in the linear region. The switching circuit, on the other hand, provides regulation by varying the duty cycle of a saturated power switch. Although switchers offer a substantial efficiency advantage in applications with large differences between input and output voltage, the savings become less significant as this difference is reduced. To illustrate this point, consider the differences in a 3A, 5V to 3.3V converter design using the two topologies.

The power dissipation in the linear regulator is a function of the difference between input and output voltage, output current, output driver power, and quiescent controller power:

Input/Output Voltage Drop (5.0-3.3V)(3A) = 5.1W

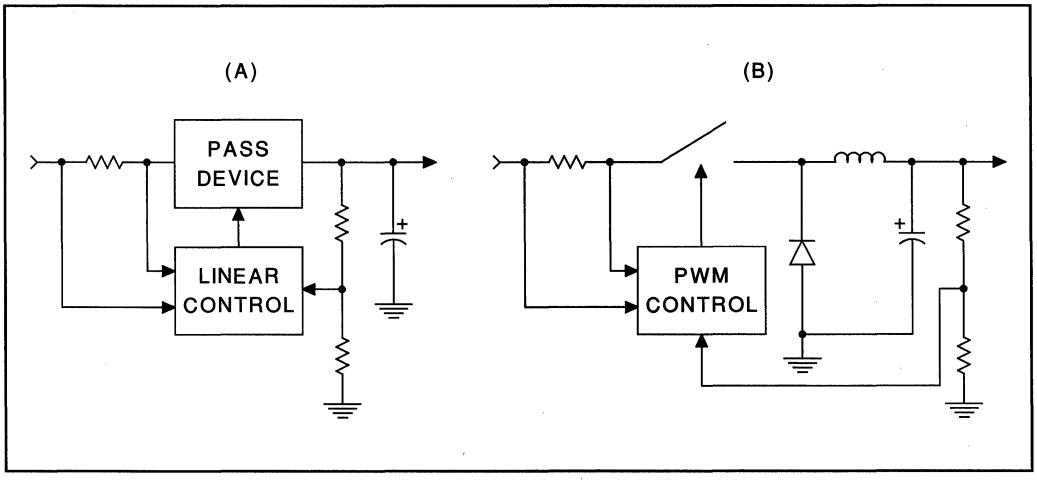


Figure 1. Basic elements of a A.) Linear and B.) Switching Regulator.

Pass Device Driver	(5.0V)(0.005A) = 0.03W
Controller Icc	(5.0V)(0.01A) = 0.05W
	Total = 5.18 W

The resulting efficiency is equivalent to the ratio of output power to input power or (3.3)(3)/((3.3)(3)+5.18) = 65.7%.

The efficiency of the switching regulator is not as simple to calculate. Power dissipated by the regulator is a combination of both conduction and switching losses in each of the circuit elements. Assuming an inexpensive, commercial power MOSFET with an Rds(on) of 0.28W, the duty cycle of the regulator is approximately:

$$\frac{t_{ON}}{t_{OFF}} = \frac{3.3}{(5 - 3(0.28))} \approx 88\%$$

Taking duty cycle into account, the itemized circuit losses are estimated as follows:

FET Conduction Losses	$(3A)^2(0.28\Omega)(80\%)$ = 2.02W
FET Switching Losses	(8.4E-9C)(5V)(250kHz) = 0.01W
Diode Forward Voltage	(0.6V)(3A)(20%) = 0.36W
Inductor Voltage	$(3A)^2(0.017\Omega)(100\%)$ = 0.15W
RSENSE Voltage	$(3A)^2(0.043\Omega)(80\%)$ = 0.31W
AC Capacitor Losses	$(0.15)^2(2.2\Omega)$ = 0.05W
Controller Icc	(5V)(1E-3A) = 0.01W
Switching Transients	≈ 0.10W
	Total = 3.01W

Based upon these losses, the efficiency of the switching regulator is approximately (3.3)(3)/((3.3)(3)+3.01) = 76.7%. These results indicate that the switching topology is approximately 11% more efficient in this application. However, the increase in efficiency doesn't come for free. The catch diode and inductor required in the switching topology increase the cost of the solution. In addition, due to the pulsed nature of the input current, the switching topology can generate considerable noise or electromagnetic interference (EMI), often requiring additional filtering to provide a compliant design. Differential current sensing and minimum load requirements further complicate the solution. Synchronous switching topologies and better components can improve the efficiency to better than 90%, but the number of components and cost of the solution increases even further.

The linear regulator, on the other hand, while slightly less efficient offers several attractive features. Low noise is inherent to the design due to the lack of fast switching circuits. Reduced component count coupled with a relatively simple design help to ensure system reliability and lower cost. Moreover, the linear solution does not have a minimum load restriction making it attractive in applications with widely varying load currents. The remainder of this application note provides the design details for a high performance linear regulator, taking advantage of each of these performance features.

TOPOLOGY OVERVIEW

Referring again to Figure 1, the linear design can be broken-down into several key elements including a pass device, driver, error amplifier, reference, output capacitance and over current protection block. The crux of the design arguably lies in the pass device. It's characteristics determine what the differential, input/output voltage limitations are in addition to how much quiescent power is required by the regulator. Error amplifier characteristics directly effect system bandwidth and the achievable DC regulation while the voltage reference primarily governs the steady state accuracy of the output voltage. Lastly, the overcurrent protection block protects the regulator during output fault conditions.

POWER PASS DEVICES

The power device selected to provide the pass function must be capable of operating under very low differential input/output voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage when compared to Darlington devices, and simpler base drive than an NPN configuration. Unfortunately, as the output requirements of the regulator grow, the gain of suitable PNP power transistors decreases, ultimately resulting in excessive base current losses. In addition, large amounts of base drive current often require more elaborate drive stages, further complicating the design. Consequently, the efficiency and advantages of the linear regulator are no longer as great.

Having eliminated bipolar configurations for either excessive drive current or dropout voltage, pass device options are limited to power MOSFETs. N-channel devices are most advantageous due to their low on-resistance and cost. Unfortunately, the gate drive difficulties associated with high side topologies make them less than ideal in applica-

tions operating from a single supply. P-channel MOSFETs, while easier to drive in high side applications, have historically been plagued with higher on-resistance. However, recent advancements in high cell density technology have led to substantial reductions in $R_{DS(on)}$. For instance, Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL, a 50A, 30V, P-channel MOSFET is one such example, specified with a maximum on-resistance of 30mΩ at drain currents of 25A and a maximum gate threshold voltage of 2.0V. The logic level gate characteristics are required in applications limited to a supply voltage of 5 volts. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in transconductance mode it can be biased with minimal drive current, further improving the efficiency and decreasing the complexity of the regulator.

OUTPUT CAPACITANCE

Bulk output capacitance is required in order for the design to meet the specified transient requirements. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time, charge is removed from the capacitor and its voltage correspondingly decreases until the control loop can catch the error and correct for the increased current demand. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship I=CdV/dt. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected to satisfy the charge relationship.

OVERCURRENT PROTECTION

Traditional over current protection schemes usually involve either "constant current" or "current foldback" techniques. Unfortunately, each of these solutions offers a compromise between the needs of the user and the optimization of the power supply. Constant current techniques, while easy to interface with, result in massive overkill in terms of thermal management and heatsink implementation. Current foldback implementations, on the other hand, ease the design of the regulator while complicating startup scenarios for the user. Newer, switchmode protection techniques offer a solution to this compromise. By modulating the output at a fixed duty-cycle during an over current condition, thermal management of the regulator is greatly simplified. Adjusting the pulse width of the duty-cycle allows start-up load characteristics to be easily accommodated.

CONTROL CIRCUIT

In the design example that follows, the regulator is implemented using a UC3833, precision linear controller. This IC incorporates all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier, and an uncommitted output stage. Providing an output driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. Switchmode current limiting is also implemented by the UC3833, significantly reducing power dissipation during fault conditions. Further information regarding this device can be found in Unitrode application note U-116.

DESIGN DETAILS

The regulator was designed to meet the following performance requirements, typical of today's microprocessor systems. The schematic is shown in Figure 2.

V_{IN} = 5V, ±10%

V_{OUT} = 3.3V, ±5%

I_{OUT} = 3.5A typical, 4A maximum

Transient Response: 5% to 75% I_{OUTmax} in 100nsec, Vreg = ±5%

In order to select a pass device for the design, the dropout voltage requirements must first be established. Input voltage tolerance, along with the voltage drop across the current sense resistor, must be taken into account. The sense resistor value is calculated based on the maximum output current specification of the regulator and the current limit threshold of the UC3633. In order to ensure the regulator can deliver 4A under worst case conditions, the maximum resistor value, including tolerance, is given by:

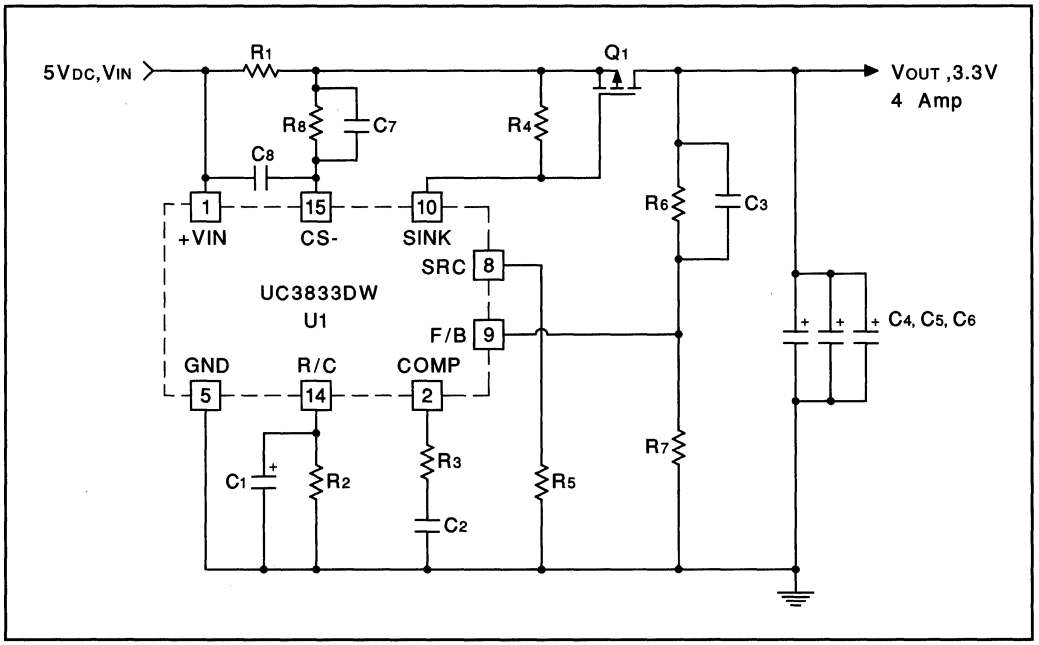


Figure 2: A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

$$R_{MAX} = \frac{V_{CLmin}}{I_{OUT}} \quad (1)$$

$$R_{MAX} = \frac{0.093}{4} = 23.25m\Omega$$

Using a 5%, 22mΩ sense resistor and low line conditions, the dropout requirement for the pass device is calculated as follows:

$$V_{DO} = V_{INmin} - I_{OUTmax}(R_{SENSEmax}) - V_{OUT} \quad (2)$$

$$V_{DO} = 4.5 - 4(1.05)(0.022) - 3.3 = 1.29V$$

This dropout voltage results in a maximum MOSFET $R_{DS}(on)$ of 0.323Ω. In addition, logic level gate characteristics are required in order to ensure adequate gate enhancement with a 5 volt input. These requirements are easily met with the MTP50P03HDL's 30mΩ (T_C=25°C) on-resistance and 2.0V maximum gate threshold voltage.

Having selected the pass device, the UC3833 output driver can now be configured. While the simplest approach would be to configure the driver as a common emitter, including a small amount of emitter resistance eliminates the drive transistor's β from the loop gain expression, thereby simplifying the frequency compensation. Resistors R6 and R7 attenuate and feedback the output voltage to the inverting input of the error amplifier.

Sprague 595D surface mount tantalum capacitors were chosen for the output based upon their ESR/ESL specifications and package style. By paralleling three 270µF, 10V capacitors, the equivalent ESR/ESL is reduced by 1/3, providing an equivalent impedance of approximately 13mΩ typical and 60mΩ maximum at 100kHz. Surface mount packaging helps to further reduce the parasitic effects induced by component leads. The equivalent 810µF provides more than sufficient capacitance to keep the transient voltage drop within specification.

SMALL SIGNAL AC RESPONSE

With the driver and power stage configured, the voltage and current control loops can now be analyzed and properly compensated. Figure 3 illustrates the basic configuration of the two loops. The frequency response of the MOSFET driver includes a gain factor of R4/R5 with a pole introduced from the combination of the MOSFET's gate to source capacitance and R4. The transconductance of the MOSFET is represented by g_{FS}. Modeling the load as a resistance in parallel with the output capacitor and it's associated ESR

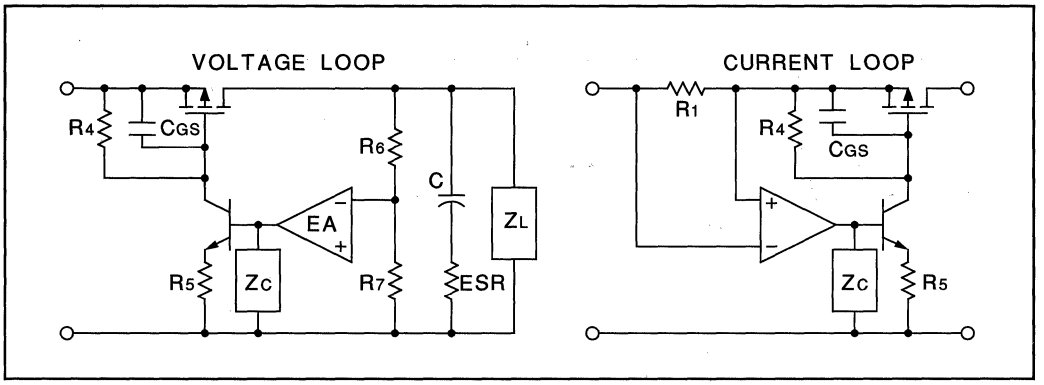


Figure 3. Basic configuration of the voltage and current control loops.

results in a loop gain expression, excluding the error amplifier, of:

$$A_V = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})}\right) \cdot \left(g_{FS}\left(\frac{R_L\,(1 + s(ESR)C)}{(1 + s(R_L + ESR)C)}\right)\right)\left(\frac{R_7}{R_6 + R_7}\right) \quad (3)$$

The dashed curves of Figure 4a represent the resulting voltage loop response. Although the response is stable, the low frequency gain and closed loop accuracy are limited. This is easily improved by compensating the UC3633's error amplifier using a series RC network. Doing so introduces a pole at 0Hz, thereby improving the DC regulation, in addition to a zero at $1/(2\pi RC)$Hz. The zero is located between the poles resulting from the load and the MOSFET gate to source capacitance. Together with the ESR zero, they provide enough phase boost to maintain adequate phase margin. Adding a capacitor across R6 helps to squeeze additional bandwidth from the loop by introducing another pole/zero pair. The gain and phase of the compensated voltage loop (solid lines) are also shown in Figure 4a.

Having stabilized the voltage loop, the current loop can now be examined. The established compensation impedance must be taken into account as both the current and error amplifier share a common output node. The complete current loop expression, including the transconductance (g_M) of the current amplifier, is given below:

$$A_I = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})}\right) \cdot \left(g_{FS}R_1\right)\left(\frac{g_M\,(1 + sR_3C_2)}{sC_2}\right) \quad (4)$$

The corresponding response is shown in Figure 4b. From this plot, it is evident the loop lacks sufficient phase margin to be stable under all conditions. Filtering the current signal with the network composed of R8, C7 and C8, as shown in Figure 2, introduces a pole and zero according to the following transfer function, rolling off the current loop gain without effecting the voltage loop. The gain and phase of the compensated current loop (solid lines) are also shown in Figure 4b.

$$\frac{V_O(s)}{V_I(s)} = \frac{(1 + sR_8C_7)}{(1 + sR_8(C_7 + C_8))} \quad (5)$$

When performing small signal analysis such as this, the use of a spreadsheet program can prove invaluable. The software can be easily configured to provide Bode plots using pole and zero locations input by the user. The graphical output allows the user to quickly evaluate a variety of compensation techniques and relatively easily optimize the design.

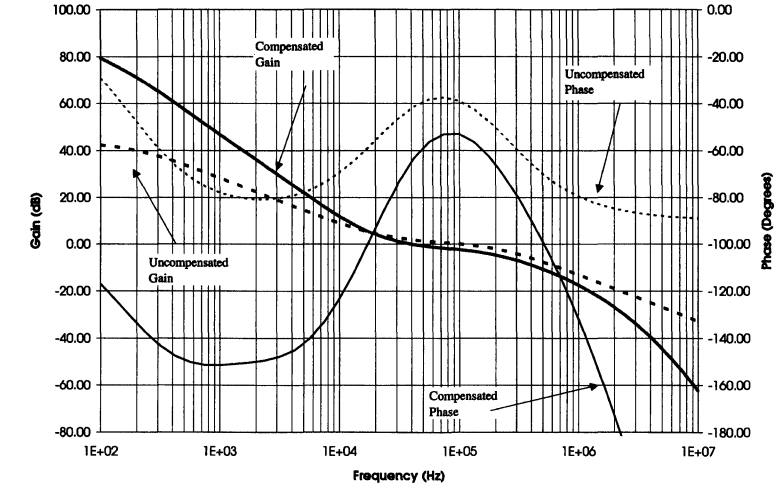
OVERCURRENT PROTECTION AND THERMAL MANAGEMENT

Overcurrent protection is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the comparator threshold the UC3833 begins to modulate the output driver. During the on-time the current sense amplifier provides constant output current by maintaining a fixed voltage across R1. On and off times are controlled by timing components C1 and R2 according to the following expressions:

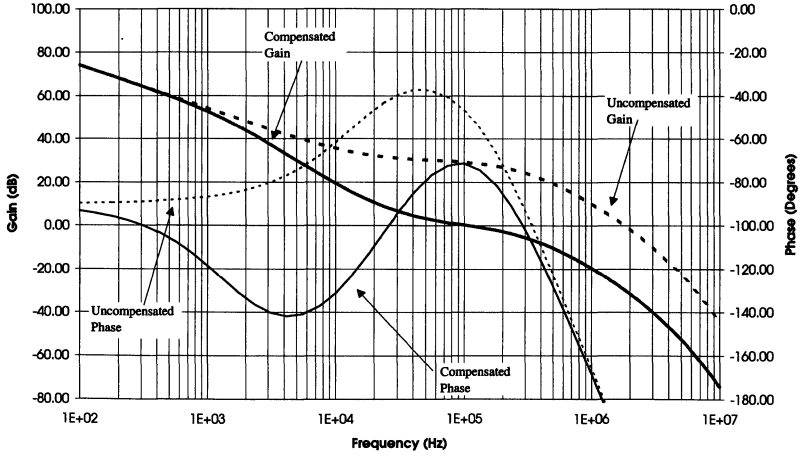
$$T_{ON} = 0.693(10k)(C_T) \quad (6)$$

$$T_{OFF} = 0.693(R_T)(C_T) \quad (7)$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{10k}{10k + R_T} \quad (8)$$



(A)



(B)

Figure 4: Uncompensated and compensated open loop responses for the circuit of Figure 2. (A) Voltage Loop, (B) Current Loop.

When implementing switchmode protection, the "on" time (T_{ON}) must be of sufficient duration to charge the output capacitance during a normal startup sequence or when recovering from a fault. If not, the charge accumulated on the output capacitor will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on. A maximum load current of just less than the trip limit results in the difference between the I_{MAX} and I_{TRIP} values as the current available to charge the output capacitance. In this case the minimum "on" time can be calculated as follows:

$$T_{ONmin} = \frac{C_{OUTmax} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}} \quad (9)$$

The duty cycle can then be adjusted to minimize power dissipation using equation (8).

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.5 volt input and a maximum output of 4A, the power dissipated in Q1 is given by:

$$P = (V_{IN} - V_{RSENSE} - V_{OUT})(I_{OUT}) \quad (10)$$

$$P = (5.5 - 4(0.022)(0.95) - 3.3)4 = 8.47W$$

The thermal resistivity of the MOSFET is specified as 1.0°C/W for the TO-220 package style. Assuming an ambient temperature of 50°C and a case to heat sink resistivity of θcs=0.3°C/W, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (11)$$

$$25 = 50 + 8.47(1.0 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \leq 7.55°C/W$$

Based on this analysis, any heatsink with a thermal resistivity of 7.55°C/W or less should suffice. Under short circuit conditions the output current will be limited to 6.14A at a 5% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = \Big(\big(V_{INmax} - (I_{OUT})(R_{SENSE})\big)I_{OUT}\Big)(d.c.) \quad (12)$$

$$P = \Big(\big(5.5 - 6.14(0.022)\big)6.14\Big)0.05 = 1.65W$$

Without switchmode protection, the short circuit power dissipation would be 33W, almost four times the nominal dissipation!

PRACTICAL CONSIDERATIONS

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

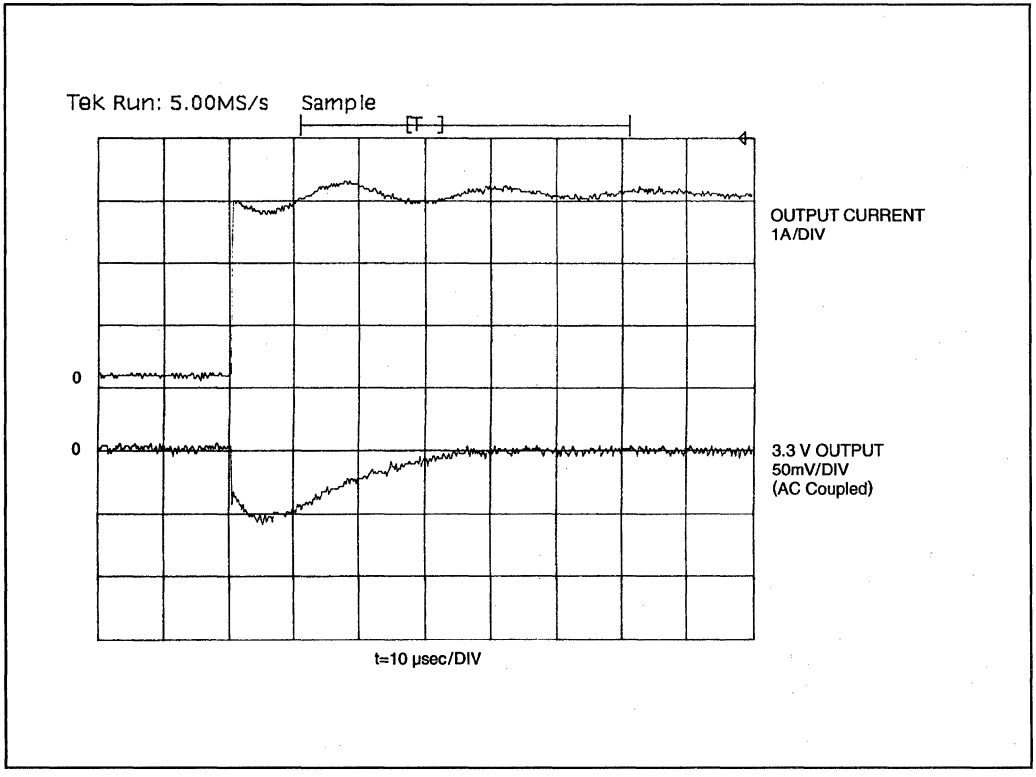


Figure 5: Transient response of the regulator illustrated in Figure 2 with a time base of 10 µsec.

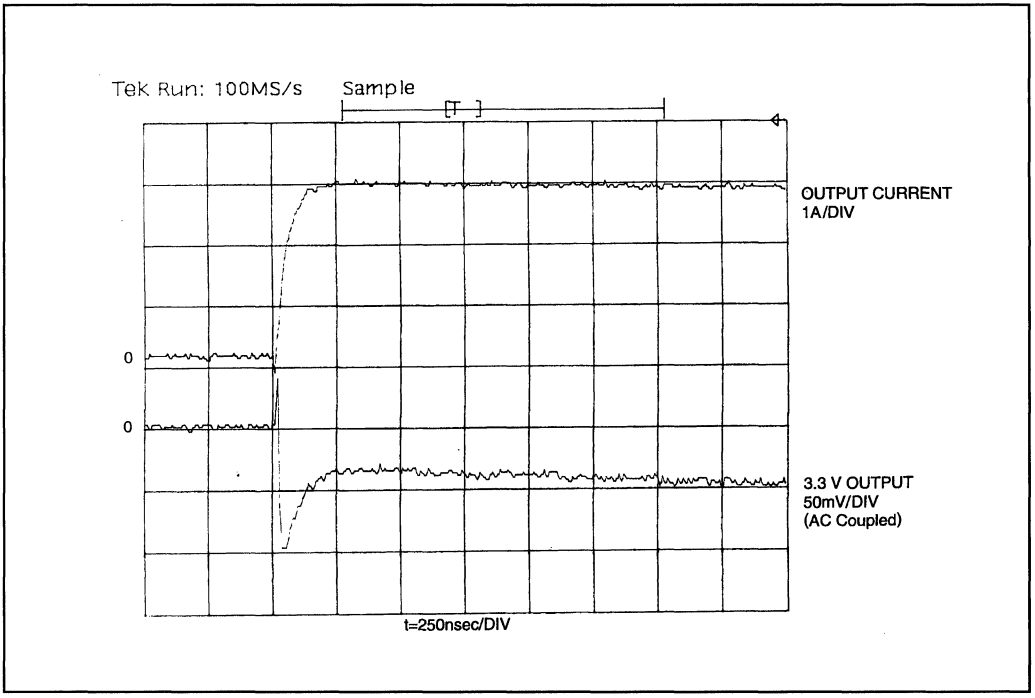


Figure 6: Transient response of the regulator illustrated in Figure 2 with a timebase of 250 nsec.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UC3833 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation!! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A.

PERFORMANCE

The efficiency of the regulator is 65.7% in a typical application with 3A of output current and a 5.0V input. Under maximum load and worst case conditions, the efficiency drops to 60%. During a short circuit scenario the regulator limits the peak current to approximately 6A. At the 5% duty cycle set by C1 and R2, the average current is 300mA, resulting in less than 2W of power dissipated in the MOSFET!

The design provides a worst case DC regulation of ±3% using the UC3833 in conjunction with 1% feedback resistors. If even tighter tolerance is required, the UC3832 can be substituted along with 0.1% resistors. The UC3832 has provisions for an external voltage reference allowing increased performance over the UC3833's ±1% internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 5 illustrates how the design behaves during the specified 100nsec transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 5. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable state within 40μsec. Figure 6 shows the same response with the timebase expanded to 250nsec. In this plot, the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

SUMMARY

The circuit described in this application note was specifically designed to meet the demanding performance requirements of today's

TABLE I

VOUT	Io	R6	R1	COUT	θSAmax	Applications
3.0V	3A	1k	0.03	810µF	9.06°C/W	D/A converters, Gate Arrays
	5A	1k	0.0169	1320µF	4.91°C/W	
	7A	1k	0.012	1980µF	3.13°C/W	
2.7V	3A	698	0.03	810µF	7.9°C/W	MCUs
	5A	698	0.0169	1320µF	4.22°C/W	
	7A	698	0.012	1980µF	3.64°C/W	
2.5V	3A	499	0.03	810µF	7.28°C/W	Low voltage digital logic
	5A	499	0.0169	1320µF	3.84°C/W	

Notes: 1. Thermal resistivities assume 50°C ambient and max TJ of 125°C.
2. COUT is comprised of multiple Sprague 595 style tantalum capacitors.

microprocessors. It is capable of providing excellent transient response with reasonable efficiency for less cost and complexity than a switching regulator. The design is easily modified to accommodate other output voltage and current requirements. Table I provides the necessary component substitutions to achieve a variety of the more popular output voltages and their typical applications. The same MTP50P03HDL MOSFET is used for all designs.

Output voltages below 2.0V dictate the use of a UC3832. The UC3832 enables the user to set the error amplifier voltage reference below 2.0V. In the UC3833 the noninverting error amplifier input is internally committed to 2.0V. For additional information regarding the UC3832/3 linear controllers, consult Unitrode application note U-116. Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectfully.

REFERENCES

[1] "Versatile UC1834 Optimizes Linear Regulator Efficiency", Application Note U-95, Unitrode Integrated Circuits, Merrimack, NH,1993-94.

[2] Mammano, R., Radovsky, J. and Harlan, G. "A New Linear Regulator Features Switch Mode Overcurrent Protection", Application Note U-116, Unitrode Integrated Circuits, Merrimack, NH,1993-94.

PARTS LIST:

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1, C8 = 1µF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2, C3 = 0.1µF		
R3, R8 = 100Ω	C4, C5, C6 = 270µF		
R4 = 300Ω	C7 = 33000pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

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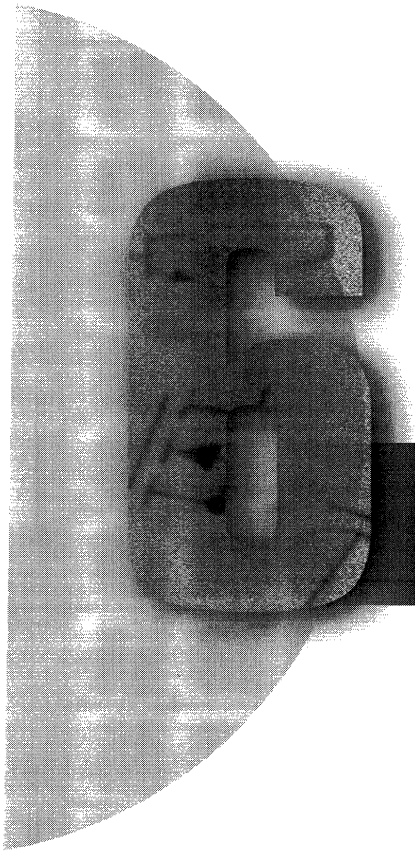

Power Drivers

Power Drivers

Power and FET Drivers	UNITRODE PART NUMBER				
	L293/D	UC2950	UC3702	UC3705	UC3706
Power Driver	Quad	Single		Single	Dual
FET Driver					
Isolated Driver Pairs					
Relay Drivers			Quad		
Output Configuration	Non-Inverting	Sink / Source TTL	Non-Inverting	Complementary	Complementary
Enable					
Inhibit	Y		Y		Y
Analog Stop					Y
Output Rise Time	250ns			60ns	60ns
Maximum Voltage	36V	35V	42.5V	40V	40V
Peak Output Current	2.0A / 1.2A	4.0A	50mA per Relay	1.5A	1.5A
Application / Design Note				U-111, U-118, U-137	U-111, U-118, U-137
Pin Count❖	16, 28	5	16	5, 8	16
Page Number	PS/6-5	PS/6-10	PS/6-12	PS/6-16	PS/6-19

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3707	UC3708	UC3709	UC3710	UC3711
Power Driver	Dual	Dual			
FET Driver			Single	Single	Dual
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Complementary	Non-Inverting	Non-Inverting	Complementary	Non-Inverting
Enable		Y			
Inhibit	Y				
Analog Stop	Y				
Output Rise Time	50ns	75ns	40ns	40ns	20ns
Maximum Voltage	40V	35V	40V	20V	40V
Peak Output Current	1.5A	3.0A	1.5A	6.0A	1.5A
Application / Design Note	U-111, U-118, U-137	DN-35, U-111, U-137	U-111, DN-118, U-137	U-111	U-111
Pin Count❖	16	8, 16	8, 16	5, 8, 16	8
Page Number	PS/6-24	PS/6-31	PS/6-35	PS/6-38	PS/6-41

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3714	UC3715	UC3724	UC3725	UC3726
Power Driver					Transmitter
FET Driver	Dual	Dual	Transmitter	Single	
Isolated Driver Pairs			FET Drv	FET Drv	IGBT Drv
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting	Non-Inverting	Non-Inverting
Enable	Y	Y			
Inhibit					
Analog Stop					
Output Rise Time	100ns / 50ns	100ns / 50ns	30ns	30ns	75ns
Maximum Voltage	20V	20V	40V	40V	40V
Peak Output Current	1.0A / 2.0A	1.0A / 2.0A	2.0A	2.0A	4.0A
Application / Design Note	U-111	U-111	DN-35, U-127	DN-35, U-127	DN-57, DN-60, U-143C
Pin Count❖	8, 16	8, 16	8, 16	8, 16	16, 28
Page Number	PS/6-43	PS/6-43	PS/6-50	PS/6-53	PS/6-57

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3727	UCC37423+	UCC37424+	UCC37425+	UCC37523+
Power Driver	Single				
FET Driver		Dual	Dual	Dual	Dual
Isolated Driver Pairs	IGBT Drv				
Relay Drivers					
Output Configuration	Non-Inverting	Inverting	Non-Inverting	One Inverting, One Non-Inverting	Inverting
Enable					Y
Inhibit					
Analog Stop					
Output Rise Time	75ns	20ns	20ns	20ns	20ns
Maximum Voltage	40V	20V	20V	20V	20V
Peak Output Current	4.0A	3.0A	3.0A	3.0A	3.0A
Special Features		UVLO	UVLO	UVLO	UVLO, Adaptive LEB
Application / Design Note	DN-57, DN-60, U-143C				
Pin Count❖	20, 28	8, 16	8, 16	8, 16	8, 16
Page Number	PS/6-62	PS/6-68	PS/6-68	PS/6-68	PS/6-73

❖The smallest available pin count for thru-hole and surface mount packages.
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Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UCC37524+	UCC37525+	UCC3776		
Power Driver					
FET Driver	Dual	Dual	Quad		
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting		
Enable	Y	Y	Y		
Inhibit					
Analog Stop					
Output Rise Time (ns)					
Maximum Voltage	20V	20V	18V		
Peak Output Current	3.0A	3.0A	1.5A / 2.0A		
Special Features	UVLO, Adaptive LEB	UVLO, Adaptive LEB	UVLO		
Application / Design Note					
Pin Count❖	8, 16	8, 16	16		
Page Number	PS/6-73	PS/6-73	PS/6-79		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product


UNITRODE

Push-Pull Four Channel Driver

FEATURES

- Output Current 1A Per Channel (600mA for L293D)
- Peak Output Current 2A Per Channel (1.2A for L293D)
- Inhibit Facility
- High Noise Immunity
- Separate Logic Supply
- Over-Temperature Protection

DESCRIPTION

The L293 and L293D are quad push-pull drivers capable of delivering output currents to 1A or 600mA per channel respectively. Each channel is controlled by a TTL-compatible logic input and each pair of drivers (a full bridge) is equipped with an inhibit input which turns off all four transistors. A separate supply input is provided for the logic so that it may be run off a lower voltage to reduce dissipation.

Additionally the L293D includes the output clamping diodes within the IC for complete interfacing with inductive loads.

Both devices are available in 16-pin Batwing DIP packages. They are also available in Power SOIC and Hermetic DIL packages.

TRUTH TABLE

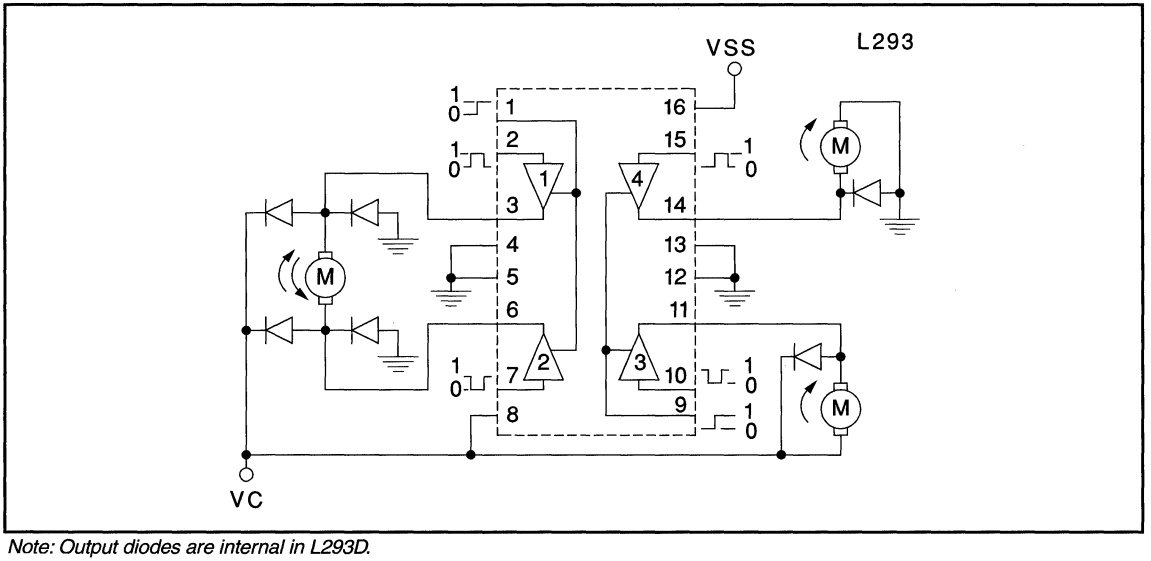
V_I (each channel)	V_{INH}*	V_O
H	H	H
L	H	L
H	L	X**
L	L	X**

**Relative to the considered channel*
***High output impedence*

ABSOLUTE MAXIMUM RATINGS

Collector-Supply Voltage, V_C 36V
Logic Supply Voltage, V_{SS} 36V
Input Voltage, V_I 7V
Inhibit Voltage, V_{INH} 7V
Peak Output Current (Non-Repetitive), I_{OUT} (L293) 2A
I_{OUT} (L293D) 1.2A
Total Power Dissipation
at Tground-pins = 80°C, N Batwing pkg, (Note) 5W
Storage and Junction Temperature, Tstg, T_J ..... -40 to +150°C
Note:Consult packaging section of Databook for thermal limitations and considerations of packages.

BLOCK DIAGRAM

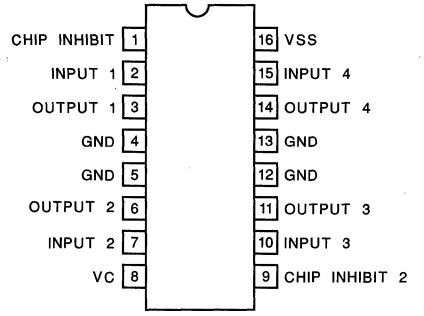


Note: Output diodes are internal in L293D.

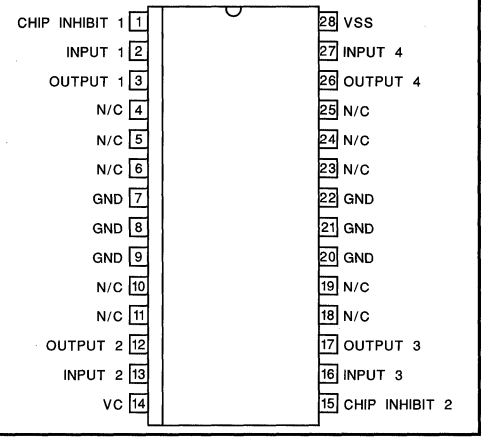
8/94

CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
N Package, SP Package



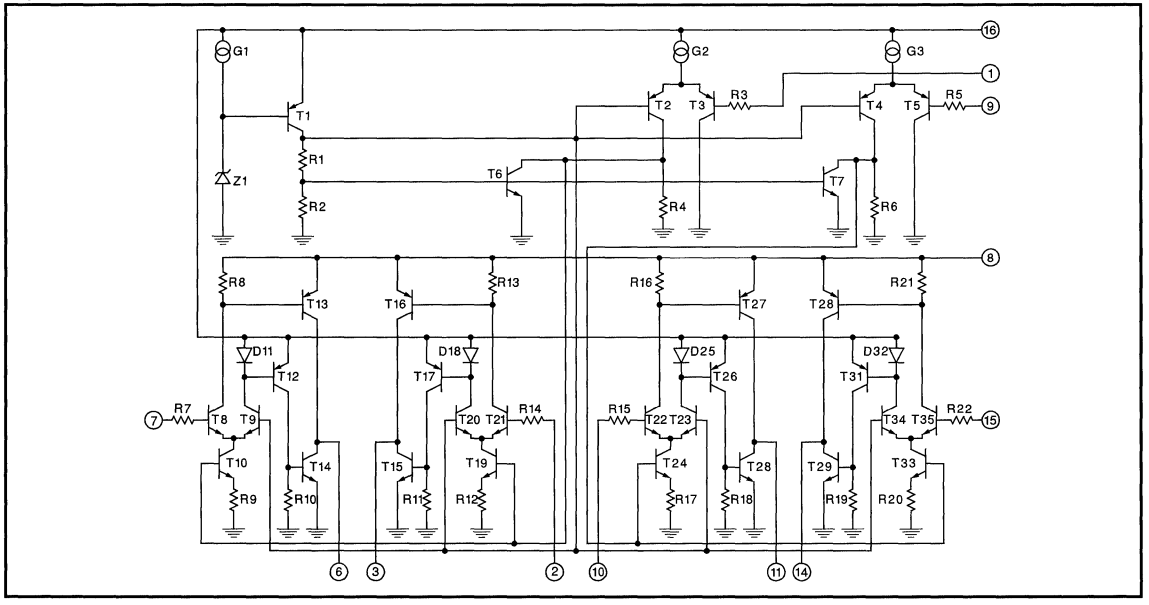
SOIC-28 (TOP VIEW)
DWP Package



ELECTRICAL CHARACTISTICS: (For each channel, V_C = 24V, V_{SS} = 5V, T_{AMB} = 25°C, unless otherwise specified; $T_A = T_J$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Collector Supply Voltage	V_C				36	V
Logic Supply Voltage	V_{SS}		4.5		36	V
Collector Supply Current	I_C	V_I = L, I_O = 0, V_{INH} = H		2	6	mA
		V_I = H, I_O = 0, V_{INH} = H		16	24	mA
		V_{INH} = L			4	mA
Total Quiescent Logic Supply Current	I_{SS}	V_I = L, I_O = 0, V_{INH} = H		44	60	mA
		V_I = H, I_O = 0, V_{INH} = H		16	22	mA
		V_{INH} = L		16	24	mA
Input Low Voltage	V_{IL}		-0.3		1.5	V
Input High Voltage	V_{IH}	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		$V_{SS} \geq 7V$	2.3		7	V
Low Voltage Input Current	I_{IL}	V_I = 0V			-10	µA
High Voltage Input Current	I_{IH}	V_I = 4.5V		30	100	µA
Inhibit Low Voltage	$V_{INH, L}$		-0.3		1.5	V
Inhibit High Voltage	$V_{INH, H}$	$V_{SS} \leq 7V$	2.3		V_{SS}	V
		V_{SS} >7V	2.3		7	V
Low Voltage Inhibit Current	$V_{INH, L}$			-30	-100	µA
High Voltage Inhibit Current	$V_{INH, H}$				10	µA
Source Output Saturation Voltage	V_{CEsatH}	I_O = -1A (-0.6A for L293D)		1.4	1.8	V
Sink Output Saturation Voltage	V_{CEsatL}	I_O = 1A (0.6A for L293D)		1.2	1.8	V
Clamp Diode Forward Voltage (L293D only)	V_F	I_F = 0.6A		1.3		V
Rise Time	T_R	0.1 to 0.9 V_O (See Figure 1)		100		ns
Fall Time	T_F	0.9 to 0.1 V_O (See Figure 1)		350		ns
Turn-on Delay	T_{ON}	0. 5 V_I to 0.5 V_O (See Figure 1)		750		ns
Turn-off Delay	T_{OFF}	0. 5 V_I to 0.5 V_O (See Figure 1)		200		ns

SCHEMATIC DIAGRAM



APPLICATION INFORMATION

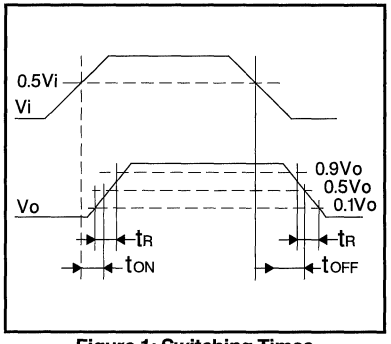


Figure 1: Switching Times

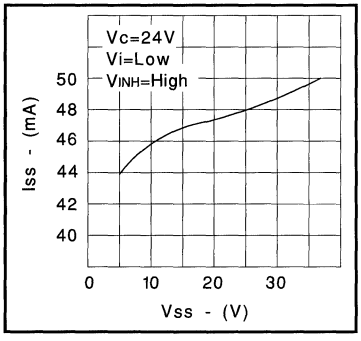


Figure 2: Quiescent Logic Supply Current vs Logic Supply Voltage

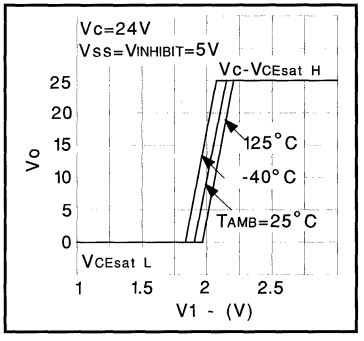


Figure 3: Output Voltage vs Input Voltage

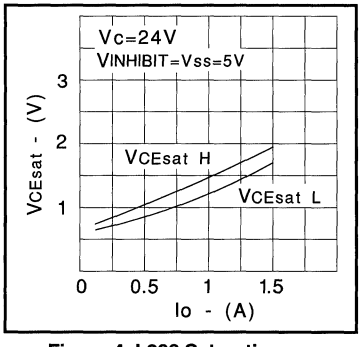


Figure 4: L293 Saturation vs Output Currrent

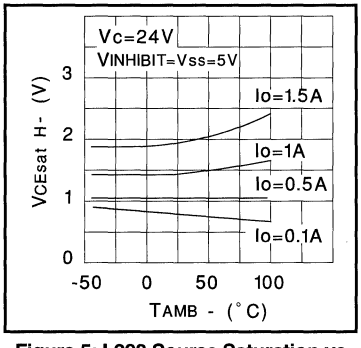


Figure 5: L293 Source Saturation vs Ambient Temperature

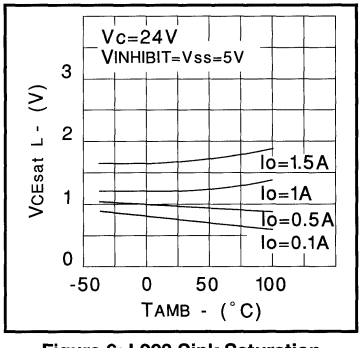


Figure 6: L293 Sink Saturation Voltage vs Ambient Temperature

NOTE: For L293D curves, multiply output current by 0.6.

APPLICATION INFORMATION (Cont.)

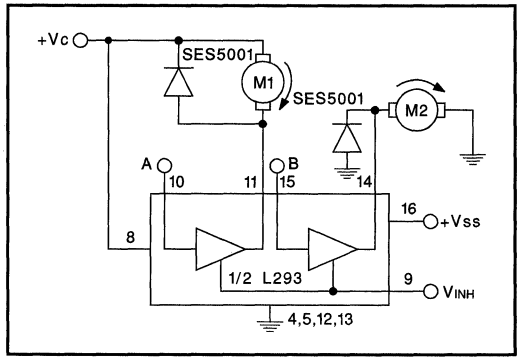


Figure 7: DC Motor Controls (with Connection to Ground and to Supply Voltage)

VINH	A	M1	B	M2
H	H	Fast Motor Stop	H	Run
H	L	Run	L	Fast Motor Stop
L	X	Free Running Motor Stop	X	Free Running Motor Stop

L = Low H = High X = Don't Care

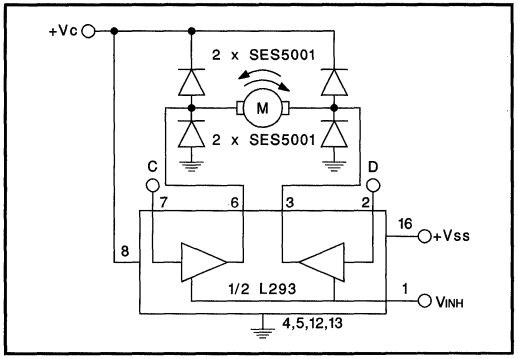


Figure 8: Bidirectional DC Motor Control

INPUTS		FUNCTION
VINH = H	C = H; D = L	Turn Right
	C = L; D = H	Turn Left
	C = D	Fast Motor Stop
VINH = L	C = X; D = X	Free Running Motor Stop

L = Low H = High X = Don't Care

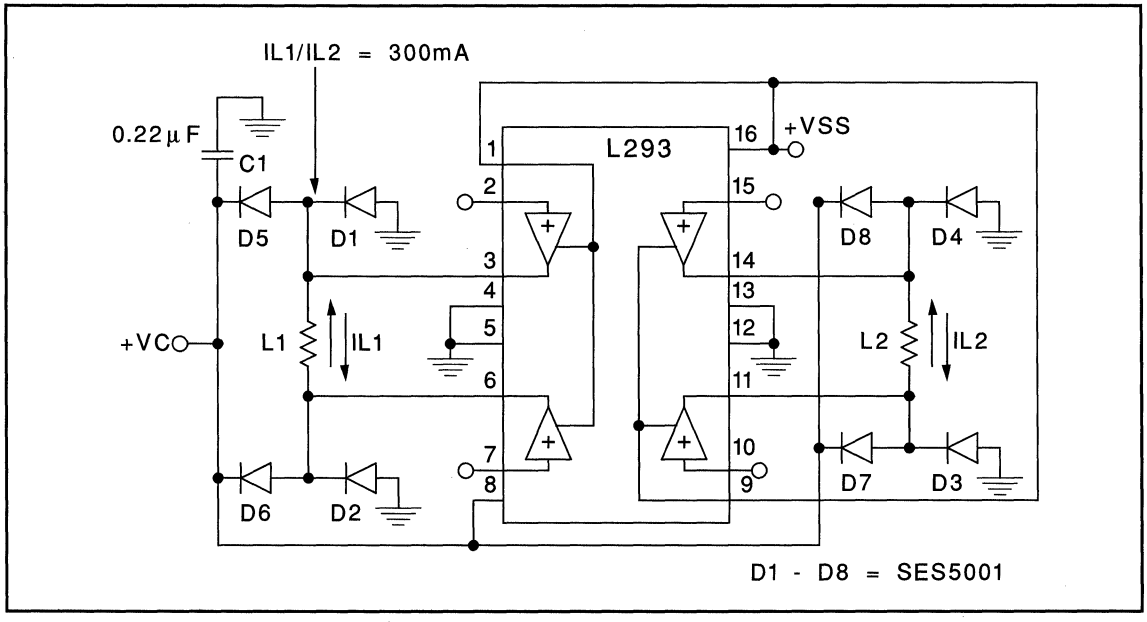


Figure 9: Bipolar Stepping Motor Control

MOUNTING INSTRUCTIONS

The Rthj-amp of the L293 can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heatsink.

The diagram of Figure 13 shows the maximum package power Ptot and the θJA as a function of the side "l" of two equal square copper areas having a thickness of 35μ (see Figure 10). In addition, it is possible to use an external heatsink (see Figure 11).

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The external heatsink or printed circuit copper area must be connected to electrical ground.

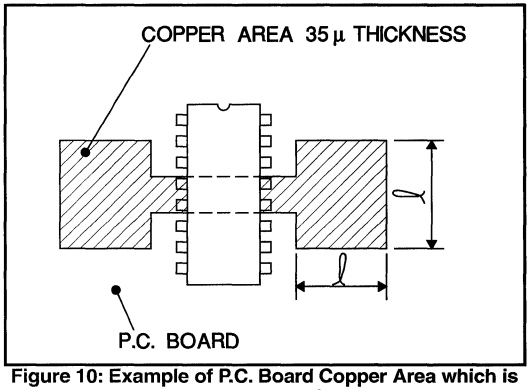


Figure 10: Example of P.C. Board Copper Area which is used as Heatsink

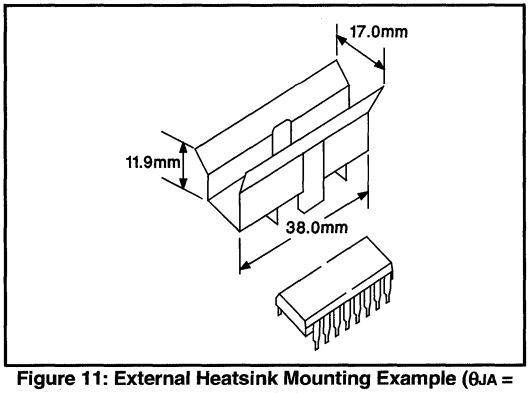


Figure 11: External Heatsink Mounting Example (θJA = 25°C/W)

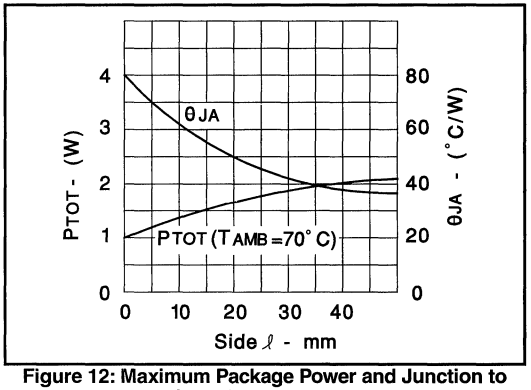


Figure 12: Maximum Package Power and Junction to Ambient Thermal Resistance

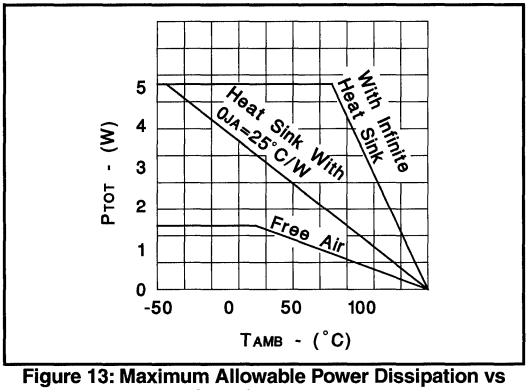


Figure 13: Maximum Allowable Power Dissipation vs Ambient Temperature

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UNITRODE

Half-Bridge Bipolar Switch

FEATURES

- Source or Sink 4.0A
- Supply Voltage to 35V
- High-Current Output Diodes
- Tri-State Operation
- TTL and CMOS Input Compatibility
- Thermal Shutdown Protection
- 300kHz Operation
- Low-Cost TO-220 Package

DESCRIPTION

This device is a monolithic integrated circuit designed to provide high-current switching with low saturation voltages when activated by low-level logic signals. Source and sink switches may be independently activated without regard to timing as a built-in interlock will keep the sink off if the source is on.

This driver has the high current capability to drive large capacitive loads with fast rise and fall times; but with high-speed internal flyback diodes, it is also ideal for inductive loads. Two UC2950s can be used together to form a full bridge, bipolar motor driver compatible with high frequency chopper current control.

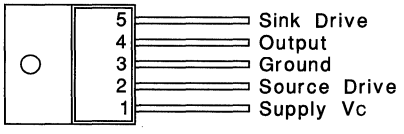
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Range, V_C	8V to 35V
Output Voltage Range, V_O	-3.0V to V_C+3V
Input Voltage Range, V_{IN}	-0.3V to +7.0V
Peak Output Current (100 ms, 10% DC)	±4.0A
Continuous Output Current	±2.0A
Power Dissipation with Heat Sink	15W
Power Dissipation in Free Air	2W
Operating Temperature Range, T_A	-20°C to +100°C
Storage Temperature Range, Ts	-55°C to +125°C

Note 1: Consult Packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAM

5-PIN TO-220 (TOP VIEW)
T Package

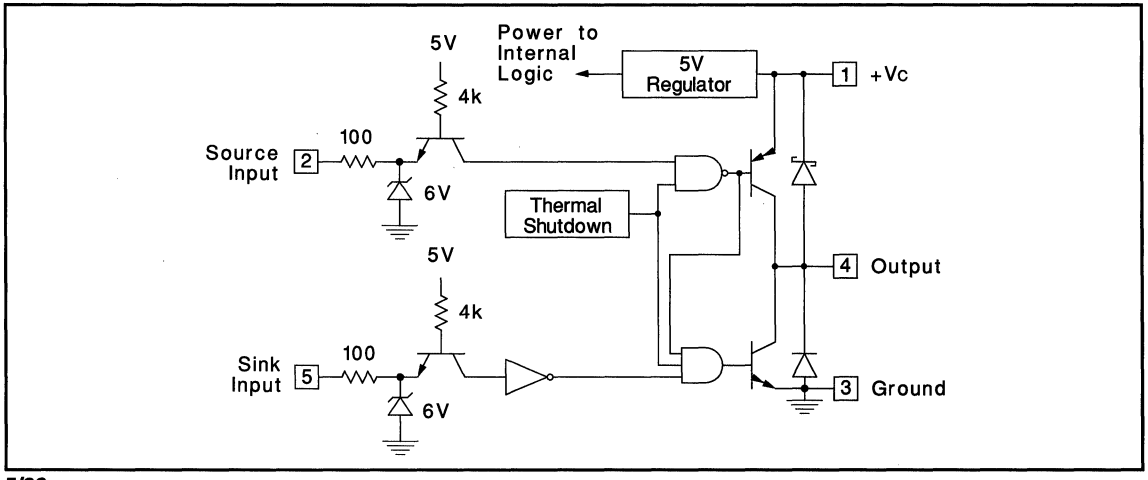


TRUTH TABLE

Source Drive Pin 2	Sink Drive Pin 5	Output Pin 4
Low	Low	Low
Low	High	Off
High	Low	High
High	High	High

Note: With no load, output voltage will be HIGH in the OFF state.

SIMPLIFIED SCHEMATIC



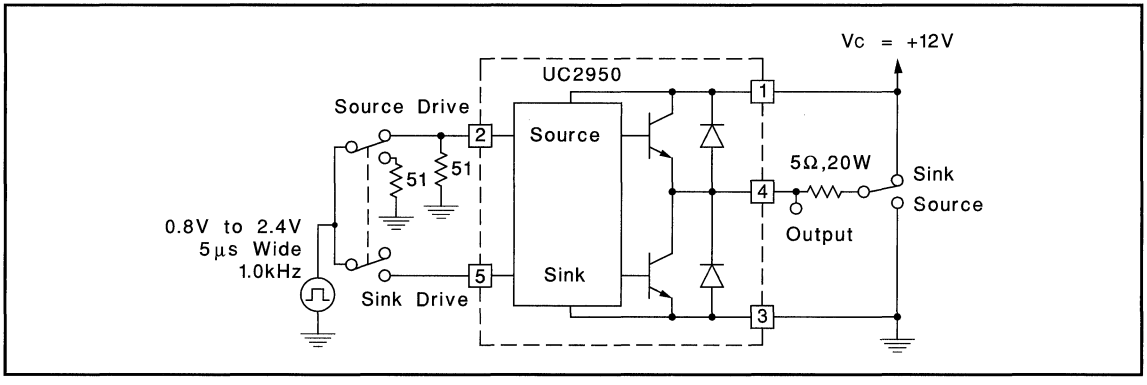
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_C = 35V, T_A = -20°C to +100°C, V_{IL} = 0.8V, V_{IH} = 2.4V for either input, T_A = T_J.

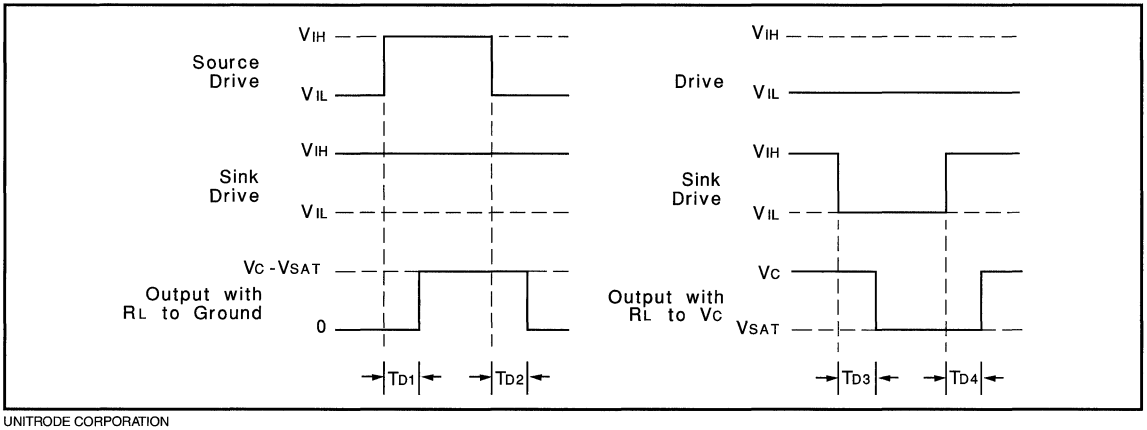
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage to V_C	Output Off		20	500	µA
Output Leakage to Ground	Output Off		-200	-500	µA
Output Sink Saturation	V_{OL}, I_L = 2.0A		1.2	2.0	V
Output Source Saturation	(V_C-V_{OL}), I_L = -2.0A		1.2	2.0	V
Sink Diode Forward Voltage	I_D = -2.0A		1.4	2.0	V
Source Diode Forward Voltage	I_D = 2.0A		1.4	2.0	V
Input Current	Either Input, V_I = 5V		20	100	µA
	Either Input, V_I = 0V		-1.0	-1.6	mA
Supply Current	Output High		20	30	mA
	Output Low		10	20	mA

SWITCHING CHARACTERISTICS: See Test Circuit. V_C = 12V, R_L = 5Ω, T_A = 25°C. Guaranteed by design, not 100% tested in production.

PARAMETERS	MIN	TYP	MAX	UNITS
Source Turn-On Delay, t_{D1}		300	500	ns
Source Turn-Off Delay, t_{D2}		1.0	2.0	µs
Sink Turn-On Delay, t_{D3}		200	400	ns
Sink Turn-Off Delay, t_{D4}		100	300	ns
Cross-Conduction Current Spike When Source and Sink are Activated Together		0.6	1.0	µs

SWITCHING TEST CIRCUIT





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Quad PWM Relay Driver

FEATURES

- Maintains Constant Average Relay Voltage With Varying Supply Voltages
- VBUS Voltages up to 42.5V
- Up to 50mA per Relay
- Integrated Schottky Flyback Diodes
- Individual Relay Control Inputs
- Short Circuit Protection
- User Selectable Operating Center Frequency and Relay Voltage
- Global Reset

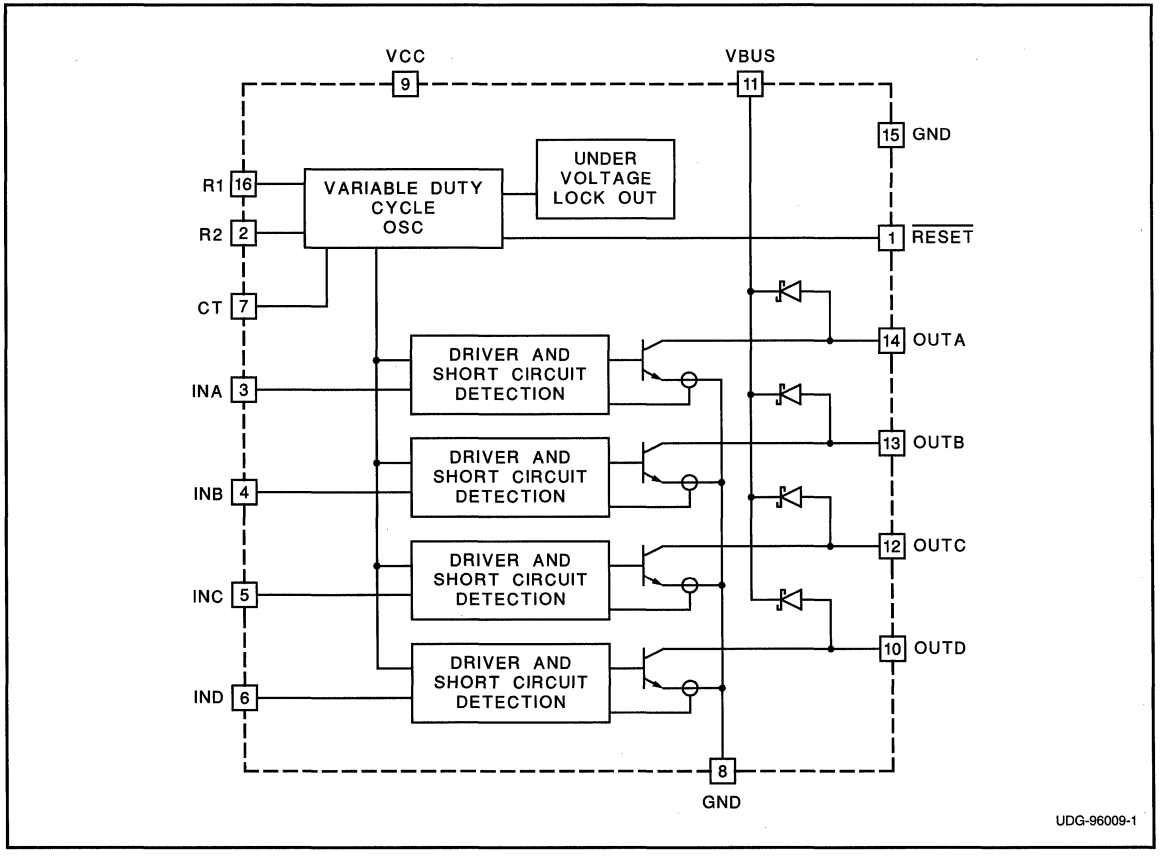
DESCRIPTION

The UC3702 Quad Relay Driver is intended to drive up to four relays from logic inputs using an unregulated relay voltage supply. The relays are driven from the Bus supply in a power efficient PWM converter fashion. The relay coil is used as the inductive element. (See the application's section concerning the relay selection.) VBUS must be higher then the rated relay voltage. Short circuit protection is provided on chip with periodic retry.

The UC3702 requires a +5V logic supply as a reference. Two external resistors program the effective relay voltage and a capacitor sets the nominal operating frequency. Internal Schottky diodes eliminate the need for any external power components.

In typical applications, the UC3702 grants the user the flexibility to choose the most cost effective relay without the added burden of generating a separate relay supply voltage. The UC3702 will even function with a poorly regulated supply VBUS, containing significant 100Hz or 120Hz ripple.

BLOCK DIAGRAM



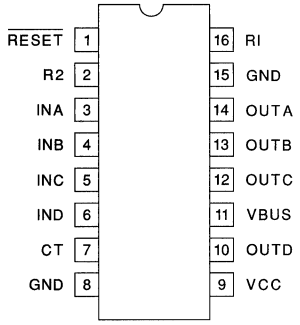
ABSOLUTE MAXIMUM RATINGS

VBUS . . . . . +50V
VCC . . . . . +9V
Input Voltage . . . . . –0.3V to VCC + 0.3V
Average Current per Relay 50mA
Total Output Capacitance 25pF
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
J or N, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1702; –25°C to +85°C for UC2702; 0°C to +70°C for UC3702; VBUS = 34V, VCC = 5V, $\overline{\text{RESET}}$ = VCC, R2 = 43.2kΩ; R1 = 203kΩ; CT = 220pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Section					
VCC		4.5	5	8	V
VCC Supply Current	$\overline{\text{RESET}}$, INA, INB, INC, IND = VCC		4	6	mA
VBUS				42.5	V
Oscillator Section					
NOMINAL Operating Frequency	R1 = 203kΩ, R2 = 43.2kΩ, CT = 220pF	150	175	200	kHz
R1		100	202	500	kΩ
R2		20	42.5	80	kΩ
CT		100			pF
Output Driver VBUS = 20V					
Rated Relay Current				50	mA
Short Circuit Current		100	175		mA
Diode Leakage Current	Control Input Low, V_{OUTX} = VBUS		0.05	5	µA
Diode Forward Voltage			500		mV
Averaged Output Voltage Error	UC2702, UC3702 (Note 1)	–10		10	%
	UC1702	–20		20	%
Control Inputs (INA, INB, INC, IND)					
Logic Low				0.5	V
Logic High		3		VCC	V
TON / TOFF Delay				250	ns
Input Current		–1	0	1	µA
Input Current	V_{IN} = 5V		70	120	µA
$\overline{\text{RESET}}$					
TON / TOFF Delay				2	µs
Input Current	V_{IN} = 0.3V	–8	–5		µA
Input Current	V_{IN} = 5V	–10	0	10	µA

Note 1: Programmed Average Voltage $= \frac{1.06 \bullet R1 \bullet VCC}{2 \bullet R2} - 400mV$

PIN DESCRIPTIONS

CT: A capacitor from the CT pin to ground sets the oscillator center frequency. Note that the oscillator period must be least an order of magnitude less than the relaxation time constant (L/R) of the relay coil. However, a needlessly high operating frequency only increases power dissipation. For best accuracy, CT should be 220pF or greater.

GND: Both ground pins must be connected to a low noise system ground.

INA, INB, INC, IND: Separate digital control inputs for each of the four relay drivers. An active high input (a logic high) turns on the respective relay. Active low disables the common-emitter drive transistor.

OUTA, OUTB, OUTC, OUTD: Each of these output pins can be connected to the low side of one relay coil. The rated relay coil voltage of all relays to be driven by a single UC3702 must be the same. (It is permissible to use coils with different rated series resistances with a single UC3702, so long as the rated coil voltages are the same and care is taken with respect to the relaxation times of the different relay coils). Output transients are slew rate limited to decrease electro-magnetic radiation.

R1: User selected external resistor must be placed from the R1 pin to the VBUS voltage supply. Sensing the VBUS amplitude, the oscillator varies its ON duty cycle such that the average voltage across the driver coil is constant.

R2: User selected external resistor must placed from R2 pin to GND. This resistor, in conjunction with the external timing capacitor, CT, sets the OFF cycle time of the oscillator. For best accuracy, use 42.3kΩ for R2.

$\overline{\text{RESET}}$: Digital reset pin is active low. When $\overline{\text{RESET}}$ is low, the oscillator stops running and all drivers are open collector.

VCC: Nominally 5V. In addition to supplying the voltage for the driver logic and oscillator circuit, the VCC supply is used as reference for the generating the average relay voltage. It is recommended that the VCC be regulated to ±5% of its nominal value or better to insure good regulation. Good decoupling with a minimum of 1µF is necessary.

VBUS: This pin should be tied to a low impedance voltage source at some voltage higher than the rated voltage of the relay coil to be driven. VBUS may even be a poorly filtered rectified sin wave, as the UC3702 will regulate the correct duty cycle. Good decoupling with a minimum of 1µF is necessary.

APPLICATIONS INFORMATION

The UC3702 must be programmed for a specific relay voltage. The table given below has some suggested values of R1, R2, and CT. The VCC supply voltage is assumed to be 5V.

Rated Relay Voltage	R1	R2	CT
9V	153kΩ	43.2kΩ	220pF
12V	203kΩ	43.2kΩ	220pF
24V	398kΩ	43.2kΩ	220pF

More generally, the following equation can be used to determine the equivalent average relay voltage:

$$V_{RELAY} = \frac{1.06 \bullet VCC \bullet R1}{2 \bullet R2} - 400mV$$

Industrial Relays

The UC3702 takes advantage of the inductance of the relay coil to regulate a constant coil current in a manner very similar to a switch-mode power supply. To use the UC3702 correctly, the coil characteristics must be known. The rated relay voltage is what the relay manufacturers specify as voltage to drive the relay coil with if the coil were driven from a dc source. Most manufacturers also specify the series resistance of the coil. This is the resistance of the copper wire and determines the steady state coil ON current. For example, a 12V relay with a 320Ω series coil resistance with a draw of 37.5mA of constant current. The relay inductance is not typically specified in the manufacturer's short-form datasheet, so the engineer will need an LCR bridge to measure it or request the information from the relay manufacturer.

APPLICATIONS INFORMATION (cont.)

Although the inductance may not be specified in the relay datasheet, it is very repeatable since it is determined by the number of turns and geometry of the relay.

The relay's coil inductance divided by its series resistance is the relay coil's relaxation time constant. It is important that the relaxation time constant be at least an order of magnitude longer than the nominal switching period of the UC3702 to obtain a constant current through the relay coil. This means that some relays may be ill-suited for use with the UC3702.

For example, a common 12V industrial relay has a series resistance of 500Ω and a coil inductance of 500mH. Its relaxation time constant is 1ms, an order of magnitude less than the period of a 10kHz oscillator.

When performing an engineering evaluation of the UC3702 in a system, it is useful to have a current probe. Alternately, a 1Ω resistor can be placed in series with the relay coil in the prototype and differential voltage probes can be used to observe the coil current. (Do not use a large series resistor, as this will impact observed relaxation time constant.)

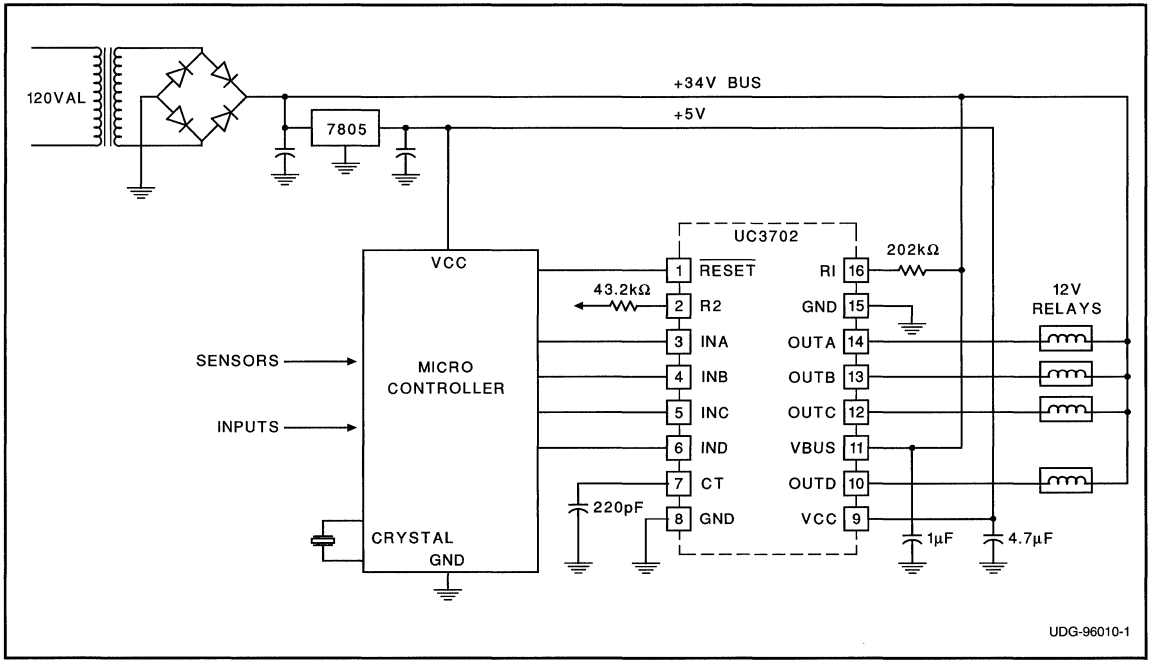
Layout Considerations

The layout of the printed circuit board and good decoupling of the power supplies is critical to proper operation of the UC3702. For best results, high quality 4.7μF tantalum capacitors should be placed as close as possible to the VCC and the VBUS pins.

In addition to decoupling considerations, the R1 and R2 pins are sensitive to capacitive coupling from any of the driver outputs (OUTA - D) which can slew at speeds of 300V/μs. The external resistors R1 and R2 should be placed as close as possible to their respective pins. Avoid routing the outputs directly past these pins without a low impedance trace (such as GND, VCC, or VBUS) in between to act as a capacitive shield.

6

Typical Microcontroller Application Driving 12V Industrial Relays



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application INFO available

UC1705
UC2705
UC3705

High Speed Power Driver

FEATURES

- 1.5A Source/Sink Drive
- 100 nsec Delay
- 40 nsec Rise and Fall into 1000pF
- Inverting and Non-Inverting Inputs
- Low Cross-Conduction Current Spike
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1705 family of power drivers is made with a high speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choice for capacitive line drivers where up to 1.5 amps may be switched in either direction. With both Inverting and Non-Inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both Vs and Vc can independently range from 5V to 40V. For additional application details, see the UC1707/3707 data sheet.

The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to +125°C operation. The UC3705 is specified for a temperature range of 0°C to +70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

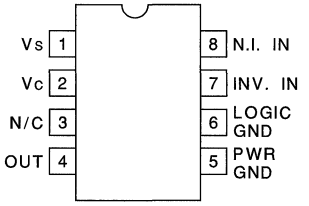
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

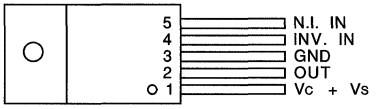
$\overline{OUT} = \overline{INV}$ and N.I.
$\overline{OUT}$ = INV or N.I.

CONNECTION DIAGRAMS

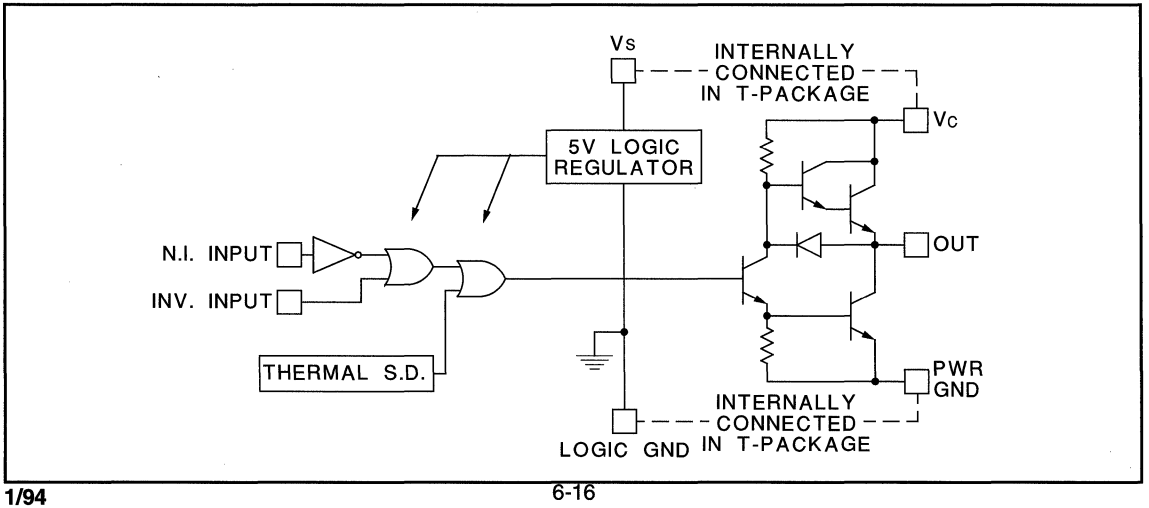
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N or J Package, D Package



5-PIN TO-220
(TOP VIEW)
T Package



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg	T-Pkg
Supply Voltage, V_{IN}	40V	40V	40V
Collector Supply Voltage, V_C	40V	40V	40V
Output Current (Source or Sink)			
Steady-State	±500mA	±500mA	±1.0A
Peak Transient	±1.5A	±1.0A	±2.0A
Capacitive Discharge Energy	20µJ	15µJ	50µJ
Digital Inputs (See Note)	5.5V	5.5V	5.5V
Power Dissipation at T_A = 25°C (See Note)	1W	1W	3W
Power Dissipation at T_A (Leads/Case) = 25°C (See Note)	3W	2W	25W
Operating Temperature Range	0°C to +70°C	-55°C to +125°C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note: All currents are positive into, negative out of the specified terminal.
Digital Drive can exceed 5.5V if input current is limited to 10mA
Consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1705, -25°C to +85°C for the UC2705, and 0°C to +70°C for the UC3705; V_S = V_C = 20V, T_A = T_J.

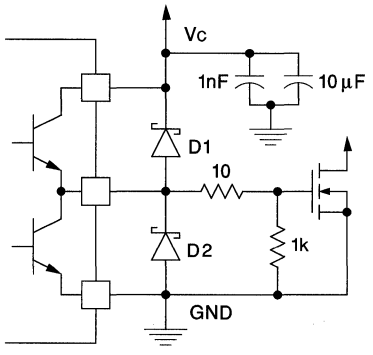
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S Supply Current	V_S = 40V, (Outputs High, T Pkg)		6	8	mA
	V_S = 40V, (Outputs Low, T Pkg)		8	12	mA
V_C Supply Current (N, J Only)	V_C = 40V, Outputs Low		2	4	mA
V_C Leakage Current (N, J Only)	V_S = 0, V_C = 30V		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.5	0.1	mA
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
	I_O = -500mA			2.5	V
Output Low Sat., V_O	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_S = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNIT
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		60	60	60	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
From N. I. Input to Output:					
Rise Time Delay		90	90	90	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		60	60	60	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Ouput Rise	25			ns
	Output Fall	0			ns

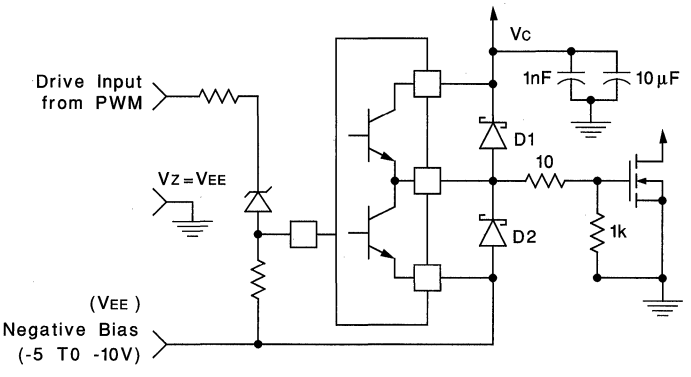
APPLICATIONS

Power MOSFET Drive Circuit



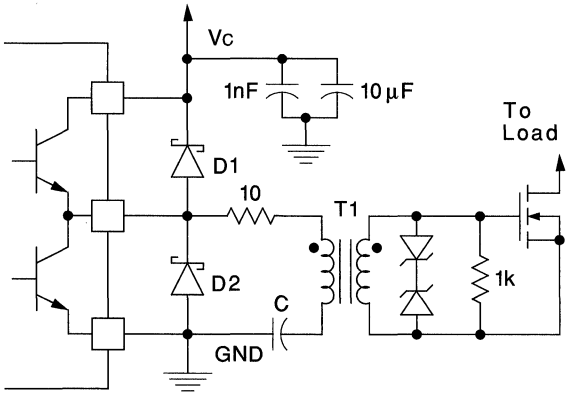
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs.



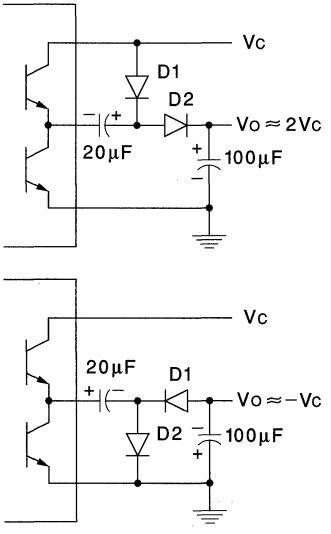
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



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application INFO available

UC1706
UC2706
UC3706

Dual Output Driver

FEATURES

- Dual, 1.5A Totem Pole Outputs
- 40nsec Rise and Fall into 1000pF
- Parallel or Push-Pull Operation
- Single-Ended to Push-Pull Conversion
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog, Latched Shutdown
- Internal Deadband Inhibit Circuit
- Low Quiescent Current
- 5 to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin Surface Mount Package

DESCRIPTION

The UC1706 family of output drivers are made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFET's. These devices implement three generalized functions as outlined below.

First: They accept a single-ended, low-current digital input of either polarity and process it to activate a pair of high-current, totem pole outputs which can source or sink up to 1.5A each.

Second: They provide an optional single-ended to push-pull conversion through the use of an internal flip-flop driven by double-pulse-suppression logic. With the flip-flop disabled, the outputs work in parallel for 3.0A capability.

Third: Protection functions are also included for pulse-by-pulse current limiting, automatic deadband control, and thermal shutdown.

These devices are available in a two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for -55°C to +125°C operation. Also available in surface mount Q and L packages.

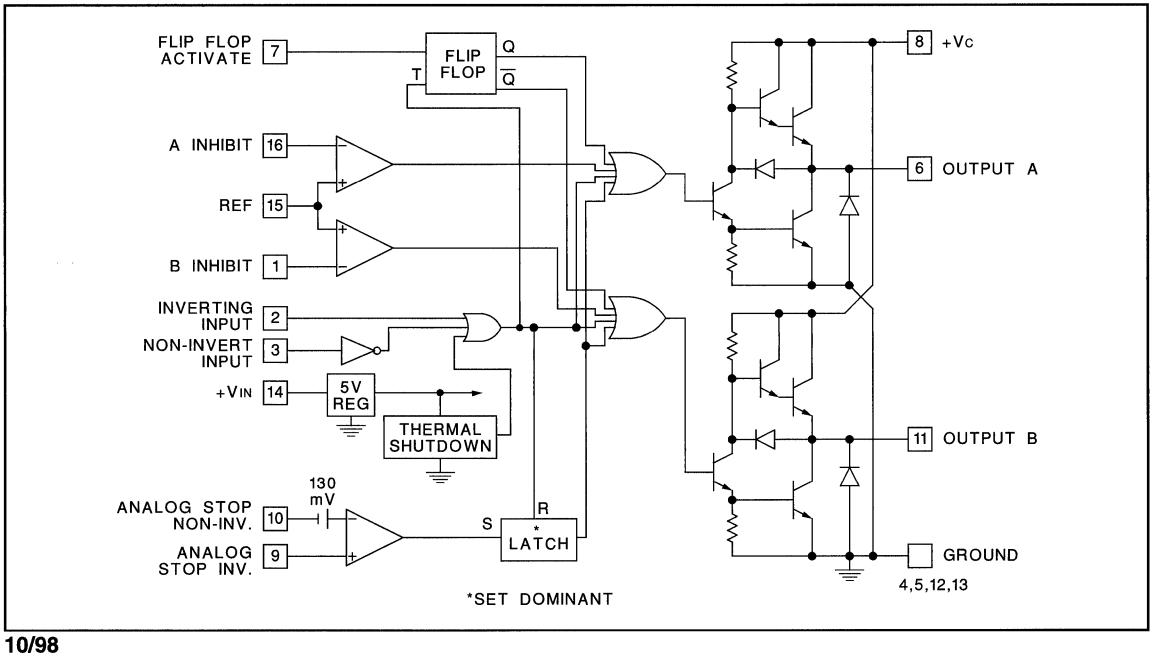
TRUTH TABLE

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

$OUT = \overline{INV}$ and N.I.

$\overline{OUT}$ = INV or $\overline{N.I.}$

BLOCK DIAGRAM



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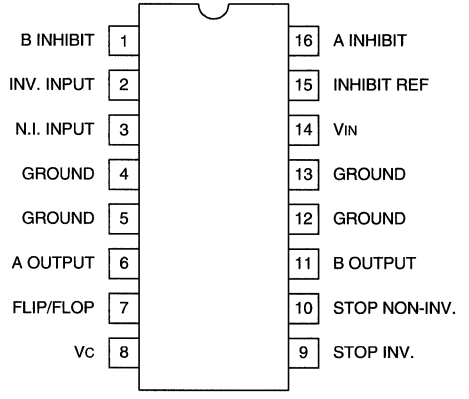
ABSOLUTE MAXIMUM RATINGS

	N--Pkg	J--Pkg
Supply Voltage, V_{IN}	40V	40V
Collector Supply Voltage, V_C	40V	40V
Output Current (Each Output, Source or Sink)		
Steady--State	±500mA	±500mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20µJ	15µJ
Digital Inputs	5.5V	5.5V
Analog Stop Inputs	V_{IN}	V_{IN}
Power Dissipation at T_A = 25°C (See Note)	2W	1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)	5W	2
Operating Temperature Range	--55°C to +125°C	
Storage Temperature Range	--65°C to +150°C	
Lead Temperature (Soldering, 10 Seconds)	300°C	

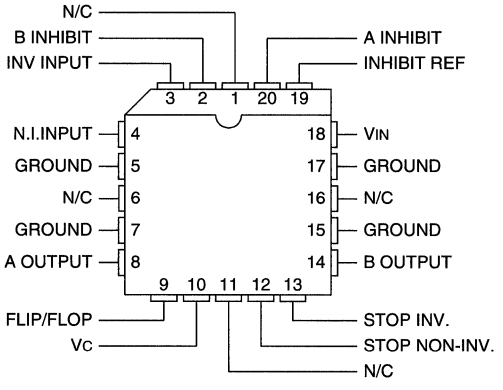
Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified trerminal. Consult Packaging sections of the Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



Note: All four ground pins must be connected to a common ground.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1706, –25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		8	10	mA
V_C Supply Current	V_C = 40V, Outputs Low		4	5	mA
V_C Leakage Current	V_{IN} = 0, V_C = 30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		–0.6	–1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1706, –25°C to +85°C for the UC2706 and 0°C to +70°C for the UC3706; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output High Sat., V_C-V_O	I_O = -50mA			2.0	V
Output Low Sat., V_O	I_O = 50mA			0.4	V
	I_O = 500mA			2.5	V
Inhibit Threshold	V_{REF} = 0.5V	0.4		0.6	V
	V_{REF} = 3.5V	3.3		3.7	V
Inhibit Input Current	V_{REF} = 0		–10	–20	µA
Analog Threshold	V_{CM} = 0 to 15V	100	130	160	mV
Input Bias Current	V_{CM} = 0		–10	–20	µA
Thermal Shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =			UNITS
From Inv. Input to Output:		open	1.0	2.2	nF
Rise Time Delay		110	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		80	90	110	ns
90% to 10% Fall		25	30	50	ns
From N. I. Input to Output:					
Rise Time Delay		120	130	140	ns
10% to 90% Rise		20	40	60	ns
Fall Time Delay		100	120	130	ns
90% to 10% Fall		25	30	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Inhibit Delay	Inhibit Ref. = 1V, Inhibit Inv. = 0.5 to 1.5V	250			ns
Analog Shutdown Delay	Stop Non-Inv. = 0V, Stop Inv. = 0 to 0.5V	180			ns

CIRCUIT DESCRIPTION

Outputs

The totem-pole outputs have been designed to minimize cross-conduction current spikes while maximizing fast, high-current rise and fall times. Current limiting can be done externally either at the outputs or at the common V_C pin. The output diodes included have slow recovery and should be shunted with high-speed external diodes when driving high-frequency inductive loads.

Flip/Flop

Grounding pin 7 activates the internal flip-flop to alternate the two outputs. With pin 7 open, the two outputs operate simultaneously and can be paralleled for higher current operation. Since the flip-flop is triggered by the digital input, an off-time of at last 200nsec must be provided to allow the flip/flop to change states. Note that the circuit logic is configured such that the "OFF" state is defined as the outputs low.

Digital Inputs

With both an inverting and non-inverting input available, either active-high or active-low signals may be accepted. These are true TTL compatible inputs—the threshold is approximately 1.2V with no hysteresis; and external pull-up resistors are not required.

Inhibit Circuit

Although it may have other uses, this circuit is included to eliminate the need for deadband control when driving relatively slow bipolar power transistors. A diode from each inhibit input to the opposite power switch collector will keep one output from turning-on until the other has turned-off. The threshold is determined by the voltage on pin 15 which can be set from 0.5 to 3.5V. When this circuit is not used, ground pin 15 and leave 1 and 16 open.

CIRCUIT DESCRIPTION (cont.)

Analog Shutdown

This circuit is included to get a latched shutdown as close to the outputs as possible, from a time standpoint. With an internal 130mV threshold, this comparator has a common-mode range from ground to (V_{IN} – 3V). When not used, both inputs should be grounded. The time required for this circuit to latch is inversely proportional to the amount of overdrive but reaches a minimum of 180nsec. As with the flip-flop, an input off-time of at least 200nsec is required to reset the latch between pulses.

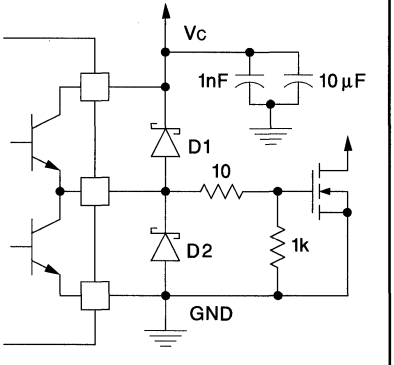
Supply Voltage

With an internal 5V regulator, this circuit is optimized for use with a 7 to 40V supply; however, with some slight response time degradation, it can also be driven from 5V. When V_{IN} is low, the entire circuit is disabled and no current is drawn from V_C. When combined with a UC1840 PWM, the Driver Bias switch can be used to supply V_{IN} to the UC1706. V_{IN} switching should be fast as if V_C is high, undefined operation of the outputs may occur with V_{IN} less than 5V.

Thermal Considerations

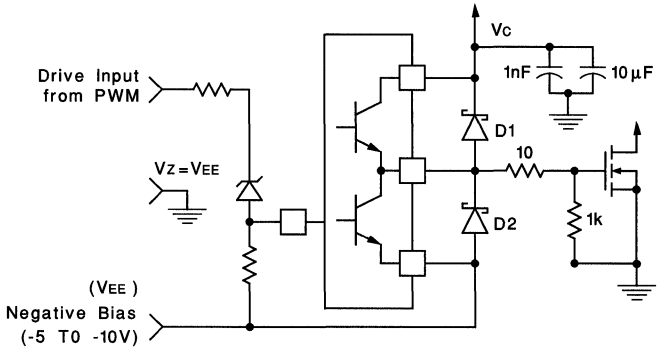
Should the chip temperature reach approximately 155°C, a parallel, non--inverting input is activated driving both outputs to the low state.

APPLICATIONS



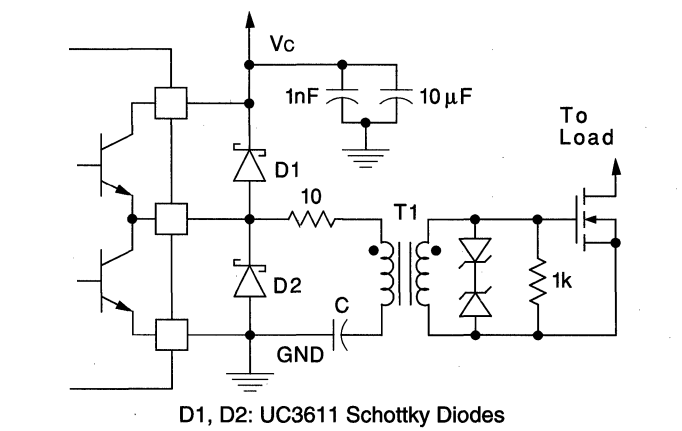
D1, D2; UC3611 Schottky Diodes

Power MOSFET Drive Circuit



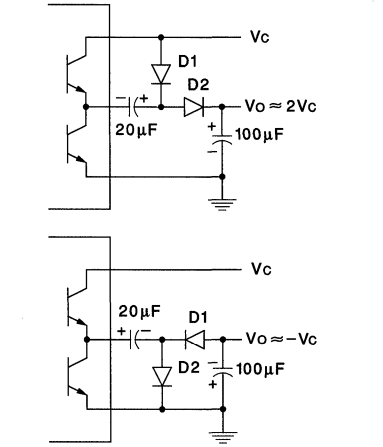
D1, D2; UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs



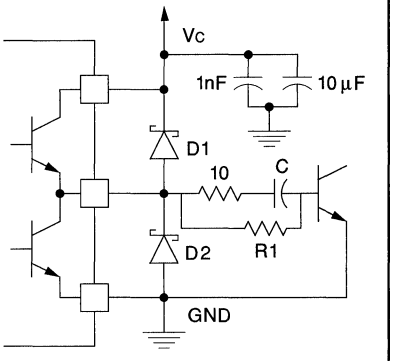
D1, D2: UC3611 Schottky Diodes

Transformer Coupled MOSFET Drive Circuit



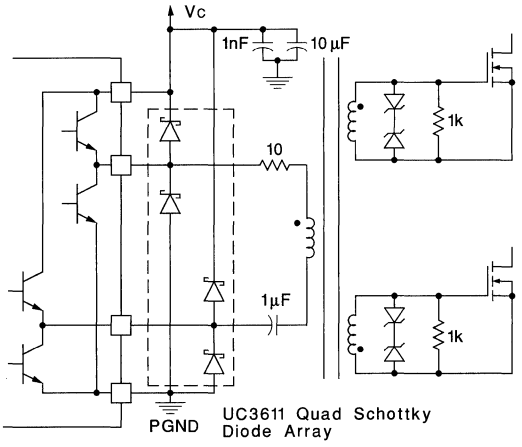
Charge Pump Circuits

APPLICATIONS (cont'd)



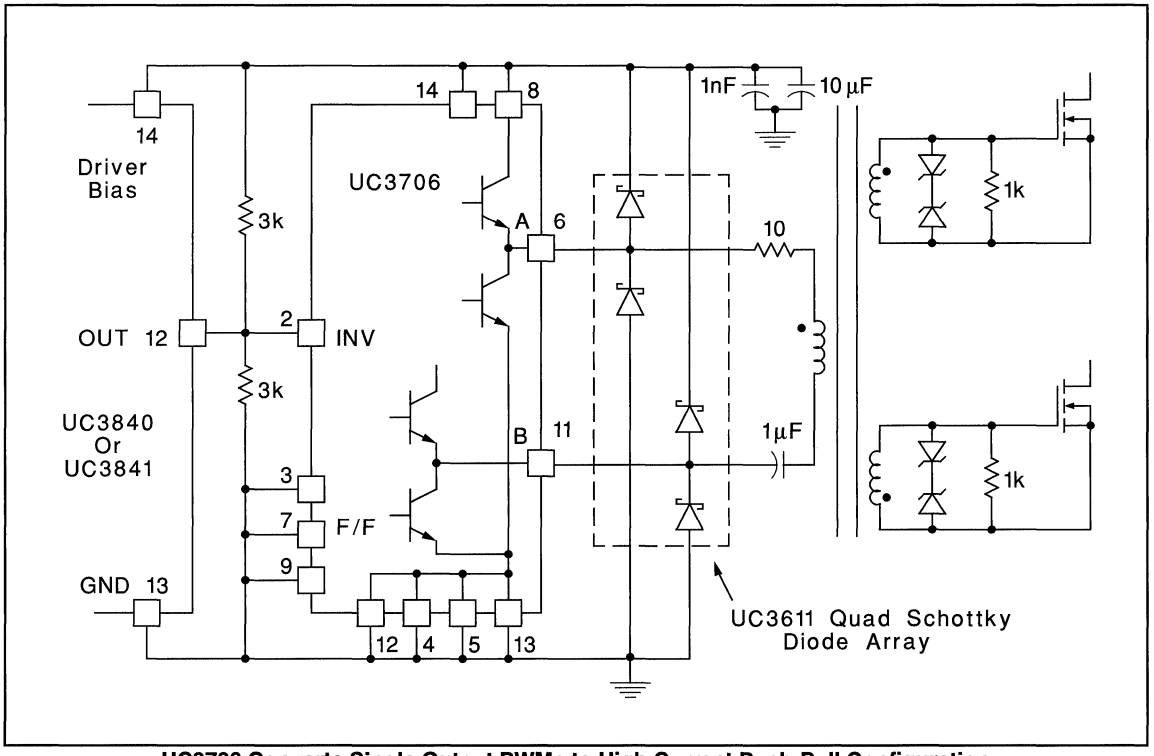
D1, D2: UC3611 Schottky Diodes

Power Bipolar Drive Circuit



D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



UC3706 Converts Single Output PWMs to High Current Push-Pull Configuration

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application INFO available

UC1707
UC2707
UC3707

Dual Channel Power Driver

FEATURES

- Two independent Drivers
- 1.5A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40ns Rise and Fall into 1000pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown with Optional Latch
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package
- 20-Pin PLCC and CLCC Package

DESCRIPTION

The UC1707 family of power drivers is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices contain two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both VIN and VC can independently range from 5V to 40V.

These devices are available in two-watt plastic "bat-wing" DIP for operation over a 0°C to 70°C temperature range and, with reduced power, in a hermetically sealed cerdip for –55°C to +125°C operation. Also available in surface mount DW, Q, L packages.

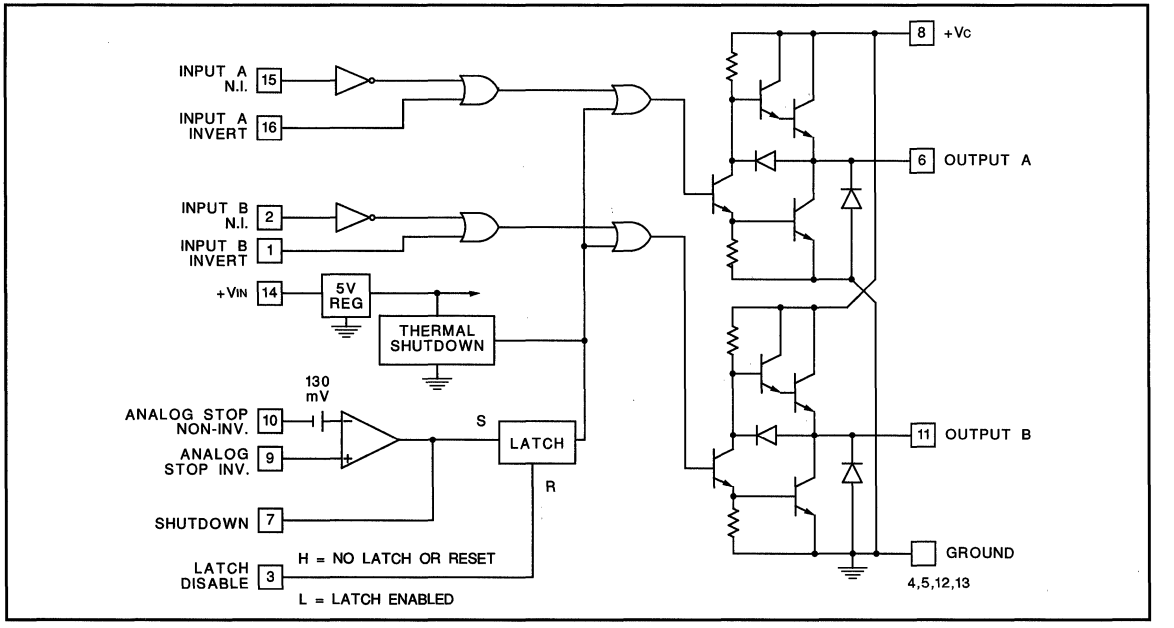
TRUTH TABLE (Each Channel)

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

OUT = $\overline{\text{INV}}$ and N.I.

$\overline{\text{OUT}}$ = INV or N.I.

BLOCK DIAGRAM



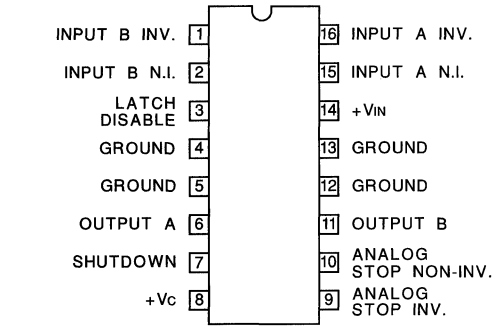
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, VIN, N/J-Pkg 40V
Collector Supply Voltage, VC, N/J-Pkg 40V
Output Current (Each Output, Source or Sink) Steady-State,
N/J-Pkg. . . . . ±500mA
Peak Transient
N-Pkg . . . . . ±1.5A
J-Pkg . . . . . ±1.0A
Capacitive Discharge Energy
N-Pkg 20mJ
J-Pkg. 15mJ
Digital Inputs (See Note), N/J-Pkg 5.5V
Analog Stop Inputs, N/J-Pkg . . . . . VIN
Power Dissipation at T_A = 25°C (See Note)
N-Pkg 2W
J-Pkg 1W
Power Dissipation at T (Leads/Case) = 25°C (See Note)
N-Pkg 5W
J-Pkg 2W
Operating Temperature Range. . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note: All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital Drive can exceed 5.5V if input current is limited to 10mA. Consult Packaging section of Databook for thermal limitations and considerations of package.

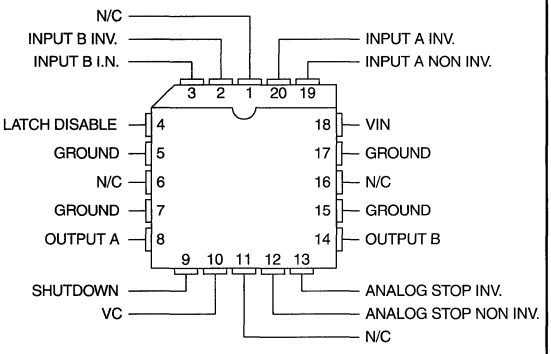
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package,



Note: All four ground pins must be connected to a common ground.

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



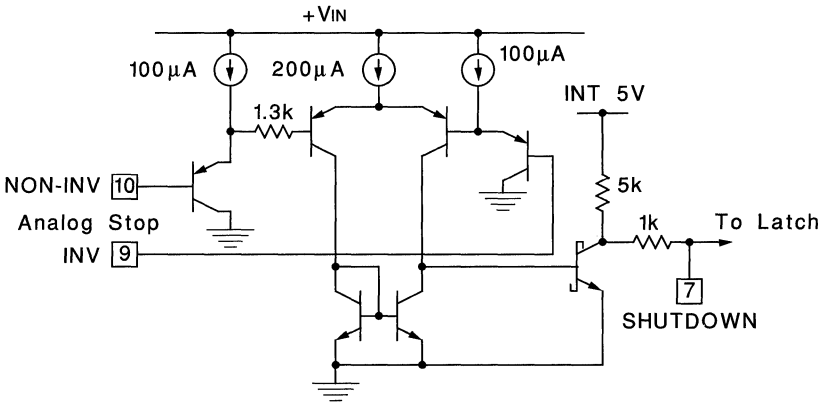
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1707, –25°C to +85°C for the UC2707 and 0°C to +70°C for the UC3707; V_{IN} = V_C = 20V. T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} = 40V		12	15	mA
V_C Supply Current	V_C = 40V, Outputs Low		5.2	7.5	mA
V_C Leakage Current	V_{IN} =0, VC =30V, No Load		.05	0.1	mA
Digital Input Low Level				0.8	V
Digital Input High Level		2.2			V
Input Current	V_I = 0		–0.06	–1.0	mA
Input Leakage	V_I = 5V		.05	0.1	mA
Output High Sat., V_C-V_O	I_O = –50mA			2.0	V
	I_O = –500mA			2.5	V
Output Low Sat., V_O	I_O = –50mA			0.4	V
	I_O = –500mA			2.5	V
Analog Threshold	V_{CM} = 0 to 15V	100	130	160	mV
Input Bias Current	V_{CM} = 0		–10	–20	µA
Thermal Shutdown			155		°C
Shutdown Threshold	Pin 7 Input	0.4	1.0	2.2	V
Latch Disable Threshold	Pin 3 Input	0.8	1.2	2.2	V

TYPICAL SWITCHING CHARACTERISTICS: V_{IN} = V_C = 20V, T_A = 25°C. Delays measured to 10% output change.

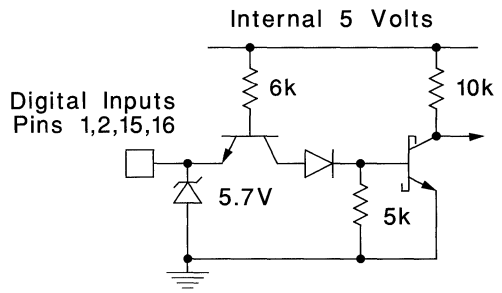
PARAMETERS	TEST CONDITIONS	OUTPUT CL =			UNITS
From Inv. Input to Output		open	1.0	2.2	nF
Rise Time Delay		40	50	60	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		30	40	50	ns
90% to 10% Fall		25	40	50	ns
From N.I. Input to Output					
Rise Time Delay		30	40	50	ns
10% to 90% Rise		25	40	50	ns
Fall Time Delay		45	55	65	ns
90% to 10% Fall		25	40	50	ns
V_C Cross-Conduction Current Spike Duration	Output Rise	25			ns
	Output Fall	0			ns
Analog Shutdown Delay	Stop non-Inv. = 0V	180			ns
	Stop Inv. = 0 to 0.5V	180			ns
Digital Shutdown Delay	2V Input on Pin 7	50			ns

SIMPLIFIED INTERNAL CIRCUITRY



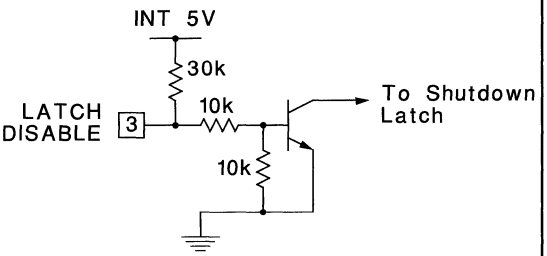
The input common-mode voltage range is from ground to (VIN-3V). When not used both inputs shoul1d be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

Figure 1. Typical digital input gate.



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

Figure 2. Typical digital input gate.



The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the VIN supply or by momentarily (>200ns) raising pin 3 high.

Figure 3. Latch disable.

SIMPLIFIED INTERNAL CIRCUITRY (cont.)

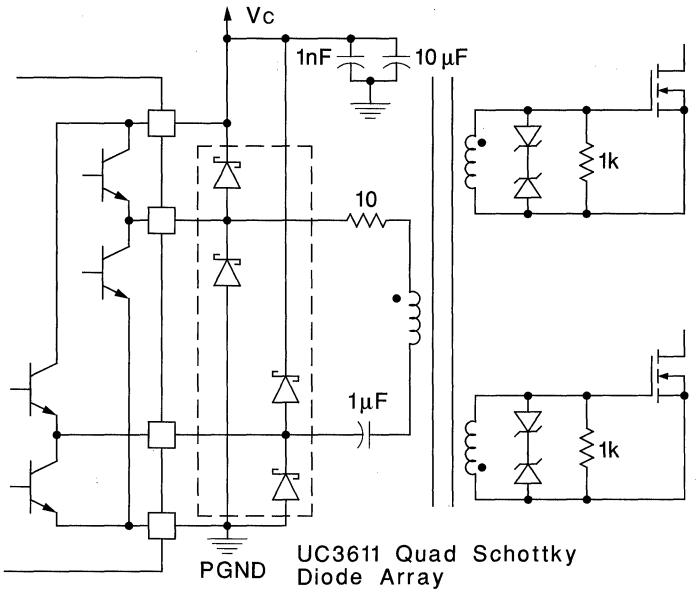
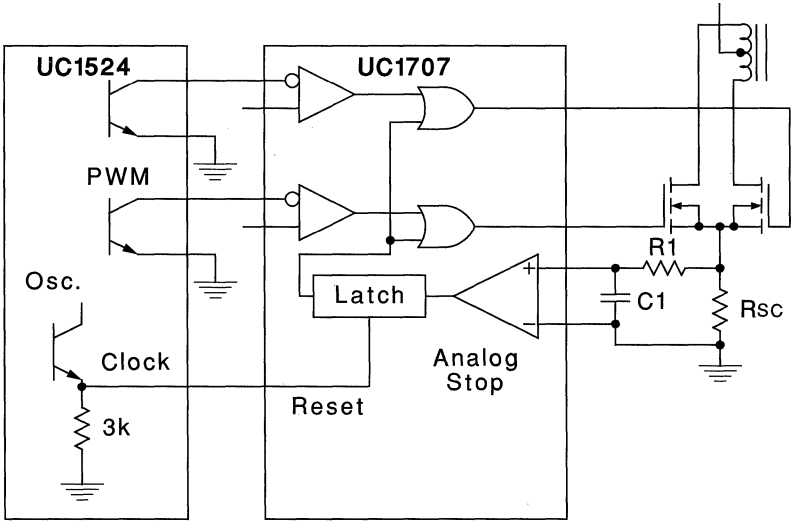


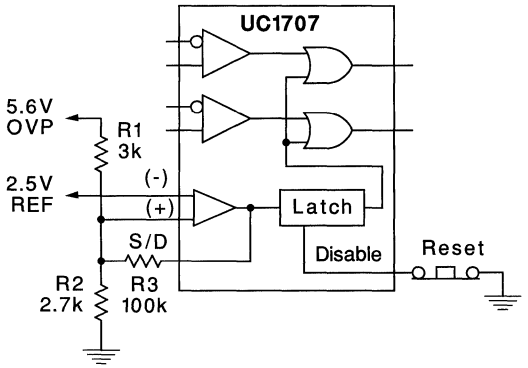
Figure 4. Transformer coupled push-pull MOSFET drive circuit.



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R1C1 is used to filter leading edge spikes.

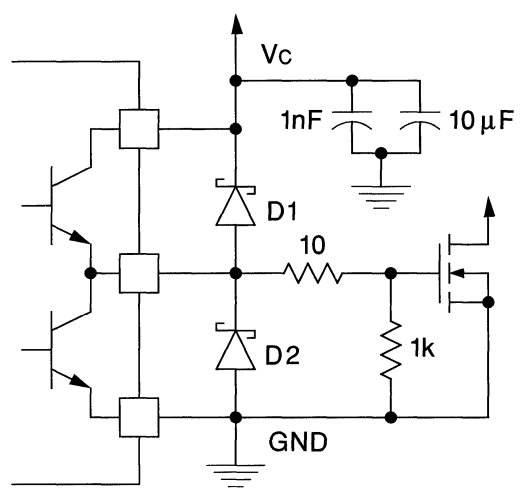
Figure 5. Current limiting.

APPLICATIONS



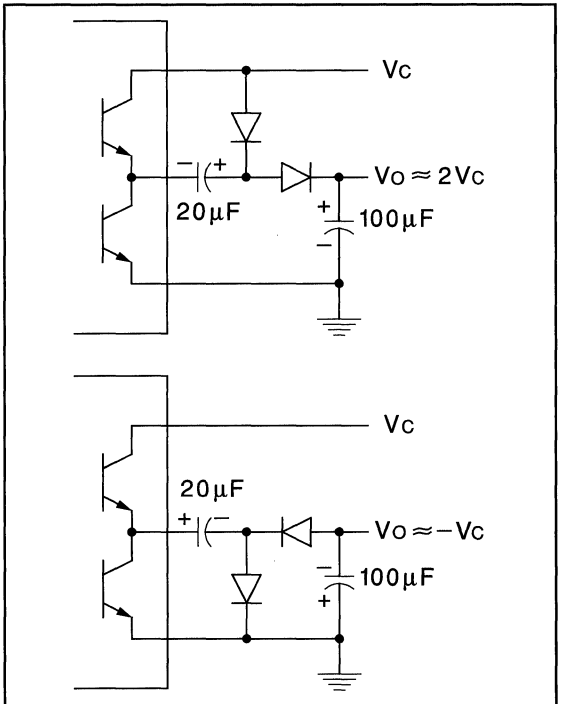
With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.

Figure 6. Over-voltage protection.



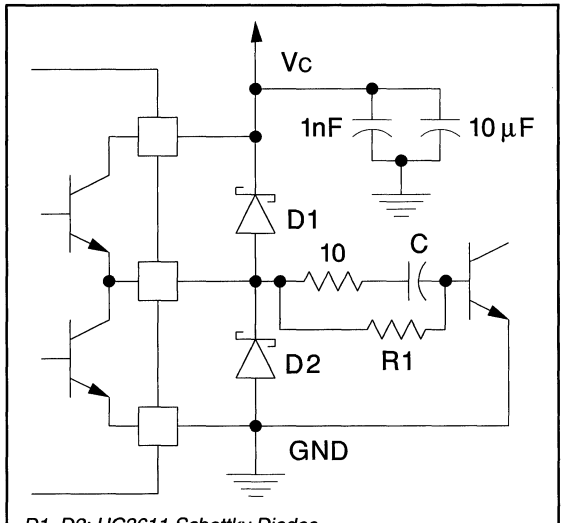
D1, D2: UC3611 Schottky Diodes

Figure 7. Power MOSFET drive circuit.



When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

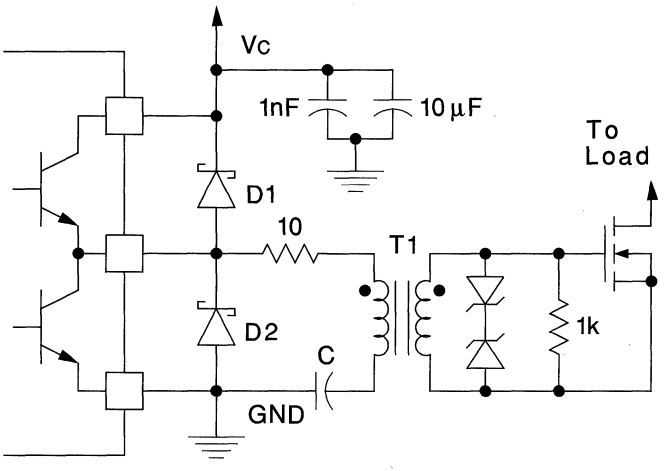
Figure 8. Charge pump circuits.



D1, D2: UC3611 Schottky Diodes

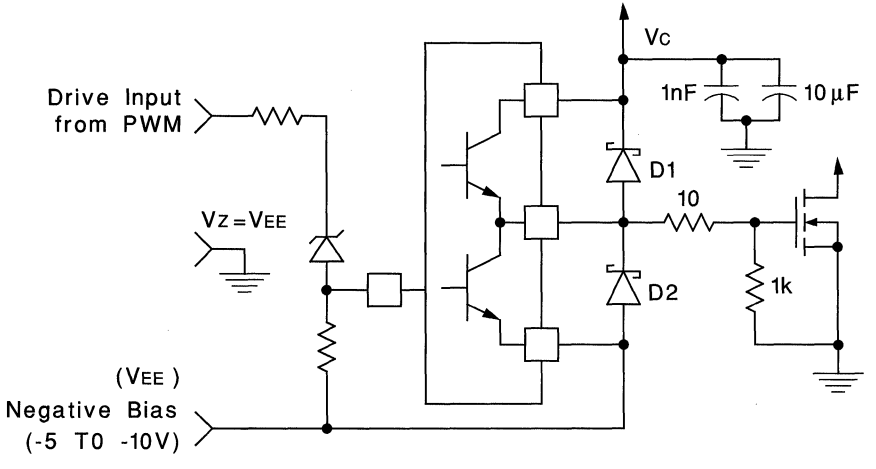
Figure 9. Power bipolar drive circuit.

TRANSFORMER COUPLING



D1, D2: UC3611 Schottky Diode

Figure 10. Transformer coupled MOSFET drive circuit.



D1, D2: UC3611 Schottky Diode

Figure 11. Power MOSFET drive circuit using negative bias voltage and level shifting to ground reference PWM.

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application INFO available

UC1708
UC2708
UC3708

Dual Non-Inverting Power Driver

FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25ns Rise and Fall Times
- 25ns Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

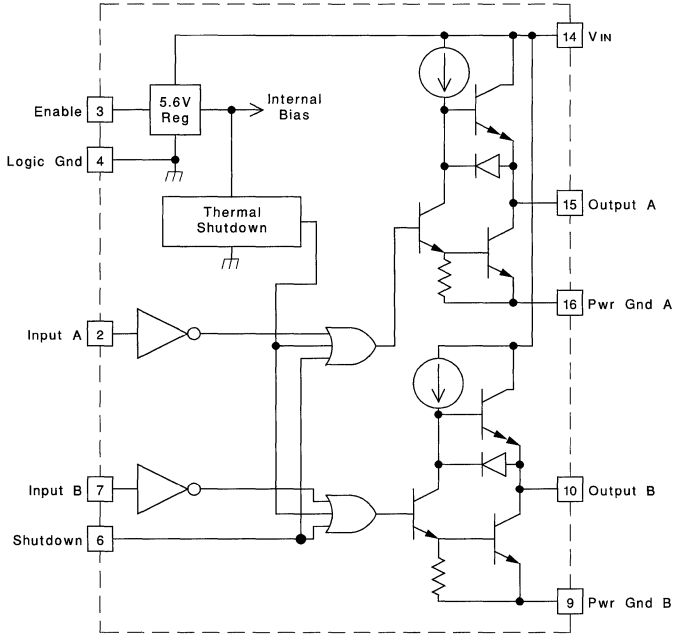
DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 to 35 volt supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as V_{IN}. Each output can source or sink up to 3A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

The UC3708 and UC2708 are available in plastic 8-pin MINIDIP and 16-pin "bat-wing" DIP packages for commercial operation over a 0°C to +70°C temperature range and industrial temperature range of -25°C to +85°C respectively. For operation over a -55°C to +125°C temperature range, the UC1708 is available in hermetically sealed 8-pin MINIDIP and 16 pin DIP packages. Surface mount devices are also available.

BLOCK DIAGRAM



Note: Shutdown feature available only in J, N, or D packages.

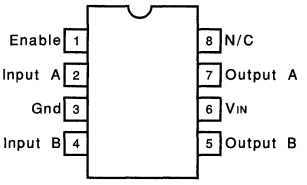
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V_{IN} 35V
Output Current (Each Output, Source or Sink)
  Steady-State 0.5A
  Peak Transient 3A
Ouput Voltage . . . . . -0.3 to (V_{IN} + 0.3)V
Enable and Shutdown Inputs . . . . . -0.3 to 6.2V
A and B Inputs . . . . . -0.3 to (V_{IN} + 0.3)V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . -65° to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

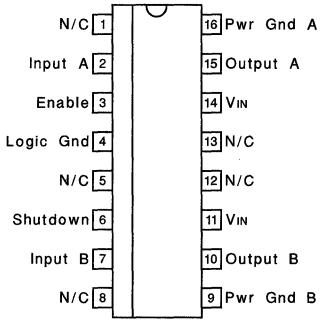
NOTE 1: All voltages are with respect to Logic Gnd pin. All currents are positive into, negative out of, device terminals.
NOTE 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

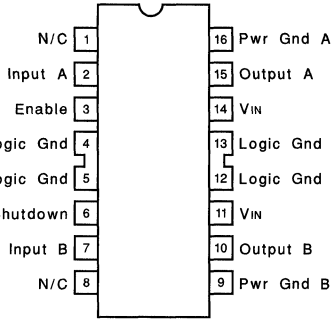
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE or NE Package



Note: In JE package Pin 4 is logic ground. Pins 5, 12, and 13 are N/C.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{IN}=10V to 35V, and these specifications apply for: –55°C<T_A<125°C for the UC1708, –25°C<T_A<+85°C for the UC2708, and 0°C<T_A<70°C for the UC3708. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	OutputsLow		18	26	mA
	Outputs High		14	18	mA
	Enable = 0V		1	4	mA
A, B and Shutdown Inputs Low Level				0.8	V
A, B and Shutdown Inputs High Level		2.0			V
A, B Input Current Low	$V_{A,B}$ = 0.4V	-1	-0.6		mA
A, B Input Current High	$V_{A,B}$ = 2.4V	-200		50	µA
A, B Input Leakage Current High	$V_{A,B}$ = 35.3V			200	µA
Shutdown Input Current Low	$V_{SHUTDOWN}$ = 0.4V		20	100	µA
Shutdown Input Current High	$V_{SHUTDOWN}$ = 2.4V		170	500	µA
	$V_{SHUTDOWN}$ = 6.2V		0.6	1.5	mA

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, V_{IN} = 10V to 35V, and these specifications apply for: $-55^{o}C<T_A<125^{o}C$ for the UC1708, $-25^{o}C<T_A<+85^{o}C$ for the UC2708, and $0^{o}C<T_A<70^{o}C$ for the UC3708. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Enable Input Current Low	V_{ENABLE} = 0V	-600	-460	200	µA
Enable Input Current High	V_{ENABLE} = 6.2V			200	µA
Enable Threshold Rising			2.8	3.6	V
Enable Threshold Falling		1.0	2.4	3.4	V
Output High Sat., V_{IN} - V_{OUT}	I_{OUT} = -50mA			2.0	V
	I_{OUT} = -500mA			2.5	V
Output Low Sat., V_{OUT}	I_{OUT} = 50mA			0.5	V
	I_{OUT} = 500mA			2.5	V
Thermal Shutdown			155		°C

SWITCHING CHARACTERISTICS (Figure 1) (V_{IN} = 20V, delays measured to 10% output change.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
From A,B Input to Output:					
Rise Time Delay (TPLH)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	40	ns
	CL = 2200pF		30	45	ns
10% to 90% Rise (TTLH)	CL = 0pF		55	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	40	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		35	50	ns
90% to 10% Fall (TTHL)	CL = 0pF		15	20	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		40	55	ns
From Shutdown Input to Output					
Rise Time Delay (TPLH)	CL = 0pF		25	75	ns
	CL = 1000pF (Note 3)		30	75	ns
	CL = 2200pF		35	75	ns
10% to 90% Rise (TTLH)	CL = 0pf		50	75	ns
	CL = 1000pF (Note 3)		25	50	ns
	CL = 2200pF		40	55	ns
Fall Time Delay (TPHL)	CL = 0pF		25	45	ns
	CL = 1000pF (Note 3)		30	50	ns
	CL = 2200pF		35	55	ns
90% to 10% Fall (TTHL)	CL = 0pF		25	20	ns
	CL = 1000pF (Note 3)		25	45	ns
	CL = 2200pF		40	55	ns
Total Supply Current	F = 200kHz, 50% duty cycle, both channels; CL = 0pF		23	25	mA
	F = 200kHz, 50% duty cycle, both channels; CL = 2200pF		38	45	mA

NOTE 3: These parameters, specified at 1000pF, although guaranteed over recommended operating conditions, are not tested in production.

Figure 1: AC Test Circuit and Switching Time Waveforms

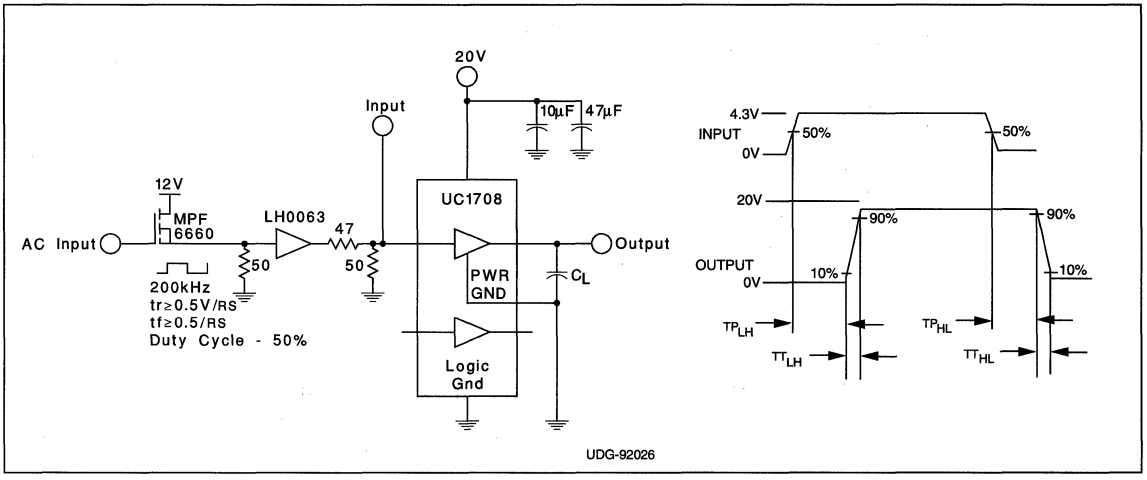
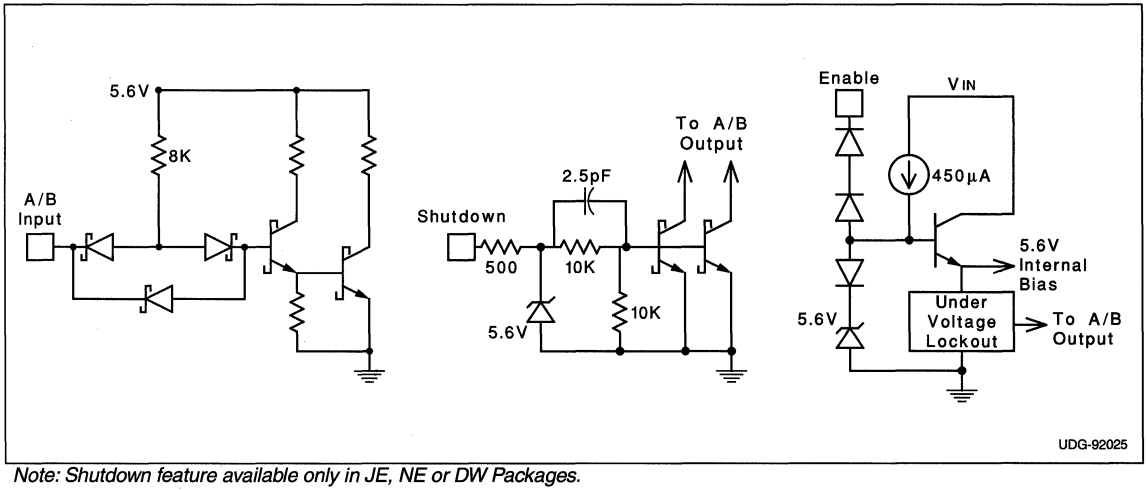


Figure 2: Equivalent Input Circuits



Note: Shutdown feature available only in JE, NE or DW Packages.

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application INFO available

UC1709
UC2709
UC3709

Dual High-Speed FET Driver

FEATURES

- 1.5 Amp Source/Sink Drive
- Pin Compatible with 0026 Products
- 40 ns Rise and Fall into 1000 pF
- Low Quiescent Current
- 5V to 40V Operation
- Thermal Protection

DESCRIPTION

The UC3709 family of power drivers is an effective low-cost solution to the problem of providing fast turn-on and off for the capacitive gates of power MOSFETs. Made with a high-speed Schottky process, these devices will provide up to 1.5 amps of either source or sink current from a totem-pole output stage configured for minimal cross-conduction current spike.

The UC3709 is pin compatible with the MMH0026 or DS0026, and while the delay times are longer, the supply current is much less than these older devices.

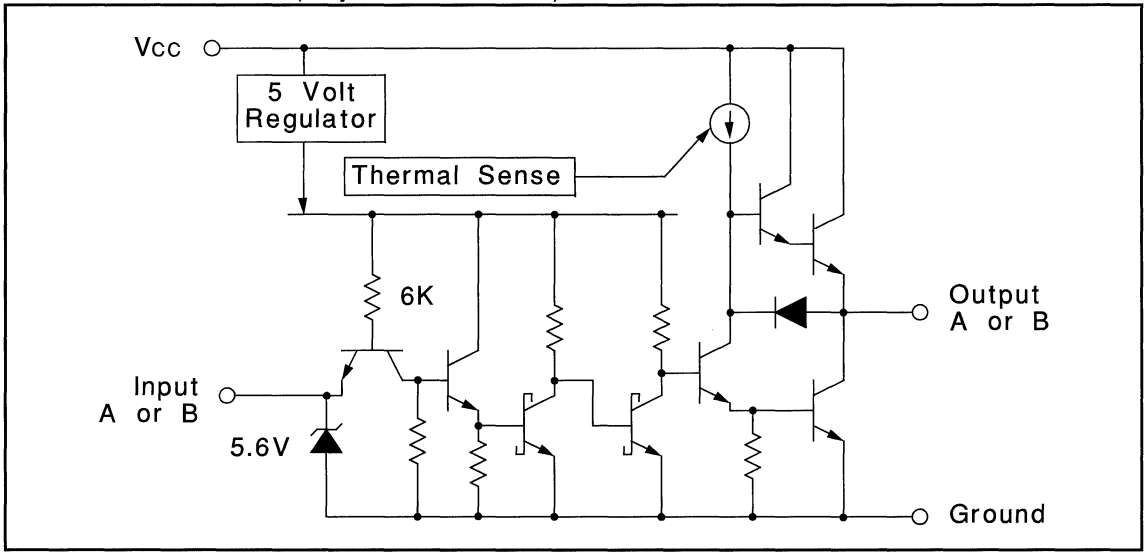
With inverting logic, these units feature complete TTL compatibility at the inputs with an output stage that can swing over 30V. This design also includes thermal shutdown protection.

ABSOLUTE MAXIMUM RATINGS

	N-Pkg	J-Pkg
Supply Voltage, V_{CC}	40V	40V
Output Current (Source or Sink)		
Steady-State	±500	±500 mA
Peak Transient	±1.5A	±1.0A
Capacitive Discharge Energy	20 µJ	15 µJ
Digital Inputs (See Note)	5.5V	5.5V
Power Dissipation at T_A = 25°C	1W	1W
Power Dissipation at T_C = 25°C	3W	2W
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C	300 °C

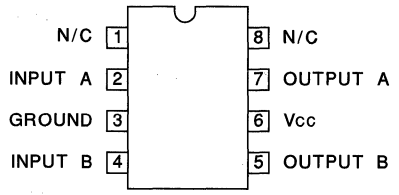
Note: All currents are positive into, negative out of the specified terminals. Digital drive can exceed 5.5V if input current is limited to 10mA. Consult Packaging section of Databook for thermal limitations and considerations of package.

SIMPLIFIED SCHEMATIC (Only One Driver Shown)

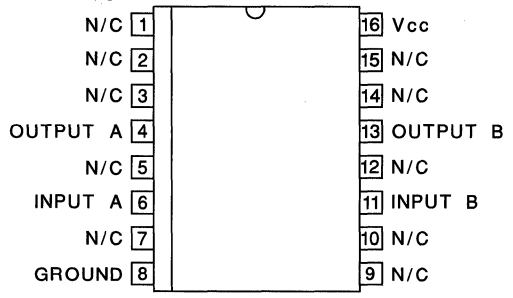


CONNECTION DIAGRAMS

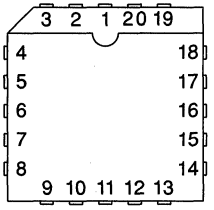
8 PIN DIL (TOP VIEW)
N or J Package



SOIC-16 (TOP VIEW)
DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
N/C	2
INPUT A	3
N/C	4
N/C	5
GROUND	6
N/C	7
N/C	8
INPUT B	9
N/C	10
N/C	11
OUTPUT B	12
N/C	13
N/C	14
N/C	15
Vcc	16
N/C	17
N/C	18
N/C	19
OUTPUT A	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1709, -40°C to +85°C for the UC2709, and 0°C to +70°C for the UC3709; V_{CC} = 20V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	Both Outputs High		10	12	mA
	Both Outputs Low		7	10	mA
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_I = 0		-0.6	-1.0	mA
Input Leakage	V_I = 5V		0.05	0.1	mA
Output High Sat., V_{CC}-V_O	I_O = -50mA		1.5	2.0	V
	I_O = -500mA		2.0	2.5	V
Output Low Sat., V_O	I_O = 50mA		0.1	0.4	V
	I_O = 500mA		2.0	2.5	V
Thermal Shutdown			155		°C

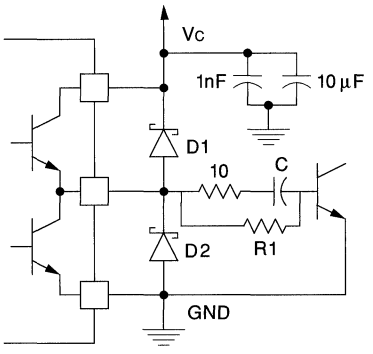
TYPICAL SWITCHING CHARACTERISTICS: V_{CC} = 20V, T_A = 25°C. Delays measured to 10% output change.

PARAMETERS	TEST CONDITIONS	OUTPUT C_L =		UNIT
		0 nF	2.2 nF	
Rise Time Delay		80	80	ns
10% to 90% Rise		20	40	ns
Fall Time Delay		60	80	ns
90% to 10% Fall		20	40	ns
V_{CC} Cross-Conduction Current Spike Duration	Output Rise	25		ns
	Output Fall	0		ns

Note: Refer to UC1705 specifications for further information

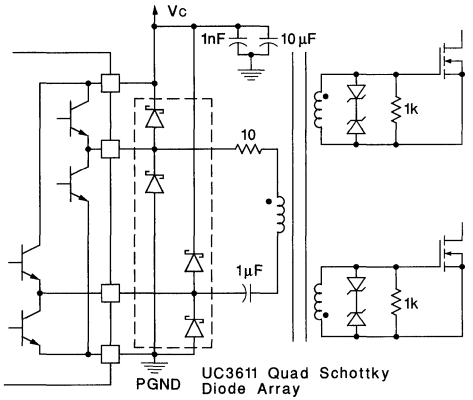
APPLICATIONS

Power Bipolar Drive Circuit



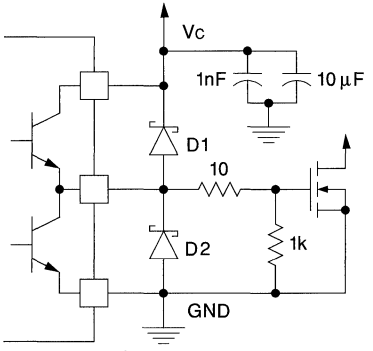
D1, D2: UC3611 Schottky Diodes

Transformer Coupled Push-Pull MOSFET Drive Circuit



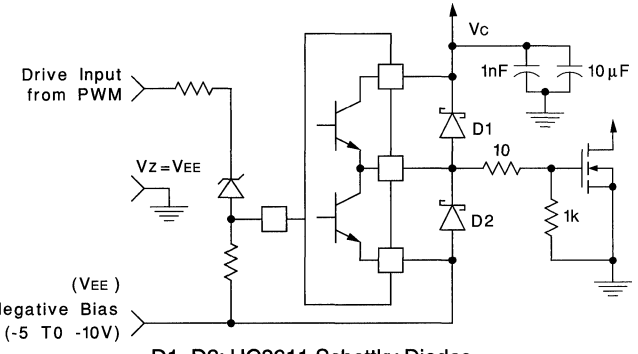
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit



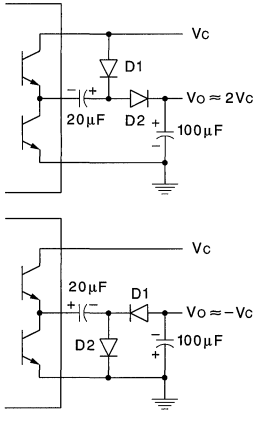
D1, D2: UC3611 Schottky Diodes

Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting To Ground Referenced PWMS

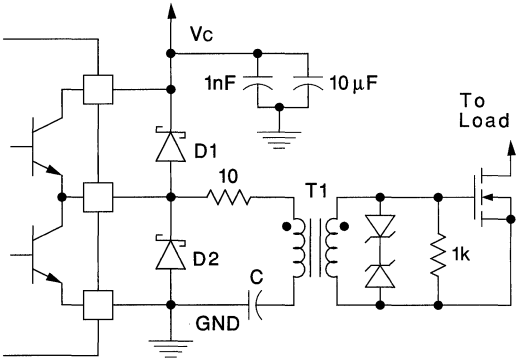


D1, D2: UC3611 Schottky Diodes

Charge Pump Circuits



Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

High Current FET Driver

FEATURES

- Totem Pole Output with 6A Source/Sink Drive
- 3ns Delay
- 20ns Rise and Fall Time into 2.2nF
- 8ns Rise and Fall Time into 30nF
- 4.7V to 18V Operation
- Inverting and Non-Inverting Outputs
- Under-Voltage Lockout with Hysteresis
- Thermal Shutdown Protection
- MINIDIP and Power Packages

DESCRIPTION

The UC1710 family of FET drivers is made with a high-speed Schottky process to interface between low-level control functions and very high-power switching devices-particularly power MOSFET's. These devices accept low-current digital inputs to activate a high-current, totem pole output which can source or sink a minimum of 6A.

Supply voltages for both V_{IN} and V_C can independently range from 4.7V to 18V. These devices also feature under-voltage lockout with hysteresis.

The UC1710 is packaged in an 8-pin hermetically sealed dual in-line package for –55°C to +125°C operation. The UC2710 and UC3710 are specified for a temperature range of –40°C to +85°C and 0°C to +70°C respectively and are available in either an 8-pin plastic dual in-line or a 5-pin, TO-220 package. Surface mount devices are also available.

TRUTH TABLE

INV	N.I.	Out
H	H	L
L	H	H
H	L	L
L	L	L

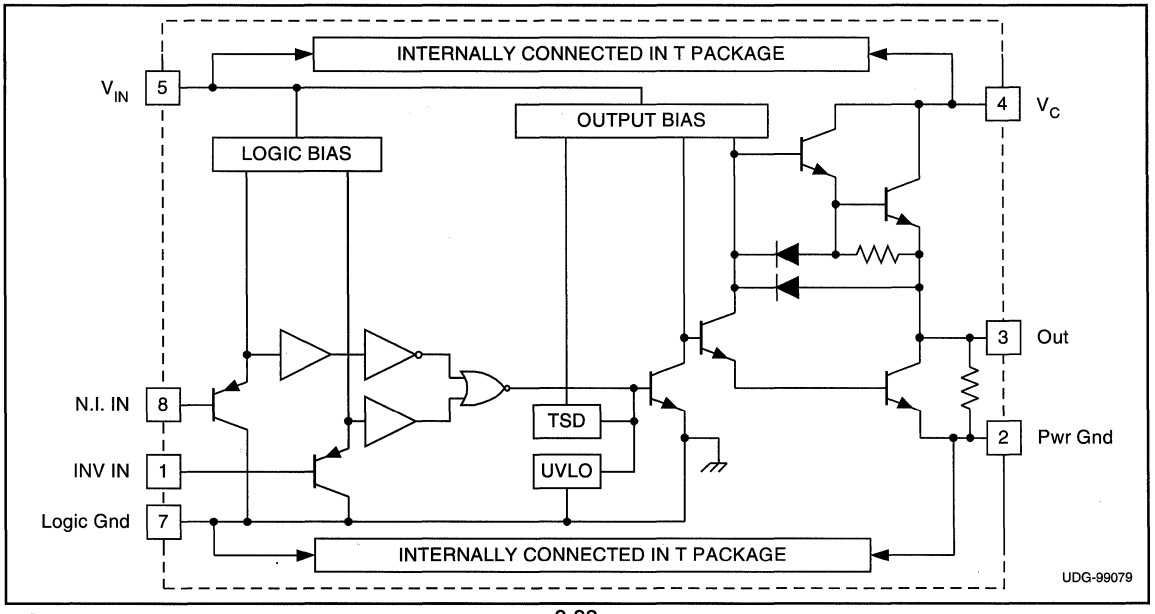
$\overline{OUT}$= $\overline{INV}$ and N.I.

$\overline{OUT}$= INV or $\overline{N.I.}$

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1710J	–55°C to +125°C	8 pin CDIP
UC2710DW	–40°C to +85°C	16 pin SOIC-wide
UC2710J		8 pin CDIP
UC2710N		8 pin PDIP
UC2710T		5 pin TO220
UC3710DW	0°C to +70°C	16 pin SOIC-wide
UC3710N		8 pin PDIP
UC3710T		5 pin TO220

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

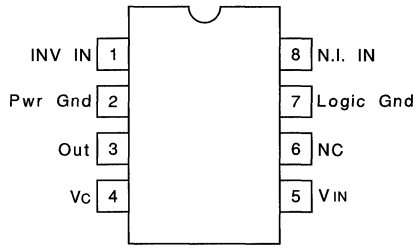
	N-Package	J-Package	T-Package
Supply Voltage, Vin	20V	20V	20V
Collector Supply Voltage, V_C	20V	20V	20V
Operating Voltage	18V	18V	18V
Output Current (Source or Sink)			
Steady-State	± 500mA	± 500mA	± 1A
Digital Inputs	–0.3V-V_{IN}	–0.3V – V_{IN}	–0.3V – V_{IN}
Power Dissipation at Ta=25°C	1W	1W	3W
Power Dissipation at T (Case) = 25°C	2W	2W	25W
Operating Junction Temperature	–55°C to +150°C	–55°C to +150°C	–55°C to +150°C
Storage Temperature	–65°C to +150°C	–65°C to +150°C	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

Note 1: All currents are positive into, negative out of the specified terminal.

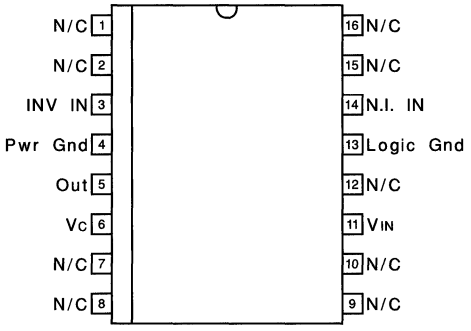
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

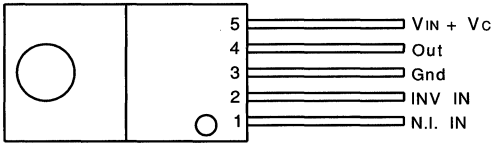
DIL-8 MINIDIP (Top View)
J or N Package



SOIC-16 (Top View)
DW Package



5-Pin TO-220 (Top View)



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $V_{IN} = V_C = 15V$, No load, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN} Supply Current	V_{IN} =18V, V_C =18V, Output Low		26	35	mA
	V_{IN} =18V, V_C =18V, Output High		21	30	mA
V_C Supply Current	V_{IN} =18V, V_C =18V, Output Low		1.5	5.0	mA
	V_{IN} =18V, V_C =18V,Output High		5.0	8	mA
UVLO Threshold	V_{IN} High to Low	3.8	4.1	4.4	V
	V_{IN} Low to High	4.1	4.4	4.8	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $V_{IN} = V_C = 15V$, No load, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold Hysteresis		0.1	0.3	0.5	V
Digital Input Low Level				0.8	V
Digital Input High Level		2.0			V
Digital Input Current	Digital Input = 0.0V	–70	–4.0		µA
Output High Sat., $V_C - V_O$	I_O= –100mA		1.35	2.2	V
	I_O= –6A		3.2	4.5	V
Output Low Sat., V_O	I_O= 100mA		0.25	0.6	V
	I_O= 6A		3.4	4.5	V
Thermal Shutdown			165		°C
From Inv., Input to Output (Note 3, 4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	40	ns
	CL = 30nF		85	150	ns
From N.I. Input to Output (Note 3,4):					
Rise Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	70	ns
10% to 90% Rise	CL = 0		20	40	ns
	CL = 2.2nF		25	40	ns
	CL = 30nF		85	150	ns
Fall Time Delay	CL = 0		35	70	ns
	CL = 2.2nF		35	70	ns
	CL = 30nF		35	80	ns
90% to 10% Fall	CL = 0		15	40	ns
	CL = 2.2nF		20	50	ns
	CL = 30nF		85	150	ns
Total Supply Current at 200kHz Input Switching Frequency	T_A = 25°C (Note 5) CL = 0		30	40	mA

Note: 3. Delay measured from 50% input change to 10% output change.

Note: 4. Those parameters with CL = 30nF are not tested in production.

Note: 5. Inv. Input pulsed at 50% duty cycle with N.I. Input = 3V. or N.I. Input pulsed at 50% duty cycle with Inv. Input = 0V.

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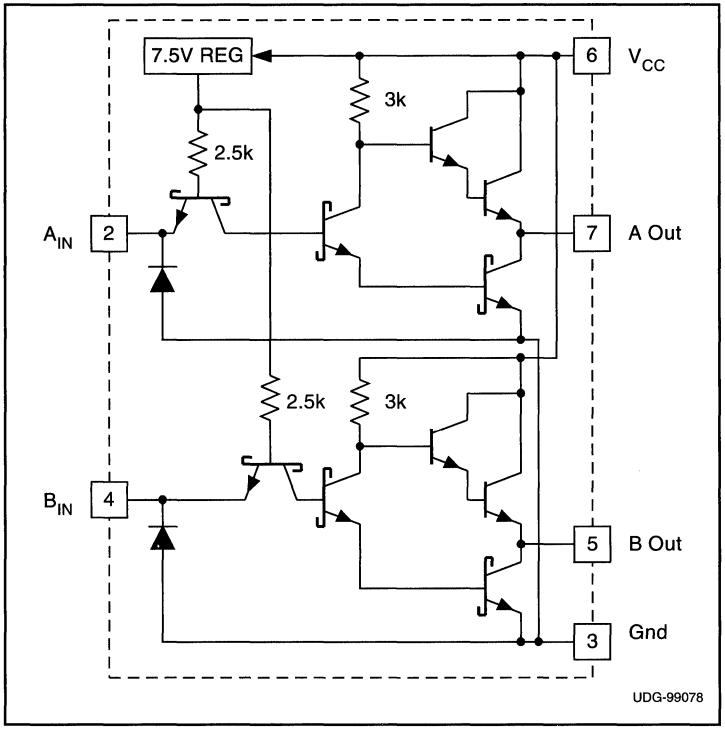
Dual Ultra High-Speed FET Driver

FEATURES

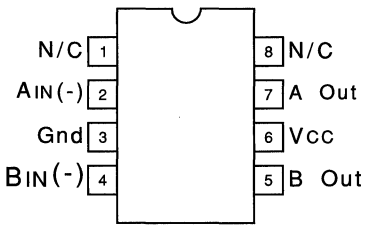
- 25ns Rise and Fall into 1000pF
- 15ns Propagation Delay
- 1.5A Source or Sink Output Drive
- Operation with 5V to 35V Supply
- High-Speed Schottky NPN Process
- 8-PIN MINIDIP Package

BLOCK DIAGRAM



CONNECTION DIAGRAM

DIL-8 (Top View)
J or N Package



DESCRIPTION

The UC1711 family of FET drivers are made with an all-NPN Schottky process in order to optimize switching speed, temperature stability, and radiation resistance. The cost for these benefits is a quiescent supply current which varies with both output state and supply voltage. For lower power requirements, refer to the the UC1709 family which is both pin compatible with, and functionally equivalent to the UC1711.

These devices implement inverting logic with TTL compatible inputs, and output stages which will either source, or sink in excess of 1.5A of load current with minimal cross-conduction charge. Due to their monolithic construction, the channels are well matched and can be paralleled for doubled output current capability.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{CC} 40V
Output Current (Source or Sink)
Steady State . . . . . ± 500mA
Peak Transient . . . . . ± 1.5A
Maximum Forced Voltage . . . . . -0.3V to 7V
Maximum Forced Current . . . . . ± 10mA
Power Dissipation 1W
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

Note 1: *Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals. All reliability information for this device has been gathered at an ambient air temperature of 125°C, and a supply voltage of 25V.*

Note 2: *Consult Unitrode databook for information regarding thermal specifications and limitations of packages.*

ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1711J	–55°C to +125°C	Ceramic DIP
UC3711J	0°C to +70°C	Ceramic DIP
UC3711N	0°C to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V. T_A =T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
Supply Current (Note 3)	Both inputs = 0V; V_{CC} = 15V		11	15	mA
	Both inputs = 5V; $V_{CC=15V}$		20	27	mA
	Both inputs = 0V; $V_{CC=35V}$		15	20	mA
	Both inputs = 5V; $V_{CC=35V}$		41	56	mA
Logic Inputs					
Logic 0 Input Voltage				0.8	V
Logic 1 Input Voltage		2.2			V
Input Current	V_{IN} = 0V	-5.0	-2.7		mA
	V_{IN} = 5V		0.5	2.0	mA
Output Stages					
Output High Level	I_{SOURCE} = 20mA, below V_{CC}		1.5	2.0	V
	I_{SOURCE} = 200mA, below V_{CC}		2.0	3.0	V
Output Low Level	I_{SINK} = 20mA		.25	0.4	V
	I_{SINK} = 200mA		0.4	1.0	V
Switching Characteristics (Note 4)					
Rise Time Delay, TPLH	C_{LOAD} = 0		10	40	ns
	C_{LOAD} = 1000pF, (Note 5)		15	50	ns
	C_{LOAD}= 2200pF		20	55	ns
Fall Time Delay, TPHL	C_{LOAD} = 0		3	20	ns
	C_{LOAD} = 1000pf, (Note 5)		5	20	ns
	C_{LOAD} = 2200pF		5	20	ns
Rise Time, TLH	C_{LOAD} = 0, (Note 5)		12	25	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD} = 2200pF		40	55	ns
Fall Time, THL	C_{LOAD} = 0, (Note 5)		7	15	ns
	C_{LOAD} = 1000pF, (Note 5)		25	40	ns
	C_{LOAD}= 2200pF		40	55	ns
Total Supply Current	Freq = 200kHz, 50% Duty-cycle Both Channels Switching				
	C_{LOAD} = 0		17	23	mA
	C_{LOAD} = 2200pF		29	35	mA

Note 3: *Supply currents at other input supply votages can be calculated by extrapolating the 15V and 35V supply currents. The impedance of the chip at the V_{CC} pin is linear for supply voltages from 8V to 35V, the approximate value of this impedance is 4.3k for both inputs low, 0.94k for both inputs high, and 1.54k for one input high and one low.*

Note 4: *Switching test conditions are, V_{CC} = 15V, Input voltage waveform levels are 0V and 5V, with transition times of <3ns. The timing terms are defined as : TPHL Propagation delay 50% V_{IN} to 90% V_{OUT}; TPLH Propogation delay 50% V_{IN} to 10% V_{OUT}; THL 90% V_{OUT} to 10% V_{OUT}; TLH 10% V_{OUT} to 90% V_{OUT}.*

Note 5: *This specification not tested in production.Unless otherwise stated specifications hold for T_A = 0 to 70°C for the UC3711, and T_A = -55 to 125°C for the UC1711, V_{CC} = 15V. T_A = T_J.*

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UNITRODE

application INFO available

UC1714/5
UC2714/5
UC3714/5

Complementary Switch FET Drivers

FEATURES

- Single Input (PWM and TTL Compatible)
- High Current Power FET Driver, 1.0A Source/2A Sink
- Auxiliary Output FET Driver, 0.5A Source/1A Sink
- Time Delays Between Power and Auxiliary Outputs Independently Programmable from 50ns to 500ns
- Time Delay or True Zero-Voltage Operation Independently Configurable for Each Output
- Switching Frequency to 1MHz
- Typical 50ns Propagation Delays
- ENBL Pin Activates 220µA Sleep Mode
- Power Output is Active Low in Sleep Mode
- Synchronous Rectifier Driver

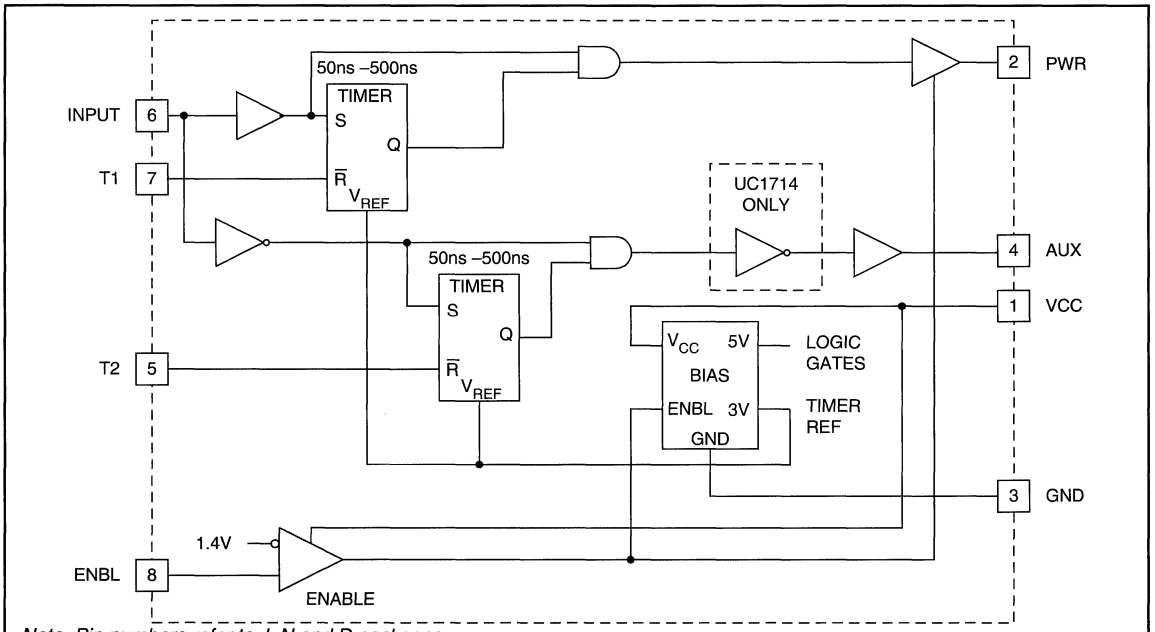
DESCRIPTION

These two families of high speed drivers are designed to provide drive waveforms for complementary switches. Complementary switch configurations are commonly used in synchronous rectification circuits and active clamp/reset circuits, which can provide zero voltage switching. In order to facilitate the soft switching transitions, independently programmable delays between the two output waveforms are provided on these drivers. The delay pins also have true zero voltage sensing capability which allows immediate activation of the corresponding switch when zero voltage is applied. These devices require a PWM-type input to operate and can be interfaced with commonly available PWM controllers.

In the UC1714 series, the AUX output is inverted to allow driving a p-channel MOSFET. In the UC1715 series, the two outputs are configured in a true complementary fashion.

6

BLOCK DIAGRAM



Note: Pin numbers refer to J, N and D packages.

UDG-99028

ABSOLUTE MAXIMUM RATINGS

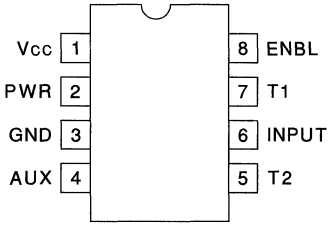
Supply Voltage V_{CC} 20V
Power Driver IOH
  continuous . . . . . –200mA
  peak . . . . . –1A
Power Driver IOL
  continuous 400mA
  peak 2A
Auxiliary Driver IOH
  continuous . . . . . –100mA
  peak . . . . . –500mA
Auxiliary Driver IOL
  continuous 200mA
  peak 1A

Input Voltage Range (INPUT, ENBL) . . . . . –0.3V to 20V
Storage Temperature Range . . . . . –65°C to 150°C
Operating Junction Temperature (Note 1) . . . . . 150°C
Lead Temperature (Soldering 10 seconds) . . . . . 300°C

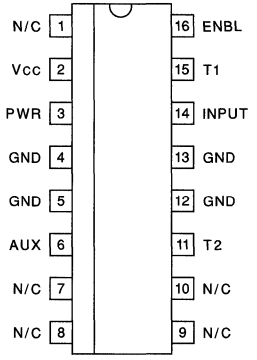
Note 1: *Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.*
Note 2: *Consult Packaging Section of databook for thermal limitations and specifications of packages.*

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
J or N, D Packages



SOIC-16 (Top View)
DP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_T1 = 100kΩ from T1 to GND, R_T2 = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
V_{CC}		7		20	V
I_{CC}, nominal	ENBL = 2.0V		18	24	mA
I_{CC}, sleep mode	ENBL = 0.8V		200	300	µA
Power Driver (PWR)					
Pre Turn-on PWR Output, Low	V_{CC} = 0V, I_{OUT} = 10mA, ENBL ® 0.8V		0.3	1.6	V
PWR Output Low, Sat. (V_{PWR})	INPUT = 0.8V, I_{OUT} = 40mA		0.3	0.8	V
	INPUT = 0.8V, I_{OUT} = 400mA		2.1	2.8	V
PWR Output High, Sat. (V_{CC} - V_{PWR})	INPUT = 2.0V, I_{OUT} = –20mA		2.1	3	V
	INPUT = 2.0V, I_{OUT} = –200mA		2.3	3	V
Rise Time	C_L = 2200pF		30	60	ns
Fall Time	C_L = 2200pF		25	60	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_T1 = 10kΩ (Note 4)	20	35	80	ns
T1 Delay, AUX to PWR	INPUT rising edge, R_T1 = 100kΩ (Note 4)	350	500	700	ns
PWR Prop Delay	INPUT falling edge, 50% (Note 3)		35	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 15V, ENBL ≥ 2V, R_T1 = 100kΩ from T1 to GND, R_T2 = 100kΩ from T2 to GND, and –55°C < T_A < 125°C for the UC1714/5, –40°C < T_A < 85°C for the UC2714/5, and 0°C < T_A < 70°C for the UC3714/5, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Driver (AUX)					
AUX Output Low, Sat (V_{AUX})	V_{IN} = 2.0V, I_{OUT} = 20mA		0.3	0.8	V
	V_{IN} = 2.0V, I_{OUT} = 200mA		1.8	2.6	V
AUX Output High, Sat ($V_{CC} - V_{AUX}$)	V_{IN} = 0.8V, I_{OUT} = -10mA		2.1	3.0	V
	V_{IN} = 0.8V, I_{OUT} = -100mA		2.3	3.0	V
Rise Time	C_L = 1000pF		45	60	ns
Fall Time	C_L = 1000pF		30	60	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_T2 = 10kΩ (Note 4)	20	50	80	ns
T2 Delay, PWR to AUX	INPUT falling edge, R_T2 = 100kΩ (Note 4)	250	350	550	ns
AUX Prop Delay	INPUT rising edge, 50% (Note 3)		35	80	ns
Enable (ENBL)					
Input Threshold		0.8	1.2	2.0	V
Input Current, I_{IH}	ENBL = 15V		1	10	µA
Input Current, I_{IL}	ENBL = 0V		–1	–10	µA
T1					
Current Limit	T1 = 0V		–1.6	–2	mA
Nominal Voltage at T1		2.7	3	3.3	V
Minimum T1 Delay	T1 = 2.5V, (Note 4)		40	70	ns
T2					
Current Limit	T2 = 0V		–1.2	–2	mA
Nominal Voltage at T2		2.7	3	3.3	V
Minumum T2 Delay	T2 = 2.5V, (Note 4)		50	100	ns
Input (INPUT)					
Input Threshold		0.8	1.4	2.0	V
Input Current, I_{IH}	INPUT = 15V		1	10	µA
Input Current, I_{IL}	INPUT = 0V		–5	–20	µA

Note 3: *Propagation delay times are measured from the 50% point of the input signal to the 10% point of the output signal's transition with no load on outputs.*

Note 4: *T1 delay is defined from the 50% point of the transition edge of AUX to the 10% of the rising edge of PWR. T2 delay is defined from the 90% of the falling edge of PWR to the 50% point of the transition edge of AUX.*

PIN DESCRIPTIONS

AUX: The AUX switches immediately at INPUT's rising edge but waits through the T2 delay after INPUT's falling edge before switching. AUX is capable of sourcing 0.5A and sinking 1.0A of drive current. See the Time Relationships diagram below for the difference between the UC1714 and UC1715 for INPUT, MAIN, and AUX. During sleep mode, AUX is inactive with a high impedance.

ENBL: The ENBL input switches at TTL logic levels (approximately 1.2V), and its input range is from 0V to 20V. The ENBL input will place the device into sleep mode when it is a logical low. The current into Vcc during the sleep mode is typically 220µA.

GND: This is the reference pin for all input voltages and the return point for all device currents. It carries the full peak sinking current from the outputs. Any tendency for the outputs to ring below GND voltage must be damped or clamped such that GND remains the most negative potential.

PIN DESCRIPTIONS (cont.)

INPUT: The input switches at TTL logic levels (approximately 1.4V) but the allowable range is from 0V to 20V, allowing direct connection to most common IC PWM controller outputs. The rising edge immediately switches the AUX output, and initiates a timing delay, T1, before switching on the PWR output. Similarly, the INPUT falling edge immediately turns off the PWR output and initiates a timing delay, T2, before switching the AUX output.

It should be noted that if the input signal comes from a controller with FET drive capability, this signal provides another option. INPUT and PWR provide a delay only at the leading edge while INPUT and AUX provide the delay at the trailing edge.

PWR: The PWR output waits for the T1 delay after the INPUT's rising edge before switching on, but switches off immediately at INPUT's falling edge (neglecting propagation delays). This output is capable of sourcing 1A and sinking 2A of peak gate drive current. PWR output includes a passive, self-biased circuit which holds this pin active low, when ENBL ≥ 0.8V regardless of VCC's voltage.

T1: A resistor to ground programs the time delay between AUX switch turn-off and PWR turn-on.

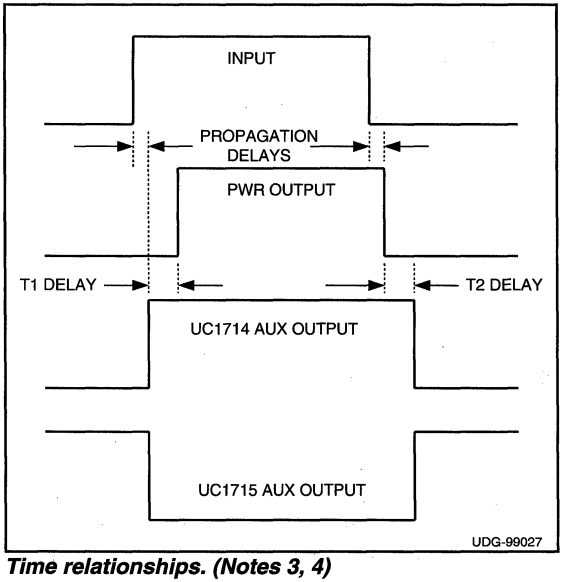
T2: This pin functions in the same way as T1 but controls the time delay between PWR turn-off and activation of the AUX switch.

T1, T2: The resistor on each of these pins sets the charging current on internal timing capacitors to provide independent time control. The nominal voltage level at each pin is 3V and the current is internally limited to 1mA. The total delay from INPUT to each output includes a propagation delay in addition to the programmable timer but since the propagation delays are approximately equal, the relative time delay between the two outputs can be assumed to be solely a function of the programmed delays. The relationship of the time delay vs. RT is shown in the Typical Characteristics curves.

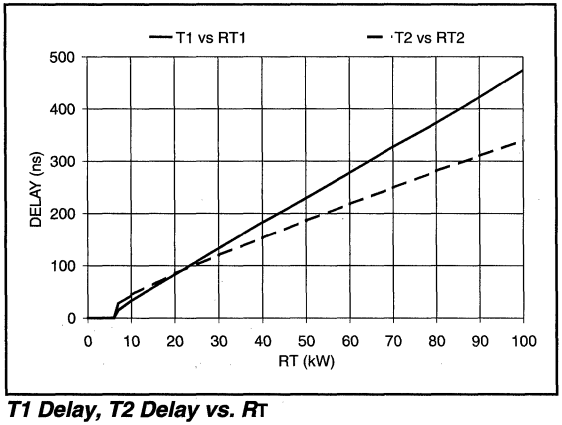
Either or both pins can alternatively be used for voltage sensing in lieu of delay programming. This is done by pulling the timer pins below their nominal voltage level which immediately activates the timer output.

VCC: The V_{CC} input range is from 7V to 20V. This pin should be bypassed with a capacitor to GND consistent with peak load current demands.

TYPICAL CHARACTERISTICS

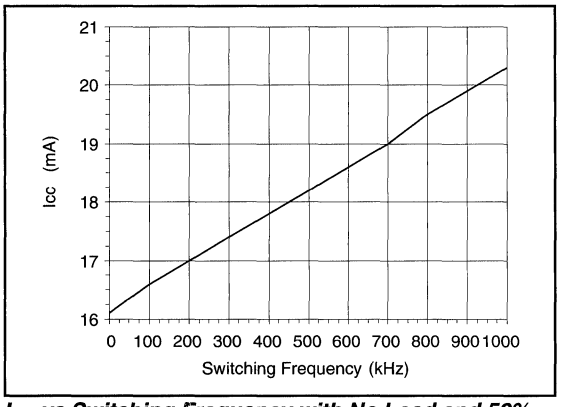


Time relationships. (Notes 3, 4)

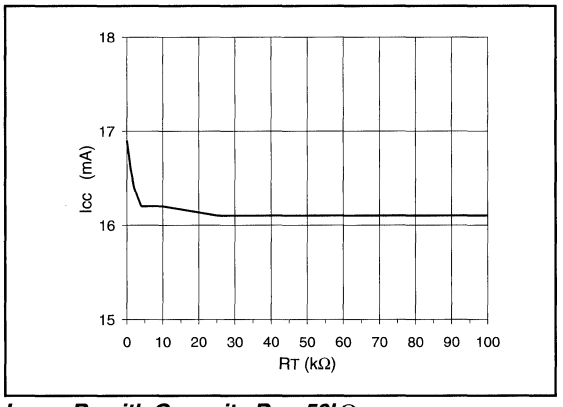


T1 Delay, T2 Delay vs. RT

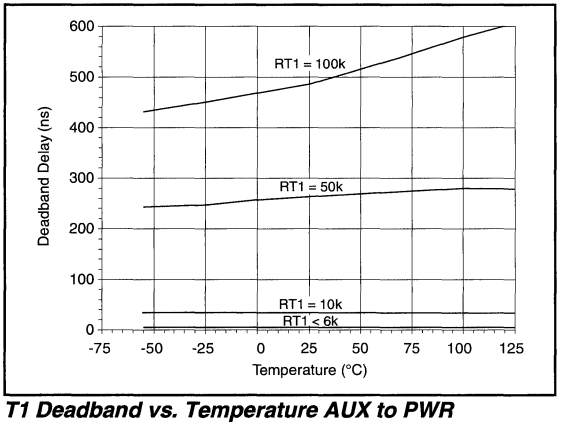
TYPICAL CHARACTERISTICS (cont.)



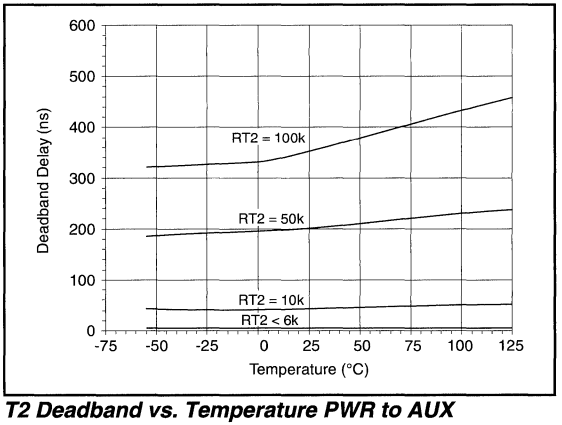
I_{CC} vs Switching Frequency with No Load and 50% Duty Cycle $R_T1 = R_T2 = 50k\Omega$



I_{CC} vs R_T with Opposite $R_T = 50k\Omega$



T1 Deadband vs. Temperature AUX to PWR



T2 Deadband vs. Temperature PWR to AUX

TYPICAL APPLICATIONS

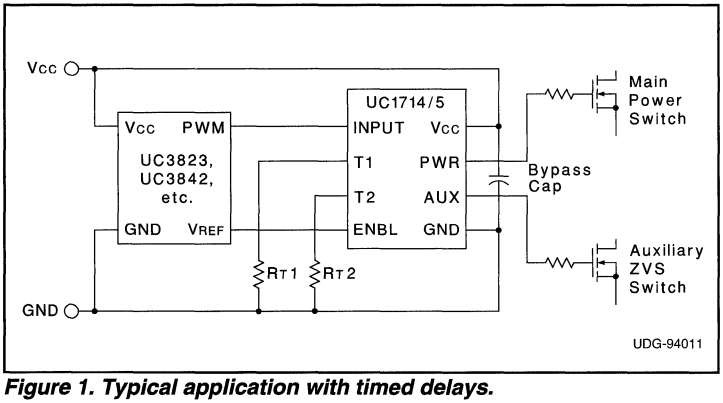


Figure 1. Typical application with timed delays.

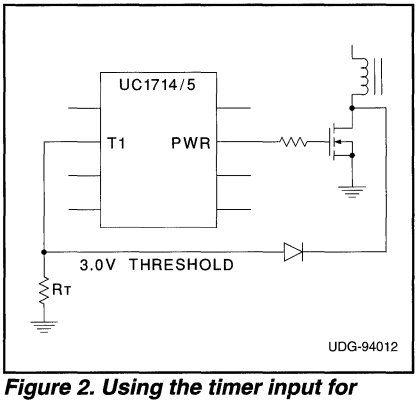


Figure 2. Using the timer input for zero-voltage sensing.

TYPICAL APPLICATIONS (cont.)

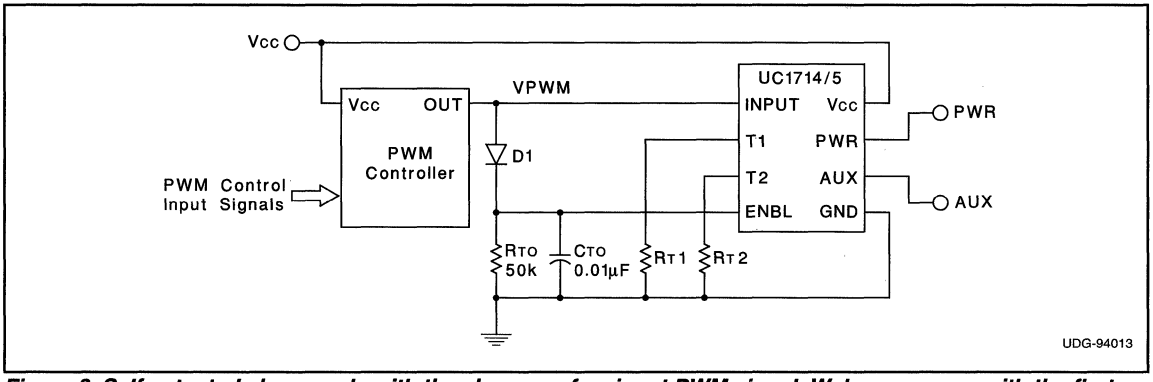


Figure 3. Self-actuated sleep mode with the absence of an input PWM signal. Wake up occurs with the first pulse while turn-off is determined by the (RTO • CTO) time constant.

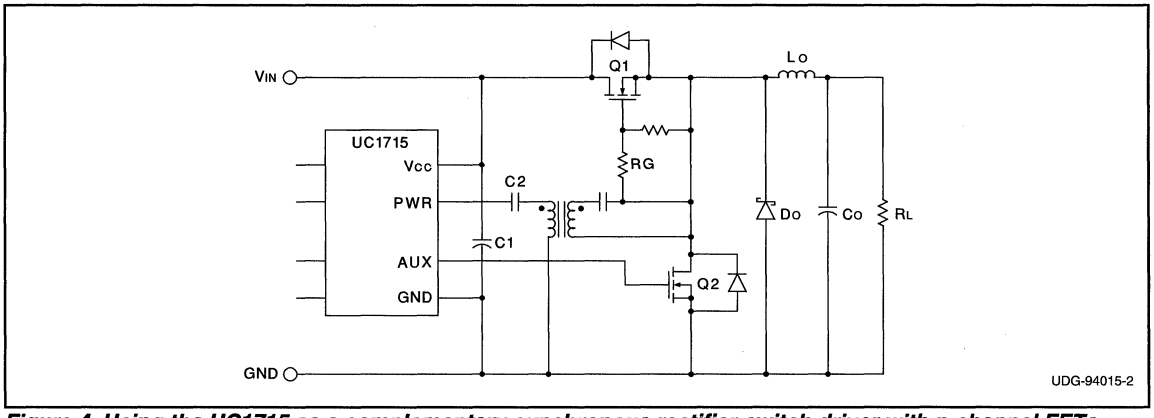


Figure 4. Using the UC1715 as a complementary synchronous rectifier switch driver with n-channel FETs

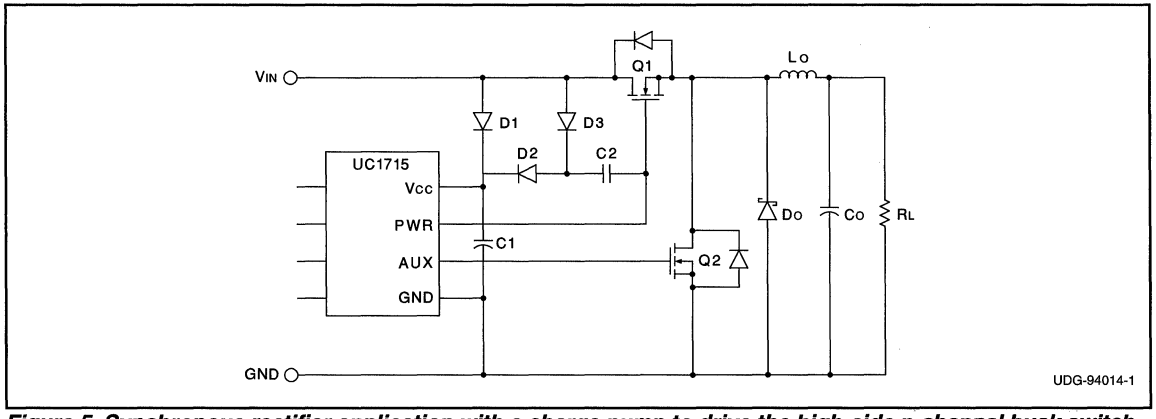


Figure 5. Synchronous rectifier application with a charge pump to drive the high-side n-channel buck switch. V_{IN} is limited to 10V as V_{CC} will rise to approximately $2V_{IN}$.

TYPICAL APPLICATIONS (cont.)

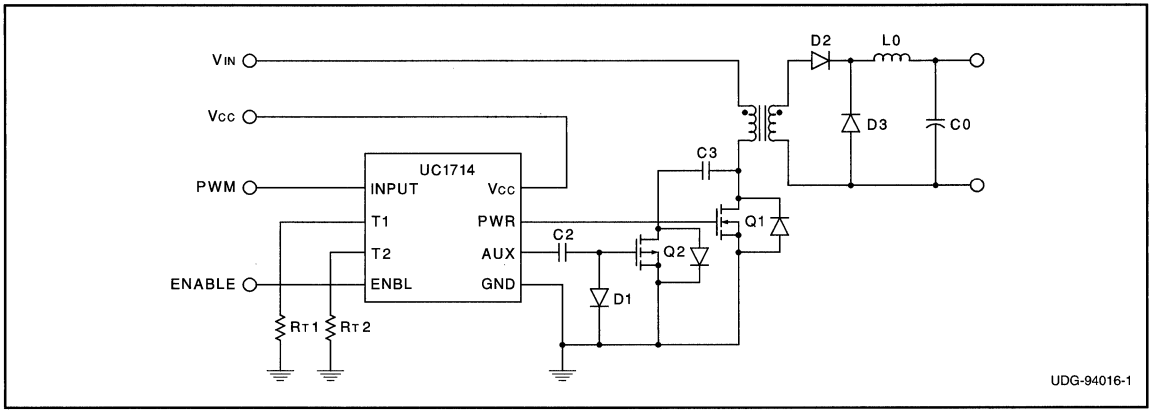


Figure 6. Typical forward converter topology with active reset provided by the UC1714 driving an N-channel switch (Q1) and a P-channel auxilliary switch (Q2).

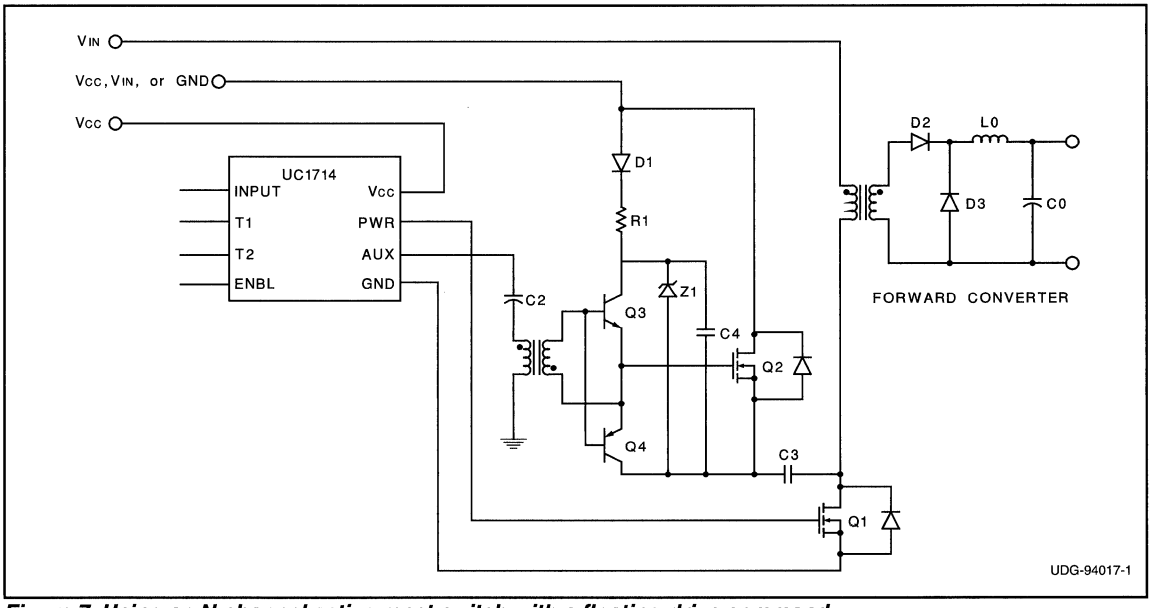


Figure 7. Using an N-channel active reset switch with a floating drive command.

Vicor Corporation has claimed that the use of active reset in a forward converter topology is covered under its U.S. Patent 4,441,146. Unitrode is not suggesting or encouraging persons to infringe or use Vicor's patented technology absent a license from Vicor.

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UNITRODE

application INFO available

UC1724
UC2724
UC3724

Isolated Drive Transmitter

FEATURES

- 500mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Logic Signal Instantly
- Programmable Operating Frequency
- Under-Voltage Lockout
- Able To Pass DC Information Across Transformer
- Up To 600kHz Operation

DESCRIPTION

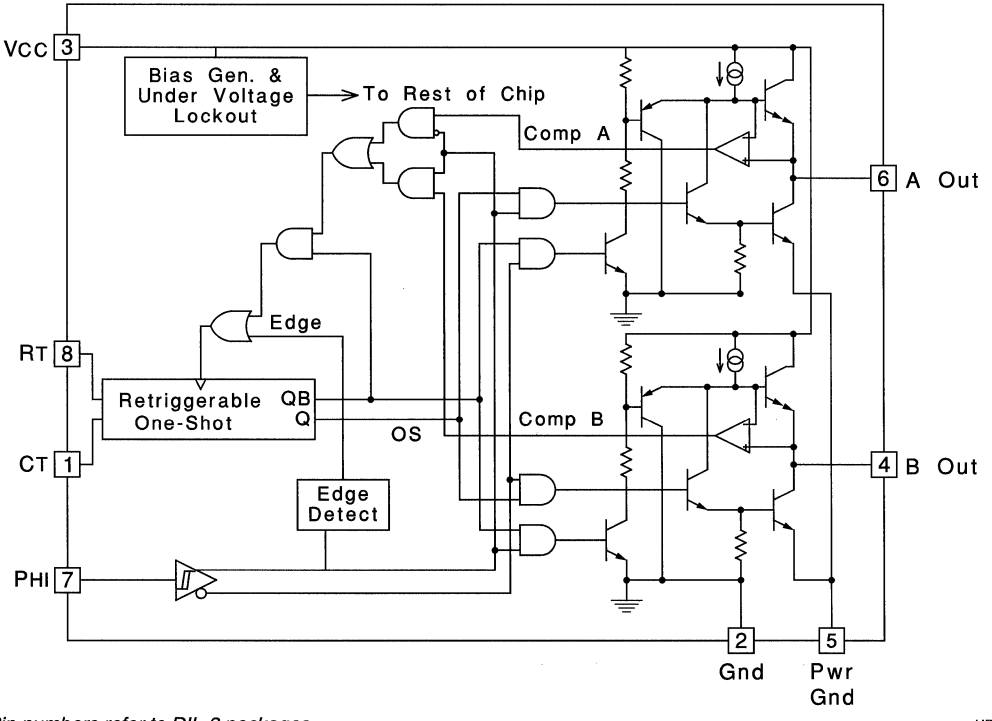
The UC1724 family of Isolated Drive Transmitters, along with the UC1725 Isolated Drivers, provide a unique solution to driving isolated power MOSFET gates. They are particularly suited to drive the high-side devices on a high-voltage H-bridge. The UC1724 devices transmit drive logic, and drive power, to the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty-cycle modulation technique that gives instantaneous response to the drive control transistions, and reliably passes steady-state, or DC, conditions. High frequency operation, up to 600kHz, allows the cost and size of the coupling transformer to be minimized.

These devices will operate over an 8 to 35 Volt supply range. The dual high current totem pole outputs are disabled by an uder-voltage lockout circuit to prevent spurious responses during startup or low voltage conditions.

These devices are available in 8 pin plastic or ceramic dual-inline packages, as well as 16 pin SOIC package.

BLOCK DIAGRAM



Note: Pin numbers refer to DIL-8 packages.

UDG-92037

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{IN} 40V
Source/Sink Current (Pulsed) 1A
Source/Sink Current (Continuous) 0.5A
Ouput Voltage (Pins 4, 6). . . . . –0.3 to (V_{IN} +0.3)V
PHI, RT, and CT inputs (Pins 1, 7, and 8) . . . . . –0.3 to 6V
Operating Junction Temperature (Note 2) . . . . . 150°C
Storage Temperature Range . . . . . –65°C to 150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

Note 1: *All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.*

Note 2: *Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.*

Note 3: *Pin numbers refer to DIL-8 packages.*

RECOMMENDED OPERATION CONDITIONS

Input Voltage . . . . . +9V to +35V
Sink/Source Load Current (each output) . . . . . 0 to 500mA
Timing Resistor. . . . . 2kW to 10kW
Timing Capacitor . . . . . 300pF to 3nF
Operating Temperature Range (UC1724) . . . –55°C<T_A<125°C
Operating Temperature Range (UC3724) . . . . . 0°C<T_A<70°C

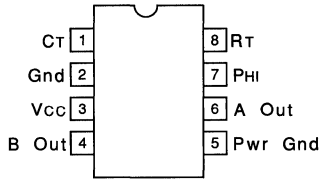
Note 4: *Range over which the device is functional and parameter limits are guaranteed.*

ORDERING INFORMATION

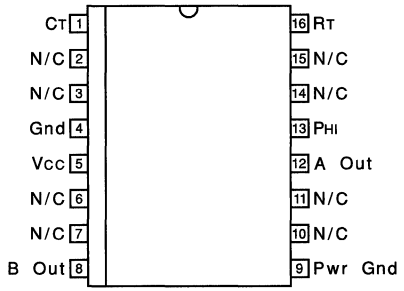
	TEMPERATURE RANGE	PACKAGE
UC1724J	–55°C to +125°C	CDIP
UC2724DW	–25°C to +85°C	SOIC-Wide
UC2724N		PDIP
UC3724DW	0°C to +70°C	SOIC-Wide
UC3724N		PDIP

CONNECTION DIAGRAMS

DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



6

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C < T_A < 125°C for the UC1724, –25°C < T_A < 85°C for the UC2724, and 0°C < T_A < 70°C for the UC3724. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Under-Voltage Lockout					
Start-Up Threshold	V_{IN} Rising		7.75	9.5	V
Threshold Hysteresis		0.4	1.0	1.5	V
Retriggerable One-Shot					
Initial Accuracy	T_J = 25°C	1.54	1.9	2.25	µs
Temperature Stability	Over Operating T_J	1.0		2.9	µs
Voltage Stability	V_{IN} = 10 to 35V		0.2	0.5	%/V
Operating Frequency	L_{LOAD} = 1.4mH	100	150	200	kHz
Minimum Pulse Width	RT = 2k CT = 300pF	100	500	1200	ns
Operating Frequency	RT = 2k CT = 300pF L_{LOAD} = 1.4mH	500	750	1100	kHz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 20V, R_T = 4.3kΩ, C_T = 1000pF, no load on any output and these specifications apply for: –55°C < T_A < 125°C for the UC1724, –25°C < T_A < 85°C for the UC2724, and 0°C < T_A < 70°C for the UC3724. T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Phi Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current	V_{IH} = +2.4V	–220	–130		µA
LOW Input Current	V_{IL} = +0.4V	–600	–300		µA
Delay to One-Shot				350	ns
Delay to Output				250	ns
Output Drivers					
Output Low Level	I_{SINK} = 50mA		0.3	0.4	V
	I_{SINK} = 250mA		0.5	2.1	V
Output High Level (Volts Below V_{CC})	I_{SOURCE} = 50 mA		1.5	2.1	V
	I_{SOURCE} = 250 mA		1.7	2.5	V
Rise/Fall Time	No load		30	90	ns
Total Supply Current					
Supply Current	C_T = 1.4V		15	30	mA

Additional Information

Please refer to the following Unitrode application topics.

[1] Application Note U-127, *Unique Chip Pair Simplified Isolated High-Side Switch Drive* by John A. O'Connor.

[2] Design Note DN-35, *IGBT Drive Using MOSFET Gate Drivers* by John A. O'Conner.

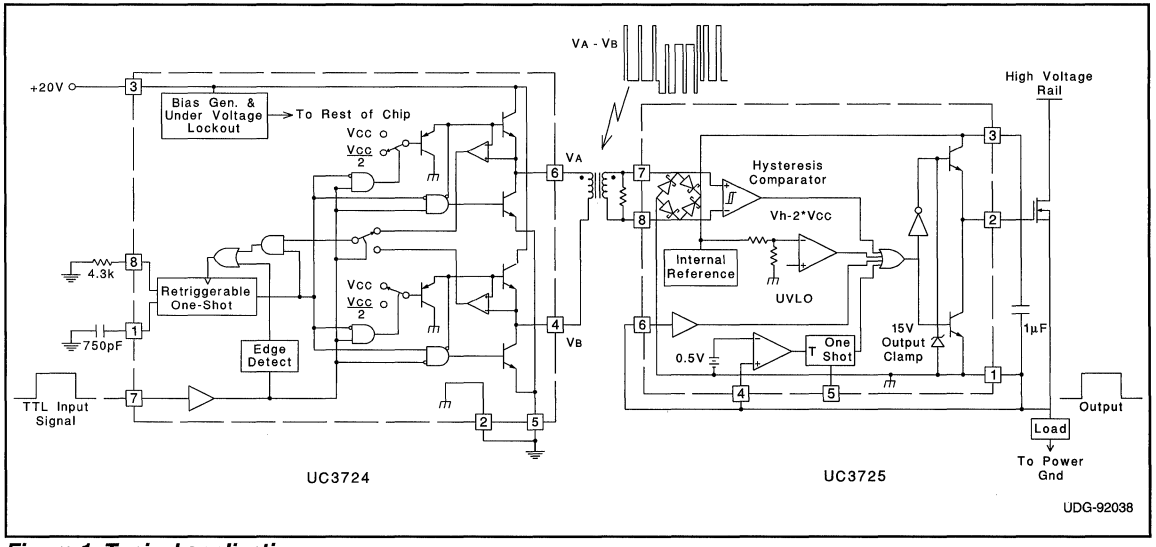


Figure 1. Typical application

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UNITRODE

application INFO available

UC1725
UC2725
UC3725

Isolated High Side FET Driver

FEATURES

- Receives Both Power and Signal Across the Isolation Boundary
- 9 to 15 Volt High Level Gate Drive
- Under-voltage Lockout
- Programmable Over-current Shutdown and Restart
- Output Enable Function

DESCRIPTION

The UC1725 and its companion chip, the UC1724, provide all the necessary features to drive an isolated MOSFET transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signals across an isolation boundary with a minimum of external components.

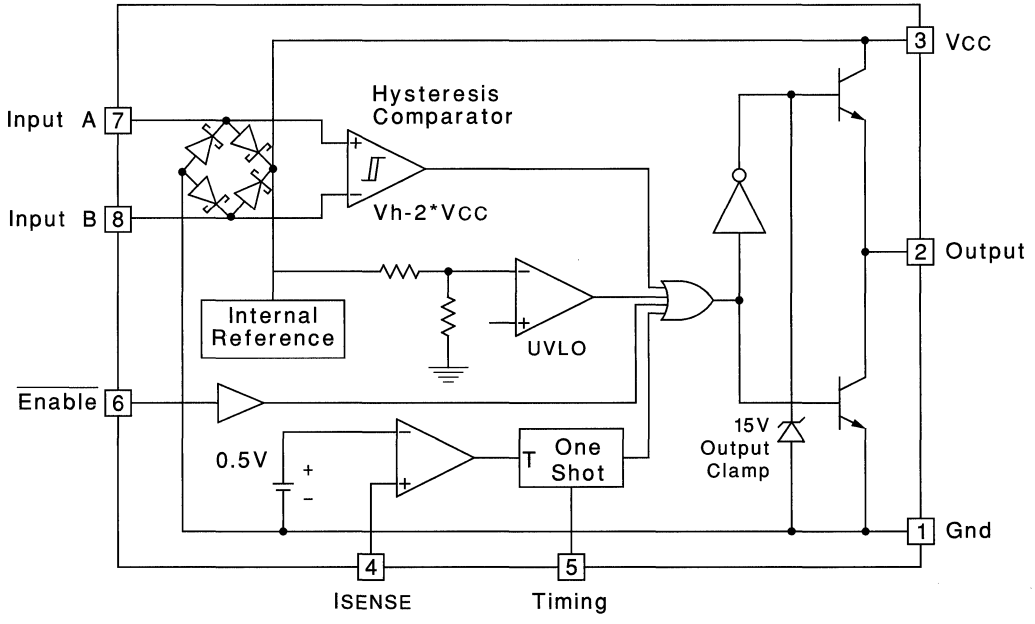
Protection circuitry, including under-voltage lockout, over-current shutdown, and gate voltage clamping provide fault protection for the MOSFET. High level gate drive is guaranteed to be greater than 9 volts and less than 15 volts under all conditions.

Uses include isolated off-line full bridge and half bridge drives for driving motors, switches, and any other load requiring full electrical isolation.

The UC1725 is characterized for operation over the full military temperature range of -55°C to +125°C while the UC2725 and UC3725 are characterized for -25°C to +85°C and 0°C to +70°C respectively.

6

BLOCK DIAGRAM



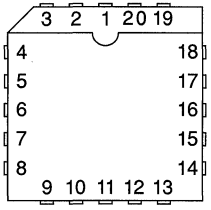
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (pin 3) 30V
Power inputs (pins 7 & 8) 30V
Output current, source or sink (pin 2)
DC 0.5A
Pulse (0.5 us) 2.0A
Enable and Current limit inputs (pins 4 & 6) ..... -0.3 to 6V
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Power Dissipation at $T_A \leq 25°C$ (SO-14) 725mW
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals (pin numbers refer to DIL-8 package).
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

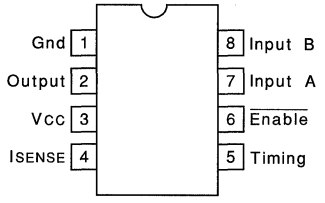
CONNECTION DIAGRAMS

PLCC-20 (Top View)
Q Package

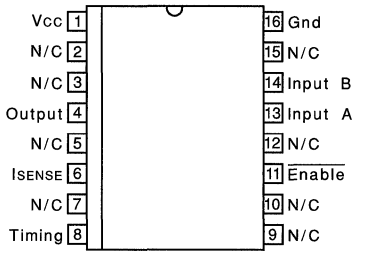


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
ISENSE	2
N/C	3-5
Timing	6
$\overline{\text{Enable}}$	7
N/C	8-9
Input A	11
N/C	12-14
Input B	15
Gnd	16
Vcc	17
N/C	18-19
Output	20

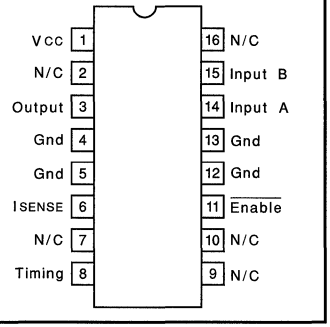
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package



DIL-16 (Top View)
JE Or NE Package



ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for $-55°C \leq T_A \leq +125°C$ for UC1725; $-25°C \leq T_A \leq +85°C$ for UC2725; $0°C \leq T_A \leq +70°C$ for UC3725; V_{CC} (pin 3) = 0 to 15V, R_T=10k, C_T=2.2nf, $T_A = T_J$, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER INPUT SECTION (PINS 7 & 8)					
Forward Diode Drop, Schottky Rectifier	I_F = 50ma		.55	.7	V
	I_F = 500ma		1.1	1.5	V
CURRENT LIMIT SECTION (PIN 4)					
Input bias current	V_{PIN4} = OV		-1	-10	µA
Threshold voltage		0.4	0.5	0.6	V
Delay to outputs	V_{PIN4} = 0 to 1V		100	250	ns
TIMING SECTION (PIN 5)					
Output Off Time		27	30	33	µs
Upper Mono Threshold		6.3	7.0	7.7	V
Lower Mono Threshold		1.9	2.0	2.3	V
HYSTERESIS AMPLIFIER (PINS 7 & 8)					
Input Open Circuit Voltage	Inputs (pins 7 & 8), Open Circuited, T_A= 25°C	7.0	Vcc/2	8.0	V
Input Impedance	T_A = 25°C	23	28	33	kΩ
Hysteresis		26.5	2*Vcc	30.5	V
Delay to Outputs	$V_{PIN7} - V_{PIN8} = V_{CC} + 1V$		100	300	ns

ELECTRICAL CHARACTERISTICS (cont.)

(Unless otherwise stated, these specifications apply for -55°C≤TA≤+125°C for UC1725; -25°C≤TA≤+85°C for UC2725; 0°C≤TA≤+70°C for UC3725; Vcc (pin 3) = 0 to 15V, Rt=10k, CT=2.2nf, TA =TJ, pin numbers refer to DIL-8 package.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE SECTION (PIN 6)					
High Level Input Voltage		2.1	1.4		V
Low Level Input Voltage			1.4	.8	V
Input Bias Current			-250	-500	µA
OUTPUT SECTION					
Output Low Level	IOUT = 20mA		0.35	0.5	V
	IOUT = 200mA		0.6	2.5	V
Output High Level	IOUT = -20mA	13	13.5		V
	IOUT = -200mA	12	13.4		V
	VCC = 30V, Iout = -20mA		14	15	V
Rise/Fall Time	CT = 1nf		30	60	ns
UNDER VOLTAGE LOCKOUT					
UVLO Low Saturation	20mA, VCC = 8V		0.8	1.5	V
Start-up Threshold		11.2	12	12.6	V
Threshold Hysteresis		.75	1.0	1.12	V
TOTAL STANDBY CURRENT					
Supply Current			12	16	ma

APPLICATION AND OPERATION INFORMATION

INPUTS: Figure 1 shows the rectification and detection scheme used in the UC1725 to derive both power and signal information from the input waveform. Vcc is generated by peak detecting the input signal via the internal bridge rectifier and storing on a small external capacitor, C1. Note that this capacitor is also used to bypass high pulse currents in the output stage, and therefore should be placed direclty between pins 1 and 3 using minimal lead lengths.

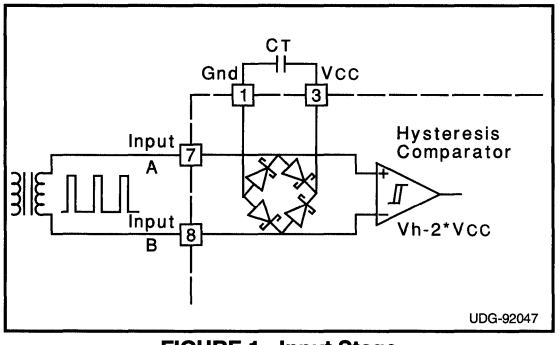


FIGURE 1 - Input Stage

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (resetting) the comparator only if the input signal exceeds Vcc (-Vcc). In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis amplifier as shown in Figure 3.

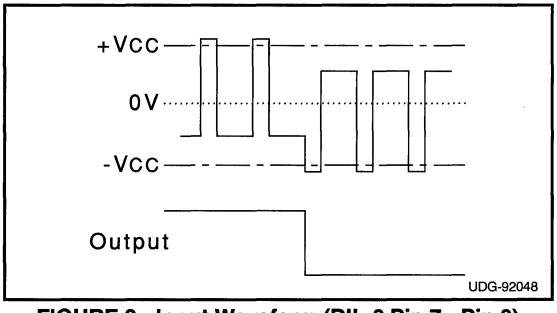


FIGURE 2 - Input Waveform (DIL-8 Pin 7 - Pin 8)

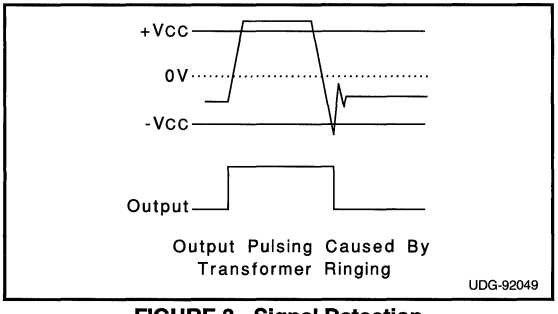


FIGURE 3 - Signal Detection

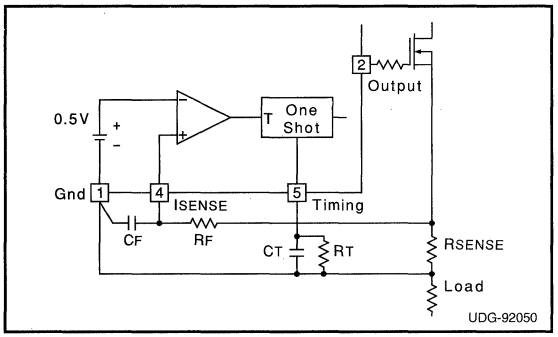


FIGURE 4 - Current Limit

CURRENT LIMIT AND TIMING: Current sensing and shutdown can be implemented directly at the output using the scheme shown in Figure 4. Alternatively, a current transformer can be used in place of RSENSE. A small RC filter in series with the input (pin 4) is generally needed to eliminate the leading edge current spike caused by parasitic circuit capacitances being charged during turn on. Due to the speed of the current sense circuit, it is very important to ground CF directly to Gnd as shown to eliminate false triggering of the one shot caused by ground drops.

One shot timing is easily programmed using an external capacitor and resistor as shown in Figure 4. This, in turn, controls the output off time according to the formula:

$$T_{OFF} = 1.28 \bullet RC.$$

If current limit feature is not required, simply ground pin 4 and leave pin 5 open.

OUTPUT: Gate drive to the power FET is provided by a totem pole output stage capable of sourcing and sinking currents in excess of 1 amp. The undervoltage lockout circuit guarantees that the high level output will never be less than 9 volts. In addition, during undervoltage lockout, the output stage will actively sink current to eliminate the need for an external gate to source resistor. High level output is also clamped to 15 volts. Under high capacitive loading however, the output may overshoot 2 to 3 volts, due to the drivers' inabitlity to switch from full to zero output current instantaneously. In a practical circuit this is not normally a concern. A few ohms of series gate resistance is normally required to prevent parasitic oscillations, and will also eliminate overshoot at the gate.

ENABLE: An enable pin is provided as a fast, digital input that can be used in a number of applications to directly switch the output. Figure 6 shows a simple means of providing a fast, high voltage translation by using a small signal, high voltage transistor in a cascode configuration. Note that the UC1725 is still used to provide power, drive and protection circuitry for the power FET.

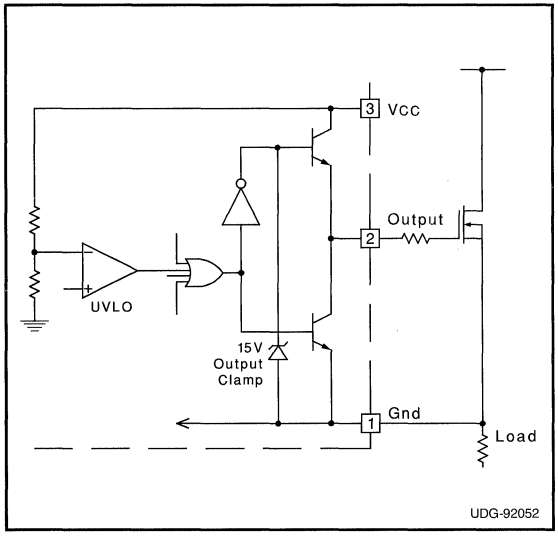


FIGURE 5 - Output Circuit

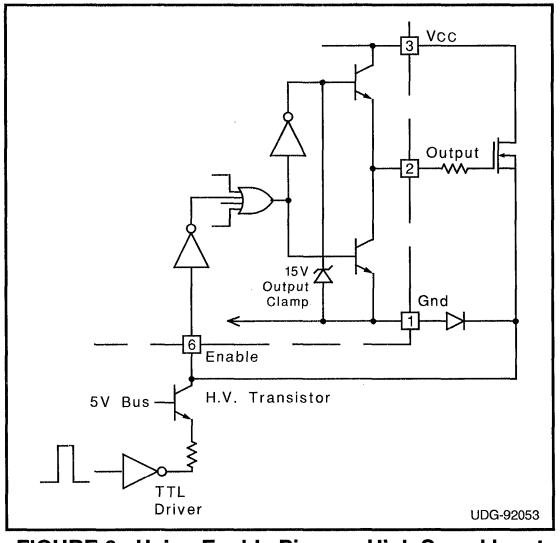


FIGURE 6 - Using Enable Pin as a High Speed Input Path

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application INFO available

UC1726
UC2726
UC3726

Isolated Drive Transmitter

FEATURES

- 750mA Output Drive, Source or Sink
- 8 to 35V Operation
- Transmits Drive Logic and Power through Low Cost Transformer
- Programmable Operating Frequency
- Up to 750kHz Operation
- Improved Output Control Algorithm Minimizes Output Jitter
- Fault Logic Monitors Isolated High Side IGBT Driver UC1727 for Faults
- User Programmable Fault Timing Screens False Fault Signals
- Shutdown Mode Disables On Chip Logic Reference for Low Standby Power
- Optional External Biasing of Logic Circuitry can Reduce Overall Power Dissipation

DESCRIPTION

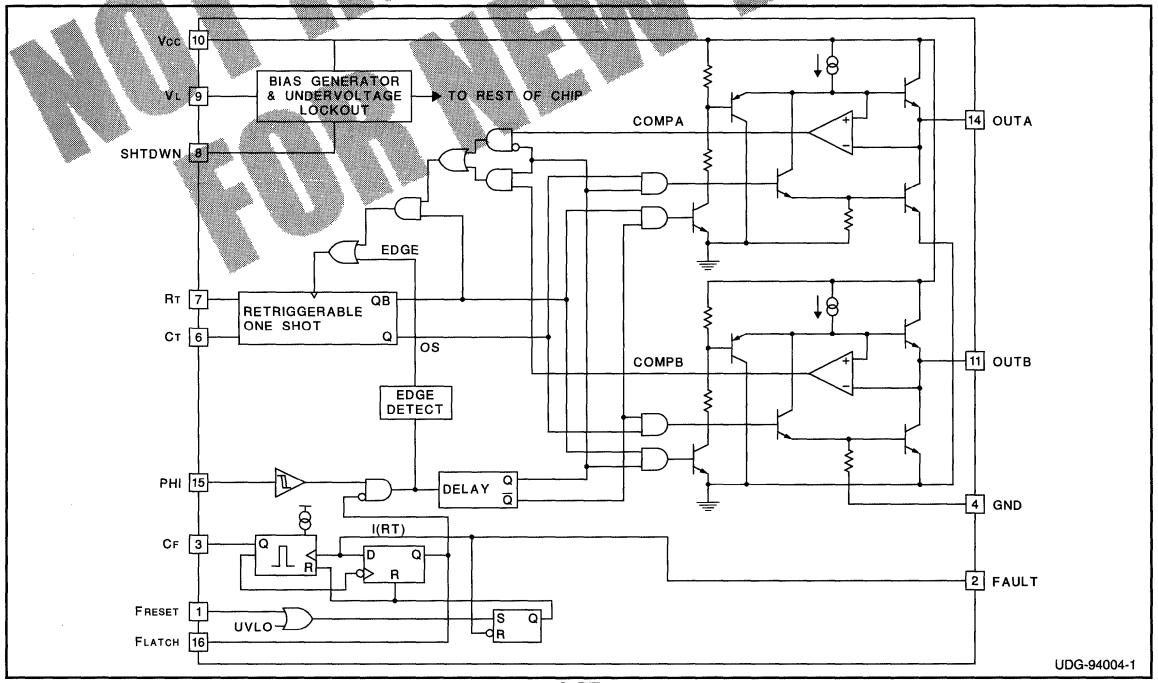
The UC1726 Isolated Drive Transmitter, and its companion chip, the UC1727 Isolated High Side IGBT Driver, provide a unique solution to driving isolated power IGBTs. They are particularly suited to drive the high side devices on a high voltage H-bridge. The UC1726 device transmits the drive logic and drive power, along with transferring and receiving fault information with the isolated gate circuit using a low cost pulse transformer.

This drive system utilizes a duty cycle modulation technique that gives instantaneous response to the drive control transitions, and reliably passes steady state, or DC conditions. High frequency operation, up to 750kHz, allows the cost and size of the coupling transformer to be minimized.

The UC1726 can be powered from a single V_{CC} supply which internally generates a voltage reference for the logic circuitry. It can also be placed into a low power shutdown mode that disables the internal reference. The IC's logic circuitry can be powered from an external supply, V_L, to minimize overall power dissipation. Fault logic monitors the Isolated High Side IGBT Driver UC1727 for faults. Based on user defined timing, the UC1726 distinguishes valid faults, which it responds to by setting the fault latch pin. This also disables the gate drive information until the fault reset pin is toggled to a logic one.

The UC1726 operates over an 8 to 35 volt supply range. The typical V_{CC} voltage will be greater than 28 volts to be compatible with the UC1727. The undervoltage lockout circuitry of the Isolated High Side IGBT Driver UC1727 locks out the drive information during its undervoltage lockout.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} 40V
Source/Sink Current (Pulsed)..... 1.5A
Source/Sink Current (Continuous)..... 1.0A
Output Voltage (pins 12, 14)..... –0.3 to (V_{CC} + 0.3)V
C_F, FRESET, FAULT, SHTDWN,
FLATCH, V_L, PHI, R_T ..... –0.3 to 6.0V
C_T ..... 1.0 to 6.0V
Operating Junction Temperature (Note 2) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 seconds)..... 300°C

Note 1: All voltages are with respect to GND (Pin 2); all currents are positive into, negative out of part.

RECOMMENDED OPERATING CONDITIONS (Note 3)

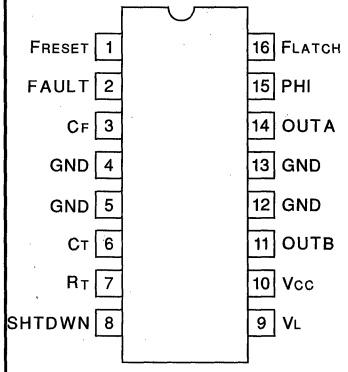
Input Voltage..... +9 to +35.0V
Sink/Source Current (each output)..... 0 to 750mA
Timing Resistor..... 2.4k to 200kΩ
Timing Capacitor (C_T)..... 75pF to 2.0nF
Timing Capacitor (C_F)..... 75pF to 3.0nF

Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

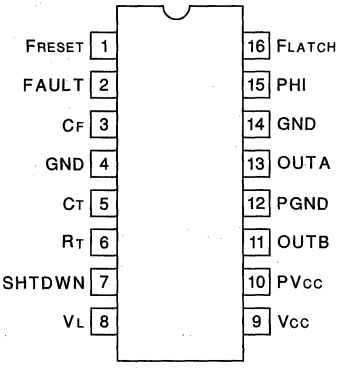
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

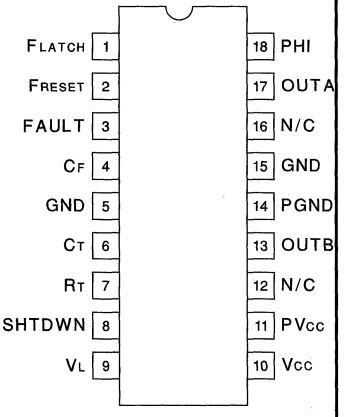
DIL-16 (Top View)
N Package



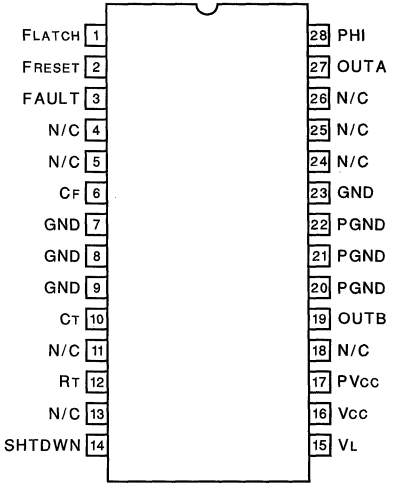
DIL-16 (Top View)
SP Package



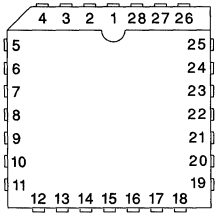
DIL-18 (Top View)
J Package



SOIC-28 (Top View)
DWP Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
GND	1
C_T	2
N/C	3-4
R_T	5
SHTDWN	6
V_L	7
V_{CC}	8
N/C	9
PV_{CC}	10
OUTB	11
PGND	12-18
GND	19
OUTA	20
PHI	21
FLATCH	22
FRESET	23
FAULT	24
N/C	25
C_F	26
N/C	27
N/C	28

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, V_{CC} = 20V, R_T = 4.32kΩ, C_T = 330pF and C_F = 2.2nF, no load on any output, and –55°C < T_A < 125°C for the UC1726, –40°C < T_A < 85°C for the UC2726, and 0°C < T_A < 70°C for the UC3726, T_A = T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Retriggerable one shot					
Initial Accuracy	T_J = 25°C	1.400	1.600	1.800	µsec
Temperature Stability	Over operating T_J	1.000		2.200	µsec
Voltage Stability	V_{CC} = 10 to 35V		0.2		%/V
Operating Frequency	L_{LOAD} = 1.5mH		170		kHz
PHI Input (Control Input)					
HIGH Input Voltage		2.0			V
LOW Input Voltage				0.8	V
HIGH Input Current			10		µA
LOW Input Current			-300	–600	µA
Delay to one shot			100	250	nsec
Delay to Output	C_T = 1.4V		250		nsec
Output Drivers					
Output Low Level	I_{SINK} = 20mA		0.3	0.5	V
	I_{SINK} = 400mA		0.5	2.6	V
Output High Level	I_{SOURCE} = –20mA		2.0	2.6	V
(volts below V_{CC})	I_{SOURCE} = –400mA		2.0	2.9	V
Rise and Fall Times	No load		30	60	nsec
Logic Voltage Reference					
V_L - Logic Voltage	Internal Voltage	4.20	4.40	4.60	V
Logic Supply Current	V_L = 4.75V to 5.25V, C_T = 1.4V		13.0	20.0	mA
Shut Down Circuit					
Logic Voltage - Off			0.5		V
High Input Current	V_{IH} = 2.4			-100	µA
Low Input Current	V_{IL} = 0.4			-20	µA
Fault Logic					
Fault Reset High Input Current	V_{IH} = 2.4			±5	µA
Fault Reset Low Input Current	V_{IL} = 0.4			-10	µA
Fault High Input Current	V_{IH} = 2.4			±5	µA
Fault Low Input Current	V_{IL} = 0.4			-60	µA
Fault Pulse Width	C_F = 330pF		3.0		µs
	C_F = 2.2nF		17.0		µs
Fault Latch, V_{OH}	I_{LOAD} = –1mA, Volts below V_L		1.3	1.8	V
Fault Latch, V_{OL}	I_{LOAD} = 1mA		0.25	0.5	V
Fault Latch, V_{OH}	I_{LOAD} = 0, Volts below V_L		0.3		V
Fault Latch, V_{OL}	I_{LOAD} = 0		0.2		V
Fault Reset Pulse Width			500		ns
UVLO					
Turn On Threshold			7.1		V
Total Supply Current					
Supply Current	C_T = 1.4V		22	40	mA
	C_T = 1.4V, V_L = 5.0V		12	20	mA
	C_T = 1.4V, Shutdown = 5.0V		2.5		mA

Refer to Typical Application on Page 5 and Application Note U-143C "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

CF: The timing input to the fault logic. A capacitor is placed across the input of CF and ground. The timing window is approximately $t = 2.1C_FR_T$.

CT: The connection to the timing capacitor that controls the operating frequency. A capacitor to ground is repetitively charged during the one shot pulse width. It is discharged when a comparator senses zero current in the primary side of the transformer. The one shot pulse width is consequently determined by the time it takes to charge the capacitor from a threshold voltage of $V_L/4$ to $V_L/2$. This pin must be tied to a capacitor. See Recommended Operating Conditions.

FAULT: This input to the fault logic initiates the user programmable timer. This time interval, specified by the capacitor on CF, determines the validity of the fault. The pin is tied to a low cost optocoupler, and is high until the UC1727 sends drive information from the PHI pin through the transformer while the FAULT pin stays low. Once this pin goes high, it must stay high during the entire fault window to be accepted as a valid fault. A valid fault sets the FLATCH pin high and prevents the transmitting of gate drive information until the FRESET is toggled high. If fault logic is not used, the FAULT pin must be grounded.

FLATCH: A valid fault sets this pin to a logic one and prevents the transmitting of gate drive information. The FLATCH pin can only be reset by connecting the FRESET to a logic 0.

FRESET: The input to the fault logic that resets the fault logic latch (FLATCH) and enables drive transmit data. This input must be low when powered up and stay low until after the fault latch has been set.

GND: The signal and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground which biases the remainder of the device.

OUTA: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between 0.3V during the one shot charge time and approximately V_{CC} + 0.4V during the remainder of the period. When PHI is low the output toggles between V_{CC} - 2V during the one shot charge time and approximately $0.6V_{CC}$ during the remainder of the period.

OUTB: One output of the two totem pole outputs connected across the transformer primary winding. When PHI is high, the output toggles between V_{CC} - 2V during the one shot charge time and approximately $0.6V_{CC}$ during the remainder of the period. When PHI is low the output toggles between 0.3V during the one shot charge time and approximately V_{CC} + 0.4V during the remainder of the period.

PGND: This is the ground for the output transistors bonded in the 28 pin packages. On the sixteen pin packages it is bonded separately to the GND pin.

PHI: A logic control input to the isolated gate drive that changes the outputs as described above. This changes the duty cycle of the voltage wave form applied across the transformer. The Isolated High Side IGBT Driver UC1727 senses the different duty cycles as different drive commands.

PVCC: This is the input voltage for the output transistors on the 28 pin package. On the sixteen pin packages it is bonded separately to the V_{CC} pin.

RT: The input that sets the CT and CF capacitor currents with a resistor to ground. The voltage on RT is approximately $0.3V_L$. The resulting charge currents are: $I_{CT} = I_{CF} = V_L / 4R_T$.

SHTDWN: This input shuts down the internal reference. A TTL logic one puts the UC1726 into a low standby current mode. This input has a pull down resistor on the chip to guarantee proper operation when left open. If an external logic voltage is applied to V_L, this shutdown feature cannot be used without bringing the external voltage source to zero volts.

VCC: The input voltage that biases the outputs and the internal reference. It can vary between 8V to 35V. This supply pin will typically be greater than 28V to be compatible with the UC1727. In order to minimize power dissipation use an external logic supply, V_{CC} approximately 15V, and a step up transformer (N = 2).

VL: The logic supply pin that biases all circuits except for the totem pole outputs. A bypass capacitor is recommended on this pin when left unconnected. The internal reference is approximately 4.4V. A 5.0V supply can be applied to this pin to assure minimum power dissipation. When an external supply higher than the V_L voltage is applied to this pin, the internal reference turns off.

OPERATING FREQUENCY:

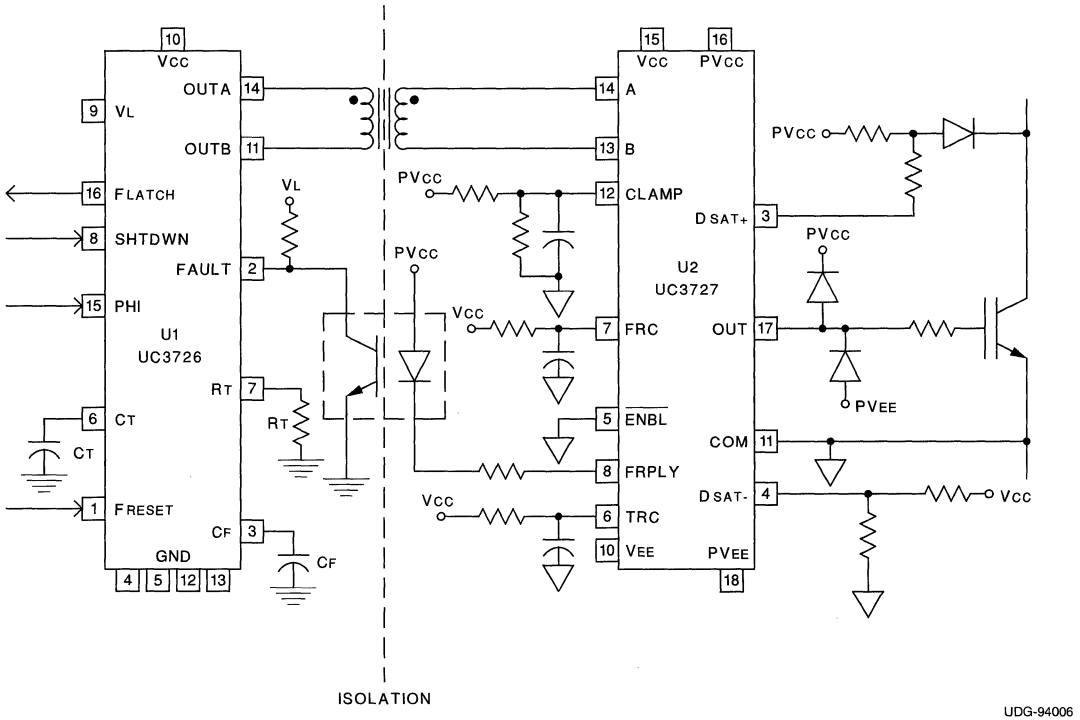
The chip operating frequency is determined by the values of components connected to the RT and CT pins. A resistor connected between RT and ground sets the charge current to ICT = VL / 4RT. The operating frequency varies slightly depending on the VCC and VL voltages. The following equations approximate the one shot pulse width at operating frequency when VCC = 20V.

$$T_{PW} = 1.1R_T(C_T + 50pF)$$

$$F_O = \frac{1}{3.3R_T(C_T + 50pF)}$$

The 50pF additional capacity represents internal chip capacitance at the CT input.

TYPICAL APPLICATION



IF FAULT LOGIC NOT USED, GROUND FAULT PIN.

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application INFO available

UC1727
UC2727
UC3727

Isolated High Side IGBT Driver

FEATURES

- Receives Power and Signal from Single Isolation Transformer
- Generates Split Rail for 4A Peak Bipolar Gate Drive
- 16V High Level Gate Drive
- Low Level Gate Drive more Negative than -5V
- Undervoltage Lockout
- Desaturation Detection and Fault Processing
- Separate Output Enable Input
- Programmable Stepped Gate Drive for Soft Turn On
- Programmable Stepped Gate Drive for Soft Fault

DESCRIPTION

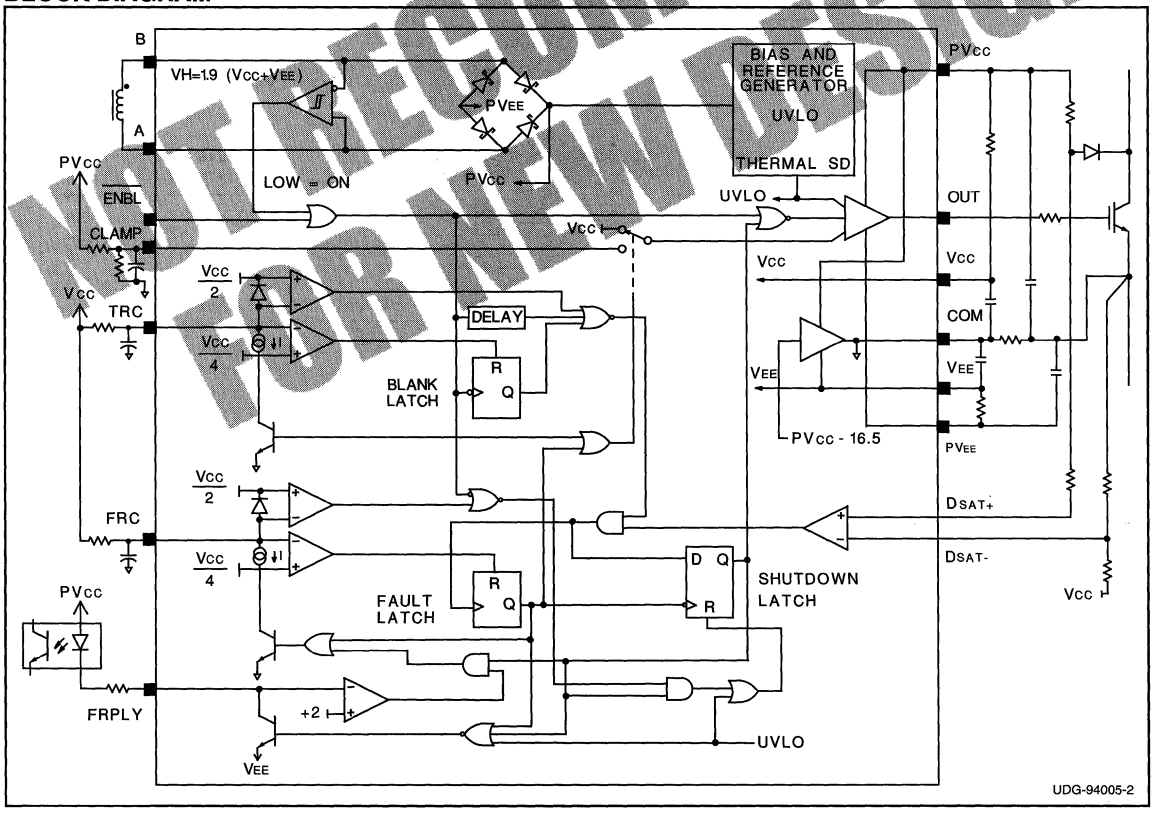
The UC1727 and its companion chip, the UC1726, provide all the necessary features to drive an isolated IGBT transistor from a TTL input signal. A unique modulation scheme is used to transmit both power and signal across an isolation boundary with a minimum of external components.

Protection features include under voltage lockout and desaturation detection. High level gate drive signals are typically 16V. Intermediate high drive levels can be programmed for various periods of time to limit surge current at turn on and in the event of desaturation due to a short circuit.

The chip generates a bipolar supply so that the gate can be driven to a negative voltage insuring the IGBT remains off in the presence of high common mode slew rates.

Uses include isolated off-line full bridge and half bridge drives for motors, switches, and any other load requiring full electrical isolation.

BLOCK DIAGRAM



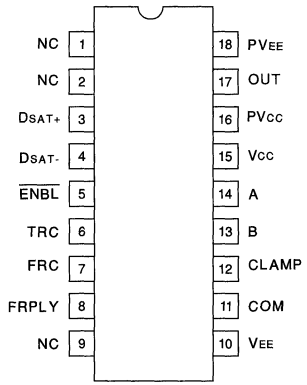
ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{CC} - V_{EE}) 40V
Power Inputs (IA - BI) 45V
Analog Input Voltage ($\overline{ENBL}$, CLAMP) ..... -0.3 To Vcc+0.3
Analog Input Voltage (D_{SAT+}, D_{SAT-}) ..... V_{EE}-0.3 to V_{CC}+0.3
Analog Input Current (D_{SAT+}, D_{SAT-}) ..... -10 to 10mA
Output Current, |I(OUT)|
DC 0.8A
Pulse (0.5µs) 4A
FRPLY Output Current 30mA

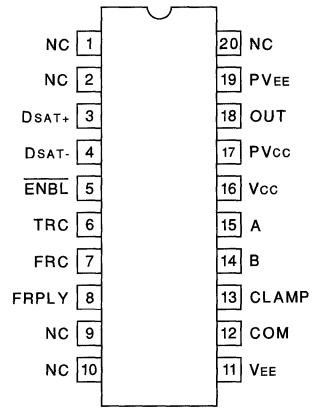
Note: All voltages are with respect to COM. Currents are positive into the specified terminal.

CONNECTION DIAGRAMS

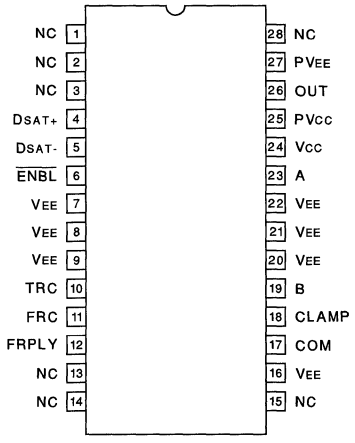
DIL-18 (Top View)
J Package



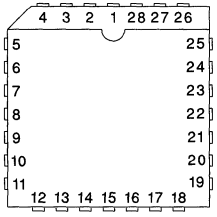
DIL-20 (Top View)
N Package



SOIC-28 (Top View)
DWP Package

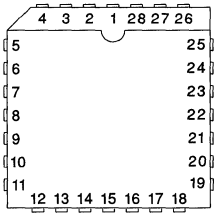


PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
PV_{EE}	12-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26
N/C	27
N/C	28

LCC-28 (Top View)
LP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
V_{EE}	2
N/C	3-4
COM	5
CLAMP	6
B	7
A	8
V_{CC}	9
PV_{CC}	10
OUT	11
N/C	12-13
PV_{EE}	14
N/C	15-18
D_{SAT+}	19
D_{SAT-}	20
$\overline{ENBL}$	21
NC	22
TRC	23
FRC	24
FRPLY	25
N/C	26-28

See Application Note U-143A "New Chip Pair Provides Isolated Drive for High Voltage IGBTs"

PIN DESCRIPTIONS

A, B: Signal and power input pins. Connect these pins to the secondary of the transformer driven by UC1726.

CLAMP: Analog programming pin for intermediate drive level to be used at turn on or in response to a desaturation event. Requires a bypass capacitor to COM.

COM: Self generated common for bipolar supply. This pin will be 16.5V below PVCC.

DSAT+, DSAT-: Inputs to the desaturation comparator. Desaturation is detected when DSAT+ is greater than DSAT-.

$\overline{\text{ENBL}}$: Negative true enable input. Tie to VCC to disable the chip. Connect to COM to enable the chip. If the $\overline{\text{ENBL}}$ pin is used as the primary input to the chip, connect B to VCC and A to VEE.

FRC: Fault Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential during a desaturation event before it is driven fully low. Also sets the period of time that OUT will be held low before allowing it to be driven high again.

FRPLY: Fault Reply pin. Open collector output. Normally connected to VEE. When desaturation is detected, the pin opens.

OUT: Gate drive output. Connect to gate of IGBT with a series damping resistor greater than 3 ohms.

TRC: Timing Resistor and Capacitor. Programs the duration that OUT will be held at CLAMP potential and the period of time the desaturation comparator will be ignored during the rising edge.

VCC: Positive supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

VEE: Negative supply voltage. Bypass to COM with a low ESL/ESR 1µF capacitor.

PVEE: Output driver negative supply. Connect to VEE with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

PVCC: Output driver positive supply. Connect to VCC with a 3.3 ohm resistor and bypass to COM with a low ESL/ESR 1µF capacitor.

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, VCC - VEE = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Input Receivers					
Forward Diode Drop	I_F = 50mA		0.5	0.65	V
	I_F = 500mA		1.2	2	V
VCC Regulator					
VCC	25 ≤ (VCC - VEE) ≤ 36V, | I(COM) | ≤ 15mA	15.5	16.5	17.5	V
Hysteresis Comparator					
Input Open Circuit Voltage	(Measured with respect to VEE)		12		V
Input Impedance			100		kΩ
Hysteresis		44	47	50	V
Enable Input					
High Level Input Voltage		12			V
Low Level Input Voltage				5	V
Input Bias Current	$\overline{\text{ENBL}}$ = COM		–460	–900	µA
Output Driver					
Saturation to VCC	I(OUT) = -20mA		1.7	2.3	V
Saturation to VCC	I(OUT) = -500mA		2	2.5	V
Saturation to VEE	I(OUT) = 20mA		2	3	V
Saturation to VEE	I(OUT) = 500mA		2.4	3.6	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C for the UC1727, T_A = –40°C to 85°C for the UC2727, T_A = 0°C to 70°C for the UC3727, R(TRC) = 54.9k, C(TRC) = 180pF, R(FRC) = 309K, C(FRC) = 200pF, V_{CC} - V_{EE} = 25V, CLAMP = 9V, T_A = T_J, and all voltages are measured with respect to COM.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Driver (cont.)					
Turn on Clamp Voltage	I(OUT) = -100mA	7	9	11	V
Fault Clamp Voltage	II(OUT)I = 100mA	8	10	12.5	V
UVLO Saturation to V_{EE}	I(OUT) = 20mA,V_{CC} no connection		2	3	V
Rise and Fall Times	Cl = 1n, CLAMP = V_{CC}, R_{OUT} = 3Ω (Note 1)		75	150	ns
Turn On Sequence Timer					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Blanking Time	(Note 1)	3	5	7	µs
Fault Manager					
Clamped Driver Time	(Note 1)	0.4	1	1.7	µs
Fault Lock Off Time	(Note 1)	15	25	35	µs
FRPLY Saturation	I(FRPLY) = 10mA		1.8	3	V
FRPLY Leakage	FRPLY = V_{CC}		0	10	µA
Desaturation Detection Comparator					
Input Offset Voltage (Iviol)	V_{CM} = V_{EE}+2, V_{CM} = V_{CC}-2		0	20	mV
Input Bias Current			–1.5	10	µA
Delay to Output	C(FRC) = 0 (Note 1)		150		ns
Undervoltage Lock Out					
V_{CC} Threshold		14	15.5	17	V
V_{CC} Hysteresis			0.35		V
V_{EE} Threshold		–4.5	–5.5	–6.5	V
V_{EE} Hysteresis		0.5	1	1.5	V
Thermal Shutdown					
Threshold	Not tested		175		°C
Hysteresis	Not tested		45		°C
Total Standby Current					
I(V_{CC})			24	30	mA

Note 1: Guaranteed by design, but not 100% tested in production.

APPLICATION INFORMATION

Figure 1 shows the rectification and detection scheme used in the UC1727 to derive both power and signal information from the input waveform. V_{CC}-V_{EE} is generated by peak detecting the input signal via the internal bridge rectifier and storing it on external capacitors. COM is generated by an internal amplifier that maintains PV_{CC}-COM = 16.5V.

Signal detection is performed by the internal hysteresis comparator which senses the polarity of the input signal as shown in Figure 2. This is accomplished by setting (or resetting) the comparator only if the input signal exceeds 0.95|V_{CC}-V_{EE}|. In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator as shown in Figure 3.

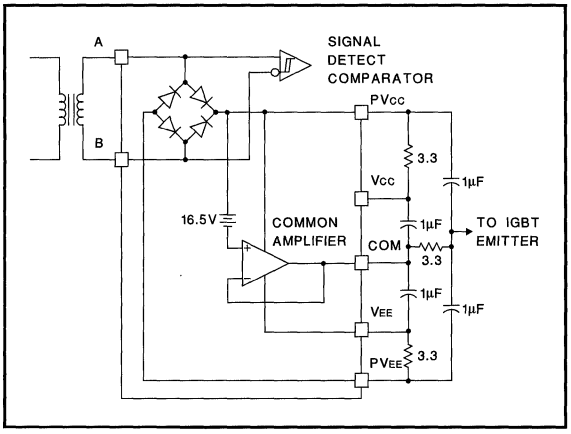


Figure 1. Input Stage & Bipolar Supply

APPLICATION INFORMATION (cont.)

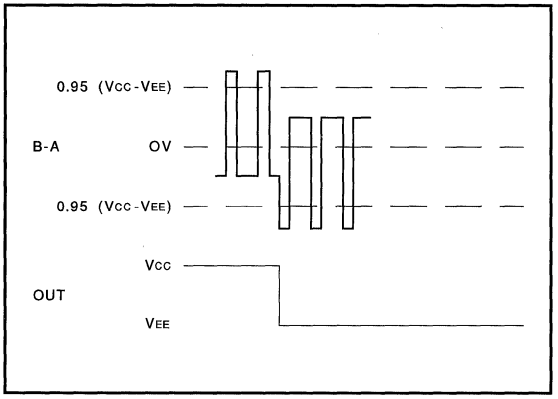


Figure 2. Input Waveform

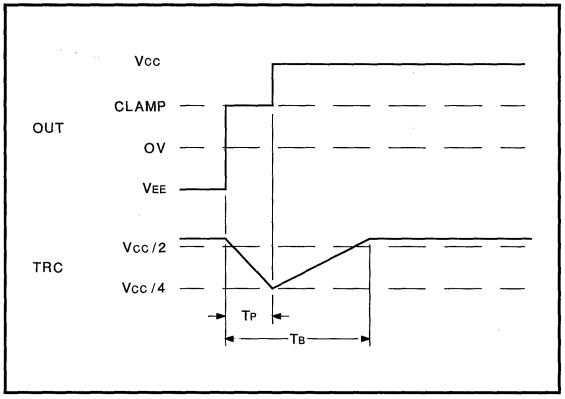


Figure 4. Rising Edge Waveform

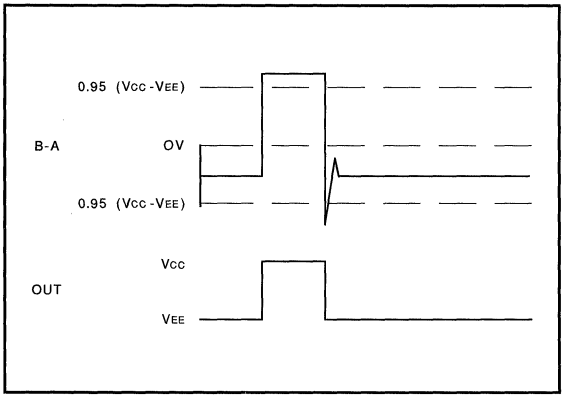


Figure 3. Output Pulsing Caused By Transformer Ringing

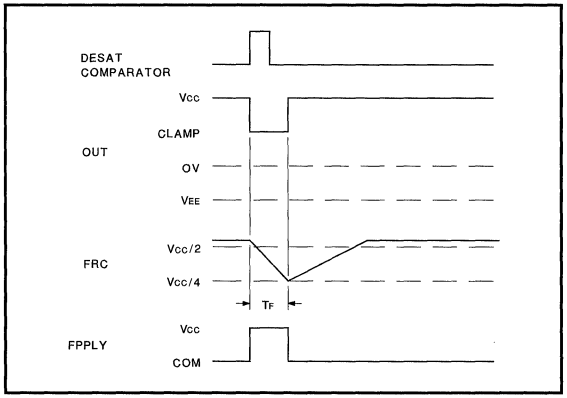


Figure 5. Transient Desaturation Response

GATE DRIVE WAVEFORM

The rising edge of OUT can be programmed for a two step sequence as shown in Figure 4. The plateau voltage is programmed by a resistive divider from VCC to COM applied at CLAMP. CLAMP must be bypassed to COM. The plateau voltage is approximately OUT = CLAMP. The plateau time is set by a resistor from TRC to VCC and a capacitor to COM as:

$$Tp = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

TRC also programs a blanking time during which the chip ignores the desaturation comparator. The blanking time is:

$$Tb = Tp + 0.4RC.$$

In the event that desaturation is detected outside the blanking interval, OUT will be driven back to the CLAMP plateau for a fault time set by a resistor from FRC to VCC and a capacitor to COM as:

$$Tf = RC \ln\left(\frac{R-7.6k}{R-12.4k}\right).$$

If the event is transient, OUT will return high at the end of Tf as shown in Figure 5. During Tf, FRPLY is open. After Tf, FRPLY is connected to COM.

Desaturation shown in Figure 6 that persists longer than Tf will cause OUT to be driven low. The chip will not accept a command to drive OUT high for a delay period of

$$Td = 0.4RC$$

FRPLY will be open during this entire period.

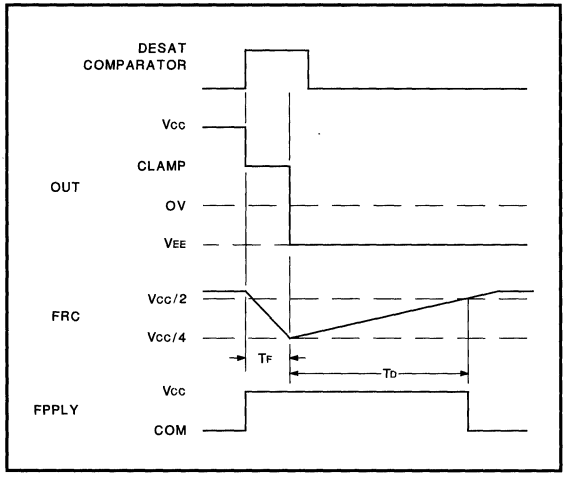


Figure 6. Desaturation Response

ENABLE

$\overline{\text{ENBL}}$ provides an alternate means of controlling the output. If $\overline{\text{ENBL}}$ is used as the primary input, B must be connected to VCC and A to VEE. $\overline{\text{ENBL}}$ can be driven by the output of an optoisolator from $\overline{\text{ENBL}}$ to COM as shown in Figure 7. If $\overline{\text{ENBL}}$ is not used, it should be connected to COM.

EXTERNAL BIPOLAR SUPPLIES

If it is desired to drive an emitter grounded IGBT from external supplies, the configuration in Figure 8 should be used. COM should never be connected to ground. VCC must be ≥ 12V and VCC-VEE must be ≥ 23.5V.

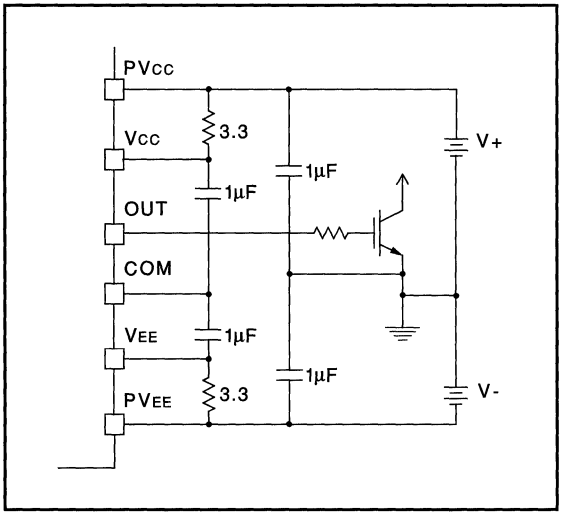


Figure 8. Using External Supplies

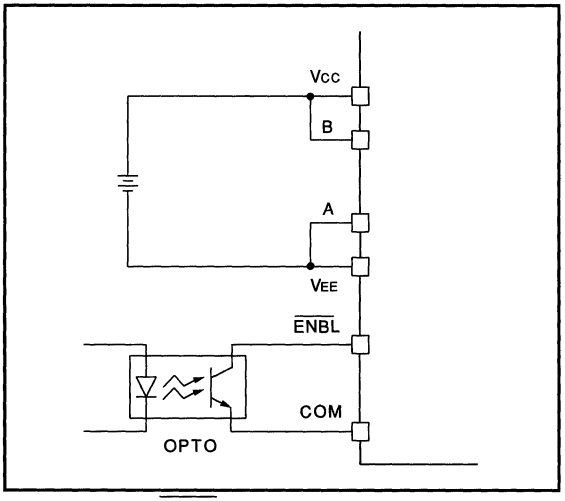


Figure 7. Using $\overline{\text{ENBL}}$ as Primary Input

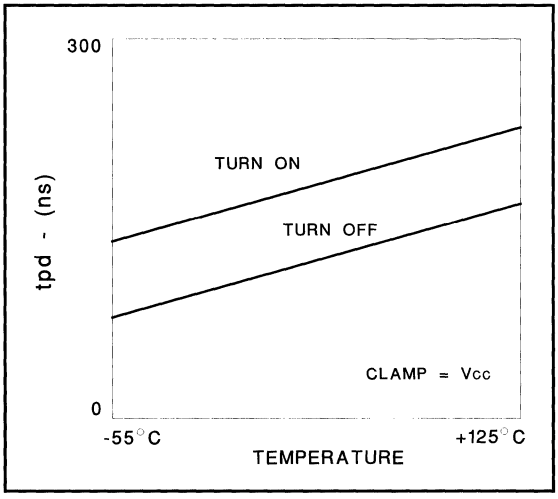


Figure 9. Input to Output Delay

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Dual 3A MOSFET Driver

FEATURES

- Built using BCDMOS Process
- High Peak Output Current (3A)
- Self Biasing Active Off Outputs
- Pinout Compatible with Industry Standard Drivers
- Undervoltage Lockout (UVLO)
- High Capacitive Load Drive Capability
- CMOS Compatible Input Threshold
- Wide Operating Voltage Range from 4.5V to 18V

DESCRIPTION

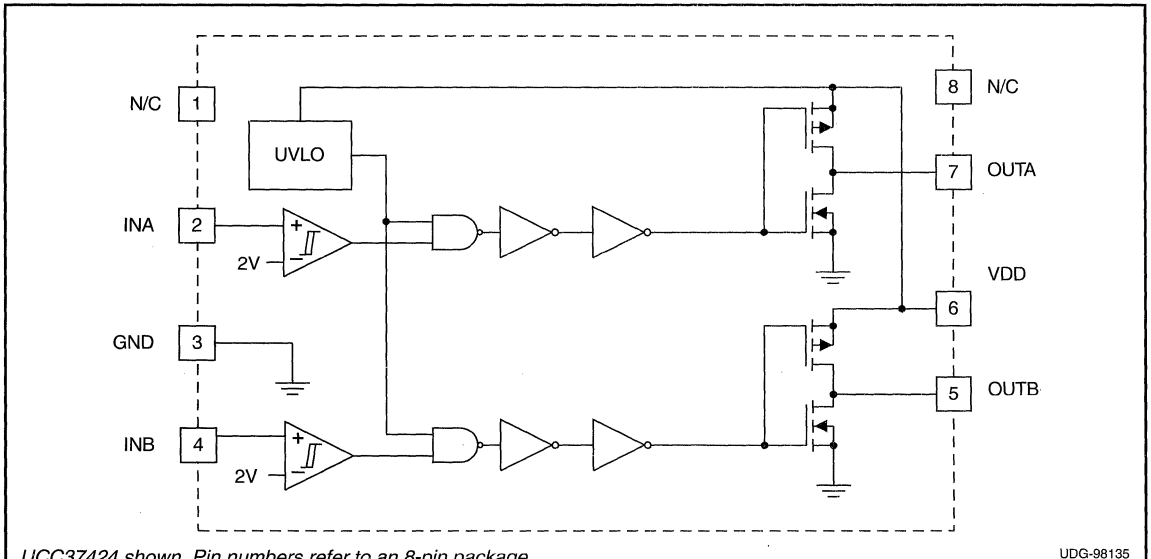
The UCC37423/37424/37425 devices are high speed, dual MOSFET drivers using the BiCMOS/DMOS process. All three devices are designed to be pin and performance compatible with industry standard '423, '424, '425, '426A, '427A, and '428A drivers. Each of the dual outputs is capable of providing 3A peak current and 6A in parallel. In addition, the devices feature Undervoltage Lockout (UVLO) protection and an improved input noise immunity.

The UCC37423 is a dual inverting driver. The UCC37424 is a dual non-inverting driver. The UCC37425 contains one inverting and one non-inverting driver.

In addition to driving two power MOSFETs in high power and high frequency switch mode power supply and motion control applications, these drivers are also capable of driving capacitive and inductive loads in applications such as small motor, relay, solenoid and actuator drivers. Unlike Bipolar Gate Driver ICs, these BCDMOS drivers do not require external Schottky clamp diodes for slight negative voltage overshoot protection.

UCC37423/37424/37425 family of drivers are available in 8 pin SOIC (D), PDIP (N) or CDIP (J), or 16 pin SOIC-Power (DP) packages.

BLOCK DIAGRAM



UCC37424 shown. Pin numbers refer to an 8-pin package.

UDG-98135

ABSOLUTE MAXIMUM RATINGS

Supply voltage 20V
Output Current (OUTA, OUTB) DC 0.2A
Output Current (OUTA, OUTB) DC . . . . . Pulsed (0.5 usec) 5A
Input voltage (pins INA, INB) . . . . . –5V to VDD+0.3V
Storage Temperature Range . . . . . –65 °C to +150°C
Operating Junction Temperature . . . . . –65 °C to +150°C
Lead Temperature (soldering 10 sec) . . . . . +300°C

Unless otherwise indicated, voltages are referenced to GND pin and currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of the packages.

ORDERING INFORMATION

UCC☐742☐☐

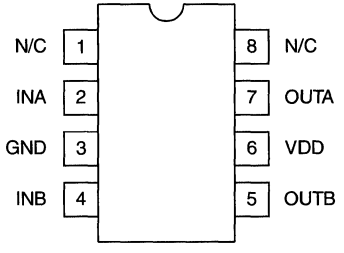
- PACKAGE SUFFIX
- OUTPUT CONFIGURATION
- TEMPERATURE RANGE

	Temperature Range	Package Suffix
UCC1742X	–55°C to +125°C	J
UCC2742X	–40°C to +85°C	D, DP, N
UCC3742X	0°C to +70°C	D, DP, N

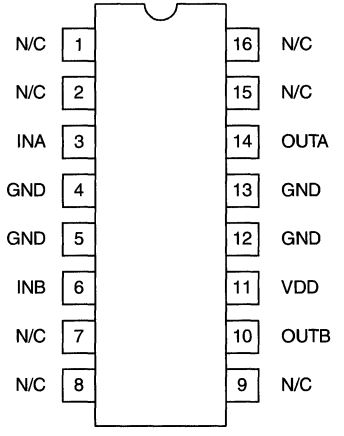
	Output Configuration
UCCX7423	Dual Inverting
UCCX7424	Dual Non-Inverting
UCCX7425	One Inverting, One Non-Inverting

CONNECTION DIAGRAMS

DIP-8, SOIC-8 (TOP VIEW)
N or J, D Packages



DIL-16 (TOP VIEW)
DP Package



POWER DISSIPATION RATING TABLE

PACKAGE	SUFFIX	T_A < 25 DEG C Power Rating (mW) *	Derating Factor Above T_A = 25°C (mW/°C) *	T_A = 70°C Power Rating (mW) *	T_A = 85°C Power Rating (mW) *	THETA (jc)	THETA (ja)
8 pin SOIC	D **	625 – 1190	6.25 – 11.90	344 – 655	250 – 476	42°C/W	84-160°C/W
8 pin Plastic DIP	N	909	9.09	500	364	49	110
16 pin Power SOIC	DP **	1724-2778	17.24 – 27.78	948 – 1528	690 – 1111	20	36-58
8 pin Ceramic DIP	J	625	6.25	344	250	26	160

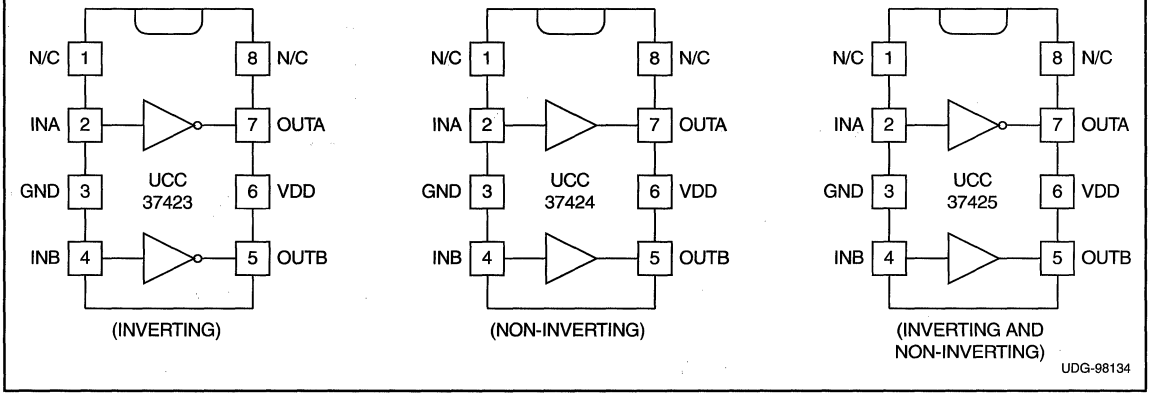
** +125°C operating junction temperature is used for power rating calculations.*

*** The range of values indicate the effect of pc-board. The lower value is for a device mounted on a 5.0 square inch, 0.062 inch think aluminum pc-board. The higher value is for a device mounted on a 5.0 square inch single sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For additional information on device temperature management, please refer to Packaging Information section in Unitrode Databook.*

INPUT/OUTPUT TABLE

INPUTS (V_{IN_L}, V_{IN_H})		UCC37423		UCC37424		UCC37425	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	H	H	L	L	H	L
L	H	H	L	L	H	H	H
H	L	L	H	H	L	L	L
H	H	L	L	H	H	L	H

PART VERSIONS



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Section					
V_{IN_H}, Logic 1 Input Threshold (INA, INB)		2.4			V
V_{IN_L}, Logic 0 Input Threshold (INA, INB)				1.6	V
Input Current (INA, INB)	0V ≤ V(IN[AB]) ≤ VDD	–10	0	10	µA
Output Section					
V_{OH}, Output OUTA, OUTB High Level	$V_{OH} = V_{DD} - V_{OUT}$, I_{OUT} = –10mA		20	50	mV
V_{OL}, Output OUTA, OUTB Low Level	I_{OUT} = 10mA		20	50	mV
Output Resistance High	I_{OUT} = –10mA, VDD = 18V		1.8	3	Ω
Output Resistance Low	I_{OUT} = 10mA, VDD = 18V		1.8	3	Ω
Peak Output Current	(Note 1)		3		A
Latch-up Protection	(Note 1)	> 500			mA
Switching Time Section					
t_R, OUTA,OUTB Rise Time	C_{LOAD} = 1800 pF (See Fig. 1)		20	60	ns
t_F, OUTA,OUTB Fall Time	C_{LOAD} = 1800 pF (See Fig. 1)		20	60	ns
t_{D1}, Delay (IN[AB] to OUT[AB]) Rising	C_{LOAD} = 1800 pF (See Fig. 1)		50	100	ns
t_{D2}, Delay (IN[AB] to OUT[AB]) Falling	C_{LOAD} = 1800 pF (See Fig. 1)		50	100	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout Section					
Start Threshold		4.2	4.3	4.5	V
Start to Stop Hysteresis		0.4	0.6	0.9	V
Power Supply Section					
Operating Current	Static, Inputs = 0V		3.5	5	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

GND: Common ground. This ground should be connected very closely to the source of the power MOSFET which the driver is driving.

INA: Input A. Input signal for the A driver, logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should NOT be left floating.

INB: Input B. Input signal for the B driver, logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should NOT be left floating.

OUTA: Driver output A. This complementary MOS output swings to both VDD and GND.

OUTB: Driver output B. This complementary MOS output swings to both VDD and GND.

APPLICATION INFORMATION

Supply Section

The IC operates over a wide supply range, from 4.5V to 18V.

Input Section

The input circuit contains hysteresis to maximize noise immunity. The inputs are designed such that they can swing up to 5V below GND without damage to the IC.

Output Section

The output circuit is designed to drive a MOSFET gate on and off in 20nsec typically. The output will supply a high peak output current (3A peak). The output of the driver uses complementary devices and will swing the gate fully between the two supply rails. The outputs are designed to withstand 500mA reverse current without either damage or logic upset. The outputs are actively pulled down during undervoltage lockout even in the absence of VDD power.

Inverting outputs of UCC37423 and OUTA of UCC37425 are intended to drive external P-channel MOSFETs. Non-inverting outputs of UCC37424 and OUTB of UCC37425 are intended to drive N-channel MOSFETs.

Undervoltage Lockout Section

The under voltage detection circuit prevents the outputs from turning on the external power MOSFET when VDD is below a preset value.

When the IC is in an Undervoltage mode, the output states will be the same as if the input was low during normal operation. For example, outputs of UCC37423 (inverting) will be held high, outputs of UCC37424 (non-inverting) will be held low and outputs of UCC37425 (inverting + non-inverting) will be held high and low respectively for OUTA and OUTB. Under this mode, the inverting outputs on UCC37423 and OUTA of UCC37425 will track VDD.

APPLICATION INFORMATION (cont.)

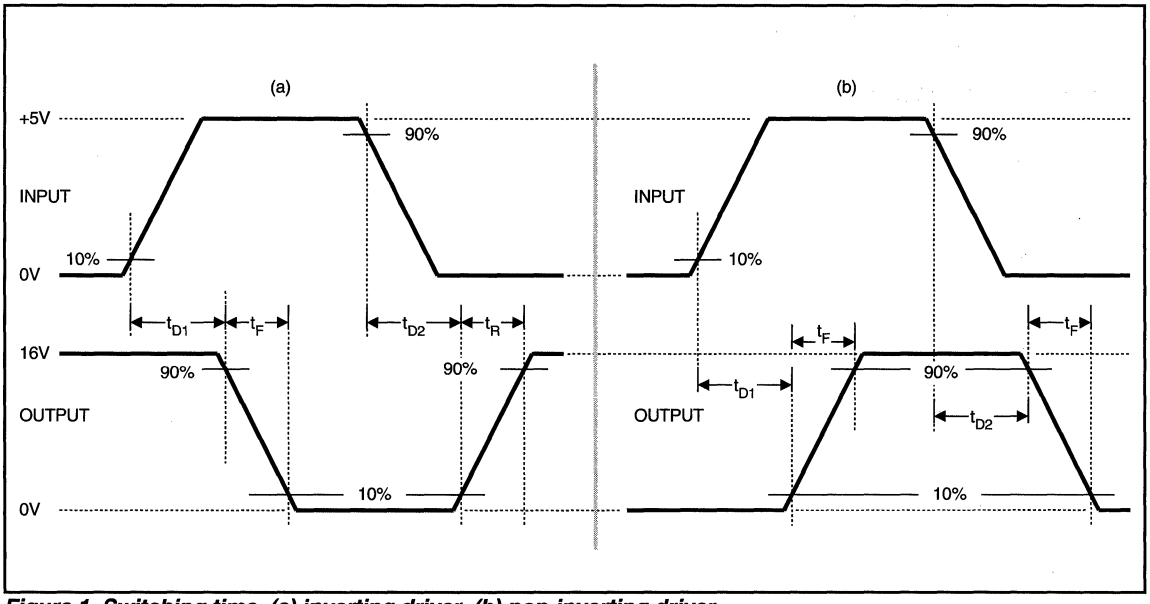


Figure 1. Switching time (a) inverting driver (b) non-inverting driver.

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Dual 3A MOSFET Driver With Adaptive LEB

FEATURES

- Built using BCDMOS Process
- High Peak Output Current (3A)
- Self Biasing Active Off Outputs
- Pinout Compatible with Industry Standard Drivers
- Patent Pending Adaptive Leading Edge Blanking (LEB)
- Undervoltage Lockout (UVLO)
- High Capacitive Load Drive Capability
- CMOS Compatible Input Threshold
- Wide Operating Voltage Range from 4.5V to 18V
- Shutdown Capability via Logic Level Input ENBL

DESCRIPTION

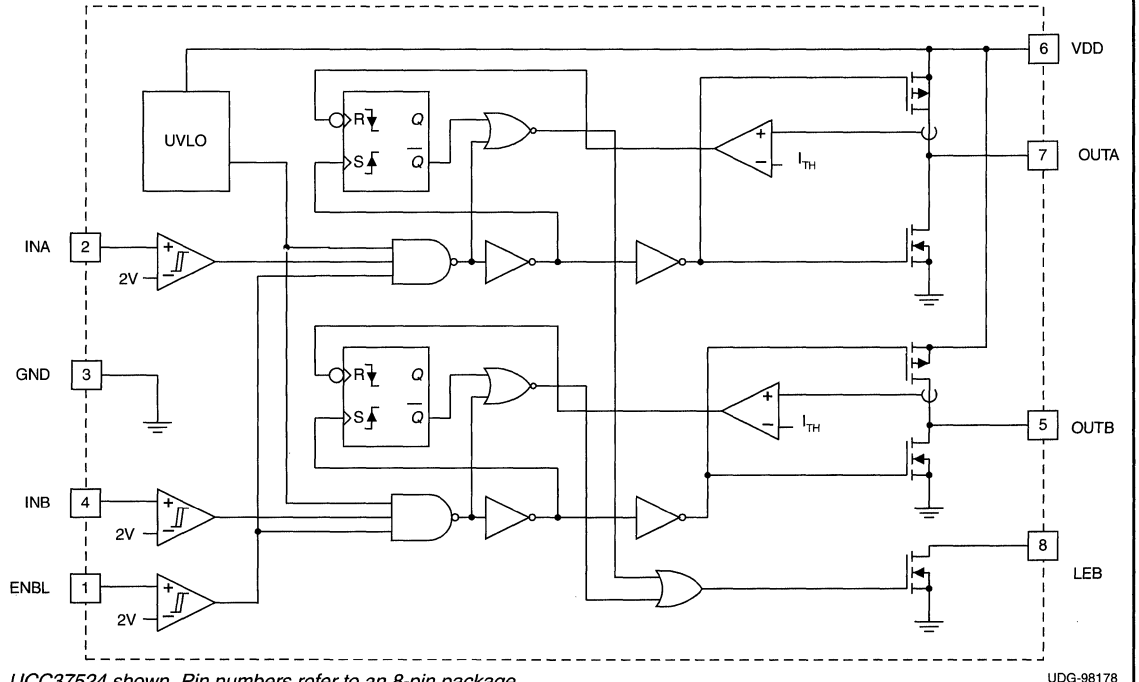
The UCC37523/37524/37525 devices are high speed, dual MOSFET drivers using the BiCMOS/DMOS process. All three devices are designed to be pin and performance compatible with industry standard '423, '424, '425, '426A, '427A, and '428A drivers. Each of the dual outputs is capable of providing 3A peak current and 6A in parallel. In addition, the devices feature Undervoltage Lockout (UVLO) protection, an improved input noise immunity and an enable/shutdown input. The ENBL function is implemented on one of the unused pins from the industry standard pinout. An adaptive leading edge blanking (LEB) signal is provided on the other unused pin.

The UCC37523 is a dual inverting driver. The UCC37524 is a dual non-inverting driver. The UCC37525 contains one inverting and one non-inverting driver.

In addition to driving two power MOSFETs in high power and high frequency switch mode power supply and motion control applications, these drivers are also capable of driving capacitive and inductive loads in applications such as small motor, relay, solenoid and actuator drivers. Unlike Bipolar Gate Driver ICs, these BCDMOS drivers do not require external Schottky clamp diodes for slight negative voltage overshoot protection.

UCC37523/37524/37525 family of drivers are available in 8 pin SOIC (D), PDIP (N) or CDIP (J), or 16 pin SOIC-Power (DP) packages.

BLOCK DIAGRAM



UCC37524 shown. Pin numbers refer to an 8-pin package.

UDG-98178

ABSOLUTE MAXIMUM RATINGS

Supply voltage 20V
Output Current (OUTA, OUTB) DC 0.2A
Output Current (OUTA, OUTB) DC . . . . . Pulsed (0.5 µsec) 5A
Input voltage (pins INA, INB, ENBL) . . . . . –5V to VDD+0.3V
Operating Junction Temperature . . . . . –55 °C to +150°C
Storage Temperature Range . . . . . –65 °C to +150°C
Lead Temperature (soldering 10 sec) . . . . . +300°C

Unless otherwise indicated, voltages are referenced to GND pin and currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of the packages.

ORDERING INFORMATION

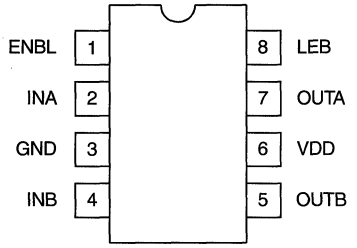
UCC☐752☐☐
- PACKAGE SUFFIX
- OUTPUT CONFIGURATION
- TEMPERATURE RANGE

	Temperature Range	Package Suffix
UCC1752X	–55°C to +125°C	J
UCC2752X	–40°C to +85°C	D, DP, N
UCC3752X	0°C to +70°C	D, DP, N

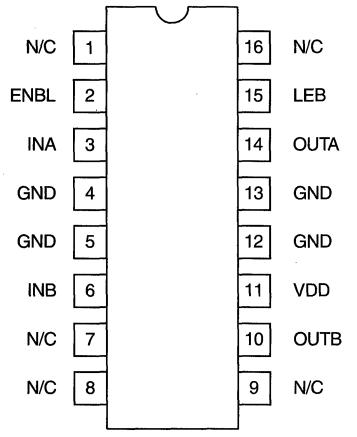
	Output Configuration
UCCX7523	Dual Inverting
UCCX7524	Dual Non-Inverting
UCCX7525	One Inverting, One Non-Inverting

CONNECTION DIAGRAMS

DIP-8, SOIC-8 (TOP VIEW)
N or J, D Packages



DIL-16 (TOP VIEW)
DP Package



POWER DISSIPATION RATING TABLE

PACKAGE	SUFFIX	T_A < 25 DEG C Power Rating (mW) *	Derating Factor Above T_A = 25°C (mW/°C) *	T_A = 70°C Power Rating (mW) *	T_A = 85°C Power Rating (mW) *	THETA (jc)	THETA (ja)
8 pin SOIC	D**	625 – 1190	6.25 – 11.90	344 – 655	250 – 476	42°C/W	84-160°C/W
8 pin Plastic DIP	N	909	9.09	500	364	49	110
16 pin Power SOIC	DP**	1724-2778	17.24 – 27.78	948 – 1528	690 – 1111	20	36-58
8 pin Ceramic DIP	J	625	6.25	344	250	26	160

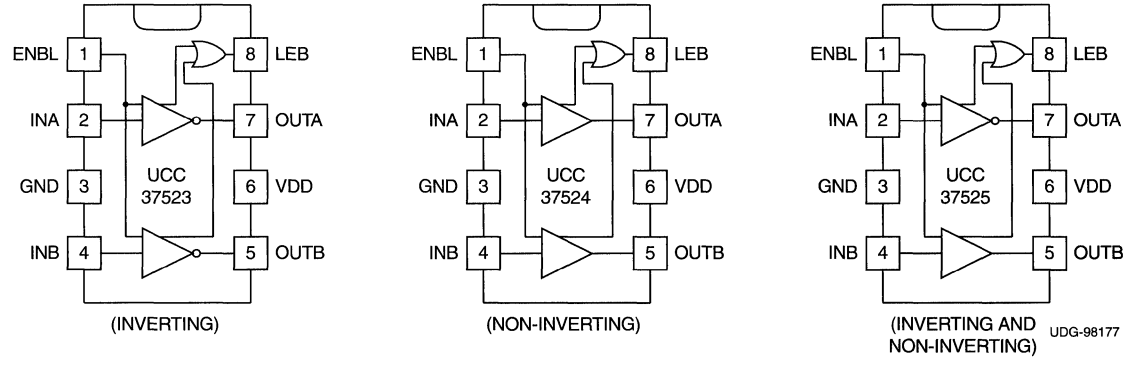
** +125°C operating junction temperature is used for power rating calculations.*

*** The range of values indicate the effect of pc-board. The lower value is for a device mounted on a 5.0 square inch, 0.062 inch think aluminum pc-board. The higher value is for a device mounted on a 5.0 square inch single sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For additional information on device temperature management, please refer to Packaging Information section in Unitrode Databook.*

INPUT/OUTPUT TABLE

Inputs (V_{IN_L}, V_{IN_H})			UCC37523		UCC37524		UCC37525	
ENBL	INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	L	H	H	L	L	H	L
L	L	H	H	H	L	L	H	L
L	H	L	H	H	L	L	H	L
L	H	H	H	H	L	L	H	L
H	L	L	H	H	L	L	H	L
H	L	H	H	L	L	H	H	H
H	H	L	L	H	H	L	L	L
H	H	H	L	L	H	H	L	H

PART VERSIONS



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Section					
V_{IN_H}, Logic 1 Input Threshold (INA, INB, ENBL)		2.4			V
V_{IN_L}, Logic 0 Input Threshold (INA, INB, ENBL)				1.6	V
Input Current (INA, INB)	0V ≤ V(IN[AB]) ≤ VDD	–1	0	1	µA
Input Current (ENBL)	V_{ENBL} = 0	–20	–10	–5	µA
	V_{ENBL} = VDD	–1	0	1	µA
Output Section					
V_{OH}, Output OUTA, OUTB High Level	$V_{OH} = V_{DD} - V_{OUT}$, I_{OUT} = –10mA		20	50	mV
V_{OL}, Output OUTA, OUTB Low Level	I_{OUT} = 10mA		20	50	mV
Output Resistance High	I_{OUT} = –10mA, VDD = 18V		1.6	3	Ω
Output Resistance Low	I_{OUT} = 10mA, VDD = 18V		1.6	3	Ω
Peak Output Current	(Note 1)		3		A
Latch-up Protection	(Note 1)	> 500			mA

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, the MIN and MAX specifications apply for 4.5V≤ VDD ≤18V, $T_J = T_A$. Unless otherwise specified, the TYP specifications apply for VDD = 12V, T_A = 25 °C, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switching Time Section					
t_R, OUTA,OUTB Rise Time	C_{LOAD} = 1800 pF (See Figure 1)		20	60	ns
t_F, OUTA,OUTB Fall Time	C_{LOAD} = 1800 pF (See Figure 1)		20	60	ns
t_{D1}, Delay (IN[AB] to OUT[AB]) Rising	C_{LOAD} = 1800 pF (See Figure 1)		50	100	ns
t_{D2}, Delay (IN[AB] to OUT[AB]) Falling	C_{LOAD} = 1800 pF (See Figure 1)		50	100	ns
Undervoltage Lockout Section					
Start Threshold		4.2	4.3	4.5	V
Start to Stop Hysteresis		0.4	0.6	0.9	V
Leading Edge Blanking Section					
Output LEB Low Level	I(LEB) = 1.25mA		0.1	0.2	V
Power Supply Section					
Operating Current	Static, Inputs = 0V		3.5	5	mA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

ENBL: Enable input with logic compatible threshold and hysteresis. Both driver outputs can be enabled/disabled with this input. The ENBL function is active high. That is, when ENBL is low, the IC will be disabled. When ENBL is high, the IC is enabled. The ENBL pin has an active pull- up such that the default state for the pin is to enable the IC. The output states when the IC is disabled will be the same as if the inputs was low during normal operation. For example, outputs of UCC37523 (inverting) will be held high, outputs of UCC37524 (non-inverting) will be held low and outputs of UCC37525 (inverting + non-inverting) will be held high and low respectively for OUTA and OUTB. Under this mode, the inverting outputs on UCC37523 and OUTA of UCC37525 will track VDD.

GND: Common ground. This ground should be connected very closely to the source of the power MOSFET which the driver is driving.

INA: Input A. Input signal for the A driver, logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should NOT be left floating.

INB: Input B. Input signal for the B driver, logic compatible threshold and hysteresis. If not used, this input should be tied to either VDD or GND. It should NOT be left floating.

LEB: Leading Edge Blanking output. This pin should be connected to the current sense node of the power converter. During the leading edge blanking period, a pulldown device will connect the node to ground, "blanking" any leading edge noise spikes. This pin is the logical OR of the LEB sensing circuits on both drivers OUTA and OUTB.

APPLICATION INFORMATION

Supply Section

The IC operates over a wide supply range, from 4.5V to 18V.

Input Section

The input circuit contains hysteresis to maximize noise immunity. The inputs are designed such that they can swing up to 5V below GND without damage to the IC.

Output Section

The output circuit is designed to drive a MOSFET gate on and off in 20nsec typically. The output will supply a high peak output current (3A peak). The output of the driver uses complementary devices and will swing the gate fully between the two supply rails. The outputs are designed to withstand 500mA reverse current without either damage or logic upset. The outputs are actively pulled down during undervoltage lockout even in the absence of VDD power.

Inverting outputs of UCC37523 and OUTA of UCC37525 are intended to drive external P-channel MOSFETs. Non-inverting outputs of UCC37524 and OUTB of UCC37525 are intended to drive N-channel MOSFETs.

Undervoltage Lockout Section

The under voltage detection circuit prevents the outputs from turning on the external power MOSFET when VDD is below a preset value.

When the IC is in an Undervoltage mode, the output states will be the same as if the input was low during normal operation. For example, outputs of UCC37523 (inverting) will be held high, outputs of UCC37524 (non-inverting) will be held low and outputs of UCC37525 (inverting + non-inverting) will be held high and low respectively for OUTA and OUTB. Under this mode, the inverting outputs on UCC37523 and OUTA of UCC37525 will track VDD.

Leading Edge Blanking Section

The UCC37523/37524/37525 features a Patent Pending Adaptive Leading Edge Blanking circuit. An open drain FET output at the LEB pin is used to shunt the current sense signal of the PWM to ground, thus providing leading edge blanking. When the driver is turned on, an internal NMOS switch is turned on whose drain is brought out to the LEB pin. This should be connected to the current sense input of the current mode control IC. After the power MOS gate is charged, the LEB is removed by turning off this NMOS device.

Adaptive Leading Edge Blanking Principle

During a power MOSFET turn-on process, the leading edge current sense signal from the output will have an undesirable noise spike falsely triggering the overcurrent protection circuit due to the internal gate impedance. The traditional implementation of Leading Edge Blanking (LEB) in a power control application is to blank the output signal for a fixed amount of time either by an external component or provided by the PWM controller. However, the interval width of the unwanted leading edge noise changes with gate resistance, load current, temperature, diode speed and MOSFET size and technology that is being used. With UCC37523/4/5 family of drivers, the leading edge blanking pulse width is varied as needed with the changing conditions.

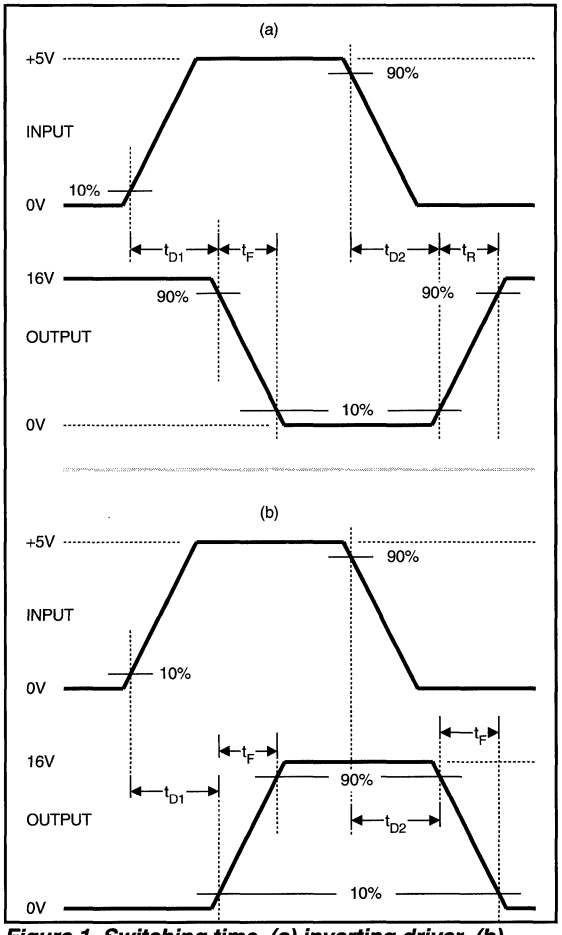


Figure 1. Switching time (a) inverting driver (b) non-inverting driver.

APPLICATION INFORMATION (cont.)

Adaptive blanking in these drivers is accomplished by monitoring both the input signal and charge current from the driver IC to MOSFET gate. The leading edge current spike only occurs while the power MOSFET is being switched ON or OFF. This is also the time when gate charge current is also flowing. As shown in Fig. 2., the LEB signal is initiated on a rising edge of the input signal (V_{IN}). The LEB control circuit monitors the gate charge current and releases the blanking signal when the gate current falls below the predefined threshold level. (I_{TH})

The advantages of this adaptive approach are many. This method does not depend on inaccurate timing circuits, eliminates the need of filter capacitor on the current sense inputs of PWM controllers (the series resistor is still needed), provides a minimum blanking interval to support higher frequency designs, allows for effective short circuit protection, and is fully adaptive to varying component and operating conditions.

Fig.3. shows two operating waveforms using the UCC37523/4/5 family of drivers with different MOSFET component selection. V_{RSENSE} is the unfiltered current sense signal and VCS+ is current sense signal with LEB. As can be seen, the LEB pulse width measurements accommodates the changing operating conditions.

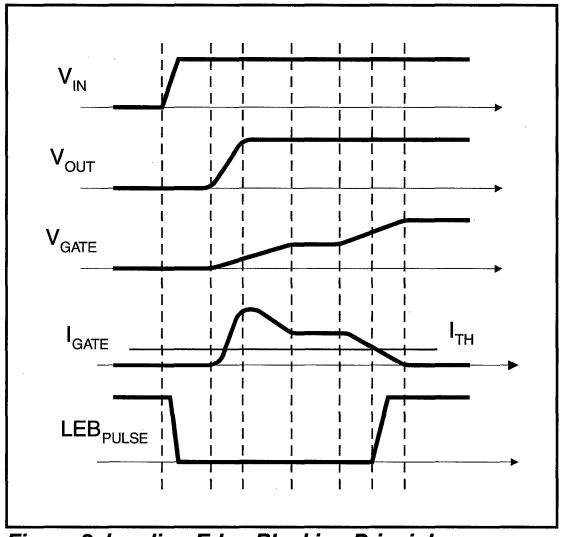


Figure 2. Leading Edge Blanking Principle

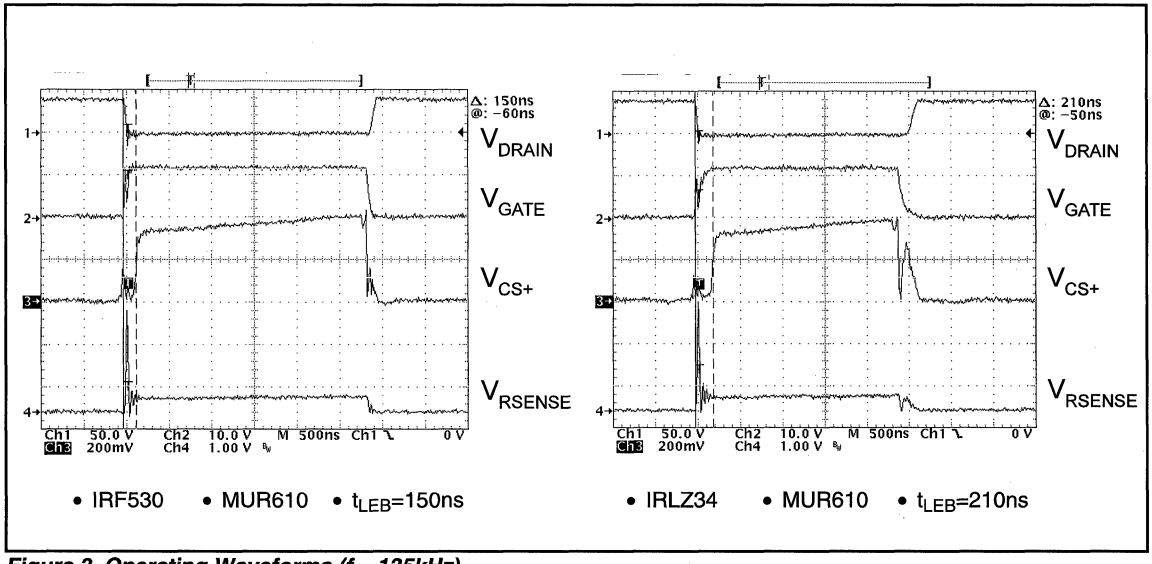


Figure 3. Operating Waveforms (f_S=135kHz)

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

UNITRODE

Quad FET Driver

UCC1776
UCC2776
UCC3776
PRELIMINARY

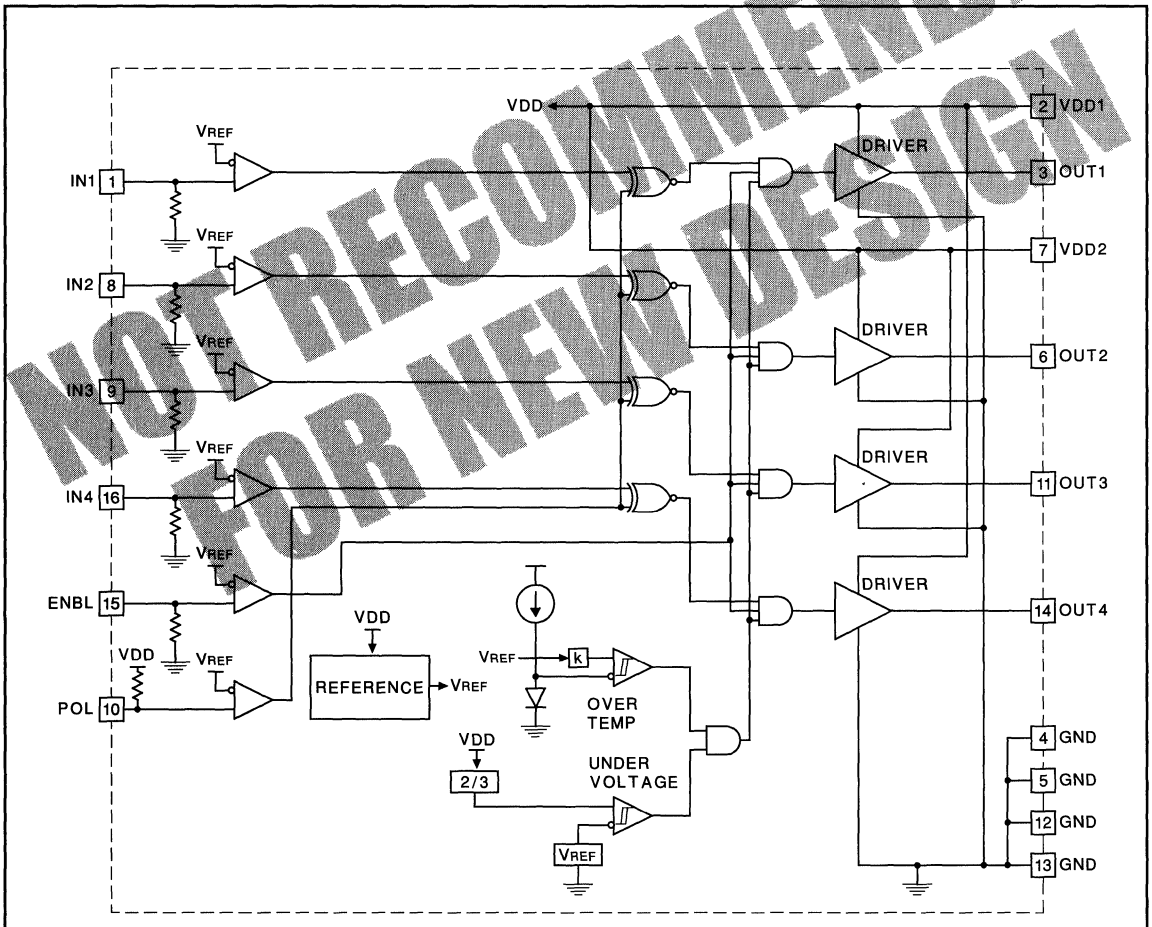
FEATURES

- High Peak Output Current Each Output – 1.5A Source, 2.0A Sink
- Wide Operating Voltage Range 4.5V to 18V
- Thermal Shutdown
- CMOS Compatible Inputs
- Outputs Are Active Low for Undervoltage Lockout Condition

DESCRIPTION

The UCC3776 is a four output BCDMOS buffer/driver designed to drive highly capacitive loads such as power MOSFET gates at high speeds. The device can be configured as either an inverting or non-inverting driver via the POL pin. The outputs are enabled by ENBL. When disabled, all outputs are active low. The device incorporates thermal shutdown with hysteresis for stability. The device also includes an undervoltage lockout circuit (UVLO) with hysteresis which disables the outputs when VDD is below a preset threshold. The outputs are held low during undervoltage lockout, even in the absence of VDD power to the device. This helps prevent MOSFET turn-on due to capacitive current through the gate-drain capacitance of the power MOSFET in the presence of high dV/dts. The logic input thresholds are compatible with standard 5V HCMOS logic.

BLOCK DIAGRAM



Note: Pin connections shown refer to 16-pin packages.

UDG-95129-2

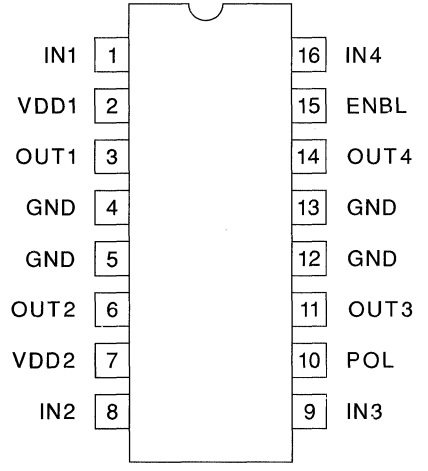
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, VDD1, VDD2 . . . . . 20V
Maximum DC Voltage Difference, VDD1 vs. VDD2 . . . . . 100mV
Logic Input, IN1, IN4, ENBL
  Maximum forced voltage . . . . . –0.3 to VDD1 + 0.3V
Logic Inputs, IN2, IN3, POL
  Maximum forced voltage . . . . . –0.3 to VDD2 + 0.3V
Latch-up Protection withstand Reverse Current
  I_{REV}, OUT1, OUT2, OUT3, OUT4 . . . . . 500mA
Power Outputs, OUT1, OUT2, OUT3, OUT4
  Maximum pulsed current (10% duty max, 10µsec max pulse width) 3A
Storage Temperature . . . . . –65°C to +150°C
Operating Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

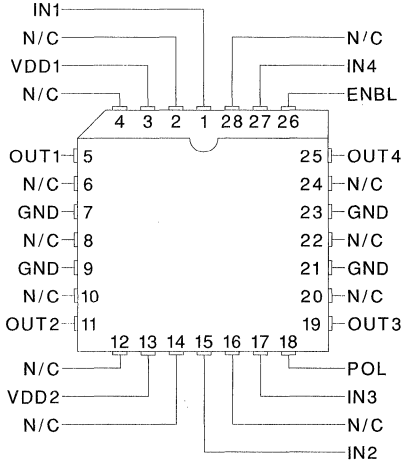
All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
N or J, DP Packages



PLCC-28 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1776; –40°C to +85°C for UCC2776; 0°C to +70°C for UCC3776; V_{POL} = 5V, V_{ENBL} = 5V, 4.5V < VDD < 18V, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Section					
VIH, Logic 1 Input Voltage		3			V
VIL, Logic 0 Input Voltage				2	V
IINn, Input Current	V_{INn} = 5V			30	µA
	V_{INn} = 0V	–1		+1	µA
ENBL Input Current	V_{ENBL} = 5V			30	µA
	V_{ENBL} = 0V	–1		+1	µA
POL Input Current	V_{POL} = 5V	–1		+1	µA
	V_{POL} = 0V	–30			µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1776; –40°C to +85°C for UCC2776; 0°C to +70°C for UCC3776; V_{POL} = 5V, V_{ENBL} = 5V, 4.5V < VDD < 18V, $T_J = T_A$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
VOH, High Output Voltage	I_{OUTn} = –10mA, VDD1 = VDD2 = 12V, V_{INn} = 5V	VDD–1.0			V
VOL, Low Output Voltage	I_{OUTn} = 10mA, VDD1 = VDD2 = 12V, V_{INn} = 0V			0.15	V
Output Resistance	I_{OUTn} = 10mA, VDD1 = VDD2 = 12V, V_{INn} = 0V		6		Ω
Output High Peak Current	VDD1 = VDD2 = 12V, OUTn = 5V, V_{INn} = 5V, T_J = 25°C (Note 1)		–1.5		A
Output Low Peak Current	VDD1 = VDD2 = 12V, OUTn = 5V, V_{INn} = 0V, T_J = 25°C (Note 1)		2.0		A
UVLO Output Pull-down Voltage	VDD1 = VDD2 = 3V, I_{OUTn} = –10mA		0.8	1.5	V
Switching Time Section					
Output Rise Time	C_{OUTn} = 1nF, V_{OUTn} = 1V to 9V, VDD1 = VDD2 = 12V		25	50	nsec
Output Fall Time	C_{OUTn} = 1nF, V_{OUTn} = 9V to 1V, VDD1 = VDD2 = 12V		10	50	nsec
IN–>OUT Delay Time (Rising Output)	V_{INn} = 2.5V, V_{OUTn} = 0.1 • VDD, VDD1 = VDD2 = 12, C_{OUTn} = 0nF		40	100	nsec
IN–>OUT Delay Time (Falling Output)	V_{INn} = 2.5V, V_{OUTn} = 0.9 • VDD, VDD1 = VDD2 = 12V, C_{OUTn} = 0nF		50	100	nsec
Power Supply Section					
Power Supply Current	V(IN1-IN4) = 0V, V_{ENBL} = 0V, VDD1 = VDD2 = 12V			2	mA
UVLO Threshold				4.5	V
UVLO Hysteresis			0.5		V

Note 1: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

ENBL: Logic level input to enable the drivers. When ENBL is low, the drivers outputs will be at GND potential, regardless of the status of POL. The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise on the input signal or input ground.

GND: Ground for the device, the supply return for the VDDs. There are four GND pads on the device.

IN1 - IN4: Inputs to each driver (1-4). The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise.

OUT1 - OUT4: Outputs to each driver (1-4). The outputs are totem pole DMOS circuits. In the absence of VDD on the device, the outputs will stay off, even with a capacitive displacement current into the output node.

POL: Polarity selection for the drivers. A logic 0 selects inverting operation. A logic 1 selects non-inverting operation. The input threshold is designed to be 5 volt CMOS compatible, independent of the VDD voltage used on the device. There is a slight hysteresis in the input circuit to help reduce sensitivity to noise.

VDD1: Supply Voltage for drivers 1 and 4. Tied internally to VDD2.

VDD2: Supply Voltage for drivers 2 and 3. Tied internally to VDD1.

APPLICATIONS INFORMATION

Figure 1 depicts a block diagram of the UCC3776 Quad FET Driver. Four high current, high speed gate drivers with CMOS compatible input stages are provided. Polarity select and enable inputs provide circuit integration flexibility, while power packaging and high speed drive circuitry allow for driving high power MOSFET gates in high speed applications.

APPLICATIONS INFORMATION (cont.)

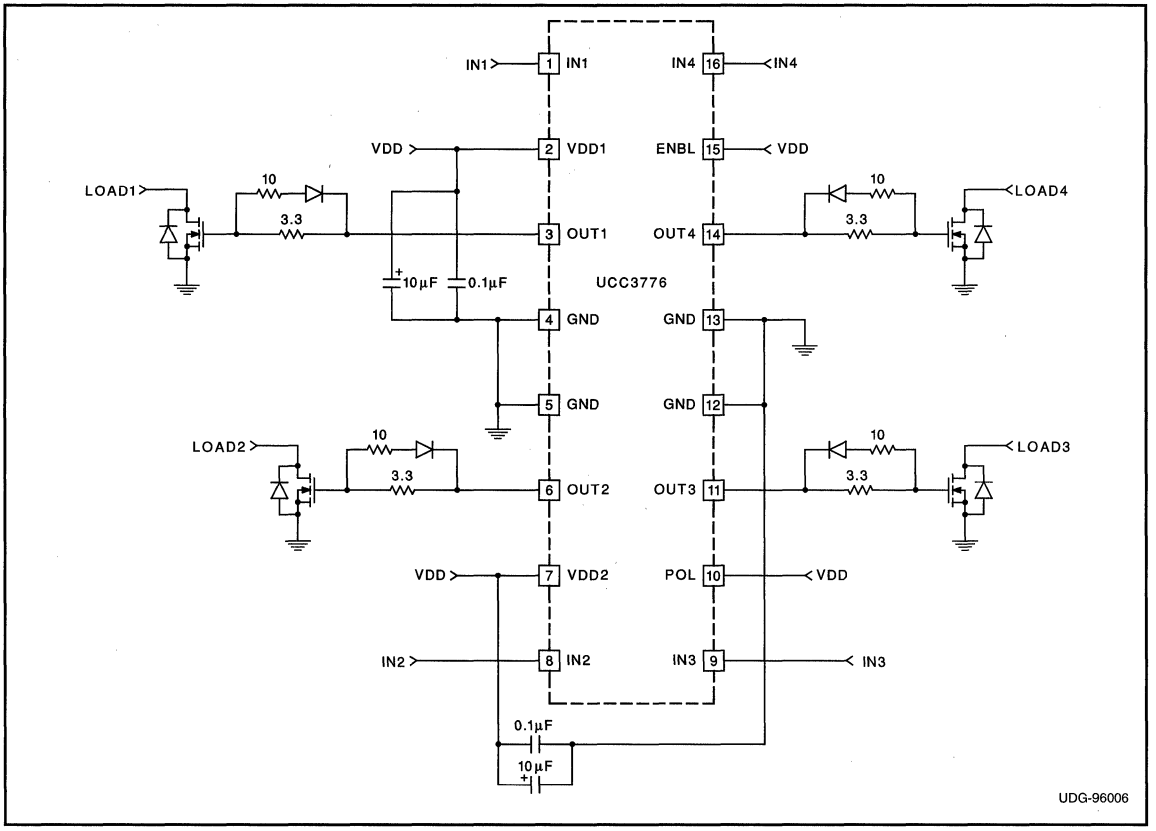


Figure 1. Typical FET Driver Application

Input Stage

Each of the four UCC3776 FET driver circuits provides an independent, CMOS compatible input stage. The allowable input voltage range extends from ground to VDD, allowing for easy interface to a wide variety of PWM and power supply support circuitry. The POL and ENBL inputs are tied to all four drivers, and all drivers must be configured as either inverting or noninverting, and all must be either enabled or not enabled.

To prevent oscillations in noisy PWM environments, any unused drivers should have their input stages tied to either VDD or ground. Unlike other CMOS FET drivers, quiescent power current is not significantly affected by the polarity of the driver input signal.

Output Stage/Gate Driver Considerations

Many power FET driver data sheets rely solely on rise and fall time specifications into a capacitive load to quan-tify speed performance. While these specifications are important, they do not provide all the required information. The UCC3776 specifies rise and fall times of 25ns and 10ns respectively into a load of 1nF. This specification can be used to calculate the average slew rate capability of the driver stage over the output voltage range.

However, the gate of a power MOSFET cannot be modeled accurately with a simple capacitor. The voltage/current requirements of the gate vary widely over several distinct phases of FET turn-on and turn-off. The most accurate way to calculate the switching times of power MOSFETs is to determine the total gate charge requirement (Qg), which is usually specified by the MOSFET manufacturer, and determine the peak current capability of the MOSFET gate driver. Ideally the driver's peak current can be delivered while the MOSFET gate is transitioning through its plateau or "Miller" level, when current demands are highest.

APPLICATIONS INFORMATION (cont.)

The UCC3776 specifies peak source and sink currents for a driver output voltage of 5V. This output voltage approximately coincides with the average gate plateau voltage of a power MOSFET. Outside of the plateau region the gate drive waveform is primarily limited by the slew rate capability of the driver. Through proper analysis of the MOSFET's gate drive requirements and the specifications for the UCC3776, an accurate model of AC performance can be created. For a detailed description of MOSFET AC gate drive requirements please see Unitrode Application Notes U-118 and U-137. Although the Unitrode power drivers referenced in these application notes are bipolar devices, the information relating to MOSFET gate drive characteristics is applicable.

Power Supply Decoupling/Grounding

The high peak currents required to charge high capacitance MOSFET gates make proper power supply decoupling and grounding essential. The UCC3776 provides two power supply inputs (VDD1 and VDD2) to allow for optimum internal circuit layout and minimum resistive voltage drop with high peak current loads. VDD1 provides the drive current for outputs 1 and 4, while VDD2 provides drive current for outputs 2 and 3. Both of these pins must be externally connected to the source power supply, and the DC potential difference between these two points should be limited to 100mV. Under no circumstances should an output driver be used with only one supply input connected.

To guarantee a low impedance current path over a wide frequency range, each supply input should be separately bypassed to ground with both a high value tantalum or electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. The exact value of the tantalum or electrolytic capacitor will depend on the charge requirements of the MOSFET gate. For most applications a value between 1μF and 10μF should suffice. Connections for ground leads should be kept as short as possible. The driver chip and support electronics should be located over a large copper ground plane if layout conditions allow it.

Power Dissipation/Thermal Considerations

Being a CMOS device, the standby power dissipation of the UCC3776 is quite low. For a 15V supply, the maximum quiescent current of 2mA results in a maximum power loss of only 30mW. However, driving high frequency MOSFETs at high peak currents results in additional power dissipation. This is because each time the MOSFET gate is charged or discharged, the energy transfer is only 50% efficient. The same amount of energy that is transferred to the gate is lost in the drive stage.

In order to determine the average output stage loss, the gate drive energy (W_{GD}) is computed as:

$$1)\ W_{GD} = 2 \bullet 0.5 \bullet C_G \bullet V^2 = \frac{Q_G}{V} \bullet V^2 = Q_G \bullet V$$

Where Q_G is the MOSFET's total gate charge, and V is the gate voltage. The factor of two results from the fact that the gate drive circuit must charge and discharge the gate every electrical cycle. Each time the gate is charged or discharged, the gate drive dissipates an amount of energy equal to the energy supplied to the gate. Power lost due to driving the gate is:

$$2)\ PL_{GD} = \frac{W_{GD}}{T} = \frac{Q \bullet V}{T} = Q_G \bullet V \bullet F$$

Where F is the operating frequency of the MOSFET. This is a worst case assumption since the power loss is shared by the output driver and the gate resistor. If a relatively large value series gate resistor is used, the power loss in the gate driver is reduced. The penalty for this is slower switching speed, and therefore more loss in the MOSFET. For high power MOSFETs this power loss can be significant.

To illustrate a typical example of driver loss, consider a MOSFET with 70nC of gate charge and a 15V gate voltage. The power loss at 200kHz is:

$$3)\ PL_{GD} = 70nC \bullet 15V \bullet 200kHz = 210mW$$

This analysis applies to one of the four drivers on the UCC3776. Four drivers operating under the same conditions results in a total power loss of 840mW. At higher frequencies the dissipation will be proportionally greater. This example demonstrates the need for power packaging which is available on the UCC3776, and not available on many other FET drivers.

After device power dissipation has been estimated, proper heat sinking must be provided to ensure that the device junction temperature does not exceed the specified maximum. Refer to the packaging section of the databook for package thermal impedance information.

Application Circuits

Figure 1 depicts a typical gate drive application circuit. Four independent, noninverting low side FET drivers are shown. Although series gate drive resistors are not required because all FET drivers have a finite peak current capability, it is good practice to include some series resistance to limit peak current and to prevent oscillations due to parasitic inductance and capacitance. The parallel diode and resistor allow for a faster gate turn off than turn on. This characteristic is often desirable for bridge driver applications to prevent MOSFET cross conduction in the power stage.

APPLICATIONS INFORMATION (cont.)

Figure 2 shows an applications circuit with paralleled output drivers. If it is required to drive high gate charge MOSFETs, the UCC3776 output drivers can be combined for higher peak current capability. It is good practice to provide separate gate resistor networks to each individual MOSFET as shown. This will ensure that each driver circuit will not see excessive current during the high gate charge portion of the switching waveform. This practice also tends to isolate driver circuits to reduce the possibility of ringing and crosstalk. If all four drivers are used to drive a single MOSFET, then four separate gate drive resistor networks should be used.

Figure 3 shows a transformer coupled full bridge power stage. The UCC3776 is ideally suited for interfacing between low power PWM outputs and high power output stages. Although the UC3879 phase shift controller is shown in this example, the UCC3776 can be used in many PWM controller applications where high power FET drivers are required.

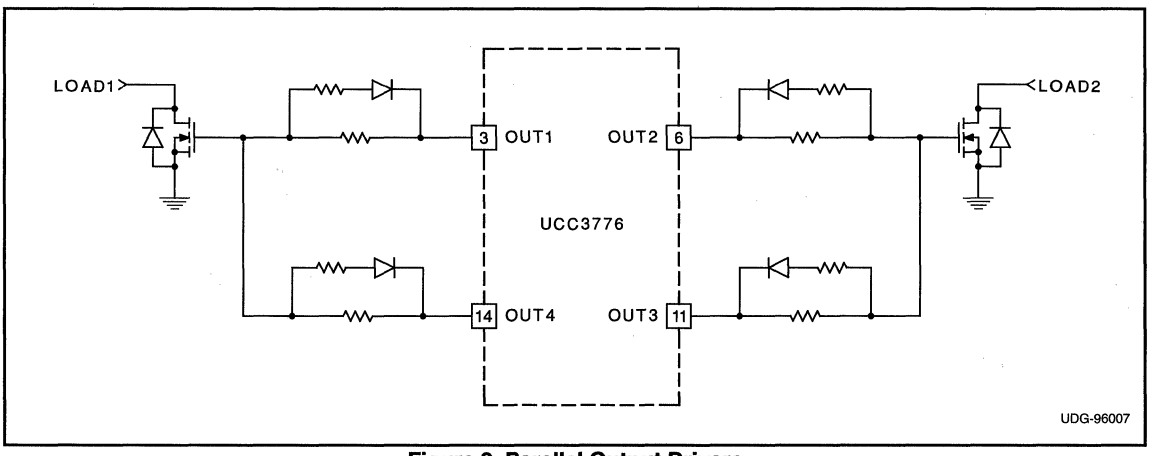


Figure 2. Parallel Output Drivers

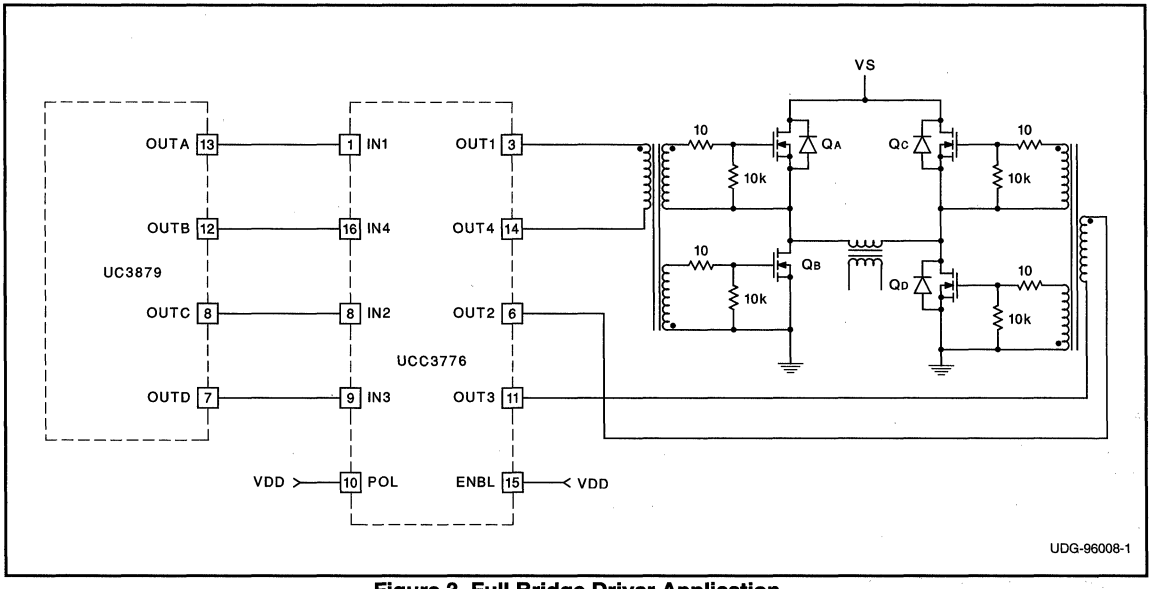


Figure 3. Full Bridge Driver Application

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IGBT DRIVE USING MOSFET GATE DRIVERS

John A. O'Connor

IGBT Drive Requirements

Insulated gate bipolar transistors (IGBTs) are gaining considerable use in circuits requiring high voltage and current at moderate switching frequencies. Typically these circuits are in motor control, uninterruptible power supply and other similar inverter applications. Much of the IGBTs popularity stems from its simple MOSFET-like gate drive requirement. In comparison to bipolar transistors which were formally used in such designs, the IGBT offers a considerable reduction in both size and complexity of the drive circuitry. Recent improvements in IGBT switching speed has yielded devices suitable for power supply applications, thus IGBTs will compete with MOSFETs for certain high voltage applications as well. Many designers have therefore turned to MOSFET drivers for their IGBT drive requirements.

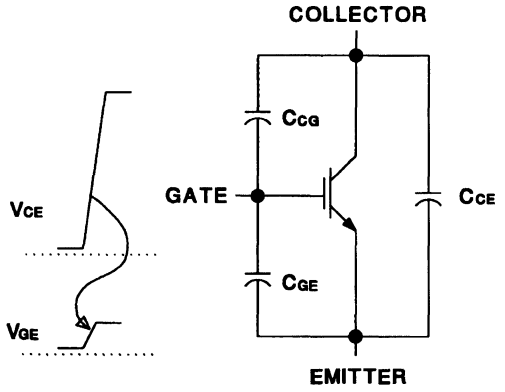

Figure 1. High dv/dt at the collector couples to the gate through parasitic capacitance.

IGBT drive requirements can be divided into two basic application categories: Those that do not apply high dv/dt to the collector/emitter of the IGBT when it is off, and those that do. Examples of the former are buck regulators and forward converters, where only one switch is employed or multiple switches are activated synchronously. High dv/dt is applied during the off-state in most bridge circuits such as inverters and motor controllers, when opposing devices are turned on. Simultaneous conduction of opposing devices can occur in such circuits, often with catastrophic results if proper gate drive and layout precautions are not followed. This behavior is caused by parasitic collector to gate (miller) capacitance, effectively forming a capacitive divider with the gate to emitter capacitance and thus inducing a gate to emitter voltage as illustrated in figure 1.

When high off-state dv/dt is not present, the IGBT can be driven like a MOSFET using any of the gate drive circuits in the UC37XX family as well as from the drivers internal to many switching power supply controllers. Normally 15 volts is applied gate to emitter during the on-state to minimize saturation voltage. The gate resistor or gate drive current directly controls IGBT turn-on, however turn-off is partially governed by minority carrier behavior and is less effected by gate drive.

There are several techniques which can be employed to eliminate simultaneous conduction when high off-state dv/dt is present. The most important technique, which should always be employed, is a Kelvin connection between the IGBT emitter and the driver's ground. High di/dt present in the emitter circuit can cause substantial transient voltages to develop in the gate drive circuit if it is not properly referenced. The Kelvin drive connection also minimizes the effective driver impedance for maximum attenuation of the dv/dt induced gate voltage. This requirement adds complication to driving multiple ground referenced IGBTs due to finite ground circuit impedance. Substantial voltages may develop across the ground impedance during switching, requiring level shift or isolation circuitry at the command signal to allow Kelvin drive circuit connections.

Bipolar Gate Driver

A Kelvin connected unipolar driver may often be adequate at lower switching speeds, however negative gate bias must be applied during the off-state to utilize the IGBT at higher rates. This becomes apparent when one considers that the gate to emitter threshold voltage drops to approximately 1.4 volts at high temperature. With high dv/dt at the collector, a very low and impractical drive

impedance is required to assure that the device remains off. By utilizing a negative turn-off bias, an adequate voltage margin is easily achieved, allowing the use of a more practical gate drive impedance. Fortunately most gate drivers have sufficient voltage capability to be used with bipolar

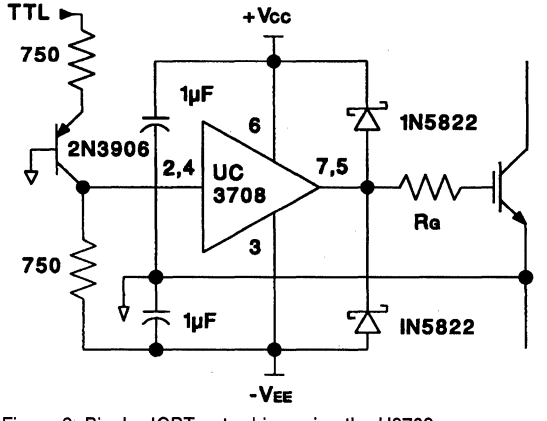

Figure 2. Bipolar IGBT gate drive using the U3708

power supplies. The UC3708 shown in figure 2 can deliver up to 6 amps peak with both output's paralleled, and is particularly suited to driving IGBTs. For added reliability during power sequencing, its output's "self bias", actively sinking current when insufficient supply voltage is present. The positive supply,+Vcc, is normally 15 to 16 volts and the negative supply, -VEE, typically ranges between -5 and -15 volts depending on circuit conditions. A PNP level shift circuit references the drive signal to ground. Opto-couplers are also commonly employed, and may be interfaced directly to the gate driver by referencing the signal to the negative supply. Note that this is a very demanding application for optocouplers, and only devices rated for high CMRR should be used.

Isolated Gate Driver

A bipolar IGBT gate driver with over-current protection can be implemented using the UC3724/UC3725 isolated gate driver pair as shown in figure 3. The UC3724/UC3725 transmits both power and signal across a small pulse transformer, thereby achieving low cost, high voltage isolation. An additional transformer winding develops a negative voltage, providing a bipolar supply for the UC3708. The UC3724/UC3725 can also be used for circuits which do not require negative turn-off bias by simply eliminating the negative supply and external driver, and using the UC3725 to drive the IGBT gate directly. Application note U-127 covers the UC3724/UC3725 in depth.

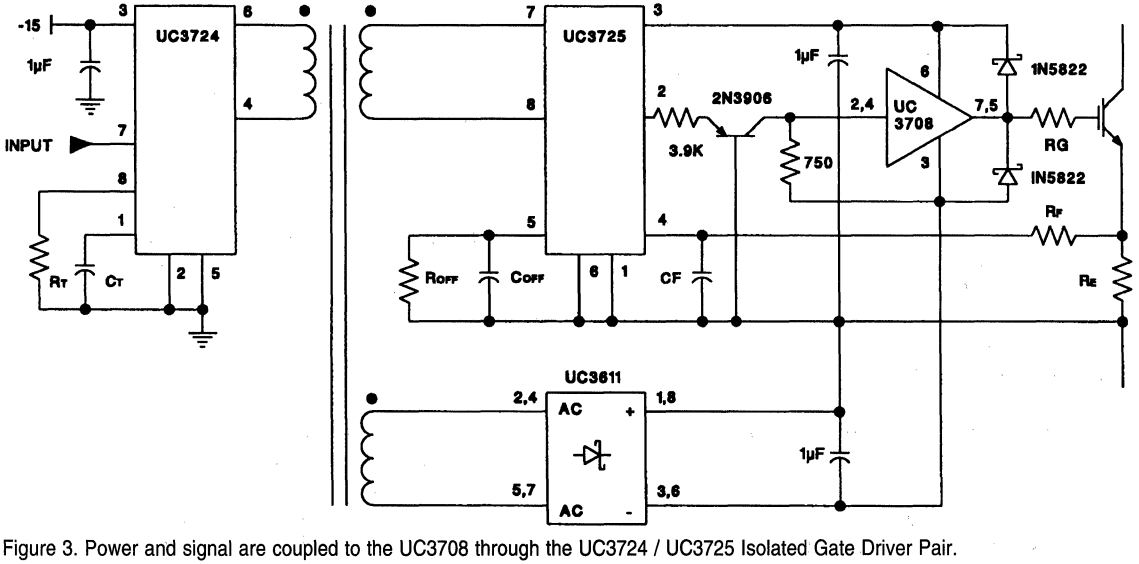

Figure 3. Power and signal are coupled to the UC3708 through the UC3724 / UC3725 Isolated Gate Driver Pair.

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Power Dissipation Considerations for the UC3726N/UC3727N IGBT Driver Pair

by Mickey McClure
Application Engineer
Motion Control Products

Optimized for driving Insulated Gate Bipolar Transistors (IGBTs), the UC3726N/UC3727N IGBT driver pair is a very versatile and cost effective solution for applications where voltage isolation is required. However, care must be taken to insure that the junction temperatures of both the UC3726N and UC3727N are kept below levels which assure reliable operation. The purpose of this design note is to outline the proper thermal design procedure for using this chip set.

BACKGROUND

In order to assure reliable operation, the junction temperatures of both ICs should be kept below 125°C. Although the absolute maximum rating is 150°C, the failure rates for silicon integrated circuits increase significantly at temperatures above 125°C. Also note that the electrical specifications of commercial grade ICs are no longer guaranteed at junction temperatures above 70°C. This does not mean that the device will not function, it simply means that some electrical parameters may fall out of their specified range. Since power devices typically operate with junction temperatures as high as 125°C, it is assumed for purposes of this analysis that operation at these temperatures is acceptable for the application. As always with power drivers, design verification in the lab is recommended. What follows is a thermal analysis of the example circuit designed in Unitrode Application Note U-143A, "New Chip Pair Provides Isolated Drive For High Voltage IGBTs."

POWER DISSIPATION IN THE UC3726N

Power losses in the UC3726N consists of output stage conduction and switching losses, as well as bias losses for the chip itself. Output stage conduction losses result from supplying the UC3727N bias current, the IGBT gate drive current,and the transformer magnetizing current. Each loss component can be calculated individually, and the results added to obtain the total power dissipation.

Since power is only transferred across the pulse transformer during the "full" voltage time period, all of the current required to power the UC3727N and the IGBT gate must be supplied during this 1/3 portion of the duty cycle. To calculate the loss associated with this power transfer, the rms value of the average current required to power the UC3727N and the IGBT gate must be calculated. For the example circuit described in U-143A, the average IGBT gate current is equal to:

$$1)\ I_G = 2 \bullet Q_G \bullet F = 2 \bullet 110nC \bullet 15kHz = 3.3mA$$

The typical bias current for the UC3727N is 24mA, resulting in a total average supply current of 27.3mA. Since the average current must be delivered in 1/3 of the duty cycle, the peak current is determined by:

$$2)\ I_{SUPPLY} = \frac{27.3mA}{0.33} = 82.7mA$$

To determine the loss resulting from this current (PL_{SUPPLY}), the rms value of the current is multiplied by the rms value of the total voltage drop of the upper and lower drive stages of the UC3726N:

$$3)\ PL_{SUPPLY} = (2.3V \bullet \sqrt{0.33})(82.7mA \bullet \sqrt{0.33}) = 63mW$$

To determine the loss resulting from the transformer magnetizing current, the rms value is determined for both the "full" time ($I_{MAGFULL}$) and "half" time ($I_{MAGHALF}$) currents. With a peak magnetizing current level of 35mA, the corresponding rms currents are calculated as:

$$4)\ I_{MAGFULL} = 35mA \bullet \sqrt{\frac{0.33}{3}} = 11mA$$

$$5)\ I_{MAGHALF} = 35mA \bullet \sqrt{\frac{0.66}{3}} = 16mA$$

The losses resulting from these currents are a function of the rms value of the appropriate voltage drops in the UC3726N. For the "full" time the voltage drop is the total saturation drop of the output drivers. For the "half" time the voltage drop is the sum of the drop across the half on driver (V_{CC} - 0.6 • V_{CC}) and the drop across the full on driver (0.4V):

6) $PL_{MAGFULL} = 11mA \bullet 2.3V \bullet \sqrt{0.33} = 14mW$

7) $PL_{MAGHALF} = 16mA \bullet 12.4V \bullet \sqrt{0.66} = 161mW$

The power dissipated due to switching loss is difficult to calculate, and some simplifying assumptions must be made. Since the transition from half to full voltage occurs when the transformer current reaches zero, it is assumed that the switching loss is very close to zero for this transition. For the transition from full to half voltage it is assumed that the transformer current remains constant as the sum of the peak magnetizing current and the peak supply current throughout the whole transition. This is a reasonable worst case assumption since the load is highly inductive. Furthermore, the fall time for the full to half driver is much slower than the rise time for the zero to full driver, and therefore the full to half driver is the primary contributor to switching loss.

Referring to Figure 3 of U-143C, the half driver fall time is 200ns, yielding a duty cycle of 0.08 for this calculation. Since the voltage transitions from 28 to 18V, the switching loss component is calculated as:

8) $$PL_{SWITCH} = (35mA + 82.7mA) \bullet \sqrt{0.08} \bullet \left(2 \bullet \sqrt{0.08} + 10 \bullet \sqrt{\frac{0.08}{3}}\right) = 72mW$$

The 2V term comes from the saturation drop of the output driver, and the 10V term comes from the 10V swing from 28V to 18V. In order to take into account other miscellaneous switching losses, the PL_{SWITCH} term is rounded up to 100mW.

The final dissipation calculation is the bias loss for the UC3726N itself. Using a single +30V supply, the typical bias current for the UC3726N is 26mA. This takes into account an additional 0.4mA/V I_{CC} component for each volt above the 20V supply level specified in the data sheet. The resulting power loss is:

9) $PL_{BIAS} = 30V \bullet 26mA = 780mW$

If an external +5V logic supply is available, it is highly recommended to power the logic supply (V_L) from this source. The bias loss in this case becomes a function of the reduced V_{CC} bias current and the bias current requirement for the external logic supply:

10) $PL_{BIAS} = 30V \bullet 16mA + 5V \bullet 13mA = 545mW$

The total power dissipation for the IC is calculated by adding the individual power loss components. If an external logic supply is not used, the total power dissipation is calculated as:

11) $PL_{TOT} = 0.063W + 0.014W + 0.161W + 0.100W + 0.780W = 1.12W$

With an external logic supply, the total power dissipation is 0.88W.

For a 16 pin plastic "batwing" package (N package) the worst case θ_{JA} is 50°C/W for typical PC board mount, resulting in a temperature rise of 56°C with no external logic supply. Using a max junction temperature of 125°C, the maximum ambient temperature for the IC in this application is 69°C. With an external 5V power supply, the worst case temperature rise is 44°C. If higher ambient temperatures are required, or if keeping the junction temperature below 70°C is required, heat sinking will be necessary.

POWER DISSIPATION IN THE UC3727N

The power dissipation calculations for the UC3727N are much more straight forward. The losses consist only of the bias loss for the IC, and the output stage conduction and switching losses. In order to determine the average output stage loss, the gate drive energy (W_{GD}) is determined by:

12) $$W_{GD} = 2 \bullet \tfrac{1}{2} \bullet C_G \bullet V^2 = \left(\frac{Q_G}{V}\right) \bullet V^2 = Q_G \bullet V$$

The factor of 2 results from the fact that the gate drive circuit must charge and discharge the gate every electrical cycle. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. This leads to the power lost due to the gate drive:

13) $$PL_{GD} = \frac{W_{GD}}{T} = \frac{Q_G \bullet V}{T} = Q_G \bullet V \bullet F = 110nC \bullet 20.5V \bullet 15kHz = 34mW$$

This is a worst case assumption since the power loss will actually be shared by the output driver and the gate resistor. In most cases there will be significant

sharing of this loss with the gate driver resistor since the output impedance of the driver stage is low. Because this calculation takes into account the total energy transferred to the gate, both switching loss and conduction loss are included.

To determine the power loss due to bias current, the total voltage drop of the UC3726N is subtracted from V_{CC}, and this result is multiplied by the bias current:

14) $PL_{BIAS} = (30V - 2.3)(24mA) = 664mW$

The resulting total power loss is calculated as:

15) $PL_{TOT} = 0.034W + 0.664W = 0.698W$

For a 20 pin plastic package (N package) the worst case θ_{JA} is 79°C/W for typical PC board mount, resulting in a temperature rise of 55°C. This leads to a maximum ambient temperature of 70°C for this application. Again, if it is desired to operate in a higher ambient, or to keep the junction temperature lower, heat sinking will be necessary.

TEST RESULTS

The UC3726/UC3727 IGBT Driver Pair Evaluation Board (See U-143C) was used to test the thermal characteristics of the driver pair. The evaluation board represents a typical PC board layout, where no heat sinking is provided except for a small copper ground plane. All electrical parameters for the circuit were programmed as described in U-143C. With a V_{CC} of 30V, and no external logic supply, driving the IGBT at 15kHz resulted in a lead temperature of 70°C for the UC3726N, and a case temperature of 47°C for the UC3727N. Assuming a θ_{JL} of 12°C/W for the UC3726N results in a junction temperature rise of 58°C, very close to the predicted rise.

Assuming a θ_{JC} of 35°C/W for the UC3727N results in a junction temperature rise of 46°C, which is significantly lower than the predicted value, indicating that the IC is dissipating less power than predicted. While this is a positive development in this case, it further points out the need to bread board circuits to prove out theoretical calculations.

Using an external +5V logic supply resulted in a lead temperature of 57°C for the UC3726N, and as expected had no effect on the case temperature of the UC3727N. The corresponding temperature rise of the UC3726N junction is 42°C. This difference in temperature rise of 16°C can be highly significant depending on the application.

As stated previously, properly heat sinking the ICs will result in much lower junction temperatures. While this technique leads to additional cost and complexity, it can lead to much greater design flexibility, particularly for driving IGBTs with very high levels of gate charge. Also, since the UC3726N features a "batwing" style package, heat is very effectively conducted to the center leads. Increasing the ground plane connected to these leads beyond what is shown on Figure 17 of U-143C will further reduce the junction temperature.

If other IC packages are used than those described in this design note, the power loss and maximum junction temperature calculations are the same. Refer to Packaging Section of the Unitrode Product and Applications Handbook for thermal impedance data.

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Design Note

UC3726 / UC3727 IGBT Isolated Driver Pair Evaluation Kit Testing Procedure

by : Bill Andreycak

The UC3726/UC3727 IGBT isolated driver pair evaluation kit is available for design engineers to verify the performance and functionality of this unique solution for isolated gate drive applications. Also relevant are datasheets for each IC and Unitrode Application Note U-143A describing each device's features, operation, programming and operational waveforms. A copy of Design Guide DG-200A containing Design Note DN-57 which addresses power dissipation issues, and a simplified test procedure for the evaluation kit is also beneficial. Users should take the time to familiarize themselves with the numerous performance features and fault protection options available with these devices for a variety of applications. This general Testing Procedure is usable for the UC3726/UC3727 Evaluation Kit as well as for debugging any prototype circuits or first run printed circuit boards. Refer to Figure 15 of Application Note U-143A for a complete circuit schematic and Table 1 for the List of Materials.

Laboratory Equipment Needed :

Oscilloscope
Power Supply to provide +30 VDC / 100mA
Signal or pulse generator
Test Leads

Laboratory Test Procedure

** Turn off all equipment prior to making any connections and verify that there is a single electrical ground connected to "earth" ground for all equipment.

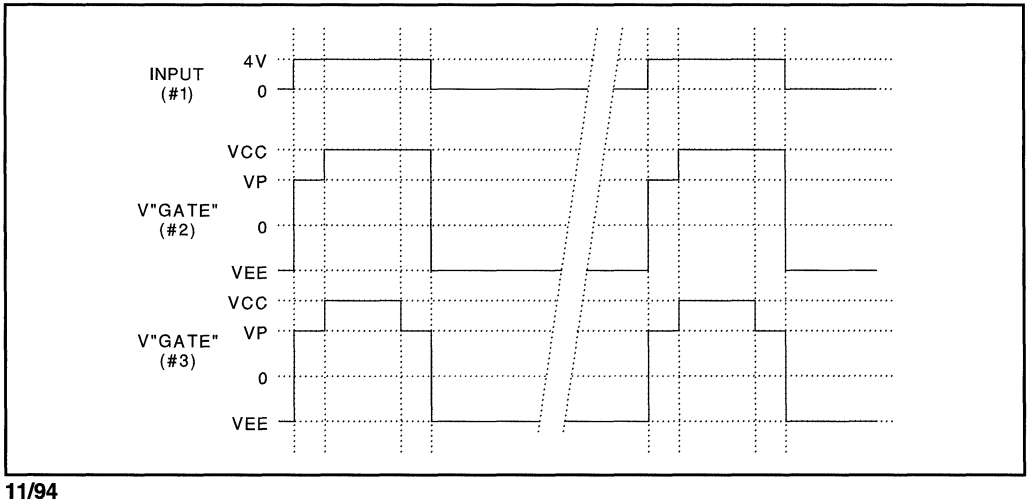
1. Configure the pulse generator to output a square wave pulse train with an amplitude of 4VDC at a frequency of 10kHz and a duty cycle of 10% (10ms on-time). See waveform #1 for reference.
2. Make the following connections to the 8 pin header connector near U1 (UC3726):

Signal	Connector Pin
+30VDC	7
Ground (return)	8
Pulse generator (+) output	4
Pulse generator (-) output (GND)	8

* Note that the header pin numbers do NOT correspond to the same IC pin numbers.

3. Make the following connections to the isolated side circuitry the opposite edge of the printed circuit board near U2 (UC3727):

WAVEFORMS



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A. Connect the "COLLECTOR" pin to the "EMITTER" pin using a jumper wire with clip leads.

B. Connect the "EMITTER" pin to the ground connection at pin 8 of the header near U1.

C. Connect the oscilloscope ground to circuit ground at the 8 pin header, pin 8.

D. Connect the oscilloscope probe to the "GATE" pin near U2.

Testing Procedure

1. Apply +30 VDC power to the evaluation kit
2. Turn ON the pulse generator
3. Verify Waveform #2 on the scope at the "GATE" pin.
4. Remove the test clip connection from the "COLLECTOR" pin
5. Verify Waveform #3 on the scope at the "GATE" pin.
6. Slowly increase the on-time (duty cycle) of the pulse generator until the "GATE" waveform latches off and remains at approximately –9VDC.
7. Reconnect the test lead to the "COLLECTOR" pin (from the "EMITTER")
8. Verify that the "GATE" waveform remains at approximately –9VDC.
9. Reduce the on-time (duty cycle) of the pulse generator back to 10µsec (10%).
10. Briefly connect header pins 6 and 2 (Vlogic to Freset)
11. Verify Waveform #2 on the scope at the "GATE" pin.

This concludes the basic testing of the UC3726/ UC3727 IGBT Evaluation Kit through verification of the gate drive waveforms. Verify isolation between the "low" and "high" side of the evaluation kit before testing in an isolated application circuit. Beware of ground loops and nonisolated power source. Whenever in doubt, use a low current (<1/4A) fuse in series with any test leads or equipment ground connections to prevent damage. The fuse will blow with any current flowing due to the attempted connections being nonisolated. Observe proper safety precautions as high voltage may be present in many IGBT applications. For complete operational details of the ICs, please refer to the datasheets and Applications literature.

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APPLICATION NOTES

NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS

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ABSTRACT

Although touted as a high impedance, voltage controlled device, prospective users of Power MOSFETs soon learn that it takes high drive currents to achieve high speed switching. This paper describes the construction techniques which lead to the parasitic effects which normally limit FETperformance, and discusses several approaches useful to improve switching speed. A series of drivers ICs, the UC3705, UC3706, UC3707 and UC3709 are featured and their performance is highlighted. This publication supercedes Unitrode Application Note U-98, originally written by R. Patel and R. Mammano of Unitrode Corporation.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFETs have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extemely fast switching. Not only is there no storage time inherent with MOSFETs, but the switching times can be user controlled to suit the application. This or course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFETs are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSFET can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell - a high power device such as the IRF 150 would have ≈ 20,000 of these cells all connected in parallel.

In operation. when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N-drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N-drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

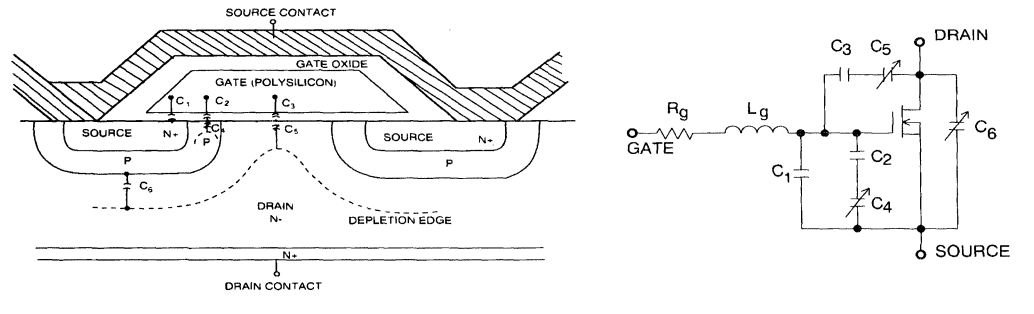


FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

In the equivalent model. the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is dielectric capacitance and is fixed while C4 is due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inducitve switching of a large class of applications and is implemented here with a IRF-510 FET, which is a 4 amp, 100V device with the following capacitances:

Ciss ~ C1 + C4 + C5 = 135 - 150 pF

Crss ~ C5 = 20 - 25 pF Vgs = 0V

Coss ~ C5 + C6 = 80-100 pF

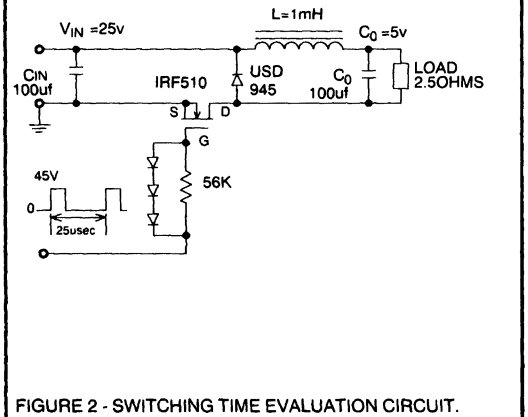


FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration the load portion of the circuit is established with Vin = 25V. Io = 2A. and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

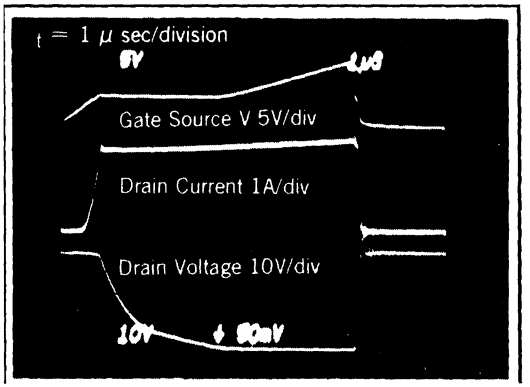


FIGURE 3-FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise time is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a significant jump when the drain-gate potential reverses polarity.

6. Unless limited circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold. C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transferred from the free-wheeling diode to the FET.

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

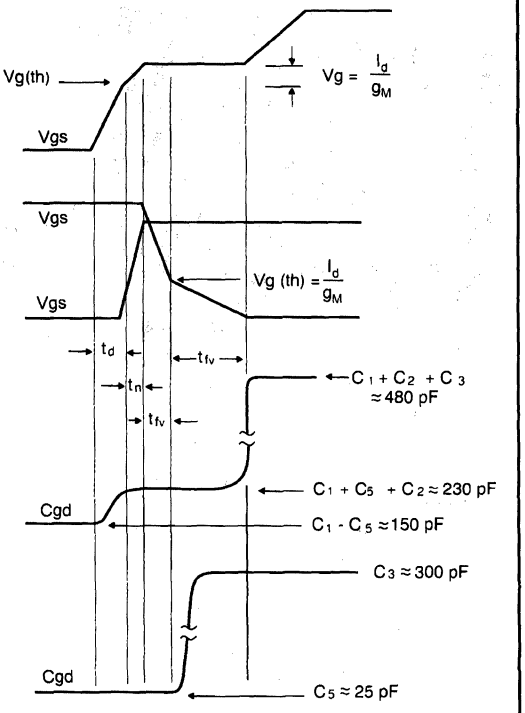


FIGURE 4 - Parasitic CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

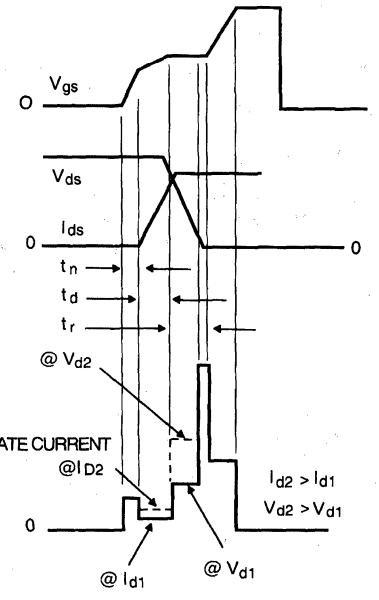


FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

AN OPTIMUM GATE DRIVE

In most switching power supply applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements

1. An initial fast pulse to get the gate voltage up to threshold.

2. A lesser amount to slow the drain current rise time. This value however, will also be a function of the required drain current.

3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.

4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approxtimated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \qquad \text{where we define } ton = td + tn + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg(th) - \frac{Id}{gM}] - Crss\,[V_{DD} - Vg(th)] - CrssV_g(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'=1.5 Ciss. With this assumption.

$$Ip \approx \frac{2}{ton}\left[Ciss\left(2.5Vg(th) + \frac{Id}{g_M}\right) + Crss\left(V_{DD} - Vg(th)\right)\right]$$

As an example, if one were to implement a 40V. 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimum drive current for this application would then take 50 nsec to ramp from zero to peak value calculated from

Ciss = 2000pF *ton = 50nsec*
Crss = 350pF V_{DD} = 40*V*
Vg(th)=3V *Id*= 10A

$$g_M = \frac{10A}{2.5V} = 4s$$

$$as\ Ip = \frac{2}{50 \times 10^{-9}}\left[2000 \times 10^{-12}\left(2.5 \times 3 + \frac{10}{4}\right) + 350 \times 10^{-12}\left(40 - 3\right)\right]$$

$\therefore$ *Ip = 1.32 amps peak*

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

TOTAL GATE CHARGE (Qg)

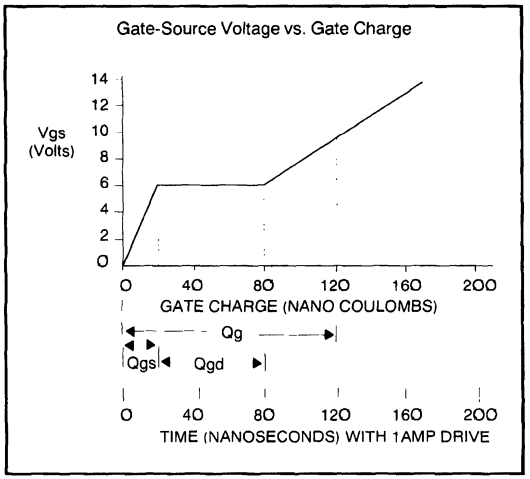
Another approach used to quantify and understand MOSFET gate drive requirements is much simpler than that of examining the instantaneous voltages, currents and capacitances. The term "Total Gate Charge", or Qg specifies the amount of gate charge required to drive the FET gate-to-source voltage (Vgs) from zero to ten volts, or vice-versa. For most high voltage devices these thresholds correspond to the FET being either completely on or off.

Charge (Q) can be expressed as the product of either current multiplied by time (I*T), or capacitance multiplied by voltage (C*V) in the units of Coulombs. Most contemporary devices have total gate charge requirements in the tens to low hundreds of nano Coulombs dependent almost entirely on die's geometry. For example, an IRF710 (size 1) FET has a total gate charge requirement of only 7.7 nC whereas the IRFP460 (size 6) demands 120 nC, and both are typical values.

PARAMETER	IRFP 440	IRFP 450	IRFP 460
Qgs (NC)	6.2	11	18
Qgd (NC)	22	43	62
Qg (NC)	42	86	120
Ciss (Nf)	1.3	2.7	4.1

There are two specified parameters contained within the total gate charge expression: Qgs, the gate-to-source charge, and Qgd the gate-to-drain, or "Miller" charge. Qgs is the amount of charge required to bring the gate voltage from zero up to its threshold VGS (th), of approximately 6 volts. Qgd defines the amount of charge that must be input to overcome the "Miller" effect as the drain voltage falls. This occurs during the plateau of the gate-to-source voltage waveform where the voltage is "constant". Excess charge is added to lower the effecive Rds (on) until the gate voltage reaches 10 volts wher Qg is specified. Further increases above this level do NOT lower Rds (on), so a 10-12 volt driver bias is ideal.

The total charge curve can be examined in sections to define the ideal driver's characteristics. Using a constant current of 1 ampere, the total charge curve (Qg=I*T) in nanoCoulombs also represents the MOSFET turn-on delay, drain current rise and drain voltage fall times in nanoseconds.



First of all, and most importantly, the average capacitive load represented by the FET to the IC driver is NOT the specified MOSFET input capacitance, Ciss. The effecive input capacitance, Ceff, is the total charge divided by the final gate voltage, Vgs(f);

Ceff = Qg(total) / Vgs(f).

Using the total gate charge curve show above, the 460 FET with Vds (off) = 400 volts has an effective input capacitance (Ceff) of approximately 120nC/10v, or 12 nF during the interval of 0 < Vgs < 10v. The specified input capacitance of Ciss = 4.1 nF applies only at Vgs=O, and is often mistaken for the driver's actual load.

The Qgs portion of the curve is primarily governed by the driver's ability to quickly turn ON. Therefore, a sharp, fast transition of the totem-pole output from low to high is essential to minimize the delays from 0 < Vgs < VGS (th). In most applications the driver IC is not peak current limited during this interval, since it is more likely to be dV/dT limited. The effective gate (load) capacitance is approximately Qgs/VGS(th). or Ciss.

Evident from the charge specifications, most of the popular size FETs used in switch-mode power supplies (sizes 4. 5 and 6) have much larger Qgd demands than their gate-to-source counterpart, Qgs. During this Qgd interval, the gate voltage remains "constant" while gate charge accumulates and the drain voltage collapses. It is also during this period that most drive circuits are simply peak current limit, whether by the driver IC or an external resistor. High peak currents are necessary for fast transitions through this interval, especially when driving large geometry FETs.

Full drain current is flowing at the beginning of the Qgd portion of the Qg curve, and notice that the drain voltage remains high. FET power loss is at its maximum here, and decreases linearly with Vds. A majority of the Qgd charge goes to combat the "Miller" effects as the drain voltage falls from that of its off condition to Vgs, or approximately Vgs(th). The remainder of the charge is used to bring the drain voltage down below that of the gate. decreasing the

effecive gate capacitance over the Qgd interval since there is relatively no change in gate voltage. The important fact, however, is that high peak currents are needed to minimize the FET power loss and transition time.

The remainder of the gate charge brings the gate voltage from VGS (th) to 10 volts. This "excess" charge reduces the FET "ON" resistance to its minimum, and raising the gate voltage above 10 volts has no further effect on reducing the Rds (on). The effective gate capacitance, which is high, can be obtained by dividing the charge input by the change in gate voltage during this region.

Ceff = [Qg - (Qgd+Qgd)] / (10v - VGS (th)) = 40nC/4v = 10nF for the IRFP460

FET DRIVER ICS

In searching for IC's capable of providing the fast transitions and high peak currents required by power MOSFETs. one of the first devices which became popular was the DS0026. While this IC was originally designed to be dual clock driver for MOS logic it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all NPN process which minimizes storage delays, and as a result, offers transition times of approximately 20 nsec. Its disadvantages, however, are high cross conduction currents, as well as requiring excessive supply current when the output is in the low (OFF) state. This leads to higher power dissipation and junction temperature than optimum.

This brings us to newer ICs designed specifically as power MOSFET drivers for switchmode power supply applications. Several factors were taken into consideration while developing the new UC3705 /06 /07 /09 series of high current drivers: the most important of which, was to isolate the high power switching noise from the low level analog signals at the PWM. Seperate supply and return paths at the driver to its signal inputs and power outputs further enhances noise immunity. Additionally, several desirable features including an analog shutdown comparator have been incorporated in the UC3706 and UC3707 devices, whereas the UC3705 and UC3709 drivers are optimized for low cost applications which incorporate this function elsewhere in the design. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross-conduction, high speed output circuitry. The corresponding block diagrams and pin assignments are shown in figures 6 thru 9, and followed by the feature selection index.

UC3705 Block Diagram

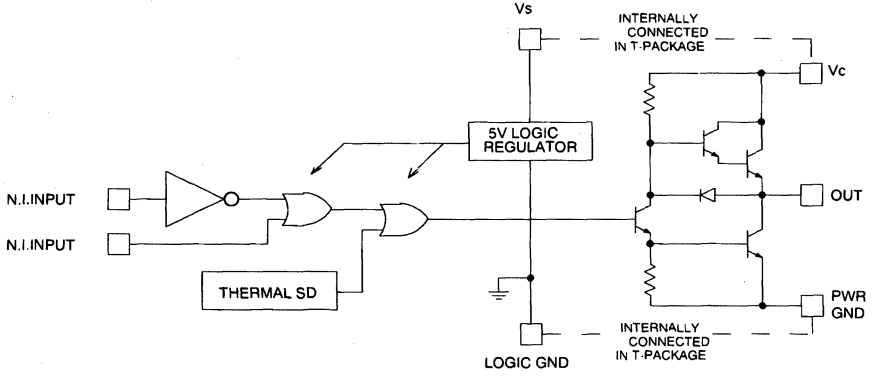


Figure 6

UC3706 Block Diagram

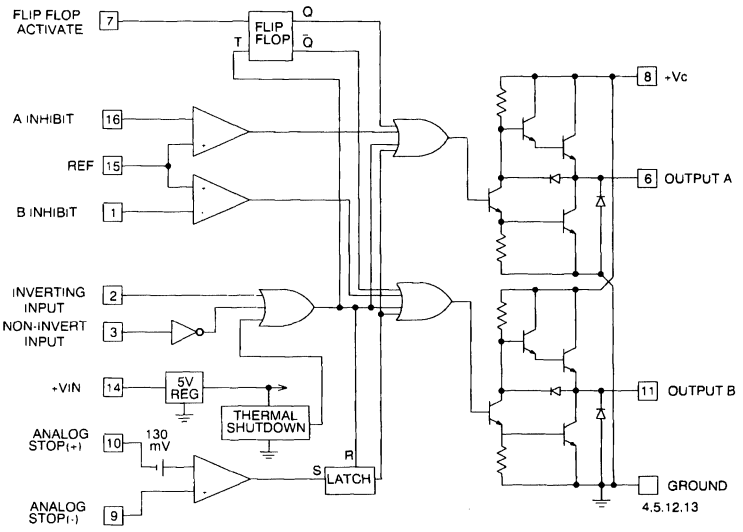


Figure 7

UC3707 Block Diagram

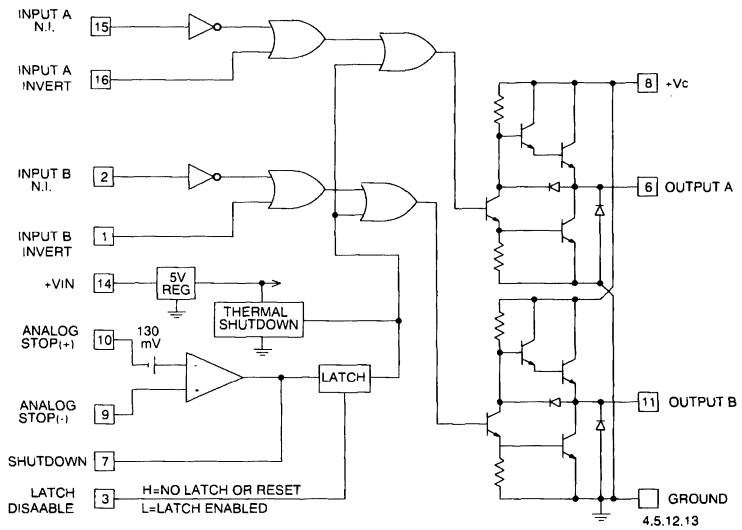
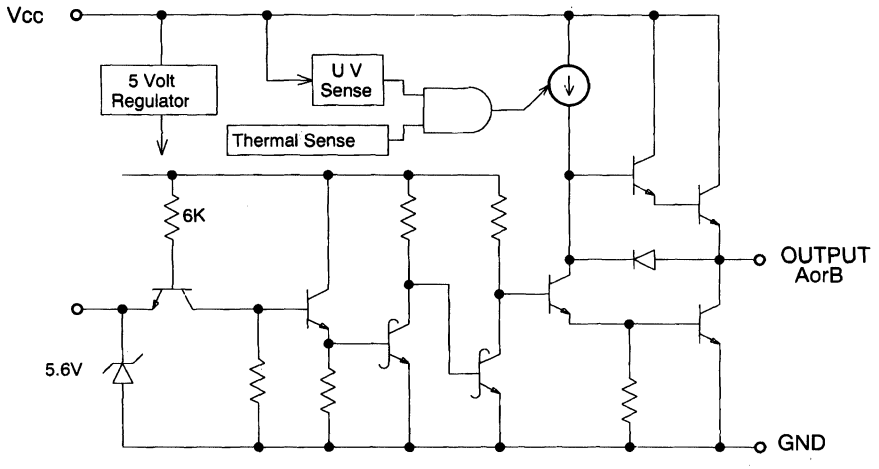


Figure 8

UC3709 Block Diagram



NOTE: One Output Shown

Figure 9

DRIVER FEATURES

1.5 Amp Peak Output Current (Per Output)

- 40 Nanosecond Rise & Fall Times into 1 NF
- Low Cross Conduction Current Spike
- 5 to 40 Volt Operation
- High Speed Power MOSFET Compatable
- Thermal Shutdown Protection

	DUAL OUTPUTS	INVERTING INPUTS	NON-INVERTING INPUTS	SEPERATE V_C & V_{in}	SEPERATE PGND & SGND	ANALOG SHUTDOWN	DIGITAL INHIBIT	TOGGLE F/F	LATCH RESET
UC3705		X	X	X	X				
UC3706	X	X	X	X	X	X	X	X	
UC3707	X	X	X	X	X	X	X		X
UC3709	X	X							

1.5 AMP PEAK TOTEM-POLE OUTPUTS

The schematic of the UC3706 output drive circuit is shown in figure 10, which is similar to the other devices in this family. While first appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in figure 11 where it can be seen that while maintaining fast transition times the cross conduction current spike has been reduced to zero when going low and only 20 nsec with a high transition. This offers negligible increase in internal circuit power dissipation at frequencies in excess of 500KHz.

Typical Output Schematic

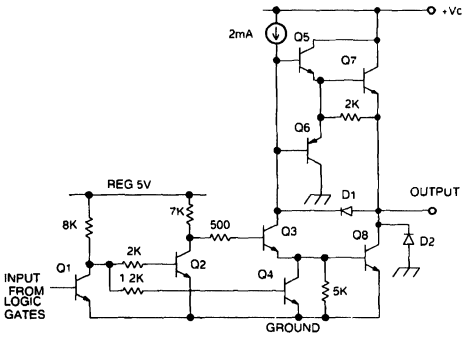


Figure 10

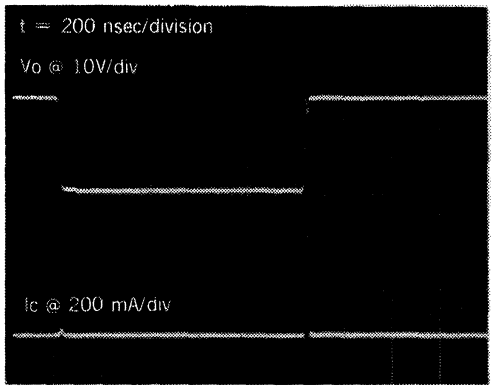


Figure 11

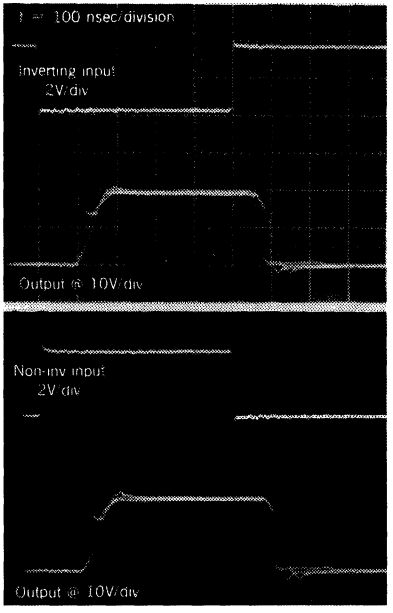


Figure 12

The overall transition time through the UC3706 is shown in figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20 nSec delay in turning off when the non-inverting input is used. Here, and in further discussions note that ON and OFF relate to the driven output switch, i.e., On is with the output HIGH, and vice versa. The shutdown, inhibit and protective functions all force the output LOW when active.

Note that the typical rise and fall times of the output waveform average 20 nsec with no load, 25 nsec with 1 nF, and 35 nsec when the capacitive load is 2.2 nF at room temperature. Multilayer ceramic capacitors are used in this test and located as physically close to the IC output as possible to minimize lead and connection inductance.

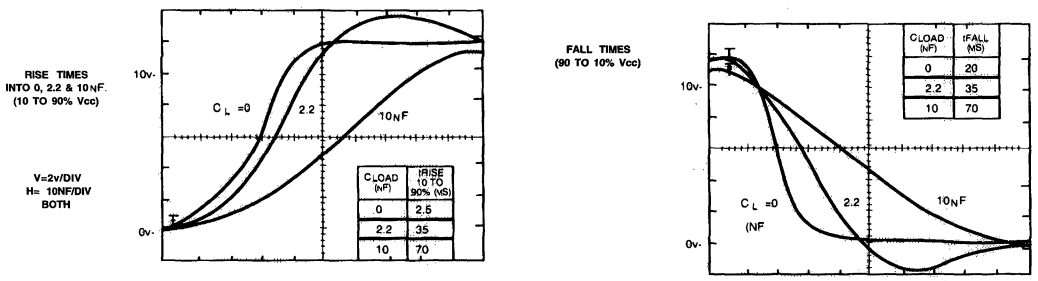


Figure 13

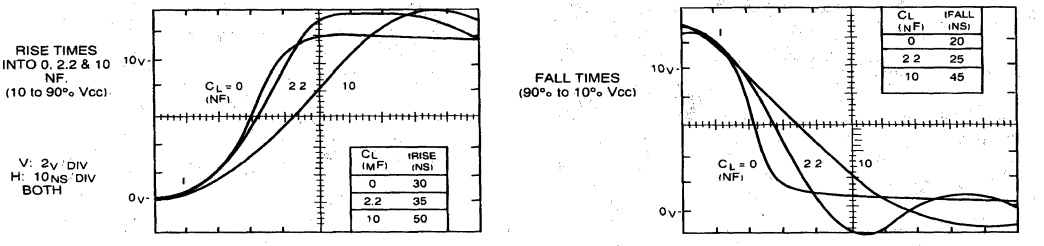


Figure 14

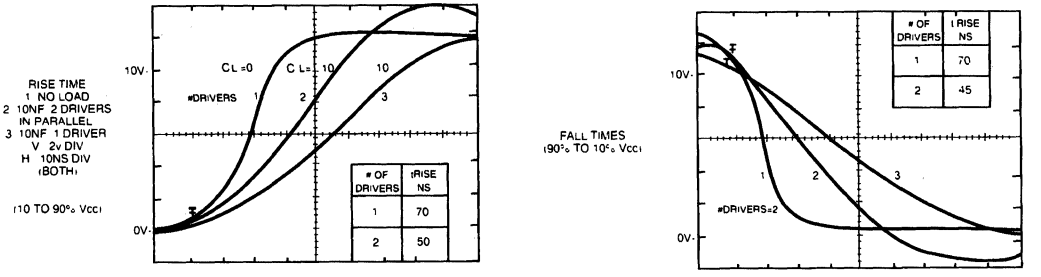


Figure 15

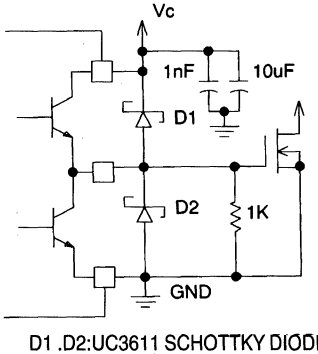
The peak current of each totem-pole output, whether source or sink, is 1.5 amps. However, on dual output versions like the UC3706, UC3707 and UC3709, both of the outputs can be paralled for 3 amp peak currents. In close proximity on the same die, each output virtually shares identical electrical and thermal characteristics. Saturation voltage is high at this current level but falls to under 2V at 500ma per output. Examples of typical switching characteristics are displayed.

It should be noted that while optimized for driving power MOSFET device, the UC3705 /06 /07 /09 ICs perform equally well into bipolar NPN transistors. In a steady-state off condition, the output saturation voltage is less than 0.4 volts as currents to 50 milliamps.

DIRECT COUPLED MOSFET DRIVE

The circuit of figure 17 shows the simplest interface to a power mosfet, direct coupling. In this example, an IRFP460 will be used to demonstrate the typical rise and fall times obtainable with a single 1.5 amp peak totem-pole driver. Further testing will include paralleling both outpus of a dual driver for a 3 amp peak capability. The IRFP460 device was selected, being the largest commercially

POWER MOSFET DRIVE CIRCUIT



D1 .D2:UC3611 SCHOTTKY DIODES

Figure 16

available FET die (a size "6") at the time of this writing whose specifications were listed previously.

The typical values of each charge will later be used in conjunction with the measured driver performance to estimate the actual peak current delivered during each interval of turn-on. The tests shown were conducted at room temperature with the FET located directly at the IC output pins to nullify any effects of series inductance. Additional tests and measurements will demonstrate the effects of circuit inductance on gate driver performance.

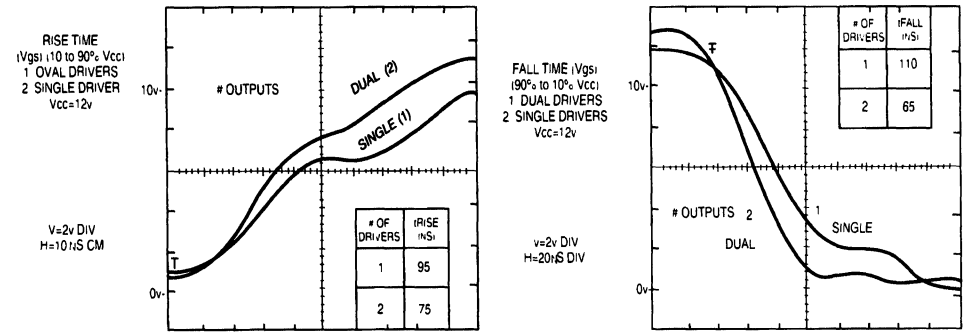


Figure 17

AVERAGE DRIVER CURRENTS DURING TURN-ON & TURN-OFF INTERVAL

EQUATIONS: $Q = CV$; $Q = IT$; $i_{AVG} = \frac{C.V}{T}$

During the transitions between 0 & 10V over Tr & Tf intervals

SINGLE OUTPUT

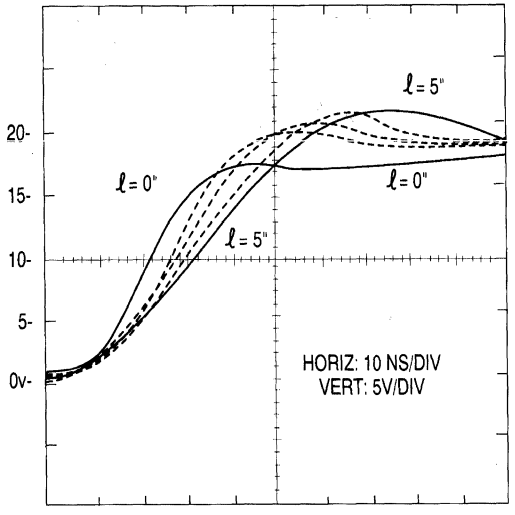
LOAD	RISE	FALL
C = 2.2NF	0.49A	0.67A
C=10NF	1.43A	1.43A
IRFP460	1.26A	1.10A

DUAL OUTPUTS

LOAD	RISE	FALL
C = 2.2NF	0.63A	0.88A
C = 10NF	2.0A	2.22A
IRFP460	1.6A	1.85A

While directly connecting the FET gate to the output of the driver is straightforward for testing purposes it does not represent the "real" application which may include several inches or wire or printed circuit board traces, Here, wiring inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. Extreme examples of this can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings.

Additionally, negative transitions (below ground) at the deriver output can raise havoc with the internal circuitry, leading to undesirable performance. While this is more of a concern with PWMs, (which use low level analog input signals) it will also detract from the drivers peak performance. Both of these conditions can easily be avoided by Schottky clamping the circuit to the auxiliary supply rails.



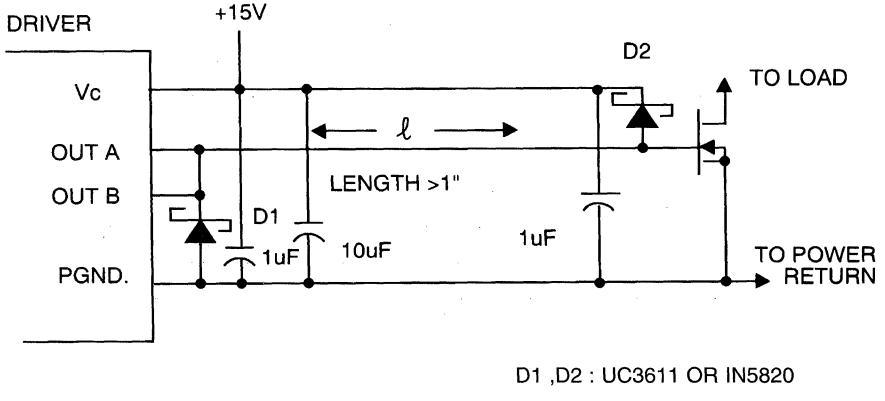
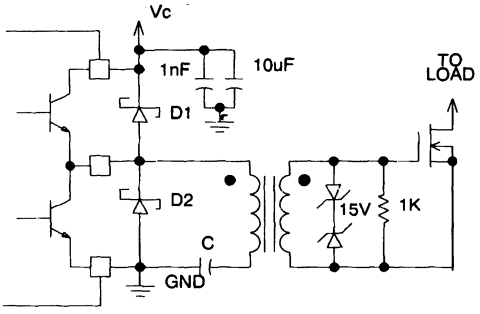


Figure 19

ISOLATED GATE DRIVE

In certain applications, the PWM is referenced to the load or secondary side of the power supply and the gate drive is transformer coupled across the isolation boundary to the power FETs. While this technique may work adequately at low switching frequencies, any series circuit inductance, as shown, will significantly degrade switching speeds and performance as the frequency is increased. An improved version of this circuit locates the drivers on the primary side, as close as possible to the FETs, and transformer couples only the low power input signals. Although somewhat more elaborate, significant improvements in turn-on and turn-off switching times are obtained and the FET switching losses are minimized.

TRANSFORMER COUPLED MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODE ARRAY

Figure 20

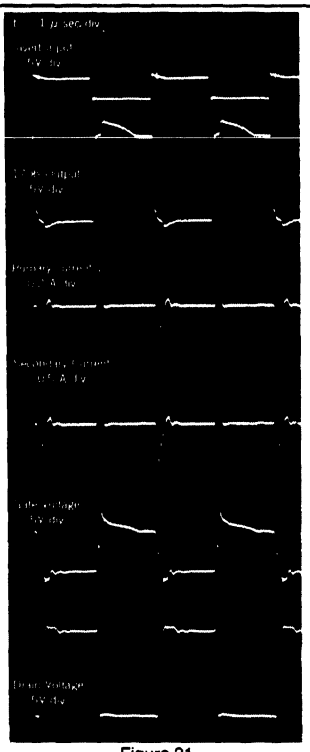


Figure 21

IMPROVED XFMR COUPLED DRIVE CIRCUIT

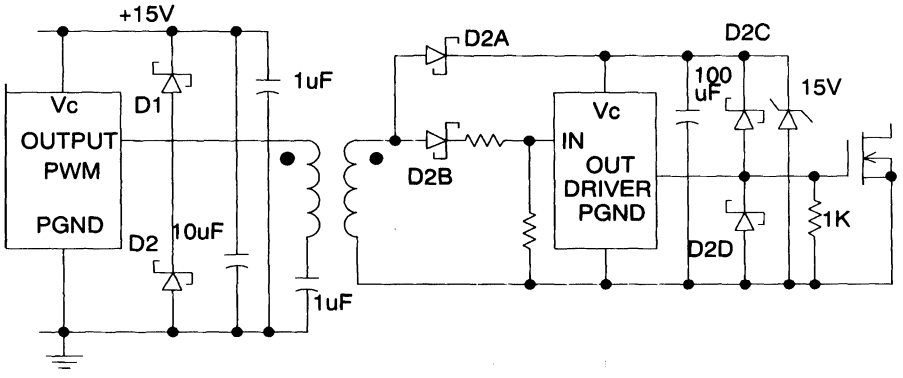


Figure 22

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC3706 can easily be configured for implementing the balanced transformer drive as shown in figure24. Outputs A and B are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC3706 output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back-to-back zeners on the secondaries are necessary to minimize the overshoot causes by the ringing of the gate capacitance with circuit inductances. Waveforms of all significant points within this circuit are shown.

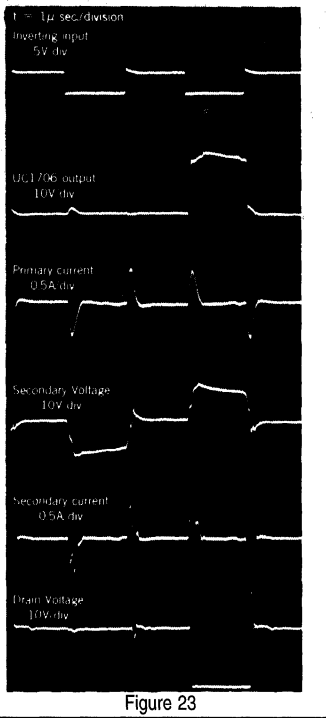


Figure 23

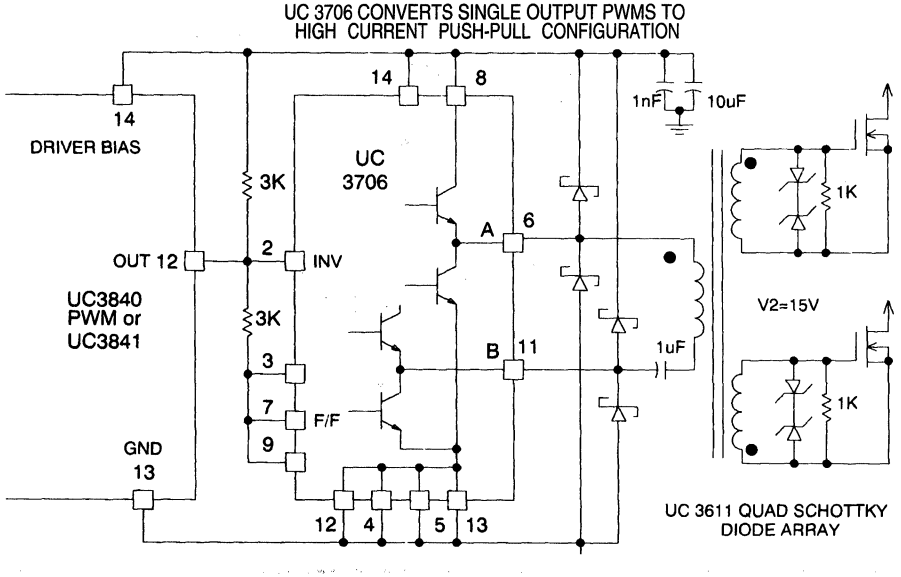


Figure 24

SUPPLYING POWER TO THE DRIVERS

From the block diagrams of figures 6 thru 8, note that the UC3705 UC3706 and UC3707 have two supply terminals, Vin and Vc. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Therefore, Vin can also be used to activate the outputs and no current is drawn from Vc when Vin is low. This is useful in off-line applications where its desirable for the control circuit to have a low start-up current. Several PWM controllers, like the UC1840, UC1841 and the UC1851 feature a Driver Bias output which goes high once the undervoltage lockout threshold is crossed, thus supplying bias to the driver. Adaptations of this technique can be made to work with a variety of other PWMs and control circuits.

USING "SPLIT" SUPPLIES

Many applications utilize a negative voltage rail in the drive circuit to guarantee complete turn-off of power MOSFETs, especially those with low gate threshold voltages, typical of "logic level" input devices. This is easy to implement with any of the UC3705 thru UC3709 drivers by offsetting the input signals with a zener diode equal in voltage to the negative supply, Vee. Although referenced at the driver IC to the Vee rail, these inputs are offset by an equal amount to the PWM controller, simulating a ground referenced input. This technique also offers moderate improvements in FET switching speeds at the penalty of slightly increased effective delay times from the driver inputs. The end results are listed below, which may be beneficial in applications where a tailored gate drive is required to alter the MOSFET switching characteristics.

POWER MOSFET DRIVE CIRCUIT
USING NEGATIVE BIAS VOLTOGE AND LEVEL SHIFTING
TO GROUND REFERENCED PWMS

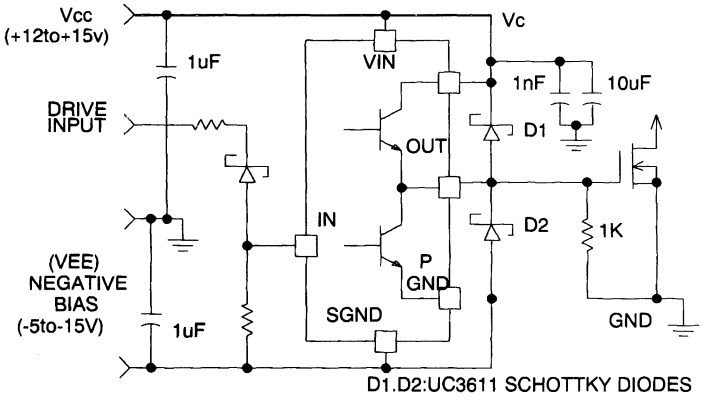


Figure 25

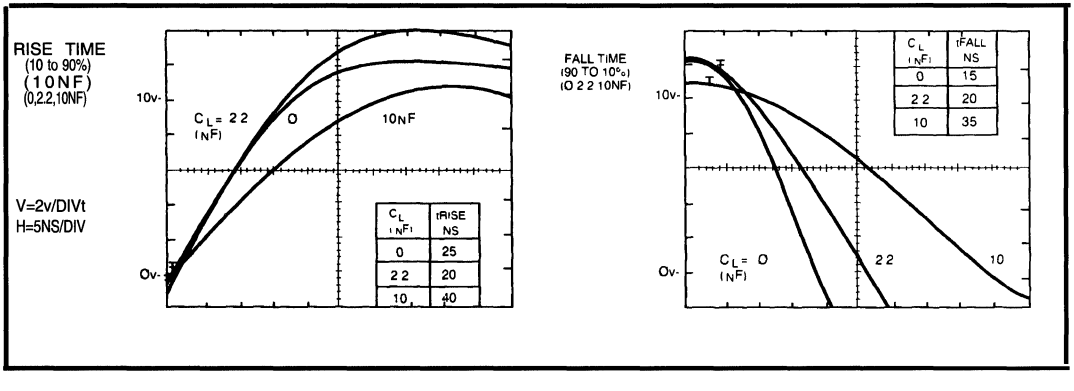


Figure 26

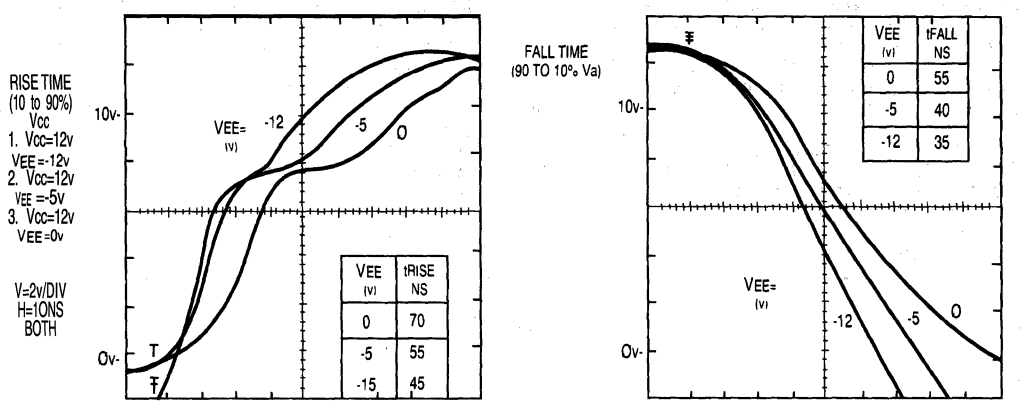


Figure 27

VEE (V)	td Rise to "0" V (NS)	T Rise 0-10V (NS)	Td Fall to begin (NS)	T Fall 10-0V (NS)I	T Delay total (NS)	Tr & Tf total (NS)	T Total tr+tf+trd (NS)
0	56	50	50	45	106	95	201
-5	70	42	50	33	120	75	195
-10	86	34	50	29	136	63	199
-12	93	32	50	28	143	60	203
-15	100	30	50	27	150	57	207

VEE (V)	Delay trd+tfd (NS)	Transition Times tr+tf (NS)
0	Minimum (106NS)	Maximum (95NS)
-15V	Maximum (143NS)	Minimum (60NS)

VEE (V)	Rise	Fall
0	2.4A	2.67A
-5	2.86A	3.64A
-10	3.53A	4.14A
-15	4.0A	4.4A

SUMMARY

This paper has presented an understanding of the dynamics of high speed power MOSFET switching in an attempt to define the optimum gate drive requirements to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed towards achieving these goals. The UC3705, UC3706, UC3707 and UC3709 drivers provide high speed response, 1.5 amps of peak current per output and ease the implementing of either direct or transformer coupled drive to a broad range of power MOSFETs. With these new devices, one more specialized function has been developed to further aid the power supply designer simplify his tasks and enhance power MOSFET switching characteristics.

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UNIQUE CHIP PAIR SIMPLIFIES ISOLATED HIGH SIDE SWITCH DRIVE

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Application Engineer
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Abstract

High voltage, high current N-channel MOSFETs, now widely accepted in the industry, have found their way into numerous high power designs. As their cost to performance ratio continually improves, gate drive circuitry becomes a more significant factor in overall switch cost. This is most notable in "high-side" switching applications where an isolated gate drive is required. A new integrated circuit pair, the UC3724/UC3725, will be presented which implements a simple, isolated MOSFET gate drive circuit. To achieve a cost effective high side switch drive, UNITRODE has developed a unique modulation technique which transmits both signal and power across a small pulse transformer. This publication supercedes Unitrode Application Note U-124, originally written by C. S. Silva.

INTRODUCTION

Designers of power drives for PWM motor controls and switching power supplies often face the problem of driving the high-side MOSFET transistor in a high voltage power stage. In many applications, for example, bridge and three phase configurations, there are several of these switch drives to implement, and the level of complexity can be discouraging. From a cost standpoint, it is advantageous to utilize N- channel MOSFET devices in comparison to their more expensive - yet easier to drive P- channel counterparts. However, these high-side switch gate drive circuits can quickly become extravagant, and frequently result in complicated or unreliable schemes.

Probably the most common technique used in high-side drive circuits is to generate an isolated, or "floating" auxiliary supply voltage. Referenced to the high-side MOSFET's source, this supply powers a conventional gate drive circuit. The average auxiliary power consumed is generally well below one watt, and varies with switching frequency, FET size and number of paralleled FETs used to configure "one" switch. A typical circuit using this method is shown in figure 1.

With the realization that average MOSFET gate drive power is quite small, charge pump circuits are frequently used to implement the floating supply. In these designs, the storage capacitor can become large in an attempt to minimize the supply's ripple voltage and may impair the useable range of frequencies and duty cycles. Due to this constraint, the switch on-time must be limited by the control circuit, and preferably, under-voltage lockout incorporated in the driver circuit to assure reliable operation.

A simple alternative to this discrete approach can be obtained by using a high voltage IC - provided that the maximum switch voltage and on-time are within it's capability. There is, however, a cost penalty for this single chip solution. While the basic gate drive and protection circuitry have a low voltage requirement, the level shifting transistors necessitate a high voltage IC process - an option which is inherently expensive. Additionally, many motor drive circuits cannot tolerate an on-time limitation, and require an auxiliary power supply for continuous (DC) operation.

Typically, an opto-coupler is used to translate the switch activation command from the ground referenced, or "low-side" control circuitry up to the high-side driver. Unfortunately, this technique comes with its own set of reliability issues which includes low common mode transient immunity, and performance degradation over time and temperature. High voltage MOSFET circuit slew rates can easily exceed 20 kV/us causing opto-coupler self turn-on or turn-off. The opto-coupler's AC common mode rejection must be carefully evaluated, as this specification is usually influenced by common mode voltage as well as dv/dt. Power up and power down sequences also present potential failure without undervoltage lockout circuitry.

TYPICAL HIGH SIDE DRIVER APPLICATION

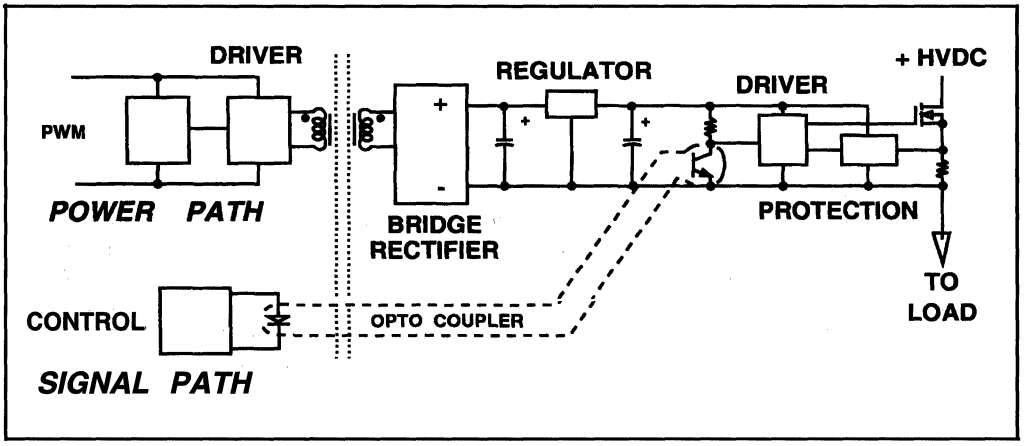

Figure 1.

UC3724 / UC3725 DRIVER PAIR - BASIC CIRCUIT

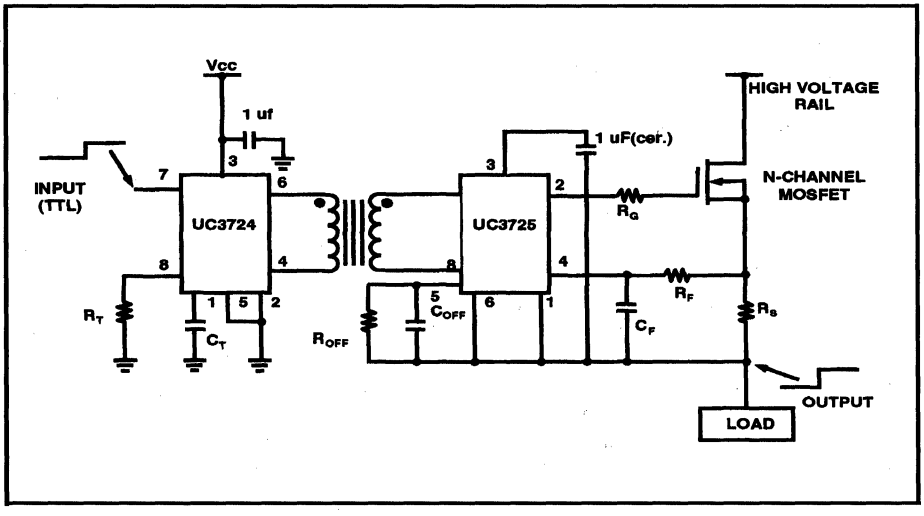

Figure 2.

UC3724/UC3725 DRIVER PAIR

The Unitrode UC3724/UC3725 IC pair offers a compact, and comparatively inexpensive design solution to the problem of supplying both isolated power and command signals. Figure 2 shows the basic circuit implementation. The two ICs, a pulse transformer, and a few passive components form a complete isolated MOSFET driver. A unique modulation technique simultaneously transmits power and command information across the transformer.

Provided the operational voltage is low, integrated circuit technology allows sophisticated circuits to be implemented at low cost. Transformers can easily provide several thousand volts of isolation, while supplying both power and signal. By exploiting each device's strengths, a low cost, high performance solution is achieved.

The UC3724 transmitter IC generates the carrier signal, with one of two possible duty cycles as commanded by the TTL level input. A unique carrier oscillator design not only sets the operating frequency, but also prevents the transformer from saturating, by assuring that the transformer magnetizing current is zero before initiating a subsequent oscillator cycle. Average transformer voltage is always zero, even under the transient conditions caused by input command changes. Saturation of the transformer core is virtually impossible using this technique.

To minimize transformer size and cost, a high frequency carrier is used. Although the carrier frequency limits the maximum transmitted switching frequency, it has no effect on input to output delay, which is solely determined by circuit propagation time.

The UC3725 driver IC rectifies the transformer isolated carrier to power the driver circuitry. Additionally, comparator circuitry determines the input command by sensing which duty cycle is transmitted, driving the MOSFET gate accordingly with the high current output stage. A comparator with programmable off time circuitry implements local over-current protection, while an enable input provides additional control and protection flexibility.

UC3724 ISOLATED DRIVE TRANSMITTER - BLOCK DIAGRAM

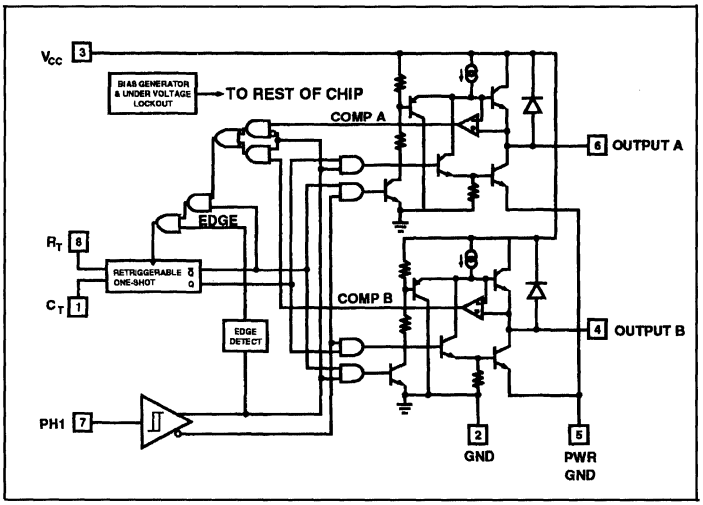

Figure 3.

UC3724 DRIVE TRANSMITTER

The UC3724 block diagram is shown in figure 3. The circuit consists of a bias voltage generator with under voltage lockout, control logic, a retriggerable one-shot, a TTL compatible input with hysteresis, two tri-level output drivers, and two zero current sense comparators.

The under voltage lockout inhibits the output drivers when the input supply voltage is below 9 volts. Once adequate supply voltage is present,

the bias generator supplies the appropriate internal voltages and currents, allowing the outputs to be enabled. This assures correct operation at power-up and power-down.

The carrier oscillator uses both a one-shot pulse width and the transformer core reset time to set the overall period. The one shot pulse width (T_{PW}) equals one-third of the nominal carrier period, and is set by timing resistor (R_T) and capacitor (C_T).

1) $T_{PW} = 0.51 \bullet R_T \bullet C_T + 150ns$ (sec)

"Full" supply voltage is applied to the transformer primary during this time by driving one output high and the other low. Transformer magnetizing current rises linearly at a rate determined by the primary inductance and applied voltage.

2) $di/dt = \dfrac{V_A - V_B}{L_{pri}}$ (amps / sec)

When the one-shot pulse ends, the low output switches high, and the high output switches to approximately one-half of the supply voltage. This applies "half" supply voltage to the primary, effectively in a reverse polarity to that of it's previous state. Internal offset circuitry compensates for output conduction voltage drops and maintains the full/half voltage ratio over temperature and supply voltage variations.

Power is transferred to the secondary circuit only while full voltage is applied to the primary. During this period the primary current is a composite of load and magnetizing current. The load current is interrupted when the half voltage is applied, so the residual primary current flowing is the magnetizing current.

With half voltage applied, the magnetizing current falls at one-half of the rate at which it had increased. An interval twice the programmed one-shot period is therefore necessary to reset the cores magnetizing current to zero and prevent any possibility of core saturation. The UC3724 incorporates a zero current detection circuit which guarantees that the magnetizing current has reached zero before initiating another oscillator cycle.

UC3724 OPERATIONAL WAVEFORMS (STEADY STATE)

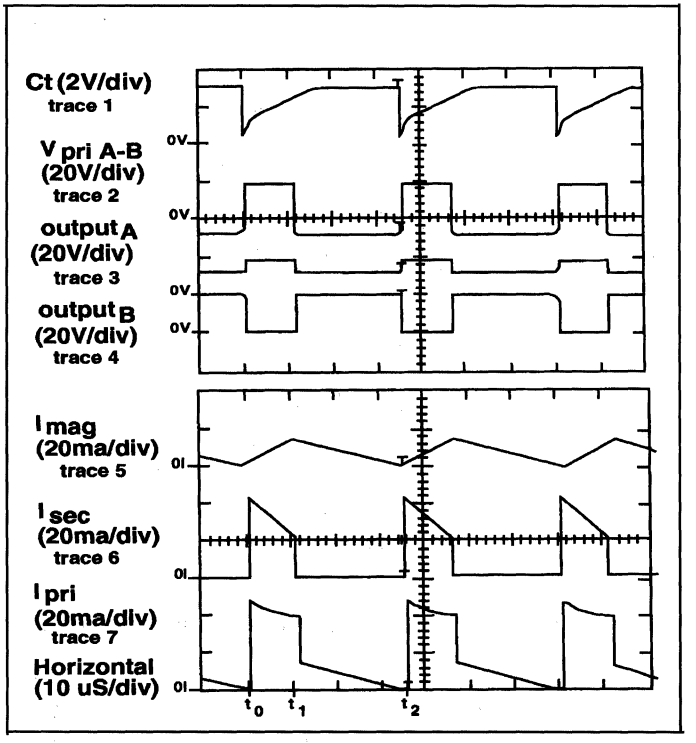

Figure 4.

Steady-state (continuous logic low input command) waveforms are shown in figure 4. The first traceshows timing capacitor (C_T) voltage, which is charged by a current set by the timing resistor (R_T). At time t_0, the one-shot is triggered, discharging the timing capacitor. Output$_A$ (trace 3) switches high, and output$_B$ (trace 4) switches low, with the resulting differential voltage V_{priA-B} (trace 2) applied across the transformer primary. The transformer magnetizing current (trace 5) increases linearly at a rate described by equation 2.

At time t_1 the timing capacitor voltage reaches the 2.5 volt threshold, ending the one-shot period. Output$_A$ is switched to $(V_{CC}/2) + V_{offset}$, and output$_B$ is switched high, allowing it's catch diode to conduct. The primary voltage (V_{priA-B}), is inverted, and reduced in half, causing the magnetizing current to fall at half the rate at which it had increased.

Output$_A$'s current sense comparator senses that the magnetizing current has reached zero at t_2 triggering the one-shot, thus initiating another oscillator cycle. If a continuous high is commanded, the waveforms for output$_A$ and output$_B$ are interchanged, and the magnetizing current is inverted.

At an input command transition, the existing oscillator cycle is terminated, the A and B outputs are reversed, and a new oscillator cycle is initiated. This applies full voltage of the appropriate polarity across the transformer primary for detection by the UC3725 Although the oscillator cycle has been terminated without allowing the core to reset, there is no danger of saturation. By reversing the outputs, the magnetizing current must first cross through zero before rising in the opposite polarity. The peak magnetizing current is actually less than a normal cycle, reducing the fall time, and hence the oscillator period.

UC3725 ISOLATED SIDE MOSFET DRIVER BLOCK DIAGRAM

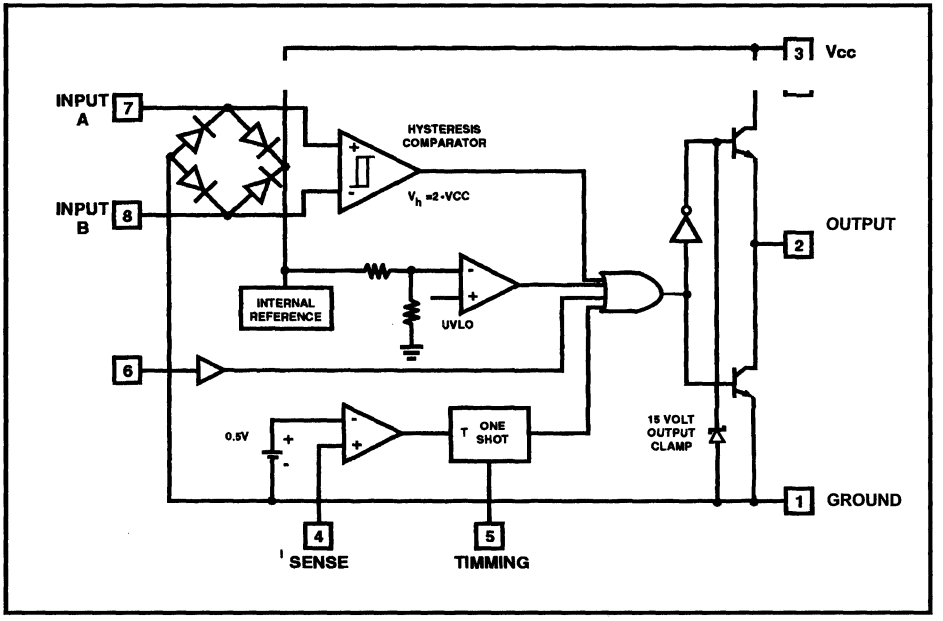

Figure 5.

UC3725 ISOLATED MOSFET DRIVER

The block diagram for the UC3725 is shown in figure 5. The circuit consists of a Schottky bridge rectifier, an internal reference with under voltage lock out, a differential hysteresis comparator, a high current totem-pole driver, a current sense comparator with programmable off time one-shot, and an enable input.

The Schottky bridge rectifies the isolated secondary voltage, providing power for the IC. A small capacitor, typically a 1uf ceramic, provides filtering and bulk storage to supply the high peak currents required to rapidly charge the MOSFET gate.

The undervoltage lockout inhibits the output driver when the supply voltage is below 12 volts. This assures that sufficient voltage is available to drive the MOSFET gate, preventing possible destructive linear operation.

The output driver is capable of delivering nearly two amps peak, which is more than adequate for most applications. The UC3725 features a self biasing drive arrangement which actively sinks gate current during under voltage lockout, preventing MOSFET self turn on. No additional gate to source resistor is required. The output voltage is clamped to 15 volts, which along with undervoltage lockout, virtually eliminates the possibility of incorrect gate drive voltages

Over-current protection is provided by monitoring the voltage across a source resistor. The current sense comparator triggers a one-shot, which turns off the MOSFET, when the voltage exceeds 0.5 volts. At power-up, C_{off} is charged to 7 volts. When an over-current is detected, the output is latched off, and the 7 volt source is disabled allowing R_{off} to discharge C_{off}. When C_{off} discharges to 2 volts, the output is enabled and C_{off} is charged back to 7 volts. Off time is typically selected to maintain safe MOSFET junction temperature with a continuous fault load, and is programmed by timing resistor (R_{off}) and capacitor (C_{off}) with the following equation.

3) $T_{off} = 1.28 \bullet R_{off} \bullet C_{off}$ (seconds)

An enable input allows direct output control for specialized applications. It can be used with level shifting transistors, optocouplers, or other source referenced circuitry such as a UC3730 thermal monitor circuit for MOSFET over-temperature protection.

The input command, transmitted by the UC3724, is demodulated using a differential hysteresis comparator. The comparator senses whether the "full voltage" applied to the transformer is positive or negative, corresponding to an "off" or "on" input command. The bridge rectifier causes the peak secondary voltage to always be two diode drops above V_{CC} while the comparator hysteresis is internally set to twice V_{cc}. The MOSFET is turned on when the secondary voltage is more negative than $-(V_{CC})$, and turned off when more positive than V_{CC}. Note that there is a logic inversion between the hysteresis comparator and the gate driver.

Referring to steady-state waveforms (figure 4) the secondary current (trace 6) charges the supply capacitor during the full voltage output segment of the oscillator cycle (time t_0 thru t_1). During the half voltage output segment (time t_1 thru t_2), no secondary current flows, thus only magnetizing current is present in the primary current (trace 7) allowing proper oscillator operation.

For this example, a 30% duty cycle input command was arbitrarily selected, and the associated waveforms are shown in figure 6. At time t_0, the input command (trace 1) transitions from low to high, immediately switching output, low, output, high, and retriggering the one-shot. The differential hysteresis comparator switches low, driving the output (trace 4) high, when the transformer secondary voltage ($V_{sec\ A-B}$, trace 3), is more negative than $-(V_{CC})$. The primary current (trace 2) is inverted from the $output_A$ and $output_B$ reversal, but power delivery to the IC is unaffected due to the bridge rectifier input.

The input command transitions low at time t_1, switching output, high, output, low, and retriggering the one-shot. The hysteresis comparator switches high, driving the output low, when the secondary voltage exceeds V_{cc}. Note the reduced magnetizing current fall time, and associated oscillator period reduction, after input command transitions.

OPERATIONAL WAVEFORMS AT 30% DUTY CYCLE

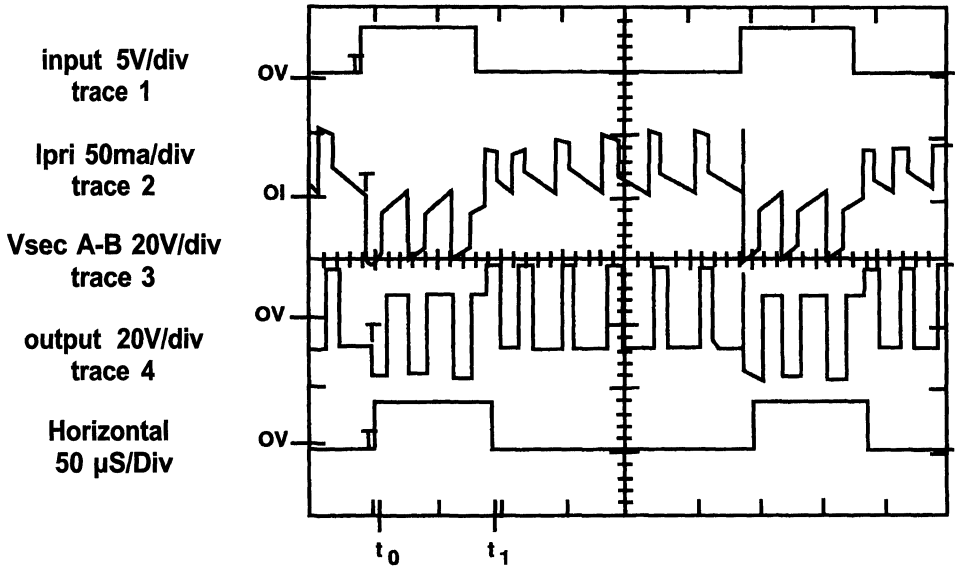

Figure 6.

PRACTICAL CONSIDERATIONS

The selection of carrier frequency (or more appropriately one-shot period since carrier frequency varies at switching transitions), is influenced more by transformer design than performance objectives. The minimum switching command period should be limited to four times the one-shot pulse width, to assure that adequate time is available to reset the core. Note that this limits the maximum switching frequency - but not the duty cycle range which is always 0 to 100%.

Waveforms for a command period approximately four times the one shot pulse width are shown in figure 7. The carrier oscillator has sufficient time to reset the transformer core and prevent saturation.

The one-shot period has no effect on input to output propagation delay, since the leading edge provides the output command information. Turn-on and turn-off propagation delay waveforms are shown in figure 8.

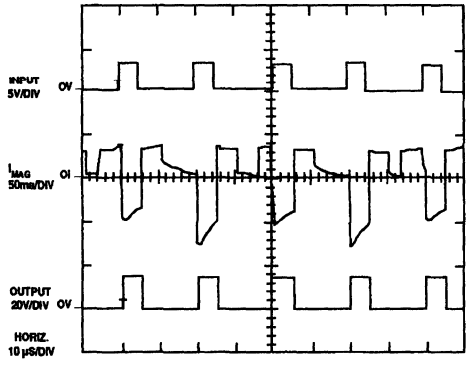

Figure 7.

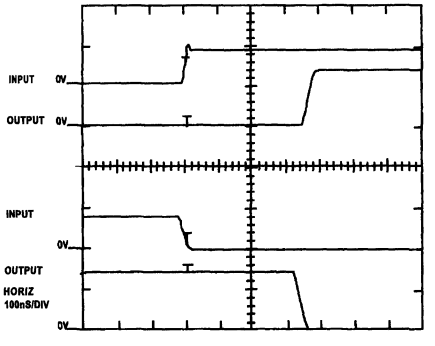

Figure 8.

The maximum carrier frequency is limited to 600 Khz. Most circuits will operate between 200 and 600 Khz., allowing switching frequencies up to 450 Khz., and a simple low cost transformer design. Nominal carrier frequency is calculated using equation 4.

$$4)\ F_c = \frac{1}{3 \bullet T_{PW}} \quad (Hz)$$

where T_{PW} = one-shot pulse width from equation 1.

Power supply voltage directly affects dissipation in the transmitter IC. Typical supply current verses voltage for the UC3724 is shown in figure 9. In most applications, bias power loss is about half of the total power dissipation.

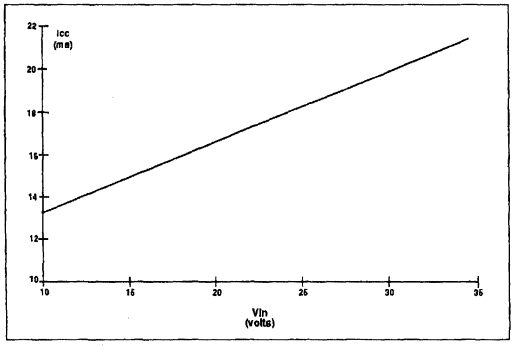

Figure 9.

The UC3725 driver IC provides sufficient gate voltage with a 15volt supply. Any further increase, although safe since the output is clamped to 15 volts, causes additional bias power dissipation. By adjusting the transformer turns ratio, a 15 to 18 volt secondary supply can be generated with any primary voltage, allowing maximum efficiency.

Magnetizing current also contributes towards increasing dissipation with supply voltage. Although the UC3724 outputs can handle several hundred milliamps of load current with the output transistors in saturation, nearly one-half V_{CC} is across the upper transistors during the magnetizing current fall time. Dissipation during this period usually limits the peak magnetizing current, although catch diode current (which only conducts falling magnetizing current) is limited to 50 mA peak. When the peak magnetizing current falls below 10 ma, the required primary inductance becomes excessive, resulting in a large number of turns or larger core size. Therefore, the optimal range of peak magnetizing current is between 10 and 40 mA.

In many applications, the average gate charge current delivered by the driver is insignificant in relation to the UC3725 bias current. When larger MOSFETs, particularly large parallel assemblies, are driven at higher frequencies, the average gate charge current will have a considerable effect on the total transformer load. Average gate charge current is the product of gate charge (Qg), which is specified by the MOSFET manufacturer, and the switching frequency.

$$5)\ I_g(avg.) = Q_g \bullet F_s \quad (amps)$$

where Q_g = gate charge
F_s = switching frequency

All of the charge delivered to the gate at turn-on must be removed at turn-off. The resultant average power dissipated by the driver and gate resistor is described by equation 6.

$$6)\ P_g = Q_g \bullet V_g \bullet F_s \quad (Watts)$$

where V_g = fully charged gate voltage

The over-current input on the UC3725 has a typical delay time of 150 ns. Most applications require a small RC filter to attenuate leading edge current spikes caused by parasitic capacitance and catch rectifier reverse recovery. Careful attention to layout and component selection is necessary to prevent false triggering. The current sense resistor should be non-inductive to minimize spiking and ringing. The filter capacitor should be located as close to the IC as possible, with direct connections to the comparator input and common. The connection between the UC3725 common, and the MOSFET source resistor, must have relatively low impedance to prevent gate drive current from affecting current sense accuracy. In addition this should be a "Kelvin" connection, such that no load current flows through it. If the current sense feature is not required, the comparator input is simply connected to common, and the timing input is allowed to float.

DESIGN PROCEDURE

Typically, the application dictates the MOSFET(s), switching frequency, and switch isolation voltage. For cost considerations, a supply voltage common with other circuitry, is usually chosen to power the UC3724. The designer is then left with the carrier frequency and peak magnetizing current to select. A high carrier frequency is normally used to minimize transformer size and cost. Magnetizing current is initially set to a nominal value, such as 20 ma, and then adjusted if necessary to optimize the transformer design.

The one-shot pulse width is set to 1/3 the carrier frequency using equation 1. By rearranging equation 2, and allowing 2 volts for saturation, the transformer primary inductance can be calculated.

$$7)\ L_{pri} = \frac{(V_{cc}-2)\bullet T_{pw}}{I} \text{ (Henries)}$$

where V_{cc} = supply voltage
T_{PW} = one-shot pulse width
I_{mag} = peak transformer magnetizing current

Transformer core selection is an iterative process based on the following two equations.

$$8)\ \Delta B = \frac{V_{applied}\bullet T_{on}\bullet 10^4}{N_{turns}\bullet A_c} \text{ (Tesla)}$$

$$9)\ N_{turns} = \sqrt{\frac{L_{pri}\bullet 10^9}{A_L}} \text{ (turns)}$$

A toroid is usually the most cost effective core geometry for this application. The core material should be chosen for low losses and high permeability at the design frequency to minimize transformer size and number of turns. Thermal resistance and loss factors provided by the manufacturer are used to select the optimum core size. A flux density of .05 Tesla (500 Gauss) will cause approximately a 20 degree C rise at 500 KHz with common power materials such as Ferroxcube 3C8.

Typically most toroids used for this application have an AL between 1000 and 3000 mH/1000 turns. An estimated number of turns is calculated using an average A_L value of 2000 mH/1000 turns in equation 8. By rearranging equation 7, an approximate core are is calculated using a flux density of .05 Tesla, and the estimated number of turns. This leads to a first core selection, and an actual A_L value, which is used in equation 8 to calculate N_{turns}. The flux density is then checked using equation 7, and a larger or smaller core is selected if necessary.

The turns ratio is calculated using the following equation, which allows 2 volts for UC3724 output saturation, and 3 volts for UC3725 rectifier drop and output saturation.

$$10)\ \text{Turns ratio} = \frac{V_{cc}-2}{V_{gate}+3}$$

The power supplied by the transformer is the sum of the UC3725 bias loss and the average gate charge power. For minimum wire size, the resulting RMS winding currents can be calculated, although typically there sufficient space to use 24 to 28 AWG wire for ease of handling.

High voltage isolation is implemented by sleaving the primary winding with an insulation suitable for the required breakdown voltage. For low leakage inductance, bifilar windings are used, with additional turns added to the primary or secondary for non 1:1 turns ratios.

DESIGN EXAMPLE

The following design example is a general purpose isolated MOSFET gate driver. Up to 200 milliwatts is available for gate drive, which is suitable for most applications. A 15 volt power supply provides sufficient secondary voltage by using a step-up transformer.

Driver specifications:
* 200 milliwatts average gate drive power
* 100 KHz. switching rate
* 15 V supply voltage
* 1KV minimum isolation voltage

A 600KHz. carrier frequency is selected to minimize transformer size and cost. The one-shot pulse width is calculated by rearranging equation 4.

$$T_{pw} = \frac{1}{3 \cdot 600\ KHz}$$

$$= 556ns$$

Since the carrier frequency is near maximum, 2K will be used for R_T. C_T is calculated with equation 1.

$$C_T = \frac{(556-150)\ ns}{0.51 \cdot 2K}$$

$$= 398pf\ (use\ 390pf)$$

30mA is selected for the peak magnetizing current. The corresponding primary inductance is calculated with equation 7.

$$L_{pri} = \frac{(15-2)\ V \cdot 556ns}{30\ mA}$$

$$= 241\mu H$$

The estimated number of turns are calculated using equation 9 with an average value of 2000 mH/1000 turns for A_L.

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{2000}}$$

$$= 11\ turns$$

The approximate core area is calculated with equation 8, using a flux density of 0.05 Tesla.

$$A_c = \frac{13V \cdot 556ns \cdot 10^4}{11\ turns \cdot 0.05\ Tesla}$$

$$= 0.131\ cm^2$$

A one-half inch diameter toroid, Ferroxcube part number 204T250-3C8, is selected which has the following specifications.

$A_C = 0.148\ cm^2$
$A_L = 1620$ mH/1000 turns

N_{turns} is calculated using the actual A, value in equation 9.

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{1620}}$$

$$= 12.2\ turns\ (use\ 12\ turns)$$

The flux density is checked using equation 8.

$$\Delta B = \frac{(15-2)\ V \cdot 556ns \cdot 10^4}{12\ turns \cdot 0.148\ cm^2}$$

$$= 0.041\ Tesla$$

The turns ratio is calculated using equation 10 for a gate voltage of 12 to 14 volts.

$$Turns\ ratio = \frac{(15-2)\ V}{(12+3)\ V}$$

$$= 0.867$$

Therefore $N_{sec} = 14$ turns

The transformer is wound with 26AWG magnet wire for ease of handling. A teflon insulation sleeve is slipped over the primary winding to improve the primary to secondary breakdown voltage. The primary and secondary are wound bifilar, to minimize leakage inductance, then the two remaining secondary turns are wound.

To verify operation, the test circuit shown in figure 10 was built. The over current, gate and bulk storage components are selected per MOSFET and load requirements. Figure 11 and 12 show turn-on and turn-off waveforms respectively.

The lower MOSFET in figure 10 was configured to test self turn-on of the upper driver during high transformer dv/dt. With 300 volts slewing at a rate in excess of 25 kv/us, no evidence of driver self turn-on was observed.

APPLICATIONS

Although the lower MOSFET driver is configured for faster switching than would normally be required, figure 10 is typical of half bridge outputs, where two or three of these circuits could implement a full or three phase bridge respectively. Full isolation for UL or VDE requirements can be met

by using isolated drivers for both upper and lower MOSFETs. This configuration can also greatly reduce noise in high current applications, by completely isolating the control circuitry from output devices.

TYPICAL HIGH SIDE DRIVE APPLICATION CIRCUIT SCHEMATIC

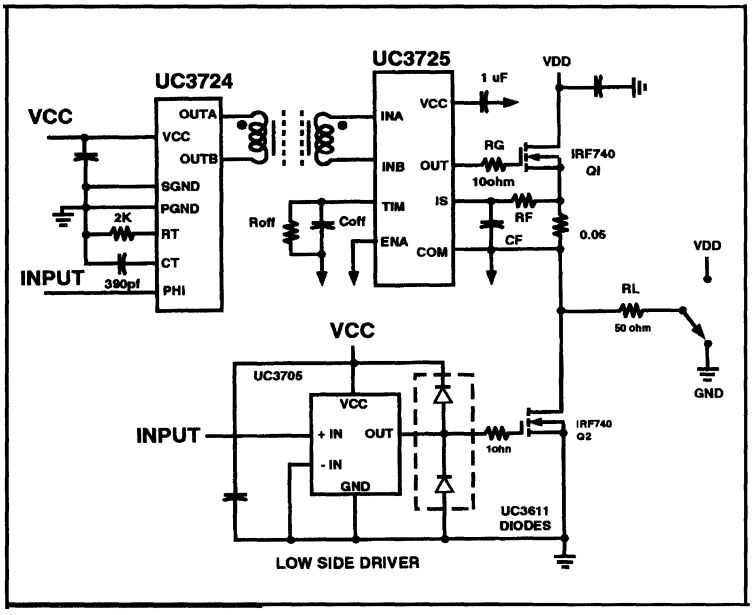

Figure 10

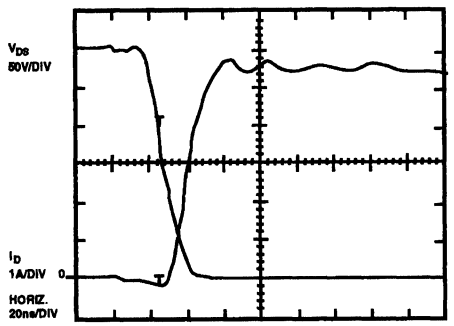

Figure 11

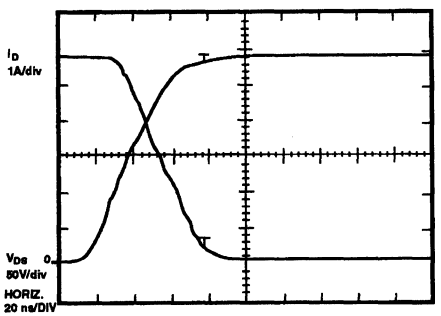

Figure 12

FULL BRIDGE OUTPUT

Some circuits have multiple MOSFETs driven from the same command, which are isolated from each other. A most notable example is the full bridge, which is commonly used in brush and stepper motor drives. Multiple secondaries can drive additional isolated UC3725 circuits, from a single UC3724, further reducing cost and complexity.

Figure 13 shows a fully isolated bridge circuit. By isolating all of the MOSFETs and the current sense signal, complete control to output isolation is achieved. Dual secondaries on each transformer eliminates the requirement for two additional transformers and UC3724s. For feedback and protection, a hall effect current sensor monitors load current directly, while providing high voltage isolation. The local over-current circuit in the upper FET drivers protects during load to ground shorts.

FULL BRIDGE OUTPUT CIRCUIT

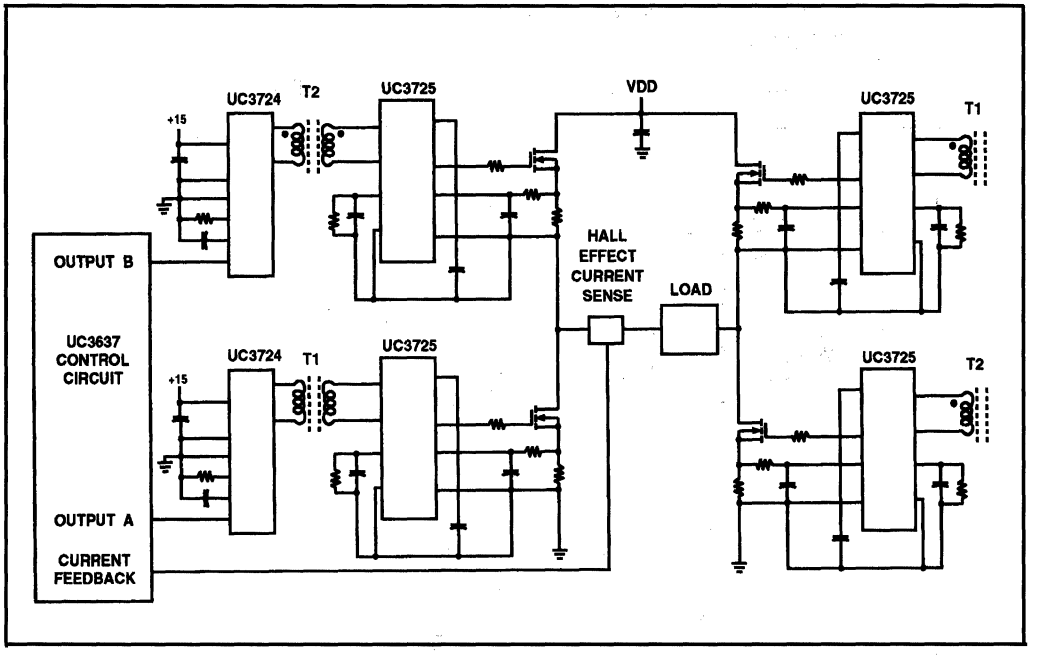

Figure 13

HALF BRIDGE OUTPUT CIRCUIT

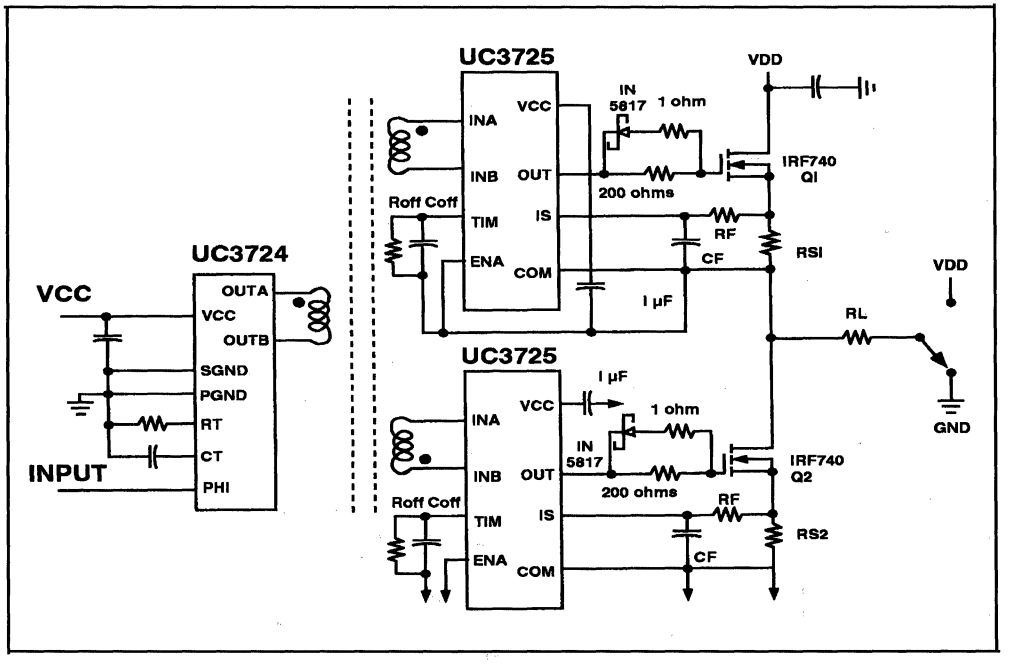

Figure 14

HALF BRIDGE OUTPUT

By reversing the polarity of one of the secondary windings on a dual secondary transformer, two FETs are switched out of phase from each other. A typical application for this arrangement is the half bridge, and is shown in figure 14. Dead-time between turn-off and turn-on is difficult to implement using this technique. To turn off both FETs, the UC3724 supply voltage must be removed, or the UC3725 enable inputs driven high. While shutting down the supply voltage is suitable for power-up/power-down protection, it is to slow to control dead-time. Isolating or level shifting the enable inputs adds complexity and negates the advantage of using a dual secondary transformer. Cross conduction is easily minimized however, by the gate resistor arrangement which provides rapid turn-off and slow turn-on. This technique is also typically used to minimize cross conduction caused by stored charge in the MOSFET body diode.

LEVEL SHIFT DRIVER

The UC3725 makes an excellent level shifted driver for lower voltage, non-isolated applications. All of the necessary protection features which are often omitted in discrete designs are incorporated in the UC3725 assuring reliable operation under all conditions. Figure 15 shows a typical level shift circuit with a "boot-strap" supply. The MPS-U10 level shift transistor has a maximum V_{ceo} of 300 volts, although it's dissipation without a heatsink limits the maximum supply to approximately 200 volts. Figure 16 shows input to output propagation delay while switching 150 volts and 3 amps. A 20 mA current source with a voltage compliance 15 volts above the supply rail can be used in place of the boot-strap circuit, for applications which cannot tolerate an on-time limitation. The cost effectiveness of this approach will depend on supply voltage and number of high-side MOSFETs.

LEVEL SHIFT CIRCUIT

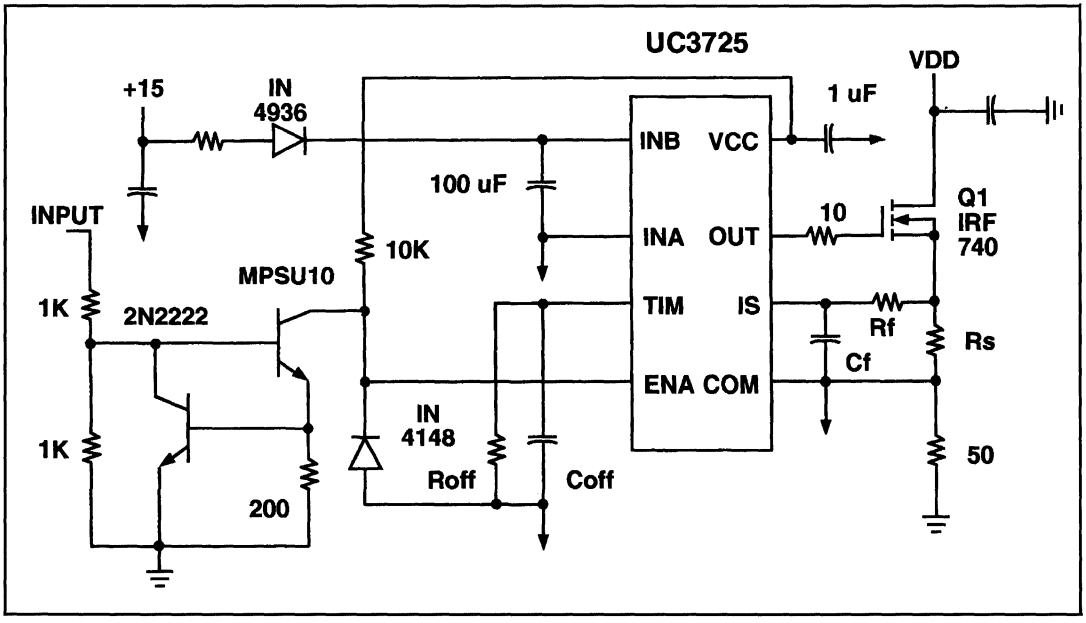

Figure 15

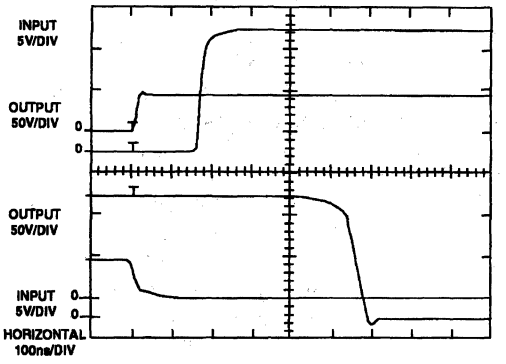

Figure 16.

LATCHED OVER-CURRENT FAULT

Current limiting is provided by the control circuit in many applications. Local protection from the UC3725 is therefore only required for fault conditions which result in high di/dt such as output shorts. It may be desirable to latch the output off under such a fault, rather than enable after a fixed off-time. Figure 17 shows a simple circuit used in place of the timing resistor and capacitor which will latch the output off after the over-current comparator is triggered. The 10uf capacitor resets the circuit at power-up by holding the timing input below the 2 volt one-shot threshold. When an over-current is sensed, the timing input voltage falls, and is clamped at 5.1 volts. The one-shot period normally ends when C_{off} is discharged below 2 volts, but by clamping the voltage, the time constant effectively appears infinite.

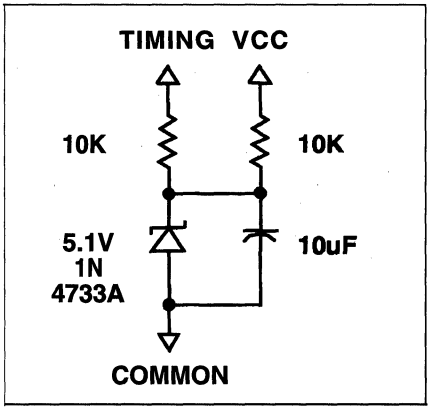

Figure 17

FAST AC SWITCH

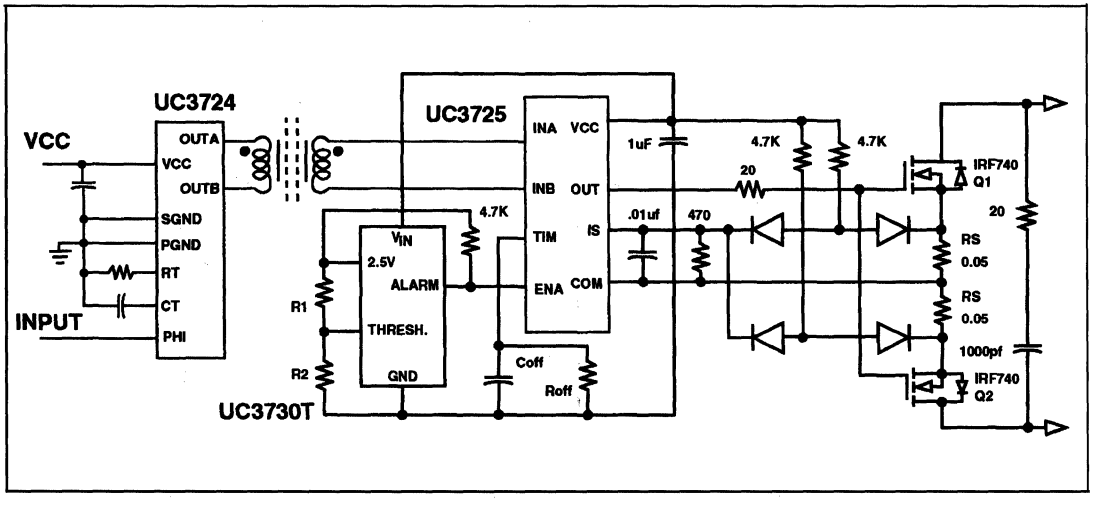

Figure 18

FAST AC SWITCH

Fully isolated gate drive lends itself to unique power switching circuits which are otherwise extremely difficult to implement. Figure 18 is a fast AC switch with over-current and over-temperature protection. The MOSFETs are selected to withstand the peak AC voltage, with each FET blocking in the opposite polarity. Figure 19 shows a 100 ohm load switched across 115 VAC, 60 Hz. The diode network allows current sensing in both directions, with the 4.7K resistors functioning as current sources. Protection against excessive MOSFET junction temperature is accomplished by mounting both FETs and the UC3730T on the same heatsink. MOSFET thermal resistance (junction to heatsink), and maximum FET dissipation must be considered when selecting the shut-down temperature set by R1 and R2. Refer to UC3730 datasheet for additional information. A 1000pf/20 ohm snubber is connected across the switch to reduce turn-off voltage spiking. The actual snubber values required are determined by load conditions.

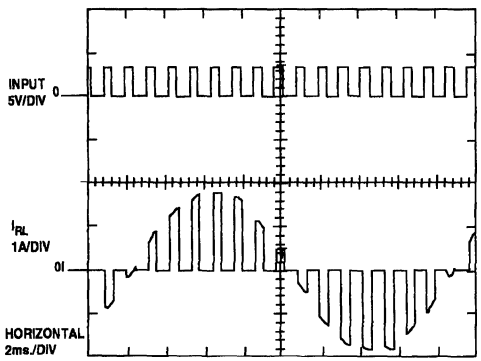

Figure 19.

SUMMARY

A unique integrated circuit pair, the UC3724/UC3725 has been presented that provides a simple, low cost, isolated MOSFET gate drive solution. Protection features prevent abnormal gate drive voltage, and provide over-current limiting. Duty cycle or on time limitations typical of other techniques are avoided, and by utilizing a transformer for isolation, there are no inherent isolation voltage limitations. The circuit is suitable for fully isolated systems which must meet UL or VDE requirements, as well as typical high-side switch applications.

REFERENCES

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2. W. Andreycak, "1.5 mHz CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY", UNITRODE APPLICATION NOTE # U-110

3. W. Andreycak, "A NEW GENERATION OF HIGH PERFORMANCE MOSFET DRIVERS FEATURES HIGH CURRENT, HIGH SPEED OUTPUTS", UNITRODE APPLICATION NOTE # U-126

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APPLICATION NOTE

PRACTICAL CONSIDERATIONS IN HIGH PERFORMANCE MOSFET, IGBT and MCT GATE DRIVE CIRCUITS

BILL ANDREYCAK

INTRODUCTION

The switchmode power supply industry's trend towards higher conversion frequencies is justified by the dramatic improvement in obtaining higher power densities. And as these frequencies are pushed towards and beyond one megahertz, the Mosfet transition periods can become a significant portion of the total switching period. Losses associated with the overlap of switch voltage and current not only degrade the overall power supply efficiency, but warrant consideration from both a thermal and packaging standpoint. A/though brief, each of the Mosfet switching transitions can be further reduced if driven from from a high speed, high current totem-pole driver - one designed exclusively for this application. This paper will highlight three such devices; the UC1708 and UC1710 high current Mosfet driver ICs, and the UC1711 high speed driver. Other Mosfet driver ICs and typical application circuits are featured in UNITRODE Application Note U-118.

EFFECTIVE GATE CAPACITANCE

The Mosfet input capacitance (Ciss) is frequently misused as the load represented by a power mosfet to the gate driver IC. In reality, the effective input capacitance of a Mosfet (Ceff) is much higher, and must be derived from the manufacturers' published total gate charge (Qg) information. Even the specified maximum values of the gate charge parameter do not accurately reflect the driver's instantaneous loads during a given switching transition. Fortunately, FET manufacturers provide a curve for the gate-to-source voltage (Vgs) versus total gate charge in their datasheets. This will be segmented into four time intervals of interest per switching transition. Each of these will be analyzed to determine the effective gate capacitance and driver requirements for optimal performance.

Inadequate gate drive is generally the result of underestimating the effective load of a power mosfet to its driver.

TOTAL GATE CHARGE (Qg)

First, a typical high power Mosfet "Gate Charge versus Gate-to-Source Voltage" curve will be examined. An IRFP460 device has been selected and this curve is applicable to most other Fet devices by adjusting the gate charge numbers accordingly. Both turn-on and turn-off trasnsitions are shown with the respective drain currents and drain-to-source voltages.

TURN-ON WAVEFORMS

Gate voltage vs time

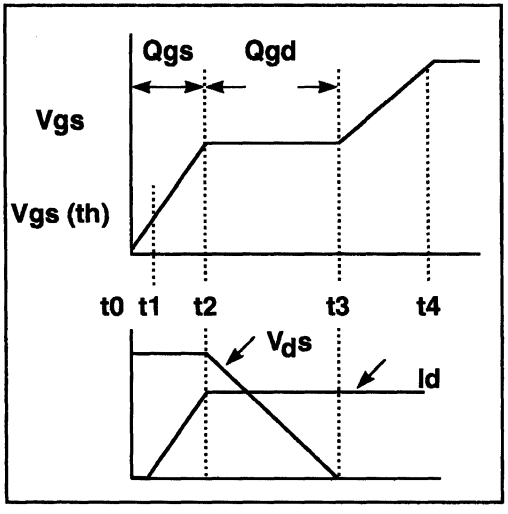


Figure 1.

INTERVAL t0-t1

The time required to bring the gate voltage from zero to its threshold Vgs(th) can be expressed as a delay time. Both the voltage across the switching device and current through it are uneffected during this interval.

INTERVAL t1-t2

This period starts at time t1 when the gate voltage has reached Vgs(th) and drain current begins to flow. Current continues to rise until essentially reaching its final value at time t2. While this occurred, the gate to source voltage had also been increasing. The drain-to-source voltage remains unchanged at Vds(off). Power in the Mosfet is wasted by the simultaneous overlap of voltage and current.

INTERVAL t2-t3

Beginning at time t2 the drain-to-source voltage starts to fall which introduces the "Miller" capacitance effects (Cgd) from the drain to the Mosfet gate. The result is the noticeable plateau in the gate voltage waveform from time t2 until t3 while a charge equal to Qgd is admitted. It is here that most drive circuits are taxed to their limits. The interval concludes at time t3 when the drain voltage approaches its minimum.

INTERVAL t3-t4

During this final interval of interest the gate voltage rises from the plateau of the prior region up to its final drive voltage. This increasing gate voltage decreases Rds(on), the Mosfet drain-to-source resistance. Bringing the gate voltage above 10 to 12 volts, however, has little effect on further reducing Rds(on).

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
to-t1	0-threshold	0	Vds(off)	Slew rate (dv/dt)
t1-t2	thrs-plateau	rising	Vds(off)	Slew rate (dv/dt)
t2-t3	V(plateau)	Ion(dc)	falling	Peak current I(max)
t3-t4	rising	Ion(dc)	Ion*Rds(t)	Peak I & dv/dt

TURN-OFF WAVEFORMS
Gate voltage vs. time

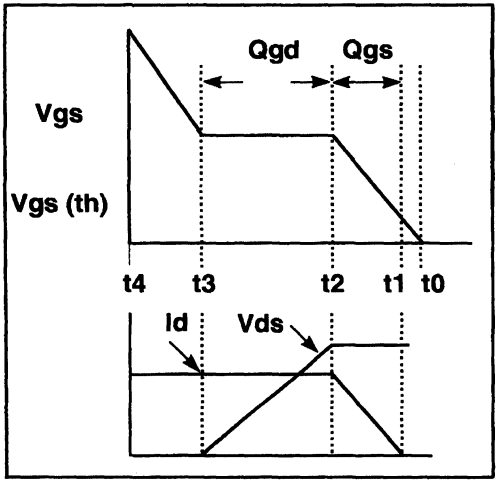


Figure 2

The intervals during turn-off are basically the same as those described for turn-on, however the sequence and corresponding waveforms are reversed.

INTERVAL t4-t3

The beginning of the turn-off cycle can be described as a delay from the final drive voltage (Vgs(on)) the the plateau region. Both the drain voltage and current waveforms remain unchanged while the devices effective resistance (Rds(on)) increases as the gate voltage decreases.

INTERVAL t3-t2

Once the plateau is reached at time t3, the gate voltage remains constant until time t2. Gate charge due to the Miller effect is being removed, an amount equal to Qgd. The drain voltage rises to its off state amplitude, Vds(off), while the drain current continues to flow and equals I(on). This lossy transition ends at time t2.

INTERVAL t2-t1

Once the Miller charge is completely removed, the gate voltage is reduced from the plateau to the threshold voltage causing the drain current to fall from I(on) to zero. Transition power loss ends at time t1 when the gate threshold is crossed.

INTERVAL t1 -t0

This brief period is of little interest in the turn-off sequence since the device is off at time t1.

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t4-t3	falling	Ion(dc)	Ion* Rds(t)	Peak I and dv/dt
t3-t2	V(plateau)	Ion(dc)	falling	Peak Current I (max)
t2-t1	Vplat-thrsh	falling	Vds(off)	Slew rate (dv/dt)
t1-t0	thrsh-0	0	Vds(off)	Slew rate (dv/dt)

FET Transition Power Loss

During each of the FET turn-on and turn-off sequences power is lost due to the switching device's simultaneous overlap of drain - source voltage and drain current. Since both the FET voltage and current are externally controlled by the application, the driver IC can only reduce the power losses by making the transition times as brief as possible. Minimization of these losses simply requires a competent driver IC, one able to provide high peak currents with high voltage slew rates.

A review of the prior transition waveforms indicates that power is lost between the times of t1 and t3. While t2 serves as the pivot point for which waveform is rising or falling, as the equations show its irrelavent in the power loss equation. For the purpose of brevity, the waveform of interest can be approximated as a triangle while the other waveform is constant. The duration between times t1 and t3 can now be defined as the net transition time, t(tran), with a conversion period of t(period)

During the two intervals from t1 to t3:

$$\text{Ploss} = \frac{0.5 * I(on) * Vds(off) * t(2\text{-}1)}{t(period)}$$

$$\text{Ploss} = \frac{0.5 * Vds(off) * I(on) * t(3\text{-}2)}{t(period)}$$

Combining the two equations with t(tran) = t3-1 results in a net loss of:

$$\text{Ploss} = \frac{0.5 * Vds(off) * I(on) * t(trans)}{t(period)}$$

Since these loses are incurred twice percycle, first at turn-on and then again at turn-off, the net result is a doubling of the power loss.

Ploss = Vds(off)*I(on)*t(trans)/t(period)

This relationship displays the need for fast transitions at any switching frequency, and is of significant concern at one megaHertz. Minimization of the FET transition power loss can be achieved with high current drivers.

GATE CHARGE

Each division of the transition interval has an associated gate charge which can be derived from the FET manufacturers datasheets. Since there are three basic shapes to the Vgs curve, the interval from t0 to t1 can be lumped together with that of the t1 to t2 period. For most large FET geometries, the amount of charge in the t0 to - t1 span is negligible anyway. This simplification allows an easy calculation of the effective gate capacitance for each interval along with quantifying the peak current required to traverse in a given amount of time.

Charge can be represented as the product of capacitance multiplied by voltage, or current multiplied by time. The effective gate capacitance is determined by dividing the required gate charge (Qg) by the gate voltage during a given interval. Likewise, the current necessary to force a transition within a specified time is obtained by dividing the gate charge by the desired time.

Cgs (effective) = delta Qg / delta Vgs

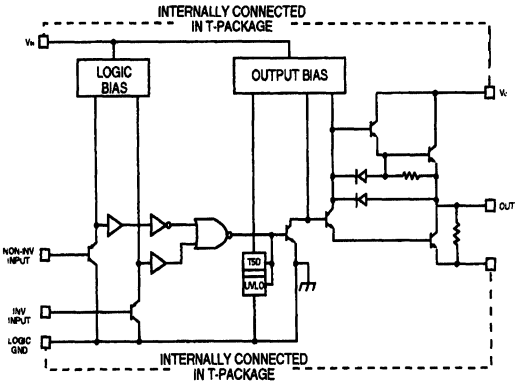
Ig(required) = delta Qg / t(transition)

UC1710
The "MILLER KILLER"

High peak gate drive currents are desirable in paralleled FET applications, typical of a high power switching section or power factor correction stage. Dubbed as "the Miller Killer", the UC1710 boasts a guaranteed 6 amp peak output current. This hefty driver current minimizes the FET parasitic "Miller" effects which would otherwise result in poor transi-

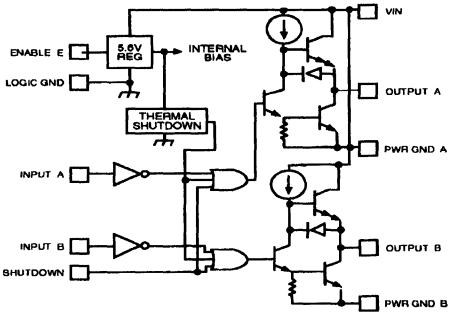
tion performance. Higher currents are possible with this driver, however the limiting factor soon becomes the parasitic series inductance of the FET package (15 nH) and the layout interconnection of 20 nH/inch. An RF type arrangement of the PC board layout is an absolute **MUST** to realize this device's full potential.

UC 1710 BLOCK DIAGRAM



The UC1710 has "no-load" rise and fall times of 20 nanoseconds (or less) which do not change significantly with any loads under 3 nanoFarads. It's also specified into a load capacitance of 30 nanoFarads, roughly equivalent to what is represented by three paralleled "size 6" FET devices. Propagation delays are brief with typical values specified at 35 nanoseconds from either input to a ten percent change in output voltage.

UC 1708 BLOCK DIAGRAM



The UC1708 is a unique blend of the high speed attributes of the UC1711 along with the higher peak current capability of the UC1710. This dual noninverting driver accepts positive TTL/CMOS logic from control circuits and provides 3 amp peak outputs from each totem pole.

Propagation delays are under 25 nanoseconds while rise and fall times typically run 35 nanoseconds into 2.2 nanoFarads. The output stage design is a "no float" version which incorporates a self biasing technique to hold the outputs low during undervoltage lockout, even with Vin removed.

In the 16 pin DIL package, the device features a remote ENABLE and SHUTDOWN function in addition to seperate signal and power grounds. The ENABLE function places the device in a low current standby mode and the SHUTDOWN circuitry is high speed logic directly to the outputs.

UC1708 / 1710 / 1711 PERFORMANCE COMPARISON
TABLE 1.

PARAMETER	LOAD	UC1708	UC1710	UC1711
Propagation Delay	0	25	30	10
t(plh)	1.0 nF	25		15
input to 10% output	2.2 nF	25	30	20
	30 nF		30	
Raise time	0	25	20	12
t(tlh)	1.0 nF	30		25
10% to 90% rise	2.2 nF	40	25	40
	30 nF		85	
Propagation Delay	0	25	30	3
t(phl)	1.0 nF	25		5
input to 90% output	2.2 nF	25	30	
	30 nF		30	
Fall Time	0	25	15	7
t(thl)	1.0 nF	30		25
90% to 10% fall	2.2 nF	40	20	40
	30 nF		85	

TRANSITION PERFORMANCE

Using the table above, the driver output slew rates and average current delivered can be calculated. The figures can be compared to lower power op-amps or comparators to gain a perspective on the relative speed of these high performance drivers.

The UC1708 delivers output slew rates (dv/dt) in the order of 300 to 480 volts per microsecond, at average load currents of under one amp, depending on the load. The high speed UC1711 exhibits similar characteristics under loaded conditions, but can achieve a no load slew rate of over 1700 volts per microsecond - nearly 2 volts per nanosecond.

For higher power applications, the UC1710 "Miller Killer" will produce an average current of 4.5 amps AT slew rates of 150 volts per microsecond. With lighter loads it will deliver an average current of 1.5 amps at a slew rate of approximately 500 volts per microsecond. In most applications, the UC1710 will easily outperform "homebrew" discrete mosfet transistor totem pole drive techniques.

Each device in this new generation of MOSFET drivers is significantly more responsive than the earlier counterparts for a given application - whether it's higher speed (UC1711), higher peak current (UC1710) or a combination of both (UC1708).

DRIVER CONSIDERATIONS

As previously demonstrated, the ideal MOSFET gate drive IC is a unique blend of both high speed switching and high peak current capability. Initially, the high speed is required to bring the gate voltage from zero to the plateau, but the current is low. Once the plateau is intersected, the driver voltage is fairly constant, and the IC must switch modes. Instantly, the driver current snaps to its maximum as charge is injected to overcome the FET's Miller effects. Finally, a combination of both high slew rate and high current is needed to complete the gate drive cycle.

At turn-off this sequence is reversed, first demanding both high slew rate and high current simultaneously. This is followed by the plateau region which is limited only by the maximum driver current. Finally, there is high speed discharge of the gate to zero volts.

Optimization of a driver for this type of application can be difficult. In general, the MOSFET driver IC output stage is designed to switch as fast as the manufacturer's process will allow.

CROSS CONDUCTION

There are numerous tradeoffs involved in the design of these drivers beyond the obvious choices of number of outputs and peak current capability. Cross-conduction is defined as the conduction of current through both of the totem pole transistors simultaneously from Vin to ground. It is an unproductive loss in the output stage which results in unnecessary heating of the driver and wasted power. Cross conduction is the result of turning one transistor ON before the opposing one is fully off, a compromise often necessary to minimize the input to output propagation delays.

An interesting observation is that cross-conduction is less of a concern with large capacitive loads (FETs) than with unloaded or lightly loaded driver outputs. Any capacitive load will reduce the slew of the output stage, slowing down its dv/dt. This causes a portion of the cross conduction current to flow from the load, rather than from the input supply through the driver's opposite output transistor. The power loss associated with a drivers inherent cross-conduction is unchanged with large capacitive loads, however it is not caused by a "shoot-through" of supply current.

DRIVER PERFORMANCE

There are a variety of applications for MOSFET drivers - each with its own unique set of speed and peak current requirements. Most general purpose drivers feature 1.5 amp peak totem-pole outputs which deliver rise and fall times of approximately 40 nanoseconds into 1 nanoFarad. Propagation delays are in the neighborhood of 40 to 50 nanoseconds, making these devices quite adaptable to numerous power supply and motor control applications. These specifications can be used for a comparison to those of a new series of higher speed and higher current devices, specifically, the UC1708, UC1710 and the UC1711 power MOSFET drivers. Each member in this group of "third" generation driver ICs features significant performance improvements over their predecessors with one parameter optimized for a specific set of applications.

MOSFET DRIVER IC FEATURE AND PERFORMANCE OVERVIEW
TABLE 2.

Feature	UC1708	UC1770	UC1711
Number of outputs	2	1	2
Peak output current (per output)	3A	6A	I.5 A
Noninverting input-output logic	YES	YES	
Inverting input-output logic		YES	YES
Maximum supply voltage Vcc	35v	20V	40V
Typical supply current Icc (1.)	16ma	30ma	17ma
Remote Enable	YES		
Shutdown Input	YES	YES (2)	
Seperate grounds, signal and power	YES (3)	YES (3)	
Seperate Vin and Vc pins		YES (3)	
8 pin DIL package	YES	YES	YES
16 pin DIL package	YES	YES	YES
5 pin TO-220 package		YES	

Note 1. Typical Vc plus Vcc current measured at 200KHZ, 50% duty cycle and no load
Note 2. Using the device's other input
Note 3. Package dependent

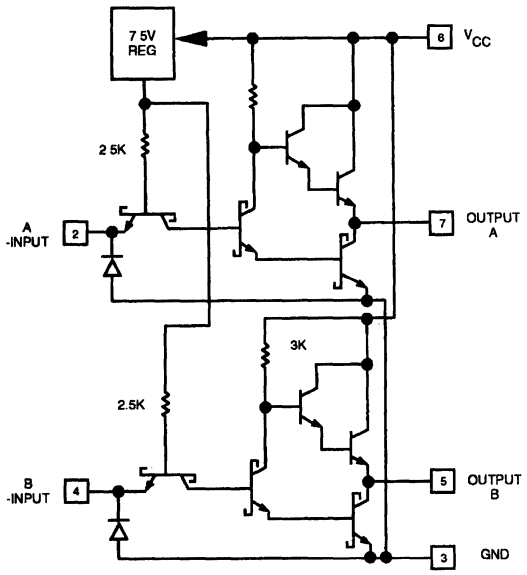
PROPAGATION DELAYS

The power supply industry's trend towards higher power densities has thrust switching frequencies well beyond one megaHertz in many low to medium power systems. With a one microsecond total conversion period, or less, the FET switching transitions should be in the order of low tens of nanoseconds to yield high efficiency. Additionally, the propagation delays from the driver input to output should be around ten nanoseconds for quick response.

UC1711

The UC1711 device features typical propagation delays of three and ten nanoseconds at no load, depending on the transition. Coupled with dual 1.5 amp peak totem-pole outputs, this device is optimized for high frequency FET drive applications. Its all NPN Schottky transistor construction is not only fast, but radiation tolerant as well.

UC1711 BLOCK DIAGRAM



GATE DRIVE POWER CONSIDERATIONS

Perhaps the most popular misconception in the power supply industry is that a FET gates require NO power from the auxiliary supply - that both turn-on and turn-off are miraculously power free. Another fallacy is that the driver consumes all the measured supply current, Icc, and none of it is used to transition the gates. Obviously, both of these statements are false.

In reality, the power required by the gate itself can be quite substantial in high frequency applications. Calculation of this begins by listing the specified total gate charge for the FET device, Qg.

The gate power utilized in charging and discharging a capacitor at frequency "F" is:

P(cap) = C * V^2 * F

Substituting the gate charge for capacitance multiplied by voltage (Q=C*V) in this equation results in:

P(gate) = Qg * V * F

The gate power required verses FET size and switching frequencies is tabulated for some common applications in Table 3. Table 4. transforms this power into driver input current at a nominal 12 volt bias.

GATE POWER (mW) VS. SWITCHING FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	10	18	28	36	46	90	136	180
SIZE 2	16	30	46	60	76	153	226	300
SIZE 3	28	54	82	108	136	275	406	504
SIZE 4	48	96	144	192	240	480	720	960
SIZE 5	100	200	300	400	550	1W	1.5W	2W
SIZE 6	144	288	432	576	720	1.4W	2W	>2w

Table 3.

DC SUPPLY CURRENT (mA) VS. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1 MEG
SIZE 1	1	1	2	4	5	6	10	12
SIZE 2	1	2	4	5	6	10	16	20
SIZE 3	2	4	6	8	10	16	26	36
SIZE 4	4	8	10	12	16	32	48	64
SIZE 5	8	14	20	26	32	66	100	130
SIZE 6	10	20	28	38	48	96	144	190

Table 4.

The driver output stage can be modelled as a resistance to the respective auxiliary supply rail driving an ideal FET capacitor. All of the power used to charge and discharge the MOSFET gate capacitor is completely transferred into heat by the driver. This gate power loss adds to the driver's own power loss - resulting in a net driver power dissipation equal to it's input voltage, Vcc, multiplied by the sum of the gate and driver currents, Ig + Icc. This can be calculated or determined empirically by measuring the driver DC input voltage and current.

THERMAL CONSIDERATIONS

Proper IC package selection and/or device heatsinking is the only method available to insure a safe operating junction temperature, tj. All IC's are specified and graded for various junction temperature ranges, and priced accordingly. As a precaution, it should be noted that using a device outside its tested temperature range can result in poor performance, parameters which run outside their specifications, and quite possibly - no operation at all.

JUNCTION TEMPERATURE

The junction temperature of the driver IC is obtained by first calculating the device's thermal rise above the ambient temperature. This is obtained by multiplying the average input power (Vin*Iin) by the device's thermal impedance to air, theta JA (Oja). This term is then added to the ambient temperature to yield the resulting junction temperature, Tj.

If the driver is thermally attached to a heatsink or "cold plate", then the thermal impedance from the device junction to it's package case, theta JC (Ojc), is used to determine the thermal rise. Likewise, this thermal rise is added to the heatsink temperature to determine the junction temperature. In either case, the maximum junction temperature (tj(max)) should be determined and checked against the device's absolute maximum specification.

Average supply currents for each of the three drivers of interest varies primarily with the switching frequency. Rather than listing each driver independently, an rough approximation of 25 milliamps will be used as the driver current, regardless of the specific device utilized and switching frequency. In addition, a typical supply voltage of 12 volts results in a power dissipation by the driver itself of 300 milliwatts.

The calculated gate power of Table 5. has been added to the estimated 300mW of device power to formulate Table 6. - the driver total power dissipation. This is of particular interest in selecting a driver package (8 pin, TO-220, etc.) and heat sink determination for a specific maximum junction temperature, or rise. Typical junction temperature rises vs. frequency and FET size for a IC package, and recommendations are shown in table 7.

AVERAGE POWER DISSIPATION (mW) VS. FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	310	318	328	336	346	390	436	480
SIZE 2	316	330	346	360	376	452	526	600
SIZE 3	328	354	382	408	436	570	706	840
SIZE 4	348	396	444	492	540	780	1.0W	1.3w
SIZE 5	400	500	600	700	800	900	1.7W	2.4W
SIZE 6	444	588	732	876	1.0W	1.7W	2.5W	3.1w

Table 5.

PACKAGE RECOMMENDATIONS

For P(diss) = or < 500mW
A: 8 pin DIL, <40 C rise
B: 8 pin DIL, <45 C rise
C: 8 pin DIL, <50 C rise

For P(diss) = or > 500mW (using heatsink)
D: 8 pin DIL, <40 C rise
E: 8 pin DIL, <50 C rise

For P(diss) > 500mW
F: TO-220 recommended

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1 MEG
SIZE 1	A	A	B	B	B	C	D	D
SIZE 2	A	B	B	B	C	D	D	D
SIZE 3	B	B	C	D	D	D	E	F
SIZE 4	B	C	D	D	D	F	F	F
SIZE 5	C	D	D	E	F	F	F	F
SIZE 6	D	D	E	F	F	F	F	F

Table 6.

HIGH POWER APPLICATIONS

Most high power applications require the use of "monster" MOSFETs or several large FETs in parallel for each switch. Generally, these are low to medium frequency applications (less than 200kHz) where obtaining a low Rds(on) is of primary concern to minimize the DC switch loss. It is not uncommon to find two, three and even four large devices used in parallel, although some of these combinations are unlikely from a cost versus performance standpoint.

Table seven displays the individual FET device characteristics and several popular parallel arrangements. Listed in descending order is Rds(on) at room temperature and the total gate charge required. This will ultimately be used to determine the gate drive current in Table 8., total power dissipation in Table 9., and driver IC recommendation in Table 10 for various applications.

PARALLELED MOSFET CHARACTERISTICS - TABLE 7.

MOSFET ARRANGEMENT	Rds(on) effective	Qg(nC) total	MOSFET ARRANGEMENT	Rds(on) effective	Qg(nC) total
1 X SIZE 4	0.85	63	2 X SIZE 5	0.200	260
1 X SIZE 5	0.40	130	2 X SIZE 6	0.135	380
1X SIZE 6	0.27	190	3 X SIZE 5 (1)	0.133	390
2 X SIZE 4 (1)	0.425	126	4 X SIZE 5 (1)	0.100	520
3XSIZE4(1)	0.283	189	3 X SIZE 6 (2)	0.090	570
4 X SIZE 4 (1)	0.213	252	4 X SIZE 6 (2)	0.068	760

1. Consider another selection 2. Consider a "Monster" FET

AVERAGE SUPPLY CURRENT (mA) VS. FREQUENCY AND FET SELECTION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz)					
		25	50	75	100	150	200
2 X SIZE 5	200	31	39	45	51	65	77
2 X SIZE 6	135	35	45	53	63	83	101
3 X SIZE 6	90	39	53	69	73	91	139
4 X SIZE 6	68	45	63	82	101	139	177

*Includes 25mA of driver supply current

Table 8

POWER DISSIPATION (mW) VS. FREQUENCY AND APPLICATION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	372	468	540	612	780	924
2 X SIZE 6	135	420	540	636	756	1.0W	1.2W
3 X SIZE 6	90	468	636	828	876	1.1W	1.7W
4 X SIZE 6	68	540	756	984	1.2W	1.7W	2.1W

* Includes **300mW** of driver dissipation

Table 9.

DRIVER IC AND PACKAGE SELECTION GUIDE

Selection Guide for < 50 C rise

A: 8 pin DIL or 20 pin PLCC
B: 8 pin DIL with heatsink. or TO-220.
C: TO-220 with heatsink

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	A	B	C	C	C	C
2 X SIZE 6	135	B	C	C	C	C	C
3 X SIZE 6	90	B	C	C	C	C	C
4 X SIZE 6	68	C	C	C	C	C	C

Table 10.

UC1710 DRIVER PERFORMANCE

Although capacitive in nature, the FET "Miller" effects and demands on the driver differ significantly than a true capacitor load as previously described. Table 11. shows the typical response of the UC1710 "Miller Killer" driving a single APT5025BN (size 6) device and paralleled MOSFET combinations for reference.

UC1710 RISE, FALL AND DELAY TIMES VS. LOADS

TEST CONDITIONS		Tp LH	Tt LH	Tp HL	Tt HL	Tp +Tt LH	Tt +TP HL
NO LOAD	VDS	28	12	36	12	40	50
ONE	0	28	26	38	30	54	68
APT5025	350	28	35	40	30	63	70
TWO	0	28	38	40	36	66	76
APT5025	350	28	48	42	38	76	80
THREE	0	28	48	42	48	76	90
APT5025	350	28	60	44	58	88	92

Table 11.

PERFORMANCE COMPARISONS

"HOMEBREW" TOTEM-POLES VS. INTEGRATED CIRCUIT DRIVERS

The prior lack of "off-the-shelf" high current or high speed drivers had prompted many to design their own gate drive circuits. Traditionally, an NPN-PNP emitter follower arrangement had been used in lower frequency applications as shown in Figure 7.

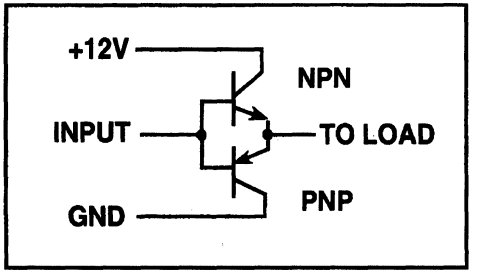


Figure 7

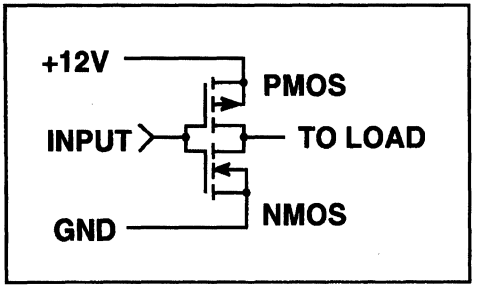


Figure 8

For higher speed applications, a P and N channel FET pair can be used as shown in figure 8. The circuit is configured with the P channel MOS as the upper side switch to simplify the auxiliary bias. Otherwise, a gate drive potential of ten volts above the auxiliary bias would required.

Unfortunately, this configuration has a few drawbacks First, it leads to an inverting logic flow from the driver input to its output, complicating matters especially during power-up and power-down sequences. Without a clever undervoltage lockout circuit the main power switch will tend to be ON as the auxiliary supply voltage is raised or lowered while the PWM is OFF.

Cross conduction of both FETs is unavoidable with this configuration due to the difference between the gate threshold voltages of each device. Both P and N channel devices are cross conducting while their input drive waveform is above Vgs(th) of the N device and below that of the P device. One technique to minimize the cross conduction peak current is to add some resistance between the FETs. While this does minimize the "shoot-through" current, it also limits the peak current available to the load. This somewhat defeats the purpose of using the MOSFETs in the first place to deliver high currents. The resistor serves an additional purpose of damping the gate drive oscillations during the transitions. In a practical application, two resistors can be used in the place of one with the center-tap connecting to the FET gate, or load as shown in figure 9.

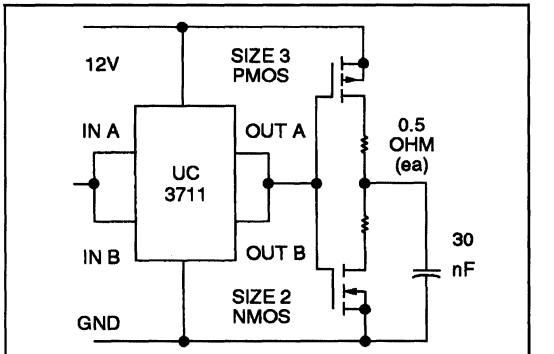
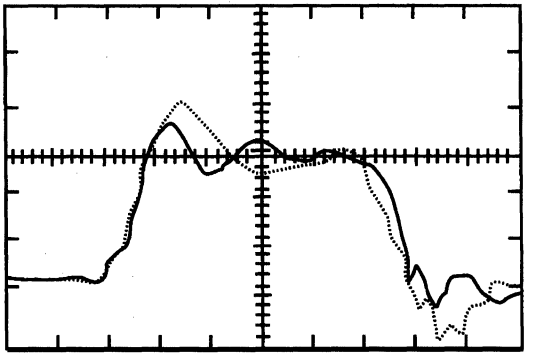


Figure 9

The performance of the circuit in figure 9 was evaluated and compared to that of the UC1710 driver into a 30 nanoFarad load. A size three P type FET and a size two N channel device were connected in series with two one-half ohm resistors to limit the shoot-through current. These FETs were driven from the UC1711 dual driver which can deliver 3 Amp peak gate drive currents for rapid transitions. The results of this test are shown in figure 10.

Driver Performance into 30nF load

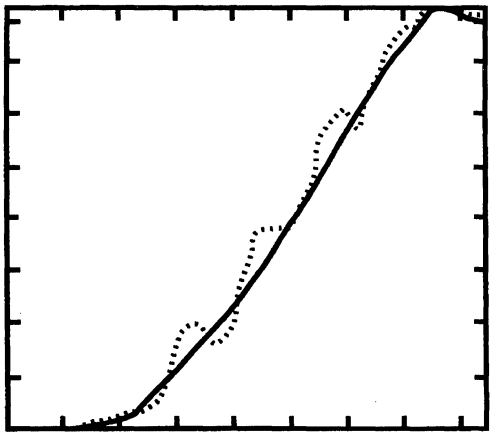


Lines: solid=UC3710, dashed=discrete
Figure 10. - VERT: 5V/DIV: HORIZ: 50 nS/DIV

The test results indicate very similar performance into this load from either technique. Obviously, the "homebrew" approach utilizes a total of three devices in comparison to a single UC1710 driver to obtain essentially the same high speed performance. Additionally, the cost of the P channel FET alone may exceed the price of the UC1710 device, not to mention the difference in PC board real estate. As a final note, the discrete FET approach required over 10 milliamps more supply current than the single UC1710 driver or a increase in supply current of twenty percent. Results of this test shown in figures 11 and 12.

RISE AND FALL TRANSITION PERFORMANCE INTO 30 nF

RISE TIMES (Fig 11.)



FALL TIMES (Fig 12.)

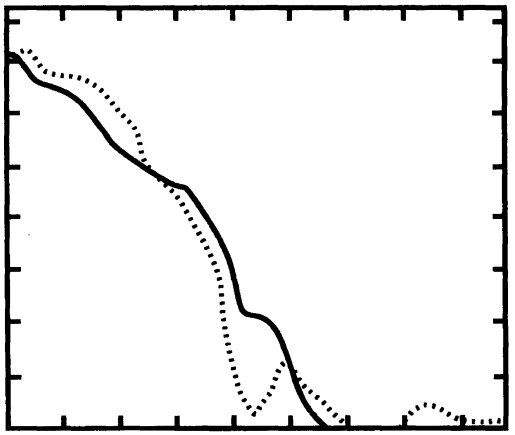


PHOTO SCALES (BOTH): VERT=2V/DIV, HORIZ=10 nS/DIV
LINES: SOLID = UC3710; DASHED = DISCRETE CIRCUIT OF FIGURE 9.

POWER DEVICES

IGBTs and MCTs: While existing generations of power MOSFETs continue to be enchanced for lower RDS(on) and faster recovery internal diodes, alternative new devices have also been introduced. Among the most popular, and viable for high voltage high power applications are IGBTs (Insulated Gate Bipolar transistors) and MCTs (MOS Controlled Thyristors). Although frequently drawn as an NPN structure, the IGBT actually resembles a PNP bipolar transistor with an internal MOS device to control the base drive. Indicative by its description, the MCT is essentially an SCR structure also utilitzing a MOS drive stage. Both devices offer significant cost advantages over MOSFETs for a given power capability.

MOSFET, IGBT and MCT Gate Drives: There are numerous reasons for driving the MOSFET gate to a negative potential during the device's off state. Degradation of the gate turn-on threshold over time and especially following high levels of irradiation are amongst the most common. However, with IGBTs, the important concern is the ability to keep the device off following turn-off with a high drain current flowing. On larger IGBT's with ratings up to 300 Amps, inductive effects caused by the device's package alone can "kick" the effective gate-to-emitter voltage positive by several Volts at the die - even with the gate shorted to the emitter at the package terminals Actually, this is the result of the high current flowing in the emitter lead (package) inductance which can less than 1nH. The corresponding voltage drop changes polarity at turn off, thus pulling the emitter below the gate, or ground. If high enough, a fast turn off will be followed by a parasitic turn-on of the

switch, and potential destruction of the semiconductor. Applying the correct amplitude of negative gate voltage can insure proper operation under these high current turn-off conditions. Also, the negative bias protects against turn-on from high dv/dt related changes that could couple into the gate through the "Miller" capacitance.

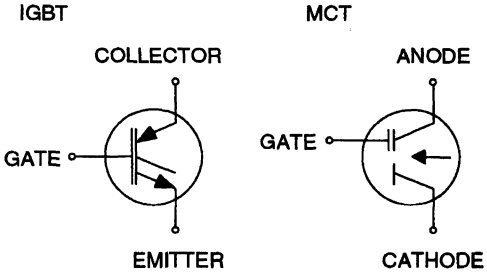


Figure 13 - IGBT and MCT Diagrams

Unlike power MOSFET switches, IGBT transconductance continues to increase with gate voltage. While most MOSFET devices peak with about 10 to 12 Volts at the gate, IGBT performance steadily improves up to the suggested 16 Volt maximum gate voltage. Typically, most IGBT manufacturers recommend a negative drive voltage between -5 and -15V. Generally, it is most convenient to derive a negative voltage equal in amplitude to the positive supply rail, and ±15V is common.

The gate charge required by an IGBT (for a given voltage and current rating) is noticeably less than that of a MOSFET. Part of this is due to the better utilization of silicon which allows the IGBT die to be considerably smaller than its FET counterpart. Additionally, the IGBT (being a bipolar transistor) does not suffer from the severe "Miller" effects of the MOS devices, easing the drive requirements in a given application. However, because of their advantages, most available IGBTs have fairly high gate charge demands - simply because of their greater power handling capability.

In contrast, MCTs (MOS Controlled Thyristors) exhibit the highest silicon utilization level among power switching devices. While relatively new to the market, these devices are quickly gaining acceptance in very high power (above several kilowatts) applications because of their high voltage (1000V) and high current (to 1000A) capability. Recently introduced parts boast maximum ratings to one megawatt, ideal for large industrial motor drives and high power distribution-even at the substation level. These devices are essentially MOS controlled SCRs and are intended for low frequency switchmode conversion. They will most likely replace high power discrete transistors, Darlingtons and SCRs because of their higher efficiency and lower cost.

Gate Charge and Effective Capacitance with Negative Bias: While several MOSFET and IGBT manufacturers recommend negative gate voltages in the device's off state, few publish any curves or information about gate charge characteristics when the gate is below zero Volts. This complicates the gate drive circuit design as each IGBT, MOSFET or MCT switch must be evaluated by the user over the ranges of operation conditions. A test fixture as shown in Figure 14 can be used to provide empirical generalizations for devices of interest. A switched constant current source/sink has been configured using a simple dual op-amp to drive a "constant" 1mA at the device under test (DUT). Gate voltage versus time can be monitored which provides the exact gate charge requirements for a given device. Any application specific requirements can also be accommodated by modifying the test circuit with external circuitry.

Negative Gate Charge - Empirical Data: Several MOSFET, IGBT and MCT gate charge measurements were taken to establish the general characteristics with negative gate charge and effective capacitance during this third quadrant operation was calculated and compared to of the first quadrant specifications from the manufacturers data sheets. Figure 15 demonstrates the general relationships of gate charges for comparison.

Both the IGBT and MCT have similar negative bias gate charge requirements as with an applied positive bias. The MOSFET, however, exhibits a slightly reduced gate charge in its negative bias region, somewhere between 70 and 75 percent of its positive bias charge. The MOSFET's more significant "Miller" effect in the first quadrant is responsible for this since the higher effective capacitance during the plateau region does not occur with negative bias.

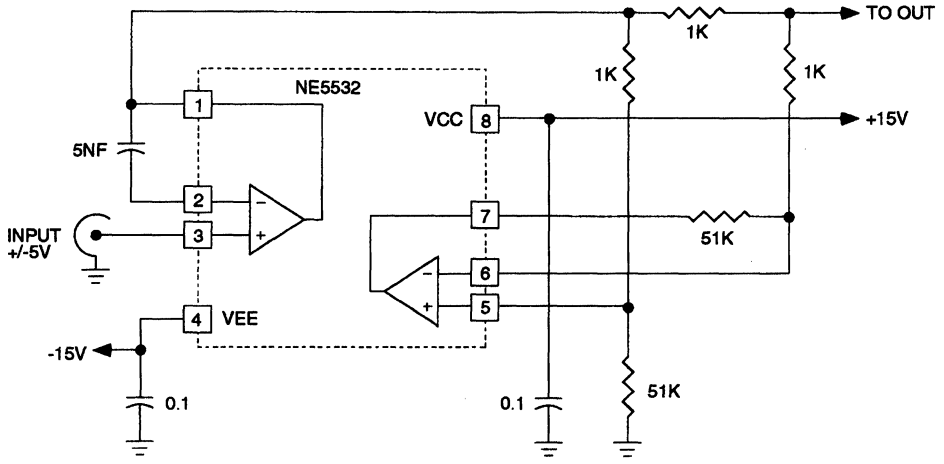


Figure 14 - Gate Charge Test Circuit

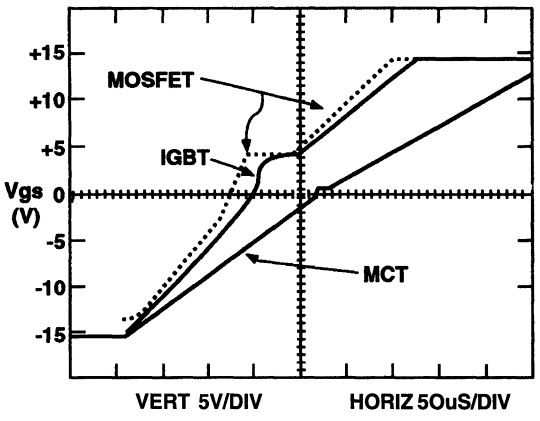


Figure 15 - Gate Charge Comparison Low to High Transition

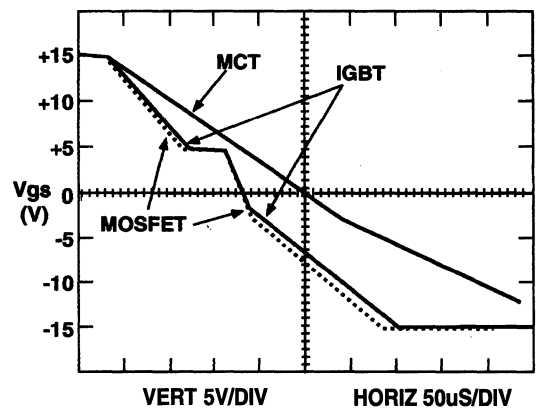


Figure 16 - Gate Drive Comparison High to Low Transition

Total Gate Power - Negative Drive Voltage Applications: All of the previously presented gate power equations still apply, however they must be modified to include the additional charge requirements of the negative supply voltage. For the sake of simplicity, a multiplication factor can be used for recalculation of the exact figures. When identical amplitudes of positive and negative supply voltages are used, for example ±15V, then the gate power utilized can be simply multiplied by a factor of two. This completes the process for the IGBTs and MCTs. The total MOSFET gate charge, on the other hand, should only be multiplied by a factor of 1.7 to 1.75 to accommodate the reduced negative bias demands. Additionally, if a negative supply voltage different than the positive rail voltage is used, for example +15 and -5, then the scaling factor must be adjusted accordingly. In this case, the new total gate power would be 1+ (-5/-15) or 1.33 times the initial 0-15V gate power for IGBTs and MCTs. The negative drive voltage scaling factor (-5/-15) would be multiplied by the 70 to 75% index if a MOSFET were used instead of an IGBT or MCT. This would result in a 1.23 to 1.25 times net increase over the initial (0-15V) gate power demand.

SUMMARY

The need for higher speed and higher current FET driver ICs has become increasingly apparent as power conversion switching frequencies are pushed towards and beyond one megaHertz. Likewise, the quest for higher overall efficiencies has resulted in creation of large, even "monster" size MOSFET geometries. These industry trends have stimulated the development of innovative MOSFET driver ICs - ones which would significantly outperform any of their predecessors, including discrete versions.

A new generation of high speed and high current MOSFET drivers has been presented. Each optimized for a unique blend of these attributes, the UC1708, UC1710 and the UC1711 devices successfully conquer the challenges of obtaining rapid transitions in MOSFET gate drive circuits.

REFERENCES

UNITRODE Application Note U-118, "New Driver IC's Optimize High Speed Power MOSFET Switching Characteristics", UNITRODE LINEAR IC DATA-BOOK, IC 600

INTERNATIONAL RECTIFIER Application Notes AN-937, AN-947 and Datasheets, I.R. HEXFET Power MOSFET Designers Manual HDB-4

ADVANCED POWER TECHNOLOGY Databook 1989

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220
UC1706/3706	Dual High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Conversion (1706Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible	16 Pin DIL "Batwing"
UC1707/3707	Dual Uncommitted High Current MOSFET Compatible Output Driver	• Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25n Sec Rise and Fall Times • 25n Sec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8-Pin DIL 16-Pin DIL
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8-Pin DIL
UC1710/3710	High CurrentSpeed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8-Pin DIL 5-Pin TO-220
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 15nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8-Pin DIL
UC3724 UC3725 (PAIR)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600kHz Carrier Capability • Local Current Limiting Feature	8-Pin DIL (Pair)

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Motion Control Products

Abstract

Recent advances in the design of Insulated Gate Bipolar Transistors (IGBTs) have increased their capabilities to the point where they are replacing power MOSFETs as the switching device of choice for high voltage/high current power supply and motor drive systems. Although switching speeds of IGBTs are generally slower than those of power MOSFETs, devices are now available with similar gate drive requirements. At the same time, these devices retain the inherent superior conduction characteristics of bipolar transistors. A new integrated circuit pair, the UC3726/UC3727, provides a cost-effective way to drive IGBTs in "high-side" and isolated switching applications. This application note describes the operation of this chip pair, as well as the unique problems associated with driving IGBTs. Many of the concepts presented here are similar to those presented in Unitrode Application Note U-127, written by John O'Connor, which describes the UC3724/UC3725 power MOSFET driver pair. This application note replaces Unitrode Application Note U-143 due to specification changes on the UC3727.

INTRODUCTION

IGBT OPERATION AND APPLICATIONS

While power MOSFETs have many desirable features such as high peak current capability, wide safe operating area (SOA), and ruggedness, they do have some inherent disadvantages. Among these are conduction characteristics that are strongly dependent on temperature, voltage rating and die size. Furthermore, the conduction characteristics of power MOSFETs are largely insensitive to gate voltage, and for large values of drain current, the drain to source voltage is primarily a linear function of the drain current. This effect severely limits the maximum current capability of MOSFETs since power loss is a squared function of drain current ($P_L = R_{DS} \bullet (I_D)^2$).

IGBTs, on the other hand, function more like bipolar transistors than MOSFETs. The IGBT equivalent circuit consists of a PNP transistor driven by a low voltage MOSFET in a pseudo-Darlington configuration. Since the voltage drop across the IGBT is the sum of the voltage drop across the P-N junction and the voltage drop across the driving MOSFET, the total voltage drop across the IGBT can never go below a diode drop. This leads to greater power dissipation at low current levels than for a MOSFET. However, this disadvantage is greatly offset by the fact that the conduction characteristics of IGBTs increase with increasing gate voltage. An increase in gate voltage leads to an increase in channel current for the driving MOSFET. This in turn leads to a reduction in voltage drop across the PNP. Furthermore, since the output PNP behaves largely like a bipolar transistor, voltage drop is not a linear function of collector current, which leads to much lower power dissipation at high current levels. Because of these superior characteristics, IGBTs can operate at much higher current levels than power MOSFETs of the same die size.

OVERVIEW OF IGBT DRIVE REQUIREMENTS AND PROBLEM AREAS

The conduction characteristics of an IGBT are similar to those of an N-channel MOSFET in that a positive gate-to-emitter voltage is required for conduction. This characteristic leads to the problem of gate biasing in "high-side" drive applications. Since the gate must be biased above the high voltage input, high side drive requirements can lead to costly and complex gate circuits, as the gate must sometimes be biased hundreds of volts above system ground.

In addition to the biasing problem, other gate drive requirements include low drive impedance to reduce switching losses, as well as sufficient current to charge the gate fast enough to achieve the desired switching time. The charge current requirement is derived from the total gate charge (Q_G) as specified on the IGBT data sheet. Additionally, since the combination of high voltage and relatively fast switching speed results in both high dv/dt and di/dt, the gate is usually biased with a negative voltage during turn off to prevent transient turn on.

This requirement results in added complexity for the gate drive circuitry. Finally some method must be implemented to protect the IGBT and/or other drive circuitry from damage during over current faults.

Unitrode Application Note U-127 mentions several common approaches to solving the high side driver problem. Among the common techniques used are floating power supplies for the driver circuitry, charge pump circuits, high voltage driver ICs, and optocoupler isolated driver circuits. Each of these techniques have limitations, and those limitations are discussed in detail in U-127.

UC3726/UC3727 DRIVER PAIR

The UC3726/UC3727 IC pair provides an elegant, yet compact and cost-effective solution to the problem of driving IGBTs in high side and isolated applications. The chip pair is similar to the UC3724/UC3725 chip pair, except optimized for the unique problems associated with driving IGBTs. Figure 1 shows the basic circuit configuration for the UC3726/UC3727 circuit pair. In addition to the IC pair, a few passive components and a pulse transformer are required to complete the circuit. Also, an optocoupler can be used to provide fault information to the UC3726 if it is desired. The optocoupler can be eliminated and fault protection still provided by the UC3727 if it is not required to pass fault information back to the system. This feature is explained in detail in the fault section of this application note.

The UC3726 transmitter generates a carrier signal that utilizes a unique duty cycle modulation technique to transmit both command signal and power to the UC3727. Operating the carrier at high frequency, up to 750kHz, allows for minimum transformer cost and size. Since the high voltage isolation is provided with a magnetic element instead of silicon, two low voltage ICs can be used. This leads to a very cost effective and simple solution to the high voltage gate drive problem.

The UC3727 comparator circuitry senses the transmitted duty cycle and decodes the ON/OFF gate drive command. A diode bridge rectifies the carrier input to provide power to the IC. The output gate drive signal is in phase with the command, and is guaranteed to be 16V. Intermediate high drive or clamp levels can be programmed for various periods of time to limit surge current at turn on, and during short term fault conditions. A bipolar voltage supply is also provided to supply negative gate drive to insure that the IGBT remains off in the presence of high common mode slew rates.

UC3726 DRIVE TRANSMITTER

Figure 2 shows the block diagram for the UC3726 drive transmitter IC. The major components of the circuit include two tri-level output drivers with zero current sense detectors and control logic, a bias voltage generator with undervoltage lockout, a retriggerable one shot, a TTL compatible input with hysteresis, as well as fault sense circuitry and control logic.

The circuit operates by using a unique duty cycle modulation technique to simultaneously pass ON/OFF command information and power to the UC3727 isolated IGBT high side driver. This technique was originally developed for the UC3724/UC3725 high side MOSFET driver pair. Application

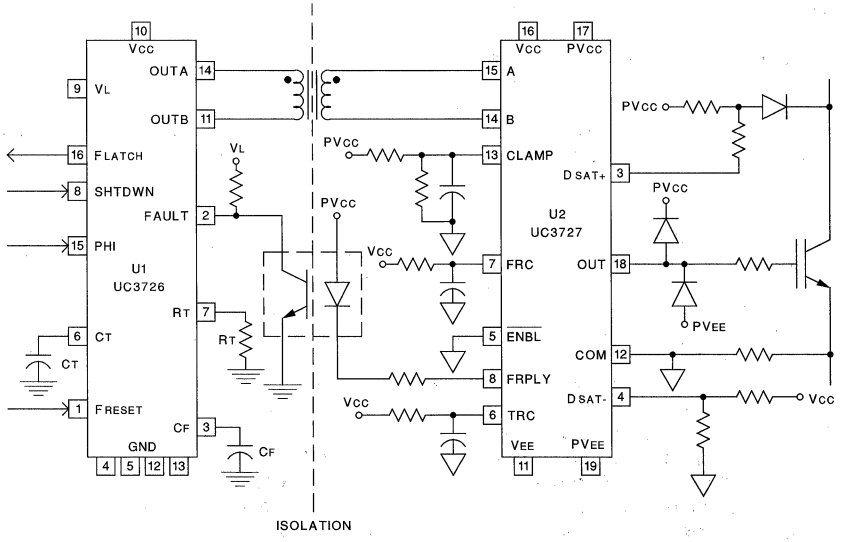

Figure 1. UC3726/UC3727 Circuit Pair

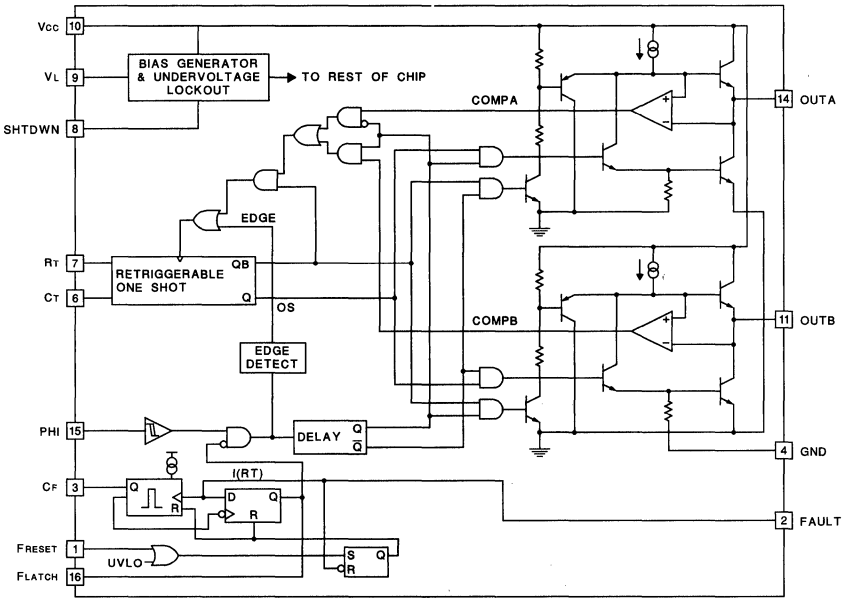

Figure 2. Drive Transmitter IC

Note U-127 describes the operation of that chip pair, and many of the concepts are similar. Specific differences primarily relate to waveform timing.

CARRIER FREQUENCY/TIMING/OUTPUT DRIVES/INPUT COMMAND

By choosing a high frequency carrier, cost efficiency can be maximized. The carrier frequency uses both a one shot pulse width and the pulse transformer reset time to set the overall period. The one shot pulse width is set by the timing resistor (R_T) and capacitor (C_T). During the one shot pulse time C_T, along with its parallel parasitic capacitance, is charged with a constant current determined by R_T and the logic voltage V_L:

1) $Ict = V_L/4R_T$

For this and all other equations in this applications note, all resistors are in ohms, all capacitors are in farads, and time is in seconds. The parasitic capacitance of approximately 50pF adds to C_T to form the total capacitance C_{TOT}. This capacitance charges from its initial value of 0.22 • V_L until it reaches the threshold voltage of 0.5 • V_L, at which time the one-shot pulse terminates. Using the current/voltage relationship for a capacitor of I=C(dv/dt) yields the pulse width time:

2) $T_{PW} = (C_{TOT} • (V_L)(0.5\text{-}0.22))/Ict = (C_{TOT} • 0.25V_L • 4R_T)/V_L = R_T • C_{TOT} • 1.1$

Notice that V_L does not appear in the final equation for T_{PW} , and therefore the tolerance on V_L does not affect the one shot period. During the one shot period "full" output voltage is applied across the primary of the pulse transformer, with one output held at VCC-2.0V, and the other output held at 0.3V. During this time, transformer magnetizing current rises linearly at a rate determined by the transformer inductance and applied voltage:

3) $di/dt = (V_A\text{-}V_B)/L_{pri}$

At the end of the one shot period, the control logic reverses the polarity of the applied voltage. During this time, one output is held at VCC • 0.6, and the other output is held at VCC + 0.4V. The result is a "half" voltage applied across the transformer primary which is opposite in polarity to the "full" voltage, and the core is reset. The magnetizing current decreases at a linear rate which is half of the rising rate. The outputs are held in this state until the current sense detectors determine that the current in the transformer has reached zero. At that point, the one-shot is retriggered, and the cycle repeats. Since the reset rate is half the energizing rate, the reset time is twice as long as the energizing time. The overall period for the carrier frequency is therefore:

4) $T_{CF} = 3 • T_{PW}$

Power is transferred to the UC3727 only during the one shot period. During this time the primary current is the sum of the magnetizing current and the load current. Since no power is transferred during the reset period, the primary current is composed of only demagnetizing current during this time. By switching when the current in the primary reaches

zero, the UC3726 assures that the core is reset, and there is no danger of saturation.

Figure 3 shows steady state waveforms for a continuous logic low input command. At time t0 the one shot pulse begins, and the voltage across CT charges until it reaches the threshold at time t1. The magnetizing current in the primary builds up linearly during this time. At t1 the one shot period ends, and the primary current begins decreasing. At time t2 zero current is reached and detectors retrigger the one shot, initiating the next one shot cycle. The waveforms for VA and VB reflect the half and full voltage concepts described previously.

The downward slope on VCT is the result of an internal timing circuit which provides a blanking interval which will not allow the output drivers to switch states while the inductor current is decreasing until a time period equal to the energizing period has expired. This protection feature is provided to prevent switching transients from triggering a state change on the output drivers prematurely.

If a continuous high input is commanded, the waveforms for VA and VB are interchanged, and the magnetizing current is inverted. The UC3727 determines command information by sensing the polarity of the full voltage at the transformer secondary.

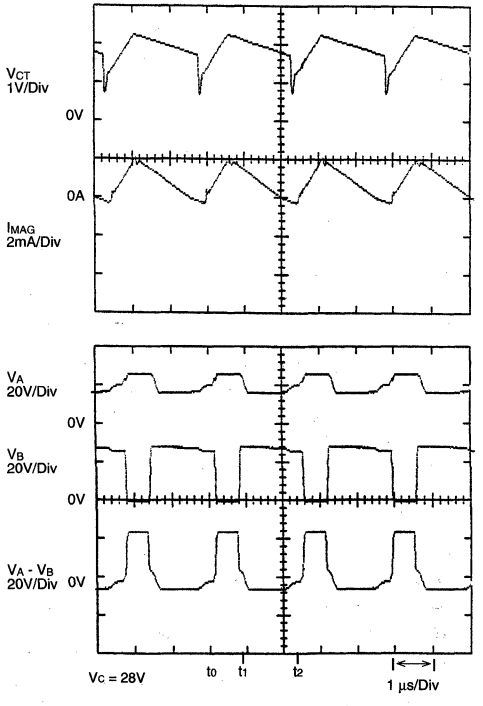

Figure 3. Steady State Waveforms Continuous Logic Low Input

This is described in detail later in this application note.

When a command transition occurs, the existing oscillator cycle is terminated, and a new cycle is started by applying full voltage in the opposite polarity. There is no danger of saturating the core, because the current must fall to zero before a new one shot trigger can occur. Newly incorporated circuitry prevents output jitter during a command transition by assuring equal propagation delay to the output regardless of the point in the cycle that the transition occurs.

FAULT/FAULT TIMING/FAULT RESET

The UC3726 contains special circuitry to prevent drive information from being transmitted during fault conditions. The FAULT input to the chip is designed to interface with the UC3727 through an optocoupler. At power up the UC3726 FAULT pin is pulled high through an external resistor, and the fault logic is reset by the UVLO circuitry.

Once its UVLO level is exceeded, the UC3727 drives the FAULT pin low, and the fault logic is enabled. After this point, the UC3727 will keep the FAULT pin low unless a fault is indicated. Special fault detection circuitry in the UC3727 detects overcurrent conditions (faults) and informs the UC3726 through the FAULT signal. To be recognized as a valid fault, the FAULT signal must remain high during the entire fault window. The timing for this window is set by CF and RT and is determined by the following equation:

5) $t_F = (C_F \bullet R_T) \bullet 2.1$

If a valid fault is recognized, the fault latch is set, and the outputs will remain in the logic low states until the FRESET signal (input to the UC3726) is toggled high. This signal should be powered up low, and remain low until a valid fault is recognized. Once the fault is cleared, the FRESET signal should be brought low again. The minimum pulse width on FRESET to guarantee a reset is 1µsec.

Figure 4 shows the waveforms for the FAULT circuitry signals for a valid fault. It should be noted that use of this function requires a "smart" system.

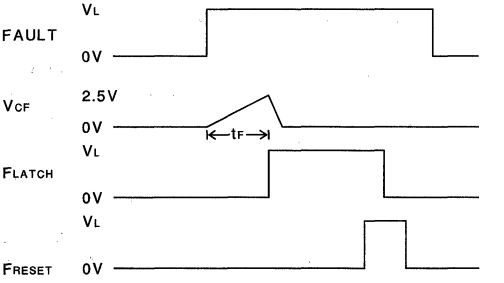

Figure 4. Fault Circuitry Signals

The fault latch must be reset in order for operation to continue once a valid fault is recognized. If the optocoupler used has a high level of output capacitance, it may be necessary to provide a reset pulse to the FRESET pin of the UC3726 after it has completed its power up sequence. Since a low to high transition on the FAULT pin indicates a valid fault, a slow rising waveform on this pin will result in a fault indication at power up. If this occurs, the output drive of the UC3726 will be latched off until the reset pulse is provided.

If this level of complexity is not desired or required, the FAULT input to the UC3726 can be permanently enabled by tying it low, allowing the UVLO circuitry to reset the fault latch. The UC3727 has additional fault protection circuitry that will protect the output IGBT independently, but the UC3726 will not be informed that a fault has occurred. Since the FAULT input to the UC3726 is tied low through a low impedance, the reset pulse after power up is not required for this case.

SHUTDOWN/UVLO/LOGIC VOLTAGE OPERATION

The UC3726 provides a shutdown pin (SHTDWN) which can be used to place the IC in a low power shutdown mode. By bringing this point high, the internal reference is disabled, and supply current is reduced to 2.5mA typical. Since the typical supply current when the chip is active is 20mA, the power savings are substantial. While in shutdown mode, both the A and B output drives are held low (ground). If an external logic supply is used, it must also be disabled for the shutdown feature to work.

The UC3726 also provides internal under voltage lockout (UVLO) circuitry. This feature will disable the internal reference, and disable the output drivers (hold at ground), if V_{CC} is below 6.5V. It should be noted, however, that V_{CC} must be held high enough to satisfy the UVLO feature of the UC3727. If the pulse transformer has a turns ratio of 1:1, V_{CC} must be held at 28V to guarantee proper operation of the UC3727. This requirement is derived from the maximum saturation drops of the UC3726, as well as the UVLO, rectifier drops, and V_{CC} specifications of the UC3727. For operation with V_{CC} less than 28V, the turns ratio of the transformer must be adjusted to provide enough voltage to the UC3727. This requirement is explained further in the output drive section of this application note, which provides detail on pulse transformer selection and design.

The UC3726 also brings out the logic voltage supply to a separate pin. If an external logic voltage supply is used, I_{CC} is reduced from 22mA typical to 12mA typical. Regardless of whether an external logic supply is used or not, this pin must be bypassed to ground with a high quality ceramic capacitor of at least 0.1µF.

UC3727 ISOLATED HIGH SIDE IGBT DRIVER

Figure 5 shows the block diagram of the UC3727 high side IGBT driver IC. The major circuit components include a Schottky diode rectifier bridge, a differential sense comparator with hysteresis, a bias and reference generator including undervoltage lockout circuitry and thermal shutdown, a high current gate driver stage with a programmable clamp drive level, a negative gate drive voltage supply, and fault detection and shutdown circuitry. An enable input is also provided to allow for stand alone operation with external bipolar voltage supplies.

SIGNAL AND POWER INPUT/NEGATIVE POWER SUPPLY

As shown on Figure 5, the input stage to the UC3727 both rectifies the input signal to supply power to the IC, and demodulates the input signal to determine the polarity of the gate drive command. Because the rectifier bridge peak detects the input signal, power is only transferred to the storage capacitors during the "full" voltage portion of the duty cycle. This operating mode prevents the flow of any secondary current through the pulse transformer during the "half" voltage portion of the duty cycle. The primary current is therefore composed of only demagnetizing current during the reset or "half" voltage portion of the cycle. Since the waveform is switched based on zero current detection, the transformer core is completely reset each cycle.

When "full" voltage is applied, the external storage capacitors are charged through the rectifier bridge. The energy stored in these capacitors is used to power the UC3727 circuitry, and to provide instantaneous charge to the IGBT gate during turn on. A detailed description of proper capacitor selection is provided in the decoupling section of this application note.

An internal "GND" amplifier maintains a floating common 16.5V below V_{CC}. By referencing this common point to the emitter of the IGBT, the gate voltage can be driven to a negative voltage during turn off.

The internal hysteresis comparator of the UC3727 senses the polarity of the input command by determining the polarity of the "full" input voltage. The comparator threshold is only set or reset if the input voltage exceeds 0.95 • (V_{CC} - V_{EE}) or 0.95 • (V_{EE} - V_{CC}). The IGBT gate is turned on if the "full" voltage is positive with respect to common, and turned off if the "full" voltage is negative with respect to common. Note that this represents a logic

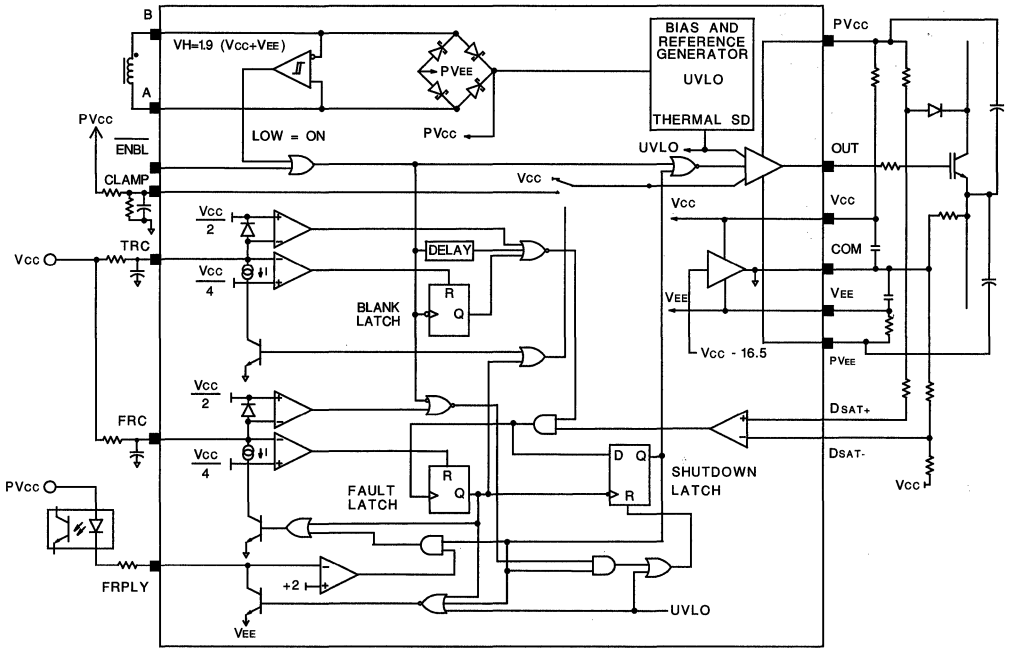

Figure 5. UC3727 High Side IGBT Driver IC

inversion to account for the logic inversion in the UC3726.

The UC3727 provides separate inputs for VCC, PVCC, VEE, and PVEE. By separating the output driver supplies (PVCC and PVEE) from the power supplies for the rest of the circuitry, better noise immunity can be achieved. The PVCC and PVEE inputs should be isolated from their respective low current supplies by 3.3Ω and bypassed to the IGBT emitter with 1.0µF capacitors as shown on Figure 5.

OUTPUT DRIVER STAGE

The output stage of the UC3727 consists of a high current, bipolar power amplifier. The peak output current of 4A provides the ability to drive IGBT gates requiring large amounts of gate charge. In order to provide a controlled or "soft" gate drive signal, the gate drive can be programmed for a two step turn on waveform. At turn on, the drive amplifier waveform will rise to a user defined clamp level for a user defined time duration. The benefits and uses of this clamp level are explained in further detail in the following section of this application note. After the time duration expires, the drive waveform will then rise to its maximum level (approximately 15V).

The common output of the UC3727 is designed to be referenced to the emitter of the IGBT to allow the gate to be driven negative during turn off. By regulating this common point to a fixed level below VCC, the remaining differential supply voltage (VCC - VEE) - (VCC - VCOM) can be used to generate the negative bias.

Under voltage lockout is also featured in the UC3727. Because VCOM is a regulated point below VCC, the differential input voltage VA - VB must exceed the maximum potential difference between VCC and VCOM, plus the UVLO level between VCOM and VEE, plus the diode drops of the rectifier bridge. In equation form this can be stated as:

6) $V_A - V_B \geq V_{CC} + V_{EEUVLO} + 2V_D$

The differential input voltage is supplied by the UC3726 through the pulse transformer (in most cases). Consideration must be given to Equation 6 when selecting a supply voltage for the UC3726, and during pulse transformer selection. If worst case specifications are considered, the differential input voltage must be greater than 25.3V to guarantee proper operation of the UC3727.

OUTPUT CLAMP/SOFT TURN ON

A common application of IGBTs involves driving clamped inductive loads. In this case, the maximum allowable reverse recovery current of the clamp diode can be a limiting factor. One way to limit the reverse recovery current is to provide a soft turn on to the IGBT gate. Since the conduction

of the IGBT channel is sensitive to gate voltage, the peak current through the channel can be limited by providing a clamp level during turn on. Unfortunately, this will result in greater switching losses. Considerable care must therefore be taken when programming the clamp level and time duration. Tradeoffs must be made at the system design level between reverse recovery current limitations and switching losses.

Referring to Figure 5, the clamp level is determined by a resistive divider between Vcc and common. The clamp level is approximately the voltage level at the clamp input pin. As the gate voltage rises, the gate drive signal is "caught" by the clamp circuit at the clamp level. Because a significant amount of charge is rerouted through the clamp circuit at this point, the clamp pin must be bypassed to common with a high quality capacitor of at least 0.1μF, and the DC impedance of the clamp network should be limited to approximately 10k ohms.

Also referring to Figure 5, the clamp time is set by the RC network at the TRC input to the UC3727. When a command is received to turn on the gate, the gate drive circuit rises to the clamp level, and the voltage at TRC is discharged by an internal current source. Once the threshold of Vcc/4 is reached, an internal comparator trips, and full gate voltage is applied. The clamp period is determined by:

$$7)\ Tp = R_{TRC} \bullet C_{TRC} \bullet ln\left(\frac{R_{TRC} - 7600}{R_{TRC} - 12400}\right)$$

This RC network also determines the blanking time for the desaturation comparator. The desaturation comparator is used to detect fault conditions which result in the IGBT coming out of saturation while the gate drive is high. Due to the turn on delay of the IGBT, this comparator must be ignored after a command transition to the on state until the IGBT transitions into saturation. The blanking time requirement is derived from the turn on and saturation characteristics of the IGBT.

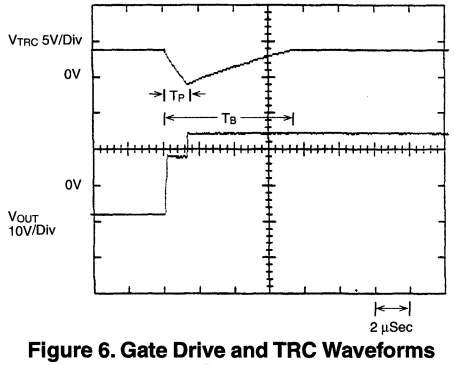

Figure 6. Gate Drive and TRC Waveforms Positive Gate Transition

Once the clamp time period has expired, the output driver increases the gate voltage to the fully on level. The voltage at TRC is then allowed to charge back to Vcc/2. The total time it takes to discharge and recharge the capacitor defines the blanking period and is determined by:

$$8)\ Tb = Tp + 0.4 \bullet R_{TRC}C_{TRC}$$

Because we have two equations and two unknowns, the clamp time and blanking time can be programmed independently. Figure 6 illustrates the gate drive waveform and the voltage at TRC during a positive gate drive transition.

FAULT/FAULT TIMING/DESATURATION AMPLIFIER

As described previously, IGBTs offer several advantages over power MOSFETs due to their superior conduction characteristics. They also exhibit several advantages over bipolar transistors and Darlingtons such as lower power dissipation and higher operating frequencies. Unfortunately, an IGBT that has been optimized for superior conduction and efficiency, is generally vulnerable to damage due to short circuits or faults. Because of their high conductivity, short circuit currents for IGBTs can be quite high, making them susceptible to damage due to excess power dissipation.

When building short circuit protection into an IGBT driver circuit, the response of the protection circuit must be fast enough to insure that the device is shut off before damage to the IGBT or any other part of the circuit occurs. At the same time, care must be taken to avoid nuisance triggering from short duration faults that do not result in any circuit damage. If the gate drive to the IGBT is shut off completely as soon as a fault is detected, the result may be an intolerable amount of nuisance shut downs. Therefore, it would be advantageous to program the allowable short circuit time as long as possible.

If the gate drive voltage is reduced when a fault is detected, the short circuit current can be reduced, and therefore the short circuit time can be stretched. However, reducing the gate voltage also increases the saturation voltage of the IGBT, which is undesirable for normal conduction. Therefore, the ideal short circuit protection technique will reduce the gate voltage only when a fault condition is detected, and keep the gate voltage at the reduced level for as long as possible, before shutting down the IGBT completely. In order for this technique to work effectively, the maximum short circuit time as a function of gate voltage must be known.

Referring again to Figure 5, the UC3727 provides a desaturation comparator designed to detect short circuit or fault conditions, and provide both short term and long term protection for the IGBT. The

DSAT+ input to the comparator is biased off to a DC level which is higher than the maximum saturation level of the IGBT plus one diode drop. During normal operation, the DSAT- input will be pulled down to the saturation voltage of the IGBT plus one diode drop. The blanking period discussed previously protects against false trips of the desaturation comparator while the IGBT is turning on.

If a fault occurs outside of the blanking interval, the gate drive will be reduced to the clamp level for a time period determined by the RC network at the FRC pin of the UC3727. The time period can be calculated by the following equation:

9) $Tf = R_{FRC} \bullet C_{FRC} \bullet ln((R - 7600)/(R - 12400))$

As soon as the fault is detected the FRPLY output of the UC3727 will go high. If the UC3726 is configured to accept this signal as an input, through an optocoupler or level shift network, its own fault timing circuitry will be activated.

If the desaturation event ends before the fault time has expired, the gate drive will be driven back to its maximum level, and FRPLY will go back low. In order to insure that the desaturation amplifier can accurately determine that a fault condition no longer exists, the DSAT- input level must be biased higher than the desaturation level of the IGBT with the reduced gate drive, plus a diode drop.

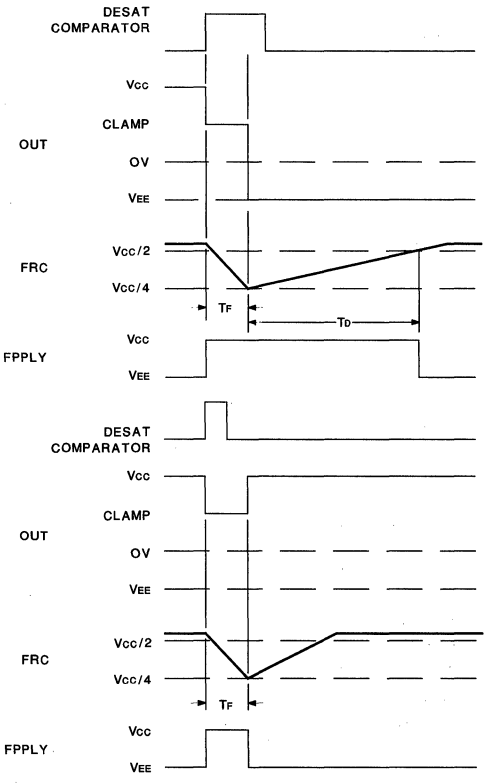

Figure 7. Fault Signal Waveforms

If the desaturation event does not end within the fault time, the output gate drive will be driven completely off, and the chip will not accept a command to drive the gate high until a delay period has expired. The equation for the delay period is determined by the same RC network as the fault time:

10) $Td = 0.4 \bullet R_{FRC} \bullet C_{FRC}$

Again, since there are two equations and two unknowns, the fault time and delay time can be programmed independently. FRPLY will remain high for the entire delay period. If the UC3726 is configured to accept FRPLY as an input, it will have the ability to prevent any command to turn on the gate from being transmitted until its fault latch has been reset. Figure 7 shows the waveforms for fault signals for both transient and long term faults.

ENABLE INPUT/STAND ALONE OPERATION

The UC3727 provides an active low enable input for stand alone operation. This input is useful for operating the chip as a high side driver with isolated power supplies. The enable input can also be used to control the chip for low side driver applications if external power supplies are available. If the UC3727 is not used in stand alone mode, i.e. it is driven by the UC3726, the enable input should be tied to common.

If $\overline{\text{ENBL}}$ is used as a command input, the B input should be tied to VCC, and the A input should be tied to VEE. Note the polarity change described previously. The output gate drive will be driven high when $\overline{\text{ENBL}}$ is held at the same potential as common, and the gate drive will held low when $\overline{\text{ENBL}}$ is tied to VCC. For low side driver applications $\overline{\text{ENBL}}$ can be controlled by a discrete transistor operating off of conventional logic. For high side driver applications, $\overline{\text{ENBL}}$ must be controlled by an optocoupler, or a discrete transistor operating off as a level shift network. Because the optocoupler or discrete transistor will function as an inverter in this case, the result will be positive logic to the output. Therefore, turning on the optocoupler or transistor will turn on the IGBT. Figure 8 shows a circuit diagram for using the $\overline{\text{ENBL}}$ input as a command input.

If external power supplies as used for grounded emitter low side operation, common should never be connected to system ground. This point is not designed to sink the large amounts of current flowing out of the emitter of the IGBT. Both the positive and negative supplies should by bypassed to common with capacitors, and the common output should be DC isolated from ground.

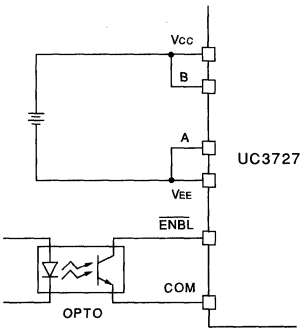

Figure 8. ENBL Used as Command Input

PRACTICAL DESIGN CONSIDERATIONS/EXAMPLE CIRCUIT

Figure 9 depicts a typical high side IGBT driver circuit. All of the features of the IC driver pair are utilized to provide maximum circuit protection and flexibility. This configuration might be used as a high side switch for a power supply, or it might form part of an H-bridge configuration for a motor driver. A resistive load is assumed in order to illustrate the high switching speeds of the driver pair. Real systems would likely require driving clamped inductive loads, and switching speed would be purposely slowed to protect external components such as clamp diodes. Component values for the support circuitry are chosen based on the specific requirements of the system. What follows is a step by step design procedure for a typical circuit.

PULSE TRANSFORMER DESIGN CONSIDERATIONS

Application note U-127 provides a detailed explanation of recommended transformer design criteria for the UC3724/UC3725 chip pair. Since the transformer design procedure is similar for the UC3726/UC3727 chip pair, the theory is not repeated in this application note. However, a transformer has been designed by Coilcraft (Q3868-A) specifically for use with the UC3726/UC3727 pair. This transformer has been optimized for operation at 400kHz, resulting in small size and low cost. Since the maximum switching frequency for the IGBT is 1/4 of the transformer frequency, the resulting 100kHz maximum IGBT frequency is near the typical maximum operating range of power IGBTs. The following calculations provide a brief overview of the design of the Q3868-A transformer:

Assuming a VC of 30V for the UC3726 and typical total saturation drops of 2.3V for the output drivers, the resulting voltage across the transformer winding will be 27.7V. Ignoring propagation delay, and choosing a peak magnetizing

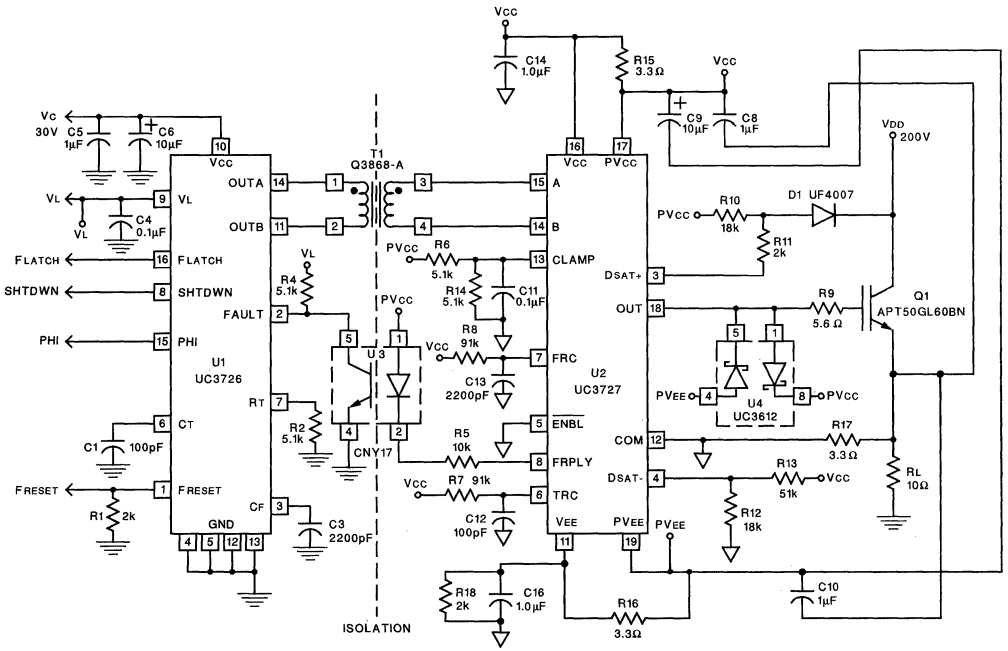

Figure 9. Typical High Side Driver Circuit

current of 35mA, the required primary inductance can be calculated using Equation 7 of U-127:

11) $L_{pri} = ((27.7V)(833ns))/0.035A = 659\mu H$

The 833ns represents 1/3 of the period of the 400kHz carrier, which is the pulse width time as defined by Equation 4 of this document:

12) $T_{PW} = 1/(3 \bullet 400kHz) = 833ns$

Using Equation 8 of U-127, and an initial value of A_L = 2000mH/1000 turns, an estimated number of turns is calculated:

13) $N_{TURNS} = ((659\mu H \bullet 10^9)/2000)^{1/2} = 18$ turns

From Equation 8 of U-127:

14) $A_e = ((27.7V)(833ns)(10^4)/((18\ turns)(0.05T)) = 0.256\ cm^2$

A Magnetics core, P-41206-TC was chosen with the following specifications:

A_L = 2820mH/1000 turns

A_e = 0.221 cm^2

V_e = 0.554 cm^3

Recalculating the number of turns yields:

15) $N_{TURNS} = ((659\mu H)(10^9)/2820)^{1/2} = 15.3$ turns, use 15 turns

The flux density of the transformer design is then checked using Equation 8 of U-127:

16) $delta\ B = ((27.7V)(833ns)(10^4)/((15\ turns)(0.221\ cm^3) = 0.069T$

To determine the core loss due to the magnetizing current, the core loss vs. flux density curve for the core is consulted:

At 400kHz and 0.069T, P_L = 400mW/cm^3

Therefore, the core loss can be calculated as:

17) $P_{CL} = (400mW/cm^3)(0.554\ cm^3) = 222mW$

The transformer is wound with AWG #30 KYNAR wire. In order to minimize leakage inductance, the primary and secondary windings are wound bifilar. The maximum DC resistance of the primary winding is 0.130 ohms, and therefore resistive losses due to magnetizing current are minimal. There will be additional resistive losses due to bias current for the UC3727 and gate drive current for the IGBT. For IGBTs with large gate charge requirements, these losses may become significant, and the transformer design must be adjusted accordingly.

In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator.

Once the transformer design has been completed, and an operating frequency has been chosen, the values for R_T and C_T can be selected. Since a wider selection of resistors is available than capacitors, we choose C_T = 100pf. We then use Equation 2 and a one shot pulse width of 833ns to determine R_T :

18) $R_T = (833ns)/((100pF + 50pF) \bullet 1.1) = 5.1k$

Referring to Figure 9, this results in R2 = 5.1k and C1= 100pF.

OUTPUT DRIVE CONSIDERATIONS/CLAMP LEVEL AND BLANKING TIME

In order to design the gate drive portion of the IGBT driver circuit, several criteria must be considered to balance what sometimes are conflicting requirements. The ideal situation would involve switching the IGBT as fast as possible to minimize switching losses. However, there will be cases when it is desirable to reduce the switching speed of the IGBT. An example case would be slowing down the turn on time to limit the reverse recovery current into the free wheel diode when driving a clamped inductive load. Another example might be reducing the turn on time in a half bridge configuration to prevent cross conduction.

In order to evaluate the drive requirements of the IGBT, the gate charge characteristics of the device are used. However, evaluating the gate charge does not lead to a good prediction of switching times as it does with power MOSFETs. The reason for this is the fact that IGBTs are minority carrier devices. This characteristics leads to slower switching times than power MOSFETs due to base charge storage. The turn off time is much slower than the turn on time, and is characterized by a "tail" in the current waveform. To predict switching times of IGBTs, the manufacturers data sheets must be consulted for turn on delay ($t_{d\ on}$), rise time (t_r), turn off delay ($t_{d\ off}$), and fall time t_f.

The drive circuitry should be designed so that additional delay is not introduced due to gate charge requirements. In the example shown in Figure 9, an APT50GL60BN IGBT is used (500V, 60A). The key timing specifications of this device are as follows:

Total Gate Charge (Q_g) = 110nC

Turn On Delay ($t_{d\ on}$) = 15ns

Rise Time (t_r) = 50ns

Turn Off Delay (t_d) = 55ns

Fall Time (t_f) = 350ns

The UC3727 output stage is a 4A peak driver. The time required to charge the gate is therefore:

19) $T_{CH} = 110nC/4A = 27.5ns$

Since this time is about half of the sum of the turn on delay time and the rise time, significantly reducing the drive current will slow down the turn on time of the device. However the fall time of the IGBT is much longer (350ns), and therefore gate drive current does not significantly affect the turn off time.

For the example circuit it is assumed that the fastest switching speed possible is desired. However, since the UC3727 is rated for 4A peak drive current, a gate resistor is used to limit the peak current. Taking into account rectifier and saturation drops, the maximum swing of the gate voltage is 20.5 volts. The gate resistor is therefore chosen by:

20) *R9 = 21.5V/4A = 5.1ohm, use 5.6ohm*

For circuits like half bridge amplifiers where cross conduction is a concern, a diode can be used with dual gate resistors to provide a higher gate impedance for turn on than for turn off, to provide cross conduction protection. An example of this technique is shown in the design example section of this application note.

For circuits where the collector of the IGBT is subjected to high dv/dt, the gate resistor must be sufficiently small to prevent unwanted gate turn on due to voltage drop across the gate resistor when current flows through the Miller capacitance in the presence of the high dv/dt. For high current IGBTs, emitter inductance can also cause transient turn on in the presence of high di/dt, by pulling the emitter node negative. These problems are partially mitigated by the negative gate bias of the gate drive in the off state, but the designer must be aware of the additional limitations in gate resistor selection if large values of gate resistors are desired.

For large IGBTs the power rating of the gate resistor must also be considered. In order to determine the average power dissipated by the gate resistor, energy supplied to the capacitor is determined by:

21) $E = (2)(1/2) \bullet C_{GATE} \bullet V^2 = (Q_{GATE}/V) \bullet V^2 = Q_{GATE} \bullet V$

The factor of 2 comes from the fact that the gate must be both charged and discharged by the gate drive circuit. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. If we assume that the gate drive signal is running at 15kHz, the average power dissipated in the gate drive circuit is:

22) $P_{AVG} = E/T = (Q_{GATE} \bullet V)/T = Q_{GATE} \bullet V \bullet F = (110nC)(20.5V)(15kHz) = 34mW$

Obviously for this example power dissipation in the gate drive circuit is not a problem. However, for IGBTs with higher gate charge requirements, and higher operating frequencies, the power dissipation can become significant, and must be taken into consideration. To select the power rating of the gate resistor, assuming that all of the power in the gate drive circuit is dissipated in the gate drive resistor will lead to a conservative gate resistor rating. If a power resistor is required, it should have low inductance. A wirewound resistor is not recommended for this application, but if one is used, it must be noninductively wound.

The output of the UC3727 should be protected against adverse affects due to voltage overshoot on the gate drive signal by clamping the output circuit to both V_{CC} and V_{EE} with Schottky diodes. This is done in the circuit shown in Figure 9 with a UC3612 dual Schottky diode. For a detailed explanation of this problem see Unitrode Application Note U-111.

Once the gate drive resistor has been selected, the clamp level, clamp time, and desaturation amplifier blanking time must be selected. Choosing the clamp level involves a trade off between the soft turn on requirements and the short circuit characteristics of the IGBT. Basically the soft turn on requirements are derived from the reverse recovery characteristics of the free wheel diode if the IGBT is driving a clamped inductive load. Since the conductivity of the IGBT is reduced for lower gate voltage, the maximum current that the free wheel diode sees during reverse recovery can be controlled.

Since this example assumes a resistive load, the short circuit characteristics of the IGBT will determine the clamp requirements. Unfortunately, the short circuit characteristics are not always well known. Considerable effort must expended to test the device and determine a safe clamp level and clamp time. Test data has suggested that for the IGBT used in this example, a reduction in gate voltage to 10V will allow for a maximum short circuit time of about 40µs with a V_{DD} of 200V. With full 15V gate drive, the short circuit time would be 5µs worst case. However, a secondary requirement of the clamp circuitry is that the protection circuitry must be able to recognize that the device is back in saturation if the fault goes away during the allowable fault period. For a gate drive voltage of 8V, the APT50GL60BN will remain in saturation at the peak normal current load of 20A. Therefore 8V is chosen as a conservative number for the clamp level.

Once the clamp level is known, the only other constraint is that the DC impedance must be limited to approximately 10k ohms. With that in mind, referring to Figure 9 we have:

23) *(16.5V)(R14 /(R6 + R14)) = 8V*

24) *R6 + R14 = 10k*

A solution of R6 = R14 = 5.1k will satisfy the design requirements. The clamp input is also bypassed to common with 0.1µF as discussed in the output clamp section of this application note.

As previously detailed, the clamp time on the rising edge of the gate drive waveform is only important when driving clamped inductive loads. For purposes of this example, this time is arbitrarily chosen as 0.5µs. The blanking time for the desaturation amplifier is limited by the maximum allowable short circuit time under full gate drive voltage. This requirement stems from the fact that if a fault is present before the IGBT is commanded on, the UC3727 has no way of determining that the fault is present. Therefore, the IGBT will drive into the short circuit at full gate voltage for the duration of the blanking time. Since the maximum allowable short circuit time under these conditions is 5µs, the blanking time should be less, and 4µs was selected. Equations 7 and 8 can be solved simultaneously to obtain C12 = 100pF, and R7 = 91k.

DESIGN CONSIDERATIONS FOR THE FAULT CIRCUITRY

To program the fault circuitry, the short circuit characteristics of the IGBT are again used. The first consideration is the threshold of the desaturation comparator, which is programmed at the inverting input. For fast response, this trigger amplitude should be as low as possible. However, it must also be high enough to allow the comparator to recognize if a fault has gone away during the fault window. As detailed in the previous section, the IGBT will be operating under reduced gate voltage at that time.

The data sheets for the APT50GL60BN indicate that for a gate voltage of 8V, and collector current of 20A, the collector to emitter saturation voltage is 2V. Allowing for 1V of margin, plus a maximum diode drop of 1V, the DSAT- input is selected as 4V. The level is programmed by the voltage divider formed by R12 and R13, assuming the minimum level for V_{CC} of 15.5V. This leads to R12 = 18k and R13 = 51k.

The diode used in the fault circuit must be chosen for fast reverse recovery, low capacitance, and high breakdown voltage rating. **The reverse recovery time should be at least an order of magnitude faster than the short circuit time rating of the IGBT.** The capacitance should be low enough to prevent high currents from flowing into the DSAT- input in the presence of high dv/dt. Finally, the breakdown voltage rating must obviously be greater than the maximum IGBT collector voltage.

If the IGBT collector voltage is relatively low, the diode can be replaced with a high value resistor. This solution has the advantages of low capacitance and no reverse recovery problems. However, extreme care must be exercised to insure that the resistor is large enough to prevent the DSAT+ from overvoltage conditions formed by the resistive divider when the IGBT is off.

Another alternative for low power applications is to use a more conventional current sense resistor at the emitter of the IGBT. The DSAT+ input can be tied to the high side of the sense resistor, and the DSAT- input can be biased to some trip point proportional to emitter current. This allows for more precise control of the maximum current through the IGBT. Usually the voltage drop and power dissipation of the sense resistor are two high to make this a practical solution though. An example of this technique is shown in the examples section of this application note.

R10 is chosen to provide adequate bias current to the diode to insure that it is in the on state when the IGBT is in saturation. R11 provides isolation between the diode and the DSAT+ input. Its selection is fairly arbitrary, but the reverse recovery and capacitance characteristics of the diode must be considered to insure that excess current is not injected into the DSAT+ input during switching transitions.

The next consideration is the selection of the time the gate will be held at the clamp level in the presence of a fault, referred to as the fault window. Since the allowable short circuit time with a gate drive of 10V is 40µs, the fault window is selected as 10µs to allow for plenty of margin. The selection of the delay period should take into account the relative slow speed of optocouplers, and the timing requirements on the FRESET signal that must be provided to the UC3726. The blanking period is chosen as 100µs for this example. Using equations 9 and 10 this leads to:

25) $10\mu s = (R8)(C13) \bullet ln((R8 - 7600)/(R8 - 12400)$

26) $100\mu s = 0.4 \bullet (R8)(C13)$

These equations do not yield standard values when solved simultaneously. A close solution is C13 = 2200pF and R8 = 91k. This results in a fault window of 11.8µs and a blanking period of 80µs.

The only remaining programmable option selection is the fault window timing for the UC3726. This time duration must be long enough to allow for the slow speed of the optocoupler. For this example, the optocoupler (CNY17) has a typical switching time of 10µs. Choosing C3 = 2200pF and solving Equation 5 results in a fault window of 23µsec.

FILTER/DECOUPLING CAPACITOR CONSIDERATIONS

Proper bypass capacitor selection is essential to insure proper operation of the UC3726/UC3727 chip pair. The UC3726 does not have the high peak current requirements that the UC3727 does and therefore a high quality ceramic capacitor of about 1µF is usually sufficient. This capacitor must be located as close to the V_{CC} and GND pins of the chip as possible.

The UC3727 on the other hand must supply high peak currents during the charging and discharging of the IGBT gate. While all of the average current for the gate drive is ultimately supplied by the UC3726 through the pulse transformer, circuit inductances force most of the instantaneous peak current to come from the bypass capacitors. If insufficient bypassing is used, the ripple voltage at the UC3727 can be large enough to trip the under voltage lockout circuitry.

In order to determine the maximum allowable ripple voltage, Equation 6 is used. The margin allowed in Equation 6 becomes the maximum ripple voltage. Since the ripple voltage results from charging the IGBT gate, the equation leads to the bypass requirements for PV_{CC} and PV_{EE}:

27) $V_{ripple} = (V_A - V_B) - (V_{CC} + V_{EEUVLO} + 2V_D)$

The ripple voltage will be composed of a gate charge component and an ESR component. The gate charge component results from the voltage drop of the bypass capacitor due to gate charge requirements. The resulting voltage drop of the decoupling capacitor due to gate charge requirements is expressed as follows:

28) $dV_{CHARGE} = Q_G/C_{BYPASS}$

The ripple component due to ESR loss is directly proportional to the peak gate current. It is expressed as:

29) $dV_{ESR} = I_{PEAK} \bullet ESR$

In Equation 29, ESR represents the equivalent series resistance of the bypass capacitor. The sum of the voltage drops represented by Equations 28 and 29 must not exceed the maximum ripple voltage.

For the example shown in Figure 9, Equation 27 yields a maximum ripple voltage of 1.6V. The peak gate current is limited to 4A, and therefore we can calculate the maximum allowable ESR from Equation 9. If we use a maximum allowable ESR loss of 0.5V we have:

30) $ESR = 0.5V/4A = 0.125\ ohm\ (max)$

Allowing 0.5V for the charge component of the ripple voltage sets the minimum value of bypass capacitance:

31) $C_{BYPASS} = 110nC/0.5V = 0.22\mu F\ (min)$

For this circuit a single 1µF capacitor on both the PV_{CC} and PV_{EE} pins of the UC3727 is sufficient. For larger values of gate charge the solution would involve a small ceramic capacitor for low ESR and a larger electrolytic capacitor in parallel to supply gate charge. To be conservative, a 10µF electrolytic capacitor is added between PV_{CC} and PV_{EE}. The V_{CC} and V_{EE} pins are also bypassed as described earlier in this application note and resistive isolation is provided between the high power and low power voltage supplies. R18 is added to balance the supply currents to ensure active start up in the presence of slowly rising supply voltages. These equations only describe the minimum bypass requirements. If the system is particularly noisy, significantly more bypass capacitance may be required.

TEST CIRCUIT RESULTS

The example circuit was built and tested to verify operation, with the results shown in Figure 10. The waveforms for V_E and I_E are shown. Notice the characteristic "tail" in the turn off waveforms for both current and voltage. The tail results from the fact that IGBTs are minority carrier devices, and therefore have stored charge. At the beginning of turn off, the collector to emitter current decreases rapidly to the level of the hole recombination current for the device. At this point di/dt decreases, and the voltage and current waveforms tail off at a much slower rate. The reason for the bump in the voltage waveform is that as di/dt decreases, inductive voltage drops also decrease, and therefore

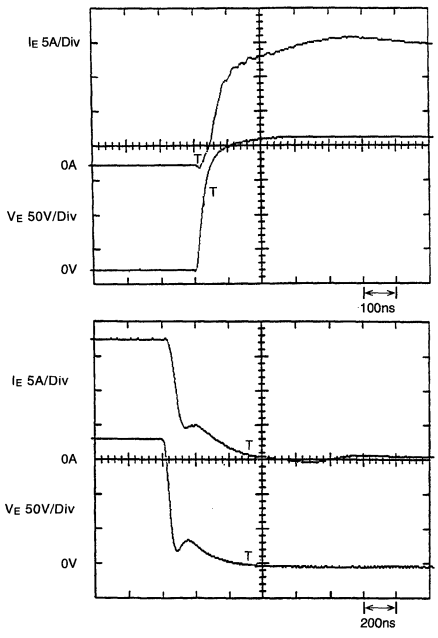

Figure 10. Test Circuit Waveforms (V_{PD} = 375V)

more voltage is dropped across the IGBT at the start of the tail.

Figure 11 shows waveforms for the same circuit when tested with V_{DD} = 375V. Notice the slower switching times due to the higher output voltage and current.

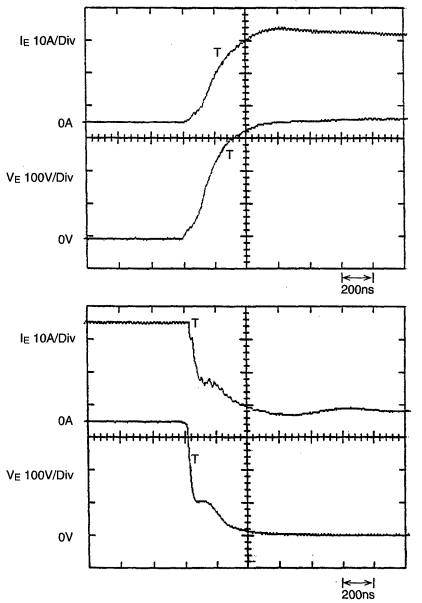

Figure 11. Test Circuit Waveforms (V_{PD} = 375V)

DESIGN EXAMPLES/APPLICATIONS

The example circuit described earlier in this application note provides a good baseline for calculating component values for the required support circuitry for the IGBT driver pair. Many other circuit topologies can be used with this chip set, and the same general rules apply as for the example circuit. The individual system designer must evaluate the particular requirements, and make component selections accordingly. This section illustrates some general circuit topologies which may be encountered by a typical system designer.

SENSING FAULTS WITH A CURRENT SENSE RESISTOR

Figure 12 shows a way of detecting faults with a current sense resistor. The desaturation comparator is used to detect over current conditions. Using a resistor divider network from V_{CC} allows the trip level to be set at the D_{SAT-} input to the comparator. Current is sensed at the emitter of the IGBT, with the filtered voltage across the current sense resistor fed into the D_{SAT+} input. This approach has an advantage for low power applications because there is no diode in the protection circuit and therefore no reverse recovery problems to worry about. Also with this technique, more precise control of the current limit is possible. A drawback to this approach is that the filter time constant required may be too long for IGBTs that can not tolerate fault conditions for very long. Also, for high power applications the power requirement for the sense resistor may be impractical.

HALF BRIDGE OUTPUT CIRCUIT

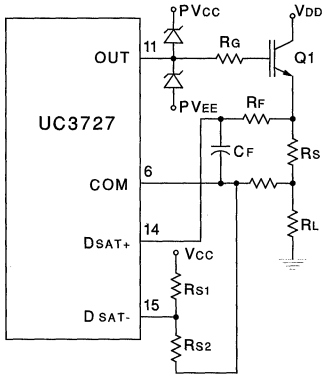

Figure 12. Detecting Faults with Current Sense Resistor

Figure 13 shows a half bridge output circuit with a dual secondary transformer. The low side of the bridge is driven by a UC3727 with its polarity reversed from the upper side driver. Cross conduction is controlled by providing dual gate resistors for both upper and lower IGBTs. Carefully selecting RG1 and RG2 can provide fast turn-off and slow turn-on. If more accurate dead time between on commands for upper and lower IGBTs is required, the $\overline{ENBL}$ inputs can be used. Using an optocou-

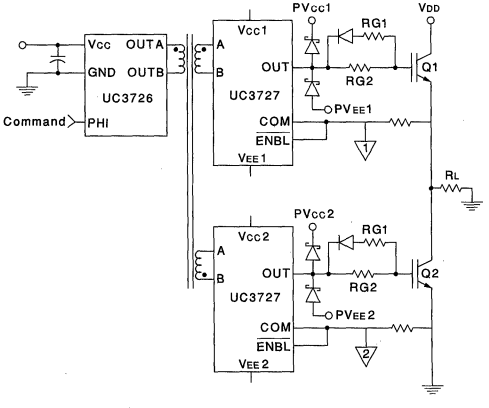

Figure 13. Half Bridge Output Circuit

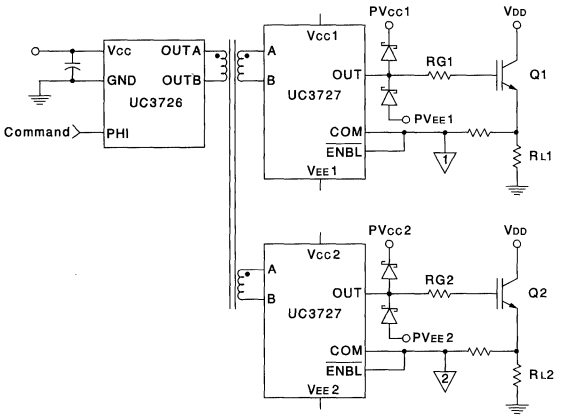

Figure 14. Dual High Side Driver Circuit

pler or level shift network, the $\overline{\text{ENBL}}$ input can be controlled separately to assure that cross conduction is prevented.

MULTIPLE ISOLATED DRIVER CIRCUIT

Figure 14 shows a dual isolated driver circuit topology. By using a multiple secondary winding transformer, several IGBTs can be driven simultaneously. Isolation, command signal, and power are provided to each IGBT by the single transformer. Obviously power dissipation in the UC3726 is a consideration, and ultimately will be a limiting factor in determining the maximum number of IGBTs that can be driven. The $\overline{\text{ENBL}}$ inputs can also be used to provide dead time between IGBTs if it is required.

UC3726/UC3727 IGBT EVALUATION KIT

Unitrode Integrated Circuits has designed an evaluation kit which can be used to demonstrate the UC3726/UC3727 IGBT driver pair. The kit consists of a custom PC board, two each of the UC3726 and UC3727, a UC3612 Schottky diode pair, and one Coilcraft Q3868-A transformer. The purpose of this evaluation kit is to provide the user with a way of quickly demonstrating the driver pair for an individual application.

The schematic, silkscreen, and artwork for the evaluation board are shown in Figures 15, 16, 17, and 18 respectively. The schematic for the evaluation board is identical to the schematic shown in the example circuit (Figure 9), except for some additional components which may be required to evaluate certain conditions.

Table 1 shows the list of materials for the demo board for building the example circuit. If it is desired to evaluate other requirements than those described in this application note, the same equations should be used to determine component values. For more information on obtaining this demo kit, contact Unitrode Integrated Circuits at (603) 429-8610.

SUMMARY

By utilizing the new UC3726/UC3727 IGBT driver chip pair, a practical and cost-effective solution to the problem of driving high-side IGBTs can be realized. This chip pair incorporates several special features to provide fault protection and optimum gate drive. Using a high voltage isolation transformer precludes the need for high voltage integrated circuits. This chip pair is ideally suited for a wide range of isolated IGBT driver applications.

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Coilcraft telephone number : 1-800-322-COIL

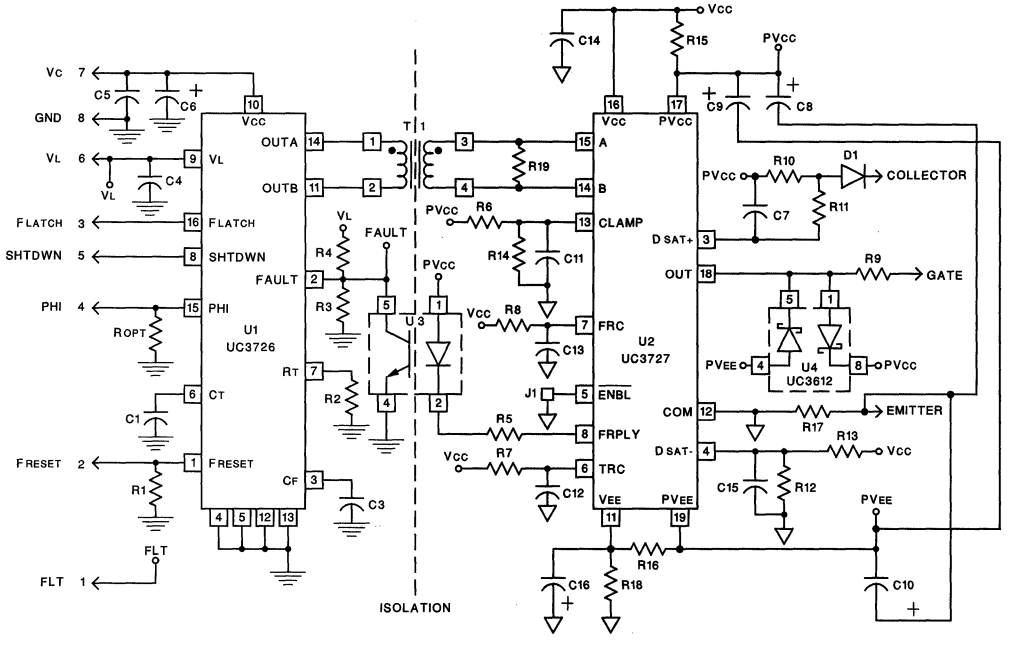

Figure 15. IGBT Driver Pair Evaluation Board Schematic

TABLE 1
UC3726/UC3727 IGBT ISOLATED DRIVER PAIR DEMO KIT
LIST OF MATERIALS

CAPACITORS

C1, C12	100pF, 35V
C3, C13	2200pF, 35V
C4, C11	0.1µF, 35V
C5, C8, C10	1µF, 35V
C14, C16	1µF, 35V
C6, C9	10µF, 35V

DIODES

D1	UF4007, BV= 1000V (General Instrument)

INTEGRATED CIRCUITS

U1*	UC3726Isolated Drive Transmitter
U2*	UC3727Isolated High Side IGBT Driver
U3	CNY17 Optocoupler, 10µs
U4*	UC3612 Schottky Diode Pair

R1, R8, R11, Ropt	2k, 1/4W
R2, R4, R6, R14	5.1k, 1/4W
R5	10k, 1/4W
R7, R8	91k, 1/4W
R9	5.6Ω, 1W
R10, R12	18k, 1/4W
R13	51k, 1/4W
R15, R16, R17	3.3Ω, 1/4W

MAGNETICS

T1* Coilcraft Q3868-A

*Included with demo kit.

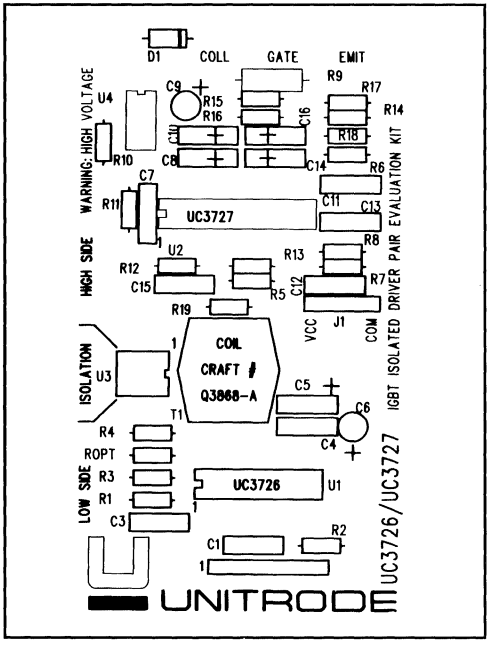

Figure 16. Silkscreen

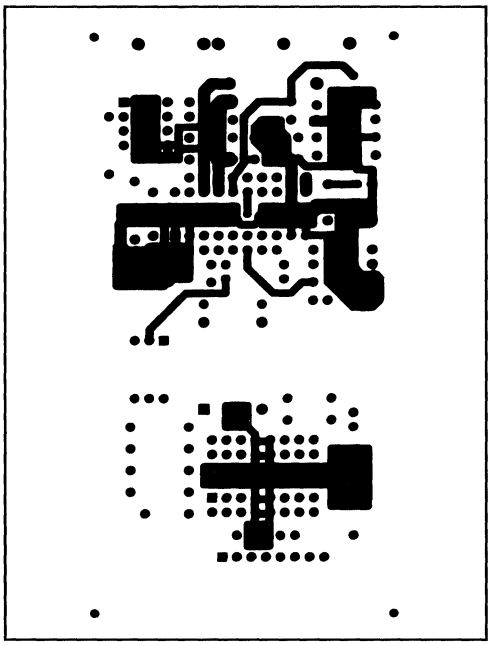

Figure 17. Component Side

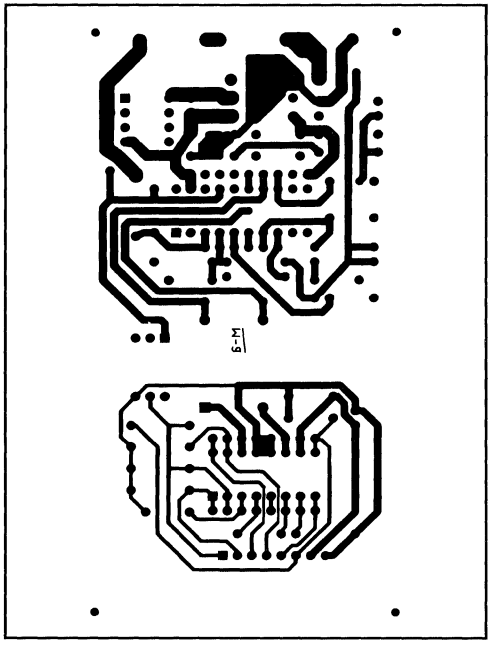

Figure 18. Solder Side

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
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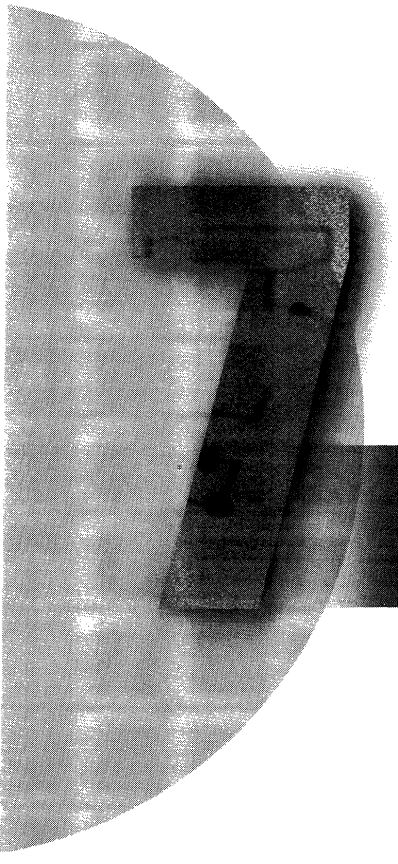


Power Supply Support

Power Supply Support

Power Supply Support

Feedback Signal Generators	UNITRODE PART NUMBER			
	UC3901	UC39431	UC39432	UC3965
Description	Isolated Feedback Generator	Precision Adjustable Shunt Regulator	Precision Analog Controller	Precision Reference with Low Offset Error Amplifier
Application	Amplitude Modulation System Used to Couple a Control Signal Across a Voltage Isolation Barrier	Adjustable 100mA Shunt Regulator, Voltage Reference Optocoupler Driver, Voltage to Current Converter	Adjustable 100mA Shunt Regulator, Optocoupler Driver, Programmable Transconductance Voltage to Current Converter	Used for High Precision PWM Switching Regulators
Key Features	•Transformer Couples Isolated Feedback Error Signal •Low Cost Alternative to Optical Couplers •5MHz Carrier Provides Fast Response Capability •Modulator Synchronizable to an External Clock	•Multiple On-chip Programmable Reference Voltages •2.2V to 36V Operating Supply Voltage and User Programmable Reference •Linear Transconductance for Optocoupler Feedback Applications	•Programmable, Linear Transconductance for Optimum Optocoupler Current Drive •Precision Reference and Error Amplifier Inputs Externally Available •2.2V to 36V Operating Supply Voltage and User Programmable Reference	•2.5V Precision Reference with 0.4% Accuracy •Low 1mV Offset Error Amplifier •2X Inverting Amplifier / Buffer Output •Drivers Optocoupler Diode for Isolated Applications
Application / Design Note	DN-19, DN-33, U-94		DN-52	U-165
Pin Count❖	14, 16	8	8	8
Page Number	PS/7-21	PS/7-50	PS/7-56	PS/7-60

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Load Share Controllers	UNITRODE PART NUMBER		
	UC3902	UC3907	
Description	8-Pin Load Share Controller	Load Share Controller	
Application	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	
Key Features	•Highly Tolerant of Voltage Differences Between Power Supply Return •2.7V to 20V Operation •High Gain, Low Offset Current Sense Amplifier Permits Low Shunt Resistor Values •Single Capacitor Sets Load Share Filter Response	•Fully Differential High Impedance Voltage Sensing •Accurate Current Amplifier for Precise Load Sharing •Optocoupler Driving Capability •4.5V to 35V Operation	
Application / Design Note	U-129, U-163	U-129, U-163	
Pin Count❖	8	16	
Page Number	PS/7-27	PS/7-44	

Schottky Diode Array / Bridges	UNITRODE PART NUMBER		
	UC3610	UC3611	UC3612
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	•Monolithic Eight-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time	•Matched, Four-diode Monolithic Array •High Peak Current •Low Forward Voltage •Parallelable for Higher Current or Lower Voltage Drop	•Monolithic Two-diode Array •High Peak Current •Low Forward Voltage •Fast Recovery Time
Application / Design Note			DN-48
Pin Count❖	8, 16	8, 16	8
Page Number	PS/7-10	PS/7-12	PS/7-15

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Supervisory and Monitor Circuits	UNITRODE PART NUMBER				
	UC3543	UC3544	UC3730	UC3903	UC3904
Power Supply Monitor	Single	Single		Quad	Quad
Temperature Monitor			Y		
Description	Power Supply Supervisory with OV, UV and Current Sensing	Power Supply Supervisory with OV, UV and Current Sensing	Combines a Temperature Transducer, Precision Reference, and Temperature Comparator for Maximum System Flexibility	Quad Supply and Line Monitor	Quad Supply and Line Monitor
Voltage Clamp					
Voltage Range	5V to 35V	5V to 35V		8V to 40V	4.75V to 18V
Window Adjust	N	N		Y	Y
Current Range					
Current Limit	Y	Y		N	N
Programmable Threshold	Y	Y		Y	Y
Programmable Time Delay	Y	Y		Y	Y
Special Features		Uncommitted OV Inputs			
Application / Design Note				DN-33	
Pin Count❖	16	18	5, 8, 20	18	18
Page Number	PS/7-5	PS/7-5	PS/7-17	PS/7-32	PS/7-39

Supervisory and Monitor Circuits	UNITRODE PART NUMBER		
	UCC3946		
Description	Microprocessor Supervisor with Watchdog Timer		
Application	Accurate Microprocessor Supervision		
Key Features	• Programmable Reset Period • Programmable Watchdog Period • 1.5% Accurate Threshold • 4mA IDD		
Pin Count❖	8		
Page Number	PP/7-88		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product


UNITRODE

UNITRODE

UC1543 UC1544
UC2543 UC2544
UC3543 UC3544

Power Supply Supervisory Circuit

FEATURES

- Includes Over-voltage, Under-voltage, And Current Sensing Circuits
- Internal 1% Accurate Reference
- Programmable Time Delays
- SCR "Crowbar" Drive Of 300mA
- Remote Activation Capability
- Optional Over-voltage Latch
- Uncommitted Comparator Inputs For Low Voltage Sensing (UC1544 Series Only)

DESCRIPTION

The monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; an under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

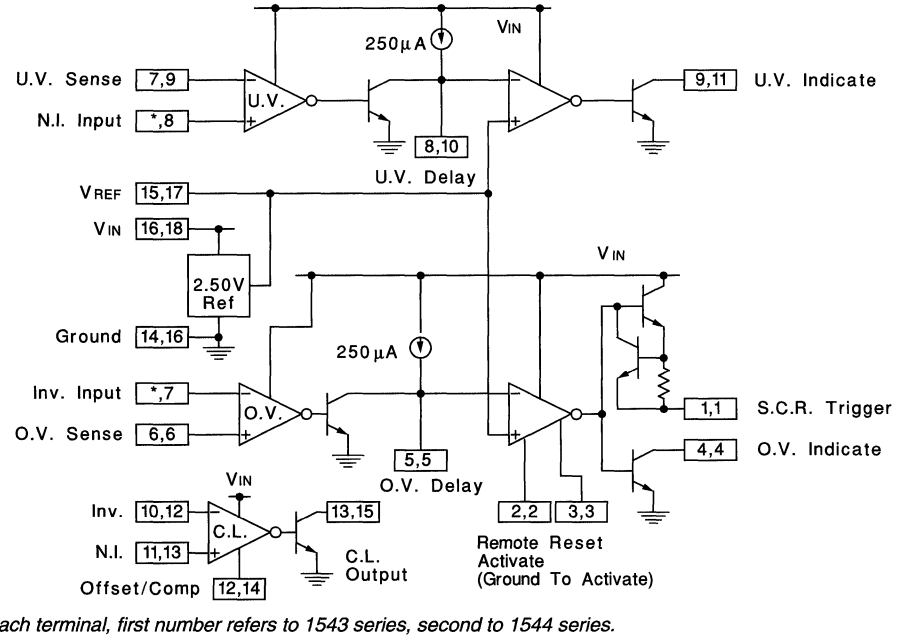
Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5V may be monitored by dividing down the internal reference voltage. The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

7

BLOCK DIAGRAM



Note: For each terminal, first number refers to 1543 series, second to 1544 series.
** On 1543 series, this function is internally connected to VREF.*

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN} 40V
Sense Inputs, Voltage Range . . . . . 0 to V_{IN}
SCR Trigger Current (Note 1) . . . . . -600mA
Indicator Output Voltage 40V
Indicator Output Sink Current 50mA
Power Dissipation (Package Limitation) 1000mW
Operating Temperature Range
UC1543, UC1544 . . . . . -55°C to +125°C
UC2543, UC2544 . . . . . -25°C to +85°C
UC3543, UC3544 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -65°C to +150°C

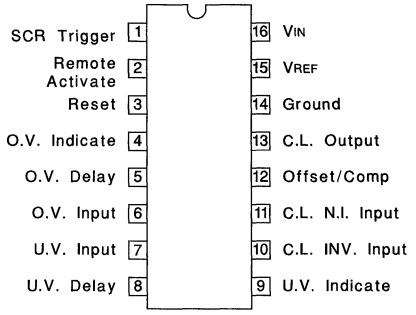
Note 1: At higher input voltages, a dissipation limiting resistor, RG, is required.

Note 2: Currents are positive-into, negative-out of the specified terminal. Consult Packaging section of Databook for thermal limitations

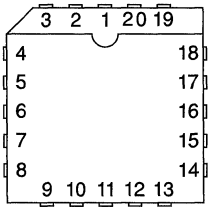
CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N, DW Package

UC 1543
UC 2543
UC 3543



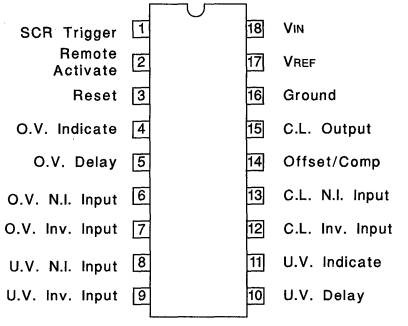
PLCC-20, LCC-20
(TOP VIEW)
Q or L Package



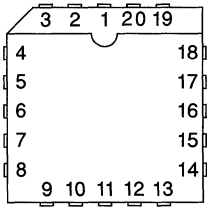
PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. Input	8
N/C	9
N/C	10
U.V. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package

UC 1544
UC 2544
UC 3544



PLCC-20, LCC-20
(TOP VIEW)
Q or L Package

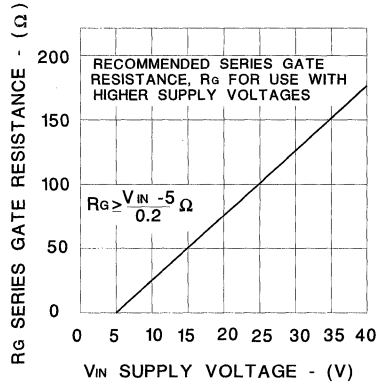


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
SCR Trigger	2
Remote Activate	3
Reset	4
O.V. Indicate	5
N/C	6
O.V. Delay	7
O.V. N.I. Input	8
O.V. INV. Input	9
U.V. N.I. Input	10
U.V. INV. Input	11
U.V. Delay	12
U.V. Indicate	13
C.L. INV. Input	14
C.L. N.I. Input	15
Offset/Comp	16
C.L. Output	17
Ground	18
V_{REF}	19
V_{IN}	20

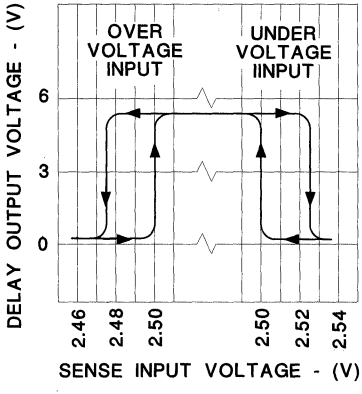
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1543 and UC1544; -25°C to +85°C for the UC2543 and UC2544; and 0°C to +70°C for the UC3543 and UC3544. Electrical tests are performed with V_{IN} = 10V and 2kΩ pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5V reference. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1543/UC1544 UC2543/UC2544			UC3543/UC3544			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Voltage Range	T_J = 25°C to T_{MAX}	4.5		40	4.5		40	V
	T_{MIN} to T_{MAX}	4.7		40	4.7		40	V
Supply Current	V_{IN} = 40V, Output Open, T_J = 25°C		7	10		7	10	mA
	$T_{MIN} \le T_J \le T_{MAX}$			15			15	mA
Reference Section								
Output Voltage	T_J = 25°C	2.48	2.50	2.52	2.45	2.50	2.55	V
Output Voltage	Over Temperature Range	2.45		2.55	2.40		2.60	V
Line Regulation	V_{IN} = 5 to 30V		1	5		1	5	mV
Load Regulation	I_{REF} = 0 to 10mA		1	10		1	10	mV
Short Circuit Current	V_{REF} = 0	-10	-20	-40	-12	-20	-40	mA
Temperature Stability			50			50		ppm/°C
SCR Trigger Section								
Peak Output Current	V_{IN} = 5V, R_G = 0, V_O = 0	-100	-300	-600	-100	-300	-600	mA
Peak Output Voltage	V_{IN} = 15V, I_O = -100mA	12	13		12	13		V
Output Off Voltage	V_{IN} = 40V		0	0.1		0	0.1	V
Remote Activate Current	R/A Pin = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Remote Activate Voltage	R/A Pin Open		2	6		2	6	V
Reset Current	Reset = Gnd, R/A = Gnd		-0.4	-0.8		-0.4	-0.8	mA
Reset Voltage	Reset open, R/A = Gnd		2	6		2	6	V
Output Current Rise Time	R_L = 50Ω, T_J = 25°C, C_D = 0		400			400		mA/µs
Prop. Delay from R/A	R_L = 50Ω, T_J = 25°C, C_D = 0		300			300		ns
Prop. Delay from O/V input	R_L = 50Ω, T_J = 25°C, C_D = 0		500			500		ns
Comparator Section								
Input Threshold (Input voltage rising on O.V. and falling on U.V.)	T_J = 25°C	2.45	2.50	2.55	2.40	2.50	2.60	V
	Over Temperature Range	2.40		2.60	2.35		2.65	V
Input Hysteresis			25			25		mV
Input Bias Current	Sense Input = 0V		-0.3	-1.0		-0.3	-1.0	µA
Delay Saturation			0.2	0.5		0.2	0.5	V
Delay High Level			6	7		6	7	V
Delay Charging Current	V_O = 0	-200	-250	-300	-200	-250	-300	µA
Indicate Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Indicate Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Propagation Delay	Input Over Drive = 200mV, T_J = 25°C, C_D = 0		400			400		ns
	Input Over Drive = 200mV, T_J = 25°C, C_D = 1µF		10			10		ms
Current Limit Section								
Input Voltage Range		0		V_{IN}-3V	0		V_{IN}-3V	V
Input Bias Current	Offset Pin Open, V_{CM} = 0		-0.3	-1.0		-0.3	-1.0	µA
Input Offset Voltage	Offset Pin Open, V_{CM} = 0		0	10		0	10	mV
	10kΩ from Offset Pin to Gnd	80	100	120	80	100	120	mV
CMRR	$0 \le V_{CM} \le 12V$, V_{IN} = 15V	60	70		60	70		dB
AVOL	Offset Pin Open, V_{CM} = 0V, R_L = 10k to 15kΩ, ΔV_{OUT} = 1 to 6V	72	80		72	80		dB
Output Saturation	I_L = 10mA		0.2	0.5		0.2	0.5	V
Output Leakage	V_{IND} = 40V		.01	1.0		.01	1.0	µA
Small Signal Bandwidth	A_V = 0dB, T_J = 25°C		5			5		MHz
Propagation Delay	$V_{OVERDRIVE}$ = 100mV, T_J = 25°C		200			200		ns

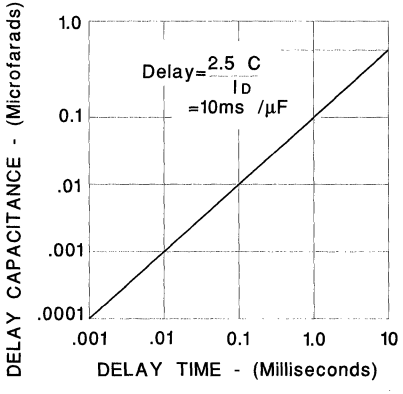
SCR Trigger Power Limiting



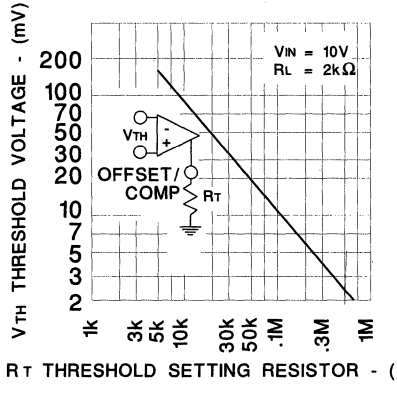
Comparator Input Hysteresis



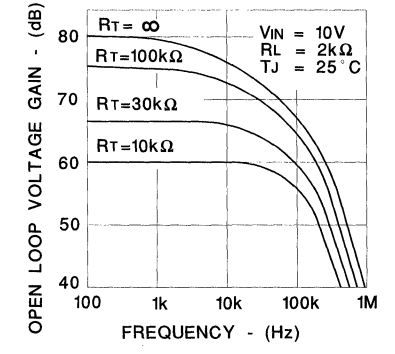
Activation Delay vs Capacitor Value



Current Limit Input Threshold

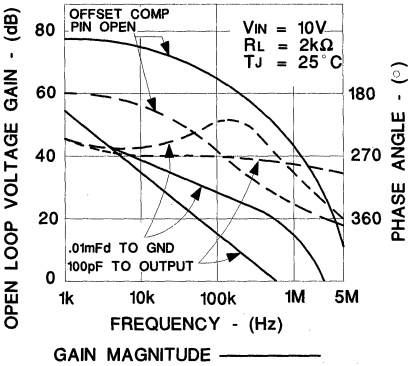


Current Limit Amplifier Gain



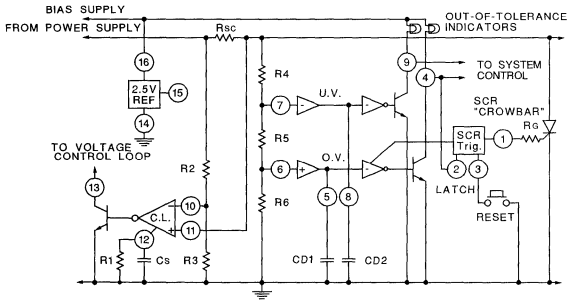
Note: RT is connected from Offset Pin to Gnd. Values of RT below 5.0k may cause Amplifier Cutoff at -55°C.

Current Limit Amplifier Frequency Response



APPLICATIONS (Pin numbers given for UC1543 series devices)

Typical Application



The values for the external components are determined as follows:

Current limit input threshold, $V_{TH} = \frac{1000}{R1}$

C_S *is determined by the current loop dynamics*

Peak current to load, $I_P \cong \frac{VTH}{RSC} + \frac{VO}{RSC}\left(\frac{R2}{R2+R3}\right)$

Short Circuit Current, $I_{SC} = \frac{VTH}{RSC}$

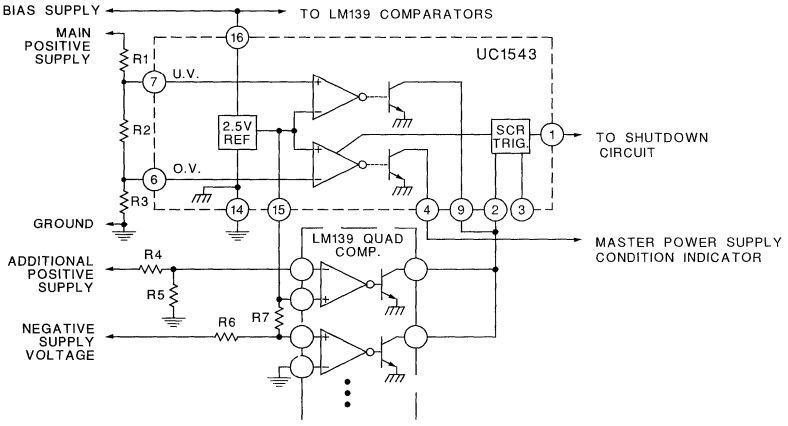
Low output voltage limit, $V_O\ (Low) = \frac{2.5\ (R4+R5+R6)}{R5+R6}$

High output voltage limit, $V_O\ (High) = \frac{2.5\ (R4+R5+R6)}{R6}$

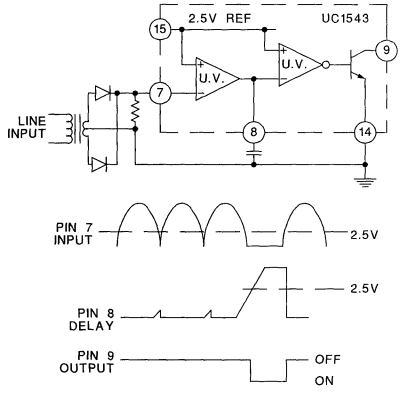
Voltage sensing delay, $t_D = 10{,}000Cd$

SCR trigger power limiting resistor, $R_G > \frac{VIN - 5}{0.2}$

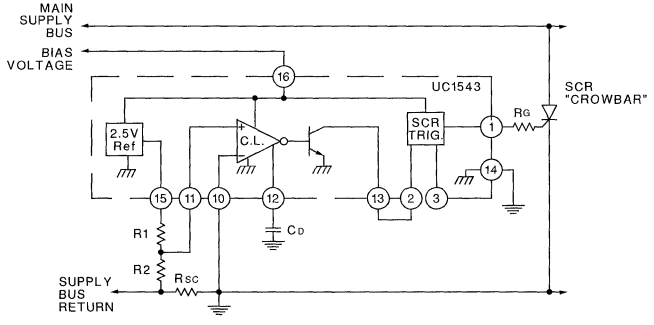
Sensing Multiple Supply Voltages



Input Line Monitor



Overcurrent Shutdown



UNITRODE CORPORATION
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Dual Schottky Diode Bridge

FEATURES

- Monolithic Eight-Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

This eight-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads. The dual bridge connection makes this device particularly applicable to bipolar driven stepper motors.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1610 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability. The UC2610 in plastic and ceramic is designed for -25°C to +125°C environments also with reduced peak current capability; while the UC3610 in plastic has higher current rating over a 0°C to +70°C temperature range.

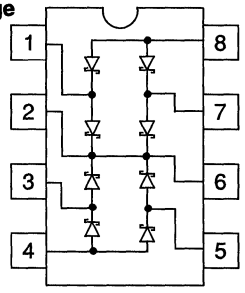
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current
  UC1610 . . . . . 1A
  UC2610 . . . . . 1A
  UC3610 . . . . . 3A
Power Dissipation at T_A = +70°C 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

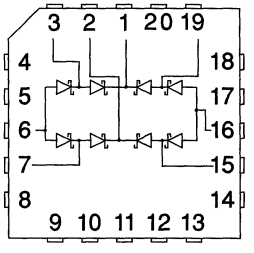
Note:Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

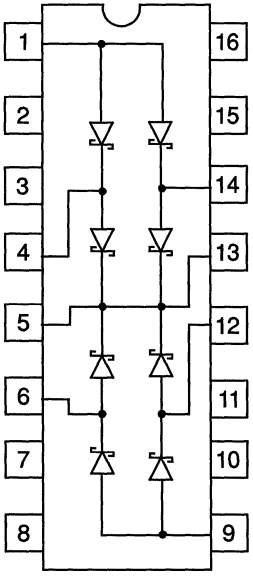
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package

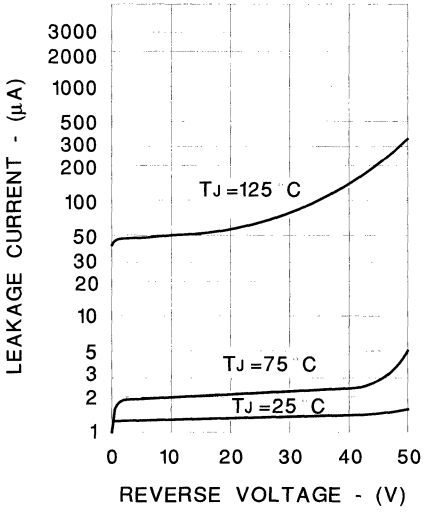


ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = 25°C except as noted. T_A = T_J.

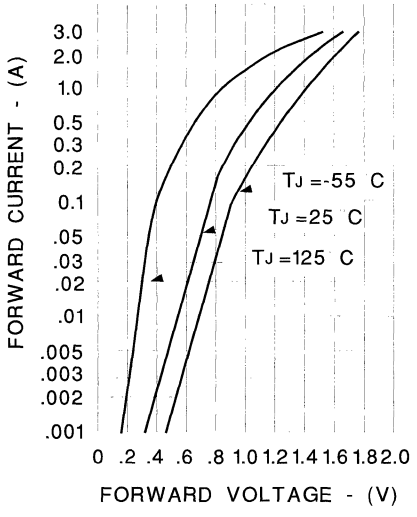
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage Drop	I_F = 100mA	0.35	0.5	0.7	V
	I_F = 1A	0.8	1.0	1.3	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

Note:At forward currents of greater than 1.0A a parasitic current of approximately 10mA may be collected by adjacent diodes.

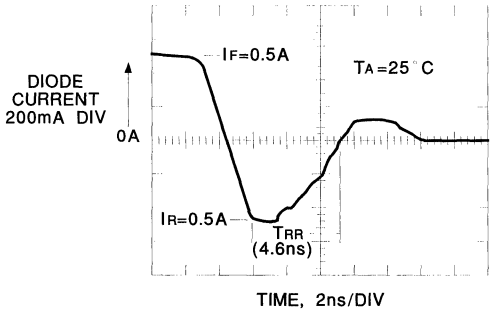
Reverse Current vs Voltage



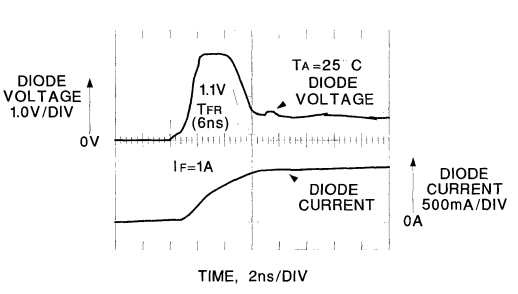
Forward Current vs Voltage



Reverse Recovery Characteristics



Forward Recovery Characteristics



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Quad Schottky Diode Array

FEATURES

- Matched, Four-Diode Monolithic Array
- High Peak Current
- Low-Cost MINIDIP Package
- Low-Forward Voltage
- Parallelable for Lower V_F or Higher I_F
- Fast Recovery Time
- Military Temperature Range Available

DESCRIPTION

This four-diode array is designed for general purpose use as individual diodes or as a high-speed, high-current bridge. It is particularly useful on the outputs of high-speed power MOSFET drivers where Schottky diodes are needed to clamp any negative excursions caused by ringing on the driven line.

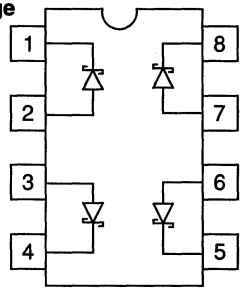
These diodes are also ideally suited for use as voltage clamps when driving inductive loads such as relays and solenoids, and to provide a path for current free-wheeling in motor drive applications.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

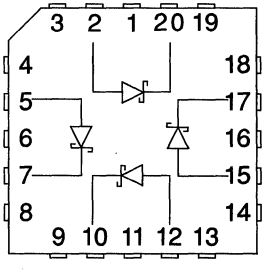
This single monolithic chip is fabricated in both hermetic CERDIP and copper-leaded plastic packages. The UC1611 in ceramic is designed for -55°C to +125°C environments but with reduced peak current capability: while the UC3611 in plastic has higher current rating over a 0°C to +70°C ambient temperature range.

CONNECTION DIAGRAM

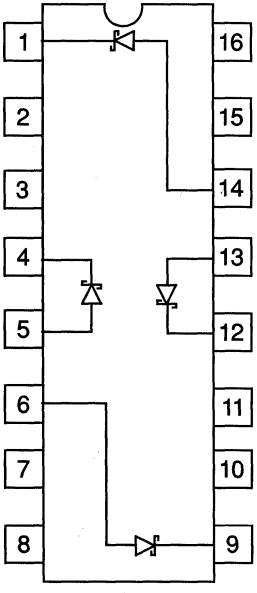
DIL-8 (TOP VIEW)
N or J Package



PLCC-20 (TOP VIEW)
Q Package



SOIC-16 (TOP VIEW)
DW Package



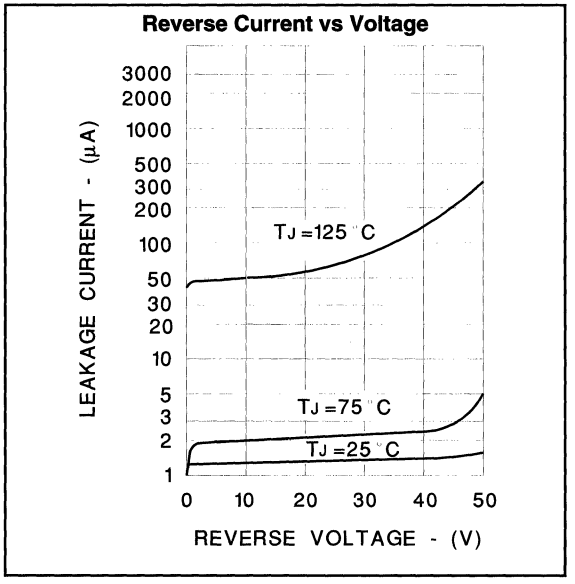
ABSOLUTE MAXIMUM RATINGS

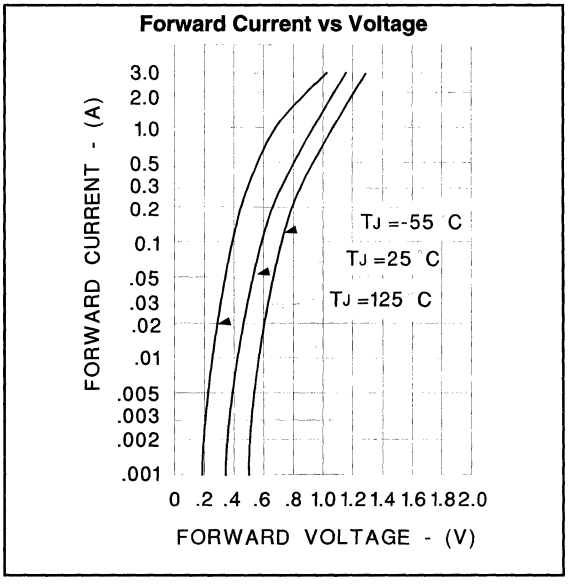
Peak Inverse Voltage (per Diode) 50V
Diode-to-Diode Voltage 80V
Peak Forward Current
UC1611 . . . . . 1A
UC3611 . . . . . 3A
Power Dissipation at TA = +70°C 1W
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C
Note: Please consult Packaging Section of Databook for thermal limitations and considerations of package.

ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = +25°C except as noted. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward Voltage Drop	I_F = 100mA	0.3	0.4	0.7	V
	I_F = 1A		0.9	1.2	V
Leakage Current	V_R = 40V		0.01	0.1	mA
	V_R = 40V, T_J = +100°C		0.1	1.0	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		20		ns
Forward Recovery	1A Forward to 1.1V Recovery		40		ns
Junction Capacitance	V_R = 5V		100		pF

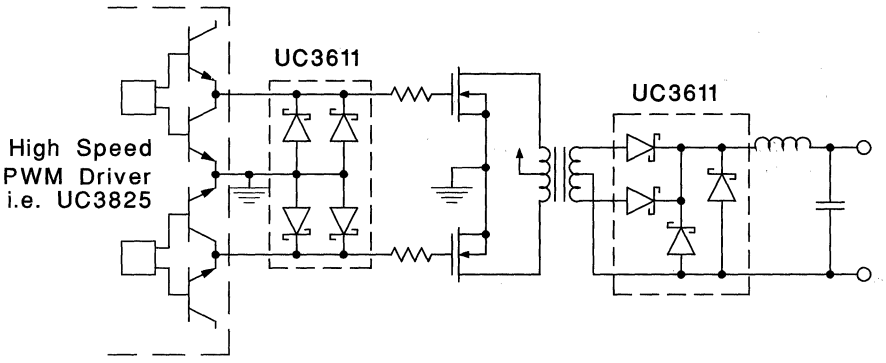
Note: At Forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.



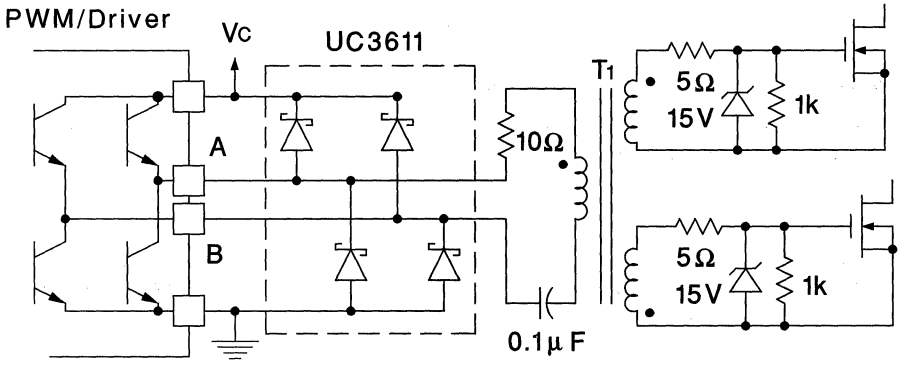


TYPICAL APPLICATIONS

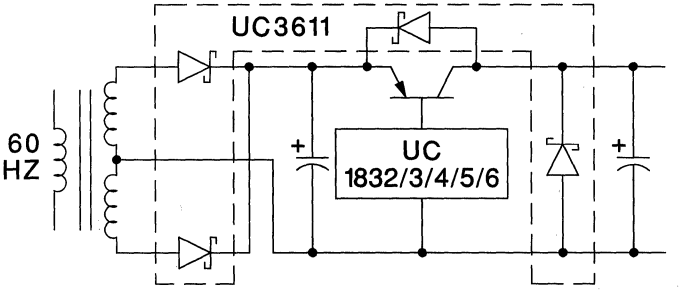
A. Clamp Diodes - PWMS and Drivers



B. Transformer Coupled Drive Circuits



C. Linear Regulations



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UNITRODE

Dual Schottky Diode

FEATURES

- Monolithic Two Diode Array
- Exceptional Efficiency
- Low Forward Voltage
- Fast Recovery Time
- High Peak Current
- Small Size

DESCRIPTION

The two-diode array is designed for high-current, low duty-cycle applications typical of flyback voltage clamping for inductive loads.

The use of Schottky diode technology features high efficiency through lowered forward voltage drop and decreased reverse recovery time.

This single monolithic chip is fabricated in hermetic CERDIP as well as copper leaded plastic MINIDIP and SOIC surface mount power pack. The UC1612 in ceramic is designed for –55°C to +125°C environments, but with reduced peak current capability; while the UC3612 has higher current rating over a 0°C to +70°C ambient temperature range.

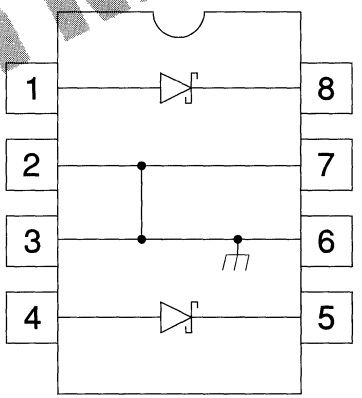
ABSOLUTE MAXIMUM RATINGS

Peak Inverse Voltage (per diode) 50V
Peak Forward Current, UC3612 . . . . . 3A
Peak Forward Current, UC1612 . . . . . 1A
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . 300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8
(Top View)
J, N, or DP Package



Pins 2, 3, 6, 7 are connected to substrate and must be electrically isolated.

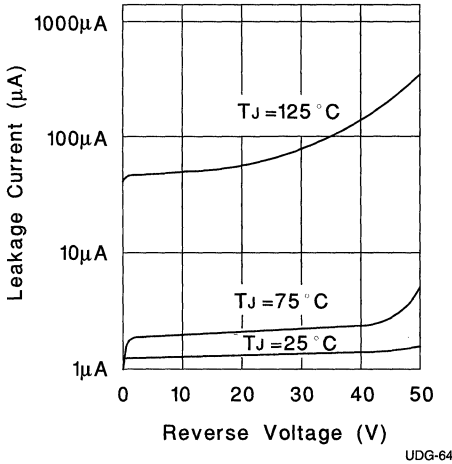
UDG-64044

ELECTRICAL CHARACTERISTICS: All specifications apply to each individual diode. T_J = 25°C except as noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Leakage Drop	I_F = 100mA		0.49	0.55	V
	I_F = 1A0		0.9	1.0	V
Leakage Current	V_R = 40V		.01	0.1	mA
	V_R = 40V, T_J = 100°C		0.1	0.1	mA
Reverse Recovery	0.5A Forward to 0.5A Reverse		15		ns
Forward Recovery	1A Forward to 1.1V Recovery		30		ns
Junction Capacitance	V_R = 5V		70		pF

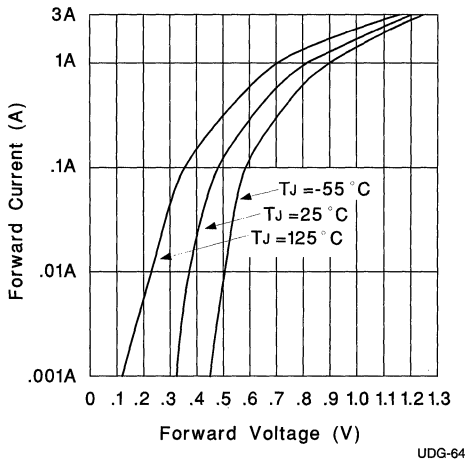
Note: At forward currents of greater than 1.0A, a parasitic current of approximately 10mA may be collected by adjacent diodes.

Reverse Current vs Voltage



UDG-64045

Forward Voltage vs Current



UDG-64046

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Thermal Monitor

FEATURES

- On-Chip Temperature Transducer
- Temperature Comparator Gives Threshold Temperature Alarm
- Power Reference Permits Airflow Diagnostics
- Precision 2.5V Power Reference Permits Airflow Diagnostics
- Transducer Output is Easily Scaled for Increased Sensitivity
- Low 2.5mA Quiescent Current

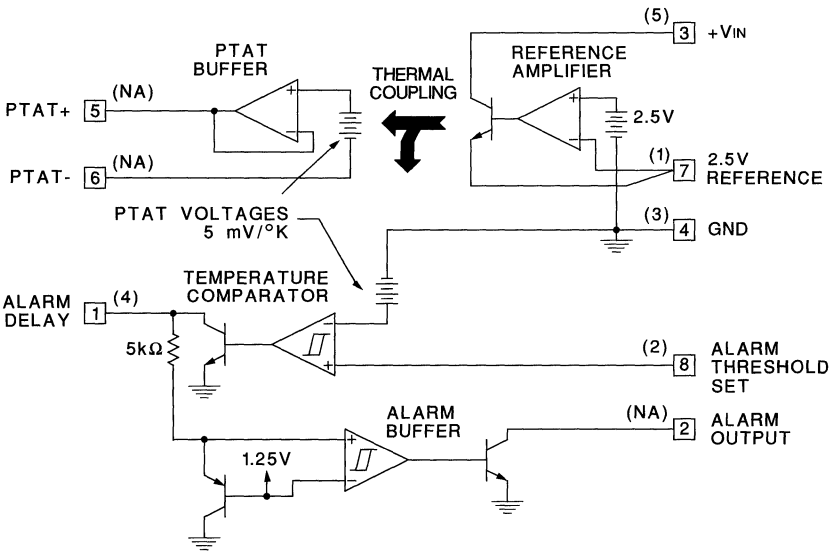
DESCRIPTION

The UC1730 family of integrated circuit devices are designed to be used in a number of thermal monitoring applications. Each IC combines a temperature transducer, precision reference, and temperature comparator allowing the device to respond with a logic output if temperatures exceed a user programmed level. The reference on these devices is capable of supplying in excess of 250mA of output current – by setting a level of power dissipation the rise in die temperature will vary with airflow past the package, allowing the IC to respond to airflow conditions

These devices come in an 8-Pin DIP, plastic or ceramic, a 5-Pin TO-220 or a PLCC-20 version. In the 8-Pin version, a PTAT (proportional to absolute temperature) output reports die temperature directly. This output is configured such that its output level can be easily scaled up with two external gain resistors. A second PTAT source is internally referenced to the temperature comparator. The other input to this comparator can then be externally programmed to set a temperature threshold. When this temperature threshold is exceeded an alarm delay output is activated. Following the activation of the delay output, a separate open collector output is turned on. The delay pin can be programmed with an external RC to provide a time separation between activation of the delay pin and the alarm pin, permitting shutdown diagnostics in applications where the open collector outputs of multiple parts are wire OR'ed together.

The 5-Pin version in the TO-220 package is well suited for monitoring heatsink temperatures. Enhanced airflow sensitivities can be obtained with this package by mounting the device to a small heatsink in the airstream. This version of the device does not include the PTAT output or the open collector alarm output.

BLOCK DIAGRAM



Pin numbers shown for 8-Pin DIP, ( ) number for 5-Pin TO-220.

10/94

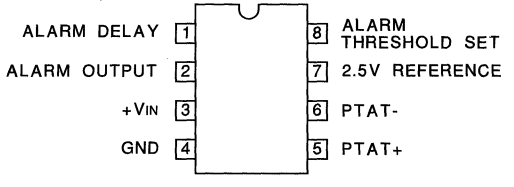
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN) 40V
Alarm Output Voltage (8-Pin Version Only) 40V
Alarm Delay Voltage 10V
Alarm Threshold Set Voltage 10V
2.5V Reference Output Current . . . . . -400 mA
Alarm Output Current (8-Pin Version Only) . . . . . 0 mA
Power Dissipation at TA = 25°C (Note 2) . . . . . 1000 mW
Power Dissipation at TC = 25°C (Note 2) . . . . . 2000 mW
Thermal Resistance Junction to Ambient
N, 8-Pin Plastic DIP . . . . . 110°C/W
J, 8-Pin Ceramic DIP . . . . . 110°C/W
T, 5-Pin Plastic DIP TO-220 . . . . . 65°C/W
Thermal Resistance Junction to Case
N, 8-Pin Plastic DIP . . . . . 60°C/W
J, 8-Pin Ceramic DIP . . . . . 40°C/W
T, 5-Pin Plastic TO-220 . . . . . 5°C/W
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

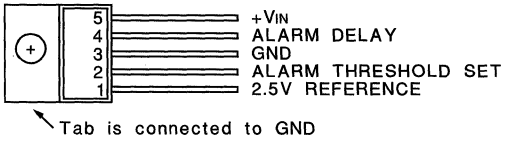
Note 1: Voltages are referenced to ground. Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

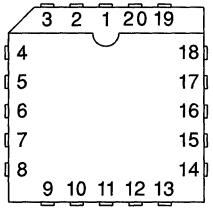
DIL-8 (TOP VIEW)
N or J Package



5-PIN TO-220 (TOP VIEW)
T Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1-3
ALARM DELAY	4
ALARM OUTPUT	5
+VIN	6
GND	7
N/C	8-13
PTAT+	14
PTAT-	15
2.5V REFERENCE	16
2.5V REFERENCE	17
ALARM THRESHOLD SET	18
N/C	19-20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TJ = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, +VIN = + 5V, and PTAT– = 0V. TA = TJ.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
Supply Current	+VIN = 35V		2.8	4.0	mA
	+VIN = 5V		2.3	3.5	mA
REFERENCE					
Output Voltage	TJ = 25°C	2.475	2.5	2.525	V
	Over Temperature	2.46		2.54	V
Load Regulation	IOUT = 0 to 250mA		8.0	25	mV
Line Regulation	+VIN = 5 to 25V		1.0	5.0	mV
TEMPERATURE COMPARATOR					
Temperature Comparator Threshold	at 300°K (26.85°C), Nominally 5mV/°K, VINPUT High to Low	1.475	1.50	1.525	V
Temperature Error		-10		10	°C
Threshold Line Regulation	+VIN = 5 to 25V		0.005	0.02	%/V
Temperature Linearity	Note 2		2.0	5.0	°C
Threshold Hysteresis		3.0	8.0	15	mV
Input Bias Current	VINPUT at 1.5V	-0.5	-0.1		µA
Max Output Current	VOUT = 1V	1.2	3.0		mA

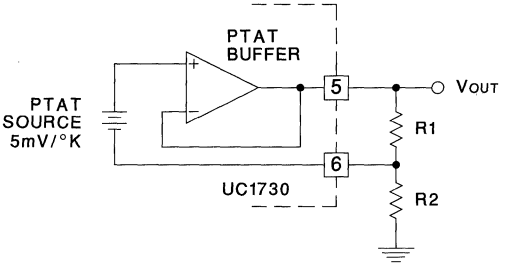
ELECTRICAL CHARACTERISTICS (cont): Unless otherwise stated, these specifications apply for T_J = 0°C to +100°C for the UC3730, -25°C to + 100°C for the UC2730 and -55°C to +125°C for the UC1730, +V_{IN} = + 5V, and PTAT– = 0V. $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE COMPARATOR (cont.)					
Output Leakage Current	V_{OUT} = 1V		0.01	1.0	µA
PTAT BUFFER (8-Pin N, or J Version Only)					
Output Voltage	at 300°K (26.85°C), Nominally 5mV/°K	1.460	1.50	1.54	V
	In 10X Config. + V_{IN} = 25V	14.6	15	15.4	V
Temperature Error		-12		12	°C
Temperature Linearity (Note 2)			2.0	5.0	°C
Line Regulation	+V_{IN} = 5 to 25V		0.02	0.04	%/V
Load Regulation	I_{OUT} = 0 to 2mA		1.0	3.0	mV
Dropout Voltage	PTAT + TO +V_{IN}		1.9	2.5	V
Input Bias Current at PTAT– Input		-3.0	-1.0		µA
ALARM BUFFER COMPARATOR (8-Pin N, or J Version Only)					
Threshold Voltage (V_{TH})	Alarm Delay Input Low to High	1.1	1.2	1.3	V
Threshold Hysteresis Voltage	Alarm Delay Voltage > V_{TH}		100	250	mV
Input Bias Current	Alarm Delay Voltage < V_{TH}		0.1	0.5	µA
Max Output Current	V_{OUT} = 1V	7.0	15		mA
Output Sat Voltage	I_{OUT} = 3mA		0.25	0.45	V

Note 2: This parameter is guaranteed by design and is not tested in production.

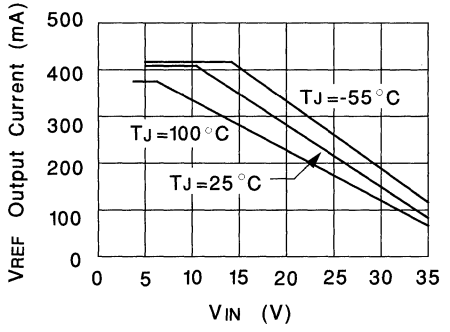
APPLICATIONS AND OPERATION INFORMATION

Scaling the PTAT Output (8 Pin Version Only)

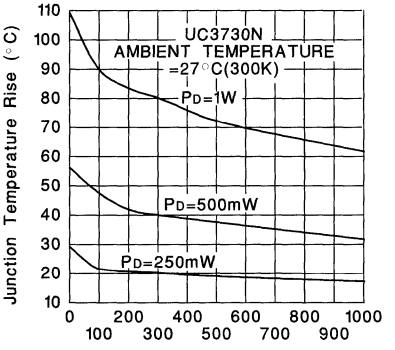


$$VOUT = 5 \times \left(1 + \frac{R2}{R1}\right) mV / °K$$

(Recommended Range for R1 is 2k to 4k)



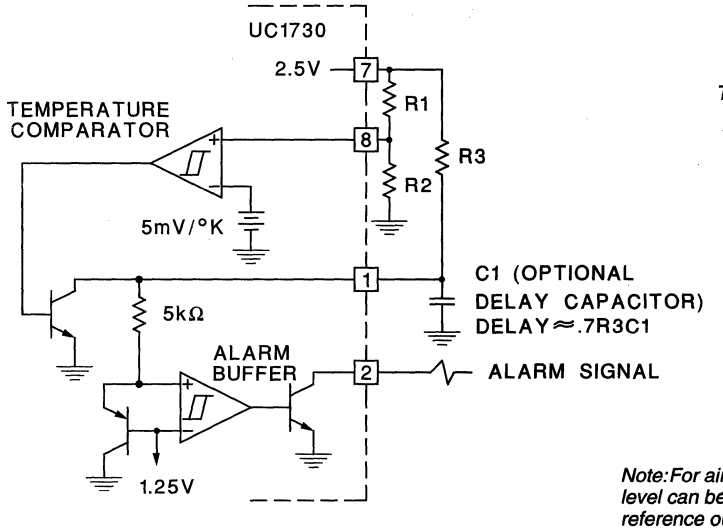
V_{REF} Maximum Output Current vs Input Supply



Junction Temperature Rise vs Airflow UC3730N (8-Pin Plastic Dip)

APPLICATIONS AND OPERATION INFORMATION (Cont.)

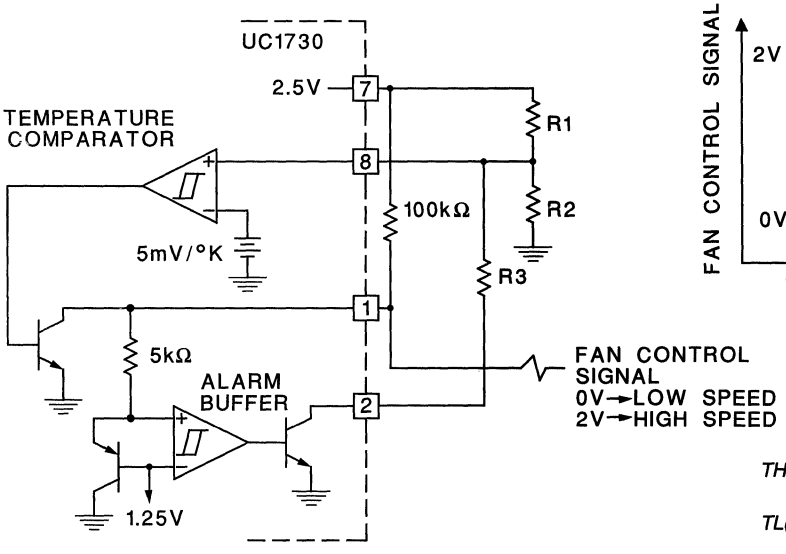
Setting a Temperature Threshold

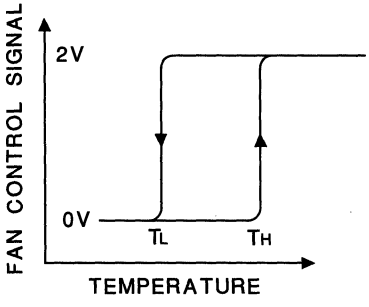


$$\text{Temperature Threshold (°C)} = \left(\frac{2.5V}{0.005}\right) x \frac{R2}{R1+R2} - 273.15$$

Note: For airflow monitoring a power dissipation level can be set with a resistive load, R_L, on the reference output.

Dual Speed Fan Control





$$TH(°C) = \frac{2.5V}{0.005} x \frac{R2}{R1+R2} - 273.15$$

$$TL(°C) = \frac{2.5V}{0.005} x \frac{RX}{R1+RX} - 273.15$$

$$\text{Where: } RX = R2 \times \frac{R3}{R2+R3}$$

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application INFO available

UC1901
UC2901
UC3901

Isolated Feedback Generator

FEATURES

- An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal
- Low-Cost Alternative to Optical Couplers
- Internal 1% Reference and Error Amplifier
- Internal Carrier Oscillator Usable to 5mHz
- Modulator Synchronizable to an External Clock
- Loop Status Monitor

DESCRIPTION

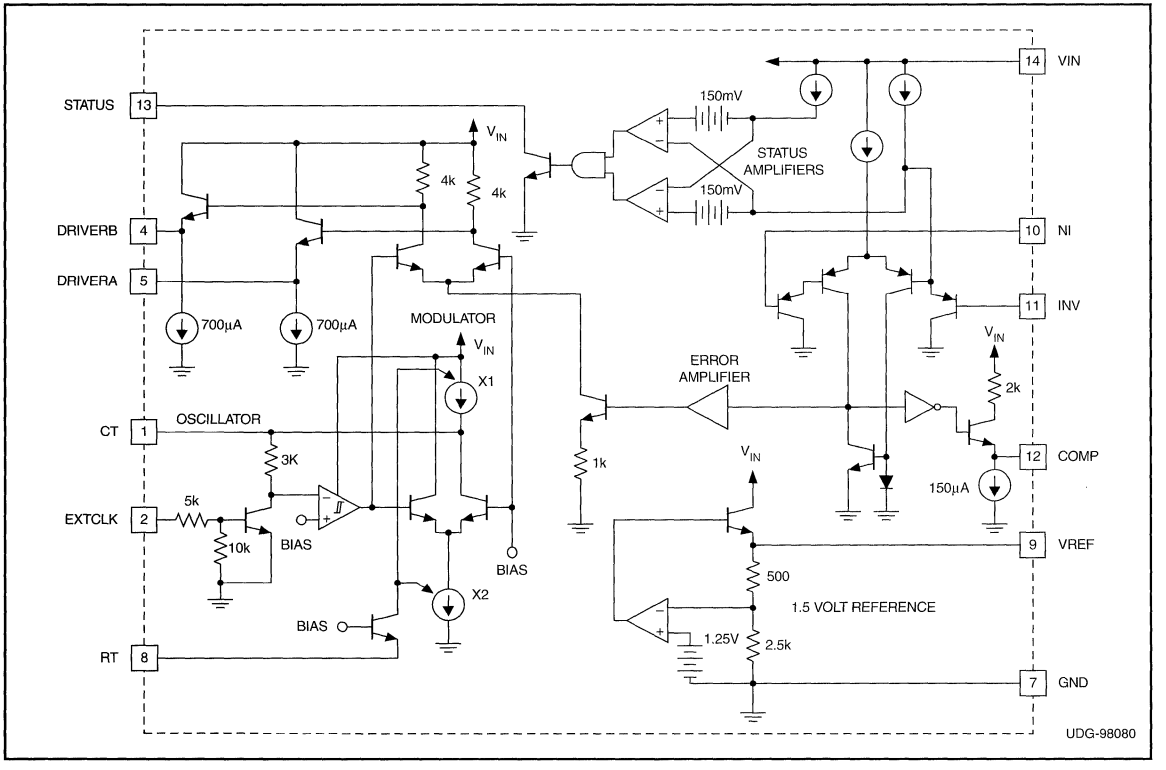
The UC1901 family is designed to solve many of the problems associated with closing a feedback control loop across a voltage isolation boundary. As a stable and reliable alternative to an optical coupler, these devices feature an amplitude modulation system which allows a loop error signal to be coupled with a small RF transformer or capacitor.

The programmable, high-frequency oscillator within the UC1901 series permits the use of smaller, less expensive transformers which can readily be built to meet the isolation requirements of today's line-operated power systems. As an alternative to RF operation, the external clock input to these devices allows synchronization to a system clock or to the switching frequency of a SMPS.

An additional feature is a status monitoring circuit which provides an active-low output when the sensed error voltage is within ±10% of the reference. The DRIVERA output, DRIVERB output, and STATUS output are disabled until the input supply has reached a sufficient level to allow proper operation of the device.

Since these devices can also be used as a DC driver for optical couplers, the benefits of 4.5 to 40V supply operation, a 1% accurate reference, and a high gain general purpose amplifier offer advantages even though an AC system may not be desired.

UC1901 SIMPLIFIED SCHEMATIC



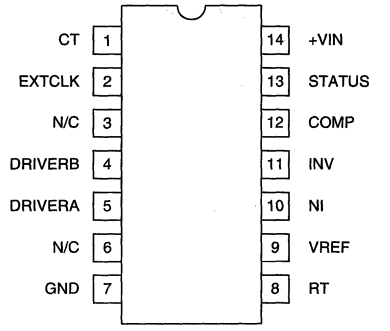
ABSOLUTE MAXIMUM RATINGS *(Note 1)*

Input Supply Voltage, V_{IN} 40V
Reference Output Current ..... –10mA
Driver Output Currents ..... –35mA
Status Indicator Voltage 40V
Status Indicator Current 20mA
Ext. Clock Input 40V
Error Amplifier Inputs ..... –0.5V to +35V
Power Dissipation at T_A = 25°C 1000mW
Power Dissipation at T_C = 25°C 2000mW
Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... 300°C

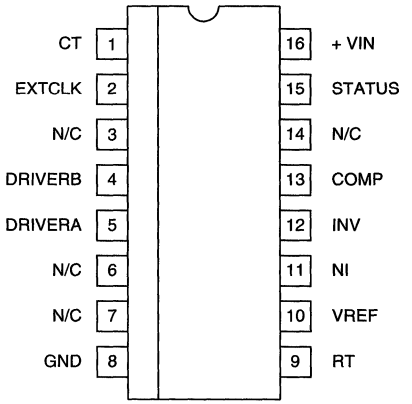
Note 1: Voltages are referenced to ground, Pin 7. Currents are positive into, negative out of the specified terminal.

CONNECTION DIAGRAMS

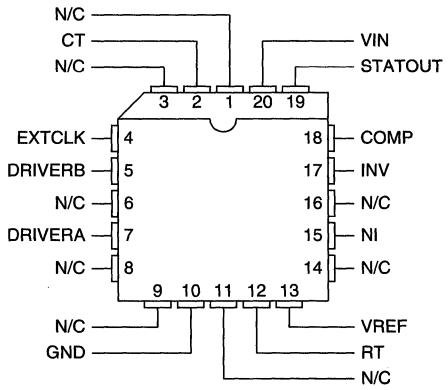
DIL-14, SOIC-14 (TOP VIEW)
J or N Package, D Package



SOIC-16 Wide (TOP VIEW)
DW Package



PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



TEMPERATURE AND PACKAGE SELECTION GUIDE

	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1901	–55°C to +125°C	J, L
UC2901	–40°C to +85°C	D, DW, J, N, Q
UC3901	0°C to +70°C	D, DW, J, N, Q

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for V_{IN} = 10V, R_T = 10kΩ, C_T = 820pF, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1901/UC2901			UC3901			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	T_J = 25°C	1.485	1.5	1.515	1.47	1.5	1.53	V
	$T_{MIN} \le T_J \le T_{MAX}$	1.470	1.5	1.530	1.455	1.5	1.545	
Line Regulation	V_{IN} = 4.5 to 35V		2	10		2	15	mV
Load Regulation	I_{OUT} = 0 to 5mA		4	10		4	15	mV
Short Circuit Current	T_J = 25°C		–35	–55		–35	–55	mV
Error Amplifier Section (To Compensation Terminal)								
Input Offset Voltage	V_{CM} = 1.5V		1	4		1	8	mV
Input Bias Current	V_{CM} = 1.5V		–1	–3		–1	–6	µA
Input Offset Current	V_{CM} = 1.5V		0.1	1		0.1	2	µA
Small Signal Open Loop Gain		40	60		40	60		dB
CMRR	V_{CM} = 0.5 to 7.5V	60	80		60	80		dB
PSRR	V_{IN} = 2 to 25V	80	100		80	100		dB
Output Swing, Δ Vo		0.4	0.7		0.4	0.7		V
Maximum Sink Current		90	150		90	150		µA
Maximum Source Current		–2	–3		–2	–3		mA
Gain Band Width Product			1			1		MHz
Slew Rate			0.3			0.3		V/µS
Modulators/Drivers Section (From Compensation Terminal)								
Voltage Gain		11	12	13	10	12	14	dB
Output Swing		±1.6	±2.8		±1.6	±2.8		V
Driver Sink Current		500	700		500	700		µA
Driver Source Current		–15	–35		–15	–35		mA
Gain Band Width Product			25			25		MHz
Oscillator Section								
Initial Accuracy	T_J = 25°C	140	150	160	130	150	170	kHz
	$T_{MIN} \le T_J \le T_{MAX}$	130		170	120		180	kHz
Line Sensitivity	V_{IN} = 5 to 35V		.15	.35		.15	.60	%/V
Maximum Frequency	R_T = 10k, C_T = 10pF		5			5		MHz
Ext. Clock Low Threshold	Pin 1 (C_T) = V_{IN}	0.5			0.5			V
Ext. Clock High Threshold	Pin 1 (C_T) = V_{IN}			1.6			1.6	V
Status Indicator Section								
Input Voltage Window	@ E/A Inputs, V_{CM} = 1.5V	±135	±150	±165	±130	±150	±170	mV
Saturation Voltage	E/A Δ Input = 0V, I_{SINK} = 1.6mA			0.45			0.45	V
Max. Output Current	Pin 13 = 3V, E/A Δ Input = 0.0V	8	15		8	15		mA
Leakage Current	Pin 13 = 40V, E/A ΔInput = 0.2V		.05	1		.05	5	µA
Supply Current	V_{IN} = 35V		5	8		5	10	mA
UVLO Section								
Drivers Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Status Output Enabled Threshold	At Input Supply V_{IN}		3.9	4.5		3.9	4.5	V
Change in Reference Output	When V_{IN} Reaches UVLO Threshold		–2	–30		–2	–30	mV

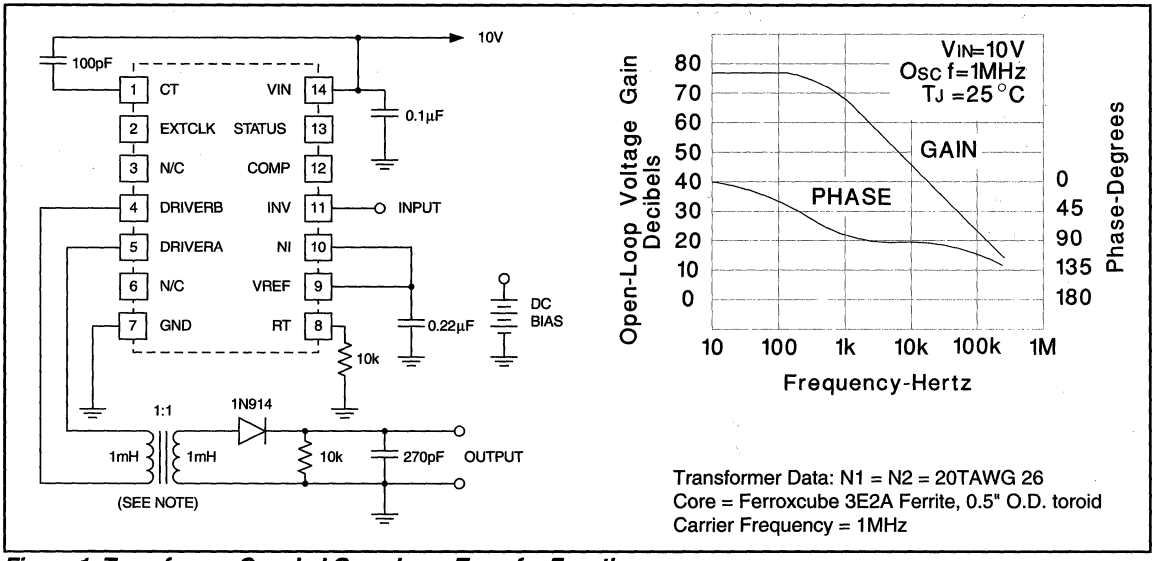


Figure 1. Transformer Coupled Open Loop Transfer Function

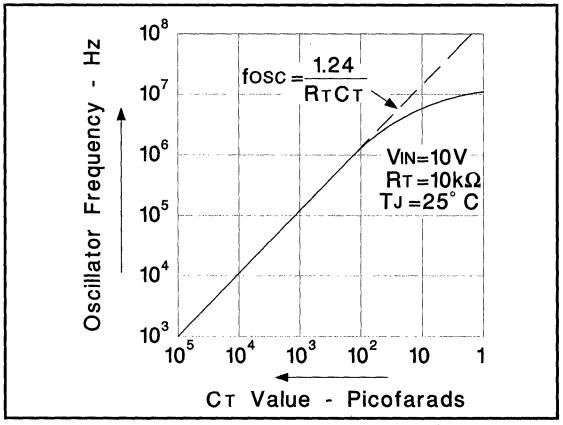


Figure 2. Oscillator Frequency

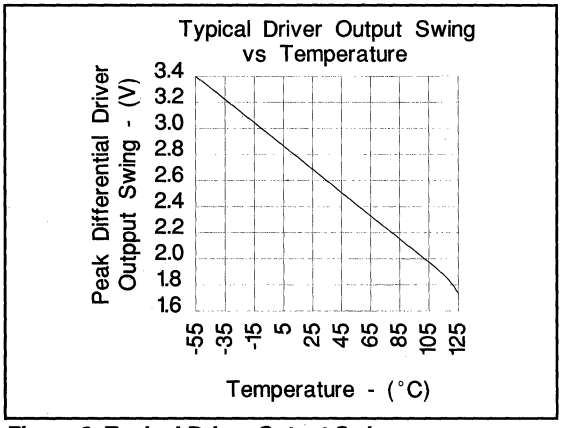


Figure 3. Typical Driver Output Swing vs Temperature

APPLICATION INFORMATION

The error amplifier compensation terminal, Pin 12, is intended as a source of feedback to the amplifier's inverting input at Pin 11. For most applications, a series DC blocking capacitor should be part of the feedback network. The amplifier is internally compensated for unity feedback.

The waveform at the driver outputs is a squarewave with an amplitude that is proportional to the error amplifier input signal. There is a fixed 12dB of gain from the error amplifier compensation pin to the modulator driver outputs. The frequency of the output waveform is controlled by either the internal oscillator or an external clock signal. With the internal oscillator the squarewave will have a fixed 50% duty cycle. If the internal oscillator is disabled by connecting Pin 1, C_R, to V_{IN} then the frequency and duty cycle of the output will be determined by the input clock waveform at Pin 2. If the oscillator remains disabled and there is not clock input at Pin 2, there will be a linear 12dB of signal gain to one or the other of the driver outputs depending on the DC state of Pin 2.

The driver outputs are emitter followers which will source a minimum of 15mA of current. The sink current, internally limited at 700µA, can be increased by adding resistors to ground at the driver outputs.

APPLICATION INFORMATION (continued)

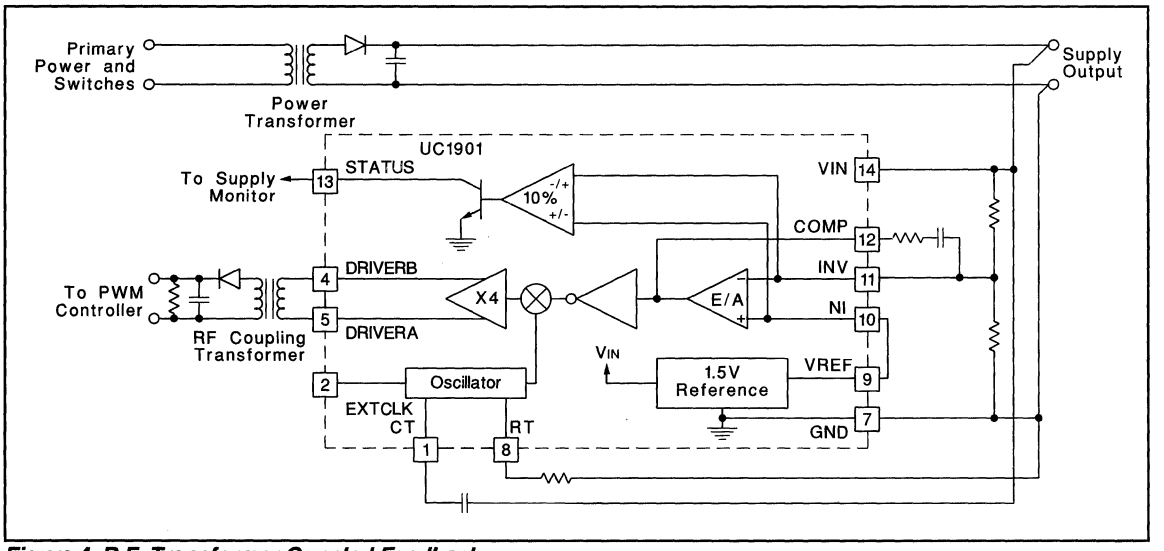


Figure 4. R.F. Transformer Coupled Feedback

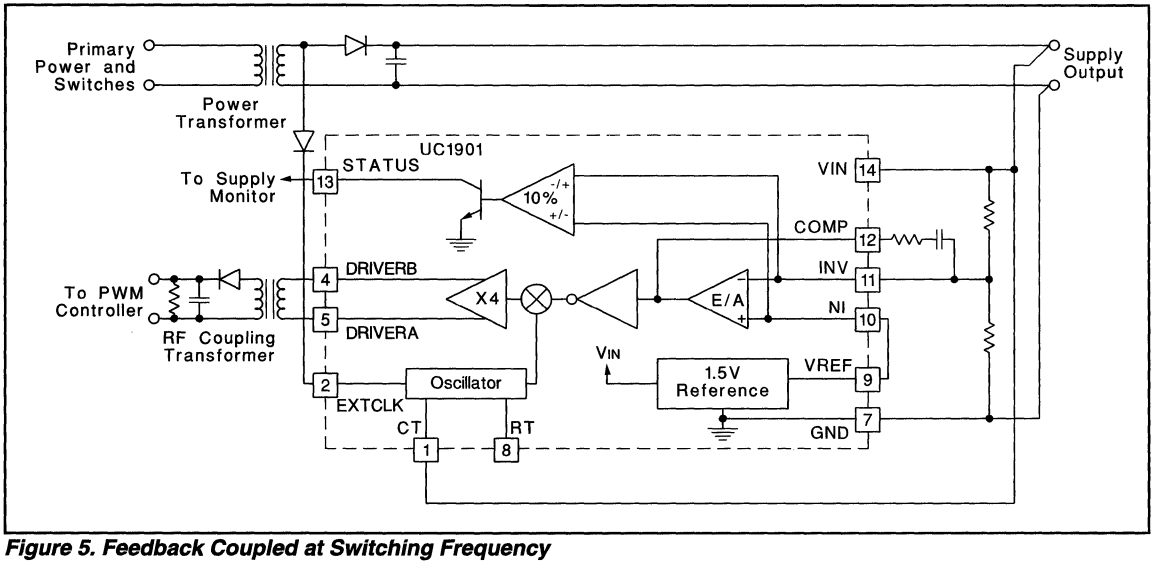


Figure 5. Feedback Coupled at Switching Frequency

TYPICAL APPLICATION

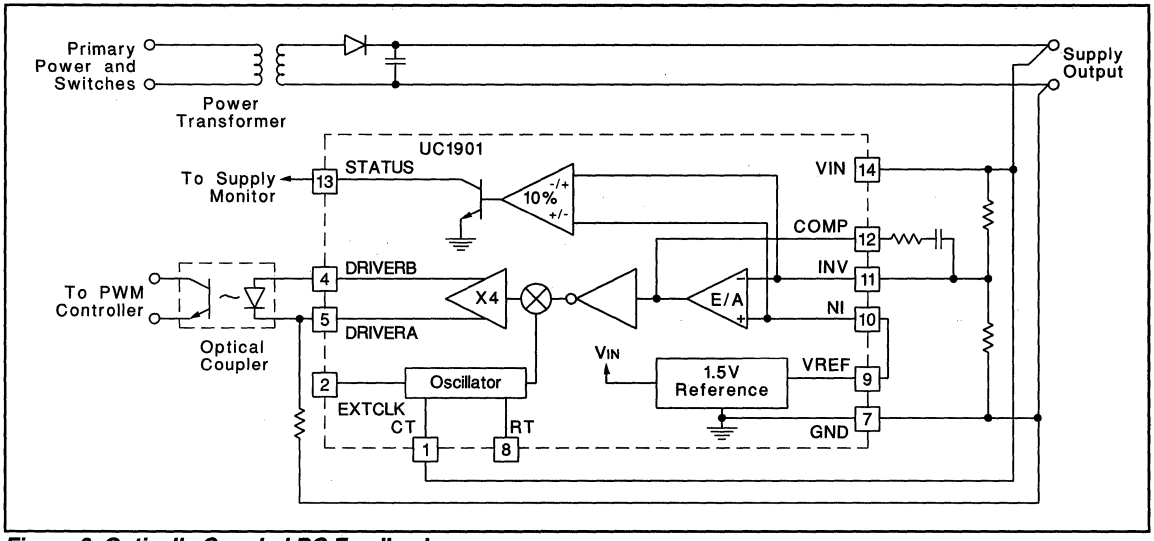


Figure 6. Optically Coupled DC Feedback

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application INFO available

UC1902
UC2902
UC3902
PRELIMINARY

Load Share Controller

FEATURES

- 2.7V to 20V Operation
- 8-Pin Package
- Requires Minimum Number of External Components
- Compatible with Existing Power Supply Designs Incorporating Remote Output Voltage Sensing
- Differential Share Bus
- Precision Current Sense Amplifier with Gain of 40
- UVLO (Undervoltage Lockout) Circuitry
- User Programmable Share Loop Compensation

DESCRIPTION

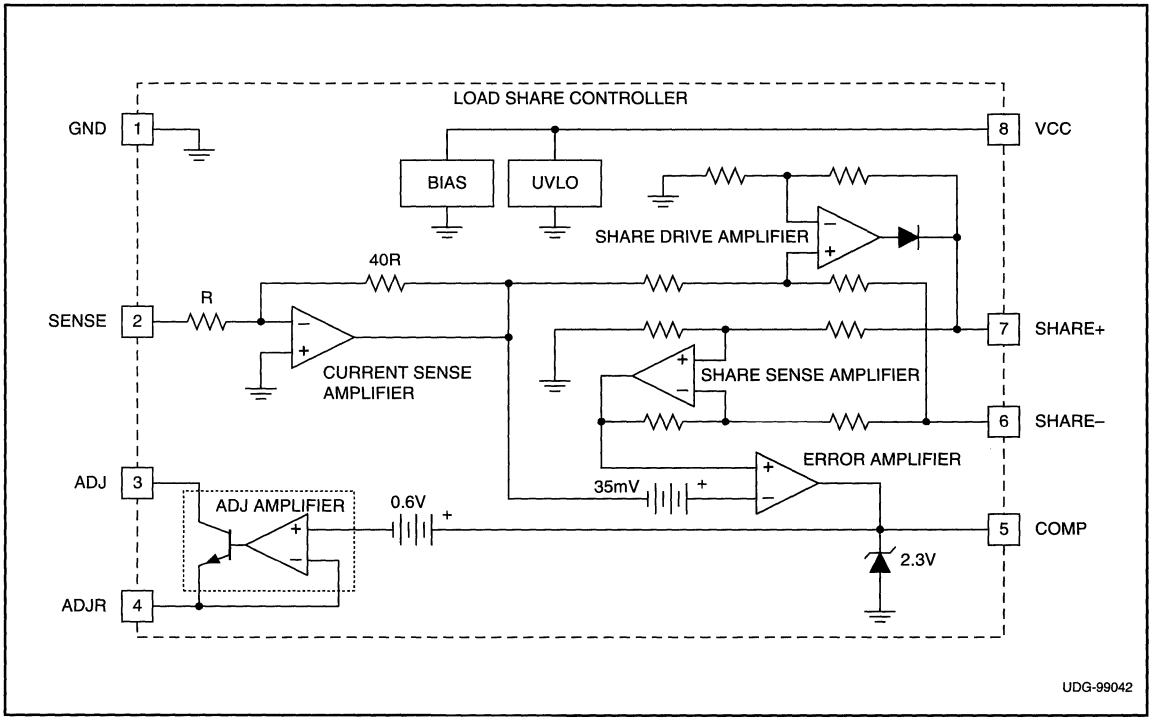
The UC3902 load share controller is an 8-pin device that balances the current drawn from independent, paralleled power supplies. Load sharing is accomplished by adjusting each supply's output current to a level proportional to the voltage on a share bus.

The master power supply, which is automatically designated as the supply that regulates to the highest voltage, drives the share bus with a voltage proportional to its output current. The UC3902 trims the output voltage of the other paralleled supplies so that they each support their share of the load current. Typically, each supply is designed for the same current level although that is not necessary for use with the UC3902. By appropriately scaling the current sense resistor, supplies with different output current capability can be paralleled with each supply providing the same percentage of their output current capability for a particular load.

A differential line is used for the share bus to maximize noise immunity and accommodate different voltage drops in each power converter's ground return line. Trimming of each converter's output voltage is accomplished by injecting a small current into the output voltage sense line, which requires a small resistance (typically 20Ω – 100Ω) to be inserted.

7

BLOCK DIAGRAM



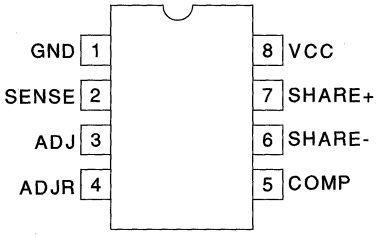
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (ADJ and VCC) ..... –0.3V to 20V
SENSE Voltage ..... –5V to +5V
ADJR, COMP Voltage..... –0.3V to +4V
SHARE–, SHARE+ Voltages ..... –0.3V to 10V
SHARE+ Current ..... –100mA to +10mA
ADJ Current..... –1mA to +30mA
Storage Temperature ..... –65°C to +150°C
Junction Temperature..... –55°C to +150°C
Lead Temperature (Soldering, 10sec.) ..... +300°C

All voltages are with respect to pin 1. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N, J and D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to +125°C for UC1902, –40°C to+85°C for UC2902, 0°C to 70°C for UC3902, VCC = 5V, R_{ADJR} = 1kΩ, V_{ADJ} = 5V, COMP = 5nF capacitor to GND, V_{SHARE-} = 0V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply					
Supply Current	SHARE+ = 1V, SENSE = 0V		4	6	mA
	VCC = 20V		6	10	mA
Undervoltage Lockout					
Startup Voltage	SHARE+ = 0.2V, SENSE = 0V, COMP = 1V	2.3	2.5	2.7	V
Hysteresis	SHARE+ = 0.2V, SENSE = 0V, COMP = 1V	60	100	140	mV
Current Sense Amplifier					
Input Offset Voltage	0.1V ≤ SHARE+ ≤ 1.1V	–2.5	–0.5	1.5	mV
Gain SENSE to SHARE	0.1V ≤ SHARE+ ≤ 1.1V	–41	–40	-39	V/V
Input Resistance		0.6	1	1.5	kΩ
Share Drive Amplifier					
SHARE+ High	VCC = 2.5V, SENSE = –50mV, I_{SHARE+} = –1mA	1.2	1.4		V
	VCC = 12V, SENSE = –250mV, I_{SHARE+} = –1mA	9.6	10	10.4	V
	VCC = 20V, SENSE = –250mV, I_{SHARE+} = –1mA	9.6	10	10.4	V
SHARE+ Low	VCC = 2.5V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
	VCC = 12V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
	VCC = 20V, SENSE = +10mV, I_{SHARE+} = –1mA		20	50	mV
SHARE+ Output Voltage	Measures SHARE+, SENSE = 0mV, R_{SHARE+} = 200Ω resistor SHARE+ to GND		20	40	mV
CMRR	0 ≤ SHARE– ≤ 1V , SENSE used as input to amplifier	50	90		dB
Load Regulation	Load on SHARE+, –1mA ≤ I_{LOAD} ≤ –20mA, SENSE = –25mV		0	20	mV
Short Circuit Current	SHARE+ = 0V, SENSE = –25mV	–85	–50	–20	mA
Slew Rate	SENSE = +10mV to –90mV Step, 200Ω resistor SHARE+ to GND	0.16	0.27	0.37	V/µs
	SENSE = –90mV to +10mV Step, 200Ω resistor SHARE+ to GND	0.12	0.24	0.34	V/µs

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = –55°C to +125°C for UC1902, –40°C to+85°C for UC2902, 0°C to 70°C for UC3902, VCC = 5V, R_{ADJR} = 1kΩ, V_{ADJ} = 5V, COMP = 5nF capacitor to GND, V_{SHARE-} = 0V, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Share Sense Amplifier					
Input Impedance	SHARE+ = 1V, SHARE– = 1V, SENSE = +10mV	10	15		kΩ
	200Ω resistor SHARE+ to GND, SHARE– = 1V, SENSE = +10mV	15	17		kΩ
Threshold	SENSE = 0V	41	70	100	mV
CMRR SHARE	0 ≤ SHARE– ≤ 1V, SENSE = –2.5mV	50	60		dB
AVOL from SHARE+ to ADJR	SENSE = –2.5mV, 5nF capacitor COMP to GND, 1k resistor ADJR to GND	50	68		dB
	SENSE = –2.5mV, 5nF capacitor COMP to GND, 150Ω resistor ADJR to GND	50	66		dB
Slew Rate	SHARE+ = Step of 0mV to 300mV through a 200Ω resistor, R_{COMP} = 500Ω resistor to 1.5V, SENSE = 10mV	0.4	0.7	1	V/µs
Error Amplifier Section					
Transconductance, SHARE+ to COMP	200Ω resistor SHARE+ to GND	3.2	4.5	5.5	mS
IOH	COMP = 1.5V, SHARE+ ≥ +300mV, SENSE = +10mV	–400	–325	–230	µA
IOL	200Ω resistor SHARE+ to GND, COMP = 1.5V, SENSE = +10mV	100	150	200	µA
Input Offset Voltage		15	35	65	mV
Δ VIO/Δ V_{SENSE}	1k Resistor, ADJR to GND, –2.5mV < SENSE < –25mV	–6	0	6	mV/V
ADJ Amplifier					
ADJR Low Voltage	SENSE = +10mV, 200Ω resistor SHARE+ to GND	–1	0	1	mV
ADJR High Voltage	SENSE = +10mV, SHARE+ = 1V	1.4	1.8	2.1	V
Current Gain ADJR to ADJ	ADJR Current = –0.5mA, ADJ = 2.5V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –0.5mA, ADJ = 20V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –10mA, ADJ = 2.5V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A
	ADJR Current = –10mA, ADJ = 20V, SENSE = +10mV, SHARE+ = 1V	0.96	0.99	1	A/A

PIN DESCRIPTIONS

ADJ: Current output of adjust amplifier circuit (NPN collector).

ADJR: Current adjust amplifier range set (NPN emitter).

COMP: Output of error amplifier, input of adjust amplifier. This is where the compensation capacitor is connected.

GND: Local power supply return and signal ground.

SENSE: Inverting input of current sense amplifier.

SHARE+: Positive input from share bus or drive to share bus.

SHARE-: Reference for SHARE+.

VCC: Local power supply (positive).

APPLICATION INFORMATION

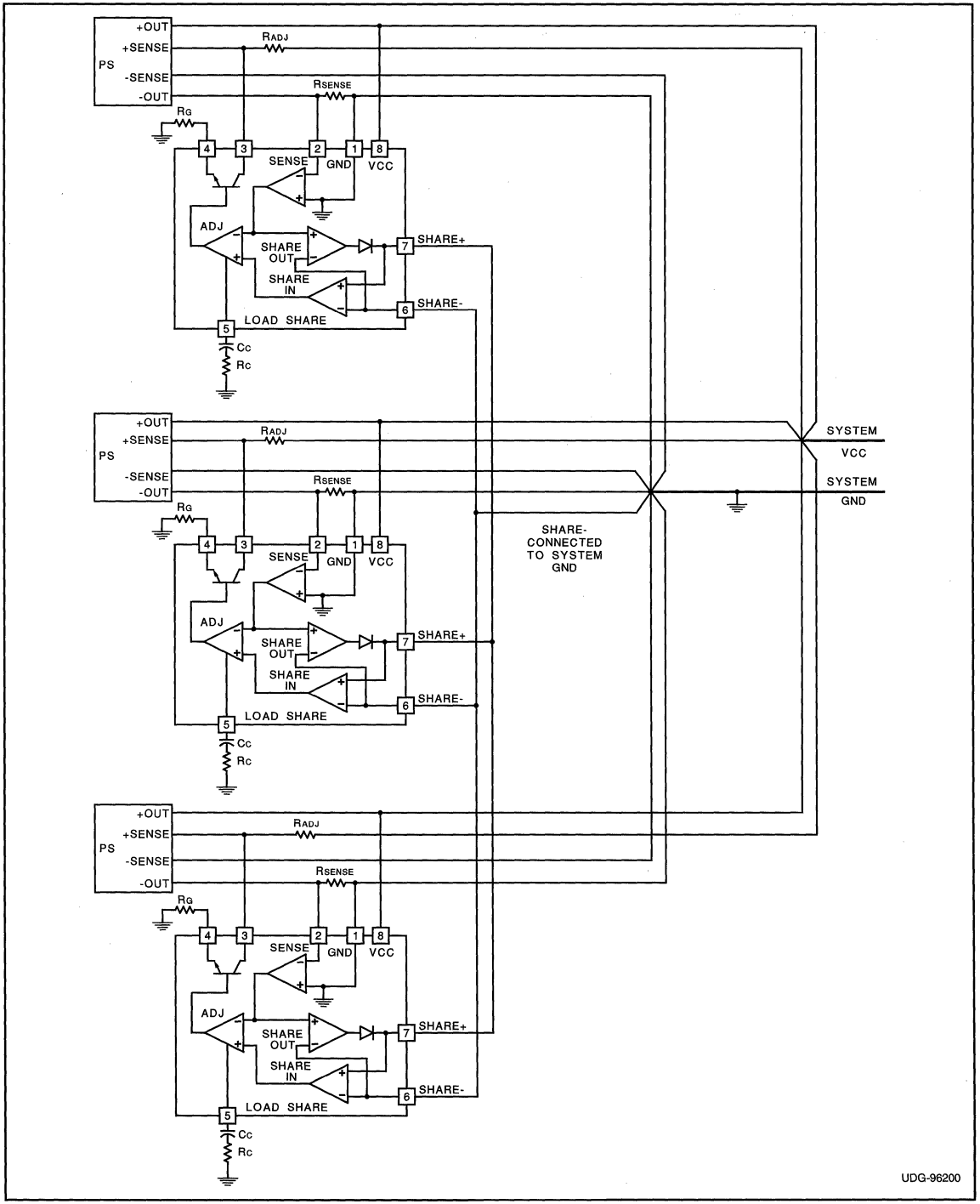


Figure 1. Typical application.

APPLICATION INFORMATION (cont.)

The values of five passive components must be determined to configure the UC3902 load share controller. The output and return lines of each converter are connected together at the load, with current sense resistor R_{SENSE} inserted in each negative return line. Another resistor, R_{ADJ}, is also inserted in each positive remote sense line. The differential share bus terminals (SHARE+ and SHARE–) of each UC3902 are connected together respectively, and the SHARE– node is also connected to the system ground. A typical application is illustrated in Figure 1.

The load share controller design can be executed by following the next few steps:

Step 1.

$$R_{SENSE} = \frac{V_{SHARE}(\max)}{A_{CSA} \bullet I_O(\max)}$$

where A_{CSA} is 40, the gain of the current sense amplifier.

At full load, the voltage drop across the R_{SENSE} resistor is I_O (max) • R_{SENSE}. Taking into account the gain of the current sense amplifier, the voltage at full load on the current share bus,

$$V_{SHARE}(\max) = A_{CSA} \bullet I_O(\max) \bullet R_{SENSE}.$$

This voltage must stay 1.5V below V_{CC} or below 10V whichever is smaller. V_{SHARE} represents an upper limit but the designer should select the full scale share bus voltage keeping in mind that every volt on the load share bus will increase the master controller's supply current by approximately 100mA times the number of slave units connected parallel.

Step 2.

$$R_G = \frac{V_{ADJ}(\max)}{I_{ADJ}(\max)}$$

Care must be taken to ensure that $I_{ADJ(max)}$ is low enough to ensure that both the drive current and power dissipation are within the UC3902's capability. For most applications, an $I_{ADJ(max)}$ current between 5mA and 10mA is acceptable. In a typical application, a 360Ω R_G resistor from the ADJR pin to ground sets $I_{ADJ(max)}$ to approximately 5mA.

Step 3.

$$RADJ = \frac{\Delta V_O(\max) - I_O(\max) \bullet R_{SENSE}}{I_{ADJ}(\max)}$$

R_{ADJ} must be low enough to not affect the normal operation of the converter's voltage feedback loop. Typical R_{ADJ} values are in the 20Ω to100Ω range depending on V_O, ΔV_O(max) and the selected I_{ADJ}(max) value.

Step 4.

$$C_C = \frac{G_M}{2 \bullet \pi \bullet fC} \bullet \frac{R_{ADJ}}{R_G} \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet A_{CSA} \bullet A_{PWR}(fC)$$

The share loop compensation capacitor, C_C is calculated to produce the desired share loop unity gain crossover frequency, fC. The share loop error amplifier's transconductance, G_M is nominally 4.5ms. The values of the resistors are already known. Typically, fC will be set at least an order of magnitude below the converter's closed loop bandwidth. The load share circuit is primarily intended to compensate for each converter's initial output voltage tolerance and temperature drift, not differences in their transient response. The term A_{PWR}(fC) is the gain of the power supply measured at the desired share loop crossover frequency, fC. This gain can be measured by injecting the measurement signal between the positive output and the positive sense terminal of the power supply.

Step 5.

$$R_C = \frac{1}{2 \bullet \pi \bullet fC \bullet C_C}$$

A resistor in series with Cc is required to boost the phase margin of the load share loop. The zero is placed at the load share loop crossover frequency, fc.

When the system is powered up, the converter with the highest output voltage will tend to source the most current and take control of the share bus. The other converters will increase their output voltages until their output currents are proportional to the share bus voltage minus 50mV. The converter which in functioning as the master may change due to warmup drift and differences in load and line transient response of each converter.

ADDITIONAL INFORMATION

Please refer to the following Unitrode topic for additional application information.

[1] Application Note U-163, *The UC3902 Load Share Controller and Its Performance in Distributed Power Systems* by Laszlo Balogh.

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application INFO available

UC1903
UC2903
UC3903

Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring up to Four Separate Supply Voltage Levels
- Internal Inverter for Sensing a Negative Supply Voltage
- Line/Switch Sense Input for Early Power Source Failure Warning
- Programmable Under- and Over-Voltage Fault Thresholds with Proportional Hysteresis
- A Precision 2.5V Reference
- General Purpose Op-Amp for Auxiliary Use
- Three High Current, >30mA, Open-Collector Outputs Indicate Over-Voltage, Under-Voltage and Power OK Conditions
- Input Supply Under-Voltage Sensing and Start-Latch Eliminate Erroneous Fault Alerts During Start-Up
- 8-40V Supply Operation with 7mA Stand-By Current

DESCRIPTION

The UC1903 family of quad supply and line monitor integrated circuits will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. An internal op-amp inverter allows at least one of these levels to be negative. A separate line/switcher sense input is available to provide early warning of line or other power source failures.

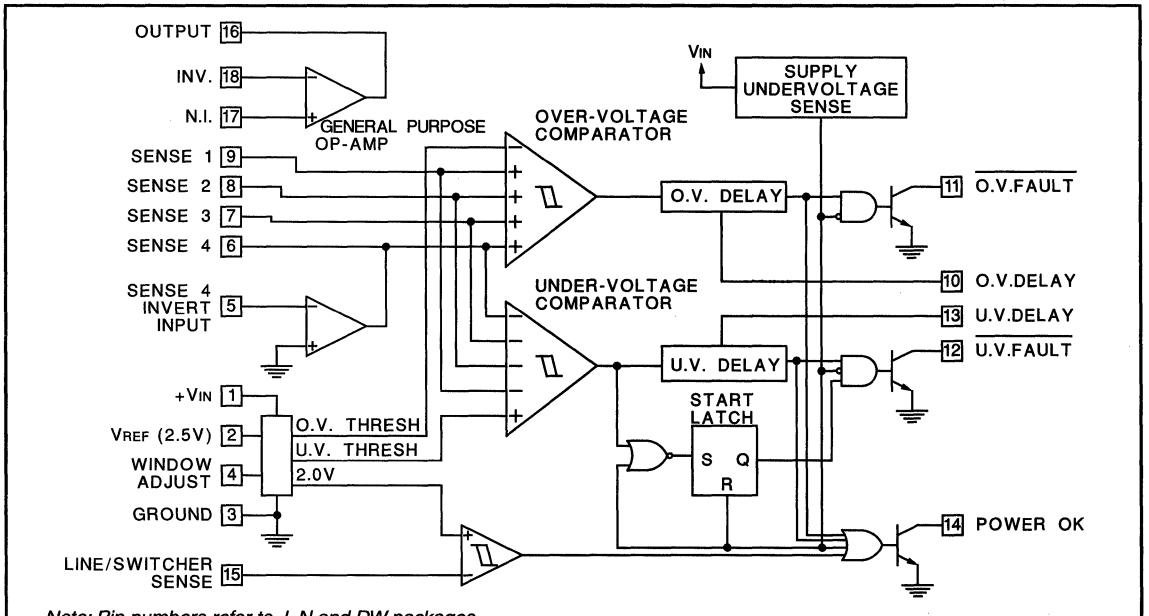
The fault window adjustment circuit on these devices provides easy programming of under- and over-voltage thresholds. The thresholds, centered around a precision 2.5V reference, have an input hysteresis that scales with the window width for precise, glitch-free operation. A reference output pin allows the sense input fault windows to be scaled independently using simple resistive dividers.

The three open collector outputs on these devices will sink in excess of 30mA of load current when active. The under- and over-voltage outputs respond after separate, user defined, delays to respective fault conditions. The third output is active during any fault condition including under- and over-voltage, line/switcher faults, and input supply under-voltage. The off state of this output indicates a "power OK" situation.

An additional, uncommitted, general purpose op-amp is also included. This op-amp, capable of sourcing 20mA of output current, can be used for a number of auxiliary functions including the sensing and amplification of a feedback error signal when the 2.5V output is used as a system reference.

In addition, these ICs are equipped with a start-latch to prevent erroneous under-voltage indications during start-up. These parts operate over an 8V to 40V input supply range and require a typical stand-by current of only 7mA.

BLOCK DIAGRAM



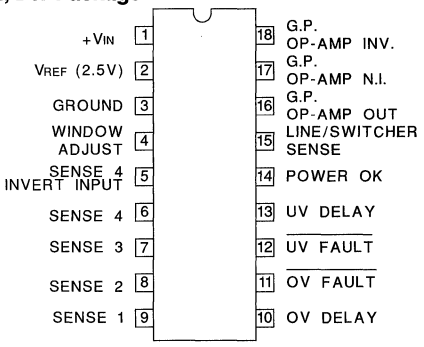
Note: Pin numbers refer to J, N and DW packages.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (+VIN) . . . . . +40V
Open Collector Output Voltages . . . . . +40V
Open Collector Output Currents 50mA
Sense 1-4 Input Voltages . . . . . -0.3V to +20V
Line/Switcher Sense Input Voltage . . . . . -0.3V to +40V
Op-Amp and Inverter Input Voltages . . . . . -0.3V to +40V
Op-Amp and Inverter Output Currents . . . . . -40mA
Window Adjust Voltage . . . . . 0.0V to +10V
Delay Pin Voltages . . . . . 0.0V to +5V
Reference Output Current . . . . . -40mA
Power Dissipation at TA = 25°C (Note 1) 1000mW
Power Dissipation at TC = 25°C (Note 1) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

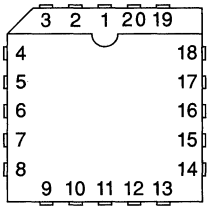
Note 1: Voltages are referenced to ground (Pin 3). Currents are positive into, negative out of, the specified terminals. Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20
(TOP VIEW)
Q, L Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
VREF (2.5V)	2
GROUND	3
GROUND	4
WINDOW ADJUST	5
N/C	6
SENSE 4 INVERT INPUT	7
SENSE 4	8
SENSE 3	9
SENSE 2	10
SENSE 1	11
OV DELAY	12
$\overline{\text{OV FAULT}}$	13
$\overline{\text{UV FAULT}}$	14
UV DELAY	15
POWER OK	16
LINE/SWITCHER SENSE	17
G.P. OP-AMP OUT	18
G.P. OP-AMP N.I.	19
G.P. OP-AMP INV.	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for TA = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; +VIN = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; VPIN 4 = 1.0V, TA = TJ.

PARAMETERS	TEST CONDITIONS	UC1903 / UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply								
Input Supply Current	No Faults		7	9		7	11	mA
	UV, OV and Line Fault		10	15		10	18	mA
Supply Under Voltage Threshold (VSUV)	Fault Outputs Enabled	6.0	7.0	7.5	5.5	7.0	8.0	V
Minimum Supply to Enable Power OK Output			3.0	4.0		3.0	4.0	V
Reference								
Output Voltage (VREF)	TJ = 25°C	2.485	2.5	2.515	2.470	2.5	2.530	V
	Over Temperature	2.465		2.535	2.465		2.535	V
Load Regulation	IL = 0 to 10mA		1	10		1	15	mV
Line Regulation	+VIN = 8 to 40V		1	4		1	8	mV
Short Circuit Current	TJ = 25°C		40			40		mA
Fault Thresholds (Note 4)								
OV Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = Low to High, 0.5V ≤ VPIN 4 ≤ 2.5V	.230	.25	.270	.230	.25	.270	V/V
UV Threshold Adj.	Offset from VREF as a function of VPIN 4 Input = High to Low, 0.5V ≤ VPIN 4 ≤ 2.5V	-.270	-.25	-.230	-.270	-.25	-.230	V/V

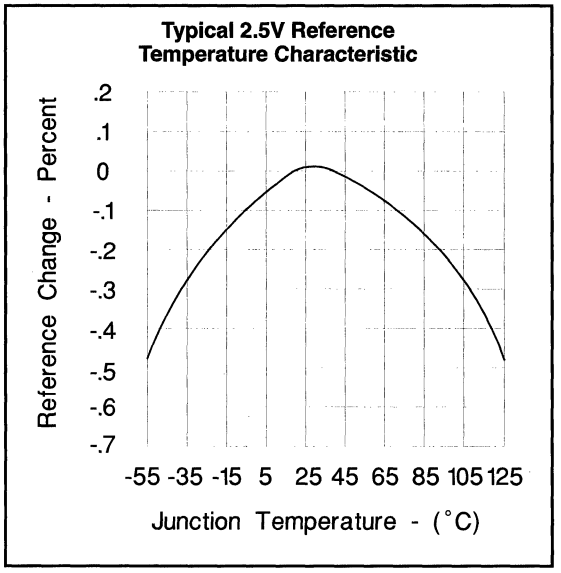
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1903; –40°C to +85°C for the UC2903; and 0°C to +70°C for the UC3903; $+V_{IN}$ = 15V; Sense Inputs (Pins 6–9 and Pin 15) = 2.5V; $V_{PIN\ 4}$ = 1.0V, T_A = T_J.

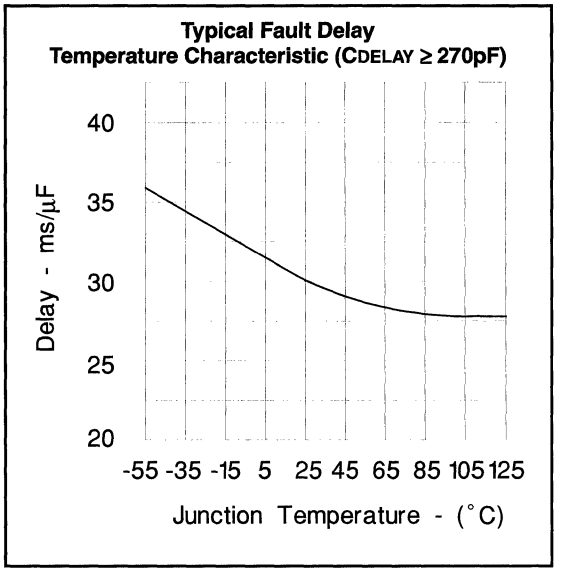
PARAMETERS	TEST CONDITIONS	UC1903/UC2903			UC3903			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Fault Thresholds (cont.)								
OV & UV Threshold Hyst.	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V	10	20	30	10	20	30	mV/V
OV & UV Threshold Supply Sensitivity	$+V_{IN}$ = 8V to 40V		.002	.01		.002	.02	%/V
Adjust Pin (Pin 4) Input Bias Current	0.5V ≤ $V_{PIN\ 4}$ ≤ 2.5V		±1	±10		±1	±12	µA/V
Line Sense Threshold	Input = High to Low	1.94	2.0	2.06	1.9	2.0	2.1	V
Line Sense Threshold Hyst.		125	175	225	100	175	250	mV
Sense Inputs								
Sense 1-4 Input Bias Current	Input = 2.8V (Note 2)		1	3		1	6	µA
	Input = 2.2 (Note 2)		-1	-3		-1	-6	µA
Line Sense Input Bias Current	Input = 2.3V (Note 2)		1	3		1	6	µA
OV and UV Fault Delay								
Charging Current			60			60		µA
Threshold Voltage	Delay Pin = Low to High		1.8			1.8		V
Threshold Hysteresis	T_J = 25°C		250			250		mV
Delay	Ratio of Threshold Voltage to Charging Current	20	30	50	20	30	50	ms/µF
Fault Outputs ($\overline{OV}$, $\overline{UV}$, & Power OK)								
Maximum Current	V_{OUT} = 2V	30	70		30	70		mA
Saturation Voltage	I_{OUT} = 12mA		.25	.40		.25	.40	V
Leakage Current	V_{OUT} = 40 V		3	25		3	25	µA
Sense 4 Inverter (Note 3)								
Input Offset Voltage			2	8		2	10	mV
Input Bias Current			.1	2		.1	4	µA
Open Loop Gain		65	80		65	80		dB
PSRR	$+V_{IN}$ = 8 to 40 V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA
G.P. Op-Amp (Note 3)								
Input Offset Voltage			1	5		1	8	mV
Input Bias Voltage			.1	2		.1	4	µA
Input Offset Current			.01	.5		.01	1.0	µA
Open Loop Gain		65	120		65	120		dB
CMRR	V_{CM} = 0 to $+V_{IN}$ = 2.0V	65	100		65	100		dB
PSRR	$+V_{IN}$ = 8 to 40V	65	100		65	100		dB
Unity Gain Frequency			1			1		MHz
Slew Rate			.4			.4		V/µs
Short Circuit Current	T_J = 25°C		40			40		mA

Note 2: These currents represent maximum input bias currents required as the sense inputs cross appropriate thresholds.

Note 3: When either the G.P. OP-Amp, or the Sense 4 Inverter, are configured for sensing a negative supply voltage, the divider resistance at the inverting input should be chosen such that the nominal divider current is ≤ 1.4mA. With the divider current at or below this level possible latching of the circuit is avoided. Proper operation for currents at or below 1.4mA is 100% tested in production.

Note 4: Reference to pin numbers in this specification pertain to 18 pin DIL N and J packages and 18 pin SOIC DW package.





OPERATION AND APPLICATION INFORMATION

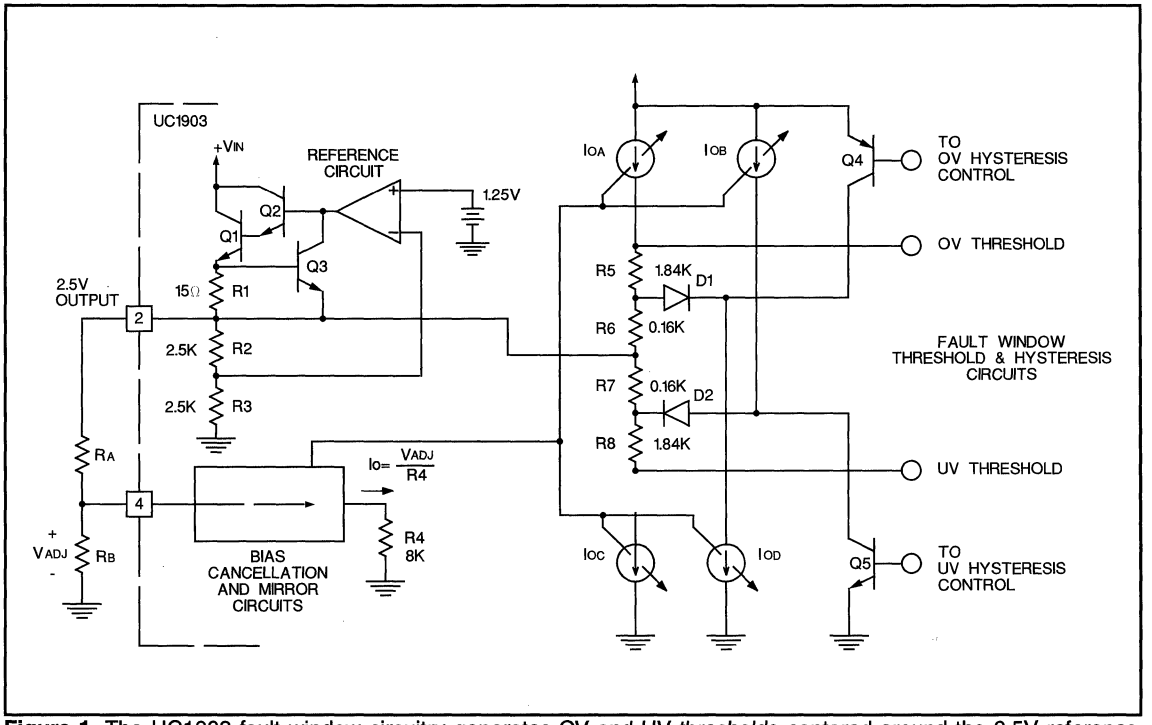


Figure 1. The UC1903 fault window circuitry generates OV and UV thresholds centered around the 2.5V reference. Window magnitude and threshold hysteresis are proportional to the window adjust input voltage at Pin 4.

OPERATION AND APPLICATION INFORMATION

Setting a Fault Window

The fault thresholds on the UC1903 are generated by creating positive and negative offsets, equal in magnitude, that are referenced to the chip's 2.5V reference. The resulting fault window is centered around 2.5V and has a magnitude equal to that of the applied offsets. Simplified schematics of the fault window and reference circuits are shown in Figure 1 (see previous page). The magnitude of the offsets is determined by the voltage applied at the window adjust pin, Pin 4. A bias cancellation circuit keeps the input current required at Pin 4 low, allowing the use of a simple resistive divider off the reference to set the adjust pin voltage.

The adjust voltage at Pin 4 is internally applied across R_4, and an 8k resistor. The resulting current is mirrored four times to generate current sources I_{OA}, I_{OB}, I_{OC}, and I_{OD}, all equal in magnitude. When all four of the sense inputs are inside the fault window, a no-fault condition, Q_4 and Q_5 are turned on. In combination with D_1 and D_2 this prevents L_{OB} and L_{OD} from affecting the fault thresholds. In this case, the OV and UV thresholds are equal to $V_{REF} + I_{OA}(R_5 + R_6)$ and $V_{REF} - I_{OC}(R_7 + R_8)$ respectively. The fault window can be expressed as:

$$(1) \qquad 2.5V \pm \frac{V_{ADJ}}{4}.$$

In terms of a sensed nominal voltage level, V_S, the window as a percent variation is:

$$(2) \qquad V_S \pm (10 \cdot V_{ADJ})\ \%.$$

When a sense input moves outside the fault window given in equation(1), the appropriate hysteresis control signal turns off Q_4 or Q_5. For the under-voltage case, Q_5 is disabled and current source I_{OB} flows through D_2. The net current through R_7 becomes zero as I_{OB} cancels I_{OC}, giving an 8% reduction in the UV threshold offset. The over-voltage case is the same, with Q_4 turning off, allowing I_{OD} to cancel the current flow, I_{OA}, through R_6. The result is a hysteresis at the sense inputs which is always 8% of the window magnitude. This is shown graphically in Figure 2.

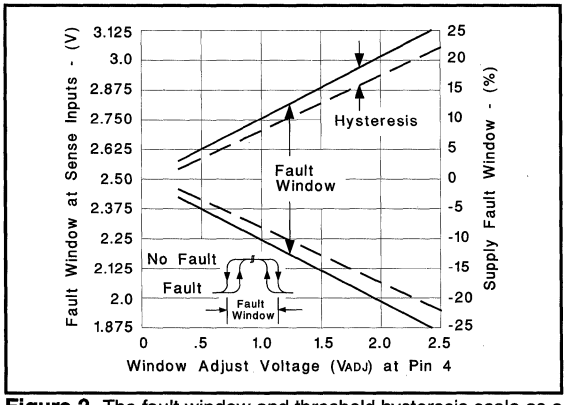


Figure 2. The fault window and threshold hysteresis scale as a function of the voltage applied at Pin 4, the window adjust pin.

Fault Windows Can Be Scaled Independently

In many applications, it may be desirable to monitor various supply voltages, or voltage levels, with varying fault windows. Using the reference output and external resistive dividers this is easily accomplished with the UC1903. Figures 3 and 4 illustrate how the fault window at any sense input can be scaled independently of the remaining inputs.

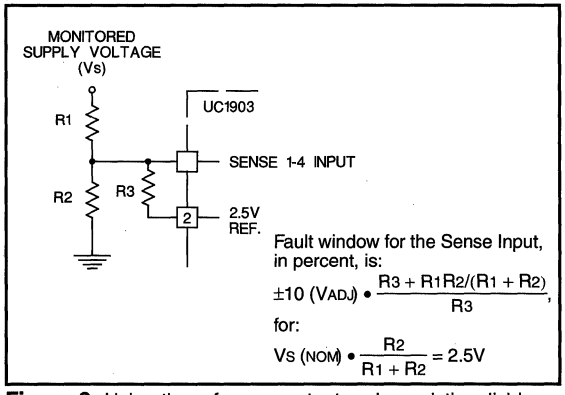


Figure 3. Using the reference output and a resistive divider, a sense input with an independently wider fault window can be generated.

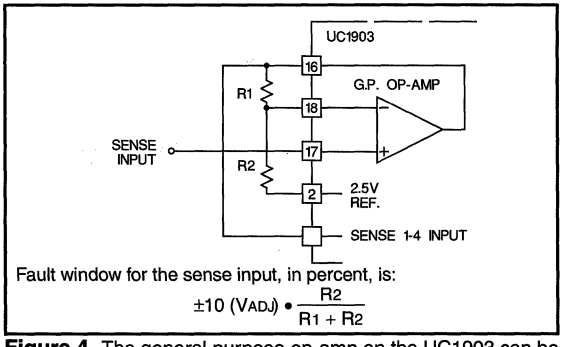


Figure 4. The general purpose op-amp on the UC1903 can be used to create a sense input with an independently tighter fault window.

Figure 4 demonstrates one of many auxiliary functions that the uncommitted op-amp on the UC1903 can be used for. Alternatively, this op-amp can be used to buffer high impedance points, perform logic functions, or for sensing and amplification. For example, the G.P. op-amp, combined with the 2.5V reference, can be used to produce and buffer an optically coupled feedback signal in isolated supplies with primary side control. The output stage of this op-amp is detailed in Figure 5. The NPN emitter follower provides high source current capability. ≥20mA while the substrate device, Q_3, provides good transient sinking capability.

OPERATION AND APPLICATION INFORMATION (continued)

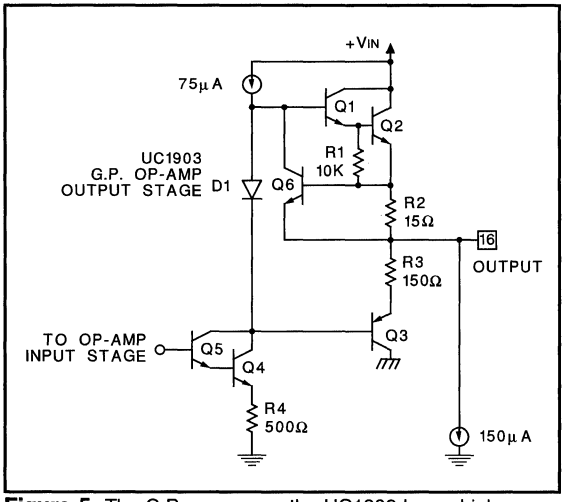
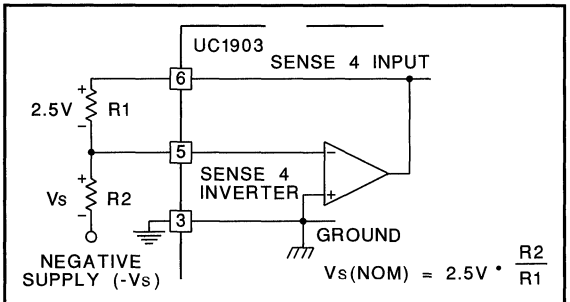


Figure 5. The G.P. op-amp on the UC1903 has a high source current (≥20mA) capability and enhanced transient sinking capability through substrate device Q3.

Sensing a Negative Voltage Level

The UC1903 has a dedicated inverter coupled to the sense 4 input. With this inverter, a negative voltage level can be sensed as shown in Figure 6. The output of the inverter is an unbiased emitter follower. By tying the inverting input, Pin 5, high the output emitter follower will be reverse biased, leaving the sense 4 input in a high impedance state. In this manner, the sense 4 input can be used, as the remaining sense inputs would be, for sensing positive voltage levels.



Note: A similar scheme w/the G.P. op-amp will allow a second negative supply to be monitored.

Figure 6. Inverting the sense 4 input for monitoring a negative supply is accommodated with the dedicated inverter.

Using The Line/Switcher Sense Output

The line switcher sense input to the UC1903 can be used for early detection of line, switcher, or other power source, failures. Internally referenced to 2.0V, the line sense comparator will cause the POWER OK output to indicate a fault (active low) condition when the LINE/SWITCHER SENSE input goes from above to below 2.0V. The line sense comparator has approximately 175mV of hysteresis requiring the line/switcher input to reach 2.175V before the POWER OK output device can be turned off, allowing a no-fault indication. In Figure 7 an example showing the use of the LINE/SWITCHER SENSE input for early switcher-fault detection is detailed. A sample signal is taken from the output of the power transformer, rectified and filtered, and used at the line/switcher input. By adjusting the R2C time constant with respect to the switching frequency of the supply and the hold up time of the output capacitor, switcher faults can be detected before supply outputs are significantly affected.

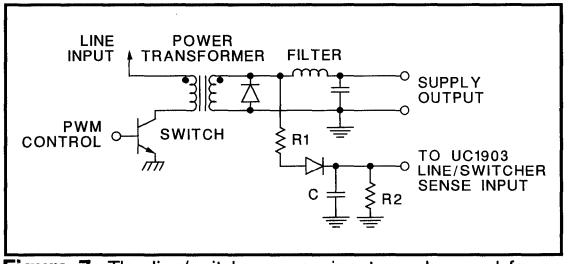


Figure 7. The line/switcher sense input can be used for an early line or switcher fault indication.

OV and UV Comparators Maintain Accurate Thresholds

The structure of the $\overline{OV}$ and $\overline{UV}$ comparators, shown in Figure 8 results in accurate fault thresholds even in the case where multiple sense inputs cross a fault threshold simultaneously. Unused sense inputs can be tied either to the 2.5V reference, or to another, utilized, sense input. The four under- and over-voltage sense inputs on the UC1903 are clamped as detailed on the Sense 1 input in Figure 8. The series 2k resistor, R_1, and zener diode Z_1, prevent extreme under- and over-voltage conditions from inverting the outputs of the fault comparators. A parasitic diode, D_1, is present at the inputs as well. Under normal operation it is advisable to insure that voltage levels at all of the sense inputs stay above -0.3V. The same type of input protection exists at the line sense input, Pin 15, except a 5k series resistor is used.

The fault delay circuitry on the UC1903 is also shown in Figure 8. In the case of an over-voltage condition at one of the sense inputs Q_{20} is turned off, allowing the internal 60µA current source to charge the user-selected delay capacitor. When the capacitor voltage reaches 1.8V, the $\overline{OV}$ and POWER OK outputs become active low. When the fault condition goes away Q_{20} is turned back on, rapidly discharging the delay capacitor. Operation of the under-voltage delay is, with appropriate substitutions, the same.

OPERATION AND APPLICATION INFORMATION (continued)

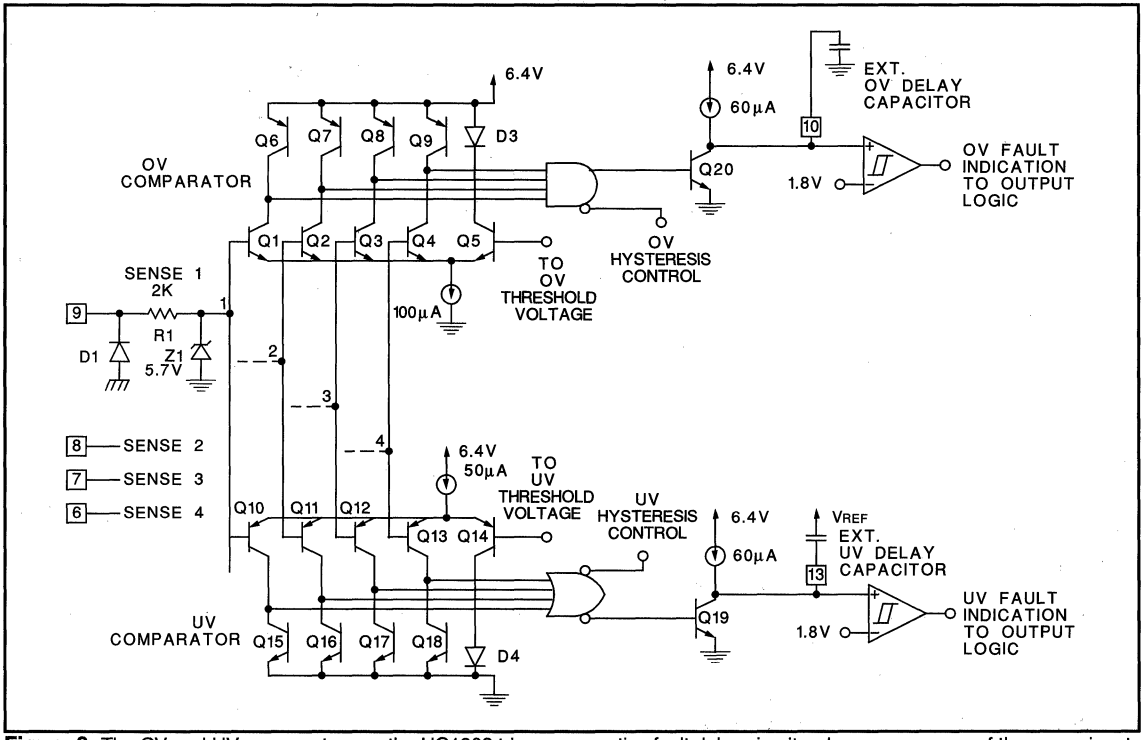


Figure 8. The OV and UV comparators on the UC1903 trigger respective fault delay circuits when one or more of the sense inputs move outside the fault window. Input clamps insure proper operation under extreme fault conditions. Terminating the UV delay capacitor to VREF assures correct logic at power up.

Start Latch and Supply Under-Voltage Sense Allow Predictable Power-Up

The supply under-voltage sense and start-latch circuitry on the UC1903 prevents fault indications during start-up or low input supply (+VIN) conditions. When the input supply voltage is below the supply under-voltage threshold the $\overline{OV}$ and $\overline{UV}$ fault outputs are disabled and the POWER OK output is active low. The POWER OK output will remain active until the input supply drops below approximately 3.0V. With +VIN below this level, all of the open collector outputs will be off.

When the input supply is low, the under-voltage sense circuitry resets the start-latch. With the start-latch reset, the UV fault output will remain disabled until the input supply rises to its normal operating level (8-40V), and all of the sense inputs are above the under-voltage threshold. This allows slow starting, or supply sequencing, without an artificial under-voltage fault indication. Once the latch is set, the UV fault output will respond if any of the sense inputs drop below the under-voltage threshold.

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Precision Quad Supply and Line Monitor

FEATURES

- Inputs for Monitoring Up to Four Supply Voltages
- Two Inputs Preset for -5V and -12V Monitoring, or Programmable Positive Levels
- Precision 2.5V Reference
- Separate Inputs for Over-Current and Line Fault Sensing
- Adjustable Under- to Over-Voltage Fault Windows
- Latched Over-Voltage and Over-Current Output
- Power Good and Power Warning Outputs
- Auto Restart Function with ON/OFF Control, and Programmable Delay
- Programmable Pwr On Reset Delay

DESCRIPTION

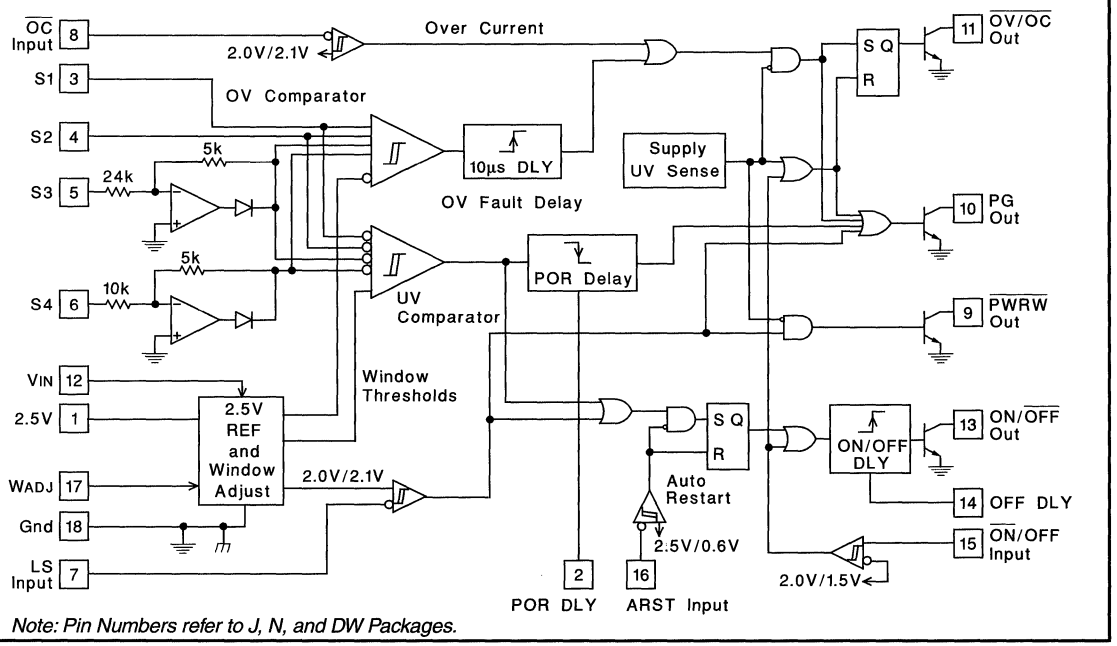
The UC1904 Quad Supply Monitor will respond to under- and over-voltage conditions on up to four continuously monitored voltage levels. Four independent positive voltages can be monitored or, alternatively, two of the sense inputs are preset to monitor -5V and -12V supplies. The device also monitors Over-Current and Line Sense inputs, both with precision input thresholds.

Four open collector outputs on the UC1904 give the following responses: 1. The $\overline{OV/OC}$ output is a latched over-voltage, or over-current response. 2. A Power Good signal responds low with any fault detection – on power-up a programmable delay is used to hold this output low for a system Power On Reset signal. 3. The $\overline{PWRW}$ output responds only to a Line Sense input, for early warning of power failures. 4. The last open collector, the $ON/\overline{OFF}$ output, generates a delayed supply OFF control signal in response to an OFF input command, under-voltage condition, or line fault detection.

The OV-UV fault window is adjustable with a programming input. The thresholds are centered around the precision 2.5V reference, with a scaled hysteresis for precise, glitch free operation. In the positive mode of operation, the fault windows at each of the sense inputs can be independently scaled using external resistors and the 2.5V reference output. An Auto Restart function couples with the under-voltage and line sensing circuits to allow controlled power supply start-up and shutdown.

This device will operate over a supply range of 4.75V to 18V. The device is available in a DIP, SOIC, or PLCC outline. This device is ESD protected on all pins.

BLOCK DIAGRAM



Note: Pin Numbers refer to J, N, and DW Packages.

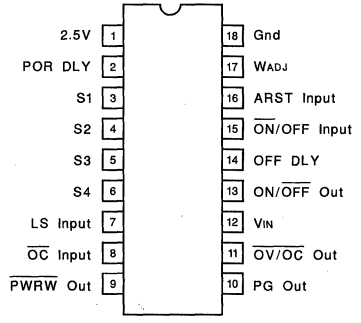
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage 20V
Sense Inputs, S1 And S2, Other Analog And Logic Inputs
  Maximum Forced Voltage ..... -0.3V to 10V
  Maximum Forced Current ..... ±10mA
Sense Input S3, (-12V Sense Input)
  Maximum Forced Voltage ..... -18V to 10V
  Maximum Forced Current ..... ±10mA
Sense Input S4, (-5V Sense Input)
  Maximum Forced Voltage ..... -10V to 10V
  Maximum Forced Current ..... ±10mA
Open Collector Outputs
  Maximum Voltage 20V
  Maximum Current 50mA
Reference Output Current ..... Internally Limited
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

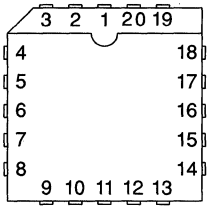
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N PACKAGE, DW PACKAGE



PLCC-20 (TOP VIEW)
Q PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
2.5V	1
POR DLY	2
N.C.	3
S1	4
S2	5
S3	6
S4	7
N.C.	8
LS Input	9
$\overline{OC}$ Input	10
$\overline{PWRW}$ Out	11
PG Out	12
$\overline{OV/OC}$ Out	13
VIN	14
$\overline{ON/OFF}$ Out	15
OFF DLY	16
$\overline{ON}$/OFF Input	17
ARST Input	18
WADJ	19
Gnd	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, +VIN = 15V, WADJ = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current	VIN = 15V		3.2	4.5	mA
VIN UVLO Threshold	Low to High		4.5	4.75	V
UVLO Threshold Hysteresis			50		mV
Minimum VIN to Enable PG Out			0.8	1.5	V
Reference					
Output Voltage(VREF)	T_J = 25°C	2.475	2.5	2.525	V
	Over Temperature, UC3904	2.47		2.53	V
	Over Temperature, UC2904 & UC1904	2.465		2.535	V
Load Regulation	IOUT = 0 to 4mA			6	mV
Line Regulation	VIN = 4.75 to 18V			5	mV
Short Circuit Current	VREF = 0V		17		mA
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds					
Over-Voltage Thresholds S1, S2	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	140	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	270	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	540	mV
Over-Voltage Thresholds S3, S4 Positive Mode	WADJ = 0.25V, Offset from VREF, Input L to H	110	125	145	mV
	WADJ = 0.5V, Offset from VREF, Input L to H	230	250	280	mV
	WADJ = 1V, Offset from VREF, Input L to H	460	500	550	mV

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for T_A = 0 to 70°C for the UC3904, -40 to +85°C for the UC2904, and -55 to +125°C for the UC1904, $+V_{IN}$ = 15V, W_{ADJ} = 0.5V, Sense Inputs 1-4, $\overline{OC}$ and LS Inputs = 2.5V. The $\overline{ON}$/OFF Input and the ARST Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV UV Window, LS Input, OC Input, ARST Input, and $\overline{ON}$/OFF Input Thresholds (cont.)					
Under-Voltage Thresholds S1, S2	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-140	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-270	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-540	-500	-460	mV
Under-Voltage Thresholds S3, S4 Positive Mode	W_{ADJ} = 0.25V, Offset from V_{REF}, Input H to L	-150	-125	-110	mV
	W_{ADJ} = 0.5V, Offset from V_{REF}, Input H to L	-285	-250	-230	mV
	W_{ADJ} = 1V, Offset from V_{REF}, Input H to L	-555	-500	-460	mV
OV and UV Threshold Hysteresis	As a Function of W_{ADJ}	30	50	70	mV/V
S3 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-13.52	-13.2	-12.88	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-11.06	-10.8	-10.54	V
	Hysteresis, W_{ADJ} = 0.5V	80	120	160	mV
S4 Negative Mode Thresholds	Over-Voltage, W_{ADJ} = 0.5V, Input H to L	-5.63	-5.5	-5.37	V
	Under-Voltage, W_{ADJ} = 0.5V, Input L to H	-4.61	-4.5	-4.39	V
	Hysteresis, W_{ADJ} = 0.5V	30	50	70	mV
W_{ADJ} Input Bias Current	0.25V < W_{ADJ} <1.0V	-5		5	µA/V
LS Threshold	Input = H to L	1.96	2	2.04	V
	Threshold hysteresis	65	100	125	mV
$\overline{OC}$ Threshold	Input = H to L	1.9	2	2.1	V
	Threshold hysteresis	50	100	150	mV
ARST Input Threshold	Input = L to H	2.25	2.5	2.75	V
	Input = H to L	0.56	0.625	0.69	V
$\overline{ON}$/OFF Input Threshold	Input high level		1.74	2.4	V
	Input low level	0.6	1.35		V
Sense and Logic Input Bias Currents					
Sense 1-4, Positive Mode	Input = 2.8V		250	800	nA
	Input = 2.2V	-1000	-250		nA
Sense 3 Negative Mode	Input = -12V	-700	-500	-300	µA
Sense 4 Negative Mode	Input = -5V	-700	-500	-300	µA
Line, and OC Inputs	Input = 2.2V		300	1000	nA
$\overline{ON}$/OFF Input	Input = 2.5V		150	600	nA
ARST Input	Input = 0.5	-2000	-700		nA
Open Collector Outputs ($\overline{OV}$/$\overline{OC}$ Out, PG Out, $\overline{PWRW}$ Out, ON/$\overline{OFF}$ Out)					
Saturation Voltage	I_{OUT} = 10mA		0.2	0.4	V
Leakage current	V_{OUT} = 20V			5	µA
POR Delay					
Delay		160	250	350	ms/µF
Internal Pullup Current			9		µA
Threshold Low to High			2.25		V
OFF Delay					
Delay		120	185	250	ms/µF
Internal Pullup current			12		µA
Threshold Low to High			2.25		V
OV Fault Delay					
Delay		10	20	50	µs

PIN FUNCTIONAL DESCRIPTION

2.5V: This is the output of the precision 2.5V reference.

ARST Input: This input, with a 4:1 hysteretic threshold, is used to sequence a power system through the **A**uto **R**e-**S**tar**T** cycle. A delayed representation of a supply output voltage is used at this pin to provide adequate startup time for the power system, and a minimum power-off period.

Gnd: Reference point for the internal reference and all thresholds, as well as the return for the remainder of the device.

LS Input: The **L**ine **S**ense input is used to monitor a voltage that varies with the input line voltage to a system. The input is compared to a precision 2.0V level and is used to activate the $\overline{\text{PWRW}}$ and PG outputs, as well as triggering the Auto Restart sequence.

$\overline{\text{OC}}$ Input: The **O**ver-**C**urrent input can be used to respond to an inverted over-current signal. A low level signal at this input latches in a fault indication at the **$\overline{\text{OV/OC}}$** output.

OFF DLY: This pin functions similarly to the **POR DLY** pin to delay the turn-on of the ON/$\overline{\text{OFF}}$ output transistor. The charging current and upper threshold are 12µA and 2.1V.

$\overline{\text{ON/OFF}}$ Input: With a high level at this input the **ON/$\overline{\text{OFF}}$ Out** pin is activated after a user-programmable delay. A high level also activates the **PG Out** pin, and resets the **OV/OC** fault latch.

On/$\overline{\text{Off}}$ Out: This output is an open collector output that is activated by the **$\overline{\text{ON/OFF}}$ Input**, or the Auto Restart circuitry. Saturation voltage on this and all the open collector outputs is rated at 10mA of current.

$\overline{\text{OV/OC}}$ Out: In response to either an **O**ver-**V**oltage or **O**ver-**C**urrent situation this output is latched active low. There is nominal 20µs delay in the OV path to the fault latch, providing rejection to transient overshooting on the monitored voltages. The low condition is cleared when the fault latch is reset by the **$\overline{\text{ON/OFF}}$ Input**, or a **UVLO** condition on the device.

POR DLY: This pin is used, with an external capacitor, to program a **P**ower-**O**n-**R**eset delay. This delay is reset whenever there is a UV condition at one of the S1-S4 inputs, and then triggered upon the clearing of the UV condition. When reset, the voltage across the capacitor is quickly discharged to near zero volts, and the **PG Out** pin goes active low. Once triggered the capacitor is charged by a 9µA current source. The **PG Out** pin remains active low until the delay capacitor voltage reaches a 2.1V threshold.

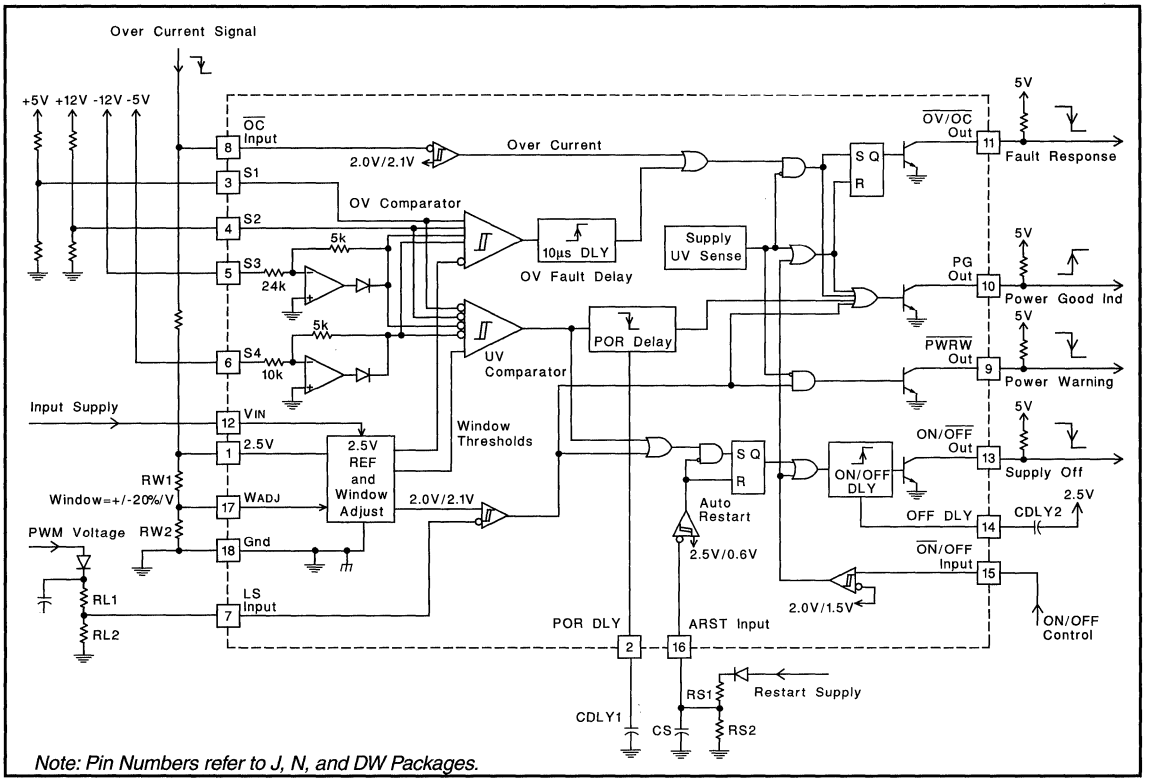
PG Out: During any fault, under-voltage, or UVLO condition this output is low. A **P**ower **G**ood indication (output off) is given when all supply conditions are within defined operating limits. During power-up the **PG** signal is delayed by a programmable **P**ower **O**n **R**eset delay. During **UVLO** the output is active low as long as the input supply, **VIN**, is above approximately 1.0V.

$\overline{\text{PWRW}}$ Out: When a low line condition is sensed by the **LS Input** this output goes low. This output is disabled (off) during a **UVLO** condition.

S1-S4: These are the sense inputs for OV and UV monitoring of external voltages. All four inputs can be used to sense positive voltages with a simple divider to scale the voltage level to the 2.5V centered window. The **S3** and **S4** inputs can also be used to sense -12V and -5V supplies respectively with no external components. This is done with internal precision resistor dividers and two source only op-amps that are disabled when the pins are used in the positive mode.

VIN: Input supply for the UC1904. The device is operational with 4.75V to 18V on this pin.

WADJ: The **WADJ** input is used to program the OV and UV window thresholds. The OV-UV window is centered around the 2.5V reference and is nominally ±20% per volt on the **WADJ** input pin.



Note: Pin Numbers refer to J, N, and DW Packages.

7

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UNITRODE

application INFO available

UC1907
UC2907
UC3907

Load Share Controller

FEATURES

- Fully Differential High Impedance Voltage Sensing
- Accurate Current Amplifier for Precise Current Sharing
- Opto Coupler Driving Capability
- 1.25% Trimmed Reference
- Master Status Indication
- 4.5V TO 35V Operation

DESCRIPTION

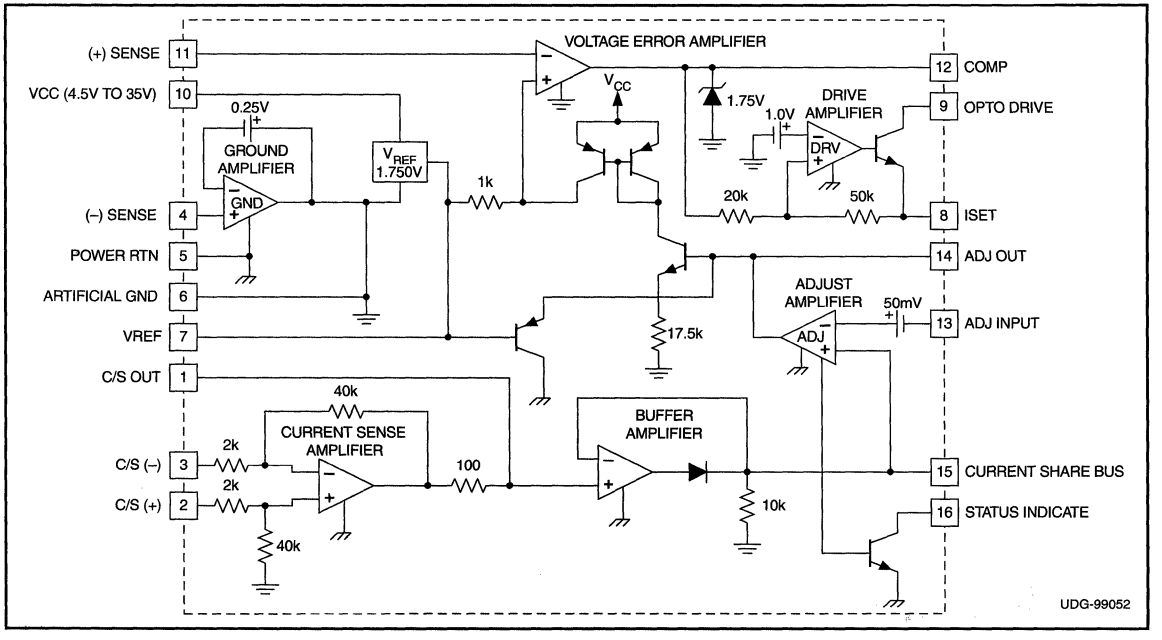
The UC3907 family of Load Share Controller ICs provides all the necessary features to allow multiple independent power modules to be paralleled such that each module supplies only its proportionate share to total load current.

This sharing is accomplished by controlling each module's power stage with a command generated from a voltage feedback amplifier whose reference can be independently adjusted in response to a common share bus voltage. By monitoring the current from each module, the current share bus circuitry determines which paralleled module would normally have the highest output current and, with the designation of this unit as the master, adjusts all the other modules to increase their output current to within 2.5% of that of the master.

The current share bus signal interconnecting all the paralleled modules is a low-impedance, noise-insensitive line which will not interfere with allowing each module to act independently should the bus become open or shorted to ground. The UC3907 controller will reside on the output side of each power module and its overall function is to supply a voltage feedback loop. The specific architecture of the power stage is unimportant. Either switching or linear designs may be utilized and the control signal may be either directly coupled or isolated though the use of an opto coupler or other isolated medium.

Other features of the UC3907 include 1.25% accurate reference: a low-loss, fixed gain current sense amplifier, a fully differential, high-impedance voltage sensing capability, and a status indicator to designate which module is performing as master.

BLOCK DIAGRAM



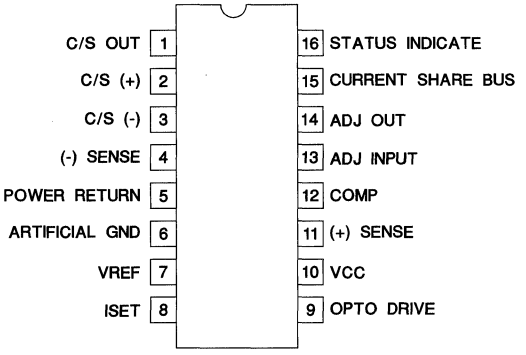
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +35V
Opto Out Voltage. . . . . +35V
Opto Out Current . . . . . +20mA
Status Indicate Sink Current. . . . . +20mA
C/S Input Voltage . . . . . +35V
Share Bus Voltage . . . . . – 0.3V to +35V
Other Analog Inputs and Outputs (Zener clamped)
Maximum Forced Voltage . . . . . – 0.3V to +10V
Maximum Forced Current. . . . . ±10mA
Ground Amp Sink Current . . . . . +50mA
Pins 1, 9, 12, 15 Sink Current. . . . . +20mA
Storage Temperature Range . . . . . – 65°C to +150°C
Junction Temperature . . . . . – 55°C to +150°C
Lead Temperature (Solder 10 Seconds) . . . . . +300°C

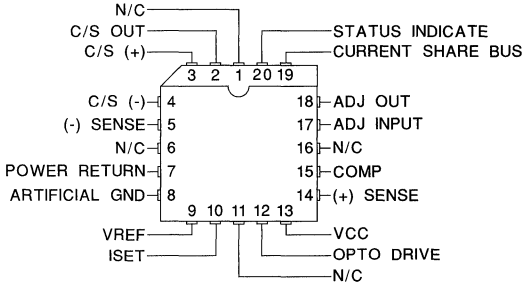
Pin Nos. refer to 16 Pin DIL Package
Currents are positive into, negative out of the specified terminal. Consult packaging section of databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

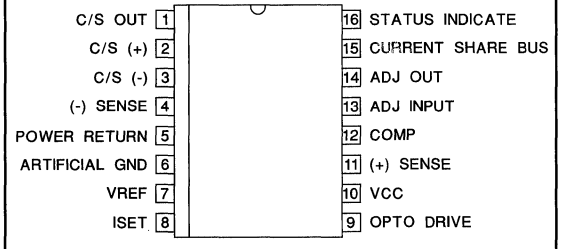
DIL-16 (Top View)
J or N Package



PLCC–20, LCC–20 (Top View)
Q PACKAGE, L PACKAGE



SOIC-16 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1907; –40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Amp Section					
Input Voltage	COMP = 1V, T_A = 25°C	1.975	2.000	2.025	V
	COMP = 1V, Over Temp	1.960	2.000	2.040	V
Line Regulation	V_{IN} = 4.5V to 35V			15	mV
Load Regulation	I_L Reference = 0.0mA to – 10mA			10	mV
Long Term Stability	T_A = 125°C, 1000hrs (Note 2)		5	25	mV
Total Output Variation	Line, Load, Temp	1.960		2.040	
Input Adjust Range	ADJ OUT from max high to max low	85	100	115	mV
Input Bias Current		–1			µA
Open Loop Gain	COMP = 0.75V to 1.5V	65			dB
Unity Gain Bandwidth	T_A = 25°C (Note 2)	700			kHz
Output Sink Current	(+) SENSE = 2.2V, COMP = 1V	6	15		mA
Output Source Current	(+) SENSE = 1.8V, COMP = 1V	400	600		µA
V_{OUT} High	(+) SENSE = 1.8V, I_L = – 400µa	1.85	2		V
V_{OUT} Low	(+) SENSE = 2.2V, I_L = +1mA		0.15	0.40	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1907; –40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output Voltage	T_A = 25°C	1.970	2.000	2.030	V
	Over Operating Temp	1.955	2.000	2.045	V
Short Circuit Current	VREF = 0.0V	– 15	– 30	– 60	mA
Ground Amp Section					
Output Voltage		200	250	300	mV
Common Mode Variation	(–) SENSE from 0.0V to 2V			5	mV
Load Regulation	I_L = 0.0mA to 20mA, T_A = 25°C			10	mV
	I_L = 0.0mA to 20mA, Over Temp			15	mV
Adjust Amp Section					
Input Offset Voltage	ADJ OUT = 1.5V, Vcm = 0.0V	40	50	60	mV
Input Bias Current		– 2			µA
Open Loop Gain	1.5V≤ ADJ OUT≤ 2.25V	65			dB
Unity Gain Bandwidth	T_A = 25°C, C_{OUT} =1µF (Note 2)		500		Hz
Transconductance	I_{OUT} = – 10µA to +10µA, V_{OUT} = 1.5V	1.7	3	4.5	ms
Output Sink Current	Vid = 0.0V, ADJ OUT = 1.5V	55	135	225	µA
Output Source Current	Vid = 250mV, ADJ OUT = 1.5V	110	200	350	µA
V_{OUT} High	Vid = 250mV, I_{OUT} = – 50µA	2.20	2.70	2.90	V
V_{OUT} Low	Vid = 0.0V, I_{OUT} = 50µA		0.75	1.15	V
Common Mode Rejection Ratio	Vcm = 0.0 to 10V	70			dB
Output Gain to V/A	V_{OUT} ADJ OUT = 1.5V to 2V	50	57	64	mV/V
	Δ(+) SENSE/ ΔADJ OUT				
Current Amp Section					
Gain	Vcm = 0.0V, Vid = 50mV to 100mV	19.2	19.6	20.1	V/V
Output Voltage	Vc/s (+) = Vc/s (–) = 0.0V, T_A = 25°C	210	250	290	mV
	Vc/s (+) = Vc/s (–) = 0.0V, Over Temp	180	250	330	mV
Input Offset Change with Common Mode Input	Vcm = 0V to 13V			600	µV/V
V_{OUT} High	Vid = 1V	10	14.5		V
V_{OUT} Low	Vid = – 1V, I_L = 1mA		350	450	mV
Power Supply Rejection Ratio	V_{IN} = 4.5V to 35V, Vcm = 0.0V	60			dB
Slew Rate			0.4		V/µs
Drive Amp Section Rset = 500Ω to Artificial Gnd, Opto Drive = 15V					
Voltage Gain	COMP = 0.5V to 1V	2.3	2.5	2.6	V/V
I_{SET} V_{OUT} High	(+) SENSE = 2.2V	3.8	4.1	4.4	V
I_{SET} V_{OUT} Low	(+) SENSE = 1.8V		270	300	mV
Opto out Voltage Range		4		35	V
Zero Current Input Threshold		1.55	1.65	1.75	V
Buffer Amp Section					
Input Offset Voltage	Input = 1V			5	mV
Output Off Impedance	Input = 1V, Output = 1.5V to 2V	5	10	20	kΩ
Output Source Current	Input = 1V, Output = 0.5V	6	15		mA
Common Mode Rejection Ratio	Vcm = 0.3V to 10V	70			dB
Power Supply Rejection Ratio	V_{IN} = 4.5V to 35V	70			dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UC1907; –40°C to +85°C for UC2907; and 0°C to +70°C for UC3907; V_{IN} = 15V, T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Under Voltage Lockout Section					
Startup Threshold			3.7	4.4	V
Threshold Hysteresis			20		mV
Status Indicate Section					
V_{OUT} Low	ADJ OUT = Current Share Bus		0.2	0.5	V
Output Leakage	ADJ OUT = 1V, V_{OUT} = 35V		0.1	5	µA
Total Stand by Current Section					
Startup Current	V_{IN} = UVLO – 0.2V		3	5	mA
Operating Current	V_{IN} = 35V		6	10	mA

Note 1: Unless otherwise specified all voltages are with respect to (–) SENSE. Currents are positive into, negative out of the specified terminal.

Note 2: Guaranteed by design. Not 100% tested in production.

PIN/BLOCK DESCRIPTIONS

(–) SENSE (Pin 4) - This is a high-impedance pin intended to allow remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. **This point should be considered as the "true" ground. Unless otherwise stated, all voltages are with respect to this point.**

ARTIFICIAL GROUND (Pin 6) - This is a low impedance circuit ground which is exactly 250 millivolts above the (–) SENSE terminal. This offset allows the Ground Buffer Amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (–) SENSE input.

POWER RTN (Pin 5) - This should be the most negative voltage available and can range from zero to 5V below the (–) SENSE terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current sensing impedances lie between this terminal and the (–) SENSE point.

VREF (Pin 7) - The internal Voltage Reference is a band-gap circuit set at 2.0 Volts with respect to the (–) SENSE input (1.75V above the ARTIFICIAL GROUND), and an accuracy of ± 1.5%. This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5V to 35V allowing operation from unregulated DC, an auxiliary voltage, or the same output voltage that it is controlling. Under voltage lockout has been included to insure proper startup by disabling internal bias currents until the reference rises into regulation.

VOLTAGE AMPLIFIER (Pins 11, 12) - This circuit is the feedback control gain stage for the power module's output voltage regulation, and overall loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal clamp of 2.0 Volts. The reference trimming is performed closed loop, and measured at pin 11, (+) SENSE. The value is trimmed to 2V ±1.25%.

DRIVE AMPLIFIER (Pins 8, 9, 12) - This amplifier is used as an inverting buffer between the Voltage Amplifier's output and the medium used to couple the feedback signal to the power controller. It has a fixed voltage gain of 2.5 and is usually configured with a current-setting resistor to ground. This establishes a current - sinking output optimized to drive optical couplers biased at any voltage from 4.5V to 35V, with current levels up to 20mA. The polarity of this stage is such that an increasing voltage at the Voltage Amplifier's sense input (as, for example, at turn on) will increase the opto's current. In a nonisolated application, a voltage signal ranging from 0.25V to 4.1V may be taken from the current-setting output but it should be noted that this voltage will also increase with increasing sense voltage and an external inverter may be required to obtain the correct feedback polarity.

CURRENT AMPLIFIER (Pins 1, 2, 3) - This amplifier has differential sensing capability for use with an external shunt in the power return line. The common-mode range of its input will accommodate the full range between the Power Return point and VCC–2V which will allow undefined line impedances on either side of the current shunt. The gain is internally set at 20 giving the user the ability to establish the maximum voltage drop across the current sense resistor at any value between 50 and 500 millivolts. While the bandwidth of this amplifier may be reduced with the addition of an external output capacitor to ground, in most cases this is not required as the compensation of the Adjust Amplifier will typically form the dominant pole in the adjust loop.

PIN/BLOCK DESCRIPTIONS (cont.)

BUFFER AMPLIFIER (Pins 1, 15) - This amplifier is a uni-directional buffer which drives the CURRENT SHARE BUS - the line which will interconnect all power modules paralleled for current sharing. Since the Buffer Amplifier will only source current, it insures that the module with the highest output current will be the master and drive the bus with a low-impedance drive capability. All other Buffer Amplifiers will be inactive with each exhibiting a 10kohm load impedance to ground. The Share Bus terminal is protected against both shorts to ground and accidental voltages in excess of 50 Volts.

ADJUST AMPLIFIER (Pins 13, 14, 15) - This amplifier adjusts the individual module's reference voltage to maintain equal current sharing. It is a transconductance type in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to ground. The function of this amplifier is to compare its own module output current to the Share Bus signal - which represents the highest output current - and force an adjust command which is capable of increasing the reference voltage as seen by the voltage amplifier by as much as 100 millivolts. This number stems from the 17.5:1 internal resistor ratio between the Adjust Amplifier's clamped output and the reference, and represents a 5% total range of adjustment - a value which should be adequate to compensate for unit-to-unit reference and external resistor tolerances. The Adjust Amplifier has a built-in 50mV offset on its inverting input which will force the unit acting as the master to have a low output resulting in no change to the reference. While this 50mV offset represents an error in current sharing, the gain of the current amplifier reduces it to only 2.5mV across the current sense resistor. It should also be noted that when the module is acting independently with no connection to the Share Bus node, or when the Share Bus node is shorted to ground, its reference voltage will be unchanged. Since only the circuit acting as a master will have a low output from the Adjust Amplifier, this signal is used to activate a flag output to identify the master should some corrective action be needed.

STATUS INDICATE (Pin 16) - This pin is an open collector output intended to indicate the unit which is acting as the master. It achieves this by sensing when the adjust amp is in its low state and pulling the status indicate pin low.

ADDITIONAL INFORMATION

Please refer to additional application information.

[1] Application Note U-129, *UC3907 Load Share IC Simplifies Parallel Power Supply Design* by Mark Jordan.

[2] Application Note U-163, *UC3902 Load Share Controller and its Performance in Distributed Power Systems* by Laszlo Balogh.

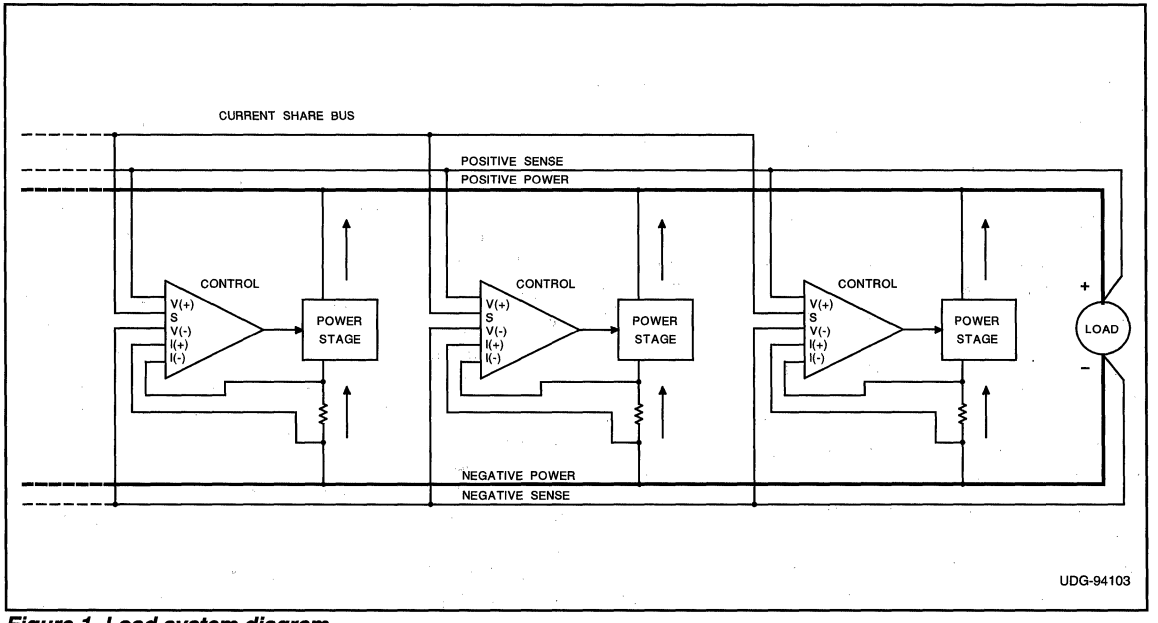


Figure 1. Load system diagram.

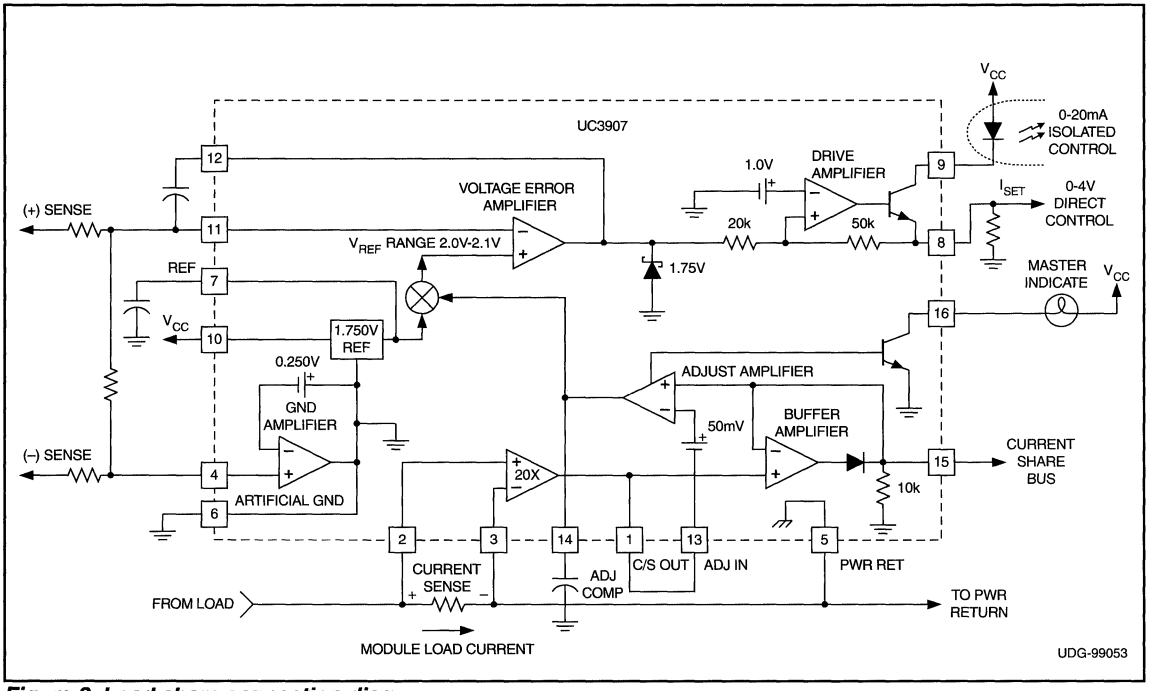


Figure 2. Load share connection diagram.

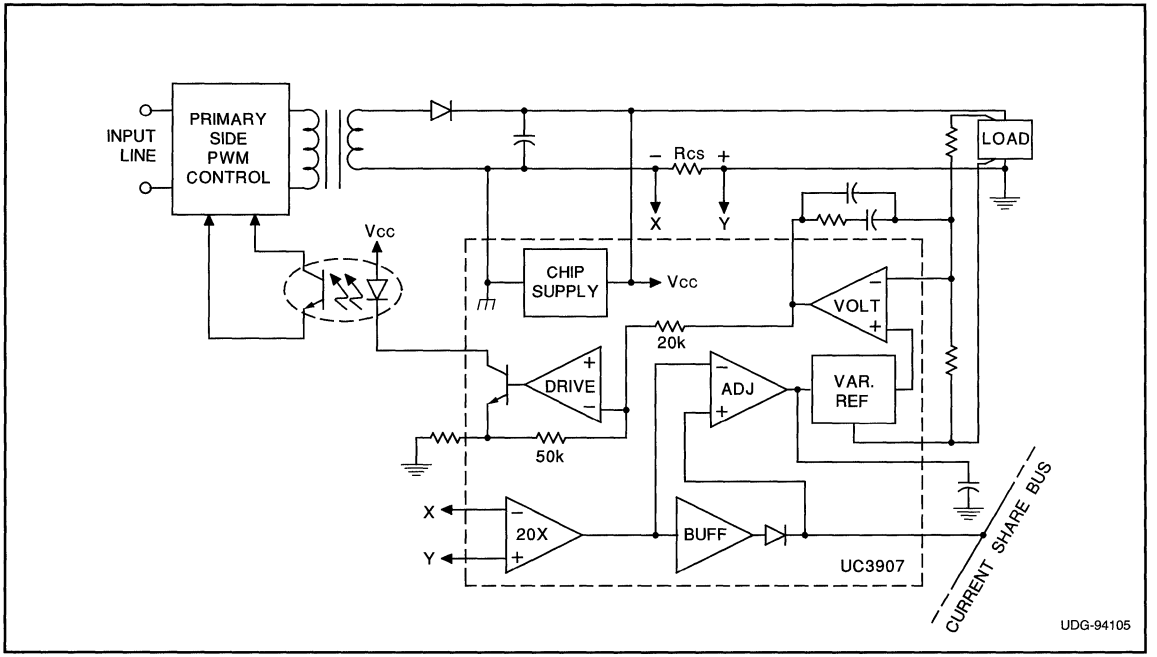


Figure 3. UC3907 In a load-sharing feedback loop for an off-line isolated supply.

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UNITRODE

Precision Adjustable Shunt Regulator

UC19431
UC29431
UC39431
UC39431B

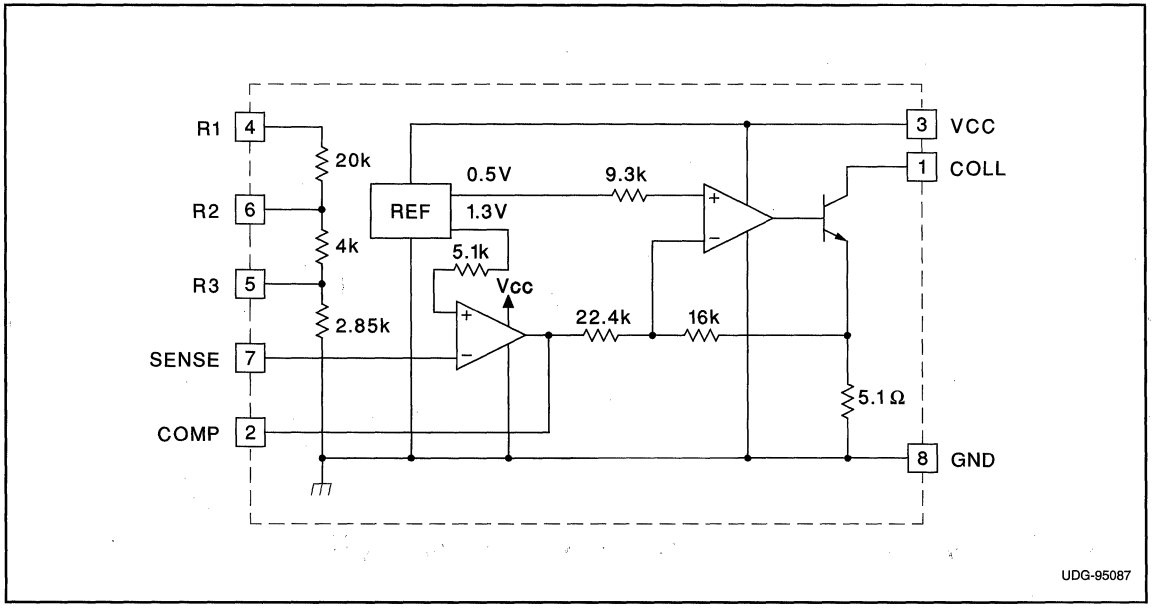
FEATURES

- Multiple On-Chip Programmable Reference Voltages
- 0.4% Initial Accuracy
- 0.7% Overall Reference Tolerance
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- 36.0V Operating Supply Voltage
- Reference Accuracy Maintained For Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Improved Architecture Provides a Known Linear Transconductance with a +5% Typical Tolerance

DESCRIPTION

The UC39431 is an adjustable shunt voltage regulator with 100mA sink capability. The architecture, comprised of an error amplifier and transconductance amplifier, gives the user separate control of the small signal error voltage frequency response along with a fixed linear transconductance. A minimum 3MHz gain bandwidth product for both the error and transconductance amplifiers assures fast response. In addition to external programming, the IC has three internal resistors that can be connected in six different configurations to provide regulated voltages of 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, and 12.24V. A sister device (UC39432) provides access to the non-inverting error ampilifer input and reference, while eliminating the three internal resistors.

BLOCK DIAGRAM



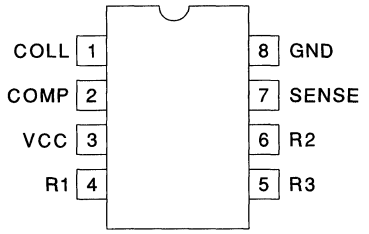
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V 36V
Regulated Output: V 36V
Internal Resistors: R1, R2, R3 ..... 13V
E/A Input: SENSE 6V
E/A Compensation: COMP 6V
Output Sink Current: I 140mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55°C$ to +125°C and COLL Output = 2.4V to 36.0V for the UC19431, $T_A = -25°C$ to +85°C and COLL Output = 2.3V to 36.0V for the UC29431, and $T_A = 0°C$ to +70°C and COLL Output = 2.3V to 36.0V for the UC39431/B, VCC = 15V, I_{COLL} = 10mA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	$T_A = 25°C$	19431*	1.295	1.3	1.305	V
		39431B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V_{COLL} = 5.0	19431*	1.291	1.3	1.309	V
		39431B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.2V to 36.0V, V_{COLL} = 5V	19431*		10	38	mV
		39431B		10	57	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL} = 5V	19431*		10	38	mV
		39431B		10	57	mV
Sense Input Current			–0.5	–0.2		µA
Minimum Operating Current	VCC = 36.0V, V_{COLL} = 5V			0.50	0.80	mA
Collector Current Limit	V_{COLL} = VCC = 36.0V, Ref = 1.35V			130	145	mA
Collector Saturation	I_{COLL} = 20mA		0.7	1.1	1.5	V
Transconductance (gm)	VCC = 2.4V to 36.0V, V_{COLL} = 3V, I_{COLL} = 20mA	19431*	–170	–140	–110	mS
		39431B	–180	–140	–100	mS
5.1V Reference	Internal Divider	19431*	5.05	5.1	5.15	V
		39431B	5	5.1	5.2	V
12.24V Reference	Internal Divider	19431*	12	12.24	12.5	V
		39431B	12	12.24	12.5	V
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

** Also applies to the UC29431 and UC39431*

Note: *The internal divider can be configured to give six unique references. These references are 2.82V, 3.12V, 5.1V, 7.8V, 10.42V, 12.24V.*

Note 1: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS (cont.)

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm • RL, where gm is designed to be –140mS ±30mS and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

R1, R2, R3: Connection points to the three internal resistors.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

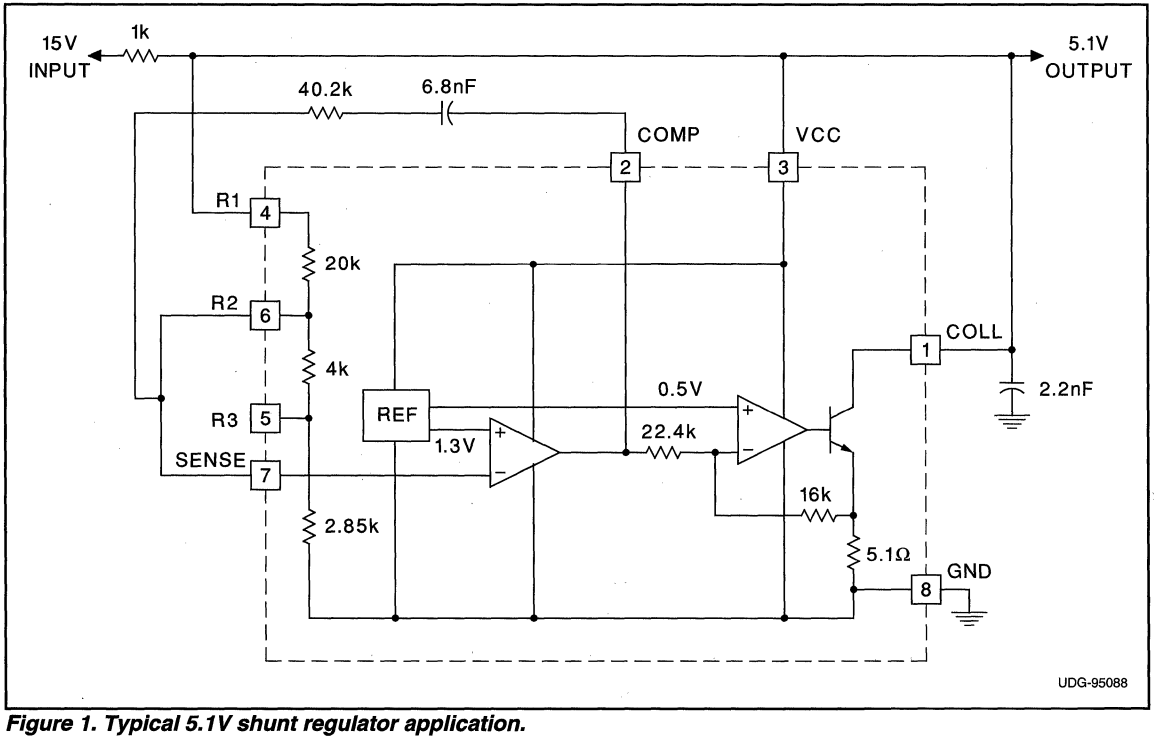


Figure 1. Typical 5.1V shunt regulator application.

APPLICATION INFORMATION

Magnetic Amplifier Controller Application

The 0.4% initial reference makes the UC39431 ideal as a programmable shunt regulator. By adding two external resistors, the on-chip 1.3V reference can be gained to any voltage between 2.2V (2.4V for the UC39431) and 36.0V. The input bias current is typically maintained at 0.2µA for the output voltage range. Since the non-inverting error amplifier input is not available, a 5.1k non-inverting input impedance is added to the input of the error amplifier. This allows the user to choose the SENSE pin input impedance to cancel the minimal offset voltage caused by the input bias current.

Frequency Compensation

The UC39431 shunt regulator is designed with two independant gain stages. The error amplifier provides 90dB of gain with a typical gain bandwidth product of 5MHz. The error amplifier provides sufficient gain in order for the sense voltage to be accurately compared to the 1.3V on-chip reference. Complete control of the frequency response of the error amplifier is accomplished with the COMP pin. By putting negative feedback across the error amplifier, either a pole or a pole-zero can be added.

The second gain stage is the transconductance (gm) amplifier. The gm amplifier is designed with a known linear 140mS of transconductance. The voltage gain is consequently gm • Ro, where Ro is the output impedance at the collector pin. The frequency response of the transconductance amplifier is controlled with the COLL pin. The gain bandwidth product of the gm amplifier is typically 3MHz. A pole or pole-zero can be added to this stage by connecting a capacitor or a series capacitor and resistor between COLL and GND.

The compensation of a control loop containing the UC39431 is made easier due to the independant compensation capability of the error amplifier and gm amplifier. As shown in the applications information, a pole-zero is created with a series resistor and capacitor between SENSE and COMP. The pole created is dominant, while the zero is used to increase the bandwidth and cancel the effects of the pole created by the capacitor between the COLL and GND pins.

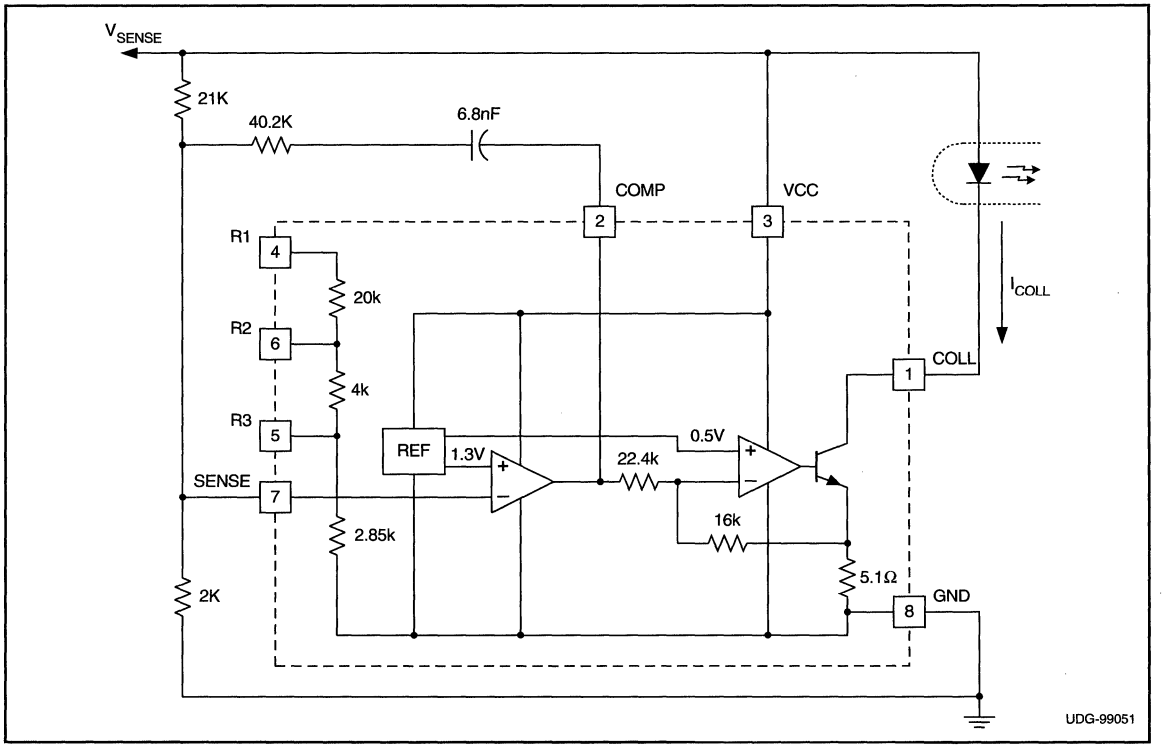


Figure 2. 15.0V optocoupler application.

APPLICATION INFORMATION (cont.)

Optocoupler Application

The two amplifier circuit architecture employed in the UC39431 is most advantageous for the optocoupler application. The error amplifier provides a fixed open loop gain that is available to apply flexible loop compensation of either poles or zeroes. A fixed transconductance amplifier provides a linear current source compared to the typical transistor's exponential output characteristics. It also eliminates the traditional optocoupler's CTR variations with power supply and voltage, and the need to suffer the additional voltage drop of a series resistor.

Magnetic Amplifier Controller Application

The UC39431 makes an excellent controller for magnetic amplifier regulated outputs. Working from either a square wave drive or from a PWM signal controlled by another output, a saturable reactor provides highly efficient control, requiring only a reset current which can be generated from its own output.

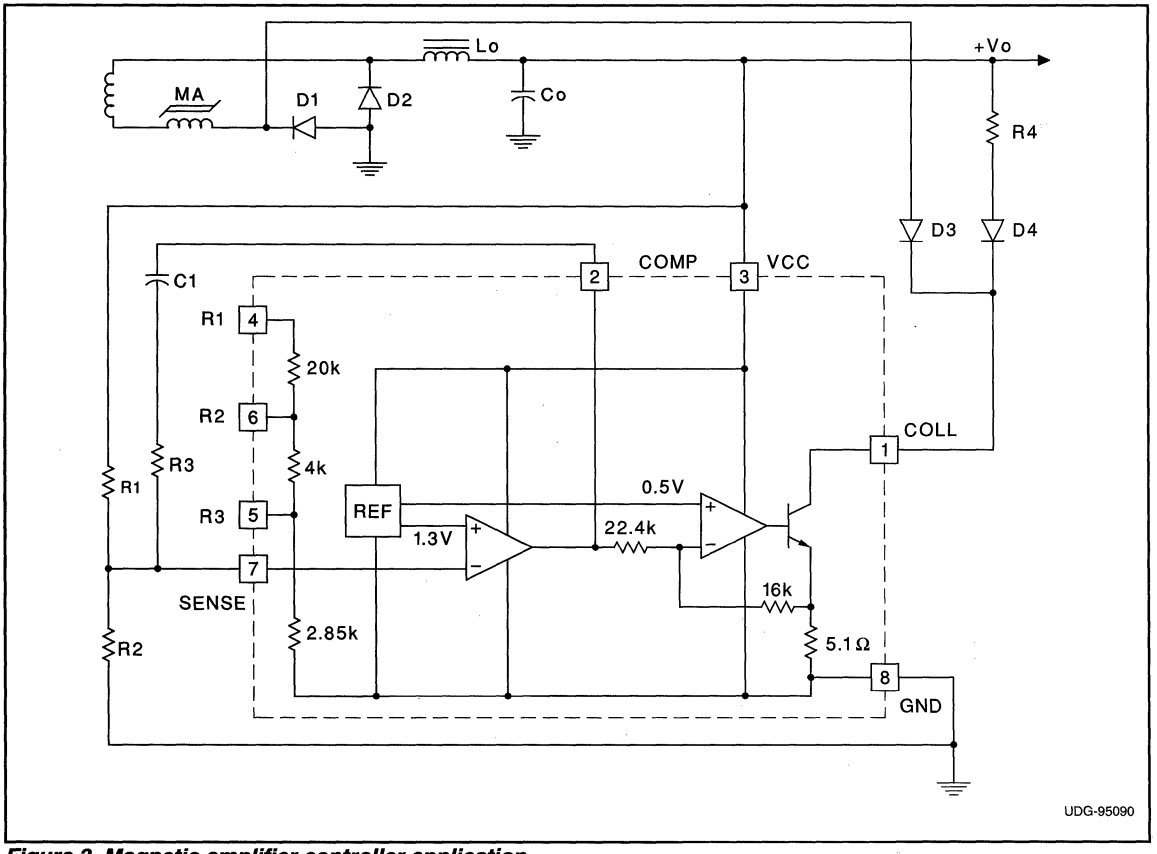


Figure 3. Magnetic amplifier controller application.

Table 1. Resistor divider connection table for shunt applications

REGULATED VOLTAGE	CONNECT R1 TO:	CONNECT R2 TO:	CONNECT R3 TO:
2.82V	SENSE (pin 7)	COLL (pin 1)	SENSE (pin 7)
3.12V	open	COLL (pin 1)	SENSE (pin 7)
5.1V	COLL (pin 1)	SENSE (pin 7)	open
7.8V	COLL (pin 1)	SENSE (pin 7)	GND (pin 8)
10.42V	COLL (pin 1)	SENSE (pin 7)	SENSE (pin 7)
12.24V	COLL (pin 1)	open	SENSE (pin 7)

Note: To obtain the shunt regulated or optocoupler sensed voltage specified in the left column, connect the internal resistors (R1, R2, R3) as indicated. Refer to the shunt regulator application in Fig.1.

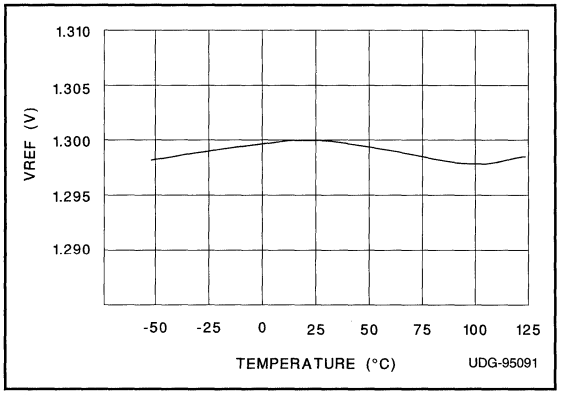


Figure 4. Internal 1.3V vs. temperature.

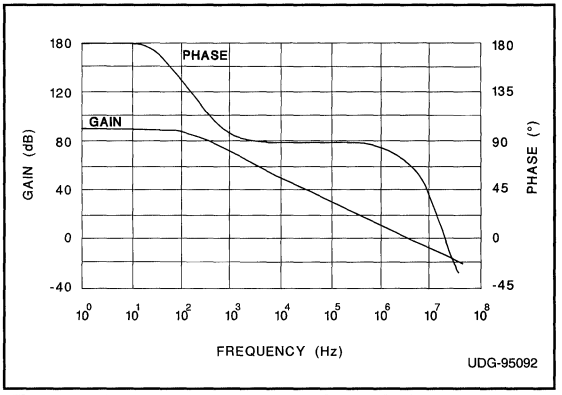


Figure 5. Error amp voltage gain and phase vs. frequency.

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application INFO available

UC19432
UC29432
UC39432
UC39432B

Precision Analog Controller

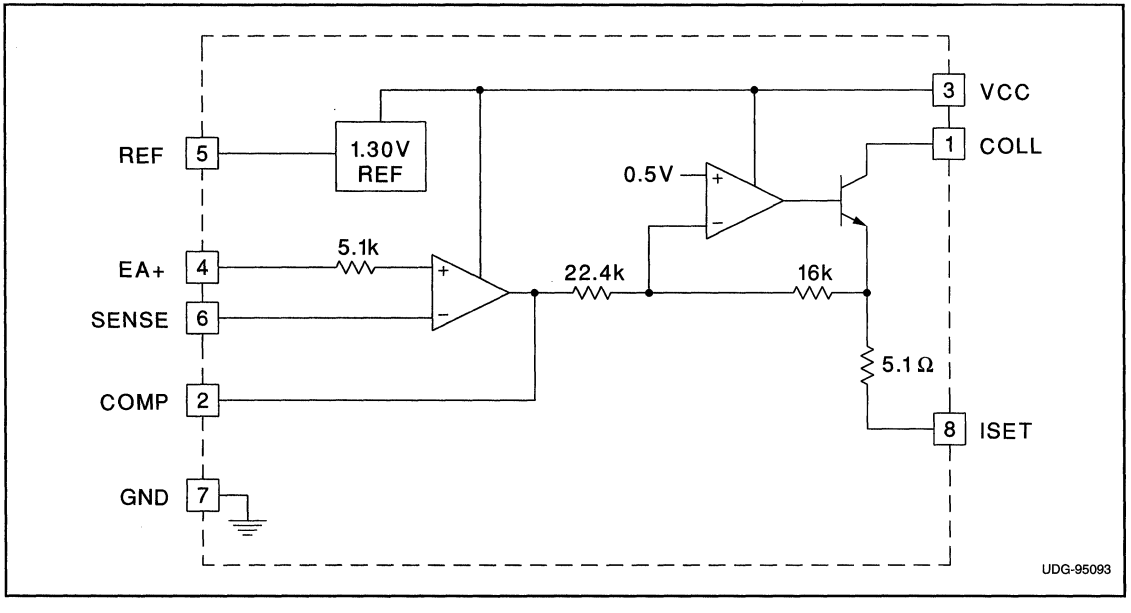
FEATURES

- Programmable Transconductance for Optimum Current Drive
- Accessible 1.3V Precision Reference
- Both Error Amplifier Inputs Available
- 0.7% Overall Reference Tolerance
- 0.4% Initial Accuracy
- 2.2V to 36.0V Operating Supply Voltage and User Programmable Reference
- Reference Accuracy Maintained for Entire Range of Supply Voltage
- Superior Accuracy and Easier Compensation for Optoisolator Application
- Low Quiescent Current (0.50mA Typ)

DESCRIPTION

The UC39432 is an adjustable precision analog controller with 100mA sink capability if the ISET pin is grounded. A resistor between ISET and ground will modify the transconductance while decreasing the maximum current sink. This will add further control in the optocoupler configuration. The trimmed precision reference along with the non-inverting error amplifier inputs are accessible for custom configuration. A sister device, the UC39431 adjustable shunt regulator, has an on-board resistor network providing six preprogrammed voltage levels, as well as external programming capability.

BLOCK DIAGRAM



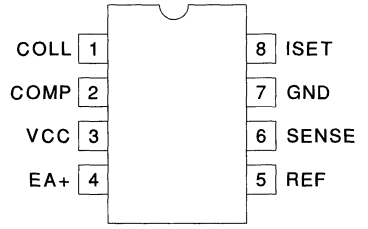
ABSOLUTE MAXIMUM RATINGS

Supply Voltage: VCC 36V
Regulated Output: V_{COLL} 36V
EA Input: SENSE, EA+ 6V
EA Compensation: COMP 6V
Reference Output: REF 6V
Output Sink Current: I_{COLL} 140mA
Output Source Current: ISET . . . . . –140mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Derate 8mW/°C for $T_A > 25°C$
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -55°C$ to +125°C and COLL Output = 2.4V to 36.0V for the UC19432, $T_A = -25°C$ to +85°C and COLL Output = 2.3V to 36.0V for the UC29432, and $T_A = 0°C$ to +70°C and COLL Output = 2.3V to 36.0V for the UC39432, VCC = 15V, I_{COLL} = 10mA, $T_A = T_J$.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage Tolerance	T_A = 25°C	19432*	1.295	1.3	1.305	V
		39432B	1.29	1.3	1.31	V
Reference Temperature Tolerance	V_{COLL} = 5.0V	19432*	1.291	1.3	1.309	V
		39432B	1.286	1.3	1.314	V
Reference Line Regulation	VCC = 2.4V to 36.0V, V_{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Load Regulation	I_{COLL} = 10mA to 50mA, V_{COLL} = 5V	19432*		10	38	mV
		39432B		10	57	mV
Reference Sink Current					10	µA
Reference Source Current					–10	µA
EA Input Bias Current			–0.5	–0.2		µA
EA Input Offset Voltage		19432*			4.0	mV
		39432B			4.0	mV
EA Output Current Sink (Internally Limited)					16	µA
EA Output Current Source					–1	mA
Minimum Operating Current	VCC = 36.0V, V_{COLL} = 5V			0.50	0.80	mA
Collector Current Limit (Note)	V_{COLL} = VCC = 36.0V, Ref = 1.35V ISET = GND			130	145	mA
Collector Saturation	I_{COLL} = 20mA		0.7	1.1	1.5	V
Transconductance (gm) (Note)	VCC = 2.4V to 36.0V, V_{COL} = 3V, I_{COLL} = 20mA ISET = GND	19432*	–170	–140	–110	mS
		39432B	–180	–140	–100	mS
Error Amplifier AVOL			60	90		dB
Error Amplifier GBW	(Note 1)		3.0	5		MHz
Transconductance Amplifier GBW				3		MHz

** Also applies to the UC29432 and UC39432*
Note: *Programmed transconductance and collector current limit equations are specified in the ISET pin description.*
Note 1: *Guaranteed by design. Not 100% tested in production.*

PIN DESCRIPTIONS

COLL: The collector of the output transistor with a maximum voltage of 36V. This pin is the output of the transconductance amplifier. The overall open loop voltage gain of the transconductance amplifier is gm • R_L, where gm is designed to be –140mS ±30mS and RL represents the output load.

COMP: The output of the error amplifier and the input to the transconductance amplifier. This pin is available to compensate the high frequency gain of the error amplifier. It is internally voltage limited to approximately 2.0V.

EA+: The non-inverting input to the error amplifier.

GND: The reference and power ground for the device. The power ground of the output transistor is isolated on the chip from the substrate ground used to bias the remainder of the device.

ISET: The current set pin for the transconductance amplifier. The transconductance will be –140mS as specified in the electrical table if this pin is grounded. If a resistance R_L is added to the ISET pin, the resulting new transconductance is calculated using the following equation: gm = –0.714V • (5.1Ω + R_L). The maximum current will be approximately

$$I_{MAX} = \frac{0.6V}{5.1\Omega + R_L}$$

REF: The output of the trimmed precision reference. It can source or sink 10μA and still maintain the 1% temperature specification.

SENSE: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point. The error amplifier uses the SENSE input to compare against the 1.3V on-chip reference.

The SENSE pin is also used as the undervoltage lockout (UVLO). It is intended to keep the chip from operating until the internal reference is properly biased. The threshold is approximately 1V. It is important that once the UVLO is released, the error amplifier can drive the transconductance amplifier to stabilize the loop. If a capacitor is connected between the SENSE and COMP pins to create a pole, it will limit the slew rate of the error amplifier. To increase the bandwidth and ensure startup at low load current, it is recommended to create a zero along with the pole as shown in the UC39431 shunt regulator application. The error amplifier must slew 2.0V to drive the transconductance amplifier initially on.

VCC: The power connection for the device. The minimum to maximum operating voltage is 2.2V to 36.0V. The quiescent current is typically 0.50mA.

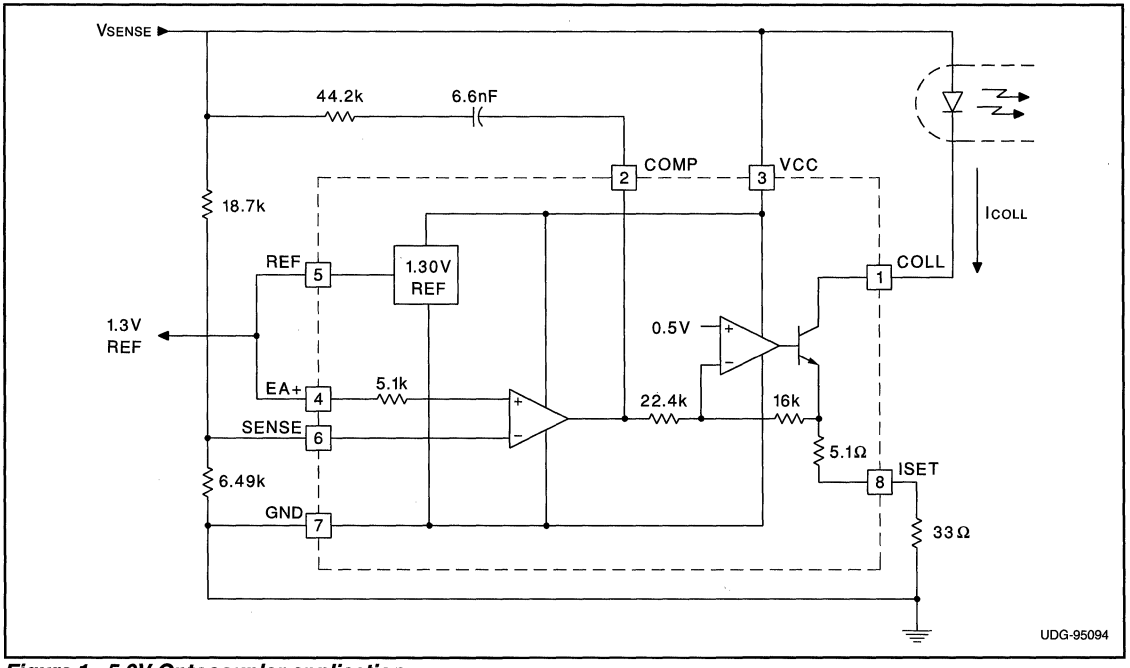


Figure 1. 5.0V Optocoupler application.

OVERVOLTAGE COMPARATOR APPLICATION

The signal V_{IN} senses the input voltage. As long as the input voltage is less than 5.5V, the output is equal to the voltage on V_{IN}. During this region of operation, the diode is reversed biased which keeps the EA+ pin at 1.3V. When V_{IN} exceeds the over voltage threshold of 5.5V, the output is driven low. This forward biases the diode and creates hysteresis by changing the threshold to 4.5V.

OPTOCOUPLER APPLICATION

The optocoupler application shown takes advantage of the accessible pins REF and ISET. The ISET pin has a 33 ohm resistor to ground that protects the opto-coupler by limiting the current to about 16mA. This also lowers the transconductance to approximately 19mS. The ability to adjust the transconductance gives the designer further control of the loop gain. The REF pin is available to satisfy any high precision voltage requirements.

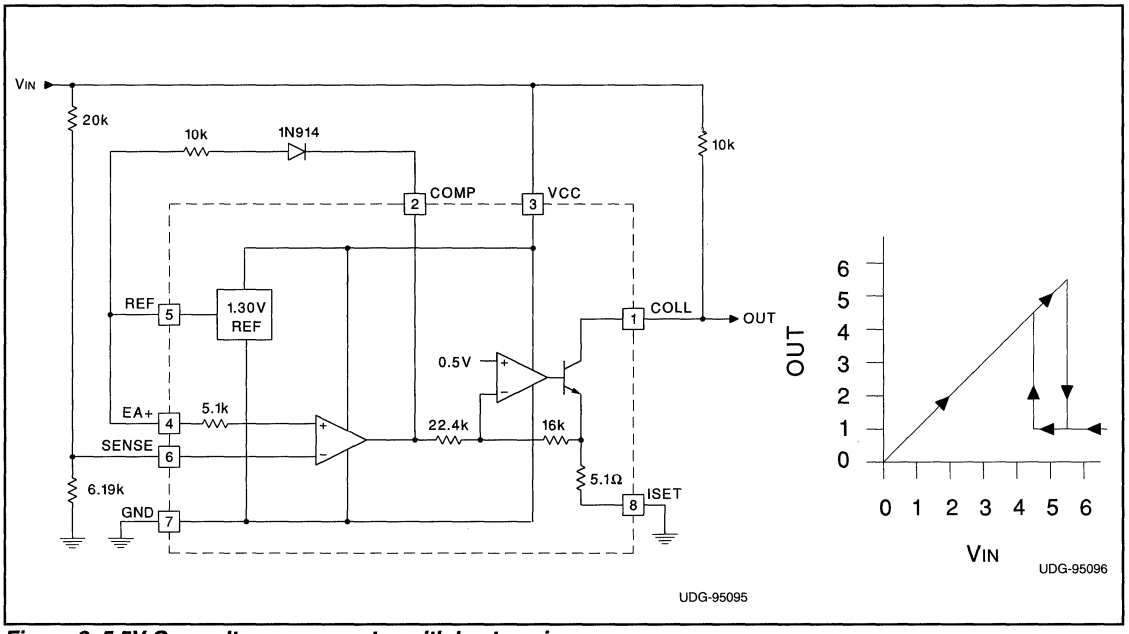


Figure 2. 5.5V Overvoltage comparator with hysteresis.

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UC1965
UC2965
UC3965

Precision Reference with Low Offset Error Amplifier

FEATURES

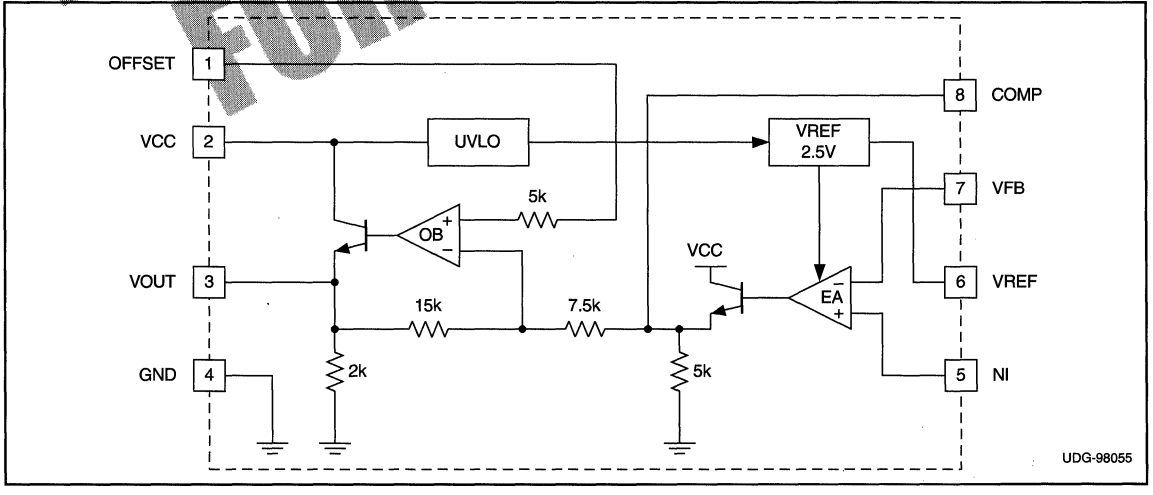
- Accessible 2.5V Precision Reference
- 0.4% Initial Reference Accuracy
- 1% Reference Accuracy over Line, Load, and Full Temperature Range
- Low 1mV Offset Error Amplifier
- Supports Closed Loop Soft Start
- 2X Inverting Amplifier / Buffer Output
- 4.1V Undervoltage Lockout
- ICC 2mA at 5V
- 8-Pin SOIC or DIL Package

DESCRIPTION

The UC3965 is suitable for applications needing greater precision and more functionality than the TL431 type shunt regulators. The wide range VCC input capability enables the device to be biased from the secondary side output voltage rail, resulting in closed loop soft start.

The UC3965 includes an accessible 2.5V precision reference which offers 0.4% initial and 1% reference accuracy over line, load, and full temperature range with a low offset error amplifier, a 2X inverting amplifier/buffer, and an undervoltage lockout circuit. The IC is ideally suited for applications where high precision PWM power supply regulation is required. Typically, the error amplifier is configured to compare a fraction of the to be regulated power supply voltage to the on-chip 2.5V reference. The 2X amplifier/buffer output is then used to drive a PWM controller or regulator. The UC3965 is also capable of driving an optocoupler diode for isolated applications.

BLOCK DIAGRAM



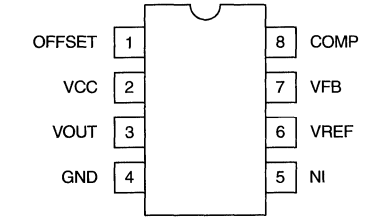
ABSOLUTE MAXIMUM RATINGS

VCC . . . . . –0.3V to 20V
VREF . . . . . –0.3V to 6V
VFB, COMP, NI, VOUT . . . . . –0.3V TO 6V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. All voltages are with respect to ground. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
J or N Package, D Package



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGE
UC1965J	–55°C to +125°C	CDIP
UC2965D	–40°C to +85°C	SOIC
UC2965N		PDIP
UC3965D	0°C to +70°C	SOIC
UC3965N		PDIP

7

ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 5V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
VCC		4.3		20	V
Operating Current	VCC = 5V	1.5	2	4	mA
Undervoltage Current				200	µA
Minimum Voltage to Start		3.9	4.1	4.3	V
Hysteresis		200	300	400	mV
VREF					
VREF Initial Accuracy	+25°C	2.49	2.5	2.51	V
VREF Over Temperature	–55°C to +125°C	2.48	2.5	2.52	V
Total Output Variation	Line, Load, Temperature	2.475	2.5	2.525	V
Line Regulation	VCC = 4.3V to 20V		2	10	mV
Load Regulation	0µA to 500µA		2	10	mV
Short Circuit Current	VREF = 0V		2		mA
Error Amplifier					
Input Bias	V_{CM} = 2.5V		200	400	nA
Input Offset Voltage	V_{CM} = 2.5V		1	2	mV
Input Offset Current	V_{CM} = 2.5V	–100	0	100	nA
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		6		MHz
Open Loop Gain	VOUT = 1V to 3.75V	80	100		dB

ELECTRICAL CHARACTERISTICS Unless otherwise specified, VCC = 5V, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Section (cont.)					
Output Low Level	I_{OUT} = 0µA		0.8		V
	I_{OUT} = 100µA		1.2		V
Output High Level	I_{OUT} = 0µA		4		V
	I_{OUT} = –500µA		4		V
Short Circuit Circuit	V_{COMP} = 0V		8		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			2		V/µs
Falling Slew Rate			0.4		V/µs
Inverting Buffer Amplifier					
Input Bias	V_{CM} = 2.5V		1	2	µA
Output Offset Voltage	V_{CM} = 2.5V	–20	0	20	mV
Gain Bandwidth Product	V_{IN} = 50mV P-P (Note 1)		1.5		MHz
Closed Loop Gain	Inverting Gain	–2.04	–2	–1.96	V/V
Output Low Level	I_{OUT} = 0µA		0.3		V
	I_{OUT} = 100µA		0.5		V
Output High Level	I_{OUT} = 0mA		4		V
	I_{OUT} = –4mA		4		V
Short Circuit Circuit	VOUT = 0V		18		mA
CMRR	V_{CM} = 1.25V to 3.75V	70	100		dB
PSRR	VCC = 4.3V to 20V	70	100		dB
Rising Slew Rate			0.9		V/µs
Falling Slew Rate			0.9		V/µs

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

COMP: The output of the error amplifier and the input to the inverting terminal of the internal output buffer. This pin is available to compensate the high frequency gain of the error amplifier.

GND: The reference and power ground for the device.

NI: The non-inverting input to the error amplifier.

OFFSET: The non-inverting input to the internal output buffer.

VCC: The power input to the device. The minimum to maximum operating voltage is 4.3V to 20V.

VFB: The inverting terminal of the error amplifier used as both the voltage sense input to the error amplifier and its other compensation point.

VOUT: The emitter of the output transistor. This pin is the output of the inverting buffer. This pin has the capability to drive an optocoupler or a PWM controller directly.

VREF: The output of the trimmed precision reference. This reference maintains within 1% of its initial value over its entire line, load, and temperature range.

APPLICATION INFORMATION

For designs requiring input-output isolation, the UC3965 is used in secondary side output voltage sensing. As shown in Fig. 1, the precision reference and low offset error amplifier can be used in converters, such as the isolated flyback, where the primary side error amplifier is not used or simply not present. In this case, the UCC3809 is used as the primary side controller.

The precision reference of the UC3965 is tied to the non-inverting input of the device's internal error amplifier. The output voltage of the converter is resistively divided and compared to this reference at the inverting input. This error amplifier has a low 1mV input offset voltage that insures accurate regulation of the output. The internal error amplifier drives the inverting input of the output buffer (OB) which drives an optocoupler diode. The wide range VCC voltage enables the device to be biased from the secondary side output voltage rail, resulting in closed loop soft start.

As the output voltage increases beyond its desired value, the voltage difference at the error amplifier increases. This results in less drive at the inverting input of the internal buffer, increasing its output drive to the optocoupler. If the application does not require input-output isolation, this buffer could be used to drive the PWM directly.

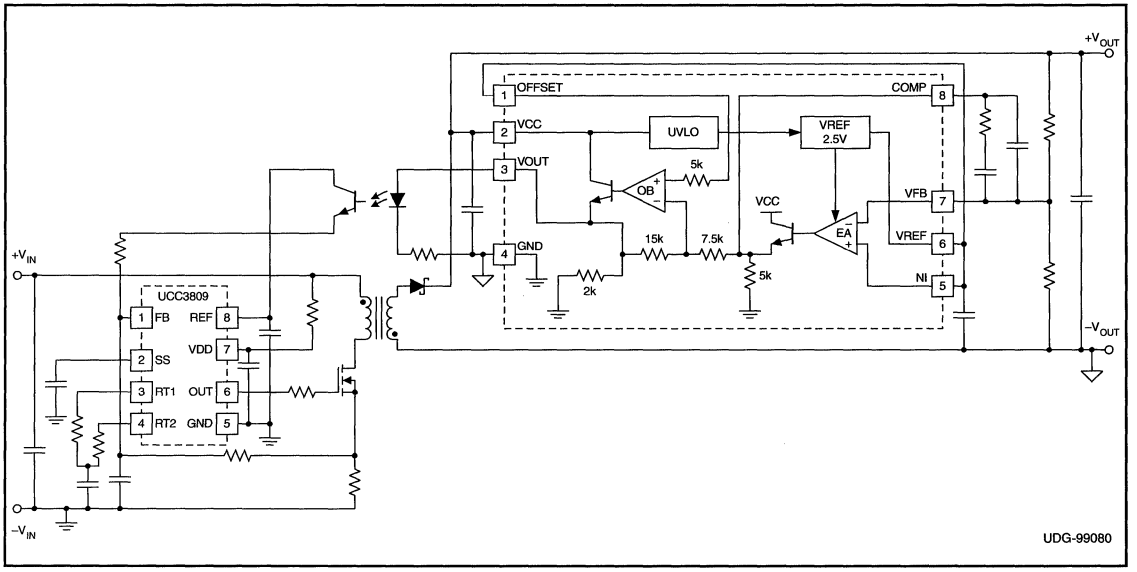


Figure 1. Typical application diagram.

ADDITIONAL INFORMATION

For additional application information biasing the UC3965, please refer to the following publication:

[1] Application Note U-165, *Design Review: Isolated 50W Flyback with the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier*, by Lisa Dinwoodie.

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A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

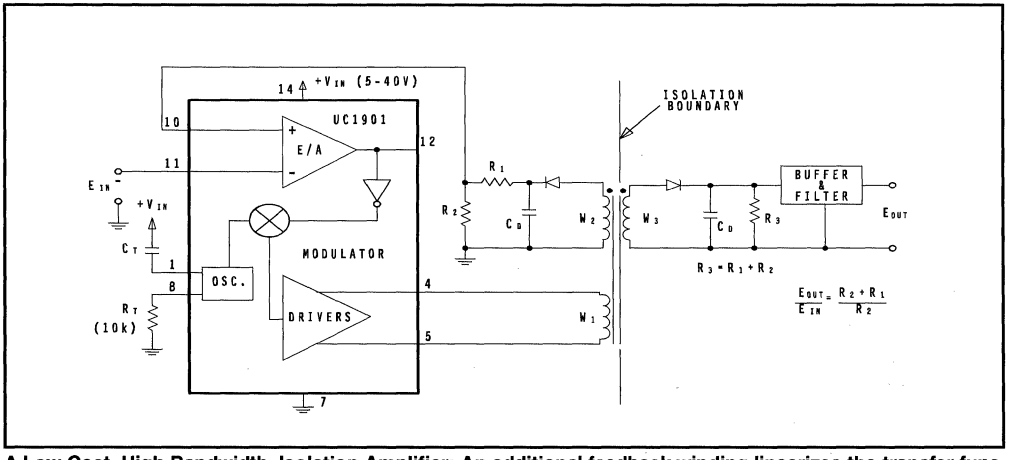
The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal, AC, transfer functions can be established across the isolation boundary.

The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W2 and W3) on a small signal transformer. The demodulated signal from winding W2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

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OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES USING THE UC 3901 AND UC3903

Numerous techniques and devices are available to the designers of optocoupler feedback circuits. The more traditional approaches utilize either an adjustable shunt regulator like the TL431 device or an op-amp and voltage reference as the optocoupler driver. While these approaches do satisfy the basic requirements in many applications, quite often they lack the performance that is achievable from a more sophisticated circuit. Too often, these low cost solutions necessitate additional protection circuitry elsewhere in the control circuit to overcome the deficiencies in the feedback path.

A variety of low cost supervisory ICs contain the required building blocks for the more demanding optocoupler feedback drive applications. Initially developed to address other specific power supply tasks, several control ICs excel in the role as precision optocoupler control and drivers.

The basic building blocks necessary for optocoupler feedback control are a precision reference, an error amplifier and a drive stage capable of approximately 20 milliamps. In a typical application, the power supply output voltage is monitored and compared to a reference voltage to the error amplifier inputs. Loop compensation and gain are programmed around the amplifier, and the resultant error voltage (Ve) modulates the optocoupler drive current, hence feedback.

In addition to the simple regulation of output voltage, several other housekeeping functions can be performed on the secondary side of the power supply - all with a single integrated controller. Fault protection, for example, from an over voltage or an over current condition can be detected and used to override the normal optocoupler drive. An undervoltage lockout feature could prevent false feedback information during power-up and power down sequences of the power supply. Also, a POWER-OK indicator could separately communicate with the primary side controller, or used to gate the optocoupler drive at the secondary side.

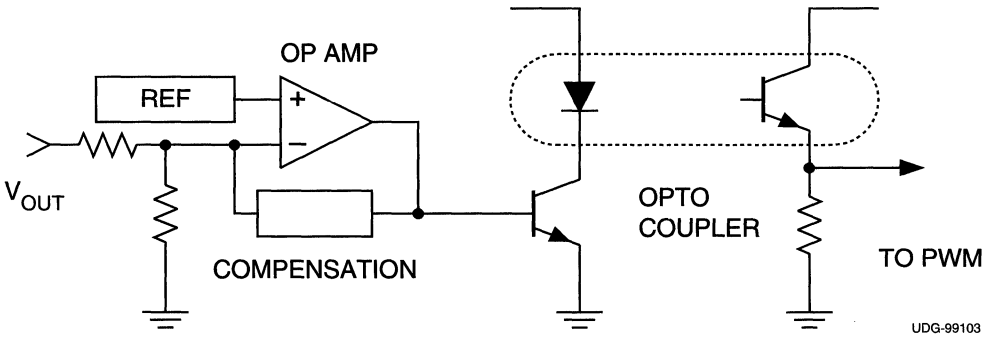

Figure 1. Basic optocoupler drive circuit.

THE UC3901 ISOLATED FEEDBACK GENERATOR

Many isolated feedback applications required higher performance than can be obtained from an optocoupler feedback technique. Generally, these fall into one of two categories; high frequency switchers (above 250kHz) and those with very high voltage isolation requirements (greater than 5kV). The UC3901 was developed to amplitude modulate a high frequency carrier applied to a transformer in place of the optocoupler. A peak detection circuit is used to reconstruct the error voltage waveform across the isolation boundary.

By disabling the internal oscillator, no chopping occurs and the outputs operate as linear drivers. When placed across an optocoupler this configuration yields similar results to other drive techniques - with two advantages. First, a closed loop startup of the power supply can be obtained since both inputs to the error amplifier are made available. Rather than using the traditional approach of soft-starting the error amplifier output, the noninverting, or reference input is gradually ramped up. This technique prevents a large overshoot from occurring as the output approaches regulation. In contrast to the prior method, the amplifers loop compensation network is not abnormally biased during startup - causing the output excursions. Additionally, an over and under voltage detection is available at the UC3901 "Status output" pin. This open collector output can drive a separate fault indication optocoupler for communication to the PWM controller.

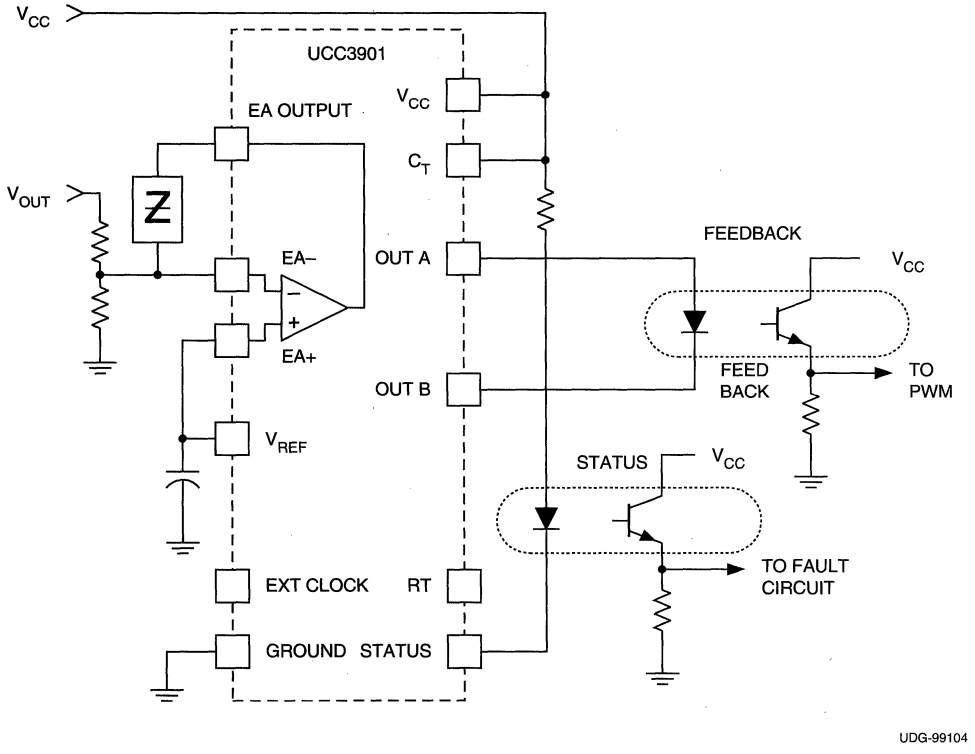

Figure 2. Optocoupler drive circuit features additional protection.

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Adjustable Electronic Load for Low Voltage DC Applications

*Operates down to 2.5V

by Bill Andreycak and John Wiggenhorn

Testing power supply regulation over a specified output current range is greatly simplified with the use of an adjustable electronic load. Load current can be varied from zero to the full rated value with the twist of a panel mounted potentiometer or by a digital interface. This design note will feature the design of a self biased, constant current adjustable electronic load which is fully operational with input voltages down to 2.5V.

Most electronic loads rely on the available load voltage to power the control and drive circuits. Since a majority of supplies have output voltages of 5 volts, or more, it has been relatively simple to obtain integrated control circuits which operate at those levels. But the emerging trend towards lower supply voltages, for example 3.3V, 3.0V, 2.7V and even 2.5V logic ICs has eliminated many popular control ICs and techniques from consideration. The UC39432 Precision Analog Controller is fully operational from a supply voltage as low as 2.2V and is usable for this electronic load application, in additional to numerous others. This IC features a precision 1.3V reference voltage, a general purpose operational amplifier and a 100mA open collector NPN transistor. Although primarily intended for optocoupler driving in a feedback loop, the UC39432 is a programmable transconductance amplifier and is adaptable to fulfill many low voltage control requirements. Additional information can be obtained from the device's datasheet

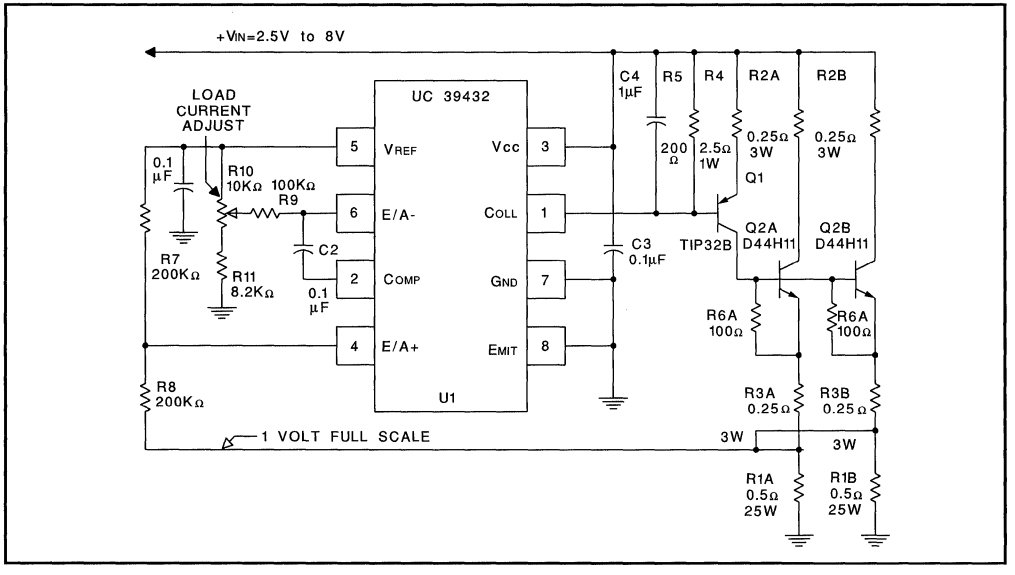

Figure 1. Electronic Load Circuit Schematic

Electronic Load Circuit Operation:

The UC39432 error amplifier noninverting input (pin 4) senses the voltage developed across the paralleled current sense resistors, R1A and R1B. This amplitude is level shifted up by two resistors (R7 and R8) to the ICs reference voltage to maintain the input within its useable common mode range. The inverting input (pin 6) of the amplifier is connected to the wiper of the current adjust potentiometer which programs load current. A 100k ohm series resistor (R9) balances the input impedances while the 8.2k ohm resistor (R11) provides offset to the potentiometer for better resolution. Compensation uses a 0.1μF capacitor (C2) which turns the amplifier into an integrator for good DC load stability. Both the input supply voltage to the IC (pin 3) and the 1.3V reference (pin 5) are bypassed with 0.1μF capacitors (C4 and C1) for noise rejection.

The power stage of this load consists of a PNP driver (Q1) to the NPN power transistors (Q2A and Q2B) in a Darlington configuration. Very common D44H11 (10A/80V) TO-220 type NPN transistors are conservatively utilized. They provide plenty of flexibility for higher output voltages and higher current applications. Heatsinking incorporates two AAVID Engineering type #E5301 parts and number #150 spring clips for the TO-220 devices. Specifications indicate a 65 degree C rise for 10 Watts of power dissipation without forced air. This is worst case operation for each transistor with an 8V input and 4A load current. Emitter ballast resistors (R3A and R3B) are included to balance the load current evenly between the NPN transistors. These two devices are held off by 100 ohm base to emitter resistors (R6A and R6B). Series collector resistance (R2A and R2B) is used to further reduce the transistor power dissipation while still enabling 2.5V operation at full load. Base drive for both is provided by a TIP32B (3A/80V) PNP transistor (Q1). Emitter resistance (R4) is used to reduce the system gain and R5 holds Q1 off with no base drive. A 1μF capacitor (C4) between the input supply and the base increases stability and reduces the potential for a load surge at power-up.

This general purpose, constant current electronic load can be easily modified for higher current and higher voltage applications with few changes. Additional NPN transistor and heatsink stages can be paralleled to draw higher currents and to divide the heat evenly amongst more transistors. The only other change needed is to the current sense resistor value which should be scaled to develop 1 volt at full current. Low voltage operation may also warrant reducing the value of R4 to provide more base drive with the same voltage drop.

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Using Copper PCB Etch for Low Value Resistance

by Larry Spaziani

INTRODUCTION

Current sensing in power supplies and motor controls demand the use of a very low value resistor. Each application varies in need for resistance value, power rating, size, form factor, inductance, temperature coefficient and accuracy. To meet some of these applications, the copper of a printed circuit board (PCB) can be utilized, but has some distinct limitations. This design note provides design equations and recommendations for designing resistors with PCB copper.

DESIGN OF A COPPER PCB RESISTOR

The resistance, as a function of temperature, for a piece of metal, is given by the equation:

$$R(T) = \frac{S(T) \bullet l}{a}$$

with the units

R=Resistance, Ω
S(T)=Resistivity, Ω–cm
l=Length, cm
a=Area, cm^2

The characteristics of copper which are pertinent to the design of a copper PCB resistor are [1]

Electrical Resistivity:
$1.7241 \bullet 10^{-6} \Omega - cm$ @ 20°C

Temperature Coefficient of Resistivity:
+0.0039 per °C

Composition:
99.5% Pure Copper, typically

These constants apply to the standard commercially annealed copper used in PCB technology.

The resistivity of copper, as a function of temperature, is therefore defined as:

$S(T) = 1.7241 \bullet 10^{-6} \bullet [1 + 0.0039 \bullet (T - 20)] \Omega - cm$

where T is the copper temperature in °C.

One PCB Definition which is also pertinent to resistor design is:

1oz copper is defined as 1 ounce of copper deposited over 1 square foot of surface area. This results in a copper clad PCB with a typical copper thickness of 0.0014 inches ±0.0002 inches. 2oz copper is simply twice as thick.

Using these parameters to calculate the resistance of a given length, width, and thickness of copper PCB etch results in the formula:

$$R(T) = \frac{S(T)[\Omega - cm] \bullet Length[cm]}{Width[cm] \bullet Thickness[cm]}$$

$$= \frac{S(T)[\Omega - cm] \bullet \frac{1000mils}{2.54cm} \bullet Length(mils)}{Width(mils) \bullet Thickness(mils)}$$

The use of a low value sense resistor implies that the current in that resistor can be quite high. A copper etch on a PCB will self heat due to the power dissipated by the resistor. MIL-STD-275E [2] provides design guidelines relating copper etch current to temperature rise and etch dimensions. Figure 1 recreates sections of the MIL-STD-275E curves. A temperature rise, above

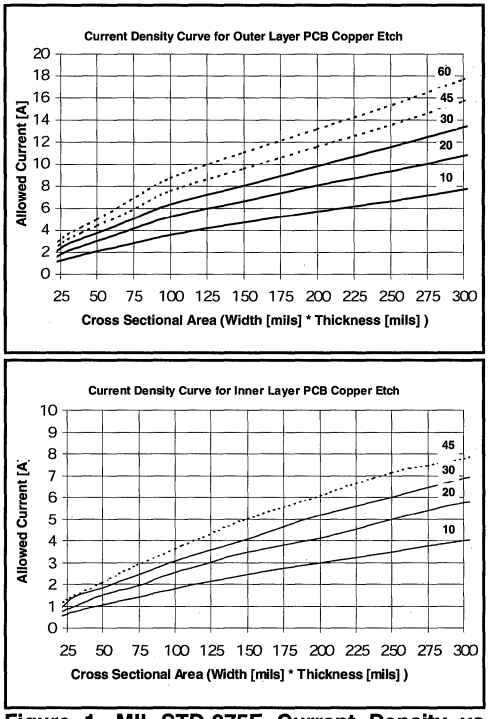

Figure 1. MIL-STD-275E Current Density vs Temperature Rise Curve for Outer and Inner Copper Layers

ambient temperature, can be found by knowing the current and the area of the copper etch.

Example: Calculate the length and width of a 10mΩ MAXIMUM PCB resistor using 1oz on an outer layer of a PCB. The resistor must carry 10A maximum while maintaining no more than a 30°C temperature rise above ambient. Ambient temperature for normal operation is 10°C to 60°C.

Step 1:

Find the cross sectional area to carry 10A with ≤ 30°C rise, and solve for the minimum width of the resistor.

From Figure 1, 205 $mils^2$ are required to carry 10 Amperes. 1oz copper is 1.4mils thick, resulting in a minimum width for the resistor of 146mils.

Set Width = 150mils

Step 2:

Find the length of the resistor, insuring that it is designed for 10mΩ maximum at 60°C ambient +30°C rise (copper temperature is 90°C).

From the equations

$$S(90) = 1.7241 \bullet 10^{-6} \bullet [1 + 0.0039 \bullet (90 - 20)]\ \Omega - cm$$

and

$$R(90) = \frac{S(90)\left[\frac{\Omega - cm}{°C}\right] \bullet \frac{1000mils}{2.54cm} \bullet Length[mils]}{Width[mils] \bullet Thickness[mils]}$$

Solving for R(90°C) = 10mΩ, using150 mils for

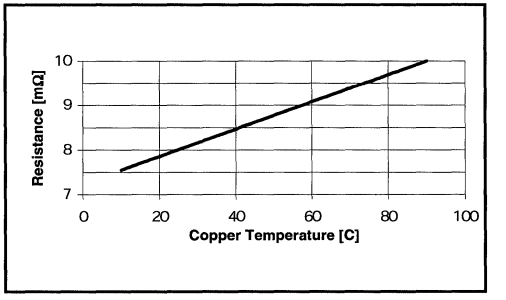

Figure 2. Resistance vs Copper Temperature for Example Design

Width and 1.4 mils for Thickness results in Length = 2.43 inches.

Final Dimensions (inches): 2.43 (L) x 0.150 (W) x 0.0014 (T)

The final resistance, as a function of the copper temperature, is shown in Figure 2.

Table 1 provides the required dimensions for a 1oz PCB copper resistor given a maximum current and desired voltage drop. Table 1 assumes

AMPS	Desired Voltage Drop 10mV	25mV	50mV	Width [in]
	PCB Etch Length [in]			
1	0.162	0.405	0.810	0.010
2	0.243	0.608	1.215	0.015
3	0.405	1.013	2.025	0.025
4	0.648	1.620	3.240	0.040
5	0.891	2.228	4.456	0.055
6	1.053	2.633	5.266	0.065
7	1.377	3.443	6.886	0.085
8	1.701	4.253	8.506	0.105
9	2.025	5.063	10.126	0.125
10	2.430	6.076	12.152	0.150
11	2.754	6.886	13.772	0.170
12	3.078	7.696	15.392	0.190

Table1. Dimension Solver for Given Current and Desired Voltage Drop for 90°C Maximum Copper Temperaturre

a maximum operating ambient temperature of 60°C, with the width specified for a 30°C temperature rise. The required resistance is equal to V/I and is calculated at a copper temperature of 90°C.

Some PCB physical and layout characteristics should be considered when designing a PCB resistor.

- The thickness tolerance of PCB copper may vary from supplier to supplier and relative to location on a PCB. A typical tolerance is ±0.2mils/oz.
- Etchback will reduce the copper area, thus increasing the resistance per unit length. Etchback has a larger impact with narrow runs, where the width/thickness ratio is lower. It is recommended that widths of ≥ 0.025 inches be used.
- The copper resistor, if it is on an outer PCB layer, should be solder masked over the entire resistive area. Solder on the copper will reduce the resistance.
- Vias through the resistor will effect the resistance.
- Curved or serpentine resistor patterns may be utilized as long as the overall width and length, including curves, is understood.
- A copper resistor connected to two larger copper planes will have a lower temperature rise than predicted by the MIL-STD-275E curves due to the heatsinking of those copper planes.

CONCLUSIONS

The design of a PCB copper resistor is straightforward once operating parameters such as voltage drop, operating current and operating ambient temperature are known. Tolerances due to PCB technology will effect the accuracy of a PCB resistor and should be considered. The length-to-width ratio of a PCB resistor is quite large due to the low resistivity of copper, but when the area is available on a PCB, this resistor is essentially free.

Applications which require current limiting are ideal for use with a PCB resistor, as current limiting can be set quite accurately at the maximum operating temperature where current limiting is most critical. Average current mode control applications require precise voltage drops independent of temperature and current levels. PCB resistors are therefore not recommended for use as an Average Current Mode control sense resistor.

REFERENCES

[1] Reference Data for Radio Engineers, Howard W. Sams & Co. Inc., Sixth Edition 1977.

[2] MIL-STD-275E, NOTICE 1, 8 July 1986, Military Standard Printed Wiring for Electronic Equipment.

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THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

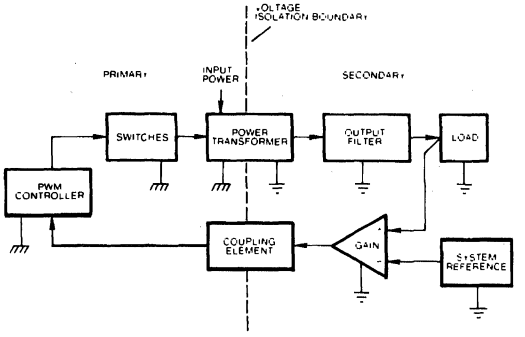


FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best understood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

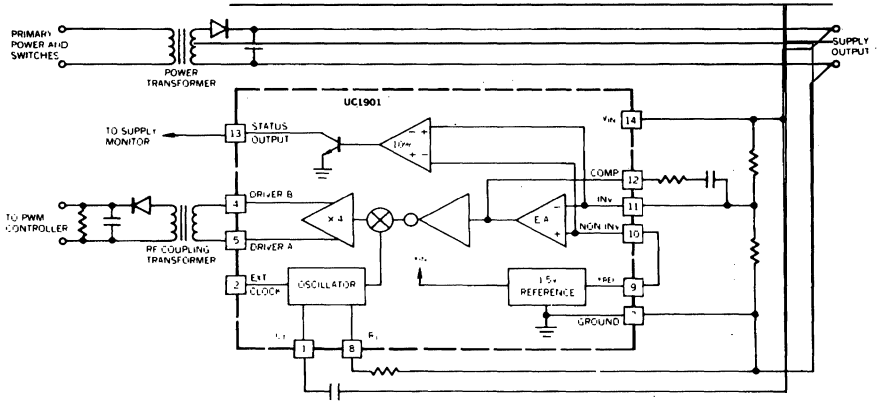


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer:

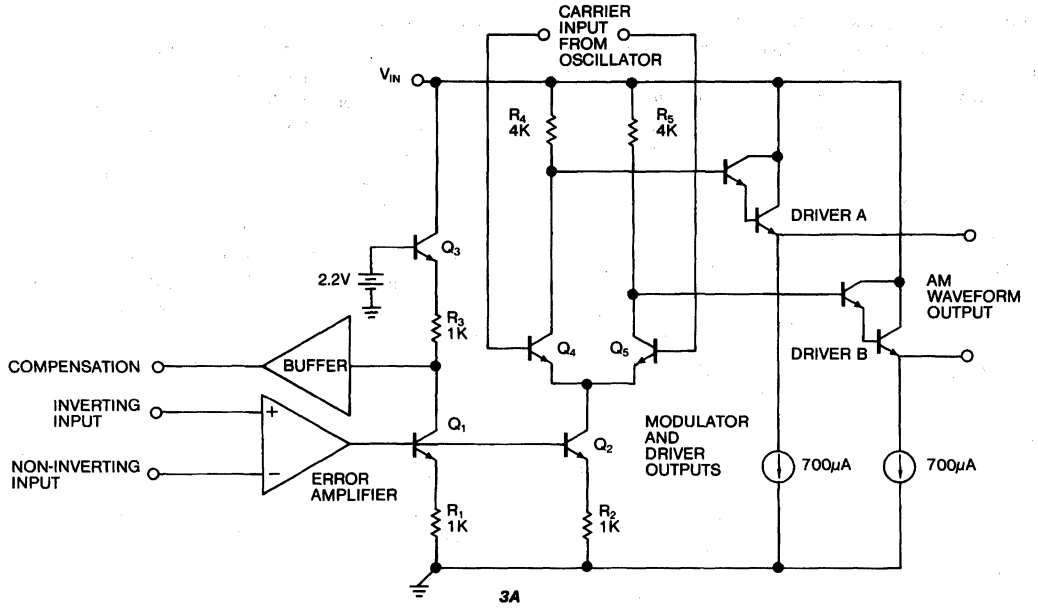


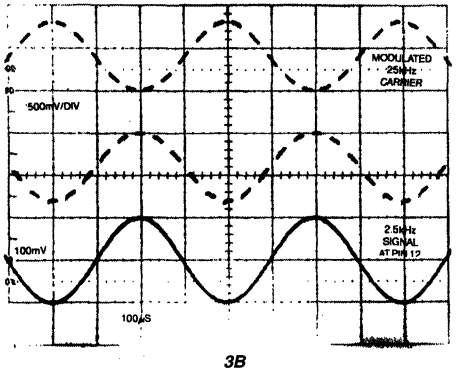
FIGURE 3: The Compensation Output on the UC7907 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator: Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward converters are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.



3B

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine-the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feed back network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin 12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

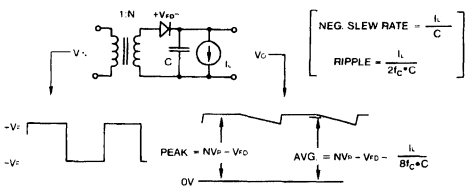


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

(1) $$L_M \geq \frac{V_P}{4 f_c I_P}$$

Where: L_M = the magnetizing inductance,
V_P = the peak carrier voltage across transformer inputs,
f_c = the UC1 operating frequency,
I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1 mH. Alternatively, if the carrier frequency is raised to 1 MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

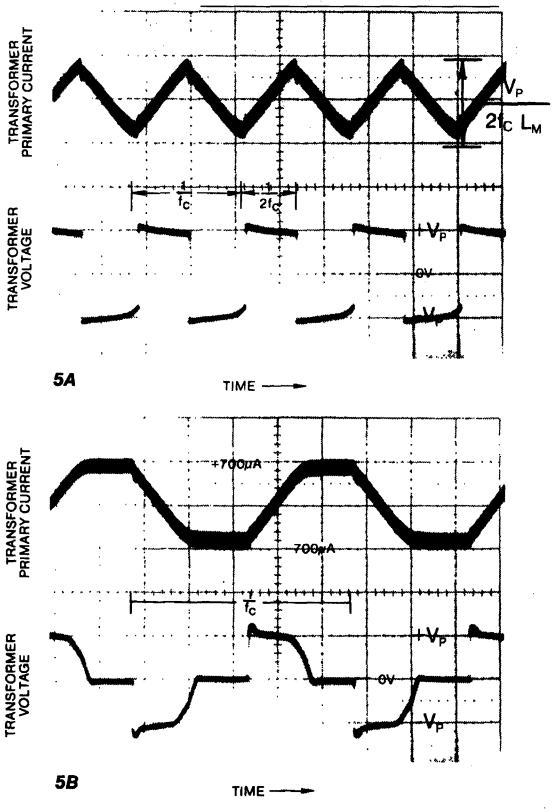


FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer; the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the > 50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt.

When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 1 A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

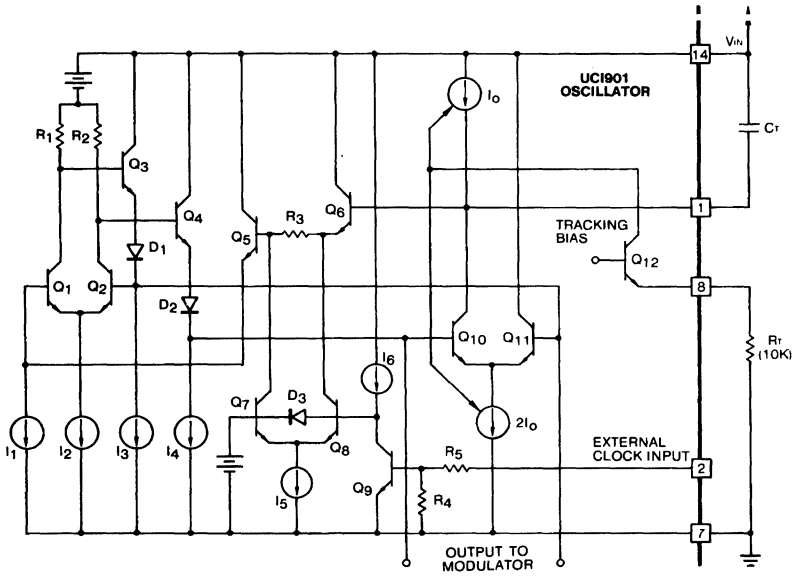


FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of-the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

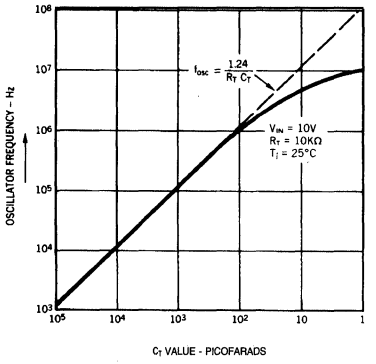


FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

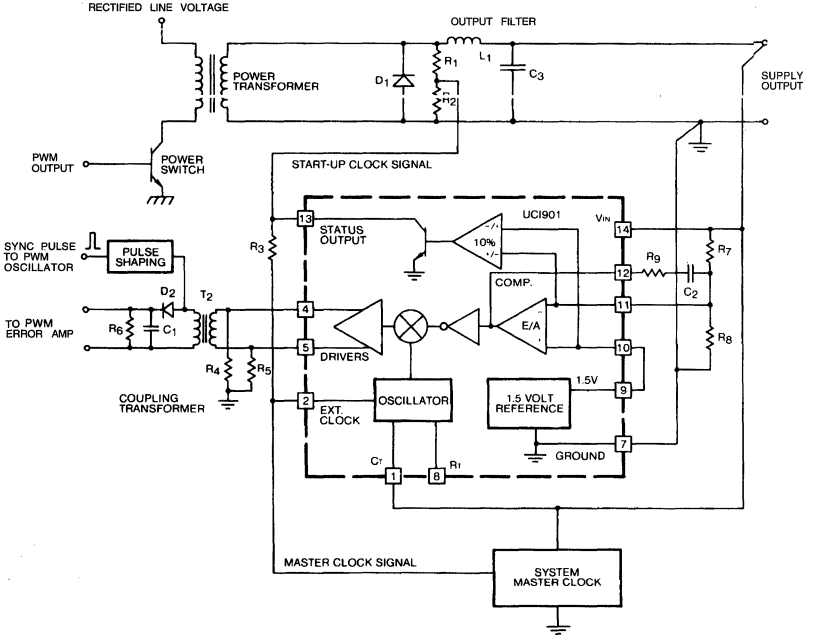


FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (< 150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3) \quad \frac{v_{OUT}}{v_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

V_{IN} = level of the rectified line voltage,

V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,

T_P = One period of the switching frequency,

L_M = Magnetizing inductance of the primary winding,

C_F = A total effective output filter capacitor,

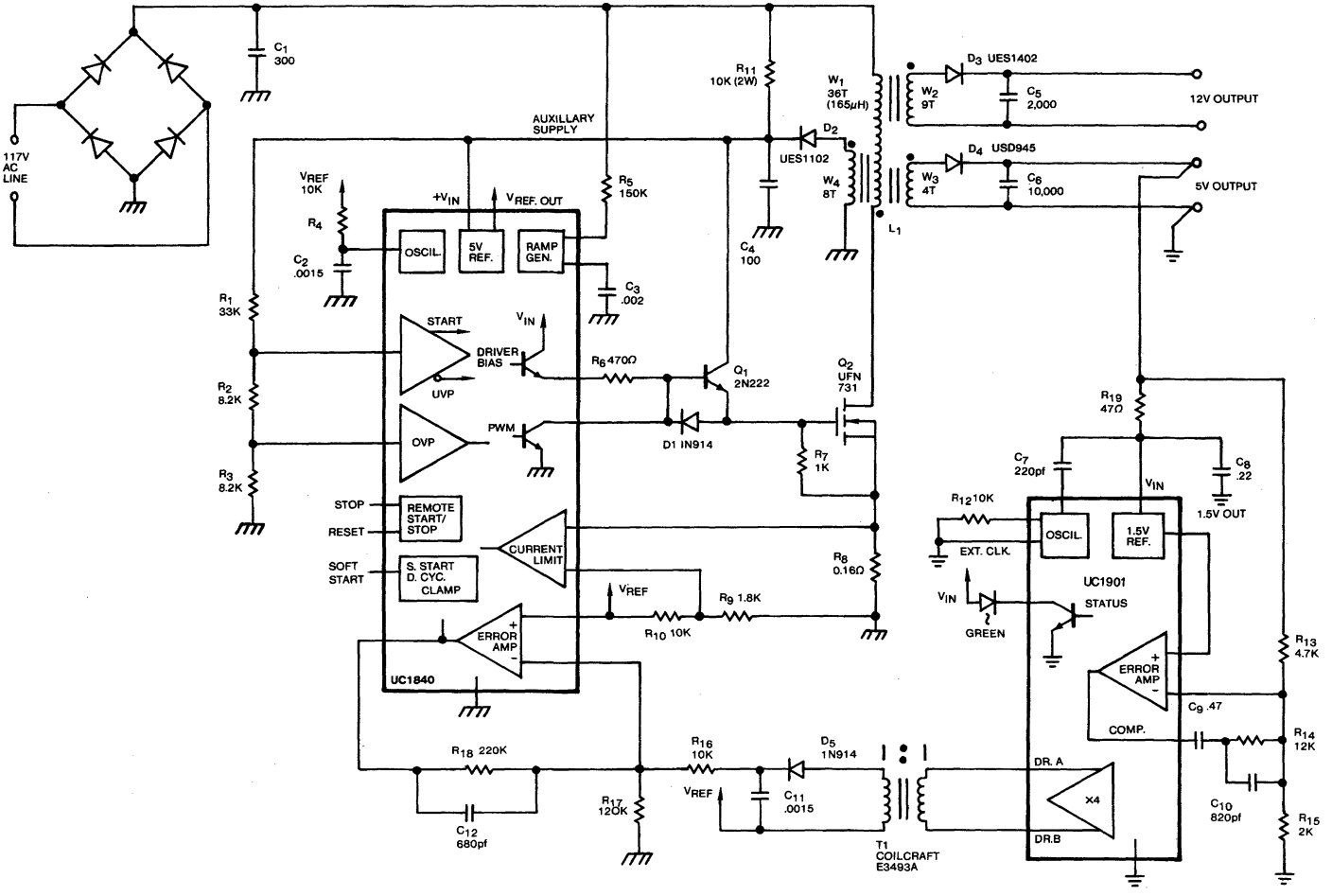


FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\ T_P}{R_5\ C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

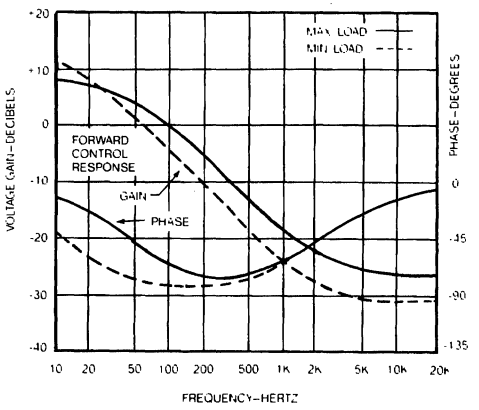


FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

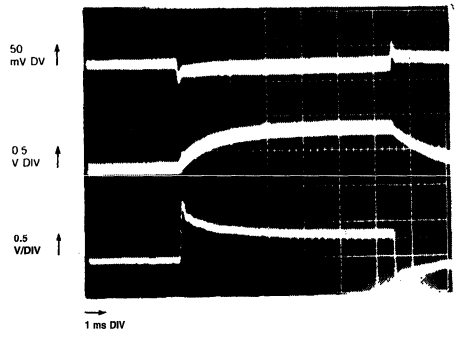


FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

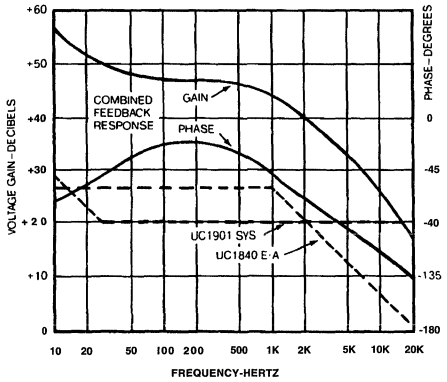


FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

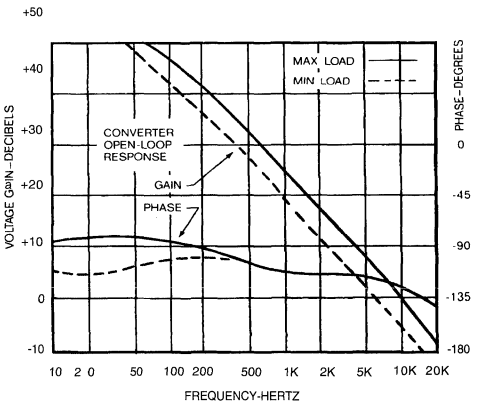


FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of > 50°.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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UC3907 LOAD SHARE IC SIMPLIFIES PARALLEL POWER SUPPLY DESIGN

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INTRODUCTION

Many power supply manufacturers have found it economically feasible to make standard modular power supplies which are easily paralleled for higher current applications. If special provisions are not made to equally distribute the load current among the paralleled supplies, then one or more units will hog the load current leaving the other units essentially idle. This results in greater thermal stresses on specific units and a reduction in the system reliability For example, reliability predictions will indicate that a component operating at 50 degrees above ambient will have one-sixth the lifetime of the same component operating at 25 degrees above ambient [1].

This paper will examine methods for load sharing presently being implemented discrete/y and then cover Unitrode's single chip solution, the UC3907 Load Share Controller, in several parallel power applications.

SYSTEM REQUIREMENTS

The basic requirements of a power supply system consisting of a number of sources paralleled to increase the total load current are:

- Maintain a regulated output voltage under variations in line or load.
- Control the output current of each supply so they share the total load current equally.

To maximize reliability of the system, there are the following features:

- Achieve redundancy, so that a failure of any one supply can be tolerated as long as there is sufficient current capacity available from the remaining power units.
- Implement a load sharing method without any external control system.

In addition, these are the following desirable features:

- To have a common, low bandwidth share bus interconnecting all power units.
- Achieve good load sharing transient response.
- The ability to margin the system output voltage with one control.

In other words, the combination of power supplies behave like one large supply with equal stress on each of the units. Also, reliability can be optimized by taking advantage of load sharing to incorporate modular redundancy.

LOAD SHARING TECHNIQUES

There are a number of schemes to achieve load sharing. Five approaches are discussed here, with an attempt made to investigate their application, highlighting features and concerns.

THE DROOP METHOD

The simplest method to load sharing is referred to as the droop method. It is an open loop technique which programs the output impedance of the power supplies to obtain load sharing. This method exhibits very poor current sharing at low currents and improves at higher currents, but can still have large current imbalances between supplies. An example of this method is shown in Fig 1 where as the individual supply current increases, the feedback voltage will decrease. This will allow other supplies to distribute more current. The programmed output impedance is given by:

$$Rout = 0.01\ Rs\ N$$

The disadvantages to the droop method are: degradation of load regulation, each module must be individually tweaked to achieve good current sharing, and difficulty in current sharing between parallel modules with different power ratings.

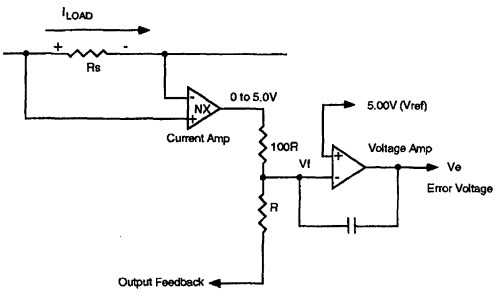

Fig 1 - The Droop method programs the output impedance of the power supplies to achieve load sharing. It is a simple open loop method, but is not accurate.

DEDICATED MASTER

Current mode supplies can accommodate several configurations to achieve a form of load sharing. One approach is to select a master module to perform the voltage control and force the remaining modules (slaves) to act as current sources, as shown in Fig. 2. This technique is facilitated with current mode control, since the error voltage is proportional to load current. If the units were similar in design then a given error voltage on the output of the voltage, or error amplifier will force all units to source the same load current. This technique achieves load sharing but does not achieve redundancy, since if the master fails, the entire system becomes disabled. Another concern with this technique is that the high bandwidth voltage loop is being bussed around the system and is prone to noise pick-up.

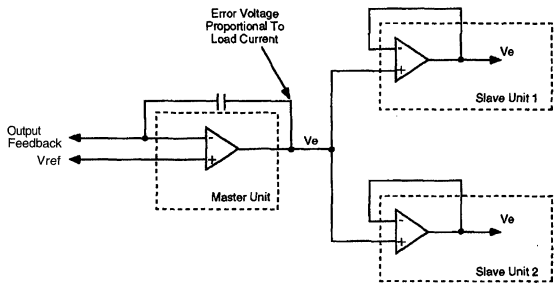

Fig 2 -A dedicated Master approach with current mode supplies will facilitate current sharing but does not achieve redundancy.

EXTERNAL CONTROLLER

Another method is to use an external controller to perform the load sharing. This is achieved by comparing all load sharing signals from the individual power units and adjust the corresponding feedback signal to balance the load currents. This system does perform well but requires an additional controller and multiple connections between the controller and each supply.

AUTOMATIC CURRENT SHARING - AVERAGE CURRENT METHOD

For Automatic current sharing no external controller is required and a single share bus interconnects all the supplies. This requires an adjustment amplifier that compares a current signal from the share bus to the individual units current, and adjusts the reference of the voltage amp until equal load current distribution is achieved.

The average Current method is a patented technique where each power module's current monitor drives a common share bus via a resistor, as shown in Fig 3. The adjust amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjusts the reference accordingly. The node where all resistors connect is a representation of the average load current contribution. While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into current limit, causing the share bus to be loaded down and the output voltage to regulate to the lower adjust limit. A similar failure mode will exist if the share bus is shorted or if any unit on the share bus is inoperative.

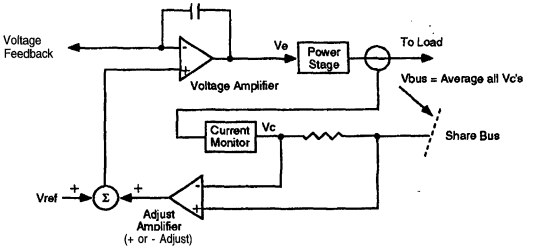

Fig. 3 - The average current method compares the individual load currents to the average load current.

AUTOMATIC CURRENT SHARING - HIGHEST CURRENT METHOD

This technique for automatic current sharing shown in Fig 4 compares the highest current module to each individual current, and adjusts the reference voltage accordingly to correct the imbalance of load current. This technique is similar to the average current method except that the resistor is replaced with a diode, allowing only one unit to communicate on the share bus. This method provides for excellent sharing among the slaves with an error in the master's load current contribution because of the diode.

The UC3907 Load Share Regulator has improved on this method by replacing the diode with a unidirectional buffer to reduce the master's error. An inoperative or insufficient capacity supply will not effect the sharing of the operational units. A shorted share bus will disable the reference adjustment section used for load sharing, making the units operate as stand alone.

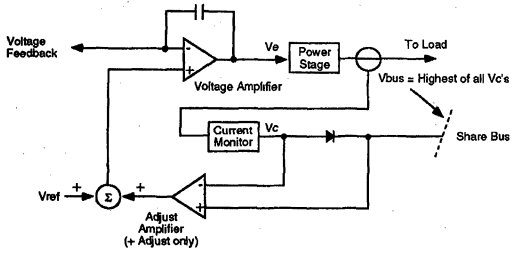

Fig. 4 - The highest current method compares the individual load currents to that of the highest. This method has several advantages over the average current method of load sharing. The UC3907 has implemented and improved version of this technique.

USING THE UC3907 - LOAD SHARE REGULATOR IC

A review of the current sharing technique used on the UC3907 and operating principles will help the reader to understand the application examples that follow and to use the IC in other examples.

A generic load share system with the basic bus connections required to perform accurate output voltage control and load sharing is shown in Fig 5. The output voltage is sensed with a fully differential, high-impedance voltage amplifier. Each individual power supply current is sensed with a differential current amplifier, and is used for the load share portion of the circuit. The share bus signal interconnecting all the paralleled modules is a low-impedance, noise insensitive line. The connection diagram is shown in FIG 6. The following discussion of the voltage and current sharing loops should help the reader understand the operation and features of the IC.

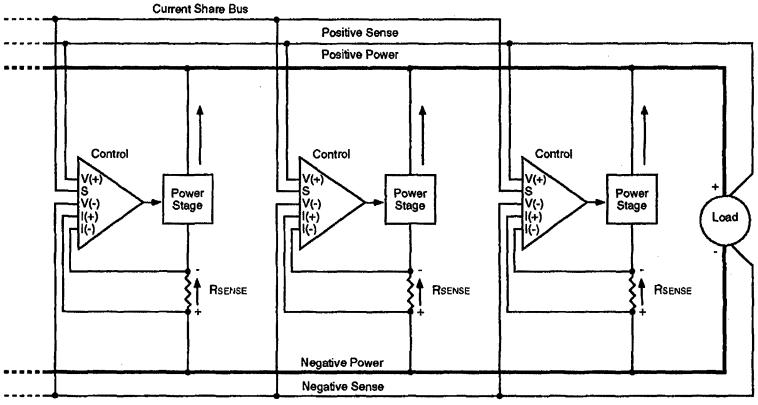

Fig. 5 - System connections for modules with independent load sharing.

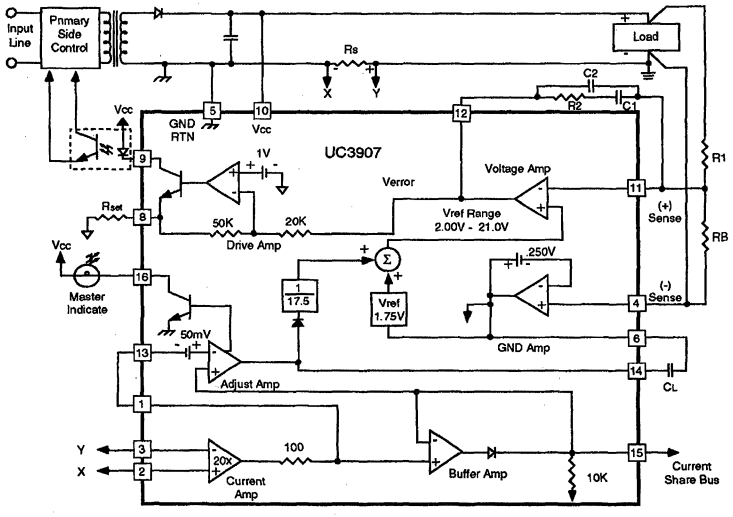

Fig. 6 - The UC3907 will control output voltage and equally distribute load current among the power modules.

THE VOLTAGE LOOP

THE VOLTAGE AMP

This Amplifier is the feedback control gain stage for the power modules output voltage regulation, and the overall voltage loop compensation will normally be applied around this amplifier. The output swing is limited to 2 Volts to improve the large signal response of the system. The voltage amplifier accomplishes the high impedance positive sensing, and the ground amp, the high impedance negative sensing.

THE GROUND AMP

This amplifier is a unity gain buffer with a 0.250V offset. The offset allows the amplifier negative headroom to return all control bias and operating currents while maintaining a high impedance negative sense input (pin 4) where this input is referred to as "'true" ground. The output of this amplifier is referred to as Artificial Ground. The 0.250V offset is added to the 1.750V bandgap reference to obtain the 2.00V reference, as seen by the voltage amp, and is trimmed to +/-1.25%.

The ground return (pin 5) should be the most negative voltage available and can range from zero to 5V below the negative sense input. All the IC's current will return through the ground return pin.

THE DRIVE AMP

This amplifier is an inverting amplifier with a gain of -2.5, which couples the feedback signal to the power controller. The Current setting resistor Rset helps to establish the forward transfer function of the control loop and the maximum drive current. The polarity of the drive amp stage is such that an increasing voltage at the plus sense input (pin 11) will increase the opto-couplers current, thereby reducing the primary side PWM's duty cycle. This will insure proper startup since there is no energy on the secondary side during initialization of the power system.

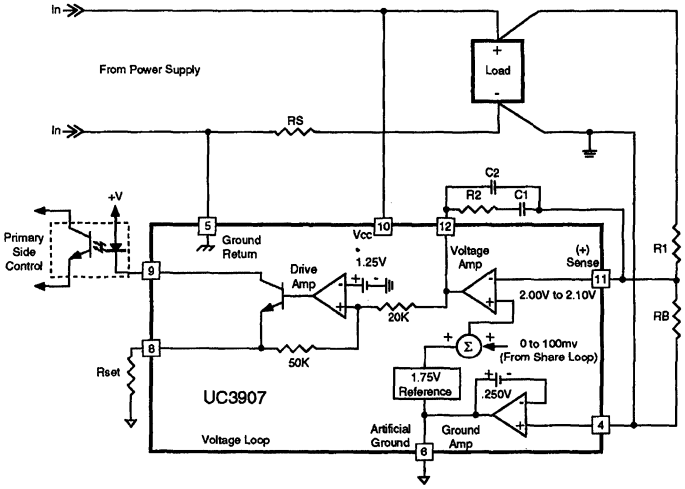

Fig. 7 - The UC3907 Voltage Loop achieves high impedance differential sensing along with optical coupler driving capability.

THE CURRENT LOOP

THE CURRENT AMP AND BUFFER AMP

The current sharing portion of the IC utilizes the current amp, the buffer amp, and the adjust amp as shown in Fig. 8. The Output of the current amp is an analog representation of individual load current, where the output voltage is given by: Vca=20*Rs*Iout. The current amp output feeds an input of a unidirectional buffer which drives the current share bus. Since the buffer amp only sources current, it insures that the module with the highest load current will be the master, or communicator to all other modules, and drives the bus through a low-impedance. All other buffer amplifiers will be inactive with each exhibiting a 10K ohm load impedance to ground.

THE ADJUST AMP

The adjust amplifier will compare its own load current with that of the highest current module, and force a command to adjust the individual modules reference voltage, (as seen by the voltage amp) to maintain equal current sharing. It is a transconductance type amplifier in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to artificial ground. The ground referenced compensation will act similar to that of integral compensation, but without the non-inverting signal feedthrough problems, thereby filtering both inputs from

unwanted noise. The adjust amplifier has a built in 50 millivolt offset on its inverting input, which forces the unit acting as a master to have a low output resulting in a zero adjust command. While the 50mv offset represents an error in current sharing, the gain of the current amplifier reduces it to 2.5 millivolts across the sense resistor. This results in all slave modules sharing equally and the master module running a few percent higher. The offset also provides some immunity from cycling, or fighting for master position due to low frequency noise.

STATUS INDICATE

The status indicate pin is designed to indicate which unit is acting as the master. Its open collector output is activated when the adjust amp output is in the low state. In a case of an overcurrent fault with one of the many paralleled units, this pin will indicate the unit with the highest current which will help diagnose the faulted module. A zero current or low current fault is transparent to the other supplies' and has no effect on voltage regulation and current sharing.

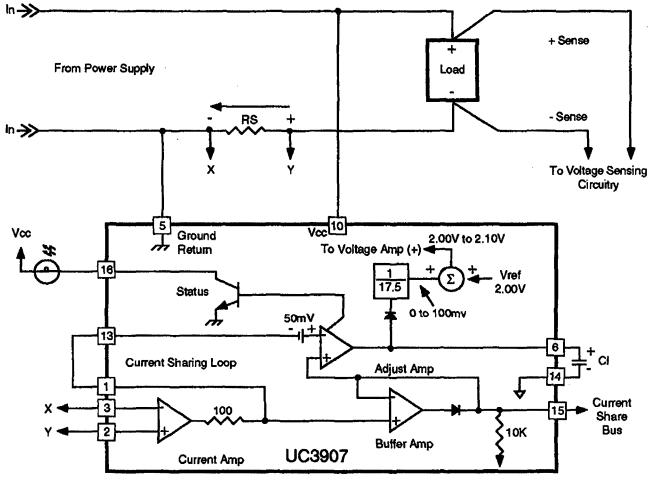

Fig. 8 - Current sharing is achieved with the UC3907 by comparing the individual module's current to that of the highest current module. The necessary adjust command increases the voltage amp reference to accomplish equal load sharing.

START-UP FOR A PARALLEL POWER SYSTEM

Start-up conditions need to be considered in a parallel power supply architecture. A start-up timing example of four 5V power modules in parallel is shown in Fig. 9. Once the primary power is applied, the power stage will be requesting maximum duty cycle until the individual units feed back a signal to regulate the output voltage. At time t1, supply #1 has become the master due to its higher reference voltage. This forces the output voltage to regulate above the other units. The other units will feedback a zero duty cycle signal to the power stage and remain idle. At this point the master unit is supplying all the supply current, and outputting the corresponding current signal on the share bus. The other units' adjust amplifiers sense the difference between their individual load currents and the master's, and start to slew up the adjust amp output to increase their references. At the same time the master's adjust amplifier output remains clamped below the adjust threshold having no effect on its original reference. At time t2 the other three adjust amps have exceeded the adjust threshold and have started to effect the reference as seen by the voltage amp.

At time t3 the unit with the closest reference to the master, supply #2, has reached the point where its references is essentially equal to the master's and the load current becomes equally distributed between the two. The other two modules, #3 and #4, are still adjusting their references and are not yet contributing to the load current. At time t4 the 3rd unit has reached the desired reference and the load current has been equally split between the three, and at time t5 the final unit has completed its reference adjustment, thereby completing the load sharing. If it is necessary to have the units come up sharing, then a soft-start scheme will need to be implemented on the primary side modulator which needs to be much slower than the adjust time. The total adjust time from t1 to t5 for this example is given by:

$$t = \frac{Cl\ Va}{I}$$

where Cl = adjust amp compensation
Va = adjust amp swing
I = Adjust amp max current - 220ua

Cl is chosen from the desired bandwidth

$$Cl = \frac{gm}{2\pi F}$$

where typ gm = 3mS and F = Adjust amp bandwidth.

If the required adjust amp bandwidth were 500 Hz, then Cl will be 1 uF. The adjust amp output for the lowest reference will adjust to a voltage calculated as follows:

$$Vadj = (VREF_{max} - VREF_{min})\ 17.5 + 1$$
$$= (30mv\ 17.5) + 1 = 1.53$$

The adjust amp must slew from approximately 0.7V to 1.53V at a slew rate of 220mV/ms which equates to a complete sharing delay time of 3.8 ms.

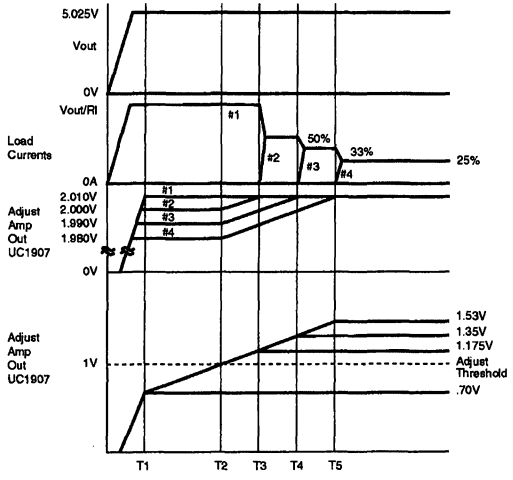

Fig. 9 - Start-up timing of a four module power system using the UC3907 (without soft-start).

THE VOLTAGE AND SHARE LOOP DESIGN

A load sharing system is composed of two loops, the voltage loop and the current share loop. As in conventional designs, the voltage loop regulates the output voltage and is the faster responding loop. The current sharing loop is a lower bandwidth loop to eliminate noise pick-up on the share line, and should be low enough in bandwidth to eliminate interactions with the voltage loop.

A complete loop diagram is shown in Fig. 10. The voltage amp transfer function is designed to optimize the voltage loop response, which is determined by the modulator topology, filters, and other gain functions in the loop. We will work through each gain block for a flyback converter example using the UC3907, and from this the user should be able to expand the design to any topology.

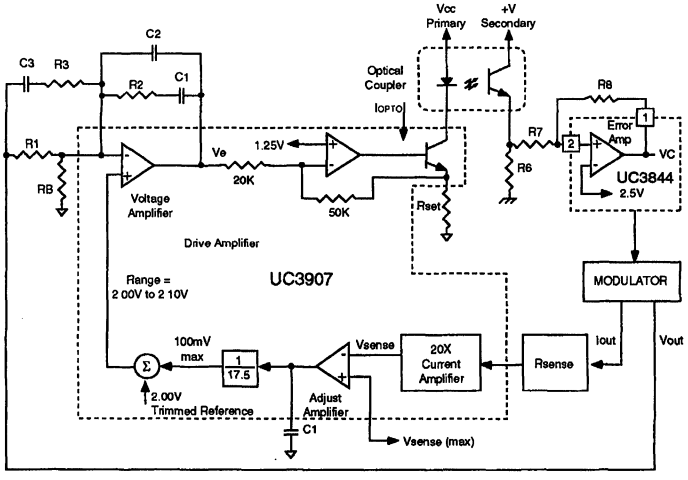

Fig. 10 - The UC3907 can be easily implemented to perform voltage control, and optical coupler drive for isolated applications.

Compensated as shown, the voltage amp response is given by:

$$UGF = \frac{1}{2\pi R_1(C_1 + C_2)} \qquad Pole = Origin$$

UGF = Unity Gain Frequency.

$$Pole\ 2 = \frac{1}{2\pi R_1 C_3} \qquad Pole\ 3 = \frac{1}{2\pi R_2\left(\frac{C_1 C_2}{C_1 + C_2}\right)}$$

$$Zero\ 1 = \frac{1}{2\pi R_2 C_1} \qquad Zero\ 2 = \frac{1}{2\pi(R_1 + R_3)C_3}$$

The drive amp will convert the output of the voltage amp to an error current to be applied to the opto coupler. The current is given by:

$$I_{opto} = \frac{(1.25 - Ve)2.5 + 1.25}{Rset}$$

where Ve = output of the voltage amp - error voltage and the small signal gain is:

$$\frac{I_{opto}}{v_e} = \frac{-2.5}{Rset}$$

The control voltage for the UC3844 pulse width modulator is given by:

$$V_c = (2.5 - I_{opto}\, CTR\, R_6)\left(\frac{R_8}{R_6 + R_7}\right) + 2.5$$

where CTR is the current transfer ratio of the opto coupler. and the small signal gain is given by:

$$\frac{v_c}{I_{opto}} = -CTR\, R_6 \left(\frac{R_8}{R_6 + R_7}\right)$$

therefore the UC3907 error voltage to PWM control voltage gain is given by:

$$\frac{v_c}{v_e} = CTR\, R_6 \left(\frac{R_8}{R_6 + R_7}\right)\left(\frac{2.5}{R_{set}}\right)$$

The CTR spread can vary from 0.4 to 2 on a given device type, but many manufacturers can sort them out to a +/- 30% tolerance. The CTR is also a function of the driving current and therefore introduces a non-linearity in the feedback gain.

The control to output gain of the modulator for various topologies is referenced in the Unitrode power supply design seminar book. For example, the control to output gain for the discontinuous flyback with current mode control is:

$$\frac{v_o}{v_c} = \sqrt{\frac{Ro\, L\, F}{2}} \frac{\left(1 + \frac{S}{wz}\right)}{\left(1 + \frac{S}{wp}\right)}$$

$$Where\ wz = \frac{1}{Rc\, C} \qquad wp = \frac{1}{Ro\, C}$$

Rc = esr of C's in parallel
Ro= Load resistance
C= Total output Capacitance
L= Primary inductance
F= Switching frequency

The total voltage loop gain is given by:

$$G(S) = A(s)\left(\frac{v_c}{v_e}\right)\left(\frac{v_o}{v_c}\right)$$

where A(s) is the voltage amp transfer function

To bandwidth limit the share loop, the adjust amplifier is compensated where the unity gain frequency of the adjust amp is given by :

$$F = \frac{gm}{2\pi C_l}$$

where typical gm = 3mS.

AN OFF-LINE LOAD SHARE APPLICATION

An off-line power supply application utilizing the UC3907 Load Share Controller is shown in Fig. 11 for a flyback regulator. The UC3844 is the modulator and its switching frequency is determined by Fs = 1.72/(Rt Ct). The resistor R5 will sense the primary inductor current, where the maximum peak current for the UC3844 is given by ISmax= 1.OV/R5. Startup is achieved with R1 and C5 until bootstrap winding W2 can feedback to power the UC3844 The snubber network D3, C4, and R2 prevents turn-off voltage spikes from exceeding the FET breakdown voltage. The primary soft-start circuit is comprised of Q1, R9 and C10.

Note that the resistor Rset and adjust compensation is connected to artificial ground (pin 6). Artificial ground is a replica of the "true" ground voltage on pin 4, negative sense, plus a 0.250V level shift. This allows a low impedance point for ground referenced elements to connect.

A master indicator lamp is included in the design so that the unit supplying the most load current and determining the output regulating voltage can be detected. There are many useful applications for this pin as in supply voltage margining or determination of a faulted supply which is supplying an excess voltage/current.

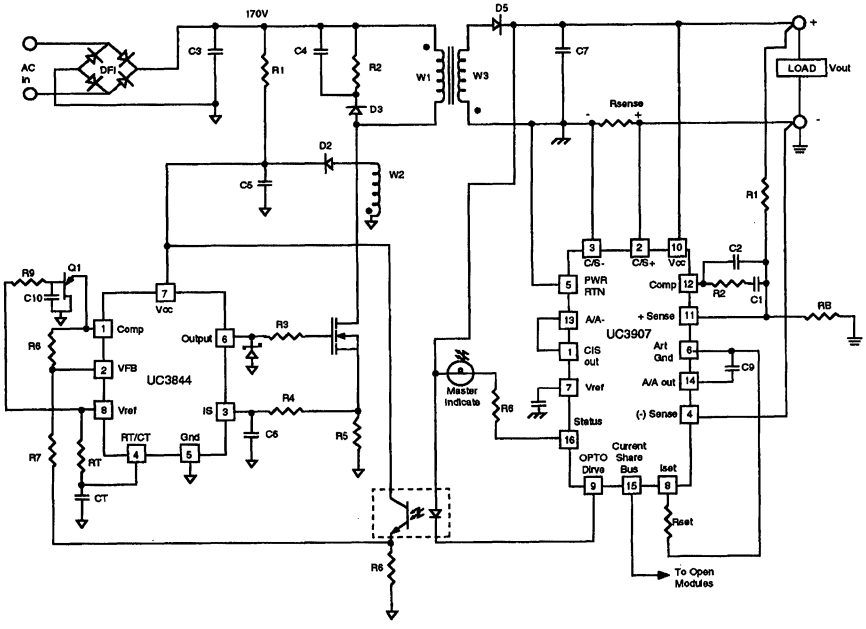

Fig. 11- The UC3907 in an off-line isolated application.

NON-ISOLATED CONVERTER APPLICATIONS

There are applications were non-isolated DC to DC converters are paralleled to make a power system. Fig. 12 shows a step down, or buck, regulator utilizing the UC3524A voltage mode PWM and the UC3907 Load share IC. For non-isolated parallel power supply applications the current sensing must be done on the high side. The reason for this is that if the sensing was performed on the low side where the power supply inputs and outputs are common, then all the current sense resistors will end up in parallel, defeating the individual sensing and load sharing. The only limitation to high side current sensing in a non-isolated application is that the current amplifier of the UC3907 has a common mode range of 0V to Vin -2V, therefore a form of level shifting or average current sensing would be required.

Since the opto-coupler is not required, an inversion has been eliminated which the driving scheme must accommodate for. The Iset voltage is a gained up inverted error voltage from the UC3907 voltage amp. The UC3524A error amp is set up as an inverter and cancels out the drive amp inversion leaving the error voltage of the UC3907 to be transposed to the UC3524A in proper phase. The iset voltage will swing from 0v to 3.8V min. Current limiting is achieved by taking the current amp output signal from the UC3907 and feeding it in to the UC3524A current limit amplifier, where the current limit is given by:

$$Icl = \frac{5\left(\frac{R_{12}}{R_{11}+R_{12}}\right)+0.2}{20\,R_{sense}}$$

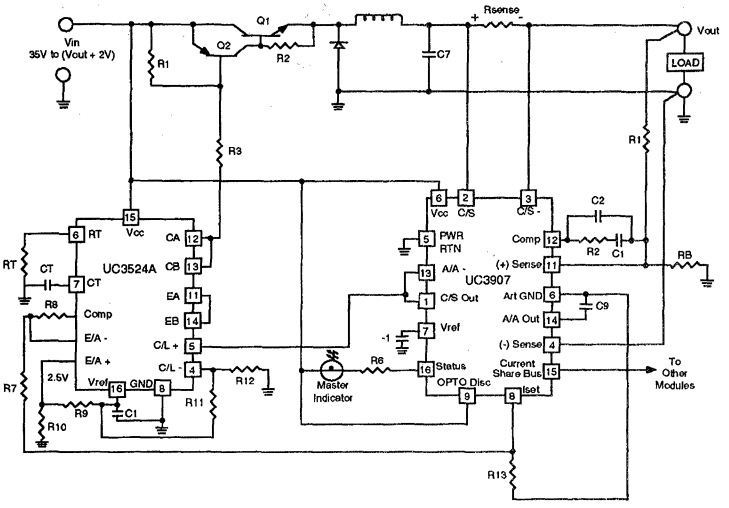

Fig. 12 - The UC3907 in a non-isolated DC to DC converter application.

LINEAR REGULATOR EXAMPLE

A simple linear regulator with load sharing using the UC3907 IC and a few external components is shown in Fig. 13. The phasing of the opto drive pin facilitates darlington drive, and supply current limiting is achieved by Q3, C1, R11, and R12 with the current limit given by:

$$Icl = \frac{VBE_{Q3}\left(1 + \frac{R_{11}}{R_{12}}\right)}{20\,R_{sense}}$$

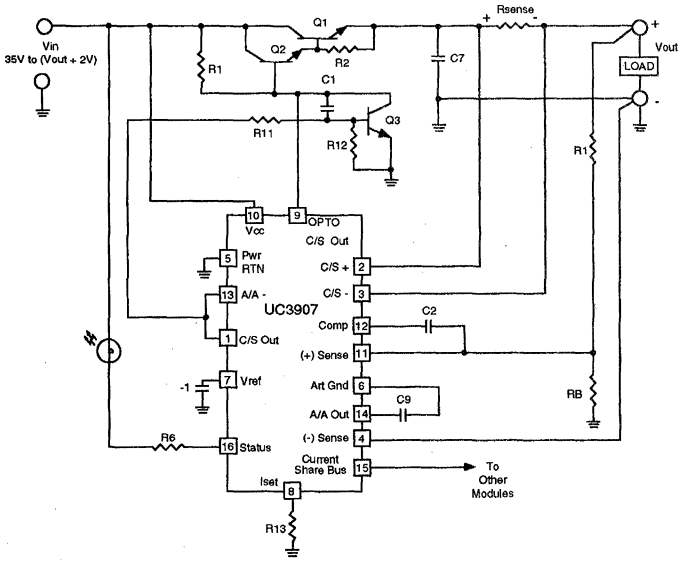

Fig. 13 - With a few external components the UC3907 can make a simple linear regulator with load sharing.

EXTERNAL LOAD SHARING

The UC3907 can be easily incorporated outside the power module to achieve load sharing, as shown in Fig 14. The load sharing loop is similar to previous examples, but instead of adjusting the internal reference of the UC3907, this technique adjusts the (+) sense line of the power module to force equal current sharing. The maximum adjust voltage is given by:

$$Vadj_{max} = 1.75\left(\frac{R_1}{R_2}\right)$$

LOAD SHARING CAN BE EXTERNALLY ADDED TO EXISTING POWER MODULES

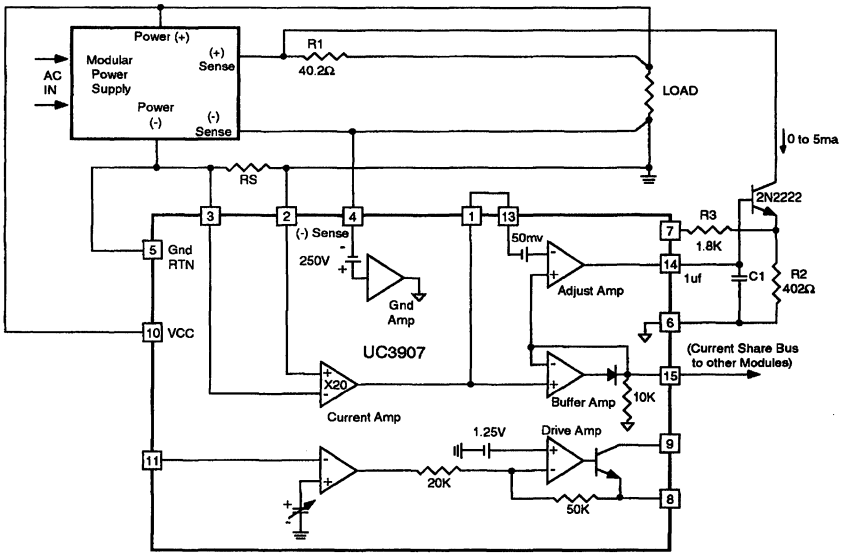

Fig. 14 - The power supplies remote sense inputs are used to facilitate load sharing.

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1. F.N. Sinnadurai "Handbook of Microelectronics Packaging and Interconnection Technologies" Electrochemical Publications Limited 1985.

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3. Bob Mammano "Isolating the Control Loop" Unitrode power Supply design seminar, SEM-700 1990.

4. Kenneth T. Small "Single Wire Current Share Paralleling of Power Supplies" US Patent 4,717,833 Jan 1988.

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Simple Circuit Modifications Enhance Optocoupler Performance

by Philip Cooke

The optocoupler is often used in pulse-width-modulated power converters to transmit an error signal across an isolation boundary. This error signal is used on the primary side to close the control loop. A phototransistor within this optocoupler has a large collector to base area in order to efficiently detect the photons of light emitted from the photodiode. This large area makes a good detector but it increases the collector to base capacitance. Larger capacitance adversely effects the bandwidth of the optocoupler by introducing a phase lag, even at low frequencies, in the small signal model of the compensation circuit. Figure 1 shows a typical optocoupler feedback scheme using a the UC3965 Precision Reference with Low Offset Error Amplifier and a Siemens Optoelectronics IL207 optocoupler. As the output voltage (V_O) drops below its nominal value, due to a sudden increase in load, the photodiode current decreases. This decrease causes the emitter voltage on the phototransistor to decrease which increases the duty cycle of the modulator. The higher duty cycle restores the output voltage to its nominal value. The type of compensation (I, PI, etc) on the UC3965 Error Amplifier is dependent on the PWM control method (i.e., voltage mode or current mode) and the power circuit topology. In all cases the bandwidth and phase of the phototransistor can effect the stability of the power supply. It is the intent of this application note to present test data on circuit configurations which show improvements in the bandwidth performance of a common optocoupler.

A test circuit, shown in Figure 2, was used to measure the gain and phase of an IL207 optocoupler along with the error amplifier of a UC3823AN PWM controller. The integrators in the compensation circuit of Figure 1 were left out and a common ground was used in all of the test circuits in order to simplify the measurements. The negative dc supply voltage (V_{NEG}) was adjusted before each test, with the V_{AC} node grounded, to get about 2 V_{DC} at the output of the error amplifier ($V_{EA,OUT}$). A Ridley Engineering, Inc. AP102A Network Analyzer (produces a swept sine wave source and has two input channels to measure the ac transfer function of a network) was used to measure the frequency response for each test circuit. During the tests an oscilloscope was used to ensure that clipping or

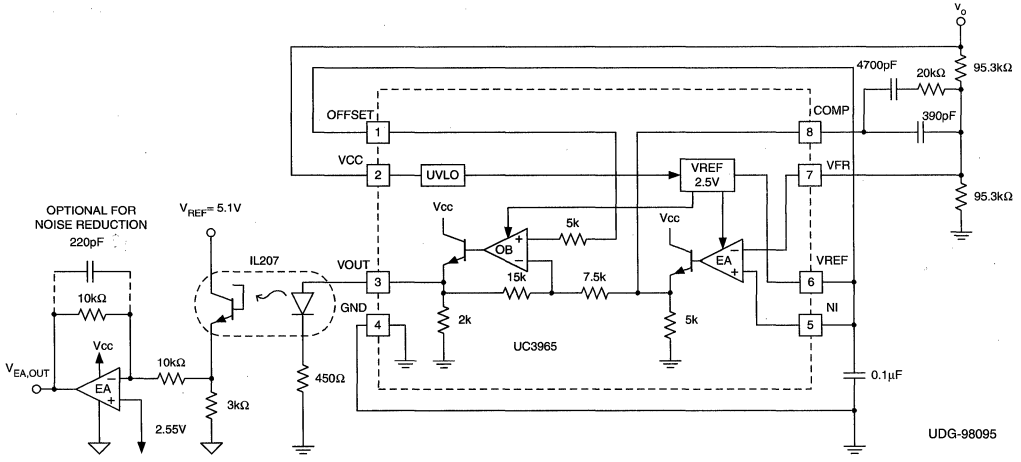

Figure 1. Typical Error Amplifier Feedback with Optocoupler

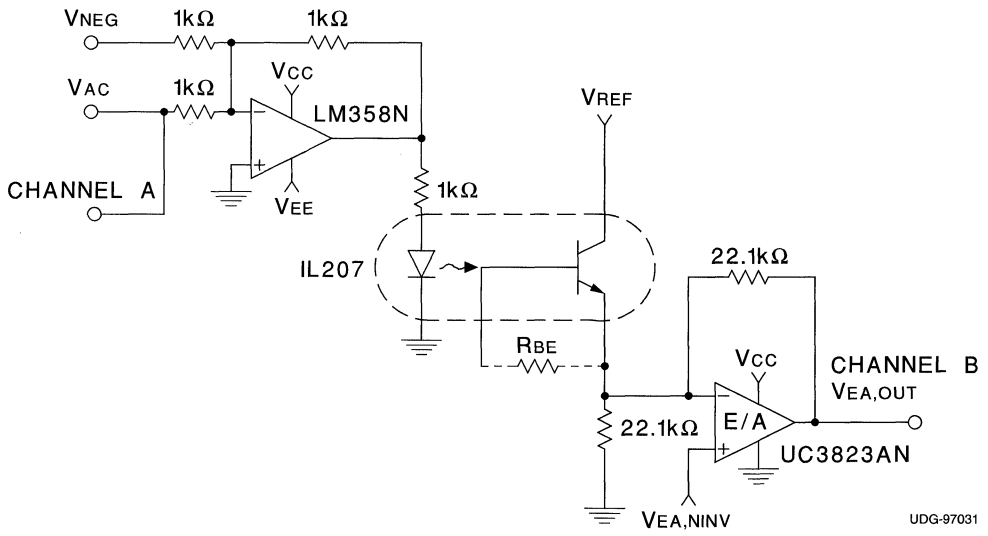

Figure 2. Data Collected for Test 1 with R_{BE} Connected, Data Collected for Test 2 with R_{BE} Not Connected

nonlinearities did not occur at the outputs of the two amplifiers. The results for test 1 are shown in Figure 3. While the noise at 20kHz was later isolated to a power supply used in the testing, its effect on the data is minimum and it was used for all the tests to maintain consistency. The gain in Figure 3 shows a –3dB frequency of about 45.9kHz and a phase of –70.1° at this point. One would expect a single pole –3dB to have a –45° phase shift, therefore this circuit is not modeled accurately by a simple RC filter. Realizing that the phase lag introduced by the optocoupler can steal away phase margin from the overall power supply control loop, it is clear that the optocoupler is phase limited with respect to bandwidth. A goal of this application note is to illustrate the importance of the phase limitations that optocouplers have in power supply feedback loops. To this end other circuit topologies will be presented to improve the effective frequency bandwidth of a given optocoupler. Note that the effective frequency bandwidth can be considered as a figure of merit for an optocoupler and should be less than the phase margin of the power supply control loop. If –15° is arbitrarily selected as this phase it is obvious that the –3dB point on the optocoupler transfer gain curve (Figure 3) will be at a higher frequency.

As mentioned above the designer should keep the control loop crossover frequency below the effective opto bandwidth to ensure enough phase margin and thus power supply stability. For the case of the data shown in Figure 3 the –15° phase point reveals an effective opto bandwidth of 8.56kHz. In contrast the –3dB point yields a much higher frequency value of 45.9kHz. The 8.56kHz frequency may be fine for some designs but others may need up to 30kHz or more of effective opto bandwidth to support a higher crossover frequency. Techniques to improve this effective bandwidth will be introduced shortly.

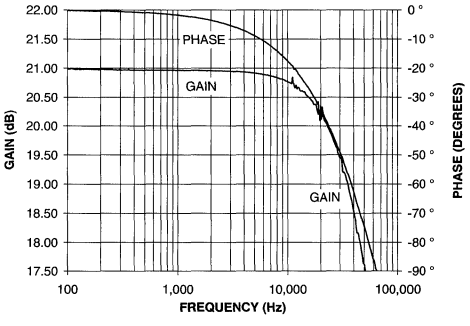

Figure 3. Gain and Phase for Figure 2 Circuit with R_{BE} Not Connected

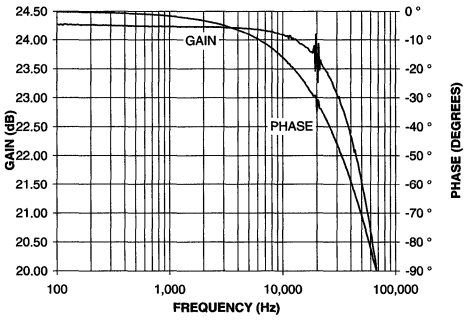

Figure 4. Gain and Phase for Figure 2 Circuit with R_{BE} = 300kΩ

By adding a 300kΩ base-to-emitter resistor in the circuit of Figure 2, test 2 results where obtained and are shown in Figure 4. The added base-to-emitter resistor is often used to reduce noise, typical in optocouplers that have the optotransistor base connection brought out to an IC pin. From the data graphed in Figure 4 it is clear that the R_{BE} resistor also increases the effective bandwidth by about 9% relative to test 1.

The circuit shown in Figure 5 was used to collect data for tests 3 and 4. Graphs of the responses are shown in Figures 6 and 7 respectively. These tests have the inverting input of the error amplifier (E/A) disconnected from the emitter terminal of the phototransistor and a resistor added between these points. The goal is to observe the effects of using the error amplifier in a topology which allows dc gain (however, unity gain was used in the test results presented here). With this configuration the effective opto bandwidth for tests 3 and 4 actually decreased from tests 1 and 2 by a factor of approximately 8, thus implying that the virtual ground at the emitter of the phototransistor was useful in increasing the bandwidth of the system. Note that for isolated power supplies the compensation gain is usually realized on the UC3965 side (secondary side). Therefore, setting up the error amplifier (on the primary side) for nearly unity gain or less is not a problem. For the final test circuit the error amplifier is used with the optotransistor to realize the widest bandwidth from the optocoupler device.

The circuit shown in Figure 8 was used for tests 5 through 9. The base of the phototransistor is connected to the feedback resistor, R_F. An increase in the effective opto bandwidth and the –3dB bandwidth is seen in this optocoupler circuit. The phototransistor has a component of base current

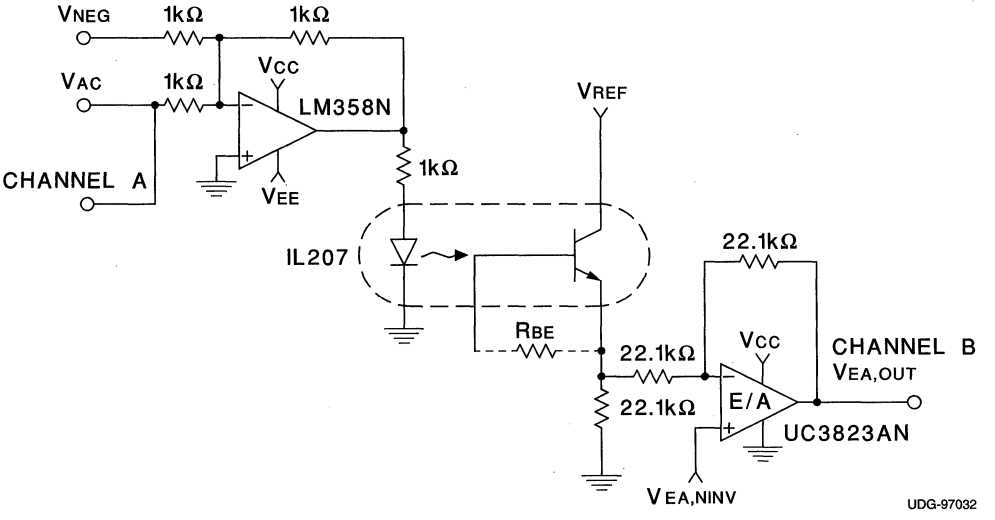

Figure 5. Data Collected for Test 3 with R_{BE} Not Connected, Data Collected for Test 4 with R_{BE} Connected

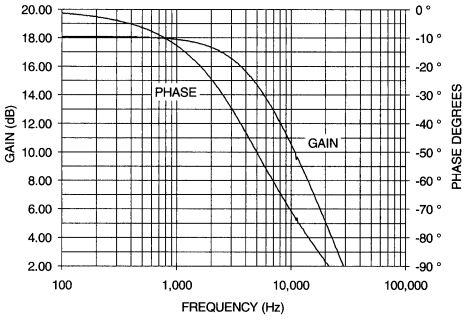

Figure 6. Gain and Phase for Figure 5 with R_{BE} = 300kΩ

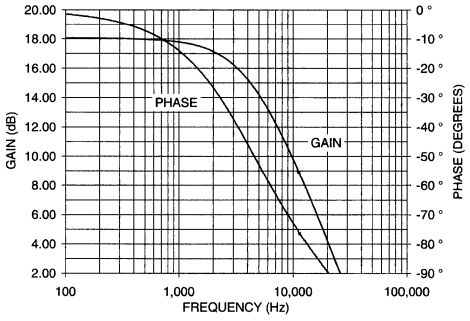

Figure 7. Gain and Phase for Figure 5 with R_{BE} Not Connected

provided by the photodiode and another component of current by the base connection to the feedback resistor. For small signal conditions the base to emitter junction is forward biased. Large signal characteristics, as would be seen under power supply start up or current limit conditions, were not investigated. In tests 5 through 9 different dc gains were achieved by varying the values of R_F and R_E, the feedback and optotransistor emitter resistors. In some cases a 3.3pF capacitor had to be put in parallel with the R_F resistor to prevent oscillation. Depending upon a given power supply design a capacitor of approximately 220pF could be used in parallel with R_F to prevent oscillations.

Test results indicate that the maximum practical overall dc gain of the error amplifier is about 7dB (Test 9). As mentioned above, the dc gain required in the compensation network for the power supply can be realized with the UC3965 so the 7dB limit does not present a system limitation.

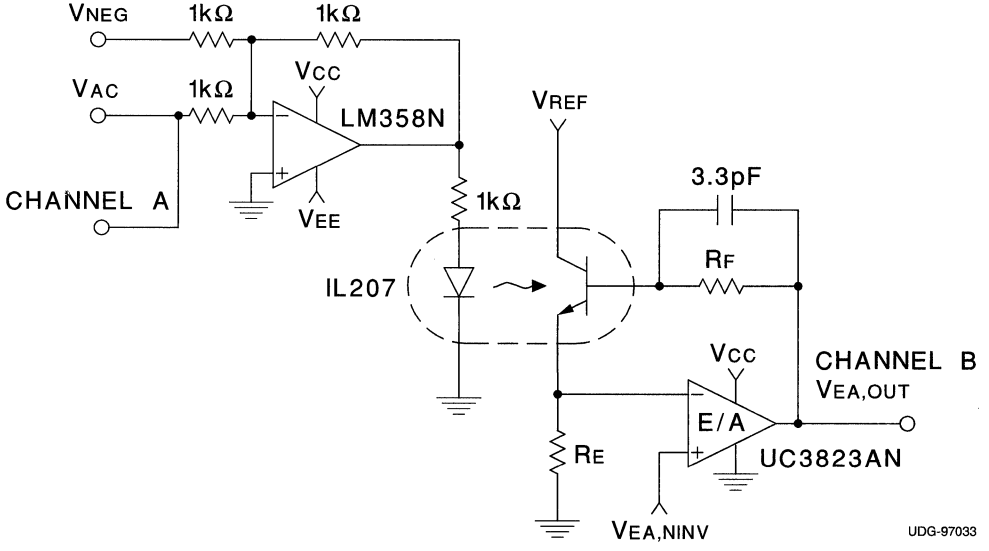

Figure 8. Circuit Used in Tests 5 through 9

(Data results shown in Figures 9 through 13)

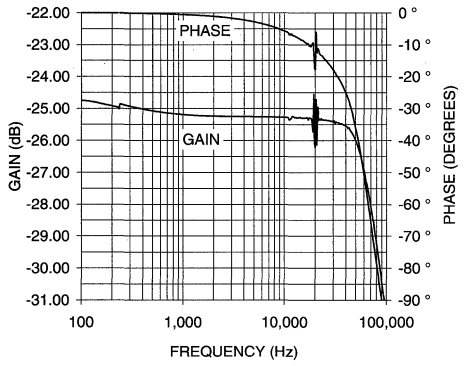

Figure 9. Gain and Phase for Figure 8, R_F = 22.1kΩ and R_E = 22.1kΩ

The maximum measured effective opto band-width of 25.5kHz was achieved for the values of R_F = 22.1kΩ and R_E = 22.1kΩ, as graphically depicted in Figure 9. This is a frequency improvement of about three to one relative to test 1 using the same opto-coupler device. All the test results are summarized in Table 1 below.

Summary

The often unknown effective opto bandwidth for a power supply design may cause stability problems. Potential variation in optocoupler parameters from manufacturer to manufacturer in addition to part-to-part variations should be of concern to the designer in terms of closing the loop. The compensation circuit reviewed in this application note can reduce the phase lag effects introduced by the optocoupler by shifting the effective opto bandwidth higher in frequency by a factor of about three. This circuit can be used to help ensure that the variations in optocoupler parameters from lot-to-lot will have less impact on the power supply closed loop performance.

References

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[2] Siemens Optoelectronics, 1995-1996 IL207A Datasheet.

[3] Krause, Bob, "*Optoelectronic Feedback Control Techniques for Linear and Switch Mode Power Supplies*", PCIM, Power Quality, 1993.

[4] Blockl, Reinhard, "*Light-Link Components Control High-Frequency Switched-Mode Power Supplies*", Siemens Appnote 41, Optoelectronics 1993 Databook.

Table I. Summary Test Data

Test No.	V_{NEG}= V_{EE} (V)	VAC (mV_{RMS})	−15° Phase Frequency (kHz)	−3dB Frequency (kHz)	R_{BE} (kΩ)	Phase at −3dB Point (deg)	"dc Gain" (dB at 100Hz)	Graph Figure No.	Circuit Figure No.	R_F (kΩ)	R_E (kΩ)
1	−1.44	49.8	8.50	45.9	NC	−70.1	21.0	3	2		
2	−2.28	49.8	9.33	53.6	300	−75.3	24.3	4	2		
3	−2.31	49.8	1.18	4.59	300	−47.3	18.1	6	5		
4	−1.49	49.8	1.07	4.14	NC	−47.0	18.1	7	5		
5	−2.31	994	25.5	64.9	NC	−58.2	−24.7	9	8	22.1*	22.1
6	−2.32	49.8	17.9	>100	NC	<−79.4	−4.39	10	8	221*	22.1
7	−4.07	198	18.5	>100	NC	<−78.3	−2.13	11	8	221*	2.25
8	−2.06	198	24.3	>100	NC	<−59.1	5.54	12	8	750	22.1
9	−1.95	198	21.0	>100	NC	<−68.1	7.56	13	8	1000	22.1

Notes:

V_{EA}, N_{INV}= 2.49V and V_{CC} = 15.0V for all tests

NC = Not Connected

** = R_F with 3.3pF in parallel*

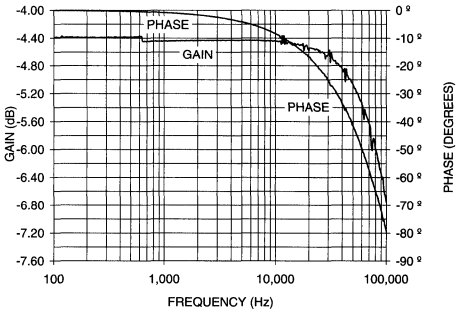

Figure 10. Gain and Phase for Figure 8, R_F = 221kΩ and RE = 22.1kΩ

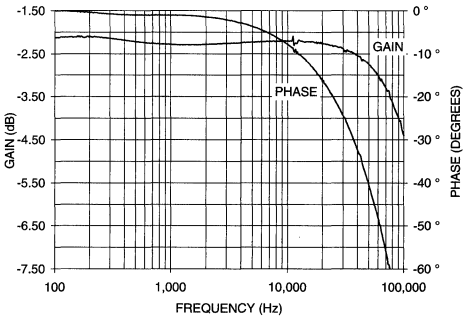

Figure 11. Gain and Phase for Figure 8, R_F = 221kΩ and R_E = 2.25kΩ

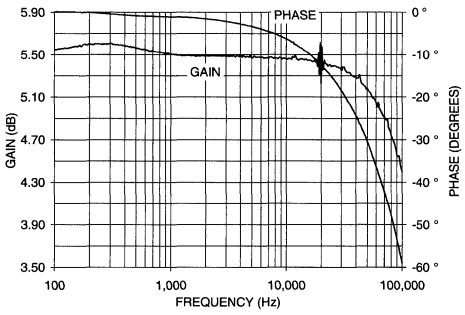

Figure 12. Gain and Phase for Figure 8, R_F = 750kΩ and R_E = 22.1kΩ

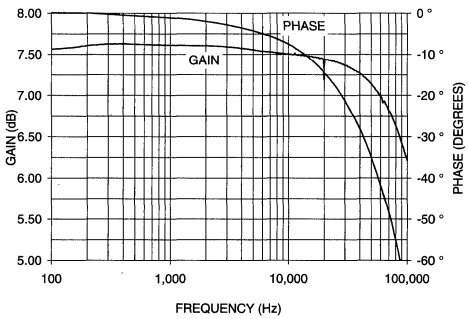

Figure 13. Gain and Phase for Figure 8, R_F = 1MΩ and R_E = 22.1kΩ

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THE UC3902 LOAD SHARE CONTROLLER AND ITS PERFORMANCE IN DISTRIBUTED POWER SYSTEMS

by Laszlo Balogh
Unitrode Corporation

UC3902 APPLICATIONS

The current demanded by large electronic systems continuously rises due to higher performance and increased functionality. At the same time, supply voltages, especially in digital circuits, are falling to previously unprecedented low levels. The combination of higher load currents and low supply voltages impose difficult requirements on the power distribution and in most cases, forces a higher voltage distribution bus with local voltage conversion.

Users of distributed power systems are seeking reliable and economic solutions to supply their loads. A modular approach, where stand alone power supplies are utilized for local power conversion, is widely accepted in these applications. The power rating of the individual converters are usually limited by the available height, board space and by the limitation on volumetric heat dissipation. High current loads are supplied by several parallel connected power supplies. In addition to higher currents, the parallel modules can also offer redundancy, an important factor to achieve reliable, uninterrupted operation and extended life expectancy in these systems.

Parallel connected power supplies require a dedicated control mechanism, called load share circuitry to assure full utilization of the system. The purpose of a load share controller, like Unitrode's UC3902, is to provide for equal distribution of the load current among the parallel connected power supplies. By equalizing the output currents, uniform thermal stress of the individual modules is also ensured which has the utmost importance for long term reliability of electronic components.

For the UC3902 to work properly, the modular power system has to consist of power supplies which possess their own feedback circuits. Furthermore, the stand alone modules have to be equipped with true remote sense capability or with an output voltage adjustment terminal. Each module must have its own load share controller. The operating principle of a load share mechanism is to measure the output current of each individual module and to be able to modify the output voltage of the units until all participating power supplies deliver equal output currents. It is accomplished by the UC3902 integrated circuits which are connected to the common load share bus and adjust the positive sense voltage (or the voltage of the output voltage adjust pin) of their respective modules to provide equal load current sharing.

UC3902 BLOCK DIAGRAM

The UC3902 is an 8-pin integrated circuit. Its sole purpose is to provide the load sharing function for existing power supplies. The chip incorporates only the building blocks required for load sharing. Tight regulation of the converters' output voltage is not anticipated with this circuit. In fact, the UC3902 performs just the opposite task by finely adjusting the regulated output voltage of the converters to match all output currents evenly.

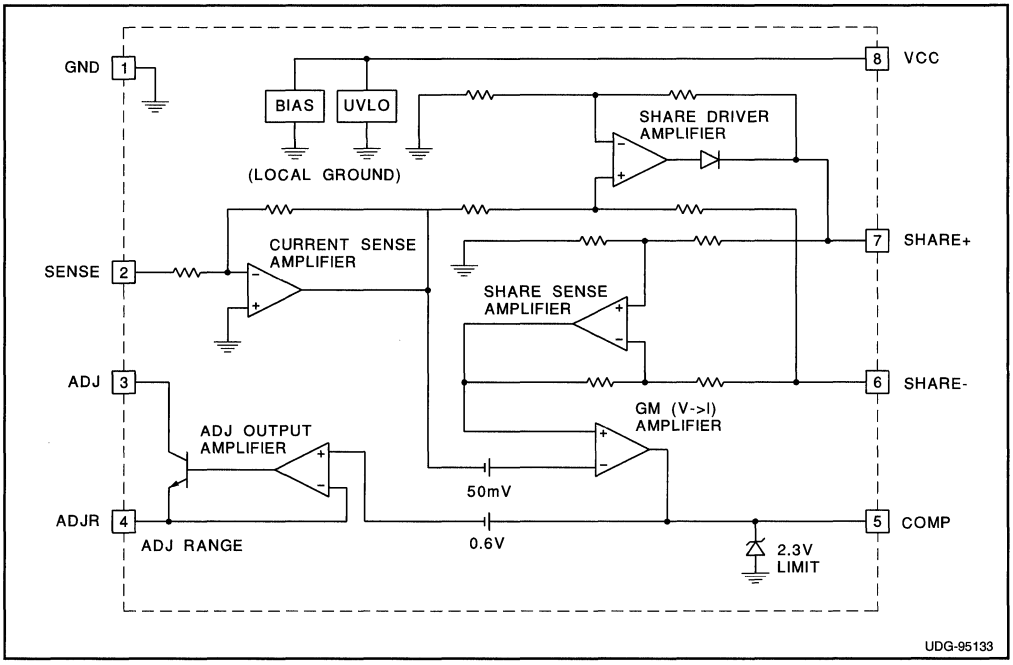

Figure 1. UC3902 Block Diagram

A unique advantage of the UC3902 is its differential load share bus. This architecture greatly enhances the noise immunity of the system. Figure 1 shows the block diagram of the load share controller.

The IC consists of a current sense amplifier, a share bus driver and sense amplifier pair, an error amplifier, a buffer stage called adjust amplifier, and housekeeping circuit which provides internal bias and the on-chip reference for the circuit.

The UC3902 has an inverting current sense amplifier with the gain of 40. The output of the current sense amplifier is proportional to the output current of the power supply it is connected to. It provides the input signals to the load share bus driver amplifier and to the inverting input of the error amplifier. Because the share driver amplifier is configured for unity gain, the voltage on the output of the share driver amplifier also equals the output voltage of the current sense amplifier. When this voltage is the highest potential among the parallel connected load share controllers, i.e. the unit delivers the highest output current, the module acts as the master unit. The output of the share driver amplifier of the master also determines the voltage on the share bus. In the case, where this voltage is lower then the share bus voltage, i.e. the module supplies less current than any one of the other units in the system, the share controller will behave as a slave. The output of the share driver amplifier of the slave controllers is disconnected from the share bus by the diodes in series with their respective outputs.

The share sense amplifier measures the voltage on the differential share bus and provides the signal for the noninverting input of the error amplifier. Similar to the share driver amplifier, this circuit has a gain of 1 which is fixed internally. Consequently, the output voltage of the share sense amplifier always corresponds to the highest output current level, delivered by the master unit in the system.

A transconductance amplifier is utilized for the error amplifier function in the UC3902. If a feedback network were connected between the output and the inverting input of the error amplifier, the output current representation would be inaccurate. The transconductance amplifier allows the feedback network to be connected from the amplifier output to the ground which preserves the authenticity of the current signal at the inverting input of the error amplifier. Also note that this type of amplifier requires a voltage difference between its inverting and noninverting inputs. Furthermore, the transconductance amplifier has high input and output impedances. Instead of the usual low impedance voltage source output of operational amplifiers, this circuit has a high impedance current source output. Accordingly, the gain is defined as transconductance (A/V) but it can be converted back to the general V/V gain term by

multiplying the transconductance of the amplifier (Gm) with the impedance of the compensation network (X_{COMP}).

The steady state output voltage of the error amplifier is the function of the voltage difference between the outputs of the current sense and the share sense amplifiers. When a particular controller works as the master in the system this voltage difference is zero. To guarantee the correct state of the error amplifier, a 50mV offset is inserted in series with the inverting input. This artificial offset will ensure zero volts at the output of the error amplifier when the unit is the master module. All slave controllers will develop a non zero error voltage at the output of the transconductance amplifier which is proportional to the difference between the output current of the respective power supply and the output current value of the master module represented on the share bus.

The output voltage of the error amplifier is used to adjust the output voltage of the power converter to balance the load current among the parallel connected modules. This is done by the adjust amplifier and its companion NPN transistor. The adjust amplifier provides signal conditioning for the error signal and its output drives a NPN transistor which is configured as a programmable current source. A resistor from its emitter to ground and the error voltage defines the current, I_{ADJ}, which flows through a resistor connected between the ADJ pin of the load-share controller and the positive output terminal. The I_{ADJ} current causes a voltage drop across the resistor which requires the power supply to increase its output voltage. The resulting higher power supply output voltage increases the output current of that particular module until the output current levels equal out among the units. At that point load sharing has been established.

UC3902 LOAD SHARE CONTROLLER DESIGN

The UC3902 load share controller requires only a few external components. Before the values of these components can be calculated, the DC/DC converter module parameters must be reviewed and some application specific limits have to be determined. There are three parameters which must be known; $V_{O,NOM}$ is the nominal output voltage of the converter, $I_{O,MAX}$ is the maximum current delivered by the unit and $\Delta V_{O,MAX}$ is the maximum adjustment range of the output voltage. The output voltage adjustment can be accomplished by using either the positive sense terminal or the adjust pin of the DC/DC converters and it is usually limited by the design of the modules. Depending on the output current level, the allocated voltage drop and the allowed power dissipation, the current sense resistor can be selected. Since the UC3902 is operational from 2.7V to 20V, in most cases the IC is powered directly from the output voltage of the system. If that is not possible because of an inappropriate value of the output voltage, the supply voltage, V_{CC}, has to be determined as well.

SETTING UP THE DC OPERATING POINT

Figure 2 shows a typical application of the UC3902 load share controller. This circuit must be repeated

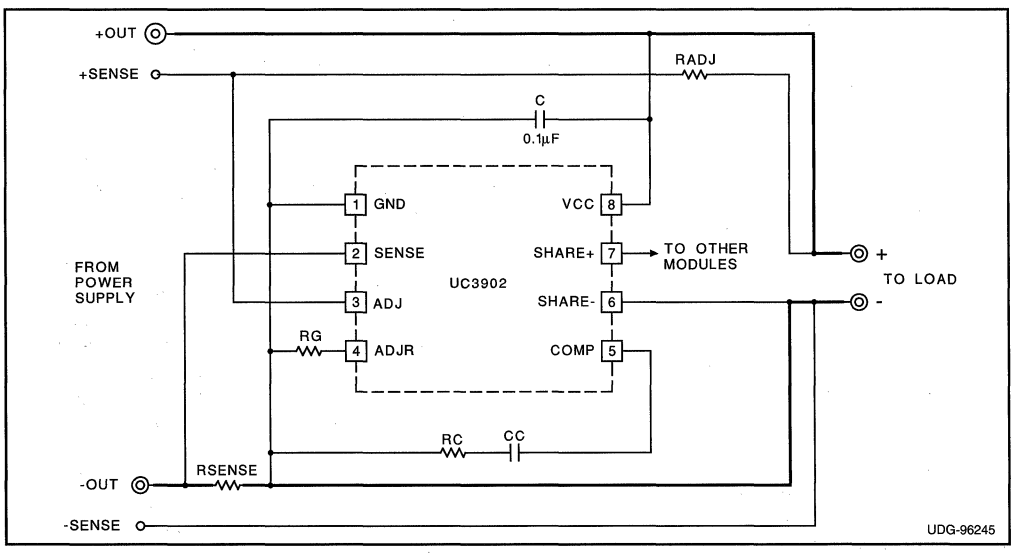

Figure 2. Typical Application

for each power supply sharing the current for a common load in the system. The design process starts with calculating the component values for setting up the basic operating conditions for the IC.

In order to precisely share the load current among parallel connected modules, the output current of each individual power supply has to be measured. A current sense resistor, R_{SENSE} is placed in the negative return path of the units. Choosing R_{SENSE} is based on two factors; the maximum power dissipation and the maximum voltage drop across the sense resistor. While the power dissipation is only limited by practical considerations like efficiency and component ratings, the maximum voltage drop has to comply with internal signal level limits of the integrated circuit. Most important is to prevent the output of the current sense amplifier from saturation. The highest voltage of the amplifier output, V_{CSAO} is a function of V_{CC}. It equals either 10V or V_{CC} - 1.5V, whichever is lower. Consequently,

$$V_{SENSE,\,MAX} = \frac{V_{CSAO}}{A_{CSA}}$$

where $V_{SENSE,MAX}$ is the maximum voltage drop across the current sense resistor, V_{CSAO} is the maximum voltage of the current sense amplifier output and A_{CSA} is 40, the gain of the current sense amplifier.

Once $V_{SENSE,MAX}$ is determined, the current sense resistor value can be calculated by the following formula:

$$R_{SENSE} = \frac{V_{SENSE,MAX}}{I_{O,MAX}}$$

$I_{ADJ,MAX}$, the maximum current of the adjust amplifier is 10mA as specified in the datasheet. It is a good practice to keep the highest current of the adjust amplifier in the 5mA to 10mA range as lower values might increase the noise sensitivity of the system. This current is determined by the highest possible voltage on the ADJR pin which is 2.6V and by the resistor, R_G, between the ADJR pin and ground. Thus the resistor value can be calculated as:

$$R_G = \frac{2.6V}{I_{ADJ,MAX}}$$

R_{ADJ} is the impedance inserted in the positive sense line of the power supply. Its value is the function of the maximum adjustment range of the output voltage, $\Delta V_{O,MAX}$ and the previously selected $I_{ADJ,MAX}$ current value. Since the voltage drop across the current sense resistor reduces the range available for output voltage adjustment, that factor has to be accounted for as shown in the equation for R_{ADJ} below:

$$R_{ADJ} = \frac{\Delta V_{O,MAX} - I_{O,MAX} \bullet R_{SENSE}}{I_{ADJ,MAX}}$$

This relationship points out an important design constraint for the system. The sum of the voltage drops across the wiring impedances and the voltage drop across the current sense resistor must be significantly lower than $\Delta V_{O,MAX}$ or the load share mechanism has no headroom to adjust the output voltage of the modules to achieve proper distribution of the load current.

CLOSING THE SHARE LOOP

Balanced distribution of the load currents among the parallel connected units is accomplished by an additional control loop provided only for the load share function. Similarly to other control loops inside the power supplies, the current share loop is based on negative feedback. Such control loops must obey certain stability criteria in order to work properly. Although this Application Note does not cover the theoretical background of loop stability, some of the most critical conditions for successfully closing the load share loop will be pointed out.

Since the load share loop is added to existing power supplies, interaction between the existing voltage control loop and the share loop must be avoided. For that reason the crossover frequencies of the two loops must be well separated.

The voltage loop crossover frequency, $f_{0,V}$ is greatly dictated by the required transient response of the converter. In order to maintain the stability of the voltage control loop, the share loop has to be set up not to cause any excess phase shift at $f_{0,V}$. This is usually achieved by placing the crossover frequency of the share loop ($f_{0,S}$) at least one, but preferably two decades lower than the crossover frequency of the voltage loop. Also a zero should be placed in the transfer function at $f_{0,S}$. This way, the effect of the share loop is minimized at the crossover frequency of the voltage loop.

Closing the load share loop at low crossover frequency is acceptable, if the purpose of load sharing is clarified. The primary concern for load sharing is to extend the life expectancy of the system and to increase reliability. It is achieved in the system by paralleling several modules and

assuring that their thermal stresses are balanced during the life of the product. Another advantage in such systems is the possibility for redundancy. These goals can be completely fulfilled by slow acting corrective measures which allow $f_{0,S}$ to be significantly lower than $f_{0,V}$.

The first step is to determine the transfer functions of the individual building blocks for the frequency range from 0.1Hz to approximately 1kHz. The unity gain crossover frequency of the load share control loop is expected to be within these frequency limits. If off-the-shelf power supplies are being used, then a network analyzer should be used to measure the transfer function. This is also a good practice to confirm actual versus calculated performance as well.

The valid transfer functions for the range of our interest are:

- $A_{PWR}(s)$: the transfer function of the power supply, measured by injecting an AC signal between V_{SENSE+} and V_{OUT+} terminals.
- $A_{Vo\rightarrow Vis}$: this gain term describes the relationship between the output voltage and the voltage across the current sense resistor. It varies with the load impedance according to

$$A_{Vo\rightarrow Vis} = \frac{R_{SENSE}}{R_{LOAD}}$$

- A_{CSA}: the gain of the current sense amplifier. This term is a constant and equals 40.
- A_{SHA}: both amplifiers driving and sensing the signal on the differential share bus are configured for unity gain. ($A_{SHA} = 1$)
- $A_{EA}(s)$: the gain of the error amplifier defined as: $A_{EA}(s) = Gm \bullet X_{COMP}(s)$ where Gm is the transconductance of the error amplifier and $X_{COMP}(s)$ is the impedance of the compensation components as a function of complex frequency.
- A_{ADJ}: the adjust circuit gain depends only on the R_G and R_{ADJ} resistors because the adjust amplifier is configured as a unity gain buffer stage. Consequently,

$$A_{ADJ} = \frac{R_{ADJ}}{R_G}$$

The overall share loop characteristic is established by multiplying the gain terms of the individual blocks:

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \bullet A_{VO\rightarrow VIS} \bullet$$
$$\bullet A_{CS} \bullet A_{SHA} \bullet A_{EA}(s) \bullet A_{ADJ}$$

DESIGN EXAMPLE

Users experimenting with the UC3902 load share controller can utilize a demonstration board featured in Figure 3. This circuit provides a solution for paralleling three power supply modules. The performance of the system was measured using three off-the-shelf DC/DC converter modules, each rated for 100W delivering 8.4A to the load at 12V nominal output voltage.

The design process starts by measuring the transfer function of the power supplies between their positive voltage sense and power output terminals. The resulting Bode plot shown in Figure 4 reveals a 40Hz crossover frequency which will require a crossover frequency of 4Hz for the load share loop. The power stage has 10dB gain at this frequency.

In the demonstration board, the UC3902 is powered from the output voltage of the system. Note the 0.1µF local bypass capacitor connected to the VCC pin of the IC. Using 12V as VCC, the maximum output voltage of the internal amplifiers are approximately 10V. This voltage denotes the highest possible full scale voltage between SHARE+ and SHARE-, but the actual voltage on the load share bus at full load is determined by the designer. Noise sensitivity, accuracy and the number of units in parallel have to be taken into consideration when choosing the full scale bus voltage. The load share bus is driven by the master controller only and each slave module represents a 10kΩ load on the bus. This means that every unit will increase the supply current of the master module by 100µA/V on the load share bus.

The power supply's 8.4A output current rating allows the use of a higher shunt resistor value in favor of better load share accuracy with only a slight decrease in overall efficiency. The full scale bus voltage, V_{CSAO} is selected to be 6V. Accordingly,

$$R_{SENSE} = \frac{6V}{8.4A \bullet 40} = 0.0178\Omega$$

and a 20mΩ standard value had been selected.

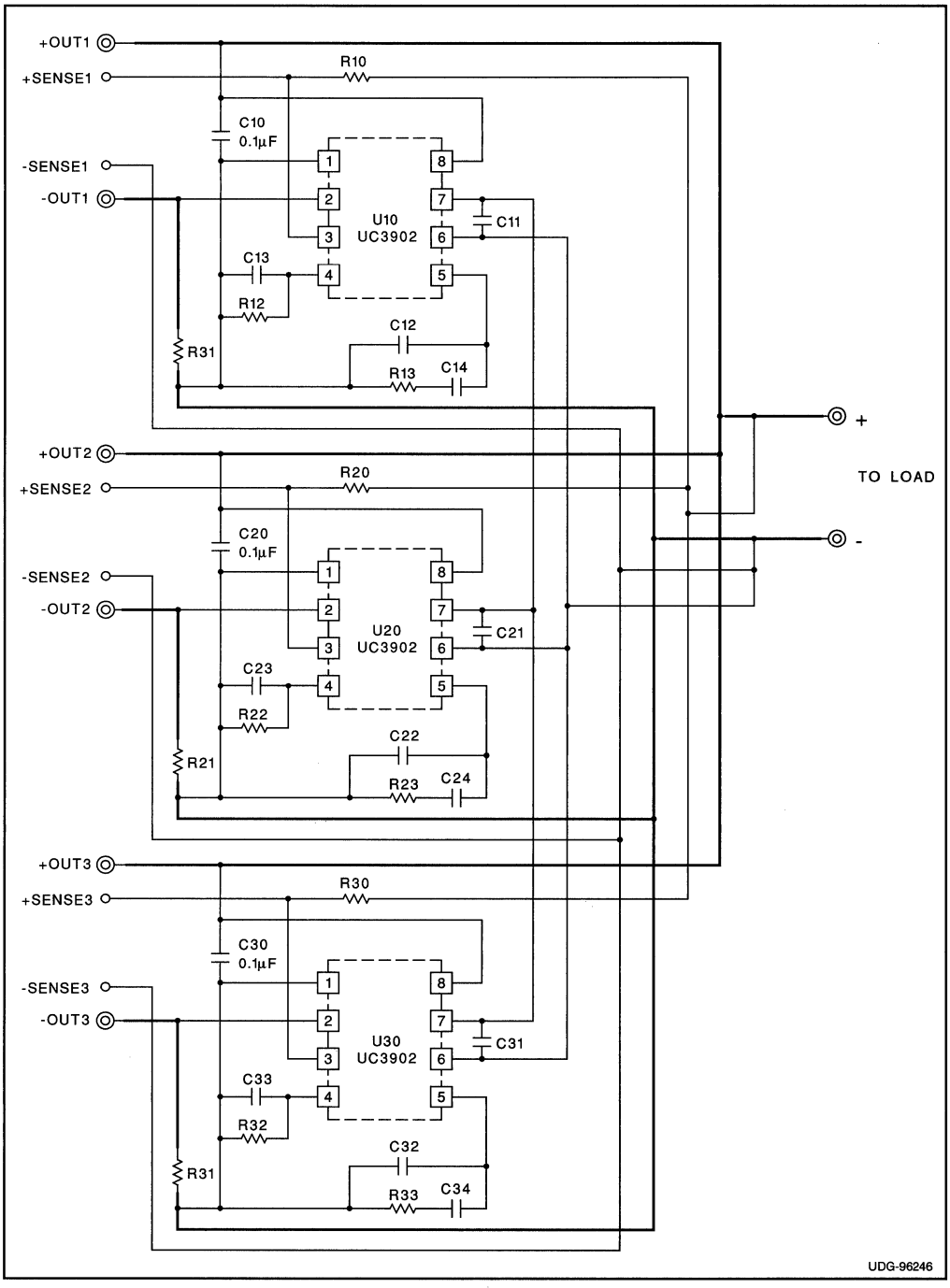

Figure 3. Demonstration Board Schematic

The R_G resistor value depends on the current flowing through the NPN buffer transistor of the adjust amplifier and in the R_{ADJ} resistor placed in the positive sense line of the converter. This current is selected by the designer but its value shall be smaller than 10mA according to the datasheet. For this application 5mA is chosen. Smaller values tend to increase the noise sensitivity of the solution while larger current values represent unnecessary power dissipation for the IC. Although this current does not show up in the I_{CC} current requirements, the power dissipation of the buffer transistor can be a significant part of the total power loss inside the integrated circuit. For instance, in this application, the voltage across the collector emitter terminals equals V_{CC} - 2.6V, approximately 10V. The power dissipated in this part of the circuit is 10V • 5mA= = 50mW. Once the maximum current for this part of the circuit is selected the value of R_G can be calculated as:

$$RG = \frac{2.6V}{5mA} = 520\Omega$$

The nearest standard value of 510Ω is used.

The R_{ADJ} resistor value is defined by the maximum adjustment range of the output voltage, the highest load current, the current sense resistor value and I_{ADJ} value. In this application, $\Delta V_{O,MAX}$ is 0.6V while the other parameters have been previously calculated. Thus,

$$R_{ADJ} = \frac{0.6V - 8.4A \bullet 20m\Omega}{5mA} = 86.4\Omega$$

Instead, an 82Ω standard value is chosen.

At this point, the steady state operating conditions of the system are defined. The compensation components C_C and R_C can be calculated from the loop gain equation.

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet$$

$$A_{CSA} \bullet Gm \bullet \left(\frac{1}{C_C \bullet s} + R_C\right) \bullet \frac{R_{ADJ}}{R_G}$$

Substituting the power stage gain of 10 at the load share loop crossover frequency and solving the equation for C_C, the compensation capacitor value can be calculated as:

$$C_C = A_{PWR}(s) \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet A_{CSA} \bullet$$

$$Gm \bullet \frac{1}{\pi \bullet f_{O,S}} \bullet \frac{R_{ADJ}}{R_G}$$

which gives

$$C_C = 10 \bullet \frac{20m\Omega}{1.43\Omega} \bullet 40 \bullet 4.5mS \bullet$$

$$\frac{1}{\pi \bullet 4Hz} \bullet \frac{82\Omega}{510\Omega} = 322\mu F$$

A 330µF capacitor is used. Note that the reason for the large capacitor value is the extremely low crossover frequency dictated by the transfer function characteristic of the DC/DC converter.

The value of R_C is determined by the selected crossover frequency and compensation capacitor value according to:

$$R_C = \frac{1}{2 \bullet \pi \bullet f_{O,S} \bullet C_C}$$

Using the previously calculated capacitor value results in a R_C value of 270Ω.

The resulting Bode plot of the load share control loop is displayed in Figure 4. The phase margin of the loop can be increased by separating the two crossover frequencies, $f_{0,V}$ and $f_{0,S}$ even further. In this particular design, moving $f_{0,S}$ to a lower frequency would have resulted in a very large capacitor value, thus this idea was not considered.

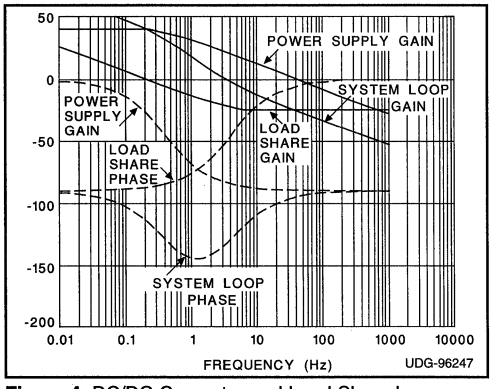

Figure 4. DC/DC Converter and Load Share Loop Bode Plots

PARTS LIST:

C = C10 = C20 = C30 = 0.1µF
C11 = C21 = C31 = 0.01µF
C12 = C22 = C32 = not used
C13 = C23 = C33 = not used
C_C = C14 = C24 = C34 = 330µF
R_{ADJ} = R10 = R20 = R30 = 82Ω
R_{SENSE} = R11 = R21 = R31 = 0.02Ω
R_G = R12 = R22 = R32 = 510Ω
R_C = R13 = R23 = R33 = 270Ω

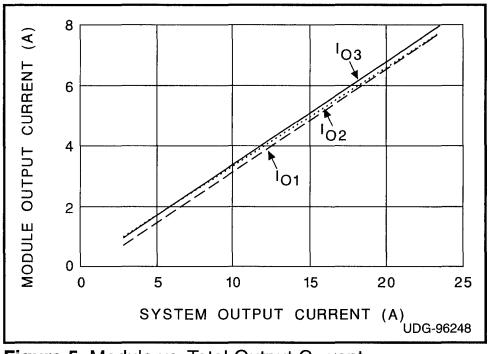

Figure 5. Module vs. Total Output Current

EXPERIMENTAL RESULTS

The performance of the demonstration circuit was measured using the calculated component values and running three DC/DC converters in parallel. Figure 5 shows the output currents of the individual modules as a function of the total load current.

In Figure 6, the percentage of deviation from the calculated average module current is depicted. The

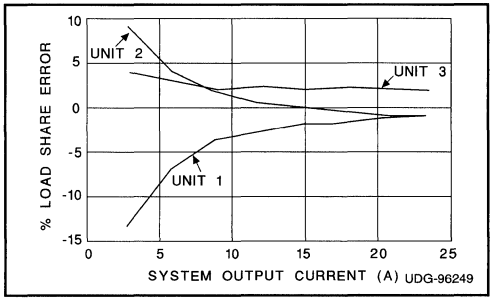

Figure 6. Load Share Accuracy

current distribution error is the largest at light load, as expected, because of the effects of internal offset voltages and the small current measurement signal level. At full load, where load sharing has the most impact, the three modules shared the load current evenly, within 1% of the ideal load current values.

Results similar to this can be obtained in other applications with the formulas contained within this Application Note.

REFERENCES

[1] *"UC3902 Load Share Controller"*, Datasheet, Unitrode Corporation

[2] M. Jordan, *"UC3907 Load Share IC Simplifies Parallel Power Supply Design"*, U-129 Application Note, Unitrode Corporation

[3] J. Rajagopalan, et al, *"Modeling and Dynamic Analysis of Paralleled DC/DC Converters with Master-Slave Current Sharing Control"*, APEC '96 Proceedings, pp. 678-684

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. 603-424-2410 • FAX 603-424-3460

8 Motion Control

Motion Control

Brushless Motor Products	UNITRODE PART NUMBER				
	UC3625	UCC3626+			
Hall Logic	Y	Y			
Tachometer	Y	Y			
Output Current per Output	0.1A	0.01A			
Operating Voltage	10V - 18V	11V - 15V			
Differential Current Sense Amplifier	Y	Y			
Current Limit	Y				
Application / Design Note	DN-50, U-115, U-120, U-130	U-120			
Pin Count❖	28	28			
Page Number	PS/8-37	PS/8-50			

DC Motor Controllers	UNITRODE PART NUMBER				
	UC3637	UC3638			
Output Clamp Diodes					
Output Current per Output	0.1A	0.1A / 0.05A			
Operating Voltage	5V - 36V	10V - 36V			
Differential Current Sense Amplifier		Y			
Thermal Shutdown					
Current Limit	Y	Y			
Application / Design Note	DN-53A, U-102, U-112, U-120	DN-76, U-120			
Pin Count❖	18, 20	20			
Page Number	PS/8-78	PS/8-84			

❖The smallest available pin count for thru-hole and surface mount packages.
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Motion Control (cont.)

Linear Power Amplifier Products	UNITRODE PART NUMBER				
	UC3173A	UC3175B	UC3176	UC3177	UC3178
Output Clamp Diodes	Y	Y	Y	Y	Y
Output Current per Output	0.55A	0.8A	2A	2A	0.45A
Operating Voltage	4V - 15V	4V - 15V	3V - 35V	3V - 35V	3V - 15V
Differential Current Sense Amplifier	Y	Y	Y	Y	Y
Thermal Shutdown	Y	Y	Y	Y	Y
Current Limit	Y	Y	Y	Y	Y
Four Quadrant	Y	Y	Y	Y	Y
Number of Outputs	2	2	2	2	2
BW	2MHz	2MHz	1MHz	1MHz	2MHz
Special Features			B+ Input Pin	Supply OK Pin	
Pin Count❖	24	24	28	28	28
Page Number	PS/8-5	PS/8-16	PS/8-21	PS/8-21	PS/8-25

Phase Locked Frequency Controllers	UNITRODE PART NUMBER				
	UC3633	UC3634	UC3635		
Internal Oscillator	Y	Y	Y		
Divider Output Provided			Y		
External Phase Detector Inputs			Y		
2 Phase Drive Logic		Y	Y		
Divide Logic Select	4/5 & 2/4/8	2/4/8	2/4		
Operating Voltage	8V - 15V	8V - 15V	8V - 15V		
Maximum Frequency	10MHz	10MHz	10MHz		
Application / Design Note	U-113	U-113	U-113		
Pin Count❖	16, 20	16, 20	16		
Page Number	PS/8-63	PS/8-70	PS/8-74		

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Motion Control (cont.)

Stepper Motor Controllers	UNITRODE PART NUMBER				
	UC3517	UC3717	UC3717A	UC3770A	UC3770B
Output Clamp Diodes		Y	Y	Lower	Lower
Output Current per Output	0.35A	0.8A	1A	1.3A	1.3A
Operating Voltage	10V - 40V	10V - 45V	10V - 46V	10V - 50V	10V - 50V
Differential Current Sense Amplifier					
Thermal Shutdown		Y	Y	Y	Y
Current Limit		Y	Y	Y	Y
Current Sense Thresholds					Tailored for half stepping applications
Application / Design Note		U-99	U-99		
Pin Count❖	16	16, 20	16, 20	16, 28	16, 28
Page Number	PS/8-30	PS/8-92	PS/8-100	PS/8-108	PS/8-108

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UNITRODE

Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- ± 500mA Load Current
- 1.3V Typical Total V_{SAT} at 550mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Bandwidth Control
- Inhibit Input and UVLO
- 5V or 12V Operation
- 12mA Quiescent Supply Current
- PLCC, SOIC, and Low Profile Quad Flat Pack Packages

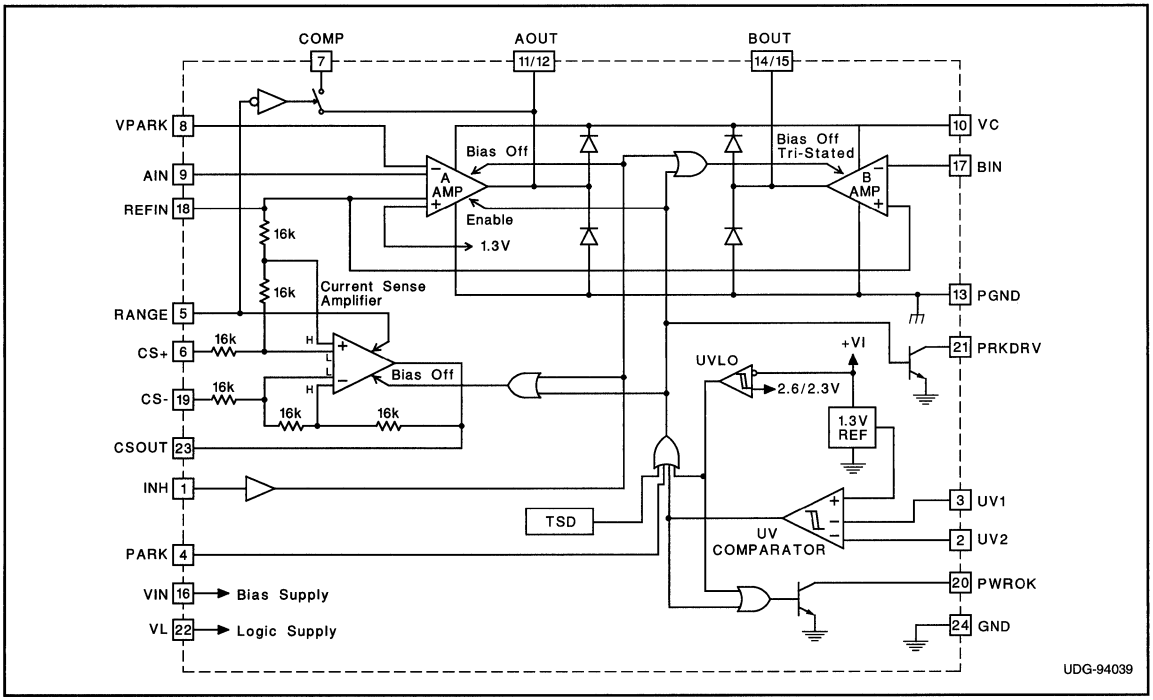
DESCRIPTION

This full bridge power amplifier, rated for continuous output current of 0.55A, is intended for use in demanding servo applications such as head positioning for high density disk drives. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3173A is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a dual input undervoltage comparator, which can monitor two independent supply voltages and activate the built in head park function when either is below minimum. The park circuitry allows a programmable retract voltage to be applied to the load for limiting maximum head velocity. A separate low side parking drive pin permits a series impedance to be inserted to control maximum retract current. The parking drive function can be configured to operate with supply voltages as low as 1.2V.

The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

BLOCK DIAGRAM



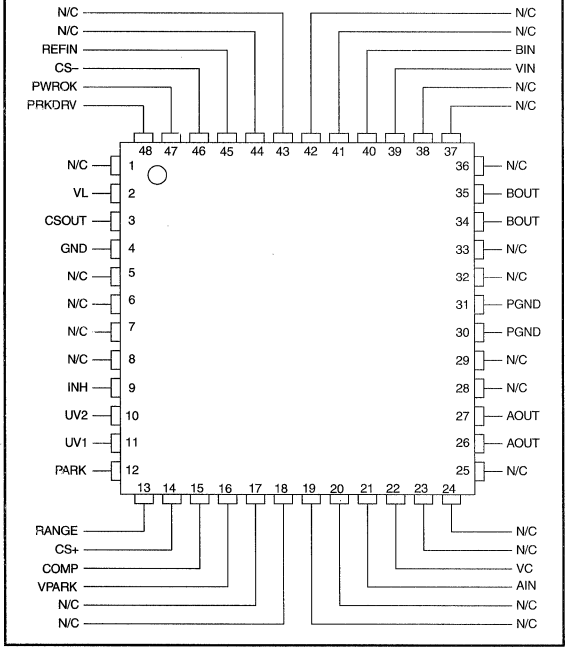
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage, (VIN, VC, VL) 20V
UV Comparator
  Maximum Forced Voltage . . . . . –0.3V to 10V
  Maximum Forced Current . . . . . ± 10mA
B Amplifier Inverting Input . . . . . –0.3V to VIN + 1.0
A Amplifier Inverting Inputs,
  (Aux. and Normal) . . . . . –0.3V to VC + 1.0V
Open Collector Output Voltages 20V
A and B Output Currents (Continuous)
  Source . . . . . Internally Limited
  Sink 0.6A
Parking Drive Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (Pulsed) 0.6A
Power OK Output Current (Continuous) 30mA
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature . . . . . +300°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.

CONNECTION DIAGRAMS

TQFP-48 (Top View)
FQ Package



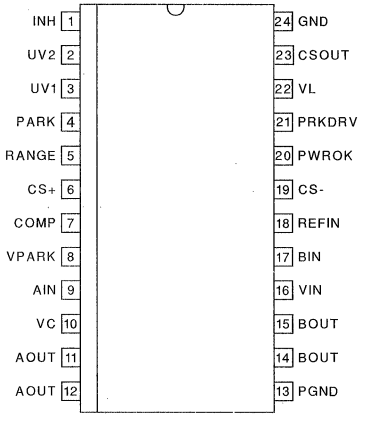
THERMAL DATA

DW Package:
  Thermal Resistance Junction to Leads, θjl . . . . . 35°C/W
  Thermal Resistance Junction to Ambient, θja . . . . 60-70°C/W
FQ Package:
  Thermal Resistance Junction to Leads, θjl . . . . . 60°C/W
  Thermal Resistance Junction to Ambient, θja . . 110-120°C/W
QP Package:
  Thermal Resistance Junction to Leads, θjl . . . . . 15°C/W
  Thermal Resistance Junction to Ambient, θja . . . . 30-40°C/W

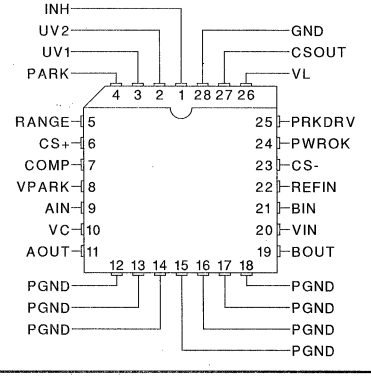
Note 2: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guide lines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

Note 3: Consult Packaging Section of Unitrode Integrated Circuits databook for thermal specifications and limitations of packages.

SOIC-24 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
VIN Supply Current			10	13	mA
VC Supply Current	I_{OUT} = 0A		1.2	2.0	mA
VL Supply Current			0.65	1.0	mA
Total Supply Current	Supplies = 5V, I_{OUT} = 0A		12	16	mA
	Supplies = 12V, I_{OUT} = 0A		13	18	mA
VL UVLO Threshold	Low to High		2.6	2.8	V
UVLO Threshold Hysteresis			300		mV
Under Voltage (UV) Comparator					
Input Bias Current	Max at Either UV Input		–0.25	–1.0	µA
UV Thresholds	Low to High, Other Input = 5V	1.28	1.3	1.32	V
UV Threshold Hysteresis		19	24	29	mV
PWROK Vsat	I_{OUT} = 5mA, UV Input Low		0.15	0.45	V
PWROK Leakage	V_{OUT} = 20V			5	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 2.5V			4	mV
	B Amplifier, V_{CM} = 2.5V			12	mV
Input Bias Current	V_{CM} = 2.5V, Inverting Inputs Only		–150	–500	nA
Input Bias Current at Ref. Input	(REFIN – CS+)/48kΩ, T_J = 25°C	15	21	27	µA/V
CMRR	V_{CM} = 1V to 10V, Supplies = 12V	70	90		dB
PSRR	VIN = 4V to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA to V_{OUT} = 11V, I_{OUT} = –300mA	3.0	15.0		V/mV
Gain Bandwidth Product	A Amplifier (Note 4)		2.0		MHz
	B Amplifier (Note 4)		1.0		MHz
Slew Rate	(Note 4)		1.0		V/µs
High-Side Current Limit	Low Range Mode	0.6	0.8		A
	High Range Mode	1.1	1.6		A
Output Saturation Voltage	High-Side, I_{OUT} = –100mA (Note 5)		0.7		V
	High-Side, I_{OUT} = –300mA (Note 5)		0.8		V
	High-Side, I_{OUT} = –550mA (Note 5)		0.95		V
	Low-Side, I_{OUT} = 100mA		0.2		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 550mA		0.35		V
	Total V_{SAT}, I_{OUT} = 100mA		0.9	1.2	V
	Total V_{SAT}, I_{OUT} = 300mA		1.05	1.4	V
	Total V_{SAT}, I_{OUT} = 550mA		1.3	1.7	V
VC to VIN Headroom	Volts below VIN, delta High-Side, V_{SAT} = 100mV, I_{OUT} = –550mA (Note 5)	0.23	0.4		V
High-Side Diode, V_F	I_D = 550mA		1.0		V
Low-Side Diode, V_F	I_D = 550mA, INH Activated, B Amplifer Only		1.0		V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0 to +70°C, VIN = 5V, VC = VIN = VL, REFIN = VIN/2, RANGE, PARK, and INH = 0V, and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 2.5V, Low range mode			2.0	mV
	V_{CM} = 2.5V, High range mode			4.0	mV
Input Offset Change with Common Mode Input	V_{CM} = –1V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
	V_{CM} = –1V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to –1.0V, V_{CM} = 2.5V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = –1mA, Referenced to VIN		0.1	0.3	V
Parking Function					
Park Input Threshold Voltage		0.6	1.1	1.7	V
Park Input Threshold Current	Internal Pull-Up, VIN = 0.6V		50	75	µA
Park Drive Saturation Voltage	I_{OUT} = 50mA		0.15	0.35	V
Park Drive Leakage	V_{OUT} = 20V			50	µA
Regulating Voltage at Park Volts Input		1.275	1.30	1.325	V
Amplifier A Auxiliary Input Bias Current			–300	–750	nA
Amplifier A Parking High-Side Saturation Voltage	I_{OUT} = –50mA, VIN = 0V, VC = VL = 5V, PARK Open, VC to V_{OUT}		0.8	0.95	V
Minimum Parking Supply	At VC and VL, VIN = 0V, A Amplifier Out - V_{SAT} PRKDRV > 0.5V, I_{PARK} = 50mA		1.4	1.7	V
Minimum Supply for Parking Drive and Power OK Operation	At VL, VC = VIN = 0V, V_{SAT} < 0.5V, I_{OUT} PRKDRV = 50mA, RI = 30Ω to 2V		1.1	1.4	V
	I_{OUT} PWROK = 5mA, RI = 300Ω to 2V		1.2	1.6	V
VL Parking Supply Current	PARK Open, VL = 5V, VC = 1.6V, VIN = 0V, PWROK I_{OUT} = 5mA, PRKDRV I_{OUT} = 50mA		1.6	3.0	mA
Auxiliary Functions					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	INH = 1.7V		–0.5	–1.0	µA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	RANGE = 1.7V		50	100	µA
Comp Adjust Pin Saturation Voltage	RANGE = 0V, Pin Current = ±500µA, Referenced to A_{OUT}		0.02	0.1	V
Comp Adjust Leakage Current	RANGE = 1.7V, Supplies = 12V, A_{OUT} - V_{COMP} = ±6V			5	µA
Total Supply Current when Inhibited	VIN, VC, and VL currents		1.0	1.5	mA
Thermal Shutdown Temperature	(Note 4)		165		°C

Note 4: Guaranteed by design. Not 100% tested in production.
Note 5: The high-side saturation performance of the UC3173A is referenced to the VIN supply pin. The VC supply pin can operate about 400mV below the VIN supply input without affecting the performance.

PIN DESCRIPTIONS

AIN: Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

AOUT: Output for the A power amplifier, providing one end of the differential drive to the load during normal operation and during park. During a UVLO condition at the VIN supply pin, this output is forced to a high, source only state. When the UC3173A is inhibited, this output will be set high, in a source only state.

BIN: Inverting input to the B amplifier. Used to program the gain of the B amplifier to guarantee maximum voltage swing to the load.

BOUT: Output for the B power amplifier, providing one end of the differential drive to the load during normal operation. During park and while inhibited this pin is tristated.

COMP: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

CS–: The inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than: REFIN / 2 –0.3V, in low range mode, and 2 • REFIN –0.9V, in high range mode.

CS+: The noninverting input to the current sense amplifier is typically tied to the connection between the A amplifier output and the current sense resistor connected in series with the load.

CSOUT: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, UV comparator, and other low level circuitry.

INH: A high impedence logic input that disables the A and B power amplifiers, as well as the Current Sense amplifier. The UV comparators and logic functions of the UC3173A remain active. This input has an internal pull-up that will inhibit the device if the input is left open. The Inhibit function is overridden by any condition that forces the Park function to be activated.

PARK: Input that forces the park condition on the UC3173A. This input has an internal pull-up that will force the park condition if the pin is left open.

PGND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

PRKDRV: A 100mA drive output that is active low during a park operation. This pin is normally used to supply the lowside drive to the load during parking, in place of the B amplifier. A series resistor can be added between this pin and the load to limit current during park.

PWROK: Indicates with an active low condition that either of the UV inputs are low, or that the supply voltage at the VL input to the UC3173A has dropped below the UVLO threshold. This output will remain active low until the VL supply has dropped to below approximately 1.2V.

RANGE: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REFIN: Reference for input control signals to the power amplifier, as well as, the noninverting inputs to the A and B amplifiers, and the output level shift for the CS amplifier.

VC: High current supply to the collectors of the high side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are activated. This pin can operate approximately 400mV below the VIN supply without affecting the voltage available to the load. This supply pin provides drive to the power amplifiers during a parking operation.

VIN: Provides bias supply to both the power amplifiers and the current sense amplifiers. The high-side drive to the power stages on both the A and B amplifiers is referenced to this pin. The high side saturation voltages are specified and measured with respect to this supply pin. The parking function of the device is fully operational independent of the voltage at this pin.

PIN DESCRIPTIONS (cont.)

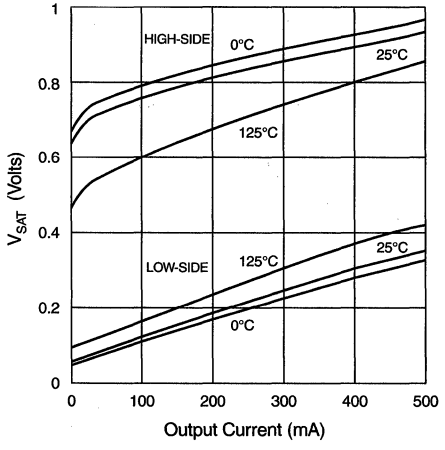
VL: Logic portions of the UC3173A are powered by this supply pin, including the reference, UVLO, the UV comparators, and the PRKDRV and PWROK outputs. This pin is a low current supply that would normally be tied to the VC pin, or to a parking hold up capacitor for extended parking operation with very low recovered back emf.

VPARK: The auxiliary inverting input to the A amplifier, activated during park conditions on the UC3173A. An internal auxiliary non-inverting input is connected to the 1.3V reference. When the auxiliary inputs are activated, the A amplifier will force a programmed voltage at its output for a maximum back-emf/velocity retract of the head. The park condition on the UC3173A is always activated by any one of the following four conditions, 1: a low condition on either of the UV inputs, 2: a high input level at the Park input, 3: a UVLO condition at the VL supply pin, and 4: activation of the TSD, (thermal shutdown) protection circuit. During a UVLO condition at the VL pin the auxiliary inputs to the A amplifier are over-ridden, and the A amplifier output is forced to its high state.

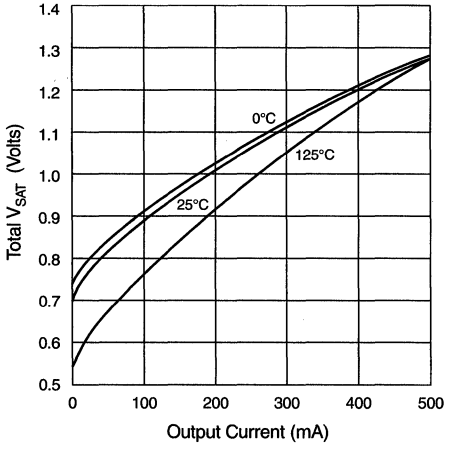
UV1 & 2: Inputs to the UV comparator, these inputs are high impedance sensing points used to monitor external supply conditions. Either of the inputs going low will force the device into a park condition, and force the PWROK output to an active low state. If either of these inputs is not used it should be connected to a voltage

APPLICATION INFORMATION

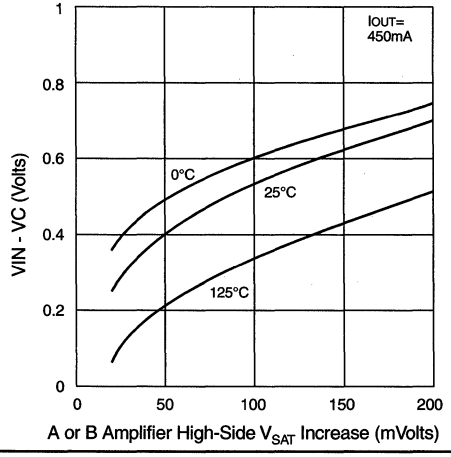
A and B Amplifier High and Low V_{SATS}



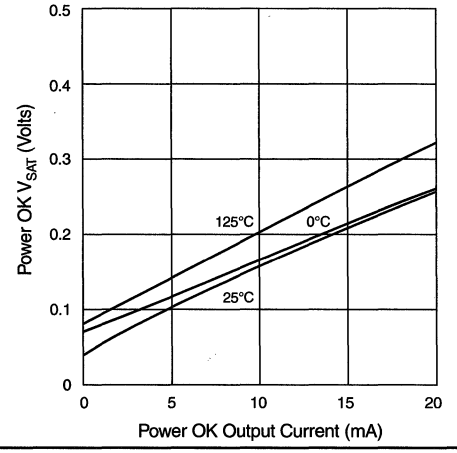
A and B Amplifier Total V_{SAT}



VIN to VC Headroom

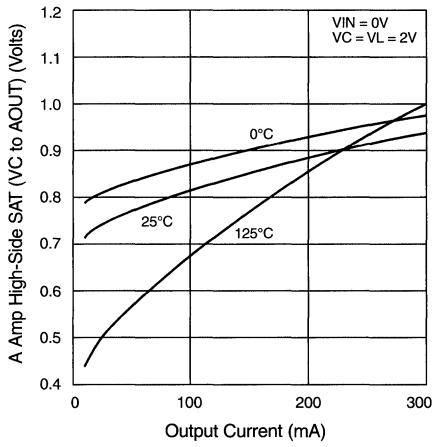


PWROK Saturation Voltage

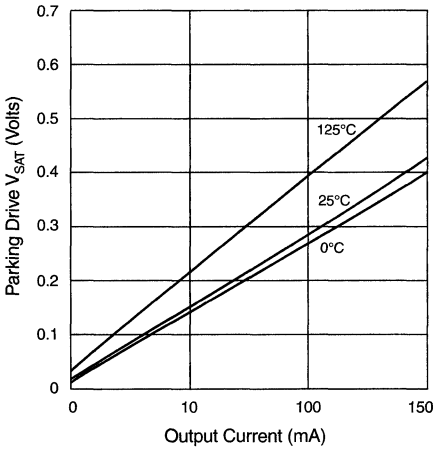


APPLICATION INFORMATION (cont.)

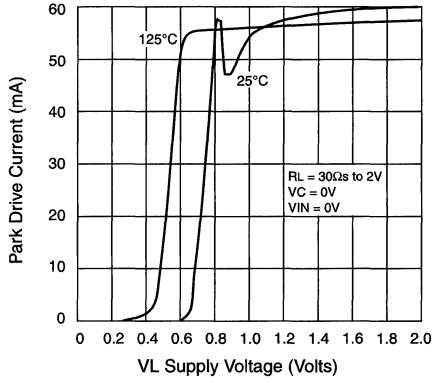
A Amplifier High-Side V_{SAT} in Park Mode



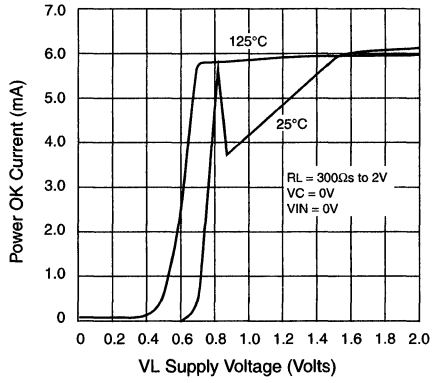
PRKDRV Saturation Voltage



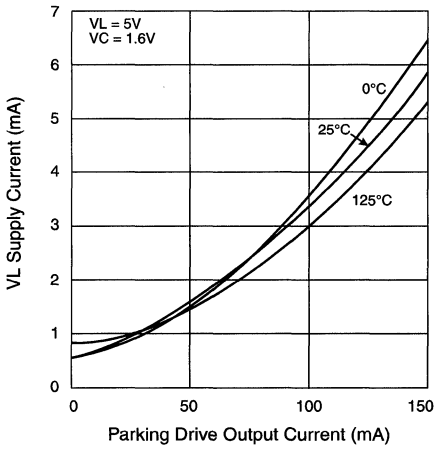
PRKDRV Current vs. VL Supply



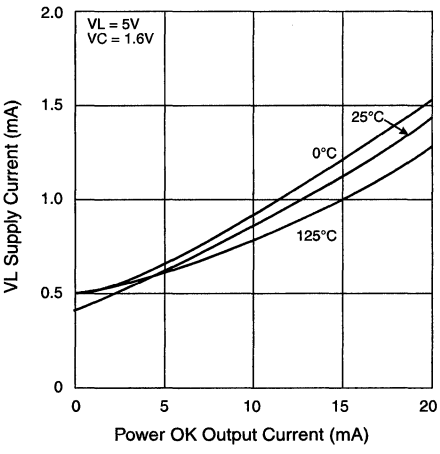
PWROK vs. VL Supply



VL Current vs. PRKDRV Current



VL Current vs. PWROK Current



APPLICATION INFORMATION (cont.)

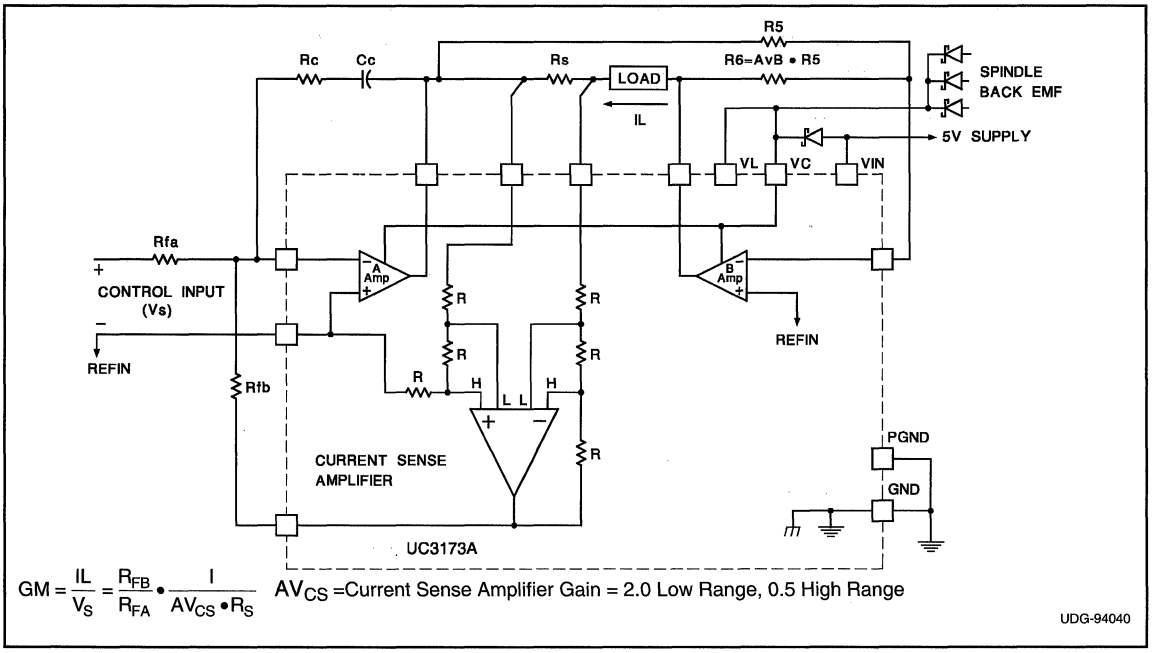


Figure 1. Typical application.

Design Procedure for Application of the UC3173A

The following is a simple design flow that can be used to configure the UC3173A Full Bridge Power Amplifiers as shown in Fig. 1.

Definitions:

f_{3DB}	=	the closed loop 3dB bandwidth
$A_V B$	=	B amplifier closed loop gain, = R6/R5
$A_V CS$	=	current sense amplifier gain, = 0.5 in high range, and 2.0 in low range
$f_{GBW}A$	=	gain bandwidth product of the A amplifier
G_{mHR}	=	closed loop transconductance in high rangemode
G_{mLR}	=	closed loop transconductance in low range mode
L	=	load inductance
R_L	=	load resistance

A. Current Sense Resistor

Choose R_S to be as large as head room will tolerate, this is the series current sense resistor.

B. Select Feedback Resistance

Choose a value of R_{FB} to be less than the peak current sense amplifier swing divided by 1mA. A value in the range of 3k to 10k is suggested.

C. Set Transconductance

Calculate R_{FA} according to:

$$R_{FA} = \frac{R_{FB}}{0.5 \bullet R_S \bullet G_{mHR}} \quad (1)$$

If the range change option is not going to be used, it is recommended that the device be set in the low range mode and R_{FA} be calculated by:

$$R_{FA} = \frac{R_{FB}}{2 \bullet R_S \bullet G_{mLR}} \quad (2)$$

D. Optimize Voltage Swing

In order to assure that maximum voltage drive to the load is achievable, there are some precautions that should be taken. In a standard configuration, the B amplifier is slaved to the A amplifier. The bias point of the and the gain of the B amplifier, as well as the saturation voltages of the power output stages, will affect the voltage available to the load.

There are two simple procedures to follow, either will insure that the capabilities of the device are fully utilized. The first is to set the REFIN voltage at the center of the available voltage swing at the output of the power amplifiers. This optimum reference is defined by equation (3)

APPLICATION INFORMATION (cont.)

$$V_{REFIN}\ (optimum) = \frac{VIN - V_{HS(SAT)} + V_{LS(SAT)}}{2} \quad (3)$$

Where: $V_{HS(SAT)}$ = high-side V_{SAT} at maximum load
$V_{LS(SAT)}$ = low-side V_{SAT} at maximum load.

A second approach is to raise the gain of the B amplifier to insure maximum swing. For a given REFIN voltage the gain of the B amplifier, set by the ratio of the feedback resistors, can be made greater than unity as given by:

$$A_VB = \frac{VIN - V_{HS(SAT)} - V_{REF}}{V_{REFIN} - V_{LS(SAT)}} \quad \text{or,} \quad (4)$$

$$\frac{V_{REFIN} - V_{LS(SAT)}}{VIN - V_{HS(SAT)} - V_{REF}}$$

whichever is greater than unity.

For a typical case, where V_{REFIN} has been set at VIN/2, the required gain for a 5 volt system will be about 1.5, and for a 12 volt system, 1.2.

It is worth noting that when using this method the B amplifier will saturate before the A amplifier on one polarity of the voltage swing. During the time when the B amplifier is saturated and the A amplifier is not, the small signal bandwidth of the loop will be reduced by a factor of $(A_VB + 1)$.

E. Loop Compensation

The normal configuration for compensation of the power amplifier is shown in Fig. 1. A simple R_C network, R_CC_C, around the A amplifier is all that is required. The value of the R_CC_C time constant is typically chosen to correspond to the electrical time constant of the load, given by R_L/L.

The bandwidth of the closed loop amplifier can be set by choosing the value of R_C. Calculate R_C according to:

$$R_C = \frac{2\pi L \bullet f_{3dB} \bullet R_{FB}}{(1 + A_VB)A_VCS \bullet R_S} \quad (5)$$

Use A_VCS = 0.5 if range changing is to be used, and A_VCS = 2.0 if only the low range mode of operation is to be used.

The compensation zero is typically set to coincide with the L/R time constant of the Load. C_C can then be calculated by:

$$C_C = \frac{L}{R_C(R_S + R_L)} \quad (6)$$

In the closed loop transconductance amplifier, the A amplifier operates at the highest noise gain. Noise gain is a measure of the feedback ratio at which the amplifier is operating. For the configuration of the A amplifier in Fig. 1, the noise gain is given by the impedance ratio of the R_C-C_C series network, to the parallel combination of R_{FA} and R_{FB}. For the A amplifier to operate at its expected closed loop gain, the noise gain at any frequency must not exceed its Gain Bandwidth Product (GBW) divided by that frequency. Applying this to the expression above will yield a result for the maximum 3dB bandwidth that can be achieved for a given configuration.

$$f_{3dB(MAX)} = \left(\frac{f_{GBW}A \bullet (1 + A_VB) \bullet A_VCS \bullet R_S \bullet R_{FA}}{2\pi L \bullet (R_{FA} + R_{FB})}\right)\frac{1}{2} \quad (7)$$

Where: $f_{GBW}A$ is the GBW of the A amplifier.

In the UC3173A, to accommodate wider power amplifier bandwidths, the GBW Product of the A amplifier has been extended to 2MHz. Care should be taken that the A amplifier gain bandwidth product is not limiting the closed loop performance of the configured power amplifier. This is easily checked by making sure that R_C is less than a critical value, $R_{C(MAX)}$, as given by:

$$R_{C(MAX)} = R_{FB}\left(\frac{f_{GBW}A \bullet 2\pi L \bullet R_{FA}}{(A_VB + 1) \bullet A_VCS \bullet R_S(R_{FA} + R_{FB})}\right)\frac{1}{2} \quad (8)$$

Again, use A_VCS = 0.5 if range changing is used, and A_VCS = 2.0 if only the low range mode of operation is used.

F. Using The Comp Pin

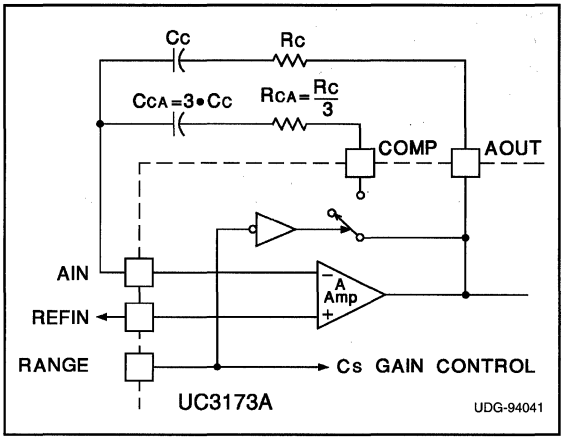
When the range change feature of the UC3173A is used, the closed loop bandwidth of the power amplifier will change according to (7). In other words, the bandwidth would be four times larger during the low range mode when A_VCS is equal to 2, than during the high range mode when A_VCS is equal to 0.5, unless the value of R_C is adjusted to compensate.

The COMP pin on the UC3173A can be used to do this. The COMP pin acts as a simple switch that allows a parallel compensation network to be applied around the A amplifier during low range operation. A simple network as shown here will keep the loop response constant independent of the range condition.

To maintain the same 3dB bandwidth in both the high and low range modes set R_{CA} and C_{CA} to:

$$R_{CA} = \frac{R_C}{3},\ C_{CA} = 3C_C \quad (9)$$

APPLICATION INFORMATION (cont.)



The COMP pin switches in a parallel compensation network to stabilize the small signal bandwidth with range changes.

Head Parking

In Fig. 2, the UC3173A is shown configured to force a programmed voltage at the A amplifier output upon the activation of a park condition. A pair of feedback resistors R1 and R2 set this voltage as defined by:

$$R1 = R2\left(\frac{VPARK}{1.3} - 1\right) \qquad (10)$$

R2 is typically chosen in the range of 10kΩ to 100kΩ.

The B amplifier output is tri-stated during park, this side of the load is driven low by the PRKDRV pin. A series resistor, RP in the figure, can be inserted in series with the load to limit the peak current if required.

The UV thresholds for the supply monitors are set by picking R4 and R6 values in the 10kΩ to 100kΩ range and then calculating R3 and R5 according to:

$$R3 = R4\left(\frac{UV1}{1.3} - 1\right), \text{and } R5 = R6\left(\frac{UV2}{1.3} - 1\right) \qquad (11)$$

During park, supply to the load, and the UC3173A, is typically recovered from the back EMF of the spindle motor. When the supply voltage at the VL supply pin drops below the UVLO voltage, (2.3V high-to-low), the output of the A amplifier is forced high, over-riding the programmed park voltage. The UC3173A will maintain drive to the load down to low supply levels. For example, with 1.5 volts of recovered back EMF, the UC3173A can still deliver 50mA of drive to a 10Ω load.

Parking With Very Low Back EMF

The UC3173A can also be configured to get parking drive to the load with very low recovered back EMF. Fig. 3 illustrates how the PWROK pin can be used to drive an external PNP device to achieve very low parking drive V_{SAT} losses. With this configuration, the UC3173A will be able to force approximately one volt across the load with a recovered back EMF voltage of 1.3V.

During system commanded parking with the supplies present, the VPARK pin is still used to set the maximum voltage to the load. The logic function of the PWROK pin is still available since the external PNP will provide isolation to this output when it is high.

Base drive to the PRKDRV and PWROK pins are provided by the VL supply pin. By using a hold up capacitor, C_{HOLD}, the drive can be maintained to the load as the back EMF drops to below 1V. A variation on this approach is to add a connection between the VL pin and the recovered back EMF, this will eliminate the need for the holdup capacitor and provide operation down to about 1.2V of back EMF recovery. Care with this approach should be taken in case the 5V supply hangs at just below the programmed UV threshold. In this situation large currents could flow from this supply through the external PNP and into the A output which, until the supply drops below a certain level, is forcing a programmed voltage.

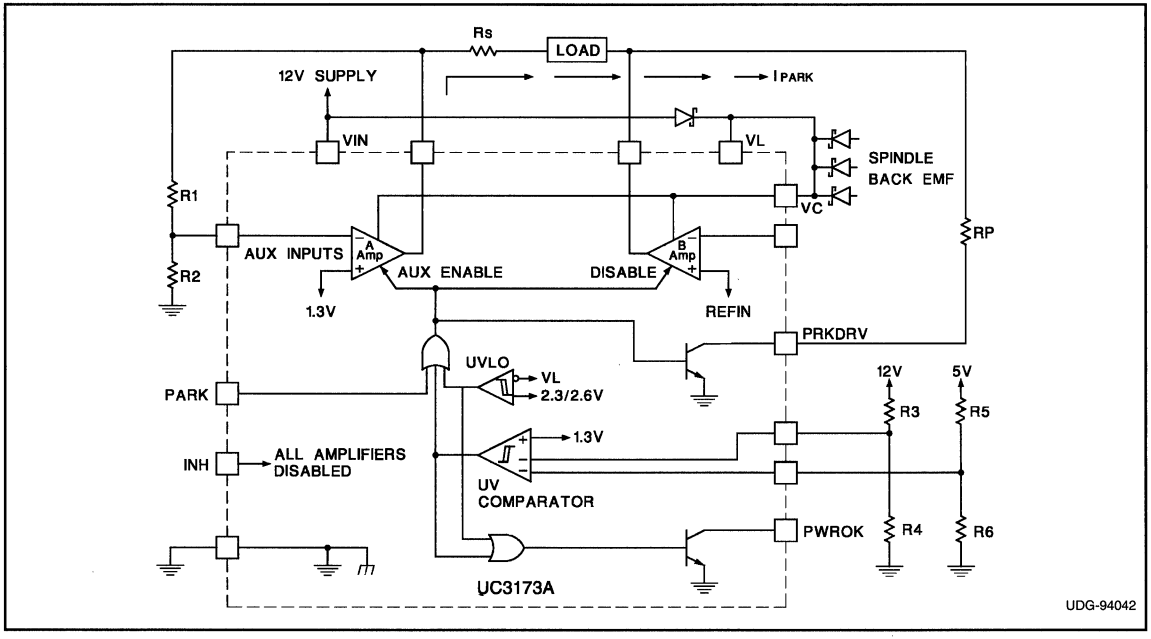


Figure 2. Controlled velocity head parking.

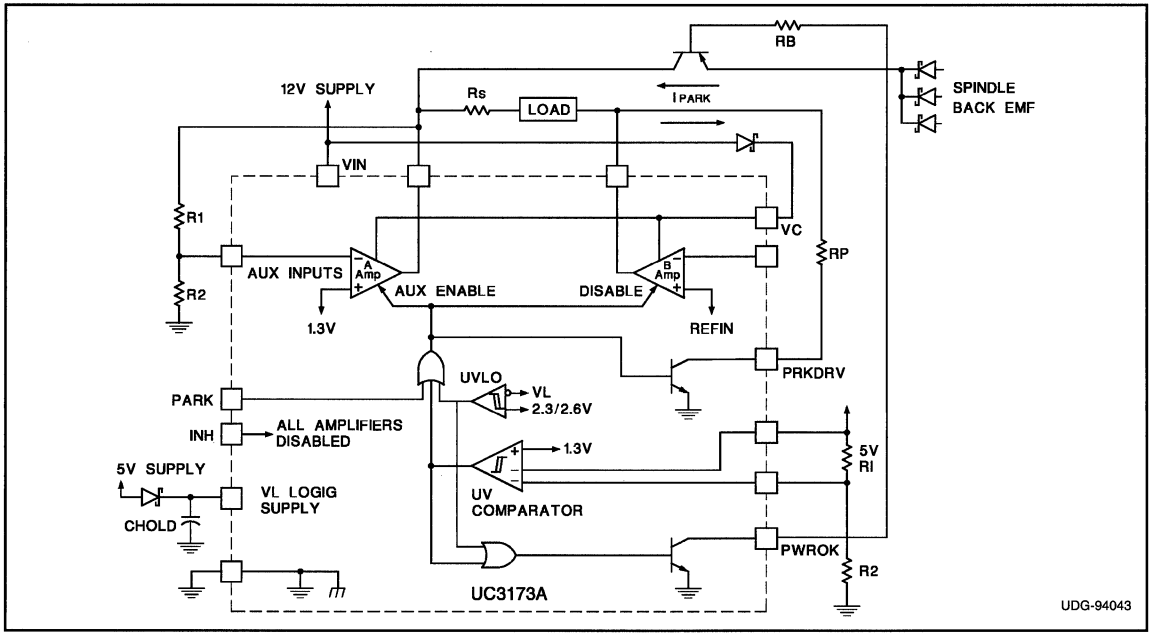


Figure 3. Head parking with low back EMF.

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- ±800mA Load Current
- 1.25V Total V_{SAT} at 800mA
- Controlled Velocity Head Parking
- Precision Dual Supply Monitor with Indicator
- Limit Input to Force Output Extremes
- Inhibit Input and UVLO
- 4V to 15V Operation

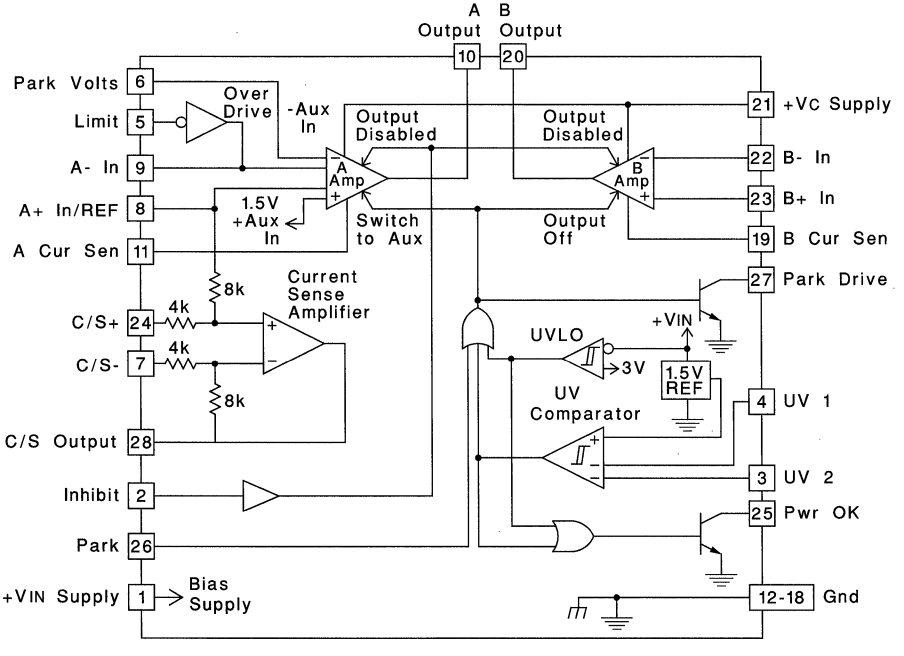
DESCRIPTION

This full-bridge power amplifier is rated for continuous output current of 0.8 Amperes and is intended for use in demanding servo applications such as head positioning for high-density disk drives. The device includes a precision current sense amplifier that provides accurate control of load current. Current is sensed with a single resistor in series with the load. The power amplifier has a very low output saturation voltage and will operate down to 4V supply levels. Power output stage protection includes current limiting and thermal shutdown.

Auxiliary functions on this device include a dual-input under-voltage comparator, which can monitor two independent supply voltages and force a built-in head park function when either is below minimum. When activated by either the UV comparator, or a command at the separate PARK input, the park circuitry will override the amplifier inputs to convert the power outputs to a programmable constant voltage source which will hold regulation as the supply voltage falls to below 3.0 Volts. Added features include a POWER OK flag output, a LIMIT input to force the drive output to its maximum level in either polarity, and a overriding INHIBIT input to disable all amplifiers and reduce quiescent supply current.

This device is packaged in a power PLCC surface mount configuration which maintains a standard 28-pin outline, but with 7 pins along one edge allocated to ground for optimum thermal transfer. And is also available in a 24-pin surface mount SOIC package.

BLOCK DIAGRAM



Note: Pin numbers refer to PLCC package.

UDG-92054-1

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (+VIN,+VC) 20V
UV Comparator, and Digital Inputs
  Maximum forced voltage ..... -0.3V to 10V
  Maximum forced current ..... ±10mA
C/S Inputs
  Maximum forced voltage ..... -0.3V to 20V
  A and B Amplifier Inputs ..... -0.3V to +VIN
Open Collector Output Voltages 20V
A and B Output Currents (continuous)
  Source ..... Internally Limited
  Sink 1.0A
Parking Drive Output Current
  Continuous 150mA
  Pulsed 1A
Output Diode Current (pulsed) 1A
Power OK Output Current(continuous) 30mA
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C

Note 1: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals. "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.
Note 2: See Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

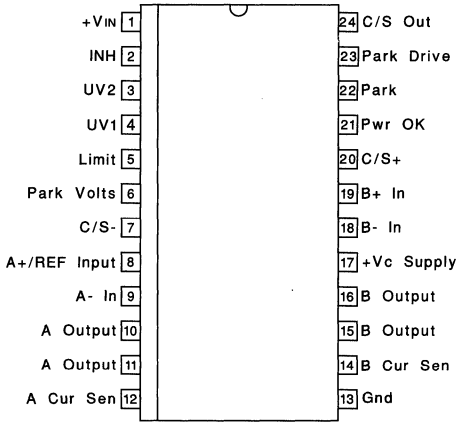
Thermal Data

QP Package:

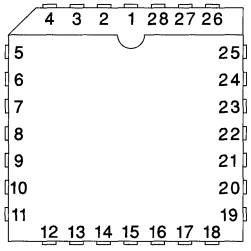
Thermal Resistance Junction to Leads,
  θJL ..... 15°C/W
Thermal Resistance Junction to Ambient,
  θJA ..... 40°C/W

CONNECTION DIAGRAMS

SOIC-24 (Top View)
DW Package



PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
INH	2
UV2	3
UV1	4
Limit	5
Park Volts	6
C/S-	7
A+/REF Input	8
A- In	9
A Output	10
A Cur Sen	11
Gnd (Heat Dissipation Pins)	12-18
B Cur Sen	19
B Output	20
+Vc Supply	21
B- In	22
B+ In	23
C/S+	24
Pwr OK	25
Park	26
Park Drive	27
C/S Out	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications apply for 0°C ≤ TA ≤ 70°C, +VIN = 12V, +VC = +VIN, A+/REF Input = 6V. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY					
+VIN Supply Current	All Amplifier Outputs = 6V		35	42	mA
+VC Supply Current	IOUT = 0A		1		mA
+VIN UVLO Threshold	Low to High		2.8	3.0	V
UVLO Threshold Hysteresis			200		mV

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated specifications apply for 0°C ≤ T_A ≤ 70°C, +V_{IN} = 12V, +V_C = +V_{IN}, A+/REF INPUT = 6V. T_A=T_J.

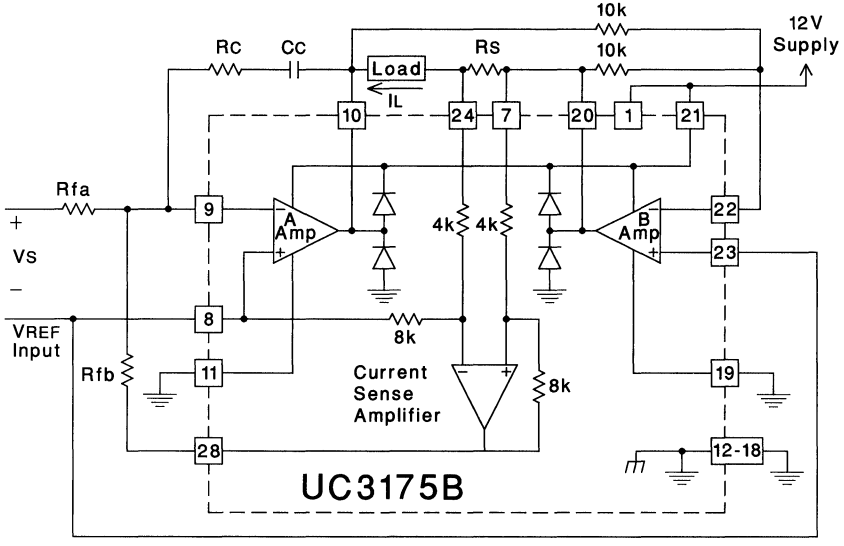
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDER VOLTAGE (UV) COMPARATOR					
Input Bias Current		-1.5	-0.5		µA
UV Thresholds	Low to High, Other Input = 5V	1.48	1.50	1.52	V
UV Threshold Hysteresis		15	25	40	mV
Pwr OK V_{SAT}	I_{OUT} = 5mA			0.45	V
Pwr OK Leakage	V_{OUT} = 20V			5	µA
POWER AMPLIFIERS A and B					
Input Offset Voltage	V_{CM} = 6V, A Amplifier			8	mV
	B Amplifier			12	mV
Input Offset Drift	Note 1, A Amplifier Only			25	µV/°C
Input Bias Current	V_{CM} = 6V, except A+/REF Input	-500	-150		nA
Input Offset Current	V_{CM} = 6V, B Amplifier Only			200	nA
Input Bias Current at A+/Ref Input	(A+/Ref–C/S+)/12k, T_J = 25°C	60	84	105	µA/V
CMRR	1V ≤ V_{CM} ≤ 10V	70	90		dB
PSRR	+V_{IN} = 4V to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	V_{OUT} = 1V, Sinking 500mA to V_{OUT} = 11V, Sourcing 500mA	3.0	15.0		V/mV
Slew Rate	1 to 13V, 13 to 1V, T_J = 25°C		1	2.1	V/µs
Unity Gain Bandwidth	Note 1, A Amplifier		2		MHz
	Note 1, B Amplifier		1		MHz
High-Side Current Limit		0.8	1.0		A
Output Saturation Voltage	High-Side, I_{SOURCE} = 250mA		0.7		V
	High-Side, I_{SOURCE} = 800mA		0.85		V
	Low-Side, I_{SINK} = 250mA		0.3		V
	Low-Side, I_{SINK} = 800mA		0.4		V
	Total, I_{OUT} = 250mA		1.0	1.2	V
	Total, I_{OUT} = 800mA		1.25	1.6	V
High Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
Low Side Diode V_F	I_D = 800mA, Inhibit Activated		1.0		V
CURRENT SENSE AMPLIFIER					
Input Offset Voltage	V_{CM} = 6V			2.0	mV
Input Offset Change with Common Mode Input	0V ≤ V_{CM} ≤ 12V			1500	µV/V
Input Offset Drift	Note 1			8	µV/°C
Voltage Gain	-1.0V ≤ V_{DIFF} ≤ +1.0V, V_{CM} = 6V	1.95	2.00	2.05	V
Output Saturation Voltage	Low-Side, I_{SINK} = 1.5mA		0.3	0.5	V
	High-Side, I_{SOURCE} = 1.5mA		0.4	0.7	V
Maximum A+/Ref Input	Volts Below +V_{IN}, C/S+ & C/S- = B_{OUTPUT} Max @ 10mA Output Current, +V_{IN} = 4.5V, C/S VIO ≤ 5mV		2.6	3.0	V
PARKING FUNCTION					
Park Input Threshold		0.7	1.1	1.7	V
Park Input Current	Park Input = 1.7V		60	100	µA
Park Drive Saturation Voltage, PD_{VSAT}	I_{SINK} = 100mA		0.3	0.5	V
Parking Drive Leakage	V_{OUT} = 20V			100	µA
Amplifier A Aux Input Bias Current		-500	-150		nA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated specifications apply for 0°C ≤ TA ≤ 70°C, +VIN = 12V, +VC = +VIN, A+/REF Input = 6V. TA=TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARKING FUNCTIONS (cont.)					
Amplifier A Saturation Voltage, AHVSAT	ISOURCE = 50mA, +VIN = 3V		0.65	0.8	V
Regulating Voltage at Park Volts		1.47	1.50	1.53	V
Minimum Parking Supply Voltage	AHVSAT + PDVSAT ≤ 1.3V @ 50mA		1.7	1.9	V
AUXILIARY FUNCTIONS					
Limit Input Low Voltage	A Output Forced Low	0.7	0.8		V
Limit Input High Voltage	A Output Forced High		2.2	2.3	V
Limit Inactive		1.2		1.8	V
Limit Open Circuit Voltage		1.45	1.50	1.55	V
Limit Input Resistance	1.2V ≤ Limit Input ≤ 1.8V		10		kΩ
Inhibit Input Threshold		0.7	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V		400	700	µA
Supply Current when Inhibited	The sum of +VIN and +VC currents		2	6	mA
Thermal Shutdown Temperature			165		°C

Note 1: This specification not tested in production.

UC3175B Series Current Sensing



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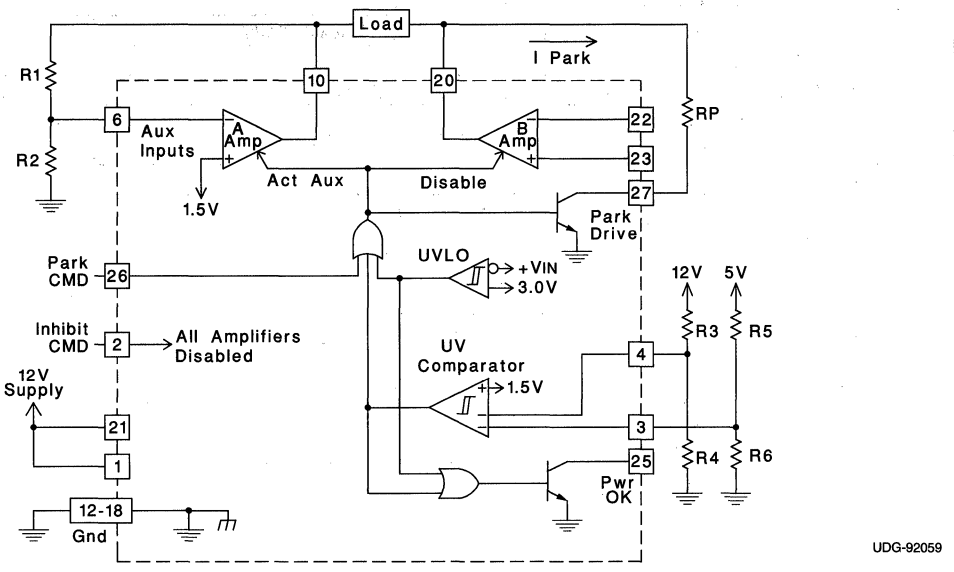
$$Go = \frac{IL}{Vs} = \frac{Rfb}{Rfa \bullet 2 \bullet Rs}$$

Parking Function



Notes: *Parking voltage* $= \dfrac{1.5V \bullet R1 + R2}{R2 - (I_L \bullet RP)}$

RP is optional for current limiting.
Inhibit and Park Inputs are active high.
Pwr OK is low on power failure.

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Full Bridge Power Amplifier

FEATURES

- Dual Power Operational Amplifiers
- ±2A Output Current Guaranteed
- Precision Current Sense Amplifier
- Two Supply Monitoring Inputs
- Parking Function and Under-Voltage Lockout
- Safe Operating Area Protection
- 3V to 35V Operation

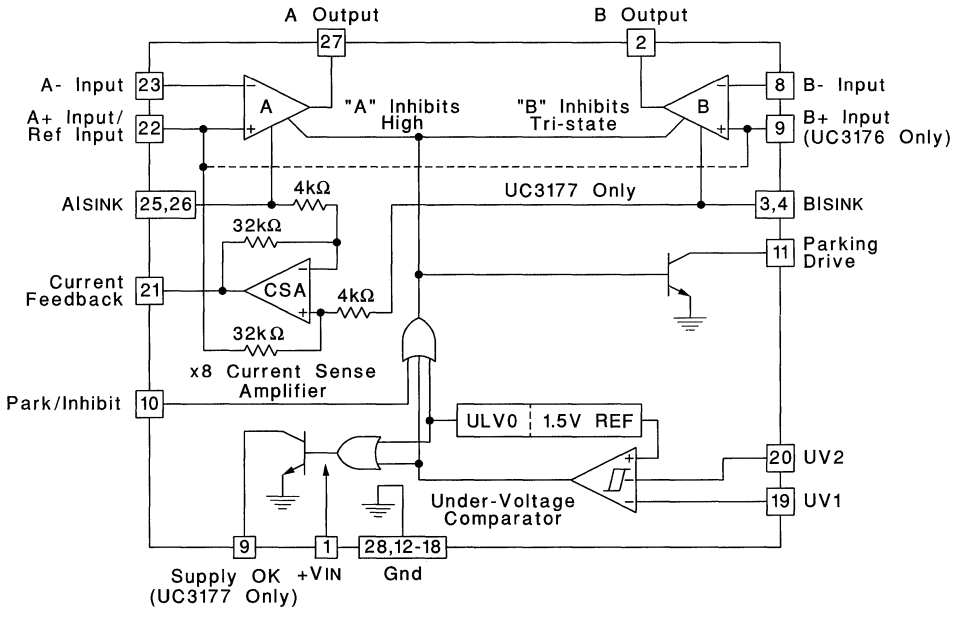
DESCRIPTION

The UC3176/7 family of full bridge power amplifiers is rated for a continuous output current of 2A. Intended for use in demanding servo applications such as disk head positioning, the onboard current sense amplifier can be used to obtain precision control of load current, or where voltage mode drive is required, a standard voltage feedback scheme can be used. Output stage protection includes foldback current limiting and thermal shutdown, resulting in a very rugged device.

Auxiliary functions on this device include a dual input under-voltage comparator that can be programmed to respond to low voltage conditions on two independent supplies. In response to an under-voltage condition the power Op-Amps are inhibited and a high current, 100mA, open collector drive output is activated. A separate Park/Inhibit command input.

The devices are operational over a 3V to 35V supply range. Internal under-voltage lockout provides predictable power-up and power-down characteristics.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply voltage, (+VIN) 40V
Park/Inhibit, UV1 and UV2 inputs (zener clamped)
  Maximum forced voltage ..... -0.3V to 10V
  Maximum forced current..... ±10mA
Other Input Voltages..... -0.3V to +VIN
AISINK and BISINK Voltages..... -0.3V to 6V
Open Collector Output Voltages..... 40V
A and B Output Currents (Continuous)
  Source ..... Internally Limited
  Sink..... 2.5A
Total Supply Current (Continuous)..... 4A
Parking Drive Output Current (Continuous)..... 200mA
Supply OK Output Current, UC3177 (Continuous) ... 30mA
Operating Junction Temperature ..... -55°C to +150°C
Power Dissipation at TC = +75°C
  QP package..... 4W
Storage Temperature..... -65°C to +150°C

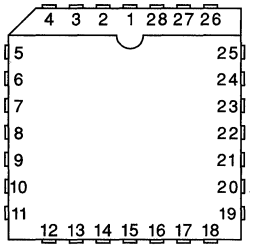
Note 1: Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of, the specified terminals.

THERMAL DATA

QP package:
Thermal Resistance Junction to Leads, θJL ..... 15°C/W
Thermal Resistance Junction to Ambient, θJA .... 50°C/W

CONNECTION DIAGRAM

PLCC-28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
+VIN	1
B Output	2
BISINK(Sense)	3
BISINK	4
N/C	5-7
B- Input	8
*	9
Park/Inhibit	10
Parking Drive	11
Gnd (Heat Flow Pins)	12-18
UV1	19
UV2	20
Current Feedback	21
A+ Input	22
A- Input	23
N/C	24
AISINK	25
AISINK(Sense)	26
A Output	27
Gnd	28

**Pin 9: UC3176, B+ Input*
UC3177, Supply OK

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0 to 70°C, +VIN = 12V, TA = TJ.

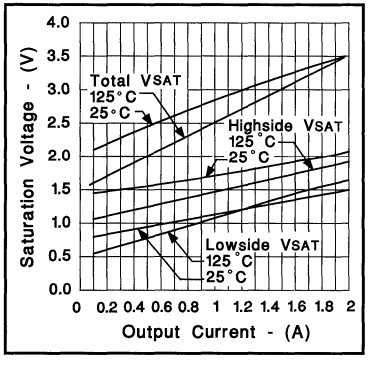
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Supply					
Supply Current	+VIN = 12V		18	25	mA
	+VIN = 35V		21	30	mA
UVOL Threshold	+VIN low to high		2.8	3.0	V
	Threshold Hysteresis		220	300	mV
Power, Amplifier, A and B					
Input Offset Voltage	VCM = 6V, VOUT = 6V			8	mV
Input Bias Current	VCM = 6V, Except A+ Input	-500	-100		nA
Input Bias Current at A+/Reference Input	(A+/Ref - BISINK)/36kohms; TJ = 25°C	23	28	35	µA/V
Input Offset Current B Amp (UC3176 Only)	VCM = 6V			200	nA
CMRR	VCM = 1 to 33V, +VIN =35V, VOUT = 6V	70	100		dB
PSRR	+VIN = 5 to 35V, VCM = 2.5V	70	100		dB
Large Signal Voltage Gain	VOUT = 3V, w/IOUT = 1A to VOUT = 9V, w/IOUT = -1A	1.5	4		V/mV
Thermal Feedback	+VIN = 20V, Pd = 20W at opposite output		25	200	µV/W
Saturation Voltage	IOUT = -2A, High Side, TJ = 25°		1.9		V
	CIOUT = 2A, Low Side, TJ = 25°C		1.6		V
	Total VSAT at 2A, TJ = 25°C		3.5	3.7	V
Unity Gain Bandwidth			1		MHz
Slew Rate			1		V/µs
Differential IOUT Sense Error Current	IOUT(A) = -IOUT(B), /IOUT/- /AISINK - BISINK/				
in Bridge Configuration	IOUT ≤200mA		3.0	6.0	mA
	IOUT ≤ 2A		5.0	10	mA
High Side Current Limiting	=VIN - VOUT < 12V		-2.7	-2.0	A

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0 to 70°C, $+V_{IN}$ = 12V, T_A = T_J.

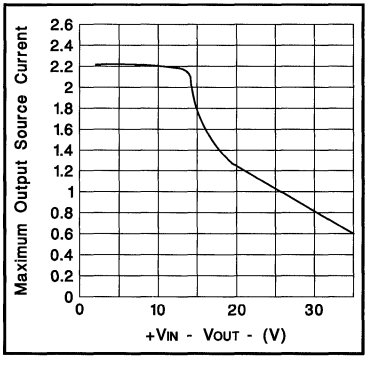
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 0V, A+/Ref at 6V			3	mV
	Ref = 2V to 20V, $+V_{IN}$ = 35, change with Ref input voltage			600	µV/V
Thermal Gradient Sensitivity	$+V_{IN}$ = 20V, Ref = 10V Pd = 20W @ A or B output		5.0	75	µV/W
PSRR	Ref = 2.5V, $+V_{IN}$ = 5 to 35V	70	100		dB
Gain	/AI_{SINK} - BI_{SINK}/ ≤ 0.5V	7.8	8	8.1	V/V
Slew Rate			2		V/µS
3dB Bandwidth			1		MHz
Max Output Current	I_{SOURCE} = $+V_{IN}$ - V_{OUT} = 0.5V	2.5	3.5		mA
Output Saturation Voltage	I_{SOURCE} = 1.5mA, High Side		0.15	0.30	V
	I_{SINK} = 5mA, Low Side		1.4	1.7	V
Under-Voltage Comparator					
Threshold Voltage	Low to High, other input at 5V	1.44	1.50	1.56	V
	Threshold Hysteresis	50	70	80	mV
Input Current	Input = 2V, other input at 5V	-2	-.05		µA
Supply OK V_{SAT} (UC3177 Only)	I_{OUT} = 5mA			0.45	V
Supply OK Leakage (UC3177 Only)	V_{OUT} = 35V			5	µA
Park/Inhibit					
Park/Inhibit Thl'd		1.1	1.3	1.7	V
Park/Inhibit Input Current	At threshold		60	100	µA
Parking Drive Saturation Voltage	I_{OUT} = 100mA		0.3	0.7	V
Parking Drive Leakage	V_{OUT} = 35V			15	µA
Thermal Shutdown					
Shutdown Temperature			165		°C

8

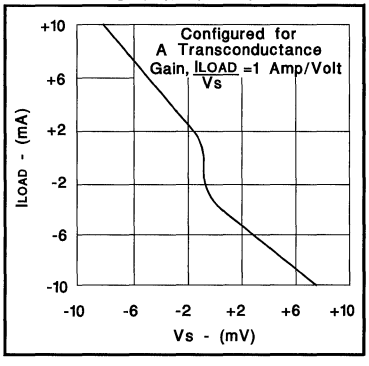
Output Saturation Voltage vs Current



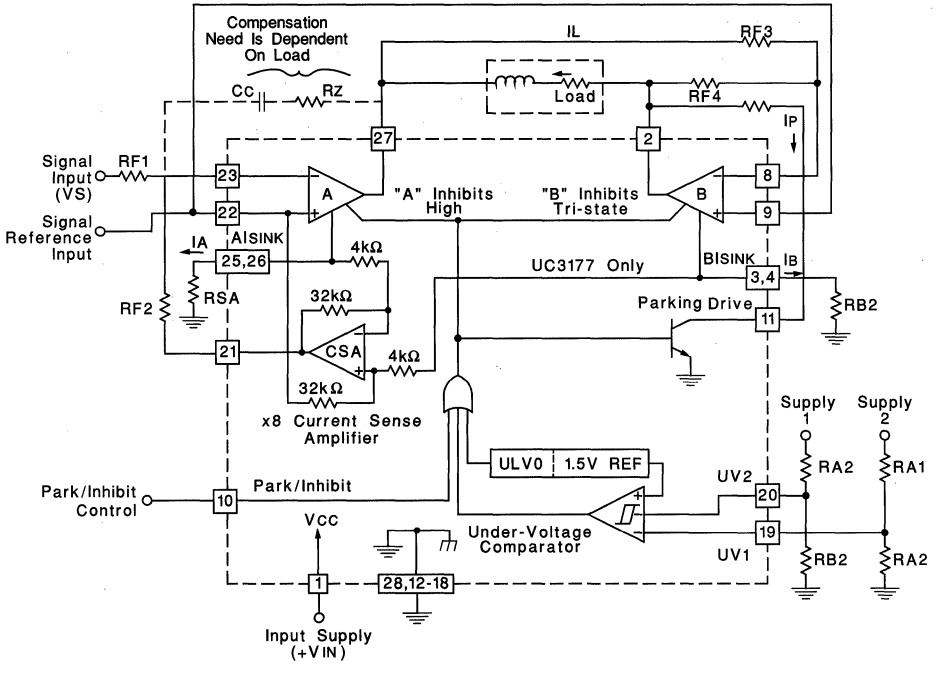
Maximum Source Current vs +VIN - VOUT



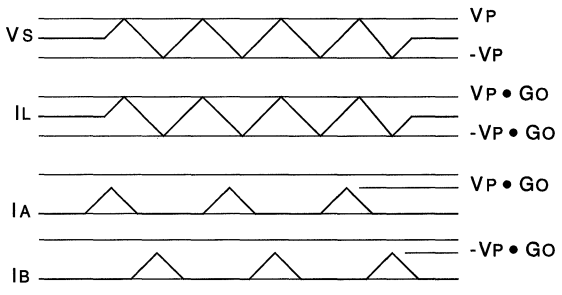
Crossover Current Error Characteristic



APPLICATION AND OPERATION INFORMATION



WAVEFORMS FOR ABOVE APPLICATION



DESIGN EQUATIONS

$$\text{Transconductance } (G_O) = \frac{I_L}{V_S} = \frac{R_{F2}}{R_{F1}} \times \left(\frac{1}{8R_S}\right)$$

with: $R_{SA} = R_{SB}$ and $R_{F3} = R_{F4}$

$$\text{Parking Current } (I_P) = \frac{V_{IN} - 1.5}{R_P + R_L}$$

where: R_L = load resistance

Under-Voltage Thresholds, at Supplies
High to Low Threshold, $(V_{LH}) = 1.425\ (R_A + R_B)/R_B$
Low to High Threshold, $(V_{HL}) = 1.5\ (R_A + R_B)/R_B$

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Full Bridge Power Amplifier

FEATURES

- Precision Current Control
- ±450mA Load Current
- 1.2V Typical Total Vsat at 450mA
- Programmable Over-Current Control
- Range Control for 4:1 Gain Change
- Compensation Adjust Pin for Range Bandwidth Control
- Inhibit Input and UVLO
- 3V to 15V Operation
- 12mA Quiescent Supply Current

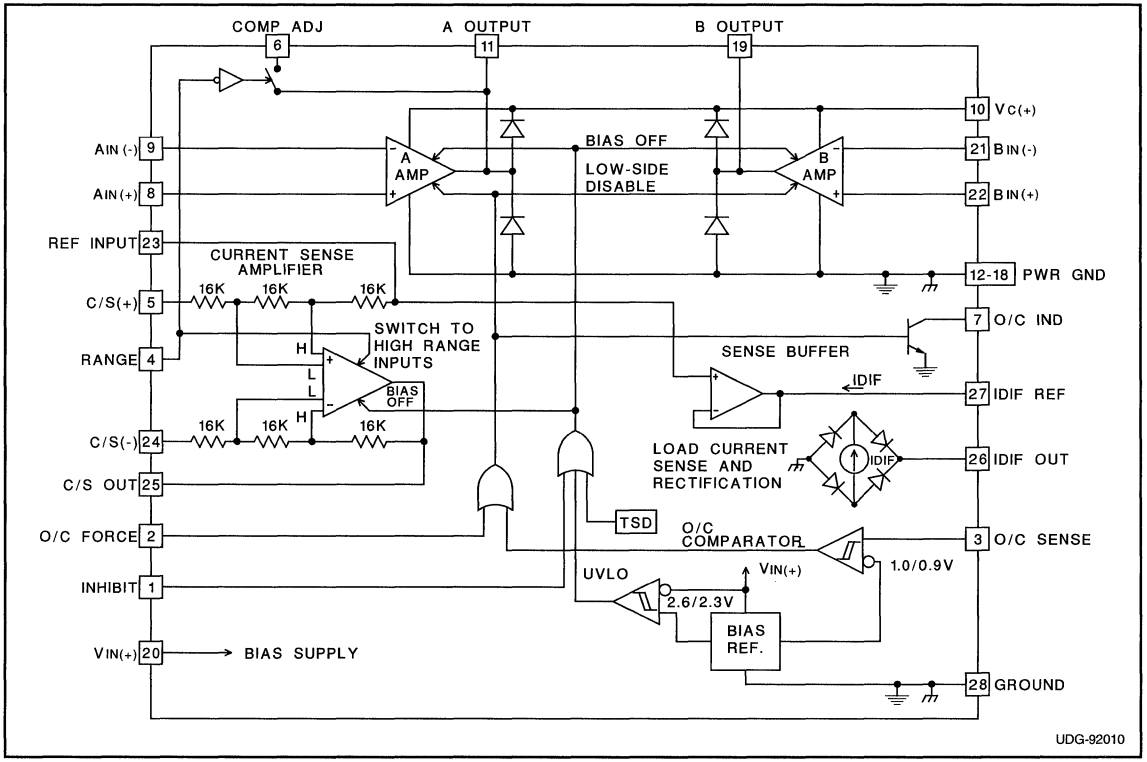
DESCRIPTION

The UC3178 full-bridge power amplifier, rated for continuous output current of 0.45 Amperes, is intended for use in demanding servo applications. This device includes a precision current sense amplifier that senses load current with a single resistor in series with the load. The UC3178 is optimized to consume a minimum of supply current, and is designed to operate in both 5V and 12V systems. The power output stages have a low saturation voltage and are protected with current limiting and thermal shutdown. When inhibited, the device will draw less than 1.5mA of total supply current.

Auxiliary functions on this device include a load current sensing and rectification function that can be configured with the device's over-current comparator to provide tight control on the maximum commanded load current. The closed loop transconductance of the configured power amplifier can be switched between a high and low range with a single logic input. The 4:1 change in gain can be used to extend the dynamic range of the servo loop. Bandwidth variations that would otherwise result with the gain change can be controlled with a compensation adjust pin.

This device is packaged a power PLCC, "QP" package which maintains a standard 28-pin outline, but with 7 pins along one edge directly tied to the die substrate for improved thermal performance.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, (V_{IN}(+), V_C(+)) 20V
O/C Sense, Logic Inputs, and REF Input
  Maximum forced voltage . . . . . -0.3V to 10V
  Maximum forced current . . . . . ±10mA
A & B Amplifier Inputs . . . . . -0.3V to (V_{IN}(+) + 1.0V)
O/C Indicate Open Collector Output Voltage 20V
A and B Output Currents(continuous)
  Source . . . . . Internally Limited
  Sink 0.6A
Output Diode Current (pulsed)* 0.5A
O/C Ind Output Current(continuous) 20mA
Operating Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C

**Notes: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals, "Pulsed" is defined as a less than 10% duty cycle pulse with a maximum duration of 500µs.*

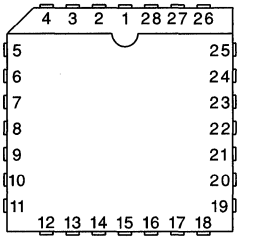
THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)
  Thermal Resistance Junction to Leads, θjl . . . . . 15°C/W
  Thermal Resistance Junction to Ambient, θja . . . 30-40°C/W

Note: The above numbers for θjl are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.

CONNECTION DIAGRAM

PLCC - 28 (Top View)
QP Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
Inhibit	1
O/C Force	2
O/C Sense	3
Range	4
C/S(+)	5
Comp Adj	6
O/C Ind	7
A_{IN}(+)	8
A_{IN}(-)	9
V_C(+) Supply	10
A Output	11
Pwr Gnd	12
Pwr Gnd	13
Pwr Gnd	14
Pwr Gnd	15
Pwr Gnd	16
Pwr Gnd	17
Pwr Gnd	18
B Output	19
V_{IN}(+)	20
B_{IN}(-)	21
B_{IN}(+)	22
REF Input	23
C/S(+)	24
C/S Out	25
IDIF Out	26
IDIF REF	27
Ground	28

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated specifications hold for T_A = 0°C to 70°C, V_C(+) = V_{IN}(+) = 12V, REF Input = V_{IN}(+)/2, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply					
V_{IN} (+)Supply Current			12	16	mA
V_C(+) Supply Current	I_{OUT} = OA		1.2	2.0	mA
Total Supply Current	Supplies = 5V,I_{OUT} = OA		12	16	mA
	Supplies = 12V,I_{OUT} = OA		13	18	mA
V_{IN}(+) UVLO Threshold	low to high		2.6	2.8	V
UVLO Threshold Hysterisis			300		mV
Over-Current (O/C) Comparator					
Input Bias Current	V input = 0.8V	-1.0	-.01		µA
Thresholds	low to high	0.97	1.0	1.03	V
Threshold Hysterisis		85	100	115	mV
O/C IND Vsat	I_{OUT} = 5mA, V input low		0.2	0.45	V
O/C IND Leakage	V_{OUT} = 20V			5.0	µA
Power Amplifiers A and B					
Input Offset Voltage	A Amplifier, V_{CM} = 6V			4.0	mV
	B Amplifier, V_{CM} = 6V			12.0	mV
Input Bias Current	V_{CM} = 6V	-500	-50		µA
CMRR	V_{CM} = 0.5 to 13V, Supplies = 15V	70	90		dB
PSRR	V_{IN}(+) = 4 to 15V, V_{CM} = 1.5V	70	90		dB
Large Signal Voltage Gain	Supplies = 12V, V_{OUT} = 1V, I_{OUT} = 300mA				
	to V_{OUT} = 10.5V, I_{OUT} = -300mA	3.0	15.0		V/mV

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated specifications hold for T_A = 0°C to 70°C , $V_C(+)$ = $V_{IN}(+)$ = 12V, REF Input = $V_{IN}(+)/2$, O/C Input & Inhibit Input = 0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Amplifiers A & B (cont.)					
Gain Bandwith Product	A Amplifier		2.0		MHz
	B Amplifier		1.0		MHz
Slew Rate			1.0		V/µs
High-Side Current Limit		0.45	0.65		A
Output Saturation Voltage	High-Side, I_{OUT} = -100mA		0.75		V
	High-Side, I_{OUT} = -300mA		0.85		V
	High-Side, I_{OUT} = -450mA		0.9		V
	Low-Side, I_{OUT} = 100mA		0.2		V
	Low-Side, I_{OUT} = 300mA		0.25		V
	Low-Side, I_{OUT} = 450mA		0.30		V
	Total Vsat, I_{OUT} = 100mA		0.95	1.2	V
	Total Vsat, I_{OUT} = 300mA		1.05	1.4	V
	Total Vsat, I_{OUT} = 450mA		1.25	1.6	V
High-Side Diode, Vf	I_D = 450mA		1.30		V
Current Sense Amplifier					
Input Offset Voltage	V_{CM} = 6V, Low range mode			2.0	mV
	High range mode			4.0	mV
Input Offset Change	V_{CM} = -1V to 13V, Supplies = 12V, Low Range Mode			2000	µV/V
with Common Mode Input	V_{CM} = -1V to 13V, Supplies = 12V, High Range Mode			4000	µV/V
Voltage Gain	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, High Range Mode	0.485	0.50	0.515	V/V
	V_{DIFF} = +1.0 to -1.0V, Vcm = 6V, Low Range Mode	1.95	2.0	2.05	V/V
Saturation Voltage	Low-Side, I_{OUT} = 1mA		0.1	0.3	V
	High-Side, I_{OUT} = -1mA, Referenced to = $V_{IN}(+)$		0.1	0.3	V
Input Bias Current at Ref. Input	(REF Input - C/S(+))/48kohms, Tj = 25°C	15	21	27	µA/V
Load Current Sense and Rectification					
Sense Buffer Offset Voltage	REF Input to IDIF REF, I_{OUT} = ±1mA			10	mV
Sense Buffer CMRR	I_{OUT} = ±1mA, REF Input = 2V to 10V	70	90		dB
IDIF REF to IDIF Out Current	IDIF = ± 100µA, IDIF Out = 1V	0.95	1.0	1.05	A/A
Ratio	IDIF = ±1mA, IDIF Out = 1V	0.94	1.0	1.06	A/A
IDIF Out Supply Sensitivity	IDIF Out = ± 1mA, $V_{IN}(+)$ = 4V to 15V,REF Input = 2V		1.0	5.0	µA/V
IDIF Out Common Mode Sensitivity	I_{OUT} = ±1mA, REF Input = 2V to10V, IDIF Out = 1V				
(delta IDIF Out/delta REF Input)			1.0	5.0	µA/V
Auxiliary Functions					
Inhibit Input Threshold		0.6	1.1	1.7	V
Inhibit Input Current	Inhibit Input = 1.7V	-1.0	-0.5		µA
O/C Force Input Threshold		0.6	1.1	1.7	V
O/C Force Input Current	O/C Force Input = 1.7V		50	100	µA
Range Input Threshold		0.6	1.1	1.7	V
Range Input Current	Range Input = 1.7V		50	100	µA
COMP ADJ Pin Saturation	Range Input = 0V, Pin Current = ±500µA, Referenced				
Voltage	to A_{OUT}		0.02	0.1	V
COMP ADJ Leakage Current	Range Input = 1.7V, Supplies = 12V				
	A_{OUT}-$V_{Comp\ Adj}$ = ±6V			5.0	µA
Total Supply Current When Inhibited	$V_{IN}(+)$ and $V_C(+)$ currents		1.0	1.5	mA
Thermal Shutdown Temperature			165		°C

PIN DESCRIPTIONS:

A & B OUT: Outputs for the A & B power amplifiers, providing differential drive to the load during normal operation. During a UVLO, Inhibit, or O/C condition both of these outputs will be in a high, source only state. High-side diodes are included to catch inductive load currents flowing into these pins, inductive kicks on the low-side are caught by the high-side output transistors.

AIN(+): Non-inverting input to the A amplifier. Normally tied to the REF Input when the current sense amplifier is used.

AIN(-): Inverting input to the A amplifier. Used as the summing node to close the loop on the overall power amplifier.

BIN(+): Non-inverting input to the B amplifier. This pin normally sets the reference point for the differential voltage swing at the load.

BIN(-): Inverting input to the B amplifier. Used to program the gain of the B amplifier.

COMP ADJ: The compensation adjust pin allows the user to provide an auxiliary compensation network for the A amplifier that is only active when the current sense amplifier is in the low range. With this option, the user can control the change in bandwidth that would otherwise result from the gain change in the feedback loop.

C/S(+): The non-inverting input to the current sense amplifier is typically tied to the load side of the series current sense resistor. This pin can be pulled below ground during an abrupt load current change with an inductive load. Proper operation of the current sense amplifier will result if this pin does not go below ground by an amount greater than:

(REF Input / 2) - 0.3V.

C/S(-): The inverting input to the current sense amplifier is typically tied to the connection between the B amplifier output and the current sense resistor that is in series with the load.

C/S Output: The output of the current sense amplifier has a 1.5mA current source pull-up and an active NPN pull-down. The output will pull to within 0.3V of either rail with a load current of less than 1mA.

GND: Reference point for the internal reference, O/C comparator, and other low-level circuitry.

IDIF OUT: Current source output pin. The value of the output current is nominally equal to the magnitude of the current through the IDIF REF pin.

IDIF REF: Output of the IDIF sense buffer. Voltage on this pin will track the applied voltage on the REF Input pin. Current through this pin is full wave rectified and appears as a current sourced from the IDIF OUT pin.

Inhibit : A high impedance logic input that disables the A and B power amplifiers, the IDIF sense buffer, and the Current Sense amplifier. This input has an internal pull-up that will inhibit the device if the input is left open.

O/C Force: Logic input that forces the O/C condition.

O/C IND: Open collector ouput that indicates, with an active low state, an O/C condition.

O/C Sense: Input to the Over Current Comparator. When this input is above its 1V threshold the low-side devices of both the A & B power amplifiers will be disabled forcing a high, source only, state at both outputs.

PWR GND: Current return for all high level circuitry, this pin should be connected to the same potential as GND.

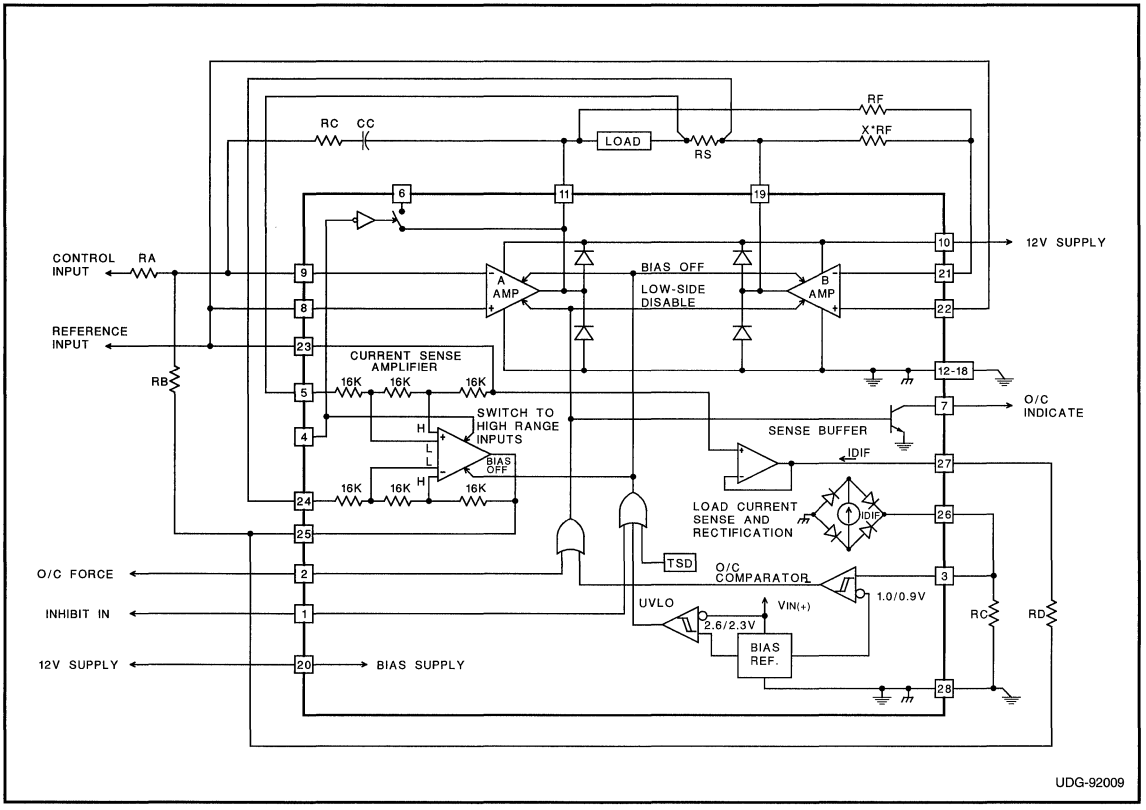
Range: When this pin is open or at a logic low potential, the current sense amplifier will be in its low range mode. In this mode the voltage gain of the amplifier will be 2. If this pin is brought to a logic high, the gain of the current sense amplifier will change into its high range value of 0.5. This factor of four change in gain will vary the overall transconductance of the power amplifier by the same ratio, with the transconductance being the highest in the high mode. This feature allows improved dynamic range of load current control for a given control input range and resolution.

REF Input: Sets the Reference level at the C/S Output, and is normally tied to the system reference level for inputs to the power amplifier.

VIN(+): Provides bias supply to the device. The High-Side drive to the power stages on both the A and B amplifiers is referenced to this pin. The High-side saturation voltages, and UVLO are specified and measured with respect to this supply pin.

VC(+): This supply pin is the high current supply to the collectors of the high-side NPN output devices on the A and B amplifiers. This supply should be powered whenever the A or B amplifiers are to be activated. This pin can operate approximately 400mV below the VIN(+) supply without affecting the voltage available to the load.

TYPICAL APPLICATION



Power amplifier transconductance

$$Go = \frac{Il}{Vs} = \frac{RB}{RA} \bullet \frac{1}{AV_{CS} \bullet RS}$$

Peak commanded load current

$$Il_{MAX} = V_{O/C} \bullet \frac{RD}{RS \bullet AV_{CS} \bullet RE}$$

where:

Il is the load current

Vs is the input command voltage

AV_{CS} is the current sense amplifier gain

= 2.0 in low range mode

= 0.5 in high range mode

$V_{O/C}$ is the 1.0V over-current comparator threshold

UNITRODE CORPORATION
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Stepper Motor Drive Circuit

FEATURES

- Complete Motor Driver and Encoder
- Continuous Drive Capability 350mA per Phase
- Contains all Required Logic for Full and Half Stepping
- Bilevel Operation for Fast Step Rates
- Operates as a Voltage Doubler
- Useable as a Phase Generator and/or as a Driver
- Power-On Reset Guarantees Safe, Predictable Power-Up

DESCRIPTION

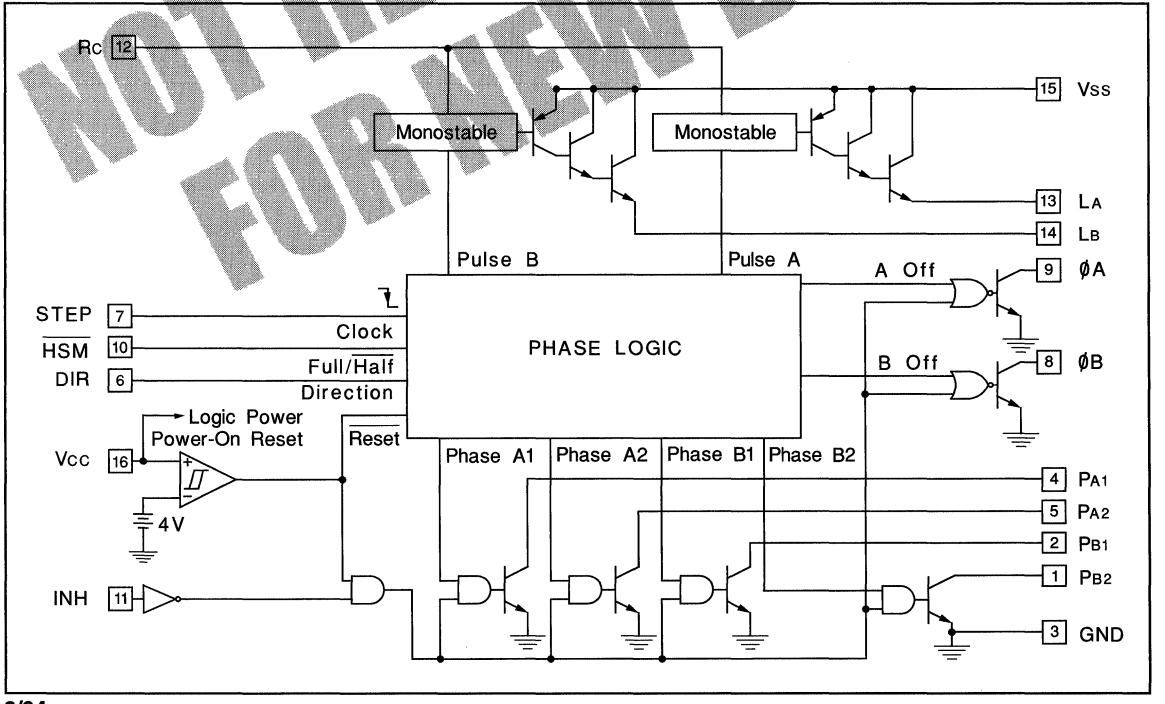
The UC3517 contains four NPN drivers that operate in two-phase fashion for full-step and half-step motor control. The UC3517 also contains two emitter followers, two monostables, phase decoder logic, power-on reset, and low-voltage protection, making it a versatile system for driving small stepper motors or for controlling large power devices.

The emitter followers and monostables in the UC3517 are configured to apply higher-voltage pulses to the motor at each step command. This drive technique, called "Bilevel," allows faster stepping than common resistive current limiting, yet generates less electrical noise than chopping techniques.

ABSOLUTE MAXIMUM RATINGS

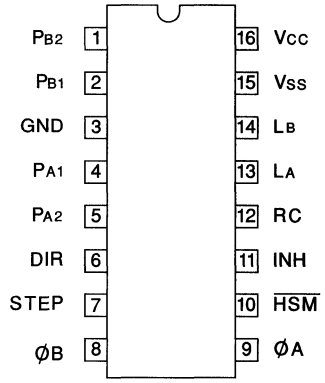
Second Level Supply, V_{SS}	40V
Phase Output Supply, V_{MM}	40V
Logic Supply, V_{CC}	7V
Logic Input Voltage	–.3V to +7V
Logic Input Current	±10mA
Output Current, Each Phase	500mA
Output Current, Emitter Follower	–500mA
Junction Temperature	150°C
Ambient Temperature, UC1517	–55°C to +125°C
Ambient Temperature, UC3517	0°C to +70°C
Storage Temperature	–55°C to +150°C

BLOCK DIAGRAM

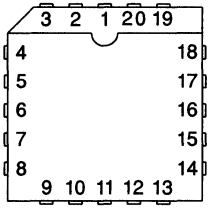


CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20, LCC-20
(TOP VIEW)
Q & L PACKAGE



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
PB2	2
PB1	3
GND	4
PA1	5
N/C	6
PA2	7
DIR	8
STEP	9
ØB	10
N/C	11
ØA	12
HSM	13
INH	14
RC	15
N/C	16
LA	17
LB	18
VSS	19
VCC	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1517 and 0°C to +70°C for the UC3517, V_{CC}=5V, V_{SS} = 20V, T_A=T_J. Pin numbers refer to DIL-16 package.

PARAMETER	TEST CONDITIONS	UC1517 / UC3517			UNITS
		MIN	TYP	MAX	
Logic Supply, V_{CC}	Pin 16	4.75		5.25	V
Second Supply, V_{SS}	Pin 15	10		40	V
Logic Supply Current	V_{INH} = 0.4V		45	60	mA
	V_{INH} = 4.0V		12		mA
Input Low Voltage	Pins 6, 7, 10, 11			0.8	V
Input High Voltage	Pins 6, 7, 10, 11	2.0			V
Input Low Current	Pins 6, 7, 10, 11; V = 0V	-400			µA
Input High Current	Pins 6, 7, 10, 11; V = 5V			20	µA
Phase Output Saturation Voltage	Pins 1, 2, 4, 5; I = 350mA		0.6	0.85	V
Phase Output Leakage Current	Pins 1, 2, 4, 5; V = 39V			500	µA
Follower Saturation Voltage to V_{SS}	Pins 13,14; I = 350mA			-2	V
Follower Leakage Current	Pins 13,14; V = 0V			500	µA
Output Low Voltage, ØA, ØB	Pins 8, 9; I = 1.6mA		0.1	0.4	V
Phase Turn-On Time	Pins 1, 2, 4, 5		2		µs
Phase Turn-Off Time	Pins 1, 2, 4, 5		1.8		µs
Second-Level On Time. T_{MONO}	Pins 13,14; Figure 3 Test Circuit	275	325	375	µs
Logic Input Set-up Time, t_S	Pins 6, 10; Figure 4	400			ns
Logic Input Hold Time, t_h	Pins 6, 10; Figure 4	0			ns
STEP Pulse Width, t_P	Pin 7; Figure 4	800			ns
Timing Resistor Value	Pin 12	1k		100k	Ω
Timing Capacitor Value	Pin 12	0.1		500	nF
Power-On Threshold	Pin 16		4.3		V
Power-Off Threshold	Pin 16		3.8		V
Power Hysteresis	Pin 16		0.5		V

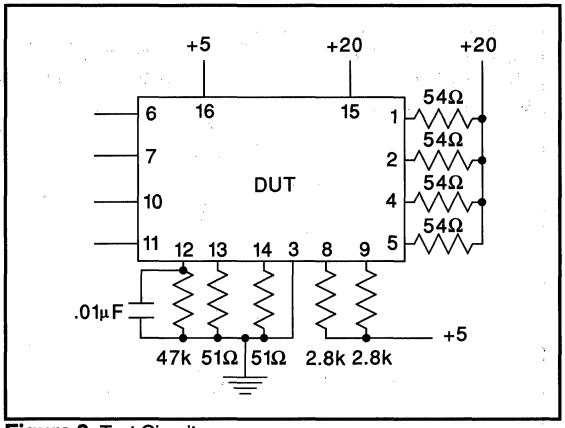


Figure 3. Test Circuit

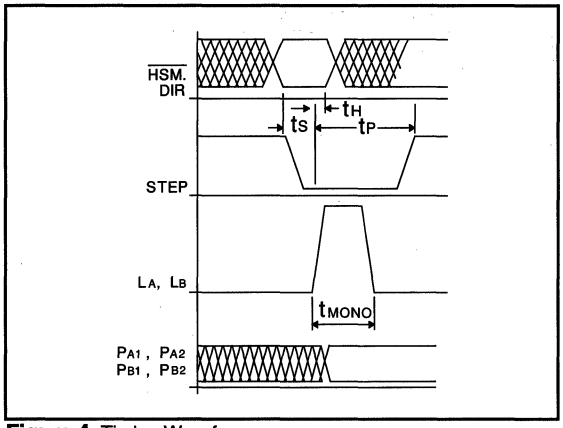


Figure 4. Timing Waveforms

PIN DESCRIPTION

VCC: VCC is the UC3517's logic supply. Connect to a regulated 5VDC, and bypass with a 0.1μF ceramic capacitor to absorb switching transients.

VMM: VMM is the primary motor supply. It connects to the UC3517 phase outputs through the motor windings. Limit this supply to less than 40V to prevent breakdown of the phase output transistors. Select the nominal VMM voltage for the desired continuous winding current.

VSS: VSS is the secondary motor supply. It drives the LA and LB outputs of the UC3517 when a monostable in the UC3517 is active. In the bilevel application, this supply is applied to the motor to charge the winding inductance faster than the primary supply could. Typically, Vss is higher in voltage than VMM, although VSS must be less than 40V. The VSS supply should have good transient capability.

GROUND: The ground pin is the common reference for all supplies, inputs and outputs.

RC: RC controls the timing functions of the monostables in the UC3517. It is normally connected to a resistor (RT) and a capacitor (CT) to ground, as shown in Figure 3. Monostable on time is determined by the formula TON ≈ 0.69 RT CT. To keep the monostable on indefinitely, pull RC to VCC through a 50k resistor. The UC3517 contains only one RC pin for two monostables. If step rates comparable to TON are commanded, incorrect pulsing can result, so consider maximum step rates when selecting RT and CT. Keep TON ≤ T STEP MAX.

ØA and ØB: These logic outputs indicate half-step position. These outputs are open-collector, low-current drivers, and may directly drive TTL logic. They can also drive CMOS logic if a pull-up resistor is provided. Systems which use the UC3517 as an encoder and use a different driver can use these outputs to disable the external driver, as shown in Figure 8. The sequencing of these outputs is shown in Figure 5.

PA1, PA2, PB1, and PB2: The phase outputs pull to ground sequentially to cause motor stepping, according to the state diagram of Figure 5. The sequence of stepping on these lines, as well as with the LA and LB lines is controlled by STEP input, the DIR input, and the $\overline{\text{HSM}}$ input. Caution: If these outputs or any other IC pins are pulled too far below ground either continuously or in a transient, step memory can be lost. It is recommended that these pins be clamped to ground and supply with high-speed diodes when driving inductive loads such as motor windings or solenoids. This clamping is very important because one side of the winding can "kick" in a direction opposite the swing of the other side.

LA and LB: These outputs pull to VSS when their corresponding monostable is active, and will remain high until the monostable time elapses. Before and after, these outputs are high-impedance. For detail timing information, consult Figure 5.

STEP: This logic input clocks the logic in the UC3517 on every falling edge. Like all other UC3517 inputs, this input is TTL/CMOS compatible, and should not be pulled below ground.

DIR: This logic input controls the motor rotation direction by controlling the phase output sequence as shown in Figure 5. This signal must be stable 400ns before a falling edge on STEP, and must remain stable through the edge to insure correct stepping.

$\overline{\text{HSM}}$: This logic input switches the UC3517 between half-stepping ($\overline{\text{HSM}}$ = low) and full-stepping ($\overline{\text{HSM}}$ = high) by controlling the phase output sequence as show in Figure 5. This line requires the same set-up time as the DIR input, and has the same hold requirement.

INH: When the inhibit input is high, the phase and θ outputs are inhibited (high impedance). STEP pulses received while inhibited will continue to update logic in the IC, but the states will not be reflected at the outputs until inhibit is pulled low. In stepper motor systems, this can be used to save power or to allow the rotor to move freely for manual repositioning.

OPERATING MODES

The UC3517 is a system component capable of many different operating modes, including:

Unipolar Stepper Driver: In its simplest form, the UC3517 can be connected to a stepper motor as a unipolar driver. L_A, L_B, RC and Vss are not used, and may be left open. All other system design considerations mentioned above apply, including choice of motor supply VMM, undershoot diodes and timing considerations.

Unipolar Bilevel Stepper Driver: If increased step rates are desired, the application circuit of Figure 6 makes use of the monostables and emitter followers as well as the configuration mentioned above to provide high-voltage pulses to the motor windings when the phase is turned on. For a given dissipation level, this mode offers faster step rates, and very little additional electrical noise.

The choice of monostable components can be estimated based on the timing relationship of motor current and voltage: V = Ldl/dt. Assuming a fixed secondary supply voltage (V_{SS}), a fixed winding inductance (L_M), a desired winding peak current (I_W), and no back EMF from the motor, we can estimate that $R_TC_T = 1.449\ I_W L_M/V_{SS}$. In practice, these calculations should be confirmed and adjusted to accommodate for effects not modeled.

Voltage-Doubled Mode: The UC3517 can also be used to generate higher voltages than available with the system power supplies using capacitors and diodes. Figure 9 shows how this might be done, and gives some estimates for the component values.

Higher Current Operation: For systems requiring more than 350mA of drive per phase, the UC3717A can be used in conjunction with discrete power transistors or power driver ICs, like the L298. These can be connected as current gain devices that turn on when the phase outputs turn on.

Bipolar Motor Drive: Bipolar motors can be controlled by the UC3517 with the addition of bipolar integrated drivers such as the UC3717A (Figure 8) and the L298, or discrete devices. Care should be taken with discrete devices to avoid potential cross-conduction problems.

LOGIC FLOW GRAPH

The UC3517 contains a bidirectional counter which is decoded to generate the correct phase and Ø outputs. This counter is incremented on every falling edge of the STEP input. Figure 5 shows a graph representing the counter sequence, inputs that determine the next state (DIR and HSM), and the outputs at each state. Each circle represents a unique logic state, and the four inside circles represent the half-step states.

The four bits inside the circles represent the phase outputs in each state (P_{A1}, P_{A2}, P_{B1}, and P_{B2}). For example, the circle labeled 1010 is immediately entered when the device is powered up, and represents P_{A1} off ("1" or high), P_{A2} on ("0" or low), P_{B1} off ("1" or high) and P_{B2} on ("0" or low). The $Ø_A$ and $Ø_B$ outputs are both low (unidentified).

The arrows in the graph show the state changes. For example, if the IC is in state 0110, DIR is high, $\overline{HSM}$ is high, and STEP falls, the next state will be 0101, and a pulse will be generated on the L_B line by the monostable.

Inhibit will not effect the logic state, but it will cause all phase outputs and both Ø outputs to go high (off). A falling edge on STEP will still cause a state change, but inhibit will have to toggle low for the state to be apparent.

A falling edge on STEP with $\overline{HSM}$ high will cause the counter to advance to the next full step state regardless of whether or not it was in a full step state previously.

No L_A or L_B pulses are generated entering half-states.

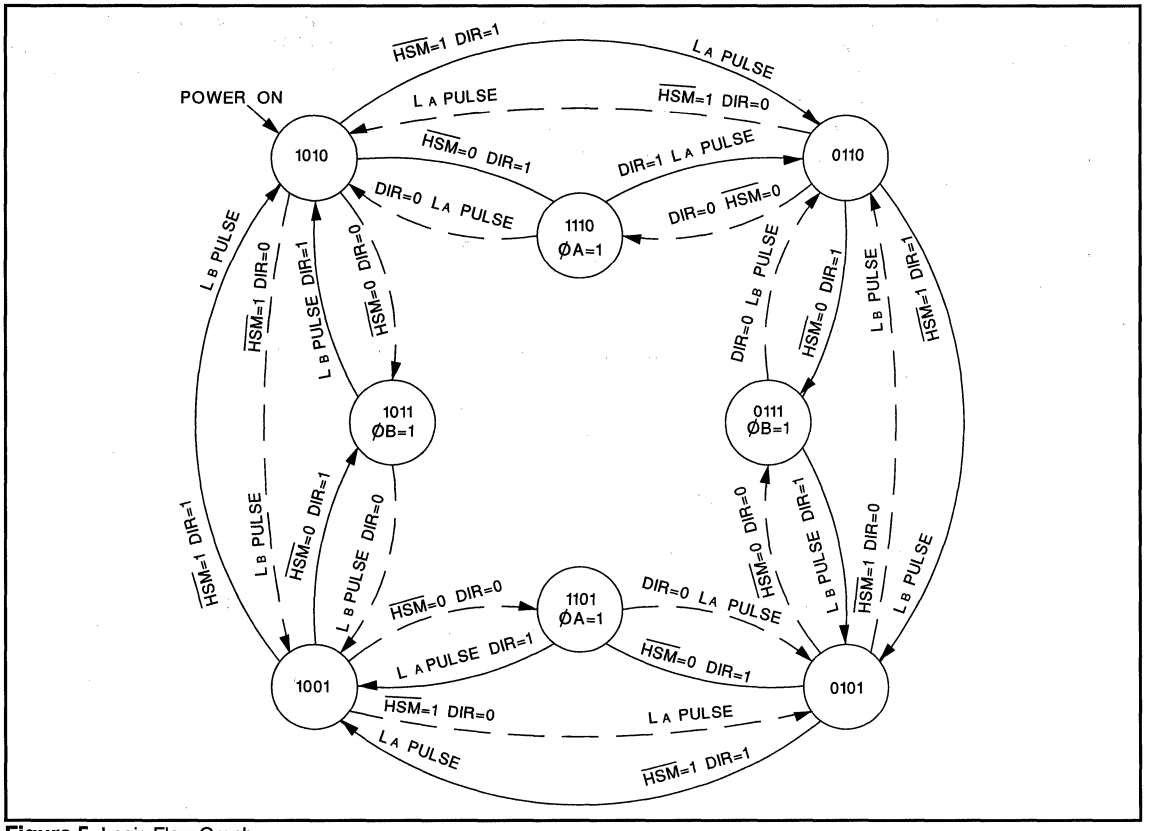
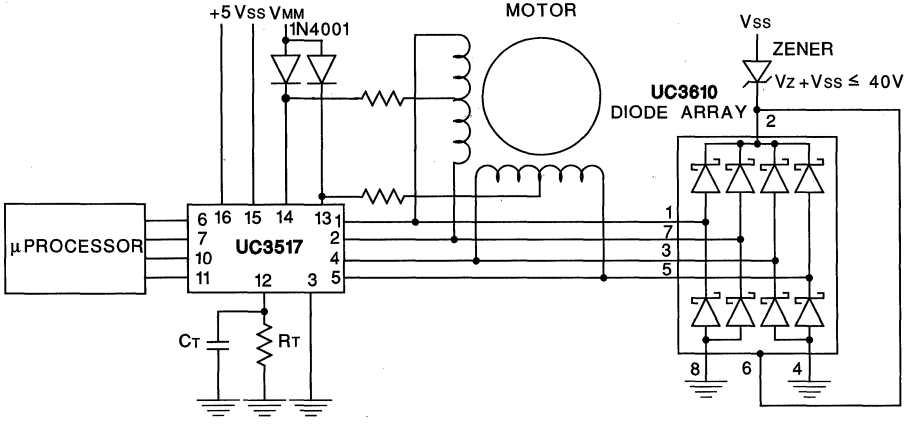
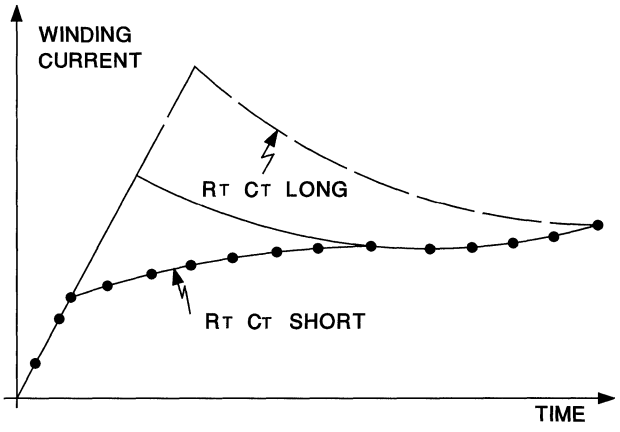


Figure 5. Logic Flow Graph



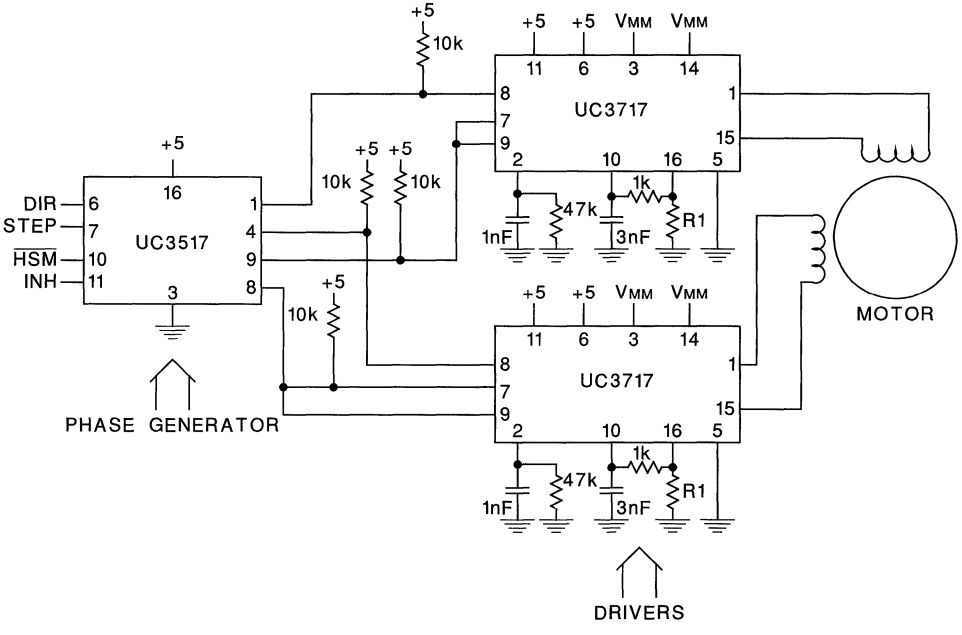
For applications requiring very fast step rates, a zener diode permits windings to discharge at higher voltages, and higher rates. Driver transistor breakdown must be considered when selecting Vss and zener voltage to insure that the outputs will not overshoot past 40V. If the zener diodes are not used and UC3610 pin 2 is connected directly to Vss then higher Vss can be used.

Figure 6. Bilevel Motor Driver



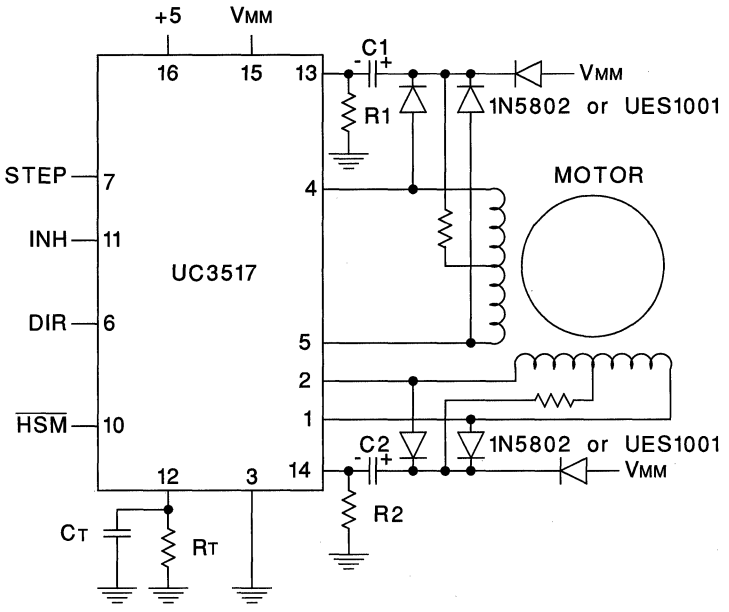
Experimental selection of RT and CT allow the designer to select a small amount of winding current overshoot, as shown above. Although the overshoot may exceed the continuous rated current of the winding and the drive transistors, the duration can be well controlled. Average power dissipation for the driver and motor must be considered when designing systems with intentional overshoot, and must stay within conservative limits for short duty cycles.

Figure 7. Effects of Different RT & CT on Bilevel Systems



In this application, the ∅A and ∅B outputs of the UC3517 are connected to the current program inputs of the UC3717. This allows the UC3517 inhibit signal to inhibit the UC3717, and also allows half-step operation of the UC3717. Peak motor winding current will be limited to approximately .42V/R1 by chopping.

Figure 8. Interface to UC3717 Bipolar Driver



Although component values can be best optimized experimentally, good starting values speed development. For this design, start with:

$R_T C_T = 3 L_W/R_W$

$C_1 = C_2 = L_W I_R/R_W$

$R_1 = R_2 = 2.9 T_{MIN}/C_1$

where:

L_W is winding inductance,
R_W is winding resistance,
I_R is rated winding current, and
T_{MIN} is minimum step period expected.

Figure 9. Using the UC3517 as a Voltage Doubler

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TEL. (603) 424-2410 • FAX (603) 424-3460

Brushless DC Motor Controller

FEATURES

- Drives Power MOSFETs or Power Darlingtons Directly
- 50V Open Collector High-Side Drivers
- Latched Soft Start
- High-speed Current-Sense Amplifier with Ideal Diode
- Pulse-by-Pulse and Average Current Sensing
- Over-Voltage and Under-Voltage Protection
- Direction Latch for Safe Direction Reversal
- Tachometer
- Trimmed Reference Sources 30mA
- Programmable Cross-Conduction Protection
- Two-Quadrant and Four-Quadrant Operation

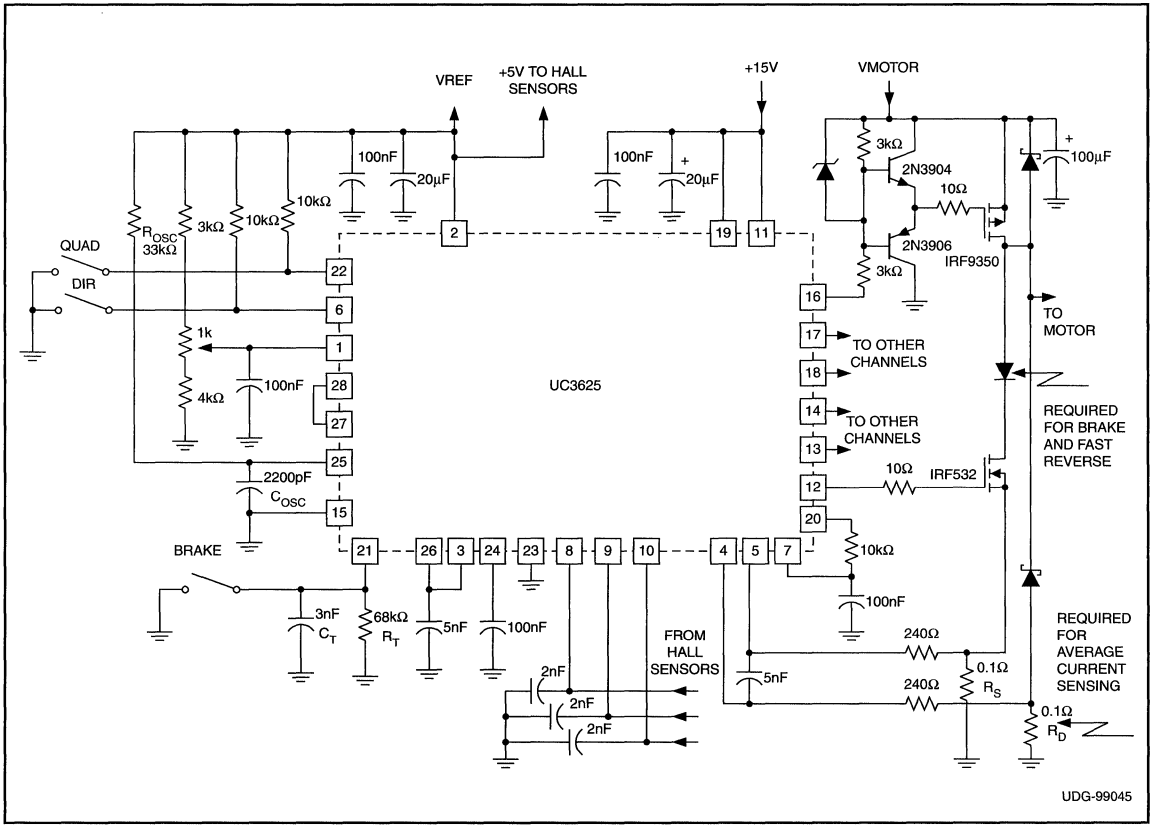
DESCRIPTION

The UC3625 family of motor controller ICs integrate most of the functions required for high-performance brushless DC motor control into one package. When coupled with external power MOSFETs or Darlingtons, these ICs perform fixed-frequency PWM motor control in either voltage or current mode while implementing closed loop speed control and braking with smart noise rejection, safe direction reversal, and cross–conduction protection.

Although specified for operation from power supplies between 10V and 18V, the UC1625 can control higher voltage power devices with external level-shifting components. The UC1625 contains fast, high-current push-pull drivers for low-side power devices and 50V open-collector outputs for high-side power devices or level shifting circuitry.

The UC1625 is characterized for operation over the military temperature range of –55° C to +125° C, while the UC2625 is characterized from –40° C to +105° C and the UC3625 is characterized from 0° C to 70° C. *(NOTE: ESD Protection to 2kV)*

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

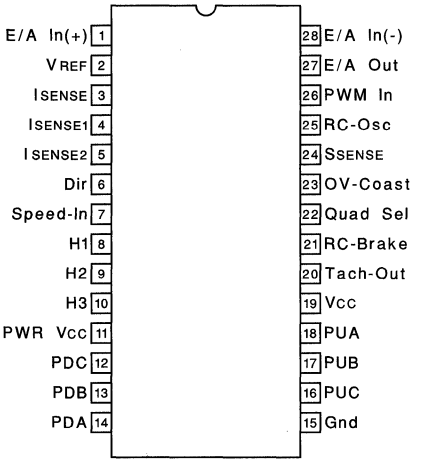
V_{CC} Supply Voltage . . . . . +20V
Pwr V_{CC} Supply Voltage . . . . . +20V
PWM In . . . . . –0.3 to 6V
E/A IN(+), E/A IN(–) . . . . . –0.3 to 12V
I_{SENSE1}, I_{SENSE2} . . . . . –1.3 to 6V
OV–Coast, Dir, Speed-In, S_{START}, Quad Sel . . . . . –0.3 to 8V
H1, H2, H3 . . . . . –0.3 to 12V
PU Output Voltage . . . . . –0.3 to 50V
PU Output Current . . . . . +200 mA continuous
PD Output Current . . . . . ±200 mA continuous
E/A Output Current . . . . . ±10 mA
I_{SENSE} Output Current . . . . . –10 mA
Tach Out Output Current . . . . . ±10 mA
V_{REF} Output Current . . . . . –50 mA continuous
Operating Temperature Range UC1625 . . . . . –55°C to 125°C
Operating Temperature Range UC2625 . . . . . –40°C to 105°C
Operating Temperature Range UC3625 . . . . . 0°C to 70°C

Note 1: *Currents are positive into and negative out of the specified terminal.*

Note 2: *Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.*

CONNECTION DIAGRAM

DIL-28 (TOP VIEW)
J or N PACKAGE



Note 3: *This pinout applies to the SOIC (DW), PLCC (Q), and LCC (L) packages (ie. pin 22 has the same function on all packages.)*

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for: T_A = 25° C; Pwr V_{CC} = V_{CC} = 12V; R_{OSC} = 20k to V_{REF}; C_{OSC} = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply current	Over Operating Range		14.5	30.0	mA
V_{CC} Turn-On Threshold	Over Operating Range	8.65	8.95	9.45	V
V_{CC} Turn-Off Threshold	Over Operating Range	7.75	8.05	8.55	V
Overvoltage/Coast					
OV-Coast Inhibit Threshold	Over Operating Range	1.65	1.75	1.85	V
OV-Coast Restart Threshold		1.55	1.65	1.75	V
OV-Coast Hysteresis		0.05	0.10	0.15	V
OV-Coast Input Current		–10	–1	0	µA
Logic Inputs					
H1, H2, H3 Low Threshold	Over Operating Range	0.8	1.0	1.2	V
H1, H2, H3 High Threshold	Over Operating Range	1.6	1.9	2.0	V
H1, H2, H3 Input Current	Over Operating Range, to 0V	-400	-250	–120	µA
Quad Sel, Dir Thresholds	Over Operating Range	0.8	1.4	2.0	V
Quad Sel Hysteresis			70		mV
Dir Hysteresis			0.6		V
Quad Sel Input Current		–30	50	150	µA
Dir Input Current		–30	–1	30	µA
PWM Amp/Comparator					
E/A In(+), E/A In(–) Input Current	To 2.5V	–5.0	–0.1	5.0	µA
PWM In Input Current	To 2.5V	0	3	30	µA
Error Amp Input Offset	0V < $V_{COMMON-MODE}$ < 3V	–10		10	mV
Error Amp Voltage Gain		70	90		dB

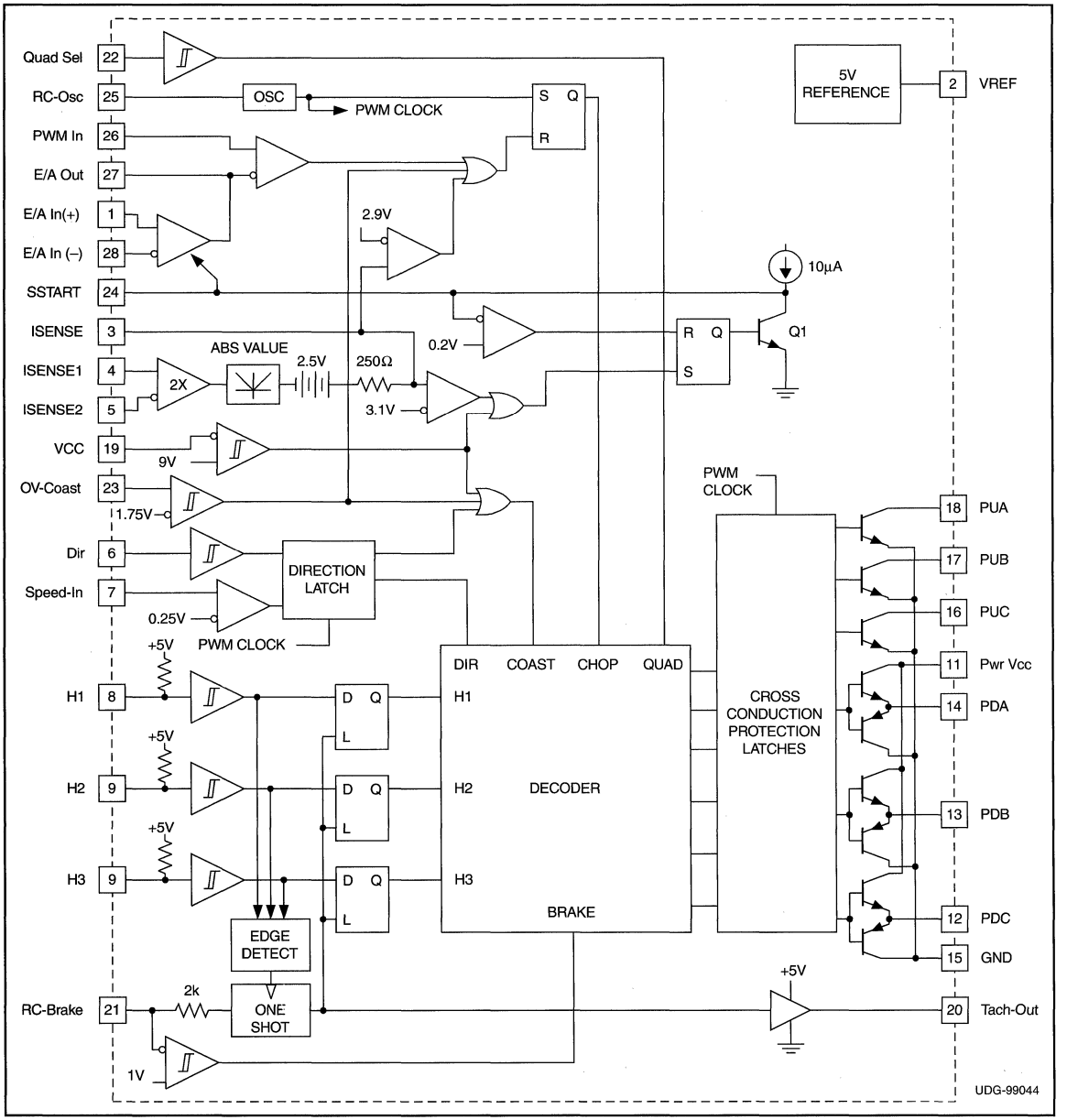
ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for: T_A = 25° C; Pwr V_{CC} = V_{CC} = 12V; R_{OSC} = 20k to V_{REF}; C_{OSC} = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Amp/Comparator (cont.)					
E/A Out Range		0.25		3.50	V
S_{START} Pull-up Current	To 0V	–16	–10	–5	µA
S_{START} Discharge Current	To 2.5V	0.1	0.4	3.0	mA
S_{START} Restart Threshold		0.1	0.2	0.3	V
Current Amp					
Gain	I_{SENSE1} = .3V, I_{SENSE2} = .5V to .7V	1.75	1.95	2.15	V/V
Level Shift	I_{SENSE1} = .3V, I_{SENSE2} = .3V	2.4	2.5	2.65	V
Peak Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.14	0.20	0.26	V
Over Current Threshold	I_{SENSE1} = 0V, Force I_{SENSE2}	0.26	0.30	0.36	V
I_{SENSE1}, I_{SENSE2} Input Current	To 0V	–850	–320	0	µA
I_{SENSE1}, I_{SENSE2} Offset Current	To 0V		±2	±12	µA
Range I_{SENSE1}, I_{SENSE2}		–1		2	V
Tachometer/Brake					
Tach-Out High Level	Over Operating Range, 10k to 2.5V	4.7	5	5.3	V
Tach-Out Low Level	Over Operating Range, 10k to 2.5V			0.2	V
On Time		170	220	280	µs
On Time Change With Temp	Over Operating Range		0.1		%
RC-Brake Input Current	To 0V	–4.0	–1.9		mA
Threshold to Brake, RC-Brake	Over Operating Range	0.8	1.0	1.2	V
Brake Hysteresis, RC-Brake			0.09		V
Speed-In Threshold	Over Operating Range	220	257	290	mV
Speed-In Input Current		–30	–5	30	µA
Low-Side Drivers					
Voh, –1mA, Down From V_{CC}	Over Operating Range		1.60	2.1	
V Voh, –50mA, Down From V_{CC}	Over Operating Range		1.75	2.2	V
Vol, 1mA	Over Operating Range		0.05	0.4	V
Vol, 50mA	Over Operating Range		0.36	0.8	V
Rise/Fall Time	10% to 90% Slew Time, into 1nF		50		ns
High-Side Drivers					
Vol, 1mA	Over Operating Range		0.1	0.4	V
Vol, 50mA	Over Operating Range		1.0	1.8	V
Leakage Current	Output Voltage = 50V			25	µA
Fall Time	10% to 90% Slew Time, 50mA Load		50		ns
Oscillator					
Frequency		40	50	60	kHz
Frequency	Over Operating Range	35		65	kHz
Reference					
Output Voltage		4.9	5.0	5.1	V
Output Voltage	Over Operating Range	4.7	5.0	5.3	V
Load Regulation	0mA to –20mA Load	–40	–5		mV
Line Regulation	10V to 18V V_{CC}	–10	–1	10	mV
Short Circuit Current	Over Operating Range	50	100	150	mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for: T_A = 25°C; Pwr V_{CC} = V_{CC} = 12V; R_{OSC} = 20k to V_{REF}; C_{OSC} = 2nF; R_{TACH} = 33k; C_{TACH} = 10nF; and all outputs unloaded. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Miscellaneous					
Output Turn-On Delay			1		µs
Output Turn-Off Delay			1		µs

BLOCK DIAGRAM



PIN DESCRIPTIONS

Dir, Speed-In: The position decoder logic translates the Hall signals and the Dir signal to the correct driver signals (PUs and PDs). To prevent output stage damage, the signal on Dir is first loaded into a direction latch, then shifted through a two-bit register.

As long as Speed-In is less than 250mV, the direction latch is transparent. When Speed-In is higher than 250mV, the direction latch inhibits all changes in direction. Speed-In can be connected to Tach-Out through a filter, so that the direction latch is only transparent when the motor is spinning slowly, and has too little stored energy to damage power devices.

Additional circuitry detects when the input and output of the direction latch are different, or when the input and output of the shift register are different, and inhibits all output drives during that time. This can be used to allow the motor to coast to a safe speed before reversing.

The shift register guarantees that direction can't be changed instantaneously. The register is clocked by the PWM oscillator, so the delay between direction changes is always going to be between one and two oscillator periods. At 40kHz, this corresponds to a delay of between 25µs and 50µs. Regardless of output stage, 25µs dead time should be adequate to guarantee no overlap cross-conduction. Toggling DIR will cause an output pulse on Tach-Out regardless of motor speed.

E/A In(+), E/A In(–), E/A Out, PWM In: E/A In(+) and E/A In(–) are not internally committed to allow for a wide variety of uses. They can be connected to the I_{SENSE}, to Tach-Out through a filter, to an external command voltage, to a D/A converter for computer control, or to another op amp for more elegant feedback loops. The error amplifier is compensated for unity gain stability, so E/A Out can be tied to E/A In(–) for feedback and major loop compensation.

E/A Out and PWM In drive the PWM comparator. For voltage-mode PWM systems, PWM In can be connected to RC-Osc. The PWM comparator clears the PWM latch, commanding the outputs to chop.

The error amplifier can be biased off by connecting E/A In(–) to a higher voltage than E/A In(+). When biased off, E/A Out will appear to the application as a resistor to ground. E/A Out can then be driven by an external amplifier.

GND: All thresholds and outputs are referred to the GND pin except for the PD and PU outputs.

H1, H2, H3: The three shaft-position sensor inputs consist of hysteresis comparators with input pull-up resistors. Logic thresholds meet TTL specifications and can be driven by 5V CMOS, 12V CMOS, NMOS, or open-collectors.

Connect these inputs to motor shaft position sensors that are positioned 120 electrical degrees apart. If noisy signals are expected, zener clamp and filter these inputs with 6V zeners and an RC filter. Suggested filtering components are 1kΩ and 2nF. Edge skew in the filter is not a problem, because sensors normally generate modified Gray code with only one output changing at a time, but rise and fall times must be shorter than 20µs for correct tachometer operation.

Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals is inverted.

I_{SENSE1}, I_{SENSE2}, I_{SENSE}: The current sense amplifier has a fixed gain of approximately two. It also has a built-in level shift of approximately 2.5V. The signal appearing on I_{SENSE} is:

$$I_{SENSE} = 2.5V + \left(2 \bullet ABS\left(I_{SENSE1} - I_{SENSE2}\right)\right)$$

I_{SENSE1} and I_{SENSE2} are interchangeable and can be used as differential inputs. The differential signal applied can be as high as ±0.5V before saturation.

If spikes are expected on I_{SENSE1} or I_{SENSE2}, they are best filtered by a capacitor from I_{SENSE} to ground. Filtering this way allows fast signal inversions to be correctly processed by the absolute value circuit. The peak-current comparator allows the PWM to enter a current-limit mode with current in the windings never exceeding approximately $0.2V/R_{SENSE}$. The over current comparator provides a fail-safe shutdown in the unlikely case of current exceeding $0.3V/R_{SENSE}$. Then, soft start is commanded, and all outputs are turned off until the high current condition is removed. It is often essential to use some filter driving I_{SENSE1} and I_{SENSE2} to reject extreme spikes and to control slew rate. Reasonable starting values for filter components might be 250Ω series resistors and a 5nF capacitor between I_{SENSE1} and I_{SENSE2}. Input resistors should be kept small and matched to maintain gain accuracy.

OV-Coast: This input can be used as an over-voltage shutdown in put, as a coast input, or both. This input can be driven by TTL, 5V CMOS, or 12V CMOS.

PIN DESCRIPTIONS (cont.)

PDA, PDB, PDC: These outputs can drive the gates of N-Channel power MOSFETs directly or they can drive the bases of power Darlingtons if some form of current limiting is used. They are meant to drive low-side power devices in high-current output stages. Current available from these pins can peak as high as 0.5A. These outputs feature a true totem-pole output stage. Beware of exceeding IC power dissipation limits when using these outputs for high continuous currents. These outputs pull high to turn a "low-side" device on (active high).

PUA, PUB, PUC: These outputs are open-collector, high-voltage drivers that are meant to drive high-side power devices in high-current output stages. These are active low outputs, meaning that these outputs pull low to command a high-side device on. These outputs can drive low-voltage PNP Darlingtons and P-channel MOSFETs directly, and can drive any high-voltage device using external charge-pump techniques, transformer signal coupling, cascode level-shift transistors, or opto-isolated drive (high-speed opto devices are recommended). (See applications).

PWR V_{CC}: This supply pin carries the current sourced by the PD outputs. When connecting PD outputs directly to the bases of power Darlingtons, the PWR V_{CC} pin can be current limited with a resistor. Darlington outputs can also be "Baker Clamped" with diodes from collectors back to PWR V_{CC}. (See Applications)

Quad Sel: The IC can chop power devices in either of two modes, referred to as "two-quadrant" (Quad Sel low) and "four-quadrant" (Quad Sel high). When two-quadrant chopping, the pull-down power devices are chopped by the output of the PWM latch while the pull-up drivers remain on. The load will chop into one commutation diode, and except for back-EMF, will exhibit slow discharge current and faster charge current. Two-quadrant chopping can be more efficient than four-quadrant.

When four-quadrant chopping, all power drivers are chopped by the PWM latch, causing the load current to flow into two diodes during chopping. This mode exhibits better control of load current when current is low, and is preferred in servo systems for equal control over acceleration and deceleration. The Quad Sel input has no effect on operation during braking.

RC-Brake: Each time the Tach-Out pulses, the capacitor tied to RC-Brake discharges from approximately 3.33V down to 1.67V through a resistor. The tachometer pulse width is approximately $T = 0.67\ R_T\ C_T$, where R_T and C_T are a resistor and capacitor from RC-Brake to ground. Recommended values for R_T are 10kΩ to 500kΩ, and recommended values for C_T are 1nF to 100nF, allowing times between 5µs and 10ms. Best accuracy and stability are achieved with values in the centers of those ranges.

RC-Brake also has another function. If RC-Brake pin is pulled below the brake threshold, the IC will enter brake mode. This mode consists of turning off all three high-side devices, enabling all three low-side devices, and disabling the tachometer. The only things that inhibit low-side device operation in braking are low-supply, exceeding peak current, OV-Coast command, and the PWM comparator signal. The last of these means that if current sense is implemented such that the signal in the current sense amplifier is proportional to braking current, the low-side devices will brake the motor with current control. (See applications) Simpler current sense connections will result in uncontrolled braking and potential damage to the power devices.

RC-Osc: The UC3625 can regulate motor current using fixed-frequency pulse width modulation (PWM). The RC-Osc pin sets oscillator frequency by means of timing resistor R_{OSC} from the RC-Osc pin to V_{REF} and capacitor C_{OSC} from RC-Osc to Gnd. Resistors 10kΩ to 100kΩ and capacitors 1nF to 100nF will work best, but frequency should always be below 500kHz. Oscillator frequency is approximately:

$$F = \frac{2}{(R_{OSC} \bullet C_{OSC})}$$

Additional components can be added to this device to cause it to operate as a fixed off-time PWM rather than a fixed frequency PWM, using the RC-Osc pin to select the monostable time constant.

The voltage on the RC-Osc pin is normally a ramp of about 1.2V peak-to-peak, centered at approximately 1.6V. This ramp can be used for voltage-mode PWM control, or can be used for slope compensation in current-mode control.

S_{START}: Any time that V_{CC} drops below threshold or the sensed current exceeds the over-current threshold, the soft-start latch is set. When set, it turns on a transistor that pulls down on S_{START}. Normally, a capacitor is connected to this pin, and the transistor will completely discharge the capacitor. A comparator senses when the NPN transistor has completely discharged the capacitor, and allows the soft-start latch to clear when the fault is removed. When the fault is removed, the soft-start capacitor will charge from the on-chip current source.

PIN DESCRIPTIONS (cont.)

S_{START} clamps the output of the error amplifier, not allowing the error amplifier output voltage to exceed S_{START} regardless of input. The ramp on RC-Osc can be applied to PWM In and compared to E/A Out. With S_{START} discharged below 0.2V and the ramp minimum being approximately 1.0V, the PWM comparator will keep the PWM latch cleared and the outputs off. As S_{START} rises, the PWM comparator will begin to duty-cycle modulate the PWM latch until the error amplifier inputs overcome the clamp. This provides for a safe and orderly motor start-up from an off or fault condition.

Tach-Out: Any change in the H1, H2, or H3 inputs loads data from these inputs into the position sensor latches. At the same time data is loaded, a fixed-width 5V pulse is triggered on Tach-Out. The average value of the voltage on Tach-Out is directly proportional to speed, so this output can be used as a true tachometer for speed feedback with an external filter or averaging circuit which usually consists of a resistor and capacitor.

Whenever Tach-Out is high, the position latches are inhibited, such that during the noisiest part of the commutation cycle, additional commutations are not possible. Although this will effectively set a maximum rotational speed, the maximum speed can be set above the highest expected speed, preventing false commutation and chatter.

V_{CC}: This device operates with supplies between 10V and 18V. Under-voltage lockout keeps all outputs off below 7.5V, insuring that the output transistors never turn on until full drive capability is available. Bypass V_{CC} to ground with an 0.1µF ceramic capacitor. Using a 10µF electrolytic bypass capacitor as well can be beneficial in applications with high supply impedance.

V_{REF}: This pin provides regulated 5 volts for driving Hall-effect devices and speed control circuitry. V_{REF} will reach +5V before V_{CC} enables, ensuring that Hall-effect devices powered from V_{REF} will become active before the UC3625 drives any output. Although V_{REF} is current limited, operation over 30mA is not advised. For proper performance V_{REF} should be bypassed with at least a 0.1µF capacitor to ground.

APPLICATION INFORMATION

Cross Conduction Prevention

The UC3625 inserts delays to prevent cross conduction due to overlapping drive signals. However, some thought must always be given to cross conduction in output stage design because no amount of dead time can prevent fast slewing signals from coupling drive to a power device through a parasitic capacitance.

The UC3625 contains input latches that serve as noise blanking filters. These latches remain transparent through any phase of a motor rotation and latch immediately after an input transition is detected. They remain latched for two cycles of the PWM oscillator. At a PWM oscillator speed of 20kHz, this corresponds to 50µs to 100µs of blank time which limits maximum rotational speed to 100kRPM for a motor with six transitions per rotation or 50kRPM for a motor with 12 transitions per rotation.

This prevents noise generated in the first 50µs of a transition from propagating to the output transistors and causing cross–conduction or chatter.

The UC3625 also contains six flip flops corresponding to the six output drive signals. One of these flip flops is set every time that an output drive signal is turned on, and cleared two PWM oscillator cycles after that drive signal is turned off. The output of each flip flop is used to inhibit drive to the opposing output (see below). In this way, it is impossible to turn on driver PUA and PDA at the same time. It is also impossible for one of these drivers to turn on without the other driver having been off for at least two PWM oscillator clocks.

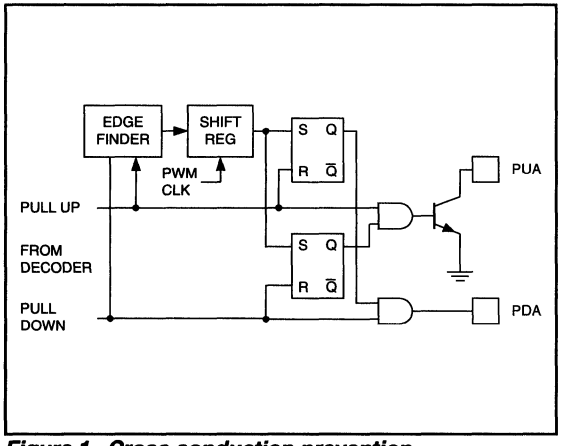


Figure 1. Cross conduction prevention.

TYPICAL CHARACTERISTICS

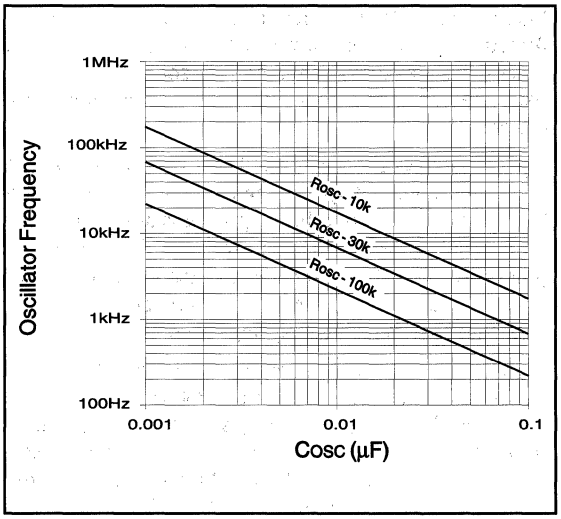


Figure 2. Oscillator frequency vs. C_{OSC} and R_{OSC}.

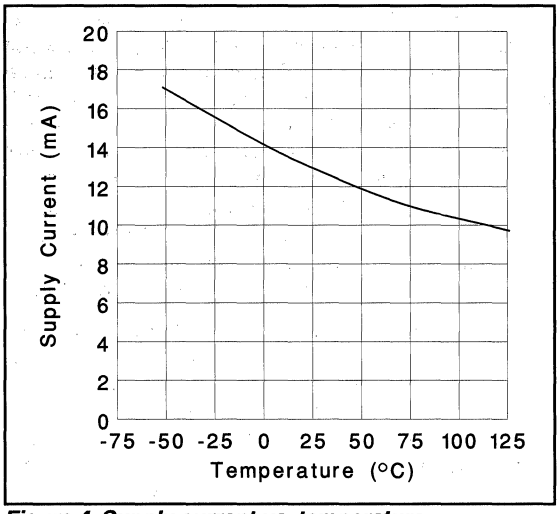


Figure 4. Supply current vs. temperature.

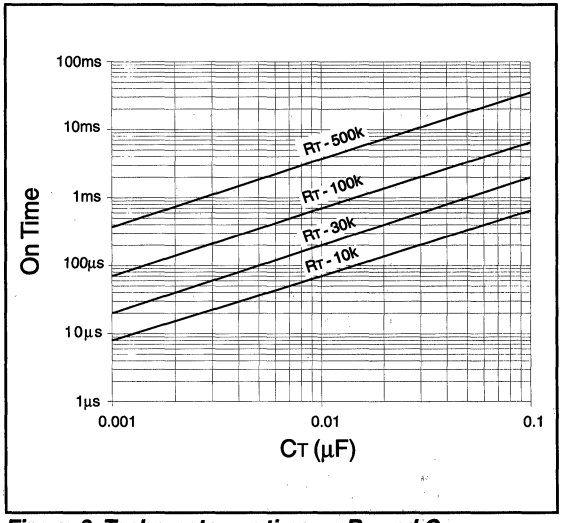


Figure 3. Tachometer on time vs R_T and C_T.

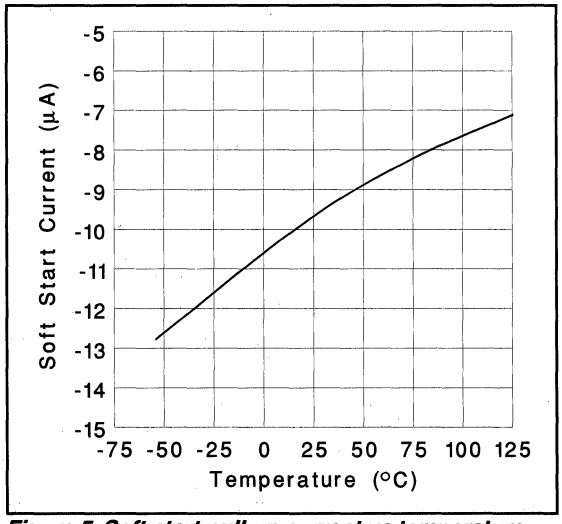


Figure 5. Soft start pull-up current vs temperature.

TYPICAL CHARACTERISTICS (cont.)

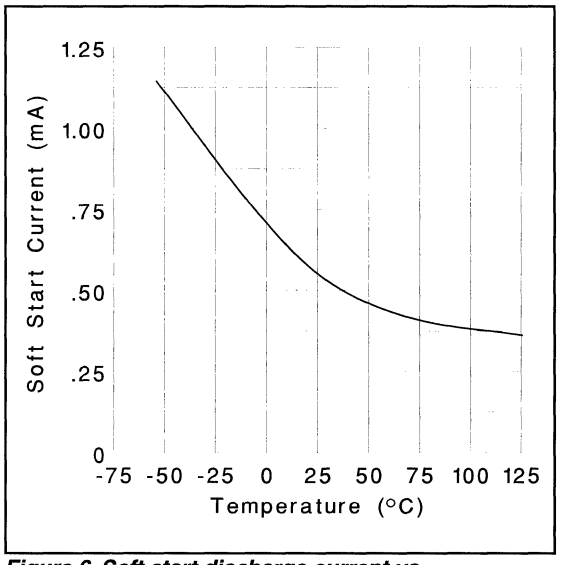


Figure 6. Soft start discharge current vs. temperature.

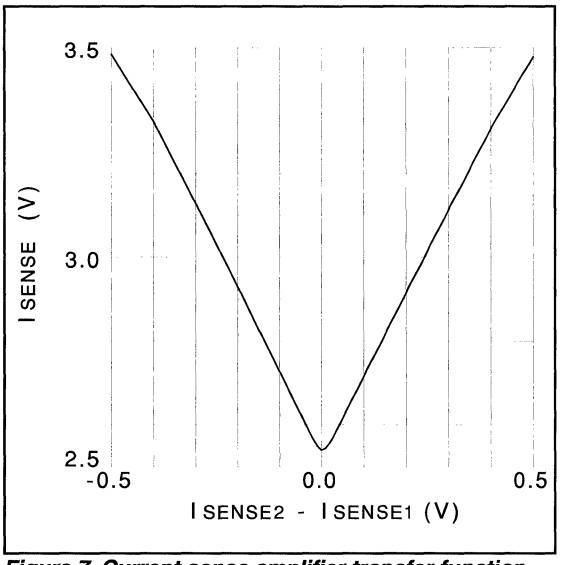


Figure 7. Current sense amplifier transfer function.

APPLICATION INFORMATION (cont.)

Power Stage Design

The UC3625 is useful in a wide variety of applications, including high-power in robotics and machinery. The power output stages used in such equipment can take a number of forms, according to the intended performance and purpose of the system. Below are four different power stages with the advantages and disadvantages of each shown.

For high-frequency chopping, fast recovery circulating diodes are essential. Six are required to clamp the windings. These diodes should have a continuous current rating at least equal to the operating motor current, since diode conduction duty-cycle can be high. For low-voltage systems, Schottky diodes are preferred. In higher voltage systems, diodes such as Microsemi UHVP high voltage platinum rectifiers are recommended.

In a pulse-by-pulse current control arrangement, current sensing is done by resistor R_S, through which the transistor's currents are passed (Fig. A, B, and C). In these cases, R_D is not needed. The low-side circulating diodes go to ground and the current sense terminals of the UC3625 (I_{SENSE1} and I_{SENSE2}) are connected to R_S through a differential RC filter. The input bias current of the current sense amplifier will cause a common mode offset voltage to appear at both inputs, so for best accuracy, keep the filter resistors below 2kΩ and matched.

The current that flows through R_S is discontinuous because of chopping. It flows during the on time of the power stage and is zero during the off time. Consequently, the voltage across R_S consists of a series of pulses, occurring at the PWM frequency, with a peak value indicative of the peak motor current.

To sense average motor current instead of peak current, add another current sense resistor (R_D in Fig. D) to measure current in the low-side circulating diodes, and operate in four quadrant mode (pin 22 high). The negative voltage across R_D is corrected by the absolute value current sense amplifier. Within the limitations imposed by Table 1, the circuit of Fig. B can also sense average current.

APPLICATION INFORMATION (cont.)

FIGURE A

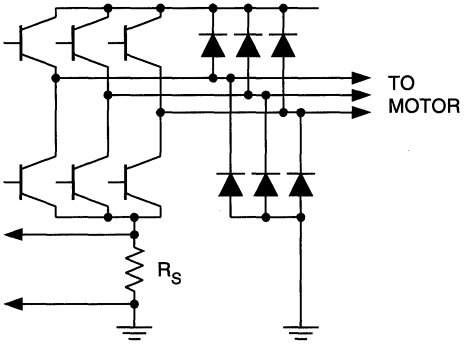


FIGURE B

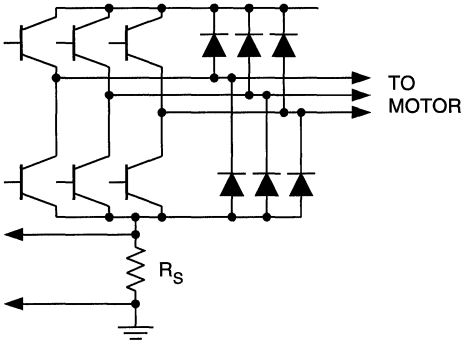


FIGURE C

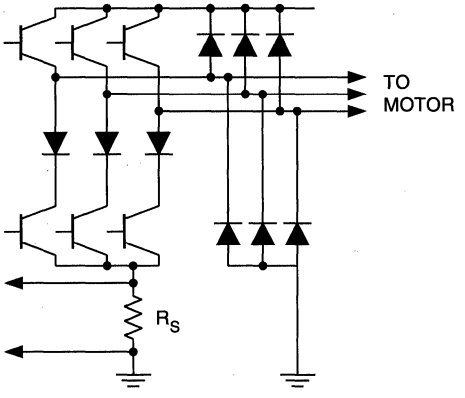
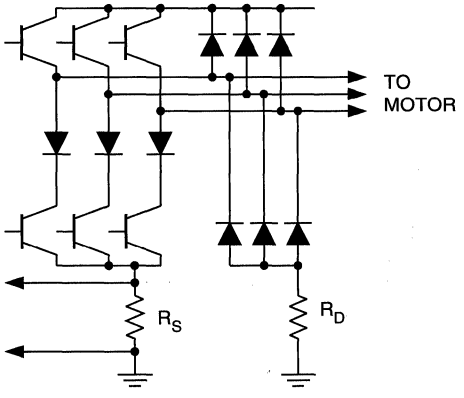


FIGURE D



	2 QUADRANT	4 QUADRANT	SAFE BRAKING	POWER REVERSE	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
FIGURE A	YES	NO	NO	NO	YES	NO
FIGURE B	YES	YES	NO	IN 4-QUAD MODE ONLY	YES	YES
FIGURE C	YES	YES	YES	IN -4QUAD MODE ONLY	YES	NO
FIGURE D	YES	YES	YES	IN-4QUADMODE ONLY	YES	YES

APPLICATION INFORMATION (cont.)

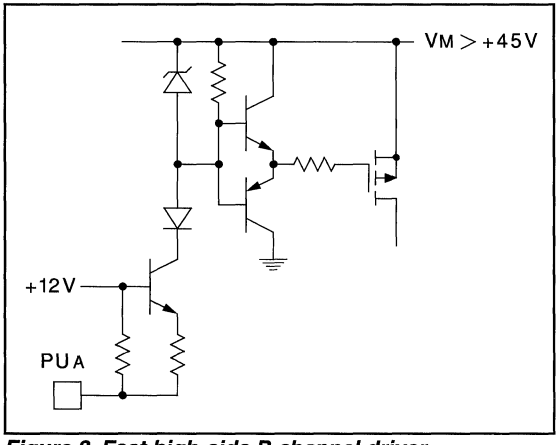


Figure 8. Fast high-side P-channel driver.

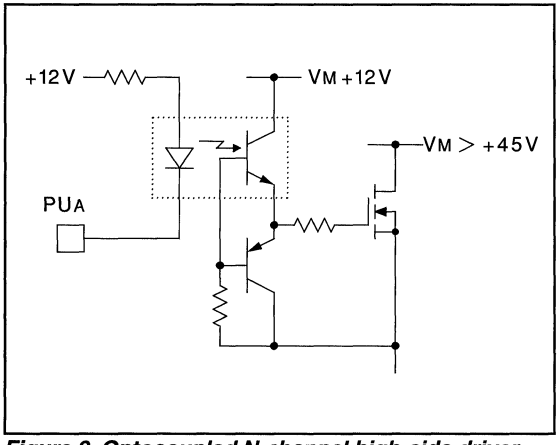


Figure 9. Optocoupled N-channel high-side driver.

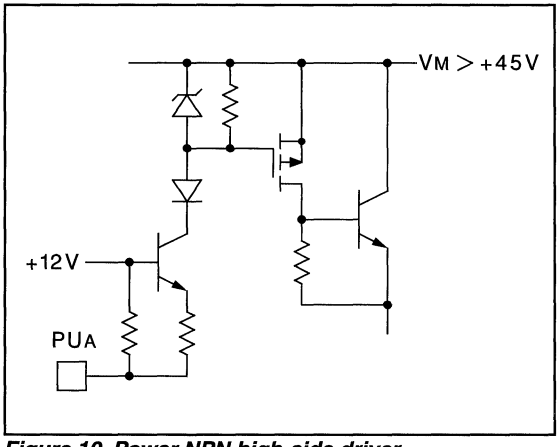


Figure 10. Power NPN high-side driver.

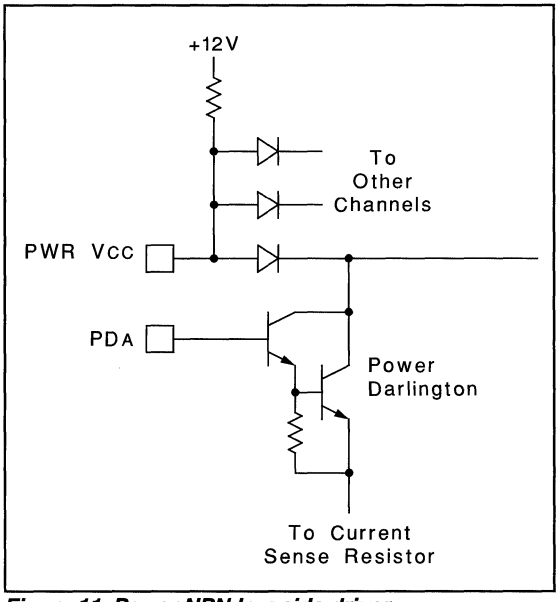


Figure 11. Power NPN low-side driver.

For drives where speed is critical, P-Channel MOSFETs can be driven by emitter followers as shown in Fig. 8. Here, both the level shift NPN and the PNP must withstand high voltages. A zener diode is used to limit gate-source voltage on the MOSFET. A series gate resistor is not necessary, but always advisable to control overshoot and ringing.

High-voltage optocouplers can quickly drive high-voltage MOSFETs if a boost supply of at least 10 volts greater than the motor supply is provided (See Fig. 9.) To protect the MOSFET, the boost supply should not be higher than 18 volts above the motor supply.

For under 200V 2-quadrent applications, a power NPN driven by a small P-Channel MOSFET will perform well as a high-side driver as in Fig. 10. A high voltage small-signal NPN is used as a level shift and a high voltage low-current MOSFET provides drive. Although the NPN will not saturate if used within its limitations, the base-emitter resistor on the NPN is still the speed limiting component.

Fig. 11 shows a power NPN Darlington drive technique using a clamp to prevent deep saturation. By limiting saturation of the power device, excessive base drive is minimized and turn-off time is kept fairly short. Lack of base series resistance also adds to the speed of this approach.

APPLICATION INFORMATION (cont.)

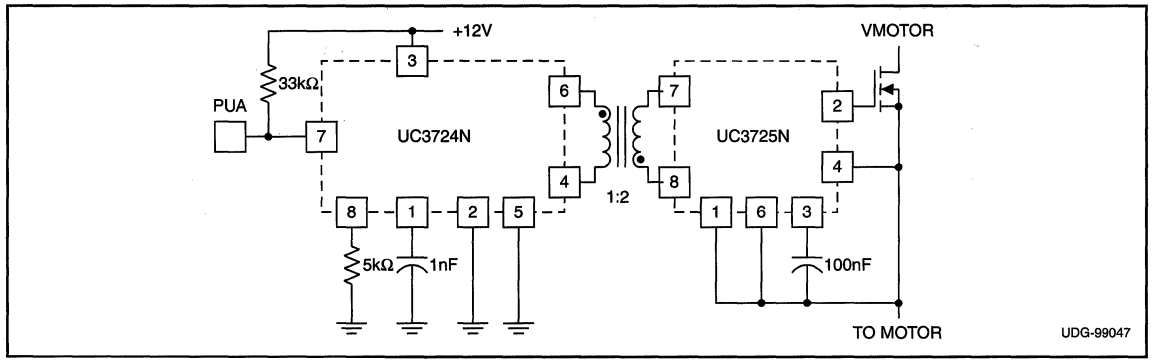


Figure 12. Fast high-side N-channel driver with transformer isolation.

Fast High-Side N-Channel Driver with Transformer Isolation

A small pulse transformer can provide excellent isolation between the UC3625 and a high-voltage N-Channel MOSFET while also coupling gate drive power. In this circuit (shown in Fig. 12), a UC3724 is used as a transformer driver/encoder that duty-cycle modulates the transformer with a 150kHz pulse train. The UC3725 rectifies this pulse train for gate drive power, demodulates the signal, and drives the gate with over 2 amp peak current.

Both the UC3724 and the UC3725 can operate up to 500kHz if the pulse transformer is selected appropriately. To raise the operating frequency, either lower the timing resistor of the UC3724 (1kΩ min), lower the timing capacitor of the UC3724 (500pF min) or both.

If there is significant capacitance between transformer primary and secondary, together with very high output slew rate, then it may be necessary to add clamp diodes from the transformer primary to +12V and ground. General purpose small signal switching diodes such as 1N4148 are normally adequate.

The UC3725 also has provisions for MOSFET current limiting. Consult the UC3725 data sheet for more information on implementing this.

Computational Truth Table

This table shows the outputs of the gate drive and open collector outputs for given hall input codes and direction signals. Numbers at the top of the columns are pin numbers.

These ICs operate with position sensor encoding that has either one or two signals high at a time, never all low or all high. This coding is sometimes referred to as "120° Coding" because the coding is the same as coding with position sensors spaced 120 magnetic degrees about the rotor. In response to these position sense signals, only one low-side driver will turn on (go high) and one high-side driver will turn on (pull low) at any time.

Table I. Computational truth table.

INPUTS				OUTPUTS					
DIR	H1	H2	H3	Low-Side			High-Side		
6	8	9	10	12	13	14	16	17	18
1	0	0	1	L	H	L	L	H	H
1	0	1	1	L	L	H	L	H	H
1	0	1	0	L	L	H	H	L	H
1	1	1	0	H	L	L	H	L	H
1	1	0	0	H	L	L	H	H	L
1	1	0	1	L	H	L	H	H	L
0	1	0	1	L	L	H	H	L	H
0	1	0	0	L	L	H	L	H	H
0	1	1	0	L	H	L	L	H	H
0	0	1	0	L	H	L	H	H	L
0	0	1	1	H	L	L	H	H	L
0	0	0	1	H	L	L	H	L	H
X	1	1	1	L	L	L	H	H	H
X	0	0	0	L	L	L	H	H	H

APPLICATION INFORMATION (cont.)

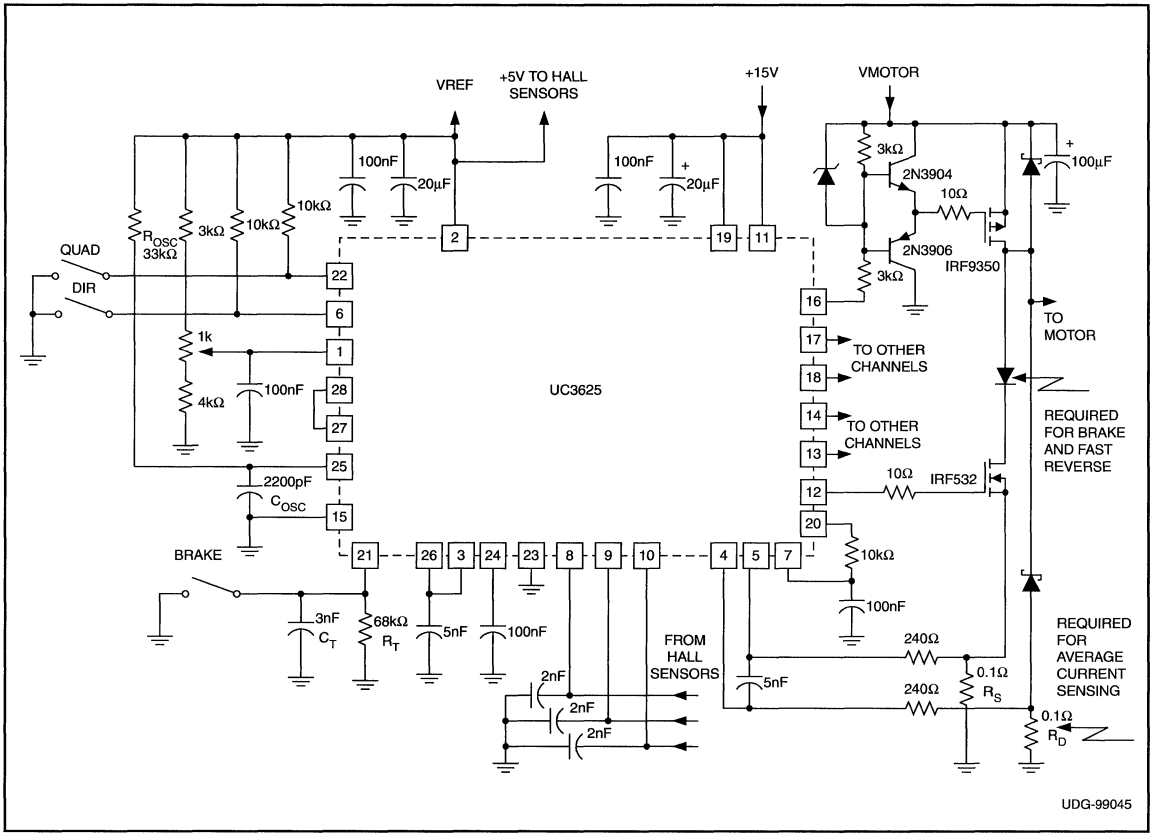


Figure 13. 45V/8A brushless DC motor drive circuit.

N–Channel power MOSFETs are used for low–side drivers, while P–Channel power MOSFETs are shown for high–side drivers. Resistors are used to level shift the UC3625 open–collector outputs, driving emitter followers into the MOSFET gate. A 12V zener clamp insures that the MOSFET gate–source voltage will never exceed 12V. Series 10Ω gate resistors tame gate reactance, preventing oscillations and minimizing ringing.

The oscillator timing capacitor should be placed close to pins 15 and 25, to keep ground current out of the capacitor. Ground current in the timing capacitor causes oscillator distortion and slaving to the commutation signal.

The potentiometer connected to pin 1 controls PWM duty cycle directly, implementing a crude form of speed control. This control is often referred to as "voltage mode" because the potentiometer position sets the average motor voltage. This controls speed because steady–state motor speed is closely related to applied voltage.

Pin 20 (Tach-Out) is connected to pin 7 (SPEED IN) through an RC filter, preventing direction reversal while the motor is spinning quickly. In two–quadrant operation, this reversal can cause kinetic energy from the motor to be forced into the power MOSFETs.

A diode in series with the low-side MOSFETs facilitates PWM current control during braking by insuring that braking current will not flow backwards through low–side MOSFETs. Dual current–sense resistors give continuous current sense, whether braking or running in four–quadrant operation, an unnecessary luxury for two–quadrant operation.

The 68kΩ and 3nF tachometer components set maximum commutation time at 140µs. This permits smooth operation up to 35,000 RPM for four–pole motors, yet gives 140µs of noise blanking after commutation.

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UNITRODE

application INFO available

UCC2626
UCC3626

Brushless DC Motor Controller

PRELIMINARY

FEATURES

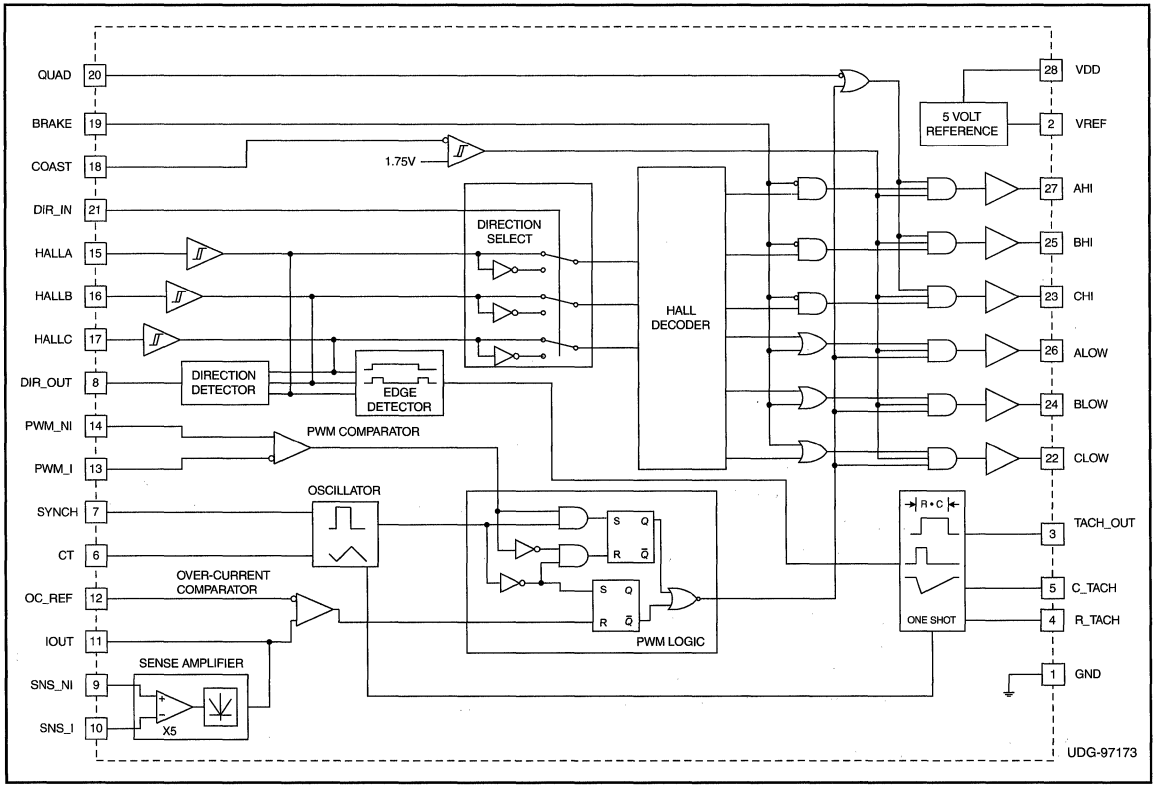
- Two Quadrant and Four Quadrant Operation
- Integrated Absolute Value Current Amplifier
- Pulse-by-Pulse and Average Current Sensing
- Accurate, Variable Duty Cycle Tachometer Output
- Trimmed Precision Reference
- Precision Oscillator
- Direction Output

DESCRIPTION

The UCC3626 motor controller IC combines many of the functions required to design a high performance, two or four quadrant, 3-phase, brushless DC motor controller into one package. Rotor position inputs are decoded to provide six outputs that control an external power stage. A precision triangle oscillator and latched comparator provide PWM motor control in either voltage or current mode configurations. The oscillator is easily synchronized to an external master clock source via the SYNCH input. Additionally, a QUAD select input configures the chip to modulate either the low side switches only, or both upper and lower switches, allowing the user to minimize switching losses in less demanding two quadrant applications.

The chip includes a differential current sense amplifier and absolute value circuit which provide an accurate reconstruction of motor current, useful for pulse by pulse over current protection as well as closing a current control loop. A precision tachometer is also provided for implementing closed loop speed control. The TACH_OUT signal is a variable duty cycle, frequency output which can be used directly for digital control or filtered to provide an analog feedback signal. Other features include COAST, BRAKE, and DIR_IN commands along with a direction output, DIR_OUT.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} . . . . . +15V
Inputs
Pins 20, 19, 18, 21, 15, 16, 17, 7, 12, 9, 10 . . . . –0.3V to V_{DD}
Pins 13, 14 . . . . . –0.3V to 8.0V
Output Current
Pins 22, 23, 24, 25, 26, 27 . . . . . ±200mA
Pins 2 . . . . . –20mA
Pins 3. 8, 11 . . . . . 1mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering 10 Seconds) . . . . . +300°C

Note: Unless otherwise indicated, voltages are referenced to ground. Currents are positive into, negative out of specified terminal. Consult packaging section of Databook for thermal limitations and considerations of package.

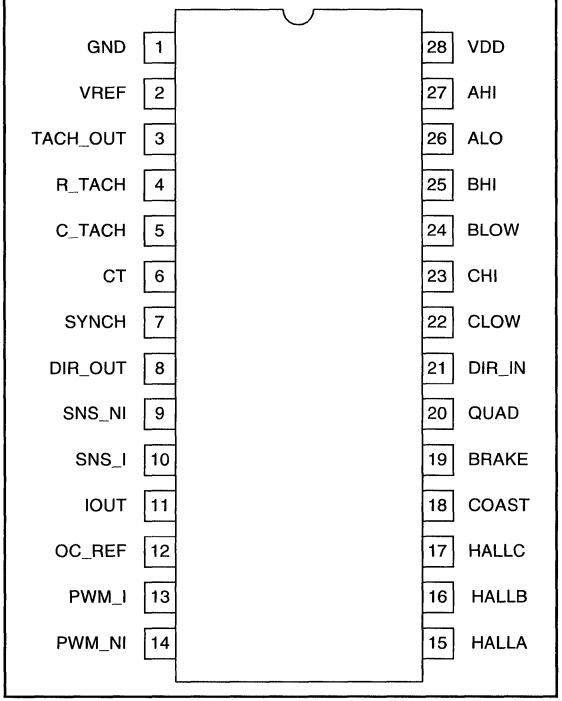
ORDERING INFORMATION

UCC ☐626☐
PACKAGE
TEMPERATURE RANGE

	TEMPERATURE RANGE	PACKAGE
UCC2626N	–40°C to +85°C	DIL
UCC2626DW		SOIC
UCC2626PW		TSSOP
UCC3626N	0°C to +70°C	DIL
UCC3626DW		SOIC
UCC3626PW		TSSOP

CONNECTION DIAGRAMS

DIL-28, SOIC-28, TSSOP-28 (Top View)
N Package, DW Package, PW Package



8

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VCC = 12V; CT = 1nF, R_{TACH} = 250K, C_{TACH} = 100pF, $T_A = T_J$, T_A = –40°C to +85°C for the UCC2626, and 0°C to +70°C for the UCC3626.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current			3	10	mA
Under-Voltage Lockout					
Start Threshold			10.5		V
UVLO Hysteresis			0.5		V
5.0 V Reference					
Output Voltage	I_{VREF} = –2mA	4.9	5	5.1	V
Line Regulation	11V < VCC < 14.5V			10	mV
Load Regulation	–1 > I_{VREF} > –5mA			30	mV
Short Circuit Current		40	120		mA
Coast Input Comparator					
Threshold			1.75		V
Hysteresis			0.1		V
Input Bias Current			0.1		µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VCC = 12V; CT = 1nF, R_{TACH} = 250K, C_{TACH} = 100pF, $T_A = T_J$, T_A = –40°C to +85°C for the UCC2626, and 0°C to +70°C for the UCC3626.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Amplifier					
Input Offset Voltage	VCM = 0V			5	mV
Input Bias Current	VCM = 0V		10		µA
Gain	VCM = 0V	4.9	5	5.1	V/V
CMRR	–0.3V < VCM < 0.5		60		dB
PSRR	11V < VCC <14.5V		60		dB
Output High Voltage	I_{IOUT}= –100µA	5			V
Output Low Voltage	I_{IOUT} = 100µA			50	mV
Output Source Current	V_{IOUT} = 2V	500			µA
PWM Comparator					
Input Common Mode Range		2.0		8.0	V
Propogation Delay			75		nS
Over-Current Comparator					
Input Common Mode Range		0.0		5.0	V
Propogation Delay			175		nS
Logic Inputs					
Logic High	QUAD, BRAKE, DIR			3.5	V
Logic Low	QUAD, BRAKE, DIR	1.5			V
Input Current	QUAD, BRAKE, DIR		0.1		µA
Hall Buffer Inputs					
VIL	HALLA, HALLB, HALLC		1		V
VIH	HALLA, HALLB, HALLC		1.9		V
Input Current	0V < V_{IN} < 5V		–25		µA
Oscillator					
Frequency	R_{TACH} = 250k, CT = 1nF		10		KHz
Frequency Change With Voltage	12V < VCC < 14.5V			5	%
CT Peak Voltage			7.5		V
CT Valley Voltage			2.5		V
CT Peak-to-Valley Voltage			5.0		V
SYNCH Pin Minimum Pulse Width		–500			ns
Tachometer					
V_{OH}/V_{REF}	I_{OUT} = –10µA	99		100	%
Vol	I_{OUT} = 10µA	0		20	mV
R_{ON} High	I_{OUT} = –100µA		1		kΩ
R_{ON} Low	I_{OUT} = 100µA		1		kΩ
Ramp Threshold, Lo			20		mV
Ramp Threshold, Hi			2.52		V
C_{TACH} Charge Current	R_{TACH} = 49.9kΩ		50		µA
T-on Accuracy	Note 1	–3		3	%
Direction Output					
DIR OUT High Level	I_{OUT} = –100µA	3.5		5.1	V
DIR OUT Low Level	I_{OUT} = 100µA	0		1	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for VCC = 12V; CT = 1nF, R_{TACH} = 250K, C_{TACH} = 100pF, $T_A = T_J$, T_A = –40°C to +85°C for the UCC2626, and 0°C to +70°C for the UCC3626.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Section					
Maximum Duty Cycle				100	%
Output Low Voltage	I_{OUT} = 10mA		0.4		V
Output High Voltage	I_{OUT} = –10mA	4.0		5.1	V
Output Low Voltage	I_{OUT} = 1mA			1	V
Output High Voltage	I_{OUT} = –1mA	4.0		5.1	V
Rise/Fall Time	Cl = 100pF		100		nS

Note 1: T(on) is calculated using the formula: $T(on) = C_{TACH} \bullet (V_{HI} - V_{LO})/I_{CHARGE}$. This number is compared to the formula $T(on) = R_{TACH} \bullet C_{TACH}$.

PIN DESCRIPTIONS

AHI, BHI, CHI: Digital outputs used to control the high side switches in a three phase inverter. For specific decoding information reference Table I.

ALOW, BLOW, CLOW: Digital outputs used to control the low side switches in a three phase inverter. For specific decoding information reference Table I.

BRAKE: BRAKE is a digital input which causes the device to enter brake mode. In brake mode all three high side outputs are turned off, AHI, BHI & CHI, while all three lowside outputs are turned on, ALOW, BLOW, CLOW. During brake mode the tachometer output remains operational. The only conditions which can inhibit the low side commands during brake are UVLO, exceeding peak current, the output of the PWM comparator, or the COAST command.

COAST: The COAST input consists of a hysteretic comparator which disables the outputs. The input is useful in implementing an overvoltage bus clamp in four quadrant applications. The outputs will be disabled when the input is above 1.75V.

CT: This pin is used in conjunction with the R_TACH pin to set the frequency of the oscillator. A timing capacitor is normally connected between this point and ground and is alternately charged and discharged between 2.5V and 7.5V.

C_TACH: A timing capacitor is connected between this pin and ground to set the width of the TACH_OUT pulse. The capacitor is charged with a current set by the resistor on pin RT.

DIR_IN: DIR_IN is a digital input which determines the order in which the HALLA,B & C inputs are decoded. For specific decode information reference Table I.

DIR_OUT: DIR_OUT represents the actual direction of the rotor as decoded from the HALLA, B & C inputs. For any valid combination of HALLA, B &C inputs there are two valid transitions, one which translates to a clockwise rotation and another which translates to a counterclockwise rotation. The polarity of DIR_OUT is the same as DIR_IN while motoring, i.e. sequencing from top to bottom in Table 1.

GND: GND is the reference ground for all functions of the part. Bypass and timing capacitors should be terminated as close to this point as possible.

HALLA, HALLB, HALLC: These three inputs are designed to accept rotor position information positioned 120° apart. For specific decode information reference Table I. These inputs should be externally pulled-up to VREF or another appropriate external supply.

IOUT: IOUT represents the output of the current sense and absolute value amplifiers. The output signal appearing is a representation of the following expression:

$$I_{OUT} = ABS(ISENS\_I - ISENS\_NI) \bullet 5$$

This output can be used to close a current control loop as well as provide additional filtering of the current sense signal.

OC_REF: OC_REF is an analog input which sets the trip voltage of the overcurrent comparator. The sense input of the comparator is internally connected to the output of the current sense amplifier and absolute value circuit.

PWM_NI: PWM_NI is the noninverting input to the PWM comparator.

PWM_I: PWM_I is the inverting input to the PWM comparator.

PIN DESCRIPTIONS (cont.)

QUAD: The QUAD input selects between "two" QUAD = 0 and "four" QUAD = 1 quadrant operation. When in "two-quadrant" mode only the low side devices are effected by the output of the PWM comparator. In "four-quadrant" mode both high and low side devices are controlled by the PWM comparator.

SYNCH: The SYNCH input is used to synchronize the PWM oscillator with an external digital clock. When using the SYNCH feature, a resistor equal to R_{TACH} must be placed in parallel with CT. When not used, ground SYNCH.

SNS_NI, SNS_I: These inputs are the noninverting and inverting inputs to the current sense amplifier, respectively. The integrated amplifier is configured for a gain of five. An absolute value function is also incorporated into the output in order to provide a representation of actual motor current when operating in four quadrant mode.

TACH_OUT: TACH_OUT is the output of a monostable triggered by a change in the commutation state, thus providing a variable duty cycle, frequency output. The on-time of the monostable is set by the timing capacitor connected to C_TACH. The monostable is capable of being retriggered if a commutation occurs during it's on-time.

R_TACH: A resistor connected between R_TACH and ground programs the current for both the oscillator and tachometer.

VDD: VDD is the input supply connection for this device. Undervoltage lockout keeps the outputs off for inputs below 10.5V. The input should be bypassed with a 0.1µF ceramic capacitor, minimum.

VREF: VREF is a 5V, 2% trimmed reference output with 5mA of maximum available output current. This pin should be bypassed to ground with a 0.1µF ceramic capacitor, minimum.

APPLICATION INFORMATION

Table 1 provides the decode logic for the six outputs, AHI, BHI, CHI, ALOW, BLOW, and CLOW as a function of the BRAKE, COAST, DIR_IN, HALLA, HALLB, and HALLC inputs.

The UCC3626 is designed to operate with 120° position sensor encoding. In this format, the three position sensor signals are never simultaneously high or low. Motor's whose sensors provide 60° encoding can be converted to 120° using the circuit shown in Fig. 1.

In order to prevent noise from commanding improper commutation states, some form of low pass filtering on HALLA, HALLB, and HALLC is recommended. Passive

Table 1. Commutation truth table.

BRAKE	COAST	DIR_IN	HALL INPUTS			HIGH SIDE OUTPUTS			LOW SIDE OUTPUTS		
			A	B	C	A	B	C	A	B	C
0	0	1	1	0	1	1	0	0	0	1	0
0	0	1	1	0	0	1	0	0	0	0	1
0	0	1	1	1	0	0	1	0	0	0	1
0	0	1	0	1	0	0	1	0	1	0	0
0	0	1	0	1	1	0	0	1	1	0	0
0	0	1	0	0	1	0	0	1	0	1	0
0	0	0	1	0	1	0	1	0	1	0	0
0	0	0	0	0	1	0	1	0	0	0	1
0	0	0	0	1	1	1	0	0	0	0	1
0	0	0	0	1	0	1	0	0	0	1	0
0	0	0	1	1	0	0	0	1	0	1	0
0	0	0	1	0	0	0	0	1	1	0	0
X	1	X	X	X	X	0	0	0	0	0	0
1	0	X	X	X	X	0	0	0	1	1	1
0	0	X	1	1	1	0	0	0	0	0	0
0	0	X	0	0	0	0	0	0	0	0	0

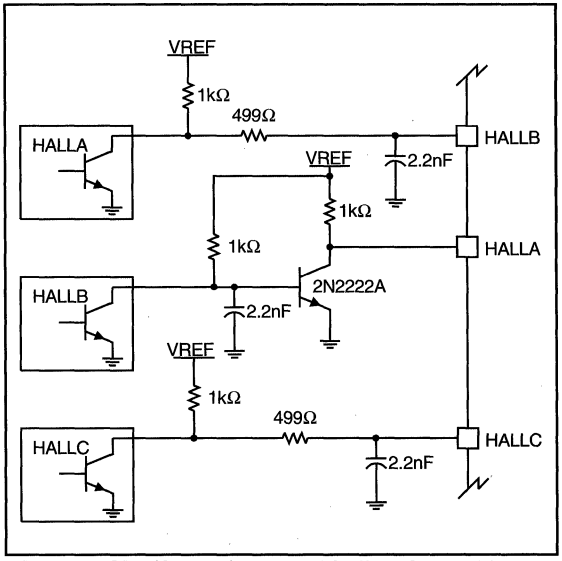


Figure 1. Circuit to convert 60° hall code to 120° code.

APPLICATION INFORMATION (cont.)

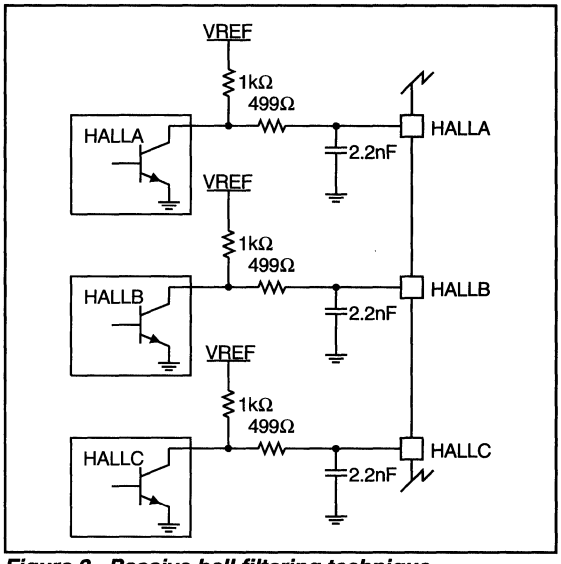


Figure 2. Passive hall filtering technique.

RC networks generally work well and should be located as close to the IC as possible. Fig. 2 illustrates these techniques.

Configuring the Oscillator

The UCC3626 oscillator is designed to operate at frequencies up to 250kHz and provide a triangle waveform on CT with a peak to peak amplitude of 5V for improved noise immunity. The current used to program CT is derived off of the R_TACH resistor according to the following equation:

$$I_{OSC} = \frac{25}{R\_TACH} Amps$$

Oscillator frequency is set by R_TACH and CT according to the following relationship:

$$Frequency = \frac{2.5}{(R\_TACH \bullet CT)} Hz$$

Timing resistor values should be between 25kΩ and 500kΩ while capacitor values should fall between 100pF and 1μF. Fig. 4 provides a graph of oscillator frequency for various combinations of timing components. As with any high frequency oscillator, timing components should be located as close to the IC pins as possible when laying out the printed circuit board. It is also important to reference the timing capacitor directly to the ground pin on the UCC3626 rather than daisy chaining it to another trace or the ground plane. This technique prevents switching current spikes in the local ground from causing jitter in the oscillator.

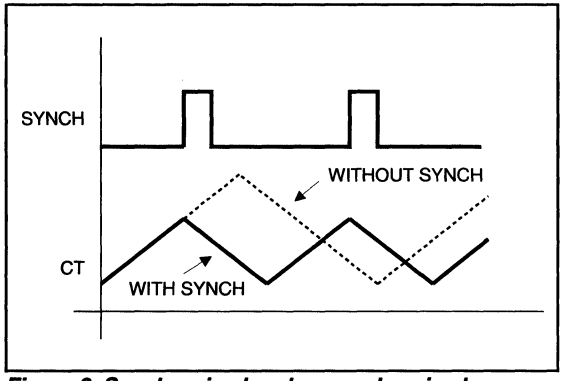


Figure 3. Synchronized and unsynchronized oscillator waveforms.

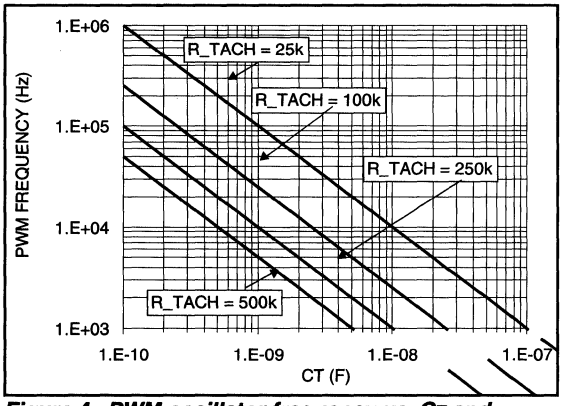


Figure 4. PWM oscillator frequency vs. CT and R_TACH.

Synchronizing the Oscillator

A common system specification is for all oscillators in a design to be synchronized to a master clock. The UCC3626 provides a SYNCH input for exactly this purpose. The SYNCH input is designed to interface with a digital clock pulse generated by the master oscillator. A positive going edge on this input causes the UCC3626 oscillator to begin discharging. In order for the slave oscillator to function properly it must be programmed for a frequency slightly lower than that of the master. Also, a resistor equal to R_{TACH} must be placed in parallel with CT. Fig. 3 illustrates the waveforms for a slave oscillator programmed to 20kHz with a master frequency of 30kHz. The SYNCH pin should be grounded when not used.

APPLICATION INFORMATION (cont.)

Programming the Tachometer

The UCC3626 tachometer consists of a precision, 5V monostable, triggered by either a rising or falling edge on any of the three Hall inputs, HALLA, HALLB, HALLC. The resulting TACH_OUT waveform is a variable dutycycle square wave whose frequency is proportional to motor speed, as given by:

$$TACH\_OUT = \frac{(V \bullet P)}{20} Hz$$

where P is the number of motor pole pairs and V is motor velocity in RPM.

The on-time of the monostable is programmed via timing resistor R_TACH and capacitor C_TACH according to the following equation:

$$On - Time = R\_TACH \bullet C\_TACH \text{ sec}$$

Fig. 5 provides a graph of On-Time for various combinations of R_TACH and C_TACH. On-Time is typically set to a value less than the minimum TACH-OUT period as given by:

$$T\_Period_{MIN} = \frac{20}{V_{MAX} \bullet P} \text{sec}$$

where P is the number of motor pole pairs and V is motor velocity in RPM.

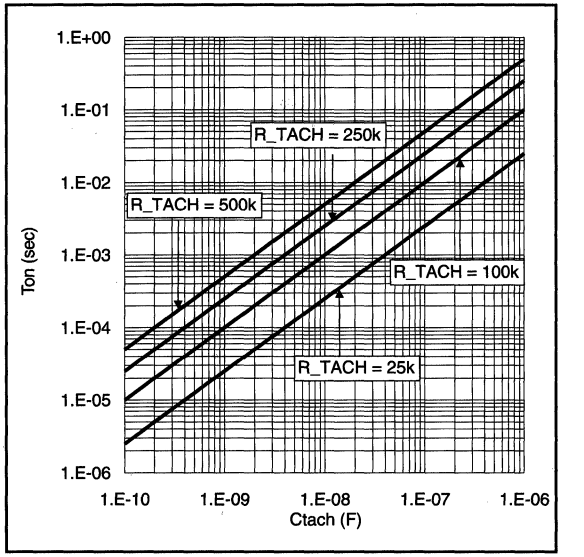


Figure 5. Tachometer on-time vs. C_TACH and R_TACH.

The TACH_OUT signal can be used to close a digital velocity loop using a microcontroller, as shown in Fig. 6, or directly low pass filtered in an analog implementation, Fig. 7.

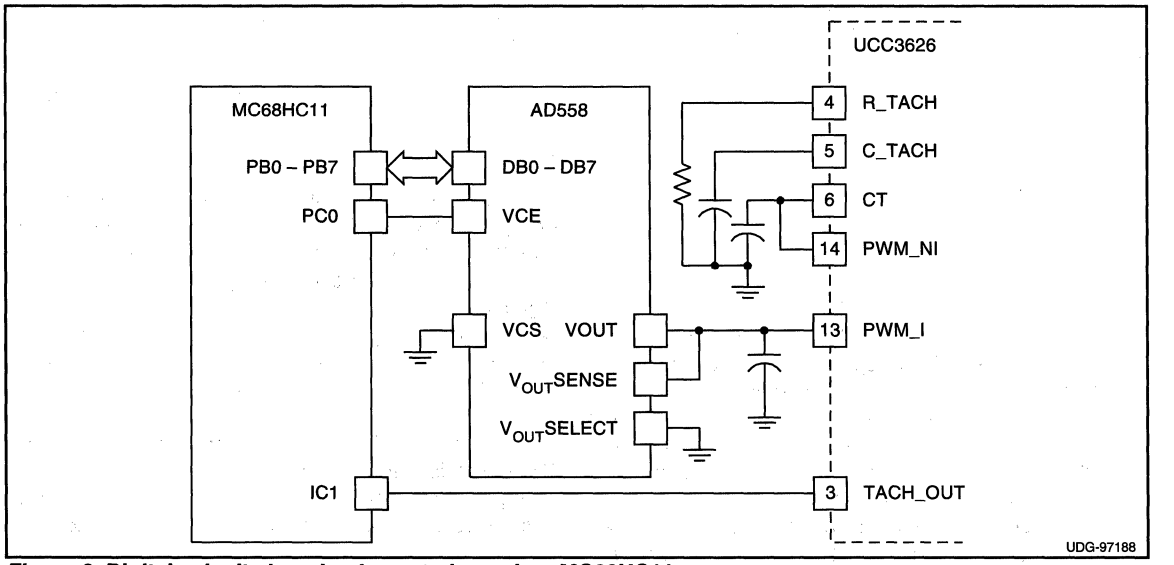


Figure 6. Digital velocity loop implementation using MC68HC11.

APPLICATION INFORMATION (cont.)

Two Quadrant vs Four Quadrant Control

Fig. 8 illustrates the four possible quadrants of operation for a motor. Two quadrant control refers to a system whose operation is limited to quadrants I and III where torque and velocity are in the same direction. With a two quadrant brushless DC amplifier, there are no provisions other than friction to decelerate the load, limiting the approach to less demanding applications. Four quadrant controllers, on the other hand, provide controlled operation in all quadrants, including II and IV, where torque and rotation are of opposite direction.

When configured for two quadrant operation, (QUAD=0), the UCC3626 will only modulate the low side devices of the output power stage. The current paths within the output stage during the PWM on and off times are illustrated in Fig. 9. During the 'on' interval, both switches are on and current flows through the load down to ground. During the 'off' time, the lower switch is shut off and the motor current circulates through the upper half bridge via the flyback diode. The motor is assumed to be operating in either quadrant I or III.

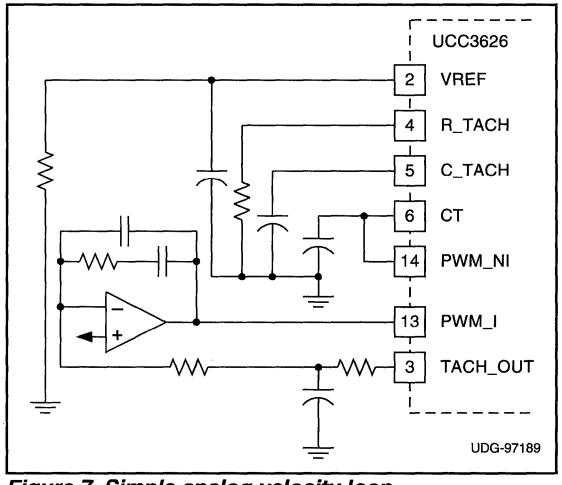


Figure 7. Simple analog velocity loop.

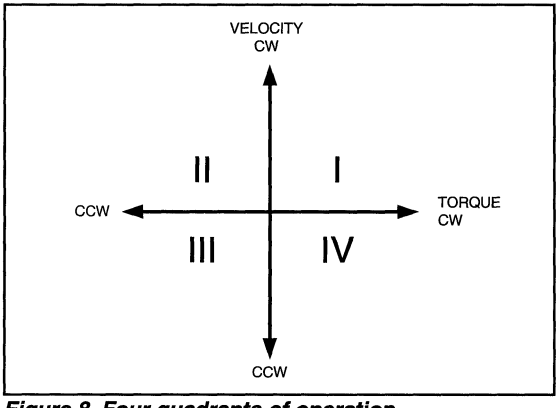


Figure 8. Four quadrants of operation.

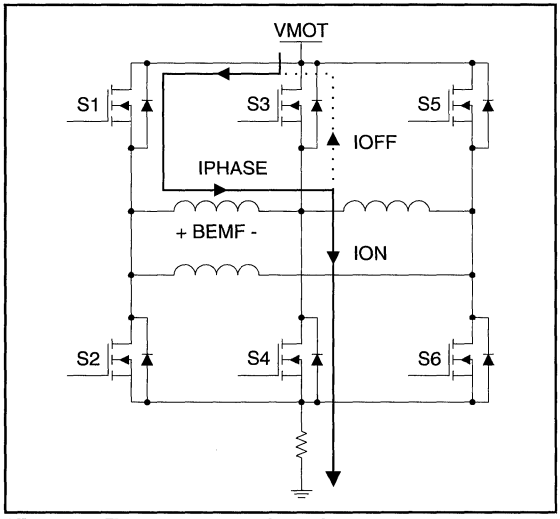


Figure 9. Two quadrant chopping.

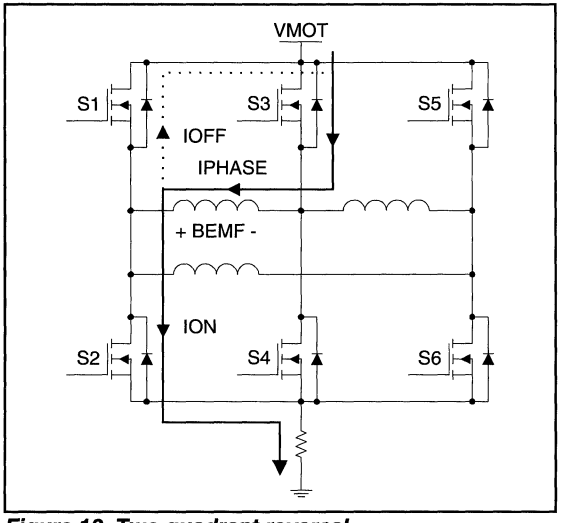


Figure 10. Two quadrant reversal.

APPLICATION INFORMATION (cont.)

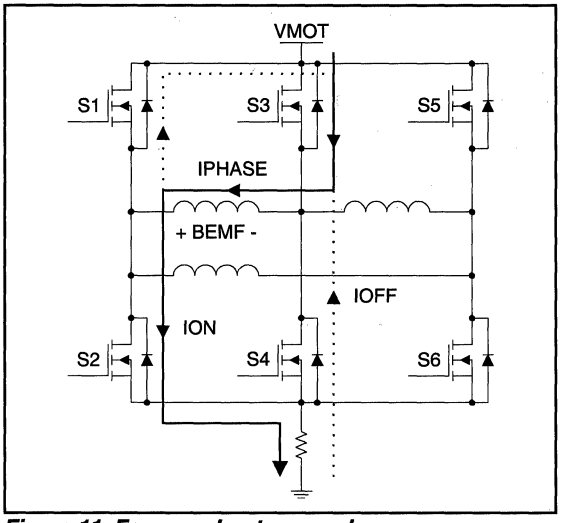


Figure 11. Four quadrant reversal.

If one attempts to operate in quadrants II or IV by changing the DIR bit and reversing the torque, switches 1 and 4 are turned off and switches 2 and 3 turned on. Under this condition motor current will very quickly decay, reverse direction and increase until the control threshold is reached. At this point switch 2 will turn off and current will once again circulate in the upper half bridge, however, in this case the motor's BEMF is in phase with the current, i.e. the motor's direction of rotation has not yet changed. Fig. 10 illustrates the current paths when operating in this mode. Under these conditions there is nothing to limit the current other than motor and drive impedance. These high circulating currents can result in damage to the power devices in addition to high, uncontrolled torque.

By pulse width modulating both the upper and lower power devices (QUAD=1), motor current will always decay during the PWM "off" time, eliminating any uncontrolled circulating currents. In addition, current will always flow through the current sense resistor, thus providing a suitable feedback signal. Fig. 11 illustrates the current paths during a four quadrant torque reversal. Motor drive waveforms for both two and four quadrant operation are illustrated in Fig. 12.

Power Stage Design Considerations

The flexible architecture of the UCC3626 requires the user to pay close attention to the design of the power output stage. Two and Four Quadrant applications that do not require the brake function are able to utilize the power stage approach illustrated in Fig. 13A. In many cases the body diode of the MOSFET can be utilized to reduce parts count and cost. If efficiency is a key requirement, Schottky diodes can be used in parallel with the switches.

If the system requires a braking function, diodes must be added in series with the lower power devices and the lower flyback diodes returned to ground, as pictured in Fig. 13B,C. This requirement prevents brake currents from circulating in the lower half bridge and bypassing the sense resistor. In addition, the combination of braking and four quadrant control necessitates an additional resistor in the diode path to sense current during the PWM 'off' time as illustrated in Fig. 13C.

Current Sensing

The UCC3626 includes a differential current sense amplifier with a fixed gain of five, along with an absolute value circuit. The current sense signal should be low pass filtered to eliminate leading edge spikes. In order to maximize performance, the input impedance of the amplifier should be balanced. If the sense voltage must be trimmed for accuracy reasons, a low value input divider or a differential divider should be used to maintain impedance matching, as shown in Fig. 14.

With four quadrant chopping motor current always flows through the sense resistor. However, during the flyback period the polarity across the sense resistor is reversed. The absolute value amplifier cancels the polarity reversal by inverting the negative sense signal during the flyback time, see Fig. 15. Therefore, the output of the absolute value amplifier is a reconstructed analog of the motor current, suitable for protection as well as feedback loop closure.

APPLICATION INFORMATION (cont.)

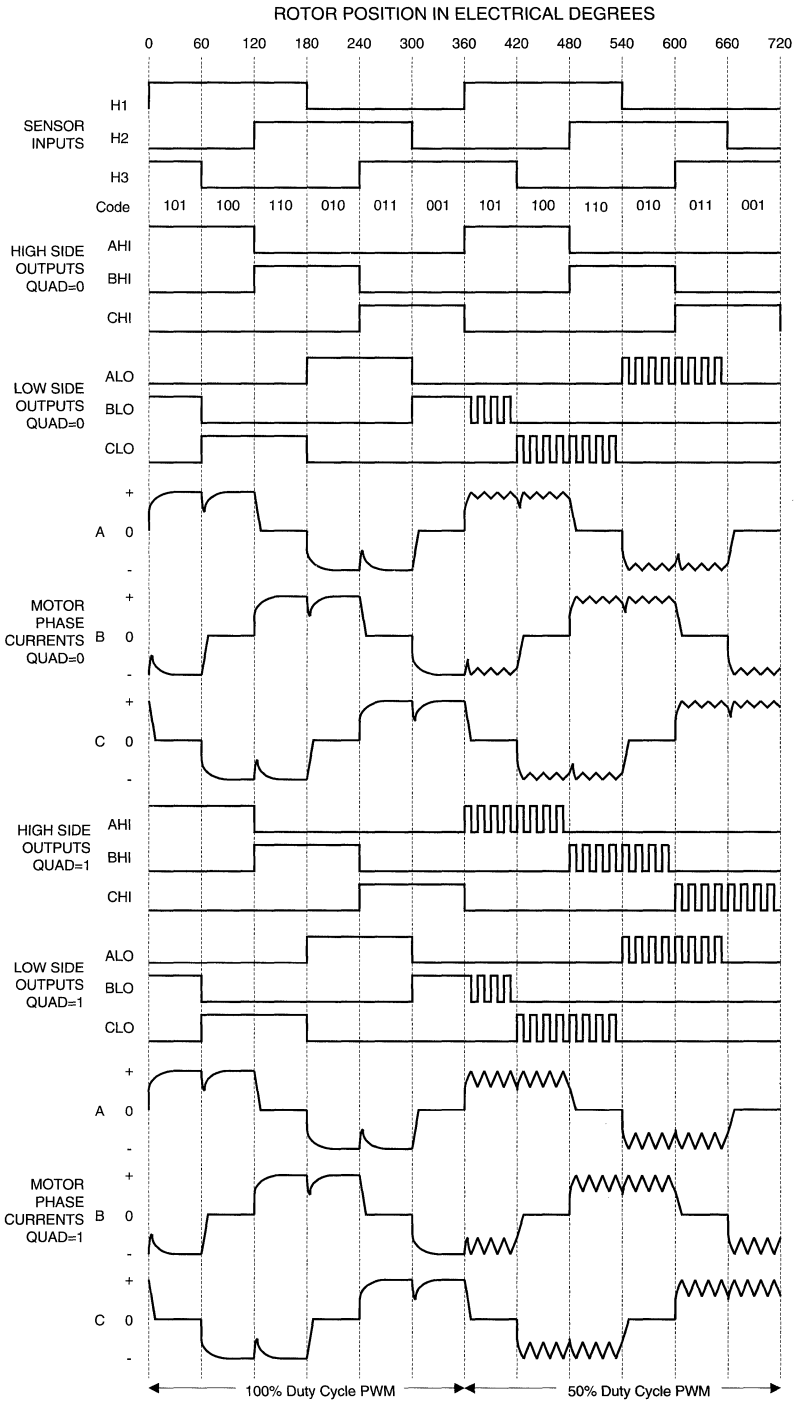
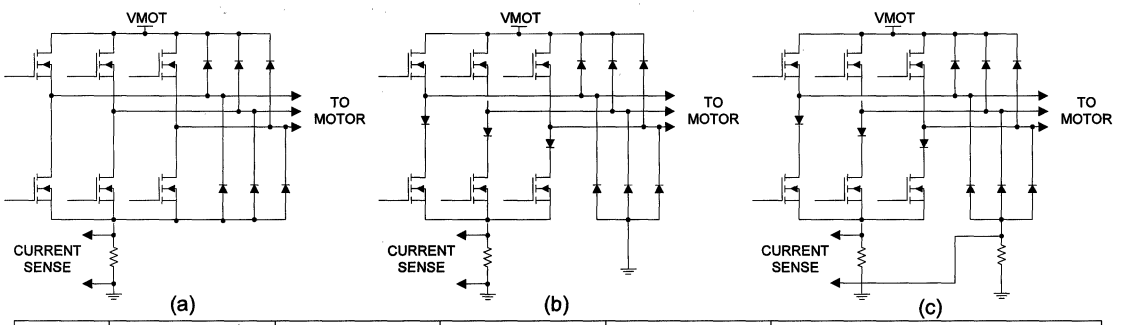


Figure 12. Motor drive and current waveforms for 2 quadrant (QUAD=0) and 4 quadrant (QUAD=1) operation.

TYPICAL APPLICATIONS



	TWO QUADRANT	FOUR QUADRANT	SAFE BRAKING	POWER REVERSAL	CURRENT SENSE	
					PULSE BY PULSE	AVERAGE
(a)	Yes	Yes	No	In 4-Quad Only	Yes	Yes
(b)	Yes	No	Yes	No	Yes	No
(c)	Yes	Yes	Yes	In 4-Quad Only	Yes	Yes

Figure 13. Power stage topologies.

Fig. 16 illustrates a simple 175V, 2A two quadrant velocity controller using the UCC3626. The power stage is designed to operate with a rectified off-line supply using IR2210s to provide the interface between the low voltage control signals and the power MOSFETs. The power topology illustrated in Fig. 13C is implemented in order to provide braking capability.

The controller's speed command is set by potentiometer R30 while the speed feedback signal is obtained by low pass filtering and buffering the TACH-OUT signal using R11 and C9. Small signal compensation of the velocity control loop is provided by amplifier U5A, whose output is used to control the PWM duty cycle. The integrating capacitor, C8, places a pole at 0Hz and a zero in conjunction with R10. This zero can be used to cancel the low frequency motor pole and cross the loop over with a –20dB gain response.

Four quadrant applications require the control of motor current. Fig. 17 illustrates a sign/magnitude current control loop within an outer bipolar velocity loop using the UCC3626. U1 serves as the velocity loop error amplifier and accepts a +/-5V command signal. Velocity feedback is provided by low pass filtering and scaling the TACH_OUT signal using U2. The direction output, DIR_OUT, switch and U3 set the polarity of the tachometer gain according to the direction of rotation. The output of the velocity error amplifier, U1, is then converted to sign/magnitude form using U5 and U6. The sign portion is used to drive the DIR input while the magnitude commands the current error amplifier, U8. Current feedback is provided by the internal current sense amplifier via the IOUT pin.

TYPICAL APPLICATION (cont.)

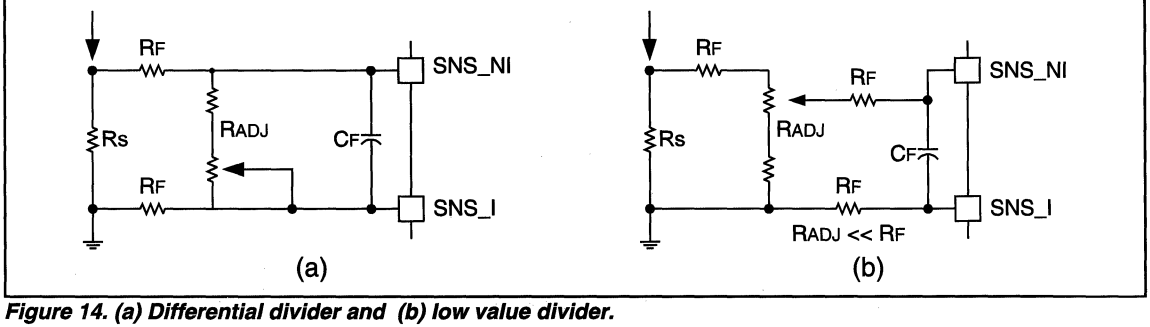


Figure 14. (a) Differential divider and (b) low value divider.

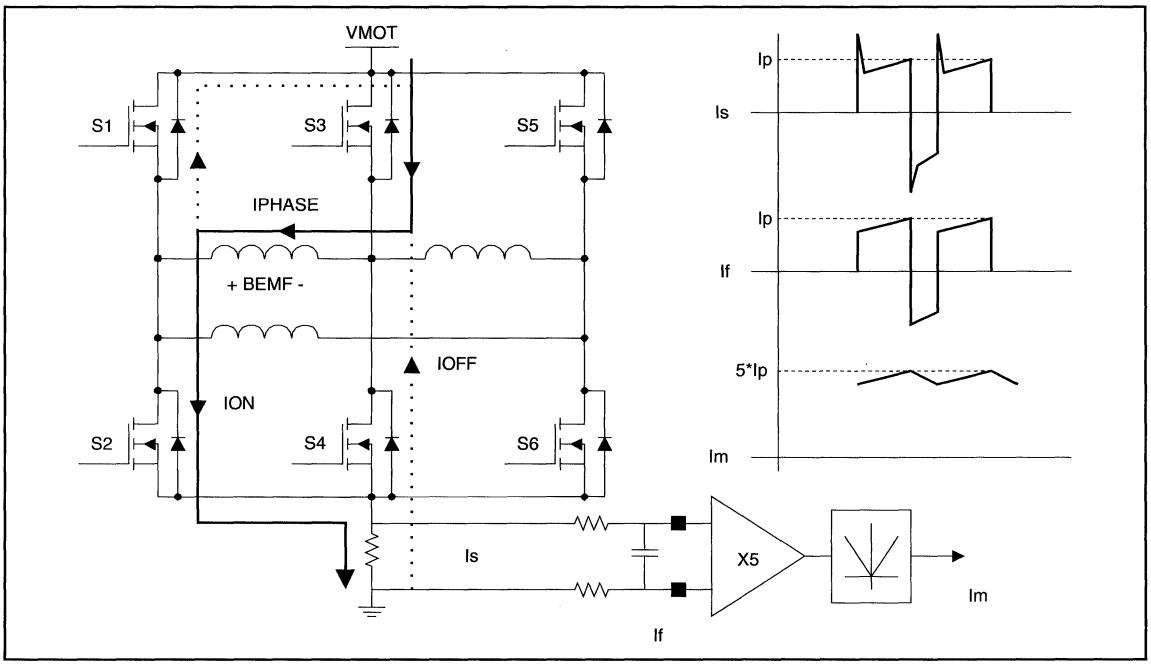


Figure 15. Current sense amplifier waveform.

TYPICAL APPLICATIONS (cont.)

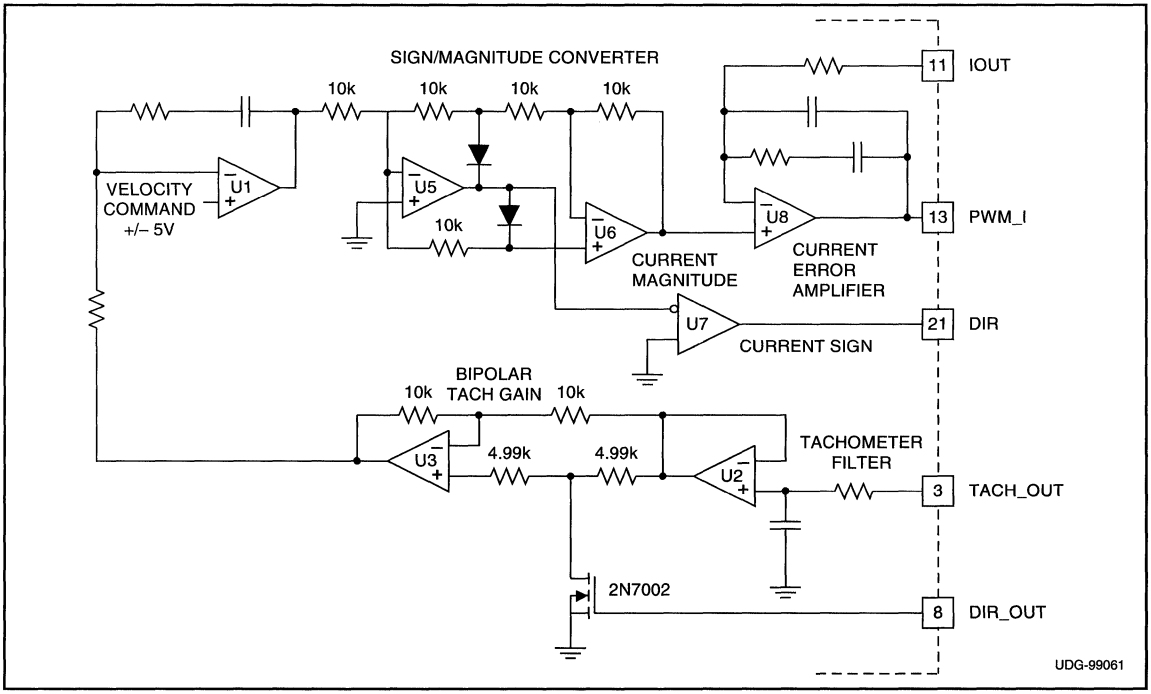


Figure 17. Four quadrant control loop.

TYPICAL APPLICATIONS (cont.)

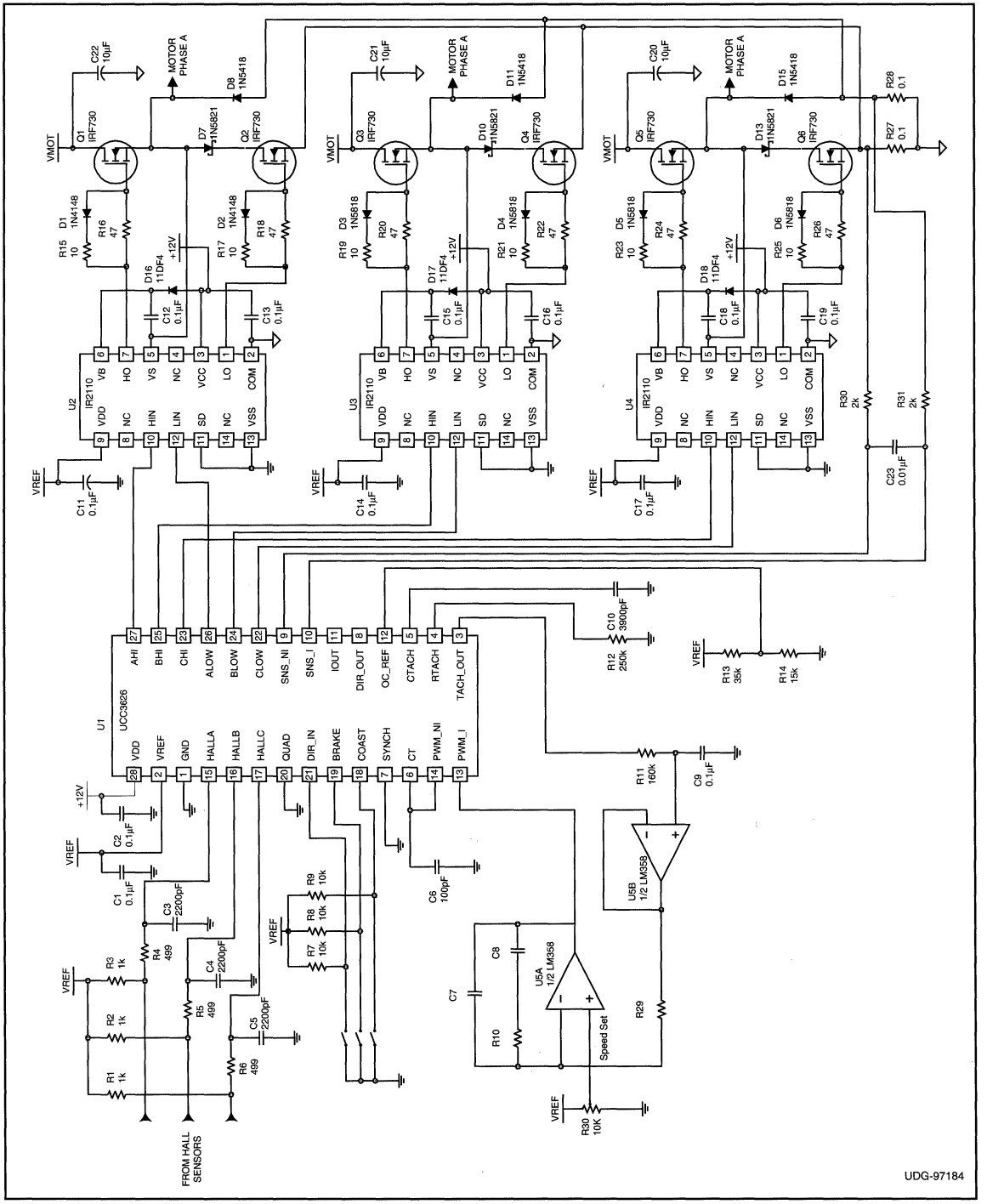


Figure 16. Two quadrant velocity controller.

UNITRODE CORPORATION
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UNITRODE

application INFO available

UC1633
UC2633
UC3633

Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

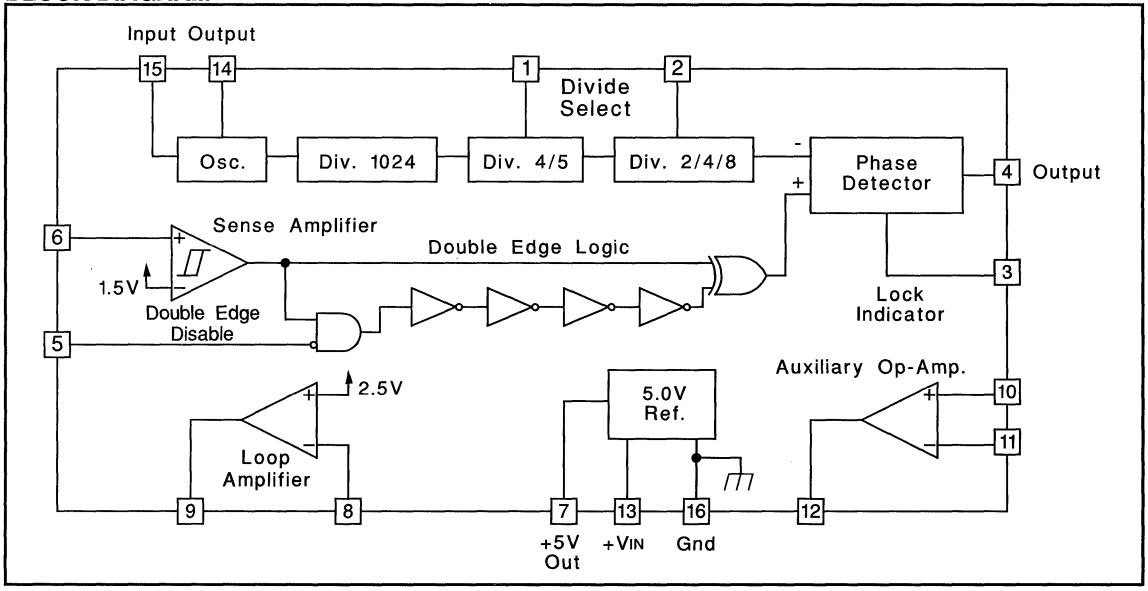
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output of other speed detection device. This signal is buffered by a sense ampilfier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of the op-amps will source or sink in excess of 16mA, so they can provide a low impedence control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM

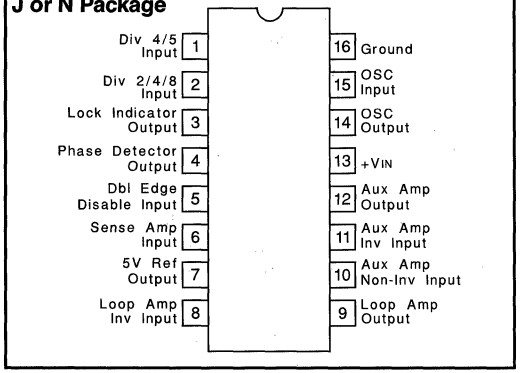


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) . . . . . +20V
Reference Output Current . . . . . -30mA
Op-Amp Output Currents . . . . . ±30mA
Op-Amp Input Voltages . . . . . -.3V to +20V
Phase Detector Output Current . . . . . ±10mA
Lock Indicator Output Current . . . . . +15mA
Lock Indicator Output Voltage . . . . . +20V
Divide Select Input Voltages . . . . . -.3V to +10V
Double Edge Disable Input Voltage . . . . . -.3V to +10V
Oscillator Input Voltage . . . . . -.3V to +5V
Sense Amplifier Input Voltage . . . . . .3V to +20V
Power Dissipation at TA = 25°C (Note 2 . . . . . 1000mW
Power dissipation at TC = 25°C (Note 2) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

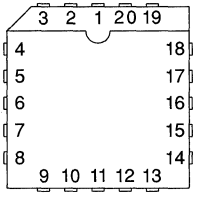
Note1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

DIL-16 (TOP VIEW)
J or N Package



CONNECTION DIAGRAMS

PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 4/5 Input	2
Div 2/4/8 Input	3
Lock Indicator Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

(Unless otherwise stated, these specifications apply for TA = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, +VIN = 12V; TA=TJ.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0V to 7mA		5.0	20	mV
Line Regulation	+VIN = 8V to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (VIB)	Oscillator Input Pin Open, TJ = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	VIN = VIB ±0.5V, TJ = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, TJ = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1VPP at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	µA
Div. 4/5 Threshold		0.5	1.6	2.2	V

Note 3: These impedence levels will vary with TJ at about 1700ppm/°C

ELECTRICAL CHARACTERISTICS (cont.): (Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, $+V_{IN}$ = 12V; T_A=T_J.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dividers (cont.)					
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Circuit Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	v
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
CMRR	V_{CM} = 0V to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedence levels will vary with T_J at about 1700ppm/°C

APPLICATION AND OPERATING INFORMATION

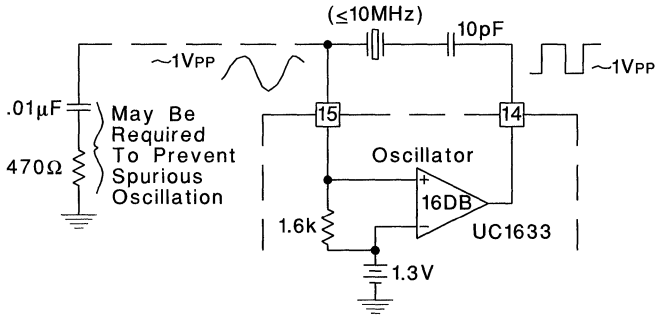
Determining the Oscillator Frequency

The frequency at the oscillator is determined by the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

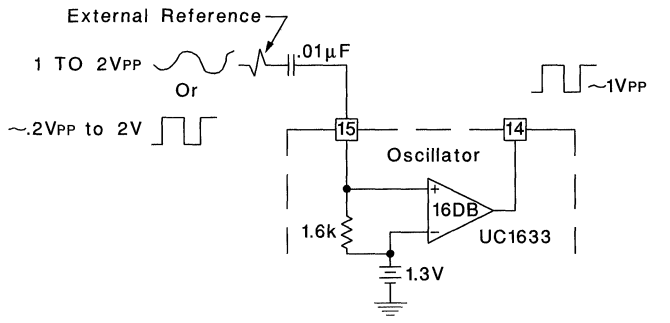
f_{OSC}(Hz) = (Divide Ratio) • (Motor RPM) • (1/60 SEC/MIN) • (No. of Rotor Poles/2) • (x 2 if Pin 5 Low)

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option, the loop reference frequency can be doubled for a given motor RPM.

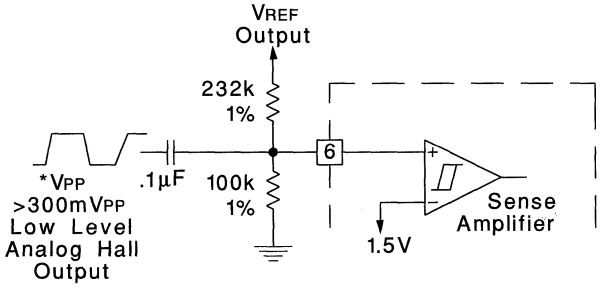
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method for Deriving Rotation Feedback Signal from Analog Hall Effect Device



**This signal may require filtering if chopped mode drive scheme is used.*

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

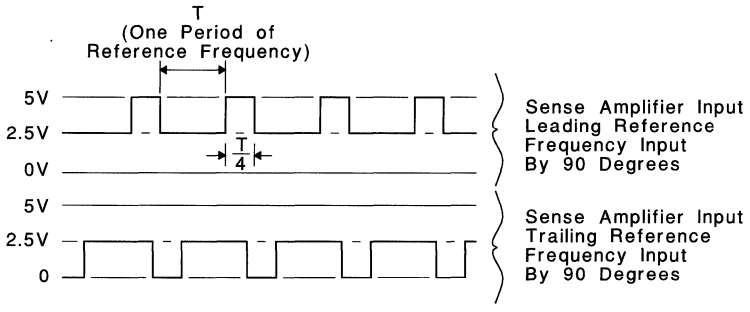
The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low and the middle state output impedence is high, typically 6.0kΩ. When there is any static frequency difference between the inputs, the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

When the frequencies of the two inputs to the detector are equal, the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level for the remainder of the period. If the phase relationship is reversed, then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector. kø, is 5V/4π radians or about 0.4V/radian. The dynamic range of the detector is ±2π radians.

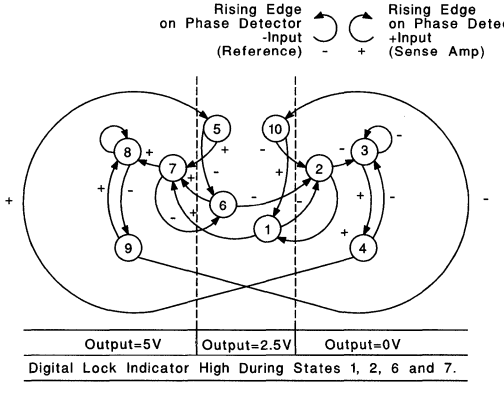
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic, and the connecting arrows represent the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge of the -input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from the frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

Typical Phase Detector Output Waveforms

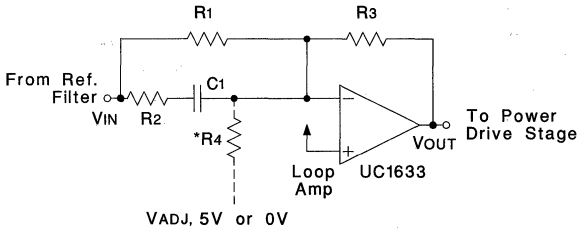


Phase Detector State Diagram



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{R_3}{R_1} \bullet \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{R_2 C_1}$$

$$\omega_z = \frac{1}{(R_1 + R_2)\, C_1}$$

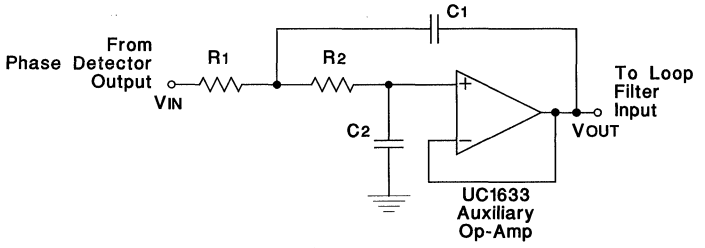
* The static phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R_4 = \frac{2.5V \bullet R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At Loop Amplifier Output During Phase Lock

If: (V_{OUT} - 2.5) > 0, R4 Goes to 0V
(V_{OUT} - 2.5) < 0, R4 Goes to 5.0V

Reference Filter Configuration



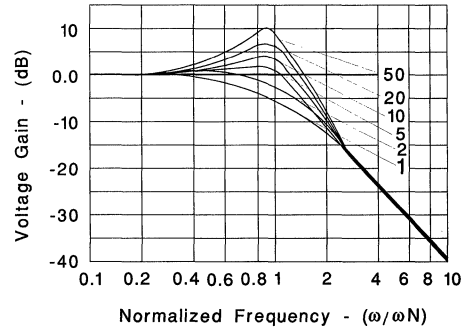
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s\,2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

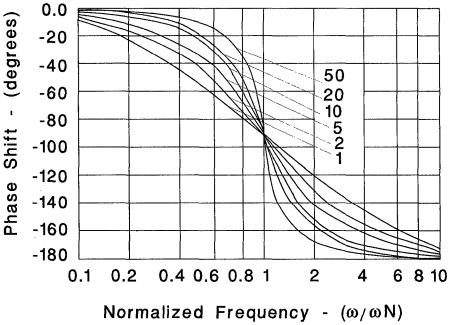
Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid - Gain Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

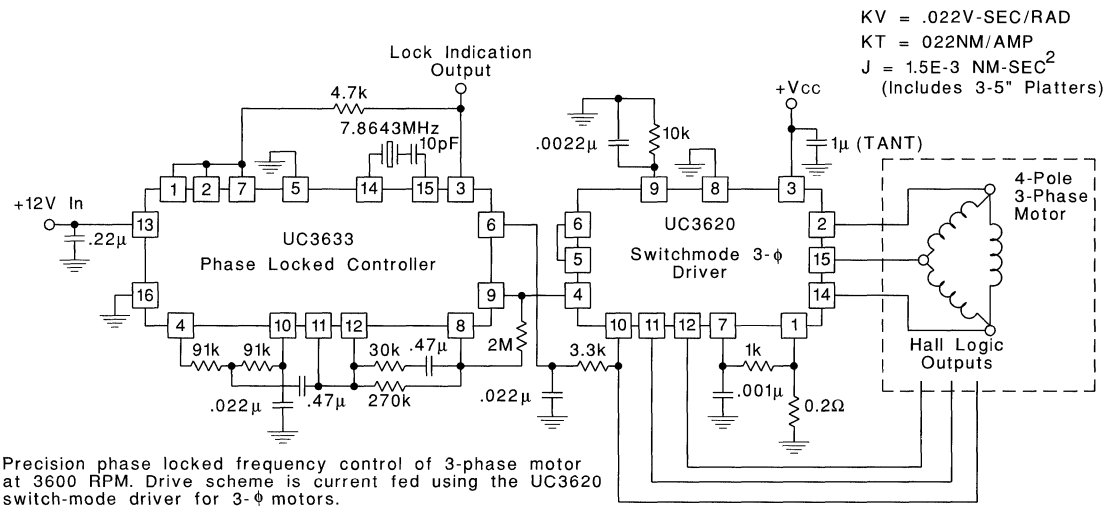
Reference Filter Design Aid - Phase Response



Variable is $1/\zeta^2$
(For R1=R2, $1/\zeta^2$=C1/C2)

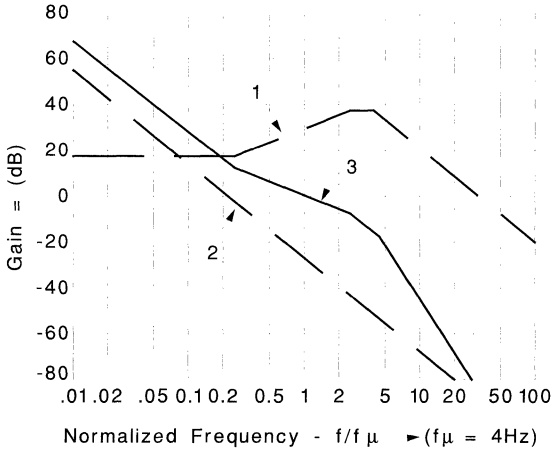
APPLICATION AND OPERATION INFORMATION

Design Example



Precision phase locked frequency control of 3-phase motor at 3600 RPM. Drive scheme is current fed using the UC3620 switch-mode driver for 3-ϕ motors.

Bode Plots - Design Example Open Loop Response



1.) $K_{LF}(s) \bullet K_{RF}(s)$

2.*) $\dfrac{N \bullet K\phi \bullet G_{PD} \bullet K_T}{s^2 \bullet J}$

3.) Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response
$K_{RF}(s)$ = Reference Filter Response
N = 4 (Using Double Edge Sensing With 4 Pole Motor)
$K\phi$ = Phase Detector Gain (.4V/RAD)
G_{PD} = Power Stage Transductance (1A/V)
K_T = Motor Torque Constant (.022NM/A)
J = Motor Moment of Inertia (.0015NM/A - SEC^2)
$s = 2\pi jf$

Note: For a current mode driver the electrical time constant, L_M / R_M, of the motor does not enter into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as **2 above, can be approximated by:*

$$\frac{N \bullet K\phi \bullet K_{PD} \bullet K_T}{s^2 \bullet J \bullet R_M} \quad \text{if: } R_M > K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T{}^2}{2\pi \bullet J \bullet R_M} < f < \frac{R_M}{2\pi \bullet L_M}$$

Here: K_{PD} = Voltage gain of Driver Stage
R_M = Motor Winding Resistance
L_M = Motor Winding Inductance

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application INFO available

UC1634
UC2634
UC3634

Phase Locked Frequency Controller

FEATURES

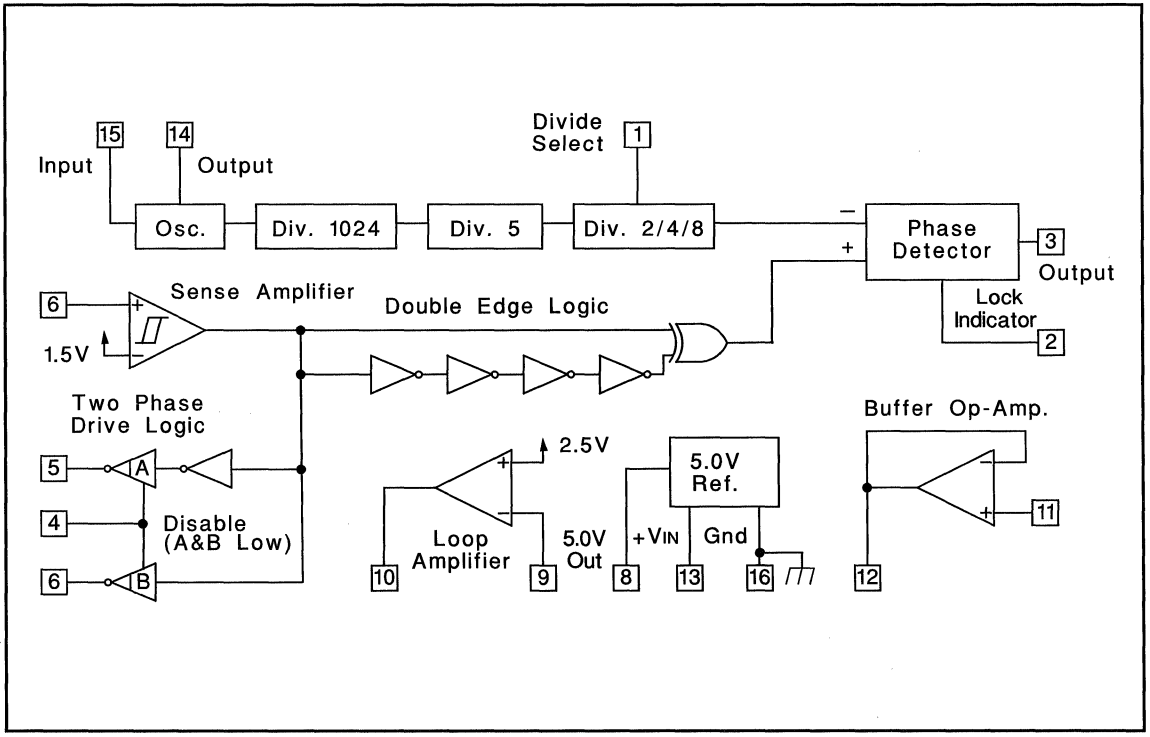
- Precision Phase Locked Frequency Control System
- Communication Logic for 2-Phase Motors
- Disable Input for Motor Inhibit
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

The UC1634 series of devices is optimized to provide precision phase locked frequency control for two phase DC brushless motors. These devices include most of the features of the general purpose UC1633 Phase Locked Control family and also provide the out-of-phase commutation signals required for driving two phase brushless motors. Only an external power booster stage is required for a complete drive and control system.

The two commutation outputs are open collector devices that can sink in excess of 16mA. A disable input allows the user to simultaneously force both of these outputs to an active low state. Double edge logic, following the sense amplifier, doubles the reference frequency at the phase detector by responding to both edges of the input signal at Pin 7.

BLOCK DIAGRAM



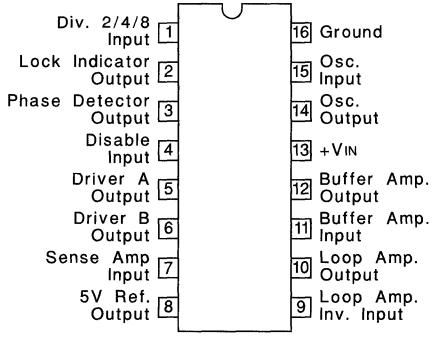
ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -.3V to +20V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltage ..... -.3V to +10V
Disable Input Voltage ..... -.3V to +10V
Oscillator Input Voltage ..... -.3V to +5V
Sense Amplifier Input Voltage ..... -.3V to +20V
Driver Output Currents ..... +30mA
Driver Output Voltages ..... +20V
Power Dissipation at T_A = 25°C(Note 2) 1000mW
Power Dissipation at T_C = 25°C (Note 2) 2000mW
Operating Junction Temperature ..... -55°C to +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

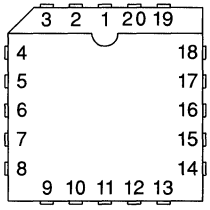
Note 1: Voltages are referenced to ground, (Pin 16, DIL Package). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
DIV 2/4/8	2
Lock Indicator Output	3
Phase Detector Output	4
Disable Input	5
N/C	6
Driver A Output	7
Driver B Output	8
Sense Amp Output	9
5V Ref Output	10
Loop Amp Inv Input	11
Loop Amp Output	12
Buffer Amp Input	13
Buffer Amp Output	14
+VIN	15
N/C	16
OSC Output	17
OSC Input	18
Ground	19
DIV 4/5 Input	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, $+V_{IN}$ = 12V. T_A=T_J.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$+V_{IN}$ = 15V		20	29	mA
Reference					
Output Voltage (V_{REF})		4.75	5.0	5.25	V
Load Regulation	I_{OUT} = 0mA to 7mA		5.0	20	mV
Line Regulation	$+V_{IN}$ = 8V to 15V		2.0	20	mV
Short Circuit Current	V_{OUT} = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator In to Oscillator Out	12	16	20	dB
Input DC Level (V_{IB})	Oscillator In Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	V_{IN} = V_{IB} ± 0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator In Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1V_{PP} at Oscillator In	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	µA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to +70°C for the UC3634, -25°C to + 85°C for the UC2634 and -55°C to +125°C for the UC1634, $+V_{IN}$ = 12V. T_A=T_J

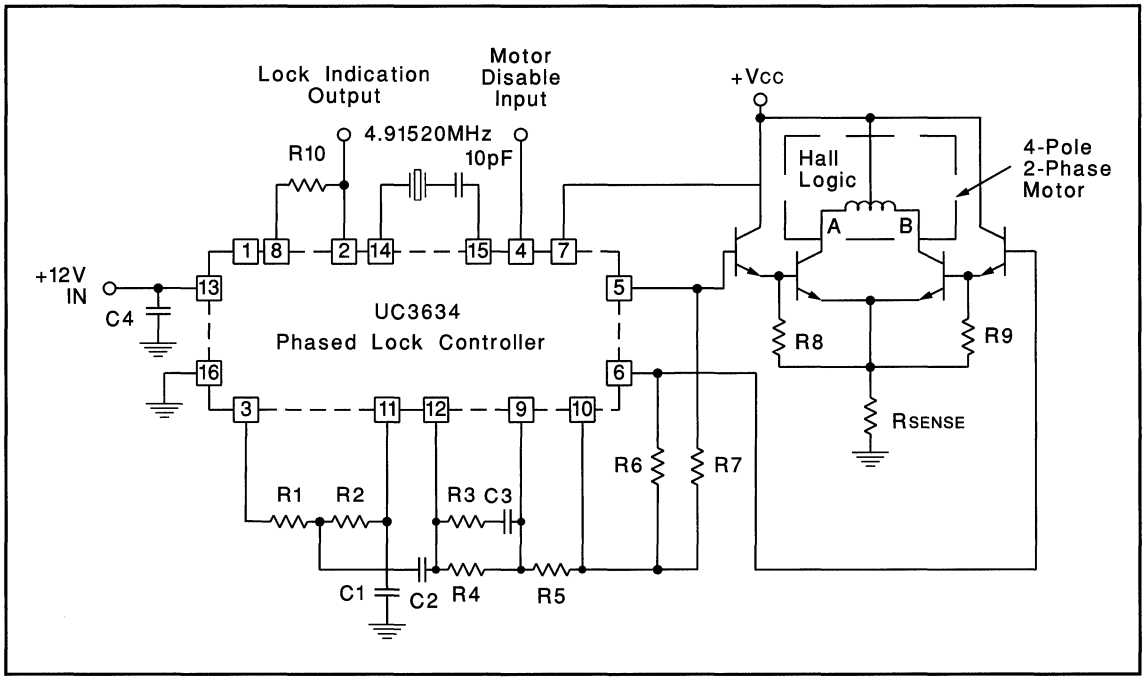
PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dividers (cont.)					
Div. 4/5 Input Threshold (Q Package Only, Note 4)		0.5	1.6	2.2	V
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	µA
	Input = 0V (Div. by 2)	-500	-150		µA
Div. 2/4/8 Open Current Voltage	Input Current = 0µA (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Two Phase Drive Outputs, A and B					
Saturation Voltage	I_{OUT} = 16mA		0.3	0.6	V
Leakage Current	V_{OUT} = 15V		0.1	5.0	µA
Disable Input					
Input Current	Input = 5V (Disabled, A and B Outputs Active Low)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase / Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase / Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase / Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} = 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Lock Indicator Output					
Saturation Voltage	Freq. Error, I_{OUT} = 5mA		0.3	0.45	V
Leakage Current	Zero Freq. Error, V_{OUT} = 15V		0.1	1.0	µA
Loop Amplifier					
N INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	$+V_{IN}$ = 8V to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA
Buffer Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.
Note 4: This part is also available in a 20 pin plastic leadless chip carrier, Q designator, where a divide by 4/5 select pin is available. Consult factory for details.

APPLICATION AND OPERATION INFORMATION (For additional information see UC1633 data sheet)

Design Example:

Precision phased locked frequency control of a 2-phase motor at 3600 RPM. Using the commutation logic on the UC3634, a simple discrete drive scheme is possible.



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UC1635
UC2635
UC3635

Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Separate Divider Outputs and Phase Detector Input Pins
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op Amps
- 5V Reference Output

DESCRIPTION

The UC1635 family of integrated circuits was designed for use in precision speed control of DC motors. An extension to the UC1633 line of phase locked controllers, these devices provide access to both of the digital phase detector's inputs, and include a reference frequency divider output pin. With this added flexibility, this family of controllers can be used to obtain phase synchronization of multiple motors.

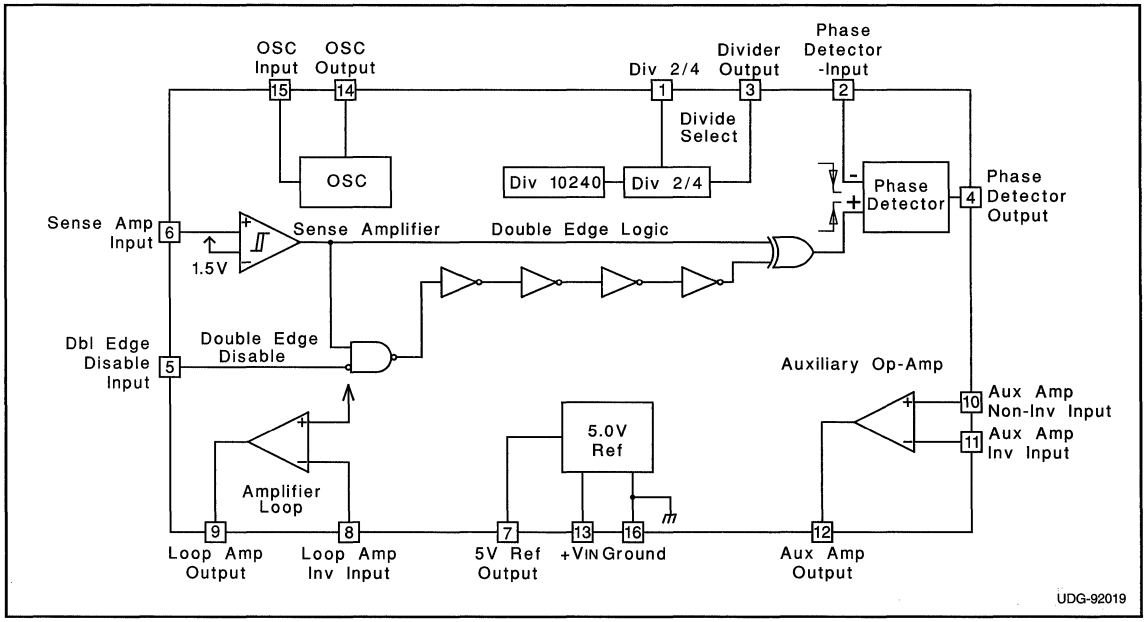
A reference frequency can be generated using the device's crystal oscillator and programmable dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector responds proportionally to the phase error between the detector's minus input pin and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of these op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A 5V reference output can be used to accurately set DC operating levels.

BLOCK DIAGRAM



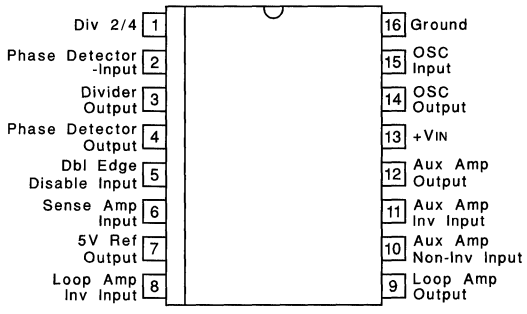
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN) ..... +20V
Reference Output Current ..... -30mA
Op-Amp Output Currents ..... ±30mA
Op-Amp Input Voltages ..... -0.3 to +20V
Phase Detector Input Voltage ..... -0.3V to +5V
Phase Detector Output Current ..... ±10mA
Lock Indicator Output Current ..... +15mA
Lock Indicator Output Voltage ..... +20V
Divide Select Input Voltages ..... -0.3V to +10V
Double Edge Disable Input Voltage ..... -0.3V to +10V
Oscillator Input Voltage ..... -0.3V to +5V
Sense Amplifier Input Voltage ..... -0.3V to +20V
Power Dissipation at TA = 25°C, (Note 2) 1000mW
Power Dissipation at TC = 25°C, (Note 2) 2000mW
Operating Junction Temperature ..... -55° to 150°C
Storage Temperature ..... -65° to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C

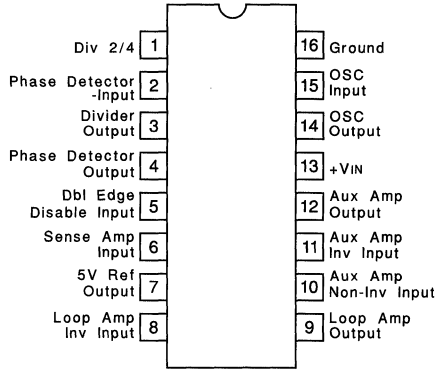
Note 1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.
Note 2: Consult Unitrode Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

CONNECTION DIAGRAMS

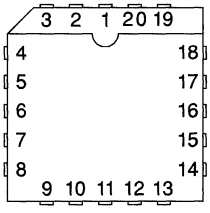
SOIC–16 (Top View)
DW Package



DIL–16 (Top View)
J & N Packages



PLCC-20 & LCC-20
(Top View)
Q & L Packages



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Div 2/4	2
Phase Detector Input	3
Divider Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, specifications hold for TA = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +VIN = 12V. TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0 to 7mA		5.0	20	mV
Line Regulation	+VIN = 8 to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	15	35		mA

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (VIB)	Oscillator Input Pin Open, T_J = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 2)	V_{IN} = V_{IB} ±0.5V, T_J = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, T_J = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1Vpp at Oscillator Input	10			MHz
Div 2/4 Input Current	Input = 5V (Div. by 2)		150	500	µA
	Input = 0V (Div. by 4)	-5.0	0.0	5.0	µA
Div 2/4 Threshold		0.5	1.6	2.2	V
Divider Output	High Level (w/6.8k Load to GND)	4.0	4.5		V
	Low Level (Open Collector Leakage)			10	µA
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		µA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	µA
	Input = 0V (Enabled)	-5.0	0.0	5.0	µA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
-Input Threshold	Detector Responds to Falling Edge	0.5	1.6	2.2	V
-Input Current	Input = 2.2V		100	250	µA
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	V_{OUT} = 4.3V	2.0	8.0		mA
Low Level Maximum Sink Current	V_{OUT} 0.7V	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	I_{OUT} = -200 to +200µA, T_J = 25°C	4.5	6.0	7.5	kΩ
Loop Amplifier					
Non-Inv Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		µA
AVOL		60	75		dB
PSRR	+V_{IN} = 8 to 15V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

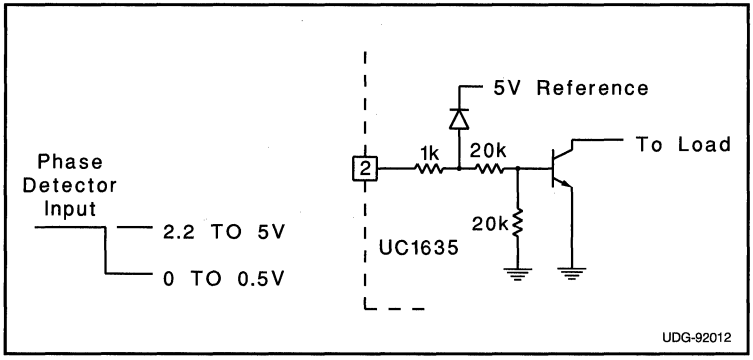
Note 3: These impedance levels will vary with T_J at about 1700ppm/°C.

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise stated, specifications hold for T_A = 0°C to +70°C for the UC3635, -25°C to +85°C for the UC2635 and -55°C to +125°C for the UC1635, +Vin = 12V. $T_A = T_J$.

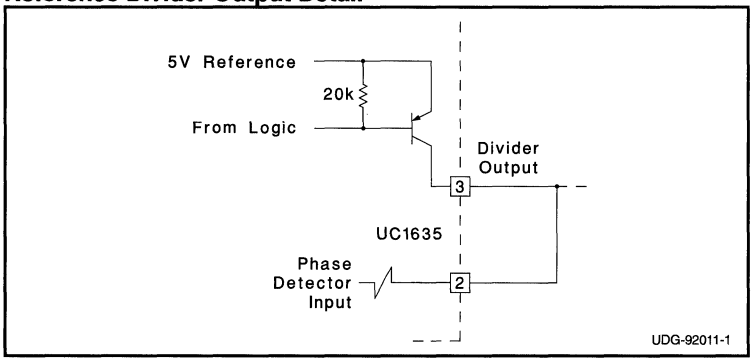
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auxiliary Op-Amp					
Input Offset Voltage	V_{CM} = 2.5V			8	mV
Input Bias Current	V_{CM} = 2.5V	-0.8	-0.2		µA
Input Offset Current	V_{CM} = 2.5V		.01	0.1	µA
AVOL		70	120		dB
PSRR	$+V_{IN}$ = 8 to 15V	70	100		dB
CMRR	V_{CM} = 0 to 10V	70	100		dB
Short Circuit Current	Source, V_{OUT} = 0V	16	35		mA
	Sink, V_{OUT} = 5V	16	30		mA

Application and Operation Information
(For Additional Application Information see the UC1633 Data Sheet)
(Pin numbers refer to DIL and SOIC packages)

Phase Detector Input Detail



Reference Divider Output Detail



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application INFO available

UC1637
UC2637
UC3637

Switched Mode Controller for DC Motor Drive

FEATURES

- Single or Dual Supply Operation
- ±2.5V to ±20V Input Supply Range
- ±5% Initial Oscillator Accuracy; ± 10% Over Temperature
- Pulse-by-Pulse Current Limiting
- Under-Voltage Lockout
- Shutdown Input with Temperature Compensated 2.5V Threshold
- Uncommitted PWM Comparators for Design Flexibility
- Dual 100mA, Source/Sink Output Drivers

DESCRIPTION

The UC1637 is a pulse width modulator circuit intended to be used for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. When used to replace conventional drivers, this circuit can increase efficiency and reduce component costs for many applications. All necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

This monolithic device contains a sawtooth oscillator, error amplifier, and two PWM comparators with ±100mA output stages as standard features. Protection circuitry includes under-voltage lockout, pulse-by-pulse current limiting, and a shutdown port with a 2.5V temperature compensated threshold.

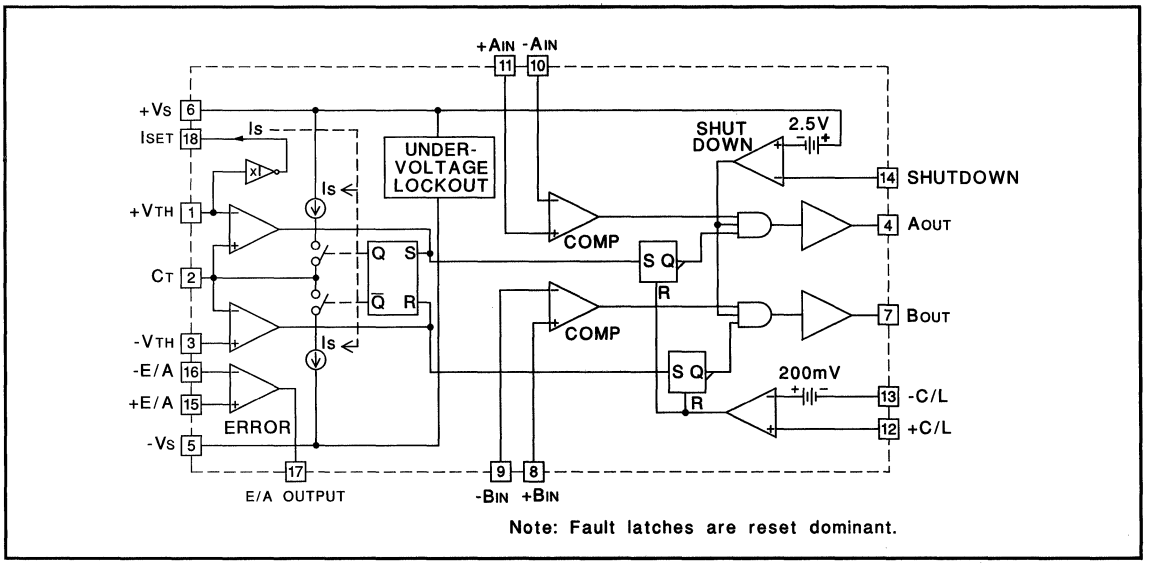
The UC1637 is characterized for operation over the full military temperature range of -55°C to +125°C, while the UC2637 and UC3637 are characterized for -25°C to +85°C and 0°C to +70°C, respectively.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (±Vs)	±20V
Output Current, Source/Sink (Pins 4, 7)	500mA
Analog Inputs (Pins 1, 2, 3, 8, 9, 10, 11 12, 13, 14, 15, 16)	±Vs
Error Amplifier Output Current (Pin 17)	±20mA
Oscillator Charging Current (Pin 18)	-2mA
Power Dissipation at T_A = 25°C (Note 2)	1000mW
Power Dissipation at T_C = 25°C (Note 2)	2000mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	+300°C

Note 1: Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

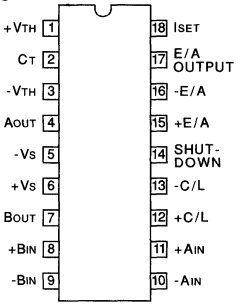
BLOCK DIAGRAM



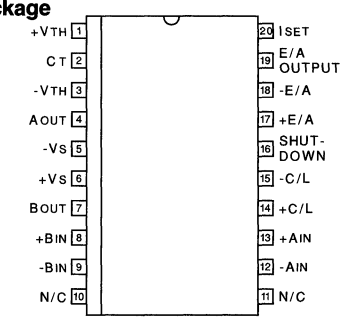
Note: Fault latches are reset dominant.

CONNECTION DIAGRAM

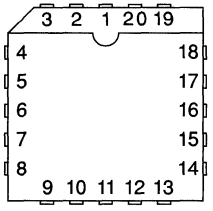
DIL-18 (TOP VIEW)
J or N Package



SOIC-20 (TOP VIEW)
DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
+VTH	1
CT	2
-VTH	3
AOUT	4
-VS	5
N/C	6
+VS	7
BOUT	8
+BIN	9
-BIN	10
-AIN	11
+AIN	12
+C/L	13
-C/L	14
SHUTDOWN	15
N/C	16
+E/A	17
-E/A	18
E/A OUTPUT	19
ISET	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637; +Vs = +15V, -Vs = - 15V, +VTH = 5V, -VTH = -5V, RT = 16.7kΩ, CT = 1500pF, TA=TJ.

PARAMETER	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator								
Initial Accuracy	T_J = 25°C (Note 6)	9.4	10	10.6	9	10	11	kHz
Voltage Stability	Vs = ±5V to ±20V, VPIN 1 = 3V, VPIN 3 = -3V		5	7		5	7	%
Temperature Stability	Over Operating Range (Note 3)		0.5	2		0.5	2	%
+VTH Input Bias Current	VPIN 2 = 6V	-10	0.1	10	-10	0.1	10	µA
-VTH Input Bias Current	VPIN 2 = 0V	-10	-0.5		-10	-0.5		µA
+VTH, -VTH Input Range		+Vs-2		-Vs+2	+Vs-2		-Vs+2	V
Error Amplifier								
Input Offset Voltage	VCM = 0V		1.5	5		1.5	10	mV
Input Bias Current	VCM = 0V		0.5	5		0.5	5	µA
Input Offset Current	VCM = 0V		0.1	1		0.1	1	µA
Common Mode Range	Vs = ±2.5 to 20V	-Vs+2		+Vs	-Vs+2		+Vs	V
Open Loop Voltage Gain	RL = 10k	75	100		80	100		dB
Slew Rate			15			15		V/µs
Unity Gain Bandwidth			2			2		MHz
CMRR	Over Common Mode Range	75	100		75	100		dB
PSRR	Vs = ±2.5 to ±20V	75	110		75	110		dB

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1637; -25°C to +85°C for the UC2637; and 0°C to +70°C for the UC3637: V_S = +15V, $-V_S$ = - 15V, $+V_{TH}$ = 5V, $-V_{TH}$ = -5V, R_T = 16.7kΩ, C_T = 1500pF, T_A=T_J.

PARAMETERS	TEST CONDITIONS	UC1637/UC2637			UC3637			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier (Continued)								
Output Sink Current	$V_{PIN\ 17}$ = 0V		-50	-20		-50	-20	mA
Output Source Current	$V_{PIN\ 17}$ = 0V	5	11		5	11		mA
High Level Output Voltage		13	13.6		13	13.6		V
Low Level Output Voltage			-14.8	-13		-14.8	-13	V
PWM Comparators								
Input Offset Voltage	V_{CM} = 0V		20			20		mV
Input Bias Current	V_{CM} = 0V		2	10		2	10	µA
Input Hysteresis	V_{CM} = 0V		10			10		mV
Common Mode range	V_S = ±5V to ±20V	-Vs+1		+Vs-2	-Vs+1		+Vs-2	V
Current Limit								
Input Offset Voltage	V_{CM} = 0V, T_J = 25°C	190	200	210	180	200	220	mV
Input Offset Voltage T.C.			-0.2			-0.2		mV/°C
Input Bias Current		-10	-1.5		-10	-1.5		µA
Common Mode Range	V_S = ±2.5V to ±20V	-Vs		+Vs-3	-Vs		+Vs-3	V
Shutdown								
Shutdown Threshold	(Note 4)	-2.3	-2.5	-2.7	-2.3	-2.5	-2.7	V
Hysteresis			40			40		mV
Input Bias Current	$V_{PIN\ 14}$ = +Vs to -Vs	-10	-0.5		-10	-0.5		µA
Under-Voltage Lockout								
Start Threshold	(Note 5)		4.15	5.0		4.15	5.0	V
Hysteresis			0.25			0.25		mV
Total Standby Current								
Supply Current			8.5	15		8.5	15	mA
Output Section								
Output Low Level	I_{SINK} = 20mA		-14.9	-13		-14.9	-13	V
	I_{SINK} = 100mA		-14.5	-13		-14.5	-13	
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 100mA	12	13.5		12	13.5		
Rise Time	(Note 3) C_L = Inf, T_J = 25°C		100	600		100	600	ns
Fall Time	(Note 3) C_L = Inf, T_J = 25°C		100	300		100	300	ns

Note 3: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 4: Parameter measured with respect to +Vs (Pin 6).
Note 5: Parameter measured at +Vs (Pin 6) with respect to -Vs (Pin 5).
Note 6: R_T and C_T referenced to Ground.

FUNCTIONAL DESCRIPTION

Following is a description of each of the functional blocks shown in the Block Diagram.

Oscillator

The oscillator consists of two comparators, a charging and discharging current source, a current source set terminal, I_{SET} and a flip-flop. The upper and lower threshold of the oscillator waveform is set externally by applying a voltage at pins $+V_{TH}$ and $-V_{TH}$ respectively. The $+V_{TH}$ terminal voltage is buffered internally and also applied to the I_{SET} terminal to develop the capacitor charging current through R_T. If R_T is referenced to $-V_S$ as shown in Figure 1, both the threshold voltage and charging current will vary proportionally to the supply differential, and the oscillator frequency will remain constant. The triangle waveform oscillators frequency and voltage amplitude is determined by the external components using the formulas given in Figure 1.

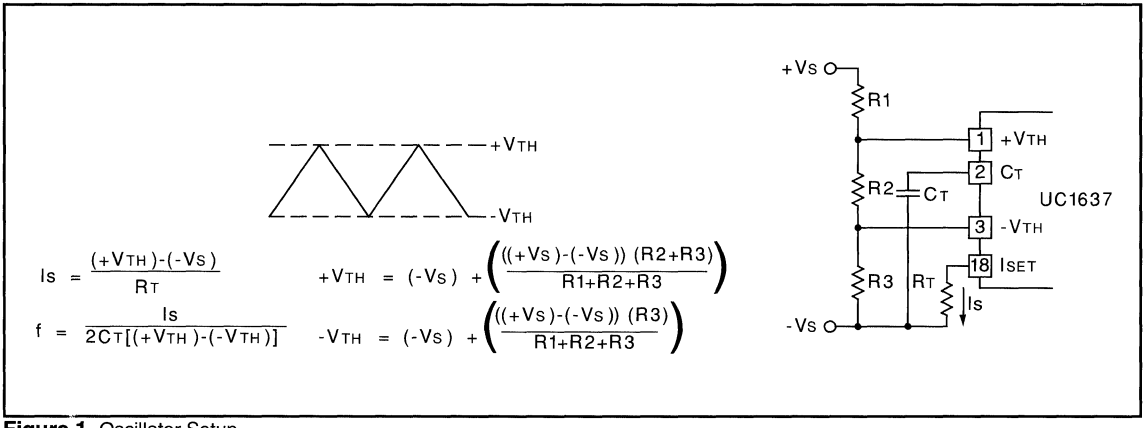


Figure 1. Oscillator Setup

PWM Comparators

Two comparators are provided to perform pulse width modulation for each of the output drivers. Inputs are uncommitted to allow maximum flexibility. The pulse width of the outputs A and B is a function of the sign and amplitude of the error signal. A negative signal at Pin 10 and 8 will lengthen the high state of output A and shorten the high state of output B. Likewise, a positive error signal reverses the procedure. Typically, the oscillator waveform is compared against the summation of the error signal and the level set on Pin 9 and 11.

MODULATION SCHEMES

Case A Zero Deadtime (Equal voltage on Pin 9 and Pin 11)
In this configuration, maximum holding torque or stiffness and position accuracy is achieved. However, the power input into the motor is increased. Figure 3A shows this configuration.

Case B Small Deadtime (Voltage on Pin 9 > Pin 11)
A small differential voltage between Pin 9 and 11 provides the necessary time delay to reduce the chances of momentary short circuit in the output stage during transitions, especially where power-amplifiers are used. Refer to Figure 3B.

Case C Increased Deadtime and Deadband Mode
(Voltage on Pin 9 > Pin 11)
With the reduction of stiffness and position accuracy, the power input into the motor around the null point of the servo loop can be reduced or eliminated by widening the window of the comparator circuit to a degree of acceptance. Where position accuracy and mechanical stiffness is unimportant, deadband operation can be used. This is shown in Figure 3C.

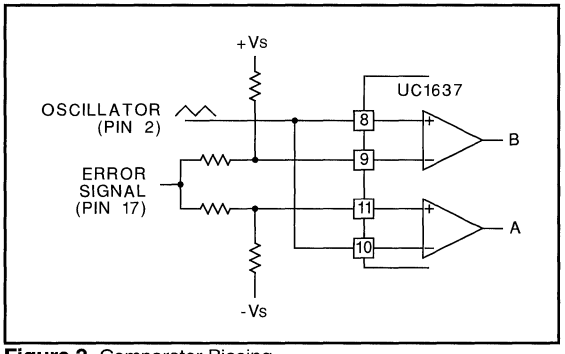


Figure 2. Comparator Biasing

Output Drivers

Each output driver is capable of both sourcing and sinking 100mA steady state and up to 500mA on a pulsed basis for rapid switching of either POWERFET or bipolar transistors. Output levels are typically -VS + 0.2V @50mA low level and +VS - 2.0V @50mA high level.

Error Amplifier

The error amplifier consists of a high slew rate (15V/µs) op-amp with a typical 1MHz bandwidth and low output impedance. Depending on the ±VS supply voltage, the common mode input range and the voltage output swing is within 2V of the VS supply.

Under-Voltage Lockout

An under-voltage lockout circuit holds the outputs in the low state until a minimum of 4V is reached. At this point, all internal circuitry is functional and the output drivers are enabled. If external circuitry requires a higher starting voltage, an over-riding voltage can be programmed through the shutdown terminal as shown in Figure 4.

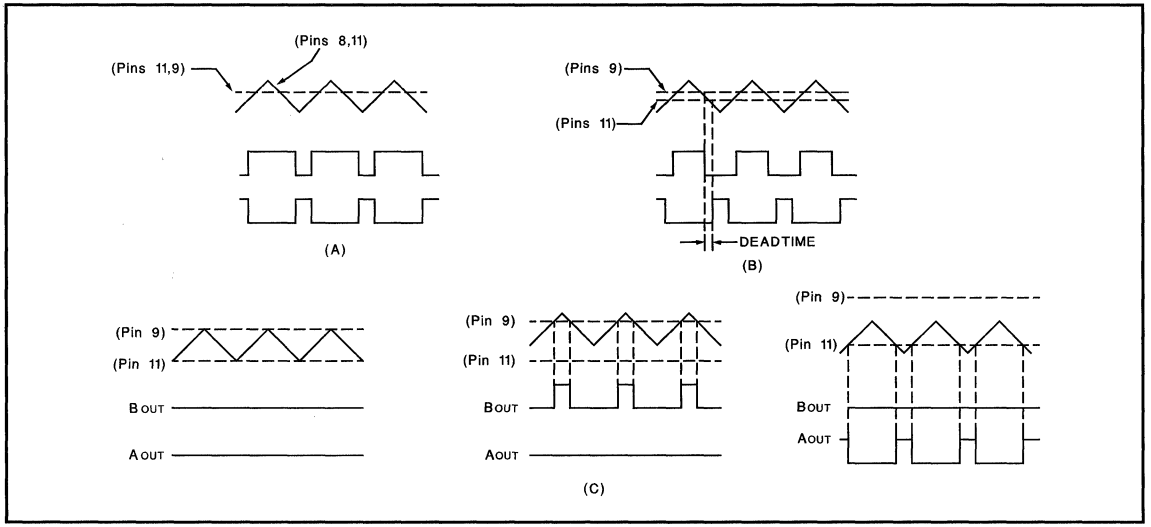


Figure 3. Modulation Schemes Showing (A) Zero Deadtime (B) Deadtime and (C) Deadband Configurations

Shutdown Comparator

The shutdown terminal may be used for implementing various shutdown and protection schemes. By pulling the terminal more than 2.5V below VIN, the output drivers will be enabled. This can be realized using an open collector gate or NPN transistor biased to either ground or the negative supply. Since the threshold is temperature stabilized, the comparator can be used as an accurate low voltage lockout (Figure 4) and/or delayed start as in Figure 5. In the shutdown mode the outputs are held in the low state.

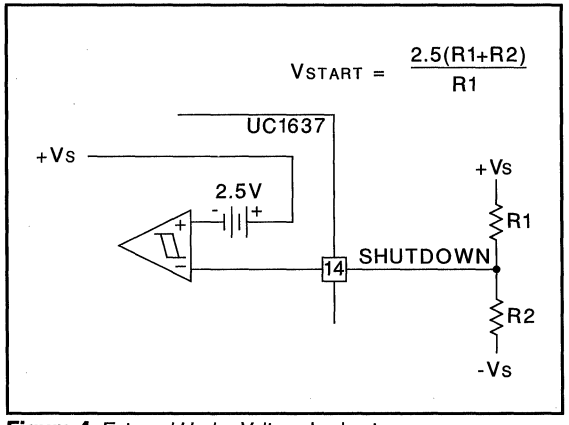


Figure 4. External Under-Voltage Lockout

Current Limit

A latched current limit amplifier with an internal 200mV offset is provided to allow pulse-by-pulse current limiting. Differential inputs will accept common mode signals from -Vs to within 3V of the +Vs supply while providing excellent noise rejection. Figure 6 shows a typical current sense circuit.

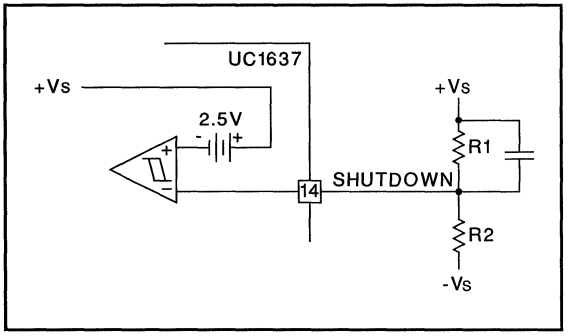


Figure 5. Delayed Start-Up

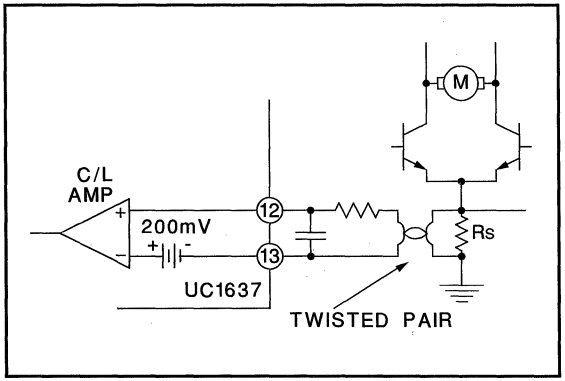


Figure 6. Current Limit Sensing

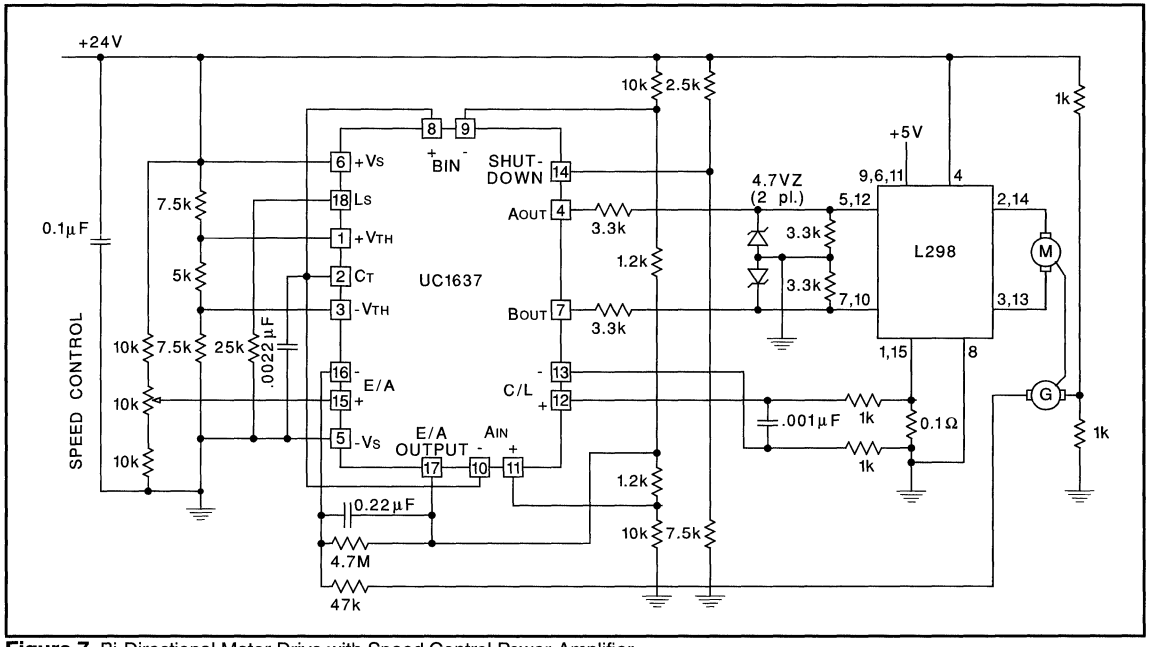


Figure 7. Bi-Directional Motor Drive with Speed Control Power-Amplifier

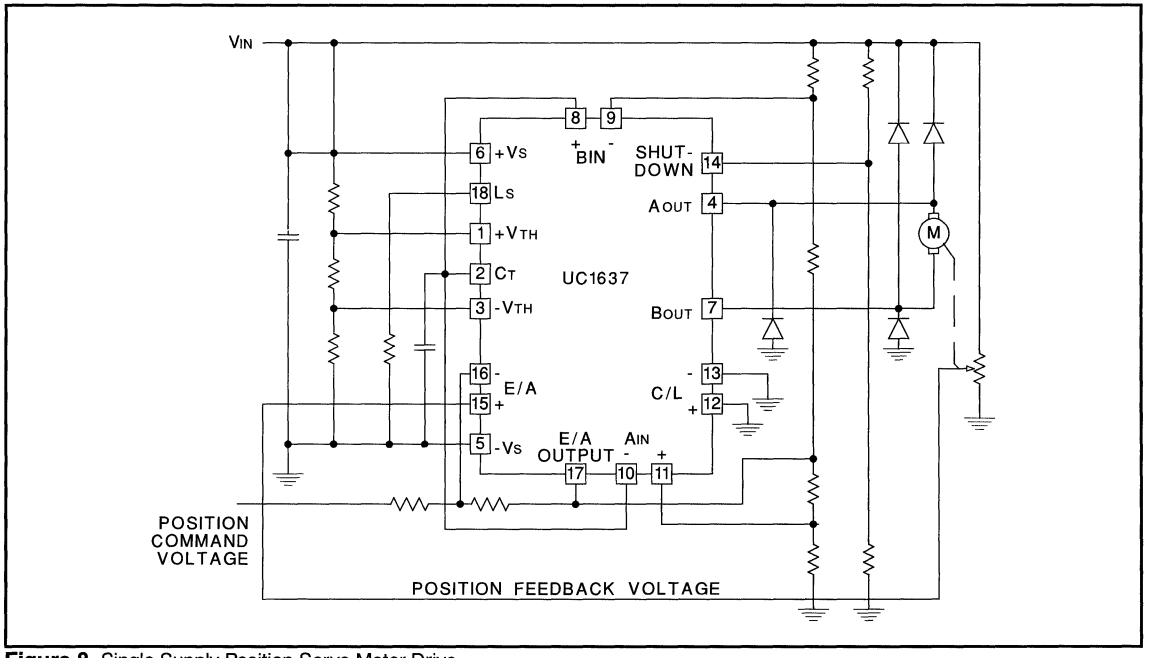


Figure 8. Single Supply Position Servo Motor Drive

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UC1638
UC2638
UC3638

Advanced PWM Motor Controller

FEATURES

- Single or Dual Supply Operation
- Accurate High Speed Oscillator
- Differential X5 Current Sense Amplifier
- Bidirectional Pulse-by-Pulse Current Limiting
- Programmable Oscillator Amplitude and PWM Deadband
- Dual 500mA Totem Pole Output Drivers
- Dual 60V, 50mA Open Collector Drivers
- Undervoltage Lockout

DESCRIPTION

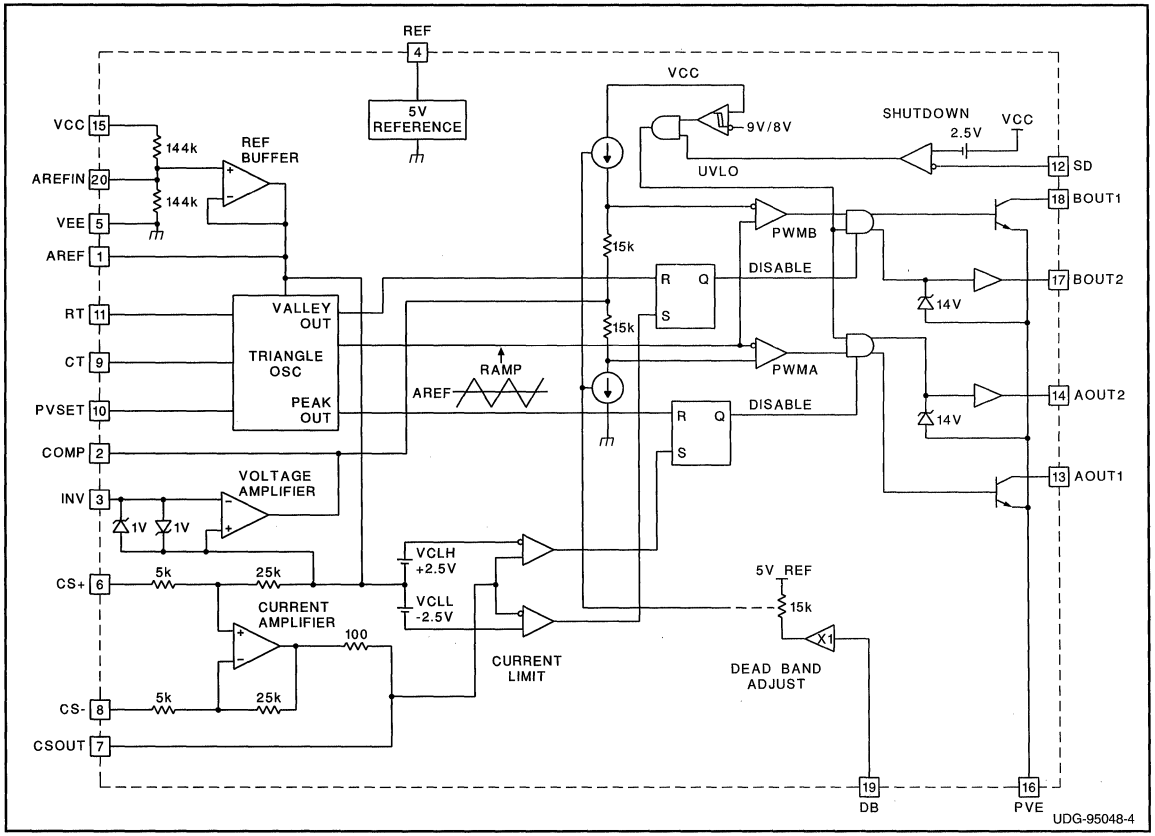
The UC1638 family of integrated circuits are advanced pulse width modulators intended for a variety of PWM motor drive and amplifier applications requiring either uni-directional or bi-directional drive circuits. Similar in architecture to the UC1637, all necessary circuitry is included to generate an analog error signal and modulate two bi-directional pulse train outputs in proportion to the error signal magnitude and polarity.

Key features of the UC1638 include a programmable high speed triangle oscillator, a 5X differential current sensing amplifier, a high slew rate error amplifier, high speed PWM comparators, and two 50mA open collector as well as two ±500mA totem pole output stages. The individual circuit blocks are designed to provide practical operation to switching frequencies of 500kHz.

Significant improvements in circuit speed, elimination of many external programming components, and the inclusion of a differential current sense amplifier, allow this controller to be specified for higher performance applications, yet maintain the flexibility of the UC1637. The current sense amplifier in conjunction with the error amplifier can be configured for average current feedback. The additional open collector outputs provide a drive sig-

continued

BLOCK DIAGRAM



DESCRIPTION (cont.)

nal for the highside switches in a full bridge configuration. The programmable AREFIN pin allows for single or dual supply operation. Oscillator ramp amplitude and PWM deadband are programmable by tapping a voltage divider off the 5V reference to the appropriate programming input (PVSET or DB).

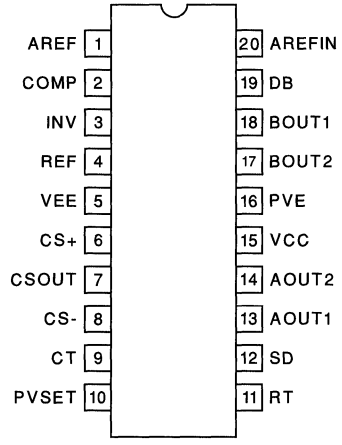
Additional features include a precision externally available 5V reference, undervoltage lockout, pulse-by-pulse peak current limiting, and a remote shutdown port. The UC1638 family is available in the 20 pin N, DW and J packages. Consult the factory for other packaging options.

ABSOLUTE MAXIMUM RATINGS

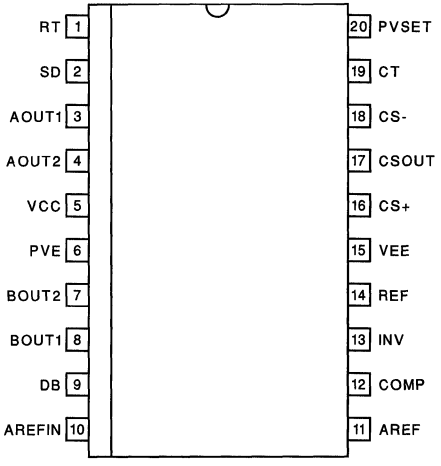
Supply Voltage VCC (referenced to VEE) 40V
Output Drivers (AOUT2, BOUT2)
Currents (continuous) . . . . . ±0.25A
Currents (peak) . . . . . ±500mA
REF Output Current . . . . . Internally Limited
PVSET, DB, RT, INV, REF, CSOUT . . . . . 0.3 to 10V
CS+, CS- . . . . . VEE–1V to VCC
CT, AREF, AREFIN, COMP, SD . . . . . VEE – 0.3
Output Voltage (AOUT1, BOUT1) 60V
Storage temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead temperature (soldering, 10 sec.) . . . . . +300°C
Currents are positive into, negative out of the specified terminal. Consult packaging section of data book for thermal limitation considerations of packages.

CONNECTION DIAGRAMS

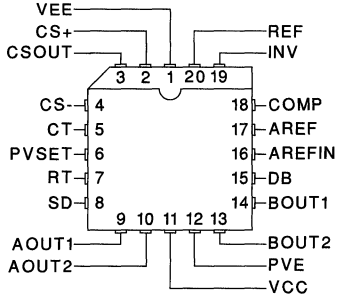
DIL-20 (Top View)
N or J Package



SOIC-20 (Top View)
DW Package



PLCC-20 (Top View)
Q Package



ELECTRICAL CHARACTERISTICS

Unless otherwise specified; VCC = 15V, VEE =–15V, CT = 680pF, RT = 3k, V_{PVSET} = 1.5V, V_{COMP} = 0V, V_{CSOUT} = 0V, V_{DB} = REF, V_{EXTREF} = 0V, V_{SD} = VCC – 3V, T_A = 55°C to 125°C for the UC1638, 25°C to 85°C for the UC2638, 0°C to 70°C for the UC3638. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overall					
Supply Current, Operating			15	23	mA
UVLO Threshold	Reference to VEE		9	10	V
UVLO Hysteresis	Reference to VEE		1		V
Voltage Amplifier					
Input Offset Voltage	COMP = 0V	15	0	15	mV
V_{SENSE} Bias Current		0	0.5	2	µA
Open Loop Gain	COMP = 5V to +5V	75	100		dB
CMRR	V_{CM} = 5V to +5V	70	100		dB
PSRR	VCM = 0V, VCC VEE = 10V to 36V	70	90		dB
V_{OUT} High	INV = 0.1V, RL = 10k	13	13.6		V
V_{OUT} Low	INV = +0.1V, RL = 10k		13.8	–13	V
Slew Rate Rising and Falling	Overdrive = 1V		12		V/µs
Output Source Current	COMP Shorted to VEE	5	15		mA
Output Sink Current	COMP Shorted to VCC	15	40		mA
Gain Bandwidth Product	F_{IN} = 100kHz, 10mV p-p	1	5		MHz
5V Reference					
Output Voltage	I_{REF} = 1mA, T_A = 25°C	4.925	5	5.075	V
Output Voltage	I_{REF} = 1mA	4.875	5	5.125	V
Load Regulation	I_{REF} = 1mA to 10mA	15	2	15	mV
Line Regulation	VCC - VEE = 10V to 36V	15	2	15	mV
Short Circuit Current	V_{REF} = 0V	15	70		mA
Oscillator					
Initial Accuracy	T_A = 0°C – 70°C	86	98	110	kHz
Voltage Stability	VCC VEE = 10V to 36V		2		%
Total Variation	Line, Temperature	76	98	120	kHz
PVSET Input Bias Current			0.5	3	µA
PVSET Input Voltage Range	(Note 1)	0.5		VREF	V
Amplitude Limit	(Note 1)	VEE+3		VCC 3	V
AOUT1, BOUT1 Output Drivers					
Output Low Voltage	I_{OUT} = 1mA, Ref. to PVE, PVE = 0V		0.9	1.3	V
	I_{OUT} = 50mA		1.2	1.8	V
Leakage Current	Output Voltage = 50V		0.1	50	µA
AOUT2, BOUT2 Output Drivers					
Output High Voltage	I_{OUT} = 20mA, Ref. to PVE, PVE = 0V	12.2	13.5		V
	I_{OUT} = 100mA, Ref. to PVE, PVE = 0V	12	13.5		V
Output High Clamp Level	I_{OUT} = 20mA, Ref. to PVE, PVE = VEE		14.4	16.5	V
Output Low Voltage	I_{OUT} = 20mA, Ref. to PVE, PVE = 0V		0.4	1	V
	I_{OUT} = 100mA, Ref. to PVE, PVE = 0V		0.6	2.2	V
Output Rise Time	C_{OUT} = 1nF		50	100	ns
Output Fall Time	C_{OUT} = 1nF		50	100	ns

(continued)
ELECTRICAL CHARACTERISTICS

Unless otherwise specified; VCC = 15V, VEE =–15V, CT = 680pF, RT = 3k, V_{PVSET} = 1.5V, V_{COMP} = 0V, V_{CSOUT} = 0V, V_{DB} = REF, V_{EXTREF} = 0V, V_{SD} = VCC – 3V, T_A = –55°C to 125°C for the UC1638, –25°C to 85°C for the UC2638, 0°C to 70°C for the UC3638. T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
X5 Amplifier					
Gain	V_{ID} = 100mV to 400mV	4.75	5	5.25	V/V
Common Mode Rejection	V_{CS+}, V_{CS-} = AREF ±5V	50	65		dB
–3dB Bandwidth		300	400		kHz
Slew Rate Rising		.75	1.5		V/µs
Slew Rate Falling		.75	1.5		V/µs
Shutdown					
Threshold	Ref. to VCC	– 1.9	– 2.25	– 2.5	V
Input Bias Current	V_{SD} = SD Threshold		–0.5	–10	µA
Current Limit					
Threshold Positive	Measured Between CS+ and CS-	400	500	600	mV
Threshold Negative	Measured Between CS+ and CS-	– 600	– 500	– 400	mV
Propagation Delay to Outputs	Overdrive = 200mV		150	250	ns
Deadband Adjust					
Maximum Deadband	V_{DB} = 0V		±5		V
Zero Deadband	V_{DB} = REF		0		V
Deadband Adjustment Gain	V_{DB} = 1V to 4V (Note 2)	± 0.9	± 1	± 1.2	V/V
Input Bias Current	V_{DB} = VREF		3	15	µA
AREF Buffer					

Note 1: Oscillator triangle amplitude = 2.5 • PV ±AREF.

Note 2: Deadband = ±(REF – DB), referenced to COMP.

Note 3: Offset = AREFIN – AREF.

8

PIN DESCRIPTIONS

AOUT1, BOUT1: AOUT1 and BOUT1 are open collector output drivers capable of sinking 50mA. These outputs can be pulled up to 60V maximum. With a few external components, these outputs can drive the opposite high side switches in a full bridge arrangement.

AOUT2, BOUT2: AOUT2 and BOUT2 are totem pole output drivers capable of driving external power MOSFETs directly. The peak current ratings are ±500mA. An integrated zener clamp limits the drive output amplitude to approximately 14V to prevent MOSFET gate oxide overstress. These outputs are configured to drive the opposite low side switches in a full bridge arrangement.

AREF: The voltage on AREF is simply a buffered version of the voltage on AREFIN. In single supply applications, AREF should be bypassed to VEE with a 0.1µF ceramic capacitor to provide a stable reference level for the internal circuitry.

AREFIN: The voltage on AREFIN is generated internally by a 50% voltage divider tied between VCC and VEE. As such, it provides the mid supply reference needed for the oscillator, voltage amplifier, current amplifier and current limit comparators when operating in single supply mode. A buffer amplifier is connected between AREFIN and AREF. In bipolar supply applications AREFIN is usually connected to VEE, which disables the buffer amplifier, and AREF is connected to 0V.

COMP: This is the output of the high slew rate error amplifier. The level on COMP modulates the controller duty cycle via the PWM comparators and the oscillator ramp. Compensation and DC gain setting resistors are connected between COMP and INV.

CS-: This is the inverting input to the X5 current sense amplifier. The common mode input range for this pin ex-

PIN DESCRIPTIONS (cont.)

tends from VEE–1V to VCC–4V. A low value resistor in series with the source or emitter of the low side switch in the full bridge develops the signal that is applied to this pin. At differential inputs of ±500mV typical (referenced to CS+)the controller reaches the current limit level, which truncates the output pulse.

CS+: This is the non-inverting input to the X5 current sense amplifier. The common mode input range for this pin extends from VEE–1V to VCC–4V. The characteristics for this pin are identical to CS-.

CSOUT: This is the output of the X5 current sense amplifier. Voltage levels greater than ±2.5V referenced to AREF will cause the device to enter current limit. An internal 100 ohm resistor between the amplifier output and CSOUT is provided to create a high frequency noise filter with an external capacitor to VEE. When used for average current feedback, CSOUT is summed into INV.

CT: A capacitor from CT to VEE will set the triangle oscillator frequency according to the following equation:

$$F = \frac{1}{5 \bullet RT \bullet CT}$$

The waveform on CT is symmetrical about the voltage on AREF and is applied internally to the inputs of hte PWM comparators. Use a high quality ceramic capacitor with low ESL and ESR for best results. A minimum CT value of 200 pF insures good accuracy and less susceptibility to circuit layout parasitics. The oscilator and PWM are designed to provide practical operation to 500kHz.

DB: This high impedance input programs output pulse train deadtime. A stable DC voltage between 0V and REF will set a bi-directional deadband centered about the level on COMP. The deadband level is equal to: 5V – VDB. That is, 1V on DB will program ±4V of deadband centered about the COMP pin level. A convenient method for generating the programming level is a voltage divider tap off of REF.

INV: This is the inverting input to the Voltage amplifier. The common mode input range for this pin extends from VEE+2V to VCC–1V. It can be tied to a command signal generated by a rate feedback element or to a position control signal. In average current feedback applications, this input is tied to the output of the X5 current sensing amplifier (CSOUT).

PVE: This is the high current ground for the IC. The external MOSFET driver transistors are referenced to this ground. Internal level shifting circuitry gives the option of tying this pin to VEE, or the system ground in split supply applications.

PVSET: A DC voltage on PVSET programs the upper and lower thresholds for the oscillator by the following relationship:

$$V_{PK} - V_{VLY} = 5 \bullet V_{PVSET}.$$

The input voltage range on PVSET is 0.5V to REF.

REF: REF is the output of the precision reference. The output is capable of supplying 15mA to peripheral circuitry and is internally short circuit current limited. Bypass REF to VEE with a 0.1µF ceramic capacitor for best performance.

RT: A single resistor from RT to VEE sets the charging and discharging currents for the triangle oscillator. The actual charge and discharge is 2X the current programmed by RT and PVSET. For best performance the current out of RT should be limited to 1mA. The voltage level on the RT pin is a buffered version of the PVSET pin voltage. Therefore, if the PVSET voltage divider is tied between VCC and VEE to incorporate line feedforward, the triangle waveform frequency will remain constant.

SD: A voltage on SD within 2.5V (typical) of VCC will cause the UC3638 to enter a UVLO condition which disables all of the driver outputs. With an external voltage divider across VCC and VEE, and a capacitor between SD and VCC, a delayed turn-on characteristic can be generated. Since the 2.5V threshold is temperature stabilized it can also be used as a higher UVLO threshold for applications which require a starting voltage higher than the internal 9V UVLO threshold.

VEE: All voltages are measured with respect to this pin. All bypass capacitors and timing components except those listed under the PVE section should be connected to this pin. Component leads should be as short and direct as possible. VEE is generally connected to the most negative voltage supply in the system. In single supply applications, VEE is tied to the system ground.

VCC: Positive supply rail for the IC. Bypass this pin to VEE and PVE with 0.1 to 1µF low ESL, ESR ceramic capacitor(s). The maximum voltage for VCC is 40V referenced to VEE. The turn on voltage level on VCC is 9V with 1V of hysteresis.

APPLICATION INFORMATION

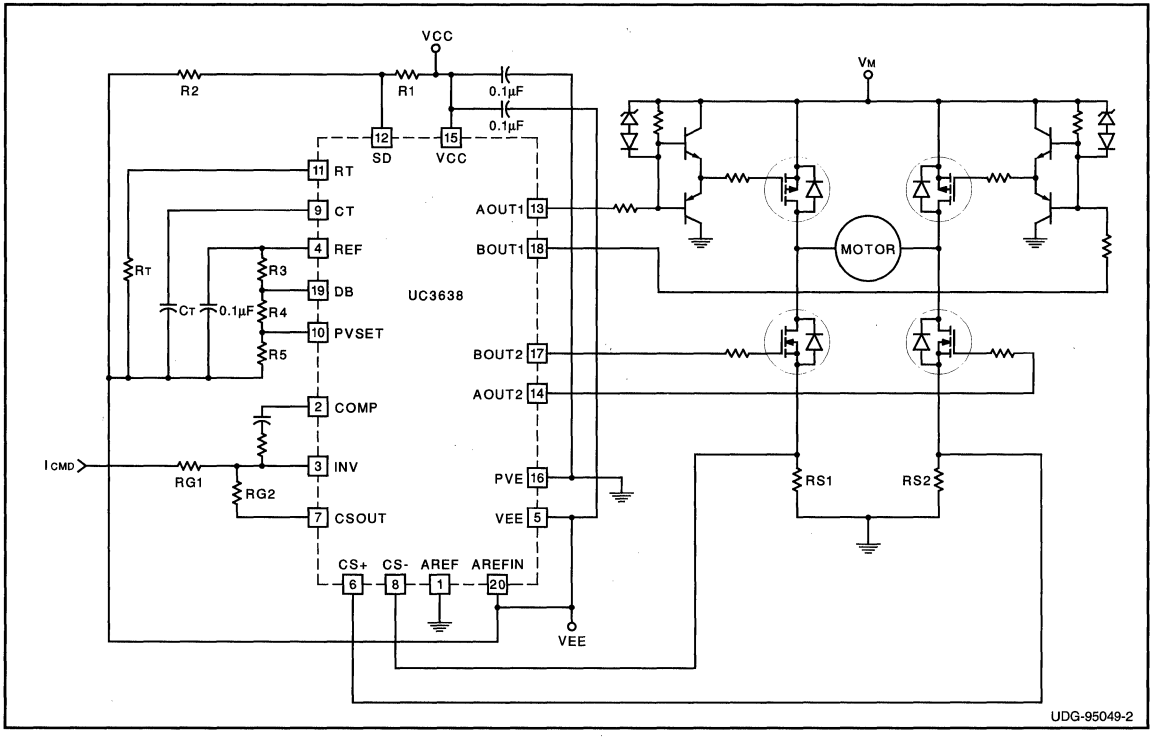


Figure 1. Average Motor Current Control Loop

The UC3638 is designed to provide pulse width modulation control of DC brush motors in applications requiring precision torque, velocity, or position control. Due to its high frequency capability, other high power applications such as switch mode audio amplifiers can also be addressed. Through a combination of circuit sophistication and integration, the designer can maintain a high level of flexibility, while reducing cost compared to solutions using other PWM ICs.

Figure 1 shows a typical application circuit for the UC3638. By taking advantage of the UC3638's many integrated functions, a low cost and compact average current mode motor controller can be designed. Depending on the level of complexity, as many as 15 discrete components and an additional high bandwidth amplifier can be saved compared to a similar circuit using the UC3637 PWM controller.

Oscillator Section and Modulation Scheme

Figure 2 depicts the UC3638 oscillator and PWM waveforms for the condition where the output of the voltage amplifier (COMP) is at the null point (same voltage as AREF). For applications using split voltage supply rails, AREF will normally be tied to system ground. This results in a voltage null point of zero volts. For this condition, AREFIN should be tied to the negative voltage supply rail (VEE), which disables the internal voltage buffer, allowing AREF to be tied to ground. For a single supply system, AREFIN should be left open circuit, and AREF should be decoupled to VEE (system ground) with at least 0.1µF. The resulting voltage null point for

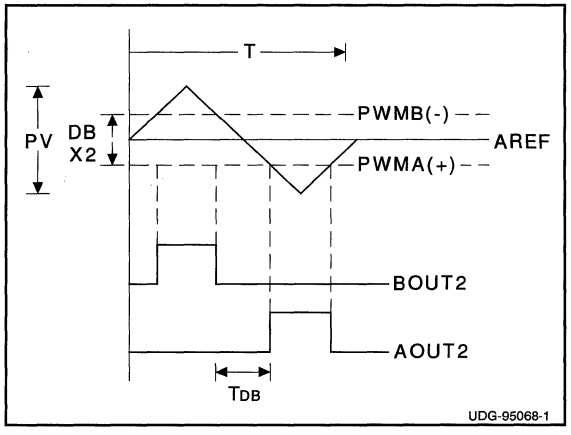


Figure 2. Oscillator and PWM Waveforms

APPLICATION INFORMATION (cont.)

this case will be half way between ground and VCC, and will automatically track changes in VCC. For cases where a different null point is desired, AREF can be tied to any voltage between VEE + 2V and VCC – 2V. Of course the user must also allow sufficient headroom for the triangle waveform.

Once the system null point has been chosen, the triangle wave amplitude and PWM deadband must be programmed. The amplitude of the triangle wave is determined by trading off noise immunity and gain requirements. In general, the larger the triangle wave amplitude, the greater the immunity to premature termination of PWM pulses due to switching noise. However, high amplitude triangle waves require a greater voltage swing at the output of the voltage amplifier which ultimately reduces forward loop gain.

Programming the PWM deadband allows the user to trade off gain linearity requirements with power amplifier efficiency. If the modulator is configured as in Figure 1, motor current is alternately pulsed by diagonally opposite drive FETs when the servo loop is at null. By adjusting the deadband, the user can program the offset voltage at the input of the PWM comparators. This offset results in deadtime, or time when neither PWM signal is active.

A minimum amount of deadtime is always recommended to provide cross conduction protection at the power amplifier. Setting the deadtime to this minimum level will provide the maximum motor stiffness or holding torque, at the expense of power losses in the output stage. These losses result from the fact that the power amplifier is always sourcing motor current, even at null. As deadtime is increased, amplifier losses at null become less, at the expense of nonlinearity in the gain function. Eventually, if the deadband voltage is increased to equal the amplitude of the triangle wave, error voltages at the null point will result in no PWM pulsing, or a dead zone. After the triangle waveform amplitude and deadband are selected, the operating frequency is easily set by proper selection of CT and RT.

Referring to Figure 1, if the voltage supply rails are ±15V, and the desired triangle wave oscillator amplitude is 6V p-p, PVSET is set by:

$$V_{PK} - V_{VLY} = 5 \bullet V_{PVSET}$$

$$V_{PVSET} = \frac{6}{5} = 1.2V$$

If 1V of deadband is chosen:

$$5 - V_{DB} = 1V$$

$$V_{DB} = 4V$$

In order to select the programming resistors, a source current for the reference is first selected. For a 1mA source current:

$$R3 + R4 + R5 = \frac{5}{ISOURCE} = \frac{5}{1mA} = 5k$$

$$R3 = \frac{5 - VDB}{ISOURCE} = \frac{1V}{1mA} = 1k$$

$$R4 = \frac{VDB - VPVSET}{ISOURCE} = \frac{4V - 1.2V}{1mA} = 2.8k$$

$$R5 = 5k - 1k - 2.8k = 1.2k$$

All of the voltages described by these equations are referenced to the negative supply rail. In other words, for a split supply system, VREF is actually a negative voltage referenced to ground.

The oscillator frequency is programmed by proper selection of RT and CT. If 220pF is chosen for CT, and an operating frequency of 30kHz is desired, RT is chosen by:

$$F = \frac{1}{5 \bullet RT \bullet CT}$$

$$30kHz = \frac{1}{5 \bullet 220pF \bullet RT}$$

$$RT = 30k$$

With RT = 30k, the charge current out of the RT pin is limited to

$$\frac{1.2V}{30k} = 40\mu A,$$

which is well within the specified maximum of 1mA.

To calculate the actual deadtime or minimum time between PWM pulses (T_{DB}), the ratio of the deadband voltage to the triangle wave amplitude is multiplied by half the oscillator period:

$$T_{DB} = \frac{DB}{VPK - VVLY} \bullet \frac{1}{f}$$

$$= \frac{5 - VDB}{5 \bullet VPVSET} \bullet (5 \bullet RT \bullet CT)$$

$$= \frac{(5 - VDB) \bullet RT \bullet CT}{VPVSET}$$

For this example the deadtime is:

$$T_{DB} = \frac{1 \bullet 30k \bullet 220pF}{1.2} = 5.5\mu sec$$

If voltage feedforward is desired, PVSET should be derived off of the supply rails instead of VREF. This way changes in the supply voltage will linearly regulate the modulator gain, which decreases control loop susceptibility to line voltage variations. Since the voltage on the RT pin is a buffered version of PVSET, charge current tracks oscillator amplitude, and therefore the frequency

APPLICATION INFORMATION (cont.)

remains constant, preventing low frequency oscillator modulation in the presence of line voltage changes.

Output Drivers

The output driver section provides separate output drivers for high and low side drive of both PWM signals. For many applications, the 500mA peak output current capability of the low side drivers (AOUT2 and BOUT2) is sufficient to directly connect to the appropriate low side MOSFETs of the H-bridge. A current limiting gate resistor may be used to control switching time if high levels of dv/dt or di/dt are expected at the drains of the MOSFETs. If more current drive capability is required, the PWM drive signals can be buffered with bipolar transistors.

The open collector high side drivers (AOUT1 and BOUT1) are designed to control high side P-channel MOSFETs. Depending on voltage and speed requirements, the driver stage can be simplified from the one shown on Figure 1. If high side N-channel MOSFETs are desired, a boot strap or charge pump based drive circuit can be used as long as 100% duty cycle operation is not required.

Average Current Control

The UC3638 incorporates all of the necessary features for precise average current loop control of a DC motor. In the circuit shown in Figure 1, motor current is sensed differentially across two current sense resistors.By using two current sense resistors both the current sourced from the motor voltage supply (Vm) and the flyback current are sensed in the correct polarity to provide true torque control. If only one current sensed resistor is used, the flyback current will circulate through the body diodes of the lower MOSFETs and bypass the current sense resistor. The result will be a duty cycle dependent error term in the loop torque control function. In order to prevent high frequency spikes from contributing excessive error to the current control loop, the switching speed of the MOSFETs must be controlled so that significant transient current spikes do not couple across the drain to source capacitance of the MOSFETs.

The X5 current amplifier multiplies the current signal by a factor of 5 and feeds the average current signal into the error amplifier. A window comparator detects if the peak current signal at the output of the current amplifier has a magnitude greater than 2.5V in either polarity and provides pulse-by-pulse peak current limiting. The loop should be designed so that peak motor current never reaches this level during normal operation.

With integral compensation, the average current loop will have very high DC gain, resulting in effectively no average DC motor current error. For stability purposes, the high frequency gain of the voltage error amplifier must be designed such that magnitude of the slope of the error amplifier output (COMP) must be less than or equal to the magnitude of the slope of the triangle waveform.

If RS1 = RS2 = RS, the DC gain of the current control loop can be calculated as:

$$\frac{IMOTOR}{ICMD} = \frac{RG2}{5 \bullet RG1 \bullet RS}$$

If the UC3638 is set up in a simple velocity or position control loop, the feedback voltage (speed or position) is summed directly into the voltage error amplifier, and the current sense amplifier is only used for peak current limit control. The motor can also be replaced by another high power device, such as an audio speaker, and the same type of amplifier can be used. In the case of audio however, a higher switching frequency will probably be desired to prevent switching noise from infiltrating the audio frequency range.

UVLO and Shutdown

The UC3638 contains undervoltage lockout (UVLO) circuitry to prevent unwanted bridge turn-on before sufficient supply voltage is available. The open collector drivers (AOUT1 and BOUT1) are held off (no sink current) and the totem pole drivers (AOUT 2 and BOUT2) are pulled low until the voltage between VCC and VEE reaches 9V typical. The UVLO circuitry becomes active at approximately 1V, and before this level the totem pole drivers are held low with passive pull down resistors.

The shutdown pin holds the output drivers in their inactive state unless it is pulled 2.5V below VCC. An open collector gate or transistor can be used as an external enable signal, or a turn-on voltage higher than UVLO can be programmed with a resistive divider. In the case of Figure 1, the turn on voltage V_{START} can be calculated as:

$$V_{START} = \frac{2.5 \bullet (R1 + R2)}{R1}$$

If a delayed start is desired, a capacitor can be placed in parallel with R1 to slow down the change in voltage at the shutdown pin, and thus provide a user programmable startup time.

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application INFO available

UC1717
UC2717
UC3717

Stepper Motor Drive Circuit

FEATURES

- Half-step and Full-step Capability
- Bipolar Constant Current Motor Drive
- Built-in Fast Recovery Schottky Commutating Diodes
- Wide Range of Current Control 5-1000mA
- Wide Voltage Range 10-45V
- Designed for Unregulated Motor Supply Voltage
- Current Levels can be Selected in Steps or Varied Continuously
- Thermal Overload Protection

DESCRIPTION

The UC3717 has been designed to control and drive the current in one winding of a bipolar stepper motor. The circuit consists of an LS-TTL-compatible logic input, a current sensor, a monostable and an output stage with built-in protection diodes. Two UC3717s and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC1717 is characterized for operation over the full military temperature range of -55°C to +125°C, the UC2717 is characterized for -25°C to +85°C, and the UC3717 is characterized for 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{CC} 7V
- Output Supply, V_M 45V

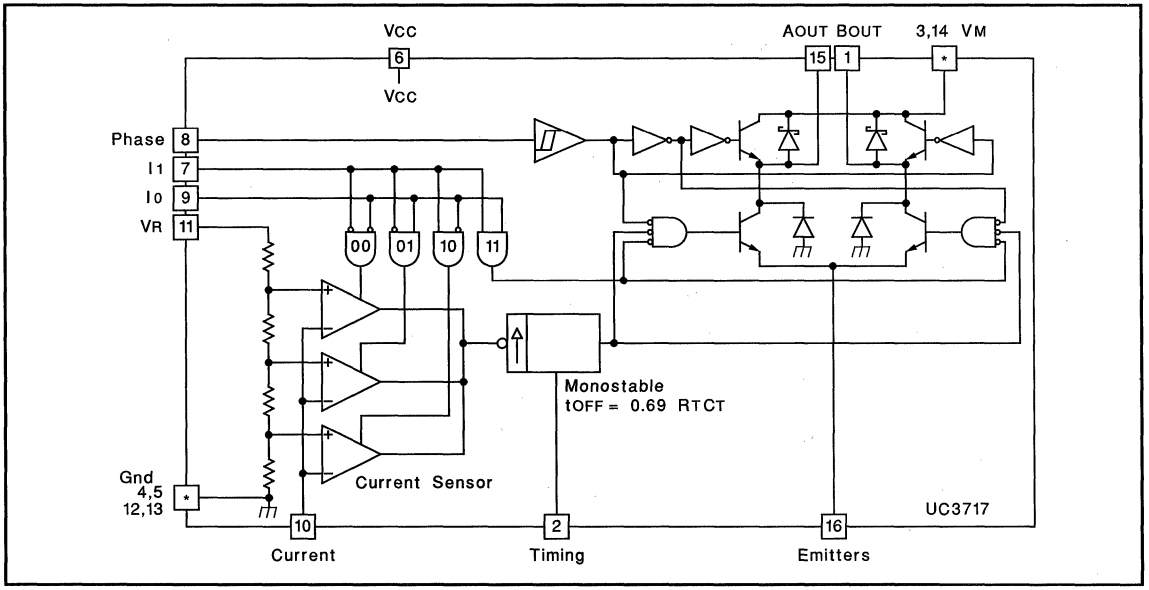
Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) Vcc
- Reference Input (Pin 11) 15V

Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1A
Junction Temperature, T_J ..... +150°C
Storage Temperature Range, T_S ..... -55°C to +150°C

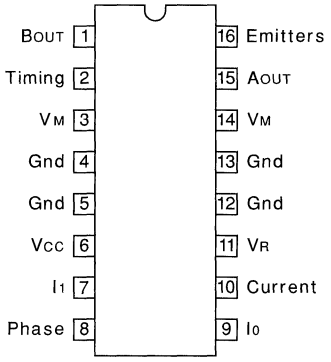
Note 1: All voltages are with respect to ground, Pins 4,5, 12, 13. Pin numbers refer to DIL-16 package. Currents are positive into, negative out of the specified terminal.
Note 2: Consult Packaging Section of Databook for information on thermal limitations and considerations of package.

BLOCK DIAGRAM

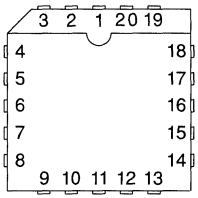


CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
VM	4
Gnd	5
N/C	6
Gnd	7
VCC	8
I1	9
Phase	10
N/C	11
IO	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNITS
Supply Voltage, VCC	4.75	5	5.25	V
Supply Voltage, VM	10		40	V
Output Current. IM	20		800	mA
Rise Time Logic Inputs, tR			2	µs
Fall Time Logic Inputs, tF			2	µs
Ambient Temperature, TA				
UC1717	-55		125	°C
UC2717	-25		85	°C
UC3717	0		70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply for VCC = 5V, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, ICC				25	mA
High-Level Input Voltage, Pins 7, 8, 9		2.0			V
Low-Level Input Voltage, Pins 7, 8, 9				0.8	V
High-Level Input Current, Pins 7, 8, 9	VI = 2.4V			20	µA
Low Level Input Current, Pins 7, 8, 9	VI = 0.4V	-0.4			mA
Comparator Threshold Voltage	IO = 0, I1 = 0, VR = 5.0V	390	420	440	mV
	IO = 1, I1 = 0, VR = 5.0V	230	250	270	mV
	IO = 0, I1 = 1, VR = 5.0V	65	80	90	mV
Comparator Input Current		-20		20	µA
Output Leakage Current	IO = 1, I1 = 1, TA = +25°C			100	µA
Total Saturation Voltage Drop	IM = 500mA			4.0	V
Total Power Dissipation	IM = 500mA, fs = 30kHz		1.4	2.1	W
	IM = 800mA, fs = 30kHz		2.9	3.1	W
Cut Off Time, tOFF	VM = 10V, tON≥ 5µs (See Figure 5 and 6)	25	30	35	µs
Turn Off Delay, tD	TA = +25°C; dVc/dt ≥ 50mV/µs (See Figure 5 and 6)		1.6	2.0	µs
Thermal Shutdown Junction Temperature		+160		+180	°C

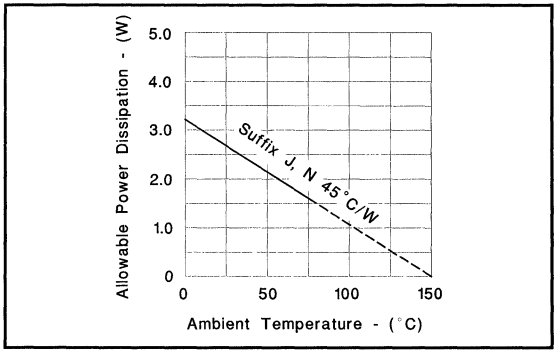


Figure 1

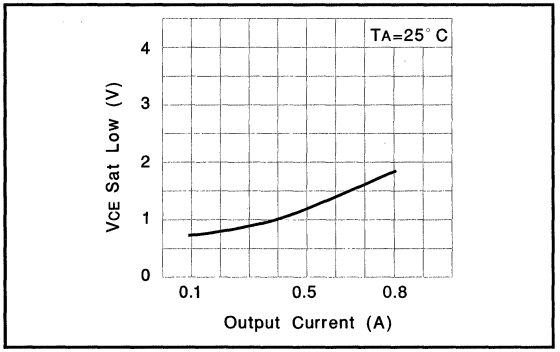


Figure 3: Typical Sink Saturation Voltage vs Output Current

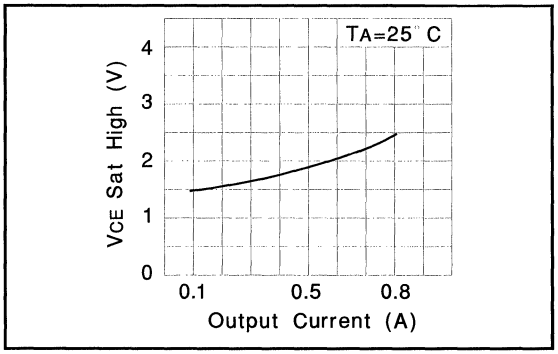


Figure 2: Typical Source Saturation Voltage vs Output Current

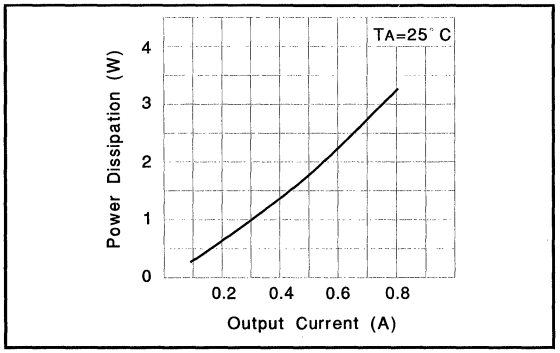


Figure 4: Typical Power Losses vs Output Current

FUNCTIONAL DESCRIPTION

The UC3717 drive circuit shown in the block diagram includes the following functions:

(1) Phase Logic and H-Bridge Output Stage
(2) Voltage Divider with three Comparators for current control
(3) Two Logic inputs for Digital current level select
(4) Monostable for off time generation

Input Logic: If any of the logic inputs are left open, the circuit will treat it as a high level input.

Phase Input: The phase input terminal, pin 18, controls the direction of the current through the motor winding. The Schmidt-Trigger input coupled with a fixed time delay assures noise immunity and eliminates cross conduction in the output stage during phase changes. A low level on the phase input will turn Q2 on and enable Q3 while a high level will turn Q1 on and enable Q4. (See Figure 7).

Output Stage: The output stage consists of four Darlington transistors and associated diodes connected in an H-Bridge configuration. The diodes are needed to provide a current path when the transistors are being switched. For fast recovery, Schottky diodes are used across the source transistors. The Schottky diodes allow the current

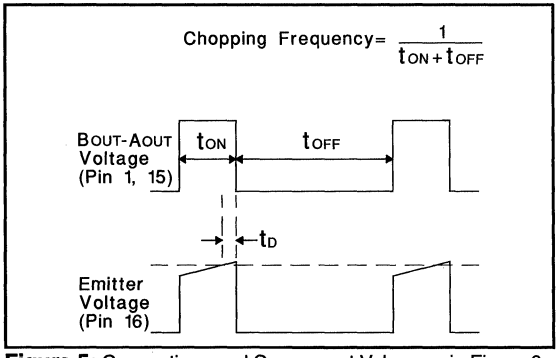


Figure 5: Connections and Component Values as in Figure 6.

to circulate through the winding while the sink transistors are being switched off. The diodes across the sink transistors in conjunction with the Schottkys provide the path for the decaying current during phase reversal. (See Figure 7).

PHASE INPUT	Q1, Q4	Q2, Q3
Low	Off	On
High	On	Off

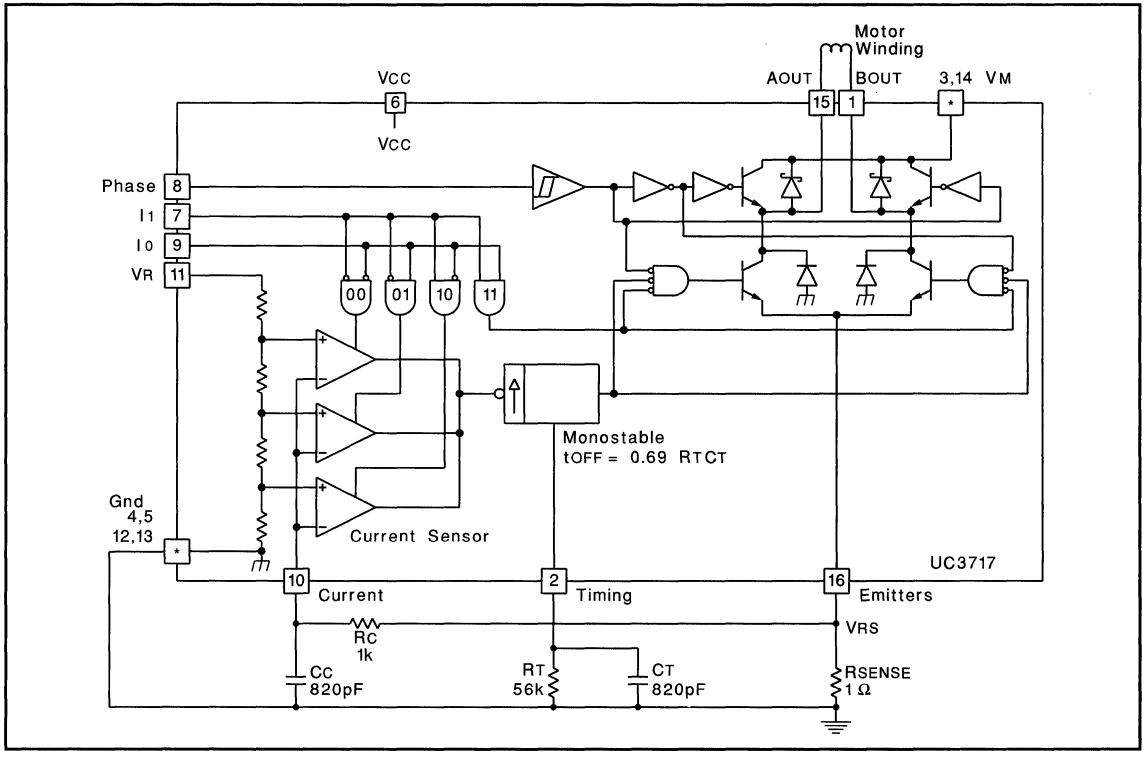


Figure 6

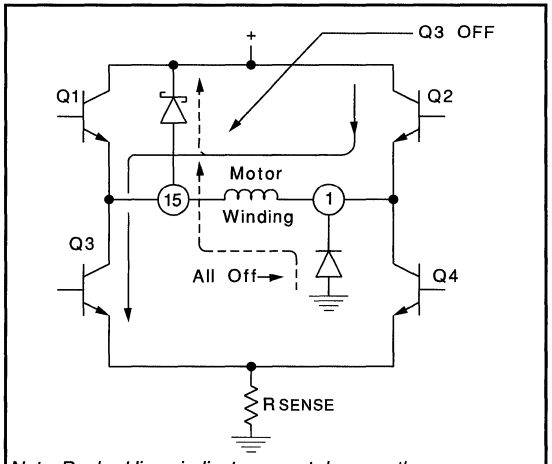
I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

Current Control: The voltage divider, comparators and monostable provide a means for current sensing and control. The two bit input (I_0, I_1) logic selects the desired comparator. The monostable controls the off time and therefore the magnitude of the current decrease. The time duration is determined by R_T and C_T connected to the timing terminal (pin 2). The reference terminal (pin 11) provides a means of continuously varying the current for situations requiring half-stepping and micro-stepping. The relationship between the logic input signals at pin 7 and 9 in reference to the current level is shown in Table 1. The values of the different current levels are determined by the reference voltage together with the value of the external sense resistor R_S (pin 16).

Single-Pulse Generator: The pulse generator is a monostable triggered on the positive going edge of the comparator. Its output is high during the pulse time and this pulse switches off the power feed to the motor winding causing the current to decay. The time is determined by the external timing components R_T and C_T as:

$$T_{OFF} = 0.69\ R_T C_T$$

If a new trigger signal should occur during T_{OFF}, it is ignored.



Note: Dashed lines indicate current decay paths.

Figure 7: Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

Overload Protection: The circuit is equipped with a thermal shutdown function, which will limit the junction temperature by reducing the output current. It should be noted however, that a short circuit of the output is not permitted.

Operation: When the voltage is applied across the motor winding the current rises linearly and appears across the external sense resistor as an analog voltage. This voltage is fed through a low pass filter Rc, Cc to the voltage comparator (pin 10). At the moment the voltage rises beyond the comparator threshold voltage the monostable is triggered and its output turns off the sink transistors. The current then circulates through the source transistor and the appropriate Schottky diode. After the one shot has timed out, the sink transistsor is turned on again and the procedure repeated until a current reverse command is given. By reversing the logic level of the phase input (pin 8), both active transistors are being turned off and the opposite pair turned on. When this happens the current must first decay to zero before it can reverse. The current path then provided is through the two diodes and the power-supply. Refer to Figure 7. It should be noted at this time that the slope of the current decay is steeper, and this is due to the higher voltage build up across the winding. For better speed performance of the stepping motor at half step mode, the phase logic level should be changed at the same time the current inhibit is applied. A typical current wave form is shown in Figure 8.

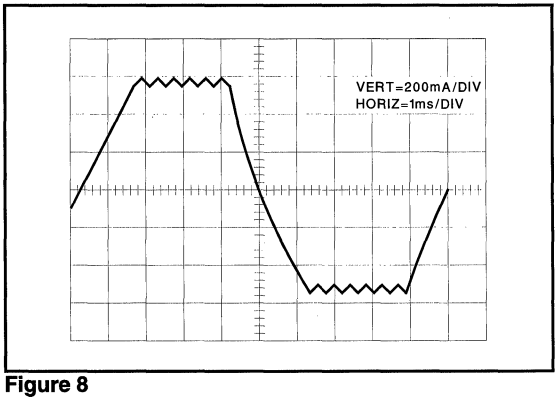


Figure 8

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 9. The input can be controlled by a microprocessor, TTL, LS or CMOS logic.

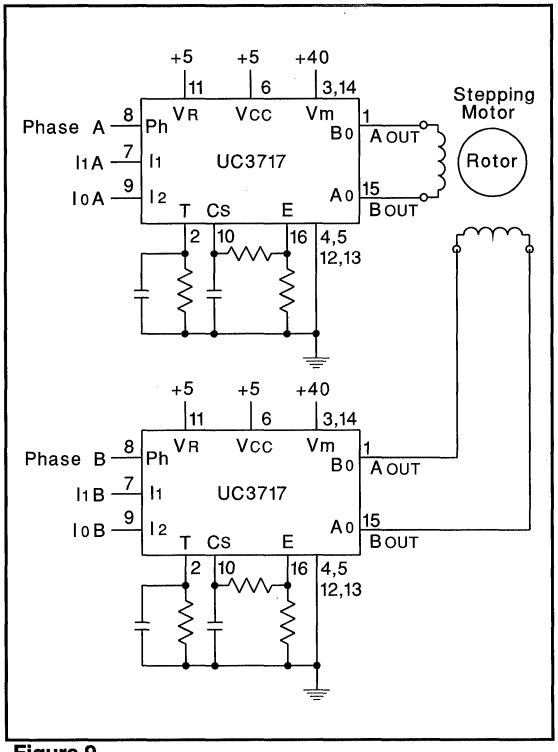


Figure 9

The timing diagram in Figure 10 shows the required signal input for a two phase, full step, stepping sequence. Figure 11 shows a one phase, full step, stepping sequence, commonly referred to as wave drive. Figure 12 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 13 provides the signal shown in Figure 10, and in conjunction with the circuit shown in Figure 9, will implement a pulse-to-step two phase, full step, bidirectional motor drive.

The schematic of Figure 14 shows a pulse to half step circuit generating the signal shown in Figure 12. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at higher step rates.

Using the UC3717 to drive the L298 provides a uniquely packaged state-of-the-art high power stepper motor control and drive. See Figure 15.

FUNCTIONAL DESCRIPTION (cont.)

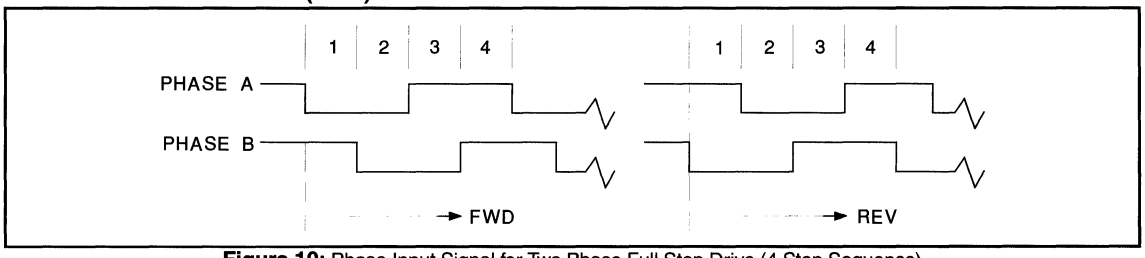


Figure 10: Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

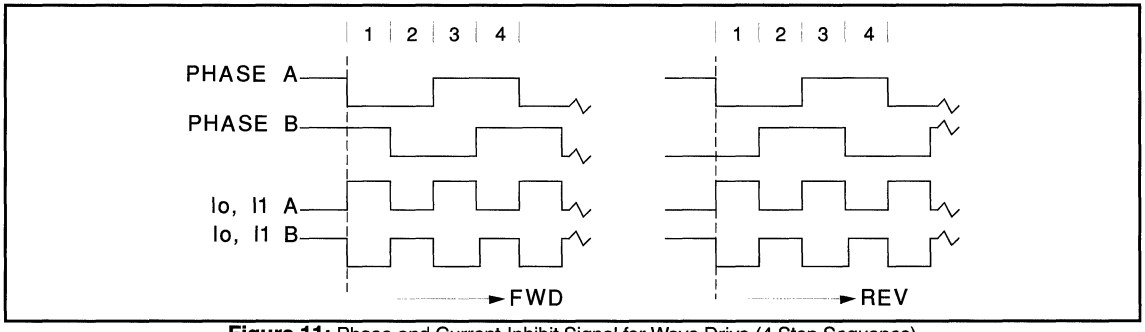


Figure 11: Phase and Current-Inhibit Signal for Wave Drive (4 Step Sequence)

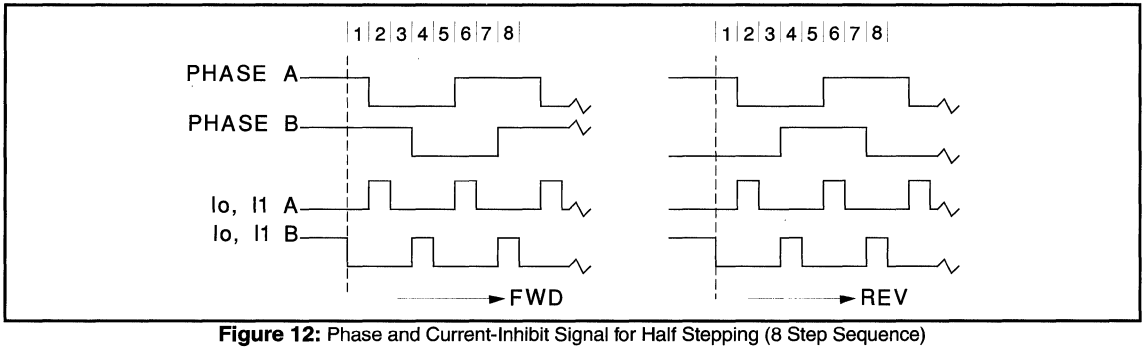


Figure 12: Phase and Current-Inhibit Signal for Half Stepping (8 Step Sequence)

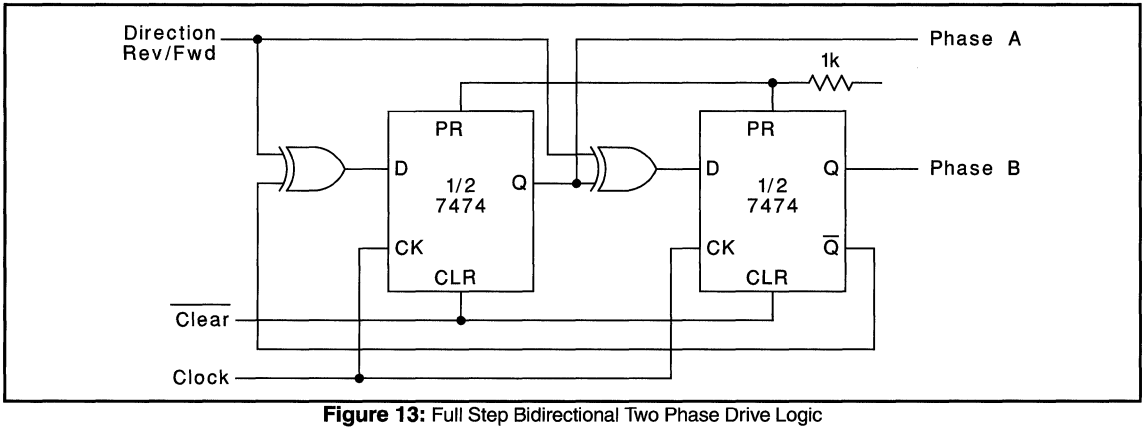


Figure 13: Full Step Bidirectional Two Phase Drive Logic

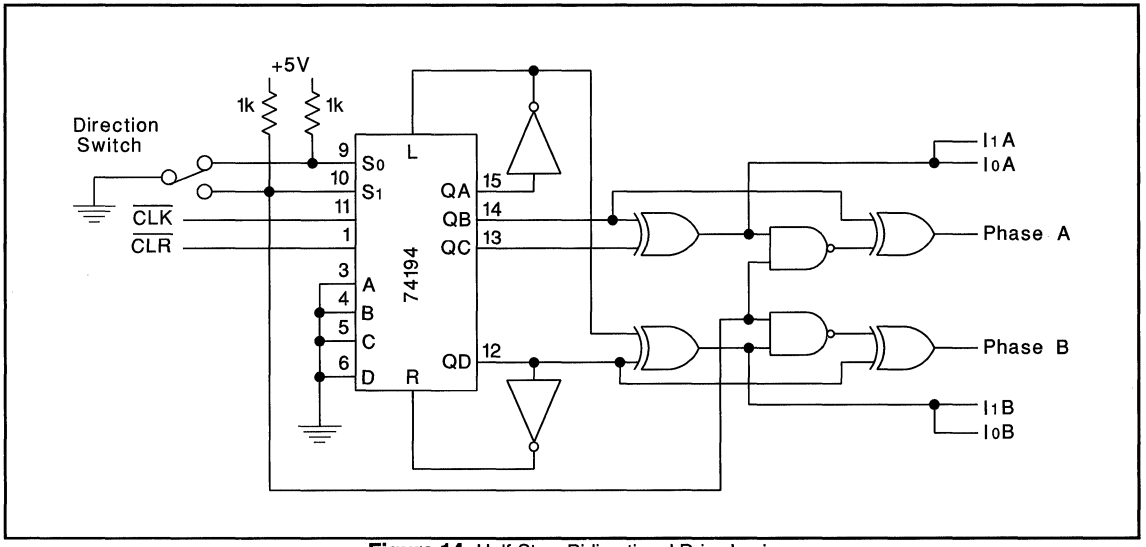


Figure 14: Half-Step, Bidirectional Drive Logic

CONSIDERATION

Half-Stepping: In the half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90 degrees. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the V_R input can be used to boost the current of the single energized winding.

Ramping: Every drive system has inertia and must be considered in the drive scheme. The rotor and load inertia plays a big role at higher speeds. Unlike the DC motor the stepping motor is a synchronous motor and does not change its speed due to load variations. Examining typical stepping motors, torque vs. speed curves indicates a sharp torque drop off for the start-stop without error curve, even with a constant current drive. The reason for this is that the torque requirements increase by the square of the speed change, and the power need increases by the cube of the speed change. As it can be seen, for good motor performance controlled acceleration and deceleration should be considered.

Iron Core Losses: Some motors, especially the Tin-Can type, exhibit high iron losses mostly due to eddy currents which rise in an exponential manner as the frequency or step rate is increased. The power losses can not be calculated by I^2R where I is the chopping current level and R the DC resistance of the coil. Actual measurements indicate the effective resistance may be many times larger. Therefore, for 100% duty cycle the current must be limited to a value which will not overheat the motor. This may not be necessary for lower duty cycle operation.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1µF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Ordering Information

UNITRODE TYPE NUMBER
UC3717N - 16 Pin Dual-in-line (DIL) "Bat Wing" Package
UC1717J - 16 Pin Dual-in-line Ceramic Package
UC1717SP - 16 Pin Dual-in-line Hermetic Power Package

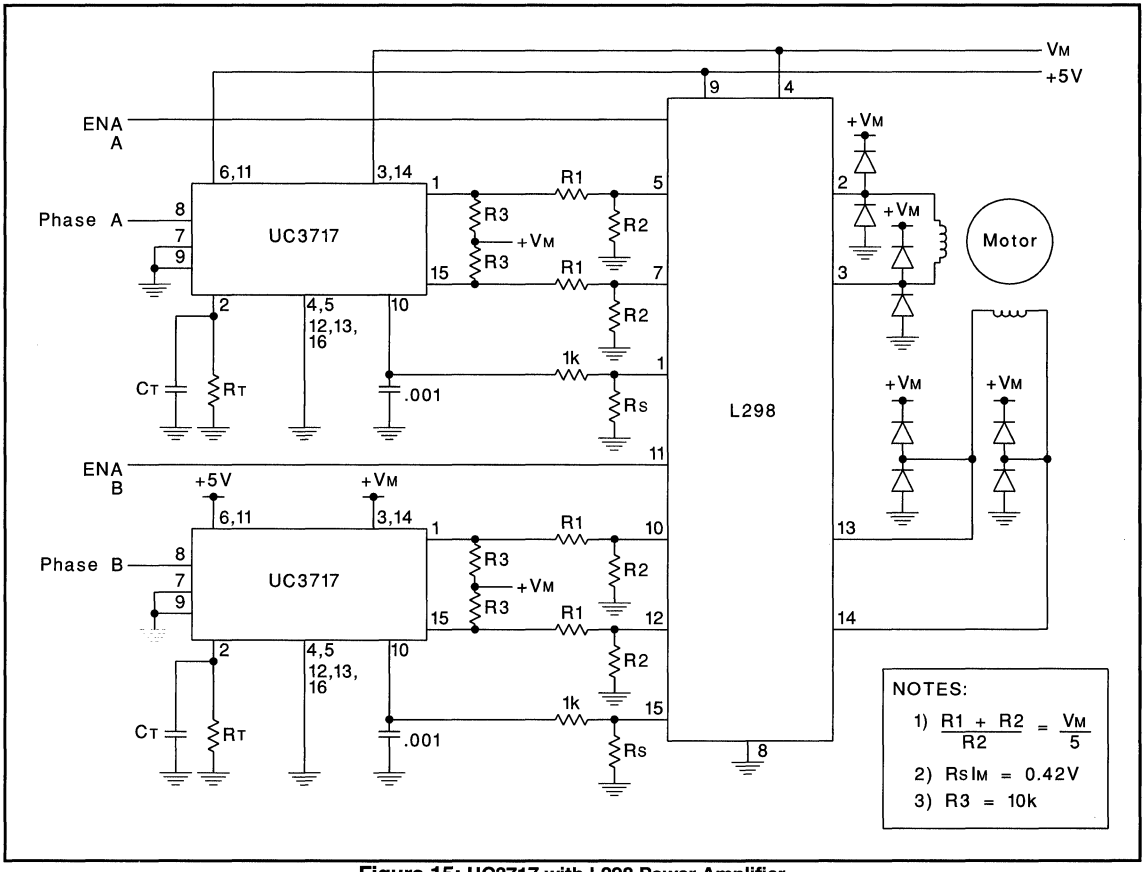


Figure 15: UC3717 with L298 Power Amplifier

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

application INFO available

Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability
- Bipolar Output Current up to 1A
- Wide Range of Motor Supply Voltage 10-46V
- Low Saturation Voltage with Integrated Bootstrap
- Built-In Fast Recovery Commutating Diodes
- Current Levels Selected in Steps or Varied Continuously
- Thermal Protection with Soft Intervention

DESCRIPTION

The UC3717A is an improved version of the UC3717, used to switch drive the current in one winding of a bipolar stepper motor. The UC3717A has been modified to supply higher winding current, more reliable thermal protection, and improved efficiency by providing integrated bootstrap circuitry to lower recirculation saturation voltages. The diagram shown below presents the building blocks of the UC3717A. Included are an LS-TTL compatible logic input, a current sensor, a monostable, a thermal shutdown network, and an H-bridge output stage. The output stage features built-in fast recovery commutating diodes and integrated bootstrap pull up. Two UC3717As and a few external components form a complete control and drive unit for LS-TTL or micro-processor controlled stepper motor systems.

The UC3717A is characterized for operation over the temperature range of 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage
- Logic Supply, V_{CC} 7V
- Output Supply, V_M 50V

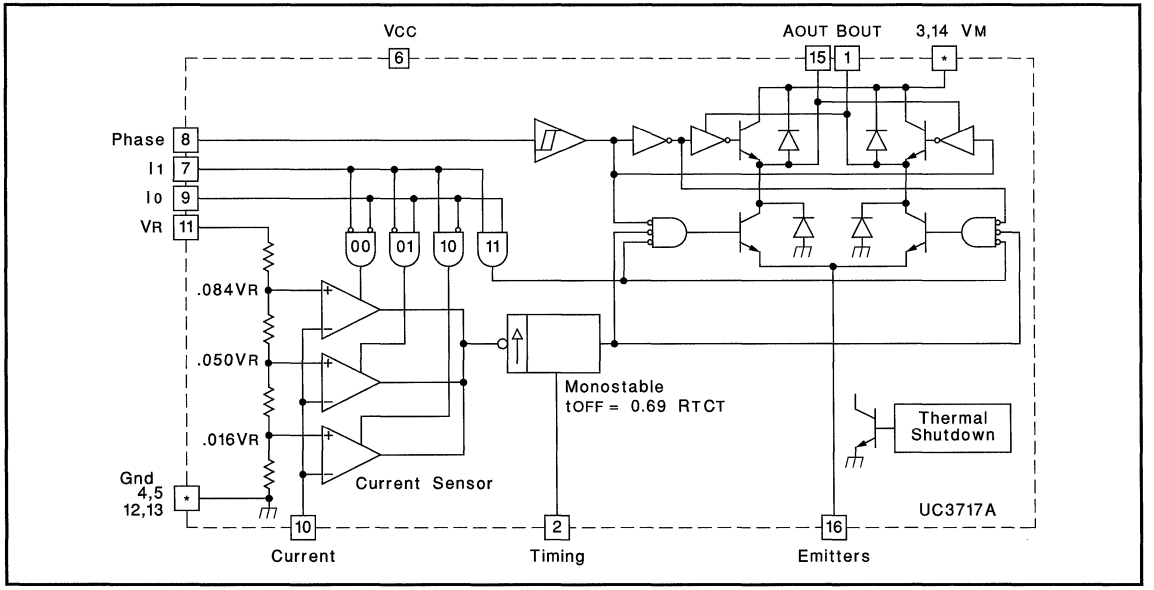
Input Voltage
- Logic Inputs (Pins 7, 8, 9) 6V
- Analog Input (Pin 10) ..... V_{CC}
- Reference Input (Pin 11) 15V

Input Current
- Logic Inputs (Pins 7, 8, 9) ..... -10mA
- Analog Inputs (Pins 10, 11) ..... -10mA

Output Current (Pins 1, 15) ..... ±1.2A
Junction Temperature, T_J ..... +150°C
Storage Temperature Range, T_S ..... -55°C to +150°C

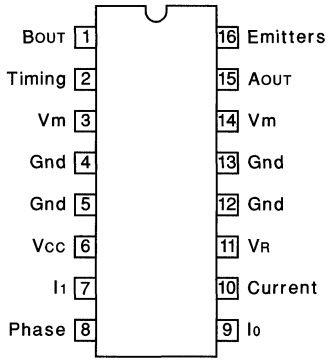
Note 1: All voltages are with respect to ground, Pins 4, 5, 12, 13. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL-16 package.
Consult Packaging Section of Databook for thermal limitations and considerations of package.

BLOCK DIAGRAM

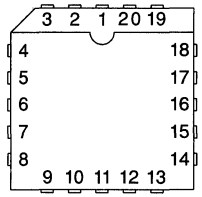


CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)
J or N Package



PLCC-20 (TOP VIEW)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
BOUT	2
Timing	3
Vm	4
Gnd	5
N/C	6
Gnd	7
VCC	8
I1	9
Phase	10
N/C	11
Io	12
Current	13
VR	14
Gnd	15
N/C	16
Gnd	17
Vm	18
AOUT	19
Emitters	20

ELECTRICAL CHARACTERISTICS

(Refer to the test circuit, Figure 6. V_m = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, V_m (Pins 3, 14)		10		46	V
Logic Supply Voltage, V_{CC} (Pin 6)		4.75		5.25	V
Logic Supply Current, I_{CC} (Pin 6)	I_O = I_1 = 0		7	15	mA
Thermal Shutdown Temperature		+160		+180	°C
Logic Inputs					
Input Low Voltage, (Pins 7, 8, 9)				0.8	V
Input High Voltage, (Pins 7, 8, 9)		2		V_{CC}	V
Low Voltage Input Current, (Pins 7, 8, 9)	V_I = 0.4V, Pin 8			-100	µA
	V_I = 0.4V, Pins 7 and 9			-400	mA
High Voltage Input Current, (Pins 7, 8, 9)	V_I = 2.4V			10	µA
Comparators					
Comparator Low, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = H	66	80	90	mV
Comparator Medium, Threshold Voltage (Pin 10)	V_R = 5V; I_O = H; I_1 = L	236	250	266	mV
Comparator High, Threshold Voltage (Pin 10)	V_R = 5V; I_O = L; I_1 = L	396	420	436	mV
Comparator Input, Current (Pin 10)				±20	µA
Cutoff Time, t_{OFF}	R_T = 56kΩ, C_T = 820pF	25		35	µs
Turn Off Delay, t_D	(See Figure 5)			2	µs
Source Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -0.5A, Conduction Period		1.7	2.1	V
(See Figure 5)	I_m = -0.5A, Recirculation Period		1.1	1.35	V
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = -1A, Conduction Period		2.1	2.8	V
(See Figure 5)	I_m = -1A, Recirculation Period		1.7	2.5	V
Leakage Current	V_m = 40V			300	mA
Diode Forward Voltage, V_F	I_m = -0.5A		1	1.25	V
	I_m = -1A		1.3	1.7	V

ELECTRICAL CHARACTERISTICS (cont.) (Refer to the test circuit, Figure 6. V_M = 36V, V_{CC} = 5V, V_R = 5V, T_A = 0°C to 70°C, unless otherwise stated, T_A = T_J.)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sink Diode-Transistor Pair					
Saturation Voltage, V_{SAT} (Pins 1, 15)	I_m = 0.5A	0.8	1.1	1.35	V
	I_m = 1A		1.6	2.3	V
Leakage Current	V_m = 40V			300	µA
Diode Forward Voltage, V_F	I_m = 0.5A		1.1	1.5	V
	I_m = 1A		1.4	2	V

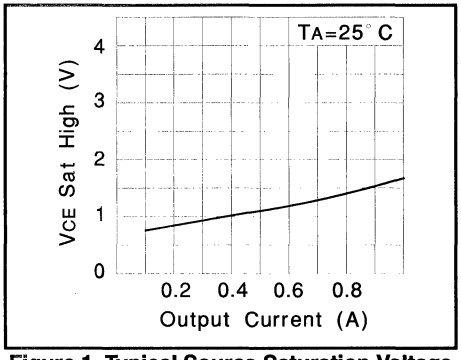


Figure 1. Typical Source Saturation Voltage vs Output Current (Recirculation Period)

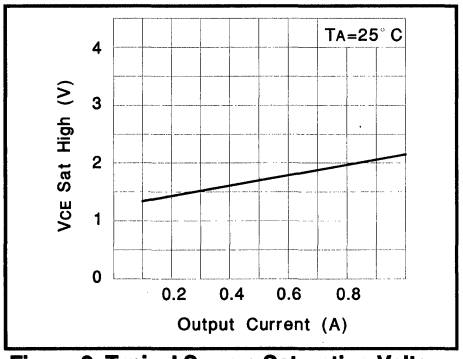


Figure 2. Typical Source Saturation Voltage vs Output Current (Conduction Period)

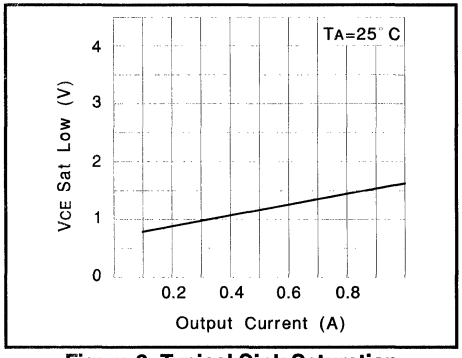


Figure 3. Typical Sink Saturation Voltage vs Output Current

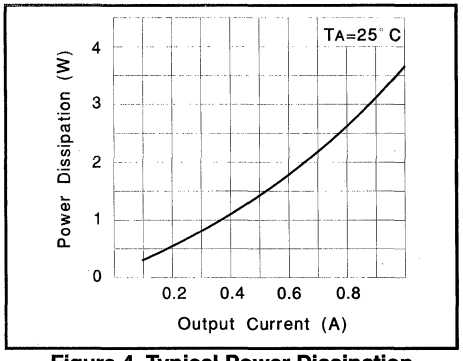


Figure 4. Typical Power Dissipation vs Output Current

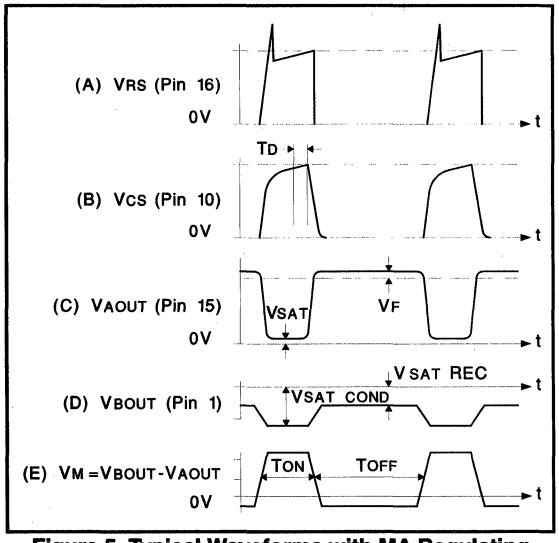


Figure 5. Typical Waveforms with MA Regulating (phase = 0)

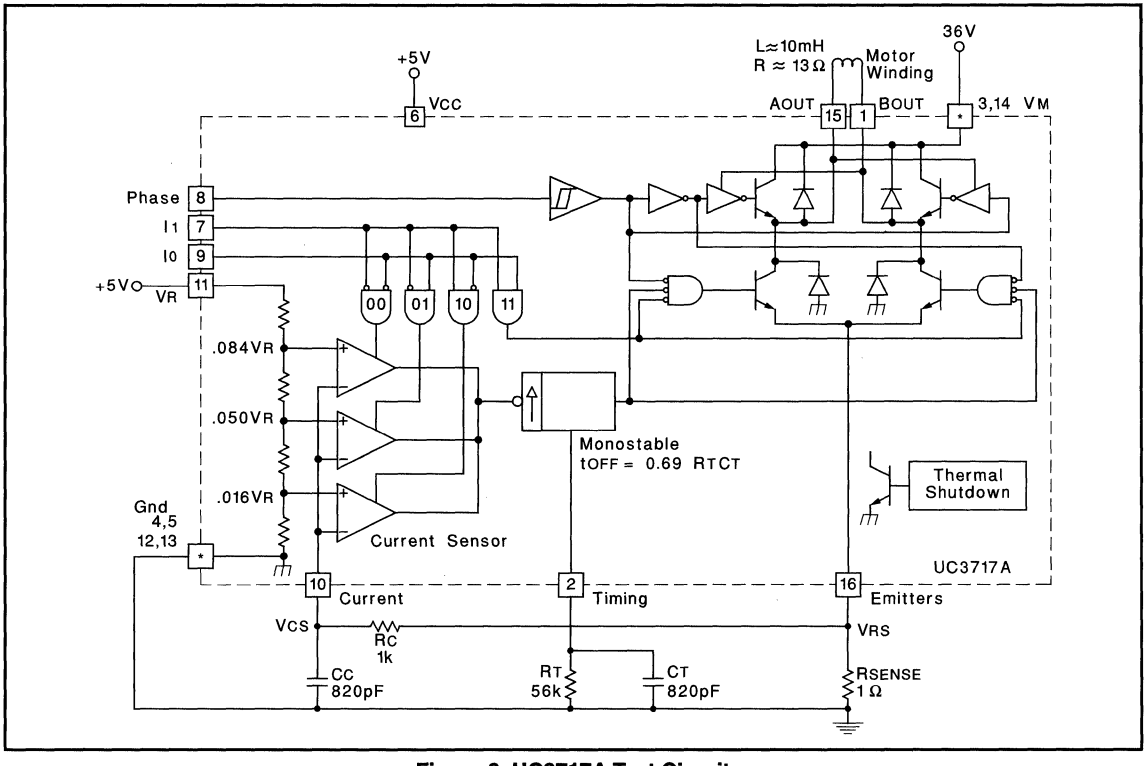


Figure 6. UC3717A Test Circuit

FUNCTIONAL DESCRIPTION

The UC3717A's drive circuit shown in the block diagram includes the following components.

(1) H-bridge output stage
(2) Phase polarity logic
(3) Voltage divider coupled with current sensing comparators
(4) Two-bit D/A current level select
(5) Monostable generating fixed off-time
(6) Thermal protection

OUTPUT STAGE

The UC3717A's output stage consists of four Darlington power transistors and associated recirculating power diodes in a full H-bridge configuration as shown in Figure 7. Also presented, is the new added feature of integrated bootstrap pull up, which improves device performance during switched mode operation. While in switched mode, with a low level phase polarity input, Q2 is on and Q3 is being switched. At the moment Q3 turns off, winding current begins to decay through the commutating diode pulling the collector of Q3 above the supply voltage. Meanwhile, Q6 turns on pulling the base of Q2 higher than its previous value. The net effect lowers the saturation voltage of source transistor Q2 during recirculation, thus improving efficiency by reducing power dissipation.

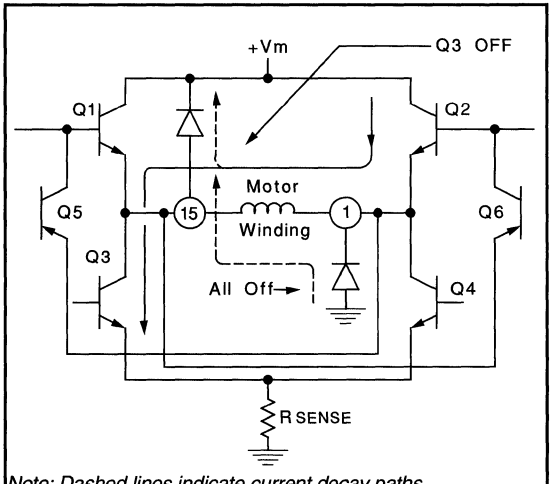


Figure 7. Simplified Schematic of Output Stage

FUNCTIONAL DESCRIPTION (cont.)

PHASE POLARITY INPUT

The UC3717A phase polarity input controls current direction in the motor winding. Built-in hysteresis insures immunity to noise, something frequently present in switched drive environments. A low level phase polarity input enables Q2 and Q3 as shown in Figure 7. During phase reversal, the active transistors are both turned off while winding current delays through the commutating diodes shown. As winding current decays to zero, the inactive transistors Q1 and Q4 turn on and charge the winding with current of the reverse direction. This delay insures noise immunity and freedom from power supply current spikes caused by overlapping drive signals.

PHASE INPUT	Q1, Q4	Q2, Q3
LOW	OFF	ON
HIGH	ON	OFF

CURRENT CONTROL

The voltage divider, comparators, monostable, and two-bit D/A provide a means to sense winding peak current, select winding peak current, and disable the winding sink transistors.

The UC3717A switched driver accomplishes current control using an algorithm referred to as "fixed off-time." When a voltage is applied across the motor winding, the current through the winding increases exponentially. The current can be sensed across an external resistor as an analog voltage proportional to instantaneous current. This voltage is normally filtered with a simple RC low-pass network to remove high frequency transients, and then compared to one of the three selectable thresholds. The two bit D/A input signal determines which one of the three thresholds is selected, corresponding to a desired winding peak current level. At the moment the sense voltage rises above the selected threshold, the UC3717A's monostable is triggered and disables both output sink drivers for a fixed off-time. The winding current then circulates through the source transistor and appropriate diode. The reference terminal of the UC3717A provides a means of continuously adjusting the current threshold to allow microstepping. Table 1 presents the relationship between the two-bit D/A input signal and selectable current level.

TABLE 1

I_0	I_1	CURRENT LEVEL
0	0	100%
1	0	60%
0	1	19%
1	1	Current Inhibit

OVERLOAD PROTECTION

The UC3717A is equipped with a new, more reliable thermal shutdown circuit which limits the junction temperature to a maximum of 180C by reducing the winding current.

PERFORMANCE CONSIDERATIONS

In order to achieve optimum performance from the UC3717A careful attention should be given to the following items.

External Components: The UC3717A requires a minimal number of external components to form a complete control and switch drive unit. However, proper selection of external components is necessary for optimum performance. The timing pin, (pin 2) is normally connected to an RC network which sets the off-time for the sink power transistor during switched mode. As shown in Figure 8, prior to switched mode, the winding current increases exponentially to a peak value. Once peak current is attained the monostable is triggered which turns off the lower sink drivers for a fixed off-time. During off-time winding current decays through the appropriate diode and source transistor. The moment off-time times out, the motor current again rises exponentially producing the ripple waveform shown. The magnitude of winding ripple is a direct function of off-time. For a given off-time T_{OFF}, the values of R_T and C_T can be calculated from the expression:

$$T_{OFF} = 0.69 R_T C_T$$

with the restriction that R_T should be in the range of 10-100k. As shown in Figure 5, the switch frequency F_S is a function of T_{OFF} and T_{ON}. Since T_{ON} is a function of the reference voltage, sense resistor, motor supply, and winding electrical characteristics, it generally varies during different modes of operation. Thus, F_S may be approximated nominally as:

$$F_S = 1/1.5\ (T_{OFF}).$$

Normally, Switch Frequency Is Selected Greater than 20kHz to prevent audible noise, and lower than 100kHz to limit power consumed during the switching cycle.

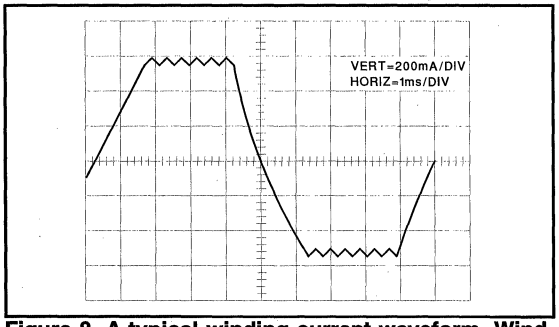


Figure 8. A typical winding current waveform. Winding current rises exponentially to a selected peak value. The peak value is limited by switched mode operation producing a ripple in winding current. A phase polarity reversal command is given and winding current decays to zero, then increases exponentially.

FUNCTIONAL DESCRIPTION (cont.)

Low-pass filter components RC CC should be selected so that all switching transients from the power transistors and commutating diodes are well smoothed, but the primary signal, which can be in the range of 1/TOFF or higher must be passed. Figure 5A shows the waveform which must be smoothed, Figure 5B presents the desired waveform that just smoothes out overshoot without radical distortion.

The sense resistor should be chosen as small as practical to allow as much of the winding supply voltage to be used as overdrive to the motor winding. V_{RS}, the voltage across the sense resistor, should not exceed 1.5V.

Voltage Overdrive: In many applications, maximum speed or step rate is a desirable performance characteristic. Maximum step rate is a direct function of the time necessary to reverse winding current with each step. In response to a constant motor supply voltage, the winding current changes exponentially with time, whose shape is determined by the winding time constant and expressed as:

$$I_m = \frac{V_m}{R\,[1-EXP\,(-R T/L)]}$$

as presented in Figure 9. With rated voltage applied, the time required to reach rated current is excessive when compared with the time required with over-voltage applied, even though the time constant L/R remains constant. With over-voltage however, the final value of current is excessive and must be prevented. This is accomplished with switch drive by repetitively switching the sink drivers on and off, so as to maintain an average value of current equal to the rated value. This results in a small amount of ripple in the controlled current, but the increase in step rate and performance may be considerable.

Interference: Electrical noise generated by the chopping action can cause interference problems, particularly in the vicinity of magnetic storage media. With this in mind, printed circuit layouts, wire runs and decoupling must be considered. 0.01 to 0.1µF ceramic capacitors for high frequency bypass located near the drive package across V+ and ground might be very helpful. The connection and ground leads of the current sensing components should be kept as short as possible.

Half-Stepping: In half step sequence the power input to the motor alternates between one or two phases being energized. In a two phase motor the electrical phase shift between the windings is 90°. The torque developed is the vector sum of the two windings energized. Therefore when only one winding is energized the torque of the motor is reduced by approximately 30%. This causes a torque ripple and if it is necessary to compensate for this, the VR input can be used to boost the current of the single energized winding.

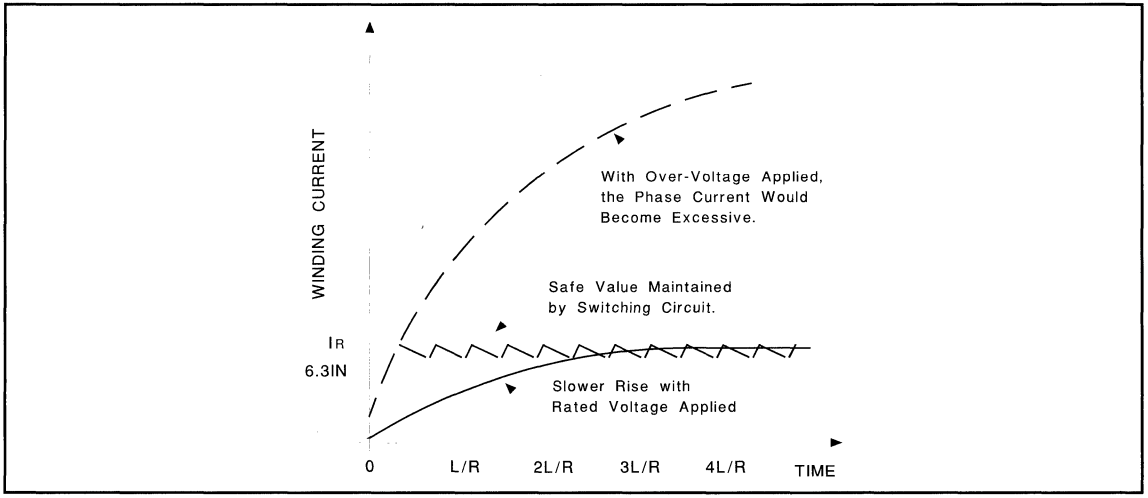


Figure 9. With rated voltage applied, winding current does not exceed rated value, but takes L/R seconds to reach 63% of its final value - probably too long. Increased performance requires an increase in applied voltage, of overdrive, and therefore a means to limit current. The UC3717A motor driver performs this task efficiently.

MOUNTING INSTRUCTIONS

The θ_{JA} of the UC3717AN plastic package can be reduced by soldering the GND pins to a suitable copper area of the printed circuit board or to an external heat sink. Due to different lead frame design, θ_{JA} of the ceramic J package cannot be similarly reduced.

The diagram of Figure 11 shows the maximum package power P_{TOT} and the θ_{JA} as a function of the side " l " of two equal square copper areas having a thickness of 35µ (see Figure 10).

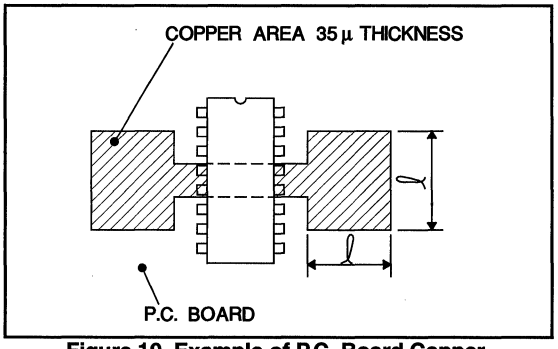


Figure 10. Example of P.C. Board Copper Area which is used as Heatsink.

During soldering the pins' temperature must not exceed 260°C and the soldering time must not be longer than 12 seconds.

The printed circuit copper area must be connected to electrical ground.

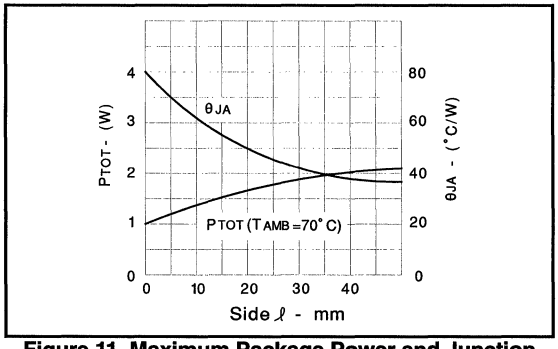


Figure 11. Maximum Package Power and Junction to Ambient Thermal Resistance vs Side "l".

APPLICATIONS

A typical chopper drive for a two phase bipolar permanent magnet or hybrid stepping motor is shown in Figure 12. The input can be controlled by a microprocessor, TTL, LS, or CMOS logic.

The timing diagram in Figure 13 shows the required signal input for a two phase, full step stepping sequence. Figure 14 shows the required input signal for a one phase-two phase stepping sequence called half-stepping.

The circuit of Figure 15 provides the signal shown in Figure 13, and in conjunction with the circuit shown in Figure 12 will implement a pulse-to-step two phase, full step, bi-directional motor drive.

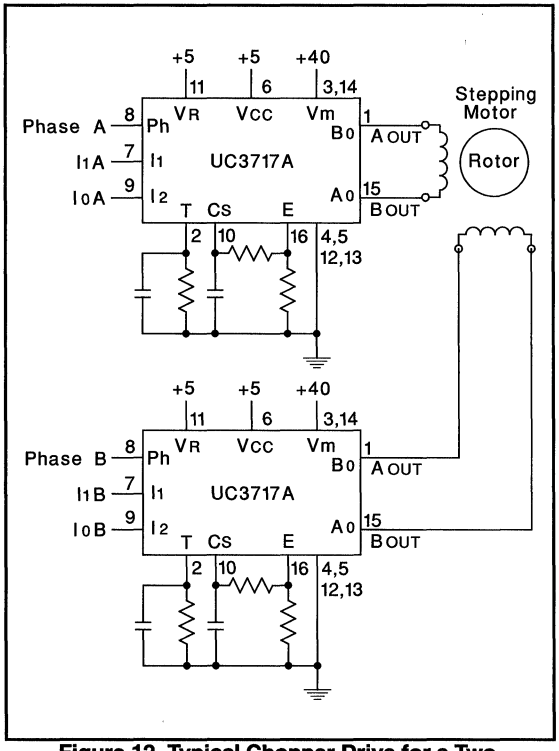


Figure 12. Typical Chopper Drive for a Two Phase Permanent Magnet Motor.

The schematic of Figure 16 shows a pulse to half step circuit generating the signal shown in Figure 14. Care has been taken to change the phase signal the same time the current inhibit is applied. This will allow the current to decay faster and therefore enhance the motor performance at high step rates.

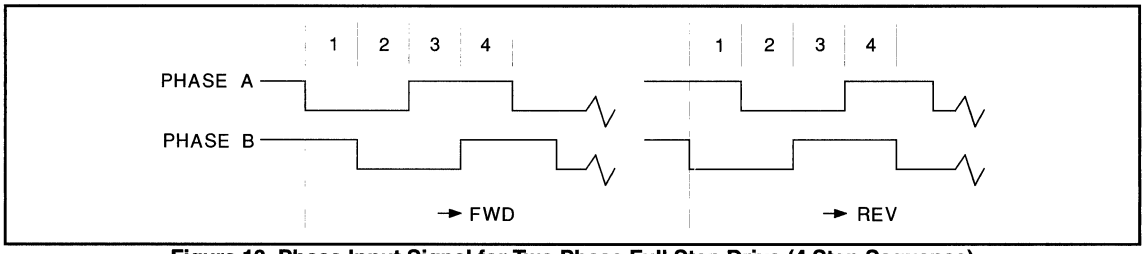


Figure 13. Phase Input Signal for Two Phase Full Step Drive (4 Step Sequence)

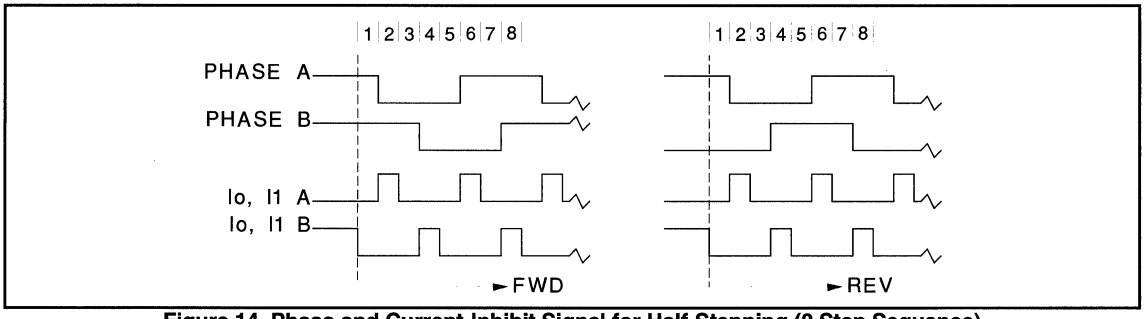


Figure 14. Phase and Current-Inhibit Signal for Half-Stepping (8 Step Sequence)

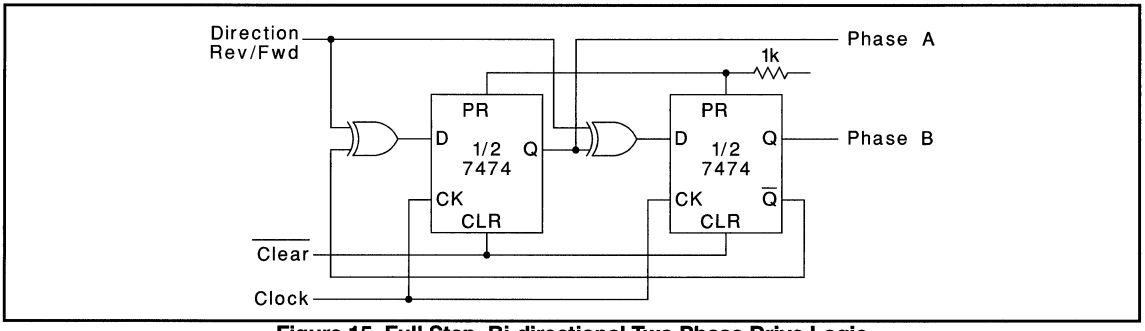


Figure 15. Full Step, Bi-directional Two Phase Drive Logic

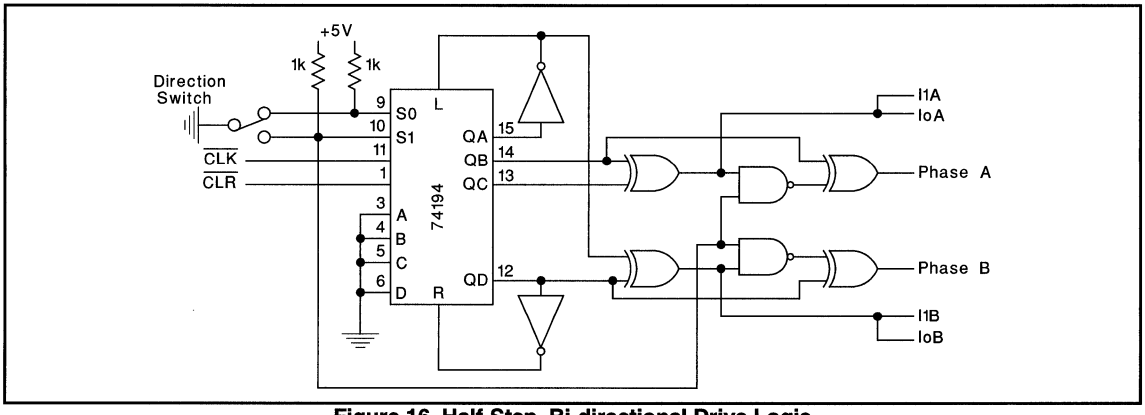


Figure 16. Half-Step, Bi-directional Drive Logic

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High Performance Stepper Motor Drive Circuit

FEATURES

- Full-Step, Half-Step and Micro-Step Capability.
- Bipolar Output Current up to 2A.
- Wide Range of Motor Supply Voltage: 10–50V
- Low Saturation Voltage
- Wide Range of Current Control: 5mA–2A.
- Current Levels Selected in Steps or Varied Continuously.
- Thermal Protection and Soft Intervention.

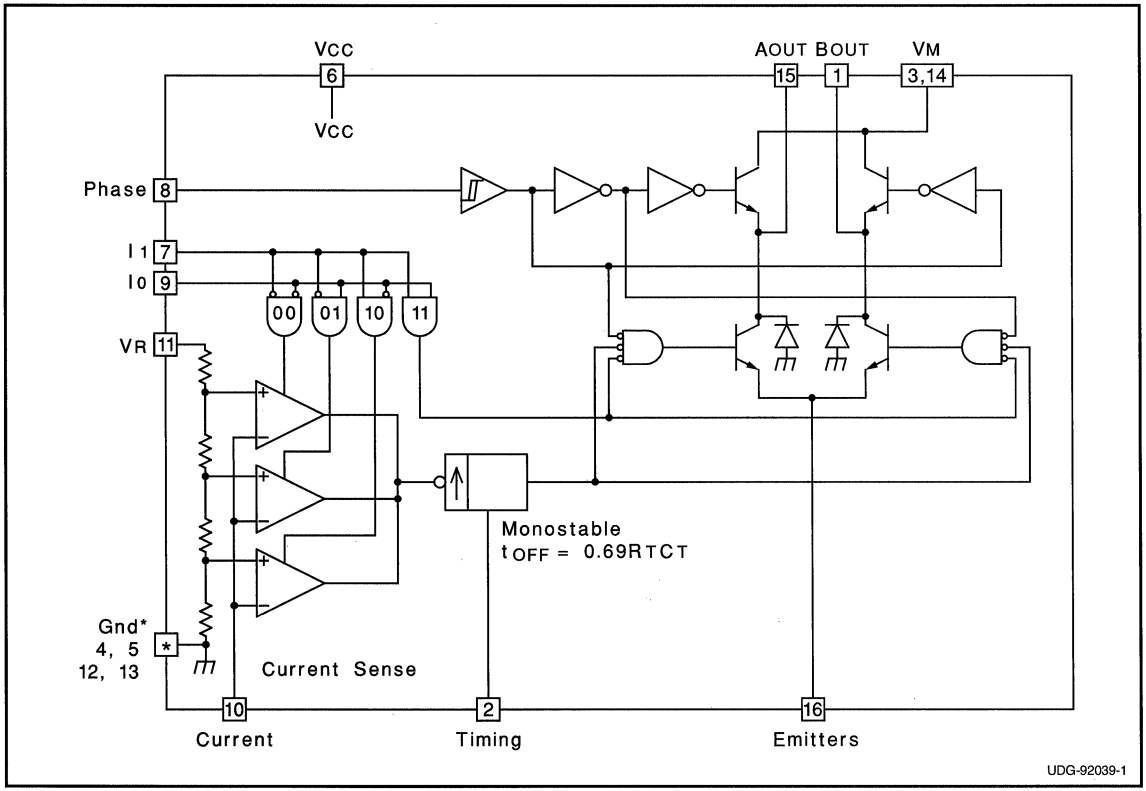
DESCRIPTION

The UC3770A and UC3770B are high-performance full bridge drivers that offer higher current and lower saturation voltage than the UC3717 and the UC3770. Included in these devices are LS-TTL compatible logic inputs, current sense, monostable, thermal shutdown, and a power H-bridge output stage. Two UC3770As or UC3770Bs and a few external components form a complete microprocessor-controllable stepper motor power system.

Unlike the UC3717, the UC3770A and the UC3770B require external high-side clamp diodes. The UC3770A and UC3770B are identical in all regards except for the current sense thresholds. Thresholds for the UC3770A are identical to those of the older UC3717 permitting drop-in replacement in applications where high-side diodes are not required. Thresholds for the UC3770B are tailored for half stepping applications where 50%, 71%, and 100% current levels are desirable.

The UC3770A and UC3770B are specified for operation from 0°C to 70°C ambient.

BLOCK DIAGRAM



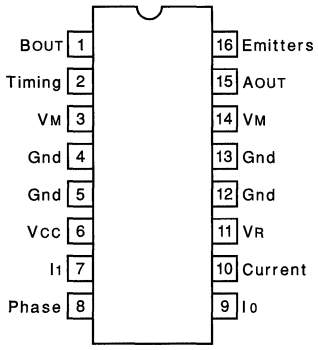
ABSOLUTE MAXIMUM RATINGS

Logic Supply Voltage, V_{CC} 7V
Output Supply Voltage, V_{MM} 50V
Logic Input Voltage (Pins 7, 8, 9) 6V
Analog Input Voltage (Pin 10) ..... V_{CC}
Reference Input Voltage (Pin 11) 15V
Logic Input Current (Pins 7, 8, 9) ..... -10mA
Analog Input Current (Pins 10, 11) ..... -10mA
Output Current (Pins 1, 15) ..... ±2A
Junction Temperature, T_J ..... +150°C

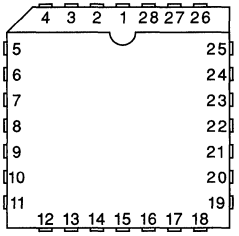
Note 1: All voltages are with respect to Gnd (DIL Pins 4, 5, 12, 13); all currents are positive into, negative out of the specified terminal.
Note 2: Consult Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-16 (Top View)
J Or N Package



PLCC-28 (Top View)
Q Package



PACKAGE PIN FUNCTION	
FUNCTION	PIN
Gnd	1-3
VM	4
N/C	5
AOUT	6
N/C	7
Emitters	8
Gnd	9
BOUT	10
Timing	11
VM	12
Gnd	13-17
VCC	18
I1	19
Phase	20
IO	21
N/C	22
Current	23
VR	24
N/C	25-27
Gnd	28

ELECTRICAL CHARACTERISTICS:

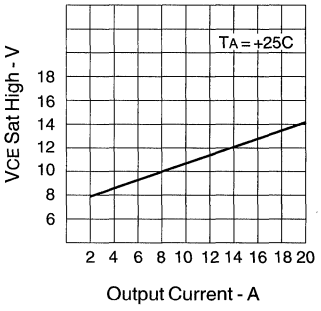
(All tests apply with V_M = 36V, V_{CC} = 5V, V_R = 5V, No Load, and 0°C<T_A<70°C, unless otherwise stated, T_A = T_J.)

		UC3770A			UC3770B			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Supply Voltage V_M (Pins 3, 14)		10		45	10		45	V
Logic Supply Voltage V_{CC} (Pin 6)		4.75	5	5.3	4.75	5	5.3	V
Logic Supply Current I_{CC} (Pin 6)	I_O = I_1 = H, I_M = 0		15	25		15	25	mA
	I_O = I_1 = L, I_M = 0		18	28		18	28	mA
	I_O = I_1 = H, I_M = 1.3A		33	40		33	40	mA
Thermal Shutdown Temperature			+170			+170		°C
Logic Threshold (Pins 7, 8, 9)		0.8		2.0	0.8		2.0	V
Input Current Low (Pin 8)	V_I = 0.4V			-100			-100	µA
Input Current Low (Pins 7, 9)	V_I = 0.4V			-400			-400	µA
Input Current High (Pins 7, 8, 9)	V_I = 2.4V			10			10	µA
Comparator Threshold (Pin 10)	V_R = 5V, I_O = L, I_1 = L	400	415	430	400	415	430	mV
	V_R = 5V, I_O = H, I_1 = L	240	255	265	290	300	315	mV
	V_R = 5V, I_O = L, I_1 = H	70	80	90	195	210	225	mV
Comparator Input Current (Pin 10)				±20			±20	µA
Off Time	R_T = 56k, C_T = 820pF	25	30	35	25	30	35	ms

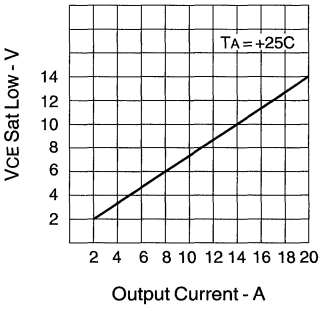
ELECTRICAL CHARACTERISTICS (cont.): (All tests apply with V_M = 36V, V_{CC} = 5V, V_R = 5V, No Load, and 0°C<T_A<70°C, unless otherwise stated, T_A = T_J.)

		UC3770A			UC3770B			
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Turn Off Delay				2			2	ms
Sink Driver Saturation Voltage	I_M = 1.0A			0.8			0.8	V
	I_M = 1.3A			1.3			1.3	V
Source Driver Saturation Voltage	I_M = 1.0A			1.3			1.3	V
	I_M = 1.3A			1.6			1.6	V
Output Leakage Current	V_M = 45V			100			100	µA

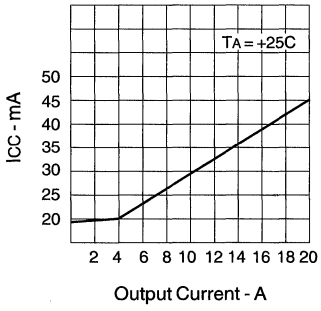
Figre 1: Typical Source Saturation Voltages vs. Load Current



Figre 2: Typical Sink Saturation Voltages vs. Load Current



Figre 3: Typical Supply Current vs. Load Current



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Simple Techniques for Isolating and Correcting Common Application Problems with UC3625 Brushless DC Motor Drives

by Mickey McClure

The UC3625 brushless DC motor control IC incorporates many useful features which greatly simplify the design of low cost and reliable brushless DC motor drive systems. Although the controller IC is designed for ease of circuit implementation, a few precautions must be taken to insure proper operation. This design note highlights a few areas where the IC may not operate correctly if suitable design techniques are not followed.

REFERENCE VOLTAGE

A common application problem is inadequate decoupling and/or excessive loading on the VREF pin of the UC3625. As the data sheet indicates, the maximum recommended current drain on this node is 30mA DC. Much of the UC3625 internal logic is also referenced off of this node and any transient or noise spikes on the VREF pin can result in improper circuit operation. When the VREF pin is affected by noise, the result is usually a "lock up" condition where the motor drive outputs become disabled. This may result from a false trip of the under-voltage lock-out circuit, a false trip of soft start, or an improper decode of the Hall sensors. Other protection signals such as RC-Brake or ISENSE may be affected as well.

A simple trouble shooting technique can be used to determine when an upset of the UC3625 internal logic is causing the lock up condition. The VREF pin of the IC should be isolated from the rest of the circuit and decoupled with at least 0.1µF. Any external +5V circuitry should be powered off of a separate bench supply. The problem should immediately go away if the VREF pin is the culprit. The motor should now operate normally, with no lock up condition.

The solution to this problem will usually involve both reducing the external current drain on VREF and increased decoupling. Every effort should be made to reduce the DC current drain as low as possible so that any AC currents will have less impact on VREF. The Hall sensors should be powered by something other than VREF, such as VCC. While there is no general rule on how much DC current is too much, as DC currents approach 30mA, there will be more reason to suspect that VREF is the source of the lock up condition.

AC current will be drawn from the VREF point when it is used to provide the pull up voltage for the Hall inputs to the UC3625. Noise spikes caused by this current drain may be severe enough to latch false logic states on the internal protection circuitry if adequate decoupling is not provided. The reference voltage should **always** be decoupled to ground with a high quality ceramic capacitor of at least 0.1µF located as close as possible to VREF and ground pins. An electrolytic capacitor should be placed in parallel with the ceramic capacitor if there is any significant DC loading on the reference voltage. A value of 10µF is usually sufficient. The placement of the electrolytic capacitor is not as critical, but it should be located as close to the ceramic capacitor as practicality will allow. Figure 1 shows the recommended power connections and decoupling for a typical UC3625 motor drive system.

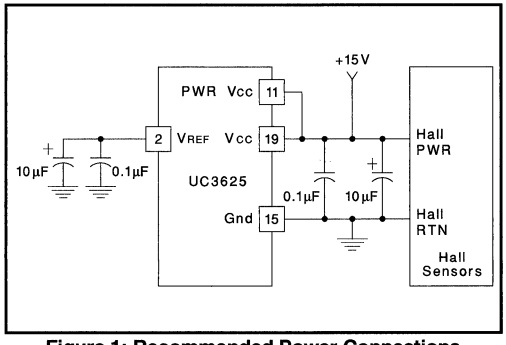

Figure 1: Recommended Power Connections and Decoupling

HALL INPUTS

High power motor drive systems are frequently characterized by large noise spikes induced by high frequency switching. Under certain conditions these noise spikes can trigger Hall sensor inputs to latch improper commutation states. If an improper commutation state is latched, the correct state is then locked out for the duration of the tach-out pulse. The result is not generally a lock out condition, but rather a motor that responds in a sluggish or unpredictable manner.

As indicated by the UC3625 data sheet, any change in the H1, H2, or H3 inputs loads data from the position sensor latches. Because the position latches are inhibited for the duration of the user programmable tach-out pulse, a noise induced state will lock out the correct commutation state. The power amplifier will then energize the wrong windings of the motor, possibly resulting in reduced torque, or zero or negative torque depending on which incorrect state is latched in. The controller will allow a new state to latch once the tach-out pulse times out. Normal operation may resume at this time, or the noise related problems may continue. The response of the motor is therefore erratic and unpredictable.

This problem can be traced with a logic analyzer or four channel oscilloscope connected to the three Hall inputs and the tach-out pulse. For normal operation, the logic analyzer should display the correct sequence of the Hall signals, and the tach-out pulse should occur at regular intervals proportional to the motor velocity. Incorrect commutation states are indicated by the tach-out pulse occurring at random intervals. These incorrect states may or may not show up on the analyzer display, depending on the frequency and amplitude of the noise.

The problem can usually be corrected by passive filtering of the Hall inputs. An RC network of 1k and 2.2nF is recommended with the filter components located as close as possible to the IC. Small delays in the filter are not a problem because the sensors normally generate modified gray code with only one output changing at a time. The rise and fall times of the Hall signal edges must be shorter than 20µs for correct tachometer operation. Figure 2 depicts the recommended implementation of this filter technique.

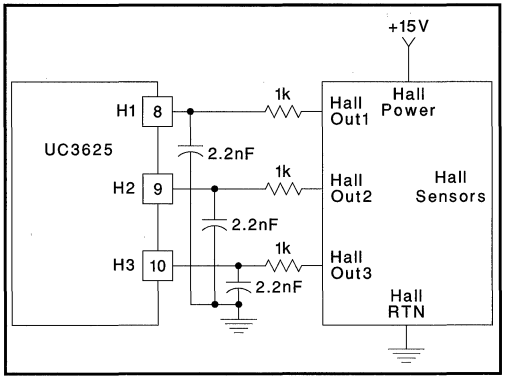

Figure 2: Recommended Hall Filtering

A more noise tolerant solution involves inserting comparators between the Hall sensors and the UC3625 if the passive technique is not sufficient. Because Hall sensors are typically open collector drivers, their outputs can easily become corrupted when driving long cables in a high noise environment. Much greater signal integrity can be achieved by using comparators configured with a large amount of hysteresis to attain greater noise margin. They must be configured in the noninverting mode so that the correct Hall states will be latched by the UC3625. Figure 3 shows an example circuit for driving the Hall inputs with comparators.

CURRENT SENSE CIRCUITRY

The UC3625 current sense circuitry must also be configured correctly to prevent improper circuit response. Noise problems may cause the UC3625 to supply less current to the motor than the controller commands, resulting in poor motor response, and possibly undesired torque limiting.

The most important factor in achieving proper current limit response is a correct differential measurement of the voltage across the current sense resistor. Separate traces must be run from the I_{SENSE1} and I_{SENSE2} inputs directly to the current sense resistor. If an input filter is used, it should be balanced, and the filter resistors should tie directly to the current sense resistor. Recommended component values for the differential filter are 270Ω and 4.7nF. **Never** should one I_{SENSE} input line be simply grounded and the other input

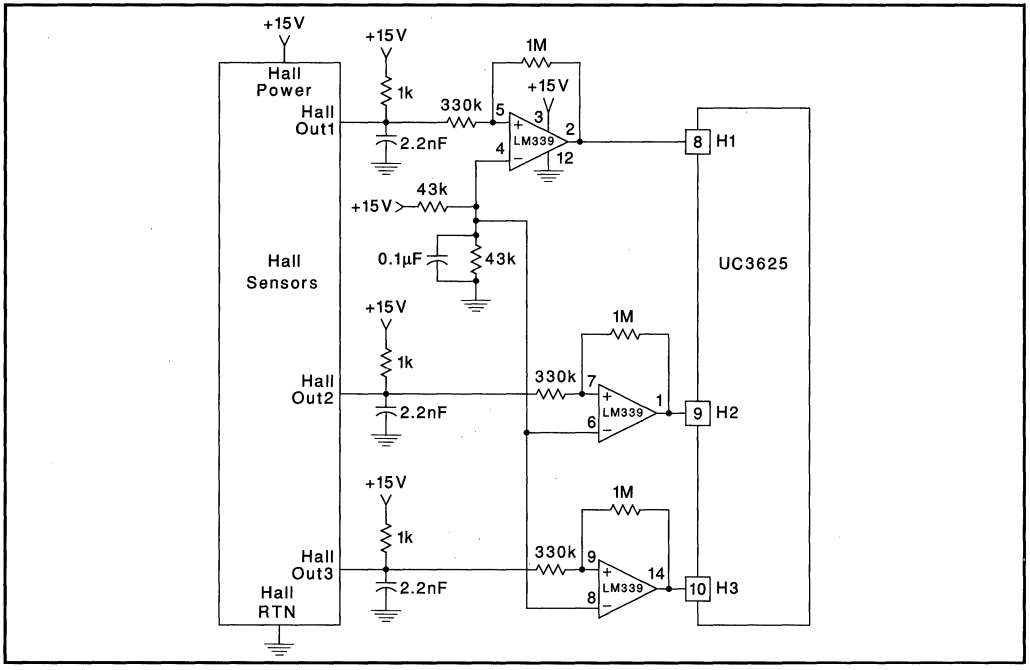

Figure 3: Comparator Sense of Hall Sensors

driven single ended. The recommended circuit layout for the ISENSE1 and ISENSE2 input signals is shown in Figure 4.

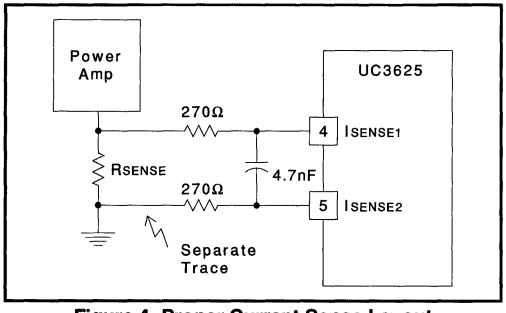

Figure 4: Proper Current Sense Layout

Additional noise immunity can be achieved by adding a capacitor from the ISENSE output to ground. This capacitor should be located as close as possible to the ISENSE pin, and a low impedance path to ground for its low side is essential. Filtering at this point has the advantage of allowing fast signal inversions to be correctly processed by the absolute value circuit before filtering takes place.

If high levels of common mode noise or ground bounce are affecting the ISENSE inputs it may be necessary to decouple the ISENSE inputs (pins 4 and 5) to ground with 470pF capacitors. These capacitors will shunt out any high frequency common mode noise, and allow for a more accurate measurement of true motor current.

NONLINEARITY PROBLEMS ASSOCIATED WITH NOISE ON THE TIMING CAPACITOR

Switching noise can result in discontinuities in the linear response of the PWM circuitry if the timing capacitor on the RC-OSC pin is not located properly. The UC3625 creates the sawtooth waveform by measuring the voltage across the capacitor tied

between RC-OSC and ground. This voltage is charged by a constant current source, and is discharged when a fixed threshold is reached. The output duty cycle of the power stage is determined by comparing the error amplifier output to the sawtooth waveform. When the magnitude of the sawtooth waveform is greater than the output of the error amplifier, the output stage is switched off.

Large current spikes can result in localized ground bounce when the power stage switches. The low side of the capacitor can be "pumped up" if the timing capacitor is not located near the IC. This problem will result in the oscillator comparator tripping early, and the sawtooth waveform will jump to a higher frequency. The effect will be a nonlinear PWM gain function. Since the PWM is usually part of the forward loop, this will not be a problem in many closed loop systems because the outer control loop will simply compensate for the nonlinearity.

For cases where the nonlinearity is a problem, the situation can usually be mitigated by connecting the timing capacitor directly across the RC-OSC and GND pins of the UC3625. Since the internal comparator is referenced from this local ground point, the correct trip point will be maintained and the frequency of the oscillator will remain constant.

For some cases it may be necessary to add a low value resistor in series with the Pwr-Vcc pin or the output (PD and PU) pins of the UC3625. These resistors will limit the peak value of transient currents in the output driver stage of the IC. By minimizing these currents, the amount of ground bounce can be reduced, and therefore the nonlinearity problem can be curtailed.

While the previously described techniques will result in a more robust and reliable motor drive design, they are by no means the answer to every problem. As with all analog circuitry, there is no substitute for good circuit design and layout practice when designing with the UC3625. Every effort should be made to keep all signal runs as short as possible, and avoid running sensitive traces near each other. Finally, proper grounding techniques should always be maintained, as well as careful attention to EMI reduction.

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Design Considerations for Synchronizing Multiple UC3637 PWMs

by Mickey McClure

As motion control and power interface systems become more complex, the need for more sophisticated control circuitry arises. One common application involves the need for synchronizing multiple pulse width modulators (PWMs). This requirement may result from the need to eliminate beat frequencies when multiple PWMs reside on the same printed circuit board, or from timing considerations in redundant systems where voting between drivers is required.

The UC3637 is an extremely versatile PWM used in many motor control and power driver applications, and the need for synchronization often arises. In order to properly accomplish this, a few simple design rules must be followed. These rules apply primarily to resetting the part's current limit latches.

Figure 1 shows a block diagram of the UC3637. In a single PWM configuration, the triangle waveform, and therefore the operating frequency of the PWM is developed by charging and discharging a capacitor at pin 2, and comparing the voltage across this capacitor to the threshold voltages applied at pins 1 and 3. The design equations for this circuit are discussed extensively in Unitrode Application Note U-102, "Switched Mode Controller For PWM DC Motor Drive."

The most common configuration for synchronized PWMs is a single master PWM driving one or more slave PWMs. In this case the triangle wave is developed by the master exactly as it is in the single PWM case. The master triangle wave is then used to drive the PWM comparators on the one or more slave ICs. The only major concern is resetting the slave current limit comparators.

Figure 2 shows a simple circuit for operating synchronized UC3637 PWMs in a master/slave configuration. The important point to note about this circuit is that the pulse be pulse current limiting feature of the UC3637 is not used. The triangle wave is developed by the master, and used to drive its own PWM comparators as well as the slave PWM comparators. The threshold levels and the CT pin of the slave IC are tied off to levels which force the current limit comparators to stay in the nonlimit state. With the slave CT grounded, and the slave +VTH tied to a

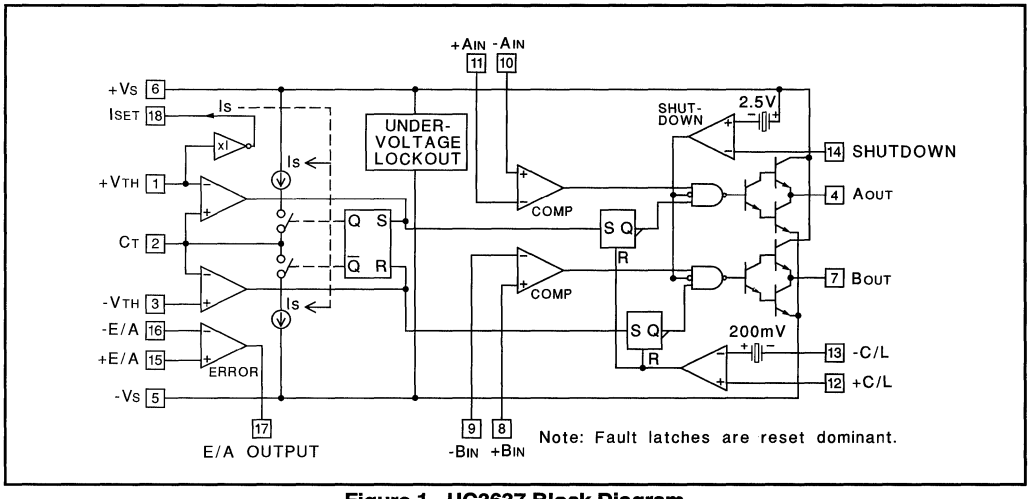

Figure 1. UC3637 Block Diagram

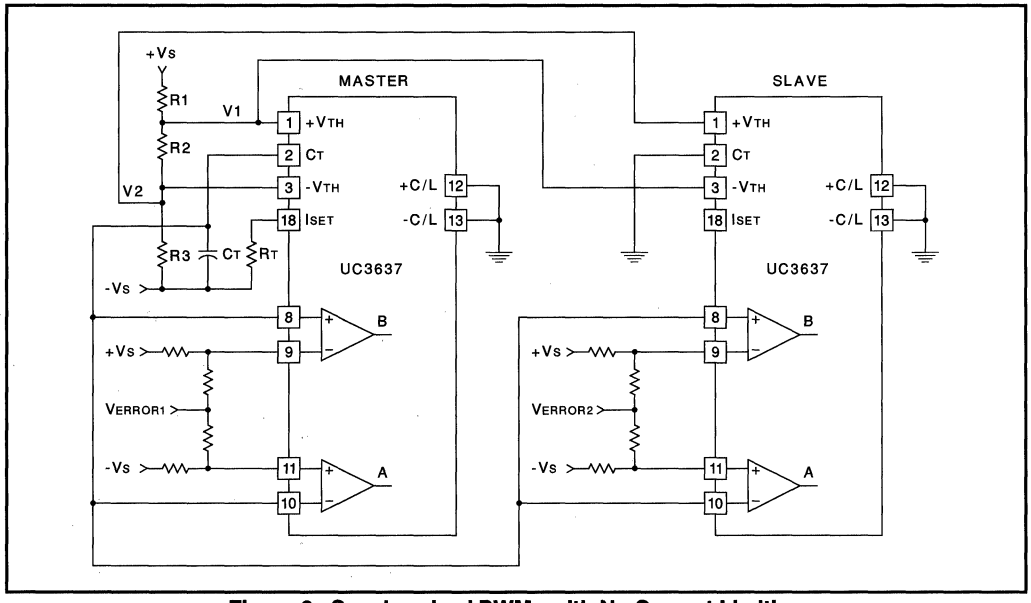

Figure 2. Synchronized PWMs with No Current Limiting

negative level, the A output current limit comparator will always keep the drive active. The B drive will also be active because -VTH is tied to a positive level. The threshold levels can not simply be tied to the supply rails because those voltages are outside of the common mode range for the comparators.

As long as CT is kept greater than 1000pF, the input capacitance of the slave comparators will not affect the oscillator frequency. If long signal runs are required, or many PWMs need to be synchronized, it is best to buffer the triangle wave with an op amp at the master IC.

While the circuit of Figure 2 is quite simple, current limiting requirements often rule out its use. The circuit shown in Figure 3 should be used for those applications where both current limiting and synchronization are required. In this circuit, the current limit comparators of the slave PWM are tied to threshold levels of the same polarity but lower magnitude than the threshold levels of the master. Independent pulse by pulse current limiting is accomplished by guaranteeing that the slave current limit comparators get reset each cycle. This can be assured by setting the difference between the master and slave threshold levels (dV) so that even with worst case offsets in both the master and slave ICs the magnitude of the master triangle wave will always be great enough to reset the comparators. The following equations outline a procedure for determining the minimum dV for the positive threshold. The dV for the negative threshold is determined by the same procedure:

1) $dV = V1 - V3$

The minimum dV must be able to compensate for the worst case offset errors of the threshold comparators. These errors result from both offset voltage and bias currents:

2) $V_{ERROR1} = (I_{BIAS}) \bullet Req$

3) $Req = \dfrac{R1 \bullet (R2+R3+R4+R5)}{R1+R2+R3+R4+R5}$

4) $V_{ERROR2} = V_{OS} = 150mV$

The worst case error occurs when the offsets of the master are opposite to the offsets of the slave. The offsets than add to each other to give the minimum dV requirement:

5) $dVmin = 2 \bullet (V_{ERROR1} + V_{ERROR2})$

The set point for dV is determined by adding the

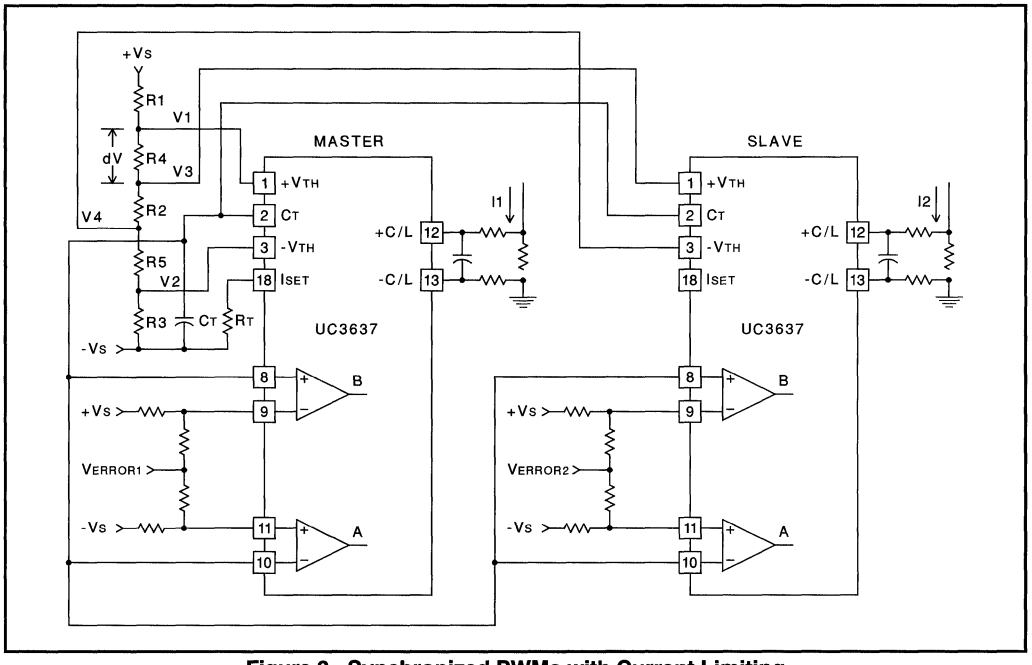

Figure 3. Synchronized PWMs with Current Limiting

maximum tolerance on dV to the minimum dV value. Because dV is set by a resistor divide network with independent terms in both the numerator and denominator of its voltage equation, the total error term is a function of twice the resistor tolerance, as well as the supply voltage. Taking these error sources into account yields the set point for dV:

6) $dV_{SET} = dVmin + dVmin \bullet (2) \bullet$ (resistor tolerance) $\bullet$ (power supply tolerance)

We now select R4 by:

$$7)\ dV_{SET} = \frac{(+Vs - (-Vs)) \bullet R4}{R1+R2+R3+R4+R5} \quad \text{or}$$

$$R4 = \frac{dV_{SET} \bullet (R1+R2+R3+R5)}{(+Vs - (-Vs)) - dV_{SET}}$$

It should be noted that deriving the threshold levels for the slave PWM off of the same divide network as the master allows for much better tracking of dV. Since the difference between the master and slave threshold levels is small compared to the absolute voltage levels, the resistor tolerance becomes much less significant. If the slave threshold levels were derived off of separate networks, the resistor tolerance would affect the absolute threshold level by the tolerance of the resistors, resulting in a much higher percentage change in dV.

While these two simple circuits will suit the requirements of most synchronized systems, there may be cases where more complex circuitry is required. If a digital square wave clock is used to synchronize many PWMs, an integrator may be required to derive the triangle waveform. For certain critical systems, a phase lock loop may be more desirable as a synchronization mechanism. As always, the individual designer must evaluate the system requirements before a final design configuration can be selected.

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Design Note

Closed Loop Temperature Regulation Using the UC3638 H-Bridge Motor Controller and a Thermoelectric Cooler

By David Salerno

INTRODUCTION

Have you ever wanted to test an IC over temperature, but couldn't put the entire application circuit in the oven? Maybe you needed to access critical circuit nodes for troubleshooting, or observe the effects of temperature on only one component. Freeze sprays and hair dryers may be good for benchtop troubleshooting, but the temperature (and temperature slew rate) is highly uncontrolled and may actually damage the part. Forced air systems which direct temperature controlled air to a specific area are available, but they are large, cumbersome and expensive. What is needed is a portable, low cost, temperature forcing system.

One solution is to use a thermoelectric cooler. Thermoelectric coolers (TEC's) employ the Peltier effect, acting as small, solid state heat pumps when a DC current is passed through them. They are relatively small, flat devices which transfer heat from one side to the other. The direction of heat transfer can be reversed, for heating or cooling, by simply reversing the direction of the current. The amount of heat transfer is controlled by the magnitude of the current. A temperature difference across a TEC of up to 50°C or more can be achieved using a single element if proper heatsinking is provided on one side of the device. Larger temperature gradients can be produced by stacking multiple elements. They can be used effectively as part of a closed loop temperature regulation system.

A number of methods can be used to regulate the magnitude and direction of the TEC current, since they operate at a relatively low DC voltage (maximum current ranges from 1A to 10A, depending on size). Linear regulation can be used, but would be very inefficient and would require bipolar supplies, or some means of switching polarity to reverse the direction of current flow. Switching techniques, using pulse width modulation, can be used to improve efficiency. If heat transfer is only required in one direction, for heating or cooling (but not both), a simple buck topology, operating from a single supply voltage, can be used to regulate the output current in one direction. However, in this case, to allow both closed loop heating and cooling from a single supply, a bridge topology is necessary . A simplified block diagram of the closed loop temperature control system is shown in Figure 1.

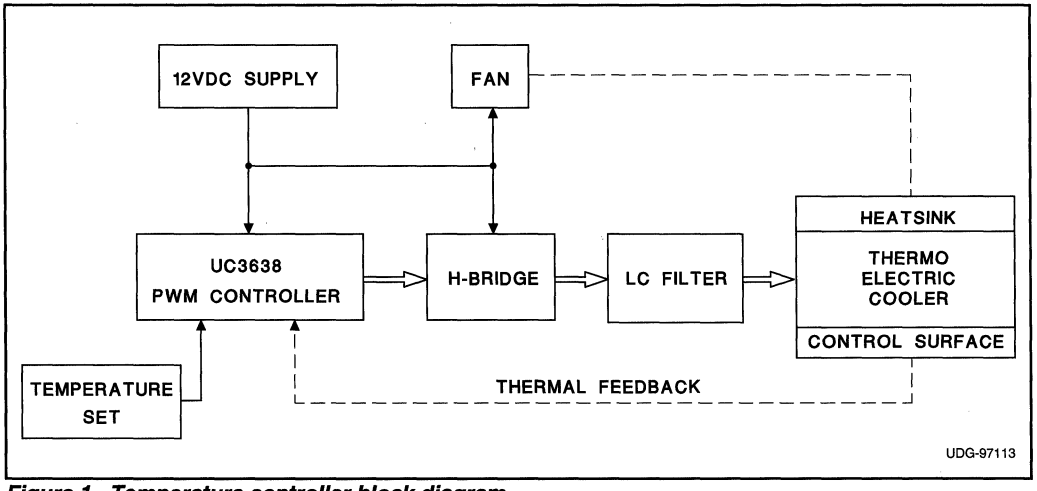

Figure 1. Temperature controller block diagram.

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Pulse width modulation minimizes conduction losses in the control electronics, but requires a sophisticated PWM controller, especially to prevent problems such as bridge cross-conduction. The building blocks required for closed loop PWM control, such as a voltage reference, error amplifier, pulse width modulator, oscillator, current sense amplifier, and FET drivers, as well as features such as undervoltage lockout (UVLO) and pulse-by-pulse current limiting, are all contained in the UC3638. The biasing circuitry needed for single supply operation is also included. A block diagram of the IC is shown in Figure 2.

The circuit in Figure 3 uses the UC3638 H-bridge controller, four FET's, a differential LC filter and a TEC to form a closed loop temperature regulator. A PWM frequency of 100kHz is set by R15 and C13. This frequency was chosen as a compromise to limit switching losses in the bridge while minimizing the size of the LC filter components. The deadtime between commutation of the bridge switches is set by the voltage on the DB pin, using the divider of R12-R14. The voltage on PVSET determines the amplitude of the triangle wave oscillator used in the PWM modulator.

MOSFET's Q1-Q4 form the bridge, while BJT's Q5-Q8 act as high side FET drivers, since outputs AOUT1 and BOUT1 of the UC3638 are open collector. AOUT2 and BOUT2 can drive the low side MOSFET's directly. Schottky diodes D1 and D2 clamp any ringing below ground due to stray circuit inductance. Sense resistor R6 is chosen to limit the peak output current to 5 Amps. The current sense voltage is amplified by the UC3638, and any noise spikes are filtered by C12 and a 100Ω resistor internal to the IC.

The LC output filter, formed by L1, L2 and C2-C6, is required to convert the PWM output from the bridge back to a DC voltage. This is necessary because AC ripple is detrimental to the TEC, and its efficiency drops off rapidly. Less than 10% ripple is recommended. The resulting architecture is a low

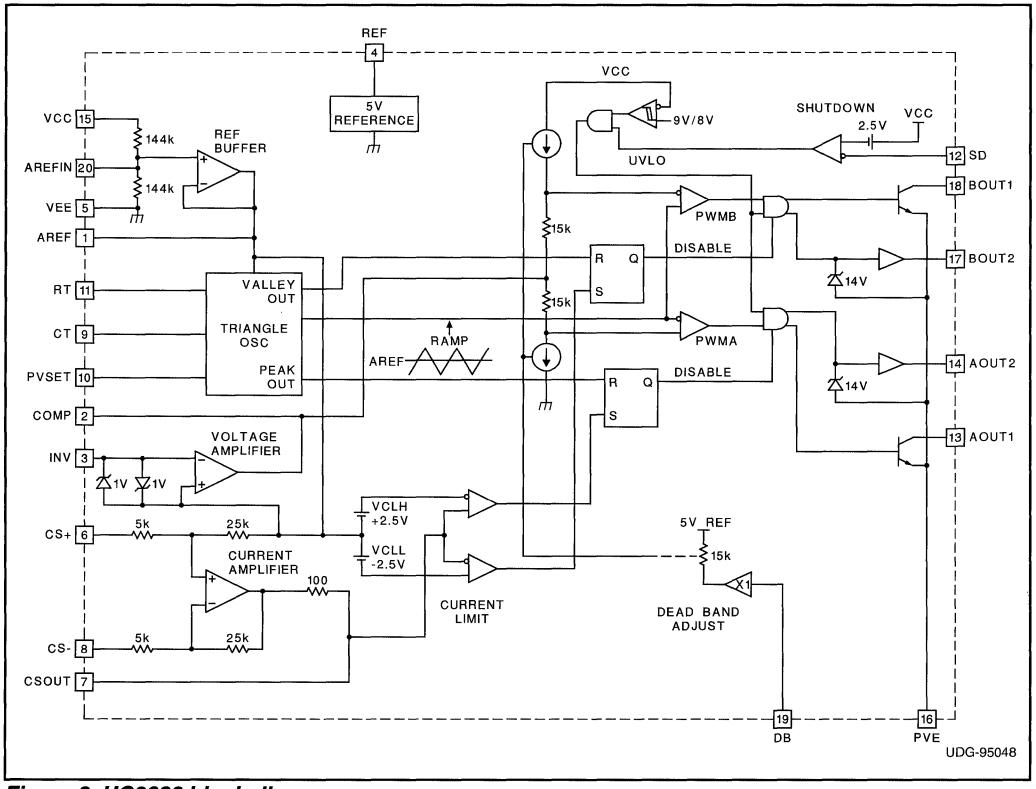

Figure 2. UC3638 block diagram.

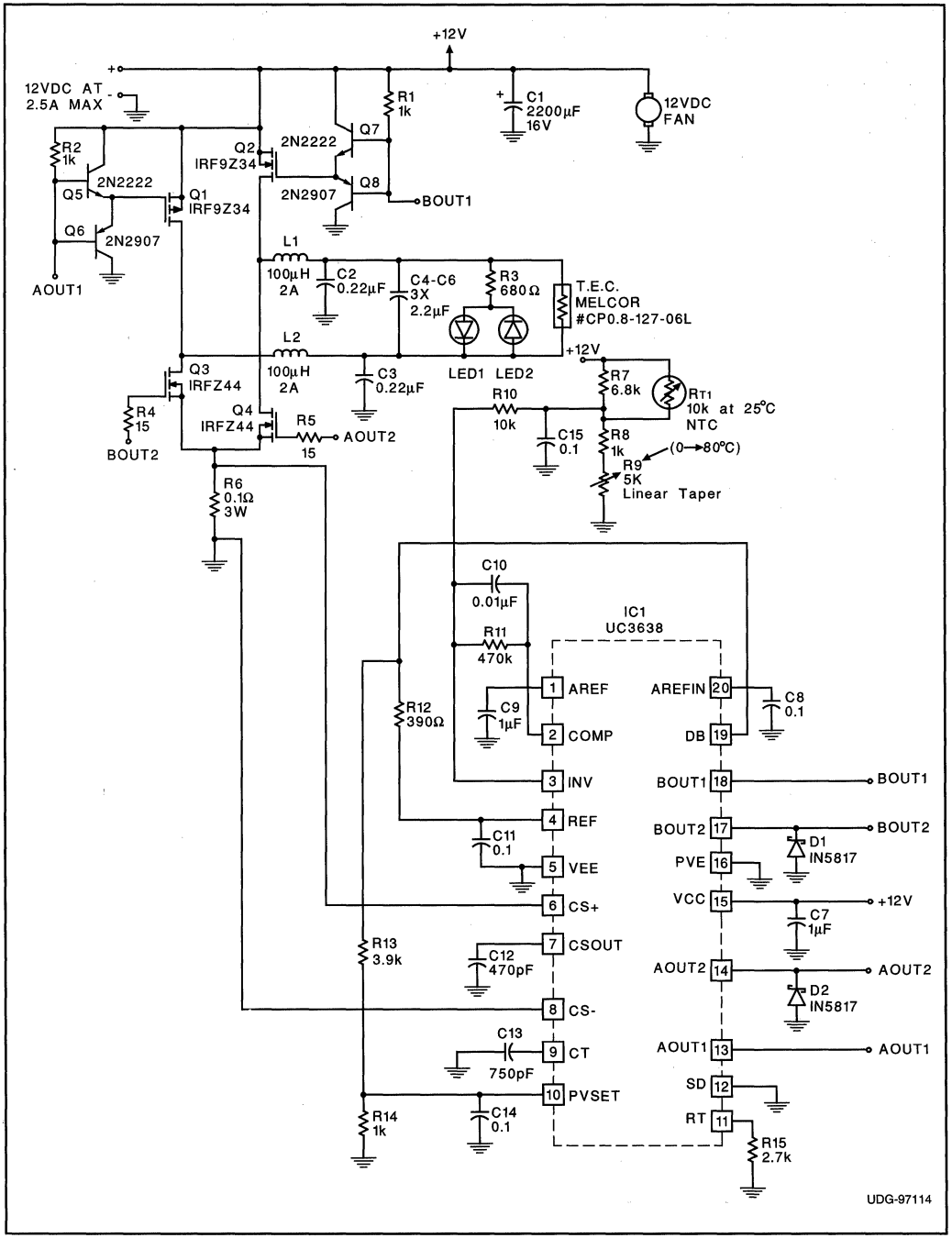

Figure 3. Circuit diagram of the temperature regulator using the UC3638 controller.

bandwidth class D amplifier, which can deliver a variable DC voltage up toæ12V at several amps to the TEC. At these currents, no heatsinking of the MOSFET's is required. If a higher current TEC is used, heatsinking of the MOSFET's may be required, primarily due to conduction losses. Another alternative is to use MOSFET's with a lower RDS_{ON}.

To dissipate the heat transferred and generated by the TEC losses, a heatsink and 12VDC fan are mounted in close thermal contact with one side of the device. An aluminum "cold plate" is mounted on the other side, forming a sandwich with the TEC in the middle. The aluminum plate, acting as the control surface, adds thermal mass to help stabilize the loop while protecting the brittle ceramic surface of the TEC. This plate is placed in intimate thermal contact with the item to be temperature controlled.

RT1, an NTC thermistor, is placed in a hole in the side of the aluminum plate to provide good thermal feedback to close the loop. A parallel resistor helps to linearize the thermistor's response. This is not critical, since the temperature control pot will be calibrated, compensating for any non-linearities.

The UC3638 error amplifier compensation uses proportional gain, since it can be difficult to compensate an integral loop due to the long thermal time constant of the mechanical system. The DC gain of the error amplifier, determined by R10 and R11, is high enough so that a temperature error of <1°C will produce full output voltage to the TEC. C10 provides a pole to filter out any noise before reaching the modulator. Note that the amplitude of the triangle wave oscillator (set by R13 and R14) also affects overall loop gain.

Temperature control pot R9 is calibrated using a thermocouple temporarily mounted to the aluminum plate. Once calibrated, it is accurate and repeatable to within 1°C. LED's across the output of the filter give a visual indication of whether the TEC is heating or cooling, depending on the polarity of the output voltage.

The entire system, using the TEC shown, operates off a 12VDC, 2.5A power supply and provides closed loop temperature regulation of a surface about 1 inch square. The temperature of the control surface can be varied from 0°C to +80°C in a room ambient environment. Hotter and colder temperatures are possible if multiple devices are stacked and proper heatsinking is provided. Remember that cooling can only take place if the heat, including that produced by the efficiency losses in the TEC, can be dissipated on the opposite surface. Note that the maximum temperature is ultimately limited by the temperature rating of the solder within the TEC. Devices with ratings of up to +200°C are available.

TEC's can be used in many temperature control applications. They are available in a wide variety of shapes, sizes, power and voltage ratings from a number of manufacturers. Some manufacturers also supply heatsinks, cold plates and fans. However, low cost Pentium style heatsink and fan combinations can often be adapted.

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UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor

A chopper drive which uses the inductance of the motor as the controlling element causes a temperature rise in the motor due to hysteresis and eddy current losses. For most motors, especially solid rotor constructions, this extra heat can force the designer to go to a larger motor and then derate it, or to a more expensive laminated construction in order to produce enough output torque for the job. Regardless of the motor type, any extra heat generated within a system will have to be removed or else other system components will be stressed unnecessarily. This could mean using a fan where convection cooling might otherwise have sufficed. In addition, the EMI generated from both the motor and its leads is of serious concern to the designer in view of ever-increasing EMI regulations.

These problems can be virtually eliminated by borrowing a simple technique from switching power supply designs, i.e., by placing a properly designed low-pass L-C filter across the output and using *this* L to control the UC3717. This removes the high frequency AC chopping losses in the motor by providing it with almost pure DC current. It also confines the EMI-causing, high frequency AC components to within the driver where they are easier to handle. This could allow increased wire lengths and possibly free up some design constraints, but remember that even though DC emits no EMI, the driver will still commutate the windings and can produce some components of frequency as high as 10 kHZ. The design of the L-C filter is straight-forward and its small additional cost can be recovered easily. The Unitrode UC3717, a complete chopper drive for one phase winding on a monolithic IC, makes the design job simple. The end result, a cooler running and EMI quieter step motor, can be achieved with just a few additional passive components.

Preliminary Considerations

For our analysis, we will use a "23" frame, bipolar motor with a solid rotor and the following specifications:

P_{max} =	9.0 Watts	= Maximum power dissipation at 25°C
V_{max} =	3.75 Volts	= Maximum voltage per motor phase at 25°C
I_{max} =	1.25 Amps	= Maximum current per motor phase at 25°C
R_m =	3.0 Ohms	= Resistance of one phase at 25°C
*L_m =	8.4 mH	= Inductance of one phase winding

*It should be noted that L_m, as given in a manufacturers data sheet, is not always *true average* inductance as seen at high current in a circuit, but rather the inductance reading you would obtain from a low current inductance bridge. This value can differ from in-circuit inductance by a factor of 2 or more! The in-circuit inductance for this motor is 5.0 mH.

We begin by calculating the electrical time constant of one phase winding using the resistance value given above and the *actual* motor inductance:

$$\tau_m = \frac{L_m}{R_m} = \frac{5.0\ \text{mH}}{3.0\ \text{Ohms}} = 1.67\ \text{msec} \quad (1)$$

If one were using a standard voltage drive then it would take approximately τ_m or 1.67 msec to reach the current level required for proper operation. This places a severe restriction on motor speed. Increasing the drive voltage will allow the motor to run faster but will cause it to draw too much current and overheat. Maximum motor speed may be increased by decreasing the time constant. Since L_m is fixed, the only parameter we can change is the effective value of R_m by placing a resistor in series with it. If we place a resistor 4 times R_m in series such that total R is 5 times R_m and increase the drive voltage by a factor of 5 then we will have reduced the time constant by a factor of 5 to 330 μsec and also increased both the maximum motor speed and maximum power output by a factor of 5 each. Unfortunately, we will have increased wasted power by a factor of 5 also.

The Chopper Drive

Using a chopper drive enables one to run at a higher voltage and thus reach proper operating current faster while still protecting the motor from excessive current that would otherwise flow due to the higher voltage. The high voltage is first applied across the motor winding and then, when I_{max} is reached, it is switched off. (If it were not switched off then the maximum current rating of the motor would be quickly exceeded.) The current is then allowed to circulate in a loop within the driver and motor for a fixed time period (t_{off}) after which the voltage is re-applied to the motor. The operating frequency, which is determined by both the motor inductance and t_{off} should be high enough that the resulting current ripple is small compared to the average DC current. Power efficiency is relatively high because there is no external resistor used.

Nothing is free in the world of physics, however, and the price one pays for the extra power output capability is an increase in wasted heat due to hysteresis and eddy current losses *within* the motor instead of in an external resistor. Being within the motor, it can now cause overheating as well as reliability problems. Since the excess heat increases rapidly with the overdrive ratio, this means that at low overdrive ratios (less than 5-to-1) there will be almost negligible heating, but at higher overdrive ratios (more than 10-to-1) the induced motor losses can become as great as, or actually exceed, the I^2R losses! By placing a low-pass L-C filter in the circuit these induced losses can once again become negligible. The L and C components selected should be capable 'of operating at frequencies of 25 kHz or higher without heating effects in the inductor core or inductive effects in the capacitor.

UC3717 and L-C Filter

Designing with the UC3717

Using a supply voltage (v_s) of 40 volts (approximately a 10/1 overdrive), the turn-on rise-time becomes:

$$t_{rise} = -\tau_m \times Ln\ (1 - V_m/V_s) = -1.67 \times 10^{-3} \times Ln\ (1 - 3.75 / 40)$$
$$= 164\ \mu sec \quad (2)$$

or *an improvement of approximate/y 10-to-1 in speed capability.*

Using an off-time (t_{off}) of 30 μsec as suggested on the UC3717 data sheet and limiting current (I_w) to 850 mA establishes a voltage across the resistive component of the winding ($V_{w\text{-}on}$) during the "on" time of:

$$V_{w\,on} = I_w \times R_w = .85 \times 3.0 = 2.55\ Volts \quad (3)$$

and during the "off' time (due to a 2.6 volt drop across the upper transistor, as shown in the data sheet, and a 0.4 volt drop across the Schottky "catch" diode) of:

$$V_{w\,off} = V_{transistor} + V_{diode} = 2.6 + 0.4 = 3.0\ Volts \quad (4)$$

Since the voltage and current changes are small, we can substitute a resistance (R_e)equivalent equivalent to$V_{w\text{-}off}/I_w$ in series with $R_w$to adjust the time constant and allow us to calculate the approximate current ripple (ΔI_w) during t_{off}:

$$\Delta I_w = I_w \left(1 - \exp.\left[\frac{-t_{off}(R_w + R_e)}{L_m}\right]\right)$$
$$= .85 \times \left(1 - \exp\left[\frac{-30\times10^{-6} \times (3.0 + 3.5)}{5\times10^{-3}}\right]\right)$$
$$= 33\ mA\ p\text{-}p \quad (5)$$

Knowing ΔI_w, we can now calculate the on-time (t_{on}):

$$t_{on} = \frac{\Delta I_w \times L_m}{V_s - V_{w\text{-}on}} = \frac{33\times10^{-3} \times 5\times10^{-3}}{40 - 2.55} = 4.4\ \mu sec \quad (6)$$

and can also find our operating frequency (f) by:

$$f = 1 / (t_{on} + t_{off}) = 1 / (4.4 + 30) \times 10^{-6} = 29.1\ kHz \quad (7)$$

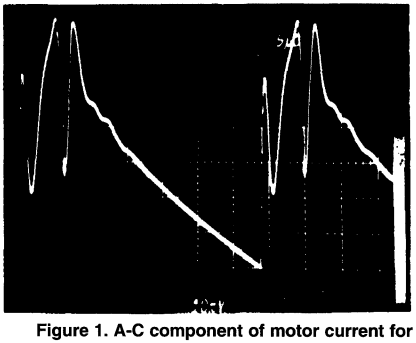


Figure 1. A-C component of motor current for standard chopper configuration.

Since this frequency is well above audible ranges, it will not cause any objectionable sound, but there are still the problems of EMI and excess motor heating to deal with. It is possible to generate EMI due to the current switching that occurs in the motor leads because they carry not only the primary frequency, but also many higher harmonics as well, so they require careful routing, shielding, or both. We can put in a low pass L-C filter to remove these high frequencies and still pass normal commutation currents without any significant loss of motor performance.

Design of the L-C Filter

Figure 2 is a block diagram of a motor connected to 2 UC3717s with the low-pass L-C filters in place.

Again we will use a current of 850 mA in each winding, an off-time of 30 μsec, and an on-time of 4.4 μsec but now we will use an

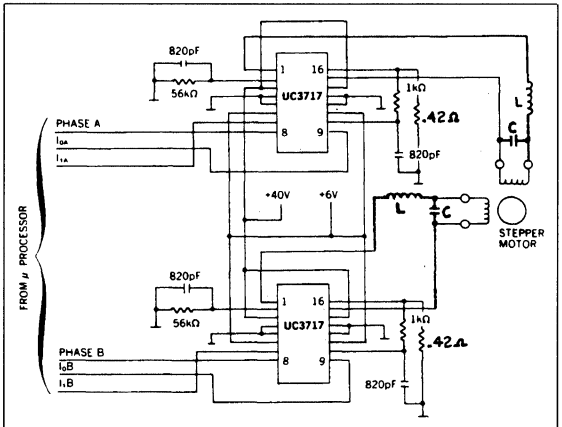


Figure 2. Low-pass L-C filters on outputs.

external inductance (L) to control the chopping. V_{drop} is the sum of the source (V_{so}) and sink (V_{si}) voltage drops at 850 mA:

$$V_{drop} = V_{so} + V_{si} + V_{sense} = (2.6 + 1.9 + 0.36)$$
$$= 4.9\ volts \quad (8)$$

In order to minimize the effects of L on the motor current risetime we will make it 10 times smaller than L_m or 500 μH. In order to keep the peak current in the UC3717 below 1 amp we will use a 0.42 ohm sense resistor and also limit $_{\Delta}I_L$ to 300 mA. Using a variation of equation (6) we can check that:

$$L = \frac{(V_s - V_{drop}) \times t_{on}}{{}_{\Delta}I_L} = \frac{(40 - 4.9) \times 4.4\times10^{-6}}{300\times10^{-3}} = 515\ \mu H \quad (9)$$

is in keeping with the constraints outlined above.

Similarly, we would like to find a value for the capacitor (C) such that it will have less than 1/10 the impedance of L at 29.1 kHz:

$$C = \frac{10}{(2 \times \pi \times f)^2 \times L} = \frac{10}{(2 \times 3.14 \times 29100)^2 \times 500\times10^{-6}} \quad (10)$$
$$= 0.6\ \mu F$$

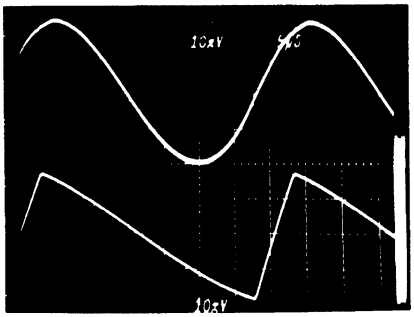
The test motor and driver, operated unloaded (nothing connected to the output shaft) and in the configuration of *Figure 2,* used values of 500 μH for the inductor and 0.47 μF for the capacitor. *Figure 1* and *Figures 3* through *6* are waveforms obtained from that motor.

The lower trace of *Figure 3 (Figure 3b)* shows the 330 mA current sawtooth in the inductor, while the upper trace *(Figure 3a)* shows an 8 mA p-p current ripple in the motor winding. While this may seem to indicate only a 12 dB reduction in EMI over *Figure 1,* comparing the *sinusoidal* waveform of *Figure 3a* to the "noisy" *sawtooth* waveform of *Figure 1* will quickly point out sources of

UC3717 and L-C Filter

EMI. In *Figure 1,* the oscillations immediately following each switch of the driver are due to the motor's distributed capacitance resonating with its inductance and are a possible source of EMI. In addition, sharp current spikes are allowed to pass along the motor leads and through the motor's distributed capacitance unhindered, thus creating high frequency EMI. EMI spikes were virtually eliminated from *Figure 3a* by using a low ESR capacitor and connecting the motor leads close to the body of the capacitor.

Figure 4 shows motor current superimposed over the inductor current. Just to the left of the center graticle line a ringing occurs in the inductor current that also appears in the motor current, although attenuated. This ringing occurs at a frequency of:



a) VERT = 2 mA / DIV A-C component of Motor Current with L-C filter.

b) VERT = 100 mA / DIV A-C component of inductor current with L-C filter.

HORIZ = 5 µS / DIV

Figure 3. Motor and inductor current waveforms.

$$f_{res} = 1 / 2\pi\sqrt{L \times C} = 1 / 6.28 \times \sqrt{500\times10^{-6} \times 0.47\times10^{-6}} = 10.4 \text{ kHz} \quad (11)$$

which is the resonant frequency of the L-C filter. This frequency can be lowered by increasing the value of either L or C, although at a cost of reducing the high speed performance of the motor.

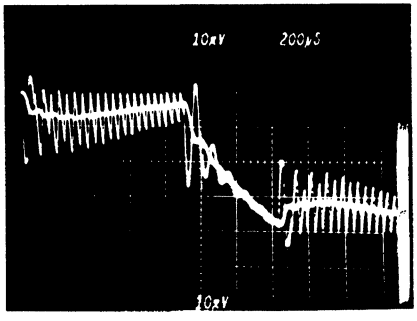
The high frequency sawtooth waveforms at the upper, flat portion of the motor current waveform are the 29.1 kHz chopping currents in the inductor. They cause a small corresponding ripple in the motor current but, because the chopping frequency is more than twice the break frequency of the 2-pole L-C filter, we would expect, and can see, an attenuation greater than 12 dB.

In a 2 phase step motor (sometimes referred to as a 4 phase step motor because of the 4 windings used in the unipolar version) the STEP RATE, in full steps per second (FSPS), is 4 times the primary frequency of the motor current waveform. The two phases of the step motor are operated in quadrature and thus will generate 4 distinct states in the 2 phases which correspond to 4 mechanical steps for each electrical cycle.

FSPS = 4 x frequency (for a 2 or "4" phase step motor) (12)

It is important to note at this time that 10.4 kHz is the highest frequency that can be passed to this motor without attenuation using the selected components, but that this corresponds to a step rate of 41,600 FSPS! The test motor was able to run at 17,000 full steps per second with the L-C filter in place, which is high enough for most situations.

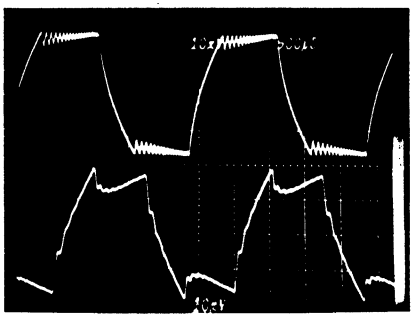
Figures 5 and *6* are current waveforms for the motor running at 1600 FSPS and 16,000 FSPS respectively. The motor was operated with the L-C filter on only the lower trace winding so that the waveforms could be compared easily. Looking at *Figure 5,* one can see that the leading edges of both waveforms have the same



VERT = 500 mA / DIV

HORIZ = 200 mS / DIV

Figure 4. Filter current waveform superimposed over motor current waveform.



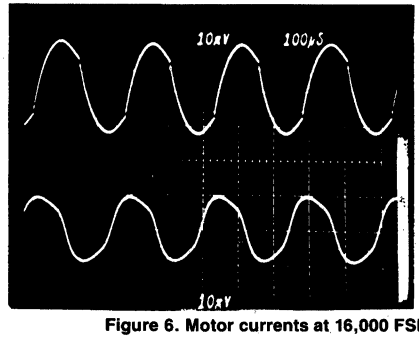
VERT = 500mA / DIV Motor current without L-C filter.

VERT = 500mA / DIV Motor current with L-C filter.

HORIZ = 500µS / DIV

Figure 5. Motor currents at 1600 FSPS.

risetimes, although the filtered one has more susceptibility toward ringing. From *Figure 6,* one can see that torque is down only 3 dB at 16,000 FSPS and that there are "glitches" in the unfiltered waveform that do not appear in the filtered waveforms.



VERT = 500mA / DIV Motor current without L-C filter.

VERT = 500 mA / DIV Motor current with L-C filter.

HORIZ = 100 mS / DIV

Figure 6. Motor currents at 16,000 FSPS.

Conclusions

The use of a low-pass filter can be an effective heat and EMI reduction mechanism when used with a step motor chopper driver such as the UC3717. The price one pays for a "clean" EMI environment is a *small* loss in very high speed performance. The technique may be applied equally well to non-IC chopper drivers but the peak currents must be accounted for and the minimum value of L adjusted accordingly. 500 µH is the smallest practical L that should be used with the UC3717 since we do not want the

UC3717 and L-C Filter

peak of the ripple to exceed 1.0 amps. This limits the usefulness of the technique to motors with inductances of 2 mH or more. At average currents less than 300 mA, the value of L may have to be larger in order to maintain continuous current in the inductor, but the physical size may be decreased. If an average current in excess of 850 mA is required, then a power amplifier may be added as shown in *Figure 7.* This will extend the peak current capabilities of the chopper drive to higher current and will also allow the value of L to be decreased.

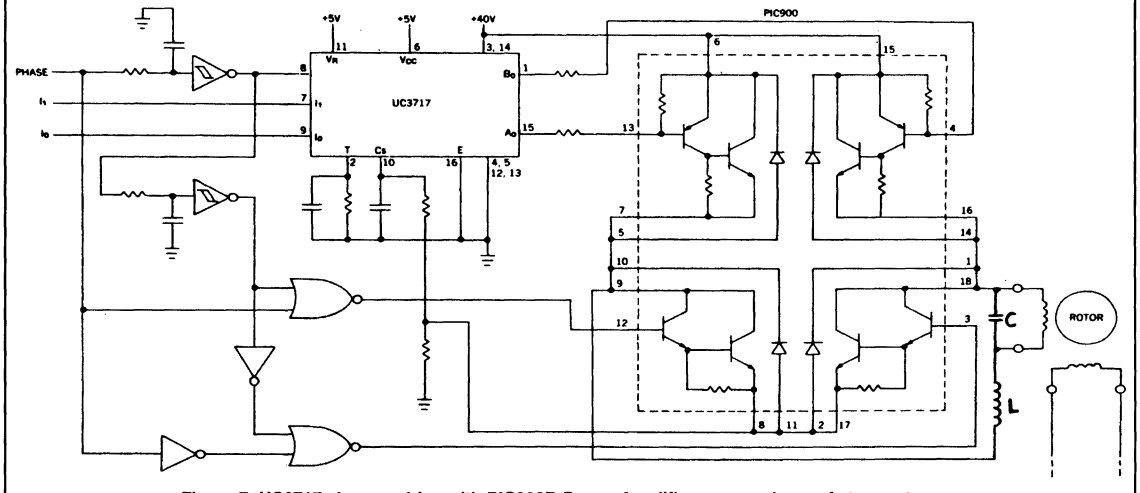


Figure 7. UC3717 chopper drive with PIC900B Power Amplifier on one phase of step motor.

UNITRODE
APPLICATION NOTE

UC1637/2637/3637
SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

INTRODUCTION

There is an increasing demand today for motor control circuits, as a result of the incredible proliferation of automated position control equipment, which is itself made possible by recent developments in the field of digital computation.

The UC1637 Switched Mode Controller for DC motors is one of several integrated circuits offered by Unitrode for motor controls. This Application Note presents the general principles of its operation and the circuit details that optimize its use. As an illustration we will carry out an actual design which will involve not only the UC1637, but also a power H-bridge using MOSFET transistors, and a modern DC motor tachometer. Using the tach output and UC1637's error amplifier, we will close the velocity control loop after a brief analysis of the factors that affect the feedback loop stability.

To achieve high efficiency power amplification, the UC1637 uses pulse width modulation, or PWM. This technique is employed today in many different circuits where power losses must be minimized, and is most suitable in applications involving inductive loads such as motors voice coils, etc.

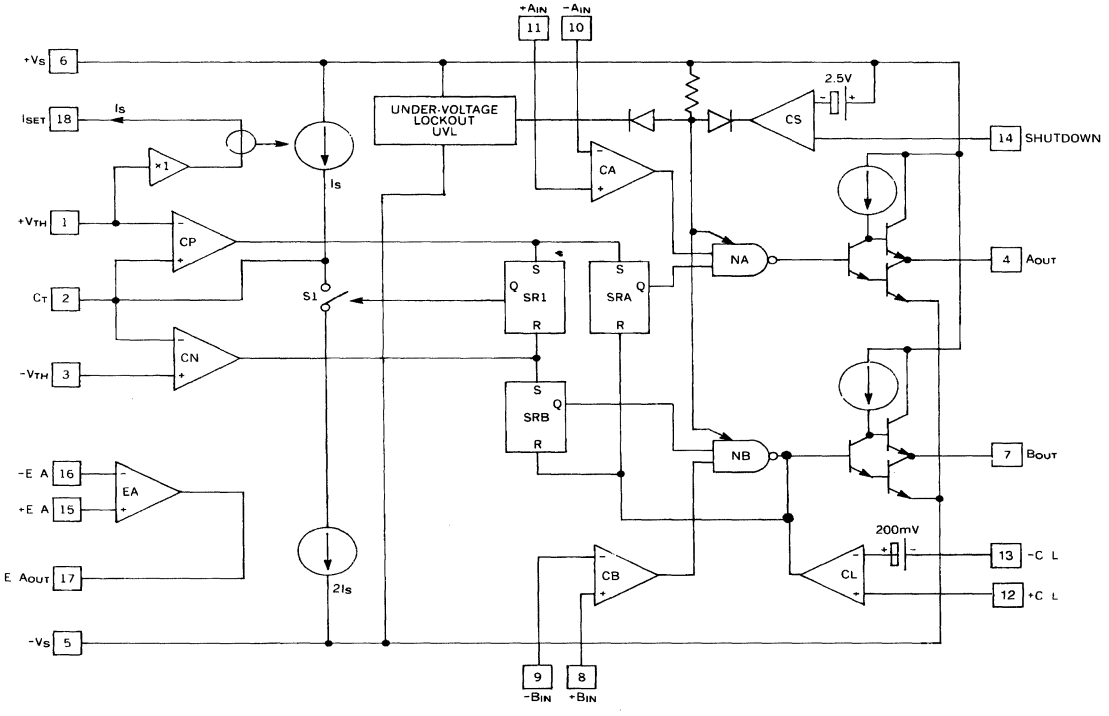


FIGURE 1. BLOCK DIAGRAM OF UC1637.

PULSE WIDTH MODULATION (PWM)

The function of a power amplifier is to regulate the flow of energy from a power supply to a load, under the control of an input signal. A linear amplifier does this by interposing a controlled voltage drop in series with the load, while carrying the full load current. The product of this voltage and current represents the amount of power that must be dissipated by the amplifier itself, and it is easy to see that the method is not very efficient. In fact, its usefulness diminishes rapidly as the amount of power to be controlled increases and, at some point, a more efficient method becomes imperative.

PWM is a switching technique in which the supply voltage is fully applied (switched) to the load and then removed, the "on" and "off" times being precisely controlled. The effect on the load is the same as if some lower voltage were continuously applied whose value depended on the duty-cycle, that is, the ratio of "on" time to the full switching period. Since supply current only flows during the "on" times, it is apparent that the efficiency should be much higher than in the linear amplifier, as in fact it is. Still, switching transistors have small but finite "on" voltages and transition times, all of which introduce losses, which limit practical PWM efficiencies to something between 75% and 90%.

THE UC1637

The diagram of Figure 1 shows in block form the internal organization of the device. The main functions are:

A) Triangular wave generator; CP, CN, S1, SR1
B) PWM comparators; CA, CB
C) Output control gates; NA, NB
D) Current limit; CL, SRA, SRB
E) Error amplifier; EA
F) Shutdown comparator: CS
G) Undervoltage lockout; UVL

The two output lines, A_{OUT} and B_{OUT}, are meant to drive the two legs of an H-bridge power amplifier, with the load driven in bipolar fashion. The A_{OUT} and B_{OUT} outputs themselves are rated at 500mA peak and 100mA continuous, which makes it easy to interface the device with most amplifiers.

In order to generate two PWM output signals, we first produce a triangular waveform, or linear ramp. This is done by charging a capacitor C_T (pin 2) with constant current I_S until the comparator CP, with a fixed threshold voltage of $+V_{TH}$, delivers a pulse to "set" the SR1 latch circuit. This forces Q high, which closes the switch S1 and adds a negative current $2\times I_S$, to the node of pin 2. As a result, a net current equal to I_S now flows out of C_T, discharging it linearly until the comparator CN resets SR1, and the cycle restarts. Thus, the voltage at pin 2 ramps continuously between $-V_{TH}$ and $+V_{TH}$ at a frequency that depends on these two threshold voltages, on C_T, and on Is.

The current I_S is programmed by means of a resistor connected to pin 18. The voltage at this pin is equal to $+V_{TH}$ and an internal current mirror forces the charging current I_S to be equal to the current flowing out of pin 18. If a resistor R_S is connected from pin 18 to $-V_S$ (pin 5) instead of to ground, the ramp frequency becomes independent of power supply voltage variations, since Is will then change together with V_{TH}.

As Figure 2 shows a triangular waveform can be compared with a reference voltage to generate a PWM signal. The UC1637 uses two separate comparators to generate the two output signals A_{OUT} and B_{OUT}. The way the signals are handled, and the results, are shown in Figure 3 where it can be seen that the difference between V_A and V_B is the cause of the time intervals during which both outputs are low.

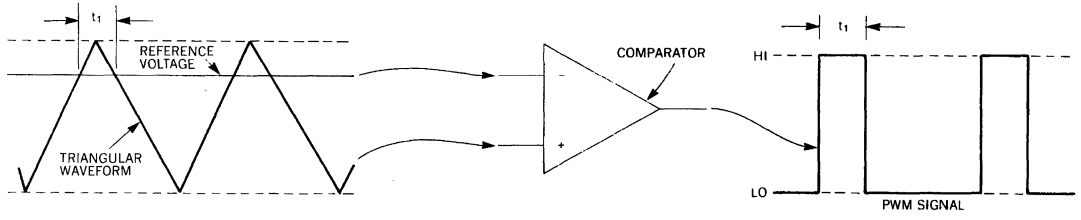


FIGURE 2. HOW A PWM SIGNAL IS GENERATED.

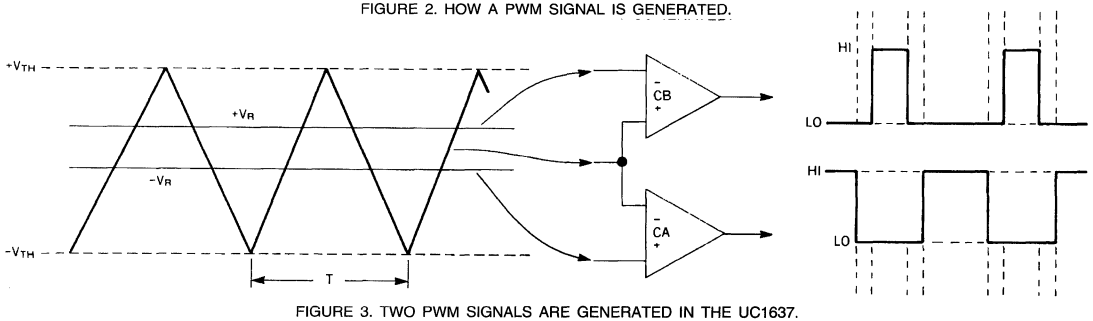


FIGURE 3. TWO PWM SIGNALS ARE GENERATED IN THE UC1637.

The two nand gates, NA and NB, will be enabled if the following two conditions are met:

A) supply voltage $+V_S$ is greater than +4.15 volts (typ)
B) the shut-down input line (pin 14) is at least 2.5 volts (typ) negative with respect to $+V_S$.

If these are satisfied, the A_{OUT} output line will be high if the CA output *and* Q of SRA are both high. Since SRA is set at each positive peak of the oscillator ramp, the output A_{OUT} can be controlled by CA singly — as long as a current-limit pulse from CL does not occur. The operation of the NB gate is similar.

The timing diagrams of Fig. 4 show the sequence of events before and after a current limit pulse occurs. Before time t_1 the PWM action is smoothly controlled by the ramp comparisons with V_A and V_B. The pulse from CL at time t_1 resets both SRA and SRB; the output lines are now disabled until SRA is set (at time t_2) and SRB is set (at time t_3).

The current limit comparator CL provides a means to protect both driver and motor from the consequences of very high currents. If the current delivered by the driver to the motor is made to flow through a low value resistor (for example, see R_S in Figure 7) the voltage drop across this resistor will be a measure of motor current. This voltage is applied between pins 12 and 13 of the UC1637, with pin 12 positive. A 200mV threshold is provided internally (see Figure 1) so that when the R_S voltage is equal to 200mV the output of CA goes high, resetting both SRA and SRB and, consequently, terminating any active output pulse. This pulse-by-pulse method of current limiting is very fast and provides effective protection, not only for the driver components, but also for the motor where the possibility of demagnetization due to excessive current is a matter of serious concern.

Finally, the UC1637 contains also an operational amplifier EA, that can be used to provide gain and phase compensation as will be seen later.

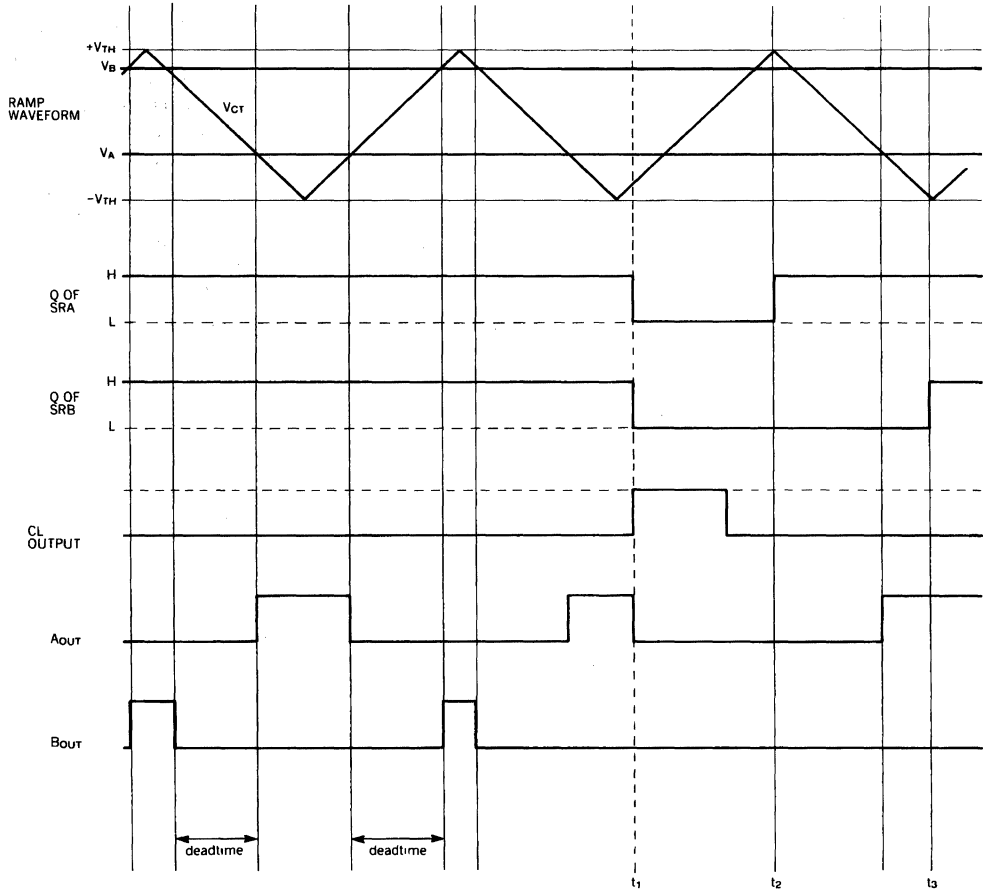


FIGURE 4. TIMING DIAGRAM SHOWING THE GENERATION OF PWM PULSES AT A_{OUT} AND B_{OUT}.
BEFORE TIME t_1, THE Q OUTPUTS OF SRA AND SRB ARE BOTH HIGH AND THE OUTPUT PULSES ARE CONTROLLED BY THE RAMP INTERSECTIONS WITH V_A AND V_B. AT TIME t_1, THE CURRENT LIMIT COMPARATOR HAS SENSED EXCESS CURRENT AND THE CL OUTPUT HAS GONE HIGH, RESETTING BOTH SRA AND SRB. THIS TERMINATES THE A_{OUT} PULSE THAT WAS ACTIVE AT THE TIME. A_{OUT} CAN RESUME ONLY AFTER SRA IS SET AT t_2; B_{OUT} CAN RESUME ONLY AFTER SRB IS SET AT t_3.

Figure 5 shows the connections needed to get the ramp generator and the two comparators ready to go. There is no great difficulty in calculating values for the various resistors, which are no more than two simple voltage dividers. Still, certain things should be considered before proceeding.

The input impedance R_{IN}, seen by the control voltage V_C will be

$$R_{IN} = \frac{R_3 + R_4}{2} \quad (1)$$

and this value may be specified or determined in advance. Also, it would be economical to have a minimum number of different values of resistors. If we make

$$R_1 = R_3 \quad (2)$$

we will have four resistors of equal value in the final circuit.

There is also the question of deciding on the separation V_G between the reference voltages $+V_R$ and $-V_R$. The voltage gain of the PWM amplifier will have one of the four characteristics depicted in Figure 6, depending on your choice of reference voltage separation. You can get a linear response by making $V_G = 0$, as in Curve #1, or by making $V_B - V_A = 2V_{TH}$, as in Curve #3. In Curve #2, there is a change in slope due to the contribution, near zero, of both V_A and V_B to the output changes, which in some systems may be undesirable, but which may be of interest due to the fact that it results in zero losses at null.

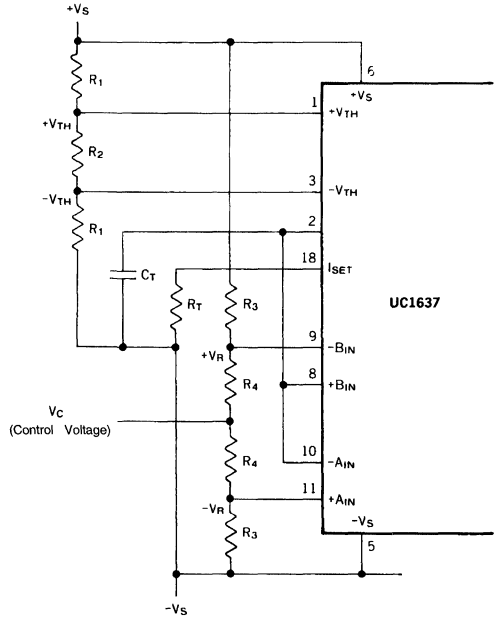


FIGURE 5. SETTING UP THE A AND B COMPARATOR INPUTS.

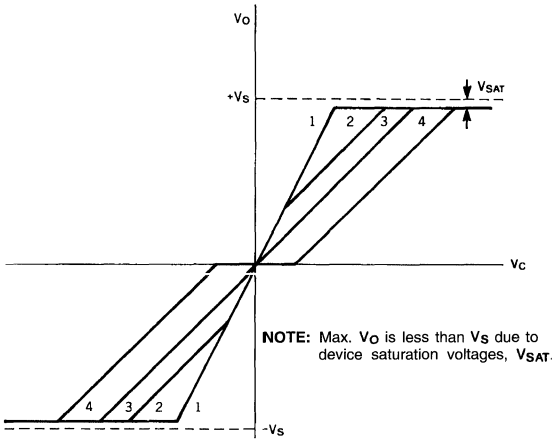


FIGURE 6. PWM VOLTAGE GAIN CHARACTERISTICS OBTAINABLE WITH VARIOUS VALUES OF REFERENCE VOLTAGE SEPARATION, OR GAP VOLTAGE 2 V_R.
1. LINEAR GAIN WITH $V_R = 0$ (a = 0).
2. NON-LINEAR GAIN WITH V_R GREATER THAN ZERO BUT LESS THAN V_{TH} ($0 < a < 1$).
3. LINEAR GAIN WITH $V_R = V_{TH}$ (a = 1).
4. NON-LINEAR GAIN WITH V_R GREATER THAN V_{TH} ($a > 1$).
NOTE: THE SLOPE OF LINE 1 IS TWICE THAT OF LINE 3.

At this point, this choice of PWM gain characteristic amounts only to the choice of the ratio between V_R and V_{TH}:

$$a = \frac{V_R}{V_{TH}} \quad (3)$$

The values of V_{TH} and V_R, as well as R_3 and R_4, depend on the following:

$\pm V_S$: power supply voltages
R_{IN}: desired control input resistance
$V_C$max: peak value or input voltage V_C. This is the input voltage at which the output reaches 100% duty cycle
a: ratio of V_R to V_{TH}

These values being known the designer can proceed to calculate the following circuit values:

$$R_3 = \frac{2\,R_{IN}\,V_S\left(1 + \frac{1}{a}\right)}{V_C\text{max} + V_S\left(1 + \frac{1}{a}\right)} \quad (4)$$

$$R_4 = 2\,R_{IN} - R_3 \quad (5)$$

$$V_A = \frac{V_S R_4}{2 R_{IN}} \quad (6)$$

$$V_{TH} = \frac{V_R}{a} \quad (7)$$

$$R_2 = 2 R_3 \frac{V_{TH}}{V_S - V_{TH}} \quad (8)$$

and, from Eq. (2), $R_1 = R_3$.

Having chosen a frequency f_T for the PWM timing circuit, you can now calculate C_T and R_T. A suitable starting value for the charging current I_S is 0.5mA which gives

$$R_T = \frac{V_S + V_{TH}}{.0005} \quad (9)$$

$$C_T = \frac{.0005}{4 f_T V_{TH}} \quad (10)$$

You will probably need to make an adjustment here, so as to get a standard value for capacitor C_T, and it is best to keep I_S in the range from 0.3mA to 0.5mA when you do this. It may be desirable, or even necessary in some conditions, to bypass the $+V_{TH}$ and $-V_{TH}$ inputs to ground, and for this, ceramic capacitors of 0.1μf should be adequate. Remember also that terminal 14, the shut-down line, must be held "low" (at least 2.5V below the positive rail) in order to enable the drive. With an external switch to ground, or to $-V_S$, and a pull-up resistor to $+V_S$, this line can be used to enable (low), and disable (high), the output. Both A_{OUT} and B_{OUT} will be low when the shut-down line is high.

The next step is to connect the UC1637 to a suitable power amplifier, and the amplifier to the motor. The UC1637 has provisions for current limiting, as discussed earlier, and you must make arrangements to develop a voltage proportional to motor current at the driver side. This can be done by adding to an H-bridge a low value resistor in series with rail connections. The current limit comparator has a common mode range that reaches all the way down to the negative rail (on the positive side the limit is 3V below the positive rail). A resistor R_S is then added at the bottom of the bridge, and its value is selected so as to give a voltage drop to 200mV when the desired limit current flows.

$$R_S = \frac{.2}{I_{MAX}} \text{ (ohms)} \quad (11)$$

where I_{MAX} is the maximum desired motor current in amperes. In a breadboard, a twisted pair of wires should be used to make the connection from this resistor to pins 12 and 13, and an RC filter should be added, as shown in Figure 7.

On a PC board, it is a good idea to keep R_S close to the UC1637 to minimize the length of the connecting traces. The RC filter should still be used.

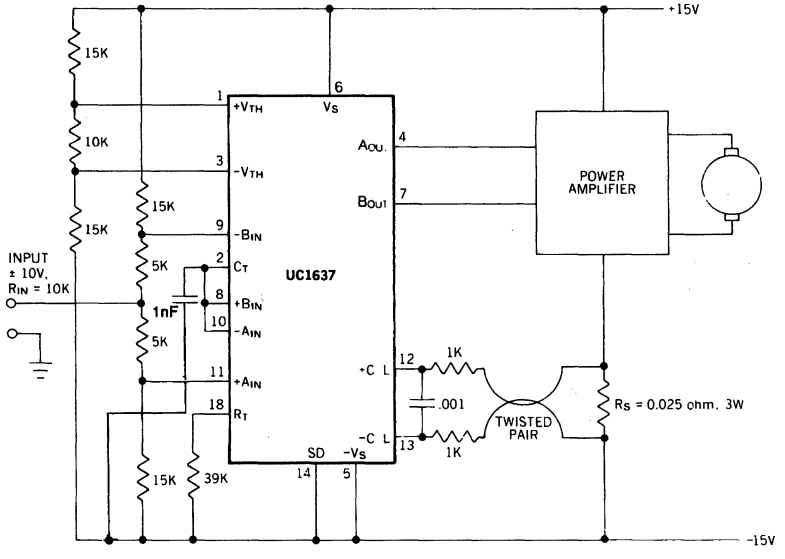


FIGURE 7. CIRCUIT DIAGRAM OF PWM VOLTAGE AMPLIFIER WITH GAIN OF 3.

AN EXAMPLE

We are ready now to design a current limited, PWM voltage amplifier to drive a small DC servomotor. Here are the requirements:

Supply voltages: ±15V
Input: ±10V max.; 10K input res.
PWM frequency: 30KHz
Motor current limited at 8A
Minimum power losses at idle

We have:
$V_S = 15V$
$V_C max = 10V$
$R_{IN} = 10^4 ohm$
$f_T = 3 \times 10^4$ Hz
and $I_{MAX} = 8A$

and also, from the last requirement, a = 1.

FROM EQUATIONS

(4) $$R_3 = \frac{2 \times 10^4 \times 15 \times 2}{10 + 15 \times 2} = 15K$$

(5) $$R_4 = 2 \times 10^4 - 15 \times 10^3 = 5K$$

(6) $$V_R = \frac{15 \times 5 \times 10^3}{2 \times 10^4} = 3.75V$$

(7) $$V_{TH} = 3.75V$$

(8) $$R_2 = (2 \times 15 \times 10^3) \times \frac{3.75}{15 - 3.75} = 10K$$

(9) $$R_T = \frac{15 + 3.75}{.0005} = 37.5K$$

and of course, $R_1 = R_3 = 15K$.

(10) $$C_T = \frac{.0005}{4 \times 30 \times 10^3 \times 3.75} = 1.11 \times 10^{-9} fd$$

If we settle for $R_T = 39K$, I_S becomes slightly less than 0.5mA and if we then pick $C_T = 1000pf$, the nominal frequency becomes 32KHz.

To limit the motor current at 8A, we need, from Eq. 11,

$$R_S = \frac{.2}{8} = 0.025 \text{ ohm}$$

The peak power in the resistor will be

$P_S = 8^2 \times .025 = 1.6$ watts.

Incidentally, the voltage gain of the amplifier can be determined from the fact that a 10V change at the input results in a 30V change at the output; therefore, the gain from input to motor terminals is 3. The above circuit is shown in Figure 7.

THE POWER AMPLIFIER

Where space is tight and motor current is less than five amperes, the Unitrode PIC900 offers a perfect solution to your power bridge design. This device comes in a DIL-18 package, requires only 5mA of input drive current, and is rated at 5A absolute maximum output current. It contains all you need for the output H-bridge - including the circulating diodes - and with only a few added parts, you are ready to go. A circuit diagram showing a velocity feedback loop using one UC1637 and one PIC900 appears in the UC1637 data sheet.

For higher currents, you will have to design your own amplifier, and for the purposes of this application note, a sample design is shown in Figure 8. Referring to that circuit, note that with $+V_S$ and $-V_S$ applied, if the inputs are left open, the power MOSFETs are all "off". If Drive A, for example, is driven to within 3.6V of either power rail, then the corresponding output is switched to that rail. Note that since the PNP and NPN junction transistors are by nature faster switching "on" than "off", while the MOSFETs are much faster than the junction transistors driving them, this connection provides a simple guarantee against cross-conduction. Also working toward this goal is the fact that the junction transistor can discharge the MOSFET's input capacitance faster than the 1K, 1W resistor can charge it. The arrangement shown in Figure 8 results in a transition time of about 1.5μS during which both MOSFETs in a given leg are off. This amount of time is a very small portion of the 33μS period toward which we are designing our example.

The power MOSFET transistors, in TO-220 package, are rated at 60V and 12A. The channel "on" resistance is quite low, 0.25 ohms at 8A, for the UFN533, resulting in low thermal losses. You can easily find other devices with even lower R_{DS} values, if needed, but as always, the price you pay is that you must pay the price.

Finally, a word about circulating diodes - conspicuous in Figure 8 by their absence. All power MOSFETs have an intrinsic rectifier, or body diode, a junction rectifier whose current rating is the same as that of the transistor. With the drive format provided by the UC1637, the two bottom MOSFETs (N-channel) are "on" during the time when motor current circulates, and as a result the reversed diode carries only a small portion of the current: most of it flows from source to drain through the channel. In fact, the diode fully conducts only during the 1.5μS when both devices in one bridge leg are off. You can add fast recovery diodes in shunt with the MOSFETs if you find that they are essential. The intrinsic MOSFET diode is not particularly fast, and as your output current requirements increase, the need for fast external diodes will become more and more apparent.

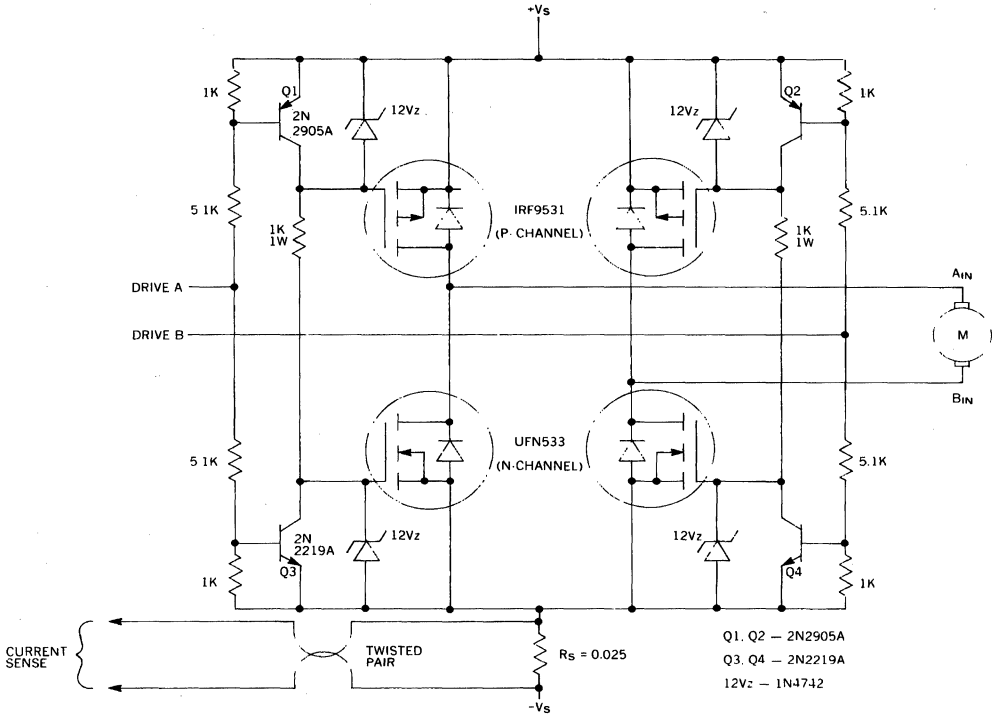


FIGURE 8. THIS 8A POWER AMPLIFIER IS SUITABLE FOR 30KHz OPERATION.

THE SERVOMOTOR

It is convenient to represent the DC servomotor by a simple equivalent circuit, and one such circuit is shown in Figure 9. Note that by expressing the moment of inertia J and the motor constant K in metric units (Nm sec^{2}and Nm/A respectively), we avoid the need to include a multiplying constant in the expressions for C_M and e_o. Also, the motor constant K, in metric units, defines both the voltage constant in volt-sec/rad, and the torque constant in Nm/A, as one and the same number.

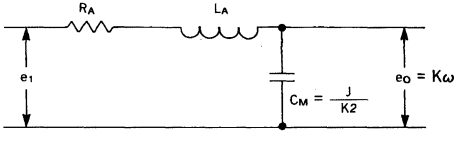


FIGURE 9. EQUIVALENT CIRCUIT OF MOTOR, WHERE J IS THE TOTAL MOMENT OF INERTIA OF ROTOR PLUS LOAD.

R_A = armature resistance; ohms.
L_A = armature inductance; henrys.
C_M = equivalent capacitance; farads.
J = total moment of inertia: Nm sec^2.
K = motor constant; volt sec/rad, or Nm/A.
ω = rotor angular velocity: rad/sec.

TO CONVERT FROM	TO	MULTIPLY BY
oz in sec^2	Nm sec^2	7.06×10^{-3}
volts/KRPM	volt sec/rad	9.55×10^{-3}

The ratio J/K^2 has the dimensions of capacitance, with a value runnng to several thousand microfarads. The voltage across this capacitor is equal to $K\omega$ where ω is the angular velocity of the rotor in rad/sec. Consequently, this voltage is the analog of shaft velocity.

Our equivalent circuit, then, is a simple series connection of R_A, the armature resistance; L_A, the armature inductance; and C_M, the equivalent capacitance, equal to J/K^2. It should come as no surprise that such a circuit will have a natural resonant frequency ω_N, and a resonant Q as well. This is indeed the case, and we have for its transfer function,

$$\frac{e_{o(s)}}{e_{1(s)}} = \frac{1}{(s/\omega_N)^2 + s/Q\omega_N + 1} \quad (12)$$

where $$\omega_N = \frac{K}{\sqrt{L_A J}} \quad (13)$$

and $$Q = \frac{K}{R_A}\sqrt{\frac{L_A}{J}} \quad (14)$$

We can now use these sample results in our sample design. Here are some of the data given by a motor manufacturer:

EG & G TORQUE SYSTEMS
MODEL NO. MT-2605-102CE
(motor - tach assembly)

MOTOR: K_T = 4.7 oz in/amp
K_V = 3.5V/KRPM
R_A = 0.7 ohms
J_M = 0.0018 oz in sec^2
T_M = 8.6 ms (mech. time const.)
T_e = 1.6 ms (el. time const.)
TACH: J_T = 0.001 oz in sec^2
K_V = 3V/KRPM

The several motors in this series and size have the same electrical time constant T_E, and since we know R_A,

$L_A = T_E R_A = 0.016 \times 0.7$
L_A = 1.12 mH

The total moment of inertia is

$J = J_M + J_T = 0.0018 + 0.001$
J = 0.0028 oz in sec^2

In metric units,

$$J = \frac{0.0028}{141.612} \text{ (Nm sec}^2\text{)}$$

Putting K_T in metric units,

$$K = \frac{4.7}{141.612} \text{ (Nm/amp)}$$

The equivalent capacitance is

$$C_M = \frac{J}{K^2} = \frac{141.612 \times 0.0028}{(4.7)^2} = 18{,}000\mu f$$

For the equivalent circuit, then, the values are

R_A = 0.7 ohms
L_A = 1.12 mH
C_M = 18,000μf

The angular velocity will be proportional to the voltage e_o across C_M;

$$\omega = \frac{e_o}{K}$$

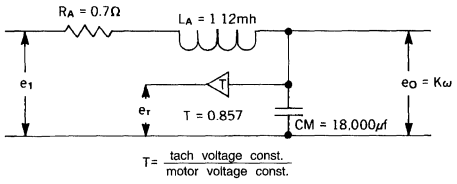


FIGURE 10. THE TACH VOLTAGE e_T IS PROPORTIONAL TO ω.

If the motor has a tachometer attached, we can include it in the equivalent circuit by deriving an equivalent tach voltage proportional to e_o. This is illustrated in Figure 10, where

$$T = \frac{\text{Tach. voltage constant}}{\text{Motor voltage constant}}$$

$$T = \frac{3\text{V/KRPM}}{3.5\text{V/KRPM}} = .857$$

From Eq. 13, ω_N = 222.7 rad/sec

From Eq. 14, Q = 0.356

(Note: Since $\zeta = \frac{1}{2Q}$, the damping factor here is 1.4)

From Eq. 12 and the above data, we can write the ratio of tach voltage to input as

$$\frac{e_T(s)}{e_1(s)} = \frac{.857}{\left(\frac{s}{222.7}\right)^2 + \frac{s}{79.3} + 1} \qquad (15)$$

THE VELOCITY LOOP

Our objective is to put together a feedback loop using our UC1637, H-bridge, and motor: the controlled variable is ω, the motor shaft's angular velocity. For high accuracy, we need a high loop gain, so that small velocity errors are magnified and corrected. The UC1637 internal ERROR amplifier is appropriate for this purpose, and will be used as a summing amplifier. But before proceeding, let us take a look at Figure 11, where a plot of the motor-tach transfer function (Eq. 17) is shown. The plot shows that as the frequency increases, the tach output decreases and the phase lag increases towards a maximum of 180°. This means that although we can introduce plenty of gain at very low frequencies, where the phase lag is low, the added gain must be reduced at the higher frequencies, where the 180° phase lag tends to make our loop a regenerative one. If we want the closed loop response to be "snappy", that is, if we want a bandwidth of several tens of hertz, then the loop gain must be

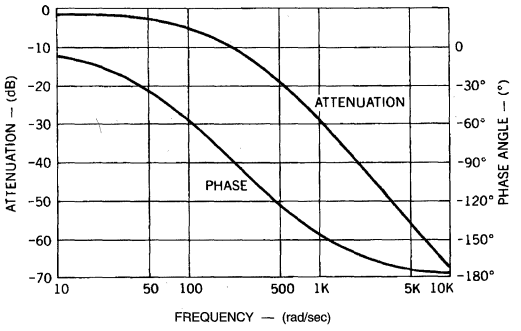
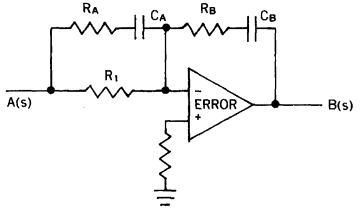


FIGURE 11. PLOT OF MAGNITUDE AND ANGLE OF EQ. 15. WHICH DESCRIBES PERFORMANCE OF OUR TEST MOTOR.

fairly high at all frequencies in the band; yet, for flat response and fast step response with no overshoot we must make certain that the overall phase shift is less than 180° at any frequency at which the gain is greater than unity.



$$\frac{A(s)}{B(s)} = \frac{(1 + sR_BC_B)\,[1 + s(R_1 + R_A)\,C_A]}{sR_1C_B\,(1 + sR_AC_A)}$$

FIGURE 12. ERROR AMPLIFIER WITH ITS FREQUENCY COMPENSATION NETWORK.
THE MAGNITUDE AND ARGUMENT OF THE TRANSFER FUNCTION CAN BE EASILY PLOTTED WITH THE AID OF A PROGRAMMABLE CALCULATOR.

The high gain ERROR amplifier of the UC1637, together with a few external components, is shown in Figure 12. Without R_A and C_A, the phase response of the circuit would go from -90° at low frequencies to 0° at high frequencies. This amount of phase correction is inadequate if we want a tight loop with good transient response. With R_A and C_A shunting R_1, it becomes possible to have a leading phase angle

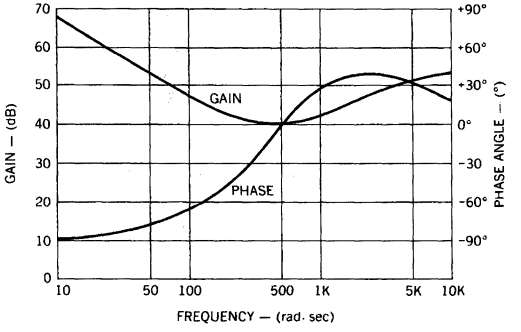


FIGURE 13. MAGNITUDE AND ANGLE OF COMPENSATION AMPLIFIER OF FIGURE 12.

somewhere at midrange, even though the high frequency asymptote is still at zero degrees (R_A and C_A introduce both a zero and a pole). The transfer function of the circuit shown in Figure 12 is plotted in Figure 13 for the following component values

$R_1 = 9.1\,K$
$R_A = 1K$
$C_A = .22\mu f$
$R_B = 470K$
$C_B = .0047\mu f$

The break frequencies are:

$$\frac{1}{R_BC_B} = \frac{1}{(R_1 + R_A)\,C_A} = 450 \text{ rad/sec}$$

$$\frac{1}{R_1C_B} = 23{,}400 \text{ rad/sec}$$

$$\frac{1}{R_AC_A} = 4{,}500 \text{ rad/sec}$$

The plot shown in Figure 14 shows the result of cascading the compensation amplifier, PWM amplifier, and motor-tach. All gain contributions have been simply added together, and all phase contributions have also been added. The result, shown in Figure 14, shows the open loop frequency response of the complete velocity control system.

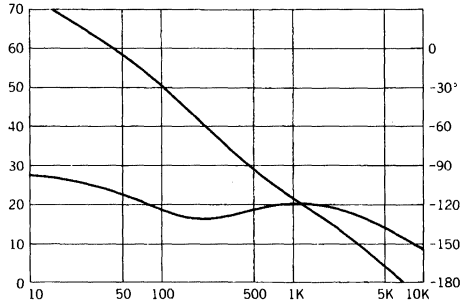


FIGURE 14. OVERALL OPEN-LOOP RESPONSE, INCLUDING +8dB DUE TO PWM AMPLIFIER GAIN AND MOTOR-TACH DC GAIN.

The inclusion of the ERROR amplifier with its compensation components has had the effect of introducing a large amount of gain at the lower frequencies, and also of reducing the phase lag at the higher frequencies. The loop gain is 0dB at about 7KHz, and the phase margin is about 40°.

Moreover, since the phase never exceeds 180°, we have the needed indication of relative stability, and can proceed to close the loop as shown in Figure 15 and make measurements. Note that a noise filter has neen added at the output of the tachometer. Such a filter is usually necessary, especially in PWM control loops of relatively wide bandwidth, because of the inevitable AC coupling between the motor signal and the tach output. In our filter, the 3dB cut-off point is at 21 KHz, which is high enough not to affect the loop behavior.

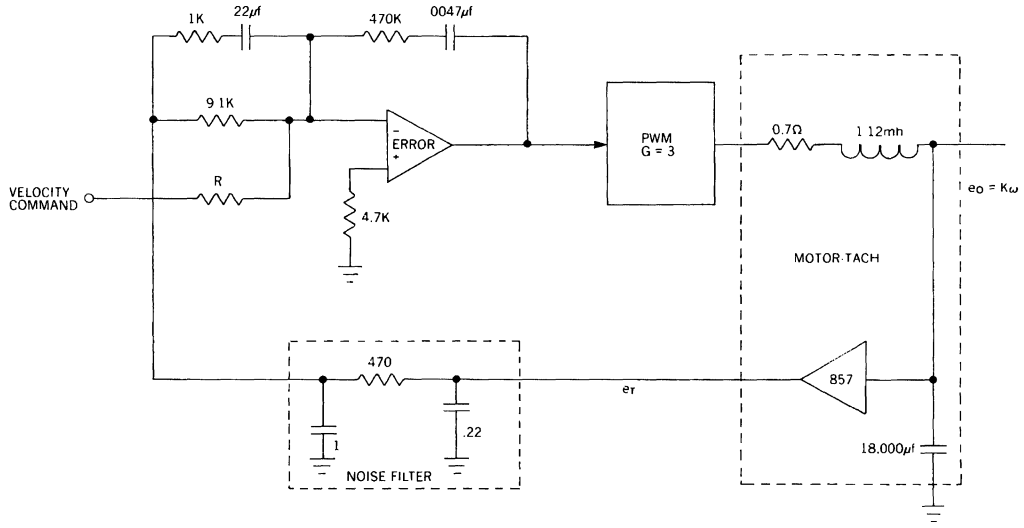
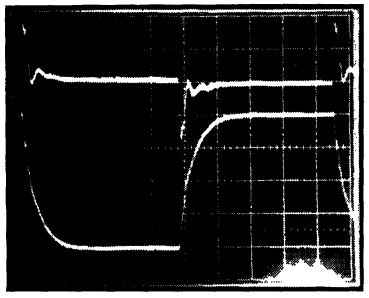


FIGURE 15. THE COMPLETE VELOCITY LOOP.

The oscilloscope trace shown in Figure 16 reveals that the step response of our loop is very well behaved. The motor shaft reaches full speed in less than 10mS, and there is no noticeable overshoot. The net velocity change in Figure 16 amounts to 133 RPM, and the current trace shows that the current does not quite reach the chosen limit of 8A. With larger input steps, the motor accelerates at constant 8A current, and the acceleration rate is approximately 100RPM per millisecond. The 3dB bandwidth of the loop measured about 80Hz.



Top trace: 5A/cm
Bottom trace: 100mV/cm
Horizontal: 5msec/cm

FIGURE 16. STEP RESPONSE OF THE VELOCITY CONTROL LOOP OF FIGURE 15. THE UPPER TRACE SHOWS THE MOTOR CURRENT: THE LOWER TRACE SHOWS THE TACH OUTPUT VOLTAGE, I.E., MOTOR VELOCITY.

CONCLUSIONS

We have discussed in some detail the characteristics of Unitrode's UC1637 and have presented in detail a design approach which illustrates those points. The sample design was built and tested, with the measured results as presented above. These results show that excellent performance can be obtained with few components, and that the design technique is quite simple. Our velocity loop would perform well as an inner loop in a position control system, for example, although a different response might perhaps be desirable. However that may be, using the UC1637 a sizable portion to the job is completed beforehand.

See Figure 17.

ACKNOWLEDGMENTS

We are grateful to EG & G Torque Systems for providing the motor-tachometer used in the sample design.

The Electra-Craft Corporation generously supplied a copy of their engineering handbook on DC Motors, 5th Edition. This book is highly recommended.

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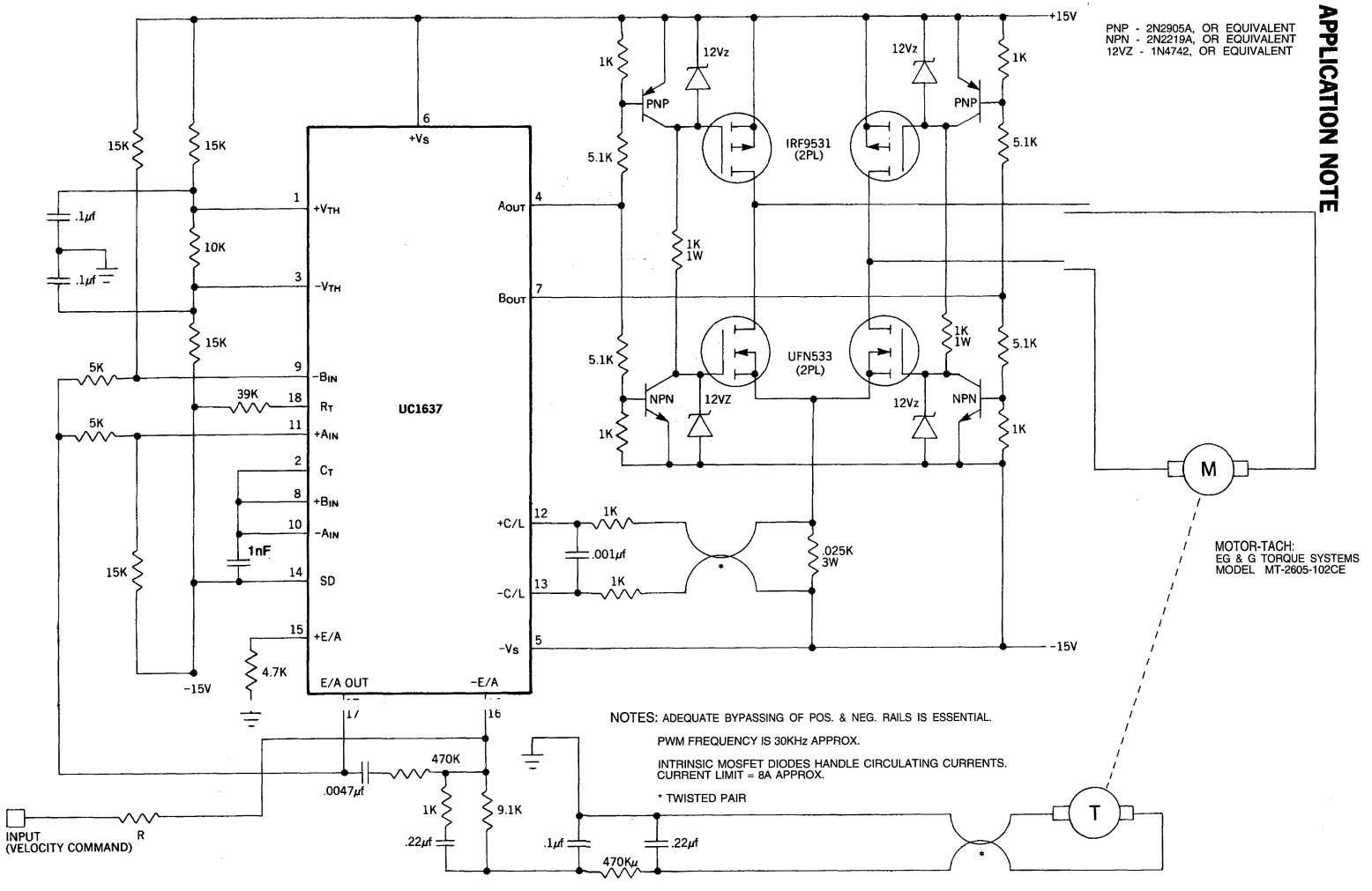


FIGURE 17. COMPLETE VELOCITY CONTROL LOOP OF SAMPLE DESIGN.

UNITRODE
APPLICATION NOTE

A HIGH PRECISION PWM TRANSCONDUCTANCE AMPLIFIER FOR MICROSTEPPING USING UNITRODE'S UC3637

INTRODUCTION

If you ask a designer why he has chosen a stepping motor for a given application, chances are that his answer will include something about "open loop positioning." Stepping motors can provide accurate positioning without expensive position sensors and feedback loops, and this fact alone results in large savings.

But there is more: steppers are tough and durable, easy to use, and high in power rate. And if you want to close a feedback loop around them, you can do that, too.

Still, there are certain problems. Steppers are *incremental motion* machines, and as such they tend to be noisy and are prone to behave erratically under certain conditions; for example, when the stepping rate is such as to excite a mechanical or electro-mechanical resonant mode. Furthermore, although the angular increments may be small–especially when half-stepping is used-the positioning resolution is restricted to a finite number of discrete points.

Therefore, this question arises: "Is there a method of driving stepping motors such that the resulting movement is smooth and quiet-that is, essentially continuous, as opposed to incremental? And would this result in improved positioning resolution?" We will try to answer these questions here.

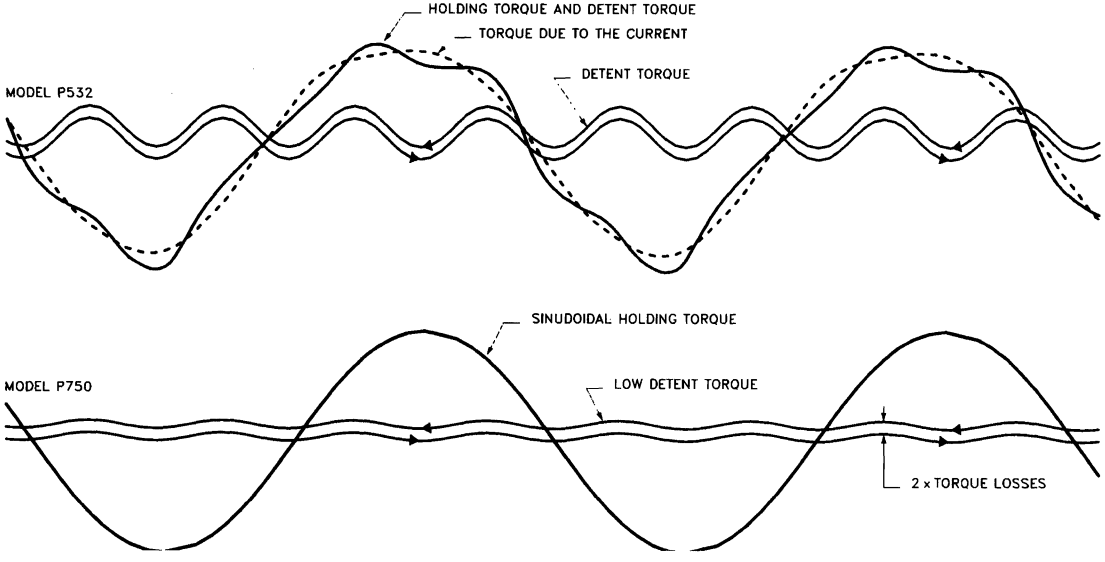


Figure 1. Static Torque Curves of Two Hybird Steppers

STATIC TORQUE CURVES

The curves in Figure 1 illustrate how a stepping motor torque behaves as a function of rotor angle. The detent torque component is a consequence of the magnetic field produced by the rotor magnet (or magnets), and is present with or without phase currents applied. It can be seen that this component contributes a fourth harmonic distortion to the static torque curves. The energized torque curves, in general, have additional harmonic components, mostly the third and fifth. Note that the two motors depicted in Figure 1 have very different characteristics in this respect. The distortion observed in the static torque characteristic is of no great consequence in the more usual applications of stepping motors, using either full step or half step sequences. It is when we start thinking about increasing the positioning resolution of these motors by some method of apportioning currents between the two phases, that we begin to be concerned about the effects of harmonic distortion. Even small amounts of added har-

monics can have a very noticeable effect on the waveshape, as shown in Figure 2.

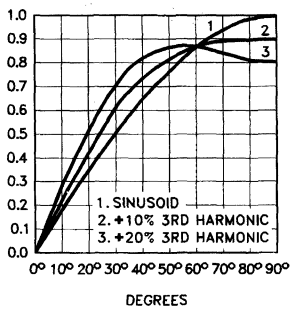


Figure 2. Effect of 10% and 20% Harmonic Content

Figure 3 shows the relationship between sine and cosine waveforms, and what it tells us is that if we can get a motor with a sinusoidal static torque characteristic-i.e., with no harmonic components-and drive phase A with a sine current function and phase B with a cosine current function, we would have smooth shaft rotation and accurate positioning at any angle.

Stepping motors having static torque curves with very low harmonic distortion are commercially available today. But most low-priced, mass produced hybrid steppers exhibit torque curves with enough harmonic components to require careful consideration in any attempt to improve resolution by what is known as *microstepping*. (The name *microstepping* originates from the fact that the required current waveforms are generated by a digital process that aproximates those waveforms incrementally. With thirty-two or sixty-four increments for an electical angle of $\pi/2$ radians, the resulting waveforms are hardly distinguishable from true sine or cosine signals.)

If the nonsinusoidal static characteristic of a given motor is known, it is possible to generate appropriate waveshapes for the phase currents so that the resulting torque curve becomes free of distortion, as required. Note that this involves no additional complexities, since it is just as easy-or difficult-to synthesize one waveform as another. Consequently, one can, in principle, linearize any motor for increased resolution and smoothness through microstepping.

Still, it should be noted that the best efficiency is obtained when the phase current waveshapes are undistorted, because of all suitable waveforms, the sine wave has the lowest form-factor.

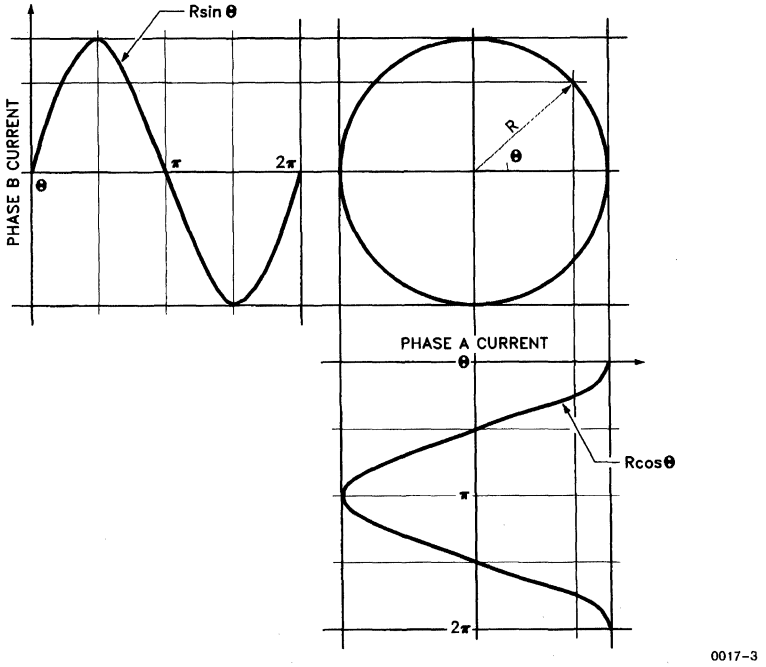


Figure 3. The sum of sine and cosine waveforms is a smoothly rotating vector.

The form-factor of a waveform is the ratio if its rms to average values. For a sine wave, this ratio is:

$$(1)\ ff_S = \frac{0.707}{0.637} = 1.111$$

Some manufacturers have used triangular waveforms–largely because they can be implemented with great simplicity-and it is interesting to note that for such a waveform, the average value is 0.5 V_{PK}, while the rms is 0.577 V_{PK}. Thus the form factor is:

$$(2)\ ff_T = \frac{0.577}{0.5} = 1.155$$

As a consequence, for the same peak power applied to the motor, the rms power of a triangular waveform is 18% less than that of a sine wave, whereas the average current is 21% less. It follows that microstepping with a triangular waveform does not use the full capabilities of the motor.

The same result is obtained with other-waveforms, as long as the peak power is limited, as it must be.

But regardless of all this, the fact remains that whether our motor has a sinusoidal torque curve or a very distorted one, the thing that will be inevitably required will be two amplifiers capable of converting the synthesized waveform into phase currents *at the required power levels.* In the next section, we will describe the design of one such amplifier, having a transconductance linearity of better than 1% and capable of delivering phase currents of up to ±6A.

UNITRODE'S UC3637 PWM CONTROLLER

Pulse width modulation (PWM) is a method of power control whose most attractive feature is the high level of efficiency that can be obtained. With careful design, and using power MOSFETs as output switches, one can easily achieve efficiencies higher than 80%.

The Unitrode UC3637 PWM controller, housed in an eighteen-pin DIL package, was originally intended to serve as a PWM amplifier for brush-type PM servomotors. But, because of its ingenious design, the device has found its way into various other uses as well, such as temperature control, uninterruptible power supplies, and even high fidelity sound reproduction. As we shall see, it can also be used in a high performance PWM transconductance amplifier.

BLOCK DIAGRAM AND LOOP EQUATIONS

A block diagram of the current feedback loop under consideration is shown in Figure 4, where the UC3637 is seen to contain the high-gain error amplifier and the main ingredients of the PWM amplifier. Since we are looking for an output of 6A, an H-bridge power stage must be added. The motor current I_M is sensed by means of a low value resistor R_S, and the derived voltage V_C is used to complete the feedback loop. Not shown in the block diagram is the back-EMF voltage, the product of motor shaft speed and K_V, the motor speed constant. Since this term does not contribute to the dynamics of the current feedback loop, it has purposely been left out.

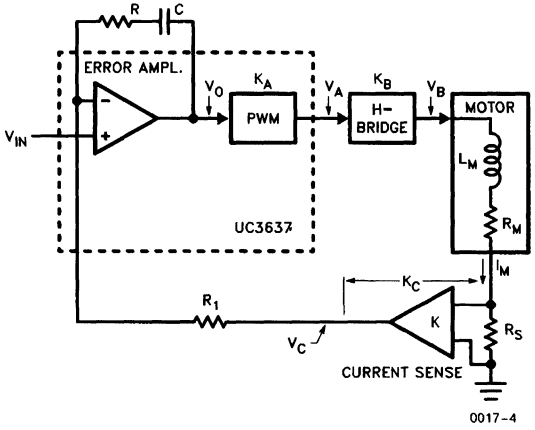


Figure 4. Block Diagram of the Complete Current-Control Loop

The transfer functions of the error amplifier and motor are as follows:

$$(3)\ \frac{V_O}{V_C} = -\frac{1 + sRC}{sR_1C}$$

$$(4)\ \frac{I_M}{V_B} = \frac{1}{R_M(1 + sTm)}$$

where TM = L_M / R_M, the motor's electronic time-constant (R_S is assumed to be low when compared with R_M). The forward transfer function is, then:

$$5)\ G(s) = \frac{-K_A K_B (1 + sRC)}{sR_1R_MC (1 + sTm)}$$

For the feedback transfer functions, we have simply:

$$(6)\ H(s) = \frac{V_C}{I_M} = K_C$$

Thus, for the closed loop,

$$(7)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B (1 + sRC)}{K_A K_B K_C (1 + sRC) + sR_1R_MC (1 + sTm)}$$

If we make the time-constant RC equal to the motor's time-constant T_M, this becomes:

$$(8)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B}{K_A K_B K_C + sR_1 R_M C}$$

$$(9)\ \frac{I_M}{V_{IN}} = \frac{1}{K_C(1 + sT_1)}$$

where,

$$(10)\ T_1 = \frac{R_1 R_M C}{K_A K_B K_C} = \frac{R_1 L_M}{K_A K_B K_C R}$$

By making RC = T_M, we have eliminated one of the transfer function poles. The resulting closed-loop response, described by (7) has a gain of 1 / Kc from $\omega = 0$ to $\omega = 1 / TI$, and drops at – 6 bd/octave thereafter.

DESIGNING THE HARDWARE

In designing circuits intended to handle power, it is customary to start with the output stage. This is surely due to the fact that the power stage is more demanding of the designer's attention and care, whereas the low level circuits are far more adaptable to the requirements of the chosen output configuration.

In the present case, power MOSFETs were chosen for the H-bridge because of their low losses, and because of their compatibility with the UC3637 outputs. Each totem-pole leg of the bridge is made up of one N-channel and one P-channel device. Such a pair can be driven in many different ways, of which several were considered for this particular design. The method that was finally chosen, shown in Figure 5, requires a few comments.

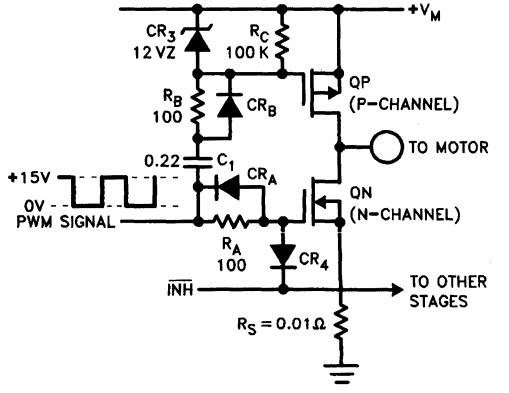


Figure 5. Totem-Pole Leg of Output H-Bridge

The first thing to notice is that the upper MOSFET, transistor QP, has its gate driven through a capacitor, C_1. This is not always practical of course, but in the case of a chopper drive combined with a stepping motor, it turns out that a driving signal is always present. At stand-still and at low speeds, it is the chopping rate that appears; at higher speeds, it is the stepping rate itself, or both. The driver is never required to deliver continuous DC (unchopped) to the motor winding, as it would to the armature of a brush-type DC motor at full speed. Consequently, QP never needs to be held in the ON state for more than a few microseconds, and for this the time constant of C1 R4 is adequate. Also, resistor R_A in parallel with CR_1, together with the gate capacitance of QN, cause this transistor to turn off faster than it turns ON. Since the same thing is done for QP, the problem of cross-conduction is neatly taken care of. The Zener diode CR3 serves as a clamp for the QP gate voltage. Finally, an inhibiting line, INH, is provided as a protection for QP and QN during the power turn-on time, when the + V_M voltage is rising and Cl must be charged. An auxiliary circuit senses a positive dV_M/dt and holds the INH line low, thus keeping QN OFF during this time.

An important point in favor of this arrangement is that the gate-drive circuit losses are independent of V_M and so this voltage can be set anywhere within the Vds rating of the power MOSFETs.

We can now consider the H-bridge with its motor winding load, as shown in Figure 6. The bridge is shown schematically with its driving circuits, but the action is still as shown in Figure 5. For example, when VIN is high, switch S1 is OFF and S3 is ON, and so forth. Furthermore, the opposite side of the bridge is driven by the complementary signal V_{IN}. With V_{IN} low, S1 and S4 will be conducting, and the load current I_M will increase in the positive direction (indicated by the + I_M arrow). Similarly, when V_{IN} is high, both S2 and S3 conduct, causing I_M to increase in the negative direction. Remember that the load is inductive, and that inductance is an energy storing element. Therefore, if we have some positive I_M, due to S1 and S4 being closed, and we switch to S2 and S3 closed, the previous value of I_M will continue to flow "uphill," so to speak, while decreasing. At the time of switching, this current ceases to flow down through sense resistor R_{S4} to ground and starts flowing up through R_{S3} and back to the supply.

Switches S1 through S4 are able to conduct in either direction when in the ON state-a very neat feature of power MOSFETs. Furthermore, their intrinsic diode protects the devices from reverse voltage pulses during the switching no-overlap transition. Since we wish to control this current very closely in both magnitude and direction, it is

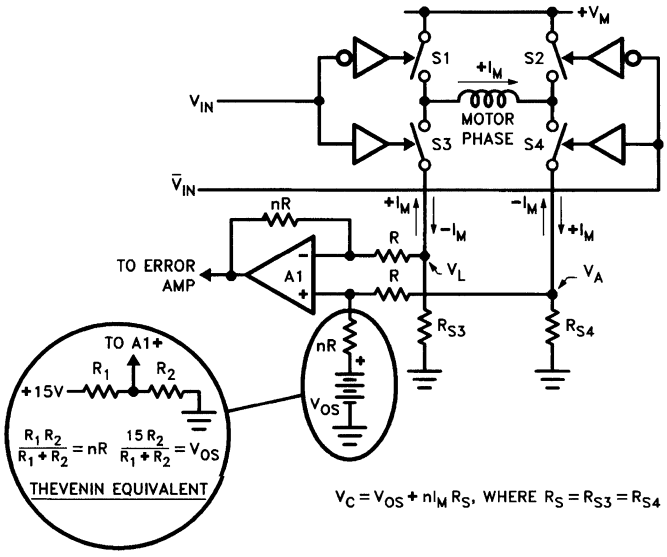


Figure 6. H-Bridge Configuration with Bidirectional Current Sensing

now necessary to generate a voltage V_C that gives an accurate indication of the current I_M over the full range from maximum positive to maximum negative. This is done by the circuit section of Figure 6 which includes the op-amp AI.

In that circuit, the voltage V_{OS} is meant to offset the output V_C of AI to some chosen value that will correspond to $I_M = 0$. The value of Vc can be written as:

(11) $V_C = V_{CS} + nI_MR_S$

This offset is necessary when the design requires a single polarity supply, as in our case. When two supply polarities are available for the control circuit, one can simply make $V_{OS} = 0$. For the single supply case, the nR and V_{OS} combination is implemented by a simple resistor divider from $\pm V_{CC}$ to ground (a Thevenin equivalent) of the required impedance and open voltage.

To keep the circuit losses to a minimum, we should use low values for the sense resistors R_{S3} and R_{S4}. Yet, they need to be accurate and temperature-stable. In our case, having decided on a V_C scale of 0.5V per motor ampere, we have selected $R_S = 0.1\ \Omega$ and a current sense amplifier gain n = 5. We have also set $V_{OS} = V_{CC}/2 = 7.5V$, so that we will have $V_C = 7.5 + 0.5\ I_M$. This means that as the current I_M varies from + 6A to -6A, the analog voltage V_C will vary from + 10.5V to + 4.5V. At $I_M = 0$, V_C will be equal to 7.5V.

SETTING UP THE PWM CONTROLLER

Having designed the power output stage (H-bridge) and the current-sense circuit, we can proceed to the PWM controller (UC3637) and its external components. The device itself has been described in great detail in its data sheet and in an application note (Publication U-102, available from Unitrode Integrated Circuits Corporation).

In the present design, we use the UC3637 to generate the two H-bridge driving signals V_{IN} and $V_{\overline{IN}}$, at the device's output pins 7 and 4, respectively.

Figure 7 shows in block form the internal workings of the device. Since operation from a single + 15V supply is desired, pin 5 will be GROUND and pin 6 will be + 15V. We selected, for the ramp oscillator, a waveform as shown in Figure 8, which fits well in the + 15V headroom given by our V_{CC} supply. The formulas given in Figure 8 show how the various components are calculated.

Next, we set up the two PWM comparators by tying the inverting inputs (pin 10) of the A comparator, and the noninverting input (pin 8) of the B comparator together and apply the ramp (pin 2) to this line. The remaining comparator inputs (pins 9 and 11) are next connected together to become the PWM input point. It can be seen from the block diagram of Figure 7 that as the control voltage applied to this point varies from + 5V to + 10V, the duty cycle of the output at pins 4 and 7 also varies. V_4 and V_7 are complementary signals; and the voltage swing of each of these signals is from a low value between 0V and + 2V, and a high value between (V_{CC} -2V) and V_{CC}.

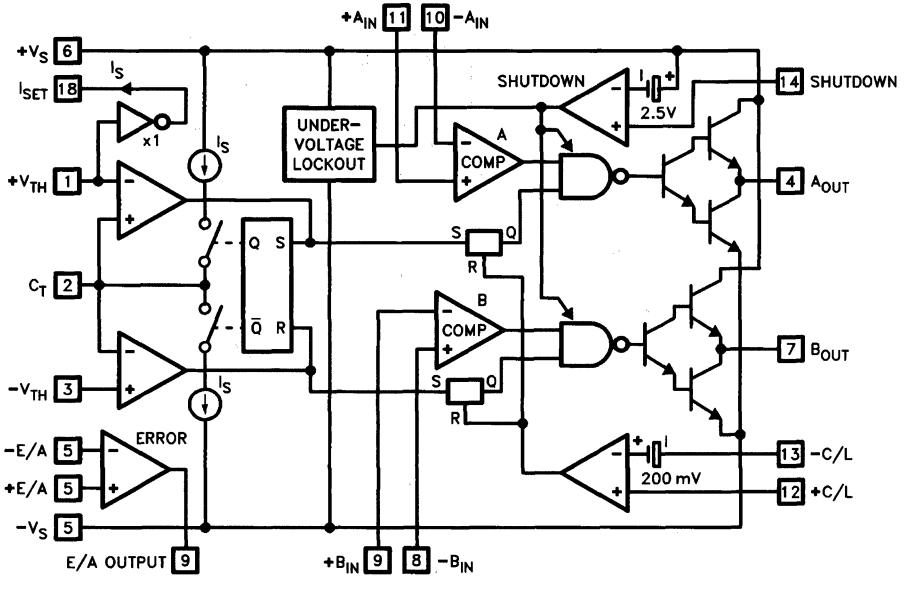
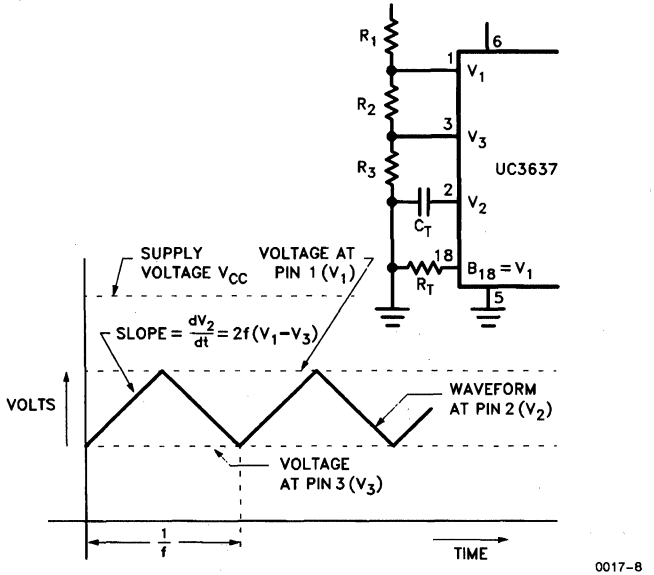


Figure 7. Block Diagram of the UC3637. The two outputs can drive power MOSFETs directly.



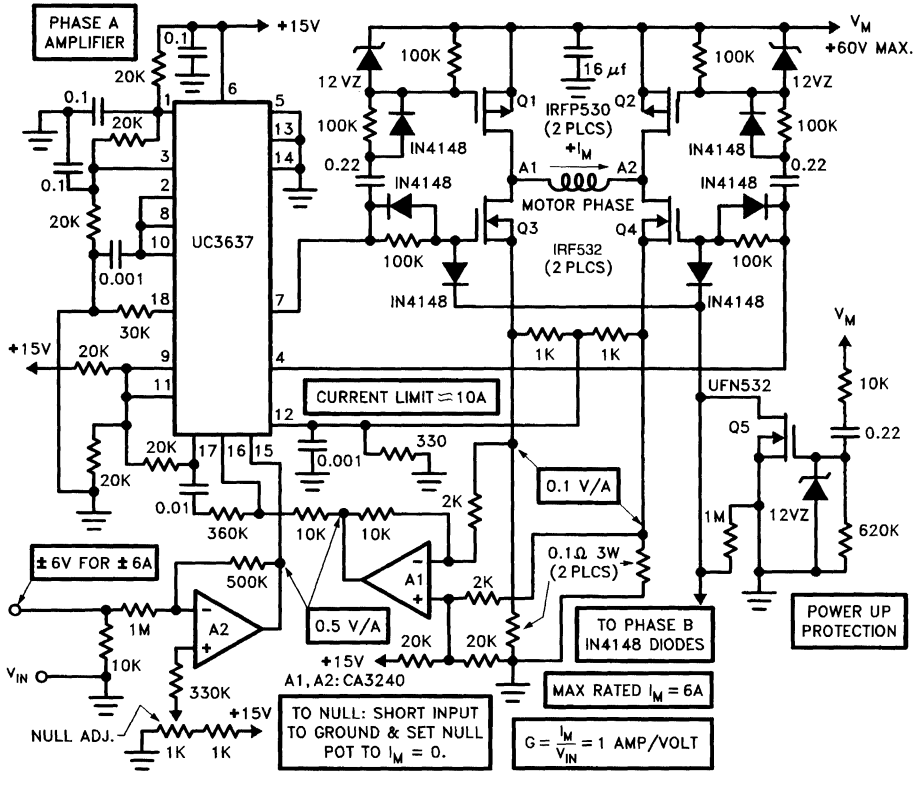
f = ramp frequency

$I_T = \frac{V_{18}}{R_T} = \frac{V_1}{R_T}$ (should be about 0.5 mA)

then, $R_T = 2000\ V_1\ (\Omega)$

$C_T = \frac{250 \times 10^{-6}}{f(V_1 - V_3)}(fd)$

Figure 8. Setting up the ramp oscillator requires only five external components.



0017-9

Figure 9. PWM Transconductance Amplifier UC3637

The error amplifier is used as a source for the control signal. But because its output (pin 17) has a voltage range greater than the + 5V to + 10V range of the V_C ramp signal, and we want to prevent the modulation range from ever reaching 0% or 100% (because of the capacitively coupled P-channel MOSFET devices) we add a simple resistive network consisting of three equal resistors to serve as an attenuator. The final result can be seen in the complete schematic of Figure 9.

CURRENT LIMIT AND CONTROL

The current limit feature of the UC3637 is used to protect the output transistors and motor from excessive current (6A in this case). As the block diagram of Figure 7 shows, the current limit comparator (pins 12 and 13) of the UC3637 is internally biased to a threshold of 200 mV. The network that connects the two sense resistors to pin 12, consisting of two 1K and one 330Ω resistors, causes a voltage of 200 mV to appear at pin 12 when the voltage at either sense resistor is about 1V, corresponding to a current of 10A. Consequently, the maximum output current will be limited to 10A. The current feedback loop is closed by feeding the output of the current sense amplifier to pin 16, the inverting input of the error amplifier of the UC3637. An RC time constant of 3.6 msec is used for the zero in this amplifier's transfer function (equations 8, 9, and 10) which is close to the effective electrical time constant of the motor. Also, a level-shift circuit is provided by means of op amp A2 to permit the use of a control input centered at zero volts, and a control range from -6A to + 6A. The circuit allows this even though the op amp is powered by a single positive supply.

TEST RESULTS

The design circuit, shown in Figure 9, was breadboarded for testing at Unitrode and also at Portescap. The assembly includes two amplifiers, one for each motor phase and a "power on" auxiliary circuit for protection of the power MOSFETs. The output devices are equipped with small sheet metal heat sinks.

The circuit draws about 65 mA from the + 15V supply. The power output section operates with a supply ranging from +20V to + 60V, with no damage occurring if this voltage is lower than + 20V.

The circuit performed very well, with excellent linearity and phase matching. The various plots taken, showing output current versus input voltage, are quite straight, and the transconductance is accurate to within 1%. Furthermore, the PWM frequency was subsequently increased to slightly above 100 KHz (by reducing C_T) and the performance re-checked. The result was a marked increase in motor efficiency, due to reduced current ripple, with all other results remaining excellent.

CONCLUSION

Microstepping is a technique of considerable interest in the design of many products, particularly those in which the lower cost of open-loop positioning is an essential parameter. A motor such as Portescap's Model P-750, with its accurately sinusoidal torque curve, becomes even more attractive once its microstepping driver is shown to be fairly simple and inexpensive. The end result is not only precise open loop positioning, but quiet operation, freedom from resonance problems, and excellent electrical efficiency. Incidentally, the motor is available with two quadrature speed sensing coils that can be used for speed and position control, if desired.

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DESIGN NOTES ON PRECISION PHASE LOCKED SPEED CONTROL FOR DC MOTORS

ABSTRACT

There are a number of high volume applications for DC motors that require precision control of the motor's speed. Phase locked loop techniques are well suited to provide this control by phase locking the motor to a stable and accurate reference frequency. In this paper, the small signal characteristics, and several large signal effects, of these loops are considered. Models are given for the loop with design equations for determining loop bandwidth and stability. Both voltage and current motor drive schemes are addressed. The design of a loop for a three phase brushless motor is presented.

PHASE LOCKING GIVES PRECISION SPEED CONTROL

The precise control of motor speed is a critical function in today's disc drives. Other data storage equipment, including 9 track tape drives, precision recording equipment, and optical disc systems also require motor speed control. As the storage density requirements increase for these media, so does the precision required in controlling the speed of the media past the read/write mechanism. One of the best methods for achieving speed control of a motor is to employ a phase locked loop.

With a phase locked loop, a motor's speed is controlled by forcing it to track a reference frequency. The reference input to the phase locked loop can be derived from a precision crystal controlled source, or any frequency source with the required stability and accuracy. A block diagram of the phase locked loop is shown in Figure 1.

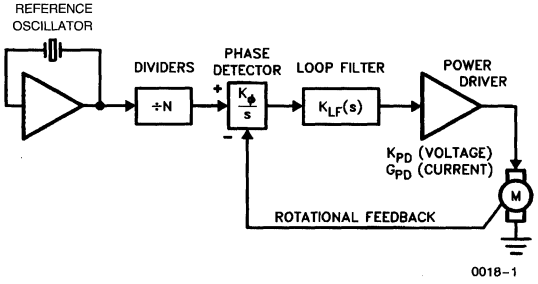


Figure 1. Precise motor speed control is obtained by phase locking the motor to a precision reference frequency.

In Figure 1, a precision crystal oscillator's frequency is digitally divided down to provide a fixed reference frequency. Alternatively, the motor could be forced to track a variable frequency source with zero frequency error. The motor speed is sensed by either a separate speed winding or, particularly in the case of the DC brushless motor, a Hall effect device. The two signals, motor speed and reference frequency, are inputs to a phase detector. The detector output is a voltage signal that is a function of the phase error between the two inputs. The transfer function of the phase detector, K_ϕ, is expressed in volts/radian. A 1/s multiplier accounts for the conversion of frequency to phase, since phase is the time integral of frequency.

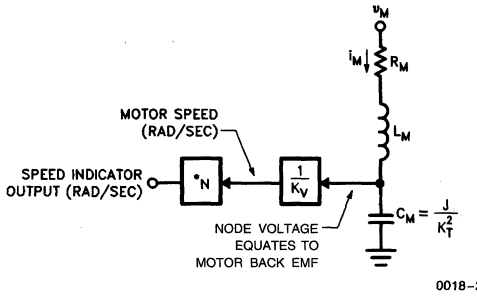
Following the phase detector is the loop filter. This block contains the required gain and filtering to set the loop's overall bandwidth and meet the necessary stability criteria. The output of the loop filter is the control input to the motor drive. Depending on the type of drive used, voltage or current, the driver will have respectively, a V_{OUT}/V_{IN} transfer characteristic, or an I_{OUT}/V_{IN} transconductance.

At first glance, it seems that the motor has simply replaced the V_{CO} (voltage controlled oscillator), in the classic phase locked loop. In fact, it is a little more complicated. The mechanical and electrical time constants of the motor come into play, making the transfer function of the motor more than just a voltage-in, frequency-out block. In order to analyze the loop's small and large signal behavior it is essential to have an equivalent electrical model for the motor.

A SIMPLE ELECTRICAL MODEL FOR A DC MOTOR

Figure 2 is an electrical representation of a DC motor. The terms used are defined here:

L_M Motor winding inductance in henrys
R_M Motor winding resistance in Ωs
J Total moment of inertia of the motor in Nm-sec^2
(Note: 1 Nm = 141.6 oz-in)
K_T Motor torque constant in Nm/Amp
K_V Voltage constant (back EMF) of motor in volt-sec/rad
(Note: $K_V = K_T$ in SI units)



*N = Number of speed sense cycles per motor revolution

Figure 2. This simple electrical model is useful for determining the small and large signal characteristics of the motor. Capacitor, C_M is used to model the mechanical energy storage of the motor.

In this model the winding inductance and resistance elements correlate directly with the corresponding physical parameters of the motor, with values taken directly off the manufacturer's data sheet. The capacitor, C_M, models the mechanical energy storage of the motor. Current into the capacitor equates, via motor constant K_T, to motor torque, and the voltage across the capacitor is equal to the motor back EMF. The back EMF voltage equates to motor velocity through the inverse of K_V. In the model, the term N is simply a multiplier equal to the number of feedback cycles obtained per revolution of the motor. For example, in a 4 pole brushless DC motor the commutation Hall effect device outputs will be at twice the rotational frequency of the motor, making N equal to 2.

The equation for the capacitor, given in Figure 2, has the units of Farads if J and K_T are expressed in SI units. In modeling the overall transfer characteristic, it is important that the moment of inertia of the load on the motor be added to the moment of inertia of the motor itself.

It is worthwhile to note that the current into the motor, minus idling current, is proportional to acceleration of the motor. This is easily seen from the model by realizing that the time derivative of the capacitor voltage relates directly to acceleration. The effects of loads on the motor can be modeled by including a current source across the capacitor for constant torque loads, or a resistor for loads that are linearly proportional to motor speed.

TRANSFER FUNCTIONS FOR VOLTAGE AND CURRENT DRIVEN MOTORS

Using the electrical model, the small signal transfer function of the motor is easily derived. Equations 1a and 1b give the small signal frequency response for both the current and voltage driven cases respectively.

$$1a)\quad \frac{N \times \omega_M(s)}{i_M(s)} = \frac{N}{K_V} \times \frac{1}{sC_M}$$

$$1b)\quad \frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{1 + sC_MR_M + s^2 L_MC_M}$$

The transfer function given in equation (1a) describes the small signal response of motor speed, $\omega_M(s)$, to changes in the drive current. Equation (1b) relates the dependence of motor speed to motor drive voltage.

The small signal response of the motor for the current driven case has a DC pole that results from the relationship of motor torque to velocity, that is, motor velocity is proportional to the integral of motor torque over time. In the current driven motor neither the winding resistance nor inductance appear in the transfer function. This is because these elements are in series with the current source output of the driver stage. As long as the output impedance of the driver remains large relative to the impedance of these elements, the resistance and inductance of the motor will have a negligible effect on the small signal response.

The voltage driven response has a second order characteristic that results from the interaction of the series RLC. In many cases the transfer function of the voltage driven case can be simplified. If the quality factor of the series RLC of the motor model is much less than one, as defined in equation 2, then the response of the motor can be accurately approximated by equation 3.

$$2)\quad Q_M = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} = \frac{K_T}{R_M}\sqrt{\frac{L_M}{J}}$$

$$\therefore Q_M \ll 1 \quad \text{If } R_M \gg K_T\sqrt{\frac{L_M}{J}}$$

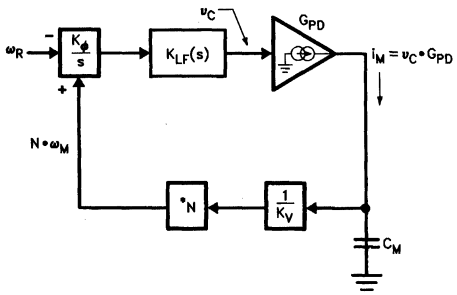
$$3)\quad \text{For } Q_M \ll 1$$

$$\frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{(1 + sC_MR_M)(1 + sL_M/R_M)}$$

CONSIDERING THE WHOLE LOOP

Figure 3 shows the complete speed control loop for the current driven case. The overall open loop response, A_{OLC}, is easily written.

$$4)\quad A_{OLC}(s) = \frac{K_\phi \times K_{LF}(s) \times G_{PD} \times N}{s^2C_M \times K_V}$$



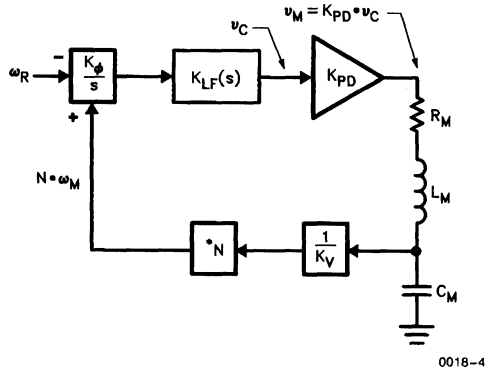
*N = Number of feedback cycles per motor revolution

Figure 3. In this phase locked loop, with current mode drive to the motor, the motor winding resistance and inductance can be ignored as long as the current driver maintains a high output impedance.

For this loop, note that there are two poles in the response at DC, i.e., s = 0. One pole is due to the response of the current driven motor, the second pole is from the frequency to phase transformation of the phase detector. The 180 degrees of phase shift this pair of poles introduce force a phase lead configuration of the loop filter in order to obtain a loop phase margin greater than zero.

The complete voltage loop is shown in Figure 4, and its open loop response, $A_{OLV}(s)$, in equation 5.

$$5)\quad A_{OLV}(s) = \frac{K_\phi \times K_F(s) \times K_{PD} \times N}{sK_V \times (1 + sC_MR_M + s^2 L_MC_M)}$$



*N = Number of feedback cycles per motor revolution

Figure 4. With voltage mode drive to the motor the electrical time constant of the motor plays a part in the small signal response of the speed control loop.

This response has only one pole at DC, although the total number of poles is three versus two for the current driven case. For most motors, particularly those used in constant velocity applications, this transfer function can be simplified by applying the results of equations 2 and 3. This is best illustrated by looking at an example. Consider the following motor, (typical 3-phase brushless for disc drive applications):

K_T ..... 1.5×10^{-2} Nm/Amp
K_V ..... 1.5×10^{-2} V-sec/rad
J (including platters) ..... 1×10^{-3} Nm-sec2
R_M 2.5R
LM 2mH

For this motor, the model capacitor, C_M, is calculated using the equation in Figure 2 to be equal to 4.4 Farads. If we calculate the quality factor of the series RLC, using equation 2, we find it is equal to 42.4×10^{-3}. This is considerably less than one, and the response closely approximates the non-complex response of equation 3 with poles at 0.014 Hz and 199 Hz.

Typical loop bandwidths will fall well inside this range of frequencies. As long as this is true, the loop response with a voltage driven motor can be approximated by:

$$6)\quad A_{OLV}(s) \approx \frac{K_\phi \times K_{LF}(s) \times K_{PD}/R_M \times N}{s^2 C_M K_V}$$

$$\text{If } Q_M \ll 1 \text{ and } \frac{1}{2\pi C_M R_M} < f < \frac{R_M}{2\pi L_M} \left(f = \left|\frac{s}{2\pi}\right|\right)$$

This expression is the same as the current driven response equation 4, with the transconductance of the current drive stage, G_{PD}, replaced by the gain of the voltage drive stage divided by the motor winding resistance, K_{PD}/R_M.

CLOSING THE LOOP

When it comes to closing the loop the goal is to have a stable loop with the required loop bandwidth. The variables that must be considered are:

1) The motor
2) The power driver, type and gain
3) The phase detector gain
4) Loop bandwidth
5) The loop filter

The first four of the above variables are usually dictated by conditions other than the stabilizing of the loop. This leaves the loop filter as the tool for achieving the small signal loop requirements.

For many cases involving constant velocity loops for DC motor speed control, the following simple Bode analysis can be applied for determining the design of the loop filter. Assuming we know, or have preliminary guesses for the first four variables listed above, we can plot the Bode asymptotes for phase and gain of the combined response of the motor and power driver. Figure 5 shows, for a typical case, such a plot on a frequency scale that has been normalized to the desired loop bandwidth, or open loop unity gain frequency. This figure illustrates the small signal open loop response for the current driven case, equation 4, minus the response of the loop filter, K_{LF}. If the previously noted assumptions hold, this plot will also apply to the voltage driven case i.e., equation 6.

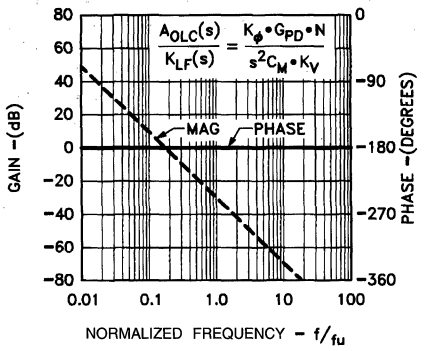


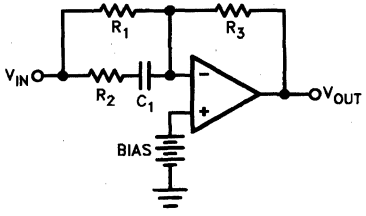
Figure 5. A Bode plot of the combined gain and phase response of the motor, motor drive, and phase detector is useful in determining the requirements on the loop filter. This plot is normalized to the desired open loop unity gain frequency.

From Figure 5 two restrictions on the loop filter are readily apparent. First, since the remaining portion of the loop has 180° of phase shift over the entire frequency range, the loop filter must have a phase lead at the unity gain frequency and at all frequencies below the unity gain frequency. By meeting this restriction the small signal loop will be unconditionally stable.

Secondly, in order to achieve the desired loop bandwidth, the loop filter must have a voltage gain at the desired unity gain frequency of 30 dB. This level is simply the inverse of the remaining loop's voltage gain at the unity gain frequency.

A loop filter configuration that will meet these restrictions is shown in Figure 6. Also shown in this figure is the small signal response equation for the filter. The response starts out from DC with a flat inverting gain that breaks upward at the zero frequency, ω_Z, and then flattens out again at the pole, ω_P. The pole in this response is necessary to prevent excess feedthrough of residual reference frequency that is present at the outputs of many digital type phase detectors–in fact, as will be discussed in the design example, a separate reference filter is normally required.

A good choice for the relative positioning of the pole and zero of the loop filter response is to space them apart by 1 decade of frequency, and center them around the unity gain frequency. Figure 7 shows the Bode plots of this suggested positioning applied to the case illustrated in Figure 5. As shown, a phase margin of about 45° is obtained with this configuration.



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_3}{R_1} \times \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\,C_1}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

Figure 6. This loop filter configuration provides the required phase lead and gain at the loop crossover frequency.

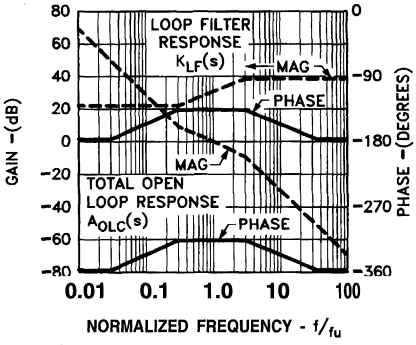


Figure 7. Using the criteria set forth for the design of the loop filter, the resulting Bode plot indicates a phase margin of 45°.

If the above results are acceptable, then the following simple steps can be applied to pick the loop amplifier component values. Referring to Figure 6.

1) Pick R_3 to be as high in value as acceptable for the Op-Amp and board restrictions.

2) $R_1 = (R_3 \times 3.33)/10^{X/20}$, where X is the voltage gain, in dB, required at the unity gain frequency.

3) $R_2 = R_1/9$, sets a 10:1 ratio for ω_P to ω_Z.

4) $C_1 = (2\pi \times R_2 \times 3.33 \times f_\mu)^{-1}$, where f_μ is the loop unity gain frequency.

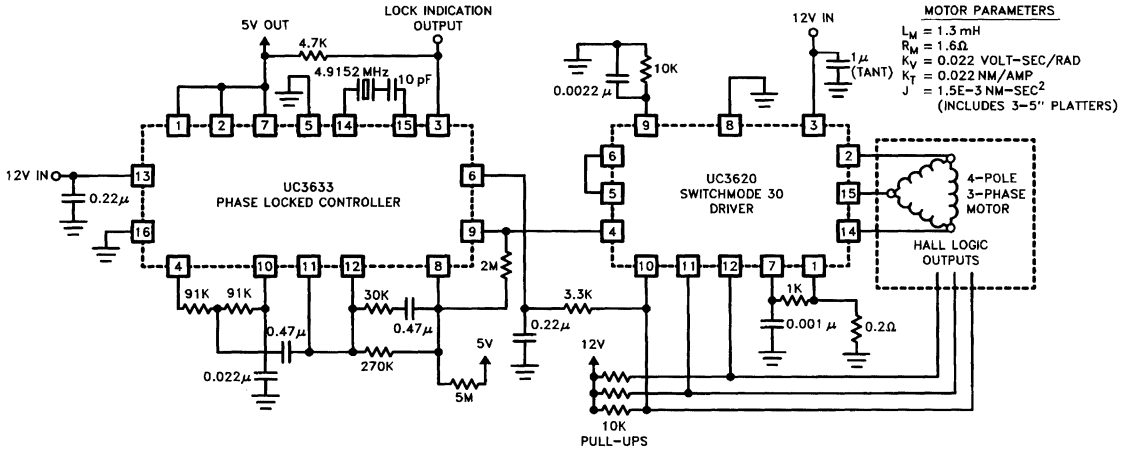
Using this simple procedure the small signal loop is easily closed for stable static operation.

A DESIGN EXAMPLE

As an example, let us take a look at the complete design of a constant velocity speed control loop for a disc drive application. The performance characteristics for the circuit can be summarized as:

Motor speed . . . . . 3600 rpm ± 60 ppm (0.006%)
Speed stability . . . . . ± 50 ppm
Start-up lock time . . . . . 10 seconds
Input voltage . . . . . 12 Volts
Motor idling current . . . . . 0.5 Amps

The schematic for this design is shown in Figure 8. The motor is a 4 pole 3-phase brushless with the electrical and mechanical specifications given in the figure. The motor is current mode driven with the UC3620 3-phase Switchmode Driver. The speed control function is realized with the UC3633 Phase Locked Controller.



0018-8

Figure 8. A precision speed control loop uses the UC3620 Switchmode 3-phase Driver and the UC3633 Phase Locked Controller to spin a DC brushless motor at 3600 rpm, ± 60 ppm.

POWER DRIVER STAGE

In Figure 9 a detail of the driver IC and the associated circuitry is shown. The UC3620 is a current-mode, fixed off-time, chopper. Three 2-Amp totem pole output stages with catch diodes drive the three motor phases. The outputs are enabled by the internal commutation logic that responds to the three Hall logic signals from the motor. The motor is equipped with open collector Hall devices making the three 10k pull-up resistors on the UC3620 Hall inputs necessary.

Current is controlled by chopping the lowside drive to the phase winding under the command of the UC3620's current sense comparator. The RC combination on the timing pin of the driver sets the off-time at 22 μs. This results in a chopping frequency of well over 20 kHz under normal operating conditions.

The transconductance of the driver is set by the value of current sense resistor used at the emitter pin of the UC3620. With a value of 0.2Ω the transconductance from the error amplifier output to the driver outputs is 1 Amp/Volt. The UC3620 error amplifier is configured here as a unity gain buffer, thus the drive control signal is applied at the non-inverting error amplifier input with the same overall transconductance. An internal 0.5V clamp diode at the current sense comparator input results in a 2.5 Amp maximum drive current. There is a 1V offset internal to the UC3620 that is reflected to the drive control input at zero current. This offset combines with the 0.5 Amp idling current level of the motor to set the steady state DC voltage at the driver control input to be 1.5V.

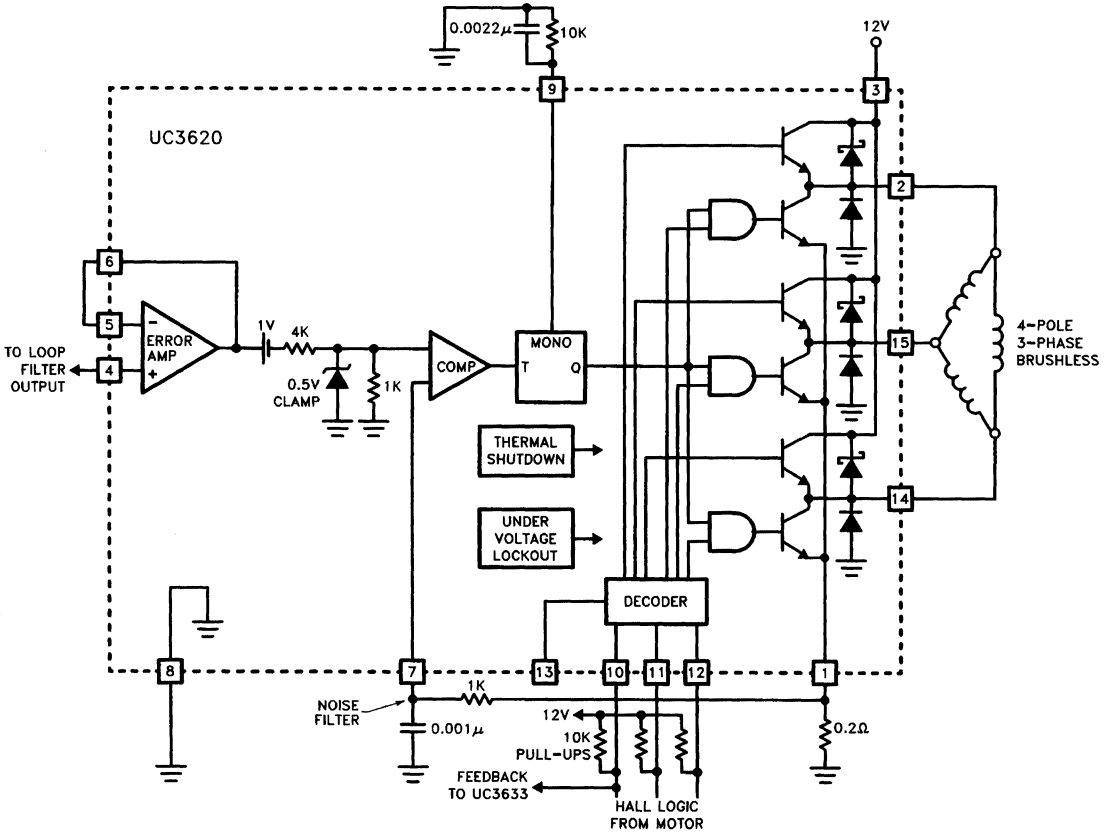
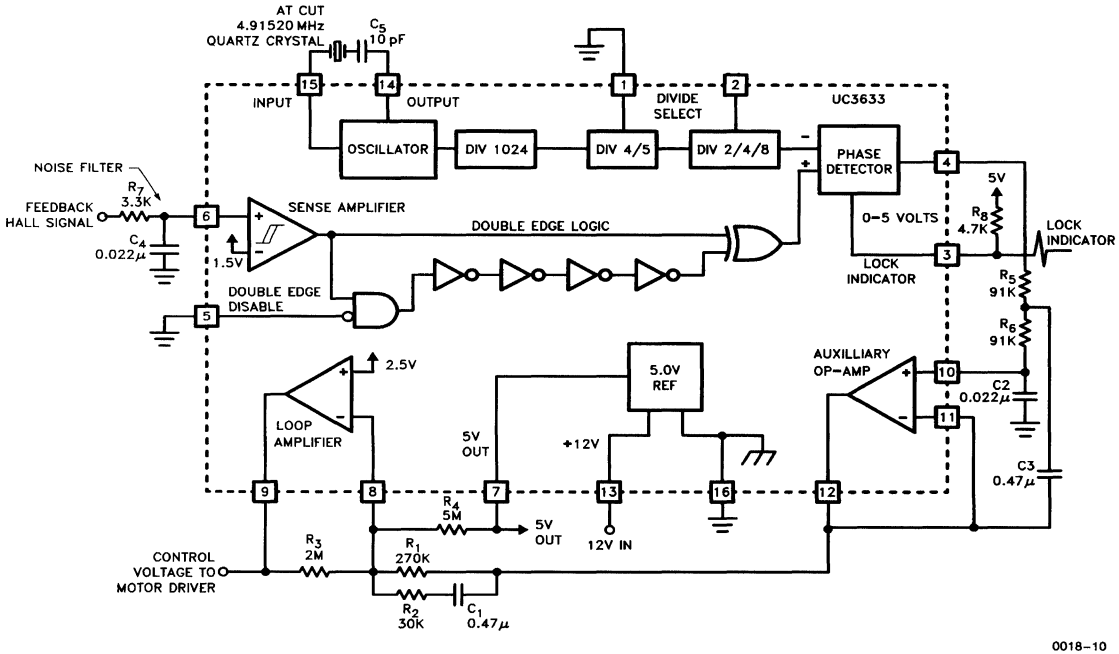


Figure 9. The UC3620 is a current mode fixed off-time driver. This device includes all the drive and commutation circuitry for a three phase brushless motor. The 0.2Ω current sense resistor and the internal divide by five sets the transconductance of this power stage to 1 Amp/Volt.



0018-10

Figure 10. Phase locking the motor to a precision reference frequency is achieved with the UC3633. The double edge sensing option on this device doubles the loop gain and allows twice the reference frequency to be used for a given motor RPM by forcing the phase detector to respond to both edges of the Hall feedback signal.

PHASE LOCKED CONTROL CIRCUIT

A detail of the phase locked control portion of the design is given in Figure 10. The UC3633 contains all of the circuitry required for this function including: a crystal oscillator, programmable reference dividers, a digital phase detector, and op-amps for the required filtering. The UC3633 receives velocity feedback from the Hall signal applied at its sense amplifier input pin. The sense amplifier has a small amount of hysteresis that provides fast rising and falling input edges to the following logic. A double edge option is available on the UC3633 sense amplifier. When this option is enabled, as it is in this design, the phase detector is supplied with a short pulse on both the rising and falling edges of the feedback signal, effectively doubling the loop gain and reference frequency.

The required reference frequency for this loop is 240 Hz, given by the product of the motor rotation of 3600 rpm (60 Hz), the number of cycles/revolution at the Hall outputs (two for a 4 pole motor), and a factor of two as a result of the double edge sensing. The divider options on the UC3633 are set up such that standard microprocessor crystals can be used. In this instance, a 4.91520 MHz (±50 ppm) AT cut crystal is divided by 20,480 to realize a 240 Hz reference frequency input to the phase detector.

The phase detector on the UC3633 responds to phase differences at its two inputs with output pulses at the reference frequency rate. The width of the pulses is linearly proportional to the magnitude of the phase error present.

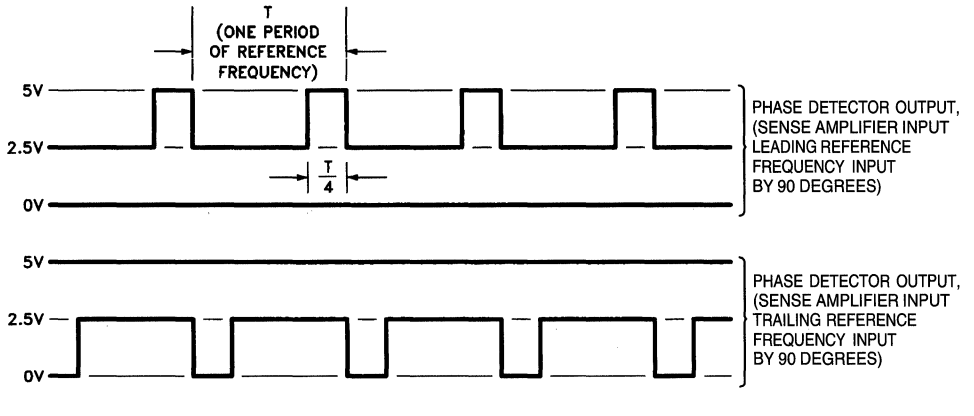


Figure 11. The phase detector on the UC3633 is a digital circuit that responds to phase error with a pulsed output at the reference frequency rate. The width and polarity of the pulses depend respectively on the phase error magnitude and polarity. If any static frequency error is present, the detector will respond with a constant 0 Volt or 5 Volt signal depending on the sign of the error present.

The pulses are always 2.5V in magnitude and are referenced to 2.5V at the detector output. The polarity of the output pulses tracks the polarity of the input phase error. This operation is illustrated in Figure 11. The resulting phase gain of the detector is $2.5V/2\pi$ radians, or about 0.4V/rad, with a dynamic range of $\pm 2\pi$ radians.

The phase detector also has the feature of absolute frequency steering. If any static frequency error exists between the two inputs, the output of the detector will stay in a constant high, or low state; 5V, if the feedback input rate is greater than the reference frequency and 0V, if the opposite frequency relationship exists. The lock indicator output on the UC3633 provides a logic low output when any static error exists between the feedback and reference frequencies.

A unity gain bandwidth of 4 Hz was chosen for this loop. This unity gain frequency is well below the effective sampling frequency, the 240 Hz reference, and is sufficiently high to not significantly affect the start-up lock time of the drive system. The design of the loop filter follows the guidelines described earlier. The magnitude of the loop gain, minus the loop filter, at 4 Hz is equal to:

$$\frac{K_\phi \times G_{PD} \times N}{(2\pi f)^2 \times C_M \times K_V} = \frac{(0.4)(1)(4)}{(2\pi 4)^2(3.1)(0.022)}$$

$= 37.2$ E-3 or -28.6 dB.

This dictates that the loop amplifier has a gain of 28.6 dB at 4 Hz. A value for the loop amplifier feedback resistor, R_3, of 2 MΩ was chosen. The values for R_1, R_2 and C_1 were calculated as follows.

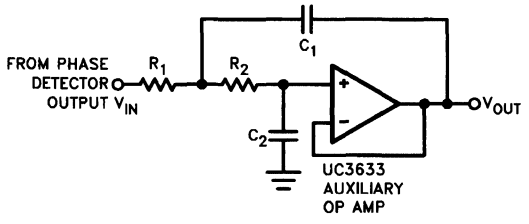
$R_1 = (2E6 \times 3.33)/10^{28.6/20} = 248$ kΩ (270 kΩ used).

$R_2 = 270/9 = 30$ kΩ

$C_1 = (2\pi \times 30E3 \times 3.33 \times 4)^{-1}$
$= 0.4$ μF (0.47 μF used).

The additional op-amp on the UC3633 is used to realize a second order active filter to attenuate the reference component out of the phase detector. The filter is a standard quadratic with a natural frequency of 17.2 Hz and a Q of about 2.3. This circuit provides 46 dB of attenuation at 240 Hz while adding only 5° of phase shift at the 4 Hz loop crossover frequency. In Figure 12 design guidelines and response curves for this filter are given.

Reference Filter Configuration



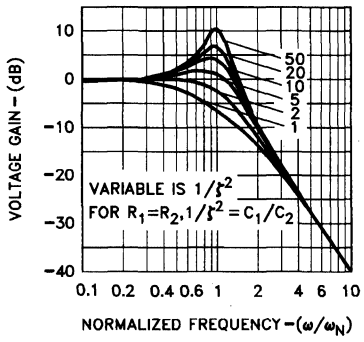
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid-Gain Response



Reference Filter Design Aid-Phase Response

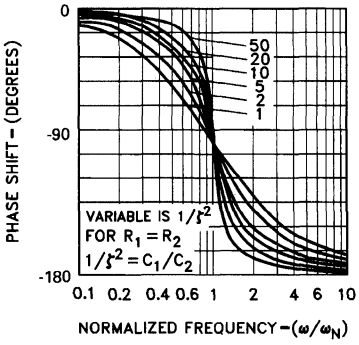


Figure 12. To keep feedthrough of the residual reference frequency at the phase detector output to a minimum, a simple quadratic filter can be used. The design of this filter is easily accomplished with the above equations and response curves.

As mentioned earlier, a separate reference filter is required in this type of phase locked loop to attenuate the reference frequency feedthrough at the output of the phase detector. With the active filter following the phase detector, the feedthrough to the loop amplifier is kept to less than $20mV_{pp}$ under the worst case condition of $\pm\pi(180°)$ phase error. This is small compared to the 1.25V DC signal out of the detector at this phase error. If the reference ripple into the loop amplifier becomes large compared to the averaged phase error term, large signal instabilities may result. These are primarily the result of the unidirectional nature of the motor drive.

The static reference ripple at the motor drive input, during phase locked conditions, can be minimized by forcing the loop to lock at zero phase error-at zero phase error there is no reference frequency component at the detector output. The finite DC gain through the loop filter, dictated by the inherent second order nature of the loop, results in a static phase error that is a function of: the DC level required at the motor drive input, the DC gain and reference voltage of the loop amplifier, and the voltage levels out the phase detector. The addition of resistor R_4, see Figure 10, from the loop amplifier's inverting input to

the 5V reference sets the zero phase operating voltage at the loop filter output to 1.5V. This matches the nominal operating voltage required at the UC3620 control input, taking into account the 0.5 Amp idling current of the motor and the 1V offset of the driver. This cancellation is subject to variations due to shifts in DC operating levels, so, while it does significantly reduce static reference feedthrough, it can not be expected to reliably set exactly zero phase operation.

The oscilliscope traces in Figure 13 show the Hall input to the UC3633 along with the output waveform of the digital phase detector under static phase locked conditions. Notice that the phase detector output is alternating between positive and negative output pulses. This is a result of a slight asymmetry on the Hall input signal in conjunction with the use of the double edge sensing being used. In this case, the asymmetry is due to differences in the rising and falling edges of the Hall signal that result from the RC filter at the sense amplifier input. This filter is required to keep high frequency noise from the motor drive out of the phase detector.

The startup response of the motor is pictured in Figure 14. Shown are the voltage waveforms at the lock indicator output, the loop amplifier output, and the phase detector output of the UC3633. At the moment the lock indicator goes high the motor has reached its operating velocity. The absolute frequency steering of the phase detector forces a slight overshoot in frequency that delays the settling of the loop by about 1 second. Without the frequency steering feature the phase detector would command a much lower average drive signal during startup, extending the start time by over 50%.

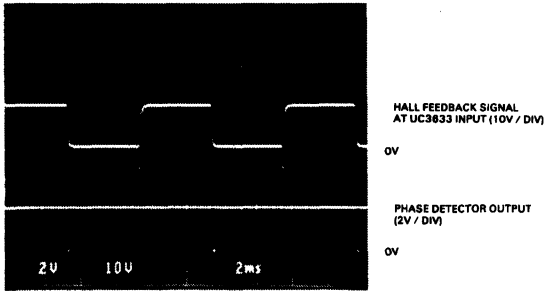


Figure 13. This oscilloscope trace shows the static waveforms at the Hall sensor input, and phase detector output of the UC3633. The static phase error has been adjusted, with R_4 in Figure 10, to be very small. The alternating positive and negative pulses at the output of the phase detector is due to an asymmetry in the Hall signal.

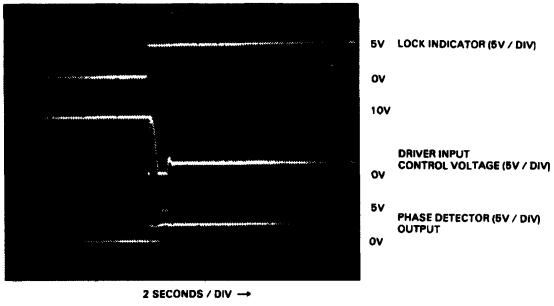


Figure 14. The startup lock time of the motor is minimized with the absolute frequency steering feature of the phase detector, keeping lock times under 10 seconds.

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APPLICATION NOTE

New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors

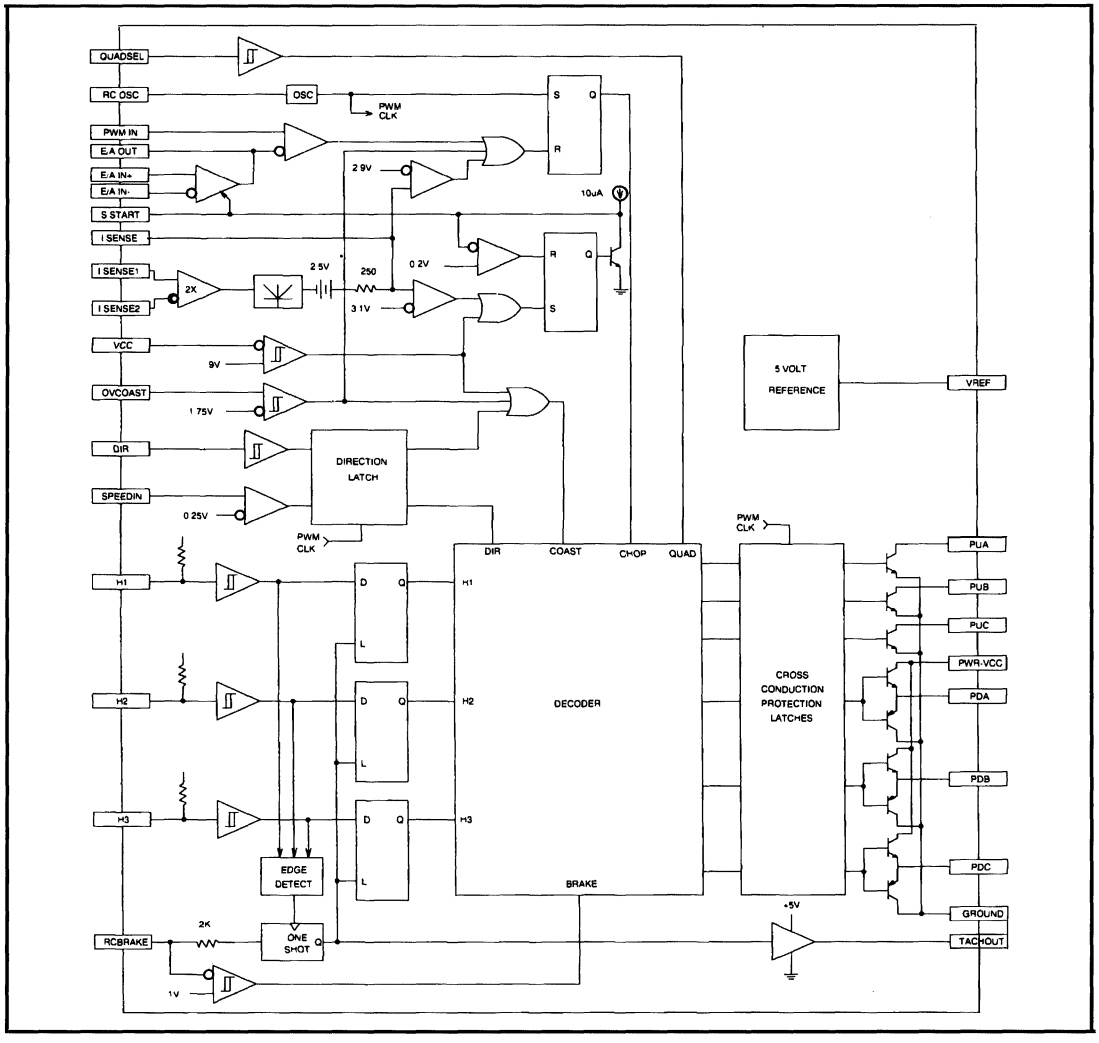
Bob Neidorff, Unitrode Integrated Circuits Corp., Merrimack, NH

Abstract

A new integrated circuit for brushless DC motor control is presented that implements many new techniques to enhance reliability and reduce the detrimental effects of noise. In addition to safety features and noise rejection circuitry, the new circuit contains a complete pulse-width modulator (PWM), a practical tachometer, a precision voltage reference, a high-speed current-sense amplifier, and high-voltage, high power, output stages.

Various applications of the IC are discussed in detail, including using the PWM for fixed frequency and fixed off-time control, driving power MOSFETs, driving bipolar power transistors, and sensing winding current. The IC is shown in applications that allow braking and direction reversal without damage to the motor or the power semiconductors.

BLOCK DIAGRAM OF THE UC3625



The Problem

Conventional brush motors have proven reliable and versatile. They remain popular partly because the pressures to improve haven't been high, and partly because nothing better has been available that is practical. Brushless DC motors (BDCMs) can pack the same horsepower into smaller, lighter boxes. They can also accelerate faster due to inherently lighter rotor construction. Without the friction and arcing of brushes, they are acoustically quieter. As they have permanent magnet rotors, they are faster to manufacture. Permanent magnet rotors also dissipate very little power, so BDCMs have far less heat dissipation problems.

One thing that has held the motor industry back has been the availability of economical control electronics. Recent price trends in power MOSFETs and monolithic motor controllers have reduced these limits. The final hurdle to broad acceptance is assurance of reliability. Brush motors proved their reliability not through design, but instead through over a hundred years of development of rugged brushes and slip rings.

Two problems with BDCMs today are performance and reliability in the presence of noise. Noise here can refer to externally generated electromagnetic noise, internally generated chopping noise, or inappropriate commands from the operator of the system.

The UC3625 specifically addresses the need for an economical, robust BDCM controller by specifically addressing these failure modes and also by implementing many functions and features desirable in high performance motor systems. The following table outlines some of the important features of the UC3625:

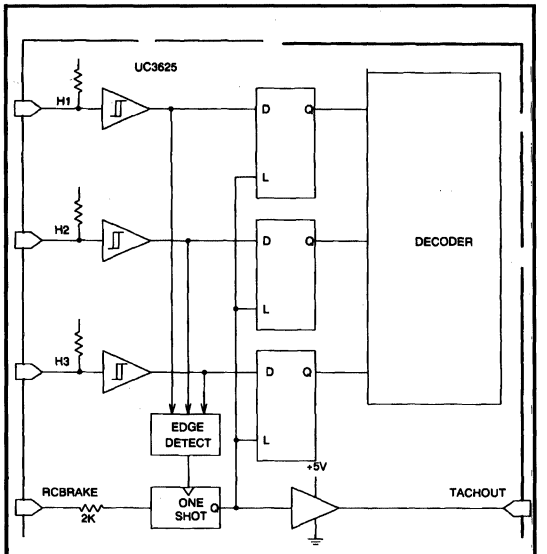
- Push-Pull Low-Side Drivers
- Versatile High-Side Drivers
- Complete PWM
- Two or Four-Quadrant Chopping
- Tachometer
- Soft Start
- Undervoltage Protection
- Overvoltage Protection
- Active Safe Braking
- Differential Current Amp
- Hysteresis on all inputs
- Direction latch
- Cross Conduction prevention

Unique Features For Noise

All logic inputs to the UC3625 have hysteresis and /or latches for maximum noise rejection. The position sensor inputs specifically contain 0.8 volts of hysteresis, yet still meet TTL input thresholds. These inputs also contain pull-up resistors allowing them to directly interface to open-collector sensors.

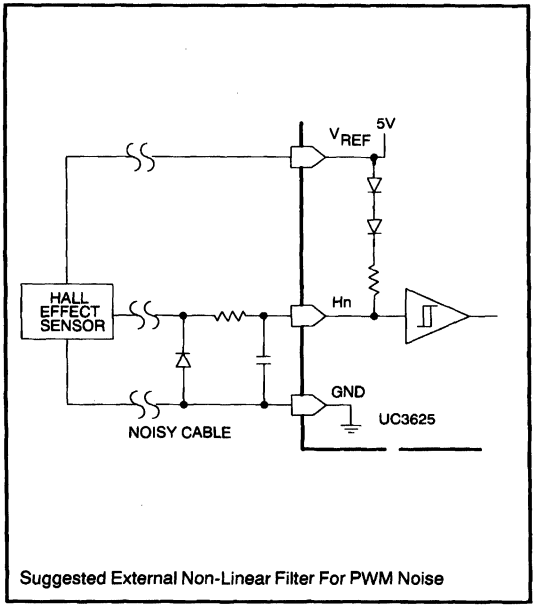
Position sensor inputs are latched immediately following commutation, and remain latched through the on-time of the tachometer monostable (one-shot). This prevents commutation noise from reaching the decoder, latching out the largest noise spike in the motor system. Although this sets a maximum motor speed, correct choice of pulse width guarantees operation up to the maximum speed of the motor while still affording excellent noise rejection.

The one-shot pulse also drives a low saturation-voltage driver connected to TACH OUT. The average value of the voltage on TACH OUT is directly proportional to motor speed, so that the pulse generator doubles as a simple tachometer.



Tachometer Doubles As Input Noise Gate

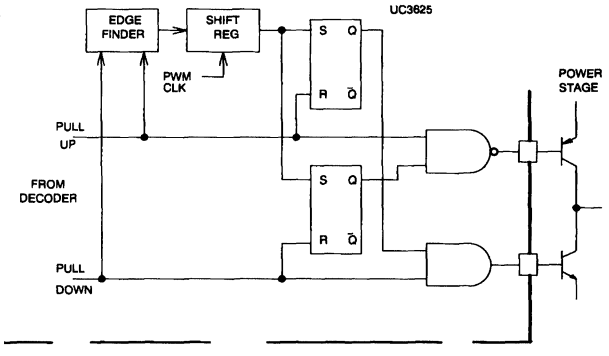
Even with input latches, external noise filtering is often valuable. Chopping noise lends itself to analog low-pass filtering because of its dominant high-frequency components. As high-frequency noise energy can be very strong, zener clamping ahead of the filter can be very effective.



Suggested External Non-Linear Filter For PWM Noise

Cross-Conduction Prevention

To further assure noise immunity, the UC3625 contains latches and a shift register to guarantee that all power stages turn off and remain off for a minimum time before changing states. In addition to preventing noise-induced cross conduction, this prevents cross conduction due to slow power stages.



Logic That Prevents Cross Conduction

The delay time is only inserted when an output is commanded from high to low or vice versa. During normal three phase commutation, outputs are turned off (opened) for a full cycle before changing states, so this delay will not impede normal operation. The only times that this delay will be inserted are during noise spikes, direction reversal, and braking.

Pulse-Width Modulation System

Motors perform better with higher operating voltages because for a given value of inductance, higher voltages can change winding current faster. A necessary adjunct to higher supply voltages is current control, either by linear amplifiers of pulse-width modulation (PWM). The UC3625 uses fixed frequency PWM for chopping.

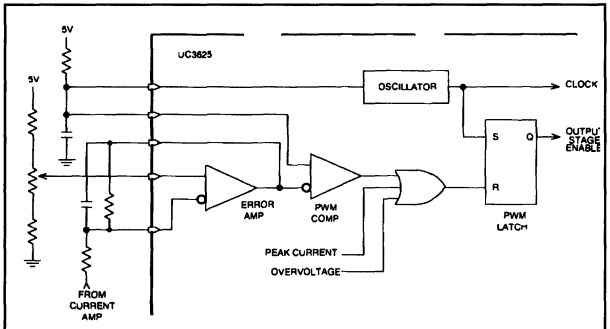
At the heart of the PWM is a sawtooth oscillator. The oscillator is programmed up to 500kHz with one resistor to the reference and one capacitor to the ground. This oscillator is used to enable the PWM latch every cycle, and also to clock the protection shift registers.

Another fundamental part of the PWM is the PWM latch. The output of this latch enables the power stages. The latch is set once per cycle by the oscillator, and cleared by either the PWM comparator, a peak current signal generated in current-sense circuitry, or by a fault signal from the OV/COAST input. This latch is reset dominant, meaning that a steady reset signal from any of three sources completely inhibits the power stages.

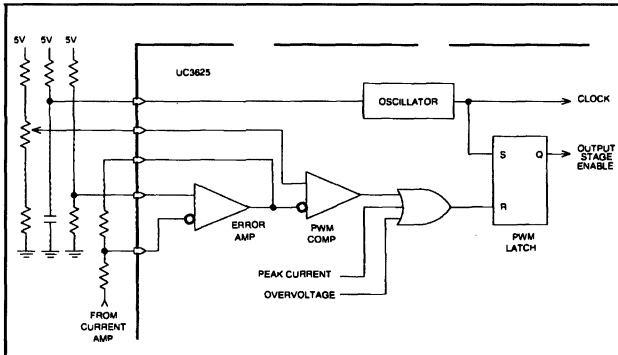
The other elements in the PWM are the PWM comparator and the error amplifier. The PWM comparator is an NPN-input comparator dedicated to comparing the output of the error amplifier to some other signal such as a command voltage, ramp, or sensed signal. The error amplifier is a PNP-input op-amp compensated for unity-gain operation, who's inputs can operate linearly down to ground.

The PWM can be configured into any number of different loops that regulate winding current (torque is nearly proportional to winding current), regulate speed, or regulate some other parameter. The PWM is internally configured for peak current control as well, although this is not intended to be the principle feedback loop.

The approach above compares winding current to a DC voltage with the PWM comparator, and pulse-by-pulse regulates winding current. This is similar to "current mode" in PWM power-supply systems, and offers the advantage of removing the pole caused by load inductance from the feedback loop.



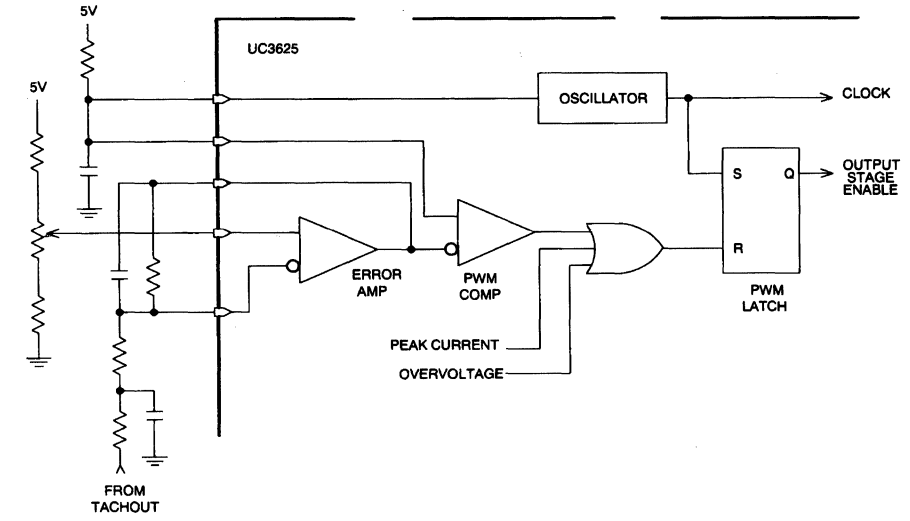
PWM Configured For Average Current Feedback



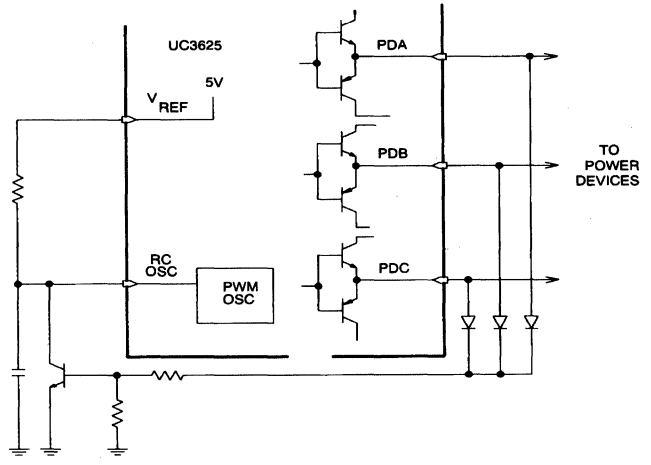
UC3625 PWM Block Diagram Configured For Pulse-By-Pulse Current Control

The PWM can also be configured to use the error amplifier to amplify the difference between the winding current and a desired current, and to use the PWM comparator to compare the error amp output to the oscillator ramp. This current loop operates on average, rather than peak current.

If the PWM comparator is used to compare the oscillator ramp to a DC voltage, then the load duty cycle is directly proportional to the applied DC voltage, as is the average load voltage. This "voltage mode" loop comes close to controlling speed because speed is nearly proportional to average winding voltage. If an overall speed feedback loop is required to regulate speed, this "voltage mode" topology can serve as a local feedback loop to make the system transfer function more linear, and the error amplifier can be used as the overall loop amplifier.



Voltage Mode Speed Control



Circuit for Fixed Off-Time PWM Using the UC3625

The advantages of each topology must be weighed considering complexity, overall stability, and sensitivity to load. In cases where current feedback seems nearly impossible to compensate, some compromise between current feedback and voltage feedback is dictated.

The PWM is also configurable to fixed off-time PWM rather than fixed frequency PWM by adding a few external components that couple the output off signal back into the oscillator.

Fixed off-time control is sometimes desirable because it uses one of the easiest feedback loops to compensate. Its main drawback is that the modulation frequency varies with load and speed. This means that for some loads chopping noise can become audible (below 20kHz). This also allows variation in the dead time inserted to prevent output stage cross conduction.

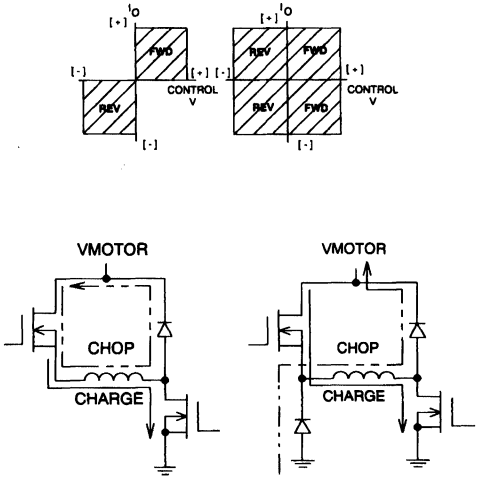
Different Chopping Techniques

Chopping capitalizes on the inductance of the load to maintain load current when the driving voltage is removed. The driving voltage is normally supplied through power switches, and diodes normally conduct across the load when the switches are opened.

Two different methods are common for chopping. The more efficient method chops one low-side power switch while one high-side switch is on. This is referred to as a two-quadrant PWM.

Two-quadrant PWM normally operates with a low duty cycle, as winding current is charged principally by the supply voltage, yet winding inductance is discharged by the voltage drop in the diode circuit (see figure below). Motor back EMF reduces the effective supply voltage and increases the effective diode voltage drop, so the duty cycle tends to increase with speed.

The main advantage of two-quadrant chopping is efficiency. Its main drawback is that it can't quickly decrease winding current. This can be very troublesome in position feedback systems.



Two-Quadrant vs. Four-Quadrant Chopping

In contrast, four-quadrant PWM systems chop both switches, and circulate load current through two diodes backwards into the supply.

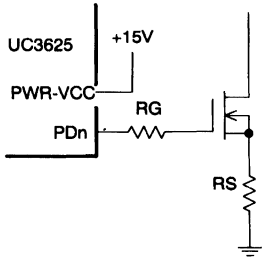
Again ignoring back EMF, four-quadrant chopping produces a nearly symmetrical current waveform, as current rises due to the supply voltage impressed on the load inductance, and decays due to reverse supply and load inductance. With four-quadrant chopping, a motor can decelerate as quickly as it can accelerate.

To program the UC3625 for one approach or the other, apply a logic signal to the QUAD SEL input. QUAD SEL can also be changed during operation to tailor performance to specific requirements.

Power Drivers

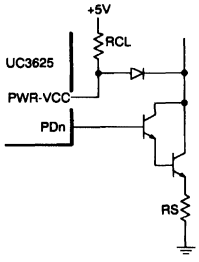
The overwhelmingly dominant power output device in new designs is the N-Channel Enhancement-Mode Power MOSFET. Bipolar power transistors and power darlingtons still have advantages in very high-voltage systems, but these advantages are being continuously eroded by developments in MOSFET structures and merged bipolar MOSFET devices. The UC3625 is able to drive both power MOSFETs and bipolar transistors.

The low-side drivers in the UC3625 are totem-poles capable of greater than 250mA peak gate or base current, but the package and the die are not constructed for continuous power dissipation greater than 1 watt, which imposes an upper limit on the available current for bipolar device drive.



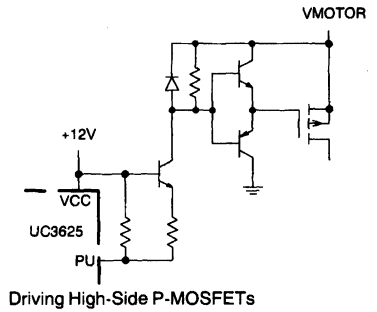
Driving Low-Side MOSFETs with the UC3625

The Power Vcc pin is separated from signal Vcc so that high gate current peaks can be isolated from signal Vcc, and also so that Power Vcc can be tailored to the power device. For fastest switching of power bipolar devices, the Power Vcc pin can be limited and clamped, as shown in this example.

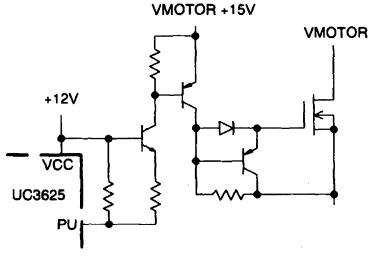


Driving Low-Side Darlingtons with the UC3625

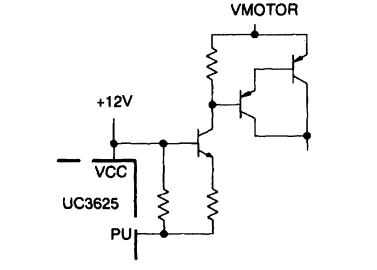
Driving high-side devices with the UC3625 requires level shifting if the motor supply is greater than 50V. The UC3625 high-side outputs are open collector NPN transistors which pull low to turn on high-side MOSFETs or bipolar transistors.



Driving High-Side P-MOSFETs



Driving High-Side N-MOSFETs



Driving High-Side PNP Darlingtons with the UC3625

Although capable of 50mA current sinking, the open collector outputs are normally operated with lower currents to minimize the power supplied by the high-voltage supply.

As a high-side switch, P-channel power MOSFETs are far easier to drive than N-Channel power MOSFETs because the gate of P-channel MOSFETS need not be pulled above the positive supply to obtain low voltage drop. Unfortunately, P-channel power MOSFETs are more expensive and less available than N-channel devices, so the added supply in the N-channel design is often justified.

Current Sense

The UC3625 contains a high-speed gain-of-two differential amplifier dedicated to current sensing. This amplifier can be connected directly across a low-value current-sense resistor or between two different current-sense resistors. Since the amplifier common mode range allows operation one volt below ground, the amplifier has excellent common-mode noise rejection.

The current-sense amplifier also embodies an ideal diode that performs absolute value and level shifting of the input, giving a transfer function of:

$$Vo = 2.5 + 2\ ABS\ (Vi_2 - Vi_1)$$

If the low-side power devices and the lower catch diodes are returned to the same current-sense resistor, and the UC3625 is chopping in four-quadrant mode, then the winding current always flows through the current-sense resistor. The voltage on the current-sense resistor flips polarity every time the PWM chops, but the absolute value current-sense amplifier rectifies this, giving a smoother representation of continuous winding current, and requiring less filtering.

Some filtering of the current-sense signal is always required, however, and the output of the current-sense amplifier is the best place to filter. The amplifier is stable with all capacitive loads, and has approximately 250 ohms output impedance.

Filtering at the input of the current-sense amplifier is also valuable to remove spikes that are faster than the amplifier can track. However, to insure that the absolute value circuit continuously tracks current, use only a minimal amount of input filtering.

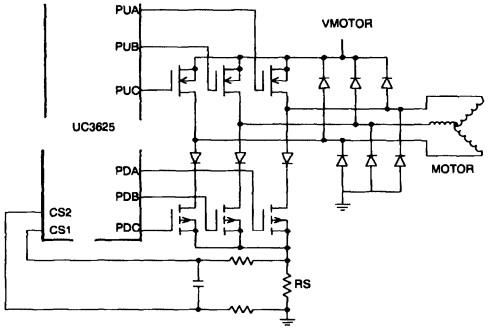
The output of the current amplifier drives two comparators through the filtering resistor: the peak current comparator and the overcurrent comparator. The peak current comparator resets the PWM latch whenever the current-sense voltage exceeds approximately 200mV. The overcurrent comparator initiates soft start if the current-sense voltage exceeds approximately 300mV.

The peak current comparator can be used to limit maximum peak winding current while a larger feedback loop limits winding current to control some other parameter, such as speed or position. The overcurrent comparator then functions as a fail-safe device that commands SOFT START if the peak current loop loses control, as might happen if a power device becomes shorted.

Is it Brake...or Break?

The UC3625 contains provisions for braking by way of a multifunction pin called "RC / BRAKE". This pin also serves as the timing pin for the internal tachometer, pulsing between 1.67V and 3.33V every time the position sensors commutate. To command BRAKE, pull RC/BRAKE low with an open collector gate or switch. The tachometer then stops pulsing and all three low-side drivers turn on.

Normal PWM configurations do not allow braking current to be modulated because the braking current does not normally flow through the sense resistor. The motor control circuit below includes three added diodes that, during BRAKE and all other circumstances causes winding current to flow through the sense resistor. Using this circuit, the UC3625 stops a motor as fast as the peak limit current setting allows and protects the output power devices and the motor.



Circuit For Safe Braking Series diodes guarantee that braking current will flow in the current-sense resistor

Direction Reversal is Worse

As with braking, direction reversal can also force excessive current into power devices if not checked. Direction reversal forces two of the three driver channels to go from high to low or low to high directly. With the UC3625, cross conduction is completely prevented, but high winding current is dependent upon the application. The higher the speed, the higher back EMF, and the higher the potential peak current.

The approach mentioned for braking also limits peak winding current during direction reversal. In addition, the direction latch and shift register in the UC3625 can be configured to prevent direction reversal until motor speed drops to a safe level. This latch also commands COAST whenever a direction reversal is commanded and motor speed is too high.

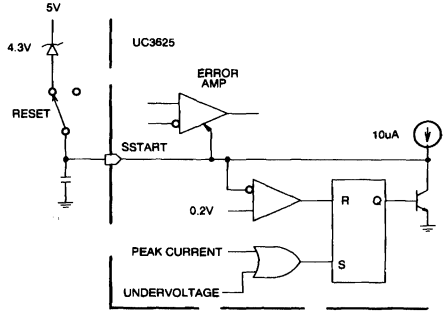
The easiest way to configure this protection is using the internal tachometer to drive "SPEED IN" through a low-pass RC filter. The "SPEED IN" threshold is set to prevent reversal whenever input voltage exceeds approximately 250mV.

Other Protection Features

To prevent confusion or insufficient drive to power MOSFETs, the UC3625 contains a comparator to lock off all six outputs until the Vcc input exceeds 9V, called under-voltage lock-out. The UC3625 also contains an uncommitted comparator that inhibits the outputs and clears the PWM latch whenever its input exceeds 1.75V. This can be used with a voltage divider for an over-voltage inhibit, or can be directly driven from TTL or CMOS for a logic controlled COAST input.

To prevent very high power supply current spikes and to limit average current during faults, the UC3625 contains latched soft start. The latch is set by low power-supply voltage or overcurrent fault, and is only cleared when the setting condition goes away and the soft start input discharges to below approximately 200mV.

Normally, the UC3625 is configured with a capacitor from soft start to ground, which is charged by the soft start 10uA current source. The UC3625 can also be configured to latch soft start until cleared by connecting a 4.3 volt zener and a normally closed switch from Vref to soft start. The switch then functions as a reset switch.



Manual Fault Reset Circuit Uses Zener Diode to Latch Faults

Voltage Reference

Finally, the UC3625 contains a precision voltage reference trimmed to 5V +/- 2%. This reference powers most of the internal circuitry for supply rejection and is available on the "Vref" pin for driving other circuitry such as Hall-effect position sensors and bias circuits. Operation of the voltage reference is guaranteed with loads up to 30mA, and the reference is also short circuit current limited to approximately 100mA.

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APPLICATION NOTE

A SIMPLIFIED APPROACH TO DC MOTOR MODELING FOR DYNAMIC STABILITY ANALYSIS.

By
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When we say that an electric motor is a device that transforms electric power into mechanical power, we say two things. First. that the motor is – and behaves as – a transformer. Second, that it stands at the dividing line between electrical and mechanical phenomena. In the case of permanent magnet (PM) motors we know that this power transformation works in both directions so that the elecrical impedance depends on the mechanical load, while the mechanical behavior of the motor depends on the conditions at the electrical end.

This being the case, it should be possible to represent a motor's mechanical load, on the electrical side, by a set of familiar electrical components such as capacitors or resistors.

CHOOSING A UNIT SYSTEM

Before we get started, let us consider for a moment the system of measurement units that we have chosen.

The metric system of units has undergone a number of changes in its history, of which the latest is the SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is a coherent system, in which the product or quotient of two or more units is the unit of the resulting quantity. It will be seen here that certain simplifications result from using this form of the metric system.

In the SI system, force IS measured in Newtons (N) and distance in meters (m). Consequently, the units of torque are Nm (see Conversion Table). If a motor shaft rotates at an angular velocity of ω_M radians per second, with torque T_M, the mechanical power output will be equal to the product T_M and ω_M and the units will be watts if T_M is in Nm.

Motor manufacturers usually specify a torque constant (K_T) and a voltage constant (K_V) for their motors. These constants have different values when the torque and speed are measured in English units, but they have the same numerical value when SI units are used. This becomes obvious when you consider that the electrical input power must be equal to the mechanical output power:

$$(1)\quad V_A I_A = T_M \omega_M \text{ (watts)}$$

$$(2)\quad \frac{V_A}{\omega_M} = \frac{T_M}{I_A} = K_{TV}$$

where V_A is the internally generated armature voltage, or back emf. and IA IS the armature current. (See Fig. 1 for definition of motor terms.)

TABLE 1. UNITS CONVERSION

THESE UNITS	{ × → = = ← ÷ }	SI UNITS	DIM
oz	2 78 × 10^{-1}	N	MLT^{-2}
lb	4.448	N	MLT^{-2}
in	2 54 × 10^{-2}	m	L
ft	3 048 × 10^{-1}	m	L
gf	9.807 × 10^{-3}	N	MLT^{-2}
g cm^2	10^{-7}	Nm sec^2	ML^2
ft lb sec^2	1.356	Nm sec^2	ML^2
oz in sec^2	7.063 × 10^{-3}	Nm sec^2	ML^2
ft lb	1.356	Nm	ML^2T^{-2}
oz in	7 063 × 10^{-3}	Nm	ML^2T^{-2}

NOTE The dimensions are M (mass) L (length) and T (time) The gram (g) is a unit of mass. and the gram-force (gf) is a unit of force The pound (lb) and the ounce (oz) are included as units of force only

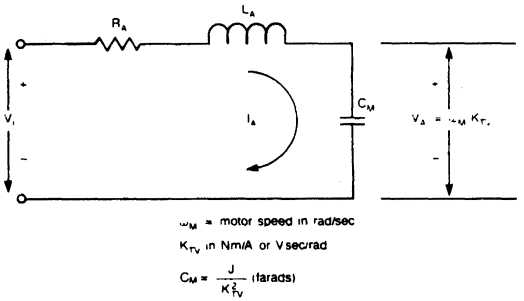

FIGURE 1. THIS SERIES RLC CIRCUIT IS AN EXCELLENT MODEL OF A DC MOTOR LOADED WITH AN ESSENTIALLY INERTIAL LOAD. HERE, J IS THE TOTAL MOMENT OF INERTIA, INCLUDING THE ROTOR'S J_M.

If we do the same thing with the familiar electrical transformer, we get the turns ratio:

$$(3)\quad V_1 I_1 = V_2 I_2 \text{ (watts)}$$

$$(4)\quad \frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Thus. the non-dimensional turns ratio N_1/N_2 is analogous to the dimensional torque (or voltage) constant K_{TV}. Furthermore, equations (2) and (4) give us a clear hint that the angular velocity (ω_M) is analogous to voltage, while the torque (T_M) is analogous to current.

The units of K_{TV} may be either Nm/A. or V sec/rad. Thus, specifying both K_T and K_V for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer, and can only make sense where redundancy is required.

THE MOTOR AS A TRANSFORMER

We have established an analogy between K_{TV} and a transformer's turns ratio; between angular velocity and voltage; and between torque and current. If the motor behaves as a transformer. then we would expect to find the square of K_{TV} involved in something analogous to impedance transformation.

Suppose we apply a constant current I_A to the armature of a motor whose load is its own moment of inertia J_M (Nm sec^2). We know that according to Newton's law for rotating objects,

(5) $T_M = J_M \alpha_M$

where α_M is the angular acceleration $d\omega_M/dt$.

Since $T_M = I_A K_{TV}$ (Eq. 2)

(6) $$I_A K_{TV} = J_M \frac{d\omega_M}{dt}$$

Furthermore. also from Eq. 2,

(7) $$\omega_M = \frac{V_A}{K_{TV}}$$

so that

(8) $$I_A = \frac{J_M}{K_{TV}^2} \cdot \frac{dV_A}{dt}$$

Equation 6 has a familiar form, and we recognize at once the quantity J_M/K_{TV}^2 as a capacitor. It follows that the motor "reflects" a moment of inertia J_M back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

A neat way to check this result is to equate the energy stored kinetically in J_M with the electrical energy stored in a capacitor C_M:

(9) $$\tfrac{1}{2} C_M V_A^2 = \tfrac{1}{2} J_M \omega_M^2$$

(10) $$C_M = J_M \left(\frac{\omega_M}{V_A}\right)^2$$

Since $$\frac{\omega_M}{V_A} = \frac{1}{K_{TV}},$$

(11) $$C_M = \frac{J_M}{K_{TV}^2} \text{ (farads)}$$

Similarly, a torsional spring with spring constant K_S (Nm/rad) is reflected as an inductance of K_{TV}^2/K_S henries. And a viscous damping component B (Nm sec/rad) appears as a resistor of K_{TV}^2/B ohms.

A MOTOR MODEL

Once we can represent the mechanical load by means of electric elements, we can draw an equivalent circurt of the motor and its mechanical load. The armature has a finite resistance R_A and an inductance L_A, through which the torque-generating current I_A must flow. These components are not negligible. and must be included. An inertially loaded motor can be represented as in Fig. 1, where the moment of inertia J is the sum of the load's J_L and the rotor's J_M.

It turns out that in practice. the moment of inertra that the motor must work against - or with, depending on how you look at it – is by far the most important component of the mechanical load. A frictional component also exists, to be sure, but because it is largely independent of speed, it would be represented electrically as a constant current source, which could not affect the dynamic behavior of the motor. And since a torsional spring – which would affect it – is rarely found in practice, we Will concentrate on the inertial problem only.

MEASURING THE COMPONENTS

The measurement of R_A and L_A is not difficult. A good ohmmeter will get you R_A, and you can measure the electrical time constant τ_E to calculate L_A:

(12) $L_A = \tau_E R_A$

Just make sure that the rotor remains stationary during these measurements.

In order to determine the value of the capacitor. C_M. we will need to measure the shaft speed. If the motor being measured is a brushless DC motor, we can use the signal from one of the Hall effect devices as a tachometer. If the Hall frequency is f_H, and the number of rotor poles is P. the angular velocity ω_M is

(13) $$\omega_M = \frac{4\pi f_H}{P} \text{ (rad/sec)}$$

With other motors you will need a strobe-light or some other means to measure speed.

A good way to measure C_M is through a measurement of the mechanical time constant T_M. We do this by driving the motor with a constant voltage driver and measuring the time it takes to accelerate from zero speed to 63% of the highest speed achievable at the voltage used. To set a safe limit to the starting current we can reduce the supply voltage or add a serves resistor with the motor, or both. The set-up is shown in Fig. 2. Note that the armature resistance R_A is already known, and we add resistors R_B. If needed, to limit the armature current I_A to a value that is safe for both driver and motor.

The first thing to do is let the motor run freely and measure ω_{MAX} and I_{MAX}, and use these values to calculate the armature voltage V_{MAX}:

(14) $V_{MAX} = V_{CC} - V_{SAT} - I_{MAX} (R_A + R_B)$

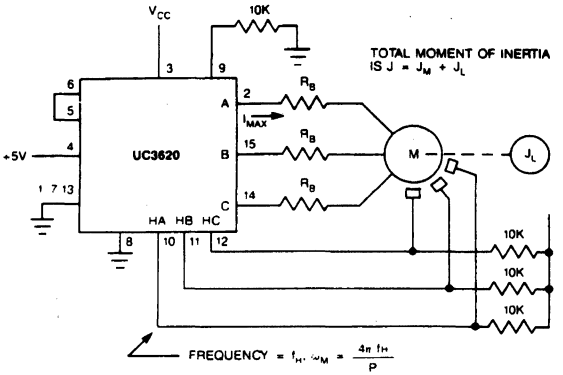

FIGURE 2. SET-UP FOR MEASUREMENT OF $C_M = J/K_{TV}$ OF A 3-PHASE BRUSHLESS DC MOTOR WITH INERTIAL LOAD J1. THE MOTOR VOLTAGE $V_M = V_{CC} \cdot V_{SAT}$, WHERE V_{SAT} IS THE OUTPUT SATURATION VOLTAGE.

Here V_{CC} is the supply voltage, V_{SAT} is the saturation voltage of the driving circuit, and I_{MAX} is the current drawn by the unloaded motor at maximum speed.

Thus we can calculate

$$(15)\quad K_{TV} = \frac{V_{MAX}}{\omega_{MAX}} \quad \text{(Vsec/rad)}$$

Next, set the oscilloscope time scale to that you can easily read a Hall frequency equal to 63% of ω_{MAX}, so that:

$$(16)\quad \omega_M = 0.63\ \omega_{MAX}$$

By holding and releasing the motor shaft, take several readings of the time T_M required to accelerate from zero to ω_M. Remember that these readings are taken "on the fly," since the motor continues to accelerate towards the maximum speed ω_{MAX}. Having obtained a good value of T_M you can now calculate

$$(17)\quad C_M = \frac{T_M}{(R_A + R_B)} \quad \text{(farads)}$$

This completes the RLC equivalent circuit, If the value of J_M is also required, it too can be calculated:

$$(18)\quad J_M = C_M K_{TV}^2$$

THE MOTOR'S TRANSFER-FUNCTION

In the circuit of Fig. 1, V_1 is the voltage applied to the motor leads. and V_A is the actual armature voltage, or back EMF. This latter voltage is equal to $\omega_M K_{TV}$, as we have seen, so that if we want to derive an expression relating the speed to the applied voltage, we can write:

$$(19)\quad \frac{\omega_M}{V_1} = \frac{1}{K_{TV}} \cdot \frac{V_A}{V_1} \quad \text{(rad/Vsec)}$$

If V_1 is a constant voltage, the speed ω_M will also be constant. This is clear from the circuit of Fig. 1 as well as from our experience with motors. If, however, V_1 varies sinusoidaly at some frequency f, the speed ω_M will vary similarly, but the amplitude and phase will in general be different from those of the driving function. This fact is very important if we are to include the motor in a feedback loop, because the motor's contribution to the overall loop gain and phase shift is an important factor in determining stability. The motor's transfer function – i.e. Eq. 19 expressed as a function of frequency – gives us a precise description of how the amplitude and phase behave at different frequencies. To do this, we use the variable $j\omega$, where $j = \sqrt{-1}$, and $\omega = 2\pi f$.

$$(20)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{(j\omega C_m)^{-1}}{j\omega^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(21)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{(j\omega)^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(22)\quad L_A C_M = \frac{1}{\omega_n^2}$$

where ω_n is the natural frequency of the circuit.

$$(23)\quad R_A C_M = \frac{R_A C_M L_A}{L_A} = \frac{R_A}{\omega_n^2 L_A} = \frac{1}{Q\omega_n}$$

since the circuit Q is

$$Q = \frac{\omega_n L_A}{R_A}$$

Therefore,

$$(24)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Furthermore, using Eq. 19,

$$(25)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} = \left(\frac{1}{K_{TV}}\right) \cdot \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Since we know the values of K_{TV}, ω_n and Q, we can calculate the magnitude and phase angle of Eq. 25 for various values of $j\omega$. For a given $\omega = \omega_1$, Eq. 25 can be evaluated into a complex number $A_1 + jB_1$, whose angle is,

$$(26)\quad \theta_1 = \tan^{-1}\frac{B_1}{A_1}$$

and whose magnitude can be expressed in decibels as follows:

$$(27)\quad M_1 = 20 \log_{10} \sqrt{A_1^2 + B_1^2}$$

A plot of these quantities. using a logarithmic frequency scale, is called a Bode plot, and can be a handy tool in understanding how the device Will affect the final loop performance.

A DISC - DRIVE EXAMPLE

A small three phase brushless DC motor, measured as above, has the following characteristics:

K_{TV} = 0.015 Nm/A, or Vsec/rad.
R_A = 2.5 ohm
L_A = 0.002 Hy
J = 0.001 Nm sec_2

The J value was measured with three magnetic discs mounted, and represents the actual value required for the application. Using Eq. 11.

$$(28)\quad C_M = \frac{J}{K_{TV}^2} = \frac{.001}{(0.015)^2} = 4.44 \text{ fd}$$

This may seem like an unusually large value for a capacitor, but it simply reflects the large amounts of kinetic energy that can be stored in the included inertia.

From Eq. 22

$$(29)\quad \omega_n = \frac{1}{\sqrt{L_A C_M}} = \frac{1}{\sqrt{0.002 \times 4.44}}$$

$$= 10.61 \text{ rad/sec}$$

From Eq. 23

$$(30)\quad Q = \frac{\omega_n L_A}{R_A} = \frac{10.61 \times 0.002}{2.5} = 0.0085$$

(The quality factor Q has no units). The motor transfer function, given in Eq. 25, is

$$(31)\quad \frac{\omega_M (j\omega)}{V_1 (j\omega)} = \frac{66.67}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1} \text{ (rad/Vsec)}$$

A calculator that is pre-programed to operate with complex numbers (HP 28C, for example, or 15C) makes the evaluation, of this equation an easy task. With the 28C you can set up a USER routine called BODE, as follows:

<<DEG DUP ABS LOG 20 X SWAP ARG>>

This will convert a complex number x + jy into 20 log $\sqrt{x^2+y^2}$ at level 2, and arc tan (y/x) at level 1. Table 2 shows a list of several such computations of Eq. 31:

At ω = 0, the gain is simply 66.67 rad/Vsec. As ω increases from zero up, the gain decreases as shown in the GAIN column of Table 2. For our Bode plot, we want to show the gain relative to the Initial, or DC, gain. Therefore, we subtract 66.67db from each gain value in Table 2 and plot the result. This is the same as plotting only the function

$$(32)\quad G(j\omega) = \frac{1}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1}$$

which should be compared with Eq. 31. The results are shown in Fig. 3.

TABLE 2. CALCULATED VALUES OF EQUATION 31.

ω (rad/sec)	$\frac{\omega_M (j\omega)}{V_1 (j\omega)}$	GAIN (db)	PHASE (deg)
0.01	65.9 - j 7.32	36.4	-6.3
0.03	60 - j 20	36.0	-18.4
0.1	29.8 - j 33.2	33.0	-48.0
0.3	5.5 - j18.4	25.7	-73.3
1.0	0.53 - j 5.95	15.5	-84.9
3.0	0.06 - j 2.00	6.0	-88.4
10.0	0 - j 0.60	-4.4	-89.9
30.0	-4.2×10^{-3} - j 0.20	-14.0	-91.2
100	-4.7×10^{-3} - j 0.06	-24.5	-94.5
300	-4.5×10^{-3} - j 0.02	-34.2	-103.5
1000	-2.9×10^{-3} - j 3.7×10^{-3}	-46.6	-128.6
3000	-7.1×10^{-3} - j 3×10^{-4}	-62.3	-157.4

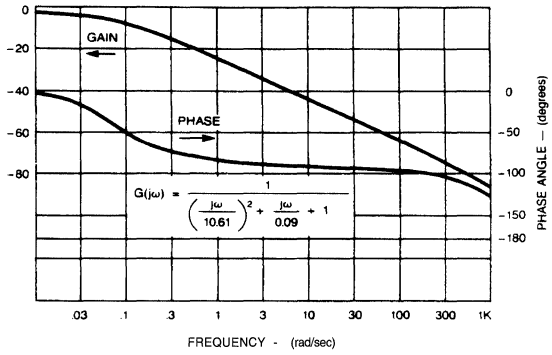

FIGURE 3. BODE PLOT OF MOTOR DATA IN EXAMPLE.

Note that up to about 100 rad/sec (15.9 Hz) the phase lag barely exceeds 90 degrees. The first pole occurs at ω = 0.09 rad/sec, at which point the phase lag is 45 degrees. The second pole, widely separated from the first in this case, occurs at a frequency in excess of 1000 rad/sec, as we can see from the further bend in the phase curve. The gain, which was drooping at a rate of -20db per decade below 100 rad/sec, now begins to bend towards a steeper droop of 40db/dec after the second pole is reached. At very high frequencies, the phase lag will reach 180 degrees.

Used in a speed control feedback loop, this motor will perform well provided that the user takes this gain and phase behavior into account. This is done by incorporating the motor transfer function into the overall loop equation, which will include other components. One's understanding of the motor's behavior improves with this type of analysis, which makes comparisons between different motors more clear and articulate.

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DEDICATED ICs SIMPLIFY BRUSHLESS DC SERVO AMPLIFIER DESIGN

John A. O'Connor

INTRODUCTION

Brushless DC motors have gained considerable commercial success in high end four quadrant servo systems, as well as in less demanding, one and two quadrant requirements. Cost sensitive four quadrant applications thus far have not fared as well. Designs which meet cost goals often suffer from poor linearity, and cumbersome protection circuits to assure reliable operation in all four quadrants. Better performance en tails more complex circuitry and the resulting additional components quickly increase size and cost. Part of the design challenge results from the lack of control ICs tailored to four quadrant applications. The other major obstacle has been implementing a reliable and cost effective high-side switch drive. With recently introduced integrated circuits in both areas, it is now possible to design a rugged, low cost, four quadrant brushless DC servo amplifier with relatively low component count and cost.

SERVO AMPLIFIER REQUIREMENTS

First, let's quickly review general servo amplifier requirements. Figure 1 displays motor speed versus torque, depicting four possible modes of operation. While a system may be considered four quadrant by simply having the ability to operate reliably in all four modes, a servo system generally requires *controlled* operation in

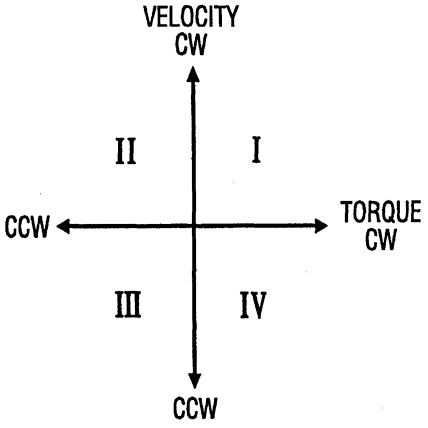


Figure 1 - Four Quadrants of Operation

all four modes. In addition, a smooth, linear transition between quadrants is essential for high accuracy position and velocity control. The major performance differences between brushless DC servo amplifiers are related to accuracy, bandwidth, and quadrant transition linearity.

Most simple brushless DC amplifiers provide two quadrant control, since even the simplest output stages (typically 3 phase bridge) allow rotation reversal. Note that this is operation in quadrants one and three where torque and rotation are in the same direction. This differs from brush motor terminology where two quadrant control normally implies unidirectional rotation with torque control in either direction. Although limited to a single rotation direction, bidirectional torque allows servo velocity control, with rapid, controlled acceleration and deceleration. These characteristics are well suited to numerous applications such as spindle and conveyer drives. With the two quadrant brushless DC amplifier, there are no provisions other than friction to decelerate the load, limiting the system to less demanding applications. Attempting to operate in quadrants two and four will result in extremely nonlinear behavior, and under many circumstances, severe damage to the output stage will follow. This occurs because the two quadrant brushless DC amplifier is unable to completely control current during torque reversal.

TWO QUADRANT VERSUS FOUR QUADRANT CONTROL

Figure 2 shows a three phase bridge output stage for driving a brushless DC motor. Current flow is shown for two quadrant control when operation is in quadrants one or three. The switches commutate based on the motor's

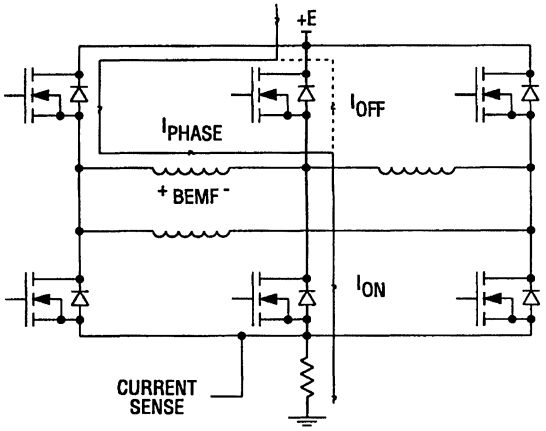


Figure 2 - Two Quadrant Chopping

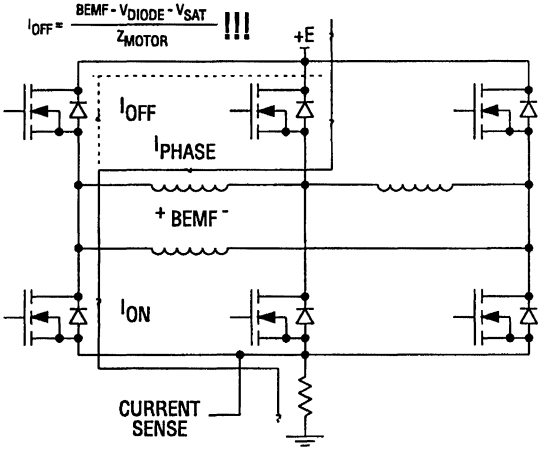


Figure 3 - Two Quadrant Reversal

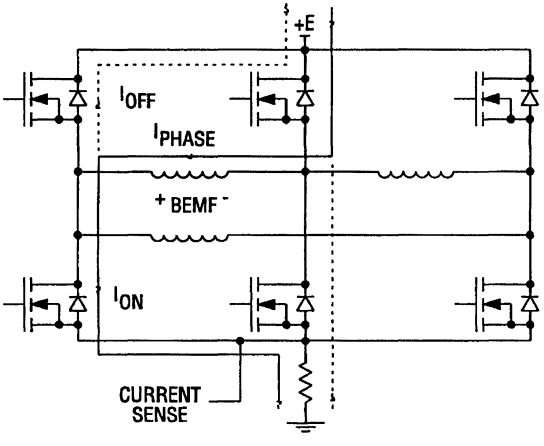


Figure 4 - Four Quadrant Reversal

rotor position, typically using Hall effect sensors for position feedback. Current is controlled by pulse width modulating (PWM) the lower switches. Figure 3 shows current flow if the direction of torque were reversed. The upper switch essentially shorts the motor's back EMF (BEMF), causing current to quickly decay and reverse direction. The current then rises to a value limited only by the motor and drive impedance, yet is undetected by supply or ground sense resistors. As the motor speed rises, its BEMF proportionally increases, quickly escalating the potential circulating current. Even if the output stage is built rugged enough to withstand this abuse, the high uncontrolled current causes high uncontrolled torque, making this technique unsuitable for most servo control applications.

By pulse width modulating the upper switches along with the lower switches, uncontrolled circulating currents are avoided. With both upper and lower switches off during during the PWM off time, motor current will always decay as shown in figure 4. Additionally, motor current always flows through the ground sense resistor, allowing easy detection for feedback. The remainder of this article will feature this mode of control, as it is well suited for a variety of demanding requirements. It should be noted however, that a penalty in the form of reduced efficiency must be paid for the improvement in control characteristics. With two switches operating at the PWM frequency, as opposed to one with two quadrant control, switching losses are nearly doubled. Ripple current is also increased which results in greater motor core loss. Although this is a small price to pay under most circumstances, extremely demanding applications may require switching between two and four quadrant operation for optimum efficiency and control.

FOUR QUADRANT CONTROLLER REQUIREMENTS

In addition to switching both upper and lower transistors, a few supplementary functions are required from the control circuit for reliable four quadrant operation. With two quadrant switching, there is inherent dead time between conduction of opposing upper and lower switches, making cross conduction virtually impossible. Four quadrant control immediately reverses the state of opposing switches at torque reversal, thus requiring a delay between turning the conducting device off and the opposing device on to avoid simultaneous conduction and possible output stage damage.

When torque is reversed, energy stored in the rotating load is transferred back to the power supply, quickly charging the bus storage capacitor. A clamp circuit is

typically used to dissipate the energy and limit the maximum bus voltage. As a second line of defense, an over-voltage comparator is often employed to disable the output if the bus voltage exceeds the clamp voltage by more than a few volts.

CURRENT LOOP CONTROL TECHNIQUE

A transconductance amplifier is normally used for brushless DC servo applications, providing direct control of motor torque. Average current feedback is usually employed rather than the more familiar peak current

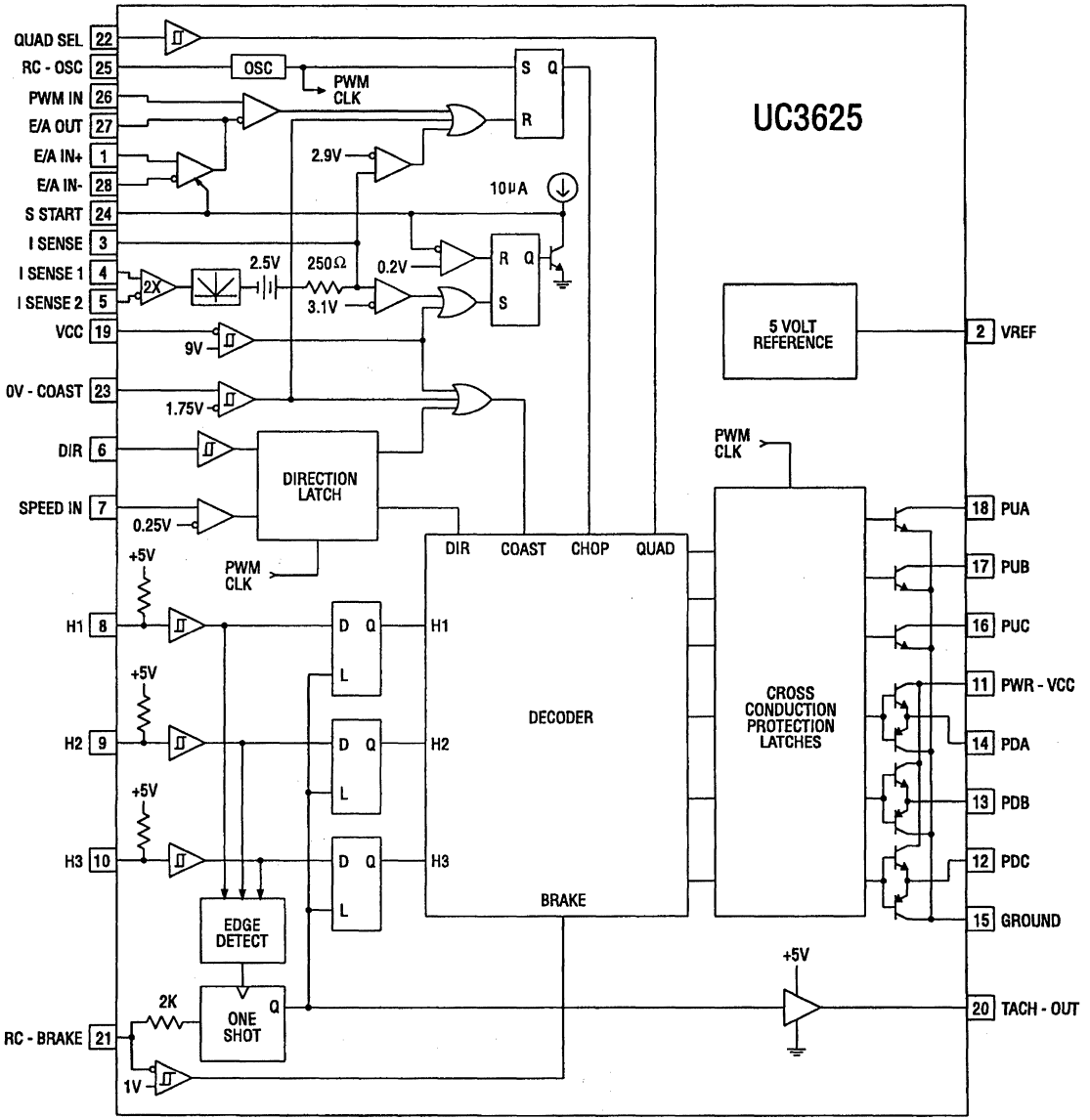


Figure 5 - UC3625 Block Diagram

control for several reasons. Peak current control is subject to subharmonic oscillation at the switching frequency for duty cycles above 50%. This condition is easily circumvented in power supply applications by summing an appropriately scaled ramp signal derived from the PWM oscillator with the current sense signal. This technique is commonly refered to as slope compensation. It can also be shown [3] that for a given inductor current decay rate, which is essentially fixed in a power supply application, there is an optimal compensation level which will produce an output current independent of duty cycle. Unfortunately, the inductor current decay rate in a four quadrant motor control system varies with both speed and supply voltage, making an optimal slope compensation circuit fairly complex. Simpler circuits which provide overcompensation assure stability but will degrade accuracy. Furthermore, severe gain degradation occurs when inductor current becomes discontinuous regardless of slope compensation, causing large nonlinearity at light load. This effect can be particularly troublesome for a position control servo. Average current feedback avoids these problems, and is therefore the preferred current control technique for servo applications.

UC3625 BRUSHLESS DC CONTROLLER

Figure 5 shows the UC3625 block diagram. Designed specifically for four quadrant operation, it minimizes the external circuitry required to implement a brushless DC servo amplifier. Flexible architecture and supplementary features make the UC3625 well suited to less demanding applications as well. The UC3625 is described in detail in references [4] and [7], however a few features critical for reliable four quadrant operation should be noted.

Cross conduction protection latches eliminate the possibility of simultaneous conduction of upper and lower switches due to driver and switch turn-off delays. Additional analog delay circuits normally associated with this function are eliminated allowing direct switch interface and reduced component count. An absolute value buffer following the current sense amplifier provides an average winding current signal suitable for feedback as well as protection. An over-voltage comparator disables the outputs if the bus voltage becomes excessive.

Although not absolutely necessary for four quadrant systems, a few additional features enhance two quadrant operation and simplify implementation of switched two / four quadrant control for optimized systems. A direction latch with analog speed input prevents reversal until an acceptably low speed is reached, preventing output stage damage. Two or four quadrant switching can be selected during operation with the Quad Select input. A brake input provides current limited dynamic braking, suitable for applications which require rapid deceleration, but do not need tight servo control.

A SIMPLE BRUSHLESS DC SERVO AMPLIFIER

To demonstrate the relative simplicity with which a brushless DC servo amplifier can be implemented, a 6 amp, off-line 115 VAC amplifier was designed and constructed. Note that current and voltage rather than horsepower are specified. Although theoretically capable of in excess of one horsepower, simultaneous high speed and torque are typically not required in servo applications, reducing the actual output power, and the corresponding power supply requirement. Average current feedback is employed, providing good bandwidth and power supply rejection, thus making the amplifier suitable for many demanding requirements. A complete amplifier schematic is shown in figure 6.

A high performance brushless servo motor from MFM Technology, Inc. was used to evaluate the amplifier. While most of the design is independent of motor parameters, several functions should be optimized for a particular motor and operating conditions. The motor used has the following electrical specifications:

Model M - 178

K_T	79 oz.in./Amp
R_M	1.3 ohms
L_M	5.5 mH
Poles	18

OUTPUT STAGE DESIGN

Having selected a four quadrant control strategy, we proceed to the output stage design, and work back to the controller. High voltage MOSFETs are well suited to this power level, however IGBTs may also be incorporated. MOSFETs were selected to minimize size and complexity, since the body diodes can be used for the flyback rectifiers. Unfortunately, this places greater demands on the MOSFET, and increases the device dissipation. The MOSFETs body diode is typically slower and stores more charge than a discrete high speed rectifier, which necessitates a slower turn-on and a corresponding increase in switching losses. These losses are partially offset by choosing a MOSFET with sufficiently low conduction losses which offers the secondary benefits of greater peak current capability and reduced thermal

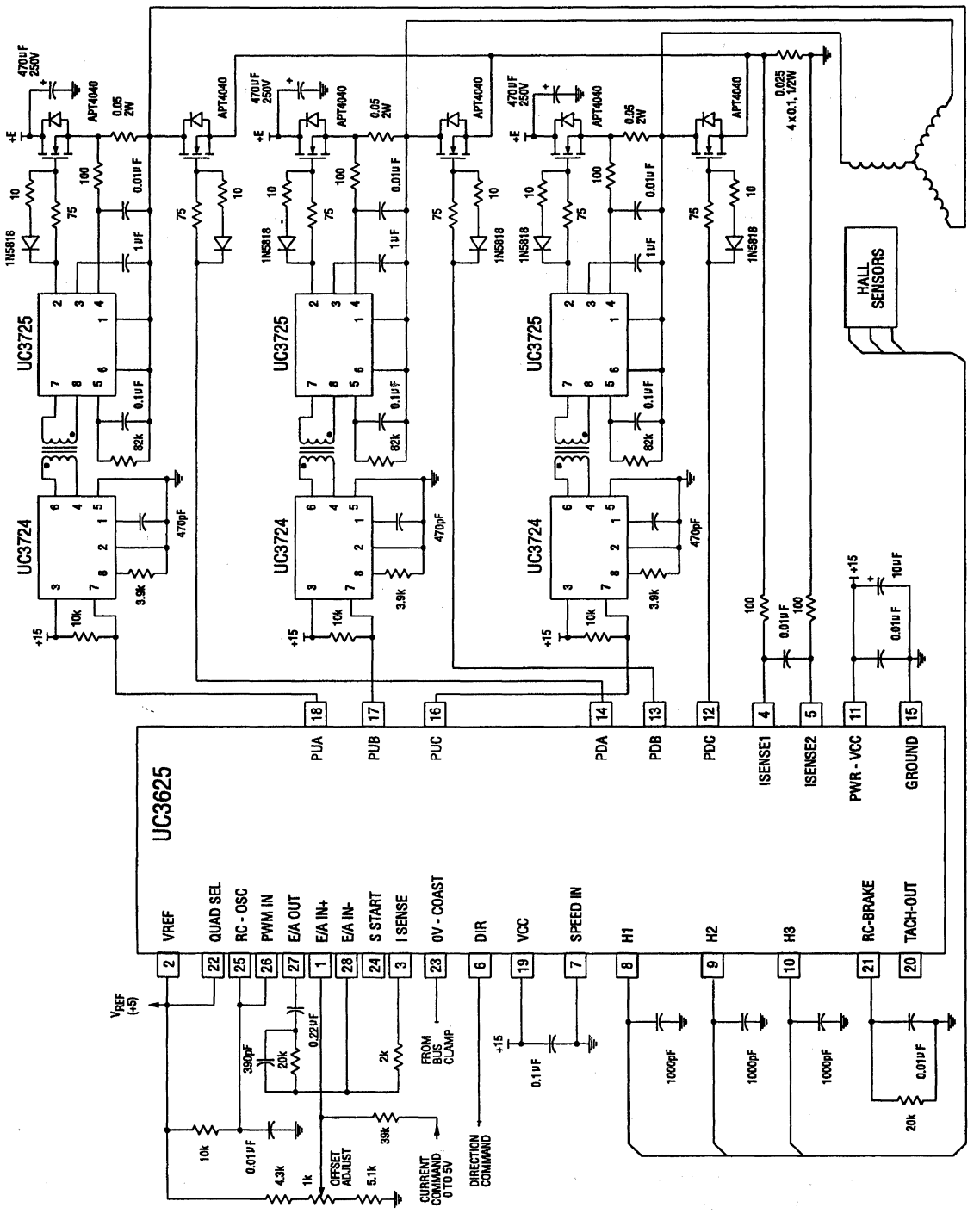


Figure 6 - Brushless DC Servo Amplifier Schematic

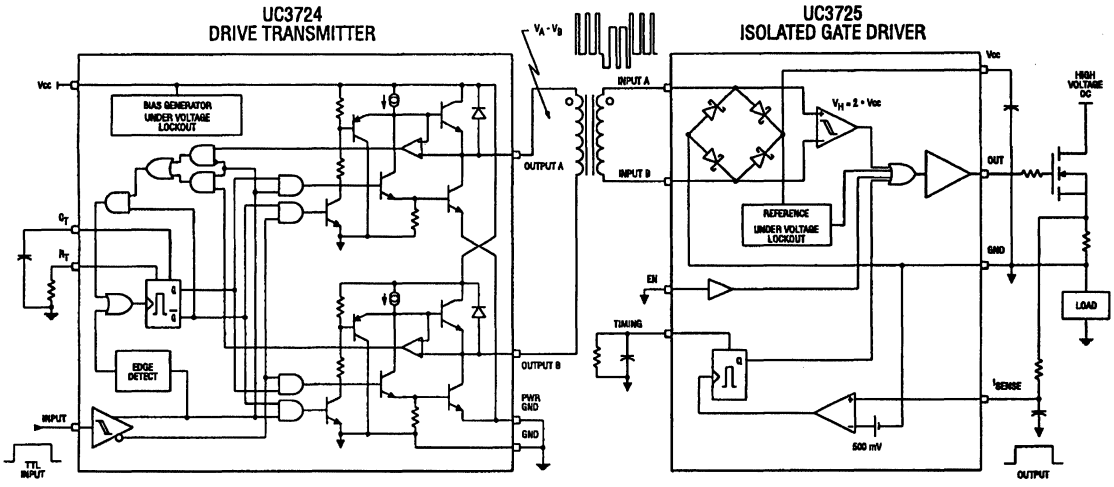


Figure 7 - UC3724/UC3725 Isolated MOSFET Driver

resistance. APT4030BN MOSFETs were selected for the output stage to handle the 6 amp load currents while providing good supply voltage transient immunity. Rated at 400 volts and 0.30 ohms, they allow high efficiency operation and have sufficient breakdown voltage for reliable off-line operation.

While the lower three FETs require simple ground referenced drive, and are easily driven directly from the UC3625 the design of the drive circuit for the upper three FETs has traditionally been challenging. Discrete implementation of the required power supply and signal transmission is often bulky and expensive. In an effort to reduce size and cost, critical functions are often omitted, opening the door to potential reliability problems. Specifically designed for high-side MOSFET drive in motor control systems, the UC3724 / UC3725 IC pair shown in figure 7, offers a compact, low cost solution. A high frequency carrier transmits both power and signal across a single pulse transformer, eliminating separate DC/DC converters, charge pump circuits, and opto-couplers. Signal and power transmission function down to DC, imposing no duty cycle or on-time limitations typical of commonly used charge pump techniques. Under-voltage lockout, gate voltage clamp, and over current protection assure reliable operation.

Design of the upper driver is a straight forward procedure, and is described in detail in reference [5].
For this application, the driver is designed with the following specifications:

500 V minimum isolation
300 kHz carrier frequency
10 Amp over-current fault
10 ms over-current off time

The pulse transformer uses a 1/2 inch O.D. toroid core (Philips 204T250-3E2A) with a 15 turn primary and 17 turn secondary. For high voltage isolation, Teflon insulated wire is used for both primary and secondary.

To provide rapid turn-off for minimal switching losses, with slower turn-on for di/dt control, a resistor/resistor-diode network is used in place of a single gate resistor. Although present generation MOSFETs can reliably commutate current from an opposing FETs body diode at high di/dt, the resulting high peak current and diode snap limit practical circuits to a more moderate rate. This increases dissipation, but significantly eases RFI filtering and shielding, as well as relaxing layout constraints. Additionally, a low impedance is maintained in the off state while turn-on dv/dt is decreased, dramatically reducing the tendency for dv/dt induced turn on. The same gate network is used for both upper and lower MOSFETs.

A sense resistor in series with the bridge ground return provides a current signal for both feedback and current limiting. This resistor, as well as the upper driver current sense resistors should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impossible to eliminate, careful

layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values, and serve double duty as the half-bridge bypass capacitors.

CONTROLLER SETUP

The UC3625 switching frequency is programmed with a timing resistor and capacitor. Unless the motor's inductance is particularly low, 20 kHz will provide acceptable ripple current and switching losses while minimizing audible noise.

(1) $F = 2 / R_{osc}C_{osc}$

The relatively small oscillator signal amplitude requires careful timing capacitor interconnect for maximum frequency stability. Circuit board traces should to be as short as possible, directly connecting the capacitor between pins 25 and 15, with no other circuits sharing the board trace to pin 15 (ground).

When tight oscillator stability is required, or multiple systems must be synchronized to a master clock, the circuit shown in figure 8 can be used. As shown, the circuit buffers, and then differentiates the falling edge of the master oscillator. The last stage provides the necessary current gain to drive the 47 ohm resistor in series with the timing capacitor. If the master clock is from a digital source, the first two stages are omitted, and the clock signal is interfaced directly to the final stage through a restive divider as shown. The slaves are programmed to oscillate at a lower frequency than the master. The pulse injected across the 47 ohm resistor causes the oscillator to terminate its cycle prematurely, and thus synchronize to the master clock.

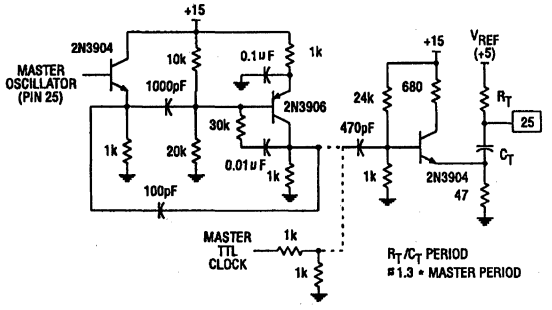
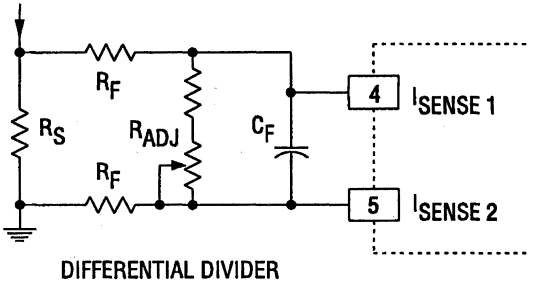
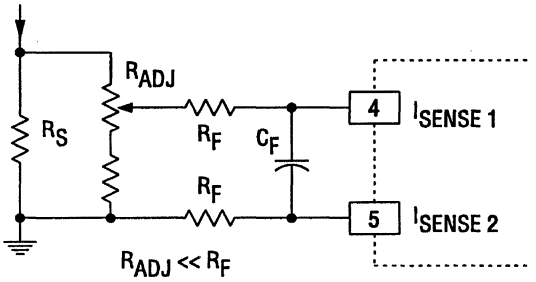


Figure 8 - External Synchronization Circuit



DIFFERENTIAL DIVIDER



LOW VALUE DIVIDER

Figure 9 - Balance Impedance Current Sense Input Circuits

The RC-Brake pin serves two functions: Brake command input (not used in this design), and tachometer / digital commutation filter one-shot programming. Whenever the commutation state changes, the one-shot is triggered, outputting a tach pulse and inhibiting another commutation state change until the one-shot terminates. The one-shot pulse width is programmed for approximately 1/2 the shortest commutation period.

(2) $T_{PW} = 0.70\ R_TC_T$

where the shortest commutation period = $20 / (RPM_{MAX}N_{POLES})$

CURRENT SENSING AND FEEDBACK

For optimum current sense amplifier performance, the input impedance must be balanced. Low value resistors (100 to 500 ohm) are used to minimize bias current errors and noise sensitivity. Additionally, if the sense voltage must be trimmed, a low value input divider or a differential divider should be used to maintain impedance matching, as shown in figure 9.

An average current feedback loop is implemented by the circuit shown in figure 10. With four quadrant chopping, motor current always flows through the sense resistor. When PWM is off however, the flyback diodes conduct,

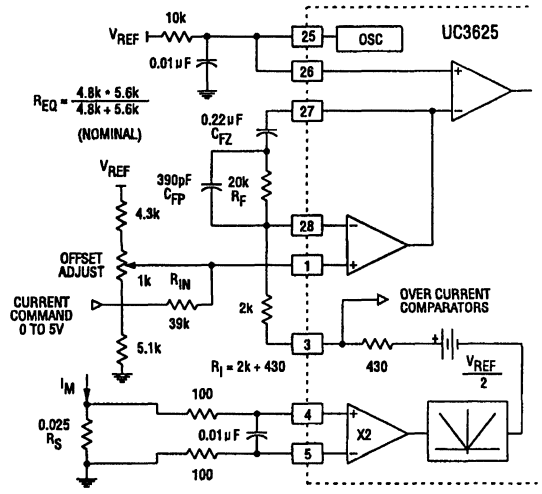


Figure 10 - Average Current Feedback Circuit Configuration

causing the current to reverse polarity through the sense resistor. The absolute value amplifier cancels the current polarity reversal by inverting the negative current sense signal during the flyback period. The output of the absolute value amplifier therefore is a reconstructed analog of the motor current, suitable for protection as well as feedback loop closure.

When the current sense output is used to drive a summing resistor as in this application example, the current sense output impedance adds to the summing resistor value. The internal output resistor and the amplifier output impedance can both significantly effect current sense accuracy if the external resistance is too low. Although not specified, the total output impedance is typically 430 ohms at 25 degrees C. Over the military temperature range of -55 to +125 degrees C, the impedance ranges from approximately 350 to 600 ohms. An external 2 k resistor will result in an actual 2.43 k summing resistance with reasonable tolerance. A higher value external resistor and trim pot will be required if high closed current loop accuracy is required.

The current sense output offset voltage is derived from the +5 V reference voltage. By developing the command offset from the +5 V reference, current sense drift over temperature is minimized. The offset divider must be trimmed initially to accommodate the current sense amplifier offset tolerance.

POWER SUPPLY AND BUS CLAMP

Input power is filtered to reduce conducted EMI, and transient protected using MOVs. Power-up current surge is suppressed using a NTC thermistor, while a bridge rectifier and capacitive filter complete the high voltage supply. A small 60 Hz. transformer supplies 15 Volts through a three pin regulator to power the control and drive circuits.

A bus clamp is easily designed around a UC3725 MOSFET driver, as shown in figure 11. As in the high-side switch drive, the UC3725 assures reliable operation, particularly during power-up and power-down. The divider current is set to 1 mA at the threshold, which is a reasonable compromise between input bias current error and dissipation. An additional tap programs the over-voltage coast a few volts above the bus clamp, saving a resistor and some dissipation while reducing the tolerance between the bus clamp and the over-voltage coast. Setting the bus clamp discharge current equivalent to the maximum motor current will assure effective clamping under all conditions. The load resistor value is therefore:

$$(3) \qquad R_L = \frac{V_{CLAMP}}{I_{MAX}}$$

The load resistor dissipation is dependant on the energy removed from the load inertia, and the frequency with which the energy is removed.

$$(4) \qquad P_{LOAD} = 1/2\, fJ\, (\omega_1^2 - \omega_2^2)$$

where J = inertia in Nm sec²
ω_1 = initial velocity in rad/sec
ω_2 = final velocity in rad/sec

Note that if the deceleration time approaches the load resistor's thermal time constant, a higher power resistor will be required to maintain reliability.

CURRENT LOOP OPTIMIZATION

The block diagram of the current control loop is shown in figure 12. The current sense input filter has minimal affect on the loop and can be ignored, since the filter pole must be much higher than the system bandwidth to maintain waveform integrity for over-current protection. The current sense resistor R_S, is chosen to establish the peak current limit threshold, which is typically set 20% higher than the maximum current command level to provide over-current protection during abnormal conditions. Under normal circumstances with a properly compensated current loop, peak current limit will not be exercised. The input divider network provides both offset adjustment and attenuation, with R_{IN} selected to accomodate the current command signal range.

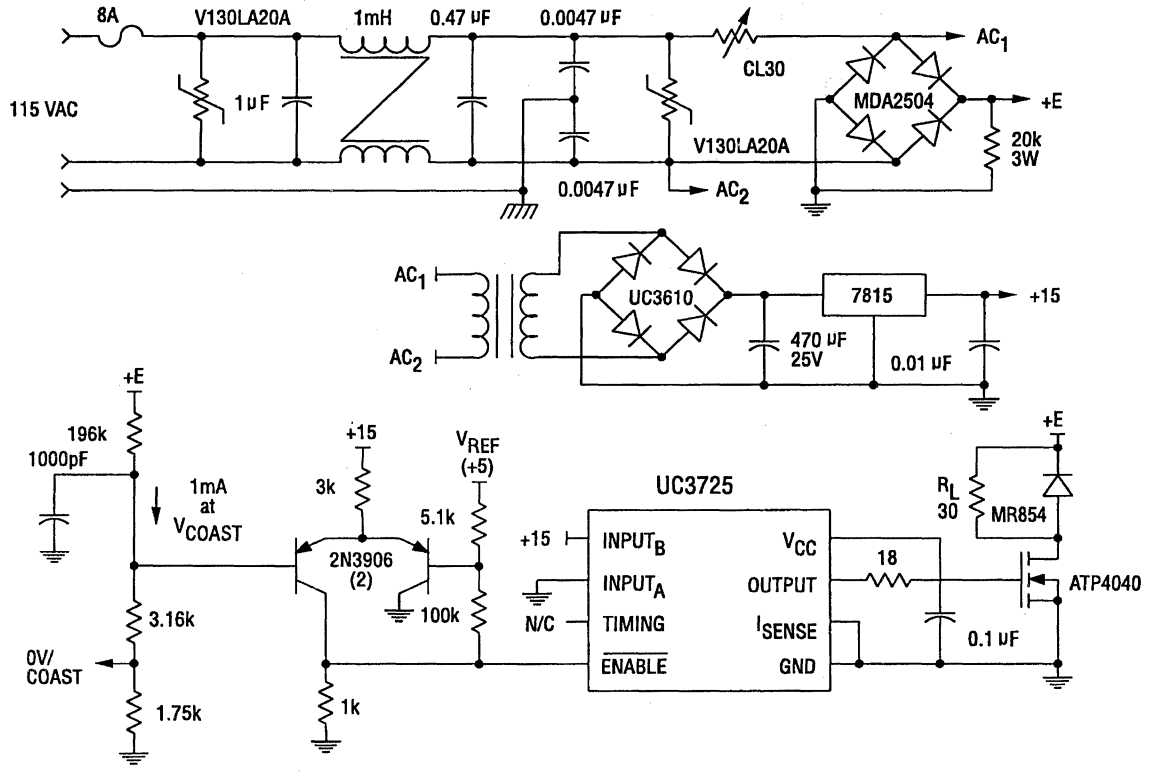


Figure 11 - Power Supply and Bus Clamp

All PWM circuits are prone to subharmonic oscillation if the modulation comparator's two input waveform slopes are inappropriately related. This behavior is most common in peak current feedback schemes, where slope compensation is typically required to achieve stability. Average current feedback systems will exhibit similar behavior if the current amplifier gain is excessively high at the switching frequency. As described by Dixon [2] to avoid subharmonic oscillation for a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion sets the maximum current amplifier gain at the switching frequency, and indirectly establishes the maximum current loop gain crossover frequency.

A voltage proportional to motor current, which is the inductor current, is generated by the current sense resistor and the current sense amplifier circuitry internal to the UC3625 This waveform is amplified and inverted by the current amplifier and applied to the PWM comparator input. Due to the signal inversion, the motor

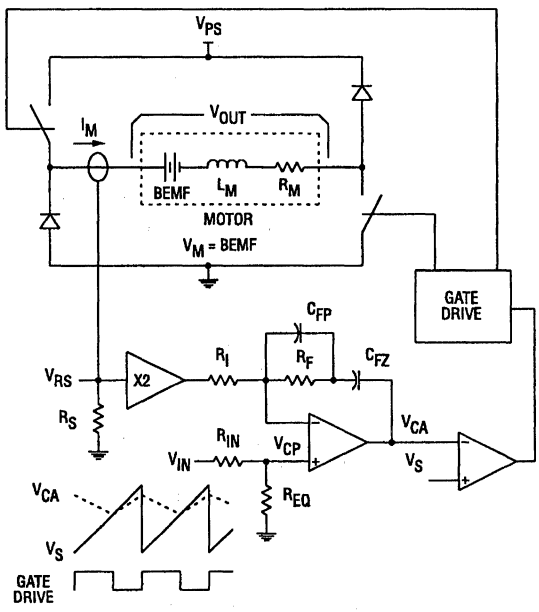


Figure 12 - Current Loop Block Diagram

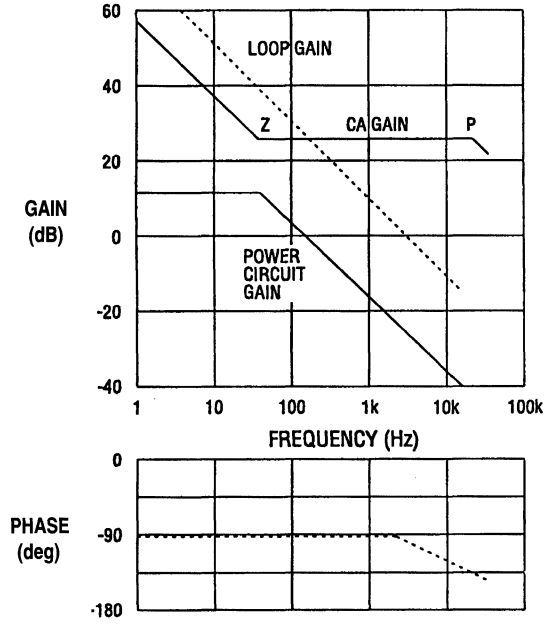


Figure 13 - Open Loop Gain and Phase Versus Frequency

current downslope appears as an upslope as shown in figure 12. To avoid subharmonic oscillation, the current amplifier output slope must not exceed the oscillator ramp slope. A motor control system typically operates over a wide range of output voltages, and is usually powered from an unregulated supply. The operating conditions which cause the greatest motor current downslope must be determined in order to determine the maximum current amplifier gain which will maintain stability. When four quadrant chopping is used, the inductor discharge rate is described by:

$$\text{Motor Current Downslope} = \frac{V_{PS} + V_M}{L_M}$$

The greatest discharge slope therefore occurs when the supply and BEMF voltages are maximum.

The oscillator ramp slope is simply:

$$\text{Oscillator Ramp Slope} = \frac{V_S}{T_S} = V_S f_S$$

Where: V_S is the oscillator ramp peak to peak voltage (1.2 V for the UC3625)
T_S is the switching period
f_S is the switching frequency

The maximum current amplifier gain at the switching frequency is determined by setting the amplified inductor current downslope equal to the oscillator ramp slope.

$$\frac{V_{PS} + V_M}{L_M} R_S G_{CA} = V_S f_S$$

$$(5) \quad \therefore \max G_{CA} = \frac{\Delta V_{CA}}{\Delta V_{RS}} = \frac{V_S f_S L_M}{R_S (V_{PS} + V_M)}$$

The maximum BEMF and supply voltage for the design example are 87 and 175 Volts respectively, which translates to a motor speed of 1500 RPM, and a high-line supply voltage of 125 Volts AC. Using equation (5) with an oscillator voltage of 1.2 volts peak to peak at a frequency of 20 kHz, the maximum value for G_{CA} is 20.2, or 26 dB. The current sense amplifier's gain of two is also part of G_{CA}. With R_I equal to 2.43 k, 20 k is selected for R_F to allow for tolerances, resulting in an actual G_{CA} of 16.5, or 24 dB.

The small-signal control to output gain of the current loop power section is described by:

$$(6) \quad \frac{\Delta V_{RS}}{\Delta V_{CA}} = \frac{R_S 2 V_{PS}}{V_S s L_M}$$

Note that the factor of two in the numerator is a result of four quadrant chopping which only utilizes one-half of the modulator's input range for a given quadrant of operation.

The overall open loop gain of the current loop is the product of the actual current amplifier gain and the control to output gain of the power circuit. The result is set equal to one to solve for the loop gain crossover frequency, f_C:

$$(7) \quad G_{CA} \frac{R_S 2 V_{PS}}{V_S 2 \pi f_C L_M} = 1$$

$$(8) \quad f_C = \frac{G_{CA} R_S V_{PS}}{V_S \pi L_M}$$

At high line, where the supply is 175 Volts DC, f_c is 3.5 kHz. The crossover frequency drops to 2.8 kHz at low line, where the supply is approximately 140 Volts DC. If greater bandwidth is required, the current amplifier gain must be increased, requiring a corresponding increase in switching frequency to satisfy equation (5).

Up to this point the motor's resistance (R_M) has been ignored. This is valid since L_M predominates at the switching frequency. The motor's electrical time constant L_M/R_M, creates a pole, which is compensated for by placing zero R_FC_{FZ} at the same frequency. Additionally, pole $R_FC_{FP}C_{FZ}/(C_{FP}+C_{FZ})$ is placed at f_S to reduce sensitivity to noise spikes generated during switching transitions. The filter pole at f_S also reduces the amplitude and slope of the amplified inductor current waveform, possibly suggesting that the current amplifier gain could be increased beyond the maximum value from equation (5). Experimentally increasing G_{CA} may incur subharmonic oscillation however, since equation (5) is only valid for a system with a single pole response at f_S. For the design example, standard values are chosen for C_{FZ} and C_{FP} of 0.22 µF and 390 pF respectively, placing the zero at 36 Hz, and the pole at 20 kHz. Figure 13 shows open loop gain and phase verses frequency.

At very light loads, the motor current will become discontinuous - motor current reaches zero before the switching period ends. At this mode boundary, the power stage gain suddenly decreases, and the single pole characteristic of continuous mode operation with its 90 degree phase lag disappears. The current loop becomes more stable, but much less responsive. Fortunately, the high gain of current amplifier is sufficient to maintain acceptable closed current loop gain and phase characteristics at typical outer velocity and/or position loop crossover frequencies.

When the current loop is closed, the output voltage of the current sense amplifier ($2V_{RS}$) is equal to the current programming voltage (V_{CP}) at frequencies below the crossover frequency. The closed current loop transconductance is simply:

$$(9) \qquad g_M = \frac{\Delta i_M}{\Delta V_{CP}} = \frac{\Delta V_{RS}/R_S}{\Delta V_{CP}} = \frac{1}{2R_S}$$

At the open loop crossover frequency, the transconductance rolls off and assumes a single pole characteristic. The input divider network attenuates the current command signal to provide compatibility with typical servo controller output voltages, and decreases the closed loop transconductance by the ratio of $R_{EQ}/(R_{EQ}+R_{IN})$. For the design example, the overall amplifier transconductance is 1.25 amps/volt, allowing full scale current (6 amps) with a 5 volt input command.

BIPOLAR TO SIGN/MAGNITUDE CONVERSION

The servo amplifier as shown in figure 6 requires a separate sign and magnitude input command. This is convenient for many microcontroller based systems which solely utilize digital signal processing for servo loop compensation. Analog compensation circuits however, usually output a bipolar signal and require conversion to sign/magnitude format to work with this amplifier. The circuit shown in figure 14 employs a differential amplifier for level shifting and ground noise rejection, and an absolute value circuit with polarity detection for conversion to sign/magnitude format. The current command signal is slightly attenuated and level shifted up 5 volts to allow single supply operation. The input divider circuit has been slightly modified from figure 9 to restore gain and provide a suitable offset adjustment range. Precision resistors (1%) should be used for both the differential amplifier and the absolute value circuit to minimize DC offset errors. Figure 15 shows approximately 2 Amp peak motor current with a 500 Hz sinwave command. Motor current follows the input command with minimal phase lag, however some crossover distortion is present. This is not crossover distortion in the traditional sense, rather it is simply a fixed off-time caused by the cross conduction protection circuitry. Since this distortion is current amplitude independent, and decreases with frequency, its effect on overall servo loop performance is minimal.

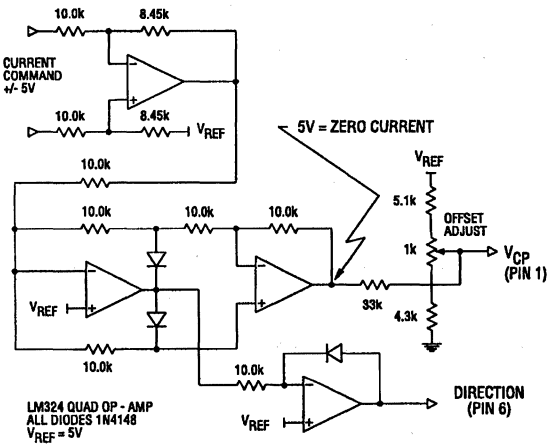


Figure 14 - Bipolar to Sign/Magnitude

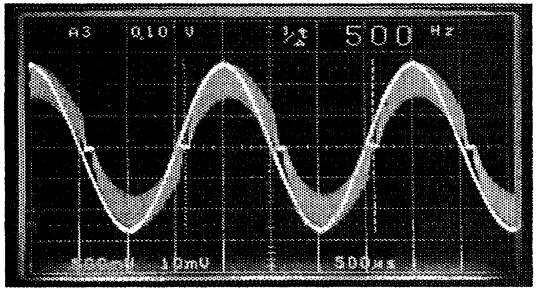


Figure 15 - 5OOHz Sine Wave Command and Output Currents

DIRECT DUTY CYCLE CONTROL

There are many less demanding brushless DC servo applications which do not need a transconductance amplifier function yet require controlled operation in all four quadrants. For these systems, direct duty cycle control, also known as voltage mode control is often employed. Note that this is not voltage feedback, which requires additional demodulation circuitry to develop a feedback signal. With direct duty cycle control the amplifier simply provides open loop voltage gain. This technique is particularly advantageous when a microcontroller is used for servo loop compensation. By outputting a PWM signal directly, a digital to analog conversion is eliminated along with the analog pulse width modulator. While the simplicity of this technique is appealing, there are two major problems which must be addressed. The first and less severe problem is the complete lack of power supply rejection. Good supply filtering will often reduce transients to acceptable levels, while the servo loop compensates for slow disturbances. The second and more troublesome predicament is the output nonlinearity which occurs when transitioning between quadrants. This is best illustrated by examining the DC equations for the two possible cases.

When operating in either quadrant one or three, rotation and torque are in the same direction. Assuming operation is above the continuous/discontinuous current mode boundary, the output voltage is described by:

$$(10) \quad V_M = 2V_{PS}D - V_{PS}$$

where D = PWM duty cycle

When the direction command is reversed while the motor is rotating, operation switches to quadrant two or four, shifting the modulator's maximum output voltage point from full duty cycle to zero duty cycle.

$$(11) \quad V_M = 2V_{PS}(1\text{-}D) - V_{PS}$$

Note that the gain does not change, only the reference point has shifted. This occurs because the modulator only has a single quadrant control range -four quadrant operation results from the output control logic which is after the modulator. With the transconductance amplifier previously described, the error amplifier quickly slews during quadrant transitions, providing four quadrant control with minimal disturbance. When direct duty cycle control is used however, the servo loop filter must slew to maintain control. Unfortunately, this causes an immediate loop disturbance, with the greatest severity at the duty cycle extremes. This behavior can greatly effect the performance of an analog compensated servo, and therefore limits such systems to lower performance requirements.

With a microcontroller providing the servo loop compensation, nonlinear duty cycle changes can be accommodated, restoring linearity when transitioning between quadrants. Although nonlinear behavior still occurs when motor current becomes discontinuous, the effect on overall system performance is usually minimal. By correcting for quadrant transition nonlinearities, the advantages of an all digital interface can be exploited without severely degrading system performance. The control system is fully digital right up to the output stage, where the motor's inductance finally makes the conversion to analog by integrating the output switching waveform.

The circuit shown in figure 16 uses a PWM input from a microcontroller to set the output duty cycle and synchronize the oscillator, while another input controls direction.

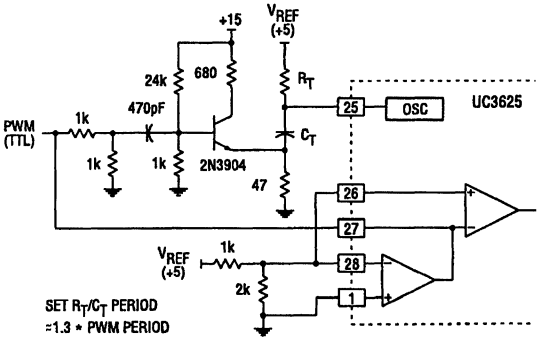


Figure 16 - Digital PWM Interface

APPLICATION NOTE

Complete line isolation can easily be achieved by using opto-couplers. Although the performance of this technique falls short of the transconductance amplifier, the circuitry's simplicity while maintaining all of the protection features of the UC3625 make it well suited to many cost sensitive applications.

SUMMARY

The application example demonstrates the relative simplicity in implementing a brushless DC transconductance servo amplifier using the latest generation controller and driver ICs. For less demanding applications, direct duty cycle control using a dedicated controller provides size and cost reduction, without sacrificing protection features. While more and more control functions are implemented in microcontrollers today, the task of interfacing to output devices, and providing reliable protection under all conditions will remain a hardware function. Dedicated integrated circuits offer considerable improvement over the discrete solutions used in the past, reducing both size and cost, while enhancing reliability.

REFERENCES

Unitrode Publications:

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4. B. Neidorff, "New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors", Application Note # U-115
5. J. O'Connor, "Unique Chip Pair Simplifies Isolated High Side Switch Drive", Application Note # U-127
6. C. de Sa e Silva, "A Simplified Approach to DC Motor Modeling For Dynamic Stability Analysis", Application Note # U-120

UNITRODE DATA SHEETS

7. UC3625
8. UC3724
9. UC3725

ADDITIONAL REFERENCES:

10. APT4030BN Data Sheet, Advanced Power Technology, Bend OR
11. M-178 Brushless Motor DataSheet, MFM Technology, Inc., Ronkonkoma NY
12. "DC Motors - Speed Controls - Servo Systems", Electro-craft Corporation, Hopkins MN

UNITRODE CORPORATION
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9 Special Function Circuits

Special Functions

Special Functions

Current Sensors	UNITRODE PART NUMBER UCC3926				
Application	Current Sensing				
Maximum Current	± 20A				
Application / Design Note	DN-91				
Pin Count❖	16				
Page Number	PS/9-43				

Lighting Controllers	UNITRODE PART NUMBER UCC3305✣				
Application	Constant Power HID Lamp Controller				
Topology	Boost, Flyback				
Outputs	3 - Single and Dual Alternating, Totem Pole				
Reference Tolerance	2%				
Open Lamp Detect	Y				
Soft Start	Y				
External Synchronization	Y				
Shutdown Current	N/A				
Maximum Frequency	500kHz				
Lamp Intensity Control	Y				
Application / Design Note	DN-72, U-161				
Pin Count❖	28				
Page Number	PS/9-5				

❖The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

Special Functions (cont.)

Ring Generator Controllers	UNITRODE PART NUMBER		
	UCC3750	UCC3751+	UCC3752+
Description	Source Ringer Controller	Single Line Ring Generator Controller	Mulit-Line Ring Generator Controller
Application	4 Quadrant Flyback Controller Develops High Voltage AC Output	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset
Key Features	•On Chip Low THD Sinewave Reference, Pin Selectable 20Hz, 25Hz, and 50Hz •Programmable Output Amplitude and DC Offset •AC and DC Current Limiting With Short Circuit Protection	•Off-hook Detection With Automatic Transition to DC Operation •Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency •Operates From a Single 12V Supply •AC Current Limiting and Short Circuit Protection	•Off-hook Detection and Indication •Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency •Operates From a Single 12V Supply •AC Current Limiting and Short Circuit Protection
Application / Design Note	DN-79, U-169		
Pin Count❖	28	16	16
Page Number	PS/9-22	PS/9-32	PS/9-38

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions (cont.)

Sensor Drivers	UNITRODE PART NUMBER				
	UC37131+	UC37132+	UC37133+		
Part Name	Smart Power Switch	Smart Power Switch	Smart Power Switch		
Description	65V Universal Low Side Driver with Current Limiting	65V Universal High or Low Side Driver with Current Limiting	65V Universal High Side Driver with Current Limiting		
Pin Count❖	8	14, 16	8		
Page Number	PS/9-13	PS/9-13	PS/9-13		

Serial DACs	UNITRODE PART NUMBER		
	UCC5950		
Part Name	Digital to Analog Converter		
Description	10-Bit BiCMOS Digital to Analog Converter for Servo and Instrumentation Systems		
Pin Count❖	8		
Page Number	PS/9-48		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product


UNITRODE

UNITRODE

application INFO available

UCC2305
UCC3305

HID Lamp Controller

FEATURES

- Regulates Lamp Power
- Compensates For Lamp Temperature
- Fixed Frequency Operation
- Current Mode Control
- Overcurrent Protected
- Overvoltage Shutdown
- Open and Short Protected
- High Current FET Drive Output
- Operates Over Wide Battery Voltage Range: 5V to 18V

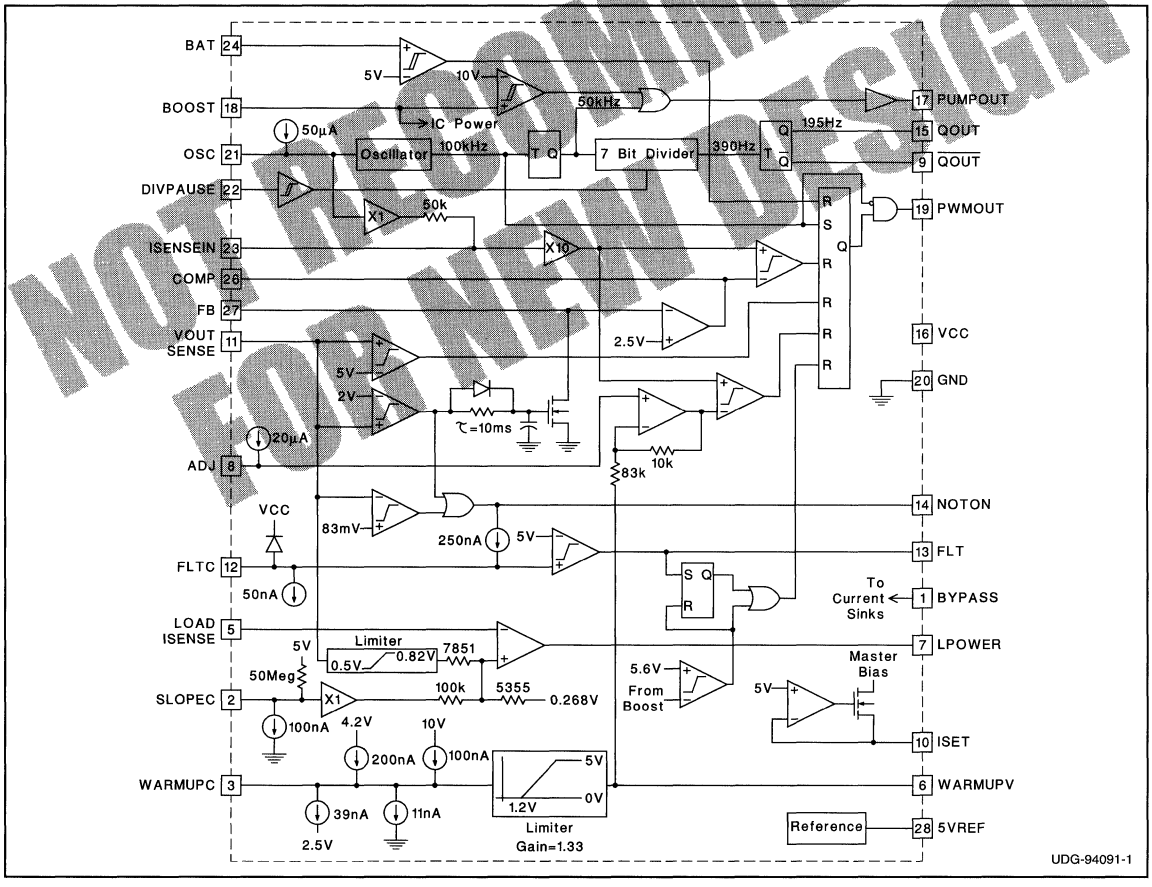
DESCRIPTION

The UCC3305 integrates all of the functions required to control and drive one HID lamp. The UCC3305 is tailored to the demanding, fast turn-on requirements of automobile headlamps, but is also applicable to all other lighting applications where HID lamps are selected. HID lamps are ideal for any lighting applications that can benefit from very high efficiency, blue-white light color, small physical lamp size, and very long life.

The UCC3305 contains a complete current mode pulse width modulator, a lamp power regulator, lamp temperature compensation, and total fault protection. Lamp temperature compensation is critical for automobile headlamps, because without compensation, light output varies dramatically from a cold lamp to one that is fully warmed up.

The UCC2305 is tested for full performance with ambient temperature from –40°C to +105°C while the UCC3305 is tested with ambient temperature from 0°C to +70°C. The UCC3305 is available in a 28 pin small-outline, surface mount plastic package (SOIC).

BLOCK DIAGRAM



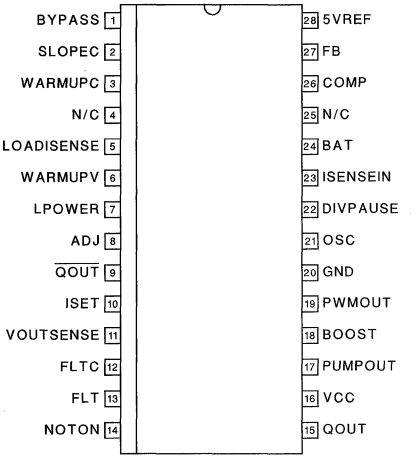
ABSOLUTE MAXIMUM RATINGS

VCC Supply Voltage 8.0V
BOOST Supply Voltage 12.0V
PWMOUT Current, Peak . . . . . ±1.0A
PWMOUT Energy, Capacitive Load 5.0µJ
Input Voltage, Any Input . . . . . –0.3V to +10.0V
Output Current, QOUT, $\overline{QOUT}$, FLT . . . . . ±10.0mA
Output Current, 5VREF, LPOWER, COMP . . . . . ±10.0mA
ISET Current . . . . . –1.0mA
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature . . . . . +300°C

All voltages with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-28 (Top View)
DW Package



ELECTRICAL CHARACTERISTICS Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Overall Section					
VCC Supply Current			0.1	1.0	mA
BOOST Supply Current			3.0	5.0	mA
BOOST Threshold to PUMP Stop		9.1	9.6	10.1	V
BOOST Threshold to PUMP Start		9.2	9.7	10.2	V
BOOST Threshold to PWMOUT		5.1	5.6	6.1	V
Battery Section					
BAT Threshold to PWMOUT Stop		4.8	5.0	5.2	V
BAT Threshold to PWMOUT Start		4.25	4.8	5.0	V
BAT Input Current	BAT = 4V	–1		1	µA
Oscillator & Divider Section					
OSC Frequency		80	100	120	kHz
OSC Pull-Up Current	OSC = 1.5V	–70	–50	–40	µA
DIVPAUSE Threshold to Pause		1.2	1.5	1.8	V
DIVPAUSE Threshold to Divide		0.9	1.2	1.5	V
DIVPAUSE Input Current	0V < DIVPAUSE < 6V	–8	–5	–2	µA
Reference Section					
5VREF Voltage		4.85	5.0	5.1	V
ISET Voltage		4.7	4.8	5.1	V
Error Amplifier Section					
FB Voltage		2.4	2.5	2.6	V
FB Input Current		–1	0	1	µA
FB Sink Current	VOUTSENSE = 4V, FB = 4V	0.3	1.5		mA
FB Release Delay	VOUTSENSE Step from 4V to 1V	17	30	43	ms
COMP Source Current	FB = 2V, COMP = 4V		–3.0	–0.2	mA

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
COMP Sink Current	FB = 3V, COMP = 1V	0.2	1.0		mA
Load Power Amplifier Section					
LOADISENSE Input Current		–2.5	–0.1	2.5	µA
LPOWER Source Current	LPOWER = 0V		–8.0	–0.4	mA
LPOWER Sink Current	LPOWER = 1V	0.4	1.3		mA
LPOWER Voltage	VOUTSENSE = 0.0V	0.35	0.40	0.45	V
	VOUTSENSE = 0.45V	0.35	0.40	0.45	V
	VOUTSENSE = 0.65V	0.41	0.46	0.51	V
	VOUTSENSE = 0.88V	0.46	0.51	0.56	V
	VOUTSENSE = 2.0V	0.46	0.51	0.56	V
	VOUTSENSE = 0.7V, SLOPEC = 0V	0.29	0.34	0.39	V
Input Current Sense Section					
ISENSEIN Threshold	COMP = 5V, WARMUPC = 0V	0.16	0.21	0.28	V
	COMP = 5V, WARMUPC = 10V	0.13	0.19	0.27	V
	COMP = 1V, WARMUPC = 0V	0.07	0.10	0.2	V
ISENSEIN Bias Current	OSC = 0V	–15	–5	–2	µA
	OSC = 2V	–65	–40	–15	µA
VOUTSENSE Section					
VOUTSENSE Threshold to PWMOUT		4.2	5.0	5.2	V
VOUTSENSE Threshold to FB		1.7	1.9	2.1	V
VOUTSENSE Threshold to NOTON		0.035	0.083	0.140	V
VOUTSENSE Input Current		–1		1	µA
OUTPUTS SECTION					
PWMOUT High Voltage	I_{PWMOUT} = –100mA	9.15	10.0		V
PWMOUT Low Voltage	I_{PWMOUT} = 100mA		0.3	0.5	V
PUMPOUT High Voltage	$I_{PUMPOUT}$ = –10mA	5.3	5.8		V
PUMPOUT Low Voltage	$I_{PUMPOUT}$ = 10mA		1.0	1.8	V
PUMPOUT Frequency	BOOST = 9.5V	35	50	60	kHz
NOTON High Voltage	I_{NOTON} = –1mA	5.0	6.3		V
NOTON Low Voltage	I_{NOTON} = 1mA		0.1	0.3	V
QOUT, $\overline{QOUT}$ High Voltage	I_{QOUT} = –1mA or $I_{\overline{QOUT}}$ = –1mA	5.0	6.3		V
QOUT, $\overline{QOUT}$ Low Voltage	I_{QOUT} = 1mA or $I_{\overline{QOUT}}$ = 1mA		0.1	0.45	V
QOUT, $\overline{QOUT}$ Frequency		175	250	275	Hz
FLT High Voltage	I_{FLT} = –1mA	6.0	6.3		V
FLT Low Voltage	I_{FLT} = 1mA		0.1	0.3	V
Timing Capacitor Section					
FLTC Discharge Current	FLTC = 2.5V	35	60	90	nA
FLTC Charge Current	FLTC = 2.5V	–380	–290	–220	nA
FLTC Threshold to FAULT		4.65	4.9	5.1	V
SLOPEC Charge Current	SLOPEC = 0.5V	–165	–90	–60	nA
	SLOPEC = 2.2	–105	–60	–40	nA
	SLOPEC = 4.2	–35	–20	–10	nA
SLOPEC Voltage	I_{SLOPEC} = –125nA	1.3	1.5	1.7	V

ELECTRICAL CHARACTERISTICS (cont.) Unless otherwise stated, VCC = 6.6V, ISET = 100kΩ to GND, ADJ = 100kΩ to GND, OSC = 200pF to GND, BAT = 4V, LOADISENSE connected to LPOWER, VOUTSENSE = 0.666V, BOOST = 10.5V, COMP connected to FB through a 100kΩ resistor, –40°C<T_A<+105°C for the UCC2305, 0°C<T_A<+70°C for the UCC3305, and T_A=T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
	I_{SLOPEC} = –50nA	2.8	3.0	3.2	V
Timing Capacitor Section (cont.)					
SLOPEC Discharge Current	SLOPEC = 2.2V, VCC = 0V, BOOST = 0V, BYPASS = 8V	40	90	175	nA
WARMUPC Charge Current	WARMUPC = 0V	–515	–375	–275	nA
	WARMUPC = 2V	–450	–375	–300	nA
	WARMUPC = 6V	–170	–120	–75	nA
WARMUPC Voltage, Charging	$I_{WARMUPC}$ = –250nA	3.5	3.8	4.1	V
WARMUPC Discharge Current	WARMUPC = 5V, VCC = 0V, BOOST = 0V, BYPASS = 8V	23	50	108	nA
	WARMUPC = 1V, VCC = 0V, BOOST = 0V, BYPASS = 8V	5	10	20	nA
WARMUPC Voltage, Discharging	$I_{WARMUPC}$ = 25nA, VCC = 0V, BOOST = 0V, BYPASS = 8V	1.5	1.9	2.3	V
ADJ Bias Current	V_{ADJ} = 0V	–38	–20	–12	µA
WARMUPV Voltage	WARMUPC = 1V	0.05	0.125	0.25	V
	WARMUPC = 2V	0.09	0.108	1.27	V
	WARMUPC = 3V	2.3	2.48	2.66	V
	WARMUPC = 5V	4.5	4.8	5.1	V
	WARMUPC = 10V	4.5	4.8	5.1	V
BYPASS Voltage	VCC = 0V	8.8	9.6		V
BYPASS Current	VCC = 0V, BOOST = 0V, BYPASS = 8V		2.5	7	µA

PIN DESCRIPTIONS

5VREF: Circuitry in the UCC3305 uses the internal 5V reference to set currents and thresholds. This reference can also be used for other functions if required.

ADJ: The ratio of cold lamp peak current to warmed-up lamp peak current is controlled by the voltage on ADJ. To select this voltage, connect a resistor from ADJ to GND.

BAT: This input is used to detect excessively high input voltage and shut down the IC if the input exceeds a predetermined level. Connect BAT to a voltage divider across the input supply. The UCC3305 shuts down when this input voltage exceeds 5V. To protect the IC in the event of very high or negative inputs, keep divider impedance higher than 10k.

BOOST: Although the UCC3305 is powered from the VCC input, most functions of the device operate from a supply voltage of approximately 10V connected to BOOST. This 10V supply can be generated by a voltage doubler using PUMPOUT as an AC signal and external diodes as switches.

BYPASS: The UCC3305 compensates for lamp temperature changes by changing the voltage on the SLOPEC and WARMUPC capacitors. These voltages rise as the lamp warms up. An internal calculation determines what power should be applied to the lamp.

When the HID lamp is turned off, power to the lamp and the controller is removed, leaving these two critical capacitors charged to specific voltages. Also, with power off, the lamp will cool down at a controlled rate. It is essential that the two capacitors discharge at a similarly controlled rate so that if the lamp is restarted before the lamp is fully cooled, the controller will have an estimate of new lamp temperature, and can again command the correct power for the lamp.

Power to control the discharge of these capacitors comes from energy stored in a large capacitor connected to BYPASS. The value of the capacitor required can be estimated assuming a maximum BYPASS current of 5µA, a discharge time of 60s, and a maximum allowable droop of 5V by:

$$C = I \bullet \frac{\Delta t}{\Delta V} = 5\mu A \bullet \frac{60s}{5V} = 60\mu F$$

COMP: Differences between commanded lamp power and desired lamp power are amplified by an error amplifier. This amplifier senses the difference between the voltage at FB and 2.5V, and drives COMP with an amplified error voltage. A capacitor is normally connected from

PIN DESCRIPTIONS (cont.)

COMP to FB to compensate the overall feedback loop so that the system will be stable.

DIVPAUSE: The QOUT and $\overline{QOUT}$ outputs can be used to switch lamp polarity in an AC ballast. It is important to stop polarity switching when the lamp is being lit, so that the arc across the electrodes can form in the correct place. Pulling high on DIVPAUSE stops the internal divider which generates the QOUT and $\overline{QOUT}$ signals, and thereby freezes the QOUT and $\overline{QOUT}$ signals.

To stop the divider when the lamp is being lit and start after the lamp has lit, connect a resistor from NOTON to DIVPAUSE and a capacitor from DIVPAUSE to GND.

FLTC: The voltage on VOUTSENSE is proportional to lamp voltage. If that voltage is too high or too low, the lamp is either open, shorted, or not yet running. During normal operation, there is a capacitor connected to FLTC, and this capacitor is discharged to 0V by a current source inside the UCC3305.

The UCC3305 monitors the voltage on VOUTSENSE and compares it to an internal 83mV lower threshold and a 2V upper threshold. If the voltage is outside this window, then the IC will pull up on FLTC with a current of approximately 250nA. If the fault remains long enough to charge the external FLTC capacitor over 5V, the controller declares a catastrophic fault and shuts the IC down. The IC will stay shut down until power is removed from BOOST.

If the fault clears before the FLTC capacitor reaches 5V, the capacitor discharges down to 0V. This discharge current is approximately 50nA, representing a five times longer discharge rate than charge rate.

FLT: If the voltage on the FLTC pin exceeds 5V, indicating a severe fault, then a latch in the UCC3305 sets and PWM drive is halted. In addition, the FLT output goes high to VCC, indicating a serious system fault.

FB: Differences between commanded lamp power and desired lamp power are amplified by an error amplifier. This amplifier senses the difference between the voltage at FB and 2.5V, and drives COMP with an amplified error voltage.

GND: Ground for all functions is through this pin.

ISENSEIN: The power regulating algorithm in the UCC3305 HID Controller computes a function of lamp current and lamp voltage and commands the appropriate battery current to keep lamp power constant. This appropriate battery current is sensed by a connection from I-SENSEIN to a current sense resistor. This current sensed pulse width modulation scheme is often referred to as current mode control.

In addition to this current regulation, the UCC3305 contains peak input current limiting. This limiting is set to 0.2V across the ISENSEIN resistor during normal operation and 0.4V during starting. The transition from starting to normal operation is accomplished by the rise of the WARMUPC capacitor.

Current mode control has an advantage over voltage mode control in that a current mode loop is easier to compensate. Current mode control has a disadvantage compared to voltage mode control in that the loop can enter into chaotic oscillations at high duty cycles. These chaotic oscillations can be prevented using slope compensation. The UCC3305 contains internal slope compensation in the form of a current proportional to OSC voltage on ISENSEIN. This current combined with an external resistor from ISENSEIN to the current sense resistor creates a voltage drop proportional to OSC voltage, which gives slope compensation.

ISET: Many functions inside the UCC3305 require precise currents to give well controlled performance. These controlled currents are programmed by a resistor from ISET to GND. A resistor of 100k programs the IC to normal operating current. Lower resistor values increase the internal currents. Some of the functions which are influenced by this resistor are WARMUPC charging and discharging, SLOPEC charging and discharging, FLTC charging and discharging, and error amplifier bandwidth

LOADISENSE: Just as ISENSEIN is normally connected to a current sense resistor which monitors battery current, LOADISENSE is normally connected to a resistor which monitors lamp current. Lamp current is then regulated by the controller such that the correct lamp power is supplied at every lamp temperature, in conjunction with the lamp voltage sensed by VOUTSENSE.

LPOWER: LOADISENSE directly drives one input of an op amp in the UCC3305. This amplifier amplifies the difference between the desired load current and the actual load current, and generates an output signal on LPOWER which feeds the error amplifier.

NOTON: While the lamp is in a fault condition, such as excessively high or low lamp voltage, NOTON is pulled high to VCC, indicating that the arc is not yet correct. When the voltage on VOUTSENSE is within the 83mV to 2V window, NOTON is pulled low.

OSC: The fixed frequency PWM in the UCC3305 operates at the frequency programmed by the OSC pin. Typically, a a 200pF capacitor from OSC to GND programs the PWM frequency at 100kHz. In addition, this programs the charge pump at 50kHz and the $\overline{QOUT}$ and QOUT signals at 192Hz. The actual oscillator frequency is a function of both the capacitor from OSC to GND and the resistor from ISET to GND.

PIN DESCRIPTIONS (cont.)

PUMPOUT: Although the UCC3305 is powered from the VCC input, most functions of the device operate from a supply voltage of approximately 10V connected to BOOST. In normal operation, this 10V supply is generated by a voltage doubler using the PUMPOUT pin as an AC signal and external diodes as switches. PUMP-OUT is a square wave which swings from VCC to GND at half of the OSC frequency.

PWMOUT: The output of the pulse width modulator is a command signal to a power MOSFET switch. This signal appears on PWMOUT. In normal systems, PWM-OUT can be directly connected to the gate of an N-channel power MOSFET such as the IRF540. If the lead between the UCC3305 and the MOSFET is longer than a few cm, a 10 ohm resistor from PWMOUT to gate may be required to dampen overshoot and undershoot.

$\overline{\text{QOUT}}$: The UCC3305 is immediately configured for DC HID lamps. To operate with AC HID lamps, it is necessary to add a power H-bridge which will toggle lamp voltage. A practical switching frequency for this toggle function is the OSC frequency divided by 512, or 192Hz for a 100kHz oscillator.

The $\overline{\text{QOUT}}$ pin is a logic output which toggles at the OSC frequency divided by 512, 180 degrees out of phase with the QOUT pin.

QOUT: The QOUT pin is a logic output which toggles at the OSC frequency divided by 512, 180 degrees out of phase with the $\overline{\text{QOUT}}$ pin.

SLOPEC: To track lamp warm-up and cool down, two capacitors connected to the UCC3305 charge and discharge. One is connected to SLOPEC. The other is connected to WARMUPC. The capacitor connected to SLOPEC charges up to 5V with a rate controlled by the resistor from ISET to GND. With a nominal 100k ISET resistor the charging current into SLOPEC is equivalent to the current from a 50Meg resistor to 5V. When power is removed from VCC, SLOPEC discharges at a constant current, nominally 100nA.

VCC: VCC is the main supply input to the UCC3305. Many functions in the UCC3305 are powered by VCC, while others are powered by BOOST. VCC should be clamped to 6.8V by an external zener diode and kept as close to 6.8V as practical with a low value resistor to the input supply.

VOUT-SENSE: The VOUTSENSE input is used to sense lamp voltage, commonly through a 120:1 voltage divider. For a normal, running HID lamp, the voltage across the lamp is between 60V and 110V. It takes higher than 300V to break down the lamp, and it is desirable to limit the voltage on the starter input to 600V maximum. A lamp voltage less than 10V is indicative of a shorted lamp.

The UCC3305 regulates lamp power by commanding the correct lamp current for a given lamp voltage. In addition, a comparator in the UCC3305 terminates a PWM cycle if VOUTSENSE reaches 5V, corresponding to 600V on the lamp. This regulates lamp voltage at 600V when the lamp is not lit. Comparators in the UCC3305 also compare VOUTSENSE to 83mV corresponding to 10V lamp voltage and 2V, corresponding to a 240V lamp voltage. When the VOUTSENSE voltage is outside this window, the lamp is either not lit, shorted, or open.

WARMUPC: In addition to the capacitor from SLOPEC to GND, lamp temperature is estimated by the voltage on a capacitor from WARMUPC to GND. This capacitor is charged by a 200nA current source to 4.2V and by a 100nA current source from 4.2V to 10V when the lamp is on, and discharged by 39nA current sink to 2.5V and 11nA current sink to GND when the lamp is off.

WARMUPV: The voltage on WARMUPC is used to modulate the signal fed to the error amplifier through FB. However, the impedance on WARMUPC is too high to be directly used. The UCC3305 contains a buffer amplifier which is derived from the PWM oscillator. It is desirable to switch lamp polarity when running, but switching lamp polarity can interfere with clean starting. The UCC3305 has a logic output called NOTON which is high when the lamp is not running (Not On) and low when the lamp is running. This output is connected to the DIVPAUSE input so that the low frequency switching stops until the lamp is fully lit.

APPLICATIONS INFORMATION

Typical Application

This circuit shows the UCC3305 HID Lamp Controller IC in a flyback converter. The output of the converter is regulated at constant power, so that lamp intensity is relatively constant regardless of small lamp manufacturing variations.

Full Bridge Output Stage

The output of the flyback converter is directed to the AC lamp through a full bridge inverter. The full bridge is switched at a low frequency (typically 195Hz), so that the average lamp voltage is zero. The low frequency switching is derived from the PWM oscillator. The UCC3305 HID Controller IC has two low frequency outputs, QOUT and $\overline{\text{QOUT}}$. These outputs are capable of driving low-side MOSFETs directly at 195Hz, but high-side MOSFETs require a level-shifted drive. This

APPLICATIONS INFORMATION (cont.)

can be as simple as a high voltage transistor and a resistor pull-up, combined with the correct choice of phases.

Regulated Lamp Input Power Gives Constant Intensity

The LPOWER output of the UCC3305 is a voltage roughly proportional to lamp input power. The UCC3305 regulates constant lamp power over a wide range of lamp voltages. The range of lamp voltages which produce constant lamp power is set by the limiting amplifier on VOUTSENSE.

For inputs to VOUTSENSE below 0.5V, such as would occur with a shorted lamp, the loop regulates constant load current. For inputs to VOUTSENSE greater than 0.82V, as might occur with a lamp that is open or not yet lit, the loop also regulates constant load current, but at a lower current than for a shorted lamp. In between those two voltages, the amplifier driving the LPOWER pin will sum the load current and load voltage and produce a signal roughly proportional to load power. The summing amplifier approximates power well enough to hold power within ±10% over a factor of two in lamp voltage.

The UCC3305 HID Controller contains a current mode PWM similar to the industry standard UC3842 and UCC3802 circuits. This controller uses a high gain op amp to regulate the output of the LPOWER circuit. This op amp drives a high speed PWM comparator, which compares converter input current to the output of the op amp and uses this signal to set duty cycle.

Slope Compensation

In addition to a complete current mode PWM, the UCC3305 HID Controller contains internal slope compensation, a valuable function which improves current loop stability for high duty cycles. Slope compensation is accomplished with an on-chip current ramp and an off-chip resistor RSL. Larger values of RSL give more slope compensation and a more stable feedback loop.

Powering The UCC3305

Conventional power MOSFETs require at least 8V of gate drive to ensure high efficiency and low on resistance. Despite this requirement, the UCC3305 HID Controller can be used to build a ballast that will drive power MOSFETs well with input supplies as low as 5V! The UCC3305 does this using a charge pump.

In this typical application, power for the UCC3305 HID Controller IC is derived from a 6.8V zener supply. This zener regulated supply gives the application overvoltage protection, reverse battery protection, low parts count, and low cost. The output of the 6.8V zener supply drives the VCC pin of the UCC3305. VCC is the input to the UCC3305 charge pump. The charge pump generates a regulated 10V supply on the BOOST output. This 10V supply drives all other functions on the UCC3305.

Protection From Over Voltage

The most significant stresses in an automotive environment are the overvoltage conditions which can occur during load dump and double-battery jump start. At these times, the voltage into the ballast can go so high that even the most overdesigned power stage will be damaged. The UCC3305 is inherently immune to damage from this when operated with a zener regulated supply. In addition, the UCC3305 will protect the ballast components by shutting down the PWM in the presence of excessive voltage on the BAT input.

This typical application shows a voltage divider consisting of a 270k resistor and a 100k resistor driving the BAT input. The threshold of the BAT input is approximately 5V, so this divider sets the shutdown voltage at approximately 18.5V.

Programming the UCC3305

All circuitry on the UCC3305 HID Lamp Controller is operated from a bias current set by the resistor from ISET to ground. For best operation, this resistor (RSET) should be between 75k and 150k.

Oscillator Frequency

The UCC3305 HID Lamp Controller PWM oscillator is set by the resistor from ISET to ground and by the capacitor from OSC to ground. Oscillator frequency can be estimated by the equation:

$$FOSC = \frac{2}{RSET \bullet COSC}$$

For operation at 100kHz, RSET should be 100k and C_{OSC} should be 200pF.

The PWM oscillator also determines the low frequency lamp switching rate for AC lamps. The exact lamp switching rate is the PWM frequency divided by 512.

Lamp Temperature Compensation

Automobile headlights must come up to full intensity very quickly, but HID lamps require many minutes to stabilize. The UCC3305 HID Controller contains sophisticated internal circuitry to anticipate lamp temperature and also to compensate for lamp temperature.

The circuits anticipate lamp temperature by monitoring charge on capacitors which charge when the lamp is on and discharge when the lamp is off. The UCC3305 HID Controller compensates for lamp temperature by driving the lamp with a higher lamp power when the lamp is cold and reducing the power to a normal operating level when the lamp is warmed up. The capacitors which set these

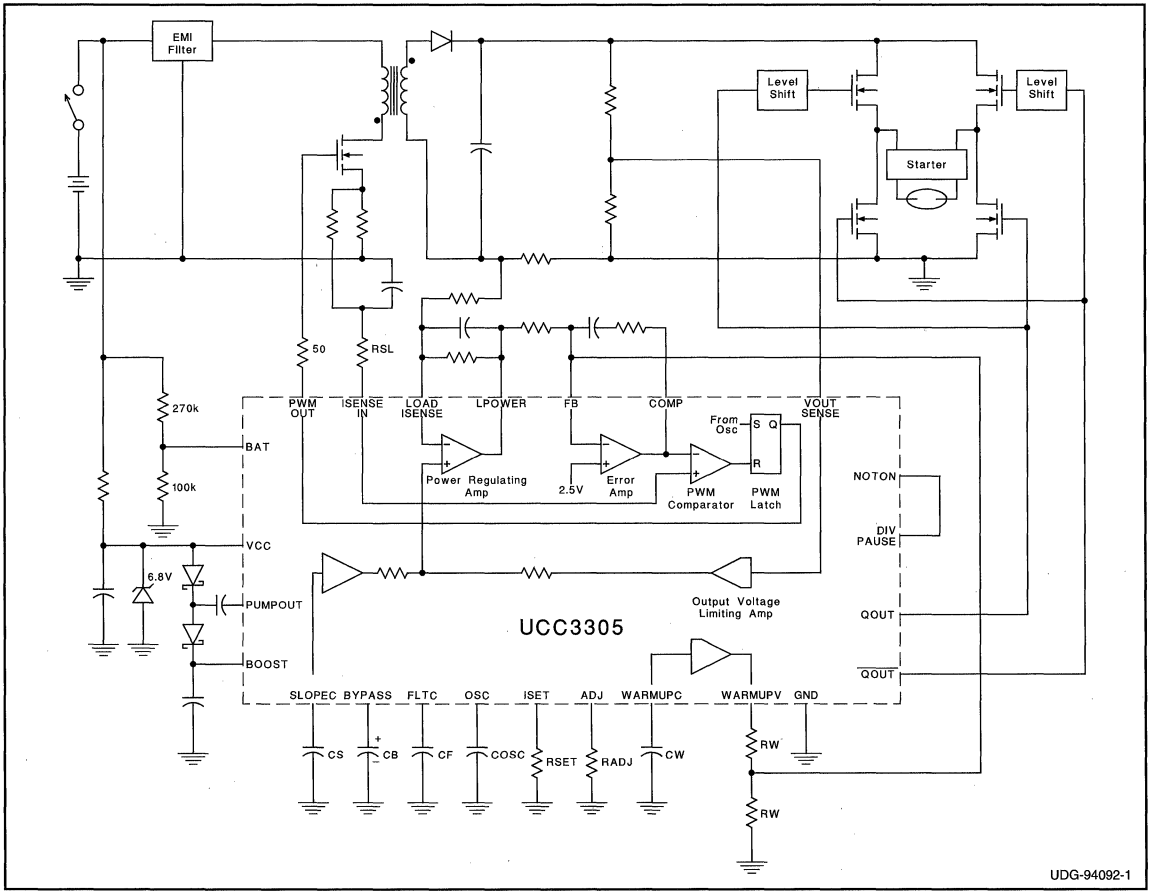
APPLICATIONS INFORMATION (cont.)

time constants are external film capacitors CS and CW, and are connected to SLOPEC and WARMUPC. CS and CW are critical capacitors and must be selected to match the time-temperature relationship of the lamp.

In addition to changing the power regulation point, the WARMUPC capacitor voltage also changes the short circuit lamp current. The ratio of cold short circuit current to warmed-up short circuit current is set by the resistor from ADJ to ground.

When power is removed from the ballast, CS and CW must discharge at a controlled rate. The discharge currents are programmed by current sources on the UCC3305 HID Controller. These current sources are powered by the power supply connected to BYPASS. In a typical application, a non-critical electrolytic capacitor from BYPASS to ground stores energy when the ballast is on and uses this energy to control the discharge rate when the ballast is off.

FLYBACK HID BALLAST



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Smart Power Switch

FEATURES

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- Low Side or High Side Switch Configuration
- 8V to 65V Operation
- Overload and Short Circuit Protection
- Power Interruption Protection
- +6V Regulated Voltage
- 2mA Quiescent Current
- Programmable Overcurrent and Power Interruption Protection
- 1% to 30% Programmable Input Comparator Hysteresis (on UC37132)
- Low and High Side Internal High Current Clamps When Driving Inductive Loads

DESCRIPTION

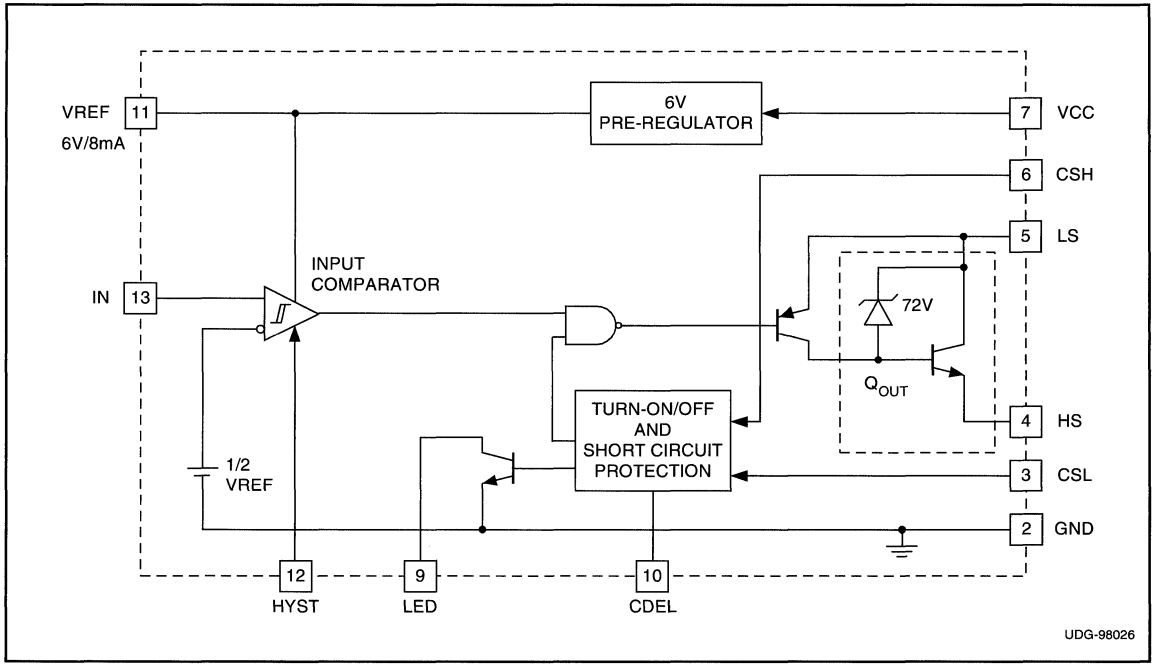
The UC37131, UC37132 and UC37133 are a family of smart power switches which can drive resistive or inductive loads from the high side or low side.

The UC37132 is available in 14 pin (DIP), 16 pin (SOIC), or 20 pin (CLCC) packages and can accommodate both low side (load to VCC) or high side (load to GND) configurations. The UC37131 and UC37133 are exclusively for a low side or a high side configuration respectively and both are available in an 8 pin package. Both high side and low side configurations provide high current switching with low saturation voltages which can drive resistive or inductive loads.

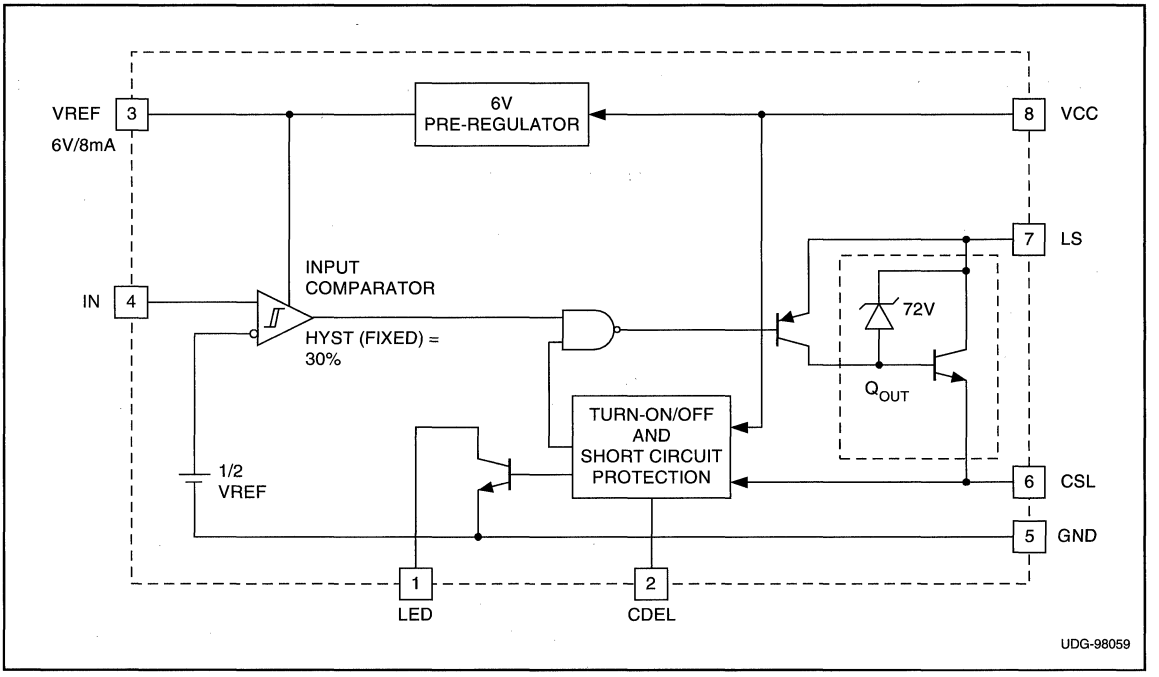
The input to the switch is driven by a low voltage signal, typically 5V. Additionally, UC37132 features adjustable hysteresis. The output of the device can switch a load between 8V and 65V. Output current capability is 300mA continuous or 700mA peak.

The device also has inherent smart features that allow for programmable turn-on delay in enabling the output following startup. The same capacitor that specifies the turn-on delay is also used to program a VCC power interruption time. If VCC drops below a threshold for a time specified by this capacitor, the output is turned off and a new turn-on delay will be re-triggered. Similarly, if high current persists longer than the response delay, the output driver will operate in a very low duty cycle mode to protect the IC.

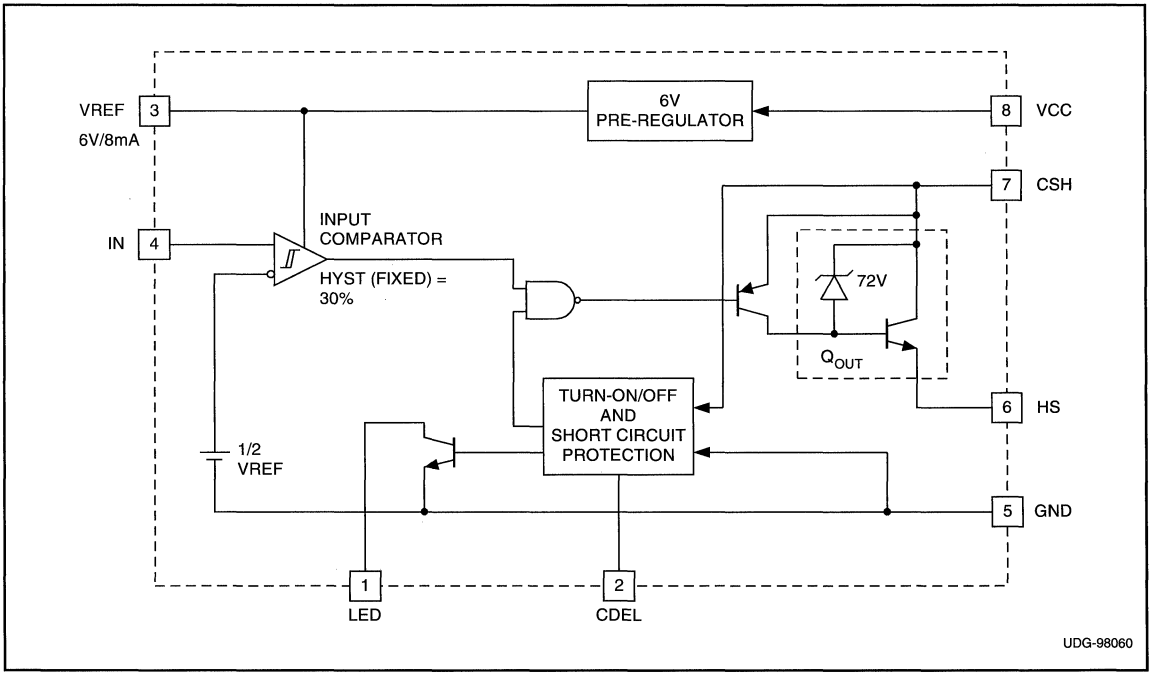
UC37132 BLOCK DIAGRAM



UC37131 BLOCK DIAGRAM



UC37133 BLOCK DIAGRAM

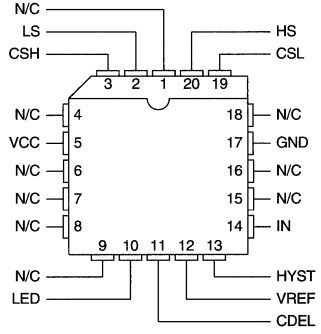


ABSOLUTE MAXIMUM RATINGS

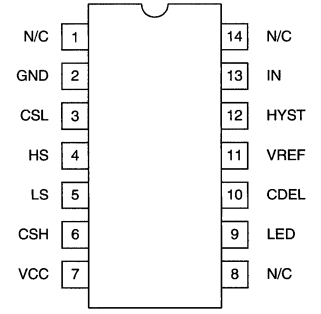
VCC 65V
LS – HS (Clamped by internal circuitry) 78V
CSH, LED 65V
Output Current
  Continuous 400mA
  Peak 900mA
Remaining Pin Voltages . . . . . –0.3V to 9V
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

PLCC-20 (Top View)
(for UCX7132)
L Packages

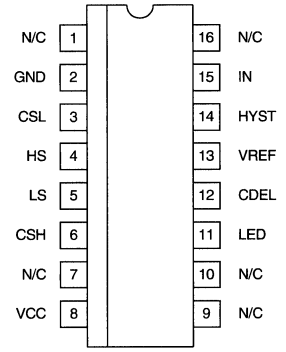


DIL-14 (Top View)
(for UCX7132)
J, or N Packages

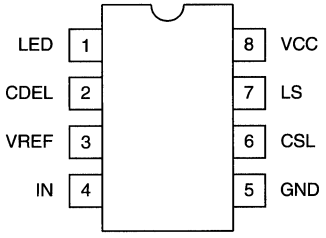


CONNECTION DIAGRAMS

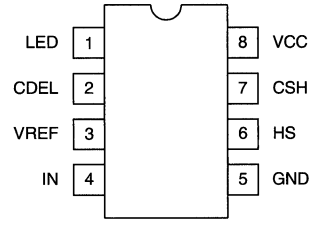
SOIC-16 (Top View) (for UCX7132)



DIL-8, SOIC-8 (Top View)
(for UCX7131)
J, N, or D Packages



DIL-8, SOIC-8 (Top View)
(for UCX7133)
J, N, or D Packages



PRODUCT SELECTION TABLES

PART NUMBER	CONFIGURATIONS	PACKAGE PIN COUNT
UCX7131	Low Side Only	8
UCX7132	Low Side or High Side	14, 16, 20
UCX7133	High Side Only	8

PART NUMBER	TEMPERATURE RANGE	AVAILABLE PACKAGES
UC1713X	–55°C to +125°C	J, L
UC2713X	–40°C to +85°C	D, N
UC3713X	0°C to +70°C	D, N

ELECTRICAL CHARACTERISTICS Unless otherwise specified, CDEL = 10nF, VCC = 25V, CSL = GND, CSH = LS; R_{CSH} = 0.5Ω (Note 1); IN=0V (for OFF condition) and IN=5V (for ON condition); $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference					
VREF	25°C	5.8	6	6.2	V
	–55°C to 125°C	5.6	6	6.4	V
Line Regulation	VCC = 8V to 64V		10	35	mV
Load Regulation	0 < I_{REF} < 8mA		10	50	mV
Short Circuit Current	REF = 0V		20	35	mA
Input Comparator					
Turn-On Threshold Voltage		2.7	3	3.3	V
Input Bias Current	V_{IN} = 3.5V			5	µA
Hysteresis	R_{HYST} = GND (Internally for X31, X33)	0.775	0.9	1.025	V
	R_{HYST} = 96.67k for (X32)		30		mV
Output: High Side (UCX7133: CSH = LS and CSL = GND Internally; See Fig. 2a)					
Rise Time (Off to On)	R_{LOAD} = 250Ω to GND		30	80	V/µs
Fall Time (On to Off)	R_{LOAD} = 250Ω to GND		30	80	V/µs
Output Short Circuit	HS = 0.25Ω to GND	500		900	mA
Voltage Clamp	LS–HS	67	72	77	V
Saturation Voltage	25°C, R_{LOAD} = 100Ω to GND			1.2	V
	–40°C, R_{LOAD} = 100Ω to GND			1.3	V
	–55°C, R_{LOAD} = 100Ω to GND			1.4	V
Leakage Current				5	µA
Output: Low Side (UCX7131; CSH = VCC and CSL = HS Internally; See Fig. 2b)					
Rise Time (On to Off)	R_{LOAD} = 250Ω to VCC, R_{CSL} = 0.5Ω		15	50	V/µs
Fall Time (Off to On)	R_{LOAD} = 250Ω to VCC, R_{CSL} = 0.5Ω		25	60	V/µs
Output Short Circuit	LS = 0.25Ω to VCC	500	700	900	mA
Voltage Clamp	LS–HS	67	72	77	V
Saturation Voltage	25°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.2	V
	–40°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.3	V
	–55°C, R_{LOAD} = 100Ω to VCC, R_{CSL} = 0.5Ω			1.4	V
Leakage Current				5	µA
VCC Fault Section					
Output Turn-On Delay, $t_{D(ON)}$	Step VCC from 0V to 8V (See Fig. 3a)	9.5	11	13.5	ms
Output Turn-Off Delay, $t_{D(OFF)}$	Pulse VCC from 25V to VCC Turn-Off Threshold	300	500	700	µs
VCC Turn-Off Threshold	Pulse VCC Low	6.5	7	7.5	V
CDEL Section					
V_{CDEL_MAX}			5.8		V
V_{FAULT_H}			4.9		V
V_{FAULT_L}			1.0		V
Overcurrent Fault Section (See Fig. 3c)					
Short Circuit Turn-Off Delay, t_{SC}	Step I_{LOAD}: 0mA to 400mA		75		µs
Short Circuit Recovery Time, t_{ROFF}	I_{LOAD} = 400mA, 100µs		10		ms
High Side Current Threshold, I_{TH-H}	R_{CSH} = 0.5Ω	250	325	400	mA
Low Side Current Threshold, I_{TH-L}	R_{CSL} = 0.5Ω	250	325	400	mA
Overcurrent Duty Cycle	R_{LOAD} = 0.25Ω to GND	0.6	0.8	1.0	%

ELECTRICAL CHARACTERISTICS Unless otherwise specified, CDEL = 10nF, VCC = 25V, CSL = GND, CSH = LS; R_{CSH} = 0.5Ω (Note 1); IN=0V (for OFF condition) and IN=5V (for ON condition); $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LED Output					
I_{SINK}, t_{DOFF}, t_{ROFF}	V_{LED} = 7V	5.0	8.0	11.0	mA
$I_{LEAKAGE}$			1	5	µA
Overall					
Delay to Output			3	6	µs
ICC	Output Off		2.0	2.8	mA
	I_L = 1mA, 250mA (High Side)		2.3	3	mA
	I_L = 1mA, 250mA (Low Side)		2.5	4	mA

Note 1: All test conditions are for a high side configuration as in Fig. 2a, unless otherwise specified.

PIN DESCRIPTIONS

CDEL: A capacitor connected to this pin is used to program both VCC pulse interruption time and power turn-on delay. The capacitor discharge time corresponds to VCC interruption and the charge time to VCC turn-on delay. The ratio between turn-on delay and turn-off delay will be fixed based on internal charge and discharge currents and voltage thresholds.

The same fault circuitry and capacitor is used for short circuit and overload protection. If an overcurrent or short circuit is detected, the capacitor starts charging and turns off the output if the condition persists at the end of its charge time. The output will then operate in a low-duty cycle mode to protect the IC. After short circuit recovery, the output will be reactivated in order to check if the short circuit was removed. If the overcurrent persists the chip will continue in this pulsing mode.

CSH: (For UC37132 and UC37133) This high side current sense pin is used to program the current limit for high side applications by connecting a resistor between VCC and CSH. An over load current is detected when the voltage drop between VCC and CSH exceeds 150mV. For the UC37132, in a high side application, the CSH pin must be tied to the LS pin; in a low side application, the CSH pin must be tied to VCC

CSL: (For UC37131 and UC37132) This low side current sense pin is used to program the current limit for low side applications by connecting a resistor between CSL and GND. An over load current is detected when the voltage drop between CSL and GND exceeds 150mV. For the UC37132, in a high side application, the CSL pin must be tied to GND; in a low side application, the CSL pin must be tied to the HS pin.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

HS: (For UC37132 and UC37133) The output of the switching transistor in the high side configuration. The emitter of the output transistor is the HS pin which is connected to the load. For the UC37132, the HS pin must be tied to the CSL pin in a low side application.

HYST: (For UC37132) The pin used to program the input comparator hysteresis by connecting a resistor to ground. The hysteresis defaults to 30% with HYST grounded (internally for UC37131 and UC37133).

$$V_{HYST} = \frac{3000}{(3330 + R_{HYST})}$$

IN: The input to the comparator that detects when the output transistor should be turned on. The input threshold is 3.0V (1/2 VREF) and the input voltage range is 0V to VREF.

LED: Open collector output intended to drive an LED. This pin is driven low whenever the output is turned off and is externally pulled high when the output is turned on (see Fig. 3b and 3c).

LS: (For UC37131 and UC37132) The output of the switching transistor in the low side configuration. The collector of the output transistor is the LS pin which is connected to the load. For the UC37132, the LS pin must be tied to the CSH pin in a high side application.

VREF: The 6V regulated reference capable of supplying up to 8mA. The recommended decoupling capacitor is 1nF.

VCC: The supply voltage for the chip. Decouple this pin with a good quality ceramic capacitor to ground.

DESCRIPTION OF OPERATION

Reference

The UC37131/2/3 family of devices features a 6V bandgap reference that is used to bias on-chip logic. Although the 6V reference is not trimmed, this bandgap reference provides less than 200ppm/°C. It is also used to generate the on-chip 3V input comparator threshold and is needed for the programmable hysteresis. The on-chip reference has 8mA maximum current sourcing capacity that is designed to power up external circuitry.

Input Comparator

The input comparator is a high gain comparator with hysteresis that fully switches with either a small signal (30mV, minimum for 1% hysteresis) or a logic signal (0 to 6V max). Only a 5mV overdrive of the 3V threshold is needed to switch the driver.

The hysteresis is set to 30% on the UC37131 and UC37133. (This is 30% of 3V equating to 0.9V of hysteresis.) On the UC37132 it is programmable from 1% to 30%.

Fault Logic

The output of the comparator is logic ANDed with the output of the fault logic. If a fault, either a power interrupt or an overcurrent condition, persists longer than it takes for the CDEL to discharge from its V_{CDEL_MAX} level of 5.8V to its V_{FAULT_L} of 1.3V, the fault protection block will output a logic 0 to the NAND gate and turn off the output driver. If the fault goes away prior to CDEL being discharged to 1.3V, the chip will resume normal operation without going through a turn-on delay.

The power interrupt normal operation consists of the chip turning the driver immediately back on if the interrupt goes away prior to CDEL reaching its lower threshold as described above. The CDEL capacitor is chosen based upon the maximum power interrupt time (t_{INT}) allowed without the output experiencing a turn-on delay. This interrupt time must be less than $t_{D(OFF)}$ where $t_{D(OFF)}$ is equal to the time it takes the CDEL capacitor to discharge from V_{CDEL_MAX} (5.8V) to V_{FAULT_L} (1.3V) with a discharge current of approximately 94µA. If the power stays off only as long as $t_{D(OFF)}$, the minimum power up delay will be equal to the time it takes to charge CDEL from V_{FAULT_L} (1.3V) to V_{FAULT_H} (4.9V) with a charge current of approximately 4µA. If the power stays off longer than this time, then a power up delay will be initialized once power is resumed. This delay is the time it takes for CDEL to charge from 0V to V_{FAULT_H} of 4.9V.

The overcurrent fault normal operation consists of the chip staying off until CDEL fully recharges to V_{FAULT_H} of 4.9V. This is $t_{R(OFF)}$. Once CDEL reaches 4.9V, the driver will turn back on. If the overcurrent fault is still present, the chip will operate in a very low duty cycle (approximately 0.7%) based on the discharge (driver on) and charge time (driver off) of the CDEL capacitor. This overcurrent timing makes the chip act "smart" by allowing very high currents needed to drive large capacitive loads without setting off an overcurrent fault.

The overcurrent and current limit thresholds are programmed with the resistor R_{CSH} from CSH to VCC (high side) or R_{CSL} from CSL to GND (low side). For example, a 150mV ($I_{LOAD} \bullet R_{CSH}$) threshold will set the high side overcurrent fault threshold. An overall short circuit protection threshold is set at 300mV. Therefore, the recommended R_{CSH} of 0.5Ω will result in the 600mA short circuit. By changing the R_{CSH} value the user can optimally set the overcurrent and short circuit current limits.

Output Driver

Once the turn-on signal is gated through from the input comparator, the output transistor is turned on. The output drive transistor is a composite PNP, NPN structure. This is a specially designed structure that keeps all the drive current needed for the load to be sourced through the LS pin. This keeps the overall power dissipation to less than 4mA independent of the load.

The output driver also has a 72V zener diode wired between its base and collector. This allows the output to swing and clamp to 72V above ground when discharging an inductive load in a low side application. The inductive zener clamp can discharge the 250mA to 400mA full load current. This consequently allows the LS pin to safely swing above VCC. Similarly, the 72V zener diode will allow the HS pin to safely swing and clamp 72V below LS/VCC when discharging an inductive load in a high side application. This 72V zener diode simplifies the user application by eliminating the need for external clamp diodes.

APPLICATION INFORMATION

Choosing The CDEL Capacitor

The maximum amount of time that VCC power can be interrupted and not require the outputs to go through a turn-on delay cycle is user programmable by the CDEL capacitor value. While VCC is interrupted, the outputs will be in an indeterminate state and they may turn off during this interval, t_{INT}. However, as long as the programmed interruption time is not exceeded, the outputs will immediately turn back on with the return of VCC.

For example:

$t_{INT} \approx 500\mu s$ (User specified)

CDEL is selected such that the time it takes for this capacitor to discharge from V_{CDEL_MAX} (5.8V) to V_{FAULT_L} (1.3V) with a discharge current of 94µA is just greater than this t_{INT}. This time is referred to as $t_{D(OFF)}$ in Fig. 3b.

$$CDEL = \frac{I_{DISCHARGE} \bullet t_{D(OFF)}}{V_{CDEL\_MAX} - V_{FAULT\_L}}$$

If $t_{D(OFF)}$ is set equal to t_{INT}, which the user has selected to be 500µs, the minimum CDEL capacitor is calculated:

$$CDEL = \frac{94\mu A \bullet 500\mu s}{5.8V - 1.3V}$$

For this application, the CDEL capacitor value calculates to 10.4nF. By using a 10nF capacitor on CDEL, VCC can be interrupted for up to 478µs and the outputs will experience an indeterminate state during this interruption, but resume normal operation when VCC power returns to normal.

If the VCC power is interrupted for a time equal to or longer than $t_{D(OFF)}$ then the following relationships apply. As the CDEL capacitor discharges past the V_{FAULT_L} threshold, the output is fully disabled and must cycle through a power up delay equal to $t_{D(ON)}$. The charge current for the CDEL capacitor is equal to 4µA. The outputs will turn on when the CDEL capacitor charges up to the V_{FAULT_H} threshold of 4.9V. The minimum turn-on delay the outputs will experience will occur if t_{INT} is exactly equal to the $t_{D(OFF)}$ time and the CDEL capacitor has only discharged to V_{FAULT_L}. This would be the minimum turn-on delay time and is calculated with the following equation:

$$t_{D(ON)_{min}} = \frac{CDEL \bullet \left| V_{FAULT\_L} - V_{FAULT\_H} \right|}{I_{CHARGE}}$$

Using the 10nF CDEL capacitor, for example, the minimum turn-on delay calculates to 9ms. If the CDEL capacitor discharges completely to zero, then the 10nF CDEL capacitor would cause a turn-on delay of 12.25ms. The outputs would be off for this amount of time after VCC power is restored. The total amount of time the outputs could be disabled is equal to the t_{INT} time, which may include the indeterminate time of $t_{D(OFF)}$, and the $t_{D(ON)}$ time, as shown in Fig. 3b.

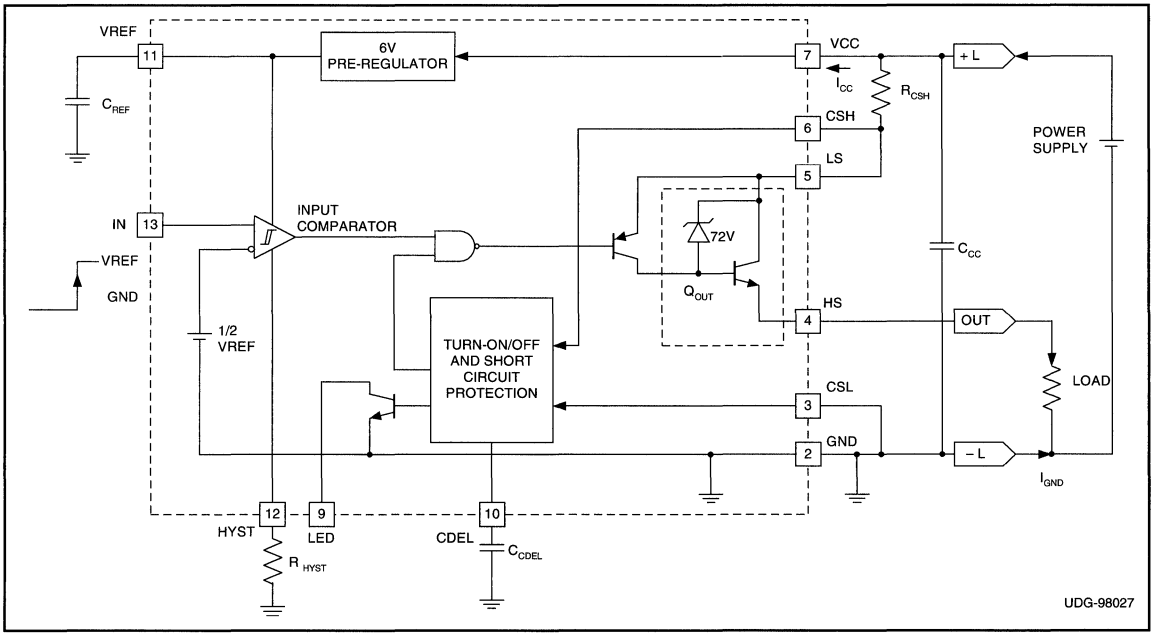


Figure 2a. High side application.

APPLICATION INFORMATION (cont.)

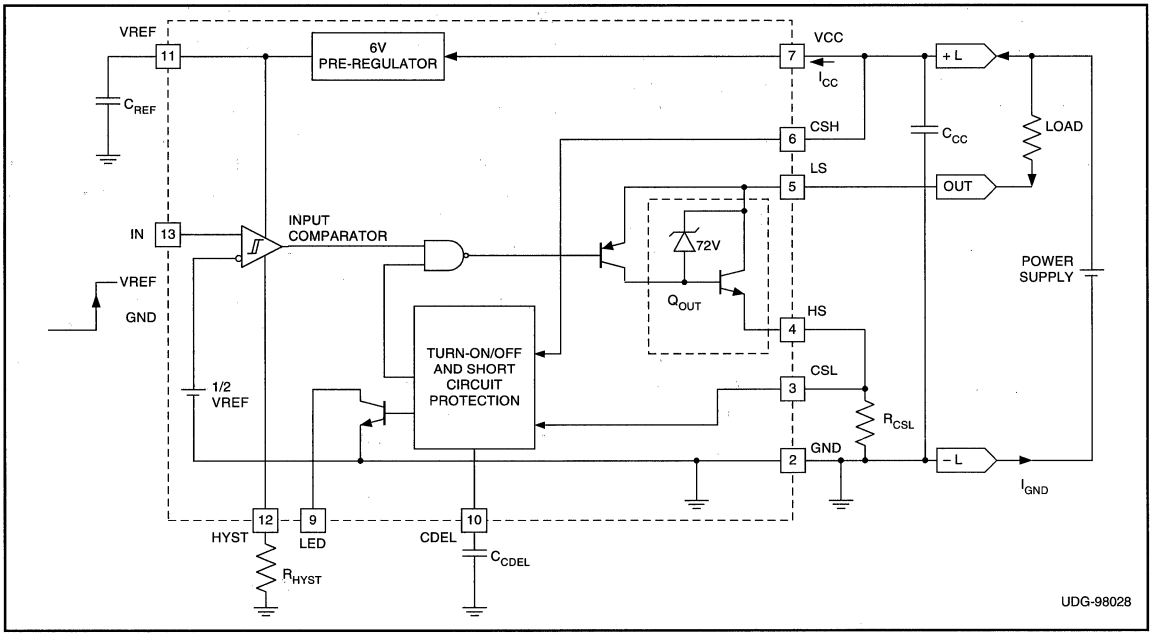


Figure 2b. Low side application.

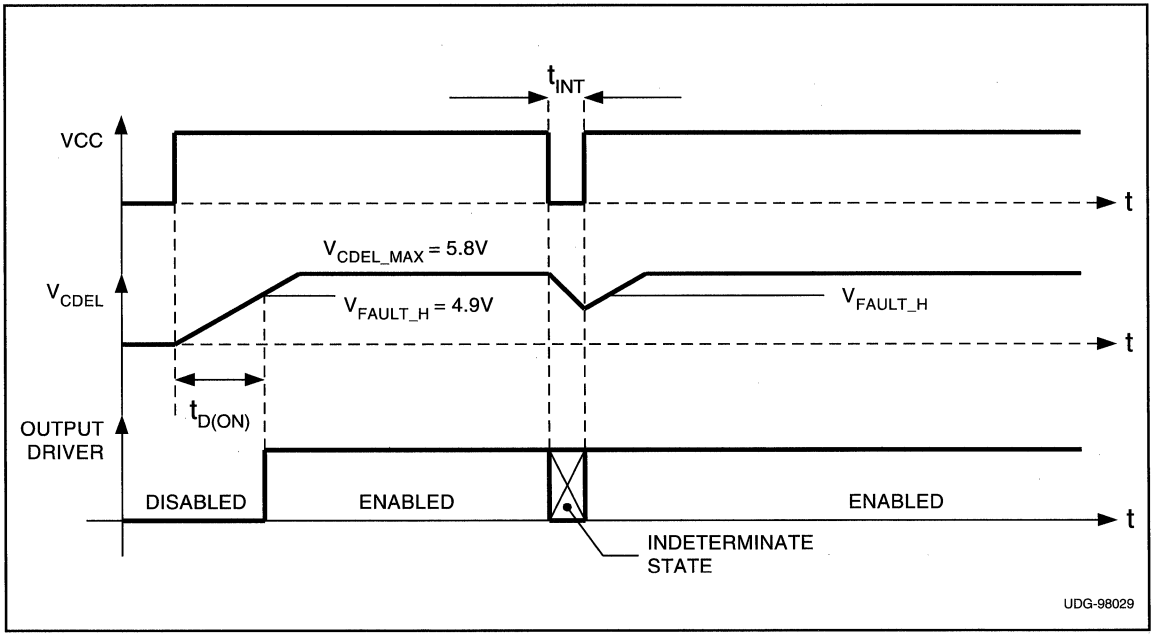


Figure 3a. Power interrupt ignore operation, high side configuration, V_{IN} = 5VDC.

APPLICATION INFORMATION (cont.)

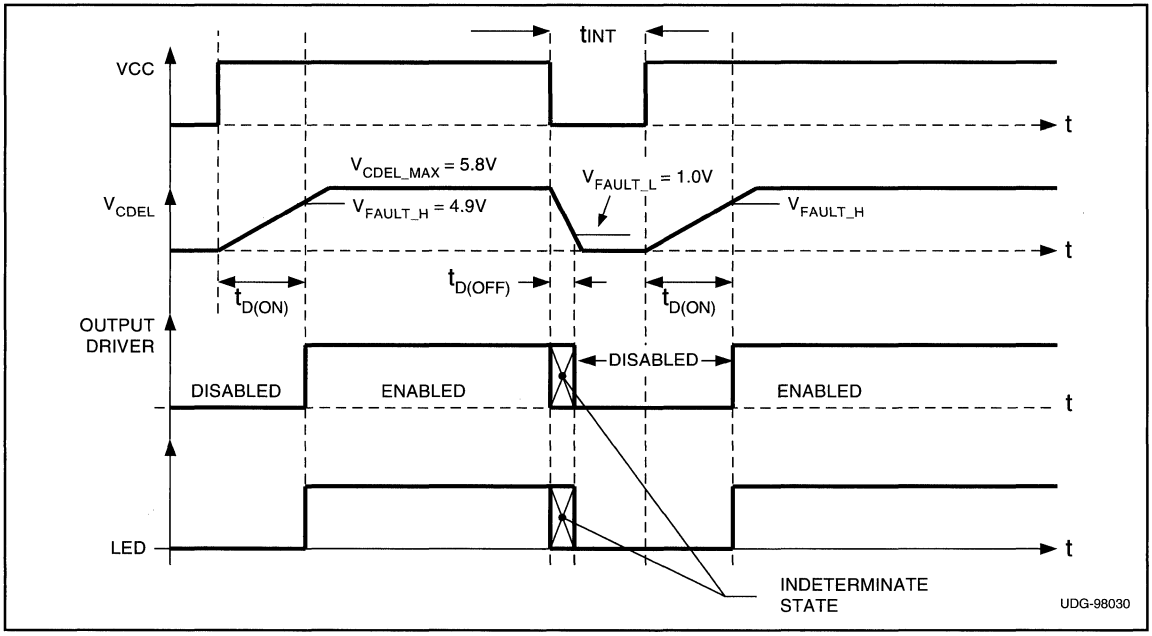


Figure 3b. Power interrupt fault operation, high side configuration, V_{IN} = 5VDC.

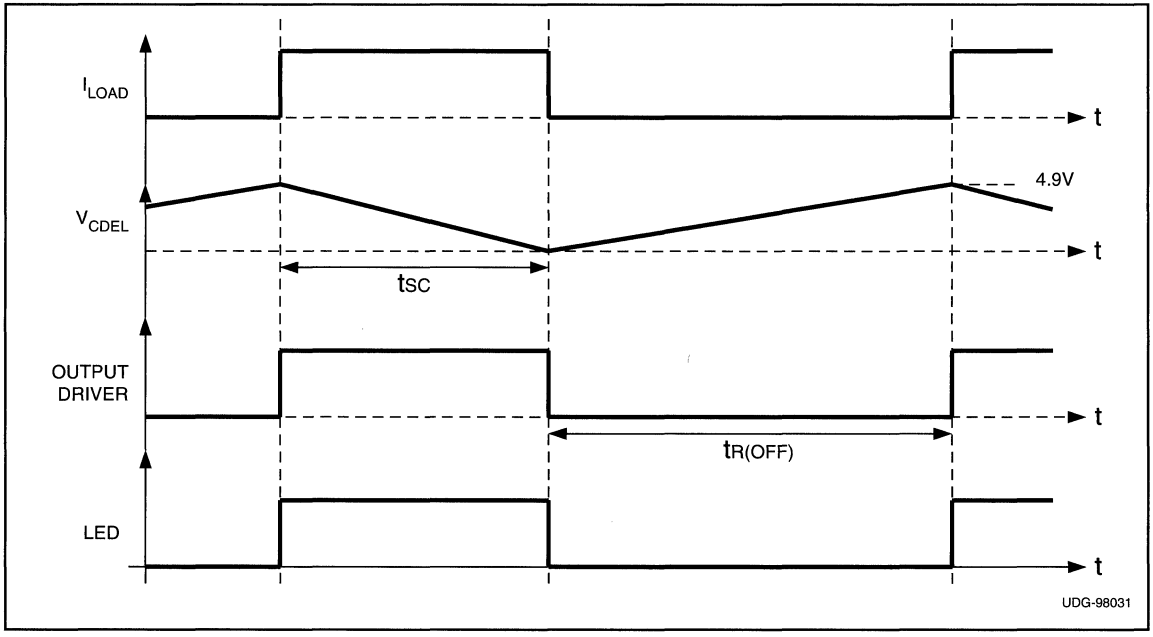


Figure 3c. Overcurrent fault operation.

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application INFO available

UCC2750
UCC3750

Source Ringer Controller

PRELIMINARY

FEATURES

- Provides Control for Flyback Based Four Quadrant Amplifier Topology
- Onboard Sine Wave Reference with Low THD
- Selectable Ringing Frequency for Different Phone Systems (20Hz, 25Hz and 50Hz)
- Programmable Output Amplitude and DC Offset
- DC Current Limiting for Short Circuit Protection
- Secondary Side Voltage Mode Control
- Operates from a Single 5V Supply

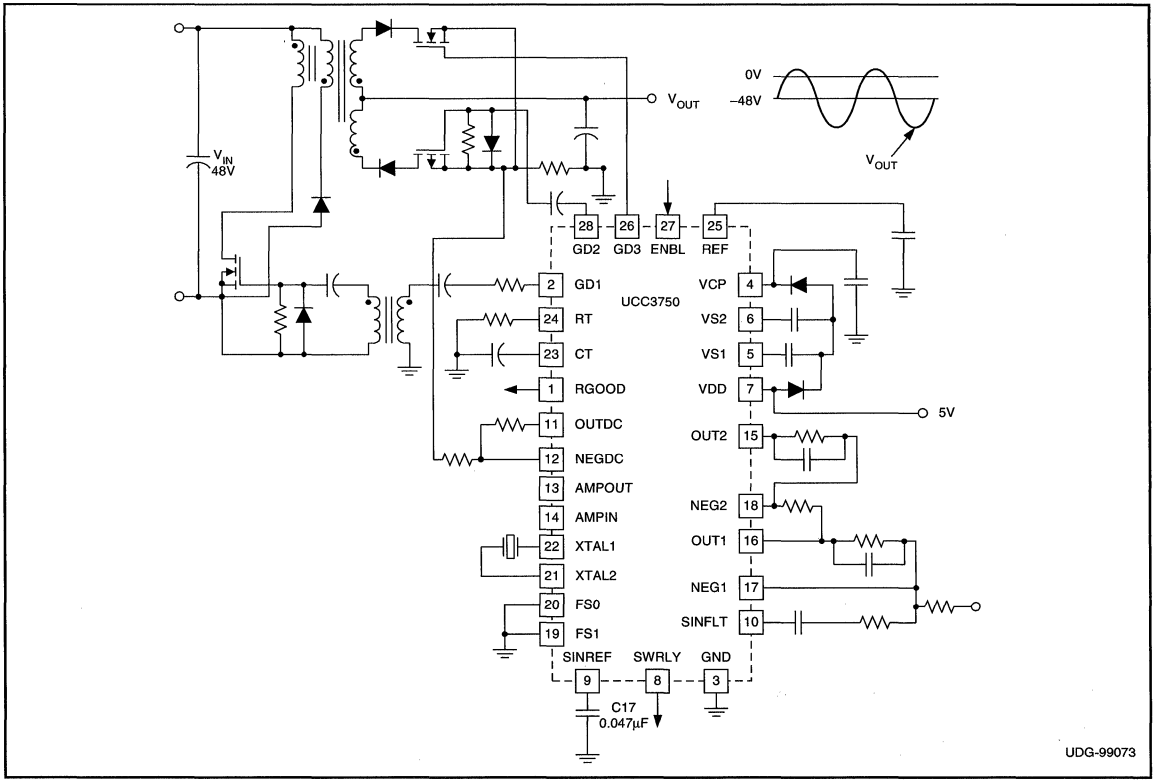
DESCRIPTION

The UCC3750 Source Ringer Controller provides a complete control and drive solution for a four quadrant flyback-based ring generator circuit. The IC controls a primary side switch, which is modulated when power transfer is taking place from input to output. It also controls two secondary switches which act as synchronous rectifier switches during positive power flow. These switches are pulse-width-modulated when the power is being delivered back to the source.

The UCC3750 has an onboard sine wave reference with programmable frequencies of 20Hz, 25Hz and 50Hz. The reference is derived from a high-frequency (32kHz) crystal connected externally. Two frequency-select pins control an internal divider to give a sinusoidal output at 20Hz, 25Hz or 50Hz. The ring generator can also be used at other frequencies by supplying externally generated sine-waves to the chip or by clocking the crystal input at a fixed multiple of the desired frequency.

Other features included in the UCC3750 are programmable DC current limit (with buffer amplifier), a charge-pump circuit for gate drive voltage, internal 3V and 7.5V references, a triangular clock oscillator and a buffer amplifier for adding programmable DC offset to the output voltage. The UCC3750 also provides an uncommitted amplifier (AMP) for other signal processing requirements.

TYPICAL APPLICATION



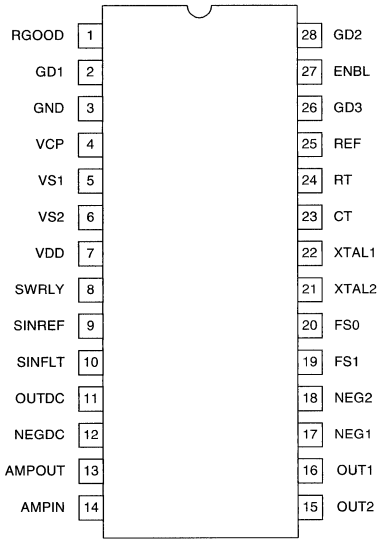
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage
VDD 7.5V
Maximum Forced Voltage
VCP ..... –0.3V to 13.2V
VS1, VS2..... –0.3V to 5V
OUT1, OUT2, AMPOUT, OUTDC
Maximum Forced Voltage ..... –0.3V to 7.5V
Maximum Forced Current..... Internally Limited
NEG1, NEG2, AMPIN, NEGDC
Maximum Forced Voltage ..... –0.3V to 7.5V
SINREF, SINFLT
Maximum Forced Voltage ..... –0.3V to 7.5V
Logic Inputs
Maximum Forced Voltage ..... –0.3V to 7.5V
Reference Output Current (REF) ..... Internally Limited
Output Current (GD1, GD2, GD3)
Pulsed..... 1.5A
Storage Temperature ..... –65°C to +150°C
Junction Temperature..... –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.)..... +300°C

Unless otherwise indicated, voltages are reference to ground and currents are positive into, negative out of the specified terminal. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500ns. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-28, SOIC- 28 (Top View)



ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, C_{REF} = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Supply					
Supply Current - Active	With 12V Supplied to V_{CP} and Charge Pump Disabled		0.5	1	mA
Internal Reference w/External Bypass					
Output Voltage (REF)		7.3	7.55	7.8	V
Load Regulation	I_{REF} = 0mA – 2mA		30	60	mV
Line Regulation	VCP = 10V to 13V, I_{REF} = 1mA		3	15	mV
Amplifier					
Input Voltage	Error, DC Offset and Amp Amplifiers	2.9	3	3.1	V
	DC Limit Amplifier	0.7125	0.75	0.7875	V
Input Bias Current			500	600	nA
AVOL	V_{OUT} = 2V to 4V		70		dB
VOH	Source 100µA	5.35	6	7.0	V
VOL	Sink 100µA		0.2	0.65	V
Short Circuit Current	V_{IN} = 0V and 5V with V_{OUT} = 0V and 5V	0.5	2	3	mA
Sine Reference					
Accuracy	T_J = 25°C, Program Frequency–Reference Frequency	–1	0	1	Hz
Total Harmonic Distortion	(Note 1)			2	%
Amplitude	Peak	0.475	0.5	0.525	V
Offset		2.85	3.0	3.15	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C for the UCC3750, –40°C to +85°C for the UCC2750, RT = 14k, CT = 470pF, C_{REF} = 0.1µF, FS0 = 0, FS1 = 0, VDD = 5V. $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Accuracy		108	128	148	kHz
Peak Voltage		4.6	4.75	4.9	V
Valley Voltage		2.9	3.05	3.2	V
Charge Pump					
Switch Pull Up Resistance (VS1, VS2)			10	30	Ω
Switch Pull Down Resistance (VS1, VS2)			10	30	Ω
Output Voltage (VCP)	VDD = 5V, I_{VCP} = 10mA	11	12	14	V
Output Drivers					
Pull Up Resistance			9	15	Ω
Pull Down Resistance			9	15	Ω
Rise Time	CL = 2.7nF		50	100	ns
Fall Time	CL = 2.7nF		50	100	ns
Current Limit					
DC Limit Threshold Voltage Positive	R5/R6 = 3	0.4	0.5	0.6	V
DC Limit Threshold Voltage Negative	R5/R6 = 3	–0.6	–0.5	–0.4	V
Duty Cycle					
Maximum PWM Duty Cycle		48	50		%
Rectifier Duty Cycle			50		%

Note 1: Guaranteed by measuring the steps of the PWL Sine Wave.

STATE	% VCC	VALUE FOR REF = 7.5	STATE	% VCC	VALUE FOR REF = 7.5
0	0.3333	2.5	5	0.4255	3.191
1	0.3384	2.538	6	0.4471	3.353
2	0.3528	2.646	7	0.4616	3.462
3	0.3745	2.808	8	0.4666	3.5
4	0.4	3			

PIN DESCRIPTIONS

AMPIN: Inverting input of the uncommitted amplifier.

AMPOUT: Output of the uncommitted amplifier.

CT: This pin programs the internal PWM oscillator frequency. Capacitor from CT to GND sets the charge and discharge time of the oscillator.

ENBL: Logic input which enables the outputs and the charge pump when high. ENBL should be pulled low to turn the outputs off.

FS0, FS1: Frequency select pins for the internal sine-wave generator. Table 1 provides the SINREF frequencies as a function of FS0 and FS1 when a 32kHz crystal is used at the crystal inputs (XTAL1, XTAL2). Other proportional frequencies can be obtained with a different crystal. Inputs FS0 and FS1 are TTL compatible.

Table I. Frequency selection table (for 32kHz crystal).

FS0	FS1	SINREF (Hz)
0	0	20
1	0	25
0	1	50
1	1	High Impedance

GD1: Output driver that controls the primary side switch in a flyback converter through a gate drive transformer. The output signal on this pin is PWM during positive power transfer modes and zero during negative power transfer modes.

PIN DESCRIPTIONS (cont.)

GD2: Output driver that controls the p-channel secondary side switch in the flyback converter. The output signal on this pin is PWM during mode 4 (Fig. 2) when the reference signal is negative and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 1 with positive reference signal and positive power transfer. This output is logically inverted to provide the correct polarity drive signal for a p-channel switch.

GD3: Output driver that controls the n-channel secondary side switch in the flyback converter. The output signal on this pin is PWM during mode 2 (Fig. 2) when the reference signal is positive and power is being returned to the input. This pin functions as a synchronous rectifier output during mode 3 with a negative reference signal and positive power transfer.

GND: Reference point for the internal reference and all thresholds. Also provides the signal return path for all other pins.

NEG1: Inverting input of the buffer amplifier that acts as a summing junction for the DC (battery) offset voltage and sinewave reference.

NEG2: Inverting input of the error amplifier where the ringer output voltage and the reference signal with the desired offset are applied with a weighted sum. Feedback compensation is connected between NEG2 and OUT2.

NEGDC: Inverting input of the amplifier used for DC current limiting.

OUT1: Output of the buffer amplifier that provides scaling and filtering for the reference signal before feeding it into the error amplifier. This output is also used internally to select the PWM mode for the flyback converter.

OUT2: Output of the error amplifier. Used to connect compensation components. This output's absolute value determines the duty cycle of the PWM pulse. The polarity of this signal also determines the PWM mode.

OUTDC: Output of the DC current limit amplifier. The DC current limit is activated when this pin is above 4.5V or below 1.5V.

REF: Internal 7.5V reference. For best results, bypass to GND with a ceramic capacitor(>0.1μF).

RGOOD: Logic output that indicates that the error amplifier output is within range (0< D< 0.5). This pin can source upto 0.5mA of current.

RT: Resistor from RT to GND helps set the oscillator frequency. RT programs the charge and discharge currents of CT.

SINFLT: This signal is the buffered version of SINREF. This signal is summed with the DC offset level with appropriate scaling.

SINREF: This pin is the output of the sine-wave reference generator. It has a high output impedance (≈25kΩ). A 0.01μF capacitor to GND is recommended to provide smoothing of the sinewave. When FS0 and FS1 are both set high, the sine reference generator is disabled allowing this pin to accept an external sinewave input.

SWRLY: Logic output that leads the battery offset crossings (by typically 5ms) to allow "zero voltage" relay switching. This pin can typically source 250μA.

XTAL1: Crystal connection for external crystal. This pin can be also used to clock the internal sine wave generator when XTAL2 is connected to VDD/2.

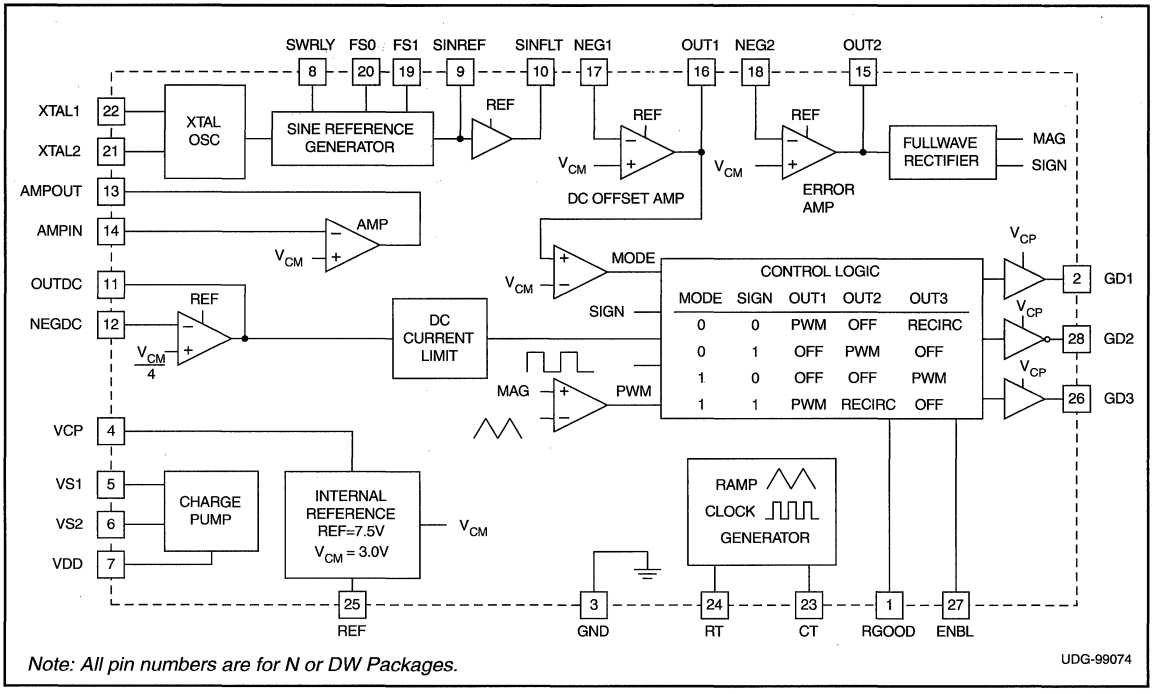
XTAL2: Crystal connection for external crystal.

VCP: External connection for charge pump storage capacitor. A capacitance ≥2.2mF is recommended for low charge pump output ripple. The voltage at this pin is used by the output drivers for gate drive voltages. Alternatively, a regulated gate drive voltage (>10V) can be connected at this pin while leaving the charge pump circuit at nodes VS1, VS2 disconnected.

VDD: External supply input used to bias internal logic functions. Typically a regulated 5V supply is connected between this pin and GND. It also is the input voltage for the voltage tripler circuit to generate the gate drive voltage.

VS1, VS2: Voltage switches for the voltage tripler (charge pump circuit). They provide different voltage

DETAILED BLOCK DIAGRAM



Note: All pin numbers are for N or DW Packages.

UDG-99074

APPLICATION INFORMATION

The UCC3750 provides complete control and protection functions for a four quadrant flyback converter used to generate ring signals for telephone circuits. A typical application circuit for a 15 REN ring generator is shown in Fig. 1.

As shown, the flyback converter takes a DC input (typically 48V) and provides an isolated output with a programmable frequency (and amplitude) AC signal superimposed on a programmable DC offset. The power path consists of a primary side PWM switch Q1, primary return rectifier DR1, a 4-winding transformer T1, output rectifiers DR2 and DR3, synchronous/PWM switches Q2 and Q3, and output filter CF. Resistor RSENSE provides the output current sensing for protection circuits.

Different operating modes of the converter are depicted in Table 2. Fig. 2 shows the output voltage and current waveforms for a purely capacitive load and identifies the four operating modes. Fig. 3 shows the PWM waveforms for the circuit and Fig. 4a - 4d show the equivalent circuits under the operating modes. The addition of Q2, Q3 and primary diode facilitates true four quadrant operation where both the output voltage and power transfer can be bi-directional. Mode 1 is similar to the commonly used DC-DC converter operation where Q1 is modulated with the PWM signal and rectification is provided through the Q2, DR2 path to provide a positive output proportional to the increasing, positive reference voltage. The pulse-width is controlled by the error amplifier output to increase or decrease the output as dictated by the reference. The maximum duty cycle is limited to 50% to prevent DR1 from turning on prior to Q2/DR2.

In mode 2, the reference begins to decrease, necessitating that the power transfer back to the input. For this mode, switch Q3 needs to be modulated while DR1 acts as the rectifier back to the input. The UCC3750 has mode decoding circuitry which automatically directs the PWM signal to Q3 and turns off Q1.

Table II. Operating modes.

Mode	Reference Polarity	Power Flow	E.A. Output	Source (PWM) Switch	Rectifier Switch
1	+	+	–	Q1	Q2
2	+	–	+	Q3	(D1)
3	–	+	+	Q1	Q3
4	–	–	–	Q2	(D1)

APPLICATION INFORMATION (cont.)

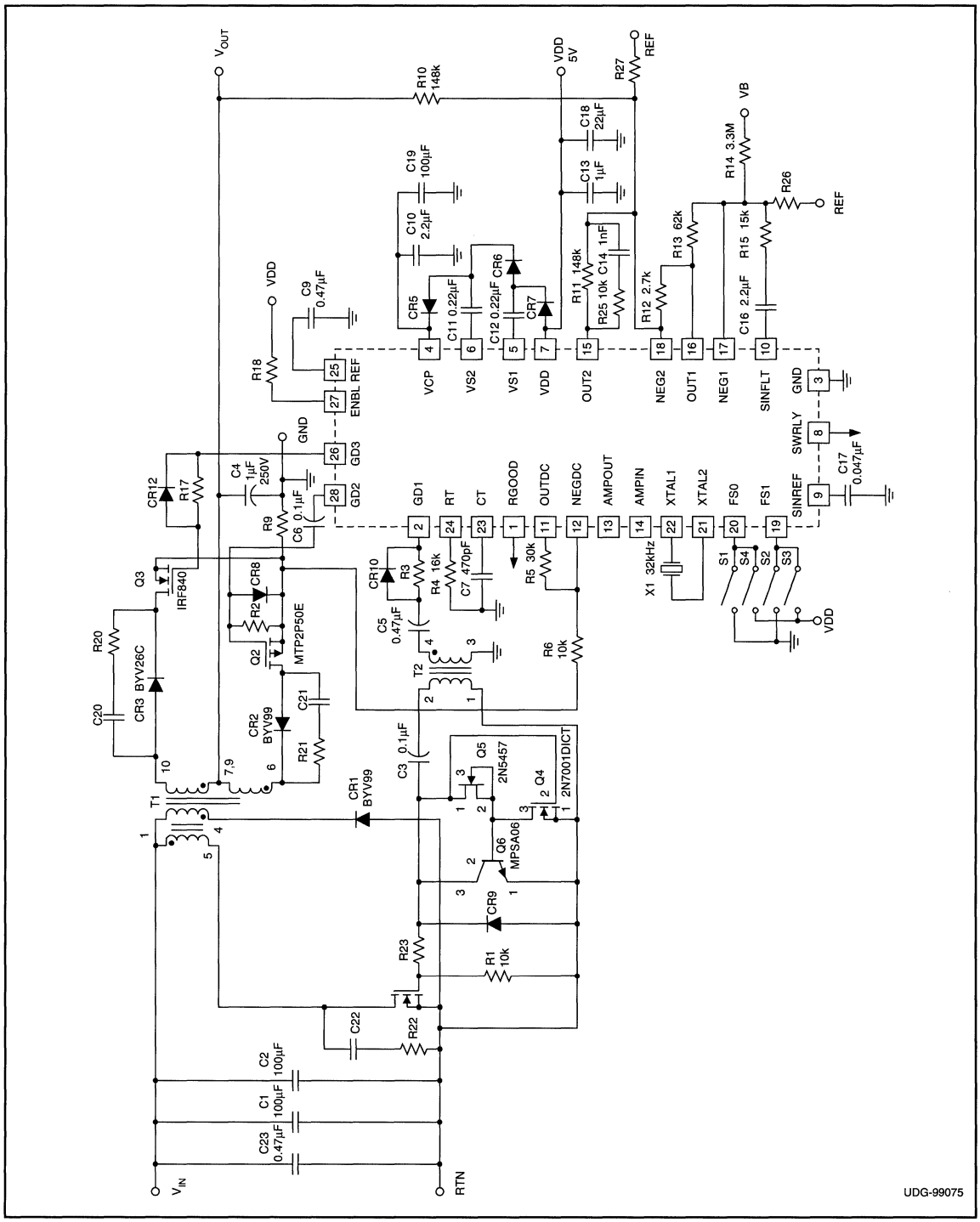


Figure 1. Typical application circuit.

APPLICATION INFORMATION (cont.)

When the reference signal goes from positive to negative, a transition is made from mode 2 to mode 3. In mode 3, the converter once again acts as a DC-DC flyback converter (with negative output). Similar to mode 1, Q1 is controlled by the PWM output, however, the rectifying path is now through Q3/DR3 as the output polarity is reversed. At the mode boundaries, there could be some distortion which won't affect the THD too much as it is near zero crossings. Finally, as the reference signal starts increasing towards zero, the direction of power transfer is again reversed and Q2 is PWMed in mode 4.

It should be noted that in modes 2 and 3 when the reference is decreasing, the phase of the feedback path is inverted compared to the other two modes. Traditional PWM methods will result in instability due to this characteristic. The UCC3750 separates the error signal magnitude and polarity and determines the correct PWM signal based on a separate mode determination circuit.

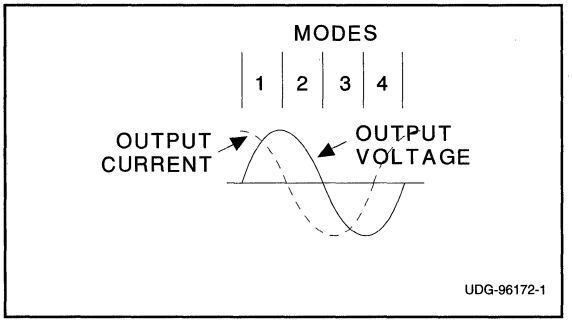


Figure 2. Operating modes.

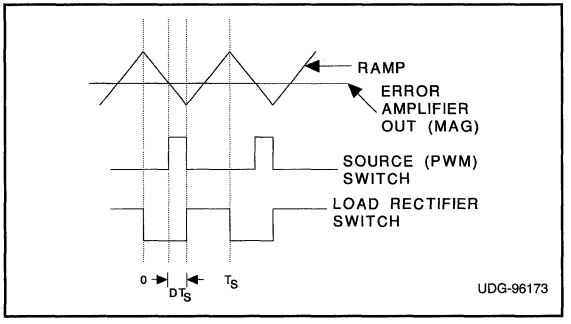


Figure 3. Circuit waveforms.

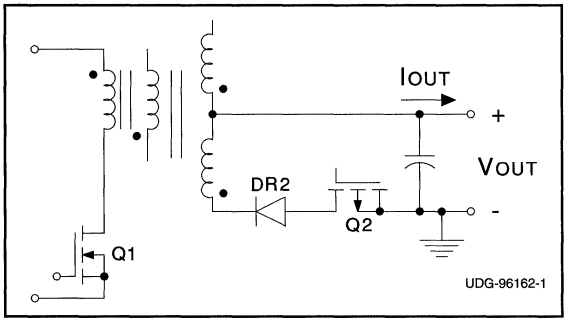


Figure 4a. Mode 1: Forward power transfer, positive output.

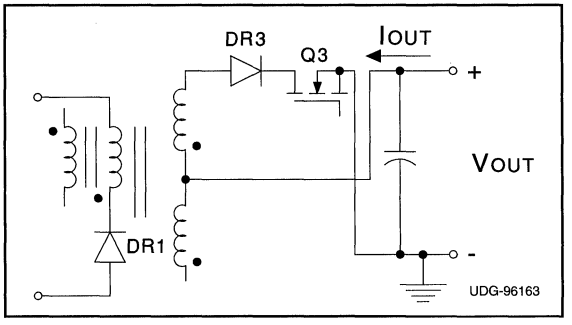


Figure 4b. Mode 2: Reverse power transfer, positive output.

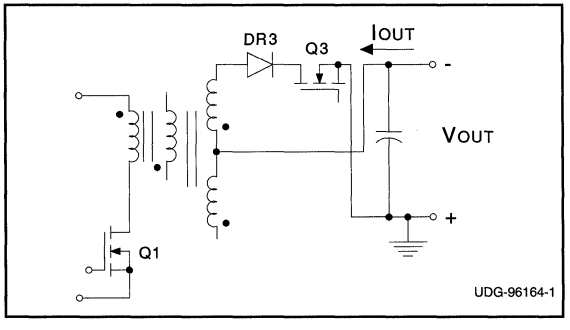


Figure 4c. Mode 3: Forward power transfer, negative output.

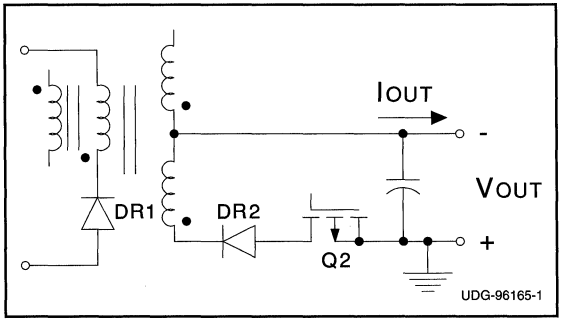


Figure 4d. Mode 4: Reverse power transfer, negative output.

APPLICATION INFORMATION (cont.)

Sine Reference Generator

The IC has a versatile low frequency sinewave reference generator with low harmonic distortion and good frequency accuracy. In its intended mode as shown in Fig. 5, the reference generator will take an input from a 32kHz crystal (connected between XTAL1 and XTAL2) and generate a sine-wave at 20Hz, 25Hz or 50Hz based on the programming of pins FS0 and FS1 (See Table 2). If the crystal frequency is changed, the output frequencies will be appropriately shifted. C-2 type Quartz crystals (Epson makes available through DigiKey) are recommended for this application. If the frequency accuracy is not a major concern, the more common and less expensive clock crystal (C-type) at 32.768kHz can be used with a minor output frequency offset (20.5Hz instead of 20Hz). Additionally, the XTAL1 input can be clocked at a desired frequency to get a different set of output frequencies at the sine-wave output (with divide ratios of 1600, 1280 and 640). The sine-wave output is centered around an internal reference of 3V. A capacitor from SINREF to GND helps provide smoothing of the sine wave reference. Recommended value is at least 0.01µF and maximum of 0.1µF. When FS0 and FS1 are both 1 (high), the sine reference is disabled and external sine-wave can be fed into the SINREF pin. This signal should have the same DC offset as the internal sine-wave (3V).

Reference and Error Amplifier

The recommended circuit connections for these circuits are shown in Fig. 6. The sine-wave is added to a DC offset to create the composite reference signal for the error amplifier. The DC reference can vary over a wide range. For pure AC outputs it is zero, while in many common applications, it is the talk battery voltage (–48V). The UCC3750 accomplishes this task by summing the two signals weighted by resisting R14 and R15. The output of AMP1 also helps determine the mode of the circuit.

Referring to Fig. 6, the output of AMP1 is given by :

$$VOUT1 = \left(1 + \frac{R13}{R14} + \frac{R13}{R26}\right) \bullet VCM - \frac{R13}{R26} \bullet REF \quad (1)$$

$$- \frac{R13}{R14} \bullet VB - \frac{R13}{R15} \bullet VAC$$

In order to nullify the effect of V_{CM} on this value, the ratio of R26 to R14 should be made 1.5. With this ratio, the equation becomes:

$$VOUT1 = VCM - \frac{R13}{R14} \bullet VB - \frac{R13}{R15} \bullet VAC \quad (2)$$

VOUT1 is the reference voltage that the second amplifier (AMP2) uses to program the output voltage. Assuming that Z4 is high DC impedance, the output voltage is derived by summing the currents into pin 18. The output is given as:

$$VO = \left(1 + \frac{R10}{R27} + \frac{R10}{R12}\right) \bullet VCM \quad (3)$$

$$- \frac{R10}{R27} \bullet REF - \frac{R10}{R12} \bullet VOUT1$$

Again, if the ratio of R27 to R10 is made 1.5, the effect of V_{CM} is nullified and the output voltage becomes (after substituting for VOUT1):

$$VO = \frac{R10 \bullet R13}{R12 \bullet R14} \bullet VB + \frac{R10 \bullet R13}{R12 \bullet R15} \bullet VAC \quad (4)$$

From equation 4, it can be seen that if the output voltage DC value has to track VB directly, the following condition should be forced:

$$R10 \bullet R13 = R12 \bullet R14 \quad (5)$$

However, in some cases, this becomes impractical due to large AC gain required form V_{AC} to V_O. Only a small part of the gain can be accommodated in the first amplifier stage due to its output voltage limitations. As a result, the required resistance values become very high. This

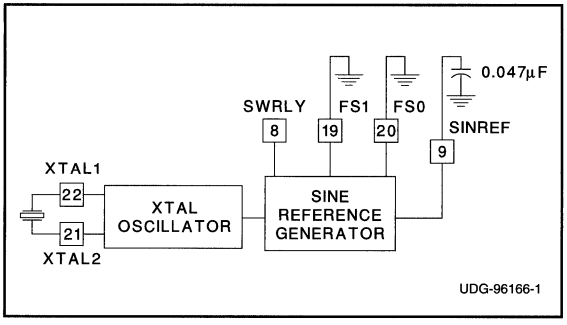


Figure 5. Sine-wave generator.

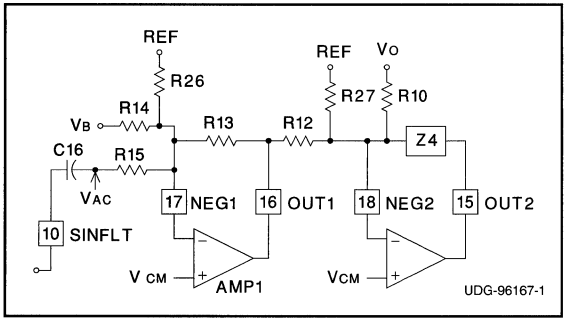


Figure 6. Error amplifier setup.

APPLICATION INFORMATION (cont.)

problem is only manifested for high values of VB (e.g. 48V) and can be alleviated by using a fraction of the required DC offset as the VB input and regaining the offset with resistive ratios.

The error amplifier compares the reference signal with the output voltage by way of weighted sum at its inverting input. The error signal is further processed to separate its polarity and magnitude. An absolute value circuit (precision full-wave rectifier) is used to get the magnitude information. The polarity is used along with the reference signal polarity to determine the mode information. The absolute value circuit provides phase inversion when appropriate for modes 2 and 3 to maintain the correct loop gain polarity. While the output of the error amplifier swings around 3V, the full-wave rectifier output (MAG) converts it into a signal above 3V. This signal is compared to the oscillator ramp to generate the PWM output.

Oscillator and PWM Comparator

The UCC3750 has an internal oscillator capable of high frequency (>250kHz) operation. A resistor on the RT pin programs the current that charges and discharges CT, resulting in a triangular ramp waveform. Fig 7. shows the oscillator hook-up circuit. The ramp peak and valley are 4.75V and 3V respectively. The nominal frequency is given by:

$$f_{OSC} = \frac{1}{1.17 \bullet RT \bullet CT}$$

The ramp waveform and the rectified output of the error amplifier are compared by the PWM comparator to generate the PWM signal. The PWM action is disabled on the positive slope of the ramp signal. Leading edge modulation turns on the PWM signal when the ramp signal falls below MAG on the falling slope and turns it off at the end of the clock cycle. This technique enables synchronized turn-on of the rectifier switches immediately after the PWM pulse is turned off. The triangular nature of the ramp ensures that the maximum duty cycle of the PWM output is 50%, providing inherent current limiting.

Control Logic and Outputs

The PWM signal is processed through control logic which takes into account the operating mode and output polarity to determine which output to modulate. The logic table for the outputs is given in Table 2. For example, assume that the reference signal is in the first quadrant (positive and increasing). The output will lag the reference by a certain delay and hence the error amp output will be positive, resulting in SIGN = 0. The logic table indicates that GD1 is modulated during this phase allowing power transfer to increase the output voltage to keep up with the reference. Increasing error (MAG) will result in larger duty cycle and enable the output to increase and catch up with the reference. If the output becomes higher than the reference (as is likely in the second quadrant when the reference is dropping), the SIGN becomes 1 and GD3 is modulated to decrease the output level by transferring power to the input. At the boundary of the first and second quadrant, there may be some switching back and forth between modes as the reference slope crosses through zero. Some of this switching can be eliminated by judicious selection of error amplifier filtering and compensation components. In the first quadrant, when PWM is applied to Q1, Q2 is turned on in the rectifier mode by the clock signal to allow the flyback transformer flux to

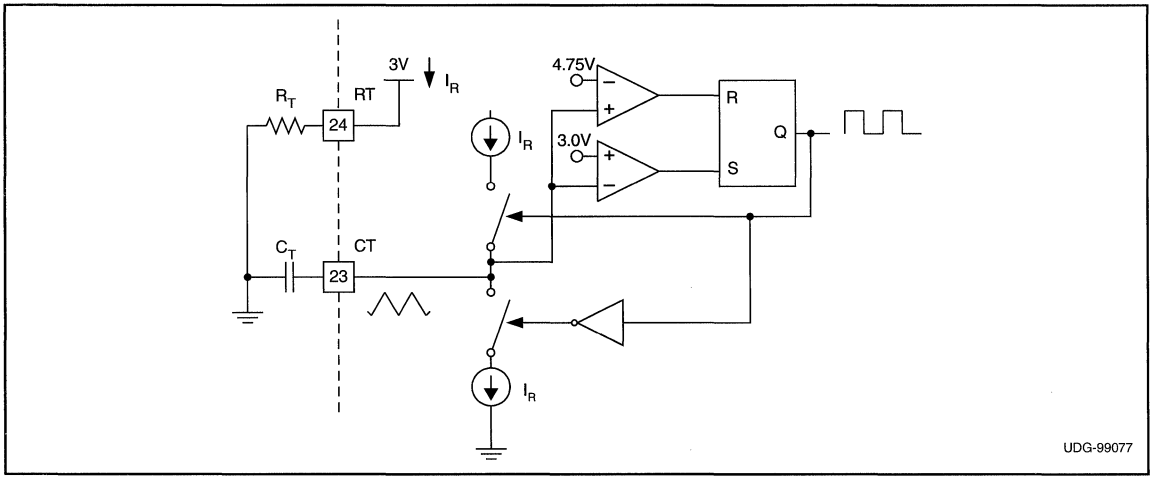


Figure 7. Oscillator setup.

APPLICATION INFORMATION (cont.)

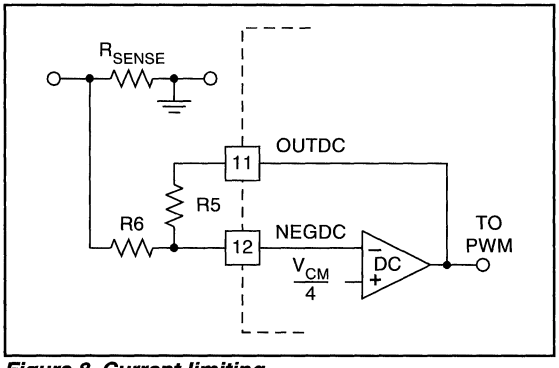


Figure 8. Current limiting.

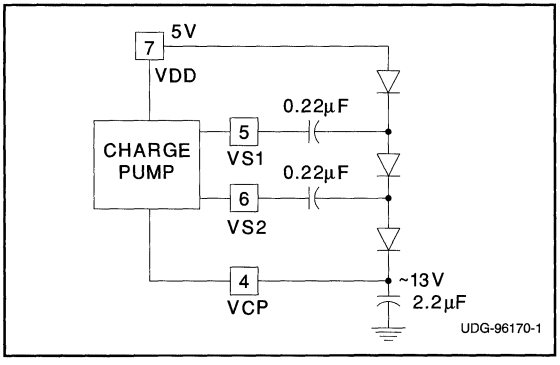


Figure 9. Charge pump circuits.

reset (and to transfer power to the output). Operation in quadrants 3 and 4 is symmetrical to the first two quadrants with Q2 and Q3 interchanged. Note that the output signal for Q2 is logically inverted to allow for driving the p-channel switch. An n-channel switch can also be used for Q2, but the drive circuit must be transformer isolated and the polarity inverted. The outputs are designed for high peak current drive and low internal impedance. In isolated systems, GD1 must be coupled to Q1 using a gate-drive transformer.

DC Current Limit

The DC current limit function provides protection against short circuit conditions by limiting the maximum current level and shutting off the PWM function when the limit point is reached.

The DC limit is activated when DC out is below 0.5 V_{CM} or above 1.5 • V_{CM}. The DC current limit can be programmed by setting:

$$\frac{R5}{R6} = 3.$$

With this ratio, a symmetric DC limit with thresholds of ±0.5V is obtained. For other ratios, the positive and negative voltage thresholds for current sense signal are given by:

$$V_{SENSE}(POS) = \frac{V_{CM}}{4} \bullet \left(1 - \frac{R6}{R5}\right)$$

$$V_{SENSE}(NEG) = \frac{V_{CM}}{4} \bullet \left(1 - \frac{5R6}{R5}\right)$$

Even though the DC current is typically sensed in the secondary, the currentl limit is applied fo the active PWM switch at the time. For example, if Q1 is the PWM switch and DCLIM is activated, the UCC3750 will prevent trun-on for Q1 during the negative slope of the ramp (Fig. 2). The DC limit is functional on a cycle-by-cycle basis.

Charge Pump and Reference

The UCC3750 is designed to work on the secondary side of an isolated power supply. It requires a 5V power supply with respect to its GND pin to operate. Note that the GND pin of the IC is also the reference point of the ring signal that is generated by the converter. If the converter output is connected in series with any other voltage, it should be ensured that the available supply voltage is referenced to the converter output return. The IC along with its associated charge pump components shown in Fig. 9 generates all the other voltages the system requires. The UCC3750 typically requires about 5mA to operate without any loads on the drive outputs. The charge pump capacitor should be large enough to keep the VCP fairly constant when driving Q1-Q3 in the converter.

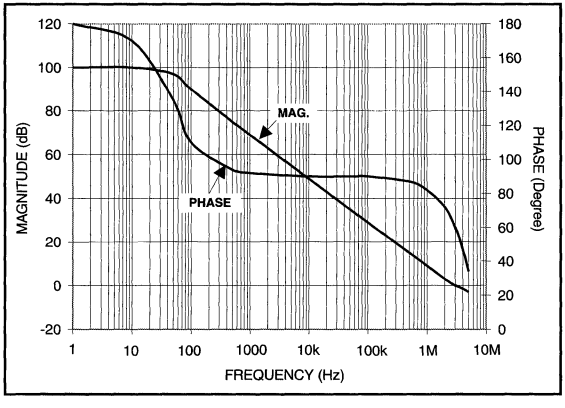


Figure 10. Frequency response to error amplifiers.

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Single Line Ring Generator Controller

PRELIMINARY

FEATURES

- Novel Topology for Low-Cost, Efficient Generation of Ring Voltage
- Provides DC Offset and "Talk Battery" Voltage for Off-Hook Conditions
- Selectable 20,25 and 50 Hz Ring Frequency
- Secondary (AC) Current Limiting Allows Removal of AC Voltage under Off-Hook Conditions
- Primary Current Limiting to turn Power Stage off under Fault Conditions
- Operates from a Single 12V Supply

DESCRIPTION

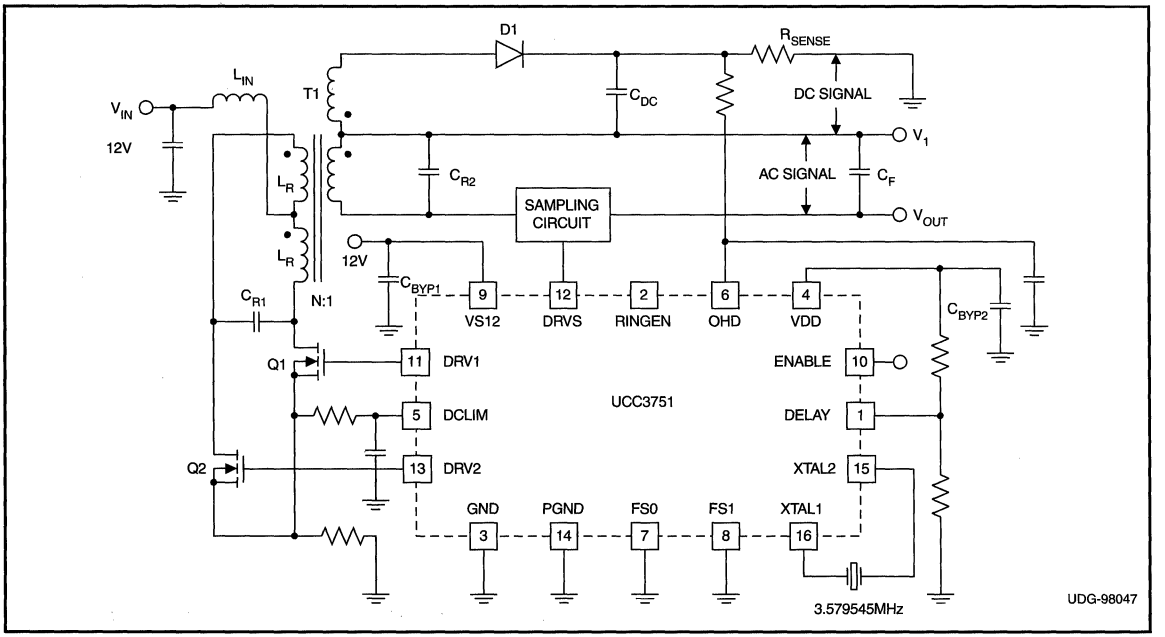
The UCC3751 controller is designed for driving a power stage that generates low frequency, high voltage sinusoidal signals for telephone ringing applications. The controller and the power stage are most suitable for single line applications where low cost, high efficiency and minimum parts count are critical. In addition to providing the sinusoidal ringing signal, the controller and the power stage are designed to provide the required DC voltage across the output when the phone goes off-hook. The DC voltage is also added as the offset to the ringing signal. This feature eliminates the need to have a separate talk battery voltage power supply as well as relays and drivers to switch between the ringing voltage and the talk battery.

The UCC3751 directly drives primary side switches used to implement a push-pull resonant converter topology and transformer coupled sampling switches located on the secondary of the converter. For normal ring signal generation, the primary switching frequency and secondary sampling frequency are precisely offset from each other by the ringing frequency to produce a high voltage low frequency alias signal at the output. The off-hook condition is detected by sensing the AC current and when AC limit is exceeded, the sampling frequency is set to be equal to the primary switching frequency to produce a DC output.

The drive signal frequencies are derived from a high frequency (3579545 Hz) crystal. The primary switching frequency is 89.488 kHz and the sampling frequency is 20, 25 or 50 Hz less depending on the status of frequency select pins FS0 and FS1.

The circuits described in this datasheet are covered under US Patent #5,663,878 and other patents pending.

TYPICAL APPLICATIONS CIRCUIT



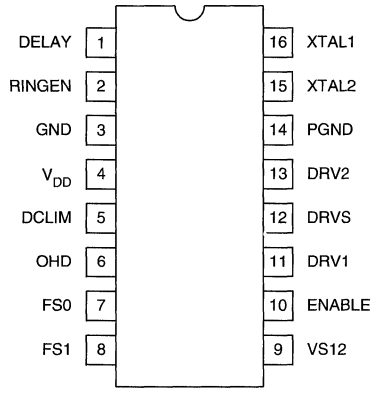
ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 14V
Analog Inputs (OHD, DCLIM, XTAL1, XTAL2)
Maximum Forced Voltage..... –0.3 to 5V
Logic Inputs
Maximum Forced Voltage ..... –0.3 to 7.5V
Reference Output Current (V_{DD})..... Internally Limited
Output Current (DRV1, DRV2, DRVS) Pulsed 1.5A
Operating Junction Temperature ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C

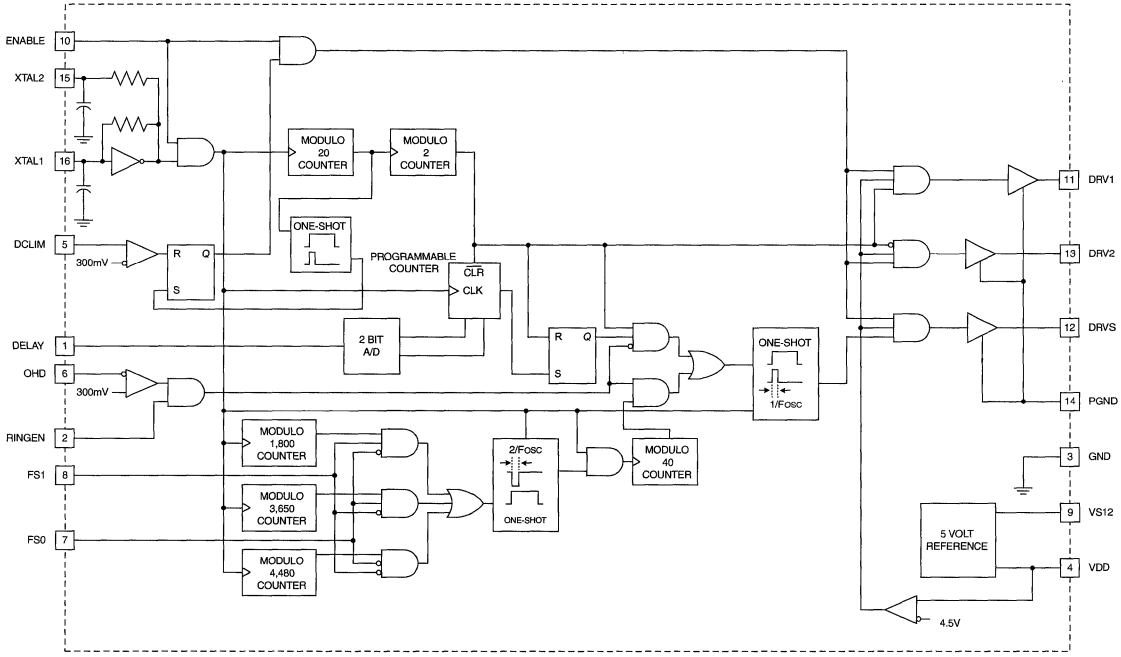
Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specific terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS.

CONNECTION DIAGRAM

DIL-16, SOIC-16 (TOP VIEW)
N or D Packages



BLOCK DIAGRAM



UDG-98020

Table I. Frequency selectability decoding.

FS1	FS0	MODE	Sine Wave Frequency (Hz)
0	0	1	20
0	1	1	25
1	0	1	50
1	1	3	0
OHD = 0.5		2	0

RINGEN	OHD	FS1	FS0	F_{DRVS}	F_{DRV}–F_{DRVS}
1	0	0	0	89.469kHz	20Hz
1	0	0	1	89.464kHz	25Hz
1	0	1	0	89.439kHz	50Hz
0	X	X	X	89.489kHz	0.0Hz
X	1	X	X	89.489kHz	0.0Hz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3751 and –40°C to +85°C for the UCC2751, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V12 Supply Current Section					
Supply Current	ENABLE = 0V		0.5	TBD	mA
	ENABLE = 5V		5		mA
Internal Reference with External Bypass Section					
Output Voltage (VDD)		4.85	5	5.15	V
Load Regulation	$0mA \le I_{VDD} \le 2mA$		5		mV
Line Regulation	$10V < VS12 < 13V$, I_{VDD} = 1mA		3		mV
Short Circuit Current	$V_{DD} = 0$	5	10		mA
Output Drivers Section (DRV1, DRV2)					
Pull Up Resistance			9	15	Ω
Pull Down Resistance			9	15	Ω
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS
Output Drivers Section (DRVS)					
Pull Up Resistance			6	10	Ω
Pull Down Resistance			6	10	Ω
Sample Pulse-Width	Mode 1 and 2, (Note 1)		280		nS
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS
Current Limit Section					
OHD Threshold			300		mV
OHD Input Current	$V_{OHD} = 0V$		–1		µA
DCLIM Threshold			300		mV
DCLIM Input Current	$V_{DCLIM} = 0V$		–1		µA
Frequency Section (Note 1)					
Primary Switching Frequency	All cases 3.579545 MHz Crystal		89489		Hz
Sampling Switching Frequency	FS0 = 0, FS1 = 0, Mode 1, (Note 1)		89469		Hz
	FS0 = 1, FS1 = 0, Mode 1		89464		Hz
	FS0 = 0, FS1 = 1, Mode 1		89439		Hz

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3751 and –40°C to +85°C for the UCC2751, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Off-Hook Sampling Delay (Note 2)					
td0	$V_{DELAY} < 0.9V$		0		nS
td1	$1.1V < V_{DELAY} < 1.9V$		280		nS
td2	$2.1V < V_{DELAY} < 2.9V$		560		nS
td3	$3.1V < V_{DELAY} < 3.9V$		840		nS
td4	$4.1V < V_{DELAY}$		1120		nS

Note 1. *Frequency setting is as shown in the Frequency Selectability Decoding Table. Sine Wave Frequency = Primary – Sampling Frequency.*

Note 2. *The delay function will delay the sample pulse from the rising edge of DRV2 to allow adjustment of the DC level provided during Mode 2.*

PIN DESCRIPTIONS

DCLIM: Primary current sense input. Signal proportional to the primary switch current. All outputs are turned off when a threshold of 300mV is exceeded on this pin. This current limit works on a cycle-by-cycle basis.

DELAY: A resistive divider from VDD to GND is programmed and fed into DELAY pin. The voltage at this pin sets the phase difference between the sampling pulses and primary pulses under off-hook condition. By programming the delay, desired level of DC voltage can be attained at the ringer output when the OHD threshold is exceeded.

DRV1, DRV2: Low impedance driver outputs for the primary switches.

DRVS: Low impedance driver output for the sampling switch(es). The pulse width of this output is 280ns. Typically, a pulse transformer is used to couple the short sampling pulses at DRVS to the floating sampling switch(es).

ENABLE: Logic input which turns off the outputs when low.

FS0, FS1: Frequency select pins for determining the difference frequency between primary and secondary pulses under normal operation. These pins can be hardwired to GND or VDD to get one of the available output frequencies (20,25 and 50 Hz). See Note 1 in the spec table.

GND: Reference point for all the internal voltages and common return for the device.

OHD: Secondary current sense input. Voltage proportional to output current DC level is fed into this pin and compared to an internal threshold of 300mV. If the threshold is exceeded, the sampling scheme is changed to eliminate the AC component in the output voltage as required by the off-hook condition.

PGND: Return point for the output drivers. Connect to GND at a single point in the circuit.

RINGEN: Logic input used to determine when the ring signal is needed. When this signal is high and OHD low, normal ring signal is available at the output of the ring generator.

VDD: Internal regulated 5V supply. This voltage is used to power all the internal precision circuits of the IC. This pin needs to be bypassed to GND with ceramic capacitor.

VS12: External 12V power supply for the IC. Powers V_{DD} and provides voltage for the output drivers.

XTAL1, XTAL2: Pins for connecting precision Crystal to attain the accurate output frequencies. An external square-wave pulse can also be applied to XTAL2 if XTAL1 is tied to VDD/2.

APPLICATION INFORMATION

Power Stage Operation

The power stage used for the UCC3751 application has two distinct switching circuits which together produce the required low frequency signal on the output. The primary side switching circuit consists of a current fed push-pull resonant circuit that generates the high frequency sinusoidal waveform across the transformer winding. The operation of this type of circuit is extensively covered in Unitrode Application notes U-141 and U-148. Resonant components C_{R1}, C_{R2}, L_R, N should be chosen so that the primary and secondary resonances are well matched. Also, for the UCC3751 operation, switching frequency is fixed by crystal selection. So, the resonant components must be selected to yield a resonant frequency close enough to the switching frequency to get a low distortion sine-wave. Practically, since it is impossible to get an exact match between the two frequencies, the switching frequency should always be higher than the resonant frequency to ensure low distortion and take advantage of ZVT operation. Switches Q1 and Q2 are pulsed at 50% duty cycle at the switching frequency (89.489 kHz) determined by a crystal (3.579545 MHz) connected to the UCC3751. The input voltage for the resonant stage (typically 12V) determines the voltage stress of Q1 and Q2. Transformer turns ratio is determined by the output voltage requirements. On the secondary side, the high frequency waveform is sampled at a predetermined frequency (e.g. 89.469 kHz) which differs from the primary switching frequency by the desired output frequency (e.g. 20 Hz). The sampling is accomplished using a bi-directional switching circuit as shown in Figure 2 and Figure 3. Figure 2 shows the sampling mechanism consisting of two back-to-back FET switches allowing current flow in both directions. The sampling can also be done with a single active switch and a full-bridge rectifier as shown in Fig. 3. The DRVS pin of the UCC3751 provides the drive signal for the sampling switch(es) and this signal is coupled through a pulse transformer. Typical pulsewidth of the sampling signal is 280ns. As a result of sampling, the resultant output signal matches the secondary voltage in amplitude and has a low output frequency desired for ring generation.

The secondary winding of the power transformer also has a tap (or a separate winding) to generate a loosely regulated DC voltage. This DC voltage can be used to offset the ring generator output. The UCC3751 is also configured such that the AC output can go to zero under certain conditions. Table 2 provides the logic levels for different operating modes of UCC3751. Operation in mode 2 is achieved by altering the sampling frequency to match the switching frequency and sampling the secondary AC voltage at zero crossings. As a result, the resultant total output voltage between V_{OUT} and GND is the semi-regulated DC voltage achieved through the tapped secondary. This feature allows the circuit to operate under off-hook and idle conditions when only the DC portion of the voltage is required. The activation of this mode occurs when the OHD voltage exceeds a set threshold or RINGEN is low. The incorporation of this mode eliminates any need for external relays or switching circuits as well as eliminating the need for an additional power supply for powering the phone. The DC voltage level can be fine tuned by adjusting the voltage on the DELAY pin of the UCC3751. This pin sets the sampling delay time during the off-hook mode and allows a DC voltage to be developed between V_1 and V_{OUT} during this mode. Fig. 1 illustrates the operation of this mode. When the DELAY is set between 0 and 1V, the sampling is done in phase with the primary switching instances (at points A), leading to an average voltage of 0V between V_1 and V_{OUT} for a sinusoidal secondary signal. If DELAY is set to another level, the sampling instance shifts (e.g. to point B) leading to an effective voltage VB being developed between V_1 and V_{OUT}. The actual V_{OUT} is the sum of VB and the DC offset voltage derived from the additional (or tapped) winding (V_1).

Table II. Operating mode selection.

Condition	OHD	RINGEN	Sampling Output Mode
Continuous Ringing	Low	High	Frequency Offset from Primary (Mode 1)
Idle (On Hook, No Ringing)	Low	Low	Synchronized to Primary Frequency with Phase Controlled by DELAY (Mode 2)
Off-Hook	High	X (Low/High)	Mode 2
Cadenced Ringing	Low	High/Low	Mode 1/Mode 2

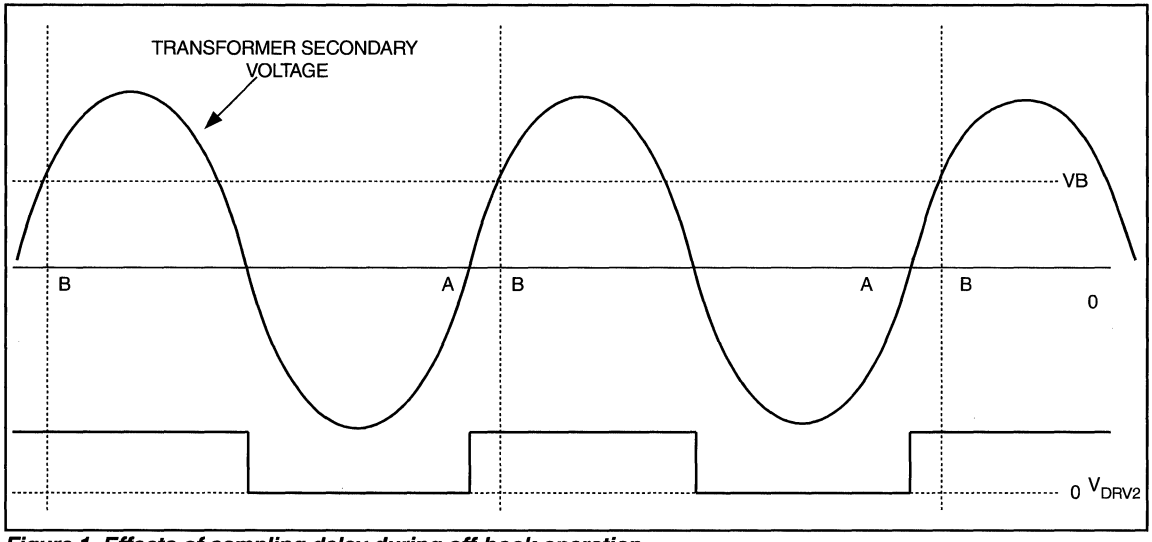


Figure 1. Effects of sampling delay during off-hook operation.

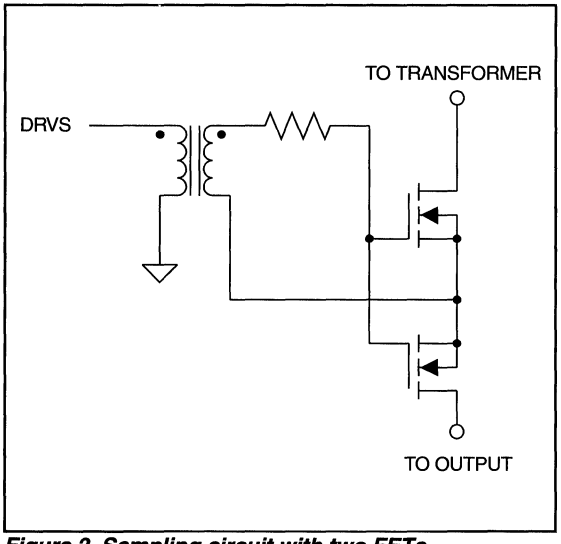


Figure 2. Sampling circuit with two FETs.

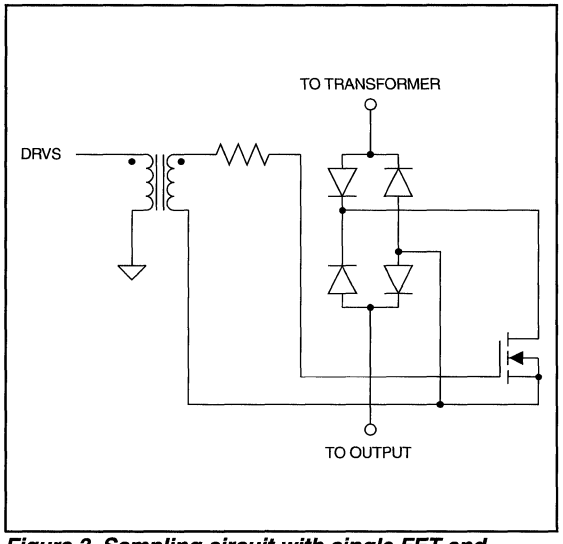


Figure 3. Sampling circuit with single FET and full-bridge rectifier.

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Resonant Ring Generator Controller

PRELIMINARY

FEATURES

- Novel Topology for Low-Cost, Efficient Generation of Ring Voltage
- Suitable for Multi-Line Operation
- Selectable 20,25 and 50 Hz Ring Frequency
- Secondary (AC) Current Limiting Generates an Off-Hook Detect Signal
- Primary Current Limiting to Turn Power Stage Off Under Fault Conditions
- Operates from a Single 12V Supply

DESCRIPTION

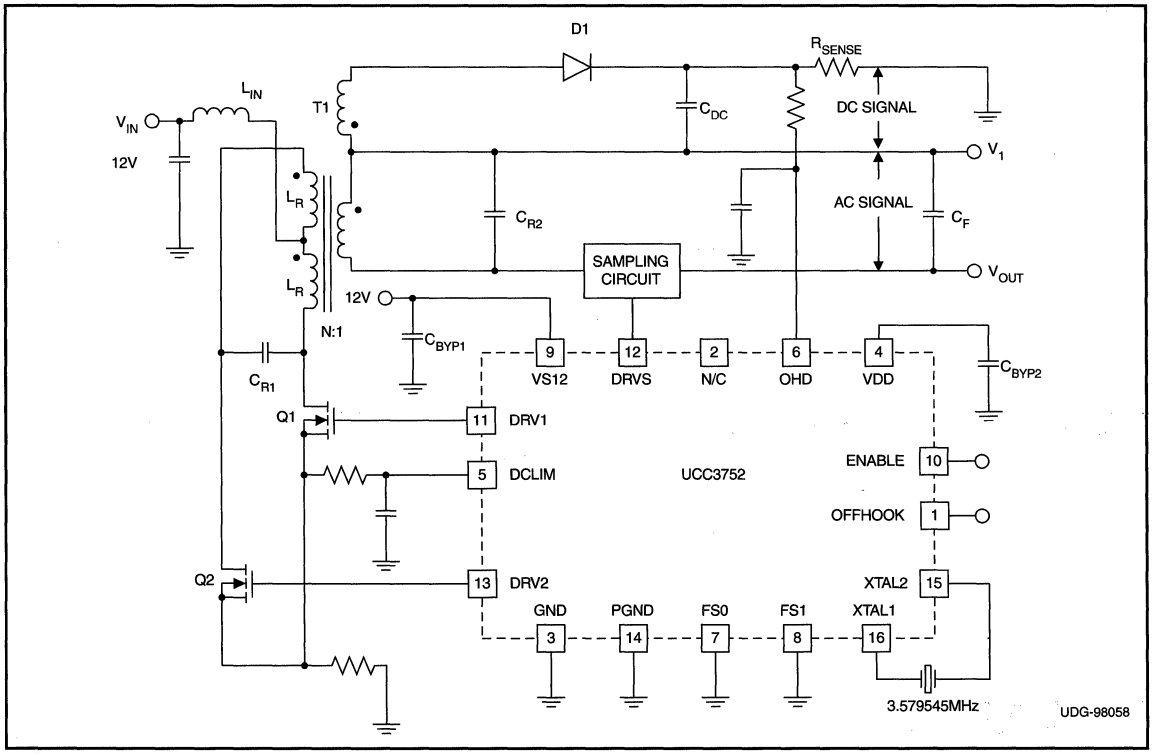
The UCC3752 controller is designed for driving a power stage that generates low frequency, high voltage sinusoidal signals for telephone ringing applications. The controller and the power stage are most suitable for up to 5 line applications where low cost, high efficiency and minimum parts count are critical. A semi-regulated DC voltage is added as an offset to the ringing signal. The ring generator operation is non-isolated and open loop.

The UCC3752 directly drives primary side switches used to implement a push-pull resonant converter topology and transformer coupled sampling switches located on the secondary of the converter. For normal ring signal generation, the primary switching frequency and secondary sampling frequency are precisely offset from each other by the ringing frequency to produce a high voltage low frequency alias signal at the output. The off-hook condition is detected by sensing the AC current and when AC limit is exceeded, a flag is generated on the OFFHOOK pin.

The drive signal frequencies are derived from a high frequency (3579545 Hz) crystal. The primary switching frequency is 89.489 kHz and the sampling frequency is 20, 25 or 50 Hz less depending on the status of frequency select pins FS0 and FS1.

The circuits described in this datasheet are covered under US Patent #5,663,878 and other patents pending.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage 13.2V
Analog Inputs (OHD, DCLIM, XTAL1, XTAL2)
  Maximum Forced Voltage. . . . . –0.3 to 5V
Logic Inputs
  Maximum Forced Voltage . . . . . –0.3 to 7.5V
Reference Output Current (V_{DD}) . . . . . Internally Limited
Output Current (DRV1, DRV2, DRVS) Pulsed 1.5A
Operating Junction Temperature . . . . . –40°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specific terminals. Pulsed is defined as a less than 10% duty cycle with a maximum duration of 500µS.

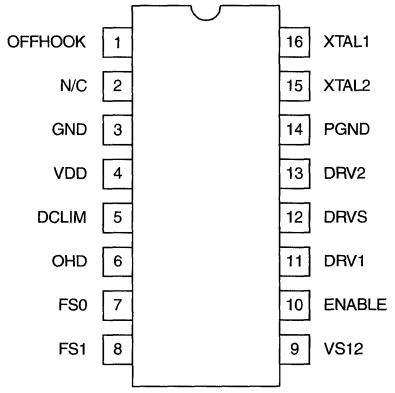
Table I. Frequency selectability decoding.

FS1	FS0	MODE	Sine Wave Frequency (Hz)
0	0	1	20
0	1	1	25
1	0	1	50
1	1	3	0

FS1	FS0	F_{DRVS}	FDRV – FDRVS
0	0	89.469kHz	20Hz
0	1	89.464kHz	25Hz
1	0	89.439kHz	50Hz

CONNECTION DIAGRAMS

(TOP VIEW) DIL-16, SOIC-16
N or D Packages



ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3752 and –40°C to +85°C for the UCC2752, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V12 Supply Current Section					
Supply Current	ENABLE = 0V		0.5	TBD	mA
	ENABLE = 5V		5		mA
Internal Reference with External Bypass Section					
Output Voltage (V_{DD})		4.85	5	5.15	V
Load Regulation	0mA ≤ I_{VDD} ≤ 2mA		5		mV
Line Regulation	10V < Vs12 < 13V, I_{VDD} = 1mA		3		mV
Short Circuit Current	VDD = 0	5	10		mA
Output Drivers Section (DRV1, DRV2)					
Pull Up Resistance	Driver Out = 2.5V		9	15	Ω
Pull Down Resistance	Driver Out = 2.5V		9	15	Ω
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS
Output Drivers Section (DRVS)					
Pull Up Resistance	Driver Out = 2.5V		6	10	Ω
Pull Down Resistance	Driver Out = 2.5V		6	10	Ω
Sample Pulse-Width	Mode 1 (Table 1)		280		nS
Rise Time	C_{LOAD} = 1nF		50	100	nS
Fall Time	C_{LOAD} = 1nF		50	100	nS

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3752 and –40°C to +85°C for the UCC2752, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Limit Section					
DCLIM Threshold			300		mV
DCLIM Input Current	V_{DCLIM} = 0V		–0.5		µA
OffHook Detect Section					
OHD Threshold			300		mV
OHD Input Current	V_{OHD} = 0V		0.5		µA
Offhook V_{OH}	$I_{OFFHOOK}$ = 100mA		4.0		V
Offhook V_{OL}	$I_{OFFHOOK}$ = –100mA		1.0		V
Offhook Pull-Up Impedance	$V_{OFFHOOK}$ = 2.5V		1.0		kΩ
Offhook Pull-Up Impedance	$V_{OFFHOOK}$ = 2.5V		1.0		kΩ
Frequency Section (Table 1)					
Primary Switching Frequency	All cases 3.579545 MHz Crystal		89489		Hz
Sampling Switching Frequency	FS0 = 0, FS1 = 0, Mode 1, (Table 1)		89469		Hz
	FS0 = 1, FS1 = 0, Mode 1		89464		Hz
	FS0 = 0, FS1 = 1, Mode 1		89439		Hz

PIN DESCRIPTIONS

DCLIM: Primary current sense input. Signal proportional to the primary switch current. All outputs are turned off when a threshold of 300mV is exceeded on this pin. This current-limit works on a cycle-by-cycle basis.

DRV1, DRV2: Low impedance driver outputs for the primary switches. DRV1 and DRV2 are complimentary and have 50% duty cycle.

DRVS: Low impedance driver output for the sampling switch(es). The pulse width of this output is 280ns. Typically, a pulse transformer is used to couple the short sampling pulses at DRVS to the floating sampling switch(es).

ENABLE: Logic input which turns off the outputs when low.

FS0, FS1: Frequency select pins for determining the difference frequency between primary and secondary pulses under normal operation. These pins can be hardwired to GND or VDD to get one of the available output frequencies (20,25 and 50 Hz). See Table 1 in the spec table.

GND: Reference point for all the internal voltages and common return for the device.

OFFHOOK: Output indicating the off-hook condition. This signal can be used by an external circuit to switch to a line from the ring generator output to the DC voltage.

OHD: Off-Hook Detect. Voltage proportional to output current DC level is fed into this pin and compared to an internal threshold of 300mV. If the threshold is exceeded, the OFFHOOK output goes high.

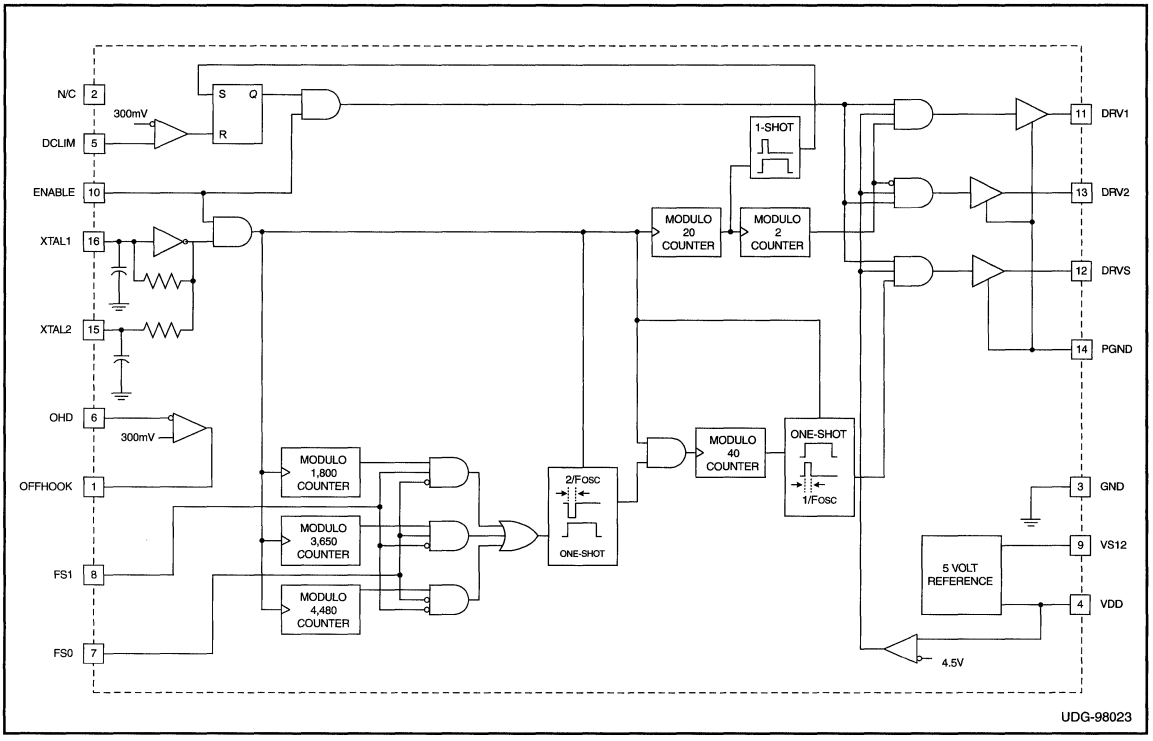
PGND: Return point for the output drivers. Connect to GND at a single point in the circuit.

VDD: Internal regulated 5V supply. This voltage is used to power all the internal precision circuits of the IC. This pin needs to be bypassed to GND with ceramic capacitor.

VS12: External 12V power supply for the IC. Powers VDD and provides voltage for the output drivers.

XTAL1, XTAL2: Pins for connecting precision Crystal to attain the accurate output frequencies. An external square-wave pulse can also be applied to XTAL2 if XTAL1 is tied to VDD/2.

BLOCK DIAGRAM



APPLICATION INFORMATION

Power Stage Operation

The power stage used for the UCC3752 application has two distinct switching circuits which together produce the required low frequency signal on the output. The primary side switching circuit consists of a current fed push-pull resonant circuit that generates the high frequency sinusoidal waveform across the transformer winding. The operation of this type of circuit is extensively covered in Unitrode Application notes U-141 and U-148. Resonant components C_{R1}, C_{R2}, L_R, N should be chosen so that the primary and secondary resonances are well matched. Also, for the UCC3752 operation, switching frequency is fixed by crystal selection. So, the resonant components must be selected to yield a resonant frequency close enough to the switching frequency to get a low distortion sine-wave. Practically, since it is impossible to get an exact match between the two frequencies, the switching frequency should always be higher than the resonant frequency to ensure low distortion and take advantage of ZVT operation. Switches Q1 and Q2 are pulsed at 50% duty cycle at the switching frequency (89.489 kHz) determined by a crystal (3.579545 MHz) connected to the UCC3752. The input voltage for the resonant stage (typically 12V) determines the voltage stress of Q1 and Q2. Transformer turns ratio is determined by the output voltage requirements. On the secondary side, the high frequency waveform is sampled at a predetermined frequency (e.g. 89.469 kHz) which differs from the primary switching frequency by the desired output frequency (e.g. 20 Hz). The sampling is accomplished using a bi-directional switching circuit as shown in Figure 1 and Figure 2. Figure 1 shows the sampling mechanism consisting of two back-to-back FET switches allowing current flow in both directions. The sampling can also be done with a single active switch and a full-bridge rectifier as shown in Fig. 2. The DRVS pin of the UCC3752 provides the drive signal for the sampling switch(es) and this signal is coupled through a pulse transformer. Typical pulsewidth of the sampling signal is 280nS. As a result of sampling, the resultant output signal matches the secondary voltage in amplitude and has a low output frequency desired for ring generation.

The secondary winding of the power transformer also has a tap (or a separate winding) to generate a loosely regulated DC voltage. This DC voltage can be used to offset the ring generator output. It an also be used as a power supply for supplying talk battery voltage in some applications.

APPLICATION INFORMATION (cont.)

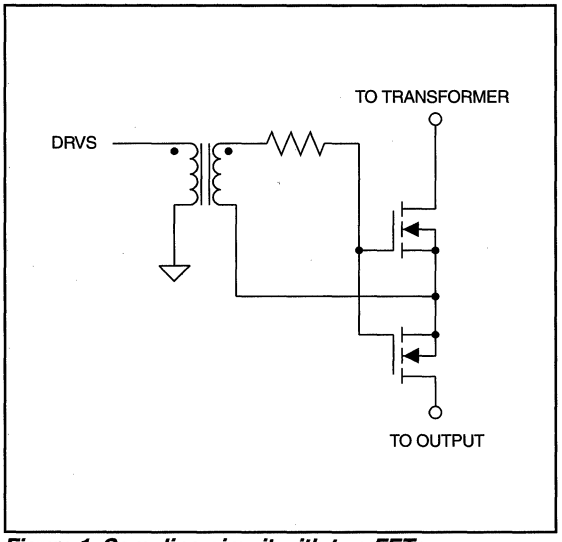


Figure 1. Sampling circuit with two FETs.

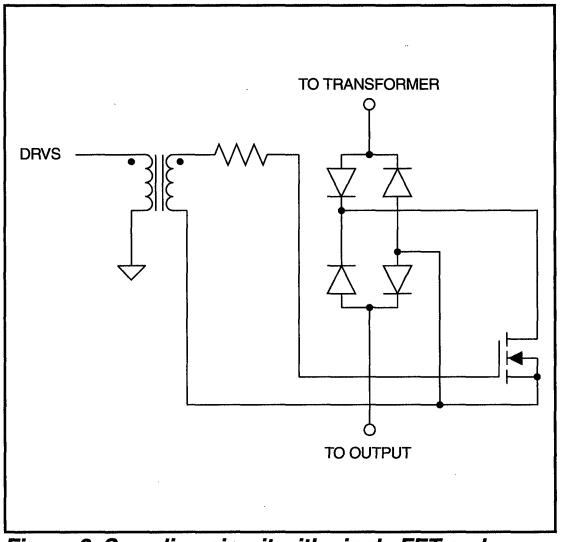


Figure 2. Sampling circuit with single FET and full-bridge rectifier.

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application INFO available

UCC1926
UCC2926
UCC3926

± 20A Integrated Current Sensor

FEATURES

- Integral Non-inductive Current Sense Element with Internal Kelvin Connections
- 20A Current Rating
- Bi-directional, High Side or Low Side Sensing
- Internal Temperature Nulling Circuitry for Current Sense Element and Amplifier
- Logic Compatible Current Direction Status Output
- Low Offset, Chopper Stabilized Current Sense Amplifier
- Uncommitted Amplifier with User Programmable Gain
- Overcurrent Indication with User Programmable Threshold

DESCRIPTION

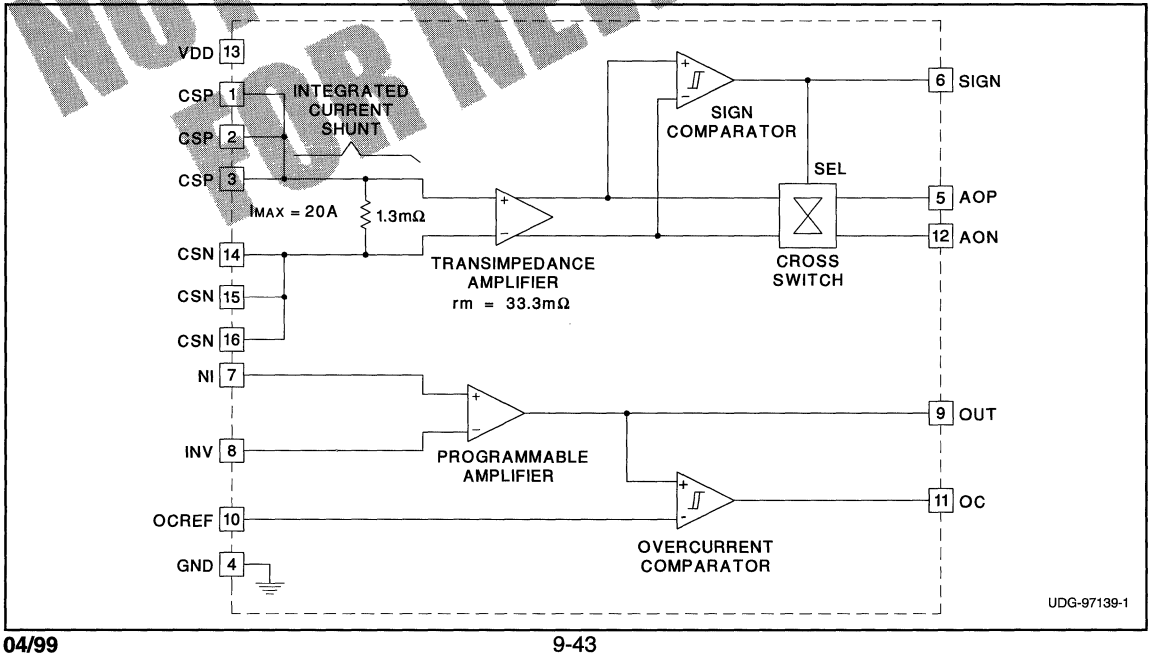
The UCC3926 Current Sensor IC contains a wideband, transimpedance amplifier for converting the current through an internal, non-inductive 1.3mΩ shunt resistor into a proportional voltage. The sense element operates in both high-side (V_{DD} referenced) and low-side (GND referenced) applications.

The UCC3926 can measure currents up to ±20A. This transimpedance amplifier gain is precisely trimmed to 33.3mΩ to convert a 15A input into a 500mV output signal. It has a very low input offset voltage from chopper-stabilization. A cross-switching block rectifies the input signal by forcing the differential output, AOP positive with respect to the other differential output, AON. SIGN indicates the polarity of the current.

The UCC3926 programmable amplifier provides three functions. It converts the differential transimpedance output signal into a single-ended signal. It has a user-controlled gain stage that sets the maximum current level to the desired voltage and it level shifts the zero current point to the desired level as well. A comparator then compares the output of the instrumentation amplifier to a user-set reference voltage on OCREF, which provides an overcurrent status bit OC.

The UCC3926 is available in the 16 pin SOIC package.

BLOCK DIAGRAM



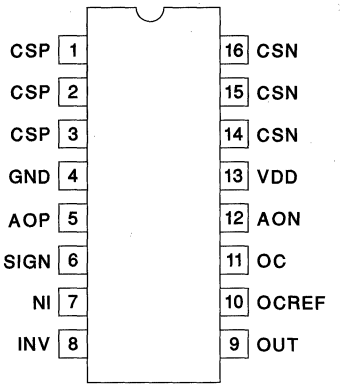
ABSOLUTE MAXIMUM RATINGS

Input Sense Current (I_{IN}) . . . . . ± 20A
Supply Voltage, VDD 14.5V
Inrush Current, 50µs . . . . . ±100A
Input Voltage Range (CSP, CSN) . . . . . –0.2V to 14.5V
CSP, CSN, Common Mode Range
(referenced to GND) . . . . . ± 200mV
CSP, CSN, Common Mode Range
(referenced to V_{DD}) . . . . . ± 200mV
Shunt Resistance 2.25mΩ
Storage Temperature . . . . . –65°C to 150°C
Junction Temperature . . . . . –55°C to 150°C
Lead Temperature (Soldering, 10sec.) . . . . . 300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

SOIC-16 (Top View)
DS Package



ORDERING INFORMATION

	TEMPERATURE RANGE	PACKAGES
UCC1926	– 55°C to +125°C	DS
UCC2926	– 40°C to +85°C	DS
UCC3926	0°C to +70°C	DS

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for V_{DD} = 4.8V; all temperature ranges and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Section					
VDD		4.8		14	V
I_{VDD}			3.8	6	mA
Transimpedance Amplifier Section					
AOP – AON	I_{IN} = 15A, VDD = 10V, 25°C	490	500	510	mV
	I_{IN} = 15A, VDD = 10V, 0°C to +70°C	485	500	515	mV
	I_{IN} = 15A, VDD = 10V, –40°C to +85°C	460	500	540	mV
	I_{IN} = 15A, VDD = 10V, –55°C to +125°C	410	500	590	mV
Quiescent Output Voltage (AOP, AON)	I_{IN} = 0		1.0		V
Quiescent Differential Voltage (AOP – AON)	I_{IN} = 0, Measure AC Peak to Peak		0	20	mV
Bandwidth	(Note 1)	20	40		MHz
Output Impedance			350	500	Ω
Shunt Resistance	CSP to CSN		1.3		mΩ
PSRR	VDD = 4.8V to 10V	45			dB
	VDD = 10V to 14V	25			dB
Temperature Coefficient	(Note 1)	–200		200	ppm/°C
Sign Comparator Section					
V_{OH}, VDD – SIGN	CSP = 1A, I_{SIGN} = –100µA, CSN = 0V		0.2	0.4	V
V_{OL}, SIGN	CSP = –1A, I_{SIGN} = 100µA, CSN = 0V		0.2	0.4	V
I_{IH} Threshold	Ramp CSP, CSN = 0V		400	600	mA
I_{IL} Threshold	Ramp CSP, CSN = 0V		–400	–600	mA
Programmable Amplifier Section					
A_{VOL}		60	70		dB
GBW	At 200kHz	6	13		MHz
V_{IO}	V_{IN} = 0.5V, 1.5V, 2.5V	–9		9	mV

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for V_{DD} = 4.8V; all temperature ranges and $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Programmable Amplifier Section (cont.)					
PSRR	V_{DD} = 4.8V to 10V	60			dB
	V_{DD} = 10V to 14V	60			dB
Common Mode Input Range		0.5		2.5	V
I_{IB}, Input Bias Current (NI, INV)			–100	–350	nA
Programmable Amplifier Section (cont.)					
I_{IO}, Input Offset Current			20	350	nA
V_{OL}	INV – NI = 20mV, IO = 0µA		100	200	mV
	INV – NI = 20mV, IO = 200µA		150	300	mV
V_{OH}	NI – INV = 20mV, IO = –200µA, (VDD – OUT)		1.2	2	V
V_{OH}, Clamp	NI – INV = 20mV, VDD = 14V	6	7	8	V
I_{OL}	OUT = 1.5V	1	3.5		mA
I_{OH}	OUT = 1.5V	– 250	– 325		mA
Overcurrent Comparator Section					
OC Comp Threshold	OCREF = 2V	2.00		2.05	V
Common Mode Range	(Note 1)	0.1		V_{DD}– 2	V
Hysteresis		20	40	60	mV
VOL	(OCREF – OUT) = 100mV, IOC = 100µA		0.2	0.4	V
VOH, VDD – OC	(OUT – OCREF) = 100mV, IOC = –100µA		0.2	0.4	V
Propagation Delay	(OUT – OCREF) = ± 100mV		90	175	ns

Note 1: Guaranteed by design. Not 100% tested in prodcution.

PIN DESCRIPTIONS

AOP: Positive output of the converted current signal. Voltage from AOP to AON is the absolute value of the transimpedance amplifier output. AOP may show some "chopping" noise. The differential to single-ended conversion removes the common-mode noise between AOP and AON.Some high frequency filtering of AOP to GND can reduce the fast transient spikes. The output stage of AOP is shown in Figure 1.

AON: Negative output of the converted current signal. Voltage from AOP to AON is the absolute value of the transimpedance amplifier output. AON may show some "chopping" noise. The differential to single-ended conversion removes the common-mode noise between AOP and AON. Some high frequency filtering of AON to GND can reduce the fast transient spikes. Note that AON is above GND voltage. The output stage of AON is shown in Figure 1.

CSN: Input connection to one end of the internal current sense shunt resistor. Nominal resistance from CSP to CSN is 1.3mΩ. The current shunt has a nominal temperature coefficient of 3530 ppm/°C. The temperature adjusted autozero gain is designed to cancel this temp co. effect. CSN may be referenced to GND for low side sensing or to VDD for high side sensing. CSP – CSN may vary from ±75mV from either GND or VDD. Current into CSN is defined as negative.

CSP: Input connection to the other end of the internal current sense shunt resistor. Nominal resistance from CSP to CSN is 1.3mW. The current shunt has a nominal temperature coefficient of 3530 ppm/°C. The temperature adjusted autozero gain should cancel this temp co. effect. CSP may be referenced to GND for low side sensing or to VDD for high side sensing. CSP – CSN may vary from ±75mV from either GND or VDD. Current into CSP is defined as positive.

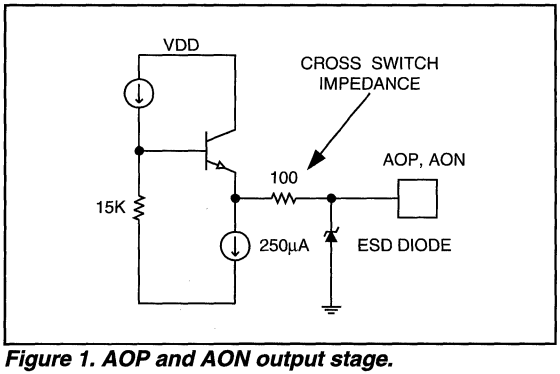


Figure 1. AOP and AON output stage.

PIN DESCRIPTIONS (cont.)

GND: This pin is the return point for all device currents.

INV: Negative input to the programmable amplifier to provide differential to single-ended signal conversion.

NI: Positive input to the programmable amplifier to provide differential to single-ended signal conversion.

OC: Overcurrent comparator output. When OUT is greater than OCREF, OC switches high. The OC comparator has a typical hysteresis of 25mV.

OCREF: The reference pin of overcurrent comparator for setting overcurrent threshold voltage.

OUT: Output of the programmable amplifier intended to provide differential to single-ended signal conversion of the transimpedance amplifier's outputs. Use this opamp to establish overall gain and nominal zero current reference voltage. This amplifier may be configured with a gain of one or more. Any non-common mode "chopping" noise between AOP and AON will show up at OUT. Some filtering of OUT may improve the application's performance.

SIGN: Sign comparator output. SIGN also controls the analog switches in the cross-switching block to keep AOP greater than AON. At currents near zero amps, the sign comparator may switch from "chopping" noise from the transimpedance amplifier.

VDD: VDD is the power input connection for this device. Its input range is from 4.8V to 14V. Bypass to GND using good quality ceramic capacitors.

TYPICAL CHARACTERISTICS CURVES

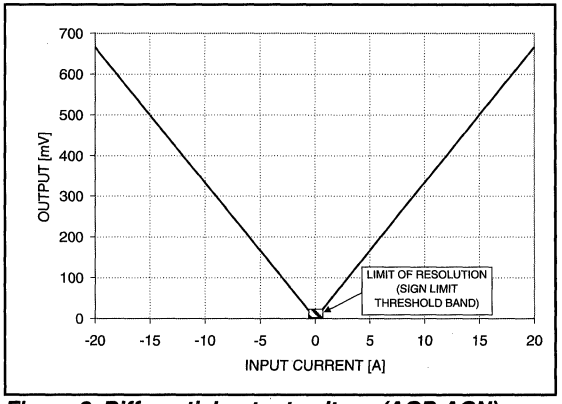


Figure 2. Differential output voltage (AOP-AON) vs. input current (I_{IN}).

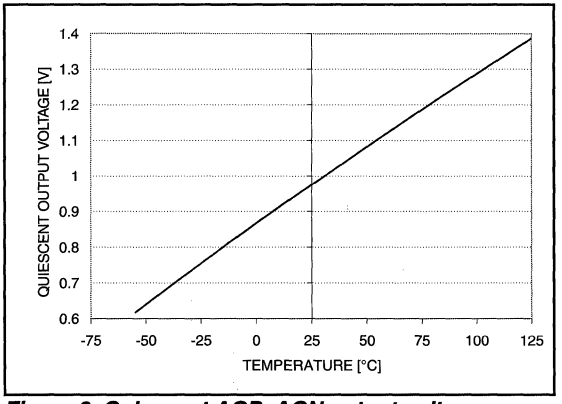


Figure 3. Quiescent AOP, AON output voltage vs. temperature.

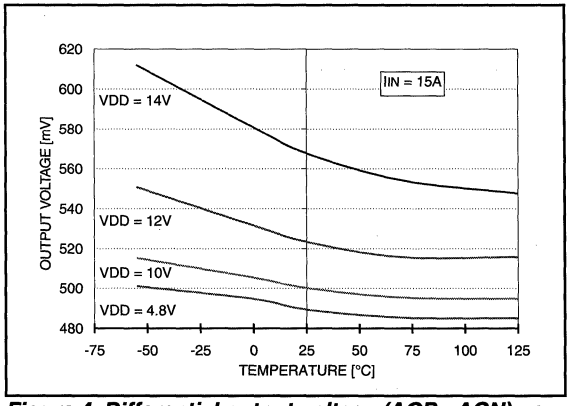


Figure 4. Differential output voltage (AOP - AON) vs. VDD and temperature.

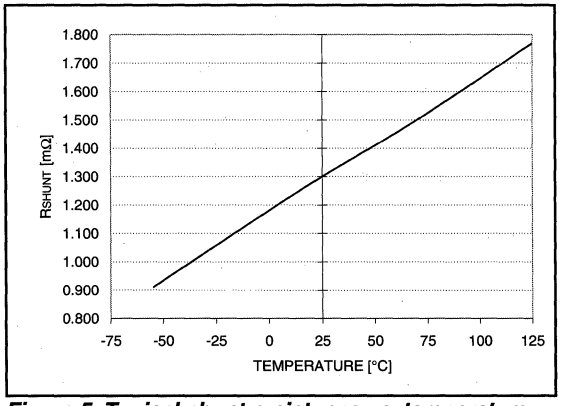
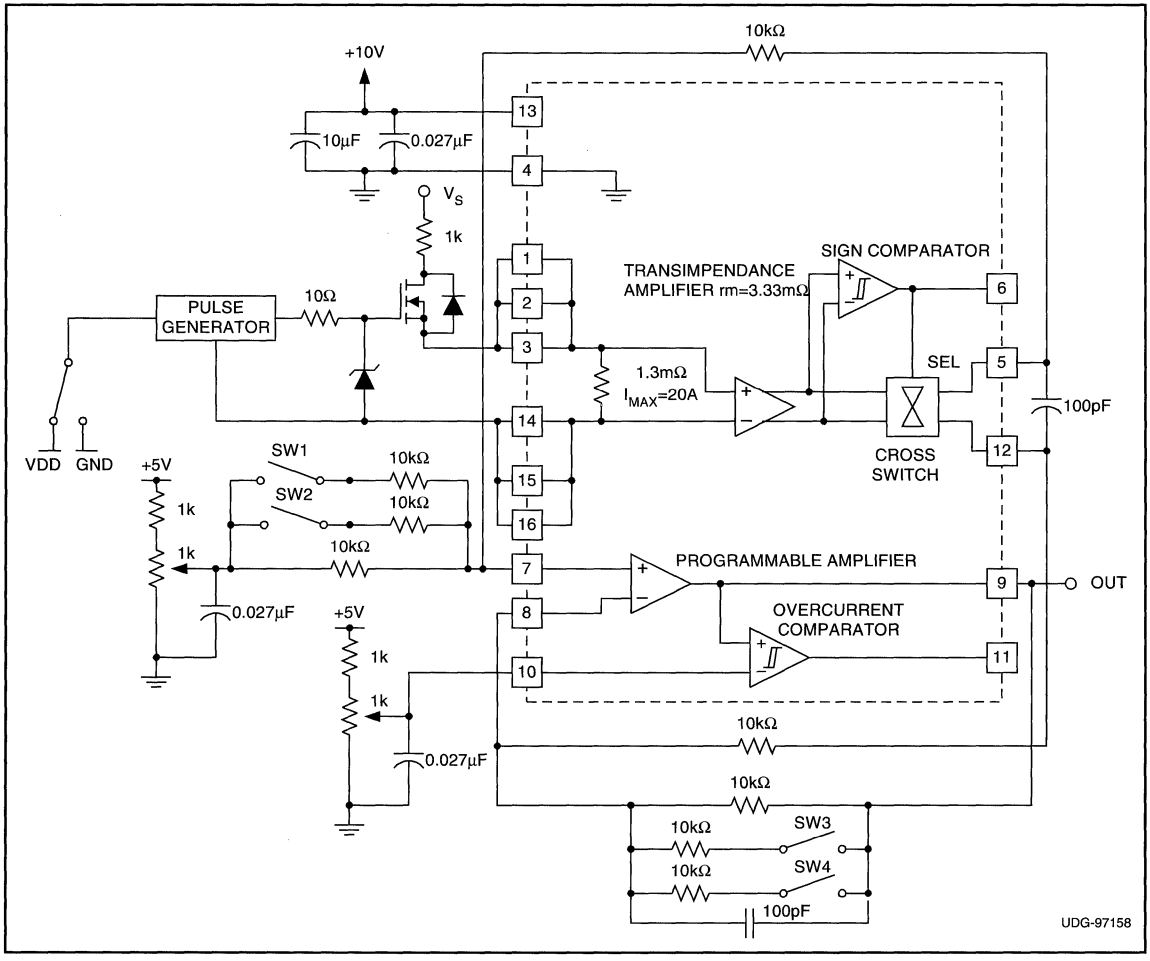


Figure 5. Typical shunt resistance vs. temperature.

LAB EVALUATION CIRCUIT

The circuit shown uses a pulse generator to switch currents while observing the analog voltage of the sensed current. A four position switch can be used to experiment with different gain settings for the programmable amplifier. The OCREF voltage and the NI DC bias voltage can be adjusted with 1kΩ potentiometers to offset the amplifier output and set the overcurrent comparator threshold.



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UNITRODE

10-Bit Serial D/A Converter

FEATURES

- 10 Bit Resolution
- 1.1µs Output Rise Time
- 2.5µs Settling Time to 1%
- Single +5V Supply
- Monotonic
- Low Power Sleep Mode
- Three-wire Serial Interface
- 20MHz Data Rate
- 8 Pin SOIC and DIL Package

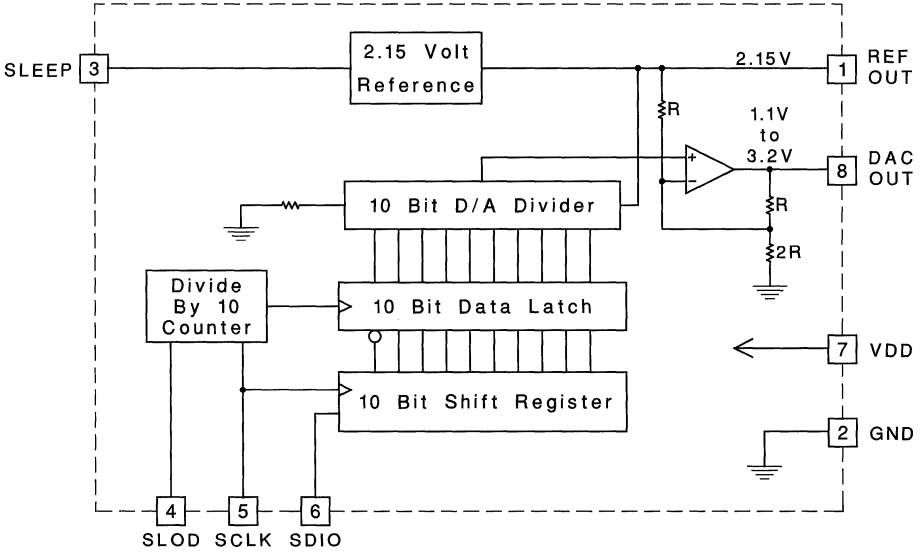
DESCRIPTION

The UCC5950 is a self-contained, microprocessor-compatible 10-bit D/A converter. It contains all of the functions required to take data directly from a three-wire serial data bus and convert it to a precise voltage, including: an input shift register, data latches, a precision voltage reference, a precision 10-bit digital to analog converter, and an output buffer amplifier.

The serial data interface is capable of clock frequencies as high as 20MHz, allowing update rates as high as two words per microsecond. The UCC5950 accepts commands encoded as 2's-complement binary.

The data converter in the UCC5950 is inherently monotonic, making this part ideal for use in closed-loop servo control systems as well as open-loop data conversion. The UCC5950 uses a unique segmented data converter which offers differential linearity better than 1 LSB, integral linearity better than 2 LSB, and fast conversion.

BLOCK DIAGRAM



UDG-95034

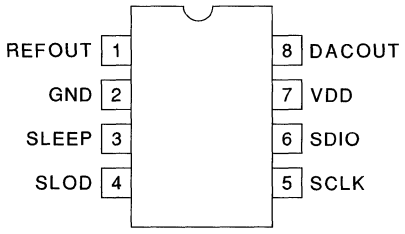
ABSOLUTE MAXIMUM RATINGS

VDD Supply Voltage 6.5V
Input Voltage, Any Input ..... –0.3V to VDD+0.3V
Output Current, Any Output ..... ±5mA
Operating Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature ..... 300°C

All voltages with respect to GND. All currents are positive into, negative out of, the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

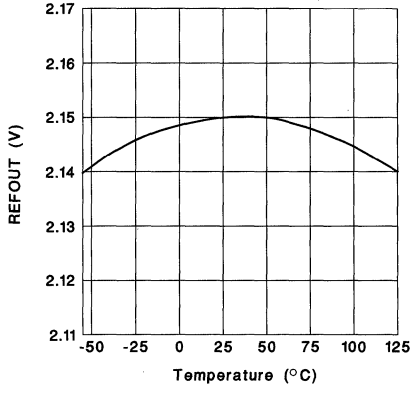
Unless otherwise stated, all specifications apply for 4.5V < VDD < 5.5V, REFOUT Load < 100pF, DACOUT Load < 100pF, 0°C < T_A < +70°C, and T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
OVERALL SECTION					
Supply Current	SLEEP = 0V		1.5	5	mA
Supply Current	SLEEP = 5V		0.1	10	µA
REFERENCE SECTION					
REFOUT Output Voltage		2.10	2.15	2.20	V
REFOUT Change with VDD	4.5V < VDD < 5.5V		1	10	mV
REFOUT Change with Load	–1mA < I_{REFOUT} < 1mA		1	10	mV
D/A SECTION					
Integral Nonlinearity	(Note 1)			2	LSB
Differential Nonlinearity				1	LSB
Full Scale Difference from 1.4924 x REF		–8		8	LSB
Zero Scale Difference from 0.5089 x REF		–8		8	LSB
DACOUT Full Scale Rise/Fall Time	From 10% to 90% of swing (Note 4)		0.7	1.1	µs
DACOUT Full Scale Settling Time (TS)	(Note 2, 3, 4)		1.4	2.5	µs
DACOUT Change with VDD	4.5V < VDD < 5.5V		1.5	10	mV
DACOUT Change with Load	–1mA < I_{DACOUT} < 1mA		1.2	10	mV
LOGIC SECTION					
Logic Input Threshold		1.5	2.5	3.5	V
Logic Input Current	0V < V_{IN} < VDD			5	µA
Logic Input Capacitance	(Note 4)		2.7	10	pF
SLOD Setup Time to SCLK low (TSLS)	(Note 4)	50			ns
SLOD Hold Time from SCLK high (TSLH)	From 10^{TH} SCLK high (Note 4)	50			ns
SDIO Setup Time to SCLK high (TDS)	(Note 4)	15			ns
SDIO Hold Time from SCLK high (TDH)	(Note 4)	7			ns

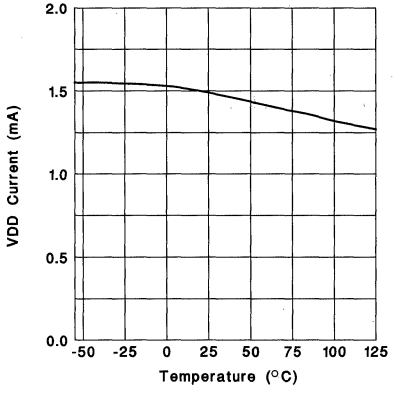
Note 1: Integral nonlinearity is defined as the worst deviation of the converter output from the best-fit straight line through all converter output codes.
Note 2: From 10^{TH} Rising Edge of SCLK.
Note 3: Settling time is to 1% of final value.
Note 4: Guaranteed by design. Not 100% tested in production.

TYPICAL CHARACTERISTICS

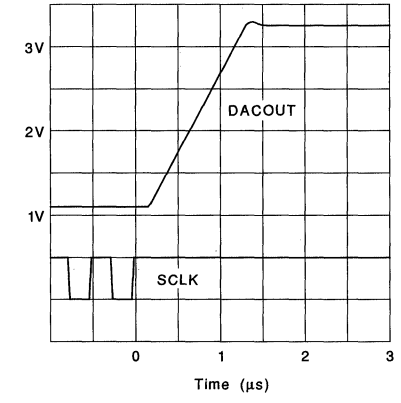
REFOUT vs Temperature



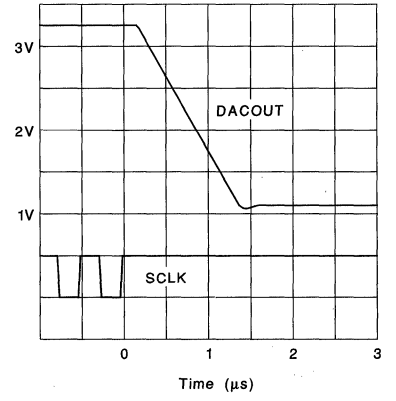
Supply Current vs Temperature



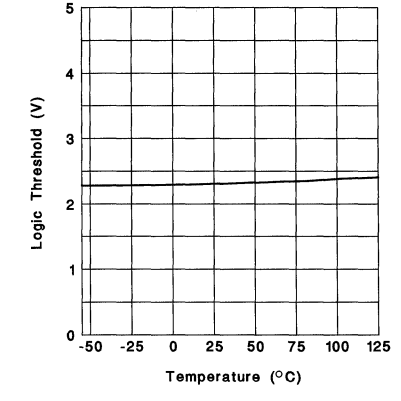
DACOUT Rising Full Scale Step Response



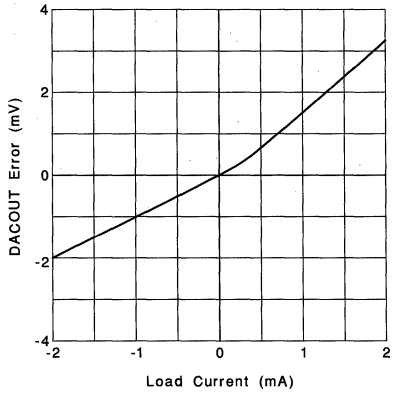
DACOUT Falling Full Scale Step Response



Logic Input Threshold vs Temperature



DACOUT Change with DACOUT Load Current



PIN DESCRIPTIONS

DACOUT: The output of the 10-bit D/A Converter. For best settling time, minimize load capacitance.

DACOUT will go to a voltage between 1.094V and 3.208V depending on the digital code loaded into the latches. The digital code follows this pattern:

Input Code	Typical DACOUT	Significance
1000000000	1.094V	Zero Scale
1000000001	1.096V	
1000000010	1.098V	
...		
1111111111	2.151V	
0000000000	2.153V	Mid Scale
0000000001	2.155V	
...		
0111111110	3.206V	
0111111111	3.208V	Full Scale

GND: All signals are referenced to GND.

REFOUT: The output of the temperature-compensated 2.15V reference. *DO NOT BYPASS REFOUT!* For best stability and transient response, minimize capacitance on REFOUT.

SCLK: Data is clocked into the D/A after SLOD goes low on rising edges of SCLK. After 10 rising edges of SCLK, the data is latched into the D/A output register and the output is updated. Further clock signals on SCLK are ignored until SLOD initiates a new read cycle.

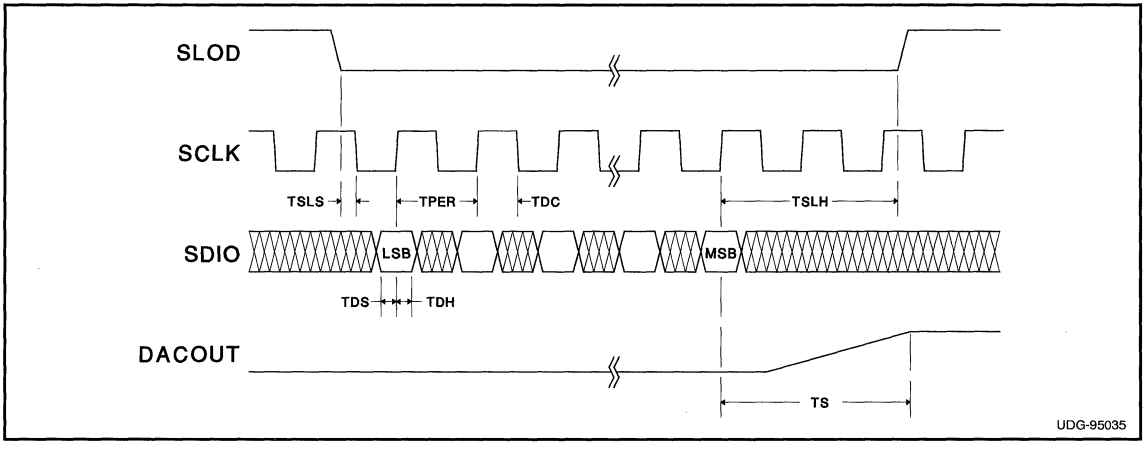
SDIO: After SLOD goes low, data is clocked into the D/A from the SDIO input, on rising edges of SCLK, LSB first. After 10 rising edges, data is latched and converted, and further SCLK and SDIO information is ignored.

SLEEP: SLEEP is the power-down input to the D/A. In systems not requiring this function, wire SLEEP to GND.

SLOD: SLOD is the chip-select input to the UCC5950. SLOD going low selects the D/A and enables clocking of data from SDIO into the D/A. After 10 SCLK pulses, the D/A is updated and SLOD is ignored until SLOD goes high and again goes low.

VDD: All analog and digital functions are powered from VDD. VDD should be a well-regulated supply to minimize output variations. Bypass VDD to GND with a ceramic capacitor very close to the UCC5950.

SERIAL DATA INTERFACE TIMING AND LOGIC TABLE



SLOD	Internal Flag	SCLK	SDIO	Internal Count	Action	DACOUT
1	1	*don't care*	*don't care*	0	*no action*	V(t)
0	0	rising edge	DATA	<10	Shift In DATA	V(t)
0	0	rising edge	DATA	10	Latch New DATA Set Internal Flag Reset Count	V(t+1)
0	1	*don't care*	*don't care*	0	*no action*	V(t)

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Lamp Ignitor Circuit

by Ron Fiorello

Both Fluorescent and HID lamps are becoming increasingly more popular due to their luminous efficiency and quality of the light output. These types of lamps, although they have many advantages over incandescent lamps, have more demanding starting requirements. This design note briefly describes a few different types of possible ignitor circuits and is not meant to be a complete description of all the possible circuit configurations.

Fluorescent Lamp Ignitor Circuit

The ignitor circuit shown in Figure 1 is typically used to start conventional Fluorescent lamps powered by an electronic ballast. Capacitor C

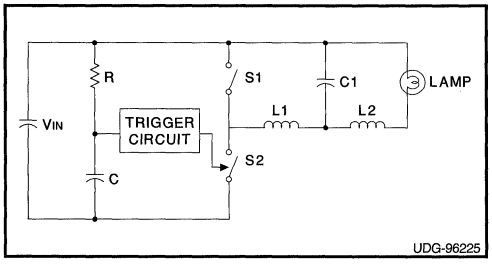

Figure 1.

charges upon application of the input voltage causing the trigger circuit to close switch S2 (where S1 and S2 are typically the power switches in a half bridge converter). This allows the series resonant circuit consisting of L1 and C1 to provide the high voltage (typically 500V) to ignite the lamp. Once the lamp has been lit, the trigger circuit is disabled. The trigger element is usually some type of semiconductor switch such as a DIAC.

Parallel Ignitor Circuit

The circuit in Figure 2 is a simple parallel ignitor circuit for a gas discharge lamp. The trigger cir-

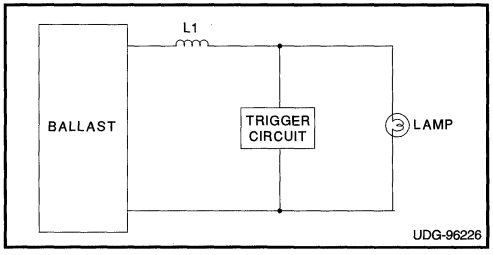

Figure 2.

cuit, which is usually part of the lamp, will repetitively trigger in order to generate the necessary voltage pulses to ignite the lamp. The pulses are due to the storage of energy in the inductor when the switch S1 turns on. The obvious advantage of this circuit is its simplicity since it consists of only two elements, an inductor and switch. Although a simple bimetal switch could be used, the disadvantage of the circuit is that the switch would need to be located in or near the lamp.

Series Ignitor Circuit for HID Lamp

The circuit in Figure 3 is typically used to ignite gas discharge lamps. The trigger circuit drives

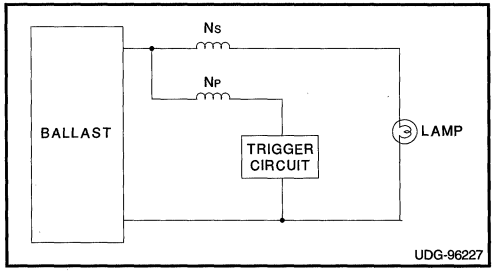

Figure 3.

the primary of a pulse transformer inducing a high voltage on the lamp electrodes. The main advantage of this series ignitor circuit is that the ballast is not exposed to the high voltage transients generated from the ignitor. The main disadvantage, which is true for most ignitor circuits, is that it should be located as close as possible to the lamp in order to minimize the parasitic effects of wiring. This effect could have significant impact on the rise time of the voltage pulse delivered to the lamp, increasing the chances of a no light condition. Methods for reducing the interwinding capacitance of the transformer must be used in order to reduce this parasitic element. The necessary voltages required to ignite HID lamps vary from lamp to lamp and manufacturer to manufacturer, but are usually between 5kV and 25kV for short arc lamp and 20kV to 50kV for long arc lamps.

The circuit in Figure 4 shows a HID ballast output stage driving a full bridge power stage for an AC lamp. Upon application of power to the output stage of the ballast, before the lamp is lit, Q1 and Q4 are turned on and held on until such time that lamp ignition has occurred. It is sometimes necessary to hold Q1 and Q4 on even after ignition occurs until the arc discharge is fully established. During this time, C1 is allowed to charge up to predetermined level set by the threshold voltage of the switch S1. S1 must be capable of switching significant current in a short period of time (typically hundreds of amps in a fraction of a microsecond). This high current capability is necessary to get the arc discharge to form properly on the tips of the electrodes of the lamp. Once the arc discharge has occurred, the ignitor circuit is rendered inactive because the lamp impedance will drop drastically and the capacitor voltage will never reach the threshold level of the switch.

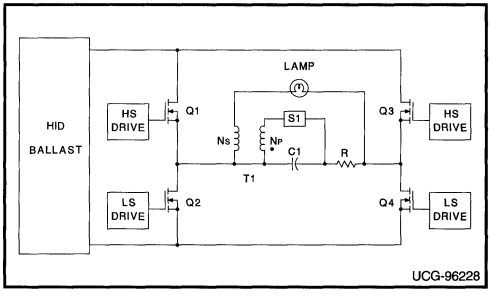

Figure 4.

Assume, for instance, that the threshold voltage of S1 is 400V. C1 will be allowed to charge up to 400V before an ignition pulse occurs. This assumes that the open circuit output voltage of the ballast is limited to 600V before ignition of the lamp. The energy stored in the capacitor is $(1/2)CV^2$. Assuming a lossless switch for S1, all energy stored in C1 is then dumped into the transformer primary winding inductance. The primary inductance required to support this energy can be determined using the above assumption from:

$$(1/2) \bullet C1V^2 = (1/2) \bullet LpI^2$$

The turns ratio from primary to secondary of T1 can be found based on the ignition voltage of the lamp. If the pulse transformer were ideal then all of the energy stored in the capacitor would be transferred to the lamp electrodes. We know, however, that this is not the case. Depending on the winding method used for the transformer, there can be significant energy lost to the interwinding capacitance. Because of this, it is necessary to take precautions to minimize this element. Usually a turns ratio 25% to 50% higher then that calculated is required to generate the necessary voltage on the secondary since it will not be possible to eliminate this capacitance entirely.

Care must be taken in choosing the secondary ignitor inductance since it is in series with the lamp and is being excited with an AC voltage. Too large an inductance will reduce the excitation voltage to the lamp. Luckily the excitation frequency of this voltage is typically between 200Hz and 1000Hz so the AC impedance can be kept to a minimum with a fairly large inductance value. The secondary inductance also provides some beneficial filtering of the current seen by the lamp. This filtering helps reduce the chance of acoustic resonances being excited in the arc

tube by the switching frequency current ripple of the ballast. These resonances can cause problems with the lamp optics as well as lead to destruction of the lamp if left unchecked. Because of this, AC HID lamps are typically driven with a low frequency square wave current.

References

[1] Waymouth "Electrical Discharge Lamps" MIT Press

[2] Murdoch "Illumination Engineering from Edison's Lamp to the Laser" Visions Communication

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UCC3750 Demonstration Board Operating Guidelines

by Dhaval Dalal

The UCC3750 demonstration board is designed to illustrate a typical ring generator application using the UCC3750. It is designed to provide a 20Hz, 85V RMS output for loads up to 10 -15 REN with no offset voltage. Accompanying schematics and parts list provide details of the circuit.

To ensure proper operation, apply +5V between VDD and GND inputs. The circuit draws about 45 mA of current and a sinusoidal output of 1Vpp (centered around 3V) should appear at pin 9 of the UCC3750. The frequency of the sinusoid is set by the DIP switches(SW1). With S1 and S2 in the ON (down) position, a 20Hz signal is obtained. With other settings of these switches (as per datasheet information), other frequencies can be obtained. Please note that it can take about 3 seconds for the crystal oscillator to stabilize after power-up or a change in setting.

The power stage can be evaluated by applying the input voltage (40V - 60V) across VIN and RTN. The VB terminal should be connected to GND for zero offset. For true isolation, the input voltage return and VDD ground should be separate. The output voltage can be observed (and load connected) across terminals labeled VOUT and GND.

The AC current limit for the board is presently disabled by shorting pins 13 and 14. It can be set at 150mA by removing the short. In an AC limit condition, the sine-wave reference is attenuated and the output AC level goes down for 5 cycles. However, there can be a transient overshoot that can make the output temporarily saturate before the current limit sets in. The DC limit is set for +/-500 mA and is sufficient for most situations. The AC limit circuit is noise sensitive and needs proper filtering if it is enabled. Based on the value of R8, C24 should be chosen to introduce a pole just above the ring frequency in order to minimize any high frequency noise. Also, introducing a scope probe at pin 13 can cause the circuit to go into AC limit.

For different output voltage levels and offset requirements, values of R10-R15 will need to be changed along with the compensation. -48V operation based on the VB input may necessitate higher values of C16 and a smaller R15. Please refer to the applications section of the datasheet for further information. With certain capacitive loads, the output voltage waveform can see distortion in modes 2 and 4. This distortion can be minimized by using a transformer with lower magnetizing inductance (with the associated penalty of higher peak currents).

Reference Designator	Part Number/Type	Manufacturer	Part Description
CR1	BYV99	Philips	
CR2, CR3	BYV26C	Philips	600V, 1A, 30ns
CR4	Short w/ jumper		
CR5 - CR12	1N5818	Diodes, Inc.	30V, 1A Schottky
Q1	IRF640	IR	200V, 0.18Ω
Q2	MTP2P50	Motorola	500V, p-channel
Q3	IRF840	IR	500V, 0.85Ω
Q4	2N7001	Diodes Inc.	60V, 1.2Ω
Q5	2N5457	National	n-channel JFET
Q6	MPSA06	National	npn - 80V, 50mA

Table 1. UCC3750 Demonstration Board Parts List

Reference Designator	Part Number/Type	Manufacturer	Part Description
C1, C2	HFS series, Aluminum	Panasonic	100µF, 63V
C3	Film	Panasonic	0.1µF, 50V
C4	ECQ-E(F)	Panasonic	1µF, 250V
C5, C9	Film	Panasonic	0.47µF, 50V
C6	Film	Panasonic	0.1µF, 50V
C7	Ceramic	Panasonic	470 pF, 63V
C8	Film	Panasonic	1µF, 50V
C10, C16	Ceramic/Tantalum	Panasonic	2.2µF, 50V/25V
C11, C12	Ceramic	Panasonic	0.22µF, 50V
C13	Ceramic	Panasonic	1µF, 63V
C14	Ceramic	Panasonic	1000 pF, 50V
C15	Omit		
C17	Film	Panasonic	0.047µF, 50V
C18	KA Series - Aluminum	Panasonic	22µF, 16V
C19	KA Series - Aluminum	Panasonic	100µF, 16V
C20, C21	Omit (short)		0Ω
C22	Ceramic	Panasonic	1nF, 500V, 10%
C23	Film	Panasonic	0.47µF, 63V
C24	Ceramic	Panasonic	3.3nF, 50V
T1	CTX08-13484-X1	Coiltronics	Power Transformer
T2	CTX08-13619-X1	Coiltronics	Gate Drive Transformer
U1	UCC3750N	Unitrode	
R1, R2, R6, R18, R25			10k
R3, R16, R17, R23			4.7Ω
R4			16.2k
R5			30.1k
R7			100k
R8			0.0k
R9			1Ω, 1W
R10			200k
R11, R20, R21			1M
R12			3.32k
R13			61.9k
R14			374k
R15			15k
R19			Not used
R22			1k
R24			Omitted
R26			560k

Table 1. UCC3750 Demonstration Board Parts List (continued)

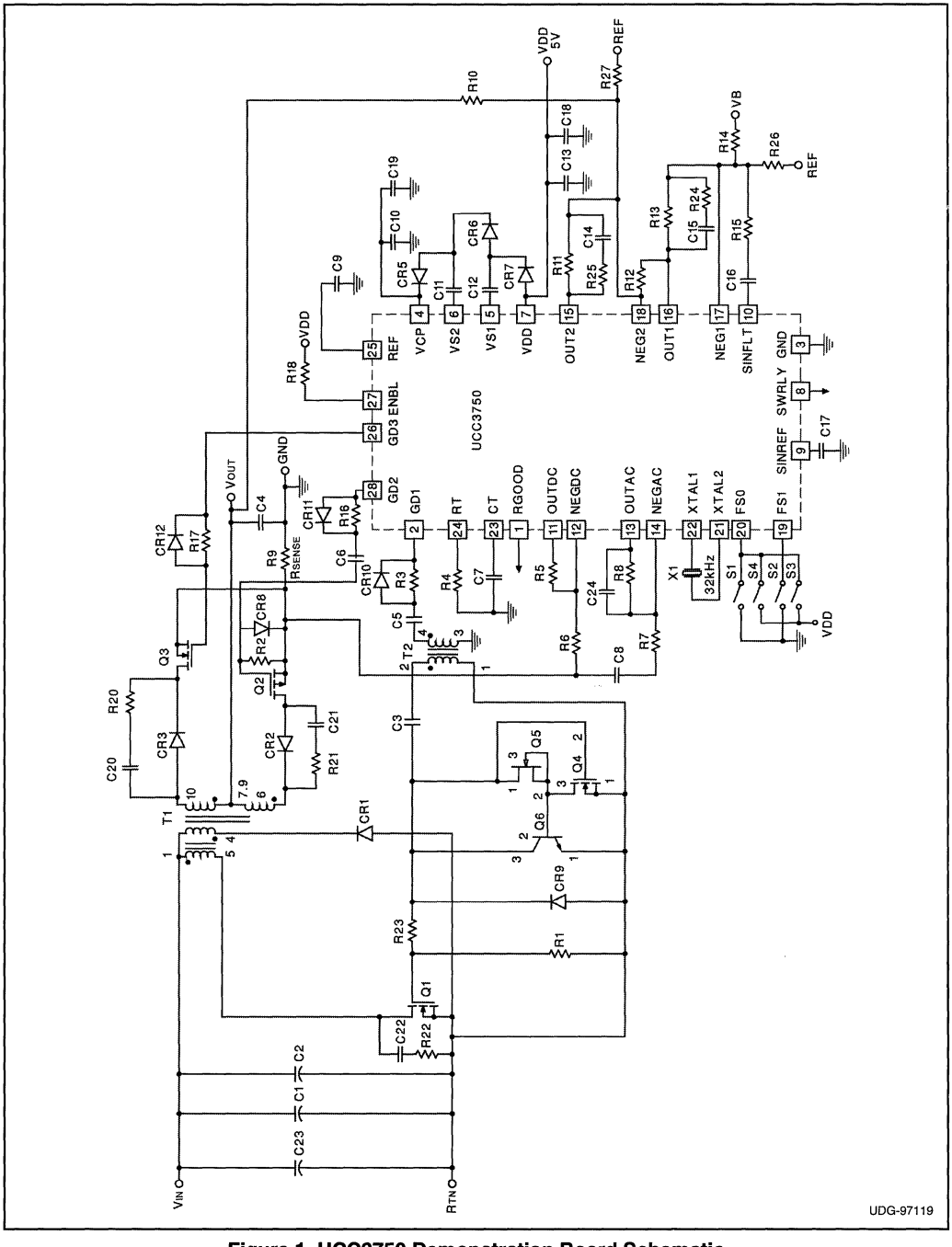

Figure 1. UCC3750 Demonstration Board Schematic

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Design Note

UCC3926DS ± 20A Integrated Current Sensor, Evaluation Board and List of Materials

By Phil Cooke

INTRODUCTION

The UCC3926 integrates a current sense element and differential amplifier into a single device and may be evaluated with this demonstration board. The current sense element is essentially non-inductive and is implemented as an integral part of an integrated circuit lead frame with only 1.3mΩ of resistance. All necessary voltage amplification is accomplished using a chopper stabilized transimpedance amplifier with Kelvin sense leads. A second uncommitted, user configurable, operational error amplifier provides common mode filtering and programmable voltage gain from the chopper amplifier stage. Over current indication is provided by an over current comparator with an adjustable threshold. Since the transimpedance amplifier provides the absolute value of the current, polarity is indicated by a sign comparator output, see Fig. 1.

OPERATING GUIDELINES

As shown in Fig. 2 the current sense terminals of the demonstration board are labeled CSP (TB1) and CSN (TB2) which connect to the external system in which current is to be measured. Shorting jumper J1 allows low side, GND referenced, current sensing. Similarly shorting jumper J2 allows high side, VDD referenced, current sensing. Only one jumper should be used, either J1 or J2, otherwise VDD is shorted to GND. Note that the operating common mode range of CSP and CSN is either VDD ±75mV or GND ±75mV. External power is supplied through connector TB3. Zener diode D1 provides a 4.3V reference for the multiturn pots R10 and R12.

The programmable amplifier gain is configured by selecting resistors R1, R2, R3, R4 (optional), R5, and R6 (optional). The gain is preset to one by us-

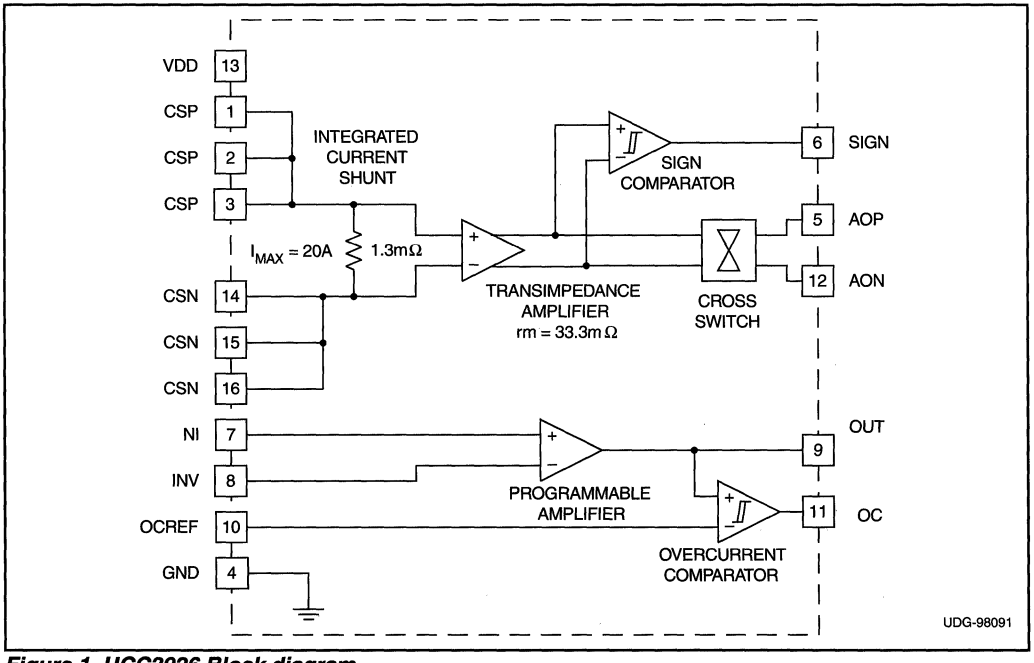

Figure 1. UCC3926 Block diagram.

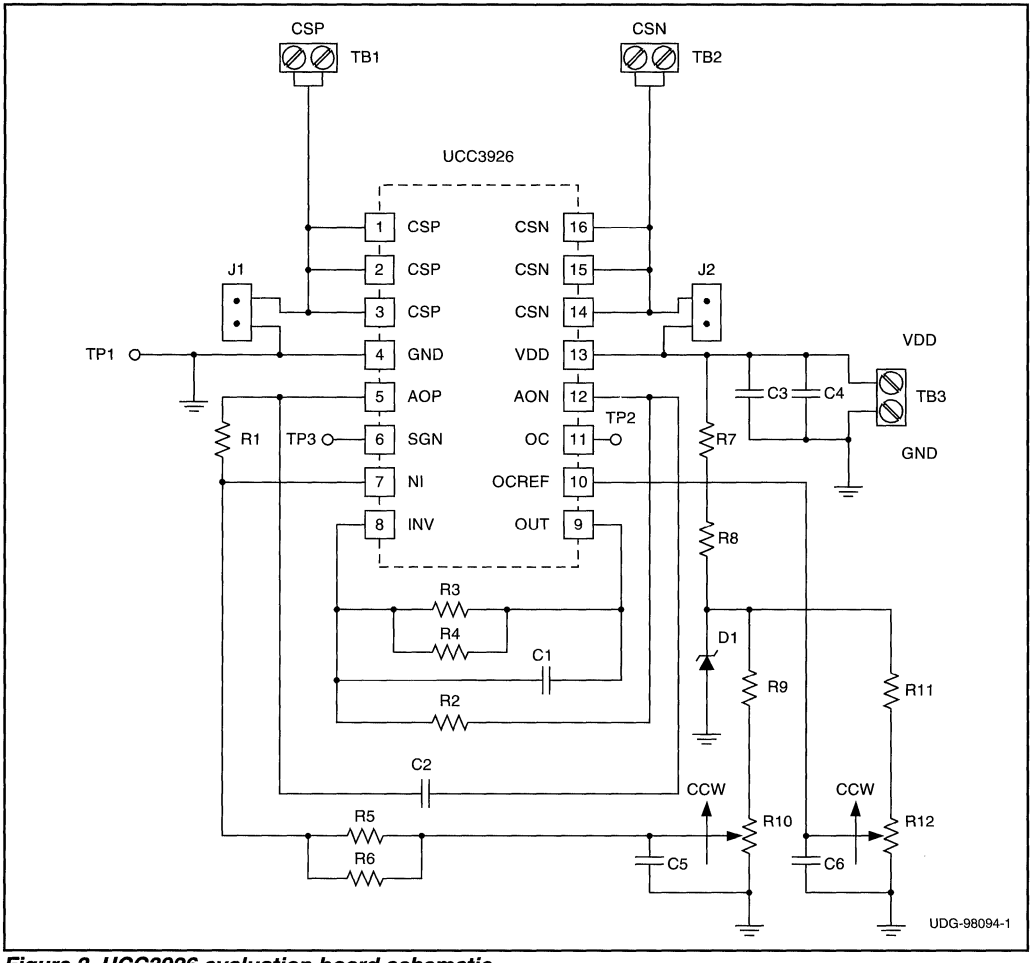

Figure 2. UCC3926 evaluation board schematic.

ing R1=R2=R3=R5=5.9kΩ. It is prudent to use values below 10kΩ to minimize noise coupling into the differential amplifier. C1 provides a high frequency noise pole which helps to reduce any differential mode chopper noise. Another optional capacitor, C2, filters spikes between AOP and AON. A non-inverting bias voltage can be used to offset the output of the programmable differential amplifier using R10.

The over current reference is set to the highest desired voltage as measured at pin 9 (OUT) by adjusting R12. Turning this pot counterclockwise (CCW) increases the OCREF voltage which increases the current limit level. The exact value depends on the external gain used for the programmable amplifier in the application and is easily calculated by referring to Fig. 2 with the appropriate component value substitutions.

In normal operation there is some common mode, square-wave chopping, that is observed at AOP and AON with respect to GND. This is to be expected and the purpose of the differential amplifier stage is to reject this noise and transform the signal to GND reference.

For more complete information, pin descriptions and specifications for the UCC3926 ± 20A Integrated Current Sensor, please refer to the UCC3926 data sheet or contact your Unitrode Field Applications Engineer at (603) 424-2410.

Table 1. UCC3831 evaluation board list of materials.

Reference Designator	Description	Manufacturer	Part Number
R1,R2,R3,R4,R5,R6	5.90kΩ, 0603, 1/16W, ±1%	Panasonic, Digikey	P5.90KHCT-ND
R7,R8	412Ω, 1206, 1/8W, ±1%	Panasonic, Digikey	P412FCT-ND
R9,R11	1kΩ, 0805, 1/10W, ±1%	Panasonic, Digikey	P1.00KCCT-ND
R10,R12	1kΩ, Multiturn Pot, Cermet, Thru Hole	Bourns, Digikey	3296Y-102-ND
C1,C2	100pF, 50V, 0603, NPO, ± 5%	Xicon, Mouser	140-CC504N101J
C3	10µF, 16V, 3.5mm x 2.8mm, Tantalum	Panasonic, Digikey	PCS3106CT-ND
C4,C5,C6	0.027µF, 50V, 0805, X7R, ± 10%	Xicon, Mouser	140-CC501B273K
D1	4.3V, SOD123, 410mW, Zener	Liteon, Digikey	BZT52-C4V3DICT-ND
J1,J2	Shorting Jumper, Thru Hole	3M, Digikey	929950-00-ND
U1	± 20A Integrated Current Sensor	Unitrode	UCC3926DS

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POWERING A 35W DC METAL HALIDE HIGH INTENSITY DISCHARGE (HID) LAMP USING THE UCC3305 HID LAMP CONTROLLER

by Ron Fiorello

Unitrode Corporation

ABSTRACT

High Intensity Discharge (HID) metal halide lamps are being used in more and more applications where lamp color, long life and efficiency are important. From automotive and industrial lighting to theatrical and stage lighting, HID promises to be the light of the future. HID lamps offer many advantages over many other types of discharge lamps because of their luminous efficiency (their ability to convert electrical power to visible light) and the color of the light output is closer to an ideal source (the sun) then other types of discharge lamps i.e.; low pressure sodium, high pressure sodium etc.

The purpose of this application note is to demonstrate the use of the UCC3305 HID lamp controller IC. Information is presented on a design example to help the user better understand all of the controllers many features.

INTRODUCTION

The following section specifies typical design requirements necessary of an HID ballast which would be powering a DC headlamp in an automotive application. The headlamp used in this application is a 35W DC metal halide lamp manufactured by OSRAM/SYLVANIA.

Input Voltage Requirements - 9 to 16VDC

Startup Requirements - Must run/startup down to 6VDC

Protection/Fault Monitor- Protection against input overvoltage, output open circuit and output short circuit.

Power Regulation - Regulate power to the lamp within +5% over a lamp voltage variation of 60 to 100VDC.

Lamp Ignition Voltage - Provide an open circuit voltage of greater then 500VDC at start-up in order to ignite the lamp.

Efficiency - greater than 85%.

Cold Start - The light output on initial start-up must be within a window as specified by SAE J2009.

Hot Restrike - The ballast must be able to properly light the lamp when hot without a cool down period.

The load presented to the ballast by the lamp is non-linear. Before ignition occurs, the lamp draws very little current from the ballast. The ballast sees essentially an open circuit on its output at start-up. The open circuit voltage feeds an ignitor circuit (internal to the lamp) which steps-up the voltage in order to provide the approximately 20kV ignition voltage necessary for the lamp. Upon ignition, metals and gases inside the lamp are ionized causing the lamp voltage to collapse. During ionization, the lamp will require significant current from the ballast to properly establish and maintain the arc discharge. During this time, the current into the lamp must also be controlled to protect the lamp electrodes [1].

The initial start-up power into the lamp is higher then its steady state value. This is necessary in order to get the light output up to 75% of its steady-state value within 2 seconds, which is a requirement for an automotive application as specified under SAE J2009. The lamp voltage right after the glow to arc transition varies from lamp to lamp but is usually between 20 and 40VDC. As the lamp warms up and the internal pressure inside the arc tube increases, the voltage begins to rise and will gradually reach a steady-state value of between 60 and 110VDC after 150 seconds. This depends on the age of the lamp. A typical steady-state voltage of this type of lamp is between 75 and 90VDC.

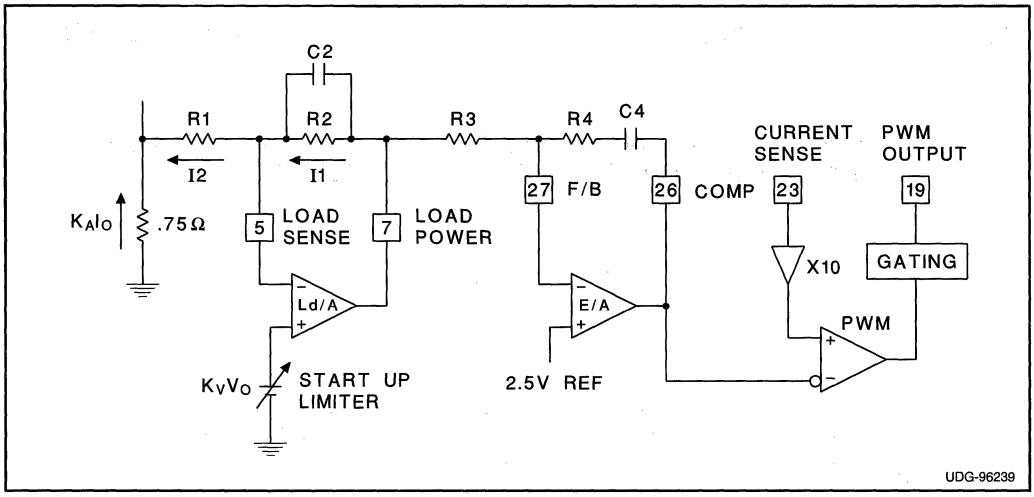


Figure 1. Power Regulation Loop

Optimal converter topology

The optimal converter topology for this application would meet the following requirements;

1) Output voltage that is capable of being higher then input voltage.
2) Low input current ripple for reduced input filter requirements
3) High efficiency
4) Minimal number of magnetic components
5) Minimal number of power semiconductors

There are a few candidate topologies which meet some of the above requirements. The best choice for this particular application is the SEPIC converter which meets all of the above requirements for a 35W lamp. The schematic of this circuit is shown in Figure 2 [2].

The UCC3305 HID controller

The features of the UCC3305 HID controller are outlined below:

- OV input protection
- Output fault protection/timing
- Power regulation vs. lamp voltage
- Lamp start-up/cool down simulation
- Current-mode control
- Fixed frequency operation
- DC or AC lamp drive capability
- High current drive capability
- On board charge pump to provide gate drive down to 6VDC
- Adjustable start-up to steady-state current ratio

Below is a summation of the different functional blocks of the UCC3305 and their major electrical characteristics;

VCC/OV Protection/VREF/VBOOST Block

VCC Maximum Voltage - 8 Volts
Must bypass with 0.1μF to 1.0μF Ceramic Monolithic Capacitor as close to the IC as possible

OV Threshold - Internal Comparator with reference voltage tied to internal 5V. OV threshold adjustable with external resistor divider

VREF:
5.0V Trimmed Bandgap Reference
Must bypass with 0.1μF Low ESR Capacitor as close to the IC as possible

VBOOST Max Voltage - 12 Volts
Supplies drive for output drive stage
Must bypass with 0.1μF to 1μF Ceramic Monolithic Capacitor as close to IC as possible

Output Drive Stage:

PWMOUT:
1.0A Peak current drive capability

Q and Q not outputs
Outputs to drive external bridge via external MOSFET drivers Output frequency is fs/512
At lamp start, outputs are disabled via RC from NOT-ON and DIV. PAUSE

Oscillator:

OSC:
Sawtooth Oscillator with Programmable Frequency D_{MAX} from 0% to 100% possible
With R_{SET} = 150k, Fs ~ 22xe-6/C_{OSC}
Maximum operating frequency is 300kHz

Load Power and Main Error Amplifiers:

LOADSENSE, LPOWER, COMP AND FB

The LOADSENSE amplifier, the main error amplifier and its external associated resistors and capacitors will determine where the peak of the power curve occurs as well as the shape of the frequency response of the ballast. Below is an analysis of this operational block based on the 35W DC lamp in an attempt to show how the power curve of the ballast is determined for this particular application.

From the simplified schematic of this loop shown in Figure 2 below, the power curve equation is determined as follows;

Power curve equation

From the simplified schematic of the power regulation loop, shown in Figure1, the currents I_1 and I_2 can be found as follows;

$$I_1 = \frac{V_{REF} - K_V \bullet V_O}{R2}$$

$$I_2 = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

where K_V and K_I are the proportionality constants for voltage and current respectively; since

$$I_1 = I_2$$

$$\frac{V_{REF} - K_V \bullet V_O}{R2} = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

rearranging the above equation and solving for I_O,

$$K_I \bullet I_O = (V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - K_V \bullet V_O$$

$$I_O = \left[(V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - KV \bullet Vo\right] \bullet \frac{1}{K_I}$$

since

$$P_O = V_O \bullet I_O$$

substituting the expression found for I_O into the power equation,

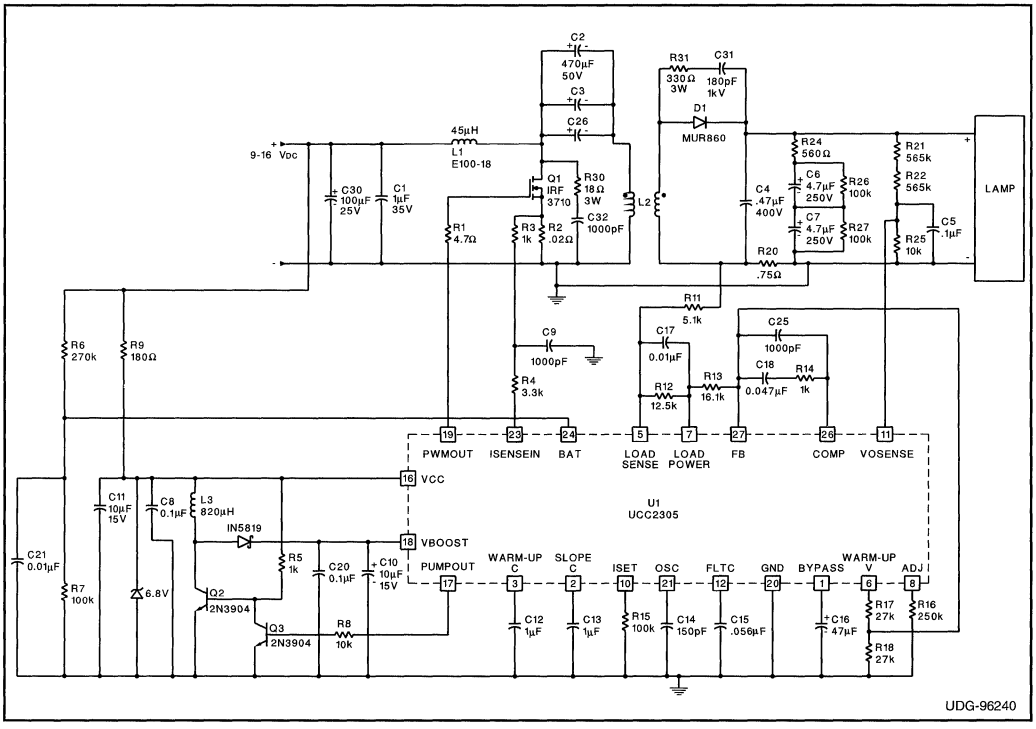
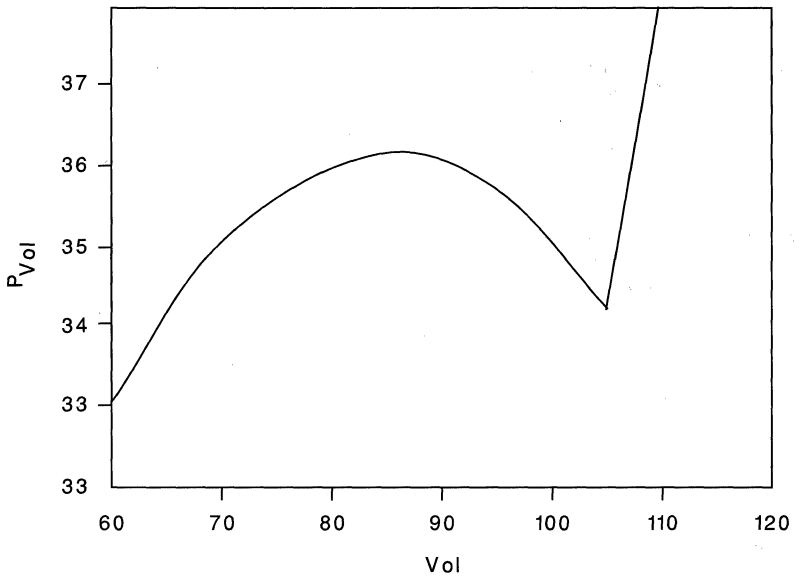


Figure 2. 35W DC HID Ballast Schematic



The expression for P_{O1} is valid for lamp voltages from 60 to 105V. The expression for P_{O2} is valid for lamp voltages above 105V (This is due to the limiter block inside the UCC3305). Above approximately 105V, the lamp will be driven in a constant current mode which results in the straight line for power vs. lamp voltage as shown. The output power can be regulated with a variation of less than ±5% from a nominal of 34.5W with a lamp voltage variation from 60 to 110V.

As the lamp ages, the voltage will normally increase due to the lamp electrode material erosion over time. Therefore it is beneficial to limit the current available to the lamp above a certain voltage.

Figure 3. Calculated Power Curve vs. Lamp Voltage of UCC3305 Controlled 35W Ballast Powering DC Metal Halide Osram/Sylvania Lamp

$$P_O = \frac{V_O}{K_I} \bullet \left[V_{REF} \bullet \frac{R1}{R2} - K_V \bullet V_O \bullet \left(1 + \frac{R1}{R2}\right)\right]$$

where

$$R_{EQ} = \frac{R_A \bullet R_B}{R_A + R_B}$$

from block diagram of UCC3305, where 1/120 is the voltage divider attenuation ratio. R_{EQ} is the parallel combination of the 100k and the 5.35k internal resistors.

$$K_V \approx \frac{1}{120} \bullet \frac{R_{EQ}}{R_{EQ} + 7.85k}$$

$R_A = 100k$

$R_B = 5.35k$

$R_{EQ} = 5.078 \bullet K$

$K_V \approx 0.0032$

$K_I = 0.75$

K_I is equal to the current sense resistor value

Substituting the values found for the constants K_V and K_I and the actual resistor values used in the circuit into the power equation, the power curve can be plotted for a range of lamp voltages as shown in the figure below.

$K_V \approx 0.0032$

$R_1 = 4.7k$

$K_I = 0.75$

$R2 = 16k$

$V_{O1} = 60, 65..110$

$V_{REF} = 2.5$

$V_{O2} = 110, 115..120$

$$P_{Vo(1)} = \frac{V_{O1}}{K_I} \bullet [(\frac{R1}{R2}) \bullet V_{REF} - K_V \bullet V_O1 \bullet (\frac{R1}{R2} + 1)],$$

$$P_{Vo(2)} = \frac{V_{O2}}{K_I} \bullet [(\frac{R1}{R2}) \bullet V_{REF} - 0.322 \bullet (\frac{R1}{R2} + 1)]$$

Current sense comparators/amplifiers

The INPUT ISENSE comparitor/amplifier inside the UCC3305 provides cycle by cycle current control as in a typical peak current-mode controller. An added feature allows the user to program the start-up to steady-state current ratio of this current. This allows the ballast to provide increased power to the lamp at start-up in order to get the lamp light output up to its steady-state level as quick as possible. The simplified schematic of this section is shown in Figure 4 below.

By the addition of an external resistor from the ADJ. pin to ground, this ratio can be programmed. At the instant of start-up, the output of the limiter is a t zero volts since the WARMUPC capacitor has not charged. Because of this, the inverting input to amplifier A1 is at ground with 20µA • R_{ADJ} volts on its non-inverting input. As an example, if R_{ADJ} = 150k, then the voltage at the non-inverting input is 3V.

$$V_{O(-)} = -(\frac{V_{(-)}}{83k}) \bullet 10k$$

$$V_{O(-)} = -(\frac{V_{(-)}}{83k}) \bullet 10k + V_{(+)}$$

where

$V_{O(+)}$ = the contribution of the non-inverting input to V_O of A1

$V_{O(-)}$ = the contribution of the inverting input to V_O of A1

$V_{(+)}$ = the voltage at the non-inverting input of A1

$$V_O = V_{(+)} \bullet (\frac{10k}{83k} + 1) - V_{(-)} \bullet (\frac{10k}{83k})$$

on start-up,

$$V_{(-)} = 0$$

so;

$$V_O = 3.36 \text{ Volts}$$

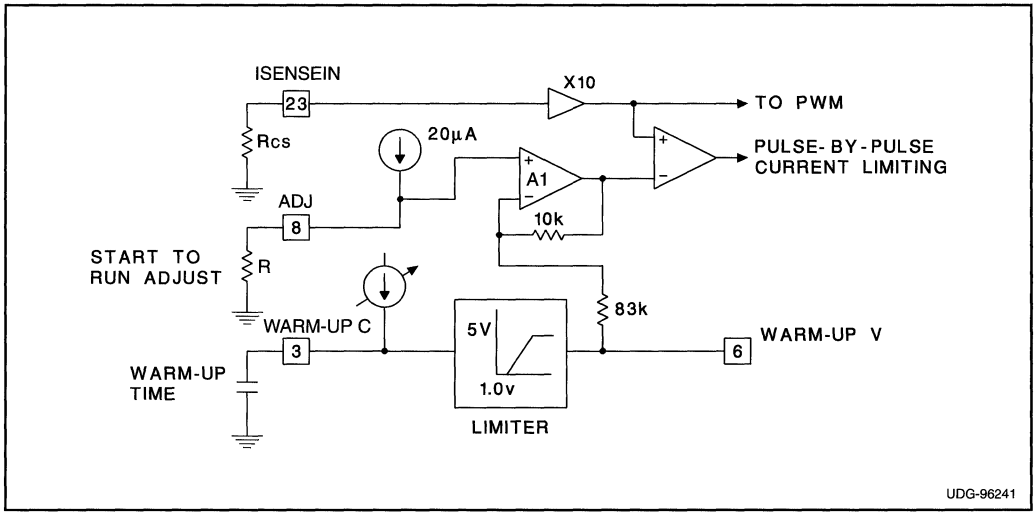


Figure 4. Current Sense / Limit Block

The current sense threshold is then;

$$V_S = \frac{3.36}{10}$$

$$V_S = 0.336 \text{ Volts}$$

This translates to a peak switch current at start-up of;

$$I_P = \frac{3.36}{0.02}$$

$$I_P = 16.8 \text{ Amps}$$

This current threshold will gradually decrease as the WARMUPC capacitor charges up to 10V.

The limiter limits the inverting input of A1 at steady-state to 5V. The current limit at this point is then;

$$V_O = 3.36 - 0.6$$

$$V_O = 2.76 \text{ Volts}$$

$$I_P = \frac{0.276}{0.02}$$

$$I_P = 13.8 \text{ Amps}$$

The switch current in the SEPIC converter is a combination of the input inductor current plus the reflected load current. At steady-state, 9 V_{IN}, the peak-to-peak current thru the output rectifier is approximately 1A. This reflects back to the primary as 6A into the switch plus 3.1 Amps from the inductor. The total current thru Q1 is then 9.1 Amps.

Output current limit on start-up

From Figure 2 the start-up current limit into the lamp can be determined. On start-up, the WARMUPV pin, which is a buffered version of WARMUPC, is at ground.Therefore, the two 27k resistors are in parallel resulting in an equivalent resistance of 13.5k. The current that flows from FB to ground is then;

$$I = \frac{2.5}{13.5k}$$

$$I_1 = 185\mu A$$

The voltage at the output of the load sense amplifier is then;

$$V_{LS} = 185\mu A \bullet 16k + 2.5V$$

$$V_{LS} = 5.46V$$

The current which flows thru the feedback resistor of the load sense amplifier is;

$$I_{LS} = \frac{5.46 - 0.30}{12k}$$

$$I_{LS} = 430\mu A$$

Assuming that the current which flows thru the feedback resistor also flows thru the inverting input resistor, the voltage across the output current sense resistor is;

$$V_{CS} = 0.30 - (430\mu A \bullet 5.1k)$$

$$V_{CS} = 1.89V$$

(the negative sign of the voltage is ignored since this is defined as positive current)

$$I_L = \frac{1.89}{0.83}$$

$$I_L = 2.3 \text{ Amps}$$

This defines the maximum startup current which flows into the lamp at ignition. The current into the lamp will decay exponentially due to the voltage charging characteristic of the WARMUPC and SLOPEC capacitors. The current will decay to a steady-state value of approximately 450mA after a period of time given by the time constant of the internal 50 Meg resistor and the capacitor placed from the SLOPEC pin to ground. In this example, the time to steady-state is 150 seconds from:

$$t = 50 \exp(6) \bullet C_{SLOPEC}$$

The capacitors used for the SLOPEC and WARMUPC functions must have low leakage characteristics since they are charged from nanoamp current sources internal to the IC. Any significant amount of leakage current caused by these components will have an effect on the output power regulation characteristic of the ballast.

Slope compensation resistor

Slope compensation in the UCC3305 is provided by the addition of an external resistor in series with the INPUT ISENSE pin. This resistor adds a portion of the oscillator ramp into the current sense signal to provide the necessary slope compensation for duty cycles exceeding 50%. The amount of slope compensation that is needed is dependent on the topology used as well as the inductor values chosen. In the SEPIC converter, both input and output inductors need to be considered when determining how much slope compensation is necessary.

The current sense comparator compares the current sense signal to the output of the error amplifier to determine the duty cycle of the power switch [3]. V_I, the voltage at the current sense resistor can be determined as follows

$$V_I = R_I \bullet \left(\frac{N_S}{N_P}\right) \bullet (I_{OAV} + M2 \bullet t) + R_I \left(I_{IN} + \frac{M_1}{2} \bullet t_{OFF}\right)$$

where;

N_S = number of turns of secondary winding of L2

N_P = number of turns of primary windings of L2

R_I = current sense resistor

L_{OAV} = secondary average output current

M_2 = down slope of secondary current thru L2

M_1 = down slope of primary current thru L1

I_{IN} = average input current

t_{OFF} = off time of switch

The above equation can be rewritten as follows;

$$V_I = R_I \bullet \left(\frac{N_S}{N_P}\right) \bullet (L_{OAV} + M2 \bullet (T - t_{ON})) + R_I \left[I_{IN} + \frac{M_1}{2} \bullet (T - t_{ON})\right]$$

The first term is the contribution of the output current thru L2 (output inductor) to the current sense resistor. The second term is the contribution of the input current thru L1 (input inductor) to the current sense resistor

This signal is set equal to the voltage at the output of the error amplifier. This results in the following equation after rearranging terms;

$$R_I \left(\frac{N_S}{N_P}\right) \bullet L_{OAV} = V_{EA} + t_{ON} \bullet \left(\frac{M_1}{2} \bullet R_I + R_I \frac{N_S}{N_P} \bullet M_2 - m\right) - I_{IN} - \frac{M_1}{2} \bullet T \bullet R_I - M_2 \bullet T$$

In order to eliminate the possibility of subharmonic oscillations, the term which multiplies t_{ON} should be set equal to zero eliminating any dependency on duty cycle.

$$\frac{M_1}{2} \bullet R_I + R_I \bullet \frac{N_S}{N_P} \bullet M_2 = M$$

From the simplified schematic of the current sense circuit;

$$S = \frac{2}{10 \bullet \exp(-6)}$$

where S is defined as the slope of the oscillator ramp. Substituting the following values into the equation for R_P will allow us to determine the value of the slope compensation resistor.

$M_2 = 178571$

$N_S = 60$

$M_1 = 178571$

$N_P = 10$

$R_I = 0.01$

$S = 181818$

$$R_P = \frac{\frac{M_1}{2} \bullet R_I + \frac{N_S}{N_P} \bullet R_I \bullet M_2}{2}$$

$R_P = 0.064$

$R4 = 50k$

R3 is the slope compensation resistor and R4 is the internal 50kΩ resistor;

$$R_P = \frac{R3}{R3 + R4}$$

Solving for R3;

$$R3 = 0.064 \bullet \frac{R4}{1 - 0.064}$$

$R3 = 3.419k$

Therefore, the slope compensation resistor chosen must be greater than 3.42k in order for stable converter operation at duty cycles which exceed 50%.

Frequency response of the power regulation loop

The frequency response of the ballast is determined by analysis of the power regulation loop. Since it is really the output current that is being regulated and not the output voltage (any change in output voltage is attenuated by 1/120), the analysis can be simplified by modeling the power stage as a voltage controlled current source with some transconductance gain G_M. This assumption is valid for a loop cross over frequency below resonance of the power stage which is approximately 10kHz.

The transconductance gain, G_M, can be found as follows;

$$G_M = \frac{\Delta I_O}{\Delta V_E}$$

The output current is converted to a voltage by the output current sense resistor. The gain of the power stage is then;

$$G_P = R_{ls}\frac{\Delta I_O}{\Delta V_E}$$

or;

$$G_P = R_{ls}\, G_M$$

where; R_{ls} = the load sense resistance (0.75Ω)

ΔI_O = load current change (500mA)

ΔV_E = error amp voltage change (5V)

G_P = –22.5dB

The loop response must now be tailored for good power regulation (high DC gain) and adequate phase and gain margin at the loop crossover frequency. The gain of the LOAD SENSE amplifier is restricted due to the fact that gain of this stage effects the power curve characteristic as shown in above analysis of the power curve equation.

The LOADSENSE amplifier should be set up as an integrator so that it can filter out switching frequency noise from the control loop. The pole frequency was chosen to be at 1kHz to give good rejection of the switching frequency noise. This results in a capacitor value of 0.01µF. The low frequency gain of this amplifier is set to 7.5dB. The combination of this gain and the power stage gain results in –15dB of low frequency gain with a pole at 1kHz.

The response can now be tailored with the main error amplifier. A zero must be added in the amplifier response at some mid-band frequency so that the DC gain for the overall loop is as high as possible. The high frequency gain of this amplifier must be well below 0dB to ensure adequate gain and phase margin for the open loop gain. Since the 16kΩ, resistor has been determined from the power curve characteristic desired, only the feedback resistor value can be chosen. If this resistor is chosen so that the high frequency gain is to be less then –20dB for good gain margin, or the feedback resistor value of 1kΩ, the capacitor value can then be determined. If a zero frequency of 3.4kHz this assumed, this will give an adequate low frequency gain boost. From this, the value of the capacitor can now be determined to be 0.047µF. The gain and phase margin with these component values is greater than 20dB and 60 degrees, respectively.

CIRCUIT EXAMPLE:

A 9 to 16VDC input SEPIC converter powering a 35W OSRAM/SYLVANIA DC lamp was built and tested. Data on efficiency, power curve and various oscillagrams of current and voltages in the power/control circuit were taken and are discussed.

Magnetics Design

L1

The input inductor L1, is designed based on the same criteria as a boost inductor. Energy is stored in L1 during the on time of Q1 and transferred during the off time. L1 is designed to operate in the continuous mode with low current ripple. At 9 V_{IN} with 36W of output power and a converter efficiency of 85%, the average input current is 4.7 Amps. If a total peak-to-peak ripple current of 2 Amps is assumed the inductance of L1 can be found. But before we can calculate the inductance required, the minimum and maximum duty cycle must be found so that the maximum and minimum on time of Q1 can be determined. The SEPIC converter has a DC transfer function of;

$$V_O = V_{IN} \bullet n\frac{D}{1-D};$$

The turns ratio, n can be found from the maximum acceptable voltage stress on Q1. The stress on Q1 is the sum of the capacitor voltage plus the reflected secondary voltage. The capacitor voltage is essentially equal to V_{IN}, so;

$$V_{DS} = V_{IN} + \frac{V_O}{n};$$

The worst case output voltage on startup of the lamp is restricted to 500V, since this voltage will be reflected back to the drain of Q1. The turns ratio must be chosen so that the drain voltage never exceeds its maximum rating. A IRF1310 was chosen for this application in part because of its 45mΩ on resistance and V_{DS} = 100V. Calculating the turns ratio at V_{IN} = 16V; n is then found to be 5.8. A turns ratio of 6 is used.

The maximum duty cycle can now be determined from the DC transfer function. To find the maximum duty cycle, the worst case steady-state lamp voltage is used of 110VDC at V_{IN} = 9V. Lamp voltages between 60 and 110V will be within the power regulation range of the ballast. Lamp voltages outside of this range will be operated in the constant current mode. Therefore;

$D_{MAX} = 0.67$

The minimum duty cycle is determined using the minimum steady-state lamp voltage of 60VDC and $V_{IN} = 16V$.

$D_{MIN} = 0.38$

For a switching frequency of 100kHz, $t_{ON\ MAX}$ = 6.7µS, $t_{ON\ MIN}$ = 3.8µS

The inductance based on $t_{ON\ MAX}$ at $V_{IN\ MIN}$ can be calculated;

$$L1 = \frac{9 \bullet 6.7\mu S}{2} = 30\mu H.$$

L1 consists of 30T of 19AWG wound on a Micrometals E100 –18 core.

L2

The voltage across the primary winding of L2 when Q1 is on, is for all practical purposes, equal to the input voltage (neglecting voltage ripple on the capacitor) since the series capacitor is switched across the primary. The inductance of the primary winding is chosen based on the peak current desired (it is desired that the inductor current is continuous). The peak current chosen is based on a tradeoff between the voltage stress on Q1 and minimal number of turns to minimize the leakage inductance which in turn means reducing the number of layers of windings. If the peak current thru L2 is restricted to 3.0A, the primary inductance can then calculated as;

$$L2 = \frac{9 \bullet 6.7\mu S}{3} = 20\mu H.$$

The inductance of L1 and L2 could have been set equal to each other. This would have made both inductors "easy" to integrate on the same core. This was not attempted here because of leakage inductance concerns between the primary and secondary windings of L2.

The number of turns for L2 can now be determined based on the particular core geometry chosen. The area product (AP) required is found from;

$$AP = \frac{L \bullet I_P \bullet I_{RMS}}{K_F \bullet J \bullet B_M} = 0.362\ cm^2$$

This is based on the following parameters;

B = 0.1T	L = 20µH	I_P = 4.7A
J = 450A/cm	K = 0.4	I_{RMS} = 5.2A

An RM10PA250-3F3 core was used which has an AP of 0.379. The number of primary turns is then;

$$N_P = \frac{L \bullet I_P}{A_E \bullet B} = \frac{20\mu H \bullet 3A}{89 \bullet e\text{-}6 \bullet 0.1T} = 7T$$

(10T is used since this will easily fit in one layer with the desired core and wire gauge chosen)

This ferrite core must be gapped since it stores energy. It is desired that the total gap be placed in the center leg. The gap is calculated from;

$$L_P = \frac{u_O \bullet u_R \bullet N_P^2 \bullet A_E}{L} = 12.56 \bullet 10^{-7}$$

$$\frac{0.89 \bullet 100}{0.020mH} = 0.56mm = 0.02\ in$$

The secondary turns can be calculated from the turns ratio as 60T. The core used for L2 has a center leg gap of 0.022 in. Multifilar wire is used for both the primary and secondary turns to minimize the copper losses. The winding sequence used was; primary-secondary-primary-secondary-primary.

Performance data

Performance data on the ballast is presented in the following curves showing efficiency and the measured power curve. Oscillograms of Q1 voltage and current are also given as well as startup characteristics of the lamp voltage and current. The maximum efficiency achieved was 86.2% at a lamp voltage of 100V. The efficiency decrease after this point is due to an increase in output power which occurs at lamp voltages above 100 to 105V. The lamp cold start voltage and current waveforms are shown with a time base of 50mS and 1Sec. As can be seen, the ballast output voltage is 600V before lamp ignition. Once the lamp ignites, the voltage collapses and the lamp current increases to 2A. Eventually, the lamp voltage begins to increase and the current decreases. They will arrive to their steady-state values of 80 to 90VDC and 450mA respectively after approximately 150 seconds.

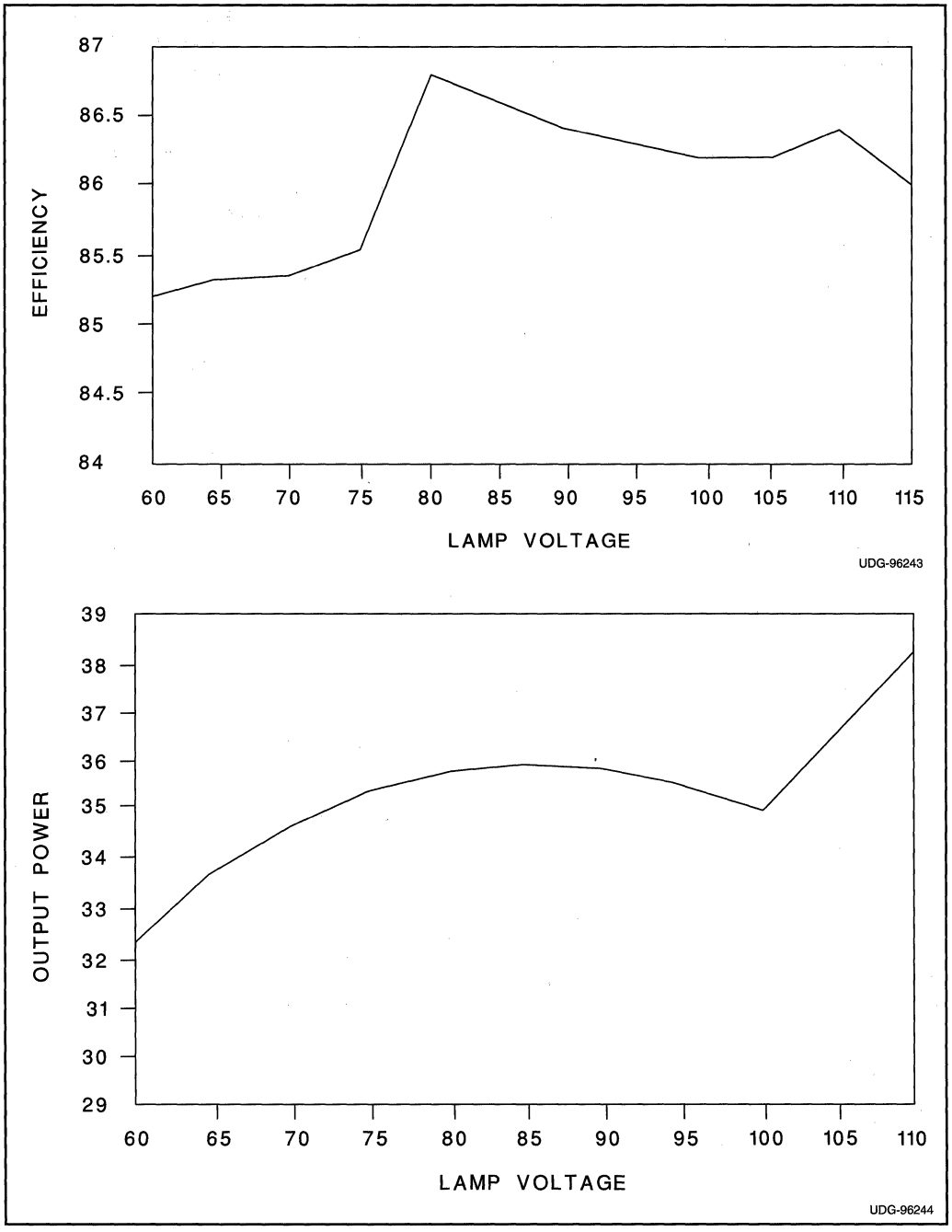


Figure 5. Efficiency and Power Curve of 35W HID Ballast

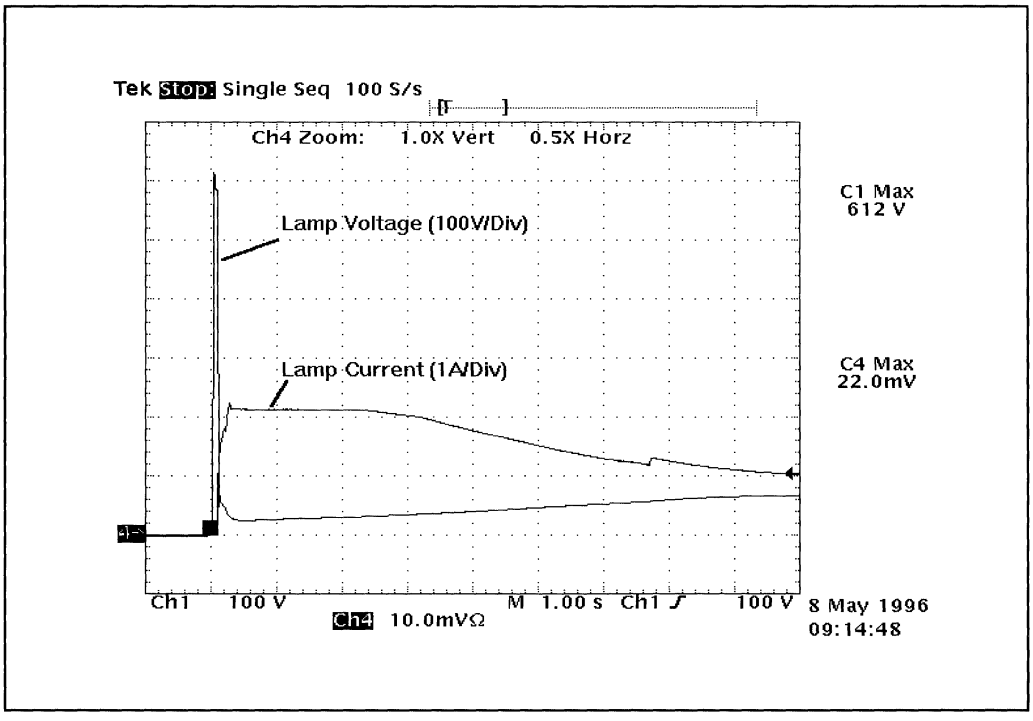


Figure 6. Ballast Output Voltage and Current

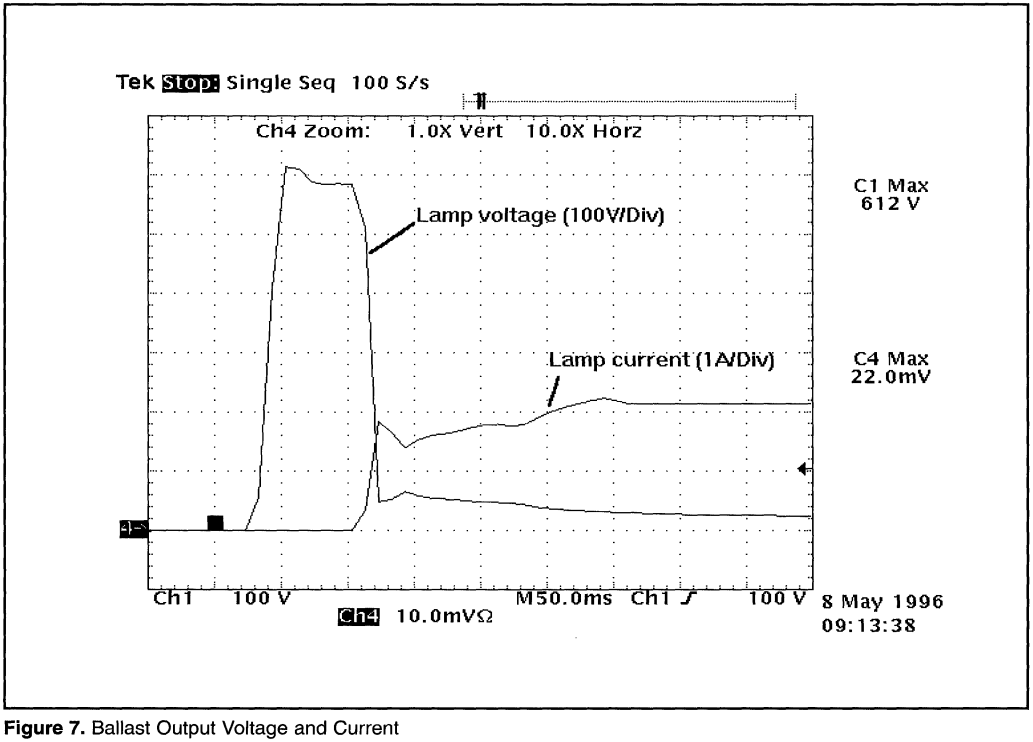


Figure 7. Ballast Output Voltage and Current

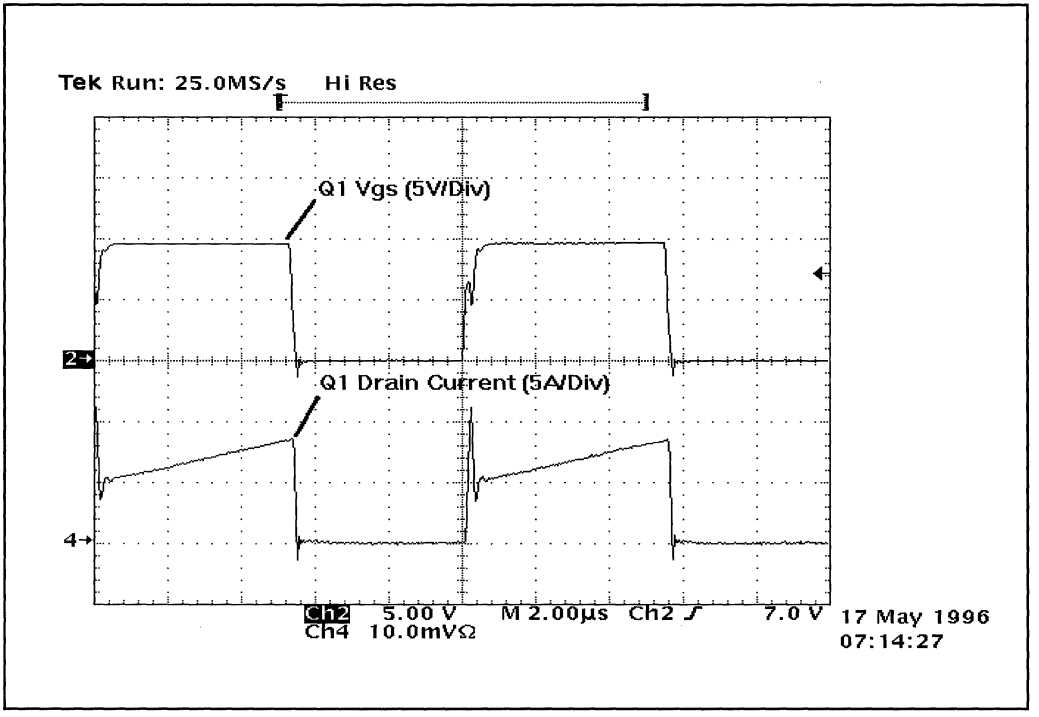


Figure 8. MOSFET (Q1) Gate and Drain Voltage at Steady State

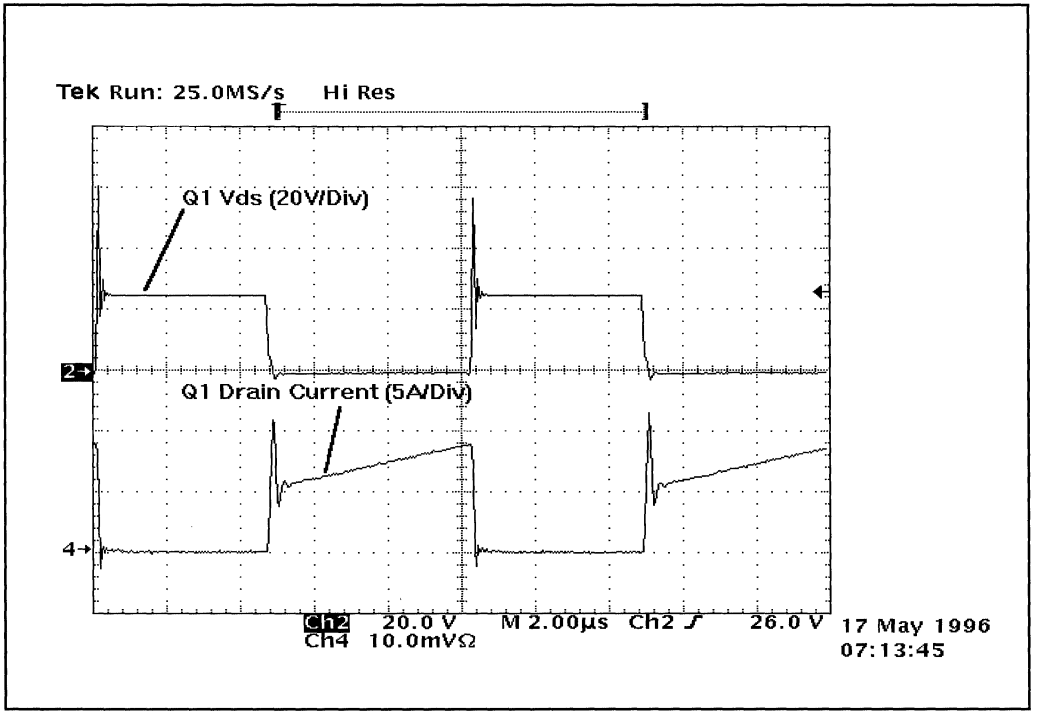


Figure 9. MOSFET (Q1) Drain Voltage and Current at Steady State

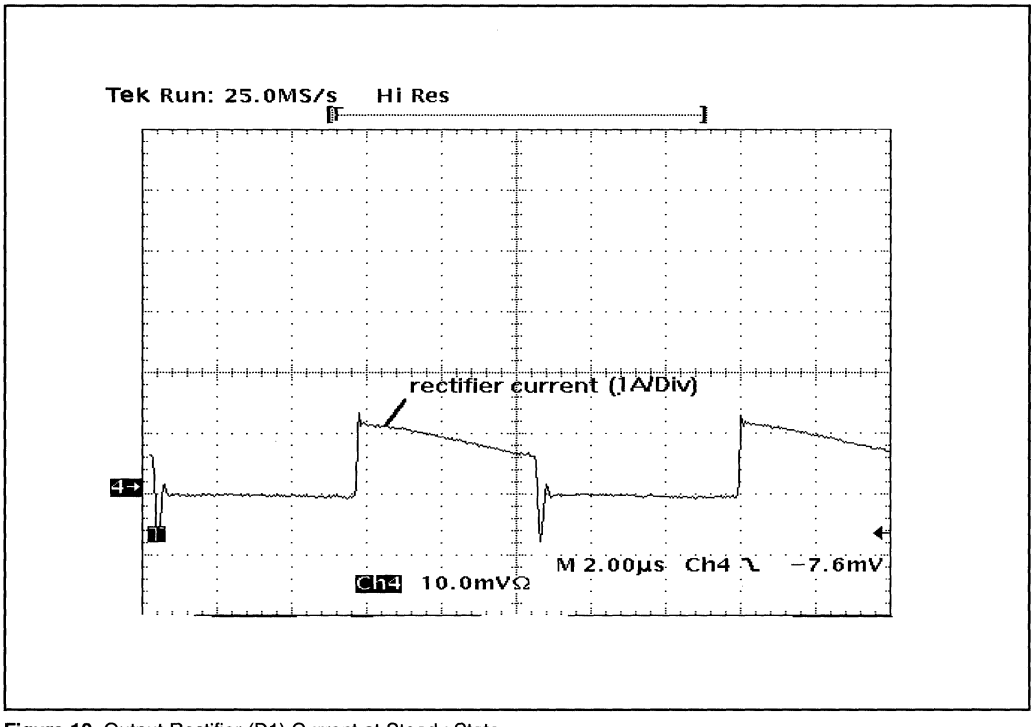


Figure 10. Output Rectifier (D1) Current at Steady State

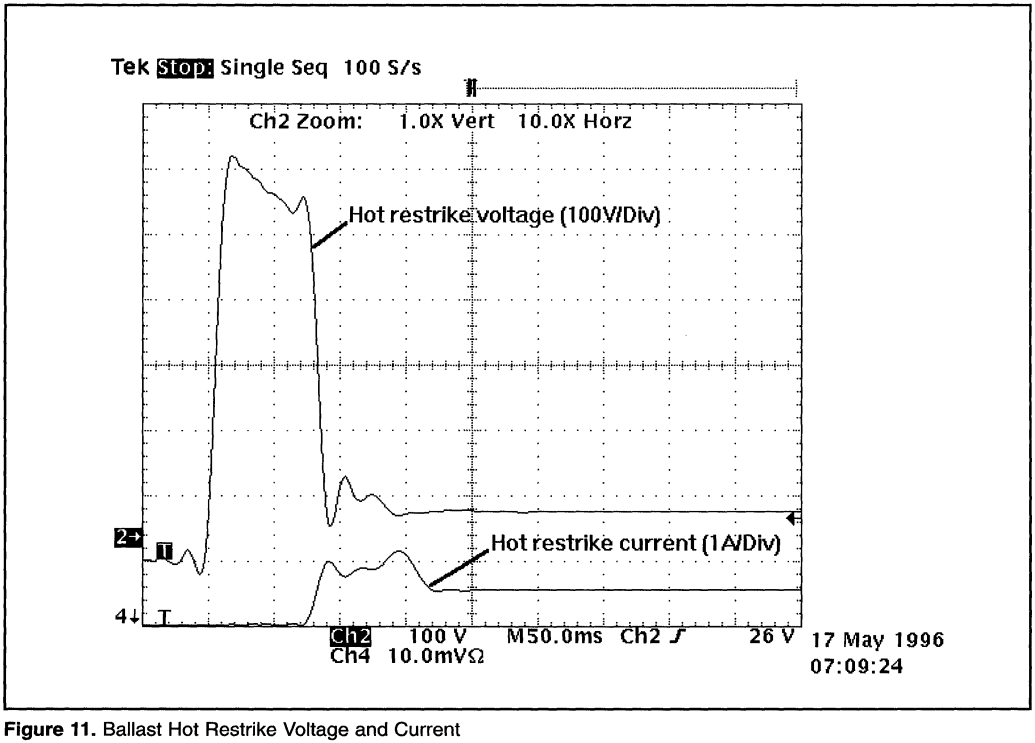


Figure 11. Ballast Hot Restrike Voltage and Current

35W HID BALLAST PARTS LIST

REF DES	PART DESCRIPTION	DIGIKEY NUMBER	QTYPER
RI	4.7Ω 1/4 W CC	10QBK-ND	1
R2	0.02Ω 1W		1
R3, R5	1k 1/4W CC	1KQBK-ND	2
R4	3.3k 1/4W CC	4KQBK-ND	1
R6	270k 1/4W CC	270KQBK-ND	1
R7	100k 1/4W CC	100KQBK-ND	1
R9	180Ω 1/2W CC	220HBK-ND	1
R11	5.1k 1/4W CC	5.1KQBK-ND	1
R12	12.5k 1/4W CC	15KQBK-ND	1
R13	16.1k 1/4W CC	16KQBK-ND	1
R14	1k 1/4W CC	1KQBK-ND	1
R15	150k 1/4W CC	150KQBK-ND	1
R16	250k 1/4W CC	250KQBK-ND	1
R17,R18	27k 1/4W CC	27KQBK-ND	2
R19,R25,R32,R8	10k 1/4W CC	10KQBK-ND	4
R20	0.75Ω 3W CC	VC3D.75-ND	1
R21	565k 1/4W CC	562KXBK-ND	1
R22,R23	282k 1/4W CC	280KXBK-ND	2
R24	560Ω 1/2W CC	560HBK-ND	1
R26,R27	100k 1/4W CC	100KQBK-ND	2
R30	18Ω 3W CC	VC3D18-ND	1
R31	330Ω 3W CC	VC3D330-ND	1
C33	10µF/100V POLY FILM	EF1106-ND	1
C1	1µF/50V METALLIZED FILM	P4675-ND	1
C2,C3,C26	470µF/50V ALUM ELEC	P1248-ND	3
C4	0.47µF/630V POLY FILM	EF4225-ND	1
C8,C11	0.47µF/50V CERAMIC	P4671-ND	2
C6,C7	4.7µF/250V ALUM ELEC	P6187-ND	2
C9	470pF/25V CERAMIC	P4808-ND	1
C10	10µF/35V ALUM ELEC	P1227-ND	1
C12,C13	1µF METALIZED FILM, NISSEI #R68105K63B		2
C14	150pF/50V CERAMIC	P4804-ND	1
C15	0.056µF/25V CERAMIC	P1240-ND	1
C16	47µF/25V ALUM ELEC	P1220-ND	1
C17,C18,C19	0.01µF/50V CERAMIC	P4513-ND	3
C5,C24	0.1µF/50V CERAMIC	P4525-ND	2
C25	1000pF/50V CERAMIC	P4812-ND	1
C30	100µF/25V ALUM ELEC	P1221-ND	1
C31	180pF/1kV CERAMIC DISK	P4119-ND	1
C32	1000pF/100V CERAMIC	P4036-ND	1
Z1	1N5235B, 6.8V ZENER	1N5235BCT-ND	1
Q2,Q3	2N3904, 40V, 0.200mA TRANISTOR		2
Q1	IRF1310, 100V, 0.027Ω	NEWARK#IRF1310	1
D1	MUR860, 600V, 8A FST REC	NEWARK#MUR860	1
HS2,3,4,5	THERMALLOY#7128D, HS FOR Q2,Q3,Q4	NEWARK#95F715	4
U1	UCC3305JP		1
HS1	THERMALLOY #6398-P2,HS FOR Q1		1
L1	E100-8 MICROMETALS		1
	CORE-30T #18AWG		
	35µH		
L2	RM10PA250-3F3 PHILIPS		
	10T PRIMARY LITZ(2X10X,1)		
	60T SECONDARY LITZ(1X15X,1)		
	WINDING SEQUENCE		
	(PRIM-10T, SEC-30T, PRIM-10T,SEC-30T, PRIM-10T)		

CONCLUSION

The performance data presented of a typical UCC3305 HID lamp controller application, demonstrated it to be a excellent means of controlling a 35W DC metal halide HID lamp. The power regulation and efficiency achieved using the SEPIC converter topology proved it to be a good alternative to other conventional circuit topologies for an automotive lighting application. The many protection and control features of the UCC3305 simplify the task of the ballast designer considerably, making it an economically feasable choice for AC as well as DC HID lamp applications.

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A Complete Control Solution For a Four-Quadrant Flyback Converter Using the New UCC3750 Source Ringer Controller

By Dhaval Dalal

Abstract

With the emergence of newer telecom distribution networks, there is a need for innovative power conversion solutions. Ring signal generation is a perennial requirement which can be addressed from a power conversion viewpoint with a switching amplifier or a dc-ac inverter. A unique flyback derived four-quadrant power inverter is discussed with a complete design procedure and control solution. While the emphasis is placed on the ring generator solution, it is clear that this approach is suitable for many other low power inverter applications such as UPS systems, audio amplifiers etc.

Introduction

The emergence of high bandwidth telecom architectures involving Fiber in the Loop (FITL) have created new challenges for powering the communication networks. One of the most demanding functions from the power management perspective is the generation of an appropriate ring signal for ringing telephones. While many of us have switched over to electronic phones, backward compatibility with the older mechanical bells is still necessary. A typical North American mechanical bell requires a ring signal of at least 45V (RMS) at a frequency of 20Hz (±1Hz) to provide an acceptable ringing tone. The ring frequencies in other international phone systems may be different (25Hz and 50Hz are other common frequencies), but the voltage level is quite similar. It is also important for the ring signal to have very low harmonic content in order to minimize interference in adjacent phone lines.

Historically, ring signal generation was done at the central office (CO) with long transmission paths requiring a high ring voltage (>80V) at the source. With the emergence of fiber networks to reduce distribution costs and increase bandwidth, ring generation and other powering functions have to be near the subscriber end. Typically, this is done at the remote switching modules (RSMs) located at the curb. Reduced transmission length implies that the ring signal amplitude can be lower (60V-70V) at the RSM, but the ring generator unit (RGU) now needs to support a higher Ringer Equivalent Number (REN) per line than the CO ring generator.

The traditional distributed power supply for telecom applications such as RSM has been a –48V battery backed voltage. For ring generation, this input voltage has to be converted into a ring signal of desired amplitude and frequency with a typical DC offset of –48V. In addition, the RGU has to provide the flexibility to control any of these parameters in addition to galvanic isolation. Many existing RGU designs use multiple conversion stages. As shown in Figure 1, the first stage is a DC-DC isolated conversion stage which creates two high voltage rails (positive and negative). These rails serve as the upper and lower bounds of the output signal. The second stage is either a linear amplifier as shown in Figure 1a (for lower power RGUs) or a full-bridge switching amplifier as shown in Figure 1b (for higher power).

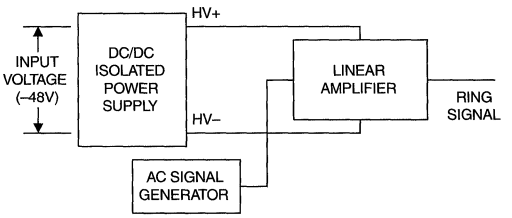


Figure 1a. Conventional Ring Generation Using Linear Amplifier

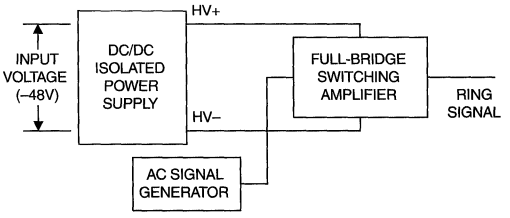


Figure 1b. Conventional Ring Generation Using Full-Bridge Amplifier

The second stage is modulated by an AC signal that has to be generated externally to provide a high voltage AC output. In some cases the modulating signal is a trapezoid (instead of the ideal sinusoid) for lower cost and complexity. The efficiency of these approaches suffers from dual stage power conversion as well as the inability to fully support the reactive phone loads encountered in some applications. A limitation of the linear approach is the lack of flexibility. The DC rail voltages set the bounds for the output ring signal and any change in DC offset or the AC amplitude requires redesign of both conversion stages. The linear amplifier also suffers from higher losses when the AC amplitude needs to be attenuated under AC current limit. While the full-bridge switching amplifier circumvents these problems, it adds significant cost and complexity.

Table I. Operating Mode Determination for Sinusoidal Signal

Mode	Output Current	Reference Polarity	Power Flow	E.A. Output	Source (PWM) Switch	Rectifier Switch
1	+	+	+	–	Q1	Q2
2	–	+	–	+	Q3	(D1)
3	–	–	+	+	Q1	Q3
4	+	–	–	–	Q2	(D1)

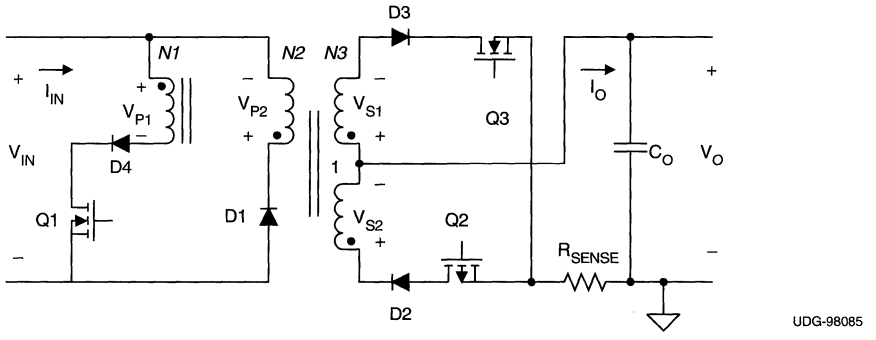


Figure 2. Four-quadrant Flyback Converter Topology

The Four-Quadrant Flyback Topology

The four-quadrant flyback topology is a unique power stage approach which simplifies the RGU implementation considerably, while providing a high degree of design versatility. This approach (Figure 2) provides a single stage solution for ring generation with isolation and the ability to return the reactive power to the source as needed.

The operating modes of the converter are summarized in Table 1 and relevant waveforms are provided in Figures 3 and 4. Figure 3 is drawn for a purely capacitive load in order to provide a clear depiction of all four operating modes (quadrants). In most applications, the load will have a resistive component to it and the circuit will operate primarily in quadrants 1 and 3. The waveforms in Figure 3 (output voltage and current) are the low frequency sinusoidal signals. Within each mode, there are number of switching cycles which follow the waveforms shown in Figure 4. The switching cycle consists of PWM and rectification intervals. During the PWM interval, one of the switches (Q1-Q3) is turned on. The selection of which switch to PWM is made based on Table 1. In modes 1 and 3, the rectification interval (rising edge of the clock signal) is accompanied by turning on of appropriate switch (Q2 or Q3). The operation of the power supply is as a flyback converter in discontinuous conduction mode (DCM) in all four quadrants. The output impedance of the converter including its output capacitor and the load determines the operating modes.

In modes 1 and 3, input to output power transfer takes place. The operation is very similar to conventional flyback operation where the primary switch (Q1) is pulsewidth modulated to build energy in the flyback winding. For the rest of the switching cycle, the stored energy is fed to the output through the rectifying diode and switch combi-

nation. In mode 1, the output (voltage and current) polarity is positive and Q2/D2 provide the rectifying path. In mode 3, the output polarity is negative and the rectifying path is through Q3/D3. Also, the negative polarity in mode 3 requires a phase reversal in the feedback path.

In modes 2 and 4, the secondary switches (Q3 and Q2 respectively) are modulated to enable energy transfer in reverse direction. As a result, the reactive power finds its way back to the input. In both modes, D1 provides the rectifying path to the input. The operation of the converter is still in flyback mode, but the secondary side functions as the input. However, the controlled variable is still the output voltage. As a result, the duty cycle to output relationship in these modes is given by:

$$\frac{|V_O|}{|I_O|} = \frac{2 \bullet L_{sec}}{D^2 \bullet T_S} \quad (1)$$

where $|Vo|$ and $|Io|$ are the magnitudes of slowly varying sinusoidal output voltage and current respectively and can be assumed to be constant for a switching cycle.

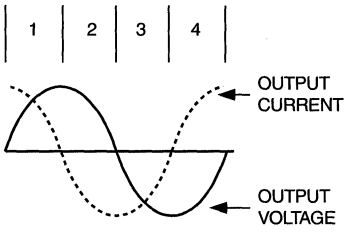


Figure 3. Operating Modes (Ring Frequency)

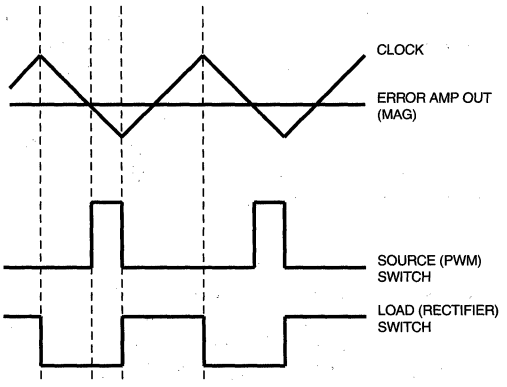


Figure 4. Circuit Waveforms (Switching Frequency)

Power Stage Design Procedure

Following specifications are required for design of the four-quadrant flyback converter. The target specifications for the reference design are also provided.

1. Input voltage range: [$V_{in(min)}$ – $V_{in(max)}$] [40V-60V].
2. Full load output voltage (RMS): V_{rms} [85V]
3. Output offset voltage: V_{os} [0V]
4. Maximum output current / Min. load impedance. [125 mA/10REN]
5. Short circuit current – Isc [200 mA]
6. Output frequency: f_{ring} [20 Hz]
7. Switching frequency: f_{sw} [130 kHz]

The voltages across the switching elements for different modes can be derived (with reference to Figure 2) using the following relationships. Voltage polarities are drain-to-source for FETs and cathode to anode for diodes. In case of diode-FET combinations, the FET polarity is used across the combination. Also, it should be noted that Q2 is assumed to be a p-channel FET. As shown in Figure 2, the turns ratios N1, N2 and N3 are all derived with respect to the secondary winding in series with Q2/D2. The polarities and the variable designations are as depicted in Figure 2.

$$\frac{V_{p1}}{N_1} = \frac{V_{p2}}{N_2} = \frac{V_{s1}}{N_3} = V_{s2} \quad (2)$$

$$V(Q1/D4) = V_{in} - V_{p1} \quad (3)$$

$$V(D1) = V_{in} + V_{p2} \quad (4)$$

$$V(Q2/D2) = V_o - V_{s2} \quad (5)$$

$$V(Q3/D3) = V_o - V_{s1} \quad (6)$$

Values of these voltages are summarized in Table 2 for all modes of operation. Sub-modes A and B within each mode represent the PWM and rectification intervals of a switching cycle respectively. It must also be recognized that within each switching cycle, there is an idle mode when neither PWM nor rectification is taking place. The values in Table 2 are used to select switching elements and the turns ratios of the converter. The table also underlines the need for a diode-FET combination as used in the secondary (to prevent the anti-parallel diode of the FET from conducting

when the voltage across it is negative). As shown later, if correct turns ratios are selected, the primary diode (D4) in series with Q1 can be eliminated.

Table II. Voltage Stresses Across Switching Elements

Mode	Polarities			Active	Transformer Voltages			Component Voltage Stresses			
	I_{in}	V_o	I_o	Switch	V_{p1}	V_{p2}	V_{s2}	*Q1*	*D1*	*Q2/D2*	*Q3/D3*
1A	+	+	0	*Q1*	V_{in}	$\frac{V_{in} \bullet N_2}{N_1}$	$\frac{V_{in}}{N_1}$	0	$\left(1+\frac{N_2}{N_1}\right)V_{in}$	$V_o+\left(\frac{V_{in}}{N_1}\right)$	$V_o-\left(\frac{N_3 V_{in}}{N_1}\right)$
1B	0	+	+	*Q2/D2*	$-N_1 V_o$	$-N_2 V_o$	$-V_o$	$V_{in}+N_1 V_o$	$V_{in}-N_2 V_o$	0	$(1+N_3)\bullet V_o$
2A	0	+	–	*Q3/D3*	$\frac{N_1 V_o}{N_3}$	$\frac{N_2 V_o}{N_3}$	$\frac{V_o}{N_3}$	$V_{in}-\left(\frac{N_1 V_o}{N_3}\right)$	$V_{in}+\left(\frac{N_2 V_o}{N_3}\right)$	$V_o+\left(\frac{V_o}{N_3}\right)$	0
2B	–	+	0	*D1*	$\frac{-N_1 V_{in}}{N_2}$	$-V_{in}$	$-\frac{V_{in}}{N_2}$	$\left(1+\frac{N_1}{N_2}\right)V_{in}$	0	$V_o+\left(\frac{V_{in}}{N_2}\right)$	$V_o+\left(\frac{N_3 V_{in}}{N_2}\right)$
3A	+	–	0	*Q1*	V_{in}	$\frac{V_{in} \bullet N_2}{N_1}$	$\frac{V_{in}}{N_1}$	0	$\left(1+\frac{N_2}{N_1}\right)V_{in}$	$V_o+\left(\frac{V_{in}}{N_1}\right)$	$V_o-\left(\frac{N_3 V_{in}}{N_1}\right)$
3B	0	–	–	*Q3/D3*	$\frac{N_1 V_o}{N_3}$	$\frac{N_2 V_o}{N_3}$	$\frac{V_o}{N_3}$	$V_{in}-\left(\frac{N_1 V_o}{N_3}\right)$	$V_{in}+\left(\frac{N_2 V_o}{N_3}\right)$	$V_o+\left(\frac{V_o}{N_3}\right)$	0
4A	0	–	+	*Q2/D2*	$-N_1 V_o$	$-N_2 V_o$	$-V_o$	$V_{in}+N_1 V_o$	$V_{in}-N_2 V_o$	0	$(1+N_3)\bullet V_o$
4B	–	–	0	D1	$\frac{-N_1 V_{in}}{N_2}$	$-V_{in}$	$-\frac{V_{in}}{N_2}$	$\left(1+\frac{N_1}{N_2}\right)V_{in}$	0	$V_o-\left(\frac{V_{in}}{N_2}\right)$	$V_o+\left(\frac{N_3 V_{in}}{N_2}\right)$

Step 1. Peak Output Voltage

Determine the peak positive and negative output voltages, Vo(pk+) and Vo(pk–)

$$V_o(pk+) = 1.414 \bullet V_{rms} + V_{os} \qquad (7a)$$

and

$$V_o(pk-) = 1.414 \bullet V_{rms} - V_{os} \qquad (7b)$$

For the reference design, since

$$V_{os} = 0V, V_o(pk+) = V_o(pk-) = 120V.$$

For many designs requiring a –48V offset, the V_o(pk+) value will be lower than the V_o(pk–) value.

Step 2. Turns ratios (N_1, N_2 and N_3)

The additional clamp winding for reverse power transfer can potentially block the normal power transfer to the output if the correct turns ratio is not used. From Table 2, it can be seen that in order to prevent D1 from conducting in modes 1B and 3B, following conditions must be satisfied:

$$V_{in} - N_2 V_o > 0 \text{ (when } V_o \text{ is positive)} \qquad (8a)$$

and

$$V_{in} + \frac{N_2 V_o}{N_3} > 0 \text{ (when } V_o \text{ is negative)} \qquad (8b)$$

Thus,

$$N_2 < \frac{V_{in}(\min)}{V_o(pk+)} \qquad (8c)$$

and

$$\frac{N_2}{N_3} < \frac{V_{in}(\min)}{V_o(pk-)} \qquad (8d)$$

N_2 should be selected to be the highest possible value to meet the above constraints. To optimize the turns ratios, N_3 may be selected such that:

$$N_3 = \frac{V_o(pk-)}{V_o(pk+)}. \qquad (9)$$

Lower values of N_2 will increase the stress on the secondary switches (Q2,Q3). On the other hand, a high value of N_2 contributes to higher stress on D1.

The value of N_1 determines if the voltage across Q1/D4 ever goes negative in modes 2A and 4A. If D4 is used, there is no theoretical upper bound on N_1 as the automatic conduction of Q1's body diode is prevented. If, however, we limit N_1 according to the following relationship we can prevent the voltage from going negative and eliminate D4:

$$N_1 < \frac{V_{in}(\min)}{V_o(pk-)} \qquad (9a)$$

and

$$N_1 < N_3 \frac{V_{in}(\min)}{V_o(pk+)} \quad (9b)$$

If the value of N_3 is selected using the guideline above, the condition for N_1 becomes:

$$N_1 < \frac{V_{in}(\min)}{V_o(pk-)} \quad (10)$$

for N_3>1(i.e. negative bias voltages).

A high value of N_1 increases the voltage stress on Q1 while a low value of N_1 increases the voltage stress on D1-D3.

For the reference design, since $V_o(pk-) = V_o(pk+)$, $N_1 = N_2 < 0.33$ (chosen to be 0.2 for some margin) and $N_3 = 1$

Step 3. Load Considerations

The load for the ring generator is normally reactive. Each mechanical ringer can be represented by a 6930Ω resistor in series with a 8μF capacitor (this specification is typical for the North American phone systems, other phone systems have different definitions of Ringer Equivalence). This load is considered as 1 REN (Ringer Equivalent Number). A load of n REN is equivalent to a 6930/nΩ resistor in series with an 8·nμF capacitor. Also, in contrast to the conventional DC-DC power supply, the output filter capacitor is considered as part of the load for the low frequency analysis. The resulting effective load for the ring generator is as shown in Figure 5. The admittance of this load can be represented as Y (= $|Y|\angle\theta$), as defined in equations 11-15:

$$\theta = \tan^{-1}\left(\frac{C_o \bullet k^2 + C_o + C_l}{k \bullet C_l}\right) \quad (13)$$

$$k = \omega \bullet R_l \bullet C_l \quad (14)$$

$$\omega = 2\pi \bullet f_{ring} \quad (15)$$

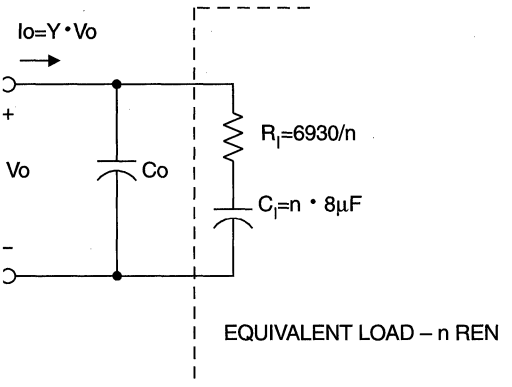


Figure 5. Equivalent Load of n Phones as Seen by the 4-Quadrant Ring Generator

The output voltage, current and power are represented by equations 16, 17 and 18.

$$V_o(t) = V_{os} + \sqrt{2} \bullet V_{rms} \bullet \cos(\omega t) \quad (16)$$

$$I_o(t) = \sqrt{2} \bullet V_{rms} \bullet |Y| \bullet \cos(\omega t + \theta) \quad (17)$$

From the power equation, it can be seen that the average power delivered to the load is given by:

$$P_o(avg) = {V_{rms}}^2 \bullet |Y| \bullet \cos\theta \quad (19)$$

However, the flyback converter components should be chosen to handle the peak power delivered. The flyback transformer energy storage is at the switching frequency and it should be designed to process the peak (not the average) power demanded by the slowly changing output. It can be shown that (for negative values of Vos) the positive peak value of $P_o(t)$ occurs when $2\omega t + \theta = 2\pi$. The resultant peak power is given by: (20)

Table 3 shows the values of Rl, Cl, $|Y|$, θ and Po(pk) for different load conditions and values of Vos and Co. These values are calculated for a ring frequency of 20 Hz and an output RMS voltage of 90V. As can be seen from the table, at higher

$$Y = \frac{\omega}{1+k^2} \bullet \left[k \bullet C_l + j\left(C_O \bullet k^2 + C_O + C_l\right)\right] \quad (11)$$

$$|Y| = \frac{\omega}{1+k^2} \bullet \sqrt{(k \bullet C_l)^2 + \left(C_O \bullet k^2 + C_O + C_l\right)^2} \quad (12)$$

$$P_O(t) = V_O(t) \bullet I_O(t) = {V_{rms}}^2 \bullet |Y| \bullet [\cos\theta + \cos(2\omega t + \theta)] + \sqrt{2} \bullet V_{rms} \bullet V_{OS} \bullet |Y| \bullet \cos(\omega t + \theta) \quad (18)$$

Table III. Output Average and Peak Power Levels for Different Load Conditions

REN	Vos (V)	Co (μF)	Rl (Ω)	Cl (μF)	|Y| (S)	θ (deg)	Po(avg) (W)	+Po(pk) (W)	–Po(pk) (W)
0	0	1	-	0	1.257e-4	90	0	1.016	–1.016
0	–48	1	-	0	1.257e-4	90	0	1.59	–1.59
0	–48	2.2	-	0	2.765e-4	90	0	3.50	–3.50
1	0	1	6930	8	2.032e-4	45.91	1.145	2.789	–0.499
1	–48	1	6930	8	2.032e-4	45.91	1.145	3.947	–1.077
1	–48	2.2	6930	8	3.287e-4	64.52	1.145	5.550	–2.710
5	0	1	1386	40	7.425e-4	17.81	5.726	11.73	–0.278
5	–48	1	1386	40	7.425e-4	17.81	5.726	16.23	–1.387
5	–48	2.2	1386	40	8.016e-4	28.13	5.726	16.98	–2.372
10	0	1	693	80	1.452e-3	13.08	11.45	23.21	–0.300
10	–48	1	693	80	1.452e-3	13.08	11.45	32.03	–2.122
10	–48	2.2	693	80	1.493e-3	18.73	11.45	32.56	-2.930

REN levels, the load appears highly resistive and the operation in the reverse power transfer modes is minimized. This is also illustrated by plots in Figure 6, which depict instantaneous output power for various operating conditions.

In addition to computing the peak power as described above, the ring generator circuit must also be designed to handle the "off-hook" condition of the phone. Under an off-hook condition the ring generator must support a much higher load current since the off-hook resistance of a single phone is 200Ω. For each design, an estimate must be made of the number of phones going off-hook simultaneously. Once the off-hook condition is detected, an external relay circuit will disconnect the ringer from the corresponding phone lines. However, the ringer circuit is required to maintain the bias voltage(VB) under off-hook conditions for at least 200ms to allow for relay switching to the talk battery voltage.

Step 4. Switching Device Selection

From Table 2, the worst case voltage stresses on individual devices [and the calculated values for the example circuit] are:

$$Q1: \left(1+\frac{N_1}{N_2}\right) \bullet V_{in}(\max)\ [120\ V] \tag{21}$$

$$D1: \left(1+\frac{N_2}{N_1}\right) \bullet V_{in}(\max)\ [120\ V] \tag{22}$$

$$Q2: -V_o(pk-) - \frac{V_{in}(\max)}{N_2}\ [-420V] \tag{23}$$

$$D2: V_o(pk+) + \frac{V_{in}(\max)}{N_1}\ [420V] \tag{24}$$

$$Q3: V_o(pk+) + N_3 \bullet \left(\frac{V_{in}(\max)}{N_2}\right)\ [420V] \tag{25}$$

$$D3: |V_o|(pk-) + N_3 \bullet \left(\frac{V_{in}(\max)}{N_1}\right)\ [420V] \tag{26}$$

Select the switching devices and rectifiers to handle the above stresses in addition to the leakage spikes associated with the flyback transformers.

The current ratings of these devices are selected by first calculating the peak current levels and then translating them into the RMS currents. The forward power transfer typically has a higher current requirement when compared to the reverse power transfer. The peak current value is given by:

$$Ipk(t) = \frac{V_{in} \bullet d(t) \bullet T_s}{L_p} \tag{27}$$

where Ipk(t) is the peak current level for duty cycle d(t). T_S is the switching period. The duty cycle d(t)

$$P_o(pk) = V_{rms}{}^2 \bullet |Y| \bullet (1+\cos\theta) - \sqrt{2} \bullet V_{rms} \bullet V_{OS} \bullet |Y| \bullet \cos\left(\frac{\theta}{2}\right)$$

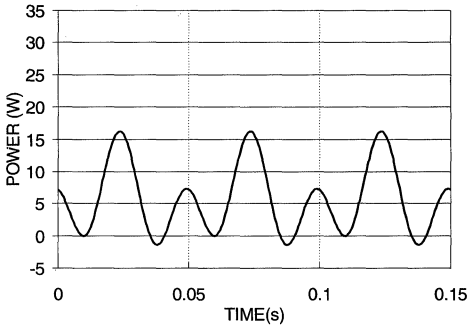


Figure 6a. Instantaneous output power for ring generator (5 REN, Vos = –48V)

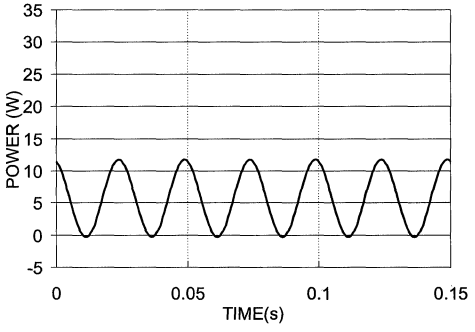


Figure 6b. Instantaneous Output Power for Ring Generator (5 REN, Vos = 0V)

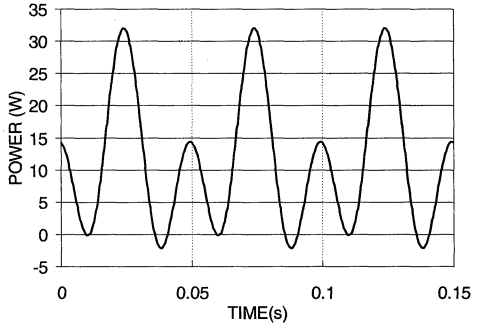


Figure 6c. Instantaneous Output Power for Ring Generator (10 REN, Vos = –48V)

varies proportionally to output voltage $V_o(t)$ and is given by:

$$d(t) = \frac{|V_o(t)|}{V_{in} \bullet k1} \tag{28}$$

where k1 is defined as:

$$k1 = \sqrt{\frac{T_s}{2 \bullet L_p \bullet |Y|}} \tag{29}$$

The RMS primary switch current can be determined by first taking the RMS value of the Ipk(t) current over a switching cycle and then computing the RMS value of the resultant quantity over the ring frequency cycle. A Mathcad program can be used for this exercise and results in a primary RMS current of 1.15A and a secondary RMS current of 0.38 A for the reference design. For the off-hook condition these currents are calculated to be 1A and 0.6A respectively. The peak currents for the primary and secondary switches are calculated in the same manner and result in values of 5.5A and 1.8A respectively.

Step 5. Transformer Design

While the transformer design is very similar to the DCM flyback design, it is important to take into consideration the peak instantaneous output power and not the average power drawn by the output. After selecting the turns ratios, calculate the maximum magnetizing inductance of the main primary winding using:

$$L_p \le \left(\frac{N_1}{N_3}\right)^2 \bullet \frac{R_o \bullet T_s}{8} \tag{30}$$

The rest of the transformer design is straightforward using the conventional (sometimes iterative) design steps of core selection, number of turns in primary and secondary, gapping, wire size selection etc.

In modes 2 and 4, the power transfer is from output to input with secondary side switches being modulated. The duty cycle to output relationship in these modes for DCM operation is given by :

$$\frac{|V_o|}{|I_o|} = \frac{2 \bullet L_{sec}}{D^2 \bullet T_s} \tag{31}$$

where $|V_o|$ and $|I_o|$ are the magnitudes of slowly varying sinusoidal output voltage and current respectively and can be assumed to be constant for a switching cycle. With a highly reactive load, the converter operates in modes 2 and 4 for substan-

tial periods of time. Under these circumstances, if the ratio $|V_o|/|I_o|$ falls below the level given by the above equation, the duty cycle limit is reached and the circuit is unable to transfer power at a rate required by the load, resulting in some distortion of the output waveform. One way to alleviate this behavior is to reduce the magnetizing inductance in the secondary. By selecting the turns ratios to correspond to the DC offset as described in step 2, the output voltage distortion is minimized.

Control Circuit Considerations

The control circuit required for the four quadrant flyback converter has to support all four modes of operation and has to be able to handle transitions from one mode to the other smoothly. While a discrete implementation is possible, the complexity of such an approach can be overwhelming due to precision timing requirements and multiple functionalities required. The converter implementation can be greatly simplified by using Unitrode's source ringer controller IC, the UCC3750.

Figure 7 shows the block diagram of the UCC3750. The UCC3750 provides complete control and drive solution for the four-quadrant flyback topology. It provides controls for switches Q1-Q3 with intelligent logic circuits to detect appropriate mode of operation and direct the PWM and rectification signals to appropriate switch. It also contains a crystal derived low frequency sine wave reference which can be programmed to 3 different frequencies with a single crystal. The sine-wave reference has versatility to accept external clocks instead of crystal and also to accept an externally generated sine wave. The IC operates from a single 5V bias supply and has the capability to generate a higher charge-pump voltage (VCP) to drive the MOSFETs. It contains internal 3V and 7.5V references, a summing amplifier (AMP1), an error amplifier (AMP2), programmable AC and DC current limits and a triangular clock oscillator. More details about the UCC3750 operation are available in the device datasheet which also contains pin descriptions and a detailed application section.

UCC3750 Interface Signals

The UCC3750 provides a number of interface signals which allow easy incorporation of the ring generator into a phone distribution system. One of the output interface signals is the RGOOD signal which can be used to determine if the ring generator is providing a sinusoidal signal or not. This output goes low if the error amplifier saturates, indicating that the output is not able to track the reference signal.

The other key output signal is the SWRLY signal. This signal provides a pulse output that precedes the zero crossing of the sine-wave output by a fixed interval (5-8 ms). There are many uses of

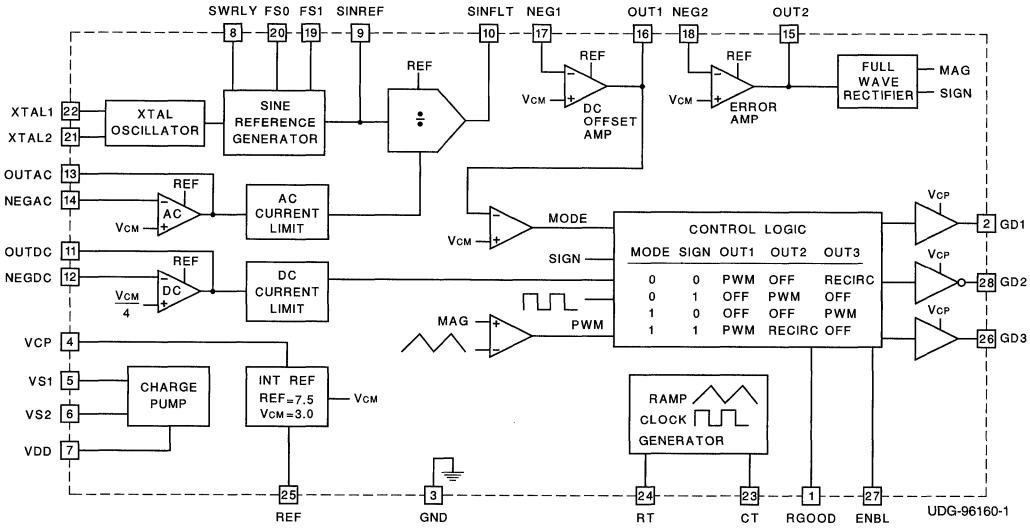


Figure 7. Block Diagram of the UCC3750

such a signal. One is to use it as a gating signal for external relay activation. When the phone goes off-hook and the need arises to switch that line from the ring generator to the talk battery, it is best done at the point when the two voltages are equal to prevent arcing. This point happens to be the zero crossing of the sine wave reference. The SWRLY signal precedes the zero crossing to allow for the activation of the relay. For different output frequencies, the pulsewidth and the lead-time of the SWRLY are given in Table 4. The timings given in Table 4 are accurate for a 32 kHz crystal and for the zero crossing of the SINREF output. Due to the filtering of the SINREF before being applied to the error amplifier and the feedback loop delays, the actual output voltage may crossover at a different point than the SINREF signal. However, these delays are much smaller compared to the designed delay times (in ms) to have an appreciable impact on the circuit operation. Another use of the SWRLY signal is for generating handshake signal such as SYNC signals or Message Waiting signals. The SWRLY signal provides an accurate, low frequency timing base that can be used to derive system specific handshake signals. These signals can also be brought back to control the UCC3750 to meet specific output signal shaping requirements.

Table IV. SWRLY Pulsewidth and Lead Time

Frequency (Hz)	SWRLY Lead Time (ms)	SWRLY Pulsewidth (ms)
20	7.8125	1.5625
25	6.25	1.25
50	5.625	0.625

Finally, if the UCC3750 is used for single line ringing applications, its output can be cadenced on and off by using the ENABLE pin to input the cadencing signal. Any external power management signals requiring sequencing and/or shutdown can also be channeled into the ENABLE pin with appropriate buffering.

Summing and Error Amplifier Configuration

In order to program the output voltage for the ring generator, the summing amplifier and the error amplifier of the UCC3750 need to be configured for required DC gain. (See Fig 8.) Depending on the output voltage requirements and the system configuration selection, there are three approaches available for programming the error amplifier components. Typically, the ring generator output voltage is some combination of a DC offset voltage and a sinusoid which is amplified from the sine-wave reference signal (V_{AC}) generated by the UCC3750.

Approach A. No DC Offset (VB=0) [V_O = k2 • V_{AC}]. In this approach, the required output voltage is a sinusoidal signal with no DC offset. As indicated, only a gain from the sinusoidal reference (V_{AC}) needs to be programmed. This approach is used when the ring generator output is cascaded with a DC voltage that is already available.

Approach B. Programmable DC offset (αVB) [V_O= k1•VB + k2•V_{AC}]. The UCC3750's capability to make the ring generator output voltage completely programmable is fully exploited with this approach. By providing 2 separate gains for the AC and DC programming signals through the error amplifier, the DC offset and AC amplitude can be independently set at the desired levels with the added flexibility of changing the offset voltage by changing an input voltage level (VB).

Approach C. Fixed DC Offset [VB =0, V_O = V_{OS} + k2•V_{AC}]. The requirement for a DC offset voltage is predetermined and fixed in some applica-

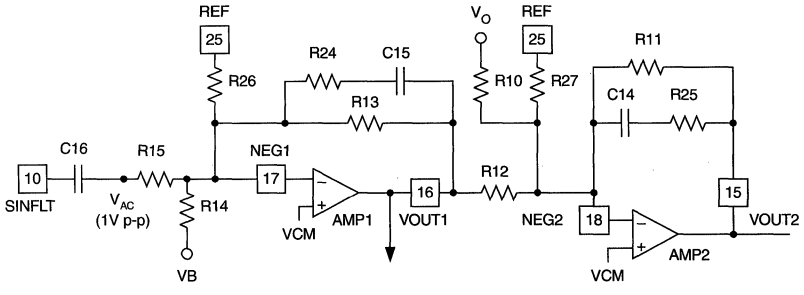


Figure 8. Summing Amplifier and Error Amplifier Configuration

tions. In this case, the requirement of a programming voltage (VB) for setting the offset voltage can be done away with and the resistor values can be selected to provide a fixed DC offset (V_{OS}).

A step-by-step procedure for selecting the error amplifier components for all the 3 approaches is provided below. Except for step 2, all other steps are common to all the 3 approaches. For step 2, the distinct procedures for approaches A-C are listed as steps 2A-2C. Equations 32-36 give formulas for the amplifier setup.

For $R_{26} = 1.5 \bullet R_{14}$; (32) can be simplified to:

$$V_{out1} = V_{CM} - \frac{R_{13}}{R_{14}} \bullet VB - \frac{R_{13}}{R_{15}} \bullet V_{AC} \quad (33)$$

For $R_{27} = 1.5 \bullet R_{10}$, (34) can be simplified to:

$$V_O = \frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{14}} \bullet VB + \frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{15}} \bullet V_{AC} \quad (35)$$

For $VB = V_{OS}$:

$$R_{10} \bullet R_{13} = R_{12} \bullet R_{14} \quad (36)$$

Step 1. Select R_{15} and C_{16}. As indicated in equation (35), the AC gain from SINFLT to V_O is inversely proportional to R_{15}. Thus, R_{15} should be chosen to be as low as possible. However, R_{15} and C_{16} form a high pass (DC blocking) filter with very low frequency cut-off in order to allow the ring frequency through. As a result, a low value of R_{15} will necessitate a high value of C_{16}. Based on component availability and output requirements, the resolution of this trade-off (low R vs. low C) will vary. In order to get a 5Hz cut-off a 15k resistor and a 2.2µF are chosen.

Step 2. The next step is to select R_{13} and R_{14} so that maximum amplification is attained from the first amplifier without saturating it. The amplifier output range is from 0.7V to 5.3V, V_{CM} = 3V and V_{AC} = 0.5V.

2A. For V_{OS}=0, select R_{13} such that the ratio of R_{13} to R_{15} is at or below 4.5. This constraint follows from equation (33) and assumes that R_{26}=1.5 • R_{14}. In this case, particular values of R_{14} and R_{26} are not very critical as they only provide a DC bias for the first amplifier. They should be chosen to achieve moderate bias levels. For the present example, R_{13} is selected to be 60k.

2B. For a programmable DC offset in the range of –48V, having VB equal to the desired offset voltage (k1=1) leads to difficult trade-offs in component value selections. For example, from equations (35) and (36), the AC gain from the sine wave reference to the output is given by (R_{14}/R_{15}). With R_{15} already chosen using the trade-off in step 1, the value of R_{14} can become very large for systems with high output voltage requirements. As a result, the ratio of R_{10} to R_{12} also becomes large, leading to a small value of R_{12} or a large value of R_{10}, both options result in non-optimal performance. Alternatively, a resistive divider can be used to scale down the offset voltage before applying it to VB. For example, a 1:10 scaling would result in VB=–4.8V for V_{OS} = –48V. The ratio: $k1 = \left[\frac{(R_{10} \bullet R_{13})}{(R_{12} \bullet R_{14})}\right] = 10$ in this case. With this arrangement, R_{13} and R_{14} can be more optimally chosen. Using equation (35) and required AC gain (k2), the value of (R_{10}.R_{13}/R_{12}) can be determined. Substituting this value for k1, the value of R_{14} is derived. R_{13} should be selected so that the output of the first amplifier provides maximum swing without saturating for all possible values of VB. The value of R_{26} equals 1.5•R_{14}.

For example, for an 85V AC output, Vo–pk =120 V, k2 = 120/0.5 = 240. With R_{15}=15k, (R_{10}•R_{13}/R_{12}) = k2·R_{15} = 3.6M. For k1=10, R_{14} becomes 360k. Putting these values into equation (33) and solving for R_{13} with V_{out1}=5.3V, V_{AC} = –0.5V and VB =–4.8V yields R_{13} = 49k.

$$V_{out1} = \left(1 + \frac{R_{13}}{R_{14}} + \frac{R_{13}}{R_{26}}\right) \bullet V_{CM} - \frac{R_{13}}{R_{26}} \bullet REF - \frac{R_{13}}{R_{14}} \bullet V_B - \frac{R_{13}}{R_{15}} \bullet V_{AC} \quad (32)$$

$$V_O = \left(1 + \frac{R_{10}}{R_{27}} + \frac{R_{10}}{R_{12}}\right) \bullet V_{CM} - \frac{R_{10}}{R_{27}} \bullet REF - \frac{R_{10}}{R_{12}} \bullet V_{out1} \quad (34)$$

2C. For a fixed, negative DC offset, R_{26} can be removed and R_{14} wired to ground (VB=0). The output voltage then becomes:

$$V_O = \left(\frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{14}}\right) \bullet V_{CM} + \left(\frac{R_{10} \bullet R_{13}}{R_{12} \bullet R_{15}}\right) \bullet V_{AC} \quad (37)$$

Again, for a required output AC level, k2 can be calculated. With k2 and R_{15} known, the value of $(R_{10} \bullet R_{13}/R_{12})$ is determined, in the present example, it is 3.6M. The value of R_{14} falls out from the required offset V_{OS} and the first part of equation given above. If V_{OS} = –48V, R_{14} can be calculated to be 225k for the continuing example. The output voltage of the first amplifier in this approach is given by:

$$V_{out1} = \left(1 + \frac{R_{13}}{R_{14}}\right) \bullet V_{CM} - \left(\frac{R_{13}}{R_{15}}\right) \bullet V_{AC} \quad (38)$$

Again, R_{13} can be calculated to get the maximum swing out of the summing amplifier (AMP1) without saturating it, in this case it also turns out to be 49k.

Step 3. Once R_{13} and R_{15} are selected, R_{10} and R_{12} are selected next. From step 2, the value of R_{10}/R_{12} is easily calculated to be $(k2 \bullet R_{15}/R_{13})$. For k2=240, the value of R_{10}/R_{12} equals 60 for approach A and 73.5 for approaches B and C in the given example. These ratios could be even higher if the choice of R_{13}–R_{15} is non-optimal or if a higher output voltage is required. The individual values of R_{10} and R_{12} can be somewhat arbitrarily chosen as long as they satisfy the ratio and the bias currents through the two are neither too low nor too high. The value of R_{10} may also be dictated by feedback loop considerations addressed in the next section. The selected values are R_{12} = 3.3k and R_{10} = 200k.

The value of R_{27} should always be $1.5 \bullet R_{10}$ for proper DC biasing of AMP2. The filter around AMP1 (consisting of R_{24}, C_{15}) can provide a high frequency noise pole if necessary.

Feedback Loop Compensation

The load behavior for the ring generator is different from a typical power supply load, which can be assumed to be resistive. The capacitive coupling introduces an integrator at the origin and a low frequency zero in the power stage gain equation. The resultant open loop power stage gain equation is given as:

$$G_d(s) = G_{lf} \bullet \frac{s_{z1}}{s} \bullet \frac{\left(1 + \frac{s}{s_{z1}}\right)}{\left(1 + \frac{s}{s_{p1}}\right)} \bullet \left(1 + \frac{s}{s_{z2}}\right) \quad (39)$$

Where:

$$G_{lf} = V_{in} \bullet \sqrt{\frac{0.4 \bullet R_l \bullet T_s}{L_p}} \quad (40)$$

$$s_{z1} = \frac{1}{R_l \bullet C_l} \quad (41)$$

$$s_{p1} = \frac{2}{R_l \bullet \left(\frac{C_l \bullet C_o}{C_l + C_o}\right)} \quad (42)$$

$$s_{z2} = \frac{1}{R_c \bullet C_o} \quad (43)$$

Using the power stage gain and the required crossover frequency, the compensation components can be calculated with conventional loop compensation techniques. The feedback loop should be designed to provide adequate phase margin at the crossover frequency. The error amplifier gain for the configuration in Figure 8 is given by (equation 44):

$$G_{vea}(s) = \left(\frac{R_{11}}{R_{10}}\right)\left(\frac{(1 + s \bullet R_{24} \bullet C_{15})}{(1 + s \bullet C_{14} \bullet [R_{11} + R_{25}])}\right) \quad (44)$$

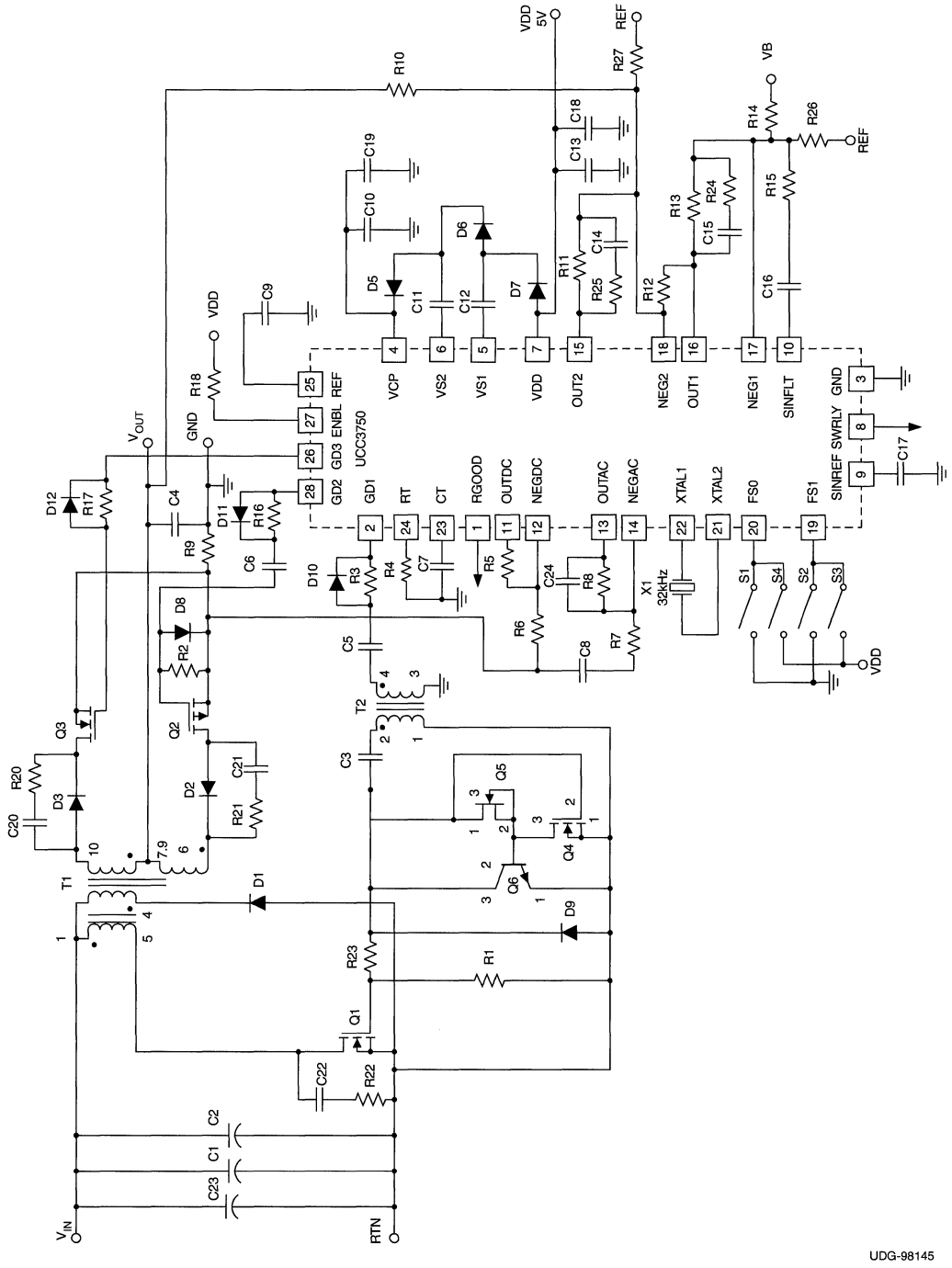


Figure 9. UCC3750 Detailed Application Circuit Schematic

This configuration can be modified by replacing R_{11} with a capacitor to give a pole at origin. That configuration also provides a high frequency pole for noise filtering. The location of the zero does not change.

Circuit Implementation and Results

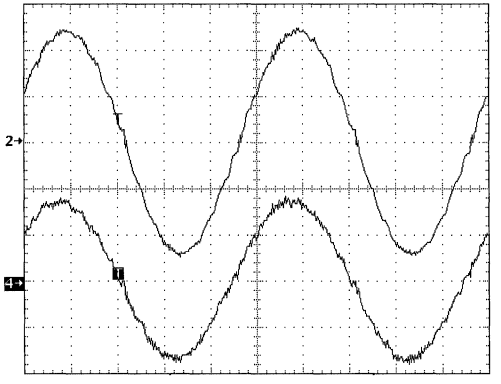
Using the design guidelines provided above, a four-quadrant flyback ring generator for 15 REN, $85V_{AC}$ output was designed and built. The circuit schematic of the designed converter is shown in Figure 9. The selection of power semiconductors and the transformer design followed the guidelines in Steps 4 and 5 respectively. The transformer used for the design is Coiltronics CTX08-13484 with primary inductance of 60µH. Values of critical circuit components are summarized in Table 5. The performance of the circuit was verified over different operating conditions. The efficiency was measured to be 81% for a 48V input and a 10 REN load. The output voltage and current waveforms are shown in Figure 10. The output voltage shows low harmonic content under normal load conditions. Under highly reactive loads, it can show some distortion near mode crossings. The distortion can be reduced by redesigning the transformer to have a lower magnetizing inductance with the associated penalty of higher peak currents and lower efficiency.

Table V.
Critical Circuit Components Selected Using Design Steps

Component (As shown in Figure 9)	Description
D1, D2, D3	BYV26C, 600V, 1A
Q1	IRF640, 200V, 0.18Ω, n-channel FET
Q2	MTP2P50, 500V, p-channel FET
Q3	IRF840, 500V, 0.85Ω n-channel FET
R10	200k
R11	1M
R12	3.32k
R13	61.9k
R14	374k
R15	15k
R26	560k
R27	300k
R5, R6	30k,10k
R9	1Ω, 1W sense resistor
T1	1:1:0.2:0.2 Turns ratio, 60µH Lp
T2	Low Lm, pulse transformer

Alternative Topology Implementations

The circuit shown in Figure 9 provides input to output isolation and uses a p-channel FET for Q2. In many applications however, isolation is not required. The circuit implementation can then be simplified by removing the gate drive transformer T2.



Time Scale: 10.0 ms/div
Upper Waveform: V_{OUT} (50V/div)
Lower Waveform: I_{OUT} (100mA/div)

Figure 10. Output Voltage and Current Waveforms

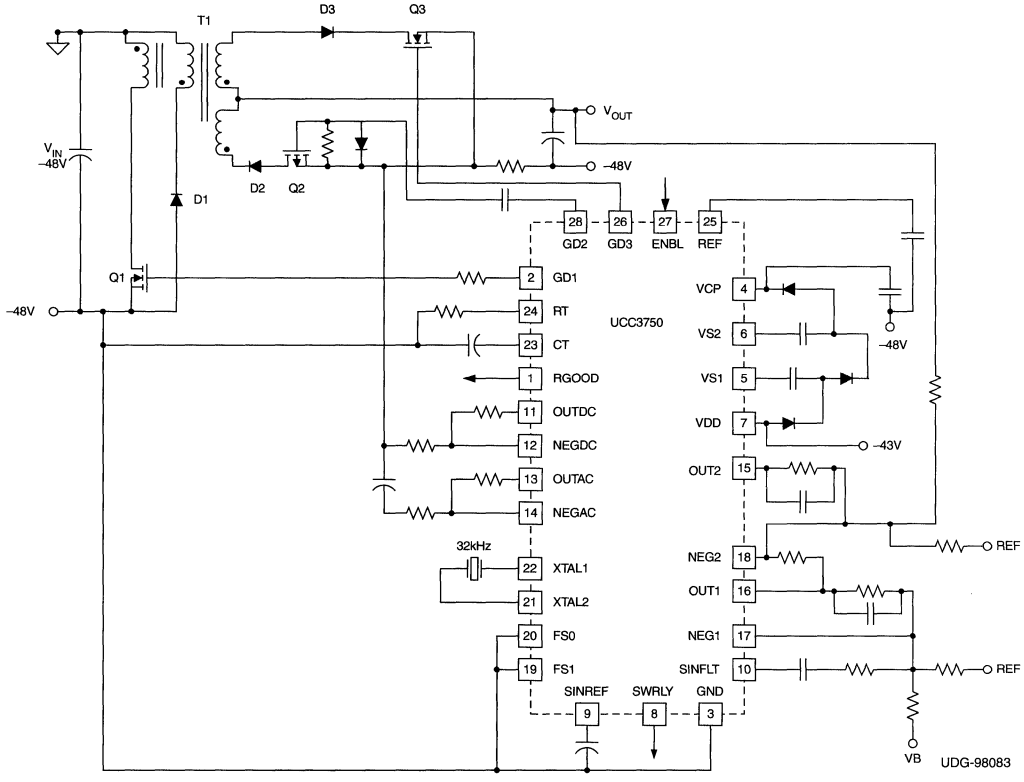


Figure 11. Non-isolated Ring Generator Implementation

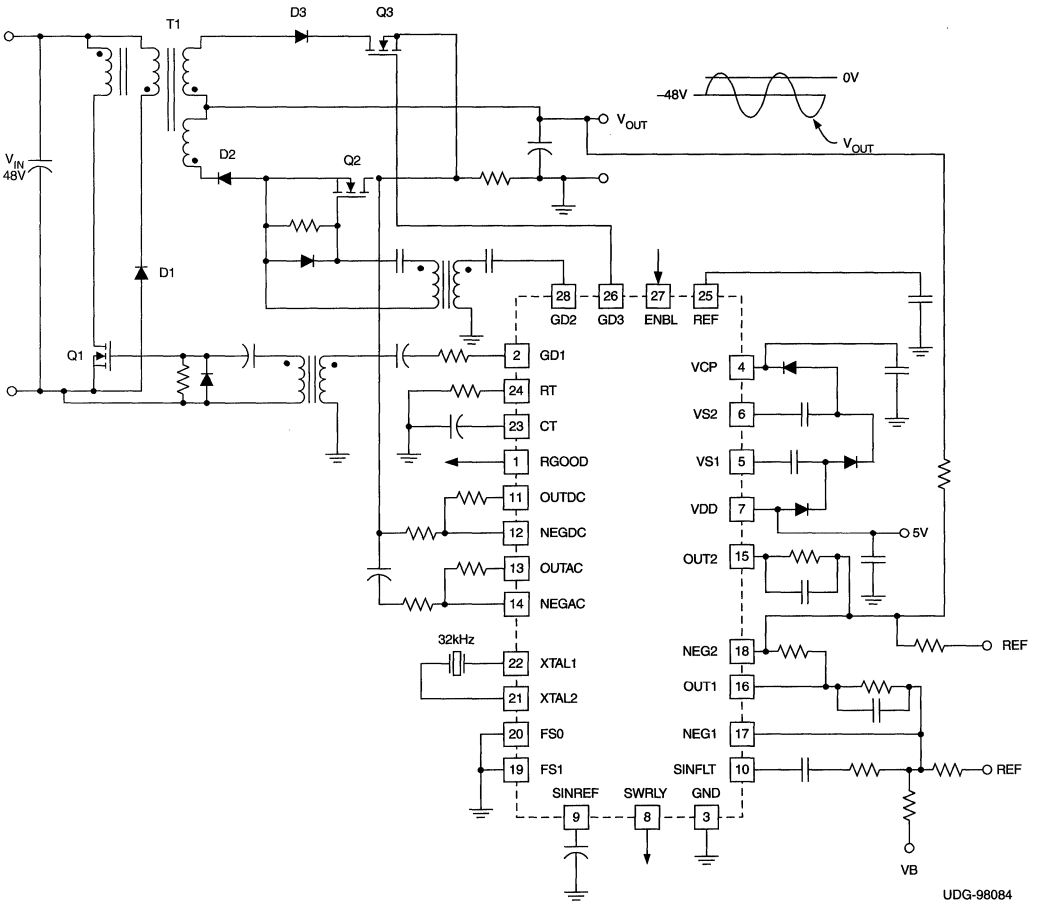


Figure 12. Alternative Implementation – N-channel Q2

This type of implementation is captured in Figure 11 where a non-isolated –48V input ring generator is depicted. The IC is referenced to the lowest voltage (–48V) and needs a 5V bias with respect to that voltage to operate. For non-isolated applications, this is easily derived using a resistive divider or a linear regulator.

In applications where the ring generator is designed as a module with isolation, other means of generating the bias voltage on the secondary are required. The most optimal way is to design a small flyback regulator for this purpose.

Another alternative that can be considered for the four-quadrant flyback converter is the selection of the switch Q2. The main reason for selecting a p-channel switch is to be able to drive it directly from the UCC3750. However, in many cases, the performance and selection available for p-channel MOSFETs are inferior to the n-channel alternatives. The n-channel switch requires an isolated/floating gate driver interface to the UCC3750.

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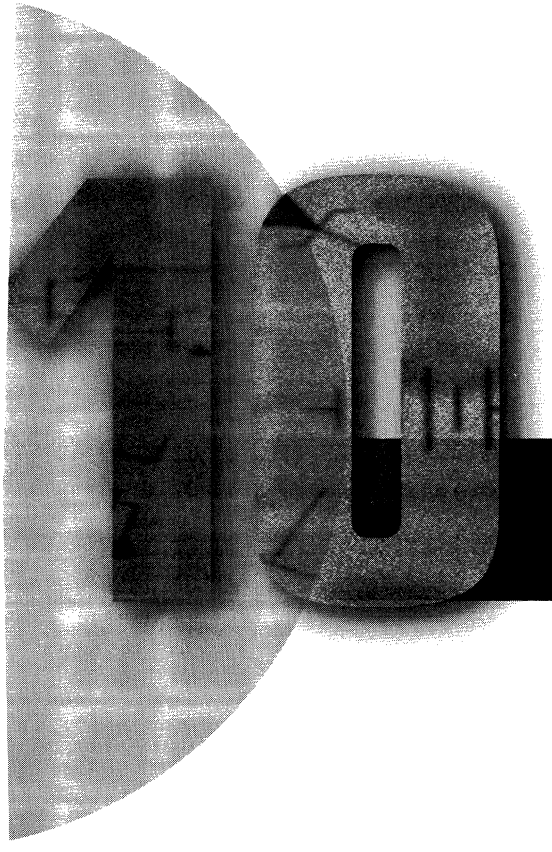


Unitrode Product Portfolio

Interface Products

Nonvolatile Products

Portable Power Products

Power Supply Control Products

SCSI

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5628+	UCC5630	UCC5632	UCC5638+	UCC5639+
Channels	14	9	9	15	15
Channel Capacitance	4	4	4	4	4
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD / SE	LVD / SE
Page Number	IF/3-78	IF/3-83	IF/3-93	IF/3-94	IF/3-99

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5640+	UCC5641+	UCC5646		
Channels	9	9	27		
Channel Capacitance	3	3	3		
Termination Impedance	Differential 105, Common Mode 150	Differential 105, Common Mode 150	Differential 105, Common Mode 150		
Disconnect High or Low	H	L	H		
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type LVD or SE / LVD	LVD	LVD	LVD		
Page Number	IF/3-104	IF/3-108	IF/3-112		

+ New Product

SCSI (cont.)

Multimode / LVD SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5510+	UCC5630A	UCC5672+	UCC5680	
Channels	9	9	9	9	
Channel Capacitance	4	4	4	4	
Termination Impedance	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single110, Differential 105, Common Mode 150	Single 110, Differential 105, Common Mode 150	
Diff B input filter	N	N	Y	Y	
Disconnect High or Low	N/A	H	H	H	
Termpwr Voltage Range	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	2.7 - 5.25	
Supports Active Negation	Y	Y	Y	Y	
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	
Type LVD or SE / LVD	LVD / SE	LVD / SE	LVD / SE	LVD	
Page Number	IF/3-5	IF/3-87	IF/3-120	IF/3-121	

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5601	UC5602	UC5603	UC5604	UC5605
Channels	18	18	9	9	9
Channel Capacitance	10	11	6	9	4
Termination Impedance	110	110	110	110	110
Disconnect High or Low	H	H	H	H	L
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	N	N	Y	N	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-9	IF/3-13	IF/3-18	IF/3-22	IF/3-26

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5606	UC5607	UC5608	UC5609	UC5612
Channels	9	18	18	18	9
Channel Capacitance	1.8	8	6	6	4
Termination Impedance	110 & 2500	110	110	110	110
Disconnect High or Low	L	2L	H	L	H
Termpwr Voltage Range	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-30	IF/3-34	IF/3-37	IF/3-40	IF/3-43

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UC5613	UCC5614	UCC5617	UCC5618	UCC5619
Channels	9	9	18	18	27
Channel Capacitance	3	1.8	2.5	2.5	3
Termination Impedance	110	110 & 2500	110	110	110
Disconnect High or Low	H	H	L	H	L
Termpwr Voltage Range	4 - 5.25	2.7 - 5.25	4 - 5.25	4 - 5.25	4 - 5.25
Supports Active Negation	Y	Y	Y	Y	Y
SCSI Hot Plug Current	<10nA	<10nA	<10nA	<10nA	<10nA
Type SE, LVD or SE / LVD	SE	SE	SE	SE	SE
Page Number	IF/3-47	IF/3-51	IF/3-55	IF/3-59	IF/3-63

+ New Product

SCSI (cont.)

Single Ended SCSI Active Terminators	UNITRODE PART NUMBER				
	UCC5620	UCC5621	UCC5622		
Channels	27	27	27		
Channel Capacitance	3	3	3		
Termination Impedance	110	110	110		
Disconnect High or Low	H	Split Low	Split High		
Termpwr Voltage Range	4 - 5.25	4 - 5.25	4 - 5.25		
Supports Active Negation	Y	Y	Y		
SCSI Hot Plug Current	<10nA	<10nA	<10nA		
Type SE, LVD or SE / LVD	SE	SE	SE		
Page Number	IF/3-66	IF/3-70	IF/3-74		

Special Functions Circuit	UNITRODE PART NUMBER		
	UCC5661		
Part Name	Ethernet Coaxial Impedance Monitor		
Description	Contains all the Functions Required to Monitor Ethernet Coaxial Systems and is Compatible with IEEE 802.3, 10Base5, 10Base2, and 10BaseT		
Page Number	IF/3-112		

+ New Product

Bus Bias Generators

Special Functions	UNITRODE PART NUMBER				
	UC382	UC385	UC560	UCC561+	UC563+
Bus Standard	GTL / BTL	GTL / BTL	SCSI-1,2,3	SPI-2,3	VME / VME64
Sink / Source Current	Pgm / 3A	Pgm / 5A	300mA / –750mA	200mA / –200mA	475mA / –575mA
Page Number	PS/4-2	PS/4-8	IF/4-3	IF/4-7	IF/4-10

+ New Product

Hot Swap Power Managers

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3912	UCC3913	UC3914	UCC3915	UCC39151
Voltage Range	3V to 8V	–10.5V to External Limitation	5V to 35V	7V to 15V	7V to 15V
Current Range	0A to 3A	Externally Limited	Externally Limited	0A to 3A	0A to 3A
Integrated Power FET	Y	N	N	Y	Y
RDSon	150mΩ	N/A	N/A	150mΩ	150mΩ
Programmable Fault Threshold	Y	Y	Y	Y	Y
Programmable Time Delay	Y	Y	Y	Y	Y
Latched Fault Mode	N	Y	Y	N	N
Average Power Limiting	N/A	Y	Y	N/A	N/A
Application / Design Note	DN-58, DN-68, U-151	DN-67		DN-58, DN-68, U-151	DN-58, DN-68, U-151
Available Package	TSSOP, SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-9	IF/5-15	IF/5-23	IF/5-37	IF/5-42

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3916	UCC39161	UCC3917+	UCC3918	UCC3919
Voltage Range	4V to 6V	4V to 6V	10V to External Limitation	3V to 6V	3V to 8V
Current Range	–1.8A to –1.5A	–1A to –0.7A	Externally Limited	0A to 4A	Externally Limited
Integrated Power FET	Y	Y	N	Y	N
RDSon	220mΩ	220mΩ	N/A	60mΩ	N/A
Programmable Fault Threshold	N	N	Y	Y	Y
Programmable Time Delays	Y	Y	Y	Y	Y
Latched Fault Mode	N	N	Y	N	Y
Average Power Limiting	N/A	N/A	Y	N/A	Y
Application / Design Note			DN-98	DN-87	DN-95
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP
Page Number	IF/5-47	IF/5-50	IF/5-53	IF/5-61	IF/5-68

+ New Product

Hot Swap Power Managers (cont.)

Hot Swap Power Managers	UNITRODE PART NUMBER				
	UCC3921	UCC3995+	UCC3996+		
Voltage Range	–10.5V to External Limitation	2.75V to 5.5V	2.75V to 13.6V Two Supplies Sequenced		
Current Range	Externally Limited	Externally Limited	Externally Limited		
Integrated Power FET	N	N	N		
RDSon	N/A	N/A	N/A		
Programmable Fault Threshold	Y	Y	Y		
Programmable Time Delay	Y	Y	Y		
Latched Fault Mode	Y	N	Y		
Average Power Limiting	Y	Y	Y		
Application / Design Note					
Available Package	SOIC or PDIP	TSSOP or SOIC	TSSOP, SOIC or PDIP		
Page Number	IF/5-78	IF/5-98	IF/5-100		

Special Functions	UNITRODE PART NUMBER				
	UCC3831	UCC38531	UCC3981+	UCC39811+	UCC3985+
Part Name	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	Universal Serial Bus Power Controller	CompactPCI Hot Swap Power Manager
Description	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Powers Four 5V Peripherals and One 3.3V USB Controller	Fully CompactPCI Compliant. Four Channels for Individual Control of Four Supplies 12V, –12V, 5V, and 3.3V
Application / Design Note					
Available Package	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	SOIC or PDIP	TSSOP, SOIC or PDIP
Page Number	IF/5-3	IF/5-6	IF/5-88	IF/5-91	IF/5-94

+ New Product

Drivers / Receivers Transceivers

Interface Drivers, Receivers	UNITRODE PART NUMBER				
	UC5170C	UC5171	UC5172	UC5180C	UC5181C
Drivers	8	8	8		
Receivers				8	8
Power	±10V	±10V	±10V	+5V	+5V
EIA232 / V.28	Y	Y	Y	Y	Y
EIA423 / V.10	Y	Y	Y	Y	Y
EIA422 / V.11	N	N	N	Y	Y
V.35	N	N	N	Y	Y
Appletalk	N	N	N	N	Y
Page Number	IF/6-3	IF/6-7	IF/6-11	IF/6-15	IF/6-18

+ New Product

Interface Transceivers	UNITRODE PART NUMBER				
	UC5350	UC5351+			
Drivers	1	1			
Receivers	1	1			
Power	+5V	+5V to 24V			
Control Area Network	Y	Y			
Device Net	Y	Y			
SDS	Y	Y			
Page Number	IF/6-21	IF/6-27			

+ New Product

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode nonvolatile controllers provide power monitoring, write-protection, and supply switching to convert standard SRAM and a backup battery into a reliable, predictable nonvolatile memory. The nonvolatile controller modules are complete battery-backup solutions including an encapsulated 130mAh lithium cell that is isolated until power is applied.

- Power monitoring and switching for 3V battery-backup applications
- 5V V_{CC} operation
- Automatic write-protection during power-up/power-down cycles
- Automatic switching from V_{CC} to first backup battery and from first backup battery to second backup battery
- Battery internally isolated until power is first supplied
- Industrial temperature range available

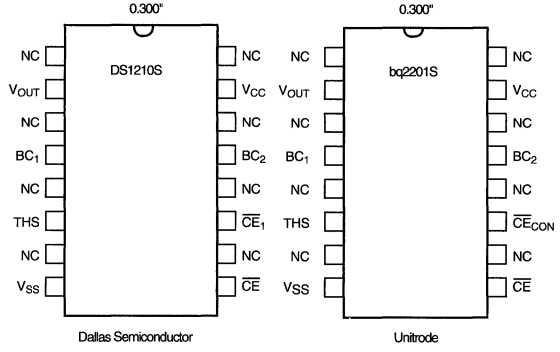
Static-RAM Nonvolatile Controler Selection Guide

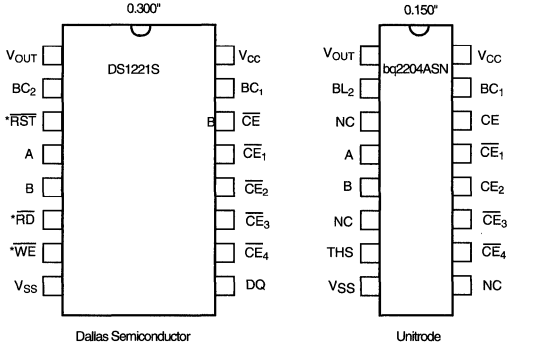
SRAM Banks Controlled	Battery Monitor Outputs	Reset Output	I_{OUT} (Typ.)	Pins / Package	Part Number	Page Number
1			160 mA	8 / NDIP, NSOIC 16 / NSOIC	bq2201	NV/3-3
2		✓	160 mA	16 / NDIP, NSOIC	bq2202	NV/3-11
2	✓	✓	160 mA	16 / NDIP, NSOIC	bq2203A	NV/3-19
4			160 mA	16 / NDIP, NSOIC	bq2204A	NV/3-27
2		✓	160 mA	12 / DIP module	bq2502	NV/3-35

Static-RAM Nonvolatile Controller Cross-Reference	
Dallas Semiconductor	**Unitrode**
DS1210	bq2201PN [1, 2]
DS1210S	bq2201S [1, 2]
DS1218	bq2201PN [1, 2]
DS1218S	bq2201SN [1, 2]
DS1221	bq2204APN [1, 3]
DS1221S	bq2204ASN [1, 3, 4]

Notes:

1. Unitrode's bq2201 and bq2204A do not incorporate a "check battery status" function.
2. Unitrode's bq2201 pins THS and BC_2 should be tied to V_{SS}.
3. Optional "security feature" DS1221 pins are no-connect on the bq2204A.
4. Unitrode's bq2204ASN is a small 16-pin, 150-mil SOIC, compared to the DS1221S, which is a 16-pin, 300-mil SOIC.





*These pairs must be connected to ground if the security option is not used.

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's NVSRAMs integrate extremely low standby power SRAM, nonvolatile control circuitry, and a long-life lithium cell in either a single DIP package or a two-piece LIFETIME LITHIUM SMT module. The NVSRAMs combine secure long-term nonvolatility (more than 10 years without power) with standard SRAM pinouts and fast, unlimited read/write operation.

- ➤ Data retention without power
- ➤ Automatic write-protection during power-up/power-down cycles
- ➤ Industry-standard pinout
- ➤ Conventional SRAM operation; unlimited write cycles
- ➤ 10 or 5 years minimum data retention in the absence of power
- ➤ Battery internally isolated until power is first supplied
- ➤ Industrial temperature range available

Nonvolatile Static RAM Selection Guide

Density	Config-uration	Access Time (ns)	Minimum Data-Retention Time	Pins / Package	Part Number[1]	Page Number
64Kb	8Kb x 8	70, 85[2], 150[2], 200	10 years	28 / DIP	bq4010/Y	NV/5-3
256Kb	32Kb x 8	70[2], 100, 150[2], 200	10 years	28 / DIP	bq4011/Y	NV/5-13
1Mb	128Kb x 8	70[2], 85[2], 120	10 years	32 / DIP 32 / SMT	bq4013/Y	NV/5-23
2Mb	256Kb x 8	85, 120	10 years	32 / DIP	bq4014/Y	NV/5-33
4Mb	512Kb x 8	70, 85, 120	10 years	32 / DIP 32 / SMT	bq4015/Y	NV/5-42
8Mb	1024Kb x 8	70	10 years	36 / DIP	bq4016Y	NV/5-52
16Mb	2048Kb x 8	70	5 years	36 / DIP	bq4017Y	NV/5-61
64Kb	8kB x 8	70	10 years	28 / SNAPHAT	bq4310/Y+	NV/5-70
256Kb	32kB x 8	70[3], 100[5]	10 years	28 / SNAPHAT	bq4311Y/L[4]+	NV/5-81

Notes:
1. "Y" version denotes 10% V_{CC} tolerance.
2. "Y" version available in -40°C to +85°C industrial temperature range.
3. "Y" version only.
4. "L" version denotes 3.2V typical Vcc operation.
5. "L" version only.

+ New Product

Nonvolatile Static RAM Cross-Reference			
Density	Dallas Semiconductor	STMicroelectronics	Unitrode
64Kb	DS1225AB	M48Z08	bq4010
	DS1225AD	M48Z18	bq4010Y
	-	M48Z58	bq4010/4823Y
	DS1225Y	M48Z58Y	bq4010Y
256Kb	DS1230AB	M48Z35	bq4011
	DS1230Y	M48Z35Y	bq4011Y/4833Y
1M	DS1245AB	M48Z128	bq4013
	DS1245Y	M48128Y	bq4013Y
2M	DS1258AB	-	bq4014
	DS1258Y	-	bq4014Y
4M	DS1250AB	M48Z512A	bq4015
	DS1250Y	M48Z512AY	bq4015Y
8M	DS1265AB	-	bq4016
	DS1265Y	-	bq4016Y
16M	DS1270AB	M48Z2M1	bq4017
	DS1270Y	M48Z2M1Y	bq4017Y

Nonvolatile SRAMs and RTCs (NV) Selection Guides

Unitrode's real-time clocks (RTCs) provide highly integrated clock/calendar solutions for microcomputer-based designs. Each *module* is a completely self-contained unit, including IC, crystal, and a battery ensuring operation for 10 years in the absence of power. The very compact, low-power *ICs* need only a battery and a crystal for operation. NVSRAM controller versions allow users to make inexpensive SRAM nonvolatile for data and configuration storage in

- Clock/calendar counts seconds through years with daylight savings and leap-year adjustments
- IBM PC AT-compatible clocks include:
  - 5- or 3-Volt operation
  - 114, 240, or 242 bytes of user nonvolatile RAM storage
- 32kHz output for power management
- Nonvolatile control for an external SRAM
- SRAM-based clocks feature:
  - SRAM interface
  - Up to 512 kilobytes of NVSRAM
  - CPU supervisor
- One minute per month clock accuracy in modules
- IC versions require only a crystal and battery

Real-Time Clock Selection Guide

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	32kHz Output	CPU Supervisor	Pins / Package	Part Number	Page Number
114		Muxed	5V			24 / DIP, SOIC	bq3285	NV/4-3
242		Muxed	5V	✓		24 / DIP, SOIC, SSOP	bq3285E	NV/4-22
242		Muxed	5V	✓		24 / SSOP	bq3285EC/ED	NV/4-46, NV/4-69
242		Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq3285L	NV/4-22
242		Muxed	3V	✓		24 / SSOP	bq3285LC/LD	NV/4-46, NV/4-69
240		Muxed	3V			24 / SSOP	bq3285LF+	NV/4-92
114		Muxed	5V			24 / DIP module	bq3287/A	NV/4-111
242		Muxed	5V	✓		24 / DIP module	bq3287E/EA	NV/4-115
242		Muxed	3V			24 / DIP Module	bq3287LD+	NV/4-119
114	✓	Muxed	5V			24 / DIP, SOIC	bq4285	NV/4-123
114	✓	Muxed	5V	✓		24 / DIP, SOIC, SSOP,	bq4285E	NV/4-143
114	✓	Muxed	3V	✓		24 / DIP, SOIC, SSOP	bq4285L	NV/4-143
114	✓	Muxed	5V			24 / DIP module	bq4287	NV/4-168
0		SRAM	3V		✓	28 / DIP, SOIC 28 / SNAPHAT	bq4802+	NV/4-174
8K	✓	SRAM	5V		✓	28 / DIP module	bq4822Y	NV/4-176
8K		SRAM	5V			28 / SNAPHAT	bq4823Y+	NV/4-191

+ New Product

Real-Time Clock Selection Guide (Continued)

Onboard RAM (bytes)	NVRAM Control	Bus Interface	Voltage	CPU Supervisor	Pins / Package	Part Number	Page Number
32K		SRAM	5V		28 / DIP module	bq4830Y	NV/4-205
32K		SRAM	5V	✓	32 / DIP module	bq4832Y	NV/4-218
32K		SRAM	5V		28 / SNAPHAT	bq4833Y+	NV/4-233
128K		SRAM	5V	✓	32 / DIP module	bq4842Y	NV/4-247
0	✓	SRAM	5V	✓	28 / DIP, SOIC	bq4845/Y	NV/4-262
0	✓	SRAM	5V	✓	28 / DIP module	bq4847/Y	NV/4-279
512K		SRAM	5V	✓	32 / DIP module	bq4850Y	NV/4-282
512K		SRAM	5V	✓	36 / DIP module	bq4852Y	NV/4-295

+ New Product

Real-Time Clock Cross-Reference

Dallas Semiconductor	STMicroelectronics	Unitrode
DS1285/885	-	bq3285P
DS1285S/885S	-	bq3285S
DS1287/887	-	bq3287MT
DS1287A/887A	M48T86	bq3287A
DS14285	-	bq4285
DS14285	-	bq4285P
DS14285S	-	bq4285S
DS14287	-	bq4287
DS1643	M48T08/T18 M48T58Y/59Y	bq4822Y
DS1644	M48T35	bq4830Y[1]
DS1646	-	bq4842Y[2]

Notes:
1. Memory upgrade.
2. Additional bq4842 features: microprocessor reset, watchdog monitor, clock alarm, and periodic interrupt.

Portable Power (PP) Selection Guides

Unitrode battery charge-management ICs provide full-function, safe charge control for all types of rechargeable chemistries. Functions include pre-charge qualification and conditioning, charge regulation, and termination.

- ➤ Fast charging and conditioning of nickel cadmium, nickel metal hydride, lead acid, lithium ion, or rechargeable alkaline batteries
- ➤ Flexible charge regulation support:
  - — Linear
  - — Switch-mode
  - — Gating control (external regulator)
- ➤ Easily integrated into systems or as a stand-alone charger
- ➤ Direct LED outputs display battery and charge status
- ➤ Fast, safe, and reliable chemistry-specific charge-termination methods, including rate of temperature rise ($\Delta T/\Delta t$), negative delta voltage ($-\Delta V$), peak voltage detect (PVD), minimum current, maximum temperature, maximum voltage, and maximum time
- ➤ Optional top-off and maintenance charging
- ➤ Discharge-before-charge option for NiCd
- ➤ Complete set of development tools available for quick product-desig

Battery Charge-Management Selection Guide

Battery Technology	Key Features	Fast-Charge Termination Method	Pins / Package	Part Number	Page Number
Multi-Chemistry	Complete change management with integrated switching controller	PVD, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000+	PP/3-7
		$\Delta T/\Delta$, minimum current, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2000T+	PP/3-20
NiMH, NiCd	Gating control of an external regulator	$-\Delta V$, PVD, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002/C/E/F/G	PP/3-3
		$\Delta T/\Delta t$, maximum temperature, maximum time	8/0.300" DIP, 8/0.150" SOIC	bq2002D/T	PP/3-3
	PWM Controller	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.300" SOIC	bq2003	PP/3-73
	PWM controller, enhanced display mode	$-\Delta V$, PVD, $\Delta T/\Delta t$, maximum temperature, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2004/E/H	PP/3-5
	Dual sequential charge-controller for 2-bay chargers	$-\Delta V$, $\Delta T/\Delta t$, maximum temperature, maximum time	20/0.300" DIP, 20/0.300" SOIC	bq2005	PP/3-119
Lithium Ion	PWM controller	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2054	PP/3-6
	Low-dropout linear with AutoComp™ feature	-	8/0.150" SOIC	bq2056/T/V	PP/3-186
	PWM controller, enhanced display mode	Minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2954+	PP/3-6
	PWM controller, differential current sense	Minimum current, maximum time	20/0.300" DIP, 20/0.300" SOIC	UCC3956	PP/3-6

+ New Product

Continued on next page

Battery Charge-Management Selection Guide (Continued)

Battery Technology	Key Features	Fast-Charge Termination Method	Pins/ Package	Part Number	Page Number
Lead Acid	PWM controller, 3 charge algorithms	Maximum voltage, $-\Delta^2V$, minimum current, maximum time	16/0.300" DIP, 16/0.150" SOIC	bq2031	PP/3-154
	Linear controller	Maximum voltage, minimum current	16/0.300" DIP 16/0.300"SOIC	UC3906	PP/3-237
	PWM controller, differential current sense	Maximum voltage, minimum current	20/0.300" DIP 20/0.300"SOIC	UC3909	PP/3-244
Rechargeable Alkaline	2-cell charging	Maximum voltage	8/0.300"DIP, 8/0.150" SOIC	bq2902	PP/3-194
	3- or 4-cell charging	Maximum voltage	14/0.300" DIP, 14/0.150" SOIC	bq2903	PP/3-204

The bq2002 fast-charge control ICs are low-cost CMOS battery charge-control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Controlling a current-limited or constant-current supply allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2002 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply or by replacement of the battery. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input. In some versions, this input may be used to synchronize voltage sampling. A low-power standby mode reduces system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Direct LED output displays charge status
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- Top-off and pulse-trickle charge rates available
- Synchronized voltage sampling available
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC packaging

bq2002 Family Selection Guide

	Part Number						
	$-\Delta V$ or PVD Termination					$\Delta T/\Delta t$ Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Fast charge time limit options (minutes)	160/80/40	160/100/40	160/80/40	200/80/40	160/80/40	320/80/40	440/110/55
Hold-off period options (seconds)	600/300/10	600/300/10	300/150/75	300/150/75	300/150/75	none	none
Top-off options	C/32,C/16,0	C/32,C/16,0	none	C/16,0	C/16,0	C/64,C/16,0	none
Top-off period	4.6ms	4.6ms	n/a	1.17s	1.17s	4.6ms	n/a
Pulse-trickle options	C/64,C/32	C/64,C/32	C/32	C/32	C/32	C/256,C/128	none
Pulse-trickle period	9 or 18ms	9 or 18ms	1.17s	1.17s	1.17s	18 or 73ms	n/a
Synchronized voltage sampling	no	no	yes	yes	yes	no	no
Minimum voltage pre-charge qualification	no	no	yes	yes	yes	no	no

Continued on next page

bq2002 Family Selection Guide (Continued)

	Part Number						
	-ΔV or PVD Termination					ΔT/Δt Termination	
Feature	bq2002	bq2002F	bq2002C	bq2002E	bq2002G	bq2002T	bq2002D
Hysteresis on high-temperature cut-off	no	no	no	no	no	yes	yes
LED in "charge pending" phase	n/a	n/a	flashes	flashes	flashes	on	off
Page number	PP/3-35	PP/3-35	PP/3-43	PP/3-61	PP/3-61	PP/3-51	PP/3-51

The bq2004 fast-charge control ICs are low-cost CMOS battery charge control ICs providing reliable charge termination for both NiCd and NiMH battery applications. Integration of PWM current control circuitry allows the ICs to be the basis for a cost-effective stand-alone or system-integrated charger. The bq2004 family includes options that integrate fast charge, top-off, and pulse-trickle charge control in a single IC for charging one or more NiCd or NiMH batteries.

A new charge cycle is started by the application of a charging supply, replacement of the battery, or a logic-level pulse. For safety, fast charge is inhibited if the battery voltage or temperature is outside of configured limits. Fast charge may be inhibited using the INH input, which also puts the IC into a low-power standby mode, reducing system power consumption.

- Fast-charge control of nickel cadmium or nickel-metal hydride batteries
- Integrated PWM closed-loop current control
- Configurable, direct LED output displays charge status
- Low-power mode
- Top-off and pulse-trickle charging available
- Fast-charge terminations available:
  - $-\Delta V$
  - Peak Voltage Detection (PVD)
  - $\Delta T/\Delta t$
- Backup safety termination on maximum voltage, maximum temperature, and maximum time
- 16-pin 300-mil DIP or 150-mil SOIC packaging

bq2004 Family Selection Guide

Feature	Part Number bq2004	bq2004E	bq2004H
Maximum time-out selections (minutes)	360/180/90/45/23	325/154/77/39/19	650/325/154/77/39
Hold-off period selections (seconds)	137/820/410/200/100	137/546/273/137/68	273/546/546/273/137
Charge rate during hold-off period	full fast-charge rate	1/8*fast-charge rate	1/8*fast-charge rate
Top-off options	C/2,C/4,C/8,C/16,0	C/2,C/4,C/8,C/16,0	C/4,C/8,C/16,C/32,0
Top-off pulse width/period (seconds)	260/2080	260/2080	260/2080
Top-off duration	MTO	0.235*MTO	0.235*MTO
Pulse-trickle selections	C/32,C/64,0	C/512,0	C/512,0
Pulse-trickle period (ms)	4.17/8.3/16.7/33.3/66.7	66.7/133/267/532	33.3/66.7/133/267
Pulse-trickle pulse width (seconds)	260	260	260
DSEL floating disables pulse-trickle	no	yes	yes
VSEL high disables low-temperature fault threshold	yes	no	no
High-temperature fault threshold	1/4LTF + 3/4 TCO	1/3LTF + 2/3 TCO	1/3LTF + 2/3 TCO
Page number	PP/3-91	PP/3-105	PP/3-105

Li-Ion PWM Charge IC Selection Guide

Feature	Part Number bq2054	bq2954	UCC3956
Charge algorithm	During pre-qualification, the bq2054 charges using a low trickle current if the battery voltage is low. Then it charges using constant current followed by constant volatge. After fast-charge termination, charge is re-initiated by resetting the power to the IC or by inserting a new battery.	Performs similar to the bq2054, but the bq2954 also re-initiates a recharge if the battery voltage falls below a threshold level. This allows the bq2954 to maintain a full charge in the battery at all times.	Uses a 4-step charge algorithm: low-current trickle charge (when the cell voltage is below a user- programmable level); high- current bulk charge; constant-voltage overcharge; optional top-off with user-programmable timer
Current-sensing technique	Low-side current sensing	Low-side and high-side current sensing	Fully differential high-side current sensing can be used up to 20V common mode without the need for external level shifting.
Charge initiation	Application of power or detection of battery insertion	Application of power or detection of battery insertion	One-shot charge initiates charging, or a simple comparator initiates charging on battery insertion.
Detection of deeply discharged (bad) cells	Minimum cell voltage required for fast charge: 2V/cell Trickle-charge period: 1 * MTO	Minimum cell voltage required for fast charge: 3V/cell Trickle-charge period: 0.25 * MTO (for faster detection of bad cells)	User-programmable threshold limits charge current when battery cells are deeply discharged and provides short-circuit protection.
Charge termination based on minimum current	User-programmable minimum current is a ratio of the charging current: 1/10, 1/20, 1/30. A safety charge timer is also available.	User-programmable minimum current is a ratio of the charging current: 1/10, 1/15, 1/20. A safety charge timer is also available.	User-programmable minimum current or user-programmable overcharge timer
Temperature monitoring	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	Measured using an external thermistor. Fast charge is inhibited if the battery temperature is outside user-configured limits.	No
Status display	3 LEDs for state of charge	2 LEDs or one bi-color LED optimize state of charge	2 LEDs for state of charge including end of charge
Full-charge indication	LEDs indicate full charge after charge termination	LEDs indicate full charge just before charge termination	LEDs indicate full charge on charge termination
Input voltage range	4.5V to 5.5V	4.5V to 5.5V	6.5V to 20V
Typical supply current	2mA	2mA	5mA
Voltage regulation accuracy	±1% at 25°C	±1% at 25°C	±1% at 25°C
Wakeup feature for battery pack protectors	No	Yes	No
Integrated PWM controller	Yes	Yes	Yes
Pins/package	16-pin narrow PDIP or SOIC	16-pin narrow PDIP or SOIC	20-pin SOIC or DIP
Page number	PP/3-170	PP/3-217	PP/3-253

Portable Power (PP) Selection Guides

Unitrode's Gas Gauge ICs measure the available charge, calculate self-discharge, and communicate the available charge of a battery pack over a serial port or by directly driving an LED display.

- ➤ Accurate measurement of available charge for nickel cadmium, nickel metal-hydride, lithium ion, lead-acid batteries, and primary lithium
- ➤ Designed for battery-pack integration
- ➤ 150µA or less typical operating current
- ➤ Serial port or direct LED display for remaining battery capacity indication
- ➤ Available capacity is compensated for charge/discharge rate and temperature
- ➤ Accurately measures across a wide range of currents

Battery Capacity-Monitoring ICs Selection Guide

Battery Technology	Approximate Pack Capacity (mAh)	Communication Interface	Additional Key Features	Pins / Package	Part Number	Page Number
NiCd/NiMH	800-5000	1-wire DQ	5 or 6 LED outputs	16 /SOIC	bq2010	PP/4-3
			Slow-charge control	16 /SOIC	bq2012	PP/4-81
			External charge-control support	16 /SOIC	bq2014	PP/4-123
		1-wire HDQ	Register-compatible with bq2050H	16 /SOIC	bq2014H+	PP/4-149
NiCd	800-2000	1-wire DQ	See bq2011 Family Selection Guide	16 /SOIC	bq2011 bq2011J bq2011K	PP/4-24, PP/4-45, PP/4-63
NiCd/NiMH/ Lead Acid	2000-10,000	1-wire HDQ	Programmable offset and load compensation	16 /SOIC	bq2013H	PP/4-103
Li-Ion	800-5000	1-wire DQ	Remaining power (Wh) indication	16 /SOIC	bq2050	PP/4-215
		1-wire HDQ	Register-compatible with bq2014H	16 /SOIC	bq2050H	PP/4-237
Primary Lithium	800-15,000	1-wire HDQ	Programmable discharge efficiency compensation	16 /SOIC	bq2052+	PP/4-259
NiCd/NiMH Lead Acid/ Li-Ion	800-10,000	2-wire SMBus	SBS rev. 1.0-compliant	16 /SOIC	bq2040	PP/4-185
			SBS rev. 0.95-compliant	16 / SOIC	bq2092	PP/4-314
			SBS rev. 1.0-compliant with 5 LEDs	16 /SOIC	bq2945	PP/4-340
		2-wire SMBus or 1-wire HDQ16	SBS rev. 1.1-compliant	28 / SSOP	bq2060+	PP/4-276
Any	Any	1-wire HDQ	Analog peripheral for µC	8 / SOIC or TSSOP	bq2018	PP/4-170

+ New Product

The bq2011 Gas Gauge ICs provide accurate capacity monitoring of rechargeable batteries in high discharge rate environments. The ICs can monitor a wide range of charge/discharge currents using the onboard V-to-F converter and a low-value sense resistor. The ICs track remaining capacity (NAC) and compensate it for battery self-discharge, charge/discharge rate, and temperature. Five LEDs can communicate remaining capacity in 20% increments. A serial port allows a host microcontroller to access the nonvolatile memory registers containing battery capacity, voltage, temperature, and other critical parameters.

- Accurate measurement of available charge in rechargeable batteries
- Designed for NiCd high discharge rate applications
- Drives 5 LEDs for capacity indication
- Automatic charge self-discharge and discharge compensation
- Low operating current
- 16-pin narrow SOIC

bq2011 Family Selection Guide

Feature	Part Number bq2011	bq2011J	bq2011K
Display	Relative or absolute	Absolute	Absolute
Programmed Full Count (PFC) range	4.5–10.5mVh	2.21–3.81mVh	2.21–3.81mVh
Nominal Available Capacity (NAC) on reset	NAC = 0	NAC = PFC or 0	NAC = PFC or 0
Self-discharge rate	NAC/80	NAC/80 or disabled	NAC/80 or disabled
Charge compensation	75–95% based on rate and temperature	65–95% based on rate and temperature	70–95% based on rate and temperature
Discharge compensation	75–100% plus temperature compensation	75–100% plus temperature compensation	100%
End-of-discharge voltage	0.9V/cell	0.9V/cell	0.96–1.16V/cell
Page number	PP/4-24	PP/4-45	PP/4-63

Portable Power (PP) Selection Guides

Unitrode's battery management module products provide true turn-key solutions for capacity monitoring and charge control of NiCd, NiMH, Li-Ion, or Rechargeable Alkaline battery packs. Designed for battery pack integration, the small boards contain all necessary components to easily implement intelligent or smart battery packs in a portable system. The wide selection of boards offers battery monitoring, capacity tracking, charge control, and remaining capacity communication to the host system or user. The boards are fully tested and provide direct cell connections for simple battery pack

- Turnkey solutions for intelligent or smart batteries for portable equipment
  - Computers, cellular phones, and camcorders
  - Handheld terminals
  - Communication radios
  - Medical and test equipment
  - Power tools
- Capacity monitoring and charge control
- Pushbutton-activated LED capacity indication
- Designed for battery pack integration
  - Small size
  - Low power
  - Direct cell connections

Battery-Management Modules Selection Guide

Battery Technology	Key Features	Part Number	Page Number
NiCd/NiMH	Capacity monitoring, LED indication, serial communications port	bq2110	PP/5-2
	Capacity monitoring, slow-charge control, LED indication, serial communications port	bq2112	PP/5-14
	Capacity monitoring, charge control output, LED indication, serial communications port	bq2114	PP/5-24
	Capacity monitoring and fast charge control	bq2164	PP/5-71
NiCd	Capacity monitoring for high discharge rates, LED indication	bq2111L	PP/5-8
NiCd/NiMH, Lead Acid	Capacity monitoring, LED indication, single-wire serial communications port	bq2113H+	PP/5-20
Li-Ion	Capacity monitoring, Smart Battery data set and interface, LED indication, pack supervision, 4-segment LED indication	bq2148	PP/5-40
	Capacity monitoring, LED indication, serial communications port	bq2150 bq2150/H	PP/5-47 PP/5-53
	Pack supervision: overvoltage, undervoltage, and overcurrent control	bq2158 bq2158T	PP/5-57 PP/5-64
	Capacity monitoring, 3- or 4-cell pack supervision, and LED indication	bq2167+ bq2168+	PP/5-77 PP/5-85
NiCd/NiMH/ Lead Acid/ Li-Ion	Capacity monitoring, Smart Battery data set and interface, 5-segment LED indication	bq2145	PP/5-34
	Capacity monitoring, Smart Battery data set and interface, 4-segment LED indication	bq219XL	PP/5-93
Any	Charge and discharge counting, serial communication port, single-wire interface	bq2118	PP/5-30

+ New Product

Unitrode Lithium Ion Pack-Protection ICs provide reversible overvoltage, undervoltage, and overcurrent protection for lithium ion battery packs.

- ➤ Protects one to four Lithium Ion series cells from overvoltage, undervoltage, and overcurrent
- ➤ User-selectable thresholds mask-programmable by Unitrode
- ➤ Designed for battery-pack integration
  - — Small outline package, minimal external components and space, and low cost

Pack-Protection and Supervisory ICs Selection Guide

Battery Technology	Number of Cells Protected	Protection Types	Key Features	Pins / Package	Part Number	Page Number
Lithium Ion	3 or 4	Overvoltage, overcurrent, and undervoltage	Very low power	16/0.150" SOIC	bq2058	PP/6-2
	2				bq2058T	PP/6-14
		Overcharge, overdischarge, overcurrent	Internal MOSFET (80mΩ total)		UCC3911	PP/6-26
	1		Internal MOSFET (50mΩ total)	16/0.150" TSSOP	UCC3952+	PP/6-32
	3 or 4	Overvoltage, undervoltage, overcurrent	Smart-discharge circuitry	16/0.150" SSOP	UCC3957	PP/6-37
	1	Overcharge, overdischarge, overcurrent	Internal MOSFETS (50mΩ total)	16/0.150" SOIC	UCC3958	PP/6-44

+ New Product

Power-Management ICs Selection Guide

Features	Part Number: UCC3581	UCC3809 -1/2	UCC3800/ 1/2/3/4/5	UCC3813- 0/1/2/3/4/5
Topology	Forward, flyback	Forward, flyback, buck, boost	Forward, flyback, buck, boost	Forward, flyback, buck, boost
Input voltage	Off-line AC	Off-line AC	Off-line AC, battery	Off-line AC, battery
Output voltage	NA	NA	NA	NA
Operating mode	Fixed/variable frequency	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)	Fixed frequency (1MHz maximum)
Output	1A FET drives	0.8A FET drives	1A FET drives	1A FET drives
Output power	N / A	N / A	N / A	N / A
Supply current	300µA	500µA	500µA	500µA
Power limit	Yes	No	Yes	Yes
Application/design note	DN-48, DN-65	DN-65, DN-89, U-165, U-168	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-133A, U-97
Pin count ❖	14	8	8	8
Page number	PS/8-128	PS/8-192	PS/8-169	PS/8-206

❖The smallest available pin count for thru-hole and surface-mount packages.

Power-Management ICs Selection Guide (Continued)

Features	Part Number: UCC39401	UCC3941 -3/-5/-ADJ	UCC39411 /2/3+	UCC39421/2+	UCC3946	UCC3954
Topology	Boost / battery charger	Boost	Boost	Boost/SEPIC/ flyback	Watchdog/ reset	Flyback
Input voltage	0.8V to (V_{OUT} + 0.5V)	0.8V to (V_{OUT} + 0.5V)	1.1V to (V_{OUT} + 0.5V)	1.8V–8V	2.1V–5.5V	2.5V–4.2V
Output voltage	ADJ to 5.0V	3.3V, 5V, ADJ	3.3V, 5V, ADJ	ADJ	V_{IN}–0.3V	3.3V
Operating mode	Variable frequency	Variable frequency	Variable	Fixed/variable frequency	Watchdog/ reset	Fixed frequency (200kHz)
Output	Internal power FETs	Internal power FETs	Internal power FETs	FET Drives	NA	Internal power FETs
Output power	200mW	500mW (1 cell) 1W (2 cells)	200mW	NA	NA	2W
Supply current	55µA	80µA	48µA	635µA	10µA	1mA
Power limit	Yes	Yes	Yes	Yes	NA	Yes
Application/ design note	-	DN-73	DN-97	-	-	DN-86
Pin count ❖	20	8	8	16/20	8	8
Page number	PP/7-34	PP/7-48	PP/7-58	PP/7-66	PP/7-88	PP/7-93

+ New Product
❖The smallest available pin count for thru-hole and surface-mount packages.

Linear Controller ICs Selection Guide

Features	Part Number UC3832	UC3833	UC3834	UC3835	UC3836	UCC3837
Type of output	Positive adjustable	Positive adjustable	Positive/ negative adjustable	5V fixed	Positive adjustable	Positive adjustable
Maximum input voltage	36V	36V	40V	40V	40V	12V
Minimum output voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V	1.5V
Output drive	300mA	300mA	350mA	500mA	500mA	1.5mA
Type of short circuit limit	Duty cycle	Duty cycle	Foldback	Foldback	Foldback	Duty cycle
Reference voltage accuracy	2%	2%	3% / 4%	2%	2%	2%
Special features	Multiple pins accessible	-	-	Built-in Rsense	Built-in Rsense	Internal charge pump; Direct N-FET drive
Application/ design note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95			-
Pin count ❖	14, 16	8, 16	16	8, 16	8, 16	8
Page number	PS/3-11	PS/3-11	PS/3-18	PS/3-24	PS/3-24	PS/3-28

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide

Features	Part Number UCC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V/ adjustable
Dropout voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output voltage accuracy	2.5%	1%	1%	1%	1%
Maximum input voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown current	10µA	-	-	-	-
Operating current	400µA	-	-	-	-
Line regulation	0.01% / V	-	-	-	-
Load regulation	0.1%, I_{OUT} = 0 to 1A	-	-	-	-
Special features	Power limit	Fast transient response	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	8	5	5	5	5
Page number	PP/7-5	PS/3-5	PS/3-5	PS/3-5	PS/3-5

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UCC383	UCC384	UC385-1	UC385-2	UC385-3
Output voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output voltage accuracy	2.5%	2.5%	1%	1%	1%
Maximum input voltage	9V	–16V	7.5V	7.5V	7.5V
Shutdown current	40µA	17µA	-		
Operating current	400µA	240µA	-		
Line regulation	0.01% / V	0.01% / V	-		
Load regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA	-		
Special features	Power limit	Power limit	Fast transient response	Fast transient response	Fast transient response
Pin count ❖	3	8	5	5	5
Page number	PP/7-12	PP/7-19	PS/3-35	PS/3-35	PS/3-35

❖The smallest available pin count for thru-hole and surface-mount packages.

Low-Dropout Linear Regulator ICs Selection Guide (Continued)

Features	Part Number UC385-ADJ	UC386+	UC387+	UC388+
Output voltage	1.2V/adjustable	3.3V	5V	Adjustable down to 1.25V
Dropout voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA
Output voltage accuracy	1%	1.5%	1.5%	1.5%
Maximum input voltage	7.5V	9V	9V	9V
Shutdown current	-	2µA	2µA	2µA
Operating current	-	10µA	10µA	10µA
Line regulation	-	25mV max	25mV max	25mV max
Load regulation	-	10mV max	10mV max	10mV max
Special features	Fast transient response	TSSOP	TSSOP	TSSOP
Pin count ❖	5	8	8	8
Page number	PS/3-35	PP/7-29	PP/7-29	PP/7-29

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Special Function Linear Regulation ICs Selection Guide

Features	Part number UC560	UCC561+	UC563+
Type of output	Positive	Positive	Positive
Application	Source/sink regulator for the 18- and 27-line SCSI termination	LVD SCSI regulator for the 18- and 27-line termination	32-line VME bus bias generator
Input voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V
Output voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V
Dropout voltage	0.9V at 750mA	-	-
Bus standard	SCSI-1,2,3	SPI-2, 3	VME / VME64
Sink/source current	300mA / –750mA	200mA / –200mA	475mA / –575mA
Application/design note	-	-	-
Pin count ❖	5, 8	16	3, 8
Page number	IF/4-3	IF/4-7	IF/4-10

❖The smallest available pin count for thru-hole and surface-mount packages.
+ New product.

Back-Light Controller ICs Selection Guide

Features	Part Number UC3871	UC3872	UCC3972+
Application	Fluorescent lamp driver with LCD Bias	Fluorescent lamp driver	Fluorescent lamp driver
Voltage range	4.5V–20V	4.5V–24V	4.5V–25V
Reference tolerance	1.2%	1.2	NA
Open lamp detect	Yes	Yes	Yes
PWM synchronization	Yes	Yes	Yes
PWM frequency	Programmable	Programmable	80kH–160kH
Analog dimming	Yes	Yes	Yes
Low-frequency dimming	Yes	Yes	Yes
Operating current	8mA	6mA	1mA
Package	18-pin SOIC	16-pin SSOP	8-pin TSSOP
Application/design note	U-141, U-148	DN-75, U-141, U-148	-
Page number	PP/8-2	PP/8-8	PP/8-13

+ New Product

IrDA Selection Guide

Device Type	Supply Voltage	Data Rate	Dynamic Range	Quiescent Current	Encoder/ Decoder	IrDA Compliant	LED Driver	Part Number	Page Number
Receiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	250µA	N	Y	N/A	UCC5341	PP/9-2
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100m A	250µA	N	Y	500mA	UCC5342	PP/9-6
Transceiver	3.3V or 5V	2.4kbps 115.2kbps	150nA 100mA	280µA	Y	Y	500mA	UCC5343	PP/9-10

PWM Control

PWM Control

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3800	UCC3801	UCC3802	UCC3803	UCC3804
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-173	PS/3-173	PS/3-173	PS/3-173	PS/3-173

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3805	UCC3806	UCC3807-1	UCC3807-2	UCC3807-3
Application	DC-DC and Battery	Isolated Output, Push-pull Controller	DC-DC	Off-line	DC-DC and Battery
Topology	Forward, Flyback	Push-pull, Full Bridge, Half Bridge	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1.5%	1%	1.5%	1.5%	1.5%
Peak Output Current	1A	0.5A	1A	1A	1A
Under Voltage Lockout	4.1V / 3.6V	7.5V / 6.75V	7.2V / 6.9V	12.5V / 8.3V	4.3V / 4.1V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y		Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	50% / 50%	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal		Y			
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-45, DN-51, DN-65, U-97, U-110, U-144	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A	DN-48, DN-65, U-97, U-133A
Pin Count ❖	8	16	8	8	8
Page Number	PS/3-173	PS/3-180	PS/3-187	PS/3-187	PS/3-187

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3808-1	UCC3808-2	UCC3809-1	UCC3809-2	UCC3810
Application	Off-line	DC-DC and Battery	DC-DC	Off-line	Dual PWM Controller, Off-line, DC-DC
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	2%	2%	5%	5%	1.5%
Peak Output Current	0.5A Source, 1A Sink	0.5A Source, 1A Sink	0.4A Source, 0.8A Sink	0.4A Source, 0.8A Sink	1A
Under Voltage Lockout	12.5V / 8.3V	4.3V / 4.1V	10V / 8V	15V / 8V	11.3V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual, Totem Pole
Startup Current	130µA	130µA	100µA	100µA	150µA
Leading Edge Blanking					Y
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	50% / 50%	50% / 50%	90%	90%	50%
Separate Oscillator / Synchronization Terminal			N/A	N/A	Y
Application / Design Note	DN-65, U-97, U-110, U-170	DN-65, U-97, U-110, U-170	DN-65, DN-89, U-165, U-168	DN-65, DN-89, U-165, U-168	DN-65, U-97, U-110, U-133A
Pin Count ❖	8	8	8	8	16
Page Number	PS/3-192	PS/3-192	PS/3-198	PS/3-198	PS/3-205

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-0	UCC3813-1	UCC3813-2	UCC3813-3	UCC3813-4
Application	DC-DC and Battery	DC-DC and Battery	Off-line	DC-DC and Battery	Off-line
Topology	Buck, Boost	Buck, Boost	Forward, Flyback	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout	7.2V / 6.9V	9.4V / 7.4V	12.5V / 8.3V	4.1V / 3.6V	12.5V / 8.3V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA	100µA	100µA	100µA	100µA
Leading Edge Blanking	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	50%	100%	100%	50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	DN-42A, DN-48, DN-54, DN-65, DN-89, U-97, U-133A
Pin Count ❖	8	8	8	8	8
Page Number	PS/3-212	PS/3-212	PS/3-212	PS/3-212	PS/3-212

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3813-5	UC3823	UC3823A	UC3823B	UC3824
Application	DC-DC and Battery	DC-DC	DC-DC	Off-line	Synchronous Rectifier, Forward Converter
Topology	Forward, Flyback	Buck, Boost	Buck, Boost	Buck, Boost	Forward, Flyback
Voltage Reference Tolerance	1.5%	1%	1%	1%	1%
Peak Output Current	1A	1.5A	2A	2A	1.5A
Under Voltage Lockout	4.1V / 3.6V	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	9.2V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Complementary, Totem Pole
Startup Current	100µA	1.1mA	0.1mA	0.1mA	1.1mA
Leading Edge Blanking	Y		Y	Y	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50%	100%	Programmable, <100%	Programmable, <100%	100%
Separate Oscillator / Synchronization Terminal		Y	Y	Y	Y
Application / Design Note	DN-42A, DN-43, DN-46, DN-48, DN-54, DN-56A, DN-65, DN-89, U-97, U-133A	U-97, U-111, U-131	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-111
Pin Count ❖	8	16	16	16	16
Page Number	PS/3-212	PS/3-219	PS/3-225	PS/3-225	PS/3-233

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3825	UC3825A	UC3825B	UC3826❍	UC3827-1
Application	DC-DC	DC-DC	Off-line	Secondary Side, Average Current Mode	Multiple Output or High Voltage Output DC-DC Converters
Topology	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Push-pull, Full Bridge, Half Bridge	Forward, Flyback, Buck, Boost	Buck Current Fed Push-pull
Voltage Reference Tolerance	1%	1%	1%	1%	4%
Peak Output Current	1.5A	2A	2A	0.25A	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers
Under Voltage Lockout	9.2V / 8.4V	9.2V / 8.4V	16V / 10V	8.4V / 8.0V	9V / 8.4V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Floating Buck, Push-pull
Startup Current	1.1mA	0.1mA	0.1mA		1mA
Leading Edge Blanking		Y	Y	N/A	
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable, <50%	Programmable, <50%	90% for Buck Stage, 50% / 50% for Push-pull Stage
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	U-97, U-110, U-111	U-97, U-110, U-111, U-128, U-131	U-97, U-110, U-111, U-128, U-131	U-135, U-140	
Pin Count ❖	16	16	16	24	24
Page Number	PS/3-240	PS/3-225	PS/3-225	PS/3-247	PS/3-257

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3827-2	UCC3830-4	UCC3830-5	UCC3830-6	UCC3839❍
Application	Multiple Output or High Voltage Output DC-DC Converters	Microprocessor Power	Microprocessor Power	Microprocessor Power	Secondary Side, Average Current Mode Control
Topology	Buck Voltage Fed Push-pull	Buck	Buck	Buck	Any Topology
Voltage Reference Tolerance	4%	1%*	1%*	1%*	1%
Peak Output Current	Floating 1A for Buck Stage, 0.8A for Push-pull Drivers	1.5A	1.5A	1.5A	10mA to Drive Opto-coupler
Under Voltage Lockout	9V / 8.4V	10.5V / 10V	10.5V / 10V	10.5V / 10V	
Maximum Practical Operating Frequency	500kHz	100kHz	200kHz	400kHz	1MHz
Outputs	Floating Buck, Push-pull	Single	Single	Single	Opto-coupler Drive
Startup Current	1mA				
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	90% for Buck Stage, 50% / 50% for Push-pull Stage	95%	95%	95%	
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note					U-140
Pin Count ❖	24	20	20	20	14
Page Number	PS/3-257	PS/3-263	PS/3-263	PS/3-263	PS/3-276

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3841	UC3842	UC3842A	UC3843	UC3843A
Application	Primary Side, Programmable, Off-line, DC-DC	Off-line	Off-line	DC-DC	DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Under Voltage Lockout		16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Open Collector	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	4.5mA	1mA	0.5mA	1mA	0.5mA
Leading Edge Blanking					
Soft Start	Y				
Maximum Duty Cycle	Programmable	100%	100%	100%	100%
Separate Oscillator / Synchronization Terminal					
Special Features			Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current
Application / Design Note	DN-28	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111
Pin Count ❖	18	8, 14	8, 14	8, 14	8, 14
Page Number	PS/3-281	PS/3-289	PS/3-296	PS/3-289	PS/3-296

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3844	UC3844A	UC3845	UC3845A	UC3846
Application	Off-line	Off-line	DC-DC	DC-DC	Off-line, DC-DC
Topology	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Forward, Flyback Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	0.5A
Under Voltage Lockout	16V / 10V	16V / 10V	8.4V / 7.6V	8.5V / 7.9V	7.7V / 6.95V
Maximum Practical Operating Frequency	500kHz	500kHz	500kHz	500kHz	500kHz
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	1mA	0.5mA	1mA	0.5mA	
Leading Edge Blanking					
Soft Start					Y
Maximum Duty Cycle	50%	50%	50%	50%	50% / 50%
Separate Oscillator / Synchronization Terminal					Y
Special Features		Trimmed Oscillator Discharge Current		Trimmed Oscillator Discharge Current	
Application / Design Note	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-27, DN-40, DN-89, U-100A, U-111	DN-26, DN-27, DN-29, DN-30, DN-40, DN-89, U-100A, U-111	DN-45, U-93, U-97, U-100A, U-111
Pin Count ❖	8, 14	8, 14	8, 14	8, 14	16
Page Number	PS/3-289	PS/3-296	PS/3-289	PS/3-296	PS/3-302

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3847	UC3848❍	UC3849❍	UC3851	UC3856
Application	Off-line, DC-DC	Average Current Mode, Off-line, DC-DC	Secondary Side, Average Current Mode	Off-line, Programmable, Primary Side Controller	Isolated Output, Push-pull Controller
Topology	Push-pull, Full Bridge, Half Bridge	Forward, Flyback	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Push-pull, Full Bridge, Half Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	0.5A	2A	0.25A	0.2A	1.5A
Under Voltage Lockout	7.7V / 6.95V	13V / 10V	8.3V / 7.9V		7.7V / 7.0V
Maximum Practical Operating Frequency	500kHz	1MHz	1MHz	500kHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current		500µA		4.5mA	
Leading Edge Blanking		N/A	N/A	Y	
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	50% / 50%	Programmable	Programmable	50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y		Y		Y
Application / Design Note	DN-45, U-93, U-97, U-100A, U-111	U-135, U-140	U-135, U-140	DN-28	DN-45, U-93, U-97, U-110
Pin Count ❖	16	16	24	18	16
Page Number	PS/3-302	PS/3-309	PS/3-317	PS/3-327	PS/3-333

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UCC3880-4	UCC3880-5	UCC3880-6	UCC3882	UCC3884
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power	Off-Line or DC-DC Frequency Foldback Controller
Topology	Buck	Buck	Buck	Synchronous Buck	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%*	1%*	1%*	1%*	2%
Peak Output Current	1.5A	1.5A	1.5A	1.5A	0.5A Source, 1A Sink
Under Voltage Lockout	10.5V / 10V	10.5V / 10V	10.5V / 10V	10.5V / 10V	8.9V / 8.3V
Maximum Practical Operating Frequency	100kHz	200kHz	400kHz	700kHz	750kHz
Outputs	Single	Single		Dual, N-FET Drive	Single
Startup Current					200µA
Leading Edge Blanking					
Average Current Mode	Y	Y		Y	
Foldback Current Limiting	Y	Y		Y	
Soft Start					Y
Maximum Duty Cycle	95%	95%		95%	80%
Separate Oscillator / Synchronization Terminal					Y
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	
Application / Design Note	U-140	U-140	U-140	U-140	DN-65, U-164
Pin Count ❖	24	18	16	28	16
Page Number	PS/3-373	PS/3-373	PS/3-373	PS/3-380	PS/3-393

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

Current Mode Controllers	UNITRODE PART NUMBER				
	UC3886				
Application	Microprocessor Power				
Topology	Buck				
Voltage Reference Tolerance	1.5%				
Peak Output Current	1.5A				
Under Voltage Lockout	10.3V / 10.05V				
Maximum Practical Operating Frequency	400kHz				
Outputs	Single				
Startup Current					
Leading Edge Blanking					
Average Current Mode					
Foldback Current Limiting					
Soft Start					
Maximum Duty Cycle	95%				
Separate Oscillator / Synchronization Terminal					
Special Features	External Reference Input, Use with UC3910				
Application / Design Note	U-140, U-156, U-157				
Pin Count ❖	16				
Page Number	PS/3-400				

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UC2577-12	UC2577-15	UC2577-ADJ
Description	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator	Simple Step-up Voltage Regulator
Application	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications	3A Step-up Switching Regulator for Boost, Flyback, and Forward Converter Applications
Output Voltage	12V	15V	Adjustable
Special Features	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available	•Circuit Requires Few External Components •NPN Output Switches 3A •Current Mode Operation for Improved Response •Fixed and Adjustable Output Versions Available
Application / Design Note	DN-47, DN-49	DN-47, DN-49	DN-49
Pin Count ❖	5	5	5
Page Number	PS/3-31	PS/3-31	PS/3-36

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER				
	UC3572	UC3573	UC3578	UCC3585+	
Application	Low Power, High Efficiency, Spot Regulator	Low Power, High Efficiency, Spot Regulator	DC-DC	Low Input Voltage Synchronous Buck Regulator with Output Voltage Tracking	
Topology	Negative Output Flyback	Buck	Buck	Voltage Mode Synchronous Buck	
Voltage Reference Tolerance	2%	2%	2%	1%	
Peak Output Current	0.5A	0.5A	0.6A Source, 0.8A Sink	0.5A	
Maximum Practical Operating Frequency	300kHz	300kHz	100kHz Internal Oscillator	700kHz	
Outputs	Single, Totem Pole	Single, Totem Pole	Single, Floating Totem Pole	P FET/N FET Synchronous	
Startup Current			N/A	2.3mA	
Voltage Feedforward				N	
Soft Start			Y	Y	
Maximum Duty Cycle	100%	100%	90%	100%	
Separate Oscillator / Synchronization Terminal				N	
Application / Design Note		DN-70	U-167		
Pin Count ❖	8	8	16	16	
Page Number	PS/3-108	PS/3-112	PS/3-116	PS/3-154	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39401+	UCC3941	UCC39411/2/3+
Description	Low Voltage Boost Controller / Charger	1V Synchronous Boost Converter	1V Low Power Boost Controller
Application	Pager Power	High Efficiency Integrated Boost Converter	High Efficiency Low Power Synchronous Boost Conversion
Special Features	•High Efficiency Boost •1V Input •Battery Charger •Backup LDO	•Full Load Startup at 1V •Power Limit Control •Auxiliary 9V Supply •Output Disconnect •Shutdown Mode	•200mW Output Power with Battery Voltages as low as 0.8V •Power Limit Control •Adaptive Current Mode Control •Auxiliary 7V Supply •Shutdown Mode
Application / Design Note			
Pin Count ❖	20	8	8
Page Number	PP/7-34	PP/7-45	PP/7-58

Dedicated DC/DC Controllers	UNITRODE PART NUMBER		
	UCC39421/2+	UCC3954	
Description	Multimode HF PWM Controller	Single Cell Lithium-Ion to 3.3V Converter	
Application	High Efficiency Boost, Sepic Flyback Converter	High Efficiency Flyback Converter	
Special Features	•2mHz Operation •1.8V Input •Current Limit •Power-on Reset •Low Voltage Detect	•Fixed 3.3V Output •750mA Output Current •Low Battery Warning •Low Battery Disconnect •Shutdown Mode	
Application / Design Note			
Pin Count ❖	16, 20	8	
Page Number	PP/7-66	PP/7-93	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3588+	UCC3830-4	UCC3830-5	UCC3830-6	UCC3880-4
Application	Synchronous Buck Regulator with 5 Bit DAC	Microprocessor Power	Microprocessor Power	Microprocessor Power	Microprocessor Power
Topology	Voltage Mode Synchronous Buck	Buck	Buck	Buck	Buck
Voltage Reference Tolerance	1%	1%*	1%*	1%*	1%*
Peak Output Current	1A	1.5A	1.5A	1.5A	1.5A
Maximum Practical Operating Frequency	700kHz	100kHz	200kHz	400kHz	100kHz
Outputs	Dual NFET Synchronous	Single	Single	Single	Single
Soft Start	Y				
Average Current Mode		Y	Y	Y	Y
Foldback Current Limiting		Y	Y	Y	Y
Maximum Duty Cycle	100%	95%	95%	95%	95%
Special Features		5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor
Application / Design Note					U-140
Pin Count ❖	16	20	20	20	20
Page Number	PS/3-163	PS/3-263	PS/3-263	PS/3-263	PS/3-373

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Controllers	UNITRODE PART NUMBER				
	UCC3880-5	UCC3880-6	UCC3882		
Application	Microprocessor Power	Microprocessor Power	Microprocessor Power		
Topology	Buck	Buck	Synchronous Buck		
Voltage Reference Tolerance	1%*	1%*	1%*		
Peak Output Current	1.5A	1.5A	1.5A		
Maximum Practical Operating Frequency	200kHz	400kHz	700kHz		
Outputs	Single	Single	Dual, N-FET Drive		
Soft Start					
Average Current Mode	Y	Y	Y		
Foldback Current Limiting	Y	Y	Y		
Maximum Duty Cycle	95%	95%	95%		
Special Features	4 Bit Programmable Output Voltage, UV/OV Monitor	4 Bit Programmable Output Voltage, UV/OV Monitor	5 Bit Programmable Output Voltage, UV/OV Monitor		
Application / Design Note	U-140	U-140	U-140		
Pin Count ❖	20	20	28		
Page Number	PS/3-373	PS/3-373	PS/3-380		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
**** Combined Reference, DAC, and Error Amplifier Tolerance.***
+ New Product

PWM Control (cont.)

MicroProcessor Power Support	UNITRODE PART NUMBER		
	UCC391+	UC3910	UCC3946
Description	5-Bit DAC 5V Operation	Reference, 4-bit DAC and Fault Monitor	Microprocessor Supervisor with Watchdog Timer
Application	Sets Control Voltage for UC3886 and other Precision PWMs	Sets Control Voltage for UC3886, UC3870 and other Precision PWMS	Accurate Microprocessor Supervision
Special Features	•5V Operation •1% Combined Reference and DAC Tolerance •Meets VID Code for Pentium II Processors	•4-bit DAC Sets Output Voltage of PWM, Meets Intel VID Code •1% Combined Reference and DAC Tolerance •Over and Under Voltage Monitoring and Protection	•Programmable Reset Period •Programmable Watchdog Period •1.5% Accurate Threshold •4mA IDD
Application / Design Note		U-157, U-158	
Pin Count ❖	8	16	8
Page Number	PS/3-434	PS/3-437	PP/7-88

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Post Regulation Controllers	UNITRODE PART NUMBER				
	UCC3583	UC3584	UC3838A		
Application	Secondary Side Post Regulation	DC-DC Secondary Side Synchronous Post Regulator	Mag-Amp Controller		
Topology	Buck	Buck			
Voltage Reference Tolerance	1.5%	1%	1%		
Peak Output Current	1.5A Source, 0.5A Sink	1.5A Source and Sink	120mA Reset Current		
Maximum Practical Operating Frequency	500kHz	1MHz			
Undervoltage Lockout	9.0V / 8.4V	10.5V / 8.8V	N/A		
Outputs	Single, Totem Pole	Single, Totem Pole			
Startup Current	100µA	N/A			
Voltage Feedforward	N/A				
Soft Start	Y	Y			
Maximum Duty Cycle	95%	94%			
Separate Oscillator / Synchronization Terminal	Y	Y			
Special Features	• For Both Single Ended and Center Tapped Secondary Circuits • Operation From Floating Supply Referenced to Output	• Can Use Existing Windings • Internally Regulated 15V Boost Supply Bias for Low Voltage Applications • Short Circuit Protection with Programmable Delay	• Dual Op-Amps • –120V Reset Driver		
Application / Design Note	DN-64	DN-64, DN-83	DN-47		
Pin Count ❖	14	16	16, 20		
Page Number	PS/3-139	PS/3-148	PS/3-272		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Secondary Side PWM Control	UNITRODE PART NUMBER				
	UC3826	UCC3839❍	UC3849❍	UCC3960+	UCC3961+
Application	Secondary Side, Average Current Mode	Secondary Side, Average Current Mode Control	Secondary Side, Average Current Mode	Primary-Side Startup Control	Primary-Side Startup Control
Topology	Forward, Flyback, Buck, Boost	Any Topology	Forward, Flyback, Buck, Boost		
Voltage Reference Tolerance	1%	1%	1%	5%	5%
Peak Output Current	0.25A	10mA to Drive Opto-coupler	0.25A	1.5A	1.5A
Undervoltage Lockout	8.4V / 8V		8.3V / 7.9V	10V / 8V	10V / 8V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	400kHz Synchronizable Switching Frequency	400kHz Synchronizable Switching Frequency
Outputs	Single, Totem Pole	Opto-coupler Drive	Single, Totem Pole	Single	Single
Startup Current				150µA	150µA
Leading Edge Blanking	N/A		N/A	N/A	N/A
Soft Start	Y		Y	Y	Y
Maximum Duty Cycle	Programmable		Programmable		Programable V-S Clamp
Separate Oscillator / Synchronization Terminal	Y		Y		
Special Features					• Multimode OVC Protection, • Programable OV and UV, • Self Bias Regulation.
Application / Design Note	U-135, U-140	U-140	U-135, U-140	DN-99	DN-99
Pin Count ❖	24	14	24	8	14
Page Number	PS/3-247	PS/3-276	PS/3-317	PS/3-442	PS/3-450

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
❍ Pulse- by-Pulse Current Limiting Not Applicable.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★	UC3860
Application	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Off-line, DC-DC, Zero Current Switching
Topology	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1.5%	1.5%	1.5%	1.5%	1%
Peak Output Current	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A	2A
Undervoltage Lockout	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V	17.3V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	2MHz
Outputs	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2	Dual Programmable, Totem Pole
Startup Current	50µA	50µA	50µA	50µA	300µA
Voltage Feedforward	Y	Y	Y	Y	
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	Programmable	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-65	DN-65	DN-65	DN-65	
Pin Count ❖	16	16	16	16	24, 28
Page Number	PS/3-122	PS/3-122	PS/3-122	PS/3-122	PS/3-341

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3861	UC3862	UC3863	UC3864	UC3865
Application	Off-line, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	DC-DC and Battery, Zero Voltage Switching	Off-line, Zero Current Switching
Topology	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Half Bridge, Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	1A	1A
Undervoltage Lockout	16.5V / 10.5V	16.5V / 10.5V	8V / 7V	8V / 7V	16.5V / 10.5V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Dual Alternating, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle	50% / 50%	100%	50% / 50%	100%	50% / 50%
Separate Oscillator / Synchronization Terminal					
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138	U-122, U-138
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-349	PS/3-349

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3866	UC3867	UC3868	UC3875	UC3876
Application	Off-line, Zero Current Switching	DC-DC and Battery, Zero Current Switching	DC-DC and Battery, Zero Current Switching	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge
Topology	Forward, Flyback	Half Bridge, Full Bridge	Forward, Flyback	Full Bridge	Full Bridge
Voltage Reference Tolerance	1%	1%	1%	1%	1%
Peak Output Current	1A	1A	1A	2A	2A
Undervoltage Lockout	16.5V / 10.5V	8V / 7V	8V / 7V	10.75V / 9.5V	15.25V / 9.25V
Maximum Practical Operating Frequency	1MHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole
Startup Current	150µA	150µA	150µA	150µA	150µA
Soft Start				Y	Y
Maximum Duty Cycle	100%	50% / 50%	100%	100%	100%
Separate Oscillator / Synchronization Terminal				Y	Y
Application / Design Note	U-122, U-138	U-122, U-138	U-122, U-138	DN-63, U-111, U-136A	DN-63, U-111, U-136A
Pin Count ❖	16	16	16	20, 28	20, 28
Page Number	PS/3-349	PS/3-349	PS/3-349	PS/3-357	PS/3-357

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Soft Switching Controllers	UNITRODE PART NUMBER				
	UC3877	UC3878	UC3879	UCC3895+	
Application	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase Shifted Bridge	Zero Voltage Transition, Phase, Shifted Bridge	
Topology	Full Bridge	Full Bridge	Full Bridge	Full Bridge	
Voltage Reference Tolerance	1%	1%	1%	1%	
Peak Output Current	2A	2A	0.1A	0.1A	
Undervoltage Lockout	10.75V / 9.5V	15.25V / 9.25V	Selectable 10.75V / 9.5V, 15.25V / 9.25V	11V / 9V	
Maximum Practical Operating Frequency	1MHz	1MHz	300kHz	1MHz	
Outputs	Quad, Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad Phase Shifted, Totem Pole	Quad, Phase Shifted, Totem Pole	
Startup Current	150µA	150µA	150µA	150µA	
Leading Edge Blanking					
Soft Start	Y	Y	Y	Y	
Maximum Duty Cycle	100%	100%	100%	100%	
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	
Application / Design Note	DN-63, U-111, U-136A	DN-63, U-111, U-136A	DN-63, U-111, U-136A, U-154	DN-63, U-136A	
Pin Count ❖	20, 28	20, 28	20	20	
Page Number	PS/3-357	PS/3-357	PS/3-367	PS/3-425	

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3524✣	UC3524A	UC3525A	UC3525B	UC3526
Application	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC
Topology	Forward, Flyback, Buck, Boost	Forward, Flyback, Buck, Boost	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge
Voltage Reference Tolerance	4%	1%	1%	0.75%	1%
Peak Output Current	100mA	200mA	400mA	200mA	100mA
Undervoltage Lockout		7.5V / 7V	7V	7V	Y
Maximum Practical Operating Frequency	300kHz	500kHz	500kHz	500kHz	400kHz
Outputs	Dual Alternating, Uncommitted	Dual Alternating, Uncommitted	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole
Startup Current		4mA			
Voltage Feedforward					
Soft Start			Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	50% / 50%	50% / 50%
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note			DN-36	DN-36	
Pin Count ❖	16	16	16	16	16
Page Number	PS/3-43	PS/3-48	PS/3-54	PS/3-61	PS/3-68

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC3526A	UC3527A	UC3527B	UC3548	UCC3570
Application	Fixed Frequency PWM Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Fixed Frequency PWM, Off-line, DC-DC	Off-line, DC-DC	Wide Range, Off-line
Topology	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Full Bridge, Half Bridge	Flyback, Forward	Forward, Flyback, Buck, Boost
Voltage Reference Tolerance	1%	1%	0.75%	1%	1%
Peak Output Current	100mA	400mA	200mA	2A	500mA
Undervoltage Lockout	Y	7V	7V	13V / 10V	13V / 9V
Maximum Practical Operating Frequency	550kHz	500kHz	500kHz	1MHz	500kHz
Outputs	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Dual Alternating, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current				500µA	85µA
Voltage Feedforward				Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	50% / 50%	50% / 50%	50% / 50%	Programmable	100%
Separate Oscillator / Synchronization Terminal	Y	Y	Y		
Application / Design Note		DN-36	DN-36		DN-48, DN-62, DN-65, U-150
Pin Count ❖	18	16	16	16	14
Page Number	PS/3-75	PS/3-54	PS/3-61	PS/3-83	PS/3-91

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC35701+	UCC3580-1★	UCC3580-2★	UCC3580-3★	UCC3580-4★
Application	Wide Range DC-DC and Off-line	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM	Active Clamp / Reset PWM
Topology	Forward, Flyback, Buck and Boost	Forward, Flyback	Forward, Flyback	Forward, Flyback	Forward, Flyback
Voltage Reference Tolerance	1%	1.5%	1.5%	1.5%	1.5%
Peak Output Current	1.2A	1A / 0.5A	1A / 0.5A	1A / 0.5A	1A / 0.5A
Undervoltage Lockout	13V / 9V	9V / 8.5V	15V / 8.5V	9V / 8.5V	15V / 8.5V
Maximum Practical Operating Frequency	700kHz	1MHz	1MHz	1MHz	1MHz
Outputs	Single, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole	Dual Complementary, Totem Pole, Inverted Out2	Dual Complementary, Totem Pole, Inverted Out2
Startup Current	130µA	50µA	50µA	50µA	50µA
Voltage Feedforward	Y	Y	Y	Y	Y
Soft Start	Y	Y	Y	Y	Y
Maximum Duty Cycle	100%	Programmable	Programmable	Programmable	Programmable
Separate Oscillator / Synchronization Terminal	Y	Y	Y	Y	Y
Application / Design Note	DN-48, DN-62, DN-65, U-150	DN-65	DN-65	DN-65	DN-65
Pin Count ❖	14	16	16	16	16
Page Number	PS/3-99	PS/3-122	PS/3-122	PS/3-122	PS/3-122

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
★ Does Not Feature Current Limiting.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UCC3581	UCC3588+	UCC3888	UCC3889	UCC3890
Application	Off-line, Primary Side PWM for ISDN Applications	Synchronous Buck Regulator with 5 Bit DAC	Off-line Power Supply Controller	Off-line Power Supply Controller	Off-line Battery Charge Controller
Topology	Forward, Flyback	Voltage Mode Synchronous Buck	Flyback	Flyback	Flyback
Voltage Reference Tolerance	1.5%	1%	3%	3%	4%
Peak Output Current	1A	1A	0.15A	0.15A	0.15A
Undervoltage Lockout	7.3V / 6.8V	10.5V / 10V	8.4V / 6.3V	8.4V / 6.3V	8.6V / 6.3V
Maximum Practical Operating Frequency	100kHz	700kHz	250kHz	250kHz	250kHz
Outputs	Single, Totem Pole	Dual NFET Synchronous	Single, Totem Pole	Single, Totem Pole	Single, Totem Pole
Startup Current	100µA		150µA	150µA	
Voltage Feedforward			Y	Y	Y
Soft Start	Y	Y			
Maximum Duty Cycle	Programmable	100%	55%	55%	N/A
Separate Oscillator / Synchronization Terminal	Y				
Application / Design Note	DN-48, DN65		DN-59A, U-149A	DN-59A, DN-65, U-149A	
Pin Count ❖	14	16	8	8	8
Page Number	PS/3-131	PS/3-163	PS/3-407	PS/3-412	PS/3-418

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

PWM Control (cont.)

Voltage Mode Controllers	UNITRODE PART NUMBER				
	UC494A/AC	UC495A/AC			
Application	DC-DC	DC-DC			
Topology	Buck, Boost, Push-Pull, Half Bridge	Buck, Boost, Push-Pull, Half Bridge			
Voltage Reference Tolerance	1%	1%			
Peak Output Current	200mA	200mA			
Undervoltage Lockout	5V / 4.7V	5V / 4.7V			
Maximum Practical Operating Frequency					
Outputs	Dual Floating	Dual Floating			
Startup Current	6mA	6mA			
Voltage Feedforward					
Soft Start					
Maximum Duty Cycle					
Separate Oscillator / Synchronization Terminal					
Special Features		On Chip 39V Zener			
Application / Design Note	DN-38	DN-38			
Pin Count ❖	16	18			
Page Number	PS/3-460	PS/3-460			

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC3817+	UCC3818+	UCC38500+	UCC38501+	UCC38502+
Soft Switching					
Maximum Practical Operating Frequency	250kHz	250kHz	250kHz	250kHz	250kHz
Current Error Amplifier Bandwidth	3MHz	3MHz	3MHz	3MHz	3MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1A	1A	1A	1A
Startup Current	0.1A	0.1A	0.1A	0.1A	0.1A
Undervoltage Lockout	16V / 10V	10.5V / 10V	16V / 10V	10.5V / 10V	16V / 10V
UVLO 2 Hysteresis			1.2V (300V Turn-off)	1.2V (300V Turn-off)	3V (200V Turn-off)
Overvoltage Protection	Y	Y	Y	Y	Y
Enable Input	Y (with OVP)	Y	Y	Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)	Y (Simplified)
Special Features			DC / DC Controller Included	DC / DC Controller Included	DC / DC Controller Included
Application / Design Note	DN-39E	DN-39E	DN-39E		
Pin Count ❖	16	16	20	20	20
Page Number	PS/4-5	PS/4-5	PS/4-15	PS/4-15	PS/4-15

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UC3854B	UC3855A	UC3855B	UCC3857	UCC3858
Soft Switching		ZVT	ZVT	ZCT	
Maximum Practical Operating Frequency	200kHz	500kHz	500kHz	500kHz	500kHz
Current Error Amplifier Bandwidth	5MHz	5MHz	5MHz	5MHz	5MHz
Average Current Mode	Y	Y	Y	Y	Y
Worldwide AC Input Voltage Operation	Y	Y	Y	Y	Y
Output Drive	1A	1.5A	1.5A	1A	0.5A
Startup Current	0.3mA	0.15mA	0.15mA	0.06mA	0.1mA
Undervoltage Lockout	10.5V / 10V	16V / 10V	10.5V / 10V	13.8V / 10V	13.8V / 10V
Overvoltage Protection		Y	Y		Y
Enable Input	Y	Y	Y		Y
Multiplier / Divider Feedforward	Y	Y	Y	Y (Faster Response)	Y (Faster Response)
Special Features		Current Synthesizer	Current Synthesizer	Single Stage Isolated Output	Improved Efficiency at Light Load
Application / Design Note	DN-39E, DN-44, DN-66	DN-39E, DN-66, U-153	DN-39E, DN-66, U-153	DN-39E	DN-39E, DN-90
Pin Count ❖	16	20	20	20	16
Page Number	PS/4-42	PS/4-48	PS/4-48	PS/4-56	PS/4-65

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Factor Correction (cont.)

Power Factor Correction Products	UNITRODE PART NUMBER				
	UCC38503+	UC3852	UC3853	UC3854	UC3854A
Soft Switching		ZCT			
Maximum Practical Operating Frequency	250kHz	Variable	125kHz	200kHz	200kHz
Current Error Amplifier Bandwidth	3MHz	N/A	1MHz	800kHz	5MHz
Average Current Mode	Y		Y	Y	Y
Worldwide AC Input Voltage Operation	Y		Y	Y	Y
Output Drive	1A	0.5A	1A	1A	1A
Startup Current	0.1A	1mA	0.25mA	1.5mA	0.3mA
Undervoltage Lockout	10.5V / 10V	16.3V / 11.5V	11.5V / 9.5V	16V / 10V	16V / 10V
UVLO 2 Hysteresis	3V (200V Turn-off)				
Overvoltage Protection	Y		Y		
Enable Input	Y			Y	Y
Multiplier / Divider Feedforward	Y (Simplified)	N/A	Y	Y	Y
Special Features	DC / DC Controller Included				
Application / Design Note		DN-39E, U-132	DN-39E, DN-77, DN-78, U-159	DN-39E, DN-41, U-134	DN-39E, DN-44, DN-66
Pin Count ❖	20	8	8	16	16
Page Number	PS/4-15	PS/4-22	PS/4-27	PS/4-32	PS/4-42

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation

Linear Regulation

Linear Controllers	UNITRODE PART NUMBER				
	UC3832	UC3833	UC3834	UC3835	UC3836
Type of Output	Positive Adjustable	Positive Adjustable	Positive / Negative Adjustable	5V Fixed	Positive Adjustable
Maximum Input Voltage	36V	36V	40V	40V	40V
Minimum Output Voltage	2.0V	2.0V	+1.5V / –2.0V		2.5V
Output Drive	300mA	300mA	350mA	500mA	500mA
Type of Short Circuit Limit	Duty Cycle	Duty Cycle	Foldback	Foldback	Foldback
Reference Voltage Accuracy	2%	2%	3% / 4%	2%	2%
Special Features	Multiple Pins Accessible	8 Pin Package		Built in Rsense	Built in Rsense
Application / Design Note	DN-32, DN-61, U-152	DN-32, DN-61, U-152	U-95		
Pin Count ❖	14, 16	8, 16	16	8, 16	8, 16
Page Number	PS/5-11	PS/5-11	PS/5-18	PS/5-24	PS/5-24

Linear Controllers	UNITRODE PART NUMBER				
	UCC3837				
Type of Output	Positive Adjustable				
Maximum Input Voltage	12V				
Minimum Output Voltage	1.5V				
Output Drive	1.5mA				
Type of Short Circuit Limit	Duty Cycle				
Reference Voltage Accuracy	2%				
Special Features	• Internal Charge Pump • Direct N-FET Drive				
Application / Design Note					
Pin Count ❖	8				
Page Number	PS/5-28				

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC381	UC382-1	UC382-2	UC382-3	UC382-ADJ
Output Voltage	3.3V, 5V, ADJ	1.5V	2.1V	2.5V	1.2V / Adjustable
Dropout Voltage	0.5V at 1A	450mV at 3A	450mV at 3A	450mV at 3A	450mV at 3A
Output Voltage Accuracy	2.5%	1%	1%	1%	1%
Maximum Input Voltage	9V	7.5V	7.5V	7.5V	7.5V
Shutdown Current	10µA				
Operating Current	400µA				
Line Regulation	0.01% / V				
Load Regulation	0.1%, I_{OUT} = 0 to 1A				
Special Features	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count ❖	8	5	5	5	5
Page Number	PP/7-5	PS/5-5	PS/5-5	PS/5-5	PS/5-5

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC383	UC384	UC385-1	UC385-2	UC385-3
Output Voltage	3.3V, 5V, ADJ	5V, 12V, ADJ	1.5V	2.1V	2.5V
Dropout Voltage	0.45V at 3A	0.2V at 500mA	450mV at 5A	450mV at 5A	450mV at 5A
Output Voltage Accuracy	2.5%	2.5%	1%	1%	1%
Maximum Input Voltage	9V	−16V	7.5V	7.5V	7.5V
Shutdown Current	40µA	17µA			
Operating Current	400µA	240µA			
Line Regulation	0.01% / V	0.01% / V			
Load Regulation	0.1%, I_{OUT} = 0 to 1A	0.1%, I_{OUT} = 0 to 500mA			
Special Features	Power Limit	Power Limit	Fast Transient Response	Fast Transient Response	Fast Transient Response
Pin Count ❖	3	8	5	5	5
Page Number	PP/7-12	PP/7-19	PS/5-35	PS/5-35	PS/5-35

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Linear Regulation (cont.)

Low Dropout Linear Regulators	UNITRODE PART NUMBER				
	UC385-ADJ	UC386+	UC387+	UC388+	
Output Voltage	1.2V / Adjustable	3.3V	5V	Adjustable down to 1.25V	
Dropout Voltage	450mV at 5A	0.2V at 200mA	0.2V at 200mA	0.2V at 200mA	
Output Voltage Accuracy	1%	1.5%	1.5%	1.5%	
Maximum Input Voltage	7.5V	9V	9V	9V	
Shutdown Current		2µA	2µA	2µA	
Operating Current		10µA	10µA	10µA	
Line Regulation		25mV max	25mV max	25mV max	
Load Regulation		10mV max	10mV max	10mV max	
Special Features	Fast Transient Response	TSSOP	TSSOP	TSSOP	
Pin Count ❖	5	8	8	8	
Page Number	PS/5-35	PP/7-29	PP/7-29	PP/7-29	

Special Functions Linear Regulators	UNITRODE PART NUMBER				
	UC560	UCC561+	UC563+		
Type of Output	Positive	Positive	Positive		
Application	Source / Sink Regulator for the 18 and 27 Line SCSI Termination	LVD SCSI Regulator for the 18 and 27 Line Termination	32 Line VME Bus Bias Generator		
Input Voltage	4V-6V	2.7V- 5.25V	4.875V-5.25V		
Output Voltage	2.85V	1.3V, 1.75V, 0.75V	2.94V		
Dropout Voltage	0.9V at 750mA				
Bus Standard	SCSI-1,2,3	SPI-2, 3	VME / VME64		
Sink / Source Current	300mA / –750mA	200mA / –200mA	475mA / –575mA		
Application / Design Note					
Pin Count ❖	5, 8	16	3, 8		
Page Number	IF/4-3	IF/4-7	IF/4-10		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers

Power and FET Drivers	UNITRODE PART NUMBER				
	L293/D	UC2950	UC3702	UC3705	UC3706
Power Driver	Quad	Single		Single	Dual
FET Driver					
Isolated Driver Pairs					
Relay Drivers			Quad		
Output Configuration	Non-Inverting	Sink / Source TTL	Non-Inverting	Complementary	Complementary
Enable					
Inhibit	Y		Y		Y
Analog Stop					Y
Output Rise Time	250ns			60ns	60ns
Maximum Voltage	36V	35V	42.5V	40V	40V
Peak Output Current	2.0A / 1.2A	4.0A	50mA per Relay	1.5A	1.5A
Application / Design Note				U-111, U-118, U-137	U-111, U-118, U-137
Pin Count ❖	16, 28	5	16	5, 8	16
Page Number	PS/6-5	PS/6-10	PS/6-12	PS/6-16	PS/6-19

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3707	UC3708	UC3709	UC3710	UC3711
Power Driver	Dual	Dual			
FET Driver			Single	Single	Dual
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Complementary	Non-Inverting	Non-Inverting	Complementary	Non-Inverting
Enable		Y			
Inhibit	Y				
Analog Stop	Y				
Output Rise Time	50ns	75ns	40ns	40ns	20ns
Maximum Voltage	40V	35V	40V	20V	40V
Peak Output Current	1.5A	3.0A	1.5A	6.0A	1.5A
Application / Design Note	U-111, U-118, U-137	DN-35, U-111, U-137	U-111, DN-118, U-137	U-111	U-111
Pin Count ❖	16	8, 16	8, 16	5, 8, 16	8
Page Number	PS/6-24	PS/6-31	PS/6-35	PS/6-38	PS/6-41

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3714	UC3715	UC3724	UC3725	UC3726
Power Driver					Transmitter
FET Driver	Dual	Dual	Transmitter	Single	
Isolated Driver Pairs			FET Drv	FET Drv	IGBT Drv
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting	Non-Inverting	Non-Inverting
Enable	Y	Y			
Inhibit					
Analog Stop					
Output Rise Time	100ns / 50ns	100ns / 50ns	30ns	30ns	75ns
Maximum Voltage	20V	20V	40V	40V	40V
Peak Output Current	1.0A / 2.0A	1.0A / 2.0A	2.0A	2.0A	4.0A
Application / Design Note	U-111	U-111	DN-35, U-127	DN-35, U-127	DN-57, DN-60, U-143C
Pin Count ❖	8, 16	8, 16	8, 16	8, 16	16, 28
Page Number	PS/6-43	PS/6-43	PS/6-50	PS/6-53	PS/6-57

Power and FET Drivers	UNITRODE PART NUMBER				
	UC3727	UCC37423+	UCC37424+	UCC37425+	UCC37523+
Power Driver	Single				
FET Driver		Dual	Dual	Dual	Dual
Isolated Driver Pairs	IGBT Drv				
Relay Drivers					
Output Configuration	Non-Inverting	Inverting	Non-Inverting	One Inverting, One Non-Inverting	Inverting
Enable					Y
Inhibit					
Analog Stop					
Output Rise Time	75ns	20ns	20ns	20ns	20ns
Maximum Voltage	40V	20V	20V	20V	20V
Peak Output Current	4.0A	3.0A	3.0A	3.0A	3.0A
Special Features		UVLO	UVLO	UVLO	UVLO, Adaptive LEB
Application / Design Note	DN-57, DN-60, U-143C				
Pin Count ❖	20, 28	8, 16	8, 16	8, 16	8, 16
Page Number	PS/6-62	PS/6-68	PS/6-68	PS/6-68	PS/6-73

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Drivers (cont.)

Power and FET Drivers	UNITRODE PART NUMBER				
	UCC37524+	UCC37525+	UCC3776		
Power Driver					
FET Driver	Dual	Dual	Quad		
Isolated Driver Pairs					
Relay Drivers					
Output Configuration	Non-Inverting	One Inverting, One Non-Inverting	Non-Inverting		
Enable	Y	Y	Y		
Inhibit					
Analog Stop					
Output Rise Time (ns)					
Maximum Voltage	20V	20V	18V		
Peak Output Current	3.0A	3.0A	1.5A / 2.0A		
Special Features	UVLO, Adaptive LEB	UVLO, Adaptive LEB	UVLO		
Application / Design Note					
Pin Count ❖	8, 16	8, 16	16		
Page Number	PS/6-73	PS/6-73	PS/6-79		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support

Feedback Signal Generators	UNITRODE PART NUMBER			
	UC3901	UC39431	UC39432	UC3965
Description	Isolated Feedback Generator	Precision Adjustable Shunt Regulator	Precision Analog Controller	Precision Reference with Low Offset Error Amplifier
Application	Amplitude Modulation System Used to Couple a Control Signal Across a Voltage Isolation Barrier	Adjustable 100mA Shunt Regulator, Voltage Reference Optocoupler Driver, Voltage to Current Converter	Adjustable 100mA Shunt Regulator, Optocoupler Driver, Programmable Transconductance Voltage to Current Converter	Used for High Precision PWM Switching Regulators
Key Features	•Transformer Couples Isolated Feedback Error Signal •Low Cost Alternative to Optical Couplers •5MHz Carrier Provides Fast Response Capability •Modulator Synchronizable to an External Clock	•Multiple On-chip Programmable Reference Voltages •2.2V to 36V Operating Supply Voltage and User Programmable Reference •Linear Transconductance for Optocoupler Feedback Applications	•Programmable, Linear Transconductance for Optimum Optocoupler Current Drive •Precision Reference and Error Amplifier Inputs Externally Available •2.2V to 36V Operating Supply Voltage and User Programmable Reference	•2.5V Precision Reference with 0.4% Accuracy •Low 1mV Offset Error Amplifier •2X Inverting Amplifier / Buffer Output •Drivers Optocoupler Diode for Isolated Applications
Application / Design Note	DN-19, DN-33, U-94		DN-52	U-165
Pin Count❖	14, 16	8	8	8
Page Number	PS/7-21	PS/7-50	PS/7-56	PS/7-60

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Load Share Controllers	UNITRODE PART NUMBER		
	UC3902	UC3907	
Description	8-Pin Load Share Controller	Load Share Controller	
Application	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	Allows Multiple Independent Power Supplies to be Paralleled so that Each Unit Supplies Only its Proportional Share of Total Load Current	
Key Features	• Highly Tolerant of Voltage Differences Between Power Supply Return • 2.7V to 20V Operation • High Gain, Low Offset Current Sense Amplifier Permits Low Shunt Resistor Values • Single Capacitor Sets Load Share Filter Response	• Fully Differential High Impedance Voltage Sensing • Accurate Current Amplifier for Precise Load Sharing • Optocoupler Driving Capability • 4.5V to 35V Operation	
Application / Design Note	U-129, U-163	U-129, U-163	
Pin Count❖	8	16	
Page Number	PS/7-27	PS/7-44	

Schottky Diode Array / Bridges	UNITRODE PART NUMBER		
	UC3610	UC3611	UC3612
Description	Dual Schottky Diode Bridge	Quad Schottky Diode Array	Dual Schottky Diode
Application	Eight-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads	Four-diode Array for High Current Bridges and Voltage Clamps	Two-diode Array for High Current, Low Duty Cycle Flyback Voltage Clamping for Inductive Loads
Key Features	• Monolithic Eight-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time	• Matched, Four-diode Monolithic Array • High Peak Current • Low Forward Voltage • Parallelable for Higher Current or Lower Voltage Drop	• Monolithic Two-diode Array • High Peak Current • Low Forward Voltage • Fast Recovery Time
Application / Design Note			DN-48
Pin Count❖	8, 16	8, 16	8
Page Number	PS/7-10	PS/7-12	PS/7-15

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Power Supply Support (cont.)

Supervisory and Monitor Circuits	UNITRODE PART NUMBER				
	UC3543	UC3544	UC3730	UC3903	UC3904
Power Supply Monitor	Single	Single		Quad	Quad
Temperature Monitor			Y		
Description	Power Supply Supervisory with OV, UV and Current Sensing	Power Supply Supervisory with OV, UV and Current Sensing	Combines a Temperature Transducer, Precision Reference, and Temperature Comparator for Maximum System Flexibility	Quad Supply and Line Monitor	Quad Supply and Line Monitor
Voltage Clamp					
Voltage Range	5V to 35V	5V to 35V		8V to 40V	4.75V to 18V
Window Adjust	N	N		Y	Y
Current Range					
Current Limit	Y	Y		N	N
Programmable Threshold	Y	Y		Y	Y
Programmable Time Delay	Y	Y		Y	Y
Special Features		Uncommitted OV Inputs			
Application / Design Note				DN-33	
Pin Count ❖	16	18	5, 8, 20	18	18
Page Number	PS/7-5	PS/7-5	PS/7-17	PS/7-32	PS/7-39

Supervisory and Monitor Circuits	UNITRODE PART NUMBER		
	UCC3946		
Description	Microprocessor Supervisor with Watchdog Timer		
Application	Accurate Microprocessor Supervision		
Key Features	• Programmable Reset Period • Programmable Watchdog Period • 1.5% Accurate Threshold • 4mA IDD		
Pin Count ❖	8		
Page Number	PP/7-88		

All products feature Pulse-by-Pulse Current Limiting and UVLO unless otherwise noted.
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control

Brushless Motor Products	UNITRODE PART NUMBER				
	UC3625	UCC3626+			
Hall Logic	Y	Y			
Tachometer	Y	Y			
Output Current per Output	0.1A	0.01A			
Operating Voltage	10V - 18V	11V - 15V			
Differential Current Sense Amplifier	Y	Y			
Current Limit	Y				
Application / Design Note	DN-50, U-115, U-120, U-130	U-120			
Pin Count ❖	28	28			
Page Number	PS/8-37	PS/8-50			

DC Motor Controllers	UNITRODE PART NUMBER				
	UC3637	UC3638			
Output Clamp Diodes					
Output Current per Output	0.1A	0.1A / 0.05A			
Operating Voltage	5V - 36V	10V - 36V			
Differential Current Sense Amplifier		Y			
Thermal Shutdown					
Current Limit	Y	Y			
Application / Design Note	DN-53A, U-102, U-112, U-120	DN-76, U-120			
Pin Count ❖	18, 20	20			
Page Number	PS/8-78	PS/8-84			

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Linear Power Amplifier Products	UNITRODE PART NUMBER				
	UC3173A	UC3175B	UC3176	UC3177	UC3178
Output Clamp Diodes	Y	Y	Y	Y	Y
Output Current per Output	0.55A	0.8A	2A	2A	0.45A
Operating Voltage	4V - 15V	4V - 15V	3V - 35V	3V - 35V	3V - 15V
Differential Current Sense Amplifier	Y	Y	Y	Y	Y
Thermal Shutdown	Y	Y	Y	Y	Y
Current Limit	Y	Y	Y	Y	Y
Four Quadrant	Y	Y	Y	Y	Y
Number of Outputs	2	2	2	2	2
BW	2MHz	2MHz	1MHz	1MHz	2MHz
Special Features			B+ Input Pin	Supply OK Pin	
Pin Count ❖	24	24	28	28	28
Page Number	PS/8-5	PS/8-16	PS/8-21	PS/8-21	PS/8-25

Phase Locked Frequency Controllers	UNITRODE PART NUMBER				
	UC3633	UC3634	UC3635		
Internal Oscillator	Y	Y	Y		
Divider Output Provided			Y		
External Phase Detector Inputs			Y		
2 Phase Drive Logic		Y	Y		
Divide Logic Select	4/5 & 2/4/8	2/4/8	2/4		
Operating Voltage	8V - 15V	8V - 15V	8V - 15V		
Maximum Frequency	10MHz	10MHz	10MHz		
Application / Design Note	U-113	U-113	U-113		
Pin Count ❖	16, 20	16, 20	16		
Page Number	PS/8-63	PS/8-70	PS/8-74		

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Motion Control (cont.)

Stepper Motor Controllers	UNITRODE PART NUMBER				
	UC3517	UC3717	UC3717A	UC3770A	UC3770B
Output Clamp Diodes		Y	Y	Lower	Lower
Output Current per Output	0.35A	0.8A	1A	1.3A	1.3A
Operating Voltage	10V - 40V	10V - 45V	10V - 46V	10V - 50V	10V - 50V
Differential Current Sense Amplifier					
Thermal Shutdown		Y	Y	Y	Y
Current Limit		Y	Y	Y	Y
Current Sense Thresholds					Tailored for half stepping applications
Application / Design Note		U-99	U-99		
Pin Count ❖	16	16, 20	16, 20	16, 28	16, 28
Page Number	PS/8-30	PS/8-92	PS/8-100	PS/8-108	PS/8-108

❖The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions

Special Functions

Current Sensors	UNITRODE PART NUMBER				
	UCC3926				
Application	Current Sensing				
Maximum Current	±20A				
Application / Design Note	DN-91				
Pin Count ❖	16				
Page Number	PS/9-43				

Lighting Controllers	UNITRODE PART NUMBER				
	UCC3305✣				
Application	Constant Power HID Lamp Controller				
Topology	Boost, Flyback				
Outputs	3 - Single and Dual Alternating, Totem Pole				
Reference Tolerance	2%				
Open Lamp Detect	Y				
Soft Start	Y				
External Synchronization	Y				
Shutdown Current	N/A				
Maximum Frequency	500kHz				
Lamp Intensity Control	Y				
Application / Design Note	DN-72, U-161				
Pin Count ❖	28				
Page Number	PS/9-5				

❖The smallest available pin count for thru-hole and surface mount packages.
✣ Does Not Feature UVLO.
+ New Product

Special Functions (cont.)

Ring Generator Controllers	UNITRODE PART NUMBER		
	UCC3750	UCC3751+	UCC3752+
Description	Source Ringer Controller	Single Line Ring Generator Controller	Mulit-Line Ring Generator Controller
Application	4 Quadrant Flyback Controller Develops High Voltage AC Output	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset	Controls Low Cost Circuit for Generating High Voltage AC Output with DC Offset
Key Features	• On Chip Low THD Sinewave Reference, Pin Selectable 20Hz, 25Hz, and 50Hz • Programmable Output Amplitude and DC Offset • AC and DC Current Limiting With Short Circuit Protection	• Off-hook Detection With Automatic Transition to DC Operation • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection	• Off-hook Detection and Indication • Pin Selectable 20Hz, 25Hz, and 50Hz Output Frequency • Operates From a Single 12V Supply • AC Current Limiting and Short Circuit Protection
Application / Design Note	DN-79, U-169		
Pin Count ❖	28	16	16
Page Number	PS/9-22	PS/9-32	PS/9-38

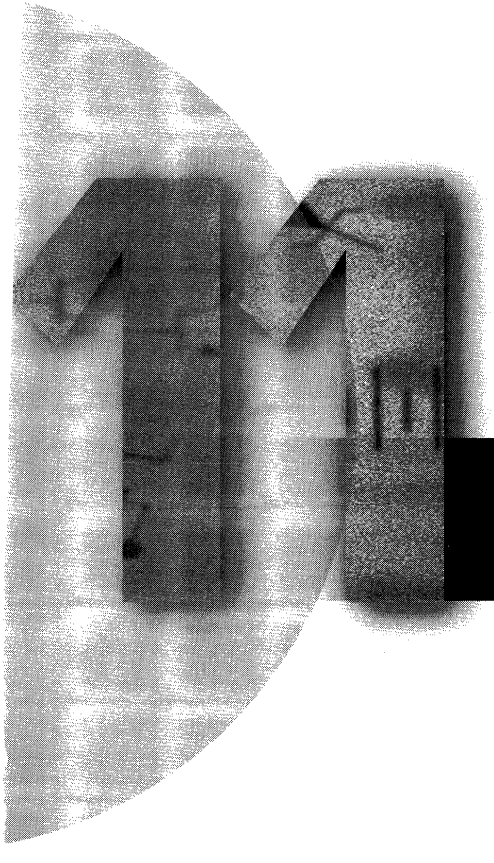
❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product

Special Functions (cont.)

Sensor Drivers	UNITRODE PART NUMBER				
	UC37131+	UC37132+	UC37133+		
Part Name	Smart Power Switch	Smart Power Switch	Smart Power Switch		
Description	65V Universal Low Side Driver with Current Limiting	65V Universal High or Low Side Driver with Current Limiting	65V Universal High Side Driver with Current Limiting		
Pin Count ❖	8	14, 16	8		
Page Number	PS/9-13	PS/9-13	PS/9-13		

Serial DACs	UNITRODE PART NUMBER		
	UCC5950		
Part Name	Digital to Analog Converter		
Description	10-Bit BiCMOS Digital to Analog Converter for Servo and Instrumentation Systems		
Pin Count ❖	8		
Page Number	PS/9-48		

❖ The smallest available pin count for thru-hole and surface mount packages.
+ New Product



Military/Aerospace Products

General Information

Die and Wafers

Unitrode offers most of its products in die and/or wafer form through die distributors. Unitrode's die utilize either linear bipolar or BiCMOS process technology featuring tight beta controls and resistor matching techniques. Die thickness is either 12 mils or 15 mils, ±1 mil. Interconnects are an alloy of copper and aluminum (to reduce the possibility of electromigration). Most product's backside material is pure silicon.

Testing. All products are tested at two separate points: (1) wafer process parameter in-line probing and (2) ambient electrical test probing. Die are tested to full data sheet specifications with the exception of some high power or high speed devices where production probe equipment limit the test environment.

Inspection. Unitrode performs visual inspections on military grade die to MIL-STD-883, Method 2010, conditions A or B, or to individual customer specifications. Die is supplied in "waffle pack" or single wafer form. Standard wafers are 100 mils, generic 4- or 6-inch diameter.

Ordering. Product is available from Unitrode's authorized die distributors, and part numbers end with the suffix "c" for chip form or "chipwfr" for wafer form.

Military/Aerospace Products

Unitrode offers its innovative, quality products in military/aerospace and high reliability versions. Our certification to MIL-PRF-38535 demonstrates our commitment to our customer's requirements in this important market segment. Our product offering includes:

- ***STANDARD MILITARY DRAWINGS (SMD)*** ~ *Conformance to Class Q performance requirements of MIL-PRF-38535, and individual SMD electrical parameters. Unitrode offers over 100 SMD products.*
- ***CLASS V*** ~ Conformance to all Class V requirements of MIL-PRF-38535, or to individual customer source control documents.
- ***SCDClass B*** ~ Unitrode also accepts unique customer source control drawings for Class B, MIL-STD-883 type products.
- ***Bare Die / Lot Acceptance Testing*** ~ Tested to individual source control documents.

Unitrode has had DESC facility certification continuously since November 1985.

Space Level Products

Unitrode is a leader in producing linear ICs to customers' Class S specifications and has many years of proven experience in this field. Our abilities in this area include all processing requirements of Class S (including MIL-PRF-38535, MIL-STD-883, and SCC9000), as well as an extensive library of radiation data on our most popular devices (see below). Our superior design support, years of experience, and flexibility to service our customers' unique requirements make us the best choice for Class S linear products.

Radiation Data Availability

Unitrode has provided products screened to the S-level requirements of MIL-STD-883, MIL-PRF-38535, and the European specification SCC9000. Due to our participation in this market, we have collected a variety of radiation reports including SEU, total dose (including low dose rate), and neutron fluence, which are available upon customer request (see listing below). These reports are results of independent testing by our customers and do not represent guaranteed levels of radiation tolerance by Unitrode. The availability of this data is subject to change. Contact your local Unitrode sales representative.

Raditation data is available for the following Unitrode products: UC1625, UC1635, UC1710, UC1711, UCC1800, UCC1806, UC1823, UC1825/A, UC1832, UC1834, UC1838A, UC1843A, UC1845, UC1846, UC1856, UC1863, UC1875, UC1901, UC1907, UCC1912.

Standard Military Drawings (SMDs) Listing Unitrode as an Approved Supplier

SMD Number	*Unitrode Part Number*
5962-8670401PA	UC1842J/883B
5962-8670401XA	UC1842L/883B
5962-8670402PA	UC1843J/883B
5962-8670402XA	UC1843L/883B
5962-8670403PA	UC1844J/883B
5962-8670403XA	UC1844L/883B
5962-8670404PA	UC1845J/883B
5962-8670404XA	UC1845L/883B
5962-8670405PA	UC1842AJ/883B
5962-8670405XA	UC1842AL/883B
5962-8670406PA	UC1843AJ/883B
5962-8670406XA	UC1843AL/883B
5962-8670407PA	UC1844AJ/883B
5962-8670407XA	UC1844AL/883B
5962-8670408PA	UC1845AJ/883B
5962-8670408XA	UC1845AL/883B
5962-86806012A	UC1846L/883B
5962-8680601EA	UC1846J/883B
5962-86806022A	UC1847L/883B
5962-8680602EA	UC1847J/883B
5962-87619012A	UC1707L/DESC
5962-8761901EA	UC1707J/DESC
5962-8764502EA	UC1524AJ/DESC
5962-87681012A	UC1825L/883B
5962-8768101EA	UC1825J/883B
5962-87681022A	UC1825AL/883B
5962-8768102EA	UC1825AJ/883B
5962-8768102XA	UC1825ALP/883B
5962-87681032A	UC1825BL/883B
5962-8768103EA	UC1825BJ/883B
5962-8768103XA	UC1825BLP/883B
5962-8774001EA	UC1543J/883B
5962-8774002EA	UC1544J/883B
5962-87742012A	UC1834L/883B
5962-8774201EA	UC1834J/883B
5962-88697012A	UC1903L/883B
5962-8869701VA	UC1903J/883B
5962-89441012A	UC1901L/883B
5962-8944101CA	UC1901J/883B
5962-89511012A	UC1525AL/DESC
5962-8951101EA	UC1525AJ/DESC
5962-89511032A	UC1525AL/883B
5962-8951103EA	UC1525AJ/883B
5962-8951104EA	UC1527AJ/883B
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5962-8989901EA	UC1838AJ/883B
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5962-8990501EA	UC1823J/883B
5962-89905022A	UC1823AL/883B
5962-8990502EA	UC1823AJ/883B
5962-89905032A	UC1823BL/883B
5962-8990503EA	UC1823BJ/88B
5962-89920012A	UC1840L/883B
5962-8992001VA	UC1840J/883B
5962-89920022A	UC1841L/883B
5962-8992002VA	UC1841J/883B
5962-89957012A	UC1637L/883B
5962-8995701VA	UC1637J/883B

SMD Number	Unitrode Part Number
5962-90538012A	UC1611L/883B
5962-9053801PA	UC1611J/883B
5962-90650012A	UC1835L/883B
5962-9065001PA	UC1835J/883B
5962-9098701M2A	UC1633L/883B
5962-9098701MEA	UC1633J/883B
5962-9168901MXA	UC1625J/883B
5962-9203101M2A	UC1864L/883B
5962-9203101MEA	UC1864J/883B
5962-9203102MEA	UC1865J/883B
5962-9235001MXC	L293DSP/883B
5962-9320601M2A	UC1907L/883B
5962-9320601MEA	UC1907J/883B
5962-9321501M2A	UC1517L/883B
5962-9321501MEA	UC1517J/883B
5962-9326101M2A	UC1854L/883B
5962-9326101MEA	UC1854J/883B
5962-9326102M2A	UC1854BL/883B
5962-9326102MEA	UC1854BJ/883B
5962-9326103M2A	UC1854AL/883B
5962-9326103MEA	UC1854AJ/883B
5962-9326501M2A	UC1832L/883B
5962-9326501MCA	UC1832J/883B
5962-9326502M2A	UC1833L/883B
5962-9326502MPA	UC1833J/883B
5962-9451301MPA	UCC1801J/883B
5962-9451302MPA	UCC1802J/883B
5962-9451303MPA	UCC1803J/883B
5962-9451304MPA	UCC1804J/883B
5962-9451305MPA	UCC1805J/883B

SMD Number	Unitrode Part Number
5962-9453001M2A	UC1856L/883B
5962-9453001MEA	UC1856J/883B
5962-9455501M3A	UC1875L/883B
5962-9455501MRA	UC1875J/883B
5962-9455501MXA	UC1875LP/883B
5962-9457501MEA	UCC1806J/883B
5962-9462201M2A	UC1871L/883B
5962-9462201MVA	UC1871J/883B
5962-9474601M2A	UC1717L/883B
5962-9474601MEA	UC1717J/883B
5962-9554401MJC	UC1620SP/883B
5962-9558601MVA	UC1851J/883B
5962-9579801M2A	UC1705L/883B
5962-9579801MPA	UC1705J/883B
77034012A	UC117L/883B
77034052A	UC117AL/DESC
7802801EA	UC1524J/DESC
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8551501VA	UC1526J/883B
85515022A	UC1526AL/883B
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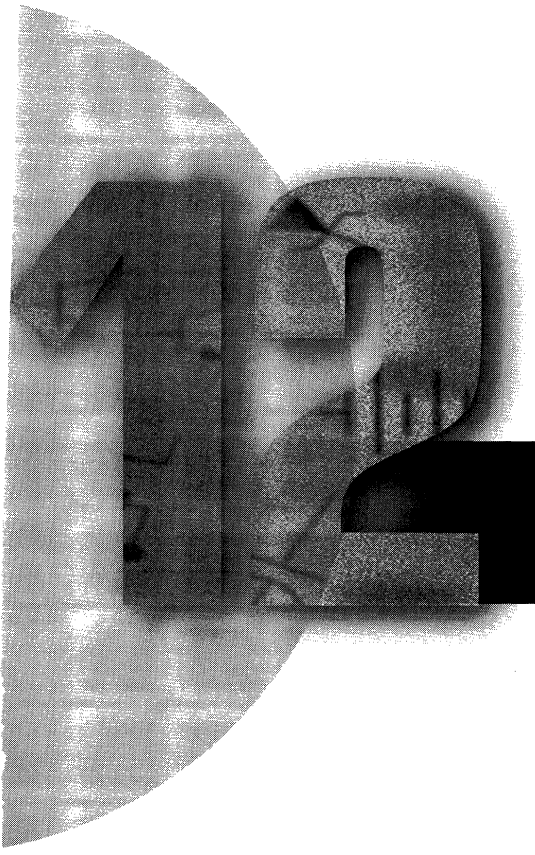


Packaging Information

Packaging Information

The following are Unitrode's recommended profiles and limits for plastic package surface-mounting and de-soldering methods. To achieve and maintain the recommended conditions near the plastic package, time/temperature profiles of the surface-mount processing equipment may differ from those below, depending on board density, oven mass, exhaust rate, and other factors.

Unitrode uses a solder reflow pre-conditioning process with a 220° C peak temperature to determine moisture sensitivity ratings for plastic packaged components. The profiles shown are used with Unitrode's moisture-sensitivity ratings of the plastic packaged surface-mount components. Published moisture sensitivity ratings may not apply when a process with a more extreme peak temperature (such as wave solder) is used. If the temperatures or rates of temperature increase exceed those noted for IR reflow, then we recommend that the packaged component be either baked before surface-mount assembly or handled in consistence with the next lower moisture-sensitivity rating. (For example, handle a Level-2 rated part as Level 3.) For baking conditions and/or definitions of moisture-sensitivity level ratings, consult JEDEC J-STD-020A and J-STD-033.

For more than one soldering pass (e.g., on boards with components on top and bottom), time between the two soldering processes must be between 5 minutes and 48 hours. Between passes, if the environmental conditions of the plastic packaged component exceed 30° C/60% RH, then the component must be baked before the second pass.

Wave Solder *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120 seconds
- Maximum rate of increase to maximum solder temperature 3° C/s
- Solder temperature of first (turbulent) wave < 250° C (4 seconds maximum)
- Solder temperature of second (broad) wave < 240° C (10 seconds maximum, 2° C/s maximum rate of cooling from first wave)
- Maximum cooling to room temperature 4° C/s maximum
- Total time over 183° C < 90s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Maximum time from 25° C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

NOTE: We **STRONGLY RECOMMEND** that the component's plastic body not contact the solder wave or bath during assembly. Contact can be prevented by shielding. If contact occurs, then do the following:

- Pre-bake parts within 4 hours before board-mount assembly (24 hours at 125° C or 192 hours at 40° C).
- Limit all rates of temperature change to 2.5° C/s.
- Limit total time over 183° C to less than 45s.

IR Reflow or Convection Reflow *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 3° C/s
- Maximum reflow temperature < 240° C (20s maximum with 5° C of peak temperature)
- Maximum rate of decrease to room temperature 6° C/s
- Maximum time over 210° C < 40s
- Maximum total time over 183° C < 150s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Maximum time from 25° C to peak temperature 6 minutes
- Minimum 5-minute cool-down time between cycles

Vapor Phase Reflow *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

- Maximum rate of increase for pre-heat 6° C/s
- Pre-heat temperature range 100–150° C
- Total pre-heat time 60–120s
- Maximum rate of increase to maximum solder temperature 10° C/s
- Maximum reflow temperature < 219°C (60s maximum with 5° C of peak temperature)
- Maximum rate of decrease to room temperature 10° C/s
- Maximum time over 183°C < 80s
- Difference between the maximum pre-heat and maximum soldering temperatures ≤100° C
- Minimum 5-minute cool-down time between cycles

Rework *(Temperatures unless otherwise noted apply to the top-side of the component body.)*

To preserve the integrity of the plastic packaged component (for further analysis), we suggest the following steps to minimize damage from component removal.

- Always keep the package body temperature below 200° C.
- Bake out moisture in packages rated JEDEC Level 2-6 or in packages exposed to uncontrolled ambient conditions since being assembled.
- For hand de-soldering (i.e., soldering iron), do not allow maximum temperature at the leads to exceed 300° C for more than 5s.

For forced-hot-air de-soldering, the following limits apply:

- Limit the rate of temperature increase to 25° C/s between ambient and 100° C.
- Limit the rate of temperature increase to 4° C/s maximum from 100° C to de-soldering temperature.
- Limit maximum de-soldering temperature at leads to less than 240° C (10s maximum).
- Carefully minimize the cooling rate after removing the part from the printed circuit board.

Introduction

All operating circuit components dissipate power, causing their temperature to rise. Unitrode integrated circuits are designed to operate in a considerable range of temperatures, but there are limits. This note suggests ways to ensure that specified temperature limits for each part are not exceeded.

Junction Temperature (Tj)

For reliability and long-term operating life of the device, the system designer must manage the power dissipated by the device in the system so junction temperature (Tj) not only does not exceed specified limits, but also is kept as low as possible. This temperature control is necessary, because higher junction temperatures adversely affect the operating life of the device.

Power Dissipation (Pd) and Thermal Resistance (q)

With power off, all components of a given circuit approach (and in time reach) ambient temperature. With the power on, the components are warmed by their internal power dissipation until a new equilibrium is reached. Some electrical power is dissipated as heat by an integrated circuit (Pd) during operation, thus raising the junction temperature. The effectiveness of the IC package and the system in dissipating this heat is "thermal resistance" (θ), a term analogous to electrical resistance in the sense that the materials of the IC, package, and system restrict the flow of heat from the higher junction temperature (Tj) to the lower ambient temperature of the system (Ta). Understanding the thermal resistance characteristics of the package and system facilitates management of the device junction temperature within desired limits.

The rate of heat flow depends on the temperature difference (DT) between the two endpoints (Tj and Ta), and also on the thermal resistance, θ, of the package and system. Heat is a form of energy, and if we choose the joule as the measuring unit we can specify the rate of heat flow in units of joules per second. Therefore, $Pd\left[joules\,per\,second\right]=\frac{\Delta T}{\theta}$ and since one *joule per second* is the same as a watt (W), we have $\theta=\frac{\Delta T}{Pd}(^{\circ}C/W)$

Thermal resistance is typically expressed in terms of resistance from junction-to-ambient (θja), which incorporates not only the internal resistance of the IC package, but also the resistance of the system as well. θja can be broken down into the sum of these two different thermal resistances, from junction-to-case, θjc (or in the case of power surface-mount packages, junction-to-lead, θjl) and case-to-ambient, θca. Therefore, $\theta ja=\frac{Tj-Ta}{Pd}=\theta jc+\theta ca$

Variables Which Affect θja

The thermal resistance of the package is a function of many variables, such as the leadframe material and design configuration, the plastic encapsulant material, the silicon die area, the die attach material, and others. However, as previously indicated, the effectiveness of the system in removing heat from the package also has a significant impact on θja. These variables include the material and configuration of the circuit board on which the package is mounted, the type of cooling used (i.e., conduction or convection), the size of the traces on the circuit board, the use of heatsinks, etc. It is essential that the system designer understand these variables and how they affect θja.

Unitrode Test Procedures

Table 1 shows thermal resistance values for Unitrode IC packages. Thermal resistance junction-to-case (θjc) is measured by mounting the device to an essentially infinite heat sink. Power leadframe surface-mount packages and the batwing DIP conduct most of the dissipated power through their leads rather than through the case. For these noted packages, the specified thermal resistance is junction-to-lead (θjl).

Junction-to-ambient (θja) thermal resistance is measured on a 5.0-square-inch printed circuit board in 1 cubic foot of still air. For through-hole packages, single-side FR-4 boards with 1-ounce copper traces are used. (See Figure 1.) However, since surface-mount devices, including those without power leadframes, conduct a significant amount of heat through their leads to the pc-board, various types of surface-mount boards are measured. (See Figure 2.) To indicate the effect of the pc-board on θja, a range of values is given. The lower value is for a device mounted on a 5.0-square-inch, 0.062 inch thick aluminum pc-board. The highest value is for a device mounted on a 5.0-square-inch single-sided pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. Some interpolation may be needed based on an individual application to arrive at an accurate estimate of the actual θja.

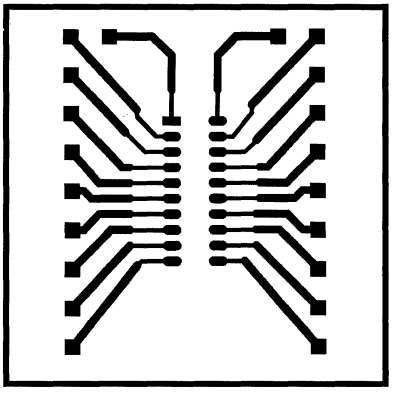


Figure 1. Typical through-hole pc-board design.

To determine the device θja, a measurement of the device junction temperature is made under the above conditions using a technique called the "temperature-sensitive parameter" method. This technique involves measuring the voltage drop of calibrated component, typically a diode, which then allows calculation of the device junction temperature. Since Pd, Tj, and Ta are known, θja can be determined. For the case of power leadframe surface-mount packages, θjl is determined by measuring the temperature of the pc-board at the device leads and then using this temperature in place of the ambient temperature in the calculation. For a more detailed discussion on surface-mount packages, refer to "Thermal Characteristics of Surface-Mount Packages," found later in this section.

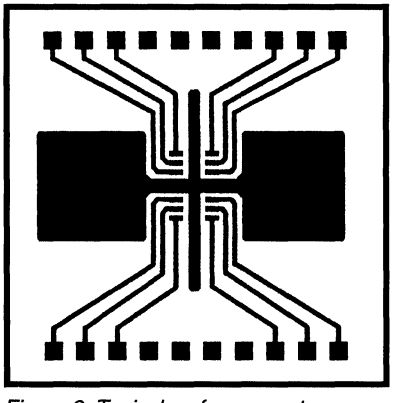


Figure 2. Typical surface mount pc-board design for power leadframe SOIC packages.

Example

Estimate the junction temperature of a UC5601DWP 18-Line SCSI Active Terminator on a 4-layer 0.062 inch thick multilayer pc-board at 1.0 watt power dissipation in a still-air environment at 30°C.

1. Determine θja. Table 1 shows that the the DWP package is a power leadframe surface-mount device, so the use of thermal resistance junction-to-lead (qjl) is appropriate. For the DWP package, qjl = 16°C/W. From Figure 8 in "Thermal Characteristics of Surface-Mount Packages," thermal resistance board-to-ambient (θba) = 19°C/W. We know that for a power leadframe surface-mount package, θja = θjl + θba, so, θja = 16°C/W + 19°C/W = 35°C/W.

2. Calculate the junction temperature, Tj.

$$Tj = (Pd \times \theta ja) + Ta$$
$$Tj = (1.0\ W \times 35°C/W) + 30°C$$
$$Tj = 65°C$$

This is well below the maximum rated junction temperature of 150°C listed in the Absolute Maximum Ratings section of the UC5601 product data sheet, so the thermal dissipation is satisfactory.

System Design Considerations

Through-hole devices such as dual in-line packages (DIPs) can be cooled by forcing airflow over the device in order to improve the convection cooling performance, or by conduction cooling of the package case to a heat sink such as the system chassis or cold-wall. Plastic DIPs are not particularly well suited to either of these techniques since the plastic encapsulant is a relatively poor thermal conductor. However, Unitrode offers several through-hole packages which have been optimized for conduction cooling techniques, namely the batwing DIP, the SP power ceramic DIP and the power leadframe Zig-Zag (ZIP) package. All of these packages provide low thermal resistance paths from the junction to the pc-board. Refer to Table 1 for the applicable ratings.

Surface-mount packages are well suited to conduction cooling since, as previously indicated, the package leads conduct a significant amount of heat to the pc-board. The pc-board itself can be utilized effectively as a heat sink when designed properly. For example, as seen in the discussion "Thermal Characteristics of Surface Mount Packages," when a power leadframe package is mounted on a multi-layer pc-board such that the heat-sink leads are thermally coupled to a ground plane in the board, or an area of copper fan-out on the board, then the overall thermal resistance is considerably lower than on a single-sided board with no heat-sinking. Additionally, Unitrode offers a power ceramic leadless chip carrier with a metallized thermal grid on the package case, which can be soldered directly to the board, thus greatly reducing its overall thermal resistance.

In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away from the device more effectively. Also, one should avoid grouping higher power devices tightly together on the board. A better approach would be to spread out the higher power devices to the cooler areas of the board. The choice of pc-board material will greatly affect the overall thermal performance of the system as well, although there are many factors involved when selecting the board material, such as cost, mechanical properties and environmental requirements.

Summary

Thermal management has been shown to be an essential factor in the reliable use of Unitrode integrated circuits. Thermal characteristics of Unitrode packages have been provided to the system designer in order to ensure that the system design effectively dissipates the power generated by the integrated circuit during operation.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
Ceramic DIP	8	J	390x288x140	150x200	N/A
	14		760x248x140	110x140	N/A
	16		760x288x140	160x250	N/A
	18		890x288x140	160x250	N/A
	20		950x288x140	160x250	N/A
	24		1250x520x170	250x250	N/A
	28		1450x520x165	250x250	N/A
Ceramic LCC	20	L	350x350x80	194x194	N/A
	28		450x450x80	250x250	N/A
Ceramic LCC Power	28	LP	450x450x80	250x250	N/A
LQFP	48	FQ	7x7x1.4 mm	200x200x5	100x100x12
	64		10x10x1.4 mm	260x260x5	100x100x12
	100		14x14x1.4 mm	276x276x5	100x100x12
LQFP Power	48	FQP	7x7x1.4 mm	185x185x5	100x100x12
	48		7x7x1.4 mm	190x190x5	100x100x12
MSOP	8	P	3x3x0.86 mm	68x94x6	50x50x8
	10		3x3x0.86 mm	68x98x6	50x50x8
PDIP	8	N	360x253x137	140x150x10	N/A
	14		760x253x137	110x140x10	N/A
	16		760x253x137	140x170x10	N/A
	18		905x253x137	160x250x10	N/A
	20		1020x253x137	150x190x10	N/A
	24		1250x525x137	180x220x10	N/A
	28		1425x525x137	200x200x10	N/A
PDIP Power	16	NP	760x253x137	160X170X10	N/A
PLCC	20	Q	350x350x155	180x180x10	N/A
	28		450x450x155	230x230x10	N/A
	44		650x650x155	230x230x10	N/A
PLCC Power	28	QP	450x450x155	200x200x10	N/A
	44		650x650x155	300x300x10	N/A

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θja, lower value is for 3x3 in. 1 oz. internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
125-160	28 (8)	
90-120	28 (8)	
80-120	28 (8)	
70-90	28 (8)	
70-85	28 (8)	
60-75	28 (8)	
50-65	28 (8)	
70-80	20 (8)	
60-70	20 (8)	
N/A	5-8*	θjc estimated for backside of device, through the metalized thermal conduction pads.
58-76**	15**	Modeled using .3 mm trace width
44-59**	12**	Modeled using .3 mm trace width
31-46**	11**	Modeled using .3 mm trace width
34 (9) 38-61**	8**	Leads 5,6,7,8,17, 18,19,29,30,31,32, 42,43 and 44 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
35 (10) 43-65**	8**	Leads 4,5,6,7,8,9,28,29,30,31,32 and 33 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
238-269** 312-373**(7)	41**	Modeled using .3 mm trace width.
210-241** 273-330**(7)	39**	Modeled using .3 mm trace width.
110 (3)	50	
90 (3)	45	
90 (3)	45	
85 (3)	40	
80 (3)	35	
60 (3)	30	
60 (3)	30	
25-50 (4)	12 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle.
43-75 (3)	34	
40-65 (3)	30	
35-50 (3)	20	
28-50 (3)	14 (2)	Leads 12,13,14,15,16,17 and 18 are fused to the die attach paddle. Single layer board used 1.2 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
24-38 (3)	12 (2)	Leads 6,7,17,29,39 and 40 are fused to the die attach paddle. Single layer board used 1.1 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.

Package Thermal Resistance Data

Package	Lead Count	Unitrode Package Code	Body Size (mils unless noted)	Die Paddle or Cavity Size (mils)	Die Size Tested (mils) (16)
QSOP	16	M	193x154x59	96x130x8	50x50x12
	20		340x154x59	96x140x8	50x50x12
	28		389x154x59	96x150x8	50x50x12
QSOP Wide Body Power	36	MWP	606x295x92	180x240x10	100x100x15 100x100x12**
	44		704x295x92	190x260x10	100x100x15 100x100x12**
SOIC Narrow Body	8	D	192x154x54	95x152x8	N/A
	14		340x154x54	83x142x8	N/A
	16		390x154x54	90x150x8	N/A
SOIC Narrow Power	8	DP	192x154x54	95x150x8	N/A
	16		390x154x54	95x165x8	N/A
SOIC Wide Body	16	DW	408x296x94	165x205x10	N/A
	18		458x296x94	145x190x10	100x100x12
	20		508x296x94	165x205x10	N/A
	24		602x296x94	165x205x10	100x100x12
	28		705x296x94	165x205x10	100x100x12
SOIC Wide Body Power	28	DWP	705x296x94	156x205x10	N/A
TO220	3	T, TH, TV	400x592x165	180x180x18	N/A
	5		400x605x165	180x180x18	N/A
TO263	3	TD	395x415x175	240x180x23	N/A
	5		395x415x175	240x180x23	N/A
TSSOP	8	PW	118x174x35	126x87x5	50x50x10
	14		197x174x35	118x150x5	100x100x10
	16		197x174x35	118x154x5	100x100x10
	20		255x174x35	118x165x5	100x100x10
	24		307x174x35	118x217x5	100x100x10
	28		382x174x35	118x217x5	100x100x10
TSSOP Power	24	PWP	307x174x35	118x217x5	100x100x10
	28		382x174x35	118x250x5	100x100x10
	28		382x174x35	118x250x5	100x100x10

* = Estimated N/A = Not Available

** = Modeled Data. If value range given for θ ja, lower value is for 3x3 in. 1 oz internal copper gnd plane, higher value is for 1x1 in. gnd plane. All model data assumes only one trace for each non-fused lead.

θja (°C/W) (6)(15)	θjc (°C/W) (15)	Comments
144-172**	38**	Modeled using .3 mm trace widths.
116-138**	36**	Modeled using .3 mm trace widths.
96-118**	33**	Modeled using .3 mm trace widths.
31 (11) 36-52**	8**	Leads 8,9,10,26,27 and 28 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
29 (12) 32-46**	7**	Leads 10,11,12,13,32,33,34 and 35 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .5 mm trace width.
84-160 (3)	42	
50-120 (3)	35	
50-120 (3)	35	
40-70 (3)	22 (2)	Leads 2,3,6 and 7 are fused to the die attach paddle.
36-58 (3)	20 (2)	Leads 4,5,12 and 13 are fused to the die attach paddle. Single layer board used .68 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
50-100 (3)	27	
89-102**	26**	Modeled using .3 mm trace widths.
45-95 (3)	25	
71-83**	24**	Modeled using .3 mm trace widths.
65-76**	21**	Modeled using .3 mm trace widths.
30-50 (3)	16 (2)	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. . Single layer board used 0.165 in^2 of 1 oz copper on top of PWB for heatsinking to fused leads.
83*	3*	
65-75*	3*	
50-87*	3	
65-75*	3	
232-257**	32**	Modeled using .3 mm trace widths.
132-158**	15**	Modeled using .3 mm trace widths.
123-147**	15**	Modeled using .3 mm trace widths.
102-125**	14**	Modeled using .3 mm trace widths.
150 (3) 88-109**	13**	Modeled using .3 mm trace widths.
77-96**	13**	Modeled using .3 mm trace widths.
30-70 (3) 63-87**	20 (2) 9**	Leads 5,6,7,8,17,18,19 and 20 are fused to the die attach paddle. Empirical tests used 1.1 in^2 of 1 oz top copper on top of PWB for heatsinking to fused leads. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.
33 (13) 61-80**	20 (2) 11**	Leads 8 and 21 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead gnd plane and .3 mm trace width.
30-70 (3) 57-79**	20 (2) 9**	Leads 7,8,9,20,21 and 22 are fused to the die attach paddle. Modeled with 2 thermal vias to gnd plane per fused lead and .3 mm trace width.

Package Thermal Resistance Data

Databook numbers for thermal resistance are for reference in making relative package-to-package performance comparisons and are not a statement of absolute performance in a system application.

Notes:

1) All data assumes testing with the long side of the die coinciding with the long side of the die attach mounting area.
2) Specified thermal resistance is jl (junction to lead) where noted.
3) Specified θja (junction to ambient) is for devices mounted to 5 in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in^2 aluminum PC board. Test PWB was .062 in thick and typically used 0.635 mm trace widths for power pkgs and 1.3 mm trace widths for non-power pkgs with a 100x100 mil probe land area at the end of each trace - see *Thermal Characteristics of Surface Mounted Packages* by John O'Connor.
4) Lower value is for 5 in^2 multi-layer PC board. The multi layer PWB was .062 in. thick and typically used 0.635 mm trace widths for power pkgs, 1.3 mm trace widths for non-power pkgs with a 100x100 mil probe land area at the end of each trace. The backside of the PWB used 1.0 mm traces in the X and Y directions to simulate 20% coverage by multilayer traces. Thermal vias were not used to connect fused leads to backside traces. - see "Thermal Characteristics of Surface Mounted Packages" by John O'Connor.
5) Lower value is with a finned heatsink.
6) θja tests were performed in still air. θja results will vary depending on test conditions and setup. Airflow can lower the θja value stated by 15-30%, depending on air speed, package type and PWB configuration.
7) Modeled with no internal gnd plane. Lower value is for .5 mm trace widths, higher value for .3 mm trace widths.
8) θjc data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "*The baseline values shown are worst case (mean + 2s) for a 60x60 mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W*".
9) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.43 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
10) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz. copper internal planes, 10 mil trace widths and 1.53 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
11) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.28 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
12) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz. copper internal planes, 10 mil trace widths and 2.74 in^2 of copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
13) Tested on multi layer 3x4.5x.062 in. PWB with (2) 1 oz copper internal planes, 10 mil trace widths and 2.2 in^2 of 1 oz. copper on top of PWB for heatsinking to fused leads. Thermal vias were not used to connect fused leads to inner copper planes.
14) Trace width for test PWBs is typically 10 mils.
15) Test conditions typically use a 110-125C junction temperature with an ambient temperature of 25-30°C.
16) Die size noted is for a thermal test die with a uniformly distributed heating area.

Typical Materials Used for Assembly

Package	Unitrode Package Code	Die Thickness (mils)	Die Attach (2)	Leadframe Material Thermal Conductivity (1)	Molding Compound or Package Material
Ceramic DIP	J	15	Eutectic or Silver Glass	75	Alumina
Ceramic LCC	L	15	Eutectic or Silver Glass	N/A	Alumina
Ceramic LCC Power	LP	15	Eutectic or Silver Glass	N/A	Alumina
LQFP	FQ	12	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
LQFP Power	FQP	12	Silver Filled Epoxy	220	Standard, non-thermally enhanced epoxy
PDIP	N	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
MSOP	P	8	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PDIP Power	NP	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
PLCC	Q	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
PLCC Power	QP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
QSOP	M	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
QSOP Wide Body Power	MWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Narrow Body	D	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Narrow Power	DP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
SOIC Wide Body	DW	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
SOIC Wide Body Power	DWP	12	Silver Filled Epoxy	208	Standard, non-thermally enhanced epoxy
TO220	T	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TO263	TD	12	Silver Filled Epoxy	150	Standard, non-thermally enhanced epoxy
TSSOP	PW	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy
TSSOP Power	PWP	10	Silver Filled Epoxy	85-110	Standard, non-thermally enhanced epoxy

Note (1): $\frac{BTU \bullet in}{ft^2 \bullet hr \bullet ^\circ F}$.

Leadframe downset is typically 8 to 15 mils. Leadframe thickness is typically 5-10 mils.

Note (2) :Die attach thickness is between 0.5-1.5 mils for plastic devices; 1.9-2.4 mils for ceramic.

Table 1. Typical materials used for assembly.

UNITRODE

THERMAL CHARACTERISTICS OF SURFACE MOUNT PACKAGES

John A. O'Connor

Introduction

Surface mount packaging continues to expand market share, displacing dual in-line packages (DIPs) at an ever increasing rate. Smaller surface mount devices allow a significant increase in circuit density with a corresponding decrease in system size. Miniaturization is not without penalty however, as thermal management can quickly dominate system packaging design.

With the familiar DIP, the majority of heat is removed through the case. Typically, this is accomplished by convection air currents, although forced air or conduction cooling is often used in more demanding applications. Unlike the DIP however, the majority of heat is removed from surface mount packages through the leads. This means that the PC board design directly affects the thermal capability of surface mounted circuitry. For optimal thermal design, the integrated circuit, the package, and the PC board must be considered as a system.

Many designers use steady-state thermal behavior (thermal resistance) to predict IC junction temperature. While this approach certainly is valid for devices subjected to continuous power dissipation, it often results in an overly conservative design when dissipation varies over time. Generating a model which accounts for transient thermal behavior allows the designer to fully exploit the system's thermal mass. Instantaneous junction temperature can then be calculated, insuring reliability with minimal system size.

Thermal Model

Figure 1 shows the basic model which is expanded for more complex situations. The power dissipated is represented by the current source. Resistance to heat flow is represented by the resistor, and the thermal mass is represented by the capacitor. The analogous thermal units for the current, thermal resistance, and thermal capacitance are also shown in figure 1. Ground is ambient temperature, so all values are temperature rise above ambient. With more complex systems, it is usually easiest to initially convert to electrical units, analyze the circuit, then convert back to thermal units. This approach allows standard electrical circuit analysis tools and techniques to be used without unnecessary confusion.

A surface mounted device on a PC board can be modeled as in figure 2. Each R-C section roughly

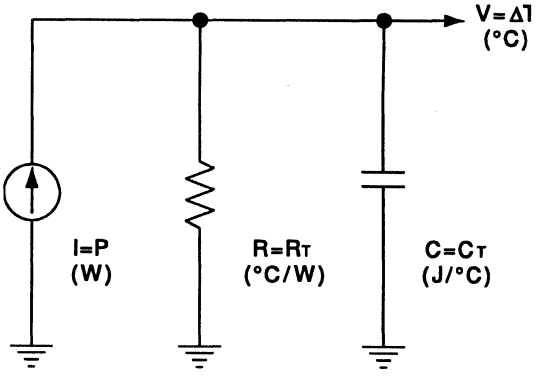


Figure 1. Basic Thermal Model

correlates to the physical system. The first R-C is the device die. The second is the lead frame and package, and the third is the PC board. Other parameters such as the junction to case and case to ambient thermal resistances, are lumped into the three R-C sections. This simplification does cause transient thermal response errors, although normally these errors are small. The additional elements can be broken out separately if greater accuracy is required. Although the physical correlation is far from perfect for the 3 R-C model, the thermal correlation can be very good.

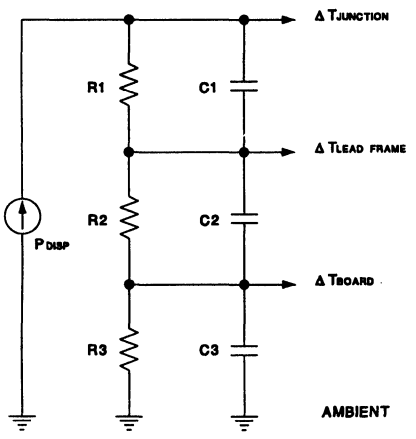


Figure 2. Surface Mounted Device on a PC Board Model

Parameter Measurement

The circuit technique shown in figure 3 can be used to evaluate the thermal performance of almost any IC. Device power dissipation must be known and constant. This is achieved with resistive loading for devices such as voltage regulators or amplifiers. Other devices may require additional circuitry to insure constant dissipation.

The change in forward voltage of a diode is typically utilized for temperature measurement, although any temperature dependant parameter could also be used. Ideally, the diode should be close to the output transistors for maximum accuracy. In practice, this is not critical since the temperature drop across the die will only be a few degrees C in a surface mountable IC. During the test, the measurement diode must not have any current other than the fixed bias current. The bias current should be as small as possible to avoid self-heating the diode.

Many devices have a diode intended for forward biased operation in the actual application circuit such as an output stage clamping diode. If such a diode is not available it may be necessary to forward bias a parasitic diode for measurement. While this approach should be considered a last resort, it can yield acceptable data. If a parasitic diode is forward biased, erratic or unspecified behavior is likely, even with low bias currents. Evaluate the test circuit carefully, insuring that dissipation is constant over the measurement temperature range.

Kelvin all connections to avoid interconnect voltage drops. Every 2mV is approximately 1°C, so even small DC offsets can cause significant error. Without any power applied to the device other than the diode bias current, characterize the diode's forward voltage in an oven at several temperatures over the expected operating junction temperature range. The slope of a best-fit line gives the thermal coefficient (T_C) which is used in subsequent calculations.

Thermocouples are used to sense PC board and ambient temperature. PC board temperature is measured as close to the device as possible.

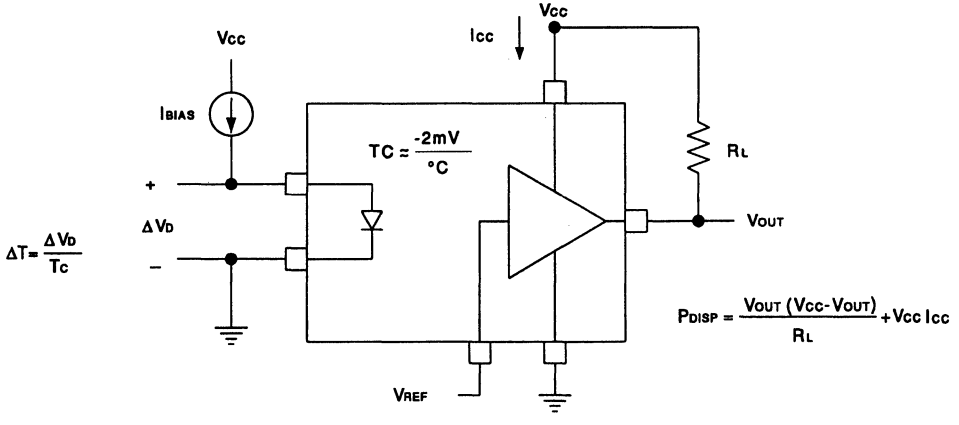


Figure 3. Typical Thermal Test Circuit

Some parameters are measured directly while others are derived by curve fitting. Junction to PC board, and PC board to ambient thermal resistance are measured by dissipating a constant power. Allow 15 minutes for the temperature to stabilize. The change in diode forward voltage and PC board temperature give the junction to ambient and board to ambient thermal resistance:

$$R_{(j\text{-}a)} = \Delta V_D / (T_C P_{DISP})$$
$$R_{(b\text{-}a)} = \Delta T_B / P_{DISP}$$

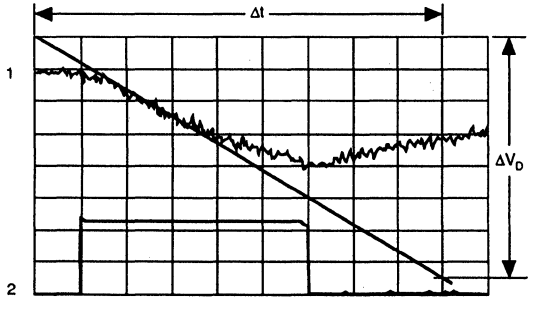
Note that these resistances are based on change in temperature - ambient is assumed constant for the duration of the test. These values correlate to R1, R2, and R3 by:

$$R1 + R2 = R_{(j\text{-}a)} - R_{(b\text{-}a)} \quad (1)$$

$$R3 = R_{(b\text{-}a)} \quad (2)$$

The thermal capacitance of the die is measured by applying a pulsed load and recording the junction temperature waveform. Varying the dissipation pulse width allows observation of each capacitance's effect, although only the die's thermal capacitance can be measured directly. A typical 10ms transient dissipation waveform is shown in figure 4. The thermal time constant of the die is on the order of 30ms. To minimize exponential decay error, the slope of the waveform is measured at (t) = 3ms. The die's thermal capacitance is then:

$$C1 = P_{DISP}\, \Delta t\, T_C / \Delta V_D \quad (3)$$



VERTICAL: (1) V_D, 1mV/DIV
(2) P_{DISP}, 1W
HORIZONTAL: 2ms/DIV

Figure 4: 10ms Transient Dissipation Waveform

Transient waveforms should also be taken for 100ms, 1s, and 10s dissipation intervals to generate an accurate temperature versus time curve. If transient thermal behavior is critical beyond 10 seconds then additional curves must be taken. The thermal time constant of the PC board can go out to several minutes, so a strip chart recorder or computer based data acquisition system will be required. For most systems, this additional data is unnecessary.

The remaining parameters are determined by curve fitting. Visual comparison of measured versus calculated curves is easily done with a spread sheet program. Measured junction temperature versus time data (4 points per decade is sufficient) is entered into the spread sheet. Junction temperature is then calculated at each point with estimated values for R2 and C2 and C3 using:

$$T(t) = P_{DISP}\,[R1(1-e^{-t/\tau 1}) + R2(1-e^{-t/\tau 2}) + R3(1-e^{-t/\tau 3})] \quad (4)$$

Data presented in the following section will help in estimating initial values. This procedure is iterated until an acceptable curve fit is achieved. C3's value is iterated only if the measured curve goes out to several minutes. Figure 5 is a typical measured and calculated junction temperature versus time curve. A logarithmic time axis aids in curve fitting by spreading data points evenly.

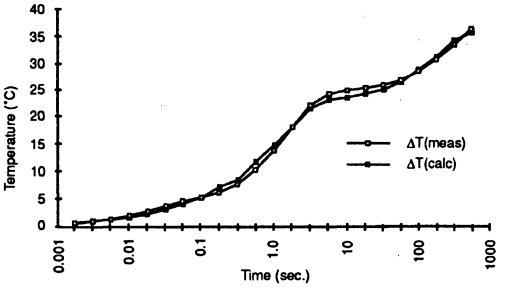


Figure 5. Juction Temperature versus Time for FQP48 Package Dissipating 1W.

Typical Data

The preceding technique was used to characterize two devices in nine different packages. Five different PC board types were also tested to provide relative comparison. This information should be used to help initially determine package, PC board type, and layout. It must be stressed that this typical data should not substitute for a rigorous thermal analysis of the actual application.

PACKAGE	R1 (°C/W)	C1 (J/°C)	τ1 (sec)	R2 (°C/W)	C2 (J/°C)	τ2 (sec)	R3 (°C/W)	C3 (J/°C)	τ3 (sec)	R(J-a) (°C/W)
D8	5	0.0035	0.02	64	0.030	1.9	15	24	360	84
D14	4	0.0045	0.02	45	0.035	1.6	16	24	384	65
DW16	4	0.0045	0.02	44	0.070	3.1	15	24	360	63
DW16	4	0.011	0.04	34	0.11	3.7	13	24	312	51
DWP28	2.5	0.008	0.02	13	0.13	1.7	15	24	360	30
Q20	3	0.010	0.02	26	0.12	3.1	14	24	336	43
Q28	2.5	0.008	0.02	25	0.12	2.9	13	24	312	40
QP28	2.5	0.009	0.02	12	0.25	3.0	14	24	336	28
FQ48	4	0.006	0.02	57	0.07	4.0	15	24	360	76
FQP48	4	0.005	0.02	21	0.08	1.7	14	25	350	39

Figure 6. Model Values Versus Package Type for 1W Dissipation on Aluminum PC Board.

Figure 6 shows model values and time constants versus package type, mounted on an aluminum PC board [1]. Junction to ambient thermal resistance is also shown to indicate overall steady state thermal performance. All data was taken with one watt dissipated. The values that were determined by curve fitting result in a fairly conservative model. Values were chosen which tended to predict higher temperature than actually measured where errors could not be eliminated. As indicated, two devices were used for testing. At 7,500 square mils, the UC3730 is representative of the smaller dies typically packaged in D8, D14, and DW16 packages. The UC3173 is 16,500 square mils, and is typical of the dies packaged in the other larger packages.

Both devices were packaged in the DW16 to isolate the effect of die size. The UC1730's smaller die increased R2 by about 30%. Interpolating between these two data points is difficult since the relationship between die size and thermal resistance is nonlinear. Curves are available which account for this dimensional difference [2], although the actual conditions differ and are more complicated than the configuration used to generate the curves. Fortunately, the resulting error will be small in most applications. Conservatively estimating R2 will minimally impact system size, but if a more accurate value is required the actual device can be characterized on a test PC board.

Figure 7 illustrates the power lead frame's dramatic improvement in thermal performance over standard lead frames by comparing the junction to ambient thermal resistances of the QP28 to the Q28, and the FQP48 to the FQ48. Standard lead frames connect the die to the leads thermally through the epoxy molding compound. Power lead frame packages incorporate a single piece for die attachment and ground leads. This uninterrupted, high thermal conductivity path offers a significant improvement over standard lead frames. Occasionally a stiffer but less conductive alloy is used for standard lead frames. The FQ48's poorer thermal performance is partially caused by the lower conductivity alloy.

Printed circuit board design significantly affects the overall thermal performance of the system, particularly with the power lead frame packages. The UC3173 in the DWP28 package was used to

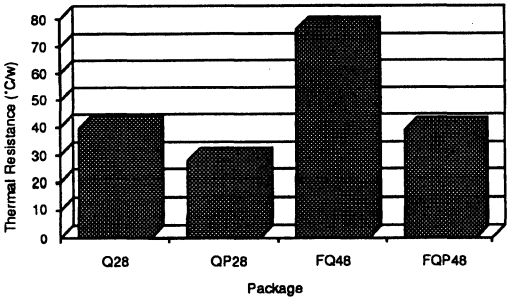


Figure 7. Power lead frames significantly reduce thermal resistance.

compare PC board thermal performance. Five different PC board types were evaluated with one watt dissipated:

1. Single side 1 oz. copper, 0.062 aluminum
2. Single side 1 oz. copper, 0.062 FR4 epoxy fiberglass
3. Single side 2 oz. copper, 0.062 FR4 epoxy fiberglass
4. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.031 FR4 epoxy fiberglass
5. Four layer (signal, ground, Vcc, signal) 1 oz. copper, 0.062 FR4 epoxy fiberglass

PCB TYPE	R(b-a) (°C/W)	C(b-a) (J/°C)	τ (sec)
Aluminum	15	24	360
FR4 -1oz.	31	2.5	78
FR4 -2oz.	25	3	74
4 layer - 0.031	21	4	84
4 layer - 0.062	19	5	94

Figure 8. Board to ambient thermal resistance and capacitance versus PC board type for DWP28 package dissipating 1W.

The thermal resistance, capacitance, and time constants for the five PC boards are shown in figure 8. The PC board layouts used for testing are shown in figure 9. Only the component side is shown for the four layer boards. The back side, which has 10 mil traces on 50 mil centers to provide a typical amount of interconnect copper, and the Vcc plane were unconnected. The inner ground plane is connected to the small component side ground plane through 16 feed-throughs.

As expected, the aluminum PC board's significantly higher specific heat results in nearly an order of magnitude increase in thermal capacitance. Surprisingly the four layer 0.062 board's thermal resistance is nearly as low as the aluminum board's, indicating good heat distribution through the inner planes. Note that although the Vcc plane is unconnected, it does help distribute the heat across the board. Conduction or forced air cooling is necessary to fully exploit the aluminum board's capability.

Summary

A method for accurately modeling the thermal behavior of a surface mounted IC has been presented. The model relies on measured data, insuring excellent correlation to the physical system. Typical thermal behavior of nine different packages and five different PC boards were also presented, indicating relative thermal performance differences. Optimum thermal system design is achievable using the techniques and data presented.

References

1. Thermal Clad insulated metal substrates, The Bergquist Company, 5300 Edina Industrial Blvd., Minneapolis, MN 55439, 612-835-2322
2. R. Tummala, E. Rymaszewski, "Microelectronics Packaging Handbook", Van Nostrand Reinhold, 1989, pp173-179

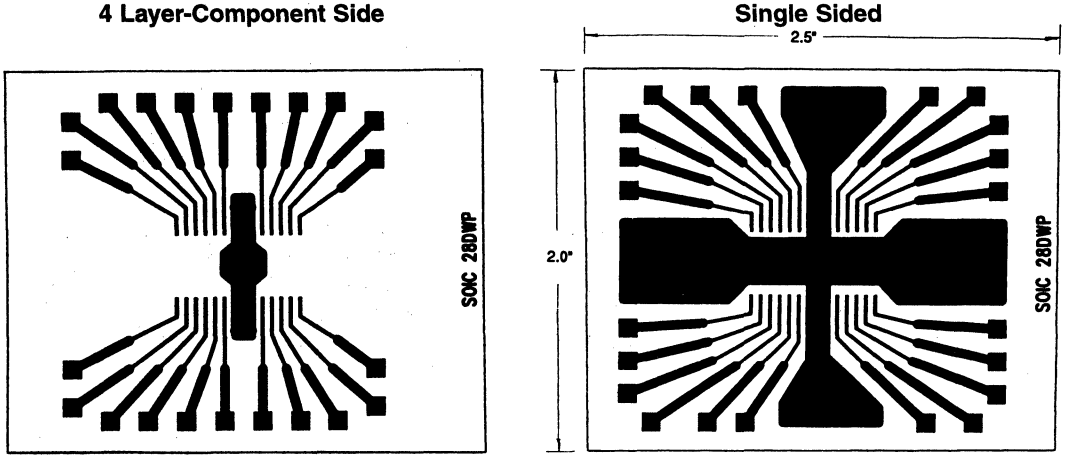
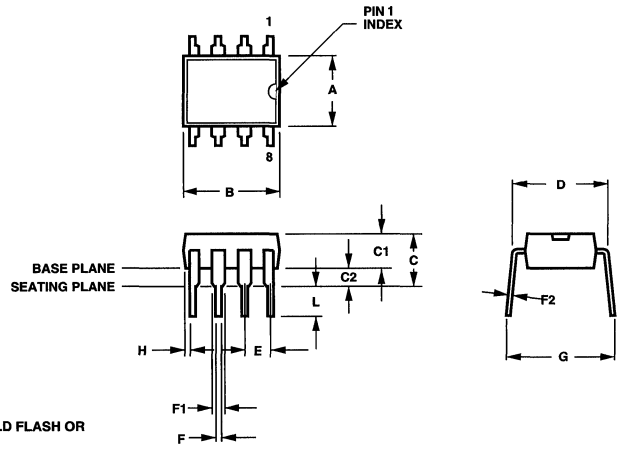


Figure 9. Test PC Board Layouts (SOIC 28DWP)

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

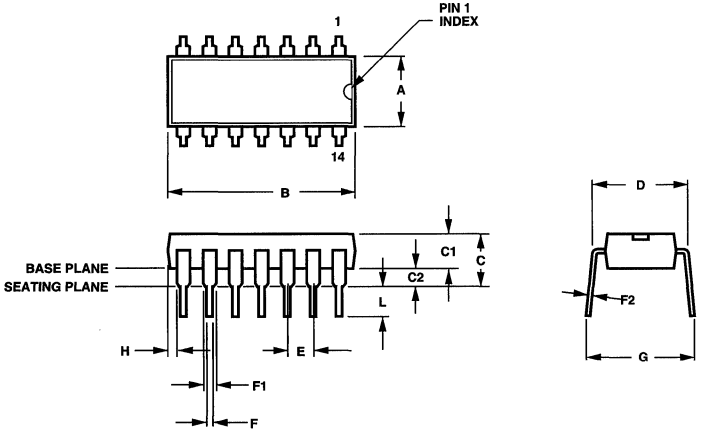
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

14-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



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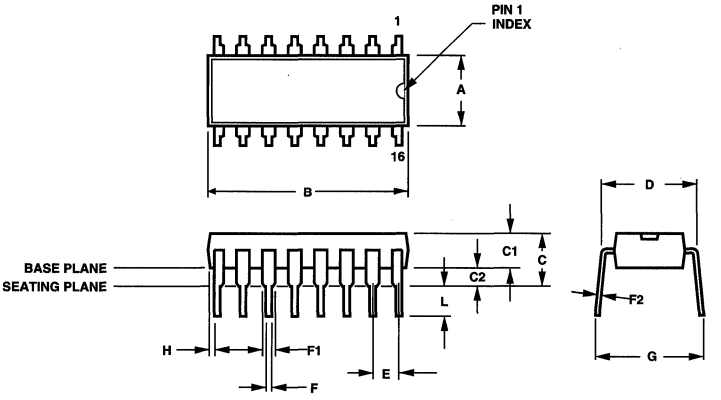
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

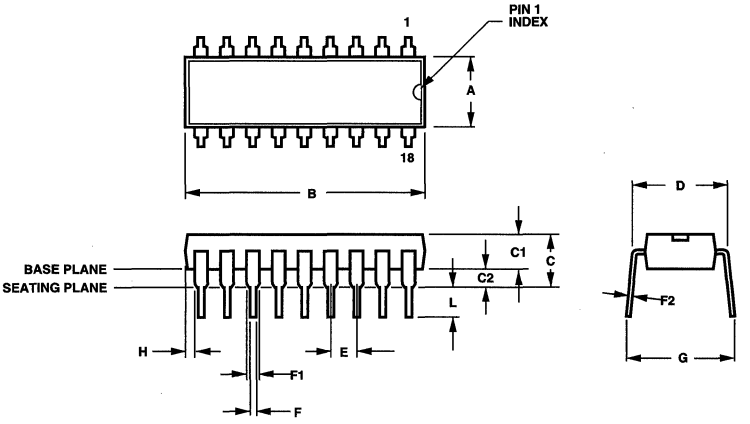
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.745	.775	18.92	19.68	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

18-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

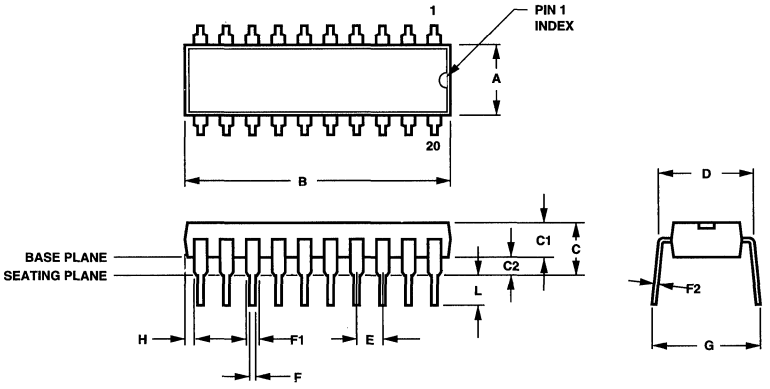
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.890	.920	22.61	23.39	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

20-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

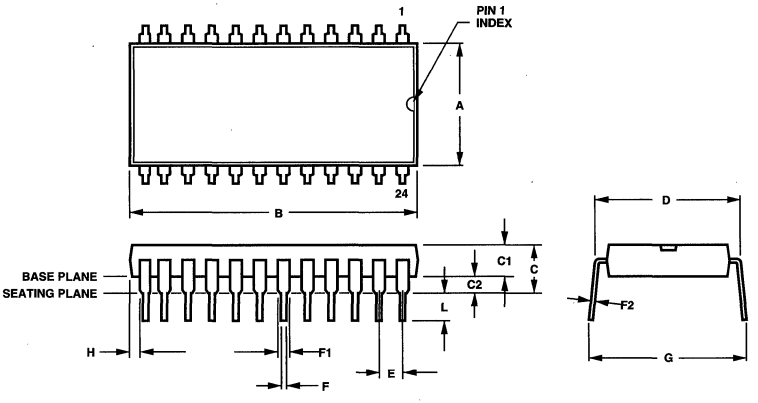
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	1.010	1.030	25.65	26.16	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

24-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

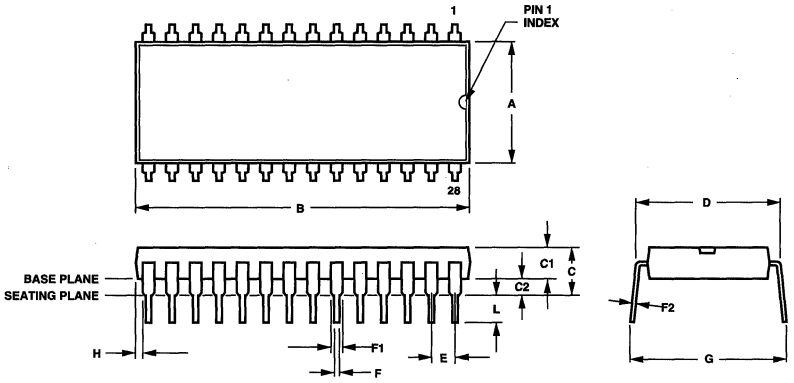
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.230	1.270	31.24	32.26	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

28-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

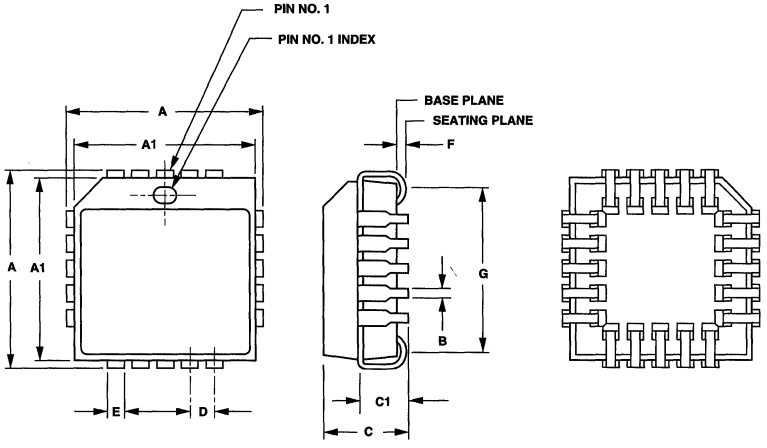
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.500	.550	12.70	13.97	1
B	1.380	1.470	35.10	37.34	1
C	–	.210	–	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.600	.625	15.24	15.87	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.600	.675	15.24	17.15	5
H	.005	–	0.13	–	
L	.115	.160	2.92	4.06	



NOTES:
1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

20-PIN PLASTIC PLCC SURFACE MOUNT ~ Q PACKAGE SUFFIX

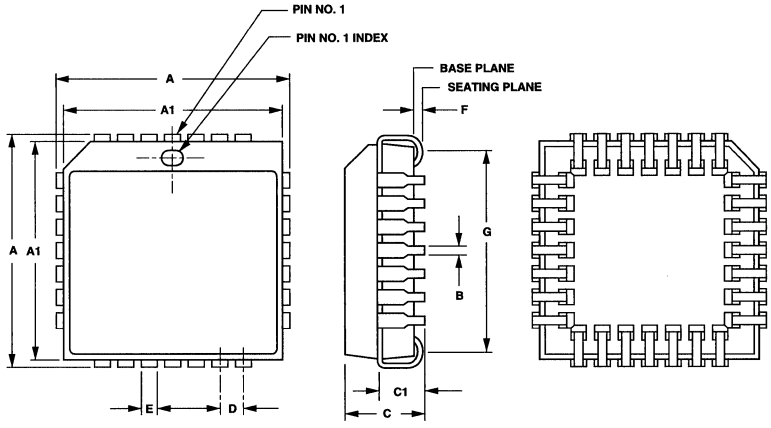
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.385	.395	9.78	10.03	
A1	.350	.356	8.89	9.04	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.290	.330	7.37	8.38	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

28-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

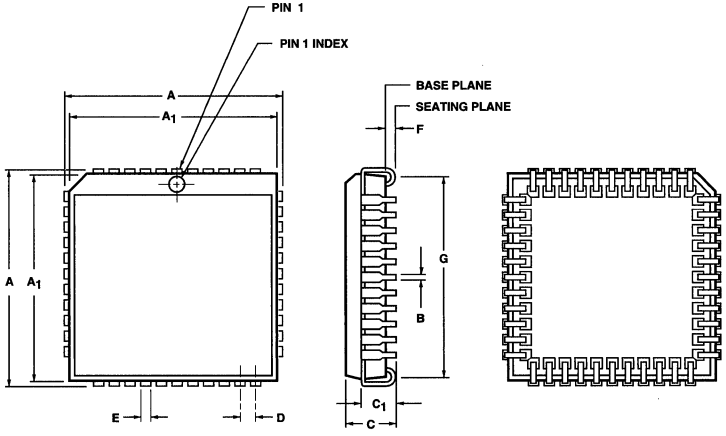
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.485	.495	12.32	12.57	
A1	.450	.456	11.43	11.58	1
B	.013	.021	0.33	0.53	
C	.170	.180	4.32	4.57	
C1	.100	.110	2.54	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3, 4
G	.390	.430	9.91	10.92	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

44-PIN PLASTIC PLCC SURFACE MOUNT ~ Q, QP PACKAGE SUFFIX

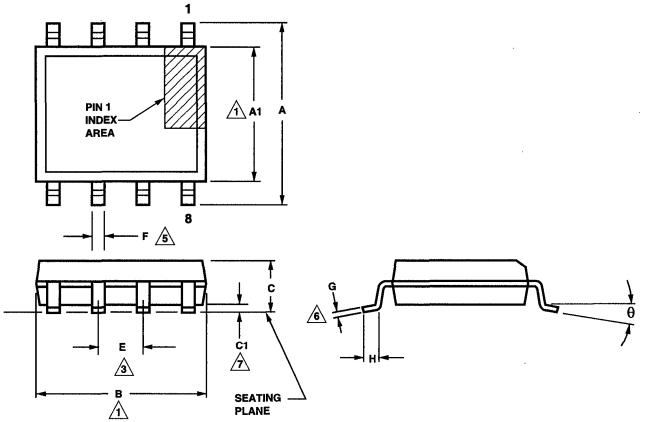
	DIMENSIONS				
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.685	.695	17.40	17.65	
A1	.650	.656	16.51	16.66	1
B	.013	.021	0.33	0.53	
C	.165	.180	4.19	4.57	
C1	.095	.110	2.41	2.79	
D	.050 BSC		1.27 BSC		2
E	.026	.032	0.66	0.81	
F	.020	–	0.51	–	3,4
G	.590	.630	14.99	16.00	



NOTES:
1. 'A1' DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
3. 'F' IS MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

8-PIN SOIC SURFACE MOUNT ~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

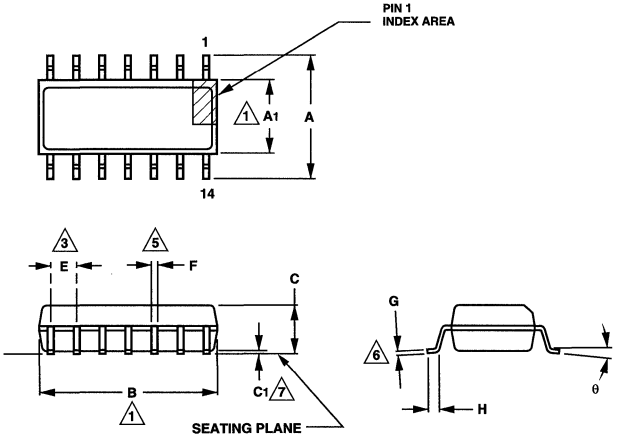


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

14-PIN SOIC SURFACE MOUNT ~ D PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.336	.344	8.55	8.75
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

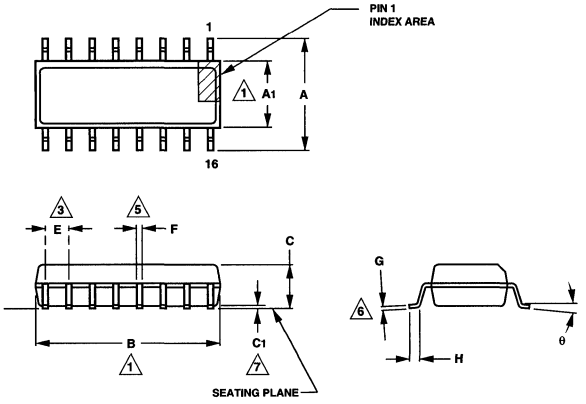


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SOIC SURFACE MOUNT ~ D, DP, DS PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°

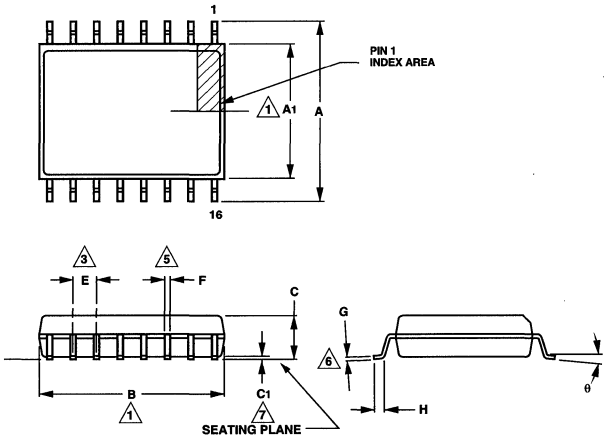


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.403	.413	10.24	10.49
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

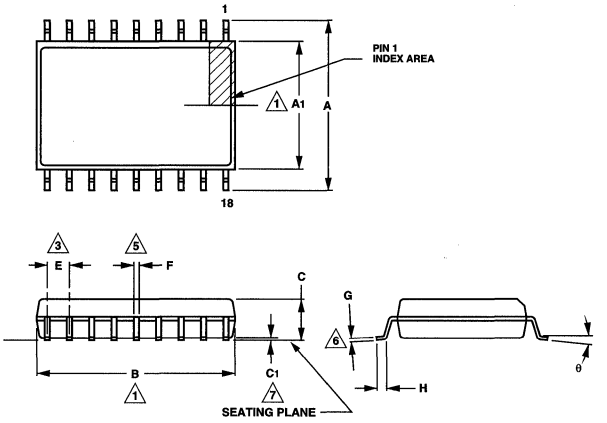


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

18-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.453	.462	11.51	11.73
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

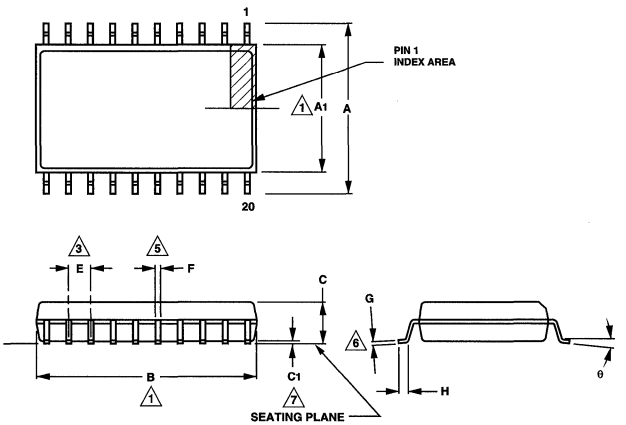


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.504	.511	12.80	12.98
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

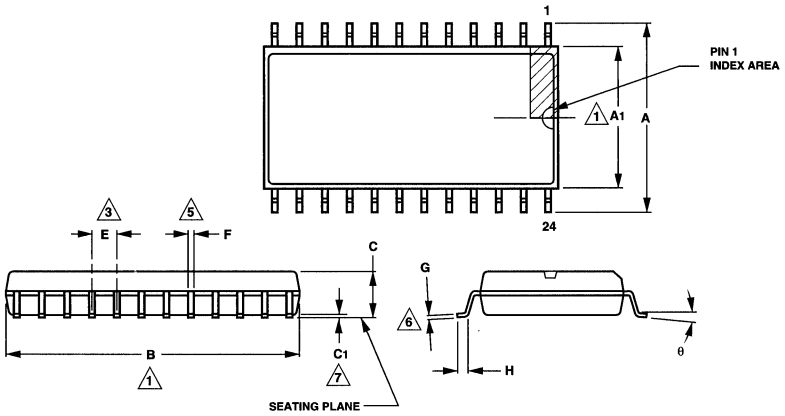


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

24-PIN SOIC SURFACE MOUNT ~ DW PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.598	.606	15.20	15.40
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.019	.035	0.46	0.89
θ	0°	8°	0°	8°

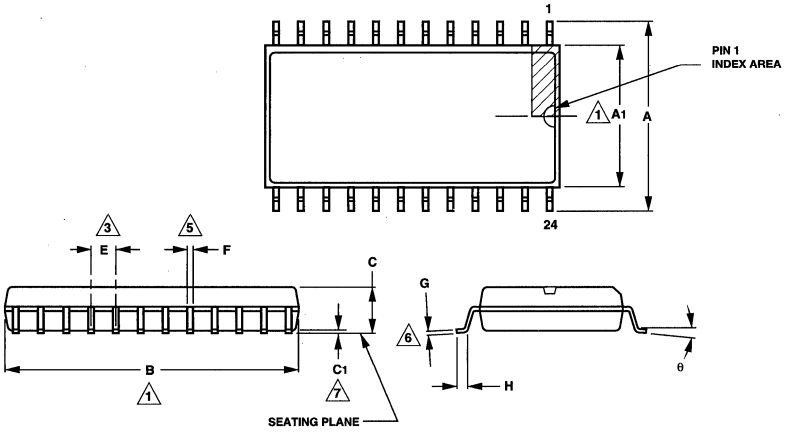


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

28-PIN SOIC SURFACE MOUNT ~ DW, DWP PACKAGE SUFFIX

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.394	.419	10.00	10.64
A1	.292	.299	7.42	7.59
B	.698	.712	17.73	18.08
C	.097	.104	2.46	2.64
C1	.004	.011	0.10	0.28
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.009	.012	0.23	0.30
H	.018	.035	0.46	0.89
θ	0°	8°	0°	8°

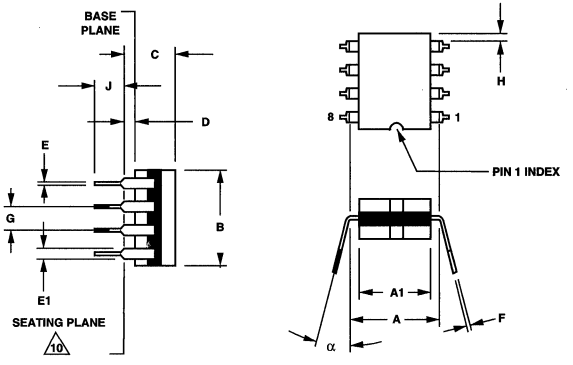


NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.405	—	10.29	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

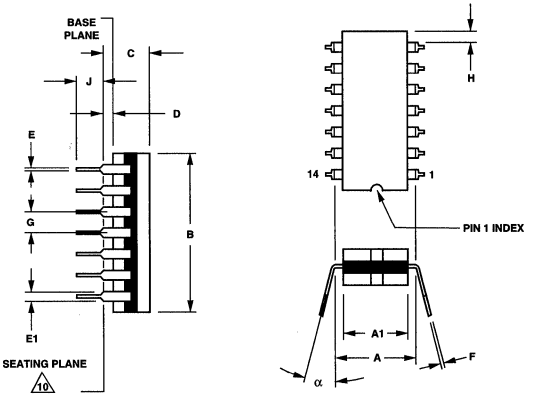


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

14-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.785	—	19.94	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

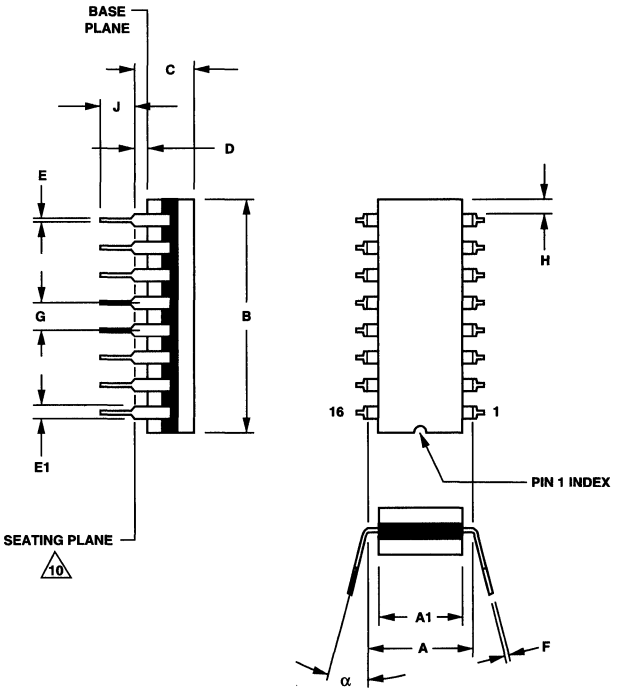


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

16-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.840	—	21.34	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

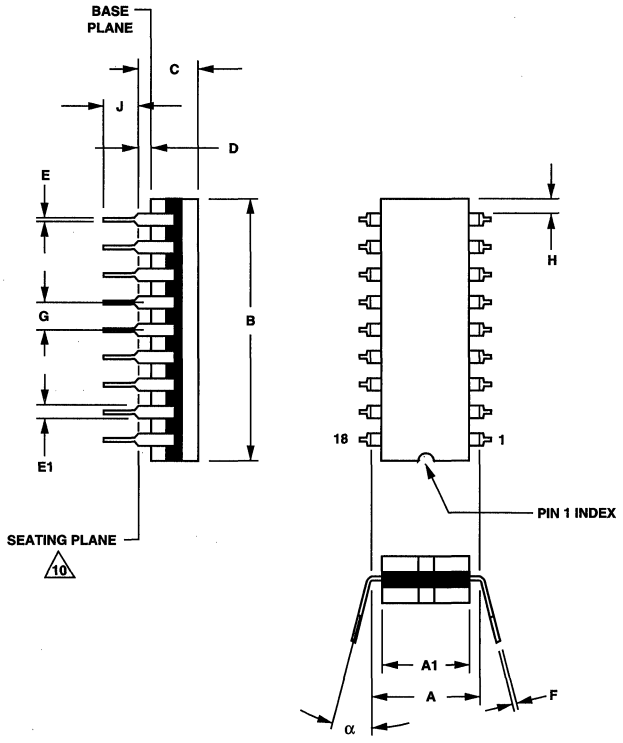


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 8, 9 AND 16 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 8, 9 AND 16).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

18-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	0.960	—	24.38	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



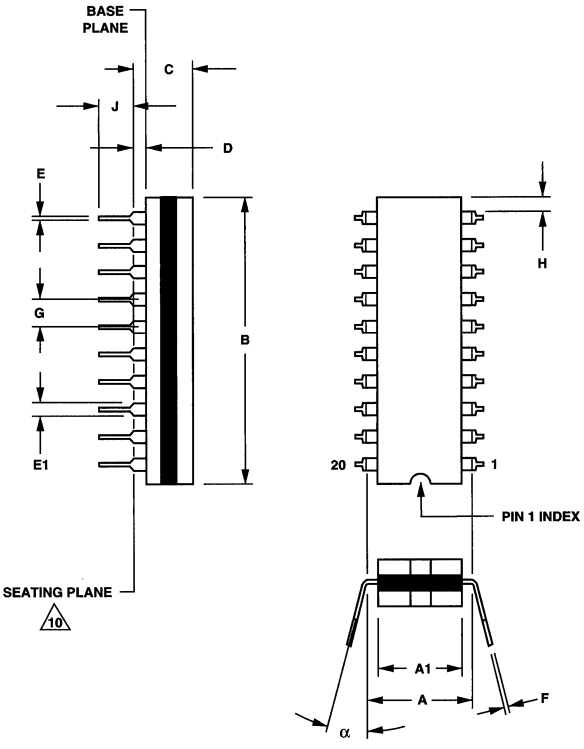
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 9, 10 AND 18 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 9, 10 AND 18).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

20-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	—	1.060	—	26.92	4
C	—	0.200	—	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.13	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



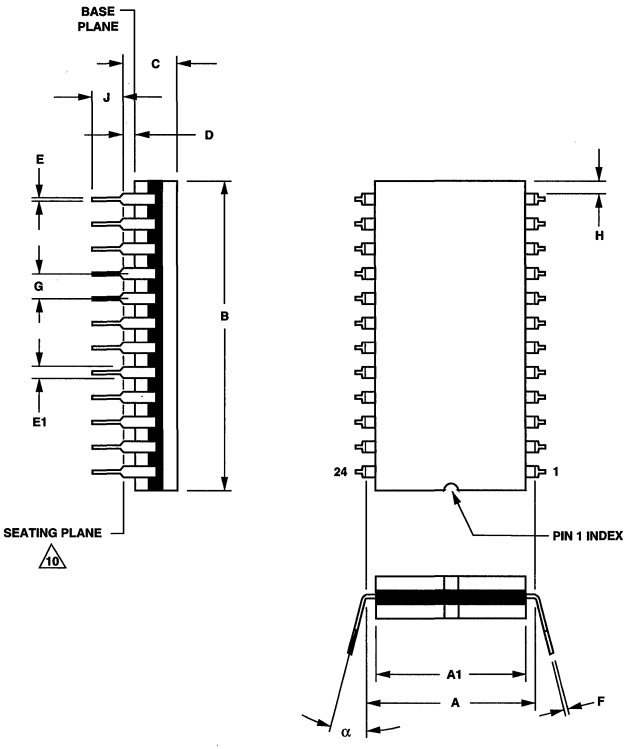
NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 10, 11 AND 20 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 10, 11 AND 20).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY,

10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

24-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.515	0.605	13.08	15.37	4
B	1.180	1.260	29.97	32.00	4
C	—	0.225	—	5.72	
D	0.015	0.055	0.38	1.40	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	0.065	0.127	1.65	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

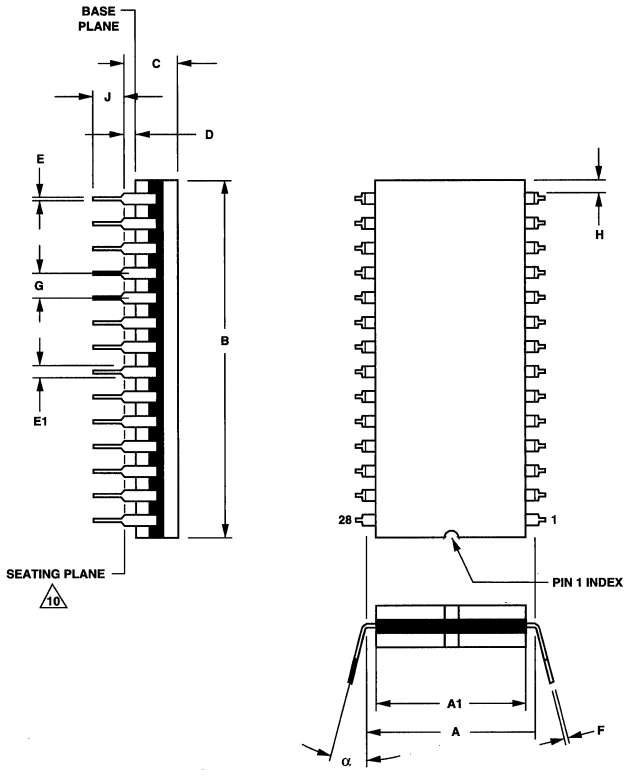


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 12, 13 AND 24 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 12, 13 AND 24).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

28-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.590	0.625	14.99	15.88	7
A1	0.570	0.605	14.48	15.37	4
B	1.380	1.460	35.05	37.08	4
C	—	0.225	—	5.72	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	—	0.127	—	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	

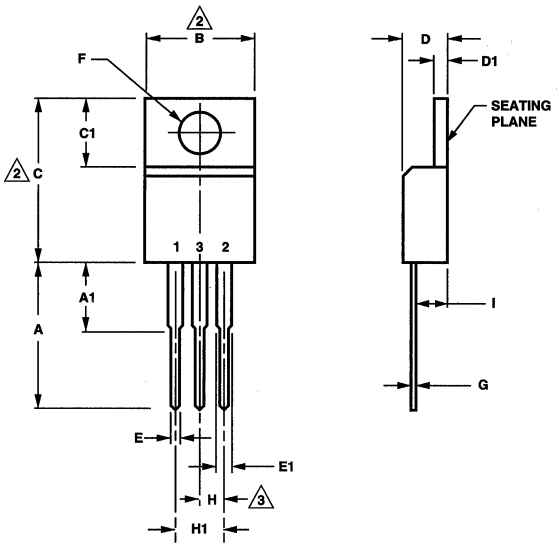


NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENT IFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION "E1" MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 14, 15 AND 28 ONLY.
3. DIMENSION "D" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 14, 15 AND 28).
7. DIMENSION "A" SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS "E" AND "F" SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.

3-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.562	12.70	14.27
A1	–	.250	–	6.35
B	.380	.420	9.66	10.66
C	.560	.625	14.23	15.87
C1	.230	.270	5.85	6.85
D	.140	.190	3.56	4.82
D1	.045	.055	1.14	1.39
E	.020	.045	0.51	1.14
E1	.045	.070	1.14	1.77
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.090	.110	2.29	2.79
H1	.190	.210	4.83	5.33
I	.080	.115	2.04	2.92

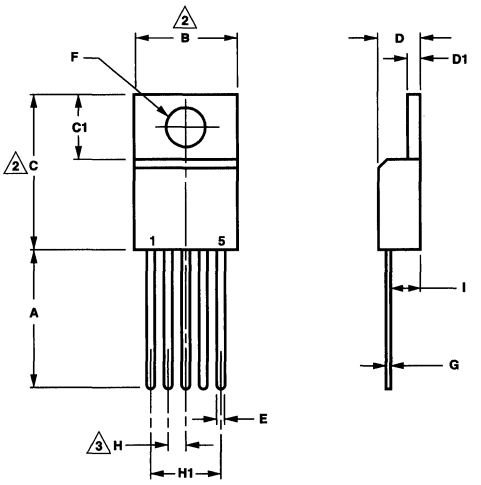


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

5-PIN TO-220 PLASTIC ~ T PACKAGE SUFFIX

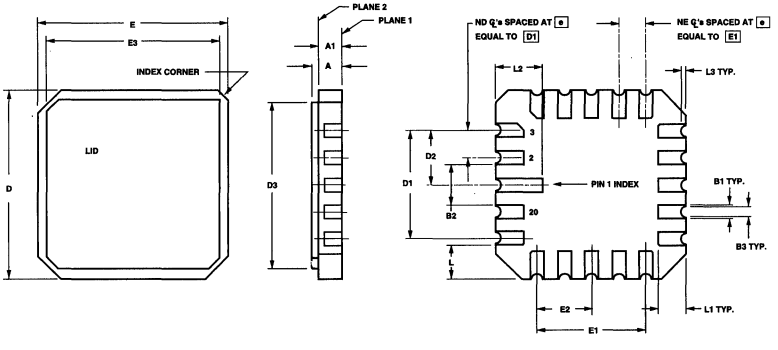
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.500	.580	12.70	14.73
B	.380	.420	9.65	10.67
C	.560	.650	14.22	16.51
C1	.230	.270	5.84	6.86
D	.140	.190	3.56	4.83
D1	.045	.055	1.14	1.40
E	.020	.045	0.51	1.14
F	.139	.161	3.53	4.09
G	.014	.022	0.36	0.56
H	.057	.077	1.45	1.96
H1	.258	.278	6.55	7.06
I	.080	.115	2.03	2.92



NOTES:
1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'B' AND 'C' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.067 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.

20-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

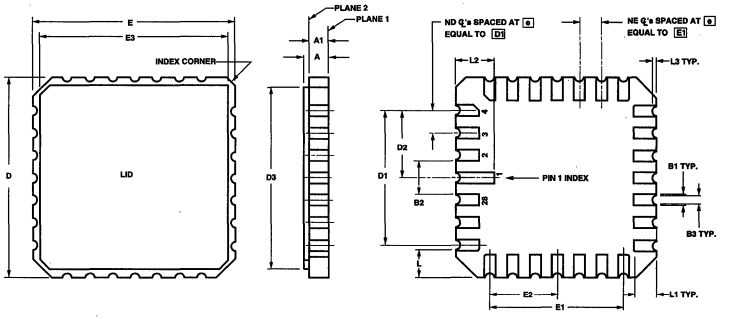
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.342	.358	8.69	9.09	
D1/E1	.200 BSC		5.08 BSC		
D2/E2	.100 BSC		2.54 BSC		
D3/E3	–	.358	–	9.09	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	20		20		2
ND/NE	5		5		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ L PACKAGE SUFFIX

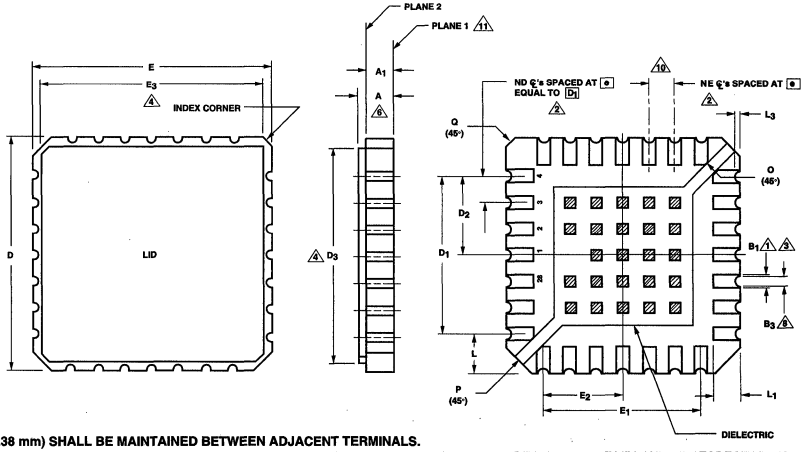
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	.060	.100	1.52	2.54	6
A1	.050	.088	1.27	2.24	
B1	.022	.028	0.56	0.71	1, 3
B2	.072 REF.		1.83 REF.		
B3	.006	.022	0.15	0.56	8
D/E	.442	.460	11.23	11.68	
D1/E1	.300 BSC		7.62 BSC		
D2/E2	.150 BSC		3.81 BSC		
D3/E3	–	.460	–	11.68	4
L	.045	.055	1.14	1.40	
L1	.045	.055	1.14	1.40	
L2	.075	.095	1.90	2.41	5
L3	.003	.015	0.08	0.38	
N	28		28		2
ND/NE	7		7		2
e	.050 BSC		1.27 BSC		10



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BELOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

28-PIN CERAMIC LEADLESS SURFACE MOUNT ~ LP PACKAGE SUFFIX

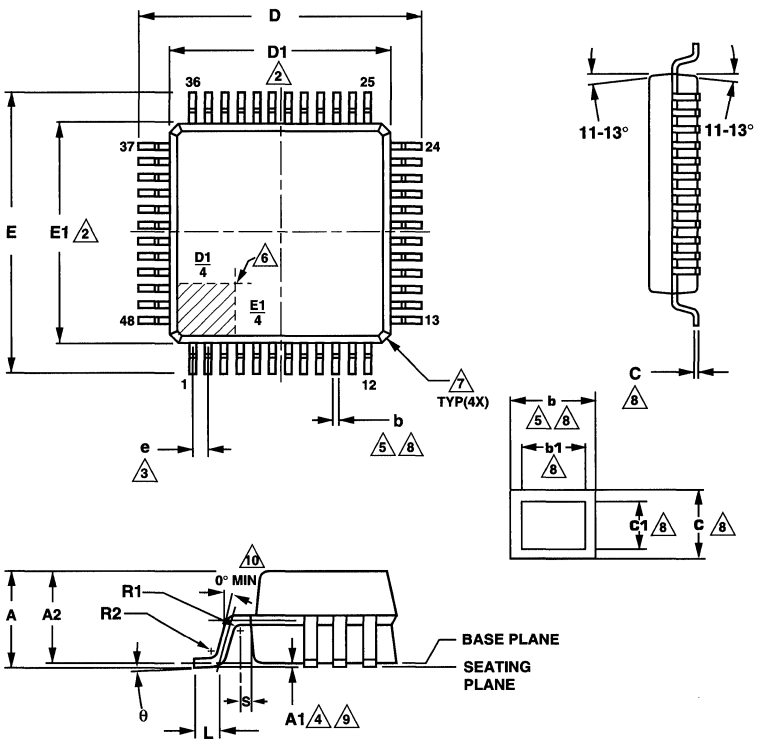
DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.060	.100	1.52	2.54
A1	.050	.088	1.27	2.24
B1	.022	.028	0.56	0.71
B3	.006	.022	0.15	0.56
D/E	.442	.458	11.23	11.63
D1/E1	.300 BSC		7.62 BSC	
D2/E2	.150 BSC		3.81 BSC	
D3/E3	–	.460	–	11.68
L	.075 REF		1.905 REF	
L1	.045	.055	1.14	1.40
L3	.003	.013	0.08	0.33
N	28		28	
ND/NE	7		7	
O	.006 REF		0.152 REF	
P	.040 REF		1.016 REF	
Q	.020 REF		0.508 REF	
e	.050 BSC		1.27 BSC	



NOTES:
1. A MINIMUM CLEARANCE OF 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN ADJACENT TERMINALS.
2. 'N' IS THE MAXIMUM QUANTITY OF TERMINAL POSITIONS. 'ND' AND 'NE' ARE THE NUMBERS OF TERMINALS ALONG THE SIDES OF LENGTH 'D' AND 'E' RESPECTIVELY.
3. ELECTRICAL CONNECTION TERMINALS ARE REQUIRED ON PLANE 1 AND OPTIONAL ON PLANE 2. HOWEVER, IF PLANE 2 HAS SUCH TERMINALS THEY SHALL BE ELECTRICALLY CONNECTED TO OPPOSING TERMINALS ON PLANE 1.
4. A MINIMUM CLEARANCE OR 0.015 INCH (0.38 mm) SHALL BE MAINTAINED BETWEEN A METAL LID AND OTHER METAL FEATURES (E.G., PLANE 2 TERMINALS, METALLIZED CASTELLATIONS, ETC.) THE LID SHALL NOT EXTEND BEYOND THE EDGES OF THE BODY.
5. THE INDEX FEATURE FOR NUMBER 1 TERMINAL IDENTIFICATION, OPTIONAL ORIENTATION OR HANDLING PURPOSES SHALL BE WITHIN THE AREA DEFINED BY DIMENSIONS 'B2' AND 'L2' ON PLANE 1.
6. DIMENSION 'A' CONTROLS THE OVERALL PACKAGE THICKNESS.
7. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
8. CASTELLATIONS ARE REQUIRED ON BOTTOM TWO LAYERS. CASTELLATIONS IN THE TOP LAYER ARE OPTIONAL.
9. WHEN SOLDER DIP LEAD FINISH APPLIES, SOLDER BUMP HEIGHT SHALL NOT EXCEED 0.007 INCHES AND SOLDER BUMP COPLANARITY SHALL NOT EXCEED 0.006 INCHES.
10. THE BASIC TERMINAL SPACING IS 0.050 INCHES BETWEEN CENTERLINES. EACH TERMINAL CENTERLINE SHALL BE LOCATED WITHIN ±0.004 INCHES OF ITS EXACT TRUE POSITION.

48-PIN LQFP ~ FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	–	1.60	–	.063
A1	0.05	0.15	.002	.006
A2	1.35	1.45	.053	.057
b	0.17	0.27	.007	.011
b1	0.17	0.23	.007	.009
C	0.09	0.20	.003	.008
C1	0.09	0.16	.003	.006
D	9.00 BSC		.354 BSC	
D1	7.00 BSC		.276 BSC	
E	9.00 BSC		.354 BSC	
E1	7.00 BSC		.276 BSC	
e	0.50 BSC		.020 BSC	
L	0.45	0.75	.018	.030
R1	0.08	–	.003	–
R2	0.08	0.20	.003	.008
S	0.20	–	.008	–
θ	0°	7°	0°	7°

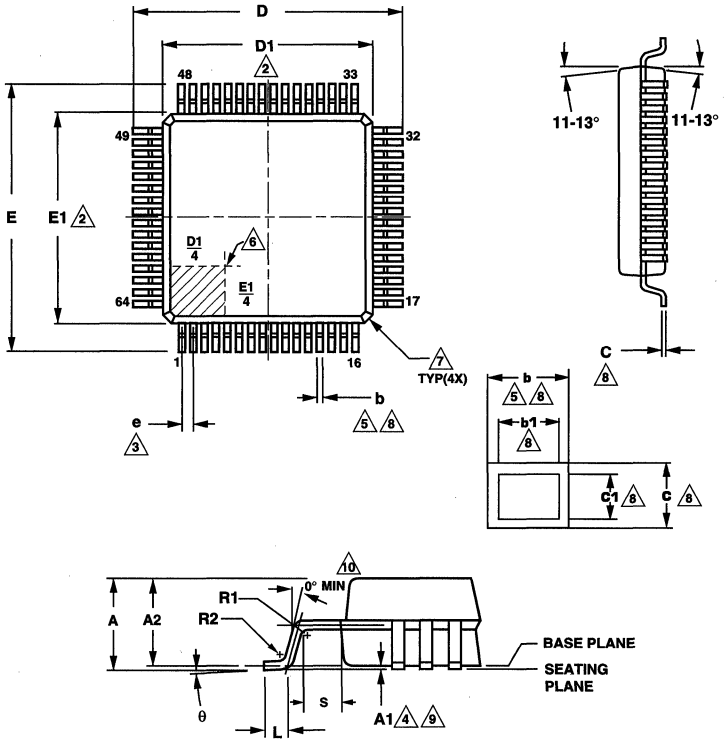


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1' AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1' AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

64-PIN LQFP ~ FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.53	0.57
b	0.17	0.27	0.007	0.011
b1	0.17	0.23	0.007	0.009
C	0.09	0.20	0.004	0.008
C1	0.09	0.16	0.004	0.006
D	12.00 BSC		0.472 BSC	
D1	10.00 BSC		0.393 BSC	
E	12.00 BSC		0.472 BSC	
E1	10.00 BSC		0.393 BSC	
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.18	0.03
R1	0.08	–	0.003	–
R2	0.08	0.20	0.003	0.008
S	0.20	–	0.008	–
θ	0°	7°	0°	7°

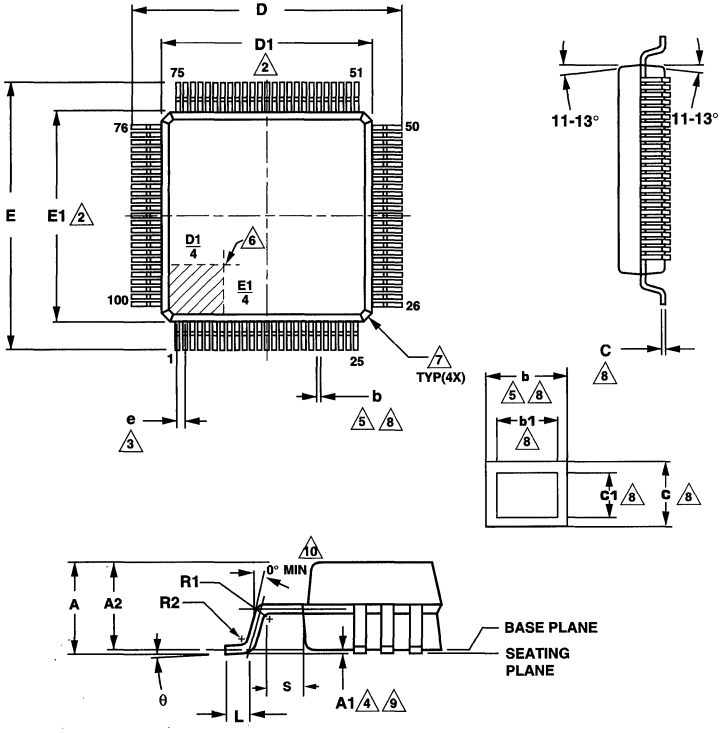


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1'AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1'AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

100-PIN LQFP ~ FQ PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.40	1.60	0.055	0.063
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.53	0.57
b	0.17	0.27	0.007	0.011
b1	0.17	0.23	0.007	0.009
C	0.09	0.20	0.004	0.008
C1	0.09	0.16	0.004	0.006
D	16.00 BSC		0.630 BSC	
D1	14.00 BSC		0.551 BSC	
E	16.00 BSC		0.630 BSC	
E1	14.00 BSC		0.551 BSC	
e	0.50 BSC		0.020 BSC	
L	0.45	0.75	0.18	0.03
R1	0.08	–	0.003	–
R2	0.08	0.20	0.003	0.008
S	0.20	–	0.008	–
θ	0°	7°	0°	7°

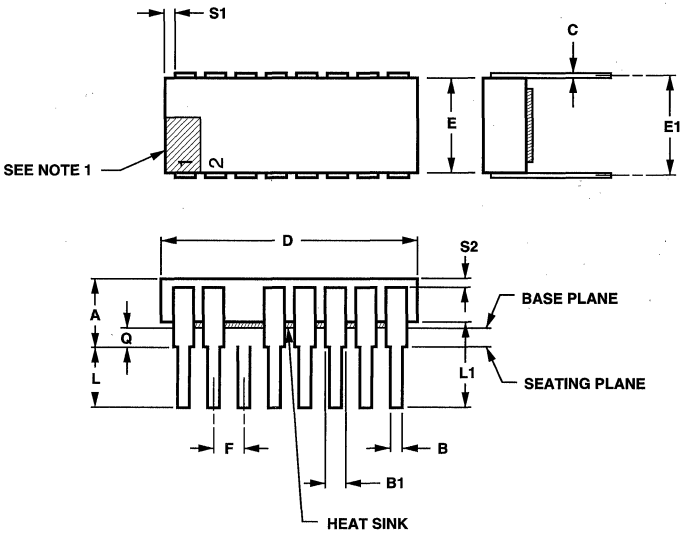


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'D1'AND 'E1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE. 'D1'AND 'E1' INCLUDE MOLD MISMATCH.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. DETAILS OF PIN1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
9. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).
10. THE TOP PACKAGE BODY MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15mm.

16-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.200	–	5.08	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	.840	–	21.34	4
E	.220	.310	5.59	7.78	4
E_1	.290	.320	7.37	8.13	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	

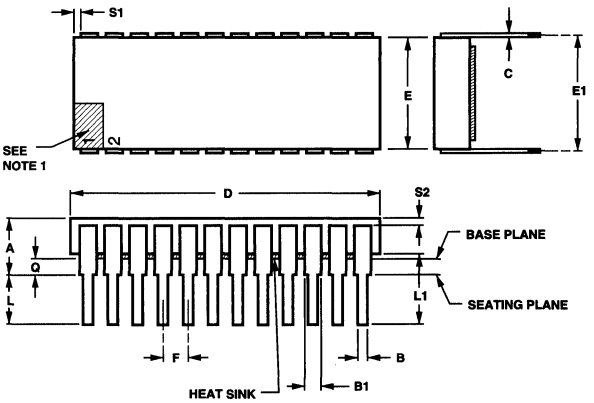


NOTES:

1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN.THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN. (0.58mm) FOR CORNER LEADS.
3. DIMENSION 'Q' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN. (2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN.(0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 14 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSIONS: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

24-PIN SIDEBRAZE DIP ~ SP PACKAGE SUFFIX

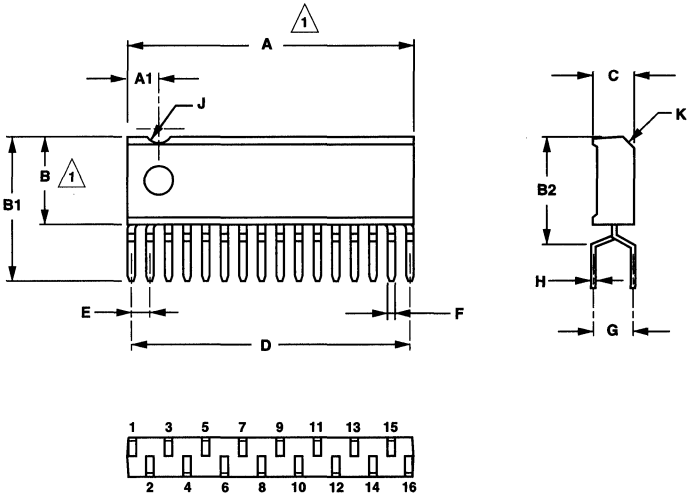
DIMENSIONS					
	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	NOTES
A	–	.225	–	5.72	
B	.014	.023	0.36	0.58	8
B_1	.045	.065	1.14	1.65	2,8
C	.008	.015	0.20	0.38	8
D	–	1.220	–	30.99	4
E	.580	.610	14.73	15.49	4
E_1	.585	.615	14.86	15.62	7
F	.100 BSC		2.54 BSC		5,9
L	.125	.200	3.18	5.08	
L_1	.150	–	3.81	–	
Q	.015	.060	0.38	1.52	3
S_1	.005	–	0.13	–	6
S_2	.005	–	0.13	–	



NOTES:
1. INDEX AREA; A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE AND SHALL BE LOCATED WITHIN THE SHADED AREA SHOWN. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'B1' MAY BE 0.023 IN.(0.58mm) FOR CORNER LEADS.
3. DIMENSION "Q" SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS, AND GLASS OVERRUN.
5. THE BASIC LEAD SPACING IS 0.100 IN.(2.54mm) BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. (0.25mm) OF ITS EXACT TRUE POSITION.
6. MEASURE ALL FOUR CORNERS.
7. E1 SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
8. ALL LEADS - INCREASE MAXIMUM LIMIT BY 0.003 IN. (0.08mm) MEASURED AT THE CENTER OF THE FLAT, WHEN SOLDER DIP IS APPLIED.
9. 22 SPACES
10. BRAZE FILLET SHALL BE CONCAVE.
11. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

16-PIN ZIG-ZAG INLINE ~ Z PACKAGE SUFFIX

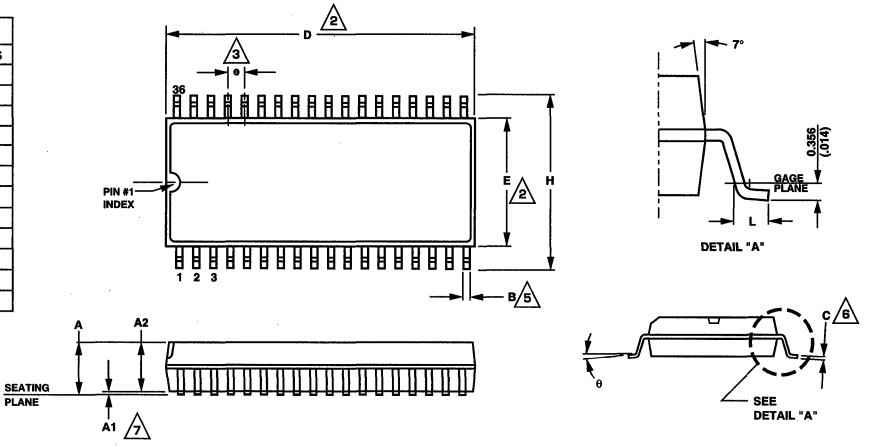
DIMENSIONS					
	MILLIMETERS		INCHES		NOTES
	MIN	MAX	MIN	MAX	
A	19.40	19.60	.764	.772	
A1	–	2.00	–	.079	
B	5.70	5.90	.224	.232	
B1	9.40	10.40	.370	.409	
B2	6.50	7.50	.256	.295	
C	2.70	2.90	.106	.114	
D	18.75	19.35	.738	.762	
E	1.07	1.47	.042	.058	
F	0.45	0.65	.018	.026	
G	2.50	3.00	.098	.118	
H	0.23	0.35	.009	.014	
J	1.00 BSC		.039 BSC		RAD.
K	1.00 BSC		.039 BSC		CHAM.



NOTES:
1. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm (0.006 IN.) PER SIDE.

36-PIN QSOP ~ MWP PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.598	.614	15.20	15.60
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°

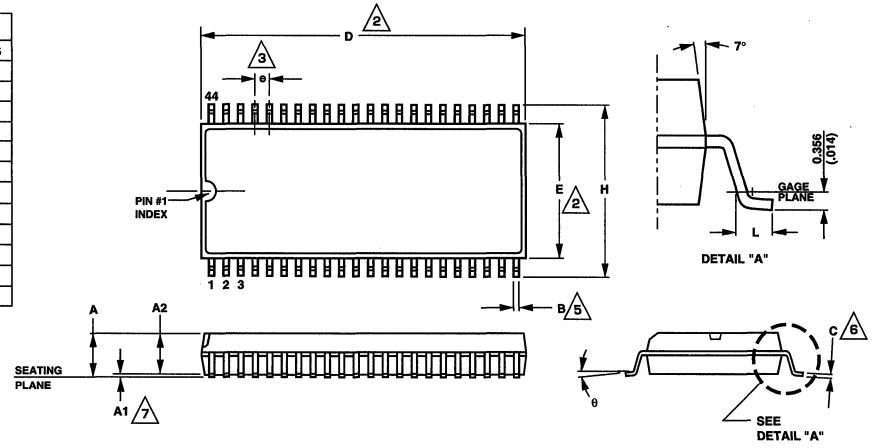


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

44-PIN QSOP ~ MWP PACKAGE SUFFIX

SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.092 TYP		2.34 TYP	
B	.011	.015	0.28	0.39
C	.006	.0125	0.15	0.32
D	.697	.712	17.70	18.10
E	.291	.299	7.40	7.60
e	.031 BSC		0 .80 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	0.40	1.27
θ	0°	8°	0°	8°

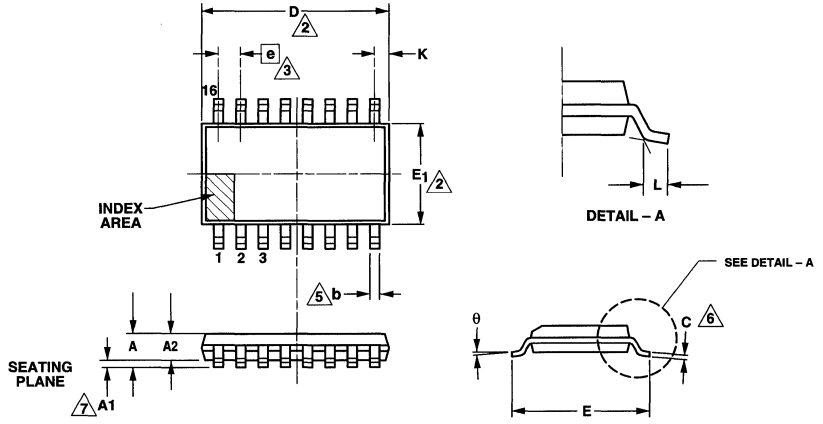


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS CONTROL LEAD PITCH ONLY.
2. 'D' AND 'E' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.80mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.10mm AT THE SEATING PLANE.
5. DIMENSION 'B' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'B' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN QSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.189	.197	4.80	5.00
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.009 REF		.23 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

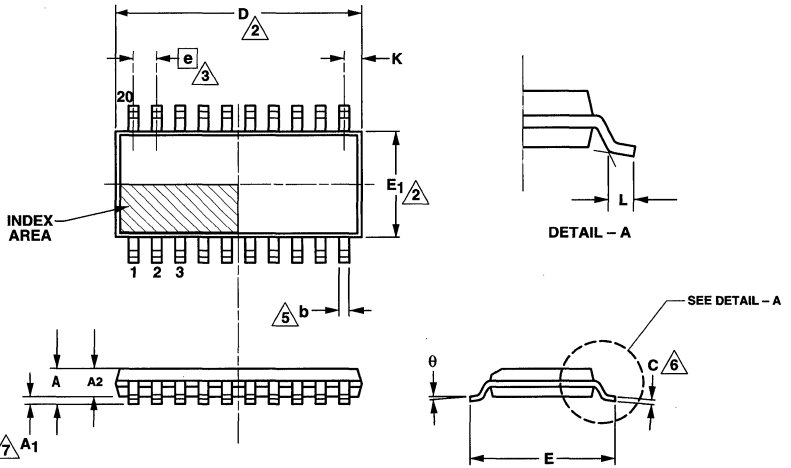


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'b' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN QSOP ~ M PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A_1	.004	.010	.10	.25
A2	–	.059	–	1.50
b	.008	.012	.20	.30
C	.007	.010	.18	.25
D	.337	.344	8.56	8.74
E	.228	.244	5.79	6.20
E_1	.150	.157	3.81	3.99
e	.025 BSC		.635 BSC	
K	.058 REF		1.47 REF	
L	.016	.050	.41	1.27
θ	0°	8°	0°	8°

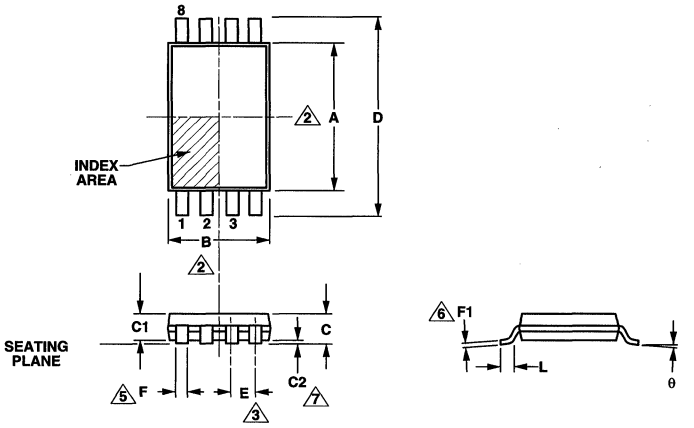


NOTES:

1. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. 'D' AND 'E_1' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
3. THE BASIC LEAD SPACING IS 0.025 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED "b" MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

8-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	2.9	3.1	0.114	0.122
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

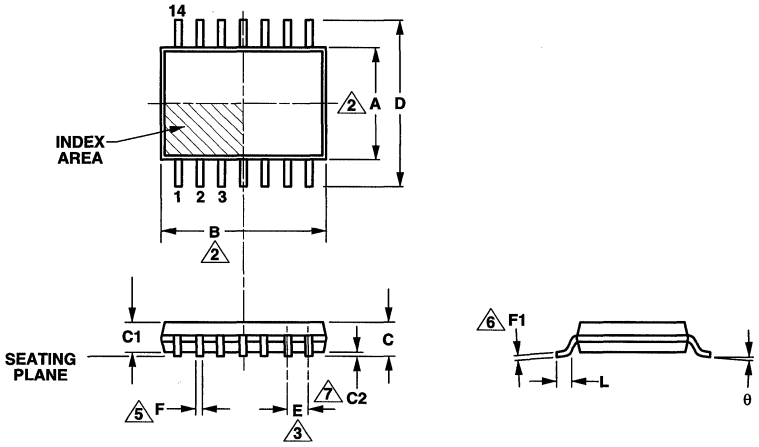


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

14-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

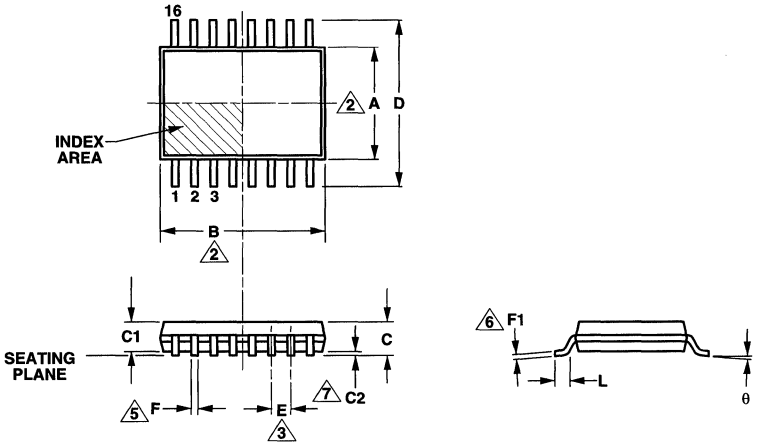


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

16-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.3	4.5	0.170	0.177
B	4.9	5.1	0.193	0.200
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	6.4 BSC		0.252 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.18	0.30	0.007	0.012
F1	0.09	0.18	0.004	0.007
L	0.50	0.70	0.020	0.028
θ	0°	7°	0°	7°

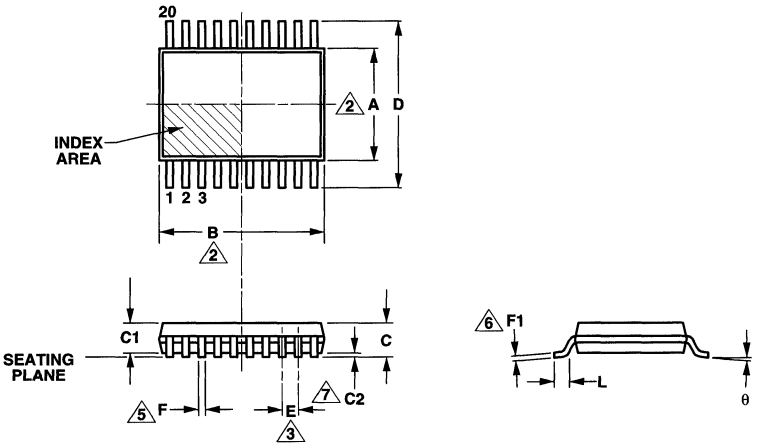


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

20-PIN TSSOP ~ PW PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	6.40	6.60	.252	.260
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°

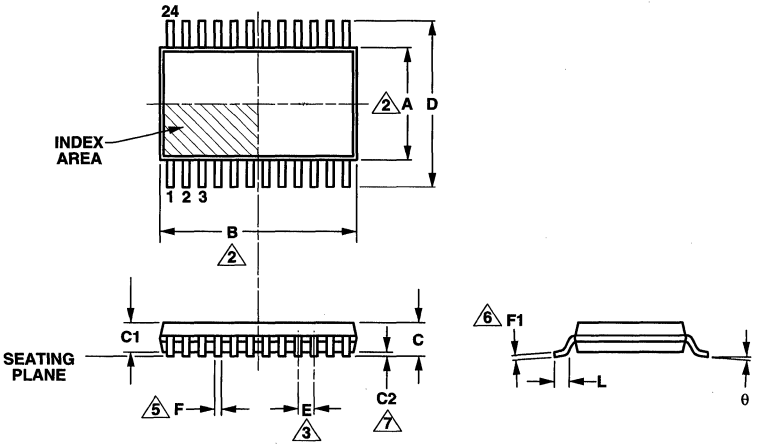


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

24-PIN TSSOP ~ PW, PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	7.70	7.90	.303	.311
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°



NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.

2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.

3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES.
   EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF
   ITS EXACT TRUE POSITION.

4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE

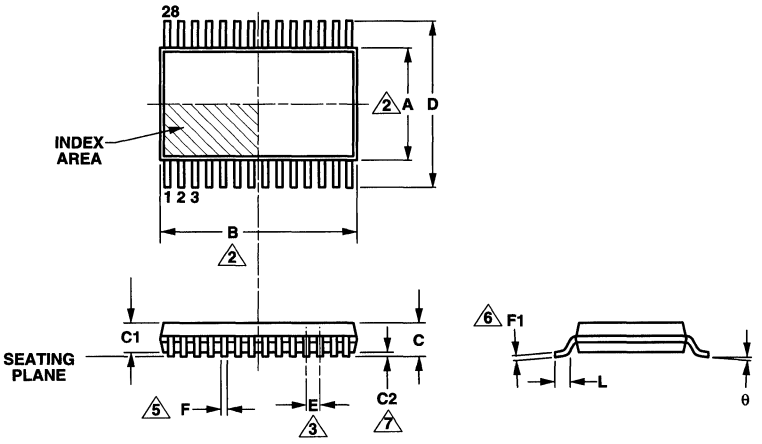
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S)
   SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm
   DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND
   0.25mm FROM THE LEAD TIP.

7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT
   OF THE PACKAGE BODY (BASE PLANE).

28-PIN TSSOP ~ PWP PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.48	.169	.176
B	9.60	9.80	.378	.386
C	–	1.10	–	.043
C1	.90 REF.		.0354 REF.	
C2	.05	.15	.002	.006
D	6.25	6.50	.246	.256
E	.65 BSC		.0256 BSC	
F	.18	.30	.007	.012
F1	.09	.18	.003	.007
L	.50	.70	.020	.028
θ	0°	8°	0°	8°



NOTES:

1. CONTROLLING DIMENSION : MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.

2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.

3. THE BASIC LEAD SPACING IS 0.65 MM BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.10mm OF ITS EXACT TRUE POSITION.

4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.

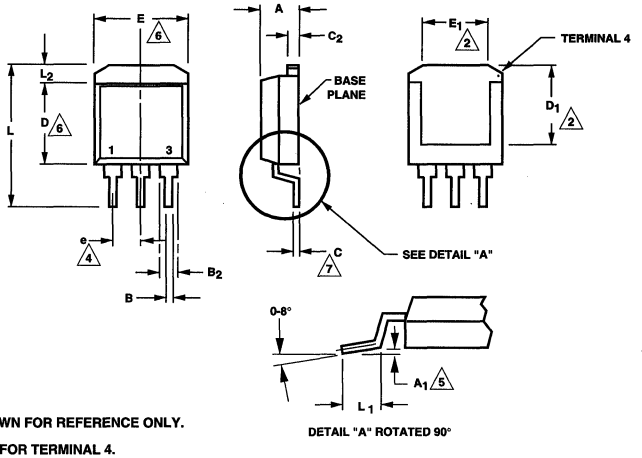
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

3-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
B_2	.045	.050	.055	1.14	1.27	1.40
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.100 BSC			2.54 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68

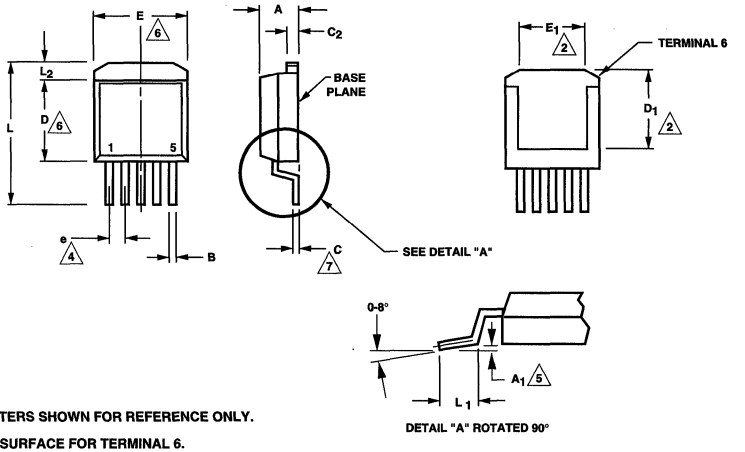


NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.100 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

5-PIN PLASTIC TO-263 POWER SURFACE MOUNT ~ TD PACKAGE SUFFIX

	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.170	.175	.180	4.31	4.44	4.57
A_1	.000	—	.010	0.00	—	0.25
B	.020	.032	.039	0.51	0.81	0.99
C	.018	—	.029	0.46	—	0.74
C_2	.045	.050	.055	1.14	1.27	1.40
D	.326	.331	.336	8.28	8.41	8.53
D_1	.305 REF.			7.75 REF.		
E	.396	.401	.405	10.05	10.18	10.31
E_1	.256 REF.			6.50 REF.		
e	.067 BSC			1.70 BSC		
L	.580	.600	.620	14.73	15.24	15.75
L_1	.090	.100	.110	2.29	2.54	2.79
L_2	.055	.061	.066	1.40	1.54	1.68

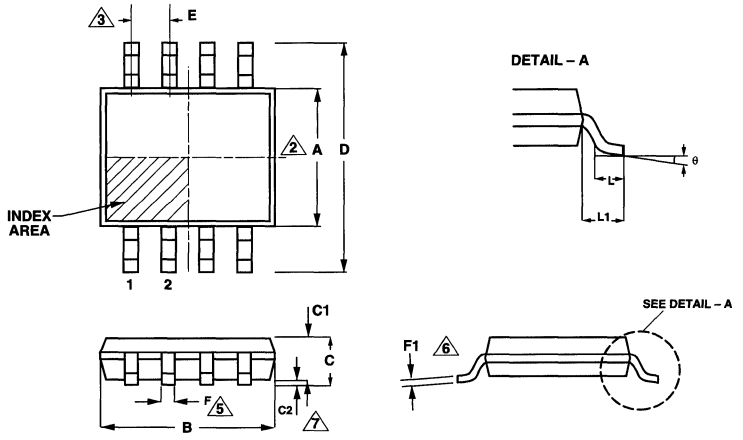


NOTES:

1. CONTROLLING DIMENSION : INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
2. D_1 AND E_1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSION E AND ZONE L_2.
4. THE BASIC LEAD SPACING IS 0.067 INCHES BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 INCHES OF ITS EXACT TRUE POSITION.
5. A_1 IS MEASURED FROM THE LEAD TIP TO THE BASE PLANE.
6. D AND E DO NOT INCLUDE MOLD FLASH ON PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
7. LEAD TIPS SHALL BE COPLANAR WITHIN 0.004 INCHES.

8-PIN MINI SO ~ P PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.84	3.15	.112	.124
B	2.84	3.15	.112	.124
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	4.9 BSC		0.193 BSC	
E	0.65 BSC		0.0256 BSC	
F	0.20	0.46	0.008	0.018
F1	0.08	0.28	0.003	0.011
L	0.41	0.71	0.016	0.028
L1	0.94 REF.		0.037 REF.	
θ	0°	6°	0°	6°

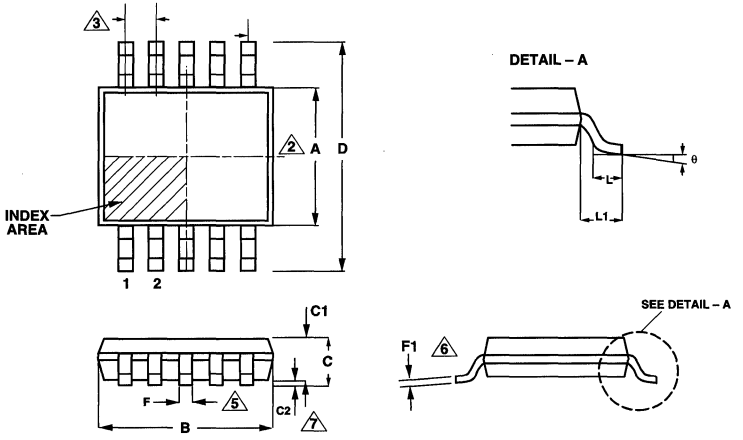


NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.65mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

10-PIN MINI SO ~ P PACKAGE SUFFIX

DIMENSIONS				
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.84	3.15	.112	.124
B	2.84	3.15	.112	.124
C	–	1.10	–	0.043
C1	0.90 REF.		0.035 REF.	
C2	0.05	0.15	0.002	0.006
D	4.9 BSC		0.193 BSC	
E	0.50 BSC		0.0197 BSC	
F	0.15	0.41	0.006	0.016
F1	0.08	0.28	0.003	0.011
L	0.41	0.71	0.016	0.028
L1	0.94 REF.		0.037 REF.	
θ	0°	6°	0°	6 °



NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS. INCHES SHOWN FOR REFERENCE ONLY.
2. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
3. THE BASIC LEAD SPACING IS 0.50mm BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN +0.10mm OF ITS EXACT TRUE POSITION.
4. LEADS SHALL BE COPLANAR WITHIN 0.08mm AT THE SEATING PLANE.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
7. 'C2' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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