TOSHIBA

C²MOS LOGIC
TC74AC/ACT SERIES
TC74HC/HCT SERIES
1990

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

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INTRODUCTION

The TOSHIBA 74AC/ACT Series of Advanced CMOS Logic (ACL) ICs match bipolar FAST* products in speed, function and pinout. The devices are fabricated with silicon gate, double-layer metal wiring C^2MOS technology which is utilized for VLSIs.

The TC74AC/ACT Series has a 3.5ns propagation delay time for gate products and operates at more than 150 MHZ for Flip-Flops. The output drive capability of 24mA ($|I_{OH}|/I_{OL}$) permits the TC74AC/ACT devices to drive 50Ω transmission lines directly.

The family features of the TC74AC/ACT product line include:

- Reduced simultaneous switching noise.
- Wide operating volt range (2~5.5V) (TC74AC type).
- High noise immunity of 28% of the power supply for AC types.
- Excellent ESD Protection (2KV;MIL-STD-883) and excellent latch-up immunity.

Applications for TC74AC/ACT include industrial products, such as telecommunications, data processing and electronic instruments.

This data book presents technical information on TOSHIBA's TC74AC/ACT series.
The information contained in this data book is subject to change without notice.

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FEBRUARY, 1990

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2. TC74AC/ACT Series Selection Guide.

GATE	NAND		AC00 ACT00 AC10 ACT10 AC20
	NOR		AC02 ACT02
	AND		AC08 ACT08 AC11
	OR		AC32 ACT32
	INVERTER,BUFFER		AC04 ACT04 AC05 AC14
	EXCLUSIVE OR		AC86 ACT86
	SCHMITT TRIGGER		AC14 ACT14
BUFFER	BUS BUFFER		AC125 AC126 AC240 ACT240 AC241 ACT241 AC244 ACT244 AC367 AC368 AC540 ACT540 AC541 ACT541
	BUS TRANSCEIVER		AC245 ACT245 AC620 AC623 AC640 ACT640 AC643 AC646 ACT646 AC648 ACT648
FLIP-FLOP	J-K FLIP-FLOP		AC109 ACT109 AC112 ACT112
	D FLIP-FLOP		AC74 ACT74 AC174 ACT174 AC175 AC273 ACT273 AC377 ACT377 AC823 ACT823 AC825 ACT825
		3-STATE	AC374 ACT374 AC534 ACT534 AC564 ACT564 AC574 ACT574 AC646 ACT646 AC648 ACT648 AC821 ACT821
LATCH			AC843 ACT843
		3-STATE	AC373 ACT373 AC533 ACT533 AC563 ACT563 AC573 ACT573 AC841 ACT841
DECODER			AC138 ACT138 AC139 ACT139
REGISTER			AC164 ACT162 AC166 AC299 AC323 ACT323
		MULTI-PORT	AC670
COUNTER		BINARY	AC161 ACT161 AC163 ACT163 AC169 AC191 AC393
		DECADE	AC160 AC162 AC390
MULTIPLEXER		DIGITAL	AC151 ACT151 AC153 ACT153 AC157 ACT157 AC158 ACT158 AC251 ACT251 AC253 ACT253 AC257 ACT257 AC258 ACT258
PARITY TREE			AC280 ACT280
ADDER			AC283 ACT283
COMPARATOR			AC520 ACT520 AC521 ACT521

3. PRODUCT OUTLINE OF THE TC74AC SERIES

3-1 Features

High Speed Operation: Same as Bipolar Schottky TTL

Low Power Dissipation: Same as standard CMOS series (μW)

Output Drive Capability: Symmetrical Output Impedance.
$|I_{OH}|$, I_{OL} at least 24mA.

High Noise Immunity: AC TYPE 28%V_{CC} (Min.)
ACT TYPE 14%V_{CC} (Min.)

Wide Operating Voltage Range:
AC TYPE = 2V-5.5V
ACT TYPE = 4.5V-5.5V

Wide Operating Temperature Range: −40 to + 85℃

Self-contained static electricity protective circuit:
±300V (typ.) by EIAJ method
±2000V (typ.) by MIL STD method
(All inputs and outputs)

Ample Latch up Capacity: Total input and output ±300 mA or more.

Same pin connection and function as 74F series.

Wide product Line up: Over 100 types

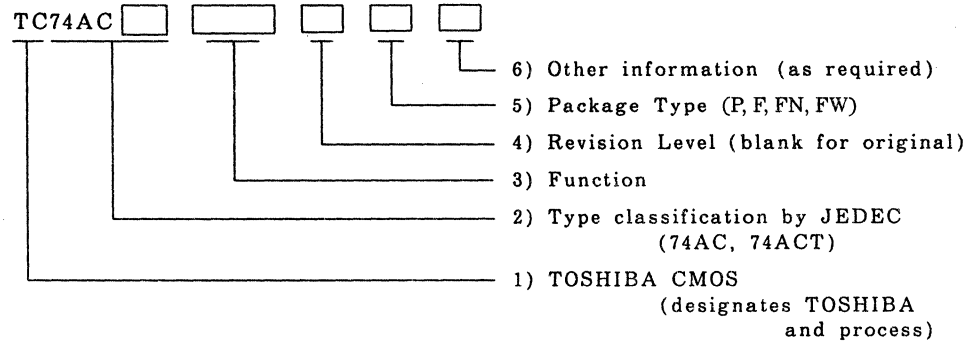
Table 3-2 shows comparison of characteristics of various logic families.

Parameter	Symbole	CMOS		TTL			unit	TEST CONDITION
		ACL (TC74ACXXX)	HCL (TC74HCXXXA)	FAST (74F)	AS-TTL (74AS)	ALS-TTL (74ALS)		
Propagation Delay Time BUS BUFFER(244) typ.	t_{pd}	4.7	10	4	4.1	6.5	ns	V =5V Ta=25℃ CL=50pF
Maximum Clock Frequency D-F • F(74)typ.	f_{MAX}	150	65	125	134	50	MHz	
Quiescent Power Dissipation GATE(00)typ.	P_D	0.01 μ	0.01 μ	22m	32m	5m	W	
Input Voltage	I_{IH} I_{IL}	1 −1	1 −1	20 −600	20 −500	20 −100	μA	over temperature and voltage range
	V_{IH} V_{IL}	3.5 1.5	3.5 1.5	2.0 0.8	2.0 0.8	2.0 0.8	V	over temp.range
Output Current	I_{OH} I_{OL}	−24 24	−4/−6 4/6	−1/−3 20/64	−2/−3 20/64	−0.4/−3 8/24	mA	over temp.range
Operating Voltage Range	$V_{opr.}$	2.0~5.5	2.0~6.0	4.75~5.25	4.5~5.5	4.5~5.5	V	
Operating Temperature Range	T_a	−40~85	−40~85	0~70	0~70	0~70	℃	

Table 3-2 Comparison of Logic Family Characteristics

3-2 Method of Designating the TC74AC Series

The TC74AC series is designated using the standard established by JEDEC and is as shown below;



(Example) TC74ACT240FW:

High Speed C^2MOS IC which is pin and functionally compatible with the bipolar 74F240 .
Input is designed for TTL voltage levels, and direct driving from TTL is possible.
Package type is plastic 300mil body width SOIC.

(1) "TC"

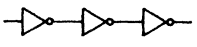
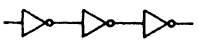
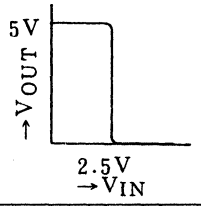
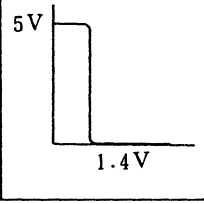
Proprietary name identifying TOSHIBA CMOS devices.

(2) Type classification (AC, ACT)

In addition to the AC devices, there are ACT types. This differentiation was made by JEDEC in order to separate CMOS devices of the same function but with different input levels or the existence of a buffer.

TYPE	Internal stages	Input threshold voltage
AC	Two stages and above	CMOS level
ACT	Two stages and above	TTL level

Taking an inverter as an example, we can show the difference between these types as follows:

	TC74AC04	TC74ACT04
Logic Diagram		
Input–Output Voltage transfer characteristics		

(3) Function

Functions are expressed by Arabic numbers of two to five figures.
In the case of TC74AC series, these numbers are the same as 74F series devices having the same pin connections and function.

(Example) 74F240↔74AC240

(4) Revision Level

This symbol is used to clarify the revision of product when improvements which change the characteristics of product are made. Normally, it is blank, however, upon revision, English characters are given successively from "A". Suffix "A" of TC74ACxxxA series would indicate the types which have refined AC characteristics due to redesign of IC chip but still meet JEDEC standards for the family.

(5) Package Type

English characters showing type of package.

P ..... dual in line package (DIP) Plastic
F ..... 200 mil small outline IC (SOIC) Plastic
FN ..... 150 mil small outline IC (SOIC) Plastic
FW ..... 300 mil small outline IC (SOIC) Plastic

In the TC74AC series, narrow 300 mil type 24 pin DIP package have been developed. Therefore, all P type, 14/16/20/24 pins devices have a 300 mil width (7.62 mm).

(6) Other information

As an example, in the case of SOIC Adhesive and Embossed Tape and Reel specifications, the following suffixes are added to the part number:

(TP 1) or (TP 2) (Difference in pin 1 position) Adhesive tape.
(ELP)...Embossed Tape and Plastic Reel.
For 150/200/300mil SOIC.
(EL)...Embossed Tape and Paper Reel.
For 200mil SOIC.

4. EXPLANATION OF RATINGS AND STANDARDS

4–1 Maximum Ratings

In general, the maximum rating value should not be exceeded in order to guarantee the life and reliability of integrated circuit products.

The Absolute Maximum Rating should not be exceeded even for a moment.
When the device is used in excess of any maximum rating, the device may not recover, and, in many cases, permanent damage will occur.

In designing the circuit, therefore, it is necessary to pay attention to the fluctuation of supply voltage, characteristics of interconnecting parts, ambient temperature, and surges in input and output signal lines, so that the maximum ratings will not be exceeded.

Table 4–1 indicates common absolute maximum ratings of the TC74AC series. When the maximum ratings and common ratings differ, the former shall control. For definition of parameters, refer to Table 4–2.

Table 4–1 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100(For 4outputs type) [1]	mA
Power Dissipation	P_D	500(DIP) [2]/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

1. For devices with more than 4 outputs, the maximum rating equals the number of outputs multiplied by +/−25 mA.

2. 500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85°C a derating factor or −10mW/°C shall be applied until 300mW.

Table 4-2

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	The voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
DC Input Voltage DC Output Voltage	V_{IN} V_{OUT}	The voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
Input Diode Current Output Diode Current	I_{IK} I_{OK}	The current value in which the IC does not present breakdown due to latch-up when input or output current flows. * Practically, a design in which DC current flows is not recommended. When a flow of current cannot be prevented, adopt a current value lower than this.
DC Output Current DC V_{CC}/Ground Current	I_{OUT} I_{CC}	Output current indicates the current value which can flow from one output. As V_{CC}/GND current includes output current, in an IC having many output terminals, substantial V_{CC}/GND current can flow.
Power Dissipation	P_D	Indicates power consumption, which, if exceeded, can cause breakdown of the device over the entire operating temperature range.
Storage Temperature	T_{stg}	The ambient temperature range over which deterioration of characteristics and reliability will not occur when left for a long time in a state without supply voltage.
Lead Temp. and Time	T_L	Indicates the maximum allowable conditions permitted when soldering is carried out after IC mounted on printed board.

4-2 Recommended Operating Conditions

These are the conditions in which the operation of the TC74AC series is guaranteed, and when exceeded, operation is not guaranteed even though they are within the maximum ratings of Table 4-1.

Common recommended operating conditions of the 74AC series are shown in Table 4-3. When recommended operating conditions for specific devices and common recommended operating conditions differ, the former shall control. Refer to Table 4-4 for definitions.

Table 4-3 Common Recommended Operating Conditions

(a) 74AC Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20 (V_{CC}= 5 ±0.5V)	ns/v

(b) 74ACT Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10(V_{CC}=5±0.5V)	ns/v

Table 4–4

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	The supply voltage range guaranteeing normal operation of the IC.
Input Voltage Output Voltage	V_{IN} V_{OUT}	The input/output voltage range guaranteeing normal operation of the IC.
Operating Temperature	T_{opr}	The operating temperature range guaranteeing normal operation and electrical characteristics of the IC.
Input Rise and Fall Time	dt/dv	The rise and fall time range of the input signal which will not cause oscillation of the output.

4–3 DC characteristics

Table 4–5 shows the DC characteristics of AC and ACT types. For the meaning of each parameter, refer to Table 4–6. Table 4–5 is the standard DC characteristics table, and when it differs from individual characteristics, the latter shall control. DC characteristics are established by JEDEC (Standard 20). In the TC74AC series, all devices meet or exceed this standard.

Table 4-5 DC Characteristics Table

(a) 74AC Type

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.50	−	−	1.50	−	V
				3.0	2.10	−	−	2.10	−	
				5.5	3.85	−	−	3.85	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.50	−	0.50	V
				3.0	−	−	0.90	−	0.90	
				5.5	−	−	1.65	−	1.65	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	2.0	1.9	2.0	−	1.9	−	V
				3.0	2.9	3.0	−	2.9	−	
				4.5	4.4	4.5	−	4.4	−	
			I_{OH} = −4 mA	3.0	2.58	−	−	2.48	−	
			I_{OH} = −24mA	4.5	3.94	−	−	3.80	−	
			I_{OH} = −75mA*	5.5	−	−	−	3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	−	0.0	0.1	−	0.1	V
				3.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
			I_{OL} = 12 mA	3.0	−	−	0.36	−	0.44	
			I_{OL} = 24 mA	4.5	−	−	0.36	−	0.44	
			I_{OL} = 75 mA*	5.5	−	−	−	−	1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE/SSI	5.5	−	−	4.0	−	40.0	
			MSI	5.5	−	−	8.0	−	80.0	

Note) * Indicates the capability of driving 50Ω transmission lines.

Test one output at a time for a 10ms maximum duration.

(b) 74ACT Type

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40 ~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	− − −	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −24mA	4.5	3.94	−	−	3.80	−	
			I_{OH} = −75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 24mA	4.5	−	−	0.36	−	0.44	
			I_{OL} = 75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE/SSI	5.5	−	−	4.0	−	40.0	
			MSI	5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} = 3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

Note) * Indicates the capability of driving 50Ω transmission lines.
Test one output at a time for a 10ms maximum duration.

Table 4-6

Parameter	Symbol	Explanation
High-Level Input Voltage	V_{IH}	The input voltage capable of setting the input of the IC to a high level, and the minimum value is guaranteed.
Low-Level Input Voltage	V_{IL}	The input voltage capable of setting the input of the IC to a low level, and the maximum value is guaranteed.
High-Level Output Voltage	V_{OH}	The output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the corresponding output level goes high. There is guaranteed a minimum value of output voltage obtainable when the specified output current (I_{OH}) flows.
Low-Level Output Voltage	V_{OL}	The output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the corresponding output level goes low. There is guaranteed a maximum value of output voltage obtainable when the specified output current (I_{OL}) flows.
Input Leakage Current	I_{IN}	This is the current flowing at the input terminal when a voltage is impressed on the input terminal of IC. Normally, this current is so small that measurement is made with the maximum value of supply voltage.
3-State Output Off-State Current	I_{OZ}	The leakage current flowing at the output terminal when the output is in a high impedance state, the device having a three state or open drain output.
Quiescent Supply Current	I_{CC}	The current flowing from the V_{CC} terminal into the IC when the V_{CC} or GND level is held constant without changing the input voltage. The maximum value under all theoretical conditions allowable for the measured IC is guaranteed.
	ΔI_{CC}	This is the current flowing from V_{CC} terminal into the IC when a TTL level voltage is impressed on one pin at a time.

4–4 AC Characteristics

AC characteristics guarantee the transient characteristics of products.

In general, impressed input waveform is set so as to have an amplitude of V_{CC} to GND and rise and fall time of 3ns.

Table 4–7 explains the meaning of each parameter of the AC characteristics, Fig. 4-1 shows the output connection diagrams for measurement and Fig. 4–2 illustrates the measured waveforms.

Table 4–7

Parameter	Symbol	Explanation	Drawing NO.	
			HC	HCT
Propagation Time	t_{pLH} t_{pHL}	Indicates the time between input signal application and output response detection. t_{pLH} is the case in which the output changes from low level to high level, and t_{pHL} is the case in which the output changes from high level to low.	(i)	(iv)
Output Disable Time	t_{pLZ} t_{pHZ}	Indicates the time, between when a signal is applied to the output control terminal and which the 3-state output is set to a high impedance state.	(iii)	(vi)
Output Enable Time	t_{pZL} t_{pZH}	Indicates the time, between when a signal is applied to the output control terminal and which the 3-state output switches to a low or high level from the high impedance state.		
Maximum Clock Frequency	f_{MAX}	Indicates the maximum frequency at which the IC operates normally.	(ii)	(v)

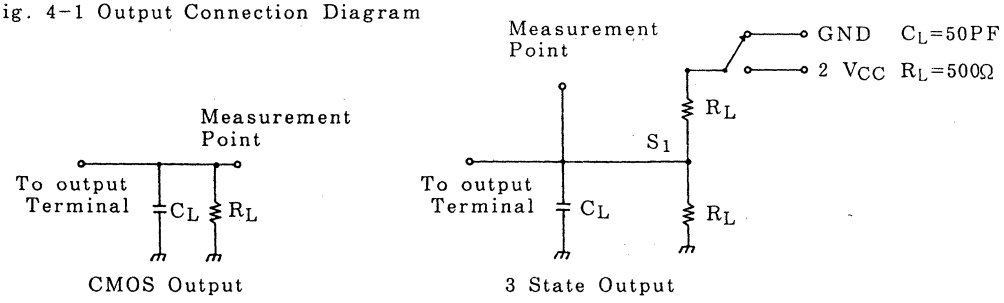
Timing requirements are a prerequisite to the normal function of devices. (See Table 4–8)

Table 4-8

Parameter	Symbol	Explanation	Drawing NO.	
			AC	ACT
Minimum Set-up Time	t_s	Regarding certain data, indicates the time which the data must be applied and held before the input regarding that data (clock, etc.) changes. For example, when the data is read in at a rise of next clock pulse, it is necessary to apply and hold that data before the rising edge of the clock pulse, to a value at least equal to the minimum value of ts.	(ii)	(v)
Minimum Hold Time	t_h	Regarding certain data, indicates the time which the data must be held after the input regarding that data (clock, etc.) has changed.		
Minimum Removal Time	t_{rem}	Indicates the minimum time between releasing of an asynchronous input (clear, preset, etc.) and application of next input (clock, etc.).		
Minimum Pulse Width	t_w	Indicates the minimum pulse width that a clock input, etc. is acceptable as a normal signal.		

Perameter	Symbol	Explanation
Input Capacitance	C_{IN}	Indicates the capacitance between input and GND.
Output Capacitance	C_{OUT}	Indicates the capacitance associated with a 3 state output or a open drain output in the high impedance state.

Fig. 4-1 Output Connection Diagram

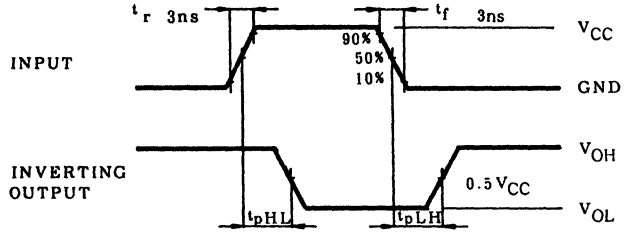


Note) C_L includes the capacitance of probe, etc.

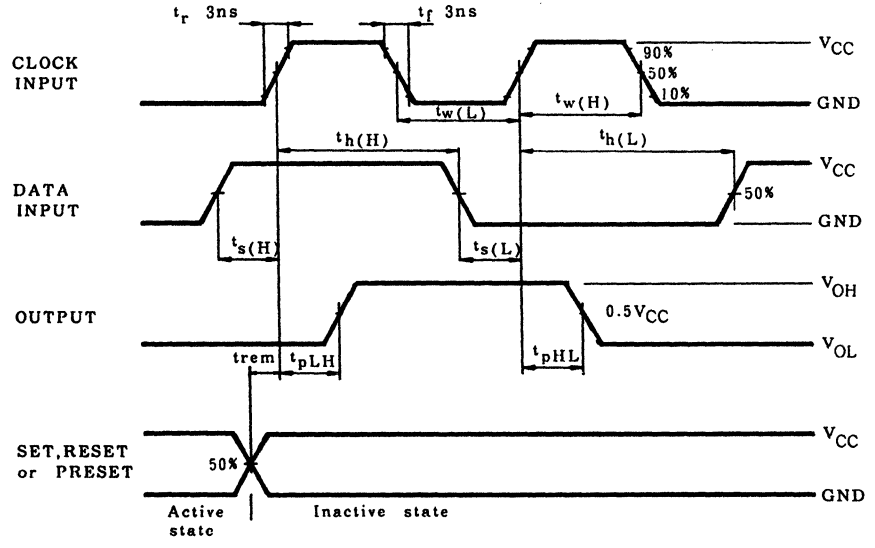
Fig. 4–2 Switching Characteristics Test Waveforms

(1) AC Types

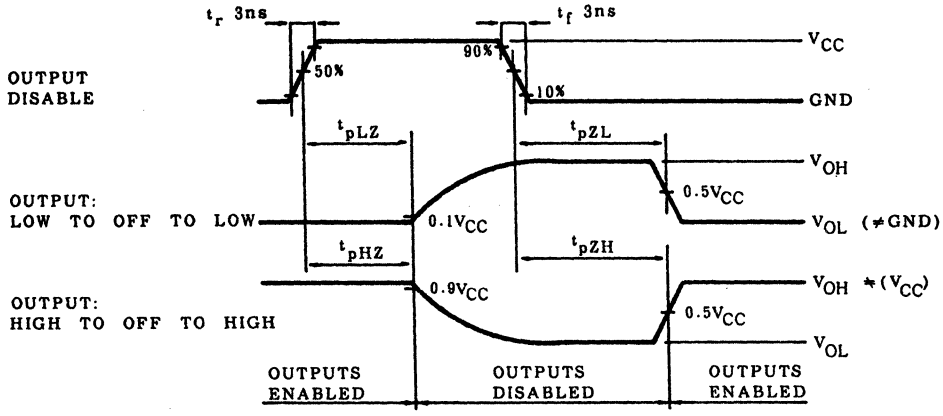
i) t_{pLH}, t_{pHL}



ii) t_w, t_s, t_h, t_{rem}

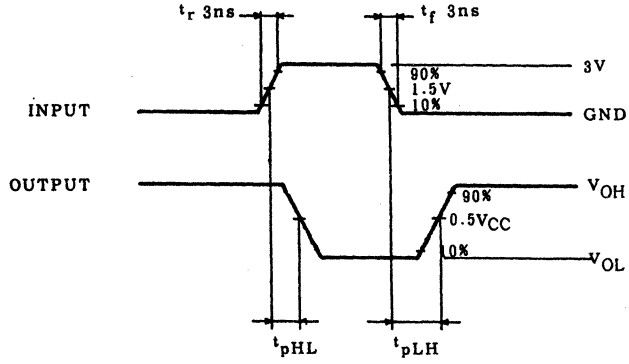


iii) t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

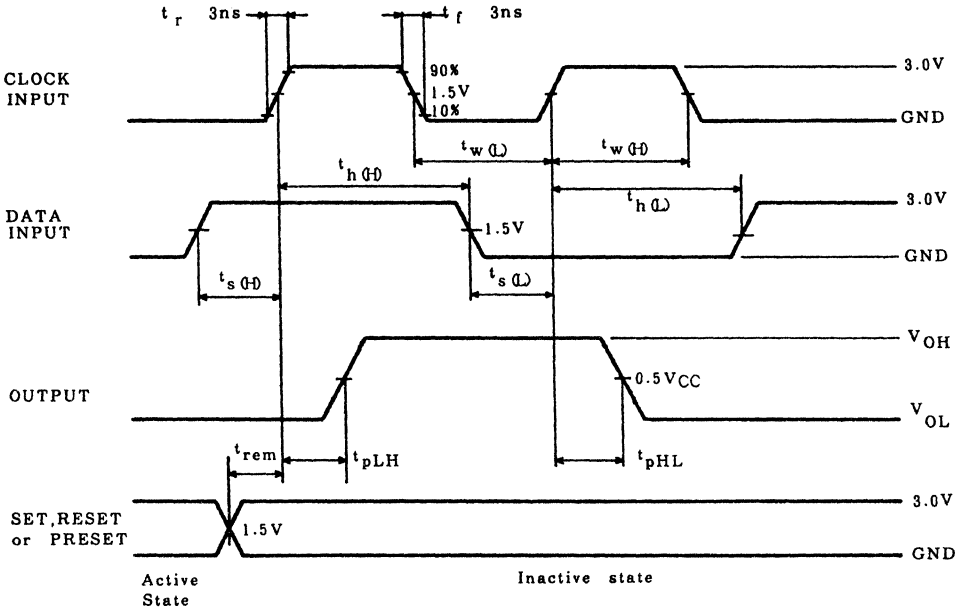


(2) ACT Types

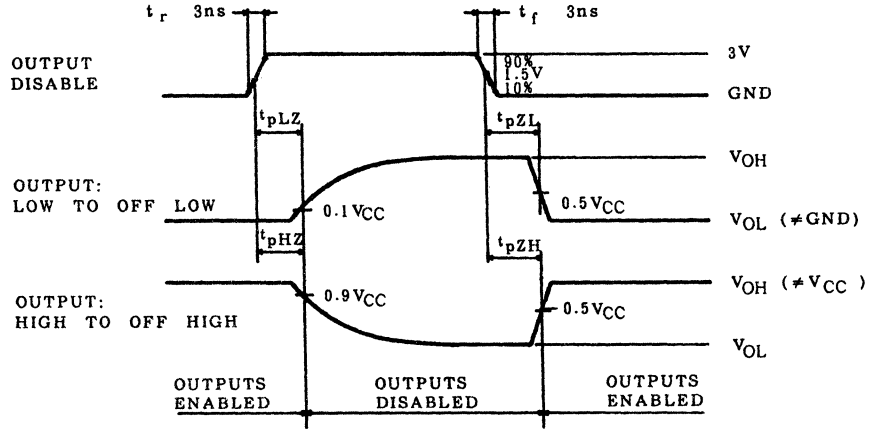
iv) t_{pLH} , t_{pHL}



V) t_w, t_{su}, t_h, t_{rem}



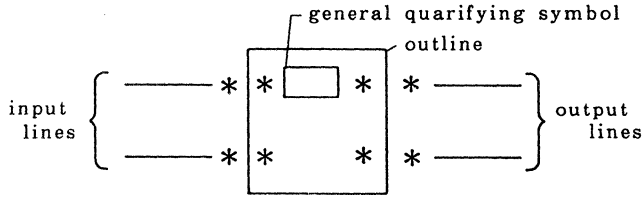
vi) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



5. EXPLANATION OF IEC LOGIC SYMBOLS

5-1 Symbol composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols. The purpose of a general qualifying symbol is to accurately portray the logic function of the device.

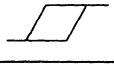
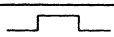
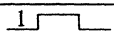
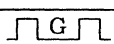
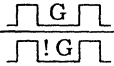
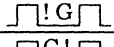
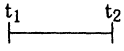


*: qualifying symbol locations for inputs and outputs

5-2 Qualifying Symbols

(1) General Qualifying Symbols

symbol	definition
&	AND element
≥1	OR element
=1	EXCLUSIVE OR element
=	Logic identify element. If all inputs have the same logic state then the output is at internal logc "1".
2K	Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1".
2K+1	Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1".
1	Buffer element without amplified output.
▷ or ◁	Buffer element with amplified output. The triangle points in the direction of signal flow.

symbol	definition
	Schmitt-trigger. It has hysterisis characteristic.
	Retriggerable monostable element.
	Non-Retriggerable monostable element.
	Astable element
	Synchronous-starting astable element.
	Synchronous-stopping astable element.
SRGm	Shift register. "m" :number of bits.
CTRm	Binary counter. "m" :number of bits. cycle length:2
CTRDIVm	Counter with cycle length m.
RCTRm	Ripple carry counter. "m" :number of bits. cycle length:2
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer / data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P-Q	Subtractor.
CPG	Look-ahead carry generator.
π	Multiplier.
COMP	Comparator.
ALU	Arithmetic logic unit.
ROM	Read only memory.
RAM	Random access memory.
FIFO	First-in First-out memory.
I=0	When power is switched ON, the element goes to internal logic "0".
I=1	When power is switched ON, the element goes to internal logic "1".
	Delay element with specified delay times.

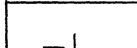
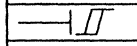
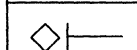
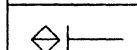
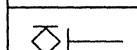
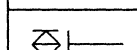
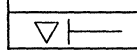
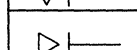
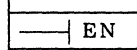
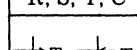
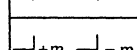
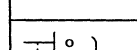
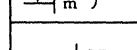
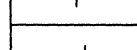
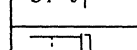
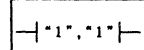
(2) Inputs and Outputs Qualifying Symbols

symbol	definition
	Logic negation at an input. An external logic "0"("1") produces an internal logic "1"("0").
	Logic negation at an output. An internal logic "0"("1") produces an external logic "1"("0").
	Porlarity indicator at an input. A "L"(Low) level active.
	Porlarity indicator at an output. A "L" level active.
	Porlarity indicator at an input where the signal flow is from right to left.
	Porlarity indicator at an output where the signal flow is from right to left.
	Indicator for direction of signal flow.
	Bidirection information flow (alternate).
	Dynamic input Positive logic. Negative logic. Porlarity indicate. The above transitions produce the internal logic active.
	Dynamic input Positive logic. Negative logic. The above transitions produce the internal logic active.
	Dynamic input Porlarity indicate. The above transitions produce the internal logic active.
	Non-logic connection.
	Input for analog signals.

(3) Symbols of the internal connection

symbol	definition
	A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left -hand side produces a transistory logic "1" at the right-hand side.
	Internal input (virtual). This input is always at internal logic "1" state unless this is overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated by dependency notation.

(4) Symbols inside the outline

symbol	definition
	Delayed output. The output change is delayed until the input that indicated the change returns to its initial external state or level.
	Schmitt trigger input.
	Open-drain output without internal pulled-up resistor.
	Open-drain output with internal pulled-up resistor.
	Open-source output without internal pulled-down resistor.
	Open-source output with internal pulled-down resistor.
	Three-state output.
	Buffered output. (The triangle points in the direction of signal flow)
	Enable input.
J, K, D	Information inputs of disable elements.
R, S, T, C	Control inputs of disable elements.
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left. "m"=1,2,3,···, however, the number may be omitted when "m"=1.
	Counting input. Count-up or count-down are indicted by + and − respectively. The number "m" is the count per command and may be omitted when "m"=1.
	Bit-grouping symbol. "m" is the highest power of 2 in the group.
	Content input. The internal logic "1" sets the element to the value "m".
	Content output. For example, when the input state is "1", the internal registor sets "9".
	Line-grouping symbol. The inputs enclosed by this symbol from a single logic input.
	Fixed-mode input, Fixed-state output. This input (output) is parmanently at internal logic "1".

5–3 Dependency Notation

Dependency notation is the powerful tool that makes IEC Logic Symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and outputs are clearly illustrated without the necessity of showing all elements and interconnections involved.

In dependency notation, the terms "affecting" and affected" are used.

(1) These general rules applied to dependency notation:

1) The input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved followed by an appropriately chosen identifying number.

2) Each input or output affected by that affecting input (or output) is labelled with that same number.

3) If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs.

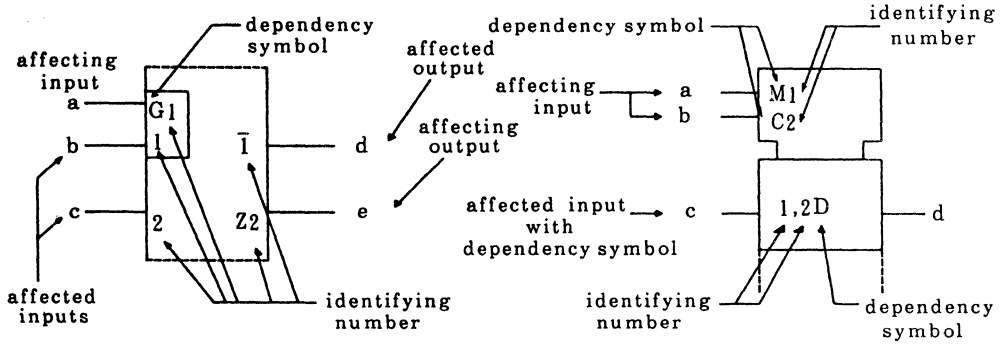
4) If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.

5) If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.

6) If the labels denoting the function of affected inputs or outputs are numbers (example: outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, eg., Greek letters.

7) If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal order of reading these numbers is the same as the sequence of the affecting relationships.

Fig. 5-1 Example for dependency notation



(2) Symbols for dependency notation

function	symbol	Input State "1"	Input State "0"
AND	G	Permits action	Imposes "0" state
OR	V	Imposes "1" state	Permits action
Negate (EX-OR)	N	Complements state	No effect
Interconnection	Z	Imposes action	Permits action
Control	C	Permits action	Prevents action
Set	S	S=1, R=0	No effect
Reset	R	S=0, R=1	No effect
Enable	EN	Permits action	Prevents action of input
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Address	A	Permits action (Address selected)	Prevents action (Address not selected)

6. HOW TO READ MIL TYPE LOGIC SYMBOLS AND TRUTH TABLES

6-1 How to read MIL type Logic Symbols

Table 6-1 shows the MIL type logic symbols used in high-speed CMOS IC. This logic chart is based on MIL-STD-806B. Clocked inverters and transmission gate, employ specific symbols.

Table 6-1 MIL Logic Symbols

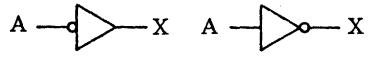
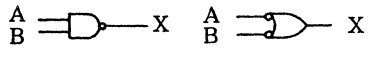
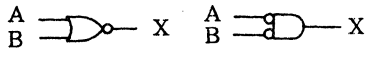
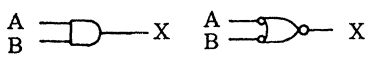
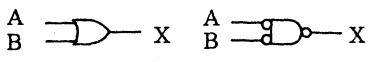
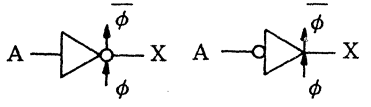
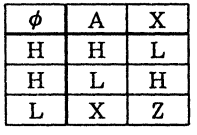
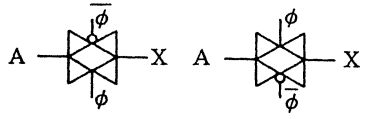
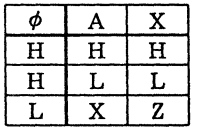
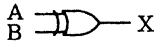
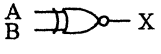
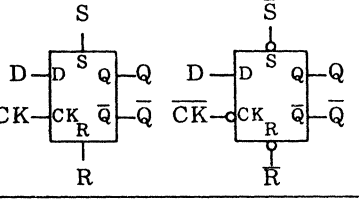
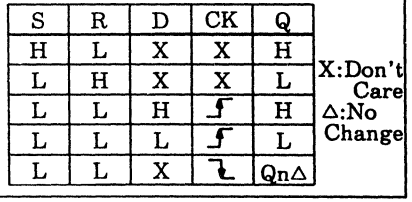
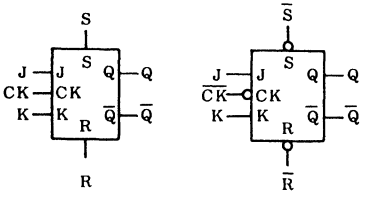
Circuit Function	Logic Symbol	Logical Equation or Truth Table
Inverter		$X=\overline{A}$
NAND Gate		$X=\overline{A \cdot B}=\overline{A}+\overline{B}$
NOR Gate		$X=\overline{A+B}=\overline{A} \cdot \overline{B}$
AND Gate		$X=A \cdot B=\overline{\overline{A}+\overline{B}}$
OR Gate		$X=A+B=\overline{\overline{A} \cdot \overline{B}}$
Clocked Inverter (Note 1)		 X:Don't Care Z:High Impedance
Transmission Gate (Note 2)		 X:Don't Care Z:High Impedance
EXCLUSIVE-OR Gate		$X=(A+B) \cdot (\overline{A}+\overline{B})$
EXCLUSIVE-NOR Gate		$X=(A \cdot B)+(\overline{A} \cdot \overline{B})$
D-Type Flip-Flop		 X:Don't Care △:No Change

Table 6–1 (Cont'd)

Circuit Function	Logic Symbol	Logical Equation or Truth Table
J/K Type Flip–Flop		S R J K CK Q H L X X X H L H X X X L L L L L ↓ Qn△ L L L H ↓ L L L H L ↓ H L L H H ↓ $\overline{Qn}$▽ L L X X ↑ Qn△ X:Don't Care △:No Change ▽:Toggle

Note 1) Clocked Inverter

A clocked inverter has the circuit shown in Fig. 6–1. In this figure, Q1 and Q2 are P–channel MOS FET, and Q3 and Q4 are N–channel MOS FET, and the four FET are connected in series from V_{CC} to GND.

If ϕ signal is high, Q1 and Q4 turn on, and the circuit can be regarded as simply an inverter composed of Q2 and Q3. When ϕ signal is low, both Q1 and Q4 turn off, and, regardless of the condition of the A input, the output, B is set to a high impedance condition cut off from both V_{CC} and GND.

That is to say, a clocked inverter can be used as a switch to turn off input and output.

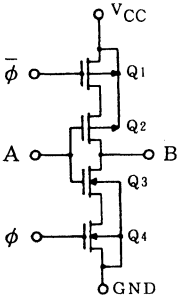


Fig. 6–1 Clocked Inverter

Note 2) Transmission Gate

A transmission gate has the circuit shown in Fig. 6–2. As shown, Q1 is a P–channel MOS FET and Q2 is an N–channel MOS FET which are connected in parallel.

If ϕ signal is high, both Q1 and Q2 turn on, and a signal can be applied in either direction.

If ϕ signal is low, both Q1 and Q2 turn off, and no signal can be passed.

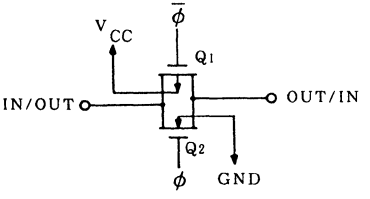


Fig. 6–2 Transmission Gate

6–2 How to Read Truth Table

Table 6–2 indicates the definition of symbols described in Truth Table.

Table 6–2

Symbol	definition
H	High level (Indicates stationary input or output)
L	Low level (Indicates stationary input or output)
	Indicates leading edge changing from "L" to "H".
	Indicates trailing edge changing from "H" to "L".
X	Don't cate (Either "H" or "L")
Z	High impedance state
a ····· h	Input level of stationary state of each input of A to H.
Q_0	Level of Q just before the realization of input condition indicated in Truth Table.
Qn	Level of Q just before inputting of active edge ( or )
	One "H" level pulse.
	One "L" level pulse.

7. COMMON ELECTRICAL CHARACTERISTICS

7-1 Power Dissipation

The power dissipation of CMOS device is composed of two components: one static, the other dynamic.

The total power dissipation is the sum of static and dynamic power dissipation.

Static power dissipation is obtained by multiplying quiescent supply current by the supply voltage range (paragraph 7-1-(1)).

Dynamic power dissipation is obtained as shown in paragraph 7-1-(2).

(1) Static power dissipation

In the case of CMOS ICs, under the condition in which the inputs are fixed at V_{CC} or GND level, either the N–channel FET or P–channel FET turns off. For this reason, the current from V_{CC} to GND becomes only the reverse-direction saturated current of the PN junction and the surface leakage current due to the strain in the chip surface, and is a current of less than several nA at room temperature.

Therefore, where the inputs are driven by another CMOS, or the inputs are pulled-down to GND or pulled-up to V_{CC}, the static power dissipation can be obtained as follows:

$$P_d\ (DC) = V_{CC} \cdot I_{CC}$$

For ACT devices where specific input pins are driven at TTL levels the following applies:

When being driven with a TTL V_{OH}, ACT devices exhibit additional currents (ΔI_{CC}) as specified on ACT device data sheets.

Therefore, the ACT static power dissipation is dependent on the number of inputs to which TTL V_{OH} logic voltage levels are applied, and can be obtained as follows:

$$P_d(DC) = V_{CC} \cdot I_{CC} + nV_{CC} \cdot \Delta I_{CCn} \cdot dn$$

n : the number of inputs at 0~3.4V (TTL V_{IH} level)

d : duty cycle

ΔI_{CC} : quiescent current when $V_{IH} = 3.4V$

(Ref. Technical data sheets)

(2) Dynamic power dissipation

The dynamic power dissipation of a MOS IC is calculated by summing "a" and "b" below:

a) The switching current obtained by charge and discharge of each capacitance added to gate output current when the gates in the circuit including the output buffer makes an inversion.

b) The through current flowing when the P-channel FET and the N-channel FET which constitute the gate during inversion time turn on briefly at the same time.

When rise and fall times of the input signal are small (about 6ns), through current of the gate is usually negligibly small in comparison with the switching current.

For this reason, the dynamic supply current is governed by internal capacitance of the IC and the charging and discharging current of the load capacity (C_L).

An example is given here for C_L = 0pF.

For the inversion of the internal gate outputs from low to high, it is necessary that the electric charge corresponding to $Ci \cdot V_{CC}$ be supplied from the V_{CC} line to the internal capacitance Ci.

Therefore the value obtained by multiplying $Ci \cdot V_{CC}$ and the output inversion frequency (Frequency = f) within a certain period corresponds to the mean current to be supplied from the V_{CC} line to the IC during that period.

In an actual IC, however, several gates operate simultaneously, and their respective internal capacity and inversion frequency are different.

Therefore, dynamic supply current in an IC is as follows:

$$I_{CC}\ (opr.) = V_{CC} \cdot \sum_{1}^{n} f_n \cdot Ci_n$$

fn: frequency of internal operated gate

As fn is divisible by an integer of input frequency (f_{IN}), the gate operating with fn/m frequency can be considered equivalent to the capacitance of Ci/m.

Therefore, the above equation can be rewritten as:

$$I_{CC}\ (opr.) = V_{CC} \cdot f_{IN} \cdot \sum_{1}^{n} Ci/m_n$$

f_{IN} : input frequency

m: integer

The final term is defined as C_{PD}.

Dynamic power dissipation with load capacity is given by the following equation:

$$P_D \text{ (opr.)} = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} \cdot C_{PD}$$

Total dynamic power dissipation with load capacity is given by the following equation:

$$P_D \text{ (opr.)} = C_{PD} \cdot V_{CC}^2 \cdot f_{IN} + \sum_{1}^{n} (C_L n \cdot V_{CC}^2 \cdot f_O n)$$

C_L : load capacity
f_O : output frequency
n : integer of output

However, in specific applications such as crystal oscillators, supply current characteristics are controlled by through current, and calculation by C_{PD} can not be used.

7–2 Standardized Capacitance Power Dissipation (C_{PD}) Test Procedure

The purpose of the C_{PD} value is to allow the user to estimate actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basis, the remaining are measured on a "per device" basis. Each device's unique set up is listed in the Table 7–1, "C_{PD} Test Conditions".

Measurements for all devices are to be made at $V_{CC} = 5.0V$, at $Ta = 25°C$ and, if the devices are tested at an high enough frequency, the DC supply current will contribute a negligible amount to the overall power consumption and can be ignored. For this reason, the power consumption is measured at 1MHz. Any device with 3–state outputs is measured in an enabled state.

In order to determine the C_{PD} of a single section of a device (i.e. one of four gates or one of two flip–flops in a package), the following procedures should be used:

As for the C_{PD} value for devices with a common clock, it can be easily obtained by measuring both the C_{PD} of the device with only one portion of the device active, and the C_{PD} found with all portions active. The C_{PD} value obtained by above two conditions should be shown.

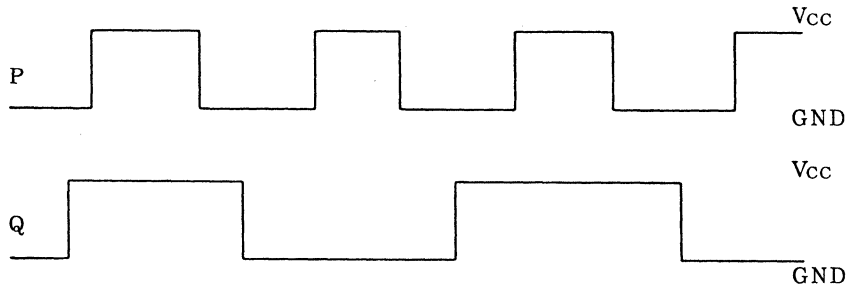
Gates:	Switch one input while biasing the remaining input(s) so that the output(s) will switch.
Flip–flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Latches:	Switch the enable and data inputs such that the latch toggles.
Decoders/ Demultiplexers:	Switch one address input which changes two outputs.
Date selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.

Analog switches:	Switch one address/select input/output which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance as shown above.
Counters:	Switch the clock with the other inputs biased so that the device counts.
Shift registers:	Switch the clock while alternating the inputs so that the device shifts alternation 1's and 0's through the register.
Transceivers:	Switch only one data input. Place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Display Drivers:	Switch one input so that approximately one-half of the outputs change state.
ALUs/Address:	Switch the least significant bit. Bias the remaining inputs so that the device is alternately adding 0000(binary) or 0001(binary) to 1111(binary).

Details of each IC's pin condition are listed in Table 7-1.

-Explanation of symbol-

V = V_{CC} (+5.0V)
G = GND (0 V)
H = logic 1 (V_{CC})
L = logic 0 (GND)
X = don't care. V_{CC} or GND. but not switching
R = 1.0 kΩ pull-up resistor to an additional 5.0V supply other than V_{CC} supply
O = open
P = 50% duty cycle input pulse (shown below)
Q = 50% duty cycle half frequency out-of-phase input pulse (shown below)



Input Pulse Waveform

Table 7–1 C_{PD} Test Conditions

TYPE NO.		Pin																					
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
00		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
02		O	P	L	O	X	X	G	X	X	O	X	X	O	V	•	•	•	•	•	•	•	•	•	•
04		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
08		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
10		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
11		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
14		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
20		P	H	O	H	H	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
32		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
74		H	Q	P	H	O	O	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•
86		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
109		H	H	L	P	H	O	O	G	O	O	X	X	X	X	X	V	•	•	•	•	•	•	•	•
112		P	H	H	H	O	O	O	G	O	X	X	X	X	X	H	V	•	•	•	•	•	•	•	•
132		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
138		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
139		L	P	L	O	O	O	O	G	O	O	O	O	X	X	X	V	•	•	•	•	•	•	•	•
151		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
153		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•
157		P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
157		P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
158		P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
158		P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
160		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
161		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
162		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
163		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
164		Q	H	O	O	O	O	G	P	H	O	O	O	O	V	•	•	•	•	•	•	•	•	•	•
166		Q	X	X	X	X	L	P	G	H	X	X	X	O	X	H	V	•	•	•	•	•	•	•	•
174	1 *	H	O	Q	X	O	X	O	G	P	O	X	O	X	X	O	V	•	•	•	•	•	•	•	•
174	6 *	H	O	Q	Q	O	Q	O	G	P	O	X	O	X	X	O	V	•	•	•	•	•	•	•	•
175	1 *	H	O	O	Q	Q	O	O	G	P	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
175	4 *	H	O	O	Q	Q	O	O	G	P	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
251		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
253		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•
257		P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•
257	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•

TYPE NO.		Pin																						
		0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0	2 1	2 2	2 3	2 4
258	1 *	P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•
258	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
266		P	L	B	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
273	1 *	H	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
273	8 *	H	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
279		L	P	P	O	X	X	O	G	O	X	X	X	O	X	X	V	•	•	•	•	•	•	•	•
299		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
323		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
367		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
368		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
373	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
373	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
374	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
374	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
390		P	L	O	Q	O	O	O	G	O	O	O	X	O	X	X	V	•	•	•	•	•	•	•	•
393		P	L	O	O	O	O	G	O	O	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
533	1 *	L	O	Q	X	O	O	X	X	O	G	G	P	X	X	O	O	X	X	O	V	•	•	•	•
533	8 *	L	O	Q	Q	O	O	Q	Q	O	G	G	P	Q	Q	O	O	Q	Q	O	V	•	•	•	•
534	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
534	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
540	1 *	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
540	8 *	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
541	1 *	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
541	8 *	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
563	1 *	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
563	8 *	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	1 *	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	8 *	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	1 *	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	8 *	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	1 *	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	8 *	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
620		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
623		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
643		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
646		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
648		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
670		Q	Q	Q	L	P	O	O	G	O	O	L	L	L	P	Q	V	•	•	•	•	•	•	•	•

* number of sections active

7-3 Output Current Characteristics

The output current characteristics of TC74AC series is capable of directly driving 15 FAST, and guarantees:

$V_{CC} - V_{OH} \leqq 0.70V$, $V_{OL} \leqq 0.44V$ over the entire temperature range.

Fig. 7-2 shows supply voltage-output current character:stics of typical device at 25℃.

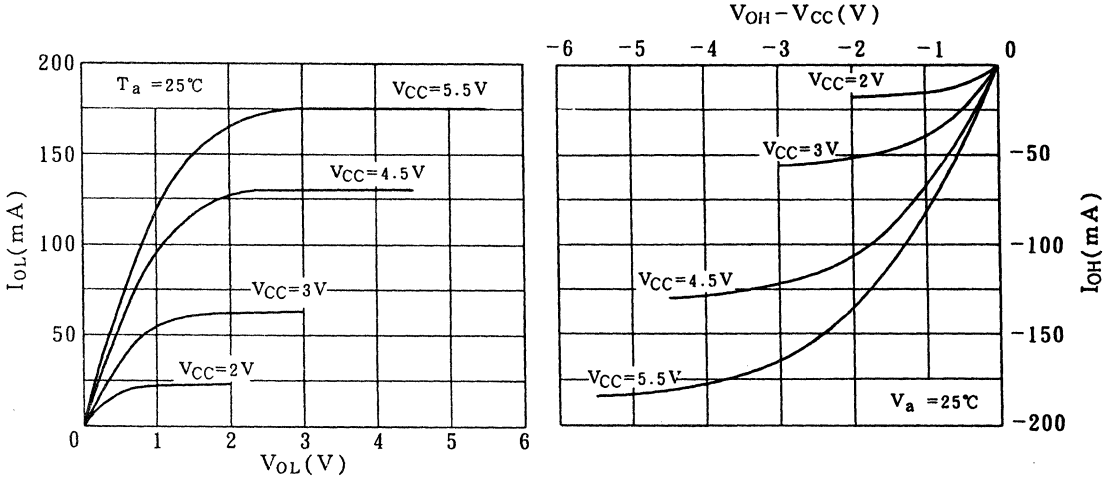


Fig 7-2 Typical Output Current Characteristics

7-4 AC

Load capacitance dependence

Fig 7-3 Shows the load capacitance dependance on propagation delay time at supply voltage of 3.0V and 4.5V.

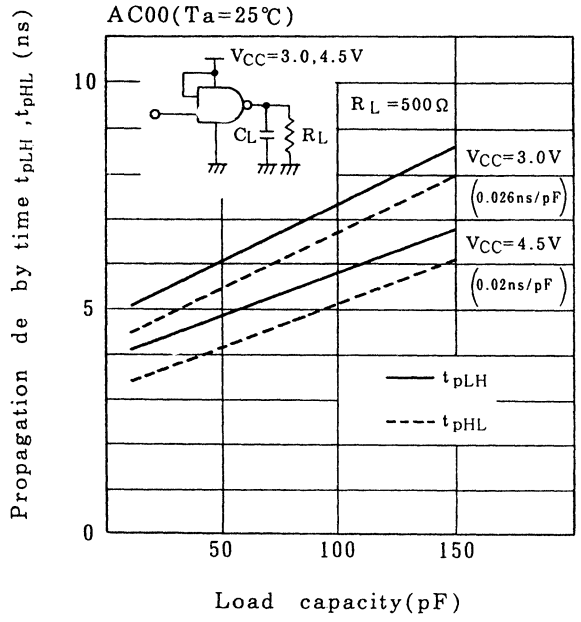


Fig. 7-3 Dependence of t_{pLH} and t_{pHL} (typical characteristics) to Load Capacitance.

7–5 Temperature Parameters of Various Characteristics

In TC74AC series, operation over the wide temperature range of −40℃ to 85℃ is guaranteed. This section shows how the switching time and output current are influenced by temperature.

(1) Temperature versus Output Current

Fig. 7–4 indicates temperature versus output current. In this figure, the line shows the temperature dependence in a standard sample.

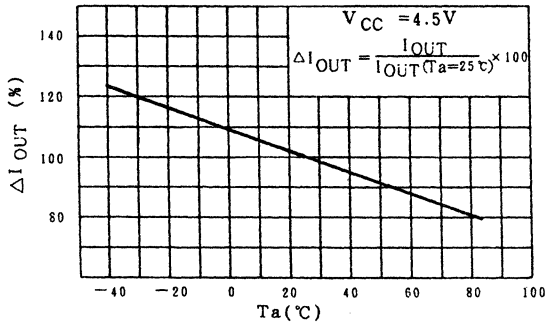


Fig 7−4 Temperature VS. Output Current

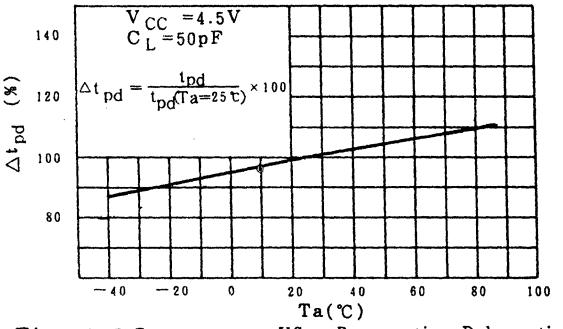


Fig 7−5 Temperature VS. Propagation Delay time

(2) Temperature versus Propagation Delay Time

Fig. 7–5 shows temperature versus propagation delay time. The line in this figure indicates standard temperature dependence of a gate.

8 PRECAUTIONS IN HANDLING

8-1 Electro Static Discharge

A CMOS IC has a very thin gate insulation oxide film. When high voltage is applied to this gate electrode (input of CMOS IC), the oxide film directly under the gate can sometimes break down. In the TC74ACxxx series, as shown in Fig. 8-1, protection diodes are added to all input terminals in order to protect the CMOS gate from such voltage. However, protective circuits may not be effective against the accidental application of high voltage; care must be taken in handling CMOS IC's.

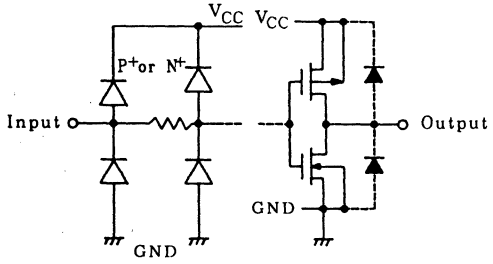


Fig. 8-1 Input Protective Circuit, Output Equivalent Circuit

Further, since a parastic diode is formed between each terminal as indicated in Fig. 8-1, thermal breakdown, etc., due to excessive current may sometimes occur when the voltage exceeding the ratings is applied between each terminal.

(1) Electrostatic Discharge Test Method

Fig. 8-2 shows the electrostatic discharge test method. In Fig. 8-2, the test is conducted with C = 200 pF, R = 0 Ω. Table 8-1 shows the results of electrostatic discharge tests applied to representative types of the TC74AC series.

In the test method, standardized by EIAJ, it is acknowledged that ±200V is sufficient to withstand damage in ordinary service. As shown be Table 8-1 Toshiba's TC74AC series has ample protection.

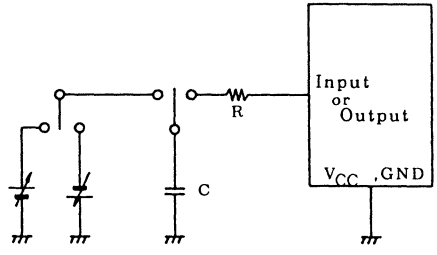


Fig. 8-2 Test Circuit

Table 8-1 Test Result

C=200pF, R=0Ω, Impression frequency 3 times

Name	Output		Input	
	Impression of + voltage	Impression of − voltage	Impression of + voltage	Impression of − voltage
TC74AC00P	> 300V	> −300V	> 300V	> −300V
TC74AC02P	> 300V	> −300V	> 300V	> −300V
TC74AC74P	> 300V	> −300V	> 300V	> −300V
TC74AC139P	> 300V	> −300V	> 300V	> −300V
TC74AC240P	> 300V	> −300V	> 300V	> −300V
TC74AC373P	> 300V	> −300V	> 300V	> −300V

8-2 Precautions in Handling

(1) Transportation and Storage

As the input and output terminals of unmounted CMOS IC's are in a state of high impedance, they are apt to receive induced charges from the surrounding charged body, space electric fields, and the human body.

For this reason, it is necessary, in transporting and storing CMOS IC's, to use dielectric mats, metal cases or aluminum foil boxes, so that each terminal of the IC will be at same potential.

The TC74AC series devices are inserted in magazines and are given antistatic treatment at the time of shipment. Do not remove devices from the magazines unnecessarily. Particularly, avoid the use of plastic or vinyl containers which are apt to create static charges.

When installing CMOS IC's on the printed wiring board, it is necessary to protect the electric equipment, work stand and assemblers from static electricity by grounding. It is advisable to ground the work stand by placing a metal plate or spreading aluminum foil on the surface. Grounding of assemblers should be made through a resistance of about 1MΩ so as to prevent electric shock. Ground through a metallic ring or wrist bands. Also, it is advisable not to wear work clothes made of chemical fibers. Further, it is necessary to periodically check electric equipment to insure absence of electric leakage.

When shaping the leads during the packaging of IC's, it is advisable to use a pincet or similar jig, so that stress may not be given to the device leads at the package entrance.

When storing or transporting the completely assembled printed wiring board, short circuit the terminals of printed wiring board of cover the entire board with aluminum foil, so that the input terminals of the IC are protected.

(3) Soldering

When soldering by use of a soldering iron, carry out the work at temperatures of 260°C or below within 10 seconds. The reliability of the TC74AC series is not affected when subjected to a temperature stress at the lead of 260°C for 10 seconds.

Use a soldering iron having no electrical leakage at its end. It is recommended to use a class A iron having an insulation resistance exceeding 10MΩ. When using a soldering tank, it is necessary to ground the tank so as to prevent the electric potential of the soldering tank from affecting the work.

After soldering the IC's on the printed wiring board, cleaning is done to remove flux, etc. For this cleaning use a flux removing solution or a cleaning method utilizing ultrasonic waves. Care must be taken in the selection of the solvent so as to prevent adverse effects on the package and marking of the CMOS IC's.

In general, it is advisable to use Freon™ cleaners.

When using ultrasonic cleaning, it is necessary to prevent stress due to signal resonance being imparted to the IC's or printed wiring board. Because of this, it is necessary to consider a method such that the main body becomes a shade against vibration, and to use a cleaning time of less than 30 seconds.

When making adjustments and tests after the completion of printed wiring board, it is necessary to check for solder bridges or cracks on the printed wiring board before applying power. As CMOS systems require only a small supply current, apply current limiting during tests by using a constant voltage power source.

Before inserting or removing printed wiring boards into or out of the test fixture, remove all power.

When inspecting the printed wiring board with a probe, care must be taken to prevent contact of the tip of the probe with other signal or power lines. It is advisable to install a special test device for use with probes.

When a test is conducted under high power and low temperature, ensure that the constant temperature oven is grounded.

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9 PRECAUTIONS IN DESIGNING CIRCUITS

9–1 Input Processing

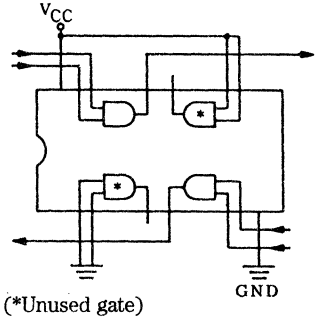
(1) Processing of unused gates.

Inputs of CMOS IC have such a high impedance that the logic level becomes undefined under open conditions. If the input is at an intermediate level, the P–channel and N–channel transistors both turn on, and excessive supply current flows.

Therefore, as shown in Fig. 9–1, be sure to connect unused input lines to V_{CC}, GND or other inputs.

In the case of CMOS, if a soldered part makes poor or no contact, a malfunction of the system or an increase in supply current can occur. Therefore, care must be taken at the time of soldering.

Fig. 9–1 Treatment of Input



(*Unused gate)

(2) Input processing of printed wiring boards.

When an input terminal of a printed wiring board is connected directly to a CMOS input, that input electrically floats. This condition is the same as a single IC being transported or stored. It is advisable, therefore, to connect this input to V_{CC} or GND through a resistance on the printed wiring board, as shown in Fig. 9–2.

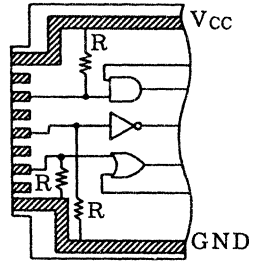


Fig. 9–2 Input processing of Printed Wiring Board

9–2 Design of Power Source

In general, CMOS has a very small current consumption in comparison with bipolar digital IC's and, therefore, it needs only a small capacity power supply. However, from the operational standpoint, CMOS consumes power in the transition state. Therefore, it is necessary to keep the high frequency impedance of the power source as low as possible.

It is advisable to make the wiring of the power source (V_{CC}) and GND lines thick and short, and insert, as a high frequency filter, a 0.001 μF to 0.1 μF capacitor between V_{CC} and GND for each IC.

Also, it is recommended that a capacitor of about 10 μF to 100 μF be inserted between the power supply entrance and GND as a low frequency filter. As mean supply current differs considerably depending upon the operating frequency of the system, existence of capacitive load, rise and fall of the input signal and supply voltage, attention must be given especially in the case of a simple power source, by using a Zener diode or by battery drive. When there is overshoot or undershoot during the transition time of the power supply use a filter, etc. so that the maximum device rating is not exceeded.

9–3 Output Short Circuit

In the TC74AC series, a buffer is added to the output, and both outflow (I_{OH}) and inflow (I_{OL}) current drive is possible. For this reason, excessive current flows in the CMOS output when the high level output line is shorted to GND or the low level output line is shorted to V_{CC}. Particularly, when the supply voltage is high, I_{OH} and I_{OL} are quite excessive and may damage the device; therefore care must be taken not to cause an output short circuit.

It is, of course, impossible to directly connect ordinary outputs together. But in the case of an IC which has a 3-state output, a wired OR connection is permitted provided that no more than two outputs are enabled simultaneously.

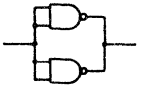


Fig. 9–3 Example of how to increase drive capacity

9–4 Effect on Input of Slow Rise and Fall Time

When a slow rise or fall time signal is impressed on a CMOS input, it sometimes happens that the output tends to oscillate around V_{TH} (threshold voltage of device). This is because the CMOS gate becomes a linear amplifier equivalent in the vicinity of V_{TH}, and minute power source ripple and noise components are amplified and appear in the output.

To prevent this, it is necessary to insert a high frequency filter capacitor between V_{CC} and GND of the oscillating IC, or use a Schmitt trigger IC.

In the case of an TC74AC series, excepting Schmitt trigger IC's, the input rise and fall time is limited as shown in Table 9–1.

Proper design requires that these rise and fall time limits be observed.

Fig. 9–4 shows an example of a malfunction when a shift counter is designed by using a D-type flip–flop in separate packages. In this case, the malfunction is considered to be caused by the difference in circuit threshold level of separate D-type flip flops.

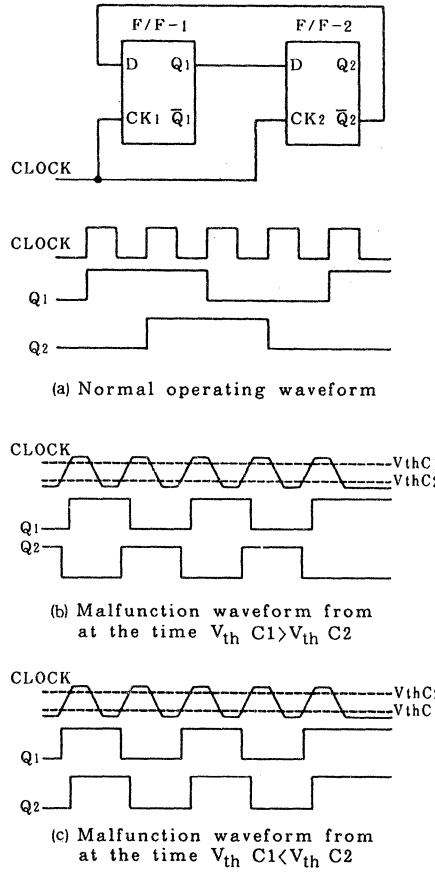


Fig. 9–4 Example of Malfunction

Let circuit threshold level of F/F–1 be V_{th} C1, and that of F/F–2 be V_{th} C2. Then, as shown in Fig. 9–4, time difference Δt is formed when the rising waveform of the clock pulse cuts the respective circuit threshold voltage, and thus a malfunction occurs.

The following condition is required for ensuring normal operation:

$$\Delta t < t_{pd}\ (CK-Q)+t_{set-up}$$

In this case, there is a possibility of malfunction even though the input signal is within the standard value of Table 9–1. Therefore, care must be taken in design of sequence circuit clock inputs.

Table 9–1 Standard Value of Input Rise and Fall Time

(1) 74AC TYPE

Item	Symbol	Limit	Unit
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC} = 3.3±0.3V) 0 ~ 20(V_{CC} = 5±0.5V)	ns/V

(2) 74ACT TYPE

Item	Symbol	Limit	Unit
Input Rise and Fall Time	dt/dv	0 ~ 10(V_{CC} = 5±0.5V)	ns/V

9–5 Wiring Precautions

As the output impedance of the TC74AC series is very low in comparison with the conventional standard CMOS IC, distortion is sometimes caused in the output waveform depending upon the L component of the wiring, long output wiring or when capacitance is connected between signal lines and V_{CC} or GND. Therefore, when designing the printed wiring board, take care not to make signal wiring too long. In the case of double sided printed wiring boards, it is ideal to limit signal wire length to 30cm or less. The clock signal line is particularly prone to distortion.

(2) Precautions for parts arrangement

The output of TC74AC series has a fast rise and fall time, and makes a full swing between V_{CC} and GND. Therefore it becomes a noise source to other signals. It is necessary to locate the output away from a part which is sensitive to the noise of an analog circuit. Also, care must be taken for the reduction of the number of loads and wiring lengths.

From its physical and electrical characteristics, the TC74AC series is apt to cause some overshoot and undershoot, and this can lead to malfunction of the circuit or breakdown of passive IC's. These troubles can be prevented to some extent by terminating the ends of signal lines. Fig. 9–5 indicates examples of termination methods.

(a) Termination by CR (b) Termination by Diode

Fig. 9–5 Examples of Termination

9–6 Interface

When interconnecting a CMOS system, an exchange of signals with external circuits or mechanisms is usually done. These input and output signal lines are made long in many cases, and have distributed inductance and/or reactance. Therefore, if directly connected to CMOS, they can give rise to various problems.

Conceivable problems can include a malfunction due to induced noise, and the destruction of the input/output elements due to surge. To cope with these problems, reduction of signal line impedance (driving impedance) or insertion of a noise eliminating circuit on the receiving side is done for the former problem, while surge protective measures are taken for the latter.

Fig. 9–6 illustrates examples of providing noise and surge protection on the input side.
(a) and (b) show examples of absorbing noise by integrating the input waveform.
(c) and (d) are examples of protecting CMOS from input surge.

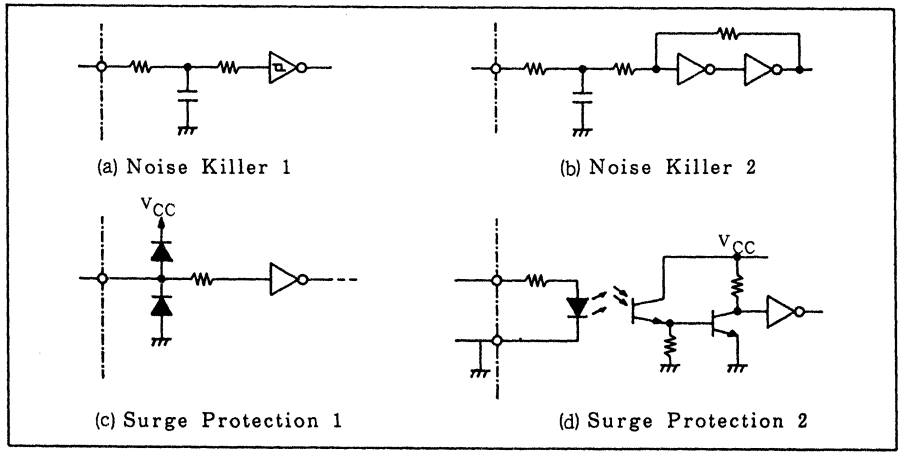


Fig. 9–6 CMOS Input Protective Circuits

(4) Interface with CPU

At present, 74F series TTL is used universally as the peripheral supporting logic for MOS microprocessors. Since the TC74AC series has the same speed as 74F, it can be used as microprocessor peripheral logic. As an interface with a CMOS CPU there is no problem since both are CMOS. At present, however, the use of NMOS CPU is greater, and the interface of NMOS to CMOS must be taken into consideration.

The output of most NMOS CPU's rises to near V_{CC}, but as shown in Fig. 9–10, as outputs of both driving MOS and load MOS are enhancement type, no switching takes place until near V_{CC}. In order to carry out the signal transfer from the NMOS CPU to the 74AC, use the 74ACT series which has a TTL level input. When connecting the 74AC series, a pull up resistor is required as shown in Fig. 9–10.

Driving an NMOS CPU from the 74AC series can be done without difficulty. The input of NMOS is high impedance like CMOS, and the DC fanout need not be taken into consideration.

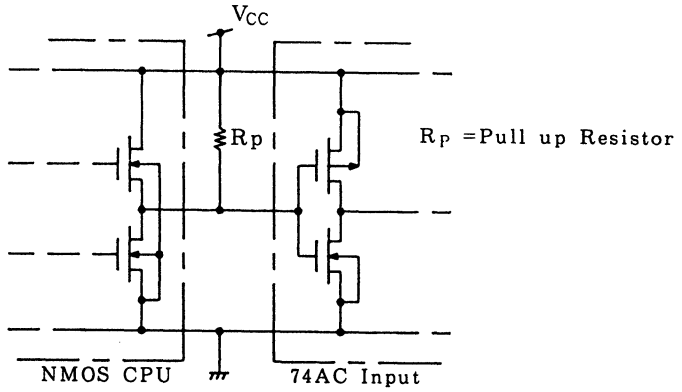


Fig. 9–10 NMOS CPU Interface

9–7 Latch–up

Latch–up is a phenomenon peculiar to CMOS, and is also called SCR (Silicon Controlled Rectifier) Phenomenon. During the normal operation, if excessive voltage and current caused by high noise or accidental surge is applied to the input or output terminal, or a supply source suddenly fluctuates, abnormal current flows between V_{CC} and GND, and this current continues to flow even though the disturbing signal is cut off, and, finally, damage is caused. Latch–up is the name given to this phenomenon.

Once latch–up takes place, the original condition is not restored unless the power supply is cut off.

(1) Cause of latch–up

Fig. 9–11 shows as equivalent circuit with the parasitic element. NPN transistor Q_2 is formed in the P–well of NMOS side while PNP transistor Q_1 is formed in the N–substrate of PMOS side, and a parasitic resistor exists between the terminals. As shown from the current path through the medium of the parasitic element, these parasitic elements constitute a Thyristor.

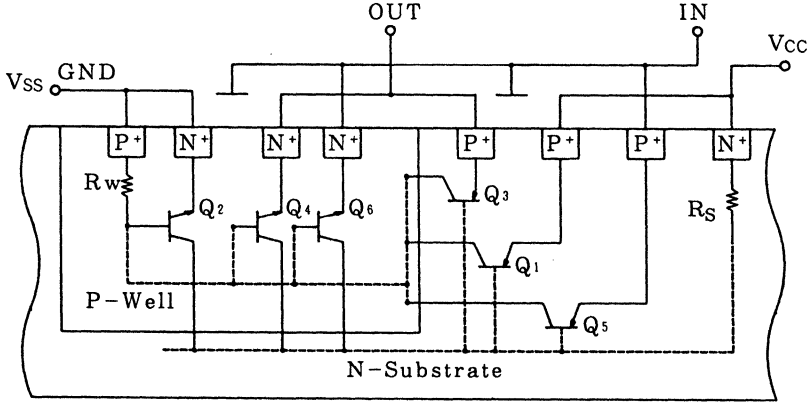


Fig. 9–11 Internal Equivalent Circuit of CMOS IC

Fig. 9–7 gives examples of an output interface. There are other methods, but in any case, some protection scheme should be provided to an interface involving long signal lines.

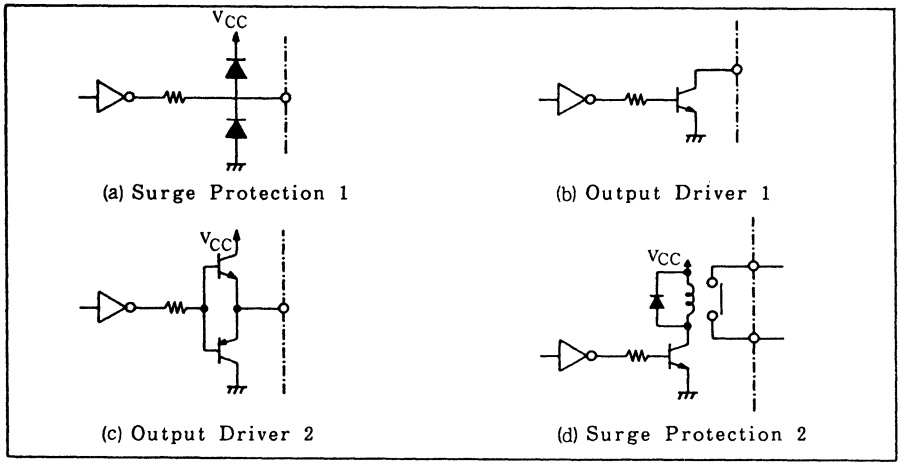


Fig. 9–7 Output Protection/Driving Circuits

(2) Interface between CMOS IC's

When CMOS IC's are interfaced, the input impedance is so large that the limitation of fanout may not be so important. However, there is a need to consider the increase in propagation delay time due to the adding effect of load capacitance and an increase in power consumption.

Input capacitance of CMOS is about 5pF per input. If 10 fan outs are taken, for example, the load capacitance is 50pF. Further, the line capacitance of the printed wiring board must also be taken into consideration. This shows that the processing speed of system is controlled not only by the circuit IC's but also by fanout.

When constructing a system with CMOS IC, the designer must examine the fanout and take these points into consideration.

(3) Interface with TTL

When driving TTL with the TC74AC series, input and output voltage levels can be connected without trouble. Fanout is determined by the output current of CMOS IC and input current of the TTL. An example is shown in Fig. 9–8.

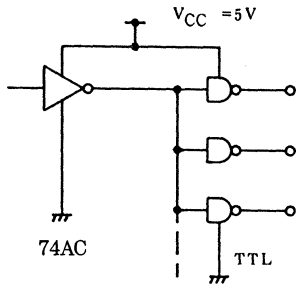


Fig. 9–8 TC74AC → TTL Interface

On the other hand, when driving TC74AC series with TTL, it is necessary to convert the output voltage level of the TTL to the input level of the 74AC. Normally, TC74ACT series devices which have same input level as FAST are used. The input current of TC74ACT series is very low like that of TC74AC series, and no burden is imposed on the driving side 74F. Additionally, the speed falls very little. Therefore, it can be said to be an effective method. Another method is to use a pull up resistor as shown in Fig. 9–9.

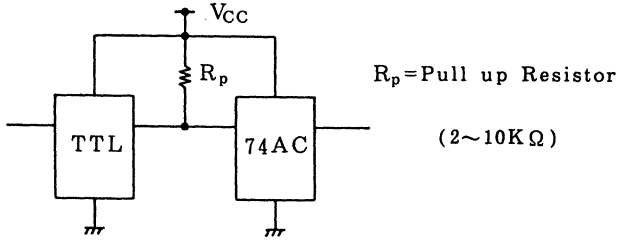


Fig. 9–9 TTL → 74AC Interface

For example, if current flows into the N–substrate from external sources, a voltage drop takes place in the resistor Rs of the N–substrate, and this turns on parasitic transistor Q_1, and current flows towards GND from V_{CC} through the medium of resistor Rw in the P–Well. When current flows in Rw, a voltage drop takes place at both ends of Rw, Q_2 turns on, and further supply current flows through Rs. As a result, the voltage drop at both ends of Rs further increases, Q_1 and Q_2 are left in the turn–on state, and the supply current continues to increase.

In this way, if the voltage drop takes place in resistance Rw in the P–Well and in resistance RS in the N–substrate, latch–up occurs, and the following events occur:

1) Input voltage goes higher than $V_{CC} + V_F$
(Q_5 turns on)

2) Input voltage goes lower than $GND - V_F$
(Q_6 turns on)

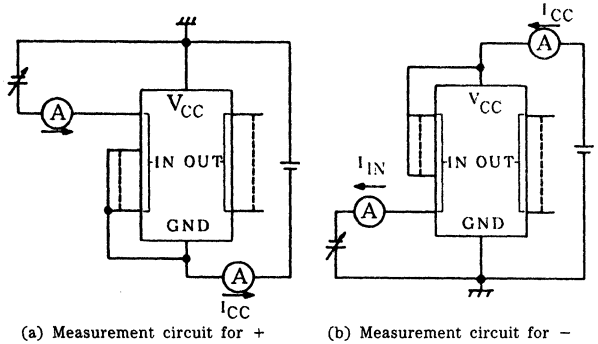
3) Output voltage goes higher than $V_{CC} + V_F$
(Q_3 turns on)

4) Output voltage goes lower than $GND - V_F$
(Q_4 turns on)

5) This raises supply voltage V_{CC} above the rated value causeing breakdown.
(Directly forces current in Rw or Rs)

Here, V_F is the forward voltage between base and emitter of parasitic bipolar transistor $Q_3 - Q_4$.

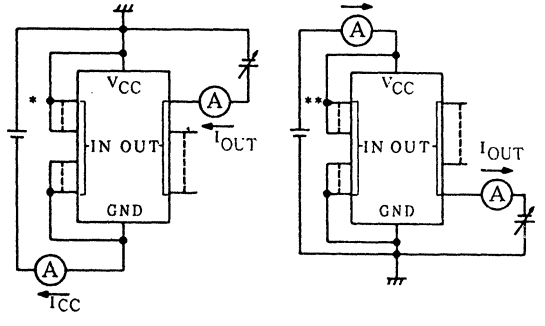
Fig. 9–12 illustrates a measurement example of latch–up strength. As indicated in Fig. 9–12, latch–up is induced by forcing current into input terminal (+ injection) or forcing current out of output terminal (– injection), and the current value at that time is measured.



(a) Measurement circuit for + Injection strength of Input Terminal

(b) Measurement circuit for − Injection strength of Input Terminal

• : Input condition to make measured terminal high level
••: Input condition to make measured terminal low level



(c) Measurement circuit for + Injection strength of Output Terminal

(d) Measurement circuit for − Injection strength of Output Terminal

Fig. 9–12 Latch up Strength Measurement Circuits by Current Feeding

(3) Countermeasures

As ample margin is provided against latch–up, there is no problem in using the device within the specifications. However, since the part has the possibility of receiving excessive current surge, it is recommended that a protective circuit be added. Fig. 9–13 contains examples.

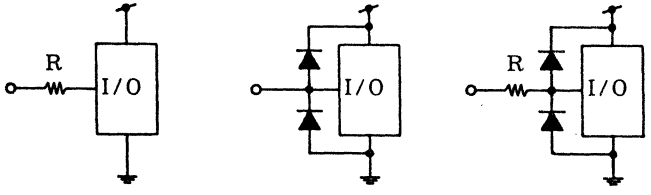


Fig. 9–13 Example of Latch up Prevention Methods

10. DATA SHEETS

TC74AC/ACT SERIES

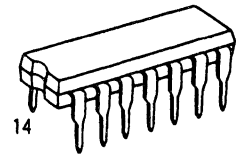
QUAD 2-INPUT NAND GATE

The TC74AC00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

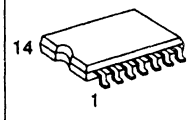
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

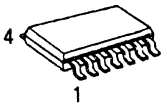
The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP14-P-300)



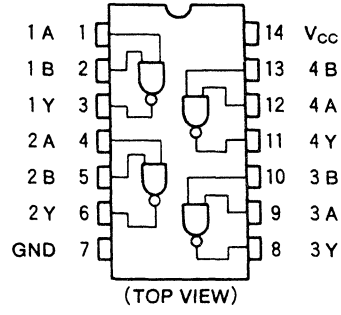


F(SOP14-P-300) FN(SOL14-P-150)

FEATURES:

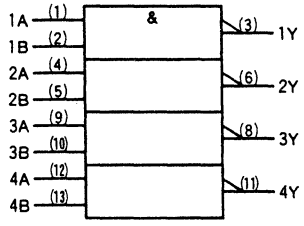
- High Speed ..... t_{pd}=3.8ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F00

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input t_r=t_f=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.6	11.2	1.0	12.9	ns
	t_{pHL}		5.0±0.5	−	4.9	7.0	1.0	8.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	68	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

QUAD 2-INPUT NAND GATE

The TC74ACT00 is an advanced high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

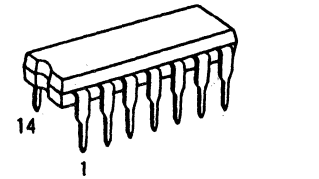
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 4.0ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4 μA (Max.) at Ta = 25℃
- Compatible with TTL outputs..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F00



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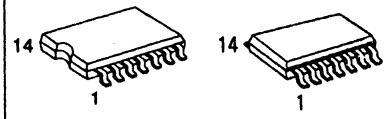
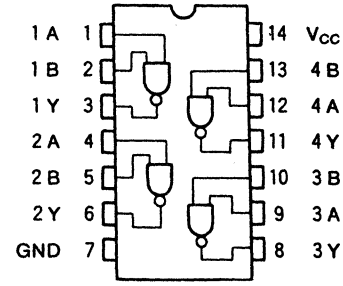


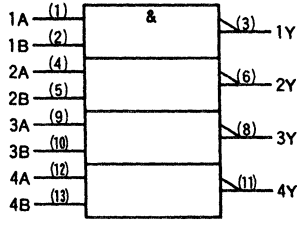
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

QUAD 2-INPUT NOR GATE

The TC74AC02 is an advanced high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

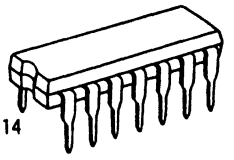
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=3.7ns (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 02



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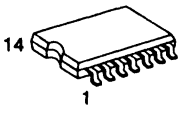
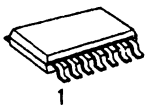
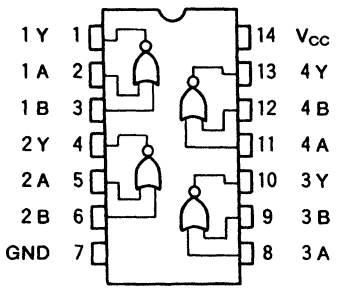




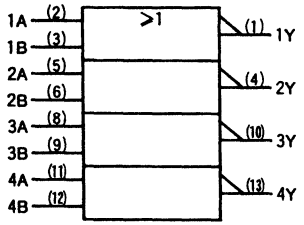
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	4.7	7.9	1.0	9.5	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	23	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.1	9.8	−	11.2	ns
	t_{pHL}		5.0±0.5	−	4.8	7.0	−	8.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	82	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

QUAD 2-INPUT NOR GATE

The TC74ACT02 is an advanced high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

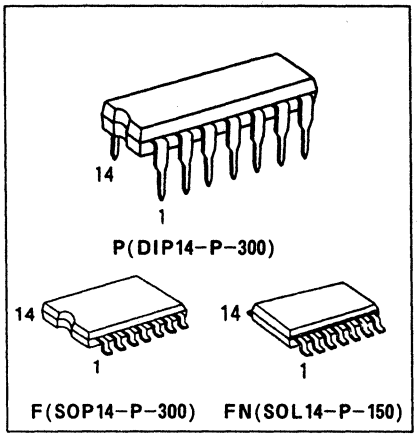
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

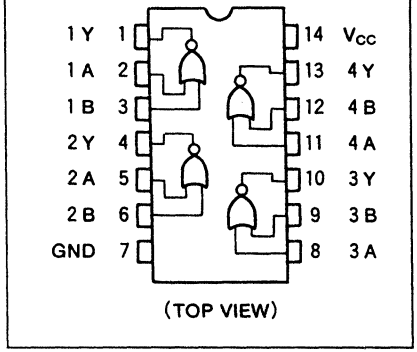
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

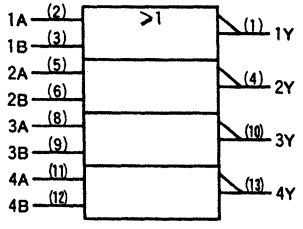
- High Speed ..... t_{pd} = 4.6ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4 μA (Max.) at Ta = 25℃
- Compatible with TTL outputs ..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 02



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.3	8.3	1.0	9.5	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	22	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

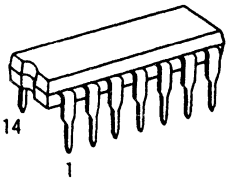
HEX INVERTER

The TC74AC04 is an advanced high speed CMOS INVERTER fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

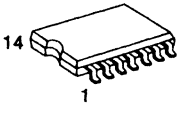
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

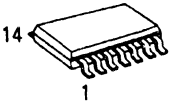
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP14-P-300)



F(SOP14-P-300)

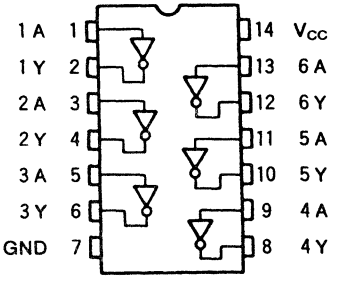


FN(SOL14-P-150)

FEATURES:

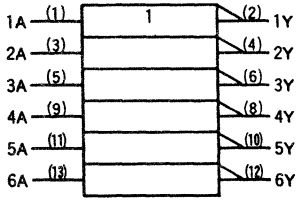
- High Speed ..... t_{pd}=3.2ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F04

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.3	15.0	1.0	17.3	ns
	t_{pHL}		5.0±0.5	−	4.3	6.6	1.0	7.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	20	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

HEX INVERTER

The TC74ACT04 is an advanced high speed CMOS INVERTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

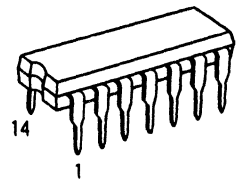
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

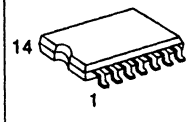
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

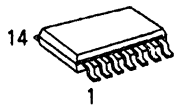
- High Speed ..... t_{pd}=4.6ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- Compatible with TTL outputs ..... V_{IL} =0.8V (Max.)
  V_{IH} =2V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 04



P(DIP14-P-300)

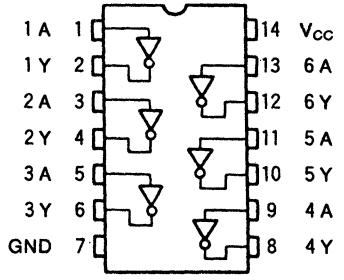


F(SOP14-P-300)



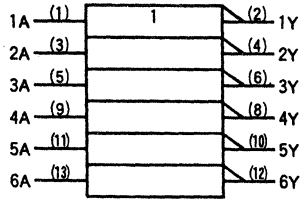
FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

HEX INVERTER(OPEN DRAIN)

The TC74AC05 is an advanced high speed CMOS INVERTER fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

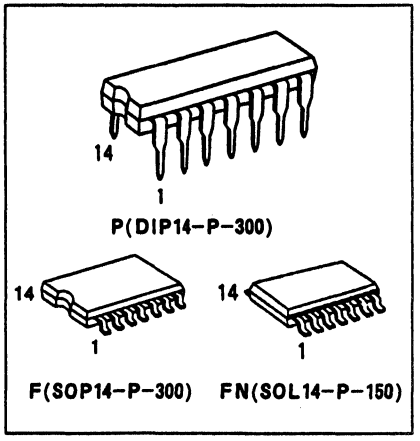
Pin configurathion and function are the same as the TC 74AC04, but the TC74AC05 has high performance MOS N-channel transistor(OPEN-DRAIN) outputs.

This device can, therfore, with a suitable pull-up rsistors, be used in wired-OR, LED drive and other applications.

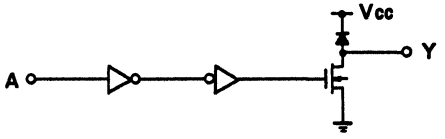
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

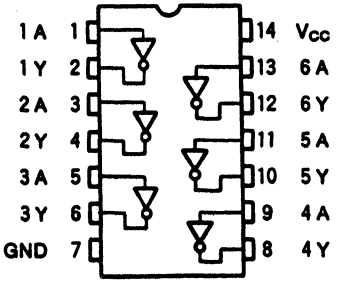
- High Speed ····· t_{pz}=3.4ns (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· I_{OL}=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Open Drain Structure.
- Pin and Function Compatible with 74F05



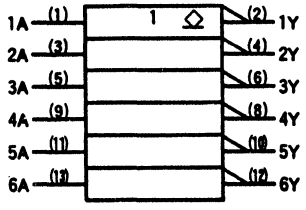
SYSTEM DIAGRAM(per gate)



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	Z
H	L

Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	+50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN} =V_{IH} or V_{IL} V_{OUT} =V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.5	7.9	1.0	9.0	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	19	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLZ}		3.3±0.3	−	4.1	7.0	1.0	8.0	ns
			5.0±0.5	−	3.5	5.3	1.0	6.0	
Propagation Delay Time	t_{pZL}		3.3±0.3	−	5.9	9.1	1.0	10.4	
			5.0±0.5	−	4.1	6.6	1.0	7.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	8	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

QUAD 2-INPUT AND GATE

The TC74AC08 is an advanced high speed CMOS 2-INPUT AND GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

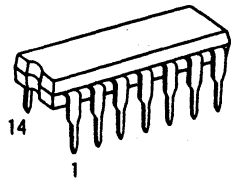
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

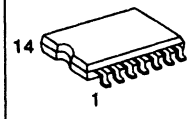
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

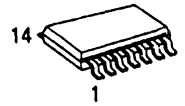
FEATURES:

- High Speed ..... t_{pd}=3.4ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F08



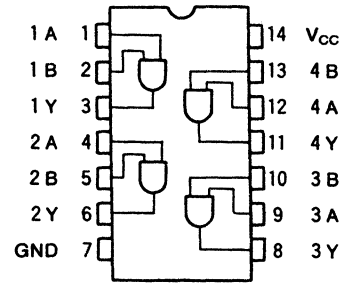
P(DIP14-P-300)





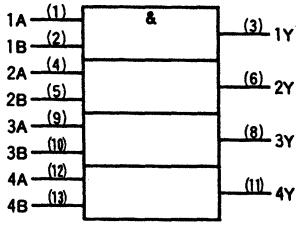
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}=V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	5.8	9.8	1.0	11.3	ns
	t_{pHL}		5.0±0.5	−	4.5	7.0	1.0	8.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	71	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

QUAD 2-INPUT AND GATE

The TC74ACT08 is an advanced high speed CMOS 2-INPUT AND GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

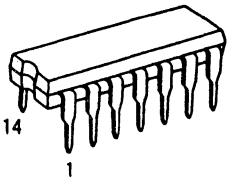
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

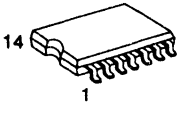
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

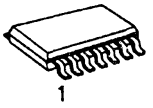
FEATURES:

- High Speed ····· t_{pd}=4.7ns (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.) at Ta=25℃
- Compatible with TTL outputs····· V_{IL} =0.8V (Max.)
  V_{IH} =2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F08



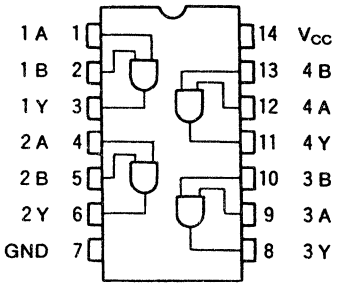
P(DIP14-P-300)





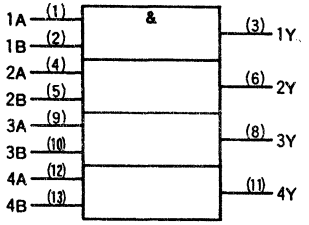
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ≀ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ≀ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.4	8.7	1.0	10.0	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	21	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TRIPLE 3-INPUT NAND GATE

The TC74AC10 is an advanced high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

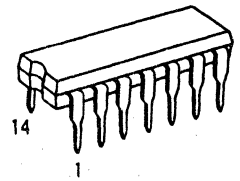
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

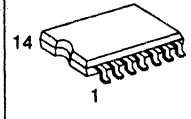
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

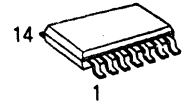
FEATURES:

- High Speed ..... t_{pd}=5.0ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F10



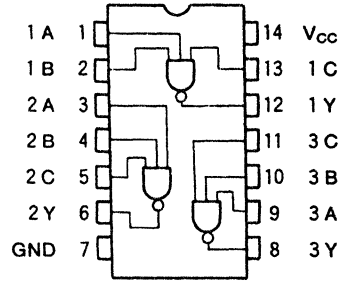
P(DIP14-P-300)





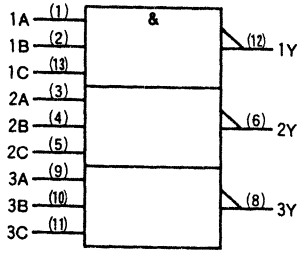
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

X : Don't Care

TRIPLE 3-INPUT AND GATE

The TC74AC11 is an advanced high speed CMOS 3-INPUT AND GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

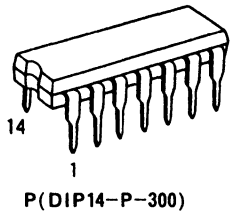
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output.

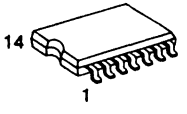
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

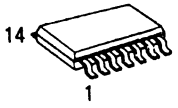
FEATURES:

- High Speed ..... t_{pd}=5.3ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 11



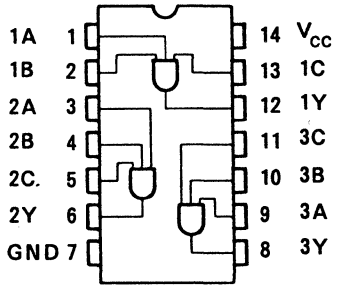
P(DIP14-P-300)





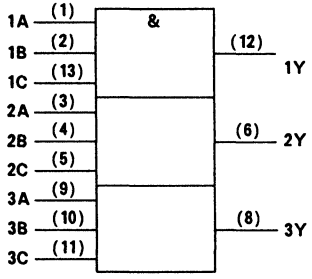
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	7.6	13.0	1.0	15.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.6	1.0	9.9	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	70	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{ (per Gate)}$$

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	8.0	14.0	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.0	9.0	1.0	10.2	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	63	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{(per Gate)}$$

TC74AC14P/F/FN

HEX SCHMITT INVERTER

The TC74AC14 is an advauced high speed CMOS SCHMITT INVERTER fabricated with silicon gate and double-layer metal wiring C²MOS technology.

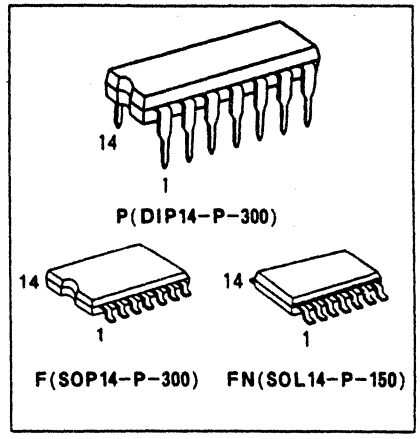
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74AC04 but the inputs have hysteresis and with its schmitt trigger function, the TC74AC14 can be used as a line receivers which will receive slow input signals.

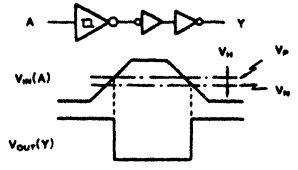
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

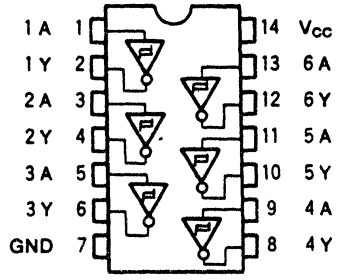
- High Speed ..... t_{pd}=5.3ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F14



SYSTEM DIAGRAM,WAVEFORM

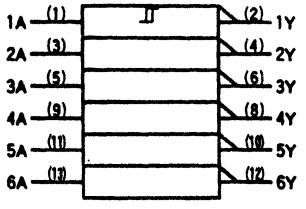


PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			3.0 4.5 5.5	− − −	− − −	2.2 3.2 3.9	− − −	2.2 3.2 3.9	V
Negative Threshold Voltage	V_N			3.0 4.5 5.5	0.5 0.9 1.1	− − −	− − −	0.5 0.9 1.1	− − −	V
Hysteresis Voltage	V_H			3.0 4.5 5.5	0.3 0.4 0.5	− − −	1.2 1.4 1.6	0.3 0.4 0.5	1.2 1.4 1.6	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	8.1	13.2	1.0	15.0	ns
	t_{pHL}		5.0±0.5	−	6.0	9.7	1.0	11.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	29	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

DUAL 4-INPUT NAND GATE

The TC74AC20 is an advanced high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

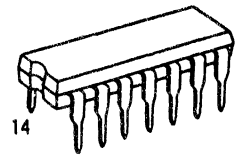
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

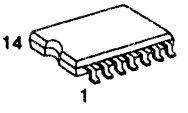
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=4.1(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 20



P(DIP14-P-300)



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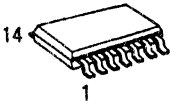

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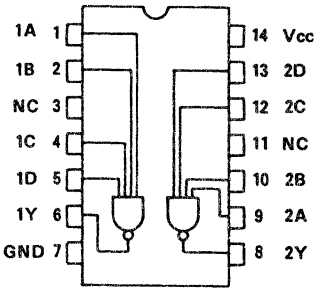
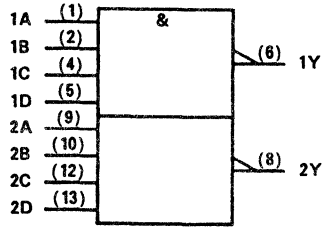
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input t_r=t_f=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.0	10.0	1.0	11.4	ns
	t_{pHL}		5.0±0.5	−	4.8	7.0	1.0	8.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	66	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

QUAD 2-INPUT OR GATE

The TC74AC32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

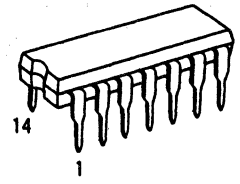
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

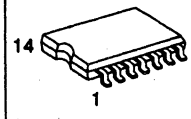
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

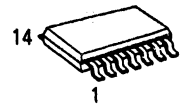
FEATURES:

- High Speed ····· t_{pd}=4.1ns (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F32



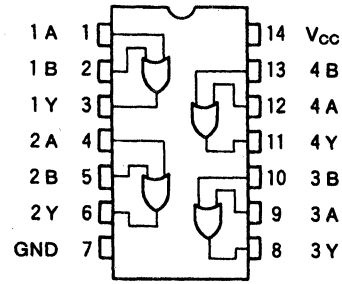
P(DIP14-P-300)





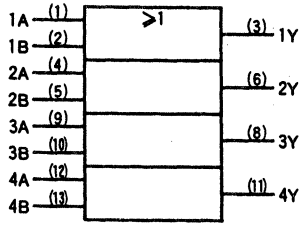
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.1	10.3	1.0	11.9	ns
	t_{pHL}		5.0±0.5	−	5.2	7.4	1.0	8.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	64	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

QUAD 2-INPUT OR GATE

The TC74ACT32 is an advanced high speed CMOS 2-INPUT OR GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

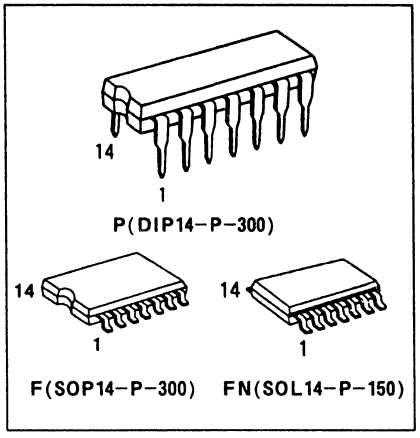
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

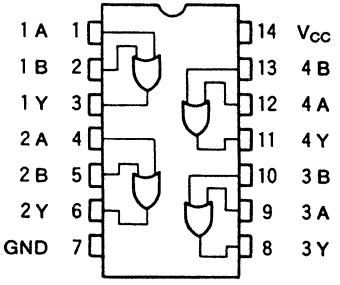
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} = 4.5ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4 μA (Max.) at Ta = 25°C
- Compatible with TTL outputs····· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F32

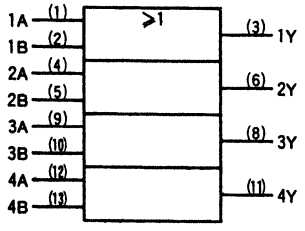


PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =Vcc or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =Vcc or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: Vcc or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.2	7.9	1.0	9.0	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	22	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74AC74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

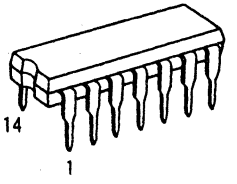
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

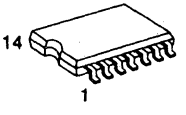
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

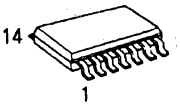
FEATURES:

- High Speed ..... f_{max}=200MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 74



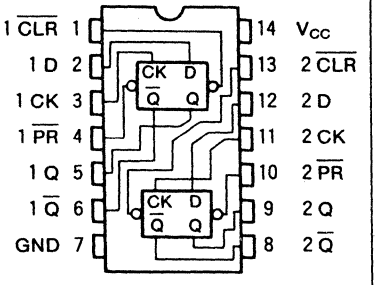
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



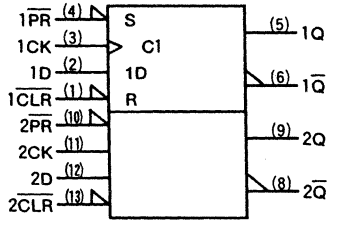
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

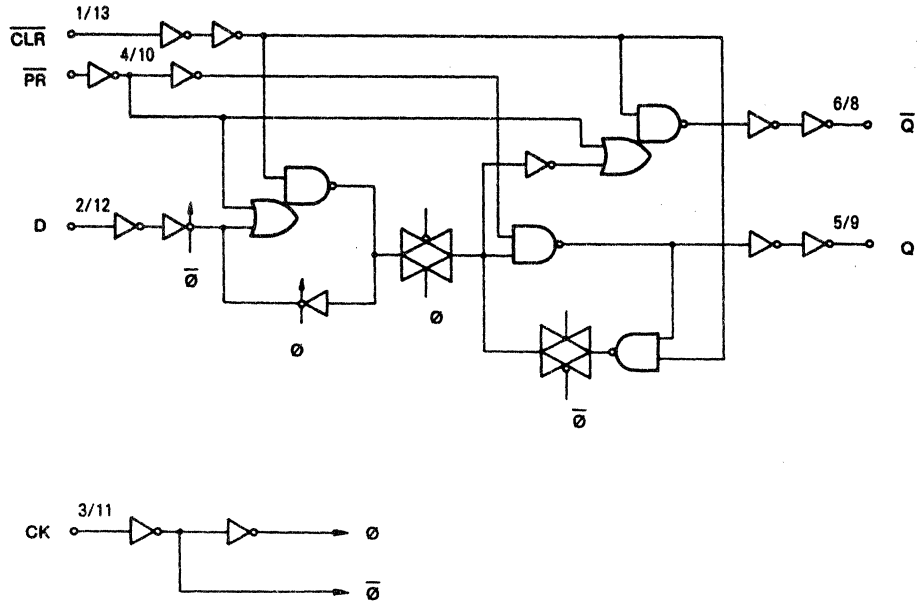
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40∼85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	ns
	$t_{W(H)}$		5.0±0.5	−	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	6.0	6.0	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3±0.3	−	4.0	4.0	
			5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.2	13.9	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.0	13.1	1.0	15.0	
	t_{pHL}		5.0±0.5	−	5.7	8.2	1.0	9.4	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	60	120	−	60	−	MHz
			5.0±0.5	100	160	−	100	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	77	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74ACT74 is an advanced high speed CMOS D-FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

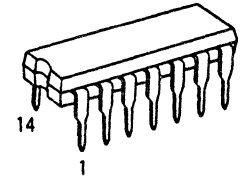
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

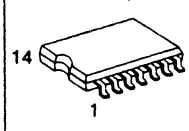
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

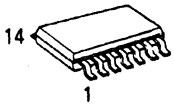
FEATURES:

- High Speed ····· f_{max}=180MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.) at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V (Max.)
  V_{IH}=2V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 74



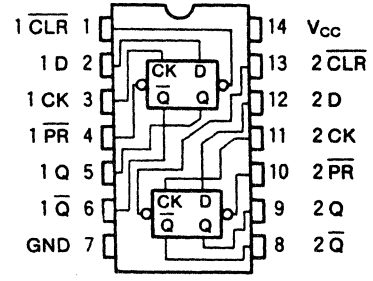
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



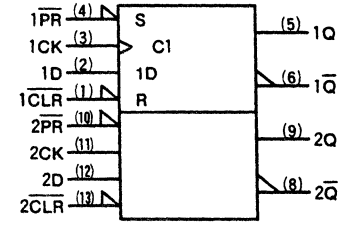
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

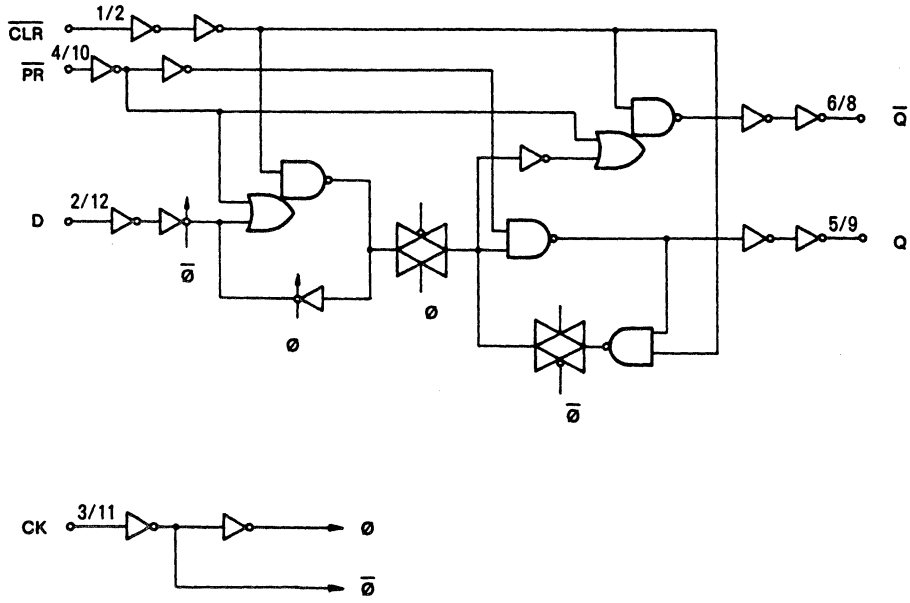
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		5.0±0.5	−	5.7	6.5	
Minimum Set−up Time	t_s		5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		5.0±0.5	−	1.5	1.5	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.1	9.2	1.0	10.5	ns
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.5	10.5	1.0	12.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	95	160	−	95	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	35	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

TC74AC86P/F/FN

QUAD EXCLUSIVE OR GATE

The TC74AC86 is an advanced high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

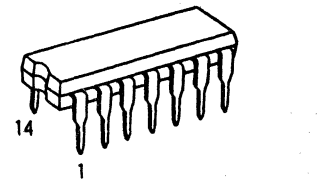
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The internal circuit includes an output buffer, which provides high noise immunity and stable output.

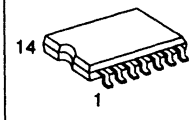
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

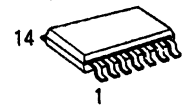
FEATURES:

- High Speed ..... t_{pd}=4.4ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 86



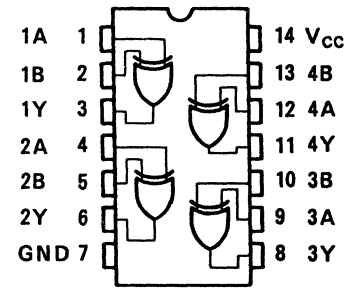
P(DIP14-P-300)





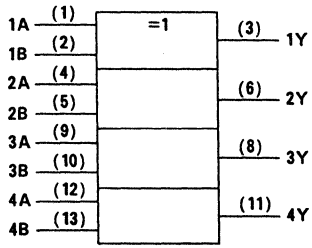
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	7.6	12.3	1.0	14.0	ns
	t_{pHL}		5.0±0.5	−	5.6	8.3	1.0	9.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	56	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4\text{(per Gate)}$$

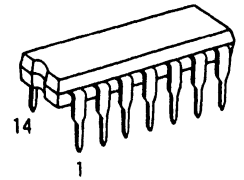
QUAD EXCLUSIVE OR GATE

The TC74ACT86 is an advanced high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

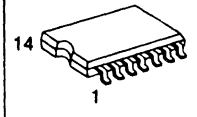
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

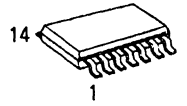
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL. NMOS and CMOS output voltage levels. The internal circuit includes an output buffer, which provides high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP14-P-300)



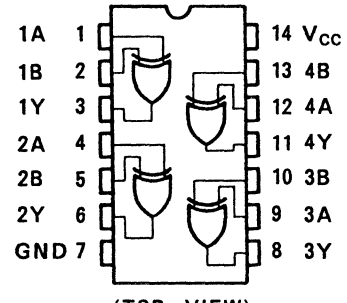


F(SOP14-P-300) FN(SOL14-P-150)

FEATURES:

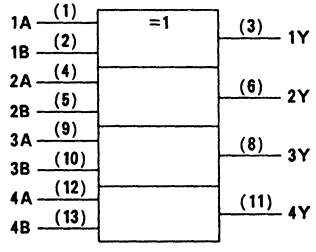
- High Speed ..... t_{pd} = 5.0ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4 μA (Max.) at Ta = 25°C
- Compatible with TTL outputs ..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 86

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.7	10.5	1.0	12.0	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	23	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DUAL J-$\overline{K}$ FLIP FLOP WITH PRESET AND CLEAR

The TC74AC109 is an advanced high speed CMOS DUAL J-$\overline{K}$ FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

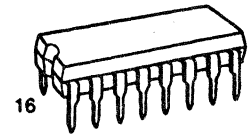
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

In accordance with the logic level on the J and $\overline{K}$ inputs this device changes state on the positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

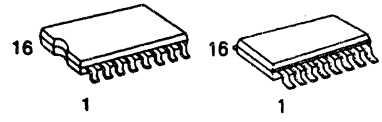
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=200MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~5.5V
- Pin and Function Compatible with 74F109

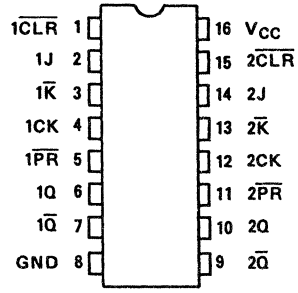


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



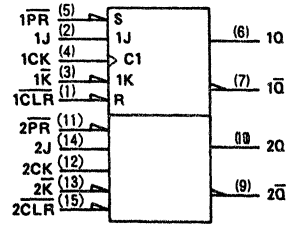
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	L	↓	L	H	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

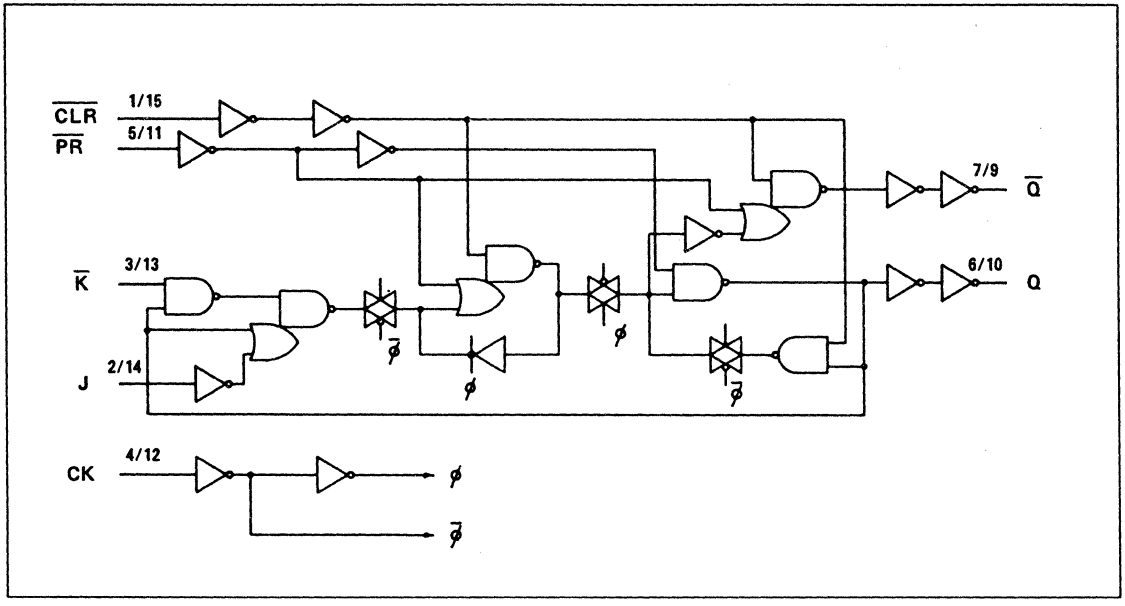
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40∼85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3±0.3	−	8.0	8.0	ns
	$t_{W(H)}$		5.0±0.5	−	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set-Pulse Time	t_s		3.3±0.3	−	9.0	9.0	
			5.0±0.5	−	5.0	5.0	
Minimum Hold Time	t_h		3.3±0.3	−	0.0	0.0	
			5.0±0.5	−	0.0	0.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3±0.3	−	3.0	3.0	
			5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.2	13.9	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.5	14.4	1.0	16.6	
	t_{pHL}		5.0±0.5	−	6.4	9.1	1.0	10.5	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	55	120	−	55	−	MHz
			5.0±0.5	100	160	−	100	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	82	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

TC74ACT109P/F/FN

DUAL J-$\overline{K}$ FLIP FLOP WITH PRESET AND CLEAR

The TC74ACT109 is an advanced high speed CMOS DUAL J-$\overline{K}$ FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

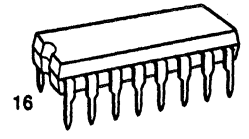
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

In accordance with the logic level applied to the J and $\overline{K}$ inputs, the output changes state on the positive going transition of the clock pulse. $\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and are accomplished by a low logic level on their inputs.

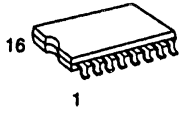
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

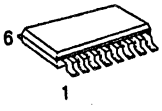
FEATURES:

- High Speed ..... f_{MAX}=185MHz (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- Compatible with TTL outputs ..... V_{IL}=0.8V(Max.)
  V_{IH}=2V(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 109



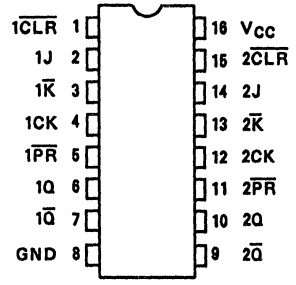
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



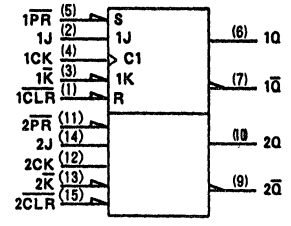
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	L	↓	L	H	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

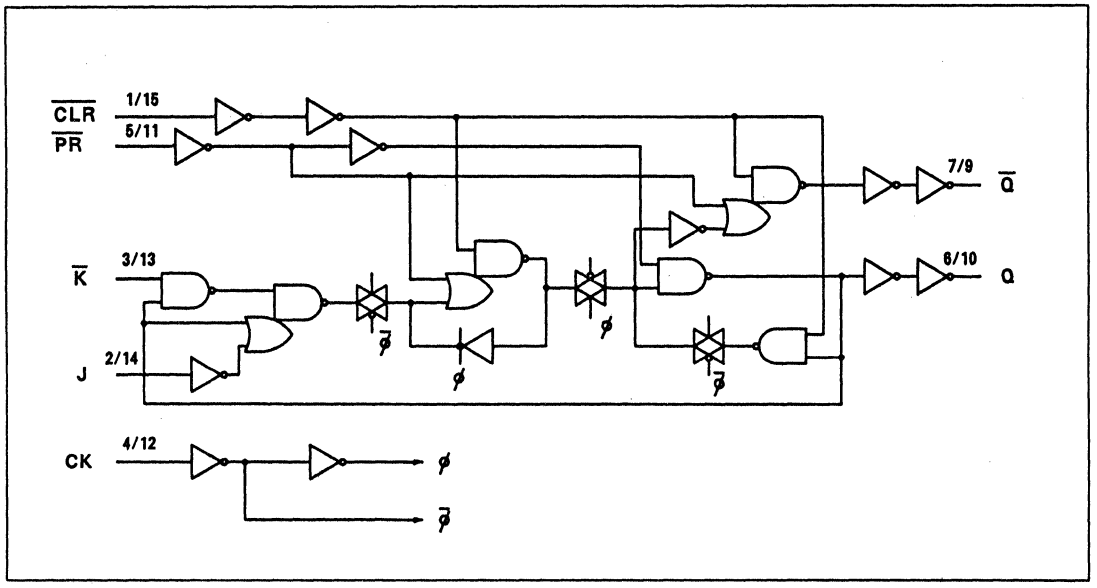
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{cc}	PER INPUT: V_{CC}=3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5	5	ns
Minimum Pulse Width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$		5.0±0.5	−	5	5	
Minimum Set−up Time	t_s		5.0±0.5	−	5	5	
Minimum Hold Time	t_h		5.0±0.5	−	2	2	
Minimum Removal Time ($\overline{CLR}$,$\overline{PR}$)	t_{rem}		5.0±0.5	−	3	3	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.1	10.4	1.0	11.4	ns
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.3	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	85	160	−	85	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	30	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

TC74AC112P/F/FN

DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74AC112 is an advanced high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

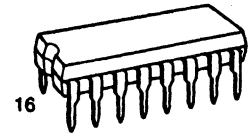
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

In accordance with the logic level on the J and $\overline{K}$ inputs this device changes state on the negative going transition of the clock pulse. $\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and accomplished by a low logic level on the corresponding input.

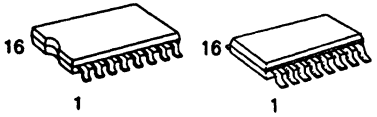
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=170MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 112

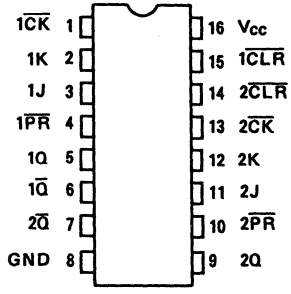


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



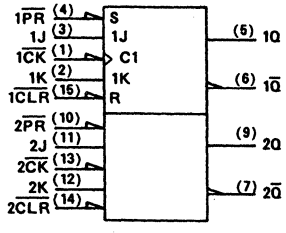
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

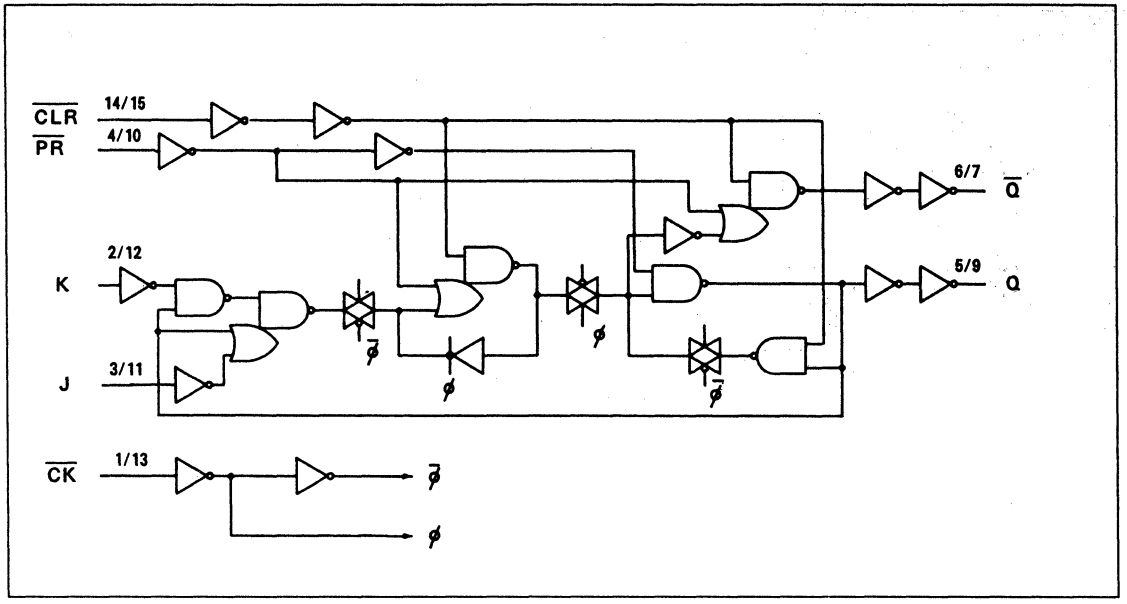
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	4.0	−	40.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25℃			Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	7.5 5.0	7.5 5.0	ns
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	
Minimum Set-up Time	t_s		3.3±0.3 5.0±0.5	− −	11.0 6.0	11.0 6.0	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	0.0 0.0	0.0 0.0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		3.3±0.3 5.0±0.5	− −	3.0 2.0	3.0 2.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CK}$-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	9.1	15.5	1.0	17.8	ns
	t_{pHL}		5.0±0.5	−	6.5	9.4	1.0	10.8	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.6	14.6	1.0	16.8	
	t_{pHL}		5.0±0.5	−	5.8	8.3	1.0	9.6	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	45	90	−	45	−	MHz
			5.0±0.5	80	150	−	80	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	85	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

TC74AC125P/F/FN, TC74AC126P/F/FN

TC74AC125P/F/FN QUAD BUS BUFFER
TC74AC126P/F/FN QUAD BUS BUFFER

The TC74AC125/126 are advanced high speed CMOS QUAD BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

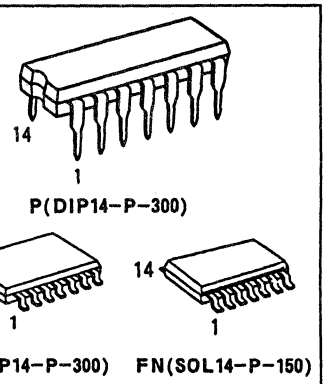
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74AC125 requires the 3-state control input $\overline{G}$ to be set high to place the output into the high impedance state, whereas the TC74AC126 requires the control input to be set low to place the output into high impedance.

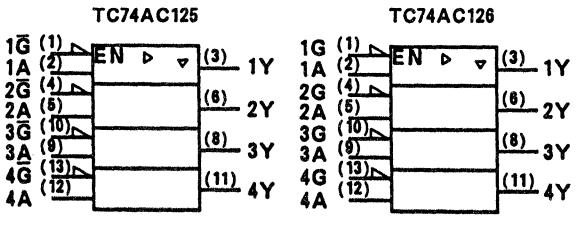
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

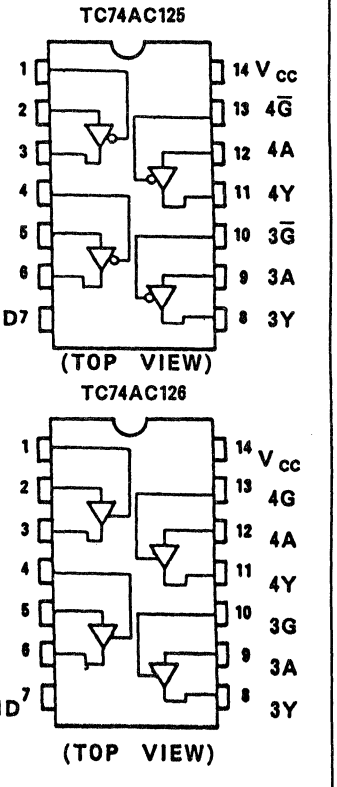
- High Speed ..... t_{pd}=4.7ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 125/126



IEC LOGIC SYMBOL



PIN ASSIGNMENT



TRUTH TABLE

TC74AC125

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X : Don't Care
Z : High Impedance

TC74AC126

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X : Don't Care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH}		3.3±0.3	−	6.4	10.5	1.0	12.0	ns
	t_{pHL}		5.0±0.5	−	4.7	7.0	1.0	8.0	
Output Enable Time	t_{pZL}		3.3±0.3	−	7.1	12.3	1.0	14.0	
	t_{pZH}		5.0±0.5	−	5.0	7.9	1.0	9.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	5.1	8.8	1.0	10.0	
	t_{pHZ}		5.0±0.5	−	4.6	6.6	1.0	7.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)			−	24	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

3-TO-8 LINE DECODER

The TC74AC138 is an advanced high speed CMOS 3-to-8 DECODER fabricated with sillicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs ($\overline{Y}0-\overline{Y}7$) will go low.

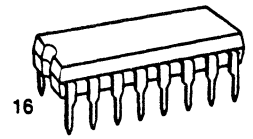
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

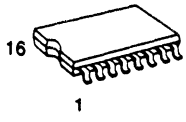
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

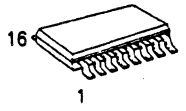
FEATURES:

- High Speed ..... t_{pd}=5.9ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 138



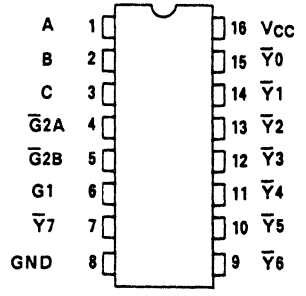
P(DIP16-P-300A)





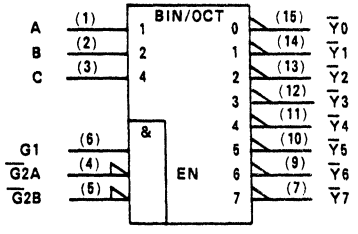
F(SOP16-P-300) FN(SOL16-P-150)

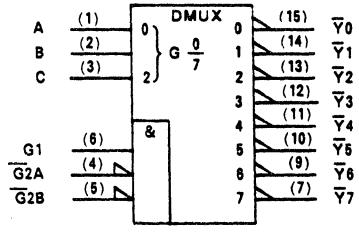
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL





ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

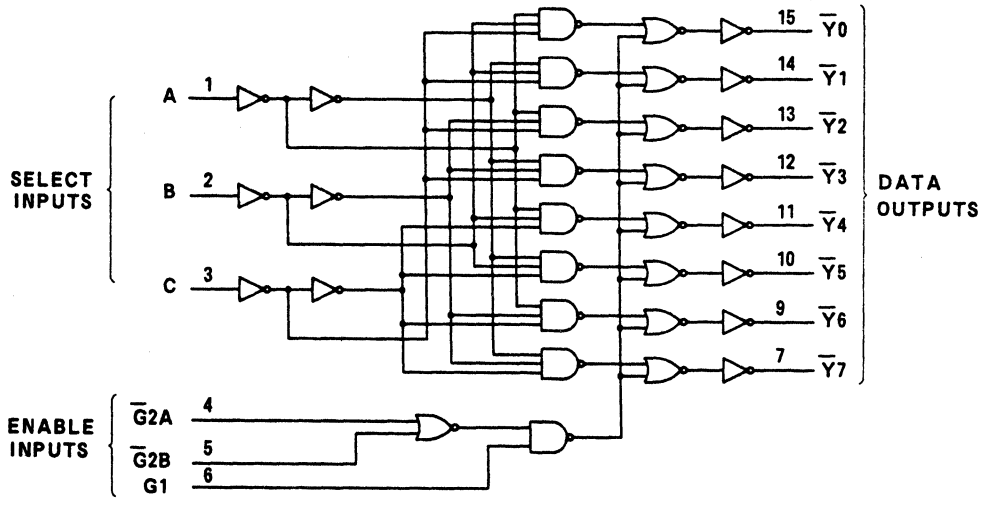
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : DON'T CARE

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH}		3.3±0.3	−	8.5	14.2	1.0	16.3	ns
	t_{pHL}		5.0±0.5	−	6.4	9.2	1.0	10.5	
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH}		3.3±0.3	−	7.5	12.8	1.0	14.7	
	t_{pHL}		5.0±0.5	−	6.1	8.9	1.0	10.2	
Propagation Delay Time ($\overline{G2}$−$\overline{Y}$)	t_{pLH}		3.3±0.3	−	8.8	15.0	1.0	17.3	
	t_{pHL}		5.0±0.5	−	7.2	10.5	1.0	12.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	143	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

3-TO-8 LINE DECODER

The TC74ACT138 is an advanced high speed CMOS 3-to-8 LINE DECODER fabricated with sillicon gate and double -layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs ($\overline{Y}0$-$\overline{Y}1$) will go low.

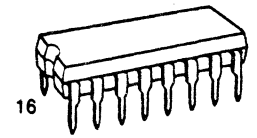
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

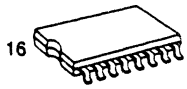
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

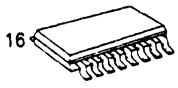
FEATURES:

- High Speed ····· t_{pd}=6.0ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.) at Ta=25℃
- Compatible with TTL outputs····· V_{IL} =0.8V (Max.)
  V_{IH} =2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|$ = I_{OL} =24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F138



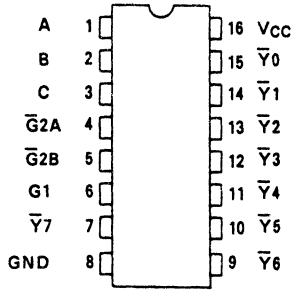
P(DIP16-P-300A)





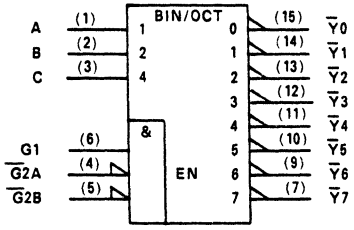
F(SOP16-P-300) FN(SOL16-P-150)

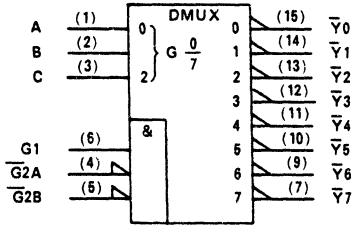
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL





ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =Vcc or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =Vcc or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:Vcc or GND		5.5	−	−	1.35	−	1.5	mA

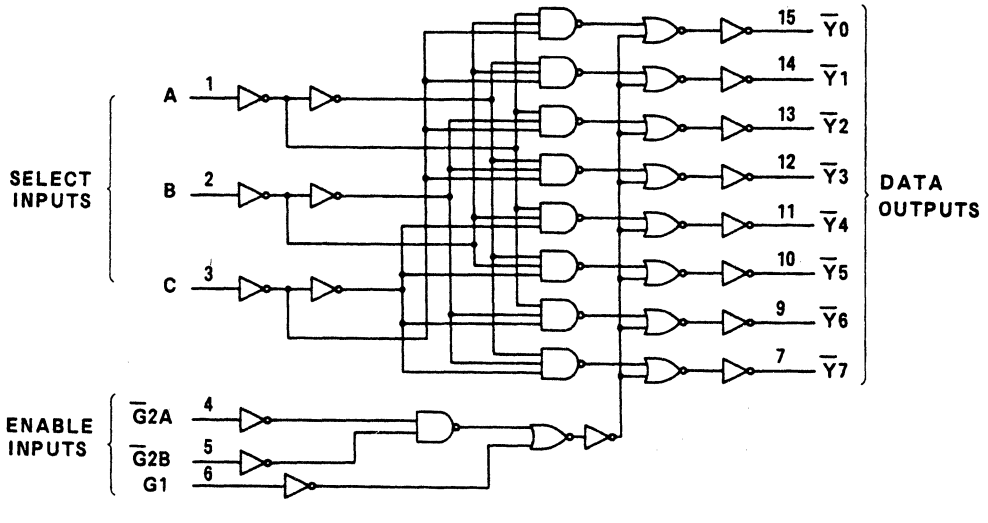
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : DON'T CARE

LOGIC DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.7	10.1	1.0	11.5	ns
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.8	10.5	1.0	12.0	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.9	11.0	1.0	12.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	55	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DUAL 2-TO-4 LINE DECODER

The TC74AC139 is an advanced high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

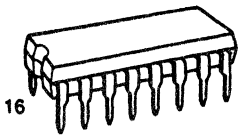
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held high, all four outputs are fixed at a high logic level independent of the other inputs.

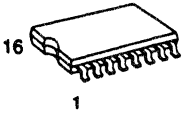
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.

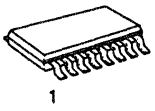
FEATURES:

- High Speed ····· t_{pd}=5.9ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~5.5V
- Pin and Function Compatible with 74F139



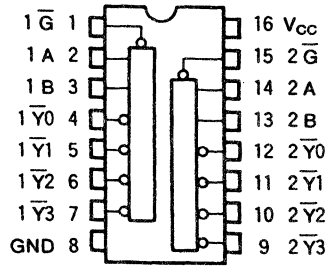
P(DIP16-P-300A)





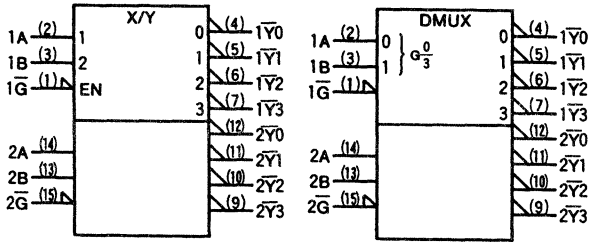
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
G̅	B	A	Y̅0	Y̅1	Y̅2	Y̅3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y̅0
L	L	H	H	L	H	H	Y̅1
L	H	L	H	H	L	R	Y̅2
L	H	H	H	H	H	L	Y̅3

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

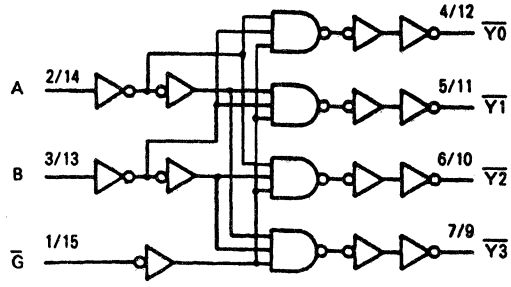
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A,B−$\overline{Y}$)	t_{pLH}		3.3±0.3	−	8.2	13.9	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.2	9.0	1.0	10.3	
Propagation Delay Time (G−$\overline{Y}$)	t_{pLH}		3.3±0.3	−	7.6	12.9	1.0	14.8	
	t_{pHL}		5.0±0.5	−	5.8	8.5	1.0	9.6	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	110	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

DUAL 2-TO-4 LINE DECODER

The TC74ACT139 is an advanced high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate and double-layer metal wiring C^2 MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

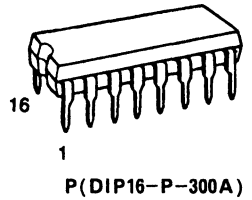
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held high, all four outputs are fixed at a high logic level independent of the other inputs.

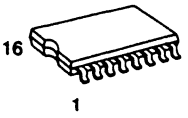
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.

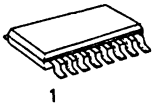
FEATURES:

- High Speed ..... t_{pd} = 5.5ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 4 μA(Max.) at Ta=25℃
- Compatible with TTL outputs ..... V_{IL} = 0.8V(Max.)
  V_{IH} = 2.0V(Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{PLH} \fallingdotseq t_{PHL}$
- Pin and Function Compatible with 74F 139



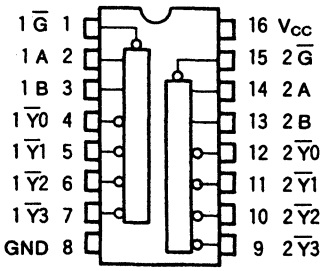
P(DIP16-P-300A)





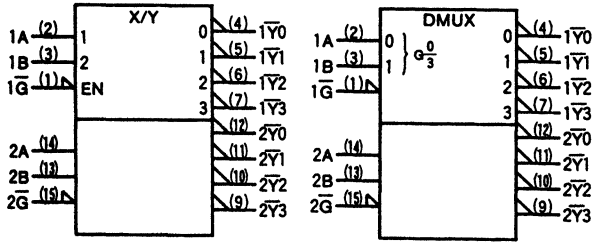
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
$\overline{G}$	B	A	$\overline{Y}$0	$\overline{Y}$1	$\overline{Y}$2	$\overline{Y}$3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	$\overline{Y}$0
L	L	H	H	L	H	H	$\overline{Y}$1
L	H	L	H	H	L	H	$\overline{Y}$2
L	H	H	H	H	H	L	$\overline{Y}$3

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 6.0	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

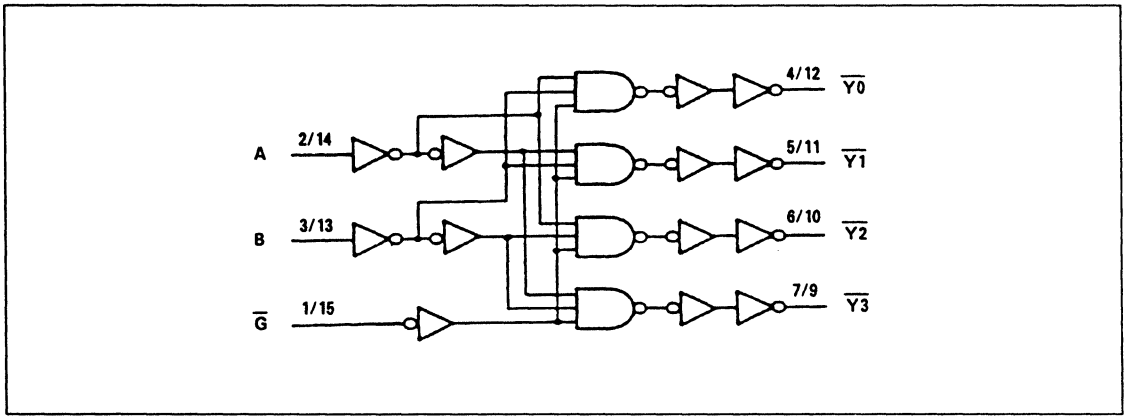
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B, $-\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.2	9.2	1.0	10.5	ns
Propagation Delay Time ($\overline{G}$, $-\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.3	9.6	1.0	11.0	ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	51	−	−	−	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

TC74AC151P/F/FN 8-CHANNEL MULTIPLEXER
TC74AC251P/F/FN 8-CHANNEL MULTIPLEXER (3-STATE)

The TC74AC151 and the TC74AC251 are advanced high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

One of eight data input signals (D0–D7) is selected by decoding of the three-bit address input (A, B, C). The selected data appears on two outputs : non-inverting (Y) and inverting (W).

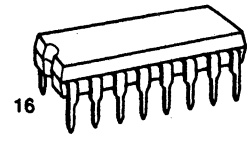
The $\overline{\text{STROBE}}$ input provides two output conditions ; a low level on the $\overline{\text{STROBE}}$ input transfers the selected data to the outputs. A high level on the $\overline{\text{STROBE}}$ input of AC151 sets the Y output low and the W output high without regard to the data or select input conditions.

When the $\overline{\text{STROBE}}$ input of AC251 is held high, both outputs are in the high-impedance state.

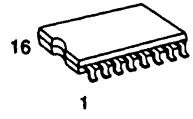
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

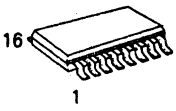
FEATURES:

- High Speed ····· t_{pd}=5.3ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~5.5V
- Pin and Function Compatible with 74F 151/251



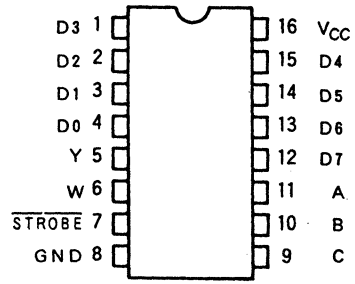
P(DIP16-P-300A)





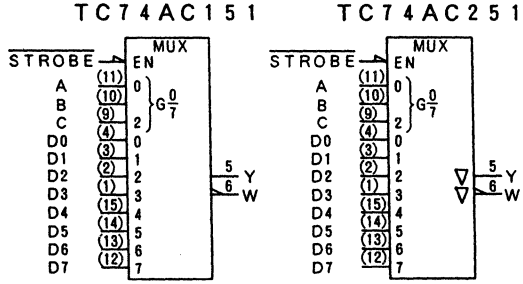
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS				OUTPUTS			
SELECT			$\overline{\text{STROBE}}$	AC151		AC251	
C	B	A		Y	W	Y	W
X	X	X	H	L	H	Z	Z
L	L	L	L	D0	$\overline{D0}$	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$	D7	$\overline{D7}$

Z:High Impedance
X:Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

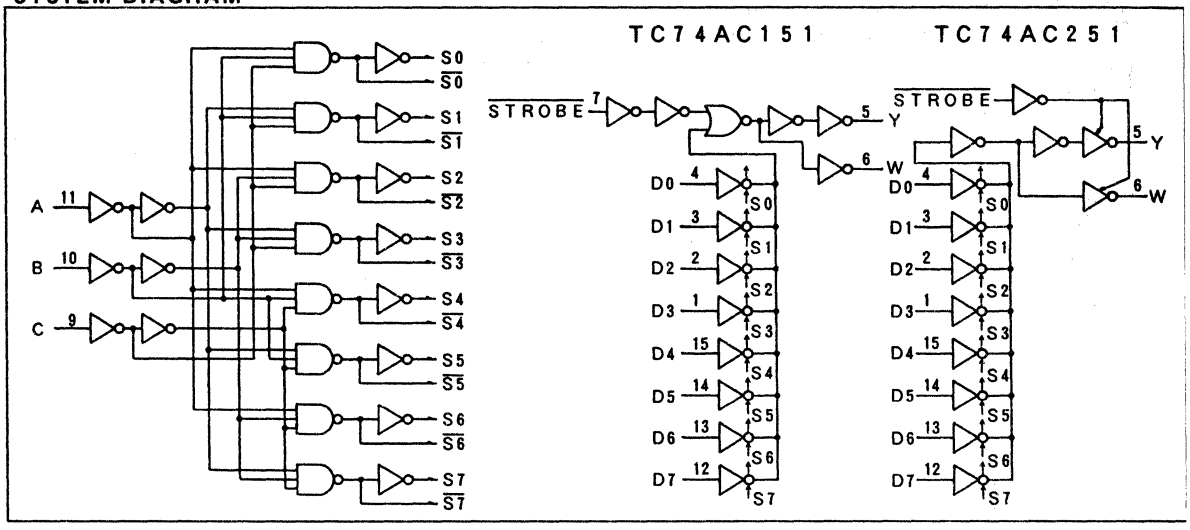
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*1	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*1	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output *2 Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	V
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA

* 1 :This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.
* 2 :for TC74AC251 only.

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=500Ω, Input t_r=t_f=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (D−Y.W)	t_{pLH}		3.3±0.3	−	10.7	19.3	−	22.0	ns
	t_{pHL}		5.0±0.5	−	6.6	10.5	−	12.0	
Propagation Delay Time (A, B, C−Y.W)	t_{pLH}		3.3±0.3	−	13.3	23.7	−	27.0	
	t_{pHL}		5.0±0.5	−	8.2	13.0	−	14.8	
Propagation Delay Time ($\overline{ST}$−Y.W) *	t_{pLH}		3.3±0.3	−	8.6	15.3	−	18.0	
	t_{pHL}		5.0±0.5	−	5.6	9.6	−	11.0	
Output Enable Time **	t_{pZL}		3.3±0.3	−	6.4	13.2	−	15.0	
	t_{pZH}		5.0±0.5	−	4.4	7.9	−	9.0	
Output Disable Time **	t_{pLZ}		3.3±0.3	−	5.9	11.4	−	13.0	
	t_{pHZ}		5.0±0.5	−	5.0	8.8	−	10.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance **	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74AC151		−	68	−	−	−	
		TC74AC251		−	72	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2) * for TC74AC151 only
** for TC74AC251 only

TC74ACT151P/F/FN 8-CHANNEL MULTIPLEXER
TC74ACT251P/F/FN 8-CHANNEL MULTIPLEXER (3-STATE)

The TC74ACT151 and the TC74ACT251 are advanced high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

One of eight date input signals (D0-D7) is selected by decoding of the three-bit address input (A, B, C). The selected data appears on two outputs : non-inverting (Y) and inverting (W).

The designer has a choice of complementary output (ACT151) and 3-state output (ACT251).

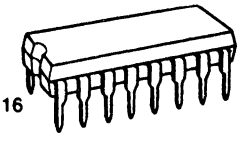
The STROBE input provides two output conditions ; a low level on the STROBE input transfers the selected data to the outputs. A high level on the STROBE input of ACT151 sets the Y output low and the W output high without regard to the data or select input conditions.

When the $\overline{\text{STROBE}}$ input of ACT251 is held high, both outputs are in the high-impedance state.

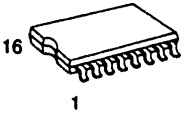
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

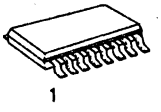
FEATURES:

- High Speed ..... t_{pd} = 7.1ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8 μA (Max.) at Ta = 25°C
- Compatible with TTL outputs..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F151/251



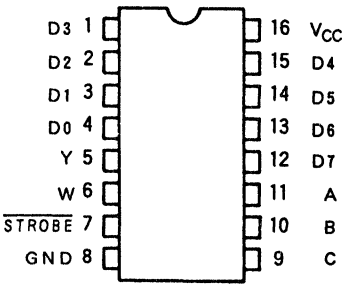
P(DIP16-P-300A)





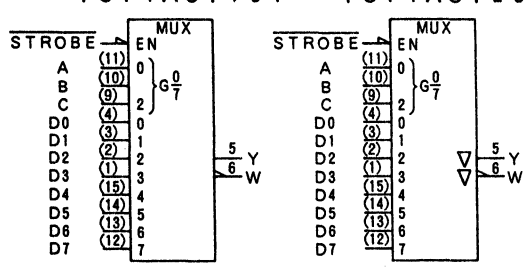
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS				OUTPUTS			
SELECT			STROBE	ACT151		ACT251	
C	B	A		Y	W	Y	W
X	X	X	H	L	H	Z	Z
L	L	L	L	D0	$\overline{D0}$	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$	D7	$\overline{D7}$

Z:High Impedance
X:Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

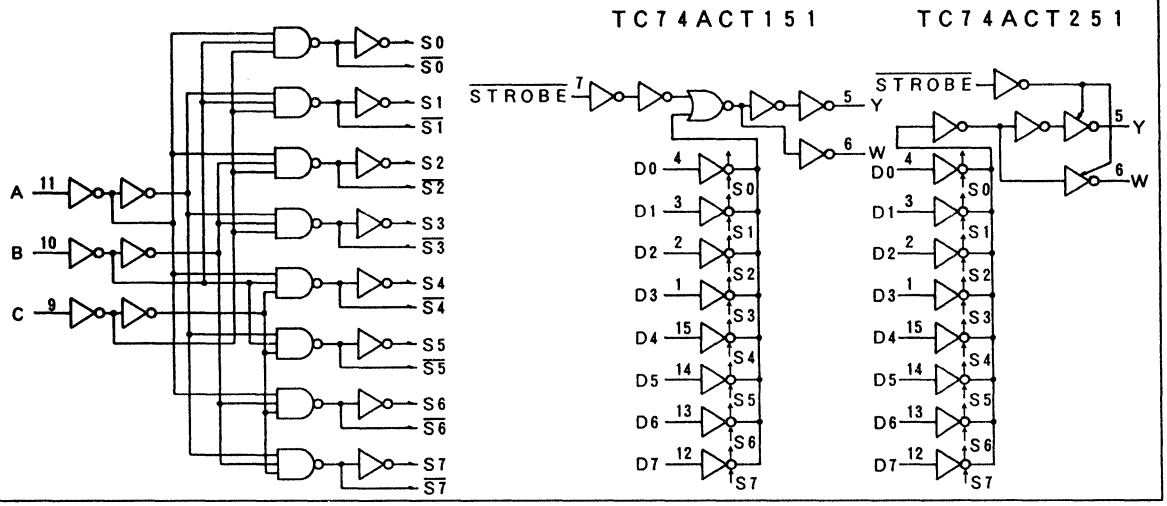
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA* 1	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA* 1	5.5	−	−	−	−	1.65	
3−State Output * 2 Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} = 3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* 1 :This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.
* 2 :for TC74ACT251 only

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (D−Y.W) *	t_{pLH} t_{pHL}		5.0±0.5	−	7.5	11.8	1.0	13.5	ns
Propagation Delay Time (A,B,C−Y.W)*	t_{pLH} t_{pHL}		5.0±0.5	−	9.5	15.8	1.0	18.0	
Propagation Delay Time (D−Y.W) * *	t_{pLH} t_{pHL}		5.0±0.5	−	7.8	12.3	1.0	14.0	
Propagation Delay Time (A,B,C−Y.W) * *	t_{pLH} t_{pHL}		5.0±0.5	−	9.9	16.2	1.0	18.5	
Propagation Delay Time ($\overline{ST}$−Y.W) *	t_{pLH} t_{pHL}		5.0±0.5	−	6.3	10.1	1.0	11.5	
Output Enable Time **	t_{pZL} t_{pZH}		5.0±0.5		5.4	9.6	1.0	11.0	
Output Disable Time **	t_{pLZ} t_{pHZ}		5.0±0.5		5.9	8.8	1.0	10.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance **	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}	TC74ACT151		−	66	−	−	−	
		TC74ACT251		−	72	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2) * for TC74ACT151 only
** for TC74ACT251 only

TC74AC153P/F/FN DUAL 4-CHANNEL MULTIPLEXER
TC74AC253P/F/FN DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74AC153 and TC74AC253 are advanced high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

Both achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipations.

The designer has a choice of complementary output (AC153) or 3-state output (AC253).

Each of the data input groups (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

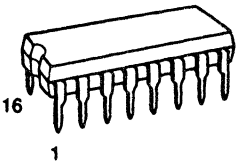
Separate strobes ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections.

The strobe ($\overline{G}$) can be used to inhibit the data output; the output of ACT153 is held low and the output of ACT253 is held in the high impedance state unconditionally, while the strobe input is held low.

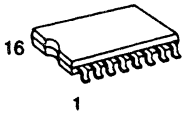
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

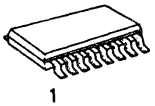
FEATURES:

- High Speed ..... t_{pd}=3.9ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr.)=2V~5.5V
- Pin and Function Compatible with 74F153/253



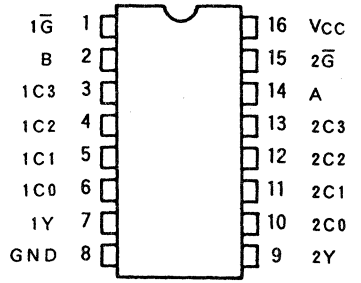
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



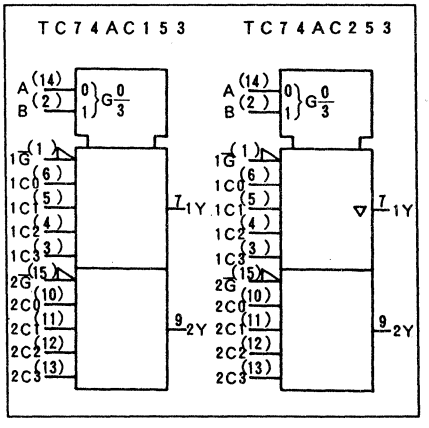
(TOP VIEW)

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C0	C1	C2	C3	$\overline{G}$	AC153	AC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X:Don't care Z:High Impedans

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

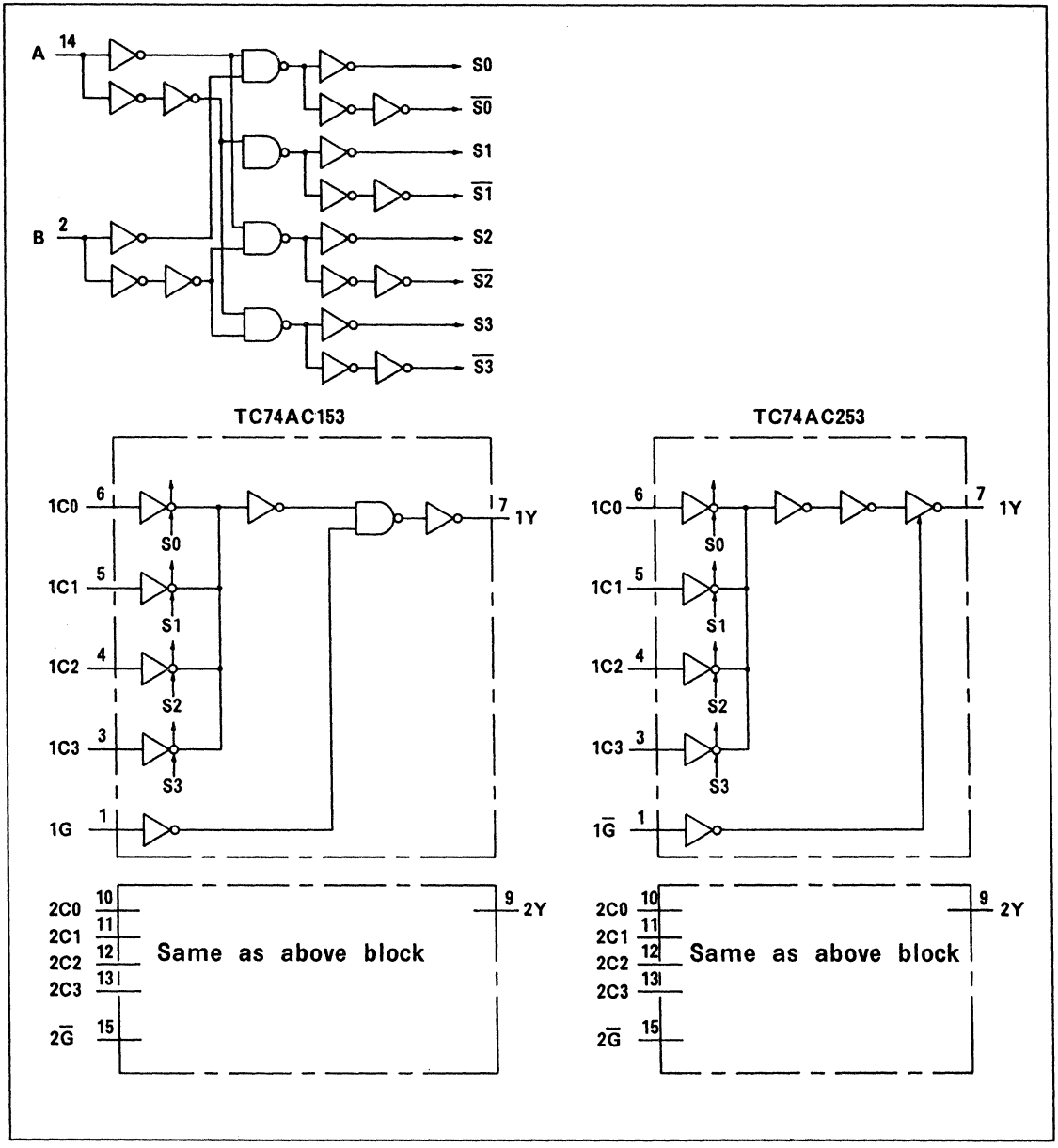
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*1	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*1	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output *2 Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	V
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA

* 1 : This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.
* 2 :for TC74AC153 only

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Cn−Y)	t_{pLH}		3.3±0.3	−	7.6	14.5	1.0	16.5	ns
	t_{pHL}		5.0±0.5	−	5.0	9.0	1.0	10.3	
Propagation Delay Time (A, B−Y)	t_{pLH}		3.3±0.3	−	10.5	20.5	1.0	23.4	
	t_{pHL}		5.0±0.5	−	6.6	10.5	1.0	12.0	
Propagation Delay Time ($\overline{G}$−Y) *	t_{pLH}		3.3±0.3	−	6.8	13.3	1.0	15.2	
	t_{pHL}		5.0±0.5	−	4.4	8.0	1.0	9.1	
Output Enable Time **	t_{pZL}		3.3±0.3	−	6.6	13.3	1.0	15.2	
	t_{pZH}		5.0±0.5	−	4.4	8.0	1.0	9.1	
Output Disable Time **	t_{pLZ}		3.3±0.3	−	5.5	9.0	1.0	10.3	
	t_{pHZ}		5.0±0.5	−	5.0	7.5	1.0	8.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance **	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	54	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2) * for TC74AC153 only

** for TC74AC253 only

TC74ACT153P/F/FN DUAL 4-CHANNEL MULTIPLEXER
TC74ACT253P/F/FN DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74ACT153 and TC74ACT253 are advanced high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

Both achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipations.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The designer has a choice of complementary output (ACT153) or 3-state output (ACT253).

Each of the data input groups (1C0–1C3, 2C0–2C3) is selected by the two address inputs A and B.

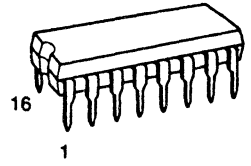
Separate strobes ($1\overline{G}$. $2\overline{G}$) are provided for each of the two four-line sections.

The strobe ($\overline{G}$) can be used to inhibit the data output; the output of ACT153 is held low and the output of ACT253 is held in the high impedance state unconditionally, while the strobe input is held low.

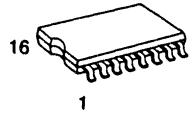
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

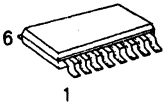
FEATURES:

- High Speed ····· t_{pd} = 5.4ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8 μA (Max.) at Ta = 25℃
- Compatible with TTL outputs····· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F153/253



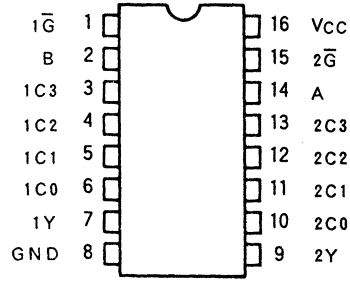
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



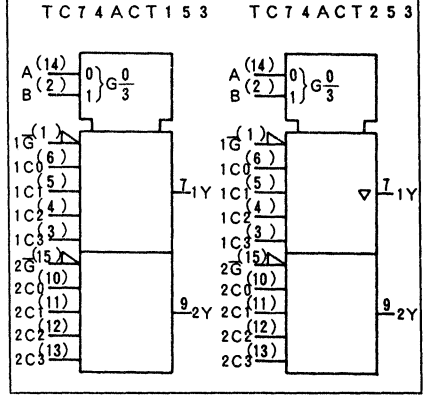
(TOP VIEW)

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C0	C1	C2	C3	$\overline{G}$	ACT153	ACT253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X:Don't care Z:High Impedans

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

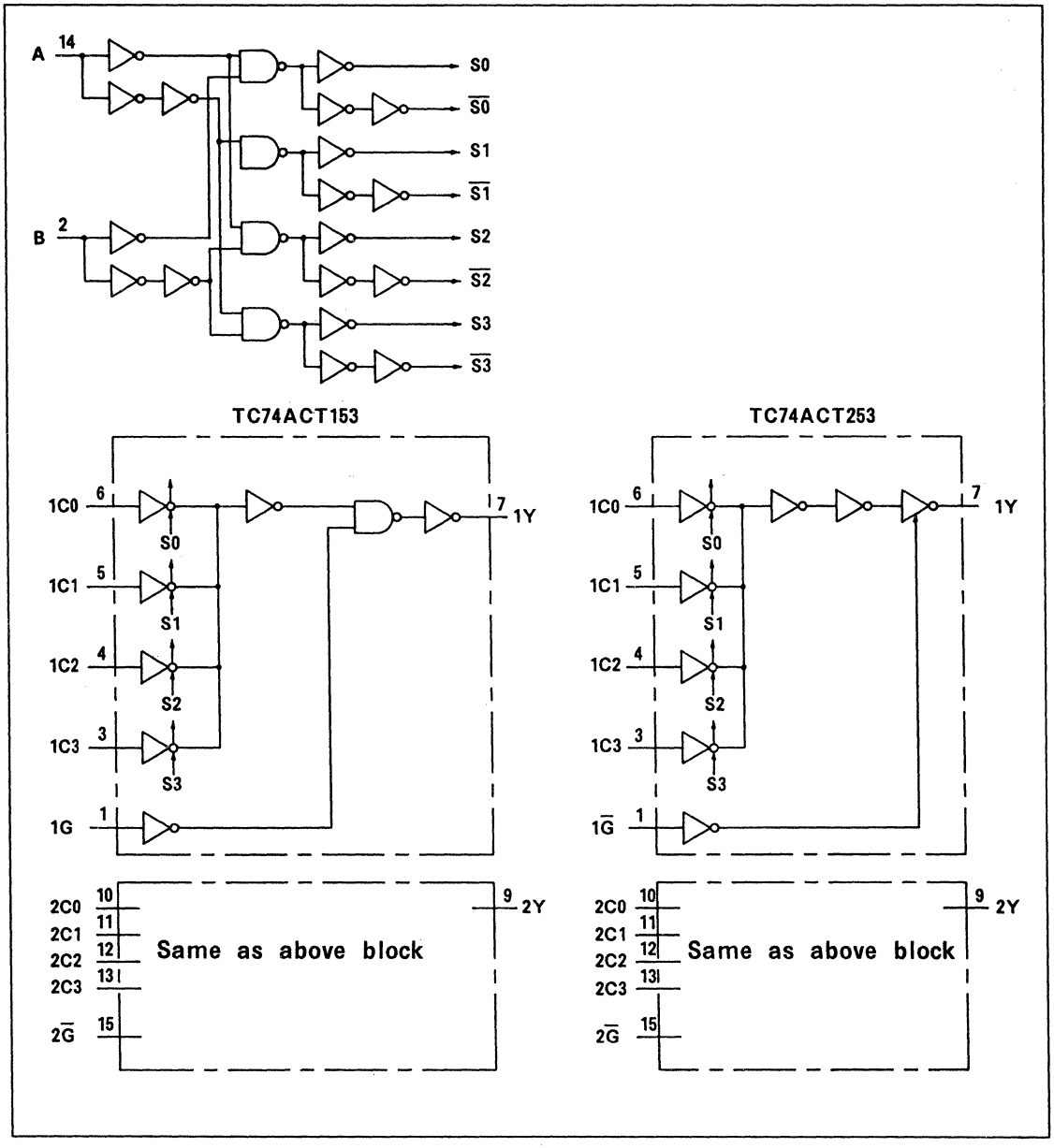
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA* 1	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA* 1	5.5	−	−	−	−	1.65	
3−State Output * 2 Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* 1 : This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.
* 2 : for TC74ACT253 only

SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Cn−Y)	t_{pLH} t_{pHL}		5.0±0.5	−	6.1	9.7	1.0	11.0	ns
Propagation Delay Time (A, B−Y)	t_{pLH} t_{pHL}		5.0±0.5	−	7.8	11.8	1.0	13.5	
Propagation Delay Time ($\overline{G}$−Y) *	t_{pLH} t_{pHL}		5.0±0.5	−	5.6	9.7	1.0	11.0	
Output Enable Time **	t_{pZL} t_{pZH}		5.0±0.5	−	5.3	8.3	1.0	9.5	
Output Disable Time **	t_{pLZ} t_{pHZ}		5.0±0.5	−	5.4	7.5	1.0	8.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance **	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance *	C_{PD}(1)			−	47	−	−	−	
Power Dissipation Capacitance**	C_{PD}(1)			−	50	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

(2) * for TC74ACT153 only
** for TC74ACT253 only

TC74AC157P/F/FN, TC74AC158P/F/FN

TC74AC157P/F/FN QUAD 2-CHANNEL MULTIPLEXER
TC74AC158P/F/FN QUAD 2-CHANNEL MULTIPLEXER (INVERTING)

The TC74AC157 and the TC74AC158 are advanced high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low Power dissipation.

These devices consist of four 2-input digital multiplexers with common select and strobe inputs.

The TC74AC158 is an inverting multiplexer while the TC 74AC157 is a non-inverting multiplexer.

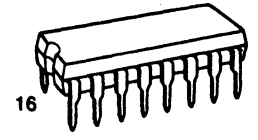
When the $\overline{\text{STROBE}}$ input is held high, selection of the data is inhibited and all the outputs go low in the case of the 157 and high in the case of the 158.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

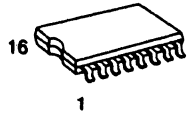
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

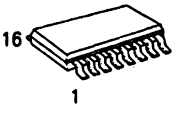
FEATURES:

- High Speed ..... t_{pd}=4.5ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F157/158



P(DIP16-P-300A)

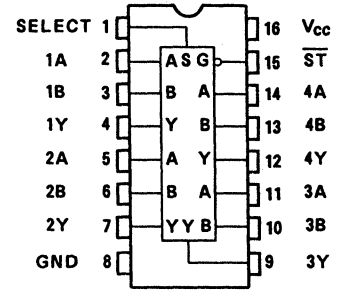




F(SOP16-P-300) FL(SOL16-P-150)

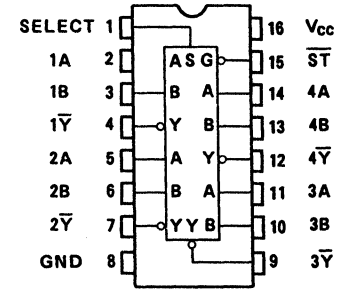
PIN ASSIGNMENT

TC74AC157



(TOP VIEW)

TC74AC158



(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUT	
$\overline{ST}$	SELECT	A	B	Y(157)	$\overline{Y}$(158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

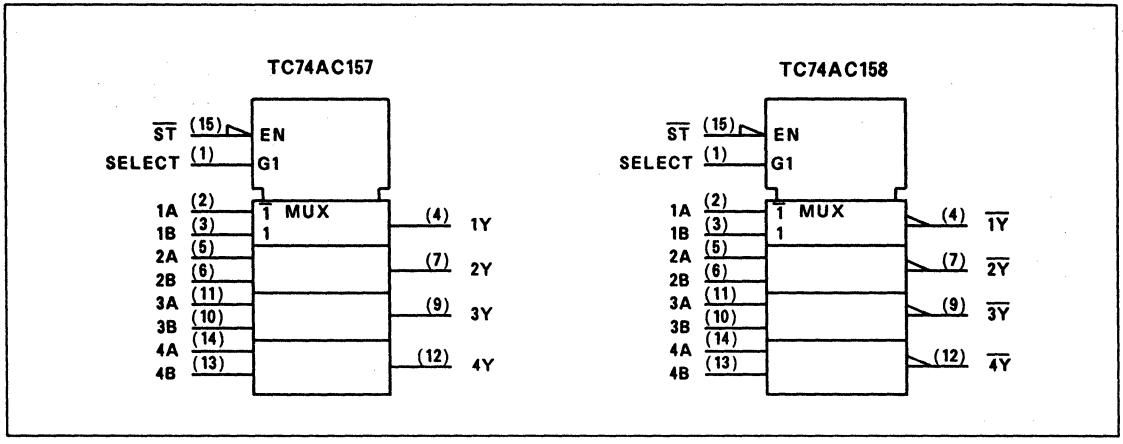
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

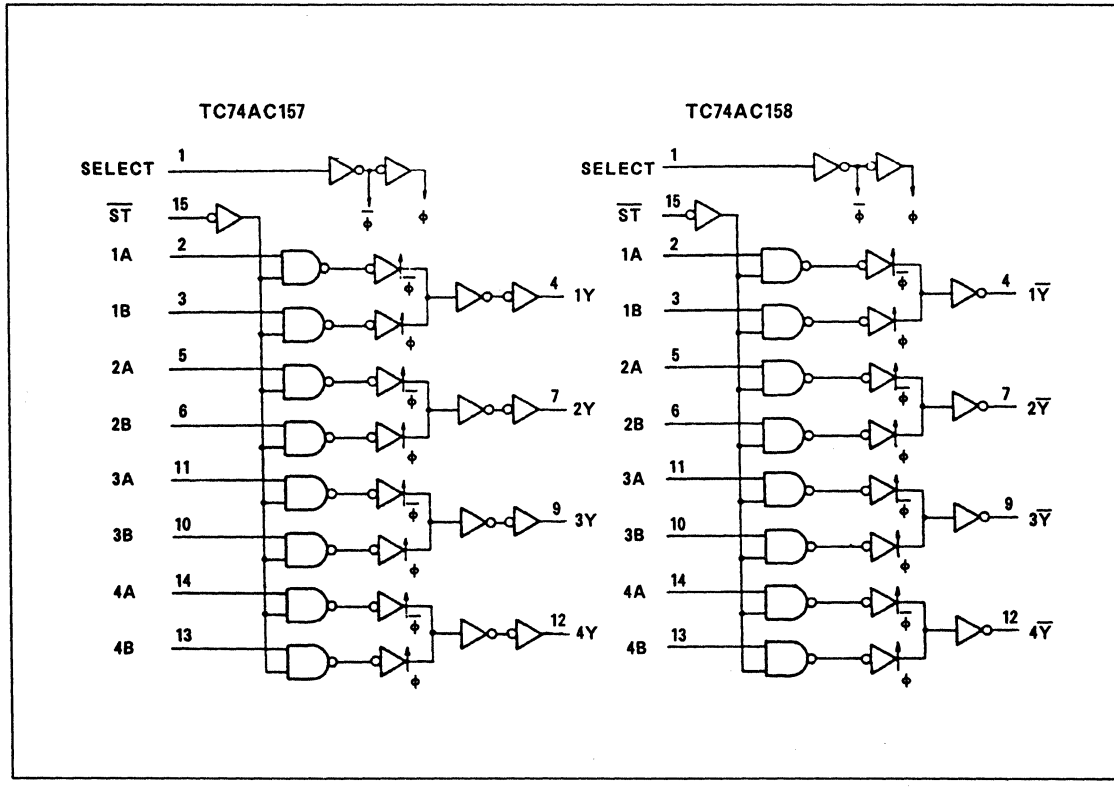
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Input Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Input Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B−Y) *	t_{pLH}		3.3±0.3	−	7.2	12.2	1.0	14.0	ns
	t_{pHL}		5.0±0.5	−	5.5	7.9	1.0	9.1	
Propagation Delay Time (A, B−Y) **	t_{pLH}		3.3±0.3	−	7.3	12.4	1.0	14.3	
	t_{pHL}		5.0±0.5	−	5.7	8.2	1.0	9.4	
Propagation Delay Time (SELECT−Y)	t_{pLH}		3.3±0.3	−	8.5	14.5	1.0	16.7	
	t_{pHL}		5.0±0.5	−	6.3	9.1	1.0	10.5	
Propagation Delay Time (ST−Y)	t_{pLH}		3.3±0.3	−	8.6	14.6	1.0	16.8	
	t_{pHL}		5.0±0.5	−	6.4	9.2	1.0	10.6	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74AC157		−	93	−	−	−	
		TC74AC158		−	98	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

(2) * for TC74AC157 only

** for TC74AC158 only

TC74ACT157P/F/FN QUAD 2-CHANNEL MULTIPLEXER
TC74ACT158P/F/FN QUAD 2-CHANNEL MULTIPLEXER (INVERTING)

The TC74ACT157 and the TC74ACT158 are advanced high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low Power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

These devices consist of four 2-input digital multiplexers with common select and strobe inputs.

The TC74ACT158 is an inverting multiplexer while the TC74ACT157 is a non-inverting multiplexer.

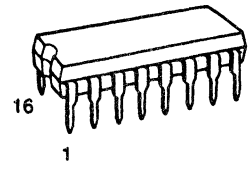
When the STROBE input is held high, selection of the data is inhibited and all the outputs go low in the case of the ACT157 and high in the case of the ACT158.

The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.

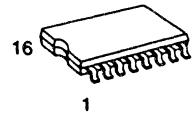
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

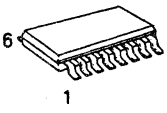
FEATURES:

- High Speed ..... t_{pd} = 5.1ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8μA (Max.) at Ta = 25℃
- Compatible with TTL outputs..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F157/158



P(DIP16-P-300A)

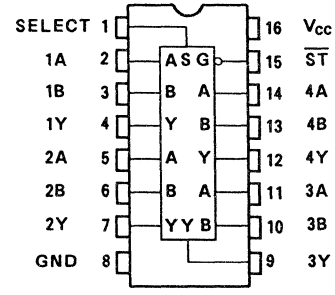




F(SOP16-P-300) FN(SOL16-P-150)

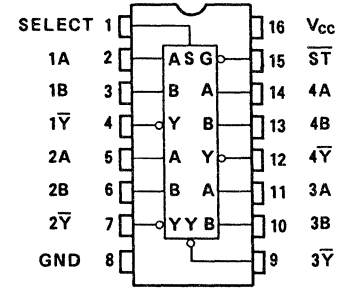
PIN ASSIGNMENT

TC74ACT157



(TOP VIEW)

TC74ACT158



(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUT	
$\overline{ST}$	SELECT	A	B	Y(157)	$\overline{Y}$(158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

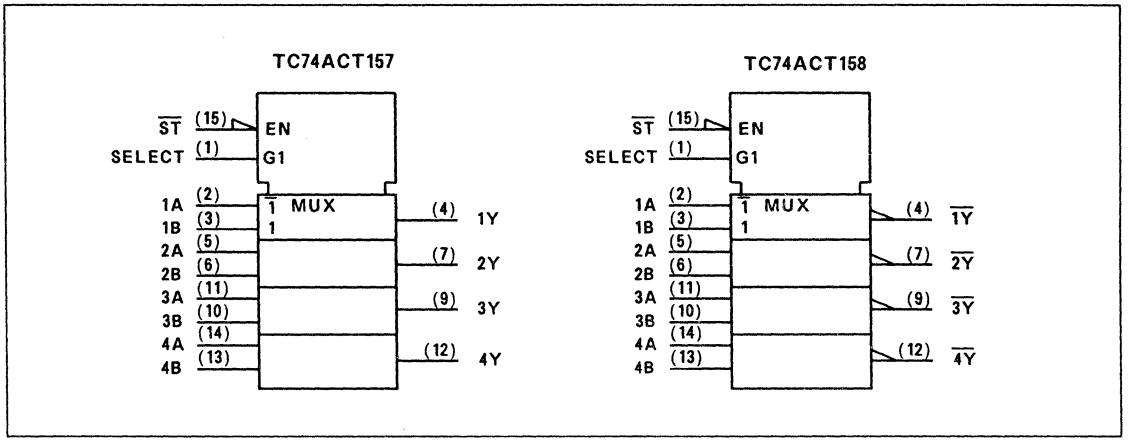
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

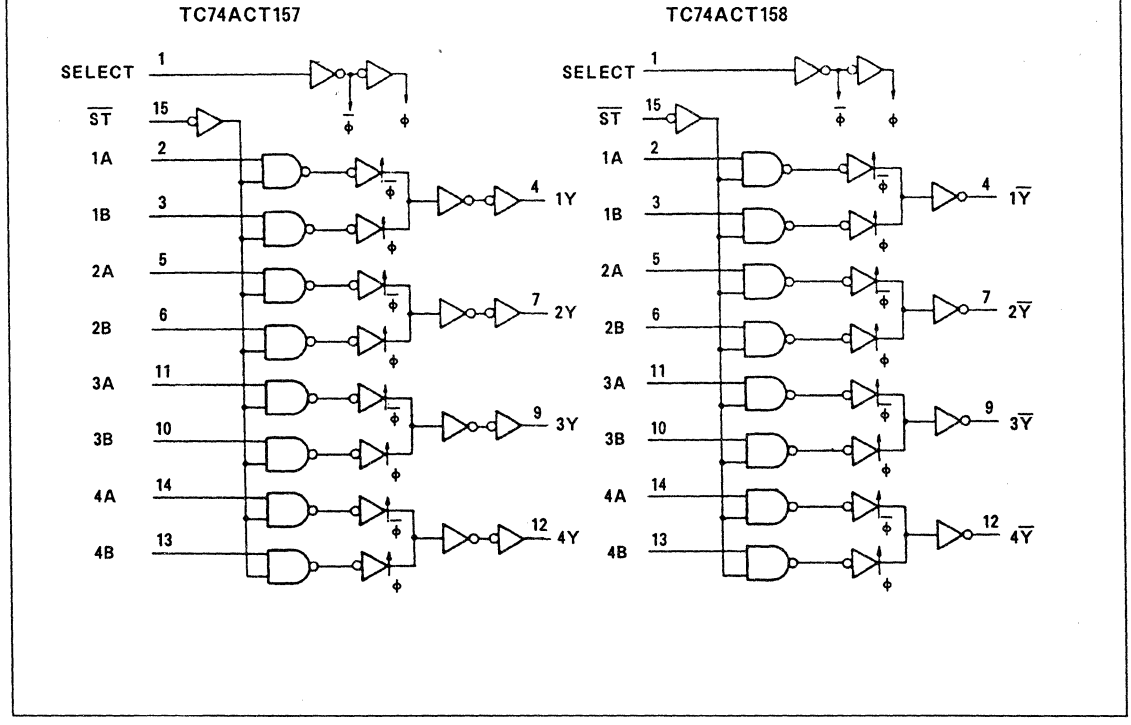
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* 1 This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B–Y) *	t_{pLH} t_{pHL}		5.0±0.5	—	5.5	8.0	1.0	9.1	ns
Propagation Delay Time (A, B–$\overline{Y}$) **	t_{pLH} t_{pHL}		5.0±0.5	—	5.8	8.6	1.0	9.8	
Propagation Delay Time (SELECT–Y, $\overline{Y}$) *	t_{pLH} t_{pHL}		5.0±0.5	—	6.9	11.4	1.0	13.0	
Propagation Delay Time (SELECT–Y, $\overline{Y}$) **	t_{pLH} t_{pHL}		5.0±0.5	—	7.4	11.9	1.0	13.5	
Propagation Delay Time ($\overline{ST}$–Y, $\overline{Y}$) *	t_{pLH} t_{pHL}		5.0±0.5	—	6.8	10.8	1.0	12.3	
Propagation Delay Time ($\overline{ST}$–$\overline{Y}$) **	t_{pLH} t_{pHL}		5.0±0.5	—	7.2	11.3	1.0	12.8	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74ACT157		—	50	—	—	—	
		TC74ACT158		—	51	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

(2) * for TC74ACT157 only
** for TC74ACT158 only

TC74AC160P/F/FN, TC74AC161P/F/FN, TC74AC162P/F/FN, TC74AC163P/F/FN

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER
TC74AC160P/F/FN DECADE, ASYNCHRONOUS CLEAR
TC74AC161P/F/FN BINARY, ASYNCHRONOUS CLEAR
TC74AC162P/F/FN DECADE, SYNCHRONOUS CLEAR
TC74AC163P/F/FN BINARY, SYNCHRONOUS CLEAR

The TC74AC160, 161, 162 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The TC74AC160/162 are BCD decade counters and the TC74AC161/163 are 4 bit binary counters.

The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active when low.

Presetting of all four IC's is synchronous to the rising edge of CK.

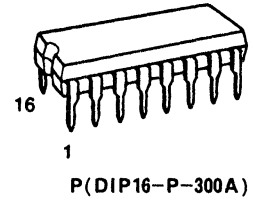
The clear function of the TC74AC162/163 is synchronous to CK, while the TC74AC160/161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

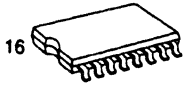
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

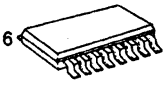
FEATURES:

- High Speed ..... f_{MAX}=170MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 160/161/162/163



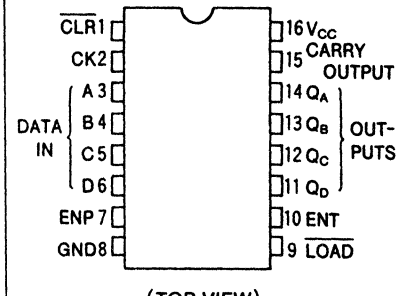
P(DIP16-P-300A)





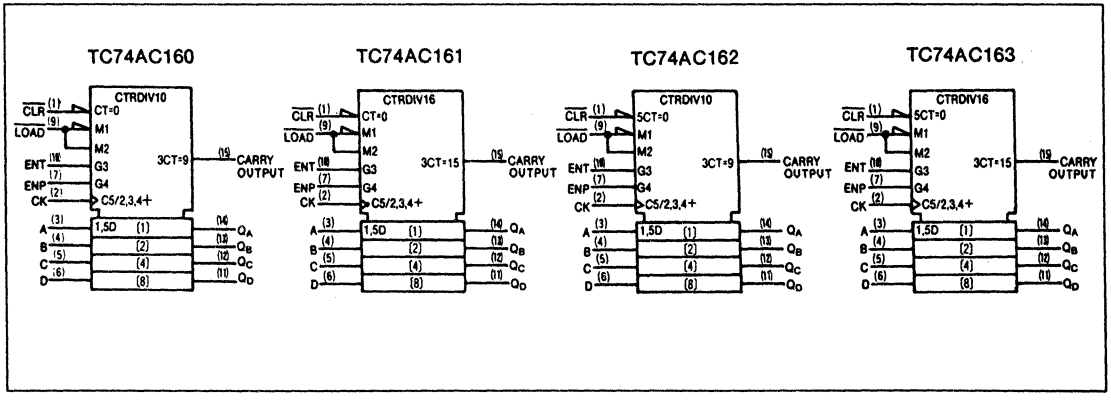
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±125	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	−	1.9 2.9 4.4	−	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	−	−	2.48 3.80 3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

TC74AC160/161 INPUTS					TC74AC162/163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

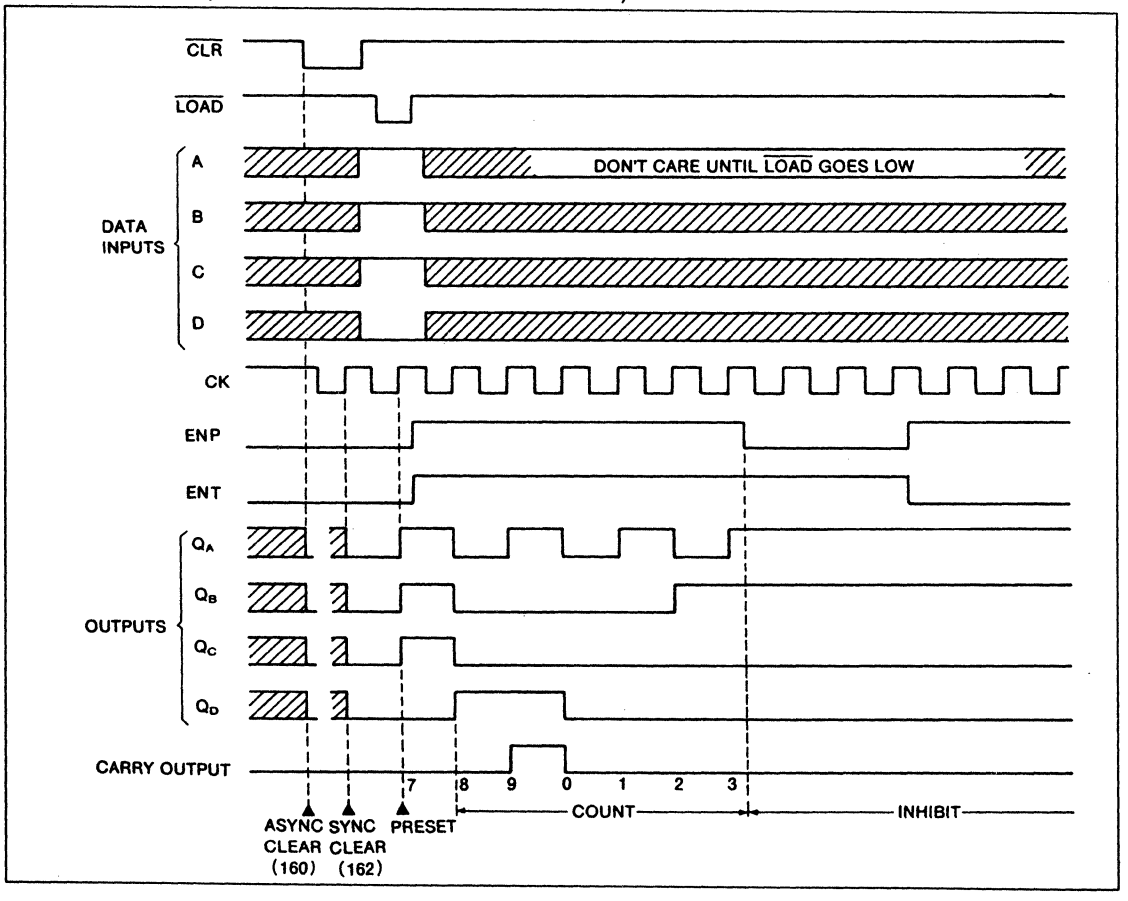
Note X : Don't care

A, B, C, D : Logic Level of Data Inputs

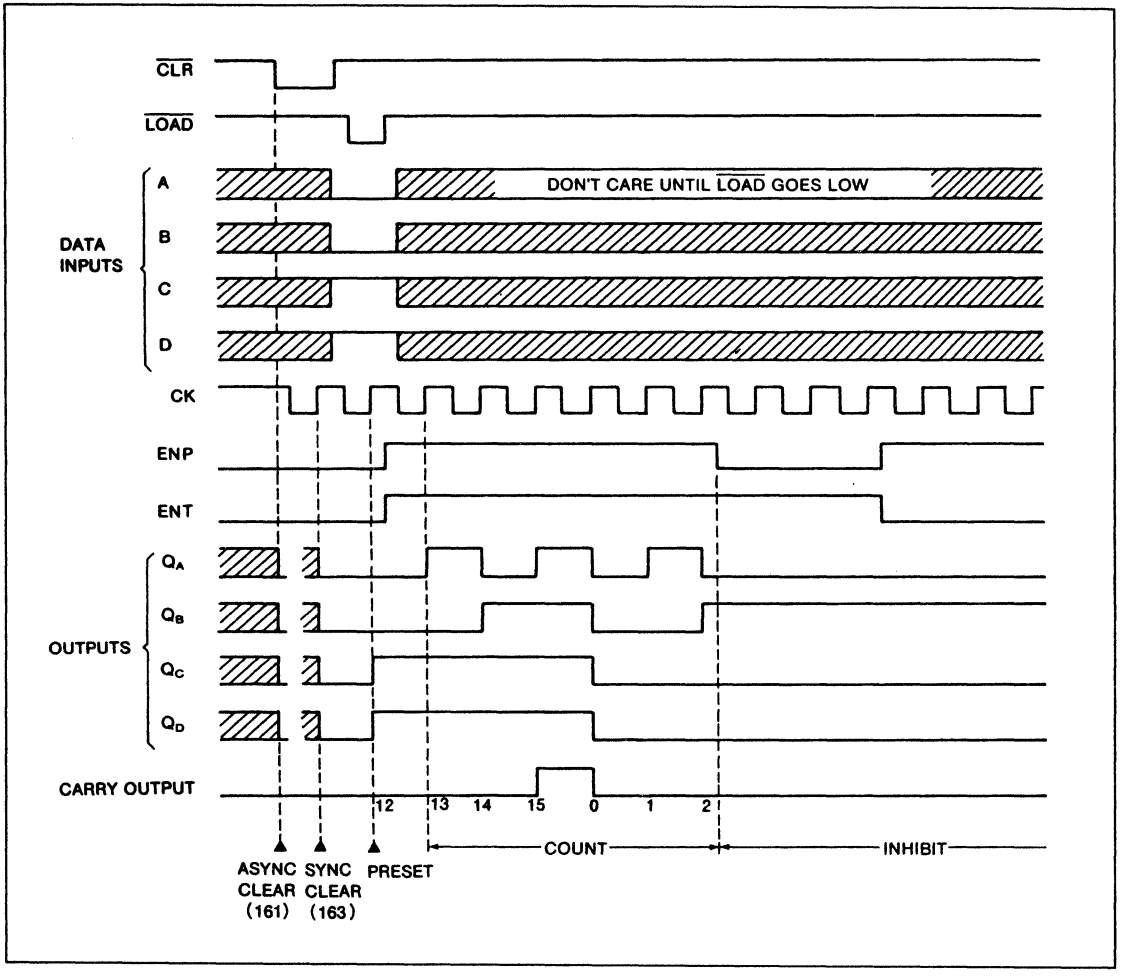
Carry : $CARRY = ENT \cdot Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot Q_D$ ·····(TC74AC160/162)

$CARRY = ENT \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$ ·····(TC74AC161/163)

TIMING CHART (TC74AC160/162: DECADE COUNTER)

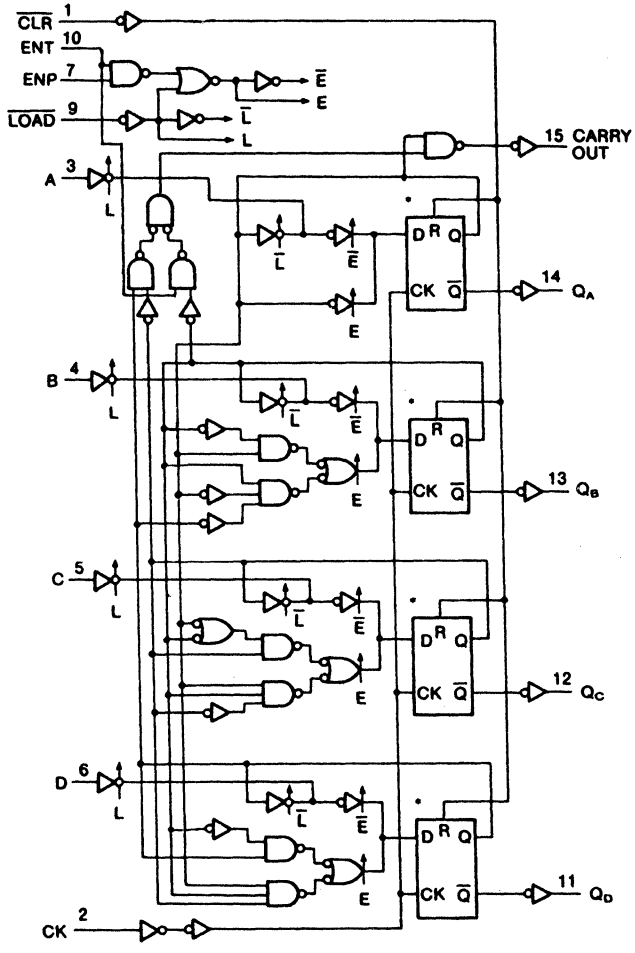


TIMING CHART (TC74AC161/163: BINARY COUNTER)



SYSTEM DIAGRAM

TC74AC160/TC74AC162



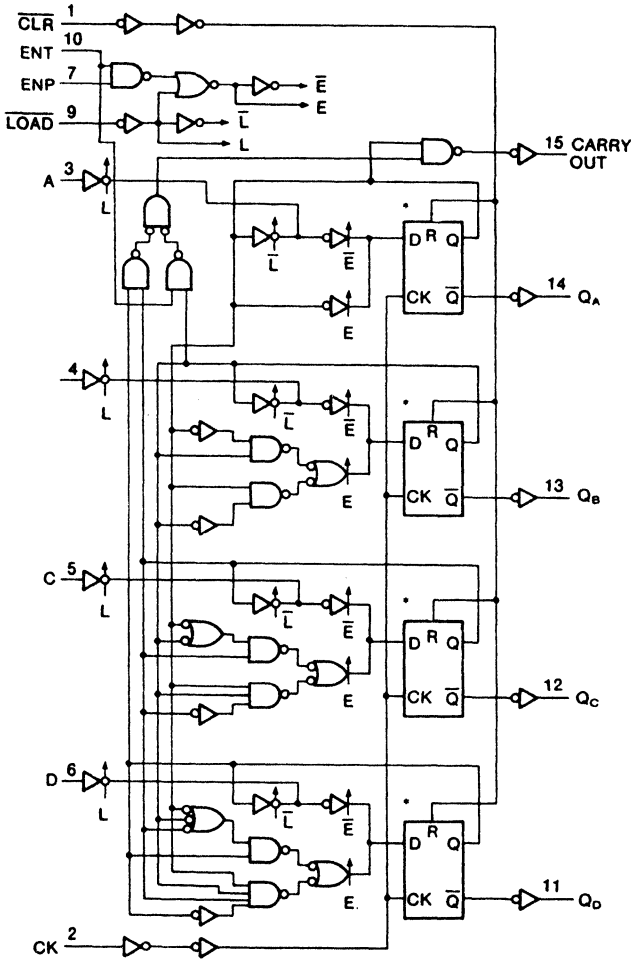
*TRUTH TABLE OF INTERNAL F/F

TC74AC160					TC74AC162				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↓	H	L	H
L	↓	L	L	H	L	↓	L	L	H
H	↓	L	H	L	H	↓	L	H	L
X	↑	L	NO CHANGE		L	↑	L	NO CHANGE	

X : Don't Care

SYSTEM DIAGRAM

TC74AC161/TC74AC163



*TRUTH TABLE OF INTERNAL F/F

TC74AC161					TC74AC163				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	H	L	H	X	↓	H	L	H
L	↓	L	L	H	L	↓	L	L	H
H	↓	L	H	L	H	↓	L	H	L
X	↑	L	NO CHANGE		L	↑	L	NO CHANGE	

X : Don't Care

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25℃			Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	
Minimum Set−up Time ($\overline{LOAD}$, ENP, ENT)	t_s		3.3±0.3 5.0±0.5	− −	11.0 7.0	13.0 7.0	
Minimum Set−up Time (A, B, C, D)	t_s		3.3±0.3 5.0±0.5	− −	8.0 4.0	8.0 4.0	
Minimum Set−up Time ($\overline{CLR}$)**	t_s		3.3±0.3 5.0±0.5	− −	6.0 4.0	6.0 4.0	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}		3.3±0.3 5.0±0.5	− −	6.0 4.0	6.0 4.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25℃				Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	8.8 6.5	15.8 9.6	1.0 1.0	18.0 11.0	ns
Propagation Delay Time (CK−CARRY, Count Mode)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	10.4 8.1	18.4 11.8	1.0 1.0	21.0 13.5	
Propagation Delay Time (CK−CARRY, Preset MODE)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	12.9 9.1	22.4 13.2	1.0 1.0	25.5 15.0	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	7.5 5.8	13.2 8.3	1.0 1.0	15.0 9.5	
Propagation Delay Time ($\overline{CLR}$−Q)*	t_{pHL}		3.3±0.3 5.0±0.5	− −	10.6 7.7	18.4 11.4	1.0 1.0	21.0 13.0	
Propagation Delay Time ($\overline{CLR}$−CARRY)*	t_{pHL}		3.3±0.3 5.0±0.5	− −	12.0 8.6	21.0 12.7	1.0 1.0	24.0 14.5	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	50 90	110 140	− −	50 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	85	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

In case of TC74AC160/162:

$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{CO}}{10} \right)$$

In case of TC74AC161/163:

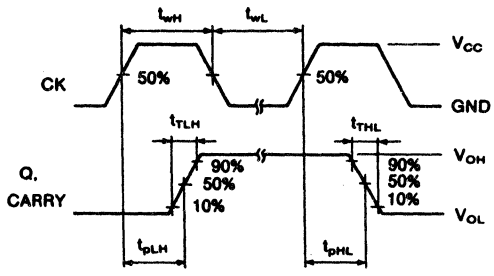
$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

$C_{QA} \sim C_{QD}$ and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CK.

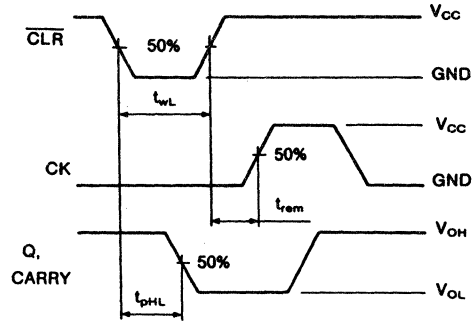
(2) * for TC74AC160/161 only
** for TC74AC162/163 only

SWITCHING CHARACTERISTICS TEST WAVEFORM

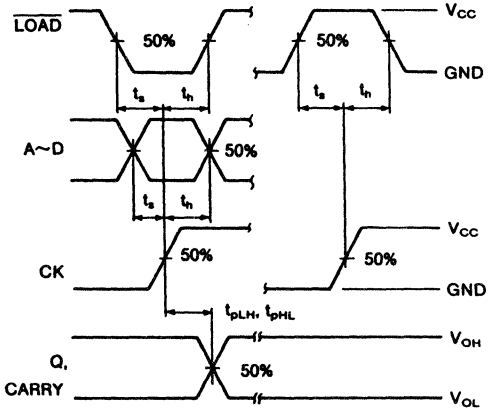
COUNT MODE (Fig. 1)



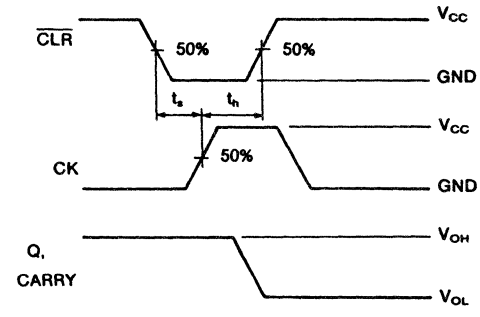
CLEAR MODE (TC74AC160/161) (Fig. 4)



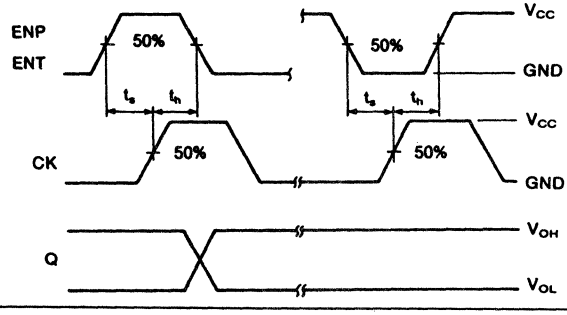
PRESET MODE (Fig. 2)



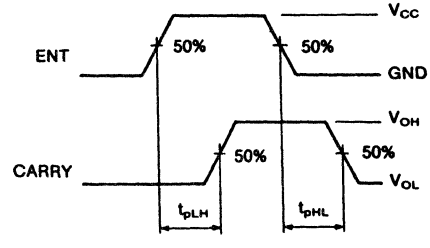
CLEAR MODE (TC74AC162/163) (Fig. 5)



COUNT ENABLE MODE (Fig. 3)

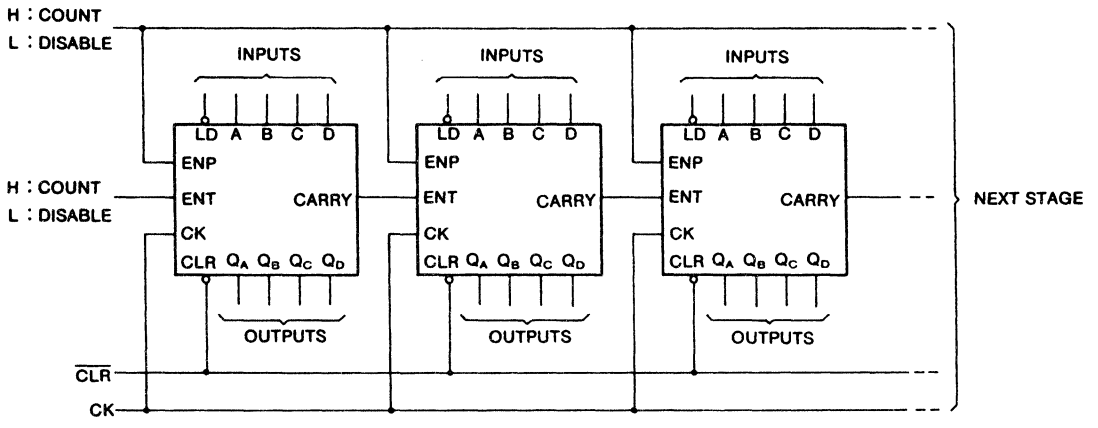


CASCADE MODE (Fix Maximum Count) (Fig. 6)



TYPICAL APPLICATION

PARALLEL CARRY N-BIT COUNTER



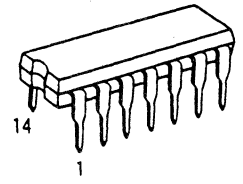
8-BIT SHIFT REGISTER(S-IN,P-OUT)

The TC74AC164 is an advanced high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

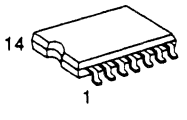
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

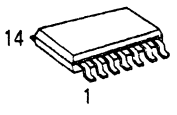
It consists of a serial-in,parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{CLEAR}$ input.Two serial data inputs(A,B)are provided so that one may be used as a data enable.

All inputs are equipped with protection circuits against static discharge or trasient excess voltage.



P(DIP14-P-300)



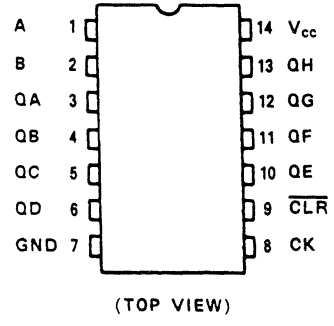


F(SOP14-P-300) FN(SOL14-P-150)

FEATURES:

- High Speed ..... f_{MAX}=170MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 164

PIN ASSIGNMENT



(TOP VIEW)

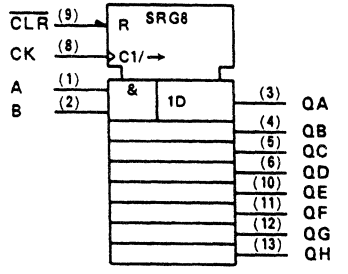
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CK	SERIAL IN		QA	QB	···	QH
		A	B				
L	X	X	X	L	L	···	L
H	⌐	X	X	NO CHANGE			
H	⌐‾	L	X	L	QAn	···	QGn
H	⌐‾	X	L	L	QAn	···	QGn
H	⌐‾	H	H	H	QAn	···	QGn

X: Don't Care

QAn~QGn: The level of QA~QG, respectively,before the most recent positive edge of the clock.

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

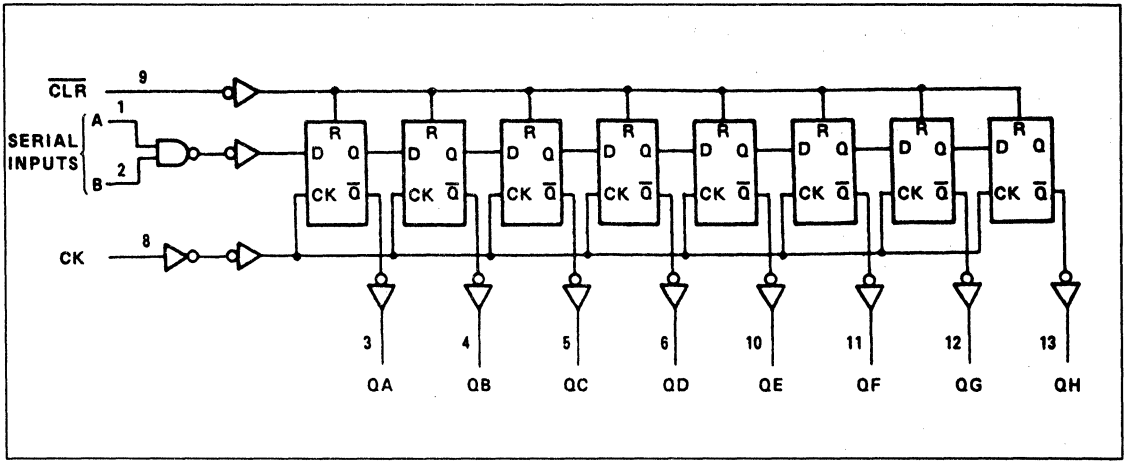
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

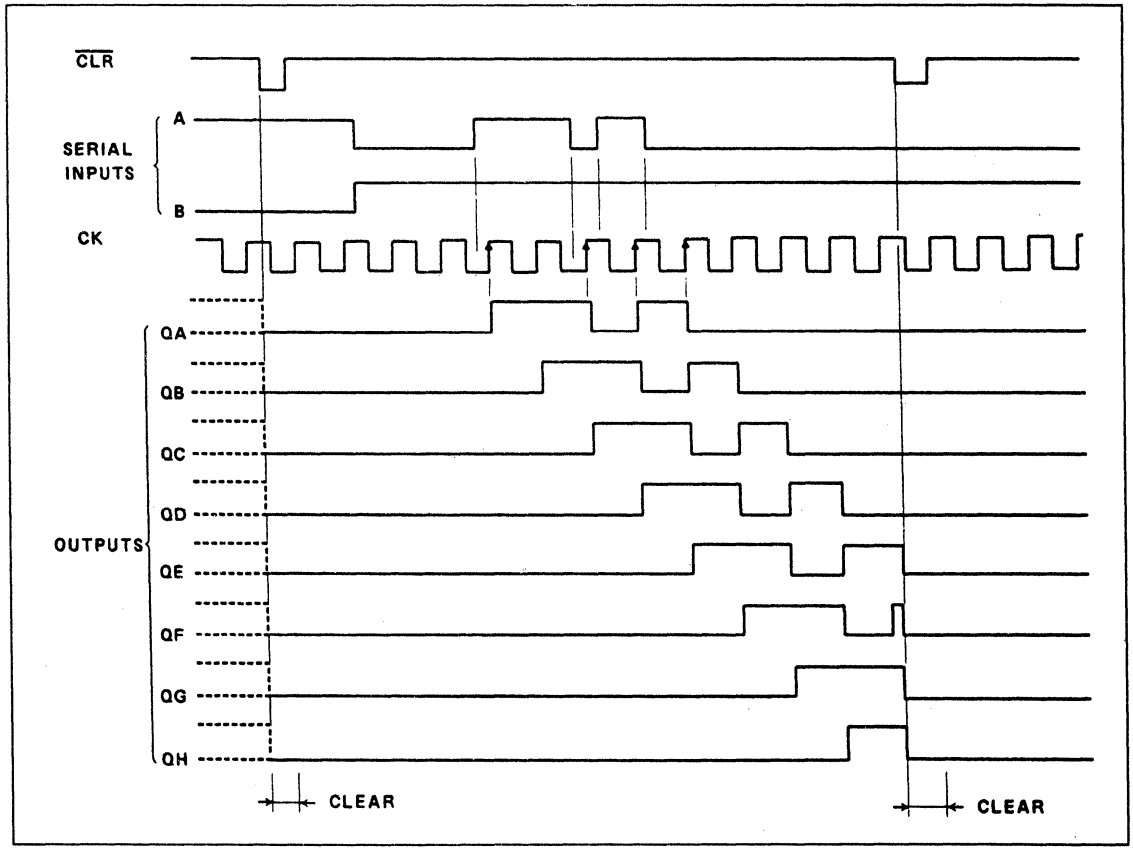
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING CHART



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$		3.3±0.3	−	9.0	10.0	ns
	$t_{W(H)}$		5.0±0.5	−	5.0	6.0	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	4.0	4.0	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3±0.3	−	8.5	8.5	
			5.0±0.5	−	5.0	5.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF, R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (CK−Q)	t_{pLH}		3.3±0.3	−	9.6	16.3	1.0	18.6	ns
	t_{pHL}		5.0±0.5	−	6.6	9.8	1.0	11.2	
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		3.3±0.3	−	9.7	16.0	1.0	18.0	
			5.0±0.5	−	7.6	11.5	1.0	13.1	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	45	100	−	45	−	MHz
			5.0±0.5	80	150	−	80	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	110	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

8-BIT SHIFT REGISTER (P-IN,S-OUT)

The TC74AC166 is an advanced high speed CMOS 8 BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with sillicon gate and duble-layer metal wiring C^2MOS technology.

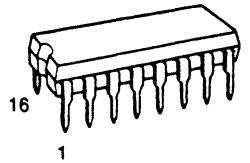
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

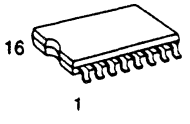
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

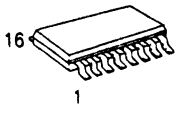
FEATURES:

- High Speed ····· f_{MAX}=170MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74HC166



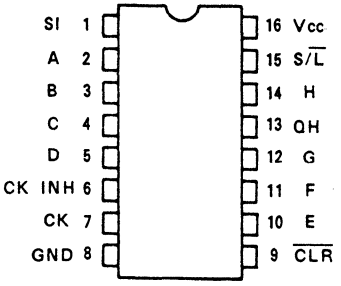
P(DIP16-P-300A)





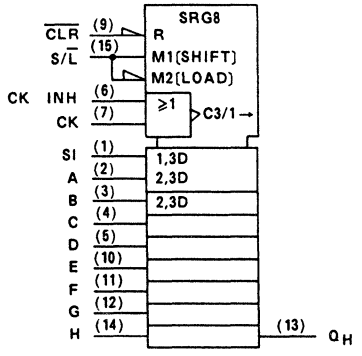
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC} =3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Input Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Input Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

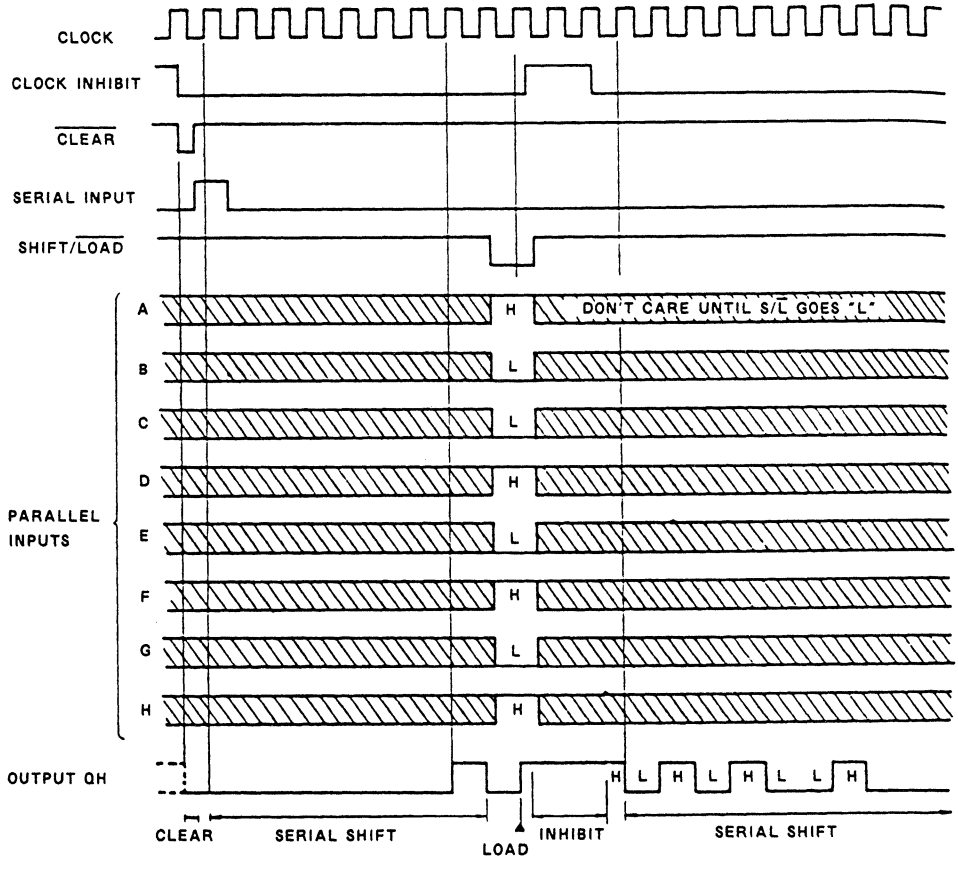
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
$\overline{\text{CLEAR}}$	SHIFT/$\overline{\text{LOAD}}$	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A·····H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↑	X	X	No change	
H	L	L	↓	X	a ····· h	a b	h
H	H	L	↓	H	X	H QAn	QGn
H	H	L	↓	L	X	L QAn	QGn
H	X	H	X	X	X	No change	

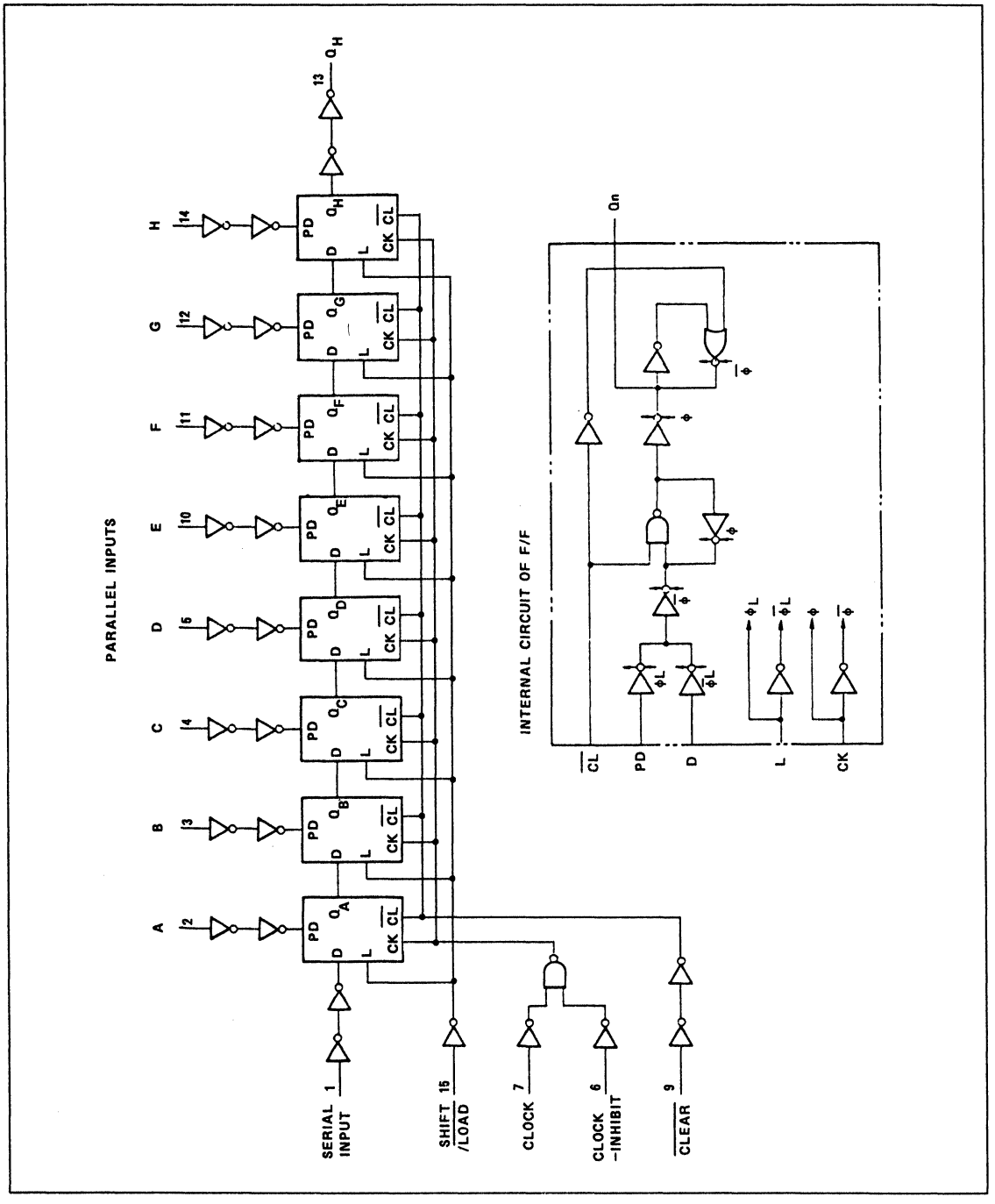
X : Don't care

a ····· h : The level of steady state input voltage at inputs A through H respectively

TIMING CHART



SYSTEM DIAGRAM



TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃		Ta=−40∼85℃	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	8.0 5.0	8.0 5.0	
Minimum Set-up Time (SI,PI)	t_s		3.3±0.3 5.0±0.5	− −	8.0 4.0	8.0 4.0	
Minimum Set-up Time (S/$\overline{L}$)	t_s		3.3±0.3 5.0±0.5	− −	7.0 4.0	7.0 4.0	
Minimum Hold Time (SI,PI)	t_h		3.3±0.3 5.0±0.5	− −	0.5 0.5	0.5 0.5	
Minimum Hold Time (S/L)	t_h		3.3±0.3 5.0±0.5	− −	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3±0.3 5.0±0.5	− −	4.0 1.5	4.0 1.5	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF, R_L = 500\Omega$, Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃			Ta=−40∼85℃		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−QH)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	9.4 6.6	16.1 10.0	1.0 1.0	18.3 11.4	ns
Propagation Delay Time ($\overline{CLR}$−QH)	t_{pHL}		3.3±0.3 5.0±0.5	− −	9.2 6.4	15.2 9.6	1.0 1.0	17.4 10.9	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	55 90	105 150	− −	55 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			−	67	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculanted from the operating current consumption without load.

Averating operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74AC174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

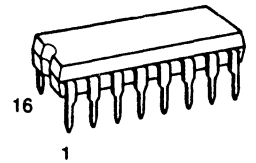
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLR}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.

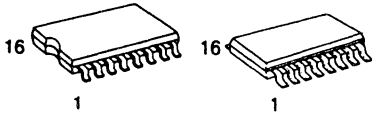
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=180MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 174

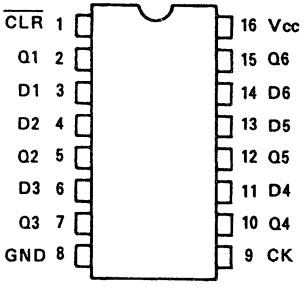


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



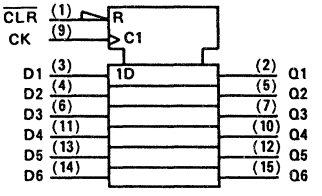
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↓	L	-
H	H	↓	H	-
H	X	↑	Qn	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

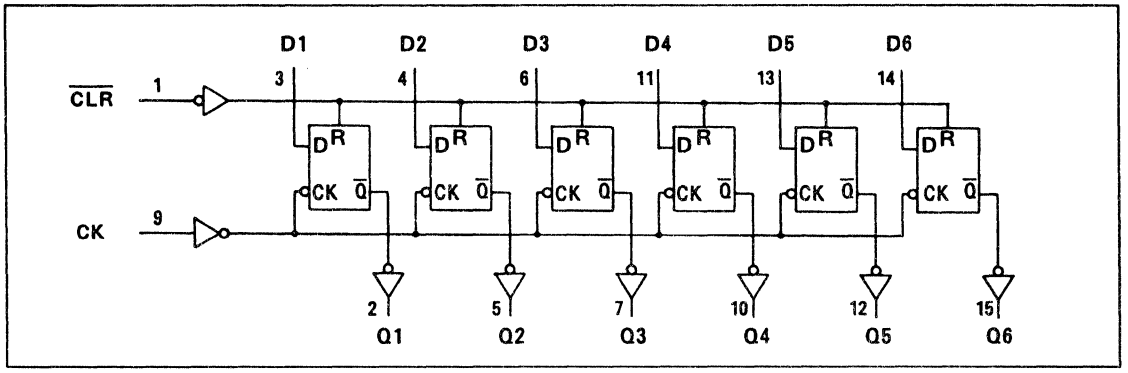
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40∼85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	
Minimum Set−up Time	t_s		3.3±0.3 5.0±0.5	− −	7.0 4.0	7.0 4.0	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	1.0 1.0	1.0 1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3±0.3 5.0±0.5	− −	6.0 3.5	6.0 3.5	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	8.5 6.7	14.4 9.6	1.0 1.0	16.6 11.0	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		3.3±0.3 5.0±0.5	− −	8.2 6.3	13.9 9.0	1.0 1.0	16.0 10.4	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	60 90	110 150	− −	60 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	74	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/6(\text{per F/F})$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD}(\text{total})=34+40 \cdot n$$

TC74ACT174P/F/FN

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74ACT174 is an advanced high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL, while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

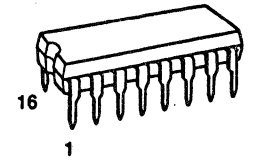
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLR}$ input is held low, the Q outputs are at a low logic level independent of the other inputs.

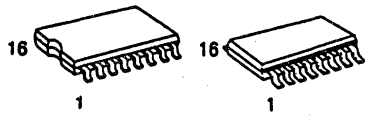
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=155MHz (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IL}=0.8V(Max.)
  V_{IH}=2V(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 174

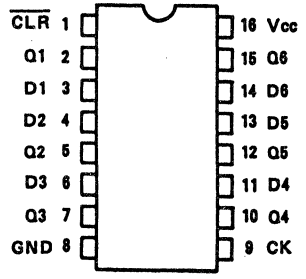


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



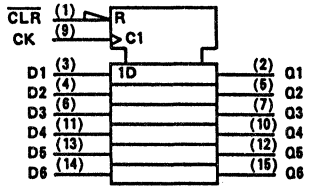
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	CLEAR
H	L	↑	L	–
H	H	↑	H	–
H	X	↓	Qn	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±150	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

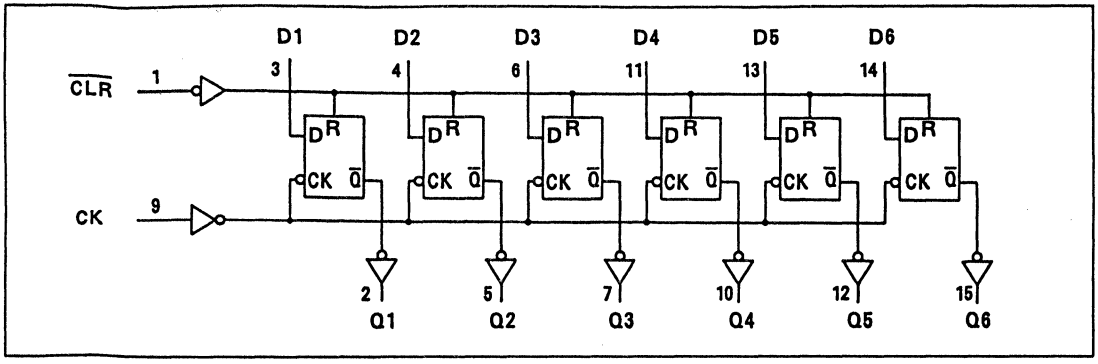
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{cc}	PER INPUT: V_{CC}=3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40∼85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
Minimum Set−up Time	t_s		5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		5.0±0.5	−	2.0	2.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		5.0±0.5	−	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		5.0±0.5	−	7.1	10.1	1.0	11.5	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		5.0±0.5	−	7.4	11.8	1.0	13.5	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	85	140	−	85	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	32	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/6(\text{per F/F})$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD}(\text{total})=20+12 \cdot n$$

NOTES

TC74AC175P/F/FN

QUAD D-TYPE FLIP FLOP WITH CLEAR

The TC74AC175 is an advanced high speed CMOS QUAD D-TYPE FLIP-FLOP fabricated with silicon gate and double-layer metal wiring CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These four flip-flops are controlled by a clock input (CLOCK) and a clear input ($\overline{CLEAR}$).

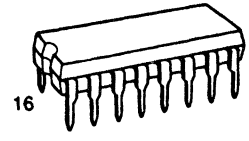
The information data applied to the D inputs (1D thru 4D) are transferred to the outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$) on the positive-going edge of the clock pulse.

Reset function is accomplished when the clear input is taken low, and all Q outputs are kept in low level regardless of other input conditions.

All input are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

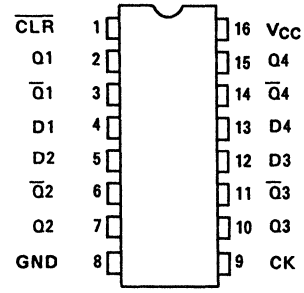
- High Speed ..... f_{MAX}=170MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~5.5V
- Pin and Function Compatible with 74F175



P(DIP16-P-300A)

F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



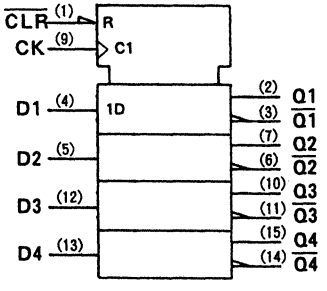
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLR}$	D	CK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↓	L	H	—
H	H	↓	H	L	—
H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

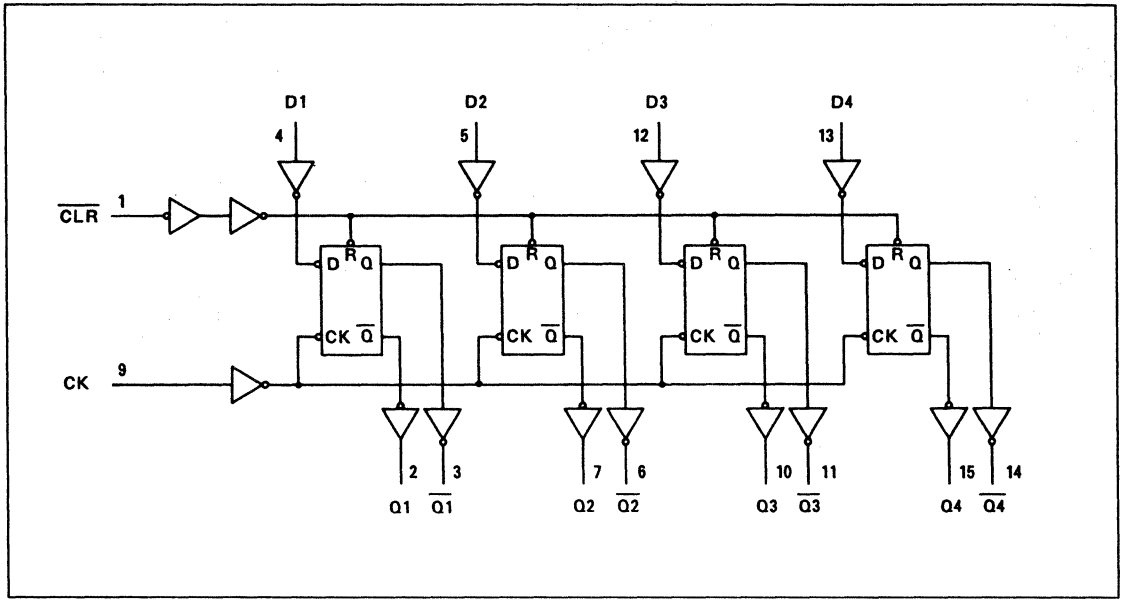
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	
Minimum Set-up Time	t_s		3.3±0.3 5.0±0.5	− −	12.0 6.5	12.0 6.5	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	0.0 0.0	0.0 0.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	8.2	13.9	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	7.8	13.3	1.0	15.3	
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	40	80	−	40	−	MHz
			5.0±0.5	80	150	−	80	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	85	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4(\text{per bit})$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(\text{total})=35+50 \cdot n$$

TC74ACT175P/F/FN

QUAD D-TYPE FLIP FLOP WITH CLEAR

The TC74ACT175 is an advanced high speed CMOS QUAD D-TYPE FLIP-FLOP fabricated with silicon gate and double-layer metal wiring CMOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

These four flip-flops are controlled by a clock input (CLOCK) and a clear input ($\overline{CLEAR}$).

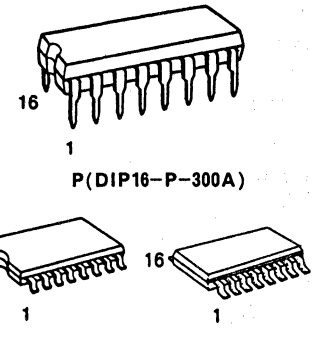
The data applied to the D inputs (1D thru 4D) are transferred to the outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$) on the positive-going edge of the clock pulse.

Reset is accomplished when the clear input is taken low, and all Q outputs are kept in low level regardless of other input conditions.

All input are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

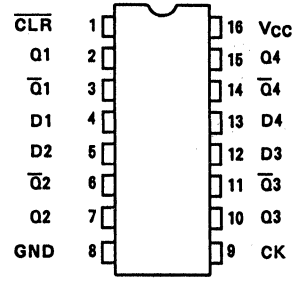
- High Speed ..... f_{MAX}=160MHz (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IL}=0.8V(Max.)
  V_{IH}=2V(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 175



P(DIP16-P-300A)

F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



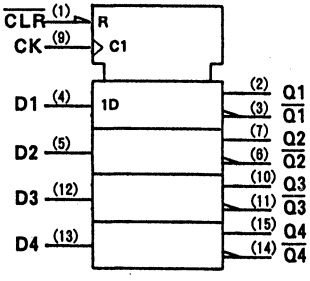
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLR}$	D	CK	Q	$\overline{Q}$	
L	X	X	L	H	CLEAR
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

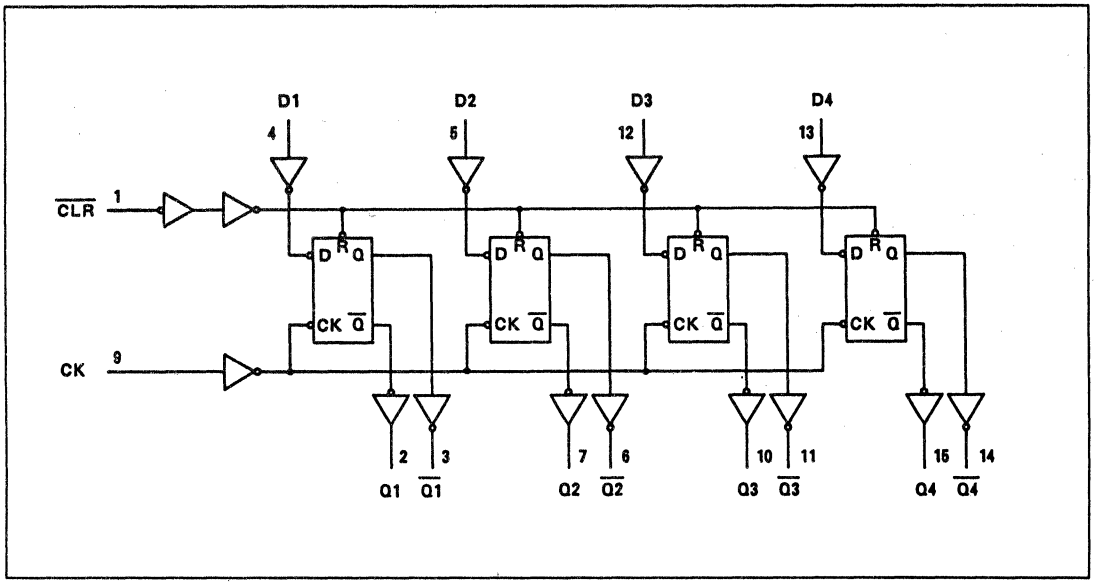
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{cc}	PER INPUT: V_{CC}=3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40∼85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
Minimum Set−up Time	t_s		5.0±0.5	−	4.0	4.0	
Minimum Hold Time	t_h		5.0±0.5	−	1.0	1.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		5.0±0.5	−	4.0	4.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.9	11.0	1.0	12.5	ns
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.5	10.4	1.0	11.8	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	80	145	−	80	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	46	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4(\text{per F/F})$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD}(\text{total})=25+21 \cdot n$$

TC74AC240P/F/FW, TC74AC241P/F/FW, TC74AC244P/F/FW

OCTAL BUS BUFFER

TC74AC240P/F/FW	INVERTED, 3-STATE OUTPUTS
TC74AC241P/F/FW	NON-INVERTED, 3-STATE OUTPUTS
TC74AC244P/F/FW	NON-INVERTED, 3-STATE OUTPUTS

The TC74AC240, 241 and 244 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

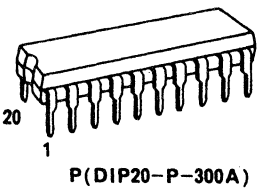
The 74AC240 is an inverting 3-state buffer having two active-low output enables. The TC74AC241 and TC74AC244 are non-inverting 3-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

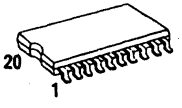
All inputs are equipped with protection circuits against static discharge or tansient excess voltage.

FEATURES:

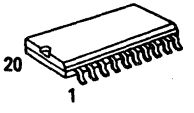
- High Speed ..... t_{pd}=4.0ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 240/241/244



P(DIP20-P-300A)



F(SOP20-P-300)



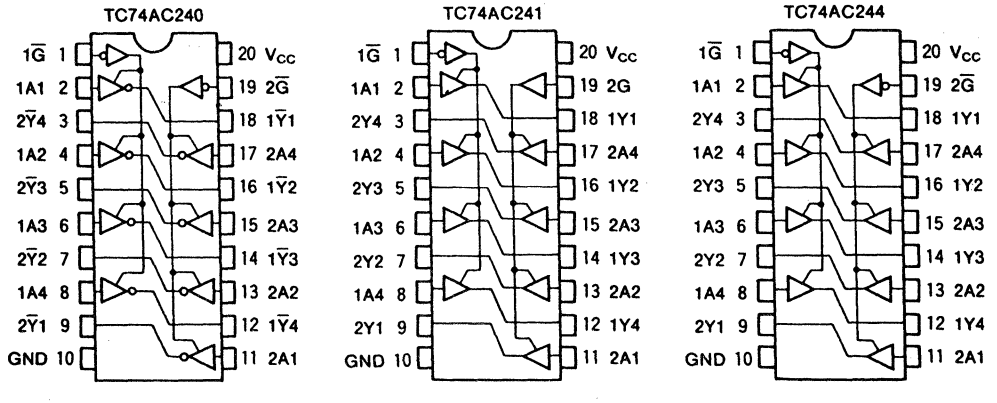
FW(SOL20-P-300)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : for TC74AC241 only
△△ : for TC74AC240 only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

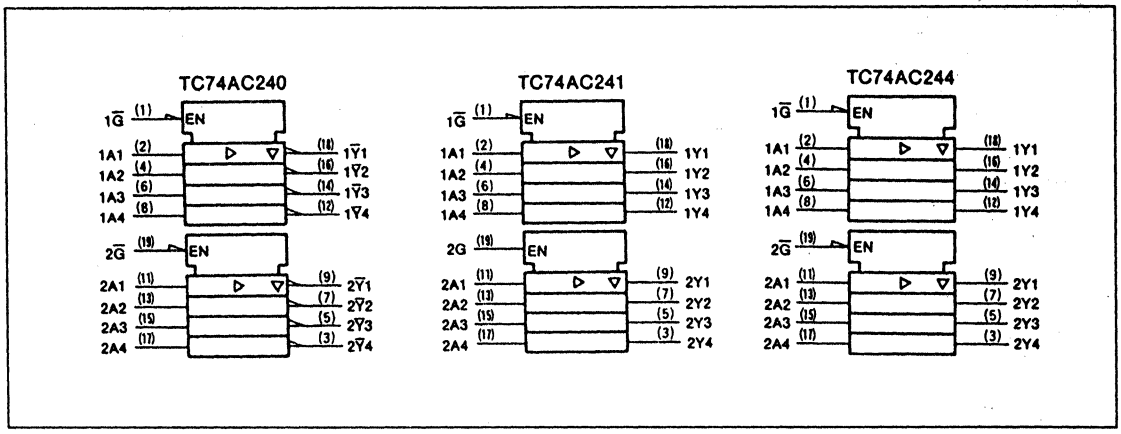
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time*	t_{pLH}		3.3±0.3	−	6.3	10.5	1.0	12.0	ns
	t_{pHL}		5.0±0.5	−	4.8	7.0	1.0	8.0	
Propagation Delay Time**	t_{pLH}		3.3±0.3	−	7.0	11.4	1.0	13.0	
	t_{pHL}		5.0±0.5	−	5.2	7.5	1.0	8.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	8.4	14.0	1.0	16.0	
	t_{pZH}		5.0±0.5	−	5.9	8.7	1.0	10.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	6.4	10.5	1.0	12.0	
	t_{pHZ}		5.0±0.5	−	5.5	7.9	1.0	9.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	30	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8 \text{(per bit)}$$

(2) * for TC74AC240 only
** for TC74AC241/244 only

OCTAL BUS BUFFER

TC74ACT240P/F/FW INVERTED, 3-STATE OUTPUTS
TC74ACT241P/F/FW NON-INVERTED, 3-STATE OUTPUTS
TC74ACT244P/F/FW NON-INVERTED, 3-STATE OUTPUTS

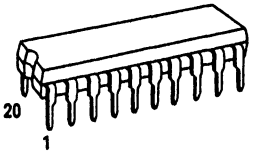
The TC74ACT240, 241 and 244 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

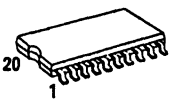
The 74ACT240 is an inverting 3-state buffer having two active-low output enables. The TC74ACT241 and TC74ACT244 are non-inverting 3-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

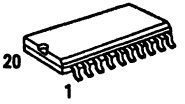
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300)



FW(SOL20-P-300)

FEATURES:

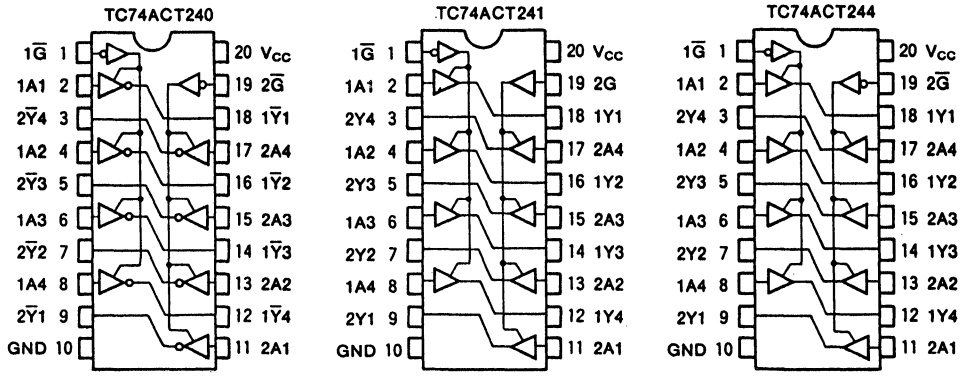
- High Speed ..... t_{pd}=5.0ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- Compatible with TTL outputs..... V_{IL} =0.8V (Max.)
  V_{IH} =2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F240/244

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : for TC74ACT241 only
△△ : for TC74ACT240 only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

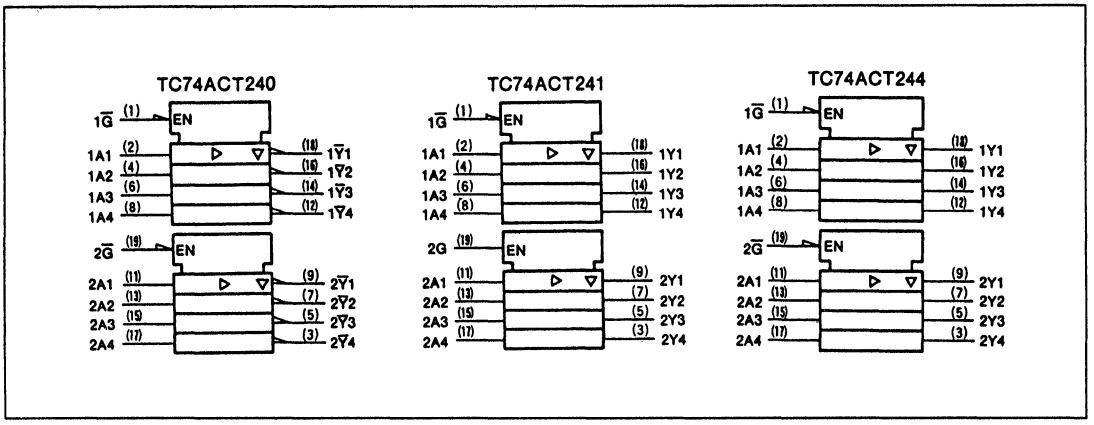
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{cc}	PER INPUT: V_{IN} = 3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		5.0±0.5	−	5.7	8.0	1.0	9.0	ns
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	6.0	9.0	1.0	10.5	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	5.9	8.5	1.0	10.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance*	C_{PD}(1)			−	25	−	−	−	
Power Dissipation Capacitance**	C_{PD}(1)			−	29	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) * for TC74ACT240 only
** for TC74ACT241/244

TC74AC245P/F/FW, TC74AC640P/F/FW, TC74AC643P/F/FW

OCTAL BUS TRANSCEIVER
TC74AC245P/F/FW 3-STATE, NON-INVERTING
TC74AC640P/F/FW 3-STATE, INVERTING
TC74AC643P/F/FW 3-STATE, INVERTING AND NON-INVERTING

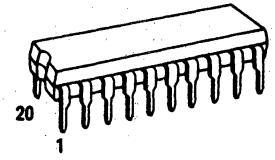
The TC74AC245, 640 and 643 are advanced high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

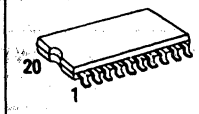
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

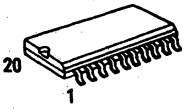
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300)



FW(SOL20-P-300)

FEATURES:

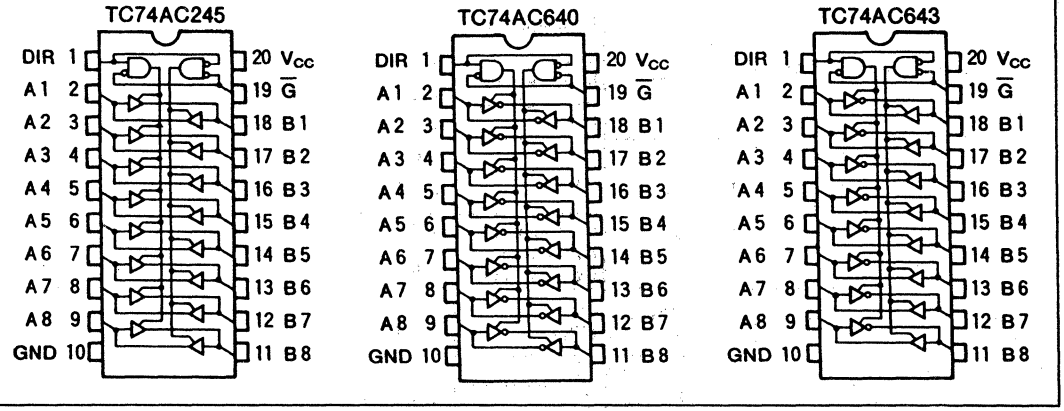
- High Speed ..... t_{pd}=3.9ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 245/640/643

APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

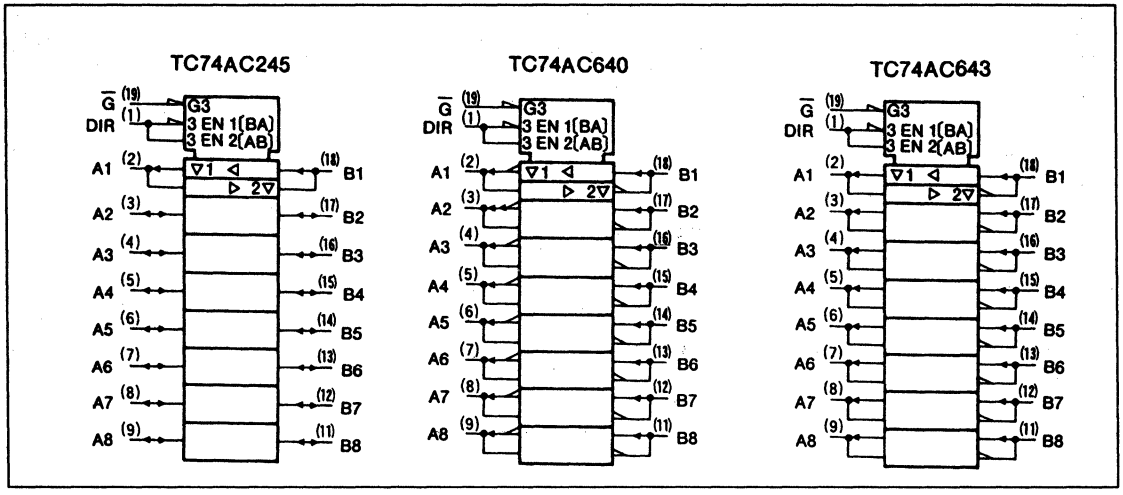
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	AC245	AC640	AC643
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High Impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time*	t_{pLH}		3.3±0.3	−	7.0	10.9	1.0	12.4	ns
	t_{pHL}		5.0±0.5	−	5.0	7.5	1.0	8.5	
Propagation Delay Time**	t_{pLH}		3.3±0.3	−	6.4	10.0	1.0	11.4	
	t_{pHL}		5.0±0.5	−	4.8	7.0	1.0	8.0	
Output Enable Time	t_{pZL}		3.3±0.3	−	9.3	15.3	1.0	17.4	
	t_{pZH}		5.0±0.5	−	7.1	10.5	1.0	12.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.1	11.4	1.0	13.0	
	t_{pHZ}		5.0±0.5	−	5.9	8.7	1.0	10.0	
Input Capacitance	C_{IN}	DIR. $\overline{G}$		−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74AC245		−	38	−	−	−	
		TC74AC640/643		−	36	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) * : for TC74AC245/643 only.

** : for TC74AC640 only

TC74ACT245P/F/FW, TC74ACT640P/F/FW

OCTAL BUS TRANSCEIVER
TC74ACT245P/F/FW 3-STATE, NON-INVERTING
TC74ACT640P/F/FW 3-STATE, INVERTING

The TC74ACT245 and 640 are advanced high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

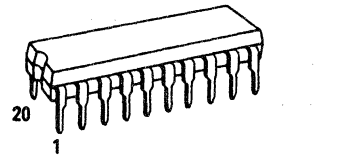
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

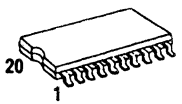
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

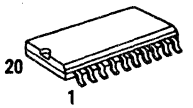
FEATURES:

- High Speed ..... t_{pd} = 4.7ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8 μA (Max.) at Ta = 25°C
- Compatible with TTL outputs..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F245/640



P(DIP20-P-300A)





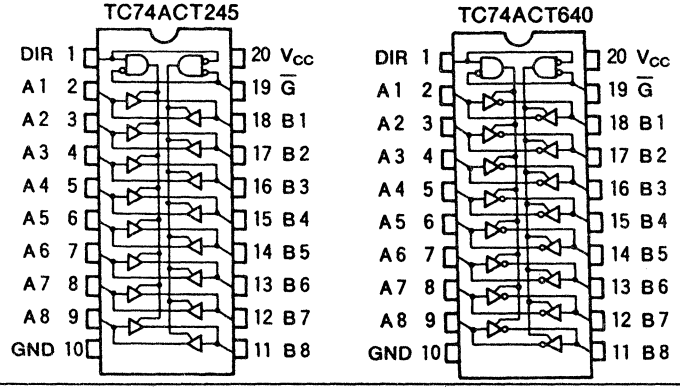
F(SOP20-P-300) FW(SOL20-P-300)

APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

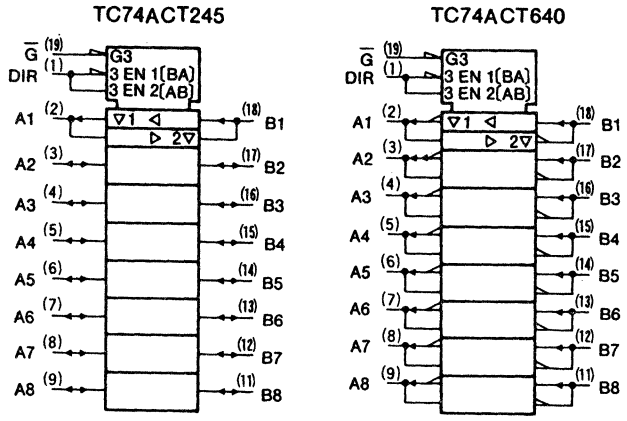
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA I_{OH}=−24mA I_{OH}=−75mA*	4.5 4.5 5.5	4.4 3.94 −	4.5 − −	− − −	4.4 3.80 3.85	− − −	V
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA I_{OL}=24mA I_{OL}=75mA*	4.5 4.5 5.5	− − −	0.0 − −	0.1 0.36 −	− − −	0.1 0.44 1.65	V
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT:V_{IN} = 3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{G}$	DIR	A BUS	B BUS	ACT245	ACT640
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$
H	X	High Impedance		Z	Z

X : "H" or "L"
Z : High Impedance

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time *	t_{pLH} t_{pHL}		5.0±0.5	−	5.0	8.0	1.0	9.0	ns
Propagation Delay Time **	t_{pLH} t_{pHL}		5.0±0.5	−	5.7	8.5	1.0	9.5	
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	7.3	12.3	1.0	14.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	6.3	9.7	1.0	11.0	
Input Capacitance	C_{IN}	DIR. $\overline{G}$		−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74ACT245		−	38	−	−	−	
		TC74ACT640		−	43	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

(2) * : for TC74ACT245 only.
** : for TC74ACT640 only

TC74AC257P/F/FN 2-CHANNEL MULTIPLEXER(3-STATE)
TC74AC258P/F/FN 2-CHANNEL MULTIPLEXER(3-STATE,INVERTING)

The TC74AC257 and TC74AC258 are advanced high speed CMOS MULTIPLEXERs fabricated with silicon gate and double-layer metal wiring C^2MOS technolgy.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

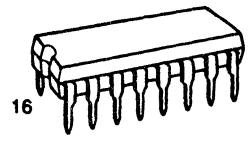
Each is composed of four independent 2-channel multiplexers with common SELECT and OUTPUT ENABLE($\overline{OE}$).

The TC74AC257 is a non-inverting multiplexer, while the TC74AC258 is inverting.

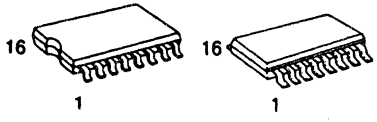
If $\overline{OE}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.

All inputs are equipped with protection citcuits against static discharge or transient excess voltage.



P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

FEATURES:

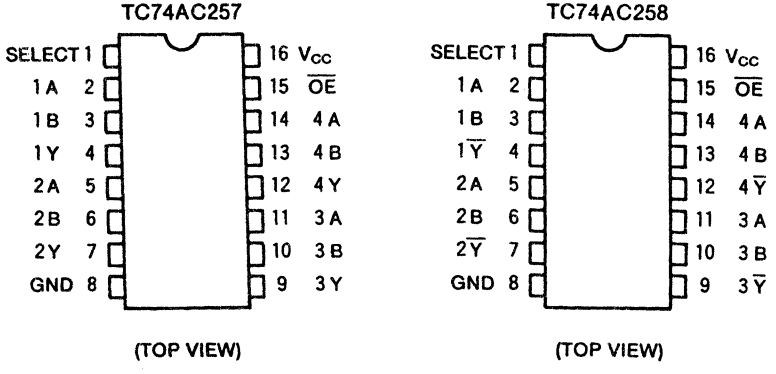
- High Speed ..... t_{pd}=3.6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8 μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 257/258

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y(257)	$\overline{Y}$(258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care
Z : High Impedance

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

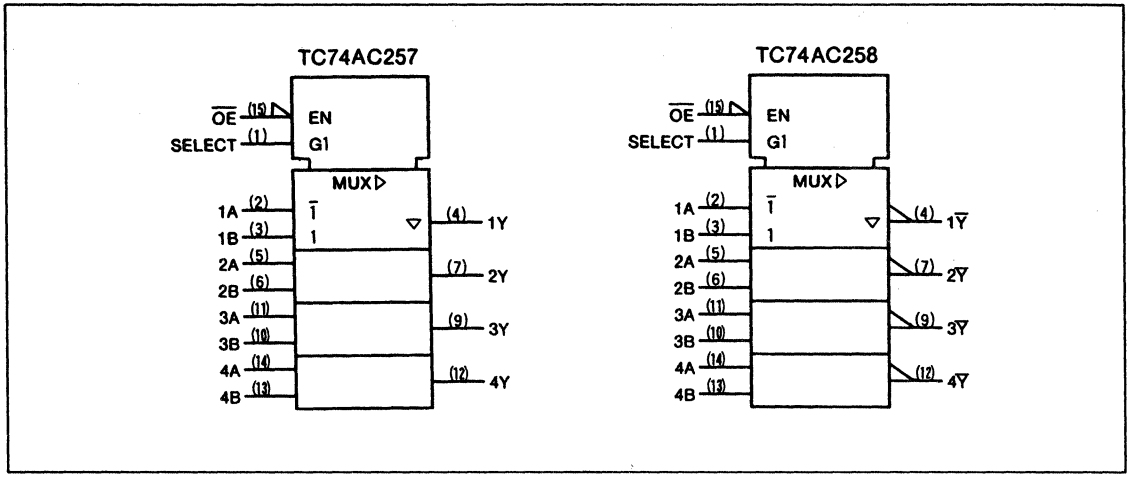
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

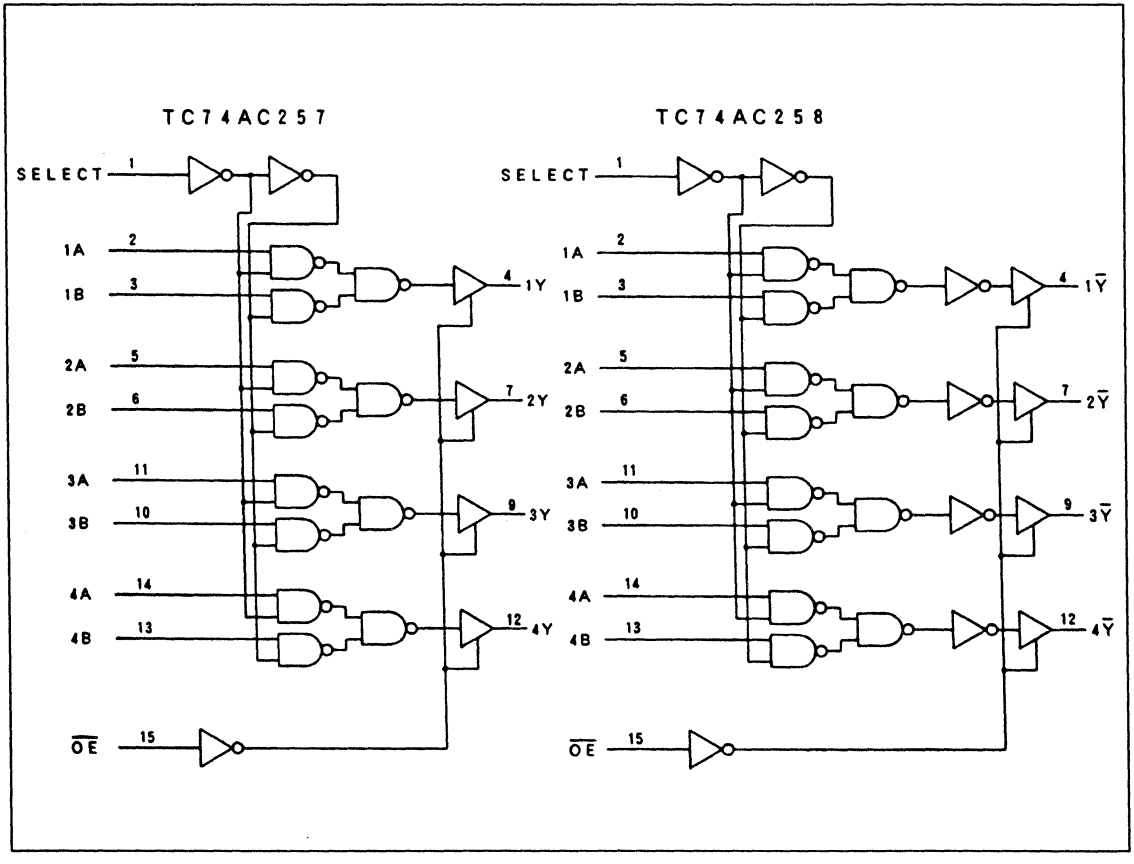
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B−Y, $\overline{Y}$)	t_{pLH}		3.3±0.3	−	7.0	14.3	1.0	16.3	ns
	t_{pHL}		5.0±0.5	−	4.7	7.5	1.0	8.5	
Propagation Delay Time (SELECT−Y, $\overline{Y}$)	t_{pLH}		3.3±0.3	−	8.6	17.2	1.0	19.6	
	t_{pHL}		5.0±0.5	−	5.5	9.1	1.0	10.4	
Output Enable Time	t_{pZL}		3.3±0.3	−	7.3	14.0	1.0	16.0	
	t_{pZH}		5.0±0.5	−	5.0	7.9	1.0	9.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	5.6	9.6	1.0	11.0	
	t_{pHZ}		5.0±0.5	−	5.1	7.9	1.0	9.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	28	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TC74ACT257P/F/FN 2-CHANNEL MULTIPLEXER(3-STATE)
TC74ACT258P/F/FN 2-CHANNEL MULTIPLEXER(3-STATE,INVERTING)

The TC74ACT257 and TC74ACT258 are advanced high speed CMOS MULTIPLEXERs fabricated with silicon gate and double-layer metal wiring C^2MOS technolgy.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

Each is composed of four independent 2-channel multiplexers with common SELECT and $\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$($\overline{\text{OE}}$).

The TC74ACT257 is a non- inverting multiplexer, while the TC74ACT258 is an inverting.

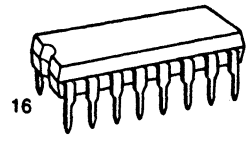
If $\overline{\text{OE}}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.

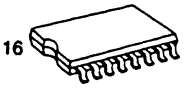
All inputs are equipped with protection citcuits against static discharge or transient excess voltage.

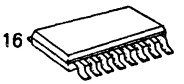
FEATURES:

- High Speed ..... t_{pd}= ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- Compatible with TTL outputs ..... V_{IL} =0.8V(Max.)
  V_{IH} =2.0V(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|$ = I_{OL}=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 257/258



P(DIP16-P-300A)





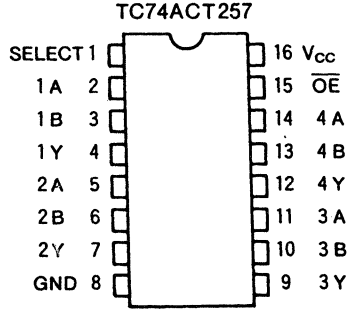
F(SOP16-P-300) FN(SOL16-P-150)

TRUTH TABLE

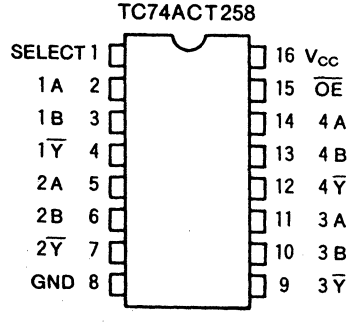
INPUTS				OUTPUTS	
$\overline{\text{OE}}$	SELECT	A	B	Y(257)	$\overline{\text{Y}}$(258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care
Z : High Impedance

PIN ASSIGNMENT



(TOP VIEW)



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

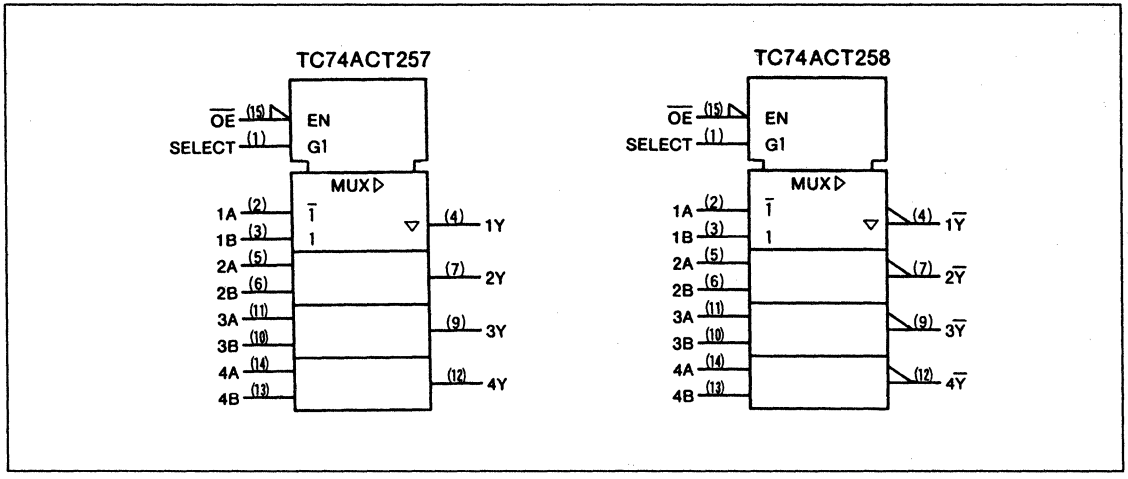
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

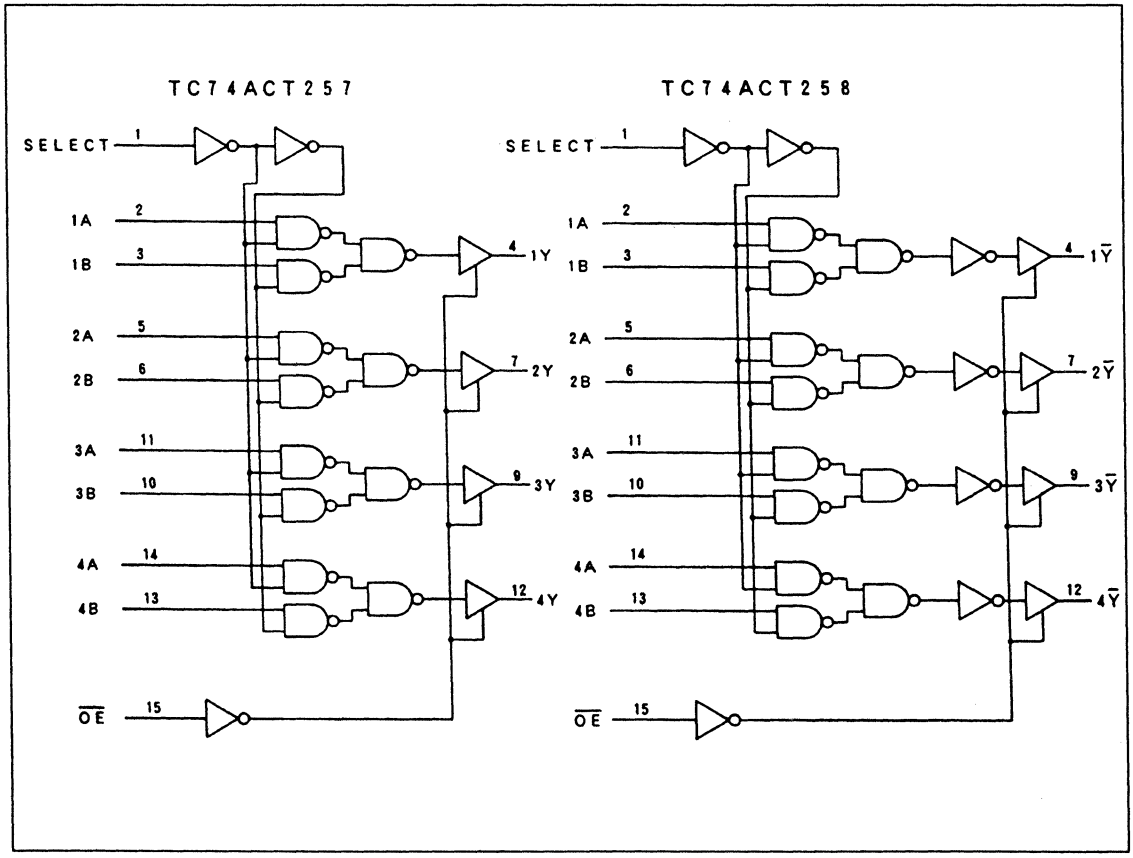
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (A, B−Y, $\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−			1.0		ns
Propagation Delay Time (SELECT−Y, $\overline{Y}$)	t_{pLH} t_{pHL}		5.0±0.5	−			1.0		ns
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−			1.0		ns
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−			1.0		ns
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	pF
Power Dissipation Capacitance	C_{PD}(1)			−		−	−	−	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

OCTAL D-TYPE FLIP FLOP WITH CLEAR

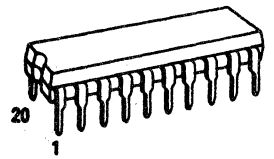
The TC74AC273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

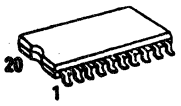
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

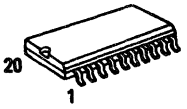
When the $\overline{CLR}$ input is held low, the Q outputs are at a low logic level independent of the other inputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



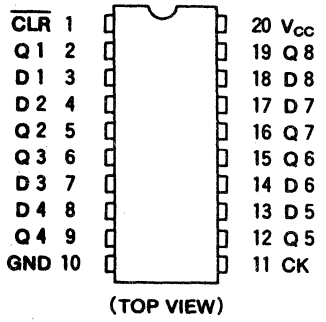


F(SOP20-P-300) FW(SOL20-P-300)

FEATURES:

- High Speed ····· f_{MAX}=170MHz (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 273

PIN ASSIGNMENT



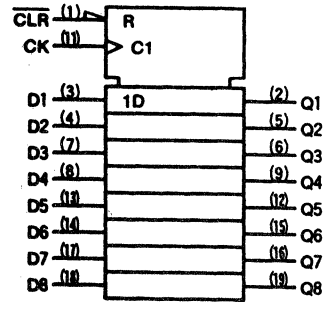
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↓	L	—
H	H	↓	H	—
H	X	↑	Q_n	No change

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

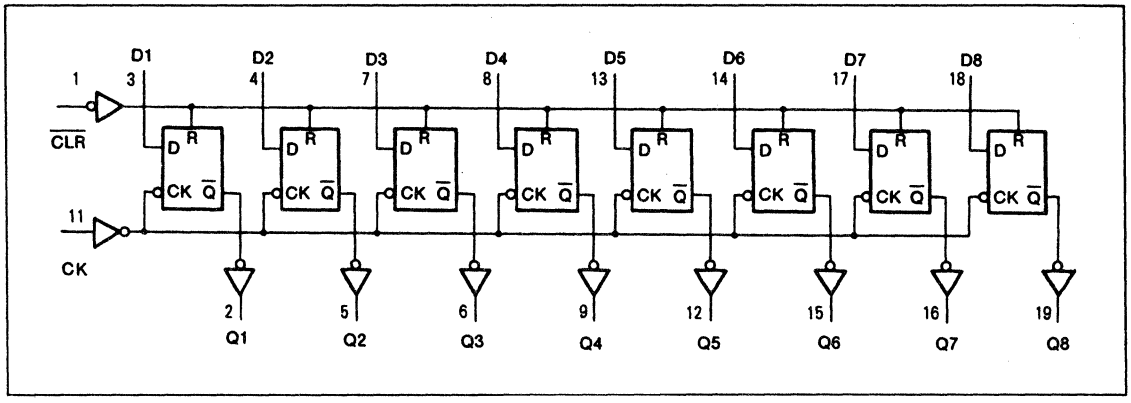
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		3.3±0.3 5.0±0.5	− −	8.0 5.0	8.0 5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.5 5.0	7.5 5.0	
Minimum Set−up Time	t_s		3.3±0.3 5.0±0.5	− −	8.5 4.5	8.5 4.5	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	0.0 0.0	0.0 0.0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		3.3±0.3 5.0±0.5	− −	7.0 3.5	7.0 3.5	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	9.0 6.5	15.8 9.6	1.0 1.0	18.0 11.0	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		3.3±0.3 5.0±0.5	− −	8.0 5.9	14.0 9.2	1.0 1.0	16.0 10.5	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	55 90	110 150	− −	55 90	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	40	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per F/F})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following eqution:

$$C_{PD}(\text{total})=29+11 \cdot n$$

OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74ACT273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

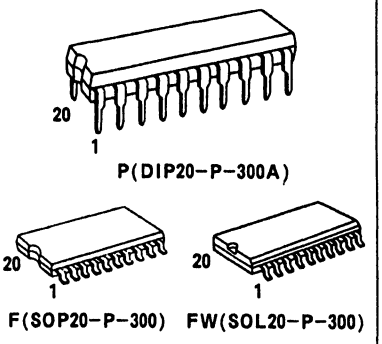
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLR}$ input is held low, the Q outputs are at a low logic level independent of the other inputs.

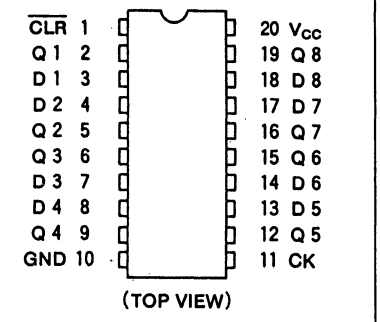
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=170MHz (typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8 μA(Max.) at Ta=25°C
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.)
  V_{IH}=2V(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 273



PIN ASSIGNMENT

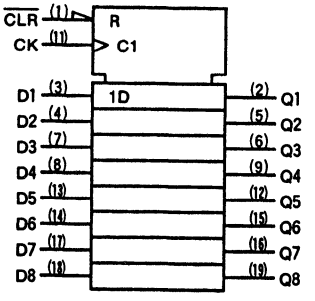


TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLR}$	D	CK	Q	
L	X	X	L	Clear
H	L	↓	L	—
H	H	↓	H	—
H	X	↑	Q_n	No change

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

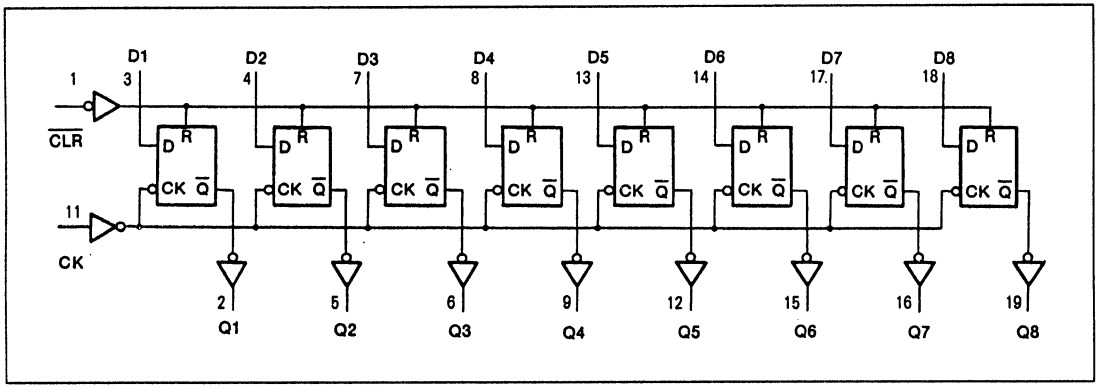
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	μA
	ΔI_{cc}	PER INPUT: V_{CC}=3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
Minimum Set−up Time	t_s		5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		5.0±0.5	−	1.5	1.5	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		5.0±0.5	−	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Propagation Delay Time (CK−Q)	t_{pLH} t_{pHL}		5.0±0.5	−	6.6	10.5	1.0	12.0	ns
Propagation Delay Time ($\overline{CLR}$−Q)	t_{pHL}		5.0±0.5	−	7.4	10.8	1.0	12.3	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	80	150	−	80	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	34	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per F/F})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following eqution:

$$C_{PD}\ (\text{total})=23+11 \cdot n$$

NOTES

TC74AC299P/F/FW 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
TC74AC323P/F/FW 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

The TC74AC299 and TC74AC323 are advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

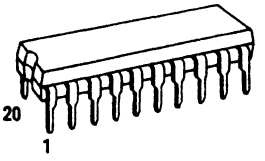
They have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enables ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. Clear function on the AC299 is asynchronous to CLOCK, while the AC323 is cleared synchronous to CLOCK.

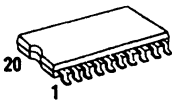
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

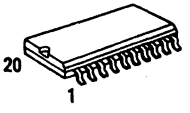
FEATURES:

- High Speed ····· f_{MAX} =150MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~5.5V
- Pin and Function Compatible with 74F299/323



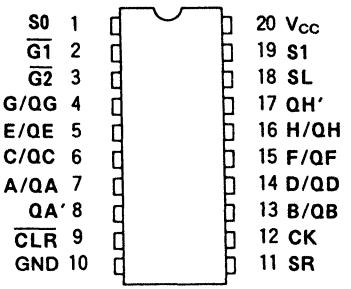
P(DIP20-P-300A)





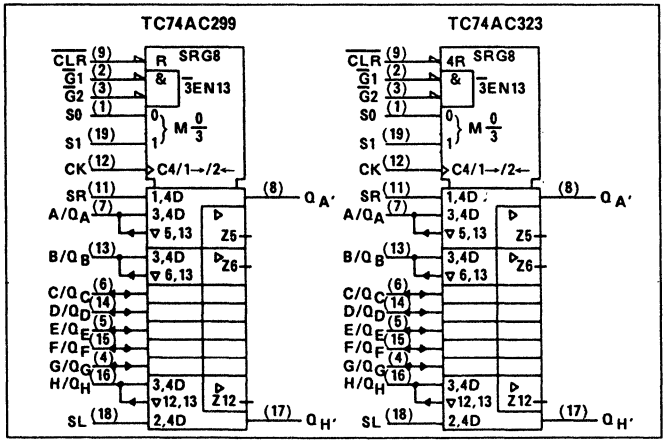
F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

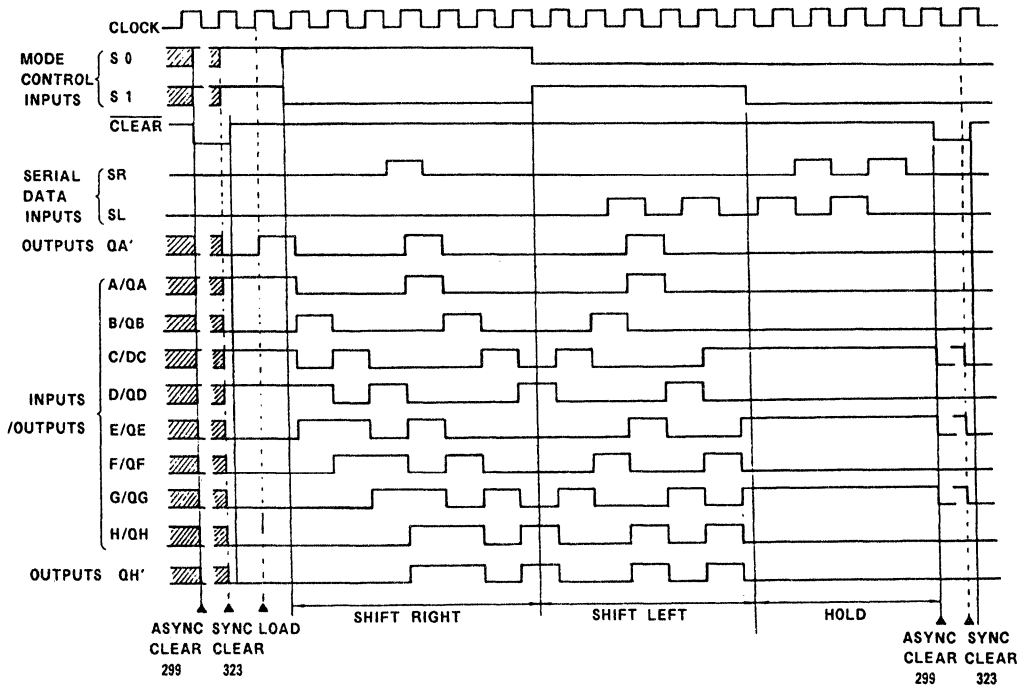
TRUTH TABLE

MODE	INPUTS									INPUTS/OUTPUTS		OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *	(299)	(323)	SL	SR				
CLEAR	L	H	H	X	X	X	↓	X	X	Z	Z	L	L
	L	L	X	L	L	X	↓	X	X	L	L	L	L
	L	X	L	L	L	X	↓	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓		X	H	H	QGn	H	QGn
	H	L	H	L	L	↓		X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓		H	X	QBn	H	QBn	H
	H	H	L	L	L	↓		L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↓		X	X	a	h	a	h

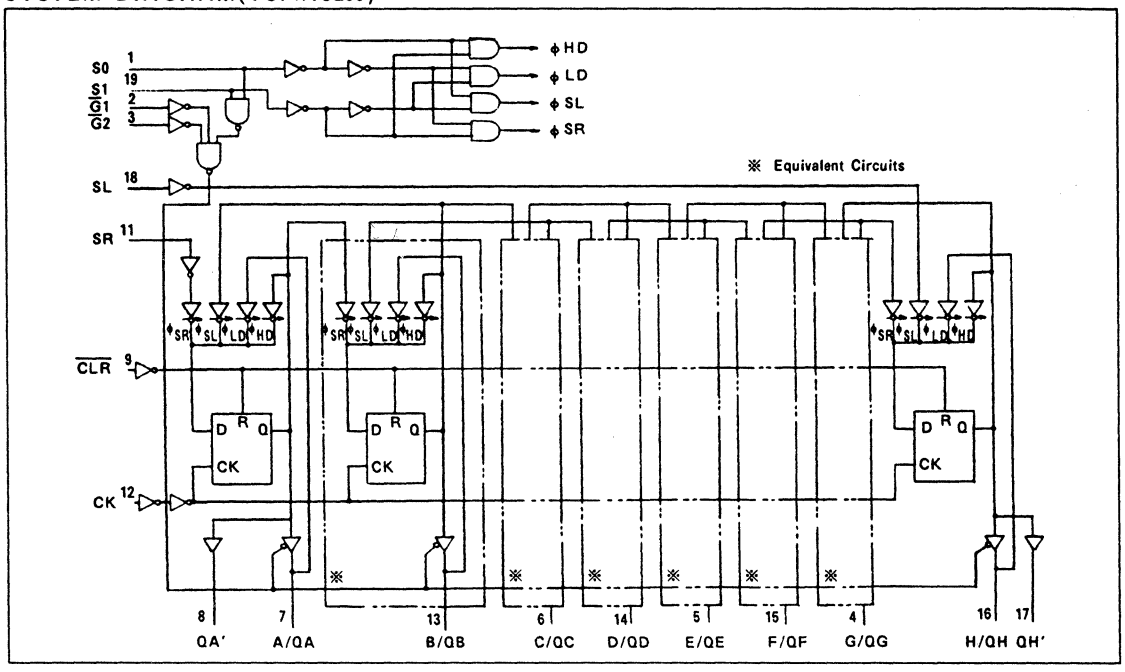
* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z : High Impedance
Qn0 : The level of An before the indicated steady-state input conditions were established.
Qnn : The level of Qn before the most recent active transition indicated by ↓ or ↑.
a,h : The level of the steady-state inputs A, H, respectively.
X : Don't care
:

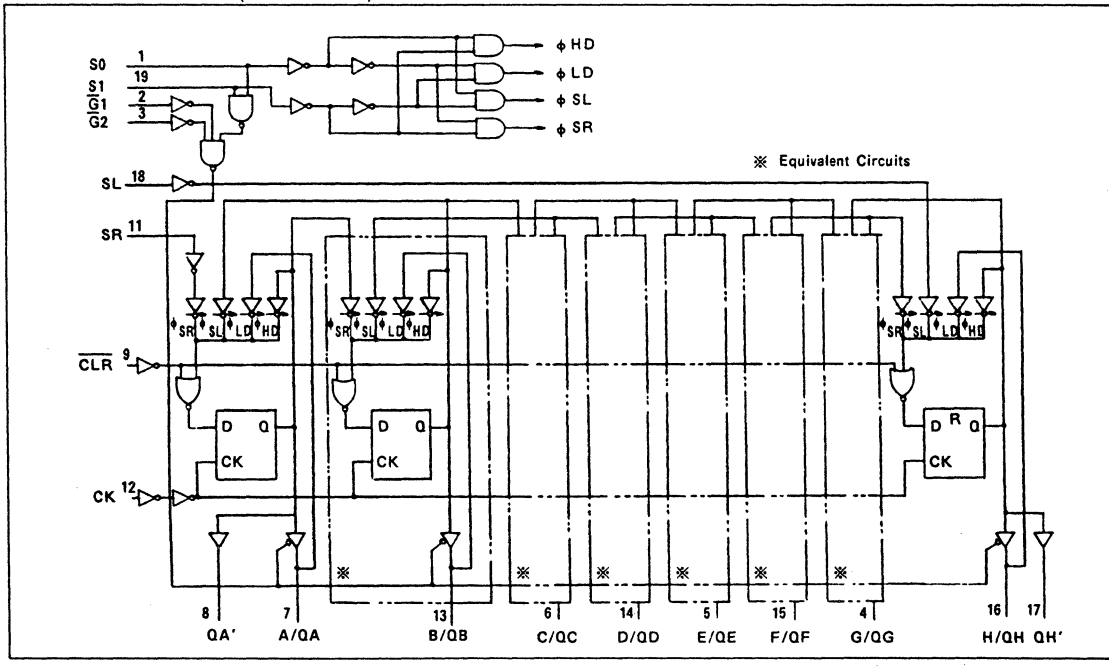
TIMING CHART



SYSTEM DIAGRAM(TC74AC299)



SYSTEM DIAGRAM(TC74AC323)



TIMING RECOMMENDED OPERATING CONDITIONS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ～85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$		3.3±0.3	−	8.0	8.0	ns
	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set−up Time (SL,SR,A～H)	t_s		3.3±0.3	−	6.0	6.0	
			5.0±0.5	−	4.0	4.0	
Minimum Set−up Time (S0,S1)	t_s		3.3±0.3	−	11.9	13.6	
			5.0±0.5	−	7.0	7.0	
Minimum Set−up Time ($\overline{CLR}$)**	t_s		3.3±0.3	−	5.0	5.0	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time (SL,SR,A～H)	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	
Minimum Hold Time (S0,S1)	t_h		3.3±0.3	−	0.0	0.0	
			5.0±0.5	−	0.0	0.0	
Minimum Hold Time ($\overline{CLR}$)**	t_h		3.3±0.3	−	1.5	1.5	
			5.0±0.5	−	1.5	1.5	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}		3.3±0.3	−	5.0	5.0	
			5.0±0.5	−	3.0	3.0	

Note :* TC74AC299 only

** TC74AC323 only

AC ELECTRICAL CHARACTERISTICS (C_L =50pF, R_L =500Ω, t_r = t_f =3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Propagation Delay Time (CK−QA'QH')	t_{pLH} t_{pHL}		3.3±0.3	−	10.6	18.4	1.0	21.0	ns
			5.0±0.5	−	6.8	10.5	1.0	12.0	
Propagation Delay Time ($\overline{CLR}$−QA'QH')	t_{pHL}		3.3±0.3	−	8.1	14.0	1.0	16.0	
			5.0±0.5	−	6.1	9.2	1.0	10.5	
Propagation Delay Time (CK−QA∼QH)	t_{pLH} t_{pHL}		3.3±0.3	−	10.9	19.3	1.0	22.0	
			5.0±0.5	−	7.3	10.5	1.0	12.0	
Propagation Delay Time ($\overline{CLR}$−QA∼QH)	t_{pHL}		3.3±0.3	−	9.8	16.7	1.0	19.0	
			5.0±0.5	−	6.7	10.9	1.0	12.4	
Output Enable time	t_{pZL} t_{pZH}		3.3±0.3	−	9.9	17.5	1.0	20.0	
			5.0±0.5	−	6.6	9.6	1.0	11.0	
Output Disable time	t_{pLZ} t_{pHZ}		3.3±0.3	−	8.1	14.0	1.0	16.0	
			5.0±0.5	−	6.4	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	45	90	−	45	−	MHz
			5.0±0.5	80	140	−	80	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	137	−	−	−	

Note(1) C_{PD} is defined as the value of the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

* TC74AC299 only

** TC74AC323 only

HEX BUS BUFFER

TC74AC367P/F/FN NON-INVERTED, 3-STATE OUTPUTS
TC74AC368P/F/FN INVERTED, 3-STATE OUTPUTS

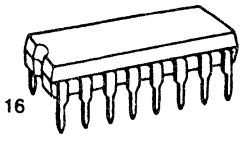
The TC74AC367 and 368 are advanced high speed CMOS HEX BUS BUFFERs fabricated with silicon gate and double -layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

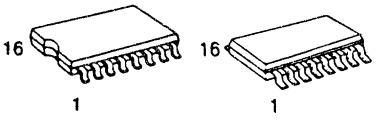
They contain six buffers; four buffers are controlled by an enable input ($\overline{G}1$), and the other two buffers are controlled by enable input ($\overline{G}2$), The outputs of each buffer group are enabled when $\overline{G}1$ and/or $\overline{G}2$ inputs are held low; if held high, these outputs are in a high impedance state.

The TC74AC367 is a non-inverting output type, while the TC74AC368 is an inverting output type.

All inputs are equipped with protection circuits against static discharge or tansient excess voltage.



P(DIP16-P-300A)



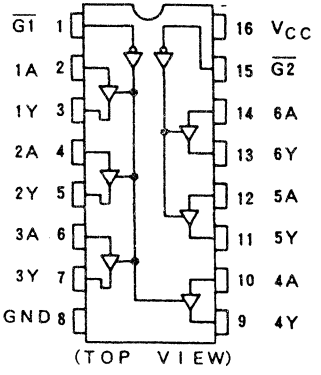
F(SOP16-P-300) FN(SOL16-P-150)

FEATURES:

- High Speed ..... t_{pd}=3.7ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 367/368

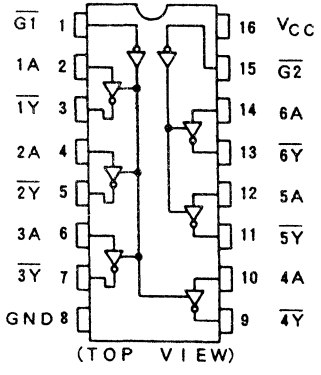
PIN ASSIGN MENT

TC74AC367



(TOP VIEW)

TC74AC368



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	A	Y(367)	$\overline{Y}$(368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X:Don't care
Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

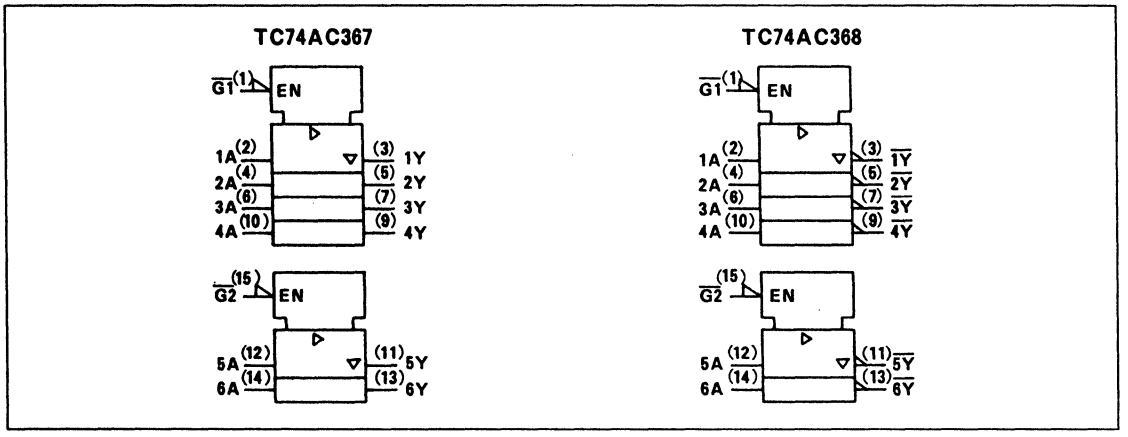
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL}, V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time*	t_{pLH}		3.3±0.3	−	6.5	11.0	1.0	12.5	ns
	t_{pHL}		5.0±0.5	−	4.5	7.0	1.0	8.0	
Propagation Delay Time**	t_{pLH}		3.3±0.3	−	6.1	10.5	1.0	12.0	
	t_{pHL}		5.0±0.5	−	4.3	7.0	1.0	7.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	7.9	13.2	1.0	15.0	
	t_{pZH}		5.0±0.5	−	5.5	8.7	1.0	10.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	6.3	10.5	1.0	12.0	
	t_{pHZ}		5.0±0.5	−	5.2	7.9	1.0	9.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74AC367		−	28	−	−	−	
		TC74AC368		−	25	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per bit)}$$

(2) * for TC74AC367 only
** for TC74AC368 only

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74AC373P/F/FW NON-INVERTING
TC74AC533P/F/FW INVERTING

The TC74AC373 and TC74AC533 are advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

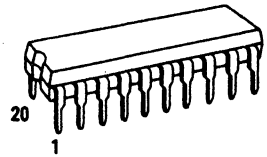
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

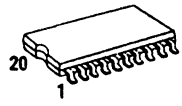
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC373 has non-inverting outputs, and TC74AC533 has inverting outputs.

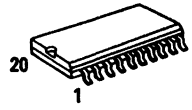
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300)



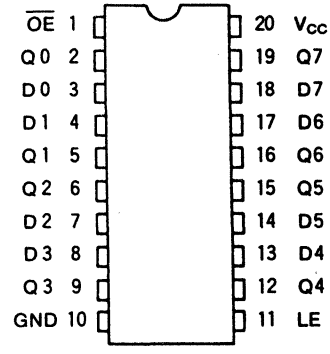
FW(SOL20-P-300)

FEATURES:

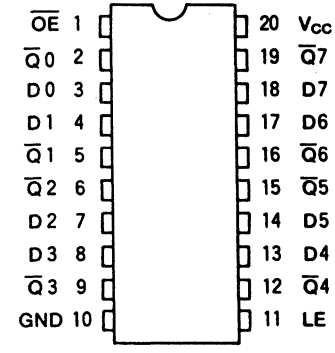
- High Speed ..... t_{pd}=4.8 ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 373/533

PIN ASSIGNMENT (TOP VIEW)

TC74AC373



TC74AC533



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(373)	$\overline{Q}$(533)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

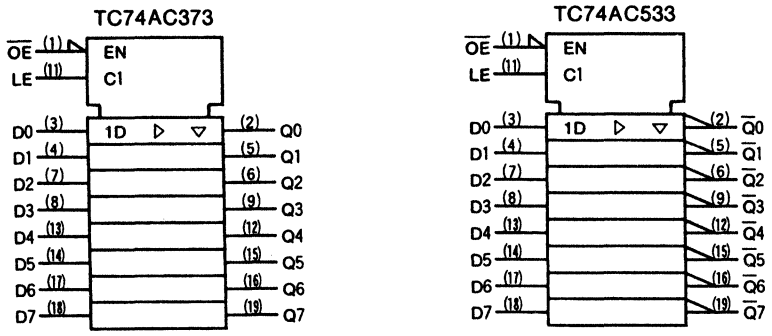
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

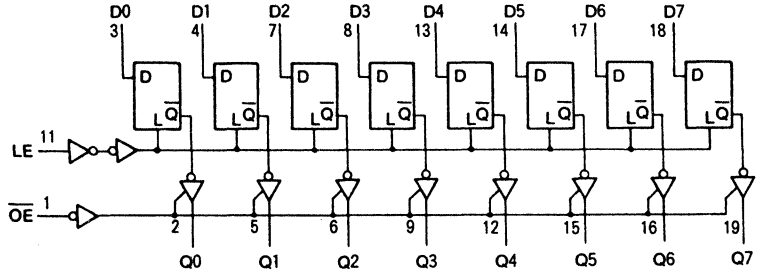
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL

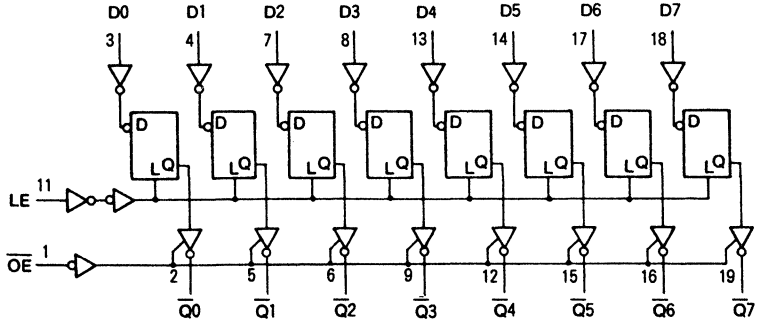


SYSTEM DIAGRAM

TC74AC373



TC74AC533



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	ns
			5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	6.0	6.0	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (LE-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	7.7	13.2	1.0	15.0	ns
	t_{pHL}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Propagation Delay Time (Dn-Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	7.6	12.9	1.0	14.7	
	t_{pHL}		5.0±0.5	−	5.8	8.3	1.0	9.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	7.6	12.9	1.0	14.7	
	t_{pZH}		5.0±0.5	−	6.1	8.7	1.0	10.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.0	11.0	1.0	12.5	
	t_{pHZ}		5.0±0.5	−	5.4	7.5	1.0	8.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=26+12 \cdot n$$

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
TC74ACT373P/F/FW NON-INVERTING
TC74ACT533P/F/FW INVERTING

The TC74ACT373 and TC74ACT533 are advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable (LE) and a output enable input ($\overline{OE}$).

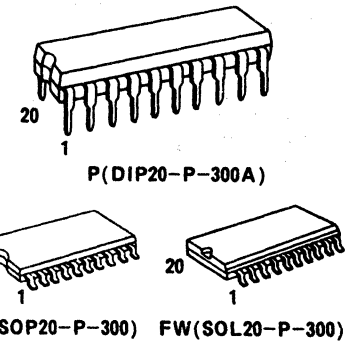
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74ACT373 has non-inverting outputs, and TC74 ACT533 has inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

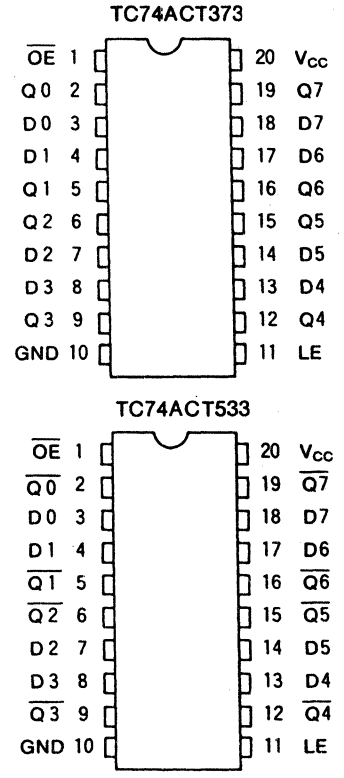
- High Speed ..... t_{pd} = 5.2ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ..... I_{CC} = 8μA (Max.) at Ta = 25℃
- Compatible with TTL outputs..... V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F373/533



P(DIP20-P-300A)

F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(373)	$\overline{Q}$(533)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q (Q) outputs are latched at the time when the LE imput is taken to a low logic level.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

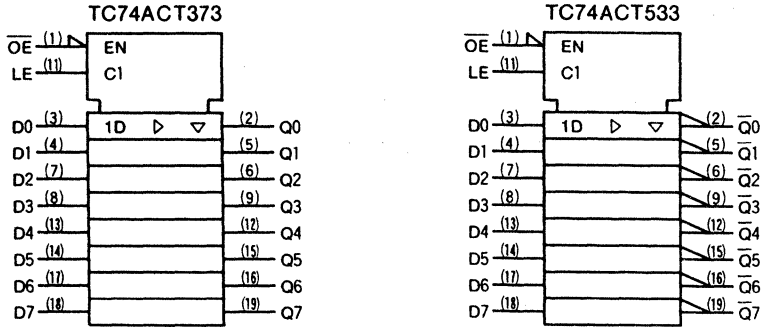
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output * Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

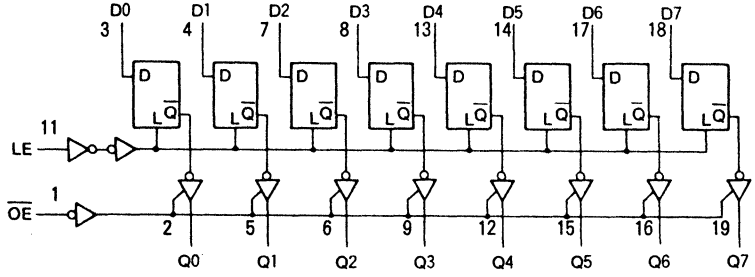
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL

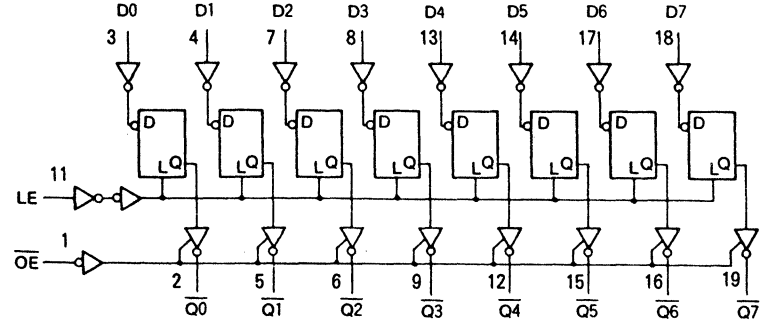


SYSTEM DIAGRAM

TC74ACT373



TC74ACT533



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Set−up Time	t_s		5.0±0.5	−	2.0	2.0	
Minimum Hold Time	t_h		5.0±0.5	−	3.0	3.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	5.8	9.2	1.0	10.5	ns
Propagation Delay Time (Dn−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	5.9	9.6	1.0	11.0	
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	6.5	10.5	1.0	12.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	5.5	7.8	1.0	9.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	32	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8$(per Latch)

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

C_{PD} (total)= + • n

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74AC374P/F/FW NON-INVERTING
TC74AC534P/F/FW INVERTING

The TC74AC374 and TC74AC534 are advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

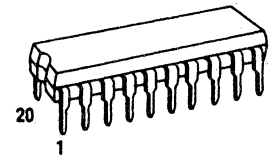
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

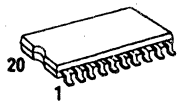
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC374 has non-inverting outputs, and TC74AC534 has inverting outputs.

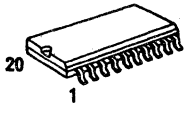
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300)



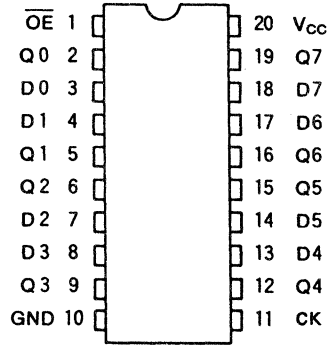
FW(SOL20-P-300)

FEATURES:

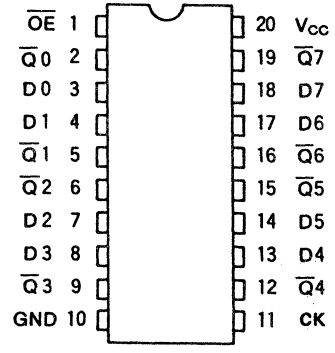
- High Speed ..... f_{MAX}=200MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 374/534

PIN ASSIGNMENT (TOP VIEW)

TC74AC374



TC74AC534



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(374)	$\overline{Q}$(534)
H	X	X	Z	Z
L	↑	X	Q_n	$\overline{Q_n}$
L	↓	L	L	H
L	↓	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Cange

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

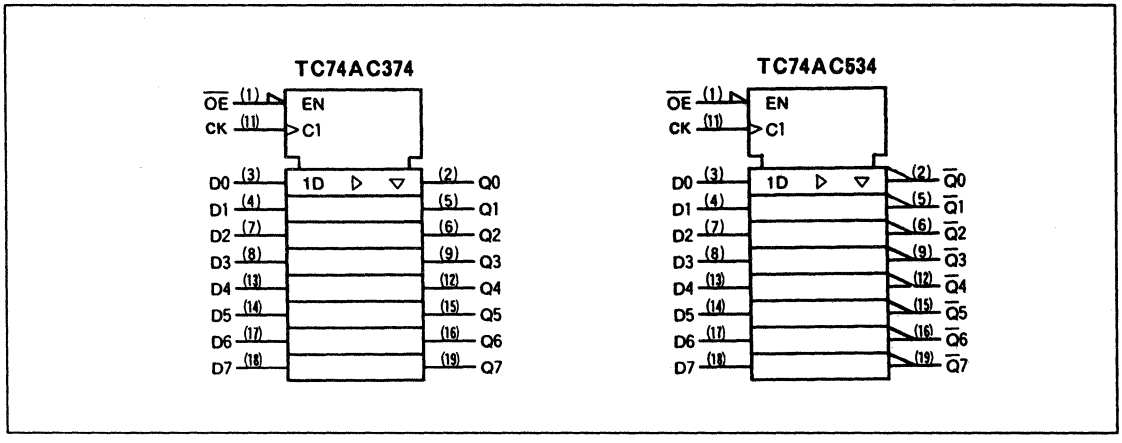
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

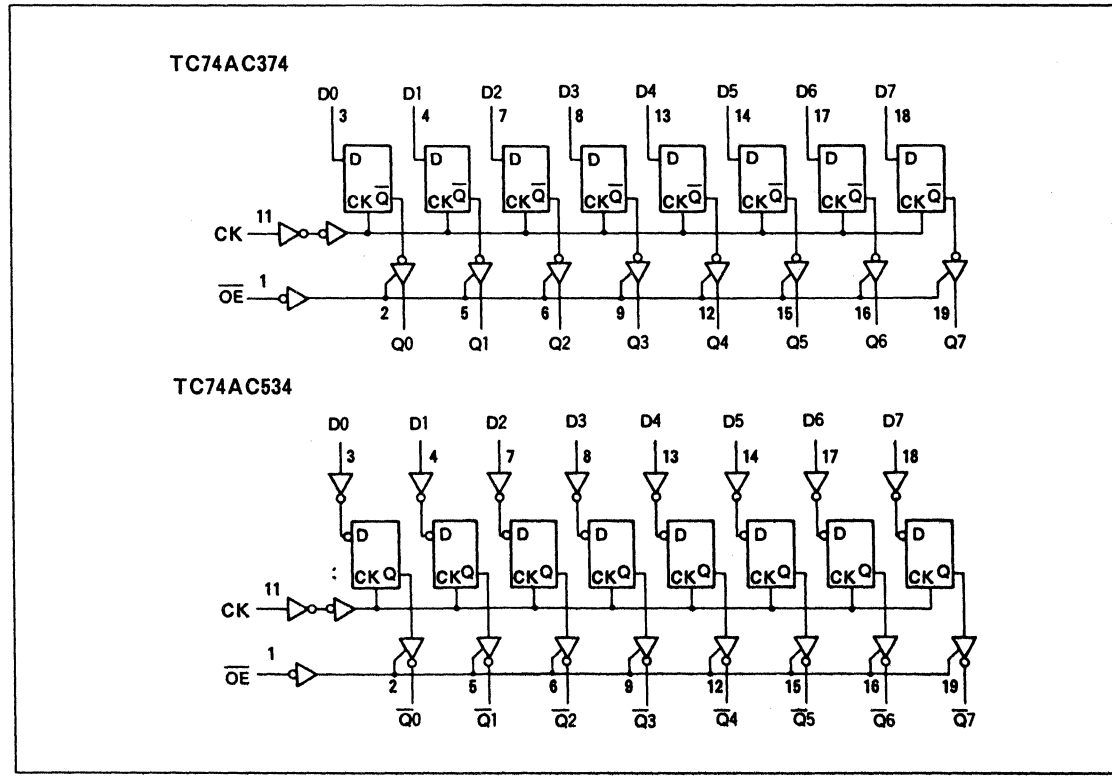
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		3.3±0.3 5.0±0.5	− −	7.0 5.0	7.0 5.0	ns
Minimum Set−up Time	t_s		3.3±0.3 5.0±0.5	− −	9.0 5.0	9.0 5.0	
Minimum Hold Time	t_h		3.3±0.3 5.0±0.5	− −	0.0 0.0	0.0 0.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		3.3±0.3 5.0±0.5	− −	8.5 6.1	15.8 8.7	1.0 1.0	18.0 10.0	ns
Output Enable Time	t_{pZL} t_{pZH}		3.3±0.3 5.0±0.5	− −	7.5 6.1	14.0 8.7	1.0 1.0	16.0 10.0	
Output Disable Time	t_{pLZ} t_{pHZ}		3.3±0.3 5.0±0.5	− −	5.5 4.7	12.3 7.0	1.0 1.0	14.0 8.0	
Maximum Clock Frequency	f_{MAX}		3.3±0.3 5.0±0.5	55 100	120 160	− −	55 100	− −	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	37	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per F/F})$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}\ (\text{total})= 25+ 12 \cdot n$$

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74ACT374P/F/FW NON-INVERTING
TC74ACT534P/F/FW INVERTING

The TC74ACT374 and TC74ACT534 are advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

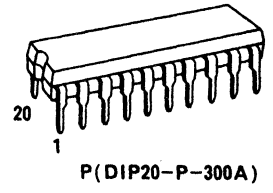
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74ACT374 has non-inverting outputs, and TC74 ACT534 has inverting outputs.

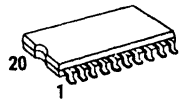
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

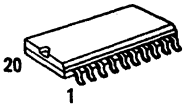
FEATURES:

- High Speed ····· f_{MAX} = 180MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8 μA (Max.) at Ta = 25°C
- Compatible with TTL outputs ····· V_{IL} = 0.8V (Max.)
  V_{IH} = 2V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA (Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 374/534



P(DIP20-P-300A)

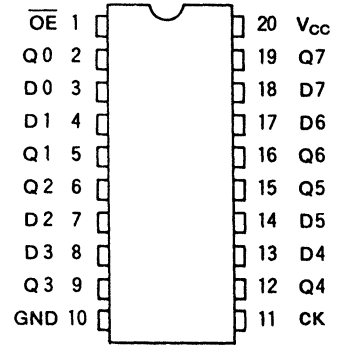




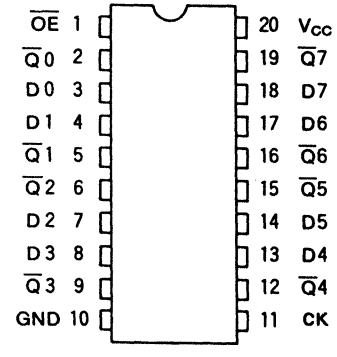
F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT (TOP VIEW)

TC74ACT374



TC74ACT534



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(374)	$\overline{Q}$(534)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Change

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

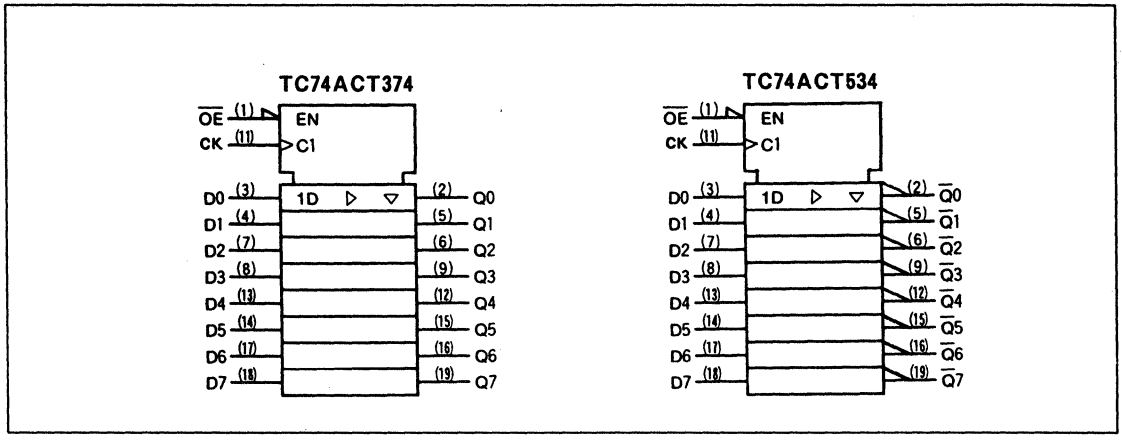
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

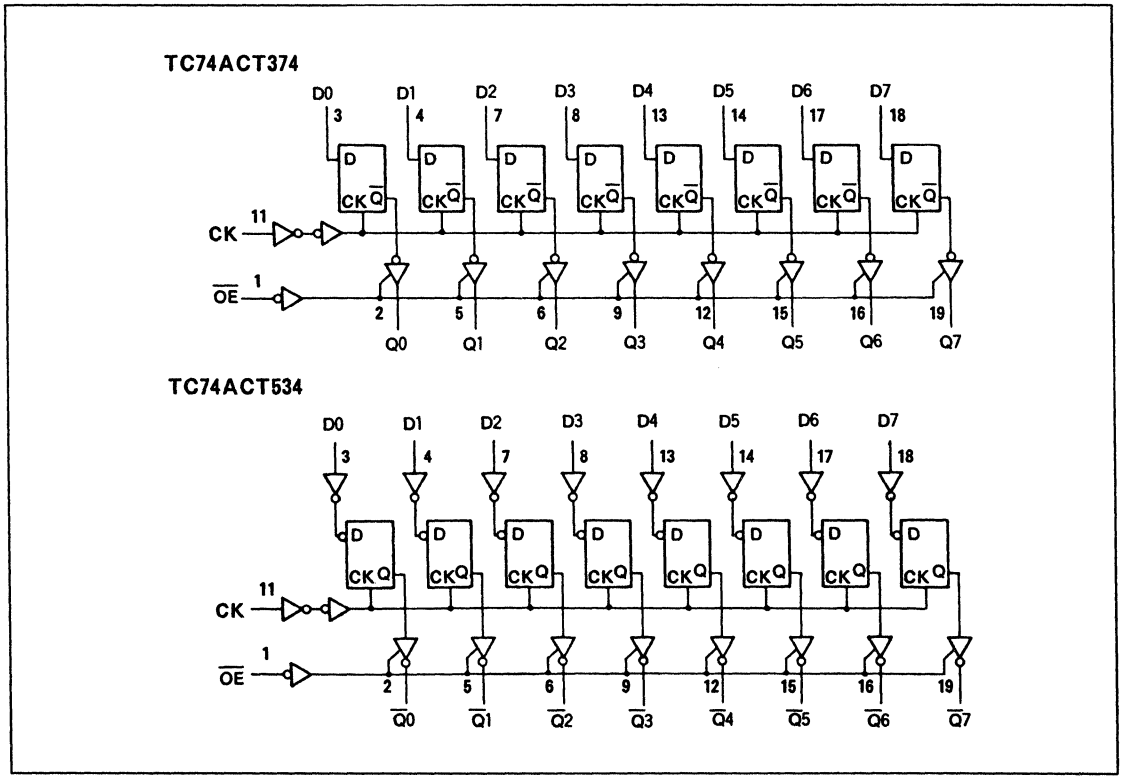
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} = 3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT.	LIMIT.	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		5.0±0.5	−	5.0	5.0	ns
Minimum Set−up Time	t_s		5.0±0.5	−	3.0	3.0	
Minimum Hold Time	t_h		5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40-85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.1	9.6	1.0	11.0	ns
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	6.2	10.1	1.0	11.5	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	5.6	7.9	1.0	9.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	95	160	−	95	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8$(per F/F)

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

C_{PD} (total)= + • n

DUAL DECADE COUNTER

The TC74AC390 is an advanced high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

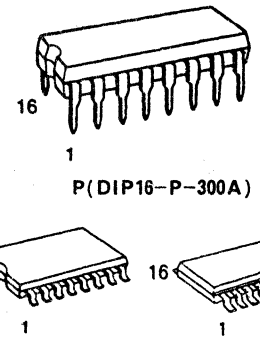
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two counter is incremented on the negative going transition of clock A($\overline{CKA}$). The divide-by-five counter is incremented on the negative going transition of clock B($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set low independent of the clock inputs.

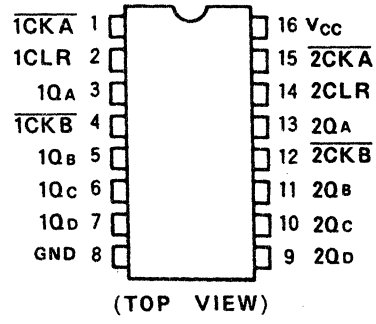
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

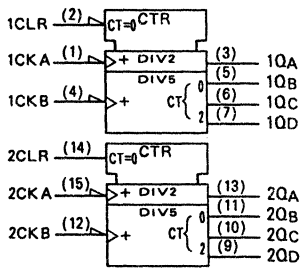
- High Speed ..... f_{MAX}=160MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74HC390



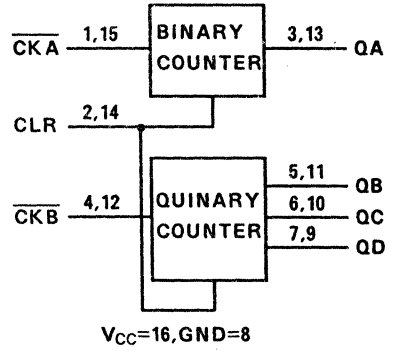
PIN ASSIGNMENT



IEC LOGIC SYMBOL



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

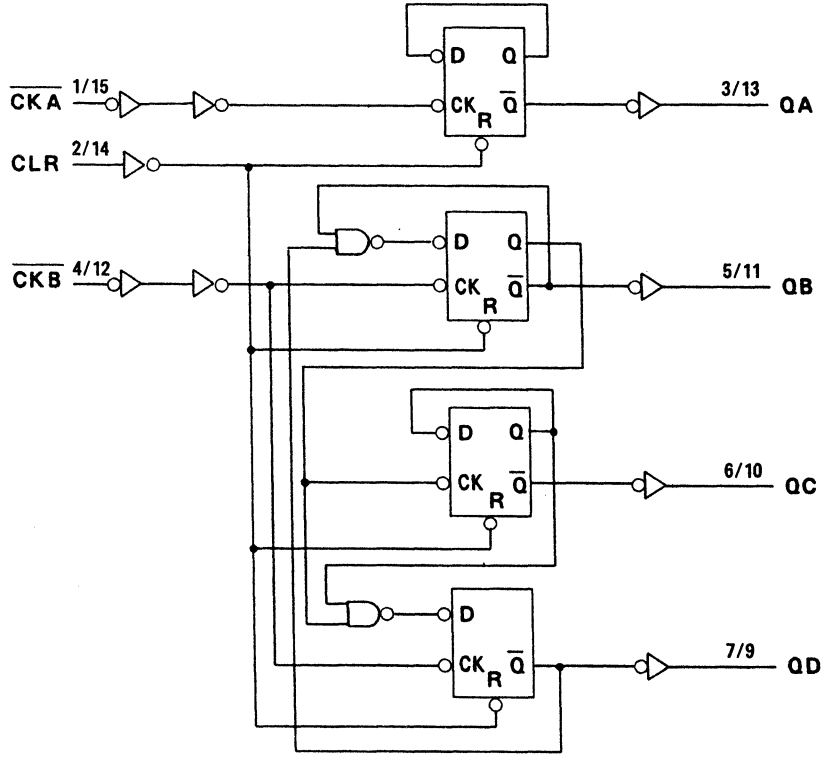
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

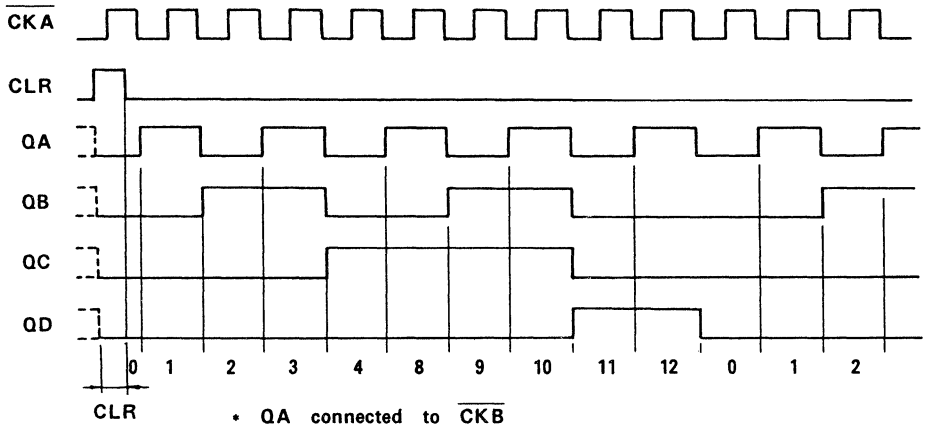
INPUTS			OUTPUTS			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

SYSTEM DIAGRAM

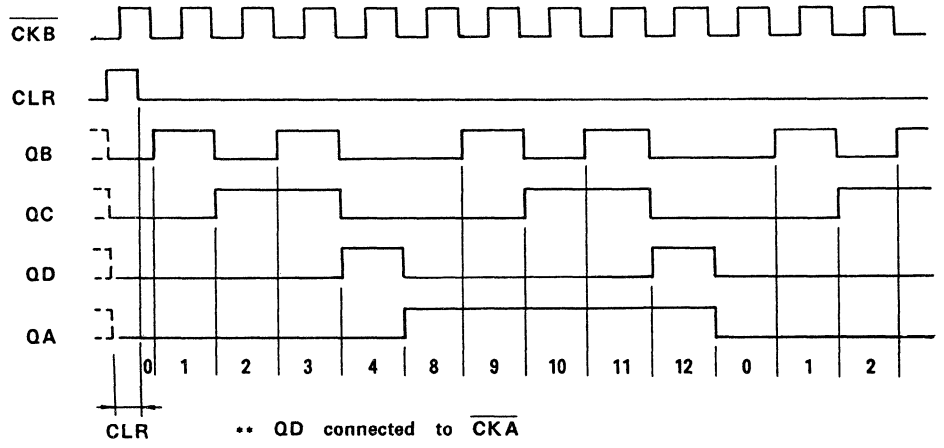


TIMING CHART

(1)BCD COUNT SEQUENCE*



(2)BI-QUINARY COUNT SEQUENCE* *



TIMING REQUIREMENTS (Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	ns
	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
Minimum Pulse Width (CLR)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	5.0	5.0	
Minimum Removal Time	t_{rem}		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	3.5	3.5	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time ($\overline{CKA}$–QA)	t_{pLH}		3.3±0.3	−	8.2	14.0	1.0	16.0	ns
	t_{pHL}		5.0±0.5	−	5.5	8.4	1.0	9.6	
Propagation Delay Time ($\overline{CKA}$–QC)	t_{pLH}	$\overline{QA}$ connected to	3.3±0.3	−	17.0	30.0	1.0	34.0	
	t_{pHL}	$\overline{CKB}$	5.0±0.5	−	10.5	17.5	1.0	20.0	
Propagation Delay Time ($\overline{CKB}$–QB,QD)	t_{pLH}		3.3±0.3	−	8.8	14.9	1.0	17.0	
	t_{pHL}		5.0±0.5	−	6.0	9.4	1.0	10.7	
Propagation Delay Time ($\overline{CKB}$–QC)	t_{pLH}		3.3±0.3	−	11.0	18.8	1.0	21.5	
	t_{pHL}		5.0±0.5	−	7.1	11.3	1.0	12.8	
Propagation Delay Time (CLR–Qn)	t_{pHL}		3.3±0.3	−	7.7	12.5	1.0	14.3	
			5.0±0.5	−	5.7	8.5	1.0	9.7	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}		3.3±0.3	60	120	−	60	−	MHz
			5.0±0.5	100	180	−	100	−	
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}		3.3±0.3	45	90	−	45	−	
			5.0±0.5	90	140	−	90	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	40	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{(per Counter)}$$

DUAL BINARY COUNTER

The TC74AC393 is an advanced high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

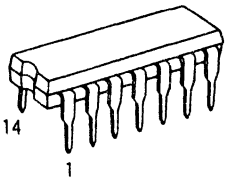
It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the $\overline{CLOCK}$ pulse. The counter can be reset to "0" (Q0~Q3="L") by a high at the CLEAR input regardless of other inputs.

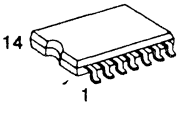
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

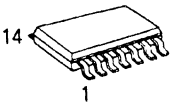
FEATURES:

- High Speed ····· f_{MAX}= MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~5.5V
- Pin and Function Compatible with 74HC393



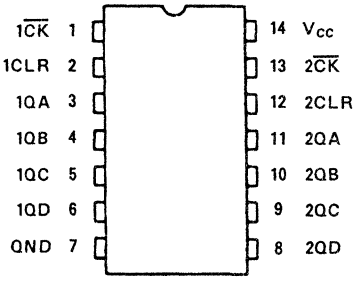
P(DIP14-P-300)





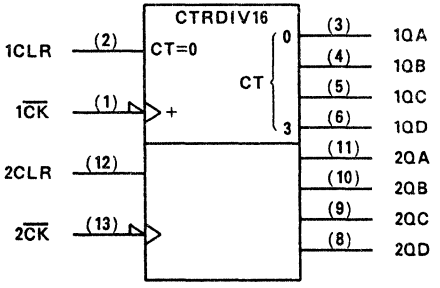
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 100(V_{CC}=3.3±0.3V) 0 ~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

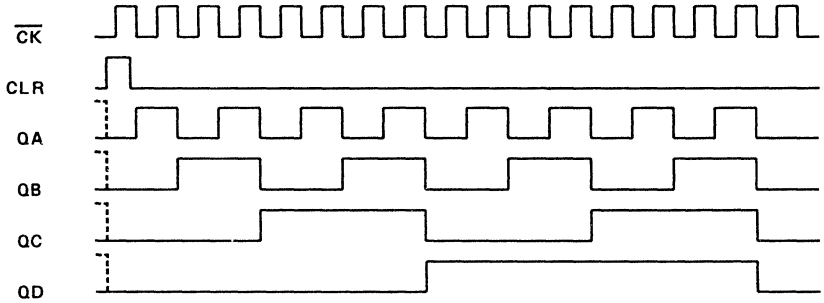
* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

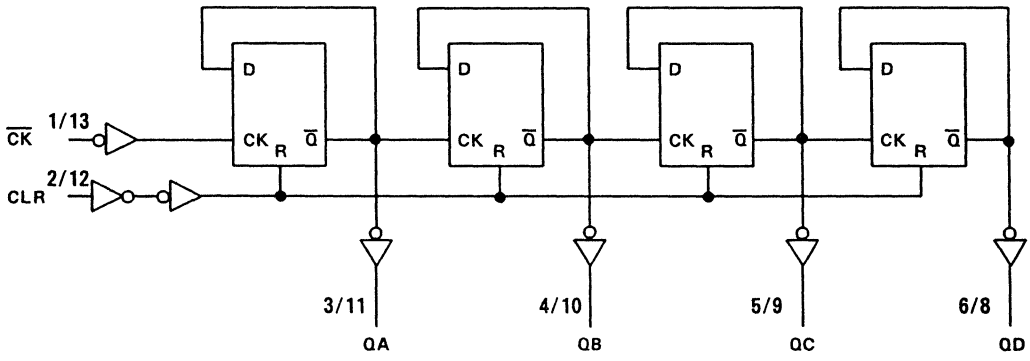
INPUTS		OUTPUTS			
$\overline{CK}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

X : Don't care

TIMING CHART



SYSTEM DIAGRAM



TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{W(H)}$		3.3±0.3	−			ns
	$t_{W(L)}$		5.0±0.5	−			
Minimum Pulse Width (CLR)	$t_{W(H)}$		3.3±0.3	−			
			5.0±0.5	−			
Minimum Removal Time	t_{rem}		3.3±0.3	−			
			5.0±0.5	−			

AC ELECTRICAL CHARACTERISTICS($C_L = 50pF$, $R_L = 500\Omega$ Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time ($\overline{CK}$−QA)	t_{pLH}		3.3±0.3	−			1.0		ns
	t_{pHL}		5.0±0.5	−			1.0		
Propagation Delay Time ($\overline{CK}$−QB)	t_{pLH}		3.3±0.3	−			1.0		
	t_{pHL}		5.0±0.5	−			1.0		
Propagation Delay Time ($\overline{CK}$−QC)	t_{pLH}		3.3±0.3	−			1.0		
	t_{pHL}		5.0±0.5	−			1.0		
Propagation Delay Time ($\overline{CK}$−QD)	t_{pLH}		3.3±0.3	−			1.0		
	t_{pHL}		5.0±0.5	−			1.0		
Propagation Delay Time (CLR−Qn)	t_{pHL}		3.3±0.3	−			1.0		
			5.0±0.5	−			1.0		
Maximum Clock Frequency	f_{MAX}		3.3±0.3			−		−	MHz
			5.0±0.5			−		−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−		−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{(per circuit)}$$

OCTAL BUS BUFFER

TC74AC540P/F/FW INVERTING,3-STATE OUTPUTS
TC74AC541P/F/FW NON-INVERTING,3-STATE OUTPUTS

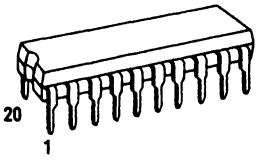
The TC74AC540/TC74AC541 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

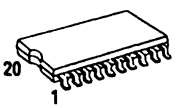
The TC74AC540 is a non-inverting type, and the TC74AC541 is an inverting type.

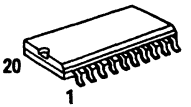
When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)





F(SOP20-P-300) FW(SOL20-P-300)

FEATURES:

- High Speed ····· t_{pd} = 4.0ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ 28% V_{CC} (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr) = 2V~5.5V
- Pin and Function Compatible with 74F540/541

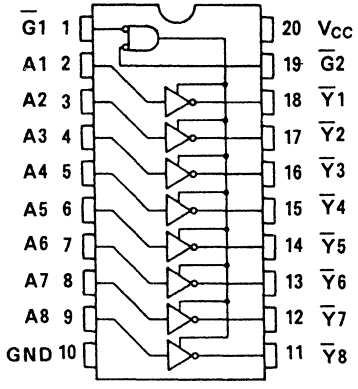
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

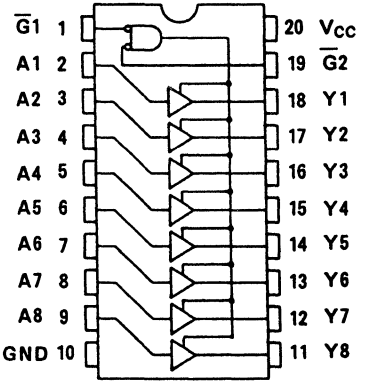
X : Don't Care
Z : High Impedance
* : Yn ····· AC541
$\overline{Yn}$ ····· AC540

PIN ASSIGNMENT

TC74AC540



TC74AC541



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

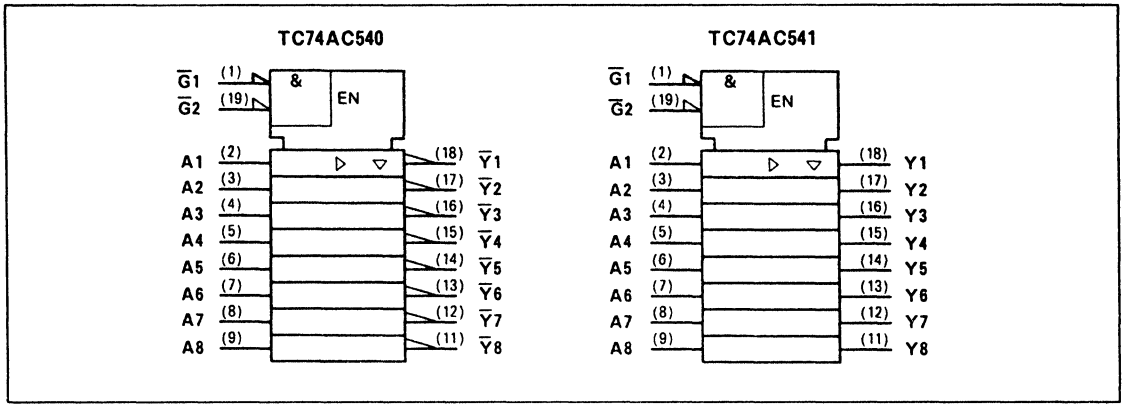
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			Vcc	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time*	t_{pLH}		3.3±0.3	−	6.8	10.5	1.0	12.0	ns
	t_{pHL}		5.0±0.5	−	4.7	7.0	1.0	8.0	
Propagation Delay Time**	t_{pLH}		3.3±0.3	−	6.8	11.4	1.0	13.0	
	t_{pHL}		5.0±0.5	−	4.7	7.5	1.0	8.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	9.6	15.8	1.0	18.0	
	t_{pZH}		5.0±0.5	−	6.4	10.0	1.0	11.4	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.7	12.3	1.0	14.0	
	t_{pHZ}		5.0±0.5	−	6.4	9.3	1.0	10.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74AC540		−	25	−	−	−	
		TC74AC541		−	28	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) * for TC74AC540 only
** for TC74AC541 only

TC74ACT540P/F/FW, TC74ACT541P/F/FW

OCTAL BUS BUFFER

TC74ACT540P/F/FW INVERTING,3-STATE OUTPUTS
TC74ACT541P/F/FW NON-INVERTING,3-STATE OUTPUTS

The TC74ACT540/TC74ACT541 are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

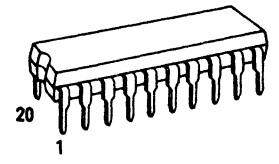
The TC74ACT540 is a non-inverting type, and the TC74 ACT541 is an inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

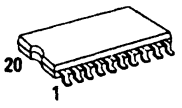
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

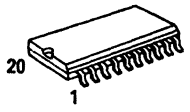
- High Speed ····· t_{pd} = 4.3ns (typ.) at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 8μA(Max.)at Ta=25℃
- Compatible with TTL outputs····· V_{IL} = 0.8V (Max.)
  V_{IH} = 2.0V (Min.)
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F540/541



P(DIP20-P-300A)



F(SOP20-P-300)



FW(SOL20-P-300)

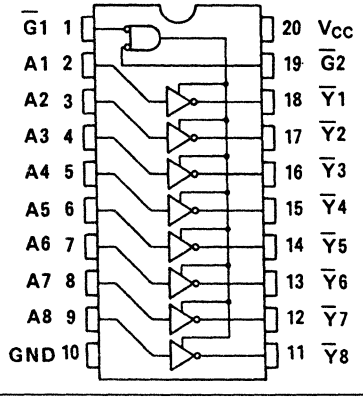
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

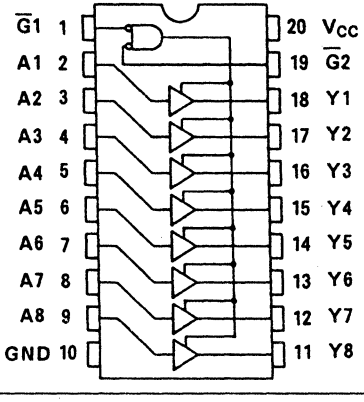
X : Don't Care
Z : High Impedance
* : Yn ····· ACT541
$\overline{Yn}$ ····· ACT540

PIN ASSIGNMENT

TC74ACT540



TC74ACT541



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

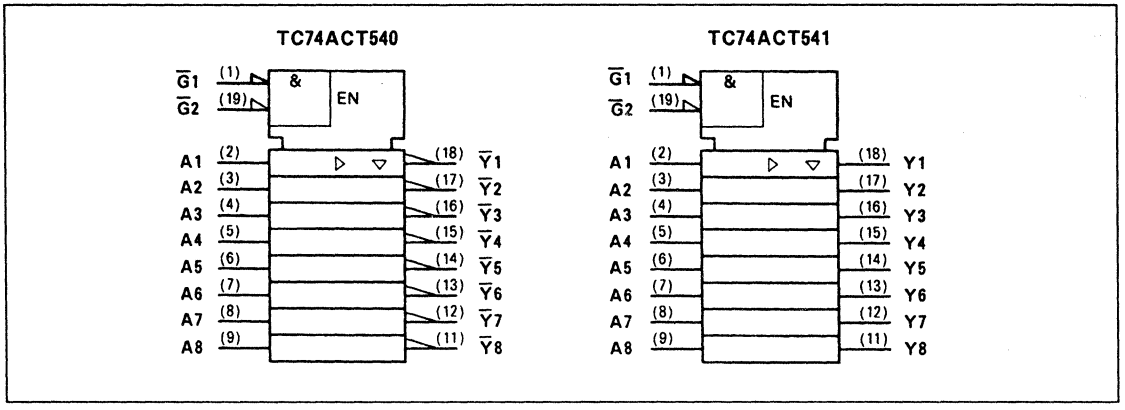
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: Vcc or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40∼85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time*	t_{pLH} t_{pHL}		5.0±0.5	− −	5.0	8.3	1.0	9.5	ns
Propagation Delay Time**	t_{pLH} t_{pHL}		5.0±0.5	− −	5.0	8.3	1.0	9.5	
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	− −	7.3	11.4	1.0	13.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	− −	5.9	9.2	1.0	10.5	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74ACT540		−	24	−	−	−	
		TC74ACT541		−	27	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) * for TC74ACT540 only
** for TC74ACT541 only

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74AC563P/F/FW INVERTING
TC74AC573P/F/FW NON-INVERTING

The TC74AC563 and TC74AC573 are advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

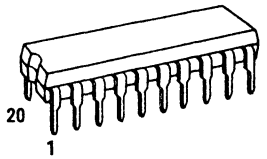
They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

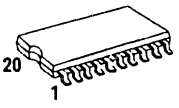
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC563 has inverting outputs, and TC74AC573 has non-inverting outputs.

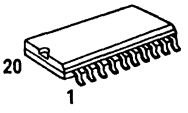
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300)



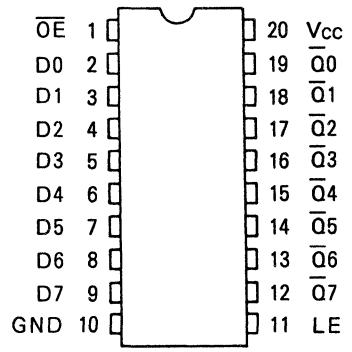
FW(SOL20-P-300)

FEATURES:

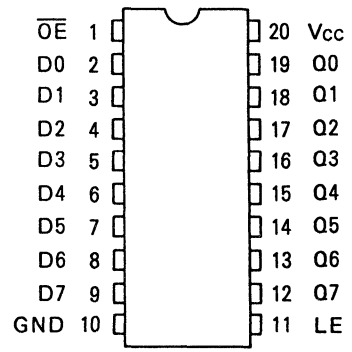
- High Speed ..... t_{pd}=6.0 ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8 μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 563/573

PIN ASSIGNMENT

TC74AC563



TC74AC573



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(573)	$\overline{Q}$(563)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

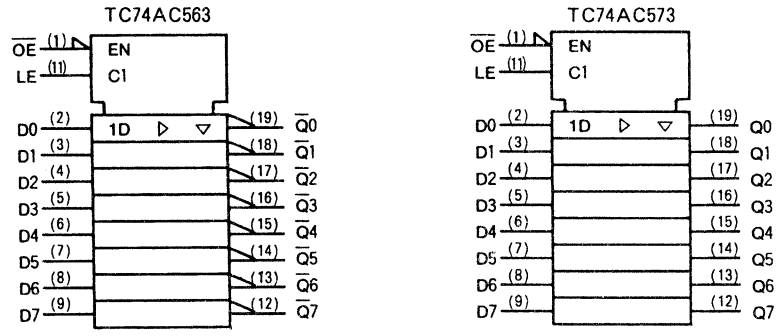
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

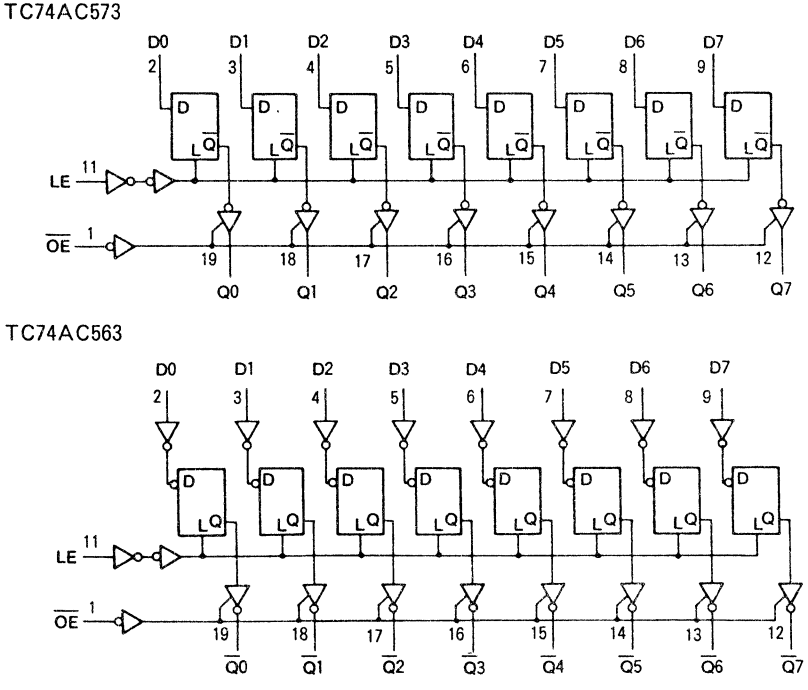
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	ns
			5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	7.0	7.0	
			5.0±0.5	−	4.0	4.0	
Minimum Hold Time	t_h		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	9.4	15.4	1.0	17.6	ns
	t_{pHL}		5.0±0.5	−	6.6	9.9	1.0	11.3	
Propagation Delay Time (Dn−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	9.4	16.0	1.0	18.2	
	t_{pHL}		5.0±0.5	−	6.2	8.9	1.0	10.2	
Output Enable Time	t_{pZL}		3.3±0.3	−	9.0	15.2	1.0	17.3	
	t_{pZH}		5.0±0.5	−	6.3	9.2	1.0	10.5	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.0	12.3	1.0	14.0	
	t_{pHZ}		5.0±0.5	−	6.0	8.8	1.0	10.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	32	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=21+11 \cdot n$$

TC74ACT563P/F/FW, TC74ACT573P/F/FW

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
TC74ACT563P/F/FW INVERTING
TC74ACT573P/F/FW NON-INVERTING

The TC74ACT563 and TC74ACT573 are advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable (LE) and a output enable input ($\overline{OE}$).

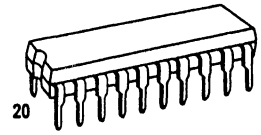
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74ACT573 has non-inverting outputs, and the TC74ACT563 has inverting outputs.

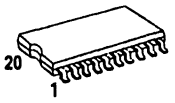
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

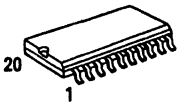
FEATURES:

- High Speed ..... t_{pd}=5.5ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- Compatible with TTL outputs..... V_{IL} =0.8V (Max.)
  V_{IH} =2.0V (Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F563/573



P(DIP20-P-300A)

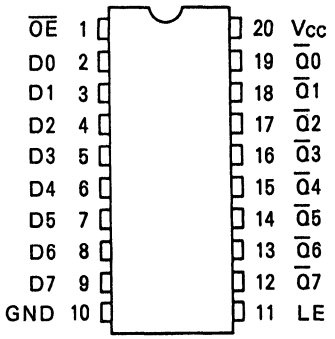




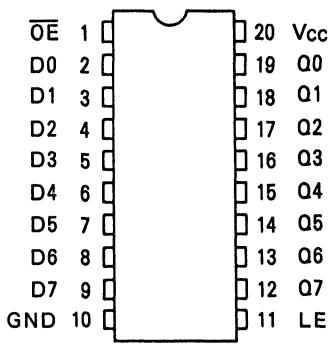
F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT (TOP VIEW)

TC74ACT563



TC74ACT573



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(573)	$\overline{Q}$(563)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q ($\overline{Q}$) outputs are latched at the time when the LE input is taken low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

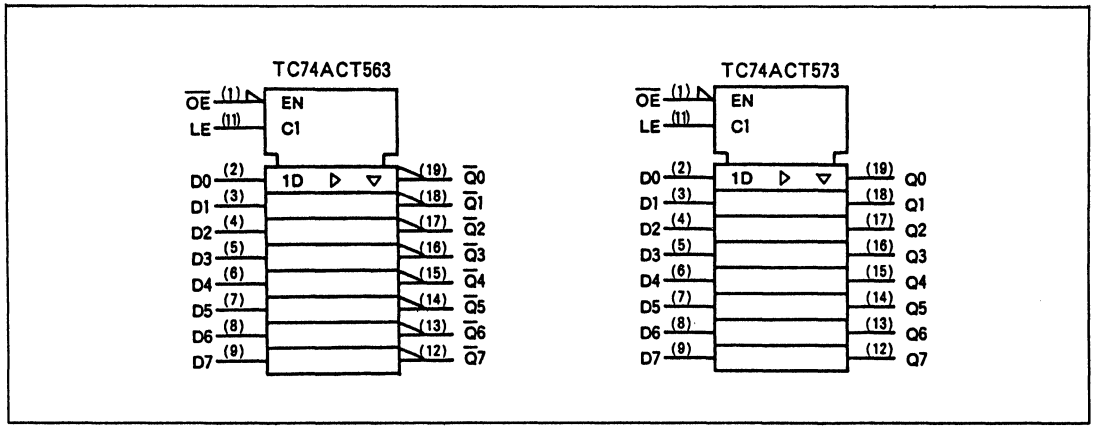
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

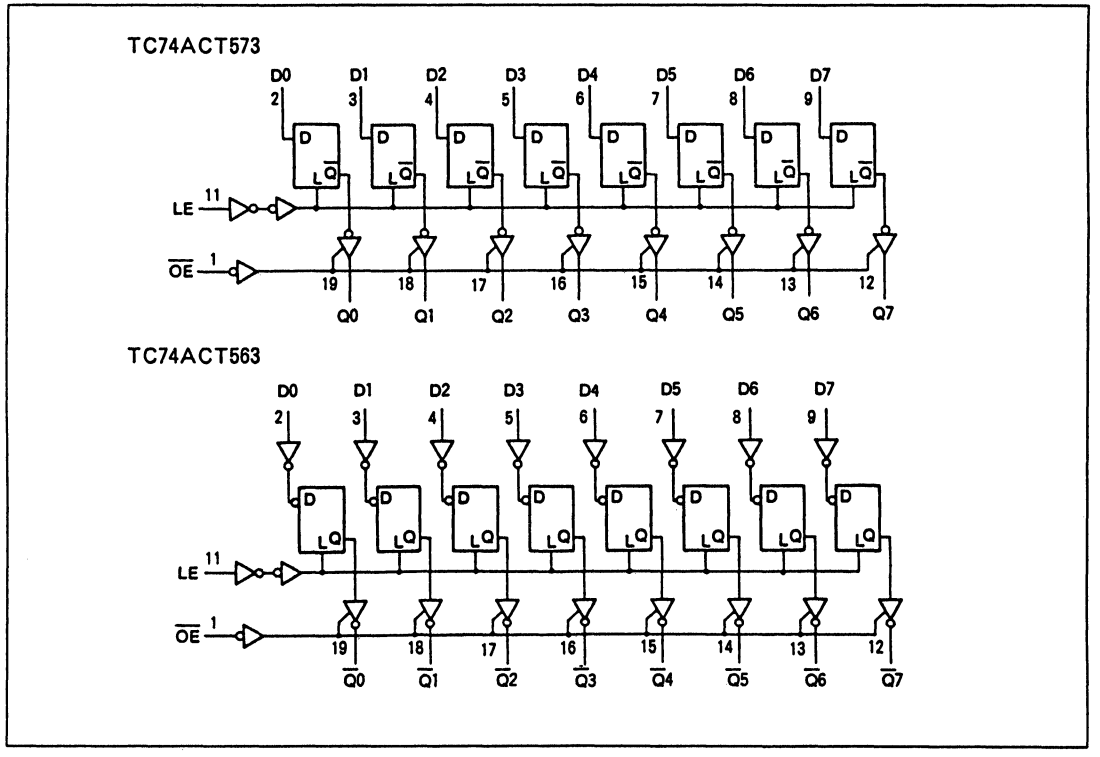
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT:V_{IN} =3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

:This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LE)	$t_{W(H)}$		5.0±0.5	−	5	5	ns
Minimum Set-up Time	ts		5.0±0.5	−	3	3	
Minimum Hold Time	th		5.0±0.5	−	2	2	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.3	10.5	1.0	12.0	ns
Propagation Delay Time (Dn−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.2	9.6	1.0	11.0	
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	6.5	10.0	1.0	11.5	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	6.5	8.8	1.0	10.0	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	22	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=6+16 \cdot n$$

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

TC74AC564P/F/FW INVERTING
TC74AC574P/F/FW NON-INVERTING

The TC74AC564 and TC74AC574 are advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

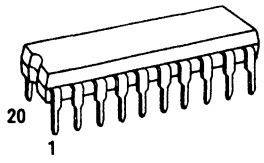
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74AC564 has inverting outputs, and TC74AC574 has non-inverting outputs.

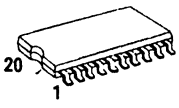
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

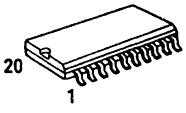
- High Speed ····· f_{MAX}=180MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8 μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 564/574



P(DIP20-P-300A)



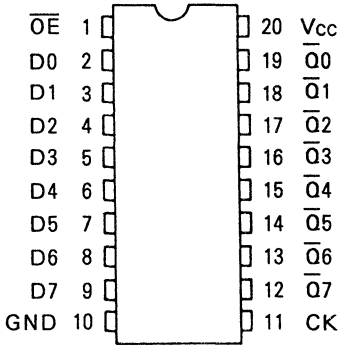
F(SOP20-P-300)



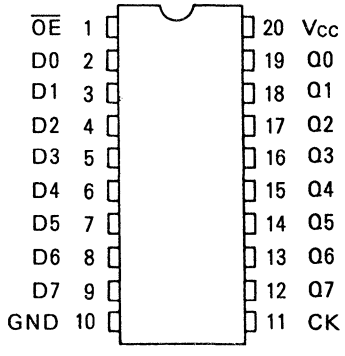
FW(SOL20-P-300)

PIN ASSIGNMENT (TOP VIEW)

TC74AC564



TC74AC574



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574)	$\overline{Q}$(564)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : No Change

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

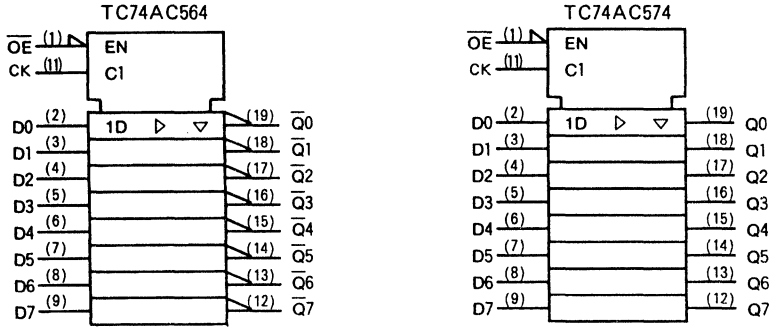
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

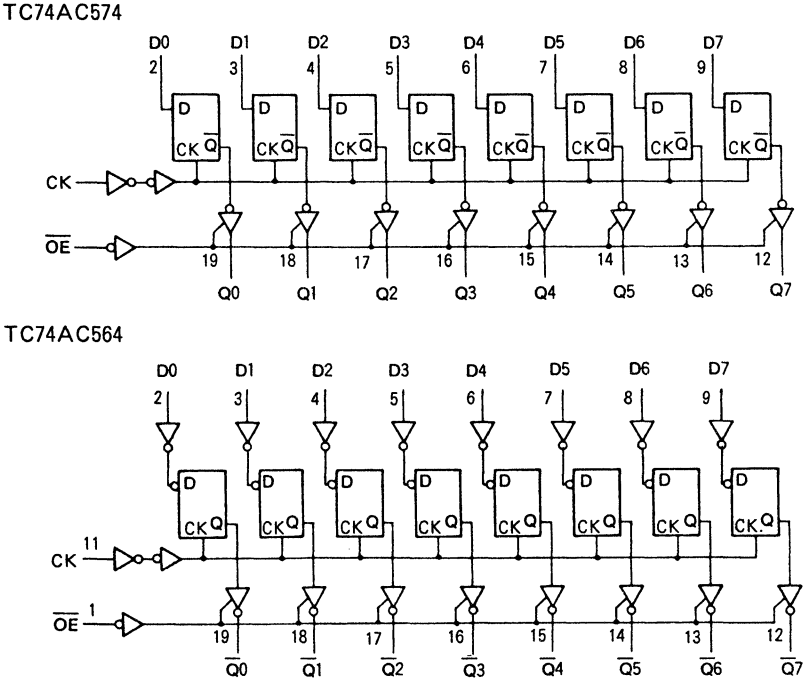
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$		3.3±0.3	−	7.0	7.0	ns
	$t_{W(L)}$		5.0±0.5	−	5.0	5.0	
* Minimum Set-up Time	t_s		3.3±0.3	−	10.0	10.0	
			5.0±0.5	−	5.5	5.5	
** Minimum Set-up Time	t_s		3.3±0.3	−	9.0	9.0	
			5.0±0.5	−	4.5	4.5	
Minimum Hold Time	th		3.3±0.3	−	1.0	1.0	
			5.0±0.5	−	1.0	1.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, $R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		3.3±0.3	−	9.8	16.7	1.0	19.0	ns
	t_{pHL}		5.0±0.5	−	6.1	9.2	1.0	10.5	
Output Enable Time	t_{pLH}		3.3±0.3	−	9.2	15.8	1.0	18.0	
	t_{pHL}		5.0±0.5	−	6.1	9.3	1.0	10.6	
Output Disable Time	t_{pZL}		3.3±0.3	−	6.6	11.0	1.0	12.5	
	t_{pZH}		5.0±0.5	−	5.8	8.8	1.0	10.0	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	50	100	−	50	−	MHz
			5.0±0.5	95	160	−	95	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	36	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=26+10 \cdot n$$

* :for TC74AC564 Only.

**:for TC74AC574 Only.

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74ACT564P/F/FW INVERTING
TC74ACT574P/F/FW NON-INVERTING

The TC74ACT564 and TC74ACT574 are advanced high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

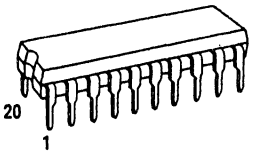
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74ACT564 has inverting outputs, and TC74ACT 574 has non-inverting outputs.

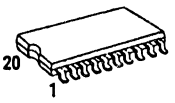
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

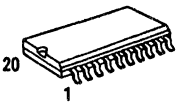
- High Speed ····· f_{MAX}=180MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8 μA(Max.) at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.)
  V_{IH}=2V(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.)
  Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74F 564/574



P(DIP20-P-300A)



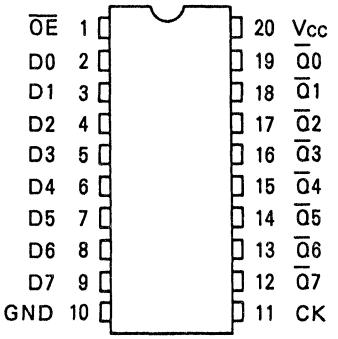
F(SOP20-P-300)



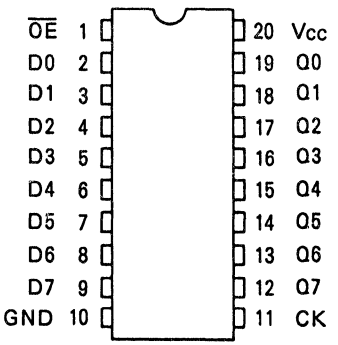
FW(SOL20-P-300)

PIN ASSIGNMENT (TOP VIEW)

TC74ACT564



TC74ACT574

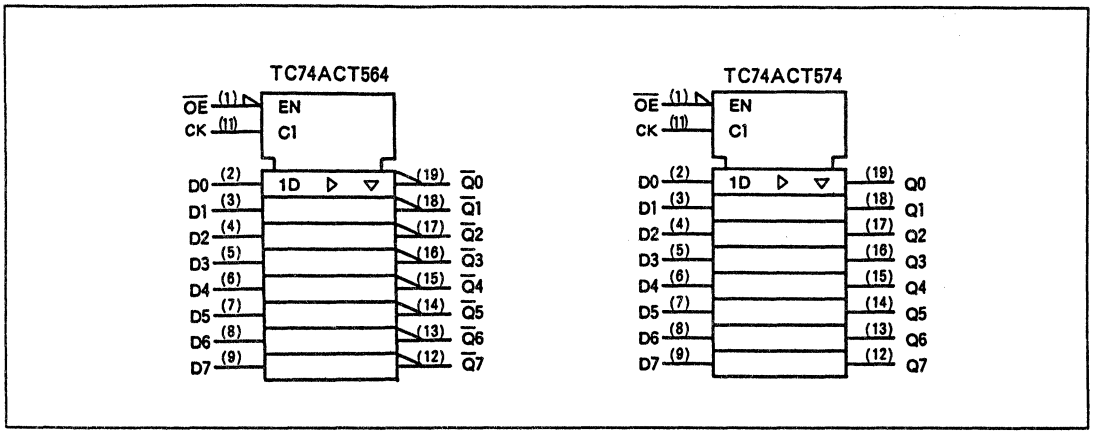


TRUTH TABLE

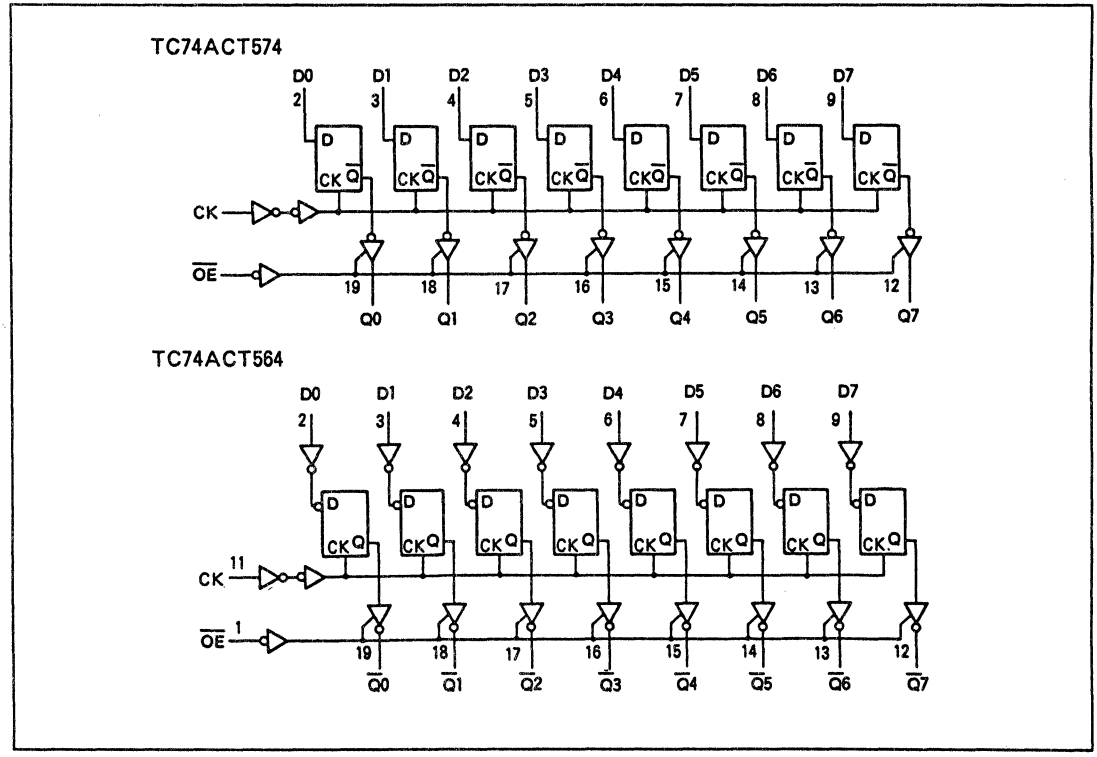
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574)	$\overline{Q}$(564)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0 ~ 10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT: V_{IN} =3.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

*:This spec indicates the capability of driving 50Ω transmission lines. One output should be tested at a time for a 10ms maximum duration.

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT.	Ta=−40 ~85℃ LIMIT.	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		5.0±0.5	−	5	5	ns
Minimum Set-up Time	t_s		5.0±0.5	−	3	3	
Minimum Hold Time	t_h		5.0±0.5	−	2	2	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}		5.0±0.5	−	6.2	10.1	1.0	11.5	ns
Output Enable Time	t_{pZL} t_{pZH}		5.0±0.5	−	6.3	10.5	1.0	12.0	
Output Disable Time	t_{pLZ} t_{pHZ}		5.0±0.5	−	6.6	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	85	160	−	85	−	MHz
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	33	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per F/F})$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

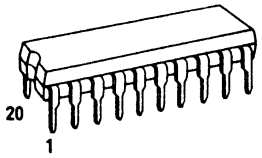
$$C_{PD}(\text{total})=21+12 \cdot n$$

OCTAL BUS TRANSCEIVER
TC74AC620P/F/FW 3-STATE,INVERTING
TC74AC623P/F/FW 3-STATE,NON-INVERTING

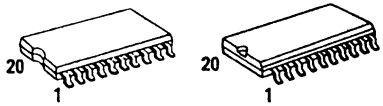
The TC74AC620 and 623 are advanced high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These IC's are intended for two-way asynchronous communication between data buses,and direction of data transmission is determined by GAB, GBA. GAB and $\overline{GBA}$ inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP20-P-300A)



F(SOP20-P-300) FW(SOL20-P-300)

FEATURES:

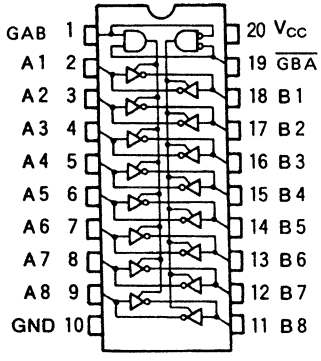
- High Speed ..... t_{pd}=3.9ns (typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=8μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74F 620/623

APPLICATION NOTES

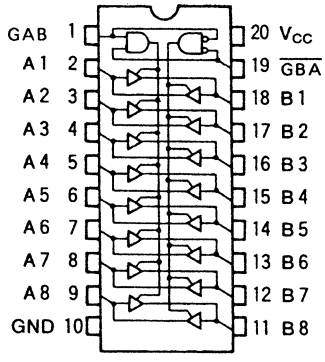
1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)

TC74AC620



TC74AC623



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

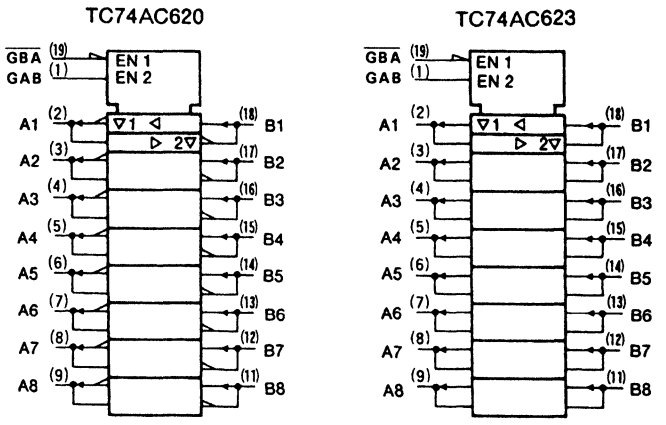
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A Bus	B Bus	AC620	AC623
L	L	Output	Input	$A=\overline{B}$	A=B
H	H	Input	Output	$B=\overline{A}$	B=A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

Z:High Impedance

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time *	t_{pLH}		3.3±0.3	−	6.8	11.4	1.0	13.0	ns
	t_{pHL}		5.0±0.5	−	4.6	7.0	1.0	8.0	
Propagation Delay Time * *	t_{pLH}		3.3±0.3	−	6.8	11.4	1.0	13.0	
	t_{pHL}		5.0±0.5	−	4.6	7.5	1.0	8.5	
Output Enable Time	t_{pZL}		3.3±0.3	−	9.7	15.8	1.0	18.0	
	t_{pZH}		5.0±0.5	−	7.0	10.5	1.0	12.0	
Output Disable Time	t_{pLZ}		3.3±0.3	−	7.8	12.3	1.0	14.0	
	t_{pHZ}		5.0±0.5	−	6.7	9.4	1.0	10.7	
Input Capacitance	C_{IN}	GAB,$\overline{GBA}$		−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An,Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)	TC74AC620		−	30	−	−	−	
		TC74AC623		−	37	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8 \text{(per bit)}$$

(2) * :for TC74AC620 Only.
* * :for TC74AC623 Only

OCTAL BUS TRANSCEIVER/REGISTER
TC74AC646P NON-INVERTING
TC74AC648P INVERTING

The TC74AC646/648 are advanced high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

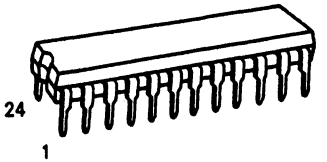
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74AC646 is a non-inverting output type while the TC74AC648 is of the inverting output type.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

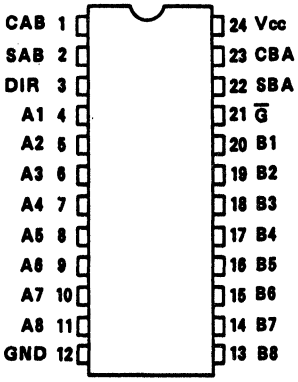
FEATURES:

- High Speed ····· f_{MAX}=150MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{PLH} \fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~5.5V
- Pin and Function Compatible with 74F646/648.



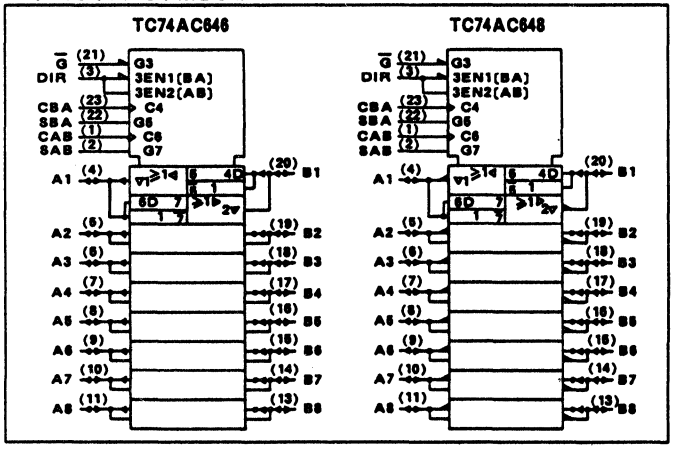
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

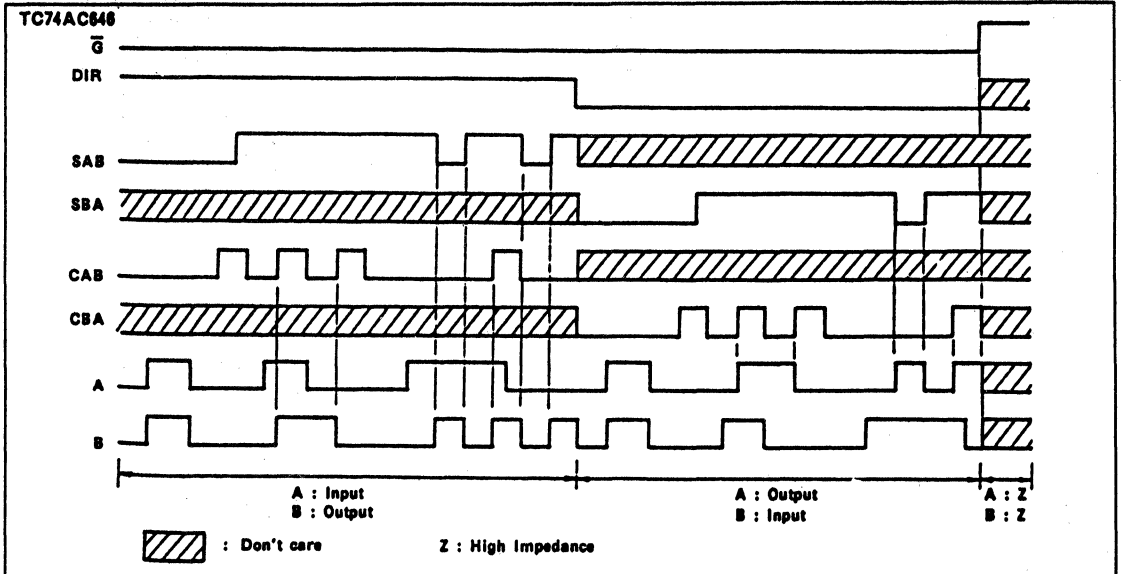


APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

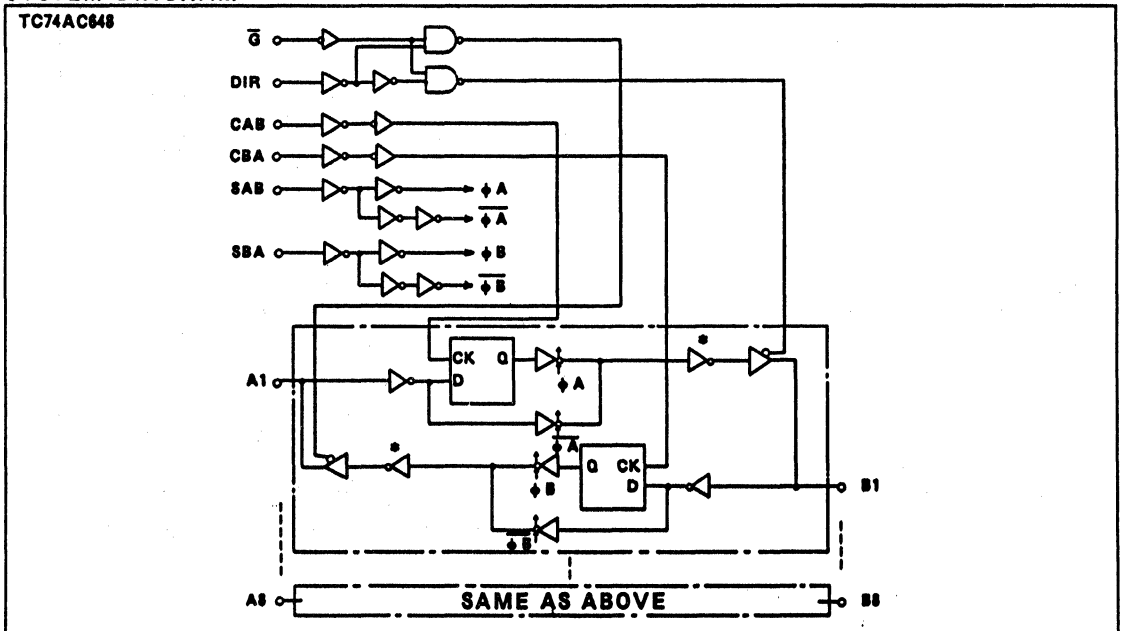
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TIMING CHART



Note: The timing chart for TC74AC648 is the same, but with the outputs inverted.

SYSTEM DIAGRAM



Note: In case of TC74AC648 output inverter marked • at A bus and B bus are eliminated.

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	ns
	$t_{W(H)}$		5.0±0.5	−	5.0	5.0	
Minimum Set-up Time	t_s		3.3±0.3	−	5.0	5.0	
			5.0±0.5	−	3.0	3.0	
Minimum Hold Time	t_h		3.3±0.3	−	2.0	2.0	
			5.0±0.5	−	2.0	2.0	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF, R_L=500\Omega$, Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (BUS-BUS) *	t_{pLH}		3.3±0.3	−	9.2	14.9	1.0	17.0	ns
	t_{pHL}		5.0±0.5	−	6.0	8.7	1.0	10.0	
Propagation Delay Time (CAB,CBA-BUS) *	t_{pLH}		3.3±0.3	−	11.3	19.3	1.0	22.0	
	t_{pHL}		5.0±0.5	−	7.5	11.4	1.0	13.0	
Propagation Delay Time (SAB,SBA-BUS) *	t_{pLH}		3.3±0.3	−	10.4	17.5	1.0	20.0	
	t_{pHL}		5.0±0.5	−	6.9	10.5	1.0	12.0	
Propagation Delay Time (BUS-BUS)**	t_{pLH}		3.3±0.3	−	8.4	14.0	1.0	16.0	
	t_{pHL}		5.0±0.5	−	5.8	8.7	1.0	10.0	
Propagation Delay Time (CAB,CBA-BUS)**	t_{pLH}		3.3±0.3	−	10.8	18.4	1.0	21.0	
	t_{pHL}		5.0±0.5	−	6.9	10.5	1.0	12.0	
Propagation Delay Time (SAB,SBA-BUS)**	t_{pLH}		3.3±0.3	−	10.1	16.7	1.0	19.0	
	t_{pHL}		5.0±0.5	−	6.4	10.1	1.0	11.5	
Output Enable time ($\overline{G}$,DIR-BUS)	t_{pZL}		3.3±0.3	−	10.5	17.5	1.0	20.0	
	t_{pZH}		5.0±0.5	−	6.7	10.5	1.0	12.0	
Output Disable time ($\overline{G}$,DIR-BUS)	t_{pLZ}		3.3±0.3	−	8.5	14.0	1.0	16.0	
	t_{pHZ}		5.0±0.5	−	6.8	9.6	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		3.3±0.3	55	85	−	55	−	MHz
			5.0±0.5	75	130	−	75	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}	Note(AC646)			21				
Power Dissipation Capacitance	C_{PD}	Note(AC648)		−	19	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating curent can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{(per.bit)}$$

*:for TC74AC646 only
**:for TC74AC648 only

TRUTH TABLE

TC74AC648 (The truth table for TC74AC648 is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X	X	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes: X: Don't Care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

Z: High Impedance

• The clocks are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TC74ACT646P, TC74ACT648P

OCTAL BUS TRANSCEIVER/REGISTER

TC74ACT646P NON-INVERTING
TC74ACT648P INVERTING

The TC74ACT646/ACT648 are advanced high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate and dovble-layer metal wiring C^2MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

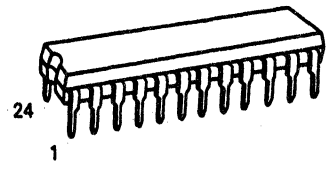
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74ACT646 is a non-inverting output type while the TC74ACT648 is of the inverting output type.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

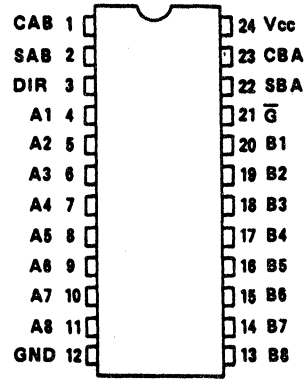
FEATURES:

- High Speed ····· f_{MAX}=160MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- Compatible with TTL Output ····· V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648



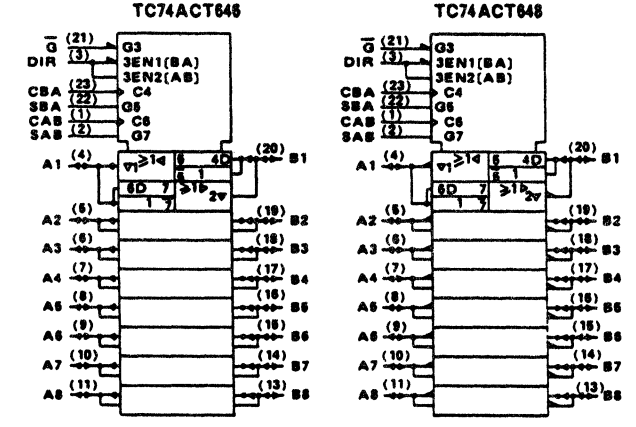
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		5.0±0.5	−	5	5	ns
Minimum Set-up Time	t_s		5.0±0.5	−	3	3	
Minimum Hold Time	t_h		5.0±0.5	−	2	2	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF, R_L=500\Omega$, Input $t_r=t_f=3ns$)

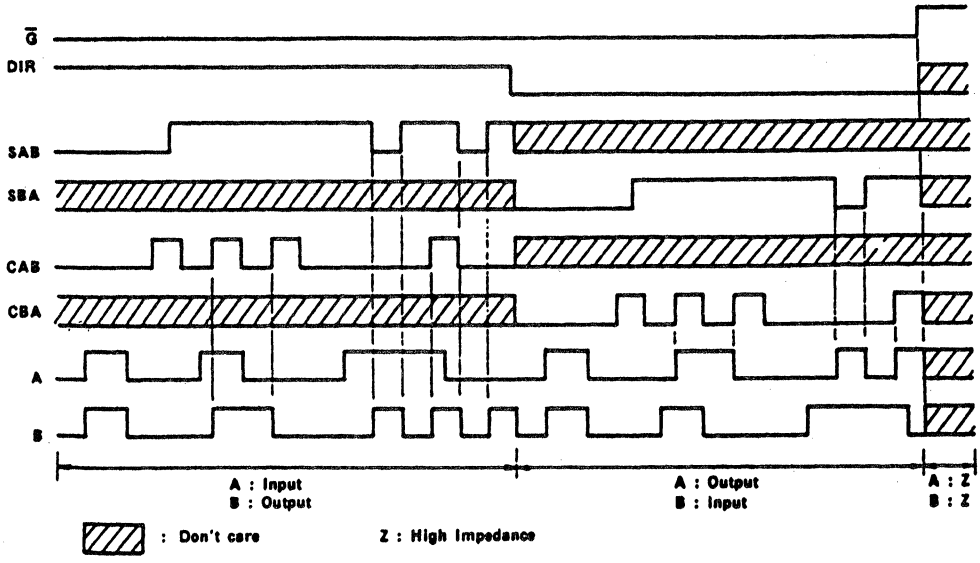
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Propagation Delay Time (BUS–BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.0	9.7	1.0	11.0	ns
Propagation Delay Time (CAB, CBA–BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.9	11.8	1.0	13.5	
Propagation Delay Time (SAB, SBA–BUS)	t_{pLH} t_{pHL}		5.0±0.5	−	6.7	11.0	1.0	12.5	
Output Enable time (DIR, $\overline{G}$–BUS)	t_{pZL} t_{pZH}		5.0±0.5	−	7.1	11.4	1.0	13.0	
Output Enable time (DIR, $\overline{G}$–BUS)	t_{pLZ} t_{pHZ}		5.0±0.5	−	6.9	9.7	1.0	11.0	
Maximum Clock Frequency	f_{MAX}		5.0±0.5	75	145	−	75	−	MHz
Input Capacitance	C_{IN}	DIR, $\overline{G}$, SAB, SBA, CAB, CBA		−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn		−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74ACT646		−	20	−	−	−	
		TC74ACT648		−	19	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from th eoperating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}/8 \text{(per bit)}$$

TIMING CHART

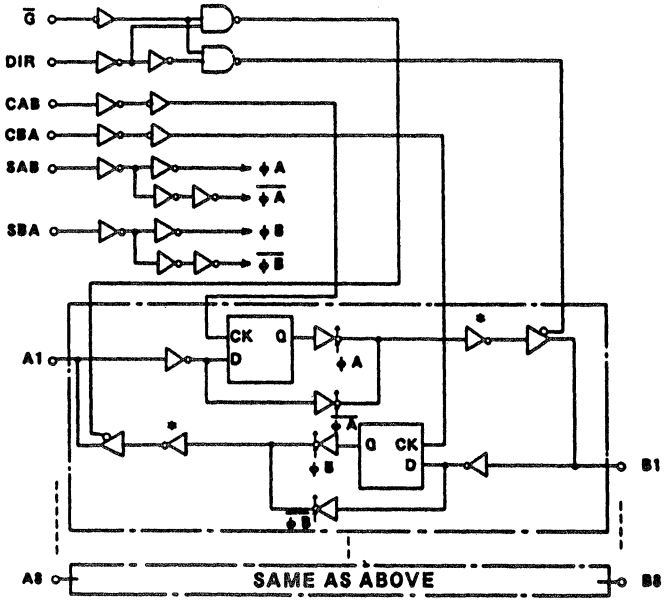
TC74ACT648



Note: The timing chart for TC74ACT648 is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74ACT648



Note: In case of TC74ACT648 output inverter marked • at A bus and B bus are eliminated.

TRUTH TABLE

TC74ACT646(The truth table for TC74ACT648 is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
• The clock are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and /or B Busses may be clocked into the storage flip-flops at any time.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±200	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ should be applied up to 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~10	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−24mA	4.5	3.94	−	−	3.80	−	
			I_{OH}=−75mA*	5.5	−	−	−	3.85	−	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=24mA	4.5	−	−	0.36	−	0.44	
			I_{OL}=75mA*	5.5	−	−	−	−	1.65	
3-State Output Off-State Current	I_{OZ}	V_{IN} =V_{IH} orV_{IL} V_{OUT} =V_{CC} orGND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	
	ΔI_{CC}	PER INPUT:V_{CC}=3.4V OTHER INPUT:V_{CC} or GND		5.5	−	−	1.35	−	1.5	mA

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TC74AC670P/F/FN 4-WORD×4-BIT REGISTER FILE (3-STATE)

The TC74AC670 is an advanced high speed 4-WORD×4-BIT REGISTER FILE fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

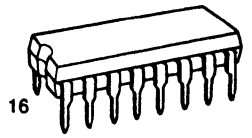
The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply bit word to be stored. Location of the word is determined by the A and B inputs. When the $\overline{\text{WRITE-ENABLE}}$ input is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the $\overline{\text{READ-ENABLE}}$ input is high, the data outputs are inhibited and go into the high-impedance state.

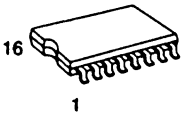
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

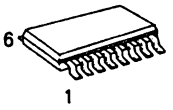
FEATURES:

- High Speed ····· t_{pd}=6.7ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=8μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=24mA(Min.) Capability of driving 50Ω transmission lines.
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~5.5V
- Pin and Function Compatible with 74HC670



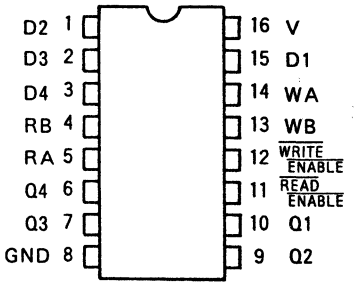
P(DIP16-P-300A)





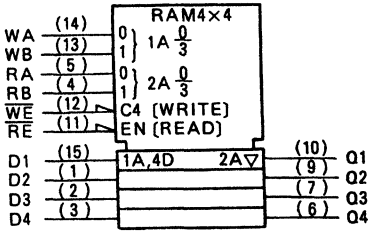
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~6.0	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±50	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	dt/dv	0~100(V_{CC}=3.3±0.3V) 0~ 20(V_{CC}= 5 ±0.5V)	ns/v

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0 3.0 5.5	1.50 2.10 3.85	− − −	− − −	1.50 2.10 3.85	− − −	V
Low−Level Input Voltage	V_{IL}			2.0 3.0 5.5	− − −	− − −	0.50 0.90 1.65	− − −	0.50 0.90 1.65	V
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	− − −	1.9 2.9 4.4	− − −	V
			I_{OH}=−4mA I_{OH}=−24mA I_{OH}=−75mA*	3.0 4.5 5.5	2.58 3.94 −	− − −	− − −	2.48 3.80 3.85	− − −	
Low−Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=50μA	2.0 3.0 4.5	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=12mA I_{OL}=24mA I_{OL}=75mA*	3.0 4.5 5.5	− − −	− − −	0.36 0.36 −	− − −	0.44 0.44 1.65	
3−State Output Off−State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		5.5	−	−	8.0	−	80.0	

* :This spec indicates the capability of driving 50Ω transmission lines.
One output should be tested at a time for a 10ms maximum duration.

TRUTH TABLE

WRITE FUNCTION TABLE

WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

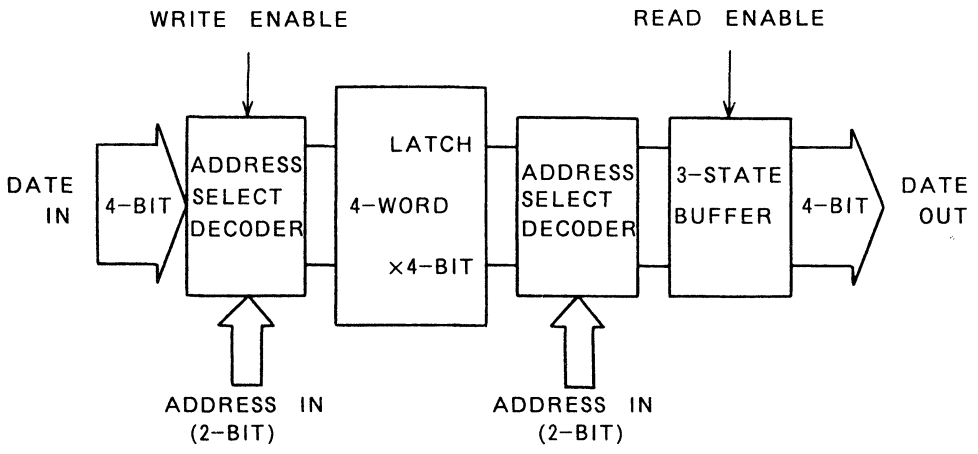
NOTES 1.X:DON'T CARE Z:HIGH IMPEDANCE

2.(Q=D)=THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.

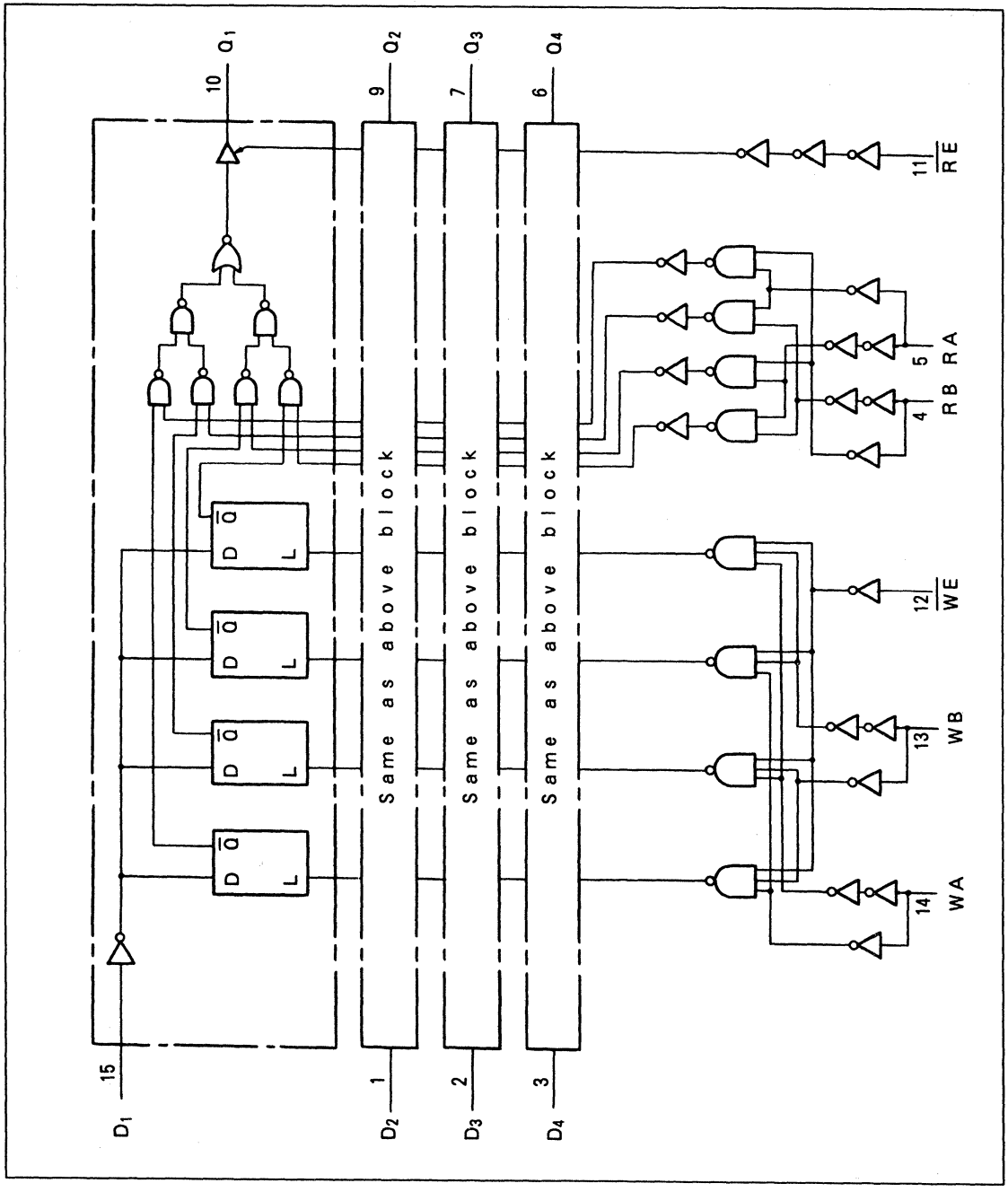
3.Q0=THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

4.W0B1=THE FIRST BIT OF WORD 0,etc.

BLOCK DIAGRAM



SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=3ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{WE}$)	$t_{W(L)}$		3.3±0.3	−	7.0	7.0	ns
			5.0±0.5	−	5.0	5.0	
Minimum Set−up Time (Dn−$\overline{WE}$)	t_s		3.3±0.3	−	9.0	9.0	
			5.0±0.5	−	5.0	5.0	
Minimum Set−up Time (WA,WB−$\overline{WE}$)	t_s		3.3±0.3	−	4.5	4.5	
			5.0±0.5	−	3.5	3.5	
Minimum Hold Time (Dn−$\overline{WE}$)	t_h		3.3±0.3	−	0.0	0.0	
			5.0±0.5	−	0.0	0.0	
Minimum Hold Time (WA,WB−$\overline{WE}$)	t_h		3.3±0.3	−	3.5	3.5	
			5.0±0.5	−	1.5	1.5	
Minimum Latch Time ($\overline{WE}$−RA,RB)	t_{latch} (1)		3.3±0.3	−	4.0	4.0	
			5.0±0.5	−	3.0	3.0	

Note(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has receive new data.

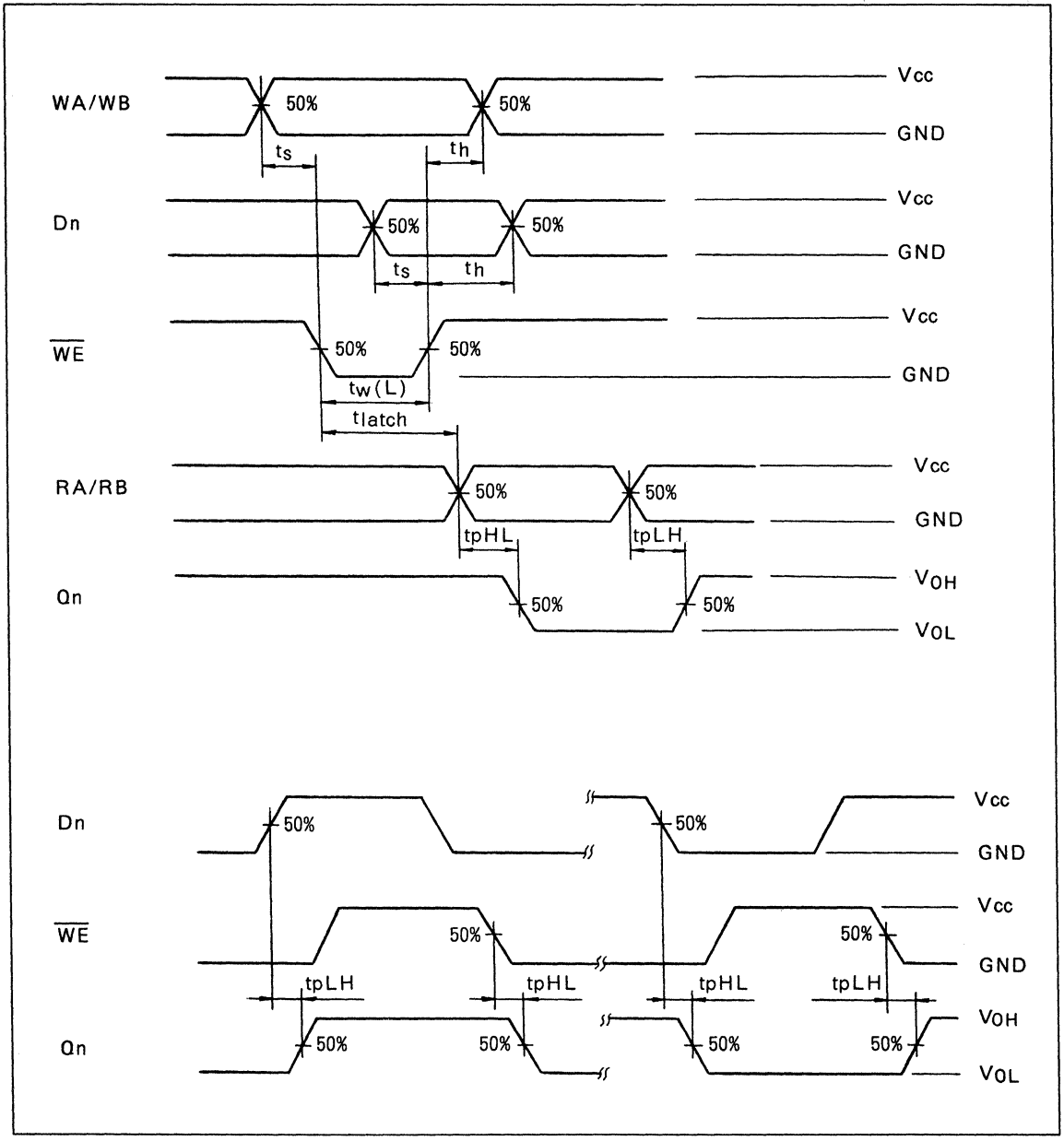
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, R_L=500Ω, Input $t_r=t_f$=3ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40-85℃ MIN.	Ta=−40-85℃ MAX.	UNIT
Propagation Delay Time (RA,RB−Qn)	t_{pLH}		3.3±0.3	−	12.9	22.3	1.0	25.4	ns
	t_{pHL}		5.0±0.5	−	8.6	13.3	1.0	15.1	
Propagation Delay Time ($\overline{WE}$−Qn)	t_{pLH}		3.3±0.3	−	11.1	19.0	1.0	21.7	
	t_{pHL}		5.0±0.5	−	7.4	11.3	1.0	12.9	
Propagation Delay Time (Dn−Qn)	t_{pLH}		3.3±0.3	−	14.7	25.3	1.0	28.8	
	t_{pHL}		5.0±0.5	−	9.9	15.3	1.0	17.4	
Output Enable Time	t_{pZL}		3.3±0.3	−	6.8	11.1	1.0	12.7	
	t_{pZH}		5.0±0.5	−	4.9	8.3	1.0	9.5	
Output Disable Time	t_{pLZ}		3.3±0.3	−	9.0	13.2	1.0	15.0	
	t_{pHZ}		5.0±0.5	−	8.5	11.5	1.0	13.1	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	160	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

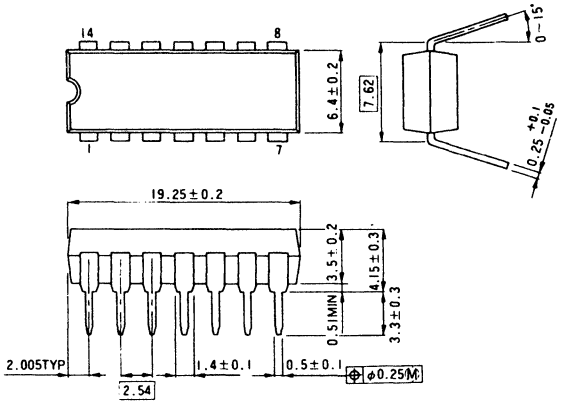


11. OUTLINE DRAWINGS

TC74AC/ACT SERIES

DIP 14PIN OUTLINE DRAWING (DIP14-P-300)

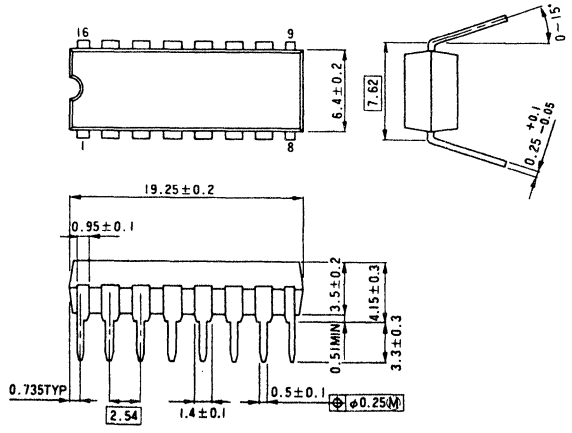
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 16PIN OUTLINE DRAWING (DIP16-P-300A)

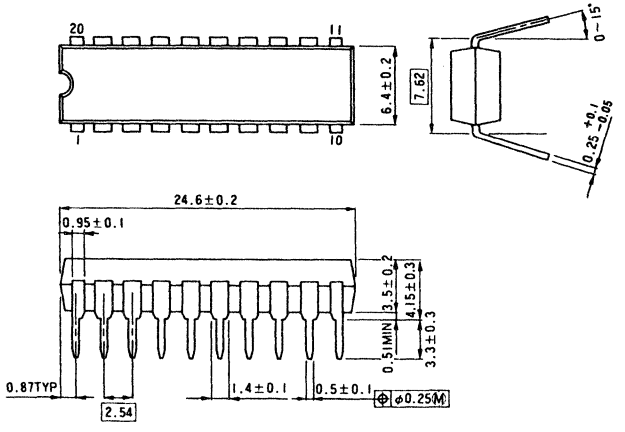
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 20PIN OUTLINE DRAWING (DIP20-P-300A)

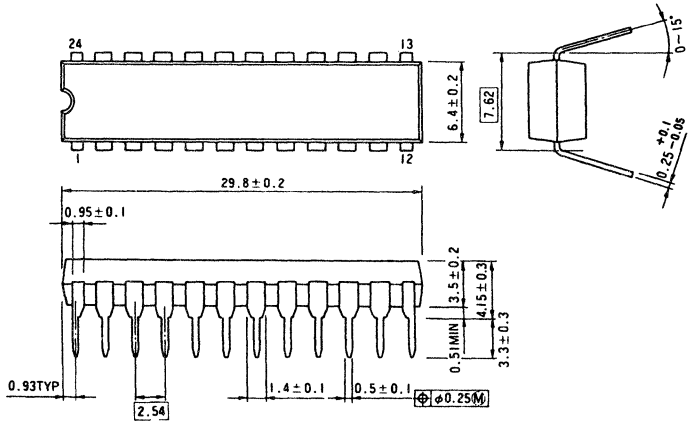
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 24PIN OUTLINE DRAWING (DIP24-P-300)

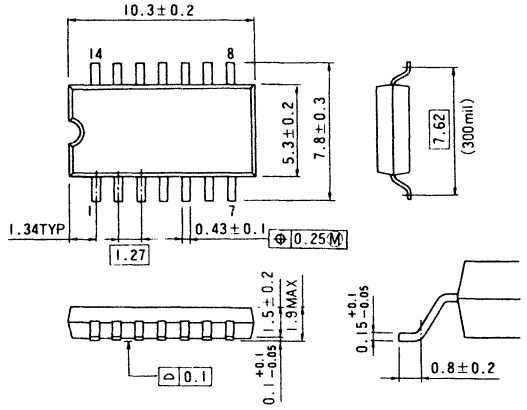
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300)

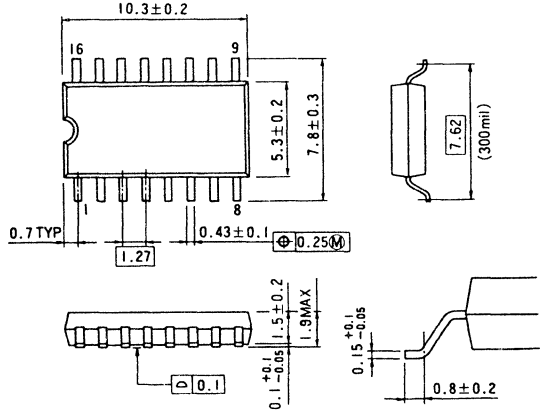
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300)

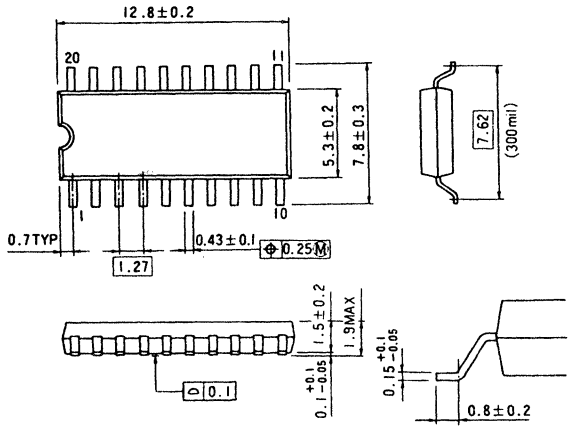
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300)

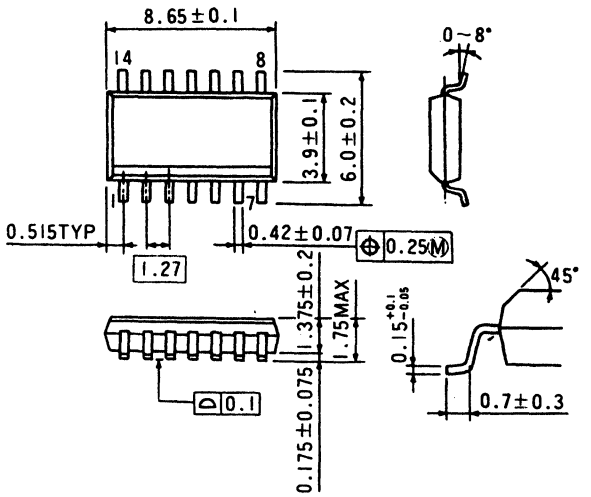
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150)

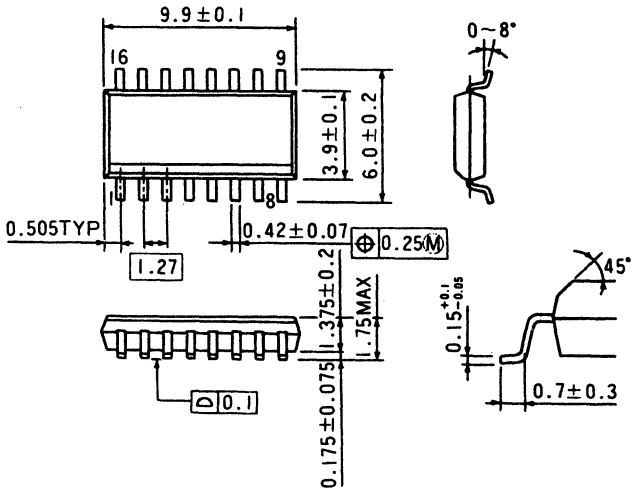
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150)

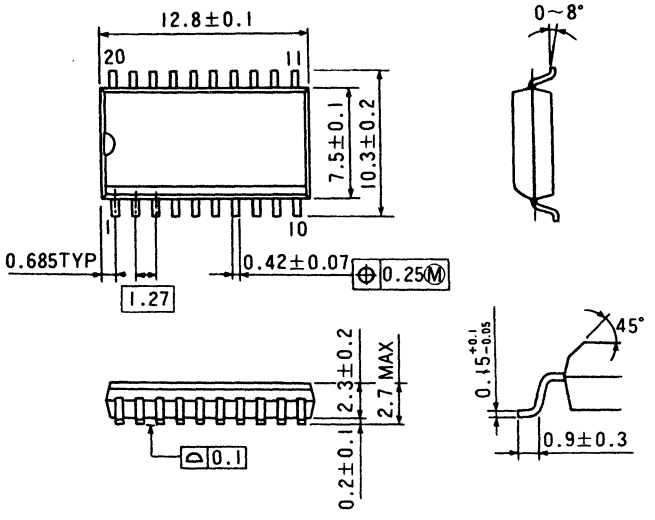
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300)

Unit in mm



Note) Package width and length do not include mold protrusion.

12. RELIABILITY DATA

TC74AC/ACT SERIES

Intrinsic Failure Rate Estimation from Life Test Results

Device	60°C Equivalent Device Hours Ea = 0.8V	Failure	Failure Rate at 60°C (Fit)
2390	308.42×10^6	2	10.1

*60% confidence level.

Reliability Test Results

(1) Long Life Test

Test	Condition		Device	Hours	Equivalent Device Hours @ 60°CEa = 0.8eV	Failures
Steady State Operation	Ta = 125°C Vcc = 6V		1020	1000	106.96×10^6	0
			50	2000		0
High Temp. DC Bias	Ta = 125°C Vcc = 6V		880	1000	201.46×10^6	0
			50	2000		0
	Ta = 150°C Vcc = 6V		250	1000		2*
High Temp. Storage	Ta = 150°C		320	1000	—	0
High Temp. Humidity Bias	Ta = 85°C RH = 85% Vcc = 6V	DIP	1590	1000	—	0
		SOIC	100	1000		0
Low Temp. DC Bias	Ta = −30°C Vcc = 6V		680	1000	—	0

*ICC Leak

(2) Thermal Environmental Test Results

Test	Condition	DIP-14	DIP-16	DIP-20
Soldering Heat	T sol = 260°C 10 sec. once	0/22	0/22	0/22
Temperature Cycle	−65°C~25°C~ 150°C~25°C (30′) (5′) (30′) (5′) ← 1 → 300 cycles	0/100	0/100	0/100
Thermal Start	100°C ← → 0°C (5′) (5′) ← 1 → 30cycles	0/22	0/22	0/22
Moisture Resistance	MIL-STD-883C Method 1004 10 cycles	0/22	0/22	0/22

(3) Mechanical Test Results

Test	Condition	DIP-14	DIP-16	DIP-20
Vibration Fatigue	60 ± 20Hz, 20G 3 orientation 32 Hrs.	0/22	0/22	0/22
Variable Vibration Freq.	100~2000~ 100Hz, 20G 4 min. 3 orientations 4 times each	0/22	0/22	0/22
Mechanical Shock	1500G, 0.5ms 4 orientations 3 times each	0/22	0/22	0/22
Constant Acceleration	20000 G, 6 orientations 1 min. each	0/22	0/22	0/22

(4) Other Test Results

Test	Condition	DIP-14	DIP-16	DIP-20
Solderability	T sol = 230°C 5 sec. once	0/22	0/22	0/22
Lead Integrity	Weight = 250g Bending 3 times 0° ~90° ~0°	0/22	0/22	0/22
Salt Mist	5% salt atmosphere 35°C, 24 Hrs.	0/22	0/22	0/22
Pressure Cooker	2.5 atm. 127°C, 100% 100 Hrs.	0/180	0/220	0/60

(5) Thermal Environmental Test Results (SOIC)

Test	Condition	200mil			150mil		300mil
		14-PIN	16-PIN	20-PIN	14-PIN	16-PIN	20-PIN
Soldering Heat	T sol = 260°C 10 sec. once	0/22	0/22	0/22	0/22	0/22	0/22
Temperature Cycle	−65°C~25°C~ 150°C~25°C (30′) (5′) (30′) (5′) ← 1 ∿ → 300 Cycles	0/50	0/50	0/50	0/50	0/50	0/50
Thermal Shock	100°C ← → 0°C (5′) (5′) ← 1 ∿ → 30cycles	0/22	0/22	0/22	0/22	0/22	0/22
Moisture Resistance	MIL-STD-883C Method 1004 10	0/22	0/22	0/22	0/22	0/22	0/22

(6) Mechanical Test Results (SOIC)

Test	Condition	200mil			150mil		300mil
		14-PIN	16-PIN	20-PIN	14-PIN	16-PIN	20-PIN
Vibration Fatigue	60 ± 20Hz, 20G 3 orientations, 32 Hrs.	0/22	0/22	0/22	0/22	0/22	0/22
Variable Vibration Freq.	100~2000~ 100Hz, 20G 4 min. 3 orientations 4 times each	0/22	0/22	0/22	0/22	0/22	0/22
Mechanical Shock	1500G, 0.5ms. 4 orientations 3 times each	0/22	0/22	0/22	0/22	0/22	0/22
Constant Acceleration	20000 G. 6 orientations 1 min. each	0/22	0/22	0/22	0/22	0/22	0/22

(7) Other Test Results (SOIC)

Test	Condition	200mil			150mil		300mil
		14-PIN	16-PIN	20-PIN	14-PIN	16-PIN	20-PIN
Solderability	T sol = 230°C 5 sec. once	0/22	0/22	0/22	0/22	0/22	0/22
Lead Integrity	Weight = 250g Bending 3 times 0° ~90° ~0°	0/22	0/22	0/22	0/22	0/22	0/22
Salt Mist	5% salt atmosphere 35°C, 25 Hrs.	0/22	0/22	0/22	0/22	0/22	0/22
Pressure Cooker	2.5 atm. 127°C, 100% 100 Hrs.	0/80	0/60	0/90	0/60	0/60	0/60

(8) Moisture Resistance After Vapor Phase Soldering (V.P.S.)

1. Treatment : Ta = 85°C, RH = 85% 20 Hrs.
2. V.P.S. : Ta = 215°C, 1 min × 2 times
3. Pressure Cooker : 2.5atm Ta = 127°C, RH = 100%

Body Size	Device	20Hrs.	50Hrs.	100Hrs.
150mil	150	0	0	0
200mil	300	0	0	0
300mil	100	0	0	0

(9) Moisture Resistance after Solder dipping (200mil SOIC)

1. Treatment : Ta = 85°C, RH = 85% 20 Hrs.
2. Dipping : Ta = 260°C, 10 sec. dip
3. Pressure Cooker : 2.5atm Ta = 127°C, RH = 100%

Device	20Hrs.	50Hrs.	100Hrs.
300	0	0	0

NOTES

13. APPLICATION NOTES

TC74AC/ACT SERIES

13-1. SIMULTANEOUS SWITCHING VOLTAGE NOISE-ADVANCED CMOS LOGIC IC'S

By Dennis Benjamin and Hiroji Tsuchihashi
Toshiba America Electronic Components, Inc.

1. INTRODUCTION

In the early days of bipolar integrated circuits, noise, particularly that noise caused by the voltage generated by the simultaneous switching of multiple inputs, was not a factor in logic design. In fact, the early, slower, low output versions of CMOS logic caused little concern in the design community. However, with the advent of the Advanced CMOS Logic (ACL) and its inherent high output drive current (24mA) and fast edge rates compared with previous CMOS families, noise generation, particularly that created by simultaneous switching voltage (ground bounce), becomes a problem. Additionally, these high voltages can cause errant switching of follow-on devices.

Toshiba Advanced CMOS Logic provides greatly reduced simultaneous switching voltage and, consequently, reduced noise generation. This reduction was obtained by use of modified pre-buffer and buffer circuits. The result is a reduction in the gradient ($\frac{di}{dt}$) of the Vcc to ground path current.

1-1 Definitions

Ground Bounce. When n-1 N channel buffers of a device having n inputs are operated simultaneously, current flows as shown in fig. 1-1. This current ($i_1 + i_2 + ... + i_{n-1}$) flows through the inductance created by the leadframe, bondwire, etc. If the n input is held at ground, the output will "bounce" due to this current flow.

Vcc Bounce. A similar action except that the P channel buffers are operated simultaneously and the n input is held at Vcc.

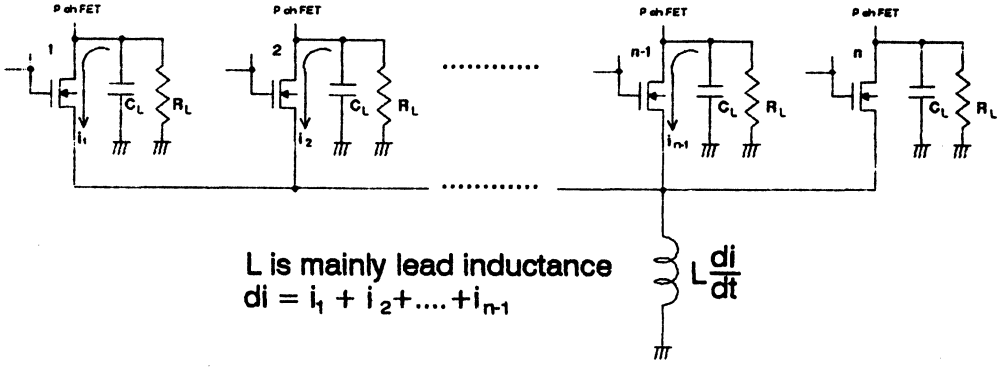
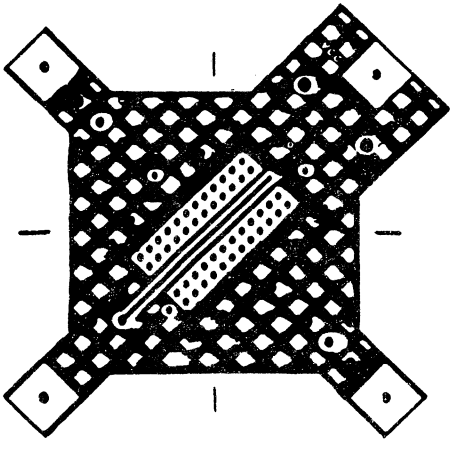
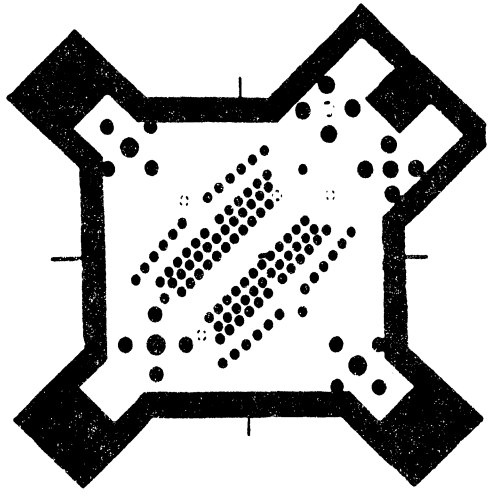


Fig. 1-1

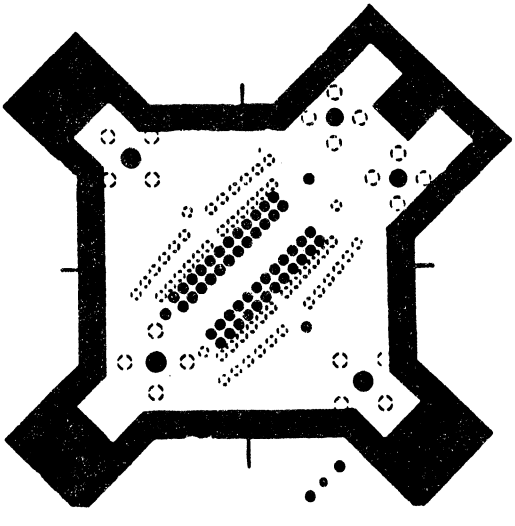
TOSHIBA'S SIMULTANEOUS SWITCHING VOLTAGE TEST BOARD



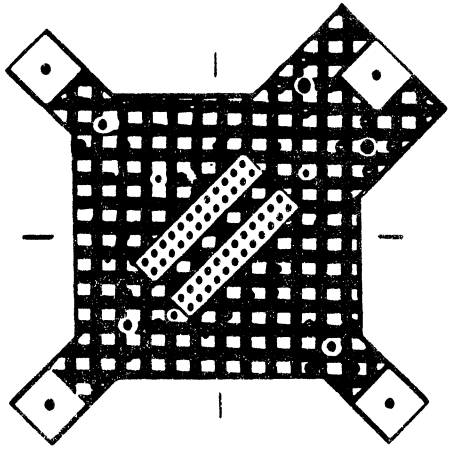
TOP METAL
VIEWED FROM ABOVE



LAYER 2
VIEWED FROM ABOVE



LAYER 3
VIEWED FROM ABOVE



BOTTOM METAL
VIEWED FROM BELOW

2. MEASURING SIMULTANEOUS SWITCHING NOISE

2-1 Test Description

2-1-1 Test Circuit

The test board used by Toshiba is a small, multilayer printed circuit board figs. (2-1, 2-2). Fig. 2-3 shows the connection and test equipment used. All leads are kept as short as possible and the probes are grounded as close to the device under test (DUT). All resistors and capacitors as well as the DUT are soldered to the board. Oscilloscope connections are made to the unswitched output as well as to one of the switched outputs. This allows for timing comparisons. The unswitched input is held at either ground or Vcc depending on the part type and whether measurement of V_{OLP} or V_{OHV} is being measured. The values of C_L and R_L are determined by the test requirements.

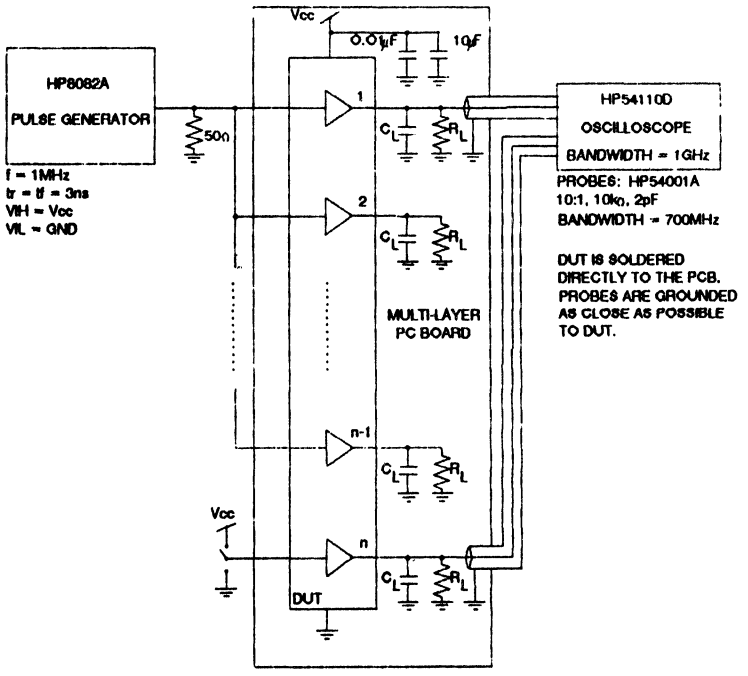


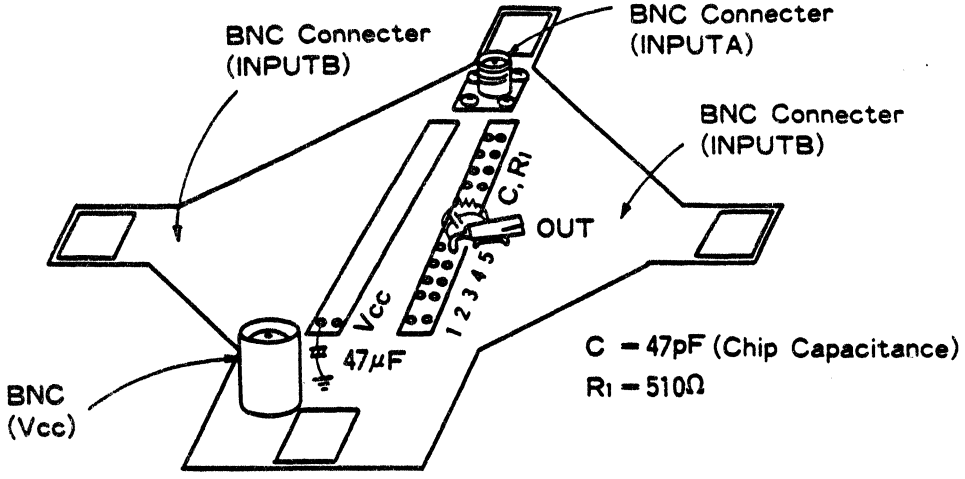
Fig. 2-3

2-1-2 Output Waveforms

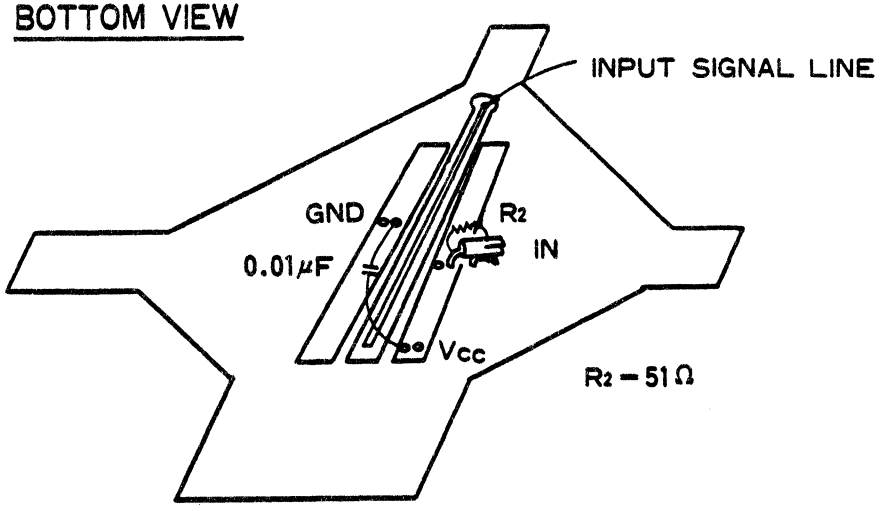
When an input pulse (Toshiba uses a 1 MHz pulse with tr = tf = 3ns) is applied to n-1 inputs of a device having n inputs, the nth output is observed on the oscilloscope along with one of the switched outputs (1 to n-1). A typical waveform is shown in fig. 2-4. Depending on the input level on the nth input and the device type, only the Vcc or GND waveform will appear in addition to the waveform for the switched output.

PC Board for ACL Switching Measurement

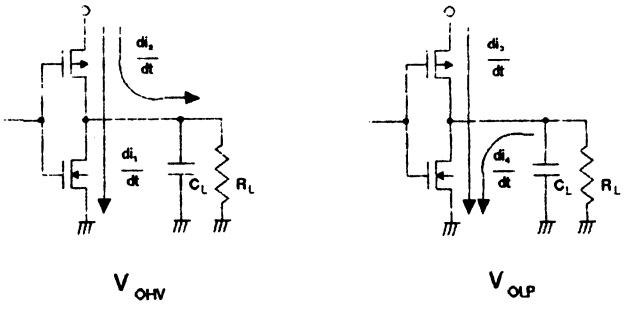
TOP VIEW



BOTTOM VIEW



As can be seen from the table, V_{OHV} has a larger value on the "L to H" transition than on the "H to L" transition. V_{OLP} has a larger value on the "H to L" transition than on the "L to H" transition. Fig. 2-5 shows the reason for this.



V_{OHV} V_{OLP}

V_{OHV} (L to H) is generated by $\frac{di1}{dt}$ and $\frac{di2}{dt}$.

V_{OHV} (H to L) is generated by $\frac{di1}{dt}$.

V_{OLP} (H to L) is generated by $\frac{di3}{dt}$ and $\frac{di4}{dt}$.

V_{OLP} (L to H) is generated by $\frac{di3}{dt}$.

Fig 2-5

2-2-2 Package Type Dependence

In its evaluation of simultaneous switching noise, Toshiba determined that this noise is package type dependent. Toshiba provides octal devices in both a Dual In-line Package (DIP) and Small Outline Integrated Circuits (SOIC). Upon evaluation of ground bounce test results, it was found that the SOIC showed a noise level that was 30% lower than that measured for the DIP. The reason for this is easy to see; because of its size, the SOIC has a substantially smaller lead frame with shorter leads. This reduces the lead inductance and the ground bounce voltage. See fig. 2-6 for a comparison of DIP to SOIC. Using the industry accepted defacto standard corner pin configuration, Toshiba can provide SOIC with very low ground bounce voltage.

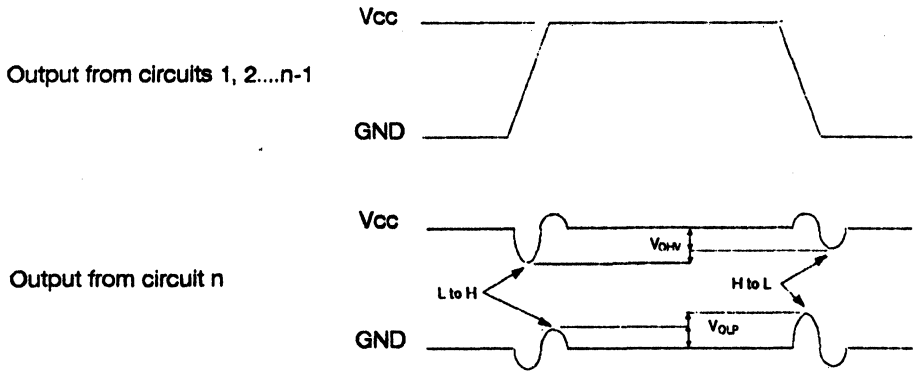


Fig. 2-4

2-2 Test Results

2-2-1 Pin Dependence

One of the critical measurements made by Toshiba is switching voltage noise based on which output is held steady. This is called "pin dependence." Table 2-1 show pin dependence simultaneous switching noise voltage for a TC74AC244P.

Switched Output Pins	Unswitched Output Pin	V_{OHV}		V_{OLP}	
		L to H	H to L	L to H	H to L
5,7,9,12,14,16,18	3	–1.33	–0.53	0.44	1.18
3,7,9,12,14,16,18	5	–1.40	–0.57	0.36	1.22
3,5,9,12,14,16,18	7	–1.33	–0.45	0.31	1.17
3,5,7,12,14,16,18	9	–1.33	–0.74	0.32	0.80
3,5,7,9,14,16,18	12	–1.46	–0.58	0.28	1.15
3,5,7,9,12,16,18	14	–1.43	–0.53	0.34	1.28
3,5,7,9,12,14,18	16	–1.39	–0.48	0.40	1.28
3,5,7,9,12,14,16	18	–1.20	–0.43	0.55	1.17

Test Conditions: V_{CC} = 5V, tr = tf = 3ns, C_L = 50pF, R_L = 500®

Table 2-1

"L to H" is the transition of the switched output pins from low (GND) to high (Vcc). The P channel FET is turned on. "H to L" is the transition of the switched output pins from high to low and the N channel FET is turned on.

The results of Toshiba's capacitance dependence tests are shown in fig. 2-7. The device tested was a TC74AC244P. The test was conducted at load capacitances of 0pF, 12pF, 50pF, 100pF and 150pF. A 100pF load capacitance (CL) will reduce ground bounce voltage when compared to a 50pF capacitance. This is due to the fact that CL acts as a filter.

2-2-4 Vendor Comparisons

In order to provide a complete study of the ground bounce situation, Toshiba evaluated several other manufacturers' ACL. The DUT in all cases was a 74AC244 DIP device. In addition, a 74F244 DIP and a Toshiba TC74HC244AP were also tested for comparison. All tests were conducted using Toshiba's multilayer test board. The test configuration in all cases was as described in paragraph 2-1-1 above. The test results are graphically shown in figs. 2-8 and 2-9.

3. Conclusions

Based on the above tests results, it appears that, with good design procedures, Toshiba's ACL will fulfill the requirements needed in today's new high speed applications. Careful design of Toshiba's TC74AC series ensures the lowest possible ground bounce. By maintaining the standard corner pin configuration, Toshiba has ensured that the customer can continue to design with tools already available.

Today, there is a trend toward SOIC. When using Toshiba's package, ground bounce can be reduced 30% over the already very low DIP simultaneous switching noise voltage level. For octal bus buffer applications, using a 100pF load capacitance will additionally reduce the ground bounce when compared to a 50pF load capacitance.

In order to keep noise at the absolute minimum, Toshiba recommends that the designer use multilayer PC boards to reduce Vcc and Ground line inductance and that a 0.1μF capacitor be placed between Vcc and Ground at every device.

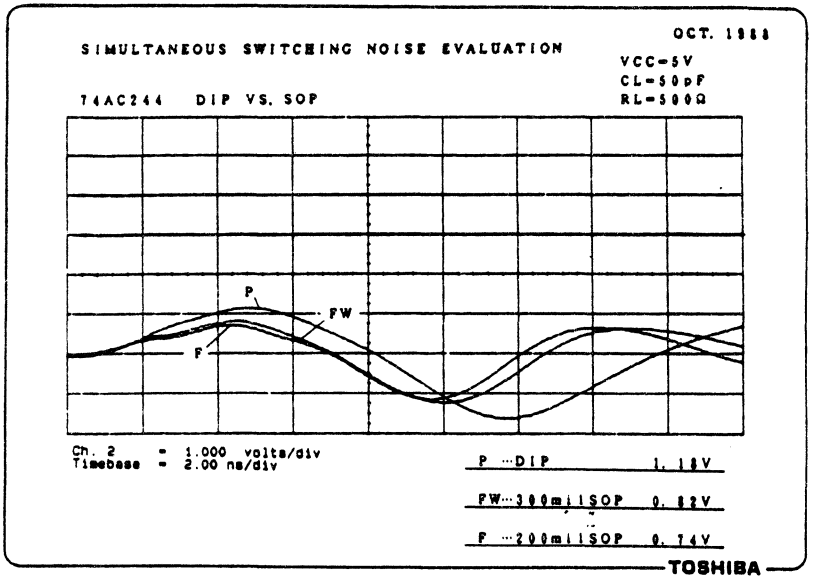


Fig. 2-6

2-2-3 Load Capacitance Dependence

Another factor which determines noise voltage value is the load capacitance C_L. As mentioned above, noise voltage can be expressed as:

$$\triangle V = L \frac{di}{dt} \quad (1)$$

$$i = C \frac{dV}{dt} \quad (2)$$

$$\therefore \triangle V = L \frac{di}{dt} = LC \frac{d^2V}{dt^2} \quad (3)$$

SIMULTANEOUS SWITCHING NOISE EVALUATION

CL Dependence

Vcc=5V Ch.1=1V/div.
tr=tf=3ns Ch.2=1V/div.
RL=500ohm Timebase=5ns/div.
SAMPLE: TC74AC244P 1pc

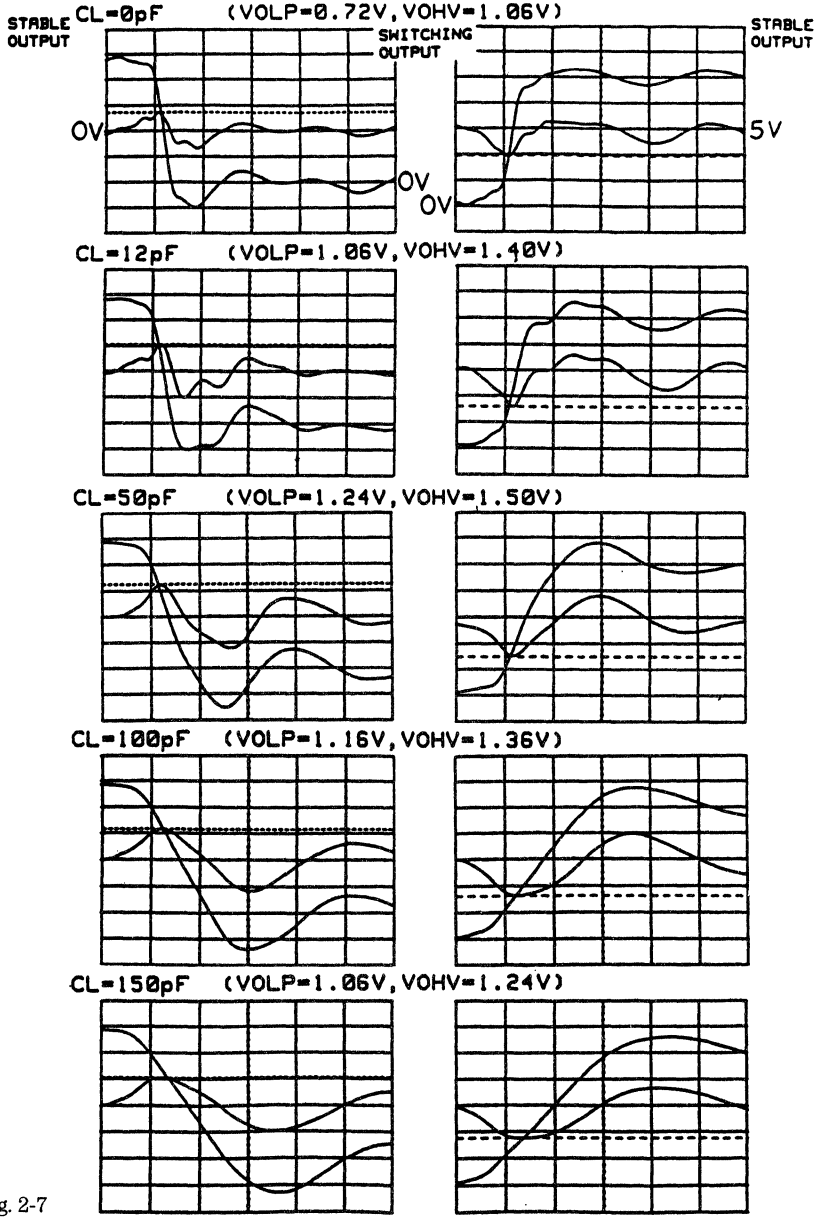


Fig. 2-7

SIMULTANEOUS SWITCHING NOISE EVALUATION

Sample Dependence

GND Bounce

CONDITION

Vcc=5V	Ch.1 = 1V/div.
tr=tf=3ns	Ch.2 = 1V/div.
CL=50pF	Timebase = 5ns/div.
RL=500ohm	

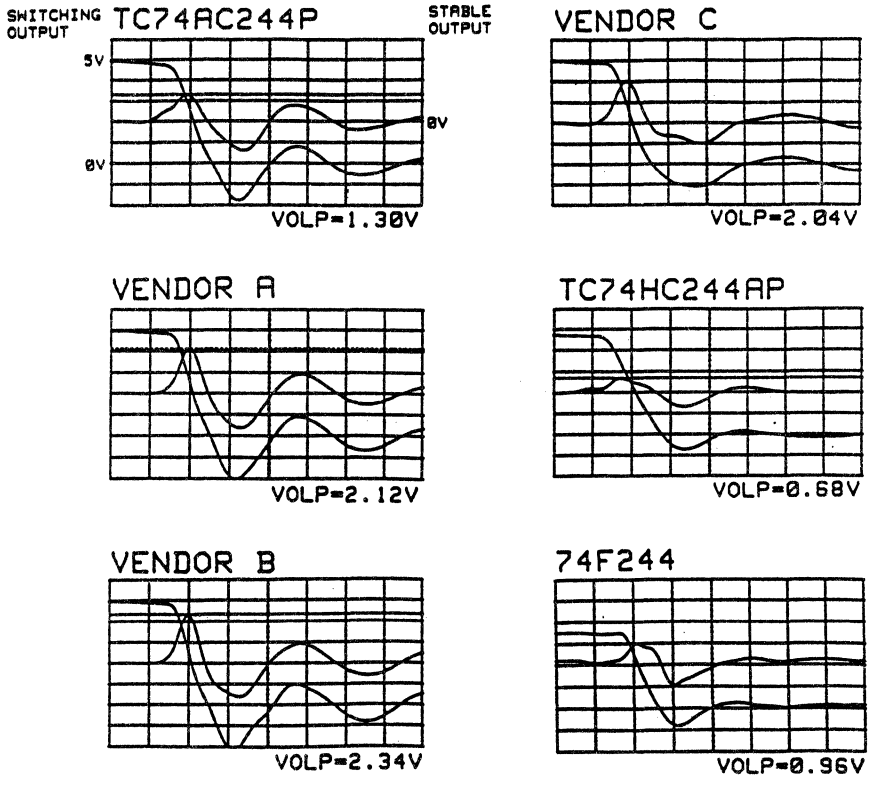


Fig. 2-8

SIMULTANEOUS SWITCHING NOISE EVALUATION

Sample Dependence

Vcc Bounce

CONDITION

Vcc=5V	Ch.1 = 1V/div.
tr=tf=3ns	Ch.2 = 1V/div.
CL=50pF	Timebase = 5ns/div.
RL=500ohm	

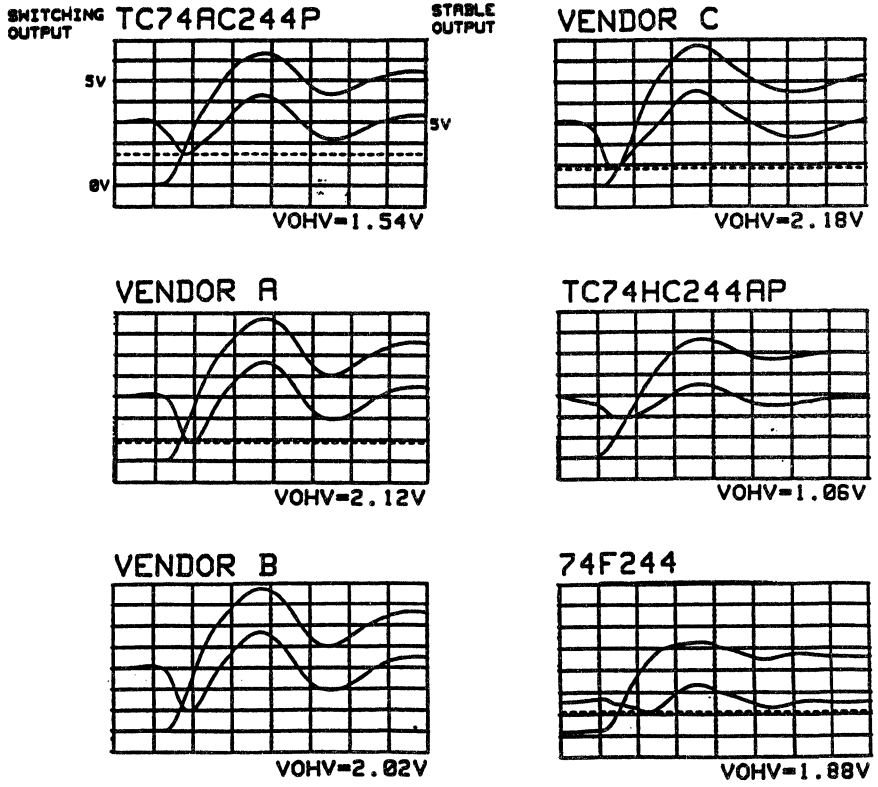


Fig. 2-9

NOTES

14. CROSS REFERENCE GUIDE

TC74AC/ACT SERIES

CROSS REFERENCE GUIDE

TOSHIBA	HARRIS	NATIONAL	MOTOROLA	HITACHI
TC74AC00	CD74AC00	74AC00	MC74AC00	HD74AC00
TC74AC02	CD74AC02	74AC02	MC74AC02	HD74AC02
TC74AC04	CD74AC04	74AC04	MC74AC04	HD74AC04
TC74AC05	CD74AC05			
TC74AC08	CD74AC08	74AC08	MC74AC08	HD74AC08
TC74AC10	CD74AC10	74AC10	MC74AC10	HD74AC10
TC74AC11		74AC11	MC74AC11	HD74AC11
TC74AC14	CD74AC14	74AC14	MC74AC14	HD74AC14
TC74AC20	CD74AC20	74AC20	MC74AC20	HD74AC20
TC74AC32	CD74AC32	74AC32	MC74AC32	HD74AC32
TC74AC74	CD74AC74	74AC74	MC74AC74	HD74AC74
TC74AC86	CD74AC86	74AC86	MC74AC86	HD74AC86
TC74AC109	CD74AC109	74AC109	MC74AC109	HD74AC109
TC74AC112	CD74AC112	74AC112		HD74AC112
TC74AC125				HD74AC125
TC74AC126				
TC74AC138	CD74AC138	74AC138	MC74AC138	HD74AC138
TC74AC139	CD74AC139	74AC139	MC74AC139	HD74AC139
TC74AC151	CD74AC151	74AC151	MC74AC151	HD74AC151
TC74AC153	CD74AC153	74AC153	MC74AC153	HD74AC153
TC74AC157	CD74AC157	74AC157	MC74AC157	HD74AC157
TC74AC158	CD74AC158	74AC158	MC74AC158	HD74AC158
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TC74AC162		74AC162	MC74AC162	
TC74AC163	CD74AC163	74AC163	MC74AC163	HD74AC163
TC74AC164	CD74AC164	74AC164		HD74AC164
TC74AC166	CD74AC166			HD74AC166
TC74AC169		74AC169	MC74AC169	HD74AC169
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TC74AC175	CD74AC175	74AC175	MC74AC175	HD74AC175
TC74AC191		74AC191	MC74AC191	
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TC74AC244	CD74AC244	74AC244	MC74AC244	HD74AC244
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TC74AC251	CD74AC251	74AC251	MC74AC251	HD74AC251
TC74AC253	CD74AC253	74AC253	MC74AC253	HD74AC253
TC74AC257	CD74AC257	74AC257	MC74AC257	HD74AC257
TC74AC258	CD74AC258	74AC258	MC74AC258	HD74AC258

CROSS REFERENCE GUIDE

TOSHIBA	HARRIS	NATIONAL	MOTOROLA	HITACHI
TC74AC259	CANCELLED			
TC74AC273	CD74AC273	74AC273	MC74AC273	HD74AC273
TC74AC280	CD74AC280			HD74AC280
TC74AC283	CD74AC283			HD74AC283
TC74AC299	CD74AC299	74AC299	MC74AC299	
TC74AC323	CD74AC323	74AC323	MC74AC323	
TC74AC367				HD74AC367
TC74AC368				HD74AC368
TC74AC373	CD74AC373	74AC373	MC74AC373	HD74AC373
TC74AC374	CD74AC374	74AC374	MC74AC374	HD74AC374
TC74AC377		74AC377	MC74AC377	HD74AC377
TC74AC390				
TC74AC393				HD74AC393
TC74AC520		74AC520	MC74AC520	
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TC74AC533	CD74AC533	74AC533	MC74AC533	
TC74AC534	CD74AC534	74AC534	MC74AC534	
TC74AC540	CD74AC540	74AC540	MC74AC540	HD74AC540
TC74AC541	CD74AC541	74AC541	MC74AC541	HD74AC541
TC74AC563	CD74AC563	74AC563	MC74AC563	
TC74AC564	CD74AC564	74AC564	MC74AC564	
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TC74AC620				
TC74AC623	CD74AC623			
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TC74AC646	CD74AC646	74AC646	MC74AC646	HD74AC646
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TC74AC670				HD74AC670
TC74AC821		74AC821		
TC74AC823		74AC823		
TC74AC825		74AC825	MC74AC825	
TC74AC841		74AC841		
TC74AC843		74AC843	MC74AC843	
TC74ACT00	CD74ACT00	74ACT00	MC74ACT00	HD74ACT00
TC74ACT02	CD74ACT02		MC74ACT02	
TC74ACT04	CD74ACT04	74ACT04	MC74ACT04	HD74ACT04
TC74ACT08	CD74ACT08	74ACT08	MC74ACT08	
TC74ACT10	CD74ACT10		MC74ACT10	

CROSS REFERENCE GUIDE

TOSHIBA	HARRIS	NATIONAL	MOTOROLA	HITACHI
TC74ACT14	CD74ACT14	74ACT14	MC74ACT14	HD74ACT14
TC74ACT32	CD74ACT32	74ACT32	MC74ACT32	
TC74ACT74	CD74ACT74	74ACT74	MC74ACT74	HD74ACT74
TC74ACT86	CD74ACT86			HD74ACT86
TC74ACT109	CD74ACT109	74ACT109	MC74ACT109	HD74ACT109
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TC74ACT138	CD74ACT138	74ACT138	MC74ACT138	HD74ACT138
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TC74ACT164	CD74ACT164			HD74ACT164
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TC74ACT541	CD74ACT541	74ACT541	MC74ACT541	HD74ACT541
TC74ACT563	CD74ACT563	74ACT563	MC74ACT563	HD74ACT563
TC74ACT564	CD74ACT564	74ACT564	MC74ACT564	HD74ACT564

CROSS REFERENCE GUIDE

TOSHIBA	HARRIS	NATIONAL	MOTOROLA	HITACHI
TC74ACT573	CD74ACT573	74ACT573	MC74ACT573	HD74ACT573
TC74ACT574	CD74ACT574	74ACT574	MC74ACT574	HD74ACT574
TC74ACT640		74ACT640	MC74ACT640	
TC74ACT646	CD74ACT646			HD74ACT646
TC74ACT648	CD74ACT648			HD74ACT648
TC74ACT821		74ACT821		
TC74ACT823		74ACT823		
TC74ACT825		74ACT825	MC74ACT825	
TC74ACT841		74ACT841		
TC74ACT843		74ACT843	MC74ACT843	

The above is provided for information only and was gathered from the latest data available. However, the accuracy of this data cannot be guaranteed and Toshiba makes no warranty as to the correctness of this information.

C²MOS LOGIC
TC74HC/HCT SERIES

INTRODUCTION

During the last several years, the scale of integration of LSI's has increased rapidly. Because of this progress, heat radiation has become a big problem, similar to the way that bipolar LSI's have been struggling for many years. It is well known that only CMOS technology can reduce this problem. The use of CMOS technology has been increasing in the field of LSI's such as high performance microprocessors and large capacity memories. Additionally, high speed CMOS devices utilizing microlithography technology have been developed as general purpose logic IC's interfacing with these high performance LSI's.

Since the introduction of the TC74HCxxx series as a high speed CMOS logic family as a new generation in 1982, TOSHIBA has produced 176 type numbers to the present time for use a variety of applications. Because the 74HC series is a CMOS design, it is susceptible to latch-up; and because of a thin gate oxide structure, electrostatic discharge (ESD) is also a problem. TOSHIBA has been working on development of CMOS devices which overcome these problems.

In response to the latch-up and ESD issues, and, as a consequence of improvements in design rules and processes, TOSHIBA has revised the TC74HCxxx series and now produces the TC74HCxxxA series. This revision has ample capacity for handling ESD as well as the elimination of latch-up in normal applications. The TC74HCxxxA series also provides an increased speed of operation of 20% to 30% over the original series. The original TC74HCxxx series will be replaced with the "A" revision series which is upward compatible. Presently, TOSHIBA produces 169 TC74HCxxxA part types and will have more than 210 part types.

This book provides technical information on TOSHIBA's TC74HCxxxA series of high speed C^2MOS devices. In addition, this book contains technical information on TC74HCxxx products for which the "A" versions are still under development.

The information contained in this data book is subject to change without notice.

February, 1990

TOSHIBA CORPORATION

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   Toshiba products described in this databook are not authorized for use as critical components in life support systems without the written consent of the appropriate officer of Toshiba America, Inc. Life support systems are either systems intended for surgical implant in the body or systems which sustain life.

   A critical component is any component of a life support system whose failure to perform may cause a malfunction or failure of the life support system, or may affect its safety or effectiveness.

3. The information in this databook has been carefully checked and is believed to be reliable, however, no responsibility can be assumed for inaccuracies that may not have been caught. All information in this databook is subject to change without prior notice. Furthermore, Toshiba cannot assume responsibility for the use of any license under the patent rights of Toshiba or any third parties.

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Type Number		Function	PIN	Page
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	652AP	OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)	24	628
TC74HC	T652AP	OCTAL BUS TRANSCEIVER / REGISTER (3-STATE)	24	634
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	688AP/AF	8-BIT EQUALITY COMPARATOR	20	645
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	690AP/AF	DECADE COUNTER REGISTER (3-STATE)	20	649
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	692AP/AF	DECADE COUNTER REGISTER (3-STATE)	20	649
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TC74HC	698P	UP / DOWN DECADE COUNTER / REGISTER (3-STATE)	20	672
	699P	UP / DOWN 4-BIT BINARY COUNTER / REGISTER (3-STATE)	20	672
	4002AP/AF	DUAL 4-INPUT NOR GATE	14	684
	4016AP/AF	QUAD BILATERAL SWITCH	14	*
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	4020AP/AF/AFN	14-STAGE BINARY COUNTER	16	693
	4022AP/AF	OCTAL COUNTER / DIVIDER	16	698
	4024AP/AF	7-STAGE BINARY COUNTER	14	702
	4028AP/AF	BCD TO DECIMAL DECODER	16	706
	4040AP/AF/AFN	12-STAGE BINARY COUNTER	16	693
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	4050AP/AF/AFN	HEX BUFFER	16	710
	4051AP/AF	8-CHANNEL ANALOG MULTIPLEXER	16	714
	4052AP/AF	DUAL 4-CHANNEL ANALOG MULTIPLEXER	16	714
	4053AP/AF/AFN	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	16	714
	4060AP/AF	14-STAGE BINARY COUNTER / OSCILLATOR	16	721
	4066AP/AF/AFN	QUAD BILATERAL SWITCH	14	726
	4072AP/AF	DUAL 4-INPUT OR GATE	14	730
	4075AP/AF	TRIPLE 3-INPUT OR GATE	14	733
	4078AP/AF	8-INPUT OR / NOR GATE	14	736
TC74HC	4094AP/AF/AFN	8-BIT SIPO SHIFT REGISTER / LATCH (3-STATE)	16	739
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	40103P	8-BIT BINARY PROGRAMMABLE DOWN COUNTER	16	745
	40105AP/AF	4-BIT x 16-WORD FIFO REGISTER	16	756
	4316AP/AF	QUAD BILATERAL SWITCH	16	*
	4351AP/AF	8-CHANNEL ANALOG MULTIPLEXER	20	*
	4352AP/AF	DUAL 4-CHANNEL ANALOG MULTIPLEXER	20	*
	4353AP/AF	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	20	*
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Type Number	Function	PIN	Page
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4538AP/AF/AFN	DUAL MONOSTABLE MULTIVIBRATOR	16	781
4543AP/AF	BCD TO 7 SEGMENT LATCH / DECODER / DRIVER	16	789
T7007AP/AF	HEX BUFFER	14	794
7240AP/AF	OCTAL BUS BUFFER (3-STATE / INVERTED)	20	797
7241AP/AF	OCTAL BUS BUFFER (3-STATE)	20	797
7244AP/AF	OCTAL BUS BUFFER (3-STATE)	20	797
7266AP/AF	QUAD EXCLUSIVE NOR GATE	14	458
TC74HC 7292P	PROGRAMMABLE DIVIDER / TIMER	16	801
7294P	PROGRAMMABLE DIVIDER / TIMER	16	801
7640AP/AF	OCTAL BUS TRANSCEIVER (3-STATE / INVERTED)	20	*
7643AP/AF	OCTAL BUS TRANSCEIVER (3-STATE)	20	*
7645AP/AF	OCTAL BUS TRANSCEIVER (3-STATE)	20	*

- All 24pin DIP products are provided in the 300mil narrow package.
- * denotes products under development.

CHANGE-OVER TO THE NEW ENHANCED VERSION PHASE II

Since 1982 TOSHIBA has been producing 176 types of TC74HCxxx series, which are well accepted in the world-wide market place.

In 1987, applying enhanced design and process technology, TOSHIBA developed the "A" version of that series.

The new enhanced TC74HCxxxA series offers higher AC performance, ESDS, reliability, and so on, while maintaining the compatibility with the old version and JEDEC standard specification.

TOSHIBA recommends customers replace the TC74HCxxx series with the new TC74HCxxxA series.

By the end of March, 1989, we have successfully changed-over the first group of 100 part numbers.

The second group, 32 types are listed in the table below, are projected to be discontinued by the end of March, 1990.

TOSHIBA would like customers to consider those enhanced types and cooperate in the change-over from the old version.

TOSHIBA believes that the new, enhanced version will contribute to the achievement of better performance of the final equipment.

DISCONTINUED TYPE LIST [Ph-II]

TYPE NAME	FUNCTION	REPLACEMENT
TC74HC 30P/F	8-INPUT NAND GATE	TC74HC 30AP/AF/AFN
86P/F	QUAD EXCLUCIVE OR GATE	86AP/AF/AFN
107P/F	DUAL J-K FLIP-FLOP WITH CLEAR	107AP/AF/AFN
113P/F	DUAL J-K FLIP-FLOP WITH PRESET	113AP/AF
153P/F	DUAL 4-CHANNEL MULTIPLEXER	153AP/AF/AFN
173P/F	QUAD D-TYPE REGISTER (3-STATE)	173AP/AF
192P/F	SYNC. UP / DOWN DECADE COUNTER	192AP/AF
193P/F	SYNC. UP / DOWN BINARY COUNTER	193AP/AF/AFN
194P/F	4-BIT PIPO SHIFT REGISTER	194AP/AF
195P/F	4-BIT PIPO SHIFT REGISTER	195AP/AF
TC74HC 237P/F	3-TO-8 LINE DECODER / LATCH	TC74HC 237AP/AF
253P/F	DUAL 4-CH MULTIPLEXER (3-STATE)	253AP/AF/AFN
259P/F	8-BIT ADDRESSABLE LATCH	259AP/AF/AFN
279P/F	QUAD $\overline{S}$-$\overline{R}$ LATCH	279AP/AF
354P/F	8-CHANNEL MULTIPLEXER / REGISTER	354AP/AF
356P/F	8-CHANNEL MULTIPLEXER / REGISTER	356AP/AF
365P/F	HEX BUS BUFFER (3-STATE)	365AP/AF
366P/F	HEX BUS BUFFER (3-STATE / INV.)	366AP/AF
377P/F	OCTAL D-TYPE FLIP-FLOP	377AP/AF
4020P/F	14-STAGE BINARY COUNTER	4020AP/AF/AFN
TC74HC 4040P/F	12-STAGE BINARY COUNTER	TC74HC 4040AP/AF/AFN
4049P/F	HEX BUFFER (INV.)	4049AP/AF/AFN
4050P/F	HEX BUFFER	4050AP/AF/AFN
4060P/F	14-STAGE BINARY COUNTER/OSCILATOR	4060AP/AF
4066P/F	QUAD BILATERAL SWITCH	4066AP/AF/AFN
4072P/F	DUAL 4-INPUT OR GATE	4072AP/AF
4078P/F	8-INPUT OR / NOR GATE	4078AP/AF
4094P/F	8-BIT SIPO SHIFT REGISTER / LATCH	4094AP/AF/AFN
4514P	4-TO-16 LINE DECODER / LATCH	4514AP
4515P	4-TO-16 LINE DECODER / LATCH (INV.)	4515AP
TC74HC 4538P/F	DUAL MONOSTABLE MULTIVIBRATOR	TC74HC 4538AP/AF/AFN
4543P/F	BCD TO 7 SEG. LATCH/DECODER/DRIVER	4543AP/AF

DISCONTINUED TYPE LIST [Ph- I] 1989 March.~

TYPE NAME	FUNCTION	REPLACEMENT
TC74HC 00P/F	QUAD 2-INPUT NAND GATE	TC74HC 00AP/AF/AFN
02P/F	QUAD 2-INPUT NOR GATE	02AP/AF/AFN
03P/F	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	03AP/AF/AFN
04P/F	HEX INVERTER	04AP/AF/AFN
T04P/F	HEX INVERTER	T04AP/AF/AFN
U04P/F	HEX INVERTER	U04AP/AF/AFN
08P/F	QUAD 2-INPUT AND GATE	08AP/AF/AFN
10P/F	TRIPPLE 3-INPUT NAND GATE	10AP/AF/AFN
11P/F	TRIPPLE 3-INPUT AND GATE	11AP/AF/AFN
14P/F	HEX SCHMITT INVERTER	14AP/AF/AFN
TC74HC 20P/F	DUAL 4-INPUT NAND GATE	TC74HC 20AP/AF/AFN
21P/F	DUAL 4-INPUT AND GATE	21AP/AF/AFN
27P/F	TRIPPLE 3-INPUT NOR GATE	27AP/AF/AFN
32P/F	QUAD 2-INPUT OR GATE	32AP/AF/AFN
42P/F	BCD TO DECIMAL DECODER	42AP/AF/AFN
51P/F	DUAL 2W-2I AND / OR INVERT GATE	51AP/AF/AFN
73P/F	DUAL J-K FLIP-FLOP WITH CLEAR	73AP/AF
74P/F	DUAL D FLIP-FLOP WITH PRESET AND CLEAR	74AP/AF/AFN
75P/F	4-BIT D-TYPE LATCH	75AP/AF
76P/F	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	76AP/AF
TC74HC 77P/F	4-BIT D-TYPE LATCH	TC74HC 77AP/AF
85P/F	4-BIT MAGNITUDE COMPARATOR	85AP/AF/AFN
109P/F	DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR	109AP/AF/AFN
125P/F	QUAD BUS BUFFER (3-STATE)	125AP/AF/AFN
126P/F	QUAD BUS BUFFER (3-STATE)	126AP/AF
131P/F	3-TO-8 LINE DECODER / LATCH	131AP/AF
132P/F	QUAD 2-INPUT SCHMITT NAND	132AP/AF/AFN
133P/F	13-INPUT NAND GATE	133AP/AF
137P/F	3-TO-8 LINE DECODER / LATCH	137AP/AF
138P/F	3-TO-8 LINE DECODER	138AP/AF/AFN
TC74HC T138P/F	3-TO-8 LINE DECODER	TC74HCT 138AP/AF/AFN
139P/F	DUAL 2-TO4 LINE DECODER	139AP/AF/AFN
151P/F	8-CHANNEL MULTIPLEXER	151AP/AF/AFN
154P	4-TO-16 LINE DECODER	154AP
155P/F	DUAL 2-TO-4 LINE DECODER	155AP/AF/AFN
157P/F	QUAD 2-CHANNEL MULTIPLEXER	157AP/AF/AFN
158P/F	QUAD 2-CHANNEL MULTIPLEXER (INV.)	158AP/AF/AFN
160P/F	SYNC. DECADE COUNTER WITH ASYNC, CLEAR	160AP/AF
161P/F	SYNC. BINARY COUNTER WITH ASYNC, CLEAR	161AP/AF/AFN
162P	SYNC. DECADE COUNTER WITH SYNC, CLEAR	162AP/AF
TC74HC 163P/F	SYNC. BINARY COUNTER WITH SYNC, CLEAR	TC74HC 163AP/AF/AFN
164P/F	8-BIT SIPO SHIFT REGISTER	164AP/AF/AFN
165P/F	8-BIT PISO SHIFT REGISTER	165AP/AF/AFN
166P/F	8-BIT PISO SHIFT REGISTER	166AP/AF/AFN
174P/F	HEX D FLIP-FLOP WITH CLEAR	174AP/AF/AFN
175P/F	QUAD D FLIP-FLOP WITH CLEAR	175AP/AF/AFN
238P/F	3-TO-8 LINE DECODER	238AP/AF
240P/F	OCTAL BUS BUFFER (3-STATE / INV.)	240AP/AF/AFW
T240P	OCTAL BUS BUFFER (3-STATE / INV.)	T240AP/AF/AFW
241P/F	OCTAL BUS BUFFER (3-STATE)	241AP/AF

DISCONTINUED TYPE LIST [Ph- I] 1989 March.~

TYPE NAME	FUNCTION	REPLACEMENT
TC74HC T241P/F	OCTAL BUS BUFFER (3-STATE)	TC74HC T241AP/AF
244P/F	OCTAL BUS BUFFER (3-STATE)	244AP/AF/AFW
T244P/F	OCTAL BUS BUFFER (3-STATE	T244AP/AF/AFW
245P/F	OCTAL BUS TRANSCEIVER (3-STATE)	245AP/AF/AFW
T245P/F	OCTAL BUS TRANSCEIVER (3-STATE)	T245AP/AF/AFW
251P/F	8-CHANNEL MULTIPLEXER (3-STATE)	251AP/AF
257P/F	QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	257AP/AF/AFN
258P/F	QUAD 2-CHANNEL MULTIPLEXER (3-STATE / INV.)	258AP/AF
273P/F	OCTAL D FLIP-FLOP WITH CLEAR	273AP/AF
280P/F	9-BIT PARITY GENERATOR / CHECKER	280AP/AF
TC74HC 283P/F	4-BIT BINARY FULL ADDER	TC74HC 283AP/AF/AFN
298P/F	QUAD 2-CHANNEL MULTIPLEXER / REGISTER	298AP/AF
299P	8-BIT PIPO SHIFT REGISTER	299AP/AF
323P	8-BIT PIPO SHIFT REGISTER	323AP/AF
367P/F	HEX BUS BUFFER (3-STATE)	367AP/AF/AFN
368P/F	HEX BUS BUFFER (3-STATE / INV.)	368AP/AF/AFN
373P/F	OCTAL D-TYPE LATCH (3-STATE)	373AP/AF/AFW
374P/F	OCTAL D FLIP-FLOP (3-STATE)	374AP/AF/AFW
T374P/F	OCTAL D FLIP-FLOP (3-STATE)	T374AP/AF/AFW
375P/F	QUAD D-TYPE LATCH	375AP/AF
TC74HC 386P/F	QUAD EXCLUSIVE OR GATE	TC74HC 386AP/AF
390P/F	DUAL DECADE COUNTER	390AP/AF/AFN
393P/F	DUAL BINARY COUNTER	393AP/AF/AFN
533P/F	OCTAL D-TYPE LATCH (3-STATE / INV.)	533AP/AF
534P/F	OCTAL D FLIP-FLOP (3-STATE / INV.)	534AP/AF
540P/F	OCTAL BUS BUFFER (3-STATE / INV.)	540AP/AF/AFW
541P/F	OCTAL BUS BUFFER (3-STATE)	541AP/AF/AFW
563P/F	OCTAL D-TYPE LATCH (3-STATE / INV.)	563AP/AF
564P/F	OCTAL D FLIP-FLOP (3-STATE / INV.)	564AP/AF
573P/F	OCTAL D-TYPE LATCH (3-STATE)	573AP/AF/AFW
TC74HC 574P/F	OCTAL D FLIP-FLOP (3-STATE)	TC74HC 574AP/AF
595P	8-BIT SHIFT REGISTER /LATCH (3-STATE)	595AP/AF/AFN
597P/F	8-BIT LATCH / SHIFT REGISTER	597AP/AF
640P/F	OCTAL BUS TRANSCEIVER (3-STATE / INV.)	640AP/AF
T640P/F	OCTAL BUS TRANSCEIVER (3-STATE / INV.)	T640AP/AF
643P/F	OCTAL BUS TRANSCEIVER (3-STATE)	643AP/AF
T643P/F	OCTAL BUS TRANSCEIVER (3-STATE)	T643AP/AF
646P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE)	646AP
T646P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE)	T646AP
648P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE / INV.)	648AP
TC74HC T648P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE / INV.)	TC74HC T648AP
651P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE / INV.)	651AP
T651P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE / INV.)	T651AP
652P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE)	652AP
T652P	OCTAL BUS TRANSCEIVER /REGISTER (3-STATE)	T652AP
688P/F	8-BIT EQUARITY COMPARATOR	688AP/AF
4002P/F	DUAL 4-INPUT NOR GATE	4002AP/AF
4075P/F	TRIPLE 3-INPUT OR GATE	4075AP/AF
T7007P/F	HEX BUFFER	T7007AP/AF
7266P/F	QUAD EXCLUSIVE NOR GATE	7266AP/AF

2. HIGH SPEED CMOS SELECTION GUIDE

GATE	NAND	HC00A HCT00A HC03A HC10A HC20A HC30A HC132A HC133A
	NOR	HC02A HCT02A HC27A HC4002A HC4078A
	AND	HC08A HCT08A HC09A HC11A HC21A
	OR	HC32A HCT32A HC4072A HC4075A HC4078A
	INVERTER, BUFFER	HC04A HCT04A HCU04A HC05A HC07A HC14A HC4049A HC4050A HCT7007A
	EXCLUCIVE OR / NOR	HC86A HCT86A HC266A HC386A HC7266A
	SCHIMITT TRIGGER	HC14A HC132A
	MULTI FUNCTION	HC51A
	LEVEL SHIFTER	HC4049A HC4050A
	BUS BUFFER	HC125A HC126A HC240A HCT240A HC241A HCT241A HC244A HCT244A HC365A HC366A HC367A HC368A HC540A HCT540A HC541A HCT541A HC7240A HC7241A HC7244A
	BUS TRANSCEIVER	HC242A HC243A HC245A HCT245A HC620A HC623A HC640A HCT640A HC643A HCT643A HC646A HCT646A HC648A HCT648A HC651A HCT651A HC652A HCT652A HC7640A HC7643A HC7645A
FLIP-FLOP	J-K FLIP-FLOP	HC73A HC76A HC107A HC109A HC112 HC113A
	D FLIP-FLOP	HC74A HCT74A HC174A HCT174A HC175A HC273A HCT273A HC377A
	3-STATE	HC374A HCT374A HC534A HCT534A HC564A HCT564 HC574A HCT574 HC646A HCT646A HC648A HCT648A HC651A HCT651A HC652A HCT652A
LATCH		HC75A HC77A HC259A HC279A HC375A
	3-STATE	HC373A HCT373A HC533A HCT533A HC563A HCT563 HC573A HCT573
MULTI VIBRATOR		HC4538A HC123A HC221A HC423A
DECODER		HC42A HC131A HC137A HCT137 HC138A HCT138A HC139A HC154A HC155A HC237A HC238A HC4028A HC4514A HC4515A
	7-SEGMENT	HC4511A HC4543A
ENCODER		HC147A HC148A
REGISTER		HC164A HCT164A HC165A HC166A HC173A HC194A HC195A HC299A HC323A HC595A HC597A HC4094A HC670A HC40105A
COUNTER	BINARY	HC161A HC163A HC191A HC193A HC393A HC590A HC592 HC593A HC691 HC693 HC697 HC699 HC4520
	DECADE	HC160A HC162A HC190A HC192A HC390A HC690 HC692 HC696 HC698 HC4518
	DIVIDER	HC4017 HC4020A HC4022 HC4024A HC4040A HC4060A HC40102 HC40103 HC7292 HC7294
MULTIPLEXER	ANALOG	HC4051A HC4052A HC4053A HC4351A HC4352A HC4353A
	DIGITAL	HC151A HC153A HC157A HCT157A HC158A HCT158A HC251A HC253A HC257A HCT257A HC258A HCT258A HC298A HC352A HC353A HC354A HC356A
ANALOG SWITCH		HC4016A HC4066A HC4316A
COMPARATOR		HC85A HC688A HCT688A
ADDER		HC283A
ALU		HC181 HC182A
PARITY TREE		HC283A

Including under development type number

GATE

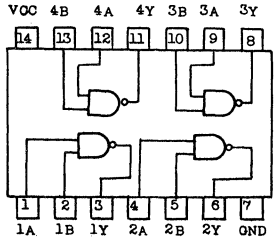
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 00	QUAD 2-INPUT NAND GATE	LS00	4011, 7400	14
74HC T00	QUAD 2-INPUT NAND GATE	LS00	4011, 7400	14
74HC 03	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	LS03	*40107,*5029	14
74HC 10	TRIPLE 3-INPUT NAND GATE	LS10	4023	14
74HC 20	DUAL 4-INPUT NAND GATE	LS20	4012	14
74HC 30	8-INPUT NAND GATE	LS30	4068	14
74HC 133	13-INPUT NAND GATE	LS133		16
74HC 02	QUAD 2-INPUT NOR GATE	LS02	4001	14
74HC T02	QUAD 2-INPUT NOR GATE	LS02	4001	14
74HC 27	TRIPLE 3-INPUT NOR GATE	LS27	4025,*4000	14
74HC4002	DUAL 4-INPUT NOR GATE	*LS25	4002	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 08	QUAD 2-INPUT AND GATE	LS08	4081	14
74HC T08	QUAD 2-INPUT AND GATE	LS08	4081	14
74HC 09	QUAD 2-INPUT AND GATE (OPEN DRAIN)	LS09	4081	14
74HC 11	TRIPLE 3-INPUT AND GATE	LS11	4073	14
74HC 21	DUAL 4-INPUT AND GATE	LS21	4082	14
74HC 32	QUAD 2-INPUT OR GATE	LS32	4071	14
74HC 32	QUAD 2-INPUT OR GATE	LS32	4071	14
74HC4075	TRIPLE 3-INPUT OR GATE		4075	14
74HC4072	DUAL 4-INPUT OR GATE		4072	14
74HC4078	8-INPUT OR/NOR GATE		4078	14
74HC 04	HEX INVERTER	LS04	*4069U	14
74HC T04	HEX INVERTER	LS04	*4069U	14
74HC U04	HEX INVERTER (SINGLE STAGE)	*LS04	4069U,7404U	14
74HC 05	HEX INVERTER (OPEN DRAIN)	*LS04	*4069U	14
74HC 51	DUAL 2W-2I AND/OR INVERT GATE	LS51	*4085	14
74HC 86	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC T86	QUAD EXCLUSIVE OR GATE	LS88,LS386	4030	14
74HC 266	QUAD EXCLUSIVE NOR GATE (OPEN DRAIN)	LS266	4077	14
74HC7266	QUAD EXCLUSIVE NOR GATE	*LS266	4077	14
74HC 386	QUAD EXCLUSIVE OR GATE	LS86,LS386	4030	14
74HC 14	HEX SCHMITT INVERTER	LS14	4584	14
74HC 132	QUAD 2-INPUT SCHMITT NAND	LS132	4093	14

* Suggested alternative

GATE

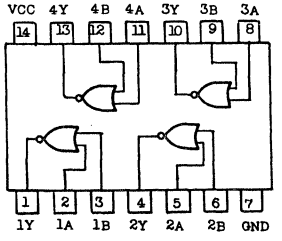
QUAD 2-INPUT NAND GATE

00
T00 Positive logic : $Y = \overline{AB}$



QUAD 2-INPUT NOR GATE

02
T02 Positive logic : $Y = \overline{A+B}$

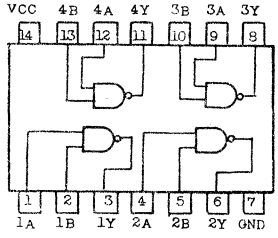


GATE (Continued)

QUAD 2-INPUT NAND GATE WITH OPEN DRAIN OUTPUT

03

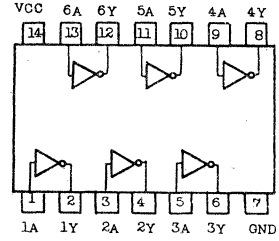
Positive logic: $Y = \overline{AB}$



HEX INVERTER

04 05
T04
U04

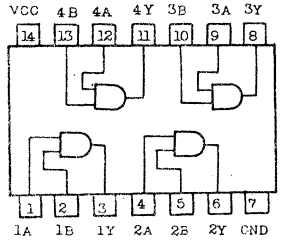
Positive logic: $Y = \overline{A}$



QUAD 2-INPUT AND GATE

08 09
T08

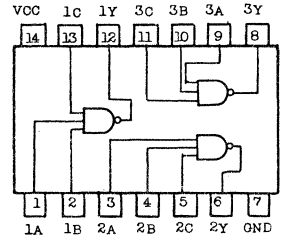
Positive logic: $Y = AB$



TRIPLE 3-INPUT NAND GATE

10

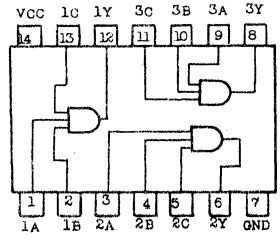
Positive logic: $Y = \overline{ABC}$



TRIPLE 3-INPUT AND GATE

11

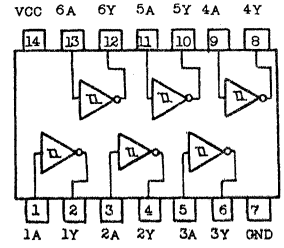
Positive logic: $Y = ABC$



HEX SCHMITT INVERTER

14

Positive logic: $Y = \overline{A}$

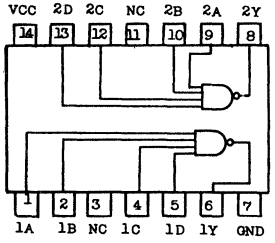


GATE (Continued)

DUAL 4-INPUT NAND GATE

20

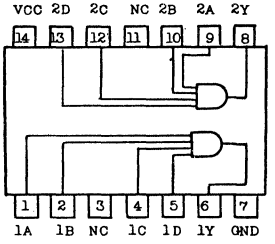
Positive logic; $Y = \overline{ABCD}$



DUAL 4-INPUT AND GATE

21

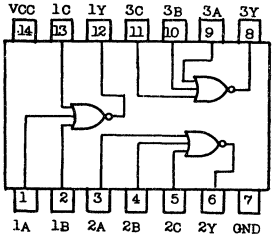
Positive logic: $Y = ABCD$



TRIPLE 3-INPUT NOR GATE

27

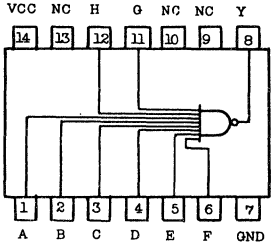
Positive logic: $Y = \overline{A+B+C}$



8-INPUT NAND GATE

30

Positive logic: $Y = \overline{ABCDEFGH}$

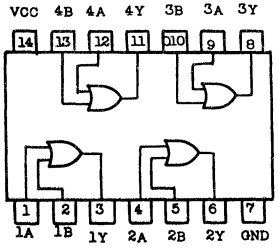


QUAD 2-INPUT OR GATE

32

T32

Positive logic: $Y = A+B$

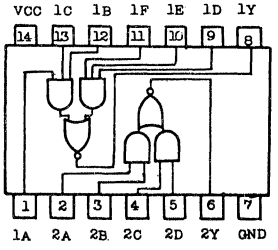


DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

51

Positive logic: $1Y=\overline{1A \cdot 1B \cdot 1C+1D \cdot 1E \cdot 1F}$

$2Y=\overline{2A \cdot 2B+2C \cdot 2D}$

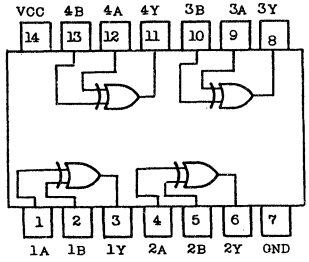


GATE (Continued)

QUAD 2-INPUT EXCLUSIVE-OR GATE

86
T86

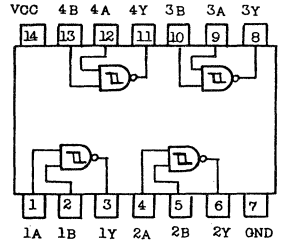
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



QUAD 2-INPUT SCHMITT NAND GATE

132

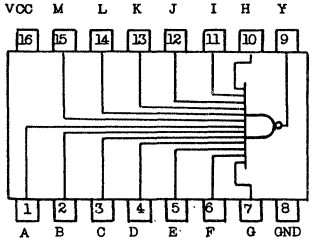
Positive logic: $Y = \overline{AB}$



13-INPUT NAND GATE

133

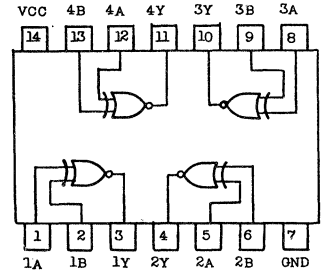
Positive logic: $Y=\overline{ABCDEFGHIJKLM}$



QUAD 2-INPUT EXCLUSIVE-NOR GATE

266
7266

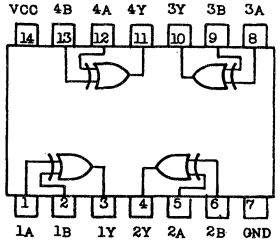
Positive logic: $Y=\overline{A\oplus B}=AB+\overline{A}\overline{B}$



QUAD 2-INPUT EXCLUSIVE-OR GATE

386

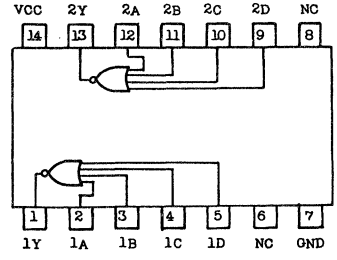
Positive logic: $Y=A\oplus B=\overline{A}B+A\overline{B}$



DUAL 4-INPUT NOR GATE

4002

Positive logic: $Y=\overline{A+B+C+D}$

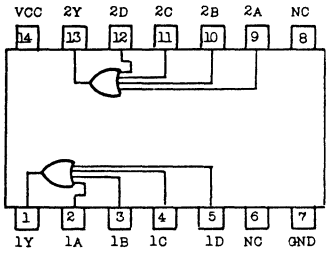


GATE (Continued)

DUAL 4-INPUT OR GATE

4072

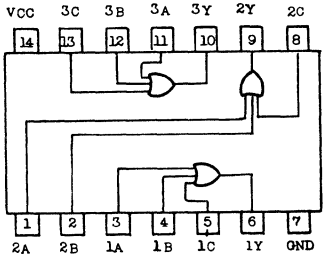
Positive logic: Y=A+B+C+D



TRIPLE 3-INPUT OR GATE

4075

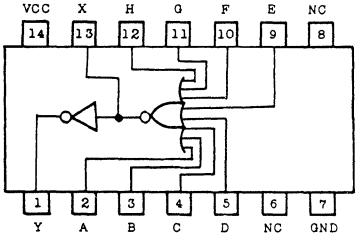
Positive logic: Y=A+B+C



8-INPUT NOR GATE

4078

Positive logic: Y=A+B+C+D+E+F+G+H



BUFFER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 07	HEX BUFFER	LS07		14
74HCT7007	HEX BUFFER	*LS07		14
74HC4049	HEX BUFFER (INVERTING)		4049	16
74HC4050	HEX BUFFER		4050	16
74HC 125	QUAD BUS BUFFER	LS125	5024	14
74HC 126	QUAD BUS BUFFER	LS126	5025	14
74HC 240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HCT240	OCTAL BUS BUFFER (INVERTING)	LS240		20
74HC 241	OCTAL BUS BUFFER	LS241		20
74HCT241	OCTAL BUS BUFFER	LS241		20
74HC 244	OCTAL BUS BUFFER	LS244		20
74HCT244	OCTAL BUS BUFFER	LS244		20
74HC 365	HEX BUS BUFFER	LS365A		16
74HC 366	HEX BUS BUFFER (INVERTING)	LS366A		16
74HC 367	HEX BUS BUFFER	LS367A	5012	16
74HC 368	HEX BUS BUFFER (INVERTING)	LS368A		16
74HC 540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HCT540	OCTAL BUS BUFFER (INVERTING)	LS540		20
74HC 541	OCTAL BUS BUFFER	LS541		20
74HCT541	OCTAL BUS BUFFER	LS541		20
74HC7240	OCTAL BUS BUFFER (SCHMITT IN)	LS240		20
74HC7241	OCTAL BUS BUFFER (SCHMITT IN)	LS241		20
74HC7244	OCTAL BUS BUFFER (SCHMITT IN)	LS244		20
74HC 242	QUAD BUS TRANSCEIVER (INVERTING)	LS242		14
74HC 243	QUAD BUS TRANSCEIVER	LS243		14
74HC 245	OCTAL BUS TRANSCEIVER	LS245		20
74HCT245	OCTAL BUS TRANSCEIVER	LS245		20
74HC 620	OCTAL BUS TRANSCEIVER (INVERTING)	LS620		20
74HC 623	OCTAL BUS TRANSCEIVER	LS623		20
74HC 640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HCT640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HC 643	OCTAL BUS TRANSCEIVER	LS643		20
74HCT643	OCTAL BUS TRANSCEIVER	LS643		20
74HC7640	OCTAL BUS TRANSCEIVER (INVERTING)	LS640		20
74HC7643	OCTAL BUS TRANSCEIVER	LS643		20
74HC7645	OCTAL BUS TRANSCEIVER	LS245		20

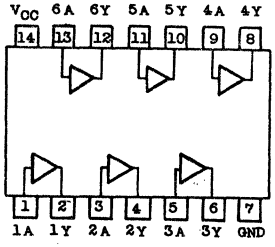
* Suggested alternative

BUFFER

HEX BUFFER

07
T7007

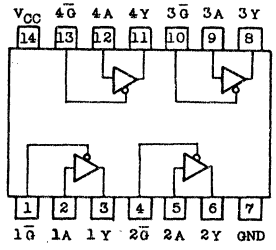
Positive logic : Y = A



QUAD BUS BUFFER

125

Positive logic : Y = A

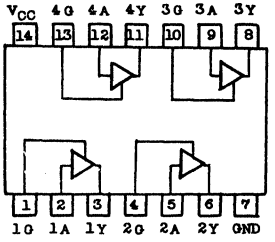


BUFFER (Continued)

QUAD BUS BUFFER

126

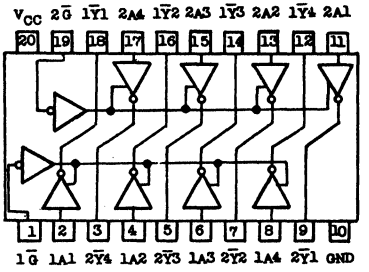
Positive logic: Y = A



OCTAL BUS BUFFER (INVERTING)

240

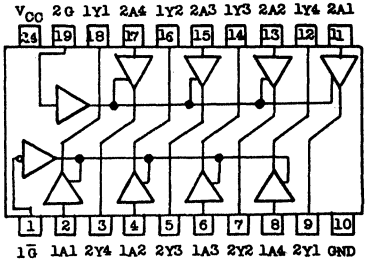
T240



OCTAL BUS BUFFER

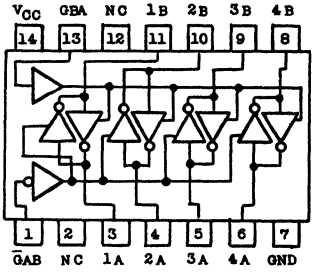
241

T241



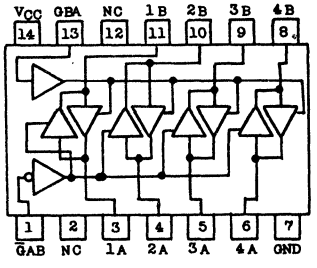
QUAD BUS TRANSCEIVER (INVERTING)

242



QUAD BUS TRANSCEIVER

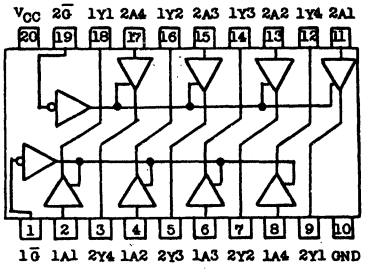
243



OCTAL BUS BUFFER

244

T244

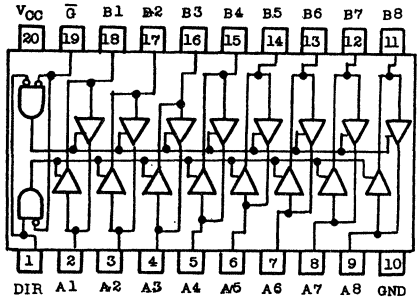


BUFFER (Continued)

OCTAL BUS TRANSCEIVER

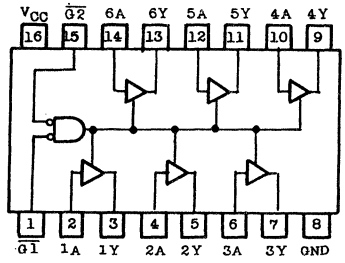
245

T245



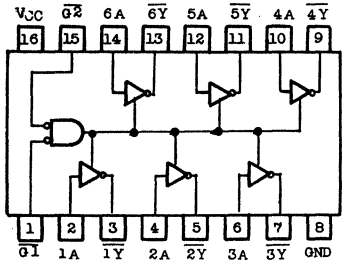
HEX BUS BUFFER

365



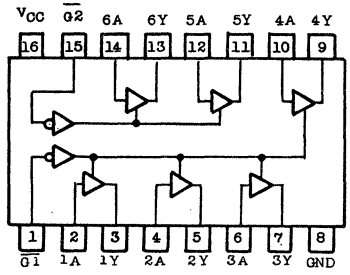
HEX BUS BUFFER (INVERTING)

366



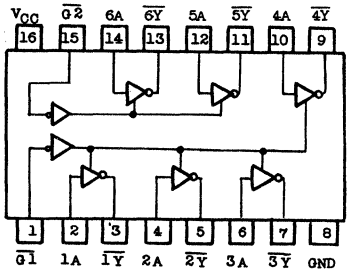
HEX BUS BUFFER

367



HEX BUS BUFFER (INVERTING)

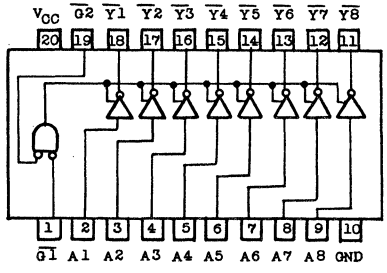
368



OCTAL BUS BUFFER (INVERTING)

540

T540

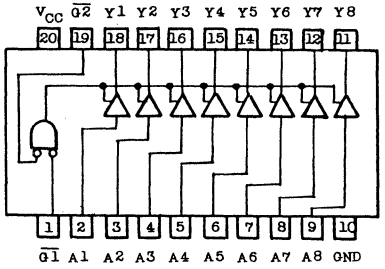


BUFFER (Continued)

OCTAL BUS BUFFER

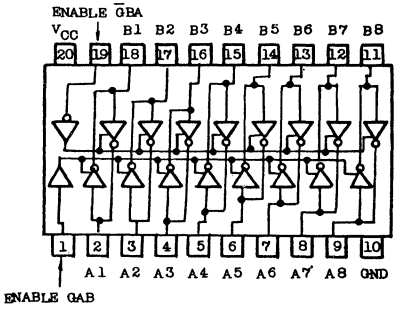
541

T541



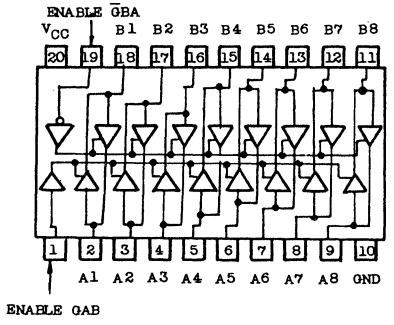
OCTAL BUS TRANSCEIVER (INVERTING)

620



OCTAL BUS TRANSCEIVER

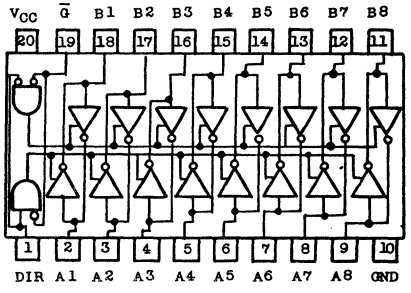
623



OCTAL BUS TRANSCEIVER (INVERTING)

640

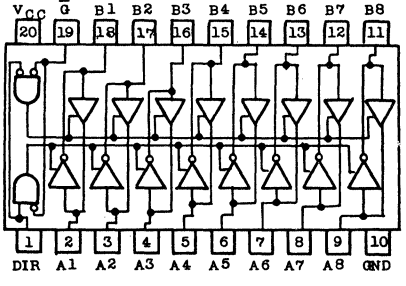
T640



OCTAL BUS TRANSCEIVER

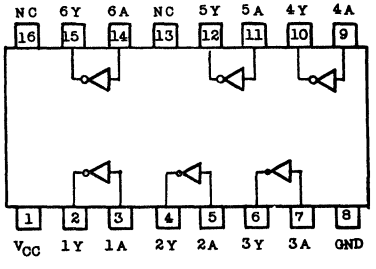
643

T643



HEX BUFFER/CONVERTER (INVERTING)

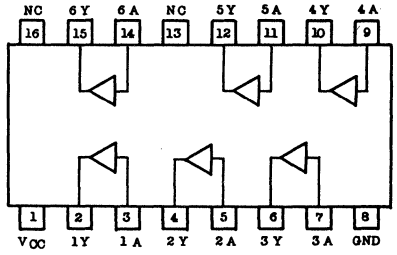
4049



BUFFER (Continued)

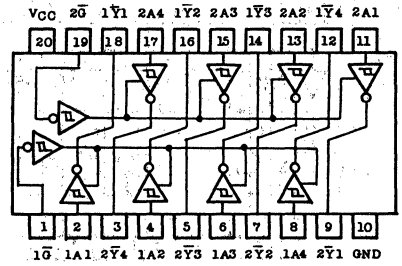
HEX BUFFER/CONVERTER

4050



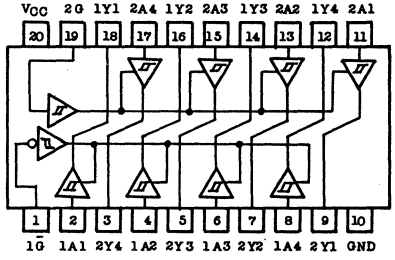
OCTAL BUS BUFFER (INVERTING)

7240



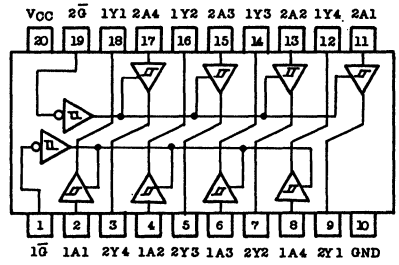
OCTAL BUS BUFFER

7241



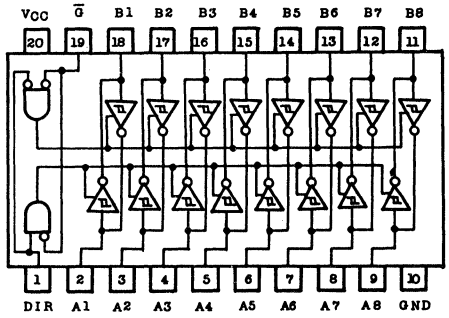
OCTAL BUS BUFFER

7244



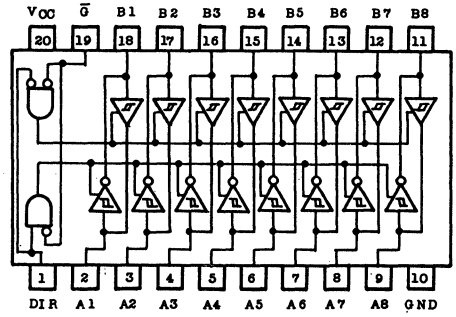
OCTAL BUS TRANSCEIVER (INVERTING)

7640



OCTAL BUS TRANSCEIVER

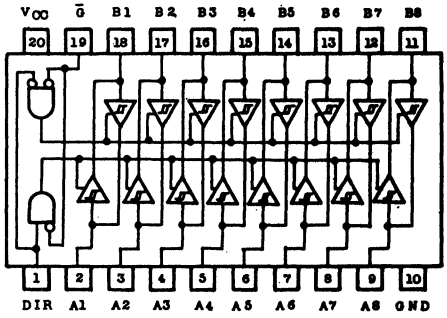
7643



BUFFER (Continued)

OCTAL BUS TRANSCEIVER

7645



FLIP-FLOP

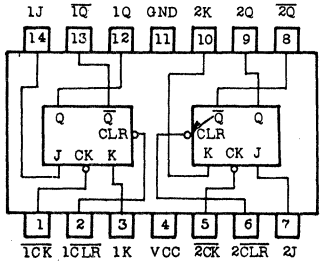
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 73	DUAL J-K FLIP-FLOP WITH CLEAR	LS73A,LS107A		14
74HC 76	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 107	DUAL J-K FLIP-FLOP WITH CLEAR	LS107A,LS73A		14
74HC 109	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS109A		16
74HC 112	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	LS76A,LS112A	4027,7476	16
74HC 113	DUAL J-K FLIP-FLOP WITH PRESET	LS113A		14
74HC 74	DUAL D F/F WITH PRESET AND CLEAR	LS74A	4013	14
74HC T74	DUAL D F/F WITH PRESET AND CLEAR	LS74A	4013	14
74HC 174	HEX D FLIP-FLOP WITH CLEAR	LS174	40174	16
74HCT174	HEX D FLIP-FLOP WITH CLEAR	LS174	40174	16
74HC 175	QUAD D FLIP-FLOP WITH CLEAR	LS175	40175	16
74HC 273	OCTAL D FLIP-FLOP WITH CLEAR	LS273		20
74HCT273	OCTAL D FLIP-FLOP WITH CLEAR	LS273		20
74HC 377	OCTAL D-TYPE FLIP-FLOP			20
74HC 374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT374	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 534	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS534		20
74HCT534	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS534		20
74HC 564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HCT564	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	LS564		20
74HC 574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HCT574	OCTAL D-TYPE FLIP-FLOP (3-STATE)	LS374,LS574		20
74HC 646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HCT646	OCTAL BUS TRANSCEIVER/REGISTER	LS646		24
74HC 648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HCT648	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS648		24
74HC 651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HCT651	OCTAL BUS TRANSCEIVER/REGISTER (INV.)	LS651		24
74HC 652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24
74HCT652	OCTAL BUS TRANSCEIVER/REGISTER	LS652		24

* Suggested alternative

FLIP-FLOP

DUAL J-K FLIP-FLOP WITH CLEAR

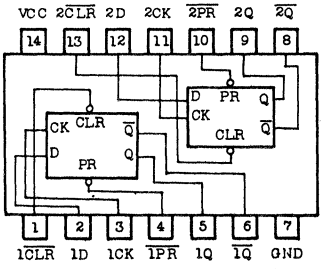
73



DUAL D FLIP-FLOP WITH PRESET AND CLEAR

74

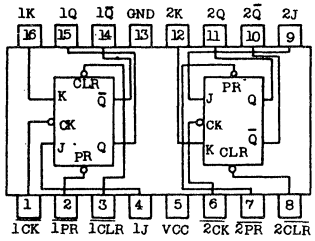
T74



FLIP-FLOP (Continued)

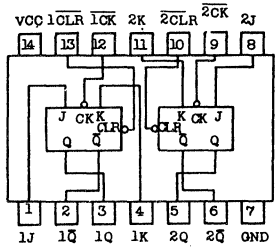
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

76



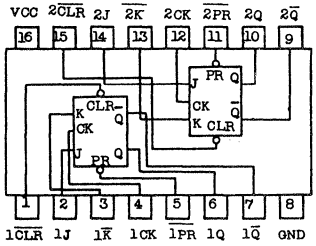
DUAL J-K FLIP-FLOP WITH CLEAR

107



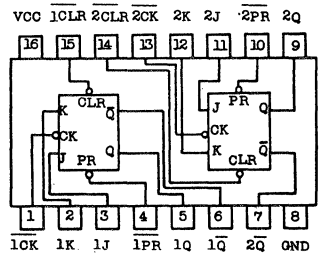
DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR

109



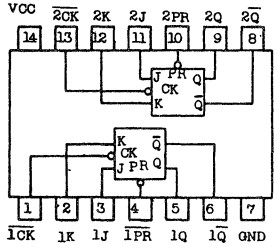
DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

112



DUAL J-K FLIP-FLOP WITH PRESET

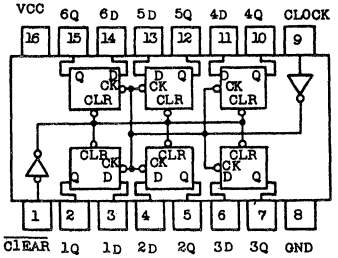
113



HEX D FLIP-FLOP WITH CLEAR

174

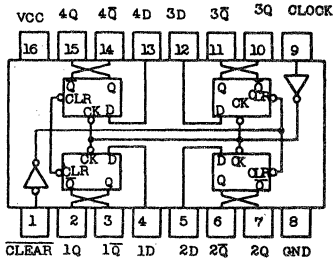
T174



FLIP-FLOP (Continued)

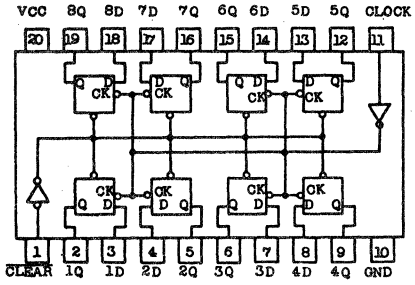
QUAD D FLIP-FLOP WITH CLEAR

175



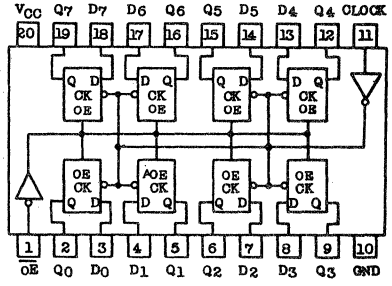
OCTAL D FLIP-FLOP WITH CLEAR

273
T273



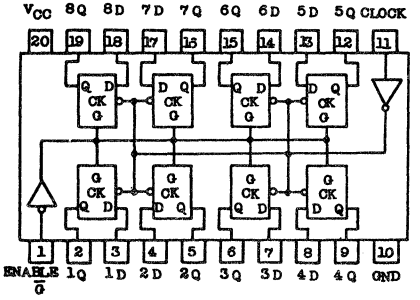
OCTAL D FLIP-FLOP (3-STATE)

374
T374



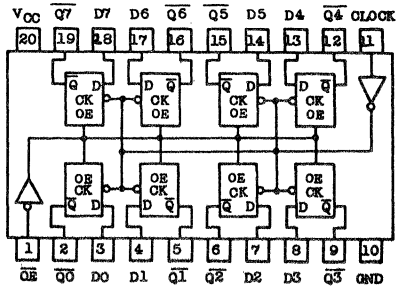
OCTAL D FLIP-FLOP

377



OCTAL D FLIP-FLOP (3-STATE/INV.)

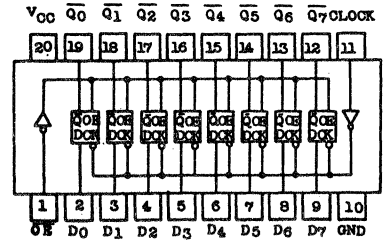
534
T534



OCTAL D FLIP-FLOP (3-STATE/INV.)

564

T564

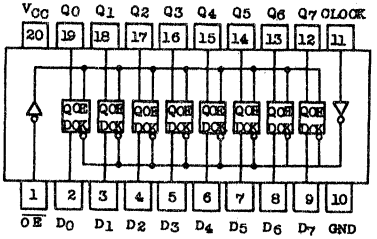


FLIP-FLOP (Continued)

OCTAL D FLIP-FLOP (3-STATE)

574

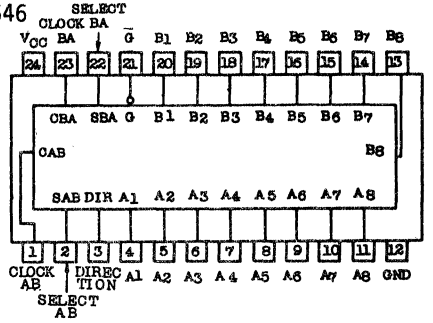
T574



OCTAL BUS TRANSCEIVER REGISTER (3-STATE)

646

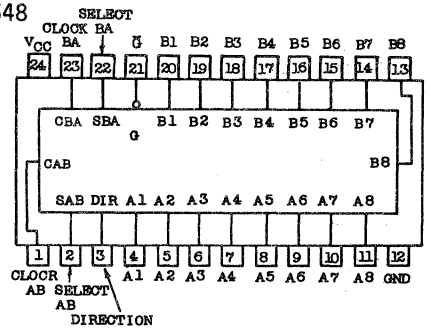
T646



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

648

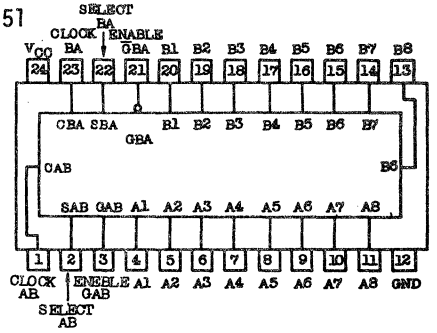
T648



OCTAL BUS TRANSCEIVER REGISTER (3-STATE/INV.)

651

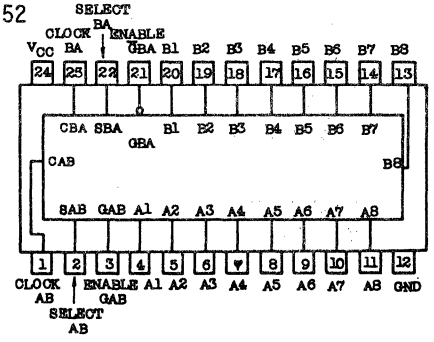
T651



OCTAL BUS TRANSCEIVERS REGISTER (3-STATE)

652

T652



LATCH

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 75	4-BIT D-TYPE LATCH	LS75	*4042	16
74HC 77	4-BIT D-TYPE LATCH	LS77	*4042	14
74HC 259	8-BIT ADDRESSABLE LATCH	LS259	*4099	16
74HC 279	QUAD $\overline{S}$-$\overline{R}$ LATCH	LS279	*4043,*4044	16
74HC 375	QUAD D-TYPE LATCH	LS375		16
74HC 373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT373	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HC 533	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS533		20
74HCT533	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS533		20
74HC 563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HCT563	OCTAL D-TYPE LATCH (3-STATE/INV.)	LS563		20
74HC 573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20
74HCT573	OCTAL D-TYPE LATCH (3-STATE)	LS373,LS573		20

* Suggested alternative

LATCH

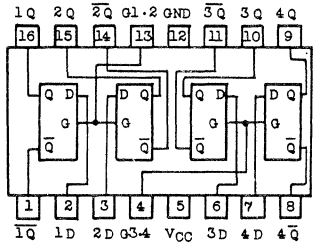
4-BIT LATCH

75

FUNCTION TABLE

INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Q}$n

X:DON'T CARE



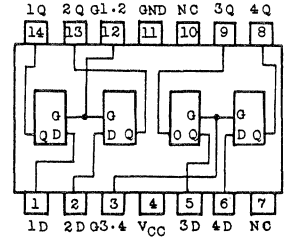
4-BIT LATCH

77

FUNCTION TABLE

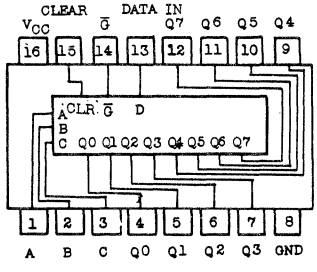
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Q}$n

X:DON'T CARE



8-BIT ADDRESSABLE LATCH

259



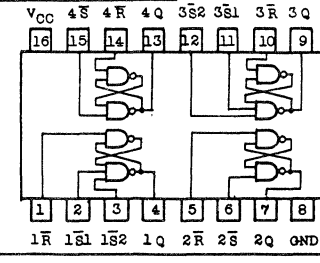
QUAD $\overline{S}$-$\overline{R}$ LATCH

279

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{S}$*	$\overline{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

* FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:
H=BOTH $\overline{S}$ INPUTS HIGH
L=ONE OF BOTH INPUTS LOW

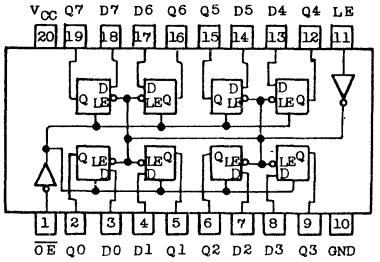


LATCH (Continued)

OCTAL LATCH (3-STATE)

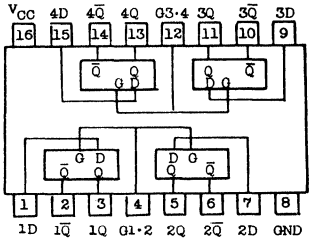
373 NONINVERTED DATA OUTPUTS

T373



QUAD LATCH

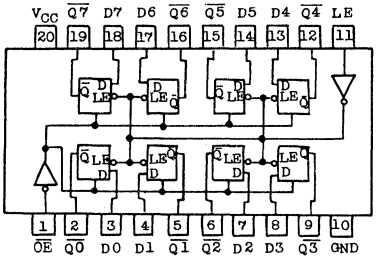
375



OCTAL LATCH (3-STATE)

533 INVERTED DATA OUTPUTS

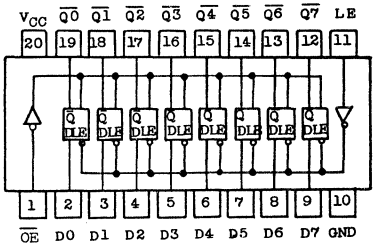
T533



OCTAL LATCH (3-STATE)

563 INVERTED DATA OUTPUTS

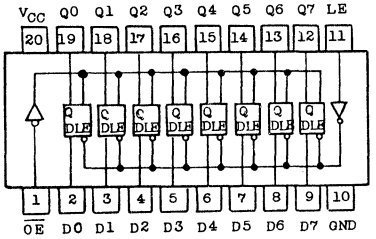
T563



OCTAL LATCH (3-STATE)

573 NONINVERTED DATA OUTPUTS

T573



MULTIVIBRATOR

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 123	DUAL MONOSTABLE MULTIVIBRATOR	LS123	*4538,*4528	16
74HC 221	DUAL MONOSTABLE MULTIVIBRATOR	LS221	*4538,*4528	16
74HC 423	DUAL MONOSTABLE MULTIVIBRATOR	LS423	*4538,*4528	16
74HC4538	DUAL MONOSTABLE MULTIVIBRATOR	*LS423	4538, 4528	16

* Suggested alternative

MULTIVIBRATOR

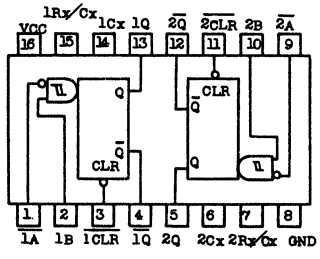
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

123

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔
↓	L	H	⊓	⊔

X: DON'T CARE



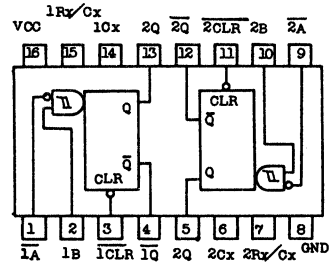
DUAL MONOSTABLE MULTIVIBRATOR

221

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔
↓	L	H	⊓	⊔

X : DON'T CARE



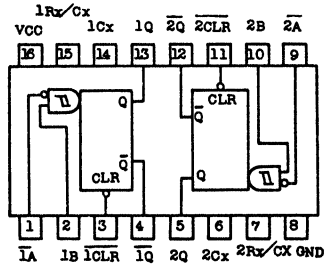
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

423

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLEAR}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔

X : DON'T CARE



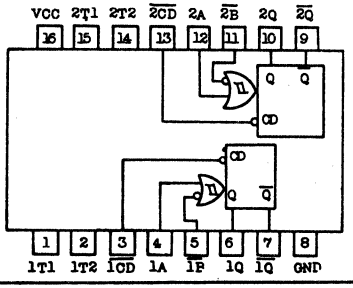
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

4538

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CD}$	A	$\overline{B}$	Q	$\overline{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↓	⊓	⊔
H	↓	H	⊓	⊔

X : DON'T CARE



DECODER

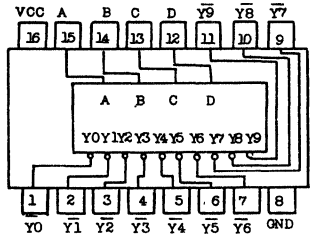
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 42	BCD TO DECIMAL DECODER	LS42	*4028	16
74HC 131	3-TO-8 LINE DECODER/LATCH	LS131		16
74HC 137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HCT137	3-TO-8 LINE DECODER/LATCH	LS137		16
74HC 138	3-TO-8 LINE DECODER	LS138		16
74HCT138	3-TO-8 LINE DECODER	LS138		16
74HC 139	DUAL 2-TO-4 LINE DECODER	LS139	4556,*4555	16
74HC 154	4-TO-16 LINE DECODER	LS154	*4515	24
74HC 155	DUAL 2-TO-4 LINE DECODER	LS155	*4556,*4555	16
74HC 237	3-TO-8 LINE DECODER/LATCH			16
74HC 238	3-TO-8 LINE DECODER			16
74HC4028	BCD-TO DECIMAL DECODER		4028	16
74HC4514	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4514	24
74HC4515	4-TO-16 LINE DECODER/LATCH	*LS154,*LS159	4515	24
74HC4511	BCD TO 7 SEGMENT L/D/D (LED)	*LS47,*LS48,*LS49	4511	16
74HC4543	BCD TO 7 SEGMENT L/D/D (LCD)	*LS47,*LS48,*LS49	4543	16

* Suggested alternative

DECODER (Continued)

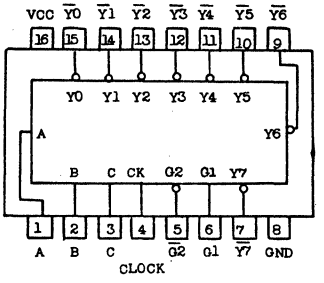
BCD TO DECIMAL DECODER

42



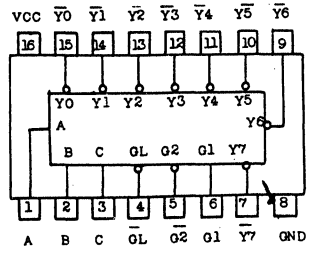
3-TO-8 LINE DECODER/LATCH

131



3-TO-8 LINE DECODER/LATCH

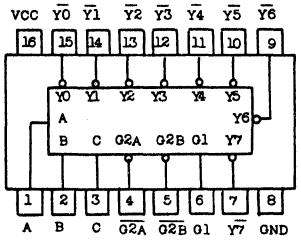
137



3-TO-8 LINE DECODER

138

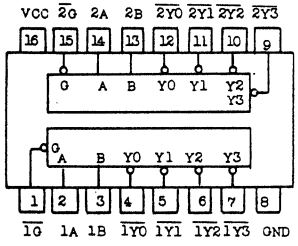
T138



DECODER (Continued)

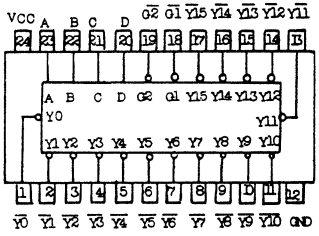
DUAL 2-TO-4 LINE DECODER

139



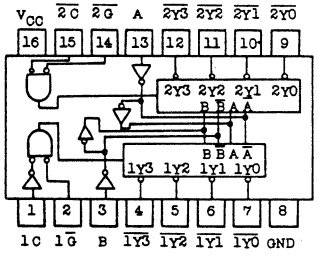
4-TO-16 LINE DECODER

154



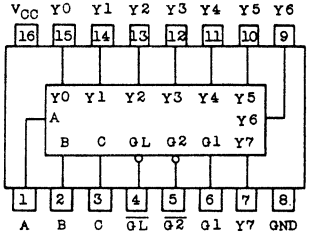
DUAL 2-TO-4 LINE DECODER 3-TO-8 LINE DECODER

155



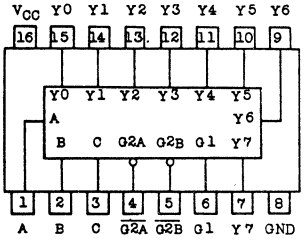
3-TO-8 LINE DECODER/LATCH

237



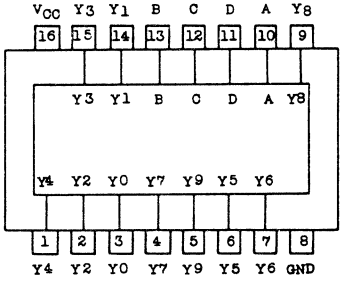
3-TO-8 LINE DECODER

238



BCD-TO-DECIMAL DECODER

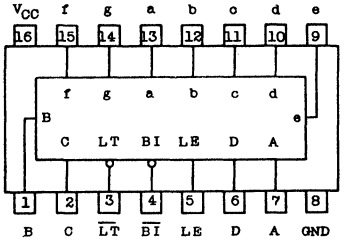
4028



DECODER (Continued)

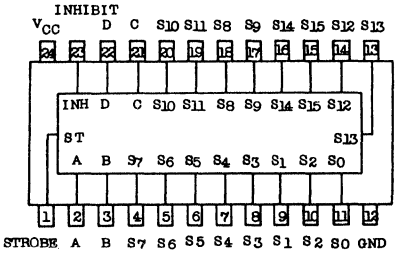
BCD TO 7 SEGMENT LATCH/DECODER/DRIVER

4511



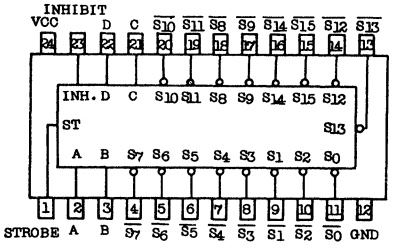
4-TO-16 LINE DECODER/LATCH

4514



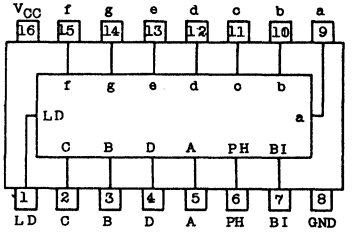
4-TO-16 LINE DECODER/LATCH

4515



BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

4543



ENCODER

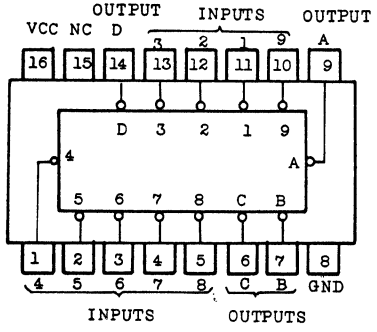
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 147	10-TO-4 LINE PRIORITY ENCODER	LS147		16
74HC 148	8-TO-3 LINE PRIORITY ENCODER	LS148	*4532	16

* Suggested alternative

ENCODER

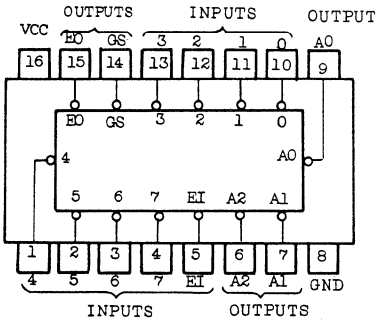
10-TO-4 LINE PRIORITY ENCODER

147



8-TO-3 LINE PRIORITY ENCODER

148



REGISTER

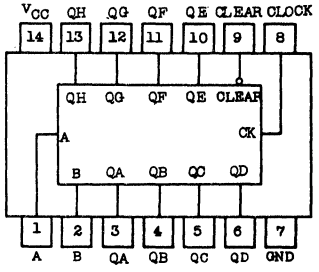
品　名	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 164	8-BIT SIPO SHIFT REGISTER	LS164	*4034	14
74HCT164	8-BIT SIPO SHIFT REGISTER	LS164	*4034	14
74HC 165	8-BIT PISO SHIFT REGISTER	LS165	*4014,*4021	16
74HC 166	8-BIT PISO SHIFT REGISTER	LS166	*4014,*4021	16
74HC 173	QUAD D-TYPE REGISTER (3-STATE)	LS173	4076	16
74HC 194	4-BIT PIPO SHIFT REGISTER	LS194A	40194,*40104	16
74HC 195	4-BIT PIPO SHIFT REGISTER	LS195A	*4035	16
74HC 299	8-BIT PIPO SHIFT REGISTER	LS299	*4034	20
74HC 323	8-BIT PIPO SHIFT REGISTER	LS323	*4034	20
74HC 595	8-BIT SHIFT REGISTER/LATCH (3-STATE)	LS595		16
74HC 597	8-BIT LATCH/SHIFT REGISTER	LS597		16
74HC 670	4 WORD × 4-BIT REGISTER FILE (3-STATE)	LS670		16
74HC4094	8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)		4094	16

* Suggested alternative

REGISTER

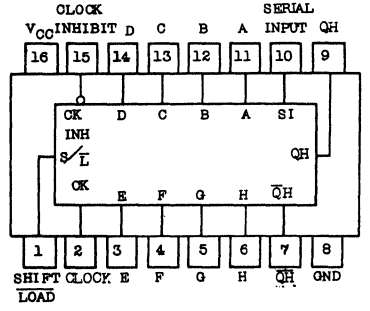
8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

164
T164



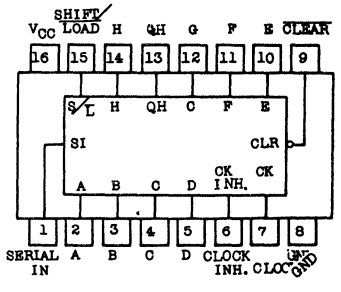
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER

165



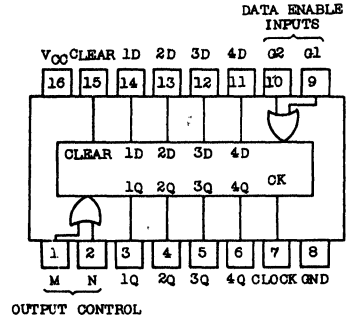
8-BIT PARALLEL-IN/SERIAL-OUT SHIFT

166



QUAD D FLIP-FLOP (3-STATE)

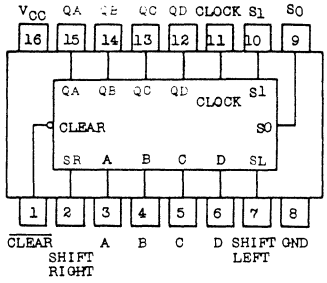
173



REGISTER (Continued)

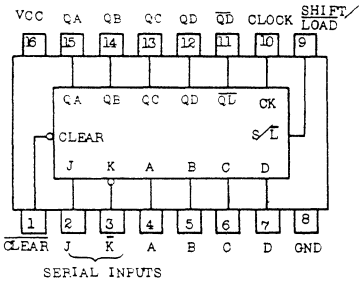
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

194



4-BIT PARALLEL-IN/PARALLEL-OUT SHIFT REGISTER

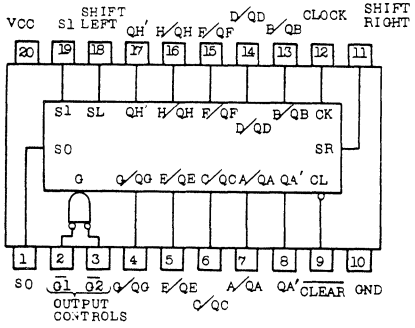
195



8-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER (3-STATE)

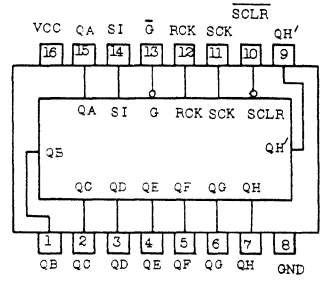
299 DIRECT CLEAR

323 SYNCHRONOUS CLEAR



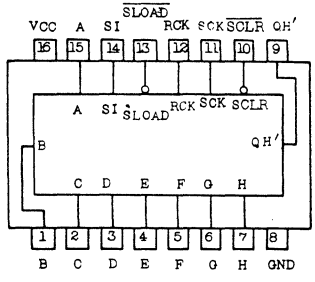
8-BIT SHIFT REGISTER/LATCH (3-STATE)

595



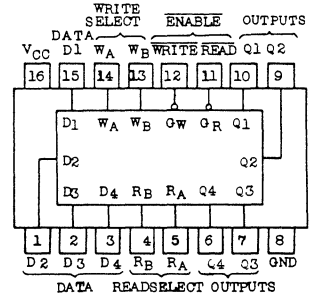
8-BIT LATCH/SHIFT REGISTER

597



4 WORD x 4 BIT REGISTER FILE(3-STATE)

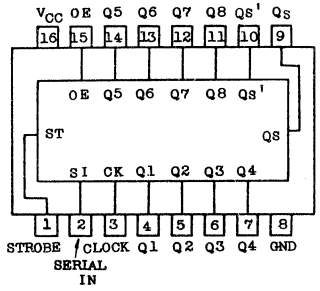
670



REGISTER (Continued)

8-BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER/LATCH (3-STATE)

4094



COUNTER

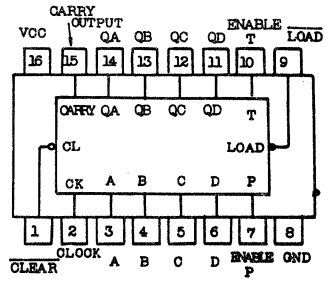
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 161	SYNC. BINARY COUNTER WITH ASYNC. CLEAR	LS161A	40161	16
74HC 163	SYNC. BINARY COUNTER WITH SYNC. CLEAR	LS163A	40163	16
74HC 191	4-BIT BINARY UP/DOWN COUNTER	LS191	*4516	16
74HC 193	SYNC. UP/DOWN BINARY COUNTER	LS193	40193	16
74HC 393	DUAL BINARY COUNTER	LS393	*4520	14
74HC 590	8-BIT BINARY COUNTER/REGISTER (3-STATE)	LS590		16
74HC 592	8-BIT REGISTER/BINARY COUNTER	LS592		16
74HC 593	8-BIT REGISTER/BINARY COUNTER (3-STATE)	LS593		20
74HC 691	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS691		20
74HC 693	4-BIT BINARY COUNTER REGISTER (3-STATE)	LS693		20
74HC 697	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS697		20
74HC 699	U/D 4-BIT BINARY CTR./REGISTER(3-STATE)	LS699		20
74HC4520	DUAL 4-BIT BINARY COUNTER		4520	16
74HC 160	SYNC. DECADE COUNTER WITH ASYNC. CLEAR	LS160A	40160	16
74HC 162	SYNC. DECADE COUNTER WITH SYNC. CLEAR	LS162A	40162	16
74HC 190	BCD UP/DOWN COUNTER	LS190	*4510	16
74HC 192	SYNC. UP/DOWN DECADE COUNTER	LS192	40192	16
74HC 390	DUAL DECADE COUNTER	LS390		16
74HC 690	DECADE COUNTER REGISTER (3-STATE)	LS690		20
74HC 692	DECADE COUNTER REGISTER (3-STATE)	LS692		20
74HC 696	U/D DECADE COUNTER/REGISTER (3-STATE)	LS696		20
74HC 698	U/D DECADE COUNTER/REGISTER (3-STATE)	LS698		20
74HC4518	DUAL DECADE COUNTER		4518	16
74HC4017	DECADE COUNTER/DIVIDER		4017	16
74HC4020	14-STAGE BINARY COUNTER		4020	16
74HC4022	OCTAL COUNTER/DIVIDER		4022	16
74HC4024	7-STAGE BINARY COUNTER		4024	14
74HC4040	12-STAGE BINARY COUNTER		4040	16
74HC4060	14-STAGE BINARY COUNTER/OSCILLATOR			16
74HC40102	DUAL BCD PROGRAMMABLE DOWN COUNTER		40102	16
74HC40103	8-BIT BINARY PROGRAMMABLE DOWN COUNTER		40103	16
74HC7292	PROGRAMMABLE DIVIDER/TIMER	*LS292		16
74HC7294	PROGRAMMABLE DIVIDER/TIMER	*LS294		16

* Suggested alternative

COUNTER

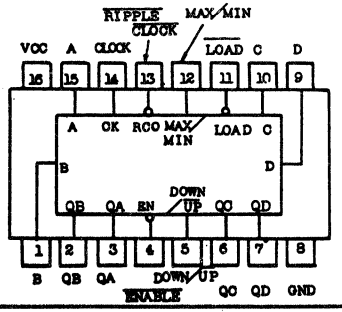
PRESETTABLE 4-BIT COUNTER

160 DECADE, ASYNCHRONOUS CLEAR
161 BINARY, ASYNCHRONOUS CLEAR
162 DECADE, SYNCHRONOUS CLEAR
163 BINARY, SYNCHRONOUS CLEAR



SYN. 4-BIT UP/DOWN COUNTER

190 BCD
191 BINARY

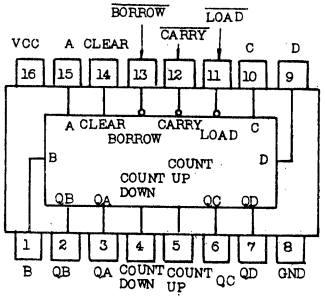


COUNTER (Continued)

SYNC. 4-BIT UP/DOWN COUNTER

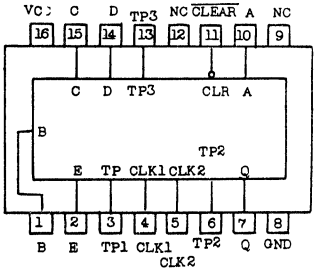
192 BCD

193 BINARY



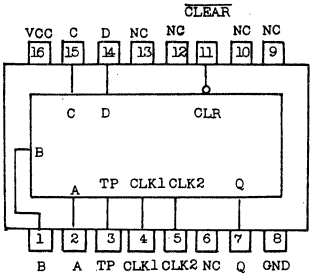
PROGRAMMABLE DIVIDER/TIMER

7292 FROM 2^2 to 2^{31}



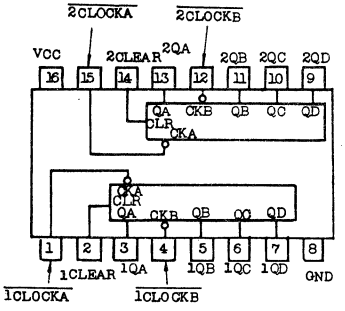
PROGRAMMALBE DIVIDER/TIMER

7294 FROM 2^2 to 2^{15}



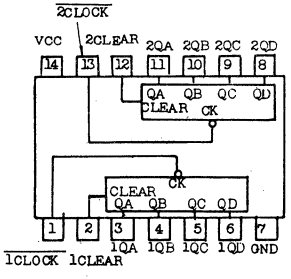
DUAL DECADE COUNTER

390 (BI-QUINARY OR BCD)



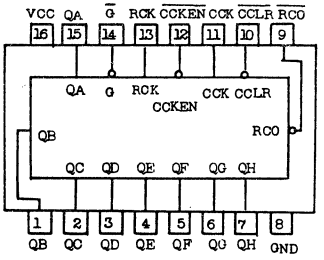
DUAL 4-BIT BINARY COUNTER

393



8-BIT BINARY COUNTER WITH OUTPUT REGISTER (3-STATE)

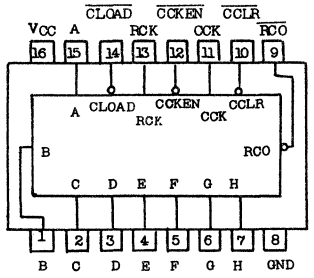
590



COUNTER (Continued)

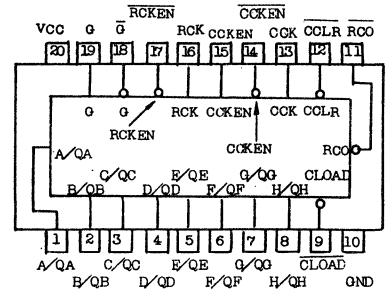
8-BIT BINARY COUNTER WITH INPUT REGISTER

592



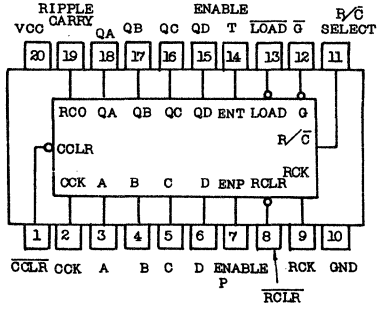
8-BIT BINARY COUNTER WITH INPUT REGISTER (MULTIPLEXED 3-STATE OUTPUTS)

593



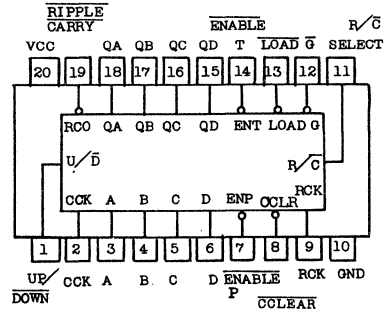
SYNCHRONOUS COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUT

690 DECADE, DIRECT CLEAR
691 BINARY, DIRECT CLEAR
692 DECADE, SYNCHRONOUS CLEAR
693 BINARY, SYNCHRONOUS CLEAR



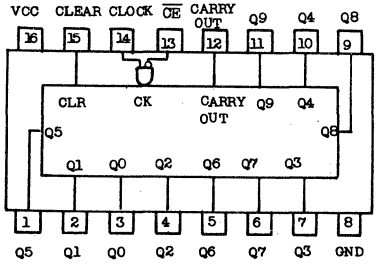
SYNCHRONOUS UP/DOWN COUNTERS/REGISTER WITH MULTIPLEXED 3-STATE OUTPUTS

696 DECADE, DIRECT CLEAR
697 BINARY, DIRECT CLEAR
698 DECADE, SYNCHRONOUS CLEAR
699 BINARY, SYNCHRONOUS CLEAR



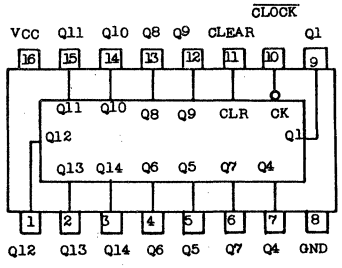
DECADE COUNTER/DIVIDER

4017



14-STAGE BINARY COUNTER

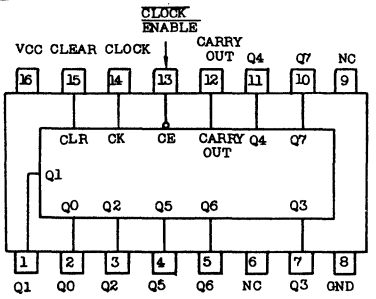
4020



COUNTER (Continued)

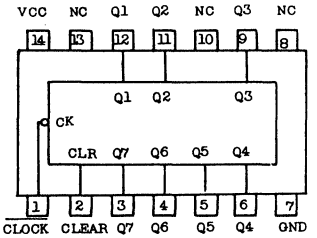
OCTAL COUNTER/DIVIDER

4022



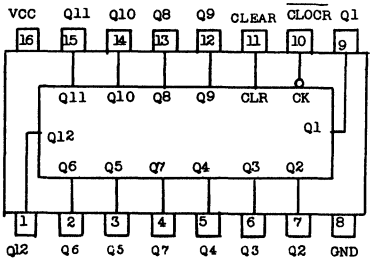
7-STAGE BINARY COUNTER

4024



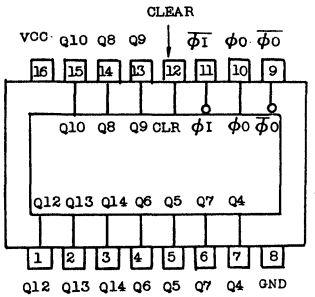
12-STAGE BINARY COUNTER

4040



14-STAGE BINARY COUNTER/OSCILLATOR

4060

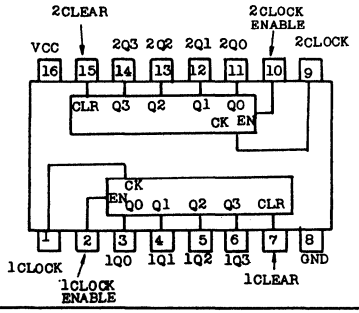


DUAL DECADE COUNTER

4518

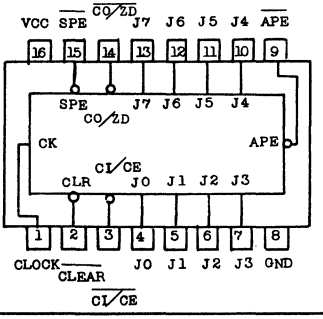
DUAL BINARY COUNTER

4520



PROGRAMMABLE DOWN COUNTER

40102 DUAL BCD
40103 8-BIT BINARY



MULTIPLEXER

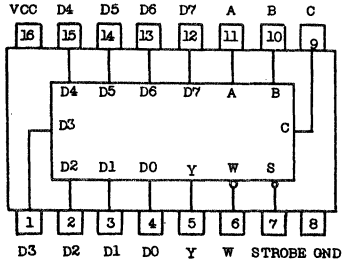
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC4016	QUAD BILATERAL SWITCH		4016	14
74HC4051	8-CHANNEL ANALOG MULTIPLEXER		4051	16
74HC4052	DUAL 4-CHANNEL ANALOG MULTIPLEXER		4052	16
74HC4053	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER		4053	16
74HC4066	QUAD BILATERAL SWITCH		4016,4066	14
74HC4316	QUAD BILATERAL SWITCH		*4016	16
74HC4351	8-CH. ANALOG MUX. WITH ADD. LATCH		*4051	20
74HC4352	DUAL 4-CH. ANALOG MUX. WITH ADD. LATCH		*4052	20
74HC4353	TRIPLE 2-CH. ANALOG MUX. WITH ADD. LATCH		*4053	20
74HC 151	8-CHANNEL MULTIPLEXER	LS151	*4512	16
74HC 153	DUAL 4-CHANNEL MULTIPLEXER	LS153	*4539	16
74HC 157	QUAD 2-CHANNEL MULTIPLEXER	LS157		16
74HC 158	QUAD 2-CHANNEL MULTIPLEXER (INVERTING)	LS158		16
74HC 251	8-CHANNEL MULTIPLEXER (3-STATE)	LS251	*4512	16
74HC 253	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	LS253	*4539	16
74HC 257	QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	LS257		16
74HC 258	QUAD 2-CHANNEL MULTIPLEXER (3-STATE/INVERTING)	LS258		16
74HC 298	QUAD 2-CHANNEL MULTIPLEXER/REGISTER	LS298		16
74HC 352	DUAL 4-CHANNEL MULTIPLEXER	L5352	*4539	16
74HC 353	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	LS354	*4539	16
74HC 354	8-CHANNEL MULTIPLEXER/REGISTER	LS354	*4512	20
74HC 356	8-CHANNEL MULTIPLEXER/REGISTER	LS356	*4512	20

* Suggested alternative

MULTIPLEXER

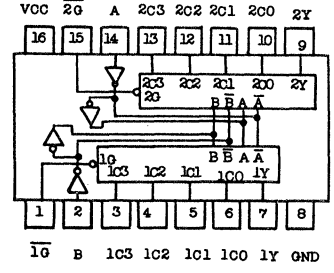
8-CHANNEL MULTIPLEXER

151



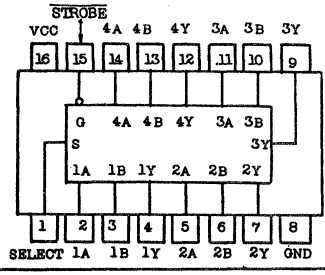
DUAL 4-CHANNEL MULTIPLEXER

153



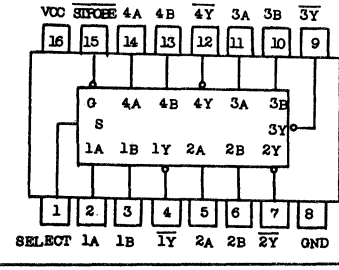
QUAD 2-CHANNEL MULTIPLEXER

157 NONINVERTED DATA OUTPUTS



QUAD 2-CHANNEL MULTIPLEXER

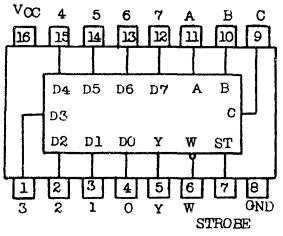
158 INVERTED DATA OUTPUTS



MULTIPLEXER (Continued)

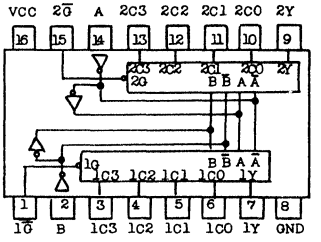
8-CHANNEL MULTIPLEXER (3-STATE)

251



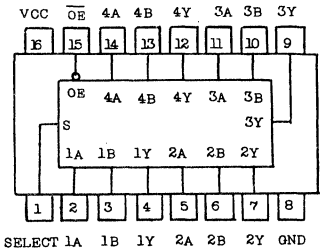
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)

253



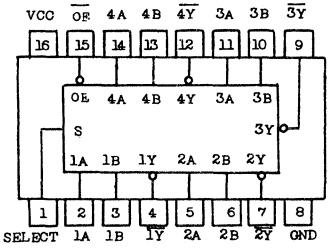
QUAD 2-CHANNEL MULTIPLEXER (3-STATE)

257 NONINVERTED DATA OUTPUTS



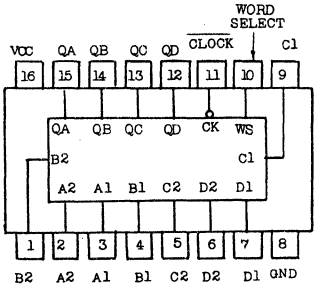
QUAD 2-CNANNEL MULTIPLEXER (3-STATE)

258 INVERTED DATA OUTPUTS



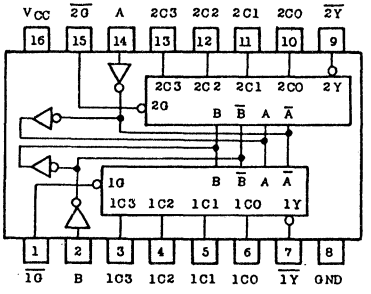
QUAD 2-CHANNEL MULTIPLEXERS WITH OUTPUT REGISTER

298



DUAL 4-CHANNEL MULTIPLEXER

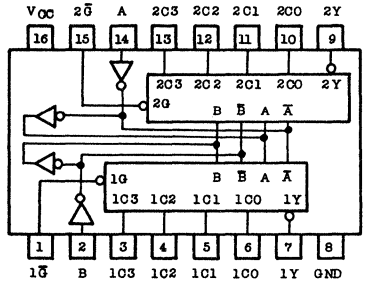
352



MULTIPLEXER (Continued)

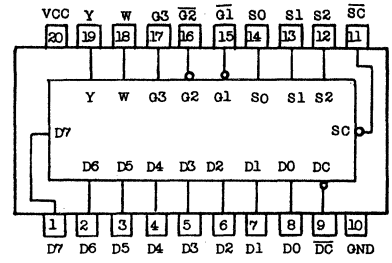
DUAL 4-CHANNEL MULTIPLEXER (3-STATE)

353



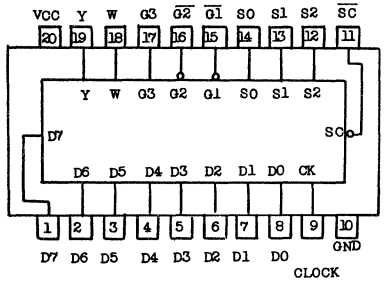
8-CHANNEL MULTIPLEXER WITH LATCH (3-STATE)

354



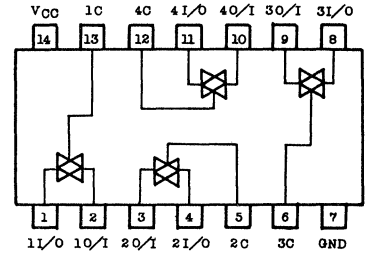
8-CHANNEL MULTIPLEXER WITH FLIP-FLOP (3-STATE)

356



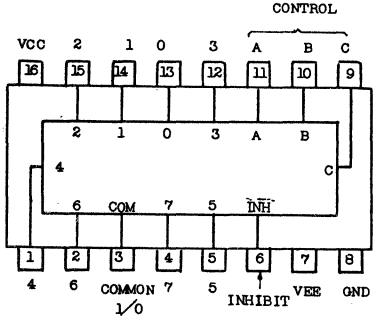
QUAD BILATERAL SWITCH

4016



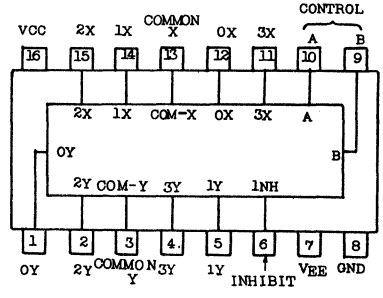
8-CHANNEL ANALOG MULTIPLEXER

4051



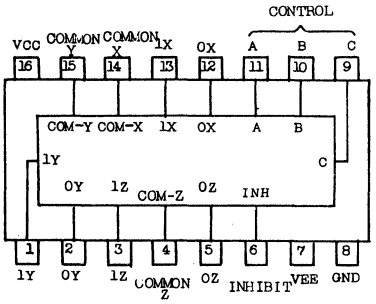
DUAL 4-CHANNEL ANALOG MULTIPLEXER

4052

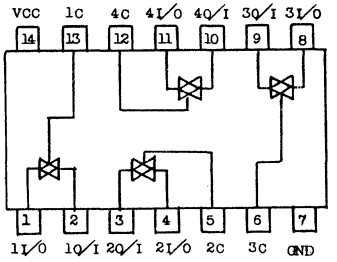


MULTIPLEXER (Continued)

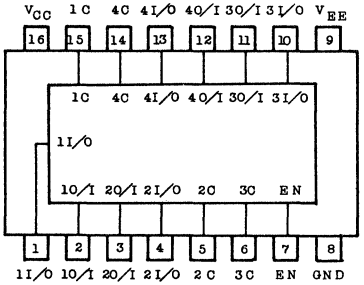
TRIPLE 2-CHANNEL ANALOG MULTIPLEXER
4053



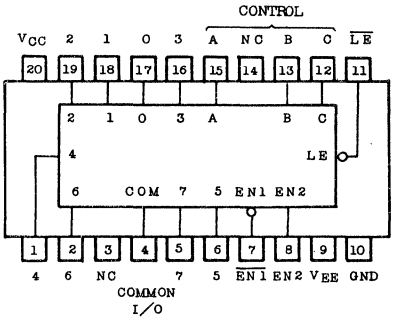
QUAD BILATERAL SWITCH
4066



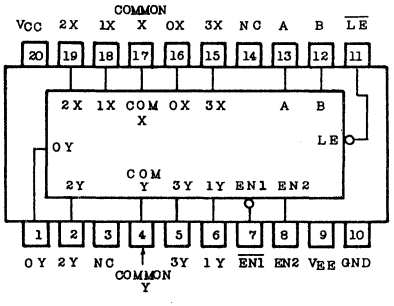
QUAD BILATERAL SWITCH
4316



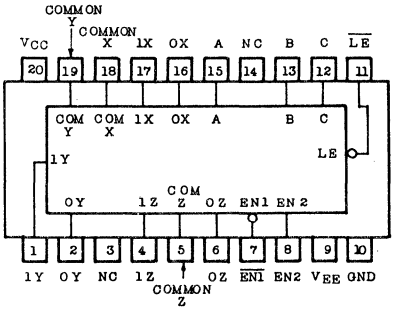
8-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH
4351



DUAL 4-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH
4352



TRIPLE 2-CHANNEL ANALOG MULTIPLEXER WITH ADDRESS LATCH
4353



COMPARATOR

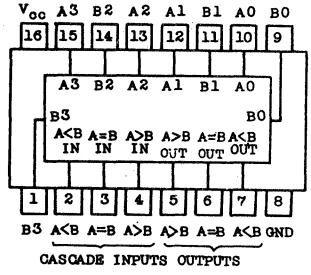
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 85	4-BIT MAGNITUDE COMPARATOR	LS 85	*4063, *4585	16
74HC 688	8-BIT EQUALITY COMPARATOR	LS688		20
74HCT688	8-BIT EQUALITY COMPARATOR	LS688		20

* Suggested alternative

COMPARATOR

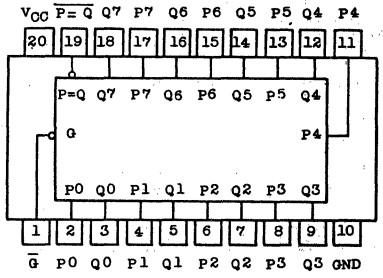
4-BIT MAGNITUDE COMPARATOR

85



8-BIT EQUALITY COMPARATOR

688
T688



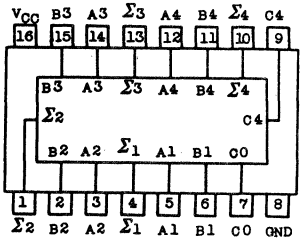
ADDER

Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 283	4-BIT BINARY FULL ADDER	LS283,LS83	4008	16

ADDER

4-BIT BINARY FULL ADDER

283



ALU

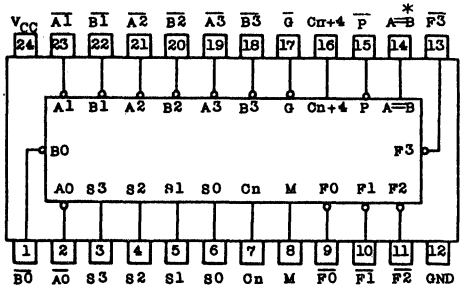
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC 181	ARITHMETIC LOGIC UNIT	LS181		24
74HC 182	LOOK AHEAD CARRY LOGIC	LS182		16

ALU

ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

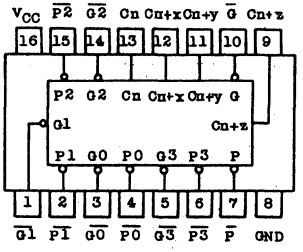
181

*: OPEN DRAIN OUTPUT



LOCK AHEAD CARRY GENERATOR

182



PARITY TREE

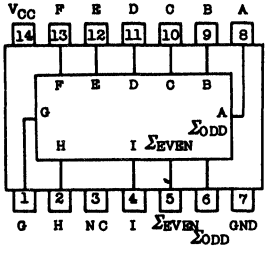
Type Number	Function	Equivalent LSTTL	Equivalent CMOS.	Pin Number
74HC280	9-BIT PARITY GENERATOR/CHECKER	LS280	*4531	14

* 類似品

PARITY TREE

9-BIT ODD/EVEN PARITY GENERATOR/ CHECKER

280



3. PRODUCT OUTLINE OF THE TC74HCxxxA SERIES

The TC74HCxxxA series is an improved High Speed Logic development of TOSHIBA. Some of these improvements are outlined below:

(1) Increased Speed of Operation:

Over 20 companies now manufacture the 74HC series worldwide. The JEDEC JC40.2 committee has standardized the electrical characteristics of this series in JEDEC Standard 7A. This permits interchangeability of devices between manufacturers for greater end-user convenience. Increasing the speed of the TC74HCxxxA series by an average of 20% to 30% ensures compatibility with Standard 7A as well as with most other worldwide 74HC products. TOSHIBA achieved the higher speed by using a thinner gate oxide layer and by decreasing the effective channel length and the internal parasitic capacitance to increase transconductance (gm) per unit channel width by 30% over that of the original series.

(2) Latch-up Strength:

TOSHIBA had previously improved the TC74HC series to make it latch-up resistant. By using the same process, the TC74HCxxxA revision also has a high resistance to latch-up; TOSHIBA high speed C^2MOS products can be used in applications in which noise and surges often occur.

Table 3-1 shows the results of latch-up tests.

Table 3-1 Results of Latch-up Tests **

		TC74xxx series		TC74xxxA series	
method	pin	TC74HC00P	TC74HC74P	TC74HC00AP	TC74HC74AP
Current Injection (static trigger)	Input	>±70mA *	>±70mA *	>±300mA	>±300mA
	Output	>±300mA	>±300mA	>±300mA	>±300mA
Charge Injection (dynamic trigger)	Input	>±250V	>±250V	>±250V	>±250V
	Output	>±250V	>±250V	>±250V	>±250V
	Power supply	>±250V	>±250V	>±250V	>±250V

* Input protection resistor limits current

** See Fig. 9-14 Latch-up strength measurement system in Sect. 9-7.

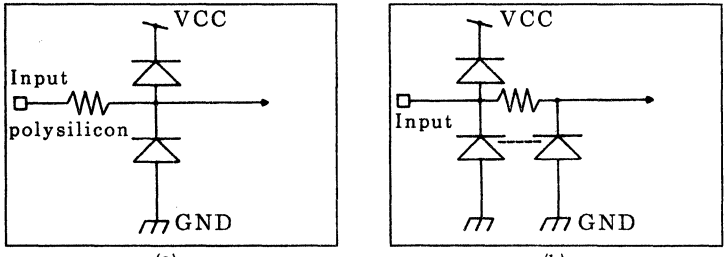
(3) Electrostatic Discharge:

In the original TC74HCxxx series, TOSHIBA designed in an input protective circuit which combines silicon diodes with a polysilicon series resistor (Fig. 3-1(a)). This circuit suppresses excess current flow in the input terminal when the input voltage is higher than V_{CC} or lower than GND. This circuit is effective for increased latch-up protection, but the electrostatic discharge protection, measured using the MIL-STD method (100pF/1.5kohms), was about ±2.0kV maximum. Anything above this caused burn damage to the polysilicon resistor or increased breakdown of the oxide film directly under the polysilicon.

As there is no latch-up problem with the TC74HCxxxA series, TOSHIBA uses a protective circuit composed of high thermal capacity silicon diodes and a resistor constructed by diffusion (Fig. 3-1(b) . According to MIL-STD, any product not reaching a ±2.0kV level must carry an ESD Sensitive (ESDS) label. TOSHIBA's TC74HCxxxA series far surpasses this level with a 2.0kV or greater rating using the MIL method.

Table 3-2 shows the Electrostatic Discharge Test Results.

Fig. 3-1 The Input Protective Circuits

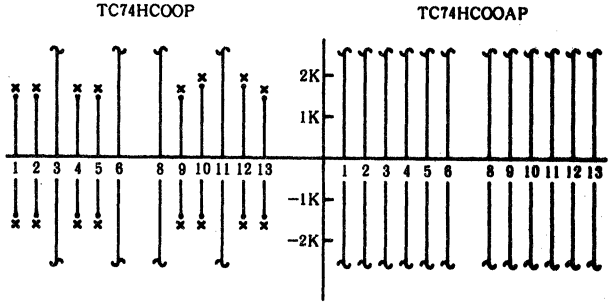


(a) TC74HCxxx series

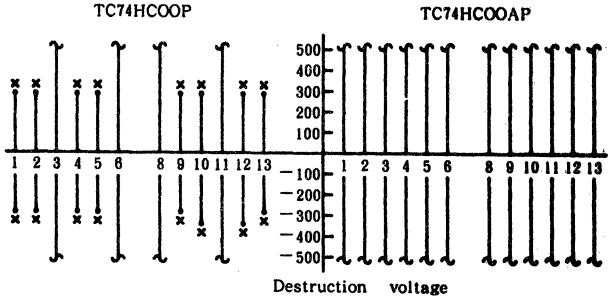
(b) TC74HCxxxA series

Table 3-2 ESD Test Result

(a) MIL Method (C=100pF, R= 1.5KΩ)

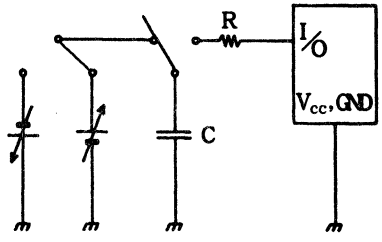


(b) EIAJ Method (C=200pF, R=0Ω)



·Normal ×Destruction ⊥ Discharge stopped

(c) Test Circuit



3-1 Features

High Speed Operation: Same as LSTTL

Low Power Dissipation: Same as standard CMOS series (μW)

Output Drive Capability: Capable of directly driving 10 LSTTL loads (Standard output type).
Capable of directly driving 15 LSTTL loads (Buffer output type).

High Noise Immunity HC/HCU Type ··· 45% V_{CC} (Typ.)
HCT Type ····· 25% V_{CC} (Typ.)

Wide Operating Voltage Range:
HC/HCU Type ··· 2 to 6V
HCT Type ····· 4.5 to 5.5V

Wide Operating Temperature Range: −40 to + 85℃

Self−contained static electricity protective circuit:
±500V (typ.) by EIAJ method
±3000V (typ.) by MIL STD method
(All inputs and outputs)

Ample Latch up Capacity: Total input and output ±300 mA and above.

Based on the same pin connection and function with LSTTL,
and line up with CMOS original version.

Wide product Line up: Over 200 types

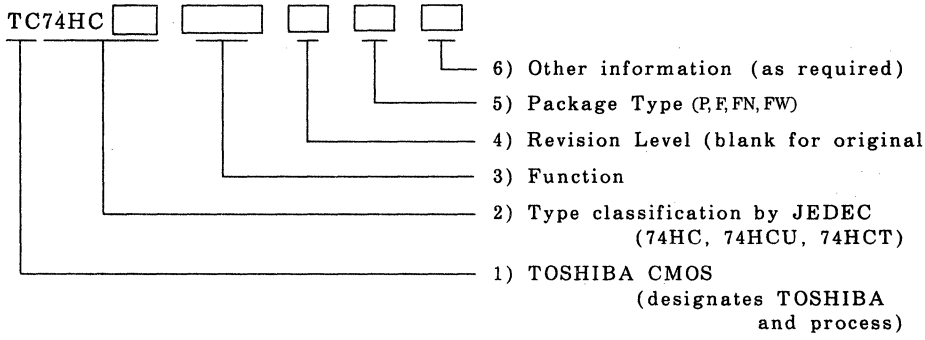
Table 3−2 shows comparison of characteristics of various logic families.

Parameter		HCL (TC74HCxxxA)	LSTTL	HS−C²MOS (TC40Hxxx)	C² MOS (TC4xxx)	Condition
Propagation Delay Time GATE (C_L=15pF)		6ns typ	9ns typ	15ns typ	65ns typ	V_{CC} =5.0V Ta=25℃
Maximum Clock Frequency J/KF • F (C_L=15pF)		80MHz typ	45MHz typ	20MHz typ	2MHz typ	
Quiescent Power Dissipation (GATE)		0.01 μW typ	8mW typ	0.01 μW typ	0.01 μW typ	Over temperature and voltage range
Input Voltage	V_{IH}	3.5V min	2.0V min	4.0V min	3.5V min	V_{CC} =5.0V Over temperature range
	V_{IL}	1.5V max	0.8V max	1.0V max	1.5V max	
Output Current	$\|I_{OH}\|$	4mA min•1	0.4mA min•2	0.36mA min•3	0.42mA min•3	•1 V_{CC}=4.5V •2 V_{CC}=4.75V •3 V_{CC}=5V Over temp. range
	I_{OL}	4mA min	4mA min	0.8mA min	0.42mA min	
Operating Voltage Range		2~6V	4.75~5.25V	2~8V	3~18V	
Operating Temperature Range		−40~85℃	0~70℃	−40~85℃	−40~85℃	

Table 3−2 Comparison of Logic Family Characteristics

3–2 Method of Designating the TC74HC Series

The TC74HC series is designated by using the standard established by JEDEC and is as shown below;



(Example) TC74HCT240AP

High Speed C^2MOS IC which is pin and functionally compatible with the bipolar 74LS240
Input is designed for TTL voltage levels, and direct driving from LSTTL is possible.
Package type is plastic Dual Inline Package (DIP).

(1) "TC"

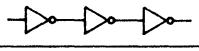
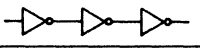
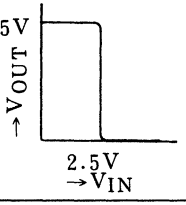
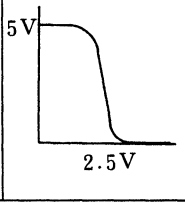
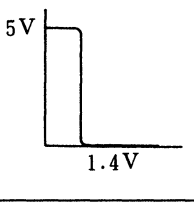
Proprietary name identifying TOSHIBA CMOS devices.

(2) Type classification (HC, HCU, HCT)

In addition to the HC devices, there are HCU and HCT types. These differentiations were made by JEDEC in order to separate CMOS devices of the same function by with different input levels or the existence of a buffer

TYPE	Internal stages	Input threshold voltage
HC	Two stages and above	CMOS level
HCU	One stage	CMOS level
HCT	Two stages and above	TTL level

Taking an inverter as an example, we can show the difference between these types as follows:

	TC74HC04A	TC74HCU04A	TC74HCT04A
Logic Diagram			
Input–Output Voltage transfer characteristics			

(3) Function

Functions are expressed by Arabic numbers of two to five figures.

In the case of TC74HC series, these numbers are the same as LSTTL and 4000B/4500B devices having the same pin connections and function.

00~999 ····· Product with same pin connections and function as 74LS series.
(Example) 74LS240↔74HC240

4000~40199 ····· Product with same pin connection and function standard
4500~4599 CMOS 4000B/4500B series.
(Example) 40102B↔74HC40102

4300~4399 ····· Function unique to 74HC series.
7000~7999 However, some function approaches LSTTL or 4000B series.
(Example) Same function with 74HC7266A↔74LS266.
However, output is of normal buffer structure (Not open drain).

(4) Revision Level

This symbol is used to clarify the revision of product when improvements which change the characteristics of product are made. Normally, it is blank, however, upon revision, English characters are given successively from "A". Suffix "A" of TC74HCxxxA series indicates the types which have refined AC characteristics due to redesign of IC chip but still meet JEDEC standards for the family.

(5) Package Type

English characters showing type of package.

P ····· dual in line package (DIP) Plastic
F ····· 200 mil small outline IC (SOIC) Plastic
FN ····· 150 mil small outline IC (SOIC) Plastic
FW ····· 300 mil small outline IC (SOIC) Plastic

In the TC74HC series, narrow 300 mil type 24 pin DIP package have been developed. Therefore all P type, 14/16/20/24 pins devices have a 300 mil width (7.62 mm).

(6) Other information

As an example, in the case of SOIC Tape and Reel specifications, the following suffixes are added to the part number.

(TP 1) or (TP 2)	Adhesive Tape and Reel (Difference in pin 1 position)
(EL)	Embossed Tape and Paper Reel.
(ELP)	Embossed Tape and Plastic Reel for 150/200/300 mil SOIC

4. EXPLANATION OF RATINGS AND STANDARDS

4-1 Maximum Ratings

In general, the maximum rating value should not be exceeded in order to guarantee the life and reliability of integrated circuit products.

The Absolute Maximum Rating should not be exceeded even for a moment.

When the device is used in excess of any maximum rating, the device may not recover, and, in many cases, permanent damage will occur.

In designing the circuit, therefore, it is necessary to pay attention to the fluctuation of supply voltage, characteristics of interconnecting parts, ambient temperature, and surges in input and output signal lines, so that the maximum ratings will not be exceeded.

Table 4-1 indicates common absolute maximum ratings of the TC74HC series. When the maximum ratings and common ratings differ, the former shall control. For definition of parameters, refer to Table 4-2.

Table 4-1 Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25 (standard type) ± 35 (buffer type)	mA
DC V_{CC}/Ground Current	I_{CC}	± 50 (standard type) ± 75 (buffer type)	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

* 500mW in the range of Ta=−40℃∼ 65℃. From Ta=65℃to 85℃ a derating factor of−10mW/℃ shall be applied until 300mW.

Table 4–2

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	The voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
DC Input Voltage DC Output Voltage	V_{IN} V_{OUT}	The voltage range in which the IC does not present breakdown, deterioration of characteristics or reduced reliability.
Input Diode Current Output Diode Current	I_{IK} I_{OK}	The current value at which the IC does not present breakdown due to latch-up when input or output current flows. * Practically, a design in which DC current flows is not recommended. When a flow of current cannot be prevented, adopt a current value lower than this.
DC Output Current DC V_{CC}/Ground Current	I_{OUT} I_{CC}	Output current indicates the current value which can flow from one output. As V_{CC}/GND current includes output current, in an IC having many output terminals, substantial V_{CC}/GND current can flow.
Power Dissipation	P_D	Indicates power consumption which exceeded can cause breakdown of the device over the entire operating temperature range.
Storage Temperature	T_{stg}	The ambient temperature range over which deterioration of characteristics and reliability will not occur when left for a long time in a state without supply voltage.
Lead Temp. and Time	T_L	Indicates the maximum allowable conditions permitted when soldering is carried out after IC mounted on printed board.

4–2 Recommended Operating Conditions

These are the conditions in which the operation of the TC74HC series is guaranteed, and when exceeded, operation is not guaranteed even though they are within the maximum rating of Table 4-1.

Common, recommended operating conditions of the 74HC series are shown in Table 4-3. When recommended operating conditions for specific devices and common recommended operating conditions differ, the former shall control. Refer to Table 4-4 for definitions.

Table 4–3 Common Recommended Operating Conditions

(a) 74HC Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

(b) 74HCT Type

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

Table 4−4

Parameter	Symbol	Explanation
Supply Voltage	V_{CC}	**The supply voltage range guaranteeing normal operation of the IC.**
Input Voltage **Output Voltage**	V_{IN} V_{OUT}	**The input/output voltage range guaranteeing normal operation of the IC.**
Operating Temperature	T_{opr}	**The operating temperature range guaranteeing normal operation and electrical characteristics of the IC.**
Input Rise and Fall Time	t_r, t_f	**The rise and fall time range of the input signal which will not cause oscillation of the output.**

4−3 DC characteristics

Table 4-5 shows the DC characteristics of HC types. For the meaning of each parameter, refer to Table 4-7. Table 4-5 is a standard DC characteristics table, and when it differs from individual characteristics, the later shall control. DC characteristics are established by JEDEC (Standard 7A). Table 4-6 indicates characteristics table standardized by JEDEC.

Table 4–5 TC74HC series DC Characteristics Table

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level ** Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level ** Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA*	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA*	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA*	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA*	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current**	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	−	−	1.0	−	10.0	
			FF	6.0	−	−	2.0	−	20.0	
			MSI	6.0	−	−	4.0	−	40.0	

Note) * Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}|$=I_{OL}=6mA, 7.8mA)

** Items guaranteed to exceed JEDEC standard 7A.

Table 4-6 JEDEC Standard No.7A (DC Electrical characteristics)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.3	−	0.3	V
				4.5	−	−	0.9	−	0.9	
				6.0	−	−	1.2	−	1.2	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	−	−	1.9	−	V
				4.5	4.4	−	−	4.4	−	
				6.0	5.9	−	−	5.9	−	
			I_{OH} =−4 mA*	4.5	3.98	−	−	3.84	−	
			I_{OH} =−5.2mA*	6.0	5.48	−	−	5.34	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	−	0.1	−	0.1	V
				4.5	−	−	0.1	−	0.1	
				6.0	−	−	0.1	−	0.1	
			I_{OL} =4 mA*	4.5	−	−	0.26	−	0.33	
			I_{OL} =5.2mA*	6.0	−	−	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND	GATE	6.0	−	−	2.0	−	20.0	
			FF	6.0	−	−	4.0	−	40.0	
			MSI	6.0	−	−	8.0	−	80.0	

Note) • Buffer Type assumes 1.5 times value, respectively.
($|I_{OH}|$=I_{OL}=6mA, 7.8mA)

Table 4-7

Parameter	Symbol	Explanation
High-Level Input Voltage	V_{IH}	The input voltage capable of setting the input of the IC to a high level, and the minimum value is guaranteed.
Low-Level Input Voltage	V_{IL}	The input voltage capable of setting the input of the IC to a low level, and the maximum value is guaranteed.
High-Level Output Voltage	V_{OH}	The output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the corresponding output level goes high. There is guaranteed a minimum value of output voltage obtainable when the specified output current (I_{OH}) flows.
Low-Level Output Voltage	V_{OL}	The output voltage such that when each input terminal is connected to V_{IH} or V_{IL}, the corresponding output level goes low. In this case, there is guaranteed a maximum value of output voltage obtainable when the specified output current I_{OL}) flows.
Input Leakage Current	I_{IN}	This is the current flowing at the input terminal when a voltage is impressed on the input terminal of IC. Normally, this current is so small that measurement is made with the maximum value of supply voltage.
3-State Output Off-State Current	I_{OZ}	The leakage current flowing at the output terminal when the output is in a high impedance state, the device having a three state or open drain output.
Quiescent Supply Current	I_{CC}	The current flowing from the V_{CC} terminal into the IC when the V_{CC} or GND level is held constant without changing the input voltage. The maximum value under all theoretical conditions allowable for the measured IC is guaranteed.

4–4 AC Characteristics

AC characteristics guarantee the transient characteristic of products.

In general, impressed input waveform is set so as to have an amplitude of V_{CC} to GND and rise and fall time of 6ns.

Table 4–8 explains the meaning of each parameter of the AC characteristics, Fig. 4–1 shows the output connection diagrams for measurement and Fig. 4–2 illustrates the measured waveforms.

Table 4–8

Parameter	Symbol	Explanation	Drawing NO.	
			HC	HCT
Output Transition Time	t_{TLH} t_{THL}	Indicates the time during which the output voltage (V_{OH}, V_{OL}) rises from 10% to 90%, and the time during which the output voltage falls from 90% to 10%.	(i)	(iv)
Propagation Time	t_{pLH} t_{pHL}	Indicates the time between input signal application and output response detection. t_{pLH} is the case in which the output changes from low level to high level, and t_{pHL} is the case in which the output changes from high level to low.		
Output Disable Time	t_{pLZ} t_{pHZ}	Indicates the time between when a signal is applied to the output control terminal and when the 3 state output is set to a high impedance state.	(iii)	(vi)
Output Enable Time	t_{pZL} t_{pZH}	Indicates the time, between when a signal is applied to the output control terminal and when the 3 state output switches go a low or high level from the high impedance state.		
Maximum Clock Frequency	f_{MAX}	Indicates the maximum frequency at which the IC operates normally.	(ii)	(v)

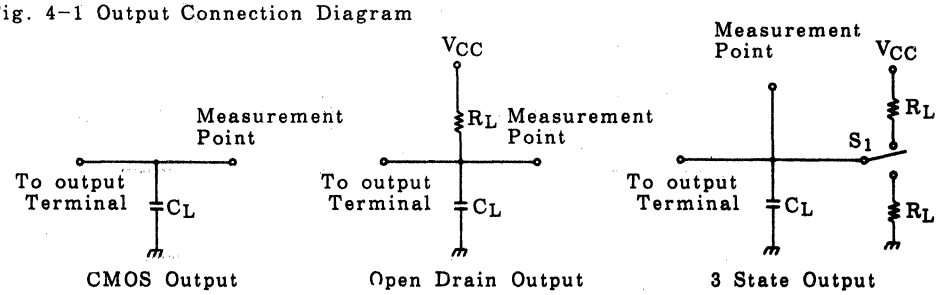
Timing requirements are a prerequisite to the normal function of devices. (See Table 4–9)

Table 4-9

Parameter	Symbol	Explanation	Drawing NO.	
			HC	HCT
Minimum Set-up Time	t_s	Regarding certain data, indicates the time which the data must be applied and held before the input regarding that data (clock, etc.) changes. For example, when the data is read in at a rise of next clock pulse, it is necessary to apply andhold that data before the rising edge of the clock pulse, to a value at least equal to the minimum value of ts.	(ii)	(v)
Minimum Hold Time	t_h	Regarding certain data, indicates the time which the data must be held after the input regarding that data (clock, etc.) has changed.		
Minimum Removal Time	t_{rem}	Indicates the minimum time between releasing of an asynchronous input (clear, preset, etc.) and application of next input (clock, etc.).		
Minimum Pulse Width	t_w	Indicates the minimum pulse width that a clock input, etc. is acceptable as a normal signal.		
Clock Frequency	f	Indicates the clock frequency that is operated the IC normally.		

Perameter	Symbol	Explanation
Input Capacitance	C_{IN}	Indicates the capacitance between input and GND.
Output Capacitance	C_{OUT}	Indicates the capacitance associated with a 3 state output or a open drain output in the high impedance state.

Fig. 4-1 Output Connection Diagram

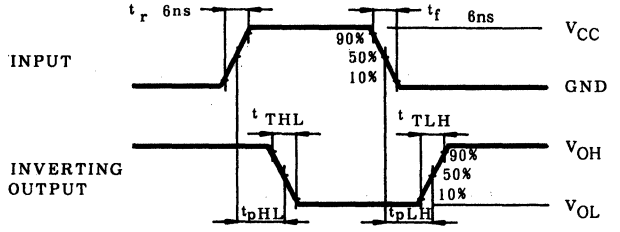


Note) C_L includes the capacitance of probe, etc.

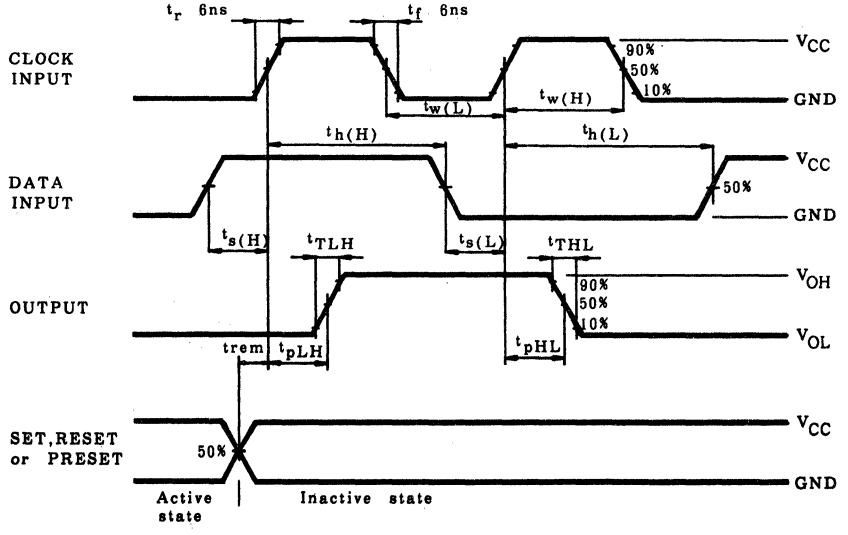
Fig. 4-2 Switching Characteristics Test Waveforms

(1) HC Types

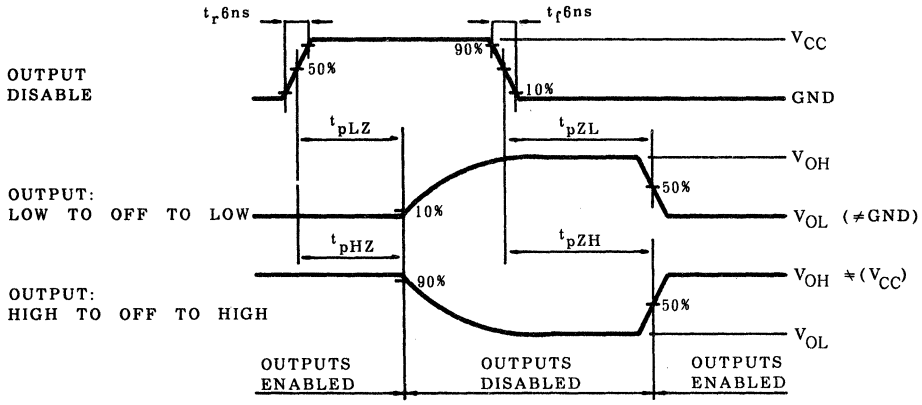
i) t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}



ii) t_w, t_s, t_h, t_{rem}

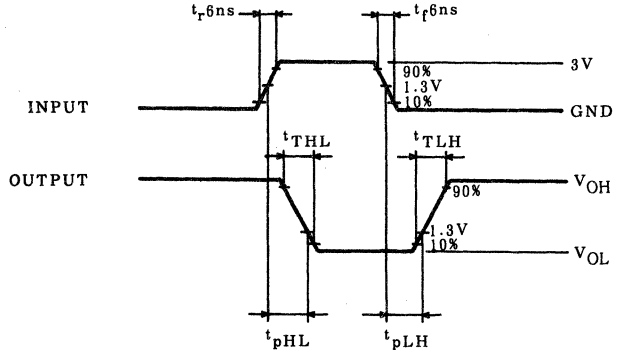


ⅲ) t_{pLZ} ,t_{pHZ} ,t_{pZL} ,t_{pZH}

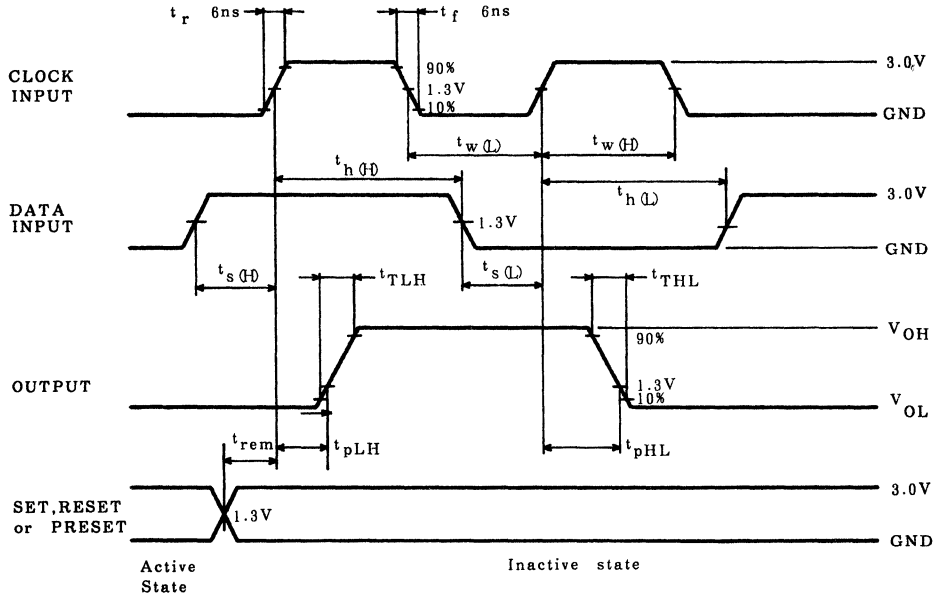


(2) HCT Types

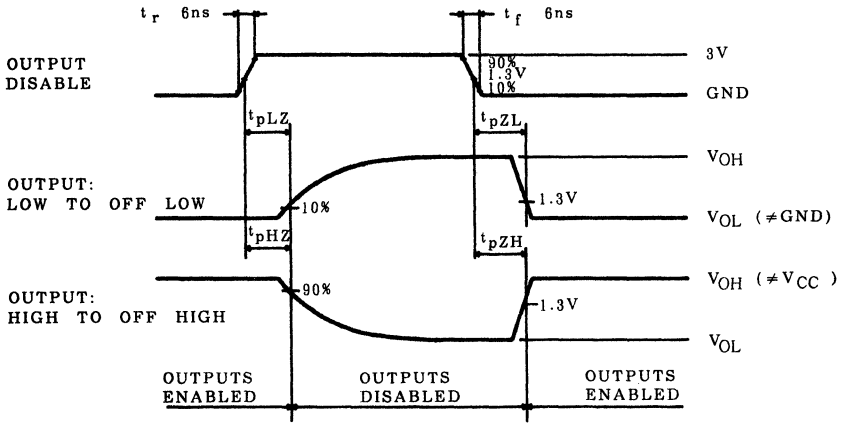
ⅳ) t_{TLH} ,t_{THL} ,t_{pLH} ,t_{pHL}



V) t_w, t_{su}, t_h, t_{rem}



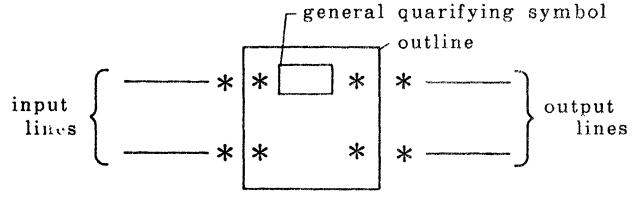
vi) t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



5. EXPLANATION OF IEC LOGIC SYMBOLS

5-1 Symbol composition

A symbol comprises an outline or a combination of outlines together with one or more qualifying-symbols. The purpose of a general qualifying symbol is to accurately portray the logic function of the device.

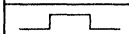
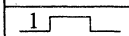
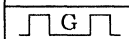
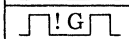
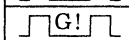
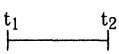


*: qualifying symbol locations for inputs and outputs

5-2 Qualifying Symbols

(1) General Qualifying Symbols

symbol	definition
&	**AND element**
≥1	**OR element**
=1	**EXCLUSIVE OR element**
=	**Logic identify element. If all inputs have the same logic state then the output is at internal logc "1".**
2K	**Even element. If an even number of inputs are at internal logic "1" then the output is at internal logic "1".**
2K+1	**Odd element. If an odd number of inputs are at internal logic "1" then the output is at internal logic "1".**
1	**Buffer element without amplified output.**
▷ or ◁	**Buffer element with amplified output. The triangle points in the direction of signal flow.**

symbol	definition
	Schmitt-trigger. It has hysterisis characteristic.
	Retriggerable monostable element.
	Non-Retriggerable monostable element.
	Astable element
	Synchronous-starting astable element.
	Synchronous-stopping astable element.
SRGm	Shift register. "m" :number of bits.
CTRm	Binary counter. "m" :number of bits. cycle length:2
CTRDIVm	Counter with cycle length m.
RCTRm	Ripple carry counter. "m" :number of bits. cycle length:2
X/Y	Coder or code converter. X and Y may be replaced by appropriate indications of the codes used.
MUX	Multiplexer / data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P-Q	Subtractor.
CPG	Look-ahead carry generator.
π	Multiplier.
COMP	Comparator.
ALU	Arithmetic logic unit.
ROM	Read only memory.
RAM	Random access memory.
FIFO	First-in First-out memory.
I=0	When power is switched ON, the element goes to internal logic "0".
I=1	When power is switched ON, the element goes to internal logic "1".
	Delay element with specified delay times.

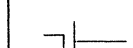
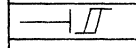
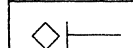
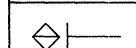
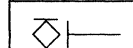
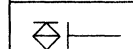
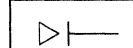
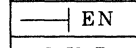
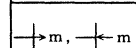
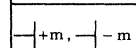
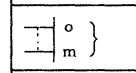
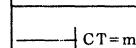
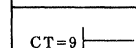
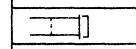
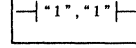
(2) Inputs and Outputs Qualifying Symbols

symbol	definition
	Logic negation at an input. An external logic "0"("1") produces an internal logic "1"("0").
	Logic negation at an output. An internal logic "0"("1") produces an external logic "1"("0").
	Porlarity indicator at an input. A "L"(Low) level active.
	Porlarity indicator at an output. A "L" level active.
	Porlarity indicator at an input where the signal flow is from right to left.
	Porlarity indicator at an output where the signal flow is from right to left.
	Indicator for direction of signal flow.
	Bidirection information flow (alternate).
	Dynamic input Positive logic. Negative logic. Porlarity indicate. The above transitions produce the internal logic active.
	Dynamic input Positive logic. Negative logic. The above transitions produce the internal logic active.
	Dynamic input Porlarity indicate. The above transitions produce the internal logic active.
	Non-logic connection.
	Input for analog signals.

(3) Symbols of the internal connection

symbol	definition
	A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Negated internal connection. A logic "1" at the left-hand side produces a logic "0" at the right-hand side.
	Dynamic internal connection. A transition from internal logic "0" to internal logic "1" at the left -hand side produces a transistory logic "1" at the right-hand side.
	Internal input (virtual). This input is always at internal logic "1" state unless this is overridden or modified.
	Internal output (virtual). This effect on the internal input connected to this output must be indicated by dependency notation.

(4) Symbols inside the outline

symbol	definition
	Delayed output. The output change is delayed until the input that indicated the change returns to its initial external state or level.
	Schmitt trigger input.
	Open-drain output without internal pulled-up resistor.
	Open-drain output with internal pulled-up resistor.
	Open-source output without internal pulled-down resistor.
	Open-source output with internal pulled-down resistor.
	Three-state output.
	Buffered output. (The triangle points in the direction of signal flow)
	Enable input.
J, K, D	Information inputs of disable elements.
R, S, T, C	Control inputs of disable elements.
	Shift input. The direction of shift is to the right or down when the arrow points to the right, or to the left. "m"=1,2,3,···, however, the number may be omitted when "m"=1.
	Counting input. Count-up or count-down are indicted by + and − respectively. The number "m" is the count per command and may be omitted when "m"=1.
	Bit-grouping symbol. "m" is the highest power of 2 in the group.
	Content input. The internal logic "1" sets the element to the value "m".
	Content output. For example, when the input state is "1", the internal registor sets "9".
	Line-grouping symbol. The inputs enclosed by this symbol from a single logic input.
	Fixed-mode input, Fixed-state output. This input (output) is permanently at internal logic "1".

5-3 Dependency Notation

Dependency notation is the powerful tool that makes IEC Logic Symbols compact and yet meaningful. With IEC symbols, the relationships between inputs and outputs are clearly illustrated without the necessity of showing all elements and interconnections involved.
In dependency notation, the terms "affecting" and "affected" are used.

(1) These general rules applied to dependency notation:

1) The input (or output) affecting other inputs or outputs is labelled with the letter symbol that indicates the relationship involved followed by an appropriately chosen identifying number.

2) Each input or output affected by that affecting input (or output) is labelled with that same number.

3) If it is the complement of the input's (or output's) internal logic state that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs.

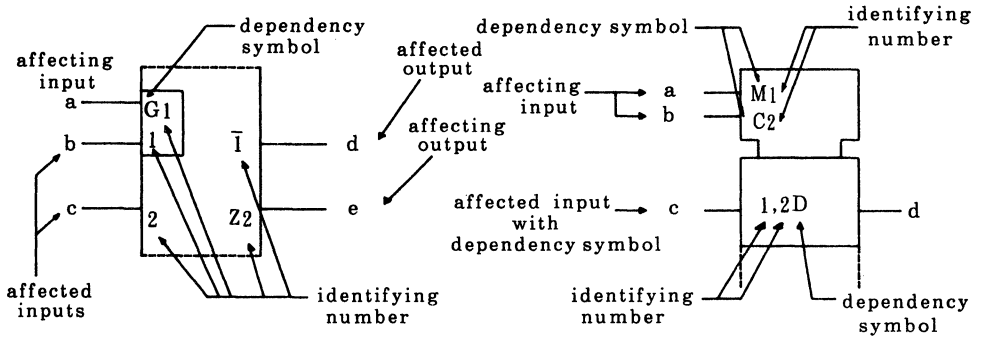
4) If the affected input or output has a label to denote its function, this label will have the identifying number of the affecting input as a prefix.

5) If two affecting inputs or outputs have the same letter and the same identifying number, they are ORed together.

6) If the labels denoting the function of affected inputs or outputs are numbers (example: outputs of a coder), the identifying number of both affecting inputs and affected inputs or outputs is replaced by another character selected to avoid ambiguity, e.g., Greek letters.

7) If an input or output is affected by more than one affecting input, each identifying number separated by a comma will appear in the label of the affected one. The normal order of reading these numbers is the same as the sequence of the affecting relationships.

Fig. 5-1 Example for dependency notation



(2) Symbols for dependency notation

function	symbol	Input State "1"	Input State "0"
AND	G	Permits action	Imposes "0" state
OR	V	Imposes "1" state	Permits action
Negate (EX-OR)	N	Complements state	No effect
Interconnection	Z	Imposes action	Permits action
Control	C	Permits action	Prevents action
Set	S	S=1, R=0	No effect
Reset	R	S=0, R=1	No effect
Enable	EN	Permits action	Prevents action of input
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Address	A	Permits action (Address selected)	Prevents action (Address not selected)

6. HOW TO READ MIL TYPE LOGIC SYMBOLS AND TRUTH TABLES

6-1 How to read MIL type Logic Symbols

Table 6-1 shows the MIL type logic symbols used in high-speed CMOS IC. This logical chart is based on MIL-STD-806B. Clocked inverters and transmission gates employ specific symbols.

Table 6-1 MIL Logic Symbols

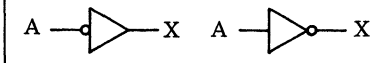
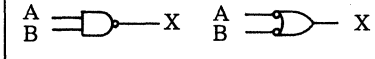
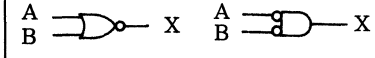
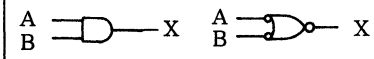
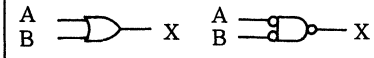
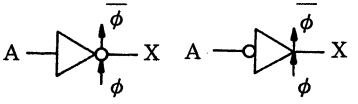
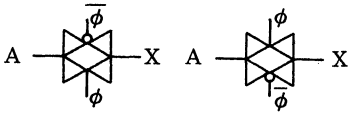
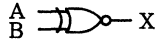
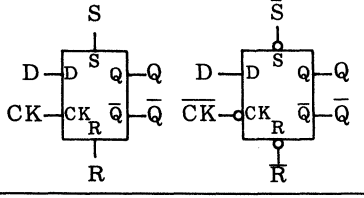
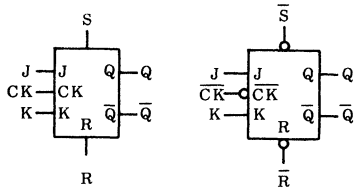
Circuit Function	Logic Symbol	Logical Equation or Truth Table
Inverter		$X=\overline{A}$
NAND Gate		$X=\overline{A \cdot B}=\overline{A}+\overline{B}$
NOR Gate		$X=\overline{A+B}=\overline{A} \cdot \overline{B}$
AND Gate		$X=A \cdot B=\overline{\overline{A}+\overline{B}}$
OR Gate		$X=A+B=\overline{\overline{A} \cdot \overline{B}}$
Clocked Inverter (Note 1)		ϕ | A | X H | H | L H | L | H L | X | Z X:Don't Care Z:High Impedance
Transmission Gate (Note 2)		ϕ | A | X H | H | H H | L | L L | X | Z X:Don't Care Z:High Impedance
EXCLUSIVE-OR Gate		$X=(A+B) \cdot (\overline{A}+\overline{B})$
EXCLUSIVE-NOR Gate		$X=(A \cdot B)+(\overline{A} \cdot \overline{B})$
D-Type Flip-Flop		S | R | D | CK | Q H | L | X | X | H L | H | X | X | L L | L | H | ↓ | H L | L | L | ↓ | L L | L | X | ↑ | Qn△ X:Don't Care △:No Change

Table 6–1 (Cont'd)

Circuit Function	Logic Symbol	Logical Equation or Truth Table
J/K Type Flip–Flop		S R J K CK Q H L X X X $\overline{Q}$ L H X X X L L L L L ↓ Qn△ L L L H ↓ L L L H L ↓ H L L H H ↓ $\overline{Qn}$▽ L L X X ↑ Qn△ X:Don't Care △:No Change ▽:Toggle

Note 1) Clocked Inverter

A clocked inverter has the circuit shown in Fig. 6-1. In this figure, Q1 and Q2 are P-channel MOS FET, and Q3 and Q4 are N-channel MOS FET, and the four FET are connected in series from V_{CC} to GND.

If Ø signal is high, Q1 and Q4 turn on, and the circuit can be regarded as simply an inverter composed of Q2 and Q3. When Ø signal is low, both Q1 and Q4 turn off, and, regardless of the condition of the A input, the output, B is set to a high impedance condition cut off from both V_{CC} and GND.

That is to say, a clocked inverter can be used as a switch to turn off input and output.

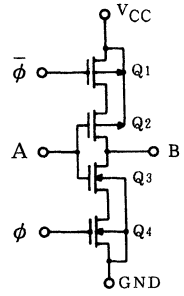


Fig. 6–1 Clocked Inverter

Note 2) Transmission Gate

A transmission gate has the circuit shown in Fig. 6-2. As shown, Q1 is a P-channel MOS FET and Q2 is an N-channel MOS FET which are connected in parallel.

If Ø signal is high, both Q1 and Q2 turn on, and a signal can be applied in either direction.

If Ø signal is low, both Q1 and Q2 turn off, and no signal can be passed.

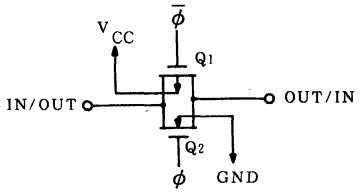


Fig. 6–2 Transmission Gate

6–2 How to Read Truth Table

Table 6–2 indicates the definition of symbols described in Truth Table.

Table 6–2

Symbol	definition
H	High level (Indicates stationary input or output)
L	Low level (Indicates stationary input or output)
	Indicates leading edge changing from "L" to "H".
	Indicates trailing edge changing from "H" to "L".
X	Don't cate (Either "H" or "L")
Z	High impedance state
a ····· h	Input level of stationary state of each input of A to H.
Q_0	Level of Q just before the realization of input condition indicated in Truth Table.
Qn	Level of Q just before inputting of active edge ( or )
	One "H" level pulse.
	One "L" level pulse.

7. COMMON ELECTRICAL CHARACTERISTICS

7-1 Power Dissipation

The power dissipation of CMOS device is composed of two components: one static, the other dynamic.

The total power dissipation is the sum of static and dynamic power dissipation.

Static power dissipation is obtained by multiplying quiescent supply current by the supply voltage range (Paragraph 7-1-(1).

Dynamic power dissipation is obtained as shown in paragraph 7-1-(2).

(1) Static power dissipation

In the case of CMOS ICs, under the condition in which the inputs are fixed at V_{CC} or GND level, either the N-channel FET or P-channel FET turns off. For this reason, the current from V_{CC} to GND becomes only the reverse-direction saturated current of the PN junction and the surface leakage current due to the strain in the chip surface, and is a current of less than several nA at room temperature.

Therefore, where the inputs are driven by another CMOS, or the inputs are pulled-down to GND or pulled-up to V_{CC} the static power dissipation can be obtained as follows :

$$P_d\ (DC) = V_{CC} \cdot I_{CC}$$

For HCT devices where specific input pins are driven at LSTTL levels the following applies:

When being driven with a TTL V_{OH} , HCT devices exhibit additional currents (ΔI_{CC}) as specified on HCT device data sheets.

Therefore, the HCT static power dissipation is dependent on the number of inputs to which TTL V_{OH} logic voltage levels are applied and can be obtained as follows:

$$P_d\,(DC) = V_{CC} \cdot I_{CC} + nV_{CC} \cdot I_{Cn} \cdot dn$$

n : the number of input at 0~2.4V (TTL V_{IH} level)

d : duty cycle

ΔI_{CC}: quiescent current when V_{IH} = 2.4V

(Ref. Technical data sheets)

(2) Dynamic power dissipation

The dynamic power dissipation of a MOS IC is calculated by summing "a" and "b" below:

a) The switching current obtained by charge and discharge of each capacitance added to gate output current when the gate in the circuit including the output buffer makes an inversion.

b) The through current flowing when the P-channel FET and the N-channel FET which constitute the gate during inversion time turn on briefly at the same time.

When rise and fall times of the input signal are small (about 6ns), through current of the gate is usually negligibly small in comparison with the switching current.

For this reason, the dynamic supply current is governed by internal capacitance of the IC and the charging and discharging current of the load capacity (C_L).

An example is given here for C_L = 0pF.

For the inversion of the internal gate outputs from low to high, it is necessary that the electric charge corresponding to Ci • V_{CC} line to the internal capacitance Ci.

Therefore the value obtained by multiplying Ci • V_{CC} and the output inversion frequency (Frequency = f) within a certain period corresponds to the mean current to be supplied from the V_{CC} line to the IC during that period.

In an actual IC however, several gates operate simultaneously, and their respective internal capacity and inversion frequency are different.

Therefore, dynamic supply current in an IC is as follows:

$$I_{CC}\ (opr.) = V_{CC} \cdot \sum_{1}^{n} f_n \cdot Ci_n$$

fn: frequency of internal operated gate

As fn is divisible by an integer of input frequency (f_{IN}), the gate operating with fn/m frequency can be considered equivalent to the capacitance of Ci/m.

Therefore, the above equation can be rewritten as:

$$I_{CC}\ (opr.) = V_{CC} \cdot f_{IN} \cdot \sum_{1}^{n} Ci/m_n$$

f_{IN} : input frequency

m: integer

The final term is defined as C_{PD}.

Dynamic power dissipation with load capacity is given by the following equation:

$$P_D\,(opr.) = C_{PD} \cdot V_{CC}{}^2 \cdot f_{IN} \cdot C_{PD}$$

Total dynamic power dissipation with load capacity is given by the following equation:

$$P_D\,(opr.) = C_{PD} \cdot V_{CC}{}^2 \cdot f_{IN} + \sum_{1}^{n} (C_L\,n \cdot V_{CC}{}^2 \cdot f_O\,n)$$

C_L : load capacity
f_O : output frequency
n : integer of output

However, in specific applications such as crystal oscillators, supply current characteristics are controlled by through current, and calculation by C_{PD} can not be used.

7-2 Standardized Capacitance Power Dissipation (C_{PD}) Test Procedure

The purpose of the C_{PD} value is to allow the user to estimate actual power consumption of his system. Therefore, the table has been set up to exercise each device in the same manner as it would usually be used. Devices which are separable into independent sections are measured on a "per section" basic, the remaining are measured on a "per device" basis. Each device's unique set up is listed in the Table 7-1, "CPD Test Conditions".

Measurements for all devices are to be made at $V_{CC} = 5.0V$ at Ta = 25°C and, if the devices are tested at a high enough frequency, the DC supply current will contribute a negligible amount to the overall power consumption and can be ignored. For this reason, the power consumption is measured at 1MHz. Any device with 3-state outputs is measured in an enabled state.

In order to determine the C_{PD} of a single section of a device (i.e. one of four gates or one of two flip-flops in a package), the following procedures should be used:

As for the C_{PD} value for devices with a common clock, it can be easily obtained by measuring both the C_{PD} of the device with only one portion of the device active, and the C_{PD} found with all portions active. The C_{PD} value obtained by above two conditions should be shown.

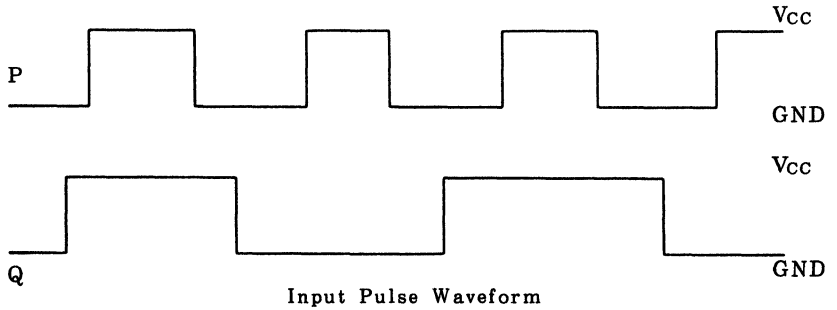
Gates:	Switch one input while biasing the remaining input(s) so that the output(s) will switch.
Flip-flops:	Switch the clock pin while changing the data pin(s) such that the output(s) change with each clock cycle.
Latches:	Switch the enable and data inputs such that the latch toggles.
Decoders/ Demultiplexers:	Switch one address input which changes two outputs.
Date selectors/ Multiplexers:	Switch one address input with the corresponding data inputs at opposite logic levels so that the output switches.

Analog switches:	Switch one address/select input/output which changes two switches. The switch inputs/outputs should be left open. For digital applications where the switch inputs/outputs change between V_{CC} and GND, the respective switch capacitance should be added to the load capacitance as shown above.
Counters:	Switch the clock with the other inputs biased so that the device counts.
Shift registers:	Switch the clock while alternating the inputs so that the device shifts alternation 1's and 0's through the register.
Transceivers:	Switch only one data input. Place transceivers in a single direction.
Monostables:	The pulse obtained with a resistor and no external capacitor is repeatedly switched.
Parity Generators:	Switch one input.
Display Drivers:	Switch one input so that approximately one-half of the outputs change state.
ALUs/Address:	Switch the least significant bit. Bias the remaining inputs so that the device is alternately adding 0000(binary) or 0001(binary) to 1111(binary).

Details of each IC's pin condition are listed in Table 7-1.

-Explanation of symbol-

V = V_{CC} (+5.0V)
G = GND (0 V)
H = logic 1 (V_{CC})
L = logic 0 (GND)
X = don't care. V_{CC} or GND. but not switching
R = 1.0 kΩ pull-up resistor to an additional 5.0V supply other than V_{CC} supply
O = open
P = 50% duty cycle input pulse (shown below)
Q = 50% duty cycle half frequency out-of-phase input pulse (shown below)



Input Pulse Waveform

Table 7-1 C_{PD} Test Condition

Type No.		Pin																					
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
00		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
02		O	P	L	O	X	X	G	X	X	O	X	X	O	V	•	•	•	•	•	•	•	•	•	•
03		P	H	R	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
04		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
08		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
10		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
11		P	H	X	X	X	O	G	O	X	X	X	O	H	V	•	•	•	•	•	•	•	•	•	•
14		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
20		P	H	O	H	H	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
21		P	H	O	H	H	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
27		P	L	X	X	X	O	G	O	X	X	X	O	L	V	•	•	•	•	•	•	•	•	•	•
30		P	H	H	H	H	H	G	O	O	O	H	H	O	V	•	•	•	•	•	•	•	•	•	•
32		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
42		O	O	O	O	O	O	O	G	O	O	O	L	L	L	P	V	•	•	•	•	•	•	•	•
51		P	X	X	X	X	O	G	O	L	L	L	H	H	V	•	•	•	•	•	•	•	•	•	•
73		P	H	H	V	X	X	X	O	O	X	G	O	O	H	•	•	•	•	•	•	•	•	•	•
74		H	Q	P	H	O	O	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•
75		O	Q	X	X	V	X	X	O	O	O	O	G	P	O	O	O	•	•	•	•	•	•	•	•
76		P	H	H	H	V	X	X	X	X	O	O	X	G	O	O	H	•	•	•	•	•	•	•	•
77		Q	X	X	V	X	X	O	O	O	O	G	P	O	O	•	•	•	•	•	•	•	•	•	•
85		L	H	P	H	O	O	O	G	L	L	L	L	L	L	L	V	•	•	•	•	•	•	•	•
86		P	L	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
107		H	O	O	H	O	O	G	X	X	X	X	P	H	V	•	•	•	•	•	•	•	•	•	•
109		H	H	L	P	H	O	O	G	O	O	X	X	X	X	X	V	•	•	•	•	•	•	•	•
112		P	H	H	H	O	O	O	G	O	X	X	X	X	X	H	V	•	•	•	•	•	•	•	•
113		P	H	H	H	O	O	G	O	O	X	X	X	X	V	•	•	•	•	•	•	•	•	•	•
123		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
125		H	P	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
126		H	P	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
131		Q	L	L	P	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
132		P	H	O	X	X	O	G	O	X	X	O	X	X	V	•	•	•	•	•	•	•	•	•	•
133		P	H	H	H	H	H	H	G	O	H	H	H	H	H	H	V	•	•	•	•	•	•	•	•
137		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
138		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
139		L	P	L	O	O	O	O	G	O	O	O	O	X	X	X	V	•	•	•	•	•	•	•	•
147		H	H	H	H	H	O	O	G	O	H	P	H	H	O	O	V	•	•	•	•	•	•	•	•
148		H	H	H	H	L	O	O	G	O	P	H	H	H	O	O	V	•	•	•	•	•	•	•	•
151		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
153		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•

Type No.		Pin																						
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
154		O	O	O	O	O	O	O	O	O	O	O	G	O	O	O	O	O	L	L	L	L	L	P	V
155		L	L	L	O	O	O	O	G	O	O	O	O	P	L	L	V	•	•	•	•	•	•	•	•
157	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
157	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
158	1*	P	L	H	O	L	L	O	G	O	L	L	O	L	L	L	V	•	•	•	•	•	•	•	•
158	4*	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
160		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
161		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
162		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
163		H	P	X	X	X	X	H	G	H	H	O	O	O	O	O	V	•	•	•	•	•	•	•	•
164		Q	H	O	O	O	O	G	P	H	O	O	O	O	V	•	•	•	•	•	•	•	•	•	•
165		H	P	X	X	X	X	O	G	O	Q	X	X	X	X	L	V	•	•	•	•	•	•	•	•
166		Q	X	X	X	X	L	P	G	H	X	X	X	O	X	H	V	•	•	•	•	•	•	•	•
173	1*	L	L	O	O	O	O	P	G	L	L	X	X	X	O	L	V	•	•	•	•	•	•	•	•
173	4*	L	L	O	O	O	O	P	G	L	L	Q	Q	Q	Q	L	V	•	•	•	•	•	•	•	•
174	1*	H	O	Q	X	O	X	O	G	P	O	X	O	X	X	O	V	•	•	•	•	•	•	•	•
174	6*	H	O	Q	Q	O	Q	O	G	P	O	Q	O	Q	Q	O	V	•	•	•	•	•	•	•	•
175	1*	H	O	O	Q	X	O	O	G	P	O	O	X	X	O	O	V	•	•	•	•	•	•	•	•
175	4*	H	O	O	Q	Q	O	O	G	P	O	O	Q	Q	O	O	V	•	•	•	•	•	•	•	•
181		P	H	H	L	L	H	H	L	O	O	O	G	O	B	O	O	O	L	H	L	H	L	H	V
182		H	L	H	L	H	L	O	G	O	O	O	O	P	H	L	V	•	•	•	•	•	•	•	•
190		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
191		X	O	O	L	L	O	O	G	X	X	H	O	O	P	X	V	•	•	•	•	•	•	•	•
192		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
193		X	O	O	H	P	O	O	G	X	X	H	O	O	L	X	V	•	•	•	•	•	•	•	•
194		H	Q	X	X	X	X	X	G	H	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
195		H	H	L	X	X	X	X	G	H	P	O	O	O	O	O	V	•	•	•	•	•	•	•	•
221		L	H	P	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
237		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
238		P	L	L	L	L	H	O	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
242		L	O	P	X	X	X	G	O	O	O	O	O	L	V	•	•	•	•	•	•	•	•	•	•
243		L	O	P	X	X	X	G	O	O	O	O	O	L	V	•	•	•	•	•	•	•	•	•	•
244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
245		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
251		X	X	L	H	O	O	L	G	L	L	P	X	X	X	X	V	•	•	•	•	•	•	•	•
253		L	L	X	X	L	H	O	G	O	X	X	X	X	P	X	V	•	•	•	•	•	•	•	•
257	1*	P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•

* number of sections active

Type No.		Pin																						
		0 1	0 2	0 3	0 4	0 5	0 6	0 7	0 8	0 9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0	2 1	2 2	2 3	2 4
257	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
258	1 *	P	L	H	O	X	X	O	G	O	X	X	O	X	X	L	V	•	•	•	•	•	•	•	•
258	4 *	P	L	H	O	L	H	O	G	O	H	L	O	H	L	L	V	•	•	•	•	•	•	•	•
259		L	L	L	O	O	O	O	G	O	O	O	O	Q	P	H	V	•	•	•	•	•	•	•	•
266		P	L	B	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
273	1 *	H	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
273	8 *	H	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
279		L	P	P	O	X	X	O	G	O	X	X	X	O	X	X	V	•	•	•	•	•	•	•	•
280		L	L	O	L	O	O	G	P	L	L	L	L	L	V	•	•	•	•	•	•	•	•	•	•
283		O	H	L	O	P	H	L	G	O	O	H	L	O	L	H	V	•	•	•	•	•	•	•	•
298	1 *	L	L	H	L	L	L	L	G	L	Q	P	O	O	O	O	V	•	•	•	•	•	•	•	•
298	4 *	L	L	H	H	L	L	H	G	H	Q	P	O	O	O	O	V	•	•	•	•	•	•	•	•
299		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
323		H	L	L	O	O	O	O	O	H	G	Q	P	O	O	O	O	O	X	L	V	•	•	•	•
352		L	L	X	X	L	H	O	G	O	L	L	X	X	P	X	V	•	•	•	•	•	•	•	•
353		L	L	X	X	L	H	O	G	O	L	L	X	X	P	X	V	•	•	•	•	•	•	•	•
354		X	X	X	X	X	X	L	H	L	G	L	L	L	P	L	L	H	O	O	V	•	•	•	•
356		X	X	X	X	X	X	X	Q	P	G	L	L	L	L	L	L	H	O	O	V	•	•	•	•
365		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
366		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
367		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
368		L	P	O	X	O	X	O	G	O	X	O	X	O	X	L	V	•	•	•	•	•	•	•	•
373	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
373	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
374	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
374	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
375		Q	O	O	P	O	O	Q	G	X	O	O	X	O	O	X	V	•	•	•	•	•	•	•	•
377	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
377	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
386		P	L	O	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
390		P	L	O	Q	O	O	O	G	O	O	O	X	O	X	X	V	•	•	•	•	•	•	•	•
393		P	L	O	O	O	O	G	O	O	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
423		L	P	H	O	O	O	O	G	X	X	X	O	O	O	R	V	•	•	•	•	•	•	•	•
533	1 *	L	O	Q	X	O	O	X	X	O	G	G	P	X	X	O	O	X	X	O	V	•	•	•	•
533	8 *	L	O	Q	Q	O	O	Q	Q	O	G	G	P	Q	Q	O	O	Q	Q	O	V	•	•	•	•
534	1 *	L	O	Q	X	O	O	X	X	O	G	P	O	X	X	O	O	X	X	O	V	•	•	•	•
534	8 *	L	O	Q	Q	O	O	Q	Q	O	G	P	O	Q	Q	O	O	Q	Q	O	V	•	•	•	•
540	1 *	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
540	8 *	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•

* number of sections active

Type No.		Pin																						
		00	00	00	00	00	00	00	00	00	11	11	11	11	11	11	11	11	11	22	22	22	22	22
		01	02	03	04	05	06	07	08	09	00	01	02	03	04	05	06	07	08	09	00	01	22	34
541	1*	L	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
541	8*	L	P	P	P	P	P	P	P	P	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
563	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
563	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
564	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
573	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	1*	L	Q	X	X	X	X	X	X	X	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
574	8*	L	Q	Q	Q	Q	Q	Q	Q	Q	G	P	O	O	O	O	O	O	O	O	V	•	•	•	•
590		O	O	O	O	O	O	O	G	O	H	P	H	P	L	O	V	•	•	•	•	•	•	•	•
592		X	X	X	X	X	X	X	G	O	H	P	H	X	H	X	V	•	•	•	•	•	•	•	•
593		O	O	O	O	O	O	O	O	H	G	O	H	P	L	H	X	H	L	H	V	•	•	•	•
595		O	O	O	O	O	O	O	G	O	H	P	P	L	Q	O	V	•	•	•	•	•	•	•	•
597		X	X	X	X	X	X	X	G	O	H	P	X	H	Q	X	V	•	•	•	•	•	•	•	•
620		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
623		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	V	•	•	•	•
640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
643		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
646		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
648		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	X	X	V
651		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	X	X	V
652		X	L	H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	H	X	X	V
670		Q	Q	Q	L	P	O	O	G	O	O	L	L	L	P	Q	V	•	•	•	•	•	•	•	•
688		L	P	L	L	L	L	L	L	L	G	L	L	L	L	L	L	L	L	O	V	•	•	•	•
690		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
691		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
692		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
693		H	P	X	X	X	X	H	H	X	G	L	L	H	H	O	O	O	O	O	V	•	•	•	•
696		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
697		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
698		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
699		H	P	X	X	X	X	L	H	X	G	L	L	H	L	O	O	O	O	O	V	•	•	•	•
4002		O	P	L	L	L	O	G	O	X	X	X	X	O	V	•	•	•	•	•	•	•	•	•	•
4016		O	O	O	O	X	X	G	O	O	O	O	X	P	V	•	•	•	•	•	•	•	•	•	•
4017		O	O	O	O	O	O	O	G	O	O	O	O	L	P	L	V	•	•	•	•	•	•	•	•
4020		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V	•	•	•	•	•	•	•	•
4022		O	O	O	O	O	O	O	G	O	O	O	O	L	P	L	V	•	•	•	•	•	•	•	•
4024		P	L	O	O	O	O	G	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•	•	•
4028		O	O	O	O	O	O	O	G	O	P	X	X	X	O	O	V	•	•	•	•	•	•	•	•

* number of sections active

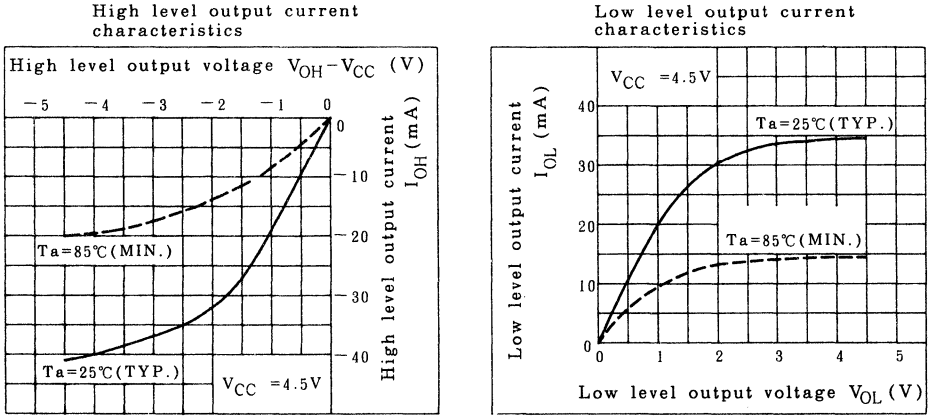
Type No.		Pin																						
		01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
4040		O	O	O	O	O	O	O	G	O	P	L	O	O	O	O	V	•	•	•	•	•	•	•	•
4049		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O	•	•	•	•	•	•	•	•
4050		V	O	P	O	X	O	X	G	X	O	X	O	O	X	O	O	•	•	•	•	•	•	•	•
4051		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
4052		O	O	O	O	O	L	G	G	L	P	O	O	O	O	O	V	•	•	•	•	•	•	•	•
4053		O	O	O	O	O	L	G	G	L	L	P	O	O	O	O	V	•	•	•	•	•	•	•	•
4060		O	O	O	O	O	O	O	G	O	O	P	L	O	O	O	V	•	•	•	•	•	•	•	•
4066		O	O	O	O	X	X	G	O	O	O	O	X	P	V	•	•	•	•	•	•	•	•	•	•
4072		O	P	L	L	L	O	G	O	X	X	X	X	O	V	•	•	•	•	•	•	•	•	•	•
4075		P	L	X	X	X	O	G	L	O	O	X	X	X	V	•	•	•	•	•	•	•	•	•	•
4078		O	P	L	L	L	O	G	O	L	L	L	L	O	V	•	•	•	•	•	•	•	•	•	•
4094		H	Q	P	O	O	O	O	G	O	O	O	O	O	O	H	V	•	•	•	•	•	•	•	•
4316		O	O	O	O	P	X	L	G	G	O	O	O	O	X	X	V	•	•	•	•	•	•	•	•
4351		O	O	O	O	O	O	L	H	O	G	H	P	L	O	L	O	O	O	O	V	•	•	•	•
4352		O	O	O	O	O	O	L	H	O	G	H	P	L	O	O	O	O	O	O	V	•	•	•	•
4353		O	O	O	O	O	O	L	H	O	G	H	P	L	O	L	O	O	O	O	V	•	•	•	•
4511		L	L	H	H	L	L	P	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
4514		H	P	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	L	L	L	V
4515		H	P	L	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	L	L	L	V
4518		P	H	O	O	O	O	L	G	X	X	O	O	O	O	X	V	•	•	•	•	•	•	•	•
4520		P	H	O	O	O	O	L	G	X	X	O	O	O	O	X	V	•	•	•	•	•	•	•	•
4538		G	R	H	P	H	O	O	G	O	O	X	X	L	O	G	V	•	•	•	•	•	•	•	•
4543		H	L	L	H	L	P	L	G	O	O	O	O	O	O	O	V	•	•	•	•	•	•	•	•
7007		P	O	X	O	X	O	G	O	X	O	X	O	X	V	•	•	•	•	•	•	•	•	•	•
7240		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7241		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7244		L	P	O	X	O	X	O	X	O	G	X	O	X	O	X	O	X	O	X	V	•	•	•	•
7266		P	L	O	O	X	X	G	X	X	O	O	X	X	V	•	•	•	•	•	•	•	•	•	•
7292		H	L	O	P	L	O	O	G	O	L	H	O	O	L	L	V	•	•	•	•	•	•	•	•
7294		H	L	O	P	L	O	O	G	O	O	H	O	O	L	L	V	•	•	•	•	•	•	•	•
7640		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
7643		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
7645		H	P	X	X	X	X	X	X	X	G	O	O	O	O	O	O	O	O	L	V	•	•	•	•
40102		P	H	L	L	L	L	L	G	H	L	L	L	L	O	H	V	•	•	•	•	•	•	•	•
40103		P	H	L	L	L	L	L	G	H	L	L	L	L	O	H	V	•	•	•	•	•	•	•	•
40105		L	O	P	Q	Q	Q	Q	G	L	O	O	O	O	O	P	V	•	•	•	•	•	•	•	•

7–3 Output Current Characteristics

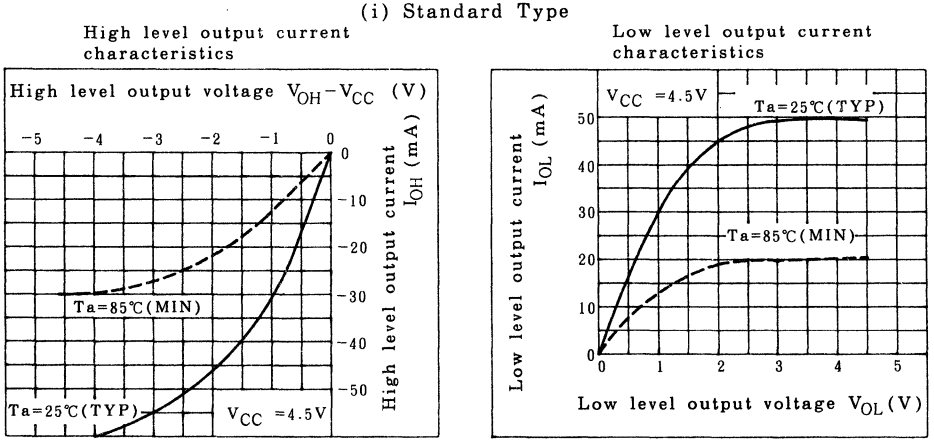
The output current characteristics of TC74HC series can be divided into standard and buffer types. An IC of the standard type is capable of directly driving 10 LSTTL, and guarantees $V_{CC} - V_{OH} \leqq 0.37V$, $V_{OL} \leqq 0.33V$ over the entire temperature range. The buffer type, is capable of directly driving 15 LSTTL under the same conditions.

Fig. 7–2 shows the standard output current characteristics of each type when used at the 4.5V.

Note) The solid line shows standard characteristics. Because there are variations depending upon the samples, use the broken line and separate standard values when making design.



(i) Standard Type



(ii) Buffer Type

Fig. 7–2 Standard Output Current Characteristics

When the structure of the device has been determined, the current flowing in the MOS FET is obtained using the gate voltage V_{GS} and the voltage V_{DS} between source and drain. In an actual IC, the gate voltage of output step MOS FET becomes nearly V_{CC} and GND level. Therefore, if $|V_{GS}| = V_{CC}$ is considered, the following equation is realized in non-saturation zone:

$$I_{DS} = K \left[2 V_{DS} (V_{GS} - V_T) - V_{DS}^2 \right]$$

If V_{DS} is made constant, I_{DS} is proportional to $V_{CC} - V_T$. In the saturation zone:

$$I_{DS} = K (V_{GS} - V_T)^2$$

Thus, I_{DS} is proportional to $(V_{CC} - V_T)^2$ not to V_{DS}. Here, V_T is the threshold voltage proper to the MOS FET's, and is set to a value of about 0.7V in TC74HC series.

Fig. 7-3 shows supply voltage-output current characteristics of standard type outputs. This figure shows standard values. Note that the variation of output current at low supply voltage becomes large in comparison with that at 4.5V.

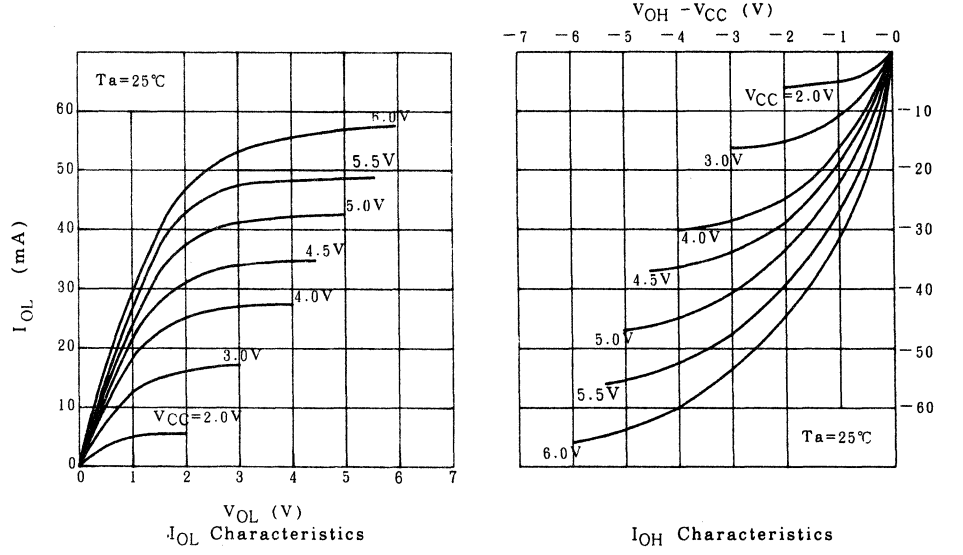


Fig. 7-3 Standard Output Current Characteristics

7–4 AC Electrical Characteristics

(1) Supply voltage dependence

Transient characteristics of IC's such as propagation delay time and maximum operating frequency are determined by delay time of the inner gate or rise and fall time of the output buffer.

Internal delay is considered to be chiefly due to the integral effect of the on resistance of the MOS FET. Load capacitance does not remarkably depend upon supply voltage, the drain current characteristics of MOS FET determine the dependence of AC electrical characteristics to supply voltage.

Fig. 7–4 shows the dependence of propagation delay time on supply voltage in a representative gate IC.

In JEDEC Standard 7A, the coefficient of dependance on supply voltage is determined as follows: In the worst case, adopt the broken line indicated in Fig. 7–4 which was made on the basis of the JEDEC standard.

Table 7–1 Calculation of AC Standard Value (excepting f_{MAX})

V_{CC}	Ta=25℃	Ta=−40～85℃
2.0	5.00X	5.00Y
4.5	X	Y=1.25X
6.0	0.85X	0.85Y

Table 7–2 Calculation of f_{MAX} Standard Value

V_{CC}	Ta=25℃	Ta=−40～85℃
2.0	0.20X	0.20Y
4.5	X	Y=0.80X
6.0	1.18X	1.18Y

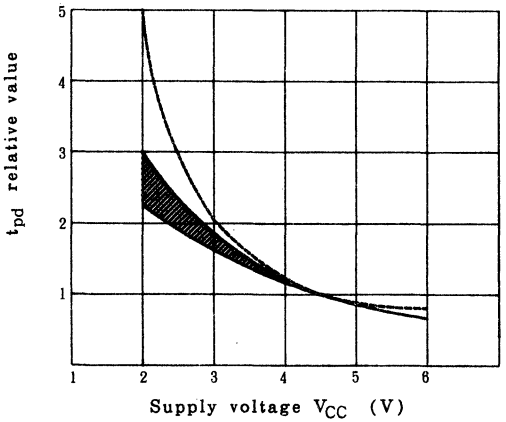


Fig. 7–4 Dependance of Propagation Delay Time on Supply Voltage

(2) Load capacitance dependence

In the TC74HC series, output current has been greatly improved in comparison with the conventional 4000B/4500B series; a capacitive load can be driven at high speed.

However, since the output impedance is determined when supply voltage is selected, the rise and fall time of the output waveform or propagation delay time will increase in proportion to an increase in load capacitance.

Fig. 7–5 indicates the load capacitance dependence on output rise and fall time at a supply voltage of 4.5V. Fig. 7–6 shows the load capacitance dependence on propagation delay time.

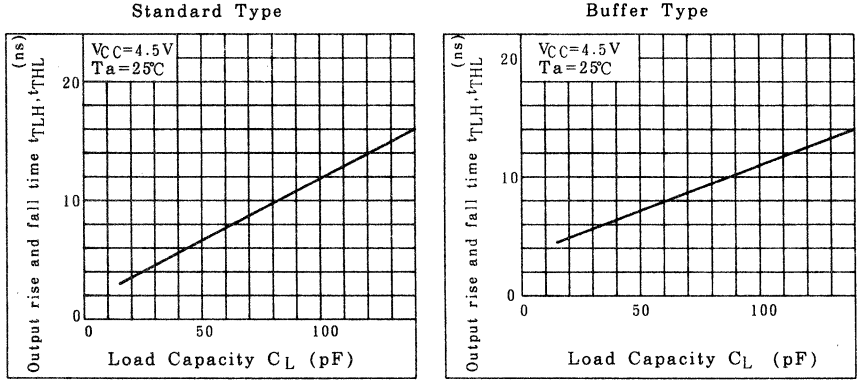


Fig. 7–5 Load Capacitance Dependence of t_{TLH}, t_{THL} (standard characteristics)

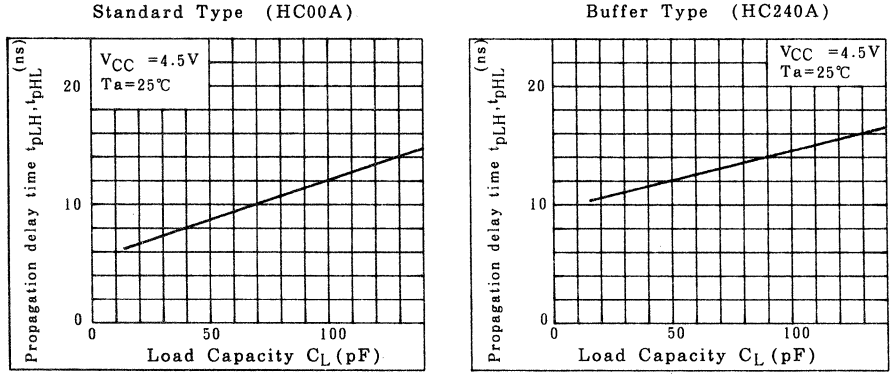


Fig. 7–6 Load Capacitance Dependence of t_{pLH}, t_{pHL} (standard characteristics)

In the TC74HC series, AC characteristics are guaranteed using a load capacitance of 50pF. Propagation delay time using a load capacitance, other than this value is obtained by the following equation:

(Example) High level propagation delay time in the case of load capacitance of XpF.

$$t_{pLH}\ (X) = A\ (X - 50) + t_{pLH}\ (50)$$

A: High level propagation delay time increase rate per unit load capacitance(ns/pF)

Table 7-3 Load Capacitance Dependence of AC Electrical Characteristics (ns/pF)

		Standard Output		Buffer Output	
	V_{CC}	Typical value (Ta=25℃)	Limit value (Ta=25℃)	Typical value (Ta=25℃)	Limit value (Ta=25℃)
t_{TLH}, t_{THL}	2.0	0.33	0.83	0.22	0.55
	4.5	0.12	0.24	0.08	0.16
	6.0	0.09	0.16	0.06	0.11
t_{pLH}, t_{pHL}	2.0	0.17	0.43	0.13	0.33
	4.5	0.06	0.12	0.05	0.10
	6.0	0.043	0.077	0.038	0.068

Table 7-3 shows increase rate per unit capacity of AC electrical characteristics having load capacitance dependence.

In the case of a heavy capacitive load, it is necessary to make the calculation using the limit values in this table.

In TC74HCxxxA series, AC characteristice of 15pF load capacitance (standard output, V_{CC} =5.0V) or 150pF load capacitance (buffer output, V_{CC} =2, 4.5, 6V) is guaranteed. (See the technical data seets)

7–5 Temperature Parameters of Various Characteristics

In TC74HC series, operation over the wide temperature range of −40℃ to 85℃ is guaranteed. This section shows how the switching time and output current are influenced by temperature.

(1) Temperature versus Output Current

Fig. 7–7 indicates temperature versus output current. In this figure, the solid line shows the temperature dependence in a standard sample. When designing, use the broken line as it is the worst case.

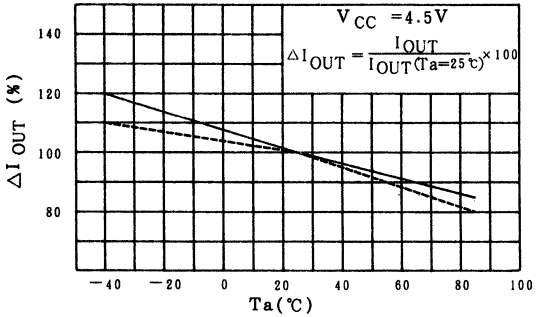


Fig. 7–7

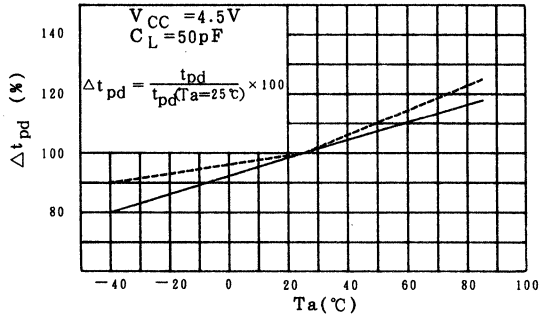


Fig. 7–8

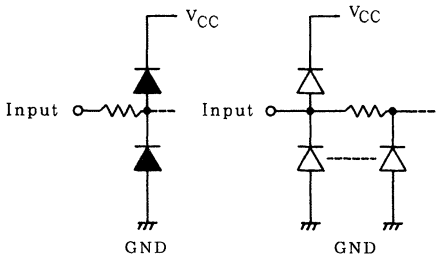
(2) Temperature Characteristics versus Propagation Delay Time

Fig. 7–8 shows temperature versus propagation delay time. The solid line in this figure indicates standard temperature dependence of a gate. When designing, use the broken line indicated as the worst case.

8 PRECAUTIONS IN HANDLING

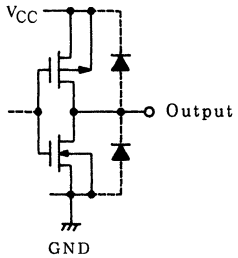
8–1 Electro-Static Discharge

A CMOS IC has a very thin gate insulation oxide film. When high voltage is applied to this gate electrode (input of CMOS IC), the oxide film directly under the gate can sometimes break down. In the TC74HCxxxA series, as shown in Fig. 8–1, protection diodes are added to all input terminals in order to protect CMOS gate from such voltage. However, protective circuits may not be effective against the accidental application of high voltage; care must be taken in handling CMOS IC's.



i) TC74HCxxx ii) TC74HCxxxA

Fig. 8–1 (a) Input Protective Circuits



(b) Output Equivalent Circuit

Further, since a parastic diode is formed between each terminal as indicated in Fig. 8–1, thermal breakdown, etc, due to excessive current may sometimes occur when the voltage exceeding the ratings is applied between each terminal.

(1) Electrostatic Discharge Test Method

Fig. 8–2 shows the electrostatic discharge test method. In Fig. 8–2, the test is conducted with C=200 pF, R=0 Ω. Table 8–1 shows the results of electrostatic discharge tests applied to representative types of the TC74HC series.

In the test method, standardized by EIAJ, it is acknowledged that ± 200V is sufficient to withstand damage in ordinary service. As shown be Table 8–1 Toshiba's TC74HC series has ample protection.

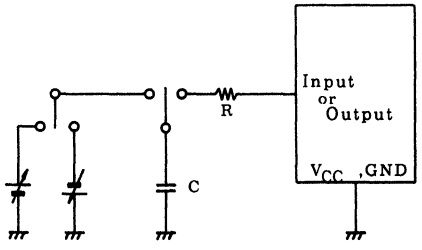


Fig. 8–2 Test Circuit

Table 8-1 Test Result

C=200pF, R=0Ω, Impression frequency 3 times

Name	Output		Input	
	Impression of + voltage	Impression of − voltage	Impression of + voltage	Impression of − voltage
TC74HC00AP	> 500V	> −500V	> 500V	> −500V
TC74HC02AP	> 500V	> −500V	> 500V	> −500V
TC74HC74AP	> 500V	> −500V	> 500V	> −500V
TC74HC139AP	> 500V	> −500V	> 500V	> −500V
TC74HC240AP	> 500V	> −500V	> 500V	> −500V
TC74HC373AP	> 500V	> −500V	> 500V	> −500V

8-2 Precautions in Handling

(1) Transportation and Storage

As the input and output terminals of unmounted CMOS IC's are in a state of high impedance, they are apt to receive induced charges from the surrounding charged body, space electric fields, and the human body.

For this reason, it is necessary, in transporating and storing CMOS IC's, to use dielectric mats, metal cases or aluminum foil boxes, so that each terminal of the IC will be at same potential.

TC74HC series devices are inserted in magazines and are given antistatic treatment at the time of shipment. Do not remove devices from the magazines unnecessarily. Particularly, avoid the use of plastic or vinyl containers which are apt to create static charges.

(2) Assembling

When installing CMOS IC's on the printed wiring board, it is necessary to protect the electric equipment, work stand and assemblers from static electricity by grounding. It is advisable to ground the work stand by placing a metal plate or spreading aluminum foil on the surface. Grounding of assemblers should be made through a resistance of about IMΩ so as to prevent electric shock. Ground through a metallic ring or wrist bands. Also, it is advisable not to wear work clothes made of chemical fibers. Further, it is necessary to periodically check electric equipment to insure absence of electric leakage.

When shaping the leads during the packaging of IC's, it is advisable to use a pincet or similar jig, so that stress may not be given to the device leads at the package entrance.

When storing or transporting the completely assembled printed wiring board, short circuit the terminals of printed wiring board or cover the entire board with aluminum foil, so that the input terminals of the IC are protected.

(3) Soldering

When soldering by use of a soldering iron, carry out the work at temperatures of 260°C or below within 10 seconds. The reliability of TC74HC series is not affected when subjected to a temperature stress at the lead of 260°C for 10 seconds.

Use a soldering iron having no electrical leakage at its end. It is recommended to use a class A iron having an insulation resistance exceeding 10MΩ. When using a soldering tank, it is necessary to ground the tank so as to prevent the electric potential of the soldering tank from affecting the work.

After soldering the IC's on the printed wiring board, cleaning is done to remove flux, etc. For this cleaning use a flux removing solution or a cleaning method utilizing ultrasonic waves. Care must be taken in the selection of the solvent so as to prevent adverse effects on the package and marking of the CMOS IC.

In general, it is advisable to use Freon™ cleaners.

When using ultrasonic cleaning, it is necessary to prevent stress due to signal resonance being imparted to the IC's or printed wiring board. Because of this, it is necessary to consider a method such that the main body becomes a shade against vibration, and also to use a cleaning time of less than 30 seconds.

(4) Adjustment, Test

When making adjustments and tests after the completion of printed wiring board, it is necessary to check for solder bridges or cracks on the printed wiring board before applying power. As CMOS systems require only a small supply current, apply current limiting during test by using a constant voltage power source.

Before inserting or removing printed wiring boards into or out of the test fixture, remove all power.

When inspecting the printed wiring board with a probe, care must be taken to prevent contact of the tip of the probe with other signal or power lines. It is advisable to install a special test device for use with probes.

When a test is conducted under high power and low temperature, it is necessary to ensure that the constant temperature oven is grounded.

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9 PRECAUTIONS IN DESIGNING CIRCUITS

9–1 Input Processing

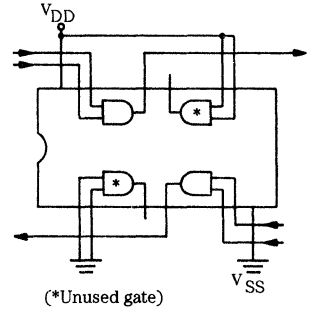
(1) Processing of unused gate

Inputs of CMOS IC have such a high impedance that the logic level becomes undefined under open conditions. If the input is at an intermediate level, the P-channel and N-channel transistors both turn on, and excessive supply current flows.

Therefore, as shown in Fig. 9–1, be sure to connect unnecessary input lines to V_{CC}, GND or other inputs.

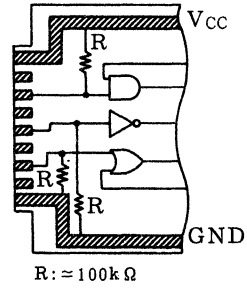
In the case of CMOS, if a soldered part makes poor or no contact, a malfunction of the system or an increase in supply current can occur. Therefore, care must be taken at the time of soldering.

Fig. 9–1 Treatment of Input



(*Unused gate)

When an input terminal of a printed wiring board is connected directly to a CMOS input, that input electrically floats. This condition is the same as a single IC being transported or stored. It is advisable, therefore, to connect this input to V_{CC} or GND through a resistance on the printed wiring board, as shown in Fig. 9–2.



R: ≃ 100kΩ

Fig. 9–2 Input processing of Printed Wiring Board

9–2 Design of Power Source

In general, CMOS has a very small current consumption in comparison with bipolar digital IC's and, therefore, it needs only a small capacity power supply. However, from the operational standpoint, CMOS consumes power in the transition state, and therefore it is necessary to keep the high frequency impedance of the power source as low as possible.

It is advisable to make the wiring of the power source (V_{CC}) and GND lines thick and short, and insert, as a high frequency filter, a 0.001μF to 0.1μF capacitor between V_{CC} and GND for each IC.

Also, it is recommended that a capacitor of about 10μF to 100μF be inserted between the power supply entrance and GND as low frequency filter. As mean supply current differs considerably depending upon the operating frequency of the system, existence of capacitive load, rise and fall of the input signal and supply voltage, attention must be given especially in the case of a simple power source, by using a Zener diode or by battery drive. When there is overshoot or undershoot during the transition time of the power supply, use a filter, etc. so that the maximum device rating is not exceeded.

Output Short circuit

In the TC74HC series, a buffer is added to the output, and both outflow (I_{OH}) and inflow (I_{OL}) current drive is possible. For this reason, excessive current flows in the CMOS output when the high level output line is shorted to GND or the low level output line is shorted to V_{CC}. Particularly, when the supply voltage is high, I_{OH} and I_{OL} are quite excessive and may damage the device; therefore care must be taken not to cause an output short curcuit.

It is, of course, impossible to directly connect ordinary outputs together. But in the case of an IC which has a 3-state output, a wired OR is permitted provided that no more than two outputs are enabled simultaneously.

Further, in order to improve drive capacity, it is possible to connect the gates in the same package as shown in Fig. 9–3.

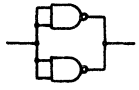


Fig. 9–3 Example of how to increase of drive capacity

9–4 Effect on Input of Slow Rise and Fall Time

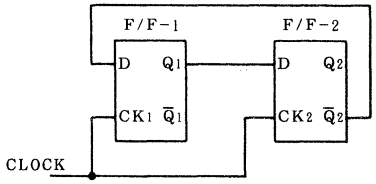
When a slow rise on fall time signal is impressed on a CMOS input, it sometimes happens that the output tends to oscillate around V_{TH} (threshold voltage of the device). This is because the CMOS gate becomes a linear amplifier equivalent in the vicinity of V_{TH}, and minute power source ripple and noise components are amplified and appear in the output.

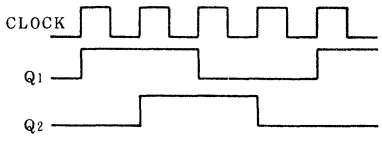
To prevent this, it is necessary to insert a high frequency filter capacitor between V_{CC} and GND of the oscillating IC, or use a Schmitt trigger IC.

In the case of the TC74HC series, excepting HCU types or Schmitt trigger IC's, input rise and fall time is limited as shown in Table 9–1.

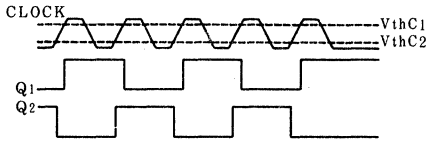
Proper design requires that these rise and fall time limits be observed.

Fig. 9–4 shows an example of a malfunction when a shift counter is designed by using a D-type flip-flop in separate packages. In this case, the malfunction is considered to be caused by the difference in circuit threshold level of separate D-type flip flops.

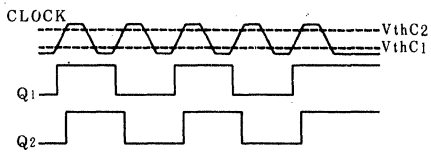




(a) Normal operating waveform



(b) Malfunction waveform from at the time V_{th} C1>V_{th} C2



Malfunction waveform from at the time V_th C1<V_th C2

Fig. 9–4 Example of Malfunction

Let circuit threshold level of F/F-1 be V_{th} C1, and that of F/F-2 be V_{th} C2. Then, as shown in Fig. 9–4, time difference Δt is formed when the rising waveform of the clock pulse cuts the respective circuit threshold voltage, and thus a malfunction occurs.

The following condition is required for ensuring normal operation:

$$\Delta t < t_{pd}\ (CK-Q)+t_{set-up}$$

In this case, there is a possibility of malfunction even though the input signal is within the standard value of Table 9–1. Therefore, care must be taken in design of sequence circuit clock inputs.

Table 9–1 Standard Value of Input Rise and Fall Time

Item	Symbol	Limit	Unit
Input Rise and Fall Time	t_r , t_f	0 ~ 1000(V_{CC} =2.0V) 0 ~ 500(V_{CC} =4.5V) 0 ~ 400(V_{CC} =6.0V)	ns

9–5 Wiring Precautions

(1) Output waveform distortion

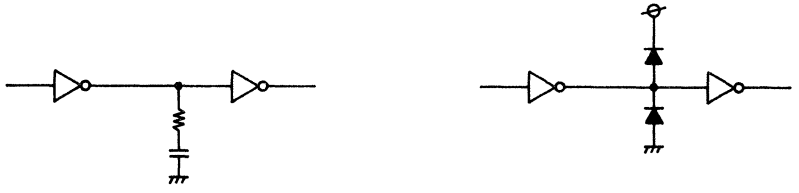
As the output impedance of the TC74HC series is very low in comparison with conventional standard CMOS IC, distortion is sometimes caused in the output waveform depending upon the L component of the wiring, long output wiring, or when capacitance is connected between signal lines and V_{CC} or GND. Therefore, when designing the printed wiring board, take care not to make signal wiring too long. In the case of double sided printed wiring boards, it is ideal to limit signal wire length to 30cm or less. The clock signal line is particularly prone to distortion.

(2) Precautions for part arrangement

The output of TC74HC series has a fast rise and fall time, and makes a full swing between V_{CC} and GND. Therefore it becomes a noise source to other signals. It is necessary to locate the output away from a part which is sensitive to the noise of an analog circuit. Also, care must be taken for the reduction of the number of loads and curtailment of wiring length.

(3) Termination

From its physical and electrical charactersitics, the TC74HC series is apt to cause some overshoot and undershoot, and this can lead to malfunction of the circuit or breakdown of passive IC's. These troubles can be prevented to some extent by terminating the ends of signal lines. Fig. 9–5 indicates examples of termination methods.



(a) Termination by CR (b) Termination by Diode

Fig. 9–5 Examples of Termination

9–6 Interface

(1) Input and output interface

When interconnecting a CMOS system, an exchange of signals with external circuits or mechanisms is usually done. These input and output signal lines are made long in many cases, and have distributed inductance and/or reactance. Therefore, if directly connected to CMOS, they can give rise to various problems.

Conceivable problems can include malfunction due to induced noise, and the destruction of the input/output elements due to surge. To cope with these problems, reduction of signal line impedance (driving impedance) or insertion of a noise eliminating circuit on the receiving side is done for the former problem, while surge protective measures are taken for the latter.

Fig. 9–6 illustrates examples of providing noise and surge protection on the input side.
(a) and (b) show examples of absorbing noise by integrating the input waveform.
(c) and (d) are examples of protecting CMOS from input surge.

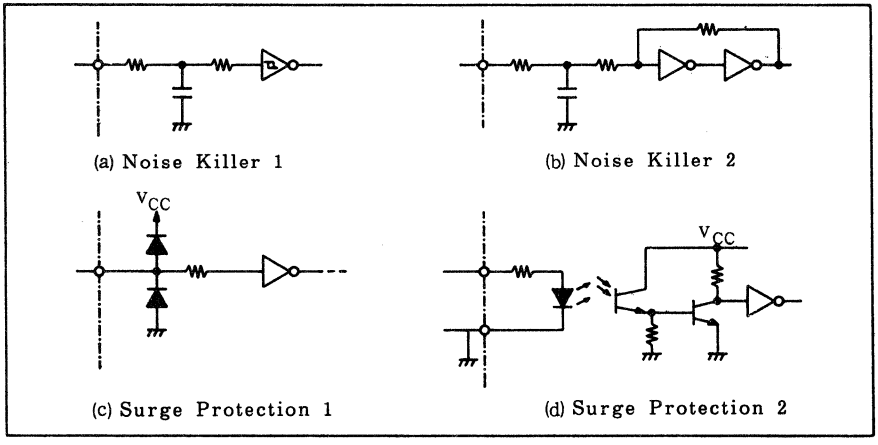


Fig. 9–6 CMOS Input Protective Circuits

Fig. 9–7 gives examples of an output interface. There are other methods, but in any case, some protection scheme should be provided to an interface involving long signal lines.

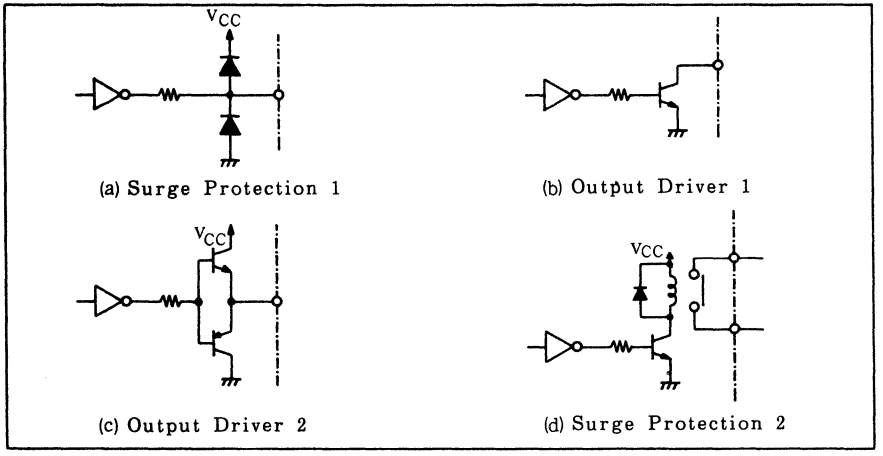


Fig. 9–7 Output Protection/Driving Circuits

(2) Interface between CMOS IC's

When CMOS IC's are interfaced, the input impedance is so large that the limitation of fanout may not be so important. However, there is a need to consider the increase in propagation delay time due to the adding effect of load capacitance and an increase in power consumption.

Input capacitance of CMOS is about 5pF per input. If 10 fan outs are taken for example, the load capacitance is 50pF. Further, the line capacitance of the printed wiring board must also be taken into consideration. This shows that the processing speed of system is controlled not only by the circuit IC's but also by fan out.

When constructing a system with CMOS IC, the designer must examine the fan out and take these points into consideration.

(3) Interface between different CMOS families

The problem to be considered when interfacing different CMOS families is the difference in supply voltage requirements between them. When different CMOS families use the same power source, only problems due to the propagation delay time difference must be considered, but in the case of separate power sources, a voltage level converting circuit is needed.

Fig. 9–8 shows an interface method from the standard CMOS operating at 6V~15V to 74HC. The most popular method is to use CMOS (4049B/4050B) which has a level shift function as shown below:

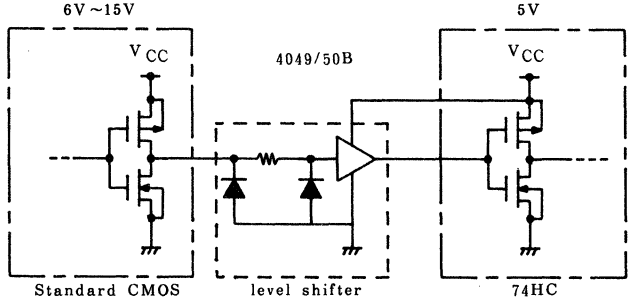
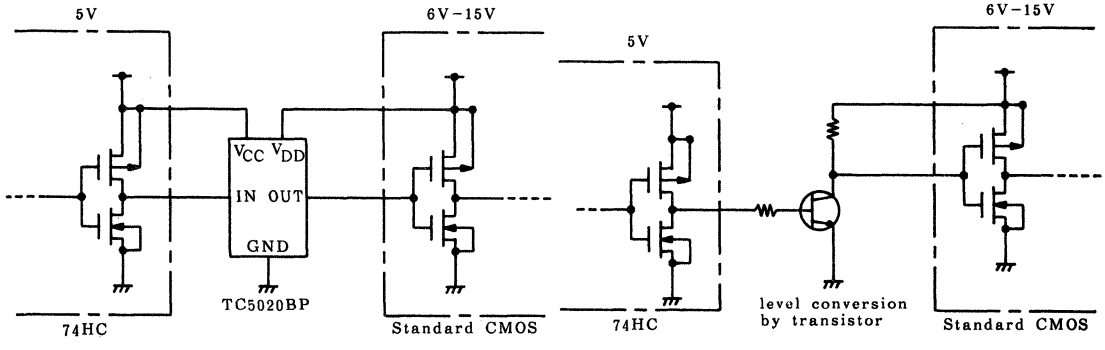


Fig. 9–8 Standard CMOS→74HC Interface

The 4049B/4050B has a GND side diode only, and is so constructed that current does not flow in the power source (V_{CC}) of a 5V system even though a voltage of 15V is impressed.

On the other hand, an interface from 74HC to standard CMOS can be realized by using TC5020BP, a level shift IC, as shown in Fig. 9–9(a). It is also possible to use discrete transistors as in Fig. 9–9(b). The circuit employing discrete transistors can, of course, be used for power inversion.

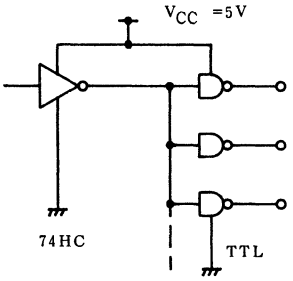


(a) Example of using level shifter IC (b) Example of using transistor

Fig. 9–9 74HC →Standard CMOS Interface

(4) Interface with TTL

When driving TTL with the TC74HC series, input and output voltage levels can be connected without trouble. Fan out is determined by the output current of the CMOS IC and input current of the TTL. An example is shown in Fig. 9–10.



Fan Out Number

	Standard Type	Buffer Type
TTL	2	3
S TTL	2	3
LS TTL	10	15
ALS TTL	20	30

Fig. 9–10 TC74HC → TTL Interface

On the other hand, when driving TC74HC series with TTL, it is necessary to convert the output voltage level of the TTL to the input level of 74HC. Normally, TC74HCT series devices which have same input level as LSTTL are used. The input current of TC74HCT series is very low like that of TC74HC series, and no burden is imposed on the driving side 74LS. Additionally, the speed falls very little. Therefore it can be said to be an effective method. Another method is to use a pull up resistor as shown in Fig. 9–11.

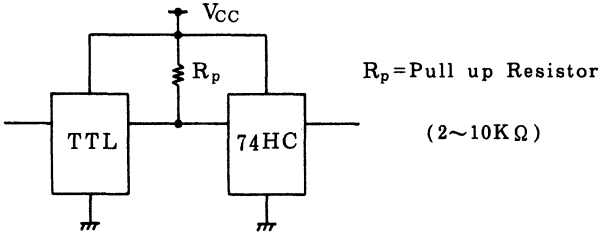


Fig. 9–11 TTL → TC74HC Interface

(5) Interface with CPU

At present, 74LS series TTL is used universally as the peripheral supporting logic for MOS microprocessors. Since the TC74HC series has the same speed as 74LS, it can be used as microprocessor peripheral logic. As an interface with a CMOS CUP there is no problem since both are CMOS. At present, however, the use of NMOS CPU is greater, and the interface of NMOS to CMOS must be taken into consideration.

The output of most NMOS CPU's rises to near V_{CC} but as shown in Fig. 9–12, as outputs of both driving MOS and load MOS are enhancement type, no switching takes place until near V_{CC}. In order to carry out the signal transfer from the NMOS CPU to the 74HC, use the 74HCT series which has a TTL lelve input. When connecting the 74HC series, a pull up resistor is required as shown in Fig. 9–12.

Driving an NMOS CPU from the 74HC series can be done without difficulty. The input of NMOS is high impedance like CMOS, and the DC fan out need not be taken into consideration.

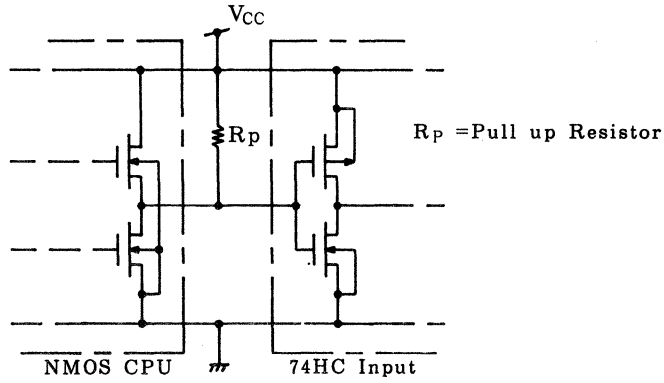


Fig. 9–12 NMOS CPU Interface

9-7 Latch-up

Latch-up is a phenomeon peculiar to CMOS, and is also called SCR (Silicon Controlled Rectifier) Phenomenon. During the normal operation if excessive voltage and current caused by high noise or accidental surge is applied to the input or output terminal, or a supply source suddenly fluctuates, abnormal current flows between V_{CC} and GND, and this current continues to flow even though the disturbing signal is cut off, and, finally, damage is caused. Latch-up is the name given to this phenomenon.

Once latch-up takes place, the original condition is not restored unless the power supply is cut off.

(1) Cause of latch-up

Fig. 9-13 shows as equivalent circuit with the parasitic element. NPN transistor Q_2 is formed in the P-well of NMOS side while PNP transistor Q_1 is formed in the N-substrate of PMOS side, and a parasitic resistor exists between the terminals. As shown from the current path through the medium of the parasitic element, these parasitic elements constitute a Thyristor.

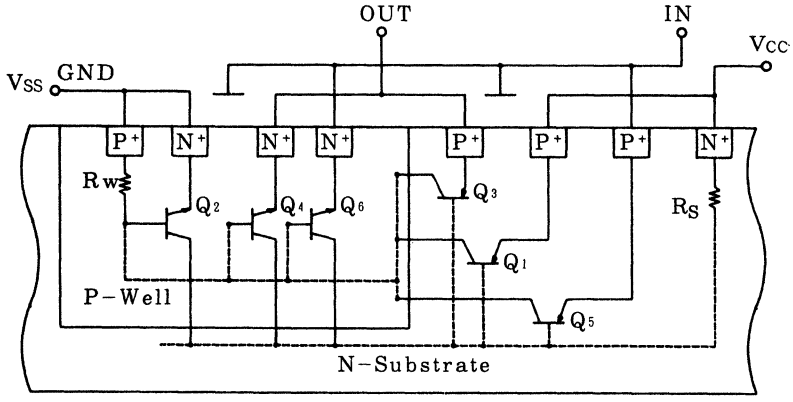


Fig. 9-13 Internal Equivalent Circuit of CMOS IC

For example, if current flows into the N-substrate from external sources, a voltage drop takes place in the resistor Rs of the N-substrate, and this turns on parasitic transistor Q_1, and current flows towards GND from V_{CC} through the medium of resistor Rw in the P-Well. When current flows in Rw, a voltage drop takes place at both ends of Rw, Q_2 turns on, and further supply current flows through Rs. As a result, the voltage drop at both ends of Rs furthers increases, Q_1 and Q_2 are left in the furn-on state, and the supply current continues to increase.

In this way, if the voltage drop takes place in resistance Rw in the P-Well and in resistance Rs in the N-substrate, latch-up occurs, and the following events occur:

1) Input voltage goes higher than $V_{CC} + V_F$
   (Q_5 turns on)

2) Input voltage goes lower than GND $- V_F$
   (Q_6 turns on)

3) Output voltage goes higher than $V_{CC} + V_F$
   (Q_3 turns on)

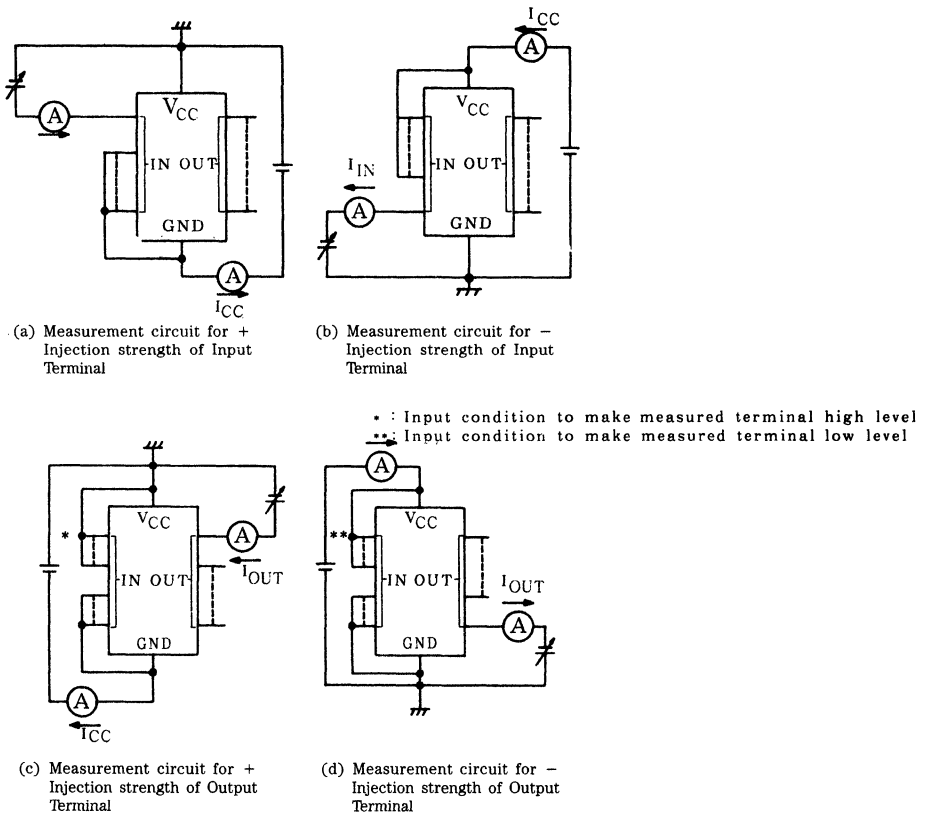
4) Output voltage goes lower than GND $- V_F$
   (Q_4 turns on)

5) This raises supply voltage V_{CC} above the rated value causes breakdown.
   (Directly forces current in Rw or Rs)

Here, V_F is the forward voltage between base and emitter of parasitic bipolar transistor Q_3-Q_4.

(2) Latch-up strength measurement

Fig. 9–14 illustrates a measurement example of latch-up strength. As indicated in Fig. 8–14, latch-up is induced by forcing current into input terminal (+ injection) or forcing current out of output terminal (− injection), and the current value at that time is measured.



(a) Measurement circuit for + Injection strength of Input Terminal

(b) Measurement circuit for − Injection strength of Input Terminal

(c) Measurement circuit for + Injection strength of Output Terminal

(d) Measurement circuit for − Injection strength of Output Terminal

Fig. 9–14 Latch-up Strength Measurement Circuits by Current Feeding System

(3) Countermeasures

As ample margin is provided against latch-up, there is no problem in using the device within the specifications. However, since the part has the possibility of receiving excessive surge current, it is recommended that a protective circuit be added as indicated in Fig. 9–15.

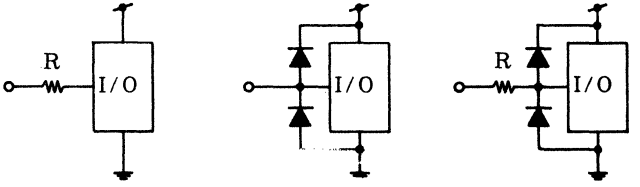


Fig. 9–15 Examples of Latch-up Prevention Methods

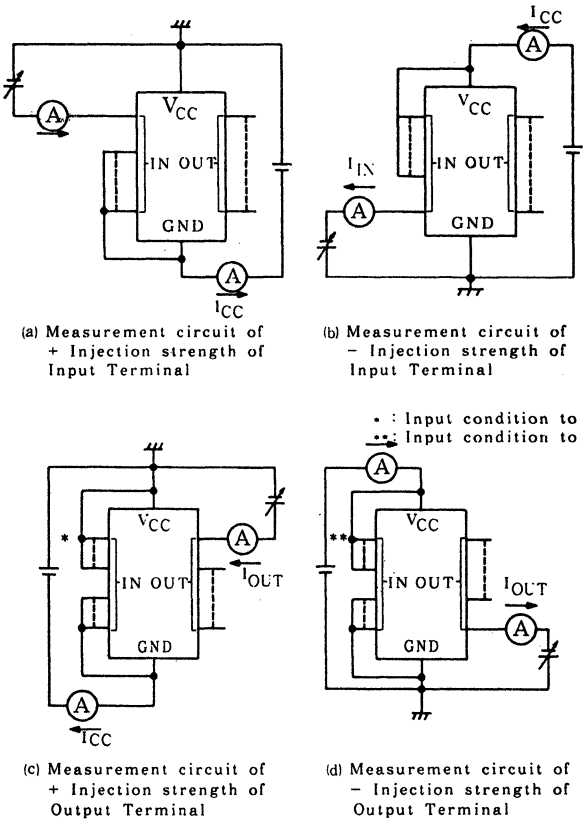


Fig. 9−14 Latch-up Strength Measurement Circuits by Current Feeding System

(3) Countermeasures

As ample margin is provided for latch−up as explained in (2), there is no problem in using the unit within the standards. However, since the interface part has the possibility of receiving excessive surge, it is recommended that the protective circuit be added as indicated in Fig. 9−15.

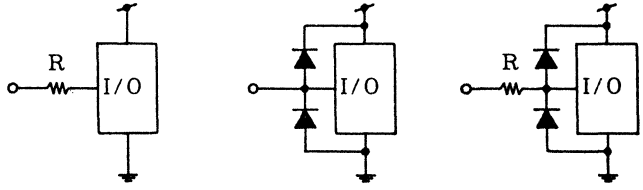


Fig. 9−15 Example of Latch-up Prevention Methods

9 - 8 Metastable Characteristics

When the set-up or hold-time of a flip-flop is violated, the device output response is uncertain. When an asynchronous signal is input to a flip-flop which is clocked by the internal clock of a synchronous system, the system designer cannot guarantee that the set-up and hold-time specifications associated with the flip-flop will not be violated.

hold-time specifications associated with the flip-flop will not be violated.

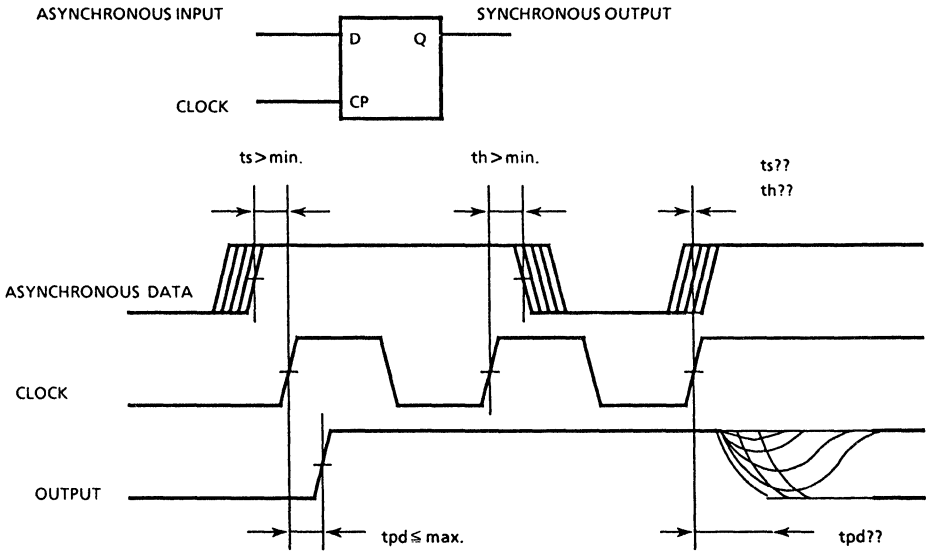


Fig. 9-16 Metastable Timing Diagram

The metastable state is defined as that time period when the output logic level is not at "1", nor at "0", but in the state of between 30% and 70% of V_{CC}.

This metastability is illustrated in the timing diagram of Fig. 9–16.

NOTES

10. DATA SHEETS

TC74HC/HCT SERIES

QUAD 2-INPUT NAND GATE

The TC74HC00A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

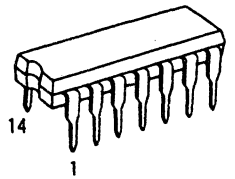
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

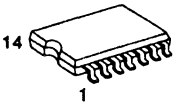
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

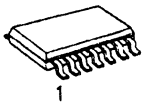
FEATURES:

- High Speed ..... t_{pd}=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS00



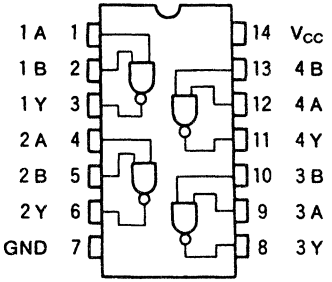
P(DIP14-P-300)





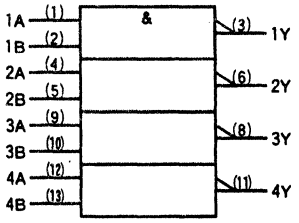
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ～85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	ns
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

QUAD 2-INPUT NAND GATE

The TC74HCT00A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

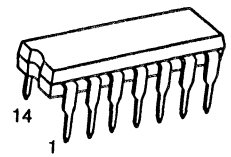
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

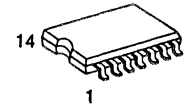
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} = 10ns(Typ.)at V_{cc} = 5V
- Low Power Dissipation ..... I_{CC} = 1 μA(Max.)at Ta=25℃
- Compatible with TTL outputs ..... V_{IH} = 2V(Min.)
  V_{IL} = 0.8V(Max.)
- Wide Interfacing ability ..... LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS00

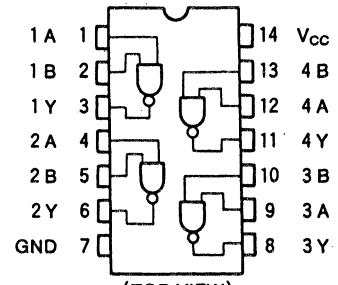


P(DIP14-P-300)



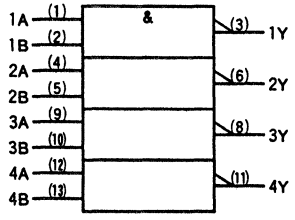
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH}=−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−4 mA	4.5	4.18	4.31	−	4.13	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	1.0	−	10.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	20	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5 5.5	– –	13 12	19 17	– –	24 21	ns
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	19	–	–	–	pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOTES

TC74HC02AP/AF/AFN

QUAD 2-INPUT NOR GATE

The TC74HC02A is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

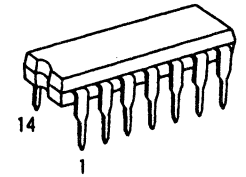
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS02



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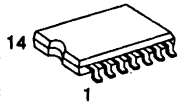
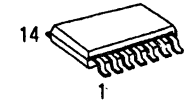
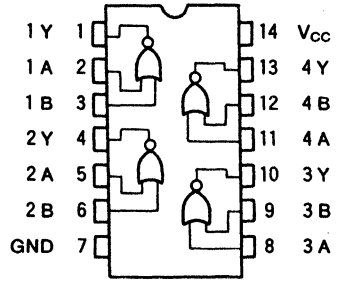




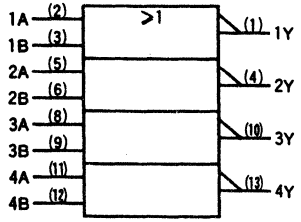
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	21	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

QUAD 2-INPUT NOR GATE

The TC74HCT02A is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

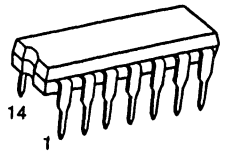
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS.The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}= 9ns(Typ.)at V_{cc}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs ..... V_{IH} =2V(Min.)
  V_{IL} =0.8V(Max.)
- Wide Interfacing ability..... LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS02



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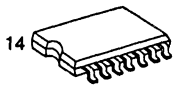
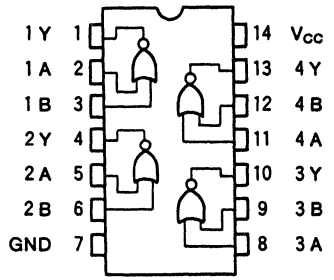


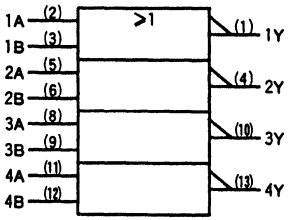
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	1.0	−	10.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	9	15	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40 ~85°C MIN.	Ta=−40 ~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	–	8	15	–	19	ns
			5.5	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	–	12	18	–	23	ns
			5.5	–	11	16	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	17	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOTES

TC74HC03AP/AF/AFN

QUAD 2-INPUT NAND GATE(OPEN DRAIN)

The TC74HC03A is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

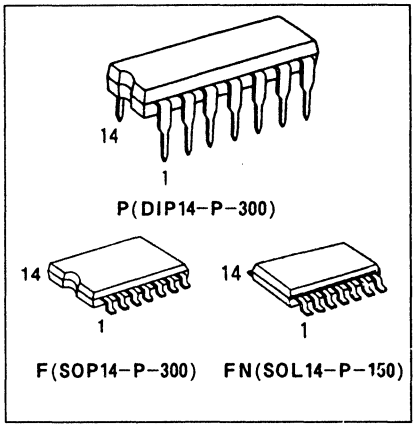
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74 HC00A. But the TC74HC03A has, as its outputs, high performance MOS N-channel transistors. (OPEN-DRAIN outputs) This device can, therfore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other application.

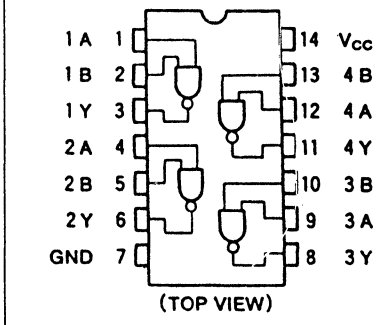
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

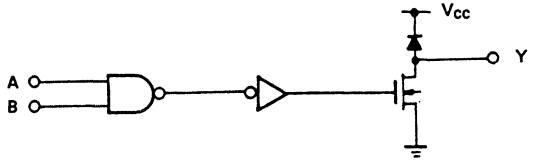
- High Speed ····· t_{pZ} =5ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS03



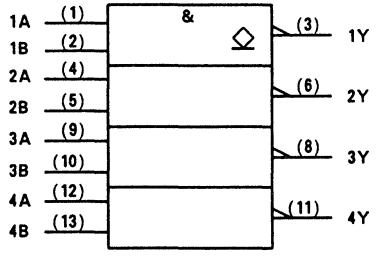
PIN ASSIGNMENT



SYSTEM DIAGRAM(per gate)



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	$+25$	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	–	5	12	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	–	5	12	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	–	20	75	–	95	
			4.5	–	10	15	–	19	
			6.0	–	9	13	–	16	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	–	24	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	5	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC04AP/AF/AFN

HEX INVERTER

The TC74HC04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

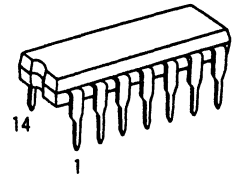
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including buffered output, which provide high noise immunity and stable output.

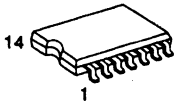
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

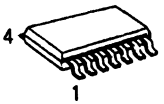
FEATURES:

- High Speed ..... t_{pd}=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS04



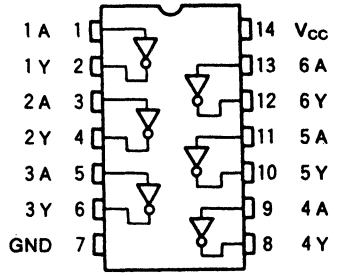
P(DIP14-P-300)





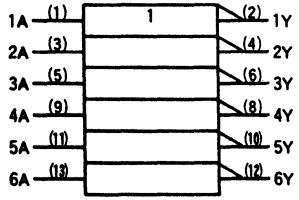
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	ns
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

TC74HCT04AP/AF/AFN

HEX INVERTER

The TC74HCT04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

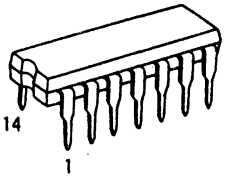
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

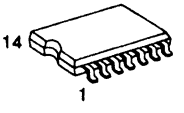
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

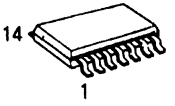
FEATURES:

- High Speed ····· t_{pd}=8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS04



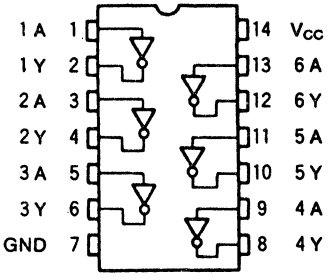
P(DIP14-P-300)





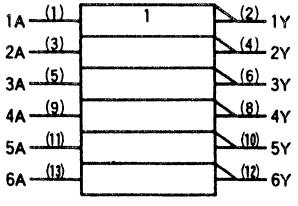
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	1.0	−	10.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 13	– –	19 16	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5 5.5	– –	11 9	18 16	– –	23 20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

TC74HCU04AP/AF/AFN

HEX INVERTER

The TC74HCU04A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

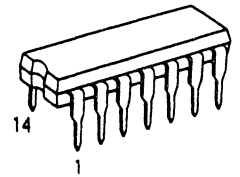
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Since the internal circuit is composed of a single stage inverter, it can be used in analog applications such as crystal oscillators.

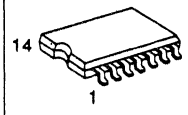
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

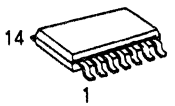
FEATURES:

- High Speed ····· t_{pd}=4ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=10% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS04



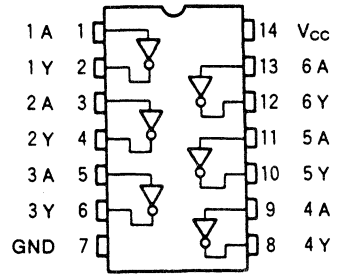
P(DIP14-P-300)





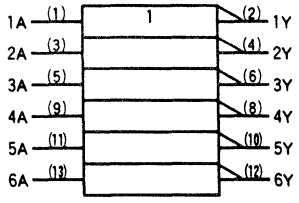
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.7	−	−	1.7	−	V
				4.5	3.6	−	−	3.6	−	
				6.0	4.8	−	−	4.8	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.3	−	0.3	V
				4.5	−	−	0.9	−	0.9	
				6.0	−	−	1.2	−	1.2	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IL}	I_{OH} =−20 μA	2.0	1.8	2.0	−	1.9	−	V
				4.5	4.0	4.5	−	4.4	−	
				6.0	5.5	5.9	−	5.9	−	
		V_{IN} = GND	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} =20 μA	2.0	−	0.0	0.2	−	0.2	V
				4.5	−	0.0	0.5	−	0.5	
				6.0	−	0.1	0.5	−	0.5	
		V_{IN} = V_{CC}	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	4	8	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	18	60	–	75	ns
			4.5	–	6	12	–	15	
			6.0	–	5	10	–	13	
Input Capacitance	C_{IN}			–	9	15	–	15	pF
Power Dissipation Capacitance	C_{PD}(1)			–	13	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

HEX INVERTER (OPEN DRAIN)

The TC74HC05A is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

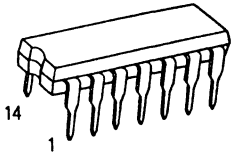
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HC04A, but the TC74HC05A has high performance MOS N-channel transistor (OPEN-DRAIN) outputs. This device can, therfore, with a suitable pull-up rsistors, be used in wired-AND, LED drive and other applications.

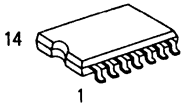
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pZ} =8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS05

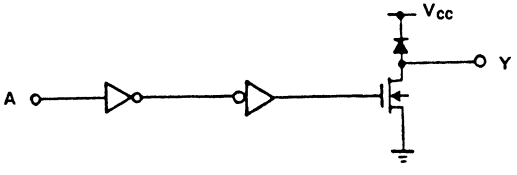


P(DIP14-P-300)

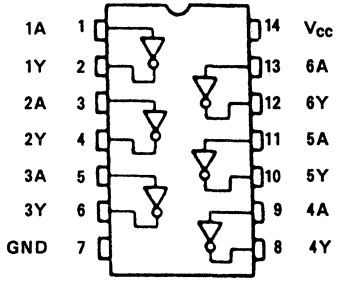


F(SOP14-P-300)

SYSTEM DIAGRAM(per gate)

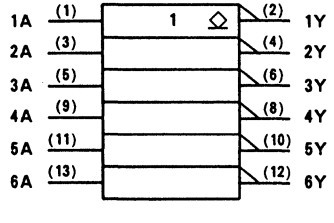


PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	Z
H	L

Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	−	−	±0.5	−	±5.0	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	–	8	15	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	–	6	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	–	20	90	–	115	
			4.5	–	11	18	–	23	
			6.0	–	10	15	–	20	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	–	33	90	–	115	
			4.5	–	9	18	–	23	
			6.0	–	7	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	3	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	7	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

HEX BUFFER (OPEN DRAIN)

The TC74HC07A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.

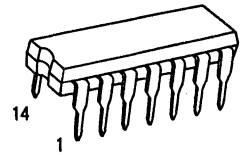
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HCT7007A. But the TC74HC07A has high performance MOS N-channel transistor (OPEN-DRAIN) outputs. This device can, therfore, with a suitable pull-up resistors, be used in wired-AND, LED driver and other applications.

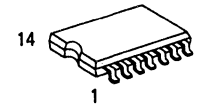
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pZ} =5ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS07

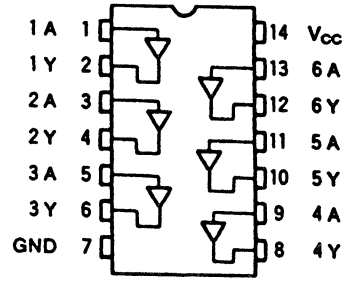


P(DIP14-P-300)



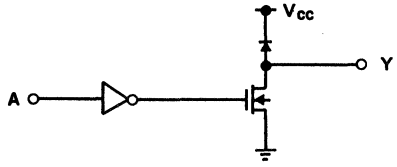
F(SOP14-P-300)

PIN ASSIGNMENT

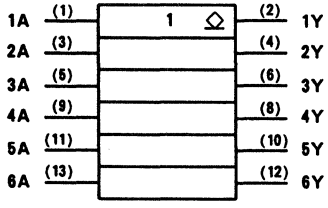


(TOP VIEW)

SYSTEM DIAGRAM(per gate)



IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	L
H	Z

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OL}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	−	−	±0.5	−	±5.0	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	–	5	15	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	–	5	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	–	10	90	–	115	
			4.5	–	7	18	–	23	
			6.0	–	6	15	–	20	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	–	17	90	–	115	
			4.5	–	7	18	–	23	
			6.0	–	5	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	3	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	4	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

QUAD 2-INPUT AND GATE

The TC74HC08A is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

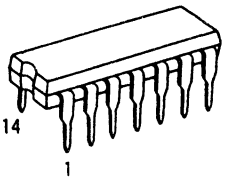
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

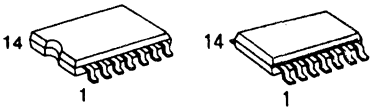
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS08

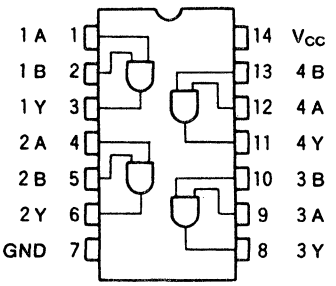


P(DIP14-P-300)



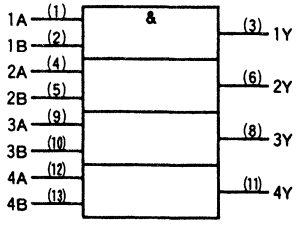
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	24	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	19	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HCT08AP/AF

QUAD 2-INPUT AND GATE

The TC74HCT08A is a high speed CMOS fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

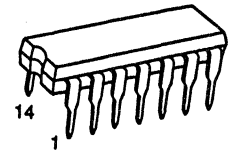
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

The internal circuit is composed of 2-stages including buffer output, which provide high noise immunity and stable otput.

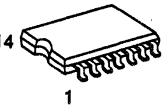
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs..... V_{IH} =2V(Min)
  V_{IL} =0.8V(Max.)
- Wide interfacing ability ..... LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS08

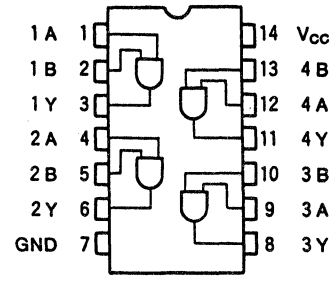


P(DIP14-P-300)



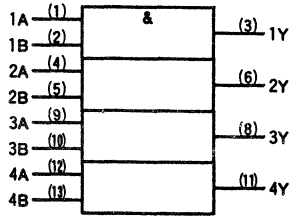
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	0.1	−	10.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	16	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 13	– –	19 16	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5 5.5	– –	13 11	20 18	– –	25 23	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	24	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOTES

QUAD 2-INPUT AND GATE (OPEN DRAIN)

The TC74HC09A is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

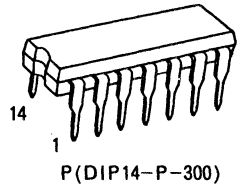
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and functon are the same as the TC74HC08A. But TC74HC09A has the high performance MOS N-channel transistor (OPEN-DRAIN) outputs. This device can, therefore, with suitable pull-up resistors, be used in wired-AND, LED driver and other applications.

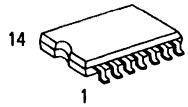
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pZ}=6ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS09

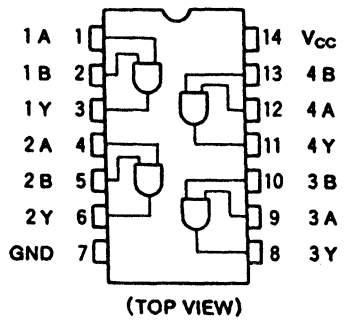


P(DIP14-P-300)



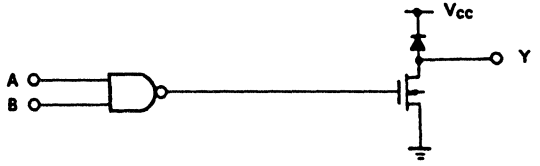
F(SOP14-P-300)

PIN ASSIGNMENT

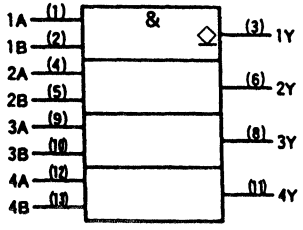


(TOP VIEW)

SYSTEM DIAGRAM(per gate)



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	L
H	L	L
H	H	Z

Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}		6.0	−	−	±0.5	−	±5.0	V
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	–	6	15	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	–	6	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	–	10	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	–	20	75	–	95	
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	3	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	5	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TRIPLE 3-INPUT NAND GATE

The TC74HC10A is a high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

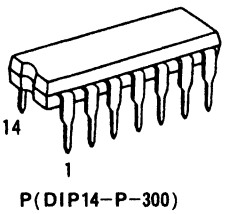
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

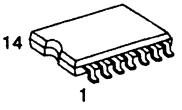
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

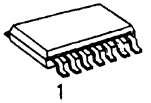
FEATURES:

- High Speed ..... t_{pd}=6ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH} =V_{NIL} =28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$ =I_{OL} =4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS10



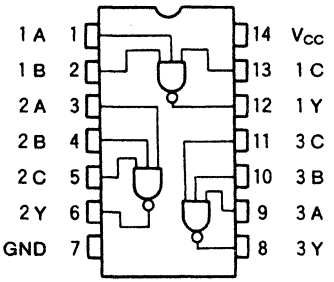
P(DIP14-P-300)





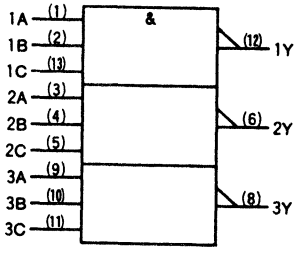
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	27	75	–	95	ns
			4.5	–	9	15	–	19	
			6.0	–	8	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	23	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC11AP/AF/AFN

TRIPLE 3-INPUT AND GATE

The TC74HC11A is a high speed CMOS 3-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

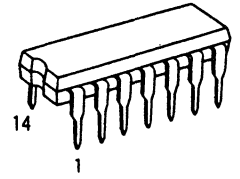
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including a buffer output, which provide high noise immunity and stable output.

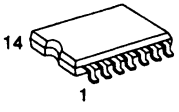
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

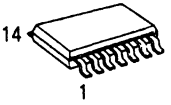
FEATURES:

- High Speed ····· t_{pd} =7ns(Typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC} =1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS11



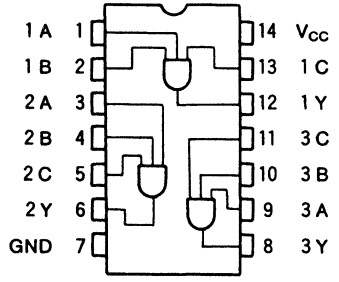
P(DIP14-P-300)





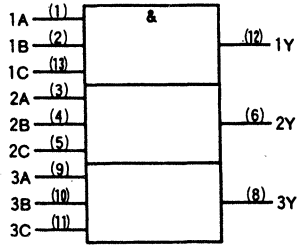
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
L	X	X	L
X	L	X	L
X	X	L	L
H	H	H	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	7	14	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	30	85	–	105	ns
			4.5	–	10	17	–	21	
			6.0	–	9	14	–	18	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	32	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{ (per Gate)}$$

HEX SCHMITT INVERTER

The TC74HC14A is a high speed CMOS SCHMITT INVERTER fabricated with silicon gate C^2MOS technology.

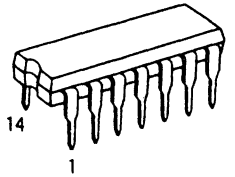
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HC04A but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger function, the TC74HC14A can be used as a line receiver which will receive slow input signals.

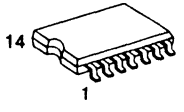
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

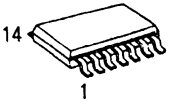
- High Speed ..... t_{pd}=11ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_H=1.1V at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS14



P(DIP14-P-300)

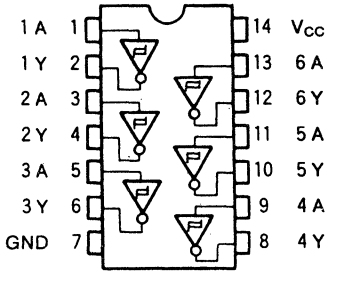


F(SOP14-P-300)



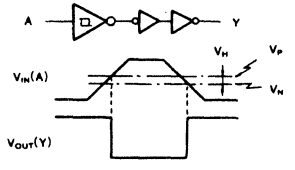
FN(SOL14-P-150)

PIN ASSIGNMENT

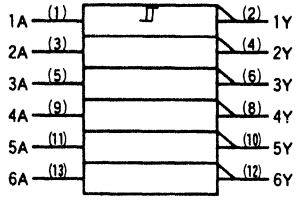


(TOP VIEW)

SYSTEM DIAGRAM,WAVEFORM



IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			2.0	1.0	1.25	1.5	1.0	1.5	V
				4.5	2.3	2.7	3.15	2.3	3.15	
				6.0	3.0	3.5	4.2	3.0	4.2	
Negative Threshold Voltage	V_N			2.0	0.3	0.65	0.9	0.3	0.9	V
				4.5	1.13	1.6	2.0	1.13	2.0	
				6.0	1.5	2.3	2.6	1.5	2.6	
Hysteresis Voltage	V_H			2.0	0.3	0.6	1.0	0.3	1.0	V
				4.5	0.6	1.1	1.4	0.6	1.4	
				6.0	0.8	1.2	1.7	0.8	1.7	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	21	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	125	–	155	
			4.5	–	14	25	–	31	
			6.0	–	12	21	–	26	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	28	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

DUAL 4-INPUT NAND GATE

The TC74HC20A is a high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

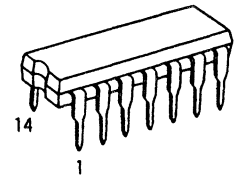
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

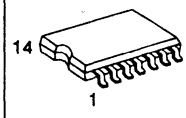
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

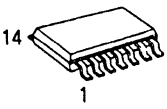
FEATURES:

- High Speed ····· t_{pd}=8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS20



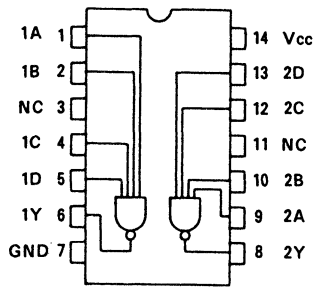
P(DIP14-P-300)





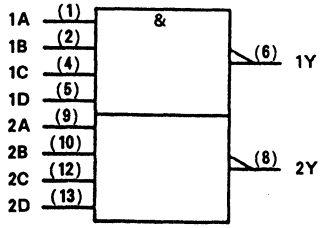
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	5	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	44	90	–	115	
			4.5	–	11	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	29	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

DUAL 4-INPUT AND GATE

The TC74HC21A is a high speed CMOS 4-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

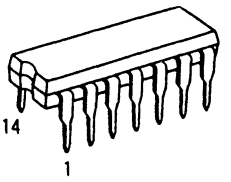
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages, including a buffer output, which provide high noise immunity and stable output.

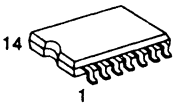
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

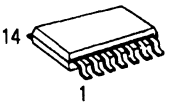
FEATURES:

- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS21



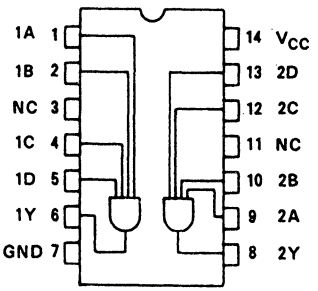
P(DIP14-P-300)





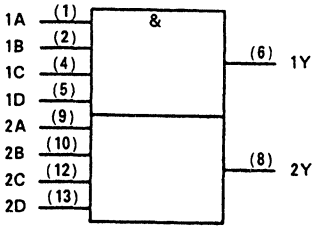
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs				Outputs
A	B	C	D	Y
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L
H	H	H	H	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

TC74HC27AP/AF/AFN

TRIPLE 3-INPUT NOR GATE

The TC74HC27A is a high speed CMOS 3-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

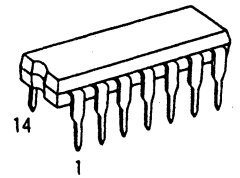
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which provide high noise immunity and stable output.

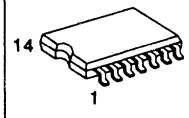
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

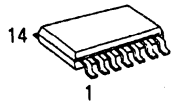
FEATURES:

- High Speed ..... t_{pd}=7ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS27



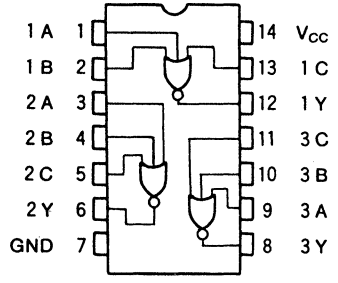
P(DIP14-P-300)





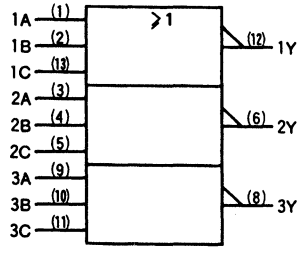
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	7	15	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	30	90	–	115	
			4.5	–	10	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{(per Gate)}$$

8-INPUT NAND GATE

The TC74HC30A is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

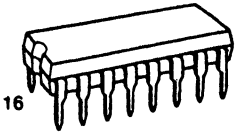
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 5 stages including buffered outputs, which provide high noise immunity and stable output.

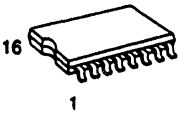
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

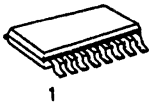
FEATURES:

- High Speed ····· t_{pd}=12ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS30



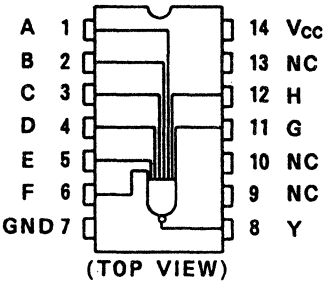
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

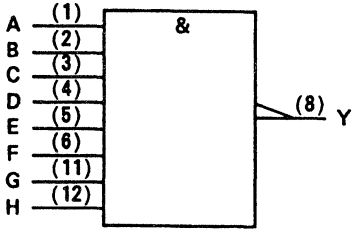
PIN ASSIGNMENT



(TOP VIEW)

NC:No Connection

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs	Outputs
All Inputs High	L
All Other Combinations	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	12	19	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	45	115	–	145	
			4.5	–	15	23	–	29	
			6.0	–	13	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	20	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC32AP/AF/AFN

QUAD 2-INPUT OR GATE

The TC74HC32A is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

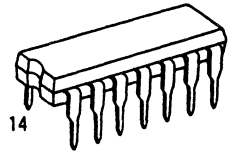
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

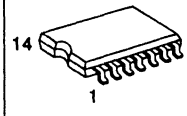
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

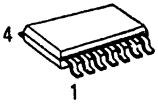
FEATURES:

- High Speed ..... t_{pd}=6ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS32



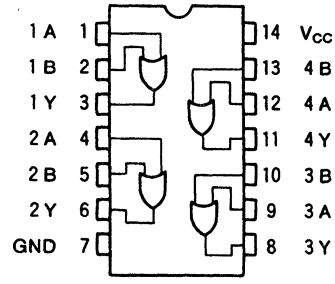
P(DIP14-P-300)





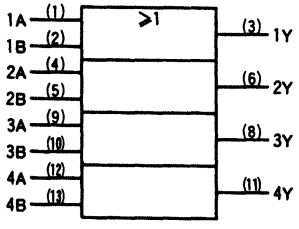
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	6	12	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	24	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	21	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

QUAD 2-INPUT OR GATE

The TC74HCT32A is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

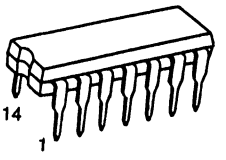
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

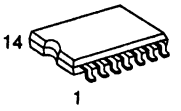
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=9ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs..... V_{IH} =2V(Min)
  V_{IL} =0.8V(Max.)
- Wide interfacing ability ..... LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS32

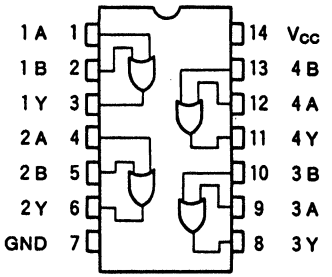


P(DIP14-P-300)



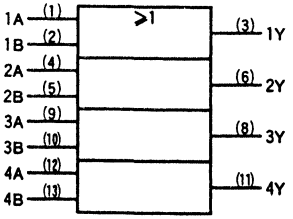
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	H
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	1.0	−	10.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	16	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		4.5	–	8	15	–	19	ns
	t_{THL}		5.5	–	7	13	–	16	
Propagation Delay Time	t_{pLH}		4.5	–	13	20	–	25	ns
	t_{pHL}		5.5	–	11	18	–	23	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	23	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

NOTES

BCD-TO-DECIMAL DECODER

The TC74HC42A is a high speed CMOS BCD-to-DECIMAL DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

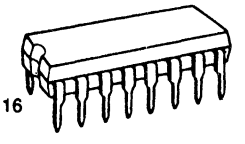
A BCD code applied to the four inputs (A-D) sets a low level at one of ten decoded outputs. A illegal BCD code such as eleven thru fifteen sets all outputs high. This device can be used as 3-to-8 LINE DECODER when input D is held low.

This device is useful for code conversion , address decoding , memory selection , multiplexing , or readout decoding.

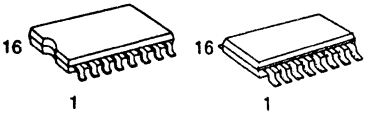
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS42

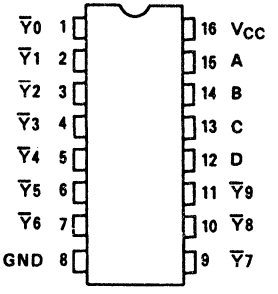


P(DIP16-P-300A)



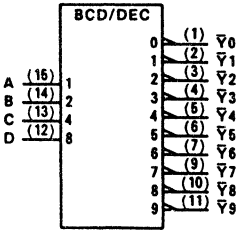
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

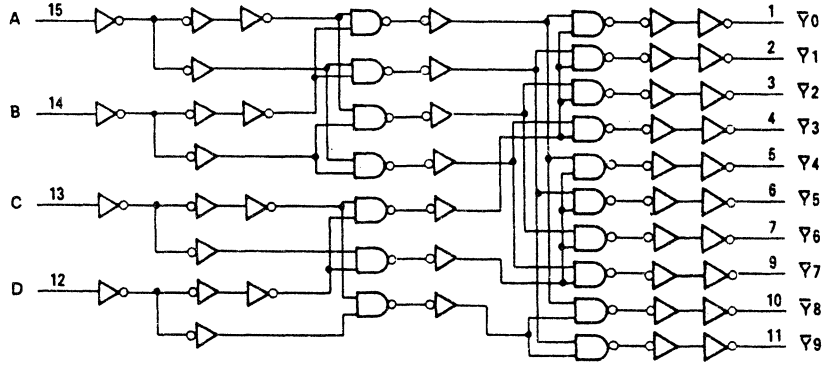


TRUTH TABLE

CODE	BCD INPUTS				DECIMAL OUTPUTS									
No.	D	C	B	A	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	$\overline{Y}8$	$\overline{Y}9$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
–	H	X	H	X	H	H	H	H	H	H	H	H	H	H
–	H	H	X	X	H	H	H	H	H	H	H	H	H	H

X; Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	13	25	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40～85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	48	145	–	180	
			4.5	–	16	29	–	36	
			6.0	–	14	25	–	31	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	68	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

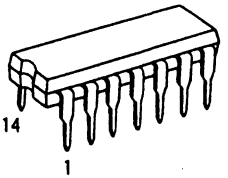
The TC74HC51A is a high speed CMOS 2-WIDE 2-INPUT/3-INPUT AND/OR/INVERT GATE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

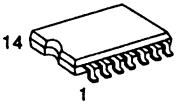
It contains a 2-WIDE 2-INPUT AND/OR/INVERT GATE and a 2-WIDE 3-INPUT AND/OR/INVERT GATE .

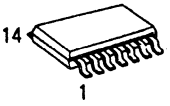
The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffer outputs, which provide high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP14-P-300)



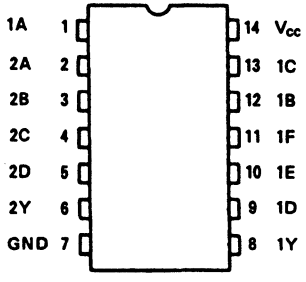


F(SOP14-P-300) FN(SOL14-P-150)

FEATURES:

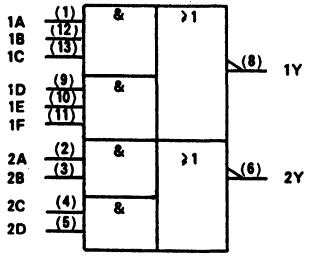
- High Speed ····· t_{pd}= 10 ns(Typ.)atV_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)atTa=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS51

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

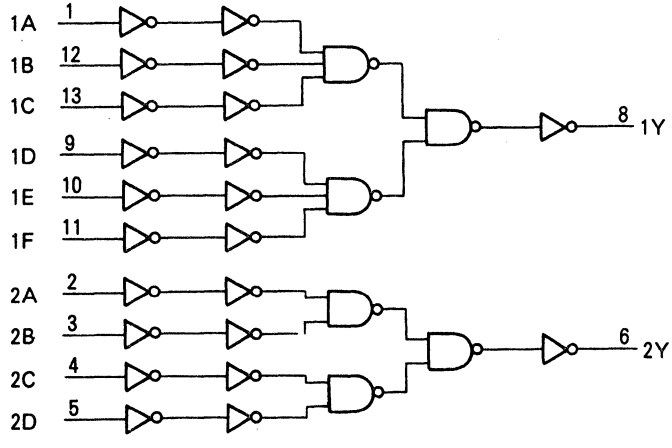
INPUTS						OUTPUT
1A	1B	1C	1D	1E	1F	1Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

X:Don't care

INPUTS				OUTPUT
2A	2B	2C	2D	2Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	39	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	35	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC73A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

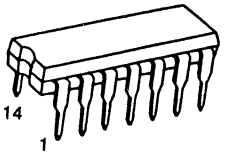
Depending on the logic levels applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.

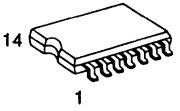
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=55MHz(Typ.) V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS73

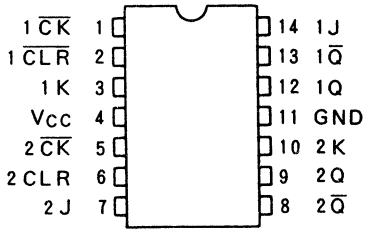


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT



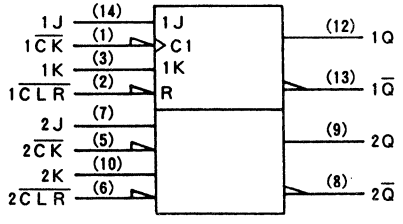
(Top View)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	–
H	H	L	↓	H	L	–
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X : Don't Care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	11	21	
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	15	25	
Maximum Clock Frequency	f_{MAX}		35	75	−	MHz

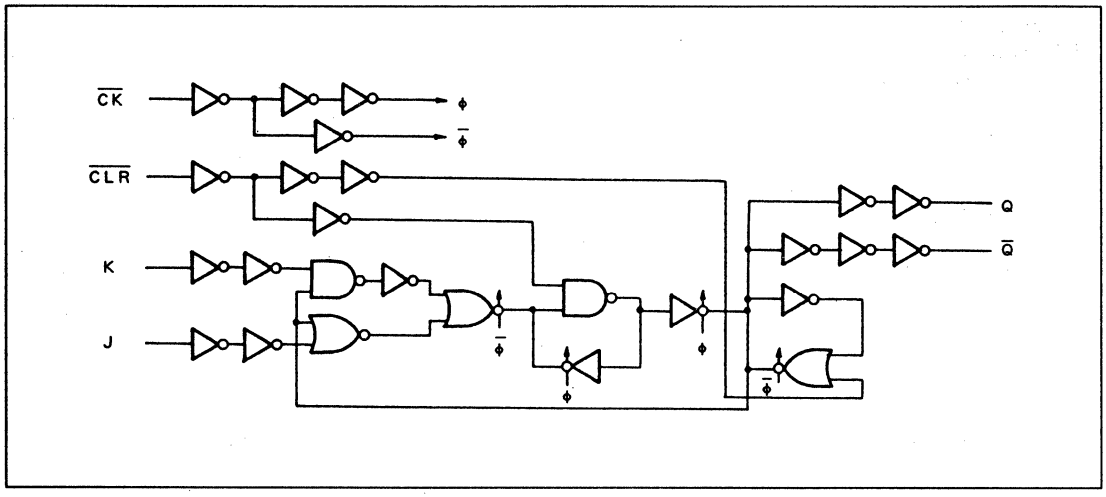
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	42	125	−	155	
			4.5	−	14	25	−	31	
			6.0	−	12	21	−	26	
Propagation Delay Time ($\overline{CLR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	54	145	−	180	
			4.5	−	18	29	−	36	
			6.0	−	15	25	−	31	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	−	5	−	MHz
			4.5	30	60	−	24	−	
			6.0	35	80	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	35	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM



TC74HC74AP/AF/AFN

DUAL D-TYPE FLIP FLOP PRESET AND CLEAR

The TC74HC74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

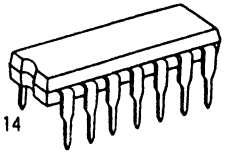
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

$\overline{\text{CLEAR}}$ and $\overline{\text{PRESET}}$ are independent of the CLOCK and are accomplished by setting the appropriate input low.

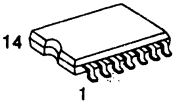
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

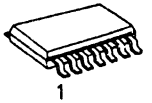
FEATURES:

- High Speed ····· f_{MAX}=77MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS74



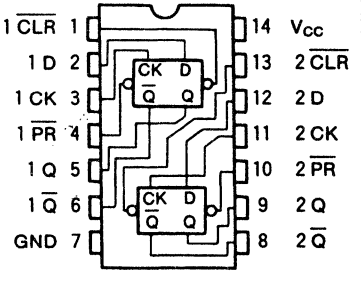
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



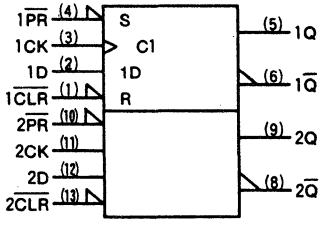
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	t_{WCL} t_{WCH}		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	t_{WCL}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	14	26	
Maximum Clock Frequency	f_{MAX}		36	77	−	MHz

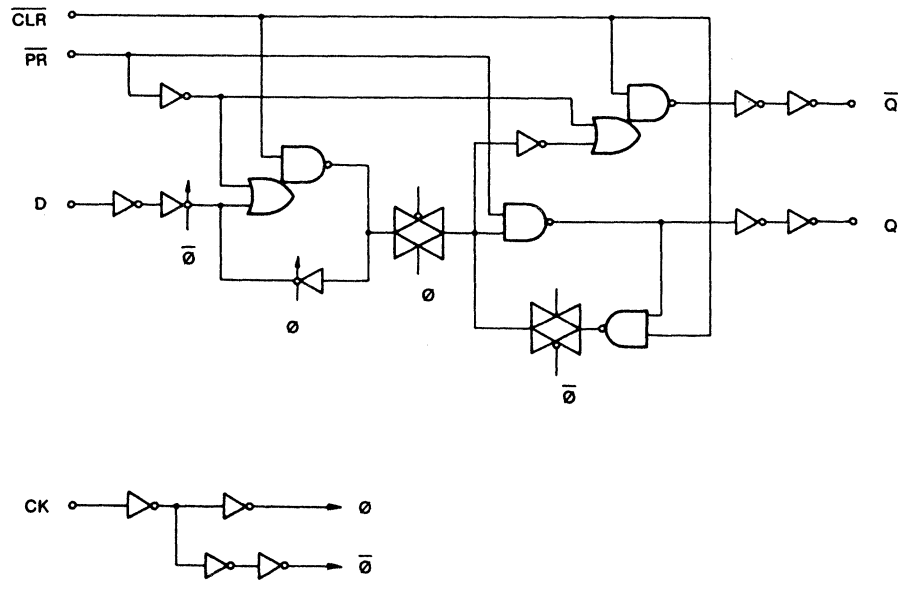
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	48	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	51	150	−	190	
			4.5	−	17	30	−	38	
			6.0	−	15	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	21	−	5	−	MHz
			4.5	31	63	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	34	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM (1/2package)



DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC74HCT74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

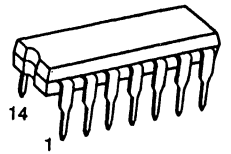
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

$\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the CLOCK and are accomplished by setting the appropriate input low.

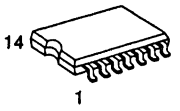
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=51MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Wide Interfacing ability ····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS74

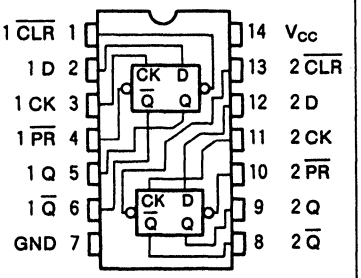


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT



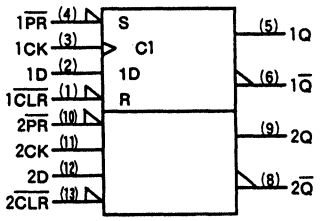
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↓	L	H	—
H	H	H	↓	H	L	—
H	H	X	↑	Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	2.0	−	20.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		4.5	−	15	19	ns
	$t_{W(H)}$		5.5	−	14	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{W(L)}$		4.5	−	15	19	
			5.5	−	14	17	
Minimum Set−up Time	t_s		4.5	−	15	19	
			5.5	−	14	17	
Minimum Hold Time	t_h		4.5	−	0	0	
			5.5	−	0	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		4.5	−	5	6	
			5.5	−	5	5	
Clock Frequency	f		4.5	−	27	22	MHz
			5.5	−	30	24	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	17	28	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	15	25	
Maximum Clock Frequency	f_{MAX}		53	29	−	MHz

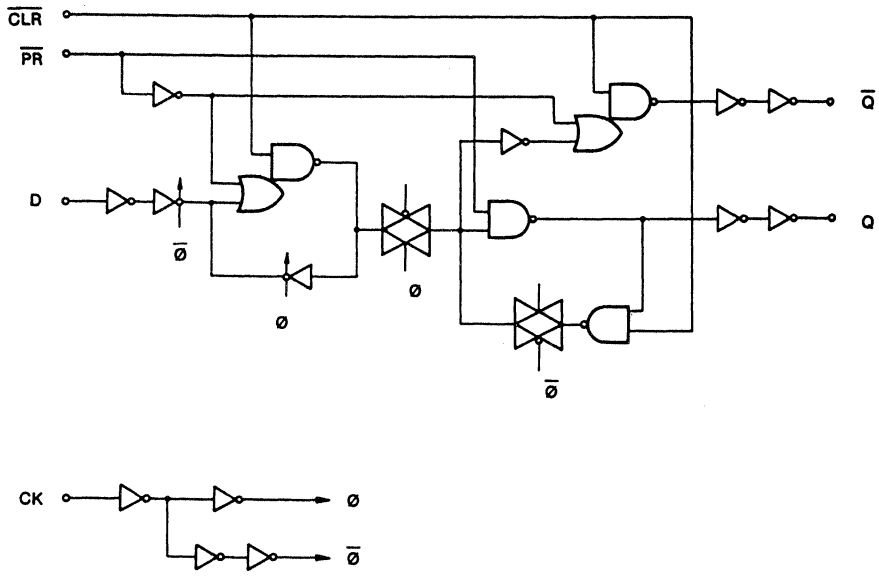
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	−	8	15	−	19	ns
			5.5	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		4.5	−	21	33	−	41	
			5.5	−	19	30	−	37	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		4.5	−	18	30	−	38	
			5.5	−	15	27	−	35	
Maximum Clock Frequency	f_{MAX}		4.5	27	48	−	22	−	MHz
			5.5	30	53	−	24	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	32	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM (1/2package)



4-BIT D TYPE LATCH

The TC74HC75A is a high speed CMOS D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

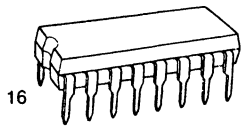
It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4) and each group can be used in different circuits.

Data applied to the data inputs are transferred to the Q and $\overline{Q}$ outputs when the enable input is high. When the enable input is low, the outputs are not affected.

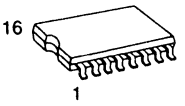
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd} =10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =2μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$ =28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS75

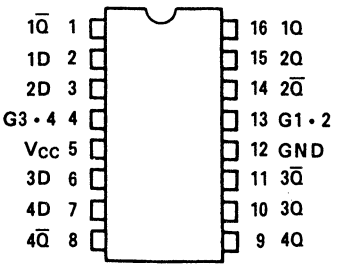


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



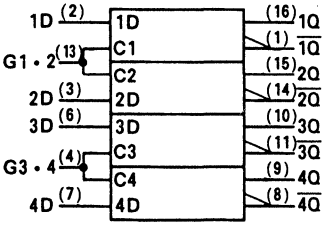
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\overline{Q}$n	LATCH

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	–	–	1.5	–	V
				4.5	3.15	–	–	3.15	–	
				6.0	4.2	–	–	4.2	–	
Low-Level Input Voltage	V_{IL}			2.0	–	–	0.5	–	0.5	V
				4.5	–	–	1.35	–	1.35	
				6.0	–	–	1.8	–	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	–	1.9	–	V
				4.5	4.4	4.5	–	4.4	–	
				6.0	5.9	6.0	–	5.9	–	
			I_{OH} =−4 mA	4.5	4.18	4.31	–	4.13	–	
			I_{OH} =−5.2mA	6.0	5.68	5.80	–	5.63	–	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	–	0.0	0.1	–	0.1	V
				4.5	–	0.0	0.1	–	0.1	
				6.0	–	0.0	0.1	–	0.1	
			I_{OL} =4 mA	4.5	–	0.17	0.26	–	0.33	
			I_{OL} =5.2mA	6.0	–	0.18	0.26	–	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	2.0	–	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (G)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	10	18	
Propagation Delay Time (G−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	10	21	

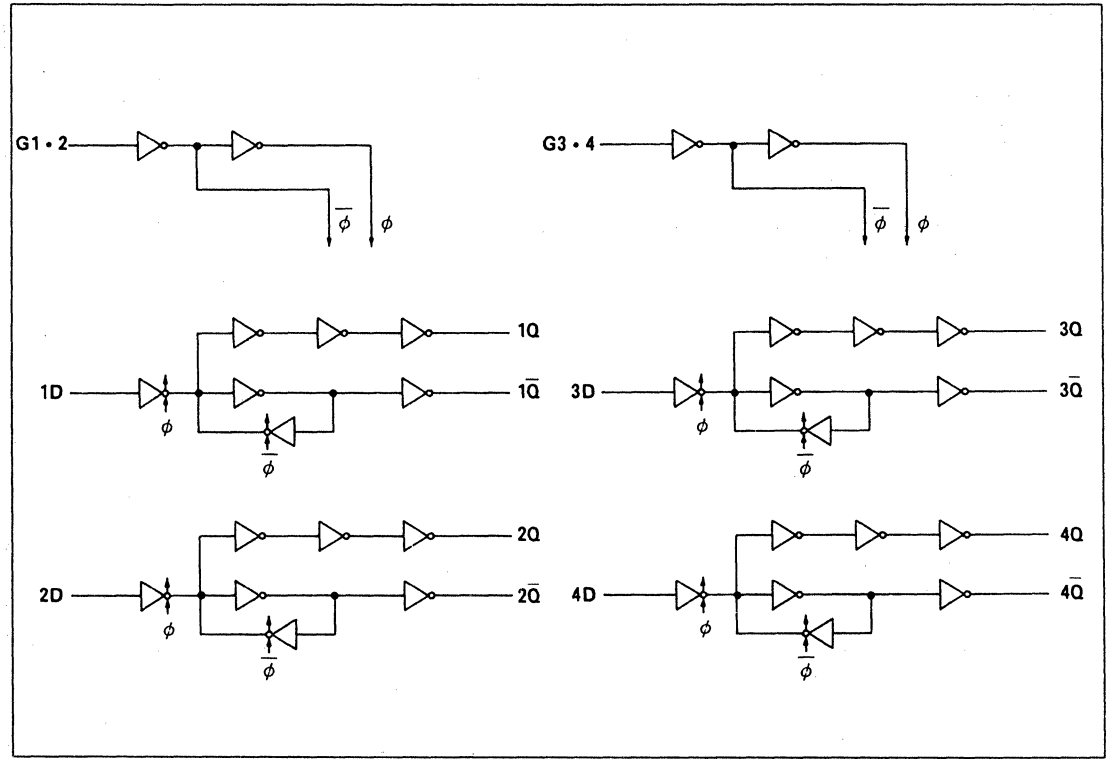
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	36	110	−	140	
			4.5	−	12	22	−	28	
			6.0	−	10	19	−	24	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	40	125	−	155	
			4.5	−	13	25	−	31	
			6.0	−	11	21	−	26	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	30	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4 \text{(per Latch)}$$

SYSTEM DIAGRAM



DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

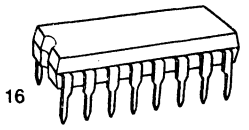
The TC74HC76A is a high speed CMOS J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

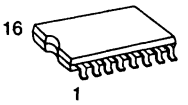
In accordance with the logic level applied to the J and K inputs,the outputs change state on the negative going transition of the clock pulse.

$\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and are accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP16-P-300A)

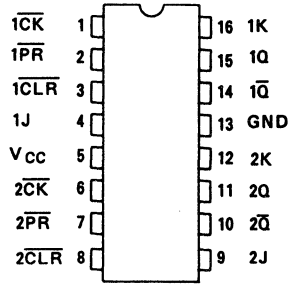


F(SOP16-P-300)

FEATURES:

- High Speed ····· f_{MAX}=65MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{PLH} \fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS76 .

PIN ASSIGNMENT



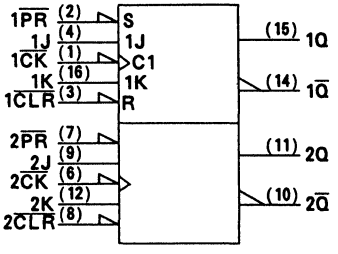
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$,$\overline{PR}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	12	21	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	14	24	
Maximum Clock Frequency	f_{MAX}		33	65	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

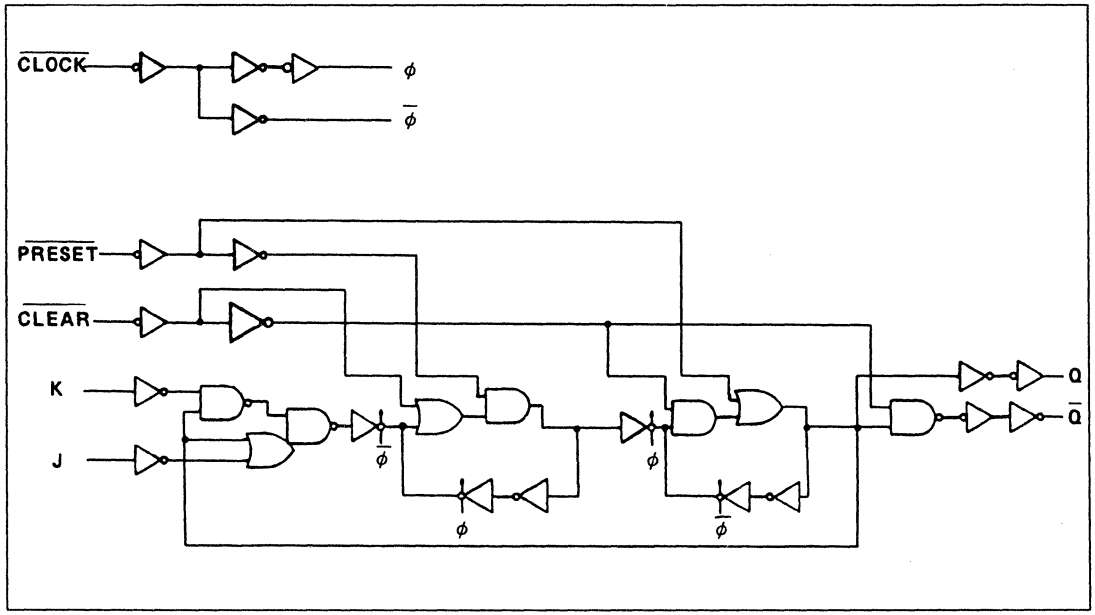
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	60	125	−	155	
			4.5	−	15	25	−	31	
			6.0	−	13	21	−	26	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	76	140	−	195	
			4.5	−	18	28	−	39	
			6.0	−	16	24	−	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	21	−	5	−	MHz
			4.5	31	63	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM (1/2 package)



4-BIT D TYPE LATCH

The TC74HC77A is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissiparion.

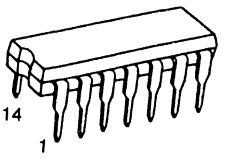
It contains two groups of 2-bit latches controlled by an enable input (G1, 2 or G3, 4) and these two groups may be used in different circuits.

The data applied to the data inputs are transferred to the respective Q outputs when the enable input is held high. When the enable input is low, the outputs remain at the level at the time the enable goes low.

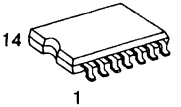
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS77

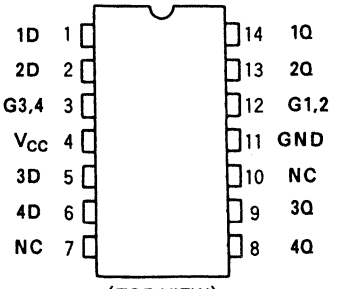


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT



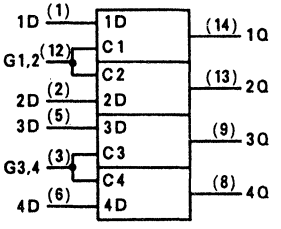
(TOP VIEW)
NC:NO CONNECTION

IEC LOGIC SYMBOL

INPUTS		OUTPUTS	FUNCTION
D	G	Q	
L	H	L	—
H	H	H	—
X	L	Q_n	LATCH

X : Don't care

TRUTH TABLE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (G)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		−	10	17	
Propagation Delay Time (G−Q)	t_{pLH} t_{pHL}		−	10	17	

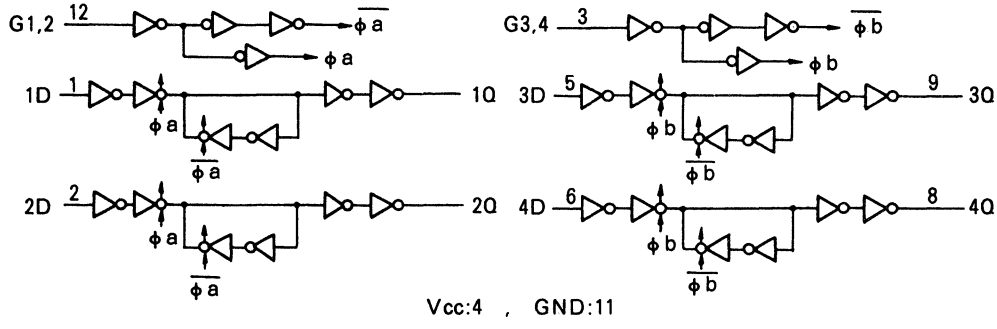
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Propagation Delay Time (G−Q)	t_{pLH} t_{pHL}		2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	20	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4 \text{(per Gate)}$$

SYSTEM DIAGRAM



4-BIT MAGNITUDE COMPARATOR

The TC74HC85A is a high speed CMOS 4 BIT MAGNITUDE COMPARATOR fabricated with silicon gate C^2MOS technology.

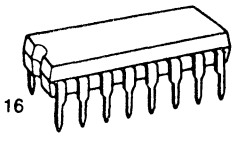
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC85A compares two 4-bit words applied to inputs A0~A3 and B0~B3,and provides a high voltage level on one of three outputs:A>B, A<B, or A=B.

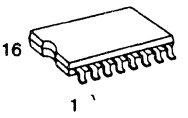
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

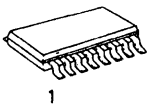
FEATURES:

- High Speed ····· t_{pd}=22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS85



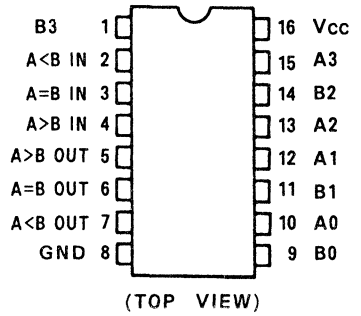
P(DIP16-P-300A)





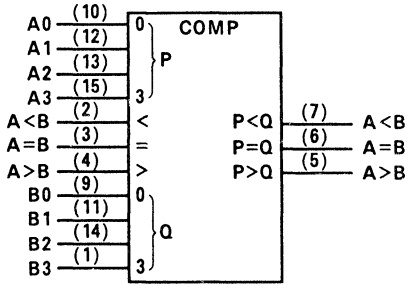
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

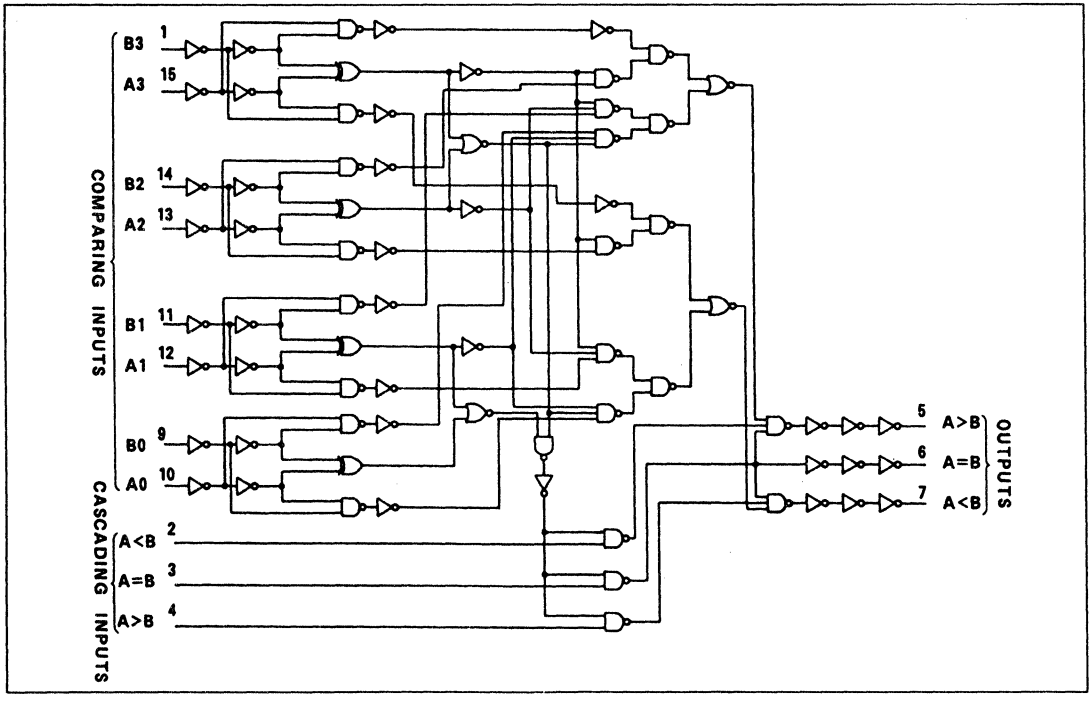


TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3 ,	A2=B2 ,	A1=B1 ,	A0=B0	L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X:Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B–OUT)	t_{pLH} t_{pHL}		–	22	34	
Propagation Delay Time (CASCADE–OUT)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

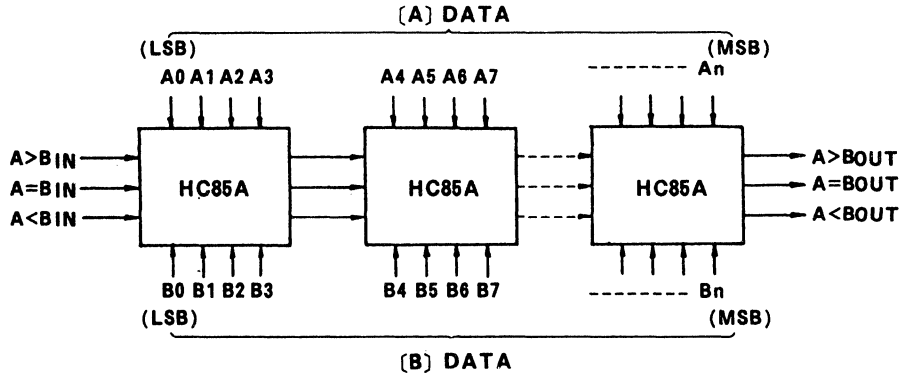
PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B–OUT)	t_{pLH} t_{pHL}		2.0	–	90	195	–	245	
			4.5	–	26	39	–	49	
			6.0	–	22	33	–	42	
Propagation Delay Time (CASCADE–OUT)	t_{pLH} t_{pLH}		2.0	–	40	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	11	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	25	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION

N-BIT CASCADING CONNECTION



COMPARING INPUT	CASCADING INPUT			OUTPUT		
	A>B	A=B	A<B	A>B	A=B	A<B
(A) > (B)	X	X	X	H	L	L
(A) = (B)	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
(A) < (B)	X	X	X	L	L	H

X:Don't Care

NOTES

QUAD EXCLUSIVE OR GATE

The TC74HC86A is a high speed CMOS EXCLUSIVE OR GATE fabricated with silicon gate C^2MOS technology.

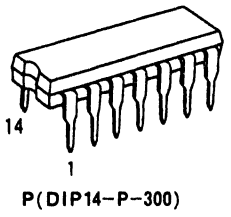
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Input and output buffers are provided which offer high noise immunity and stable output.

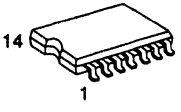
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

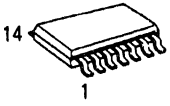
- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS86



P(DIP14-P-300)

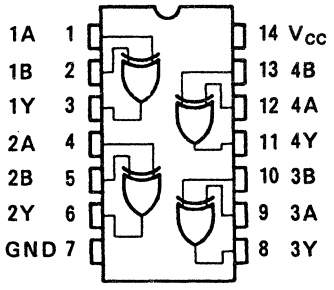


F(SOP14-P-300)



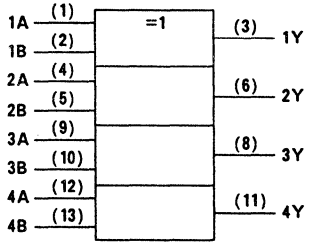
FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
H	H	L
L	H	H
H	L	H
L	L	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	45	100	–	125	ns
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	26	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC107A is a high speed CMOS DUAL J-K FLIP-FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

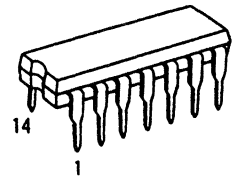
In accordance with the logic levels applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

$\overline{CLEAR}$ is independent of the clock and is accomplished by a low logic level on the input.

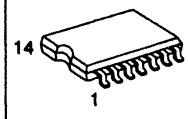
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

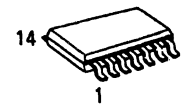
FEATURES:

- High Speed ····· f_{MAX}=75MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS107



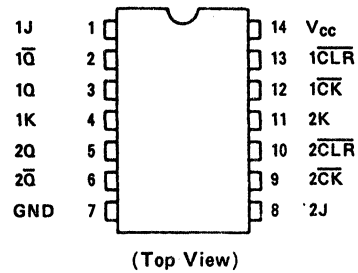
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



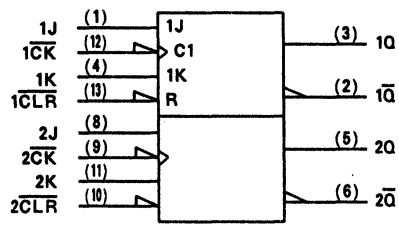
(Top View)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	–
H	H	L	↓	H	L	–
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X : Don't Care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLR)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time (CLR)	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	37	30	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	11	21	
Propagation Delay Time ($\overline{CLR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	12	24	
Maximum Clock Frequency	f_{MAX}		34	75	−	MHz

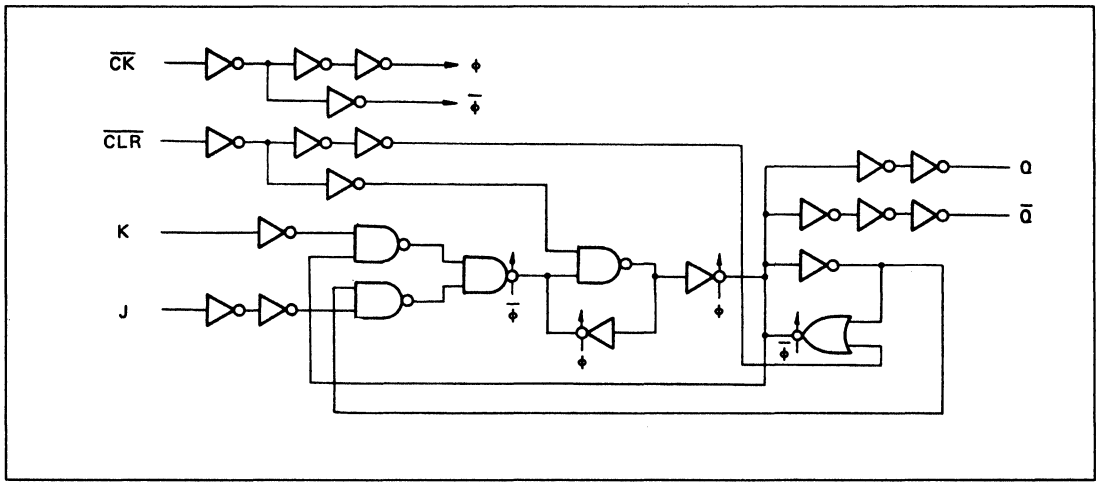
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	48	125	−	155	
			4.5	−	14	25	−	31	
			6.0	−	12	21	−	26	
Propagation Delay Time ($\overline{CLR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	52	140	−	175	
			4.5	−	15	28	−	35	
			6.0	−	13	24	−	30	
Maximum Clock Frequency	f_{MAX}		2.0	6	23	−	5	−	MHz
			4.5	31	70	−	25	−	
			6.0	37	80	−	30	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	33	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM



TC74HC109AP/AF/AFN

DUAL J-$\overline{K}$ FLIP-FLOP WITH PRESET AND CLEAR

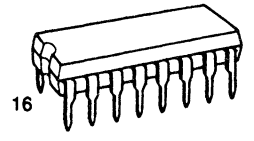
The TC74HC109A is a high speed CMOS J-$\overline{K}$ FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

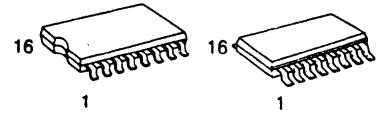
In accordance with the logic level applied to the J and $\overline{K}$ inputs,the outputs change state on the positive going transition of the clock pulse.

$\overline{CLEAR}$ and $\overline{PRESET}$ are independent of the clock and are accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP16-P-300A)

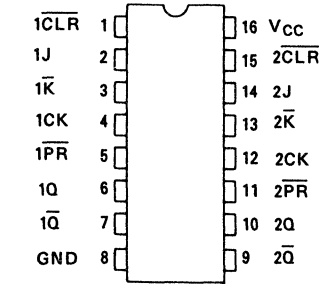


F(SOP16-P-300) FN(SOL16-P-150)

FEATURES:

- High Speed ····· f_{MAX}=63MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS109.

PIN ASSIGNMENT



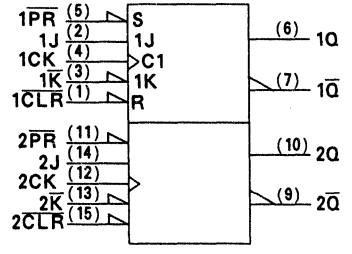
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	L	↓	L	L	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{PR}$,$\overline{CLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{PR}$,$\overline{CLR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Propagation Delay Time ($\overline{PR}$,$\overline{CLR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	26	
Maximum Clock Frequency	f_{MAX}		33	63	−	MHz

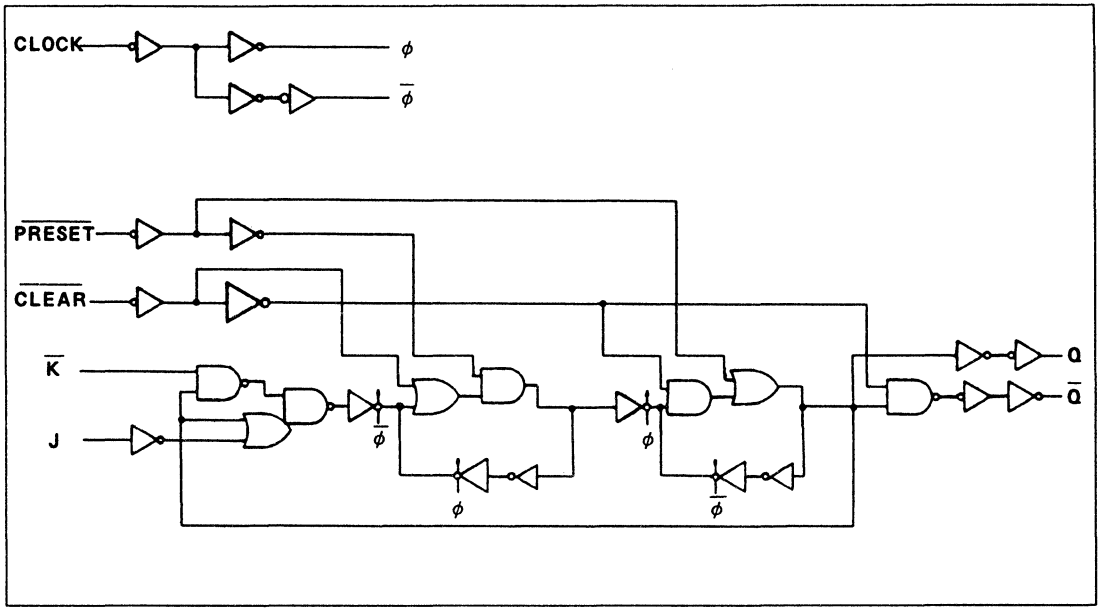
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Propagation Delay Time ($\overline{PR}$,$\overline{CLR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	150	−	190	
			4.5	−	16	30	−	38	
			6.0	−	13	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	17	−	5	−	MHz
			4.5	31	59	−	25	−	
			6.0	36	67	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	41	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SYSTEM DIAGRAM (1/2 package)



TC74HC112AP/AF/AFN

DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR

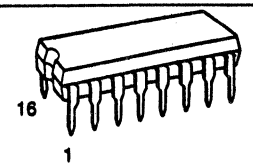
The TC74HC112A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

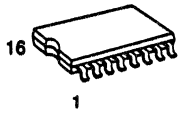
In accordance with the logic level applied to the J and K inputs,the outputs change state on the negative going transition of the clock pulse.

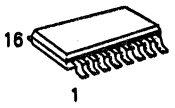
CLEAR and PRESET are independent of the clock and are actived by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



P(DIP16-P-300A)



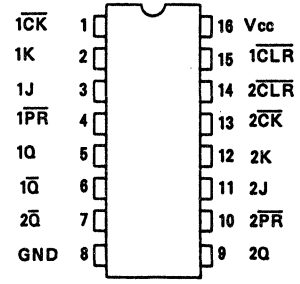


F(SOP16-P-300) FL(SOL16-P-150)

FEATURES:

- High Speed ····· f_{MAX}=63MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS112.

PIN ASSIGNMENT



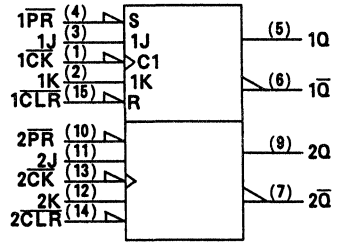
(TOP VIEW)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X:Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$,$\overline{PR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$,$\overline{PR}$)	t_{rem}		2.0	−	50	60	
			4.5	−	10	12	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	8	6	MHz
			4.5	−	40	32	
			6.0	−	47	38	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	21	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	14	22	
Maximum Clock Frequency	f_{MAX}		40	63	−	MHz

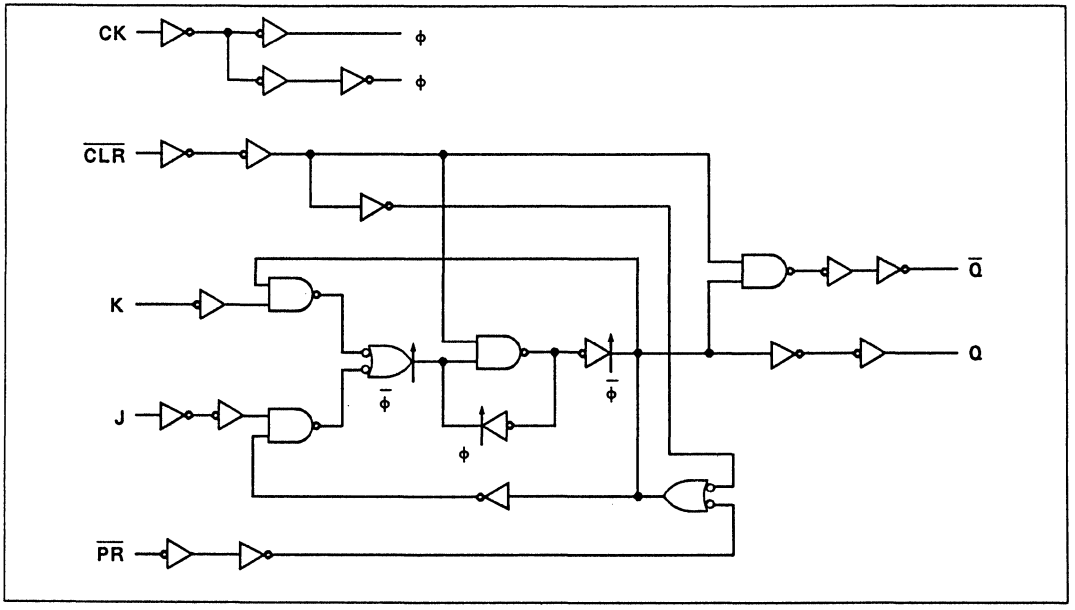
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	64	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	14	21	−	26	
Propagation Delay Time ($\overline{CLR}$,$\overline{PR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	68	135	−	170	
			4.5	−	17	27	−	34	
			6.0	−	14	23	−	29	
Maximum Clock Frequency	f_{MAX}		2.0	8	16	−	6	−	MHz
			4.5	40	63	−	32	−	
			6.0	47	79	−	38	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	33	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

SISTEM DIAGRAM (1/2 package)



NOTES

TC74HC113AP/AF

DUAL J-K FLIP FLOP WITH PRESET

The TC74HC113A is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

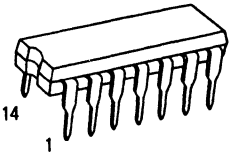
In accordance with the logic level applied to the J and K inputs, the outputs change state on the negative going transition of the clock pulse.

$\overline{PRESET}$ is independent of the clock and is accomplished by a low logic level on the input.

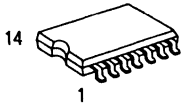
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MHz}=71MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS113

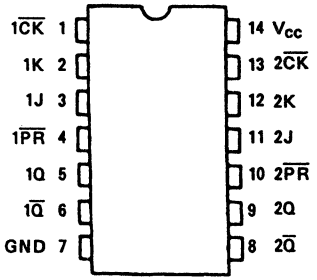


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT



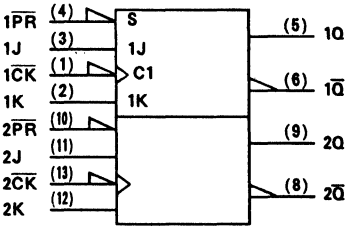
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	PRESET
H	L	L	↓	Qn	$\overline{Q}$n	NO CHANGE
H	L	H	↓	L	H	–
H	H	L	↓	H	L	–
H	H	H	↓	$\overline{Q}$n	Qn	TOGGLE
H	X	X	↑	Qn	$\overline{Q}$n	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{PR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	8	6	MHz
			4.5	−	40	32	
			6.0	−	47	38	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time (CLOCK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	21	
Propagation Delay Time ($\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	21	
Maximum Clock Frequency	f_{MAX}		43	71	−	MHz

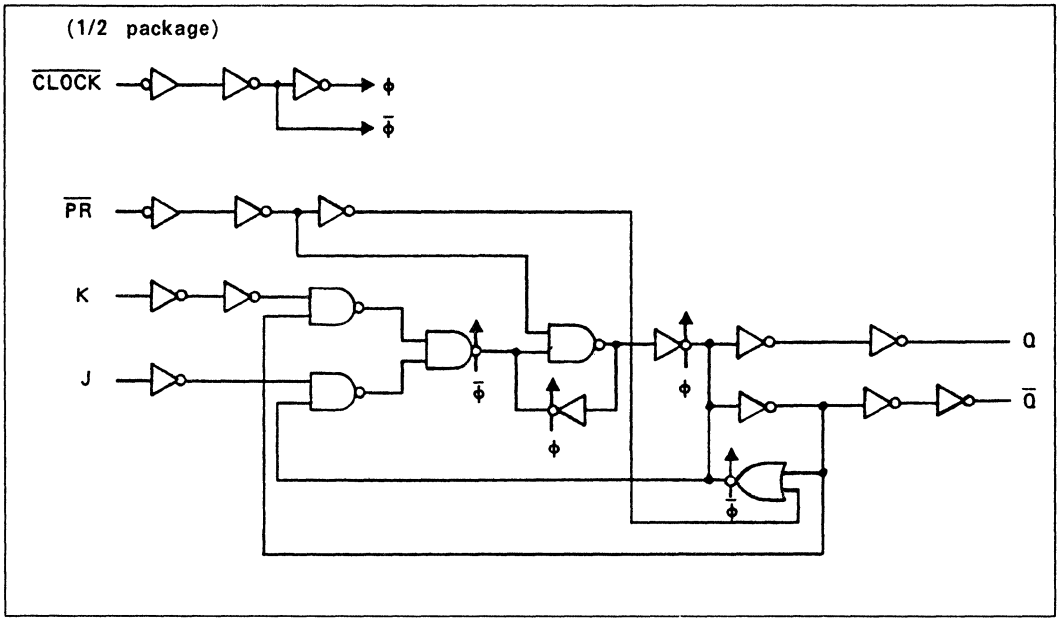
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	46	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	12	21	−	26	
Propagation Delay Time ($\overline{PR}$−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	48	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	13	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	8	16	−	6	−	MHz
			4.5	40	63	−	32	−	
			6.0	47	79	−	38	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	32	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/2 \text{(per F/F)}$$

SYSTEM DIAGRAM



TC74HC123AP/AF/AFN

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC123A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation simlar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (tr=tf=1sec.) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the $\overline{CLR}$ input breaks this state. In the MONOSTABLE state, if a new trigger is applied, it extends the MONOSTABLE period (retrigger mode).

Limits for Cx and Rx are :

External capacitor, Cx·····No limit

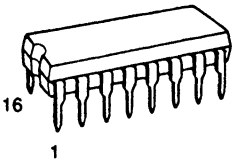
External resistor, Rx·····Vcc<3.0V more than 5kΩ

Vcc≥3.0V more than 1kΩ

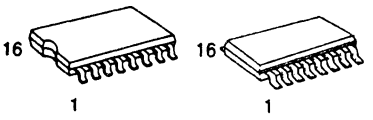
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=25ns(Typ.)at V_{CC}=5V
- Low Power Dissipation
  - Standby State ····· I_{CC}=4μA(Max.)at Ta=25℃
  - Active State ····· I_{CC}=700μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS123

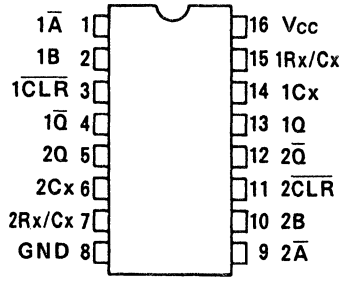


P(DIP16-P-300A)



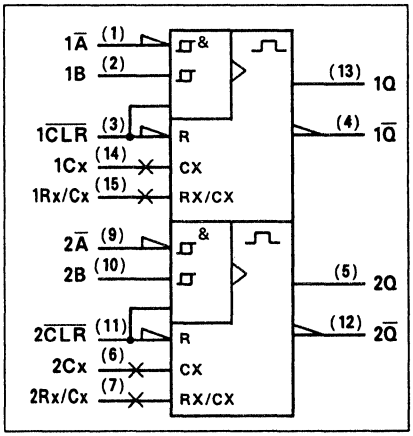
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

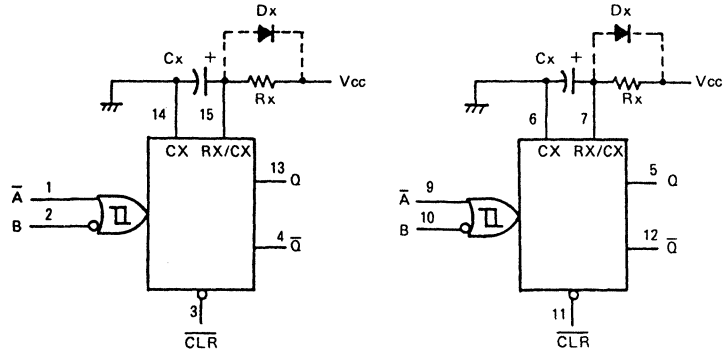


TRUTH TABLE

INPUT			OUTPUT		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎍	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⎍	⎍	OUTPUT ENABLE
L	H	↑	⎍	⎍	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:Don't Care

BLOCK DIAGRAM



Notes: (1) Cx, Rx, Dx are external.
Capacitor, Resistor, and Diode, respectively.

(2) External clamping diode, Dx;

The external capacitor is charged to Vcc level in the wait state, i.e. when no trigger is applied. If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and Vcc drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and Vcc drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20mA.

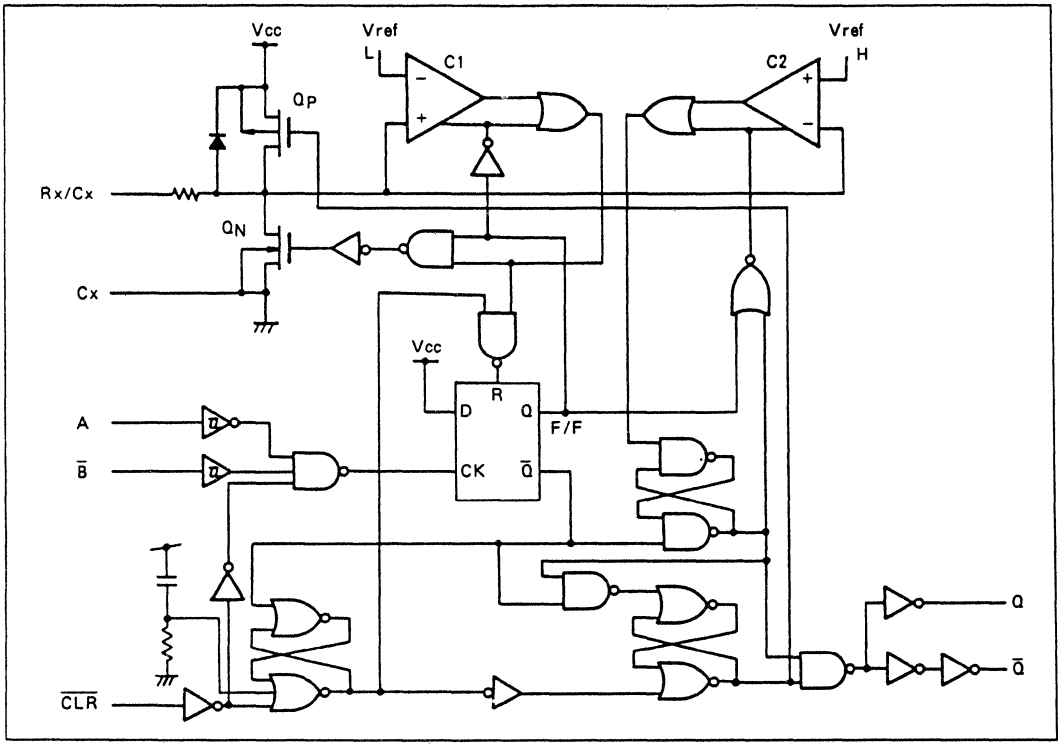
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (Vcc - 0.7)\ Cx/20mA$$

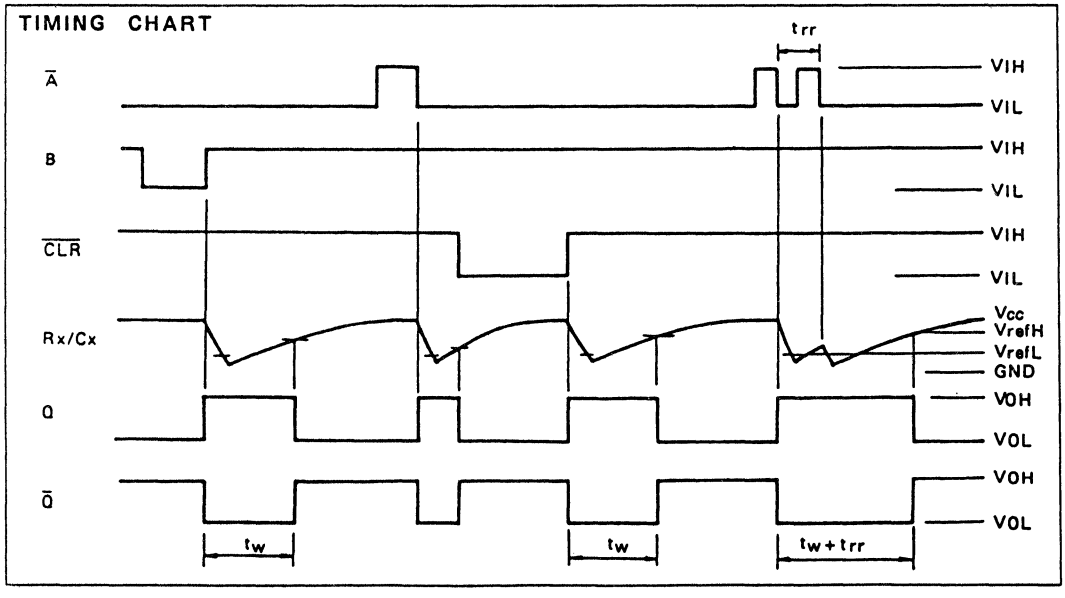
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 Vcc.)

In the event a system does not satisfy the above condition, an external clamping diode (Dx) is needed to protect the IC from in rush current.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by State

The external capacitor (Cx) is fully charged to Vcc in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

After Q_N turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx node reaches Vref H, the IC returns to its MONOSTABLE state.

With large values of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, tw (OUT), is as follows:

$$tw\ (OUT) = 1.0\ Cx\ Rx$$

(3) Retrigger operation

When a new trigger is applied to either input $\overline{A}$ or B while in the MONOSTABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx/Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, trr(Min.), depends on Vcc and Cx.

(4) Reset operation

In normal operation, the $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, Q_P turns on and Cx is charged rapidly to Vcc.

This means if $\overline{CLR}$ is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation *	F
External Resistor	Rx	≥5K (V_{CC}<3.0V) * ≥1K (V_{CC}≥3.0V) *	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC123A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for Rx>1MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage (Q,$\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage (Q,$\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Rx/Cx Terminal Off−State Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active−State * Supply Current	I_{CC}	V_{IN} =V_{CC} or GND Rx/Cx=0.5V_{CC}		2.0	−	45	200	−	260	μA
				4.5	−	400	500	−	650	μA
				6.0	−	0.7	1.0	−	1.3	mA

*: per circuit

TIMING REQUIREMENTS(Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Pulse Width	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Retrigger Time	t_{rr}	Rx=1KΩ Cx=100pF	2.0	325	−	−	
			4.5	108	−	−	
			6.0	78	−	−	
		Rx=1KΩ Cx=0.01μF	2.0	5.0	−	−	μs
			4.5	1.4	−	−	
			6.0	1.2	−	−	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{A}$, B–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		–	25	36	
Propagation Delay Time ($\overline{CLR}$ TRIGGER–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		–	26	41	
Propagation Delay Time ($\overline{CLR}$–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		–	16	27	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{A}$,B–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	102	210	–	265	
			4.5	–	29	42	–	53	
			6.0	–	22	36	–	45	
Propagation Delay Time ($\overline{CLR}$ TRIGGER–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	102	235	–	295	
			4.5	–	31	47	–	59	
			6.0	–	23	40	–	50	
Propagation Delay Time ($\overline{CLR}$–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	68	160	–	200	
			4.5	–	20	32	–	40	
			6.0	–	16	27	–	34	
Output Pulse Width	tw_{OUT}	Cx=28PF Rx=6KΩ(V_{CC}=2V)	2.0	–	700	2000	–	2500	ns
			4.5	–	250	400	–	500	
		Rx=2KΩ(V_{CC}=4.5V,6V)	6.0	–	210	340	–	425	
		Cx=0.01μF Rx=10KΩ	2.0	90	110	130	90	130	μs
			4.5	95	105	115	95	115	
			6.0	95	105	115	95	115	
		Cx=0.1μF Rx=10KΩ	2.0	0.9	1.0	1.2	0.9	1.2	ms
			4.5	0.9	1.0	1.1	0.9	1.1	
			6.0	0.9	1.0	1.1	0.9	1.1	
Output Pulse Width Error Between Circuits (In same Package)	Δtw_{OUT}			–	±1	–	–	–	%
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	162	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

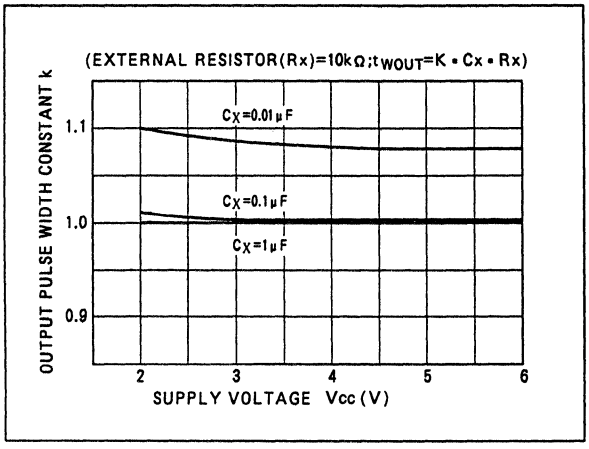
Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per circuit)

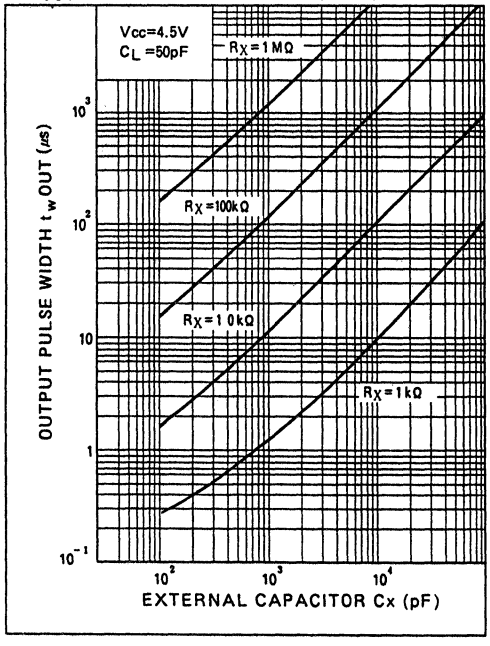
(I_{CC}': Active Supply Current)

(Duty: %)

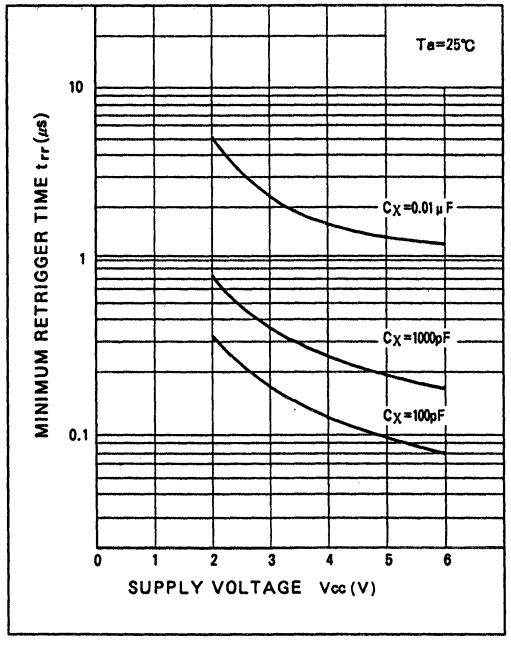
OUTPUT PULSE WIDTH CONSTANT K–SUPPLY VOLTAGE (TYPICAL)



tWOUT –Cx CHARACTERISTICS (TYP.)



trr –Vcc CHARACTERISTICS (TYP.)



TC74HC125AP/AF/AFN
TC74HC126AP/AF

TC74HC125AP/AF/AFN QUAD BUS BUFFER
TC74HC126AP/AF QUAD BUS BUFFER

The TC74HC125A/126A are high speed CMOS QUAD BUS BUFFERs fabricated with silicon gate C^2MOS technology.

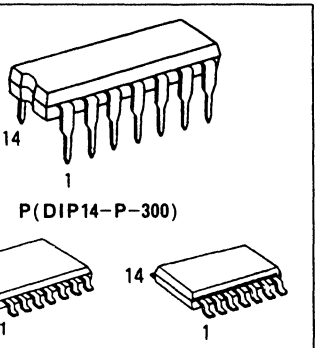
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC125A requires the 3-state control input $\overline{G}$ to be set high to place the output into the high impedance state, whereas the TC74HC126A requires the control input to be set low to place the output into high impedance.

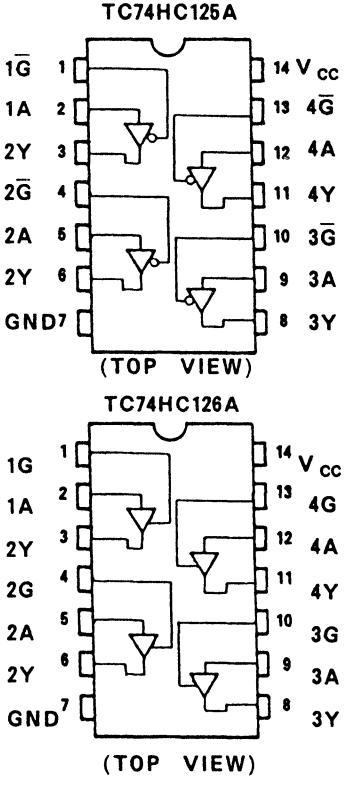
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

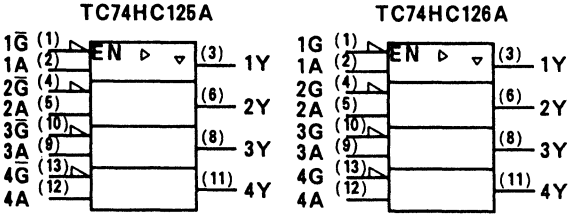
- High Speed ····· t_{pd} =10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS125/126



PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

TC74HC125A

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't Care
Z: High Impedance

TC74HC126A

INPUTS		OUTPUTS
G	A	Y
L	X	Z
H	L	L
H	H	H

X: Don't Care
Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	−	30	90	−	115	
				4.5	−	11	18	−	23	
				6.0	−	10	15	−	20	
			150	2.0	−	42	130	−	165	
				4.5	−	14	26	−	33	
				6.0	−	12	22	−	28	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1\,k\Omega$	50	2.0	−	30	90	−	115	
				4.5	−	11	18	−	23	
				6.0	−	10	15	−	20	
			150	2.0	−	42	130	−	165	
				4.5	−	14	26	−	33	
				6.0	−	12	22	−	28	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	24	100	−	125	
				4.5	−	12	20	−	25	
				6.0	−	10	17	−	21	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	41	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Gate)}$$

TC74HC131AP/AF

3-TO-8 LINE DECODER/LATCH

The TC74HC131A is a high speed CMOS 3-to-8 LINE DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

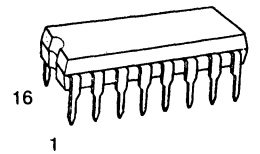
It is composed of 3-bit input register with a common CLOCK input and 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into input register on the positive going transition of the clock pulse. The value of the binary data determines which one of outputs will go to low.

When enable input G1 held low or $\overline{G2}$ is held high, the decoding function is inhibited and all outputs go high. These enable inputs are provided for cascade connection and for use as an address decoder for memory systems.

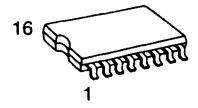
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V

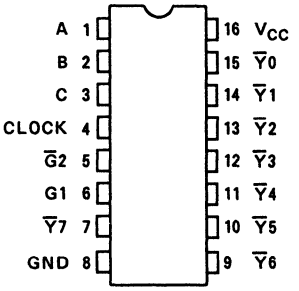


P(DIP16-P-300A)



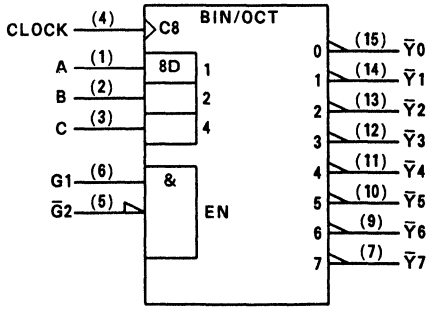
F(SOP16-P-300)

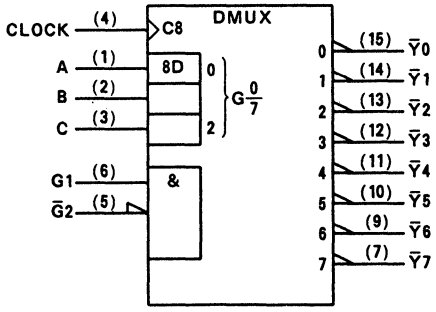
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



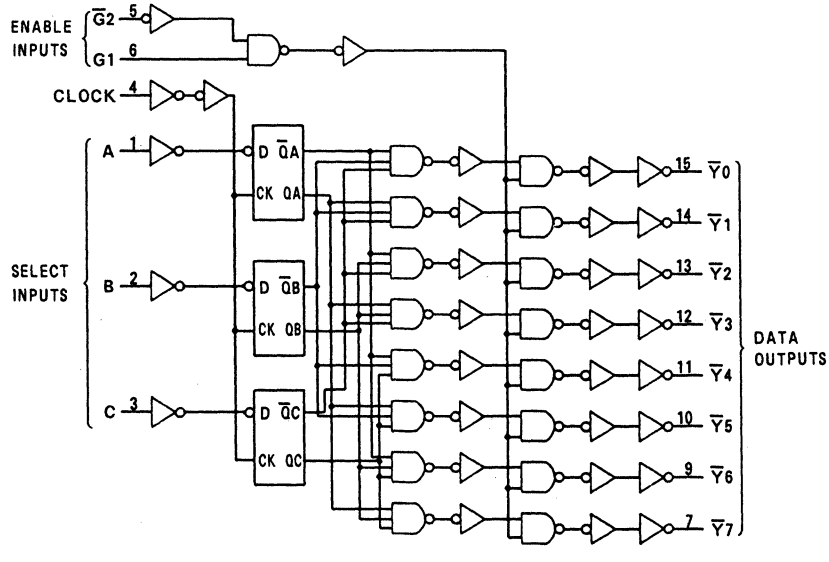


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE		CLOCK	SELECT											
G1	$\overline{G2}$		C	B	A	$\overline{Y}0$	$\overline{Y}1$	$\overline{Y}2$	$\overline{Y}3$	$\overline{Y}4$	$\overline{Y}5$	$\overline{Y}6$	$\overline{Y}7$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	↑	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}0$
H	L	↑	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}1$
H	L	↑	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}2$
H	L	↑	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}3$
H	L	↑	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}4$
H	L	↑	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}5$
H	L	↑	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}6$
H	L	↑	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}7$
H	L	↓	X	X	X	NO CHANGE								

X : DON'T CARE

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B, C)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−$\overline{Y}$)	t_{pLH} t_{pHL}		−	22	35	
Propagation Delay Time (G1, G2−$\overline{Y}$)	t_{pLH} t_{pHL}		−	12	24	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	78	200	−	240	
			4.5	−	26	40	−	48	
			6.0	−	22	34	−	41	
Propagation Delay Time (G1, $\overline{G2}$−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	60	140	−	175	
			4.5	−	15	28	−	35	
			6.0	−	13	24	−	30	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	37	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

QUAD 2-INPUT SCHMITT NAND GATE

The TC74HC132A is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fabricated with silicon gate C^2MOS technology.

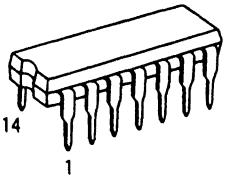
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as the TC74HC00A but the inputs have 25% V_{CC} hysteresis and with its schmitt trigger inputs, the TC74HC132A can be used as a line receiver for slow input signals.

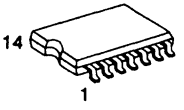
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

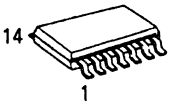
FEATURES:

- High Speed ..... t_{pd}=11ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_H=1.1V at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS132



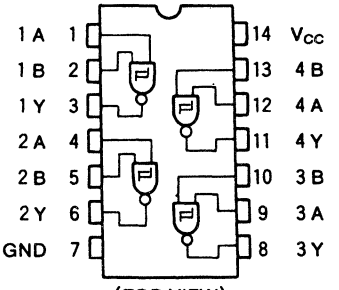
P(DIP14-P-300)





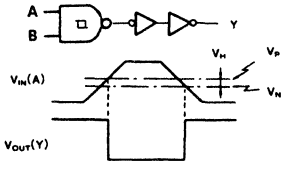
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT

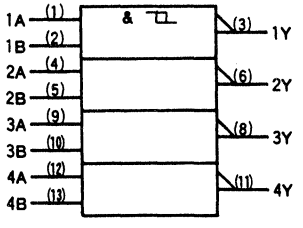


(TOP VIEW)

SYSTEM DIAGRAM,WAVEFORM



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			2.0	1.0	1.25	1.5	1.0	1.5	V
				4.5	2.3	2.7	3.15	2.3	3.15	
				6.0	3.0	3.5	4.2	3.0	4.2	
Negative Threshold Voltage	V_N			2.0	0.3	0.65	0.9	0.3	0.9	V
				4.5	1.13	1.6	2.0	1.13	2.0	
				6.0	1.5	2.3	2.6	1.5	2.6	
Hysteresis Voltage	V_H			2.0	0.3	0.6	1.0	0.3	1.0	V
				4.5	0.6	1.1	1.4	0.6	1.4	
				6.0	0.8	1.2	1.7	0.8	1.7	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	18	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	110	–	140	ns
			4.5	–	14	22	–	28	
			6.0	–	12	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	29	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

TC74HC133AP/AF

13-INPUT NAND GATE

The TC74HC133A is a high speed CMOS 13-INPUT NAND GATE fabricated with silicon gate C^2MOS technology.

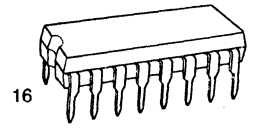
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 7 stages, including a buffer output, which provide high noise immunity and stable output.

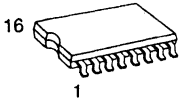
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS133

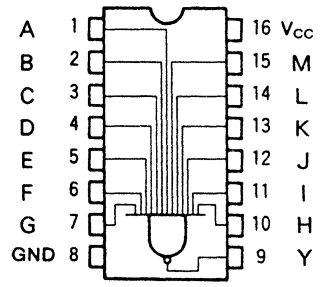


P(DIP16-P-300A)



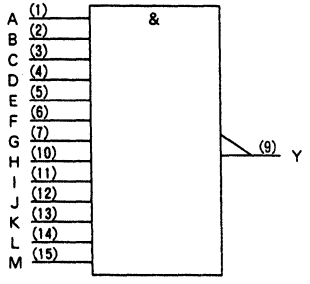
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs	Outputs
All Inputs High	L
All Other Combinations	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	13	22	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	42	130	–	165	
			4.5	–	16	26	–	33	
			6.0	–	14	22	–	28	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	29	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

3-TO-8 LINE DECODER/LATCH

The TC74HC137A is a high speed CMOS 3-to-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

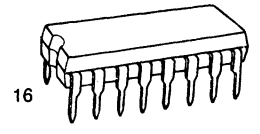
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It is composed of a 3-bit input latch with a common $\overline{GL}$ enable input and a 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of the outputs will go low. When the enable input G1 is held low or $\overline{G2}$ is held high, decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application of address decoder for memory system.

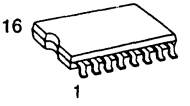
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS137

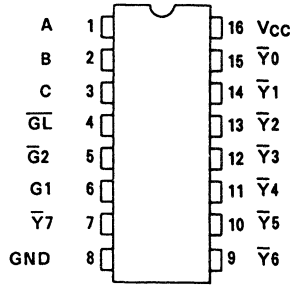


P(DIP16-P-300A)



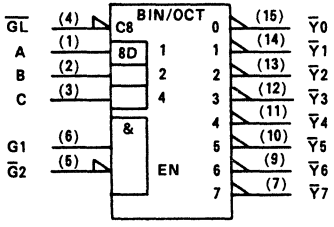
F(SOP16-P-300)

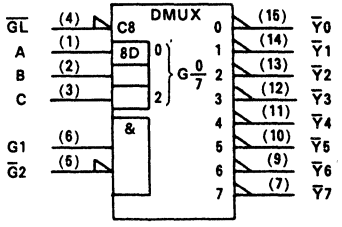
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



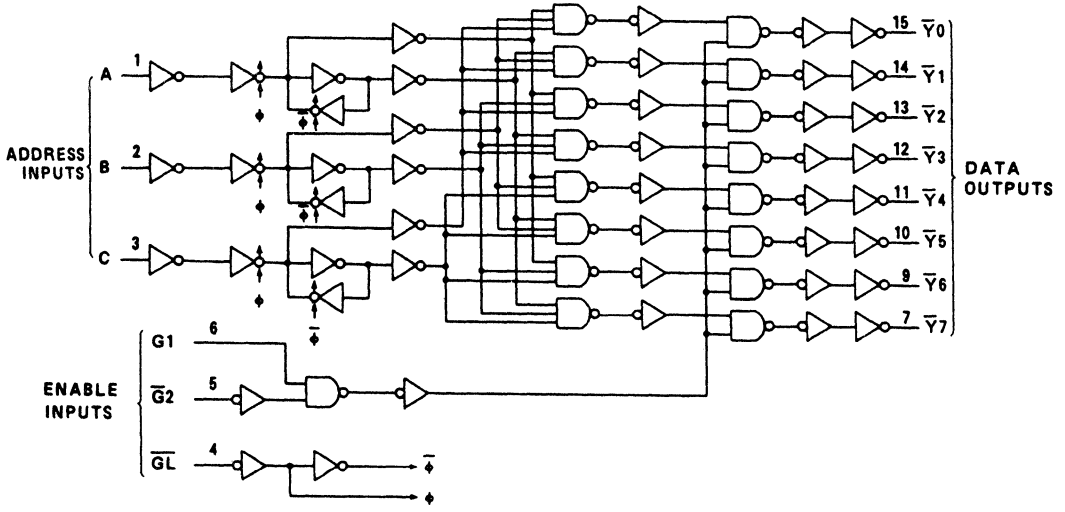


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			ADDRESS											
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
L	L	H	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
L	L	H	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
L	L	H	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
L	L	H	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
L	L	H	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
L	L	H	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
L	L	H	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
L	L	H	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$
H	L	H	X	X	X	OUTPUTS are latched at the time when $\overline{GL}$ is taken High level.								

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (A, B, C−$\overline{GL}$)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B, C−$\overline{GL}$)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		−	11	19	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pLH} t_{pHL}		−	12	19	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	18	29	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH} t_{pHL}		−	17	28	

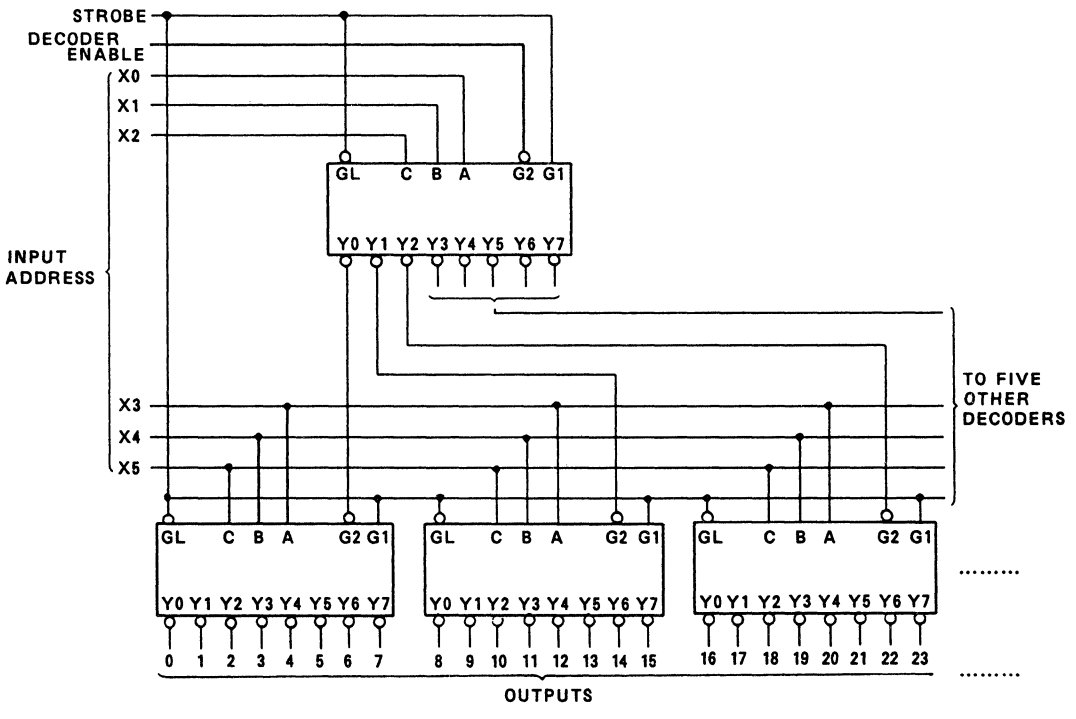
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (G1−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	−	45	115	−	145	
			4.5	−	14	23	−	29	
			6.0	−	12	20	−	25	
Propagation Delay Time ($\overline{G}$2−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	50	115	−	145	
			4.5	−	15	23	−	29	
			6.0	−	13	20	−	25	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	70	170	−	215	
			4.5	−	22	34	−	43	
			6.0	−	19	29	−	37	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pHL} t_{pHL}		2.0	−	70	165	−	205	
			4.5	−	21	33	−	41	
			6.0	−	18	28	−	35	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	56	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

3-TO-8 LINE DECODER/LATCH

The TC74HCT137A is a high speed CMOS 3-to-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

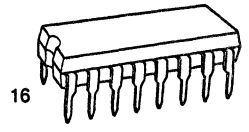
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

It is composed of a 3-bit input latch with a common $\overline{GL}$ enable input, and a 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of the outputs will go low. When the enable input G1 is held low or $\overline{G2}$ is held high, the decoding function is inhibited and all the 8 outputs go high. The two enable inputs are provided to ease cascade connection and permits the application of address decoder to memory systems.

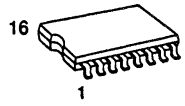
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH} =2V(Min.)
  V_{IL} =0.8V(Max.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS137

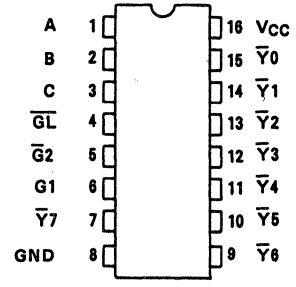


P(DIP16-P-300A)



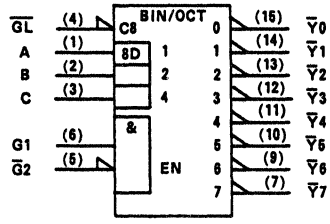
F(SOP16-P-300)

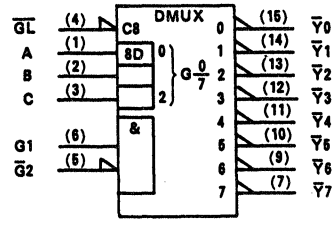
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



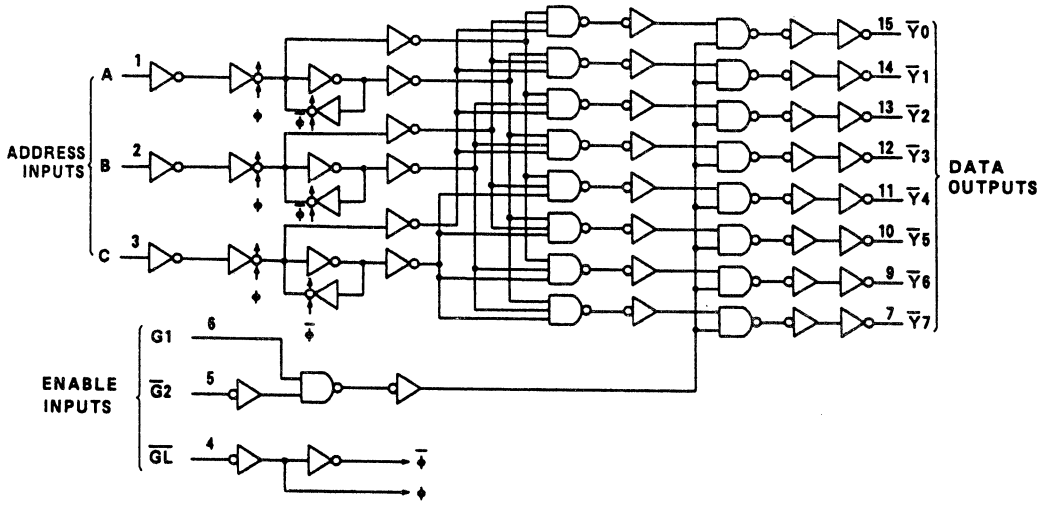


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			ADDRESS											
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
L	L	H	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
L	L	H	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
L	L	H	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
L	L	H	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
L	L	H	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
L	L	H	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
L	L	H	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
L	L	H	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$
H	L	H	X	X	X	OUTPUTS are latched at the time when $\overline{GL}$ is taken High level.								

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{OL}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{cc}	PER INPUT: V_{IN}=0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$		4.5	−	10	13	ns
			5.5	−	9	11	
Minimum Set-up Time (A, B, C−$\overline{GL}$)	t_s		4.5	−	10	13	
			5.5	−	9	11	
Minimum Hold Time (A, B, C−$\overline{GL}$)	t_h		4.5	−	5	5	
			5.5	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	6	12	ns
Propagation Delay Time ($\overline{G1}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	15	23	
Propagation Delay Time ($\overline{G2}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	15	23	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pLH} t_{pHL}		−	22	32	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pLH} t_{pHL}		−	21	32	

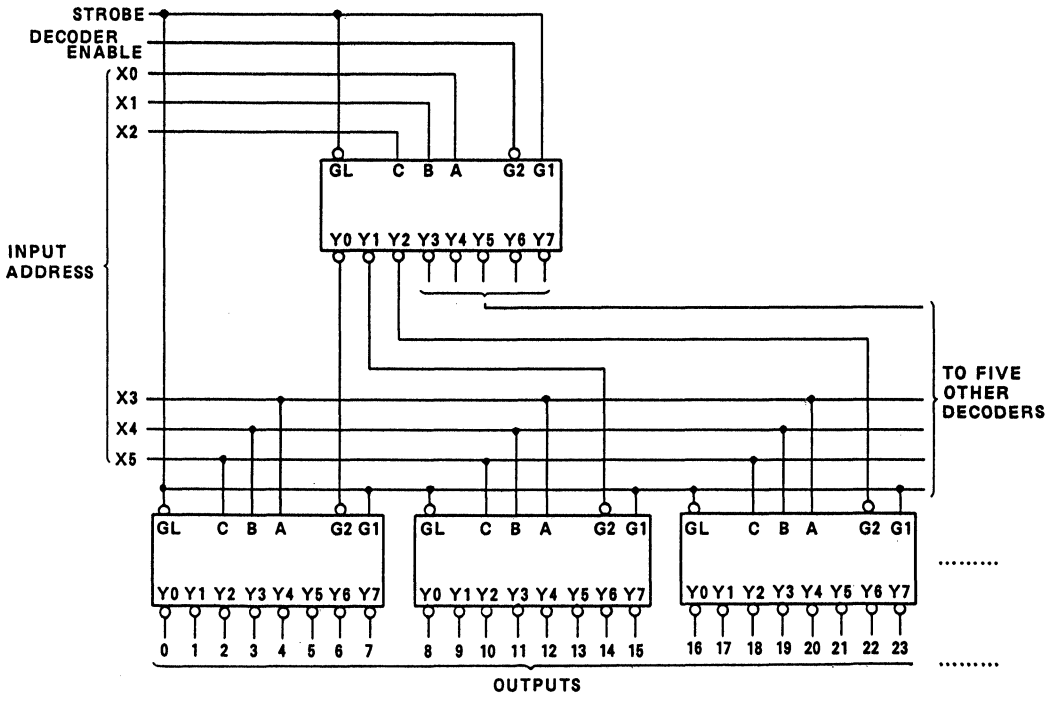
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	−	8	15	−	19	ns
			5.5	−	7	13	−	16	
Propagation Delay Time ($\overline{G1}$−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5	−	18	27	−	34	
			5.5	−	16	24	−	31	
Propagation Delay Time ($\overline{G2}$−$\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	19	29	−	36	
			5.5	−	17	26	−	33	
Propagation Delay Time ($\overline{GL}$−$\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	26	38	−	48	
			5.5	−	20	34	−	43	
Propagation Delay Time (A, B, C−$\overline{Y}$)	t_{pHL} t_{pHL}		4.5	−	25	38	−	48	
			5.5	−	23	34	−	43	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	56	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

NOTES

TC74HC138AP/AF/AFN

3-TO-8 LINE DECODER

The TC74HC138A is a high speed CMOS 3-to-8 DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs ($\overline{Y}0-\overline{Y}1$) will go low.

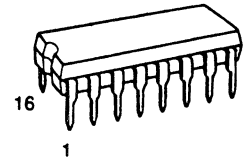
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

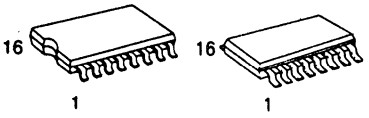
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=16ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS138.

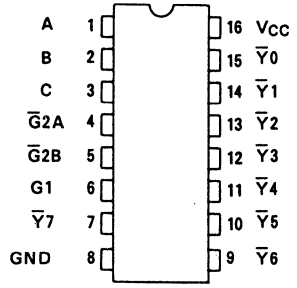


P(DIP16-P-300A)



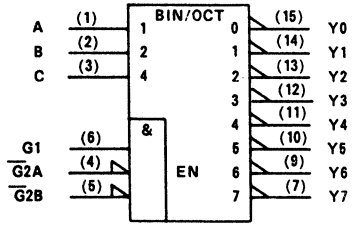
F(SOP16-P-300) FN(SOL16-P-150)

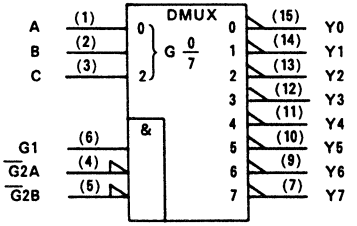
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



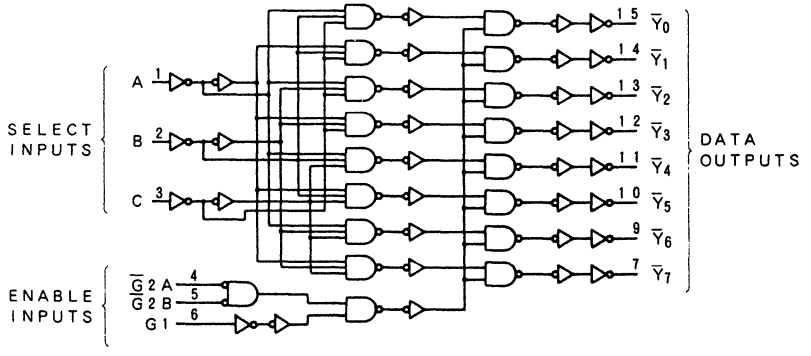


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		–	16	26	
Propagation Delay Time (G,$\overline{G}$−$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	25	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	70	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	16	26	–	32	
Propagation Delay Time (G,$\overline{G}$−$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	65	145	–	180	
			4.5	–	18	29	–	36	
			6.0	–	15	25	–	31	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	47	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

3-TO-8 LINE DECODER

The TC74HCT138A is a high speed CMOS 3-to-8 LINE DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL,NMOS and CMOS output voltage levels.

When the device is enabled, 3 Binary Select inputs (A,B and C) determine which one of the outputs (Y0-Y1) will go low.

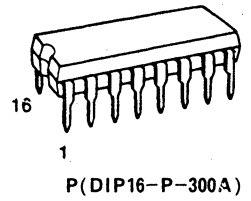
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high, decoding function is inhibited and all outputs go high.

G1, $\overline{G}2A$, and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

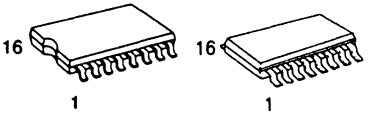
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=17ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs..... V_{IH} =2V (Min.)
  V_{IL} =0.8V(Max.)
- Wide interfacing ability.....LSTTL,NMOS,CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· t_{pLH}= t_{pHL}
- Pin and Function Compatible with 74LS138.

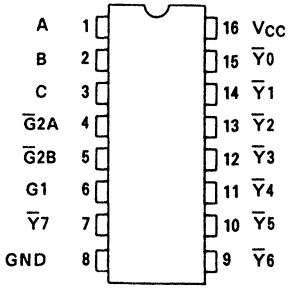


P(DIP16-P-300A)



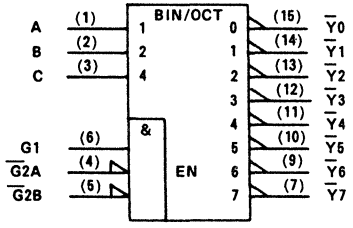
F(SOP16-P-300) FN(SOL16-P-150)

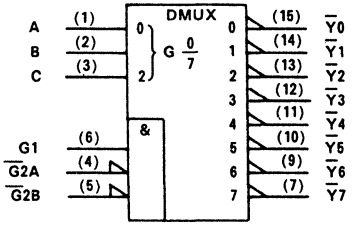
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



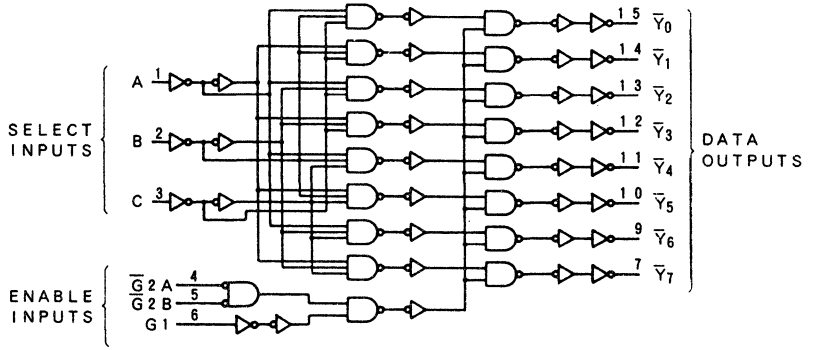


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH}=−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−4 mA	4.5	4.18	4.31	−	4.13	−	
High-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN}=0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		–	17	28	
Propagation Delay Time ($\overline{G1}$−$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	25	
Propagation Delay Time ($\overline{G2}$−$\overline{Y}$)	t_{pLH} t_{pHL}		–	17	28	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time (A,B,C−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	21 18	33 30	– –	44 40	
Propagation Delay Time ($\overline{G1}$−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	19 17	30 27	– –	38 34	
Propagation Delay Time ($\overline{G2}$−$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	22 20	33 30	– –	41 37	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	55	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC139AP/AF/AFN

DUAL 2-TO-4 LINE DECODER

The TC74HC139A is a high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

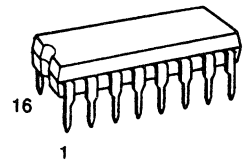
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held "H", all four outputs are fixed at a high logic level independent of the other inputs.

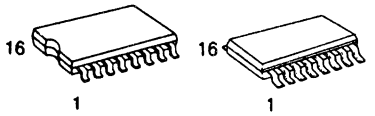
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS139

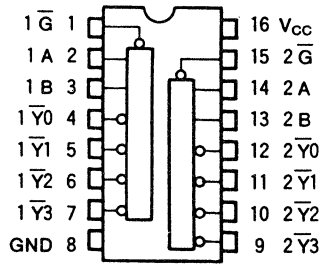


P(DIP16-P-300A)



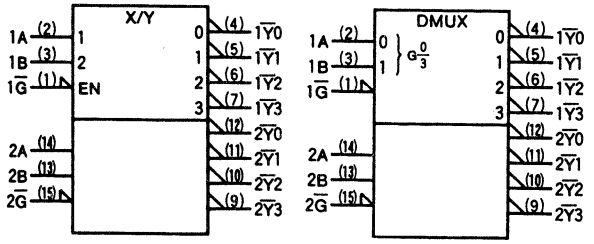
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
G̅	B	A	Y̅0	Y̅1	Y̅2	Y̅3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y̅0
L	L	H	H	L	H	H	Y̅1
L	H	L	H	H	L	R	Y̅2
L	H	H	H	H	H	L	Y̅3

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B–$\overline{Y}$)	t_{pLH} t_{pHL}		–	12	22	
Propagation Delay Time ($\overline{G}$–Y)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B–$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	45	130	–	165	
			4.5	–	15	26	–	33	
			6.0	–	13	22	–	28	
Propagation Delay Time ($\overline{G}$–Y)	t_{pLH} t_{pHL}		2.0	–	39	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	11	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	46	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

DUAL 2-TO-4 LINE DECODER

The TC74HCT139A is a high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

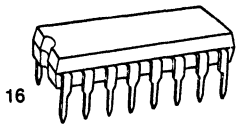
The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

When the enable input is held high, all four outputs are set to a high logic level independent of the other inputs.

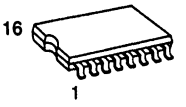
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ..... V_{IH} =2V(Min.)
  V_{IL} =0.8V(Max.)
- Wide Interfacing ability..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS139

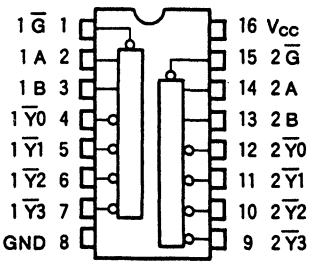


P(DIP16-P-300A)



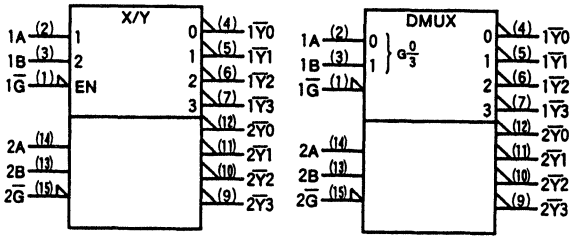
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS			OUTPUTS				SELECTED OUTPUT
ENABLE	SELECT						
G̅	B	A	Y̅0	Y̅1	Y̅2	Y̅3	
H	X	X	H	H	H	H	NONE
L	L	L	L	H	H	H	Y̅0
L	L	H	H	L	H	H	Y̅1
L	H	L	H	H	L	R	Y̅2
L	H	H	H	H	H	L	Y̅3

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperrature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r , t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} =0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	12	ns
Propagation Delay Time (A, B–$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	25	
Propagation Delay Time ($\overline{G}$–Y)	t_{pLH} t_{pHL}		–	14	23	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 17	ns
Propagation Delay Time (A, B–$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	19 16	30 27	– –	38 35	
Propagation Delay Time ($\overline{G}$–Y)	t_{pLH} t_{pHL}		4.5 5.5	– –	17 14	27 25	– –	34 31	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	40	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Decoder)}$$

NOTES

10-TO-4 LINE PRIORITY ENCODER

The TC74HC147A is a high speed CMOS LINE ENCODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC147A is 10-to-4 line priority encoder.

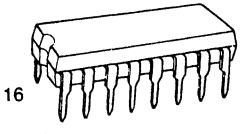
All data inputs and outputs of HC147A are active when low.

The HC147A detects a low on the highest order among nine input signals and outputs the corresponding signal position in BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are high.

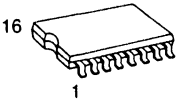
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=15ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS147.

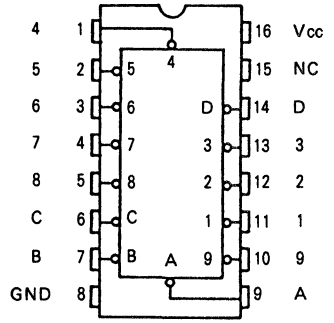


P(DIP16-P-300A)



F(SOP16-P-300)

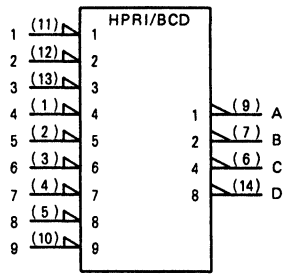
PIN ASSIGNMENT



(TOP VIEW)

NC:NO CONNECTION

IEC LOGIC SYMBOL

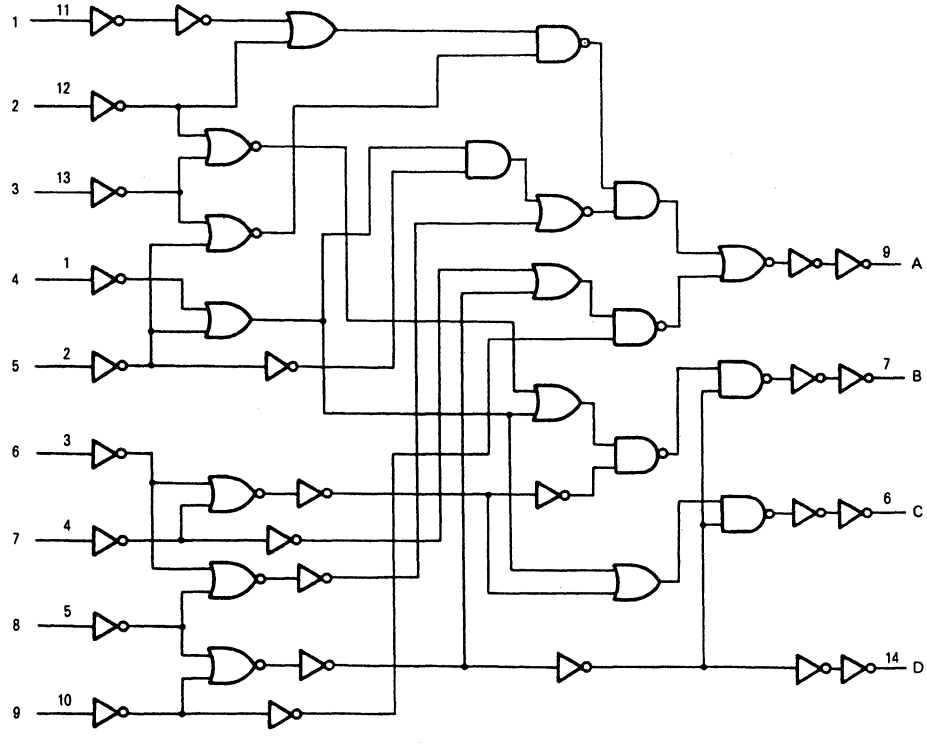


TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X:Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	15	25	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	60	150	–	190	ns
			4.5	–	18	30	–	38	
			6.0	–	15	26	–	33	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	24	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

8-TO-3 LINE PRIORITY ENCODER

The TC74HC148A is a high speed CMOS 8-to-3 LINE ENCODER fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

All data inputs and outputs of these encoders are active when low.

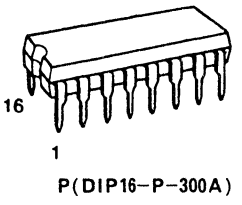
The encoder detects a low on the highest order among eight input signals and outputs the corresponding signal position in binary code.

Enable Input EI and Enable Output EO are used to easily cascade without using external circuits.

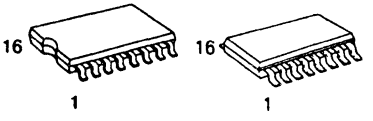
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=15ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS 148

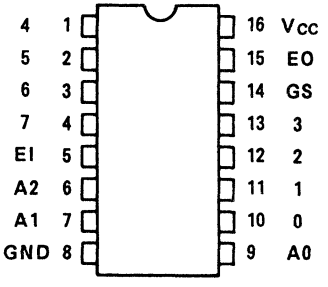


P(DIP16-P-300A)



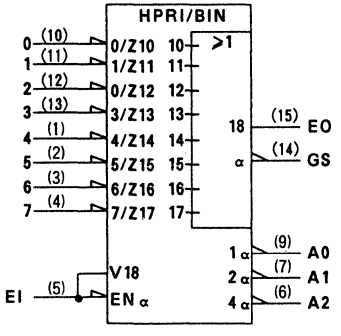
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

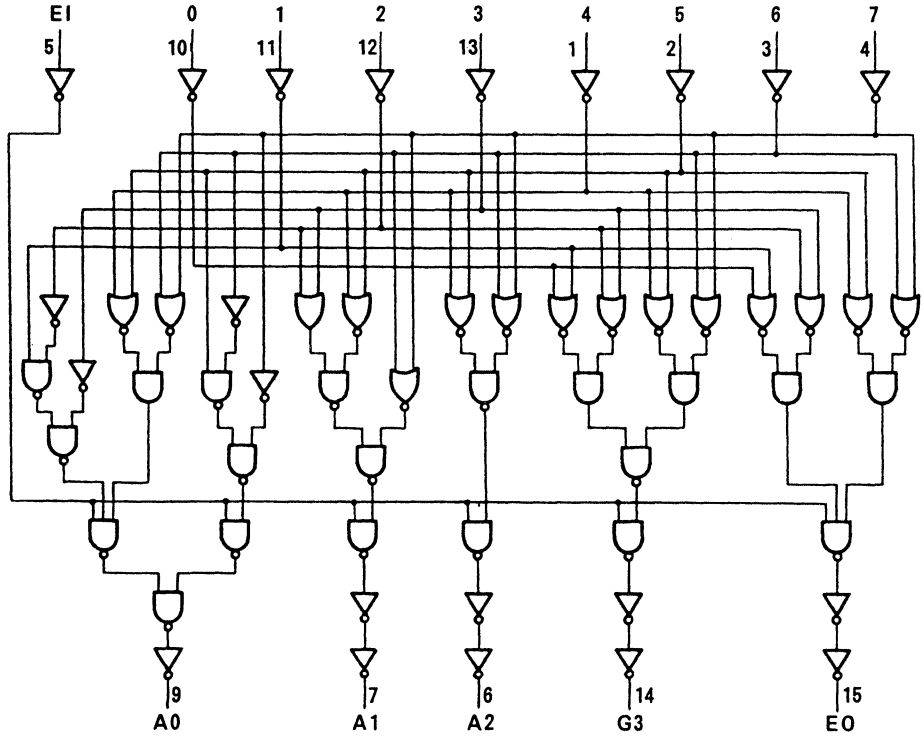


TRUTH TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X:Don't Care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (IN–A0,A1,A2)	t_{pLH} t_{pHL}		–	15	25	
Propagation Delay Time (IN–EO,ES)	t_{pLH} t_{pHL}		–	15	25	
Propagation Delay Time (EI–EO)	t_{pLH} t_{pHL}		–	11	19	
Propagation Delay Time (EI–GS)	t_{pLH} t_{pHL}		–	11	19	
Propagation Delay Time (EI–A0,A1,A2)	t_{pLH} t_{pHL}		–	11	19	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input tr=tf=6ns)

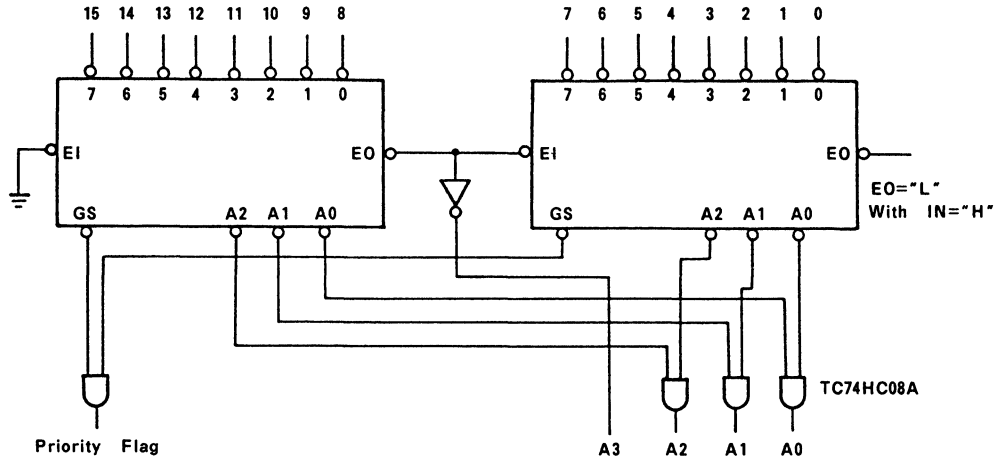
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=–40 ~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (IN–A0,A1,A2)	t_{pLH} t_{pHL}		2.0	–	52	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	15	26	–	33	
Propagation Delay Time (IN–EO,GS)	t_{pLH} t_{pHL}		2.0	–	52	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	15	26	–	33	
Propagation Delay Time (EI–EO)	t_{pLH} t_{pHL}		2.0	–	40	115	–	145	
			4.5	–	14	23	–	29	
			6.0	–	11	20	–	25	
Propagation Delay Time (EI–GS)	t_{pLH} t_{pHL}		2.0	–	40	115	–	145	
			4.5	–	14	23	–	29	
			6.0	–	12	20	–	25	
Propagation Delay Time (EI–A0,A1,A2)	t_{pLH} t_{pHL}		2.0	–	40	115	–	145	
			4.5	–	14	23	–	29	
			6.0	–	12	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}			–	55	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION

4–bit CASCADE CONNECTION



TC74HC151AP/AF/AFN

8-CHANNEL MULTIPLEXER

The TC74HC151A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

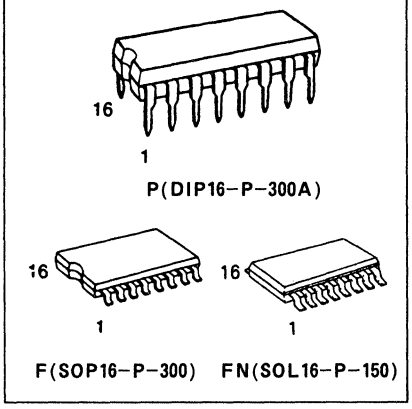
One of eight date input signals (D0-D7) is selected by decoding of the three-bit address input (A, B, C). The selected data appears on two outputs : non-inverting (Y) and inverting (W).

The strobe input provides two output conditions ; a low level on the strobe input transfers the selected data to the outputs. A high level on the strobe input sets the Y output low and the W output high without regard to the data or select input conditions.

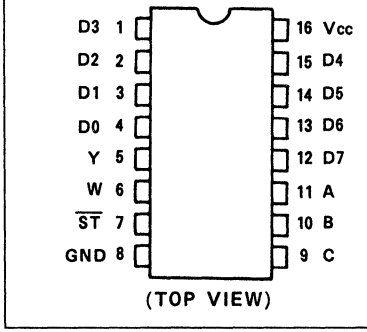
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS151



PIN ASSIGNMENT

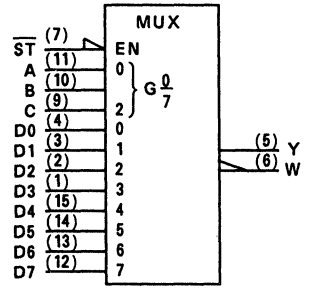


TRUTH TABLE

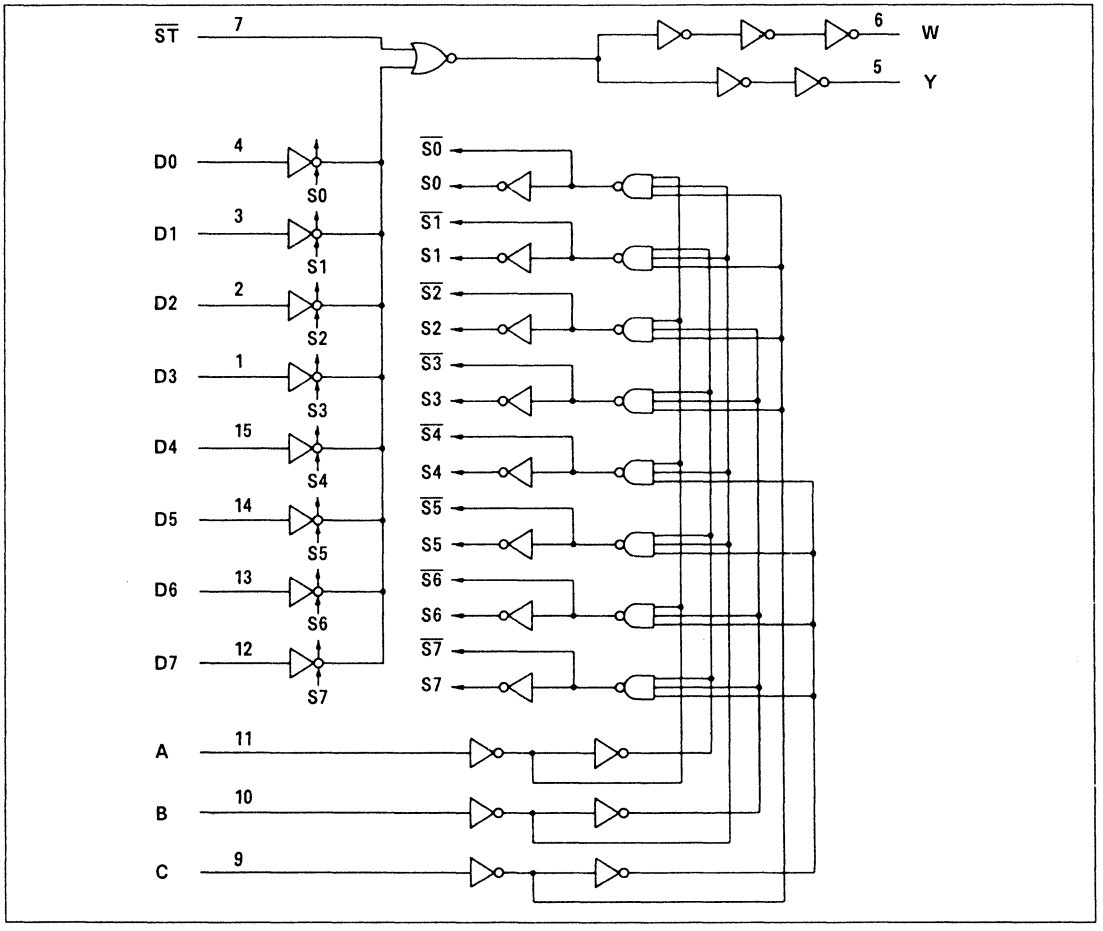
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{ST}$		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time ($\overline{ST}$–Y)	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time ($\overline{ST}$–W)	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		–	19	31	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time ($\overline{ST}$–Y)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time ($\overline{ST}$–W)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	69	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC\,opr} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC153AP/AF/AFN
TC74HC253AP/AF/AFN

TC74HC153AP/AF/AFN DUAL 4-CHANNEL MULTIPLEXER
TC74HC253AP/AF/AFN DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74HC153A and TC74HC253A are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC153A has standard outputs, while the TC74HC253A has 3-state outputs.

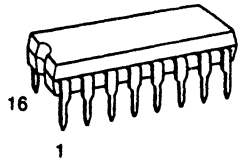
Input data (1C0~1C3, 2C0~2C3) are selected by the two address inputs, A and B.

Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections. They can be used to inhibit the data outputs. The output of the HC153A is set low, and the HC253A output is set to the high impedance state, when the strobe inputs are low.

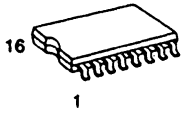
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

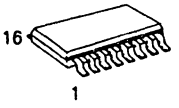
FEATURES:

- High Speed ····· t_{pd}=12ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS153,74LS253



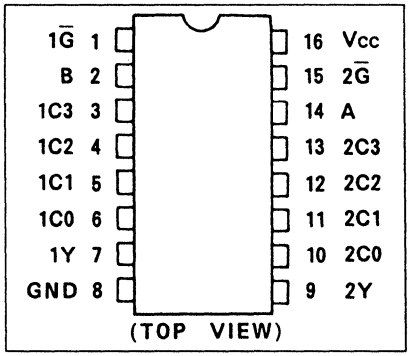
P(DIP16-P-300A)



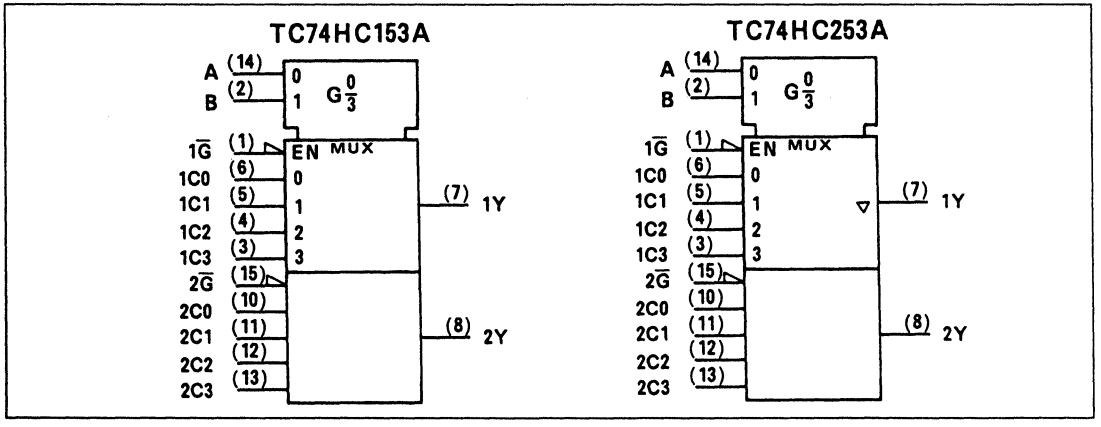


F(SOP16-P-300) FN(SOL16-P-150)

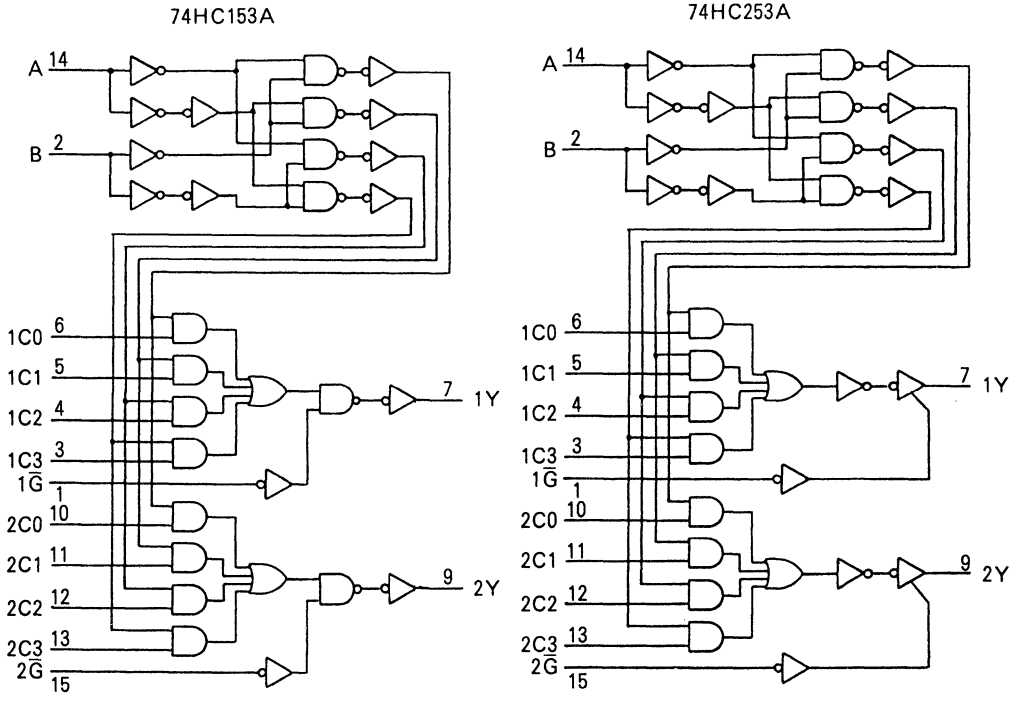
PIN ASSIGNMENT



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C0	C1	C2	C3	$\overline{G}$	HC153A	HC253A
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X : Don't care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}*	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

* TC74HC253A only

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (Cn–Y)	t_{pLH} t_{pHL}		–	12	19	
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		–	17	26	
Propagation Delay Time ($\overline{G}$–Y) *	t_{pLH} t_{pHL}		–	8	16	
3-State Output Enable Time ($\overline{G}$–Y) **	t_{pZL} t_{pZH}		–	9	16	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=–40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (Cn–Y)	t_{pLH} t_{pHL}		2.0	–	48	115	–	145	
			4.5	–	15	23	–	29	
			6.0	–	12	20	–	25	
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		2.0	–	68	150	–	190	
			4.5	–	20	30	–	38	
			6.0	–	16	26	–	33	
Propagation Delay Time (G–Y) *	t_{pLH} t_{pHL}		2.0	–	31	95	–	120	
			4.5	–	11	19	–	24	
			6.0	–	9	16	–	20	
3-State Output Enable Time (G–Y) **	t_{pZL} t_{pZH}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	9	17	–	21	
3-State Output Disable Time (G–Y) **	t_{pLZ} t_{pHZ}		2.0	–	22	115	–	145	
			4.5	–	13	23	–	29	
			6.0	–	11	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74HC153A		–	58	–	–	–	
		TC74HC253A		–	59	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

* for TC74HC153A only
** for TC74HC253A only

TC74HC154AP

4-TO-16 LINE DECODER

The TC74HC154A is a high speed CMOS 4 to 16 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology.

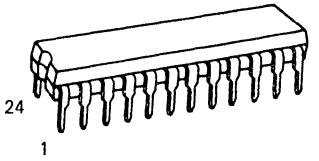
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A binary code applied to the four inputs A thru D is decoded within the device. Depending on the binary code, one of sixteen outputs goes low, when both the strobe inputs, $\overline{G}1$ and $\overline{G}2$, are held low. When either strobe input is held high, the decoding function is inhibited to keep all outputs high. The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decoding circuits in a memory control system.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

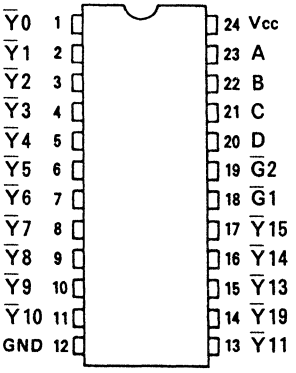
FEATURES:

- High Speed ····· t_{pd}=15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS154



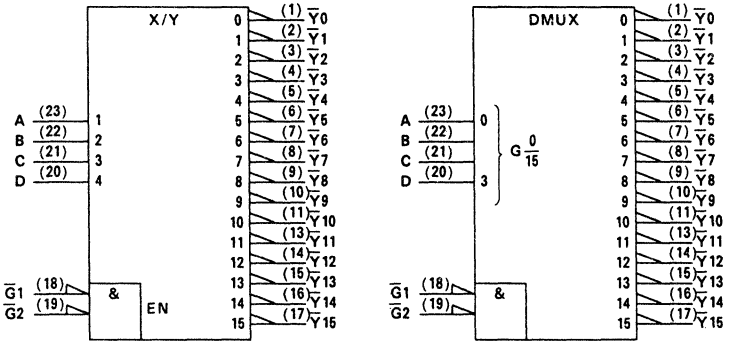
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

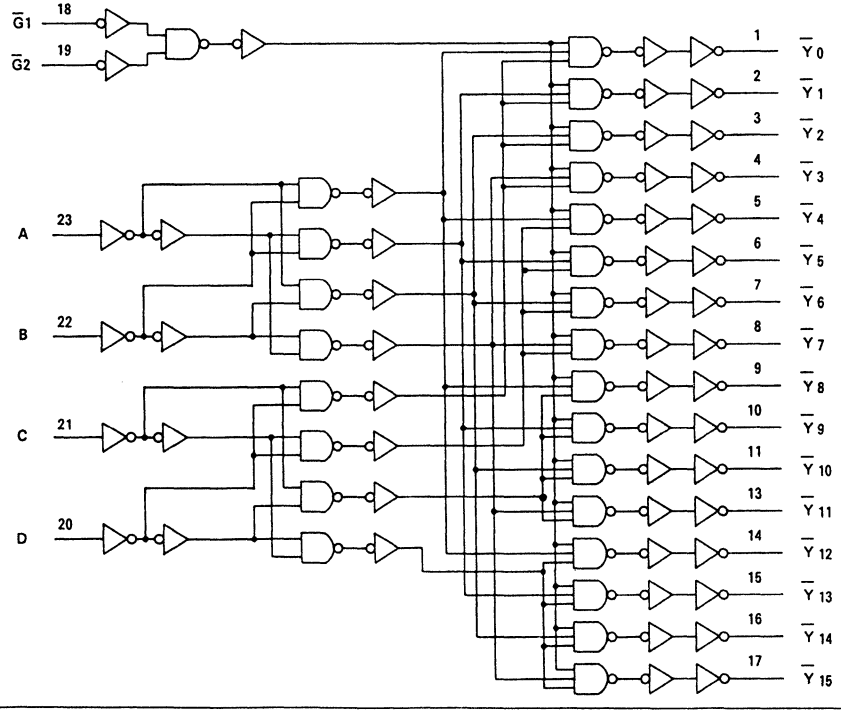


TRUTH TABLE

INPUT						SELECTED OUTPUT(L)
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y}0$
L	L	L	L	L	H	$\overline{Y}1$
L	L	L	L	H	L	$\overline{Y}2$
L	L	L	L	H	H	$\overline{Y}3$
L	L	L	H	L	L	$\overline{Y}4$
L	L	L	H	L	H	$\overline{Y}5$
L	L	L	H	H	L	$\overline{Y}6$
L	L	L	H	H	H	$\overline{Y}7$
L	L	H	L	L	L	$\overline{Y}8$
L	L	H	L	L	H	$\overline{Y}9$
L	L	H	L	H	L	$\overline{Y}10$
L	L	H	L	H	H	$\overline{Y}11$
L	L	H	H	L	L	$\overline{Y}12$
L	L	H	H	L	H	$\overline{Y}13$
L	L	H	H	H	L	$\overline{Y}14$
L	L	H	H	H	H	$\overline{Y}15$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r , t_f	0~1000(V_{CC} =2.0V) 0~ 500(V_{CC} =4.5V) 0~ 400(V_{CC} =6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.5 3.15 4.2	− − −	− − −	1.5 3.15 4.2	− − −	V
Low-Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.5 1.35 1.8	− − −	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH}=−4 mA I_{OH}=−5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL}=4 mA I_{OL}=5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A, B, C, D–$\overline{Y}$)	t_{pLH} t_{pHL}		–	15	30	
Propagation Delay Time ($\overline{G}1$, $\overline{G}2$–$\overline{Y}$)	t_{pLH} t_{pHL}		–	14	28	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, B, C, D–$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	65	175	–	220	
			4.5	–	19	35	–	44	
			6.0	–	16	30	–	37	
Propagation Delay Time ($\overline{G}1$, $\overline{G}2$–Y)	t_{pLH} t_{pHL}		2.0	–	55	160	–	200	
			4.5	–	17	32	–	40	
			6.0	–	15	27	–	34	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	57	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC155AP/AF/AFN

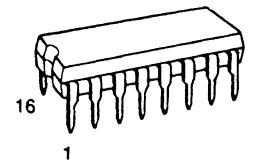
DUAL 2-TO-4 LINE DECODER/DUAL 3-TO-8 LINE DECODER

The TC74HC155A is a high speed CMOS DUAL 2-to-4 LINE DECODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It features dual 1-to-4 line demultiplexers with individual strobe inputs(1G and 2G),individual data inputs(1C and 2C)and common binary address inputs(A and B).
When both decoders are enabled by the strobes,the inverted output of 1C data and non-inverted output of 2C data will be brought to the selected output pins of each section.
A 1-to-8 line demultiplexer can be easily built up by providing a data signal to both the 1C and 2C inputs;the output order will be 1Y3(MSB),1Y2,1Y1,1Y0,2Y3,2Y2,2Y1,2Y0(LSB).
This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and 2C is held low.

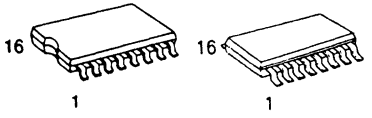
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =12ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS155

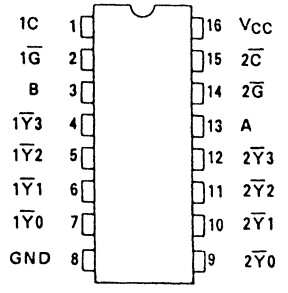


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

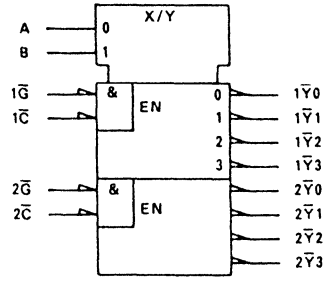
INPUTS				OUTPUTS			
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X : DON'T CARE

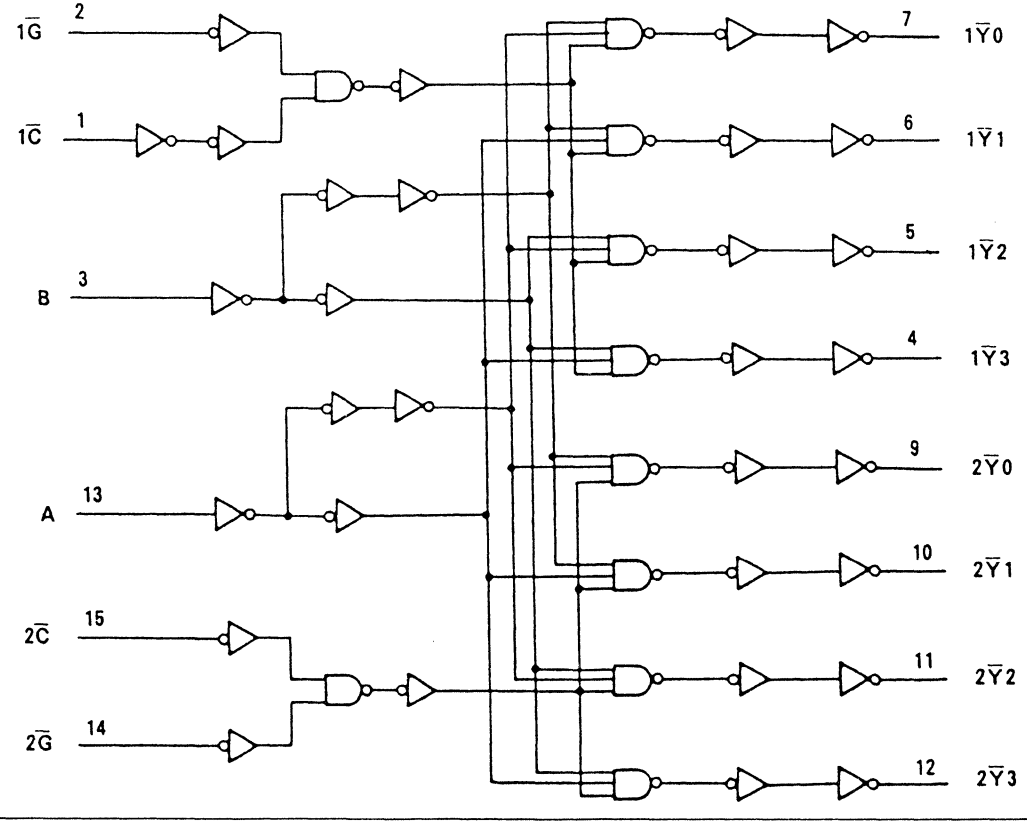
INPUTS				OUTPUTS			
B	A	2G	2C	2Y0	2Y1	2Y3	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

X : DON'T CARE

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	12	22	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	45	130	–	165	ns
			4.5	–	15	26	–	33	
			6.0	–	13	22	–	28	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	(Note 1)		–	53	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC157AP/AF/AFN
TC74HC158AP/AF/AFN

TC74HC157AP/AF/AFN QUAD 2-CHANNEL MULTIPLEXER
TC74HC158AP/AF/AFN QUAD 2-CHANNEL MULTIPLEXER(INVERTING)

The TC74HC157A and TC74HC158A are high speed CMOS 2-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC158A is an inverting multiplexer while the TC74HC157A is a non-inverting.

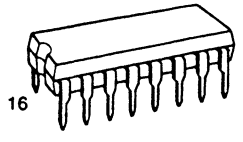
When $\overline{STROBE}$ is held high, selection of data is inhibited and all the outputs become low in the case of HC157A or high in the case of HC158A.

The SELECT decoding determines whether the A or B inputs get transferred to their corresponding Y ($\overline{Y}$) outputs.

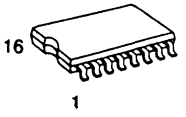
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

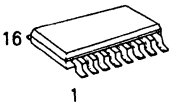
FEATURES:

- High Speed ..... t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS157/158



P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

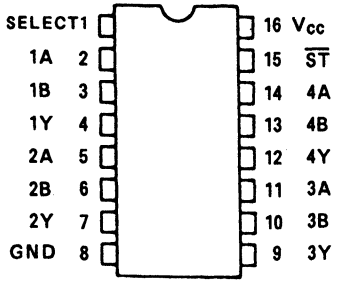
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{ST}$	SELECT	A	B	Y(157A)	$\overline{Y}$(158A)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care

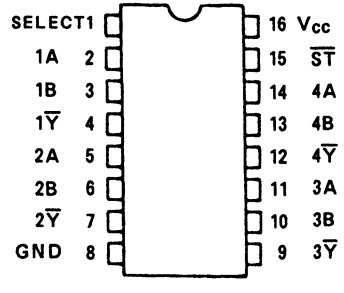
PIN ASSIGNMENT

TC74HC157A



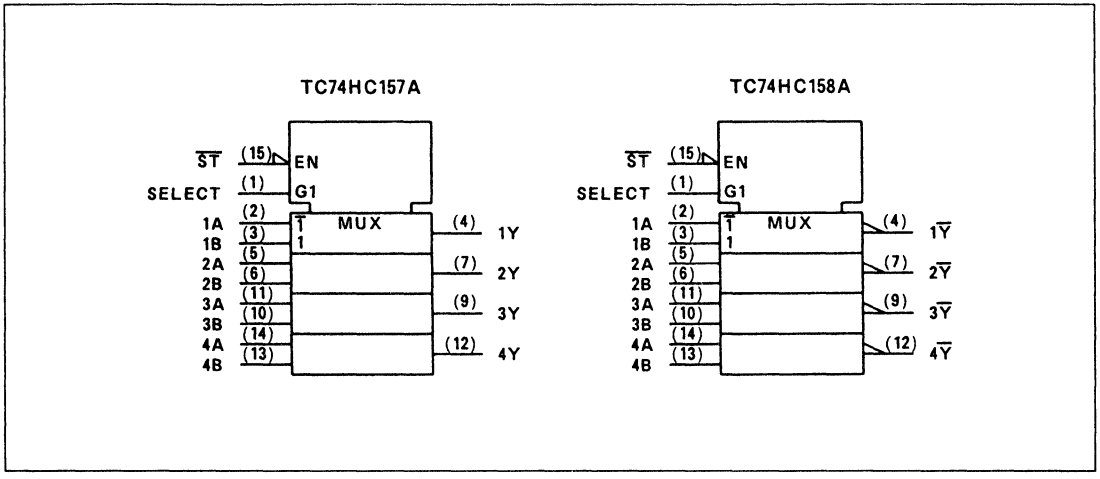
(TOP VIEW)

TC74HC158A



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		–	10	16	
Propagation Delay Time (SELECT–Y)	t_{pLH} t_{pHL}		–	13	21	
Propagation Delay Time ($\overline{STOROBE}$–Y)	t_{pLH} t_{pHL}		–	10	19	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B–Y)	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time (SELECT–Y)	t_{pLH} t_{pHL}		2.0	–	50	125	–	155	
			4.5	–	16	25	–	31	
			6.0	–	14	21	–	26	
Propagation Delay Time ($\overline{STOROBE}$–Y)	t_{pLH} t_{pHL}		2.0	–	36	115	–	145	
			4.5	–	12	23	–	29	
			6.0	–	10	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC157A			57	–	–	–	
		TC74HC158A			53	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

TC74HCT157AP/AF
TC74HCT158AP/AF

TC74HCT157AP/AF QUAD 2-CHANNEL MULTIPLEXER
TC74HCT158AP/AF QUAD 2-CHANNEL MULTIPLEXER(INVERTING)

The TC74HCT157A and TC74HCT158A are high speed CMOS 2-CHANNEL MULTIPLEXERs fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HCT158A is an inverting multiplexer while the TC74HCT157A is non-inverting.

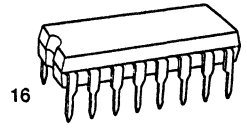
When $\overline{\text{STROBE}}$ is held high, selection of data is inhibited and all the outputs become low in the case of HCT157A or high in the case of HCT158A.

The SELECT decoding determines whether the A or B inputs get transferred to their corresponding Y ($\overline{Y}$) outputs.

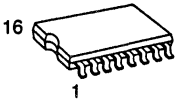
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=8ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Wide Interfacing ability ····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS157/158



P(DIP16-P-300A)



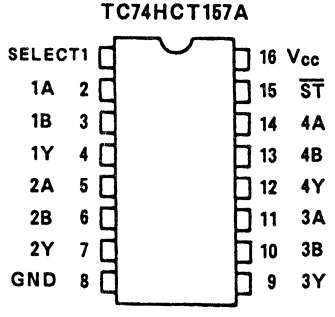
F(SOP16-P-300)

TRUTH TABLE

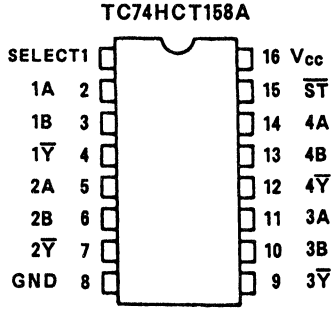
INPUTS				OUTPUTS	
$\overline{ST}$	SELECT	A	B	Y(157A)	$\overline{Y}$(158A)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care

PIN ASSIGNMENT

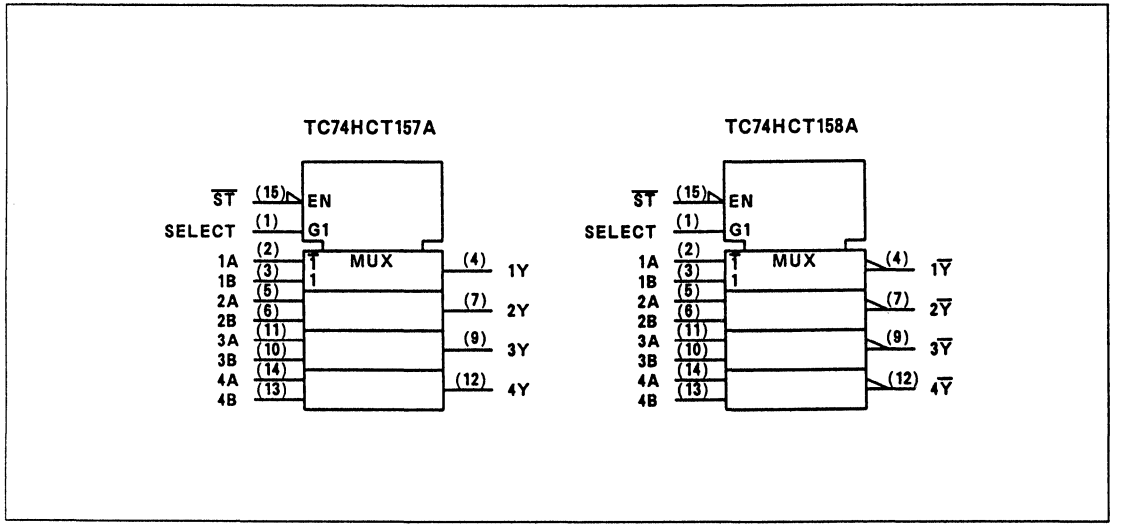


(TOP VIEW)



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500(V_{CC}=4.5V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	− − −	− − −	2.0	− − −	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	− − −	− − −	0.8	− − −	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{cc}	PER INPUT: V_{IN} =0.5V or 2.4V OTHER INPUT: Vcc or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		–	19	30	
Propagation Delay Time ($\overline{STOROBE}$-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		–	19	30	
Propagation Delay Time • (SELECT-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		–	21	32	
Propagation Delay Time •• (SELECT-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		–	23	35	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40 ~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5 5.5	– –	8 7	15 14	– –	19 18	ns
Propagation Delay Time (A,B-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	23 20	35 32	– –	44 40	
Propagation Delay Time ($\overline{STOROBE}$-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	23 20	35 32	– –	44 40	
Propagation Delay Time * (SELECT-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	25 21	37 34	– –	46 42	
Propagation Delay Time ** (SELECT-Y,$\overline{Y}$)	t_{pLH} t_{pHL}		4.5 5.5	– –	27 25	40 36	– –	50 45	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT157A		–	59	–	–	–	
		TC74HCT158A		–	56	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

* TC74HC157A only.
** TC74HC157A only.

TC74HC160AP/AF·TC74HC161AP/AF/AFN
TC74HC162AP/AF·TC74HC163AP/AF/AFN

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

TC74HC160AP/AF	DECADE, ASYNCHRONOUS CLEAR
TC74HC161AP/AF/AFN	BINARY, ASYNCHRONOUS CLEAR
TC74HC162AP/AF	DECADE, SYNCHRONOUS CLEAR
TC74HC163AP/AF/AFN	BINARY, SYNCHRONOUS CLEAR

The TC74HC160A, 161A, 162A and 163A are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC160A/162A are BCD decade counters and the TC74HC161A/163A are 4 bit binary counters.

The CLOCK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLEAR}}$ inputs are active on low logic level.

Presetting of all four IC's is synchronous to the rising edge of CLOCK.

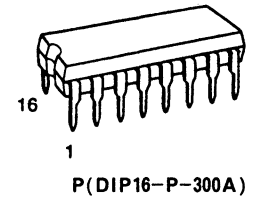
The clear function of the TC74HC162A/163A is synchronous to CLOCK, while the TC74HC160A/161A are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

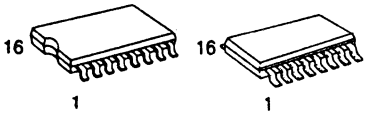
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=63MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS160~163

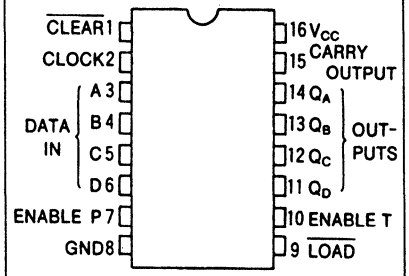


P(DIP16-P-300A)



F(SOP16-P-300) FN(SOL16-P-150)

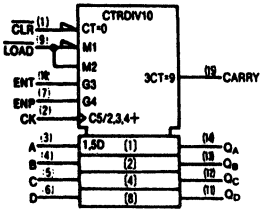
PIN ASSIGNMENT



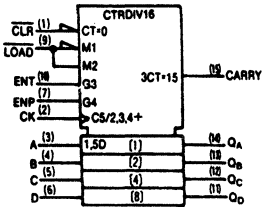
(TOP VIEW)

IEC LOGIC SYMBOL

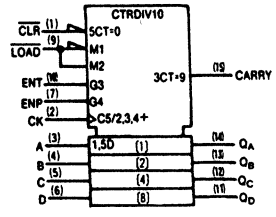
TC74HC160A



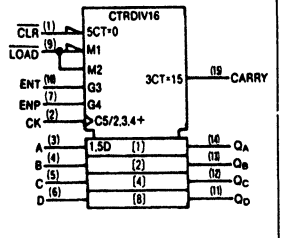
TC74HC161A



TC74HC162A



TC74HC163A



TRUTH TABLE

TC74HC160A/161A INPUTS					TC74HC162A/163A INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

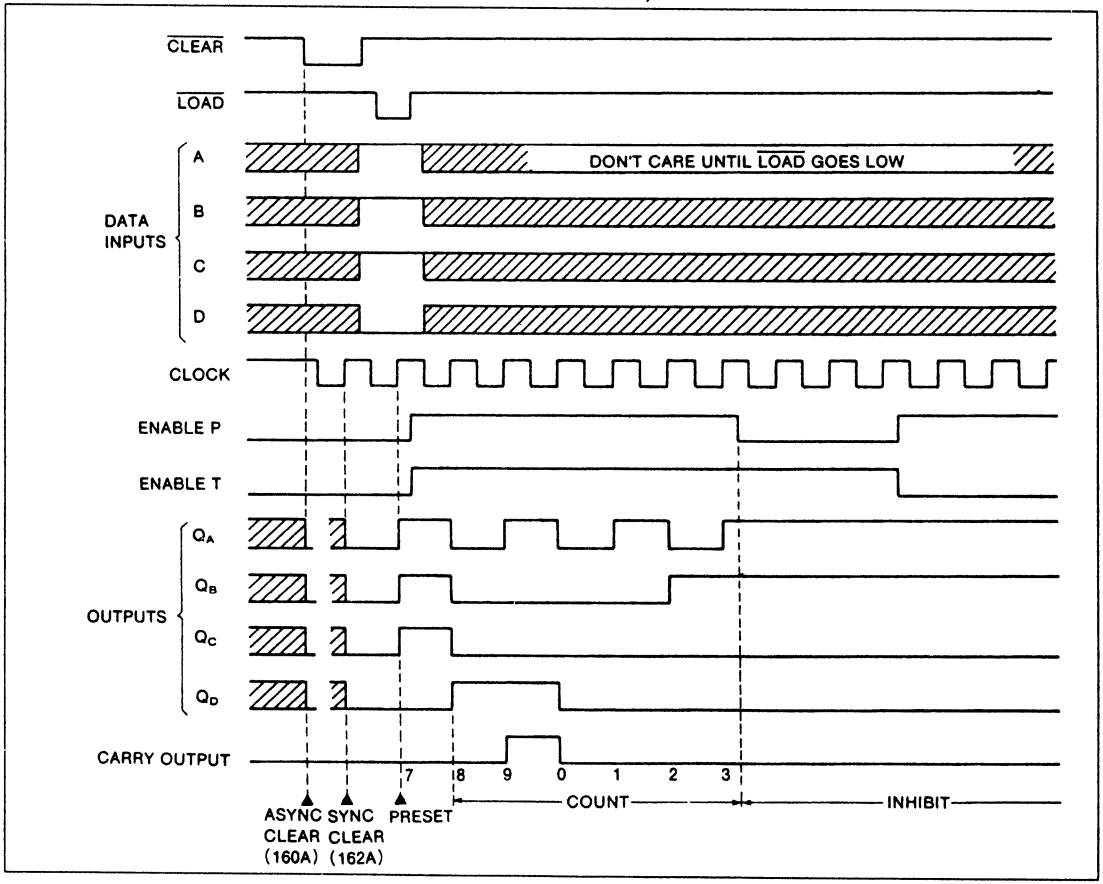
Note X : Don't care

A, B, C, D : Logic Level of Data Inputs

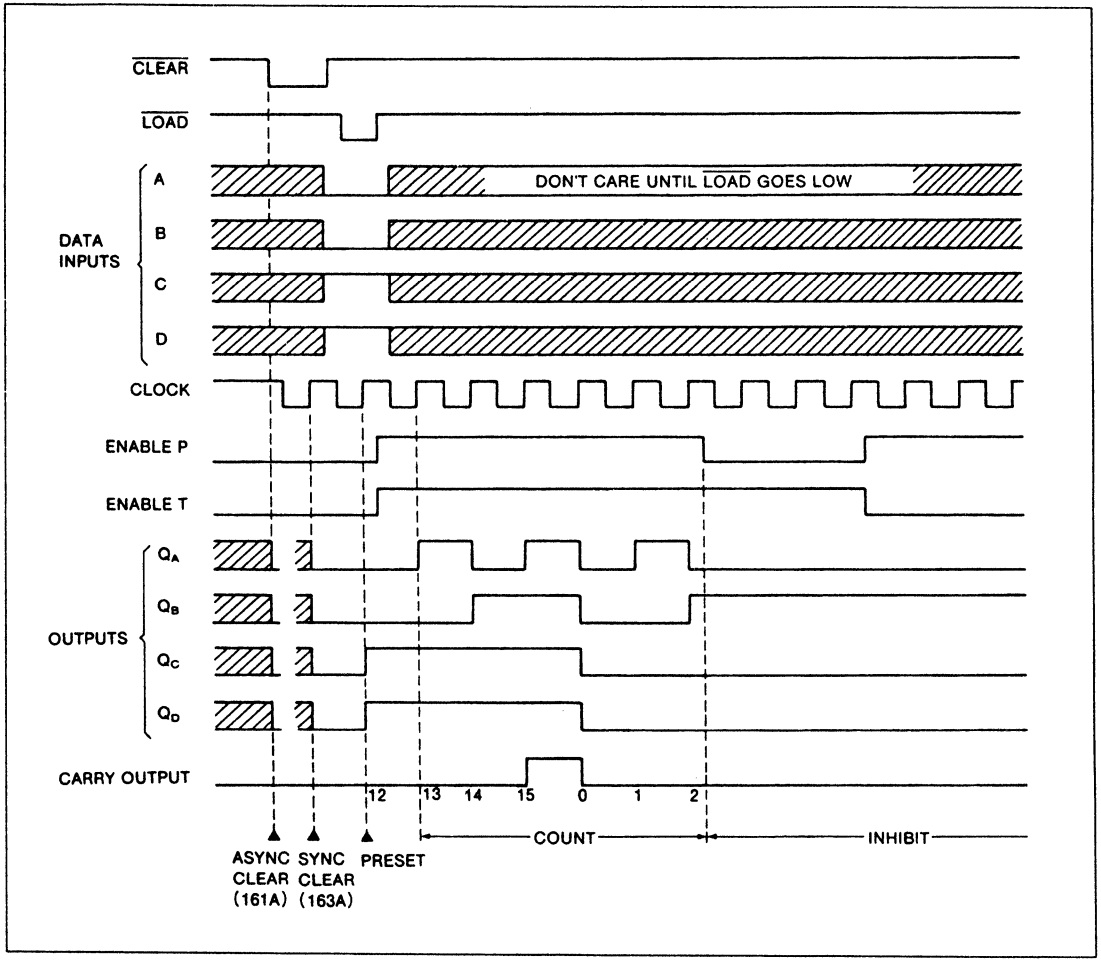
Carry : CARRY=ENT·Q_A·$\overline{Q_B}$·$\overline{Q_C}$·Q_D·····(TC74HC160A/162A)

CARRY=ENT·Q_A·Q_B·Q_C·Q_D·····(TC74HC161A/163A)

TIMING CHART (TC74HC160A/162A: DECADE COUNTER)

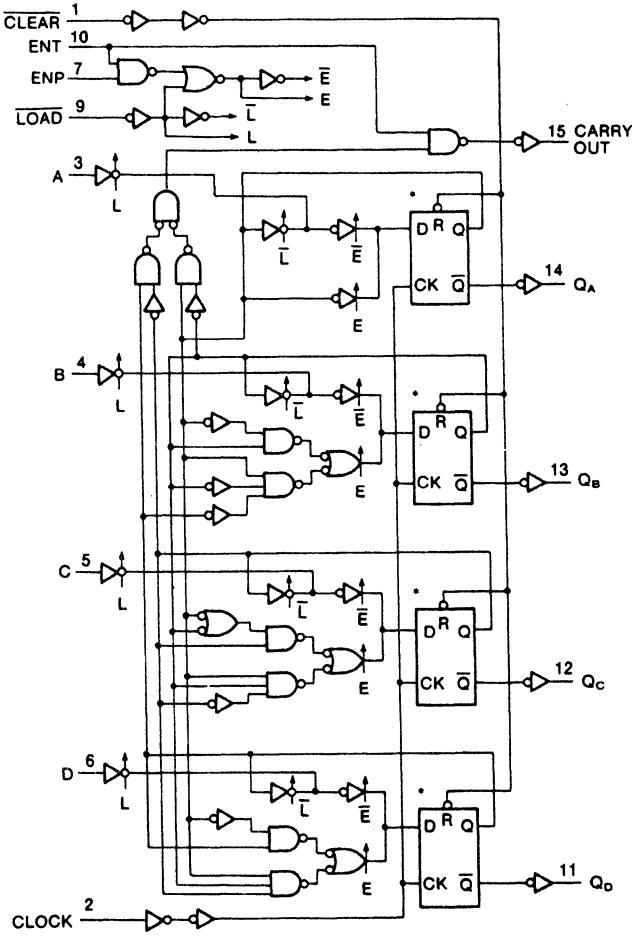


TIMING CHART (TC74HC161A/163A: BINARY COUNTER)



SYSTEM DIAGRAM

TC74HC160A/TC74HC162A



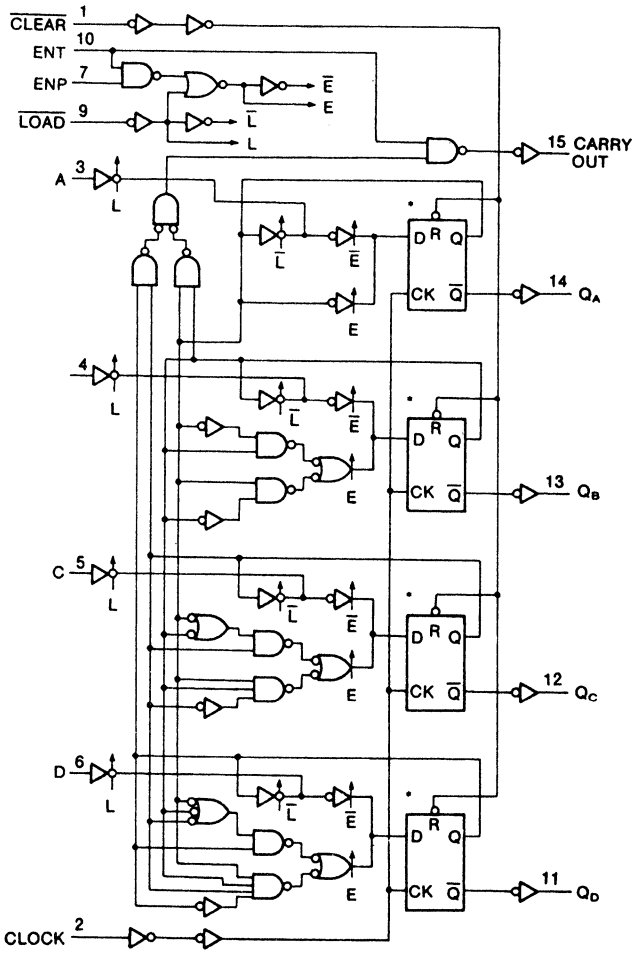
*TRUTH TABLE OF INTERNAL F/F

TC74HC160A					TC74HC162A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↑	L	L	H
L	↑	H	L	H	L	↑	H	L	H
H	↑	H	H	L	H	↑	H	H	L
X	↓	H	NO CHANGE		L	↓	H	NO CHANGE	

X : Don't Care

SYSTEM DIAGRAM

TC74HC161A/TC74HC163A



*TRUTH TABLE OF INTERNAL F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↑	L	L	H
L	↑	H	L	H	L	↑	H	L	H
H	↑	H	H	L	H	↑	H	H	L
X	↓	H	NO CHANGE		L	↓	H	NO CHANGE	

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$	Fig. 1	2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)*	$t_{W(L)}$	Fig. 4	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (LOAD, ENP, ENT)	t_s	Fig. 2, 3	2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (A, B, C, D)	t_s	Fig. 2	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (CLEAR)**	t_s	Fig. 5	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h	Fig. 2, 3, 5	2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time (CLEAR)*	t_{rem}	Fig. 4	2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}	Fig. 1	−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}	Fig. 1	−	13	21	
Propagation Delay Time (CLOCK−CARRY) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	−	16	26	
Propagation Delay Time (CLOCK−CARRY) [Preset Mode]	t_{pLH}	Fig. 2	−	18	30	
	t_{pHL}		−	20	35	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}	Fig. 6	−	10	17	
Propagation Delay Time (CLEAR−Q)*	t_{pHL}	Fig. 4	−	17	26	
Propagation Delay Time (CLEAR−CARRY)*	t_{pHL}	Fig. 4	−	20	35	
Maximum Clock Frequency	f_{MAX}		36	63	−	MHz

* : for TC74HC160A/161A only
** : for TC74HC162A/163A only

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}	Fig. 1	2.0	−	48	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	14	21	−	26	
Propagation Delay Time (CLOCK−CARRY) [Count Mode]	t_{pLH} t_{pHL}	Fig. 1	2.0	−	57	150	−	190	
			4.5	−	19	30	−	38	
			6.0	−	16	26	−	33	
Propagation Delay Time (CLOCK−CARRY) [Preset Mode]	t_{pLH}	Fig. 2	2.0	−	66	175	−	220	
			4.5	−	22	35	−	44	
			6.0	−	19	30	−	37	
	t_{pHL}		2.0	−	72	200	−	250	
			4.5	−	24	40	−	50	
			6.0	−	20	34	−	43	
Propagation Delay Time (ENT−CARRY)	t_{pLH} t_{pHL}	Fig. 6	2.0	−	39	100	−	125	
			4.5	−	13	20	−	25	
			6.0	−	11	17	−	21	
Propagation Delay Time (CLEAR−Q) *	t_{pHL}	Fig. 4	2.0	−	60	150	−	190	
			4.5	−	20	30	−	38	
			6.0	−	17	26	−	33	
Propagation Delay Time (CLEAR−CARRY)*	t_{pHL}	Fig. 4	2.0	−	72	200	−	250	
			4.5	−	24	40	−	50	
			6.0	−	20	34	−	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	62	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)	(注 1)		−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and $\triangle I_{CC}$ which is obtained from the following formula:

In case of TC74HC160A/162A:

$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{CO}}{10} \right)$$

In case of TC74HC161A/163A:

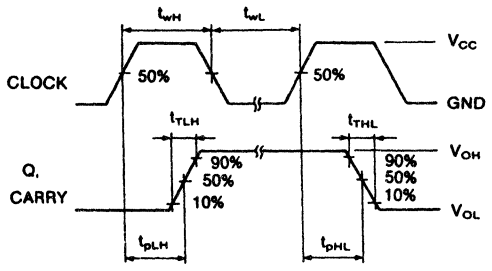
$$\triangle I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
f_{CK} is the input frequency of the CLOCK.

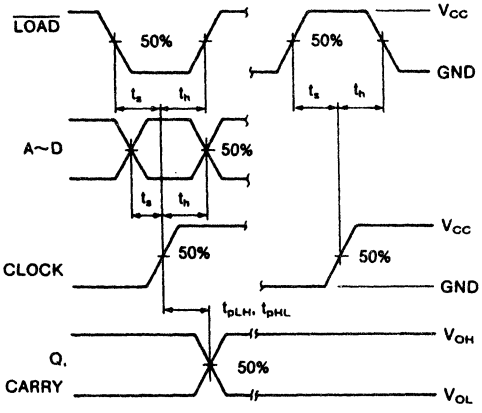
(2) * for TC74HC160A/161A only

SWITCHING CHARACTERISTICS TEST WAVEFORM

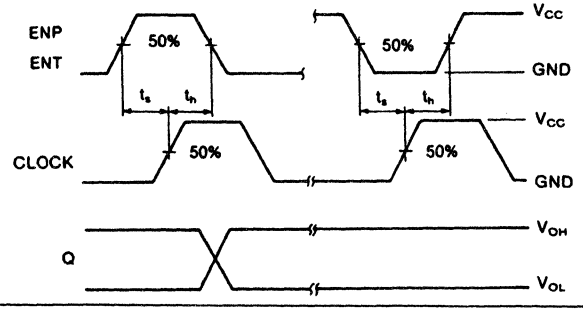
COUNT MODE (Fig. 1)



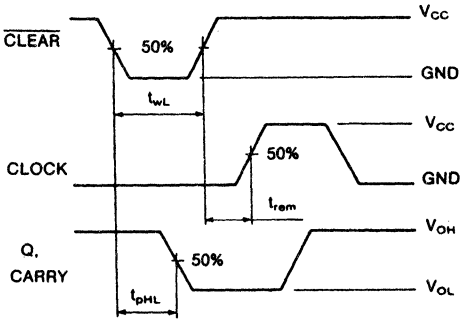
PRESET MODE (Fig. 2)



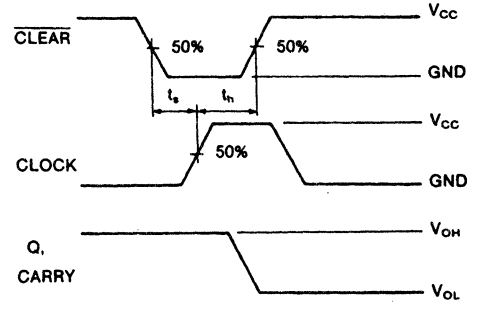
COUNT ENABLE MODE (Fig. 3)



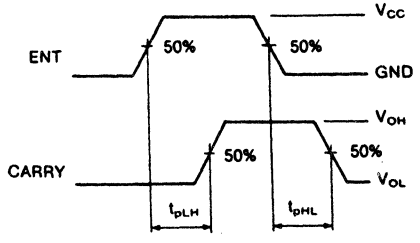
CLEAR MODE (TC74HC160A/161A) (Fig. 4)



CLEAR MODE (TC74HC162A/163A) (Fig. 5)

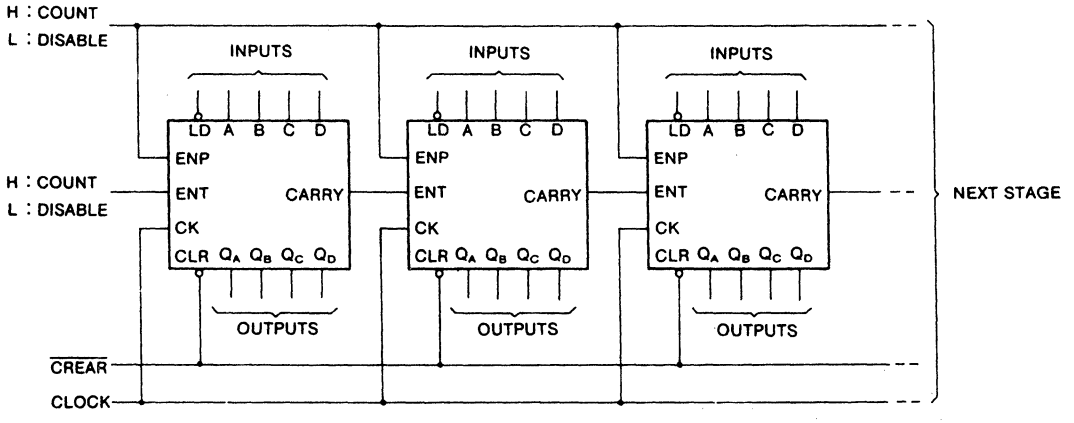


CASCADE MODE (Fix Maximum Count) (Fig. 6)



TYPICAL APPLICATION

PARALLEL CARRY N-BIT COUNTER



TC74HC164AP/AF/AFN

8-BIT SHIFT REGISTER(S-IN, P-OUT)

The TC74HC164A is a high speed CMOS 8-BIT SERIAL -IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

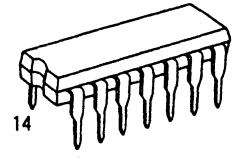
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of a serial-in, parallel-out 8-bit shift register with a CLOCK input and an overriding $\overline{CLEAR}$ input. Two serial data inputs (A, B) are provided so that one may be used as a data enable.

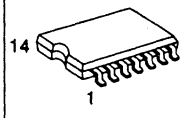
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

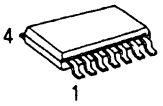
FEATURES:

- High Speed ····· f_{MAX}=58MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS164



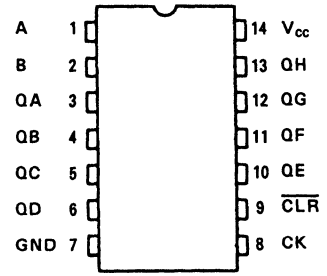
P(DIP14-P-300)





F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(TOP VIEW)

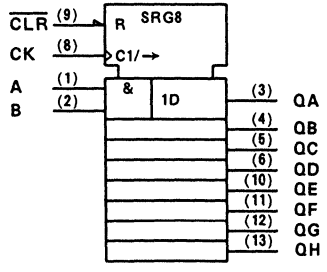
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{CLR}$	CK	SERIAL IN		QA	QB	···	QH
		A	B				
L	X	X	X	L	L	···	L
H	↓	X	X	NO CHANGE			
H	↓	L	X	L	QAn	···	QGn
H	↓	X	L	L	QAn	···	QGn
H	↓	H	H	H	QAn	···	QGn

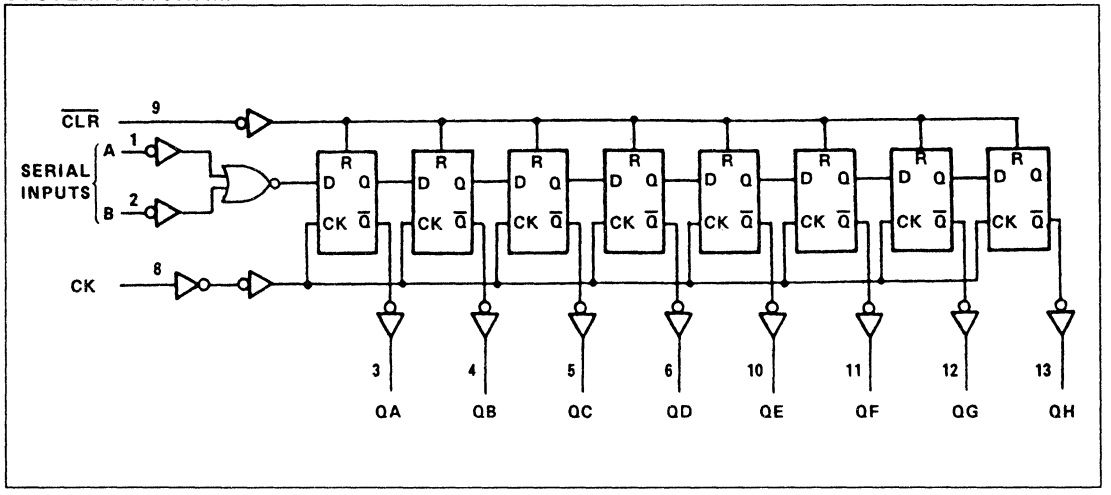
X: Don't Care

QAn~QGn: The level of QA~QG, respectively, before the most recent positive edge of the clock.

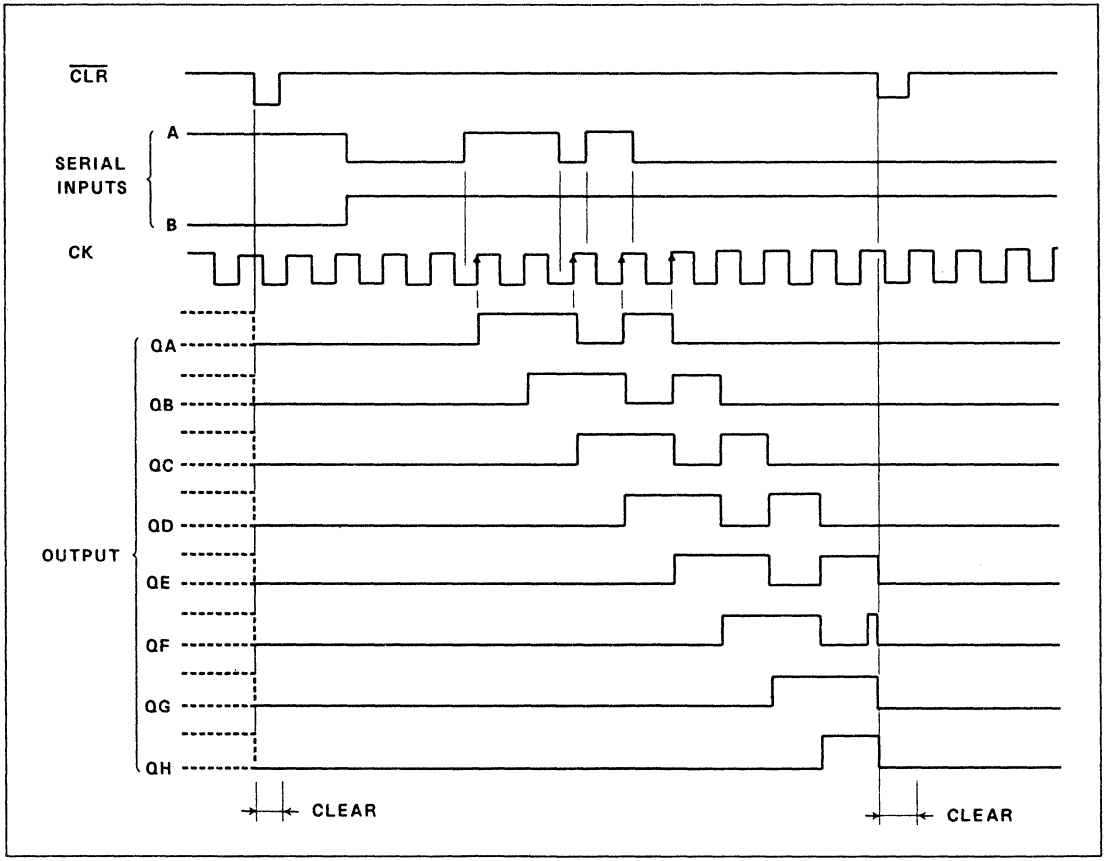
IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	80	100	
			4.5	−	16	20	
			6.0	−	14	17	
Minimum Set−up Time (A, B)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A, B)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Qn)	t_{pLH} t_{pHL}		−	15	27	
Propagation Delay Time ($\overline{CLEAR}$−Qn)	t_{pHL}		−	16	30	
Maximum Clock Frequency	f_{MAX}		33	58	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Qn)	t_{pLH} t_{pHL}		2.0	−	57	160	−	200	
			4.5	−	19	32	−	40	
			6.0	−	16	27	−	34	
Propagation Delay Time ($\overline{CLEAR}$−Qn)	t_{pHL}		2.0	−	60	175	−	220	
			4.5	−	20	35	−	44	
			6.0	−	17	30	−	37	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	62	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	107	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

8-BIT SHIFT REGISTER (P-IN,S-OUT)

The TC74HC165A is a high speed CMOS 8-BIT PARALLEL/ SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock inputs. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.

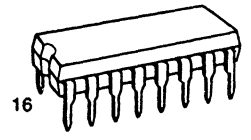
When the SHIFT/$\overline{\text{LOAD}}$ input is held low, the parallel data is loaded asynchronously into the register at positive going transition of the clock pulse.

The CLOCK-INHIBIT input should be shifted high only when the CLOCK input is held high.

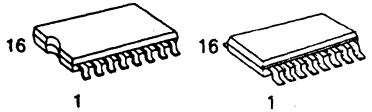
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=56MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS165

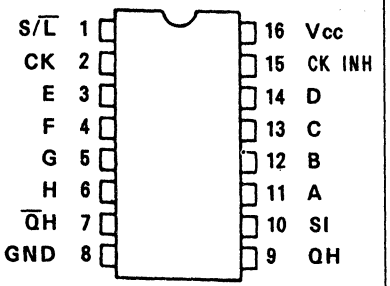


P(DIP16-P-300A)



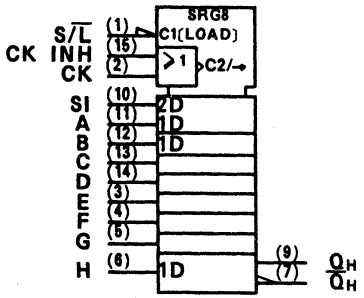
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

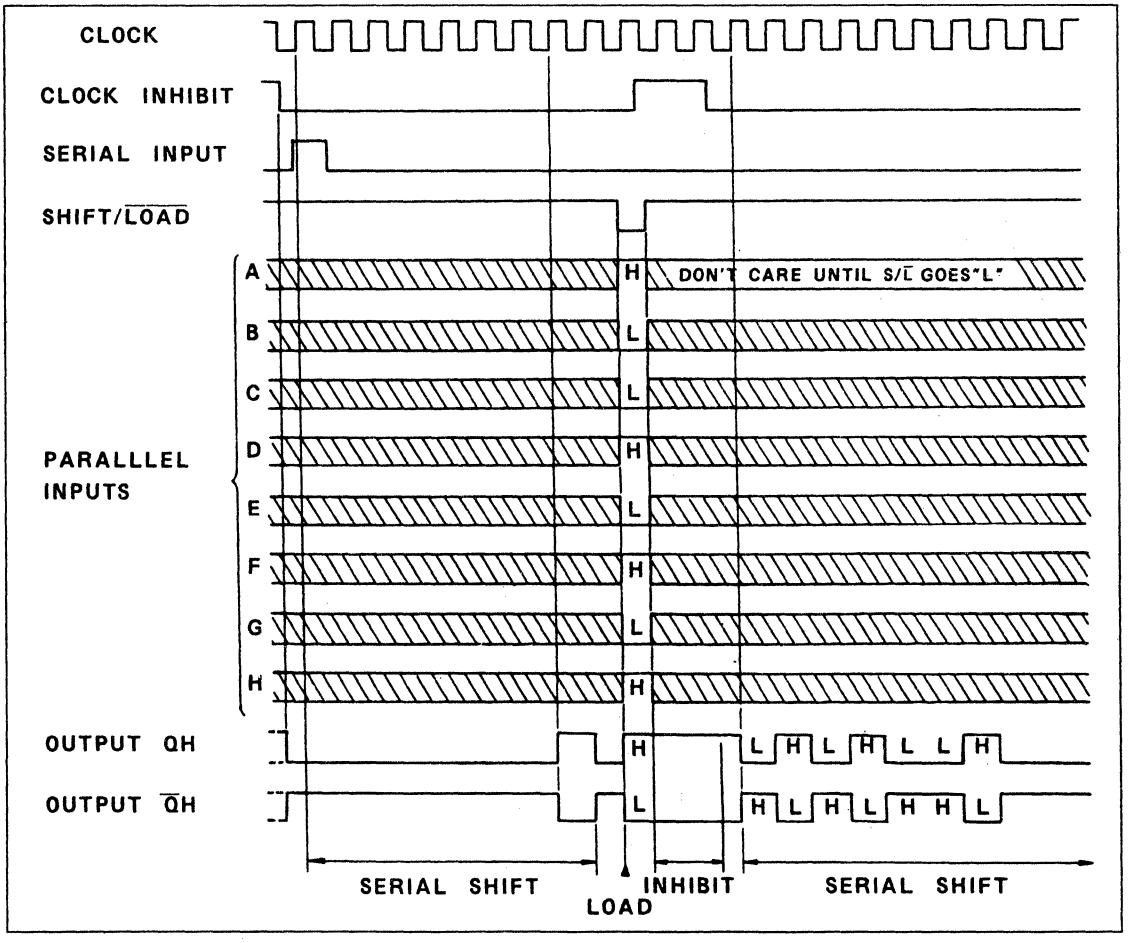


TRUTH TABLE

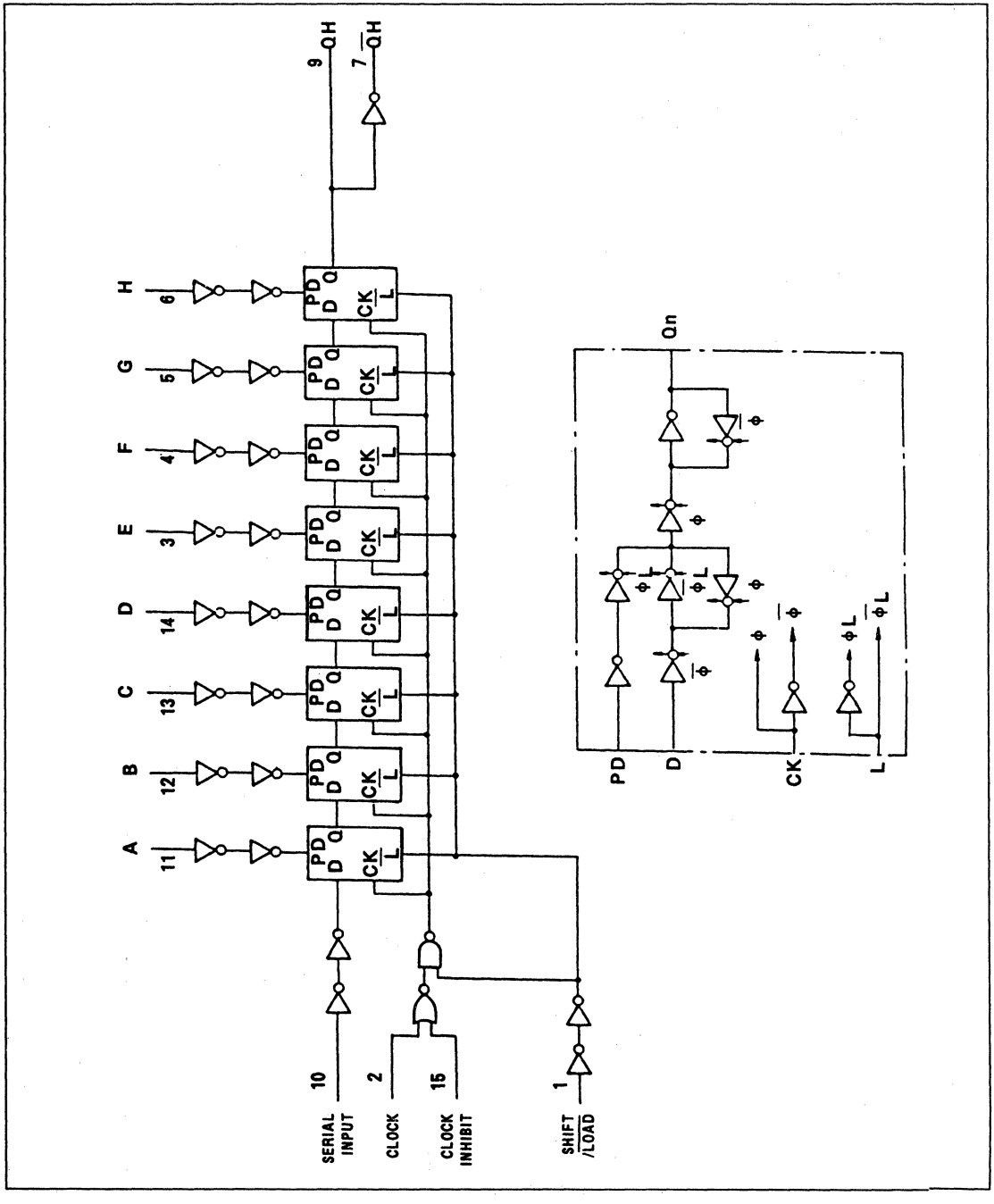
INPUTS					INTERNAL OUTPUTS		OUTPUTS	
SHIFT/$\overline{LOAD}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A……H	QA	QB	QH	$\overline{QH}$
L	X	X	X	a……h	a	b	h	$\overline{h}$
H	L	↑	H	X	H	QAn	QGn	$\overline{QGn}$
H	L	↑	L	X	L	QAn	QGn	$\overline{QGn}$
H	↑	L	H	X	H	QAn	QGn	$\overline{QGn}$
H	↑	L	L	X	L	QAn	QGn	$\overline{QGn}$
H	X	H	X	X	No change			
H	H	X	X	X	No change			

X:Don't Care
a……h :The level of steady input voltage at inputs A through H respectively.
QAn~QGn:The level of QA~QG,respectively,before the most recent positive transition of the CLOCK.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING RECOMMENDED OPERATING CONDITIONS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK, CK INH)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($S/\overline{L}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($PI-S/\overline{L}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI−CK,CK INH)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($S/\overline{L}$−CK,CK INH)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time ($PI-S/\overline{L}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (SI−CK,CK INH)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time ($S/\overline{L}$−CK,CK INH)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time (CK INH−CK) (CK−CK INH)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	30	24	
			6.0	−	41	28	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CK,CK INH−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time ($S/\overline{L}$−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time (H−QH,$\overline{QH}$)	t_{pLH} t_{pHL}		−	14	26	
Maximum Clock Frequency	f_{MAX}		35	56	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CK,CK INH−QH,$\overline{Q}$H)	t_{pLH} t_{pHL}		2.0	−	55	150	−	190	
			4.5	−	18	30	−	38	
			6.0	−	15	26	−	33	
Propagation Delay Time (S/$\overline{L}$−QH,$\overline{Q}$H)	t_{pLH} t_{pHL}		2.0	−	60	165	−	205	
			4.5	−	19	33	−	41	
			6.0	−	16	28	−	35	
Propagation Delay Time (H−QH,$\overline{Q}$H)	t_{pHL}		2.0	−	52	135	−	170	
			4.5	−	17	27	−	34	
			6.0	−	14	23	−	29	
Maximum Clock Frequency	f_{MAX}		2.0	7	14	−	6	−	MHz
			4.5	30	46	−	24	−	
			6.0	41	65	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	55	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC166AP/AF/AFN

8-BIT SHIFT REGISTER (P-IN,S-OUT)

The TC74HC166A is a high speed CMOS 8 BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

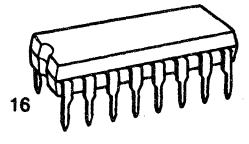
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of parallel-in or serial-in, serial-out 8-bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CLOCK-INHIBIT input should be shifted high only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing charts.

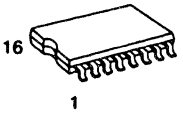
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

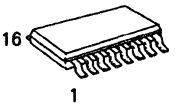
FEATURES:

- High Speed ····· f_{MAX}=57MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS166



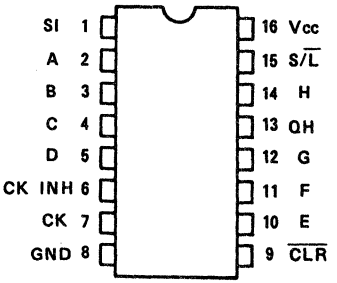
P(DIP16-P-300A)





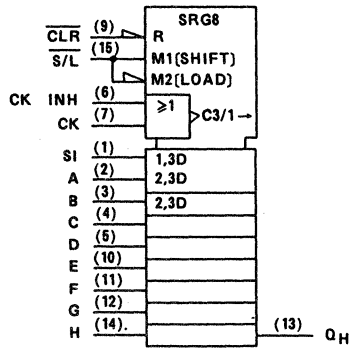
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



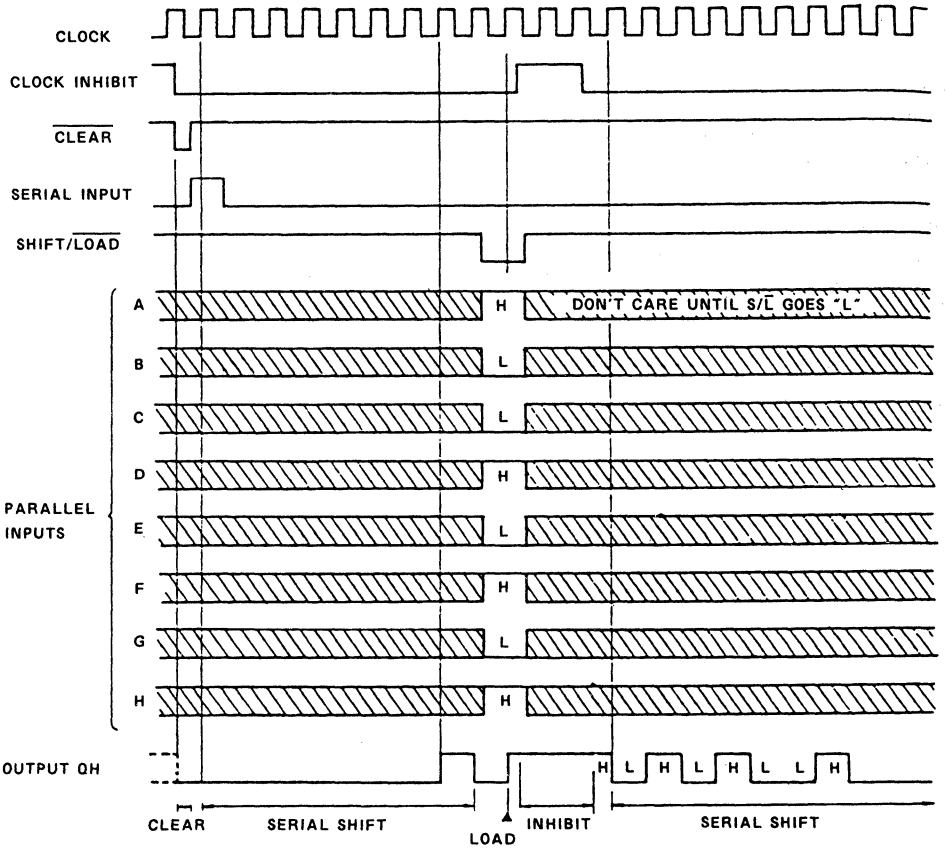
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
$\overline{\text{CLEAR}}$	SHIFT/$\overline{\text{LOAD}}$	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A·····H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	⊓	X	X	No change	
H	L	L	⊔	X	a ····· h	a b	h
H	H	L	⊔	H	X	H QAn	QGn
H	H	L	⊔	L	X	L QAn	QGn
H	X	H	X	X	X	No change	

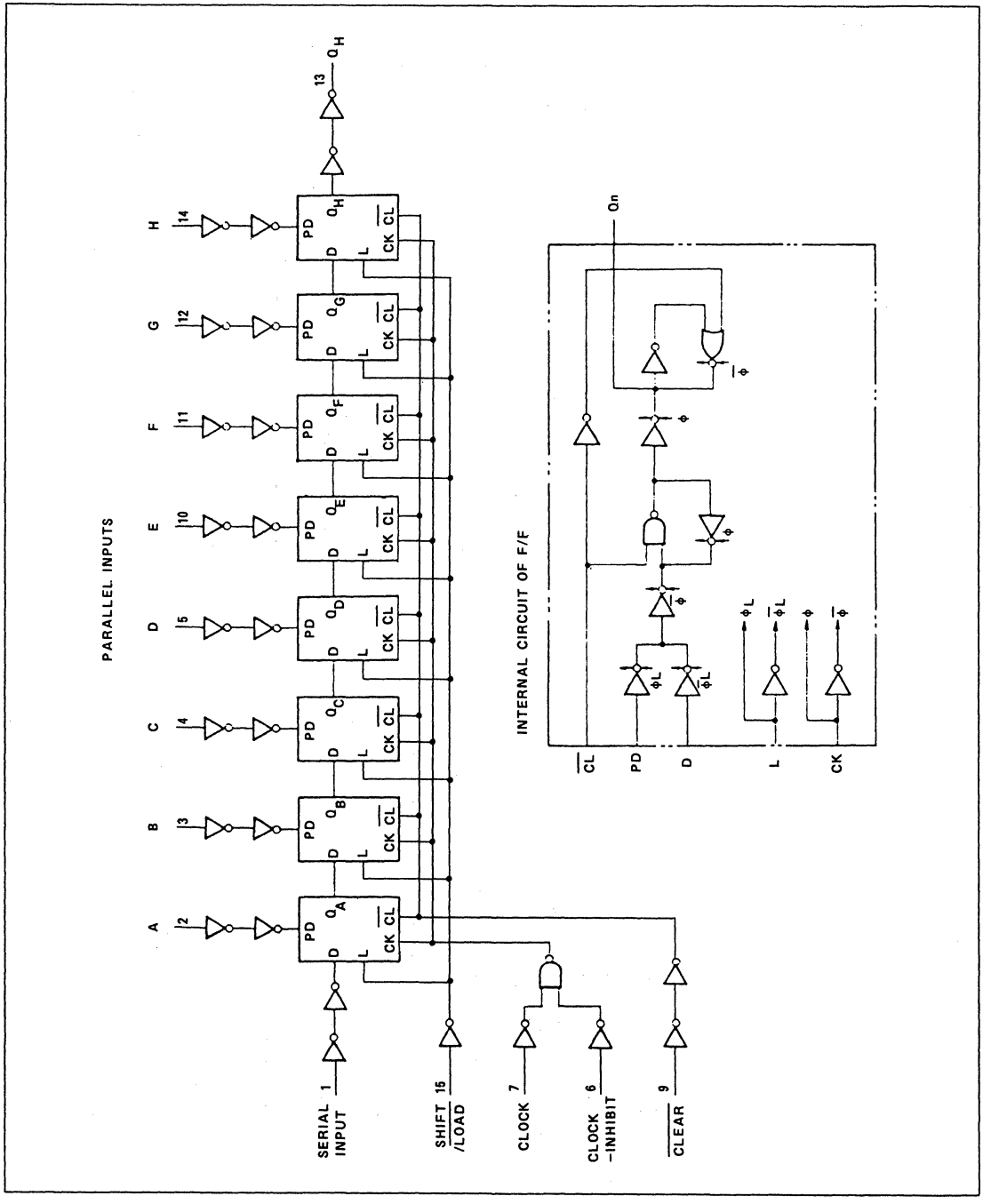
X : Don't care

a ····· h : The level of steady state input voltage at inputs A through H respectively

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI,PI)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($S/\overline{L}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (SI,PI)	th		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (S/L)	th		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−QH)	t_{pLH} t_{pHL}		−	16	26	
Propagation Delay Time ($\overline{CLEAR}$−QH)	t_{pHL}		−	15	24	
Maximum Clock Frequency	f_{MAX}		33	57	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−QH)	t_{pLH} t_{pHL}		2.0	−	70	150	−	190	
			4.5	−	20	30	−	38	
			6.0	−	16	26	−	32	
Propagation Delay Time ($\overline{CLEAR}$−QH)	t_{pHL}		2.0	−	60	135	−	170	
			4.5	−	18	27	−	34	
			6.0	−	14	23	−	29	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	−	5	−	MHz
			4.5	31	50	−	25	−	
			6.0	36	63	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	60	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

QUAD D-TYPE REGISTER(3-STATE)

The TC74HC173A is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate C ^{2}MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains a 4-bit register consisting of D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common clear input (CLEAR).

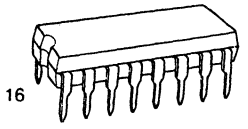
Signals applied to the data inputs (D1~D4) are stored in the respective flip-flops on the positive going transition of CLOCK when clock control inputs (G1, G2) are held low.

The clear function is asynchronous to CLOCK and active on a high level. The stored data are enabled to each outputs when output control inputs (M, N) are held low, else the outputs are high impedance state.

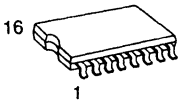
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=47MHz(Typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS173

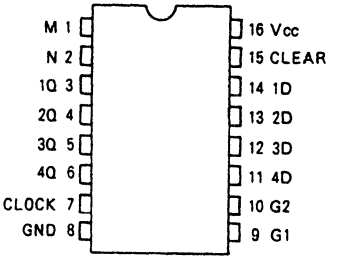


P(DIP16-P-300A)



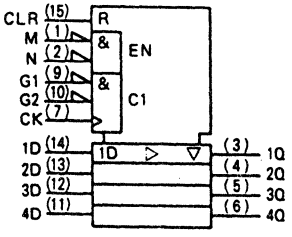
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



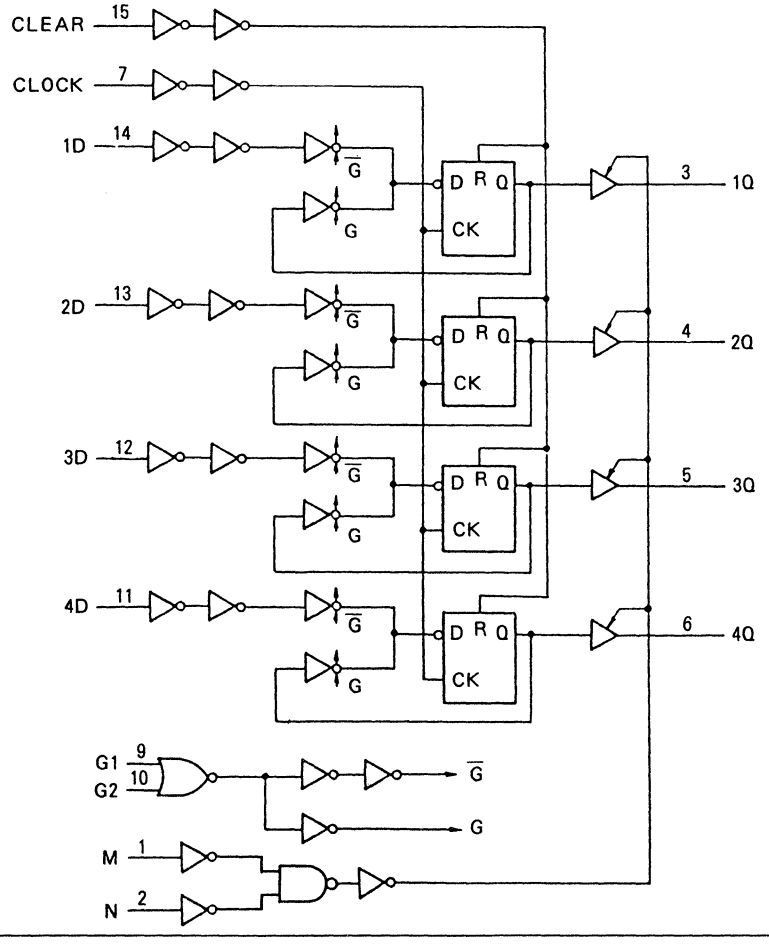
TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE G1	DATA ENABLE G2	Dn	OUTPUT CONTROL M	OUTPUT CONTROL N	Qn
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↑	X	X	X	L	L	Q0
L	↓	H	X	X	L	L	Q0
L	↓	X	H	X	L	L	Q0
L	↓	L	L	H	L	L	H
L	↓	L	L	L	L	L	L

X : Don't Care

Z : High Impedance

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (G1, G2)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (D)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (G1, G2, D)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	9	7	MHz
			4.5	−	43	34	
			6.0	−	51	40	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	12	20	−	25	
			150	2.0	−	65	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	16	26	−	33	
Propagation Delay Time (CLEAR−Q)	t_{pHL}		50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	12	20	−	25	
			150	2.0	−	63	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	16	26	−	33	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	12	20	−	25	
			150	2.0	−	63	115	−	195	
				4.5	−	20	31	−	39	
				6.0	−	16	26	−	33	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	36	135	−	170	
				4.5	−	17	27	−	34	
				6.0	−	15	23	−	29	
Maximum Clock Frequency	f_{MAX}		50	2.0	9	20	−	7	−	MHz
				4.5	43	67	−	34	−	
				6.0	51	84	−	40	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	45	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=28+17 \cdot n$$

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74HC174A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

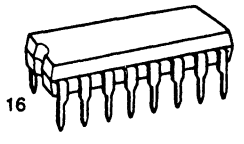
Information signals applied to the D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q outputs are in the low logic level independent of the other inputs.

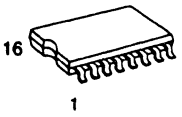
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

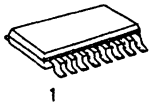
FEATURES:

- High Speed ..... f_{MAX}=71MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS174



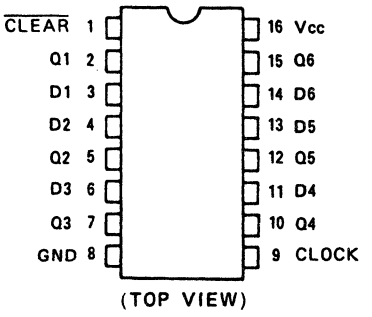
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



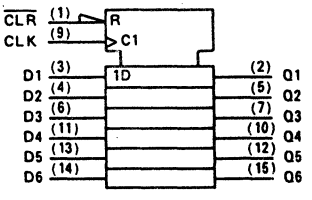
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L	⌐	L	-
H	H	⌐	H	-
H	X	⌐	Qn	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	4	5	
Clock Frequency	f		2.0	−	6	4	MHz
			4.5	−	33	26	
			6.0	−	38	30	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	14	26	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		−	15	26	
Maximum Clock Frequency	f_{MAX}		39	71	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	27	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	68	150	−	190	
			4.5	−	17	30	−	38	
			6.0	−	14	26	−	32	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		2.0	−	72	150	−	190	
			4.5	−	18	30	−	38	
			6.0	−	15	26	−	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	−	4	−	MHz
			4.5	33	59	−	26	−	
			6.0	38	71	−	30	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	40	−	−	−	

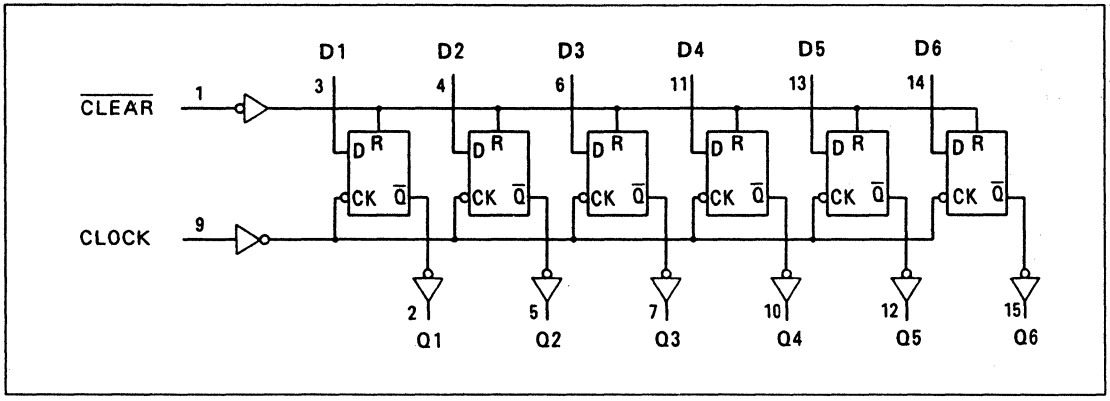
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total})=28+12 \cdot n$$

SYSTEM DIAGRAM



TC74HC175AP/AF/AFN

QUAD D-TYPE FLIP FLOP WITH CLEAR

The TC74HC175A is a high speed CMOS D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

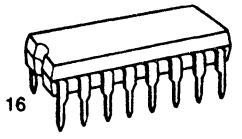
Information signals applied to D inputs are transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q outputs are at the low logic level and the $\overline{Q}$ outputs are at the high logic level independent of the other inputs.

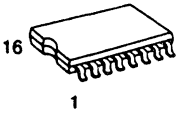
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

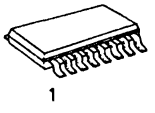
FEATURES:

- High Speed ····· f_{MAX}=63MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS175



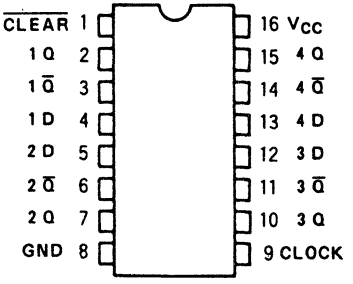
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



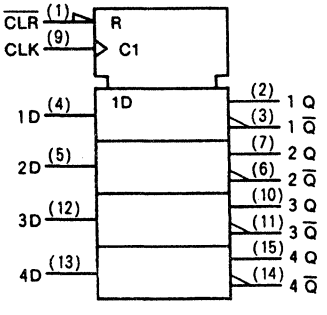
(TOP VIEW)

TRUTH TABLE

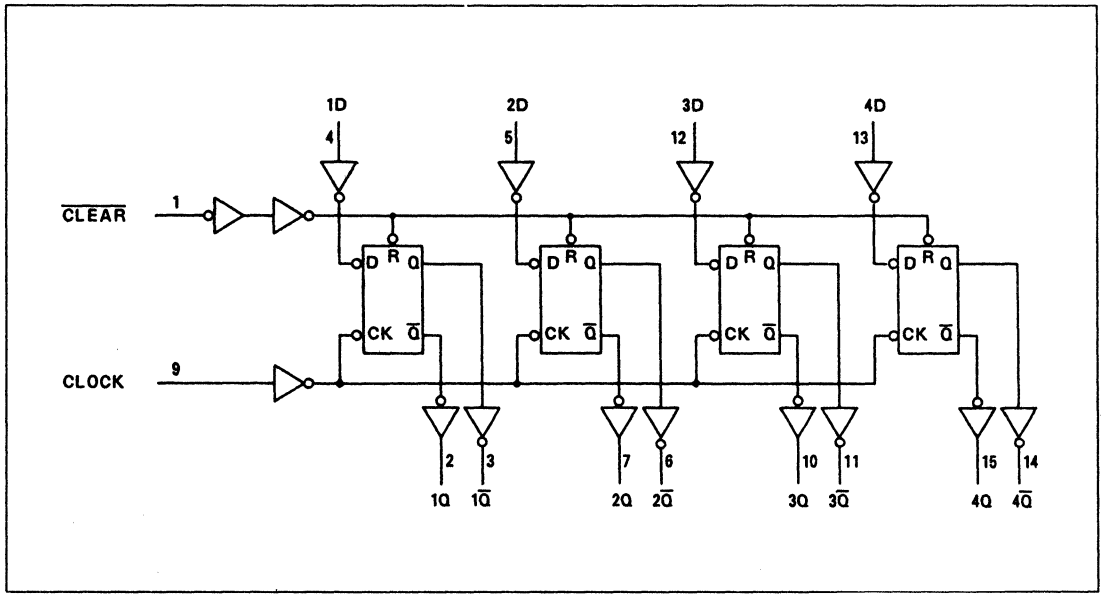
INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	Clear
H	L	↑	L	H	—
H	H	↑	H	L	—
H	X	↓	Q_n	$\overline{Q}_n$	No change

X : Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	t_{WL} t_{WH}		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	t_{WL}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	16	24	
Propagation Delay Time ($\overline{CLEAR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		−	13	21	
Maximum Clock Frequency	f_{MAX}		36	63	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	70	140	−	175	
			4.5	−	19	28	−	35	
			6.0	−	16	24	−	30	
Propagation Delay Time ($\overline{CLEAR}$−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	50	125	−	160	
			4.5	−	16	25	−	32	
			6.0	−	12	22	−	27	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	−	5	−	MHz
			4.5	31	53	−	25	−	
			6.0	36	63	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	53	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=32-21 \cdot n$$

TC74HC181P ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The TC74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT(ALU)/FUNCTION GENERATORS fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This circuit perform 16 binary arithmetic operations on two 4-bit word as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

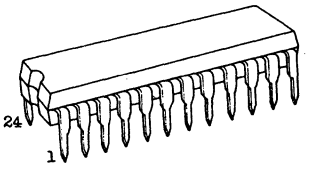
When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look ahead scheme is made available in these devices for fast, simultaneous carry generation be means of two cascade-outputs (pins 15 and 17) for the four bits in the package.

When used in conjunction with the TC74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS181



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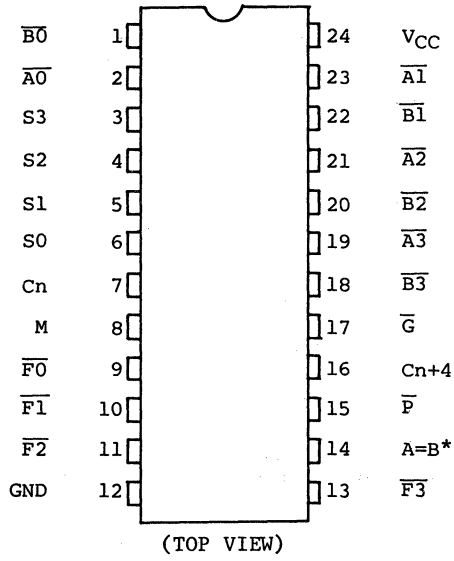
PIN ASSIGNMENT



(TOP VIEW)

*: Open drain Output Structure

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A=B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

FUNCTIONAL DESCRIPTION

The HC181 will accomodate active-high or active-low data, if the pin designations are interpreted as show below.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn+4	$\overline{P}$	$\overline{G}$
Active-high data(Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{Cn}$	$\overline{Cn+4}$	X	Y

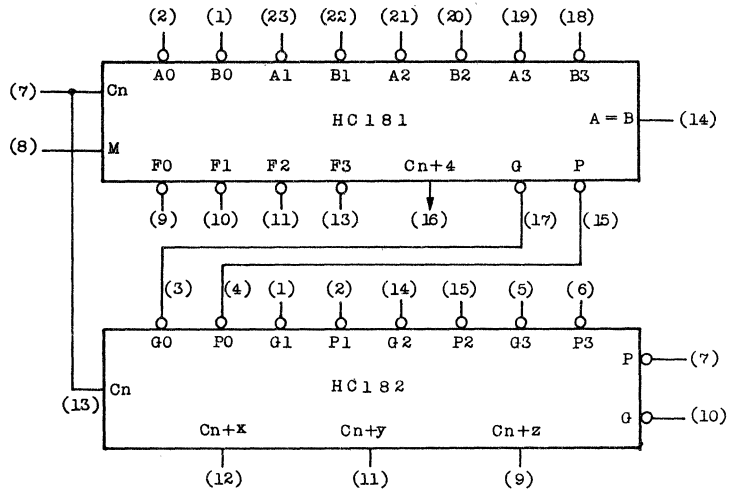
Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to produce A-B.

The HC181 also be utilized as a comparator. The A=B output is internally decoder from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B **inputs, it** will assume a high level to indicate equality (A=B). The ALU should be **in the subtract** mode with Cn=H when performing this comparison. The A=B output **is open-drain** so that it can be wire-AND connected to give a comparison for more **than four bits.** The carry output (Cn+4) can also be used to supply relative magnitude **information.** Again, the ALU should be placed in the subtract mode by placing the **function select** input S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output Cn+4	Active-low data (Figure 1)	Active-high data (Figure 2)
H	H	A≥B	A≤B
H	L	A<B	A>B
L	H	A>B	A<B
L	L	A≤B	A≥B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

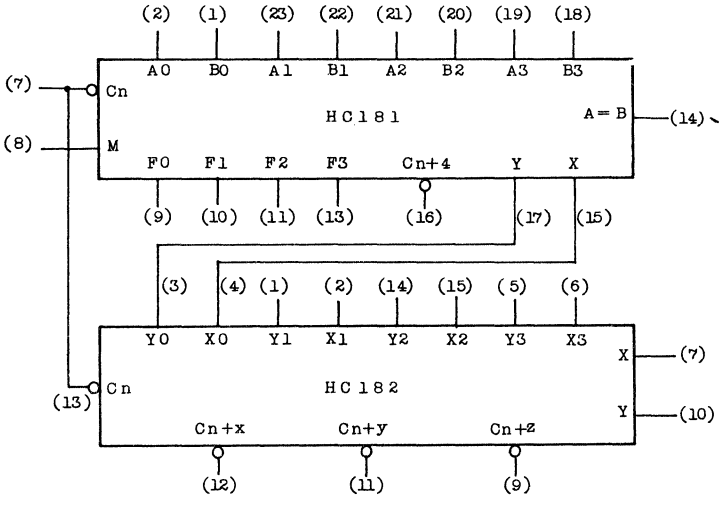


(Figure 1)

Table 1

Selection				Active Low Data		
				M=H	M=L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	$F = \bar{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \bar{A} + B$	$F = A\bar{B}$ Minus 1	$F = (A\bar{B})$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus $(A + \bar{B})$	F = A Plus$(A + \bar{B})$ Plus 1
L	H	L	H	$F = \bar{B}$	F = AB Puls (A + B)	F = AB Plus$(A + \bar{B})$ Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \bar{B}$	$F = A + \bar{B}$	$F = (A + \bar{B})$ Plus 1
H	L	L	L	$F = \bar{A}B$	F = A Plus (A + B)	F = A Plus(A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	$F = A\bar{B}$ Plus (A + B)	$F = A\bar{B}$ Plus(A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\bar{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	$F = A\bar{B}$ Plus A	$F = A\bar{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.



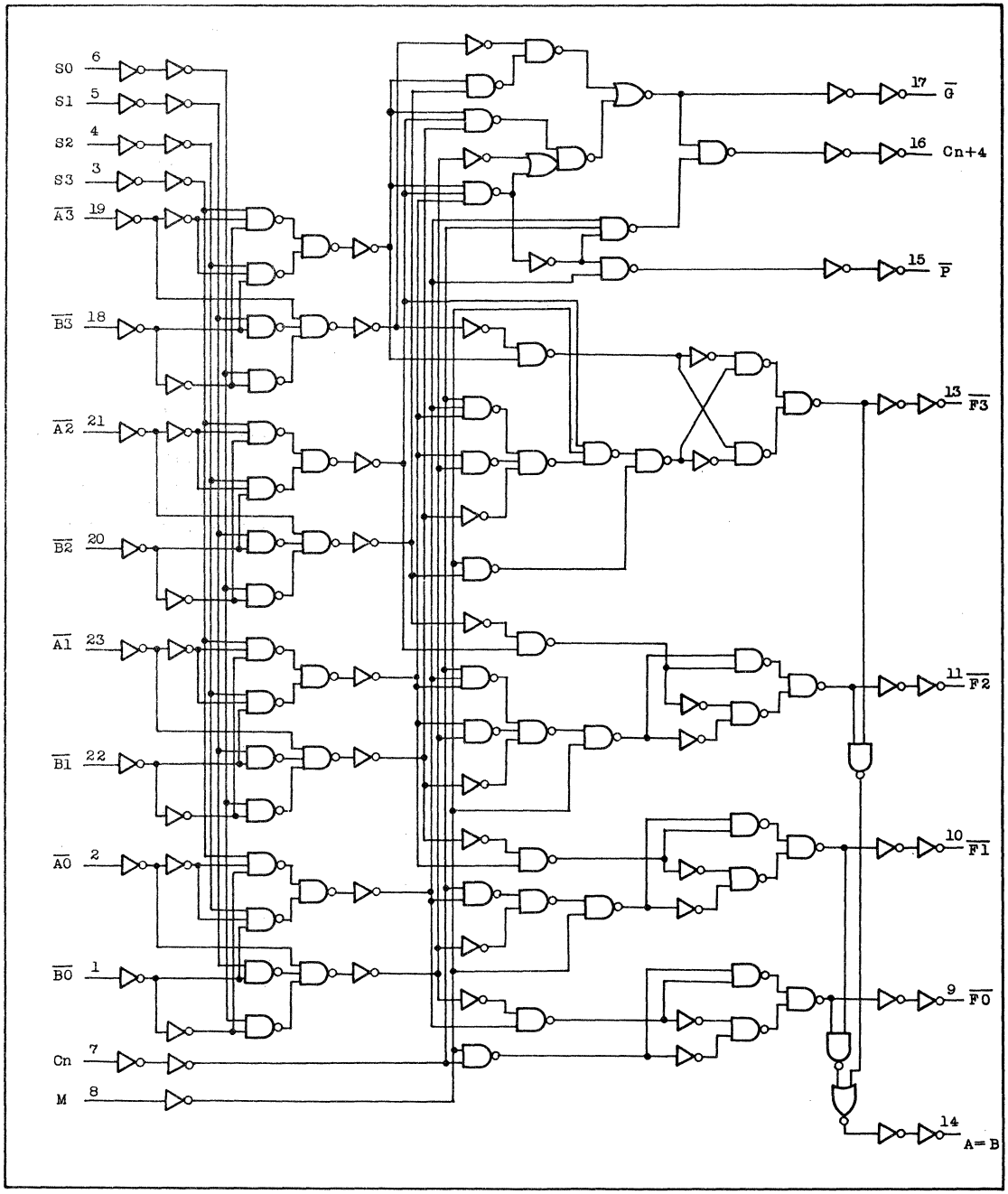
(Figure 2)

Table 2

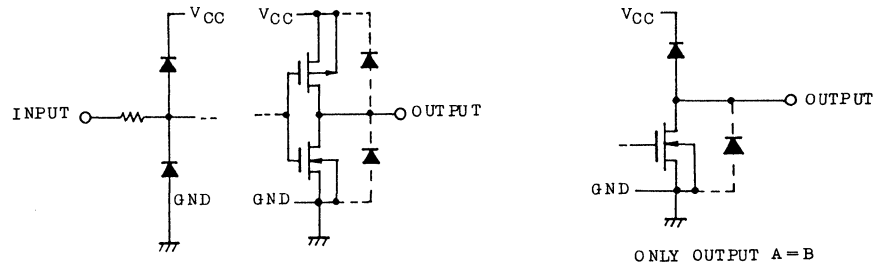
Selection S3	S2	S1	S0	Active High Data: M=H Logic Functions	M=L: Arithmetic Operations: C_n=H (no carry)	M=L: Arithmetic Operations: C_n=L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A+B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1(2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	$F = A \oplus B$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	$F = \overline{A}+B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Any output except A=B	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.00	0.1	-	0.1	V
				4.5	-	0.00	0.1	-	0.1	
				6.0	-	0.00	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	$V_{IN}=V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (1)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time (2)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (3)	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (4)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
Propagation Delay Time (5)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (6)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Propagation Delay Time (7)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (8)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (9)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (10)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (11)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
3-State Output Enable Time (12)	t_{pZL}	R_L=1kΩ	2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
3-State Output Disable Time (12)	t_{pLZ}	R_L=1kΩ	2.0	-	140	260	-	325	
			4.5	-	35	52	-	65	
			6.0	-	30	44	-	55	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	216	-	-	-	

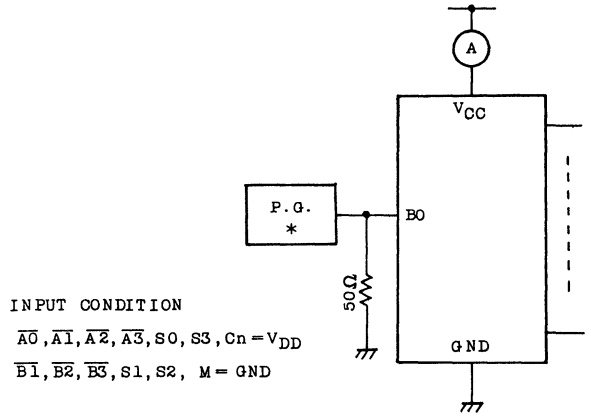
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

PROPAGATION DELAY TIME TEST CONDITIONS

TEST NO.	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M=GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=VCC, S1=S2=GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A=B	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)

$I_{CC(opr.)}$ TEST CIRCUIT



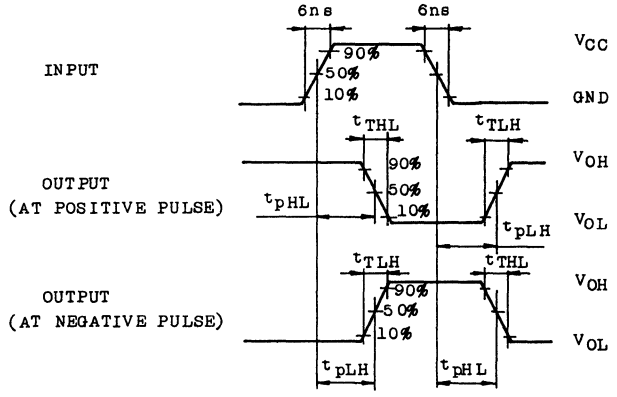
INPUT CONDITION

$\overline{A0}, \overline{A1}, \overline{A2}, \overline{A3}, S0, S3, Cn = V_{DD}$

$\overline{B1}, \overline{B2}, \overline{B3}, S1, S2, M = GND$

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC182AP/AF

LOOK AHEAD CARRY LOGIC

The TC74HC182A is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These circuits are capable of anticipating a carry across four binary adders or group of adders.They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

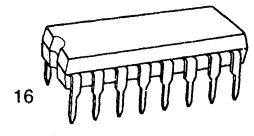
When used in conjunction with the HC181A arithmetic logic unit, these generators provide high-speed carry look -ahead capability for any word length. Each HC182A generates the look-ahead (anticipated carry)across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate(P) and carry generate(G) are in negated form; therefore, the carry functions(inputs, output, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181A data sheet are also applicable to and compatible with the look-ahead generator.

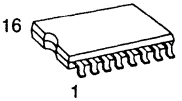
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=14ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS182

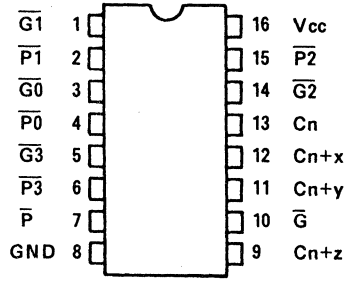


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

Pin Designation

Active"L"	Active"H"	Pin No.	Function
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	G0, G1, G2, G3	3 , 1 , 14 , 5	Carry Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	P0, P1, P2, P3	4 , 2 , 15 , 6	Carry Propagate Inputs
Cn	$\overline{Cn}$	13	Carry Input
Cn+z, Cn+y Cn+z	$\overline{Cn+x}$, $\overline{Cn+y}$ $\overline{Cn+z}$	12 , 11 , 9	Carry Outputs
$\overline{G}$	Y	10	Carry Generate Output
$\overline{P}$	X	7	Carry Propagate Output
Vcc		16	Supply Voltage
GND		8	Ground

TRUTH TABLE

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
All other combinations			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

X:Don't care

$Cn+x=G0+P0Cn$

$Cn+y=G1+P1G0+P1P0Cn$

$Cn+z=G2+P2G1+P2P1G0+P2P1P0Cn$

$\overline{G}=\overline{G3+P3G2+P3P2G1+P3P2P1G0}$

$\overline{P}=\overline{P3P2P1P0}$

or

$\overline{Cn+x}=\overline{Y0(X0+Cn)}$

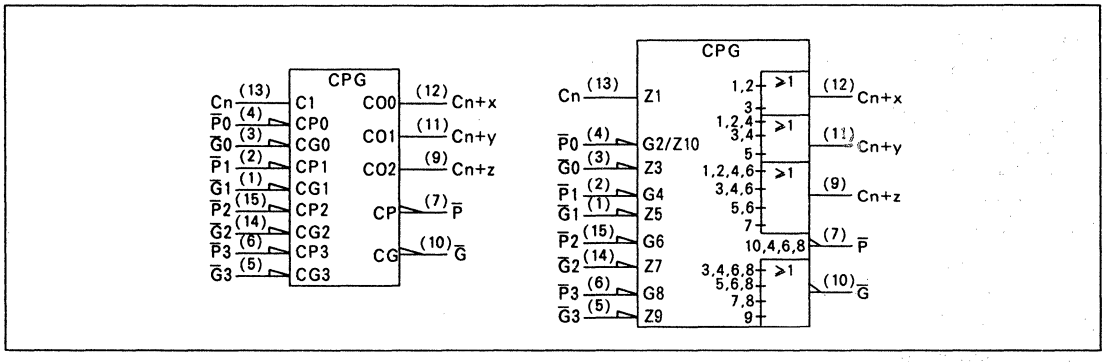
$\overline{Cn+y}=\overline{Y1[X1+Y0(X0+Cn)]}$

$\overline{Cn+z}=\overline{Y2\{X2+Y1[X1+Y0(X0+Cn)]\}}$

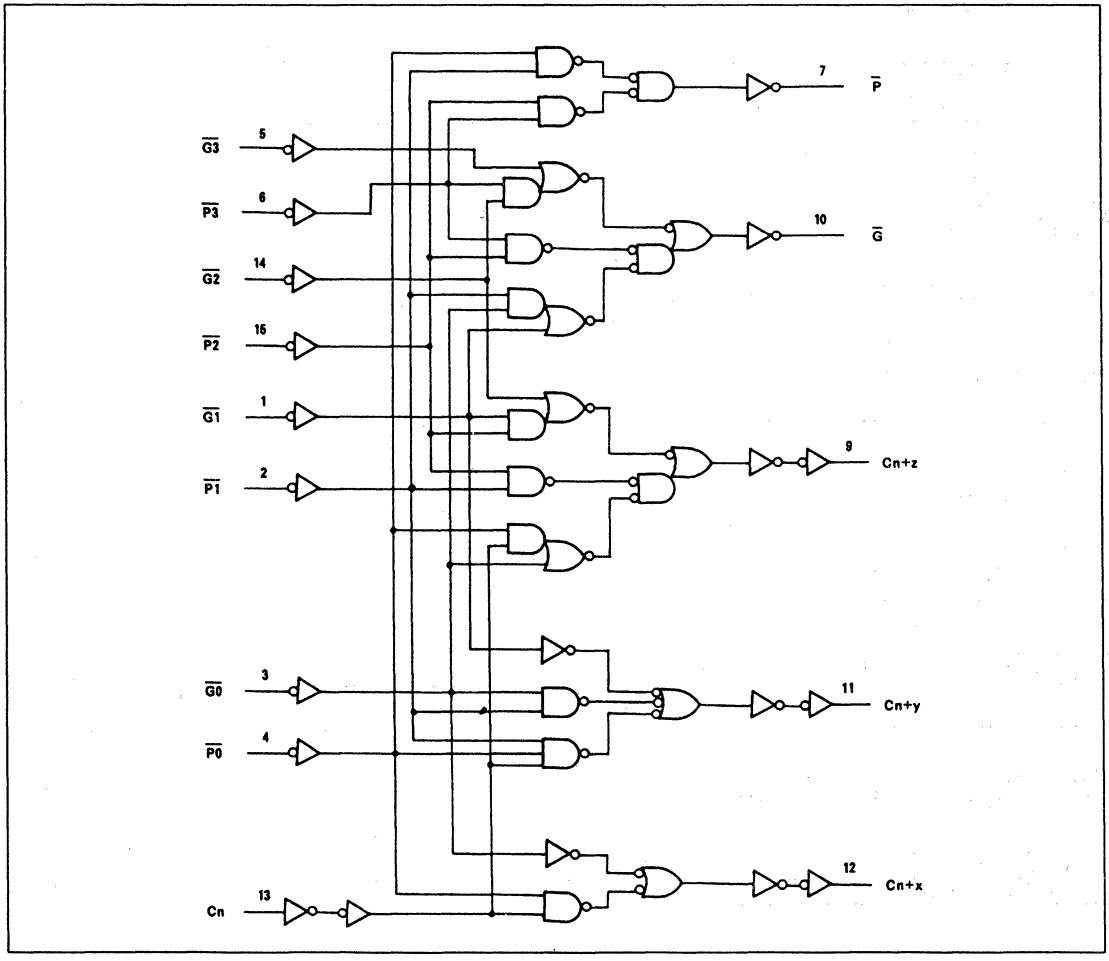
$Y=Y3(X3+Y2)(X3+X2+Y1)(X3+X2+X1+Y0)$

$X=X3+X2+X1+X0$

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}$ / $\overline{P0}, \overline{P1}, \overline{P2}$ – Cn+x, Cn+y / Cn+z)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}, G3$ / $\overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{G}$)	t_{pLH} t_{pHL}		–	16	27	
Propagation Delay Time ($\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$–$\overline{P}$)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time (Cn–Cn+x, Cn+y, Cn+z)	t_{pLH} t_{pHL}		–	14	24	

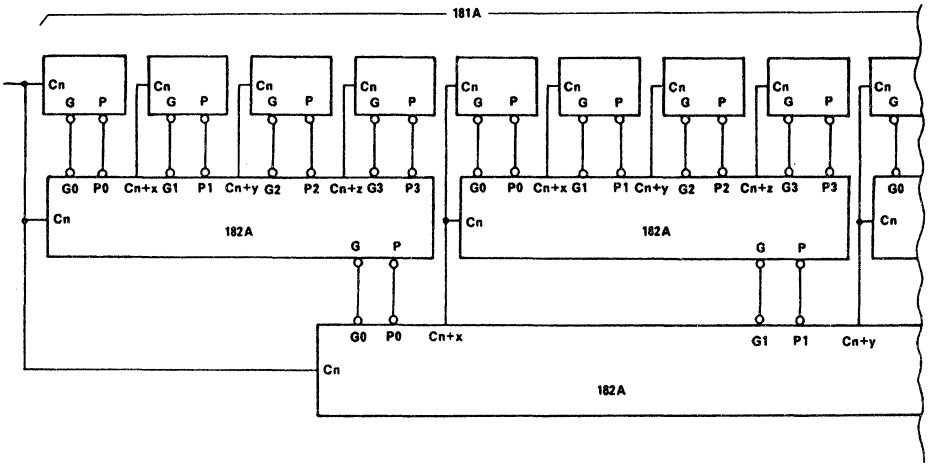
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}$ / $\overline{P0}, \overline{P1}, \overline{P2}$ – Cn+x, Cn+y / Cn+z)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$ / $\overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{G}$)	t_{pLH} t_{pHL}		2.0	–	72	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	14	26	–	33	
Propagation Delay Time ($\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$–$\overline{P}$)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Propagation Delay Time (Cn–Cn+x, Cn+y, Cn+z)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	61	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

TC74HC190AP/AF
TC74HC191AP/AF

TC74HC190AP/AF BCD UP/DOWN COUNTER
TC74HC191AP/AF 4-BIT BINARY UP/DOWN COUNTER

The TC74HC190A and TC74HC191A are high speed CMOS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC190A is BCD up/down counter and the TC74HC191A is 4-bit binary up/down counter.

They have an asynchronous load input (LOAD) which is active low.

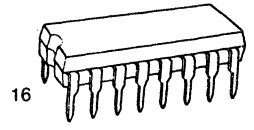
The direction of counting is determined by the level of DOWN/$\overline{UP}$. When D/$\overline{U}$ is low, the counter counts up; when D/$\overline{U}$ is high, it counts down. Counting occurs on the positive going transition of the clock input.

Enable input (ENABLE) and two carry inputs (RIPPLE CLOCK OUT, MAX/MIN) are provided to permit easy cascading of the counters, which facilitates easy implementation of N-bit counters without using external gates.

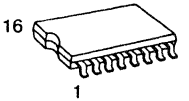
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=48MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS190/191

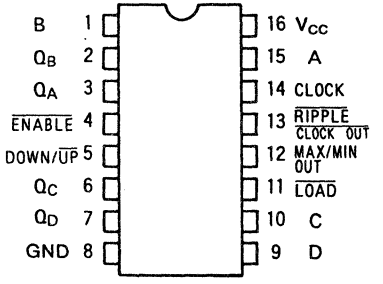


P(DIP16-P-300A)



F(SOP16-P-300)

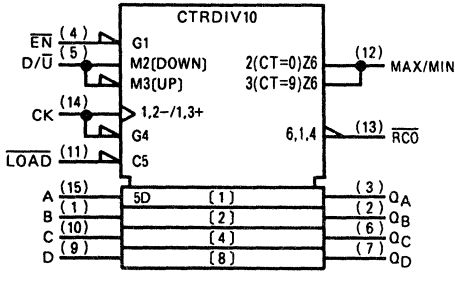
PIN ASSIGNMENT



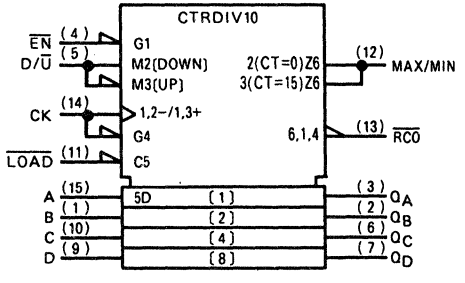
(TOP VIEW)

IEC LOGIC SYMBOL

TC74HC190A



TC74HC191A



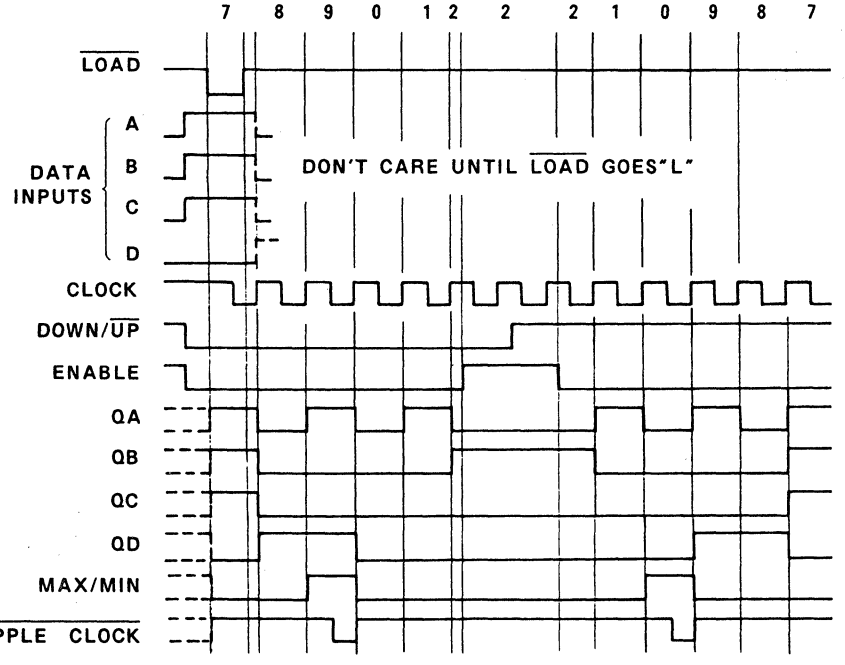
TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	PRESET DATA
H	L	L	↑	UP COUNT				UP COUNT
H	L	H	↑	DOWN COUNT				DOWN COUNT
H	H	X	↑	NO CHANGE				NO COUNT
H	X	X	↓	NO CHANGE				NO COUNT

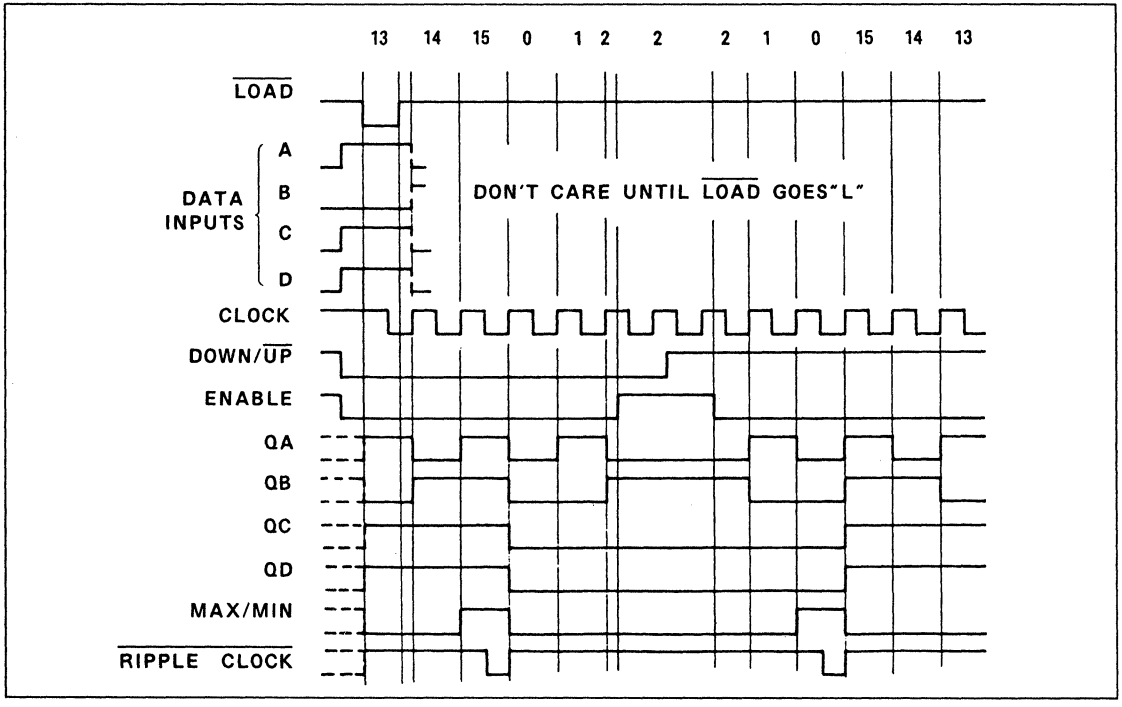
NOTE X:DON'T CARE

a~d:Inputs Level of A~D

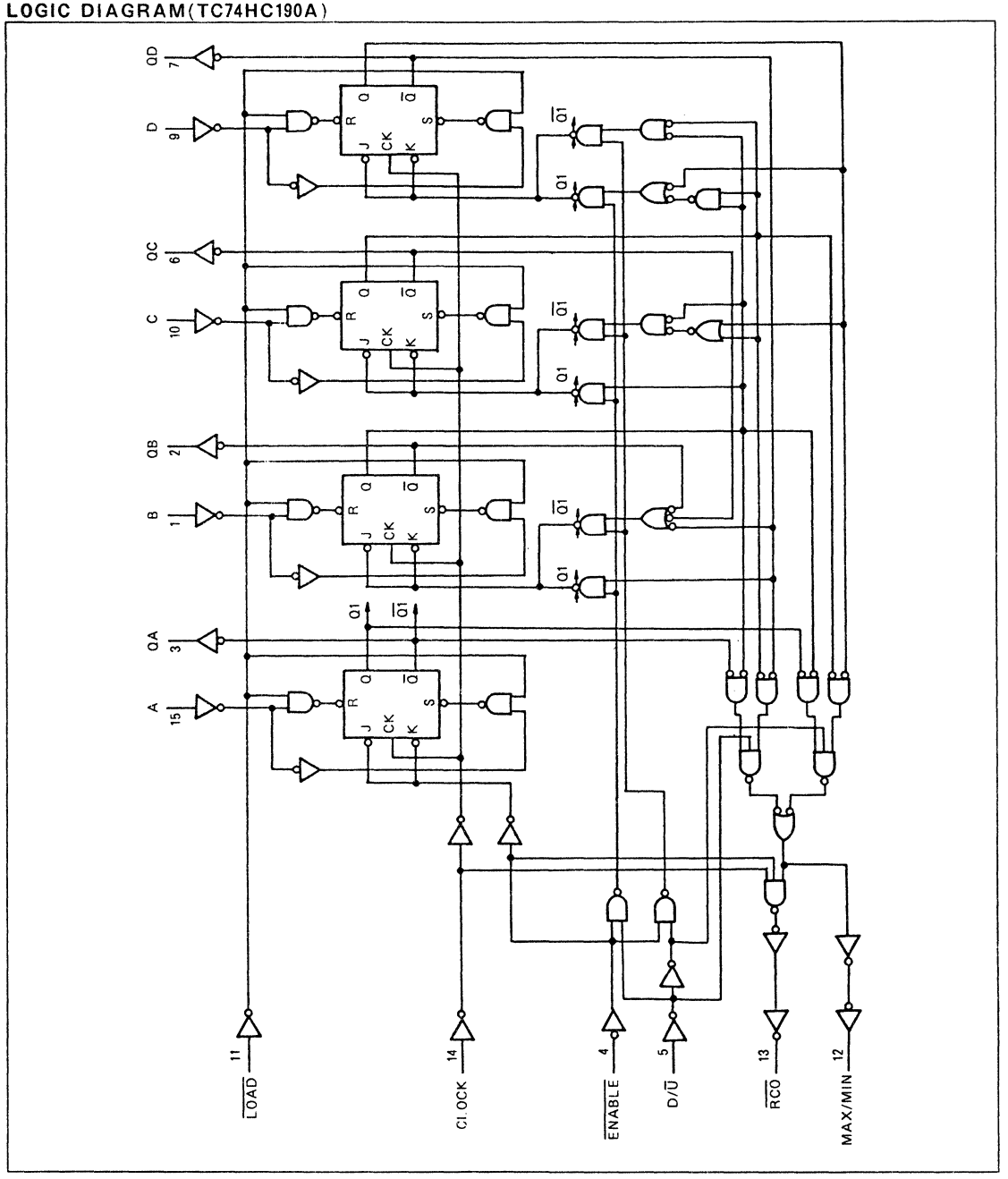
TIMING CHART(TC74HC190A)



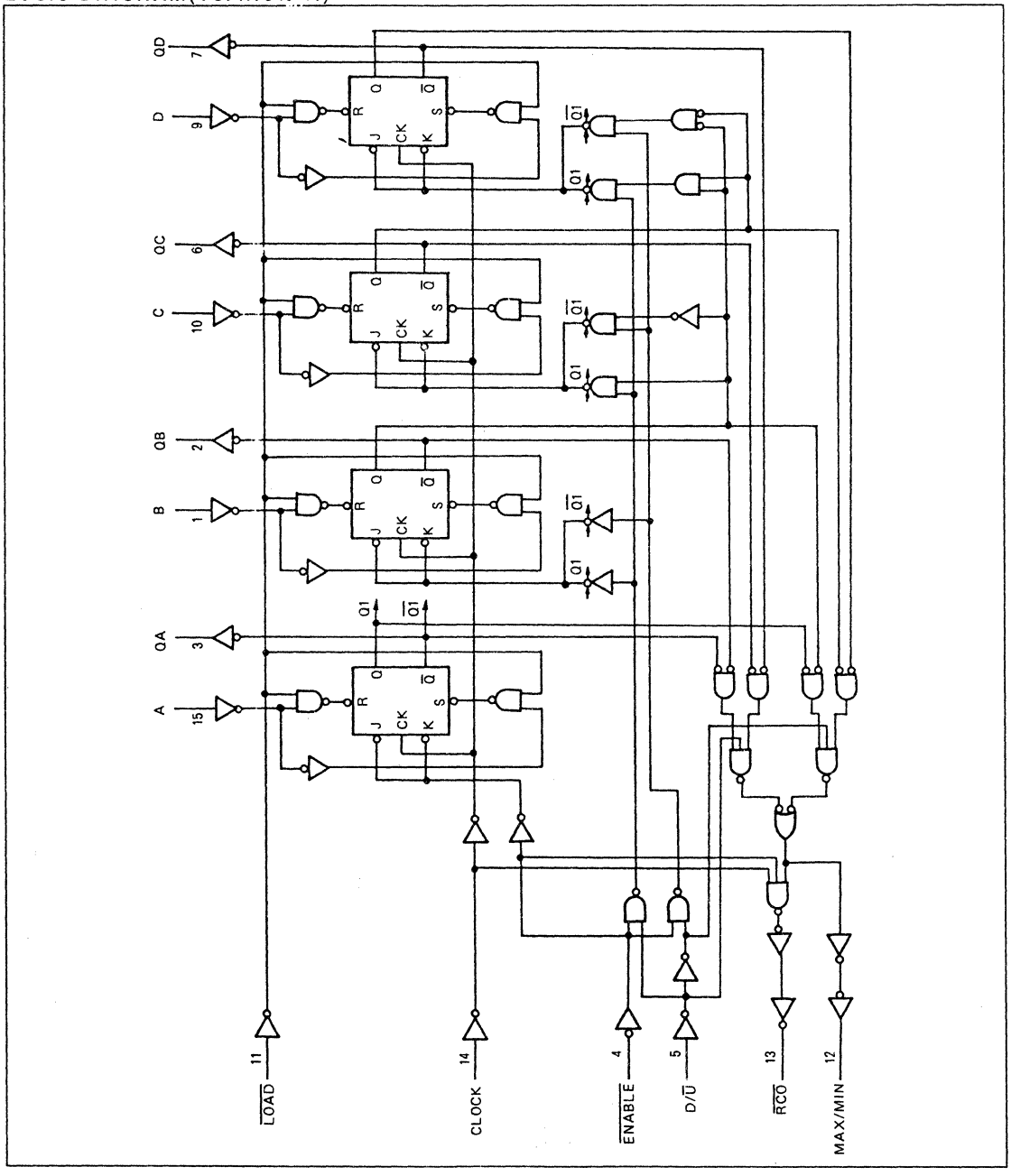
TIMING CHART(TC74HC191A)



LOGIC DIAGRAM(TC74HC190A)



LOGIC DIAGRAM(TC74HC191A)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	100	125	ns
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{ENABLE}$,D/$\overline{U}$)	t_s		2.0	−	150	190	
			4.5	−	30	38	
			6.0	−	26	33	
Minimum Set−up Time (DATA−$\overline{LOAD}$)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time ($\overline{ENABLE}$,D/$\overline{U}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (DATA−$\overline{LOAD}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	5	4	MHz
			4.5	−	25	20	
			6.0	−	29	24	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF$, $V_{CC}=5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	18	31	
Propagation Delay Time (CLOCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	10	20	
Propagation Delay Time (CLOCK−MAX/MIN)	t_{pLH} t_{pHL}		−	23	42	
Propagation Delay Time ($\overline{LOAD}$−Q)	t_{pLH} t_{pHL}		−	21	35	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		−	17	30	
Propagation Delay Time ($\overline{ENABLE}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	11	17	
Propagation Delay Time (D/$\overline{U}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		−	17	31	
Propagation Delay Time (D/$\overline{U}$−MAX/MIN)	t_{pLH} t_{pHL}		−	15	27	
Maximum Clock Frequency	f_{MAX}		27	48	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	88	180	−	225	
			4.5	−	22	36	−	45	
			6.0	−	19	31	−	38	
Propagation Delay Time (CLOCK−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	−	52	120	−	150	
			4.5	−	13	24	−	30	
			6.0	−	11	20	−	26	
Propagation Delay Time (CLOCK−MAX/MIN)	t_{pLH} t_{pHL}		2.0	−	108	240	−	300	
			4.5	−	27	48	−	60	
			6.0	−	23	41	−	51	
Propagation Delay Time ($\overline{LOAD}$−Q)	t_{pLH} t_{pHL}		2.0	−	100	205	−	255	
			4.5	−	25	41	−	51	
			6.0	−	22	35	−	43	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		2.0	−	84	175	−	220	
			4.5	−	21	35	−	44	
			6.0	−	18	30	−	37	
Propagation Delay Time ($\overline{ENABLE}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	−	56	105	−	130	
			4.5	−	14	21	−	26	
			6.0	−	12	18	−	22	
Propagation Delay Time (D/$\overline{U}$−$\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	−	84	180	−	225	
			4.5	−	21	36	−	45	
			6.0	−	18	31	−	38	
Propagation Delay Time (D/$\overline{U}$−MAX/MIN)	t_{pLH} t_{pHL}		2.0	−	72	160	−	200	
			4.5	−	18	32	−	40	
			6.0	−	15	27	−	34	
Maximum Clock Frequency	t_{pLH} t_{pHL}		2.0	5	11	−	4	−	MHz
			4.5	25	44	−	20	−	
			6.0	29	52	−	24	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74HC190A		−	104	−	−	−	
		TC74HC191A			101				

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC192AP/AF
TC74HC193AP/AF/AFN

TC74HC192AP/AF SYNCHRONOUS UP/DOWN DECADE COUNTER
TC74HC193AP/AF/AFN SYNCHRONOUS UP/DOWN BINARY COUNTER

The TC74HC192A/TC74HC193A are high speed CMOS SYNCHRONOUS 4-BIT UP/DOWN COUNTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

They have a clear input (CLEAR), a load input ($\overline{LOAD}$), load data inputs (A~D), two clock inputs (COUNT UP, COUNT DOWN), four count data outputs (Q_A~Q_D), and other outputs ($\overline{CARRY}$, $\overline{BORROW}$).

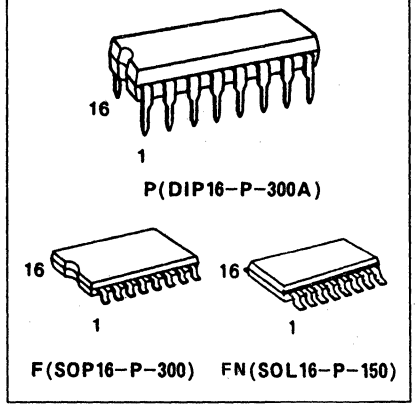
CLEAR is active high and forces Q_A thru Q_D outputs low independent of the other inputs.

$\overline{CARRY}$ and $\overline{BORROW}$ outputs are provided in order to make a cascade connection without external circuitry.

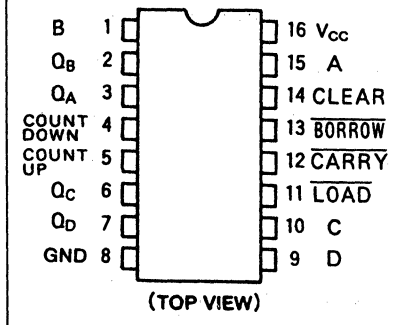
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

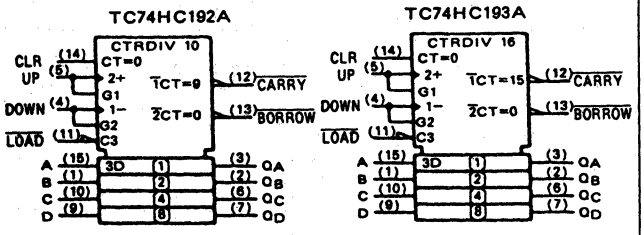
- High Speed ····· f_{MAX}=54MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS192/193



PIN ASSIGNMENT



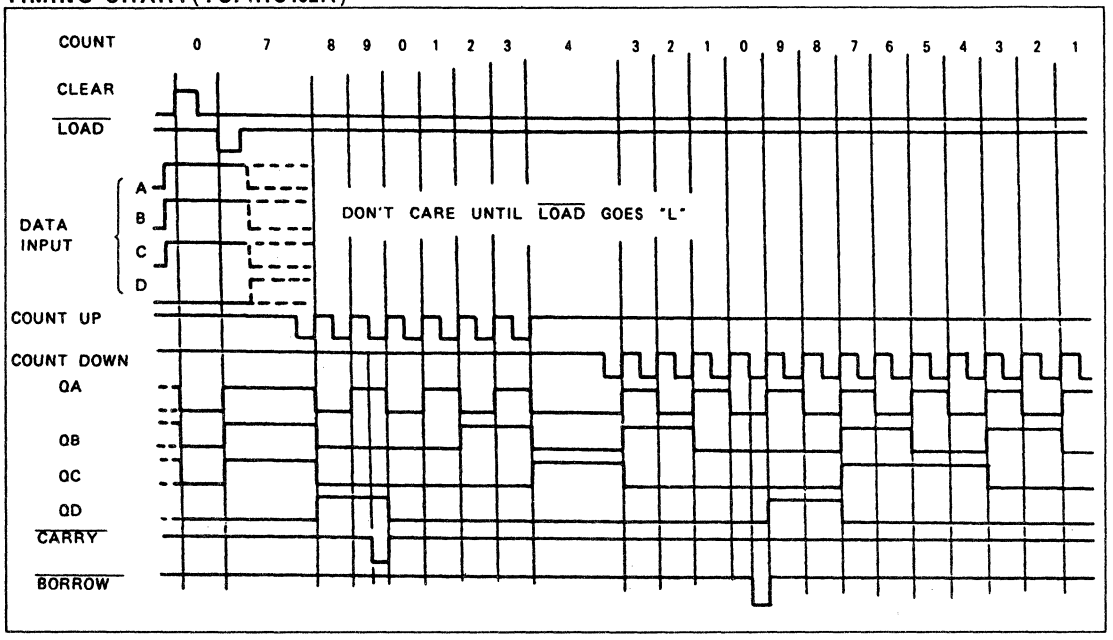
IEC LOGIC SYMBOL



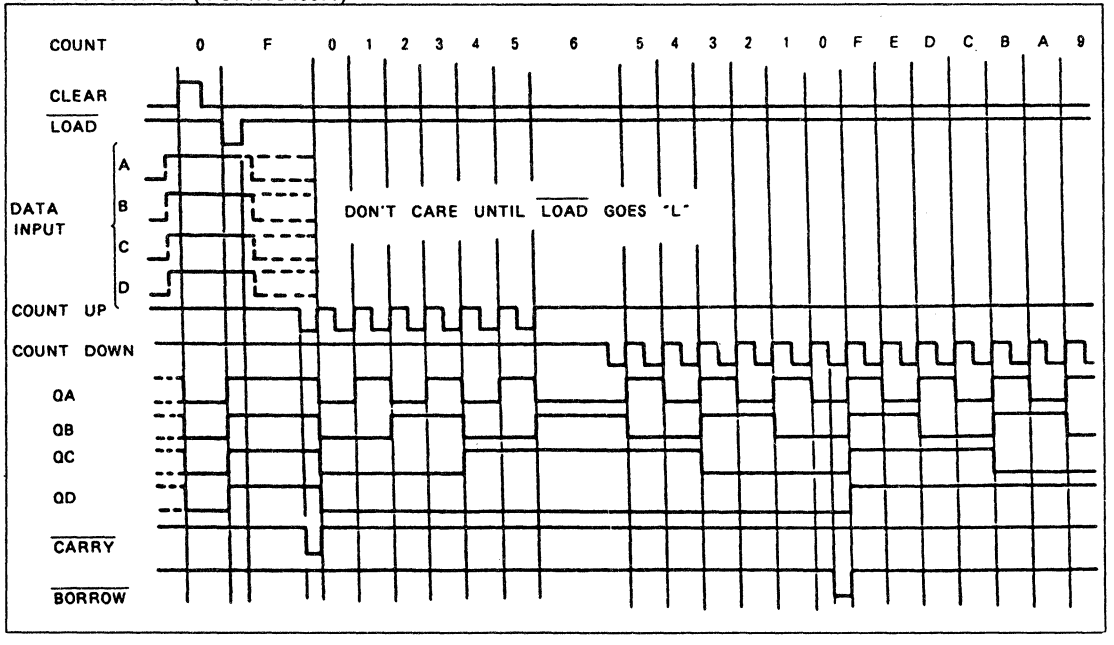
TRUTH TABLE

INPUTS				FUNCTION
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	
↑	H	H	L	COUNT UP
↓	H	H	L	NO COUNT
H	↑	H	L	COUNT DOWN
H	↓	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

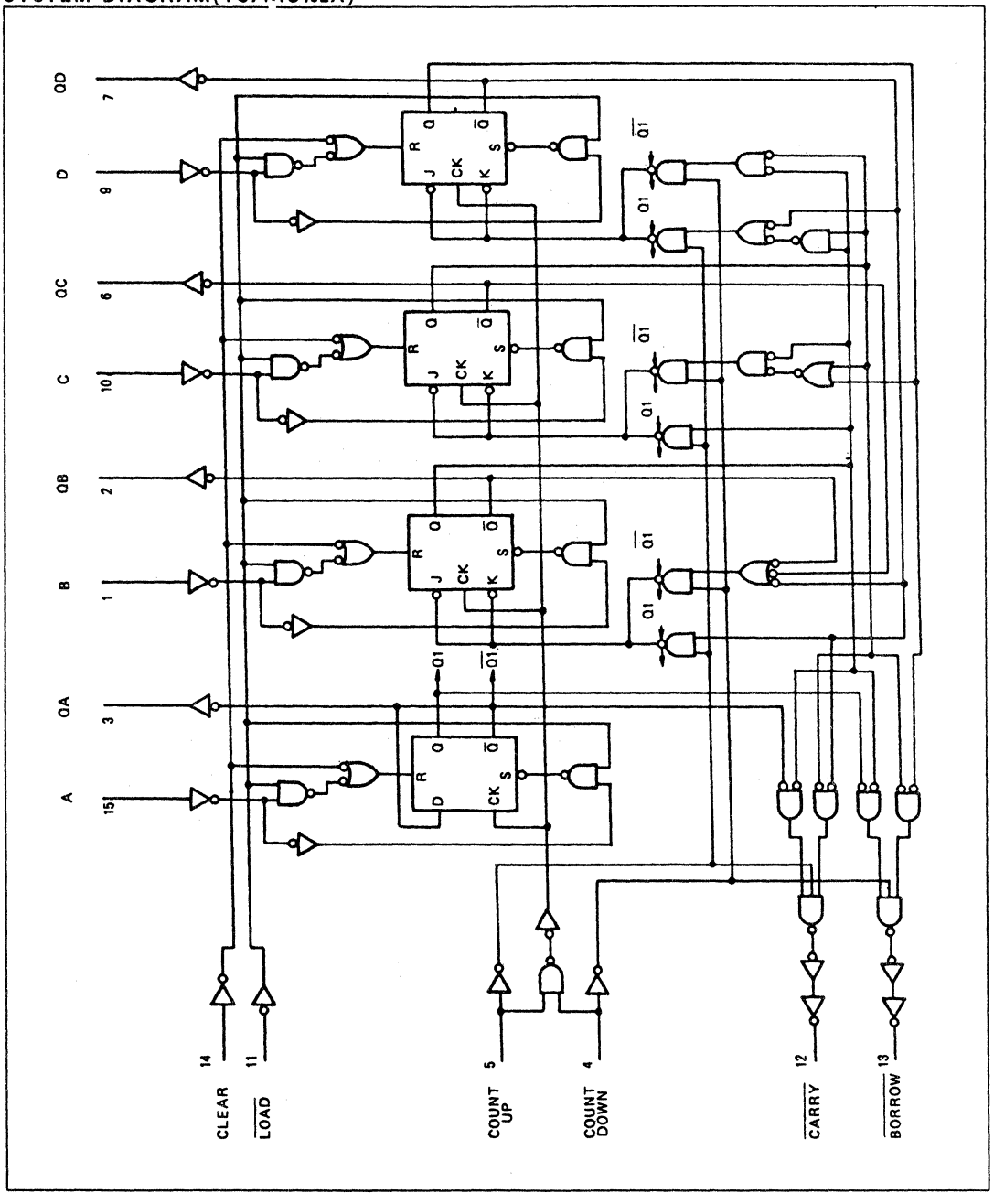
TIMING CHART(TC74HC192A)



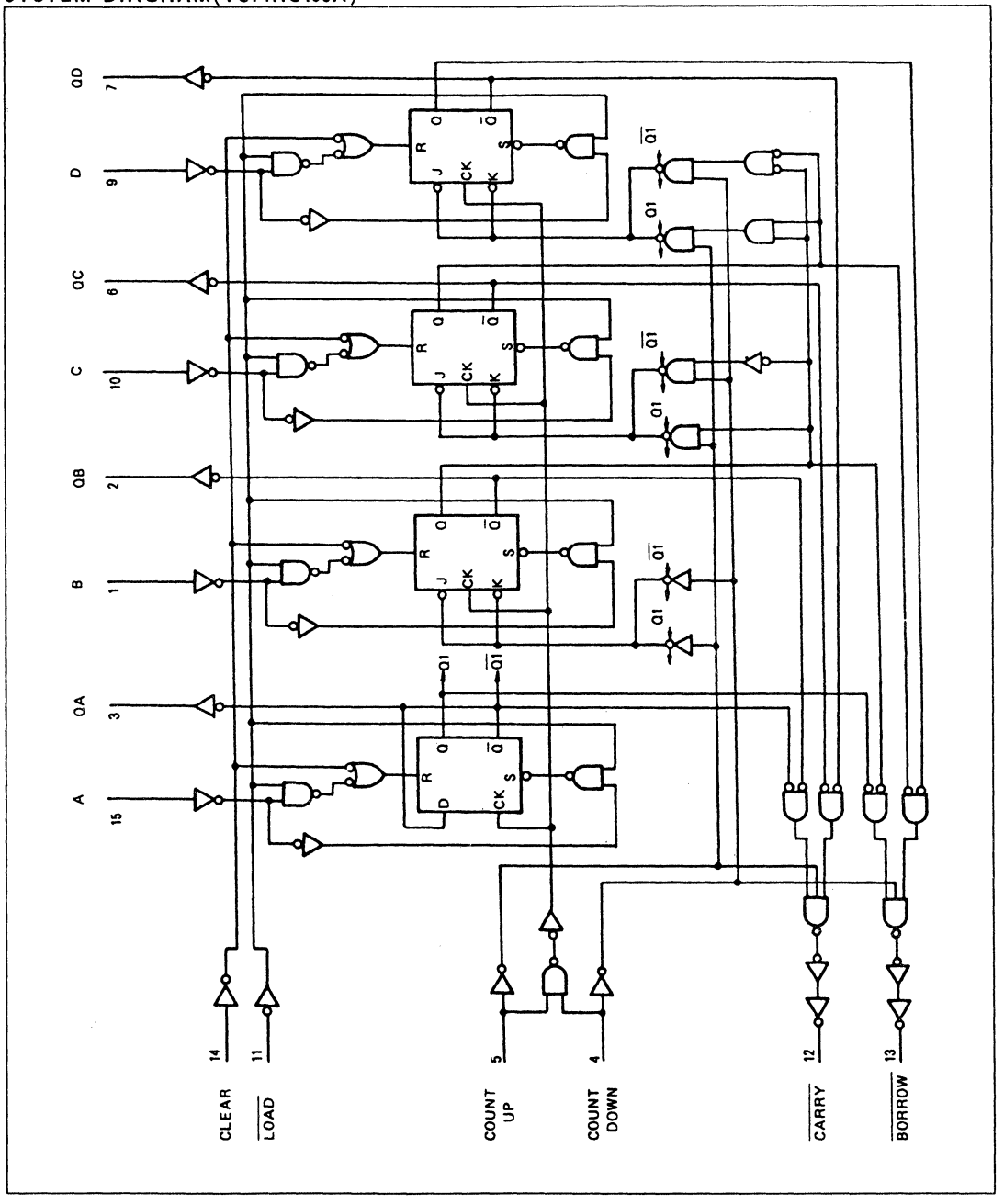
TIMING CHART(TC74HC193A)



SYSTEM DIAGRAM(TC74HC192A)



SYSTEM DIAGRAM(TC74HC193A)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	100	125	ns
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (CLEAR)	$t_{W(H)}$		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (DATA−$\overline{LOAD}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (DATA−$\overline{LOAD}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	10	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	10	
Clock Frequency	f		2.0	−	5	4	MHz
			4.5	−	25	20	
			6.0	−	29	24	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time (UP,DOWN–Q)	t_{pLH} t_{pHL}		–	16	33	
Propagation Delay Time (UP–$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		–	10	22	
Propagation Delay Time (DOWN–$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		–	10	22	
Propagation Delay Time ($\overline{\text{LOAD}}$–Q)	t_{pLH} t_{pHL}		–	21	38	
Propagation Delay Time ($\overline{\text{LOAD}}$–$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		–	25	44	
Propagation Delay Time ($\overline{\text{LOAD}}$–$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		–	26	44	
Propagation Delay Time (DATA IN–Q)	t_{pLH} t_{pHL}		–	21	33	
Propagation Delay Time (DATA IN–$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		–	29	44	
Propagation Delay Time (DATA IN–$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		–	26	44	
Propagation Delay Time (CLEAR–Q)	t_{pHL}		–	25	39	
Propagation Delay Time (CLEAR–$\overline{\text{CARRY}}$)	t_{pLH}		–	30	44	
Propagation Delay Time (CLEAR–$\overline{\text{BORROW}}$)	t_{pHL}		–	30	44	
Maximum Clock Frequency	f_{MAX}		27	52	–	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (UP,DOWN−Q)	t_{pLH} t_{pHL}		2.0	−	65	190	−	240	
			4.5	−	20	38	−	48	
			6.0	−	16	32	−	41	
Propagation Delay Time (UP−$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		2.0	−	40	130	−	165	
			4.5	−	13	26	−	33	
			6.0	−	11	22	−	28	
Propagation Delay Time (DOWN−$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		2.0	−	40	130	−	165	
			4.5	−	13	26	−	33	
			6.0	−	11	22	−	28	
Propagation Delay Time ($\overline{\text{LOAD}}$−Q)	t_{pLH} t_{pHL}		2.0	−	85	220	−	275	
			4.5	−	25	44	−	55	
			6.0	−	20	37	−	47	
Propagation Delay Time ($\overline{\text{LOAD}}$−$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		2.0	−	110	250	−	315	
			4.5	−	30	50	−	63	
			6.0	−	25	43	−	54	
Propagation Delay Time ($\overline{\text{LOAD}}$−$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		2.0	−	110	250	−	315	
			4.5	−	30	50	−	63	
			6.0	−	25	43	−	54	
Propagation Delay Time (DATA IN−Q)	t_{pLH} t_{pHL}		2.0	−	80	190	−	240	
			4.5	−	25	38	−	48	
			6.0	−	20	32	−	41	
Propagation Delay Time (DATA IN−$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}		2.0	−	120	250	−	315	
			4.5	−	34	50	−	63	
			6.0	−	28	43	−	54	
Propagation Delay Time (DATA IN−$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}		2.0	−	110	250	−	315	
			4.5	−	31	50	−	63	
			6.0	−	25	43	−	54	
Propagation Delay Time (CLEAR−Q)	t_{pHL}		2.0	−	100	225	−	280	
			4.5	−	30	45	−	56	
			6.0	−	25	38	−	48	
Propagation Delay Time (CLEAR−$\overline{\text{CARRY}}$)	t_{pLH}		2.0	−	120	250	−	315	
			4.5	−	35	50	−	63	
			6.0	−	29	43	−	54	
Propagation Delay Time (CLEAR−$\overline{\text{BORROW}}$)	t_{pHL}		2.0	−	120	250	−	315	
			4.5	−	35	50	−	63	
			6.0	−	29	43	−	54	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	−	4	−	MHz
			4.5	25	48	−	20	−	
			6.0	29	55	−	24	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74HC192A		−	68	−	−	−	
		TC74HC193A			67	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC194AP/AF

4-BIT PIPO SHIFT REGISTER

The TC74HC194A is a high speed CMOS BIDIRECTIONAL SHIFT REGISTER fablicated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of a parallel in,parallel out 4 bit register with SHIFT RIGHT and SHIFT LEFT input. In the parallel mode, data bits A~D are shifted into the internal flip-flops on the positive transition of CLOCK.

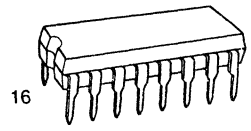
SHIFT RIGHT and SHIFT LEFT inputs are inhibited during parallel operating mode. In the shift right(shift left)mode, data from SHIFT RIGHT(SHIFT LEFT)input is shifted to the right(left)by 1 bit, synchronously with the positive transition of CLOCK.

A direct $\overline{CLEAR}$ input overrides all other inputs, including CLOCK, and sets all flip-flops to low.

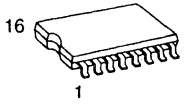
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=70MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS194

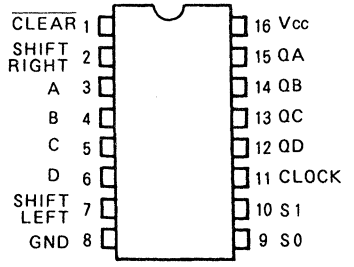


P(DIP16-P-300A)



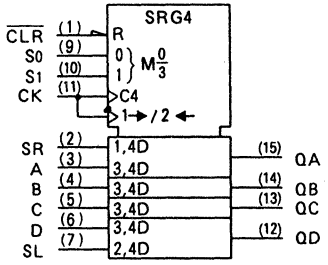
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS										OUTPUTS			
$\overline{\text{CLEAR}}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SL	SR	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	⌐	X	X	X	X	X	X	QAo	QBo	QCo	QDo
H	H	H	⌐	X	X	a	b	c	d	a	b	c	d
H	L	H	⌐	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	⌐	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	⌐	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	⌐	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QAo	QBo	QCo	QDo

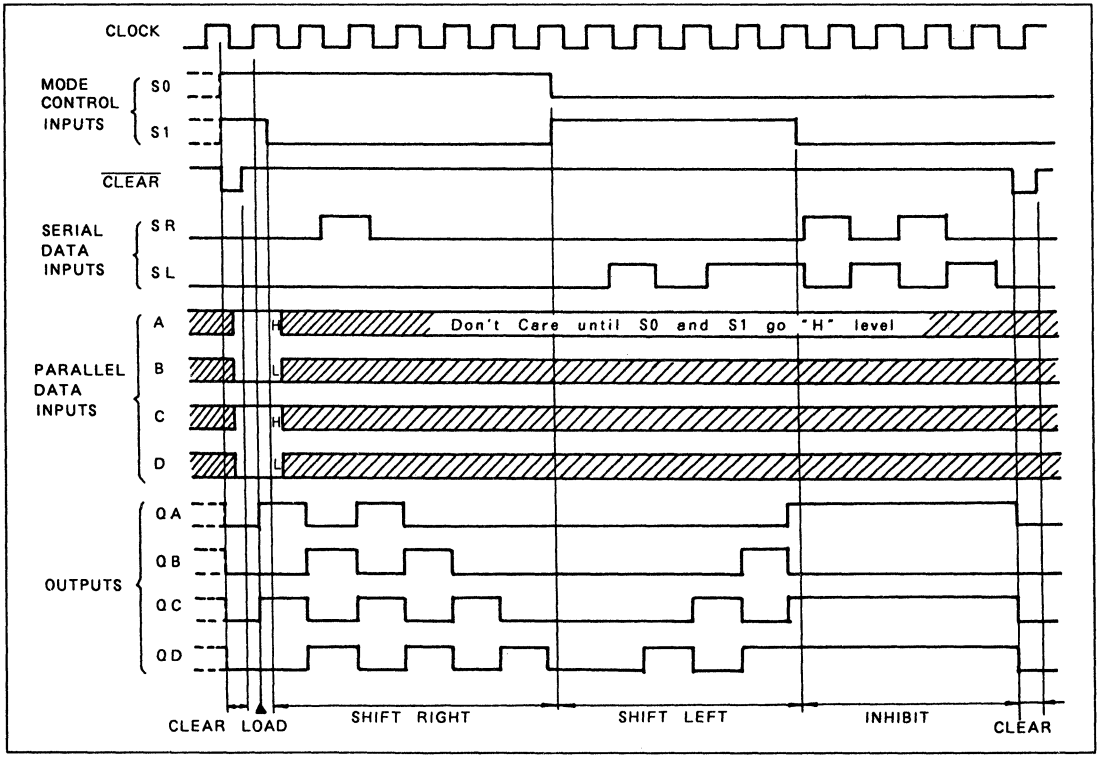
X:Don't Care

a~d:The level of steady state input voltage at input A~D respectively.

QAo~QDo:No change.

QAn~QDn:The level of QA, QB, QC, QD, respectively, before the most-recent positive transition of the clock.

TIMING CHART



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

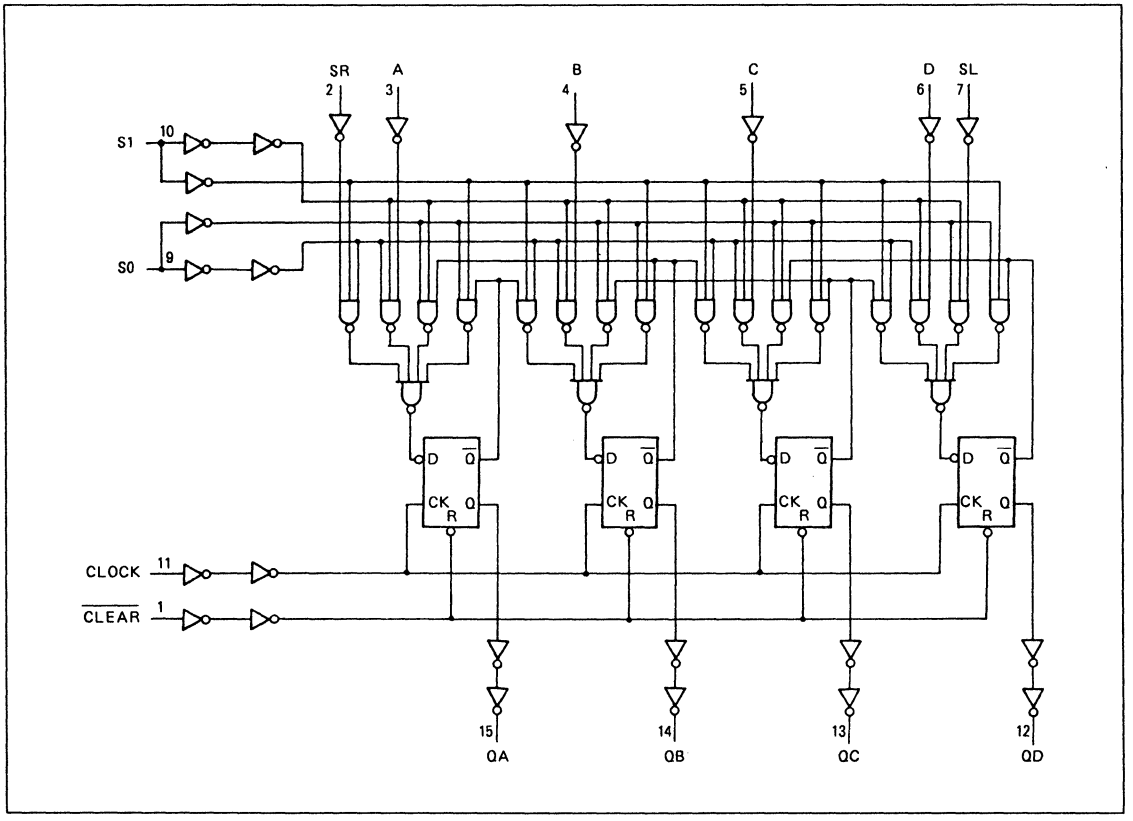
RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

SYSTEM DIAGRAM



TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI,PI)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (S0,S1)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	37	30	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	12	18	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		−	14	21	
Maximum Clock Frequency	f_{MAX}		34	70	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	48	115	−	145	
			4.5	−	15	23	−	29	
			6.0	−	13	20	−	25	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		2.0	−	52	125	−	155	
			4.5	−	17	25	−	31	
			6.0	−	15	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	31	64	−	25	−	
			6.0	37	77	−	30	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	87	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC195AP/AF

4-BIT PIPO SHIFT REGISTER

The TC74HC195A is a high speed CMOS 4-BIT SHIFT REGISTER fabricated with silicon gate C ^{2} MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The HC195A consists of parallel inputs, parallel outputs, two serial inputs (J,$\overline{K}$), and a SHIFT/$\overline{LOAD}$ input to control the device. When S/$\overline{L}$ is held low, the parallel data inputs are enabled, synchronous loading occurs and these data appear at the outputs on the next positive going edge of CLOCK.

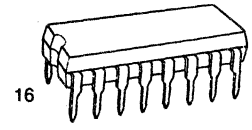
When S/$\overline{L}$ is held high, the serial data inputs are enabled, and the four flip-flops perform serial shifting on the positive going edge of each clock pulse.

The $\overline{CLEAR}$ input overrides all other inputs, including the clock, and sets all flip-flops low.

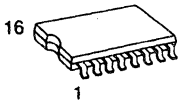
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=68MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS195

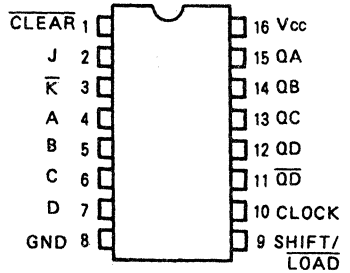


P(DIP16-P-300A)



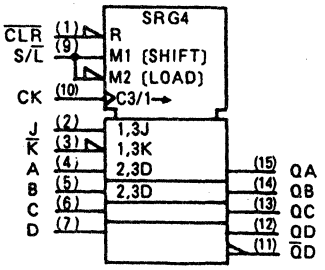
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD	$\overline{QD}$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QC0	$\overline{Q}$D0
H	H	↑	L	H	X	X	X	X	QAn	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	L	L	X	X	X	X	L	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	H	X	X	X	X	H	QAn	QBn	QCn	$\overline{Q}$Cn
H	H	↑	H	L	X	X	X	X	$\overline{Q}$An	QAn	QBn	QCn	$\overline{Q}$Cn

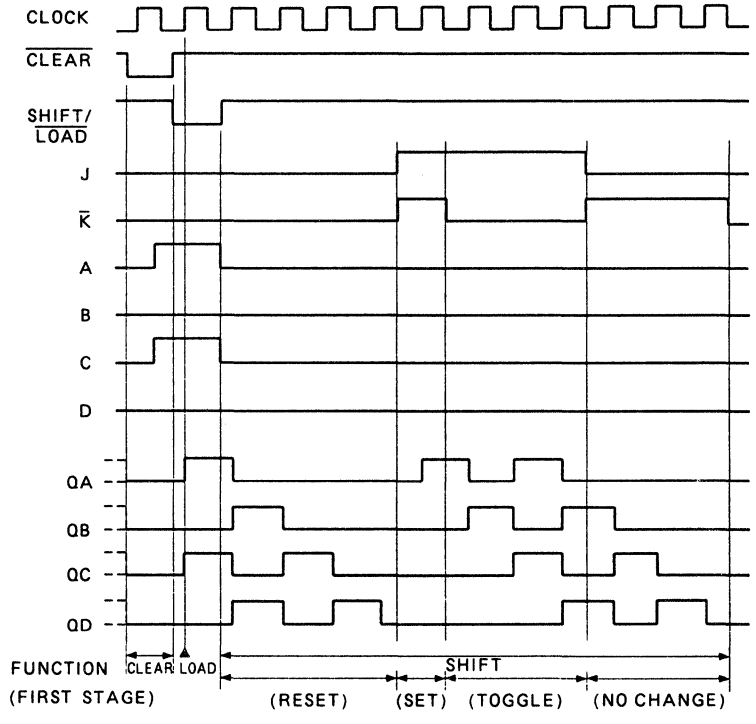
X : Don't care

QA0~AD0 : No change

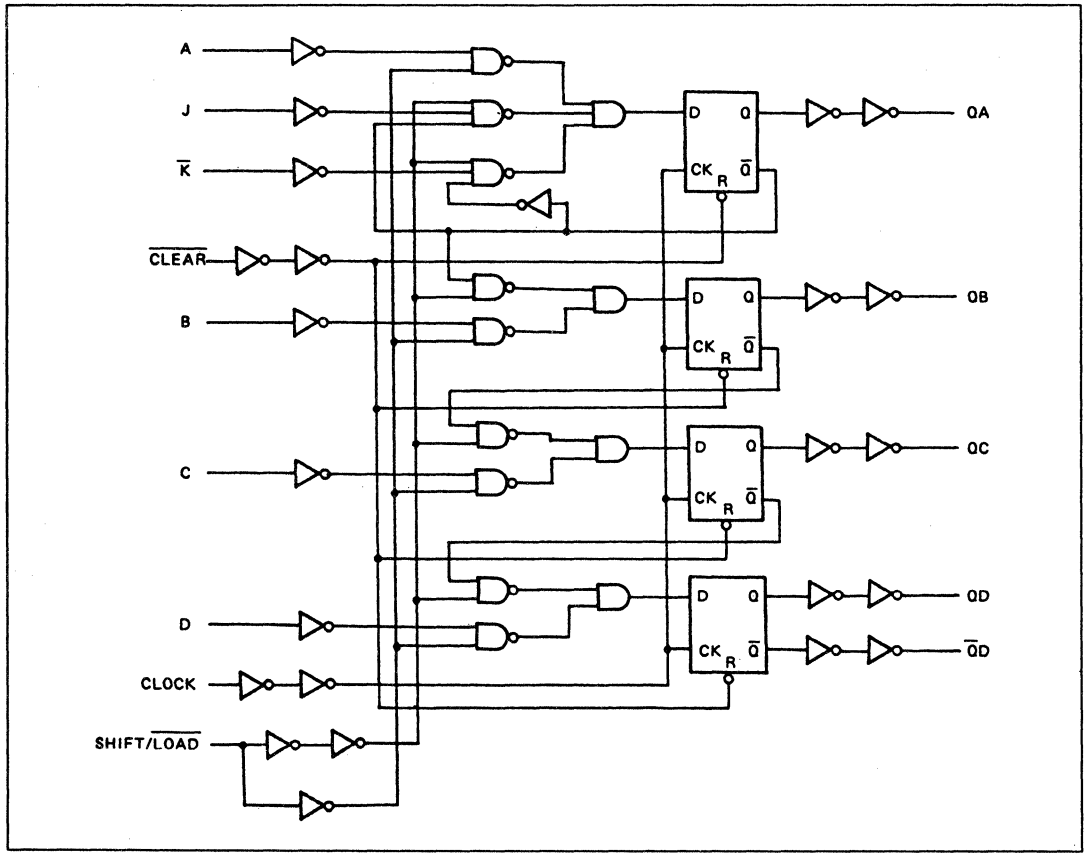
QAn~QDn : The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

a . . . d, $\overline{d}$: The level of steady state input voltage at inputs A~D respectively.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ～85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A,B,C,D)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (J, $\overline{K}$, S/$\overline{L}$)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	38	30	
			6.0	−	45	35	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		−	13	21	
Propagation Delay Time ($\overline{CLEAR}$−Qn, $\overline{QD}$)	t_{pLH} t_{pHL}		−	14	21	
Maximum Clock Frequency	f_{MAX}		41	68	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	47	125	−	155	
			4.5	−	16	25	−	31	
			6.0	−	13	21	−	26	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		2.0	−	49	125	−	155	
			4.5	−	17	25	−	31	
			6.0	−	14	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	7	15	−	6	−	MHz
			4.5	38	60	−	30	−	
			6.0	45	75	−	35	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	76	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC221AP/AF/AFN

DUAL MONOSTABLE MULTIVIBRATOR

The TC74HC221A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (tr=tf=1sec.) as they are schmitt trigger inputs. This device may also be triggered by using $\overline{CLR}$ input (Positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the $\overline{CLR}$ input breaks this state.

Limitations for Cx and Rx are :

External capacitor Cx....more than 100pF

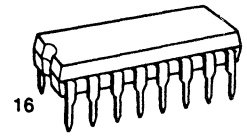
External resistor Rx.... Vcc<2.0V more than 5KΩ

Vcc ≥3.0V more than 1KΩ

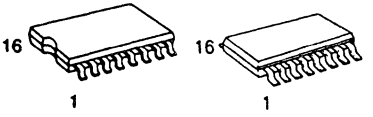
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=25ns(typ.)at V_{CC}=5V
- Low Power Dissipation
  - Standby State I_{CC} =4μA(max.)at Ta=25℃
  - Active State I_{CC}=700μA(max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V_{CC}
- Pin and Function Compatible with 74LS221

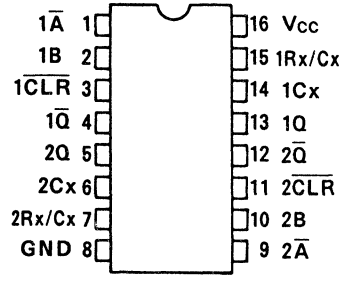


P(DIP16-P-300A)



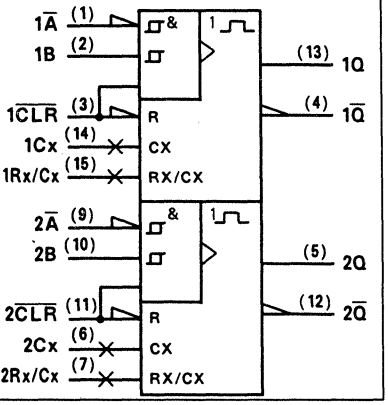
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

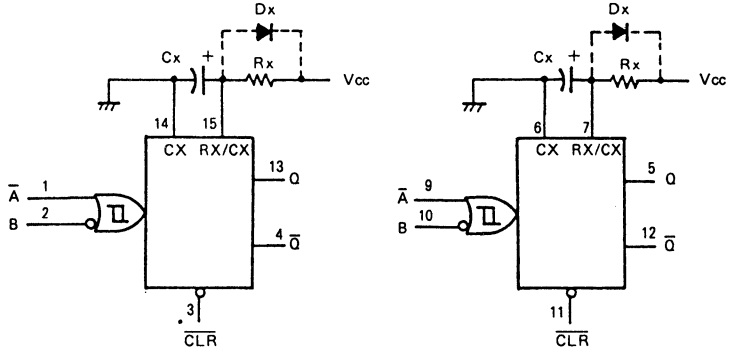


TRUTH TABLE

INPUT			OUTPUT		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
L	H	↑	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:Don't Care

BLOCK DIAGRAM



Notes: (1)Cx,Rx,Dx are external .
Capacitor,Resistor,and Diode,respectively.

(2)External clamping diode,Dx;

The external capacitor is charged to Vcc level in the wait state, i.e. when no trigger is applied. If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and Vcc drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and Vcc drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20mA.

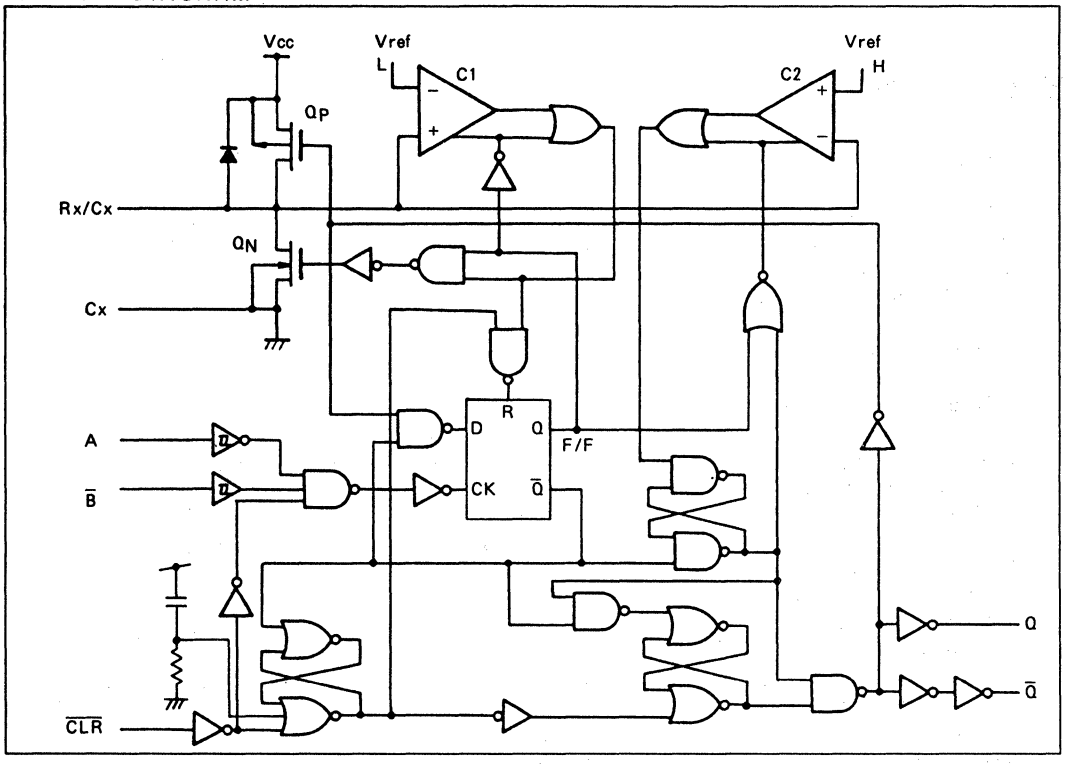
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (Vcc-0.7)\ Cx/20mA$$

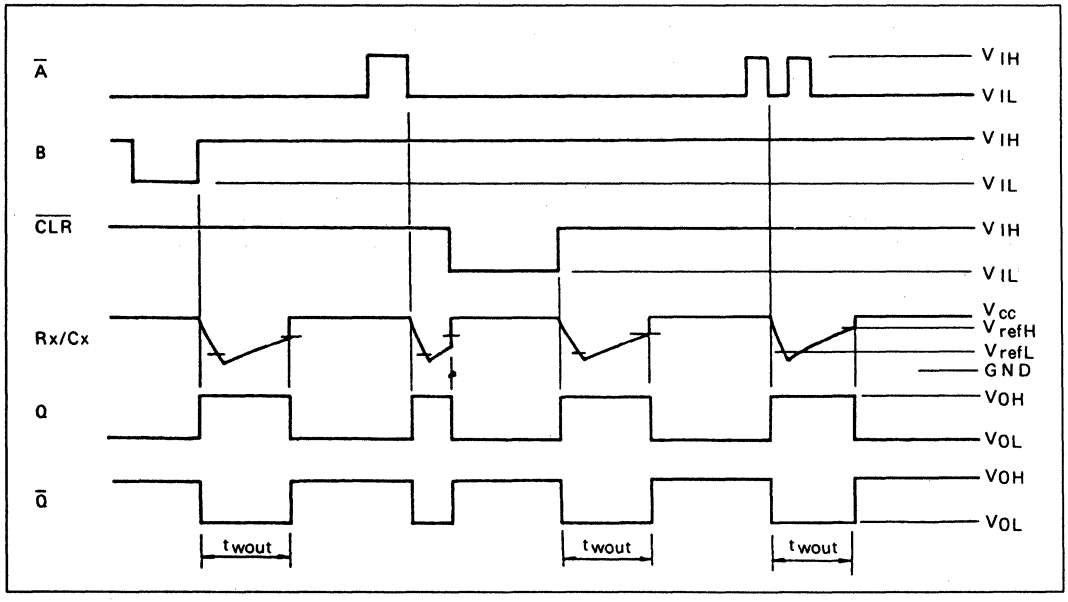
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 Vcc.)

In the event a system does not satisfy the above condition,an external clamping diode (Dx) is needed to protect the IC from rush current.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1)Stand-by State

The external capacitor(Cx) is fully charge to Vcc in the stand-by state. That means, befor triggering, the Q_P and Q_N transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2)Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal; and third, where the $\overline{A}$ input is low and the B input is high, and the $\overline{CLR}$ input has a rising signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level at the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

After Q_N turns off, the voltage at the Rx/Cx node starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx reaches Vref H, the IC returns to its MONO STABLE state.

With large value of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse tw(OUT) is as follows:

$$tw(OUT) = 1.0 \cdot Cx \cdot Rx$$

(3)Reset operation

In normal operation, $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and trigger control F/F is reset. Also Q_P turns on and Cx is charged rapidly to Vcc.

This means if $\overline{CLR}$ input is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	$0 \sim 1000$(V_{CC} =2.0V) $0 \sim 500$(V_{CC} =4.5V) $0 \sim 400$(V_{CC} =6.0V)	ns
External Capactior	Cx	More than 100pF*	F
External Resistor	Rx	$\geq$ 5K* (V_{CC} <3.0V) $\geq$ 1K* ($V_{CC} \geq$ 3.0V)	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC221A, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for Rx>1MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage (Q,$\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage (Q,$\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Rx/Cx Terminal Off−State Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active−State * Supply Current	I_{CC}	V_{IN} =V_{CC} or GND, Rx/Cx =0.5V_{CC}		2.0	−	45	200	−	260	μA
				4.5	−	400	500	−	650	μA
				6.0	−	0.7	1.0	−	1.3	mA

*: per circuit

TIMING REQUIREMENTS(Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Width	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{A}$,B–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		–	25	36	
Propagation Delay Time ($\overline{CLR}$ TRIGGER–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		–	25	41	
Propagation Delay Time ($\overline{CLR}$–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		–	16	27	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

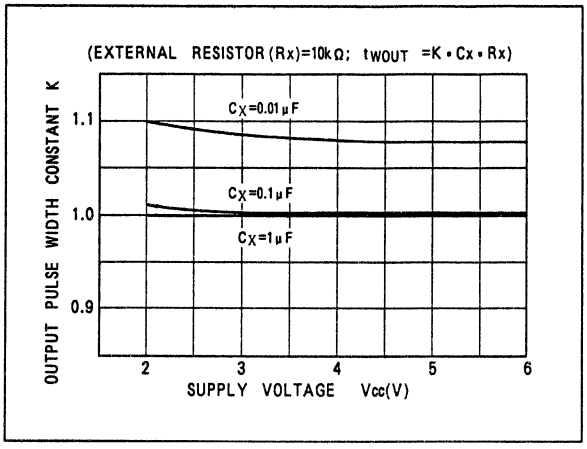
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{A}$,B–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	102	210	–	265	
			4.5	–	30	42	–	53	
			6.0	–	24	36	–	45	
Propagation Delay Time ($\overline{CLR}$ TRIGGER–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	102	235	–	295	
			4.5	–	30	47	–	59	
			6.0	–	24	40	–	50	
Propagation Delay Time ($\overline{CLR}$–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	67	160	–	200	
			4.5	–	20	32	–	40	
			6.0	–	16	27	–	34	
Output Pulse Width	tw_{OUT}	Cx=28pF Rx=6KΩ(V_{CC}=2V) Rx=2KΩ(V_{CC}=4.5V,6V)	2.0	–	700	2000	–	2500	ns
			4.5	–	250	400	–	500	
			6.0	–	210	340	–	425	
		Cx=0.01μF Rx=10KΩ	2.0	90	110	130	90	130	μs
			4.5	95	105	115	95	115	
			6.0	95	105	115	95	115	
		Cx=0.1μF Rx=10KΩ	2.0	0.9	1.0	1.2	0.9	1.2	ms
			4.5	0.9	1.0	1.1	0.9	1.1	
			6.0	0.9	1.0	1.1	0.9	1.1	
Output Pulse Width Error. Between Circuits (In same Package)	Δtw_{OUT}			–	±1	–	–	–	%
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	174	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

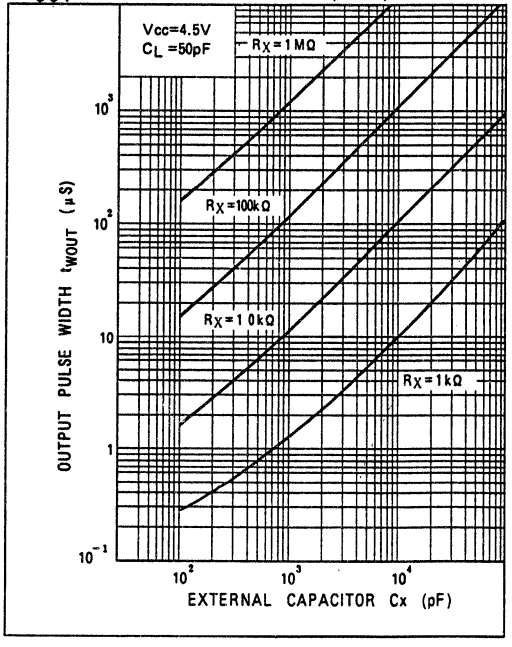
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per circuit)

(I_{CC}' : Active Supply Current)
(Duty:%)

OUTPUT PULSE WIDTH CONSTANT K-SUPPLY VOLTAGE (TYPICAL)



tw OUT -Cx CHARACTERISTICS (TYP.)



TC74HC237AP/AF

3-TO-8 LINE DECODER/LATCH

The TC74HC237A is a high speed CMOS 3-to-8 LINE DECODER ADRESS LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

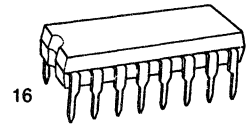
It is composed of 3-bit input latches with a common $\overline{GL}$ enable input and 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into the input latch on the high level of $\overline{GL}$. The value of this data determines which one of outputs will go to low.

When the enable input G1 is held low or $\overline{G2}$ is held high, decoding function is inhibited and all 8 outputs go high. The two enable inputs are provide to ease cascade connection and permits the application address decoder for memory system.

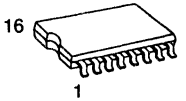
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=12ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS237

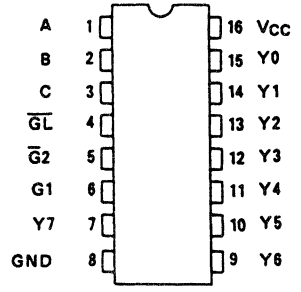


P(DIP16-P-300A)



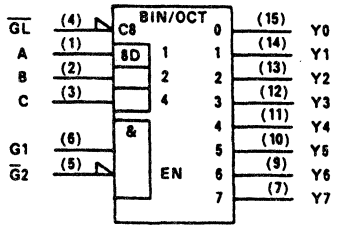
F(SOP16-P-300)

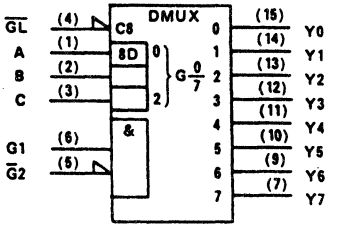
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



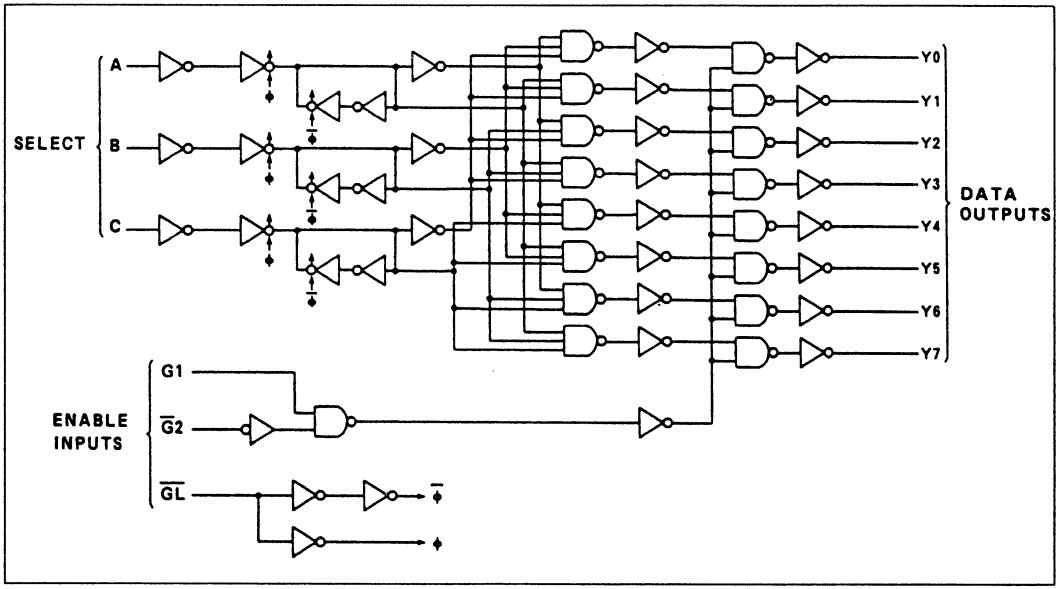


TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	Depends upon the address previously applied while $\overline{GL}$ was at a low level							

X : Don't Care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{GL}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A,B,C−$\overline{GL}$)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (A,B,C−$\overline{GL}$)	t_h		2.0	−	25	30	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (G1−Y)	t_{pLH} t_{pHL}		−	12	24	
Propagation Delay Time ($\overline{G2}$−Y)	t_{pLH} t_{pHL}		−	12	24	
Propagation Delay Time ($\overline{GL}$−Y)	t_{pLH} t_{pHL}		−	17	33	
Propagation Delay Time (A,B,C−Y)	t_{pLH} t_{pHL}		−	15	31	

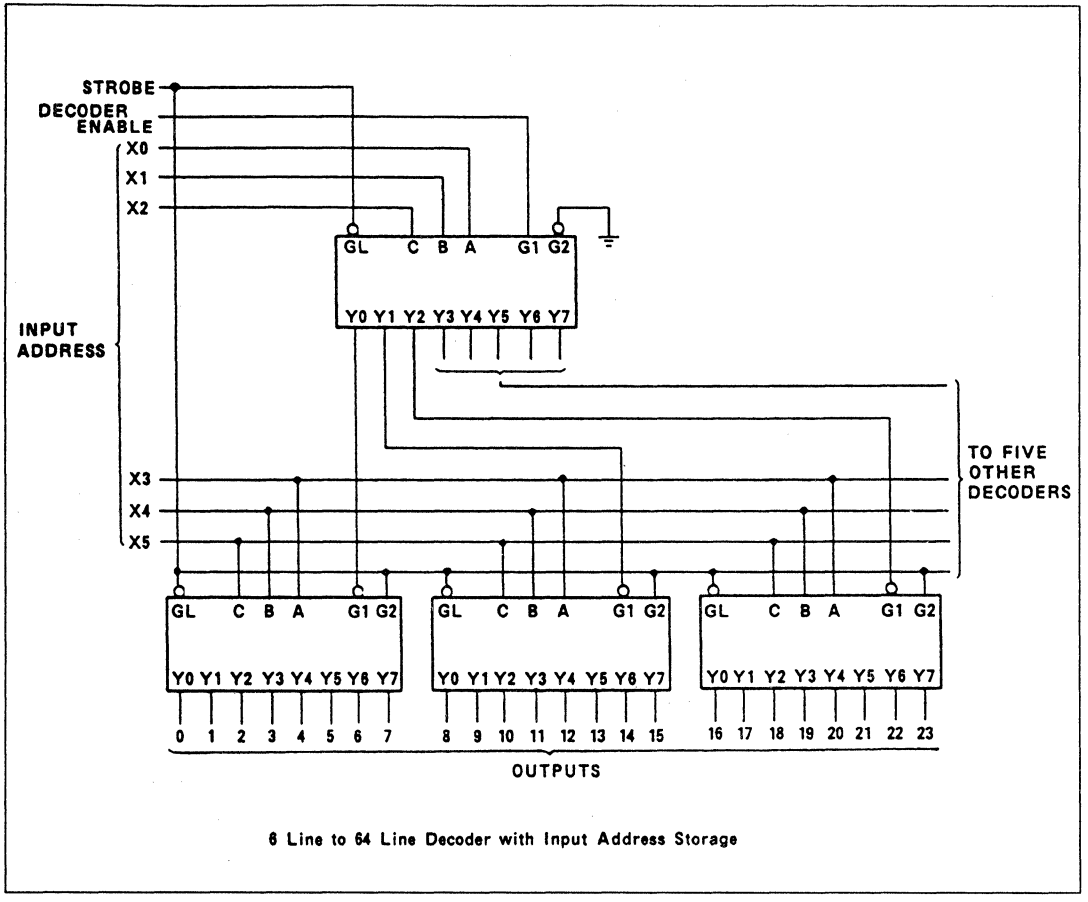
AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (G1−Y)	t_{pLH} t_{pHL}		2.0	−	45	140	−	175	
			4.5	−	15	28	−	35	
			6.0	−	13	24	−	30	
Propagation Delay Time ($\overline{G2}$−Y)	t_{pLH} t_{pHL}		2.0	−	45	140	−	175	
			4.5	−	15	28	−	35	
			6.0	−	13	24	−	30	
Propagation Delay Time ($\overline{GL}$−Y)	t_{pLH} t_{pHL}		2.0	−	65	190	−	240	
			4.5	−	21	38	−	48	
			6.0	−	18	32	−	41	
Propagation Delay Time (A,B,C−Y)	t_{pLH} t_{pHL}		2.0	−	60	180	−	225	
			4.5	−	19	36	−	45	
			6.0	−	16	31	−	38	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	52	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}$$

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

3-TO-8 LINE DECODER

The TC74HC238A is a high speed CMOS 3-to-8 DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

When the device is enabled,3 Binary Select inputs(A,B and C)determine which one of the outputs(Y0-Y1)will go high.

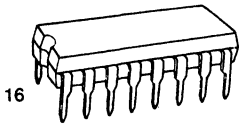
When enable input G1 is held low or either $\overline{G}2A$ or $\overline{G}2B$ is held high,decoding function is inhibited and all the outputs go low.

G1,$\overline{G}2A$,and $\overline{G}2B$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

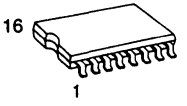
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· tpd=14ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH} =V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS238

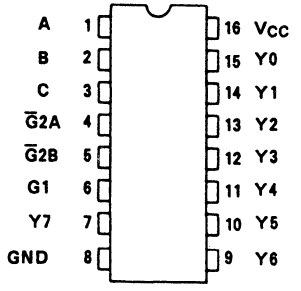


P(DIP16-P-300A)



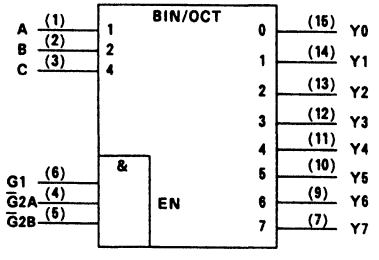
F(SOP16-P-300)

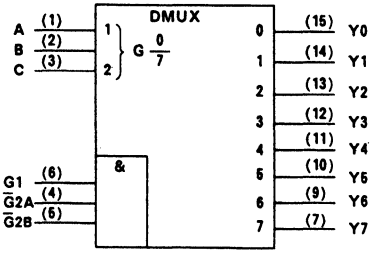
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



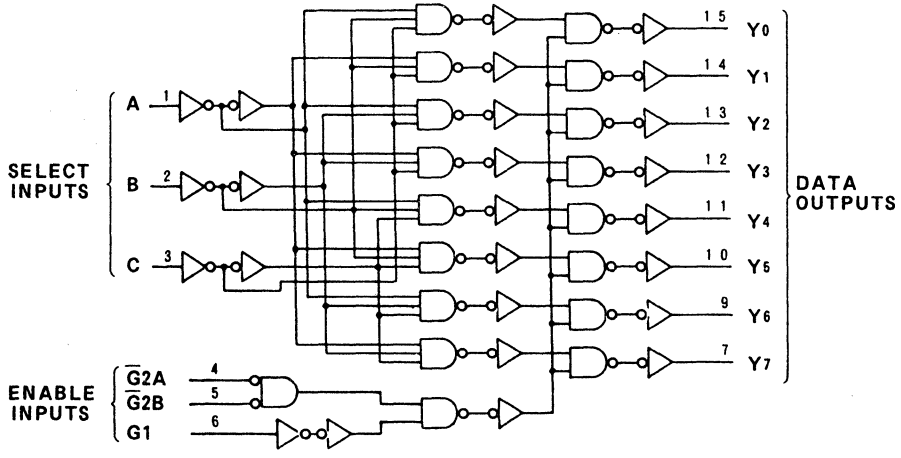


TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
L	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
X	X	H	X	X	X	L	L	L	L	L	L	L	L	NONE
H	L	L	L	L	L	H	L	L	L	L	L	L	L	Y0
H	L	L	L	L	H	L	H	L	L	L	L	L	L	Y1
H	L	L	L	H	L	L	L	H	L	L	L	L	L	Y2
H	L	L	L	H	H	L	L	L	H	L	L	L	L	Y3
H	L	L	H	L	L	L	L	L	L	H	L	L	L	Y4
H	L	L	H	L	H	L	L	L	L	L	H	L	L	Y5
H	L	L	H	H	L	L	L	L	L	L	L	H	L	Y6
H	L	L	H	H	H	L	L	L	L	L	L	L	H	Y7

X:Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (A,B,C–Y)	t_{pLH} t_{pHL}		–	14	26	
Propagation Delay Time (G,$\overline{G}$–$\overline{Y}$)	t_{pLH} t_{pHL}		–	14	26	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=–40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C–Y)	t_{pLH} t_{pHL}		2.0	–	50	150	–	190	
			4.5	–	17	30	–	38	
			6.0	–	15	26	–	32	
Propagation Delay Time (G,$\overline{G}$–Y)	t_{pLH} t_{pHL}		2.0	–	50	150	–	190	
			4.5	–	17	30	–	38	
			6.0	–	15	26	–	32	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	53	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC240AP/AF/AFW
TC74HC241AP/AF
TC74HC244AP/AF/AFW

OCTAL BUS BUFFER

TC74HC240AP/AF/AFW	INVERTED, 3-STATE OUTPUTS
TC74HC241AP/AF	NON-INVERTED, 3-STATE OUTPUTS
TC74HC244AP/AF/AFW	NON-INVERTED, 3-STATE OUTPUTS

The TC74HC240A, 241A and 244A are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

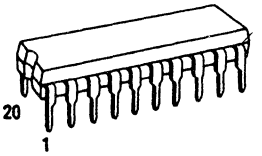
The 74HC240A is an inverting 3-state buffer having two active-low output enables. The TC74HC241A and TC74HC244A are non-inverting 3-state buffers that differ only in that the 241A has one active-high and one active-low output enable, and the 244A has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers, etc.

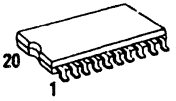
All inputs are equipped with protection circuits against static discharge or tansient excess voltage.

FEATURES:

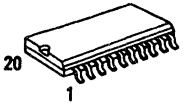
- High Speed ..... t_{pd}=10ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS240/241/244



P(DIP20-P-300A)



F(SOP20-P-300)



FW(SOL20-P-300)

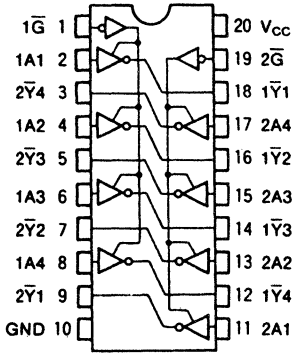
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	$G^{\triangle}$	A_n	Y_n	$\overline{Y}_n^{\triangle\triangle}$
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

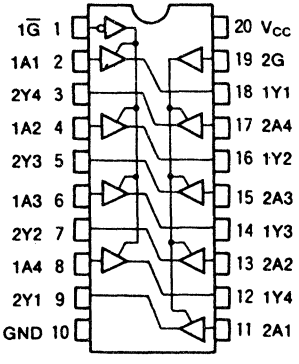
△ : for TC74HC241A only
△△ : for TC74HC240A only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)

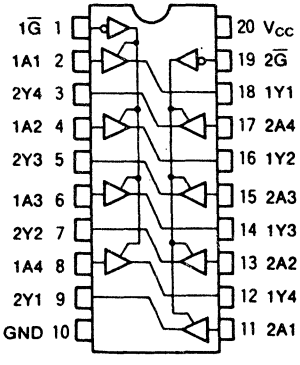
TC74HC240A



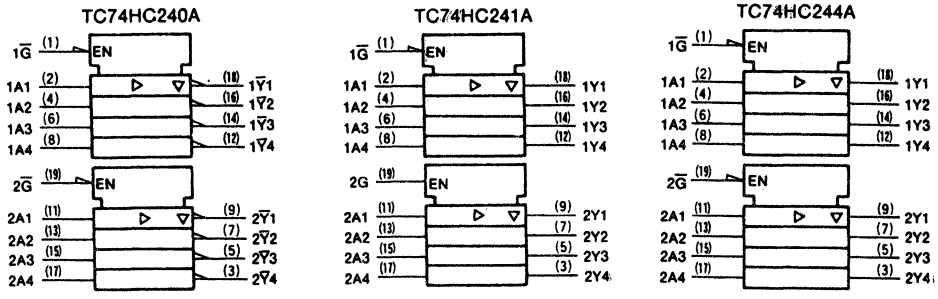
TC74HC241A



TC74HC244A



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	36	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	51	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	14	22	−	28	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	
	t_{pZH}		150	2.0	−	63	165	−	205	
				4.5	−	21	33	−	41	
				6.0	−	18	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	32	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	14	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC240A			−	31	−	−	−	
		TC74HC241A/244A			−	33	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HCT240AP/AF/AFW
TC74HCT241AP/AF
TC74HCT244AP/AF/AFW

OCTAL BUS BUFFER WITH TTL INPUT LEVEL

TC74HCT240AP/AF/AFW	INVERTED,3-STATE OUTPUTS
TC74HCT241AP/AF	NON-INVERTED,3-STATE OUTPUTS
TC74HCT244AP/AF/AFW	NON-INVERTED,3-STATE OUTPUTS

The TC74HCT240A, HCT241A and HCT244A are high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate C^2MOS technoligy.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

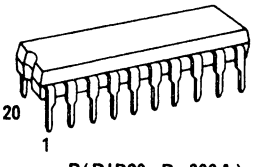
The TC74HCT240A is an inverting 3-state buffer having two active-low output enables. The TC74HCT241A and TC74HCT244A are non-inverting 3-state buffers that differ only in that the HCT241A has one active-high and one active-low output enable, and the HCT244A has two active-low output enables.

These devices are designed to be used with 3-state memory address drivers,etc.

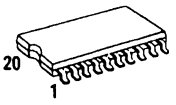
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

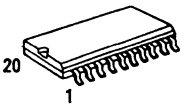
- High Speed ····· t_{pd}=13ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.),V_{IH}=2.0V(Min.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS240/241/244



P(DIP20-P-300A)



F(SOP20-P-300)



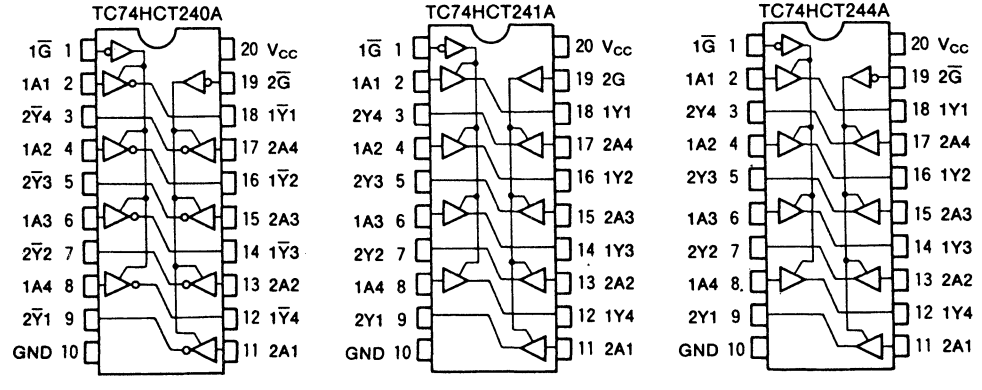
FW(SOL20-P-300)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

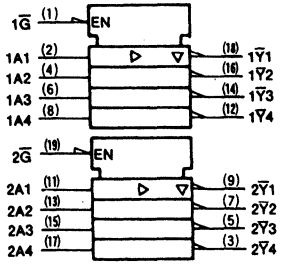
△ : TC74HCT241A Only
△△ : TC74HCT240A Only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)

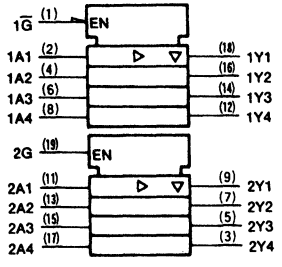


IEC LOGIC SYMBOL

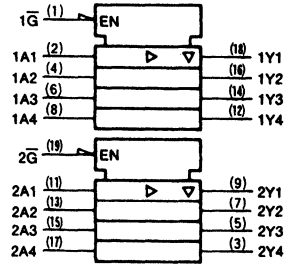
TC74HCT240A



TC74HCT241A



TC74HCT244A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperrature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r , t_f	$0 \sim 500$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ≀ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ≀ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	Per input: V_{IN} =0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time *	t_{pLH}		50	4.5	−	15	22	−	28	
				5.5	−	13	20	−	25	
	t_{pHL}		150	4.5	−	21	30	−	38	
				5.5	−	16	27	−	34	
Propagation Delay Time * *	t_{pLH}		50	4.5	−	15	25	−	31	
				5.5	−	13	22	−	28	
	t_{pHL}		150	4.5	−	21	33	−	41	
				5.5	−	18	29	−	37	
3−State Output Enable Time	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	14	27	−	34	
	t_{pZH}		150	4.5	−	23	38	−	48	
				5.5	−	20	34	−	43	
3−State Output Disable Time	t_{pLZ}	$R_L=1k\Omega$	50	4.5	−	16	30	−	38	
	t_{pHZ}			5.5	−	13	27	−	34	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An			−	13	−	−	−	
Power Dissipation Capacitance (Note 1)	C_{PD}	*			−	33	−	−	−	
		* *			−	31	−	−	−	

Note 1 : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}/8 \text{(per bit)}$$

Note 2 : *=TC74HCT240A
* *=TC74HCT241A/HCT244A

TC74HC242AP/AF
TC74HC243AP/AF

QUAD BUS TRANSCEIVER

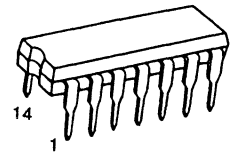
TC74HC242AP/AF 3-STATE,INVERTING
TC74HC243AP/AF 3-STATE,NON-INVERTING

The TC74HC242A and TC74HC243A are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C^2MOS technology.

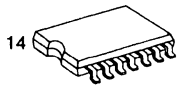
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are intended for two-way asynchronous communication between data busses, and the direction of data transmission is determined by $\overline{GAB}$, GBA.

All inputs are equipped with protection circuits against static discharge or tansient excess voltage.



P(DIP14-P-300)



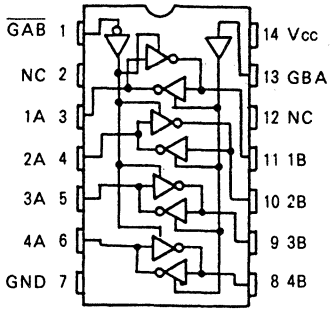
F(SOP14-P-300)

FEATURES:

- High Speed ····· t_{pd}=9ns(typ.) at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS242/243

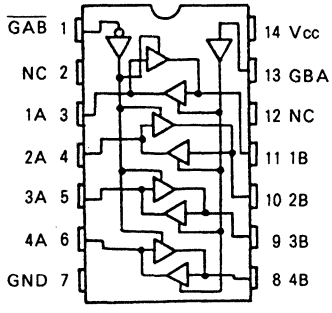
PIN ASSIGNMENT(TOP VIEW)

TC74HC242A



(TOP VIEW)

TC74HC243A



(TOP VIEW)

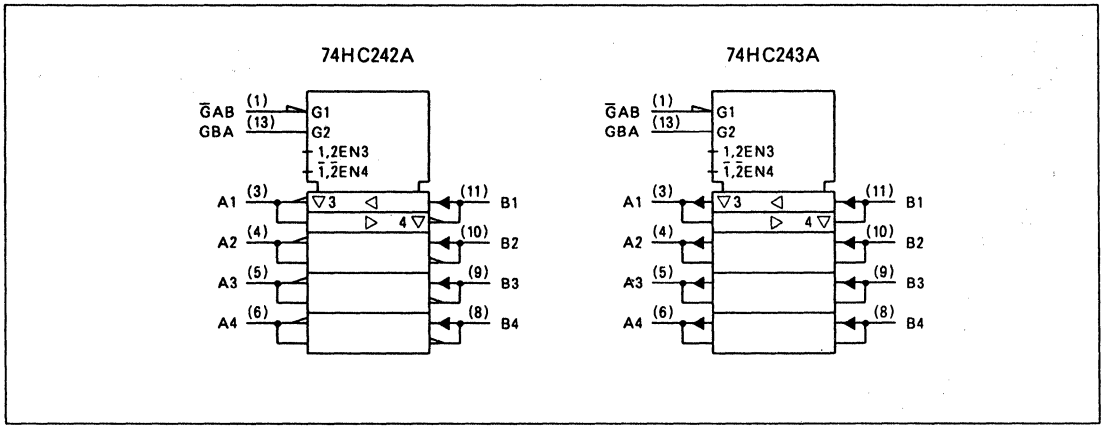
NC :NO CONNECTION

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GBA	A BUS	B BUS	HC242A	HC243A
H	H	OUTPUT	INPUT	A=$\overline{B}$	A=B
L	L	INPUT	OUTPUT	B=$\overline{A}$	B=A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

Z : HIGH IMPEDANCE

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
Bus Terminal Voltage	$V_{I/O}$	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃				Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

* Applicable only to $\overline{GAB}$, GBA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	38	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	54	145	−	180	
				4.5	−	17	29	−	36	
				6.0	−	14	25	−	31	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	55	145	−	180	
				4.5	−	17	29	−	36	
				6.0	−	15	25	−	31	
	t_{pZH}		150	2.0	−	73	185	−	230	
				4.5	−	22	37	−	46	
				6.0	−	17	31	−	39	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	42	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	15	26	−	33	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC242A			−	28	−	−	−	
		TC74HC243A			−	32	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

TC74HC245AP/AF/AFW
TC74HC640AP/AF
TC74HC643AP/AF

OCTAL BUS TRANSCEIVER
TC74HC245AP/AF 3-STATE, NON-INVERTING
TC74HC640AP/AF 3-STATE, INVERTING
TC74HC643AP/AF 3-STATE, INVERTING AND NON-INVERTING

The TC74HC245A, 640A and 643A are high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

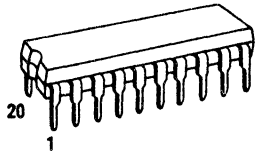
They are intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

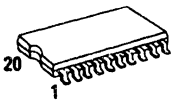
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

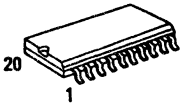
- High Speed ..... t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS245,640,643



P(DIP20-P-300A)



F(SOP20-P-300)



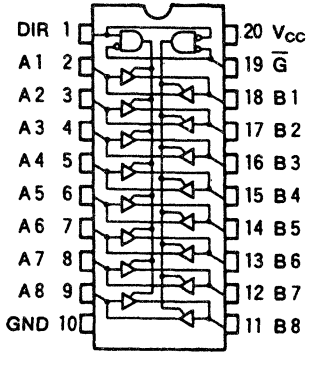
FW(SOL20-P-300)

APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)

TC74HC245A



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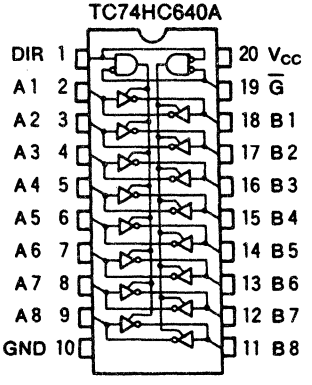
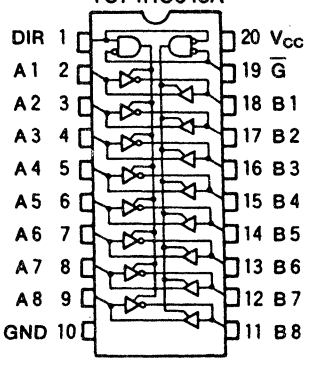
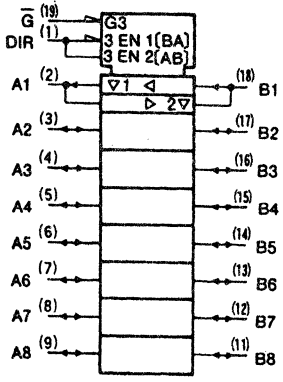


TC74HC643A



IEC LOGIC SYMBOL

TC74HC245A



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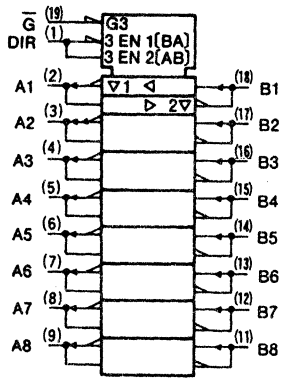

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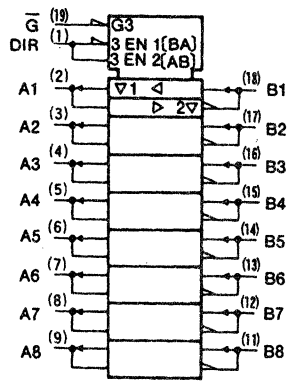


TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	HC245A	HC640A	HC643A
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High Impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	33	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	48	120	−	150	
				4.5	−	16	24	−	30	
				6.0	−	14	20	−	26	
3−State Output Enable Time	t_{pZL}	R_L = 1 kΩ	50	2.0	−	48	150	−	190	
				4.5	−	16	30	−	38	
				6.0	−	14	26	−	32	
	t_{pZH}		150	2.0	−	63	180	−	225	
				4.5	−	21	36	−	45	
				6.0	−	18	31	−	38	
3−State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	−	37	150	−	190	
				4.5	−	17	30	−	38	
				6.0	−	15	26	−	32	
Input Capacitance	C_{IN}	DIR, G			−	5	10	−	10	pF
Bus Input Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC245A			−	39	−	−	−	
		TC74HC640A/643A			−	37	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

TC74HCT245AP/AF/AFW
TC74HCT640AP/AF
TC74HCT643AP/AF/AFW

OCTAL BUS TRANSCEIVER

TC74HCT245AP/AF/AFW 3-STATE,NON-INVERTING
TC74HCT640AP/AF 3-STATE,INVERTING
TC74HCT643AP/AF/AFW 3-STATE,INVERTING AND NON-INVERTING

The TC74HCT245A, HCT640A and HCT643A are high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

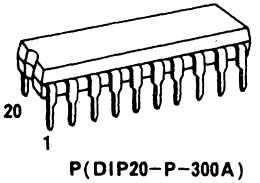
They are intended for two-way asynchronous communication between data busses. The direction of date transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

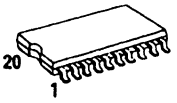
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

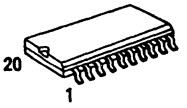
- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at TA=25℃
- Combatible with TTL outputs ····· V_{IL}=0.8V(Max.), V_{IH}=2.0(Min.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS245,640,643



P(DIP20-P-300A)



F(SOP20-P-300)



FW(SOL20-P-300)

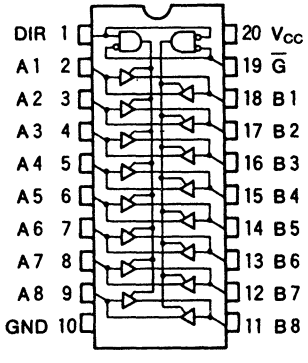
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is the output mode. Damage may result.

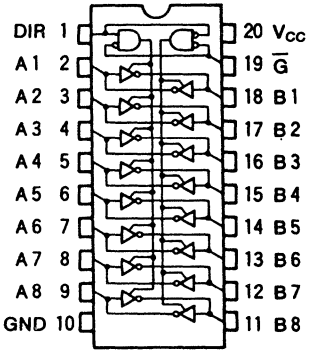
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)

TC74HCT245A



TC74HCT640A



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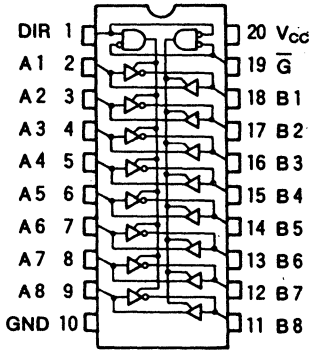
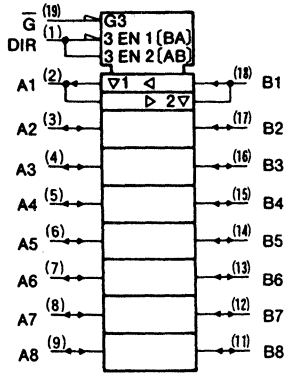


IEC LOGIC SYMBOL

TC74HCT245A



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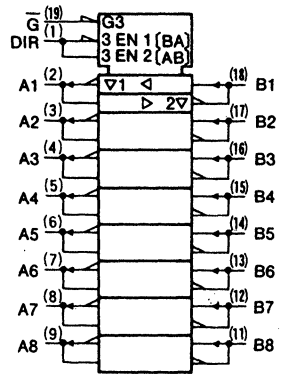

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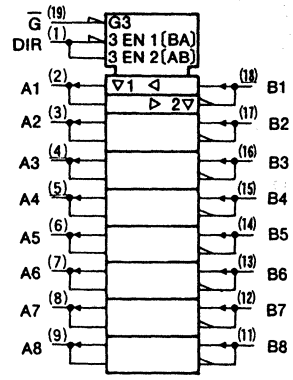


TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	HCT245A	HCT640A	HCT643A
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High Impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	Per input: V_{IN} = 0.5V or 2.4V, Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time	t_{pLH}		50	4.5	−	13	22	−	28	
				5.5	−	11	20	−	25	
	t_{pHL}		150	4.5	−	18	30	−	38	
				5.5	−	16	27	−	34	
3−State Output Enable Time	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
	t_{pZH}		150	4.5	−	24	38	−	48	
				5.5	−	22	34	−	43	
3−State Output Disable Time	t_{pLZ}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
	t_{pHZ}			5.5	−	16	27	−	34	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT245A			−	41	−	−	−	
		TC74HCT640A/T643A			−	39	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

8-CHANNEL MULTIPLEXER (3-STATE)

The TC74HC251A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

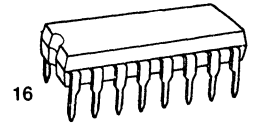
One of eight data input signals (D0-D7) is selected by decoding of the address inputs (A, B, C). The selected data appears on two outputs: non-inverting (Y) and inverting (W).

When the strobe input is held high, both outputs are in the high-impedance state.

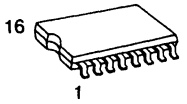
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =15ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS251

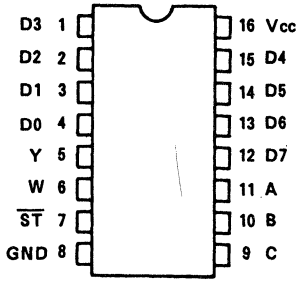


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



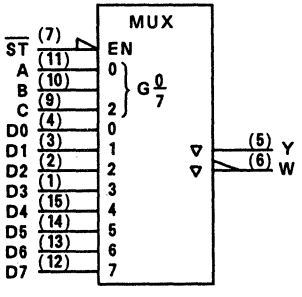
(TOP VIEW)

TRUTH TABLE

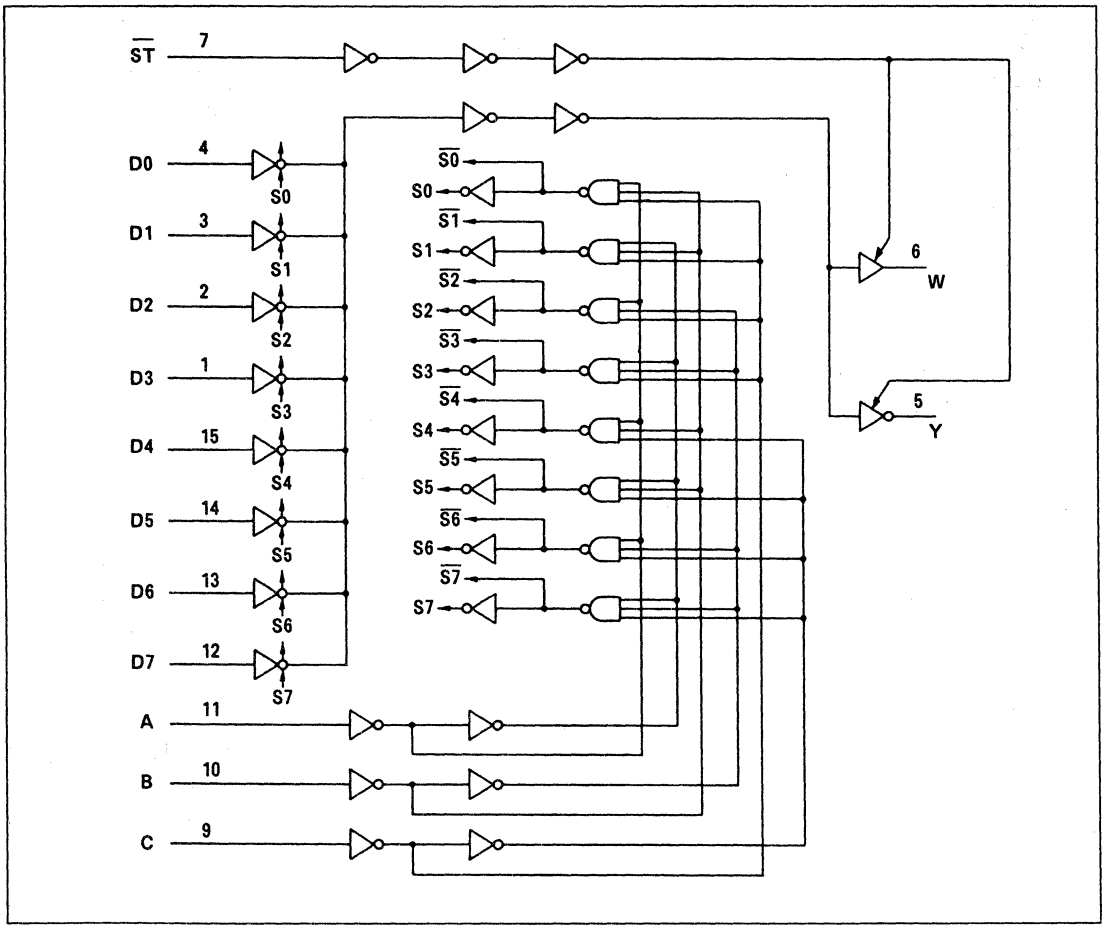
INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	$\overline{ST}$		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't care Z : High Impedance

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Off Leak Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		–	15	24	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		–	19	31	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		–	19	31	
3–State Output Enable Time	t_{pZL} t_{pZH}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (D–Y)	t_{pLH} t_{pHL}		2.0	–	65	140	–	175	
			4.5	–	17	28	–	35	
			6.0	–	14	24	–	30	
Propagation Delay Time (D–W)	t_{pLH} t_{pHL}		2.0	–	70	140	–	175	
			4.5	–	18	28	–	35	
			6.0	–	15	24	–	30	
Propagation Delay Time (A, B, C–Y)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
Propagation Delay Time (A, B, C–W)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	23	36	–	45	
			6.0	–	19	31	–	38	
3–State Output Enable Time	t_{pZL} t_{pZH}		2.0	–	40	105	–	130	
			4.5	–	13	21	–	26	
			6.0	–	10	19	–	22	
3–State Output Disable Time	t_{pLZ} t_{pHZ}		2.0	–	25	105	–	130	
			4.5	–	13	21	–	26	
			6.0	–	11	19	–	22	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	69	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC257AP/AF/AFN
TC74HC258AP/AF

TC74HC257AP/AF/AFN 2-CHANNEL MULTIPLEXER(3-STATE)
TC74HC258AP/AF 2-CHANNEL MULTIPLEXER(3-STATE,INVERTING)

The TC74HC257A and TC74HC258A are high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technolgy.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each is composed of four independent 2-channel multiplexers with common SELECT and $\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$($\overline{\text{OE}}$).

The TC74HC257A is an inverting multiplexer, while the TC74HC258A is non-inverting.

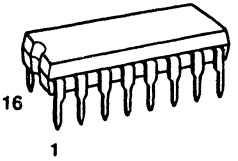
If $\overline{\text{OE}}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.

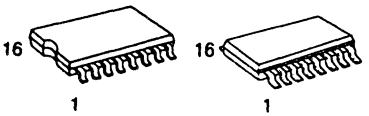
All inputs are equipped with protection citcuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· V_{NIH} =V_{NIL} =28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$ =I_{OL} =6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS257/258



P(DIP16-P-300A)



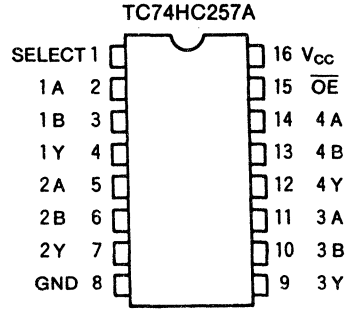
F(SOP16-P-300) FN(SOL16-P-150)

TRUTH TABLE

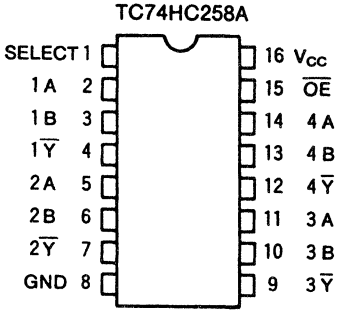
INPUTS				OUTPUTS	
$\overline{\text{OE}}$	SELECT	A	B	Y(257A)	$\overline{\text{Y}}$(258A)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care
Z : High Impedance

PIN ASSIGNMENT

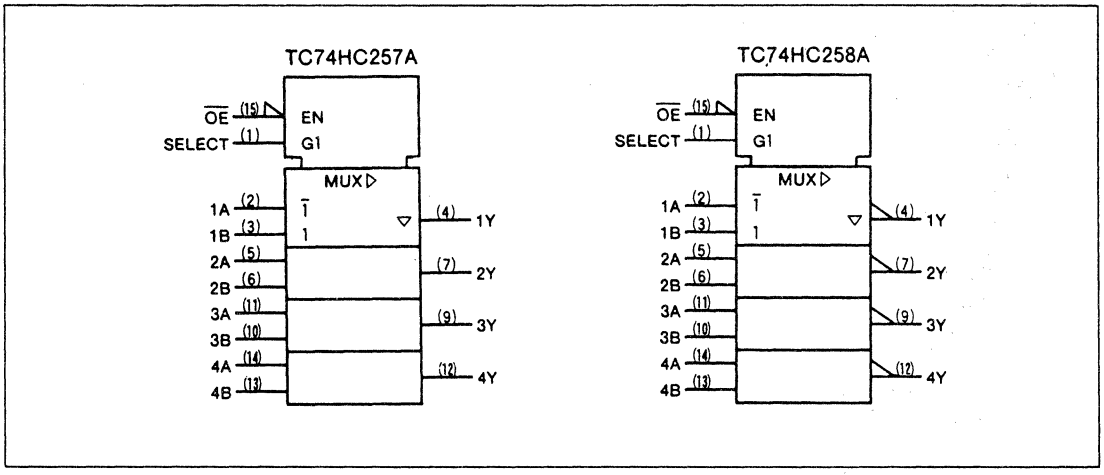


(TOP VIEW)



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (A, B−Y, $\overline{Y}$)	t_{pLH}		50	2.0	−	45	100	−	125	
				4.5	−	13	20	−	25	
				6.0	−	11	17	−	21	
	t_{pHL}		150	2.0	−	62	140	−	175	
				4.5	−	18	28	−	35	
				6.0	−	15	24	−	30	
Propagation Delay Time (SELECT−Y, $\overline{Y}$)	t_{pLH}		50	2.0	−	45	100	−	125	
				4.5	−	13	20	−	25	
				6.0	−	11	17	−	21	
	t_{pHL}		150	2.0	−	62	140	−	175	
				4.5	−	18	28	−	35	
				6.0	−	15	24	−	30	
3−State Output Enable Time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	40	110	−	140	
				4.5	−	12	22	−	28	
				6.0	−	10	19	−	24	
	t_{pZH}		150	2.0	−	57	150	−	190	
				4.5	−	17	30	−	38	
				6.0	−	14	26	−	33	
3−State Output Disable Time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	28	140	−	175	
				4.5	−	14	28	−	35	
				6.0	−	13	24	−	30	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC257A			−	47	−	−	−	
		TC74HC258A			−	47	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

TC74HCT257AP/AF
TC74HCT258AP/AF

TC74HCT257AP/AF QUAD 2-CHANNEL MULTIPLEXER(3-STATE)
TC74HCT258AP/AF QUAD 2-CHANNEL MULTIPLEXER(3-STATE,INVERTING)

The TC74HCT257A and TC74HCT258A are high speed CMOS MULTIPLEXERs fabricated with silicon gate C^2MOS technolgy.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each is composed of four independent 2-channel multiplexers with common SELECT and $\overline{\text{OUTPUT}}$ $\overline{\text{ENABLE}}$($\overline{\text{OE}}$).

The TC74HCT257A is an inverting multiplexer, while the TC74HC258A is non-inverting.

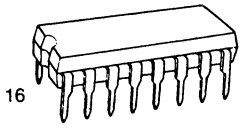
If $\overline{\text{OE}}$ is set low, the outputs are held in a high-impedance state. When SELECT is set low, "A" data inputs are enabled.

Conversely, when SELECT is high, "B" data inputs are enabled.

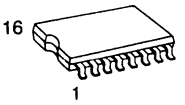
All inputs are equipped with protection citcuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =16ns(typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.), V_{IH}=2.0V(Min.)
- Wide Interfacing ability ····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS257/258



P(DIP16-P-300A)



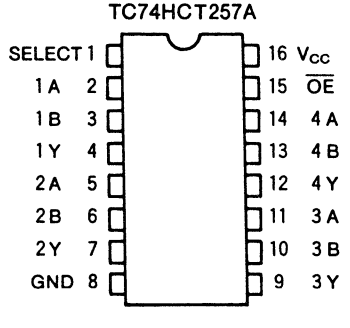
F(SOP16-P-300)

TRUTH TABLE

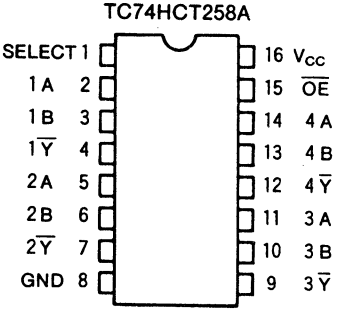
INPUTS				OUTPUTS	
$\overline{\text{OE}}$	SELECT	A	B	Y(257A)	$\overline{\text{Y}}$(258A)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't Care
Z : High Impedance

PIN ASSIGNMENT

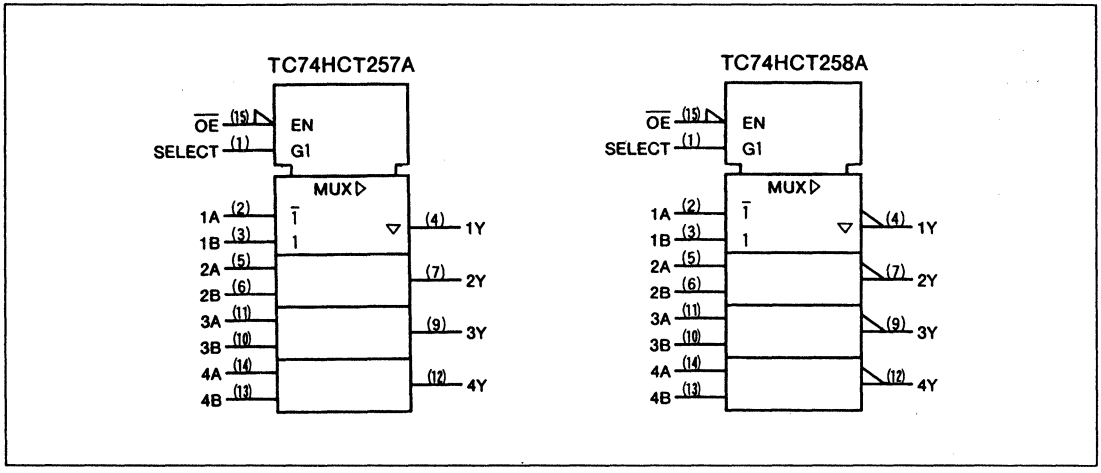


(TOP VIEW)



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperrature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r , t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{CC}	Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time (A,B−Y,$\overline{Y}$)	t_{pLH}	TC74HCT257A	50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
	t_{pHL}		150	4.5	−	24	38	−	48	
				5.5	−	20	35	−	44	
	t_{pLH}	TC74HCT258A	50	4.5	−	17	27	−	34	
				5.5	−	14	25	−	31	
	t_{pHL}		150	4.5	−	22	35	−	44	
				5.5	−	18	32	−	40	
Propagation Delay Time (SELECT−Y,$\overline{Y}$)	t_{pLH}		50	4.5	−	20	30	−	38	
				5.5	−	17	27	−	34	
	t_{pHL}		150	4.5	−	25	38	−	48	
				5.5	−	21	35	−	44	
3−State Output Enable Time	t_{pZL}	$R_L=1\,k\Omega$	50	4.5	−	18	30	−	38	
				5.5	−	15	27	−	34	
	t_{pZH}		150	4.5	−	23	38	−	48	
				5.5	−	19	35	−	44	
3−State Output Disable Time	t_{pLZ}	$R_L=1\,k\Omega$	50	4.5	−	16	30	−	38	
	t_{pHZ}			5.5	−	13	27	−	34	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance (Note 1)	C_{PD}	TC74HCT257A			−	34	−	−	−	
		TC74HCT258A			−	33	−	−	−	

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4(\text{per bit})$$

8-BIT ADDRESSABLE LATCH

The TC74HC259A is a high speed CMOS ADDRESSABLE LATCH fabricated with silicon gate C^2MOS technology.

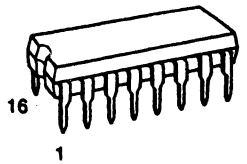
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The respective bits are controlled by address inputs A, B, and C. When $\overline{CLEAR}$ input is held high and enable input G is held low, the data is written into the bit selected by address inputs, the other bits hold their previous conditions. When both $\overline{CLEAR}$ and $\overline{G}$ held high, writing of all bits is inhibited regardless of address inputs, and their previous conditions are held. When $\overline{CLEAR}$ is held low and $\overline{G}$ is held high, all bits are reset to low regardless of the other inputs. When both of $\overline{CLEAR}$ and $\overline{G}$ held low, all bits not selected by address inputs are reset to low.

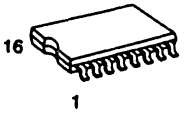
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

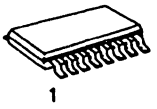
FEATURES:

- High Speed ····· t_{pd}=15ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS259



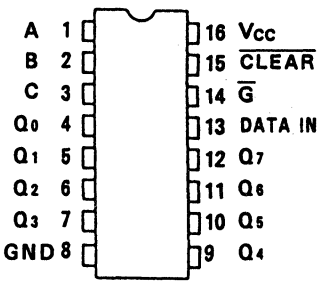
P(DIP16-P-300A)





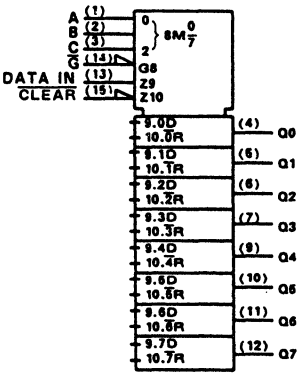
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



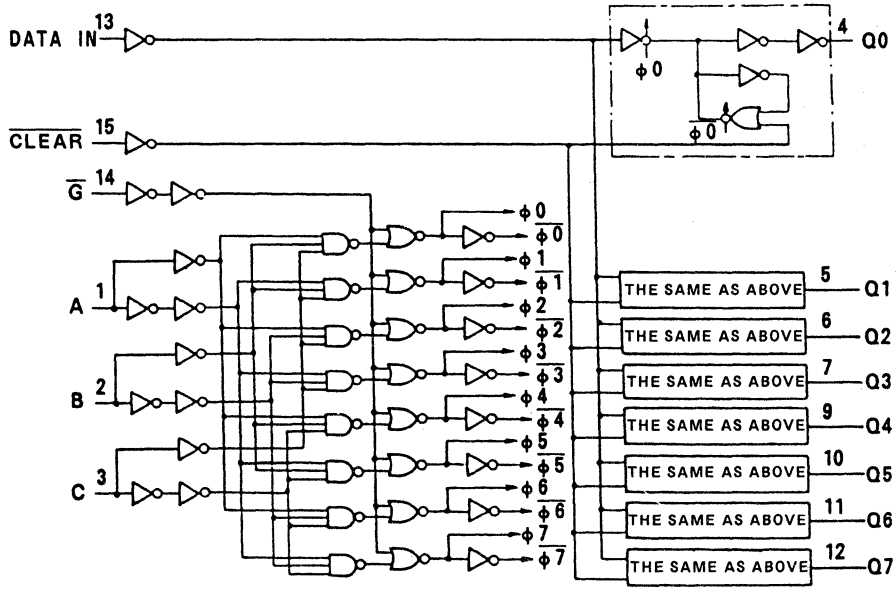
TRUTH TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	QiO	ADDRESSABLE LATCH
H	H	QiO	QiO	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO "L"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : The level at the data input.
QiO : The level before the indicated steady-state input conditions were established (i = 0, 1, ···7)

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{G}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (DATA)	t_s		2.0	−	50	60	
			4.5	−	10	12	
			6.0	−	9	11	
Minimum Set−up Time (A, B, C)	t_s		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time (DATA)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time (A, B, C)	t_h		2.0	−	0	0	MHz
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		−	15	22	
Propagation Delay Time (A, B, C−Q)	t_{pLH} t_{pHL}		−	21	32	
Propagation Delay Time ($\overline{G}$−Q)	t_{pLH} t_{pHL}		−	16	28	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		−	13	23	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Q)	t_{pLH} t_{pHL}		2.0	−	56	130	−	165	
			4.5	−	18	26	−	33	
			6.0	−	15	22	−	28	
Propagation Delay Time (A, B, C−Q)	t_{pLH} t_{pHL}		2.0	−	83	185	−	230	
			4.5	−	25	37	−	46	
			6.0	−	21	31	−	39	
Propagation Delay Time ($\overline{G}$−Q)	t_{pLH} t_{pHL}		2.0	−	67	165	−	205	
			4.5	−	20	33	−	41	
			6.0	−	17	28	−	35	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pHL}		2.0	−	52	135	−	170	
			4.5	−	16	27	−	34	
			6.0	−	14	23	−	29	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)			−	35	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Latch)}$$

TC74HC266AP/AF
TC74HC7266AP/AF

TC74HC266AP/AF QUAD EXCLUSIVE NOR GATE (OPEN DRAIN)
TC74HC7266AP/AF QUAD EXCLUSIVE NOR GATE

The TC74HC266A/7266A are high speed CMOS QUAD EXCLUSIVE NOR GATE fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC266A has a high-performance MOS N-channel transistor (OPEN-DRAIN output).

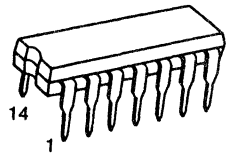
Therefore, with suitable output pullup resistors, this device can be used in wired-AND application.

The TC74HC7266A has an output buffer which is CMOS structure.

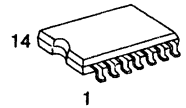
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS266

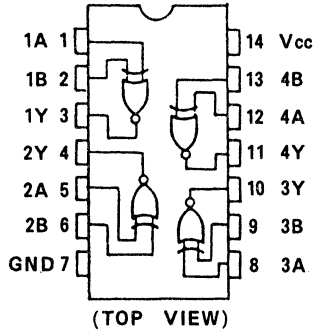


P(DIP14-P-300)



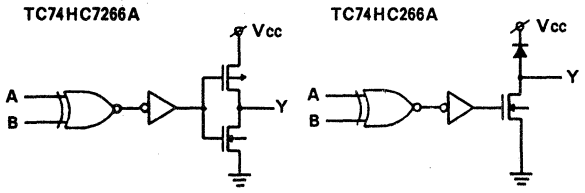
F(SOP14-P-300)

PIN ASSIGNMENT

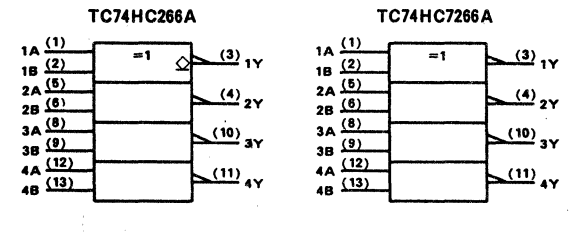


(TOP VIEW)

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y	
		7266A	266A
L	L	H	Z
L	H	L	L
H	L	L	L
H	H	H	Z

Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL} (TC74HC7266A)	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} (TC74HC266A)		5.5	−	−	±0.5	−	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time *	t_{pLH} t_{pHL}		–	10	17	
Propagation Delay Time **	t_{pLZ}	R_L=1kΩ	–	11	17	
Propagation Delay Time **	t_{pZL}	R_L=1kΩ	–	10	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time **	t_{pLZ}	R_L=1kΩ	2.0	–	26	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	11	17	–	21	
Propagation Delay Time **	t_{pZL}	R_L=1kΩ	2.0	–	40	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Output Capacitance	C_{OUT}			–	3	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC266A		–	16	–	–	–	
		TC74HC7266A		–	30	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

* for TC74HC7266A only
** for TC74HC266A only

OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74HC273A is a high speed CMOS OCTAL D TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

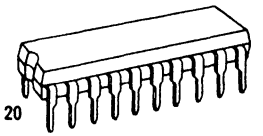
Information signals applied to D inputs are transfered to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held "L", the Q outputs are at a low logic level independent of the other inputs.

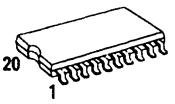
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

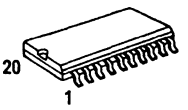
FEATURES:

- High Speed ····· f_{MAX}=48MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS273



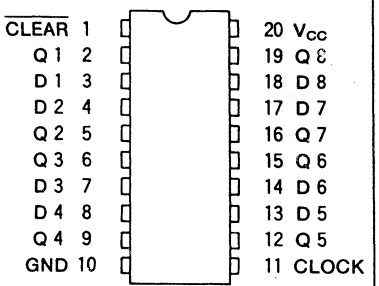
P(DIP20-P-300A)





F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT



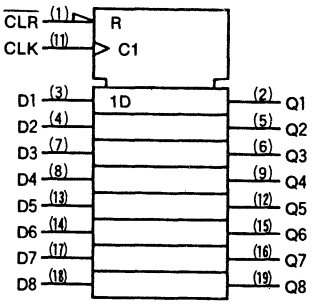
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No change

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		−	16	27	
Maximum Clock Frequency	f_{MAX}		40	67	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	25	75	−	95	ns
			4.5	−	7	15	−	19	
			6.0	−	6	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	54	145	−	180	
			4.5	−	18	29	−	36	
			6.0	−	15	25	−	31	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		2.0	−	60	160	−	200	
			4.5	−	20	32	−	40	
			6.0	−	17	27	−	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	18	−	5	−	MHz
			4.5	30	56	−	24	−	
			6.0	35	66	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	43	−	−	−	

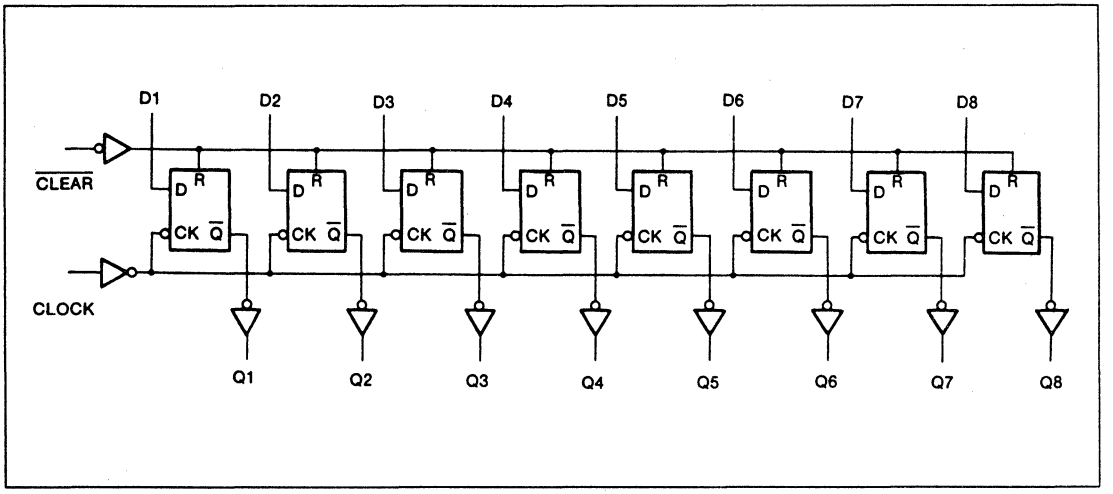
C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=32+11 \cdot n$$

SYSTEM DIAGRAM



OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74HCT273A is a high speed CMOS OCTAL D TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

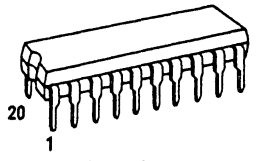
Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q outputs are at a low logic level independent of the other inputs.

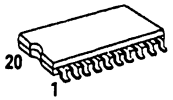
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

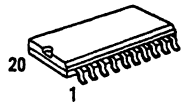
FEATURES:

- High Speed ····· f_{MAX}=76MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH} =2V(Min.)
  V_{IL} =0.8V(Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS273



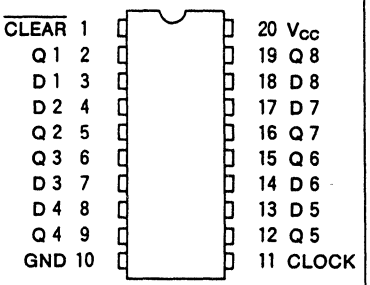
P(DIP20-P-300A)





F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT



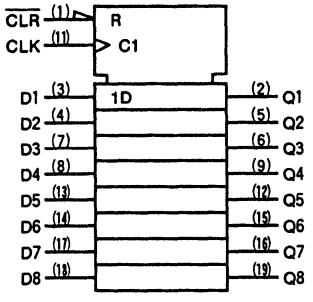
(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No change

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH}=−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH}=−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL}=20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL}=6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Curren	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{cc}	PER INPUT: V_{IN} = 0.5V or 2.4V, OTHER INPUT: V_{IN} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{W(L)}$		4.5	−	15	19	
			5.5	−	14	17	
Minimum Set−up Time	t_s		4.5	−	10	13	
			5.5	−	10	13	
Minimum Hold Time	t_h		4.5	−	5	6	
			5.5	−	10	13	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		4.5	−	10	13	
			5.5	−	9	12	
Clock Frequency	f		4.5	−	30	24	MHz
			5.5	−	35	28	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	15	25	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		−	18	28	
Maximum Clock Frequency	f_{MAX}		40	90	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	−	9	15	−	19	ns
			5.5	−	8	14	−	18	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		4.5	−	19	30	−	38	
			5.5	−	17	27	−	34	
Propagation Delay Time ($\overline{CLEAR}$−Q)	t_{pLH} t_{pHL}		4.5	−	22	32	−	40	
			5.5	−	18	29	−	36	
Maximum Clock Frequency	f_{MAX}		4.5	30	71	−	24	−	MHz
			5.5	35	81	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	29	−	−	−	

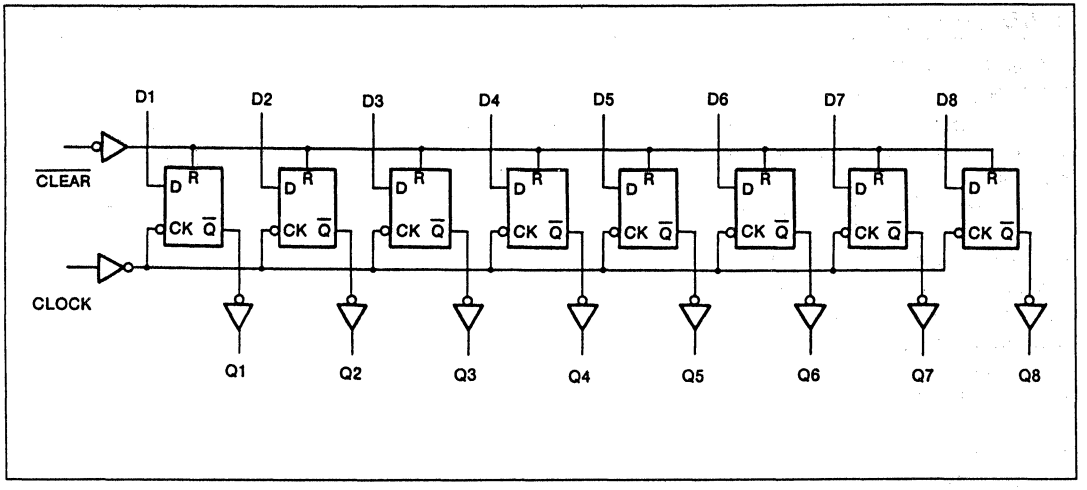
Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}/8 \text{(per Flip Flop)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=18+11 \cdot n$$

SYSTEM DIAGRAM



QUAD $\overline{S}$–$\overline{R}$ LATCH

The TC74HC279A is a high speed CMOS QUAD S–R LATCH fabricated with silicon gate C^2MOS technology.

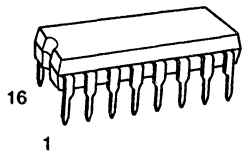
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Each latch has an independent Q output and Set and Reset inputs. $\overline{S}$ and $\overline{R}$ are active low. When $\overline{S}$ input is low, the Q output goes high and when $\overline{R}$ input is low, the Q output goes low. When both $\overline{S}$ and $\overline{R}$ are low, $\overline{S}$ takes precedence resulting Q=low. When both of $\overline{S}$ and $\overline{R}$ are held high,Q output doesn't change.

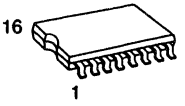
All inputs are equipped with protection circuits against static discharge or trasient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=12ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS279

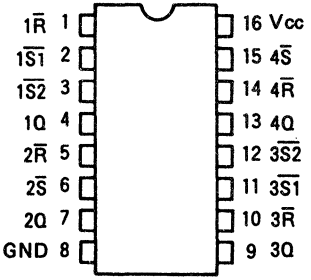


P(DIP16–P–300A)



F(SOP16–P–300)

PIN ASSIGNMENT

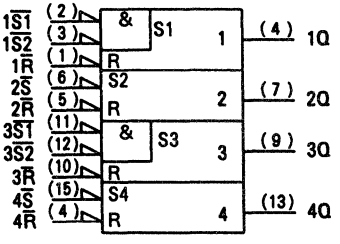


TRUTH TABLE

INPUT		OUTPUT
$\overline{S}$#	$\overline{R}$	Q
H	H	Qn
L	H	H
H	L	L
L	L	H

NOTE:
Qn ---The level of Q before the indicated input condition were established.
# ---For latches with doble $\overline{S}$ input.
H=Both $\overline{S}$ input high
L=One of both inputs low

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, Vcc=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{S1}$,$\overline{S2}$–Q)	t_{pLH} t_{pHL}		–	12	22	
Propagation Delay Time ($\overline{S}$–Q)	t_{pLH} t_{pHL}		–	9	17	
Propagation Delay Time ($\overline{R}$–Q)	t_{pLH} t_{pHL}		–	11	20	

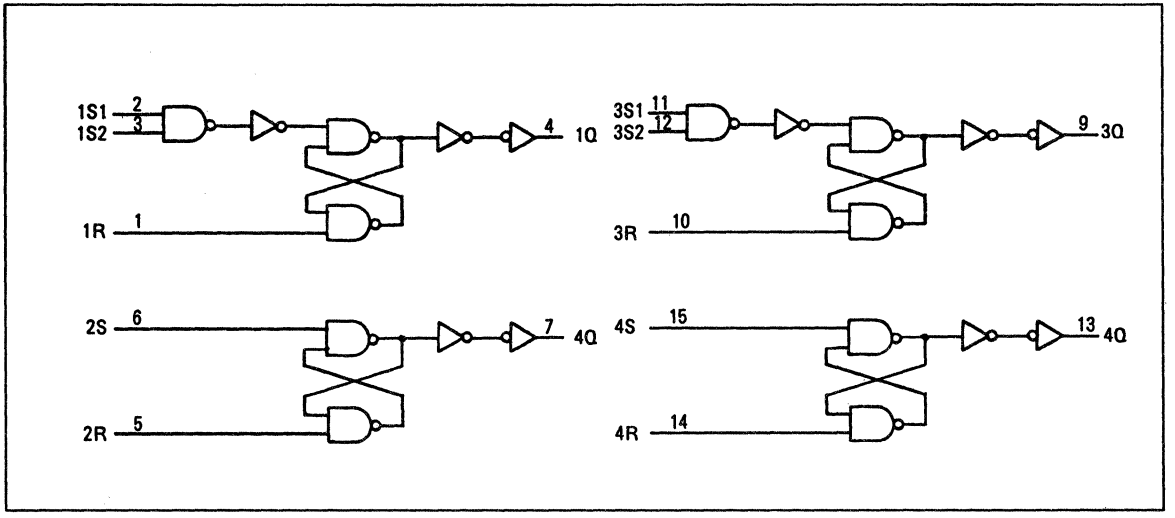
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{S1}$,$\overline{S2}$–Q)	t_{pLH} t_{pHL}		2.0	–	45	130	–	165	
			4.5	–	15	26	–	33	
			6.0	–	13	22	–	28	
Propagation Delay Time ($\overline{S}$–Q)	t_{pLH} t_{pHL}		2.0	–	38	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Propagation Delay Time ($\overline{R}$–Q)	t_{pLH} t_{pHL}		2.0	–	42	120	–	150	
			4.5	–	14	24	–	30	
			6.0	–	12	20	–	26	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	18	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per circuit)}$$

SYSTEM DIAGRAM



8-CHANNEL MULTIPLEXER

The TC74HC280A is a high speed CMOS 9-BIT PARITY GENERATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC280A is composed of nine data inputs A thru I and odd/even parity outputs ΣODD and ΣEVEN.

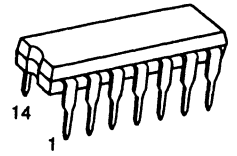
The odd parity output is high when an odd number of data inputs are high. The even parity output is high when an even number of data inputs are high.

The word-length capability is easily expanded by cascading.

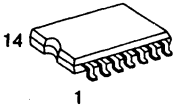
All inputs are equipped with protection circuits aainst static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=22ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS280

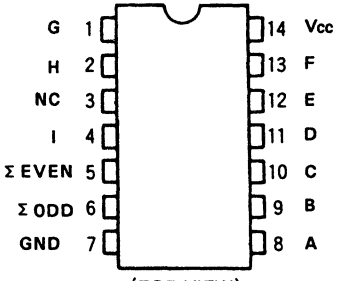


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT

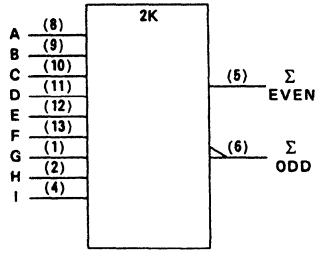


(TOP VIEW)
NC : No Connection

TRUTH TABLE

Number of inputs A through I that are High	Outputs	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	22	35	ns

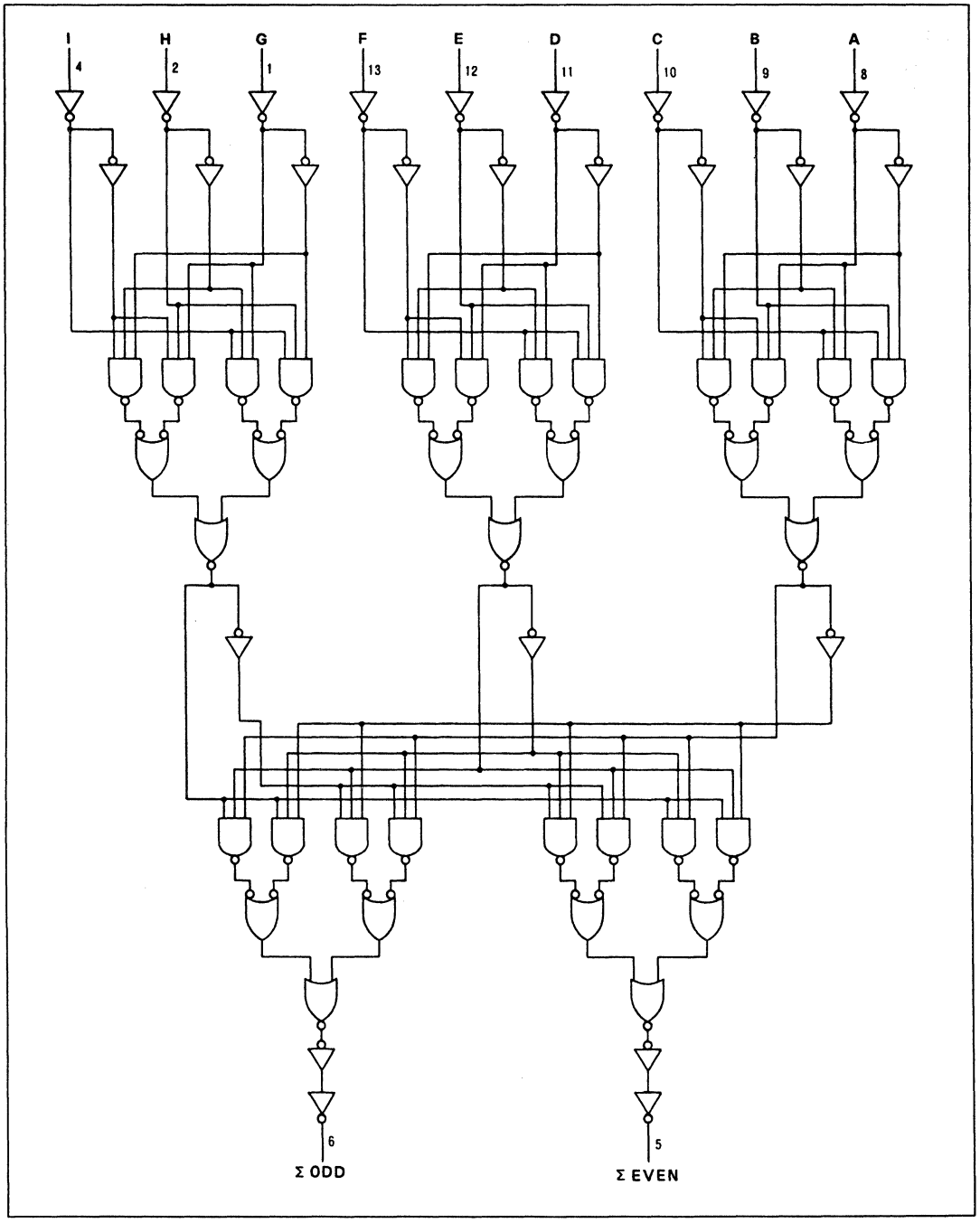
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	80	200	–	250	
			4.5	–	26	40	–	50	
			6.0	–	22	34	–	43	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	61	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SYSTEM DIAGRAM



4-BIT BINARY FULL ADDER

The TC74HC283A is a high speed CMOS 4-BIT BINARY FULL ADDER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit.

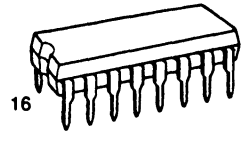
This adder features full internal look-ahead across all four bits.

A 4 × n bit binary adder is easily built up by cascading the HC283A without any additional logic.

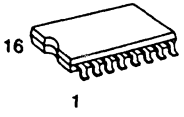
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

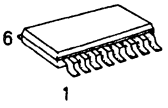
FEATURES:

- High Speed ····· t_{pd}=17ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS283



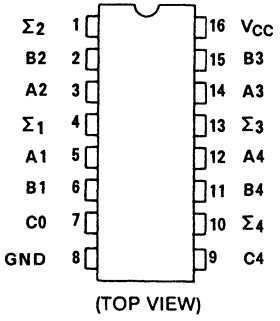
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT

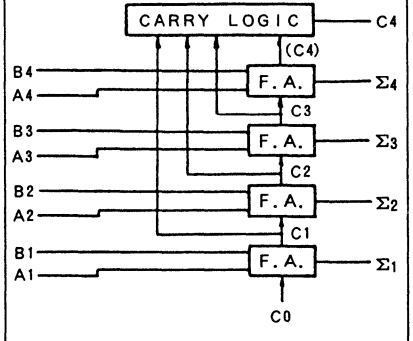


(TOP VIEW)

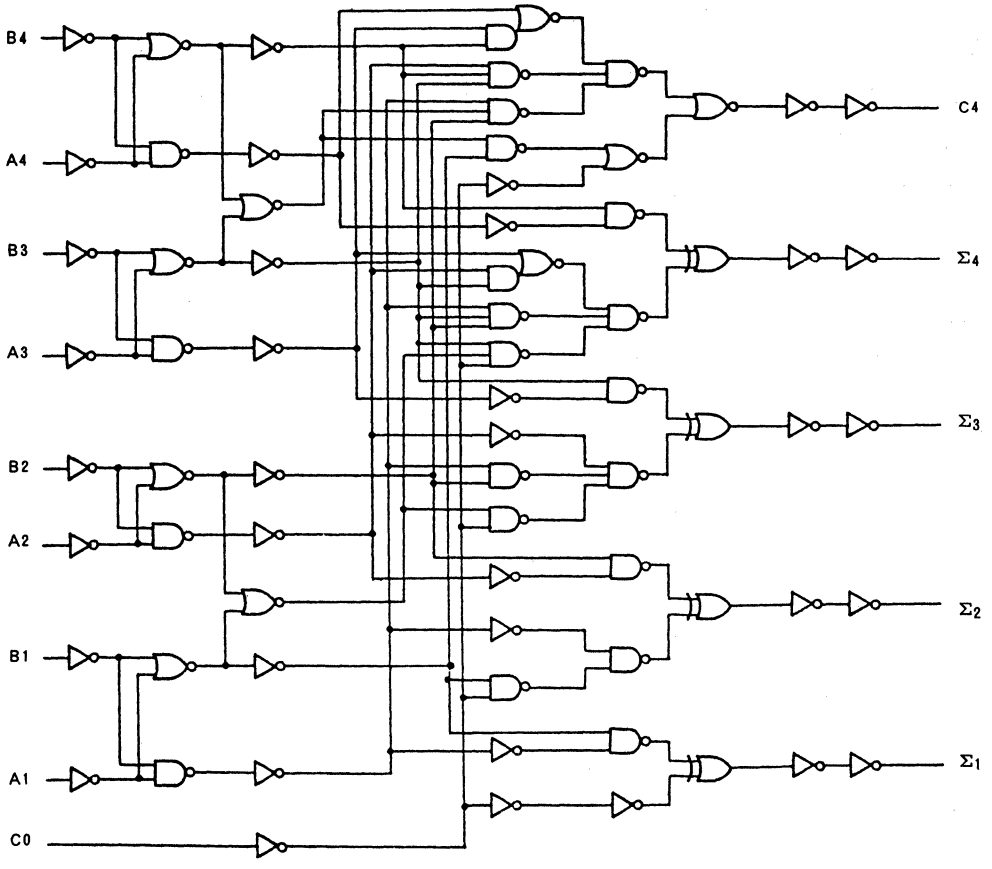
TRUTH TABLE(1 bit)

INPUTS			OUTPUTS	
Bn	An	cn−1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

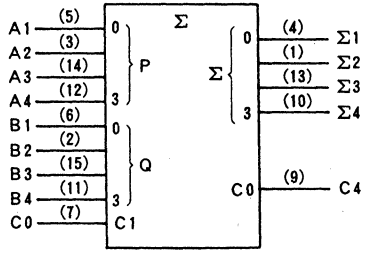
BLOCK DIAGRAM



SYSTEM DIAGRAM



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($C_0-\sum n$)	t_{pLH} t_{pHL}		–	17	26	
Propagation Delay Time (C_0-C_4)	t_{pLH} t_{pHL}		–	17	26	
Propagation Delay Time (An,Bn−$\sum n$)	t_{pLH} t_{pHL}		–	23	37	
Propagation Delay Time (An,Bn−C_4)	t_{pLH} t_{pHL}		–	21	34	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($C_0-\sum n$)	t_{pLH} t_{pHL}		2.0	–	60	150	–	190	
			4.5	–	20	30	–	38	
			6.0	–	17	26	–	32	
Propagation Delay Time (C_0-C_4)	t_{pLH} t_{pHL}		2.0	–	60	150	–	190	
			4.5	–	20	30	–	38	
			6.0	–	17	26	–	32	
Propagation Delay Time (An,Bn−$\sum n$)	t_{pLH} t_{pHL}		2.0	–	95	210	–	265	
			4.5	–	27	42	–	53	
			6.0	–	22	36	–	45	
Propagation Delay Time (An,Bn−C_4)	t_{pLH} t_{pHL}		2.0	–	80	195	–	245	
			4.5	–	25	39	–	49	
			6.0	–	20	33	–	42	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	126	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

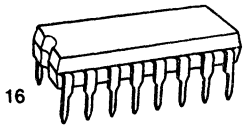
QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

The TC74HC298A is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

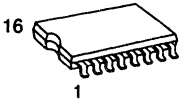
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains a 4-bit 2-channel multiplexer and a 4-bit output register. When the word select input (W.S.) is held low, the data of word 1(A1,B1,C1,D1)is selected and is applied to the registers. When W.S. is held high, the data of word 2(A2,B2,C2,D2)will be applied to the registers. This selected data is transferred to the output(QA,QB, QC,QD)on the negative going transition of $\overline{CLOCK}$.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.



P(DIP16-P-300A)

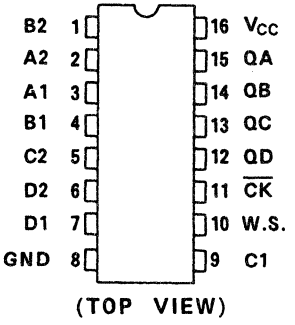


F(SOP16-P-300)

FEATURES:

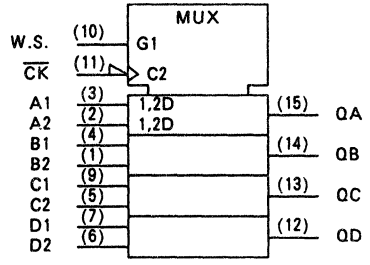
- High Speed ····· f_{MAX}=73MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS298

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

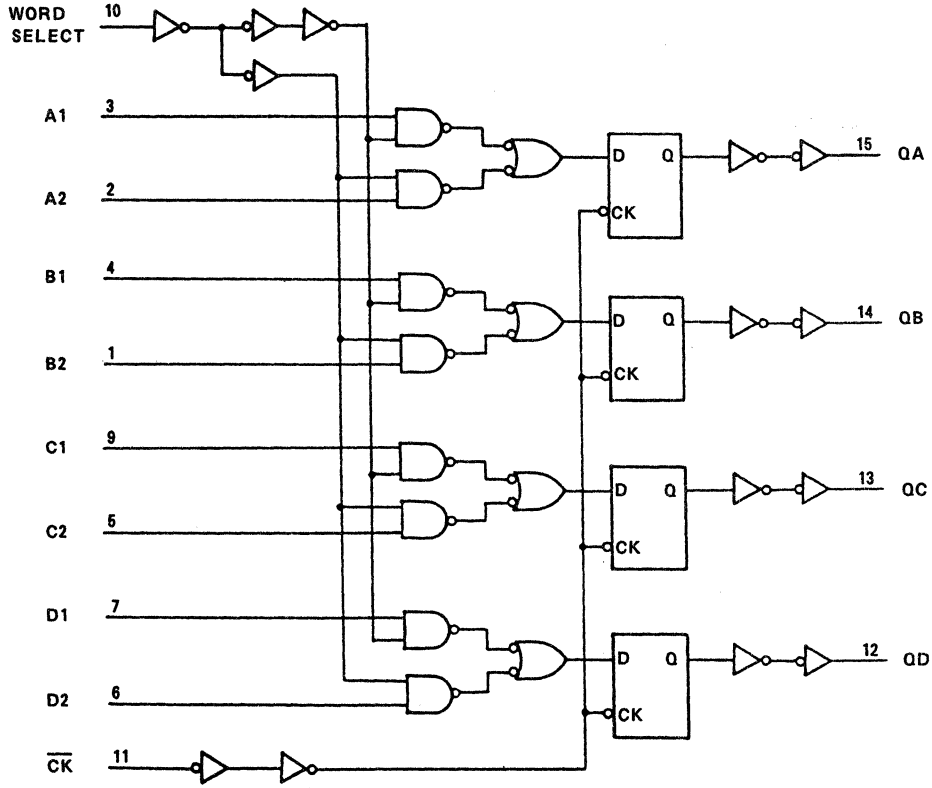


TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CK}$	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QD0	QD0

X : Don't care (Including transition)
a1, a2····· : The Level of steady-state Input at A1, A2, etc.
QA0, QB0··· : The level of QA, QB, etc. entered on the most recent negative transition of the clock input.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (A, B, C, D)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (W. S.)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (A, B, C, D)	t_h		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Minimum Hold Time (W. S.)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	35	27	
			6.0	−	41	33	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		−	12	21	
Maximum Clock Frequency	f_{MAX}		38	73	−	

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CK}$−Q)	t_{pLH} t_{pHL}		2.0	−	45	125	−	155	
			4.5	−	15	25	−	31	
			6.0	−	13	21	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	7	22	−	6	−	
			4.5	35	67	−	28	−	
			6.0	41	79	−	33	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	39	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per bit)}$$

And the total C_{PD} when n−bits operate can be gained by the following equation:

$$C_{PD}\text{ (total)}=27+12 \cdot n$$

TC74HC299AP/AF
TC74HC323AP/AF

TC74HC299AP/AF 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR
TC74HC323AP/AF 8-BIT PIPO SHIFT REGISTER WITH SYNCHRONOUS CLEAR

The TC74HC299A and TC74HC323A are high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

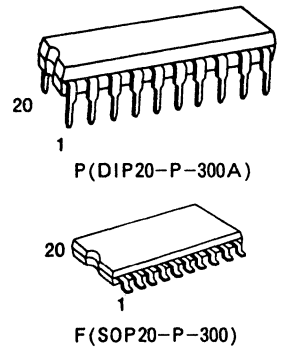
They have four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected. Clear function on the TC74HC299A is asynchronous to CLOCK, while the TC74HC323A is cleared synchronous to CLOCK.

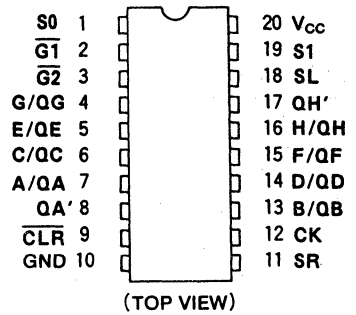
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

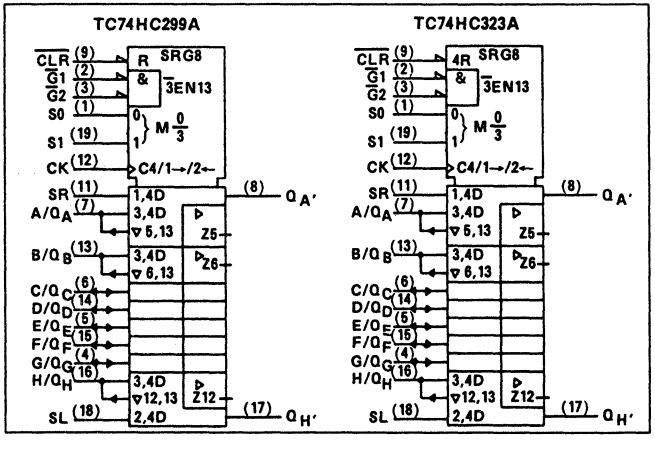
- High Speed ····· f_{MAX}=42MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For QA',QH'
- Symmetrical Output Impedance ···
  $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QA', QH'
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS299/323



PIN ASSIGNMENT



IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

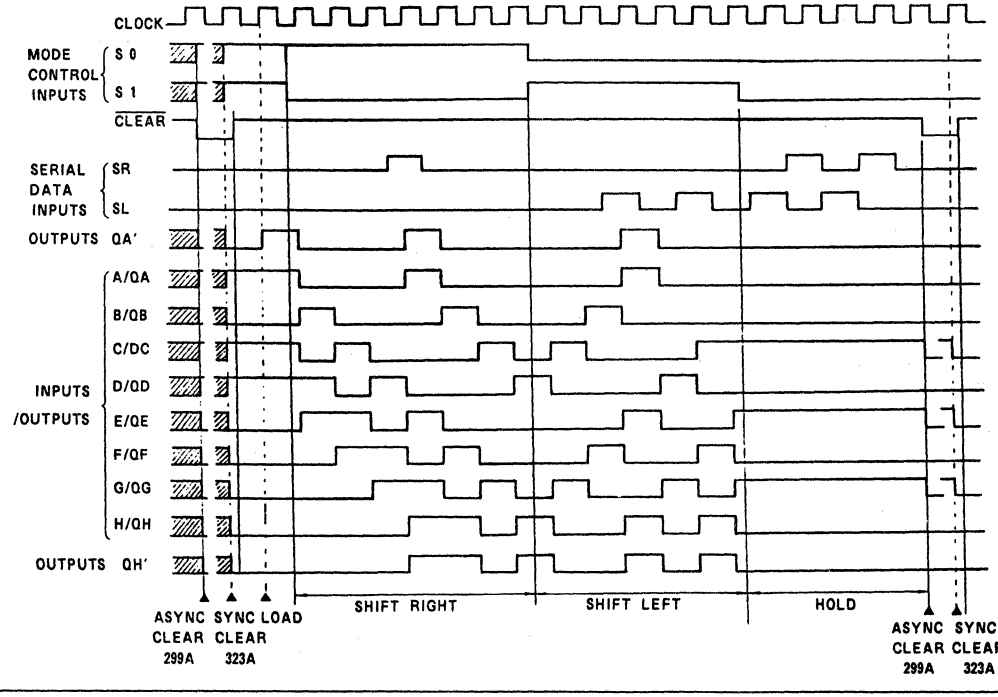
TRUTH TABLE

MODE	INPUTS									INPUTS/OUTPUTS		OUTPUTS	
	$\overline{CLR}$	FUNCTION SELECT		OUTPUT CONTROL		CK		SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *	(299A)	(323A)	SL	SR				
Z	L	H	H	X	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	↓	X	X	L	L	L	L
	L	X	L	L	L	X	↓	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓		X	H	H	QGn	H	QGn
	H	L	H	L	L	↓		X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓		H	X	QBn	H	QBn	H
	H	H	L	L	L	↓		L	X	QBn	I	QBn	L
LOAD	H	H	H	X	X	↓		X	X	a	h	a	h

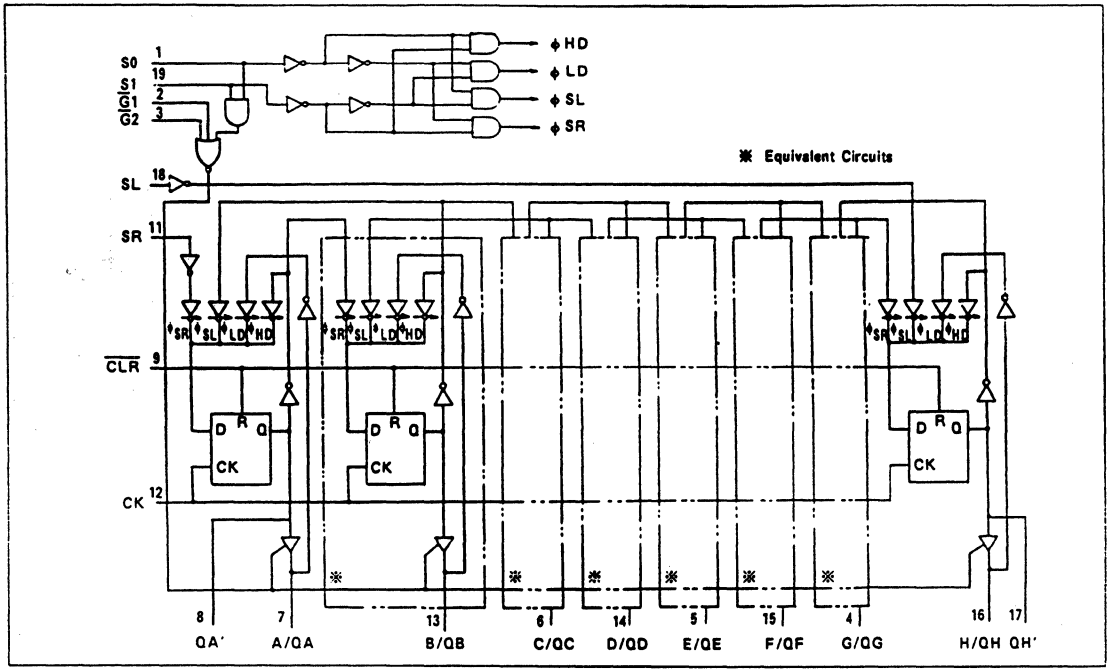
* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z :High Impedance
Qn0:The level of An before the indicated steady-state input conditions were established.
Qnn:The level of Qn before the most recent active transition indicated by ↓ or ↑.
a,h :The level of the steady-state inputs A, H, respectively.
X :Don't care

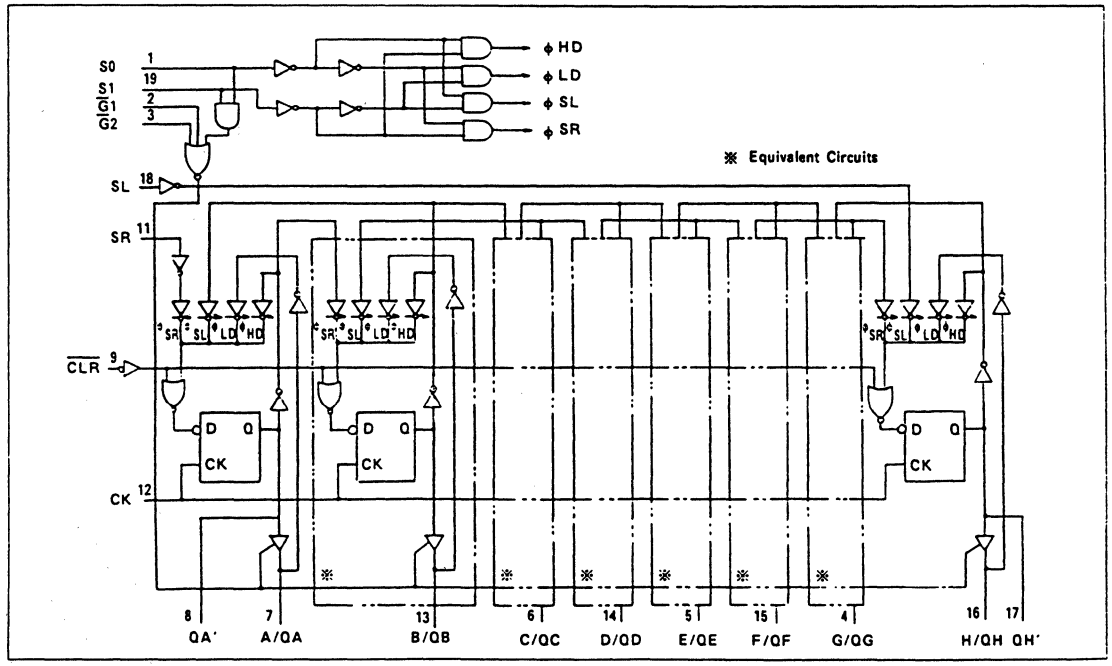
TIMING CHART



SYSTEM DIAGRAM(TC74HC299A)



SYSTEM DIAGRAM(TC74HC323A)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (Q_H') / (Q_A ~ Q_H)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		Q_A', Q_H'	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_A~Q_H	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		Q_A', Q_H'	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_A~Q_H	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING RECOMMENDED OPERATING CONDITIONS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CLR}$)*	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SL,SR,A~H)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (S0,S1)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time ($\overline{CLR}$)**	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (SL,SR,A~H)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (S0,S1)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time ($\overline{CLR}$)**	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CLR}$)*	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	8	10	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	23	

Note :* TC74HC299A only

** TC74HC323A only

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (QA',QH')	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CK−QA',QH')	t_{pLH} t_{pHL}		−	19	30	
Propagation Delay Time ($\overline{CLR}$−QA',QH')	t_{pLH} t_{pHL}		−	17	30	
Maximum Clock Frequency	f_{MAX}		35	73	−	MHz

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time (QA~QH)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (QA',QH')	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CK-QA'QH')	t_{pLH} t_{pHL}		50	2.0	−	85	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	18	29	−	37	
Propagation Delay Time ($\overline{CLR}$-QA',QH')**	t_{pHL}		50	2.0	−	85	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	18	30	−	37	
Propagation Delay Time (CK-QA~QH)	t_{pLH} t_{pHL}		50	2.0	−	80	160	−	20	
				4.5	−	21	32	−	40	
				6.0	−	17	27	−	34	
			150	2.0	−	100	200	−	250	
				4.5	−	26	40	−	50	
				6.0	−	21	34	−	43	
Propagation Delay Time ($\overline{CLR}$-QA~QH)**	t_{pHL}		50	2.0	−	85	190	−	240	
				4.5	−	24	38	−	48	
				6.0	−	18	30	−	38	
			150	2.0	−	105	230	−	90	
				4.5	−	29	46	−	58	
				6.0	−	22	36	−	46	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	60	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	13	22	−	28	
			150	2.0	−	78	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	17	29	−	36	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	54	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	33	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	12	−	5	−	MHz
				4.5	30	58	−	24	−	
				6.0	35	80	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	170	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_N + I_{CC}$$

* TC74HC299A only

** TC74HC323A only

TC74HC352AP/AF
TC74HC353AP/AF

TC74HC352AP/AF DUAL 4-CHANNEL MULTIPLEXER
TC74HC353AP/AF DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74HC352A and TC74HC353A are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC352A is an inverted output version of the TC74HC153A (normal outputs), and the TC74HC353A is an inverted output version of TC74HC253A (3-state outputs).

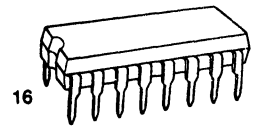
Input data (1C0~1C3, 2C0~2C3) are selected by the two address inputs A and B.

Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections. They can be used to inhibit the data outputs: The output of HC352A is set low, and the HC353A output set is to the high impedance state, when the strobe input is held low.

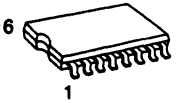
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=12ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS352,74LS353

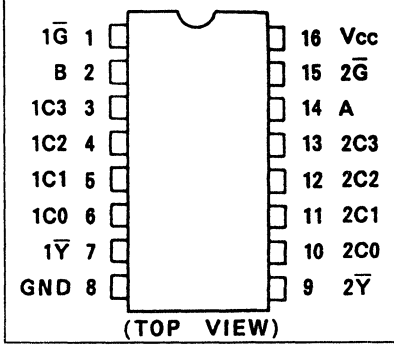


P(DIP16-P-300A)

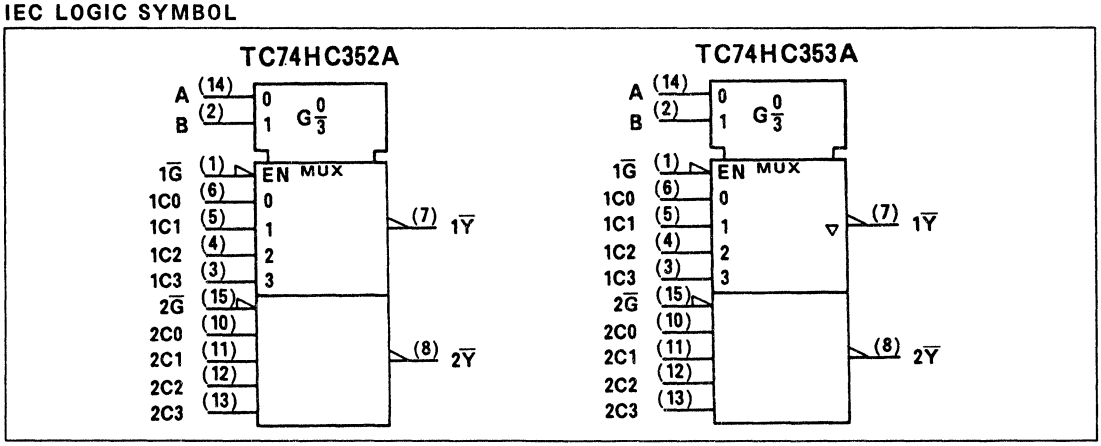


F(SOP16-P-300)

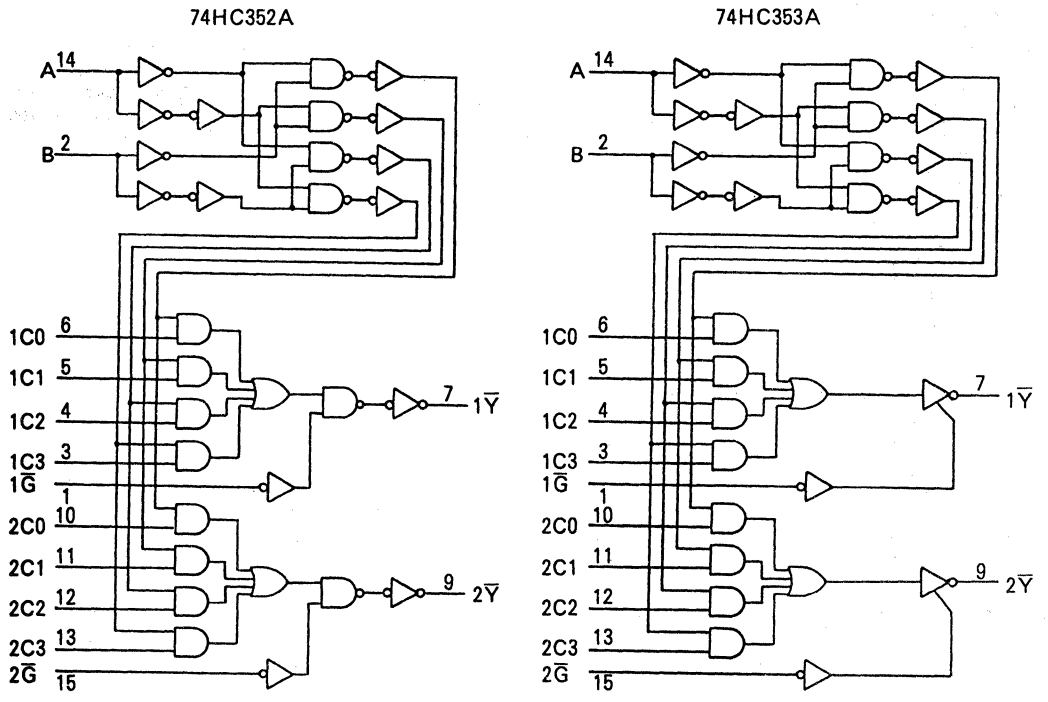
PIN ASSIGNMENT



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TRUTH TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C0	C1	C2	C3	G	HC352A	HC353A
X	X	X	X	X	X	H	H	Z
L	L	L	X	X	X	L	H	H
L	L	H	X	X	X	L	L	L
L	H	X	L	X	X	L	H	H
L	H	X	H	X	X	L	L	L
H	L	X	X	L	X	L	H	H
H	L	X	X	H	X	L	L	L
H	H	X	X	X	L	L	H	H
H	H	X	X	X	H	L	L	L

X : Don't care
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ} *	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

* for TC74HC353A only

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (Cn–$\overline{Y}$)	t_{pLH} t_{pHL}		–	12	19	
Propagation Delay Time (A,B–$\overline{Y}$)	t_{pLH} t_{pHL}		–	18	29	
Propagation Delay Time ($\overline{G}$–$\overline{Y}$) *	t_{pLH} t_{pHL}		–	9	16	
3-State Output Disable Time ($\overline{G}$–$\overline{Y}$) **	t_{pLZ} t_{pHZ}		–	9	16	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=–40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (Cn–$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	48	115	–	145	
			4.5	–	15	23	–	29	
			6.0	–	12	20	–	25	
Propagation Delay Time (A,B–$\overline{Y}$)	t_{pLH} t_{pHL}		2.0	–	72	170	–	215	
			4.5	–	22	34	–	43	
			6.0	–	18	29	–	37	
Propagation Delay Time ($\overline{G}$–$\overline{Y}$) *	t_{pLH} t_{pHL}		2.0	–	36	95	–	120	
			4.5	–	12	19	–	24	
			6.0	–	9	16	–	20	
3-State Output Enable Time ($\overline{G}$–$\overline{Y}$) **	t_{pZL} t_{pZH}		2.0	–	36	100	–	125	
			4.5	–	12	20	–	25	
			6.0	–	9	17	–	21	
3-State Output Disable Time ($\overline{G}$–$\overline{Y}$) **	t_{pLZ} t_{pHZ}		2.0	–	22	115	–	145	
			4.5	–	13	23	–	29	
			6.0	–	11	20	–	25	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)	TC74HC352A		–	63	–	–	–	
		TC74HC353A		–	62	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

* for TC74HC352A only
** for TC74HC353A only

TC74HC354AP/AF

8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

The TC74HC354A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains an 8 channel digital multiplexer with an 8-bit input data register(D0~D7), a 3-bit address input register(S0~S2)and 3-state outputs.

Data from one of the eight inputs will be shifted onto the Y output (non-inverted)and the W output (inverted) pins as determined by the address data.

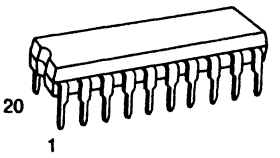
Its outputs go into a high-impedance state when either $\overline{G1}$ or G2 is held high or G3 is held low.

In the TC74HC354A, the data enable input ($\overline{DC}$) controls transparent latches that pass data to the outputs when $\overline{DC}$ is high, and latchs in new data when $\overline{DC}$ is low.

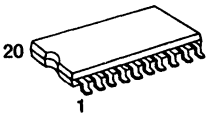
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=24ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS354

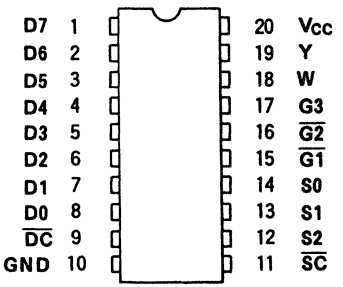


P(DIP20-P-300A)



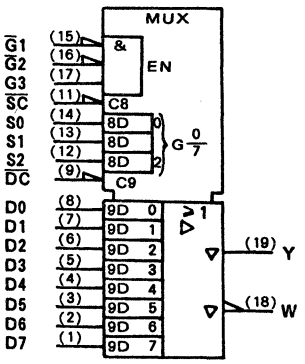
F(SOP20-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

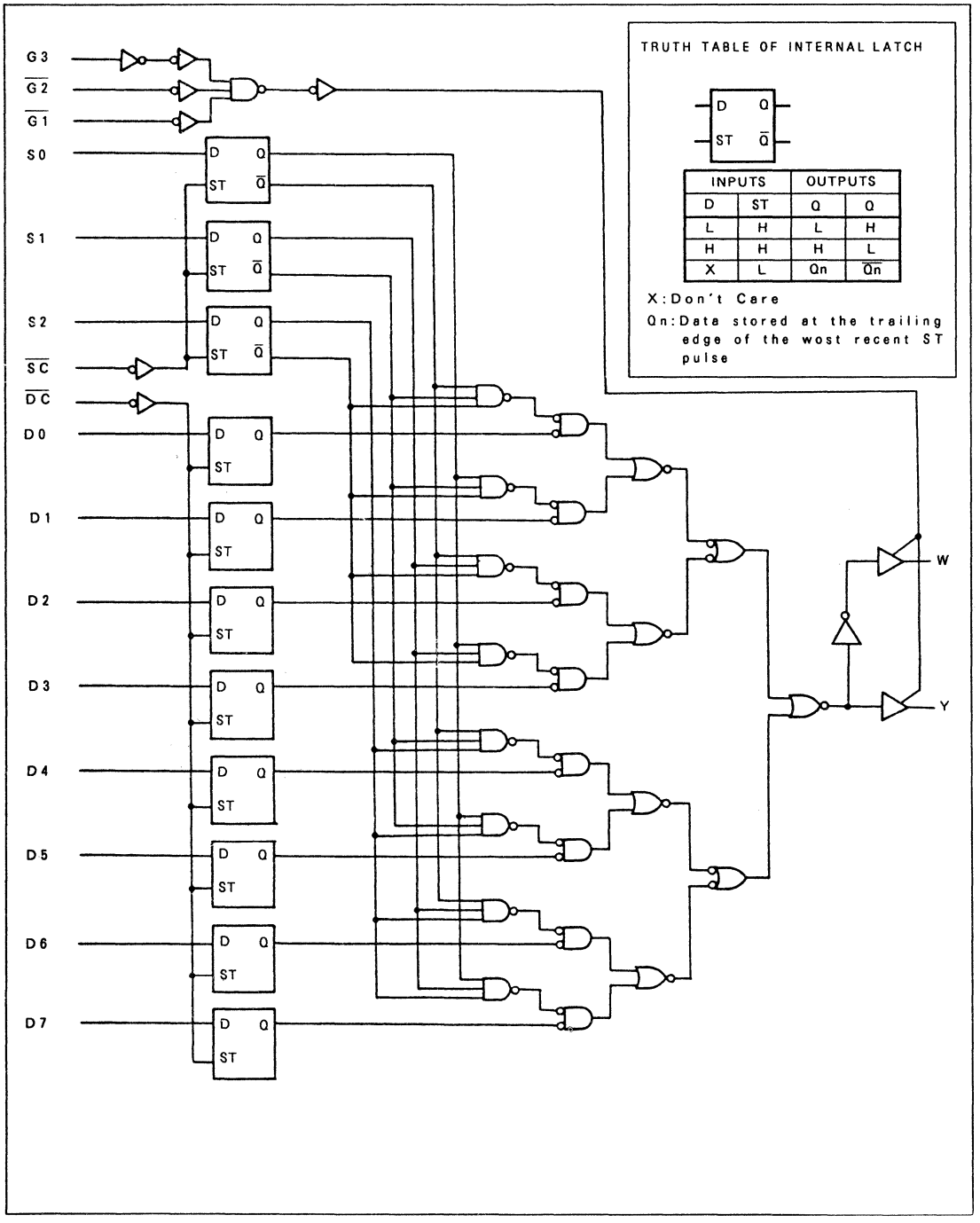


TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #			$\overline{DC}$	OUTPUT ENABLES			W	Y
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X:Don't care
Z:High Impedance
D0n……D7n:The level of steady-state inputs at input D0 through D7, respectively, before the most recent"L"to"H"transistor ofdata control.
#:This columu shows the input address setup with $\overline{SC}$ low.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃				Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃		Ta=−40∼85℃	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{DC}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (Dn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set-up Time (Sn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Dn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Hold Time (Sn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	Vcc	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	11	−	13	
Propagation Delay Time (Dn−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	83	210	−	265	
				4.5	−	26	42	−	53	
				6.0	−	21	36	−	45	
			150	2.0	−	99	250	−	315	
				4.5	−	31	50	−	63	
				6.0	−	25	43	−	54	
Propagation Delay Time ($\overline{DC}$−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	83	210	−	265	
				4.5	−	26	42	−	53	
				6.0	−	21	36	−	45	
			150	2.0	−	99	250	−	315	
				4.5	−	31	50	−	63	
				6.0	−	25	43	−	54	
Propagation Delay Time (Sn−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	98	260	−	325	
				4.5	−	30	52	−	65	
				6.0	−	25	44	−	55	
			150	2.0	−	114	300	−	375	
				4.5	−	35	60	−	75	
				6.0	−	29	51	−	64	
Propagation Delay Time ($\overline{SC}$−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	102	270	−	340	
				4.5	−	31	54	−	68	
				6.0	−	27	46	−	58	
			150	2.0	−	118	310	−	390	
				4.5	−	36	62	−	78	
				6.0	−	31	53	−	66	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	44	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
			150	2.0	−	60	165	−	205	
				4.5	−	19	33	−	41	
				6.0	−	16	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	42	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	17	26	−	33	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD(1)}$				−	77	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC356AP/AF

8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

The TC74HC356A is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device contains an 8 channel digital multiplexer with an 8-bit input data register(D0~D7), a 3-bit address input register(S0~S2)and 3-state outputs.

Data from one of the eight inputs will be shifted onto the Y output (non-inverted)and the W output (inverted) pins as determined by the address data.

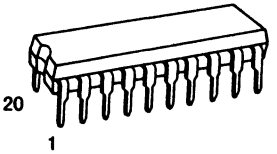
Its outputs go into a high-impedance state when either $\overline{G1}$ or $\overline{G2}$ is held high or G3 is held low.

In the TC74HC356A, the data is stored into the 8-bit flip-flop at the positive going transition of the clock input (CLOCK).

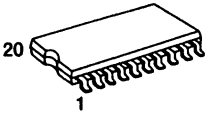
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=25ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS356

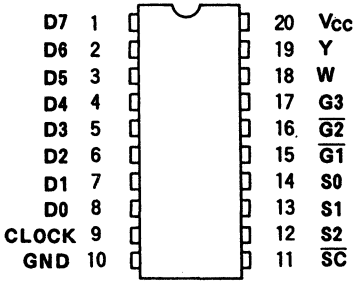


P(DIP20-P-300A)



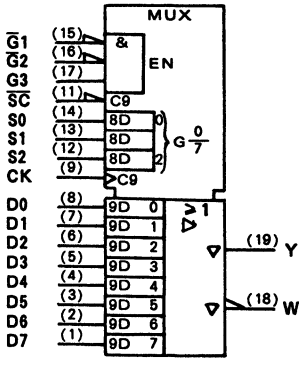
F(SOP20-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

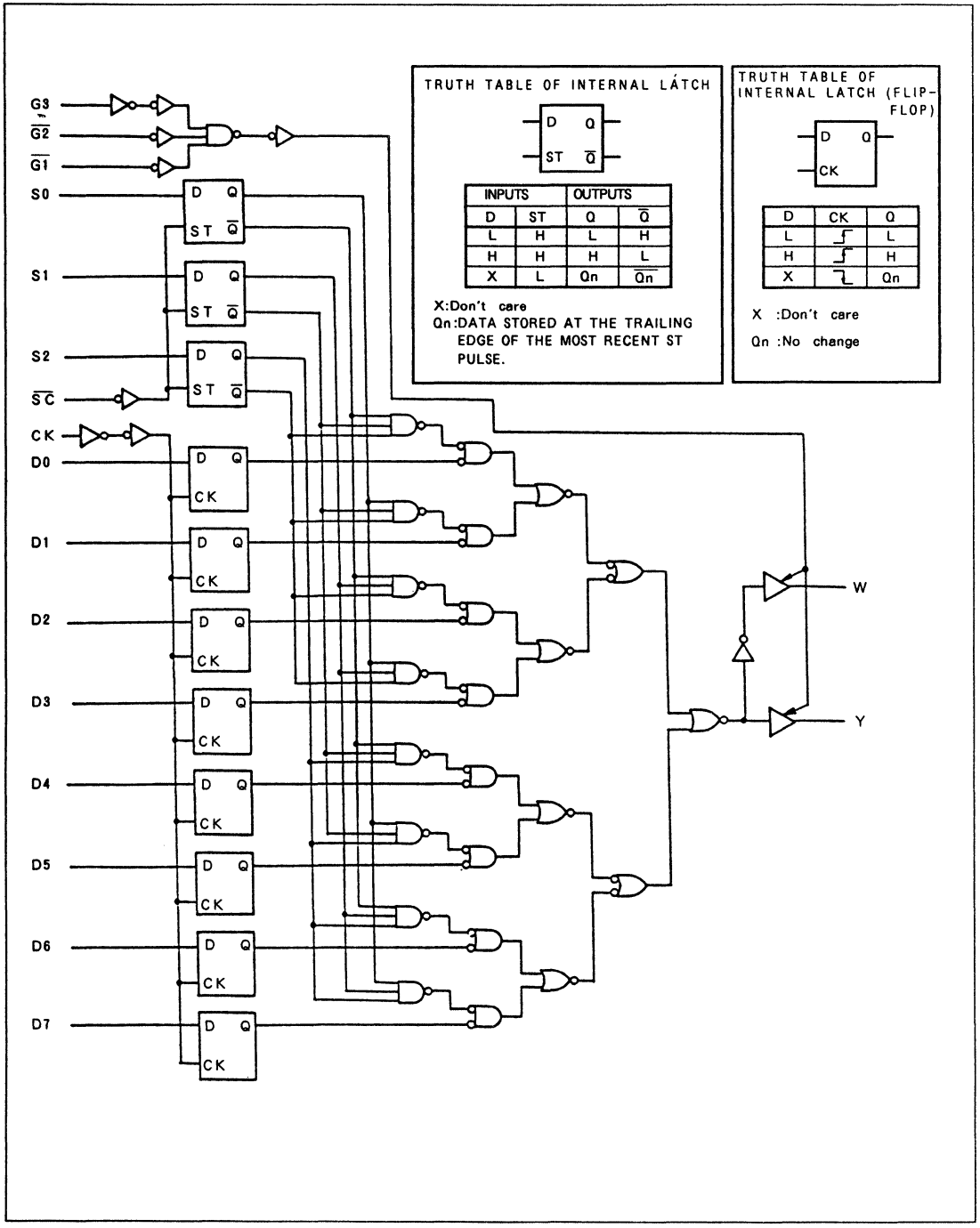


TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #			CLOCK	OUTPUT ENABLES			W	Y
S2	S1	S0		$\overline{G1}$	$\overline{G2}$	G3		
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	↓	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	↓	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	↓	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	↓	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	↓	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	↓	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	↓	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	↓	L	L	H	$\overline{D7n}$	D7n

X:Don't care
Z:High Impedance
D0n·····D7:The level of steady-state inputs at inputs D0 through D7, respectively, before the most recent "L" to "H" transition of data control.
#:This column shows the input address setup with $\overline{SC}$ low.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃		Ta=−40~85℃	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (Dn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set-up Time (Sn)	t_S		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Dn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Hold Time (Sn)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	24	
			6.0	−	36	28	

AC ELECTRICAL CHARCTERISTICS (Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	11	−	13	
Propagation Delay Time (CLOCK−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	99	240	−	300	
				4.5	−	28	48	−	60	
				6.0	−	22	41	−	51	
			150	2.0	−	117	280	−	350	
				4.5	−	33	56	−	70	
				6.0	−	26	48	−	60	
Propagation Delay Time (Sn−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	111	260	−	325	
				4.5	−	32	52	−	65	
				6.0	−	24	44	−	55	
			150	2.0	−	128	300	−	375	
				4.5	−	37	60	−	75	
				6.0	−	28	51	−	64	
Propagation Delay Time ($\overline{SC}$−Y,W)	t_{pLH} t_{pHL}		50	2.0	−	115	270	−	340	
				4.5	−	33	54	−	68	
				6.0	−	25	46	−	58	
			150	2.0	−	132	310	−	390	
				4.5	−	38	62	−	78	
				6.0	−	29	53	−	66	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	11	21	−	26	
			150	2.0	−	65	165	−	205	
				4.5	−	19	33	−	41	
				6.0	−	15	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	43	155	−	195	
				4.5	−	18	31	−	39	
				6.0	−	16	26	−	33	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	20	−	5	−	
				4.5	31	80	−	24	−	
				6.0	36	32	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD(1)}$				−	59	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC365AP/AF
TC74HC366AP/AF

HEX BUS BUFFER
TC74HC365AP/AF NON-INVERTED
TC74HC366AP/AF INVERTED

The TC74HC365A and TC74HC366A are high speed CMOS 3-STATE BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

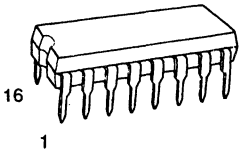
The TC74HC365A is an inverting type, while the TC74HC366A is non-inverting.

All six buffers are controlled by the combination of two enable inputs ($\overline{G}1$ and $\overline{G}2$); the outputs of these buffers are enabled only when both $\overline{G}1$ and $\overline{G}2$ inputs held low, and at the other combinations, these outputs are disabled to the high impedance state.

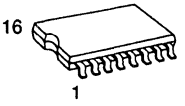
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=9ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Open Drain Structure
- Pin and Function Compatible with 74LS365/366



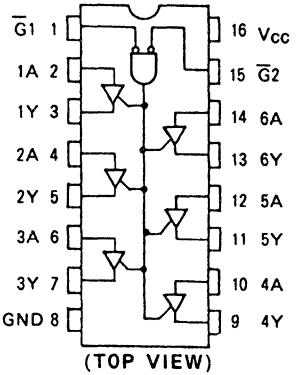
P(DIP16-P-300A)



F(SOP16-P-300)

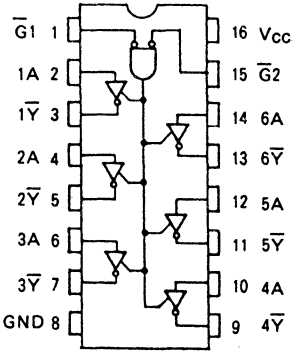
PIN ASSIGNMENT

TC74HC365A



(TOP VIEW)

TC74HC366A



(TOP VIEW)

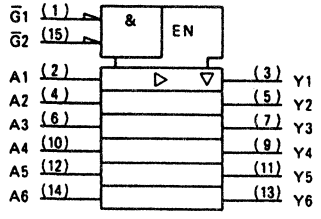
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}1$	$\overline{G}2$	An	Yn(365A)	$\overline{Yn}$(366A)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

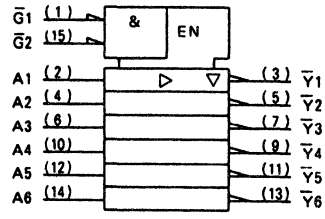
X : Don't care, Z : High Impedance

IEC LOGIC SYMBOL

TC74HC365A



TC74HC366A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} = −6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} = 6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	38	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	51	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	14	22	−	28	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	56	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	13	22	−	28	
	t_{pZH}		150	2.0	−	69	170	−	215	
				4.5	−	22	34	−	44	
				6.0	−	17	29	−	37	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	42	130	−	165	
				4.5	−	18	26	−	33	
				6.0	−	15	22	−	28	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD}(1)$				−	25	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

TC74HC367AP/AF/AFN
TC74HC368AP/AF/AFN

HEX BUS BUFFER
TC74HC367AP/AF/AFN NON-INVERTED
TC74HC368AP/AF/AFN INVERTED

The TC74HC367A and TC74HC368A are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

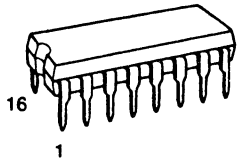
They contain six buffers; four buffers are controlled by enable input ($\overline{G1}$), and the other two buffers are controlled by enable input ($\overline{G2}$). The inputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low; if held high, these outputs are in a high impedance state.

The TC74HC367A is a non-inverting output type, while the TC74HC368A is an inverting output type.

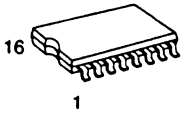
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

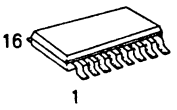
FEATURES:

- High Speed ····· t_{pd} = 11ns(Typ.)at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4 μA(Max.)at Ta = 25℃
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 6mA
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS367/368



P(DIP16-P-300A)

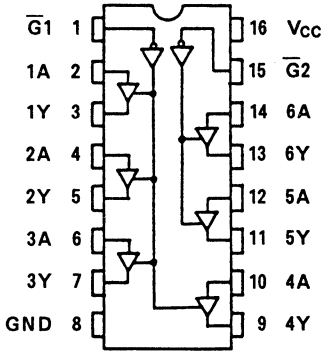




F(SOP16-P-300) FN(SOL16-P-150)

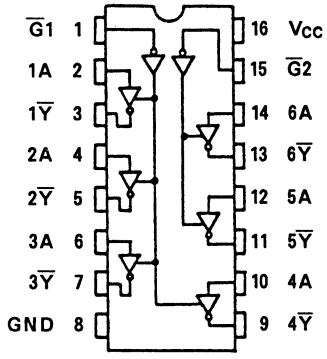
PIN ASSIGNMENT

TC74HC367A



(TOP VIEW)

TC74HC368A



(TOP VIEW)

TRUTH TABLE

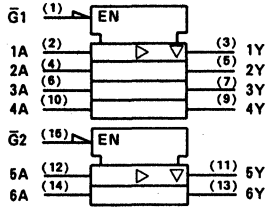
INPUTS		OUTPUTS	
$\overline{G}$	An	Y(367A)	$\overline{Y}$(368A)
L	L	L	H
L	H	H	L
H	X	Z	Z

X:DON'T CARE Z:HIGH IMPEDANCE

IEC LOGIC SYMBOL

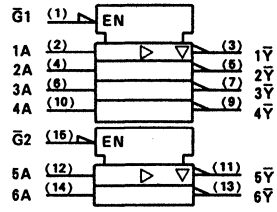
TC74HC367A

HEX BUS BUFFER
(3-STATE)



TC74HC368A

HEX BUS BUFFER
(3-STATE/INV.)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	Vcc	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	−	36	95	−	120	
				4.5	−	12	19	−	24	
				6.0	−	10	16	−	20	
			150	2.0	−	40	130	−	165	
				4.5	−	16	26	−	33	
				6.0	−	14	22	−	28	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	50	2.0	−	36	120	−	150	
				4.5	−	12	24	−	30	
				6.0	−	10	20	−	26	
			150	2.0	−	40	160	−	200	
				4.5	−	16	32	−	40	
				6.0	−	14	27	−	34	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	50	2.0	−	35	120	−	150	
				4.5	−	15	24	−	30	
				6.0	−	13	20	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HC367A			−	36	−	−	−	
		TC74HC368A			−	30	−	−		

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6$ (per bit)

TC74HC373AP/AF/AFW
TC74HC533AP/AF

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC373AP/AF NON-INVERTING
TC74HC533AP/AF INVERTING

The TC74HC373A and TC74HC533A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$).

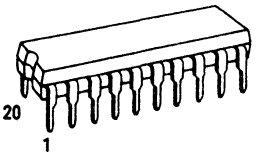
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC373A has non-inverting outputs, and TC74HC533A has inverting outputs.

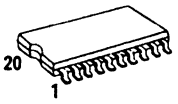
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

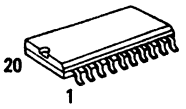
- High Speed ..... t_{pd}=11ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS373/533



P(DIP20-P-300A)



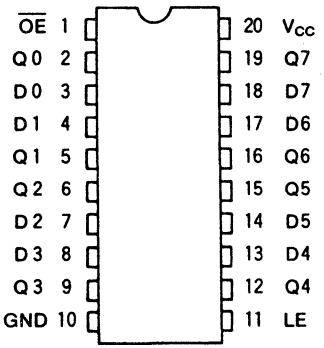
F(SOP20-P-300)



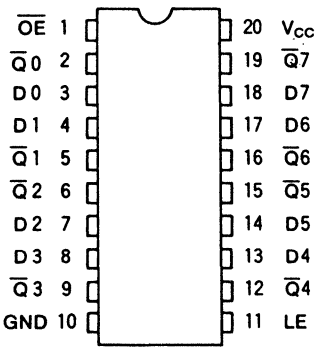
FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HC373A



TC74HC533A

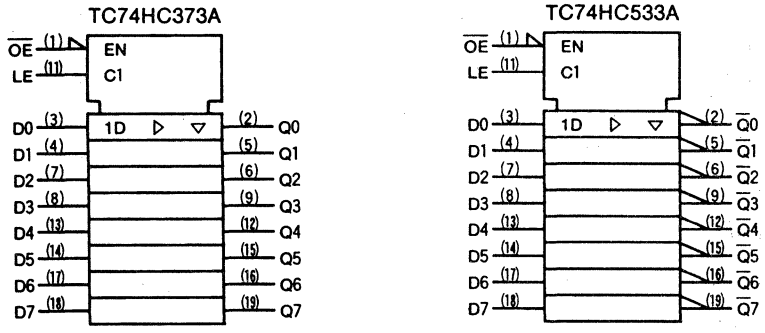


TRUTH TABLE

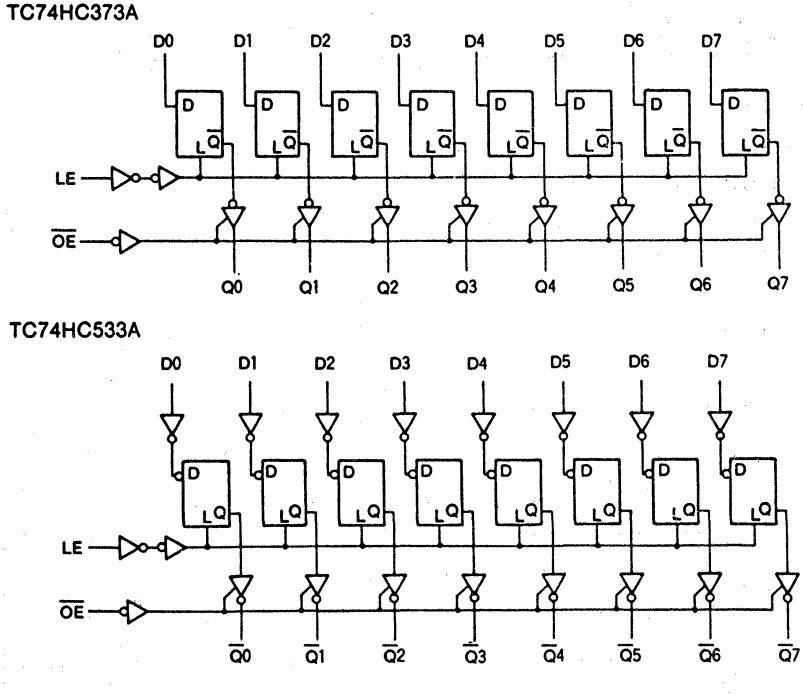
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC373A)	$\overline{Q}$(HC533A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n ($\overline{Q_n}$) : Q (Q) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Data)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pHL}		150	2.0	−	57	175	−	220	
				4.5	−	19	35	−	44	
				6.0	−	16	30	−	37	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	39	125	−	155	
				4.5	−	13	25	−	31	
				6.0	−	11	21	−	26	
	t_{pZH}		150	2.0	−	54	175	−	220	
				4.5	−	18	35	−	44	
				6.0	−	15	30	−	37	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	30	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	13	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total})=22+16 \cdot n$$

TC74HCT373AP/AF/AFW
TC74HCT533AP/AF

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HCT373AP/AF/AFW NON-INVERTING
TC74HCT533AP/AF INVERTING

The TC74HCT373A and HCT533A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

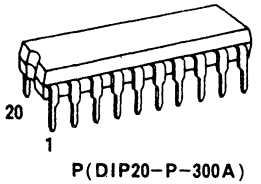
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HCT373A has non-inverting outputs, and TC74HCT533A has inverting outputs.

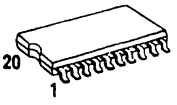
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

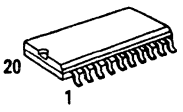
FEATURES:

- High Speed ····· t_{pd} =17ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V (Min.)
  V_{IL}=0.8V (Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS373/533



P(DIP20-P-300A)

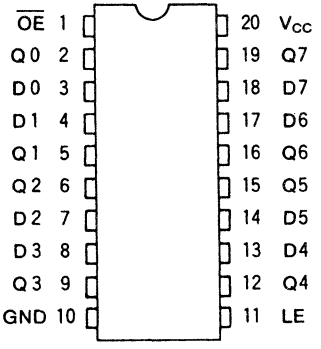




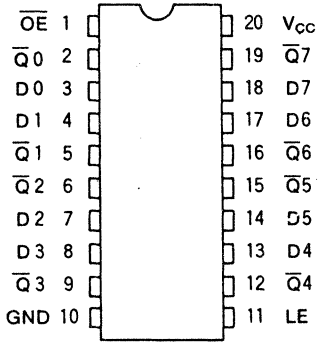
F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HCT373A



TC74HCT533A

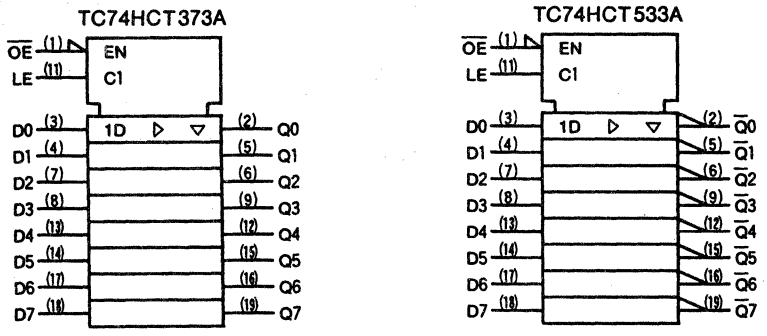


TRUTH TABLE

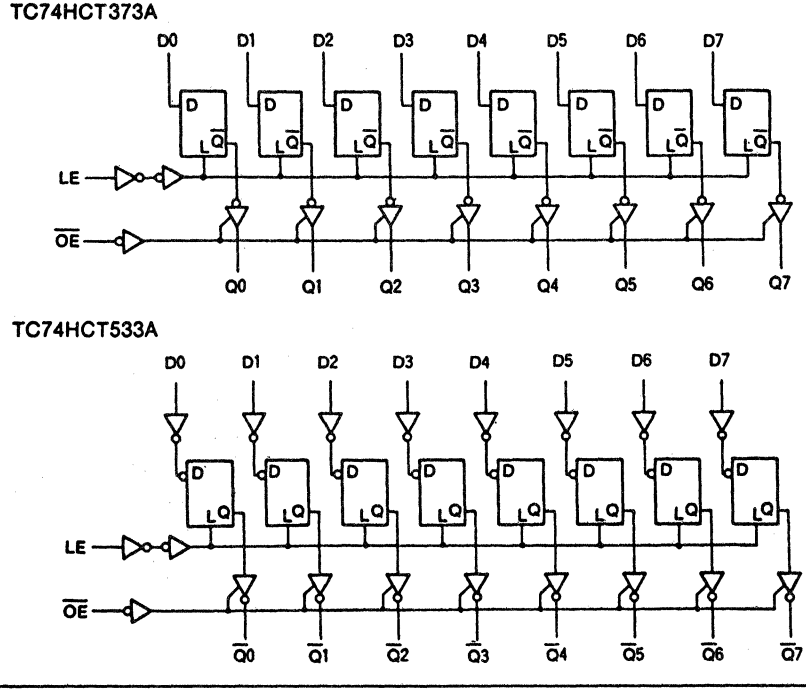
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(T373A)	$\overline{Q}$(T533A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
Q_n (Q_n) : Q (Q) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{IN} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Set−up Time (Data)	t_s		4.5	−	10	13	
			5.5	−	9	12	
Minimum Hold Time (Data)	t_h		4.5	−	5	5	
			5.5	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5	−	7	12	−	15	ns
				5.5	−	6	11	−	14	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
			150	4.5	−	24	38	−	48	
				5.5	−	22	34	−	43	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5	−	20	30	−	38	
				5.5	−	18	27	−	34	
			150	4.5	−	25	38	−	48	
				5.5	−	22	34	−	43	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
			150	4.5	−	24	38	−	48	
				5.5	−	22	34	−	43	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	20	30	−	38	
				5.5	−	18	27	−	34	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT373A			−	36	−	−	−	
Power Dissipation Capacitance	C (1)	TC74HCT533A			−	35	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Latch)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$C_{PD}(total)=19+17 \cdot n$ (TC74HCT373A)

$C_{PD}(total)=21+14 \cdot n$ (TC74HCT533A)

TC74HC374AP/AF/AFW
TC74HC534AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

TC74HC374AP/AF/AFW NON-INVERTING
TC74HC534AP/AF INVERTING

The TC74HC374A and TC74HC534A are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$).

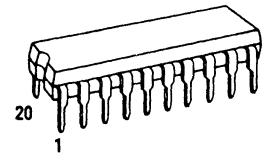
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC374A has non-inverting outputs, and TC74 HC534A has inverting outputs.

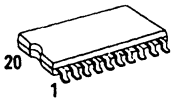
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

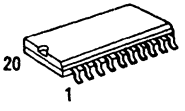
FEATURES:

- High Speed ····· f_{MAX}=77MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS374/534



P(DIP20-P-300A)

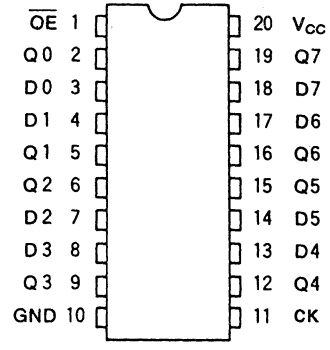




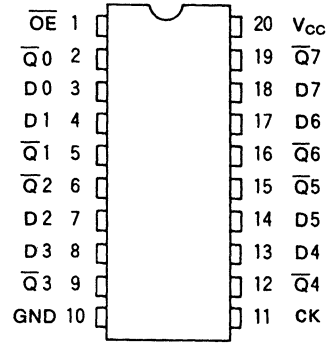
F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HC374A



TC74HC534A

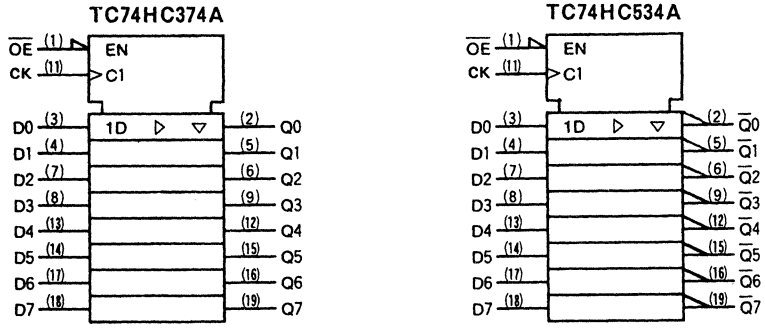


TRUTH TABLE

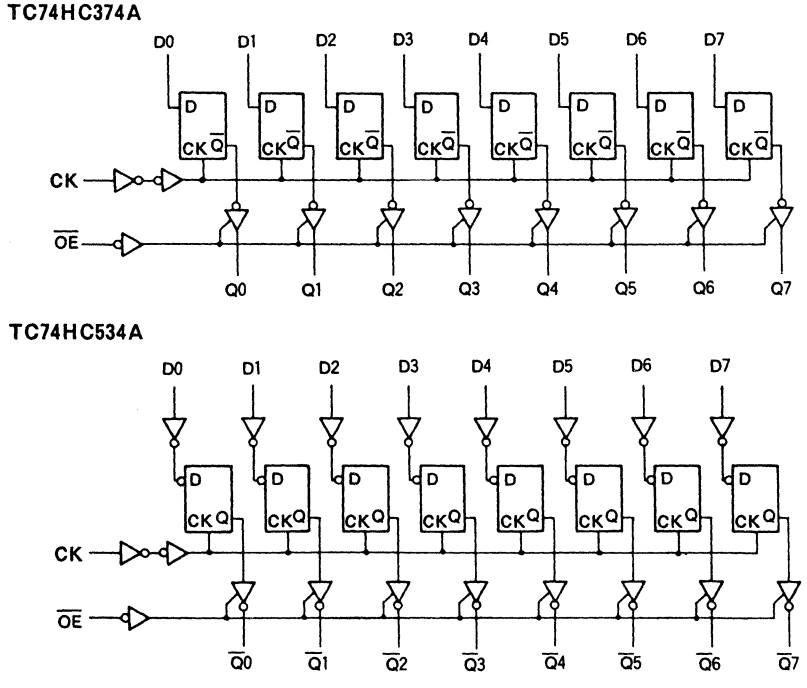
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(HC374A)	$\overline{Q}$(HC534A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Cange

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Dn)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (Dn)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	45	140	−	175	
				4.5	−	15	28	−	35	
				6.0	−	13	24	−	30	
	t_{pHL}		150	2.0	−	60	190	−	240	
				4.5	−	20	38	−	48	
				6.0	−	17	32	−	41	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	39	135	−	170	
				4.5	−	13	27	−	34	
				6.0	−	11	23	−	29	
	t_{pZH}		150	2.0	−	54	185	−	230	
				4.5	−	18	37	−	46	
				6.0	−	15	31	−	39	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	30	135	−	170	
				4.5	−	13	27	−	34	
				6.0	−	12	23	−	29	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	18	−	5	−	
				4.5	31	75	−	25	−	
				6.0	36	90	−	29	−	
			150	2.0	4	16	−	3	−	
				4.5	22	54	−	17	−	
				6.0	26	62	−	20	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)				−	47	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Flip Flop)}$$

And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

$$C_{PD}(total)=30+17 \cdot n$$

TC74HCT374AP/AF/AFW
TC74HCT534AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HCT374AP/AF/AFW NON-INVERTING
TC74HCT534AP/AF INVERTING

The TC74HCT374A and HCT534A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

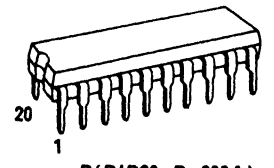
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HCT374A has non-inverting outputs, and the TC74HCT534A has inverting outputs.

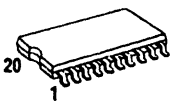
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

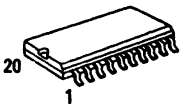
FEATURES:

- High Speed ····· f_{MAX}=41MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ··· V_{IH}=2V (Min.)
  V_{IL}=0.8V (Max.)
- Wide interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS374/534



P(DIP20-P-300A)

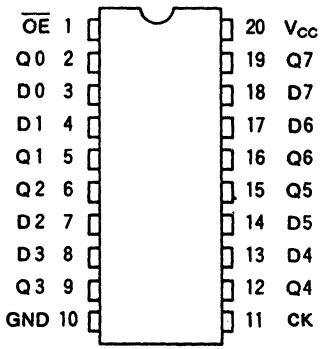




F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HCT374A



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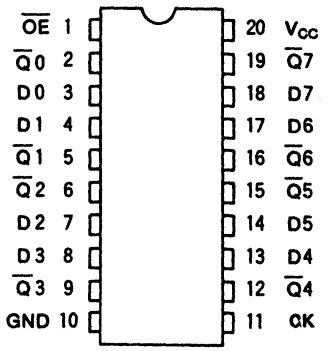
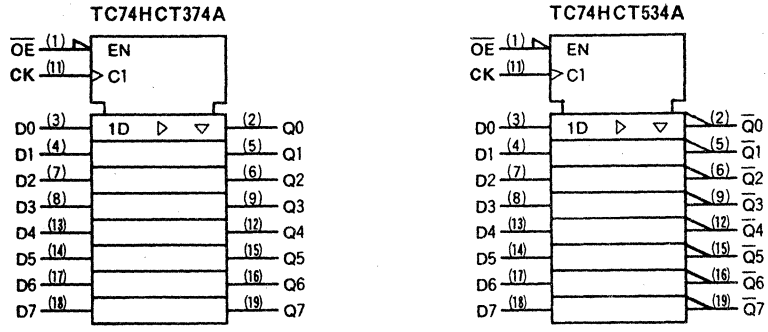


TRUTH TABLE

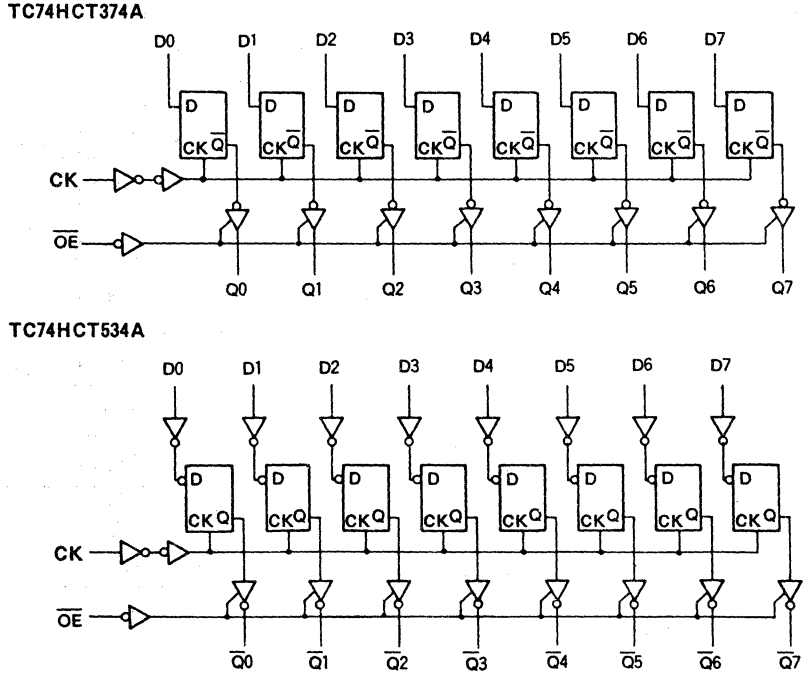
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(T374A)	$\overline{Q}$(T534A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
$Q_n(\overline{Q_n})$: No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{IN} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Set−up Time (Dn)	t_s		4.5	−	15	19	
			5.5	−	14	17	
Minimum Hold Time (Dn)	t_h		4.5	−	0	0	
			5.5	−	0	0	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5	−	7	12	−	15	ns
				5.5	−	6	11	−	14	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5	−	20	30	−	38	
				5.5	−	17	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	22	33	−	41	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	14	25	−	31	
			150	4.5	−	25	38	−	48	
				5.5	−	19	33	−	41	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	16	28	−	35	
				5.5	−	14	24	−	30	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	50	−	25	−	
				5.5	37	59	−	30	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	48	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total)=30+18 \cdot n$$

4-BIT D TYPE LATCH

The TC74HC375A is a high speed CMOS D-TYPE LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

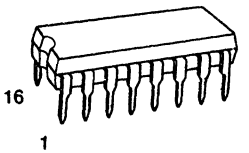
It contains two groups of 2-bit latches controlled by an enable input (G1 • 2 or G3 • 4) and each group can be used in different circuits.

Data applied to the data inputs are transferred to the Q and $\overline{Q}$ outputs when the enable inputs is high. When the enable input is low, the outputs are not affected.

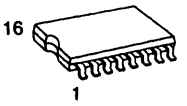
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC} =4μA(Max.)at Ta=25℃
- High Noise Immunity ..... V_{NIH}=V_{NIL} =28%V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=I_{OL} =4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)= 2 V~6V
- Pin and Function Compatible with 74LS375

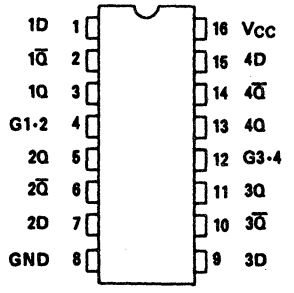


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



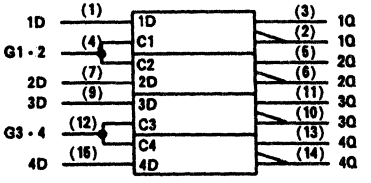
(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\overline{Q}$n	LATCH

X : Don't care

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (G)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	14	20	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		−	13	20	

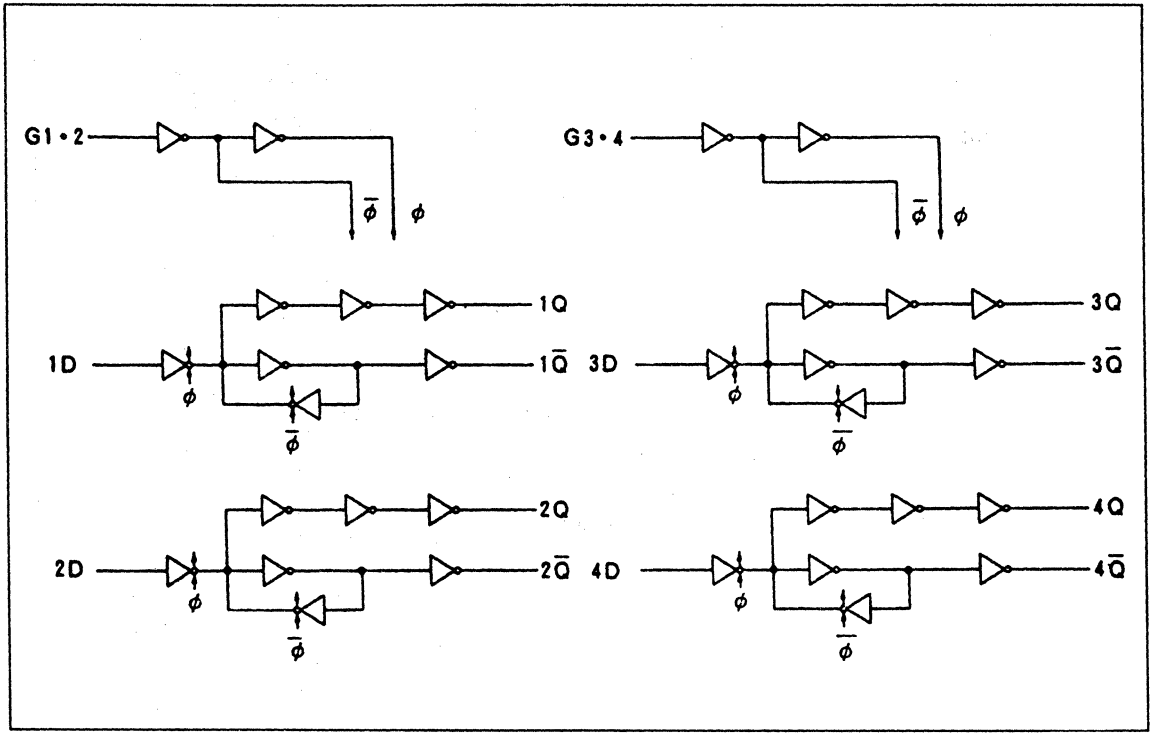
AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	60	120	−	150	
			4.5	−	17	24	−	30	
			6.0	−	15	20	−	26	
Propagation Delay Time (G−Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	−	56	120	−	150	
			4.5	−	16	24	−	30	
			6.0	−	14	20	−	26	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	55	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{(per Latch)}$$

SYSTEM DIAGRAM



TC74HC377AP/AF

OCTAL D-TYPE FLIP-FLOP

The TC74HC377A is a high speed CMOS OCTAL D-TYPE FLIP-FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{G}$).

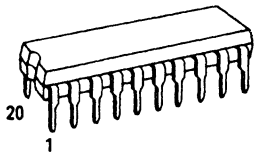
The signal level applied to the D inputs are transferred to Q outputs during the positive going transition of CK.

When the $\overline{G}$ is high, the eight outputs are in a high impedance state.

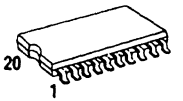
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=73MHZ(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS377

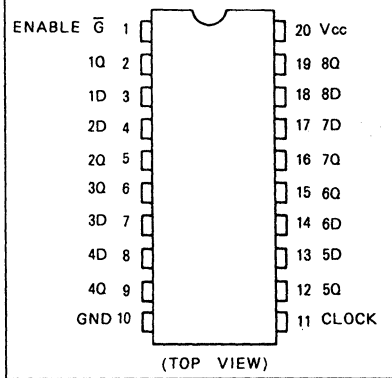


P(DIP20-P-300A)



F(SOP20-P-300)

PIN ASSIGNMENT

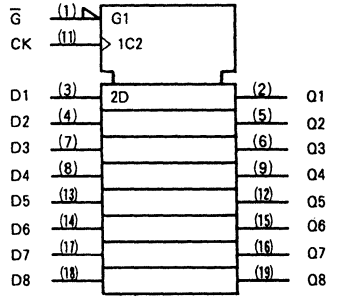


TRUTH TABLE

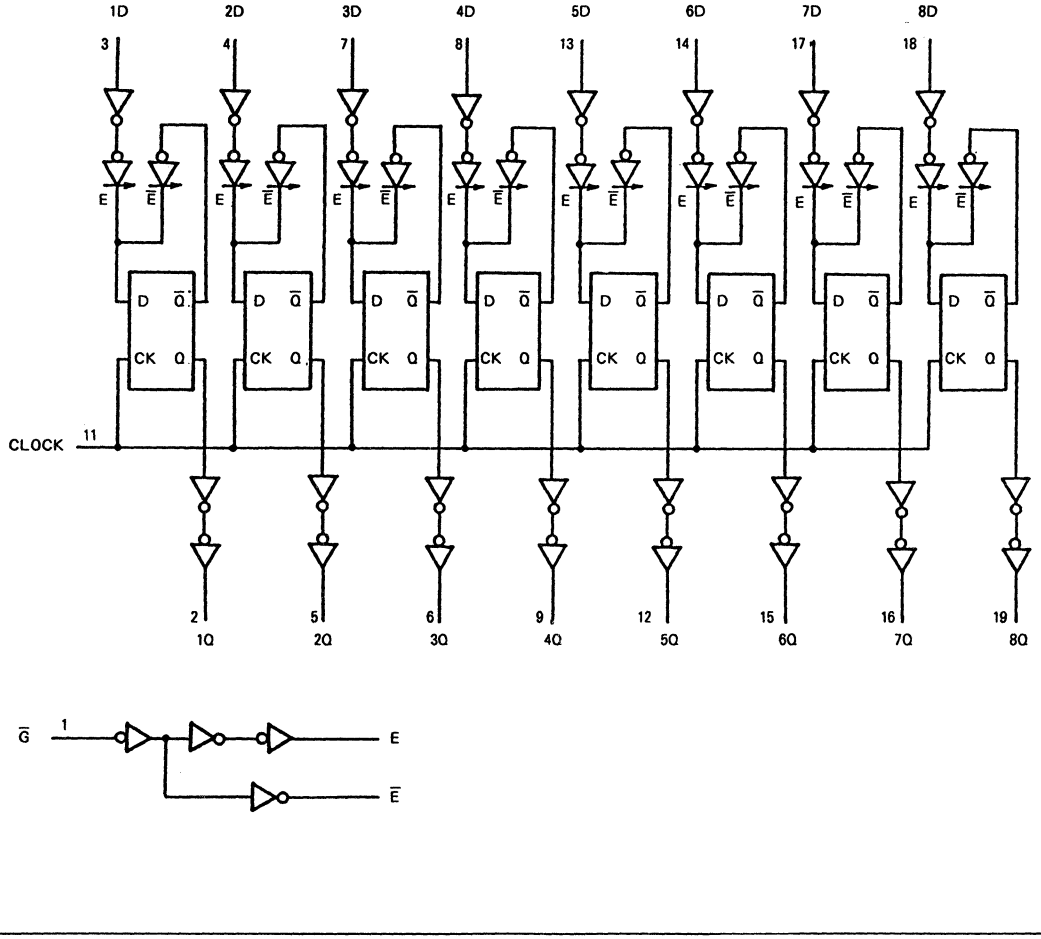
INPUTS			OUTPUTS
$\overline{G}$	CLOCK	DATA	Q
H	X	X	No Change
L	↑	L	L
L	↑	H	H
X	↓	X	No Change

X : Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~ 85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time (D-CK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time ($\overline{G}$-CK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	7	6	MHz
			4.5	−	36	29	
			6.0	−	42	34	

AC ELECTRICAL CHARACTERISTICS($C_L = 15pF, V_{CC} = 5V, Ta = 25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		−	14	24	
Maximum Clock Frequency	f_{MAX}		38	73	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L = 50pF$, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q)	t_{pLH} t_{pHL}		2.0	−	57	140	−	175	
			4.5	−	17	28	−	35	
			6.0	−	13	24	−	30	
Maximum Clock Frequency	f_{MAX}		2.0	7	18	−	6	−	MHz
			4.5	36	59	−	29	−	
			6.0	42	77	−	34	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}			−	32	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Frip Flop)}$$

And the total C_{PD} when n pcs.of Flip Flop operate can be gained by the following equation:

$$C_{PD}(total) = 22 + 10 \cdot n \quad (PF)$$

TC74HC386AP/AF

QUAD EXCLUSIVE OR GATE

The TC74HC386A is a high speed CMOS EXCLUSIVE-OR GATE fabricated with silicon gate C^2MOS technology.

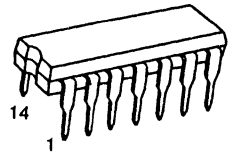
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is includes on output buffer, which provide high noise immunity and stable output.

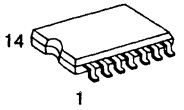
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$ =4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS386

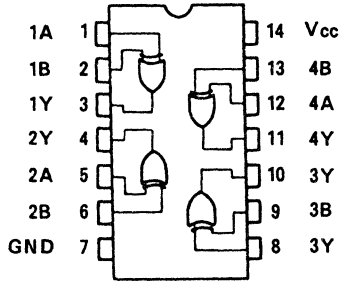


P(DIP14-P-300)



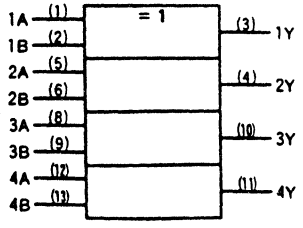
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	$T_{opr.}$	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	48	100	–	125	ns
			4.5	–	12	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	31	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per Gate)}$$

DUAL DECADE COUNTER

The TC74HC390A is a high speed CMOS DUAL DECADE COUNTER LATCH fabricated with silicon gate C^2MOS technology.

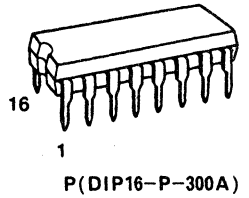
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of two independent 4-bit counters, each composed of a divide-by-two and a divide-by-five counter.The divide-by-two counter is incremented on the negative going transition of clock A($\overline{CKA}$). The divided-by-five counter is incremented on the negative going transition of clock B($\overline{CKB}$). The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, the Q outputs are set to low independent of the clock inputs.

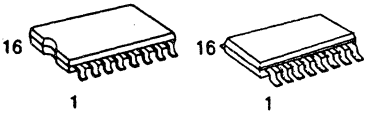
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=84MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS390

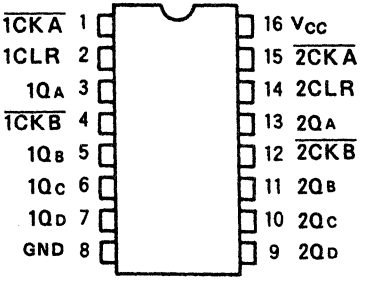


P(DIP16-P-300A)



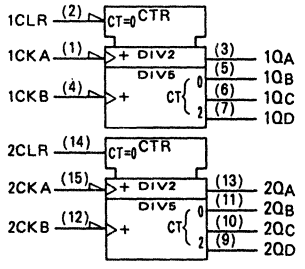
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT

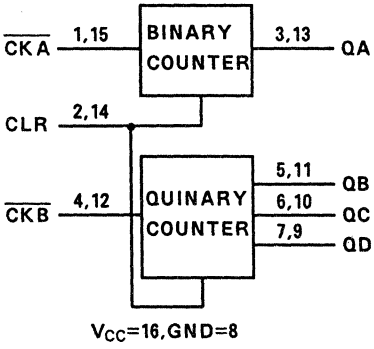


(TOP VIEW)

IEC LOGIC SYMBOL



BLOCK DIAGRAM

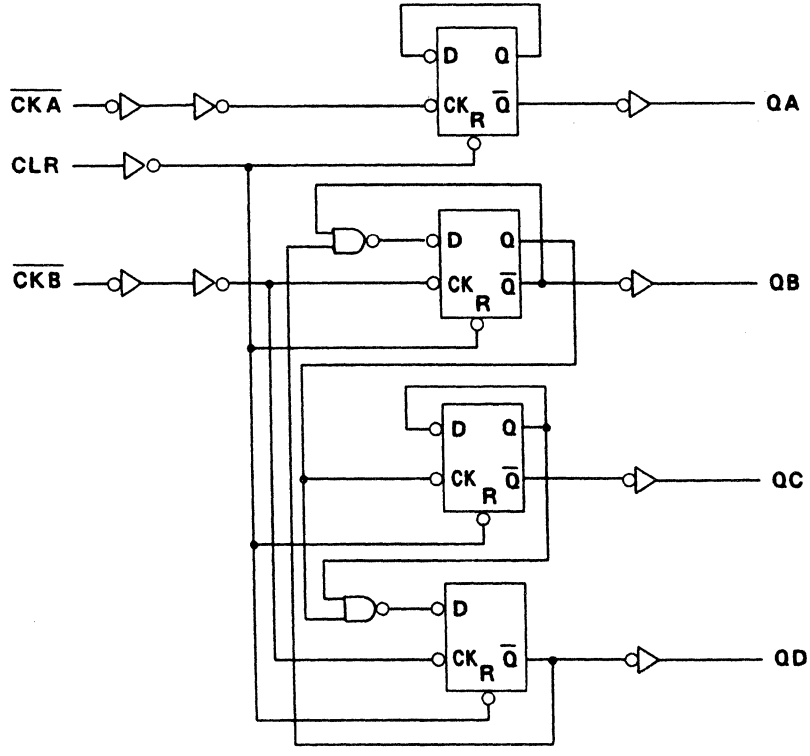


V_{CC}=16,GND=8

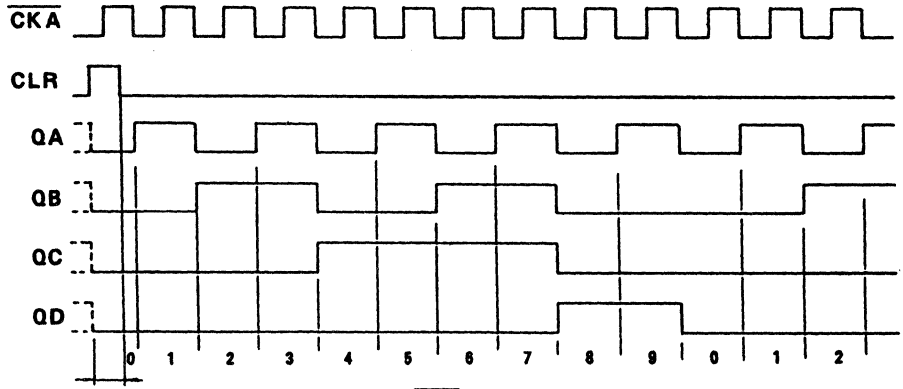
TRUTH TABLE

INTPUTS			OUTPUTS			
$\overline{CKA}$	$\overline{CKB}$	CLR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

SYSTEM DIAGRAM(1/2 package)

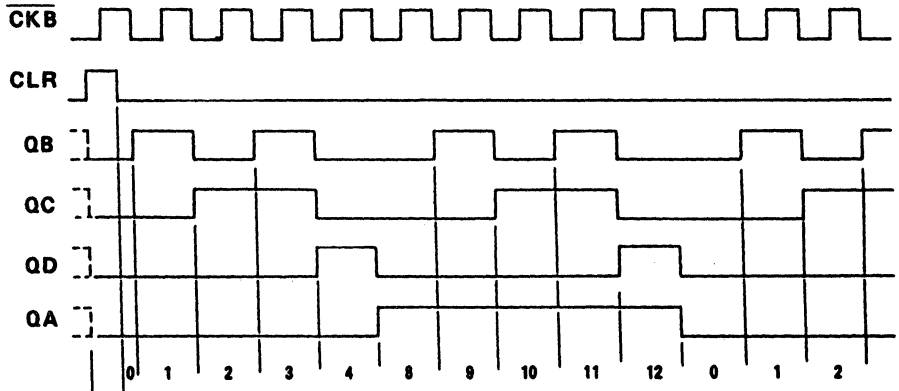


(1)BCD COUNT SEQUENCE*



* QA connected to $\overline{CKB}$

(2)BI-QUINARY COUNT SEQUENCE**



** QD connected to $\overline{CKA}$

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Clock Frequency ($\overline{CKA}$)	f		2.0	−	6	5	
			4.5	−	32	26	
			6.0	−	38	31	
Clock Frequency ($\overline{CKB}$)	f		2.0	−	6	5	
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CKA}$–QA)	t_{pLH} t_{pHL}		−	10	20	
Propagation Delay Time ($\overline{CKA}$–QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	−	29	51	
Propagation Delay Time ($\overline{CKB}$–QB, QD)	t_{pLH} t_{pHL}		−	12	22	
Propagation Delay Time ($\overline{CKB}$–QC)	t_{pLH} t_{pHL}		−	17	32	
Propagation Delay Time (CLR–Qn)	t_{pHL}		−	12	26	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}		35	84	−	MHz
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}		33	65	−	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CKA}$−QA)	t_{pLH} t_{pHL}		2.0	−	39	120	−	150	
			4.5	−	13	24	−	30	
			6.0	−	11	20	−	26	
Propagation Delay Time ($\overline{CKA}$−QC)	t_{pLH} t_{pHL}	QA connected to $\overline{CKB}$	2.0	−	102	290	−	365	
			4.5	−	34	58	−	73	
			6.0	−	29	49	−	62	
Propagation Delay Time ($\overline{CKB}$−QB, QD)	t_{pLH} t_{pHL}		2.0	−	45	130	−	165	
			4.5	−	15	26	−	33	
			6.0	−	13	22	−	28	
Propagation Delay Time ($\overline{CKB}$−QC)	t_{pLH} t_{pHL}		2.0	−	63	185	−	165	
			4.5	−	21	37	−	33	
			6.0	−	18	31	−	28	
Propagation Delay Time (CLR−Qn)	t_{pHL}		2.0	−	45	150	−	190	
			4.5	−	15	30	−	38	
			6.0	−	13	26	−	32	
Maximum Clock Frequency ($\overline{CKA}$)	f_{MAX}		2.0	6	20	−	5	−	MHz
			4.5	32	77	−	26	−	
			6.0	38	90	−	31	−	
Maximum Clock Frequency ($\overline{CKB}$)	f_{MAX}		2.0	6	15	−	5	−	
			4.5	31	60	−	25	−	
			6.0	36	70	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	44	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Counter)}$$

TC74HC393AP/AF/AFN

DUAL BINARY COUNTER

The TC74HC393A is a high speed CMOS 4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

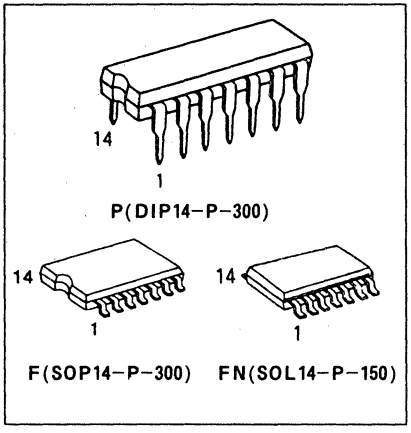
It contains two independent counter circuits in one package, so that counting or frequency division of eight binary bits can be achieved with one IC.

This device changes state on the negative going transition of the $\overline{CLOCK}$ pulse. The counter can be reset to "0" (Q0~Q3="L") by a high at the CLEAR input regardless of other inputs.

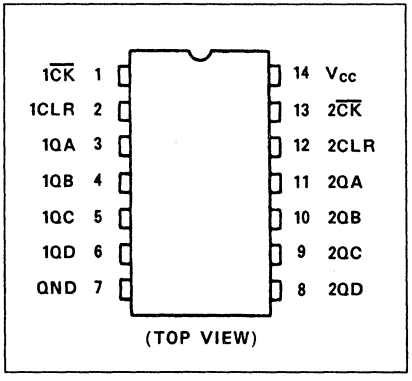
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

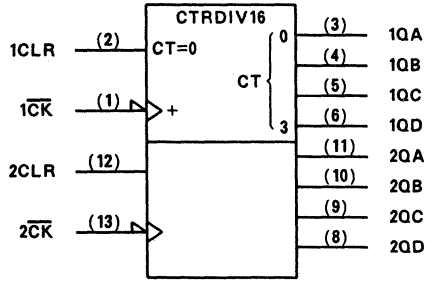
- High Speed ····· f_{MAX}=72MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS393



PIN ASSIGNMENT



IEC LOGIC SYMBOL

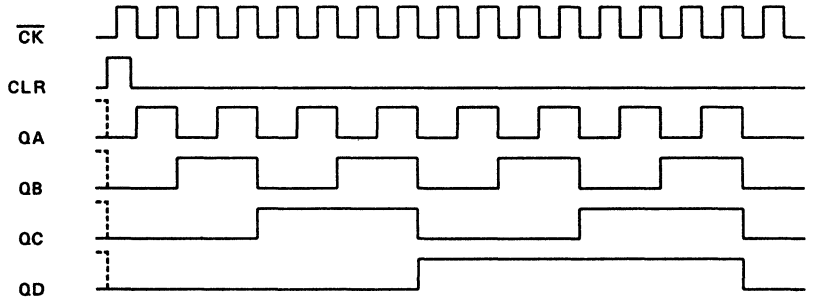


TRUTH TABLE

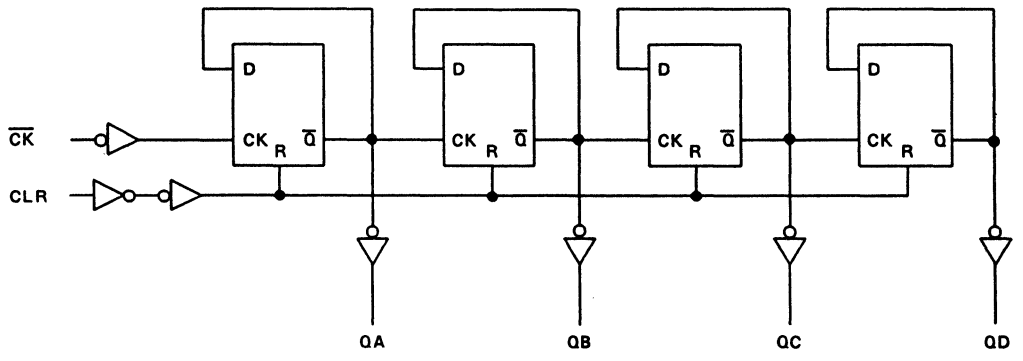
INPUTS		OUTPUTS			
$\overline{CK}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

X : Don't care

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$–QA)	t_{pLH} t_{pHL}		–	12	20	
Propagation Delay Time ($\overline{CLOCK}$–QB)	t_{pLH} t_{pHL}		–	16	31	
Propagation Delay Time ($\overline{CLOCK}$–QC)	t_{pLH} t_{pHL}		–	21	38	
Propagation Delay Time ($\overline{CLOCK}$–QD)	t_{pLH} t_{pHL}		–	25	46	
Propagation Delay Time (CLEAR–Qn)	t_{pHL}		–	15	26	
Maximum Clock Frequency	f_{MAX}		35	72	–	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	25	75	–	95	ns
			4.5	–	7	15	–	19	
			6.0	–	6	13	–	16	
Propagation Delay Time ($\overline{CLOCK}$–QA)	t_{pLH} t_{pHL}		2.0	–	45	120	–	150	
			4.5	–	15	24	–	30	
			6.0	–	13	20	–	26	
Propagation Delay Time ($\overline{CLOCK}$–QB)	t_{pLH} t_{pHL}		2.0	–	60	180	–	225	
			4.5	–	20	36	–	45	
			6.0	–	17	31	–	38	
Propagation Delay Time ($\overline{CLOCK}$–QC)	t_{pLH} t_{pHL}		2.0	–	80	220	–	275	
			4.5	–	25	44	–	55	
			6.0	–	21	37	–	47	
Propagation Delay Time ($\overline{CLOCK}$–QD)	t_{pLH} t_{pHL}		2.0	–	100	260	–	325	
			4.5	–	30	52	–	65	
			6.0	–	26	44	–	55	
Propagation Delay Time (CLEAR–Qn)	t_{pHL}		2.0	–	55	150	–	190	
			4.5	–	18	30	–	38	
			6.0	–	15	26	–	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	22	–	5	–	
			4.5	32	67	–	27	–	
			6.0	38	77	–	32	–	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	40	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC423AP/AF

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC423A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, $\overline{A}$ input (Negative edge), and B input (Positive edge). These inputs are valid for a slow rise/fall time signal (tr=tf=1sec.) as they are schmitt trigger inputs.

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor (Rx, Cx). A low level at the $\overline{CLR}$ input breaks this state. In the MONO STABLE state, if a new trigger is applied, it extends the MONOSTABLE period (retrigger mode).

Limitations for Cx and Rx are :

External capacitor Cx....No limit

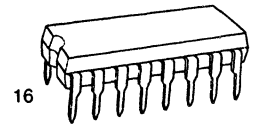
External resistor Rx.... Vcc<2.0V more than 5Ω

Vcc≥3.0V more than 1kΩ

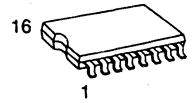
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=25ns(typ.)at V_{CC}=5V
- Low Power Dissipation
  - Standby State I_{CC} =4μA(max.)at Ta=25℃
  - Active State I_{CC} =700μA(max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V_{CC}
- Pin and Function Compatible with 74LS423

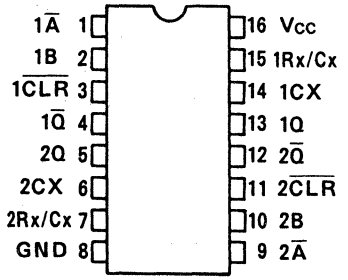


P(DIP16-P-300A)



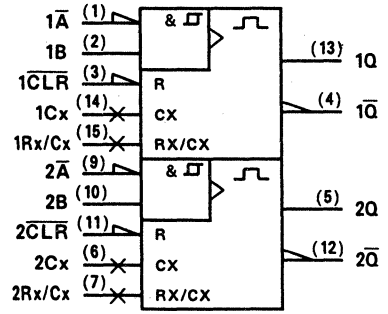
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

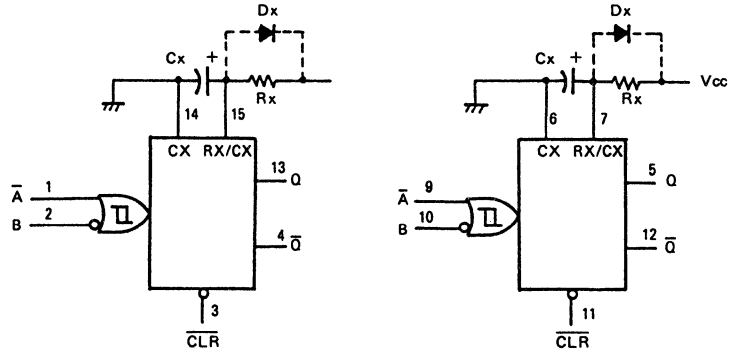


TRUTH TABLE

INPUT			OUTPUT		NOTE
$\overline{A}$	B	$\overline{CLR}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:Don't Care

BLOCK DIAGRAM



Notes: (1)Cx,Rx,Dx are external.
Capacitor,Resistor,and Diode,respectively.

(2)External clamping diode,Dx;

The external capacitor is charged to Vcc level in the wait state, i. e. when no trigger is applied. If the supply voltage is turned off, Cx is discharges mainly through the internal (parasitic) diode. If Cx is sufficiently large and Vcc drops rapidly, there will be some possibility of damaging the IC through in rush current or latch-up. If the capacitance of the supply voltage filter is large enough and Vcc drops slowly, the in rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20mA.

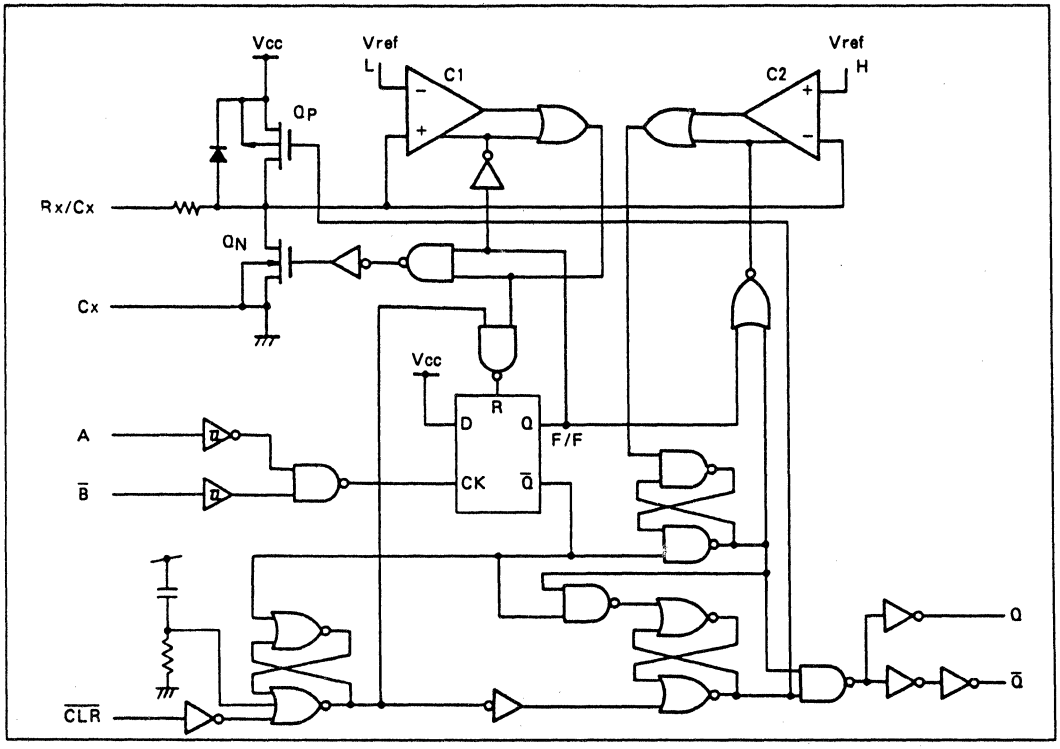
In the case of a large Cx, the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (Vcc-0.7)\ Cx/20mA$$

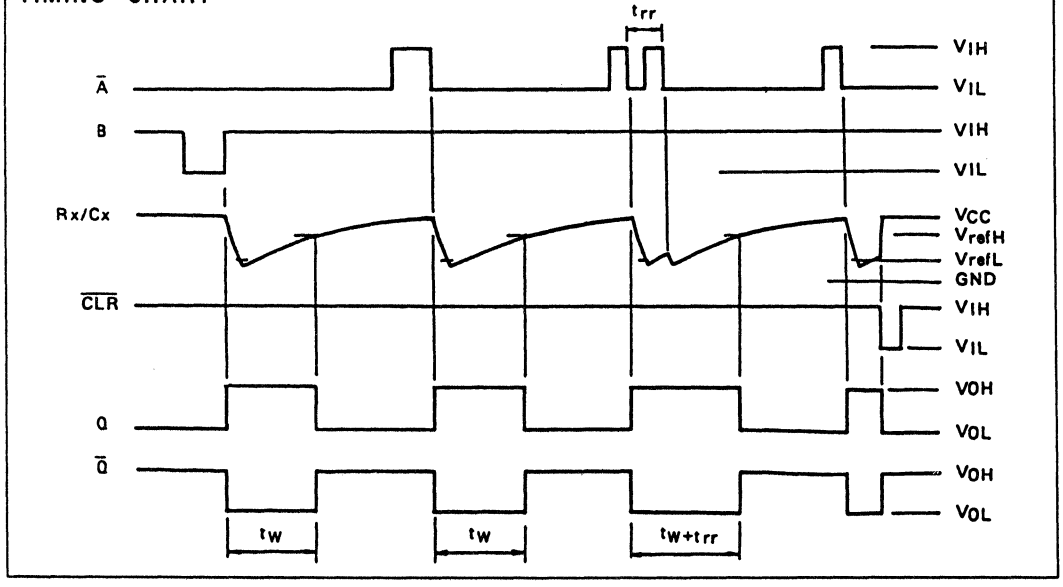
(t_f is the time between the supply voltage turn off and the supply voltage reaching 0.4 Vcc.)

In the event a system does not satisfy the above condition,an external clamping diode (Dx) is needed to protect the IC from rush current.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1)Stand-by State

The external capacitor Cx is fully charged to Vcc in the stand-by state. That means, before triggering, the Q_P and Q_N transistors which are connected to the Rx/Cx node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

(2)Trigger operation

Trigger operation is effective in either of the following two cases. First, the condition where the $\overline{A}$ input is low, and the B input has a rising signal; second, where the B input is high, and the $\overline{A}$ input has a falling signal.

After a trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N . The voltage level of the Rx/Cx node drops. If the Rx/Cx voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

After Q_N turns off, the voltage at the Rx/Cx starts rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

Upon the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of Rx/Cx changes from falling to rising. When Rx/Cx reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of the Rx/Cx reaches Vref H, the IC returns to its MONO STABLE state.

With large value of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse tw(OUT) is as follows:

$$tw(OUT)=1.0Cx\ Rx$$

(3)Retrigger operation

When a new trigger is applied to input $\overline{A}$ or B while in the MONO STABLE state, it is effective only if the IC is charging Cx. The voltage level of the Rx/Cx node then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.

If the 2nd trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2nd trigger, trr(Min), depends on Vcc and Cx.

(4)Reset operation

In normal operation, $\overline{CLR}$ input is held high. If $\overline{CLR}$ is low, a trigger has no effect because the Q output is held low and trigger control F/F is reset. Also Q_P turns on and Cx is charged rapidly to Vcc.

This means if $\overline{CLR}$ input is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns
External Capactior	Cx	No Limitation*	F
External Resistor	Rx	$\geq$5K* (Vcc<2.0V) $\geq$1K* (Vcc$\geq$3.0V)	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC423A, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for Rx>1MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage (Q,$\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage (Q,$\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Rx/Cx Terminal Off−State Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active−State * Supply Current	I_{CC}	V_{IN} =V_{CC} or GND Rx/Cx =0.5V_{CC}		2.0	−	45	200	−	260	μA
				4.5	−	400	500	−	650	μA
				6.0	−	0.7	1.0	−	1.3	mA

*: per circuit

TIMING REQUIREMENTS(Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Width	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Removal Time	t_{rem}		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Retrigger Time	t_{rr}	Rx=1KΩ Cx=100pF	2.0	325	−	−	
			4.5	108	−	−	
			6.0	78	−	−	
		Rx=1KΩ Cx=0.01pF	2.0	5.0	−	−	μs
			4.5	1.4	−	−	
			6.0	1.2	−	−	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{A}$,B–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		–	25	36	
Propagation Delay Time ($\overline{CL}$–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		–	16	27	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

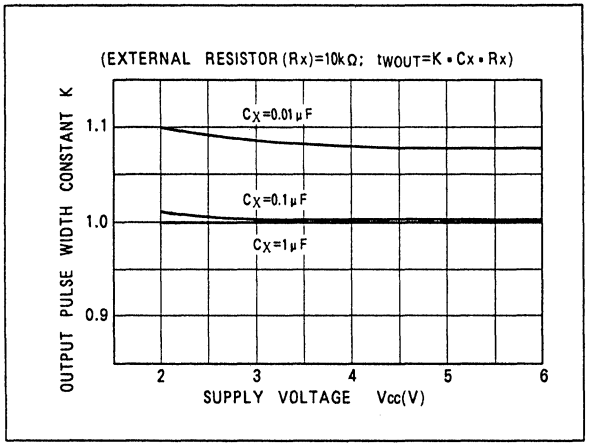
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{A}$,B–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	102	210	–	265	
			4.5	–	29	42	–	53	
			6.0	–	22	36	–	45	
Propagation Delay Time ($\overline{CL}$–Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	68	160	–	200	
			4.5	–	20	32	–	40	
			6.0	–	16	27	–	34	
Output Pulse Width	tw_{OUT}	Cx=28pF Rx=6KΩ(V_{CC} =2V) Rx=2KΩ(V_{CC}=4.5V,6V)	2.0	–	700	2000	–	2500	ns
			4.5	–	250	400	–	500	
			6.0	–	210	340	–	425	
		Cx=0.01μF Rx=10KΩ	2.0	90	110	130	90	130	μs
			4.5	95	105	115	95	115	
			6.0	95	105	115	95	115	
		Cx=0.1μF Rx=10KΩ	2.0	0.9	1.0	1.2	0.9	1.2	ms
			4.5	0.9	1.0	1.1	0.9	1.1	
			6.0	0.9	1.0	1.1	0.9	1.1	
Output Pulse Width Error Between Circuits (In same Package)	Δtw_{OUT}			–	±1	–	–	–	%
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	Note (1)		–	162	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

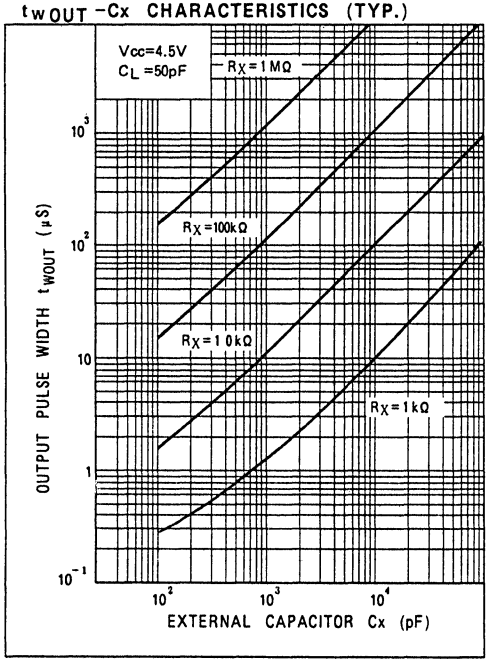
$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}' \cdot Duty/100+I_{CC}/2$(per circuit)

(I_{CC}' :Active Supply Current)
(Duty:%)

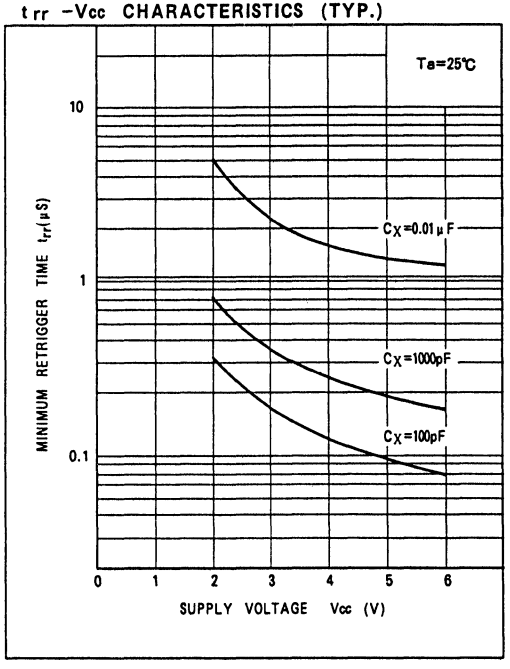
OUTPUT PULSE WIDTH CONSTANT K-SUPPLY VOLTAGE (TYPICAL)



tWOUT -Cx CHARACTERISTICS (TYP.)



trr -Vcc CHARACTERISTICS (TYP.)



TC74HC540AP/AF/AFW
TC74HC541AP/AF/AFW

OCTAL BUS BUFFER

TC74HC540AP/AF/AFW INVERTING,3-STATE OUTPUTS

TC74HC541AP/AF/AFW NON-INVERTING,3-STATE OUTPUTS

The TC74HC540A/TC74HC541A are high speed CMOS OCTRAL BUS BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

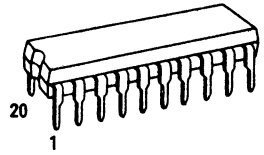
The TC74HC540A is a non-inverting type, and the TC74 HC541A is an inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

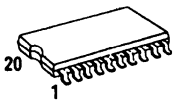
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

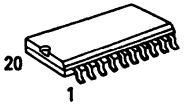
FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS540/541



P(DIP20-P-300A)





F(SOP20-P-300) FW(SOL20-P-300)

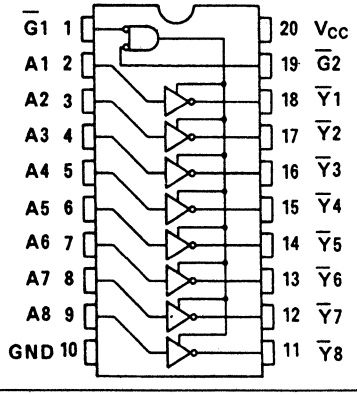
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

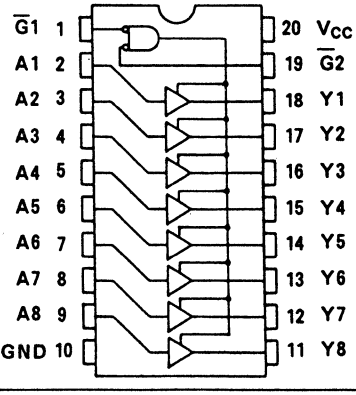
X : Don't Care
Z : High Impedance
* : Yn ····· HC541A
$\overline{Yn}$ ····· HC540A

PIN ASSIGNMENT

TC74HC540A

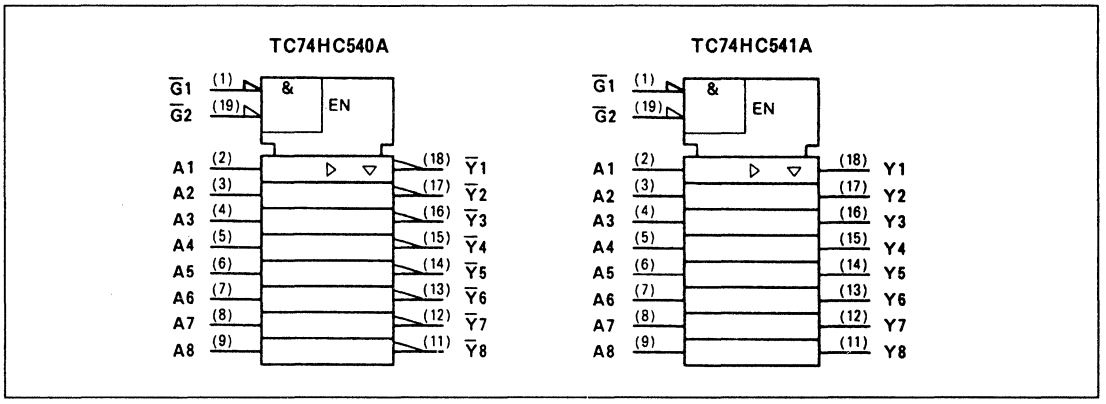


TC74HC541A



(TOP VIEW)

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	36	90	−	115	
				4.5	−	12	18	−	23	
				6.0	−	10	15	−	20	
	t_{pHL}		150	2.0	−	51	130	−	165	
				4.5	−	17	26	−	33	
				6.0	−	14	22	−	28	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	2.0	−	45	125	−	155	
				4.5	−	14	25	−	31	
				6.0	−	12	21	−	26	
	t_{pZH}		150	2.0	−	60	165	−	205	
				4.5	−	19	33	−	41	
				6.0	−	16	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	40	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	$C_{PD}(1)$	TC74HC540A			−	32	−	−	−	
		TC74HC541A			−	35	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HCT540AP/AF/AFW
TC74HCT541AP/AF/AFW

OCTAL BUS BUFFER WITH TTL INPUT LEVEL
TC74HCT540AP/AF/AFW INVERTING,3-STATE OUTPUTS
TC74HCT541AP/AF/AFW NON-INVERTING,3-STATE OUTPUTS

The TC74HCT540A/TC74HCT541A are high speed CMOS OCTRAL BUS BUFFERS fabricated with silicon gate C^2MOS technology.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

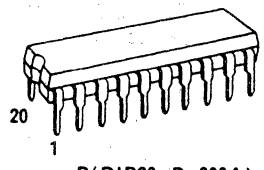
The TC74HCT540A is a non-inverting type, and the TC 74HCT541A is an inverting type.

When either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.

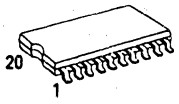
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

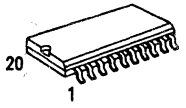
- High Speed ····· t_{pd} = 10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IL}=0.8V(Max.), V_{IH}=2.0V(Min.)
- Wide Interfacing ability ····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS540/541



P(DIP20-P-300A)



F(SOP20-P-300)



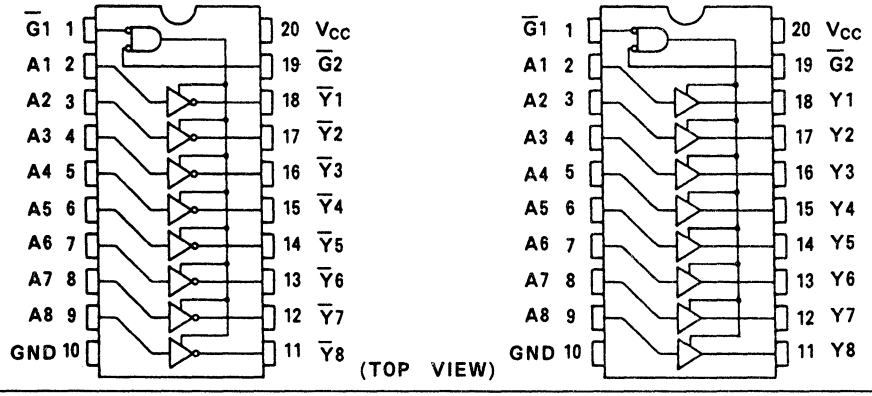
FW(SOL20-P-300)

TRUTH TABLE

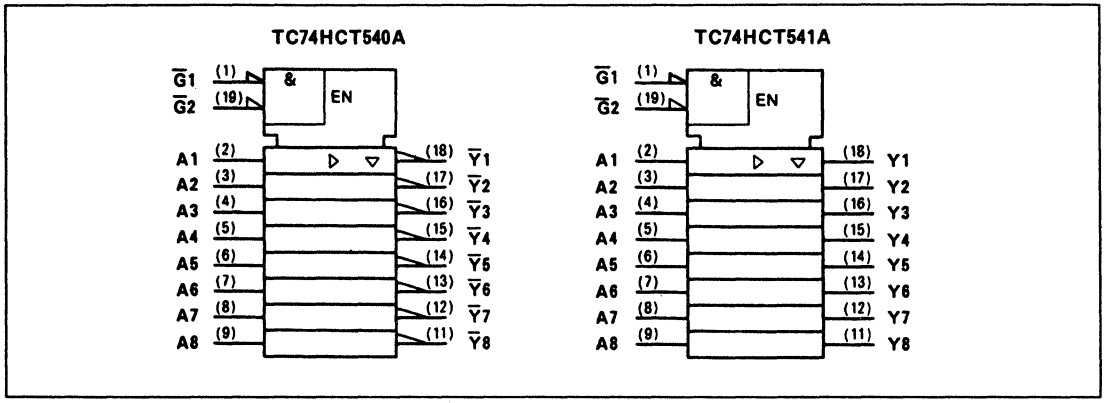
INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	H	L
L	L	L	L	H

X : Don't Care
Z : High Impedance
* : Yn ····· HCT541A
$\overline{Yn}$ ····· HCT540A

PIN ASSIGNMENT



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperrature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r , t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{CC}	Per input: V_{IN} =0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5 5.5	− −	7 6	12 11	− −	15 14	ns
Propagation Delay Time	t_{pLH}	TC74HCT540A	50	4.5 5.5	− −	12 9	20 18	− −	25 23	
	t_{pHL}		150	4.5 5.5	− −	17 14	26 24	− −	33 30	
Propagation Delay Time	t_{pLH}	TC74HCT541A	50	4.5 5.5	− −	14 11	23 21	− −	29 27	
	t_{pHL}		150	4.5 5.5	− −	19 16	29 27	− −	36 33	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	4.5 5.5	− −	18 16	30 27	− −	38 35	
	t_{pZH}		150	4.5 5.5	− −	23 21	36 33	− −	45 41	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	4.5 5.5	− −	18 16	30 27	− −	38 35	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT540A			−	35	−	−	−	
		TC74HCT541A			−	31	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HC563AP/AF
TC74HC573AP/AF/AFW

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT
TC74HC563AP/AF INVERTING
TC74HC573AP/AF/AFW NON-INVERTING

The TC74HC563A and TC74HC573A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input($\overline{OE}$).

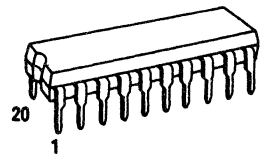
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HC563A has inverting outputs, and TC74HC573A has non-inverting outputs.

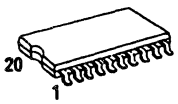
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

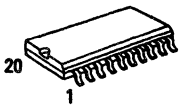
- High Speed ····· t_{pd} =13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS563/573



P(DIP20-P-300A)



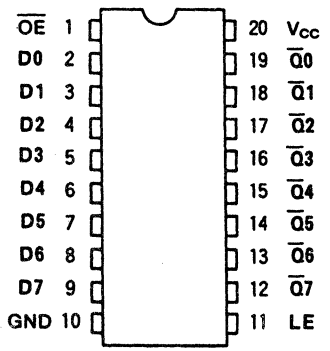
F(SOP20-P-300)



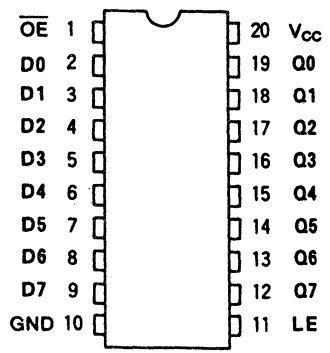
FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HC563A



TC74HC573A

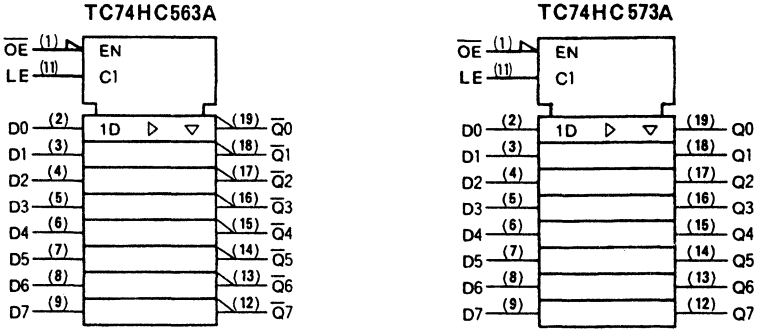


TRUTH TABLE

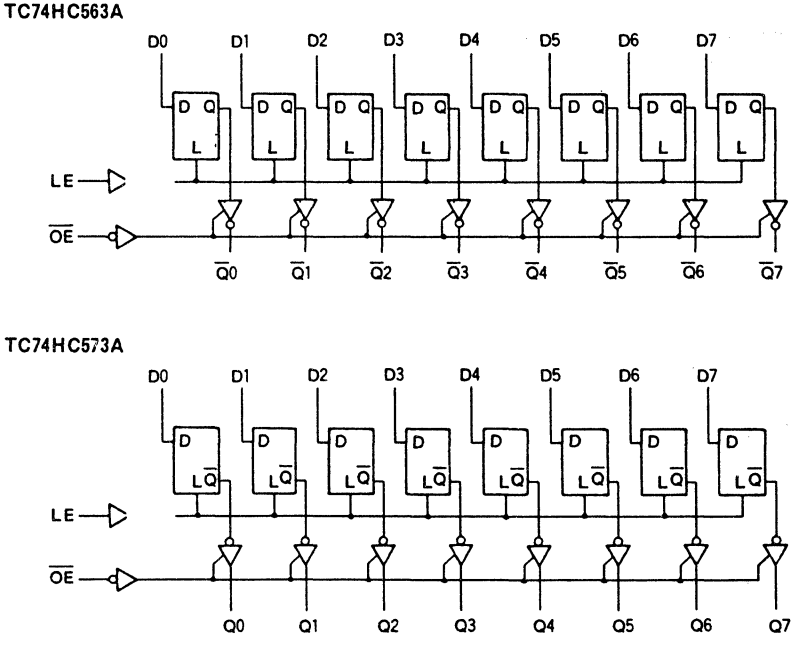
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HC573A)	$\overline{Q}$(HC563A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
$Q_n(\overline{Q_n})$: Q($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Data)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (Data)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	20	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	50	115	−	145	
				4.5	−	15	23	−	29	
				6.0	−	13	20	−	25	
	t_{pHL}		150	2.0	−	60	155	−	195	
				4.5	−	20	31	−	39	
				6.0	−	17	26	−	33	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	2.0	−	42	110	−	140	
				4.5	−	14	22	−	28	
				6.0	−	12	19	−	24	
	t_{pHL}		150	2.0	−	57	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	32	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	2.0	−	55	140	−	175	
				4.5	−	17	28	−	35	
				6.0	−	14	24	−	30	
	t_{pZH}		150	2.0	−	66	180	−	225	
				4.5	−	22	36	−	45	
				6.0	−	19	31	−	38	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	40	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	15	21	−	26	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC563A			−	49	−	−	−	
		TC74HC573A			−	51	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per Latch})$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$C_{PD}(total)=33+16 \cdot n$ (TC74HC563A)

$C_{PD}(total)=33+18 \cdot n$ (TC74HC573A)

TC74HCT563AP/AF
TC74HCT573AP/AF/AFW

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HCT563AP/AF INVERTING
TC74HCT573AP/AF/AFW NON-INVERTING

The TC74HCT563A and TC74HCT573A are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

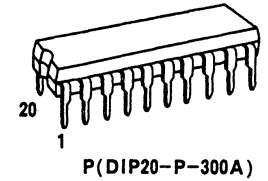
When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

The TC74HCT563A has inverting outputs, and the TC74HCT573A has non-inverting outputs.

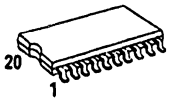
All inputs are equipped with protection circuits against static dischage or transient excess voltage.

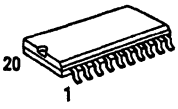
FEATURES:

- High Speed ····· t_{pd} =18ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH} =2.0V(Min.)
  V_{IL} =0.8V(Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS563/573



P(DIP20-P-300A)

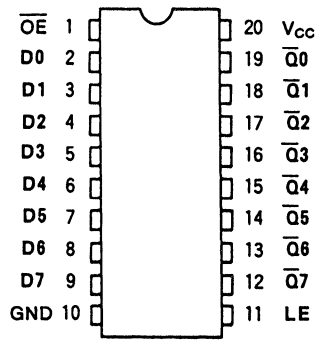




F(SOP20-P-300) FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HCT563A



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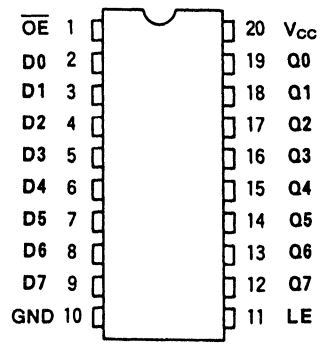
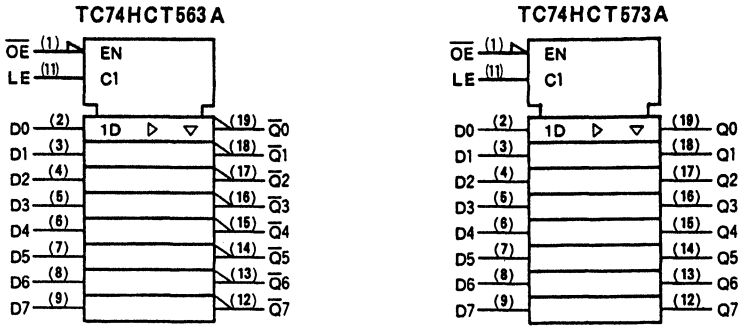


TRUTH TABLE

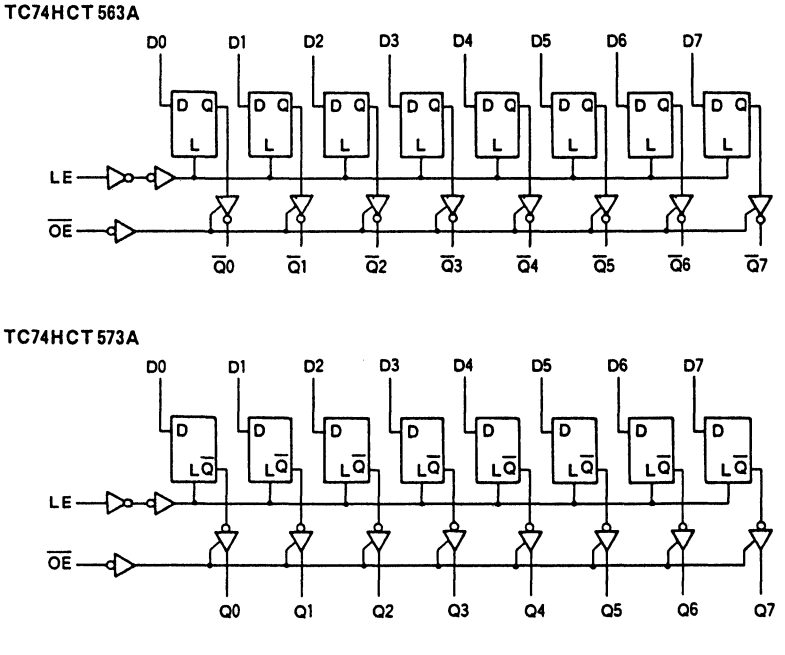
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HCT573A)	$\overline{Q}$(HCT563A)
H	X	X	Z	Z
L	L	X	Q_n	$\overline{Q_n}$
L	H	L	L	H
L	H	H	H	L

X : Don't Care
Z : High Impedance
$Q_n(\overline{Q_n})$: Q($\overline{Q}$) outputs are latched at the time when the LE input is taken to a low logic level.

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{cc}	Per input: V_{IN} = 0.5V or 2.4V, Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(H)}$		4.5	−	15	19	ns
			5.5	−	14	17	
Minimum Set−up Time (Data)	t_s		4.5	−	10	13	
			5.5	−	9	11	
Minimum Hold Time (Data)	t_h		4.5	−	5	5	
			5.5	−	5	5	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5	−	7	12	−	15	ns
				5.5	−	6	11	−	14	
Propagation Delay Time (LE−Q, $\overline{Q}$)	t_{pLH}		50	4.5	−	19	29	−	36	
				5.5	−	17	26	−	33	
	t_{pHL}		150	4.5	−	24	37	−	46	
				5.5	−	22	34	−	43	
Propagation Delay Time (D−Q, $\overline{Q}$)	t_{pLH}		50	4.5	−	17	26	−	23	
				5.5	−	14	23	−	21	
	t_{pHL}		150	4.5	−	22	34	−	43	
				5.5	−	20	31	−	39	
Output Enable time	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	18	27	−	34	
				5.5	−	15	24	−	30	
	t_{pZH}		150	4.5	−	23	35	−	44	
				5.5	−	20	32	−	40	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	18	24	−	30	
				5.5	−	16	22	−	28	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT563A			−	37	−	−	−	
		TC74HCT573A			−	38	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per Latch)}$$

And the total C_{PD} when n pcs. of Latch operate can be gained by the following equation:

$C_{PD}(total)=25+12 \cdot n$ (TC74HC563A)

$C_{PD}(total)=25+13 \cdot n$ (TC74HC573A)

TC74HC564AP/AF
TC74HC574AP/AF/AFW

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT
TC74HC564AP/AF INVERTING
TC74HC574AP/AF/AFW NON-INVERTING

The TC74HC564A and HC574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUTS fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

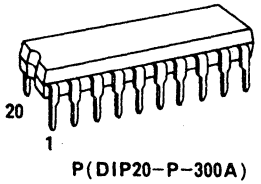
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HC564A has inverting outputs, and the TC74 HC574A has non-inverting outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=62MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS564/574



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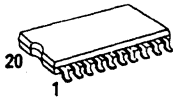

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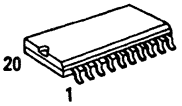
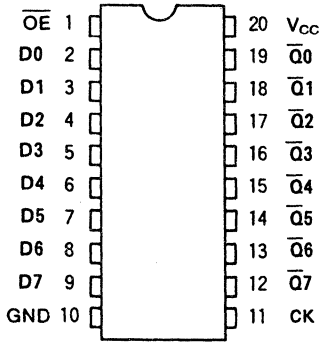


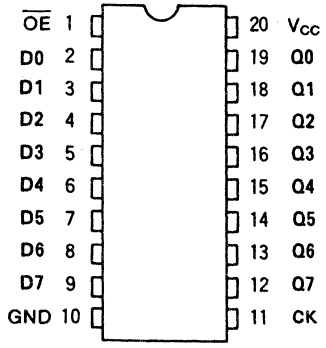
FW(SOL20-P-300)

PIN ASSIGNMENT

TC74HC564A



TC74HC574A

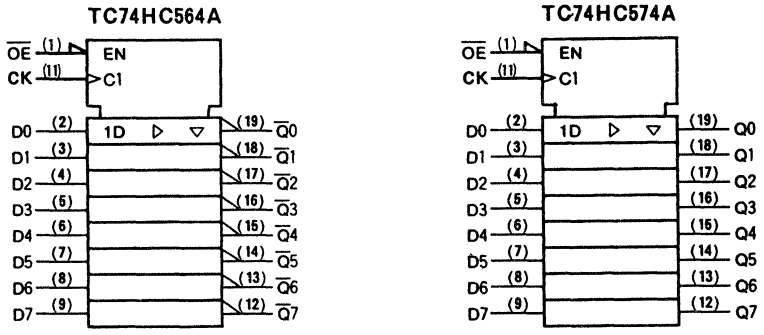


TRUTH TABLE

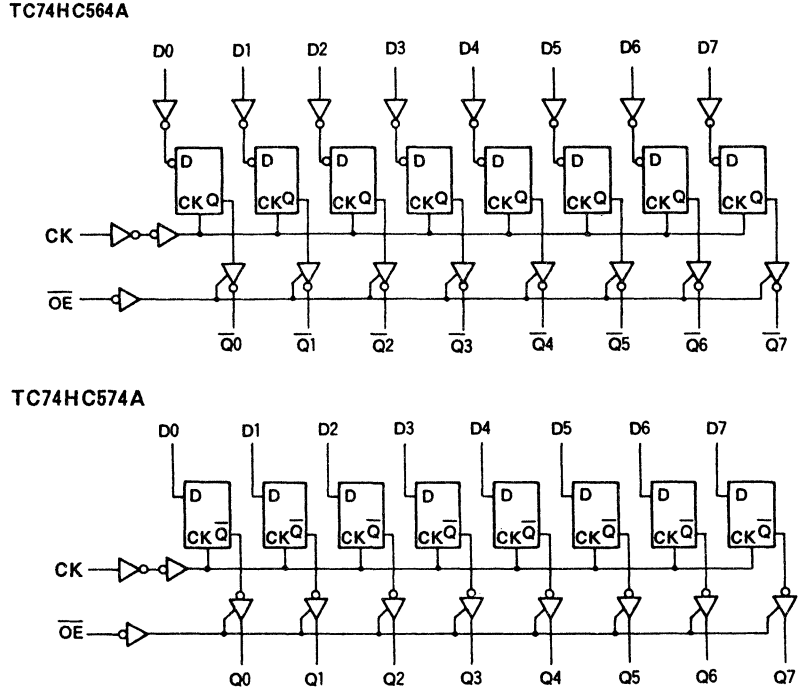
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(574A)	$\overline{Q}$(564A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n(Q_n) : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Dn)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time (Dn)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	24	
			6.0	−	36	28	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	2.0	−	70	150	−	190	
				4.5	−	20	30	−	38	
				6.0	−	15	26	−	33	
			150	2.0	−	88	190	−	240	
				4.5	−	25	38	−	48	
				6.0	−	19	33	−	41	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	48	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	12	21	−	26	
			150	2.0	−	60	165	−	205	
				4.5	−	20	33	−	41	
				6.0	−	16	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	34	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	15	21	−	26	
Maximum Clock Frequency	f_{MAX}		50	2.0	6	17	−	5	−	
				4.5	31	50	−	24	−	
				6.0	36	59	−	28	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)				−	54	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per bit})$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

$$C_{PD}(\text{total})=39+15 \cdot n$$

TC74HCT564AP/AF
TC74HCT574AP/AF

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

TC74HCT564AP/AF INVERTING
TC74HCT574AP/AF NON-INVERTING

The TC74HCT564A and HCT574A are high speed CMOS OCTAL FLIP-FLOPs with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

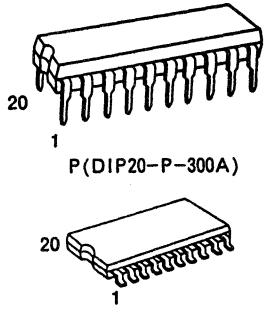
These 8-bit D-type flip-flops are controlled by a clock input (CK) and an output enable input ($\overline{OE}$).

The TC74HCT564A has inverting outputs, and the TC74 HCT574A has non-inverting outputs.

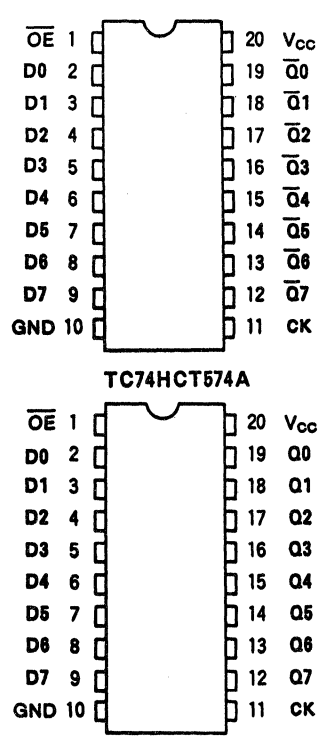
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=62MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL outputs ····· V_{IH} = 2 V(Max.)
  V_{IL} =0.8V(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS564/574



PIN ASSIGNMENT

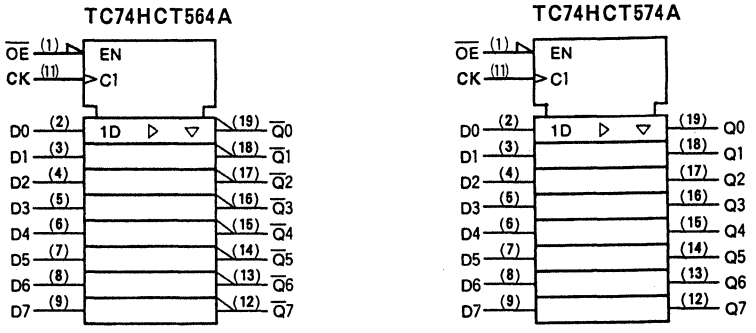


TRUTH TABLE

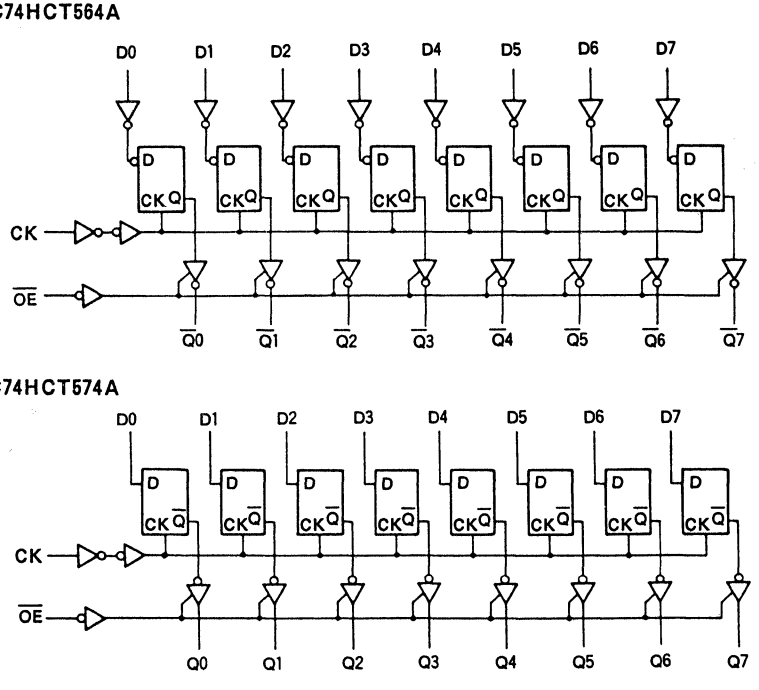
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(T574A)	$\overline{Q}$(T564A)
H	X	X	Z	Z
L	↓	X	Q_n	$\overline{Q_n}$
L	↑	L	L	H
L	↑	H	H	L

X : Don't Care
Z : High Impedance
Q_n($\overline{Q_n}$) : No Change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−		μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	PER INPUT: V_{IN}=0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		4.5 5.5	− −	15 14	19 17	ns
Minimum Set−up Time (Dn)	t_s		4.5 5.5	− −	15 14	19 17	
Minimum Hold Time (Dn)	t_h		4.5 5.5	− −	0 0	0 0	
Clock Frequency	f		4.5 5.5	− −	31 34	25 27	MHz

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	4.5 5.5	− −	7 6	12 11	− −	15 14	ns
Propagation Delay Time (CK−Q, $\overline{Q}$)	t_{pLH} t_{pHL}		50	4.5 5.5	− −	19 16	30 27	− −	38 34	
			150	4.5 5.5	− −	24 21	40 35	− −	48 44	
Output Enable time	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	4.5 5.5	− −	19 16	30 27	− −	38 34	
			150	4.5 5.5	− −	24 21	40 35	− −	48 44	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5 5.5	− −	19 16	30 27	− −	38 34	
Maximum Clock Frequency	f_{MAX}		50	4.5 5.5	− −	50 60	31 34	− −	25 27	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT564A			−	65	−	−	−	
		TC74HCT574A			−	62	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

And the total C_{PD} when n pcs. of Flip Flop operate can be gained by the following equation:

C_{PD}(total)=51+14 • n(TC74HCT564A)

C_{PD}(total)=47+15 • n(TC74HCT574A)

NOTES

NOTES

TC74HC590AP/AF

8-BINARY COUNTER/REGISTER WITH 3-STATE OUTPUTS

The TC74HC590A is a high speed CMOS 8-BIT COUNTER/REGISTER fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

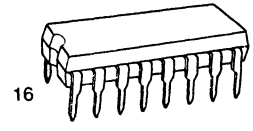
The internal counter counts on the positive going edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is low. When Counter Clear ($\overline{CCLR}$) is low, the internal counter is cleared asynchronously to the clock.

Data in the internal counter are loaded into the register at positive going edge of Register Clock (RCK), and the register outputs are countrolled by enable input ($\overline{G}$).

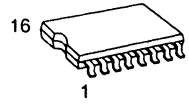
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=62MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For $\overline{RCO}$
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For $\overline{RCO}$
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS590

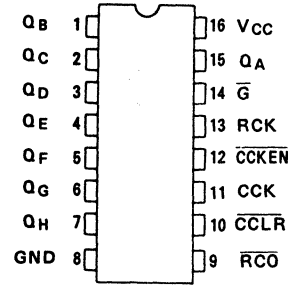


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

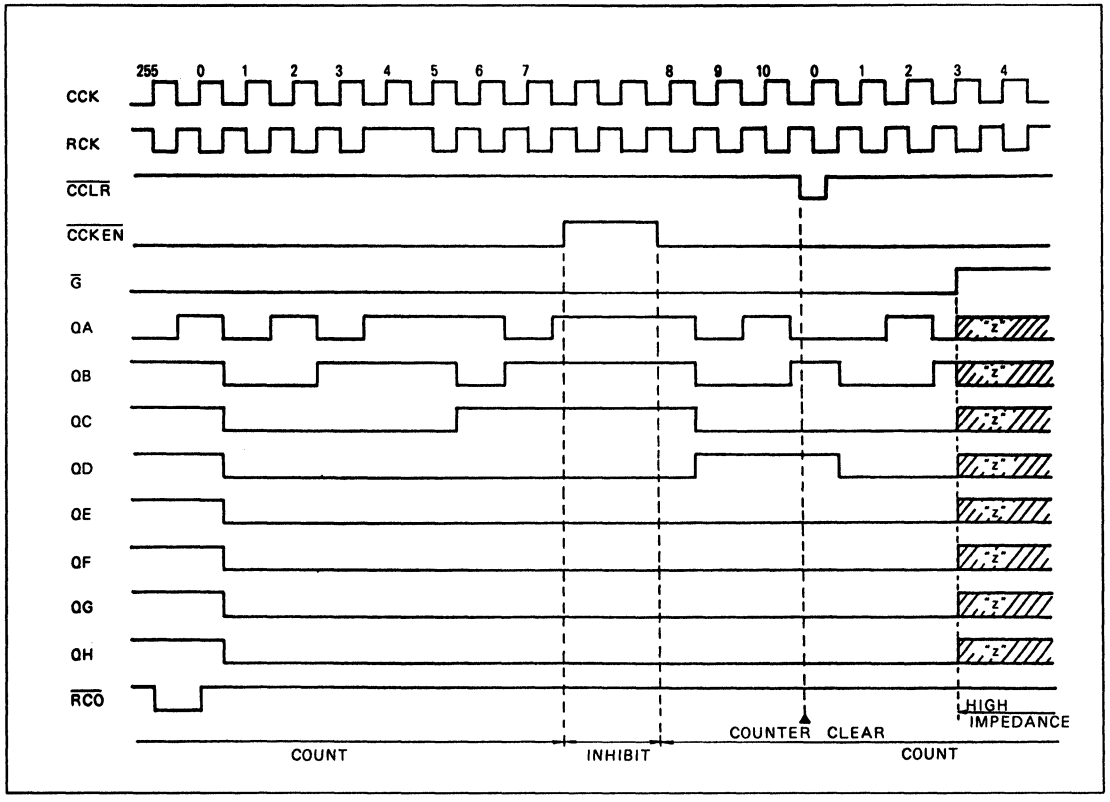
INPUT					FUNCTION
G	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q OUTPUTS DISABLE
L	X	X	X	X	Q OUTPUTS ENABLE
X	↑	X	X	X	COUNTER DATA IS STORED INTO REGISTER.
X	↓	X	X	X	REGISTER STATE IS NOT CHANGED.
X	X	L	X	X	COUNTER CLEAR
X	X	H	L	↑	ADVANCE ONE COUNT.
X	X	H	L	↓	NO COUNT
X	X	H	H	X	NO COUNT

X:Don't care

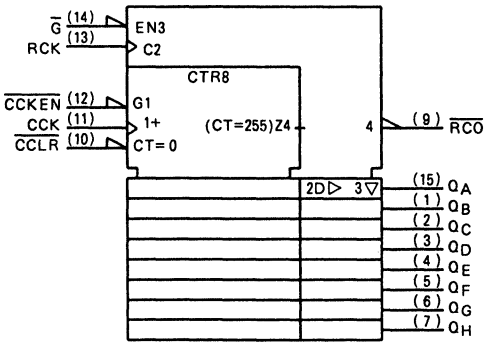
$\overline{RCO}=QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'$

(QA'~QH':Internal outputs of the counter)

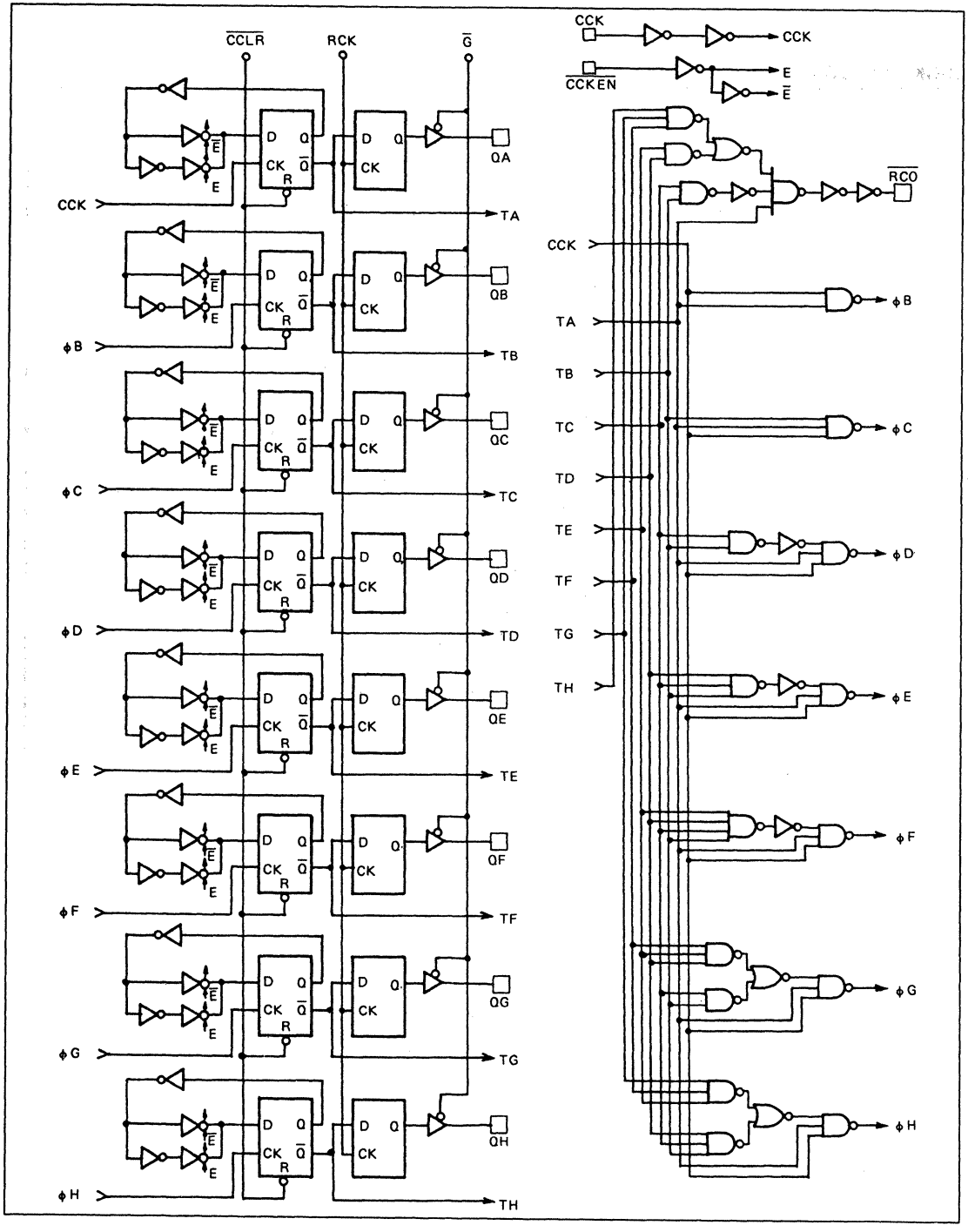
TIMING CHART



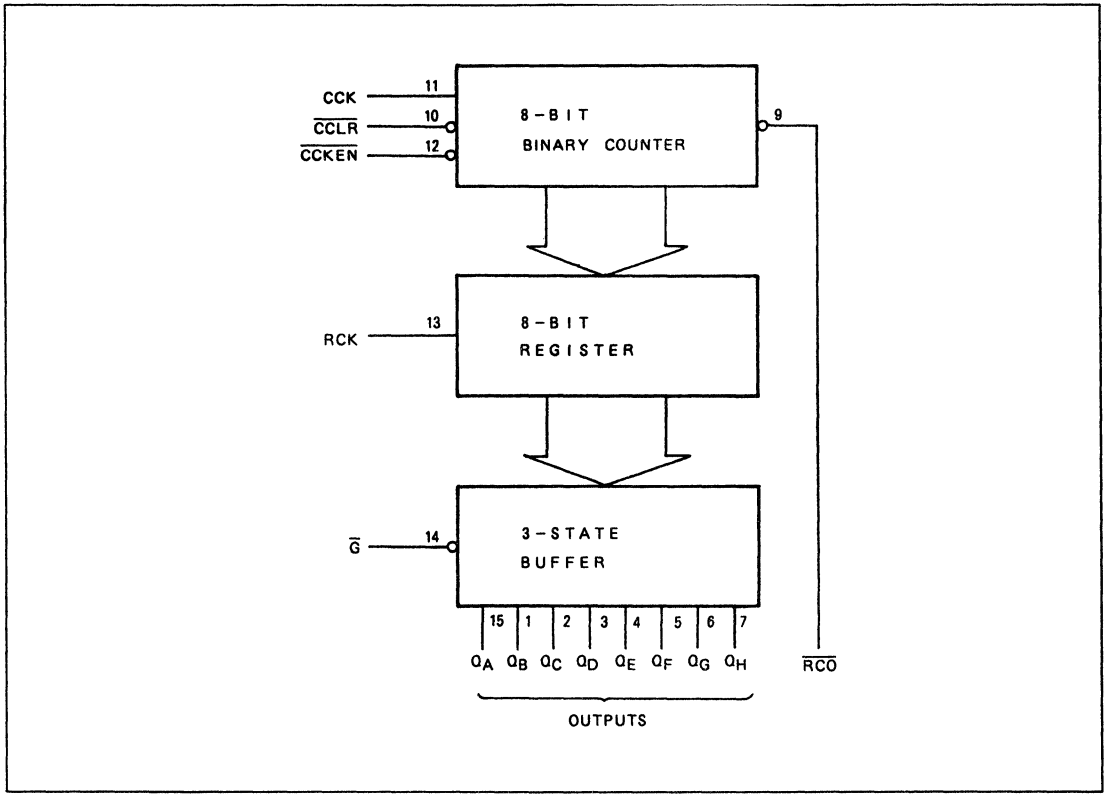
IEC LOGIC SYMBOL



LOGIC DIAGRAM



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current ($\overline{RCO}$) / (Q_A~Q_H)	I_{OUT}	±25 / ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		$\overline{RCO}$	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_A~Q_H	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		$\overline{RCO}$	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_A~Q_H	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CCK,RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time ($\overline{CCKEN}$-CCK)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set-up Time (CCK-$\overline{RCK}$)	t_s		2.0	−	200	250	
			4.5	−	40	50	
			6.0	−	34	43	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	33	26	
			6.0	−	39	31	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (CCK–$\overline{RCO}$)	t_{pLH} t_{pHL}		–	18	28	
Propagation Delay Time (CCK–$\overline{RCO}$)	t_{pLH}		–	20	30	
Maximum Clock Frequency	f_{MAX}		32	62	–	MHz

AC ELECTRICAL CHARACTERISTICS(C_L =50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time (Qn)	t_{TLH} t_{THL}		50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		50	2.0	–	30	75	–	95	
				4.5	–	8	15	–	19	
				6.0	–	7	13	–	16	
Propagation Delay Time (CCK–$\overline{RCO}$)	t_{pLH} t_{pHL}		50	2.0	–	75	163	–	205	
				4.5	–	22	33	–	41	
				6.0	–	17	28	–	35	
Propagation Delay Time ($\overline{CCLR}$–$\overline{RCO}$)	t_{pLH}		50	2.0	–	78	175	–	220	
				4.5	–	23	35	–	44	
				6.0	–	18	30	–	37	
Propagation Delay Time (RCK–Qn)	t_{pLH} t_{pHL}		50	2.0	–	62	145	–	180	
				4.5	–	19	29	–	36	
				6.0	–	15	25	–	31	
			150	2.0	–	78	185	–	230	
				4.5	–	24	37	–	46	
				6.0	–	19	31	–	39	
Output Enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	–	43	105	–	130	
				4.5	–	14	21	–	26	
				6.0	–	12	18	–	22	
			150	2.0	–	58	150	–	190	
				4.5	–	19	30	–	38	
				6.0	–	16	26	–	33	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	–	33	105	–	130	
				4.5	–	16	21	–	26	
				6.0	–	12	18	–	22	
Maximum Ciock Frequency	f_{MAX}		50	2.0	6	12	–	5	–	MHz
				4.5	30	51	–	24	–	
				6.0	35	80	–	28	–	
Input Capacitance	C_{IN}				–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)				–		–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

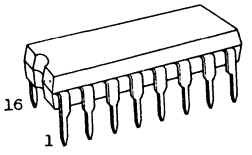
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC592P 8-BIT BINARY COUNTER WITH INPUT REGISTER

The TC74HC592 is a high speed CMOS 8-bit register/counter fabricated with silicon gate C^2MOS technology.
It achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The internal counter counts at positive edge of Counter Clock (CCK) when Counter Clock Enable ($\overline{CCKEN}$) is held "L" level.
If Counter clear ($\overline{CCLR}$) is held "L", the internal counter is cleared asynchronous to clock.
Input A∿H are loaded to register at positive edge of Register Clock (RCK), and register outputs are loaded to Counter when Counter Load ($\overline{CLOAD}$) is held "L" level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=38MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with LSTTL(74LS592)



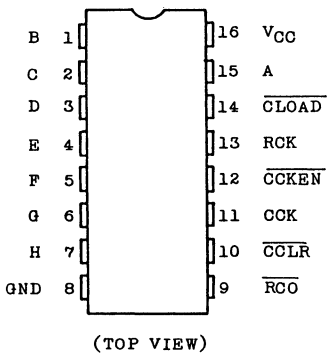
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

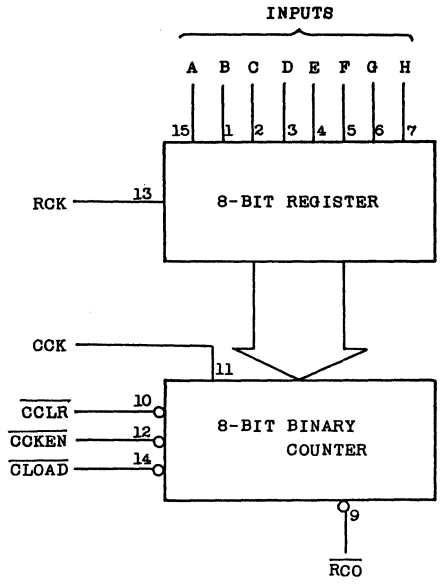
INPUTS					FUNCTION
RCK	$\overline{CLOAD}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
X	L	H	X	X	REGISTER DATA IS LOADED INTO COUNTER.
X	H	L	X	X	COUNTER CLEAR
↑	H	H	X	X	THE DATA OF A THRU H INPUTS IS STORED INTO REGISTER
↓	H	H	X	X	REGISTER STATE IS NOT CHANGED.
X	H	H	L	↑	COUNTER ADVANCES THE COUNT.
X	H	H	L	↓	NO COUNT
X	H	H	H	X	NO COUNT

X: Don't care

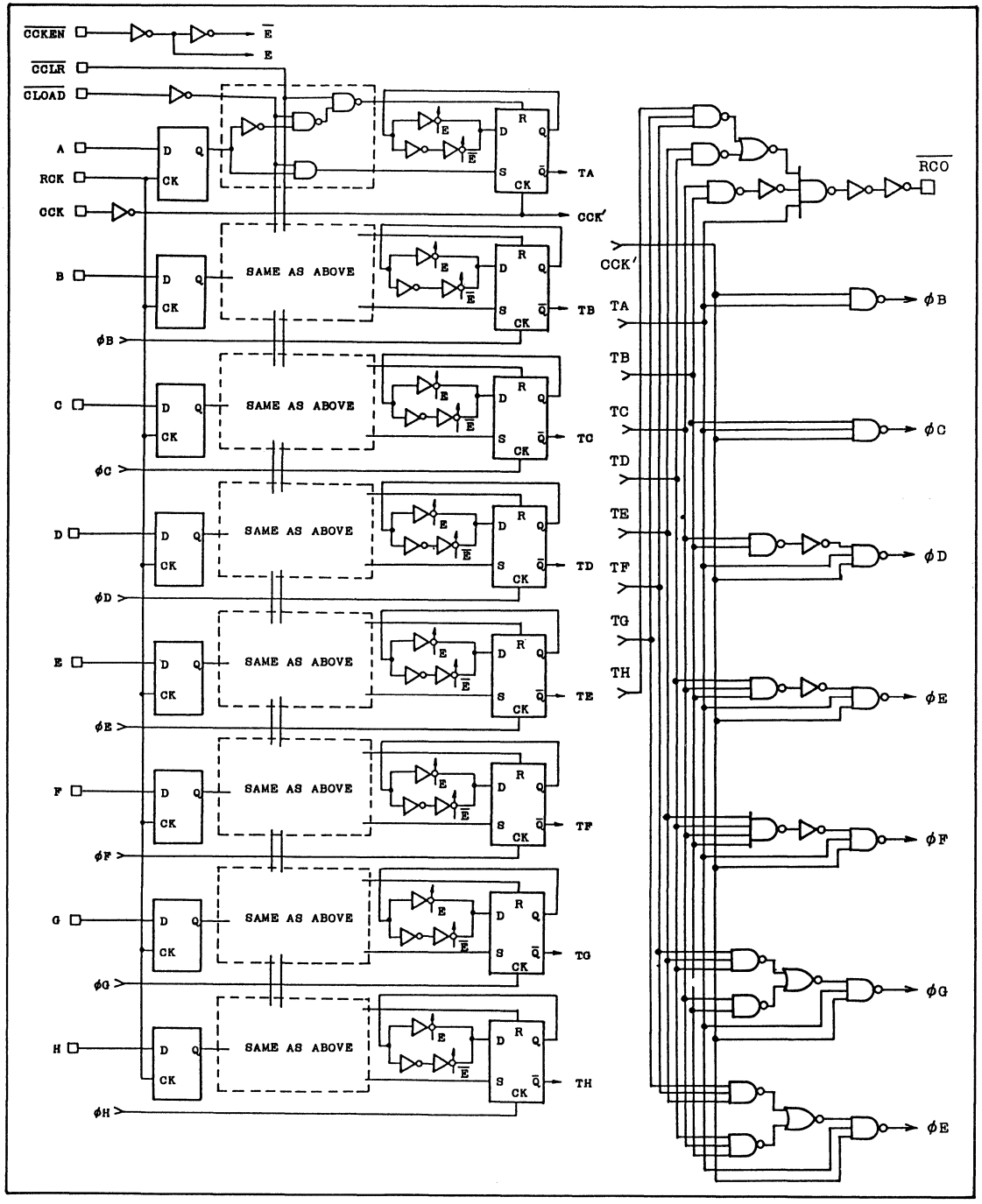
$\overline{RCO}=\overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH'}$

(QA' ∿ QH'; Internal outputs of the counter)

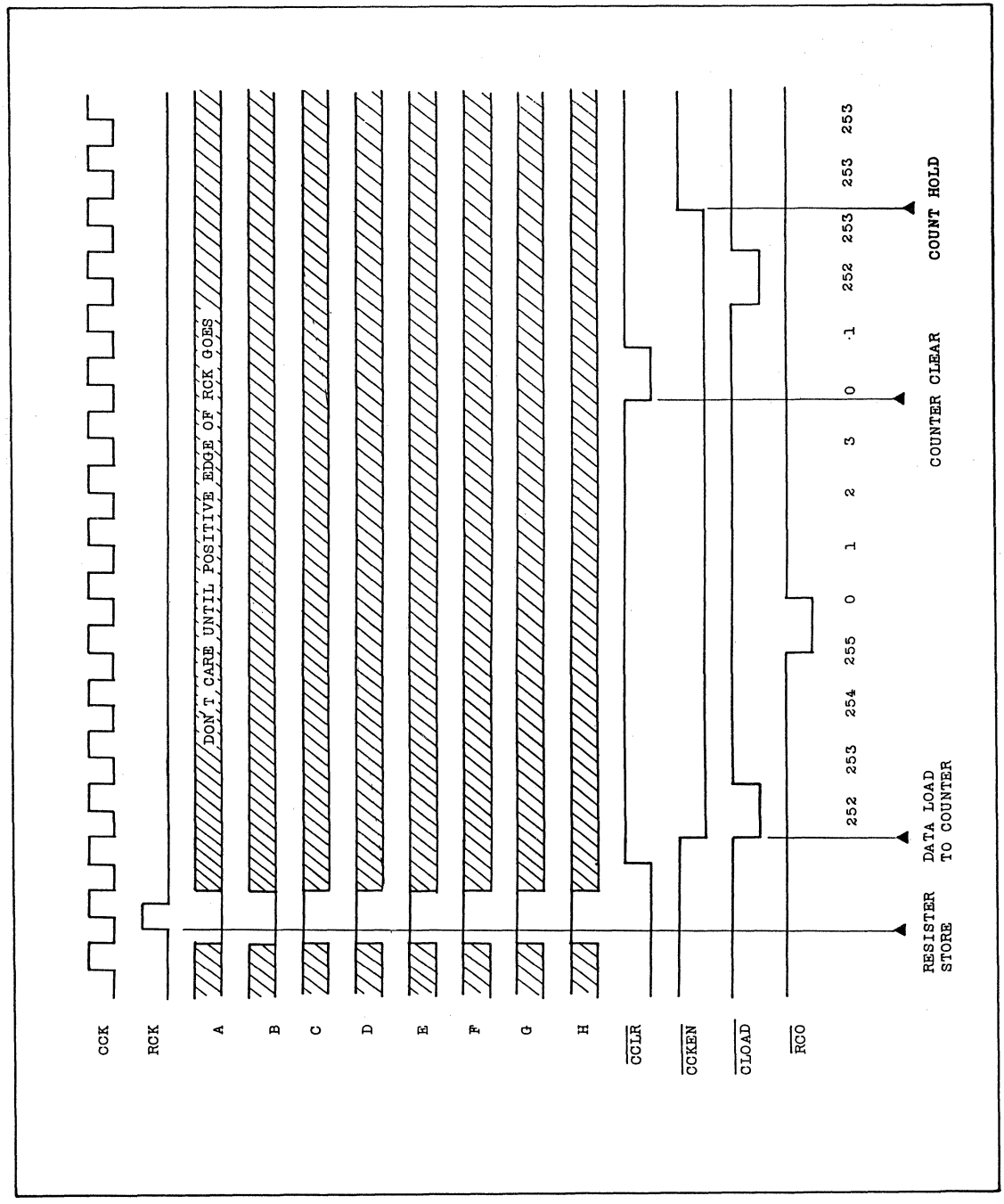
BLOCK DIAGRAM



LOGIC DIAGRAM



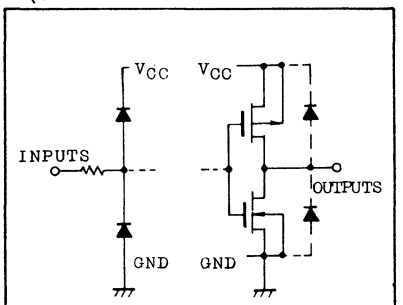
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CLOAD}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	164	315	-	395	
			4.5	-	41	63	-	79	
			6.0	-	35	54	-	67	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pLH}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (RCK - $\overline{RCO}$)	t_{pLH} t_{pHL}	$\overline{CLOAD}$="L"	2.0	-	188	360	-	450	
			4.5	-	47	72	-	90	
			6.0	-	40	61	-	77	
Maximum Clock Frequency	f_{MAX}		2.0	4	9	-	3.5	-	MHz
			4.5	22	34	-	18	-	
			6.0	26	42	-	21	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Pulse Width ($\overline{CLOAD}$)	$t_{w(L)}$		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Removal Time ($\overline{CLOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Set-up Time ($\overline{CCKEN}$ - CCK)	t_s		2.0	-	32	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	17	-	16	
Minimum Set-up Time (RCK - $\overline{CLOAD}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Set-up Time (A∿H - RCK)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

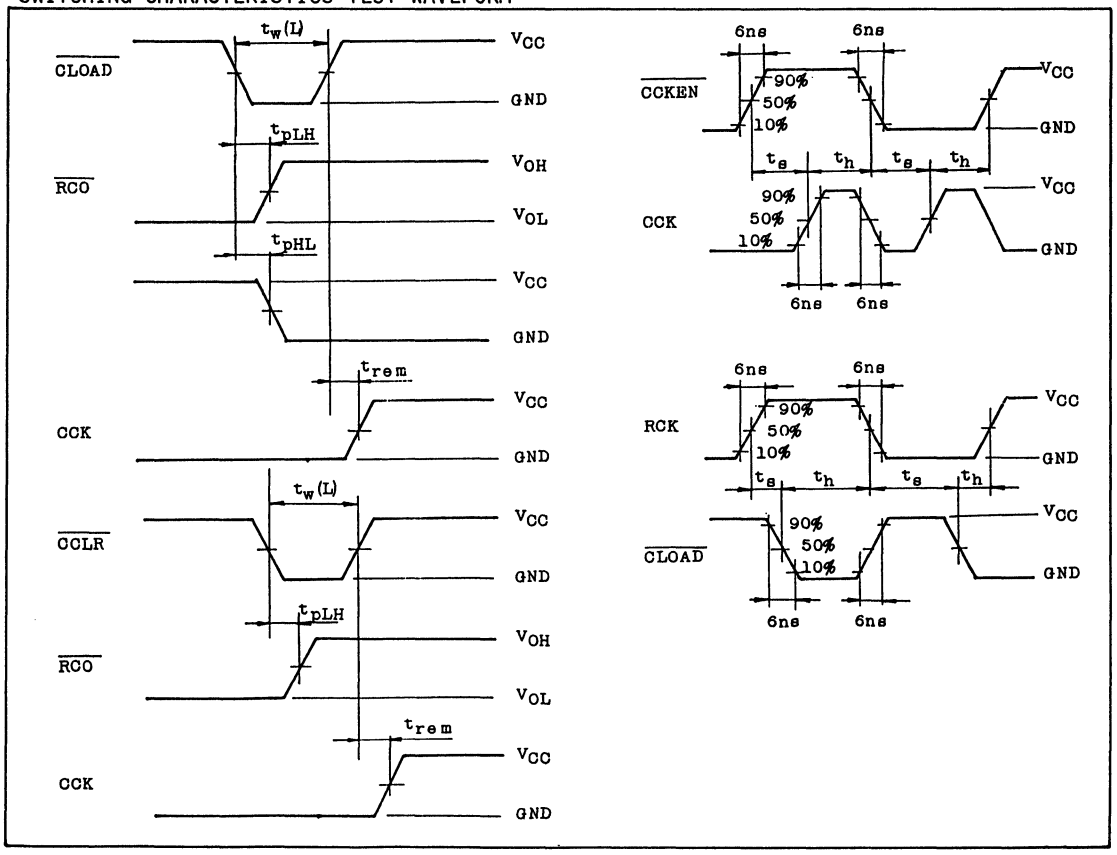
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Hold Time	t_h		2.0	-	-	25	-	30	ns
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	44	-	-	-	

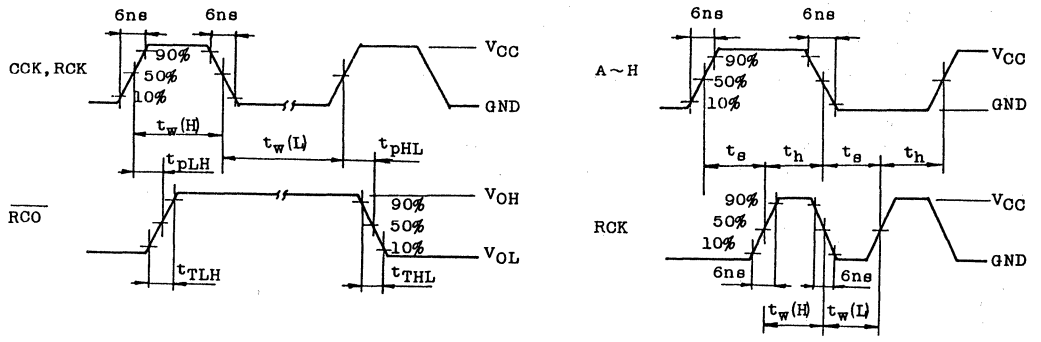
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

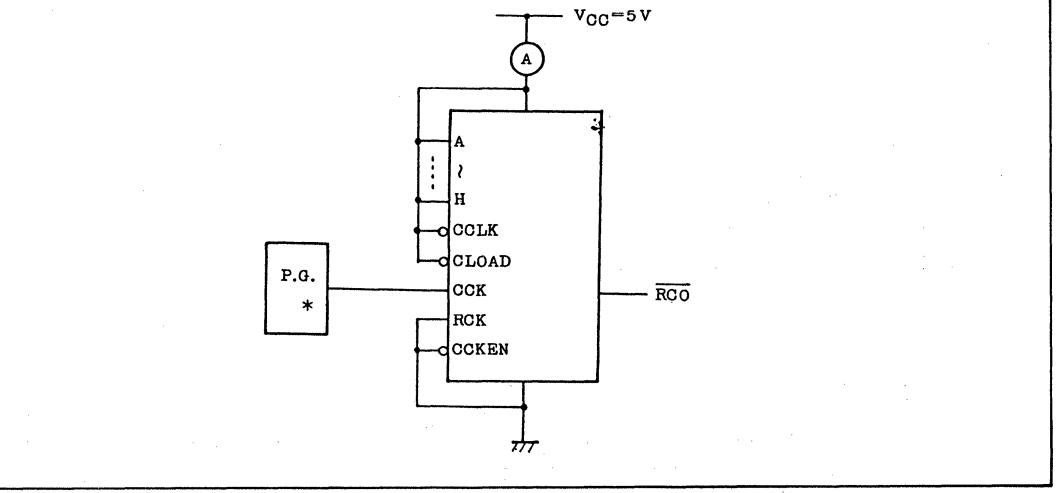
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT



8-BIT SHIFT REGISTER/LATCH(3-STATE)

The TC74HC595A is a high speed 8-BIT SHIFT REGISTER/LATCH fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

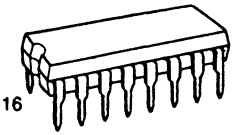
The TC74HC595A contains an 8-bit static shift register which feeds an 8-bit storage register.

Shift operation is accomplished on the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independent, parallel outputs can be held stable during the shift operation. And, since the parallel outputs are 3-state, it can be directly connected to 8-bit bus. This register can be used in serial-to-parallel conversion, data receivers, etc.

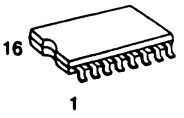
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

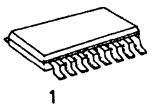
FEATURES:

- High Speed ····· f_{MAX}=55MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QH
  10 LSTTL Loads For QH'
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.) For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QH'
- Balanced Propaation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS595



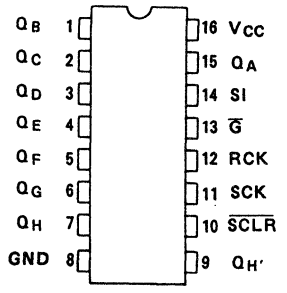
P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



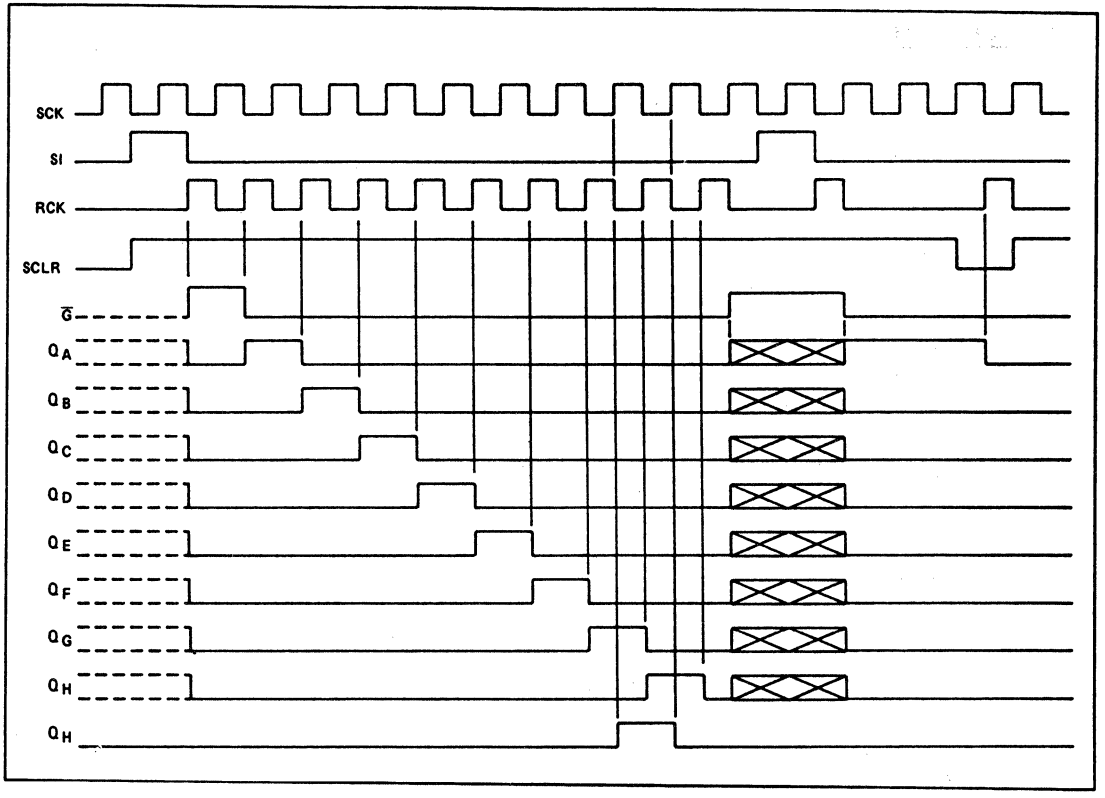
(TOP VIEW)

TRUTH TABLE

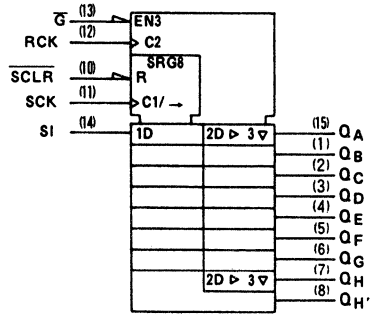
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

X : DON'T CARE

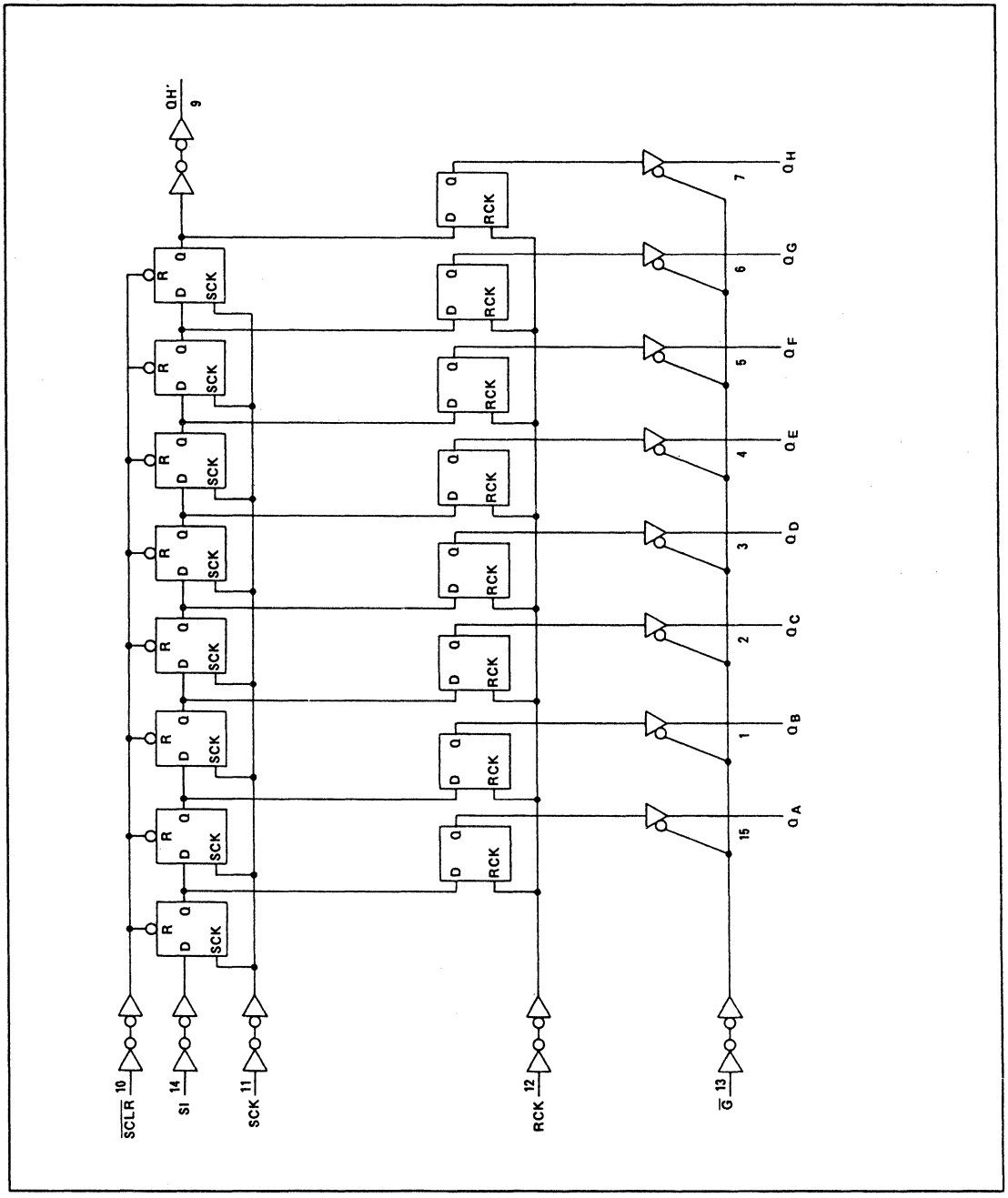
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current ($Q_{H'}$) / (Q_A~Q_H)	I_{OUT}	±25 / ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		$Q_{H'}$	I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_A~Q_H	I_{OH} = −6 mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH} = −7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		$Q_{H'}$	I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_A~Q_H	I_{OL} = 6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SCK,RCK)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SI−SCK)	t_s		2.0	−	50	165	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (SCK−RCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time ($\overline{SCLR}$−RCK)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{SCLR}$)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	25	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Q_H')	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (SCK–Q_H')	t_{pLH} t_{pHL}		–	12	21	ns
Propagation Delay Time ($\overline{SCLR}$–Q_H')	t_{pLH} t_{pHL}		–	15	30	ns
Maximum Clock Frequency	f_{MAX}		35	77	–	MHz

AC ELECTRICAL CHARACTERISTICS(C_L =50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=–40 ~85℃ MIN.	Ta=–40 ~85℃ MAX.	UNIT
Output Transition Time (Qn)	t_{TLH} t_{THL}		50	2.0	–	25	60	–	75	ns
				4.5	–	7	12	–	15	
				6.0	–	6	10	–	13	
Output Transition Time (Q_H')	t_{TLH} t_{THL}		50	2.0	–	30	75	–	95	
				4.5	–	8	15	–	19	
				6.0	–	7	13	–	16	
Propagation Delay Time (SCK–Q_H')	t_{pLH} t_{pHL}		50	2.0	–	45	125	–	155	
				4.5	–	15	25	–	31	
				6.0	–	13	21	–	26	
Propagation Delay Time ($\overline{SCLR}$–Q_H')	t_{pLH} t_{pHL}		50	2.0	–	60	175	–	220	
				4.5	–	18	35	–	44	
				6.0	–	15	30	–	37	
Propagation Delay Time (RCK–Qn)	t_{pLH} t_{pHL}		50	2.0	–	60	150	–	190	
				4.5	–	20	30	–	38	
				6.0	–	17	26	–	32	
			150	2.0	–	75	190	–	240	
				4.5	–	25	38	–	48	
				6.0	–	22	32	–	41	
Output Enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	2.0	–	45	135	–	170	
				4.5	–	15	27	–	34	
				6.0	–	13	23	–	29	
			150	2.0	–	60	175	–	220	
				4.5	–	20	35	–	44	
				6.0	–	17	30	–	37	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	–	30	150	–	190	
				4.5	–	15	30	–	38	
				6.0	–	14	26	–	33	
Maximum Ciock Frequency	f_{MAX}		50	2.0	6	17	–	5	–	MHz
				4.5	30	50	–	25	–	
				6.0	35	59	–	28	–	
Input Capacitance	C_{IN}				–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)				–	184	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

8-BIT LATCH/SHIFT REGISTER(3-STATE)

The TC74HC597A is a high speed CMOS 8-BIT PARALLEL-IN/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate C^2MOS technology.

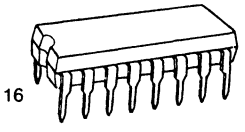
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of an 8-bit data register feeding an 8-bit shift register. The parallel data on the A-H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{SLOAD}$ input is held low, the input register data is passed into the shift registers. When $\overline{SLOAD}$ input is held high, the serial data input (SI) is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear input ($\overline{SCLR}$) sets the 8-bit shift register to zero.

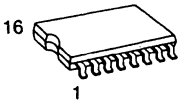
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 74LS597

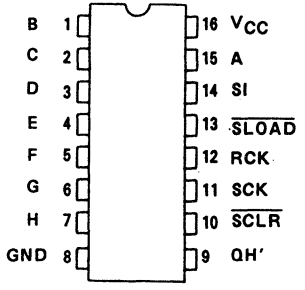


P(DIP16-P-300A)



F(SOP16-P-300)

PIN ASSIGNMENT



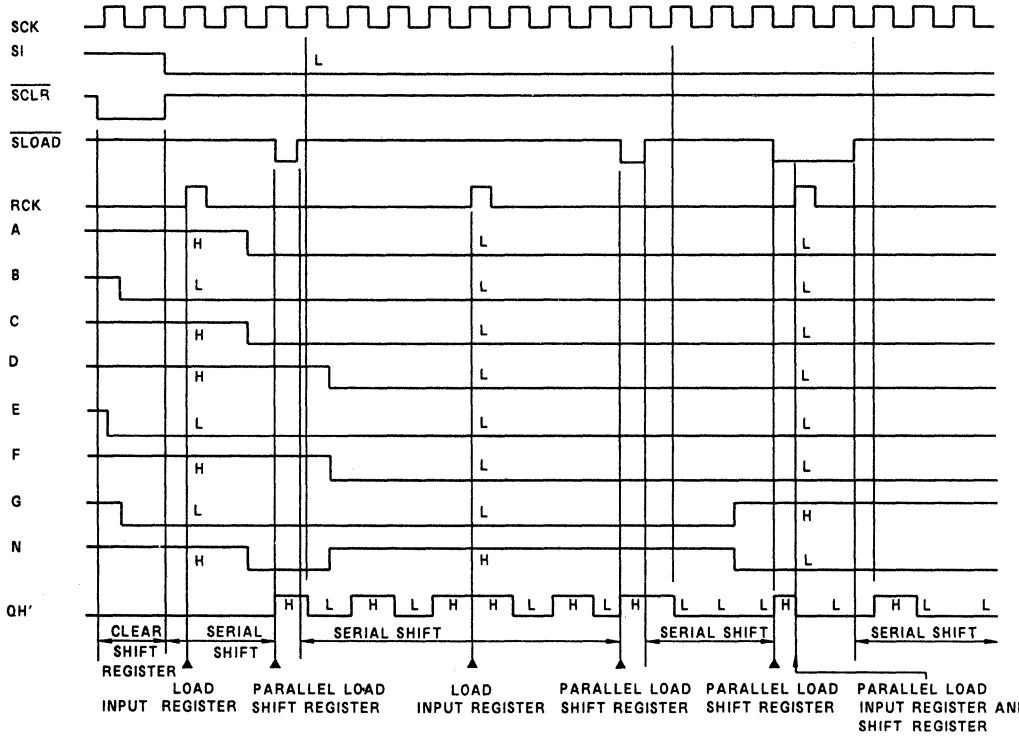
(TOP VIEW)

TRUTH TABLE

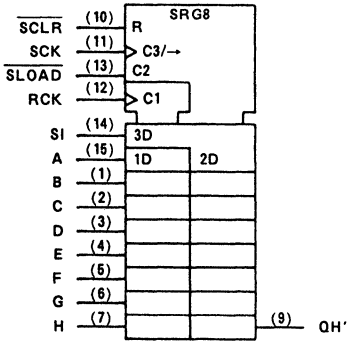
INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S. R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S. R.
L	↑	H	H	X	First stage of S. R. become "L". Other stages store the data of previous stage, respectively.
H	↑	H	H	X	First stage of S. R. become "H". Other stages store the data of previous stage, respectively.
X	↓	H	H	X	State of S. R. is not changed.
X	X	X	X	↑	Input data on A~H line is stored into input register
X	X	X	X	↓	Storage register state is not changed.

X : DON'T CARE

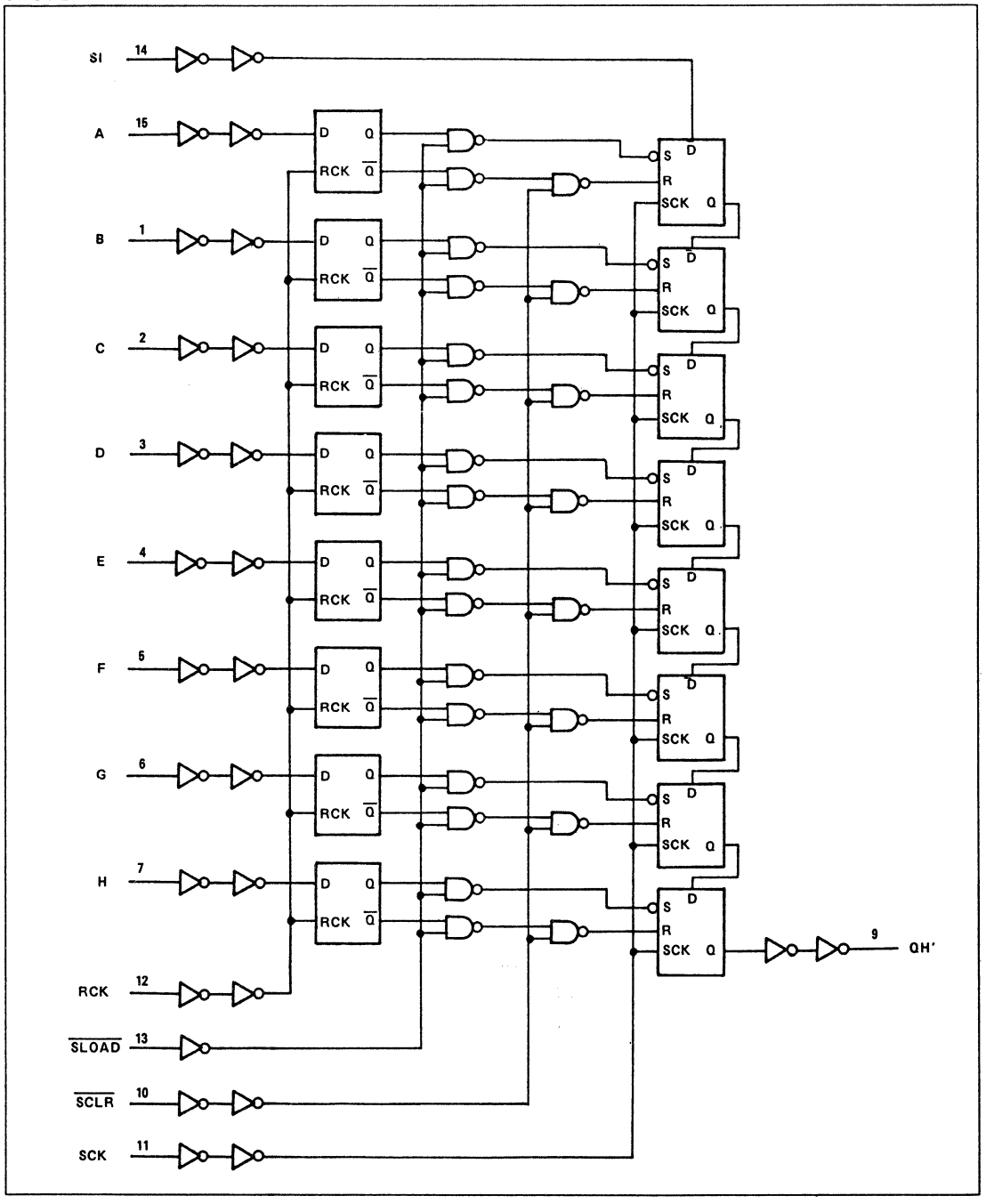
TIMING CHART



IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(FMP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (SCK, RCK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SLOAD}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (RCK−$\overline{SLOAD}$)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Set−up Time (SI−SCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (PI−RCK)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time ($\overline{SCLR}$, $\overline{SLOAD}$)	t_{rem}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	5	8	ns
Propagation Delay Time (SCK−QH')	t_{pLH} t_{pHL}		−	16	25	
Propagation Delay Time ($\overline{SCLR}$−QH')	t_{pLH} t_{pHL}		−	20	32	
Propagation Delay Time ($\overline{SLOAD}$−QH')	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (RCK−QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ ="L"	−	25	37	
Maximum Clock Frequency	f_{MAX}		30	59	−	MHz

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	32	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (SCK−QH')	t_{pLH} t_{pHL}		2.0	−	78	145	−	180	
			4.5	−	20	29	−	36	
			6.0	−	16	25	−	31	
Propagation Delay Time ($\overline{SCLR}$−QH')	t_{pLH} t_{pHL}		2.0	−	90	175	−	220	
			4.5	−	24	35	−	44	
			6.0	−	20	30	−	37	
Propagation Delay Time ($\overline{SLOAD}$−QH')	t_{pLH} t_{pHL}		2.0	−	80	175	−	220	
			4.5	−	22	35	−	44	
			6.0	−	18	30	−	37	
Propagation Delay Time (RCK−QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$ = "L"	2.0	−	112	210	−	265	
			4.5	−	30	42	−	53	
			6.0	−	24	36	−	45	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	−	5	−	MHz
			4.5	30	48	−	24	−	
			6.0	35	50	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	60	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC620AP/AF
TC74HC623AP/AF

OCTAL BUS TRANSCEIVER
TC74HC620AP/AF 3-STATE, INVERTING
TC74HC623AP/AF 3-STATE, NON-INVERTING

The TC74HC620A and TC74HC623A are high speed CMOS QUAD TRANSCEIVERS fabricated with silicon gate C^2MOS technology.

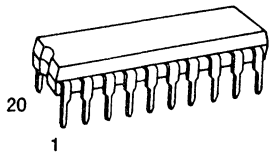
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These ICs are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by GAB, $\overline{GBA}$.

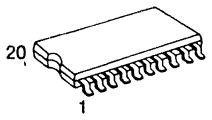
GAB and $\overline{GBA}$ inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS620,623



P(DIP20-P-300A)



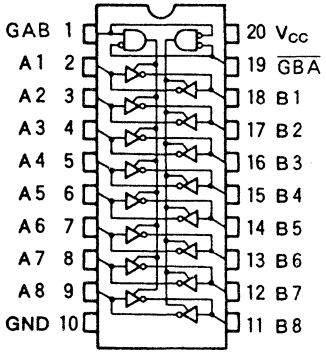
F(SOP20-P-300)

APPLICATION NOTES

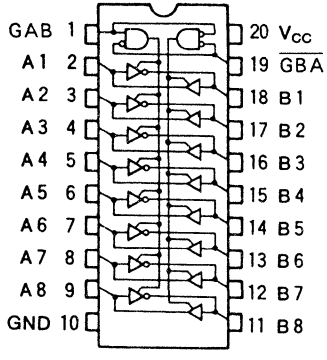
1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)

TC74HC620A

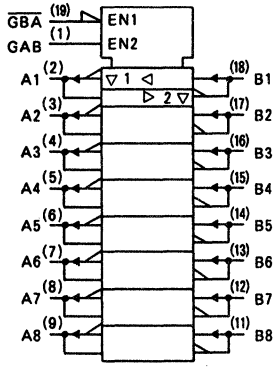


TC74HC623A

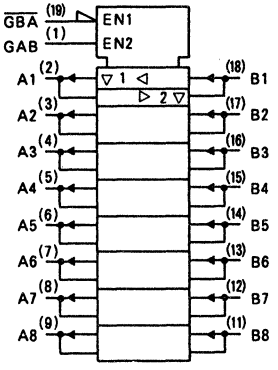


IEC LOGIC SYMBOL

TC74HC620A



TC74HC623A



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A BUS	B BUS	HC620A	HC623A
L	L	OUTPUT	INPUT	$A=\overline{B}$	A=B
H	H	INPUT	OUTPUT	$B=\overline{A}$	B=A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

Z:High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	11	−	13	
Propagation Delay Time	t_{pLH}	TC74HC620A	50	2.0	−	42	100	−	125	
				4.5	−	13	20	−	25	
				6.0	−	11	17	−	21	
	t_{pHL}		150	2.0	−	58	140	−	175	
				4.5	−	18	28	−	35	
				6.0	−	15	24	−	30	
Propagation Delay Time	t_{pLH}	TC74HC623A	50	2.0	−	38	85	−	105	
				4.5	−	12	17	−	21	
				6.0	−	10	14	−	18	
	t_{pHL}		150	2.0	−	54	125	−	155	
				4.5	−	17	25	−	31	
				6.0	−	14	21	−	26	
3−State Output Enable Time	t_{pZL}	R_L = 1 kΩ	50	2.0	−	48	150	−	190	
				4.5	−	19	30	−	38	
				6.0	−	16	26	−	33	
	t_{pZH}		150	2.0	−	61	190	−	240	
				4.5	−	24	38	−	48	
				6.0	−	20	32	−	41	
3−State Output Disable Time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	2.0	−	45	150	−	190	
				4.5	−	20	30	−	38	
				6.0	−	18	26	−	33	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC620A			−	31	−	−	−	
		TC74HC623A			−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HC646AP
TC74HC648AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HC646AP NON-INVERTING
TC74HC648AP INVERTING

The TC74HC646A/648A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

When the direction input (DIR) is held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the DIR input is held low, the A1 thru A8 become outputs and the B1 thru B8 become inputs.

The enable input $\overline{G}$ is held high, both the A Bus and B Bus become high impedance.

The select inputs (SAB, SBA) can multiplex stored and real-time (transparent mode) data.

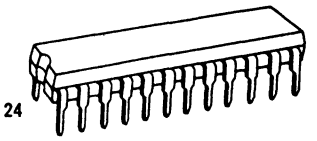
Data on the A Bus or B Bus can be clocked into the registers on the positive going transition of either CAB or CBA clock inputs, respectively.

The TC74HC646A is a non-inverting output type while the TC74HC648A is of the inverting output type.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

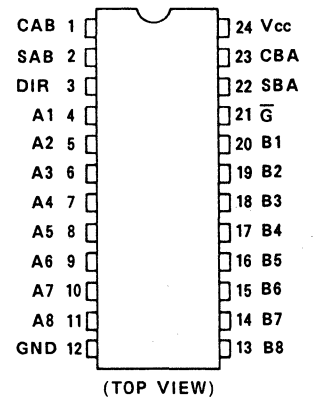
FEATURES:

- High Speed ····· f_{MAX}=73MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS646/648.



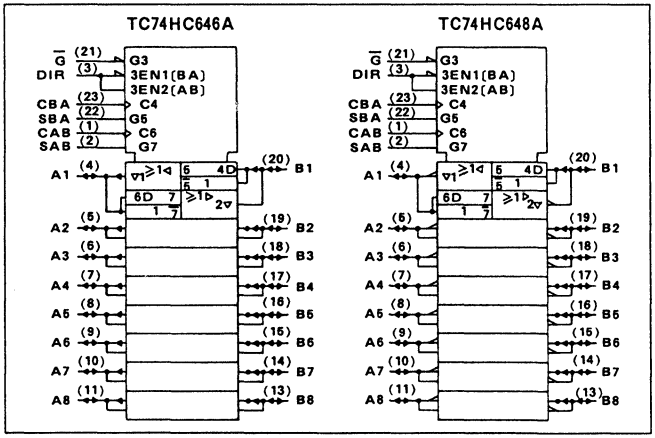
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

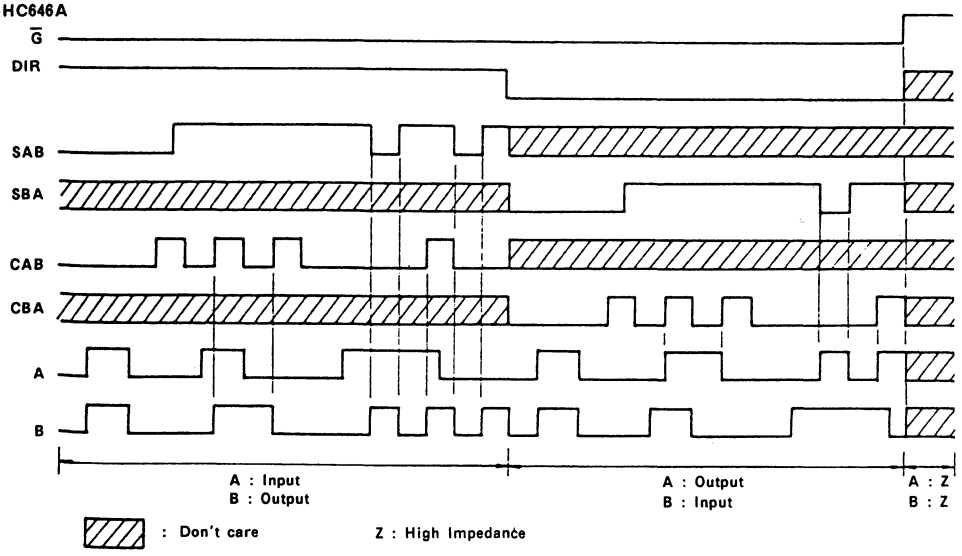
TC74HC646A (The truth table for TC74HC648A is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X	X	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip–flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip–flops on the rising edge of CAB.
		X	X*	H	X	X	Qn	The data in the A storage flip–flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip–flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip–flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip–flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip–flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes: X: Don't Care
Qn: The data stored into the internal flip–flops by most recent low to high transition of the clock inputs.
Z: High Impedance
• The clocks are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and/or B Busses may be clocked into the storage flip–flops at any time.

TIMING CHART

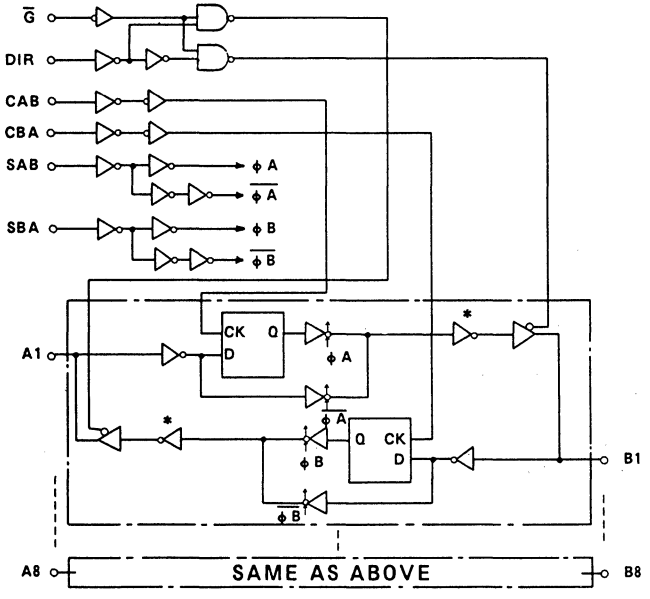
TC74HC646A



Note: The timing chart for TC74HC648A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HC648A



Note: In case of TC74HC646A output inverter marked * at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (BUS−BUS)	t_{pLH} t_{pHL}		50	2.0	−	74	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
			150	2.0	−	91	190	−	240	
				4.5	−	26	38	−	48	
				6.0	−	22	32	−	41	
Propagation Delay Time (CAB,CBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
			150	2.0	−	116	250	−	315	
				4.5	−	33	50	−	63	
				6.0	−	28	43	−	54	
Propagation Delay Time (SAB,SBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	81	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	20	29	−	37	
			150	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
Output Enable time ($\overline{G}$,DIR−BUS)	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	2.0	−	84	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	20	30	−	37	
			150	2.0	−	102	215	−	270	
				4.5	−	29	43	−	54	
				6.0	−	25	37	−	46	
Output Disable time ($\overline{G}$,DIR−BUS)	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	2.0	−	60	175	−	220	
				4.5	−	23	35	−	44	
				6.0	−	20	30	−	37	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	−	19	6	−	5	MHz
				4.5	−	67	31	−	25	
				6.0	−	79	36	−	29	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	39	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8(\text{per bit})$$

TC74HCT646AP
TC74HCT648AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HCT646AP NON-INVERTING
TC74HCT648AP INVERTING

The TC74HCT646A/HCT648A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

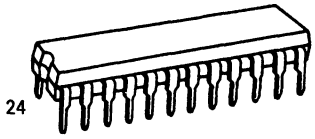
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74HCT646A is a non-inverting output type while the TC74HCT648A is of the inverting output type.

All inputs are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL Output ····· V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648



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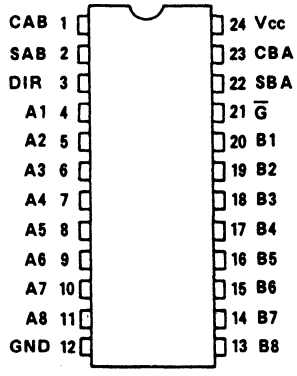
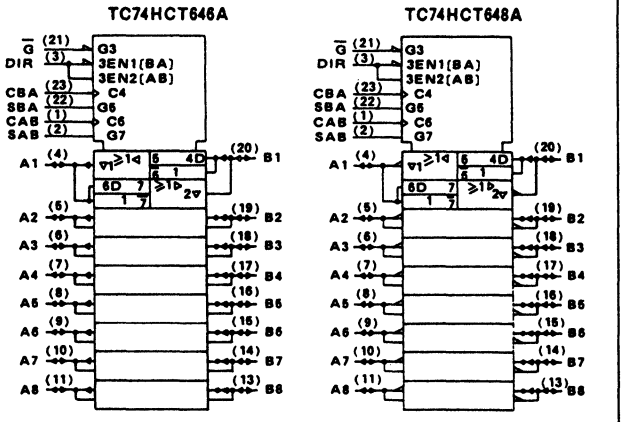
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

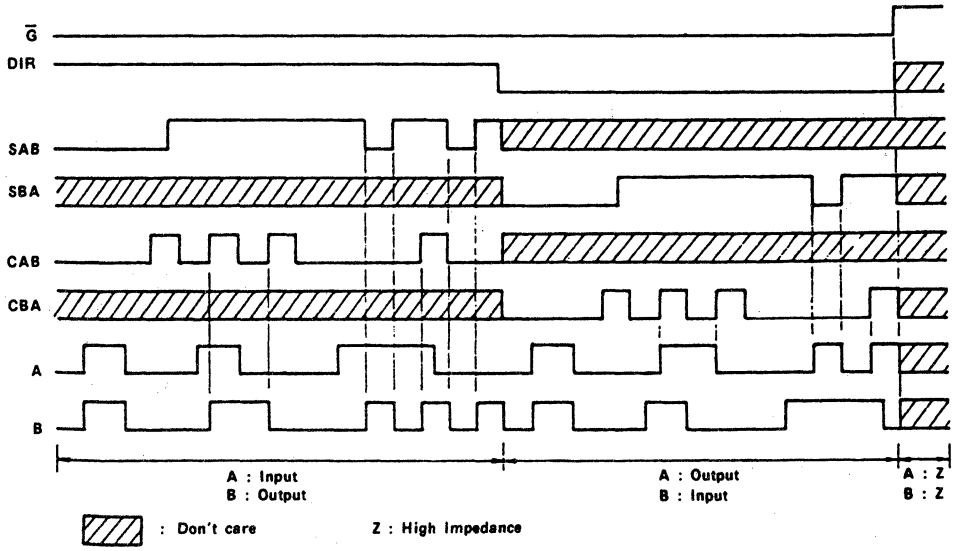
TC74HCT646A(The truth table for TC74HCT648A is the same, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
* The clock are not internally gated with either $\overline{G}$ or DIR. Therfore, data on the A and /or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

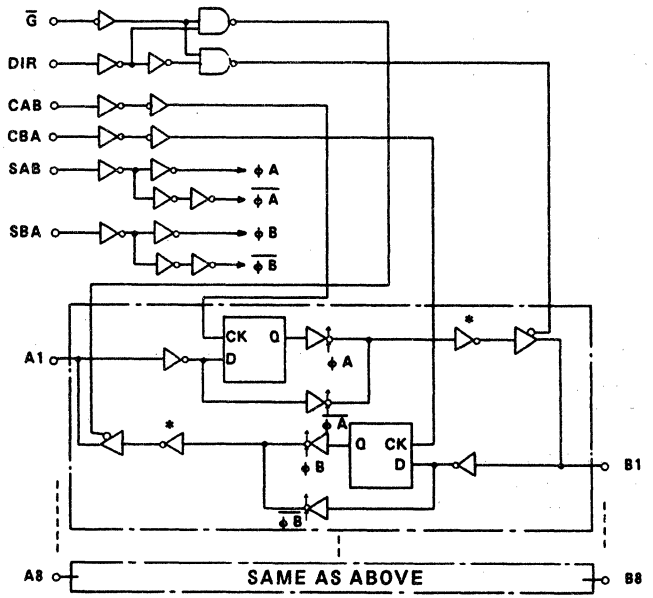
TC74HCT646A



Note: The timing chart for TC74HCT648A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HCT648A



Note: In case of TC74HCT646A output inverter marked • at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −6 μA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 6 μA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	Per input: V_{IN} = 0.5V or 2.4V, Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		4.5	−	15	19	ns
	$t_{W(H)}$		5.5	−	14	17	
Minimum Set−up Time	t_s		4.5	−	10	13	
			5.5	−	9	12	
Minimum Hold Time	t_h		4.5	−	5	5	
			5.5	−	5	5	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time (BUS−BUS)	t_{pLH}		50	4.5	−	20	30	−	38	
				5.5	−	17	27	−	34	
	t_{pHL}		150	4.5	−	25	38	−	48	
				5.5	−	22	34	−	43	
Propagation Delay Time (CAB, CBA−BUS)	t_{pLH}		50	4.5	−	29	44	−	55	
				5.5	−	26	40	−	50	
	t_{pHL}		150	4.5	−	34	52	−	65	
				5.5	−	31	47	−	59	
Propagation Delay Time (SAB, SBA−BUS)	t_{pLH}		50	4.5	−	24	34	−	43	
				5.5	−	21	31	−	39	
	t_{pHL}		150	4.5	−	29	42	−	53	
				5.5	−	26	38	−	46	
Output Enable time (DIR, $\overline{G}$−BUS)	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	26	38	−	48	
				5.5	−	23	34	−	43	
	t_{pZH}		150	4.5	−	31	46	−	58	
				5.5	−	28	41	−	52	
Output Enable time (DIR, $\overline{G}$−BUS)	t_{pLZ}	$R_L=1k\Omega$	50	4.5	−	26	35	−	44	
	t_{pHZ}			5.5	−	23	32	−	40	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	55	−	25	−	MHz
				5.5	37	61	−	30	−	
Input Capacitance	C_{IN}	DIR, $\overline{G}$, SAB, SBA, CAB, CBA			−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT646A			−	40	−	−	−	
		TC74HCT648A			−	39	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HC651AP
TC74HC652AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HC651AP INVERTING
TC74HC651AP NON-INVERTING

The TC74HC651A/652A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuiry arranged for multiplexed transmission of data directly from the internal registers.

When the enable inputs GAB and $\overline{GBA}$ are held high, the A1 thru A8 become inputs and the B1 thru B8 become outputs. When the GAB and $\overline{GBA}$ are held low, the A1 thru A8 become outputs and the B1 thru B8 become inputs. When GAB is low and $\overline{GBA}$ is high, the outputs functions of the A and B Busses are disabled.

The select inputs (SAB,SBA) can multiplex stored and real-time(transparent mode)data.

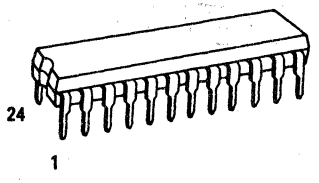
Data on the A Bus or B Bus can be clocked into the registers on the positive going transition of either CAB or CBA clock inputs, respectively.

The TC74HC651A is of the inverting output type while the TC74HC652A is a non-inverting output type.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

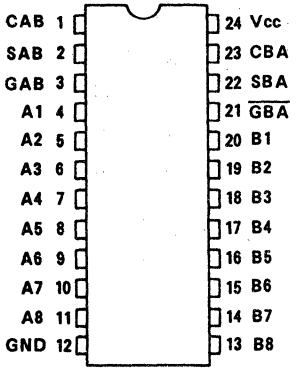
FEATURES:

- High Speed ····· f_{MAX}=73MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS651/652.



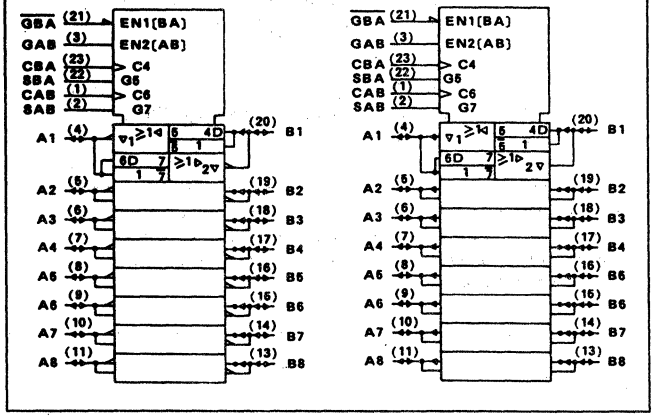
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

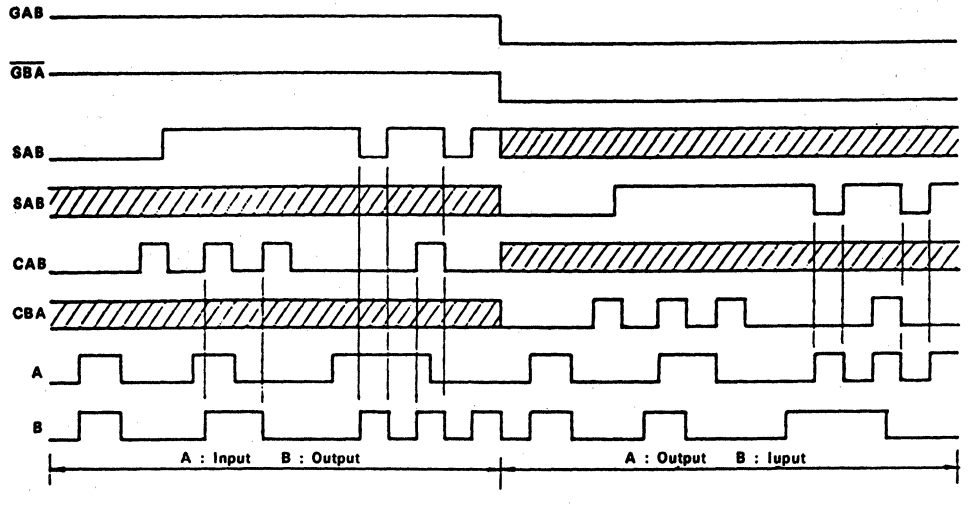
TC74HC652A (The truth table for TC74HC651A is the same, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of the A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data in the A storage flip-flops are displayed on the B Bus, and the data in the B storage flip-flops are displayed onthe A

Notes: X: Don't Care Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs. Z: High Impedance * The clocks are not internally gated with either Output Enables or Select Inputs. Therfore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

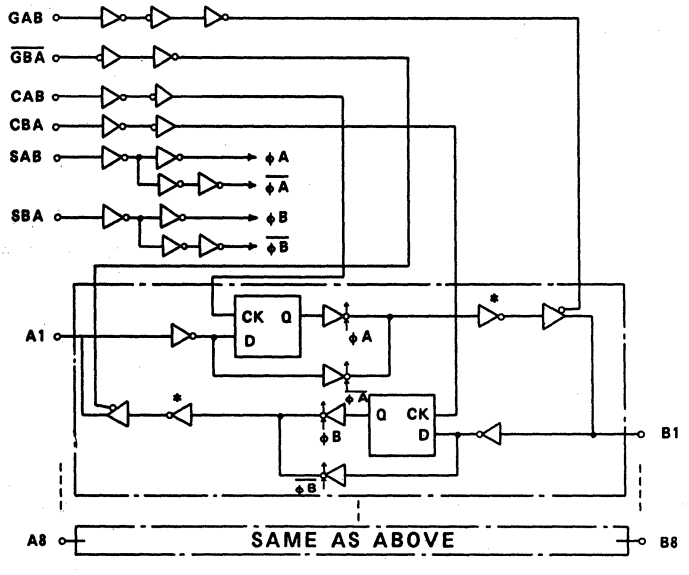
TC74HC652A



Note:The timing chart for TC74HC651A is the same,but with the outputs inverted.

SYSTEM DIAGRAM

TC74HC651A



Note: In case of TC74HC652A output inverter marked * at A bus and B bus areeliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time (BUS−BUS)	t_{pLH} t_{pHL}		50	2.0	−	74	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	18	26	−	32	
			150	2.0	−	91	190	−	240	
				4.5	−	26	38	−	48	
				6.0	−	22	32	−	41	
Propagation Delay Time (CAB,CBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
			150	2.0	−	116	250	−	315	
				4.5	−	33	50	−	63	
				6.0	−	28	43	−	54	
Propagation Delay Time (SAB,SBA−BUS)	t_{pLH} t_{pHL}		50	2.0	−	81	170	−	215	
				4.5	−	23	34	−	43	
				6.0	−	20	29	−	37	
			150	2.0	−	98	210	−	265	
				4.5	−	28	42	−	53	
				6.0	−	24	36	−	45	
Output Enable time (GAB,$\overline{GBA}$−BUS)	t_{pZL} t_{pZH}	$R_L=1k\Omega$	50	2.0	−	74	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	
			150	2.0	−	91	215	−	270	
				4.5	−	26	43	−	54	
				6.0	−	22	37	−	46	
Output Disable time (GAB,$\overline{GBA}$−BUS)	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	2.0	−	50	175	−	220	
				4.5	−	21	35	−	44	
				6.0	−	18	30	−	37	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40∼85℃ MIN.	Ta=−40∼85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	−	19	6	−	5	MHz
				4.5	−	67	31	−	25	
				6.0	−	79	36	−	29	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HCT651AP
TC74HCT652AP

OCTAL BUS TRANSCEIVER/REGISTER
TC74HCT651AP NON-INVERTING
TC74HCT652AP INVERTING

The TC74HCT651A/HCT652A are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

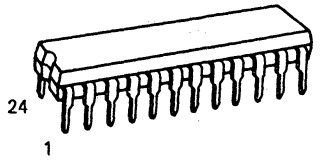
These devices are bus transceivers with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers.

The TC74HCT651A is of the inverting output type while the TC74HCT652A is a non-inverting output type.

ALL inputs are equipped with protection circuits against static dischage or transient excess voltage.

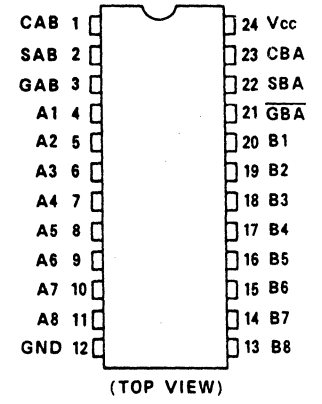
FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- Compatible with TTL Output ····· V_{IH}=2V(Min.)V_{IL}=0.8V(Max.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS651/652



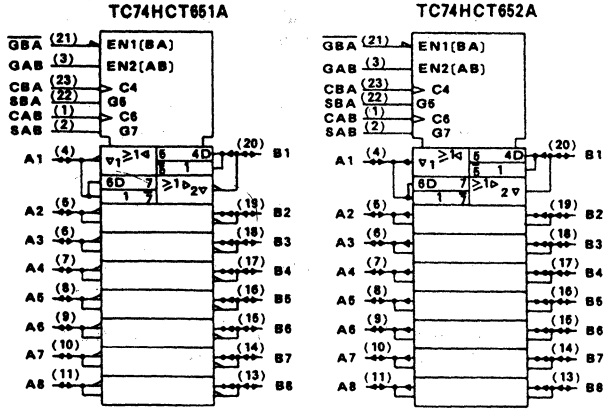
P(DIP24-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the out put mode. Damage may result.

2) All floating (high impedance) bus terminal must have their input levels fixed by means of pull up or pull down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

TRUTH TABLE

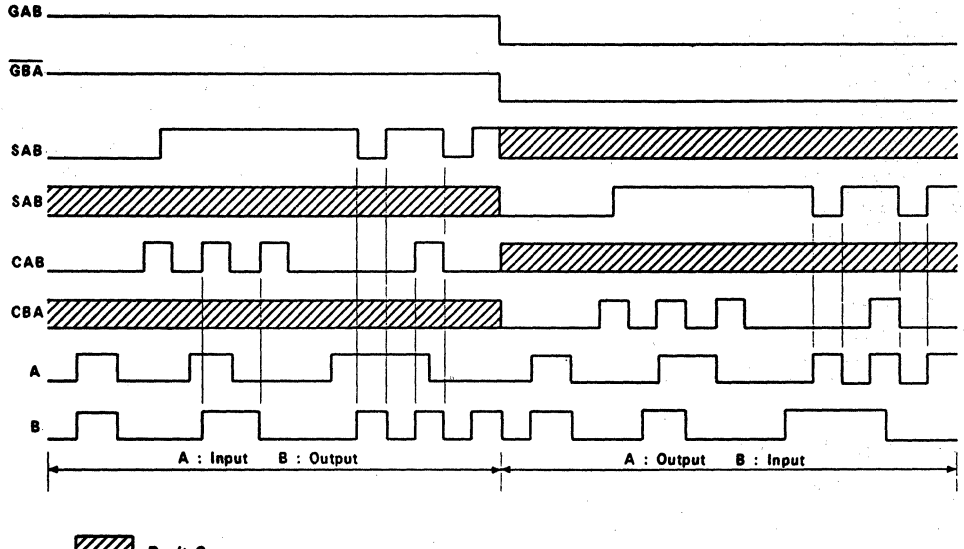
TC74HCT652A(The truth for TC74HCT651A is the same, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output funcions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flips-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus
		↓	X*	L	X	L H	L H	The data on the A Bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flip-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.

Notes : X : Don't Care
Qn : The data stored into the internal flip-flops by most recent low to high transition of the clock inputs
Z : High Impedance
* The clock are not internally gated with either GAB or GBA. Therfore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART

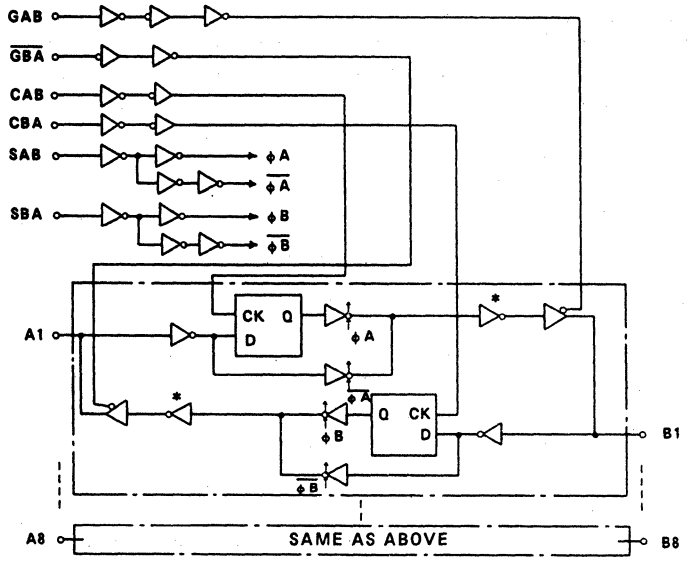
TC74HCT652A



Note : The timing chart for TC74HCT651A is the same, but with the outputs inverted.

SYSTEM DIAGRAM

TC74HCT651A



Note : In case of TC74HCT652A output inverter marked • at A bus and B bus are eliminated.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −6 μA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 6 μA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{IN} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	
	ΔI_{CC}	Per input: V_{IN} = 0.5V or 2.4V Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$		4.5	−	15	19	ns
	$t_{W(H)}$		5.5	−	14	17	
Minimum Set-up Time	t_s		4.5	−	10	13	
			5.5	−	9	12	
Minimum Hold Time	t_h		4.5	−	5	5	
			5.5	−	5	5	
Clock Frequency	f		4.5	−	31	25	MHz
			5.5	−	37	20	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time (BUS-BUS)	t_{pLH}		50	4.5	−	20	30	−	38	
				5.5	−	17	27	−	34	
	t_{pHL}		150	4.5	−	25	38	−	48	
				5.5	−	22	34	−	43	
Propagation Delay Time (CAB, CBA-BUS)	t_{pLH}		50	4.5	−	29	44	−	55	
				5.5	−	26	40	−	50	
	t_{pHL}		150	4.5	−	34	52	−	65	
				5.5	−	31	47	−	59	
Propagation Delay Time (SAB, SBA-BUS)	t_{pLH}		50	4.5	−	24	34	−	43	
				5.5	−	21	31	−	39	
	t_{pHL}		150	4.5	−	29	42	−	53	
				5.5	−	26	38	−	48	
Output Enable time (GAB, $\overline{GBA}$-BUS)	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	22	33	−	41	
				5.5	−	20	30	−	37	
	t_{pZH}		150	4.5	−	27	41	−	51	
				5.5	−	24	37	−	46	
Output Enable time (GAB, $\overline{GBA}$-BUS)	t_{pLZ}	$R_L=1k\Omega$	50	4.5	−	24	35	−	44	
	t_{pHZ}			5.5	−	22	32	−	40	
Maximum Clock Frequency	f_{MAX}		50	4.5	31	55	−	25	−	MHz
				5.5	37	61	−	30	−	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$, SAB, SBA, CAB, CBA			−	5	10	−	10	pF
Output Capacitance	C_{OUT}	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT651A			−	38	−	−	−	
		TC74HCT652A			−	39	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

4 WORD × 4 BIT REGISTER FILE(3 -STATE)

The TC74HC670A is a high speed CMOS 4-WORDs x 4-BITs REGISTER FILE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The register file is organized as 4 words of 4 bits each.

Separate read and write address inputs (RA, RB, and WA, WB) and enable inputs ($\overline{RE}$, $\overline{WE}$) are available permitting simultaneous writing into one word location and reading from another location.

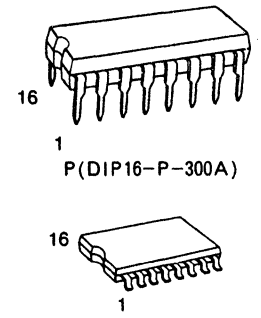
Four data inputs (D0 D3) are provided to store the 4-bit words.

The write address inputs (WA, WB) determine the location of the stored word in the register. When write Enable($\overline{WE}$)is held low, the data is entered into addressed location. When WE is held high, data and address inputs are inhibited. The data acquisition from the four registers is made possible by the read address inputs (RA, RB) when the Read Enable ($\overline{RE}$) is held low. When RE is held high the data outputs are in the high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

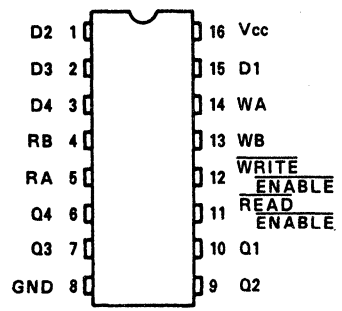
- High Speed ····· t_{pd}=23ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ···| I_{OH} |=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 74LS670



P(DIP16-P-300A)

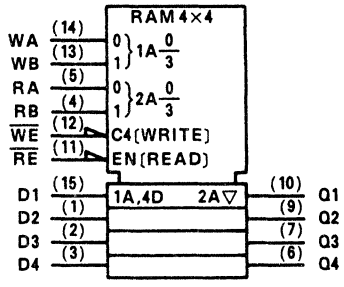
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

WRITE FUNCTION TABLE

WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

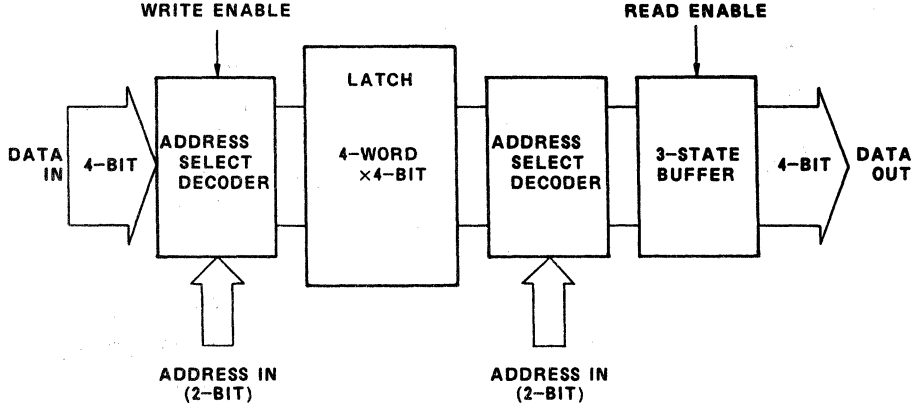
READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

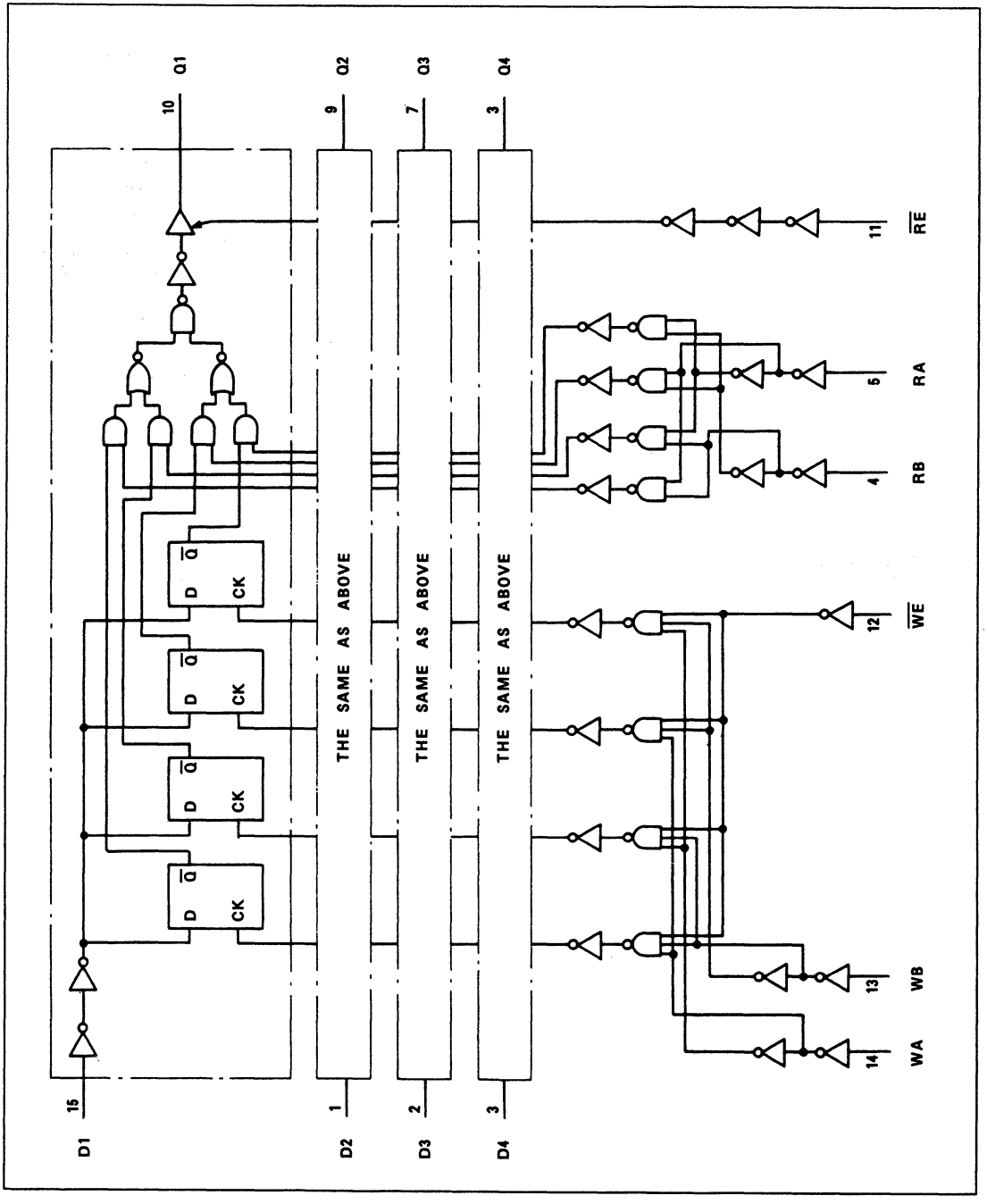
NOTES 1. X : DON'T CARE Z : HIGH IMPEDANCE

2. (Q=D)=THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3. Q0=THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4. W0B1=THE FIRST BIT OF WORD 0,etc.

BLOCK DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{WE}$)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (Dn−$\overline{WE}$)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Set−up Time (WA,WB−$\overline{WE}$)	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (Dn−$\overline{WE}$)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Hold Time (WA,WB−$\overline{WE}$)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Latch Time ($\overline{WE}$−RA,RB)	t_{latch}	Note(1)	2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	

Note(1):t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a loction immediately after that location has received new data.

AC ELECTRICAL CHARACTERISTICS(C_L =15pF,V_{CC}=5V,Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (RA,AB−Qn)	t_{pLH} t_{pHL}		−	23	34	
Propagation Delay Time ($\overline{WE}$−Qn)	t_{pLH} t_{pHL}		−	24	38	
Propagation Delay Time (Dn−Qn)	t_{pLH} t_{pHL}		−	22	32	
3−State Output Enable Time	t_{pZL} t_{pZH}	R_L = 1 kΩ	−	11	18	
3−State Output Disable Time	t_{pLH} t_{pHL}	R_L = 1 kΩ	−	11	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (RA, AB−Qn)	t_{pLH} t_{pHL}		2.0	−	90	195	−	245	
			4.5	−	27	39	−	49	
			6.0	−	22	33	−	42	
Propagation Delay Time ($\overline{WE}$−Qn)	t_{pLH} t_{pHL}		2.0	−	95	220	−	275	
			4.5	−	28	44	−	55	
			6.0	−	22	37	−	47	
Propagation Delay Time (Dn−Qn)	t_{pLH} t_{pHL}		2.0	−	90	185	−	230	
			4.5	−	26	37	−	46	
			6.0	−	20	31	−	39	
Output Enable time	t_{pZH} t_{pZL}	R_L = 1 kΩ	2.0	−	46	110	−	140	
			4.5	−	14	22	−	28	
			6.0	−	12	19	−	24	
Output Disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	2.0	−	25	95	−	120	
			4.5	−	14	19	−	24	
			6.0	−	12	16	−	20	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Output Capacitance	C_{OUT}			−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)			−	101	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

8-BIT EQUALITY COMPARATOR

The TC74HC688A is a high speed cmos 8-BIT EQUALITY COMPARATOR fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

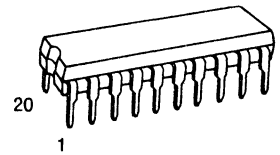
The TC74HC688A compares two 8-bit binary or BCD words applied inputs $P_0 \sim P_7$, and inputs $Q_0 \sim Q_7$, and indicates whether or not they are equal.

A signal active low enable is provided to facilitate cascading of several packages to compare of words greater than 8 bits

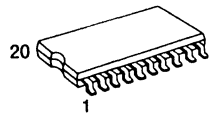
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =17ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS688

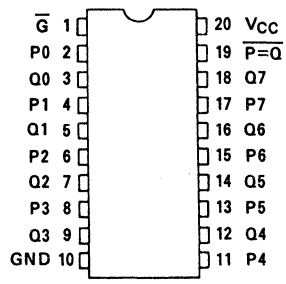


P(DIP20-P-300A)



F(SOP20-P-300)

PIN ASSIGNMENT



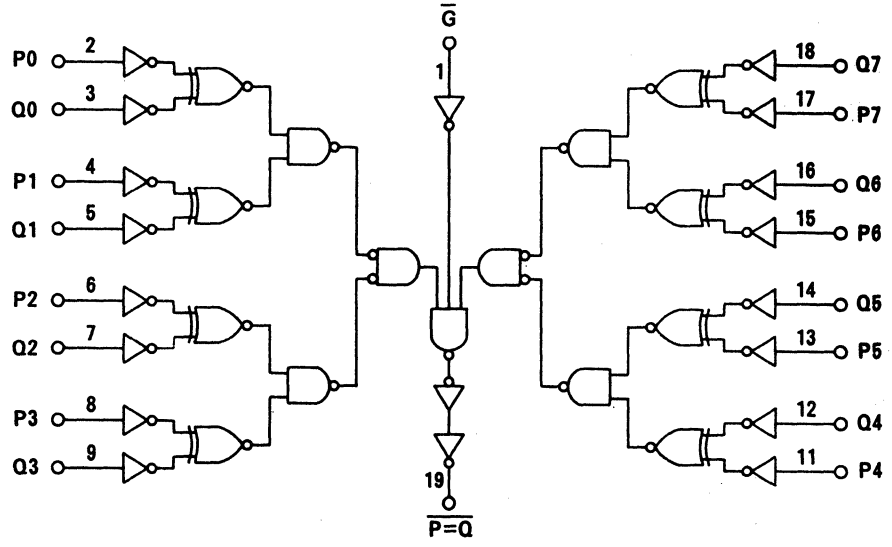
(TOP VIEW)

TRUTH TABLE

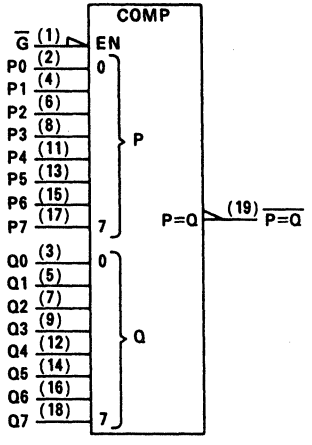
INPUTS		OUTPUT
P , Q	$\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P ≠ Q	L	H
X	H	H

X : Don't care

SYSTEM DIAGRAM



IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time (Pn, Qn−$\overline{P=Q}$)	t_{pLH} t_{pHL}		–	17	29	
Propagation Delay Time ($\overline{G}$−$\overline{P=Q}$)	t_{pLH} t_{pHL}		–	10	18	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (Pn, Qn−$\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	–	60	170	–	215	
			4.5	–	21	34	–	43	
			6.0	–	17	29	–	37	
Propagation Delay Time ($\overline{G}$−$\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	–	40	110	–	140	
			4.5	–	13	22	–	28	
			6.0	–	10	19	–	24	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	32	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC690AP/AF•TC74HC691AP/AF
TC74HC692AP/AF•TC74HC693AP/AF

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER WITH OUTPUT REGISTER (MULTIPLEXED 3-STATE OUTPUTS)

TC74HC690AP/AF DECADE, ASYNCHRONOUS CLEAR
TC74HC691AP/AF BINARY, ASYNCHRONOUS CLEAR
TC74HC692AP/AF DECADE, SYNCHRONOUS CLEAR
TC74HC693AP/AF BINARY, SYNCHRONOUS CLEAR

The TC74HC690A -693A are high speed CMOS COUNTER/REGISTERS fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 690A/692A are BCD DECADE COUNTERS, and the 691A/693A are 4-BIT BINARY COUNTERS. These devices have output registers.

If the $\overline{LOAD}$ input is held low, the data inputs (A~D) are loaded into an internal counter on the positive edge of counter clock (CCK). In the counter mode, the internal counter counts up on the positive edge of counter clock. Counter clear input ($\overline{CCLR}$) is active low. The counter clear function of the 692A/693A is synchronous to CCK, while the 690A/691A are cleared asynchronously.

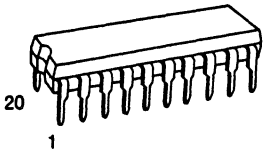
The internal counter's output is stored in the output register on the positive edge of register clock (RCK). Register clear input ($\overline{RCLR}$) is active low. The register clear function of the 692A/693A is synchronous to RCK, while the 690A/691A are cleared asynchronously. At this point, the internal counter outputs do not change. The outputs (QA~QD) are selected as internal counter outputs or register outputs by output select (R/$\overline{C}$).

Two enable inputs (ENT and ENP) and carry output (RCO) are provided to enable easy cascading of counters without using external gates.

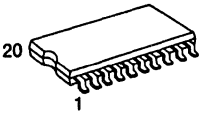
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=63MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads For QA~QD
  10 LSTTL Loads For RCO
- Symmetrical Output Impedance ····· $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA~QH
  $|I_{OH}|=I_{OL}$=4mA(Min.)
  For RCO
- Balanced Propagation Delays ··· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS690-693

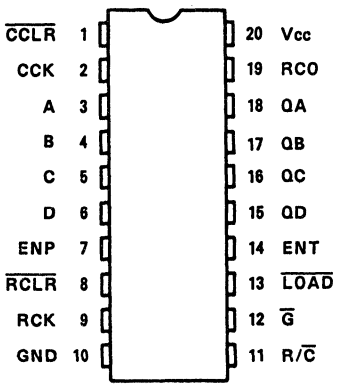


P(DIP20-P-300A)



F(SOP20-P-300)

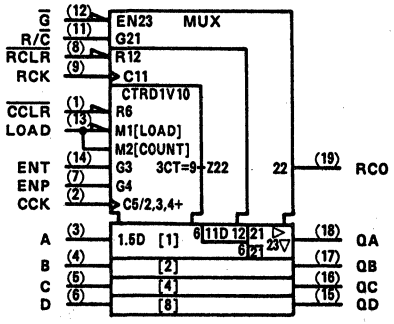
PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

TC74HC690A



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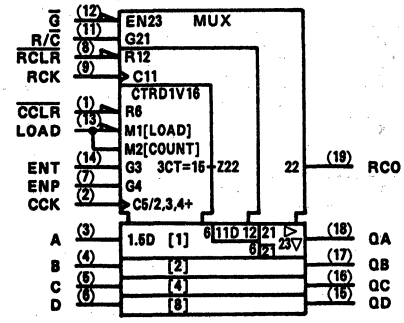

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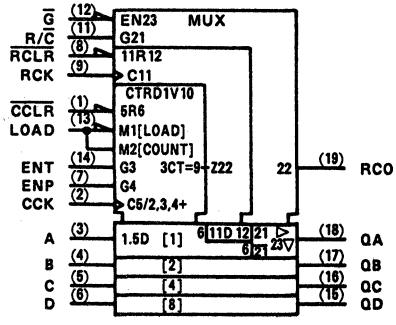

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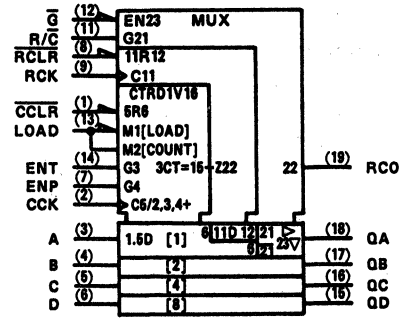


INPUTS											OUTPUTS				FUNCTION
					690A/691A		692A/693A								
$\overline{CCLR}$	$\overline{LOAD}$	ENP	ENT	$\overline{RCLR}$	CCK	RCK	CCK	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	CD	
X	X	X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	↓	X	X	X	L	L	L	L	COUNTER CLEAR
H	L	X	X	X	↓	X	↓	X	L	L	a	b	c	d	LOAD DATA
H	H	L	X	X	↓	X	↓	X	L	L	NO CHANGE				COUNT DISABLE
H	H	X	L	X	↓	X	↓	X	L	L					NO CHANGE
H	H	H	H	X	↓	X	↓	X	L	L	COUNT UP				COUNT UP
H	X	X	X	X	↑	X	↑	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	L	X	X	X	↓	H	L	L	L	L	L	REGISTER CLEAR
X	X	X	X	H	X	↓	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	H	X	↑	X	↑	H	L	NO CHANGE				NO CHANGE

X : DON'T CARE

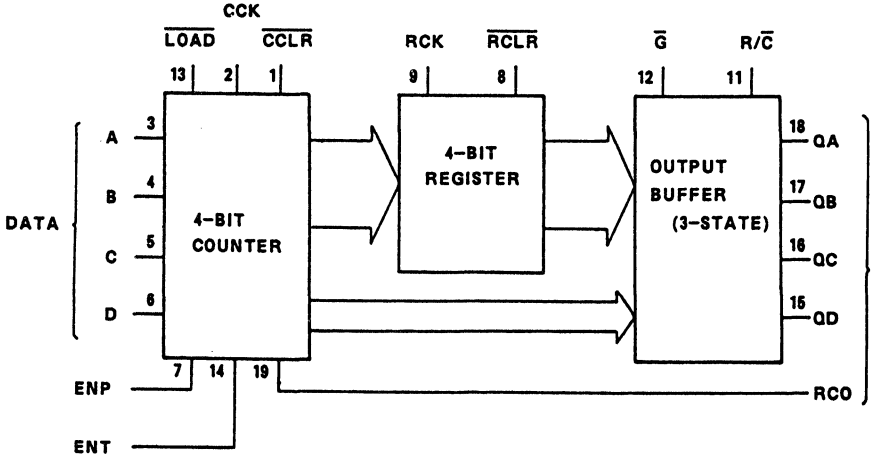
Z : High Impedance

a ~ d : The level of steady state input voltage at inputs A ~ D respectively.

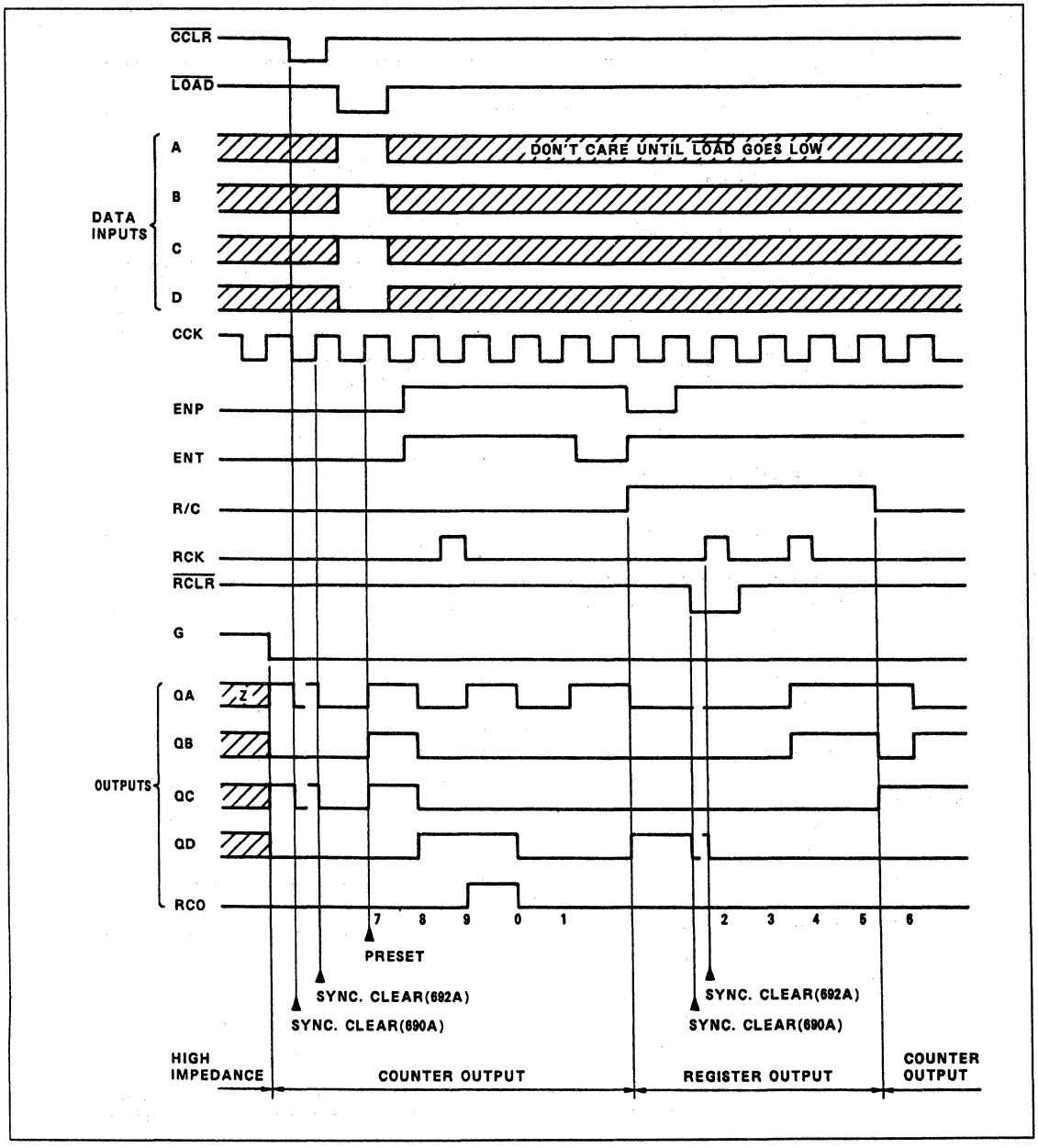
a' ~ d' :The level of internal counter outputs respectly ,before the most recent postive edge of the register clock.

HC690A/692A ; RCO=QA • QD • ENT

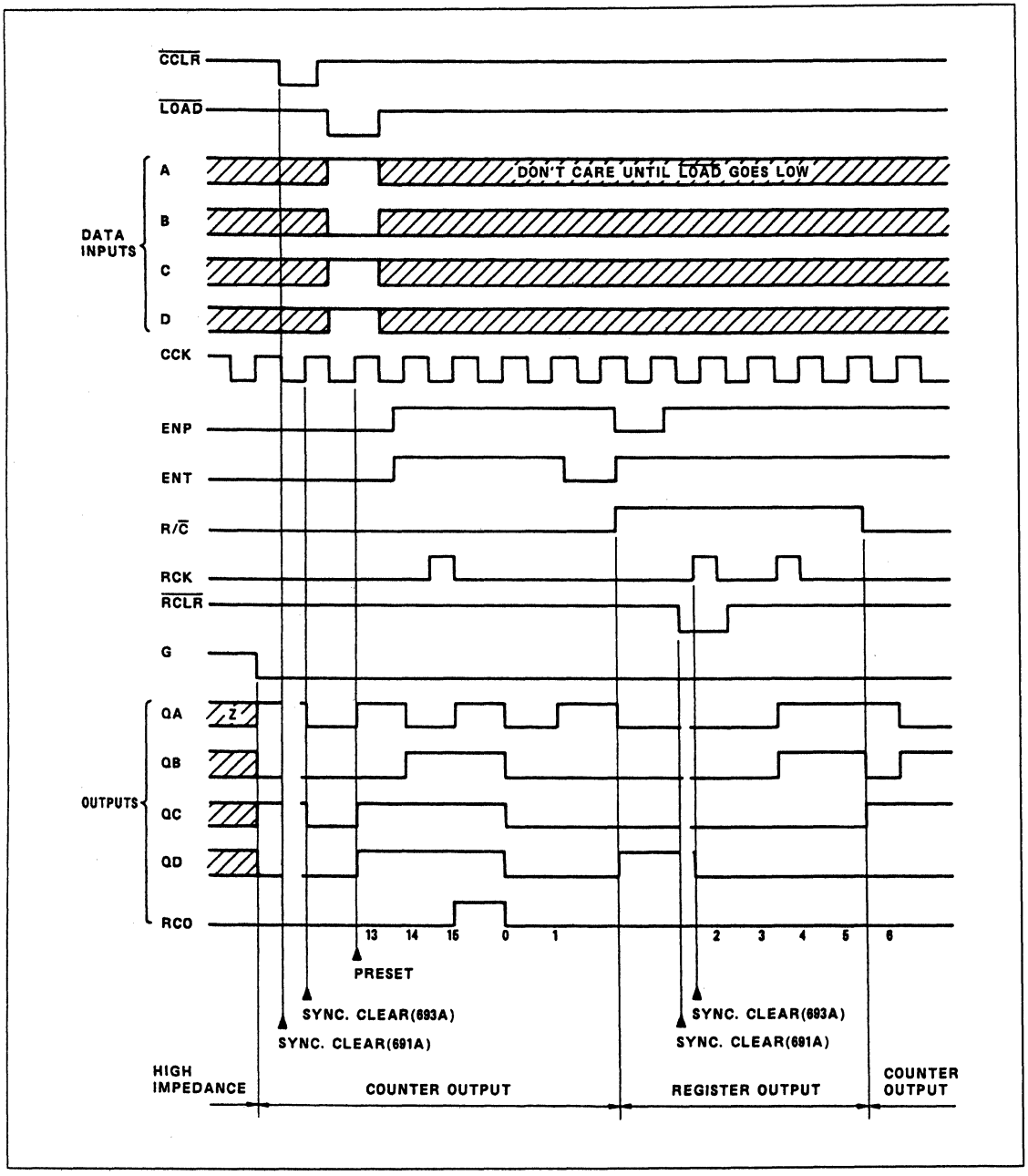
HC691A/693A ; RCO=QA • QB • QC • QD • ENT



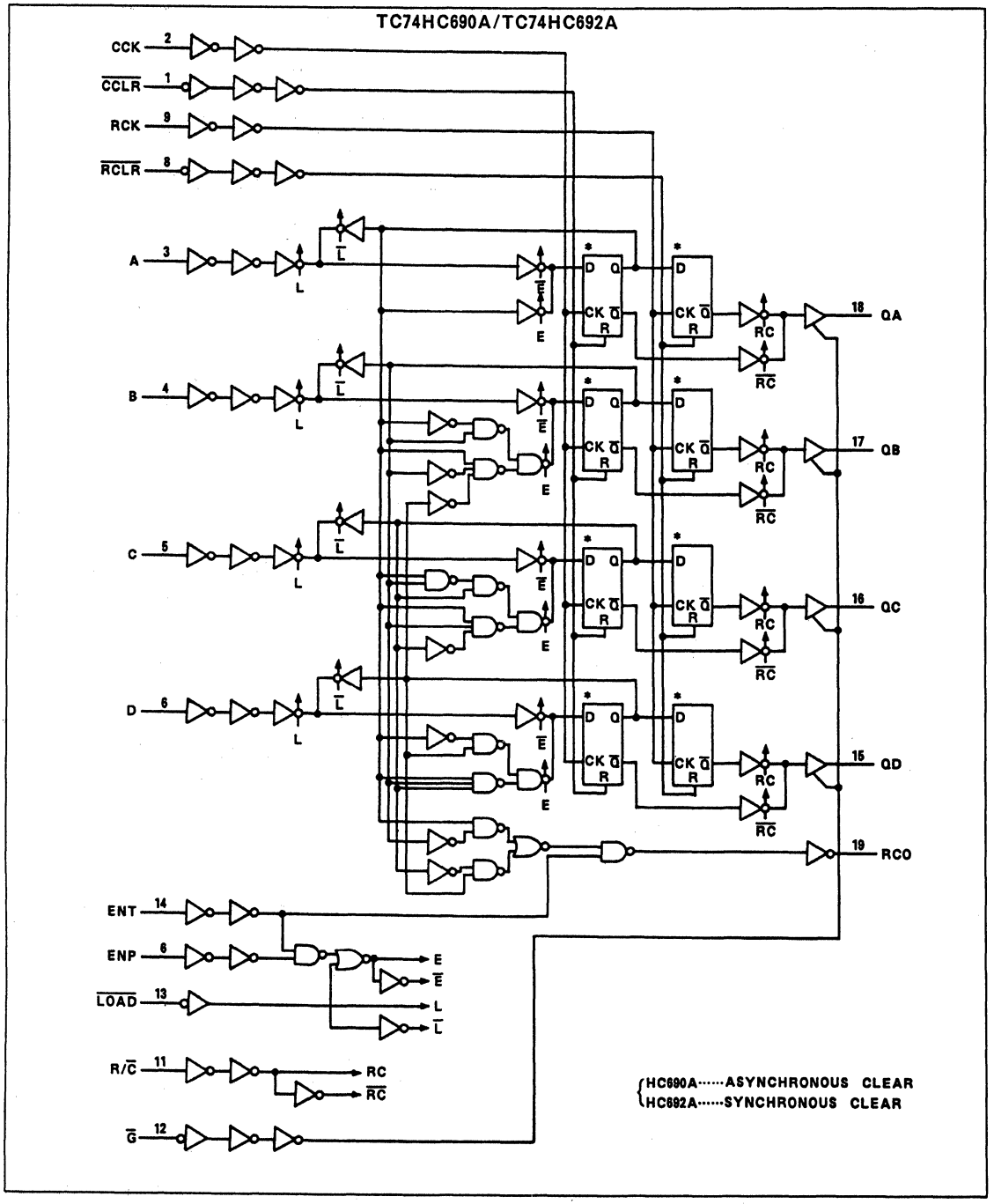
TIMING CHART (TC74HC690A/692A ; DECADE COUNTER)



TIMING CHART (TC74HC691A/693A ; BINARY COUNTER)

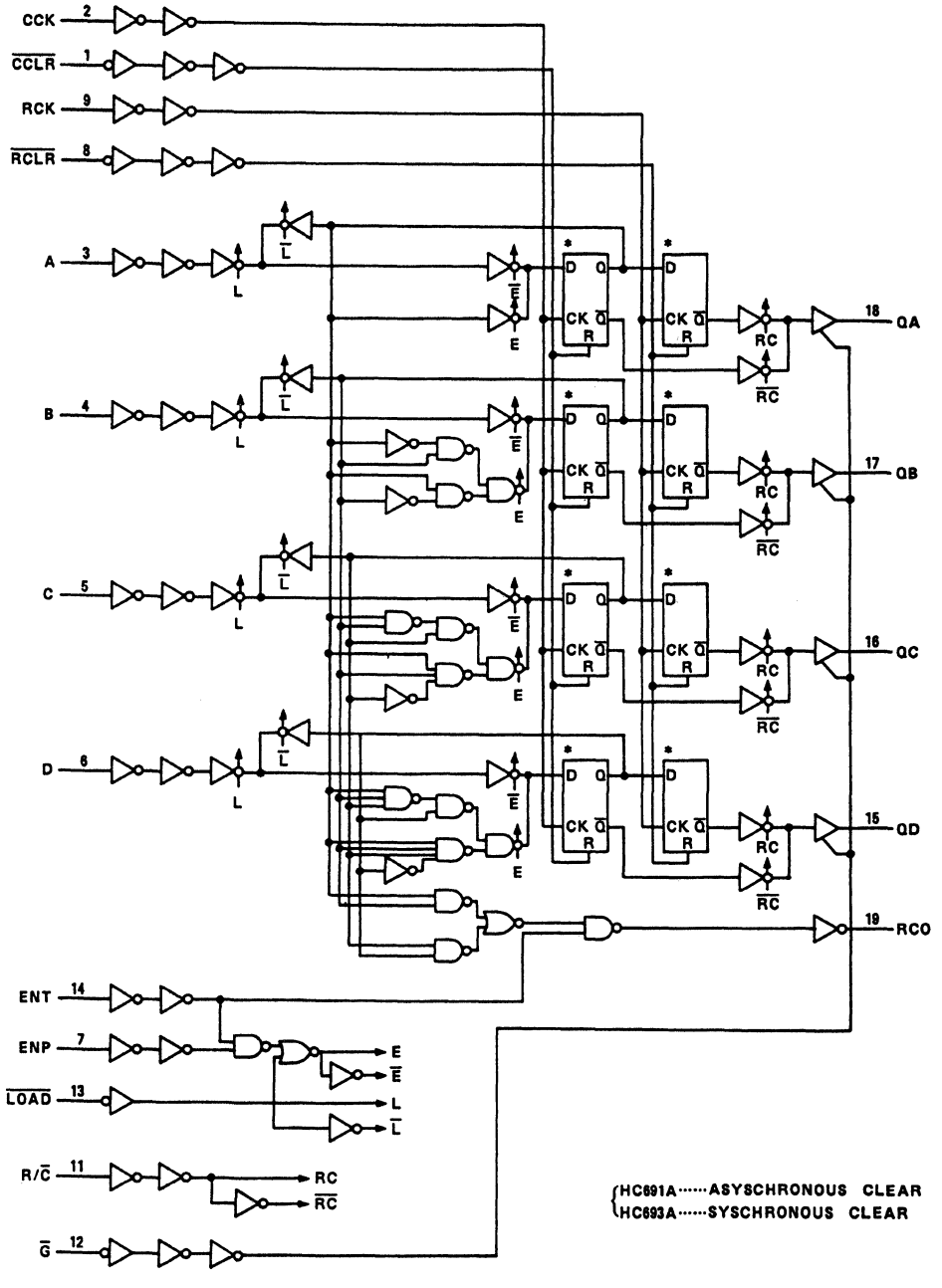


SYSTEM DIAGRAM



SYSTEM DIAGRAM

TC74HC691A/TC74HC693A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (RCO) / (Q_A~Q_H)	I_{OUT}	±25 / ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}				2.0	1.5	−	−	1.5	−	V
					4.5	3.15	−	−	3.15	−	
					6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}				2.0	−	−	0.5	−	0.5	V
					4.5	−	−	1.35	−	1.35	
					6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}		I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
					4.5	4.4	4.5	−	4.4	−	
					6.0	5.9	6.0	−	5.9	−	
			RCO	I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
				I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
			Q_A~Q_H	I_{OH} =−6 mA	4.5	4.18	4.31	−	4.31	−	
				I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}		I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
					4.5	−	0.0	0.1	−	0.1	
					6.0	−	0.0	0.1	−	0.1	
			RCO	I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
				I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
			Q_A~Q_H	I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
				I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND			6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND			6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND			−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	12	15	
Minimum Pulse Width ($\overline{CCLR}$,$\overline{RCLR}$) *	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	12	15	
Minimum Set−up Time ($\overline{CCLR}$,$\overline{RCLR}$) **	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	16	20	
Minimum Set−up Time ($\overline{LOAD}$,ENT,ENP)	t_s		2.0	−	150	190	
			4.5	−	30	38	
			6.0	−	24	25	
Minimum Set−up Time (A,B,C,D)	t_s		2.0	−	125	155	
			4.5	−	25	31	
			6.0	−	20	25	
Minimum Set−up Time (CCK−RCK)	t_s		2.0	−	125	155	
			4.5	−	25	31	
			6.0	−	20	25	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Removal Time *	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	8	10	
Clock Frequency	f		2.0	−	4	3.5	MHz
			4.5	−	22	18	
			6.0	−	26	21	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF,V_{CC}=5V,Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (RCO)	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CCK−RCO)	t_{pLH} t_{pHL}		−	18	32	
Propagation Delay Time (ENT−RCO)	t_{pLH} t_{pHL}		−	8	15	
Propagation Delay Time ($\overline{CCLR}$−RCO) *	t_{pLH}		−	19	34	
Maximum Clock Frequency	f_{MAX}		24	58	−	MHz

*: for TC74HC690A/691A only
**: for TC74HC692A/693A only

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (RCO)	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (CCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	84	215	−	270	
				4.5	−	27	43	−	54	
				6.0	−	22	34	−	43	
			150	2.0	−	99	255	−	320	
				4.5	−	32	51	−	64	
				6.0	−	26	41	−	51	
Propagation Delay Time (RCK−Q)	t_{pLH} t_{pHL}		50	2.0	−	84	215	−	270	
				4.5	−	28	43	−	54	
				6.0	−	22	34	−	43	
			150	2.0	−	99	255	−	320	
				4.5	−	33	51	−	64	
				6.0	−	26	41	−	51	
Propagation Delay Time ($R/\overline{C}$−Q)	t_{pLH} t_{pHL}		50	2.0	−	63	170	−	215	
				4.5	−	21	34	−	43	
				6.0	−	17	27	−	34	
			150	2.0	−	78	210	−	265	
				4.5	−	26	42	−	53	
				6.0	−	21	34	−	42	
Propagation Delay Time ($\overline{CCLR}$−Q)*	t_{pHL}		50	2.0	−	93	250	−	315	
				4.5	−	31	50	−	63	
				6.0	−	25	40	−	50	
			150	2.0	−	108	290	−	365	
				4.5	−	36	58	−	73	
				6.0	−	29	46	−	58	
Propagation Delay Time ($\overline{RCLR}$−Q)*	t_{pHL}		50	2.0	−	90	250	−	315	
				4.5	−	30	50	−	63	
				6.0	−	24	40	−	50	
			150	2.0	−	105	290	−	365	
				4.5	−	35	58	−	73	
				6.0	−	28	46	−	58	
Propagation Delay Time (CCK−RCO)	t_{pLH} t_{pHL}		50	2.0	−	72	185	−	230	
				4.5	−	23	37	−	46	
				6.0	−	19	30	−	37	
Propagation Delay Time (ENT−RCO)	t_{pLH} t_{pHL}		50	2.0	−	36	95	−	120	
				4.5	−	12	19	−	24	
				6.0	−	10	15	−	19	
Propagation Delay Time ($\overline{CCLR}$−RCO)*	t_{pHL}		50	2.0	−	75	195	−	245	
				4.5	−	25	39	−	49	
				6.0	−	20	31	−	39	

*: for TC74HC160A/160A only

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Enable time ($\overline{G}$–Q)	t_{pZL} t_{pZH}	R_L =1kΩ	50	2.0	−	48	120	−	150	ns
				4.5	−	16	24	−	30	
				6.0	−	13	19	−	24	
			150	2.0	−	63	160	−	200	
				4.5	−	21	32	−	40	
				6.0	−	17	26	−	32	
Output Disable time ($\overline{G}$–Q)	t_{pLZ} t_{pHZ}	R_L =1kΩ	50	2.0	−	34	145	−	180	
				4.5	−	18	29	−	36	
				6.0	−	14	23	−	29	
Maximum Ciock Frequency	f_{MAX}		50	2.0	4	17	−	3.5	−	MHz
				4.5	22	52	−	18	−	
				6.0	26	65	−	21	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	13	−	−	−	
Power Dissipation Capacitance	C_{PD} (1)				−	63	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

NOTES

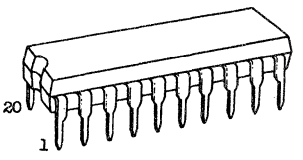
TC74HC696P
TC74HC697P

TC74HC696P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC697P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC696/697 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC696 is BCD DECADE COUNTER, and TC74HC697 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input $U/\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ∿ QD) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$). Their clear function are cleared asynchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=33MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ∿ QD)
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ∿ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS696/697)



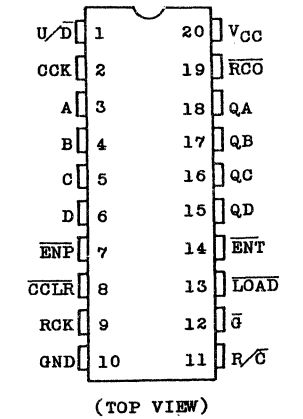
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ∿ QD) ±20 (RCO)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	X	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↑	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↑	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↑	X	X	L	L					
H	H	L	L	↑	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↑	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↓	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↑	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↓	H	L	NO CHANGE				NO LOAD

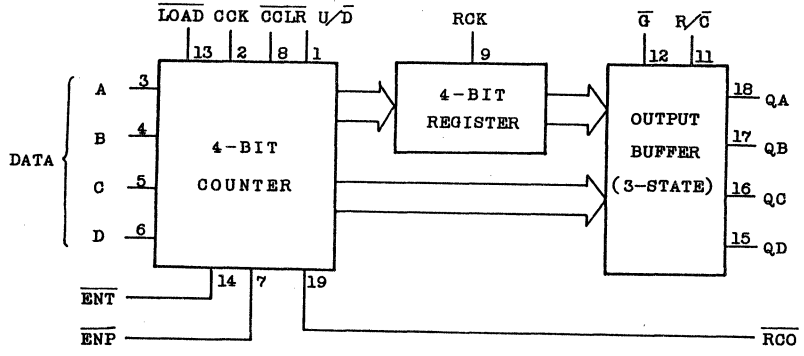
X: Don't care
Z: High Impedance
a∿d : The level of steady state inputs at inputs A through D respectively.
a'∿d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

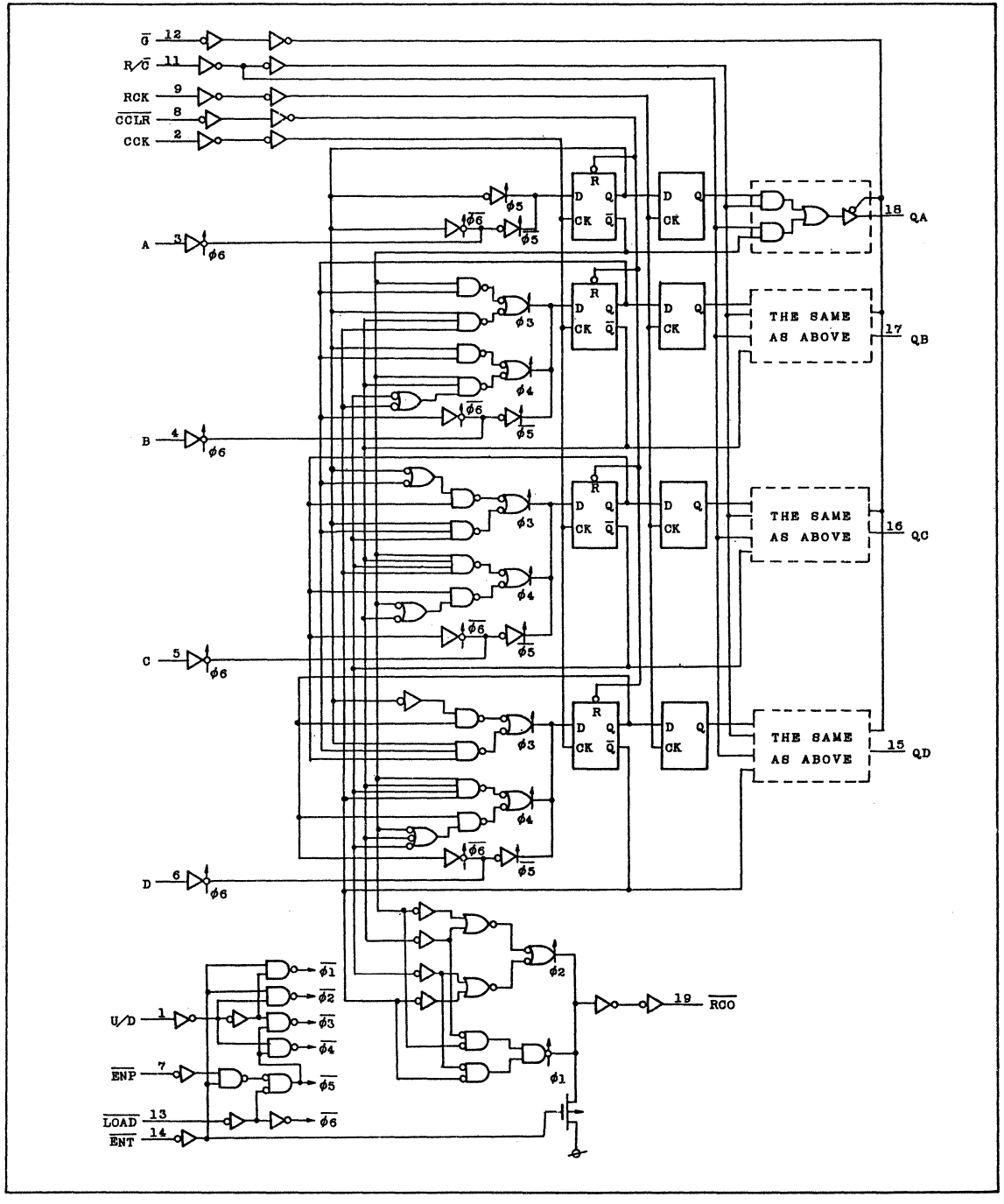
TC74HC696 $\overline{RCO}=\overline{(UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT)}$

TC74HC697 $\overline{RCO}=\overline{(UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT)}$

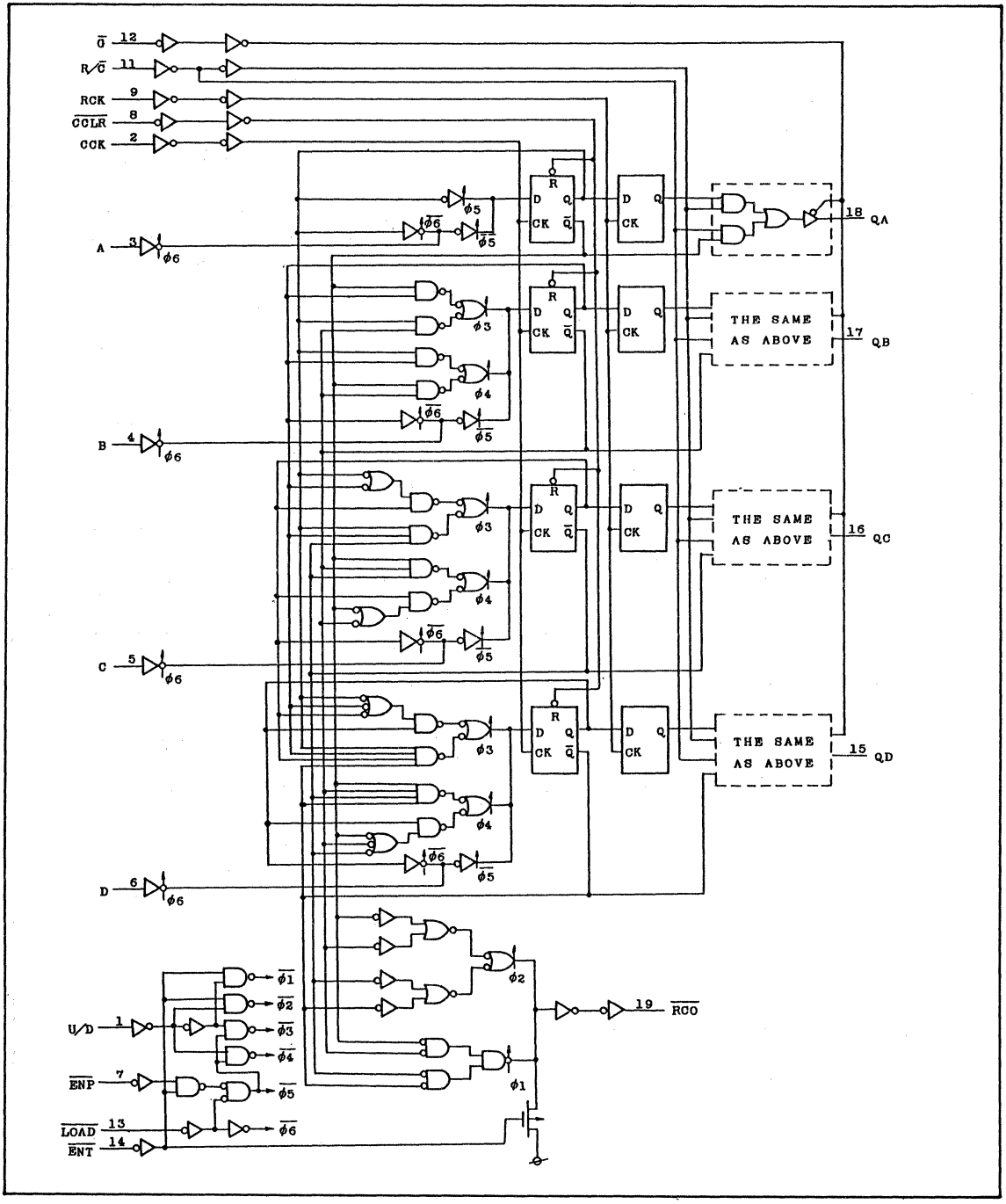
BLOCK DIAGRAM



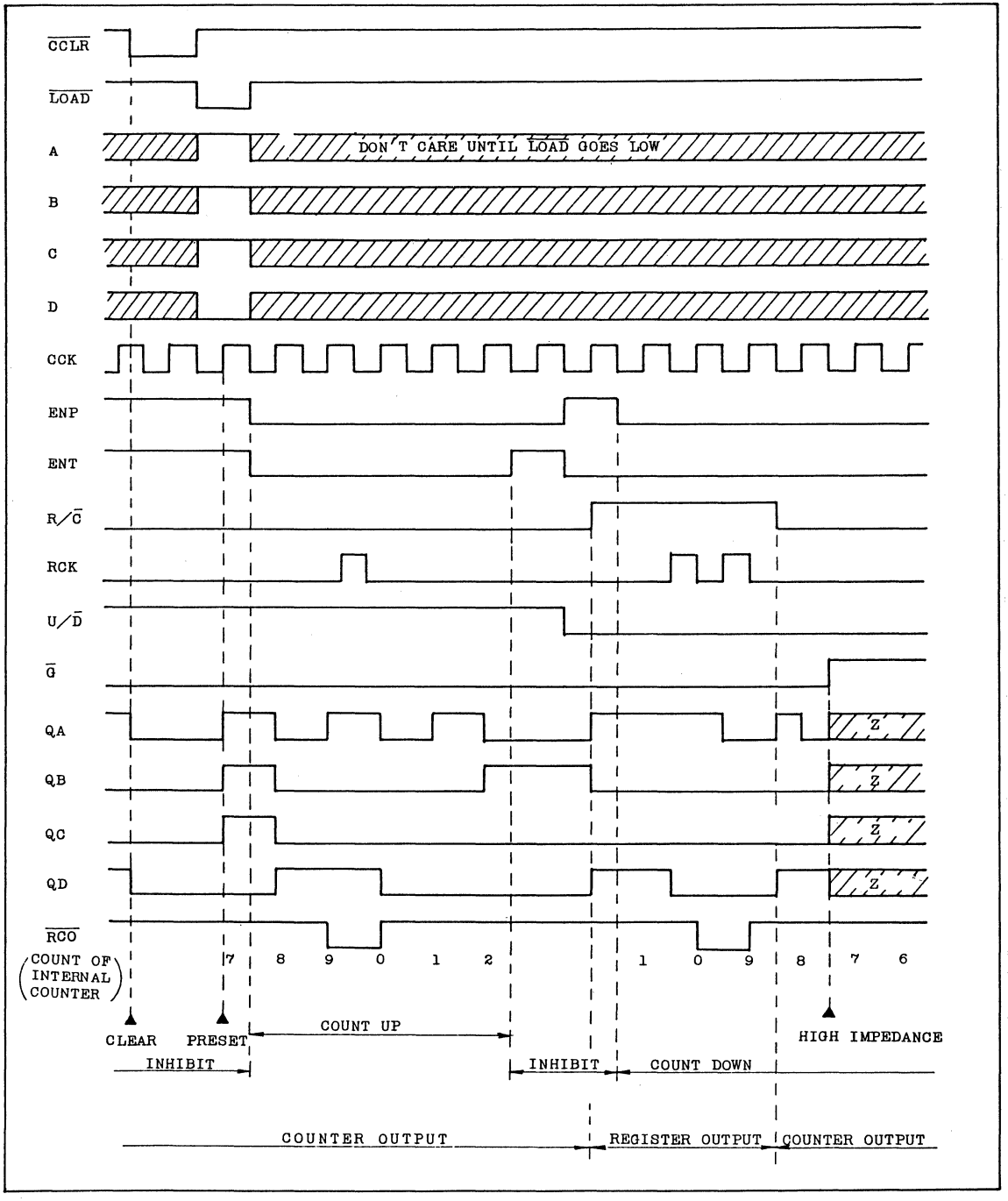
LOGIC DIAGRAM TC74HC696



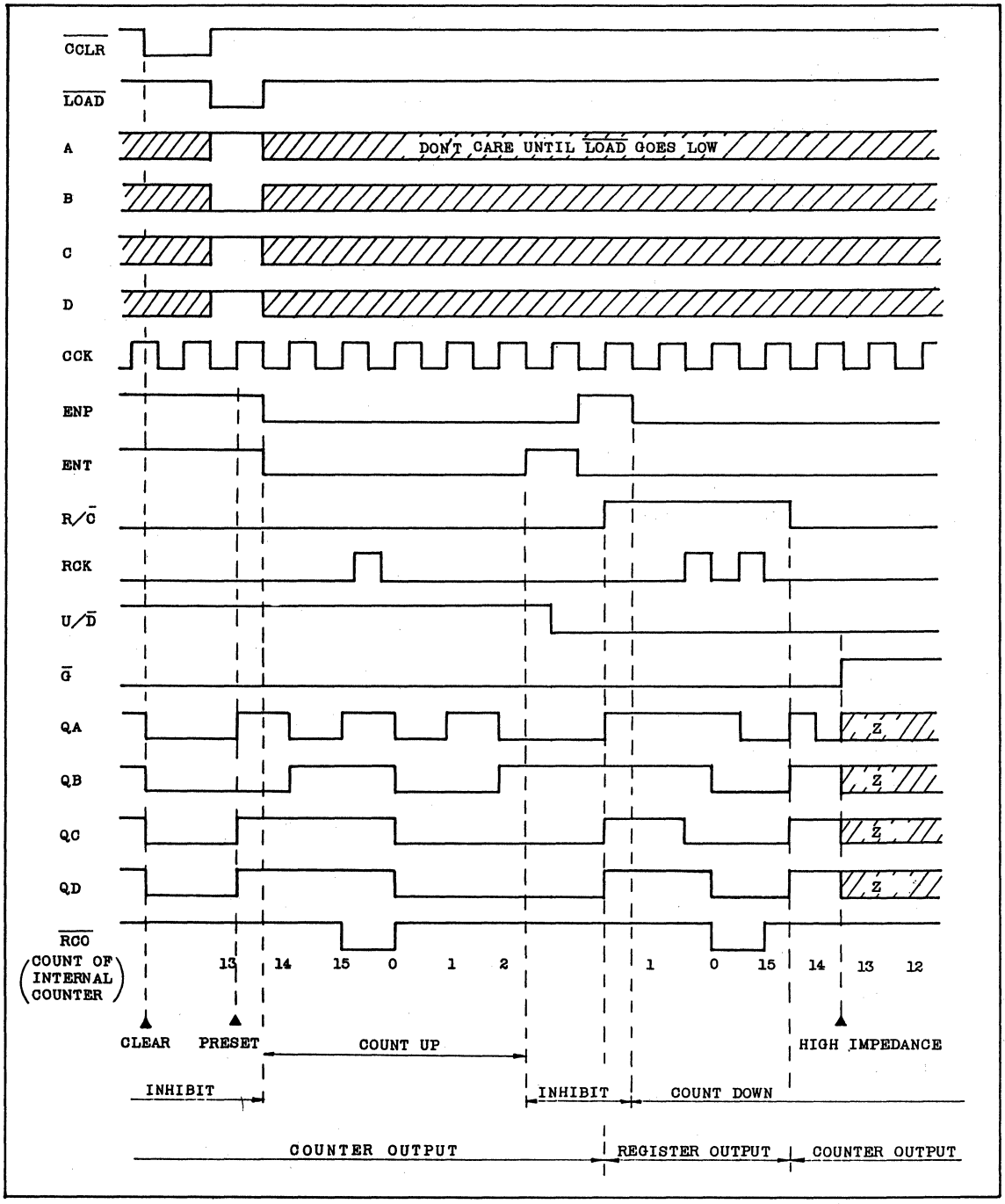
LOGIC DIAGRAM TC74HC697



TIMING CHART TC74HC696



TIMING CHART TC74HC697



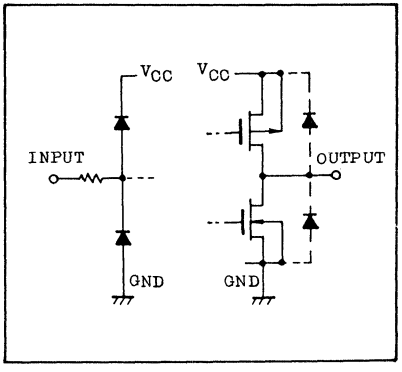
AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	136	260	-	325	
			4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	160	305	-	380	
			4.5	-	40	61	-	76	
			6.0	-	34	52	-	65	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	225	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CCLR}$ - Q)	t_{pHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CCLR}$ - $\overline{RCO}$)	t_{pHL}		2.0	-	172	325	-	405	
			4.5	-	43	65	-	81	
			6.0	-	37	55	-	69	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	30	-	16	-	
			6.0	24	35	-	19	-	
Minimum Pulse Widht (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CCLR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	96	225	-	280	
			4.5	-	24	45	-	56	
			6.0	-	20	38	-	48	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		QA ∿ QH	I_{OH}=−6mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−7.8mA	6.0	5.68	5.80	−	5.63	−	
		$\overline{RCO}$	I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=7.8mA	6.0	−	0.18	0.26	−	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

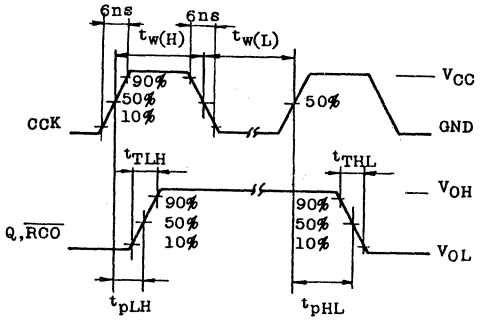
AC ELECTRICAL CHARACTERISTICS (Continued)

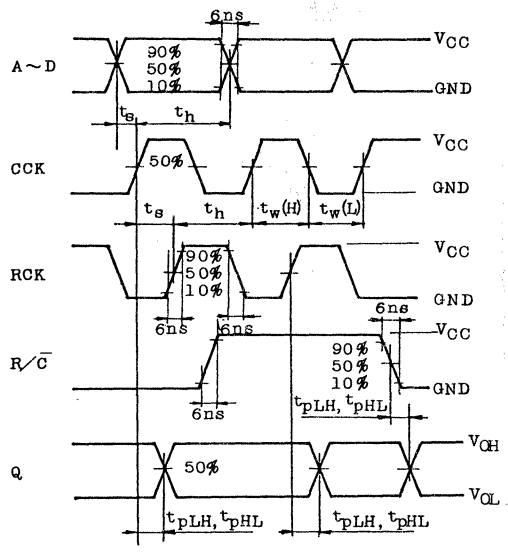
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	20	75	-	95	ns
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	52	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
Minimum Set-up Time ($U/\overline{D}$)	t_s		2.0	-	64	150	-	190	
			4.5	-	16	30	-	38	
			6.0	-	14	26	-	32	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC696		-	90	-	-	-	
		TC74HC697		-	92	-	-	-	

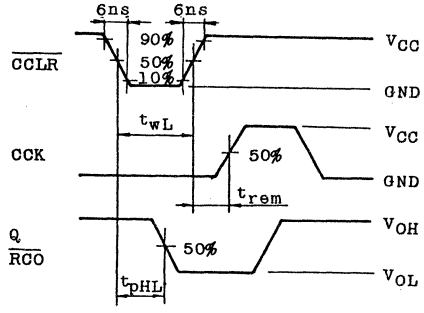
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

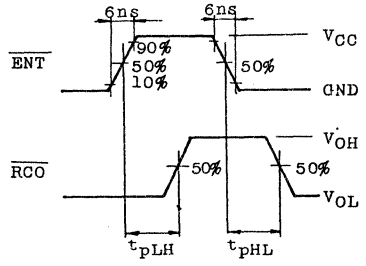
$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

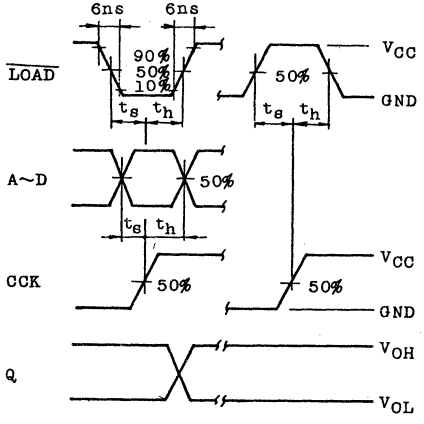
SWITCHING CHARACTERISTICS TEST WAVEFORM

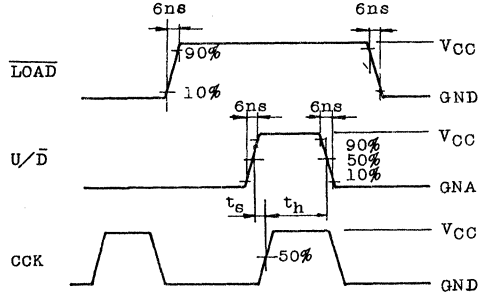






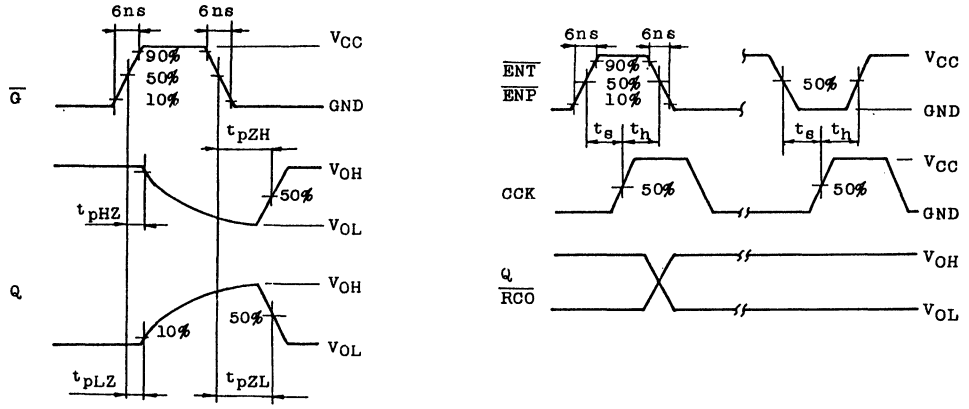




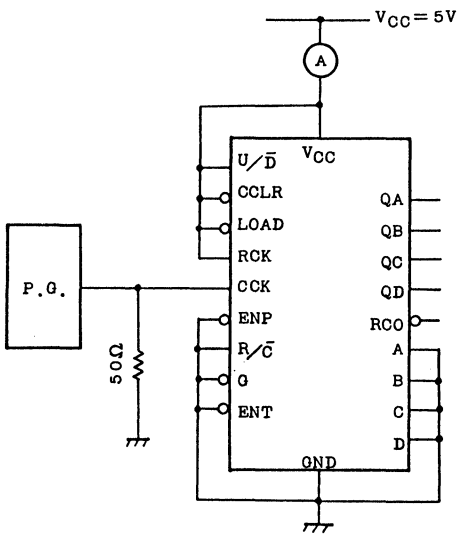


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

OUTPUT DISABLE, ENABLE



$I_{CC(Opr.)}$ TEST CIRCUIT



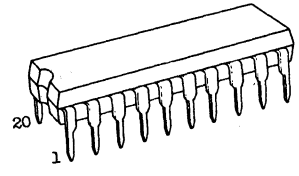
TC74HC698P
TC74HC699P

TC74HC698P U/D DECADE COUNTER/REGISTER (3-STATE)
TC74HC699P U/D 4-BIT BINARY COUNTER/REGISTER (3-STATE)

The TC74HC698/699 are high speed CMOS up/down counters fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. TC74HC698 is BCD DECADE COUNTER, and TC74HC699 is 4-BIT BINARY COUNTER. Both devices have registers respectively. They count at positive edge of counter clock input (CCK) when selected at "Counter Mode". If input $U/\overline{D}$ is held "H", internal counter counts up, and held "L", counts down. Internal counter's outputs are memoried in output register at positive edge of register clock (RCK). The outputs (QA ∿ QD) are selected internal counter outputs or register outputs respectively by output select input ($R/\overline{C}$). Their clear function are cleared synchronously to clock. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=31MHz(Max.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads (For $\overline{RCO}$)
  15 LSTTL Loads (For QA ∿ QD)
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
  For QA ∿ QD Output
  $|I_{OH}|=I_{OL}$=4mA(Min.)For $\overline{RCO}$ Output
- Balanced Propagation Delays ..... $t_{PLH} \fallingdotseq t_{PHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with LSTTL (74LS698/699)



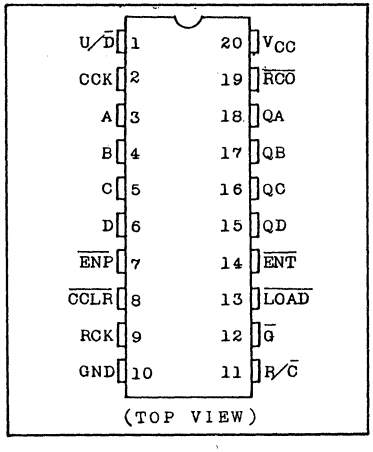
DIP20(3D20AP)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ∿ 7	V
DC Input Voltage	V_{IN}	−0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35 (QA ∿ QD) ±25 ($\overline{RCO}$)	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	−65 ∿ 150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=−40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of −10mW/°C shall be applied until 300mW.

PIN ASSIBNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS									OUTPUTS				FUNCTION
$\overline{CCLR}$	$\overline{LOAD}$	$\overline{ENP}$	$\overline{ENT}$	CCK	U/$\overline{D}$	RCK	R/$\overline{C}$	$\overline{G}$	QA	QB	QC	QD	
X	X	X	X	X	X	X	X	H	Z	Z	Z	Z	HIGH IMPEDANCE
L	X	X	X	↓	X	X	L	L	L	L	L	L	CLEAR COUNTER
H	L	X	X	↓	X	X	L	L	a	b	c	d	LOAD COUNTER
H	H	H	X	↓	X	X	L	L	NO CHANGE				NO COUNT
H	H	X	H	↓	X	X	L	L					
H	H	L	L	↓	H	X	L	L	COUNT UP				COUNT UP
H	H	L	L	↓	L	X	L	L	COUNT DOWN				COUNT DOWN
H	X	X	X	↑	X	X	L	L	NO CHANGE				NO COUNT
X	X	X	X	X	X	↓	H	L	a'	b'	c'	d'	LOAD REGISTER
X	X	X	X	X	X	↑	H	L	NO CHANGE				NO LOAD

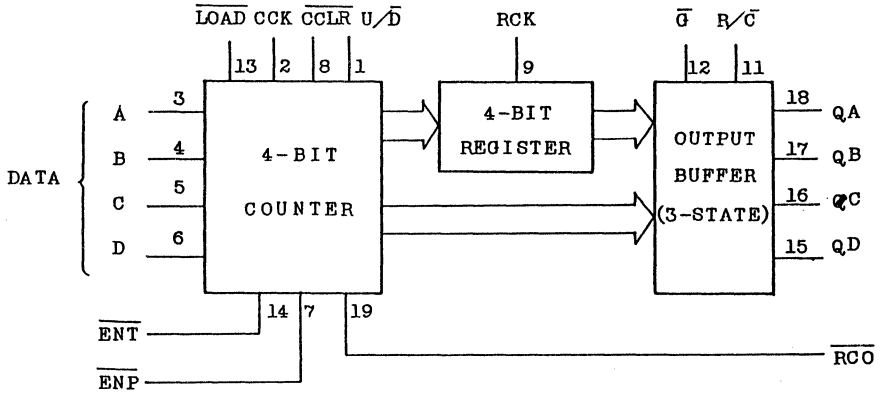
X: Don't care
Z: High Impedance
a∿d : The level of steady state inputs at inputs A through D respectively.
a'∿d': The level of steady state outputs at internal counter outputs QA' through QD' respectively.

$\overline{RCO}$ Function

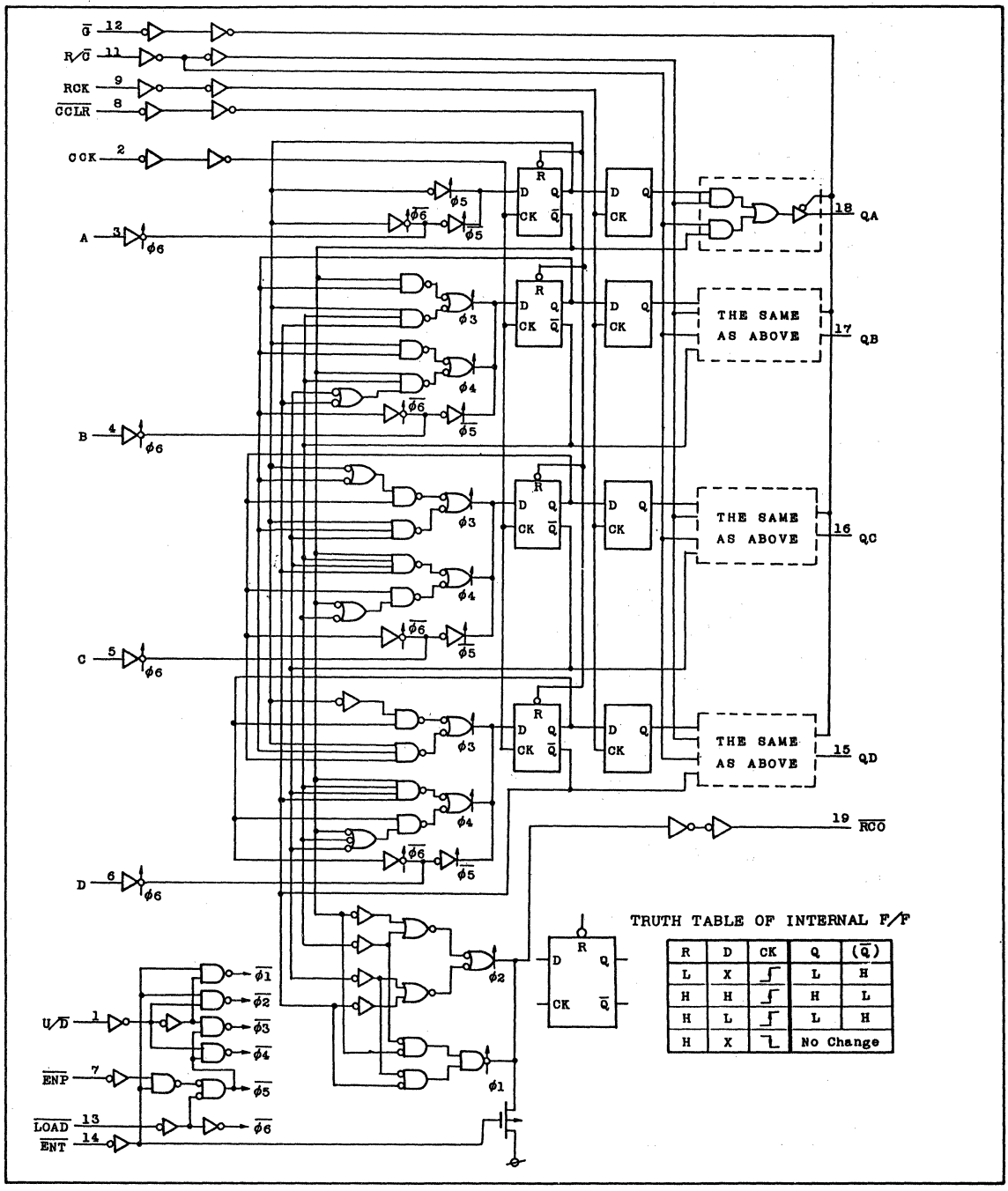
TC74HC698 $\overline{RCO}=(\overline{UP \cdot QA \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QD} \cdot ENT})$

TC74HC699 $\overline{RCO}=(\overline{UP \cdot QA \cdot QB \cdot QC \cdot QD \cdot ENT + \overline{UP} \cdot \overline{QA} \cdot \overline{QB} \cdot \overline{QC} \cdot \overline{QD} \cdot ENT})$

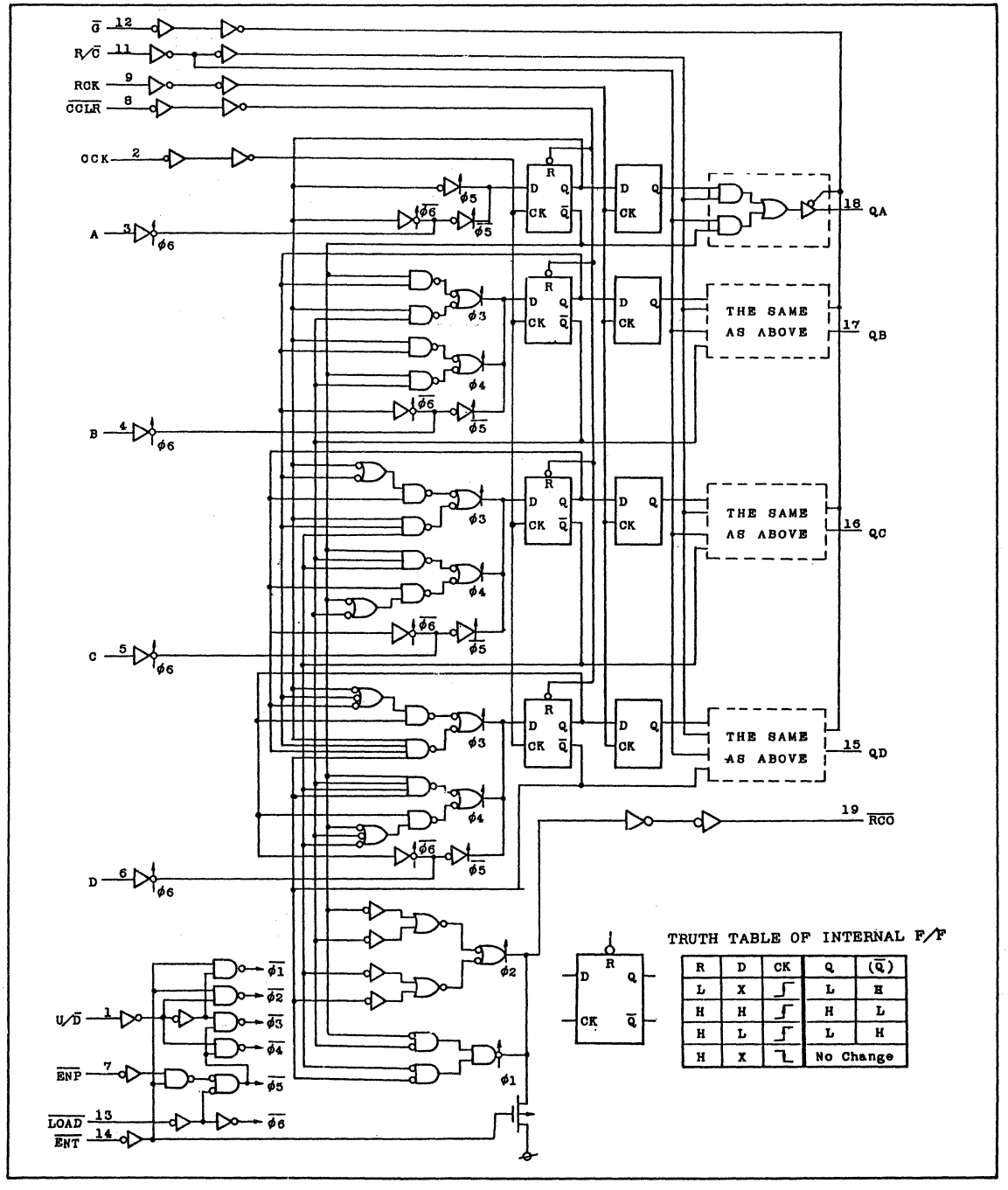
BLOCK DIAGRAM



LOGIC DIAGRAM TC74HC698



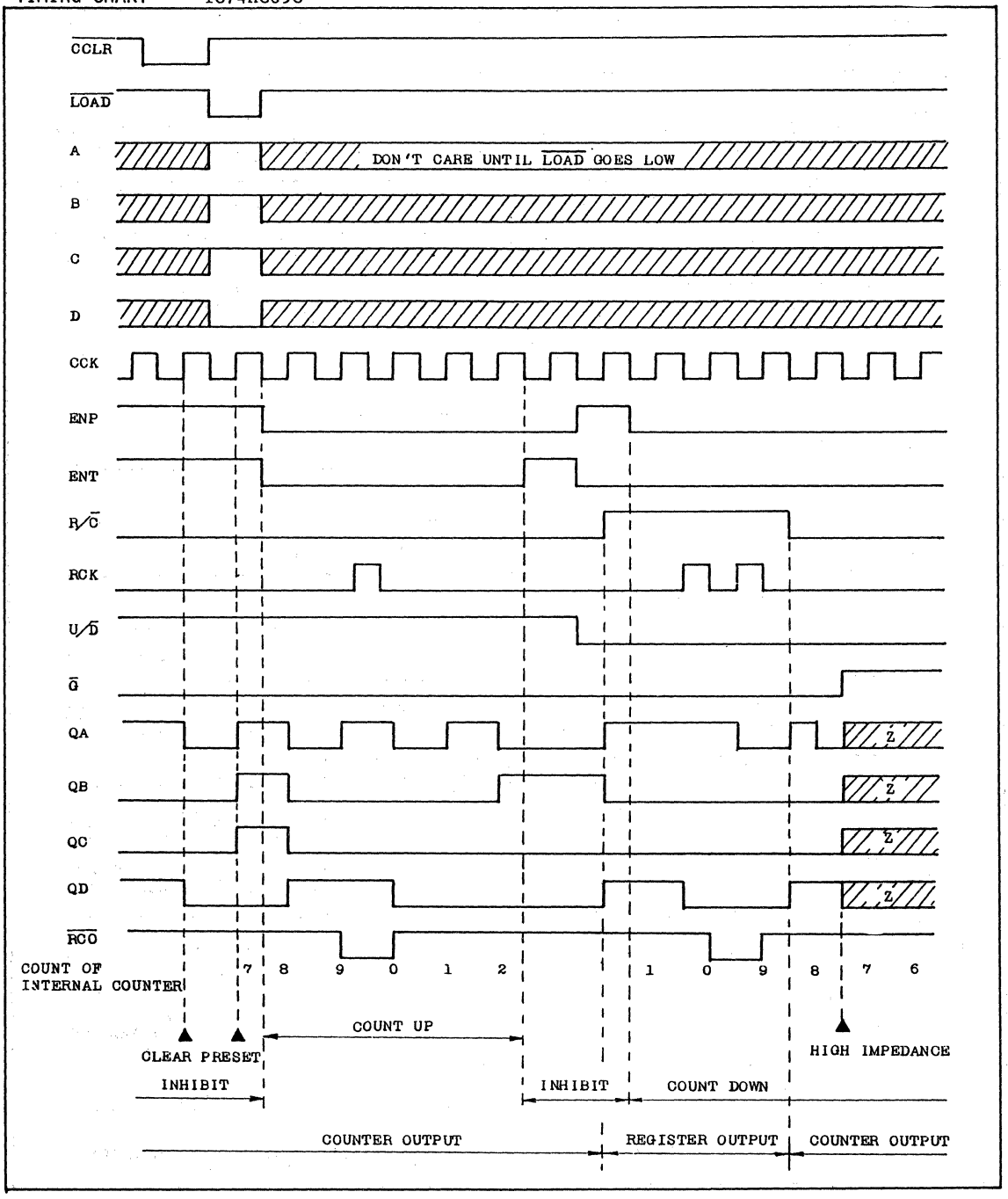
LOGIC DIAGRAM TC74HC699



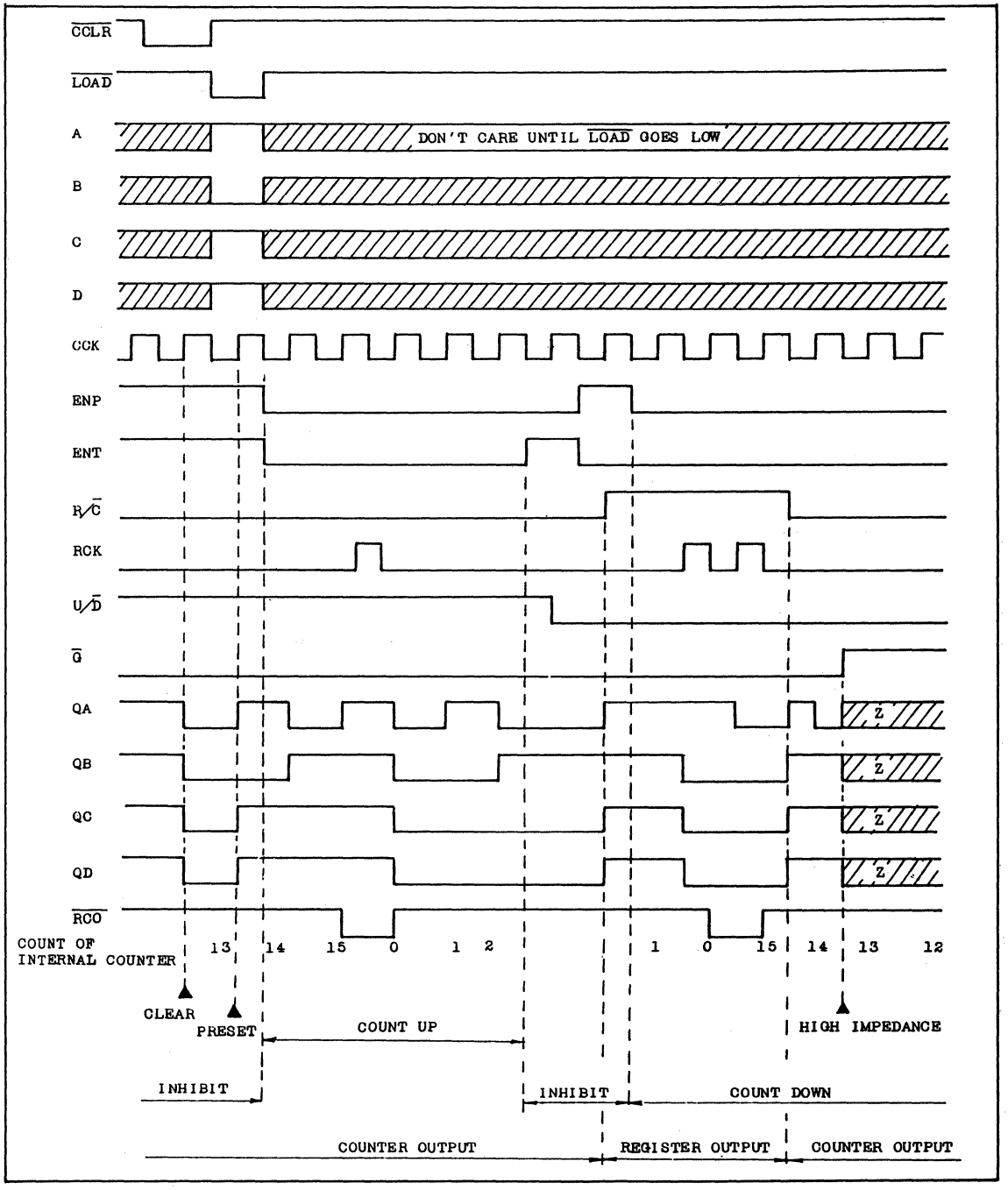
TRUTH TABLE OF INTERNAL F/F

R	D	CK	Q	$\overline{Q}$
L	X	↑	L	H
H	H	↑	H	L
H	L	↑	L	H
H	X	↓	No Change	

TIMING CHART TC74HC698



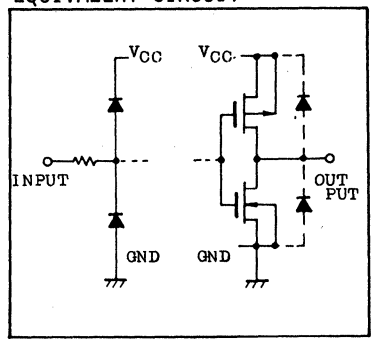
TIMING CHART TC74HC699



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QD	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		$\overline{RCO}$	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QD	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		$\overline{RCO}$	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time ($\overline{RCO}$)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CCK - Q)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (RCK - Q)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	144	275	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (R/$\overline{C}$ - Q)	t_{pLH} t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Propagation Delay Time ($\overline{ENT}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Maximum Clock Frequency (CCK, RCK)	f_{MAX}		2.0	3.5	7	-	2.5	-	MHz
			4.5	18	28	-	14	-	
			6.0	21	33	-	16	-	
Minimum Pulse Width (CCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	44	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time ($\overline{LOAD}$, $\overline{ENP}$, $\overline{ENT}$)	t_s		2.0	-	84	200	-	250	
			4.5	-	21	40	-	50	
			6.0	-	18	34	-	43	
Minimum Set-up Time (A, B, C, D)	t_s		2.0	-	16	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	

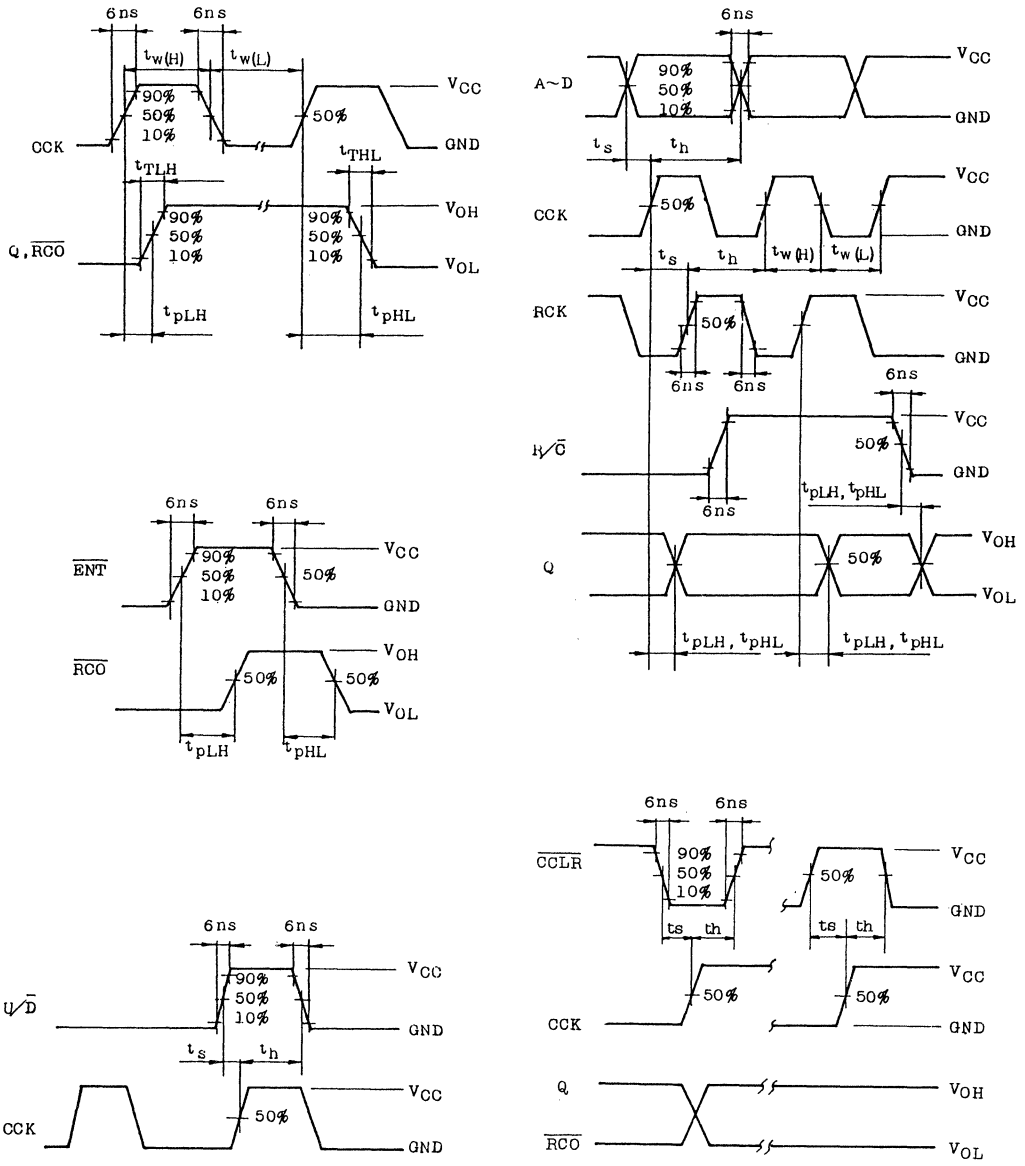
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time ($\overline{CCLR}$)	t_s		2.0	-	12	50	-	65	ns
			4.5	-	3	10	-	13	
			6.0	-	2.5	9	-	11	
Minimum Set-up Time (U/$\overline{D}$)	t_s		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Set-up Time (CCK - RCK)	t_s		2.0	-	48	125	-	160	
			4.5	-	12	25	-	32	
			6.0	-	10	21	-	27	
Minimum Hold Time	t_h		2.0	-	-	25	-	36	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	145	-	180	
			4.5	-	20	29	-	36	
			6.0	-	17	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD} (1)			-	113	-	-	-	

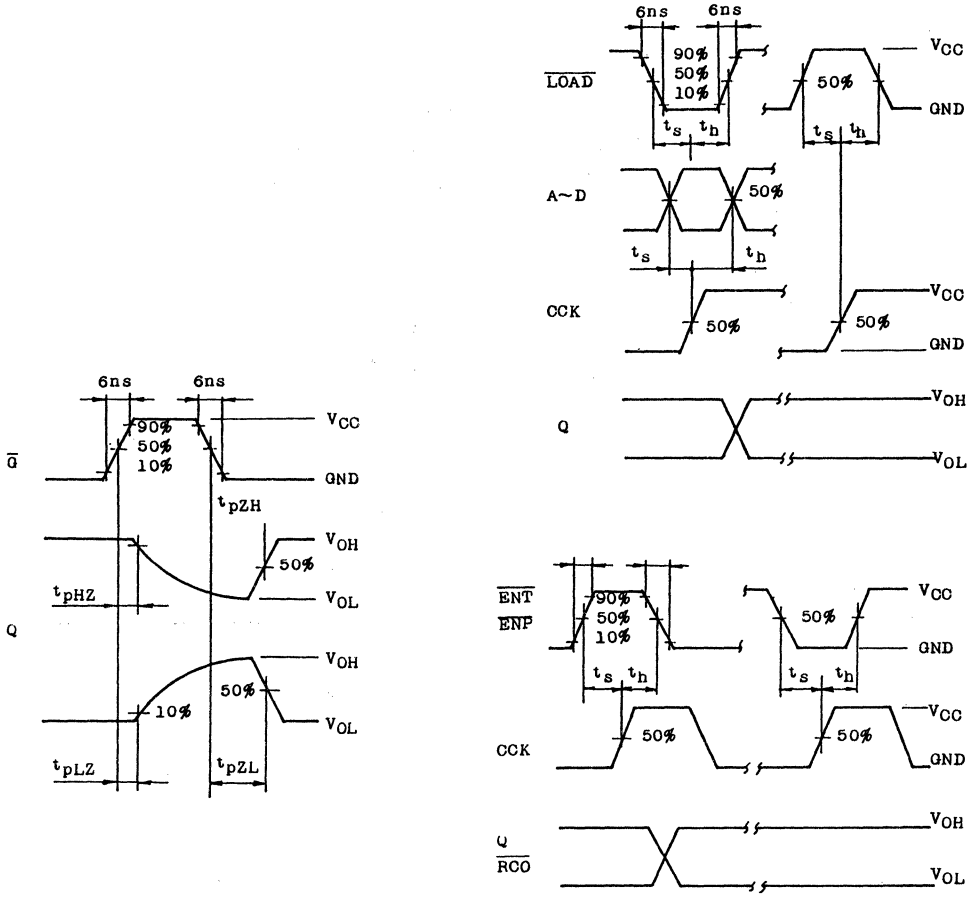
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.)=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

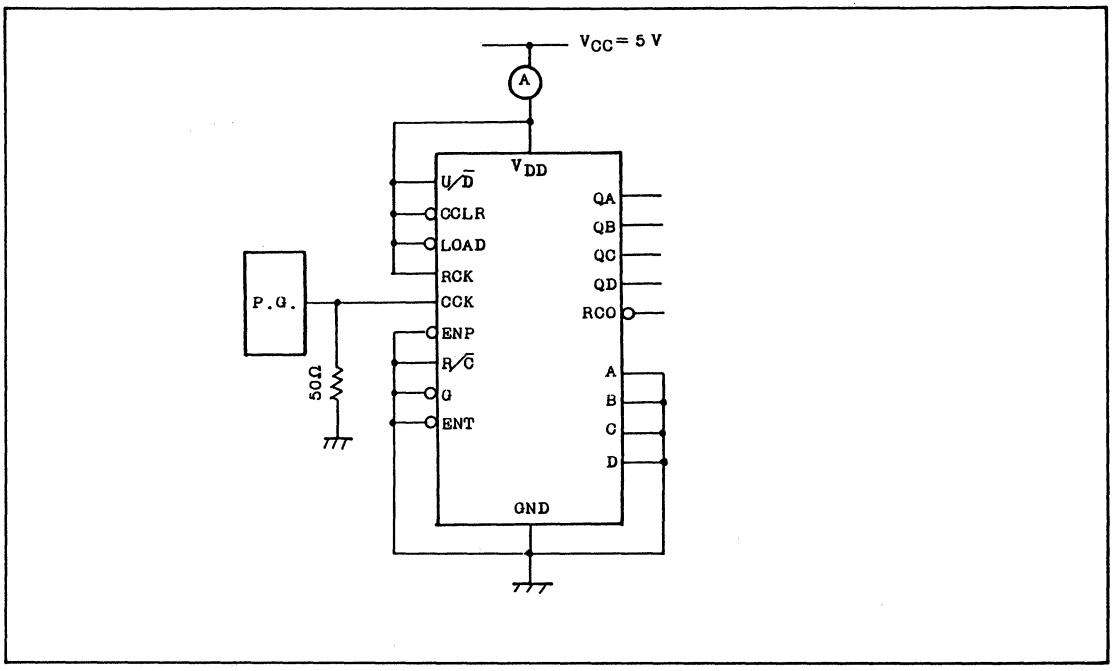
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



I_{CC}(Opr.) TEST CIRCUIT



TC74HC4002AP/AF

DUAL 4-INPUT NOR GATE

The TC74HC4002A is a high speed CMOS 4-INPUT NOR GATE fabricated with sillicon gate C^2MOS technology.

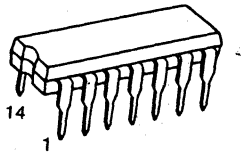
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including a buffer output, which provide high noise immunity and stable output.

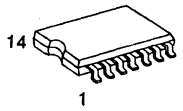
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4002B.

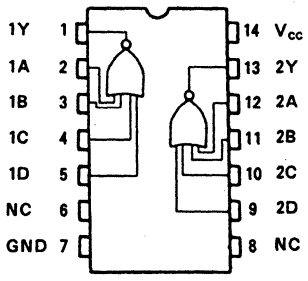


P(DIP14-P-300)



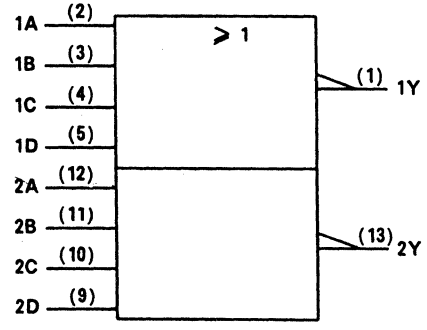
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L
L	L	L	L	H

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	10	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	40	100	–	125	
			4.5	–	13	20	–	25	
			6.0	–	11	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	22	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

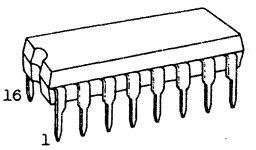
$$I_{CC(pd)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{(per Gate)}$$

TC74HC4017P/F DECADE COUNTER/DIVIDER

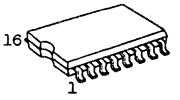
The TC74HC 4017 is a high speed CMOS DECADE JOHNSON COUNTER fabricated with silicon C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 5-stage divided-by-10 Johnson counter with 10 decoded output (Q0 - Q10) and carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{CE}$ input is held low, or it is advanced on the negative edge of the clock enable signal ($\overline{CE}$) when CLOCK input is held high, and selected one of ten outputs goes high. Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4017B



DIP16(3D16A-P)



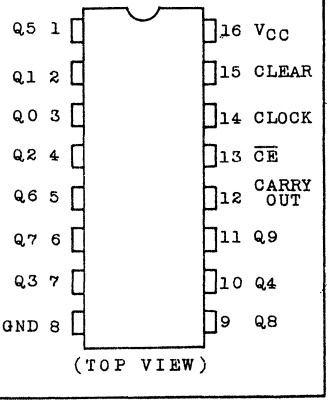
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



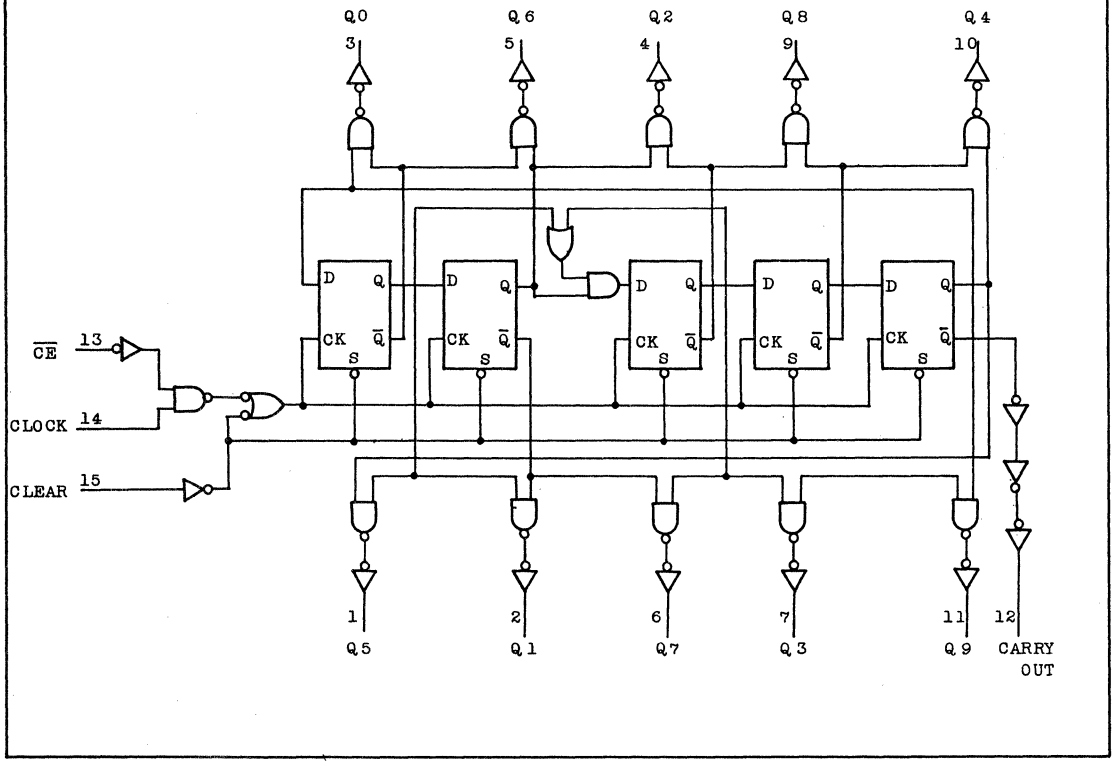
(TOP VIEW)

TRUTH TABLE

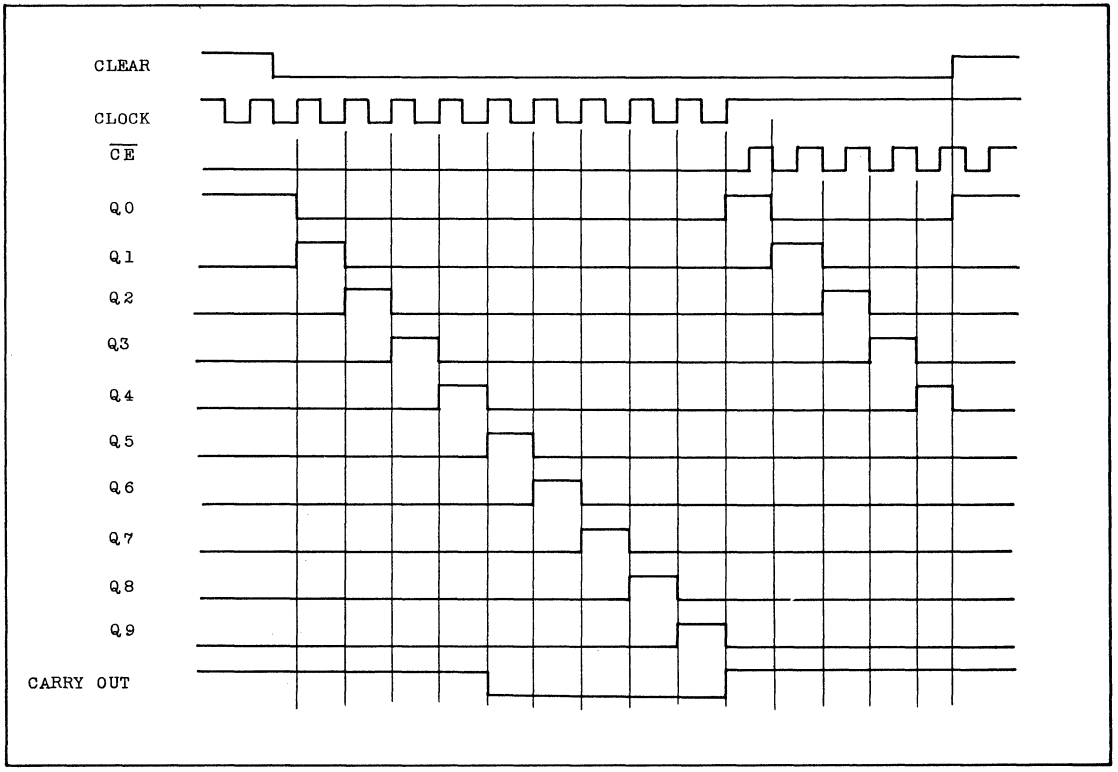
CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↑	L	L	Qn+1
↓	L	L	Qn
H	↑	L	Qn
H	↓	L	Qn+1

X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



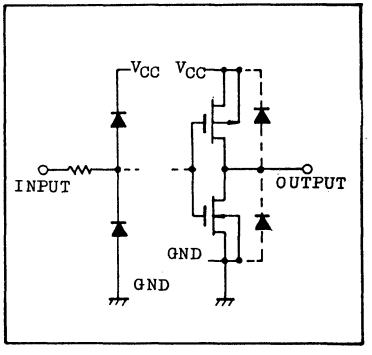
TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK, $\overline{CE}$ - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

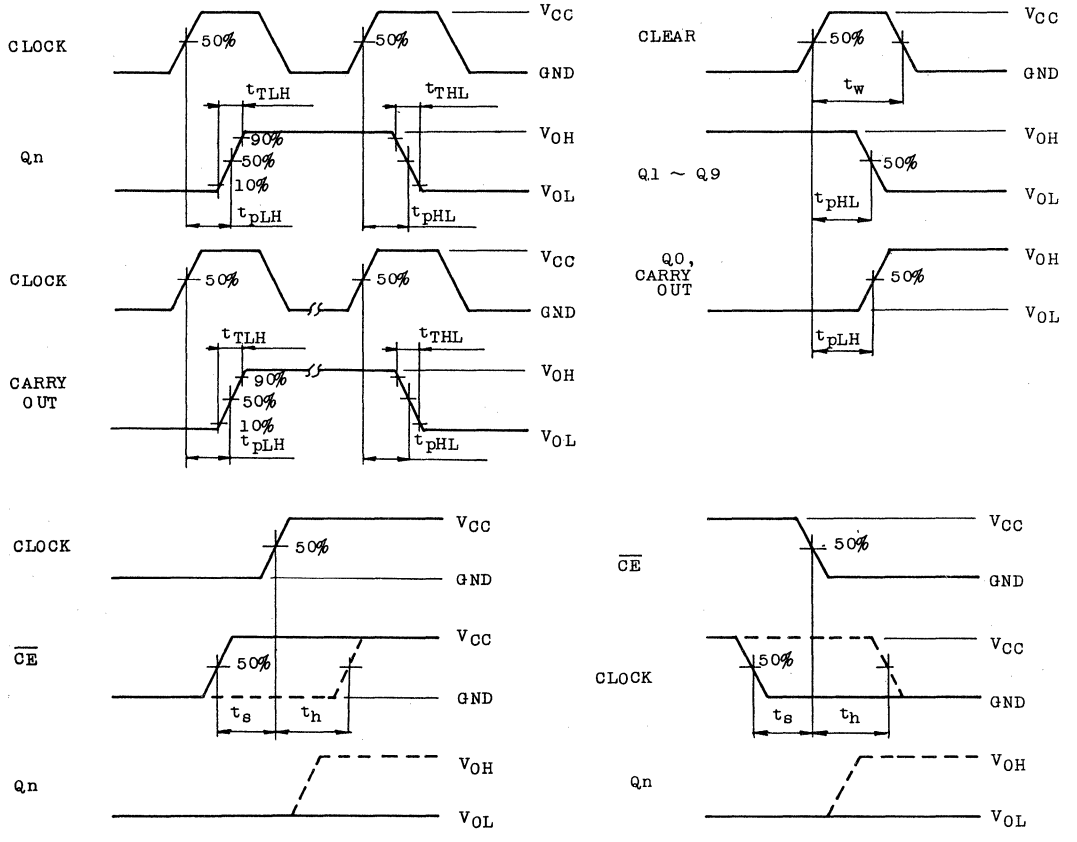
AC ELECTRICAL CAHRACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	41	-	20	-	
			6.0	29	48	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	74	-	-	-	

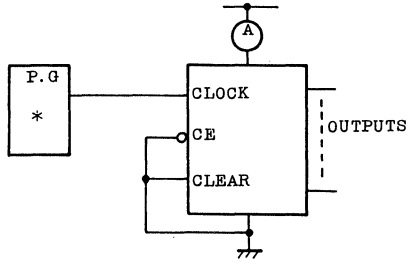
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4020AP/AF/AFN
TC74HC4040AP/AF/AFN

TC74HC4020AP/AF/AFN 14-STAGE BINARY COUNTER
TC74HC4040AP/AF/AFN 12-STAGE BINARY COUNTER

The TC74HC4020A/TC74HC4040A are high speed CMOS BINARY COUNTER/DIVIDERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS dissipation.

The TC74HC4020A is a 14-STAGE BINARY COUNTER, and the TC74HC4040A is a 12-STAGE BINARY COUNTER.

Setting CLEAR to high resets the counter to low.

A negative transition on the CLOCK input brings one increment into the counter.

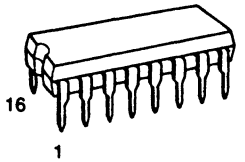
The TC74HC4020A provides 12 divided outputs: 1'st stage and stage 4 thru stage 14. At Q14, a 1/16384 divided frequency will be output.

The TC74HC4040A provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

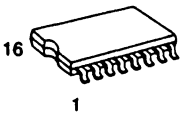
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

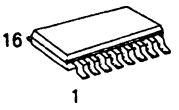
FEATURES:

- High Speed ····· f_{MAX}=60MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 4020B/4040B



P(DIP16-P-300A)





F(SOP16-P-300) FN(SOL16-P-150)

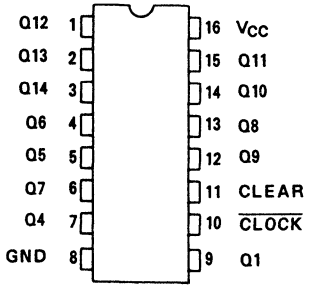
TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
⎍	L	NO CHANGE
⎎	L	ADVANCE TO NEXT STATE

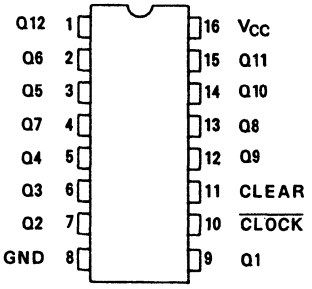
X : DON'T CARE

PIN ASSIGNMENT

TC74HC4020A

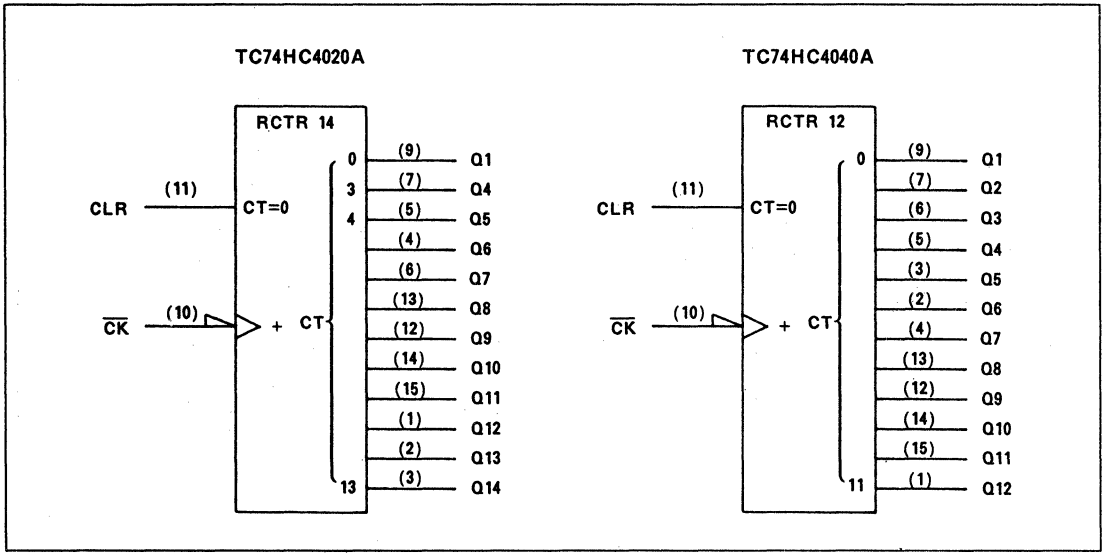


TC74HC4040A



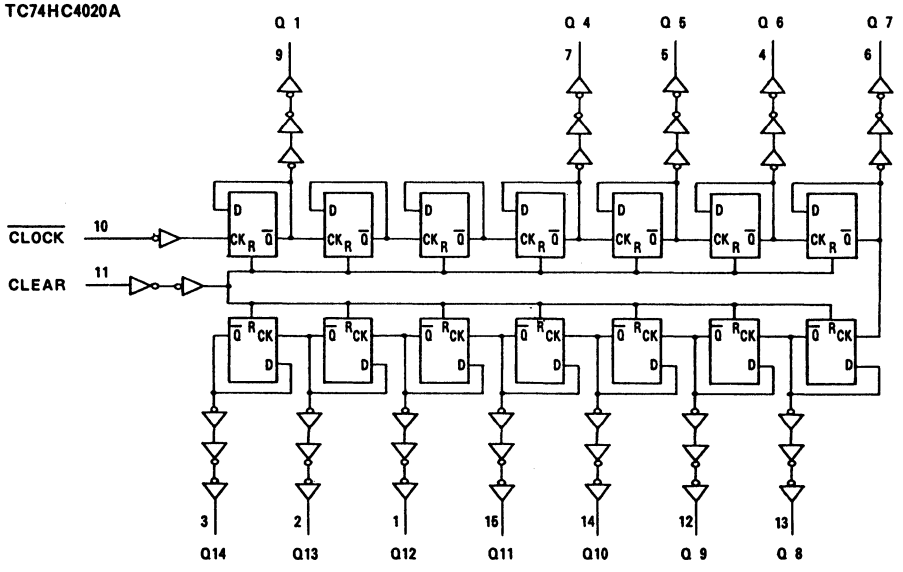
(TOP VIEW)

IEC LOGIC SYMBOL

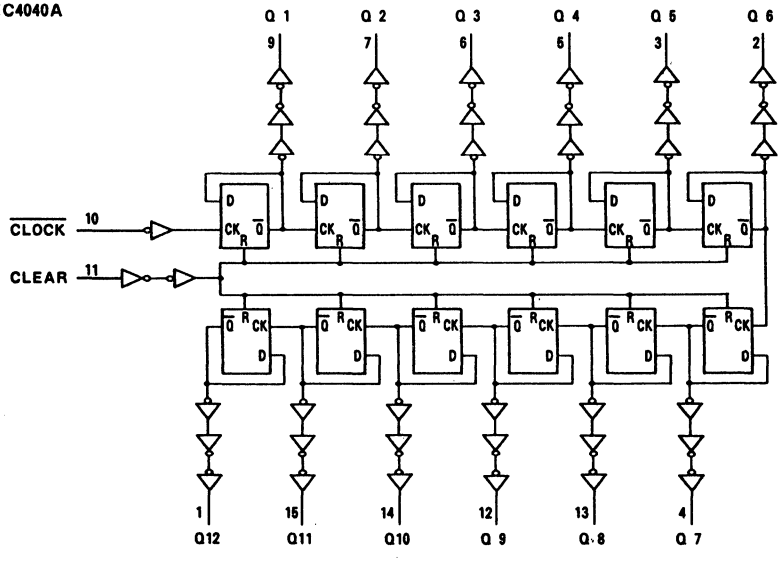


SYSTEM DIAGRAM

TC74HC4020A



TC74HC4040A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃				Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q1)	t_{pLH} t_{pHL}		−	16	24	
Propagation Delay Time (Qn−Qn+1)	t_{pLH} t_{pHL}		−	5	14	
Propagation Delay Time (CLEAR)	t_{pLH} t_{pHL}		−	14	24	
Maximum Clock Frequency	f_{MAX}		33	73	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q1)	t_{pLH} t_{pHL}		2.0	−	70	145	−	180	
			4.5	−	20	29	−	36	
			6.0	−	17	25	−	31	
Propagation Delay Time (Qn−Qn+1)	t_{pLH} t_{pHL}		2.0	−	20	75	−	95	
			4.5	−	6	15	−	19	
			6.0	−	4	13	−	16	
Propagation Delay Time (CLEAR)	t_{pLH} t_{pHL}		2.0	−	55	140	−	175	
			4.5	−	17	28	−	35	
			6.0	−	14	24	−	30	
Maximum Clock Frequency	f_{MAX}		2.0	6	17	−	5	−	MHz
			4.5	30	66	−	24	−	
			6.0	35	78	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4020A		−	27	−	−	−	
		TC74HC4040A		−	37	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4022AP/AF

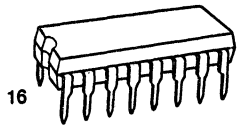
OCTAL COUNTER/DIVIDER

The TC74HC4022A is a high speed CMOS OCTAL COUNTER DIVIDER fabricated with silicon gate C^2 MOS technology.

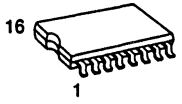
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 4-stage divide-by-8 Johnson counter with 8 decoded outputs (Q0~Q7) and a carry-out bit.

This counter is advanced on the positive edge of clock signal when $\overline{\text{CLOCK ENABLE}}$ input is held low, or it is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high. By holding the CLEAR input high, the counter is cleared to its zero state without regard to the other input conditions.

All inputs are equipped with protection circuits against static discharge or tansient excess voltage.



P(DIP16-P-300A)

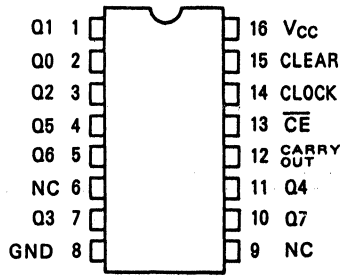


F(SOP16-P-300)

FEATURES:

- High Speed ..... f_{MAX}=57MHz(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4022B

PIN ASSIGNMENT



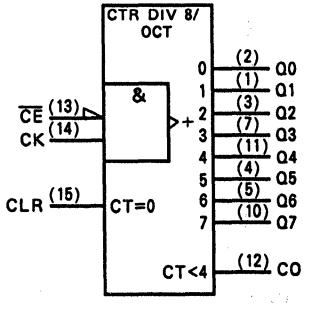
(TOP VIEW)

TRUTH TABLE

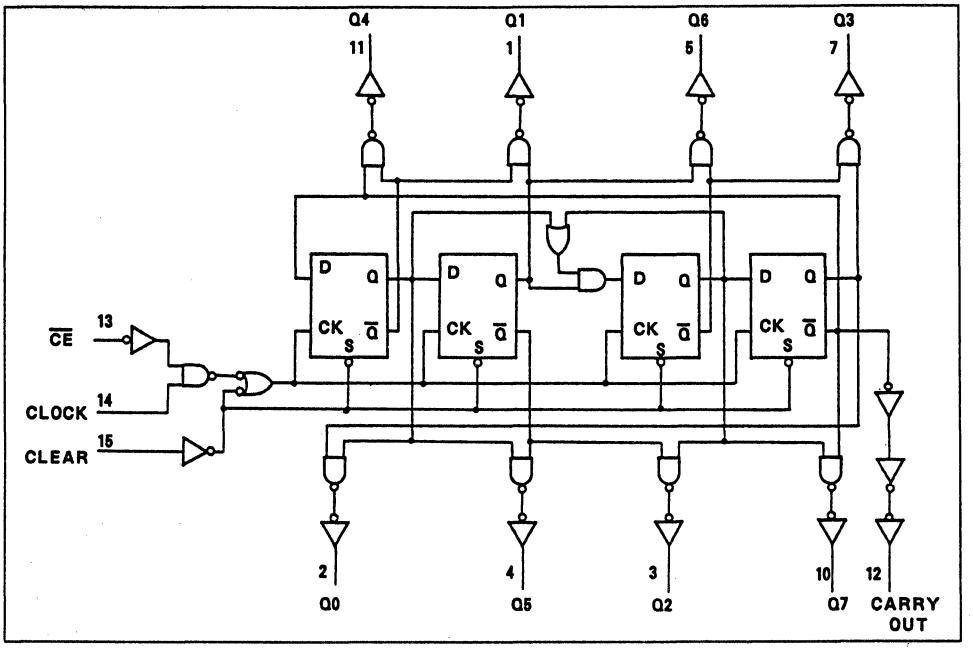
INPUTS			DECODE OUTPUT(H)
CLOCK	$\overline{\text{CE}}$	CLEAR	
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↑	L	L	Qn+1
↓	L	L	Qn
H	↑	L	Qn
H	↓	L	Qn+1

X:DON'T CARE
Qn:NO CHANGE

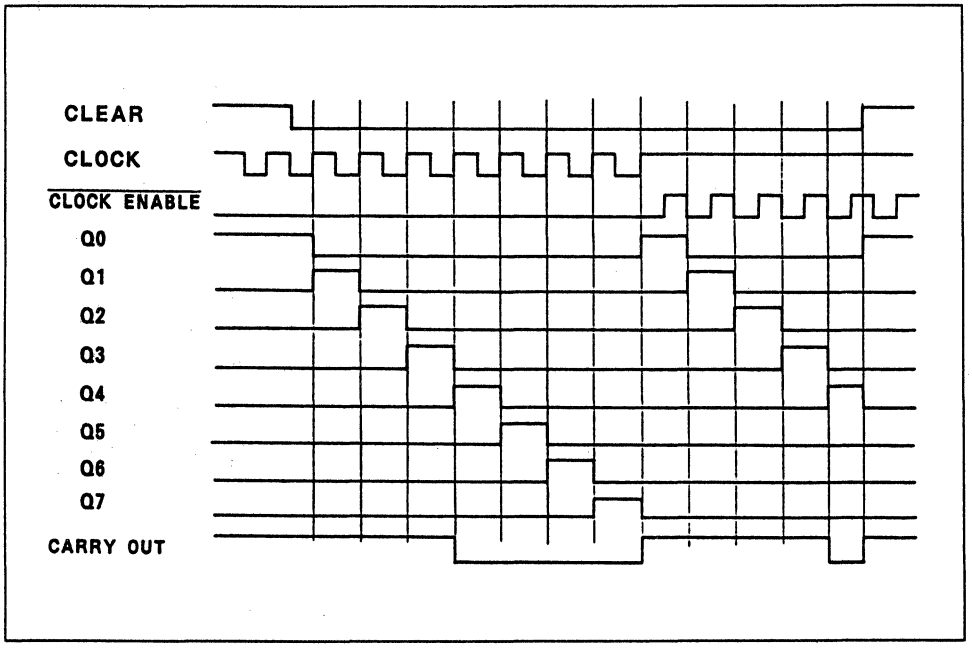
IEC LOGIC SYMBOL



SYSTEM DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time	t_h		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	−	50	65	
			4.5	−	10	19	
			6.0	−	9	16	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK, $\overline{CE}$−Q, CARRY)	t_{pLH} t_{pHL}		−	17	27	
Propagation Delay Time (CLEAR−Q, CARRY)	t_{pLH} t_{pHL}		−	15	25	
Maximum Clock Frequency	f_{MAX}		33	57	−	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK, $\overline{CE}$−Q, CARRY)	t_{pLH} t_{pHL}		2.0	−	71	160	−	200	
			4.5	−	21	32	−	40	
			6.0	−	16	27	−	34	
Propagation Delay Time (CLEAR−Q, CARRY)	t_{pLH} t_{pHL}		2.0	−	69	145	−	180	
			4.5	−	19	29	−	36	
			6.0	−	15	25	−	31	
Maximum Clock Frequency	f_{MAX}		2.0	6	11	−	5	−	MHz
			4.5	31	51	−	25	−	
			6.0	36	63	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	53	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4024AP/AF

7-STAGE BINARY COUNTER

The TC74HC4024A is a high speed CMOS 7-STAGE BINARY COUNTER fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A negative transition on the $\overline{\text{CLOCK}}$ input brings one increment to the counter.

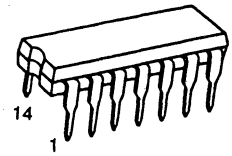
A CLEAR input is used to reset the counter to the all low level state . A high level at CLEAR accomplishes the reset function.

All divided output stages are provided, and at the last stage, 1/128 divided frequency will be obtained.

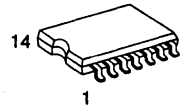
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=70MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4024B

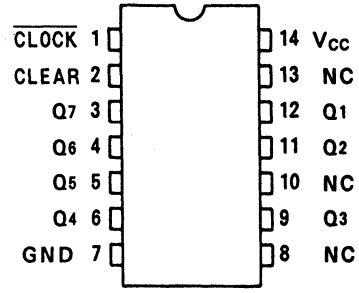


P(DIP14-P-300)



F(SOP14-P-300)

PIN ASSIGNMENT



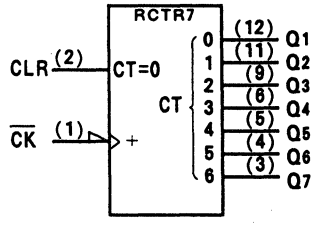
(TOP VIEW)

TRUTH TABLE

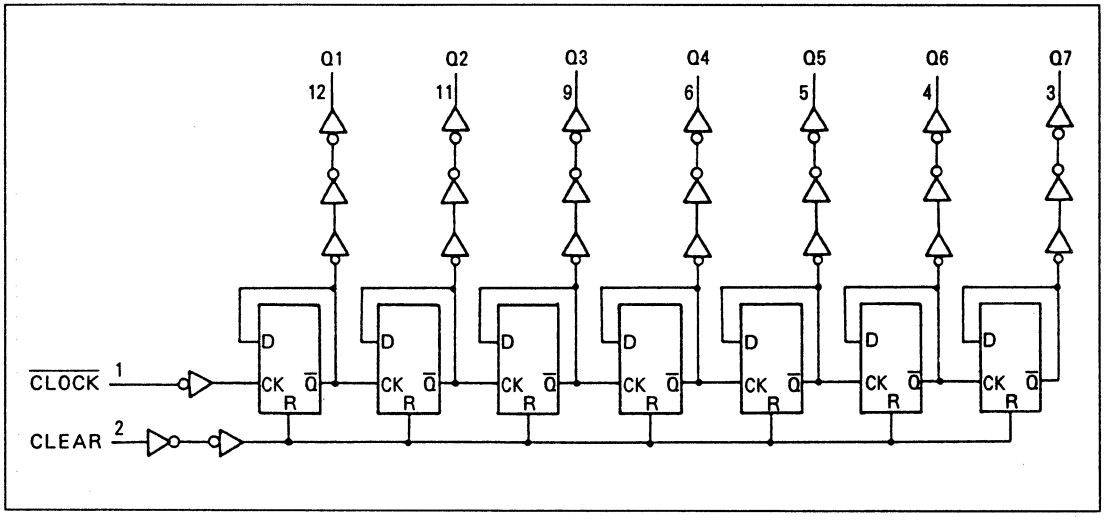
INPUTS		OUTPUT STATUS
CLOCK	CLEAR	
X	H	ALL OUTPUTS="L"
↑	L	NO CHANGE
↓	L	ADVANCE TO NEXT STAGE

X:Don't care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (CLEAR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time	t_{rem}		2.0	−	25	30	
			4.5	−	5	6	
			6.0	−	5	5	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	31	25	
			6.0	−	36	29	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time ($\overline{CLOCK}$−Q1)	t_{pLH} t_{pHL}		−	13	20	
Propagation Delay Time (Qn−Qn+1)	Δt_{pd}		−	4	9	
Propagation Delay Time (CLEAR−Qn)	t_{pLH} t_{pHL}		−	13	20	
Maximum Clock Frequency	f_{MAX}		34	70	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L=50pF$, Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time ($\overline{CLOCK}$−Q1)	t_{pLH} t_{pHL}		2.0	−	60	120	−	150	
			4.5	−	16	24	−	30	
			6.0	−	13	20	−	26	
Propagation Delay Time (Qn−Qn+1)	Δt_{pd}		2.0	−	24	60	−	75	
			4.5	−	6	12	−	15	
			6.0	−	5	10	−	13	
Propagation Delay Time (CLEAR−Qn)	t_{pLH} t_{pHL}		2.0	−	50	120	−	150	
			4.5	−	16	24	−	30	
			6.0	−	13	20	−	26	
Maximum Clock Frequency	f_{MAX}		2.0	6	17	−	5	−	MHz
			4.5	31	63	−	25	−	
			6.0	36	73	−	29	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	36	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4028AP/AF

BCD-TO-DECIMAL DECODER

The TC74HC4028A is a high speed CMOS BCD-to-DECIMAL DECODER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

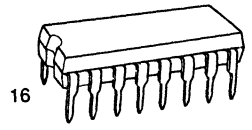
A BCD code applied to the four inputs (A-D) sets a high level at one of ten decoded outputs. A illegal BCD code such as eleven thru fifteen sets all outputs low. This device can be used as 3-to-8 LINE DECODER when input D is held high.

This device is useful for code conversion , address decoding , memory selection , multiplexing , or readout decoding.

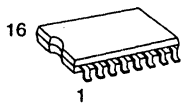
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=18ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4028B

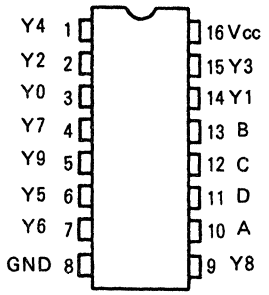


P(DIP16-P-300A)



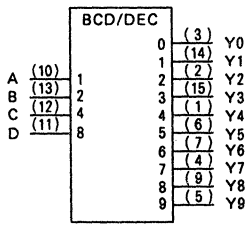
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

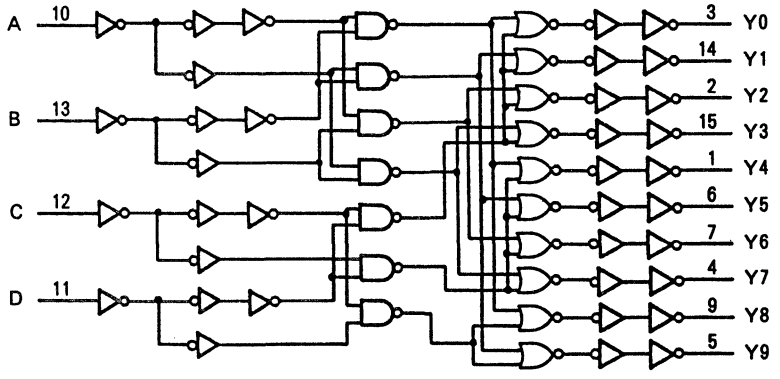


TRUTH TABLE

INPUTS				OUTPUTS										SELECTED OUTPUT
D	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y2
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

X;Don't care

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	18	34	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A,B,C,D−Y)	t_{pLH} t_{pHL}		2.0	–	80	180	–	225	
			4.5	–	22	36	–	45	
			6.0	–	18	31	–	38	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	44	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4049AP/AF/AFN
TC74HC4050AP/AF/AFN

TC74HC4049AP/AF/AFN HEX BUFFER CONVERTER(INVERTING)
TC74HC4050AP/AF/AFN HEX BUFFER CONVERTER

The TC74HC4049A and TC74HC4050A are high speed CMOS HEX BUFFERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

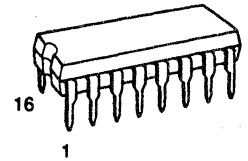
The TC74HC4049A is an inverting buffer, while the TC74 HC4050A is a non-inverting buffer. The internal circuits are composed of 3-stages (HC4049A) or 2-stages (HC405 0A) of inverters, which provide high noise immunity and stable output.

Input protection circuits are different from those of other high speed CMOS IC's. They eliminate the diodes on the V_{CC} side thus providing of logic-level conversion from high-level voltages up to 15V to low-level voltages.

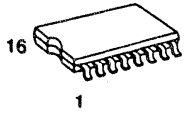
They are useful for battery back up circuits, because input voltage can be applied on IC's which are not biased by V_{CC} .

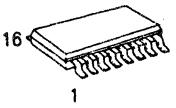
FEATURES:

- High Speed ····· t_{pd}=9ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4049B/4050B



P(DIP16-P-300A)



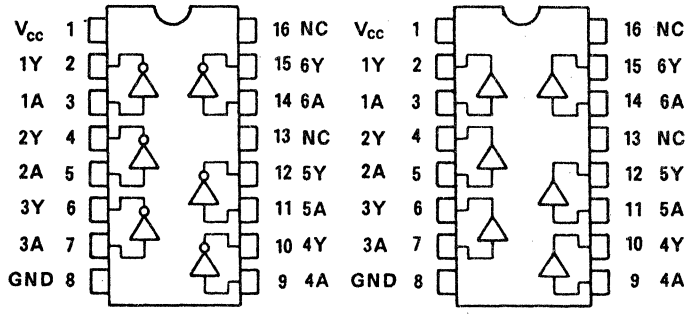


F(SOP16-P-300) FN(SOL16-P-150)

TRUTH TABLE

A	Y(4049A)	Y(4050A)
L	H	L
H	L	H

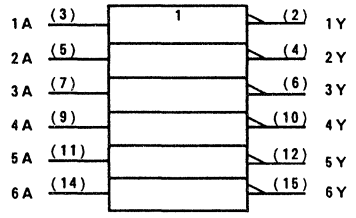
PIN ASSIGNMENT



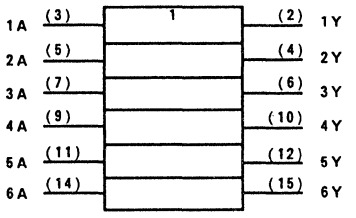
(Top View) NC : No Connection

IEC LOGIC SYMBOL

TC74HC4049A

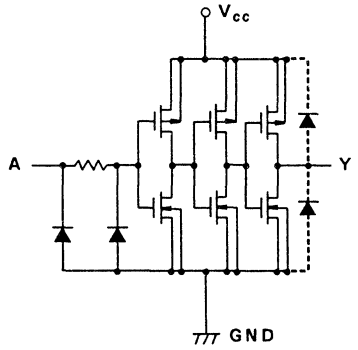


TC74HC4050A

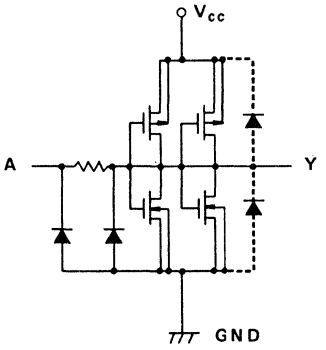


INPUT and OUTPUT EQUIVALENT CIRCUIT

TC74HC4049A



TC74HC4050A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ 18*	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)**/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

Note)

* DC input voltage (V_{IN}) specified is measured to GND and is not related to V_{CC}. Recommended operating range is 0V to 15V and it is possible to convert logic-levels from 15V to 5V or 5V to 2V.

**500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ 15	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	6	12	−	15	
				6.0	−	5	10	−	13	
Propagation Delay Time	t_{pLH} t_{pHL}		50	2.0	−	30	75	−	95	
				4.5	−	10	15	−	19	
				6.0	−	8	13	−	16	
			150	2.0	−	45	100	−	145	
				4.5	−	15	20	−	29	
				6.0	−	13	17	−	25	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)				−	26	−	−	−	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{(per Gate)}$$

TC74HC4051AP/AF
TC74HC4052AP/AF
TC74HC4053AP/AF/AFN

TC74HC4051AP/AF 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4052AP/AF DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4053AP/AF/AFN TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel × 2 configuration and the TC74HC4053A has a 2 channel × 3 configuration.

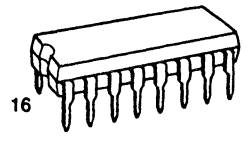
The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ($V_{CC}-V_{EE}$) can then be switched by the small logical amplitude ($V_{CC}-GND$) control signal.

For example, in the case of V_{CC}=5V, GND=0V, V_{EE}=−5V, signals between −5V and + 5V can be switched from the logical circuit with a single power supply of 5V. As the ON−resistance of each switch is low, they can be connected to circuits with low input impedance.

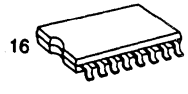
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

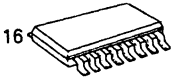
FEATURES:

- High Speed ····· t_{pd}=15ns(typ.)atV_{CC}=5V,V_{EE}=0V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Low ON Resistance ····· R_{ON}=50Ω(typ.)at $V_{CC}-V_{EE}$=9V
- High Degree of Linearity ··· THD=0.02%(typ.)at $V_{CC}-V_{EE}$=9V
- Pin and Function Compatible with 4051/4052/4053B



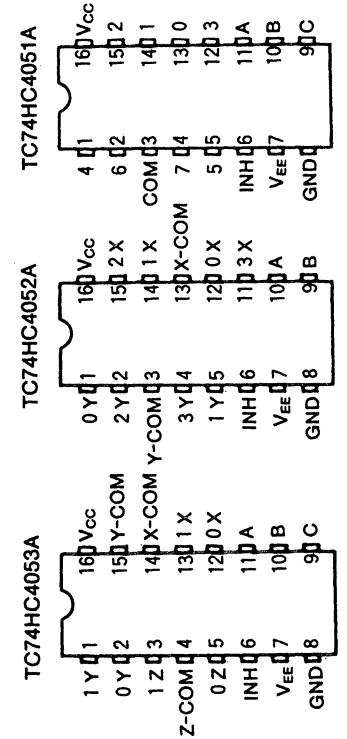
P(DIP16−P−300A)





F(SOP16−P−300) FN(SOL16−P−150)

PIN ASSIGNMENT

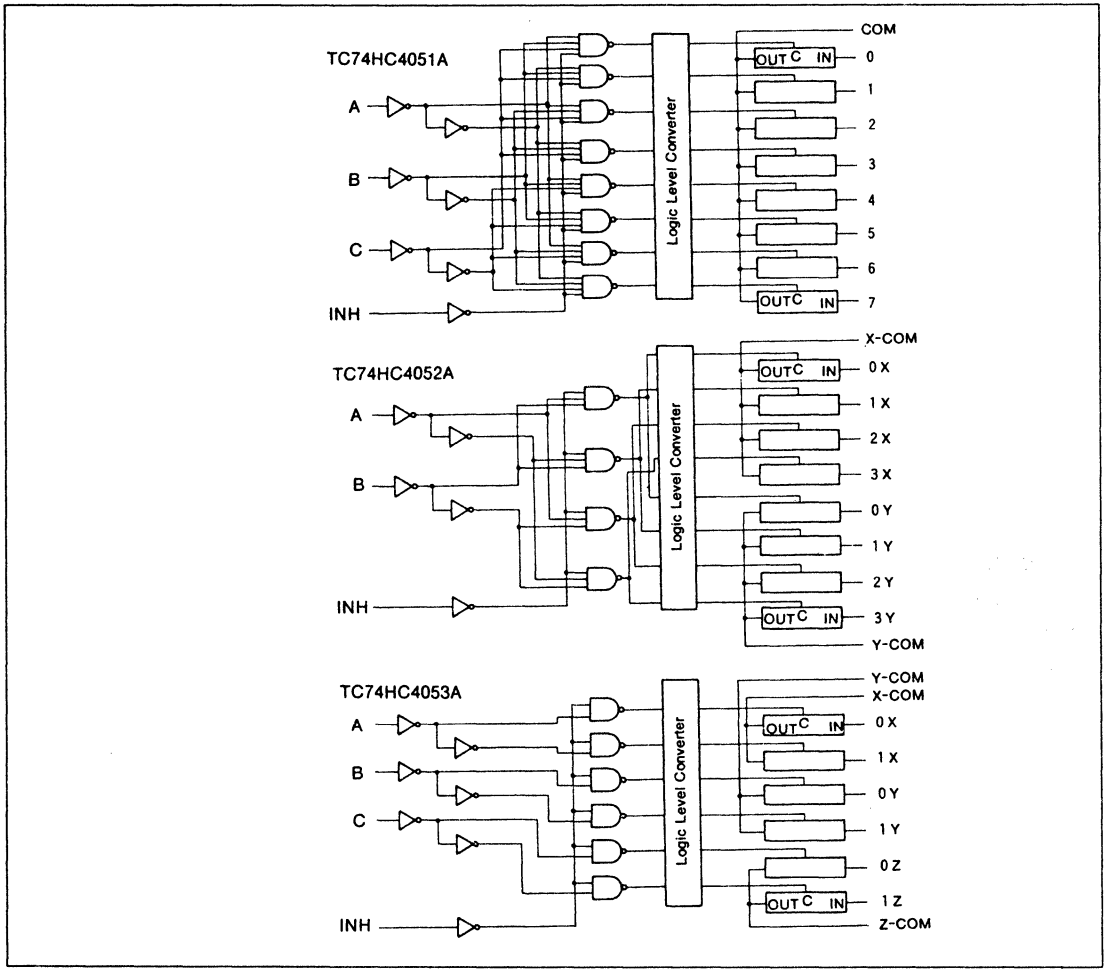


TRUTH TABLE

CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	— —	0X, 0Y, 1Z
L	H	L	H	5	— —	1X, 0Y, 1Z
L	H	H	L	6	— —	0X, 1Y, 1Z
L	H	H	H	7	— —	1X, 1Y, 1Z
H	X	X	X	NONE	NONE	NONE

X : DON'T CARE, * : Except HC4052A

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

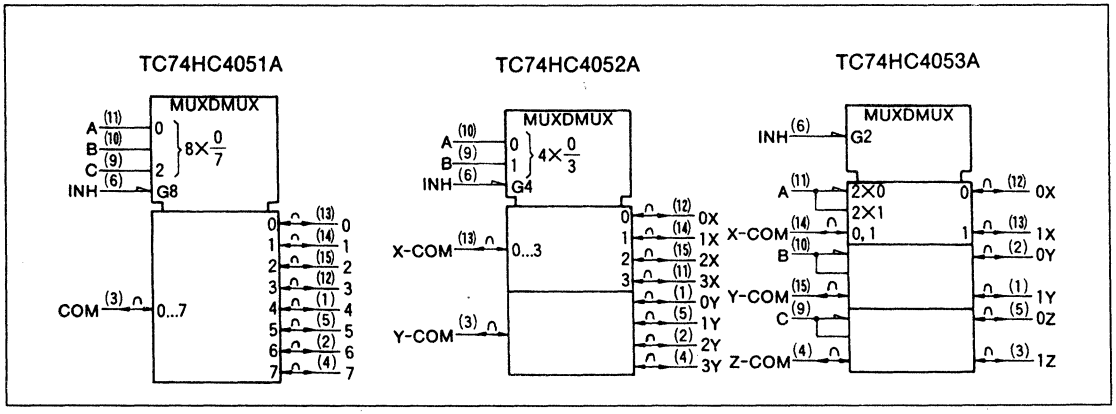
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
Supply Voltage Range	$V_{CC}-V_{EE}$	−0.5 ~13	V
Control Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
Switch I/O Voltage	$V_{I/O}$	V_{EE} −0.5 ~V_{CC}+0.5	V
Control Input Diode Current	I_{CK}	±20	mA
I/O Diode Current	I_{IOK}	±20	mA
Switch through Current	I_T	±25	mA
DC V_{CC} or GND Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	2 ~ 6	V
Supply Voltage Range	V_{EE}	−6 ~ 0	V
Supply Voltage Range	$V_{CC}-V_{EE}$	2 ~ 12	V
Control Input Voltage	V_{IN}	0 ~ V_{CC}	V
Switch I/O Voltage	$V_{I/O}$	V_{EE} ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Control Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

IEC LOGIC SYMBOL



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{EE}	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Control Input Voltage	V_{IHC}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Control Input Voltage	V_{ILC}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
ON Resistance	R_{ON}	$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND	4.5	−	85	180	−	225	Ω
			−4.5	4.5	−	55	120	−	150	
			−6.0	6.0	−	50	100	−	125	
		$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ or V_{EE} $I_{I/O} \leq 2mA$	GND	2.0	−	150	−	−	−	
			GND	4.5	−	70	150	−	190	
			−4.5	4.5	−	50	100	−	125	
			−6.0	6.0	−	45	80	−	100	
Difference of ON Resistance Between Switches	$\triangle R_{ON}$	$V_{IN}=V_{ILC}$ or V_{IHC} $V_{I/O}=V_{CC}$ to V_{EE} $I_{I/O} \leq 2mA$	GND	4.5	−	10	30	−	35	
			−4.5	4.5	−	5	12	−	15	
			−6.0	6.0	−	5	10	−	12	
Input/Output Leakage Current (SWITCH OFF)	I_{OFF}	$V_{OS}=V_{CC}$ or GND V_{IS}=GND or V_{CC} $V_{IN}=V_{ILC}$ or V_{IHC}	GND	6.0	−	−	± 60	−	± 600	nA
			−6.0	6.0	−	−	±100	−	±1000	
Switch Input Leakage Current (SWITCH ON)	I_{IZ}	$V_{OS}=V_{CC}$ or GND $V_{IN}=V_{ILC}$ or V_{IHC}	GND	6.0	−	−	± 60	−	± 600	
			−6.0	6.0	−	−	±100	−	±1000	
Control Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	GND	6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	GND	6.0	−	−	4.0	−	40.0	
			−6.0	6.0	−	−	8.0	−	80.0	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns, GND=0V)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Phase difference between Input and Output	$\varphi_{I/O}$	ALL TYPES		GND	2.0	−	25	60	−	75	ns
				GND	4.5	−	6	12	−	15	
				GND	6.0	−	5	10	−	13	
				−4.5	4.5	−	4	−	−	−	
Output Enable Time	t_{pZL}, t_{pZH}	*1	4051	GND	2.0	−	64	225	−	280	
				GND	4.5	−	18	45	−	56	
				GND	6.0	−	15	38	−	48	
				−4.5	4.5	−	18	−	−	−	
		*1	4052	GND	2.0	−	64	225	−	280	
				GND	4.5	−	18	45	−	56	
				GND	6.0	−	15	38	−	48	
				−4.5	4.5	−	18	−	−	−	
		*1	4053	GND	2.0	−	50	225	−	280	
				GND	4.5	−	14	45	−	56	
				GND	6.0	−	12	38	−	48	
				−4.5	4.5	−	14	−	−	−	
Output Disable Time	t_{pLZ}, t_{pHZ}	*1	4051	GND	2.0	−	100	250	−	315	
				GND	4.5	−	33	50	−	63	
				GND	6.0	−	28	43	−	54	
				−4.5	4.5	−	29	−	−	−	
		*1	4052	GND	2.0	−	100	250	−	315	
				GND	4.5	−	33	50	−	63	
				GND	6.0	−	28	43	−	54	
				−4.5	4.5	−	29	−	−	−	
		*1	4053	GND	2.0	−	95	225	−	280	
				GND	4.5	−	30	45	−	56	
				GND	6.0	−	26	38	−	48	
				−4.5	4.5	−	26	−	−	−	
Control Input Capacitance	C_{in}	ALL TYPES		−	−	−	5	10	−	10	pF
COMMON Terminal Capacitance	C_{IS}		4051	−5.0	5.0	−	36	70	−	70	
			4052			−	19	40	−	40	
			4053			−	11	20	−	20	
SWITCH Terminal Capacitance	C_{OS}		4051	−5.0	5.0	−	7	15	−	15	
			4052			−	7	15	−	15	
			4053			−	7	15	−	15	
Feedthrough Capacitance	C_{IOS}		4051	−5.0	5.0	−	0.95	2	−	2	
			4052			−	0.85	2	−	2	
			4053			−	0.75	2	−	2	
Power Dissipation Capacitance	C_{PD}	*2	4051	GND	5.0	−	70	−	−	−	
			4052			−	71	−	−	−	
			4053			−	67	−	−	−	

* 1: R_L=1kΩ

* 2: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

ANALOG SWITCH CHARACTERISTICS(GND=0V,Ta=25°C)

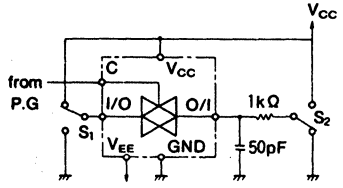
PARAMETER	SYMBOL	TEST CONDITION			V_{CC}	V_{CC}	TYP.	UNIT
Sine Wave Distortion (T.H.D)		R_L=10kΩ, C_L=50pF, f_{IN}=1kHz	V_{IN}=4.0V_{P-P}		−2.25	2.25	0.025	%
			V_{IN}=8.0V_{P-P}		−4.5	4.5	0.020	
			V_{IN}=11.0V_{P-P}		−6.0	6.0	0.018	
Frequency Response (Switch ON)	f_{MAX}	Adjust f_{IN} Voltage to obtain 0dBm at Vos; Increase f_{IN} Frequency until dB Meter reads−3dB; R_L=50Ω, C_L=10pF, f_{IN}=1MHz, Sine Wave	* 1	ALL	−2.25	2.25	120	MHz
			* 2	4051			45	
				4052			70	
				4053			95	
			* 1	ALL	−4.5	4.5	190	
			* 2	4051			70	
				4052			110	
				4053			150	
			* 1	ALL	−6.0	6.0	200	
			* 2	4051			85	
				4052			140	
				4053			190	
Feedthrough Attenuation (Switch OFF)		Vin is centered at(V_{CC}−V_{EE})/2, Adjust input for 0dBm; R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	
Crosstalk (Control Input to Signal Output)		R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Square Wave (t_r=t_f 6ns)			−2.25	2.25	60	mV
					−4.5	4.5	140	
					−6.0	6.0	200	
Crosstalk (Between any switches)		Adjust V_{IN} to obtain 0dBm at Input; R_L=600Ω, C_L=50pF, f_{IN}=1MHz, Sine Wave			−2.25	2.25	−50	dB
					−4.5	4.5	−50	
					−6.0	6.0	−50	

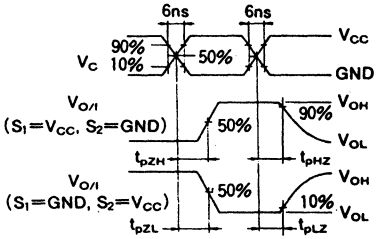
* 1: Input COMMON Terminal, and measured at SWITCH Terminal.
* 2: Input SWITCH Terminal, and measured at COMMON Terminal.

NOTE:These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUITS

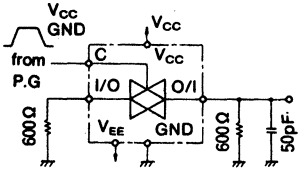
1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



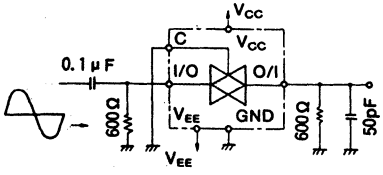


2. CROSSTALK (CONTROL INPUT–SWITCH OUTPUT)

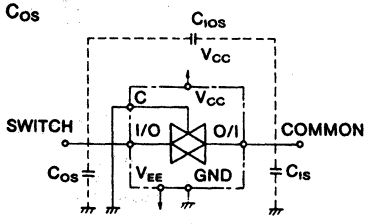
fin=1MHz duty=50% tr=tf=6ns



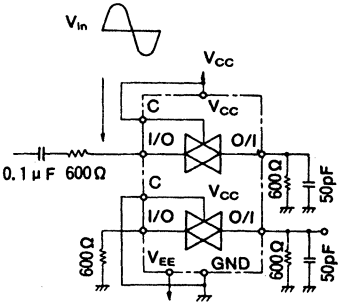
3. FEEDTHROUGH ATTENUATION



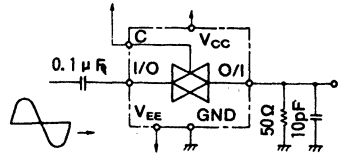
4. C_{IOS}, C_{IS}, C_{OS}



5. CROSSTALK (BETWEEN ANY TWO SWITCHES)



6. FREQUENCY RESPONSE (SWITCH ON)



14-STAGE BINARY COUNTER/OSCILLATOR

The TC74HC4060A is a high speed CMOS 14-STAGE BINARY COUNTER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The oscillator configuration allows designs using either RC or crystal oscillator circuits, or an external clock may be used.

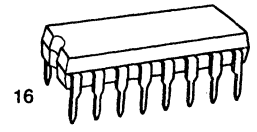
The clear input resets the counter to a low level on all outputs and disables the oscillator. A high CLEAR accomplishes this reset function.

A negative transition on the clock input ($\overline{\phi}$I) increments the counter. Ten levels of divided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. At the last stage (Q14), a 1/16384 divided frequency is obtained.

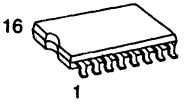
The $\overline{\phi}$I input and CLEAR input are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=58MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28%V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(opr)=2V～6 V
- Oscillator Configuration ..... RC or Crystal Oscillator
- Pin and Function Compatible with 4060B

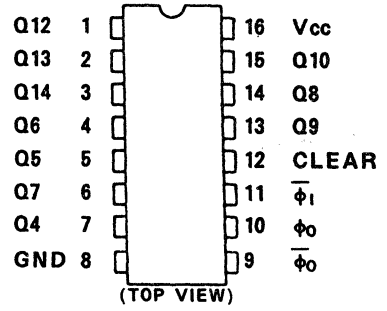


P(DIP16-P-300A)



F(SOP16-P-300)

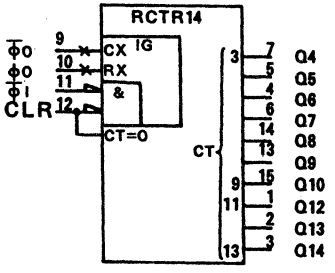
PIN ASSIGNMENT



TRUTH TABLE

INPUTS		Function
$\overline{\phi}$I	CLEAR	
X	H	Counter is reset to zero state. ϕ_O output goes to high level. $\overline{\phi}_O$ output goes to low level.
↓	L	Count up one step.
↑	L	NO change

IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃ ~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage (Qn)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
High−Level Output Voltage (ϕo, $\overline{\phi}$o)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.8	2.0	−	1.8	−	
				4.5	4.0	4.5	−	4.0	−	
				6.0	5.5	5.9	−	5.5	−	
Low−Level Output Voltage (Qn)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Low−Level Output Voltage (ϕo, $\overline{\phi}$o)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20μA	2.0	−	0.0	0.2	−	0.2	
				4.5	−	0.0	0.5	−	0.5	
				6.0	−	0.1	0.5	−	0.5	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Time (CLEAR)	$t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Removal Time	t_{rem}		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS($C_L = 15pF$, $V_{CC} = 5V$, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (CLOCK−Q4)	t_{pLH} t_{pHL}		−	36	53	
Propagation Delay Time Difference (Qn−Qn+1)	Δt_{pd}	$C_L = 15pF$ (Qn, Qn+1)	−	6	14	
Propagation Delay Time (CLEAR)	t_{pLH} t_{pHL}		−	19	34	
Maximum Clock Frequency	f_{MAX}		33	58	−	MHz

AC ELECTRICAL CHARACTERISTICS($C_L = 50pF$, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (CLOCK−Q4)	t_{pLH} t_{pHL}		2.0	−	170	300	−	375	
			4.5	−	41	60	−	75	
			6.0	−	30	51	−	64	
Propagation Delay Time Difference (Qn−Qn+1)	Δt_{pd}	$C_L = 50pF$ (Qn, Qn+1)	2.0	−	32	75	−	95	
			4.5	−	7	15	−	19	
			6.0	−	5	13	−	16	
Propagation Delay Time (CLEAR)	t_{pLH} t_{pHL}		2.0	−	85	195	−	245	
			4.5	−	23	39	−	49	
			6.0	−	17	33	−	42	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	−	5	−	MHz
			4.5	30	50	−	24	−	
			6.0	35	65	−	28	−	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}(1)			−	27	−	−	−	

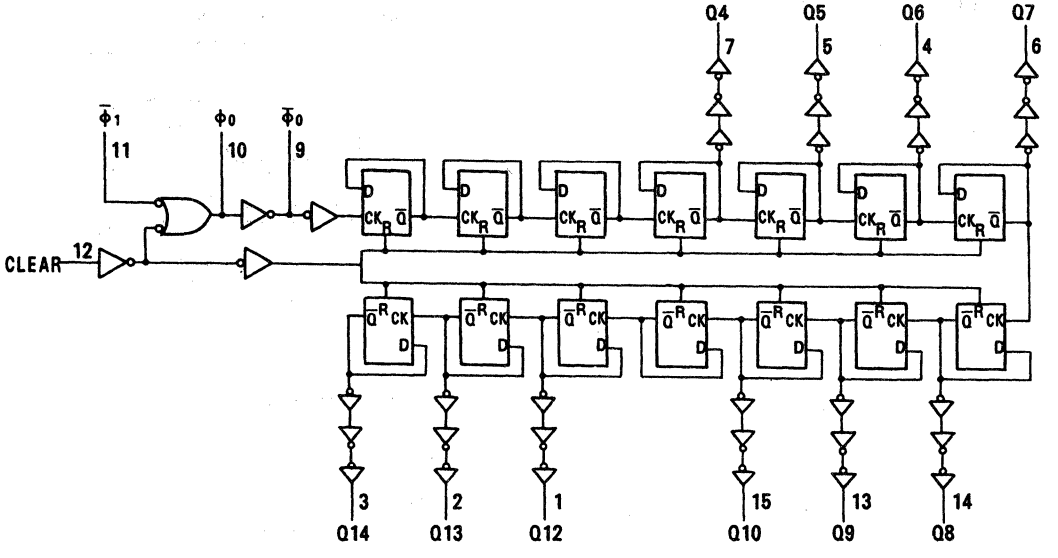
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

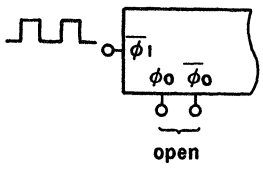
When CR or Crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the above calculation, because these oscillation circuits spend much supply current.

SYSTEM DIAGRAM

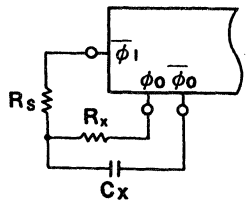


TYPICAL CLOCK DRIVE CIRCUITS

External Clock Drive

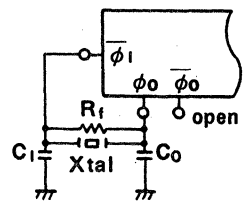


Typical RC Circuit

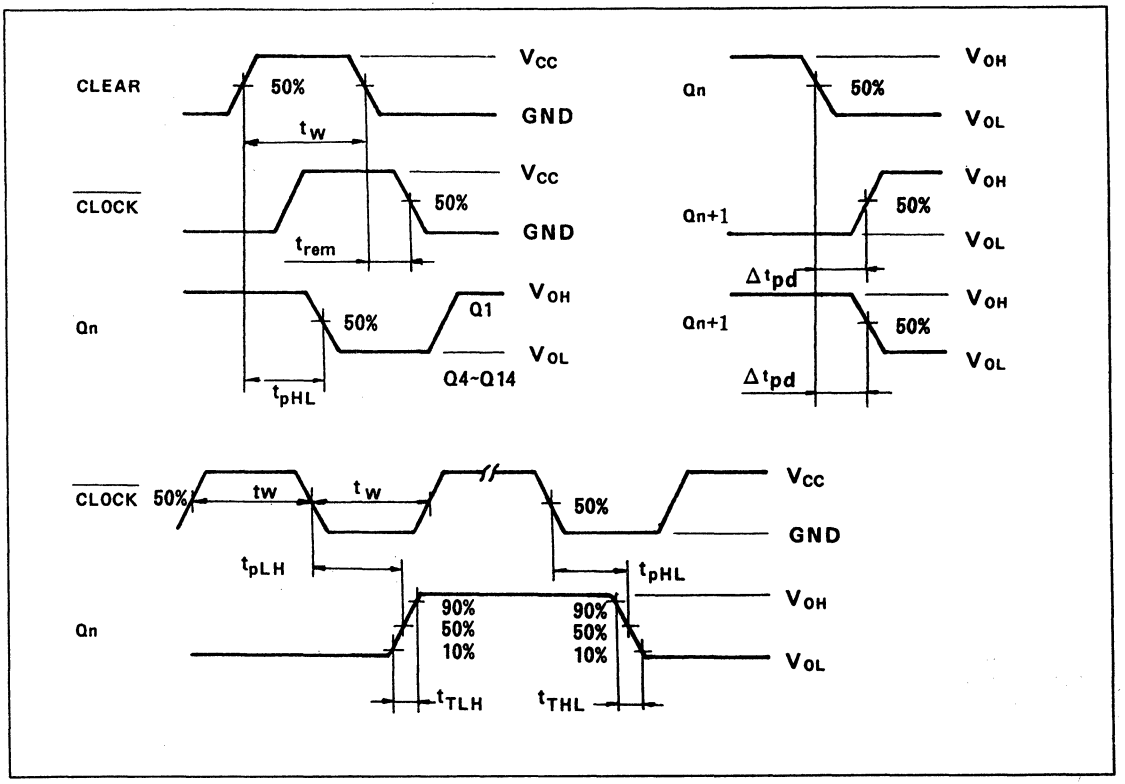


R_S : $2R_X$-$10R_X$

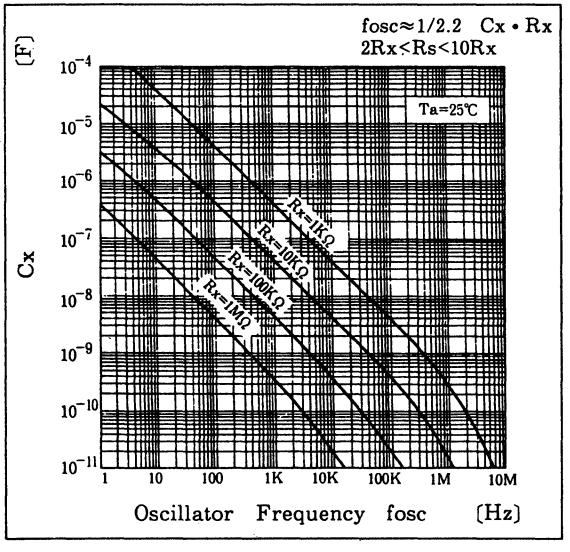
Typical Crystal Circuit



SWITCHING CHARACTERISTICS TEST WAVEFORM



CR Oscillator Characteristics (Typical)



TC74HC4066AP/AF/AFN

QUAD BILATERAL SWITCH

The TC74HC4066A is a high speed CMOS QUAD BILATERAL SWITCH fabricated with silicon gate C^2MOS technology.

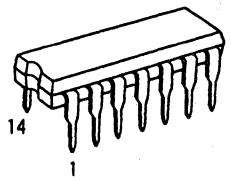
It consists of four independent high speed switches capable of controlling either digital or analog signals while maintaining the CMOS low power dissipation.

Control input (C) is provided to control the switch. The switch turns ON while the C input is high, and the switch turns OFF while low.

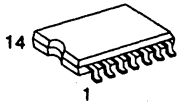
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

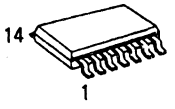
FEATURES:

- High Speed ····· t_{pd}=7ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Low ON Resistance ····· R_{ON}=50Ω(typ.)at V_{CC}=9V
- High Degree of Linearity ····· THD=0.05%(typ.)at V_{CC}=5V
- Pin and Function Compatible with 4066B



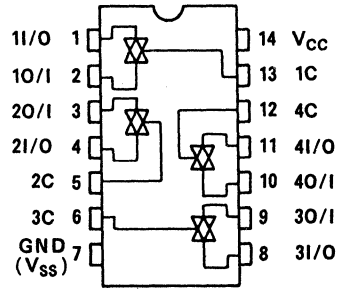
P(DIP14-P-300)





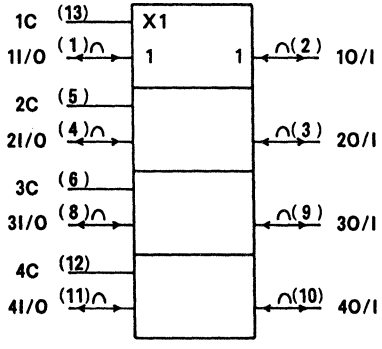
F(SOP14-P-300) FN(SOL14-P-150)

PIN ASSIGNMENT



(Top View)

IEC LOGIC SYMBOL



TRUTH TABLE

CONTROL	SWITCH FUNCTION
H	ON
L	OFF

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~13	V
Control Input Voltage	V_{IN}	−0.5 ~V_{CC} +0.5	V
Switch I/O Voltage	$V_{I/O}$	−0.5 ~V_{CC}+0.5	V
Control Input Diode Current	I_{CK}	±20	mA
I/O Diode Current	I_{IOK}	±20	mA
Switch through Current	I_T	±25	mA
DC V_{CC}/GND Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 12	V
Control Input Voltage	V_{IN}	0 ~ V_{CC}	V
Switch I/O Voltage	$V_{I/O}$	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~85	℃
Input Rise and Fall Time	tr, t f	0 ~ 1000(V_{CC}= 2.0V) 0 ~ 500(V_{CC}= 4.5V) 0 ~ 400(V_{CC}= 6.0V) 0 ~ 250(V_{CC}=10.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40~85℃ MIN.	Ta=−40~85℃ MAX.	UNIT
High−Level Control Input Voltage	V_{IHC}		2.0 4.5 9.0 12.0	1.5 3.15 6.3 8.4	− − − −	− − − −	1.5 3.15 6.3 8.4	− − − −	V
Low−Level Control Input Voltage	V_{ILC}		2.0 4.5 9.0 12.0	− − − −	− − − −	0.5 1.35 2.7 3.6	− − − −	0.5 1.35 2.7 3.6	V
ON Resistance	R_{ON}	V_{IN} = V_{IHC} $V_{I/O}$= V_{CC} toGND $I_{I/O}$≦1mA	4.5 9.0 12.0	− − −	96 55 45	170 85 80	− − −	200 100 90	Ω
		V_{IN} = V_{IHC} $V_{I/O}$= V_{CC} orGND $I_{I/O}$≦1mA	2.0 4.5 9.0 12.0	− − − −	160 70 50 45	− 100 75 70	− − − −	− 130 95 90	
Difference of ON Resistance Between Switches	$\triangle R_{ON}$	V_{IN} = V_{IHC} $V_{I/O}$= V_{CC} toGND $I_{I/O}$≦1mA	4.5 9.0 12.0	− − −	10 5 5	− − −	− − −	− − −	
Input/Output Leakage Current (SWITCH OFF)	I_{OFF}	V_{OS} = V_{CC} orGND V_{IS} = GNDorV_{CC} V_{IN} = V_{ILC}	12.0	−	−	±100	−	±1000	nA
Switch Input Leakage Current (SWITCH ON,OUTPUT OPEN)	I_{IZ}	V_{OS} = V_{CC} orGND V_{INH}= V_{IHC}	12.0	−	−	±100	−	±1000	
Control Input Current	I_{IN}	V_{IN} = V_{CC} orGND	6.0	−	−	±100	−	±1000	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} orGND	6.0 9.0 12.0	− − −	− − −	1.0 4.0 8.0	− − −	10.0 40.0 80.0	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Phase difference between Input and Output	$\phi_{I/O}$		2.0	−	10	50	−	65	
			4.5	−	4	10	−	13	
			9.0	−	3	8	−	10	
			12.0	−	3	7	−	9	
Output Enable Time	t_{pZL} t_{pZH}	R_L =1KΩ	2.0	−	18	100	−	125	ns
			4.5	−	8	20	−	25	
			9.0	−	6	12	−	22	
			12.0	−	6	12	−	18	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L =1KΩ	2.0	−	20	115	−	145	
			4.5	−	10	23	−	29	
			9.0	−	8	20	−	25	
			12.0	−	8	18	−	22	
Maximum Control Input Frequency		R_L =1KΩ, C_L =15pF, V_{OUT} =1/2V_{CC}	2.0	−	30	−	−	−	MHz
			4.5	−	30	−	−	−	
			9.0	−	30	−	−	−	
			12.0	−	30	−	−	−	
Control Inputl Capacitance	C_{IN}			−	5	10	−	10	pF
Switch Terminal Capacitance	$C_{I/O}$			−	6	−	−	−	
Feed through Capacitance	C_{IOS}			−	0.5	−	−	−	
Power Dissipation Capacitance	C_{PD}	(1)		−	15	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/4$ (per channel)

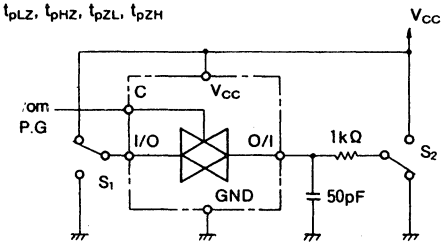
ANALOG SWITCH CHARACTERISTICS (GND=0V, Ta=25℃)

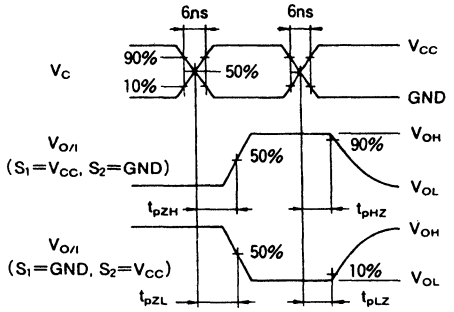
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	TYP.	UNIT
Sine Wave Distortion (T.H.D)		f_{IN} = 1kHz, R_L = 10kΩ, C_L = 50pF, V_{IN} = 4.0 V_{P-P} @ V_{CC} = 4.5V	4.5	0.05	%
		V_{IN} = 8.0 V_{P-P} @ V_{CC} = 9.0V	9.0	0.04	
Frequency Response (Swith ON)	f_{MAX}	Adjust f_{IN} voltage to obtain 0dBm at V_{OS}. Increase f_{IN} Frequency until dB Meter reads −3dB. R_L = 50Ω, C_L = 10pF, f_{IN} = 1MHz, Sine Wave	4.5	200	MHz
			9.0	200	
Feedthrough Attenuation (Switch OFF)		Vin is centered at V_{CC}/2. Adjust input for 0dBm. R_L = 600Ω, C_L = 50pF, f_{IN} = 1MHz, Sine Wave	4.5	−60	dB
			9.0	−60	
Crosstalk (Control Input to Signal Output)		R_L = 600Ω, C_L = 50pF, f_{IN} = 1MNz, Square Wave ($t_r=t_f$ = 6ns)	4.5	60	mV
			9.0	100	
Crosstalk (Between any switches)		Adjust V_{IN} to obtain 0dBm at Input. R_L = 600Ω, C_L = 50pF, f_{IN} = 1MHz, Sine Wave	4.5	−60	dB
			9.0	−60	

NOTE: These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUITS

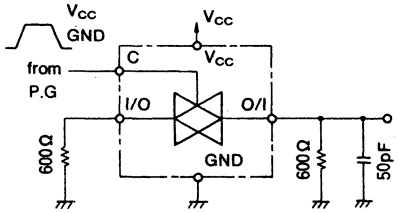
1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



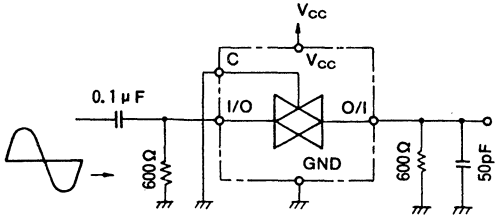


2. **CROSSTALK (CONTROL INPUT–SWITCH OUTPUT)**

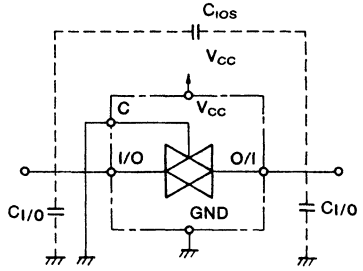
fin=1MHz duty=50% tr=tf=6ns



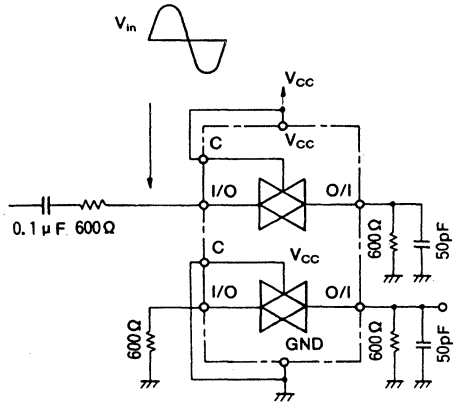
3. FEEDTHROUGH ATTENUATION



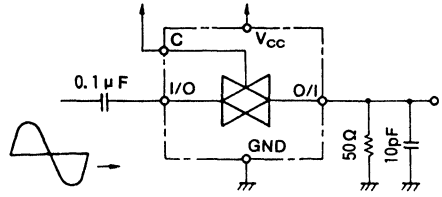
4. Clos,C I/O



5. CROSSTALK(BETWEEN ANY TWO SWITCHES)



6. FREQUENCY RESPONSE(SWITCH ON)



TC74HC4072AP/AF

DUAL 4-INPUT OR GATE

The TC74HC4072A is a high speed CMOS 4-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

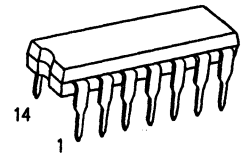
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffered outputs, which provide high noise immunity and stable output.

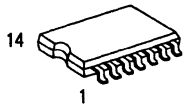
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=9ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4072B

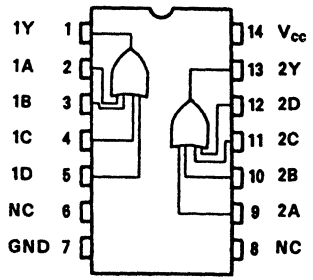


P(DIP14-P-300)



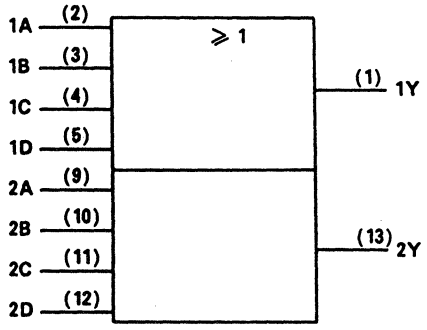
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	D	Y
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H
L	L	L	L	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	9	16	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	36	100	–	125	ns
			4.5	–	12	20	–	25	
			6.0	–	10	17	–	21	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	22	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

TRIPLE 3-INPUT OR GATE

The TC74HC4075A is a high speed CMOS 3-INPUT OR GATE fabricated with silicon gate C^2MOS technology.

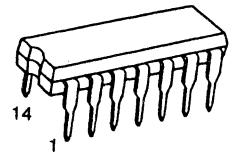
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including a buffer output, which provide high noise immunity and stable output.

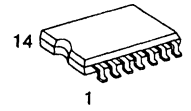
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=8ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=2μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4075B

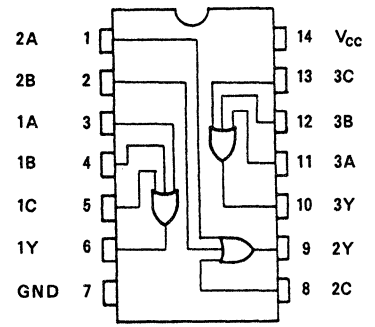


P(DIP14-P-300)

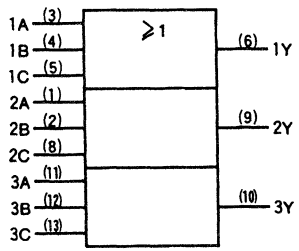


F(SOP14-P-300)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

A	B	C	Y
H	X	X	H
X	H	X	H
X	X	H	H
L	L	L	L

X : Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	2.0	−	20.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	8	15	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	35	90	–	115	
			4.5	–	11	18	–	23	
			6.0	–	9	15	–	20	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	27	–	–	–	

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/3 \text{(per Gate)}$$

TC74HC4078AP/AF

8-INPUT OR/NOR GATE

The TC74HC4078A is a high speed CMOS 8-INPUT OR/NOR GATE fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

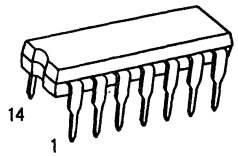
Output X is an 8-INPUT NOR, output Y is an 8-INPUT OR.

Each output has a buffer, which provide high noise immunity and stable output.

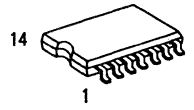
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=13ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4078B

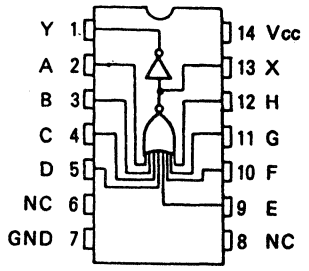


P(DIP14-P-300)



F(SOP14-P-300)

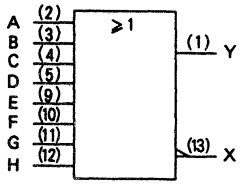
PIN ASSIGNMENT



(TOP VIEW)

NC:No Connection

IEC LOGIC SYMBOL



TRUTH TABLE

Inputs A through H	Outputs X	Outputs Y
All inputs L	H	L
All other combinations	L	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	1.0	−	10.0	

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	13	22	ns

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	–	50	130	–	165	ns
			4.5	–	16	26	–	33	
			6.0	–	14	22	–	28	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	40	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

8-BIT SHIFT AND STORE REGISTER(3-STATE)

The TC74HC4094A is a high speed 8-BIT SHIFT AND STORE REGISTER fabricated with silicon gate C^2MOS technology.

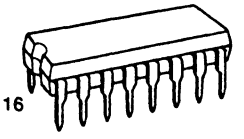
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It consists of an 8-bit shift register and an 8-bit latch with 3-state output buffers. Data is shifted serially through the shift register on the positive going transition of the CLOCK input. The output of the last stage (Qs) can be used to cascade several devices. Data on the Qs output is transferred to a second output (Q's) on the following negative transition of the CLOCK input. The data in each stage of the shift register is provided to a corresponding latch, on the negative going transition of the STROBE input. When STROBE is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is set high.

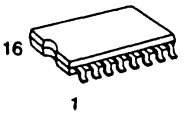
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

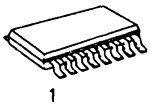
FEATURES:

- High Speed ····· f_{MAX}=73MHz(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 4094B



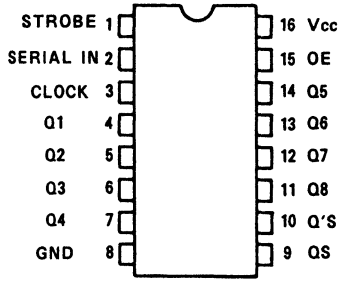
P(DIP16-P-300A)





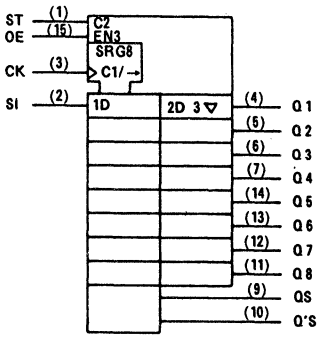
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

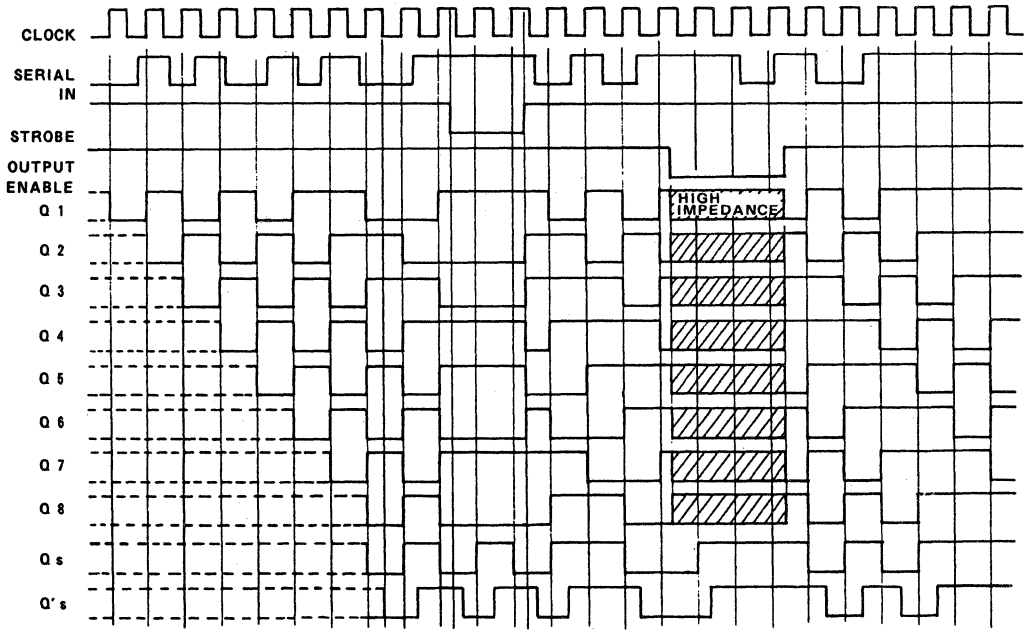


TRUTH TABLE

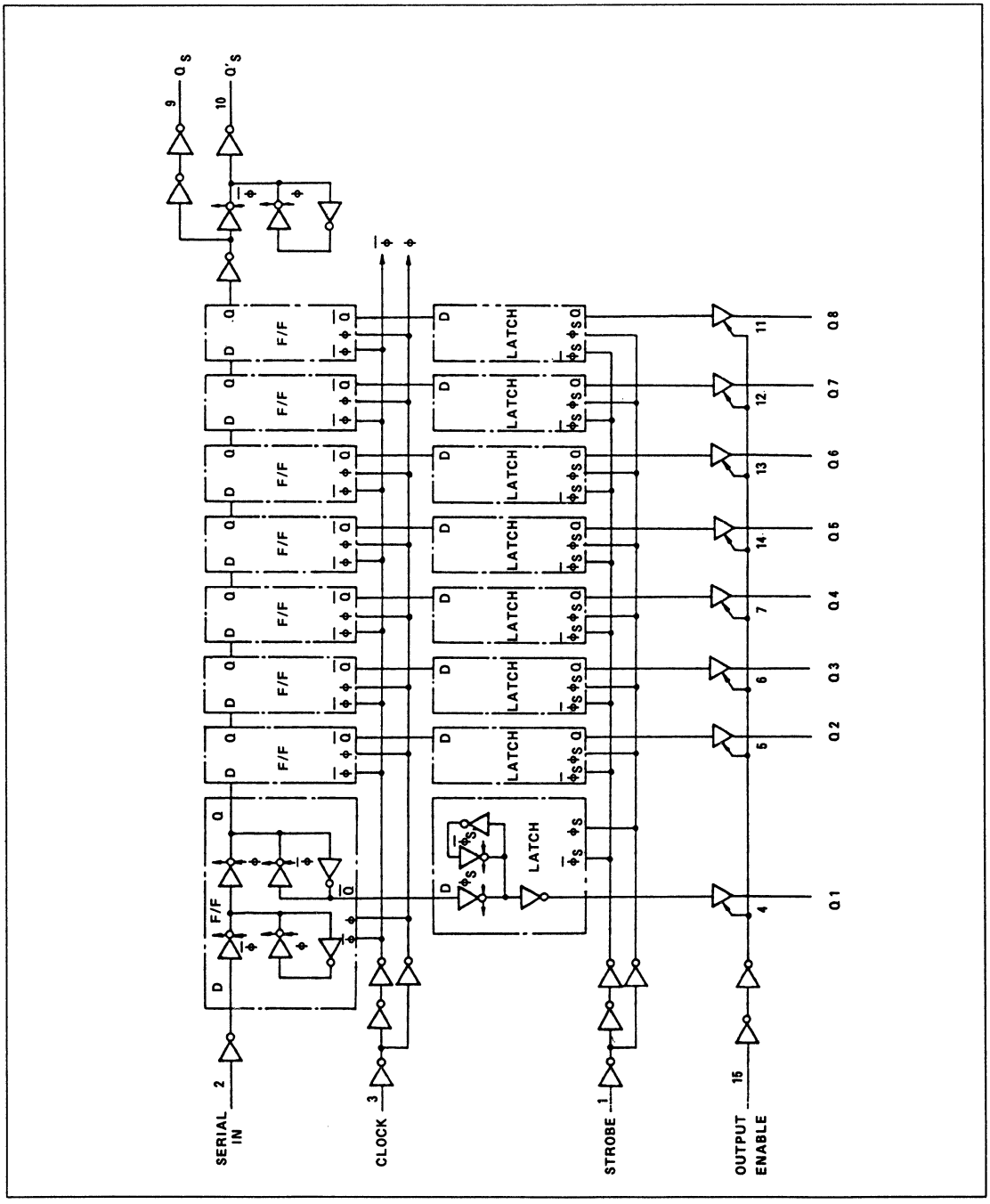
CK	OE	ST	SI	PARA.OUT		SERI.OUT	
				Q1	Qn	Qs	Q's
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	*	NC	NC	Q7	NC
↑	L	*	*	Z	Z	Q7	NC
↓	H	*	*	NC	NC	NC	Qs
↓	L	*	*	Z	Z	NC	Qs

X : DON'T CARE
NC : NO CHANGE
Z : HIGH IMPEDANCE

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		−	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CLOCK)	t_{WH} t_{WL}		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (STROBE)	t_{WH}		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (SERIAL)	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (STROBE)	t_s		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Hold Time (SERIAL)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (STROBE)	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Clock Frequency	f		2.0	−	6	5	MHz
			4.5	−	30	24	
			6.0	−	35	28	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC} =5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Prcpagation Delay Time (CLOCK–Qn)	t_{pLH} t_{pHL}		–	22	35	
Propagation Delay Time (CLOCK–QS,Q'S)	t_{pLH} t_{pHL}		–	16	25	
Propagation Delay Time (STROBE–Qn)	t_{pLH} t_{pHL}		–	16	27	
3–State Output Enable Time	t_{pZL} t_{pZH}	R_L =1KΩ	–	13	25	
Maximum Clock Frequency	f_{MAX}		33	73	–	MHz

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=–40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (CLOCK–Qn)	t_{pLH} t_{pHL}		2.0	–	92	200	–	250	
			4.5	–	26	40	–	50	
			6.0	–	20	34	–	43	
Propagation Delay Time (CLOCK–QS,Q'S)	t_{pLH} t_{pHL}		2.0	–	65	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	15	26	–	32	
Propagation Delay Time (CLOCK–Qn)	t_{pLH} t_{pHL}		2.0	–	75	160	–	200	
			4.5	–	20	32	–	40	
			6.0	–	16	27	–	34	
3–State Output Enable Time	t_{pZL} t_{pZH}	R_L =1KΩ	2.0	–	58	150	–	190	
			4.5	–	16	30	–	38	
			6.0	–	13	26	–	32	
3–State Output Disable Time	t_{pLZ} t_{pHZ}	R_L =1KΩ	2.0	–	35	150	–	190	
			4.5	–	16	30	–	38	
			6.0	–	13	26	–	32	
Maximum Clock Frequency	f_{MAX}		2.0	6	16	–	5	–	MHz
			4.5	30	66	–	24	–	
			6.0	35	80	–	28	–	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Bus Input Capacitance	C_{OUT}			–	10	–	–	–	
Power Dissipation Capacitance	C_{PD}(1)			–	140	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

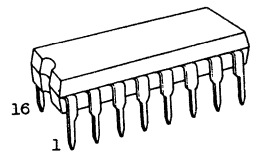
TC74HC40102P
TC74HC40103P

TC74HC40102P DUAL BCD PROGRAMMABLE DOWN COUNTER
TC74HC40103P 8-BIT BINARY PROGRAMMABLE DOWN COUNTER

The TC74HC40102 and TC74HC40103 are high speed CMOS PROGRAMMABLE DOWN COUNTER fabricated with silicon gate C^2MOS technology.
They operate ten times as fast as that of metal-gate C^2MOS IC (40102/40103B) with the same power dissipation. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero. As the TC74HC40102 adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The 74HC40103 with 8-bits binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{CLR}$ control input setting counter to maximum counting mode.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 40102B, 40103B



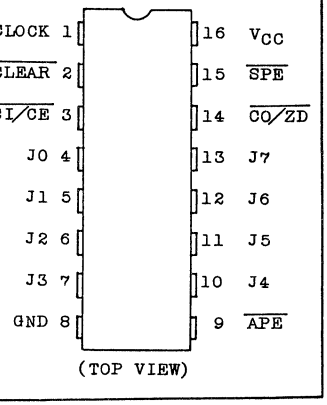
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

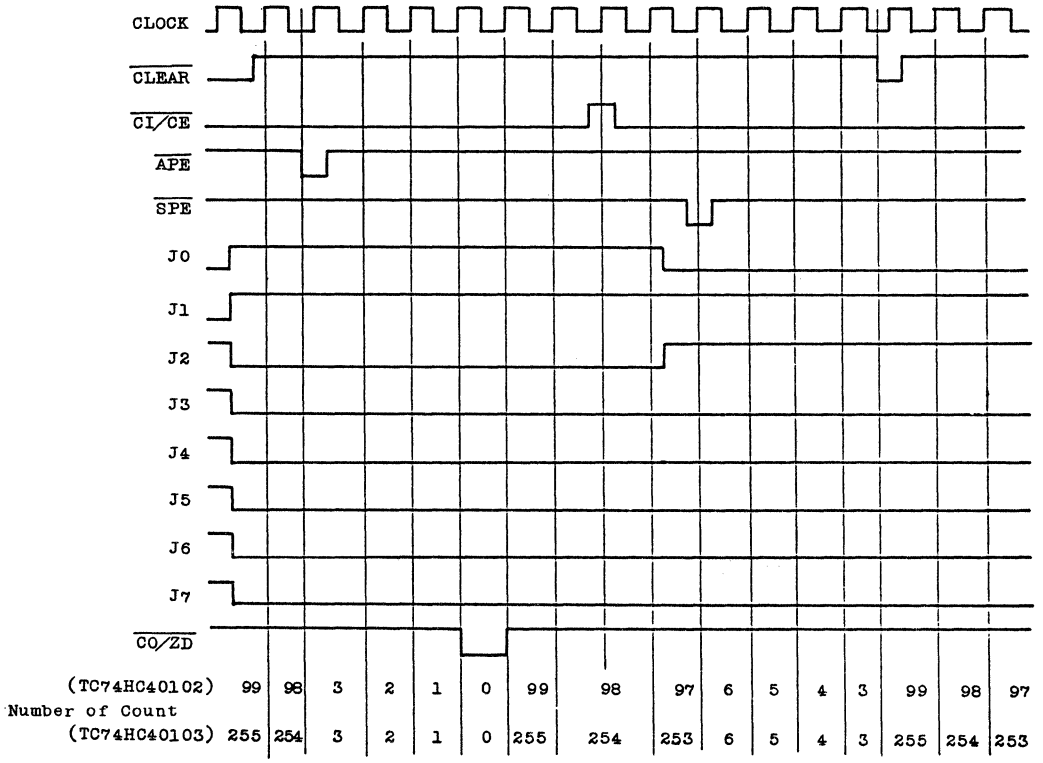
TRUTH TABLE

CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	X	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	X	X	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	X	X	X	Clear	Counter is set to maximum count.

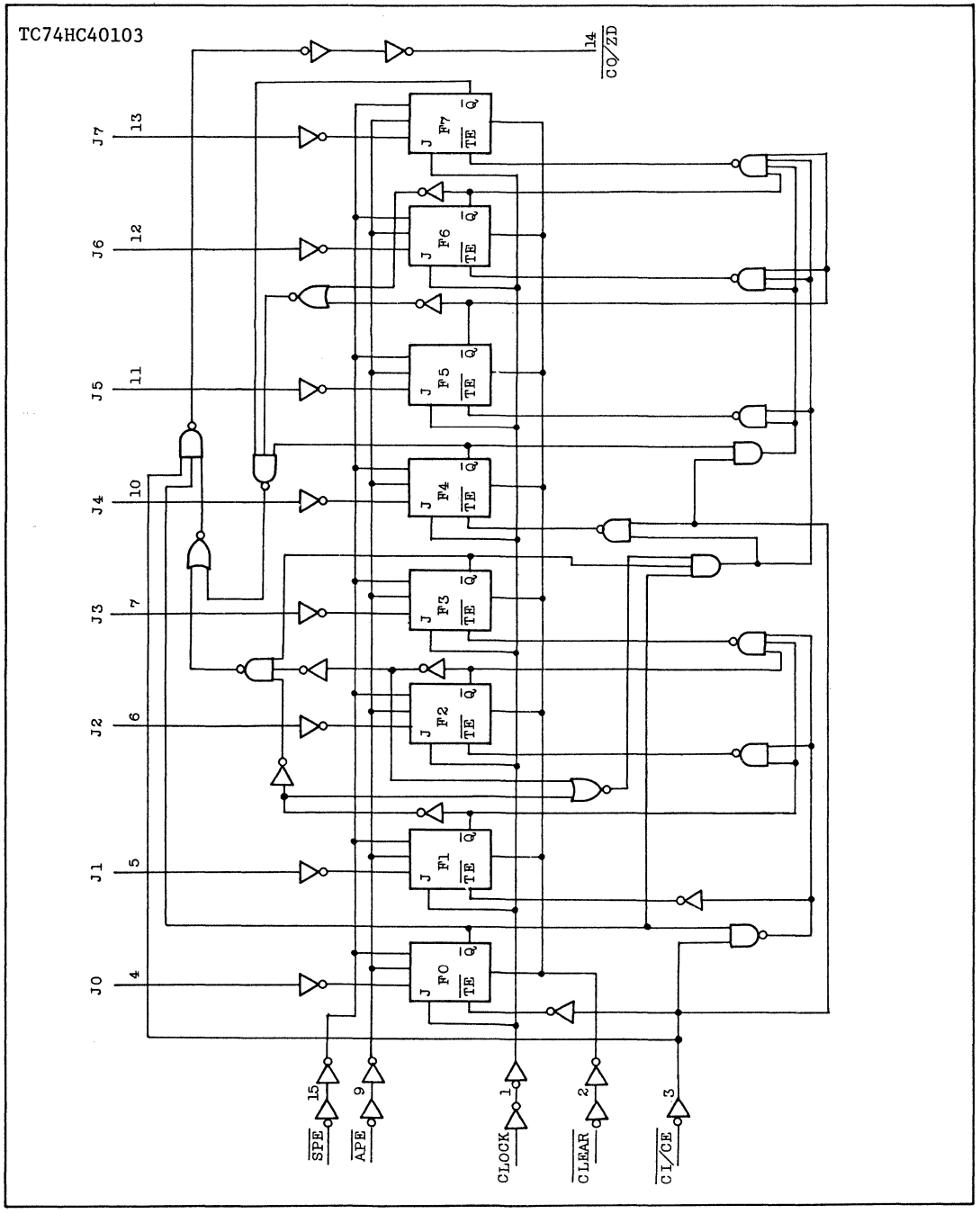
Note 1. X: Don't care

2. Maximum count: "99" for TC74HC40102 and "255" for TC74HC40103.

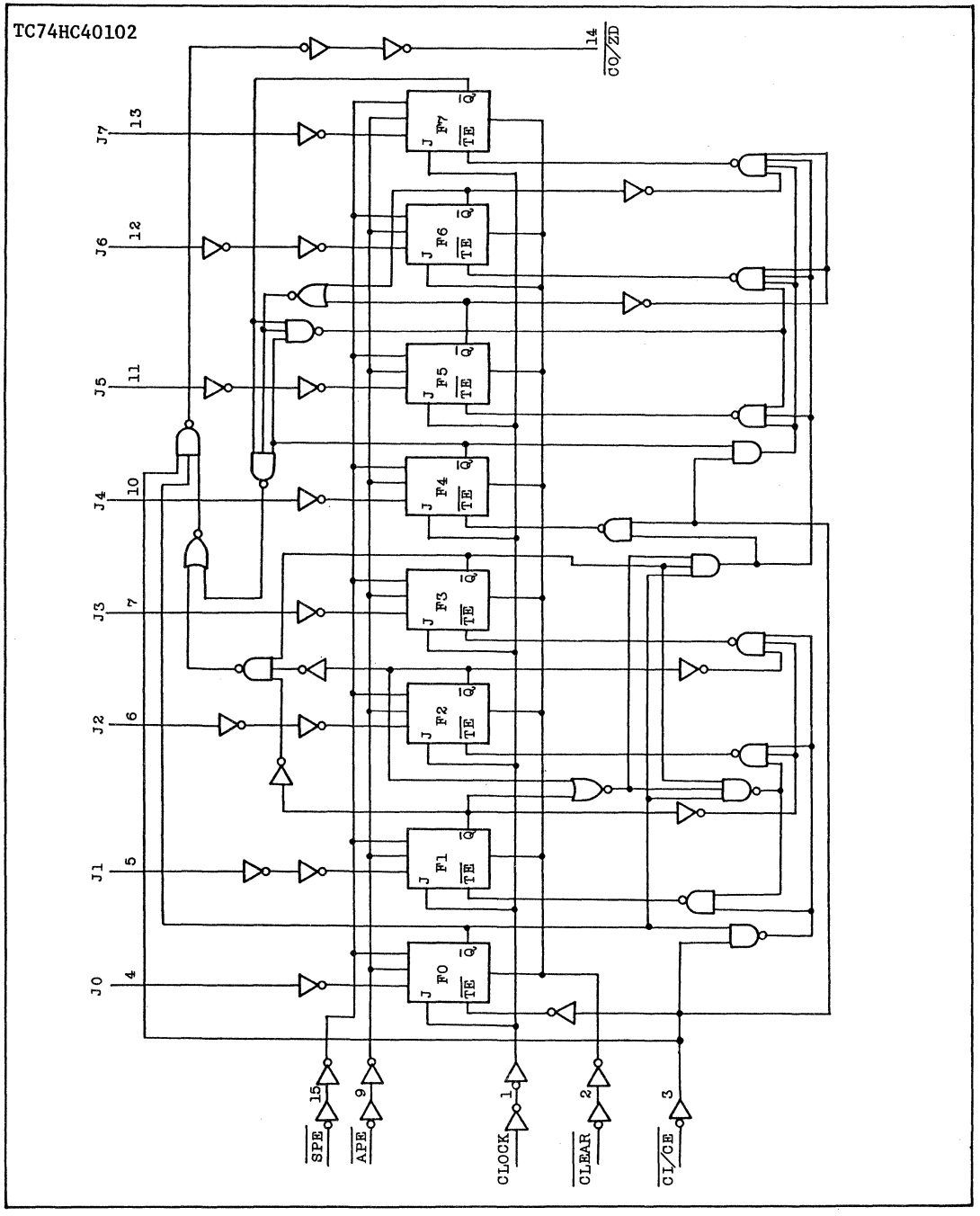
TIMING CHART

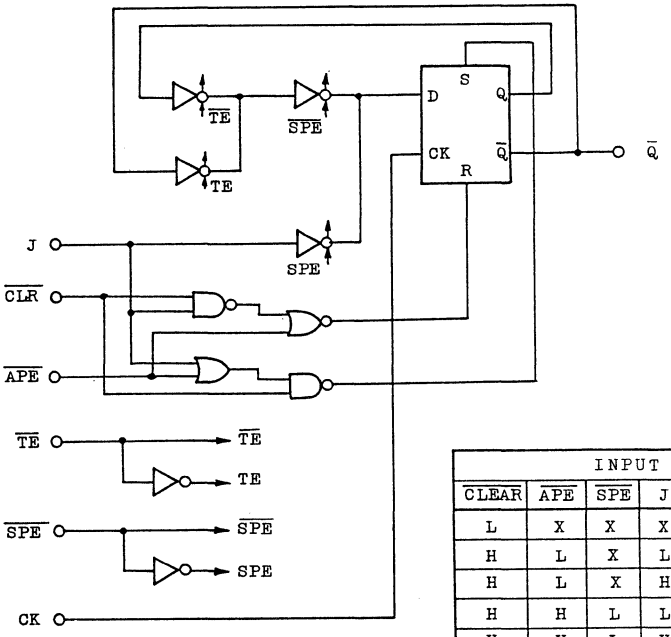


LOGIC DIAGRAM



LOGIC DIAGRAM





INPUT						OUTPUT
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	J	$\overline{TE}$	CLOCK	$\overline{Q_n}+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↓	L
H	H	L	H	X	↓	H
H	H	L	X	X	↑	$\overline{Q_n}$
H	H	H	X	L	↓	Q_n
H	H	H	X	H	X	$\overline{Q_n}$

FUNCTIONAL DESCRIPTION

The TC74HC40102 and TC74HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103 adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level.

(Continued)

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102 and 255 for the TC74HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102 and TC74HC40103, respectively, when clock input alone is given without various kinds of preset operations.

PRESET OPERATION AND RESET OPERATION

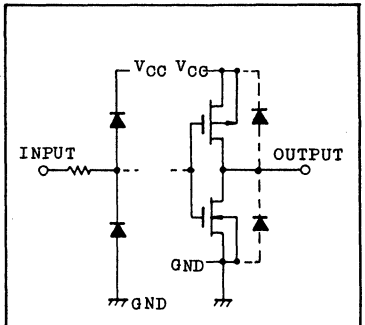
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	128	245	-	305	
	t_{pHL}		4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	156	300	-	375	
	t_{pHL}		4.5	-	39	60	-	75	
			6.0	-	33	51	-	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

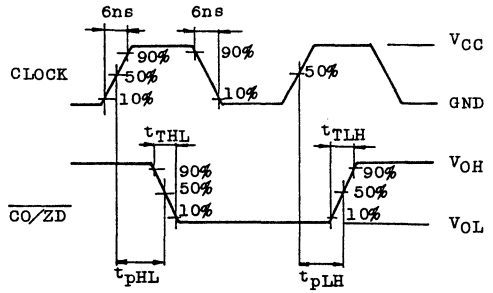
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CLEAR}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	124	240	-	300	ns
			4.5	-	31	48	-	60	
			6.0	-	27	41	-	51	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	31	-	16	-	
			6.0	24	36	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$, $\overline{APE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$, $\overline{APE}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set up Time ($\overline{SPE}$ - CK)	t_s		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Set up Time ($\overline{CI/CE}$ - CK)	t_s		2.0	-	56	125	-	160	
			4.5	-	14	25	-	32	
			6.0	-	12	21	-	27	
Minimum Set up Time (Jn - CK)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set up Time (Jn - $\overline{APE}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (All Inputs)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	74HC40102		-	110	-	-	-	
		74HC40103		-	128	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

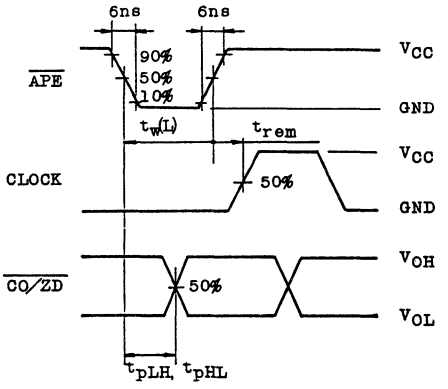
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

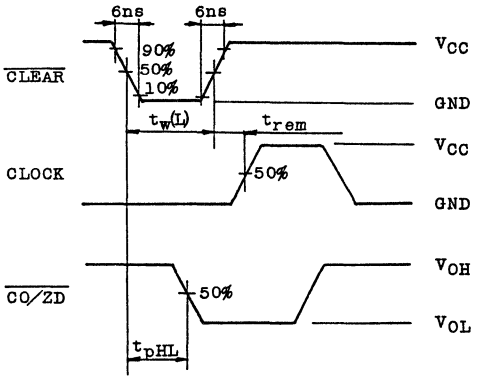
WAVEFORM 1



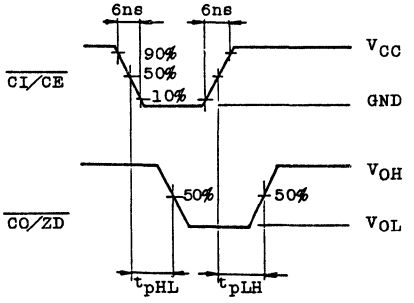
WAVEFORM 2



WAVEFORM 3

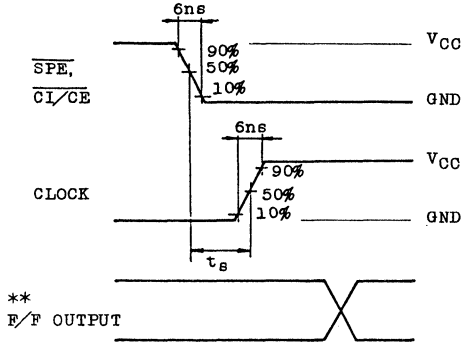


WAVEFORM 4

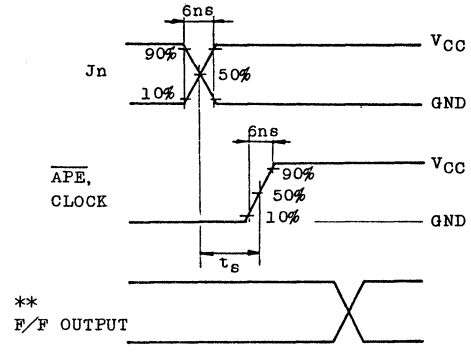


SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

WAVEFORM 5

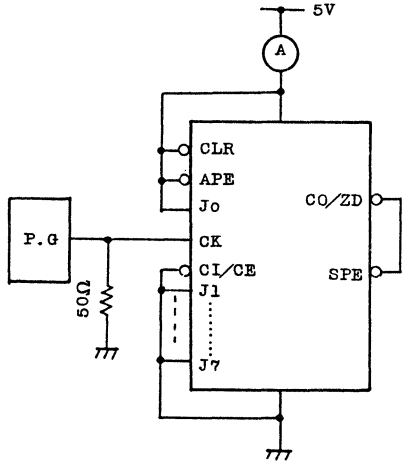


WAVEFORM 6



(** F/F output is internal signal of IC)

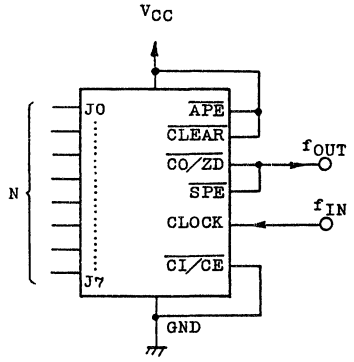
I_{CC}(Opr.) TEST CIRCUIT



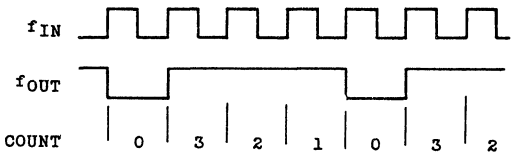
Input transition time is the same as that in case of switching characteristics test.

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

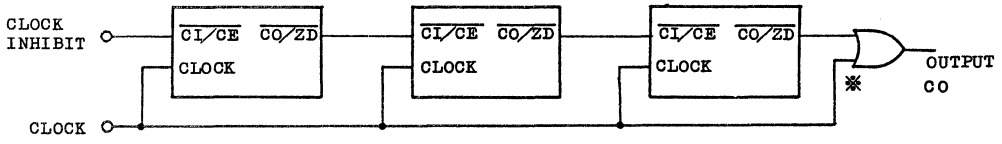


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (J0, J1=V_{CC}, J2 ∿ J7=GND)



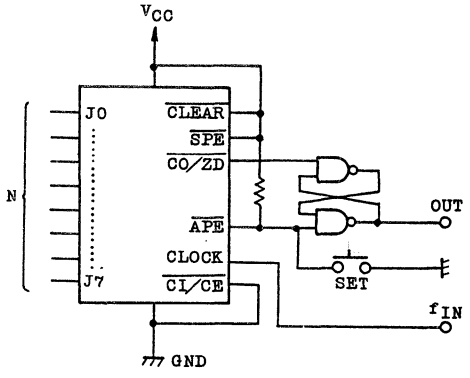
- TC74HC40102P .... 1/2 to 1/100 are dividable.
- TC74HC40103P .... 1/2 to 1/256 are dividable.

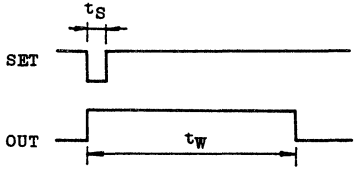
PARALLEL CARRY CASCADING



※ At synchronous cascade connection, huzzerd occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC74HC32 or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ∿ the above formula.

TC74HC40105AP/AF

TENTATIVE

FIFO 4 Bit × 16 Word REGISTER

The TC74HC40105A is a high speed CMOS 4bit x 16 word first-in, first-out (FIFO) Storage register fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation while maintaining the CMOS low power dissipation.

The device is capable of handling 16 four-bit words and it is possible to handle the input and output data at different shifting rates.

When the DATA-IN-READY (DIR) is high, data is written into the registers by a low to high transition of the SHIFT IN (SI) input. And when DATA-OUT-READY (DOR) is high, data is read out of the registers by a high to low transition of the $\overline{\text{SHIFT OUT}}$ ($\overline{\text{SO}}$) input.

If the MASTER RESET (MR) is high, the DIR goes high and DOR goes low. The data in the internal registers are not changed but are declared invalid.

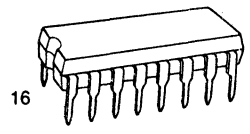
The TC74HC40105A can be cascaded to form longer registers or wider words.

The DATA OUTPUTs (Qn) are 3-State Outputs. When $\overline{\text{OUTPUT ENABLE}}$ ($\overline{\text{OE}}$) is held high, the Qn's are in high impedance state.

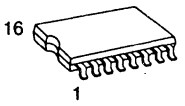
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· f_{MAX}=25MHz(typ.)at V_{CC}=5V
- Low Power Dissipation ····· 4 μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Load
  - 10(For DIR, DOR)
  - 15(For $Q_0 \sim Q_3$)
- Symmetrical Output Impedance ···
  - $|I_{OH}|=I_{OL}$=4mA(Min.)(For DIR, DOR)
  - $|I_{OH}|=I_{OL}$=6mA(Min.)(For $Q_0 \sim Q_3$)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ····· V_{CC}(opr)=2V~6V

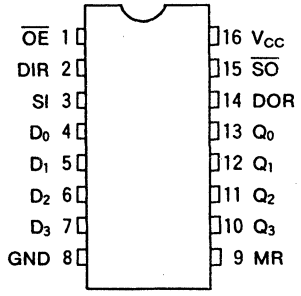


P(DIP16-P-300A)



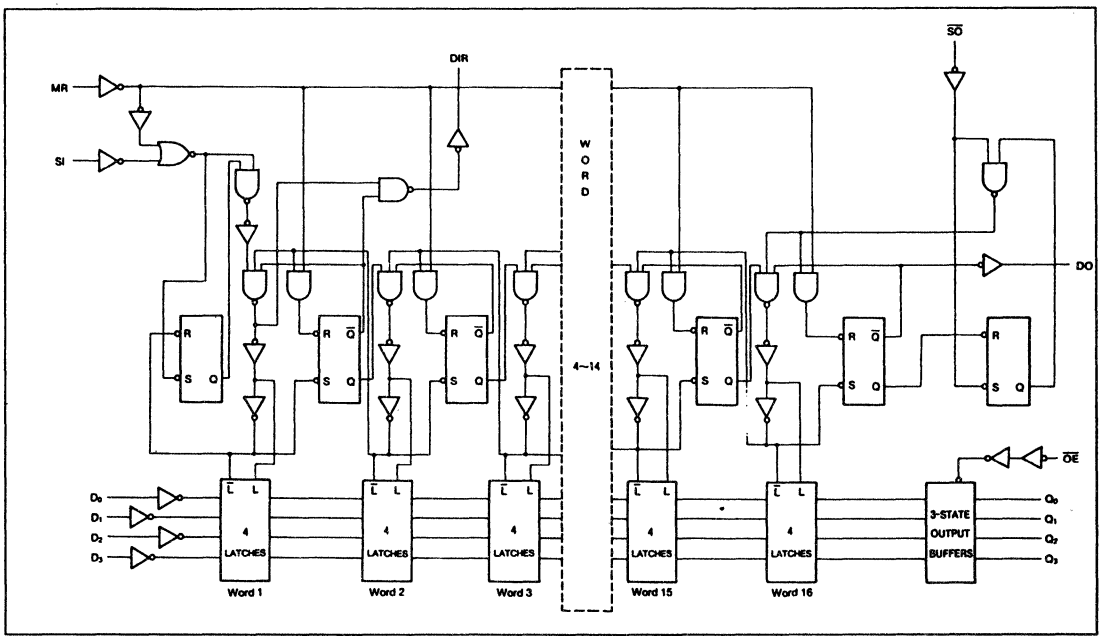
F(SOP16-P-300)

PIN ASSIGNMENT

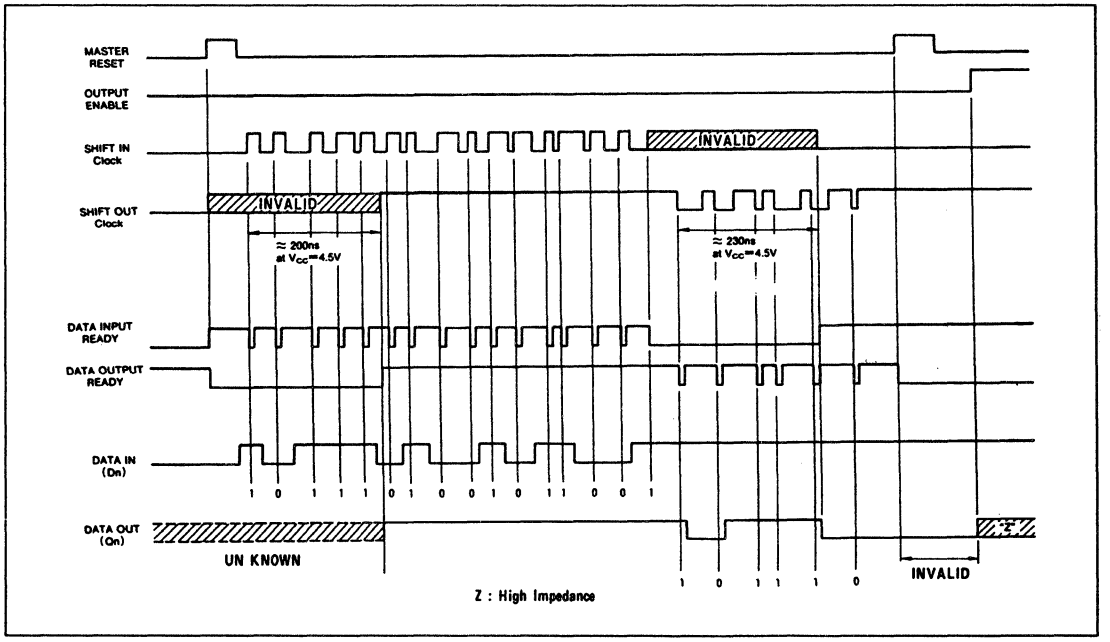


(TOP VIEW)

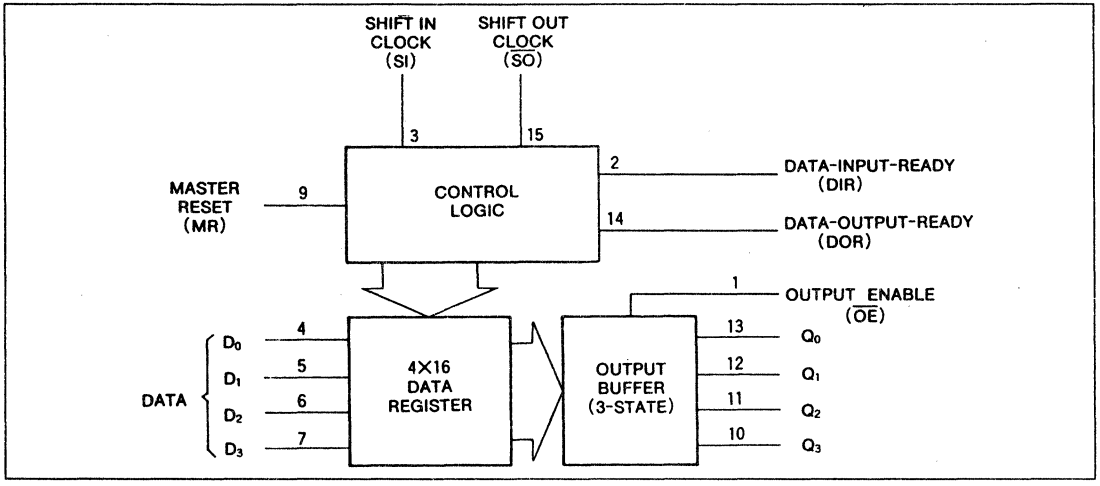
SYSTEM DIAGRAM



TIMING DIAGRAM



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

1) WRITING DATA

Data can be written into the FIFO whenever DIR is high and a low to high transition occurs on the SI pin. DIR will toggle momentarily until the data has been transferred to the second word register.

SI must be toggled before the next 4-bit word can be written. The first and subsequent words will automatically ripple to the output end of the device even if there is not a full 16 words of input data. When all 16 words are filled with data, DIR will go low and additional data cannot be written into the device.

2) READING DATA

When a data word appears in the sixteenth data register (just before the output buffer), DOR goes high and, if $\overline{OE}$ is low, data can be output on the high to low transition of $\overline{SO}$.

The data remaining in the registers now ripples to the next higher word position opening the first word position for new data. DIR goes high and additional data can be written in. During the output of data, DOR toggles momentarily after each read. When the data registers become empty, DOR goes low and $\overline{SO}$ is ignored.

3) MASTER REST

When a high is input to MR, the internal control logic is initiallized. This causes DIR to go high and DOR to go low. The contents of the data registers are not changed, but are invalid and will be written over when the first word is loaded.

4) CASCADING

The TC74HC40105A can be cascaded to form longer registers simply by connecting DOR of the first device to SI of the second and DIR of the second device to $\overline{SO}$ of the first. Additional devices may be cascaded by repeating the above. Of course, the Qn outputs of the first device must be connected to the Dn inputs of the second.

In this mode, an MR pulse must be applied after the supply voltage is turned on. For words wider than 4-bits, the DIR and DOR outputs from each FIFO must be ANDed respectively and the SI and $\overline{SO}$ inputs must each be paralleled.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current (DIR, DOR) (Q_0~Q_3)	I_{OUT}	±25 ±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
		DIR, DOR	I_{OH} = −4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −5.2mA	6.0	5.68	5.80	−	5.63	−	
		Q_0~Q_3	I_{OH} = −6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} = −7.8mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
		DIR, DOR	I_{OL} = 4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 5.2mA	6.0	−	0.18	0.26	−	0.33	
		Q_0~Q_3	I_{OL} = 6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} = 7.8mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (SI)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width ($\overline{SO}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Pulse Width (MR)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (DATA−SI)	t_s		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	
Minimum Hold Time (DATA−SI)	t_h		2.0	−	100	125	
			4.5	−	20	25	
			6.0	−	17	21	
Minimum Removal Time (MR−SI)	t_{rem}		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Clock Frequency	f		2.0	−	3	24	MHz
			4.5	−	15	12	
			6.0	−	18	13	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time (DIR,DOR)	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (SO,MR−DOR)	t_{pHL}		−	22	39	
Propagation Delay Time (SO−DIR)	t_{pLH}		−	242	365	
Propagation Delay Time (SI,DOR)	t_{pLH}		−	187	300	
Propagation Delay Time (SI−DIR)	t_{pHL}		−	22	35	
Propagation Delay Time (MR−DIR)	t_{pLH} t_{pHL}		−	25	39	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time ($Q_0 \sim Q_3$)	t_{TLH} t_{THL}		50	2.0	−	21	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Output Transition Time (DIR,DOR)	t_{TLH} t_{THL}		50	2.0	−	24	75	−	95	
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (SO,MR−DOR)	t_{pHL}		50	2.0	−	84	225	−	280	
				4.5	−	28	45	−	56	
				6.0	−	24	38	−	48	
Propagation Delay Time (SO−DIR)	t_{pLH}		50	2.0	−	798	2000	−	2500	
				4.5	−	266	400	−	500	
				6.0	−	226	340	−	425	
Propagation Delay Time (SI−DOR)	t_{pLH}		50	2.0	−	624	1650	−	2060	
				4.5	−	208	330	−	412	
				6.0	−	177	280	−	350	
Propagation Delay Time (SI−DIR)	t_{pHL}		50	2.0	−	78	200	−	250	
				4.5	−	26	40	−	50	
				6.0	−	22	34	−	43	
Propagation Delay Time (SO−Qn)	t_{pLH} t_{pHL}		50	2.0	−	156	400	−	500	
				4.5	−	52	80	−	100	
				6.0	−	44	68	−	85	
			150	2.0	−	171	440	−	550	
				4.5	−	57	88	−	110	
				6.0	−	48	75	−	94	
Propagation Delay Time (SI−Qn)	t_{pLH} t_{pHL}		50	2.0	−	612	1500	−	1875	
				4.5	−	204	300	−	375	
				6.0	−	173	255	−	319	
			150	2.0	−	627	1540	−	1925	
				4.5	−	209	308	−	385	
				6.0	−	178	262	−	327	
Propagation Delay Time (MR−DIR)	t_{pLH} t_{pHL}		50	2.0	−	87	225	−	280	
				4.5	−	29	45	−	56	
				6.0	−	25	38	−	48	
Output Enable time	t_{pZL} t_{pZH}	$R_L = 1\,k\Omega$	50	2.0	−	45	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	13	21	−	26	
			150	2.0	−	60	165	−	205	
				4.5	−	20	33	−	41	
				6.0	−	17	28	−	35	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L = 1\,k\Omega$	50	2.0	−	32	125	−	155	
				4.5	−	16	25	−	31	
				6.0	−	14	21	−	26	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)(Cont'd)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		50	2.0	3	7	−	2.4	−	MHz
				4.5	15	22	−	12	−	
				6.0	18	26	−	14	−	
			150	2.0	2.6	6	−	2	−	
				4.5	13	20	−	10	−	
				6.0	15	24	−	12	−	
Output Pulse Width (DIR)	$t_{W(H)}$ $t_{W(L)}$		50	2.0	−	95	−	−	−	ns
				4.5	−	25	−	−	−	
				6.0	−	21	−	−	−	
Output Pulse Width (DOR)	$t_{W(H)}$ $t_{W(L)}$		50	2.0	−	95	−	−	−	
				4.5	−	25	−	−	−	
				6.0	−	21	−	−	−	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}	(注 1)			−	300	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

The TC74HC4511A is high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The segment output driver, which is of CMOS construction, has a large I_{OH} capability which permits the device to drive cathode common LED directly.

When lamp test (LT) is held low, all segment outputs will go high, and when the blanking input (BI) is held low and LT is held high, all segment outputs will go low. These functions are independent of other inputs and used to test the display.

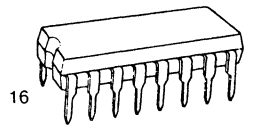
BI is used to pulse-modulate the brightness of the display.

When error code (over 10) is applied to BCD inputs, all segment outputs will go to low (turn off).

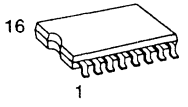
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=23ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|$=20mA
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with TC4511B

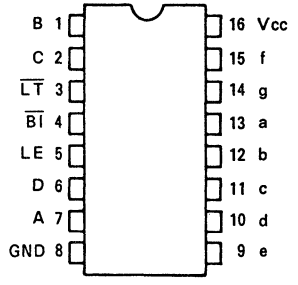


P(DIP16-P-300A)



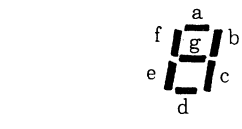
F(SOP16-P-300)

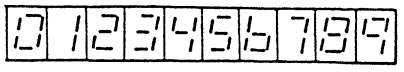
PIN ASSIGNMENT



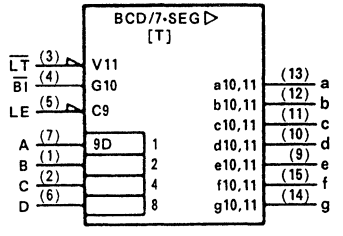
(TOP VIEW)

DISPLAY MODE



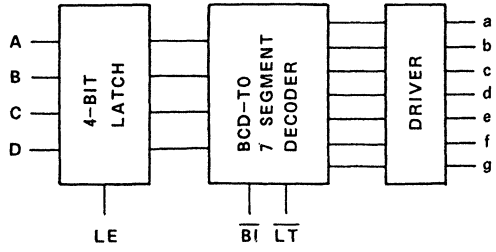


IEC LOGIC SYMBOL



[T]:

BLOCK DIAGRAM

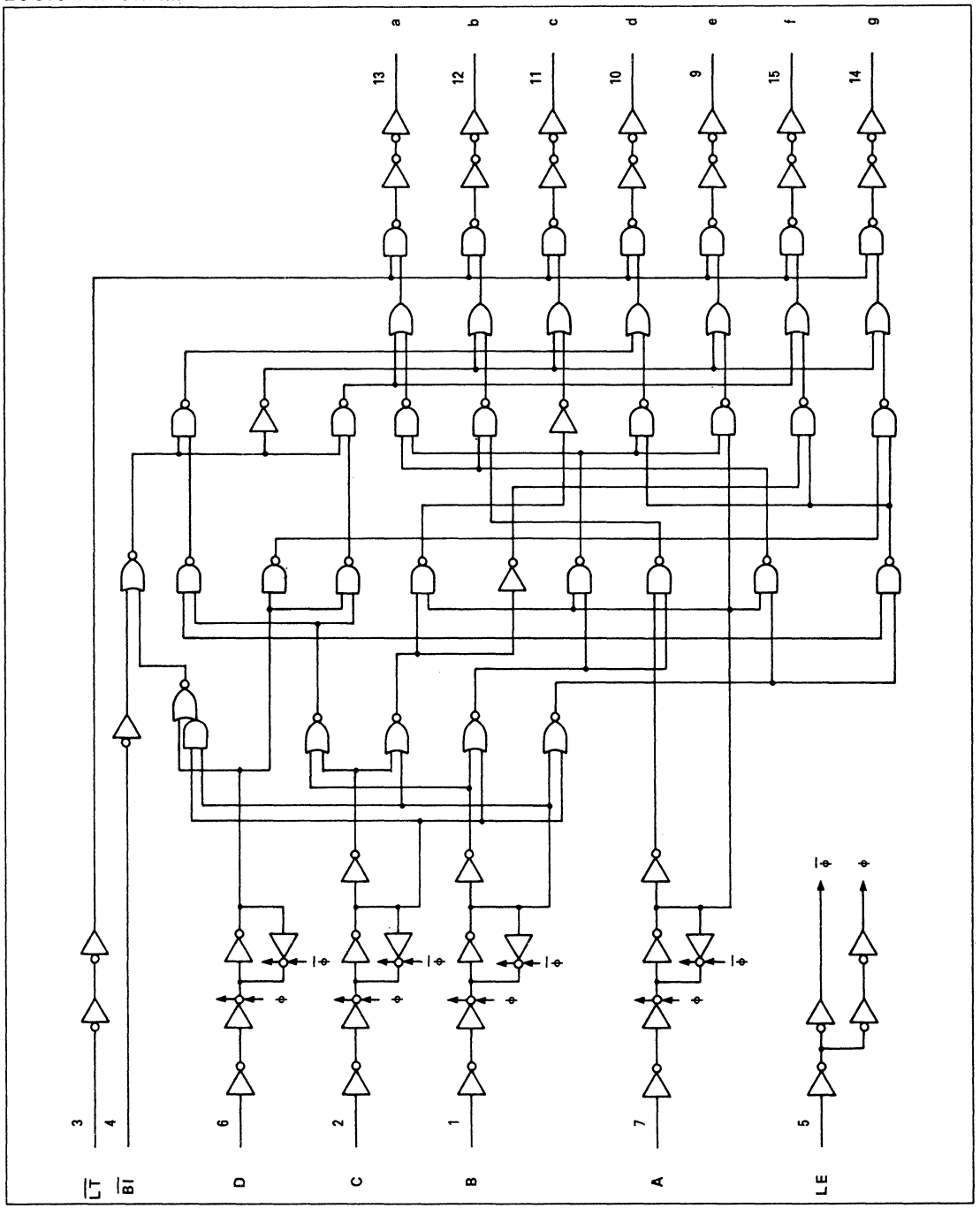


TRUTH TABLE

INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
※	※	L	※	※	※	※	H	H	H	H	H	H	H	8
※	L	H	※	※	※	※	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	※	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	※	※	L	L	L	L	L	L	L	BLANK
H	H	H	※	※	※	※	Hold the stage at the leading edege of LE							

※ Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25(Sinc)/−35(Source)	mA
DC V_{CC}/Ground Current	I_{CC}	+150(I_{CC})/−50(I_{GND})	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−20 mA	4.5	3.20	3.80	−	2.90	−	
			I_{OH} =−7.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (LE)	$t_{W(L)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH}		−	4	8	ns
Output Transition Time	t_{THL}		−	4	8	
Propagation Delay Time (BCD−Segment)	t_{pLH} t_{pHL}		−	28	45	
Propagation Delay Time ($\overline{BI}$−Segment)	t_{pLH} t_{pHL}		−	18	31	
Propagation Delay Time ($\overline{LT}$−Segment)	t_{pLH} t_{pHL}		−	12	21	
Propagation Delay Time (LE−Segment)	t_{pLH} t_{pHL}		−	26	44	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r=t_f$=6ns)

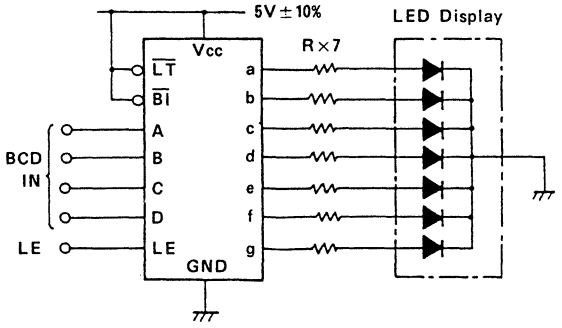
PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time Low to High	t_{TLH}		2.0	−	25	60	−	75	ns
			4.5	−	7	12	−	15	
			6.0	−	6	11	−	13	
Output Transition Time High to Low	t_{THL}		2.0	−	30	75	−	95	
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (BCD–Segment)	t_{pLH} t_{pHL}		2.0	−	125	255	−	320	
			4.5	−	33	51	−	64	
			6.0	−	23	43	−	54	
Propagation Delay Time ($\overline{BI}$–Segment)	t_{pLH} t_{pHL}		2.0	−	70	175	−	220	
			4.5	−	22	35	−	44	
			6.0	−	17	30	−	37	
Propagation Delay Time ($\overline{LT}$–Segment)	t_{pLH} t_{pHL}		2.0	−	60	120	−	150	
			4.5	−	15	24	−	30	
			6.0	−	12	20	−	26	
Propagation Delay Time (LE–Segment)	t_{pLH} t_{pHL}		2.0	−	95	240	−	300	
			4.5	−	32	48	−	60	
			6.0	−	23	41	−	51	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)	Note (1)		−	95	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

APPLICATION CIRCUIT

Static Display Circuit



Recommended Resistance R

DISPLAY	COLOR	LETTER HIGHT	R
TLR358T	Red	13.4mm	390Ω
TLR362T	〃	14.2	〃
TLR332T	〃	7.6	〃
TLR342T	〃	10.9	〃
TLG358T	Green	13.4mm	160Ω
TLG362T	〃	14.2	〃
TLG332T	〃	7.6	〃
TLG342T	〃	10.9	〃

TC74HC4514AP
TC74HC4515AP

TC74HC4514AP 4-TO-16 LINE DECODER/LATCH
TC74HC4515AP 4-TO-16 LINE DECODER/LATCH(INV.)

The TC74HC4514A/TC74HC4515A are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

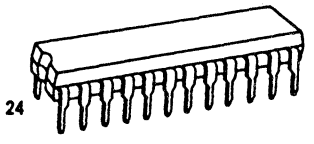
The selected output is enabled by a low on the inhibit input (INHIBIT). A binary code stored in the four input latches (A thru D) is decided and provides a high level (HC4514A) or a low level (HC4515A) at the corresponding one of sixteen outputs. When the INHIBIT is held low, all outputs are kept low (HC4514A) or high (HC4515A), however, the latch function is available.

The data applied to the data inputs are transferred to the outputs of latches when the strobe input is held high. When the strobe input is taken low, the data is retained at the output of the latches.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

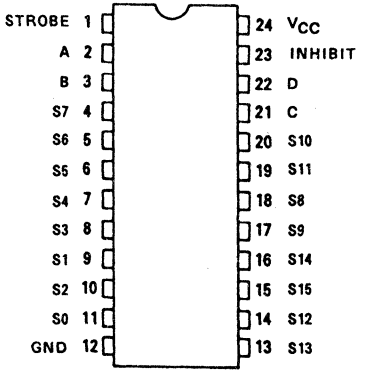
FEATURES:

- High Speed ····· t_{pd} =18ns(typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 4514B/4515B



P(DIP24-P-300)

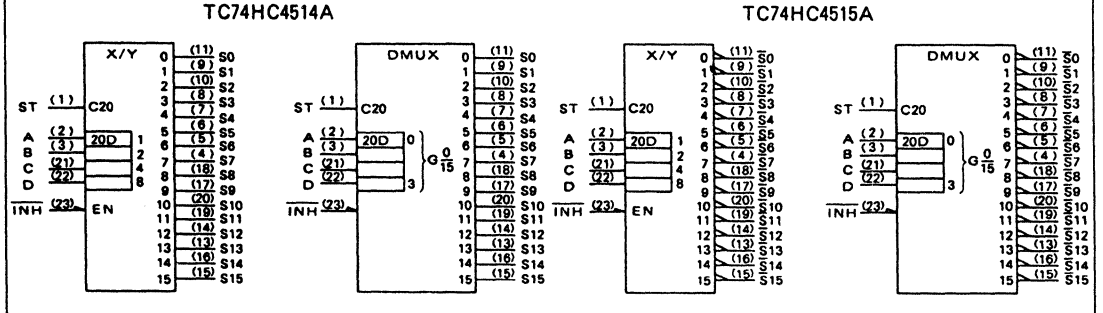
PIN ASSIGNMENT



(TOP VIEW)

NOTE: In case of TC74HC4515A $\overline{S0}$~$\overline{S15}$

IEC LOGIC SYMBOL



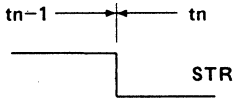
TRUTH TABLE

INPUTS					SELECTED OUTPUTS	
INHIBIT	A	B	C	D	TC74HC4514A-"H"	TC74HC4515A-"L"
L	L	L	L	L	S_0	$\overline{S_0}$
L	H	L	L	L	S_1	$\overline{S_1}$
L	L	H	L	L	S_2	$\overline{S_2}$
L	H	H	L	L	S_3	$\overline{S_3}$
L	L	L	H	L	S_4	$\overline{S_4}$
L	H	L	H	L	S_5	$\overline{S_5}$
L	L	H	H	L	S_6	$\overline{S_6}$
L	H	H	H	L	S_7	$\overline{S_7}$
L	L	L	L	H	S_8	$\overline{S_8}$
L	H	L	L	H	S_9	$\overline{S_9}$
L	L	H	L	H	S_{10}	$\overline{S_{10}}$
L	H	H	L	H	S_{11}	$\overline{S_{11}}$
L	L	L	H	H	S_{12}	$\overline{S_{12}}$
L	H	L	H	H	S_{13}	$\overline{S_{13}}$
L	L	H	H	H	S_{14}	$\overline{S_{14}}$
L	H	H	H	H	S_{15}	$\overline{S_{15}}$
H	X	X	X	X	ALL OUTPUT"L"	ALL OUTPUT"H"

○ X : Don't Care

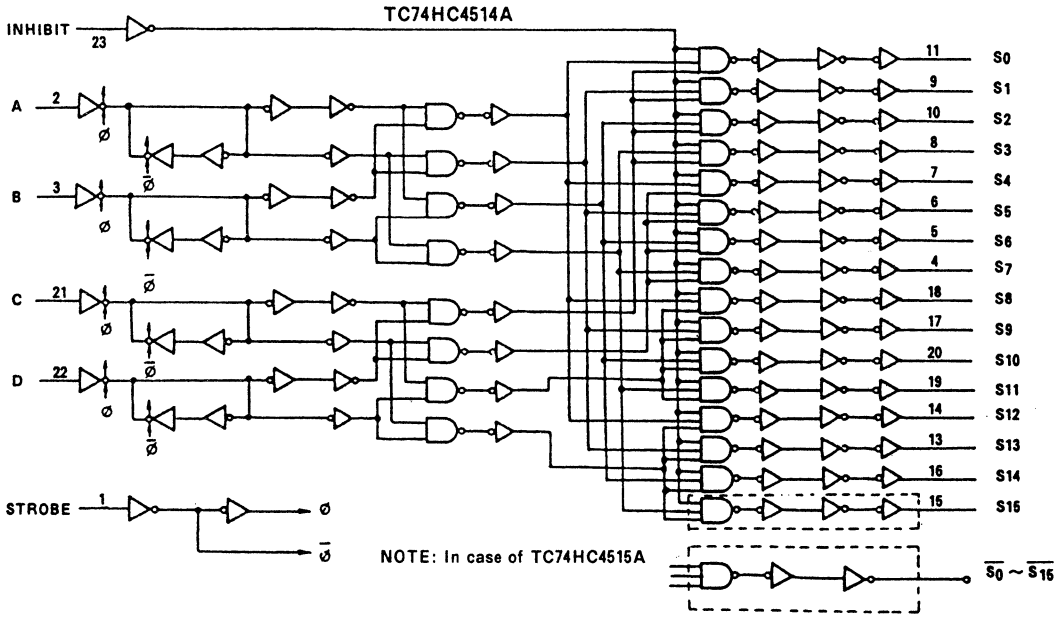
○ STROBE="H"; REFER TO TRUTH TABLE

○ STROBE="H"



Data at the negative going transition of strobe shall be provided on each output while strobe is held low.

SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ～85℃ MIN.	Ta=−40 ～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃		Ta=−40 ~85℃	UNIT
			V_{CC}	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (STROBE)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set−up Time (DATA)	t_s		2.0	−	50	65	
			4.5	−	10	13	
			6.0	−	9	11	
Minimum Hold Time (DATA)	t_h		2.0	−	5	5	
			4.5	−	5	5	
			6.0	−	5	5	

AC ELECTRICAL CHARACTERISTICS($C_L=15pF, V_{CC}=5V, Ta=25℃$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (DATA−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (STROBE−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	20	30	
Propagation Delay Time (INHIBIT−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		−	16	30	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	30	75	−	95	ns
				4.5	−	8	15	−	19	
				6.0	−	7	13	−	16	
Propagation Delay Time (DATA−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	65	175	−	220	
				4.5	−	22	35	−	44	
				6.0	−	19	30	−	37	
Propagation Delay Time (STROBE−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	75	175	−	220	
				4.5	−	24	35	−	44	
				6.0	−	20	30	−	37	
Propagation Delay Time (INHIBIT−Sn, $\overline{Sn}$)	t_{pLH} t_{pHL}		50	2.0	−	60	175	−	220	
				4.5	−	20	35	−	44	
				6.0	−	17	30	−	37	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD} (1)				−	61	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

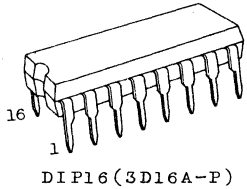
TC74HC4518P
TC74HC4520P/F

TC74HC4518P/F DUAL BCD COUNTER
TC74HC4520P/F DUAL 4-BIT BINARY COUNTER

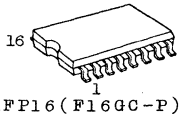
The TC74HC4518 and TC74HC4520 are high speed CMOS DUAL BCD/4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.
It operates ten times as fast as that of metal-gate C^2MOS IC (4518B/4520B) with the same power dissipation.
Since both of TC74HC4518 and TC74HC4520 contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" ($Q_0 \sim Q_3$="L") by giving "H" level signal to CLEAR input regardless of other inputs. The counting condition is changed by the positive going transition of CLOCK input if CE="H" or by the negative going transition of CE if CLOCK="L".
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4518B/4520B



DIP16(3D16A-P)



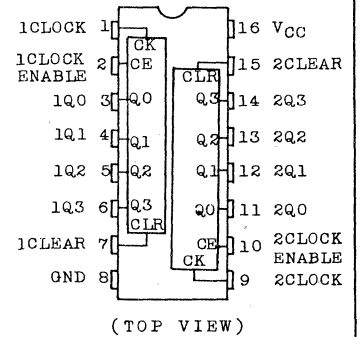
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



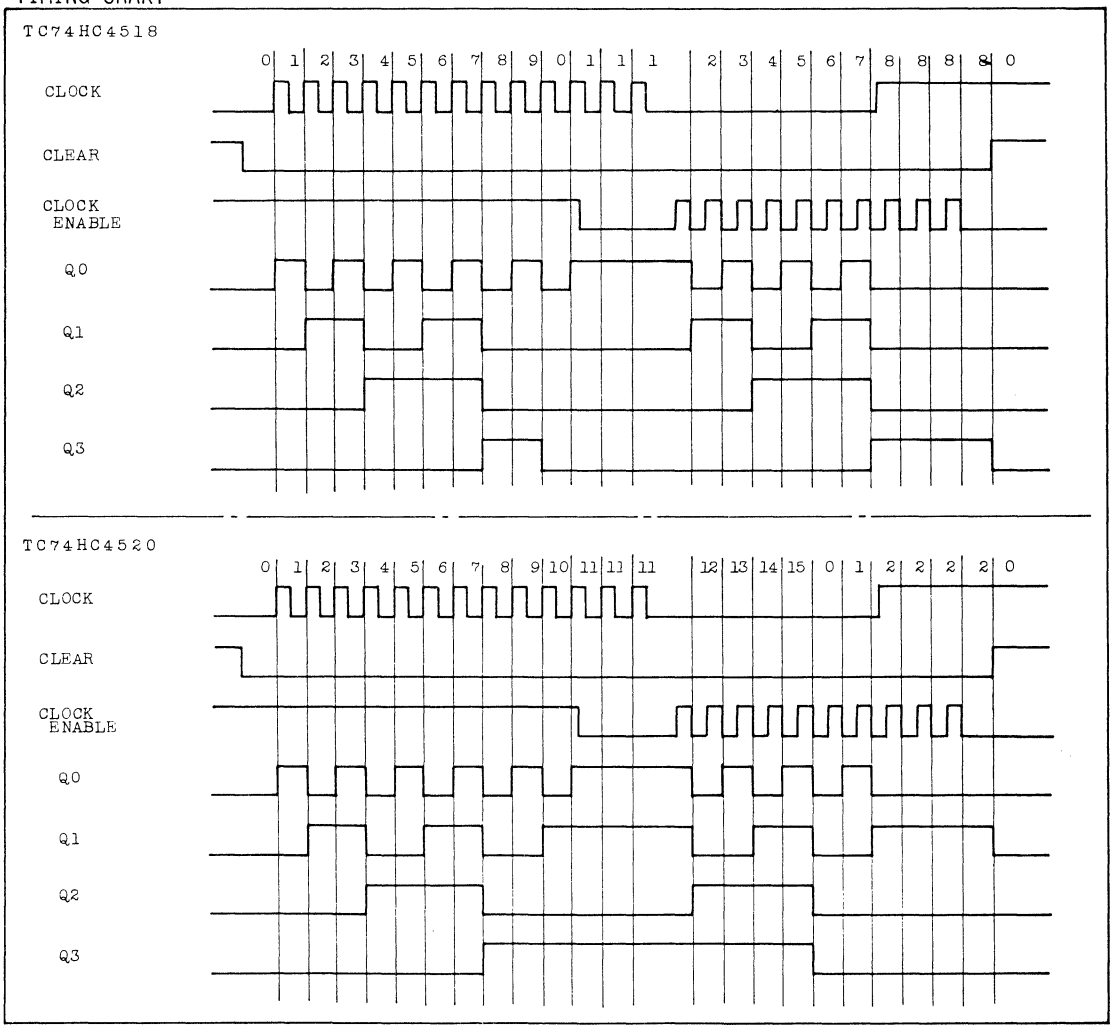
(TOP VIEW)

TRUTH TABLE

INPUTS			FUNCTION
CLOCK	CLOCK ENABLE	CLEAR	
↑	H	L	INCLEMENT COUNTER
L	↓	L	INCLEMENT COUNTER
↓	X	L	NO CHANGE
X	↑	L	NO CHANGE
↑	L	L	NO CHANGE
H	↓	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

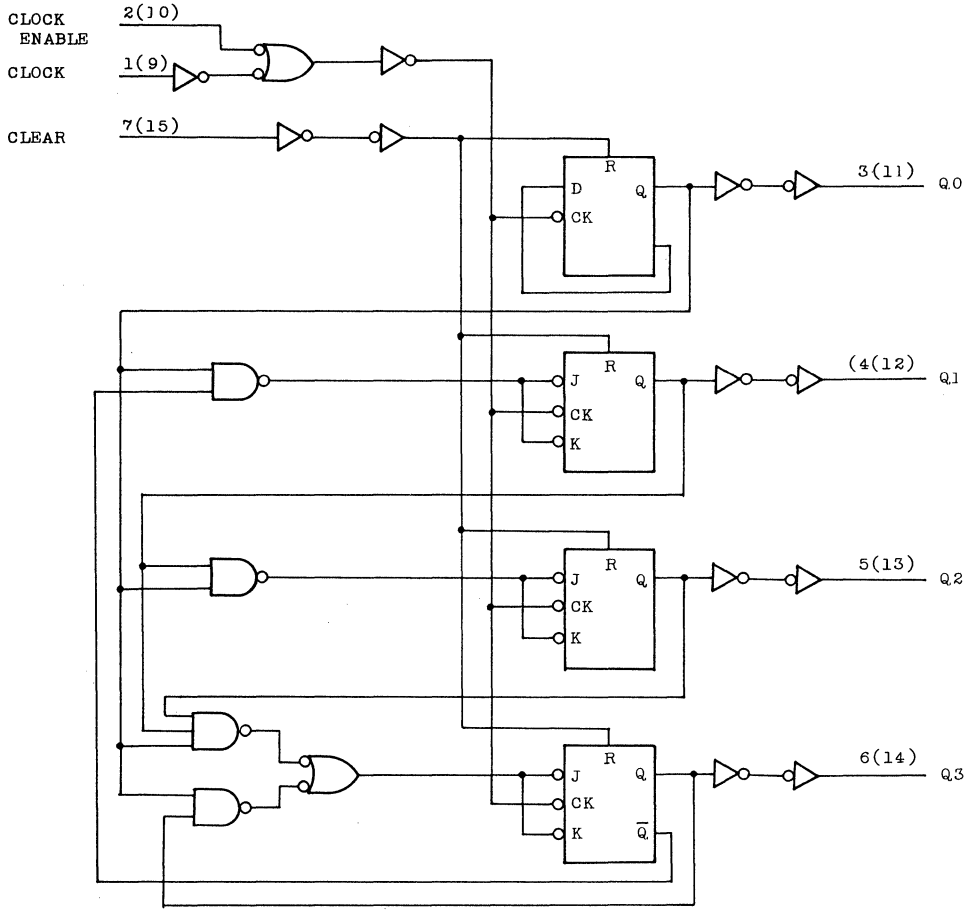
X : DON'T CARE

TIMING CHART

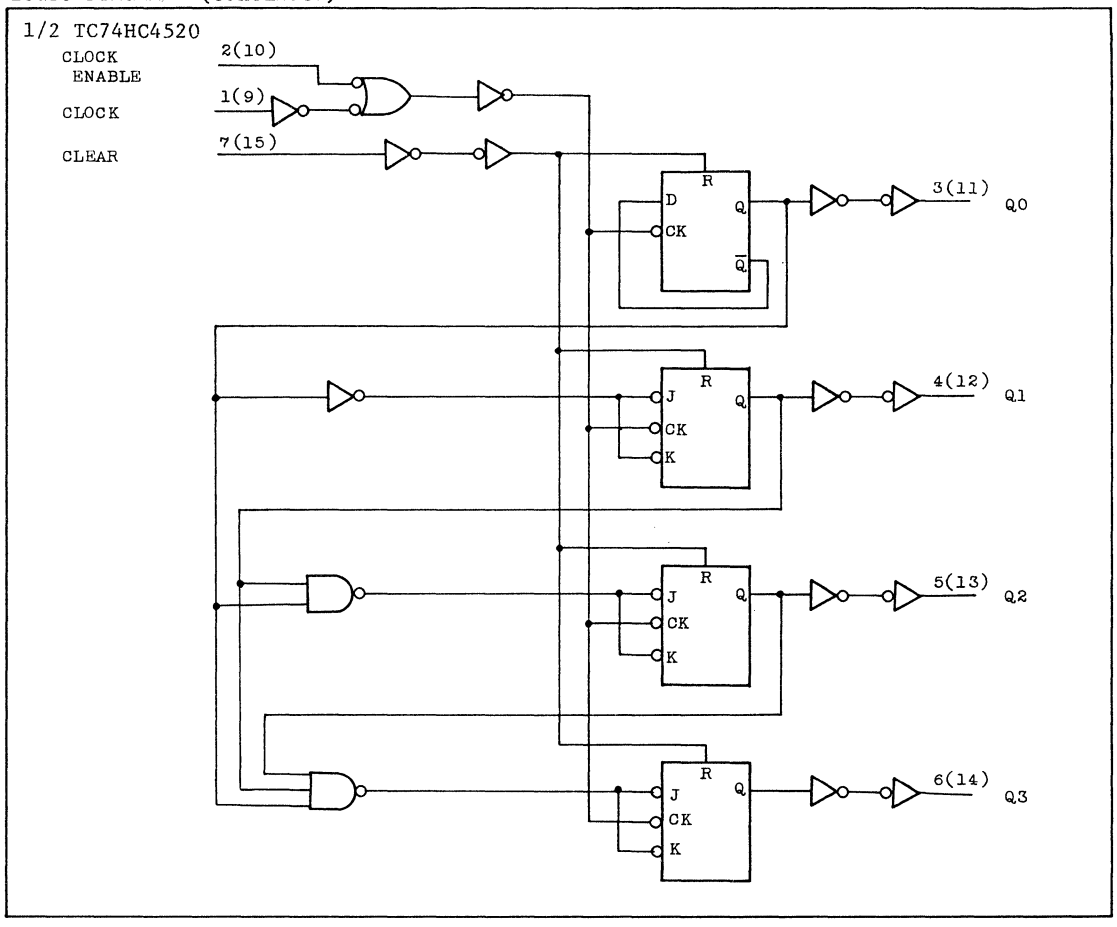


LOGIC DIAGRAM

1/2 TC74HC4518



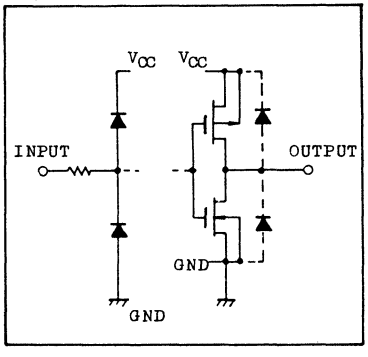
LOGIC DIAGRAM (Continued)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CK, CE - Qn)	t_{pLH}		2.0	-	100	190	-	240	
	t_{pHL}		4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time (CLR - Qn)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	25	48	-	20	-	
			6.0	29	56	-	24	-	

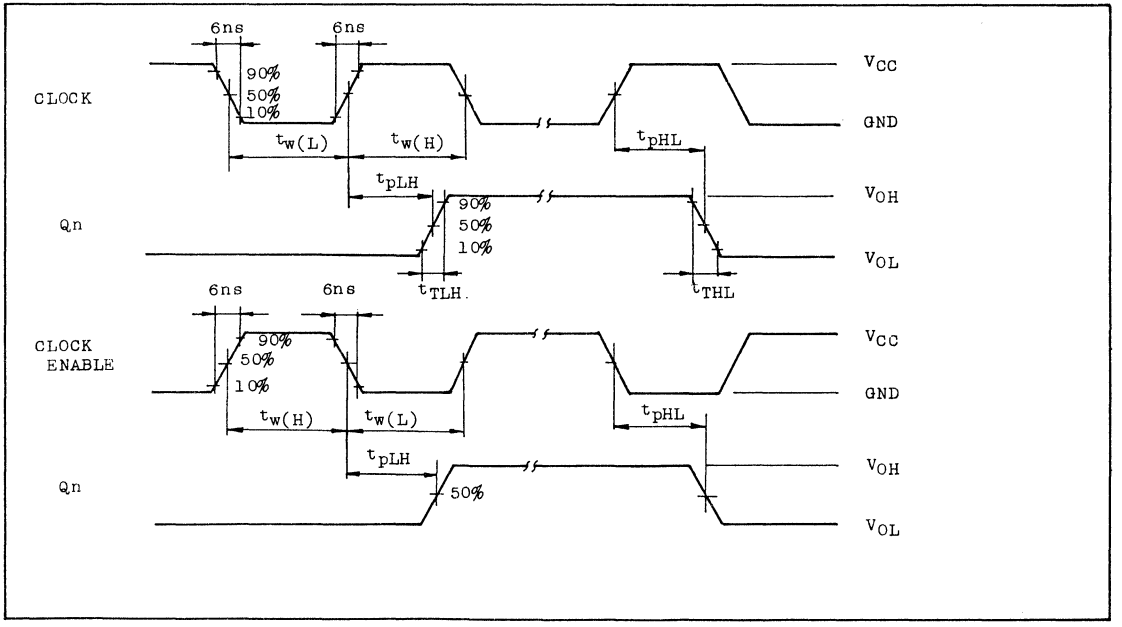
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CK, CE)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum PUlse Width (CLR)	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Removal Time (CLR)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4518		-	145	-	-	-	
		TC74HC4520		-	145	-	-	-	

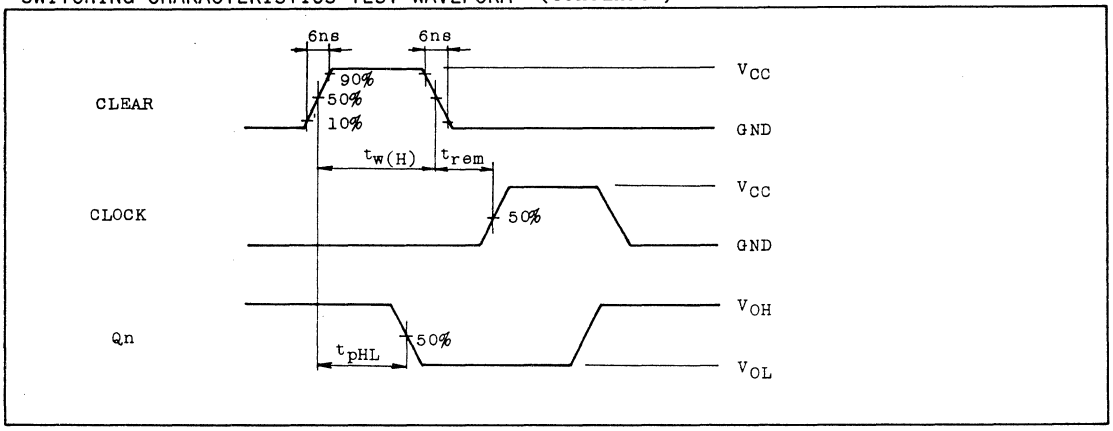
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

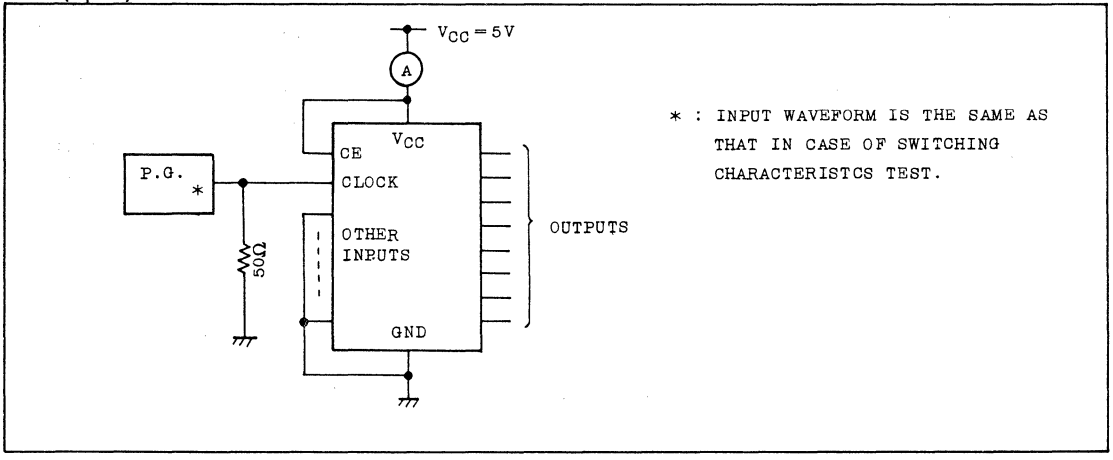
SWITCHING CHARACTERISTICS TEST WAVEFORM



SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTCS TEST.

TC74HC4538AP/AF/AFN

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC4538A is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, A input (Positive edge input), and $\overline{B}$ input (Negative edge input). These inputs are valid for a slow rise/fall time signal (tr=tf=1sec.) as they are schmitt trigger inputs.

After triggering, the output stays in a MONO STABLE STATE for the time period determined by the external resistor and capacitor (Rx, Cx). A low level at $\overline{CD}$ input breaks this STABLE STATE. In the MONO STABLE STATE, if a new trigger is applied, it makes the MONO STABLE period longer (retrigger mode).

Limitations for Cx and Rx are as follows:

External capacitor Cx....No limitation

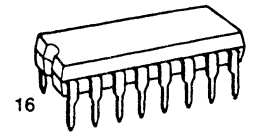
External capacitor Rx....Vcc<3.0V more than 5kΩ

Vcc≥3.0V more than 1kΩ

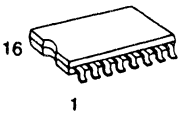
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

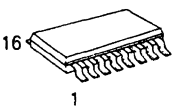
FEATURES:

- High Speed ····· t_{pd}=25ns(typ.)at V_{CC}=5V
- Low Power Dissipation
  - Stand by State I_{CC} =4μA(max.)at Ta=25℃
  - Active State I_{CC}=300μA(max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr.)=2V~6V
- Pin and Function Compatible with 4538B



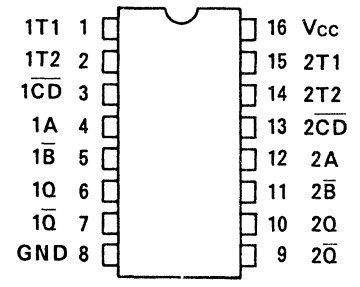
P(DIP16-P-300A)





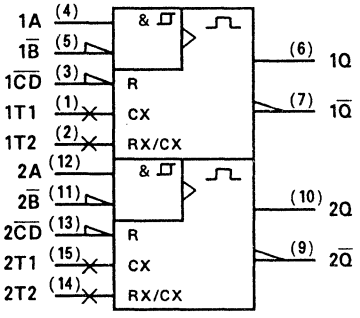
F(SOP16-P-300) FN(SOL16-P-150)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL

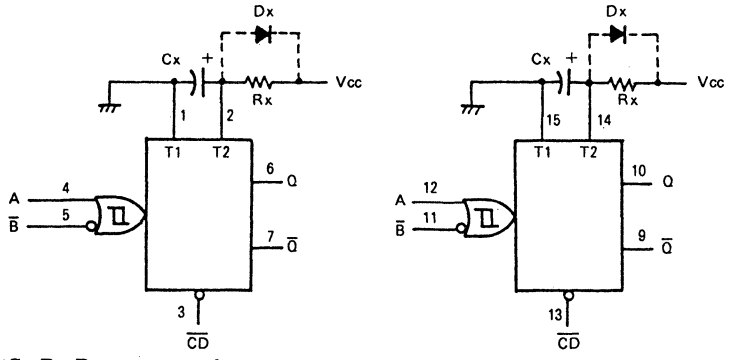


TRUTH TABLE

INPUT			OUTPUT		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↑	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:Don't Care

BLOCK DIAGRAM



Notes: (1)Cx,Rx,Dx are external .
Capacitor,Resistor,and Diode,respectively.

(2)External clamping diode,Dx

The external capacitor is charged to Vcc level in the wait state, i.e. when no trigger is applied. Supply voltage is turned off and Cx is discharged mainly through the internal (parasitic) diode. If Cx is sufficiently large and Vcc drops rapidly, there will be some possibility of damaging the IC by rush current or latch-up. If the capacitance of the supply voltage filter is large enough and Vcc drops slowly, the rush current is automatically limited and damage to the IC is avoided.

The maximum value of forward current through the parasitic diode is ±20mA.

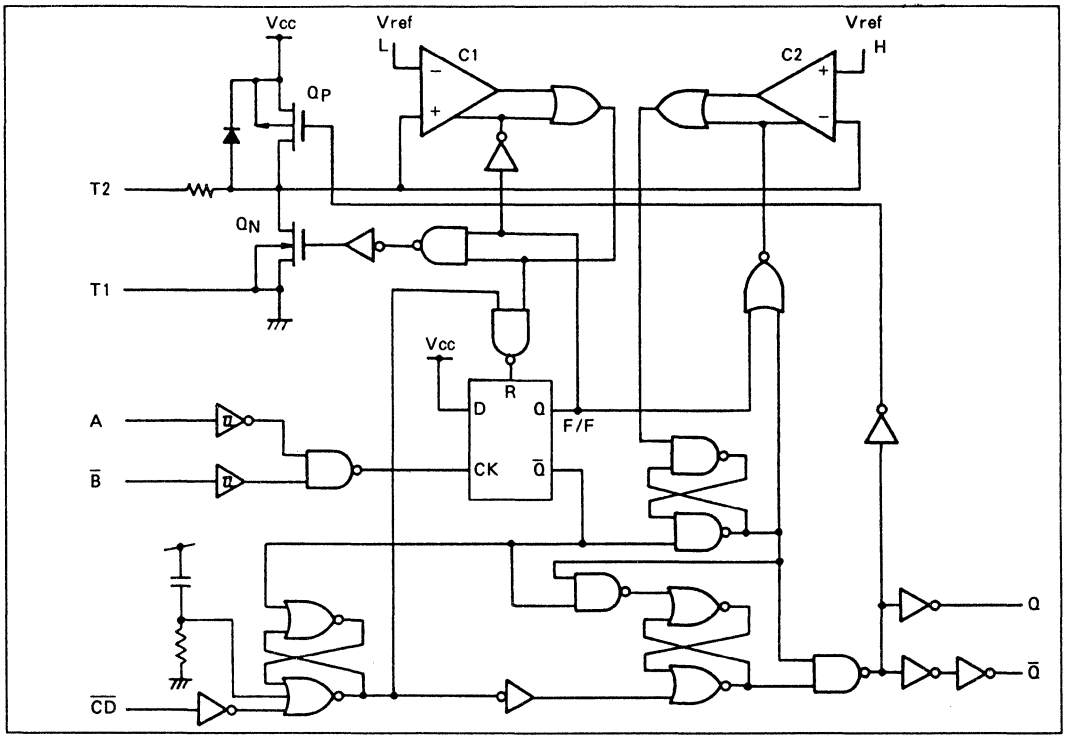
In the case of a large Cx, the limitation of fall time of the supply voltage is determined as follows:

$$t_f \geq (Vcc - 0.7)\ Cx/20mA$$

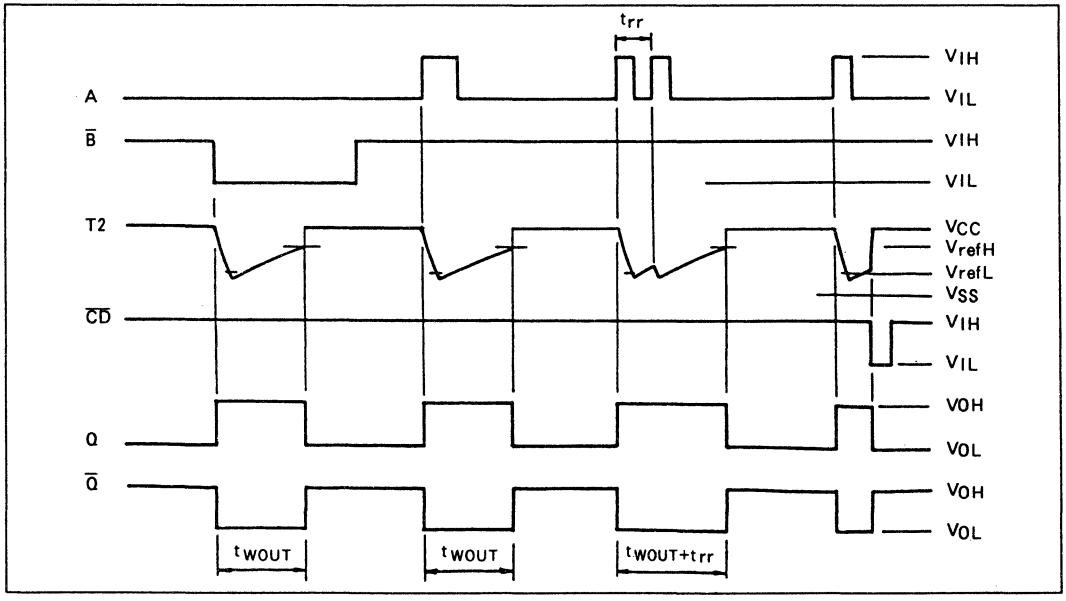
(t_f is the time from the voltage supply turning off to the level of supply voltage reaching 0.4 Vcc.)

In the case of a system that does not satisfy the above condition, an external clamping diode is needed to protect the IC from rush current.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1)Stand-by State

The external capacitor is fully charge to Vcc in the stand-by state. That means, befor triggering, Q_P and Q_N transistors which are connected to the T2 node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies stop their operation. The total supply current is only leakage current.

(2)Trigger operation

Trigger operation is effective in either of the following two cases. One is the condition where the A input is low, and the $\overline{B}$ input has a falling signal. The other, where the $\overline{B}$ input is high, and the A input has a rising signal.

After trigger becomes effective, comparators C1 and C2 start operating, and Q_N is turned on. The external capacitor discharges through Q_N. The voltage level of the T2 node drops. If the T2 voltage level falls to the internal reference voltage Vref L, the output of C1 becomes low. The flip-flop is then reset and Q_N turns off. At that moment C1 stops but C2 continues operating.

After Q_N turns off, the voltage at T2 start rising at a rate determined by the time constant of external capacitor Cx and resistor Rx.

After the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of T2 changes from falling to rising. When T2 reaches the internal reference voltage Vref H, the output of C2 becomes low, the output Q goes low and C2 stops its operation. That means, after triggering, when the voltage level of T2 reaches Vref H, the IC returns to its MONO STABLE STATE.

In the case of large value of Cx and Rx, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse tw (OUT)is as follows:

$$tw\ (OUT) = 0.70\,Cx\,Rx$$

(3)Retrigger operation

When another new trigger is applied to input A or $\overline{B}$ while in the MONO STABLE STATE, it is effective only if the IC is charging Cx. The voltage level of T2 then falls to Vref L level again. Therefore the Q output stays high if the next trigger comes in before the time period set by Cx and Rx.

If the 2nd trigger is very close to previous trigger, such as application during the discharge cycle, the 2nd trigger will not be effective.

The minimum time for effective 2nd trigger, trr(Min), depends on Vcc and Cx.

(4)Reset operation

In normal operation, $\overline{CD}$ input is held high. If $\overline{CD}$ is low, a trigger has no effect because the Q output is held low and trigger control F/F is reset. Also Q_P turns on and Cx is charged rapidly to Vcc.

This means if $\overline{CD}$ input is set low, the IC goes into a wait state.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time ($\overline{CD}$ Only)	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns
External Capactior	Cx	No Limitation *	F
External Resistor	Rx	≥5K*(V_{CC}<3.0V) ≥1K*(V_{CC}≥3.0V)	Ω

* The maximum allowable values of Cx and Rx are a function of leakage of capacitor Cx, the leakage of TC74HC4538A, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for Rx>1MΩ.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage (Q,$\overline{Q}$)	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage (Q,$\overline{Q}$)	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
R/C Terminal Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active−State * Supply Current	I_{CC}	V_{IN} =V_{CC} or GND Rx/Cx ext=0.5V_{CC}		2.0	−	40	120	−	160	μA
				4.5	−	0.2	0.3	−	0.4	mA
				6.0	−	0.3	0.6	−	0.8	mA

*: per circuit

TIMING REQUIREMENTS(Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ TYP.	Ta=25℃ LIMIT	Ta=−40 ~85℃ LIMIT	UNIT
Minimum Pulse Width (A,$\overline{B}$)	$t_{W(L)}$ $t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Width ($\overline{CD}$)	$t_{W(L)}$		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Clear Removal Time	t_{rem}		2.0	−	15	15	
			4.5	−	5	5	
			6.0	−	5	5	
Minimum Retrigger Time	t_{rr}	Rx=1KΩ Cx=100pF	2.0	380	−	−	
			4.5	92	−	−	
			6.0	72	−	−	
		Rx=1KΩ Cx=0.01pF	2.0	6.0	−	−	μs
			4.5	1.4	−	−	
			6.0	1.2	−	−	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time (A, $\overline{B}$–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		–	25	44	
Propagation Delay Time ($\overline{CD}$–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		–	21	34	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

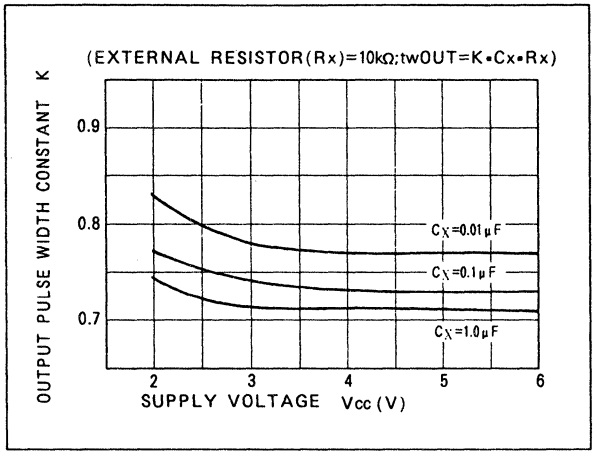
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃ MIN.	TYP.	MAX.	Ta=−40 ~85℃ MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (A, $\overline{B}$–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	120	250	–	315	
			4.5	–	30	50	–	63	
			6.0	–	25	43	–	54	
Propagation Delay Time ($\overline{CD}$–Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	–	100	195	–	245	
			4.5	–	25	39	–	49	
			6.0	–	20	33	–	42	
Output Pulse Width	tw_{OUT}	Cx=0 Rx=5KΩ(V_{CC} =2V) Rx=1KΩ(V_{CC} =4.5V,6V)	2.0	–	540	1200	–	1500	ns
			4.5	–	180	250	–	320	
			6.0	–	150	200	–	260	
		Cx=0.01μF Rx=10KΩ	2.0	70	83	96	70	96	μs
			4.5	69	77	85	69	85	
			6.0	69	77	85	69	85	
		Cx=0.1μF Rx=10KΩ	2.0	0.67	0.75	0.83	0.67	0.83	ms
			4.5	0.67	0.73	0.77	0.67	0.77	
			6.0	0.67	0.73	0.77	0.67	0.77	
Output Pulse Width Error Between Circuits (In same Package)	Δtw_{OUT}			–	±1	–	–	–	%
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	70	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

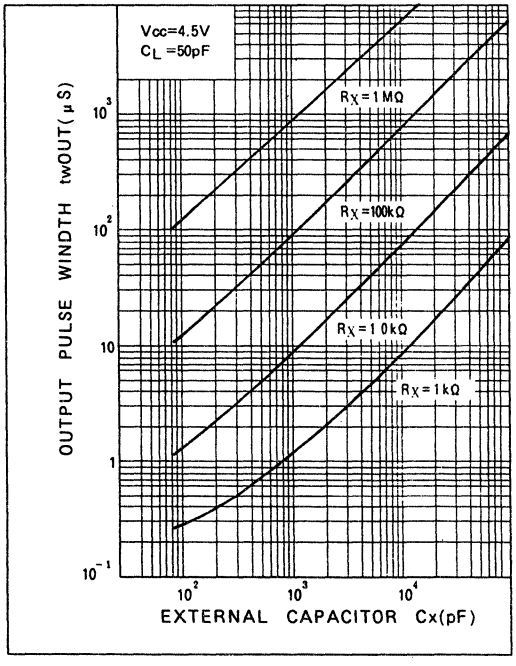
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot \text{Duty}/100 + I_{CC}/2 \text{ (per Circuit)}$$

(I_{CC}': Active Supply Current)
(Duty: %)

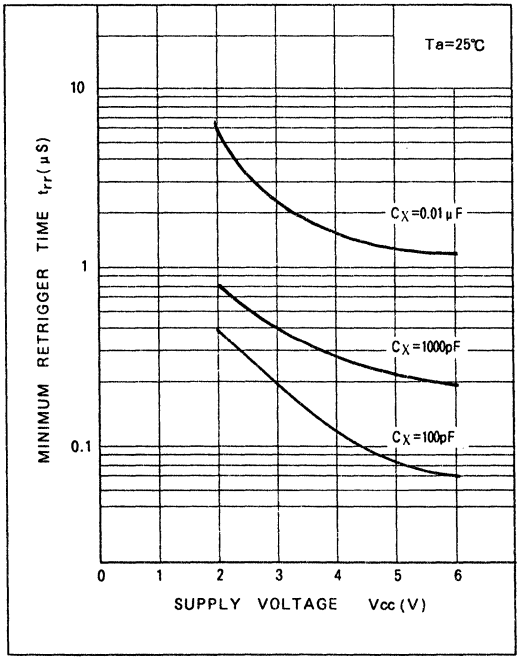
OUTPUT PULSE WIDTH CONSTANT,K–SUPPLY VOLTAGE(TYP.)



twOUT–Cx CHARACTERISTICS(TYP.)



trr–Vcc CHARACTERISTICS(TYP.)



BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

The TC74HC4543A is a high speed CMOS BCD-TO-7 SEGMENT DECODER with LCD DRIVER fabricated with sillicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device consists of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for the liquid crystal display (LCD).

When an error code (over 10) is applied to BCD inputs or, when blanking input (BI) is held high, all segment outputs will go low (turn off).

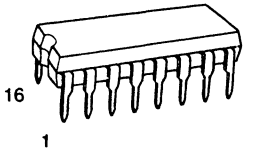
When driving LCD, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display.

For other types of readouts, such as light emitting diodes (LED), some additional drivers, such as a transistor array, is required.

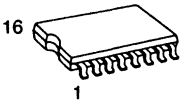
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_w=6ns(Typ.)at V_{CC} =5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ =28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr)=2V~6V
- Pin and Function Compatible with 4543B

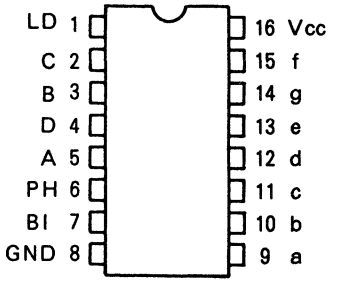


P(DIP16-P-300A)



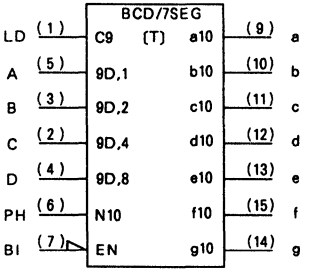
F(SOP16-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

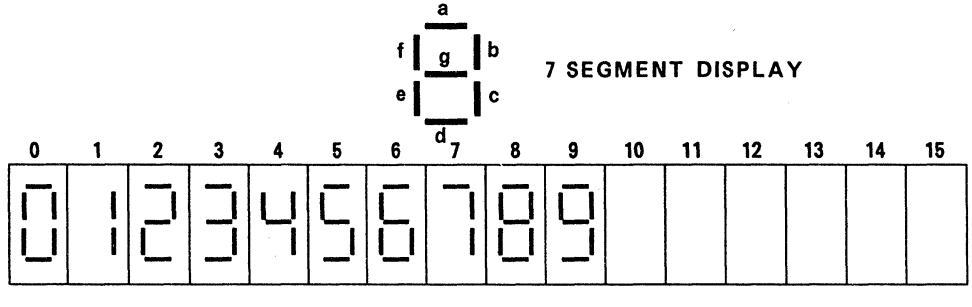
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	###							###
↑	↑	H	↑				INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X:Don't care

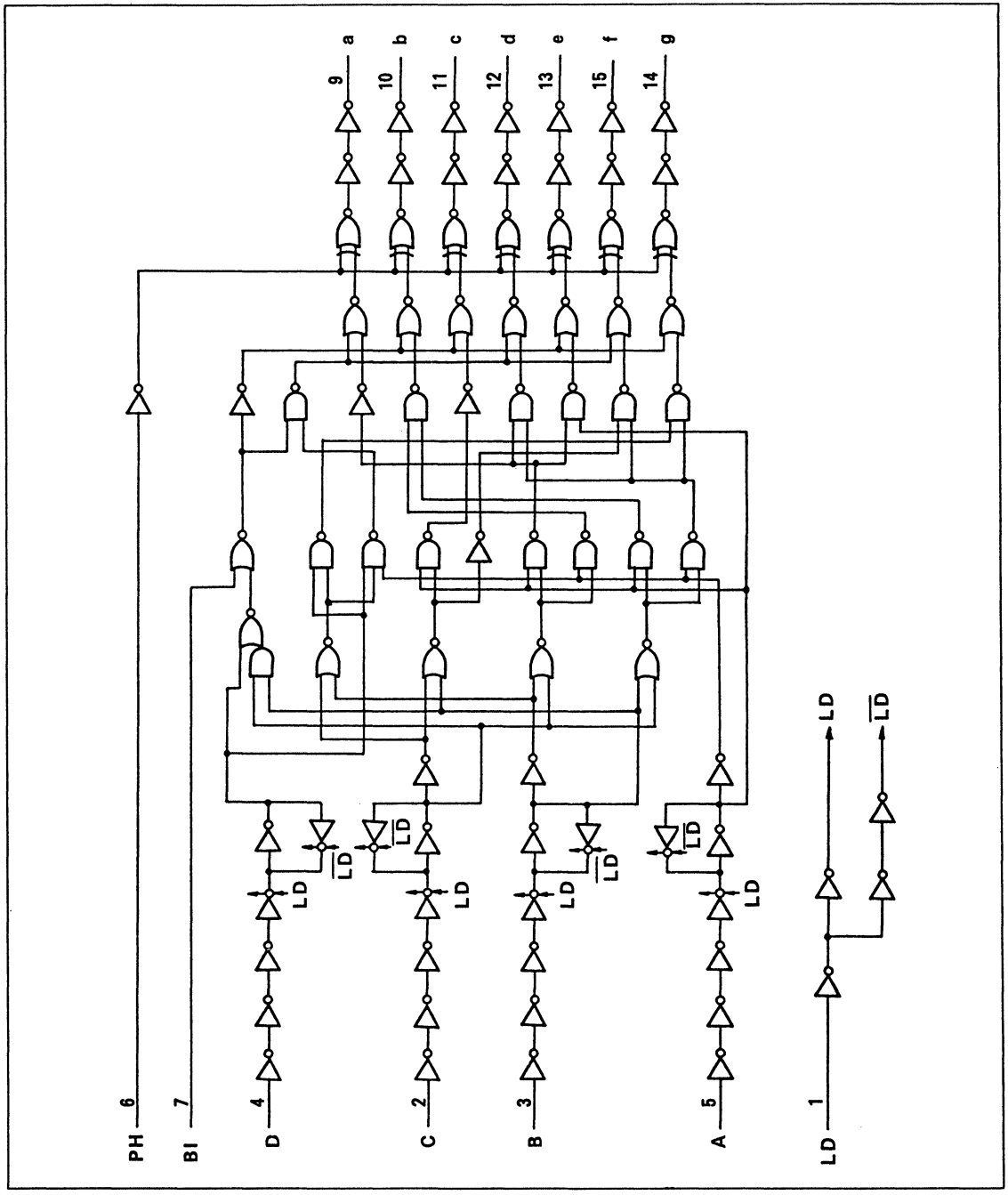
↑:SAME AS ABOVE COMBINATIONS

###:DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD="H"

DISPLAY MODE



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC}/Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃～ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	℃
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000(V_{CC}=2.0V)$ $0 \sim 500(V_{CC}=4.5V)$ $0 \sim 400(V_{CC}=6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40～85℃ MIN.	Ta=−40～85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low−Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS(Input $t_r = t_f$ =6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃		Ta=−40 ~ 85℃	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (LD)	$t_{W(H)}$		2.0	−	75	95	ns
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Set-up Time	t_s		2.0	−	75	95	
			4.5	−	15	19	
			6.0	−	13	16	
Minimum Hold Time	t_h		2.0	−	0	0	
			4.5	−	0	0	
			6.0	−	0	0	

AC ELECTRICAL CHARACTERISTICS(C_L =15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		−	4	8	ns
Propagation Delay Time (BCD−OUT)	t_{pLH} t_{pHL}		−	32	53	
Propagation Delay Time (BI−OUT)	t_{pLH} t_{pHL}		−	18	30	
Propagation Delay Time (PH−OUT)	t_{pLH} t_{pHL}		−	13	22	
Propagation Delay Time (LD−OUT)	t_{pLH} t_{pHL}		−	26	46	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input $t_r = t_f$ =6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25℃			Ta=−40 ~85℃		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	−	30	75	−	95	ns
			4.5	−	8	15	−	19	
			6.0	−	7	13	−	16	
Propagation Delay Time (BCD−OUT)	t_{pLH} t_{pHL}		2.0	−	160	300	−	375	
			4.5	−	40	60	−	75	
			6.0	−	30	51	−	64	
Propagation Delay Time (BI−OUT)	t_{pLH} t_{pHL}		2.0	−	80	175	−	220	
			4.5	−	23	35	−	44	
			6.0	−	17	30	−	37	
Propagation Delay Time (PH−OUT)	t_{pLH} t_{pHL}		2.0	−	58	130	−	165	
			4.5	−	17	26	−	33	
			6.0	−	14	22	−	28	
Propagation Delay Time (LD−OUT)	t_{pLH} t_{pHL}		2.0	−	130	265	−	335	
			4.5	−	35	53	−	66	
			6.0	−	16	45	−	56	
Input Capacitance	C_{IN}			−	5	10	−	10	pF
Power Dissipation Capacitance	C_{PD}			−	115	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HCT7007AP/AF

HEX BUFFER

The TC74HCT7007A is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

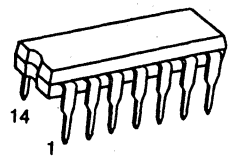
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The internal circuit is composed of 4 stages including a buffer output, which provides high noise immunity and stable output.

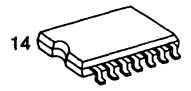
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd} =11ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=1μA(Max.)at Ta=25℃
- Compatible with TTL outputs····· V_{IH}=2V(Min.)
  V_{IL} =0.8V(Max.)
- Wide Interfacing ability····· LSTTL,NMOS,CMOS
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS07

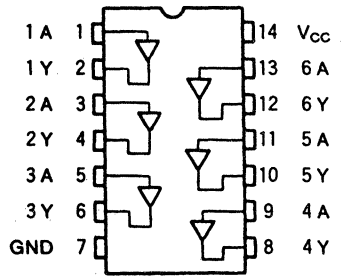


P(DIP14-P-300)



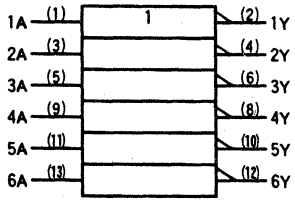
F(SOP14-P-300)

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

A	Y
L	L
H	H

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW· in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃			Ta=−40~85℃		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −4 μA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 4 μA	4.5	−	0.17	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IH} = V_{IL} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IH} = V_{IL} or GND		5.5	−	−	1.0	−	10.0	μA
	ΔI_{CC}	PER INPUT: V_{IN} = 0.5V or 2.4V OTHER INPUT: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(C_L=15pF, V_{CC}=5V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	6	12	ns
Propagation Delay Time	t_{pLH} t_{pHL}		–	11	17	

AC ELECTRICAL CHARACTERISTICS(C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25℃			Ta=−40 ~85℃		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	–	8	15	–	19	ns
			5.5	–	7	14	–	18	
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	–	14	23	–	28	
			5.5	–	12	21	–	26	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)			–	22	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Gate)}$$

TC74HC7240AP/AF
TC74HC7241AP/AF
TC74HC7244AP/AF

OCTAL BUS BUFFER (WITH SCHMITT TRIGGER INPUTS)

TC74HC7240AP/AF	INVERTED, 3-STATE OUTPUTS
TC74HC7241AP/AF	NON-INVERTED, 3-STATE OUTPUTS
TC74HC7244AP/AF	NON-INVERTED, 3-STATE OUTPUTS

The TC74HC7240A/7241A/7244A are high speed CMOS OCTAL BUS BUFFERs with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

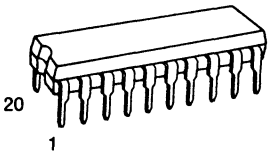
The TC74HC7240A/7241A/7244A have same pin configuration and function as the TC74HC240A/241A/244A. And they have hystereis characteristics on each input, so TC74HC7240A/7241A/7244A can be used as a line receiver, etc.

The TC74HC7240A is an inverting 3-state buffer having two active low output enables. The TC74HC7241A and HC7244A are non-inverting 3-state buffers that differ only in that the HC7241A has one active-high and one active-low output enable, and the HC7244A has two active low output enables.

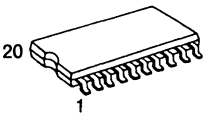
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25℃
- High Noise Immunity ..... V_H=1.1V(typ.)at V_{CC}=5V
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC}(opr)=2V~6V
- Pin and Function Compatible with 74LS240/241/244



P(DIP20-P-300A)



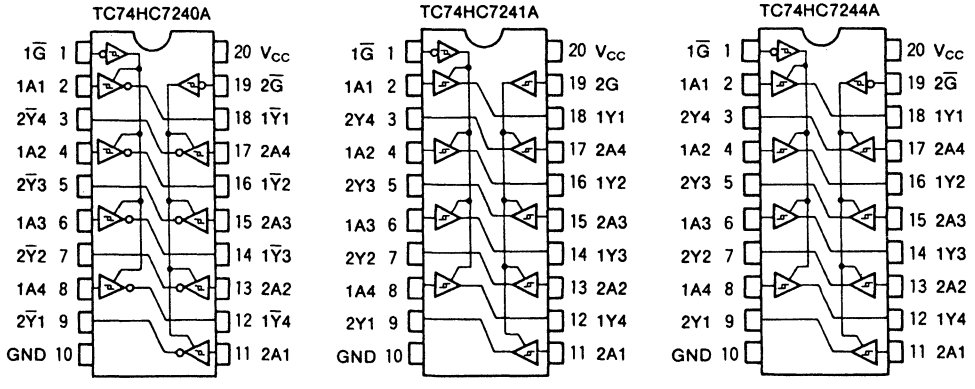
F(SOP20-P-300)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$△△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

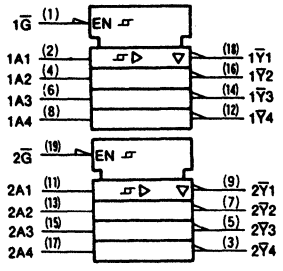
△ : for TC74HC7241A only
△△ : for TC74HC7240A only
X : Don't Care
Z : High Impedance

PIN ASSIGNMENT(TOP VIEW)

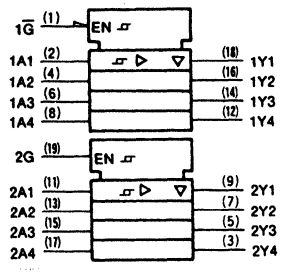


IEC LOGIC SYMBOL

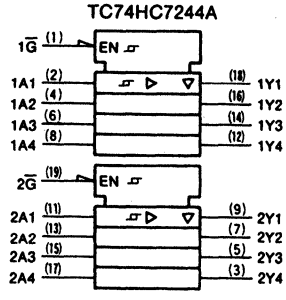
TC74HC7240A



TC74HC7241A



TC74HC7244A



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Positive Threshold Voltage	V_P			2.0	1.0	1.25	1.5	1.0	1.5	V
				4.5	2.3	2.7	3.15	2.3	3.15	
				6.0	3.0	3.5	4.2	3.0	4.2	
Negative Threshold Voltage	V_N			2.0	0.3	0.65	0.9	0.3	0.9	V
				4.5	1.13	1.6	2.0	1.13	2.0	
				6.0	1.5	2.3	2.6	1.5	2.6	
Hysteresis Voltage	V_H			2.0	0.3	0.6	1.0	0.3	1.0	V
				4.5	0.6	1.1	1.4	0.6	1.4	
				6.0	0.8	1.2	1.7	0.8	1.7	
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−7.8mA	6.0	5.68	5.80	−	5.63	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =7.8mA	6.0	−	0.18	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		50	2.0	−	25	60	−	75	ns
				4.5	−	7	12	−	15	
				6.0	−	6	10	−	13	
Propagation Delay Time	t_{pLH}		50	2.0	−	50	125	−	155	
				4.5	−	15	25	−	31	
				6.0	−	13	21	−	26	
	t_{pHL}		150	2.0	−	67	165	−	205	
				4.5	−	20	33	−	41	
				6.0	−	17	28	−	35	
Output Enable time	t_{pZL}	$R_L=1\,k\Omega$	50	2.0	−	68	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	16	26	−	32	
	t_{pZH}		150	2.0	−	84	165	−	230	
				4.5	−	26	37	−	46	
				6.0	−	20	31	−	39	
Output Disable time	t_{pLZ} t_{pHZ}	$R_L=1\,k\Omega$	50	2.0	−	48	150	−	190	
				4.5	−	21	30	−	38	
				6.0	−	19	26	−	32	
Input Capacitance	C_{IN}				−	5	10	−	10	pF
Output Capacitance	C_{OUT}				−	10	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC7240A			−	33	−	−	−	
		TC74HC7241A/7244A			−	34	−	−	−	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{(per bit)}$$

TC74HC7292P
TC74HC7294P

TC74HC7292P PROGRAMMABLE DIVIDER/TIMER
TC74HC7294P PROGRAMMABLE DIVIDER/TIMER

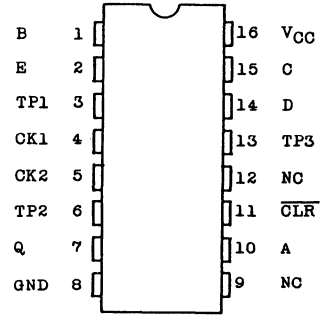
The TC74HC7292 and TC74HC7294 are high speed CMOS PROGRAMMABLE DIVIDER/TIMER fabricated with silicon C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are programmable frequency divider. Both types have two clock inputs, either one may be used for clock gating. (See the function table (1)).
The TC74HC7292 can divide from 2^2 to 2^{31}, and the TC74HC7294 can divide from 2^2 to 2^{15}.
Both types feature an active-low clear input to initialize the state of all flip-flops.
To facilitate incoming inspection, test points are provided. (TP1, TP2 and TP3 on the 74HC7292 and TP on the 74HC7294).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... $f_{MAX}=\begin{matrix}50MHz\ [7292]\\60MHz\ [7294]\end{matrix}$ (Typ.) at $V_{CC}=5V$
- Low Power Dissipation ..... $I_{CC}=4\mu A$(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}=28\%\ V_{CC}$(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Summetrical Output Impedance ..... $|I_{OH}|=I_{OL}=4mA$(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..... $V_{CC(Opr.)}=2V\sim 6V$
- Pin and Function Compatible with 74LS292/294

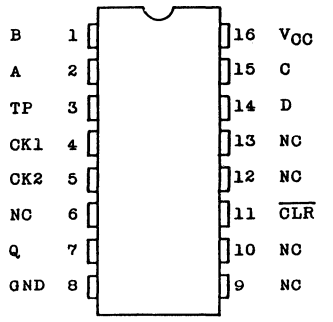
PIN ASSIGNMENT

TC74HC7292



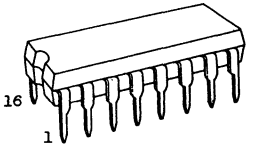
(TOP VIEW)

TC74HC7294



(TOP VIEW)

NC: NO CONNECTION



DIP16(3D16A-P)

TRUTH TABLE

$\overline{\text{CLEAR}}$	CLOCK1	CLOCK2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↓	L	UP Count
H	L	↓	
H	H	X	NO Change
H	X	H	

TC74HC7292

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP2	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2^2	4	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	L	H	H	2^3	8	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	L	2^4	16	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	L	H	2^5	32	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	L	2^6	64	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	L	H	H	H	2^7	128	2^9	512	2^{17}	131,072	2^{24}	16,777,216
L	H	L	L	L	2^8	256	2^9	512	2^{17}	131,072	2^2	4
L	H	L	L	H	2^9	512	2^9	512	2^{17}	131,072	2^2	4
L	H	L	H	L	2^{10}	1,024	2^9	512	2^{17}	131,072	2^4	16
L	H	L	H	H	2^{11}	2,048	2^9	512	2^{17}	131,072	2^4	16
L	H	H	L	L	2^{12}	4,096	2^9	512	2^{17}	131,072	2^6	64
L	H	H	L	H	2^{13}	8,192	2^9	512	2^{17}	131,072	2^6	64
L	H	H	H	L	2^{14}	16,384	2^9	512	Disabled Low		2^8	256
L	H	H	H	H	2^{15}	32,768	2^9	512	Disabled Low		2^8	256
H	L	L	L	L	2^{16}	65,536	2^9	512	2^3	8	2^{10}	1,024
H	L	L	L	H	2^{17}	131,072	2^9	512	2^3	8	2^{10}	1,024
H	L	L	H	L	2^{18}	262,144	2^9	512	2^5	32	2^{12}	4,096
H	L	L	H	H	2^{19}	524,288	2^9	512	2^5	32	2^{12}	4,096
H	L	H	L	L	2^{20}	1,048,576	2^9	512	2^7	128	2^{14}	16,384
H	L	H	L	H	2^{21}	2,097,152	2^9	512	2^7	128	2^{14}	16,384
H	L	H	H	L	2^{22}	4,194,304	Disabled Low		2^9	512	2^{16}	65,536
H	L	H	H	H	2^{23}	8,388,608	Disabled Low		2^9	512	2^{16}	65,536
H	H	L	L	L	2^{24}	16,777,216	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	L	H	2^{25}	33,554,432	2^3	8	2^{11}	2,048	2^{18}	262,144
H	H	L	H	L	2^{26}	67,108,864	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	L	H	H	2^{27}	134,217,728	2^5	32	2^{13}	8,192	2^{20}	1,048,576
H	H	H	L	L	2^{28}	268,435,456	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	L	H	2^{29}	536,870,912	2^7	128	2^{15}	32,768	2^{22}	4,194,304
H	H	H	H	L	2^{30}	1,073,741,824	2^9	512	2^{17}	131,072	2^{24}	16,777,216
H	H	H	H	H	2^{31}	2,147,483,648	2^9	512	2^{17}	131,072	2^{24}	16,777,216

TRUTH TABLE

TC74HC7294

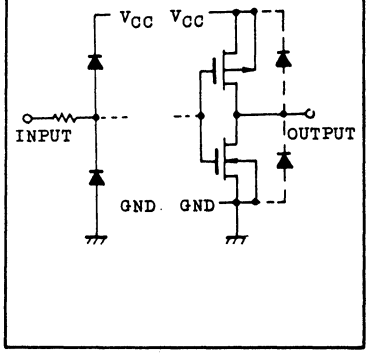
PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2^2	4	2^9	512
L	L	H	H	2^3	8	2^9	512
L	H	L	L	2^4	16	2^9	512
L	H	L	H	2^5	32	2^9	512
L	H	H	L	2^6	64	2^9	512
L	H	H	H	2^7	128	Disabled Low	
H	L	L	L	2^8	256	2^2	4
H	L	L	H	2^9	512	2^3	8
H	L	H	L	2^{10}	1,024	2^4	16
H	L	H	H	2^{11}	2,048	2^5	32
H	H	L	L	2^{12}	4,096	2^6	64
H	H	L	H	2^{13}	8,192	2^7	128
H	H	H	L	2^{14}	16,384	2^8	256
H	H	H	H	2^{15}	32,768	2^9	512

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

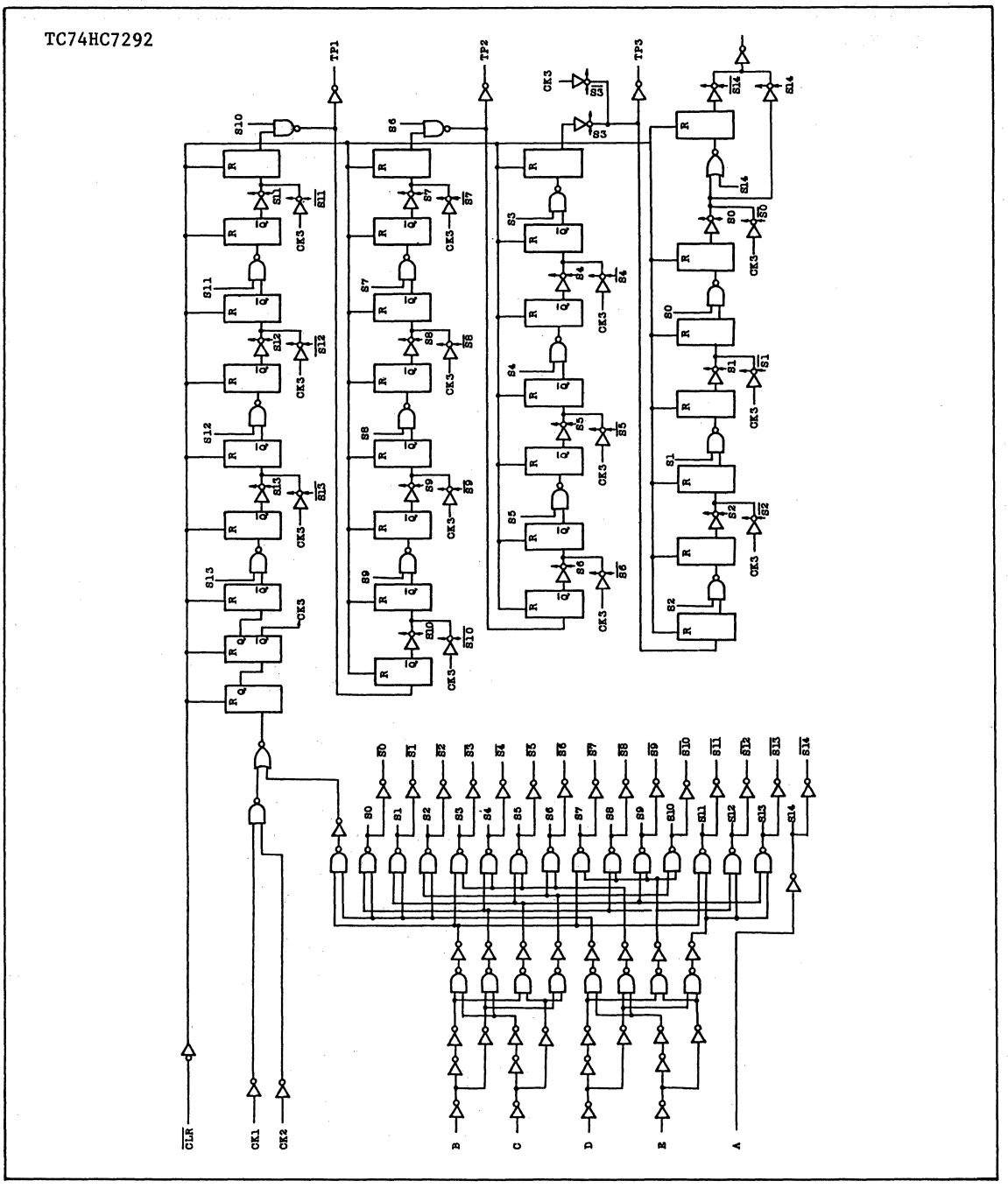
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



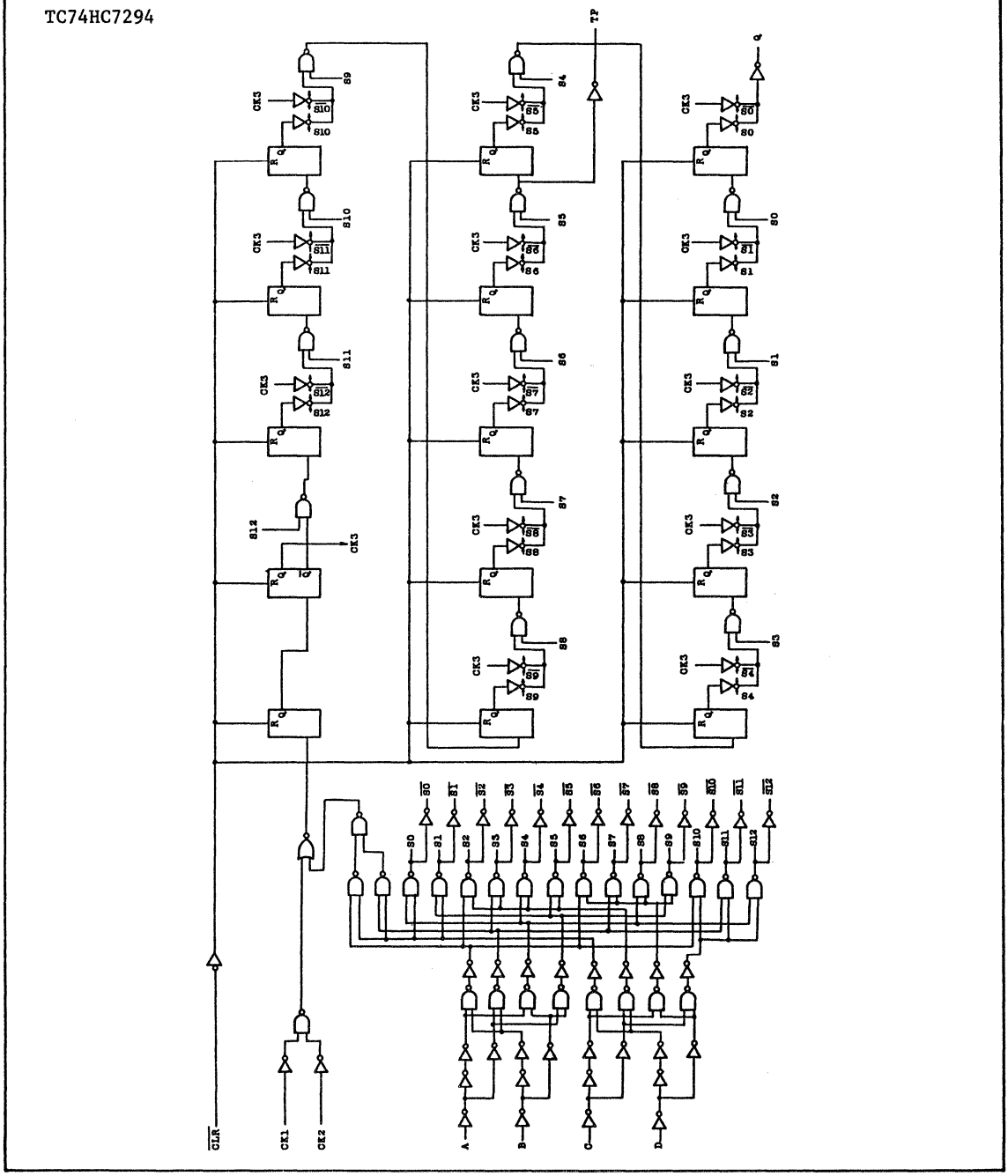
LOGIC DIAGRAM

TC74HC7292



LOGIC DIAGRAM

TC74HC7294



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	
Output Voltage	V_{OUT}	0 ∿ V_{CC}	
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0∿1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

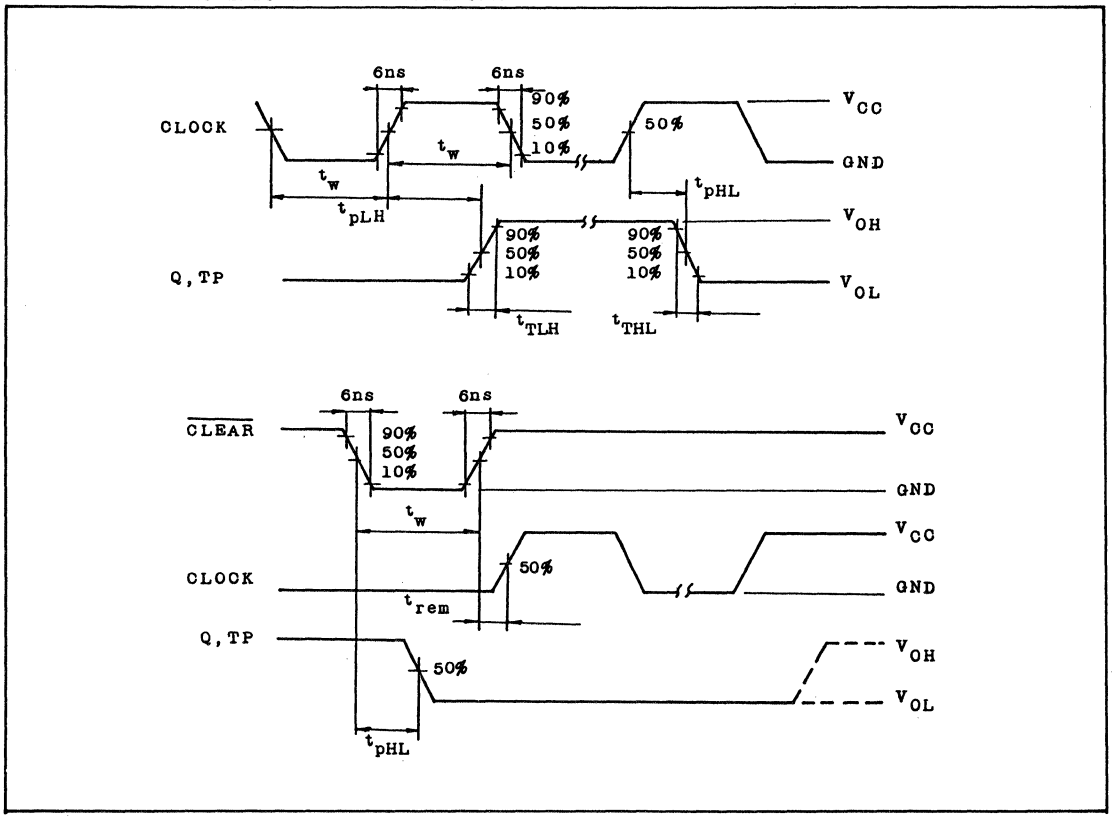
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Transition Time (TP)	t_{TLH} t_{THL}		2.0	-	132	255	-	320	
			4.5	-	33	51	-	64	
			6.0	-	28	43	-	54	
Propagation Delay Time (CLOCK - Q) *	t_{pLH} t_{pHL}	B="H" A=C=D=E="L"	2.0	-	264	500	-	625	
			4.5	-	66	100	-	125	
			6.0	-	56	85	-	106	
Propagation Delay Time (CLOCK - Q) **	t_{pLH} t_{pHL}	B="H" A=C=D="L"	2.0	-	236	455	-	570	
			4.5	-	59	91	-	114	
			6.0	-	50	77	-	97	
Propagation Delay Time ($\overline{CLEAR}$ - Q) *	t_{pHL}		2.0	-	224	425	-	530	
			4.5	-	56	85	-	106	
			6.0	-	48	72	-	90	
Propagation Delay Time ($\overline{CLEAR}$ - Q) **	t_{pHL}		2.0	-	204	390	-	490	
			4.5	-	51	78	-	98	
			6.0	-	43	66	-	83	
Maximum Clock Frequency *	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	32	48	-	26	-	
			6.0	38	56	-	31	-	
Maximum Clock Frequency **	f_{MAX}		2.0	7	14	-	6	-	ns
			4.5	32	55	-	30	-	
			6.0	44	65	-	35	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	36	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Pulse Width ($\overline{CLEAR}$) *	$t_{w(L)}$		2.0	-	60	150	-	190	
			4.5	-	15	30	-	38	
			6.0	-	13	26	-	32	
Minimum Pulse Width ($\overline{CLEAR}$) **	$t_{w(L)}$		2.0	-	72	175	-	220	
			4.5	-	18	35	-	44	
			6.0	-	15	30	-	37	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	74HC7292		-	22	-	-	-	
		74HC7294		-	23	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

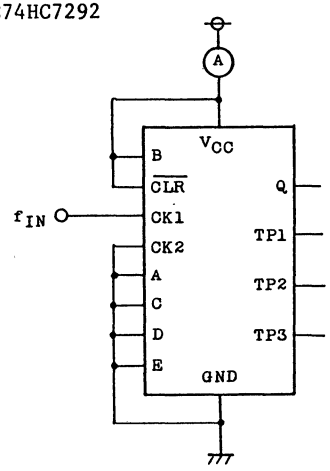
(2): * ; for TC74HC7292
**; for TC74HC7294

SWITCHING CHARACTERISTICS TEST WAVEFORM

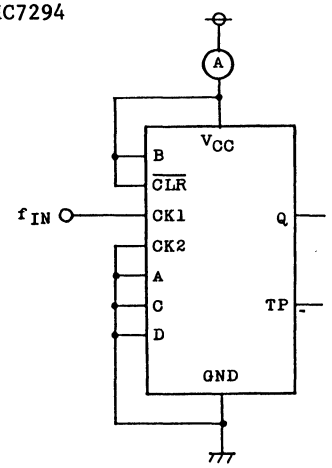


I_{CC}(Opr.) TEST CIRCUIT

TC74HC7292



TC74HC7294



* Input transition time is the same as that in case of switching characteristics test.

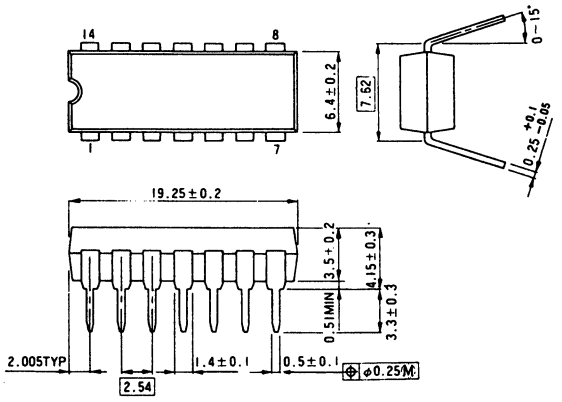
NOTES

11. OUTLINE DRAWINGS

TC74HC/HCT SERIES

DIP 14PIN OUTLINE DRAWING (DIP14-P-300)

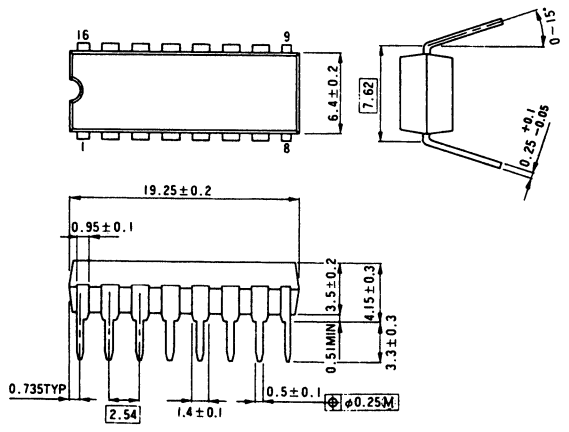
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 16PIN OUTLINE DRAWING (DIP16-P-300A)

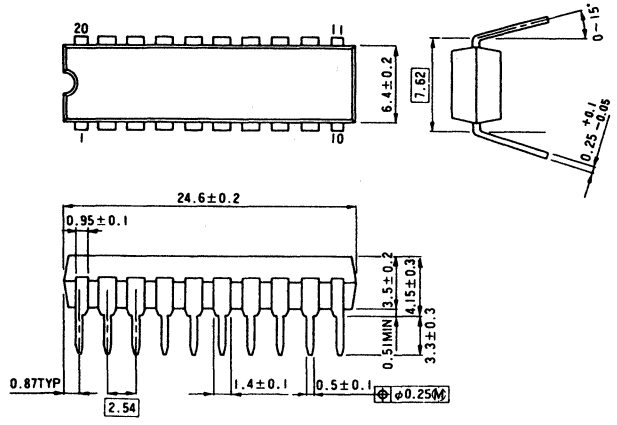
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 20PIN OUTLINE DRAWING (DIP20-P-300A)

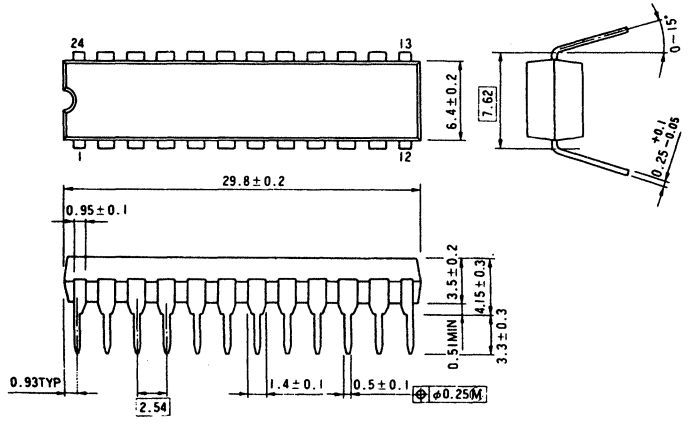
Unit in mm



Note) Package width and length do not include mold protrusion.

DIP 24PIN OUTLINE DRAWING (DIP24-P-300)

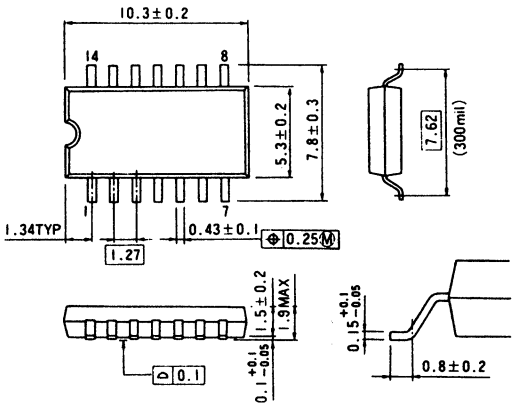
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300)

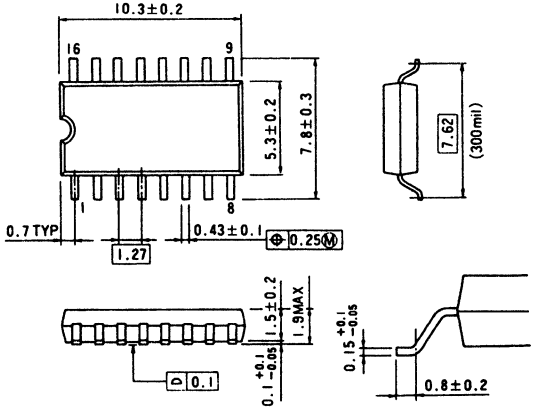
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300)

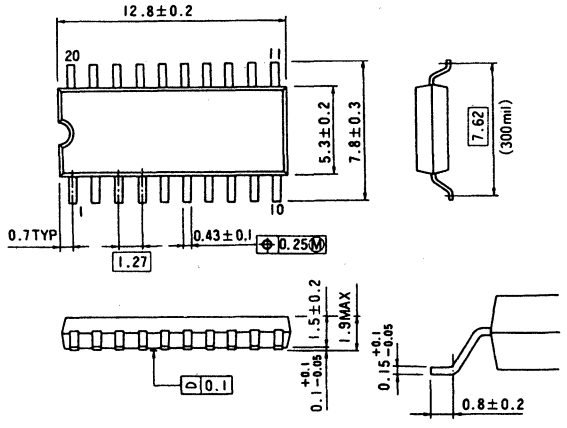
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 20PIN (200mil BODY) OUTLINE DRAWING (SOP20-P-300)

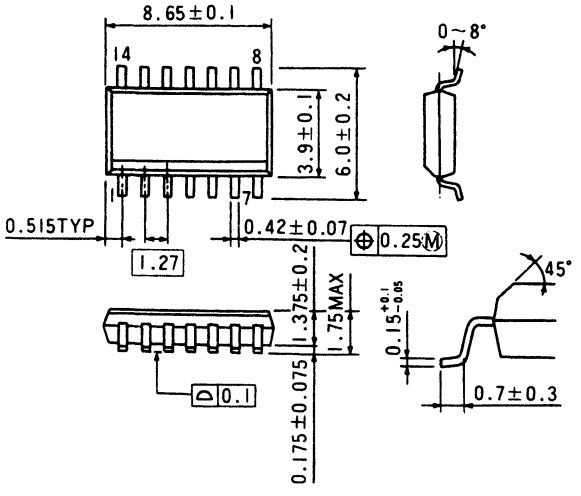
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150)

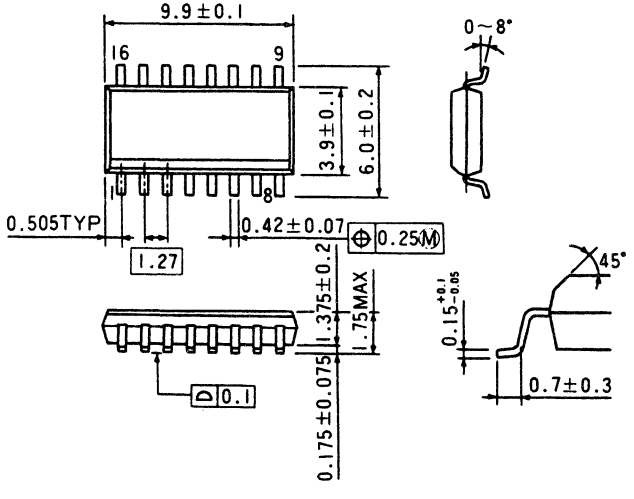
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150)

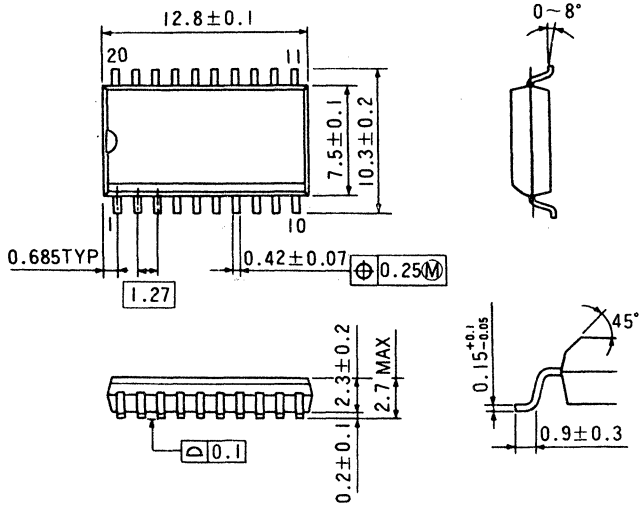
Unit in mm



Note) Package width and length do not include mold protrusion.

SOP 20PIN (300mil BODY) OUTLINE DRAWING (SOL20-P-300)

Unit in mm



Note) Package width and length do not include mold protrusion.

12. CROSS REFERENCE GUIDE

TC74HC/HCT SERIES

CROSS REFERENCE GUIDE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC00A	MC74HC00	SN74HC00	CD74HC00	PC74HC00	MM74HC00
TC74HCT00A			CD74HCT00	PC74HCT00	MM74HCT00
TC74HC02A	MC74HC02	SN74HC02	CD74HC02	PC74HC02	MM74HC02
TC74HCT02A			CD74HCT02	PC74HCT02	
TC74HC03A	MC74HC03	SN74HC03	CD74HC03	PC74HC03	MM74HC03
TC74HC04A	MC74HC04	SN74HC04	CD74HC04	PC74HC04	MM74HC04
TC74HCU04A	MC74HCU04	SN74HCU04	CD74HCU04	PC74HCU04	MM74HCU04
TC74HCT04A	MC74HCT04		CD74HCT04	PC74HCT04	MM74HCT04
TC74HC05A	MC74HC05	SN74HC05			
TC74HC07A					
TC74HC08A	MC74HC08	SN74HC08	CD74HC08	PC74HC08	MM74HC08
TC74HCT08A			CD74HCT08	PC74HCT08	
TC74HC09A		SN74HC09			
TC74HC10A	MC74HC10	SN74HC10	CD74HC10	PC74HC10	MM74HC10
TC74HC11A	MC74HC11	SN74HC11	CD74HC11	PC74HC11	MM74HC11
TC74HC14A	MC74HC14	SN74HC14	CD74HC14	PC74HC14	MM74HC14
TC74HC20A	MC74HC20	SN74HC20	CD74HC20	PC74HC20	MM74HC20
TC74HC21A		SN74HC21	CD74HC21	PC74HC21	
TC74HC27A	MC74HC27	SN74HC27	CD74HC27	PC74HC27	MM74HC27
TC74HC30A	MC74HC30	SN74HC30	CD74HC30	PC74HC30	MM74HC30
TC74HC32A	MC74HC32	SN74HC32	CD74HC32	PC74HC32	MM74HC32
TC74HCT32A			CD74HCT32	PC74HCT32	
TC74HC42A	MC74HC42	SN74HC42	CD74HC42	PC74HC42	MM74HC42
TC74HC51A	MC74HC51	SN74HC51			MM74HC51
TC74HC73A	MC74HC73	SN74HC73	CD74HC73	PC74HC73	MM74HC73
TC74HC74A	MC74HC74	SN74HC74	CD74HC74	PC74HC74	MM74HC74
TC74HCT74A			CD74HCT74	PC74HCT74	MM74HCT74
TC74HC75A	MC74HC75	SN74HC75	CD74HC75	PC74HC75	MM74HC75
TC74HC76A	MC74HC76	SN74HC76			MM74HC76
TC74HC77A		SN74HC77			
TC74HC85A	MC74HC85	SN74HC85	CD74HC85	PC74HC85	MM74HC85
TC74HC86A	MC74HC86	SN74HC86	CD74HC86	PC74HC86	MM74HC86
TC74HCT86A			CD74HCT86	PC74HCT86	
TC74HC107A	MC74HC107	SN74HC107	CD74HC107	PC74HC107	MM74HC107
TC74HC109A	MC74HC109	SN74HC109	CD74HC109	PC74HC109	MM74HC109
TC74HC112A	MC74HC112	SN74HC112	CD74HC112	PC74HC112	MM74HC112
TC74HC113A	MC74HC113	SN74HC113			MM74HC113
TC74HC123			CD74HC123	PC74HC123	
TC74HC123A	MC74HC123A				MM74HC123A
TC74HC125A	MC74HC125	SN74HC125	CD74HC125	PC74HC125	MM74HC125
TC74HC126A	MC74HC126	SN74HC126	CD74HC126	PC74HC126	MM74HC126
TC74HC131A					
TC74HC132A	MC74HC132		CD74HC132	PC74HC132	MM74HC132
TC74HC133A	MC74HC133	SN74HC133			MM74HC133
TC74HC137A	MC74HC137	SN74HC137	CD74HC137	PC74HC137	MM74HC137

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TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HCT137A		SN74HCT137	CD74HCT137	PC74HCT137	
TC74HC138A	MC74HC138	SN74HC138	CD74HC138	PC74HC138	MM74HC138
TC74HCT138A		SN74HCT138	CD74HCT138	PC74HCT138	MM74HCT138
TC74HC139A	MC74HC139	SN74HC139	CD74HC139	PC74HC139	MM74HC139
TC74HCT139A			CD74HCT139	PC74HCT139	
TC74HC147A	MC74HC147	SN74HC147	CD74HC147	PC74HC147	MM74HC147
TC74HC148A		SN74HC148			
TC74HC151A	MC74HC151	SN74HC151	CD74HC151	PC74HC151	MM74HC151
TC74HC153A	MC74HC153	SN74HC153	CD74HC153	PC74HC153	MM74HC153
TC74HC154A	MC74HC154	SN74HC154	CD74HC154	PC74HC154	MM74HC154
TC74HC155A					MM74HC155
TC74HC157A	MC74HC157	SN74HC157	CD74HC157	PC74HC157	MM74HC157
TC74HCT157A			CD74HCT157	PC74HCT157	MM74HCT157
TC74HC158A	MC74HC158	SN74HC158	CD74HC158	PC74HC158	MM74HC158
TC74HCT158A			CD74HCT158	PC74HCT158	MM74HCT158
TC74HC160A	MC74HC160	SN74HC160	CD74HC160	PC74HC160	MM74HC160
TC74HC161A	MC74HC161	SN74HC161	CD74HC161	PC74HC161	MM74HC161
TC74HC162A	MC74HC162	SN74HC162	CD74HC162	PC74HC162	MM74HC162
TC74HC163A	MC74HC163	SN74HC163	CD74HC163	PC74HC163	MM74HC163
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TC74HC165A	MC74HC165	SN74HC165	CD74HC165	PC74HC165	MM74HC165
TC74HC166A	MC74HC166	SN74HC166	CD74HC166	PC74HC166	
TC74HC173A	MC74HC173	SN74HC173	CD74HC173	PC74HC173	MM74HC173
TC74HC174A	MC74HC174	SN74HC174	CD74HC174	PC74HC174	MM74HC174
TC74HCT174A			CD74HCT174	PC74HCT174	
TC74HC175A	MC74HC175	SN74HC175	CD74HC175	PC74HC175	MM74HC175
TC74HC181A	MC74HC181		CD74HC181	PC74HC181	MM74HC181
TC74HC182A	MC74HC182		CD74HC182	PC74HC182	MM74HC182
TC74HC190A	MC74HC190	SN74HC190	CD74HC190	PC74HC190	MM74HC190
TC74HC191A	MC74HC191	SN74HC191	CD74HC191	PC74HC191	MM74HC191
TC74HC192A	MC74HC192	SN74HC192	CD74HC192	PC74HC192	MM74HC192
TC74HC193A	MC74HC193	SN74HC193	CD74HC193	PC74HC193	MM74HC193
TC74HC194A	MC74HC194	SN74HC194	CD74HC194	PC74HC194	MM74HC194
TC74HC195A	MC74HC195	SN74HC195	CD74HC195	PC74HC195	MM74HC195
TC74HC221			CD74HC221	PC74HC221	
TC74HC221A	MC74HC221A				MM74HC221A
TC74HC237A	MC74HC237	SN74HC237	CD74HC237	PC74HC237	MM74HC237
TC74HC238A		SN74HC238	CD74HC238	PC74HC238	MM74HC238
TC74HC240A	MC74HC240	SN74HC240	CD74HC240	PC74HC240	MM74HC240
TC74HCT240A	MC74HCT240	SN74HCT240	CD74HCT240	PC74HCT240	MM74HCT240
TC74HC241A	MC74HC241	SN74HC241	CD74HC241	PC74HC241	MM74HC241
TC74HCT241A	MC74HCT241	SN74HCT241	CD74HCT241	PC74HCT241	MM74HCT241
TC74HC242A	MC74HC242	SN74HC242	CD74HC242	PC74HC242	MM74HC242
TC74HC243A	MC74HC243	SN74HC243	CD74HC243	PC74HC243	MM74HC243

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TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC244A	MC74HC244	SN74HC244	CD74HC244	PC74HC244	MM74HC244
TC74HCT244A	MC74HCT244	SN74HCT244	CD74HCT244	PC74HCT244	MM74HCT244
TC74HC245A	MC74HC245	SN74HC245	CD74HC245	PC74HC245	MM74HC245
TC74HCT245A	MC74HCT245	SN74HCT245	CD74HCT245	PC74HCT245	MM74HCT245
TC74HC251A	MC74HC251	SN74HC251	CD74HC251	PC74HC251	MM74HC251
TC74HC253A	MC74HC253	SN74HC253	CD74HC253	PC74HC253	MM74HC253
TC74HC257A	MC74HC257	SN74HC257	CD74HC257	PC74HC257	MM74HC257
TC74HCT257A			CD74HCT257	PC74HCT257	MM74HCT257
TC74HC258A		SN74HC258	CD74HC258	PC74HC258	
TC74HCT258A			CD74HCT258	PC74HCT258	
TC74HC259A	MC74HC259	SN74HC259	CD74HC259	PC74HC259	MM74HC259
TC74HC266A	MC74HC266	SN74HC266			MM74HC266
TC74HC273A	MC74HC273	SN74HC273	CD74HC273	PC74HC273	MM74HC273
TC74HCT273A			CD74HCT273	PC74HCT273	MM74HCT273
TC74HC279A					
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TC74HC283A	MC74HC283		CD74HC283	PC74HC283	MM74HC283
TC74HC298A	MC74HC298	SN74HC298			MM74HC298
TC74HC299A	MC74HC299		CD74HC299	PC74HC299	MM74HC299
TC74HC323A					MM74HC323
TC74HC352A		SN74HC352			
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TC74HC356A	MC74HC356	SN74HC356	CD74HC356	PC74HC356	MM74HC356
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TC74HC367A	MC74HC367	SN74HC367	CD74HC367	PC74HC367	MM74HC367
TC74HC368A	MC74HC368	SN74HC368	CD74HC368	PC74HC368	MM74HC368
TC74HC373A	MC74HC373	SN74HC373	CD74HC373	PC74HC373	MM74HC373
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TC74HCT374A	MC74HCT374	SN74HCT374	CD74HCT374	PC74HCT374	MM74HCT374
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TC74HC386A		SN74HC386			
TC74HC390A	MC74HC390	SN74HC390	CD74HC390	PC74HC390	MM74HC390
TC74HC393A	MC74HC393	SN74HC393	CD74HC393	PC74HC393	MM74HC393
TC74HC423			CD74HC423	PC74HC423	
TC74HC423A					MM74HC423A
TC74HC533A	MC74HC533	SN74HC533	CD74HC533	PC74HC533	MM74HC533
TC74HCT533A	MC74HCT533	SN74HCT533	CD74HCT533	PC74HCT533	MM74HCT533
TC74HC534A	MC74HC534	SN74HC534	CD74HC534	PC74HC534	MM74HC534
TC74HCT534A	MC74HCT534	SN74HCT534	CD74HCT534	PC74HCT534	MM74HCT534
TC74HC540A	MC74HC540	SN74HC540	CD74HC540	PC74HC540	MM74HC540
TC74HCT540A	MC74HCT540	SN74HCT540	CD74HCT540	PC74HCT540	MM74HCT540

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TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC541A	MC74HC541	SN74HC541	CD74HC541	PC74HC541	MM74HC541
TC74HCT541A	MC74HCT541	SN74HCT541	CD74HCT541	PC74HCT541	MM74HCT541
TC74HC563A	MC74HC563	SN74HC563	CD74HC563	PC74HC563	MM74HC563
TC74HCT563A		SN74HCT563	CD74HCT563	PC74HCT563	MM74HCT563
TC74HC564A	MC74HC564	SN74HC564	CD74HC564	PC74HC564	MM74HC564
TC74HCT564A		SN74HCT564	CD74HCT564	PC74HCT564	MM74HCT564
TC74HC573A	MC74HC573	SN74HC573	CD74HC573	PC74HC573	MM74HC573
TC74HCT573A		SN74HCT573	CD74HCT573	PC74HCT573	MM74HCT573
TC74HC574	MC74HC574	SN74HC574	CD74HC574	PC74HC574	MM74HC574
TC74HCT574		SN74HCT574	CD74HCT574	PC74HCT574	MM74HCT574
TC74HC590A					MM74HC590
TC74HC592A					MM74HC592
TC74HC593A					MM74HC593
TC74HC595A	MC74HC595				MM74HC595
TC74HC597A	MC74HC597		CD74HC597	PC74HC597	MM74HC597
TC74HC620A	MC74HC620	SN74HC620			
TC74HC623A	MC74HC623	SN74HC623			
TC74HC640A	MC74HC640	SN74HC640	CD74HC640	PC74HC640	MM74HC640
TC74HCT640A	MC74HCT640	SN74HCT640	CD74HCT640	PC74HCT640	MM74HCT640
TC74HC643A	MC74HC643	SN74HC643	CD74HC643	PC74HC643	MM74HC643
TC74HCT643A	MC74HCT643	SN74HCT643	CD74HCT643	PC74HCT643	MM74HCT643
TC74HC646A	MC74HC646	SN74HC646	CD74HC646	PC74HC646	MM74HC646
TC74HCT646A	MC74HCT646	SN74HCT646	CD74HCT646	PC74HCT646	
TC74HC648A	MC74HC648	SN74HC648	CD74HC648	PC74HC648	MM74HC648
TC74HCT648A		SN74HCT648	CD74HCT648	PC74HCT648	
TC74HC651A	MC74HC651	SN74HC651			
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TC74HC652A	MC74HC652	SN74HC652			
TC74HCT652A		SN74HCT652			
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TC74HC692A					
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TC74HC698A					
TC74HC699A					
TC74HC4002A	MC74HC4002	SN74HC4002	CD74HC4002	PC74HC4002	MM74HC4002
TC74HC4016A	MC74HC4016		CD74HC4016	PC74HC4016	MM74HC4016
TC74HC4017A	MC74HC4017	SN74HC4017	CD74HC4017	PC74HC4017	MM74HC4017
TC74HC4020A	MC74HC4020	SN74HC4020	CD74HC4020	PC74HC4020	MM74HC4020
TC74HC4022A		SN74HC4022			

CROSS REFERENCE GUIDE

TOSHIBA	MOTOROLA	TI	RCA	SIGNETICS	NATIONAL SEMICONDUCTOR
TC74HC4024A	MC74HC4024	SN74HC4024	CD74HC4024	PC74HC4024	MM74HC4024
TC74HC4028A					
TC74HC4040A	MC74HC4040	SN74HC4040	CD74HC4040	PC74HC4040	MM74HC4040
TC74HC4049A	MC74HC4049		CD74HC4049	PC74HC4049	MM74HC4049
TC74HC4050A	MC74HC4050		CD74HC4050	PC74HC4050	MM74HC4050
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TC74HC4053A	MC74HC4053		CD74HC4053	PC74HC4053	MM74HC4053
TC74HC4060A	MC74HC4060	SN74HC4060	CD74HC4060	PC74HC4060	MM74HC4060
TC74HC4066A	MC74HC4066	SN74HC4066	CD74HC4066	PC74HC4066	MM74HC4066
TC74HC4072A					
TC74HC4075A	MC74HC4075	SN74HC4075	CD74HC4075	PC74HC4075	MM74HC4075
TC74HC4078A	MC74HC4078	SN74HC4078A			MM74HC4078
TC74HC4094A			CD74HC4094	PC74HC4094	
TC74HC40102A			CD74HC40102	PC74HC40102	
TC74HC40103A			CD74HC40103	PC74HC40103	
TC74HC40105A			CD74HC40105	PC74HC40105	
TC74HC4316A	MC74HC4316		CD74HC4316	PC74HC4316	MM74HC4316
TC74HC4351A	MC74HC4351		CD74HC4351	PC74HC4351	
TC74HC4352A	MC74HC4352		CD74HC4352	PC74HC4352	
TC74HC4353A	MC74HC4353		CD74HC4353	PC74HC4353	
TC74HC4511A	MC74HC4511		CD74HC4511	PC74HC4511	MM74HC4511
TC74HC4514A	MC74HC4514	SN74HC4514	CD74HC4514	PC74HC4514	MM74HC4514
TC74HC4515A		SN74HC4515	CD74HC4515	PC74HC4515	
TC74HC4518A			CD74HC4518	PC74HC4518	MM74HC4518
TC74HC4520A			CD74HC4520	PC74HC4520	MM74HC4520
TC74HC4538A	MC74HC4538		CD74HC4538	PC74HC4538	MM74HC4538
TC74HC4543A	MC74HC4543		CD74HC4543	PC74HC4543	MM74HC4543
TC74HCT7007A					
TC74HC7240A					
TC74HC7241A					
TC74HC7244A					
TC74HC7266A	MC74HC7266	SN74HC7266	CD74HC7266		
TC74HC7292A					
TC74HC7294A					
TC74HC7640A					
TC74HC7643A					
TC74HC7645A					

NOTES

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

REGIONAL SALES OFFICES

NORTHWEST REGION
1220 Midas Way
Sunnyvale, CA 94086
TEL: (408) 737-9844
FAX: (408) 737-9905

SOUTHWEST REGION
15621 Redhill Ave.
Suite 205
Tustin, CA 92680
TEL: (714) 259-0368
FAX: (714) 259-9439

CENTRAL REGION
One Parkway North
Suite 500
Deerfield, IL 60015-2547
TEL: (708) 945-1500
FAX: (708) 945-1044
TWX: 29-7131

SOUTHCENTRAL REGION
777 E. Campbell Road
Suite 650
Richardson, TX 75081
TEL: (214) 480-0470
FAX: (214) 235-4114

EASTERN REGION
25 Mall Road
5th Floor
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