TOSHIBA AMERICA, INC.

LOGIC

TC74HC SERIES

MAR
1986

INTRODUCTION

TOSHIBA HS-C^2 MOS FAMILY (TC74HC SERIES)

During the past few years, the integration scale of MOS LSIs has made a rapid progress owing to the advance of the micro-lithograph technology. Along with this progress, the heat radiation of MOS LSIs has become a big problem in the same way the bipolar world has been struggling for many years. At present, it is well known that only CMOS technology will solve this problem, and CMOS technology has been adopted increasingly in the field of various LSIs for major example high-performance microprocessors and large capacity memories.

However, there was no general purpose logic IC interfacing these high-performance LSIs except LSTTLs which will satisfy simply the speed requirement.

Therefore, in many cases the excellent features of CMOS LSIs could not be fully utilized in the application systems.

The TC74HC series IC is the CMOS logic IC in a new generation which achieves the high-speed operation thirty times as much as that of conventional B series CMOS IC while maintaining the low power dissipation of conventional CMOS. This high-performance was accomplished utilizing as much advanced micro-lithograph technology as that of the high-performance CMOS LSIs.

These logic ICs will bring a large improvement into the limited performance of conventional systems in every respect of characteristics such as power dissipation, noise margin, margin for operating voltage and operating temperature, etc.

Since the individual ICs are pin-to-pin compatible with LSTTL or conventional B series CMOS, no logical redesign may be required at the time of adopting TC74HC series ICs into the existing systems.

This data book provides technical information on TOSHIBA's TC74HC series high-speed C^{2}MOS devices. The contents described in this data book are subject to change without notice due to standardization of the specification in JEDEC, etc.

Note: Toshiba does not assume any responsibility for use of any circuity described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

CONTENTS

1. HIGH SPEED CMOS PRODUCT GUIDE

(* : Mentioned in this Hand Book)

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC00*	QUAD 2-INPUT NAND GATE	14	13	O	O
TC74HC02*	QUAD 2-INPUT NOR GATE	14	16	O	O
TC74HC03*	QUAD 2-INPUT NAND GATE (OPEN DRAIN)	14	19	O	O
TC74HC04*	HEX INVERTER	14	23	O	O
TC74HCT04*	HEX INVERTER	14	26	O	O
TC74HCU04*	HEX INVERTER (SINGLE STAGE)	14	29	O	O
TC74HC08*	QUAD 2-INPUT AND GATE	14	32	O	O
TC74HC10*	TRIPLE 3-INPUT NAND GATE	14	35	O	O
TC74HC11*	TRIPLE 3-INPUT AND GATE	14	38	O	O
TC74HC14*	HEX SCHMITT INVERTER	14	41	O	O
TC74HC20*	DUAL 4-INPUT NAND GATE	14	45	O	O
TC74HC21*	DUAL 4-INPUT AND GATE	14	48	O	O
TC74HC27*	TRIPLE 3-INPUT NOR GATE	14	51	O	O
TC74HC30*	8-INPUT NAND GATE	14	54	O	O
TC74HC32*	QUAD 2-INPUT OR GATE	14	57	O	O
TC74HC42*	BCD TO DECIMAL DECODER	16	60	O	O
TC74HC51*	DUAL 2W-2I AND/OR INVERT GATE	14	64	O	O
TC74HC73*	DUAL J-K FLIP-FLOP WITH CLEAR	14	68	O	2Q86
TC74HC74*	DUAL D FLIP-FLOP WITH PRESET AND CLEAR	14	73	O	O
TC74HC75*	4-BIT D-TYPE LATCH	16	78	O	O
TC74HC76*	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	16	83	O	O
TC74HC77*	4-BIT D-TYPE LATCH	14	88	O	2Q86
TC74HC85*	4-BIT MAGNITUDE COMPARATOR	16	93	O	O
TC74HC86*	QUAD EXCLUSIVE OR GATE	14	98	O	O
TC74HC107*	DUAL J-K FLIP-FLOP	14	102	O	O
TC74HC109*	DUAL J-K FLIP-FLOP WITH PRESET AND CLEAR	16	107	O	
TC74HC112*	DUAL J-K FLIP-FLOP	16	112	O	O
TC74HC113*	DUAL J-K FLIP-FLOP	14	117	O	
TC74HC123*	DUAL MONOSTABLE MULTIVIBRATOR	16	122	O	O
TC74HC125*	QUAD BUS BUFFER (3-STATE)	14	130	O	O

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC126*	QUAD BUS BUFFER (3-STATE)	14	130	O	2Q86
TC74HC131*	3-TO-8 LINE DECODER/LATCH	16	135	O	2Q86
TC74HC132*	QUAD 2-INPUT SCHMITT NAND	14	141	O	O
TC74HC133*	13-INPUT NAND GATE	16	145	O	2Q86
TC74HC137*	3-TO-8 LINE DECODER/LATCH	16	148	O	O
TC74HCT137*	3-TO-8 LINE DECODER/LATCH	16	154	O	2Q86
TC74HC138*	3-TO-8 LINE DECODER	16	160	O	O
TC74HCT138*	3-TO-8 LINE DECODER	16	165	O	O
TC74HC139*	DUAL 2-TO-4 LINE DECODER	16	171	O	O
TC74HC147*	10-TO-4 LINE PRIORITY ENCODER	16	175	O	
TC74HC148*	8-TO-3 LINE PRIORITY ENCODER	16	179	O	2Q86
TC74HC151*	8-CHANNEL MULTIPLEXER	16	184	O	O
TC74HC153*	DUAL 4-CHANNEL MULTIPLEXER	16	189	O	O
TC74HC154*	4-TO-16 LINE DECODER	24	195	O	
TC74HC155*	DUAL 2-TO-4 LINE DECODER	16	200	O	2Q86
TC74HC157*	QUAD 2-CHANNEL MULTIPLEXER	16	204	O	O
TC74HC158*	QUAD 2-CHANNEL MULTIPLEXER (INVERTING)	16	204	O	O
TC74HC160*	SYNC. DECADE COUNTER WITH ASYNC. CLEAR	16	209	O	O
TC74HC161*	SYNC. BINARY COUNTER WITH ASYNC. CLEAR	16	209	O	O
TC74HC162*	SYNC. DECADE COUNTER WITH SYNC. CLEAR	16	209	O	O
TC74HC163*	SYNC. BINARY COUNTER WITH SYNC. CLEAR	16	209	O	O
TC74HC164*	8-BIT SIPO SHIFT REGISTER	14	219	O	O
TC74HC165*	8-BIT PISO SHIFT REGISTER	16	224	O	O
TC74HC166*	8-BIT PISO SHIFT REGISTER	16	230	O	O
TC74HC173*	QUAD D-TYPE REGISTER (3-STATE)	16	236	O	O
TC74HC174*	HEX D FLIP-FLOP WITH CLEAR	16	241	O	O
TC74HC175*	QUAD D FLIP-FLOP WITH CLEAR	16	246	O	O
TC74HC181*	ARITHMETIC LOGIC UNIT	24	251	O	
TC74HC182*	LOOK AHEAD CARRY LOGIC	16	262	O	2Q86
TC74HC190*	BCD UP/DOWN COUNTER	16	269	O	O

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC191*	4-BIT BINARY UP/DOWN COUNTER	16	269	○	○
TC74HC192*	SYNC. UP/DOWN DECADE COUNTER	16	279	○	○
TC74HC193*	SYNC. UP/DOWN BINARY COUNTER	16	279	○	○
TC74HC194*	4-BIT PIPO SHIFT REGISTER	16	288	○	○
TC74HC195*	4-BIT PIPO SHIFT REGISTER	16	294	○	2Q86
TC74HC221	DUAL MONOSTABLE MULTIVIBRATOR	16	—	1Q86	2Q86
TC74HC237*	3-TO-8 LINE DECODER/LATCH	16	300	○	○
TC74HC238*	3-TO-8 LINE DECODER	16	306	○	2Q86
TC74HC240*	OCTAL BUS BUFFER (INVERTING)	20	311	○	○
TC74HCT240*	OCTAL BUS BUFFER (INVERTING)	20	316	○	
TC74HC241*	OCTAL BUS BUFFER	20	311	○	2Q86
TC74HCT241*	OCTAL BUS BUFFER	20	316	○	
TC74HC242*	QUAD BUS TRANSCEIVER	14	321	○	
TC74HC243*	QUAD BUS TRANSCEIVER	14	321	○	
TC74HC244*	OCTAL BUS BUFFER	20	311	○	○
TC74HCT244*	OCTAL BUS BUFFER	20	316	○	
TC74HC245*	OCTAL BUS TRANCEIVER	20	326	○	○
TC74HCT245*	OCTAL BUS TRANCEIVER	20	331	○	
TC74HC251*	8-CHANNEL MULTIPLEXER (3-STATE)	16	337	○	○
TC74HC253*	DUAL 4-CHANNEL MULTIPLEXER (3-STATE)	16	189	○	○
TC74HC257*	QUAD 2-CHANNEL MULTIPLEXER (3-STATE)	16	342	○	○
TC74HC258*	QUAD 2-CHANNEL MULTIPLEXER (3-STATE/INV.)	16	342	○	○
TC74HC259*	8-BIT ADDRESSABLE LATCH	16	347	○	○
TC74HC273*	OCTAL D FLIP-FLOP WITH CLEAR	20	353	○	○
TC74HC279*	QUAD S-R LATCH	16	358	○	2Q86
TC74HC280*	9-BIT PARITY GENERATOR/CHECKER	14	362	○	2Q86
TC74HC283*	4-BIT BINARY FULL ADDER	16	366	○	
TC74HC298*	QUAD 2-CHANNEL MULTIPLEXER/REGISTER	16	370	○	2Q86
TC74HC299*	8-BIT PIPO SHIFT REGISTER	20	375	○	
TC74HC323	8-BIT PIPO SHIFT REGISTER	20	—	○	

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC354*	8-CHANNEL MULTIPLEXER/REGISTER	20	383	O	2Q86
TC74HC356*	8-CHANNEL MULTIPLEXER/REGISTER	20	389	O	2Q86
TC74HC365*	HEX BUS BUFFER	16	395	O	O
TC74HC366*	HEX BUS BUFFER (INVERTING)	16	395	O	O
TC74HC367*	HEX BUS BUFFER	16	400	O	O
TC74HC368*	HEX BUS BUFFER (INVERTING)	16	400	O	O
TC74HC373*	OCTAL D-TYPE LATCH (3-STATE)	20	405	O	O
TC74HCT373*	OCTAL D-TYPE LATCH (3-STATE)	20	412	O	O
TC74HC374*	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	417	O	O
TC74HCT374*	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	424	O	O
TC74HC375*	OCTAL D-TYPE LATCH	16	430	O	O
TC74HC377	OCTAL D-TYPE LATCH FLIP-FLOP	20	—	O	
TC74HC386*	QUAD EXCLUSIVE OR GATE	14	434	O	O
TC74HC390*	DUAL DECADE COUNTER	16	438	O	O
TC74HC393*	DUAL BINARY COUNTER	14	445	O	O
TC74HC423*	DUAL MONOSTABLE MULTIVIBRATOR	16	451	O	2Q86
TC74HC533*	OCTAL D-TYPE LATCH (3-STATE/INV.)	20	405	O	O
TC74HC534*	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV.)	20	417	O	O
TC74HC540*	OCTAL BUS BUFFER	20	459	O	O
TC74HCT540*	OCTAL BUS BUFFER	20	464	O	O
TC74HC541*	OCTAL BUS BUFFER	20	459	O	O
TC74HCT541*	OCTAL BUS BUFFER	20	464	O	O
TC74HC563*	OCTAL D-TYPE LATCH (3-STATE/INV)	20	405	O	O
TC74HCT563*	OCTAL D-TYPE LATCH (3-STATE/INV)	20	469	O	
TC74HC564*	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV)	20	417	O	O
TC74HCT564*	OCTAL D-TYPE FLIP-FLOP (3-STATE/INV)	20	475	O	
TC74HC573*	OCTAL D-TYPE LATCH (3-STATE)	20	405	O	O
TC74HCT573*	OCTAL D-TYPE LATCH (3-STATE)	20	469	O	
TC74HC574*	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	417	O	O
TC74HCT574*	OCTAL D-TYPE FLIP-FLOP (3-STATE)	20	475	O	

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC590	8-BIT BINARY COUNTER/REGISTER (3-STATE)	16	—	2Q86	
TC74HC592	8-BIT REGISTER/BINARY COUNTER	16	—	2Q86	
TC74HC593	8-BIT REGISTER/BINARY COUNTER (3-STATE)	20	—	TBD	
TC74HC595*	8-BIT SHIFT REGISTER/LATCH (3-STATE)	16	481	○	
TC74HC597*	8-BIT LATCH/SHIFT REGISTER	16	488	○	○
TC74HC620*	OCTAL BUS TRANSCEIVER	20	496	○	
TC74HC623*	OCTAL BUS TRANSCEIVER	20	496	○	
TC74HC640*	OCTAL BUS TRANSCEIVER	20	326	○	○
TC74HCT640*	OCTAL BUS TRANSCEIVER	20	331	○	○
TC74HC643*	OCTAL BUS TRANSCEIVER	20	326	○	○
TC74HCT643*	OCTAL BUS TRANSCEIVER	20	331	○	○
TC74HC646*	OCTAL BUS TRANSCEIVER/REGISTER	24	501	○	
TC74HCT646*	OCTAL BUS TRANSCEIVER/REGISTER	24	509	○	
TC74HC648*	OCTAL BUS TRANSCEIVER/REGISTER	24	501	○	
TC74HCT648*	OCTAL BUS TRANSCEIVER/REGISTER	24	509	○	
TC74HC651*	OCTAL BUS TRANSCEIVER/REGISTER	24	517	○	
TC74HCT651*	OCTAL BUS TRANSCEIVER/REGISTER	24	525	○	
TC74HC652*	OCTAL BUS TRANSCEIVER/REGISTER	24	517	○	
TC74HCT652*	OCTAL BUS TRANSCEIVER/REGISTER	24	525	○	
TC74HC670*	4-WORD × 4-BIT REGISTER FILE (3-STATE)	16	534	○	
TC74HC688*	8-BIT EQUALITY COMPARATOR	20	541	○	2Q86
TC74HC690	DECADE COUNTER REGISTER (3-STATE)	20	—	○	
TC74HC691	4-BIT BINARY COUNTER REGISTER (3-STATE)	20	—	○	
TC74HC692	DECADE COUNTER REGISTER (3-STATE)	20	—	2Q86	
TC74HC693	4-BIT BINARY COUNTER REGISTER (3-STATE)	20	—	2Q86	
TC74HC696	U/D DECADE COUNTER REGISTER (3-STATE)	20	—	○	
TC74HC697	U/D 4-BIT BINARY CTR. REGISTER (3-STATE)	20	—	○	
TC74HC698	U/D DECADE COUNTER REGISTER (3-STATE)	20	—	2Q86	
TC74HC699	U/D 4-BIT BINARY CTR. REGISTER (3-STATE)	20	—	2Q86	
TC74HC4002*	DUAL 4-INPUT NOR GATE	14	545	○	2Q86

Type Number	Function	Number of Pins	Page	Sample	
				DIP	MFP
TC74HC4017*	DECADE COUNTER/DIVIDER	16	548	O	O
TC74HC4020*	14-STAGE BINARY COUNTER	16	554	O	O
TC74HC4022*	OCTAL COUNTER/DIVIDER	16	559	O	2Q86
TC74HC4024*	7-STAGE BINARY COUNTER	14	565	O	2Q86
TC74HC4028*	BCD-TO-DECIMAL DECODER	16	571	O	O
TC74HC4040*	12-STAGE BINARY COUNTER	16	575	O	O
TC74HC4049*	HEX BUFFER (INVERTING)	16	580	O	O
TC74HC4050*	HEX BUFFER	16	580	O	O
TC74HC4051	8-CHANNEL ANALOG MULTIPLEXER	16	—	TBD	
TC74HC4052	DUAL 4-CHANNEL ANALOG MULTIPLEXER	16	—	TBD	
TC74HC4053	TRIPLE 2-CHANNEL ANALOG MULTIPLEXER	16	—	TBD	
TC74HC4060*	14-STAGE BINARY COUNTER/OSCILLATOR	16	584	O	O
TC74HC4066*	QUAD BILATERAL SWITCH	14	590	O	O
TC74HC4072*	DUAL 4-INPUT OR GATE	14	595	O	2Q86
TC74HC4075*	TRIPLE 3-INPUT OR GATE	14	599	O	O
TC74HC4078*	8-INPUT OR/NOR GATE	14	603	O	
TC74HC4094*	8-BIT SIPO SHIFT REGISTER/LATCH (3-STATE)	16	607	O	O
TC74HC40102*	DUAL BCD PROGRAMMABLE DOWN COUNTER	16	615	O	
TC74HC40103*	8-BIT BINARY PROGRAMMABLE DOWN COUNTER	16	615	O	
TC74HC4511*	BCD TO 7 SEGMENT L/D/D (LED)	16	626	O	O
TC74HC4514*	4-TO-16 LINE DECODER/LATCH	24	633	O	
TC74HC4515*	4-TO-16 LINE DECODER/LATCH (INVERTING)	24	633	O	
TC74HC4518*	DUAL DECADE COUNTER	16	638	O	
TC74HC4520*	DUAL 4-BIT BINARY COUNTER	16	638	O	O
TC74HC4538*	DUAL MONOSTABLE MULTIVIBRATOR	16	645	O	O
TC74HC4543*	BCD TO 7 SEGMENT L/D/D (LCD)	16	653	O	O
TC74HCT7007*	HEX BUFFER	14	659	O	O
TC74HC7266*	QUAD EXCLUSIVE NOR GATE	14	662	O	
TC74HC7292	PROGRAMMABLE DIVIDER/TIMER	16	—	O	
TC74HC7294	PROGRAMMABLE DIVIDER/TIMER	16	—	O	

Note: 1. All DIP 24 pin products service as an enclosure of the narrow type (300 mil)

2. O: Available, TDB: 3Q86~

2. HIGH SPEED CMOS SELECTION GUIDE

FUNCTION			TYPE NUMBER
GATE BUFFER	NAND NOR AND OR INVERTER		74HC00, 74HC03, 74HC10, 74HC20, 74HC30, 74HC133 74HC02, 74HC27, 74HC4002, 74HC4078 74HC08, 74HC11, 74HC21 74HC32, 74HC4075, 74HC4072, 74HC4078 74HCU04, 74HC04, 74HCT04
	BUFFER		74HC4049 , 74HC4050 , 74HCT7007
		3-STATE	74HC125, 74HC126, 74HC240, 74HCT240, 74HC241, 74HCT241, 74HC244, 74HCT244, 74HC365, 74HC367, 74HC368, 74HC540, 74HCT540, 74HC541, 74HCT541
		BIDIRECTIONAL	74HC242, 74HC243, 74HC245, 74HCT245, 74HC620, 74HC623, 74HC640, 74HCT640, 74HC643, 74HCT643
	MULTIFUNCTION		74HC51, 74HC86, 74HC386, 74HC7266
	SCHMITT TRIGGER		74HC14, 74HC132
FLIP-FLOP	J-K, FLIP-FLOP		74HC73, 74HC76, 74HC107, 74HC109, 74HC112, 74HC113
	D FLIP-FLOP		74HC74, 74HC174, 74HC175, 74HC273, 74HC377
		3-STATE	74HC374, 74HCT374, 74HC534, 74HC564, 74HCT564, 74HC574, 74HCT574, 74HC646, 74HCT646, 74HC648, 74HCT648, 74HC651, 74HCT651, 74HC652, 74HCT652
LATCH			74HC75, 74HC77, 74HC259, 74HC279, 74HC375
		3-STATE	74HC373, 74HCT373, 74HC533, 74HC563, 74HCT563, 74HC573, 74HCT573
MULTIVIBRATOR			74HC123, 74HC221, 74HC423, 74HC4538
DECODER			74HC42, 74HC131, 74HC137, 74HCT137, 74HC138, 74HCT138, 74HC139, 74HC154, 74HC155, 74HC237, 74HC238, 74HC4028, 74HC4514, 74HC4515
		7-SEGMENT	74HC4511, 74HC4543
ENCODER			74HC147, 74HC148
REGISTER			74HC164, 74HC165, 74HC166, 74HC173, 74HC194, 74HC195, 74HC299, 74HC323, 74HC595, 74HC597, 74HC670, 74HC4094
COUNTER		BINARY	74HC161, 74HC163, 74HC191, 74HC193, 74HC393, 74HC590, 74HC592, 74HC593, 74HC691, 74HC693, 74HC697, 74HC699, 74HC4520
		DECADE	74HC160, 74HC162, 74HC190, 74HC192, 74HC390, 74HC690, 74HC692, 74HC696, 74HC698, 74HC4518
		DIVIDER	74HC4017, 74HC4020, 74HC4022, 74HC4024, 74HC4040, 74HC4060, 74HC40102, 74HC40103, 74HC7292, 74HC7294
MULTI-PLEXER		ANALOG	74HC4051, 74HC4052, 74HC4053, 74HC4066
		DIGITAL	74HC151, 74HC153, 74HC157, 74HC158, 74HC251, 74HC253 74HC257, 74HC258, 74HC298, 74HC354, 74HC356
OTHERS	COMPARATOR		74HC85, 74HC688
	ADDER		74HC283
	ALU		74HC181, 74HC182
	PARITY TREE		74HC280

3. DATA SHEETS

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC00P/F

PRELIMINARY

TC74HC00P/F QUAD 2-INPUT NAND GATE

The TC74HC00 is a high speed CMOS 2-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

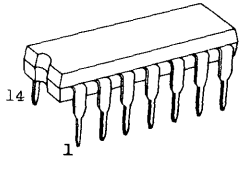
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

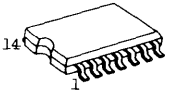
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTLL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS00

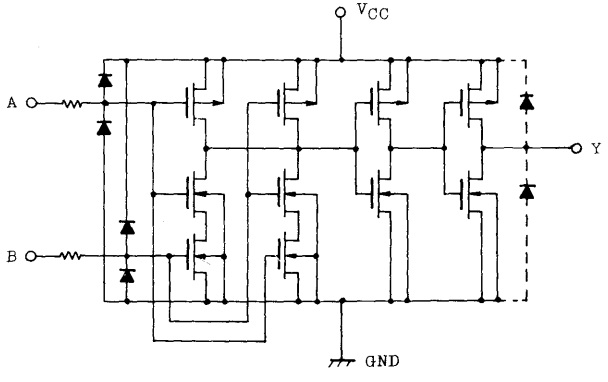


DIP14(3D14A-P)

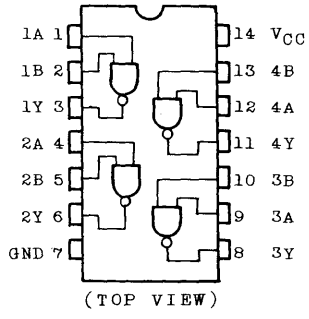


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC00P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

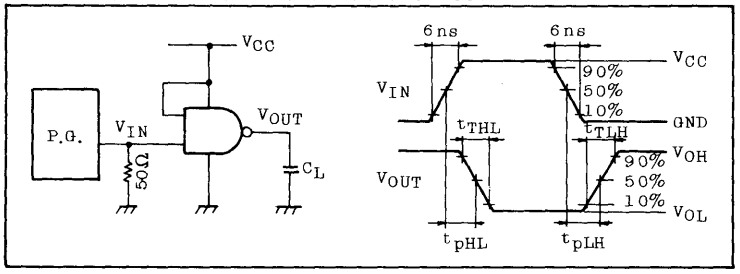
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

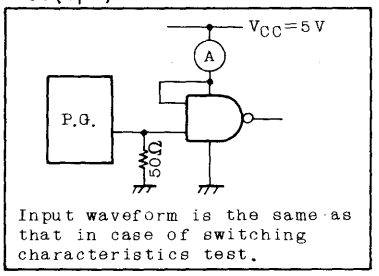
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	22	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC02P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC02P/F QUAD 2-INPUT NOR GATE

The TC74HC02 is a high speed CMOS 2-INPUT NOR GATE fabricated with silicon gate C²MOS technology.

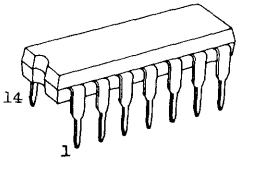
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

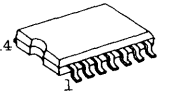
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS02

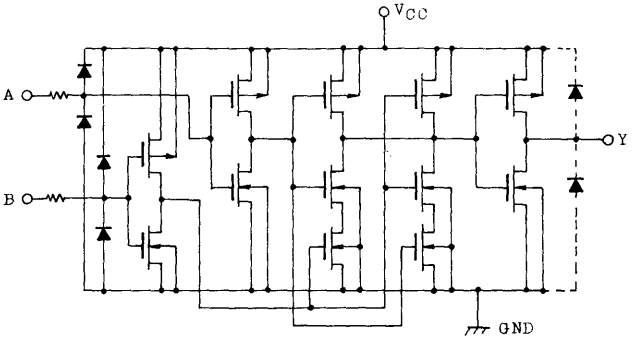


DIP14(3D14A-P)

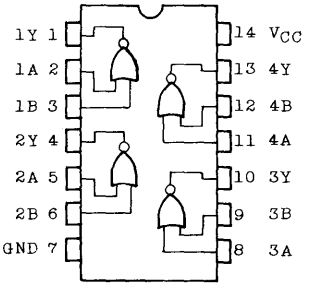


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC02P/F

DC ELECTRICAL CHARACTERISTICS

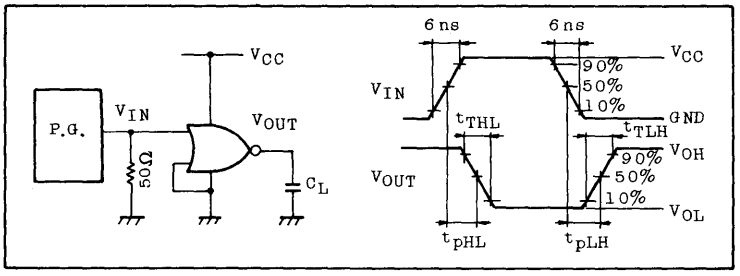
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

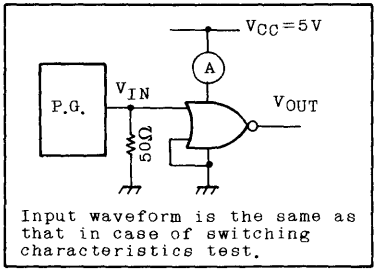
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC03P/F

PRELIMINARY

TC74HC03P/F QUAD 2-INPUT NAND GATE (OPEN DRAIN)

The TC74HC03 is a high speed CMOS QUAD 2-INPUT NAND GATE (OPEN DRAIN) fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

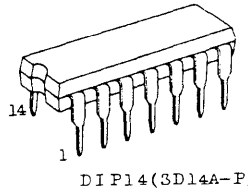
The TC74HC03 has, as its output, a high-performance MOS N-channel transistor. (OPEN-DRAIN outputs)

This device can, therefore, with a suitable pullup resistor, be used in wired-AND, LED driver and etc. application.

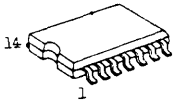
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{PLZ}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Open Drain Structure
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS03



DIP14(3D14A-P)



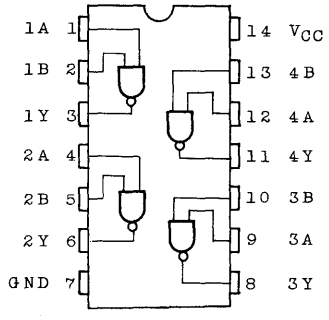
MFP14(F14G5-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

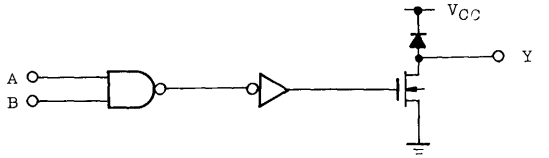
TC74HC03P/F

TRUTH TABLE

INPUTS		OUTPUT
A	B	Y
L	L	Z
L	H	Z
H	L	Z
H	H	L

Z : HIGH IMPEDANCE

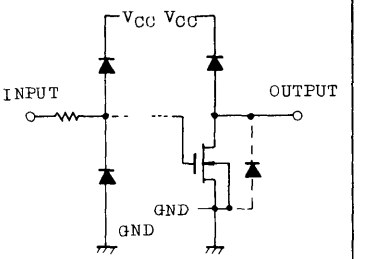
CIRCUIT DIAGRAM (PER GATE)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	A or B=V_{IL} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	←	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

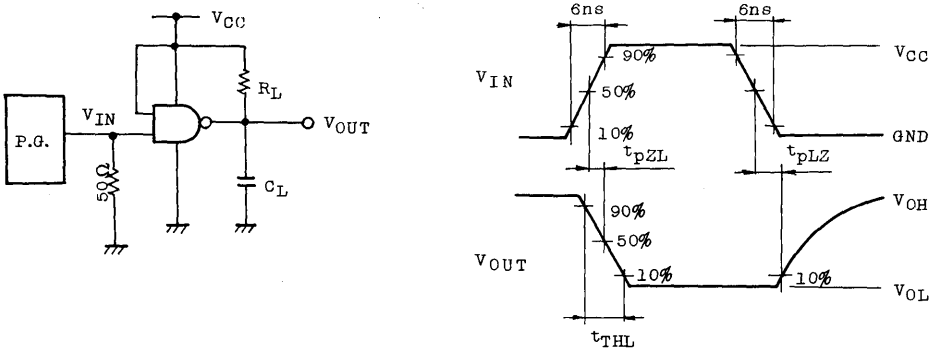
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLZ}	R_L=1kΩ	2.0	-	52	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Propagation Delay Time	t_{pZL}	R_L=1kΩ	2.0	-	52	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	5	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	17	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

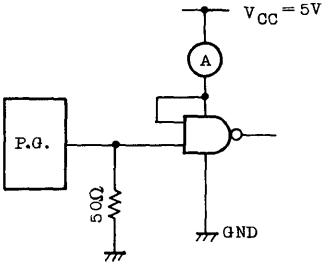
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per gate)}$$

TC74HC03P/F

SWTICHING CHARACTERISTICS TEST CIRCUIT



ICC(Opr.) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC04P/F

PRELIMINARY

TC74HC04P/F HEX INVERTER

The TC74HC04 is a high speed CMOS INVERTER fabricated with silicon gate C^2MOS technology.

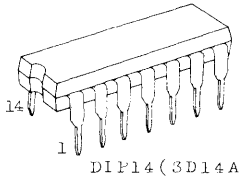
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

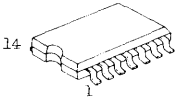
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=8ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA (Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|$=I_{OL}=4mA (Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V∿6V
- Pin and Function Compatible with 74LS04



DIP14(3D14A-P)



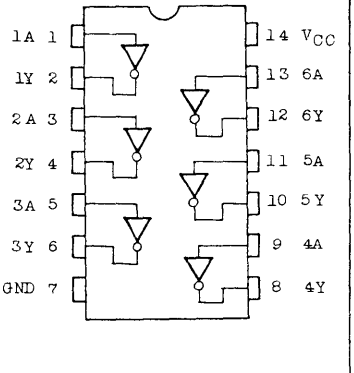
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

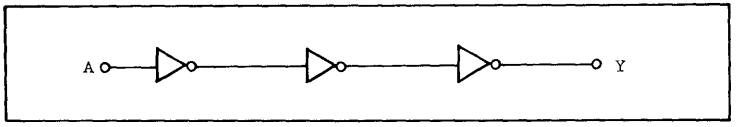
* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

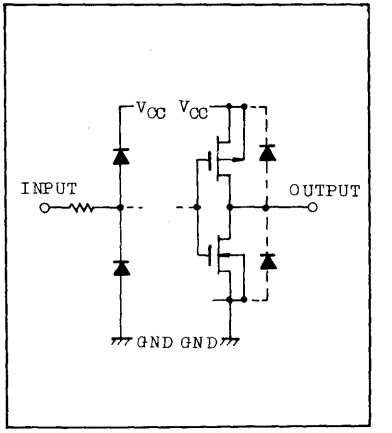


TC74HC04P/F

LOGIC DIAGRAM (per Gate)



INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

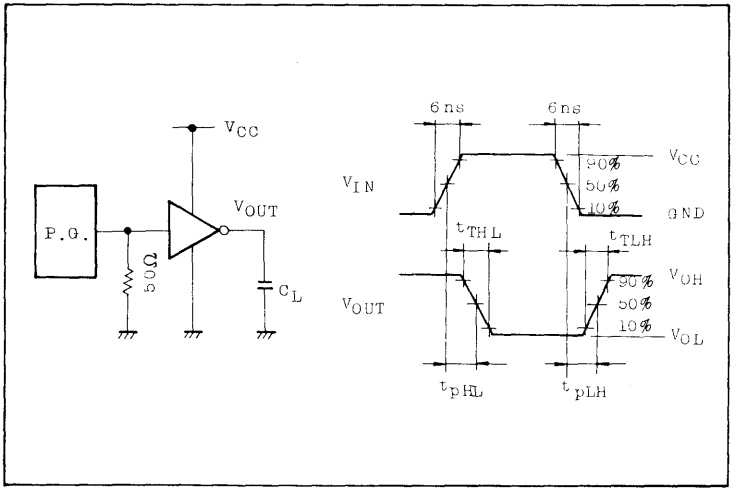
AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH} t_{PHL}		2.0	-	40	90	-	115	
			4.5	-	10	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	23	-	-	-	

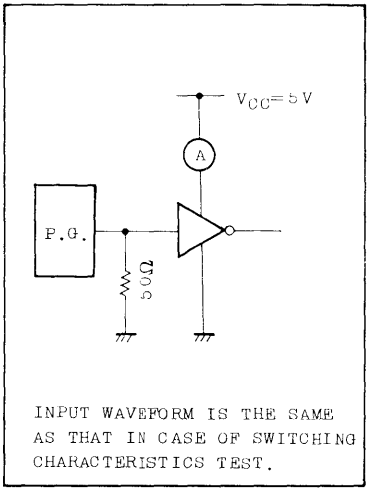
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HCT04P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HCT04P/F HEX INVERTER

The TC74HCT04 is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

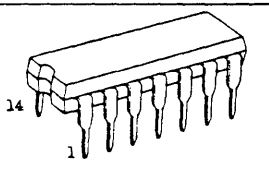
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

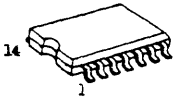
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS04



DIP14(3D14A-P)



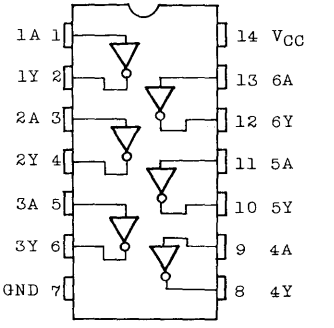
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

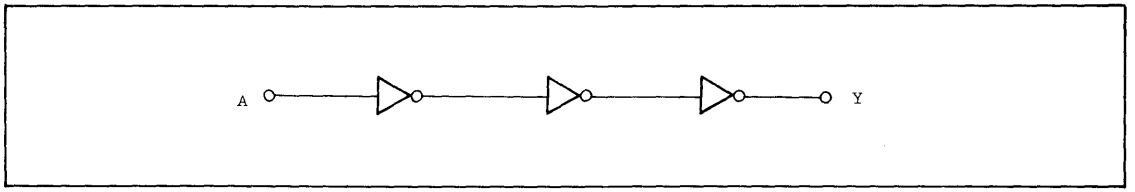
* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

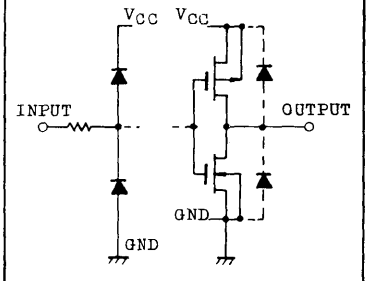
CIRCUIT DIAGRAM (per Circuit)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500 (V_{CC}=4.5V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	V
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	1.0	-	10.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

TC74HCT04P/F

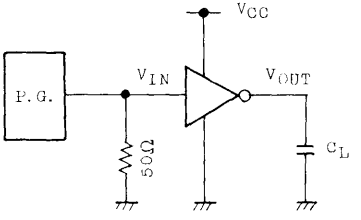
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

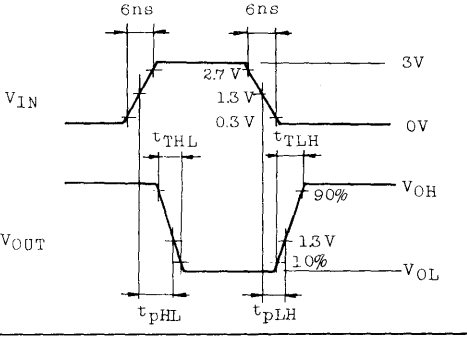
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	13	20	-	25	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	pF

Note 1: C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

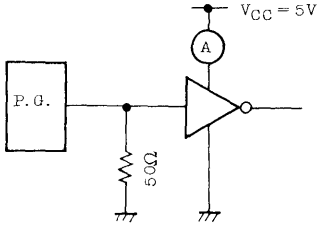
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT

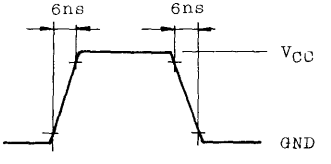




$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCU04P/F

PRELIMINARY

TC74HCU04P/F HEX INVERTER

The TC74HCU04 is a high speed CMOS INVERTER fabricated with silicon gate C²MOS technology.

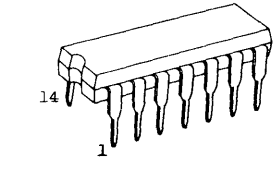
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

As the internal circuit is composed of single stage inverter, it can be applied for crystal oscillation.

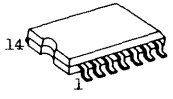
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=5ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=10% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V 6V
- Pin and Function Compatible with 74LS04

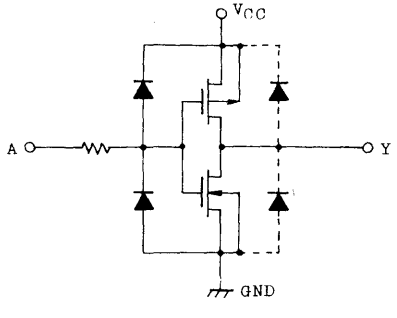


DIP14(3D14A-P)

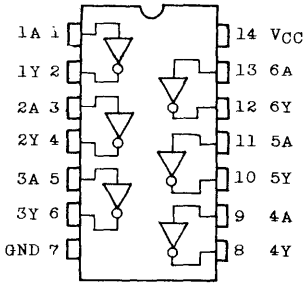


MFP14(F140B-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HCU04P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.7	-	-	1.7	-	V
			4.5	3.6	-	-	3.6	-	
			6.0	4.8	-	-	4.8	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.3	-	0.3	V
			4.5	-	-	0.9	-	0.9	
			6.0	-	-	1.2	-	1.2	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}, I_{OH}=-20μA	2.0	1.8	2.0	-	1.8	-	V
			4.5	4.0	4.5	-	4.0	-	
			6.0	5.5	5.9	-	5.5	-	
		V_{IN}=GND, I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
		V_{IN}=GND, I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

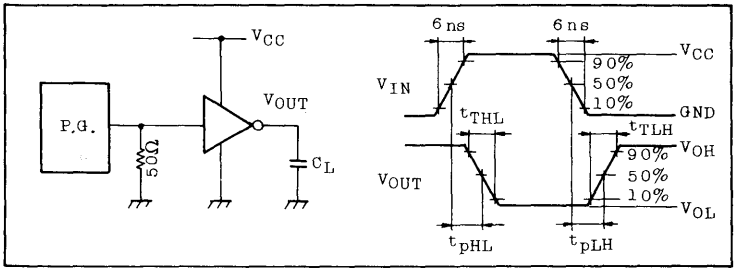
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$, I_{OL}=20μA	2.0	-	0.0	0.2	-	0.2	V
			4.5	-	0.0	0.5	-	0.5	
			6.0	-	0.1	0.5	-	0.5	
		$V_{IN}=V_{CC}$, I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
		$V_{IN}=V_{CC}$, I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

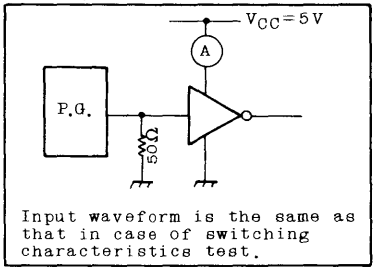
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	9	15	-	15	pF
Power Dissipation Capacitance	C_{PD}(1)			-	14	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC08P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC08P/F QUAD 2-INPUT AND GATE

The TC74HC08 is a high speed CMOS 2-INPUT AND GATE fabricated with silicon gate C²MOS technology.

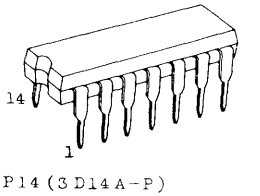
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output.

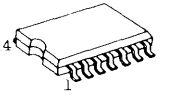
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS08

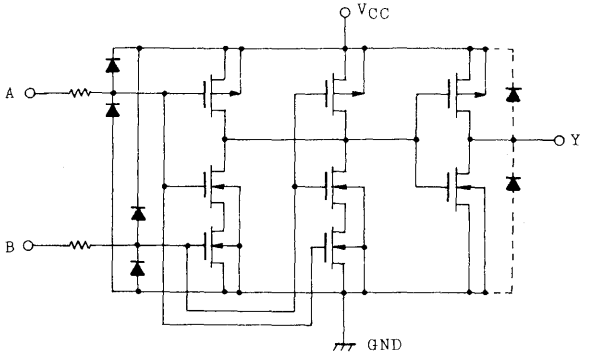


DIP14(3D14A-P)

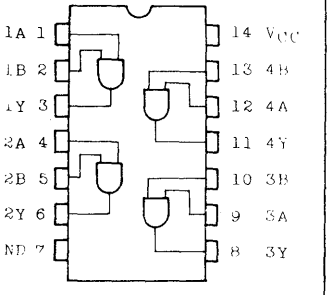


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC08P/F

DC ELECTRICAL CHARACTERISTICS

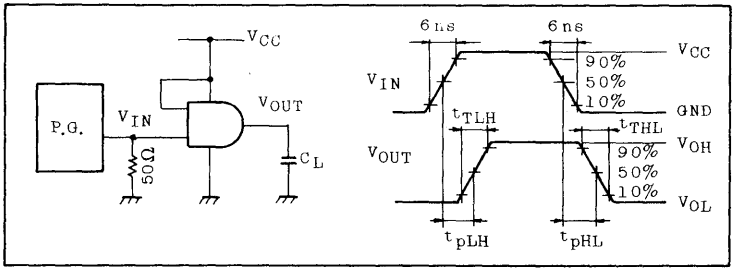
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0 1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

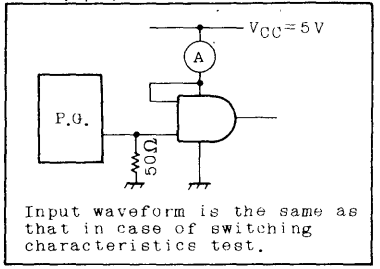
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	21	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC10P/F

PRELIMINARY

TC74HC10P/F TRIPLE 3-INPUT NAND GATE

The TC74HC10 is a high speed CMOS 3-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

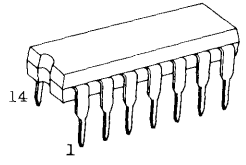
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

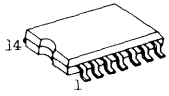
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH} ≒ t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS10

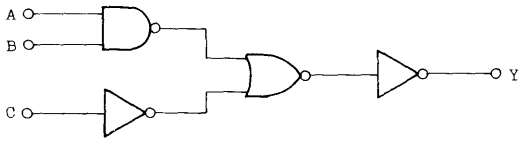


DIP14(3D14A-P)

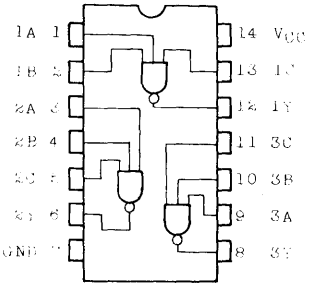


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC10P/F

ABSOLUTE MAXIMUM RATINGS

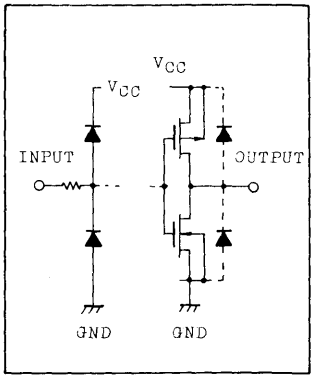
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

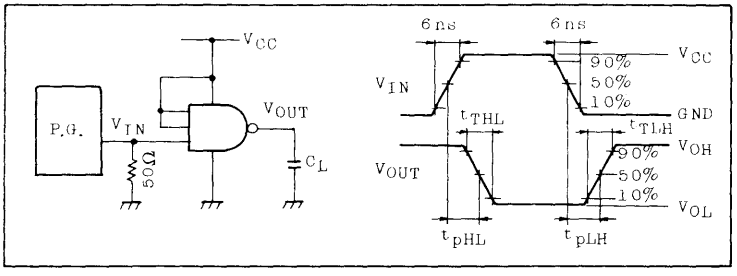
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

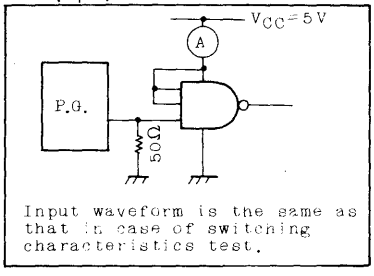
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	44	90	-	115	ns
			4.5	-	11	18	-	23	
	t_{PHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC11P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC11P/F TRIPLE 3-INPUT AND GATE

The TC74HC11 is a high speed CMOS 3-INPUT AND GATE fabricated with silicon gate C^2MOS technology.

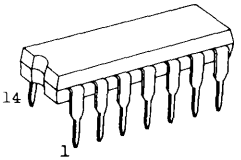
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

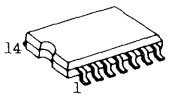
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS11

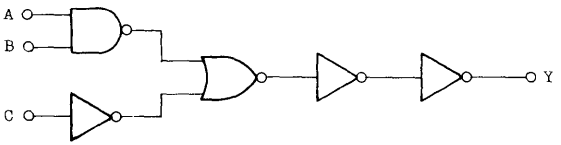


DIP14(3D14A-P)

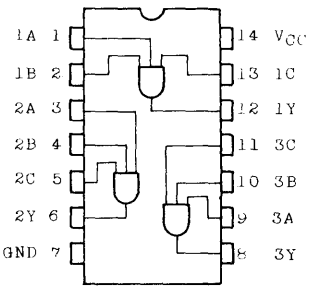


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMEMT



(TOP VIEW)

TC74HC11P/F

ABSOLUTE MAXIMUM RATINGS

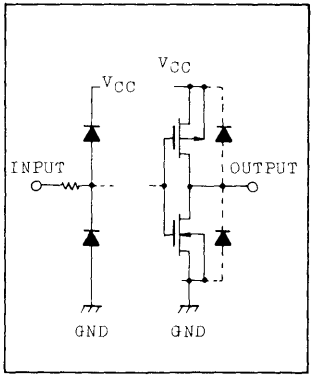
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$(V_{CC}=2.0V) $0 \sim 500$(V_{CC}=4.5V) $0 \sim 400$(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC11P/F

DC ELECTRICAL CHARACTERISTICS

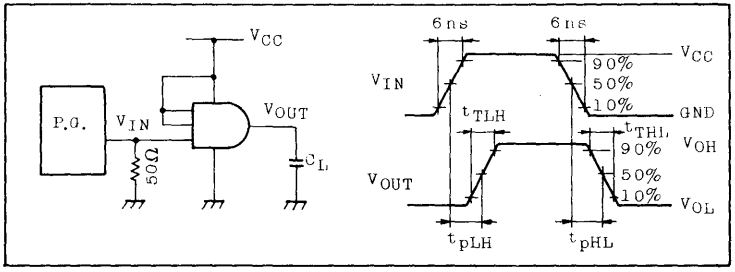
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

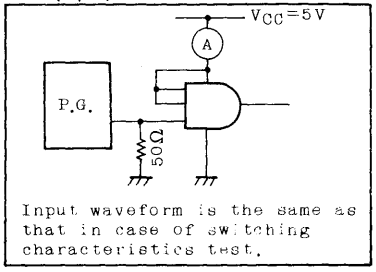
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	56	110	-	140	ns
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC14P/F

PRELIMINARY

TC74HC14P/F HEX SCHMITT INVERTER

The TC74HC14 is a high speed CMOS HEX SCHMITT INVERTER fabricated with silicon gate C²MOS technology.

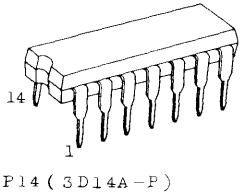
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin configuration and function are the same as those of the TC74HCU04 but all the inputs have 20% V_{CC} hysteresis and with its schmitt trigger function, it can be applicable to line receivers which will receive slow input signals.

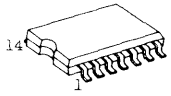
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_H=0.9V at V_{CC}=5V
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS14

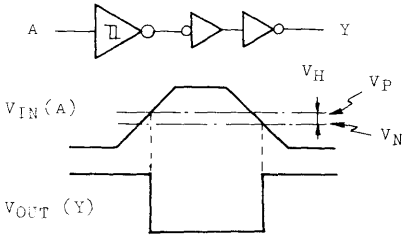


DIP14(3D14A-P)

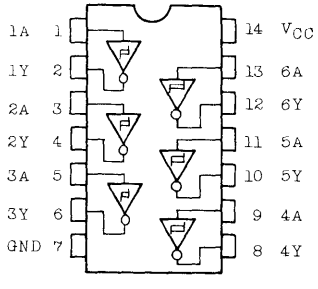


MFP14(F14GB-P)

LOGIC DIAGRAM, WAVEFORM



PIN ASSIGNMENT



(Top View)

TC74HC14P/F

ABSOLUTE MAXIMUM RATINGS

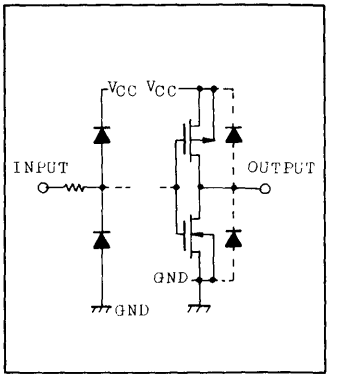
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/ 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Positive Threshold Voltage	V_P		2.0	0.8	1.25	1.5	0.8	1.5	V
			4.5	2.25	2.7	3.15	2.25	3.15	
			6.0	3.0	3.6	4.2	3.0	4.20	
Negative Threshold Voltage	V_N		2.0	0.4	0.75	1.0	0.3	1.2	V
			4.5	1.35	1.9	2.25	1.08	2.25	
			6.0	1.8	2.6	3.0	1.44	3.0	
Hysteresis Voltage	V_H		2.0	0.20	0.5	1.0	0.20	1.0	V
			4.5	0.4	0.8	1.4	0.4	1.40	
			6.0	0.6	1.0	1.7	0.6	1.70	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IL}$	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

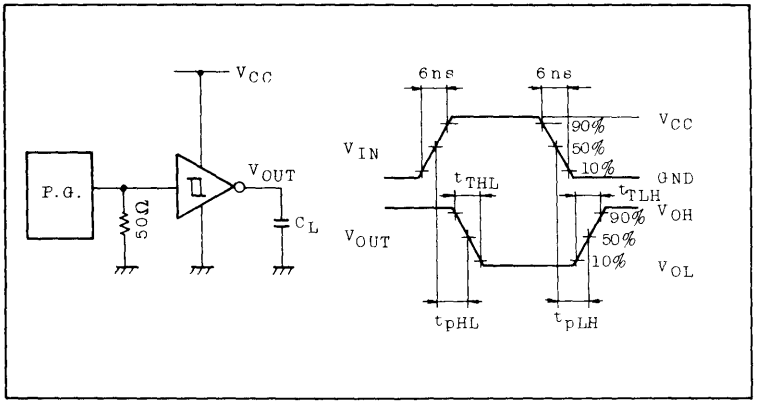
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	ns
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	31	-	-	-	

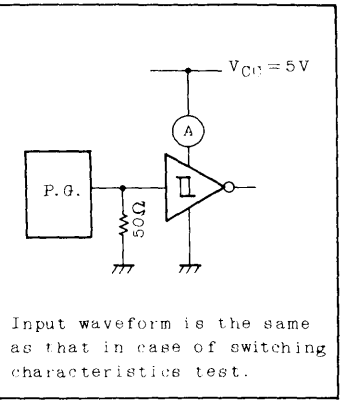
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

TC74HC14P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



C_{PD} TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC20P/F

PRELIMINARY

TC74HC20P/F DUAL 4-INPUT NAND GATE

The TC74HC20 is a high speed CMOS 4-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

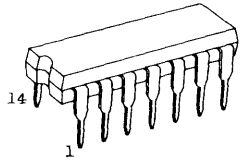
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

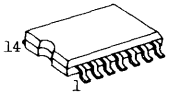
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}= 9 ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS20

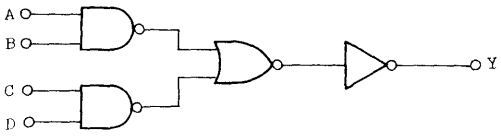


DIP14(3D14A-P)

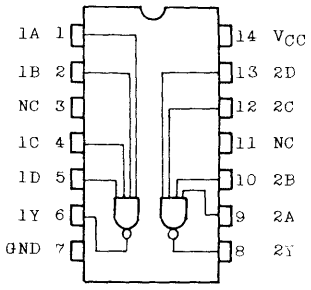


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC20P/F

ABSOLUTE MAXIMUM RATINGS

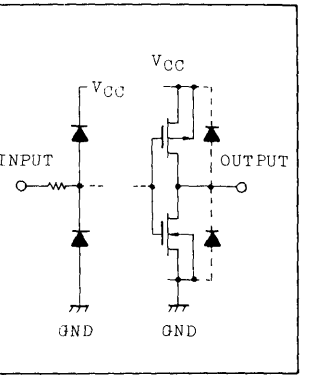
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

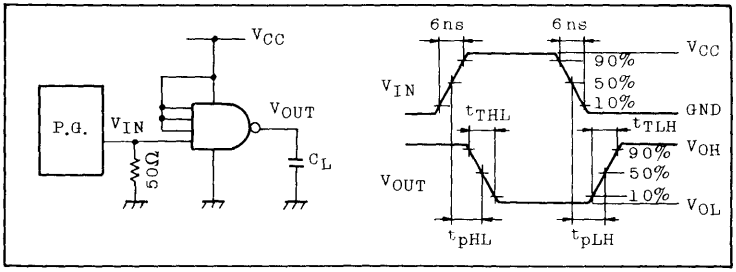
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

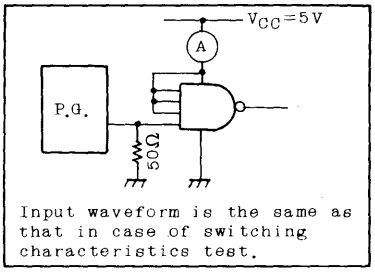
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	44	90	-	115	ns
			4.5	-	11	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC21P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC21P/F DUAL 4-INPUT AND GATE

The TC74HC21 is a high speed CMOS 4-INPUT AND GATE fabricated with silicon gate C²MOS technology.

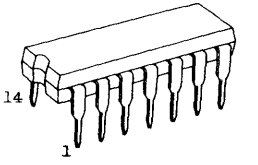
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

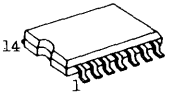
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS21

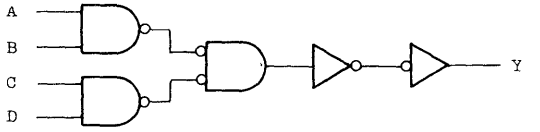


DIP14(3D14A-P)

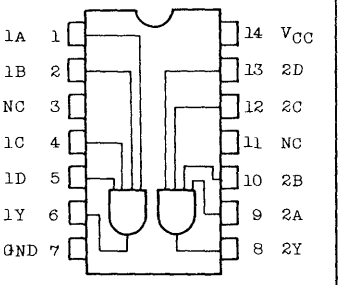


MFP14(F14GB-P)

LOGIC DIAGRAM (per Gate)



PIN ASSIGNMENT



(Top View)

TC74HC21P/F

ABSOLUTE MAXIMUM RATINGS

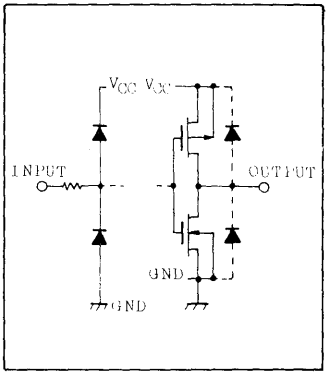
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC21P/F

DC ELECTRICAL CHARACTERISTICS

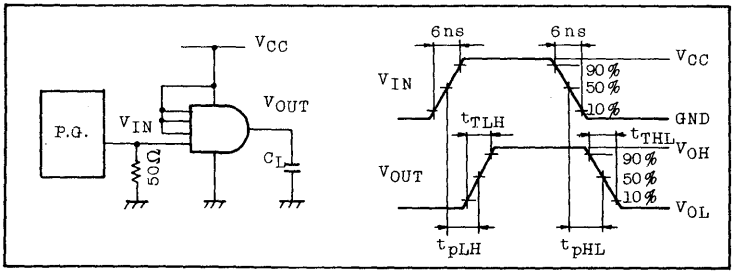
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

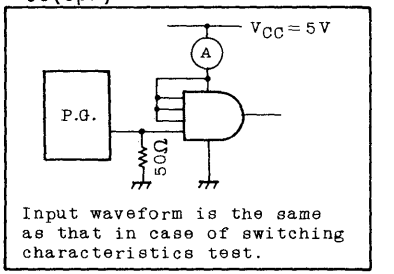
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	ns
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	29	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC27P/F

PRELIMINARY

TC74HC27P/F TRIPLE 3-INPUT NOR GATE

The TC74HC27 is a high speed CMOS 3-INPUT NOR GATE fabricated with silicon gate C^2MOS technology.

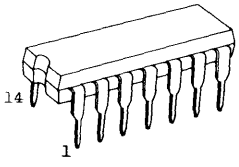
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

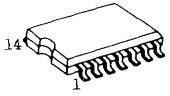
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}= 9ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS27

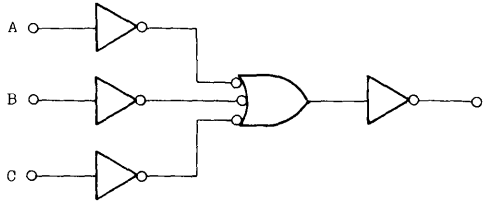


DIP14(3D14A-P)

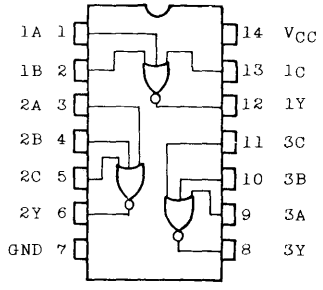


MFP14(F14GB-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC27P/F

ABSOLUTE MAXIMUM RATINGS

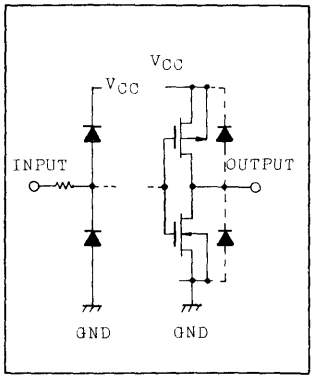
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC27P/F

DC ELECTRICAL CHARACTERISTICS

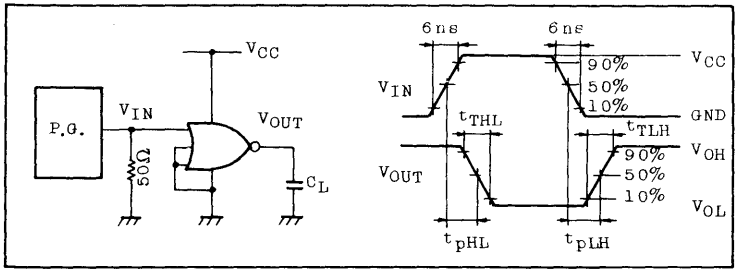
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

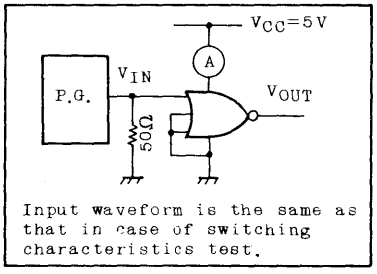
PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C				Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	44	90	-	115	ns
			4.5	-	11	18	-	23	
			6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC30P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC30P/F 8-INPUT NAND GATE

The TC74HC30 is a high speed CMOS 8-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

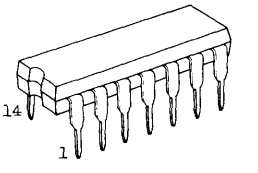
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 5 stages including buffer output, which enables high noise immunity and stable output.

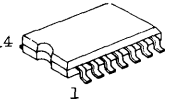
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=11ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA (Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS30.



DIP14(3D14A-P)



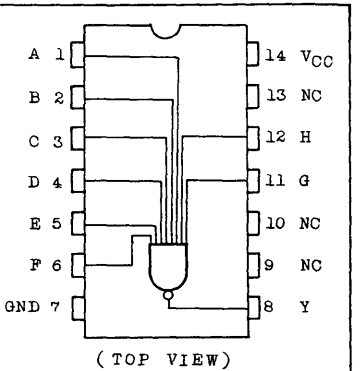
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

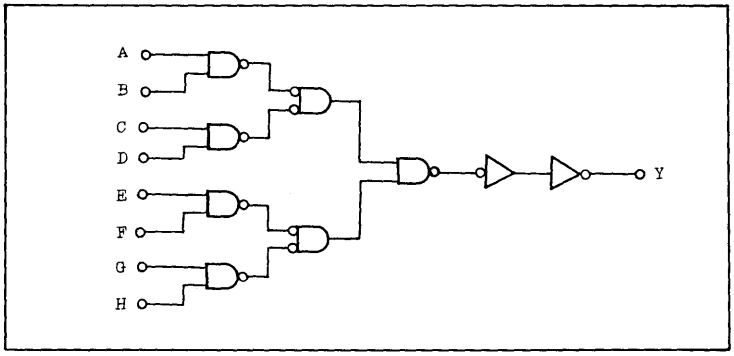


(TOP VIEW)

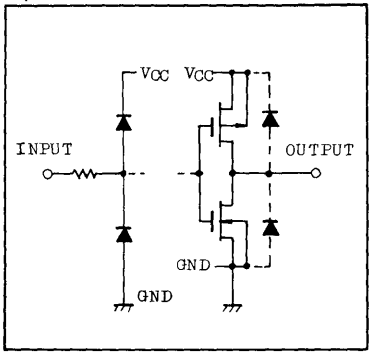
NC : No Connection

TC74HC30P/F

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC30P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

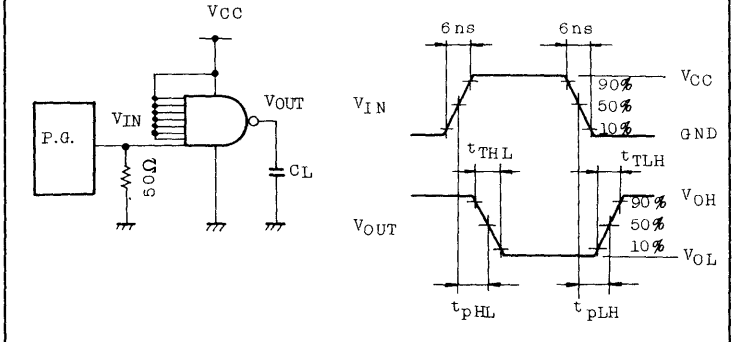
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

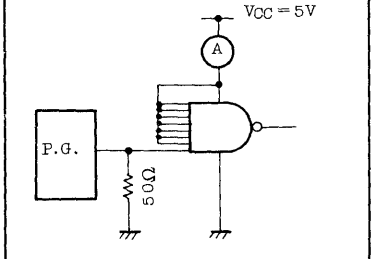
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
	t_{pHL}		6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	30	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST CIRCUIT



ICC(opr.) TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC32P/F

PRELIMINARY

TC74HC32P/F QUAD 2-INPUT OR GATE

The TC74HC32 is a high speed CMOS 2-INPUT OR GATE fabricated with silicon gate C²MOS technology.

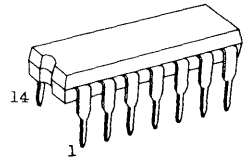
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 2 stages including buffer output, which enables high noise immunity and stable output.

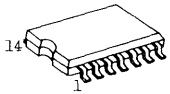
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS32

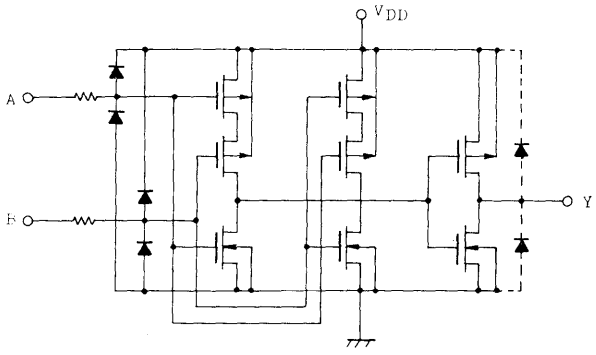


DIP14(3D14A-P)

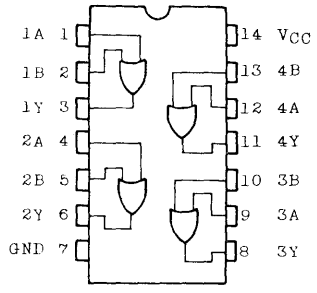


MFP14(F14GB-P)

CIRCUIT SCHEMATIC (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC32P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC32P/F

DC ELECTRICAL CHARACTERISTICS

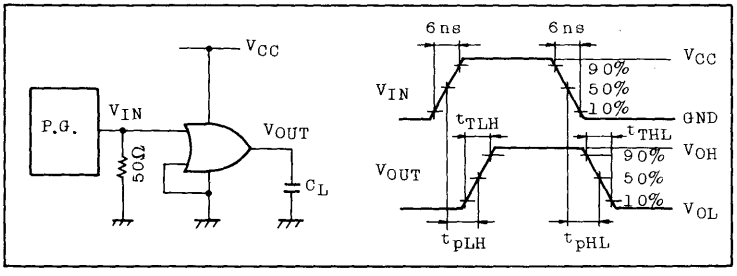
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

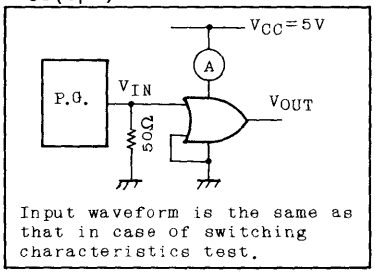
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	40	90	-	115	ns
			4.5	-	10	18	-	23	
	t_{pHL}		6.0	-	9	15	-	20	
Input Capacitance	C_{IN}			-	6	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	23	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC42P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

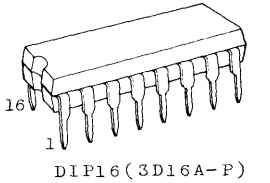
PRELIMINARY

TC74HC42P/F BCD-TO-DECIMAL DECODER

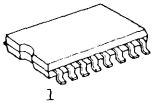
The TC74HC42 is a high speed CMOS BCD-TO-DECIMAL DECODER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining CMOS low power dissipation.
A BCD code applied to the four inputs (A - D) provides a low level at the selected one of ten decimal decoded outputs. A illegal BCD code such as eleven thru fifteen gives a high level at all outputs. This device also can be used as 3-to-8 LINE DECODER, when D input is assigned as a disable input.
This device is useful for code conversion, address decoding, memory selection, demultiplexing, or readout decoding.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V∿6V
- Pin and Function Compatible with 74LS42



DIP16(3D16A-P)



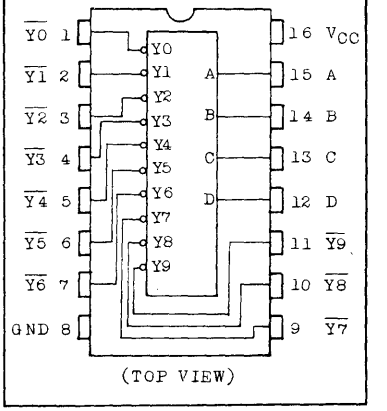
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN·ASSIGNMENT



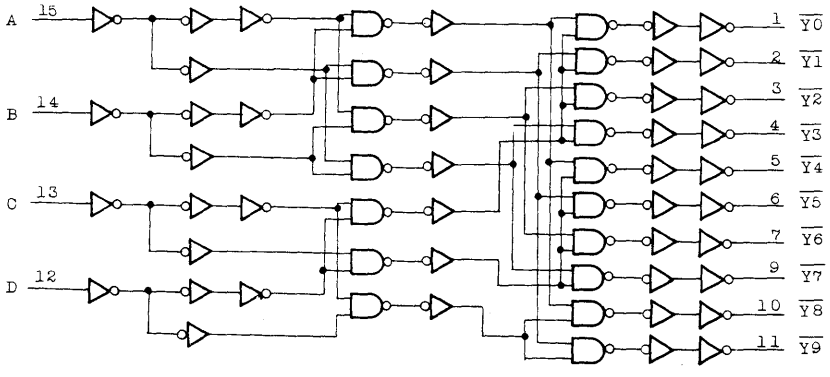
(TOP VIEW)

TC74HC42P/F

TRUTH TABLE

CODE No.	BCD INPUTS				DECIMAL OUTPUTS									
	D	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DIAGRAM

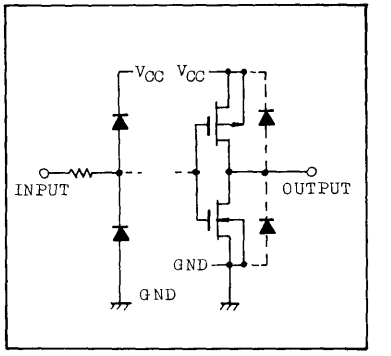


TC74HC42P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC42P/F

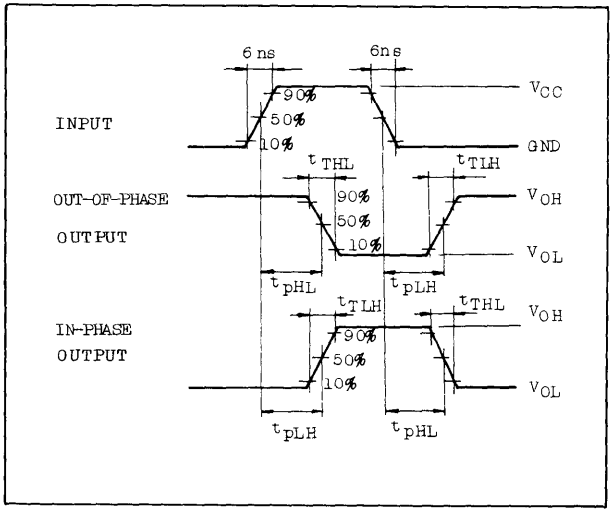
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH}		2.0	-	76	145	-	180	
	t_{PHL}		4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	67	-	-	-	

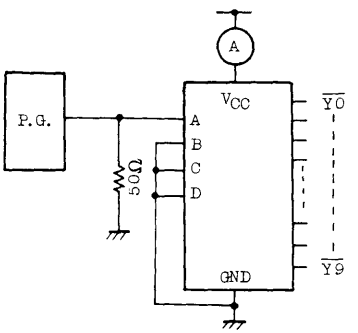
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC51P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC51P/F DUAL 2 WIDE-2 INPUT AND/OR INVERT GATE

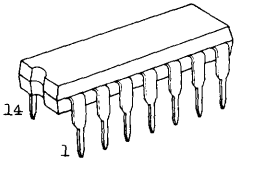
The TC74HC51 is a high speed CMOS 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE fabricated with silicon gate CMOS technology.

It acheives the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains a 2-WIDE 2-INPUT AND-OR-INVERT GATE and a 2-WIDE 3-INPUT AND-OR-INVERT GATE.

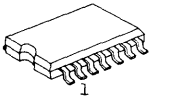
The internal circuit is composed of 3 stages (2-INPUT) or 5 stages (3-INPUT) including buffer output, which enables high noise immunity and stable output. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS51



DIP14(3D14A-P)



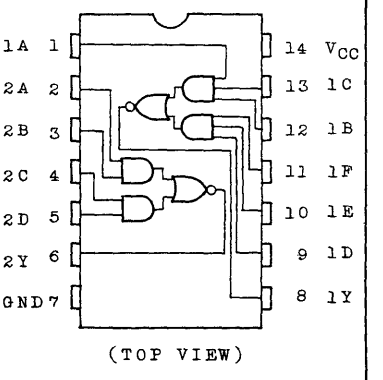
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

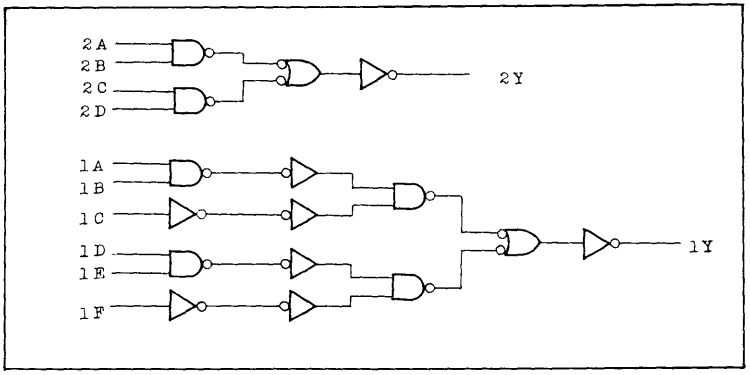
PIN ASSIGNMENT



(TOP VIEW)

TC74HC51P/F

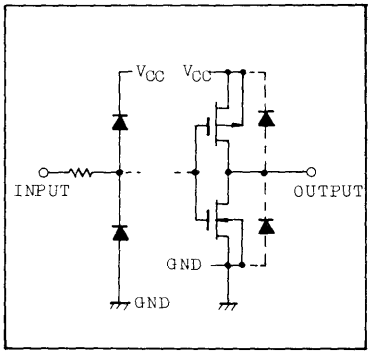
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC51P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

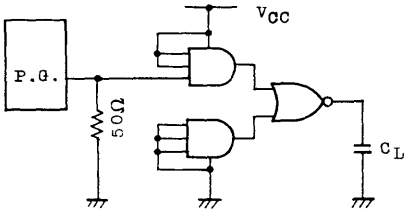
AC ELECTRICAL CAHRACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

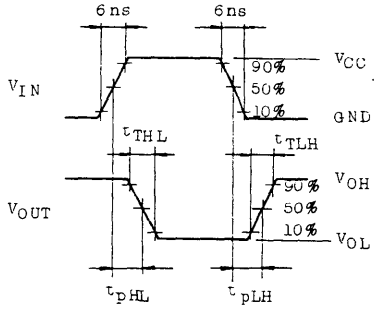
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40∿85°C MIN.	-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
	t_{pHL}		6.0	-	11	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	33	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

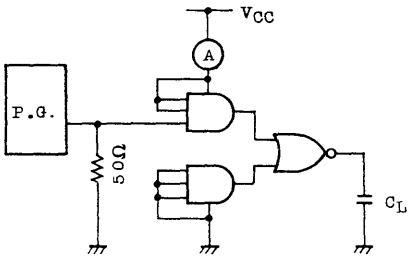
$$I_{DD(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per Gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT





$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC73P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC73P DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC73 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

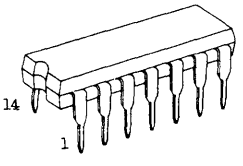
In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=55MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=2μA(Max.) (Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS73



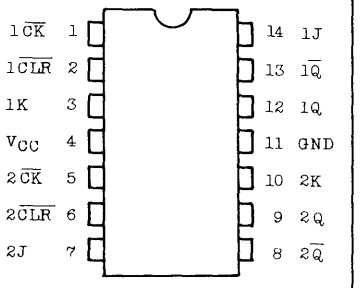
DIP14(3D14A P)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	-
H	H	L	↓	H	L	-
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X: Don't care

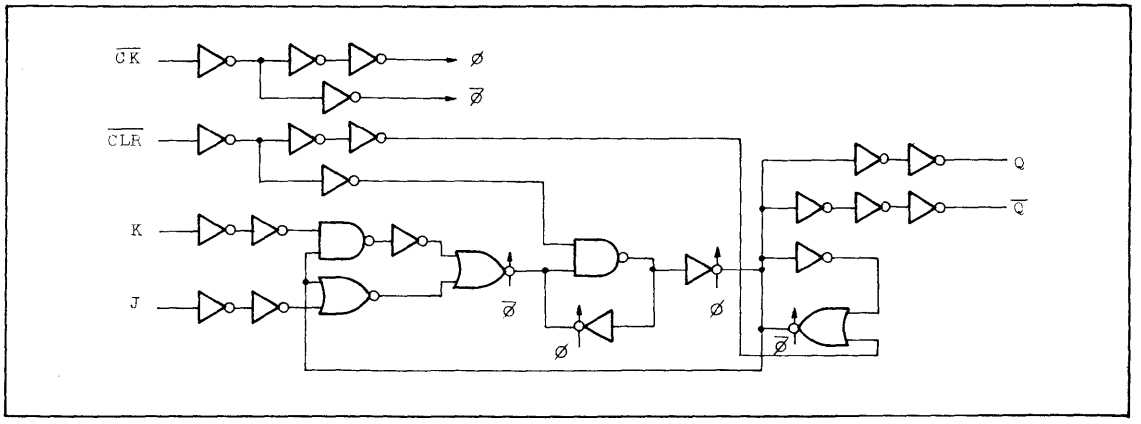
PIN ASSIGNMENT



(Top View)

TC74HC73P

LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)

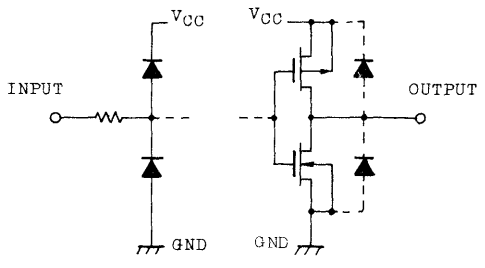


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC73P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

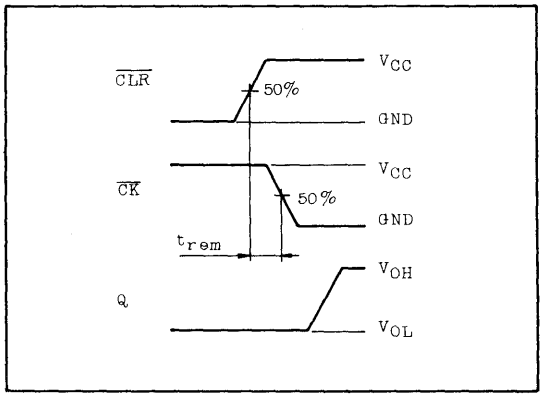
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	52	-	24	-	
			6.0	35	61	-	28	-	
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	42	-	-	-	

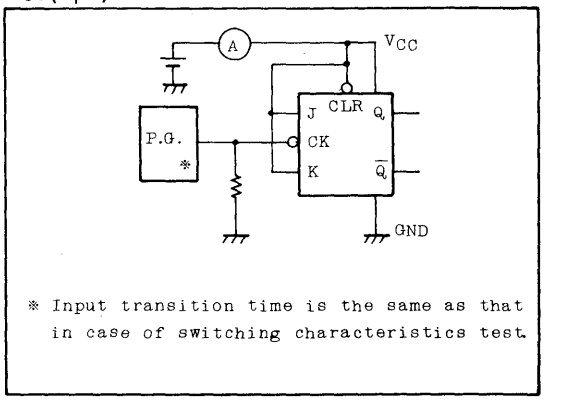
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per FF)

TC74HC73P

SWITCHING CHARACTERISTICS TEST WAVEFORM

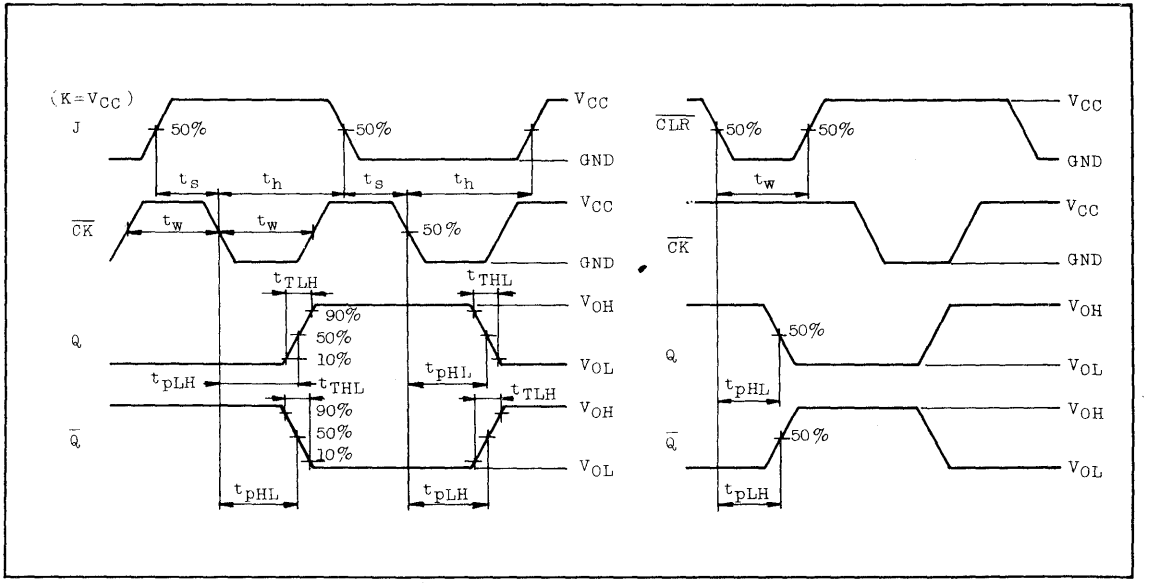


ICC(opr) TEST CIRCUIT



* Input transition time is the same as that in case of switching characteristics test.

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC74P/F

PRELIMINARY

TC74HC74P/F DUAL D FLIP FLOP WITH PRESET AND CLEAR

The TC74HC74 is a high speed CMOS DUAL D FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

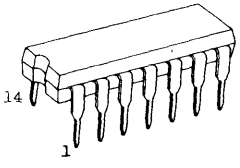
Signal given D INPUT is transferred to Q OUTPUT during the positive going transition of the clock pulse.

CLEAR and PRESET are independent of the clock and accomplished by "L" level at the appropriate input.

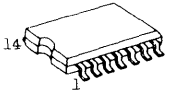
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS74



DIP14(3D14A-P)



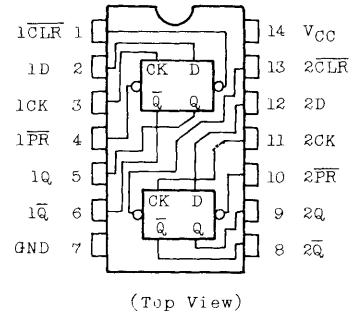
MFP14(F14GB-P)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	-
H	H	L	↑	L	H	-
H	H	H	↑	H	L	-
H	H	X	↓	Qn	$\overline{Q}$n	NO CHANGE

X: Don't care

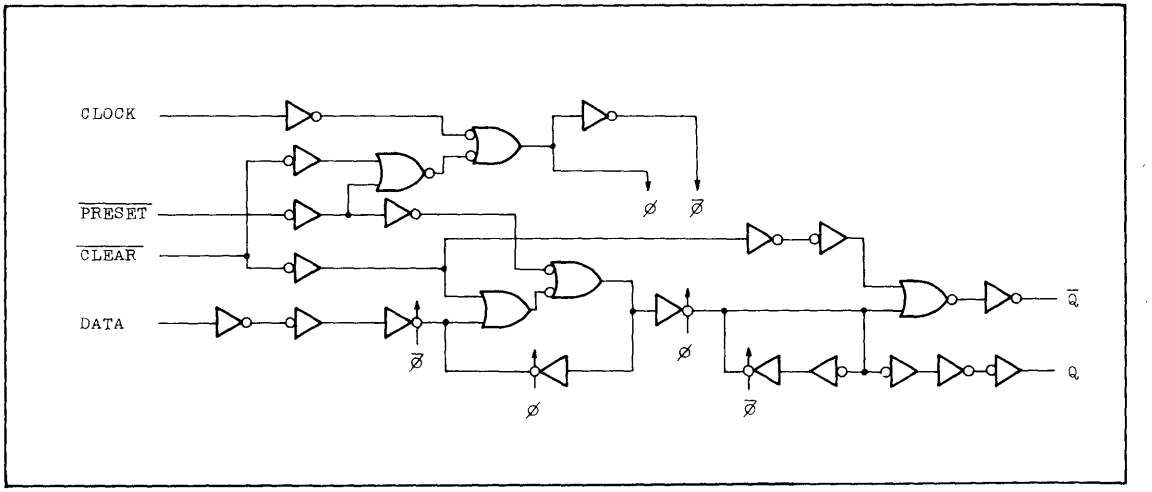
PIN ASSIGNMENT



(Top View)

TC74HC74P/F

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

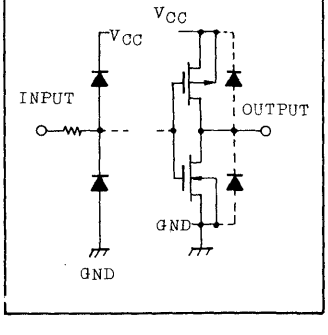
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	ns
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	104	205	-	255	ns
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	

TC74HC74P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

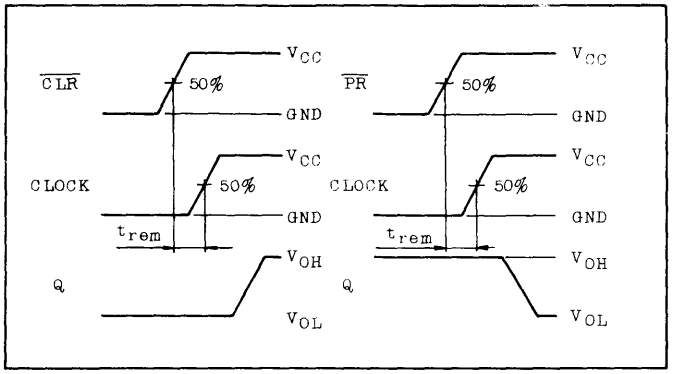
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	27	49	-	22	-	
			6.0	32	58	-	26	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	45	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	53	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

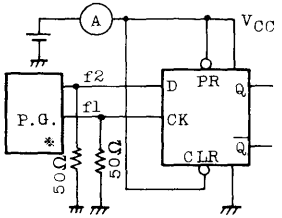
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \text{ (per FF)}$$

TC74HC74P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

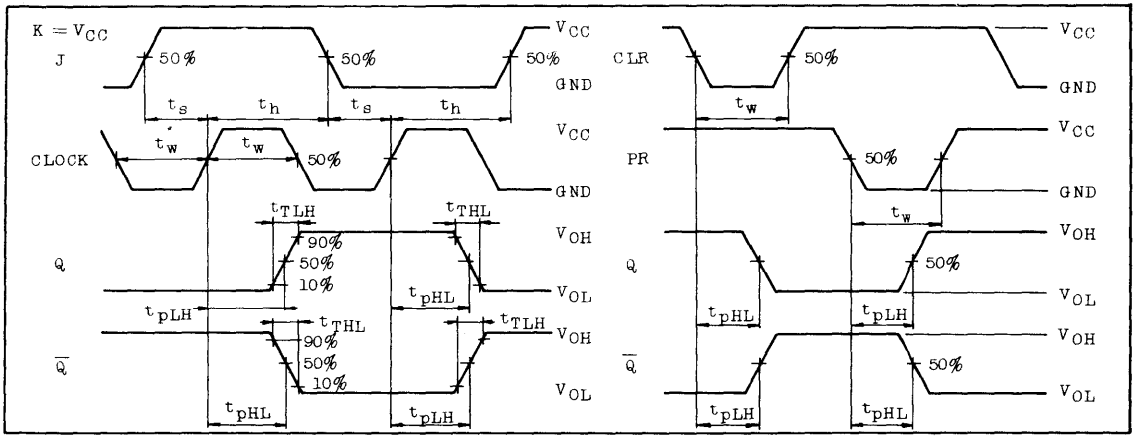


$I_{CC(opr)}$ TEST CIRCUIT



※ Input transient time is the same as that in case of switching characteristics test. f2 = f1/2

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC75P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

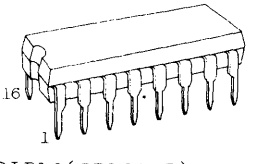
TC74HC75P/F 4-BIT D-TYPE LATCH

The TC74HC75 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C²MOS technology.

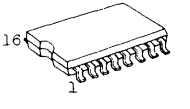
It achieves the high speed operation similar to equivalent LS TTL while maintaining the CMOS low power dissipation.

It contains two groups of 2-bit latches controled by a enable input (G1·2 or G3·4). And those two latch groups can be used in the different circuits.

Each latch has Q and $\overline{Q}$ outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at a time is retained at the outputs. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

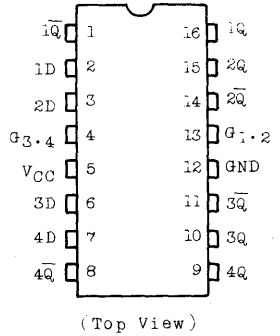


MFP16(F16GC-P)

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{HIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS75

PIN ASSIGNMENT



(Top View)

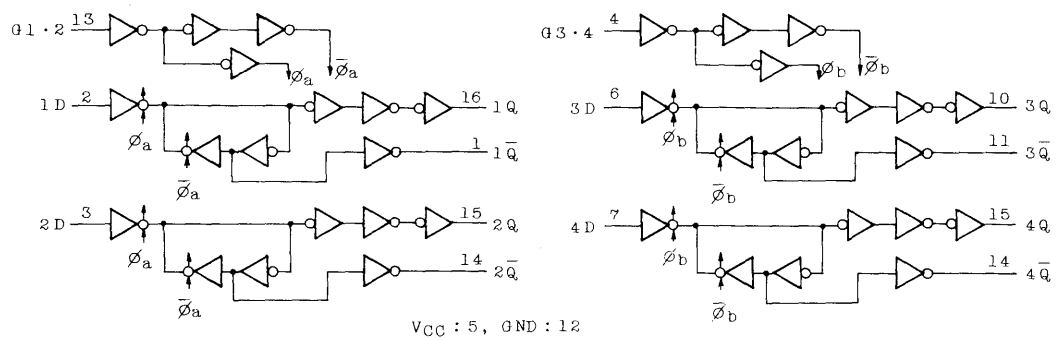
TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\overline{Q}$	
L	H	L	H	-
H	H	H	L	-
X	L	Q_n	$\overline{Q}_n$	LATCH

X : Don't care

TC74HC75P/F

LOGIC DIAGRAM

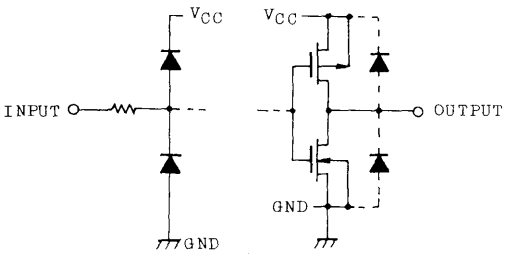


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC75P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

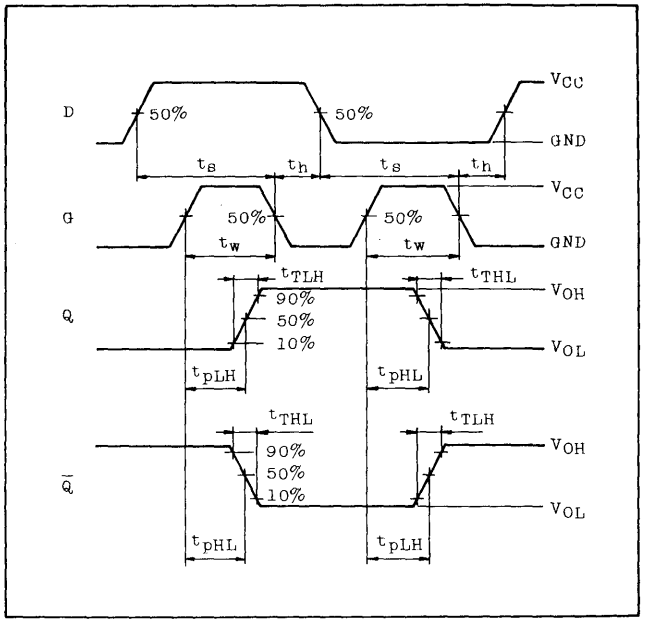
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Minimum Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	4	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	48	-	-	-	

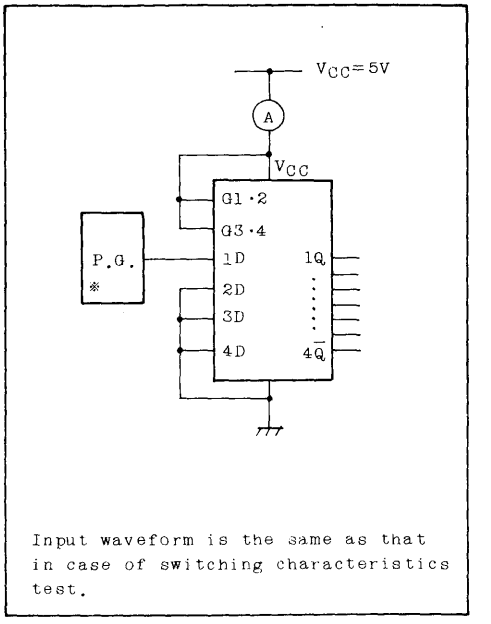
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}/4$ (per Latch)

TC74HC75P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC76P/F

PRELIMINARY

TC74HC76P/F DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC76 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C²MOS technology.

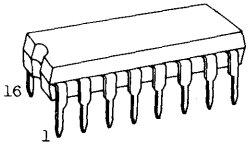
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

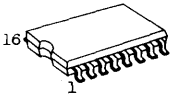
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS76.



DIP16(3D16A-P)



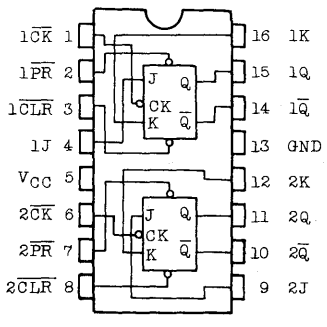
MFP16(F16GC-P)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: Don't care

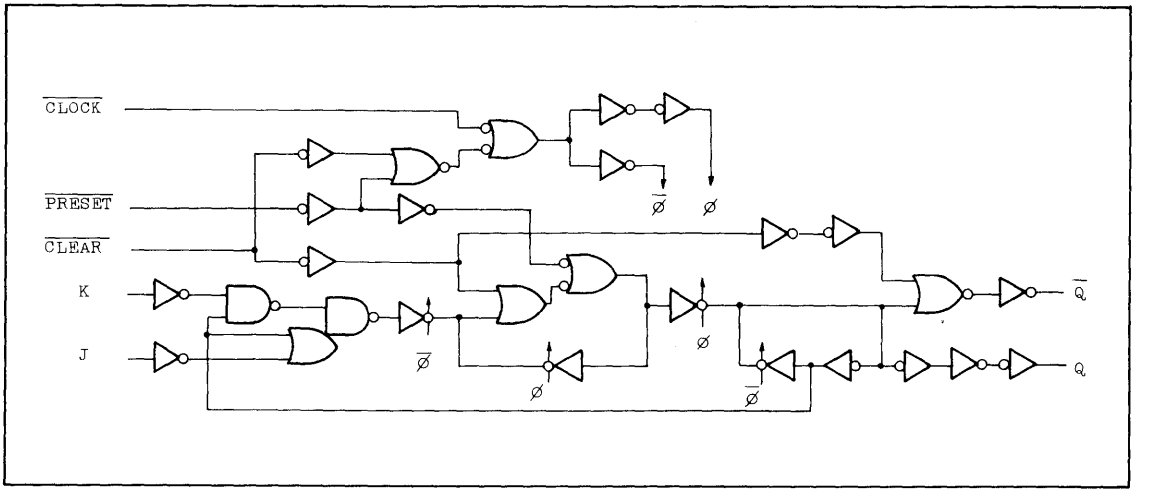
PIN ASSIGNMENT



(TOP VIEW)

TC74HC76P/F

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

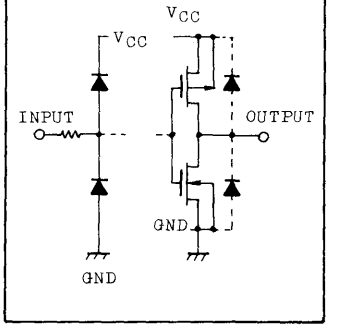
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	ns
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	

TC74HC76P/F

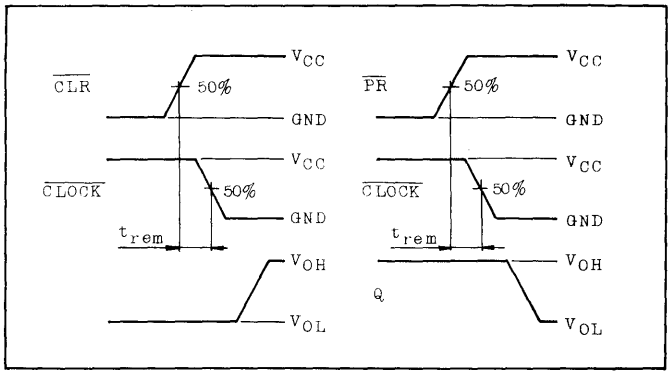
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	35	75	-	95	
			4.5	-	9	20	-	19	
			6.0	-	8	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

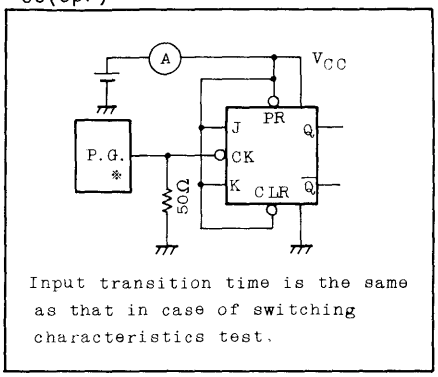
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per FF)

TC74HC76P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

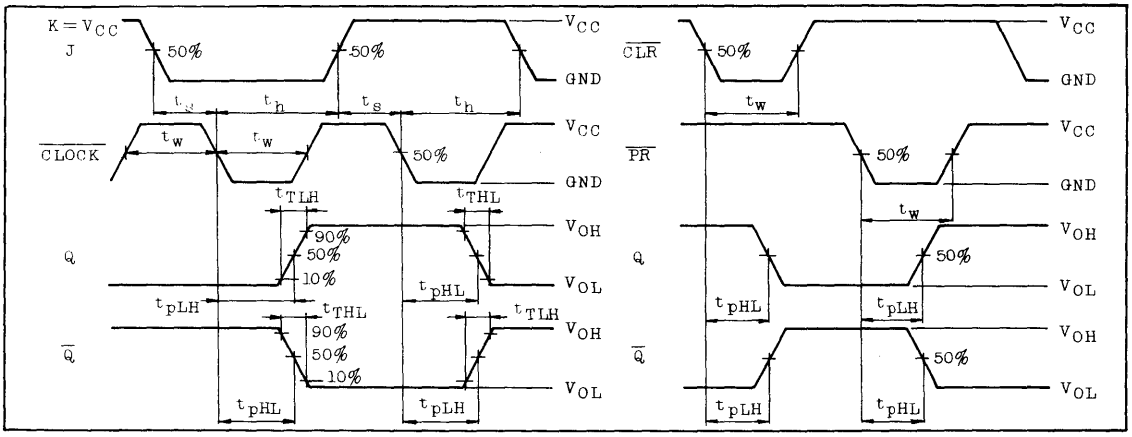


$I_{CC(opr)}$ TEST CIRCUIT



Input transition time is the same as that in case of switching characteristics test.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC77P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC77P 4-BIT D-TYPE LATCH

The TC74HC77P is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate CMOS technology.

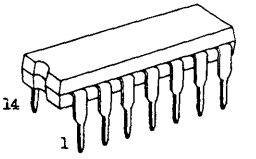
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

It contains two groups of 2-bit latches controled by a enable input (G1·2 or G3·4). And these two latch groups can be used in the different circuits.

The data applied to the data inputs (1D, 2D or 3D, 4D) are transfered to the Q outputs (1Q, 2Q or 3Q, 4Q) respectively when the enable input (G1·2 or G3·4) is taken high and the Q outputs will follow the data inputs as long as the enable input is kept high.

When the enable input is taken low, the information data applied to the data inputs at a time are retained at the Q outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

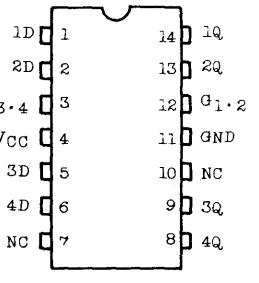


DIP14(3D14A-P)

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS77

PIN ASSIGNMENT

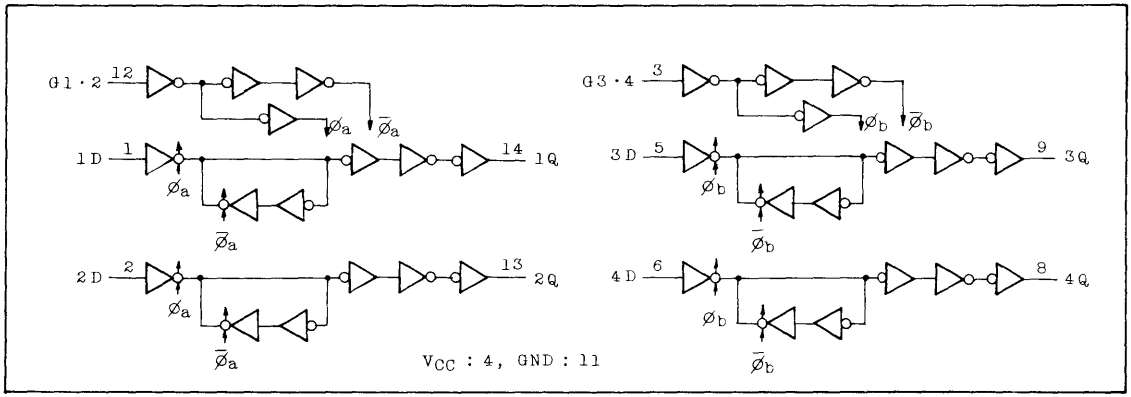


(Top View)

NC : No Connection

TC74HC77P

LOGIC DIAGRAM

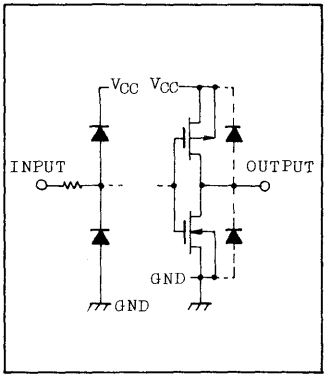


TRUTH TABLE

INPUTS		OUTPUT	FUNCTION
D	G	Q	
L	H	L	-
H	H	H	-
X	L	Q_n	Latch

X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C
shall be applied until 300mW.

TC74HC77P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IN}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

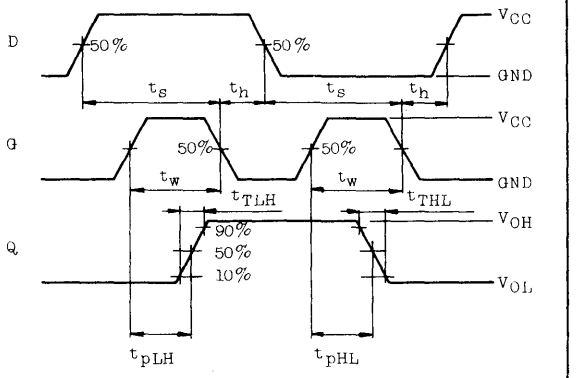
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q)	t_{pLH} t_{pHL}		2.0	-	75	145	-	180	
			4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Minimum Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	4	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	27	-	-	-	

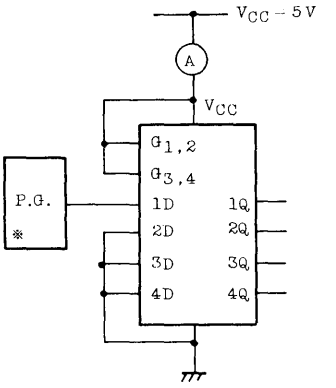
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Latch)

TC74HC77P

AC CHARACTERISTICS TEST WAVEFORM



I_{CC}(opr) TEST CIRCUIT



※ Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC85P/F

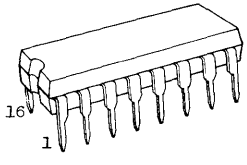
PRELIMINARY

TC74HC85P/F 4-BIT MAGNITUDE COMPARATOR

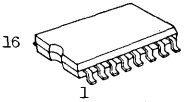
The TC74HC85 is a high speed CMOS 4-BIT MAGNITUDE COMPARATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This comparator compares two 4-bit words and provides a high voltage level on one of the A > Bout, A = Bout and A < Bout output. The comparing bit number is easily expanded by cascading several devices as shown at the typical application. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=24ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS85



DIP16(3D16A-P)



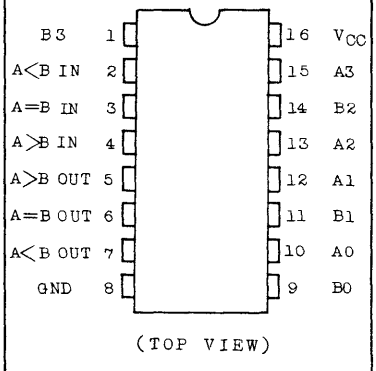
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

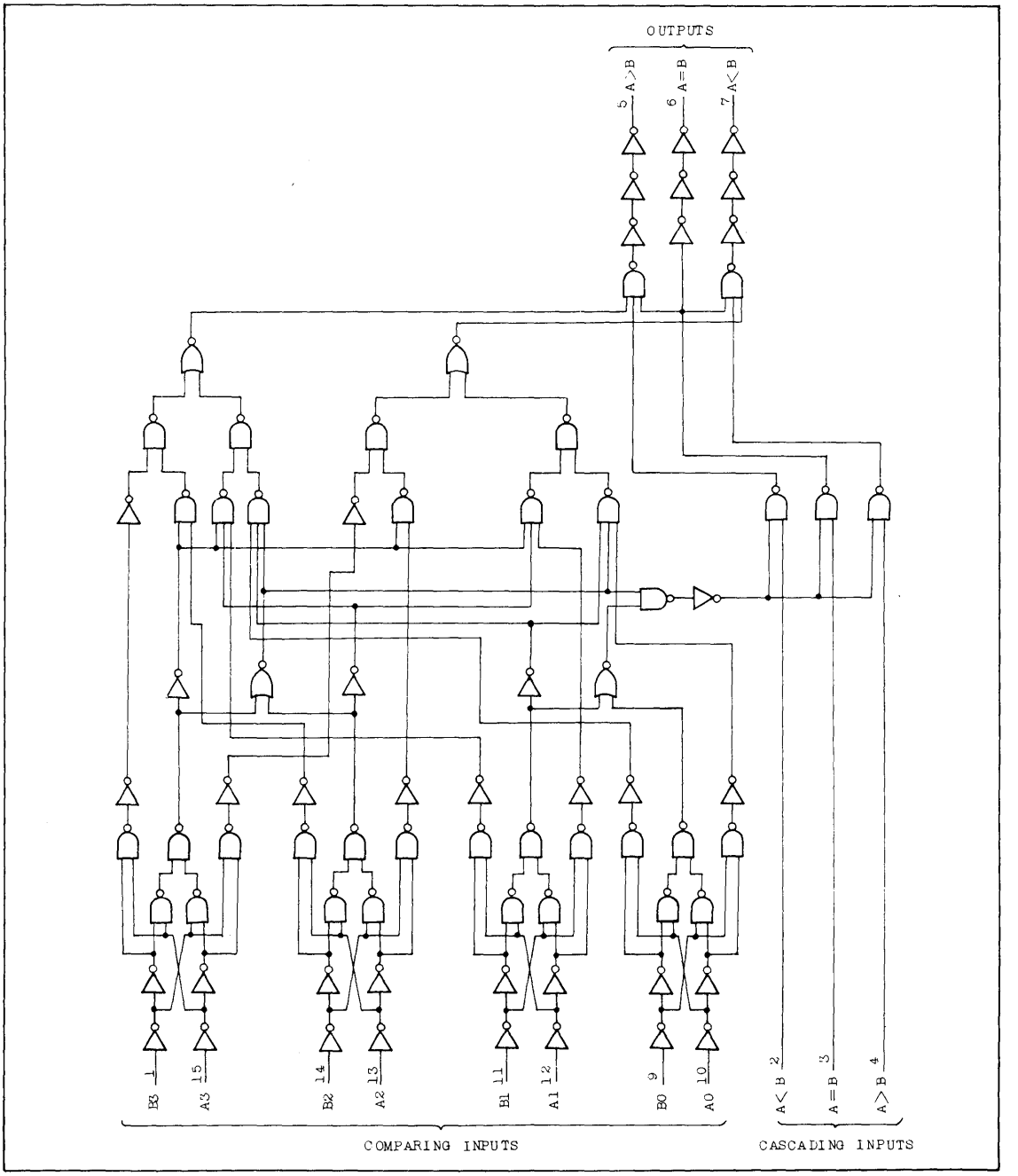
PIN ASSIGNMENT



(TOP VIEW)

TC74HC85P/F

LOGIC DIAGRAM



TC74HC85P/F

TRUTH TABLE

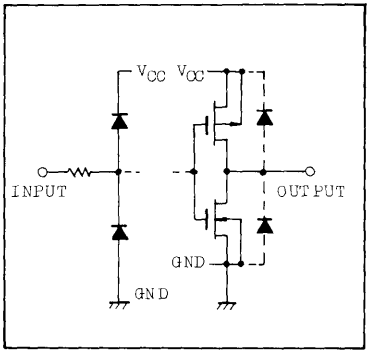
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
				A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3 , A2=B2 , A1=B1 , A0=B0				L	L	L	H	H	L
				X	X	H	L	L	H
				L	H	L	L	H	L
				H	L	L	H	L	L
				H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3<B3	X	X	X	X	X	X	L	H	L

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=−40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	−	−	1.5	−	V
			4.5	3.15	−	−	3.15	−	
			6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}		2.0	−	−	0.5	−	0.5	V
			4.5	−	−	1.35	−	1.35	
			6.0	−	−	1.8	−	1.8	

TC74HC85P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6ns)

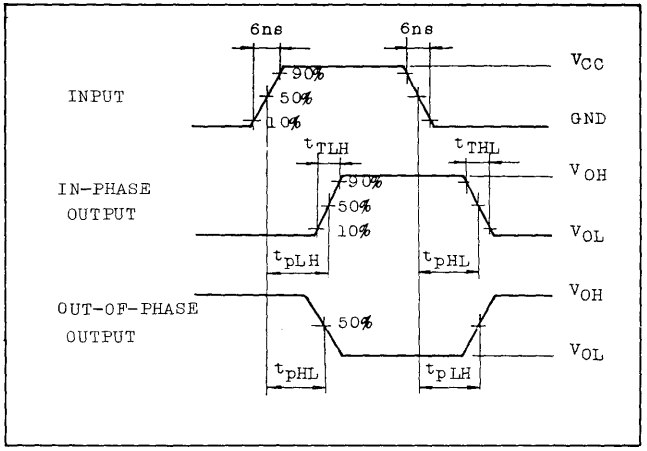
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40∿85°C MIN.	-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, B - OUT)	t_{PLH} t_{PHL}		2.0	-	112	230	-	290	
			4.5	-	28	46	-	58	
			6.0	-	24	39	-	49	
Propagation Delay Time (CASCADE - OUT)	t_{PLH} t_{PHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

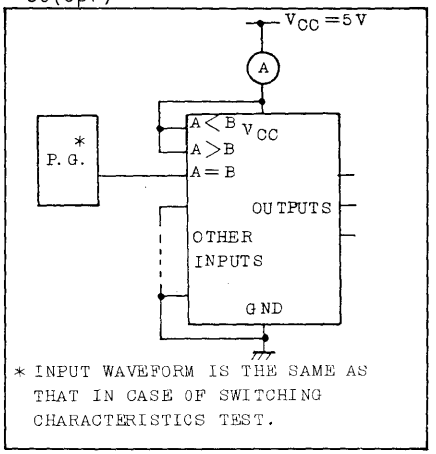
$$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC85P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



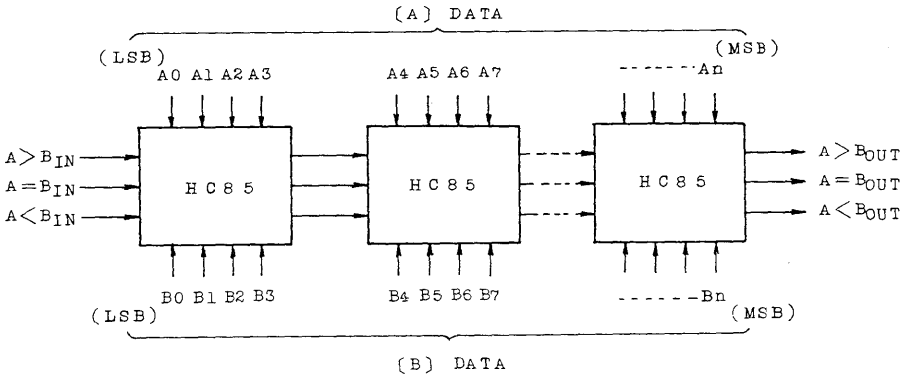
ICC(opr) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

N-BIT CASCADE CONNECTION



COMPARING INPUTS	CASCADING INPUTS			OUTPUTS		
	A>B	A=B	A<B	A>B	A=B	A<B
(A) > (B)	X	X	X	H	L	L
(A) = (B)	H	L	L	H	L	L
	X	H	X	L	H	L
	L	L	H	L	L	H
(A) < (B)	X	X	X	L	L	H

X : DON'T CARE

TC74HC86P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC86P/F QUAD EXCLUSIVE OR GATE

The TC74HC86 is a high speed CMOS QUAD EXCLUSIVE OR GATE fabricated with silicon gate C²MOS technology.

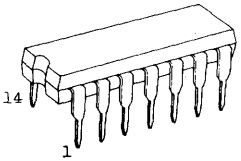
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Input and output buffer are installed, which enables high noise immunity and stable output.

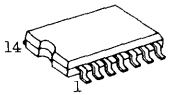
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V～6V
- Pin and Function Compatible with 74LS86

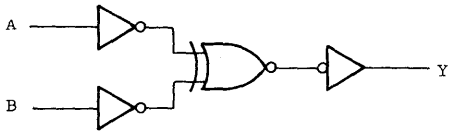


DIP14(3D14A-P)

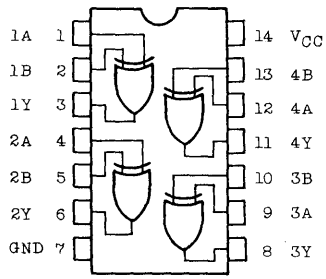


MFP14(F14GB-P)

LOGIC DIAGRAM (per Gate)



PIN ASSIGNMENT



(Top View)

TC74HC86P/F

ABSOLUTE MAXIMUM RATINGS

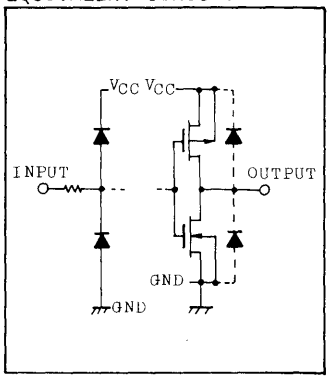
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC86P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

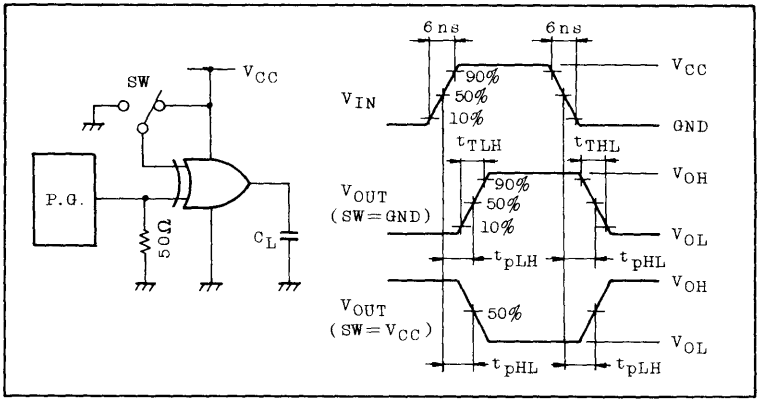
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	120	-	150	ns
			4.5	-	16	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

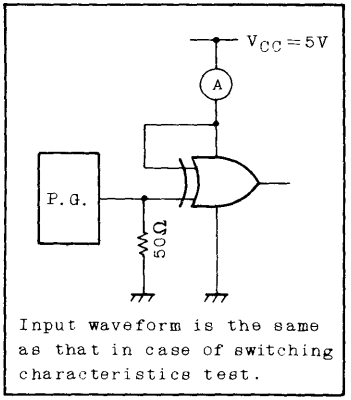
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

TC74HC86P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC107P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

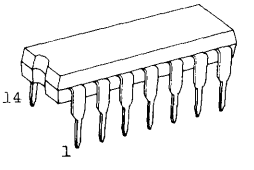
PRELIMINARY

TC74HC107P/F DUAL J-K FLIP FLOP WITH CLEAR

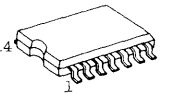
The TC74HC107 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=52MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=2μA(Max.) (Ta=25°C)
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS107



DIP14(3D14A-P)



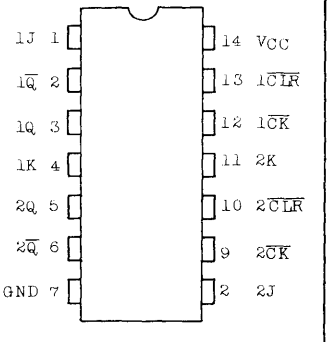
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Doide Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{STG}	-65 ∿ 150	°C
Lead Temperature 10 sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



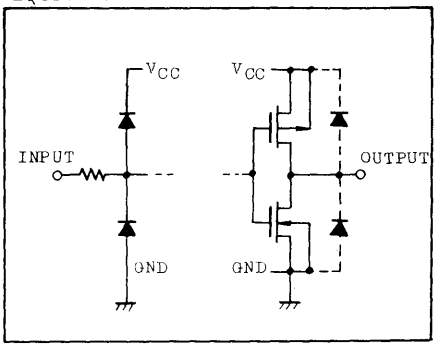
(TOP VIEW)

TC74HC107P/F

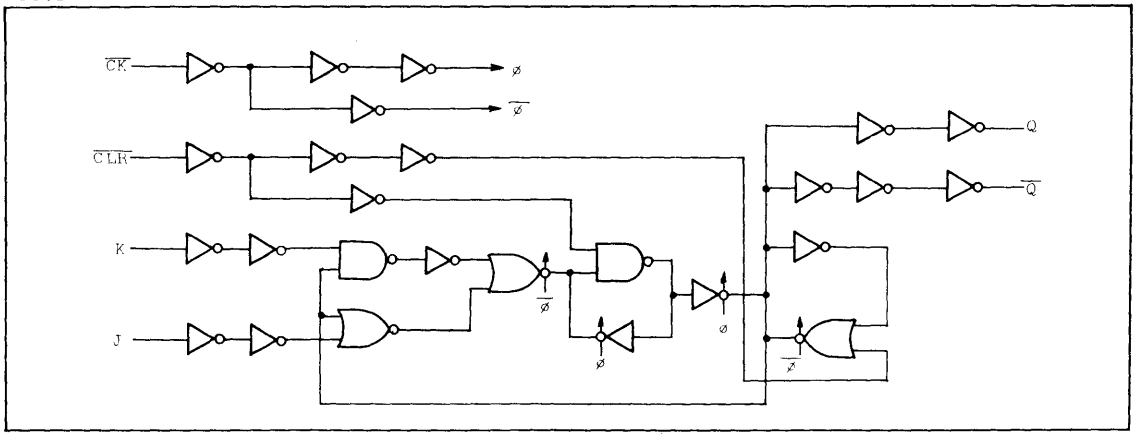
TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	--
H	H	L	↓	H	L	--
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

INPUT and OUTPUT
EQUIVALENT CIRCUIT



LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

TC74HC107P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	48	-	24	-	
			6.0	35	56	-	28	-	

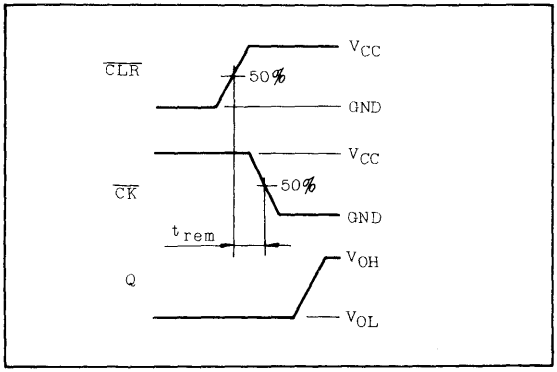
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

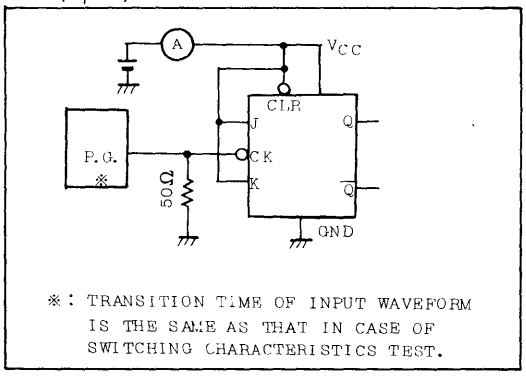
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



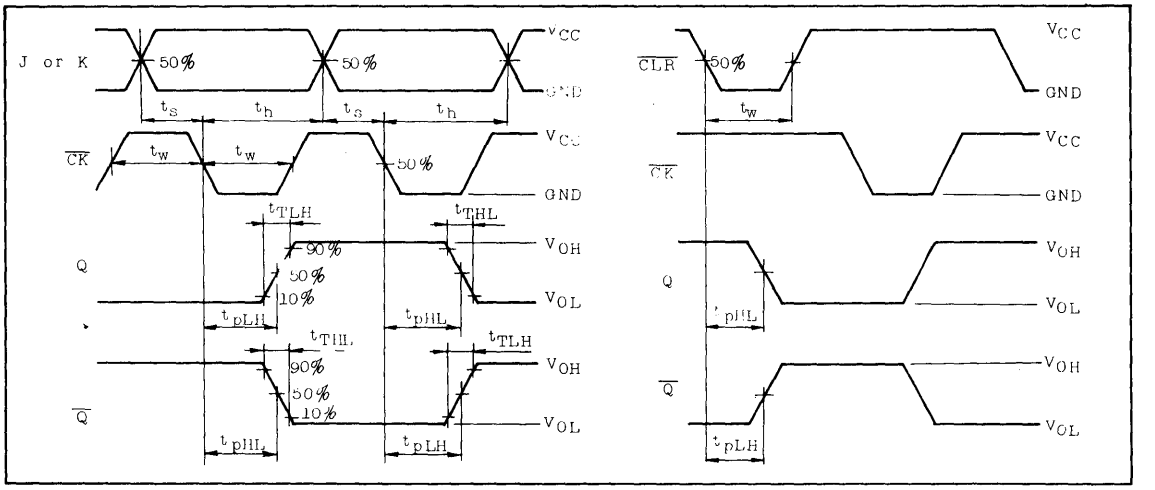
$I_{CC(opr.)}$ TEST CIRCUIT



※ : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC107P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC109P

PRELIMINARY

TC74HC109P DUAL J-$\overline{K}$ FLIP FLOP WITH PRESET AND CLEAR

The TC74HC109 is a hgih speed CMOS DUAL J-$\overline{K}$ FLIP FLOP fabricated with silicon gate C²MOS technology.

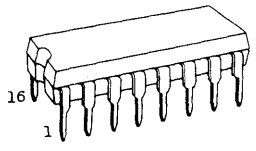
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and $\overline{K}$ input this device changes state on positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS109



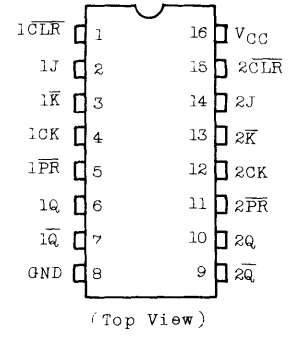
DIP16(3D16A-P)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	$\overline{K}$	CK	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	↓	Qn	$\overline{Q}$n	NO CHANGE
H	H	L	L	↓	L	H	
H	H	H	H	↓	H	L	
H	H	H	L	↓	$\overline{Q}$n	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Q}$n	NO CHANGE

X : Don't care

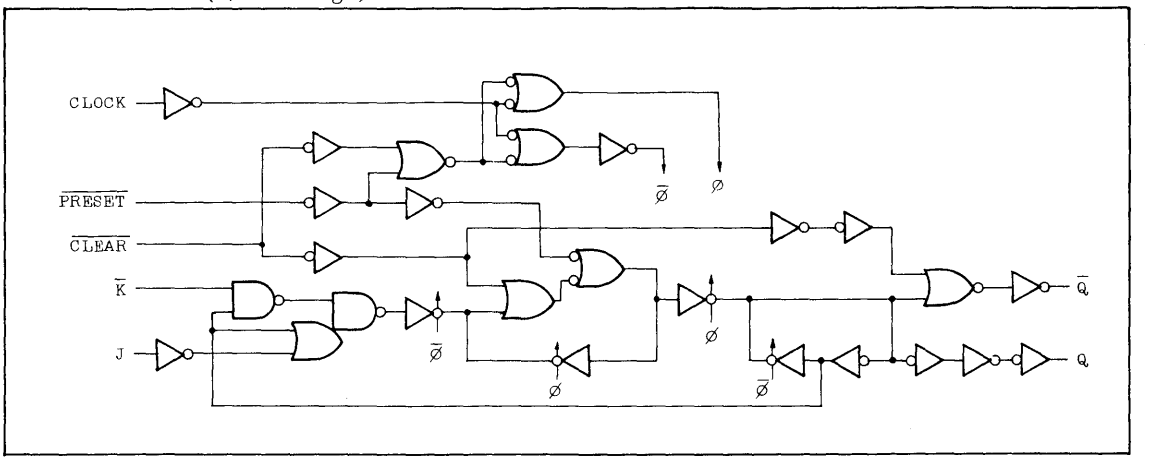
PIN ASSIGNMENT



(Top View)

TC74HC109P

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

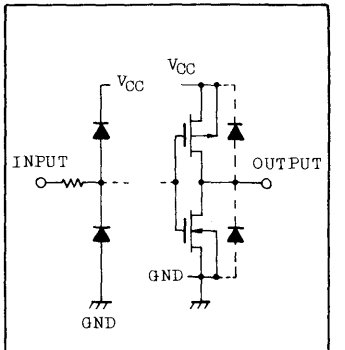
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0~500 (V_{CC}=4.5V) 0~400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	ns
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	ns
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	

TC74HC109P

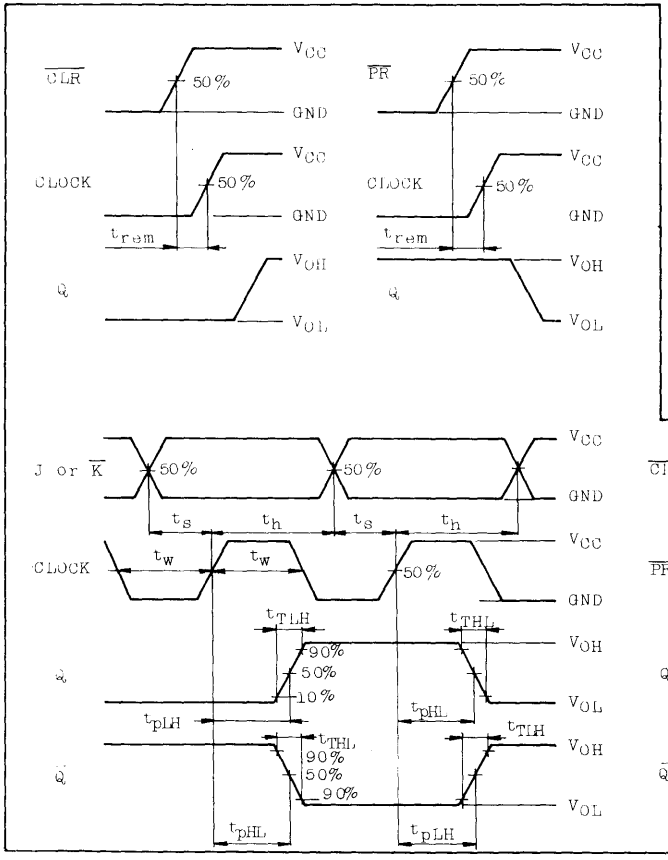
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	57	-	24	-	
			6.0	35	67	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	5	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

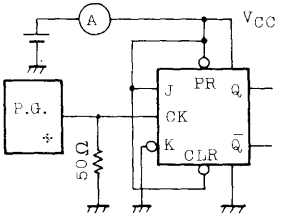
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (Per FF)

TC74HC109P

SWITCHING CHARACTERISTICS TEST WAVEFORM



ICC(opr) TEST CIRCUIT



Input transition time is the same as that in case of switching characteristics test.

TC74HC112P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC112P DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC112 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

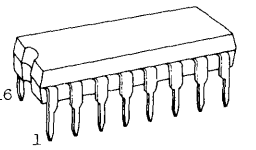
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and K input this device changes state on negative going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

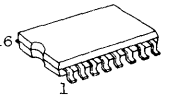
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=58MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS112



DIP16(3D16A-P)



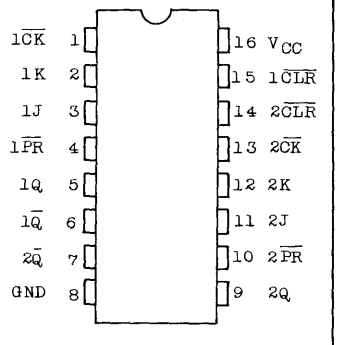
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

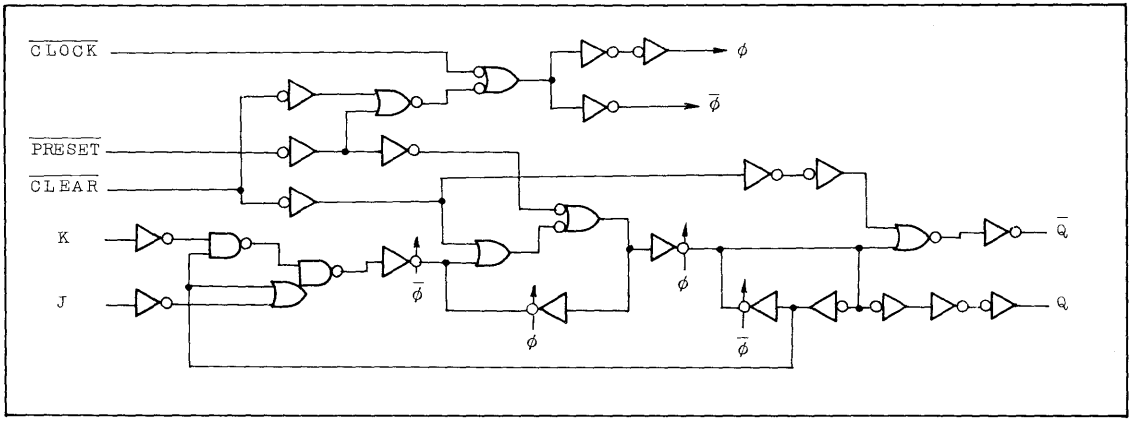
TC74HC112P/F

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	H	L	H	↓	L	H	
H	H	H	L	↓	H	L	
H	H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X : Don't care

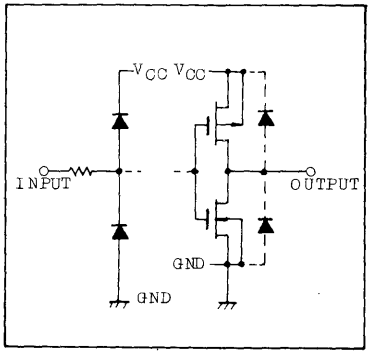
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC112P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	53	-	24	-	
			6.0	35	62	-	28	-	

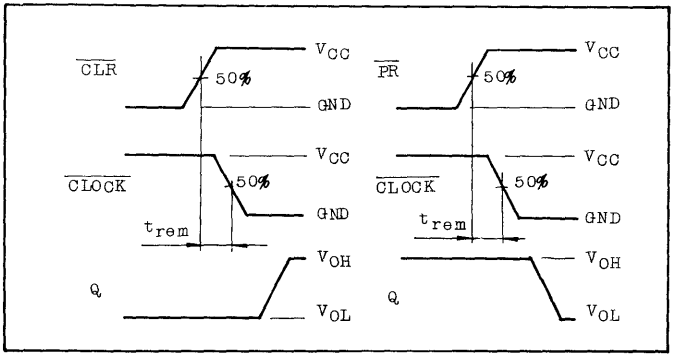
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.0	-	40	100	-	120	
			4.5	-	10	20	-	24	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	54	-	-	-	

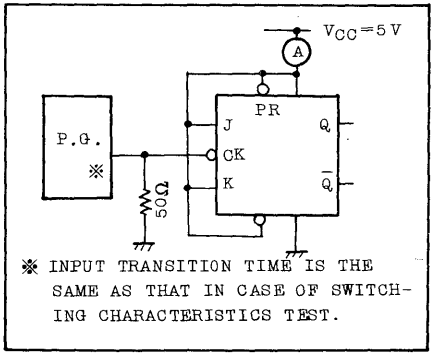
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



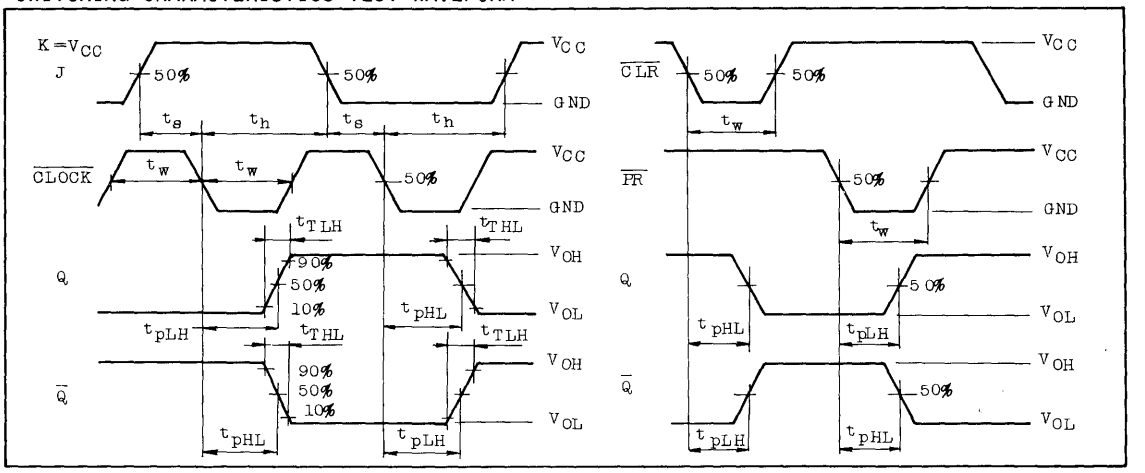
$I_{CC(opr.)}$ TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC112P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC113P

PRELIMINARY

TC74HC113P DUAL J-K FLIP FLOP WITH CLEAR

The TC74HC113 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

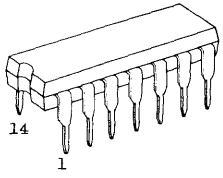
In accordance with logic level applied to J and K input, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$).

The **Preset function** is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=63MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS113



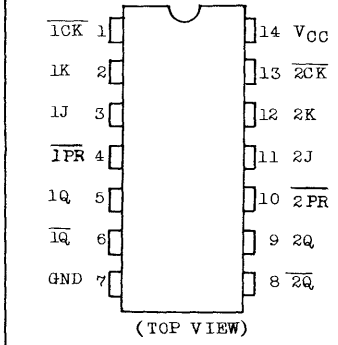
DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

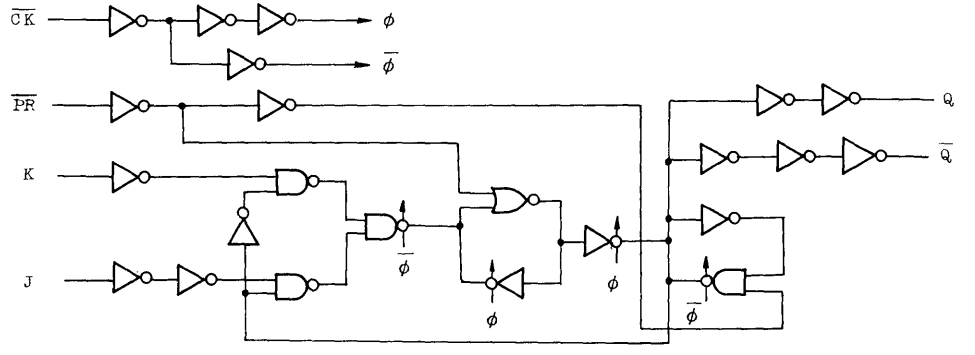
TC74HC113P

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{PR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	H	L	Clear
H	L	L	↓	Qn	$\overline{Qn}$	No Change
H	L	H	↓	L	H	-
H	H	L	↓	H	L	-
H	H	H	↓	$\overline{Qn}$	Qn	Toggle
H	X	X	↑	Qn	$\overline{Qn}$	No Change

X:DON'T CARE

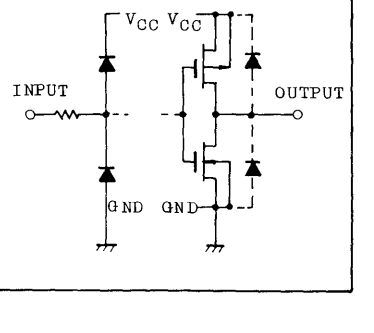
LOGIC DIAGRAM (1/2 Package)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC113P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	68	135	-	170	
	t_{pHL}		4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{PR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	80	160	-	200	
	t_{pHL}		4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	15	-	5	-	MHz
			4.5	32	58	-	27	-	
			6.0	38	68	-	32	-	

TC74HC113P

AC ELECTRICAL CHARACTERISTICS (Continued)

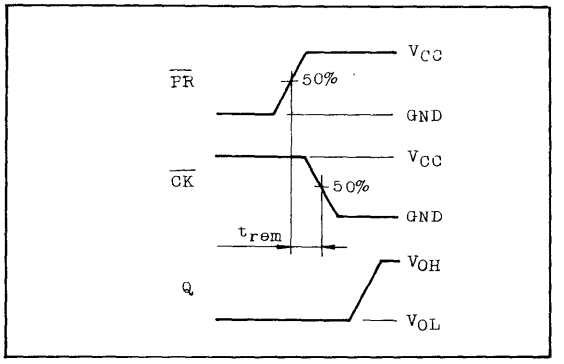
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width ($\overline{CK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width PRESET	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	25	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time PRESET	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	38	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

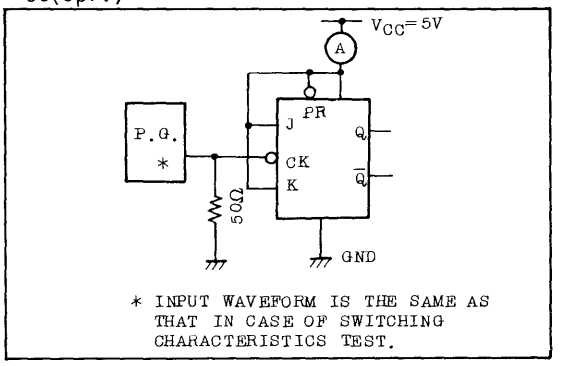
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

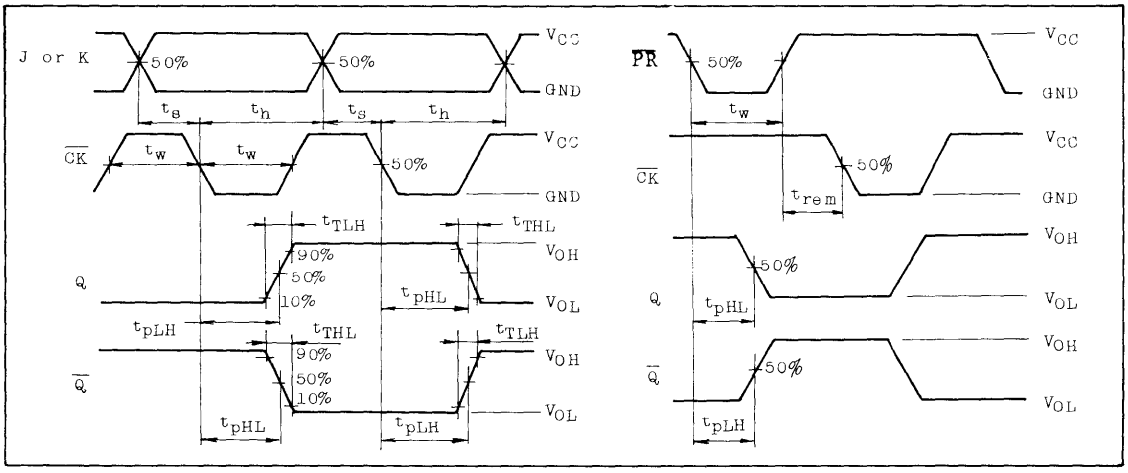


$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWTICHING CHARACTERISTICS TEST WAVEFORM



TC74HC123P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC123P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

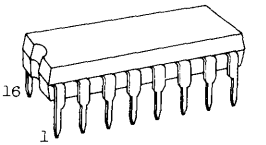
The TC74HC123 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal (t_r=t_f=1 sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CL}$ INPUT (Positive-edge input). After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5KΩ to 1MΩ
..... V_{CC}≧3.0V from 1KΩ to 1MΩ

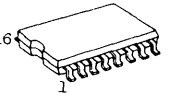
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=26ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Output Pulse Width Range .... $t_{w(OUT)}$=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



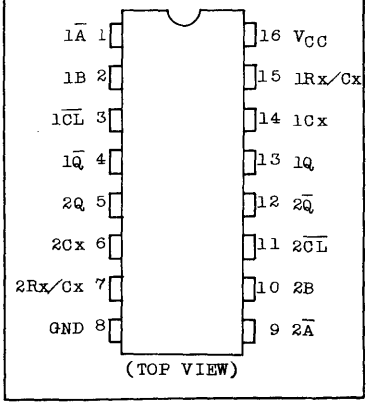
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



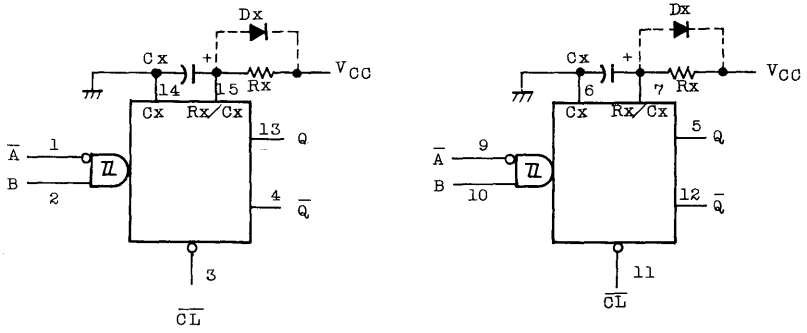
TC74HC123P/F

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⊓	⊔	OUTPUT ENABLE
L	H	↑	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X:DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

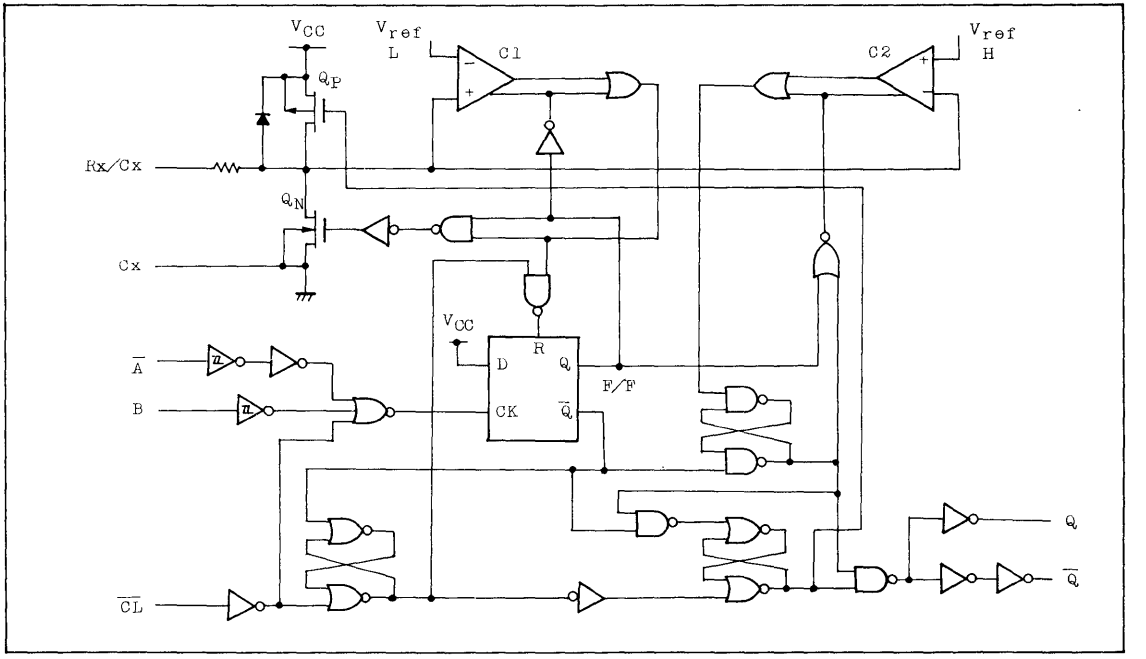
$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

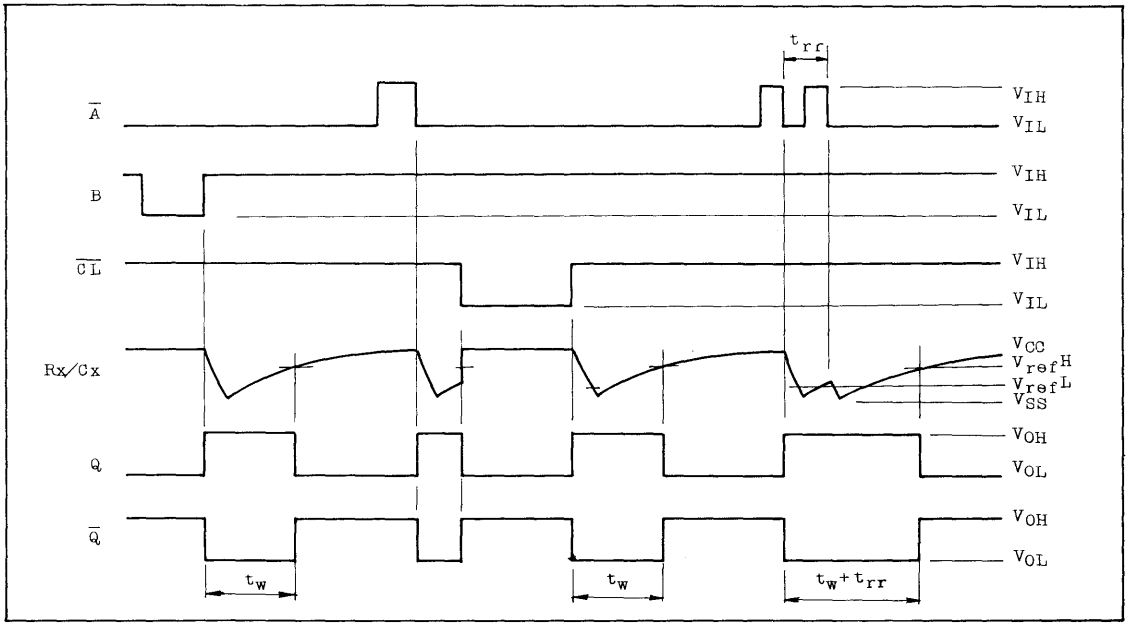
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

TC74HC123P/F

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CL}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{W(OUT)}$ is as follows.

$$t_{W(OUT)} = 0.46 \quad Cx\ Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

(4) Reset operation

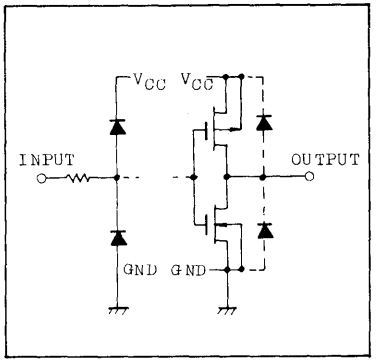
$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC123P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=VCC or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per Circuit

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	t_{PLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{PHL}		6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ TRIGGER - Q, $\overline{Q}$)	t_{pLH}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
	t_{pHL}		6.0	-	29	45	-	55	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Minimum Pulse Width (TRIGGER)	$t_{w(H)}$		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
	$t_{w(L)}$		6.0	-	9	17	-	21	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error Between Circuits In Same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	2.0	-	412	-	-	-	ns
			4.5	-	74	-	-	-	
			6.0	-	63	-	-	-	
		Cx=0.01μF Rx=1kΩ	2.0	-	4.9	-	-	-	μs
			4.5	-	1.1	-	-	-	
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	t_{wOUT} (MIN.)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	t_{wOUT}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1μF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	113	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

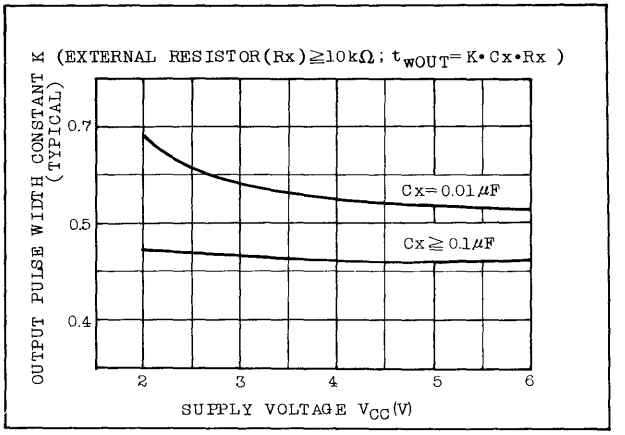
$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current)

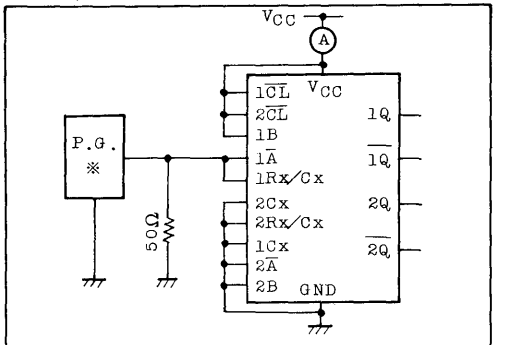
(Duty: %)

TC74HC123P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

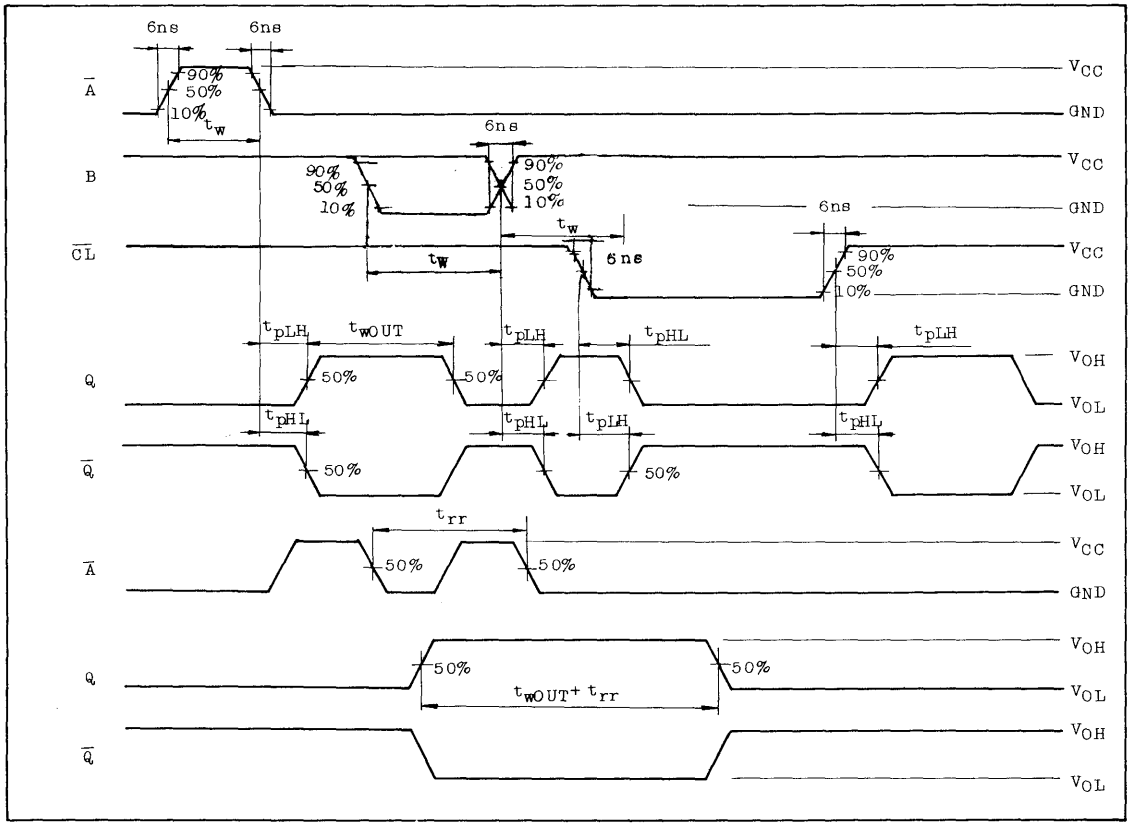


$I_{CC(opr.)}$ TEST WAVEFORM

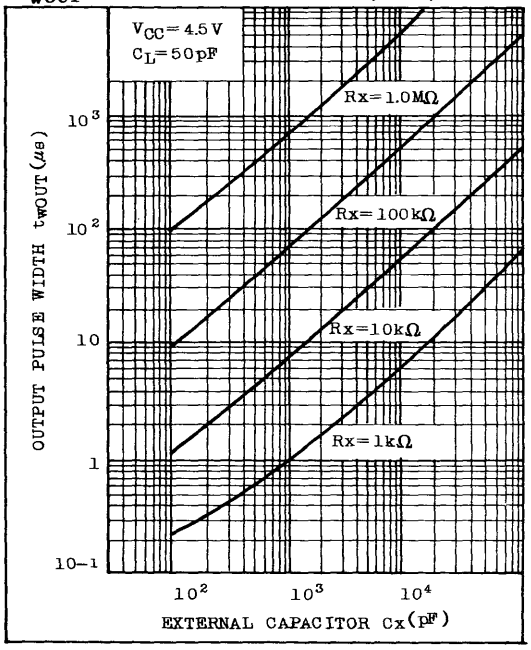


※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

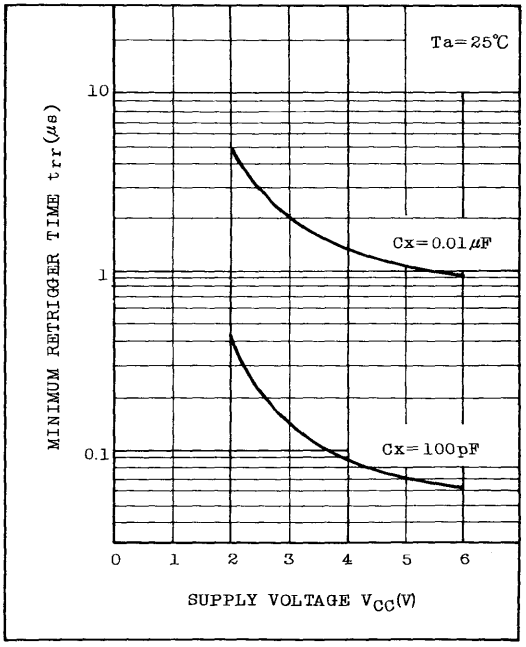
SWITCHING CHARACTERISTICS TEST WAVEFORM



t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



TC74HC125P/F
TC74HC126P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

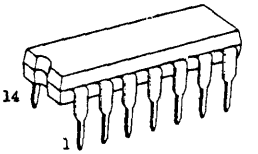
TC74HC125P/F QUAD BUS BUFFER
TC74HC126P QUAD BUS BUFFER

The TC74HC125 and the TC74HC126 are high speed CMOS QUAD BUS BUFFER fabricated with silicon gate C^2MOS technology.

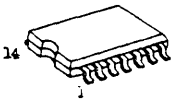
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC125 require the 3-STATE control input $\overline{G}$ to be taken high to put the output into the high impedance condition, whereas the TC74HC126 requires the control input to be taken low to put the output into high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP14(3D14A-P)



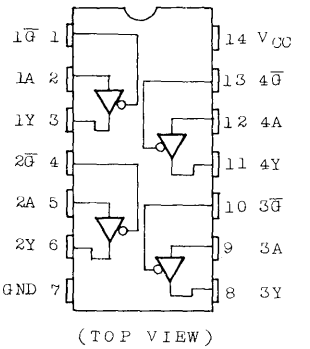
MFP14(F14GB-P)

FEATURES:

- High Speed ..... t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ~ 6V
- Pin and Function Compatible with 74LS125/126

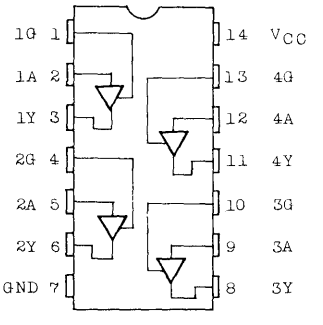
PIN ASSIGNMENT

TC74HC125



(TOP VIEW)

TC74HC126



(TOP VIEW)

TRUTH TABLE

TC74HC125

INPUTS		OUTPUT
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC126

INPUTS		OUTPUT
G	A	Y
L	X	Z
H	L	L
H	H	H

X : DON'T CARE
Z : HIGH IMPEDANCE

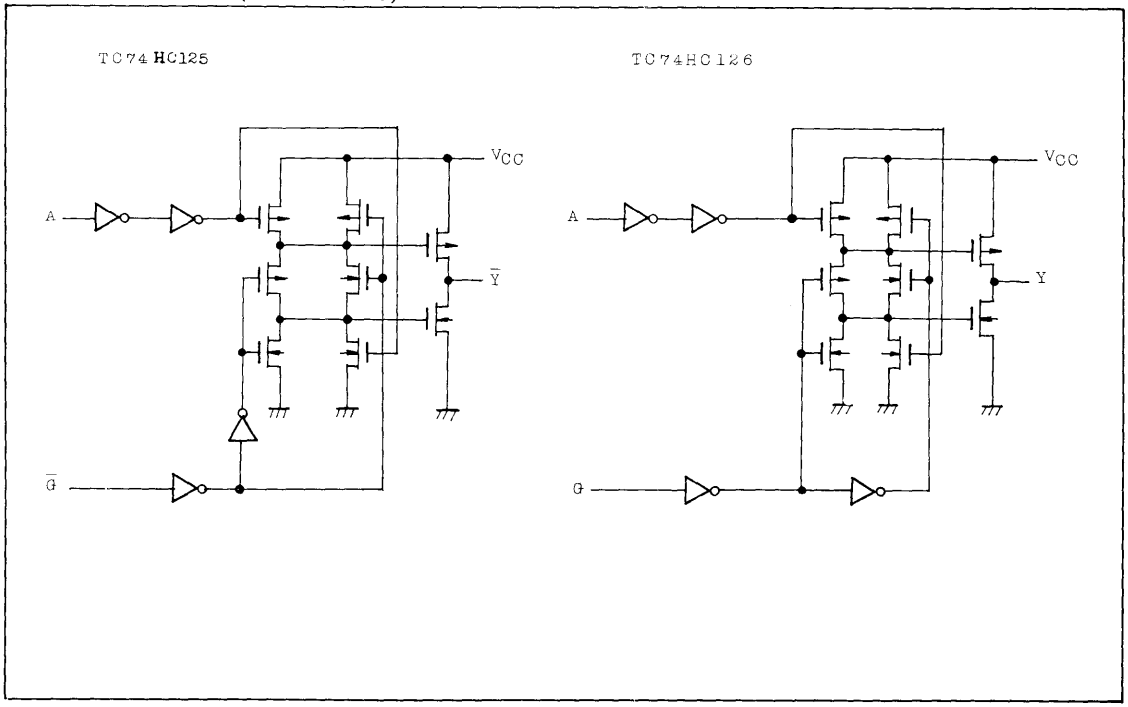
TC74HC125P/F
TC74HC126P

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

CIRCUIT DIAGRAM (Per circuit)

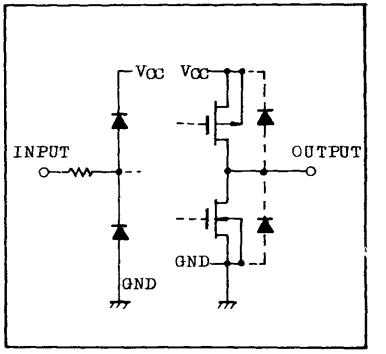


TC74HC125P/F
TC74HC126P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC125P/F
TC74HC126P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

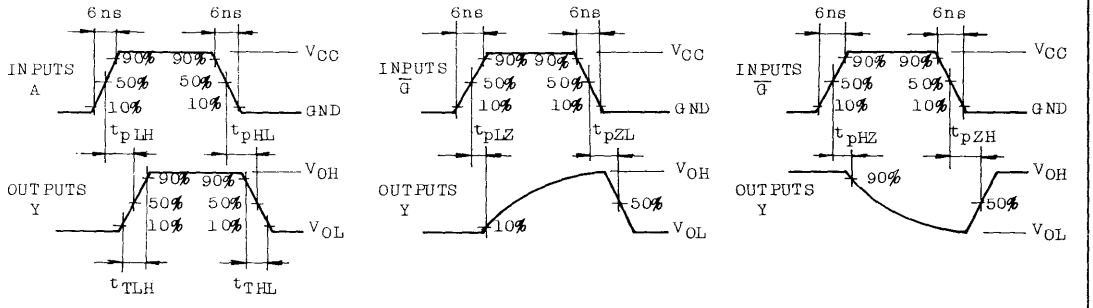
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	44	90	-	115	
			4.5	-	11	18	-	23	
			6.0	-	19	15	-	20	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	68	120	-	150	
			4.5	-	17	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

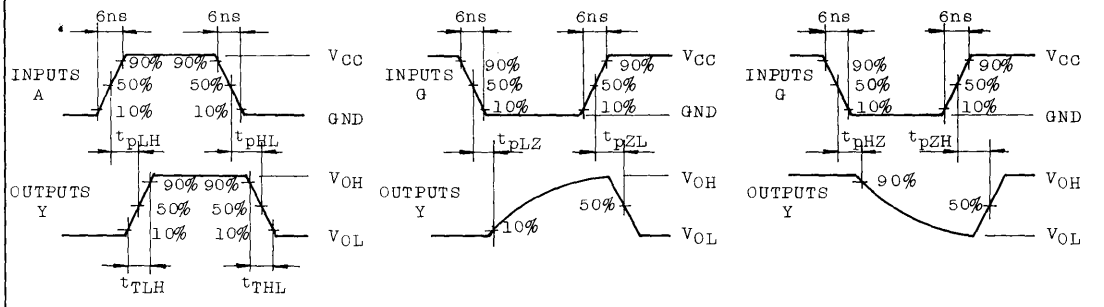
TC74HC125



TC74HC125P/F
TC74HC126P

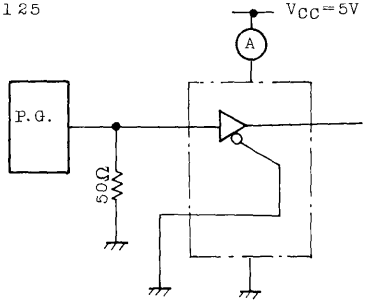
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

TC74HC126

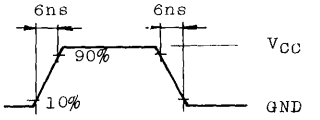


$I_{CC(Opr.)}$ TEST CIRCUIT

TC74HC125



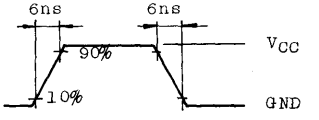
INPUT WAVEFORM

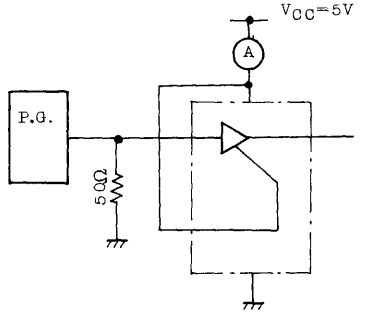


THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

TC74HC126

INPUT WAVEFORM





THE OTHER INPUTS ARE CONNECTED TO V_{CC} LINE OR GND LINE.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC131P

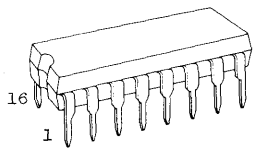
PRELIMINARY

TC74HC131P 3-TO-8 LINE DECODER/LATCH

The TC74HC131 is a high speed CMOS 3-TO-8 LINE DECODER with input register fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input register with a common CLOCK input and 3-to-8 line decoder with enable inputs G1 and $\overline{G2}$. The 3-bit binary data is stored into input register on the positive going transition of the clock pulse, determine which one of outputs will go low.
Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS131



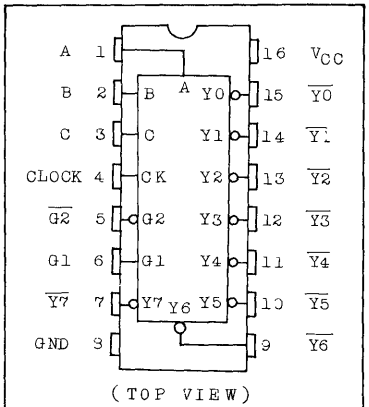
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

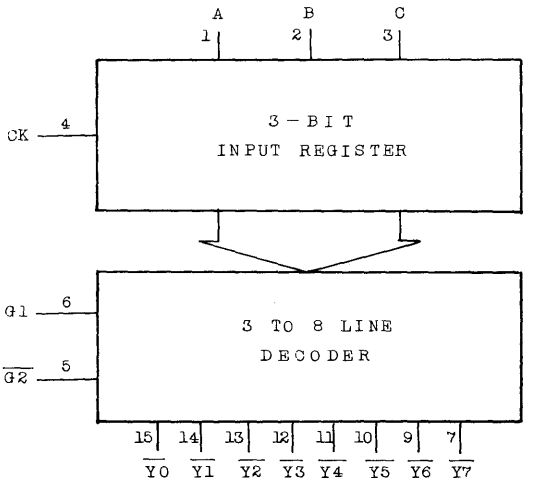
TC74HC131P

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE		CLOCK	SELECT										
G1	$\overline{G2}$		C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	↓	L	L	L	L	H	H	H	H	H	H	H
H	L	↓	L	L	H	H	L	H	H	H	H	H	H
H	L	↓	L	H	L	H	H	L	H	H	H	H	H
H	L	↓	L	H	H	H	H	H	L	H	H	H	H
H	L	↓	H	L	L	H	H	H	H	L	H	H	H
H	L	↓	H	L	H	H	H	H	H	H	L	H	H
H	L	↓	H	H	L	H	H	H	H	H	H	L	H
H	L	↓	H	H	H	H	H	H	H	H	H	H	L
H	L	↑	X	X	X	Outputs corresponding to stored address ····· L All others ····· H							

X : Don't care

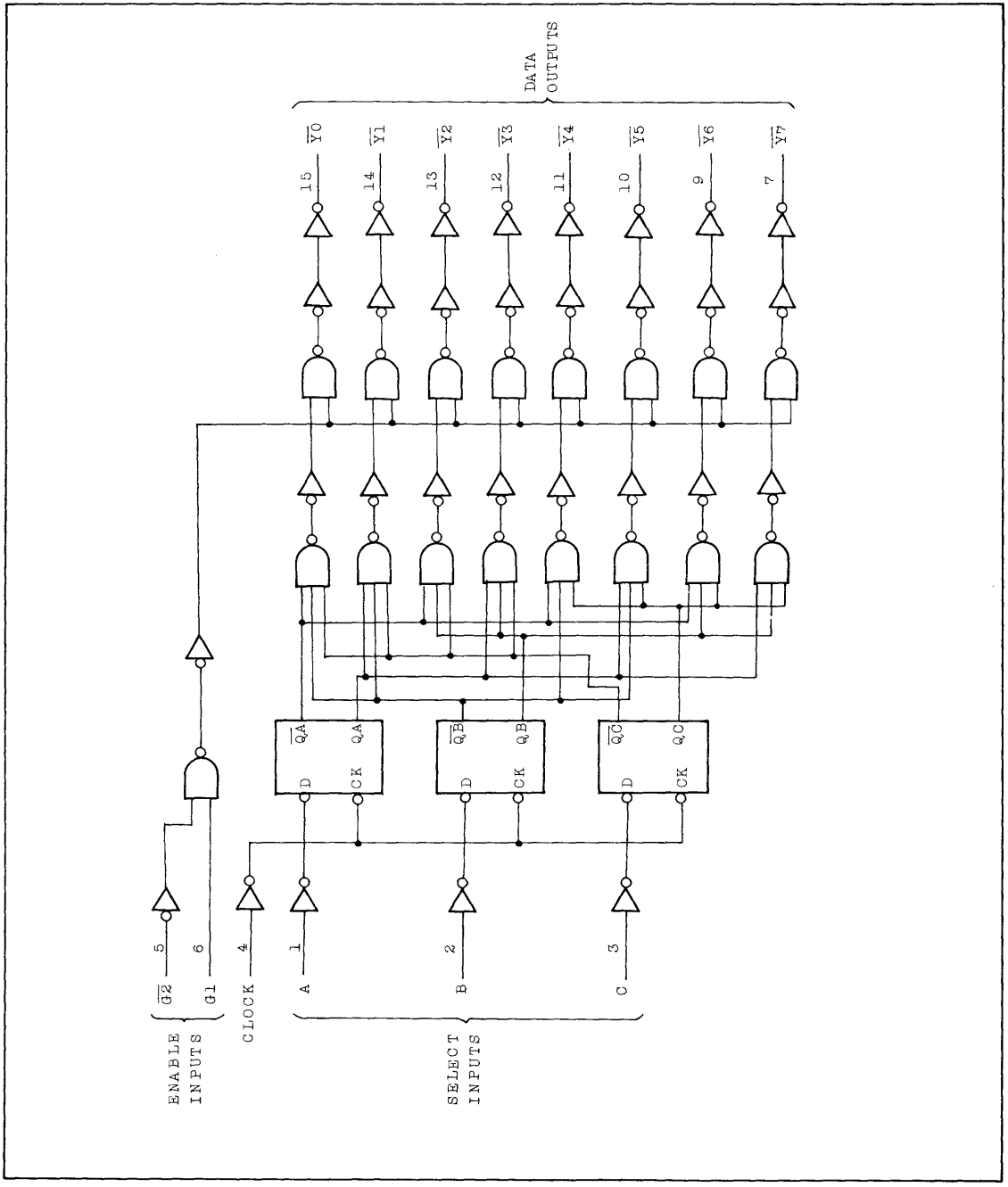
BLOCK DIAGRAM



V_{CC} = 16
GND = 8

TC74HC131P

LOGIC DIAGRAM

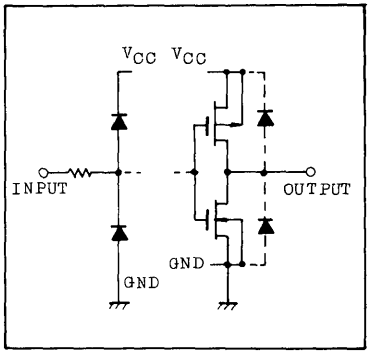


TC74HC131P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{Yn}$)	t_{pLH}		2.0	-	112	210	-	265	
			4.5	-	27	42	-	53	
	t_{pHL}		6.0	-	23	36	-	45	
Propagation Delay Time (G1, $\overline{G2}$ - $\overline{Yn}$)	t_{pLH}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
	t_{pHL}		6.0	-	16	24	-	30	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	12	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	89	-	-	-	

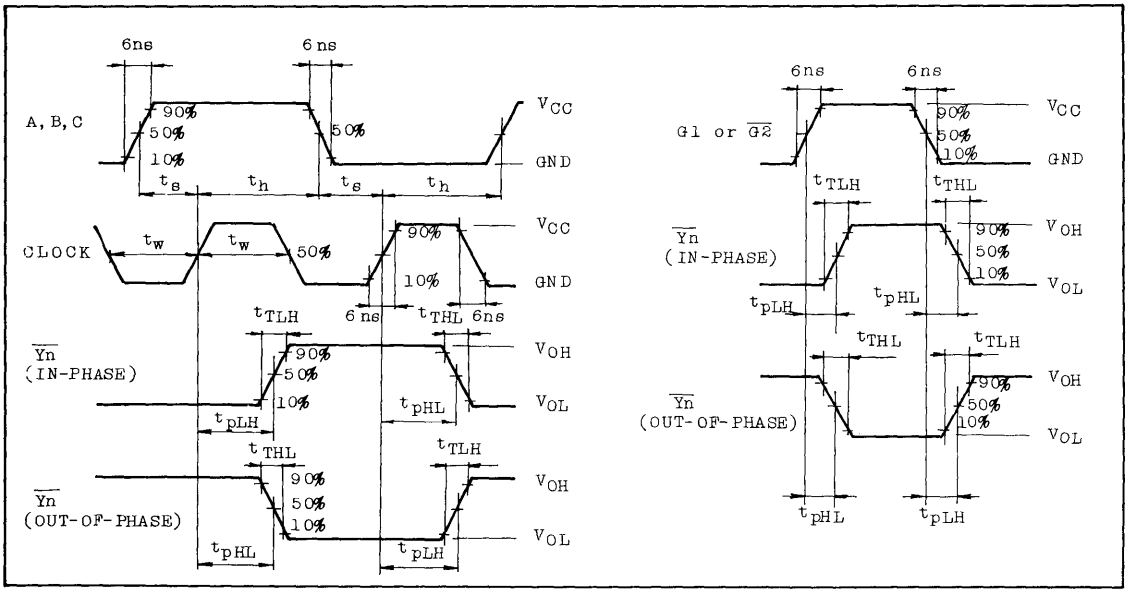
Note 1 C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

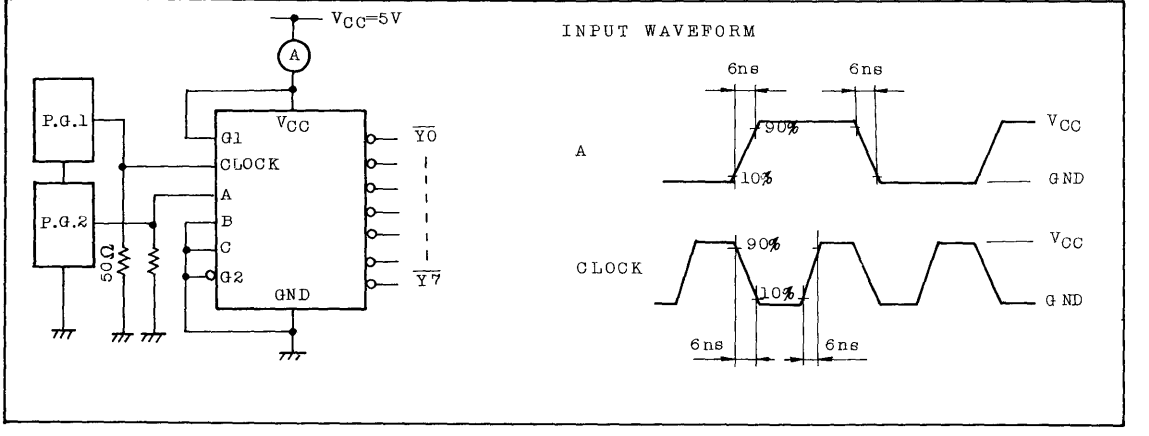
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC131P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC132P/F

PRELIMINARY

TC74HC132P/F QUAD 2-INPUT SCHMITT NAND GATE

The TC74HC132 is a high speed CMOS 2-INPUT NAND SCHMITT TRIGGER GATE fablicated with silicon gate C²MOS technology.

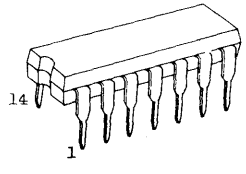
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Pin connection and function are identical to those of the TC74HC00, and provided hysteresis characteristics (around 20% V_{CC}) of all input enables transforming slowly changing input signals into sharply defined jitter-free output signals.

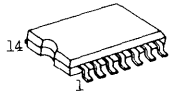
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_H=0.9V at V_{CC}=5V
- Output Drive Capability.....10 LSTTL Loads
- Symmertical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS132

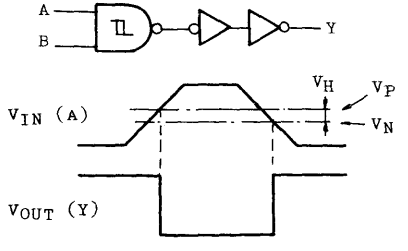


DIP14(3D14A-P)

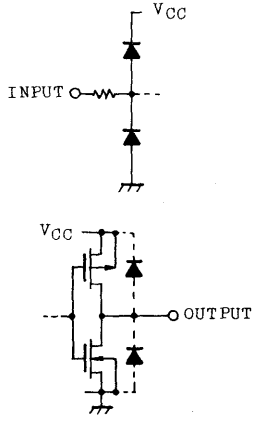


MFP14(F14GB-P)

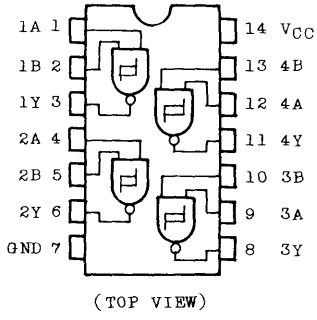
LOGIC DIAGRAM and INPUT OUTPUT WAVEFORM



INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGNMENT



(TOP VIEW)

TC74HC132P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Threshold Voltage	V_P		2.0	0.8	1.25	1.5	0.8	1.7	V
			4.5	2.25	2.7	3.15	2.25	3.15	
			6.0	3.0	3.6	4.2	3.0	4.20	
Low-Level Threshold Voltage	V_N		2.0	0.4	0.75	1.0	0.3	1.2	V
			4.5	1.35	1.9	2.25	1.35	2.25	
			6.0	1.8	2.6	3.0	1.8	3.0	
Hysteresis Voltage	V_H		2.0	0.20	0.5	1.0	0.20	1.0	V
			4.5	0.4	0.8	1.4	0.4	1.4	
			6.0	0.6	1.0	1.7	0.6	1.70	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

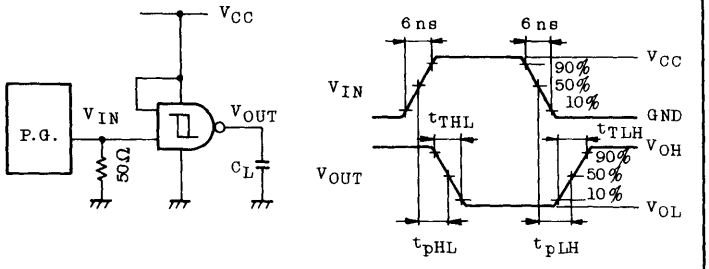
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	ns
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	35	-	-	-	

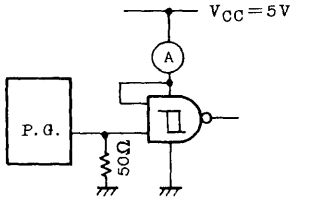
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

TC74HC132P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC133P

PRELIMINARY

TC74HC133P 13 INPUT NAND GATE

The TC74HC133 is a high speed CMOS 13-INPUT NAND GATE fabricated with silicon gate C²MOS technology.

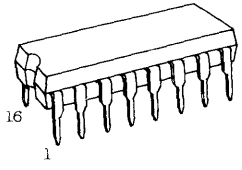
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 7 stages including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

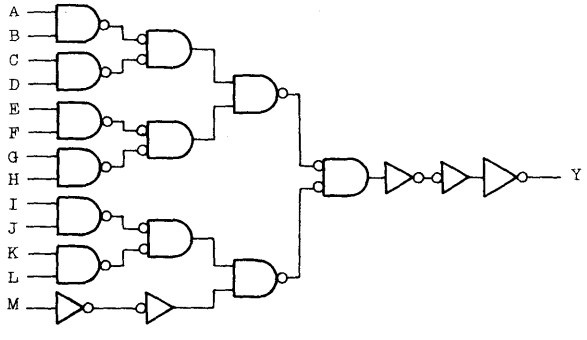
FEATURES:

- High Speed.....t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS133

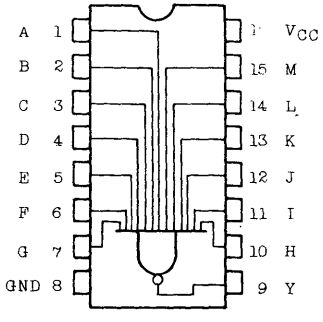


DIP16(3D16A-P)

LOGIC DIAGRAM



PIN ASSIGNMENT



(Top View)

TC74HC133P

ABSOLUTE MAXIMUM RATINGS

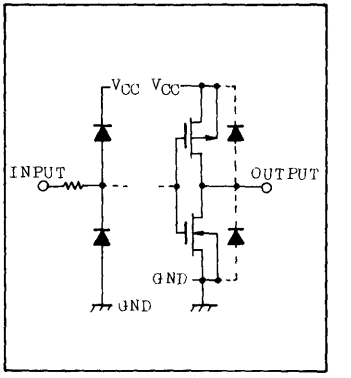
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC133P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

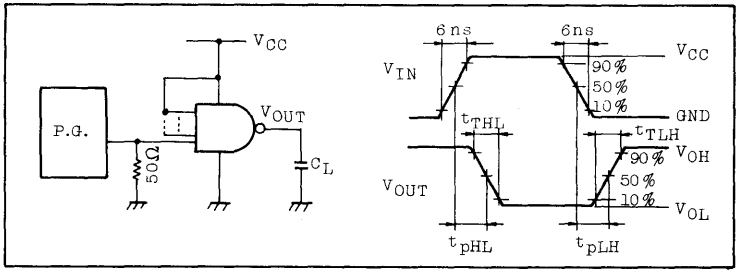
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	80	150	-	190	ns
			4.5	-	20	30	-	38	
			6.0	-	17	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

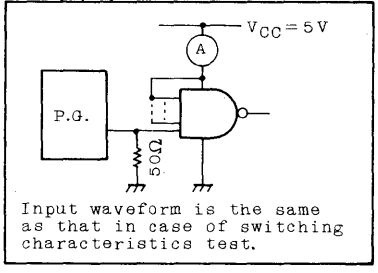
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC137P/F

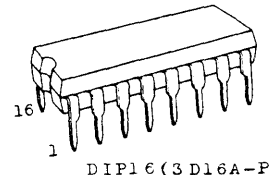
PRELIMINARY

TC74HC137P/F 3-TO-8 LINE DECODER/LATCH

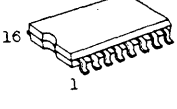
The TC74HC137 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go low. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS137.



DIP16(3D16A-P)



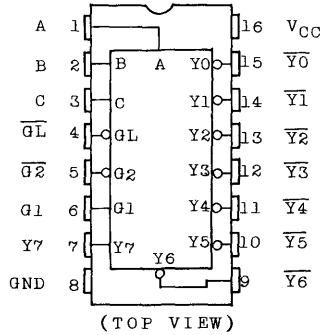
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



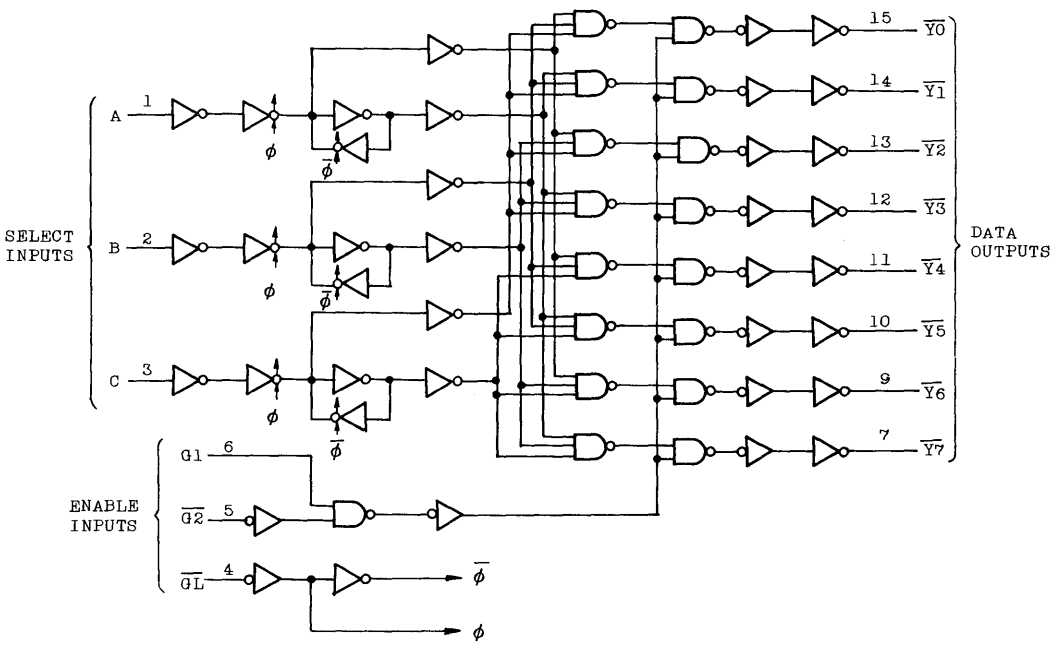
(TOP VIEW)

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	Output corresponding to stored address, L; all others, H							

X: Don't care

LOGIC DIAGRAM

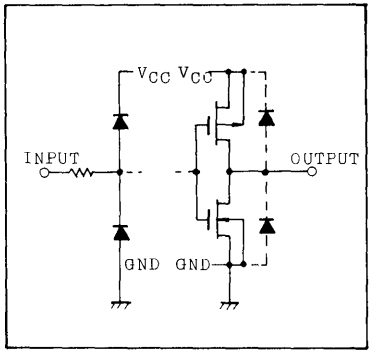


TC74HC137P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

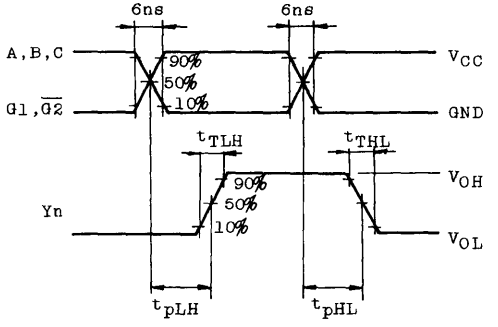
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

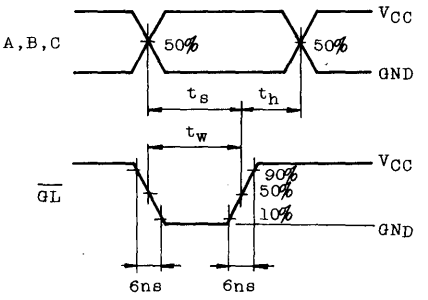
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	80	155	-	195	
			4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{GL}$ - Y)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C, - $\overline{GL}$)	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time (A, B, C, - $\overline{GL}$)	t_h		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	65	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

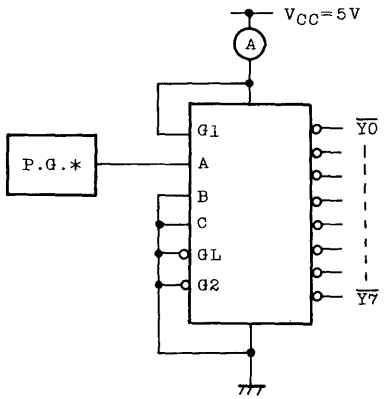
TC74HC137P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



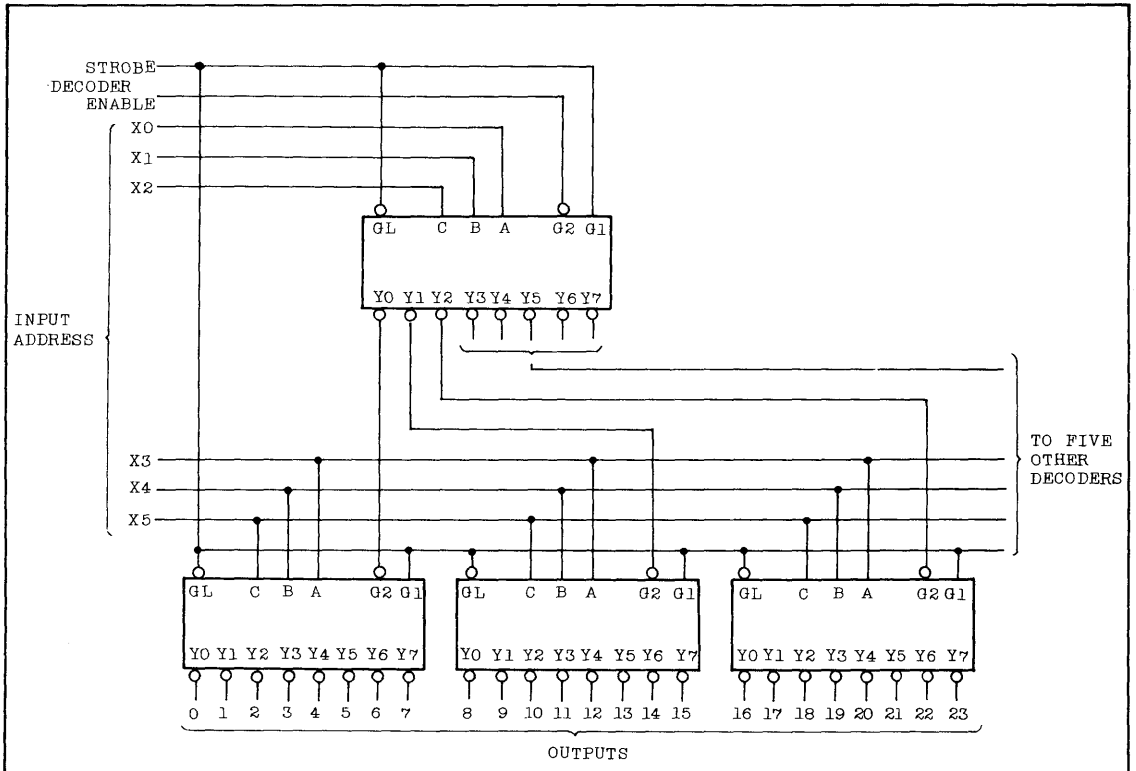


I_{CC}(Opr.) TEST CIRCUIT



* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HCT137P

CMOS DIGITAL INTEGRATED CIRCUIT

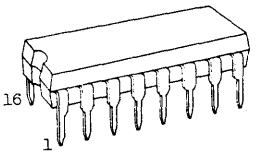
PRELIMINARY

TC74HCT137P/F 3-TO-8 LINE DECODER/LATCH

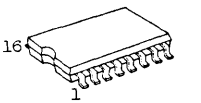
The TC74HCT137 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C^2MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go low. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=23ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Pin and Function Compatible with 74LS137



DIP16(3D16A-P)



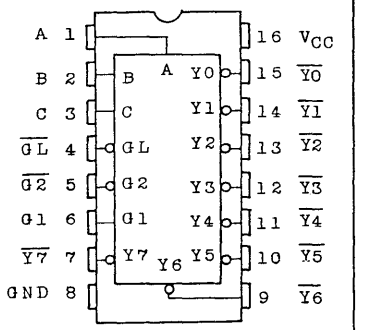
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

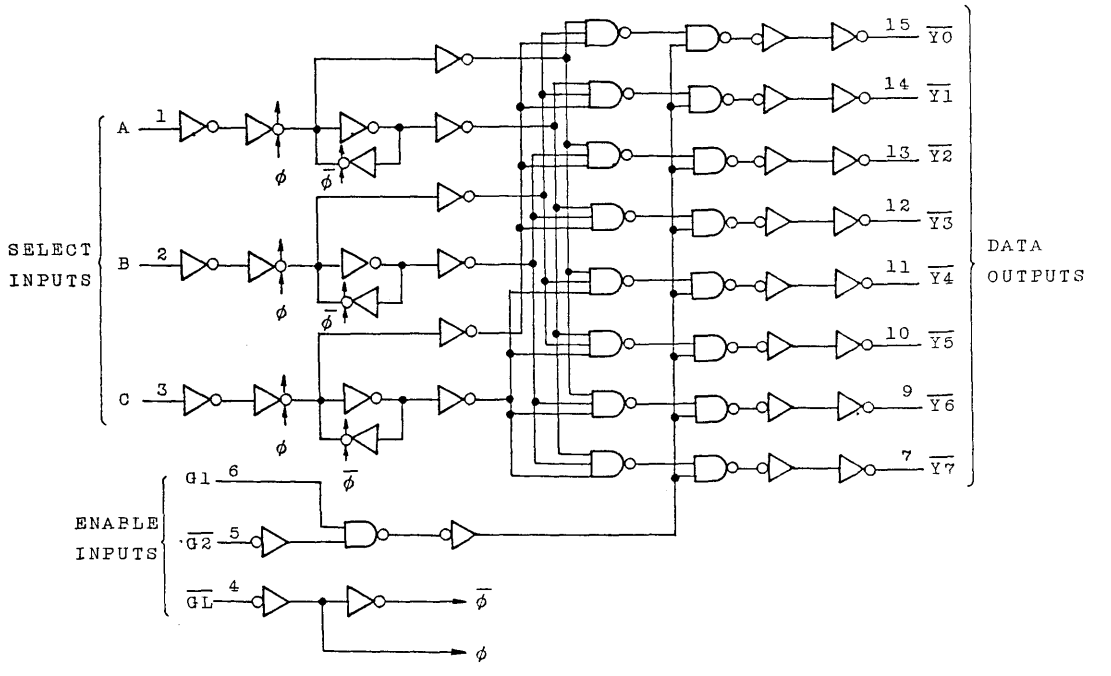
TC74HCT137P

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	L	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	H	X	X	X	Output corresponding to stored address, L; all others, H							

X : DON'T CARE

LOGIC DIAGRAM

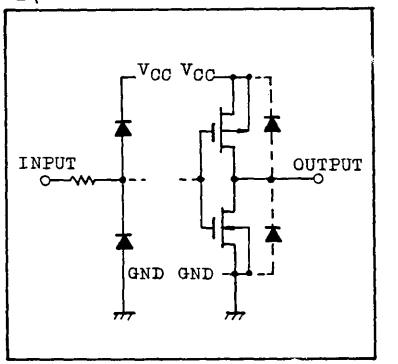


TC74HCT137P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ⟨ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ⟨ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

TC74HCT137P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

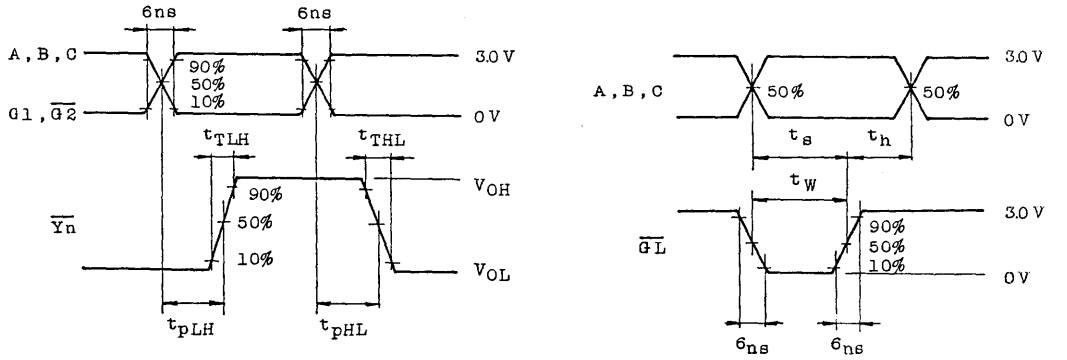
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time ($\overline{G1}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	25	39	-	49	
Propagation Delay Time ($\overline{G2}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	24	37	-	46	
Propagation Delay Time ($\overline{GL}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	34	52	-	65	
Propagation Delay Time (A, B, C - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	29	45	-	56	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		4.5	-	8	15	-	19	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		4.5	-	2	10	-	13	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		4.5	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	68	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

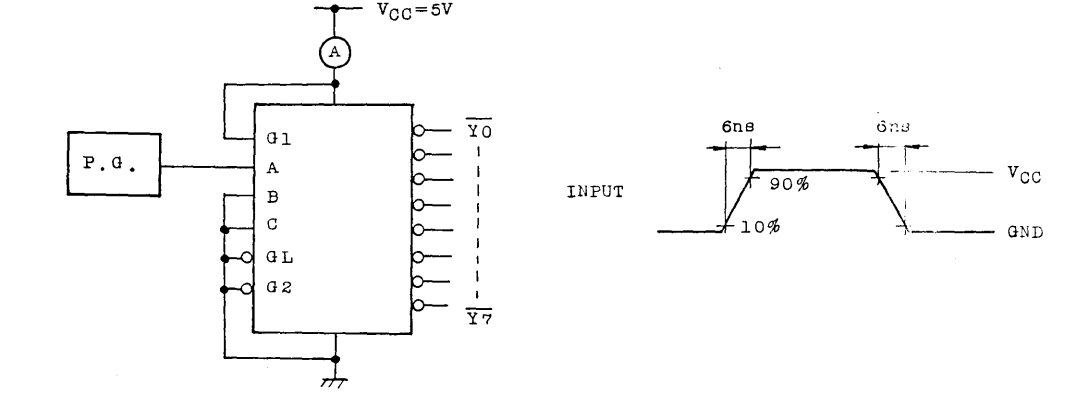
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HCT137P

SWITCHING CHARACTERISTICS TEST WAVEFORM

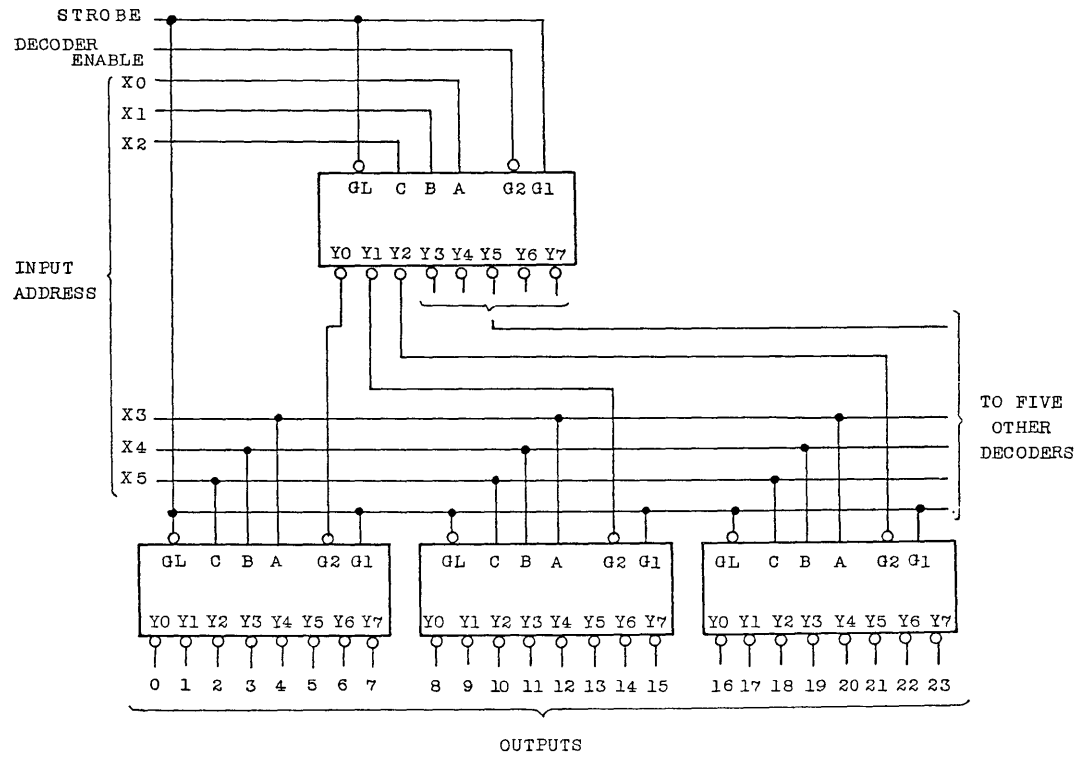


$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HCT137P

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HC138P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

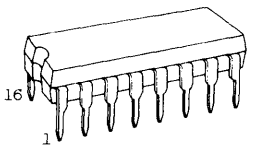
PRELIMINARY

TC74HC138P/F 3-TO-8 LINE DECODER

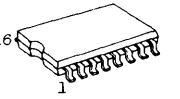
The TC74HC138 is a high speed CMOS DECODER (3-8 LINE) fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
If the device is enabled, 3 binary select inputs (A,B and C) determine which one of outputs will go low.
Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=17ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS138.

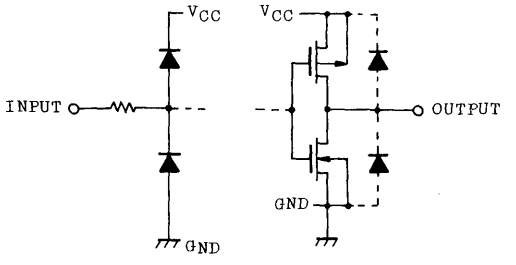


DIP16(3D16A-P)

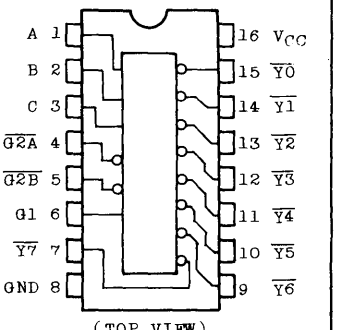


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT

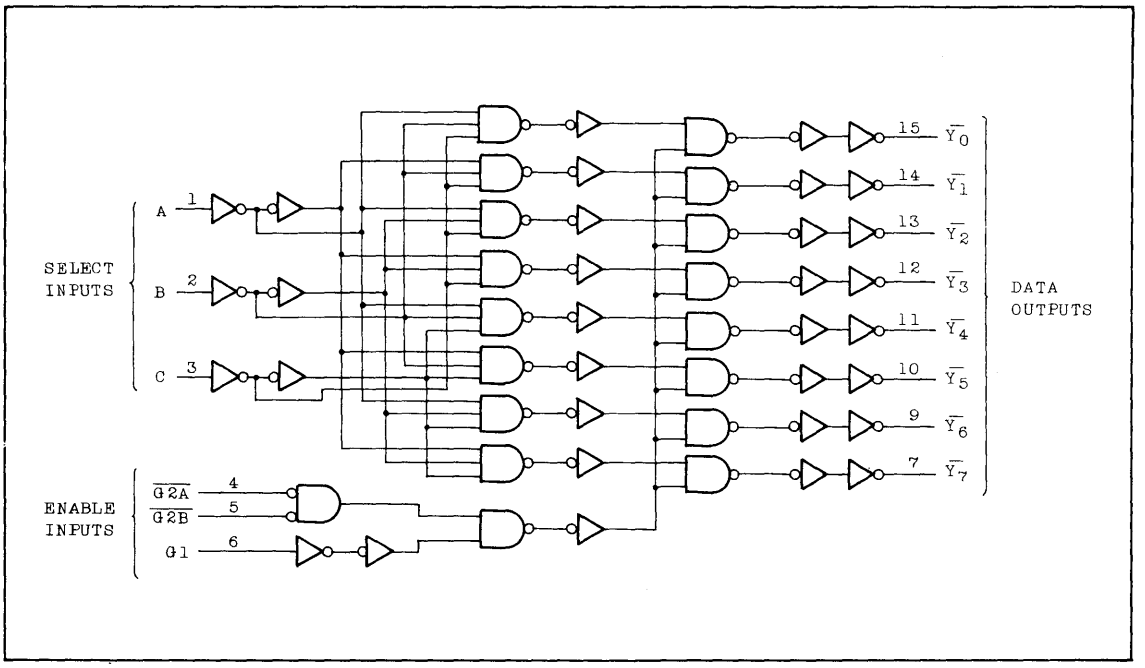


PIN ASSIGNMENT



(TOP VIEW)

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y}_0$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y}_1$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y}_2$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y}_3$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y}_4$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y}_5$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y}_6$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y}_7$

X : Don't Care

TC74HC138P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

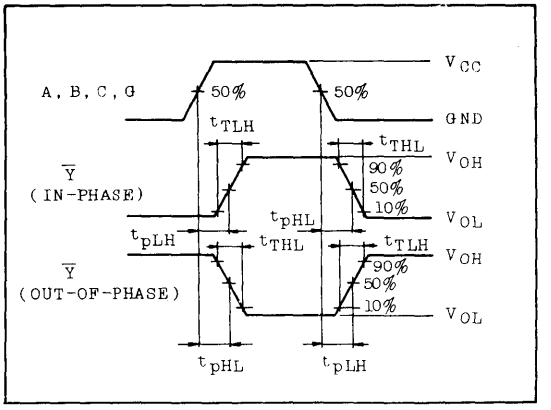
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A,B,C - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	ns
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (G, $\overline{G}$ - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	57	-	-	-	

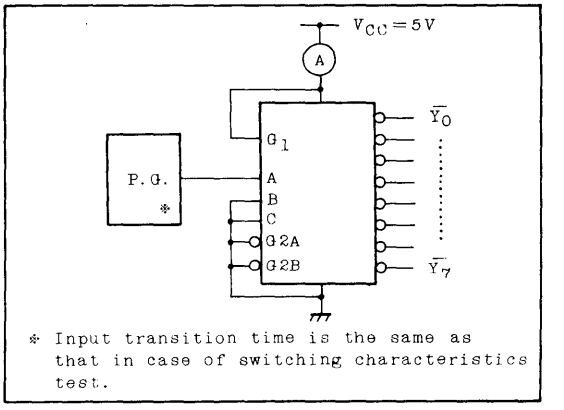
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

TC74HC138P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



* Input transition time is the same as that in case of switching characteristics test.

CMOS DIGITAL INTEGRATED CIRCUIT **TC74HCT138P/F**

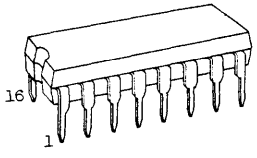
PRELIMINARY

TC74HCT138P/F 3-TO-8 LINE DECODER

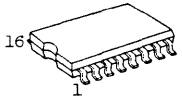
The TC74HCT138 is a high speed CMOS DECODER (3-8 LINE) fabricated with silicon gate C^2MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go low.
Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go high.
3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discahrge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL Outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}| = I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS138

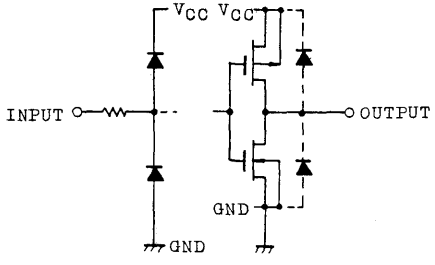


DIP16(3D16A-P)

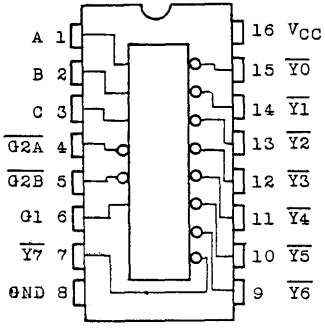


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT



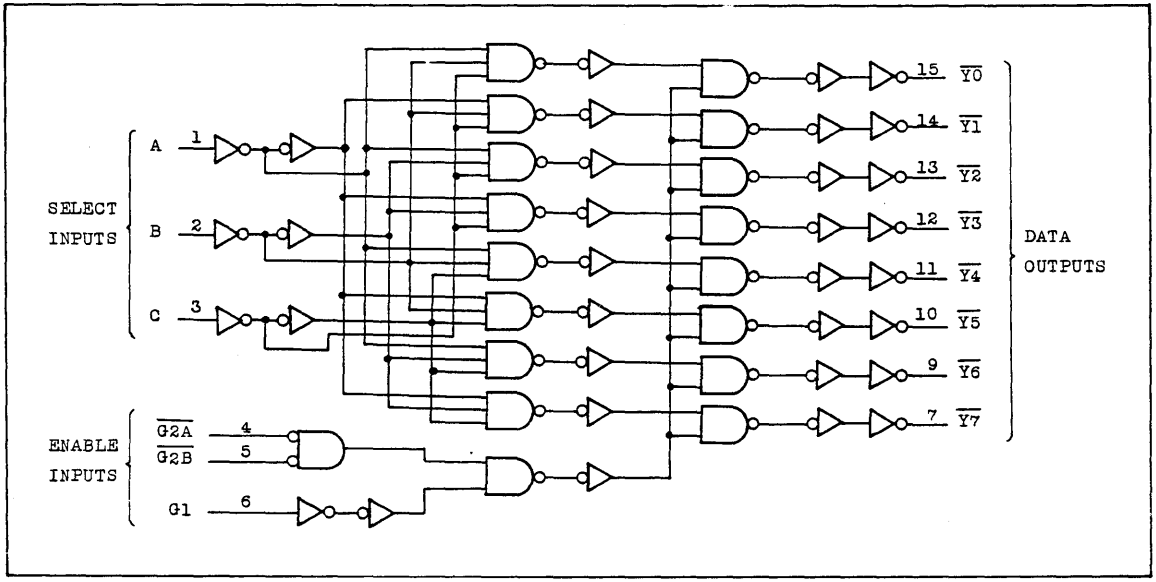
PIN ASSIGNMENT



(Top View)

TC74HCT138P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS								SELECTED OUTPUT
ENABLE			SELECT											
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	H	X	X	X	X	H	H	H	H	H	H	H	H	NONE
X	X	H	X	X	X	H	H	H	H	H	H	H	H	NONE
H	L	L	L	L	L	L	H	H	H	H	H	H	H	$\overline{Y0}$
H	L	L	L	L	H	H	L	H	H	H	H	H	H	$\overline{Y1}$
H	L	L	L	H	L	H	H	L	H	H	H	H	H	$\overline{Y2}$
H	L	L	L	H	H	H	H	H	L	H	H	H	H	$\overline{Y3}$
H	L	L	H	L	L	H	H	H	H	L	H	H	H	$\overline{Y4}$
H	L	L	H	L	H	H	H	H	H	H	L	H	H	$\overline{Y5}$
H	L	L	H	H	L	H	H	H	H	H	H	L	H	$\overline{Y6}$
H	L	L	H	H	H	H	H	H	H	H	H	H	L	$\overline{Y7}$

X : DON'T CARE

TC74HCT138P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ∫ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∫ 5.5	-	-	0.8	-	0.8	
High-Level Ouptut Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA

TC74HCT138P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	μA
	I_C	Per Input: V_{IN}=2.4V or 0.5 Other Input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS

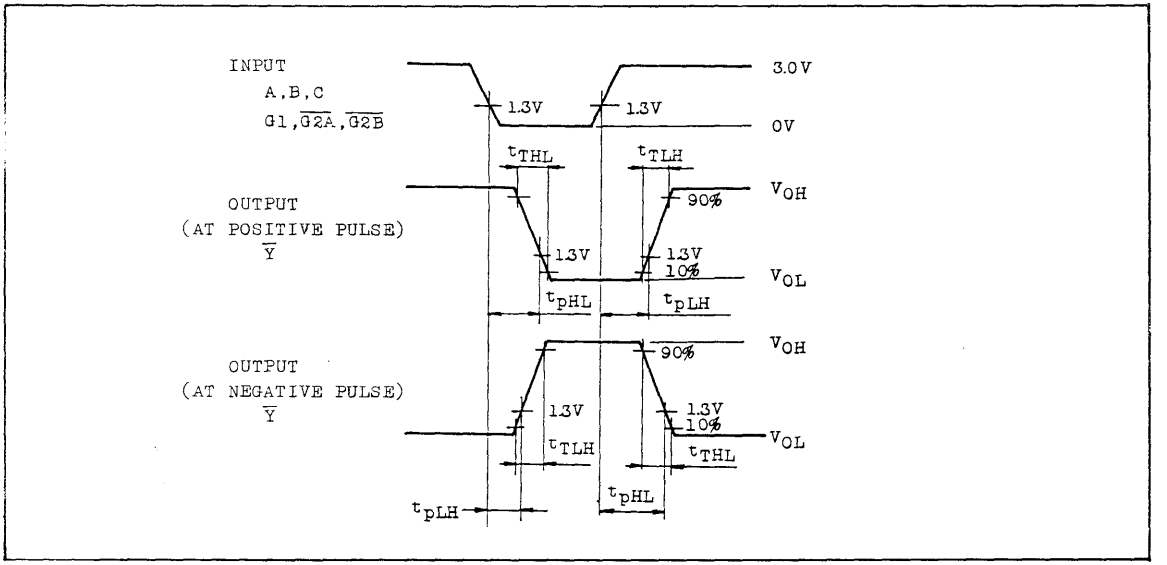
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time (G1 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	26	41	-	51	
Propagation Delay Time (G2 - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	30	47	-	59	
Propagation Delay Time (A, B, C, - $\overline{Y}$)	t_{pLH} t_{pHL}		4.5	-	32	50	-	63	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	65	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

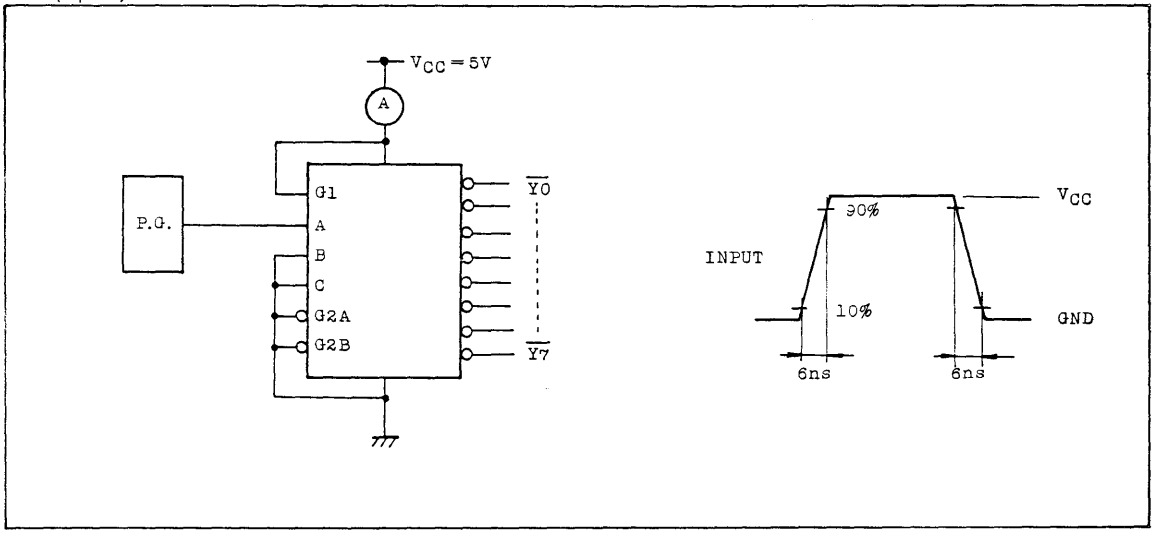
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HCT138P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC139P/F

PRELIMINARY

TC74HC139P/F DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER

The TC74HC139 is a high speed CMOS DUAL TWO LINE TO FOUR LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology.

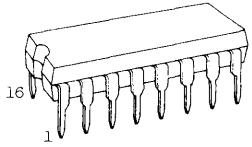
The active low enable input can be used for gating or can be used as a data input for demultiplexing applications.

While the enable input is held high, all four outputs are fixed in high logic level independent of the other inputs.

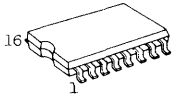
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS139

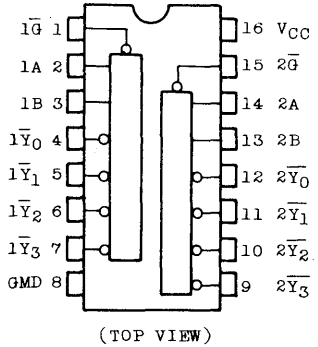


DIP16(3D16A-P)



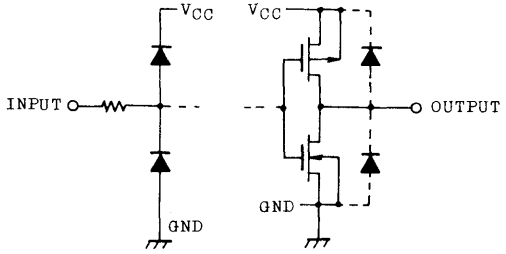
MFP16(F16GC-P)

PIN ASSIGNMENT



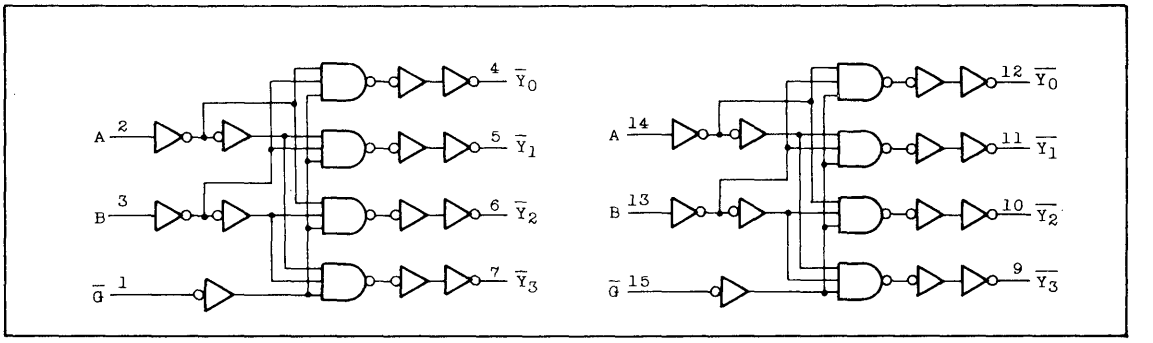
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC139P/F

BLOCK DIAGRAM



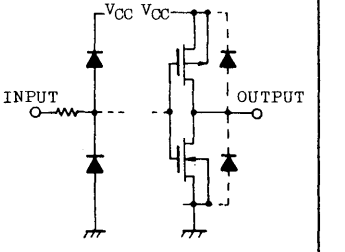
INPUTS			OUTPUTS				SELECTED OUTPUT	Note
ENABLE	SELECT							X : Don't care
$\overline{G}$	B	A	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$		
H	X	X	H	H	H	H	NONE	
L	L	L	L	H	H	H	$\overline{Y}_0$	
L	L	H	H	L	H	H	$\overline{Y}_1$	
L	H	L	H	H	L	H	$\overline{Y}_2$	
L	H	H	H	H	H	L	$\overline{Y}_3$	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT

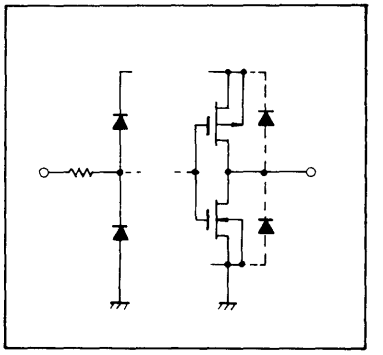


TC74HC139P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Suppl Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

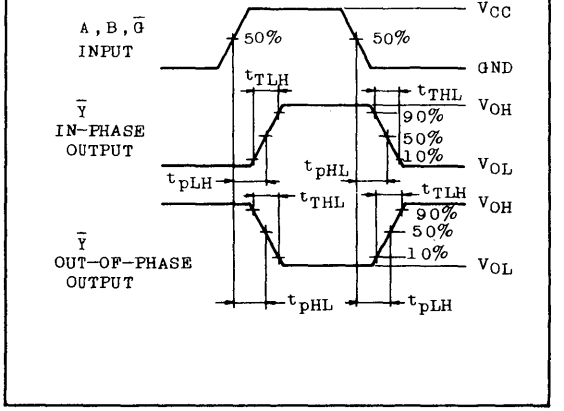
TC74HC139P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

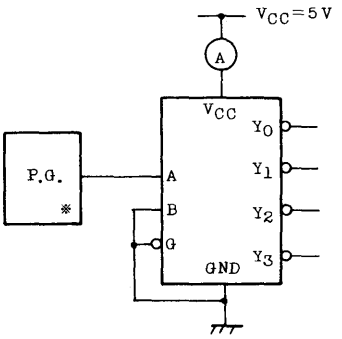
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75		95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time A,B-Y	t_{pLH} t_{pHL}		2.0	-	76	150		190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time $\overline{G}$ - Y	t_{pLH} t_{pHL}		2.0	-	68	135		170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	49	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Decoder)

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



* Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC147P

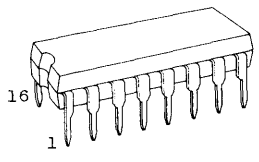
PRELIMINARY

TC74HC147P 10-TO-4 LINE PRIORITY ENCODER

The TC74HC147 is a high speed CMOS 10-TO-4 LINE PRIORITY ENCODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
This encoder features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS147



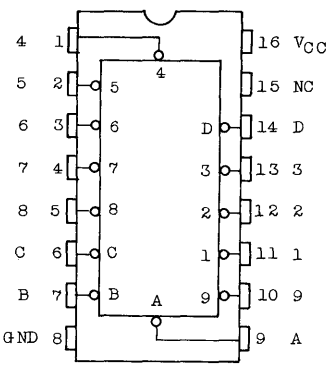
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)
NC : NO CONNECTION

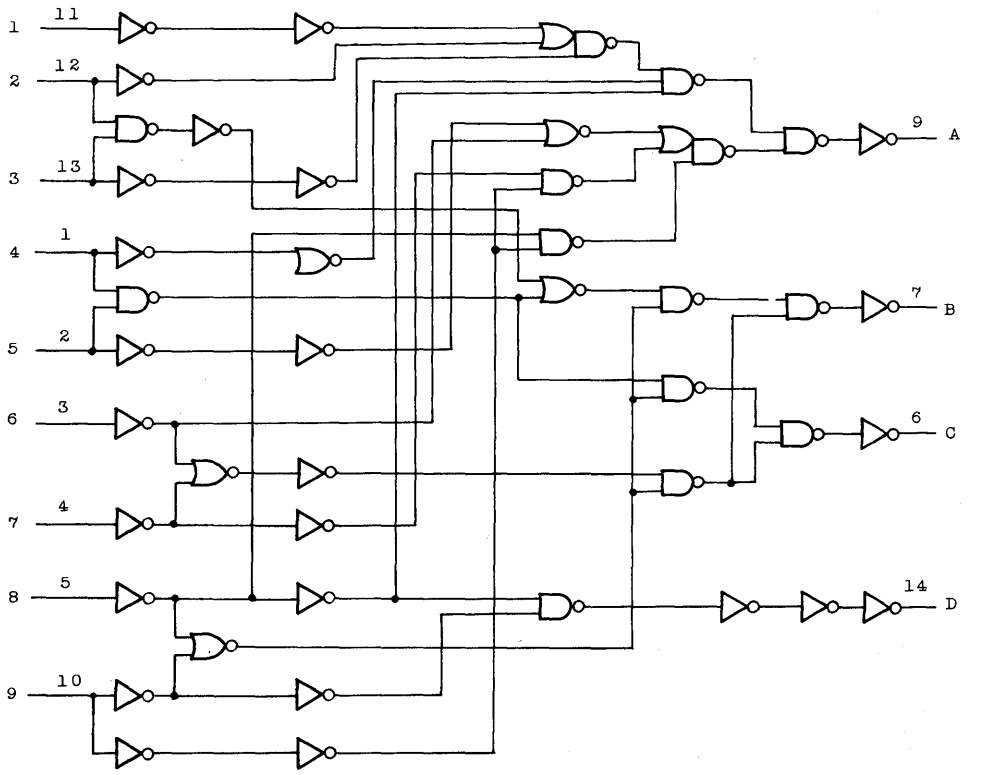
TC74HC147P

TRUTH TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

X : Don't Care

LOGIC DIAGRAM

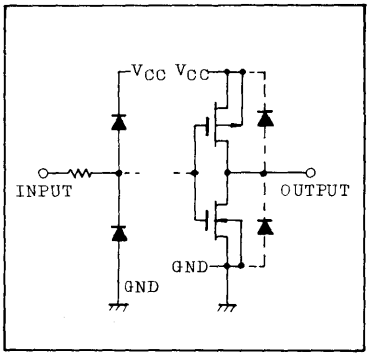


TC74HC147P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC147P

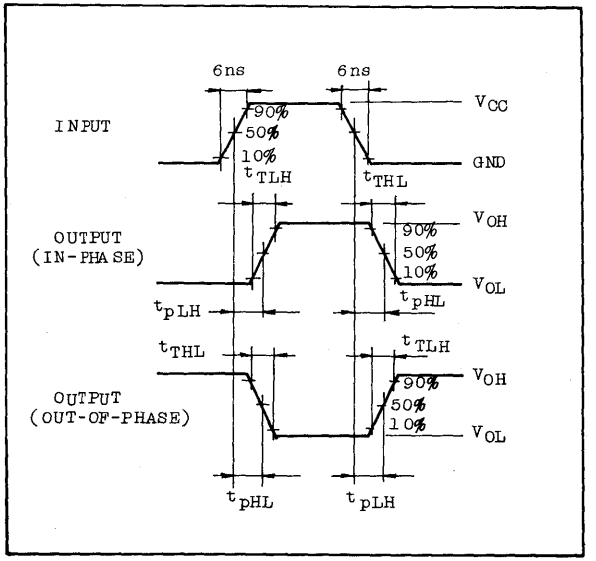
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	37	-	-	-	

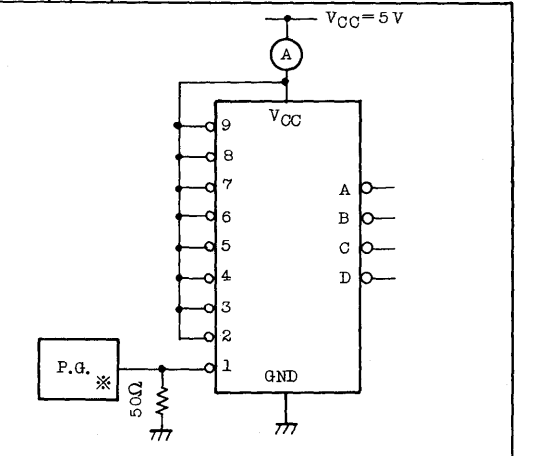
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST WAVEFORM



※ : INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC148P

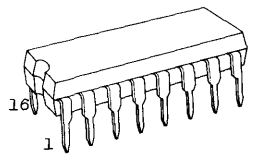
PRELIMINARY

TC74HC148P 8-TO-3 LINE PRIORITY ENCODER

The TC74HC148 is a high speed CMOS 8-TO-3 LINE PRIORITY ENCODER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The encoder detects "L" level of the highest order among eight input signals and outputs the corresponding signal position in binary code. The inputs are eight input signals of 0 through 7 and input EI and when EI is set to "H" level, the encode operation is inhibited making all the outputs at "H" level. The encoded output appears on three signal lines A0 through A2 in binary. Outputs EO and GS are the outputs to indicate the operational mode of encoder and used when the number of bits is to be increased by cascade connection. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS148



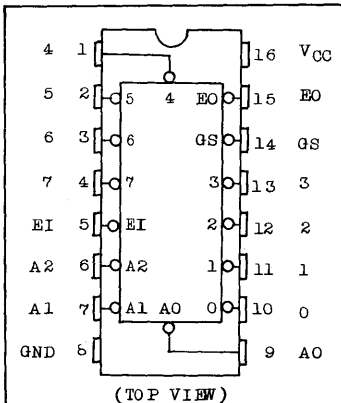
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

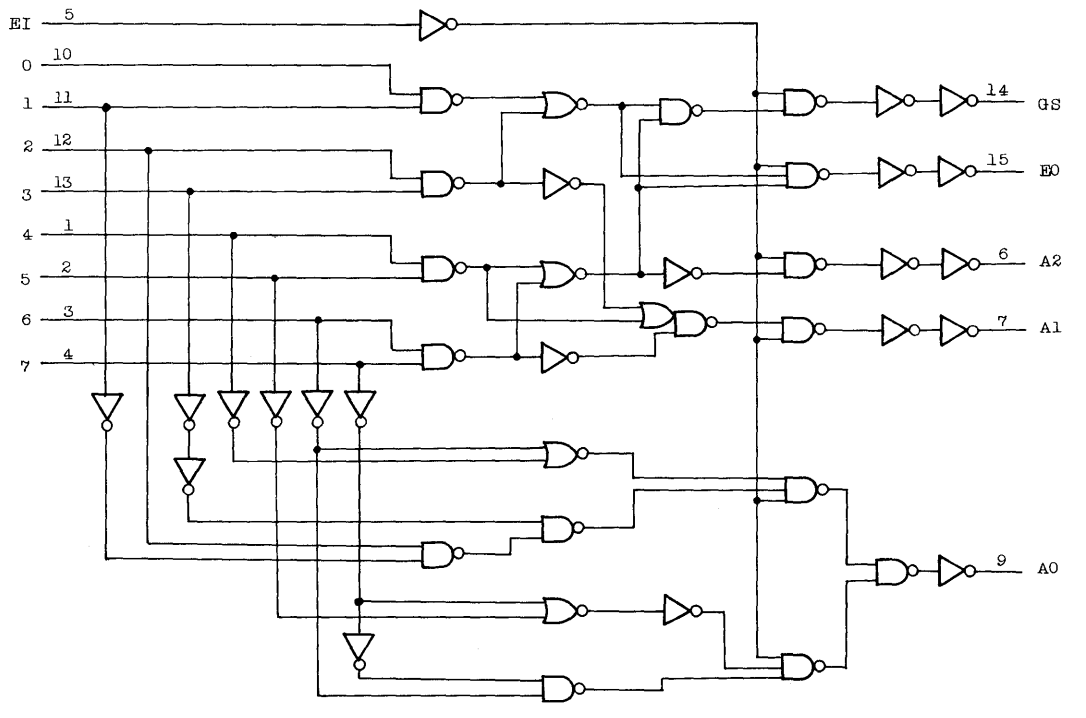
TC74HC148P

TRUTH TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

X : Don't Care

LOGIC DIAGRAM

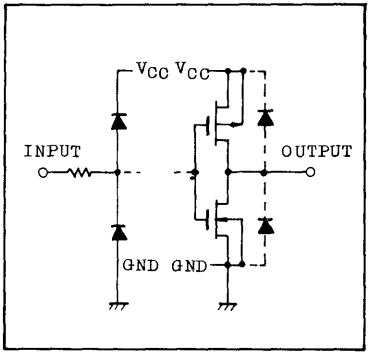


TC74HC148P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC148P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

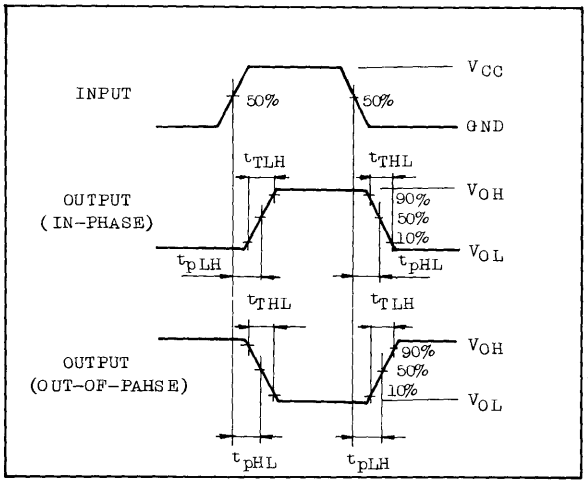
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (IN - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (IN - EO, GS)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (EI - EO)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (EI - GS)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Propagation Delay Time (EI - A0, A1, A2)	t_{pLH} t_{pHL}		2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Input Capacitance	C_{IN}			-	5	10		10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	57	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

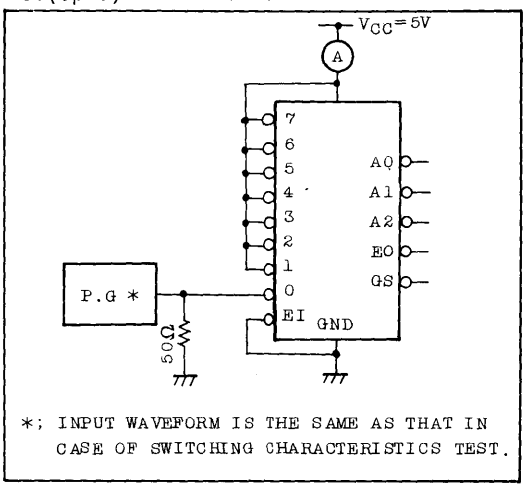
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN}$$

TC74HC148P

SWITCHING CHARACTERISTICS TEST WAVEFORM



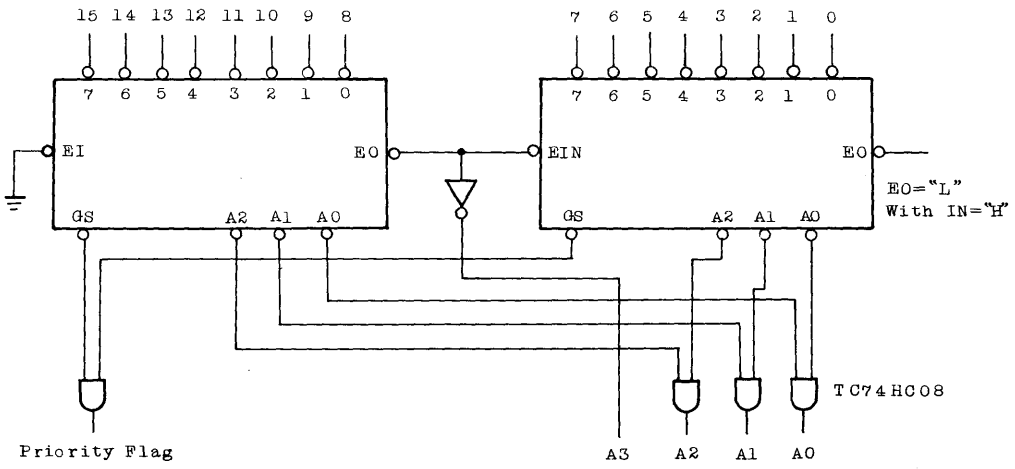
I_{CC}(Opr.) TEST WAVEFORM



*; INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TYPICAL APPLICATION

4-bit CASCADE CONNECTION



TC74HC151P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

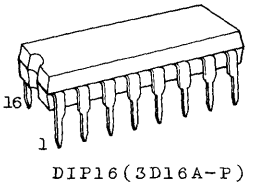
PRELIMINARY

TC74HC151P/F 8-CHANNEL MULTIPLEXER

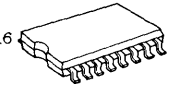
The TC74HC151 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. One of the eight data input signal (D0 - D7) is selected by a three-bit address input (A, B, C) and the selected data will be provided on two outputs; a non-invering output (Y) and a invering output (W). A strobe input is provided to control the output conditions; a low level on the strobe input brings the selected data on the outputs. On the other hand a high level on the strobe input provides the low level with Y output and the high level with W output without regard to the other input conditions.
All outputs are equipped protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS151



DIP16(3D16A-P)



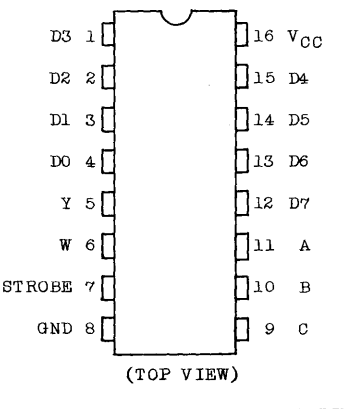
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

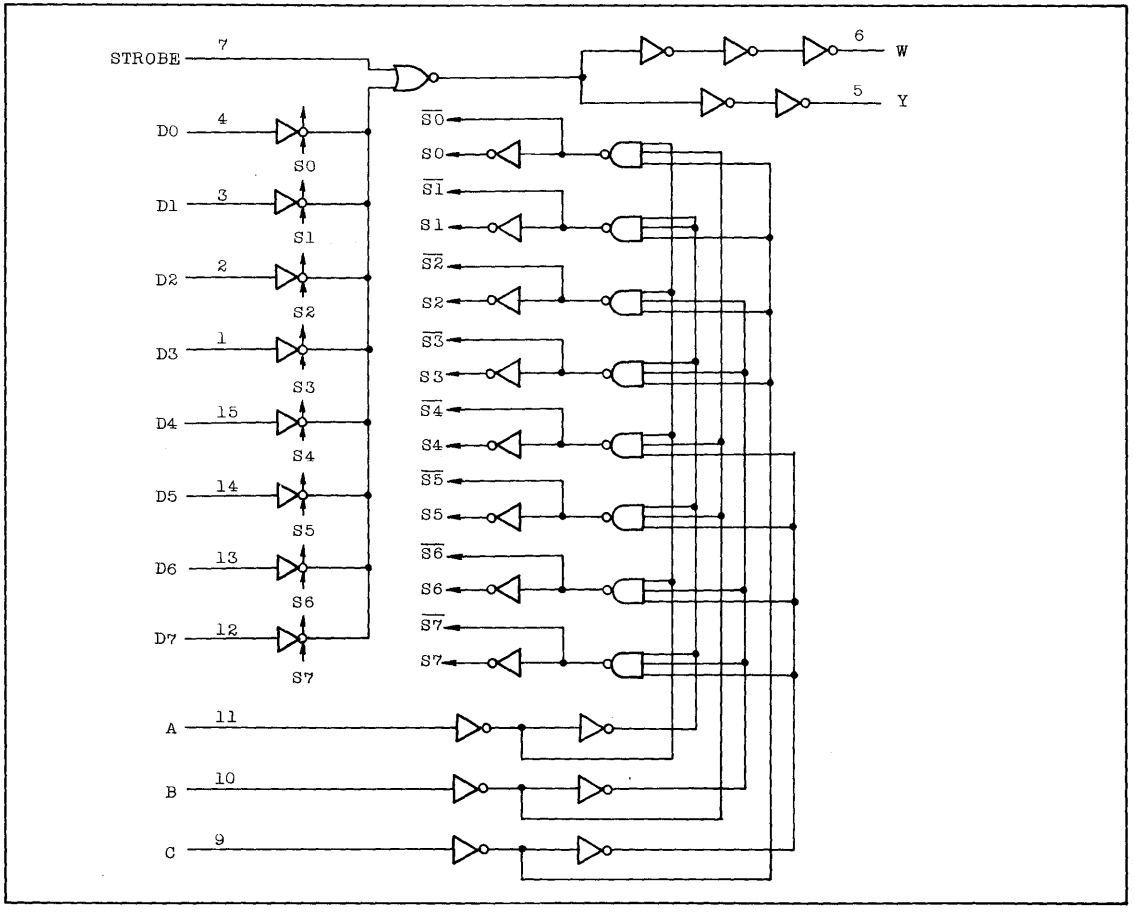
TC74HC151P/F

TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

X : Don't Care

LOGIC DIAGRAM

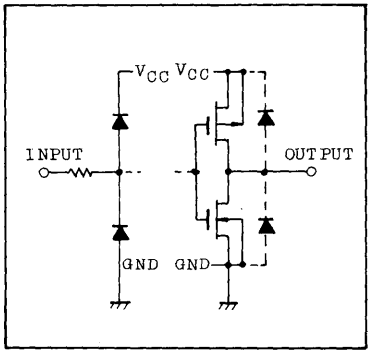


TC74HC151P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6nS)

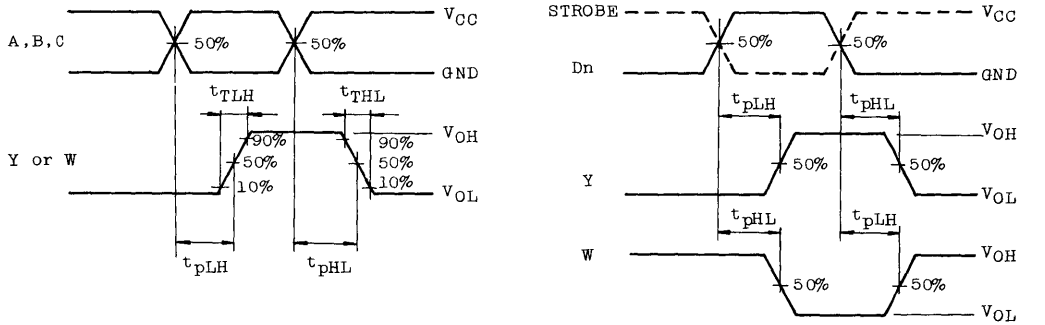
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (D - W)	t_{pLH}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
	t_{pHL}		6.0	-	18	28	-	35	
Propagation Delay Time (D - Y)	t_{pLH}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
	t_{pHL}		6.0	-	17	27	-	34	
Propagation Delay Time (ST - W)	t_{pLH}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
	t_{pHL}		6.0	-	12	20	-	25	
Propagation Delay Time (ST - Y)	t_{pLH}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
	t_{pHL}		6.0	-	11	18	-	22	
Propagation Delay Time (A, B, C - W)	t_{pLH}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
	t_{pHL}		6.0	-	22	35	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
	t_{pHL}		6.0	-	21	33	-	42	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	75	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

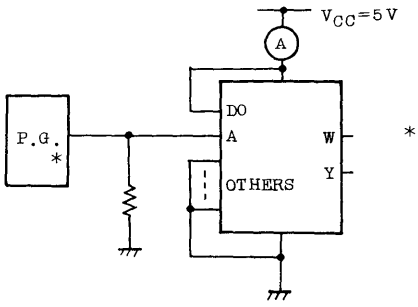
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC151P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC153P/F
TC74HC253P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC153P/F DUAL 4-CHANNEL MULTIPLEXER

TC74HC253P/F DUAL 4-CHANNEL MULTIPLEXER WITH 3-STATE OUTPUT

The TC74HC153 and TC74HC253 are high speed CMOS DUAL 4-CHANNEL MULTIPLEXERs fabricated with silicon gate C²MOS technology.

Both achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipations.

The designer has a choice of complementary output (HC153) and 3-state output (HC253).

Each of these data (1C0-1C3, 2C0-2C3) is selected by the two address inputs A and B.

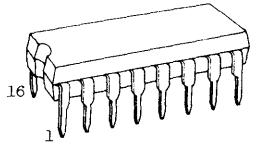
Separate strobe inputs ($1\overline{G}$, $2\overline{G}$) are provided for each of the two four-line sections.

The strobe input ($\overline{G}$) can be used to inhibit the data output; the output of HC153 is fixed in low level and the output of HC253 is disabled to be high impedance unconditionally, while the strobe input is held low.

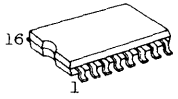
All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS157/158.



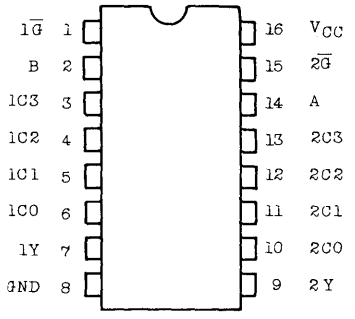
DIP16(3D16A-P)



MFP16(F16GC-P)

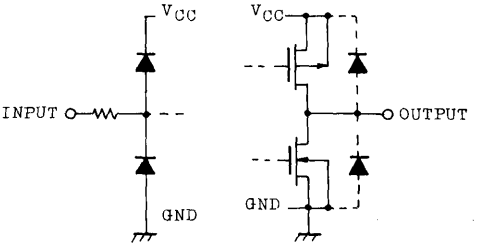
TC74HC153P/F
TC74HC253P/F

PIN ASSIGNMENT



(Top View)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TRUTH TABLE

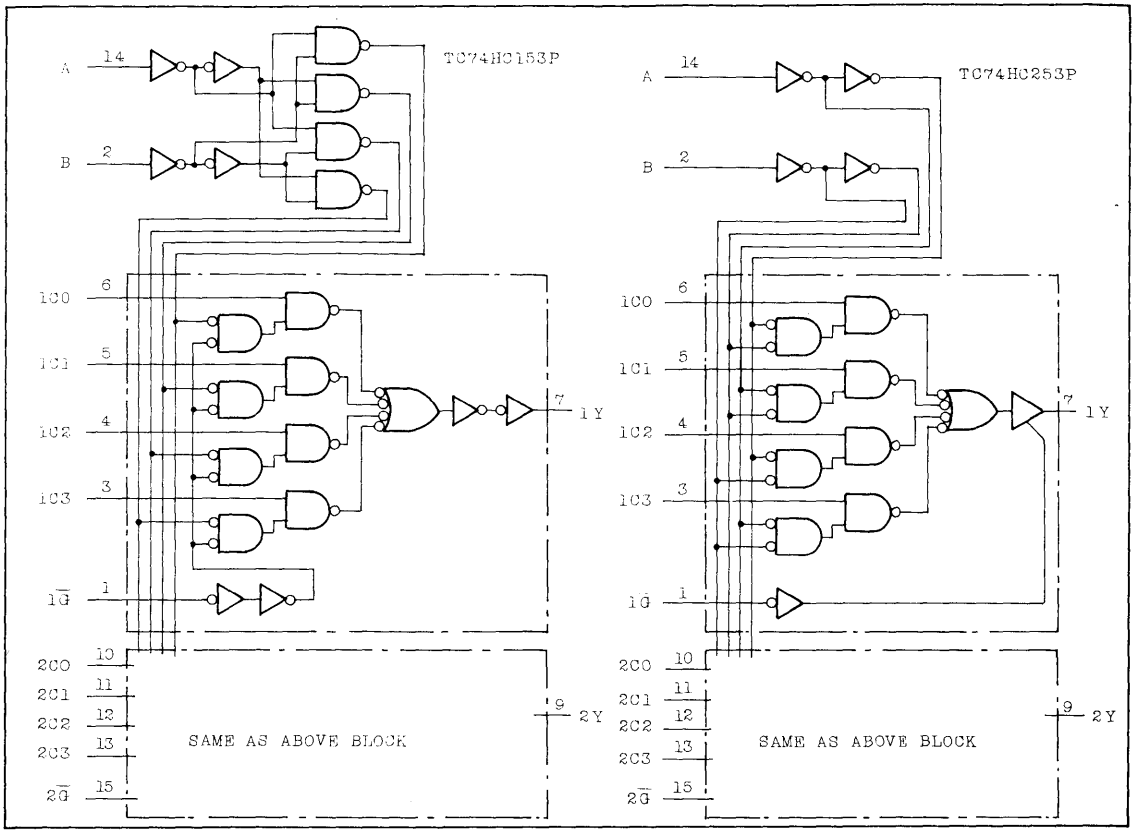
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT Y	
B	A	C_0	C_1	C_2	C_3	$\overline{G}$	HC153	HC253
X	X	X	X	X	X	H	L	Z
L	L	L	X	X	X	L	L	L
L	L	H	X	X	X	L	H	H
L	H	X	L	X	X	L	L	L
L	H	X	H	X	X	L	H	H
H	L	X	X	L	X	L	L	L
H	L	X	X	H	X	L	H	H
H	H	X	X	X	L	L	L	L
H	H	X	X	X	H	L	H	H

X : Don't care

Z : High Impedance

TC74HC153P/F
TC74HC253P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC153P/F
TC74HC253P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}(1)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

Note (1) Applied only for TC74HC253P

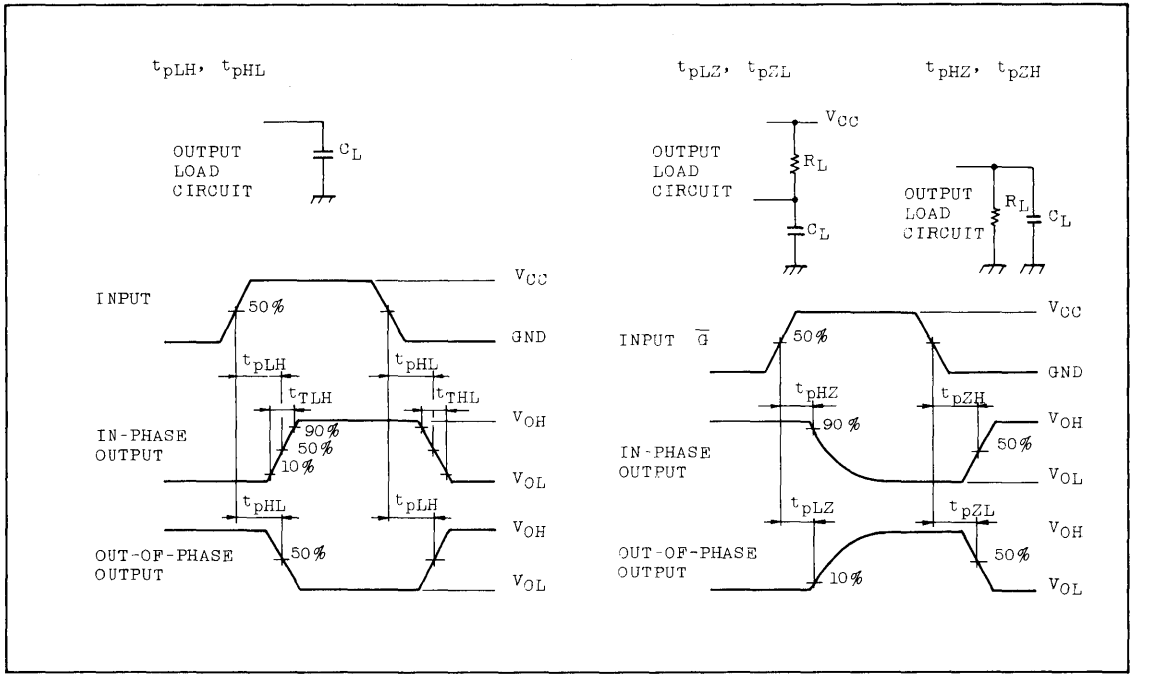
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	75	-	95	ns
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
TC74HC153/253 Propagation Delay Time C_n - Y	t_{pLH} t_{pHL}		2.0	-	68	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
TC74HC153/253 A,B - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC153 Propagation Delay Time G - Y	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
TC74HC253 Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	46	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
TC74HC253 Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	TC74HC253		-	7	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC153		-	56	-	-	-	
		TC74HC253		-	56	-	-	-	

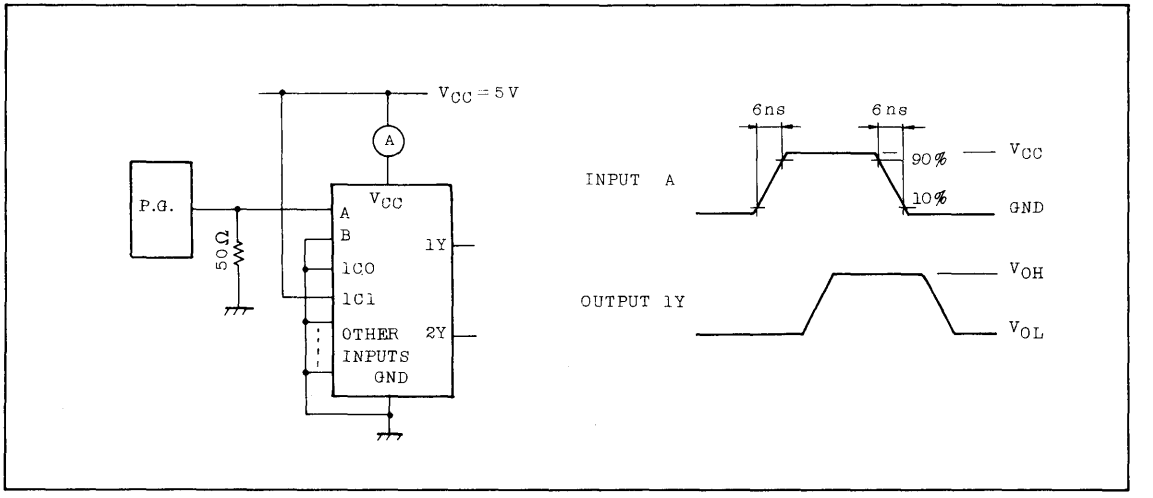
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Channel)

TC74HC153P/F
TC74HC253P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC154P

PRELIMINARY

TC74HC154P 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

The TC74HC154 is a high speed CMOS 4-LINE TO 16-LINE DECODER/DEMULTIPLEXER fabricated with silicon gate CMOS technology.

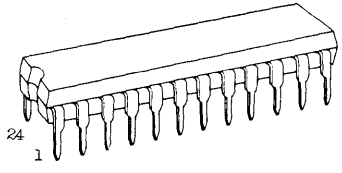
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

A binary code applied to the four inputs (A thru D) provides a low level at the selected one of sixteen outputs excluding the other fifteen outputs, when both the strobe inputs, $\overline{G1}$ and $\overline{G2}$, are held low.

When either strobe input is held high, the decording function is inhibited to keep all outputs high.

The strobe function makes it easy to expand the decoding lines through cascading, and simplifies the design of address decording circuit in the memory control system.

All inputs are equipped with protection circuit against static discharge or transient excess voltage.

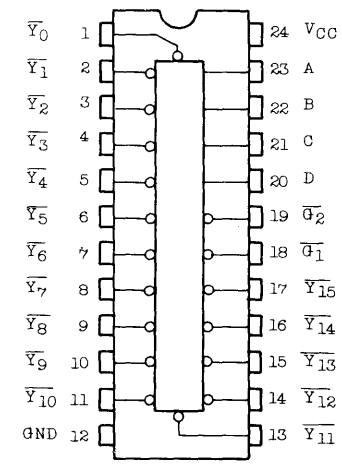


DIP24-300A-P)
0.300 INCH (7.62) ROW SPACING

FEATURES:

- High Speed.....t_{pd}=22ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS154
- Small Package.....0.300(7.62) Row Spacing

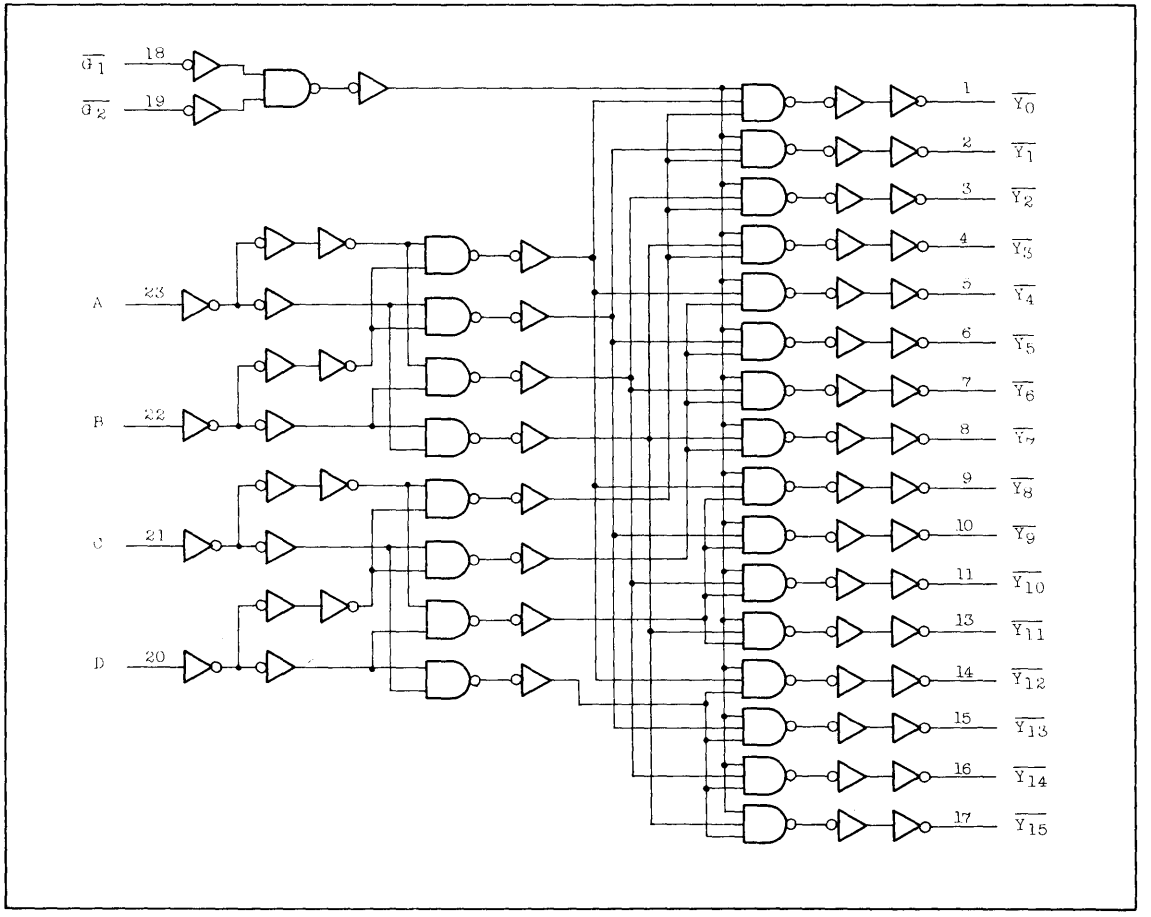
PIN ASSIGNMENT



(Top View)

TC74HC154P

LOGIC DIAGRAM



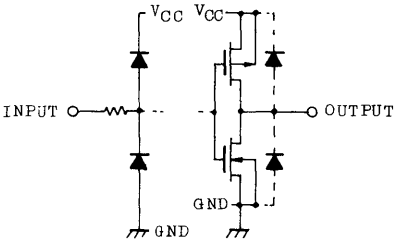
TC74HC154P

TRUTH TABLE

INPUTS						SELECTED OUTPUT (L)
$\overline{G}_1$	$\overline{G}_2$	D	C	B	A	
L	L	L	L	L	L	$\overline{Y}_0$
L	L	L	L	L	H	$\overline{Y}_1$
L	L	L	L	H	L	$\overline{Y}_2$
L	L	L	L	H	H	$\overline{Y}_3$
L	L	L	H	L	L	$\overline{Y}_4$
L	L	L	H	L	H	$\overline{Y}_5$
L	L	L	H	H	L	$\overline{Y}_6$
L	L	L	H	H	H	$\overline{Y}_7$
L	L	H	L	L	L	$\overline{Y}_8$
L	L	H	L	L	H	$\overline{Y}_9$
L	L	H	L	H	L	$\overline{Y}_{10}$
L	L	H	L	H	H	$\overline{Y}_{11}$
L	L	H	H	L	L	$\overline{Y}_{12}$
L	L	H	H	L	H	$\overline{Y}_{13}$
L	L	H	H	H	L	$\overline{Y}_{14}$
L	L	H	H	H	H	$\overline{Y}_{15}$
X	H	X	X	X	X	NONE
H	X	X	X	X	X	NONE

X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC154P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

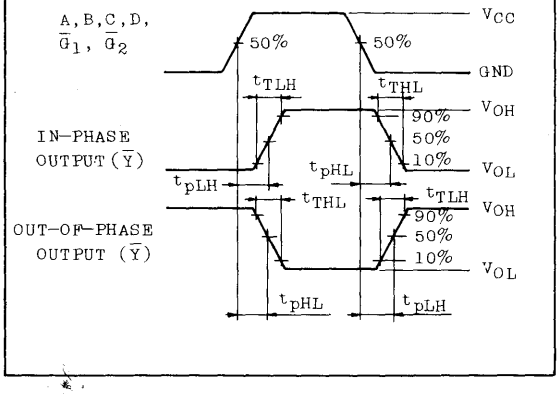
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, B, C, D - $\overline{Y}$)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	ns
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time ($\overline{G}_1$, $\overline{G}_2$ - Y)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	ns
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

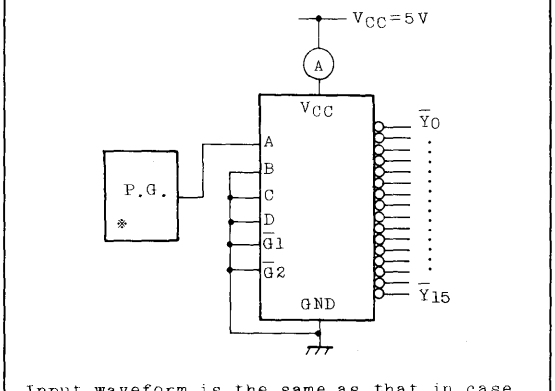
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC155P

C²MOS DIGITAL INTEGRATED CIRCUIT

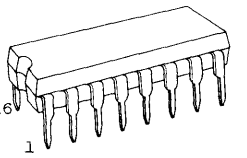
PRELIMINARY

TC74HC155P DUAL 2-TO-4 LINE DECODER/3-TO-8 LINE DECODER

The TC74HC155 is a high speed CMOS 2-TO-4 LINE DECODER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It features dual 1-TO-4 line demultiplexers with individual strobe inputs (1G and $\overline{2G}$), individual data inputs (1C and $\overline{2C}$) and common binary address inputs (A and B). When both decoders are enabled by the strobes, the inverted output of 1C data and non-inverted output of $\overline{2C}$ data will be brought to the selected output pins of each sections. A 1-TO-8 line demultiplexer will be also easily built up by providing a data signal to both 1C and $\overline{2C}$ inputs; the output order from significance bit is $\overline{1Y3}$, $\overline{1Y2}$, $\overline{1Y1}$, $\overline{1Y0}$, $\overline{2Y3}$, $\overline{2Y2}$, $\overline{2Y1}$, $\overline{2Y0}$ (BOTTOM). This device can be used as a 2-to-4 line decoder or a 3-to-8 line decoder when 1C is held high and $\overline{2C}$ is held low. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ~ 6V
- Pin and Function Compatible with 74LS155



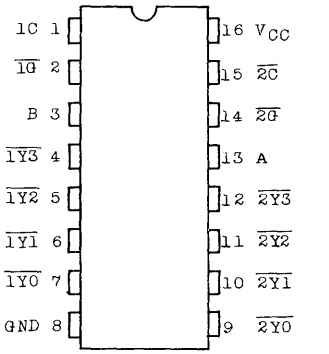
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ~ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC155P

TRUTH TABLE

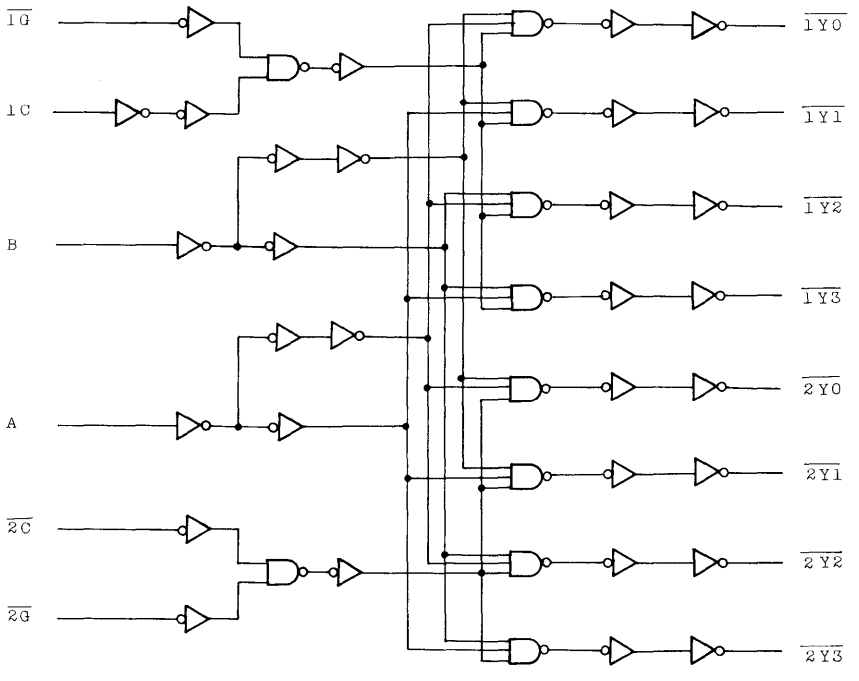
INPUTS				OUTPUTS			
B	A	$\overline{1G}$	1C	$\overline{1Y0}$	$\overline{1Y1}$	$\overline{1Y2}$	$\overline{1Y3}$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

X : DON'T CARE

INPUTS				OUTPUTS			
B	A	$\overline{2G}$	$\overline{2C}$	$\overline{2Y0}$	$\overline{2Y1}$	$\overline{2Y3}$	$\overline{2Y3}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

X : DON'T CARE

LOGIC DIAGRAM

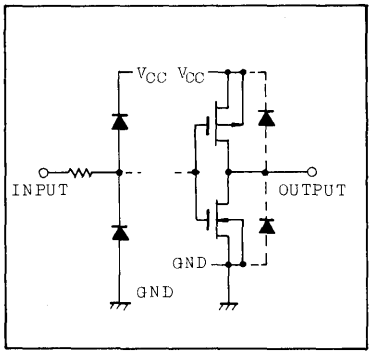


TC74HC155P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

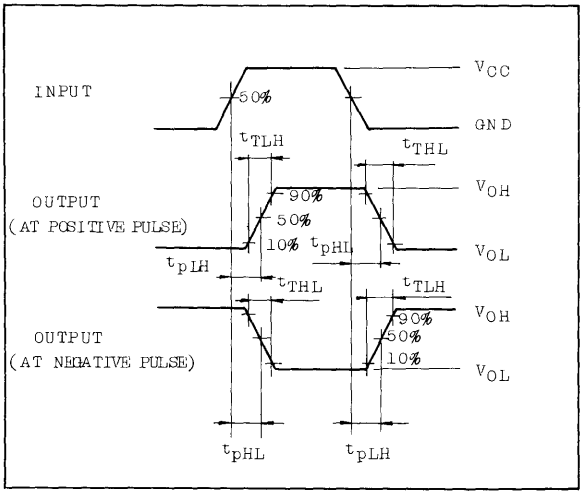
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	65	-	-	-	

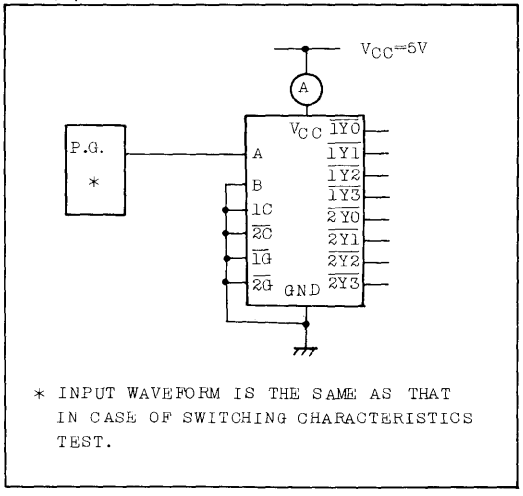
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC157P/F
TC74HC158P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

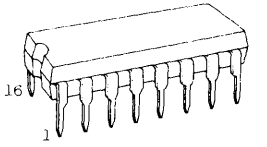
TC74HC157P/F QUAD 2-CHANNEL MULTIPLEXER

TC74HC158P/F QUAD 2-CHANNEL MULTIPLEXER (INVERTING)

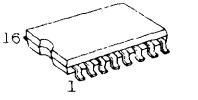
The TC74HC157 and the TC74HC158 are high speed CMOS QUAD 2-CHANNEL MULTIPLEXER's fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low Power dissipation.
These devices consist of four 2-input digital multiplexers with common select and strobe inputs.
The TC74HC158 is an inverting multiplexer while the TC74HC157 is a non-inverting multiplexer.
When the $\overline{\text{STROBE}}$ input is held "H" level, selection of data is inhibited and all the outputs become "L" level in case of 157 and all the outputs become "H" level in case of 158.
The SELECT decoding determines whether the A or B inputs get routed to their corresponding Y outputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS157/158.



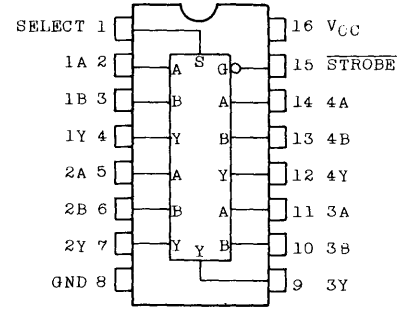
DIP16(3D16A-P)



MFP16(F16GC-P)

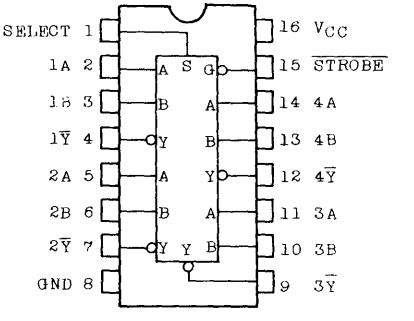
PIN ASSIGNMENT

TC74HC157



(TOP VIEW)

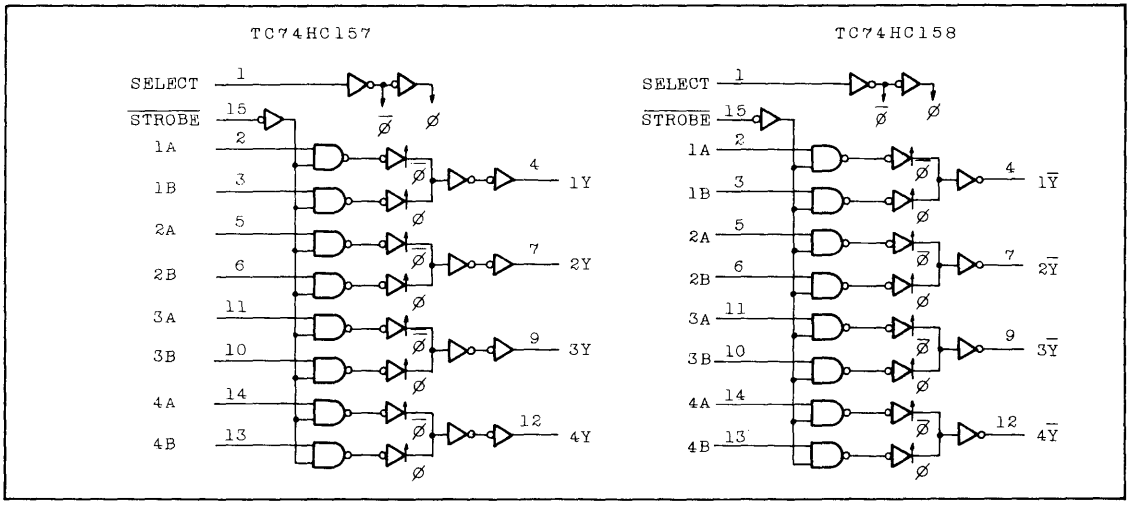
TC74HC158



(TOP VIEW)

TC74HC157P/F
TC74HC158P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{\text{STROBE}}$	SELECT	A	B	Y (157)	$\overline{\text{Y}}$ (158)
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

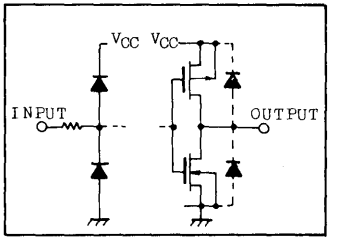
* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC157P/F
TC74HC158P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC157P/F
TC74HC158P/F

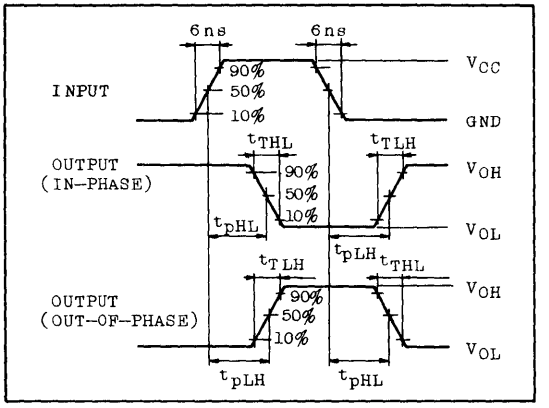
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
TC74HC157 Propagation Delay Time A,B -Y	t_{pLH} t_{pHL}		2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
SELECT - Y	t_{pLH} t_{pHL}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
$\overline{STROBE}$ - Y	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
TC74HC158 Propagation Delay Time A,B - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	46	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
SELECT - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
$\overline{STROBE}$ - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Input Capacitance	C_{IN}			-	6	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC157		-	53	-	-	-	
		TC74HC257		-	51	-	-	-	

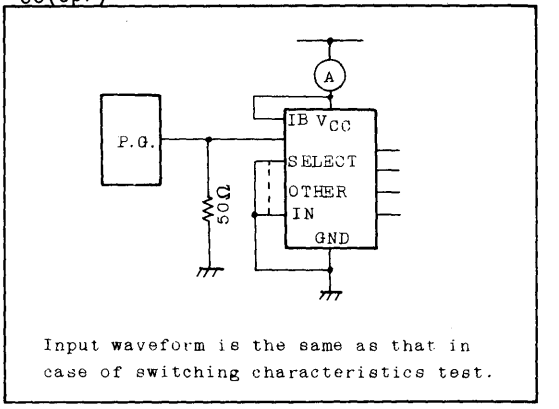
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Channel)

TC74HC157P/F
TC74HC158P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC160P/F • TC74HC161P/F
TC74HC162P/F • TC74HC163P/F

PRELIMINARY

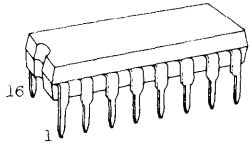
SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

TC74HC160P/F DECADE, ASYNCHRONOUS CLEAR
TC74HC161P/F BINARY, ASYNCHRONOUS CLEAR
TC74HC162P DECADE, SYNCHRONOUS CLEAR
TC74HC163P/F BINARY, SYNCHRONOUS CLEAR

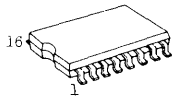
The TC74HC160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC160/162 are BCD decode counters and the TC74HC161/163 are 4 bit binary counters.
The CLOCK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLEAR}$ inputs are active on "L" level.
Presetting of all four IC's is synchronous to the rising edge of CLOCK.
Clear function on the TC74HC162/163 is synchronous to CLOCK, while the TC74HC160/161 counters are cleared asynchronously.
Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilitates easy implementation of N-bit counters without using external gate.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=50MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS160 ~163.

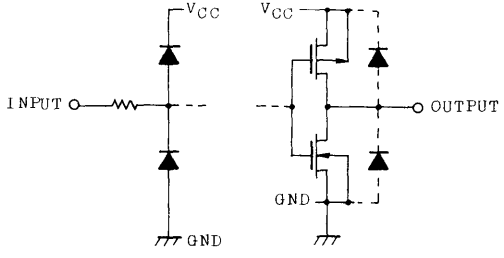


DIP16(3D16A-P)

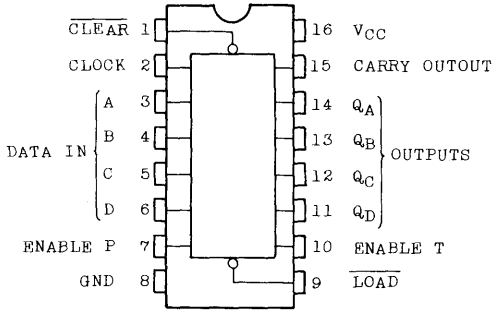


MFP16(F16GC-P)

INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGNMENT



(TOP VIEW)

TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

TRUTH TABLE

TC74HC160/161					TC74HC162/163					OUTPUTS				FUNCTION
INPUTS					INPUTS									
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	↓	L	L	L	L	RESET TO "0"
H	L	X	X	↓	H	L	X	X	↓	A	B	C	D	PRESET DATA
H	H	X	L	↓	H	H	X	L	↓	NO CHANGE				NO COUNT
H	H	L	X	↓	H	H	L	X	↓	NO CHANGE				NO COUNT
H	H	H	H	↓	H	H	H	H	↓	COUNT UP				COUNT
H	X	X	X	↑	X	X	X	X	↑	NO CHANGE				NO COUNT

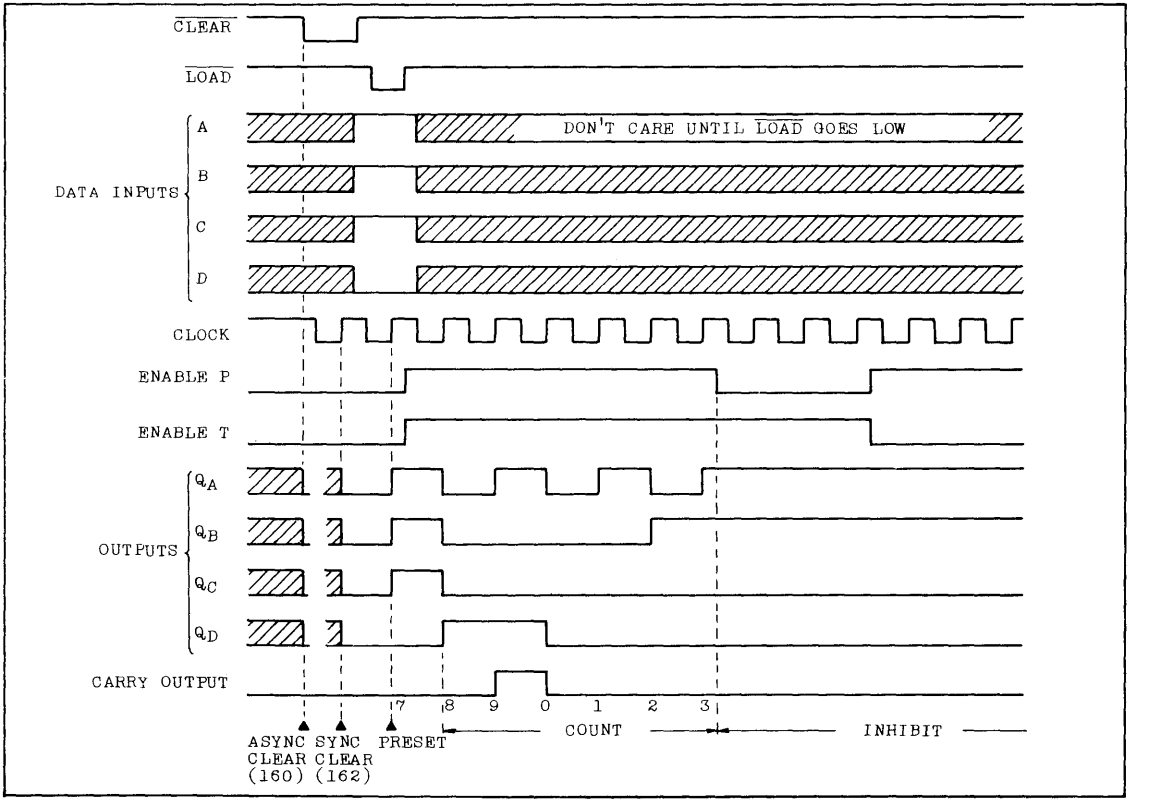
Note X ; Don't Care

A, B, C, D ; Logic level of data inputs

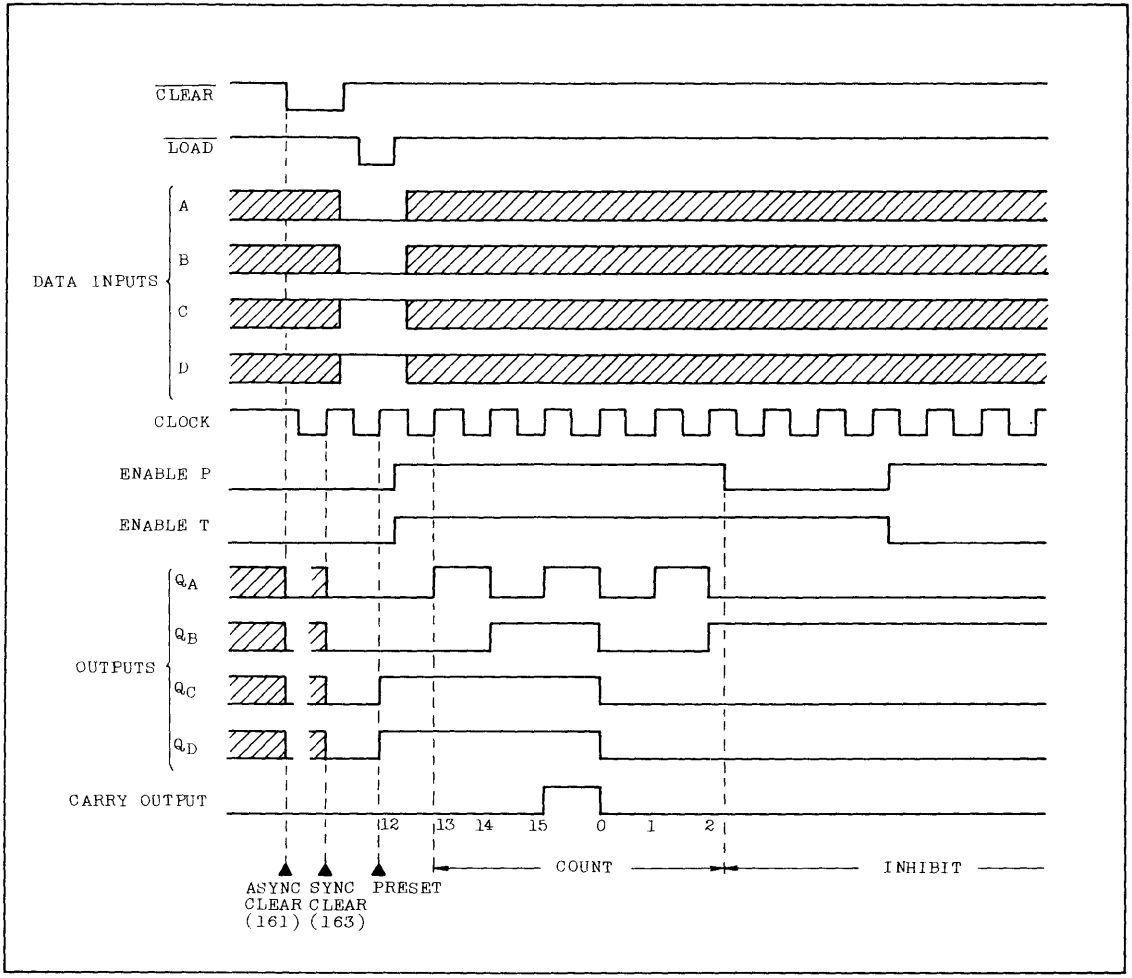
Carry ; $CARRY = TE \cdot Q_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot Q_D$ ····· (TC74HC160/162)

$CARRY = TE \cdot Q_A \cdot Q_B \cdot Q_C \cdot Q_D$ ····· (TC74HC161/163)

TIMING CHART (TC74HC160/162 : DECADE COUNTER)

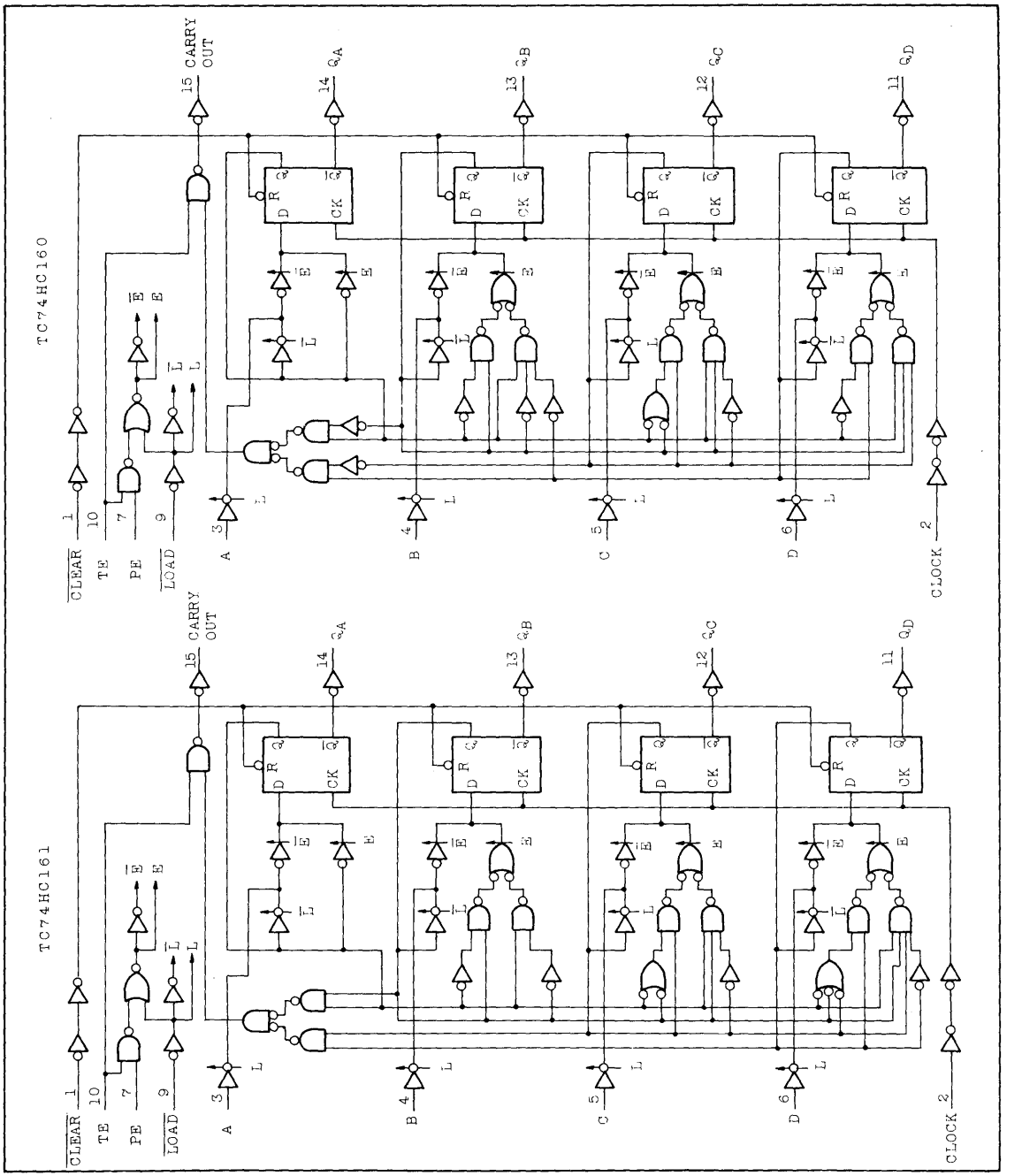


TIMING CHART (TC74HC161/163 : BINARY COUNTER)



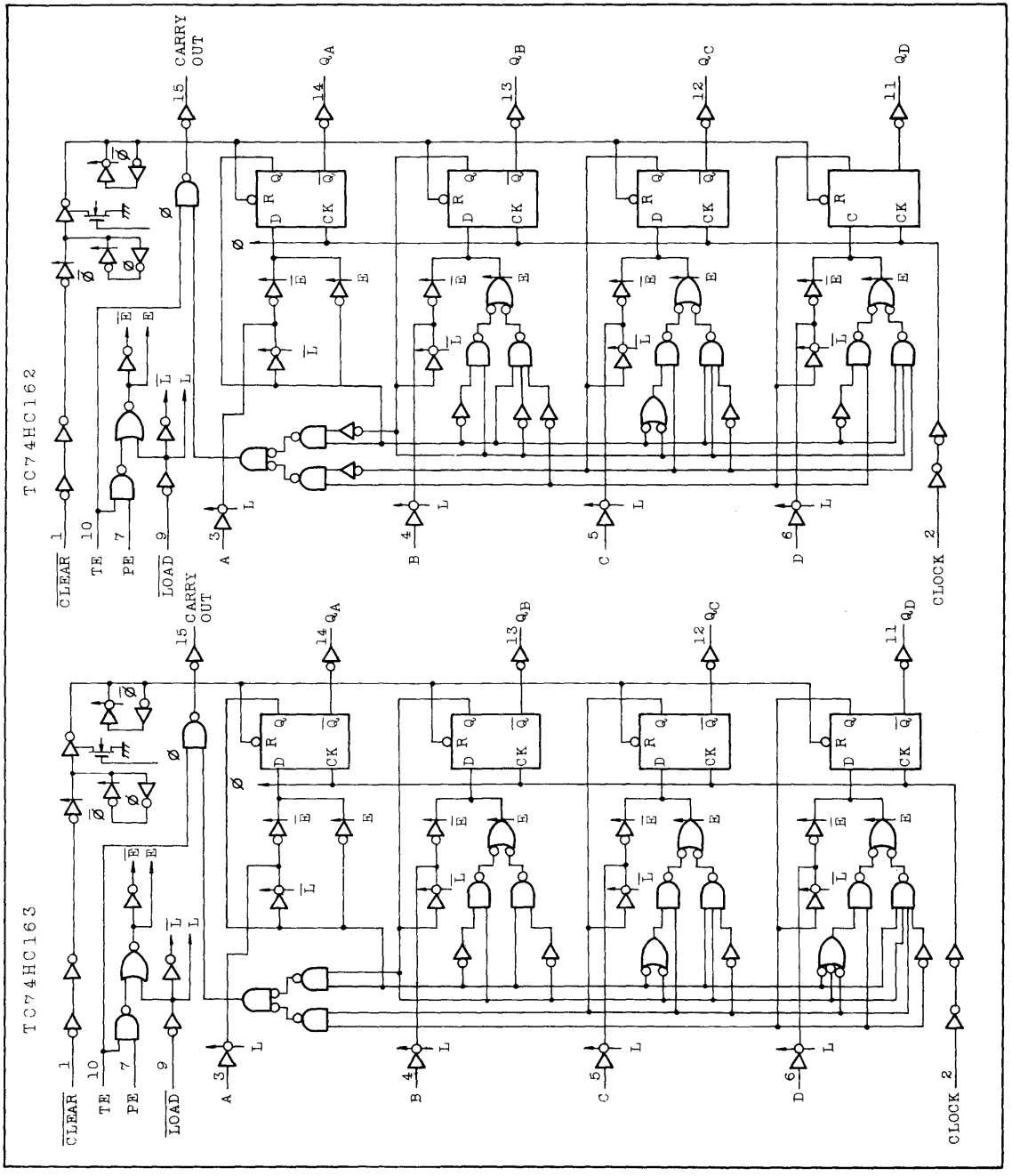
TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

LOGIC DIAGRAM



TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

LOGIC DIAGRAM



TC74HC160P/F • TC74H161P/F
TC74HC162P/F • TC74H163P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	88	165	-	205	
			4.5	-	22	33	-	41	
			6.0	-	19	28	-	35	
CLOCK - CARRY	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
TE - CARRY	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
$\overline{\text{CLEAR}}$ - Q*	t_{pHL}		2.0	-	100	185	-	230	
			4.5	-	25	37	-	46	
			6.0	-	21	31	-	39	
$\overline{\text{CLEAR}}$ - CARRY*	t_{pHL}		2.0	-	112	210	-	265	
			4.5	-	28	42	-	53	
			6.0	-	24	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	45	-	22	-	
			6.0	32	53	-	26	-	

TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
$\overline{CLEAR}$ *	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time $\overline{LOAD}$, PE, TE	t_s		2.0	-	50	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
A, B, C, D	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
$\overline{CLEAR}$ **	t_s		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{CLEAR}$ *	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Input Capacitance	C_{IN}			-	5	7.5	-	7.5	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	57	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

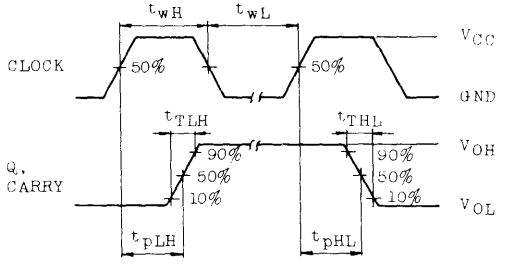
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

(2) * for TC74HC160/161 only
** for TC74HC162/163 only

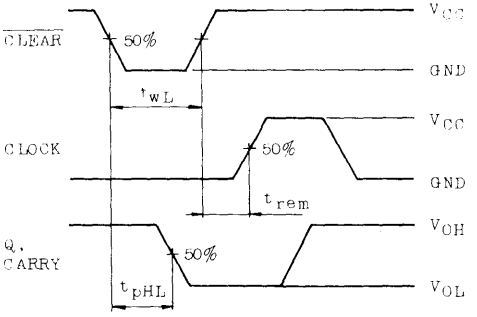
TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

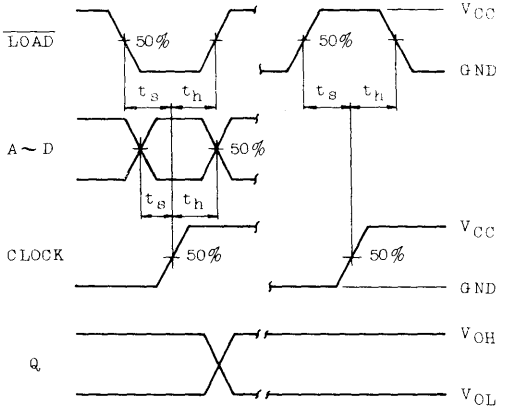
COUNT MODE



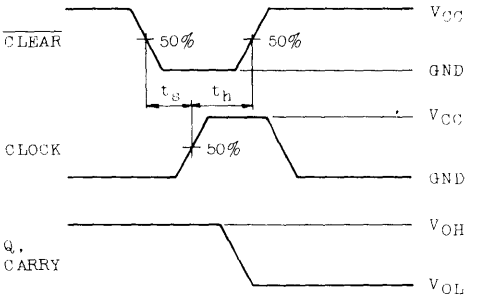
CLEAR MODE (TC74HC160P/161P)



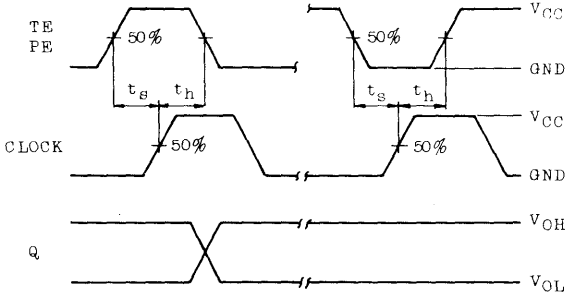
PRESET MODE



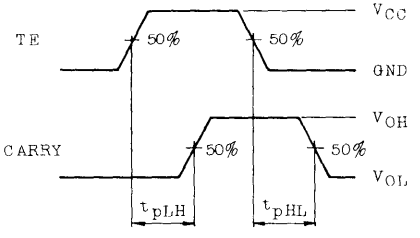
CLEAR MODE (TC74HC162P/163P)



COUNT ENABLE MODE

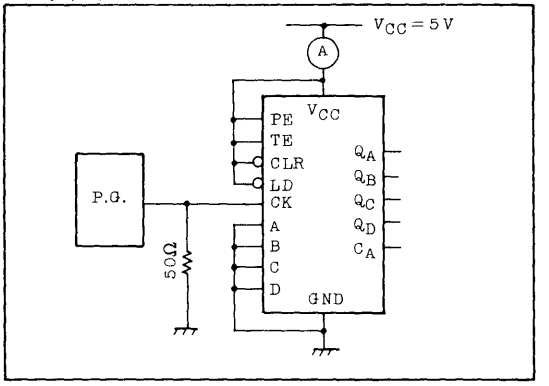


CASCADE MODE
(Fix Maximum Count)



TC74HC160P/F•TC74H161P/F
TC74HC162P/F•TC74H163P/F

$I_{CC(opr)}$ TEST CIRCUIT



OPERATING CURRENT CONSUMPTION WITH LOAD CAPACITANCE

When the outputs drive capacitive load, total current consumption is to be a sum of the value calculated from C_{PD} and ΔI_{CC} obtained from the following formula.

In case of TC74HC160/162

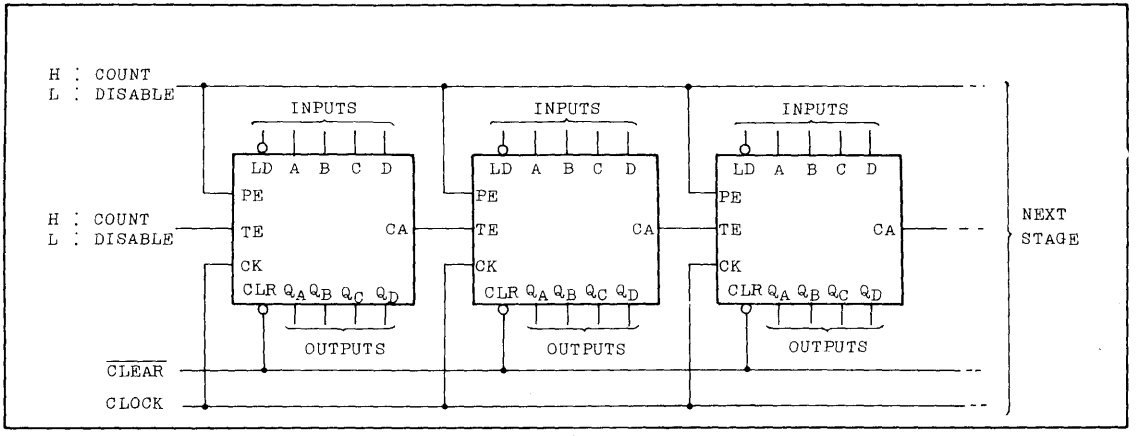
$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

In case of TC74HC161/163

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

$C_a \sim C_{ca}$ are the capacitance at $Q_A \sim$ CARRY output.

TYPICAL APPLICATION



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC164P/F

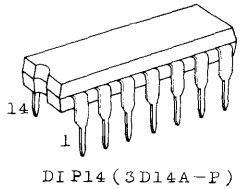
PRELIMINARY

TC74HC164P/F 8-BIT SHIFT REGISTER (S-IN, P-OUT)

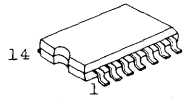
The TC74HC164 is a high speed CMOS 8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of serial-in, parallel-out 8-bit shift register with a clock inputs and an overriding clear input. Two serial data inputs (A, B) are provided so that one input may be used as a data enable.
Data is shifted serially through the shift register on the positive going transition of the clock input.
A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=50MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS164



DIP14(3D14A-P)



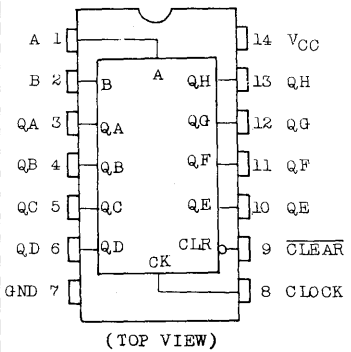
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC164P/F

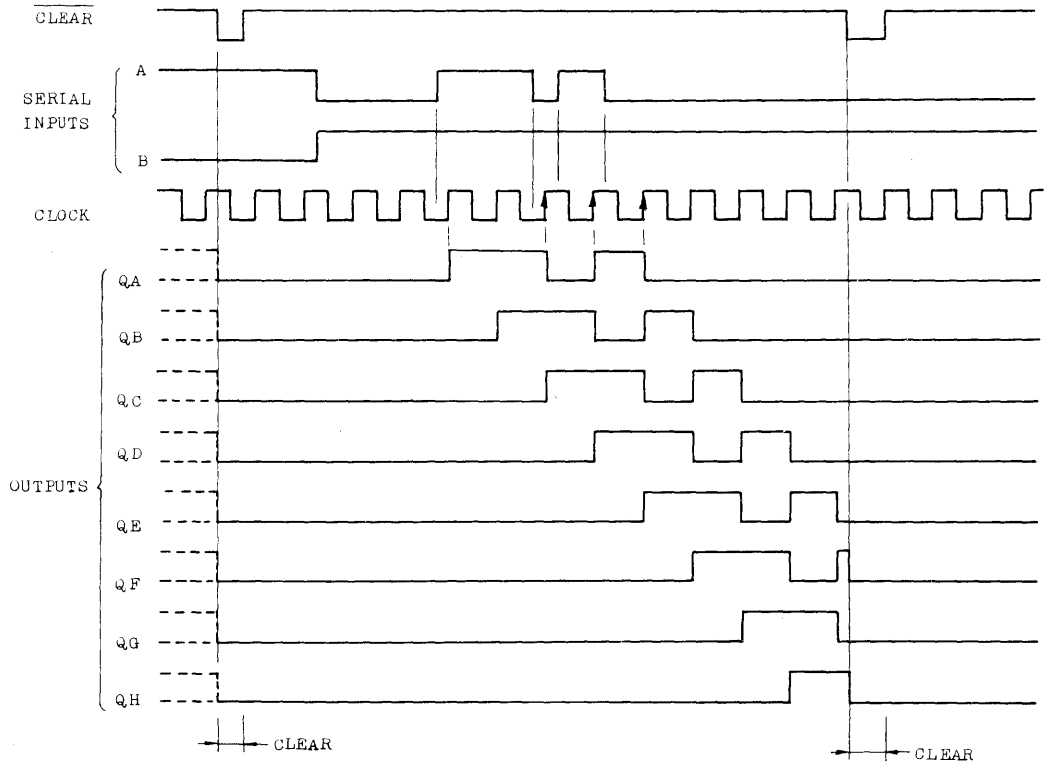
TRUTH TABLE

INPUTS				OUTPUTS			
$\overline{\text{CLEAR}}$	CLOCK	SERIAL IN		QA	QB	·····	QH
		A	B				
L	X	X	X	L	L	·····	L
H	↓	X	X	NO CHANGE			
H	↑	L	X	L	QAn	·····	QGn
H	↑	X	L	L	QAn	·····	QGn
H	↑	H	H	H	QAn	·····	QGn

X : DON'T CARE

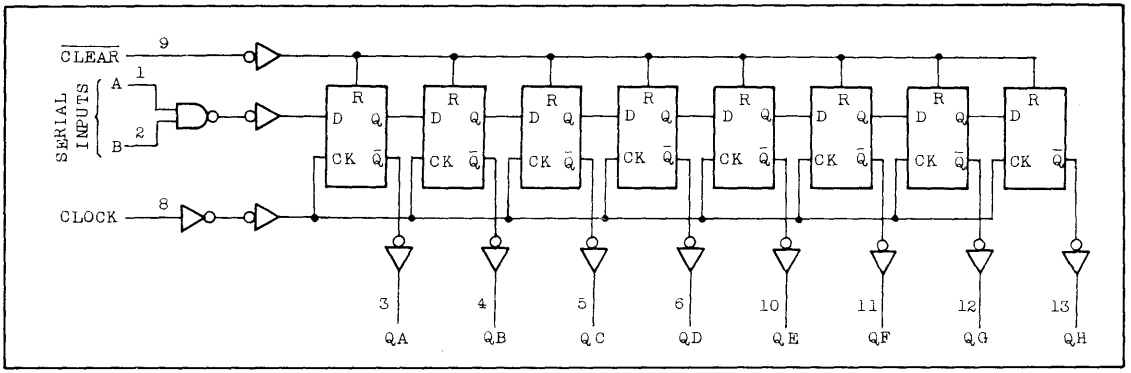
QAn~QGn : THE LEVEL OF QA~QG, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

TIMING CHART



TC74HC164P/F

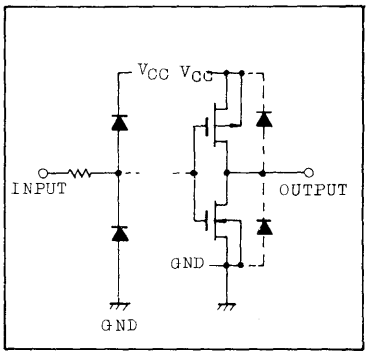
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC164P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn)	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	
Propagation Delay Time ($\overline{CLEAR}$ - Qn)	t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	46	-	22	-	
			6.0	32	54	-	26	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	96	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Set-up Time (A, B)	t_s		2.0	-	25	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	

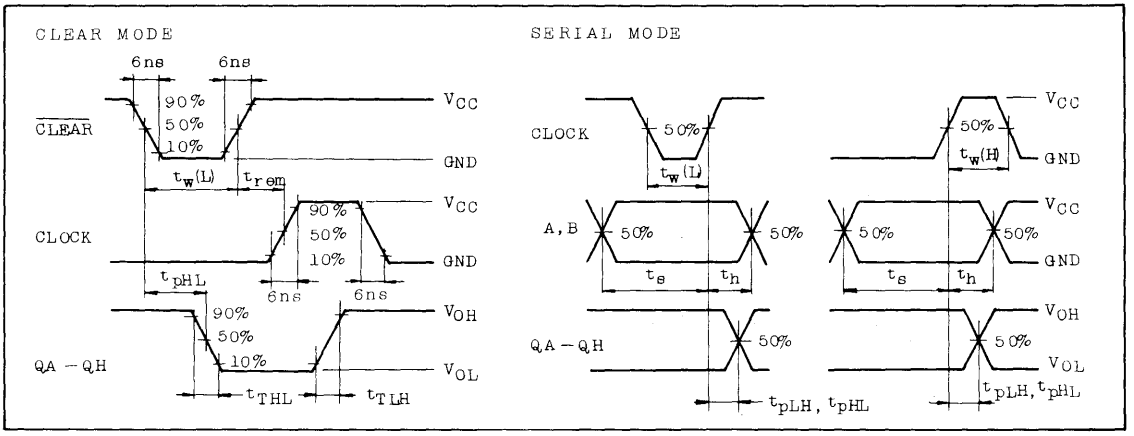
TC74HC164P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

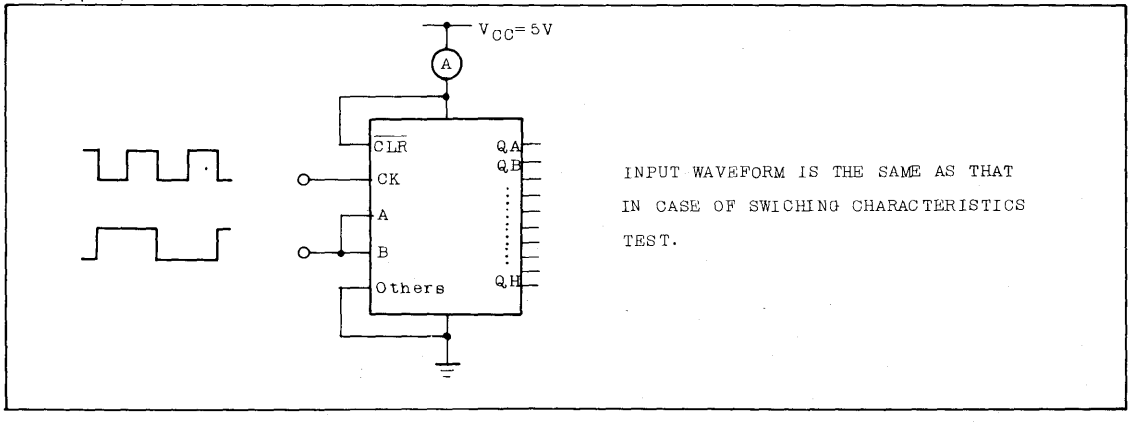
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Hold Time (A, B)	t_h		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	112	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



ICC(Opr.) TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWICHING CHARACTERISTICS TEST.

TC74HC165P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

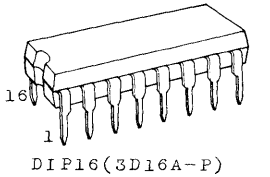
PRELIMINARY

TC74HC165P/F 8-BIT SHIFT REGISTER (P-IN, S-OUT)

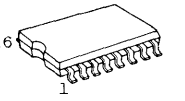
The TC74HC165 is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock input.
When the SHIFT/$\overline{LOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse.
When the SHIFT/$\overline{LOAD}$ input is held low, the parallel data is loaded asychronously into the register.
Clocking is accomplished on the positive going transition of the clock pulse.
The CLOCK-INHIBIT input should be changed to the high level only while the CLOCK input is held high.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=48MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delay ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS165



DIP16(3D16A-P)



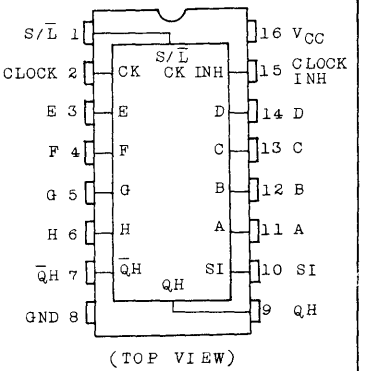
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

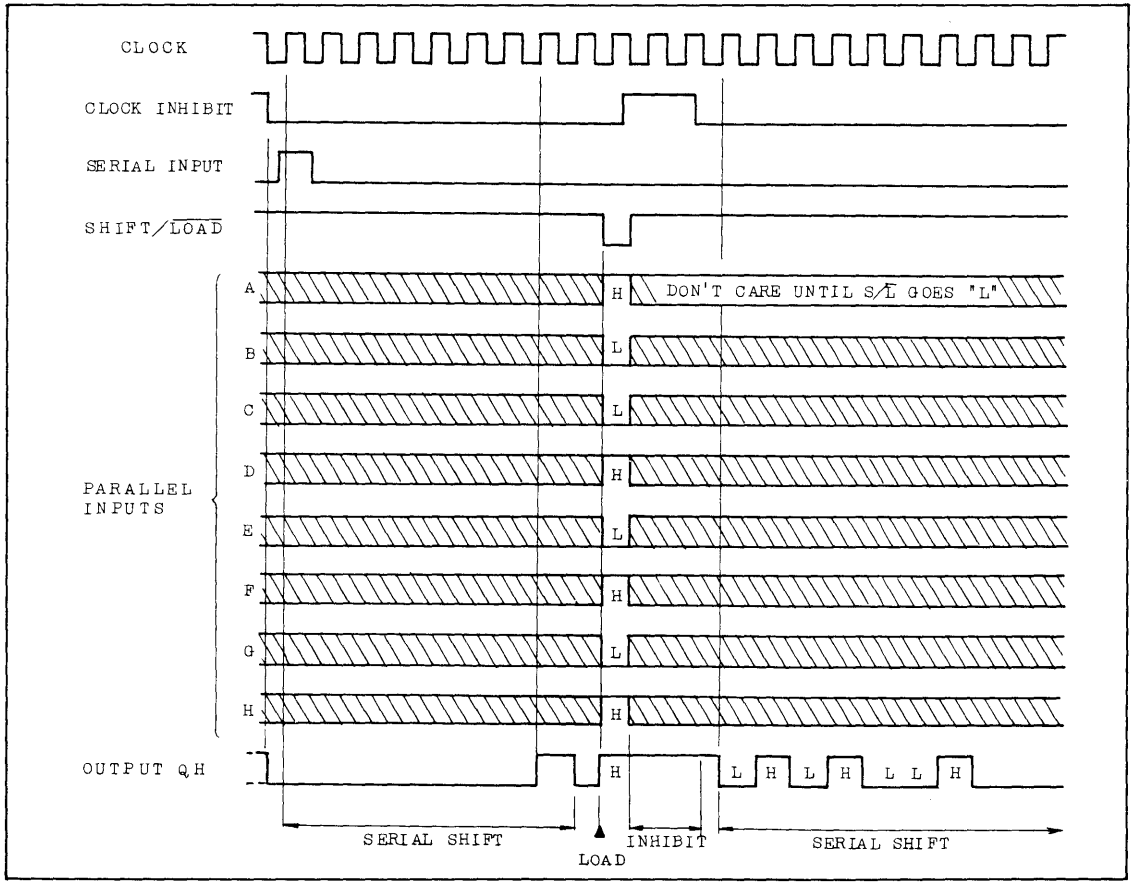
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/$\overline{\text{LOAD}}$	CLOCK INH	CLOCK	SERIAL IN	PARALLEL A ····· H	Q_A	Q_B	Q_H
L	X	X	X	a ····· h	a	b	h
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	L	H	X	H	Q_{An}	Q_{Gn}
H	↑	L	L	X	L	Q_{An}	Q_{Gn}
H	X	H	X	X	No change		
H	H	X	X	X	No change		

X : DON'T CARE

a ····· h : THE LEVEL OF STEADY INPUT VOLTAGE AT INPUTS A THROUGH H RESPECTIVELY

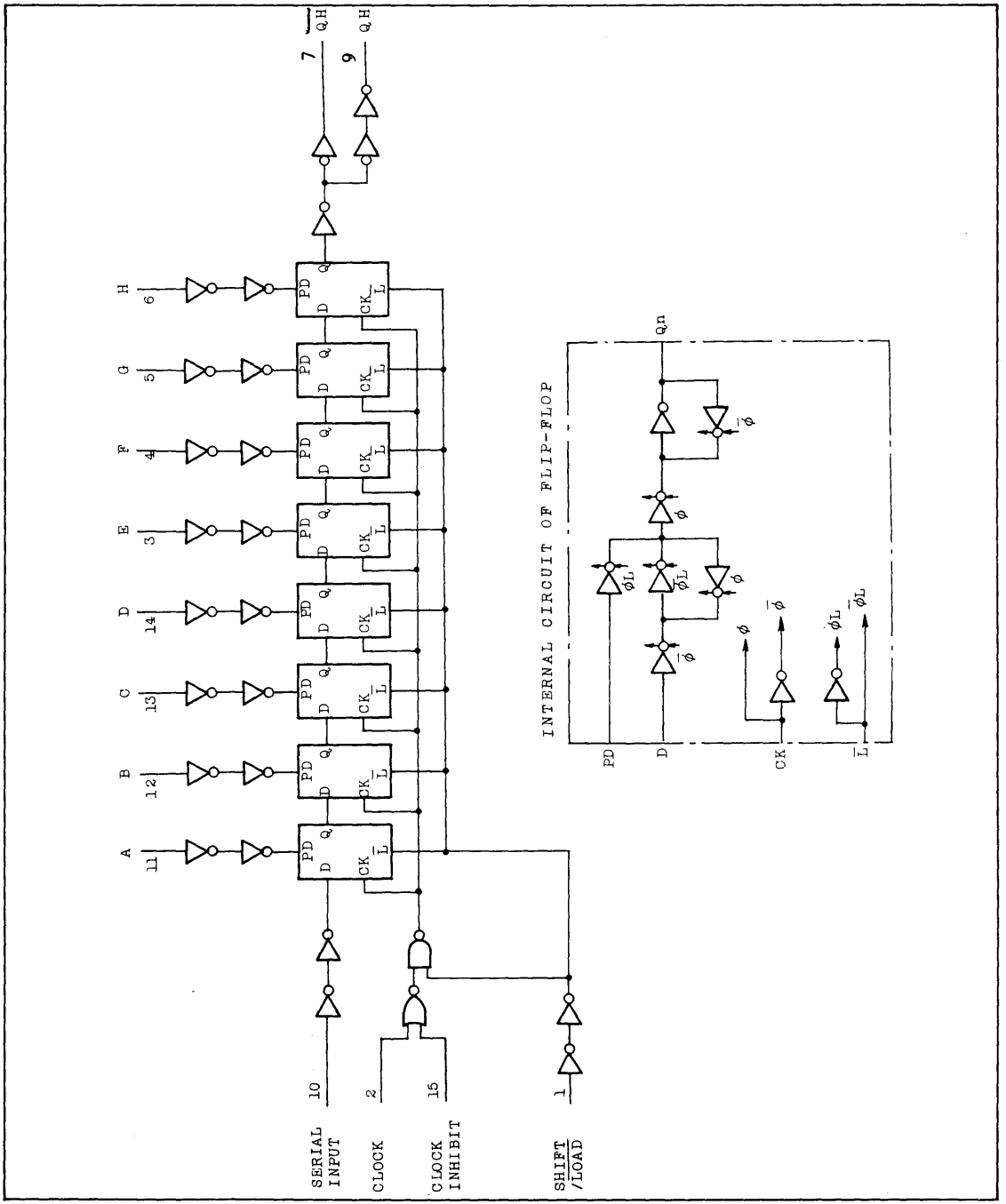
Q_{An} ··· Q_{Gn} : THE LEVEL OF Q_A~Q_G, RESPECTIVELY, BEFORE THE MOST-RECENT POSITIVE TRANSITION OF THE CLOCK.

TIMING CHART



TC74HC165P/F

LOGIC DIAGRAM

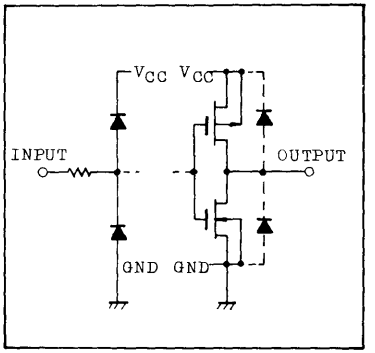


TC74HC165P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC165P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT tr=tf=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CK, CK INH - QH, $\overline{QH}$)	t_{pLH} t_{pHL}		2.0	-	96	190	-	240	
			4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Propagation Delay Time (S/$\overline{L}$ - QH, $\overline{QH}$)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (H - QH, $\overline{QH}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	25	44	-	20	-	
			6.0	29	52	-	24	-	
Minimum Pulse Width (CK, CK INH)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (S/$\overline{L}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (PI-S/$\overline{L}$)	t_s		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (SI-CK, CK INH)	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Set-up Time (S/L-CK, CK INH)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (PI - S/$\overline{L}$) (SI - CK, CK INH)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (S/$\overline{L}$ - CK, CK INH)	t_h		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time (CK INH - CK) (CK - CK INH)	t_{rem}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	95	-	-	-	

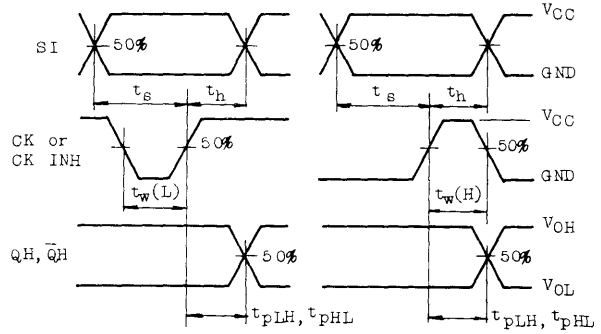
Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

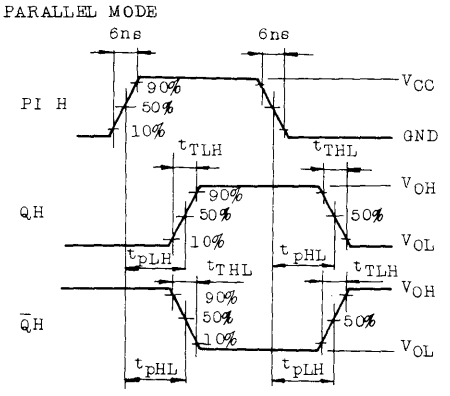
TC74HC165P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

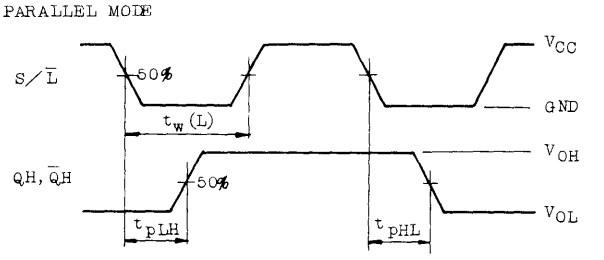
SERIAL MODE



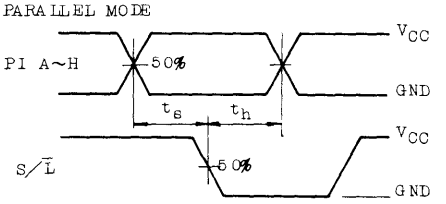
PARALLEL MODE



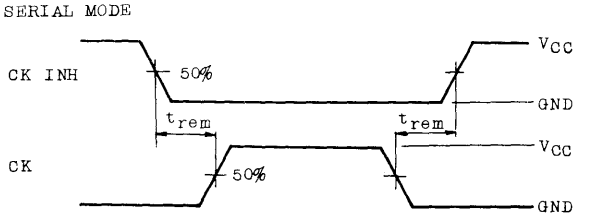
PARALLEL MODE



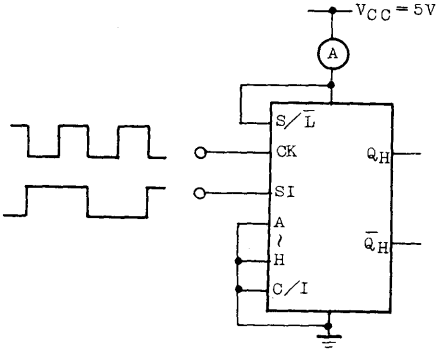
PARALLEL MODE



SERIAL MODE



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC166P/F C²MOS DIGITAL INTEGRATED CIRCUIT

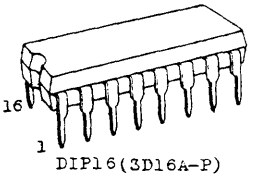
PRELIMINARY

TC74HC166P/F 8-BIT SHIFT REGISTER (P-IN, S-OUT)

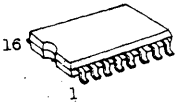
The TC74HC166 is a high speed CMOS 8 BIT PARALLEL/SERIAL-IN SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of parallel-in or serial-in, serial-out 8-bit shift register with gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{LOAD}$ input. When the SHIFT/$\overline{LOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting with each clock pulse. When held low, the parallel data inputs are enabled and synclonous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high level edge of the clock pulse. The CLOCK-INHIBIT input should be changed to the high level only while the CLOCK input is held high. A direct clear input overrides all other inputs, including the clock, and sets all flip-flop to zero. The detail about the function is shown at the truth table and the timing chart. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delay ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V∿6V
- Pin and Function Compatible with 74LS166



DIP16(3D16A-P)



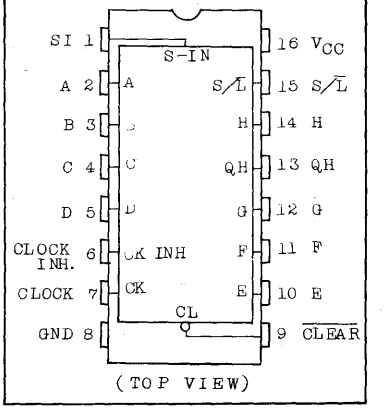
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

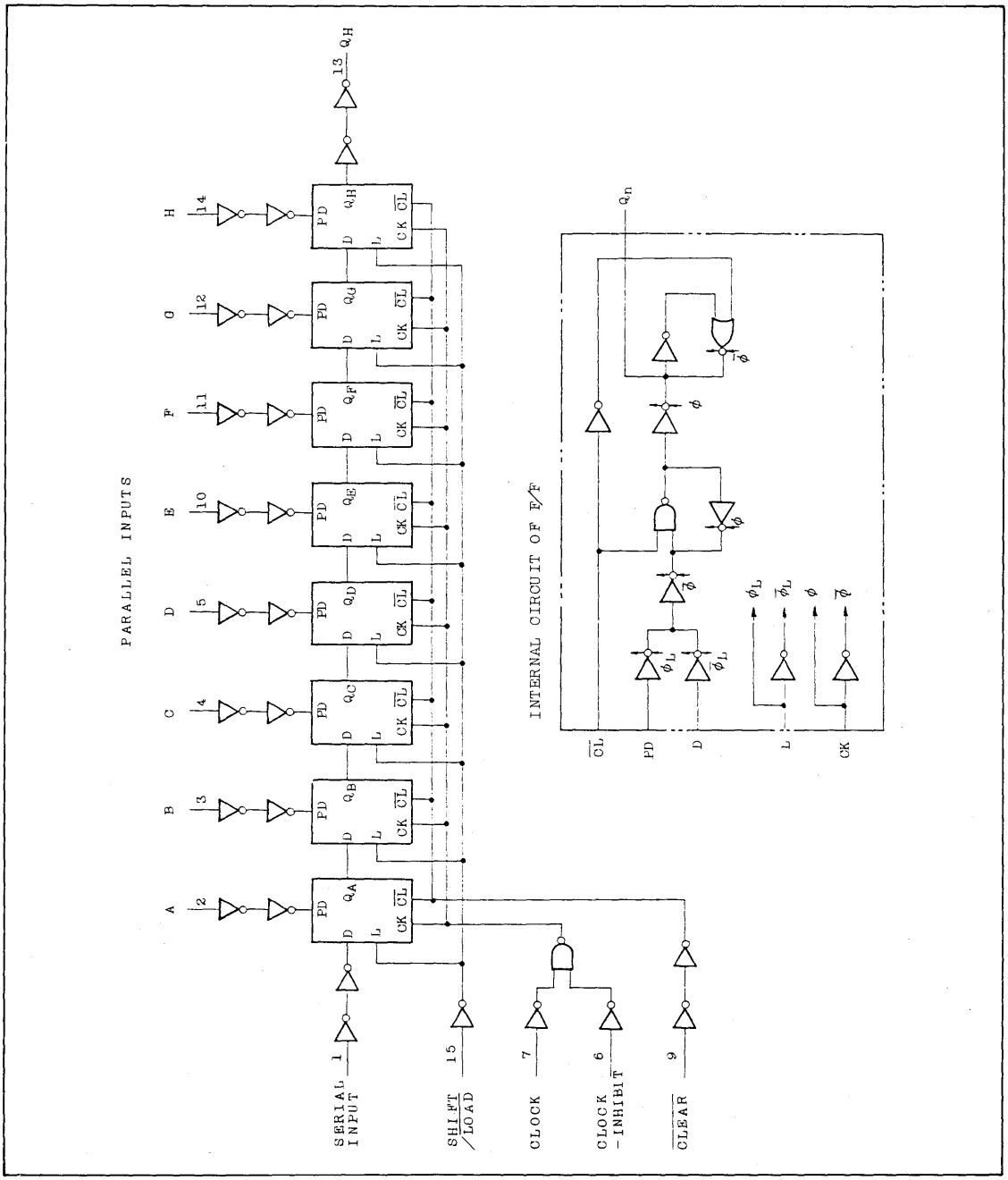
PIN ASSIGNMENT



(TOP VIEW)

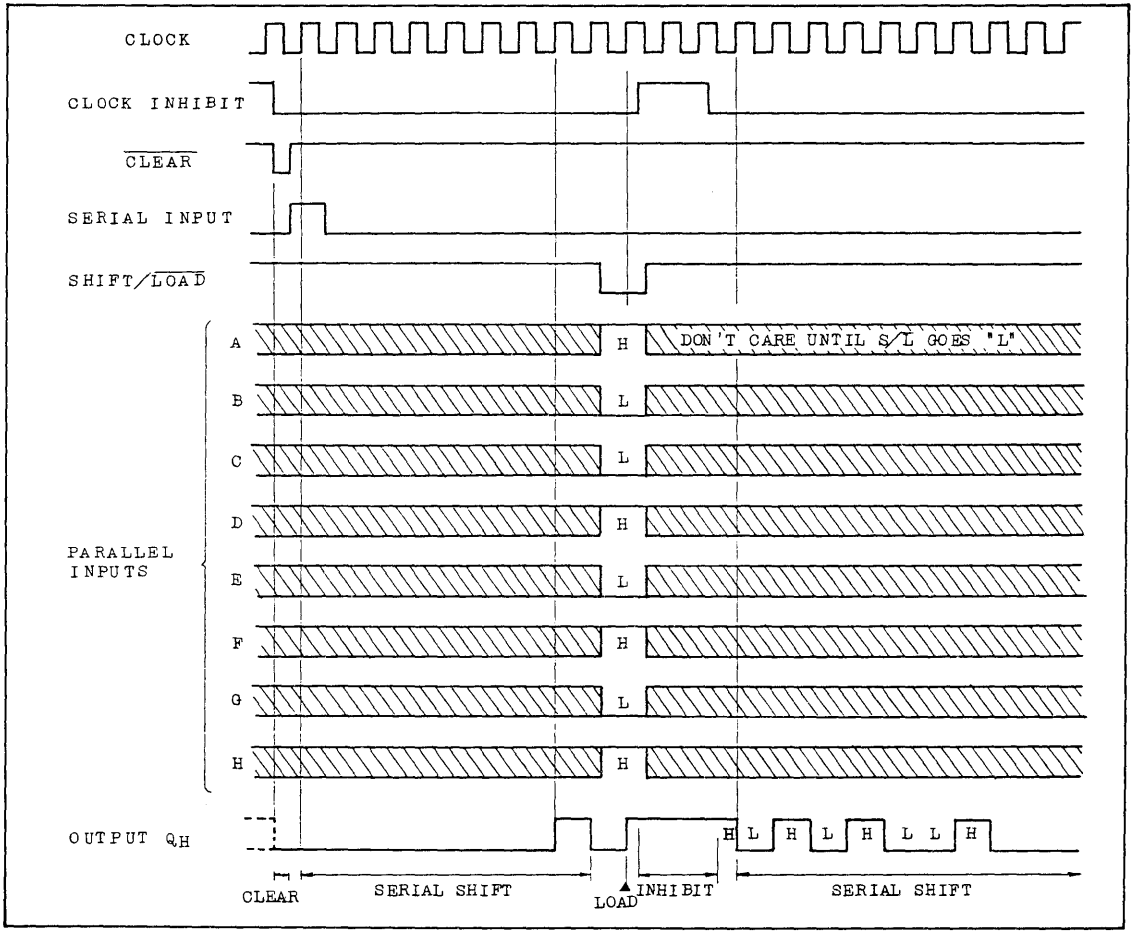
TC74HC166P/F

LOGIC DIAGRAM



TC74HC166P/F

TIMING CHART



TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
CLEAR	SHIFT/LOAD	CLOCK INH.	CLOCK	SERIAL IN	PARALLEL A ····· H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↓	X	X	No change	
H	L	L	↑	X	a ····· h	a b	h
H	H	L	↑	H	X	H QAn	QGn
H	H	L	↑	L	X	L QAn	QGn
H	X	H	X	X	X	No change	

x: Don't Care

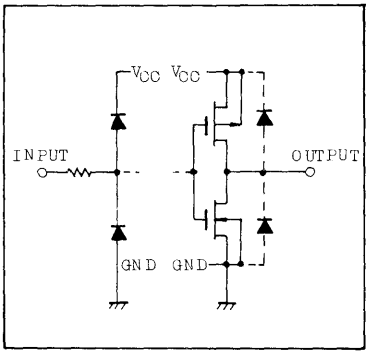
a ····· h: The level of steady state input voltage at inputs A through H respectively

TC74HC166P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC166P/F

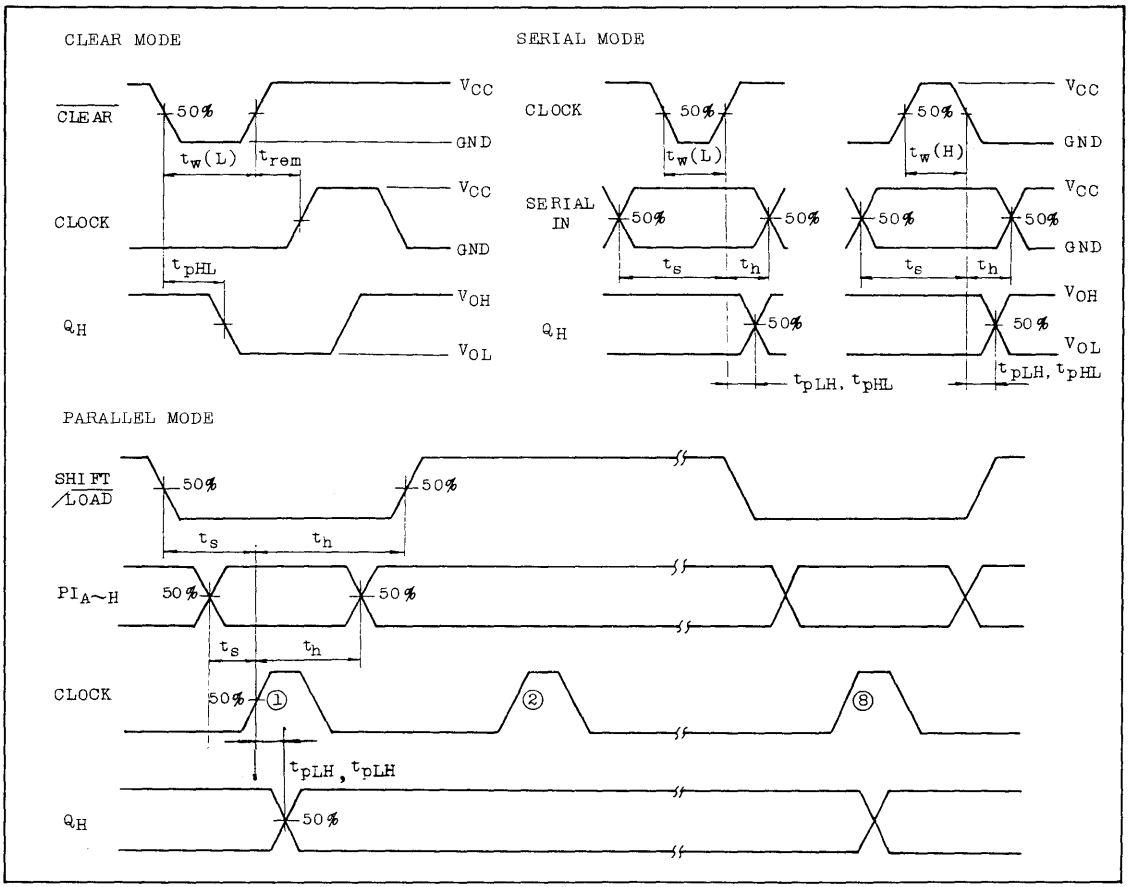
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{TLH}		6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - QH)	t_{pLH}		2.0	-	80	150	-	190	
			4.5	-	20	30	-	38	
	t_{pHL}		6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{CLEAR}$ - QH)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0		0	
			6.0	-	-	0	-	0	
Minimum Set-up Time (SI, PI)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (S/$\overline{L}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (SI, PI)	t_h		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Minimum Hold Time (S/$\overline{L}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD} (1)			-	58	-	-	-	

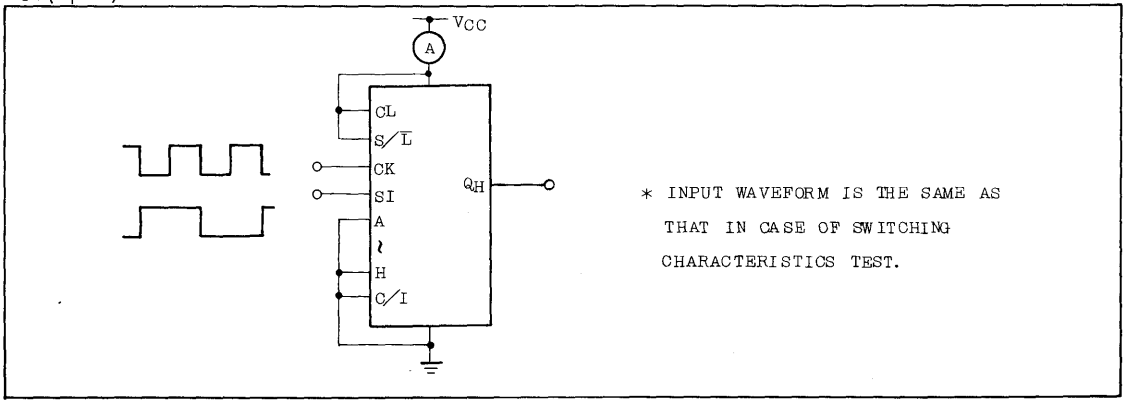
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



ICC(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC173P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

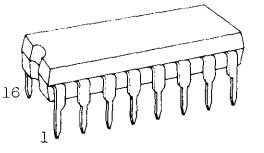
PRELIMINARY

TC74HC173P/F QUAD D-TYPE REGISTER (3-STATE)

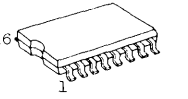
The TC74HC173 is a high speed CMOS D-TYPE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device is composed of four-bit register including D-type flip-flops and 3-state buffers. The four flip-flops are controlled by a common clock input (CLOCK) and a common reset input (CLEAR). Signals applied to the data inputs ($D_1 - D_4$) are stored at the respective flip-flops on the positive going transition of the clock input, only when both clock control inputs (G_1 and G_2) are held low. The reset feature is asynchronous and active high. The stored data are provided on each output only when both output control inputs (M and N) are held low, and otherwise the outputs are in a high-impedance state. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS173



DIP16(3D16A-P)



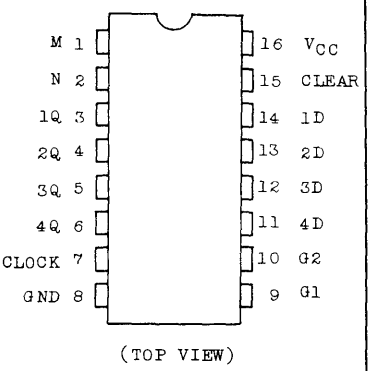
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC173P/F

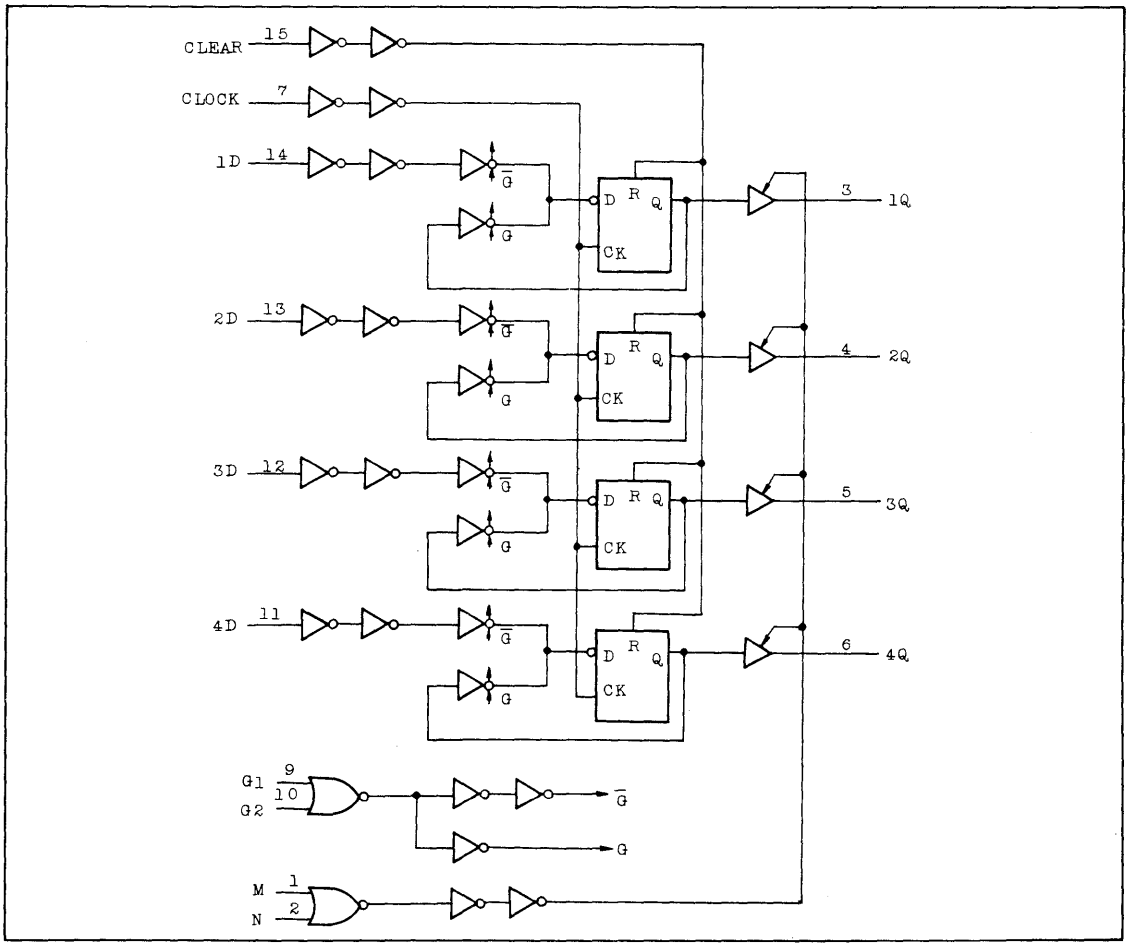
TRUTH TABLE

CLEAR	CLOCK	DATA ENABLE		Dn	OUTPUT CONTROL		Qn
		G1	G2		M	N	
X	X	X	X	X	H	X	Z
X	X	X	X	X	X	H	Z
H	X	X	X	X	L	L	L
L	↓	X	X	X	L	L	Q0
L	↑	H	X	X	L	L	Q0
L	↑	X	H	X	L	L	Q0
L	↑	L	L	H	L	L	H
L	↑	L	L	L	L	L	L

X : DON'T CARE

Z : HIGH IMPEDANCE

LOGIC DIAGRAM

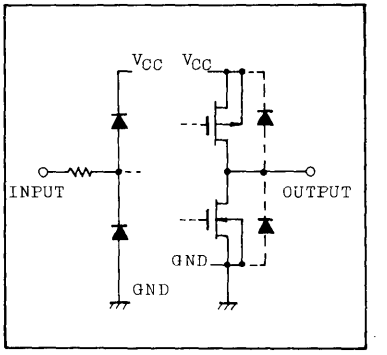


TC74HC173P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CLOCK - Q)	t_{PLH}		2.0	-	84	165	-	205	
	t_{PHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (CLEAR - Q)	t_{PLH}		2.0	-	84	165	-	205	
	t_{PHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	ns
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set-up Time (G_1, G_2)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Set-up Time (D)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (G_1, G_2, D)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL}	R_L=1 kΩ	2.0	-	60	120	-	150	
	t_{PZH}		4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
3-State Output Disable Time	t_{PLZ}	R_L=1 kΩ	2.0	-	84	150	-	190	
	t_{PHZ}		4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}			-	30	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

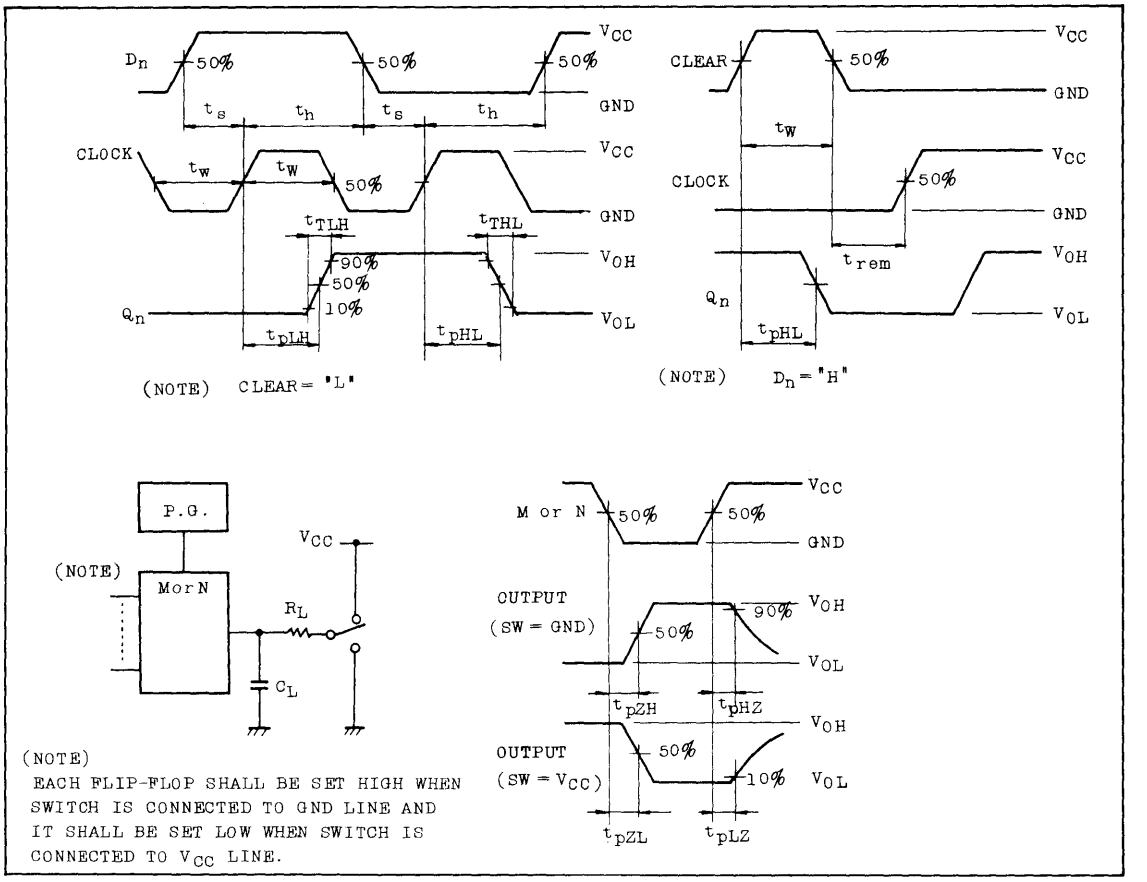
$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per 1 Circuit)}$$

And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD(total)}=14 + 16 \cdot n$$

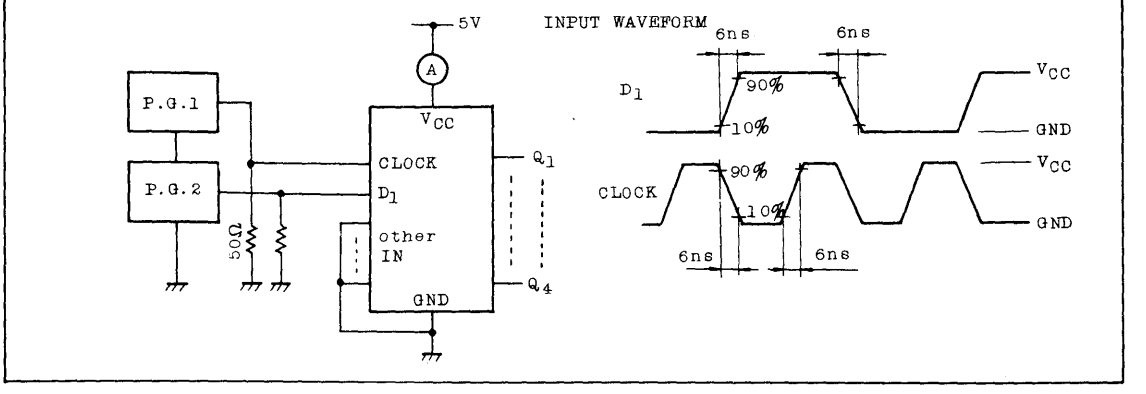
TC74HC173P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

$I_{CC(opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC174P/F

PRELIMINARY

TC74HC174P/F HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74HC174 is a high speed CMOS HEX D-TYPE FLIP FLOP fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

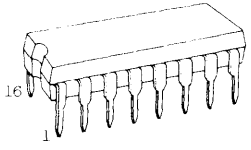
Information signals applied to D inputs are transfered to the Q output on the positive-going edge of the clock pulse.

When the $\overline{CLEAR}$ input is held low, the Q output are in the low logic level independent of the other inputs.

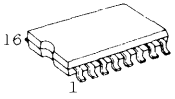
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=43MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS174

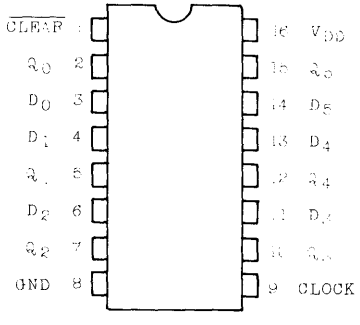


DIP16(3D16A-P)



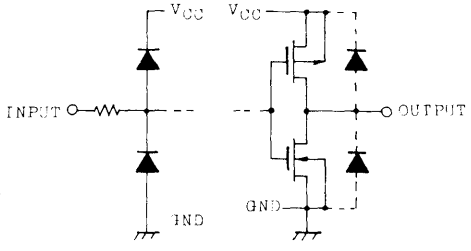
MFP16(F16GC-P)

PIN ASSIGNEMENT



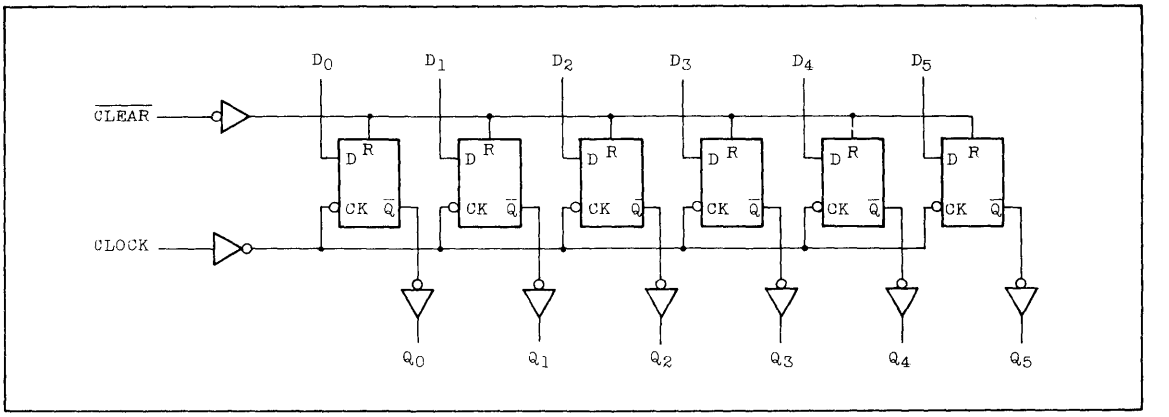
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC174P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	-
H	H	↑	H	-
H	X	↓	Q_n	No change

X : Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C
shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC174P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time $\overline{\text{CLEAR}}$ - Q	t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	44	-	22	-	
			6.0	32	52	-	26	-	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width $\overline{\text{CLEAR}}$	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{\text{CLEAR}}$	t_{rem}		2.0	-	15	75	-	95	
			4.5	-	4	15	-	19	
			6.0	-	3	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	53	-	-	-	

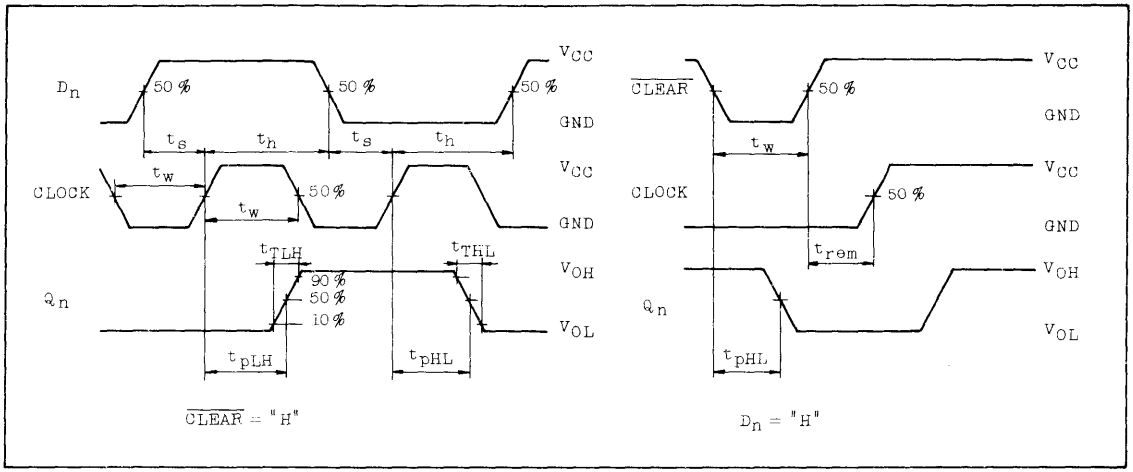
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per Flip Flop)}$$

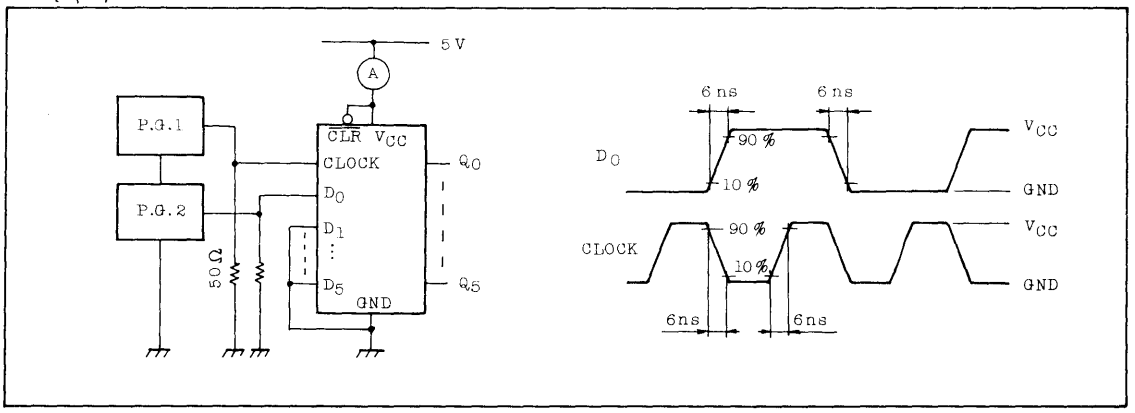
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$$C_{PD}(total) = 38 + 15 \cdot n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC175P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC175P/F QUAD D-TYPE FLIP-FLOP WITH CLEAR

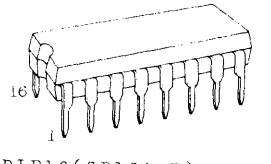
The TC74HC175 is a high speed CMOS QUAD D-TYPE FLIP-FLOP fabricated with silicon gate CMOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

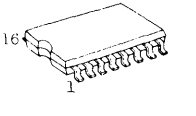
These four flip-flops are controled by a clock input (CLOCK) and a clear input (CLEAR). The infomation data applied to the D inputs (1D thru 4D) are transfered to the outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$) on the positive-going edge of the clock pulse.

Reset function is accomplished when the clear input is taken low, and all Q outputs are kept in low level regardless of other input conditions.

All input are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

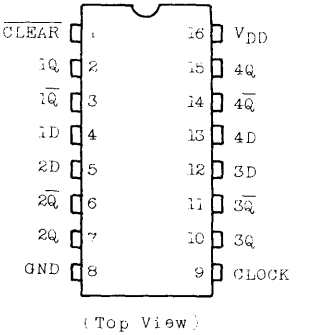


MFP16(F16GC-P)

FEATURES:

- High Speed.....f_{MAX}=53Hz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS175

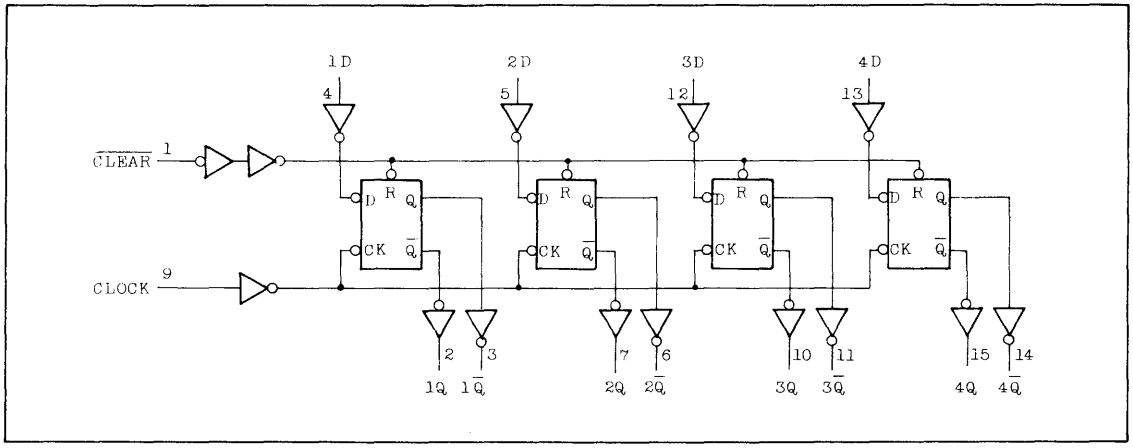
PIN ASSIGNMENT



(Top View)

TC74HC175P/F

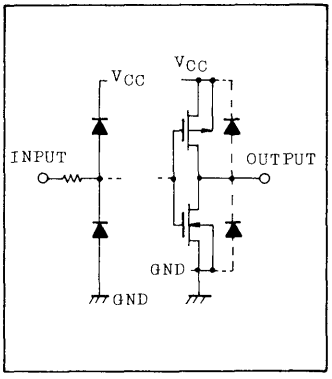
LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS		FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	$\overline{Q}$	
L	X	X	L	H	Clear
H	L	↑	L	H	-
H	H	↑	H	L	-
H	X	↓	Qn	$\overline{Q}_n$	No change
X : Don't care					

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC175P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	tr, tf	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	105	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	115	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	48	-	24	-	
			6.0	35	56	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0	-	0	75	-	95	
			4.5	-	0	15	-	19	
			6.0	-	0	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	71	-	-	-	

TC74HC175P/F

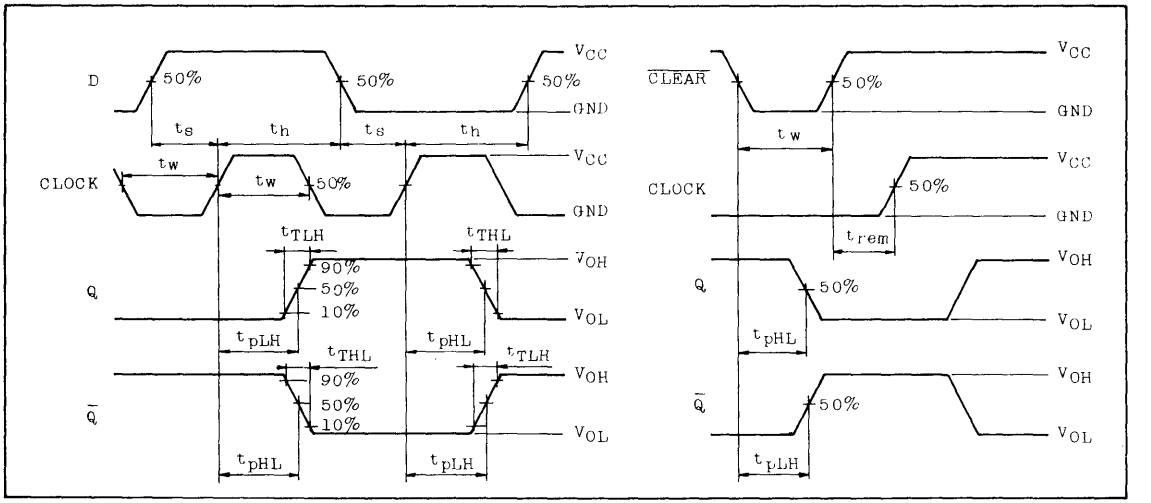
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Flip-Flop)}$$

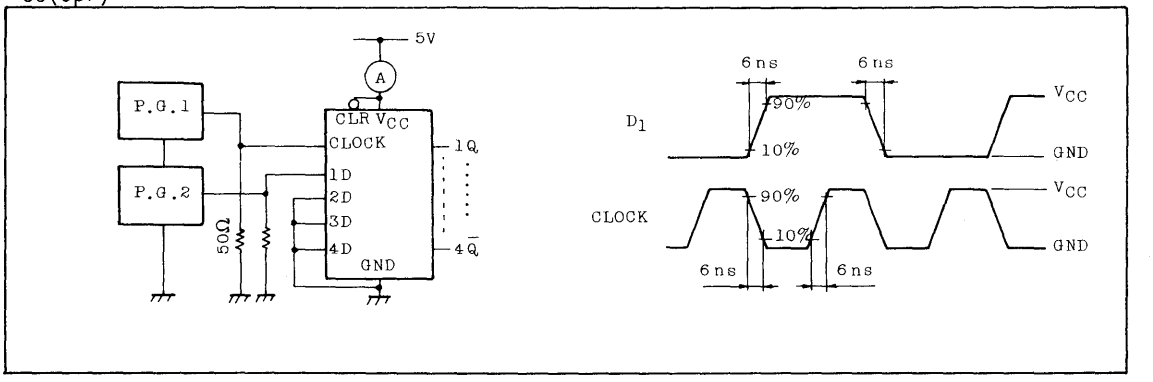
And the total C_{PD} at the time when n pcs of Flip-Flop operate can be gained by the following equation.

$$C_{PD}(\text{total}) = 43 + 28 \times n$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC181P

PRELIMINARY

TC74HC181P ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR

The TC74HC181 is a high speed CMOS ARITHMETIC LOGIC UNIT(ALU)/FUNCTION GENERATORS fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This circuit perform 16 binary arithmetic operations on two 4-bit word as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer.

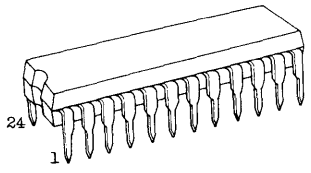
When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look ahead scheme is made available in these devices for fast, simultaneous carry generation be means of two cascade-outputs (pins 15 and 17) for the four bits in the package.

When used in conjunction with the TC74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

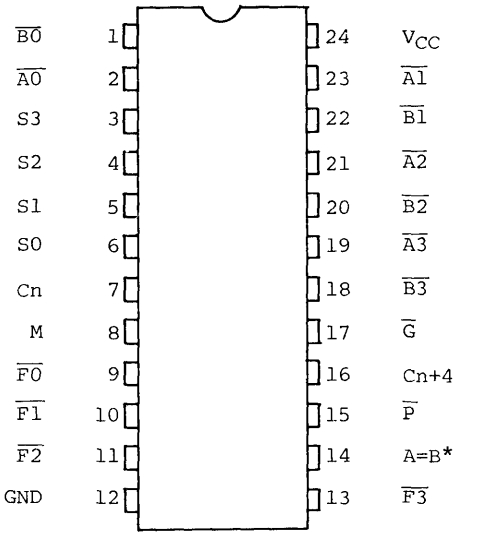
- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS181



DIP24(3D24A-P)

TC74HC181P

PIN ASSIGNMENT



(TOP VIEW)

*: Open drain Output Structure

PIN DESIGNATIONS

Designations	Pin No.	Function
$\overline{A0}$, $\overline{A1}$, $\overline{A2}$, $\overline{A3}$	2, 23, 21, 19	Word A Inputs
$\overline{B0}$, $\overline{B1}$, $\overline{B2}$, $\overline{B3}$	1, 22, 20, 18	Word B Inputs
S0, S1, S2, S3	6, 5, 4, 3	Function Select Inputs
Cn	7	Inv. Carry Input
M	8	Mode Control Input
$\overline{F0}$, $\overline{F1}$, $\overline{F2}$, $\overline{F3}$	9, 10, 11, 13	Function Outputs
A=B	14	Comparator Outputs
$\overline{P}$	15	Carry Propagate Output
Cn+4	16	Inv. Carry Output
$\overline{G}$	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

FUNCTIONAL DESCRIPTION

The HC181 will accomodate active-high or active-low data, if the pin designations are interpreted as show below.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-low data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	Cn	Cn+4	$\overline{P}$	$\overline{G}$
Active-high data(Table 2)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{Cn}$	$\overline{Cn+4}$	X	Y

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A-B-1, which requires an end-around or forced carry to produce A-B.

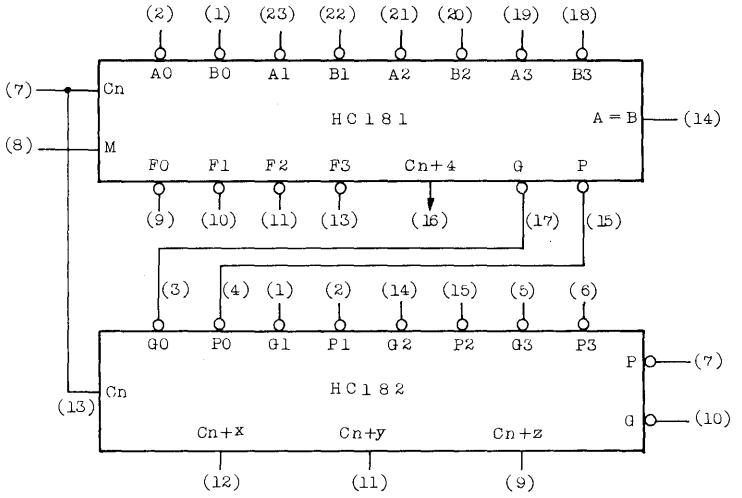
The HC181 also be utilized as a comparator. The A=B output is internally decoder from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with Cn=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (Cn+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select input S3, S2, S1, S0 at L, H, H, L, respectively.

Input Cn	Output Cn+4	Active-low data (Figure 1)	Active-high data (Figure 2)
H	H	$A \geq B$	$A \leq B$
H	L	$A < B$	$A > B$
L	H	$A > B$	$A < B$
L	L	$A \leq B$	$A \geq B$

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry.

The logic functions and arithmetic operations obtained with signal designations of Figure 1 are given in Table 1; those obtained with signal designations of Figure 2 are given in Table 2.

TC74HC181P

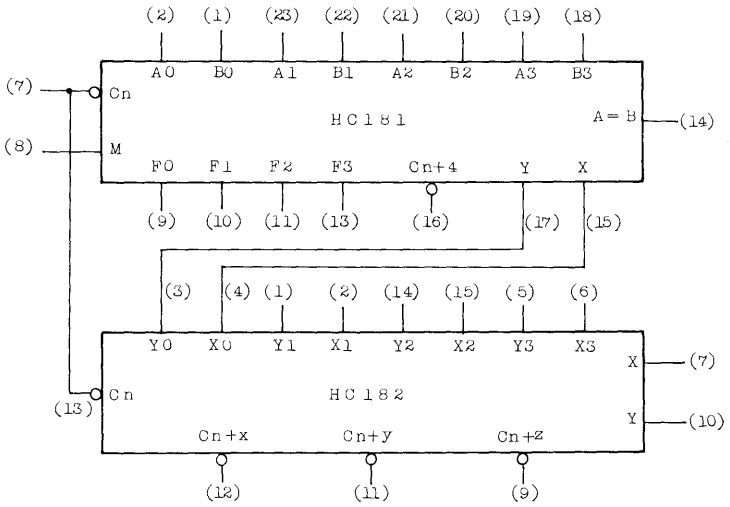


(Figure 1)

Table 1

Selection				Active Low Data		
				M=H	M=L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=L (no carry)	C_n=H (with carry)
L	L	L	L	$F = \bar{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \bar{A} + B$	F = $A\bar{B}$ Minus 1	F = ($A\bar{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus ($A + \bar{B}$)	F = A Plus($A + \bar{B}$) Plus 1
L	H	L	H	$F = \bar{B}$	F = AB Puls (A + B)	F = AB Plus($A + \bar{B}$) Plus 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	$F = A + \bar{B}$	$F = A + \bar{B}$	F = ($A + \bar{B}$) Plus 1
H	L	L	L	$F = \bar{A}B$	F = A Plus (A + B)	F = A Plus(A + B) Plus 1
H	L	L	H	$F = A \oplus B$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = $A\bar{B}$ Plus (A + B)	F = $A\bar{B}$ Plus(A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	$F = A\bar{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = $A\bar{B}$ Plus A	F = $A\bar{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

* Each bit is shifted to the next more significant position.



(Figure 2)

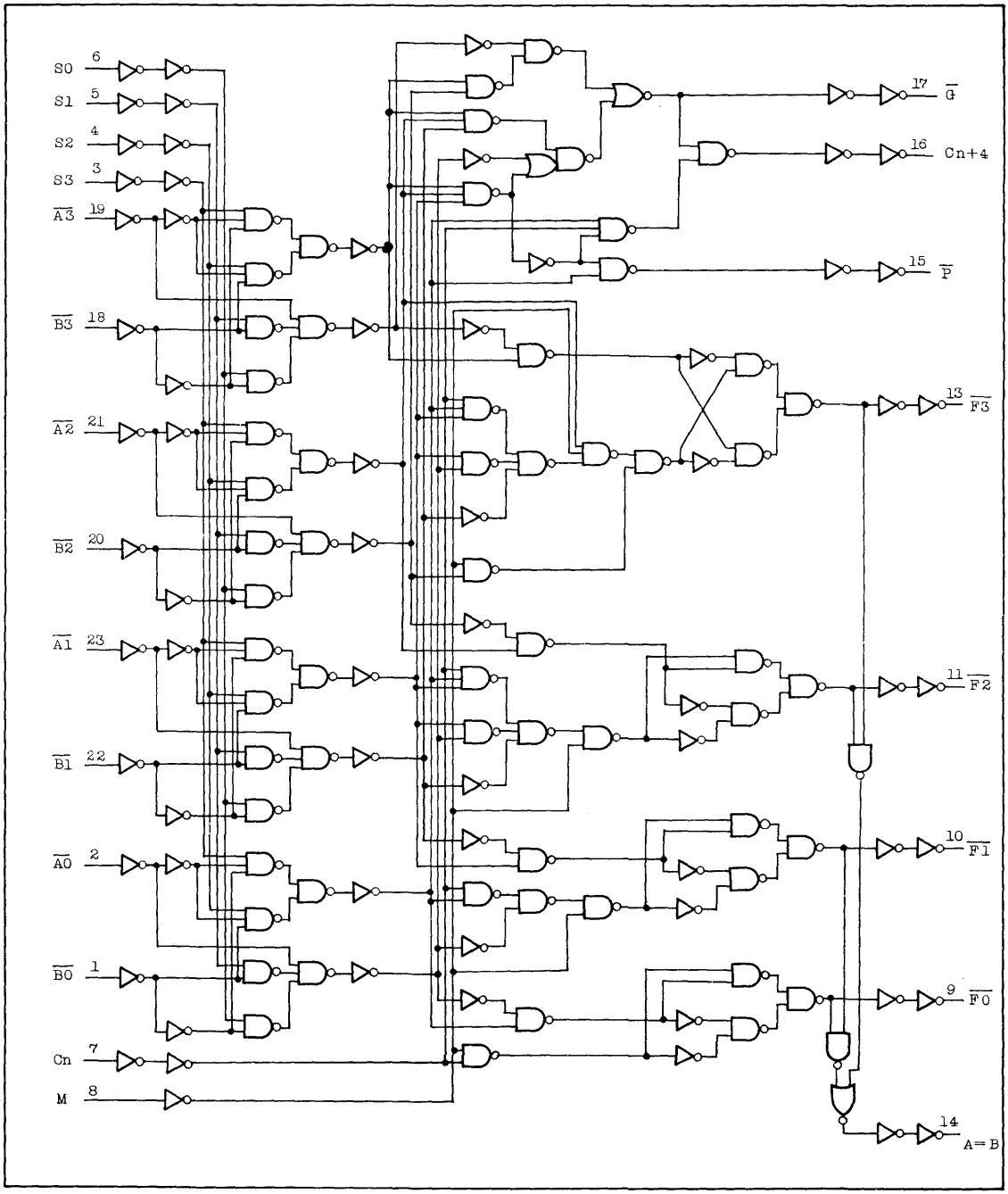
Table 2

Selection				Active High Data		
				M=H	M=L: Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A+B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{A}$B	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1(2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

* Each bit is shifted to the next more significant position.

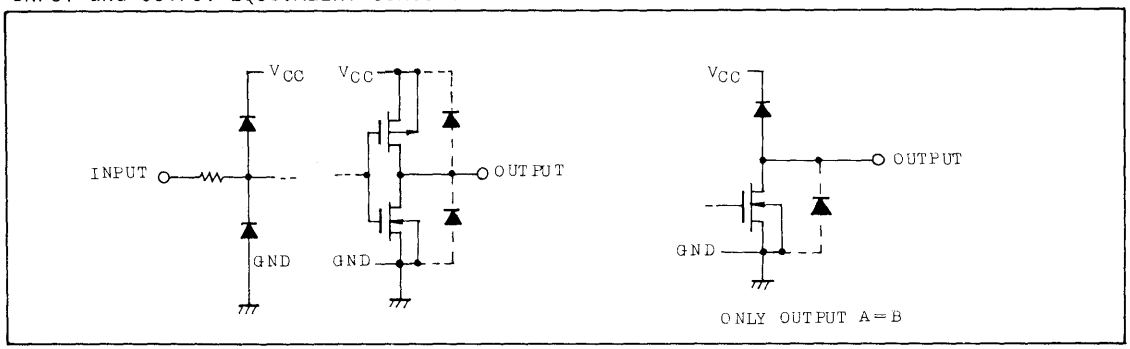
TC74HC181P

LOGIC DIAGRAM



TC74HC181P

INPUT and OUTPUT EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

TC74HC181P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Any output except A=B	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$	I_{OL}=20μA	2.0	-	0.00	0.1	-	0.1	V
				4.5	-	0.00	0.1	-	0.1	
				6.0	-	0.00	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Output Off-State Current	I_{OZ}	$V_{IN}=V_{IL}$ or V_{IH} $V_{OUT}=V_{CC}$		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

TC74HC181P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (1)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time (2)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51.	
Propagation Delay Time (3)	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (4)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
Propagation Delay Time (5)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time (6)	t_{pLH} t_{pHL}		2.0	-	116	220	-	275	
			4.5	-	29	44	-	55	
			6.0	-	25	37	-	47	
Propagation Delay Time (7)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (8)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (9)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (10)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (11)	t_{pLH} t_{pHL}		2.0	-	112	215	-	270	
			4.5	-	28	43	-	54	
			6.0	-	24	37	-	46	
3-State Output Enable Time (12)	t_{pZL}	R_L=1 kΩ	2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
3-State Output Disable Time (12)	t_{pLZ}	R_L=1 kΩ	2.0	-	140	260	-	325	
			4.5	-	35	52	-	65	
			6.0	-	30	44	-	55	

TC74HC181P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	216	-	-	-	

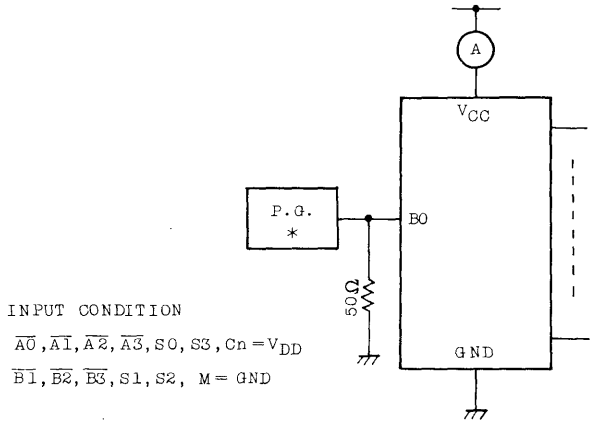
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

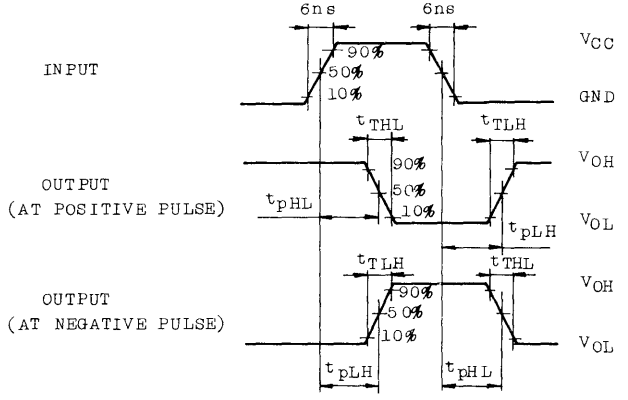
PROPAGATION DELAY TIME TEST CONDITIONS

TEST NO.	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS
(1)	Cn	Cn+4	
(2)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(3)	Any $\overline{A}$ or $\overline{B}$	Cn+4	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(4)	$\overline{Cn}$	Any $\overline{F}$	M=GND ($\overline{SUM}$ or $\overline{DIFF}$ mode)
(5)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(6)	Any $\overline{A}$ or $\overline{B}$	$\overline{G}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(7)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(8)	Any $\overline{A}$ or $\overline{B}$	$\overline{F}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(9)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=V_{CC}, S1=S2=GND ($\overline{SUM}$ mode)
(10)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)
(11)	$\overline{Ai}$ or $\overline{Bi}$	$\overline{Fi}$	M=V_{CC} (Logic mode)
(12)	Any $\overline{A}$ or $\overline{B}$	A=B	M=GND, S0=S3=GND, S1=S2=V_{CC} ($\overline{DIFF}$ mode)

$I_{CC(opr.)}$ TEST CIRCUIT



SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC182P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC182P FUNCTION LOOK AHEAD CARRY GENERATOR

The TC74HC182 is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated with silicon gate C^2MOS technology.

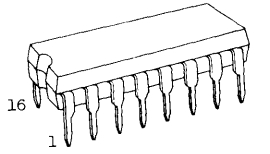
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These circuit are capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide hihg-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

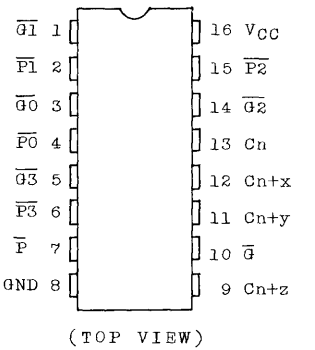
Carry input and output of the ALU's are in their true form, and the carry propagate(P) and carry generate(G) are in negated form; therefore, the carry functions (inputs, output, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS182

TC74HC182P

TRUTH TABLE

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
All other combinations			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

X: Don't care

$Cn+x = G0 + P0Cn$

$Cn+y = G1 + P1G0 + P1P0Cn$

$Cn+z = G2 + P2G1 + P2P1G0 + P2P1P0Cn$

$\overline{G} = \overline{G3+P3G2+P3P2G1+P3P2P1G0}$

$\overline{P} = \overline{P3P2P1P0}$

or

$\overline{Cn+x} = \overline{Y0(X0+Cn)}$

$\overline{Cn+y} = \overline{Y1[X1+Y0(X0+Cn)]}$

$\overline{Cn+z} = \overline{Y2\{X2+Y1[X1+Y0(X0+Cn)]\}}$

$Y = Y3(X3+Y2)(X3+X2+Y1)(X3+X2+X1+Y0)$

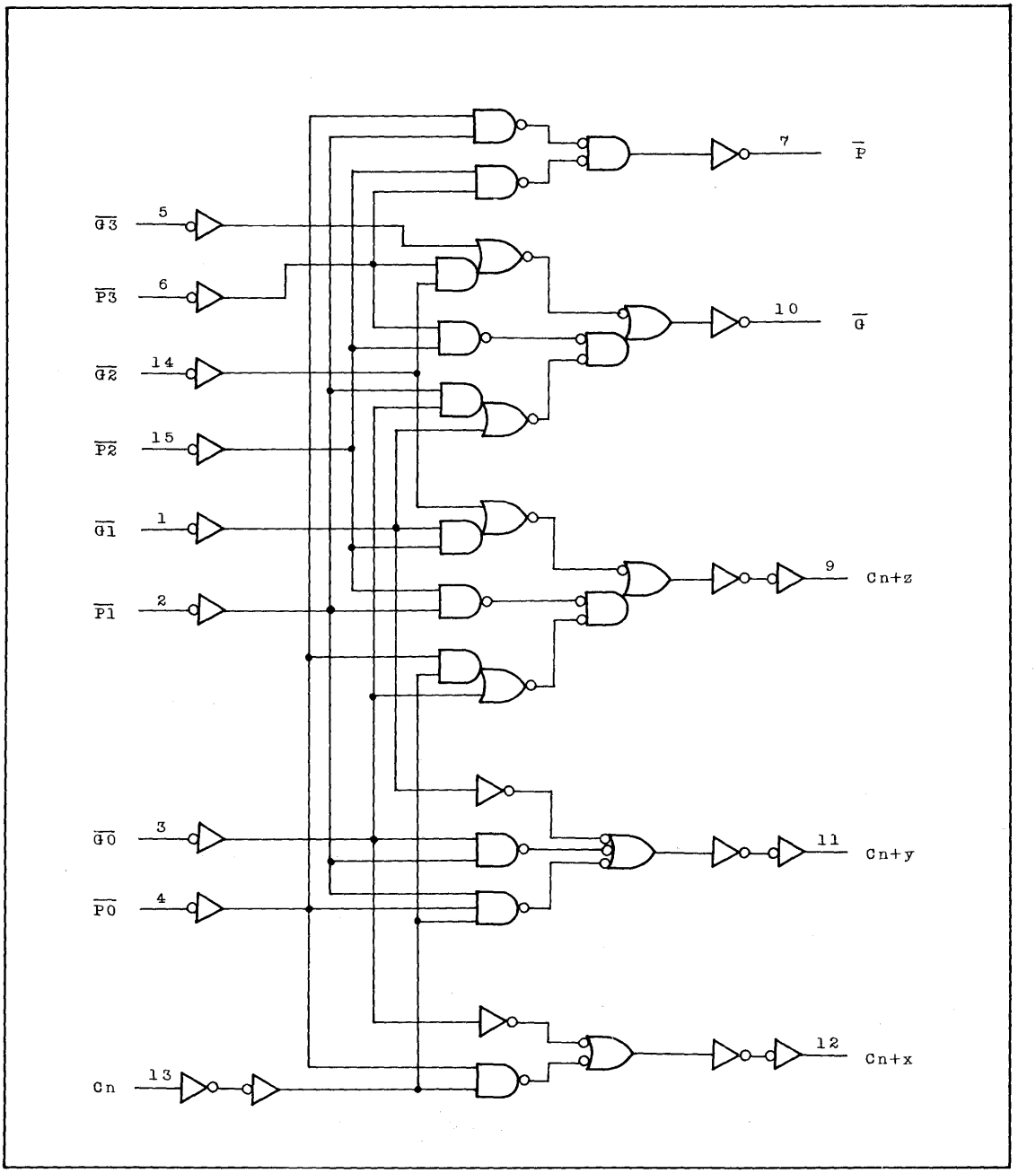
$X = X3+X2+X1+X0$

Pin Designation

Active "L"	Active "H"	Pin No.	Function
$\overline{G0}$,$\overline{G1}$,$\overline{G2}$,$\overline{G3}$	G0,G1,G2,G3	3,1,14,5	Carry Generate Inputs
$\overline{P0}$,$\overline{P1}$,$\overline{P2}$,$\overline{P3}$	P0,P1,P2,P3	4,2,15,6	Carry Propagate Inputs
Cn	$\overline{Cn}$	13	Carry Input
Cn+z, Cn+y Cn+z	$\overline{Cn+x}$, $\overline{Cn+y}$ $\overline{Cn+z}$	12,11,9	Carry Outputs
$\overline{G}$	Y	10	Carry Generate Output
$\overline{P}$	X	7	Carry Propagate Output
VCC		16	Supply Voltage
GND		8	Ground

TC74HC182P

LOGIC DIAGRAM



TC74HC182P

ABSOLUTE MAXIMUM RATINGS

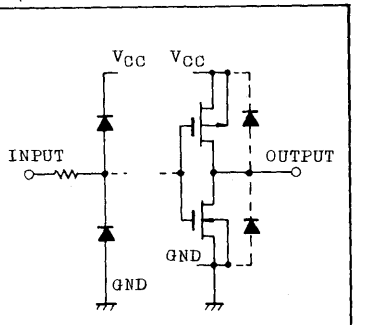
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC182P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

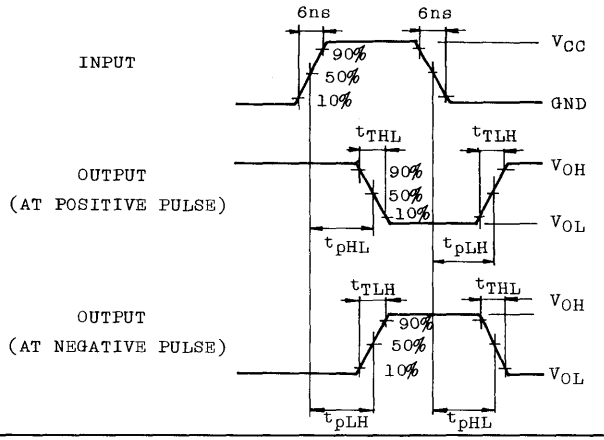
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2}$ - Cn+x, Cn+y; $\overline{P0},\overline{P1},\overline{P2}$ - Cn+z)	t_{pLH}		2.0	-	72	145	-	180	
	t_{pHL}		4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{G0},\overline{G1},\overline{G2},\overline{G3}$ - $\overline{G}$; $\overline{P1},\overline{P2},\overline{P3}$ - $\overline{G}$)	t_{pLH}		2.0	-	84	165	-	205	
	t_{pHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{P0},\overline{P1},\overline{P2},\overline{P3}$ - $\overline{P}$)	t_{pLH}		2.0	-	80	155	-	195	
	t_{pHL}		4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time (Cn - Cn+x, Cn+y, Cn+z)	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	88	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

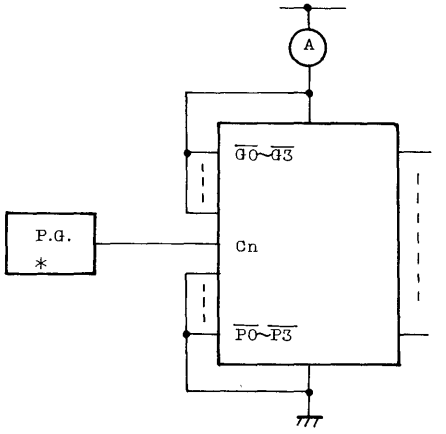
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC182P

SWITCHING CHARACTERISTICS TEST WAVEFORM



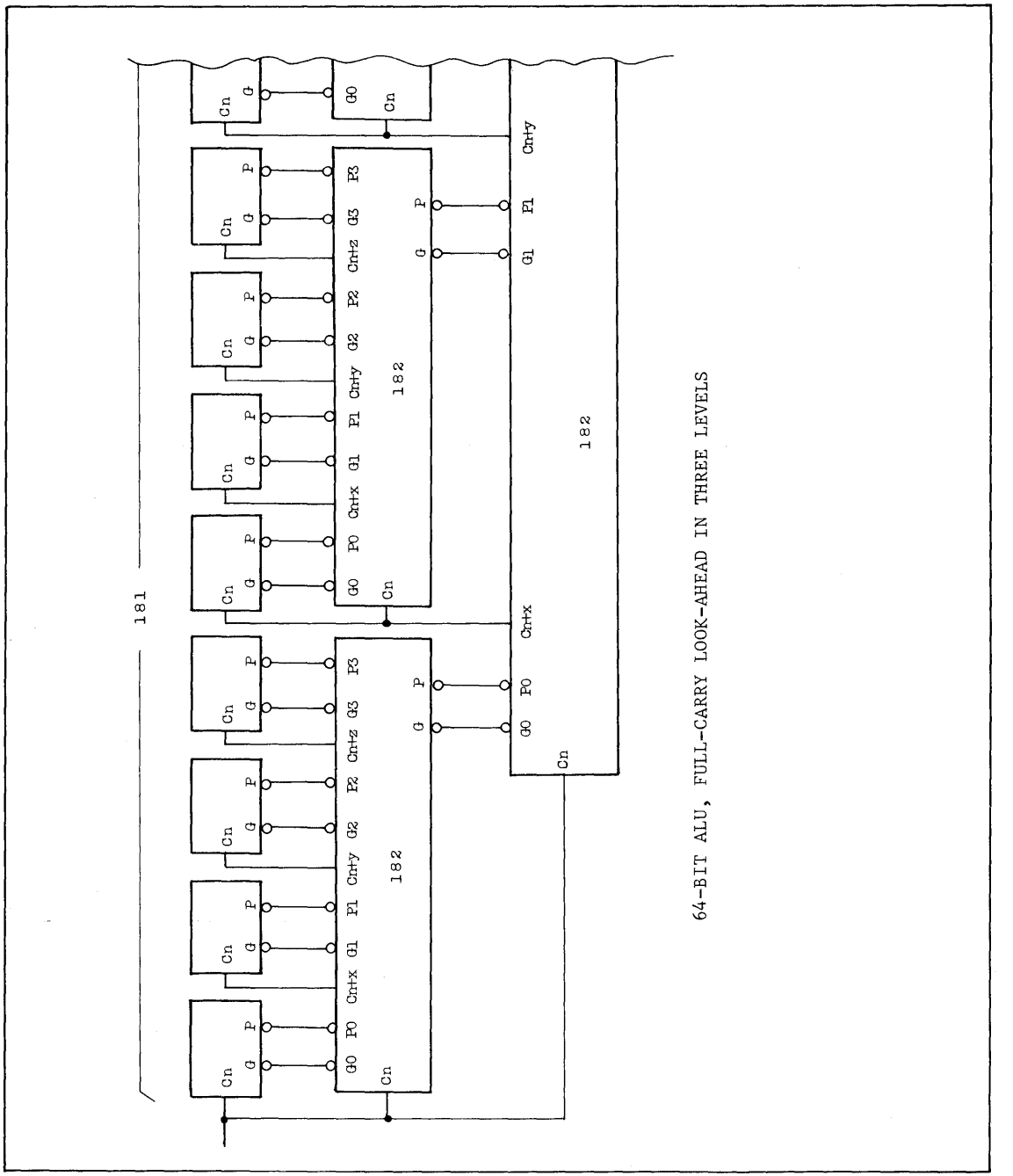
$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC182P

TYPICAL APPLICATION



TC74HC190P
TC74HC191P

CMOS DIGITAL INTEGRATED CIRCUIT

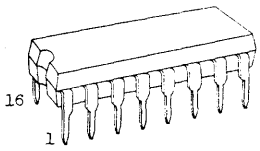
PRELIMINARY

TC74HC190P BCD UP/DOWN COUNTER
TC74HC191P 4-BIT BINARY UP/DOWN COUNTER

The TC74HC190 and TC74HC191 are high speed CMOS 4-BIT UP/DOWN COUNTERS fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC190 is BCD up/down counter and the TC74HC191 is 4-bit binary up/down counter.
These devices have asynchronous inputs LOAD ($\overline{LOAD}$). $\overline{LOAD}$ is active low and Load the load data.
The direction of the count is determined by the level of the DOWN/$\overline{UP}$ input. When low, the counter counts up and when high, it counts down. These counter change on the positive transition of the clock input.
Enable input ($\overline{ENABLE}$) and two CARRY output ($\overline{RIPPLE\ CLOCK\ OUT}$, MAX/MIN) are provided to enable easy cascading of counters, which facilitates easy implementation of N-bit counters without using external gate.
All inputs are equipped with protection circuits against static discahrge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- High Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS190/191



DIP16(3D16A-P)

TRUTH TABLE

INPUTS				OUTPUTS				FUNCTION
$\overline{LOAD}$	$\overline{ENABLE}$	D/$\overline{U}$	CLOCK	QA	QB	QC	QD	
L	X	X	X	a	b	c	d	Preset Data
H	L	L	⎍	Up Count				Up count
H	L	H	⎍	Down Count				Down Count
H	H	X	⎍	No Change				No Count
H	X	X	⎎	No Change				No Count

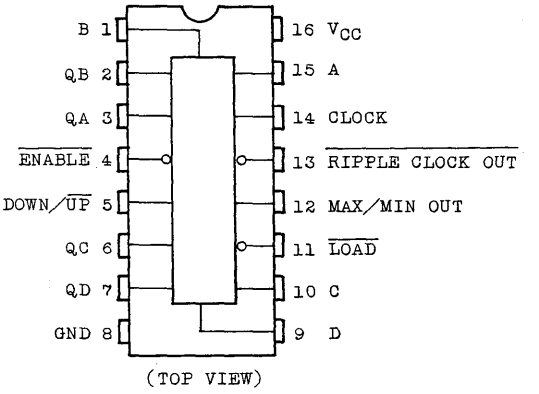
Note X: Don't care

a ∿ d: The level of steady state inputs at inputs A through D respectively.

TC74HC190P
TC74HC191P

PIN ASSIGMENT

TC74HC190/191



ABSOLUTE MAXIMUM RATINGS

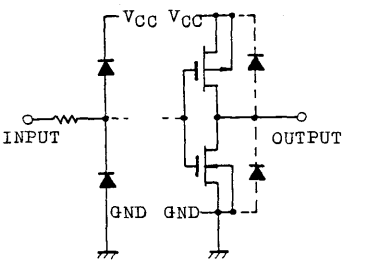
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

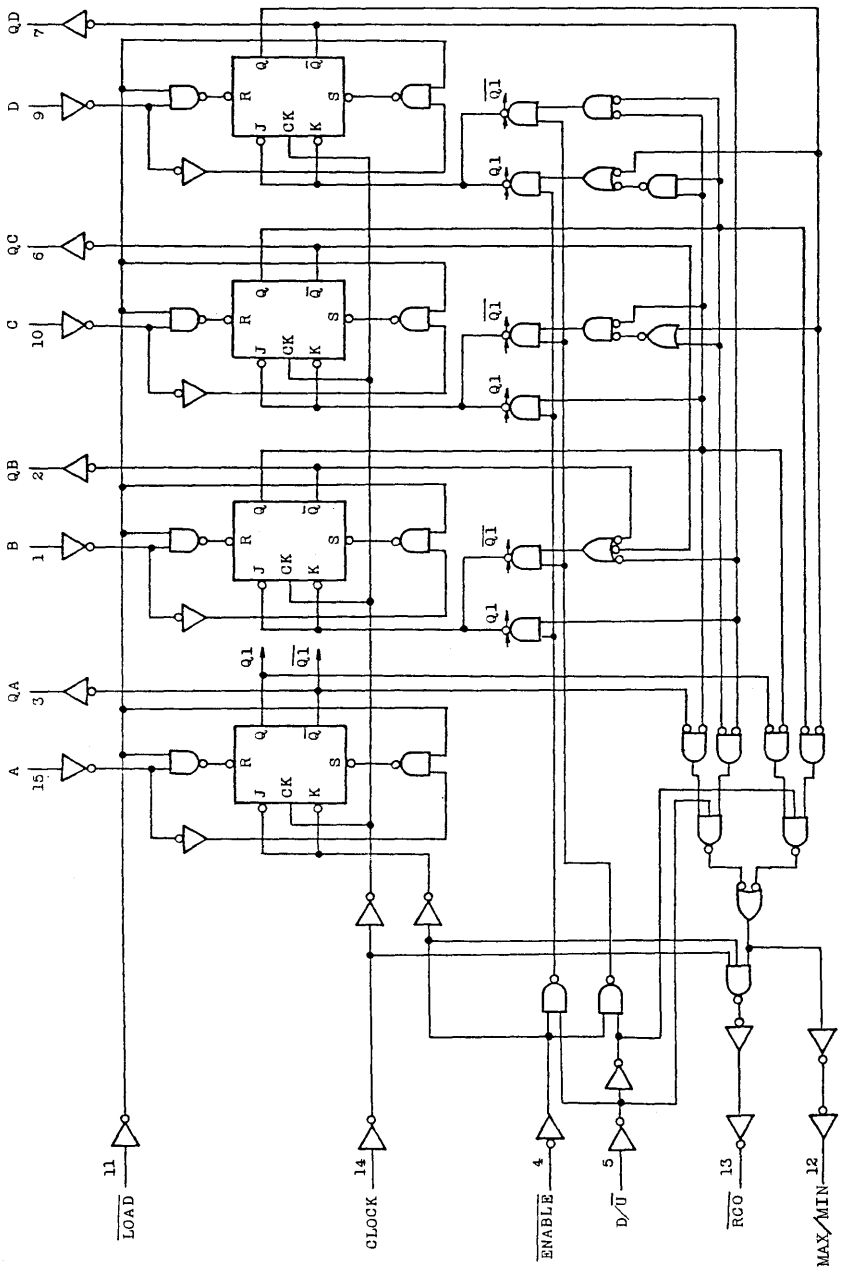
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC190P
TC74HC191P

LOGIC DIAGRAM - 1

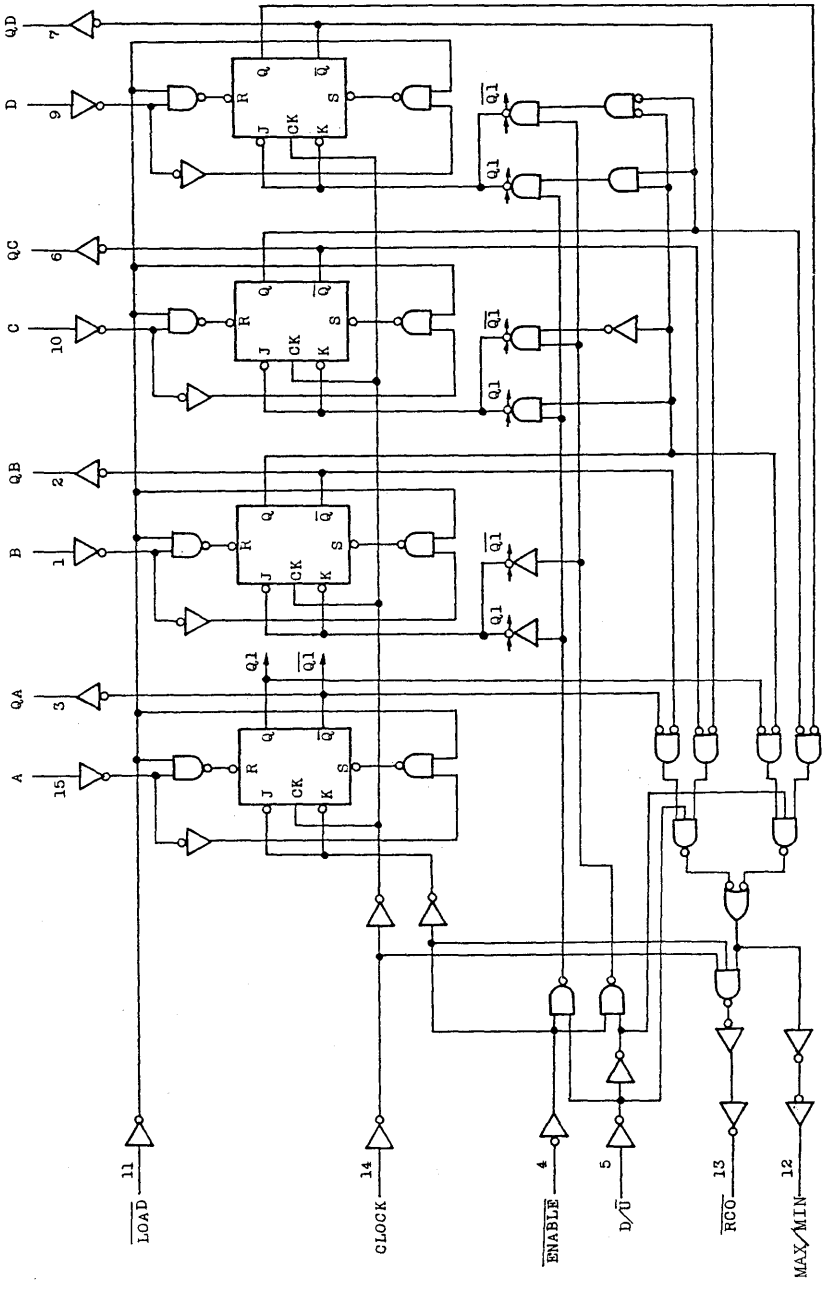
TC74HC190



TC74HC190P
TC74HC191P

LOGIC DIAGRAM - 2

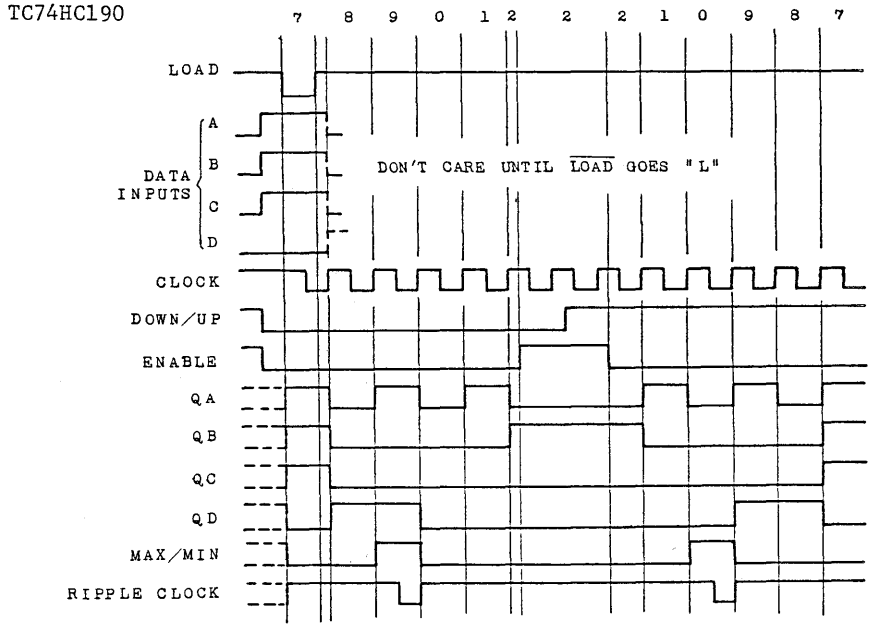
TC74HC191



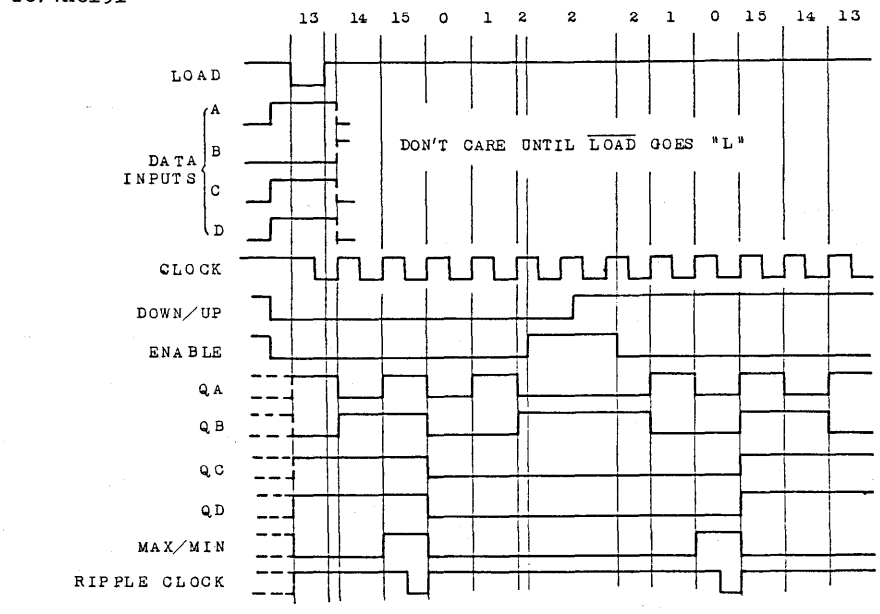
TC74HC190P
TC74HC191P

TIMING CHART

TC74HC190



TC74HC191



TC74HC190P
TC74HC191P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagrtion Dealy Time (CLOCK - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{pLH} t_{pHL}		2.0	-	104	205	-	255	ns
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Propagation Dalay Time (DATA -Q)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time ($\overline{ENABLE}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (D/$\overline{U}$ - $\overline{RCO}$)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (D/$\overline{U}$ - MAX/MIN)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	25	42	-	20	-	
			6.0	29	49	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	45	100	-	125	ns
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Set-up Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_s		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time ($\overline{ENABLE}$, D/$\overline{U}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	

TC74HC190P
TC74HC191P

AC ELECTRICAL CHARACTERISTICS (Continued)

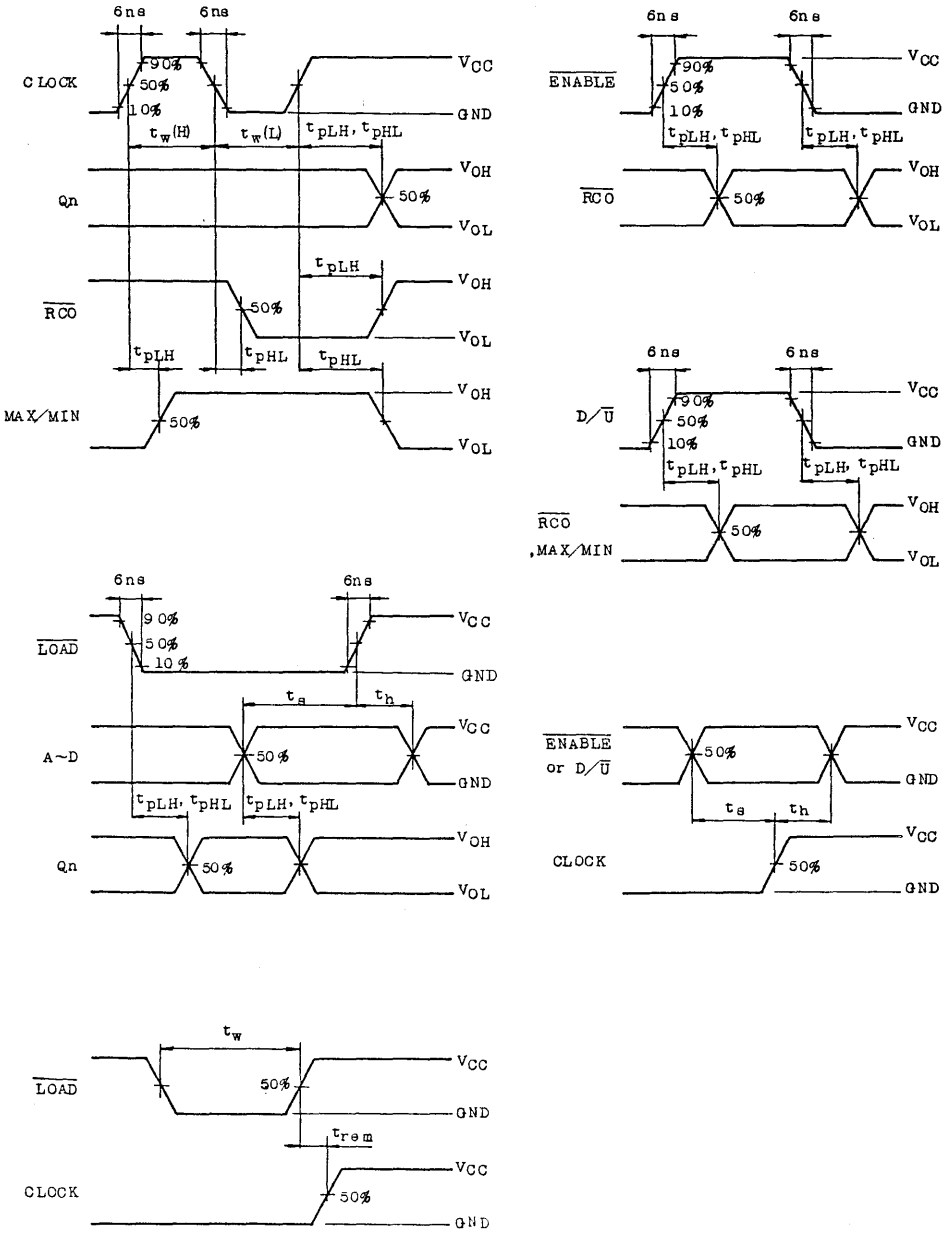
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	5	-	5	ns
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}				5	10		10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	124	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

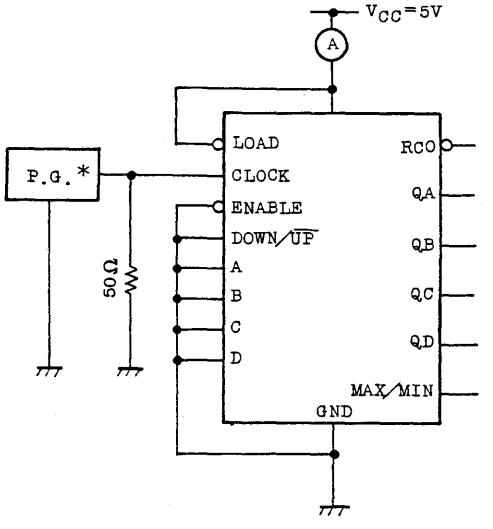
TC74HC190P
TC74HC191P

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC190P
TC74HC191P

$I_{CC(Opr.)}$ TEST WAVEFORM



* INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC192P/F
TC74HC193P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

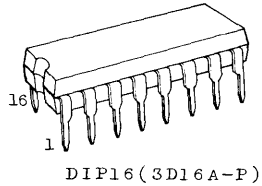
PRELIMINARY

TC74HC192P/F SYNCHRONOUS UP/DOWN DECADE COUNTER
TC74HC193P/F SYNCHRONOUS UP/DOWN BINARY COUNTER

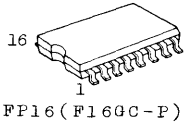
The TC74HC192 and TC74HC193 are high speed CMOS SYNCRONOUS 4-BIT UP/DOWN COUNTERs fabricated with silicon gate C^2MOS technology. They achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipaiton. These counters have a clear input(CLEAR), a load input($\overline{LOAD}$), load data inputs(A - D), two clock inputs(COUNT UP/COUNT DOWN), four count data outputs(Q_A - Q_D) and carry and borrow outputs. CLEAR is active high and forces Q_A thru Q_D outputs low independently of the other inputs. $\overline{LOAD}$ is active low and load the load data when CLEAR input is held low. COUNT UP input pulse and COUNT DOWN input pulse independently bring a up-counting or down at the positive going transition of each clock pulse. CARRY and BORROW outputs are provided in order to make a cascade connection without external circuitry. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=32MHZ(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS192/193



DIP16(3D16A-P)



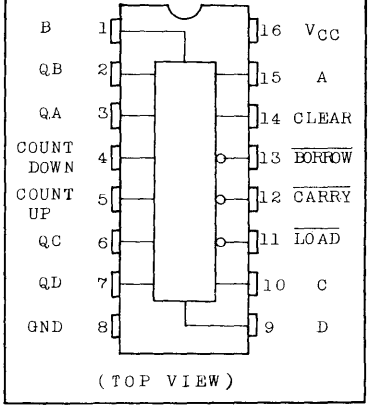
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

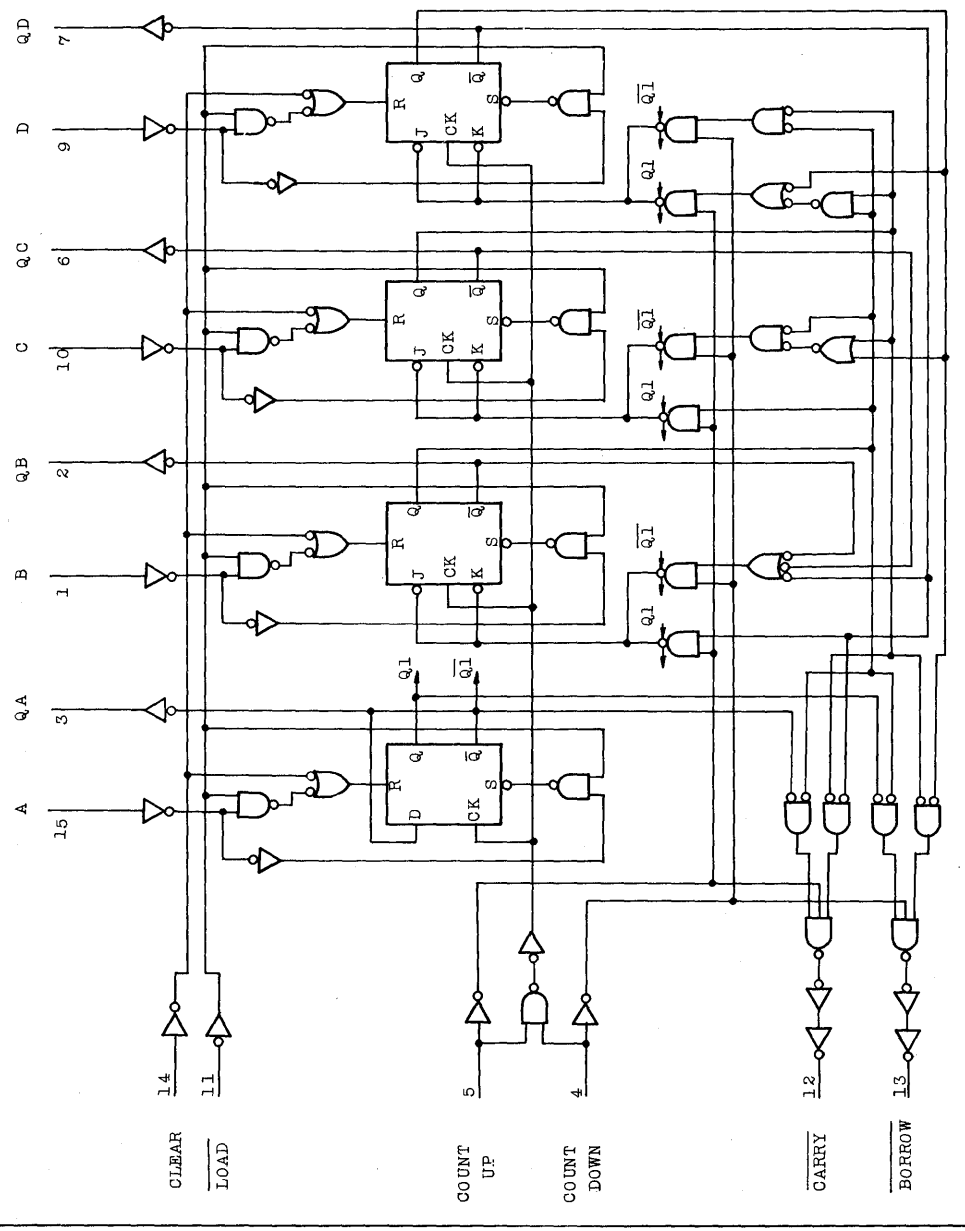


(TOP VIEW)

TC74HC192P/F
TC74HC193P/F

CIRCUIT DIAGRAM

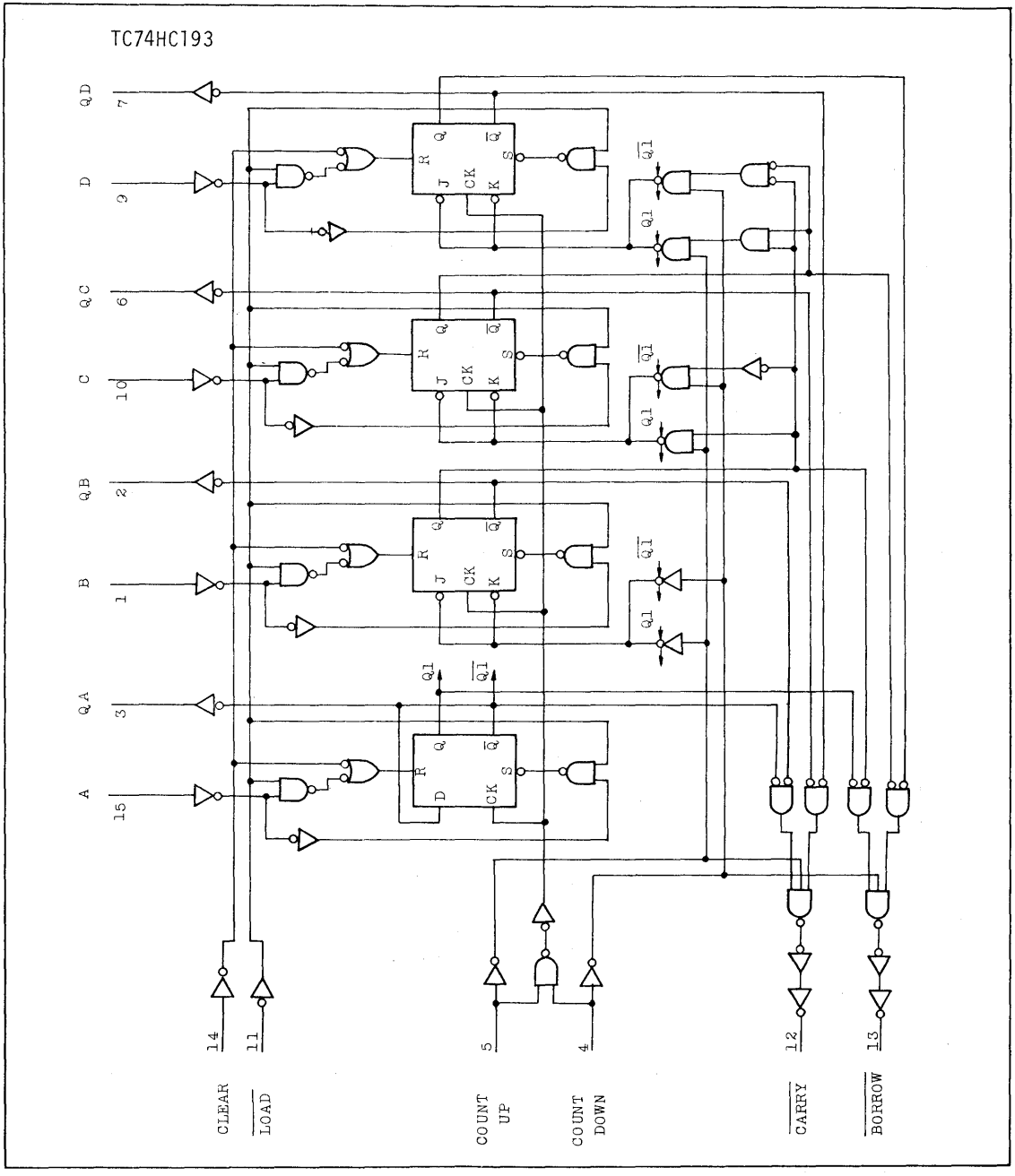
TC74HC192



TC74HC192P/F
TC74HC193P/F

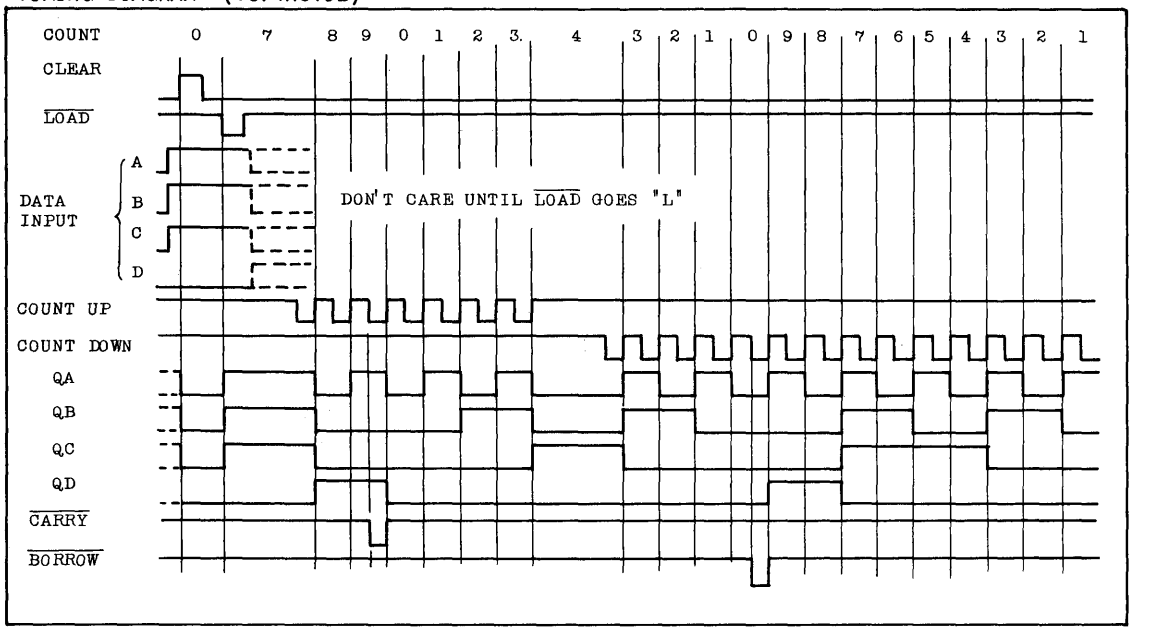
CIRCUIT DIAGRAM

TC74HC193

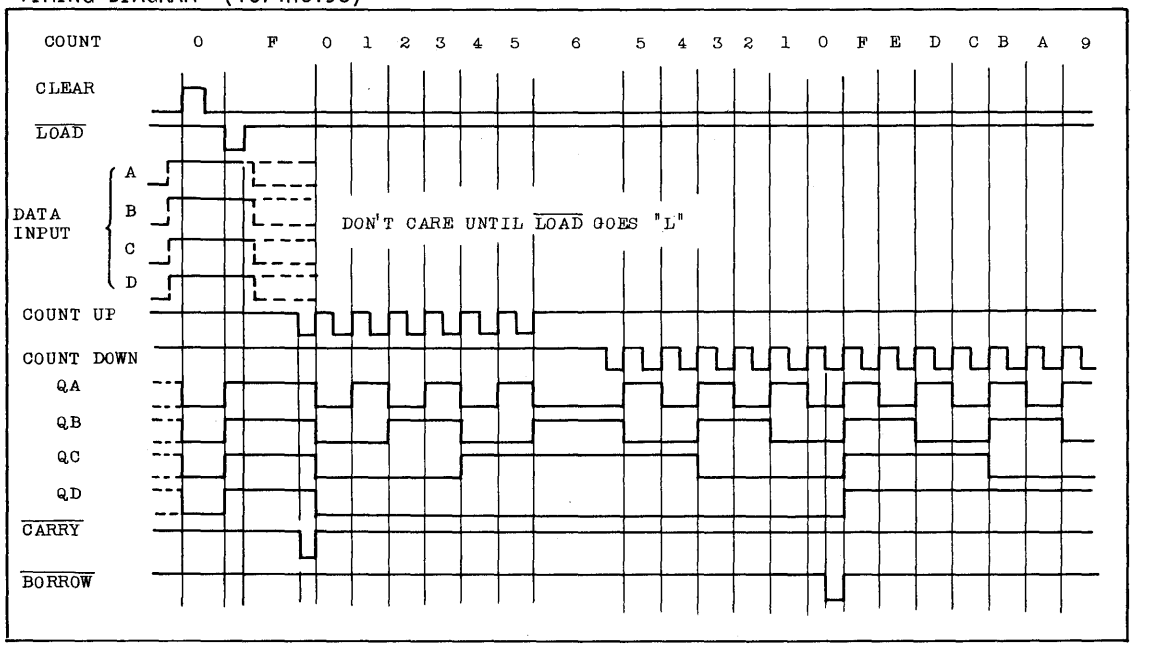


TC74HC192P/F
TC74HC193P/F

TIMING DIAGRAM (TC74HC192)



TIMING DIAGRAM (TC74HC193)



TC74HC192P/F
TC74HC193P/F

TRUTH TABLE

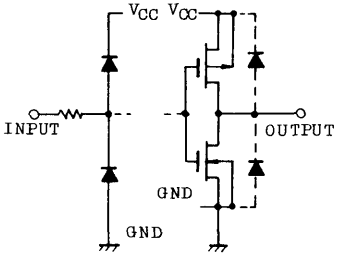
COUNT UP	COUNT DOWN	$\overline{\text{LOAD}}$	CLEAR	FUNCTION
↑	H	H	L	COUNT UP
↓	H	H	L	NO COUNT
H	↑	H	L	COUNT DOWN
H	↓	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=−40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	

TC74HC192P/F
TC74HC193P/F

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (UP, DOWN - Q)	t_{PLH}		2.0	-	96	190	-	240	
	t_{PHL}		4.5	-	24	38	-	48	
			6.0	-	20	32	-	41	
Propagation Delay Time (UP - $\overline{CARRY}$)	t_{PLH}		2.0	-	76	140	-	175	
	t_{PHL}		4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time (DOWN - $\overline{BORROW}$)	t_{PLH}		2.0	-	76	140	-	175	
	t_{PHL}		4.5	-	18	28	-	35	
			6.0	-	15	24	-	30	
Propagation Delay Time ($\overline{LOAD}$ - Q)	t_{PLH}		2.0	-	128	250	-	315	
	t_{PHL}		4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{CARRY}$)	t_{PLH}		2.0	-	160	310	-	390	
	t_{PHL}		4.5	-	40	62	-	78	
			6.0	-	34	53	-	66	
Propagation Delay Time ($\overline{LOAD}$ - $\overline{BORROW}$)	t_{PLH}		2.0	-	144	280	-	350	
	t_{PHL}		4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (JAM IN - Q)	t_{PLH} t_{PHL}		2.0	-	116	230	-	290	ns
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Propagation Delay Time (JAM IN - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	172	330	-	415	
			4.5	-	43	66	-	83	
			6.0	-	37	56	-	71	
Propagation Delay Time (JAM IN - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	144	265	-	345	
			4.5	-	36	55	-	69	
			6.0	-	31	47	-	59	
Propagation Delay Time (CLEAR - Q)	t_{PHL}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time (CLEAR - $\overline{CARRY}$)	t_{PLH}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Propagation Delay Time (CLEAR - $\overline{BORROW}$)	t_{PHL}		2.0	-	148	285	-	355	
			4.5	-	37	57	-	71	
			6.0	-	31	48	-	60	
Maximum Frequency (CLOCK)	f_{MAX}		2.0	3	7	-	2.5	-	MHz
			4.5	16	29	-	13	-	
			6.0	19	34	-	15	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	70	150	-	190	ns
			4.5	-	17	30	-	38	
			6.0	-	14	26	-	32	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(H)}$		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	45	100	-	125	
			4.5	-	11	20	-	25	
			6.0	-	9	17	-	21	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	

TC74HC192P/F
TC74HC193P/F

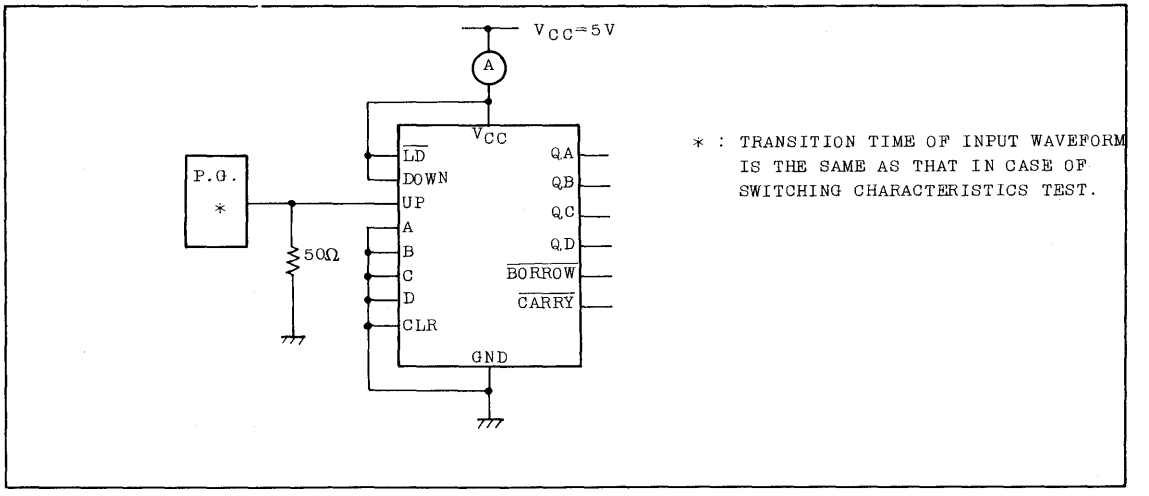
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_s		2.0	-	40	100	-	125	ns
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	66	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{DD(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

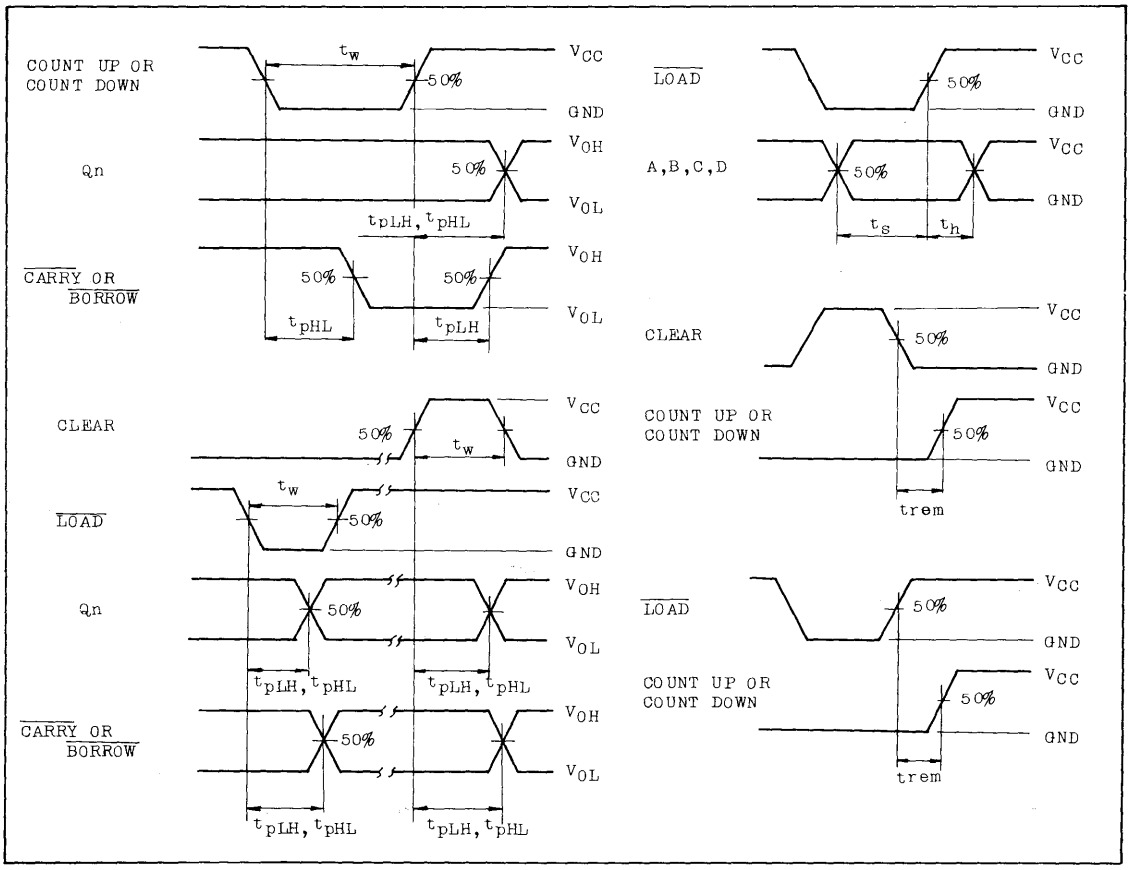
$I_{CC(opr.)}$ TEST WAVERORM



* : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC192P/F
TC74HC193P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC194P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

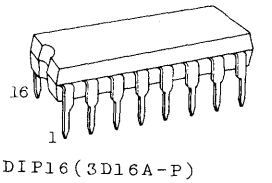
PRELIMINARY

TC74HC194P/F 4-BIT PIPO SHIFT REGISTER

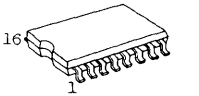
The TC74HC194 a high speed CMOS 4-BIT BIDIRECTIONAL SHIFT REGISTER fabricated with silicon C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It consists of parallel in, parallel out, 4 ibt register with shift right and shift left input. In parallel mode, data of D0 ∿ D3 are stored into the internal flip-flops at the low-to-high level transition of the clock pulse. Shift right and shift left inputs are inhibited during parallel operating mode. In shift right and shift left modes, data from shift right and shift left inputs are shifted to the right and to the left by 1 bit, respectively, synchronously with the low-to-high level edge of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS194



DIP16(3D16A-P)



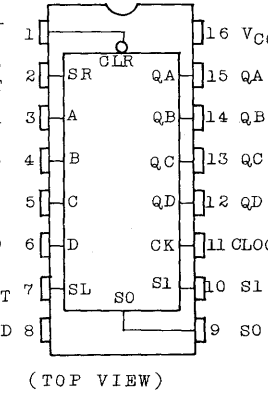
MFP16(F16QC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC194P/F

TRUTH TABLE

INPUTS										OUTPUTS			
$\overline{CLEAR}$	MODE		CLOCK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SL	SR	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	↓	X	X	X	X	X	X	QA0	QB0	QC0	QD0
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QAn	QBn	QCn
H	L	H	↑	X	L	X	X	X	X	L	QAn	QBn	QCn
H	H	L	↑	H	X	X	X	X	X	QBn	QCn	QDn	H
H	H	L	↑	L	X	X	X	X	X	QBn	QCn	QDn	L
H	L	L	X	X	X	X	X	X	X	QA0	QB0	QC0	QD0

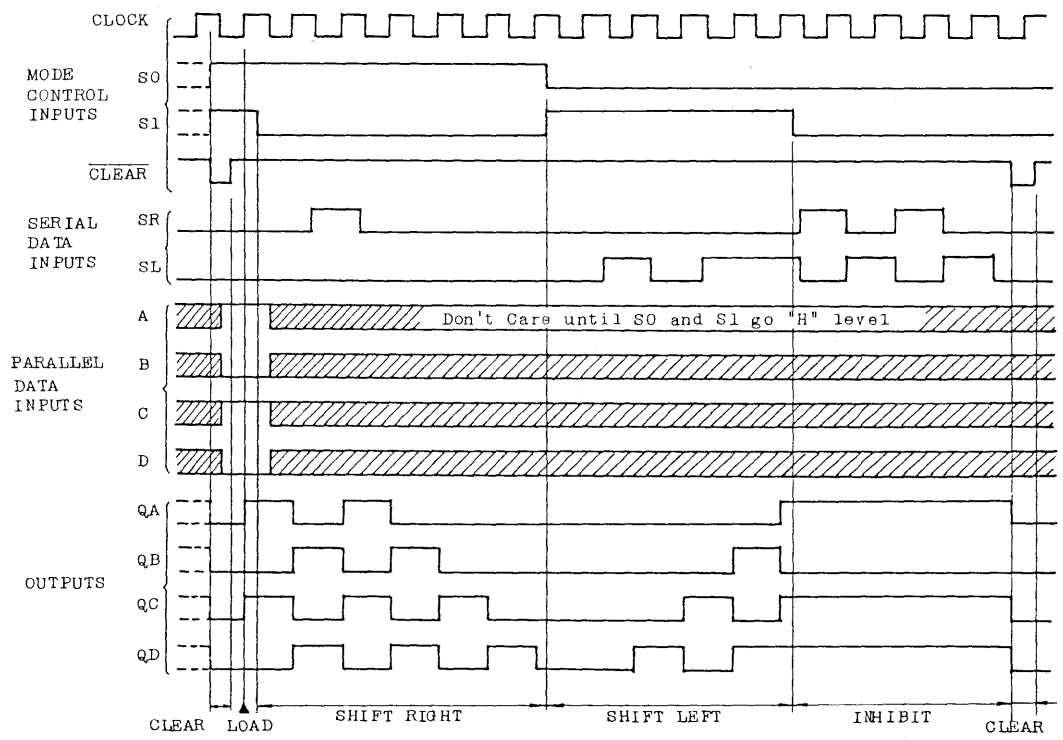
X: Don't care

a ∿ d: The level of steady state input voltage at input A ∿ D respectively

QA0 ∿ QD0: No change

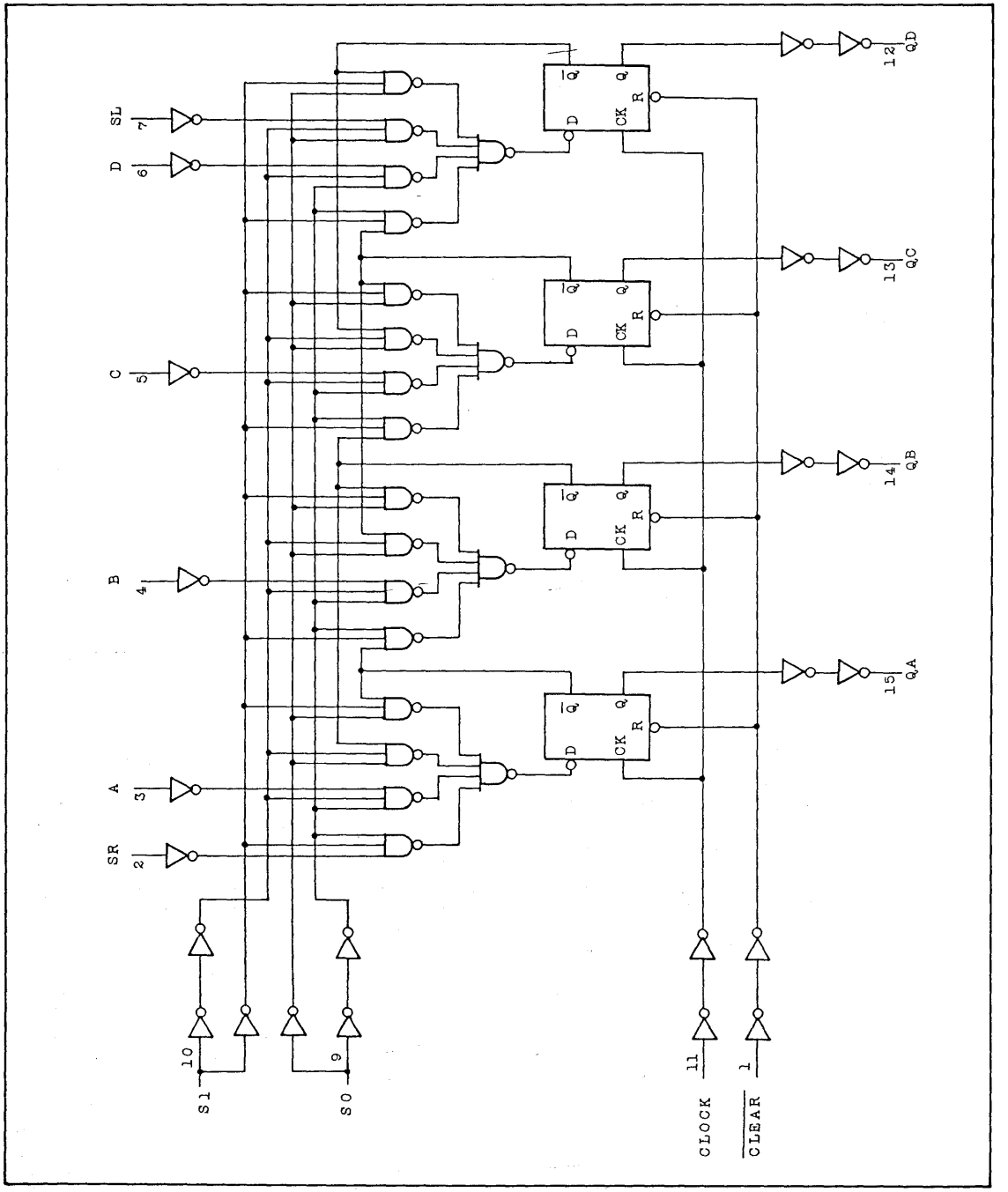
QAn ∿ QDn: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

TIMING CHART



TC74HC194P/F

LOGIC DIAGRAM

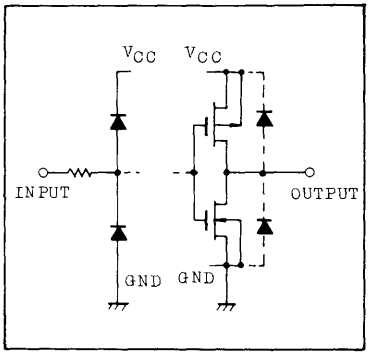


TC74HC194P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TC74HC194P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

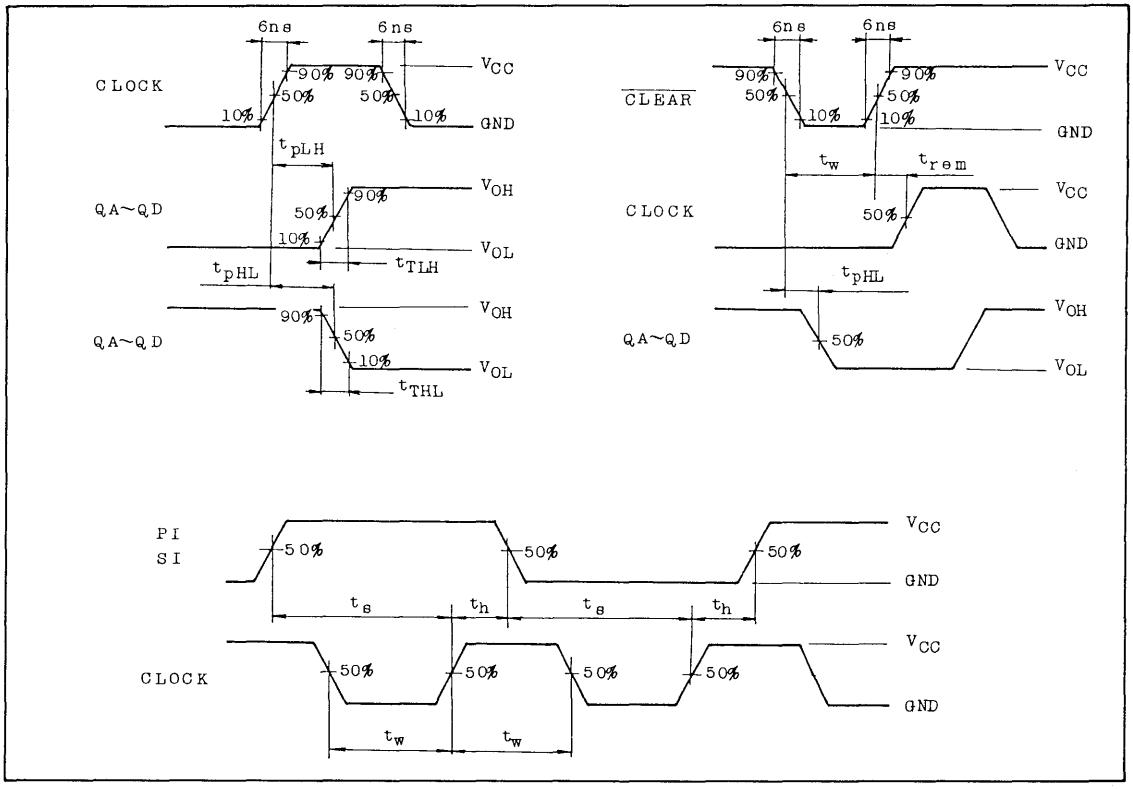
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S_{IN}, P_{IN})	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (S0, S1)	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	103	-	-	-	

Note (1): C_{PD} is defined as the vlaue of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit.) Average operating current can be obtained by the equation hereunder.

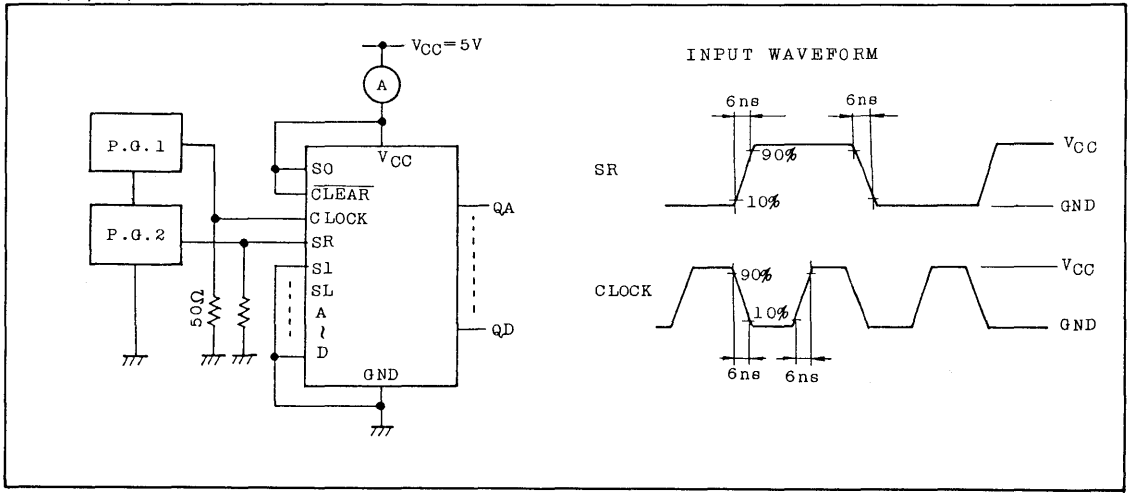
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC194P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC195P

C²MOS DIGITAL INTEGRATED CIRCUIT

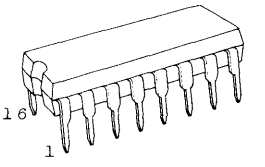
PRELIMINARY

TC74HC195P 4-BIT PARALLEL SHIFT REGISTER

The TC74HC195 is a high speed CMOS 4-BIT SHIFT REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This register features parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{LOAD}$ input. When the SHIFT/$\overline{LOAD}$ input is held low, the parallel mode operation is designated. The data of A∿D inputs is loaded into the internal register and appears at the outputs after the positive transition of the clock. When the SHIFT/$\overline{LOAD}$ input is held high, the serial mode operation having J, $\overline{K}$ logical inputs is designated and four flip-flops perform shifting at the positive transition of the clock. A direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS195



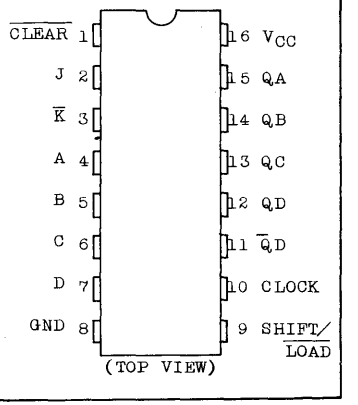
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TC74HC195P

TRUTH TABLE

INPUTS									OUTPUTS				
$\overline{CLEAR}$	SHIFT/$\overline{LOAD}$	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	X	↓	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

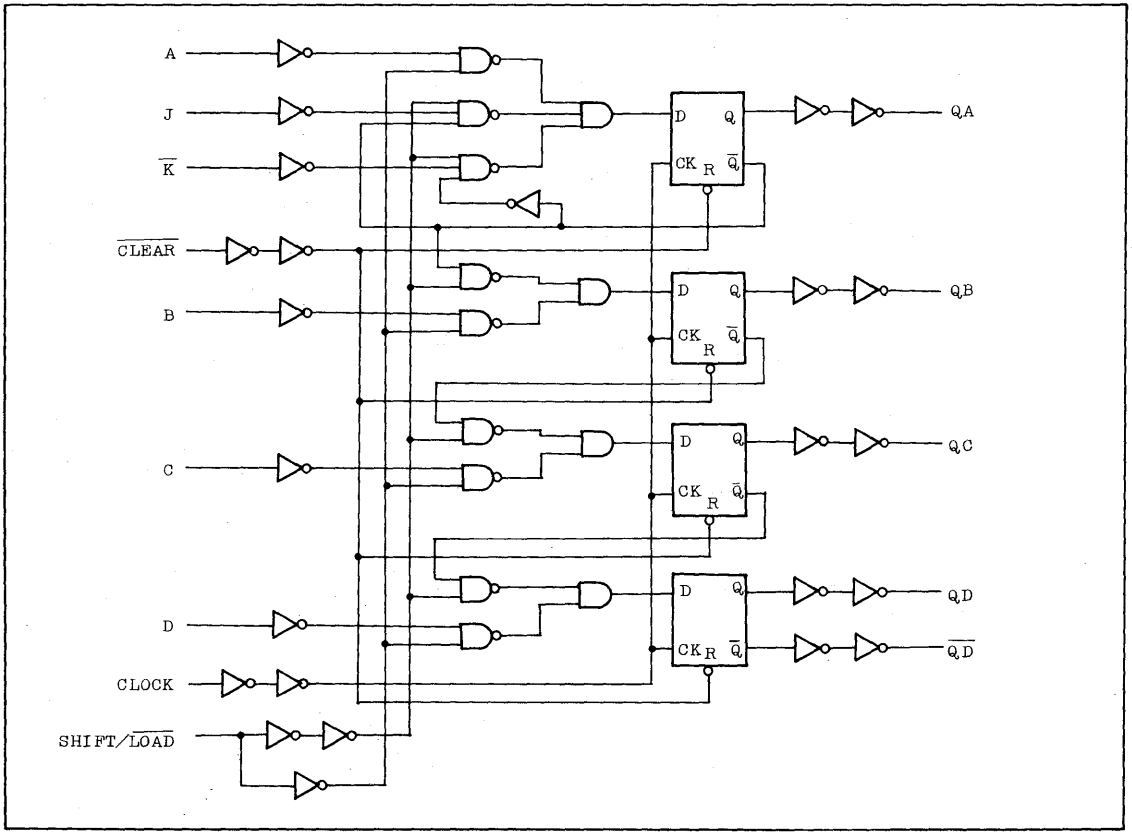
X: Don't care

$Q_{A0} \sim A_{D0}$: No change

$Q_{An} \sim Q_{Dn}$: The level of QA, QB, QC, respectively, before the most-recent positive transition of the clock.

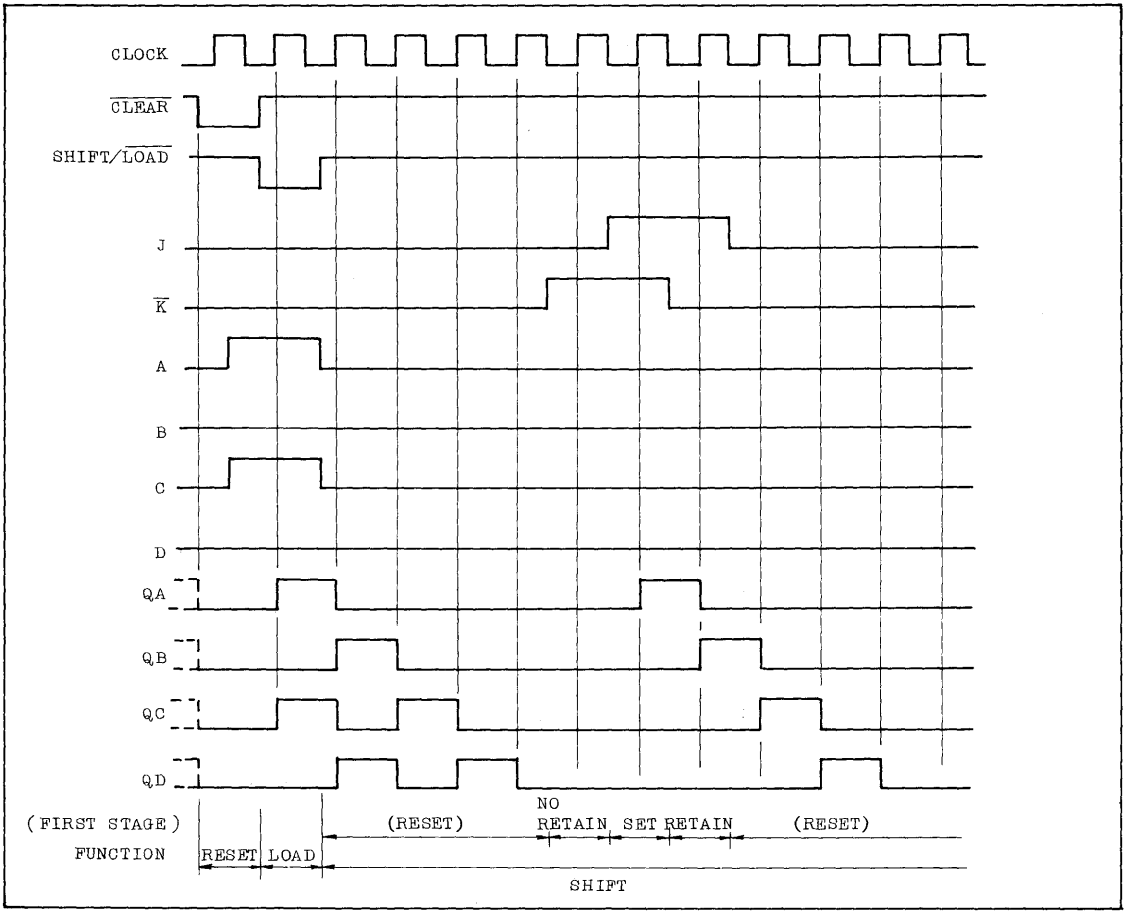
a ...d, $\overline{d}$: The level of steady state input voltage at inputs A ~ D respectively.

LOGIC DIAGRAM



TC74HC195P

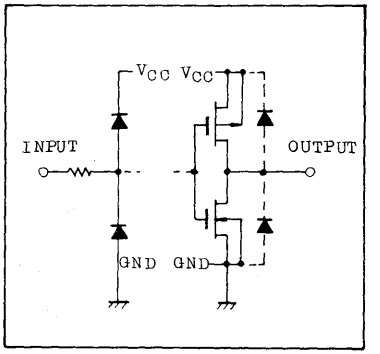
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn, $\overline{QD}$)	t_{pLH}		2.0	-	76	145	-	180	
	t_{pHL}		4.5	-	19	29	-	36	
			6.0	-	16	25	-	31	
Propagation Delay Time ($\overline{CLR}$ - Qn, $\overline{QD}$)	t_{pLH}		2.0	-	84	160	-	200	
	t_{pHL}		4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
Maximum Clock Frequency	f_{MAX}		2.0	6	13	-	5	-	MHz
			4.5	32	51	-	27	-	
			6.0	38	60	-	32	-	

TC74HC195P

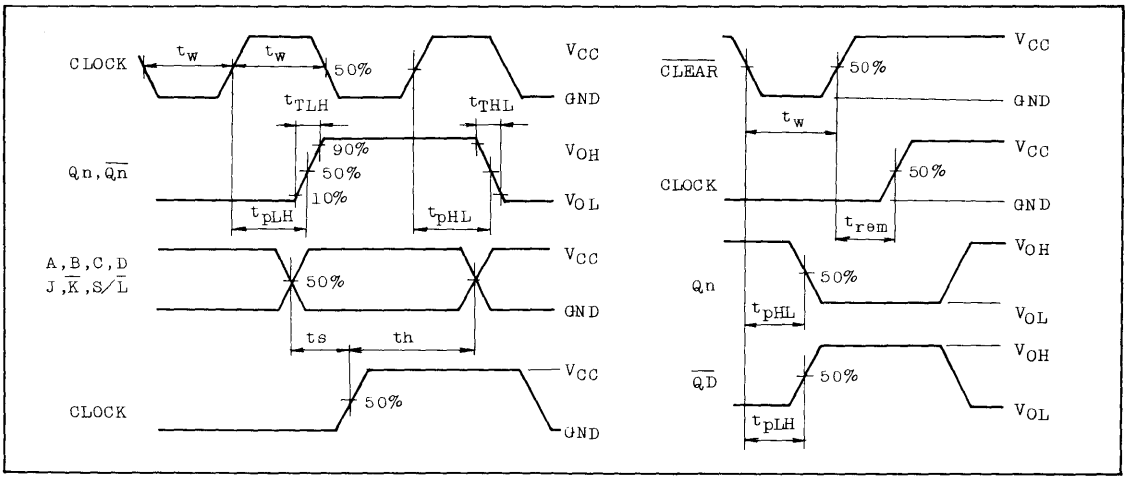
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (PI)	t_s		2.0	-	15	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set Up Time (J, $\overline{K}$, S/$\overline{L}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	1	5	-	6	
			6.0	-	1	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	115	-	-	-	

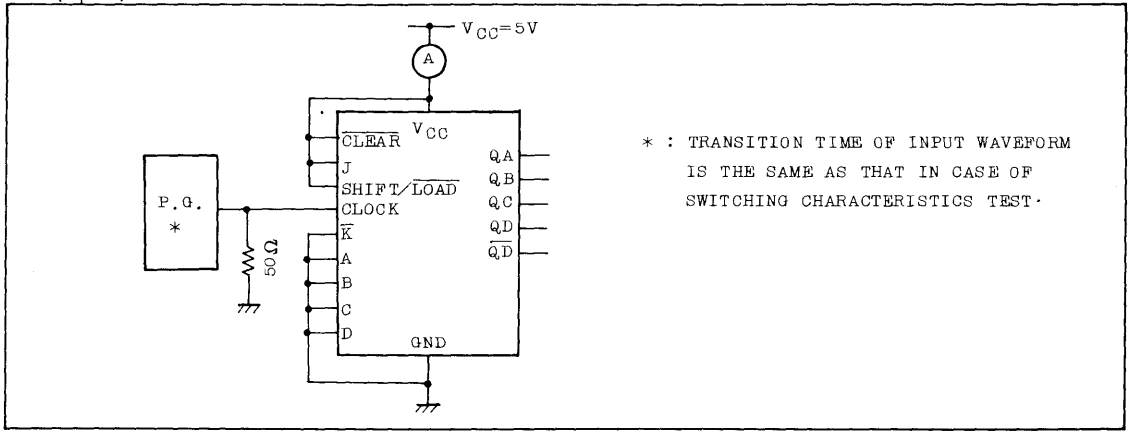
Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC237P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

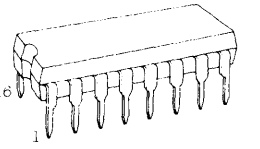
PRELIMINARY

TC74HC237P/F 3-TO-8 LINE DECODER/LATCH

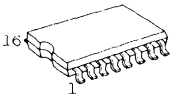
The TC74HC237 is a high speed CMOS 3-TO-8 LINE DECODER ADDRESS LATCH fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of a 3-bit input latches with a common $\overline{GL}$ input and 3-to-8 line decoder with enable input G1 and $\overline{G2}$. The 3-bit binary data is stored into input latch on the "H" level of $\overline{GL}$, determine which one of outputs will go high. Enable input G1 is held "L" level or $\overline{G2}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low.
2 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Inverting type of the 74HC137



DIP16(3D16A-P)



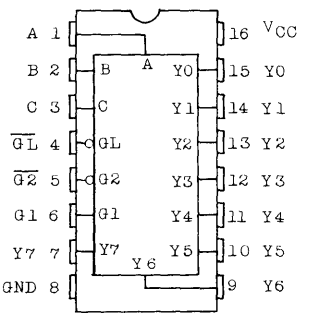
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

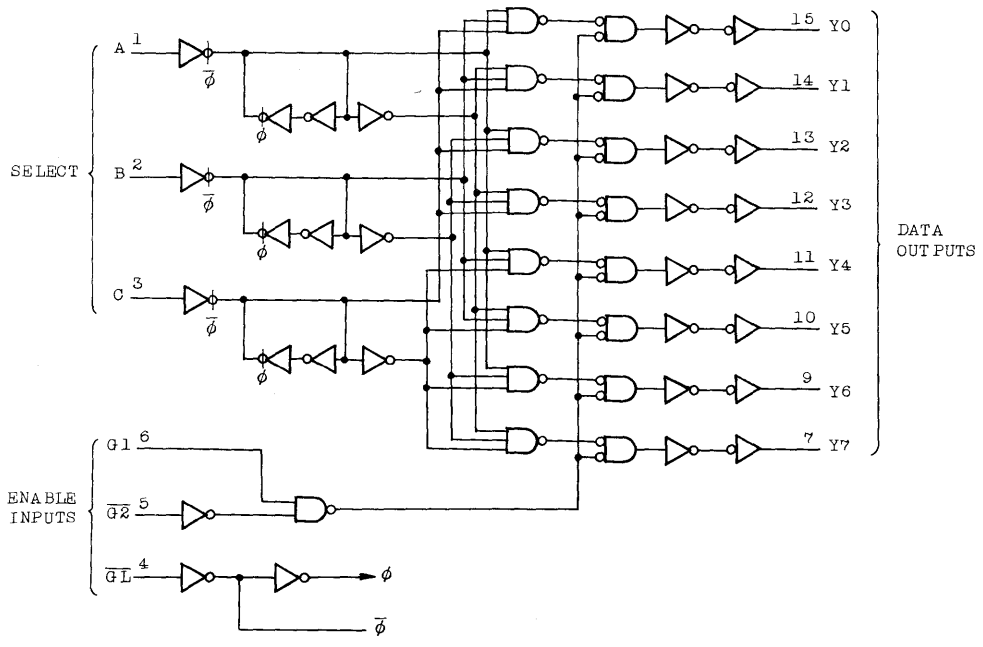
TC74HC237P/F

TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{G1}$	$\overline{G2}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	L	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	L	H	L	L	L	H	L	L	L	L	L	L	L
L	L	H	L	L	H	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	H	L	L	L	L	L
L	L	H	L	H	H	L	L	L	H	L	L	L	L
L	L	H	H	L	L	L	L	L	L	H	L	L	L
L	L	H	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	H	L	L	L	L	L	L	L	H
H	L	H	X	X	X	OUTPUT CORRESPONDING TO STORED ADDRESS, H ; ALL OTHERS, L							

X : DON'T CARE

LOGIC DIAGRAM

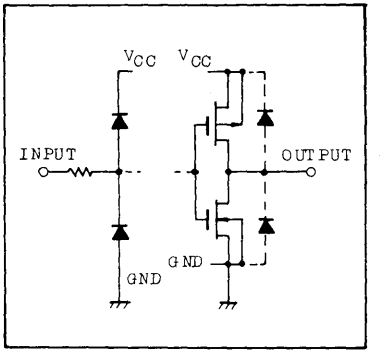


TC74HC237P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

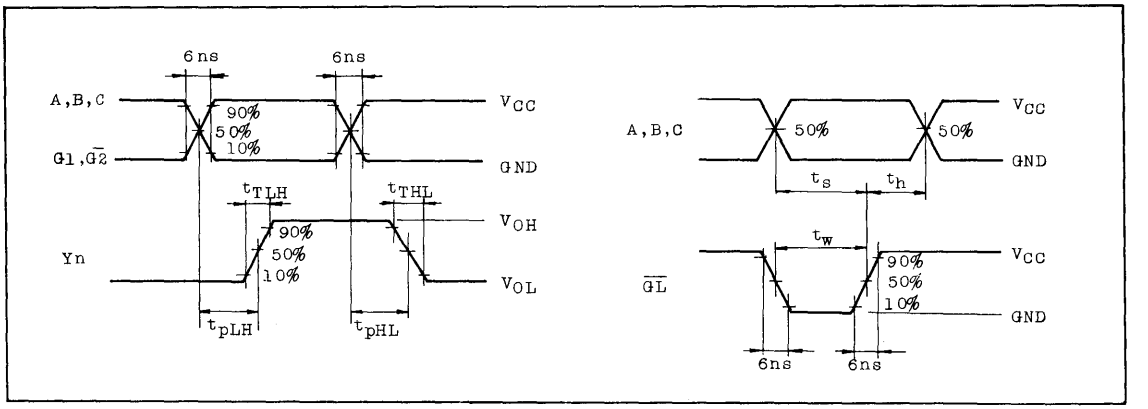
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time ($\overline{GL}$ - Y)	t_{pLH} t_{pHL}		2.0	-	104	200	-	250	
			4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Minimum Pulse Width ($\overline{GL}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set Up Time (A, B, C - $\overline{GL}$)	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (A, B, C - $\overline{GL}$)	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	68	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

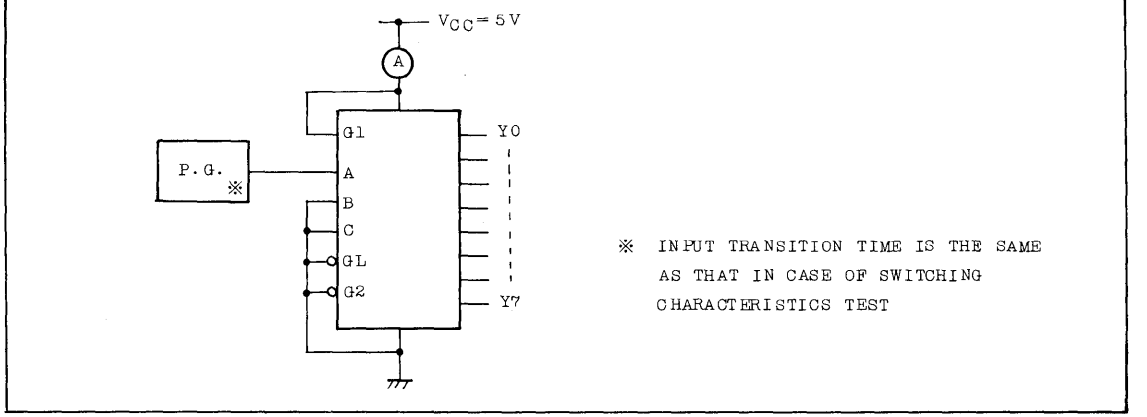
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC237P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



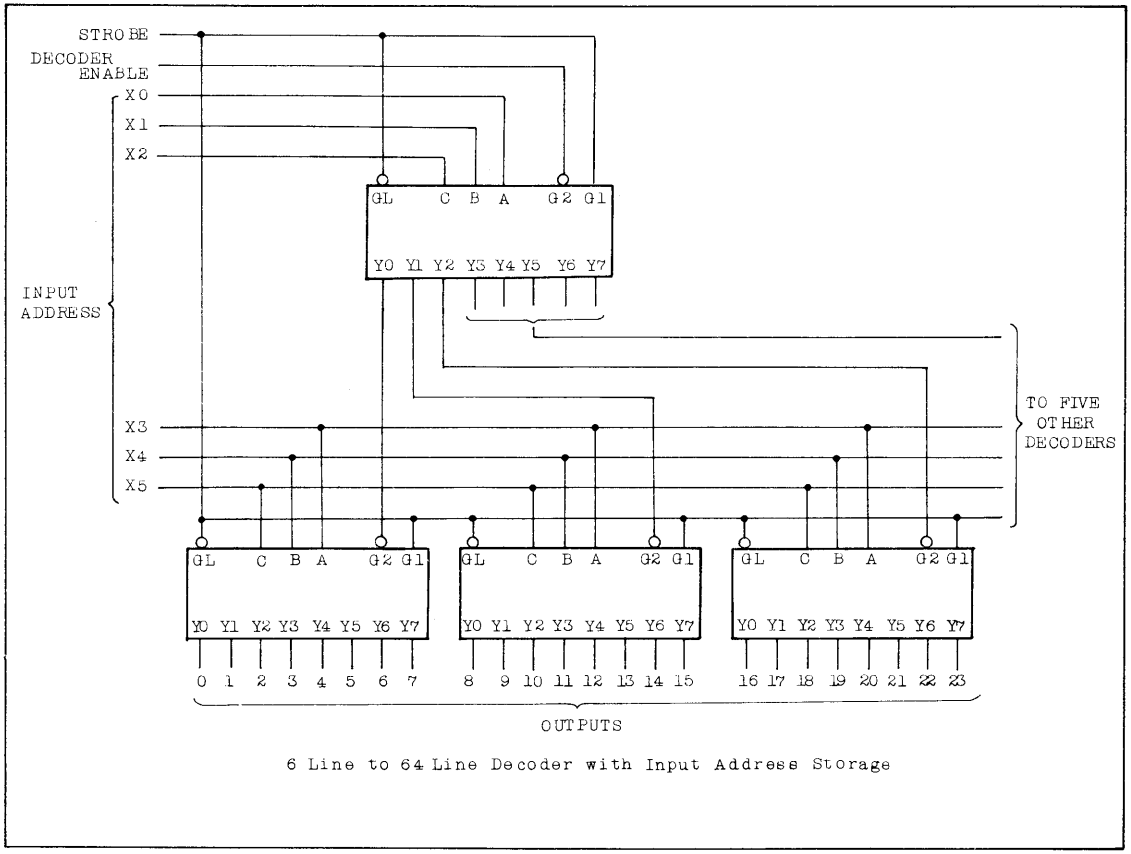
$I_{CC(Opr.)}$ TEST CIRCUIT



※ INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TC74HC237P/F

TYPICAL APPLICATION



6 Line to 64 Line Decoder with Input Address Storage

TC74HC238P

C²MOS DIGITAL INTEGRATED CIRCUIT

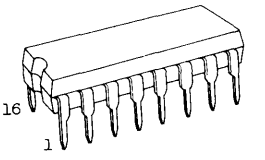
PRELIMINARY

TC74HC238P 3-TO-8 LINE DECODER

The TC74HC238 is a high speed CMOS 3-TO-8 LINE DECODER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. If the device is enabled, 3 binary select inputs (A, B and C) determine which one of outputs will go high. Enable input G1 is held "L" level or either $\overline{G2A}$ or $\overline{G2B}$ is held "H" level, decoding function is inhibited and all the 8 outputs go low. 3 enable inputs are provided to ease cascade connection and application of address decoder for memory system.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=18ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... tpLH≒tpHL
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Noninverting type of the 74HC138



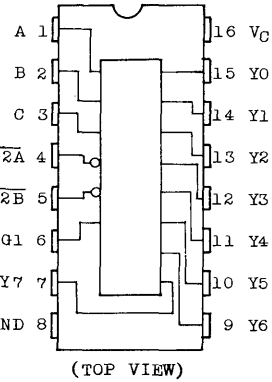
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

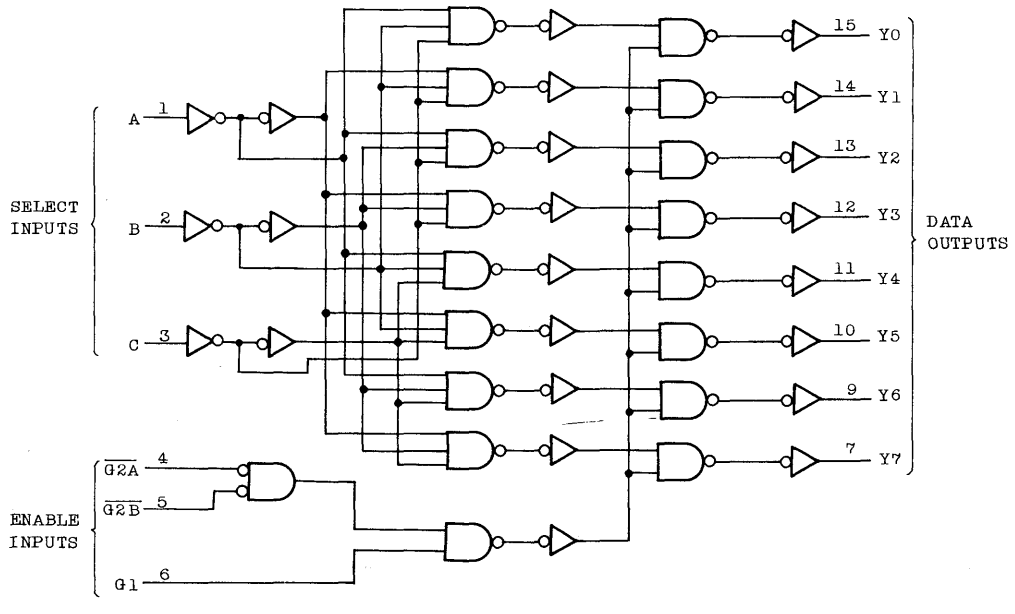
TC74HC238P

TRUTH TABLE

INPUTS						OUTPUTS								SELECTED
ENABLE			SELECT											
$\overline{G2B}$	$\overline{G2A}$	G1	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	OUTPUT
X	X	L	X	X	X	L	L	L	L	L	L	L	L	NONE
X	H	X	X	X	X	L	L	L	L	L	L	L	L	NONE
H	X	X	X	X	X	L	L	L	L	L	L	L	L	NONE
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y0
L	L	H	L	L	H	L	H	L	L	L	L	L	L	Y1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	Y2
L	L	H	L	H	H	L	L	L	H	L	L	L	L	Y3
L	L	H	H	L	L	L	L	L	L	H	L	L	L	Y4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	Y5
L	L	H	H	H	L	L	L	L	L	L	L	H	L	Y6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	Y7

X: Don't care

LOGIC DIAGRAM

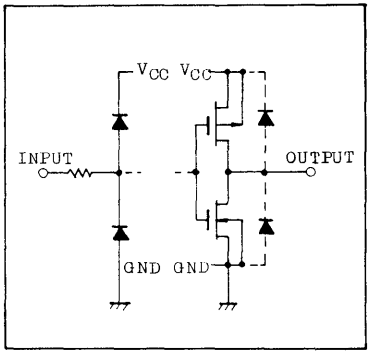


TC74HC238P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC238P

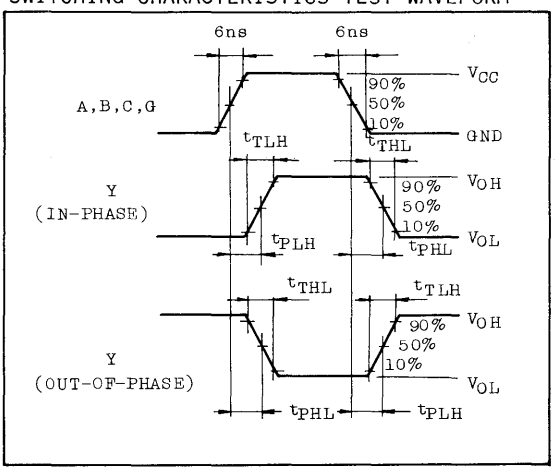
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time (G1 - Y)	t_{pLH} t_{pHL}		2.0	-	80	155	-	195	
			4.5	-	20	31	-	39	
			6.0	-	17	26	-	33	
Propagation Delay Time ($\overline{G2}$ - Y)	t_{pLH} t_{pHL}		2.0	-	88	170	-	215	
			4.5	-	22	34	-	43	
			6.0	-	19	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	67	-	-	-	

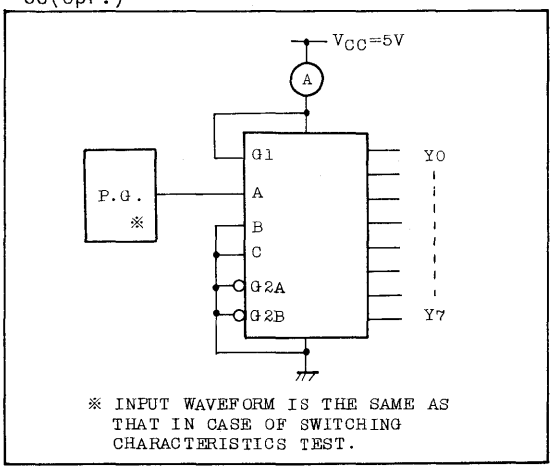
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



※ INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC240P/F • TC74HC241P TC74HC244P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

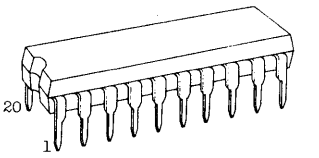
PRELIMINARY

TC74HC240P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HC241P OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS
TC74HC244P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

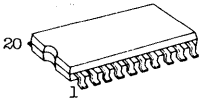
The TC74HC240, TC74HC241 and TC74HC244 are high speed CMOS OCTAL BUS BUFFER's fabricated with silicon C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input govern four BUS BUFFERs.
These divices are designated to be used with 3-state memory address drivers, etc.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS 240/241/244



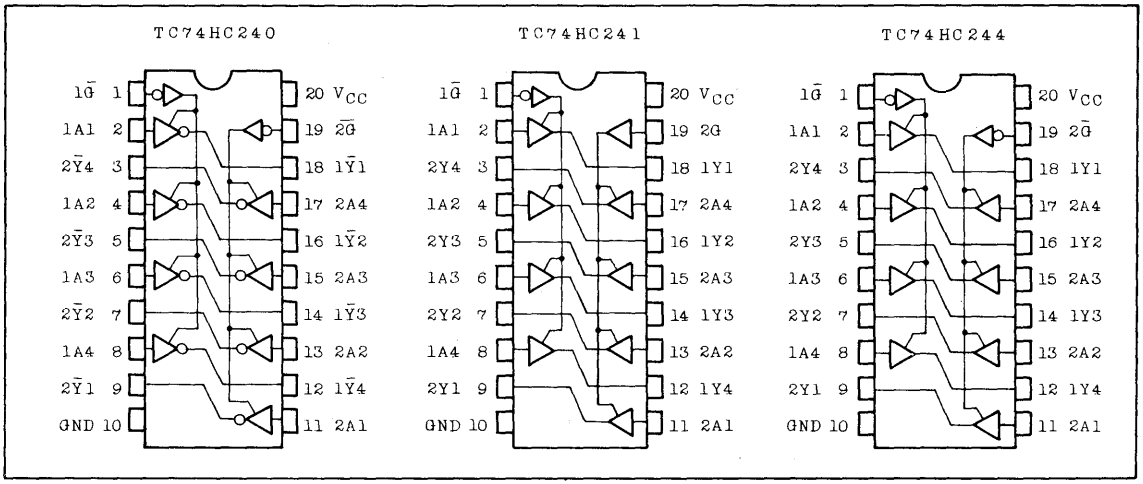
DIP20(3D20A-P)



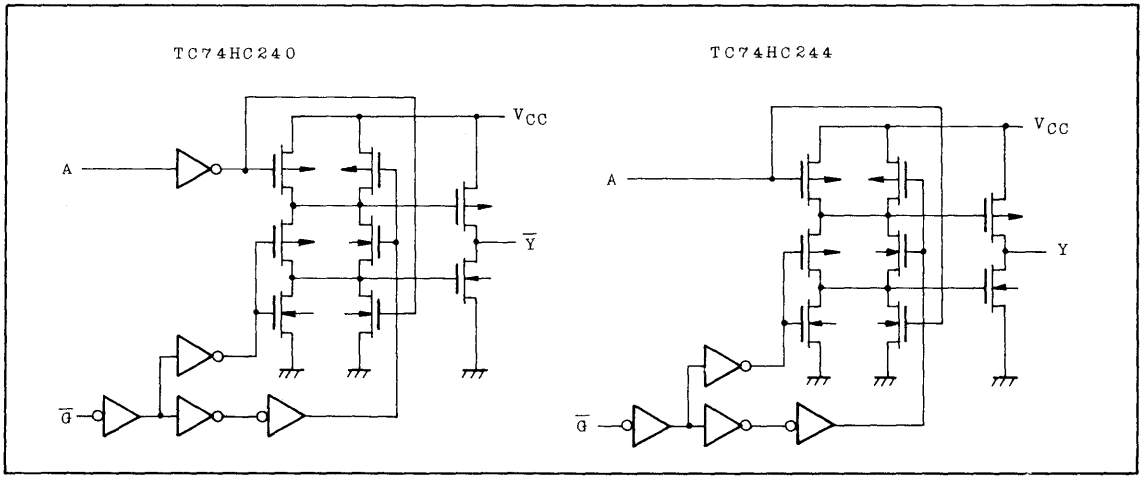
MFP20(F20GA-P)

TC74HC240P/F•TC74HC241P TC74HC244P/F

PIN ASSIGNMENT (TOP VIEW)



CIRCUIT SCHEMATC (1/8 PACKAGE)



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	A_n	Y_n	$\overline{Y}_n$ △△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

△ : Applied only for TC74HC241

△△ : Applied only for TC74HC240

X : Don't Care

Z : High Impedance

TC74HC240P/F • TC74HC241P
TC74HC244P/F

ABSOLUTE MAXIMUM RATINGS

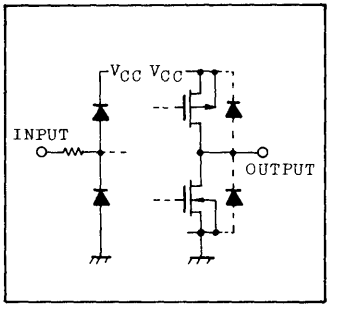
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

TC74HC240P/F • TC74HC241P TC74HC244P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

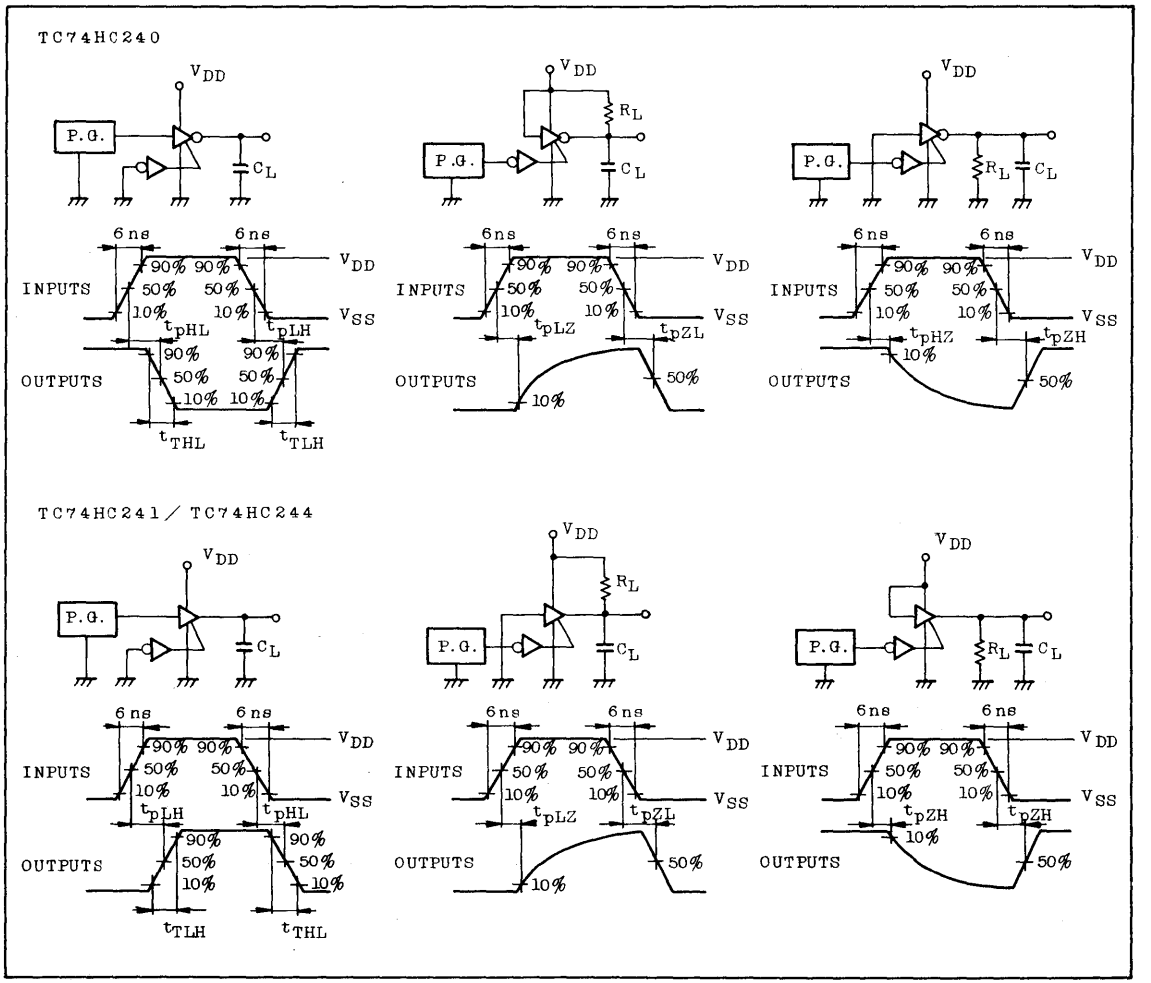
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	
Propagation Delay Time ΔΔ	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Output Enable Time Δ	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	44	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	40	-	-	-	

TC74HC240P/F•TC74HC241P
TC74HC244P/F

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/8$ (per Gate)

(2) Δ : for TC74HC241 only
ΔΔ: for TC74HC240 only

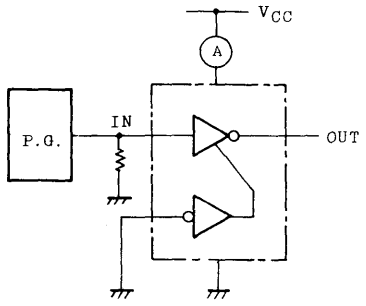
SWITCHING CHARACTERISTICS TEST CIRCUIT

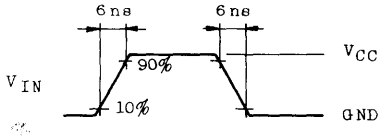


TC74HC240P/F • TC74HC241P TC74HC244P/F

$I_{CC(opr)}$ TEST CIRCUIT

TC74HC240





The other inputs are connected to V_{CC} line or GND line.

TC74HCT240P • TC74HCT241P TC74HCT244P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HCT240P OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS (TTL INPUT LVEL)
TC74HCT241P OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS (TTL INPUT LEVEL)
TC74HCT244P OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS (TTL INPUT LEVEL)

GENERAL DESCRIPTION

The TC74HCT240, TC74HCT241 and TC74HCT244 are high speed CMOS OCTAL BUS BUFFER's fabricated with silicon C^2MOS technology.

These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

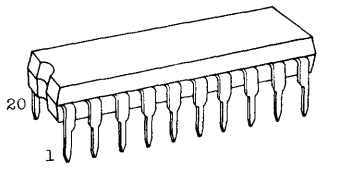
The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. Each control input govern four BUS BUFFERs.

These divices are designated to be used with 3-state memory address drivers, etc.

All inputs are equipped with protection circuits against static discharge or transient excess voltage

FEATURES:

- High Speed ..... t_{pd}=20ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS 240/241/244



DIP20(3D20A-P)

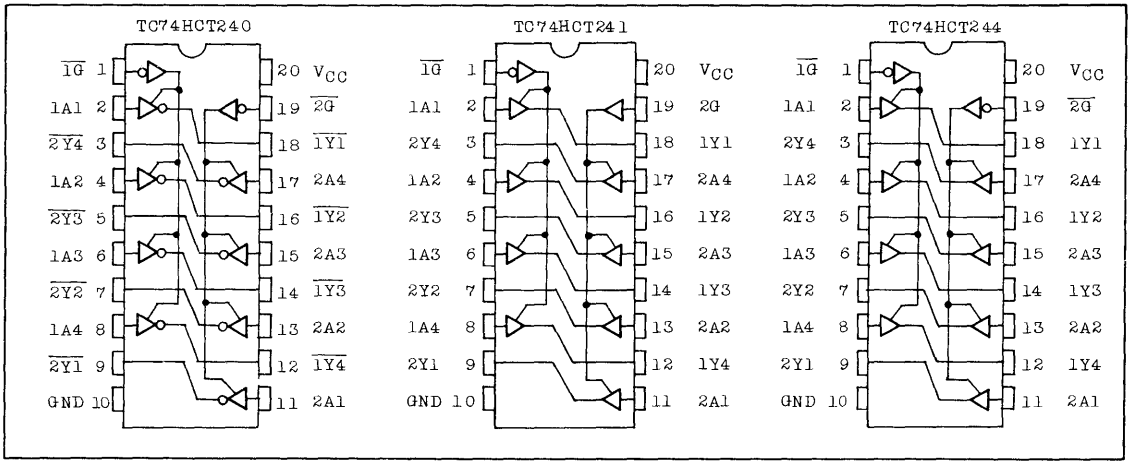
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G}$	G△	An	Yn	$\overline{Yn}$ △△
L	H	L	L	H
L	H	H	H	L
H	L	X	Z	Z

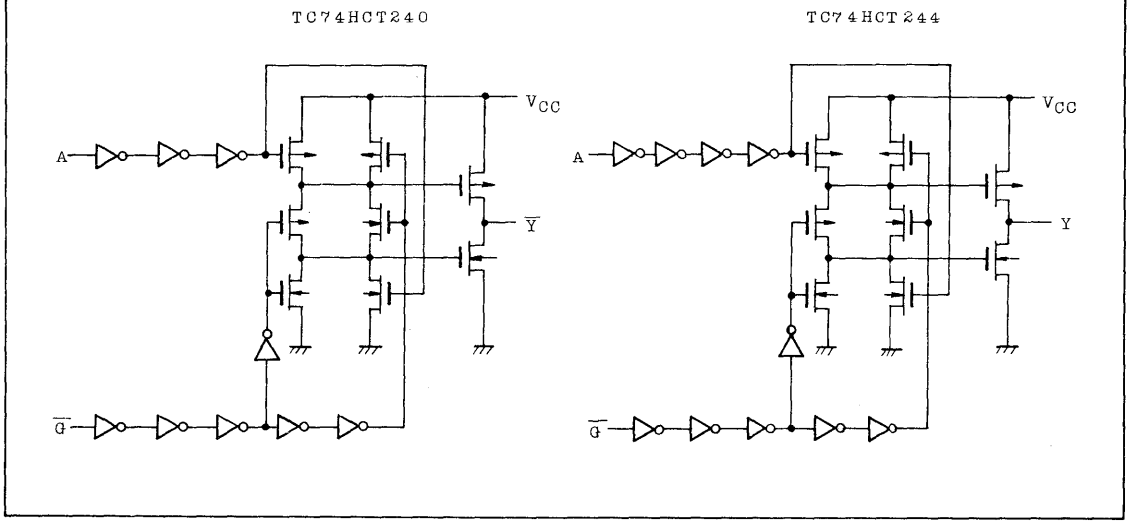
△ : TC74HCT241 ONLY
△△ : TC74HCT240 ONLY
X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HCT240P•TC74HCT241P
TC74HCT244P

PIN ASSIGNMENT (TOP VIEW)



CIRCUIT DIAGRAM (Per Circuit)

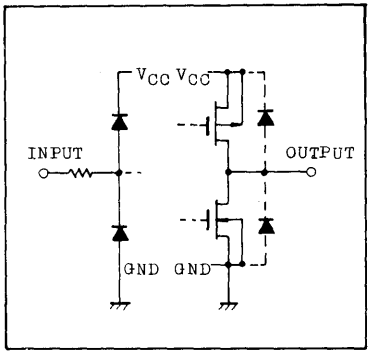


TC74HCT240P·TC74HCT241P TC74HCT244P

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

INPUT and OUTPUT EQUIVALENT CIRCUIT



* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V

TC74HCT240P·TC74HCT241P TC74HCT244P

DC ELECTRICAL CHARACTERISTICS (Continued)

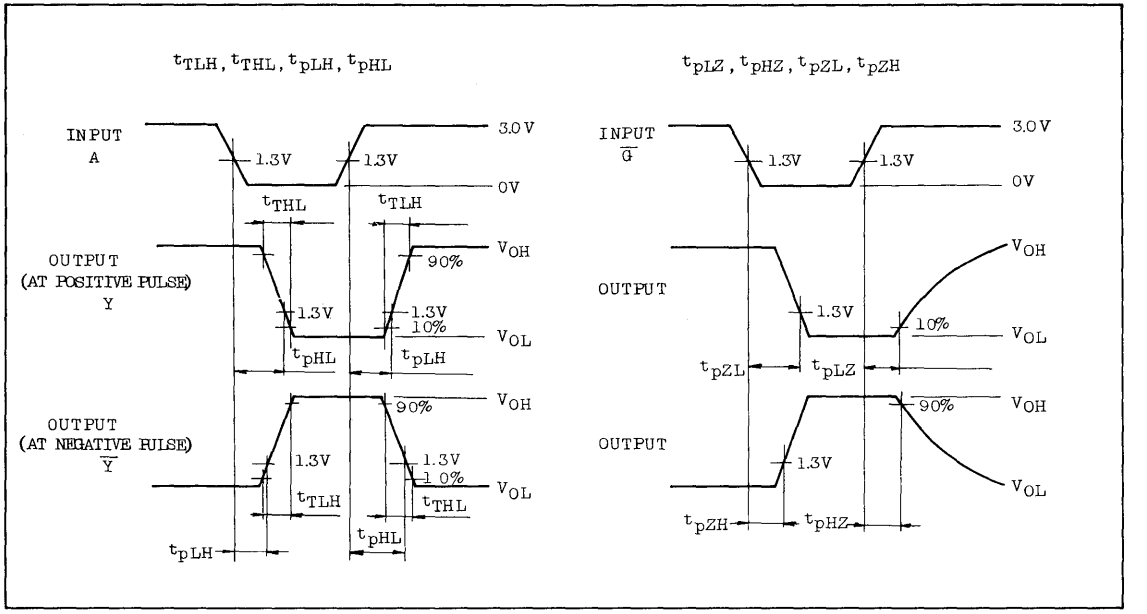
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{TLH}		4.5	-	8	12	-	15	ns
Propagation Delay Time (HCT240)	t_{pLH} t_{pHL}		4.5	-	22	35	-	42	
Propagation Delay Time (HCT241, HCT244)	t_{pLH} t_{pHL}		4.5	-	23	36	-	44	
Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	4.5	-	23	36	-	44	
Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	4.5	-	30	47	-	57	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

TC74HCT240P • TC74HCT241P
TC74HCT244P

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC242P
TC74HC243P

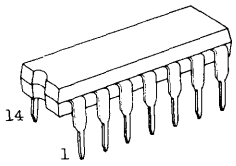
C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

QUAD BUS TRANSCEIVER

TC74HC242P 3-STATE, INVERTING
TC74HC243P 3-STATE, NON-INVERTING

The TC74HC242 and TC74HC243 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by $\overline{GAB}$, GBA. $\overline{GAB}$ and GBA inputs are equipped with protection circuits against static discharge or transient excess voltage.



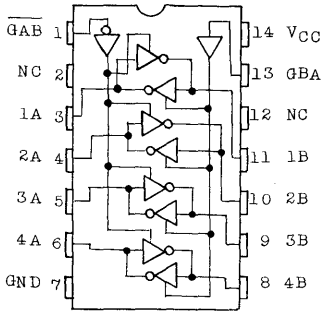
DIP14 (3D14A-P)

FEATURES:

- High Speed ..... t_{pd}=10ns[242] t_{pd}=9ns[243] (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS242/243

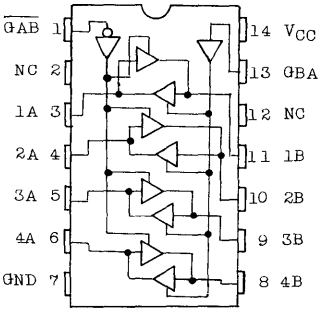
PIN ASSIGNMENT

TC74HC242



(TOP VIEW)

TC74HC243



(TOP VIEW)

NC : NO CONNECTION

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
$\overline{GAB}$	GBA	A BUS	B BUS	HC242	HC243
H	H	OUTPUT	INPUT	$A=\overline{B}$	A=B
L	L	INPUT	OUTPUT	$B=\overline{A}$	B=A
H	L	HIGH IMPEDANCE		Z	Z
L	H	HIGH IMPEDANCE		Z	Z

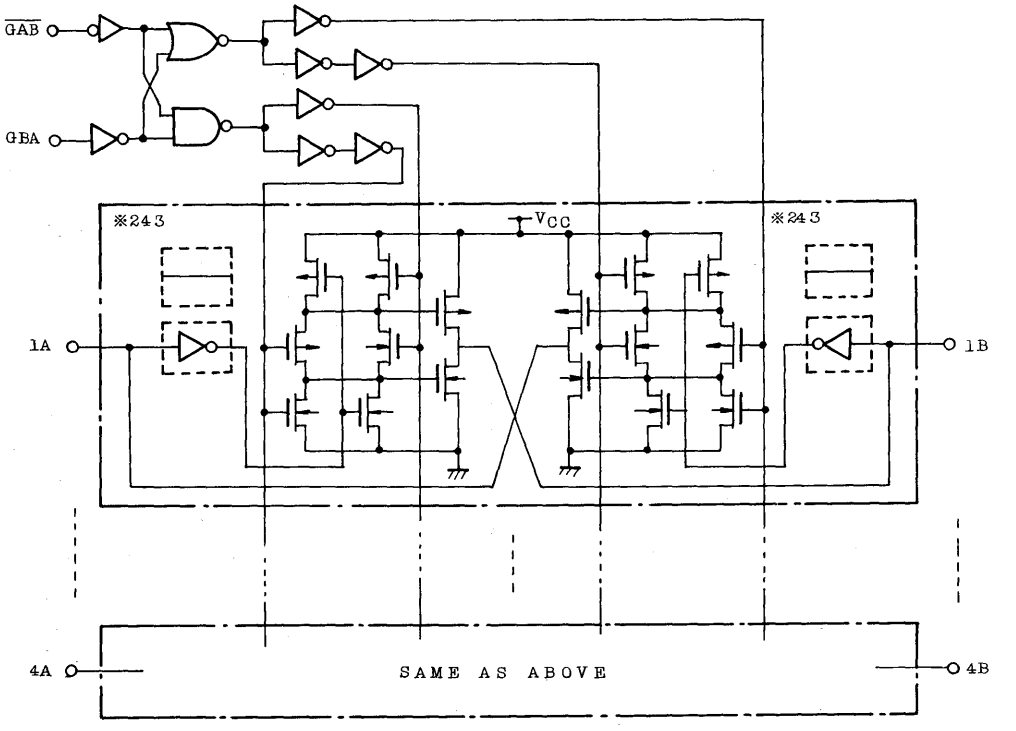
Z : HIGH IMPEDANCE

TC74HC242P
TC74HC243P

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

LOGIC DIAGRAM



In case of TC74HC243, input inverters marked ※ are eliminated.

TC74HC242P
TC74HC243P

ABSOLUTE MAXIMUM RATINGS

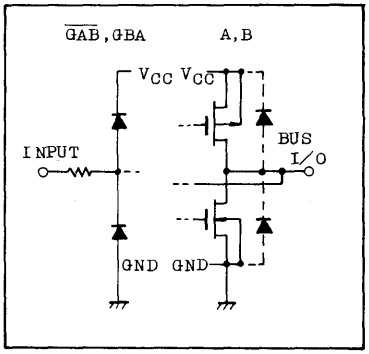
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be a applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

TC74HC242P
TC74HC243P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MIN.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to $\overline{GAB}$, GBA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

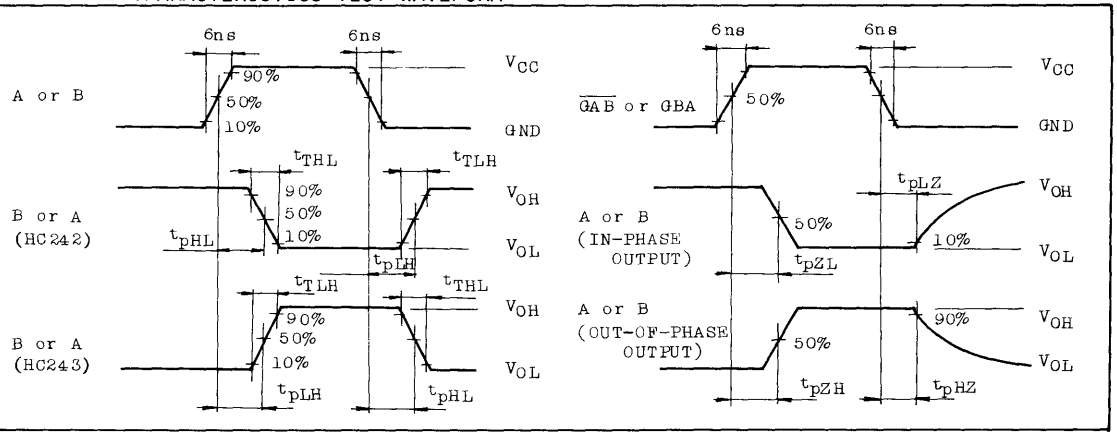
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time	t_{pLH}	TC74HC242	2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
	t_{pHL}	TC74HC243	2.0	-	44	90	-	115	
			4.5	-	11	18	-	23	
			6.0	-	9	15	-	20	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}	$\overline{GAB}$, GBA		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC242		-	42	-	-	-	
		TC74HC243		-	36	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

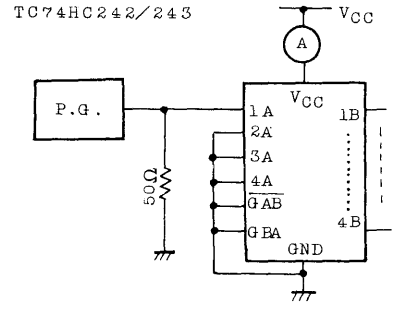
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

TC74HC242P
TC74HC243P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of I_{CC}(Opr.) in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC245P/F • TC74HC640P/F TC74HC643P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

OCTAL BUS TRANSCEIVER

TC74HC245P/F3-STATE, NON-INVERTING

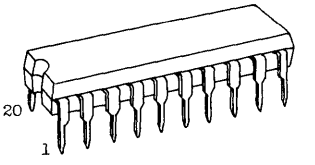
TC74HC640P/F3-STATE, INVERTING

TC74HC643P/F3-STATE, INVERTING AND NON-INVERTING

The TC74HC245, TC74HC640 and TC74HC643 utilize silicon gate C²MOS technology to achieve operating speed equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C²MOS integrated circuit, it possesses the driving capability of 15 LSTTL loads.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS245/640/643

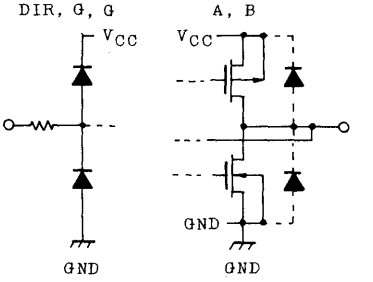


DIP20(3D20A-P)

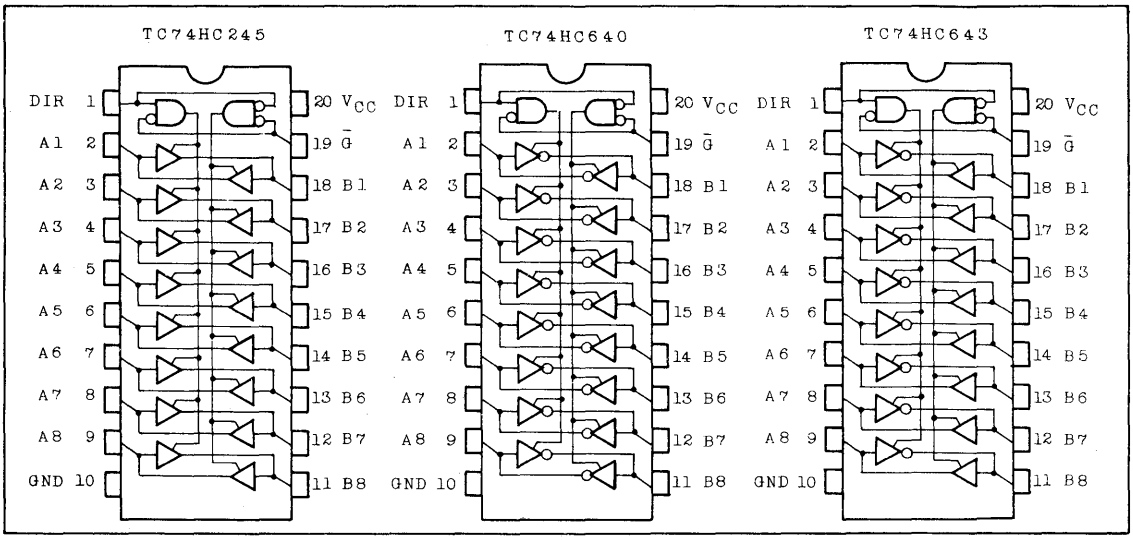
NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

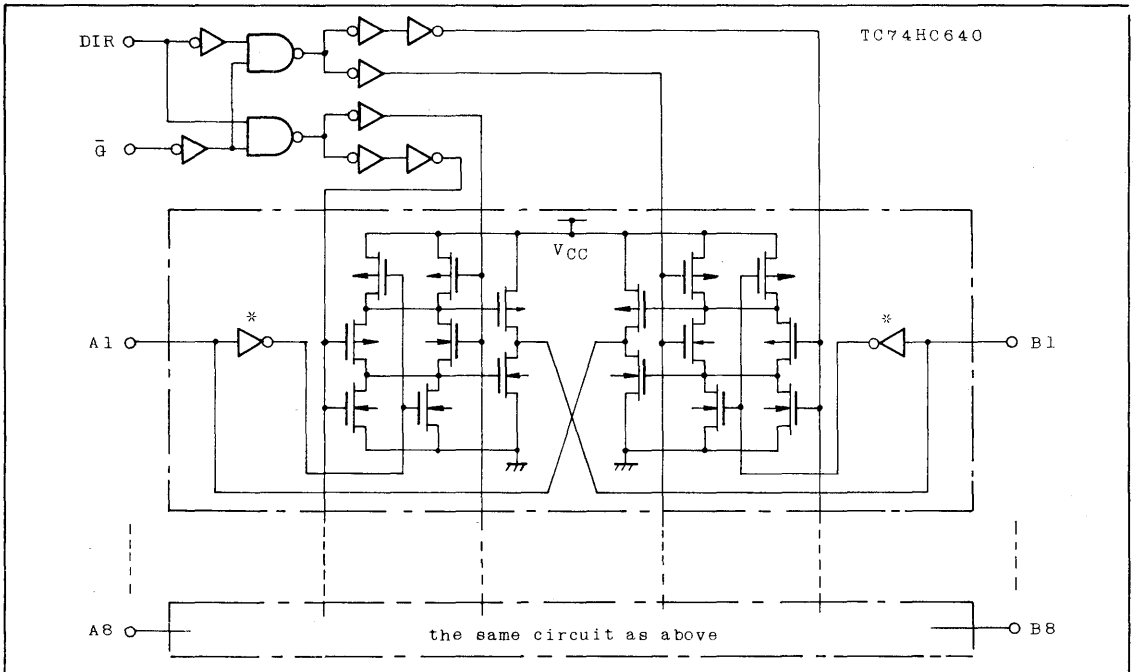
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC245P/F • TC74HC640P/F TC74HC643P/F



LOGIC DIAGRAM



Note. In case of TC74HC245 or TC74HC643, input inverters marked *at A bus and B bus or at B bus are eliminated respectively.

TC74HC245P/F • TC74HC640P/F TC74HC643P/F

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HC245	HC640	HC643
L	L	OUTPUT	INPUT	A = B	A = $\overline{B}$	A = B
L	H	INPUT	OUTPUT	B = A	B = $\overline{A}$	B = $\overline{A}$
H	X	Z		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)/180(MFP)*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

TC74HC245P/F • TC74HC640P/F TC74HC643P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current*	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to DIR, G, $\overline{G}$ input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40 85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{tHL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	48	90	-	115	
			4.5	-	12	18	-	23	
			6.0	-	10	15	-	20	
Propagation Delay Time **	t_{pLH} t_{pHL}		2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	

TC74HC245P/F • TC74HC640P/F TC74HC643P/F

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

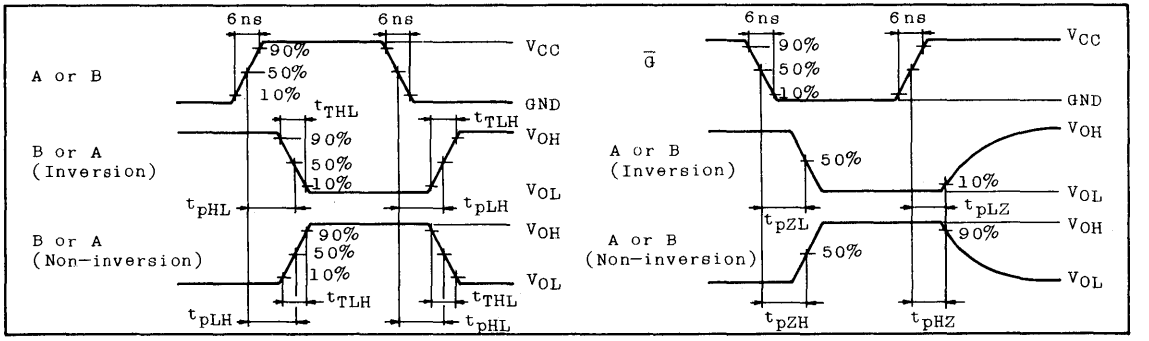
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
3-State Output Enable Time	t_{pZL} / t_{pZH}	R_L=1kΩ	2.0	-	80	160	-	200	ns
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
3-State Output Disable Time	t_{pLZ} / t_{pHZ}	R_L=1kΩ	2.0	-	80	190	-	240	
			4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Input Capacitance	C_{IN}	DIR, G, $\overline{G}$		-	5	10	-	10	pF
Bus Input Capacitance	$C_{I/O}$	A_n, B_n		-	13		-		
Power Dissipation Capacitance	C_{PD}(1)	TC74HC245		-	33	-	-	-	
		TC74HC640/643		-	40	-	-	-	

Note (1) C_{PD} is the value of internal equivalent capacitance calculated from I_{CC} operation without load. Average operating current can be obtained by the following formula.

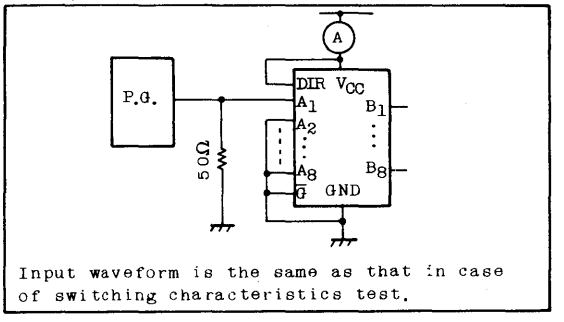
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

(2) *: for TC74HC245 only.
**: for TC74HC640/643 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

TC74HCT245P • TC74HCT640P TC74HCT643P

CMOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

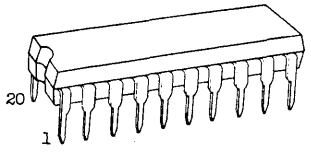
OCTAL BUS TRANCEIVER

TC74HCT245P 3-STATE, NON-INVERTING
TC74HCT640P 3-STATE, INVERTING
TC74HCT643P 3-STATE, INVERTING AND NON-INVERTING

The TC74HCT245, TC74HCT640 and TC74HCT643 utilize silicon gate C^2MOS technology to achieve operating speed equivalent to LSTTL parts.
Along with the low power dissipation and high noise immunity of standard C^2MOS integrated circuit, it possesses the driving capability of 15 LSTTL loads.
The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These IC's are intended for two-way asynchronous communication between data buses, and the direction of data transmission is determined by DIR input.
The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Wide Interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS245/640/643

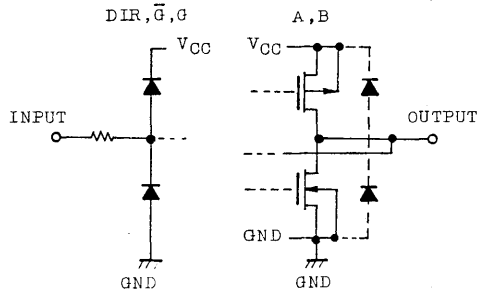


DIP20(3D20A-P)

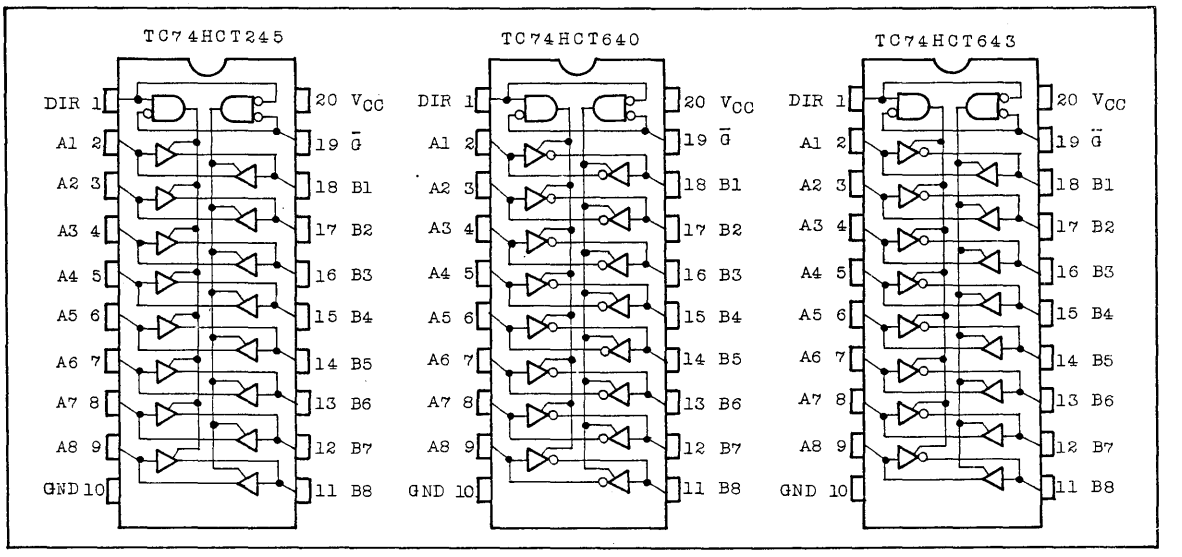
NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

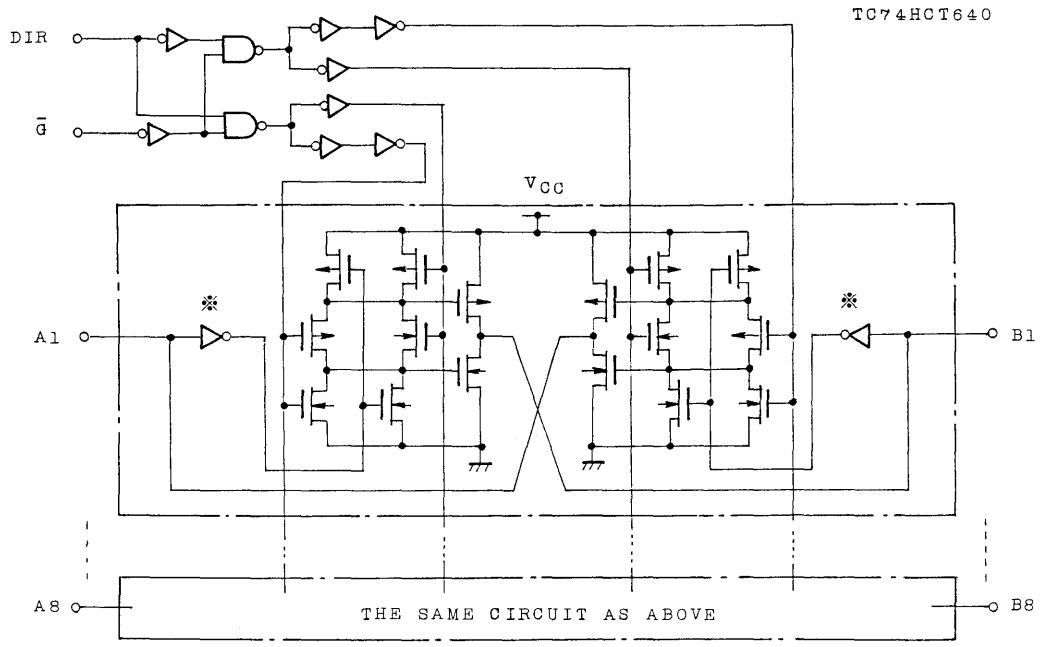
INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT245P TC74HCT640P TC74HCT643P



LOGIC DIAGRAM



Note: In case of TC74HCT245 or TC74HCT643, input inverters marked ※ at A bus and B bus or at B bus are eliminated respectively.

TC74HCT245P TC74HCT640P TC74HCT643P

TRUTH TABLE

INPUT		FUNCTION		OUTPUT		
$\overline{G}$	DIR	A BUS	B BUS	HCT245	HCT640	HCT643
L	L	OUTPUT	INPUT	A = B	A = B	A = B
L	H	INPUT	OUTPUT	B = A	B = A	B = A
H	X	Z		Z	Z	Z

X: Don't Care

Z: High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C, and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	°C

TC74HCT245P TC74HCT640P TC74HCT643P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5	-	4.4	-	V
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.31	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	
	I_C	Per Input: V_{IN}=0.5V or 2.4V Other Input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

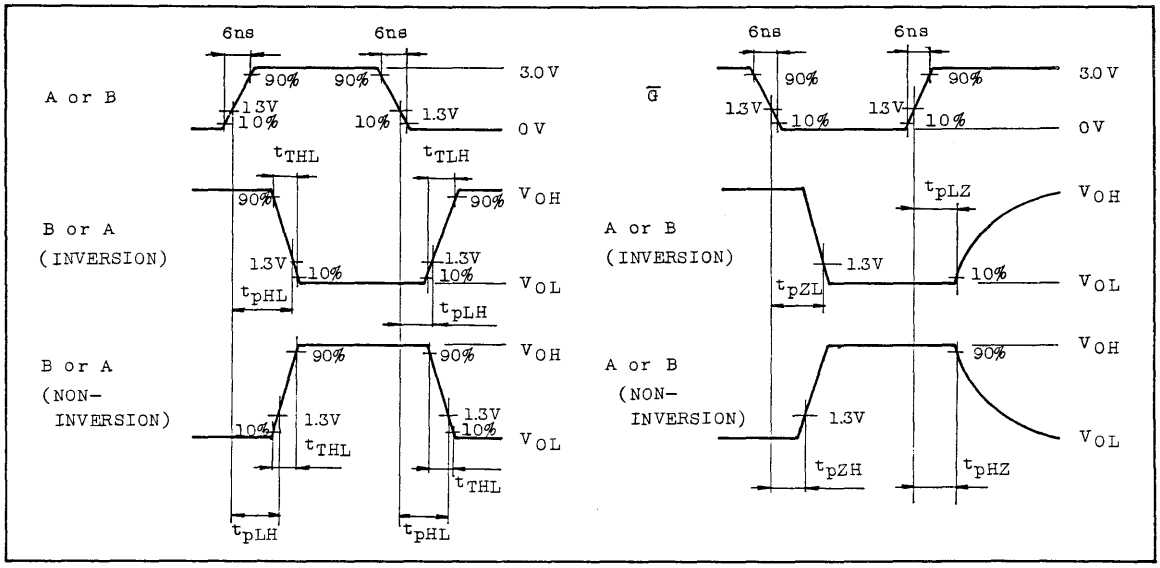
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	12	-	15	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	19	28	-	35	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	27	42	-	53	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	27	40	-	50	
Input Capacitance	C_{IN}	DIR, G, $\overline{G}$		-	5	10	-	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$	TC74HCT245		-	46	-	-	-	
		TC74HCT640/643		-	44	-	-	-	

TC74HCT245P TC74HCT640P TC74HCT643P

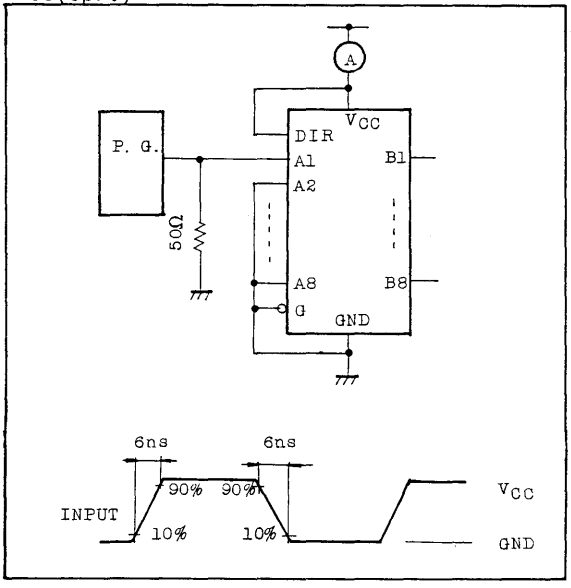
Note (1) C_{PD} is the value of internal equivalent capacitance calculated from I_{CC} operation without load. Average operating current can be obtained by the following formula.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC251P/F

PRELIMINARY

TC74HC251P/F 8-CHANNEL MULTIPLEXER (3-STATE)

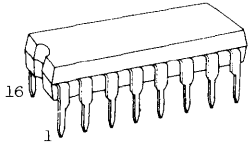
The TC74HC251 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. One of the eight data input signal (D0 ∿ D7) is selected by a three-bit address input (A, B, C) and the selected data will be provided on two outputs; a non-inverting output (Y) and a inverting output (W). When STROBE input is held high, both outputs become high-impedance state.

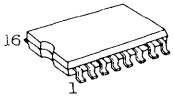
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=19ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS251



DIP16(3D16A-P)



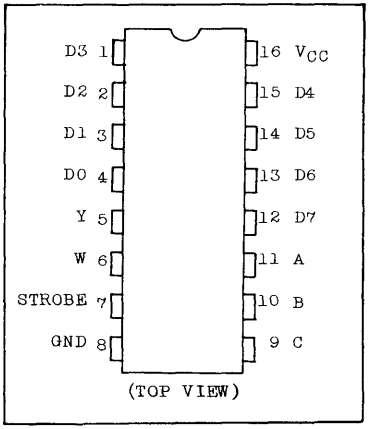
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TC74HC251P/F

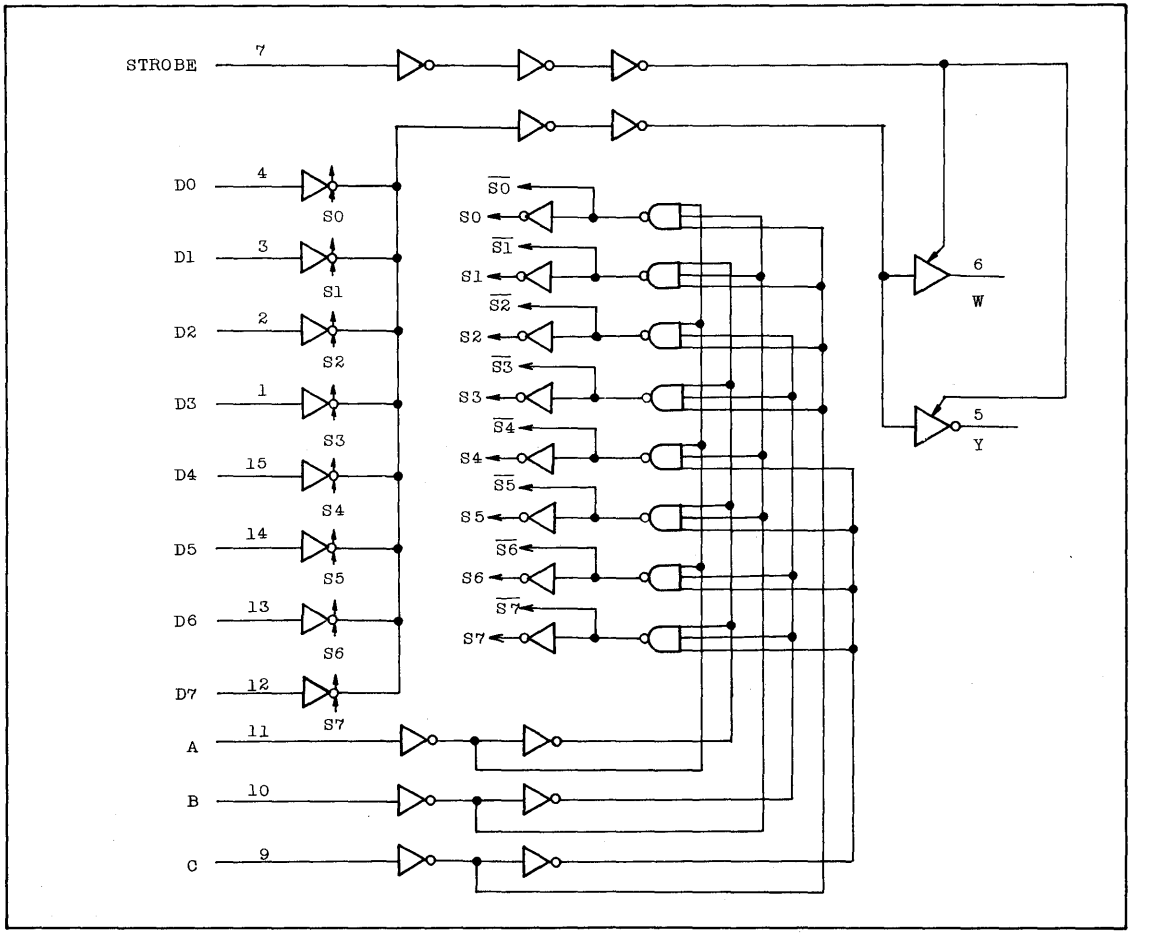
TRUTH TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Z: HIGH IMPEDANCE

X: DON'T CARE

LOGIC DIAGRAM

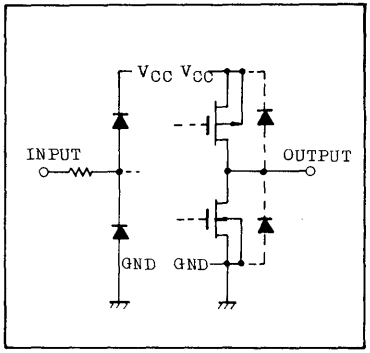


TC74HC251P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TC74HC251P/F

AC ELECTIRCAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

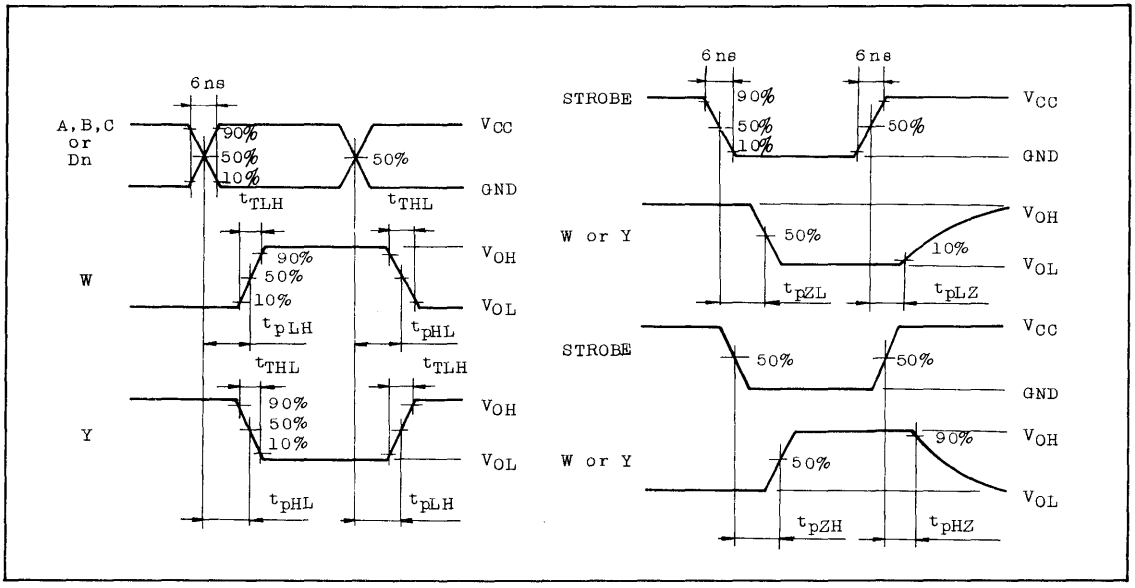
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (D - Y)	t_{pLH} t_{pHL}		2.0	-	76	160	-	200	
			4.5	-	19	32	-	40	
			6.0	-	16	27	-	34	
Propagation Delay Time (D - W)	t_{pLH} t_{pHL}		2.0	-	76	165	-	205	
			4.5	-	19	33	-	41	
			6.0	-	16	28	-	35	
Propagation Delay Time (A, B, C - Y)	t_{pLH} t_{pHL}		2.0	-	96	195	-	245	
			4.5	-	24	39	-	49	
			6.0	-	20	33	-	42	
Propagation Delay Time (D - W)	t_{pLH} t_{pHL}		2.0	-	96	205	-	255	
			4.5	-	24	41	-	51	
			6.0	-	20	35	-	43	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
3-State Output Enable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	60	105	-	130	
			4.5	-	15	21	-	26	
			6.0	-	13	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	100	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

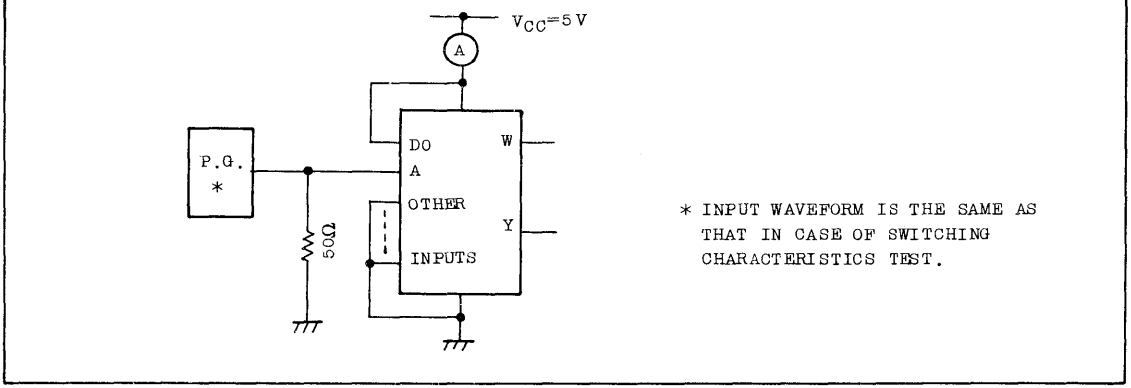
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC251P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC257P/F
TC74HC258P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

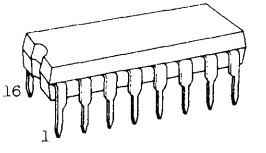
TC74HC257P/F QUAD 2-CHANNEL MULTIPLEXER (3-STATE)

TC74HC258P/F QUAD 2-CHANNEL MULTIPLEXER (3-STATE, INVERTING)

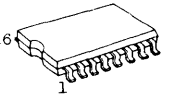
The TC74HC257 and the TC74HC258 are high speed CMOS MULTIPLEXER's fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These IC's are composed of independent 2-channel multiplexer with common SELECT and ENABLE INPUT.
The TC74HC258 is an inverting multiplexer while the TC74HC257 is a non-inverting multiplexer.
If ENABLE INPUT is held "H", outputs of both IC's become high-impedance state.
SELECT INPUT is held "L", A data is chosen, while "H", B data is chosen.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V~6V
- Pin and Function Compatible with 74LS257/258.

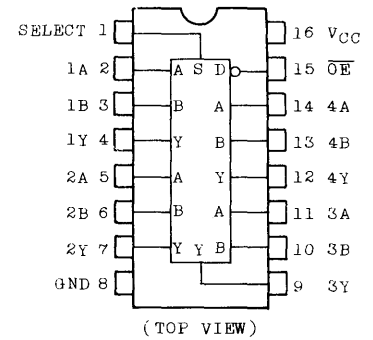


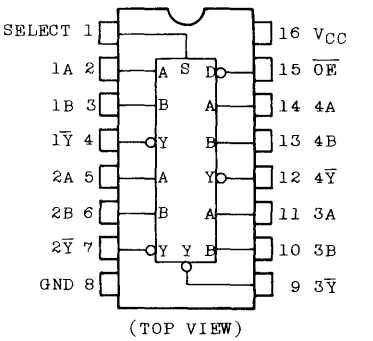
DIP16(3D16A-P)



MFP16(F16GC-P)

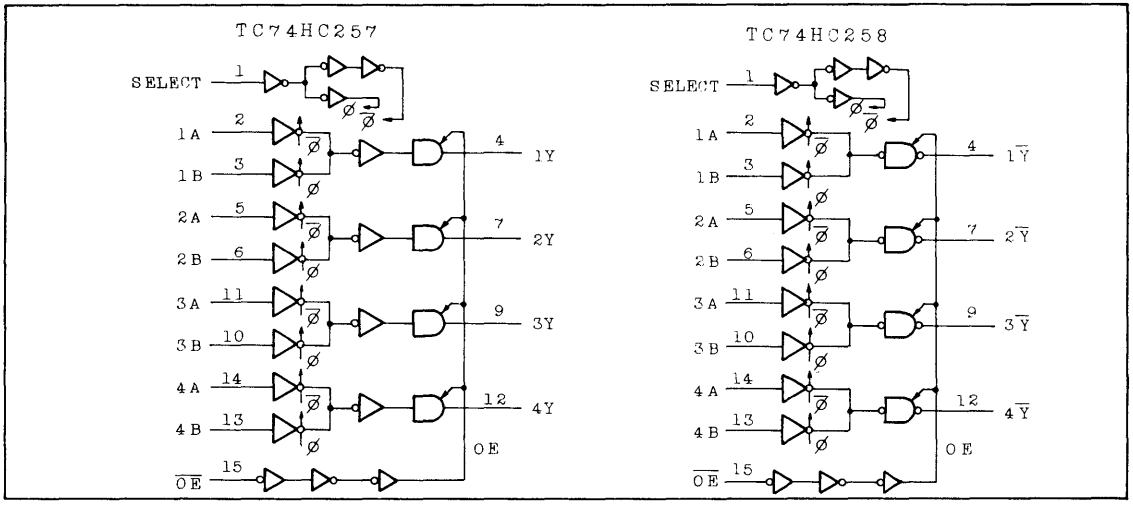
PIN ASSIGNMENT





TC74HC257P/F
TC74HC258P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	SELECT	A	B	Y (257)	$\overline{Y}$ (258)
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

X : Don't care

Z : High impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

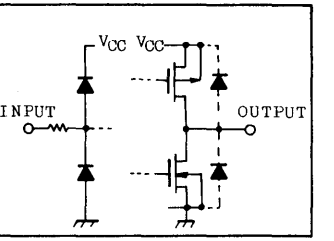
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC257P/F
TC74HC258P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC257P/F
TC74HC258P/F

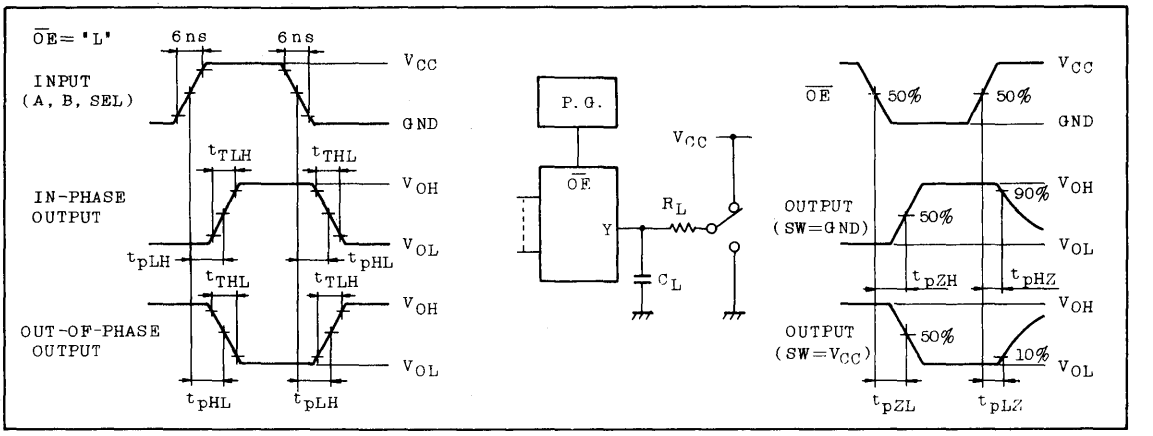
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
TC74HC257 Propagation Delay Time A,B - Y	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
SELECT -Y	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
TC74HC258 Propagation Delay Time A,B - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	52	100	-	125	
			4.5	-	13	20	-	25	
			6.0	-	11	17	-	21	
SELECT - $\overline{Y}$	t_{pLH} t_{pHL}		2.0	-	84	160	-	200	
			4.5	-	21	32	-	40	
			6.0	-	18	27	-	34	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	80	140	-	175	
			4.5	-	20	28	-	35	
			6.0	-	17	24	-	30	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC257		-	60	-	-	-	
		TC74HC258		-	59	-	-	-	

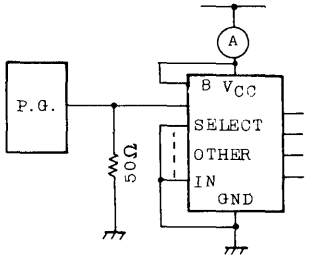
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\ f_{IN}+I_{CC}/4$ (per Channel)

TC74HC257P/F
TC74HC258P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC259P/F

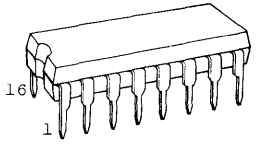
PRELIMINARY

TC74HC259P/F 8-BIT ADDRESSABLE LATCH

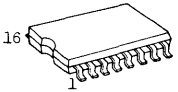
The TC74HC259 is a high speed CMOS 8-BIT ADDRESSABLE LATCH fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The respective bits are controlled by A, B and C inputs. When $\overline{CLEAR}$ input is held "H" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "L" level, the data is written into the bit selected by A, B and C inputs, the other bits hold their previous conditions. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$($\overline{G}$) input held "H" level, write of all bits is inhibited regardless of A, B and C input, and their previous conditions are held. When $\overline{CLEAR}$ input is held "L" level and $\overline{ENABLE}$ ($\overline{G}$) input is held "H" level, all bits are reset to "L" level regardless of the other inputs. When both of $\overline{CLEAR}$ input and $\overline{ENABLE}$ ($\overline{G}$) input held "L" level, all bits which isn't selected by A, B and C inputs are reset to "L" level. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS259



DIP16(3D16A-P)



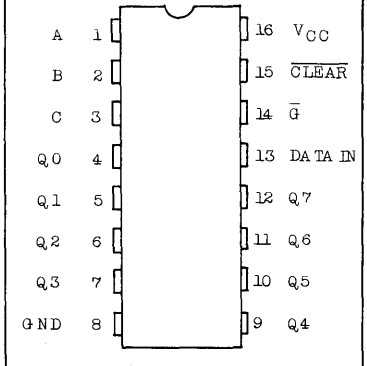
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC259P/F

TRUTH TABLE

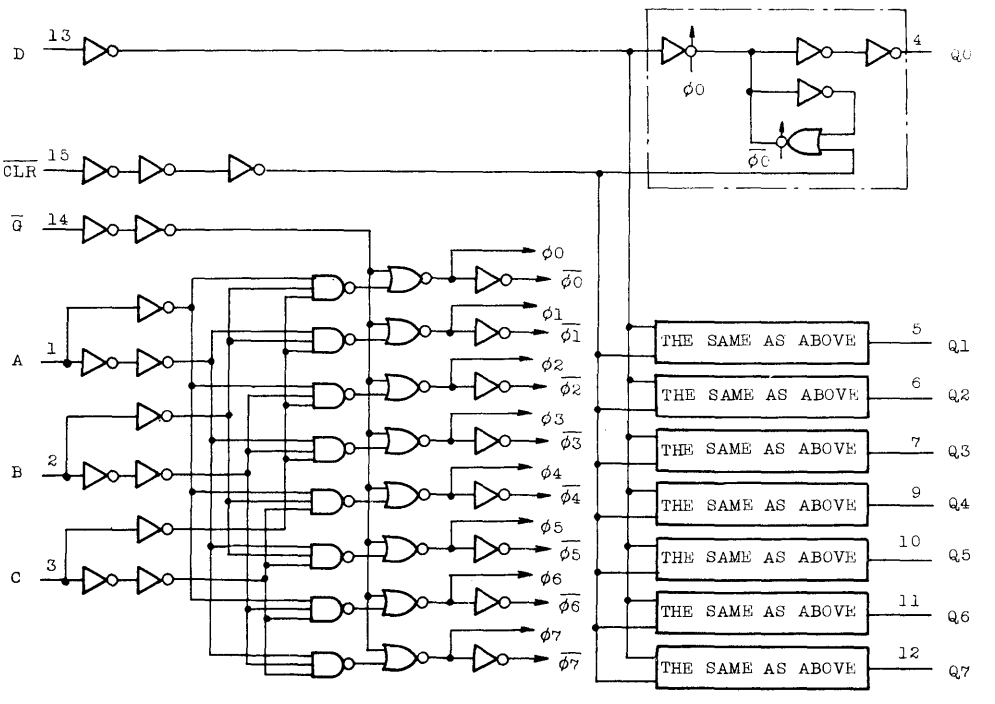
INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{CLEAR}$	$\overline{G}$			
H	L	D	Q_{i0}	ADDRESSABLE LATCH
H	H	Q_{i0}	Q_{i0}	MEMORY
L	L	D	L	8-LINE DEMULTIPLEXER
L	H	L	L	CLEAR ALL BITS TO "L"

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	Q0
L	L	H	Q1
L	H	L	Q2
L	H	H	Q3
H	L	L	Q4
H	L	H	Q5
H	H	L	Q6
H	H	H	Q7

D : THE LEVEL AT THE DATA INPUT

Q_{i0} : THE LEVEL BEFORE THE INDICATED STEADY-STATE INPUT CONDITIONS WERE ESTABLISHED, (i = 0, 1, ····· , 7).

LOGIC DIAGRAM

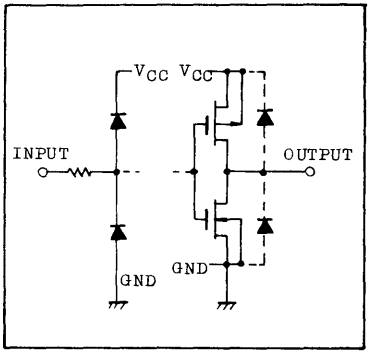


TC74HC259P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC259P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

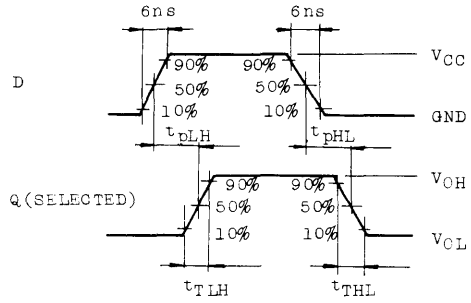
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q)	t_{pLH}		2.0	-	64	130	-	165	
	t_{pHL}		4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time (A, B, C - Q)	t_{pLH}		2.0	-	96	190	-	240	
	t_{pHL}		4.5	-	24	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time ($\overline{G}$ - Q)	t_{pLH}		2.0	-	84	165	-	205	
	t_{pHL}		4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Propagation Delay Time ($\overline{CLEAR}$ - Q)	t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	15	23	-	29	
Minimum Pulse Width ($\overline{G}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (DATA)	t_s		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Set-up Time (A, B, C)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Hold Time (DATA)	t_h		2.0	-	10	25	-	30	
			4.5	-	2	5	-	6	
			6.0	-	2	5	-	5	
Minimum Hold Time (A, B, C)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	32	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

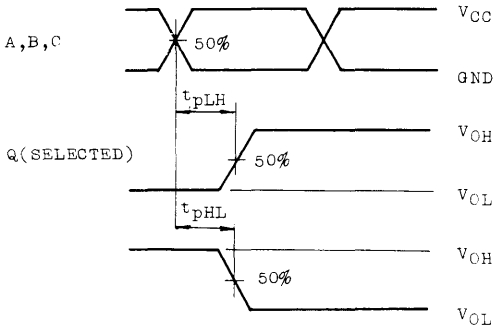
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

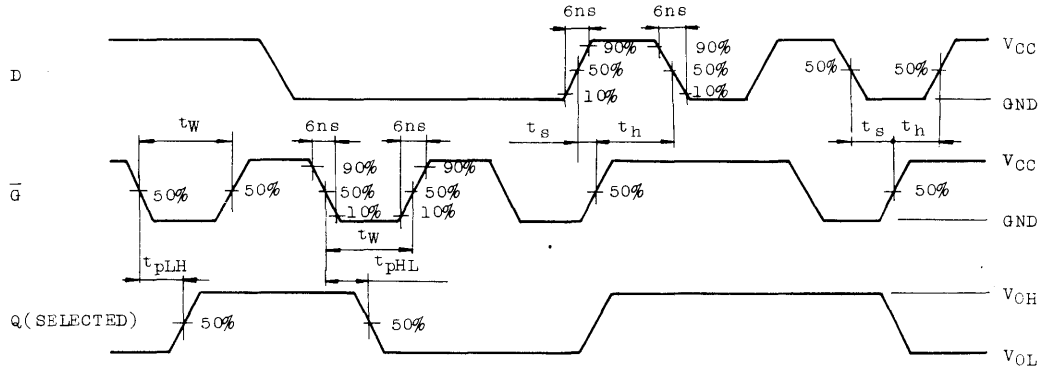
WAVEFORM 1. ($\overline{G}$=L, $\overline{CLR}$=H, A~C=STABLE)



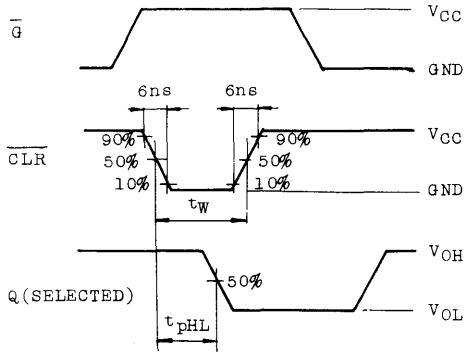
WAVEFORM 2. ($\overline{G}$=L)



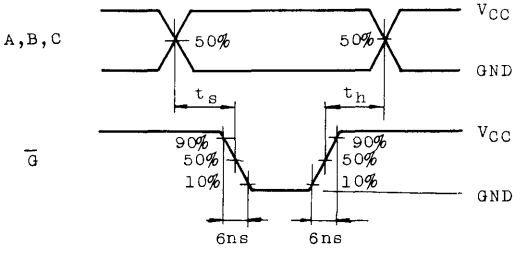
WAVEFORM 3. ($\overline{CLR}$=H, A~C=STABLE)



WAVEFORM 4. (D=H, A~C=STABLE)

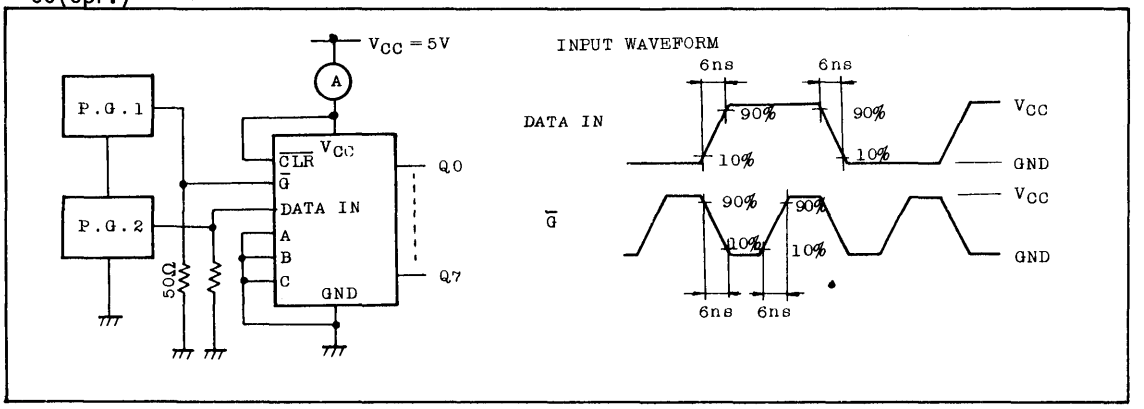


WAVEFORM 5. ($\overline{CLR}$=H)



TC74HC259P/F

$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC273P/F

PRELIMINARY

TC74HC273P/F OCTAL D-TYPE FLIP FLOP WITH CLEAR

The TC74HC273 is a high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achives the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation.

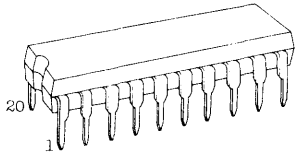
Information signals applied to D inputs are transfered to the Q outputs on the positive-going edge of the clock pulse.

When the $\overline{\text{CLEAR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

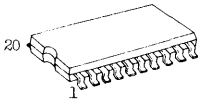
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=48MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH} ≈ t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS273

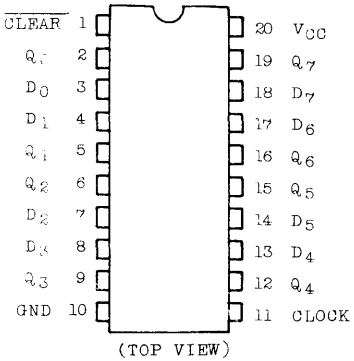


DIP20(3D20A-P)



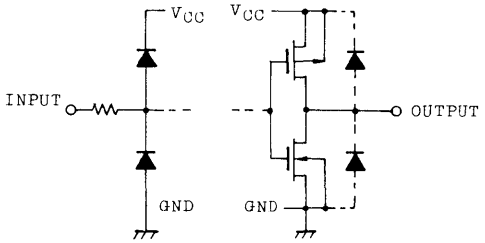
MFP20(F20GA-P)

PIN ASSIGNMENT



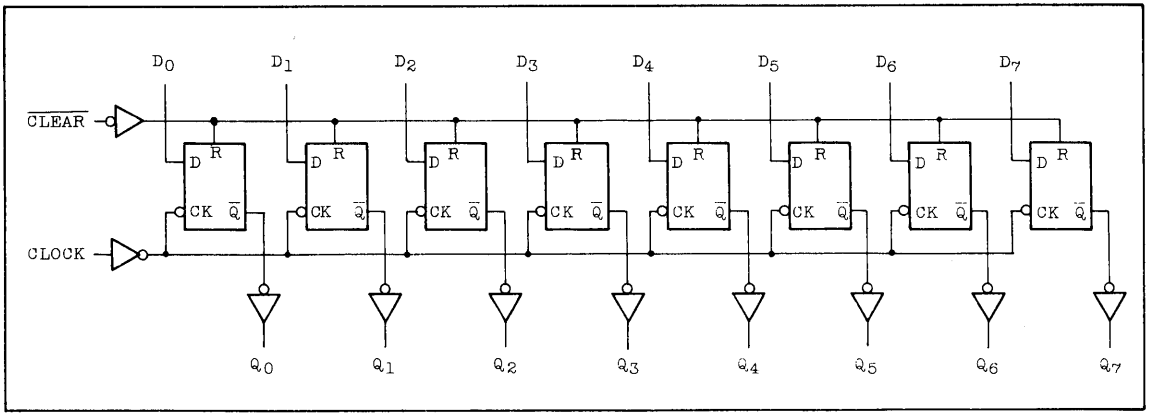
(TOP VIEW)

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC273P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{CLEAR}$	D	CLOCK	Q	
L	X	X	L	Clear
H	L	↑	L	-
H	H	↑	H	-
H	X	↓	Qn	No change

X: Don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=60°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC273P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Propagation Delay Time CLOCK - Q	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time $\overline{\text{CLEAR}}$ - Q	t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Maximum Clock Frequency	f_{MAX}		2.0	5	11	-	4	-	MHz
			4.5	27	44	-	22	-	
			6.0	32	52	-	26	-	
Minimum Pulse Width CLOCK	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width $\overline{\text{CLEAR}}$	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time $\overline{\text{CLEAR}}$	t_{rem}		2.0	-	15	75	-	95	
			4.5	-	4	15	-	19	
			6.0	-	3	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	53	-	-	-	

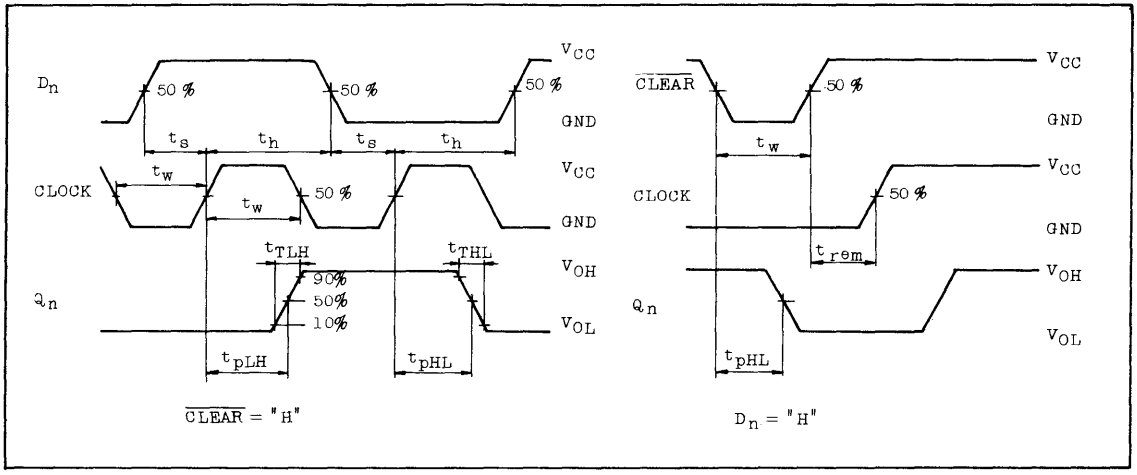
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per Flip Flop)

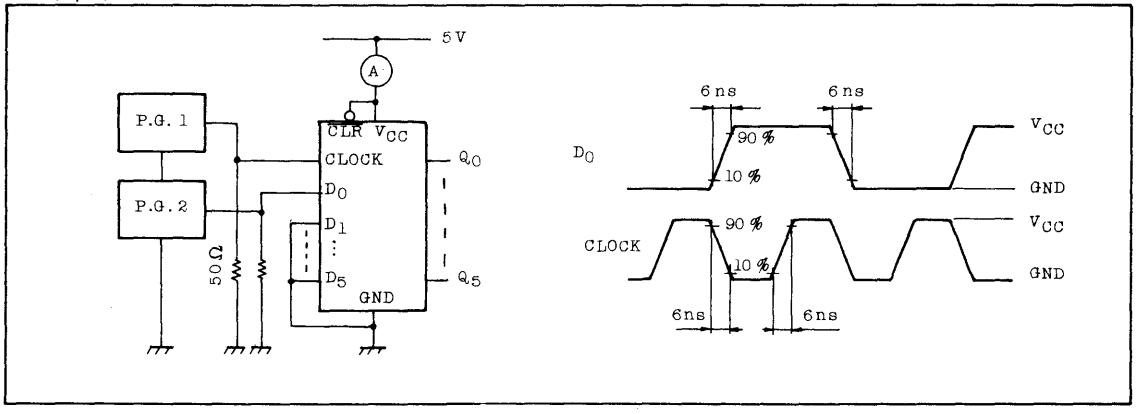
And the total C_{PD} when n pcs of Flip Flop operate can be gained by the following equation.

$C_{PD(total)} = 38 + 15 \cdot n$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



TC74HC279P

C²MOS DIGITAL INTEGRATED CIRCUIT

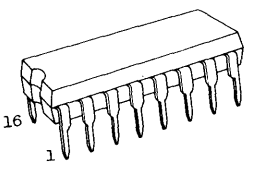
PRELIMINARY

TC74HC279P QUAD S-R LATCH

The TC74HC279 is a high speed CMOS QUAD S-R LATCH fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
Each latch has an independent Q output and set and reset inputs. $\overline{S}$ and $\overline{R}$ are accomplished by "L" level. When $\overline{S}$ input is placed at "L", Q output becomes "H" and when $\overline{R}$ input is placed at "L", Q output becomes "L". When both of $\overline{S}$ and $\overline{R}$ are placed at "L", $\overline{S}$ takes precedence resulting Q="H" and when both of $\overline{S}$ and $\overline{R}$ are placed at "H", Q output doesn't change.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=2μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS279



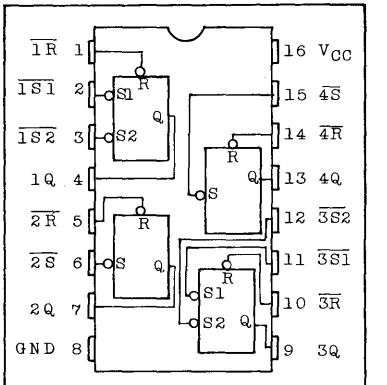
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC279P

TRUTH TABLE

INPUTS		OUTPUT
$\overline{S}$#	$\overline{R}$	Q
H	H	Q0
L	H	H
H	L	L
L	L	H

NOTE :

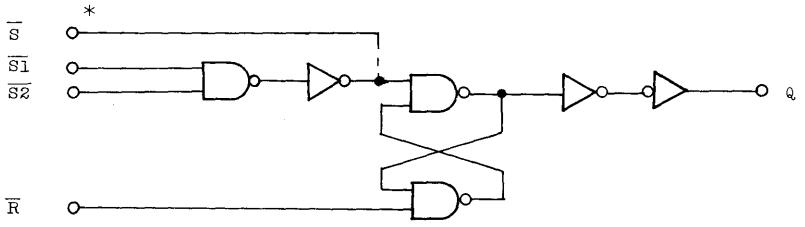
Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.

FOR LATCHES WITH DOUBLE $\overline{S}$ INPUTS:

H = BOTH $\overline{S}$ INPUTS HIGH

L = ONE OF BOTH INPUTS LOW

LOGIC DIAGRAM (Per Circuit)

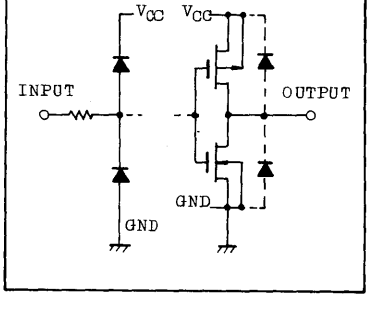


* : FOR LATCH WITH ONE $\overline{S}$ INPUT

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC279P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{S1}$, $\overline{S2}$ - Q)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{S}$ - Q)	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Delay Time ($\overline{R}$ - Q)	t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	

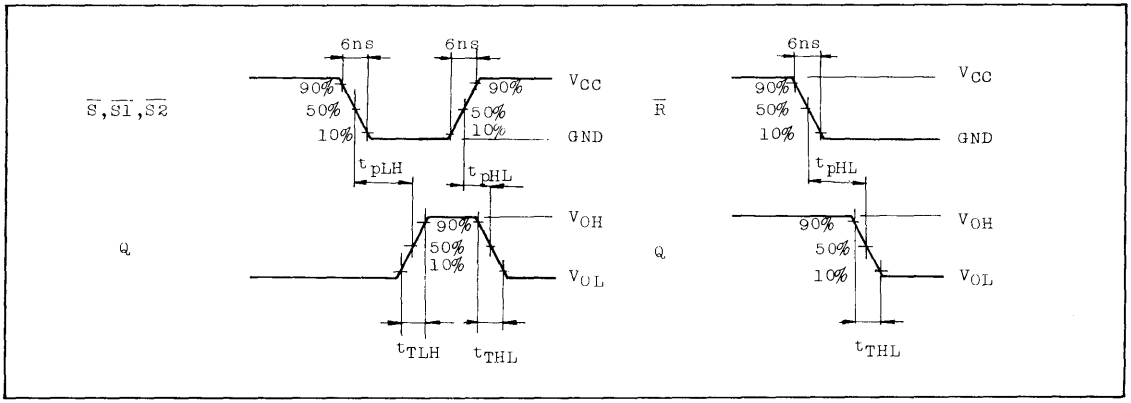
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	26	-	-	-	

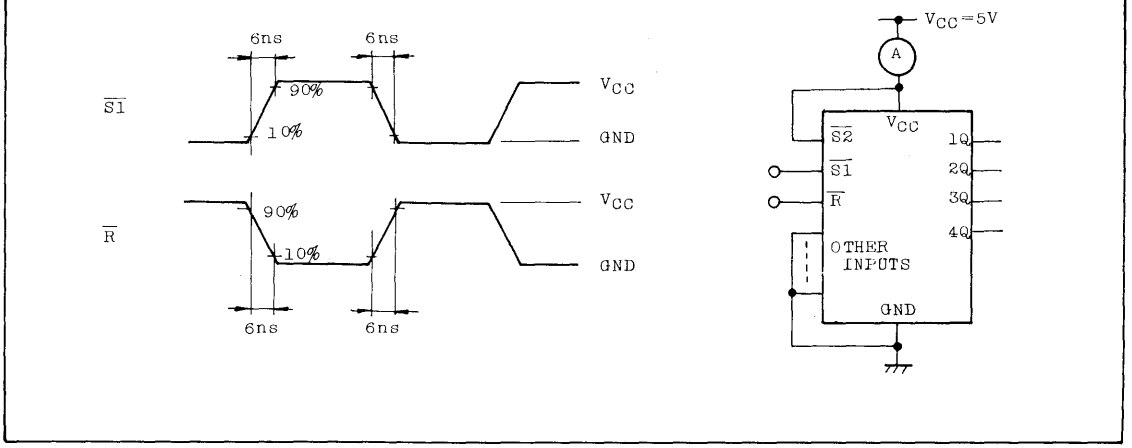
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC280P

C²MOS DIGITAL INTEGRATED CIRCUIT

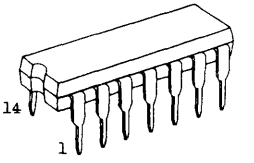
PRELIMINARY

TC74HC280P 9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

TheTC74HC280 is a high speed CMOS 9-BIT PARITY GENERATOR fabricated with silicon gate CMOS technology.
It acieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It is composed of nine data inputs (A thru I) and odd/even parity outputs (Σ ODD and Σ EVEN).
The nine input data control the output conditions.
When the number of high level inputs is odd, ΣODD output is kept high and ΣEVEN output low. On the contary, when the number is ven, ΣEVEN output is kept high and ΣODD low.
This IC facilitates operation of either odd or even aprity application.
The word-length capability is easily expanded by cascading.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

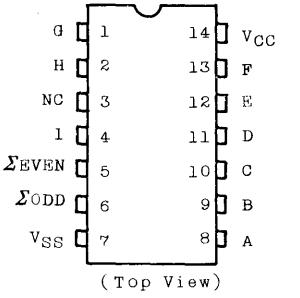
FEATURES:

- High Speed ..... t_{pd}=25ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4 μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{HIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS280



DIP14(3D14A-P)

PIN ASSIGNMENT



(Top View)

NC : No Connection

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Dicde Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

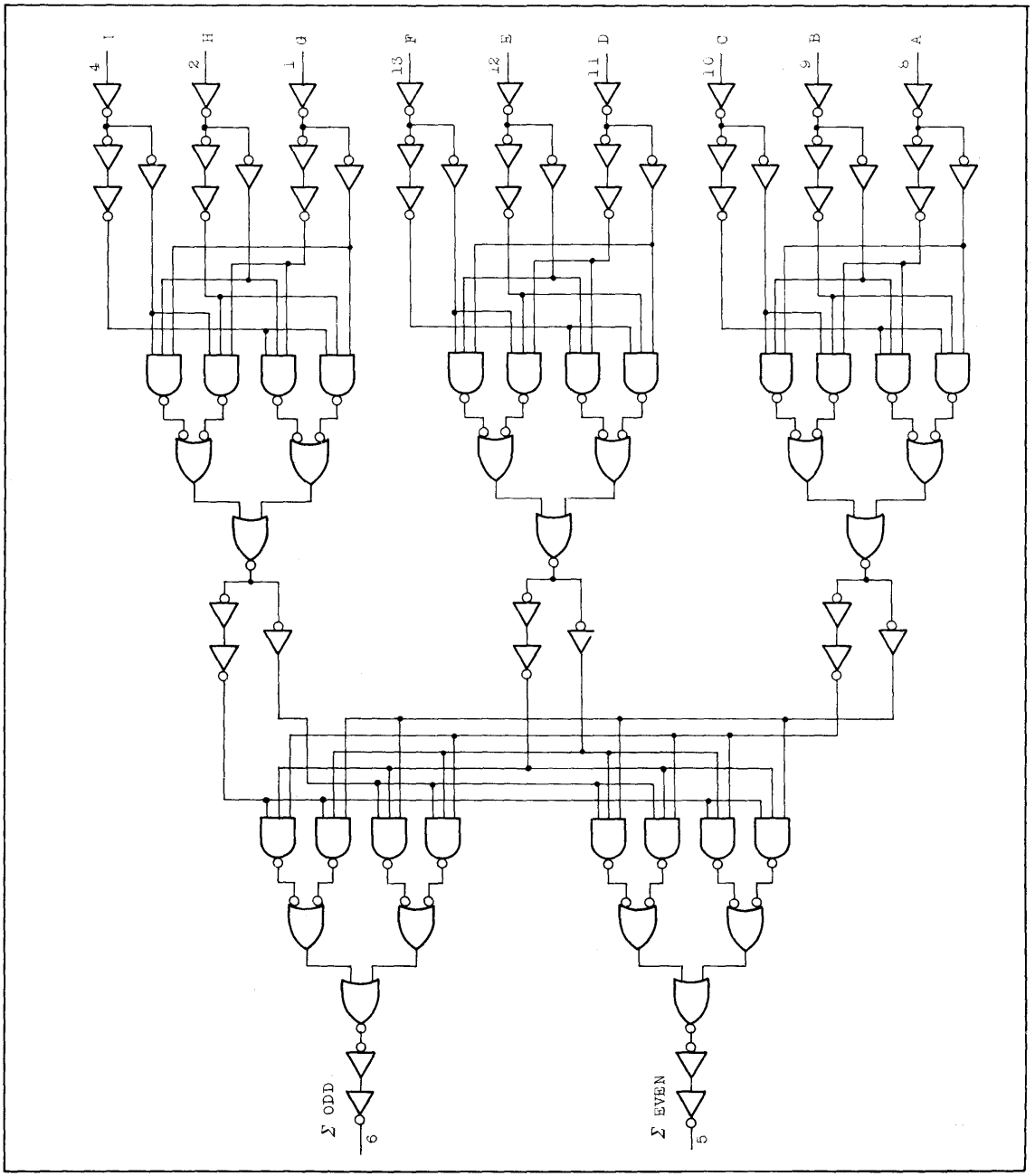
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUT	
	ΣEVEN	ΣODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

TC74HC280P

LOGIC DIAGRAM



TC74HC280P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC280P

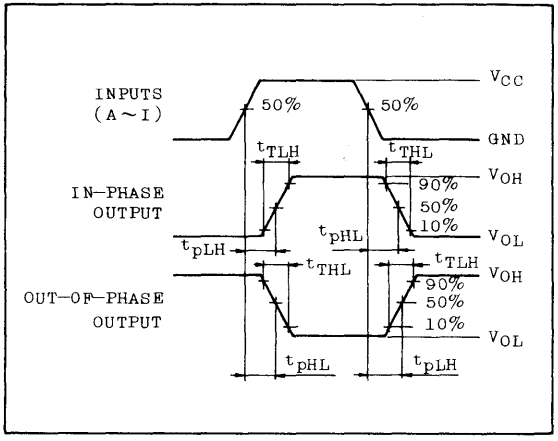
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	124	235	-	295	ns
			4.5	-	31	47	-	59	
			6.0	-	26	40	-	50	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	110	-	-	-	

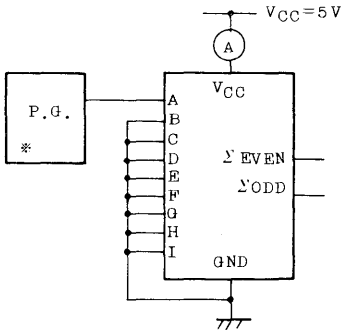
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC283P

C²MOS DIGITAL INTEGRATED CIRCUIT

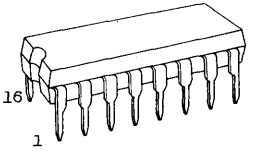
PRELIMINARY

TC74HC283P 4-BIT BINARY FULL ADDER

The TC74HC283 is a high speed CMOS 4-BIT BINARY FULL ADDER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The sum (Σ) outputs are provided for each bit and a resultant carry (C4) is obtained from the fourth bit. This adder features full internal look a head across all four bits. 4 × n bit binary adder is easily built up by cascading without any additional logic. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=30ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Ouptut Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS283



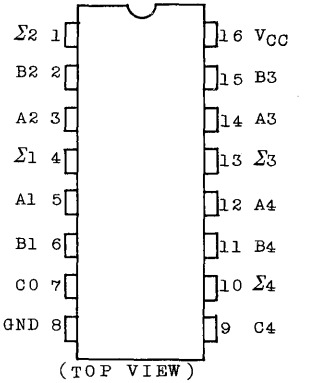
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



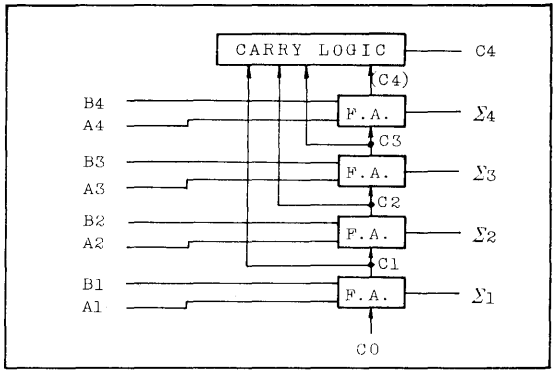
(TOP VIEW)

TC74HC283P

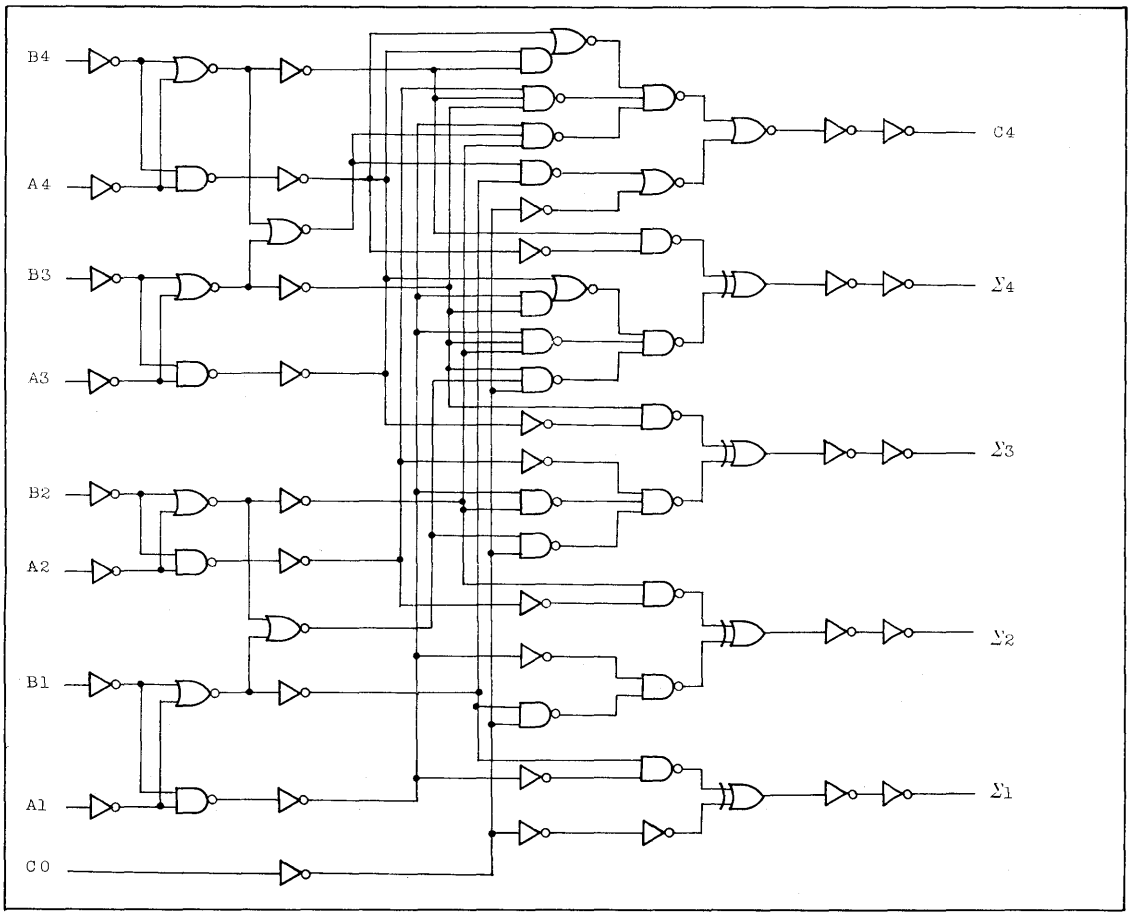
TRUTH TABLE (1 bit)

INPUTS			OUTPUTS	
Bn	An	Cn-1	Σn	Cn
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

BLOCK DIAGRAM



LOGIC DIAGRAM

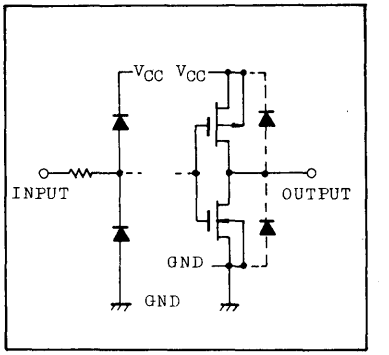


TC74HC283P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

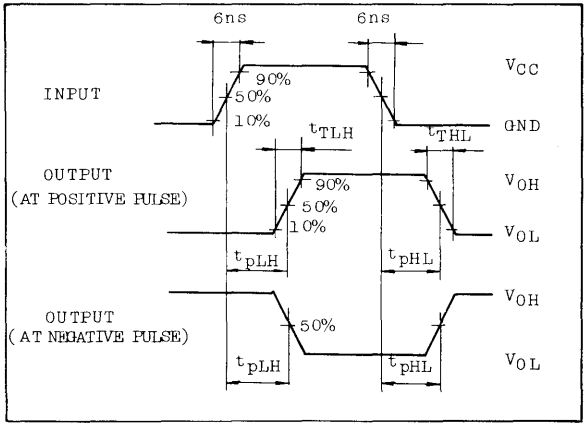
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (Co - Σn)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Propagation Delay Time (Co - C4)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay time (An, Bn - Σn)	t_{pLH} t_{pHL}		2.0	-	140	270	-	340	
			4.5	-	35	54	-	68	
			6.0	-	30	46	-	58	
Propagation Delay Time (An, Bn - C4)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	114	-	-	-	

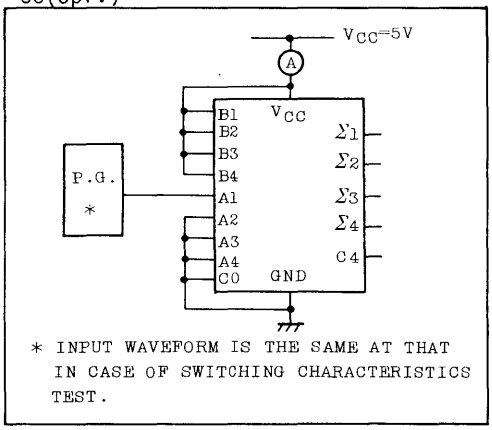
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AT THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC298P

C²MOS DIGITAL INTEGRATED CIRCUIT

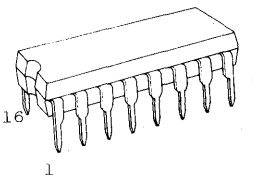
PRELIMINARY

TC74HC298P QUAD 2-CHANNEL MULTIPLEXER WITH OUTPUT REGISTER

The TC74HC298 is a high speed CMOS 2-CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contains a 4 bit 2-channel multiplexer and a 4-bit output register. When the word-select input (W.S.) is held low, word 1 (A1, B1, C1, D1) input data is selected and is applied to the registers. On the other hand W.S. is held high, word 2 (A2, B2, C2, D2) input data will be applied to the registers. This selected data is transfered to the output terminals (Q_A, Q_B, Q_C, Q_D) on the negative-going transition of the clock pulse ($\overline{CLOCK}$).
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=15ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS298



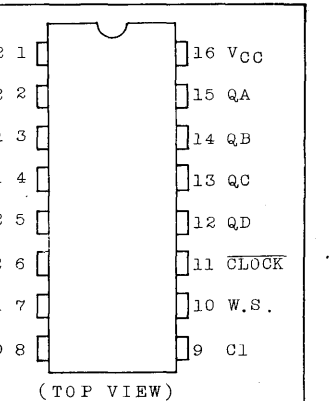
DIP16(3D16A-F)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

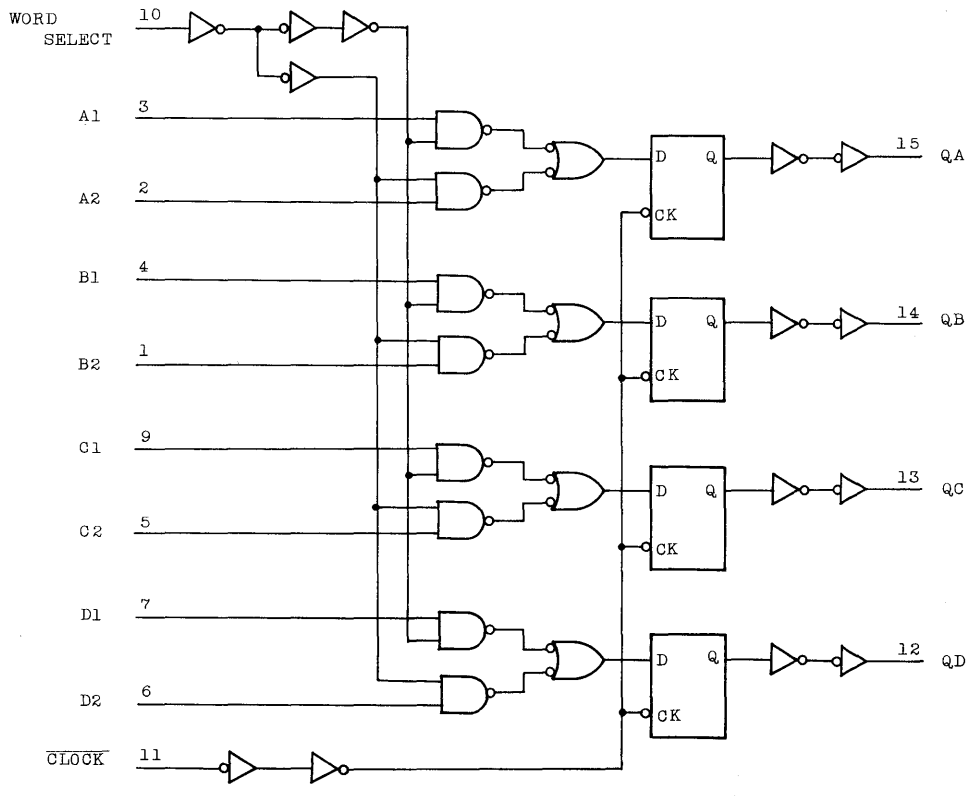
TC74HC298P

TRUTH TABLE

INPUTS		OUTPUTS			
WORD SELECT	$\overline{CLOCK}$	QA	QB	QC	QD
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	↑	QA0	QB0	QC0	QD0

X : DON'T CARE(INCLUDING TRANSITION)
a1,a2, ETC. : THE LEVEL OF STEADY-STATE INPUT AT A1,A2,ETC.
QA0,QB0,ETC. : THE LEVEL OF QA,QB,ETC. ENTERED ON THE MOST RECENT NEGATIVE TRANSITION OF THE CLOCK INPUT.

LOGIC DIAGRAM

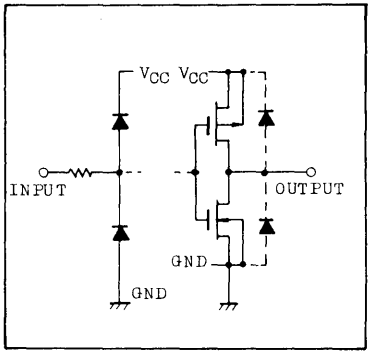


TC74HC298P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	72	140	-	175	
			4.5	-	18	28	-	35	
($\overline{CLOCK}$ - Q)	t_{pHL}		6.0	-	15	24	-	30	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
($\overline{CLOCK}$)	$t_{w(L)}$		6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
(A, B, C, D)			6.0	-	2	9	-	11	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
(W.S.)			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
(A, B, C, D, W.S.)			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	47	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

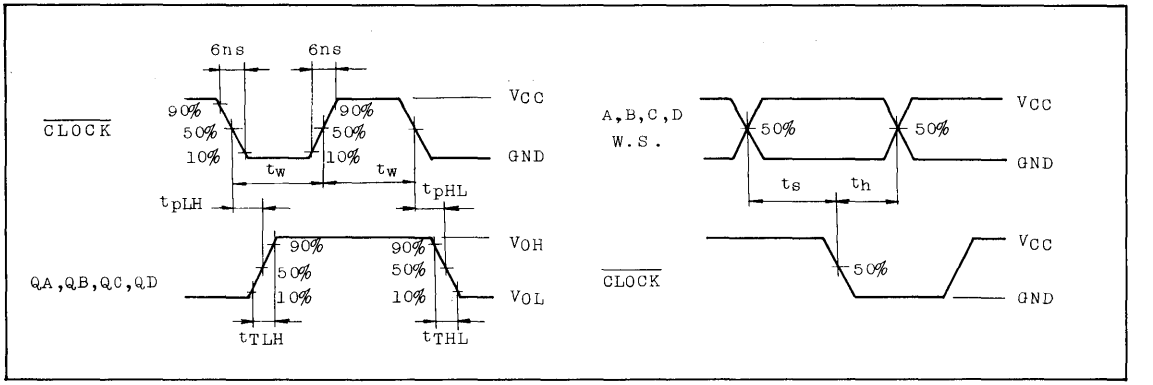
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per bit)}$$

And the C_{PD} for the operating n-bit can be obtained by the following equation.

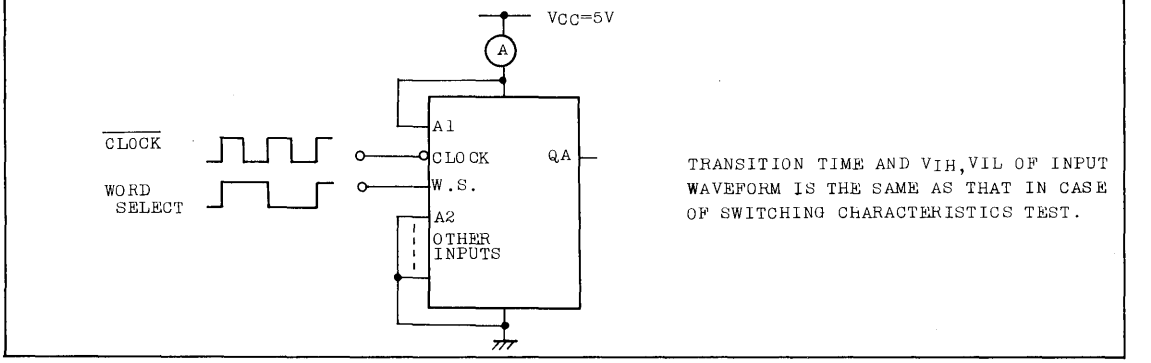
$$C_{PD} = 32 + n \cdot 15$$

TC74HC298P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



TRANSITION TIME AND V_{IH}, V_{IL} OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

CMOS DIGITAL INTEGRATED CIRCUIT

TC74HC299P

PRELIMINARY

TC74HC299P 8-BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

The TC74HC299 is a high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate C^2MOS technolgy.

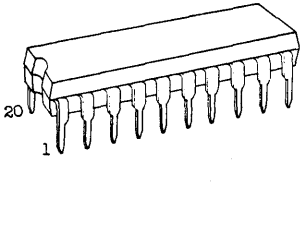
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device has four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs (S0, S1). When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected. The TC74HC323 is similar but have synchronous clear.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{max}=35MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....
  $|I_{OH}|=I_{OL}$=6mA(Min.) For QA ~ QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QA', QH'
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ~ 6V
- Pin and Function Compatible with 74LS299



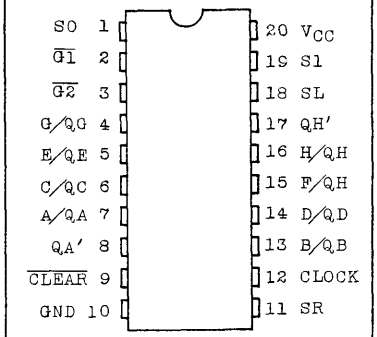
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C~65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC299P

TRUTH TABLE

MODE	INPUTS								INPUTS/OUTPUTS		OUTPUTS	
	$\overline{CLEAR}$	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$ *	$\overline{G2}$ *		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	↓	X	H	H	QGn	H	QGn
	H	L	H	L	L	↓	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	↓	H	X	QBn	H	QBn	H
	H	H	L	L	L	↓	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	↓	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential operation or clearing of the register is not affected.

Z : High Impedance

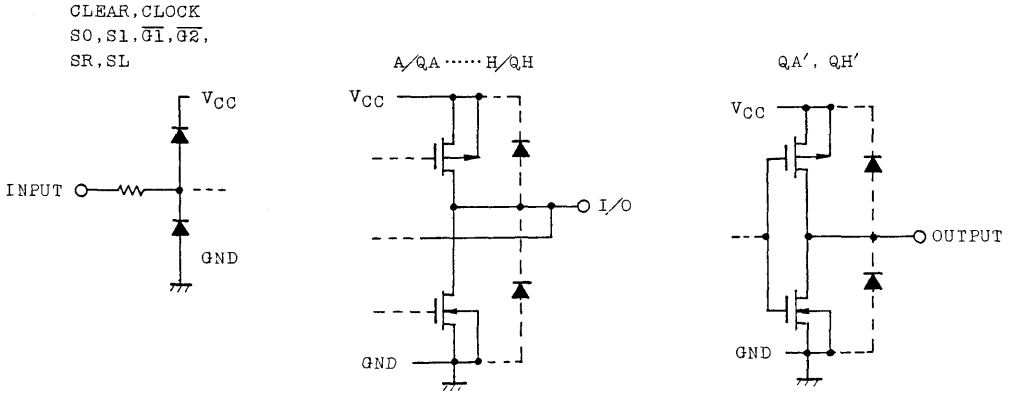
Qno: The level of An before the indicated steady-state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by ↓ or ↑.

a,h: The level of the steady-state inputs A, H, respectively.

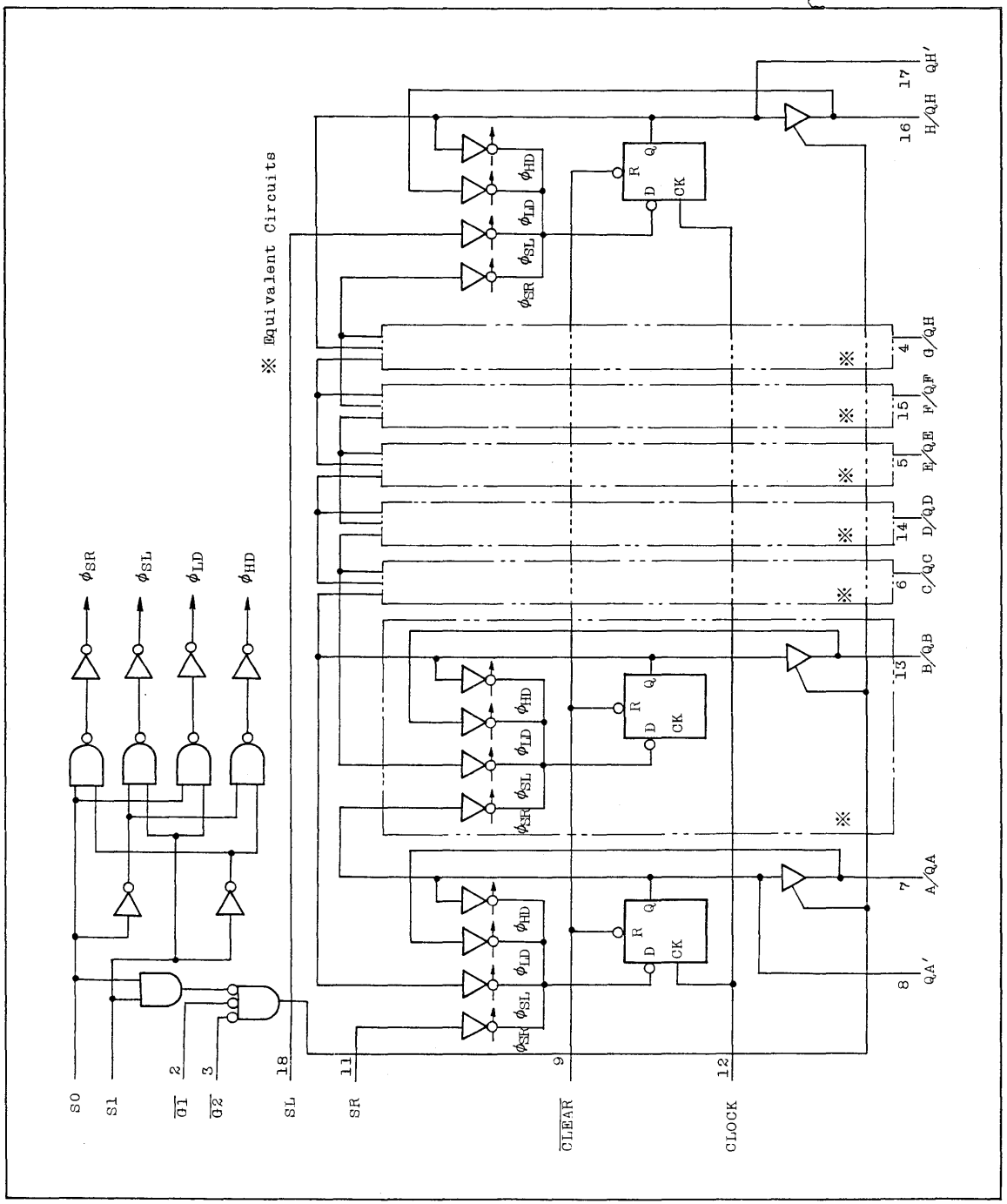
X : Don't care

INPUT and OUTPUT EQUIVALENT CIRCUIT



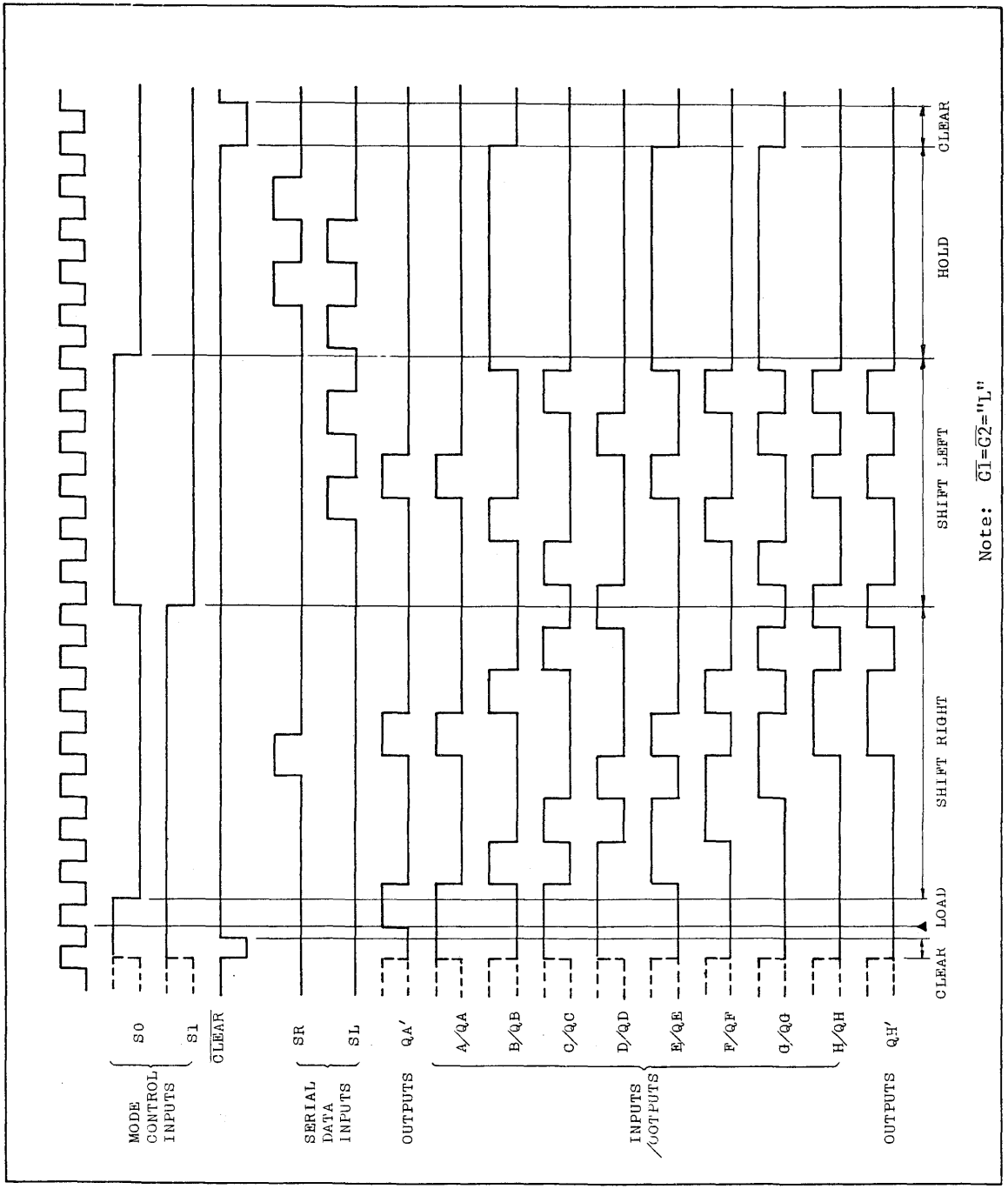
TC74HC299P

LOGIC DIAGRAM



TC74HC299P

TIMING CHART



TC74HC299P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		Q_A ∿ Q_H	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		Q_A', Q_H'	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		Q_A ∿ Q_H	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		Q_A', Q_H'	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current of Bus Terminal	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC299P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time (QA∿QH)	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Output Transition Time (QA', QH')	t_{TLH} t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - QA∿QH)	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time (CLOCK - QA', QH')	t_{pLH} t_{pHL}		2.0	-	120	235	-	295	
			4.5	-	30	47	-	59	
			6.0	-	26	40	-	50	
Propagation Delay Time ($\overline{CLEAR}$ - QA∿QH)	t_{pHL}		2.0	-	116	230	-	290	
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Propagation Delay Time ($\overline{CLEAR}$ - QA', QH')	t_{pHL}		2.0	-	116	230	-	290	
			4.5	-	29	46	-	58	
			6.0	-	25	39	-	49	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	33	-	16	-	
			6.0	24	39	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$)	$t_{w(L)}$		2.0	-	50	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Minimum Set-up Time (SL, SR, A∿H)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set-up Time (S0, S1)	t_s		2.0	-	50	125	-	160	
			4.5	-	13	25	-	32	
			6.0	-	11	21	-	27	
Minimum Hold Time (SL, SR, A∿H)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	

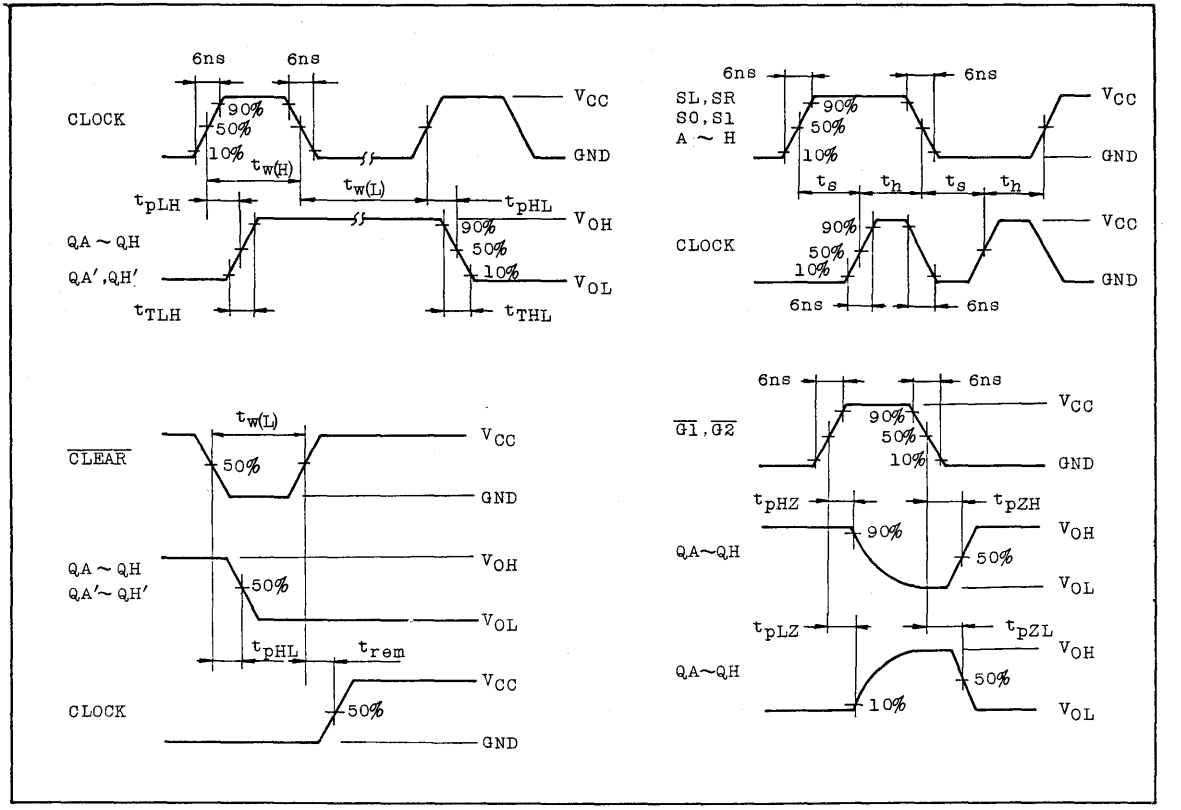
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Hold Time (S0, S1)	t_h		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLEAR}$)	t_{rem}		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	112	200	-	250	
			4.5	-	28	40	-	50	
			6.0	-	24	34	-	43	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance (QA∿QH)	C_{OUT}			-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	221	-	-	-	

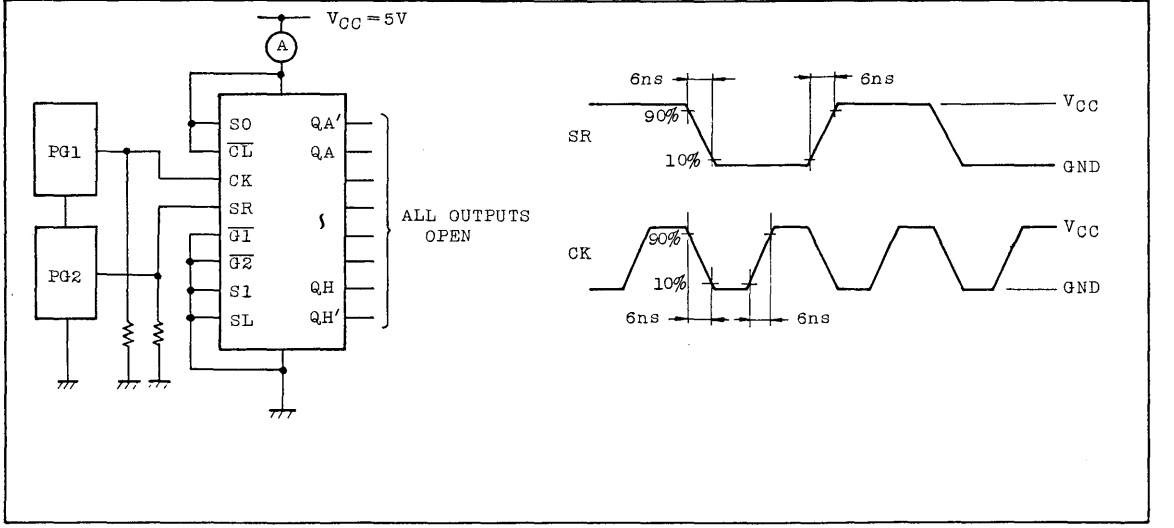
Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC}(Opr.)=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74NC299P



$I_{CC(Opr.)}$ TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC354P

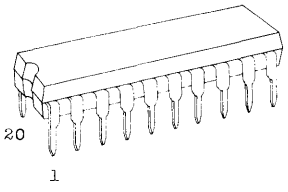
PRELIMINARY

TC74HC354P 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

The TC74HC354 is a high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit latch at the negative pulse on $\overline{DC}$ input. The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC354 is similar in function to TC74HC356, which has a 8-bit flip-flop as the data registers instead of 8-bit latch. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=33ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS354



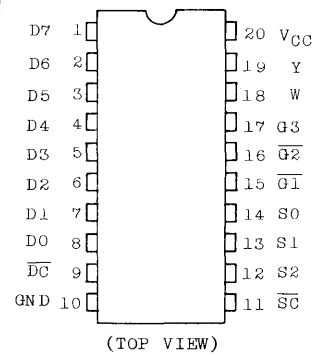
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC354P

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	$\overline{DC}$	G1	G2	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	$\overline{D0}$	D0
L	L	L	H	L	L	H	$\overline{D0n}$	D0n
L	L	H	L	L	L	H	$\overline{D1}$	D1
L	L	H	H	L	L	H	$\overline{D1n}$	D1n
L	H	L	L	L	L	H	$\overline{D2}$	D2
L	H	L	H	L	L	H	$\overline{D2n}$	D2n
L	H	H	L	L	L	H	$\overline{D3}$	D3
L	H	H	H	L	L	H	$\overline{D3n}$	D3n
H	L	L	L	L	L	H	$\overline{D4}$	D4
H	L	L	H	L	L	H	$\overline{D4n}$	D4n
H	L	H	L	L	L	H	$\overline{D5}$	D5
H	L	H	H	L	L	H	$\overline{D5n}$	D5n
H	H	L	L	L	L	H	$\overline{D6}$	D6
H	H	L	H	L	L	H	$\overline{D6n}$	D6n
H	H	H	L	L	L	H	$\overline{D7}$	D7
H	H	H	H	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z : HIGH IMPEDANCE

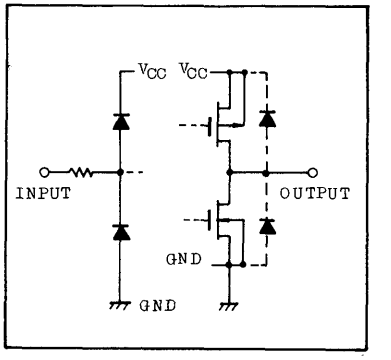
D0n·····D7n : THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7 ,RESPECTIVELY, BEFORE THE MOST RECENT LOW-TO-HIGH TRANSITION OF DATA CONTROL.

: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH $\overline{SC}$ LOW.

RECOMMENDED OPERATING CONDITIONS

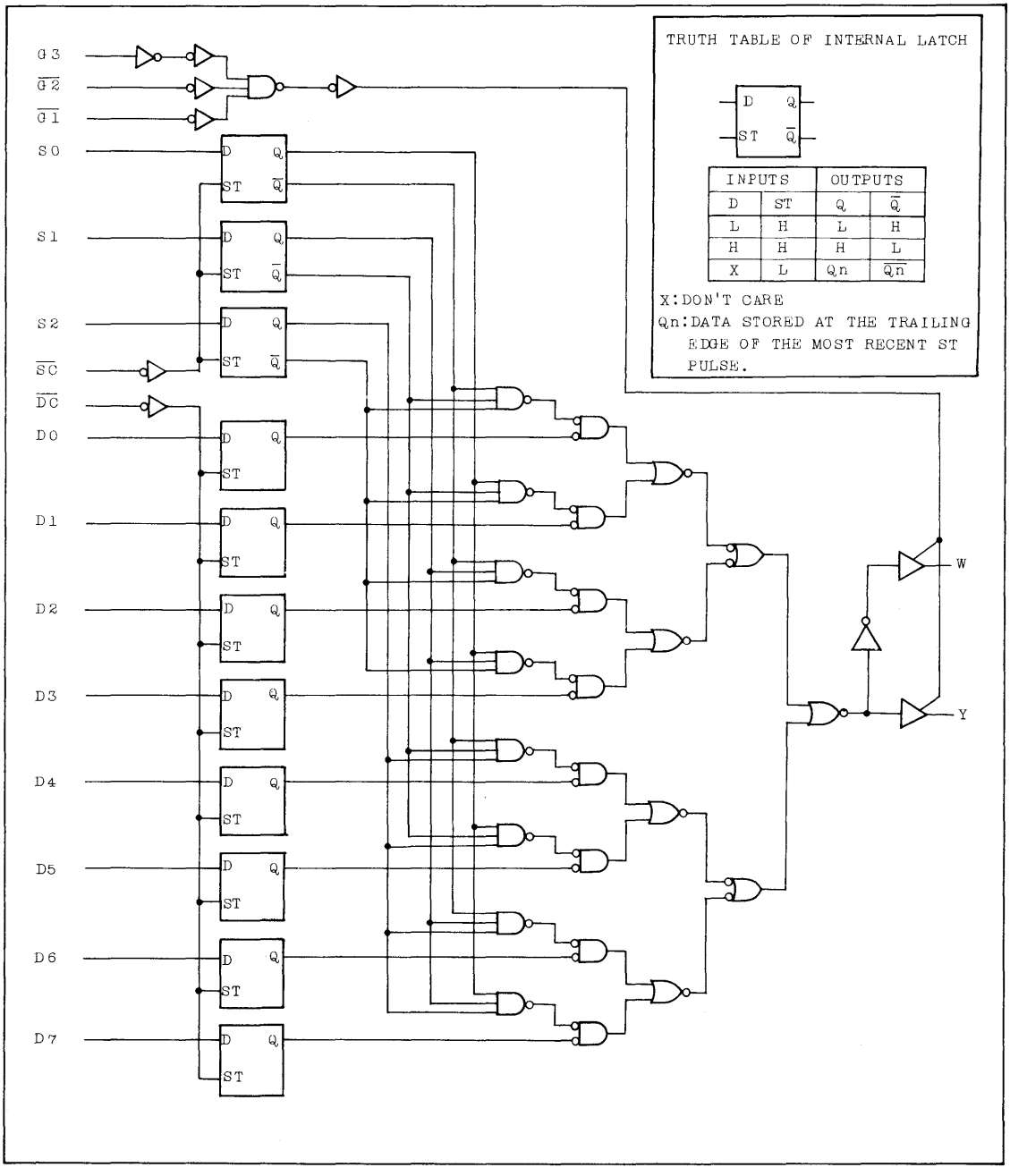
PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC354P

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X: DON'T CARE

Qn: DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TC74HC354P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (Dn - Y, W)	t_{pLH}		2.0	-	136	260	-	325	
	t_{pHL}		4.5	-	34	52	-	65	
			6.0	-	29	44	-	55	
Propagation Delay Time ($\overline{DC}$ - Y, W)	t_{pLH}		2.0	-	136	265	-	330	
	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	

AC ELECTRICAL CHARACTERISTICS (Continued)

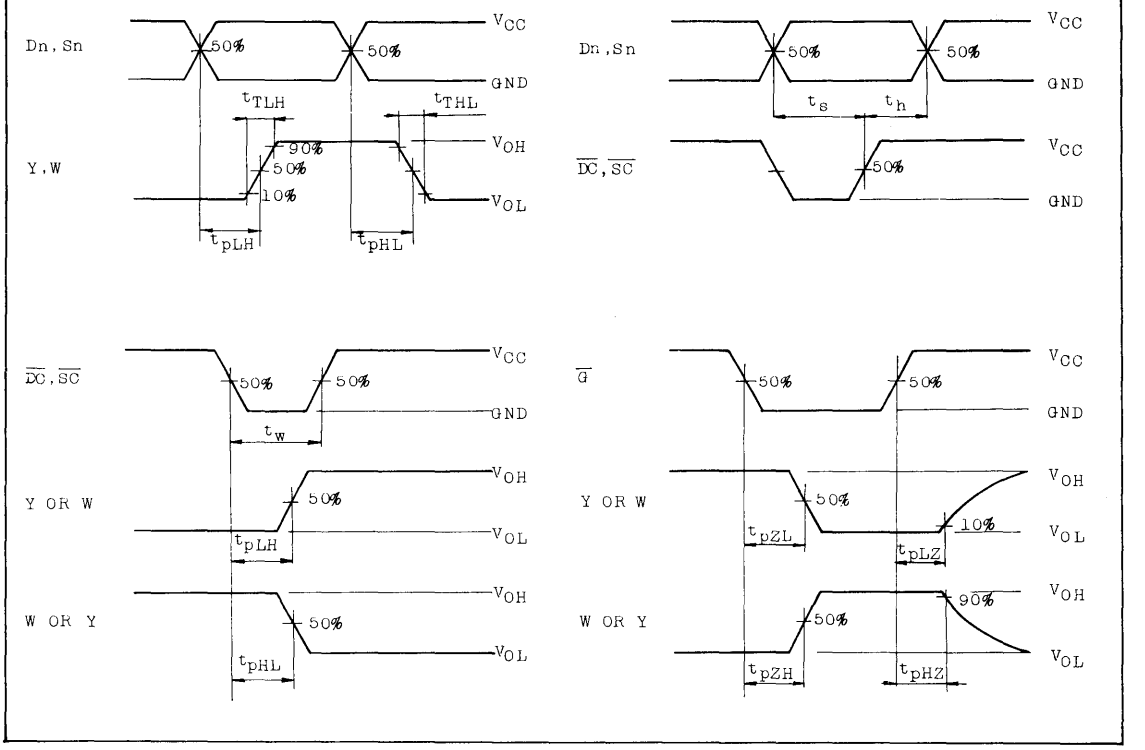
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Sn - Y, W)	t_{pLH} t_{pHL}		2.0	-	152	285	-	355	nS
			4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	156	295	-	370	
			4.5	-	39	59	-	74	
			6.0	-	33	50	-	63	
Minimum Pulse Width ($\overline{DC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	84	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

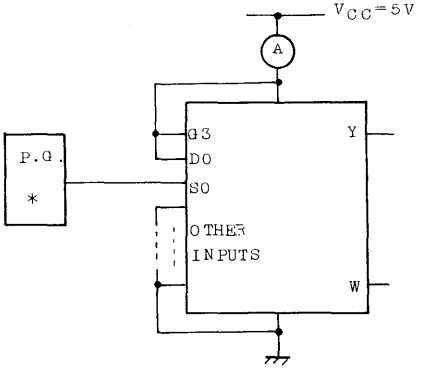
$$I_{CC(opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC354P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC356P

PRELIMINARY

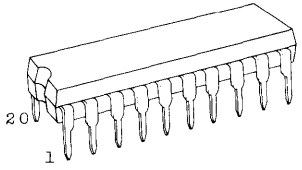
TC74HC356P 8-CHANNEL MULTIPLEXER WITH INPUT REGISTER

GENERAL DESCRIPTION

The TC74HC356 is high speed CMOS 8-CHANNEL MULTIPLEXER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device contains 8 channel digital multiplexer with a 8-bit input data register and a 3-bit address input register and with 3-state outputs. The one of eight input data will be provided on the Y output pin (non-inverted output) and W output pin (inverted output) determined by the address data. The information at the data inputs (D0 thru D7) is stored in the 8-bit flip-flop at the positive going edge of clock input (CLOCK). The information at the address inputs (S0 thru S2) is stored in the 3-bit latch at the negative pulse on $\overline{SC}$ input. These outputs are disabled to be high-impedance when $\overline{G1}$ input is held high, $\overline{G2}$ input is held high or G3 input is held low. This device is suitable for interfacing with bus lines in a bus organized system. The TC74HC356 is similar in function to TC74HC354, which has a 8-bit latch as the data register instead of 8-bit flip-flop. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=29ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Ouptut Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS356



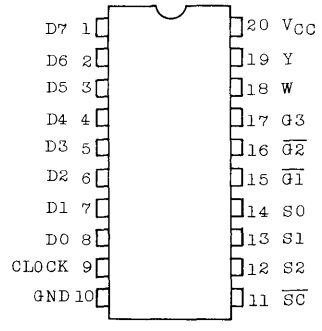
DIP20(3D20A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC356P

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT #				OUTPUT ENABLES				
S2	S1	S0	CLOCK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↓	L	L	H	$\overline{D0}$	D0
L	L	L	↑	L	L	H	$\overline{D0n}$	D0n
L	L	H	↓	L	L	H	$\overline{D1}$	D1
L	L	H	↑	L	L	H	$\overline{D1n}$	D1n
L	H	L	↓	L	L	H	$\overline{D2}$	D2
L	H	L	↑	L	L	H	$\overline{D2n}$	D2n
L	H	H	↓	L	L	H	$\overline{D3}$	D3
L	H	H	↑	L	L	H	$\overline{D3n}$	D3n
H	L	L	↓	L	L	H	$\overline{D4}$	D4
H	L	L	↑	L	L	H	$\overline{D4n}$	D4n
H	L	H	↓	L	L	H	$\overline{D5}$	D5
H	L	H	↑	L	L	H	$\overline{D5n}$	D5n
H	H	L	↓	L	L	H	$\overline{D6}$	D6
H	H	L	↑	L	L	H	$\overline{D6n}$	D6n
H	H	H	↓	L	L	H	$\overline{D7}$	D7
H	H	H	↑	L	L	H	$\overline{D7n}$	D7n

X : DON'T CARE

Z: HIGH IMPEDANCE

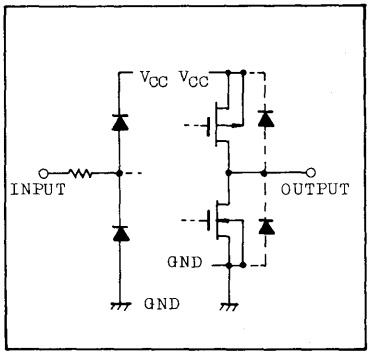
D0 ····· D7: THE LEVEL OF STEADY-STATE INPUTS AT INPUT D0 THROUGH D7, RESPECTIVELY, AT THE TIME OF THE LOW-TO-HIGH TRANSITION OF CLOCK.

#: THIS COLUMN SHOWS THE INPUT ADDRESS SETUP WITH SC LOW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



74HC356P

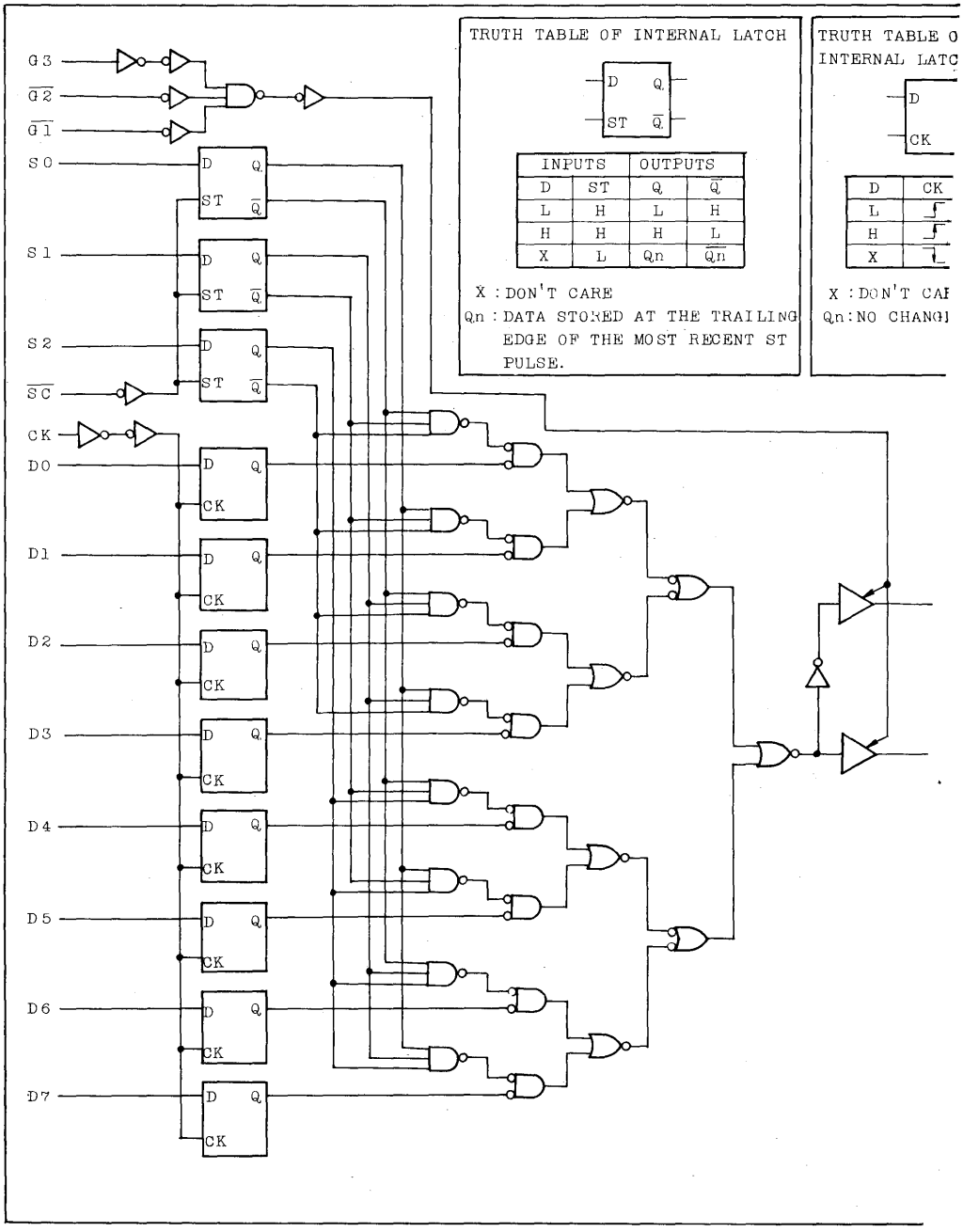
ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
gh-Level put Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
w-Level put Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
gh-Level tput Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
w-Level put Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
State Output -State rent	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
ut Leakage rent	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
escent ply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
tput Transition Time	t_{TLH}		2.0	-	25	60	-	75	
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
pagation Delay Time	t_{pLH}		2.0	-	136	265	-	330	
(CLOCK - Y, W)	t_{pHL}		4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
pagation Delay Time	t_{pLH}		2.0	-	152	285	-	355	
(Sn - Y, W)	t_{pHL}		4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE
Qn : DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE O
INTERNAL LATC

D	CK
L	↓
H	↓
X	↑

X : DON'T CAI
Qn : NO CHANGI

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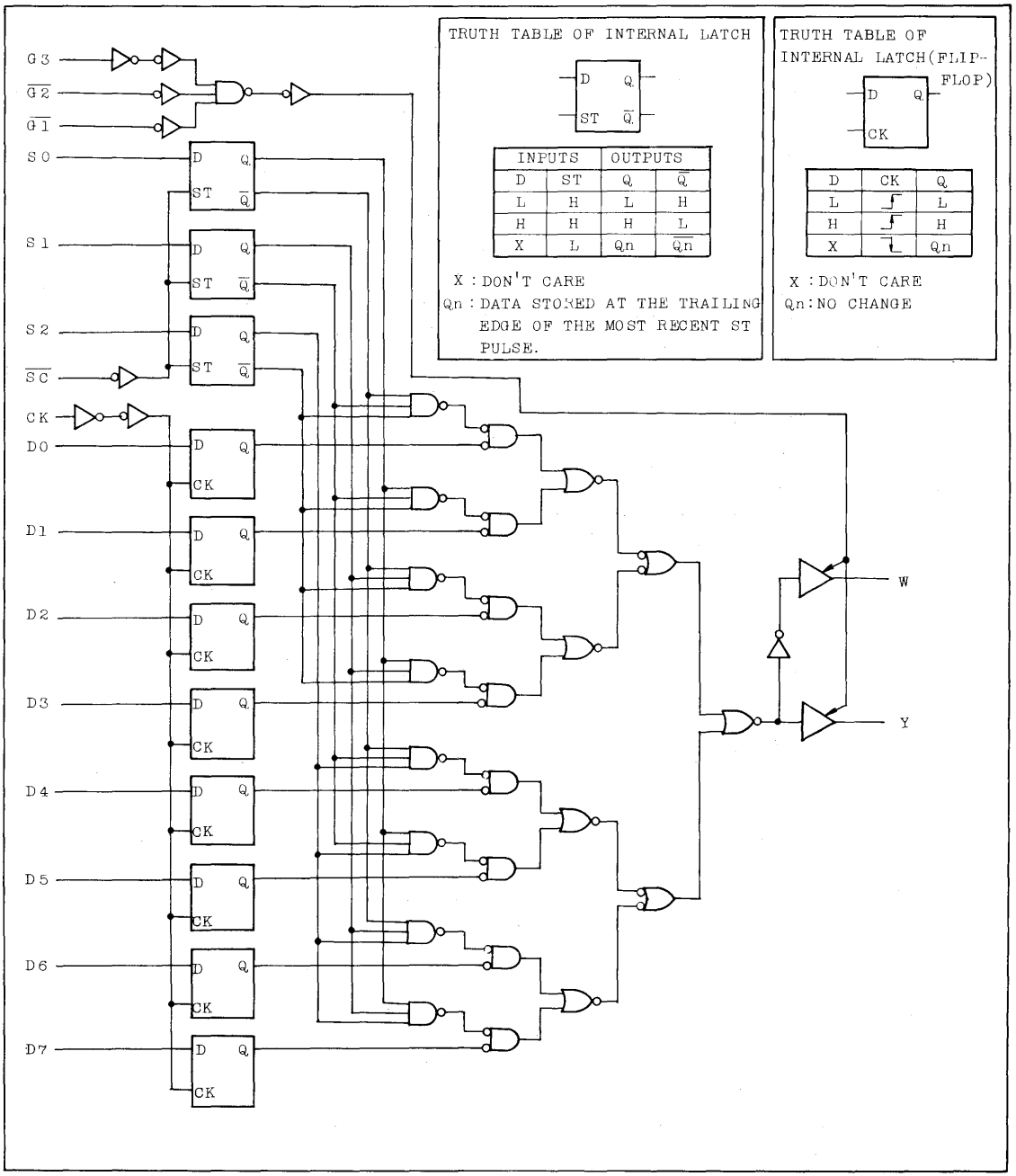
TC74HC356P

LOGIC DIAGRAM



TRUTH TABLE OF INTERNAL LATCH

INPUTS		OUTPUTS	
D	ST	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Qn	$\overline{Qn}$

X : DON'T CARE
Qn : DATA STORED AT THE TRAILING EDGE OF THE MOST RECENT ST PULSE.

TRUTH TABLE OF INTERNAL LATCH(FLIP-FLOP)

D	CK	Q
L	↓	L
H	↓	H
X	↑	Qn

X : DON'T CARE
Qn : NO CHANGE

TC74HC356P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Ouptut Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time (CLOCK - Y, W)	t_{pLH} t_{pHL}		2.0	-	136	265	-	330	
			4.5	-	34	53	-	66	
			6.0	-	29	45	-	56	
Propagation Delay Time (Sn - Y, W)	t_{pLH} t_{pHL}		2.0	-	152	285	-	355	
			4.5	-	38	57	-	71	
			6.0	-	32	48	-	60	

AC ELECTRICAL CHARACTERISTICS (Continued)

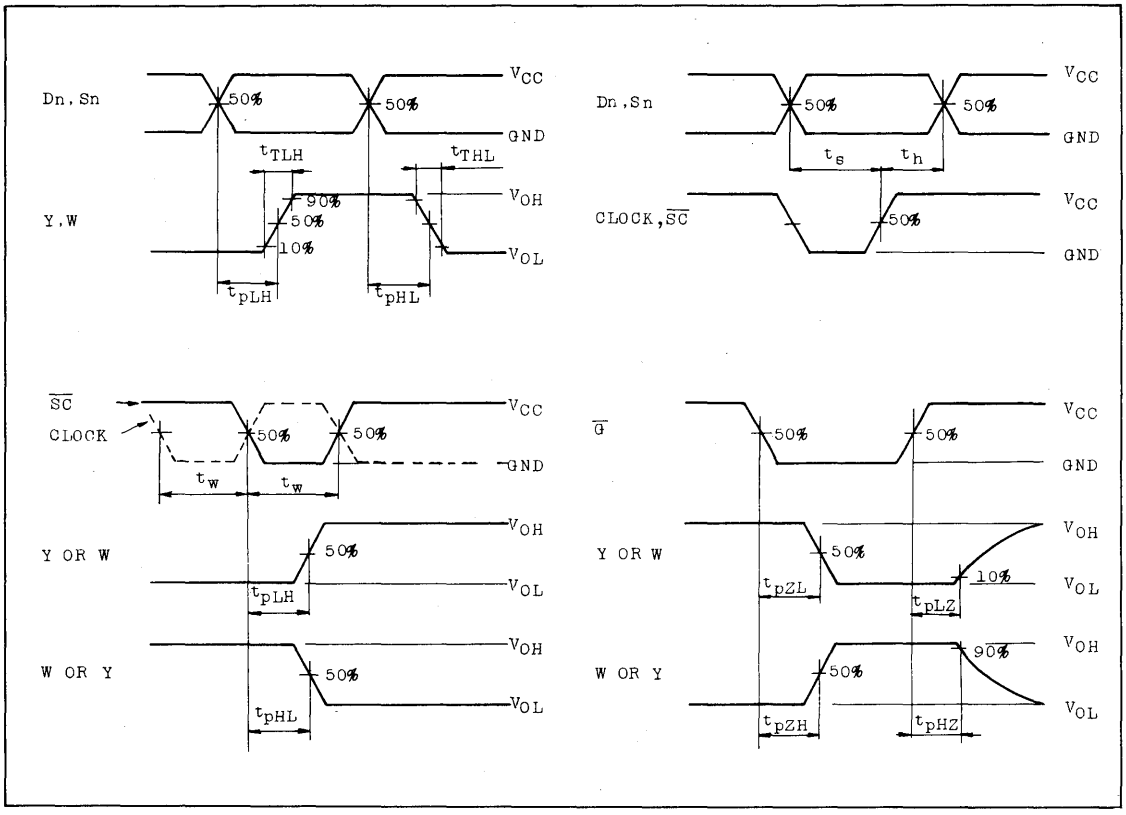
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{SC}$ - Y, W)	t_{pLH} t_{pHL}		2.0	-	156	295	-	370	ns
			4.5	-	39	59	-	74	
			6.0	-	33	50	-	63	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SC}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Sn)	t_s		2.0	-	10	75	-	95	
			4.5	-	2	15	-	19	
			6.0	-	2	13	-	16	
Minimum Set-up Time (Dn)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (Sn)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Hold Time (Dn)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	64	125	-	155	
			4.5	-	16	25	-	31	
			6.0	-	14	21	-	26	
Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	88	155	-	195	
			4.5	-	22	31	-	39	
			6.0	-	19	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	53	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

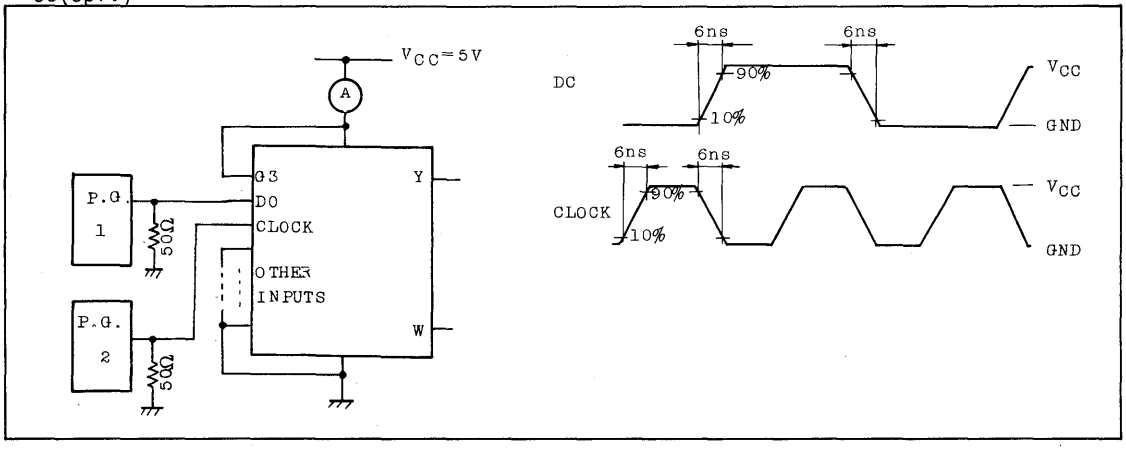
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC356P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT, WAVEFORM



TC74HC365P/F
TC74HC366P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

HEX BUS BUFFER
TC74HC365P/F NON-INVERTING
TC74HC366P/F INVERTING

The TC74HC365 and TC74HC366 are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.

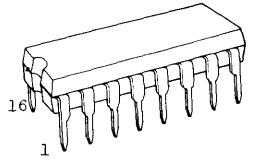
These devices achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. All six buffers are controlled by the combination of two enable inputs ($\overline{G1}$ and $\overline{G2}$); all outputs of these buffers are enabled only when both $\overline{G1}$ and $\overline{G2}$ inputs are held low, and at the other conditions these output are disabled to be high-impedance.

These outputs are capable of driving up to 15 LSTTL. The designer has a choice of non-inverting outputs (HC365) and inverting outputs (HC366).

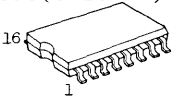
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS365/366



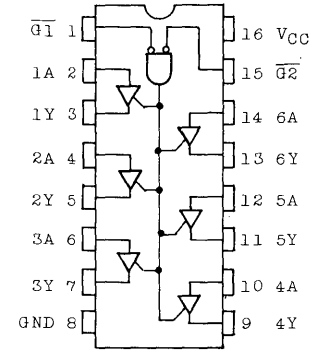
DIP16(3D16A-P)



MFP16(F16GC-P)

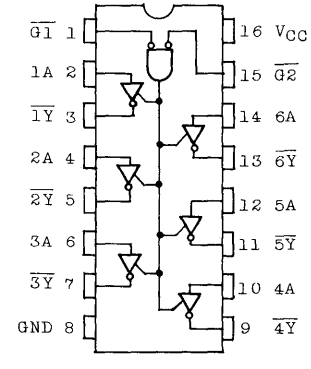
PIN ASSIGNMENT

TC74HC365



(TOP VIEW)

TC74HC366



(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn(365)	$\overline{Yn}$(366)
L	L	L	L	H
L	L	H	H	L
H	X	X	Z	Z
X	H	X	Z	Z

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC365P/F
TC74HC366P/F

ABSOLUTE MAXIMUM RATINGS

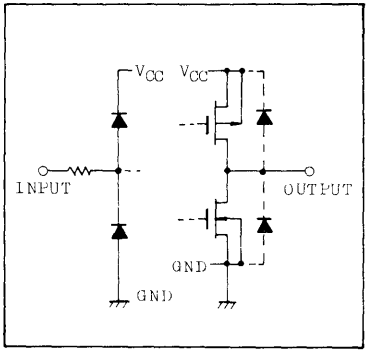
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC}/Ground Current	I_{CC}	± 70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=-40∿85°C MIN.	MAX.	UNIT
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC365P/F
TC74HC366P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time **	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	96	175	-	220	
			4.5	-	24	35	-	44	
			6.0	-	20	30	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

TC74HC365P/F
TC74HC366P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

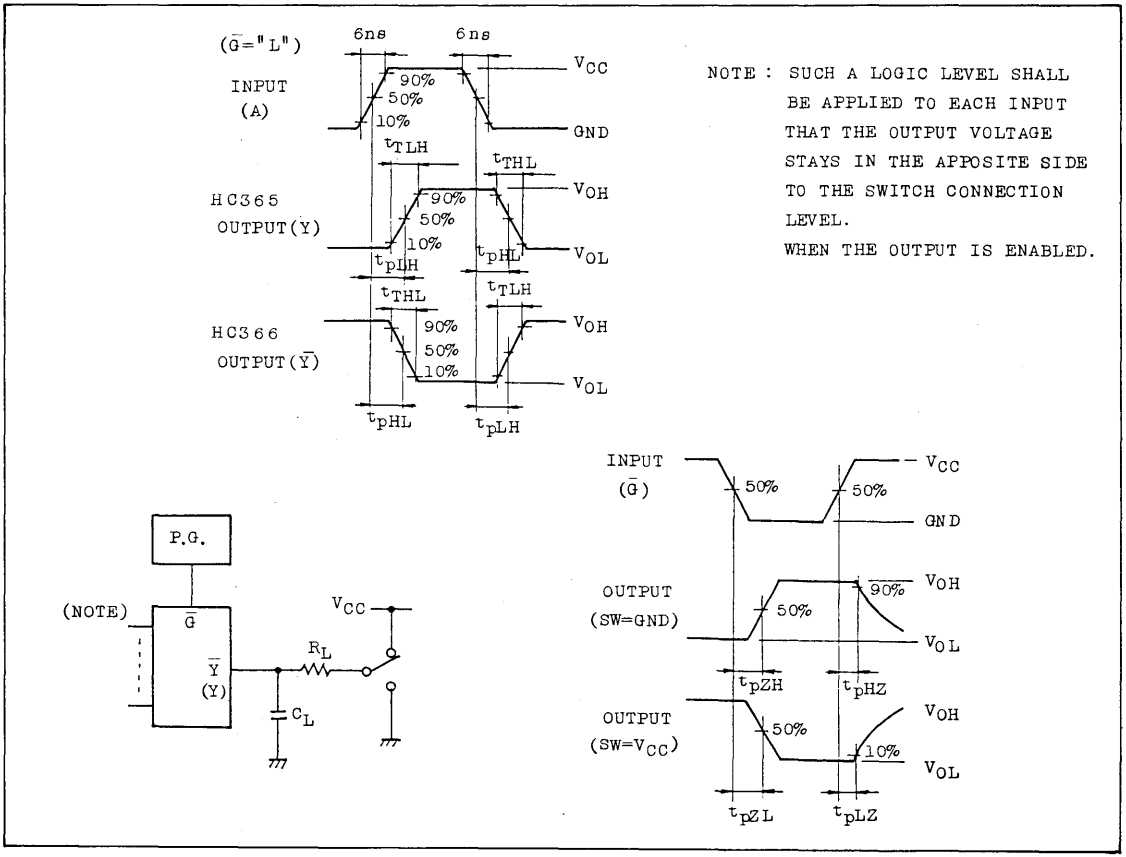
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC365		-	33	-	-	-	pF
		TC74HC366		-	31	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per Circuit)}$$

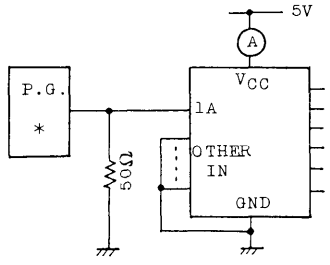
(2) * : for TC74HC365 only.
**: for TC74HC366 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC365P/F
TC74HC366P/F

$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

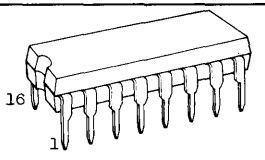
TC74HC367P/F
TC74HC368P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

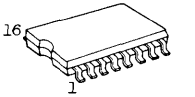
PRELIMINARY

HEX BUS BUFFER
TC74HC367P/F NON-INVERTING
TC74HC368P/F INVERTING

The TC74HC367 and TC74HC368 are high speed CMOS 3-STATE BUS BUFFERs fabricated with silicon gate C^2MOS technology.
These devices achieve the high speed operation similar to equivalent LSTTL, while maintaining the CMOS low power dissipation. These devices contain six buffers, and four buffers are controlled by a enable input ($\overline{G1}$) and the other two buffers are controlled by the other enable input ($\overline{G2}$); these outputs of each buffer group are enabled when $\overline{G1}$ and/or $\overline{G2}$ inputs are held low, and when held high these outputs are disabled to be high-impedance.
These outputs are capable of driving up to 15 LSTTL.
The designer has a choice of non-inverting outputs (HC367) and inverting outputs (HC368).
All outputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)



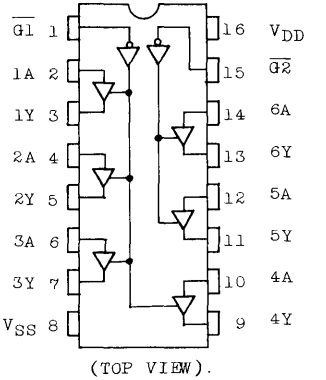
MFP16(F16QC-P)

FEATURES:

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$= 6 mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS367/368

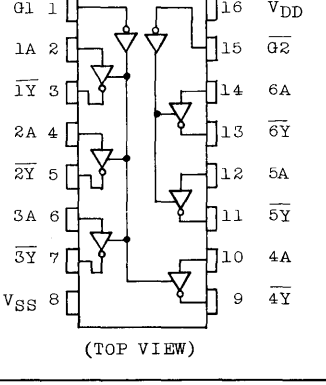
PIN ASSIGNMENT

TC74HC367



(TOP VIEW)

TC74HC368



(TOP VIEW)

TRUTH TABLE

INPUTS		OUTPUTS	
$\overline{G}$	An	Yn(367)	$\overline{Yn}$(368)
L	L	L	H
L	H	H	L
H	X	Z	Z

X : DON'T CARE
Z : HIGH IMPEDANCE

TC74HC367P/F
TC74HC368P/F

ABSOLUTE MAXIMUM RATINGS

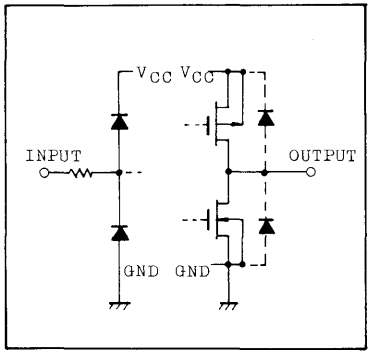
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC367P/F
TC74HC368P/F

DC ELECTRICAL CHARACTERISITCS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time *	t_{pLH}		2.0	-	60	120	-	150	
	t_{pHL}		4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time **	t_{pLH}		2.0	-	56	115	-	145	
	t_{pHL}		4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Enable Time	t_{pZL}	R_L=1kΩ	2.0	-	60	120	-	150	
	t_{pZH}		4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Output Disable Time	t_{pLZ}	R_L=1kΩ	2.0	-	80	150	-	190	
	t_{pHZ}		4.5	-	20	30	-	38	
			6.0	-	17	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	

TC74HC367P/F
TC74HC368P/F

AC ELECTRICAL CHACTERISTICS (Continued)

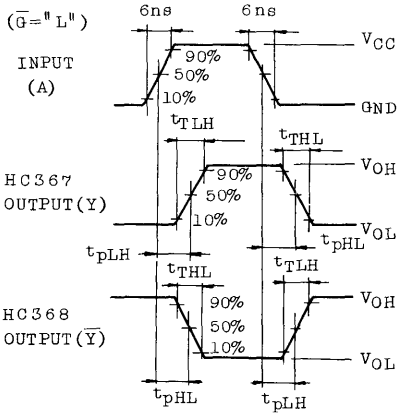
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Power Dissipation Capacitance	C_{PD}(1)	TC74HC367		-	32	-	-	-	pF
		TC74HC368		-	29	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

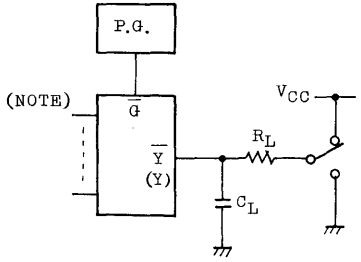
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(Per Circuit)}$$

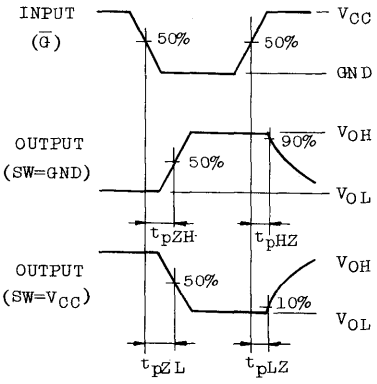
(2) *: for TC74HC367 only.
**: for TC74HC368 only.

SWITCHING CHARACTERISTICS TEST WAVEFORM



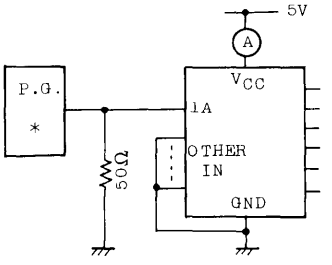
NOTE : SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL, WHEN THE OUTPUT IS ENABLED.





TC74HC367P/F
TC74HC368P/F

$I_{CC(opr)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C_{PD} CALCULATION

C_{PD} is to be calculated with the for mula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

PRELIMINARY

OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

TC74HC373P/F NON-INVERTING
TC74HC533P/F INVERTING
TC74HC563P/F INVERTING
TC74HC573P/F NON-INVERTING

The TC74HC373, TC74HC533, TC74HC563 and TC74HC573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type latches are controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.

The application designer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

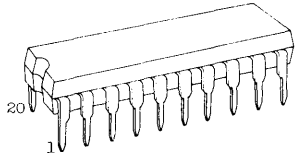
The TC74HC373 and the TC74HC573, the TC74HC533 and The TC74HC563 have the same function and the same characteristics respectively, but have the different pin layouts.

The three-state output configuration and the wide choice of outline will make the bus-organized system simple.

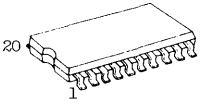
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=15ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance...$|I_{OH}|$=I_{OL}=6mA
- Balanced Propagation Delays....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range...$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS373/533/563/573



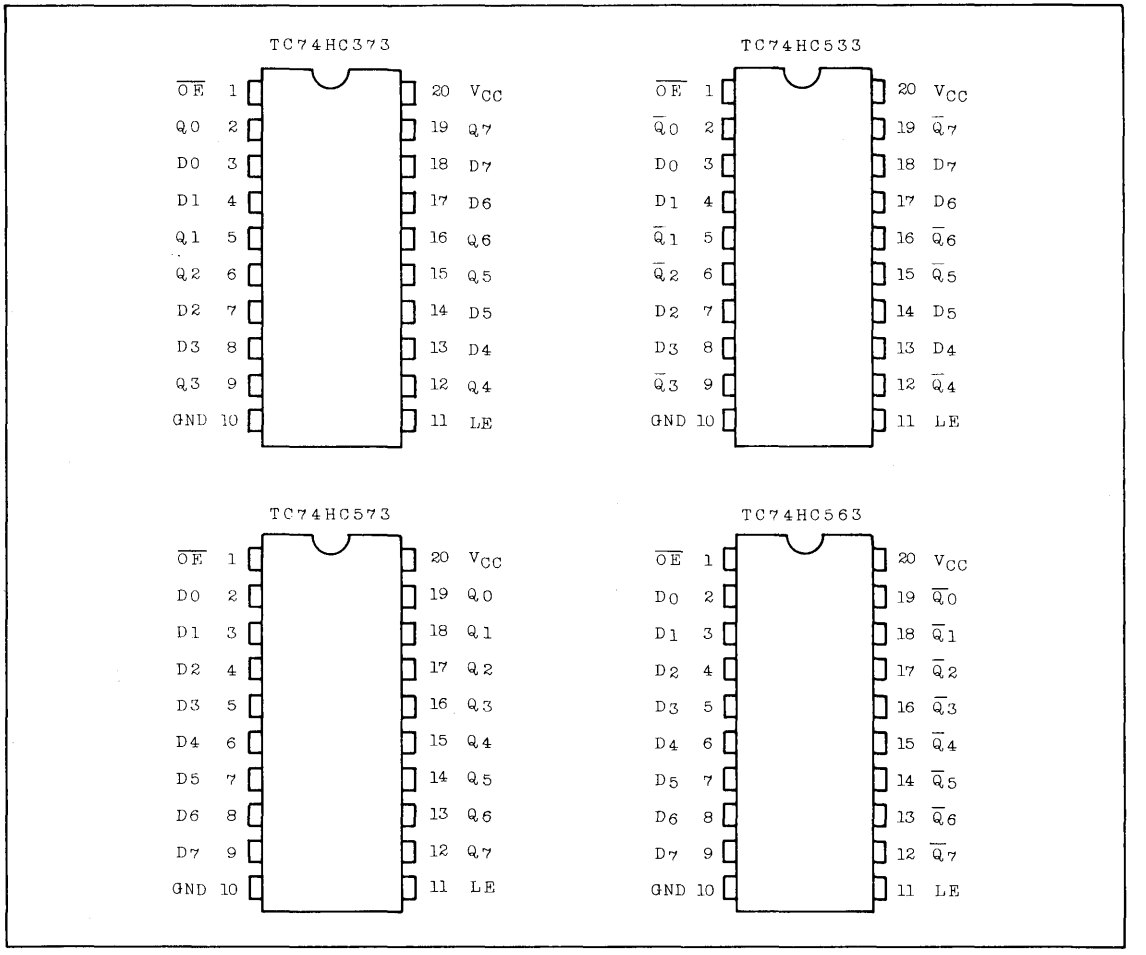
DIP20(3D20A-P)



MFP20(F20GA-P)

TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

PIN ASSIGNMENT (TOP VIEW)



TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q (HC373,HC573)	$\overline{Q}$ (HC533,HC563)
H	X	X	Z	Z
L	L	X	No change	No change
L	H	L	L	H
L	H	H	H	L

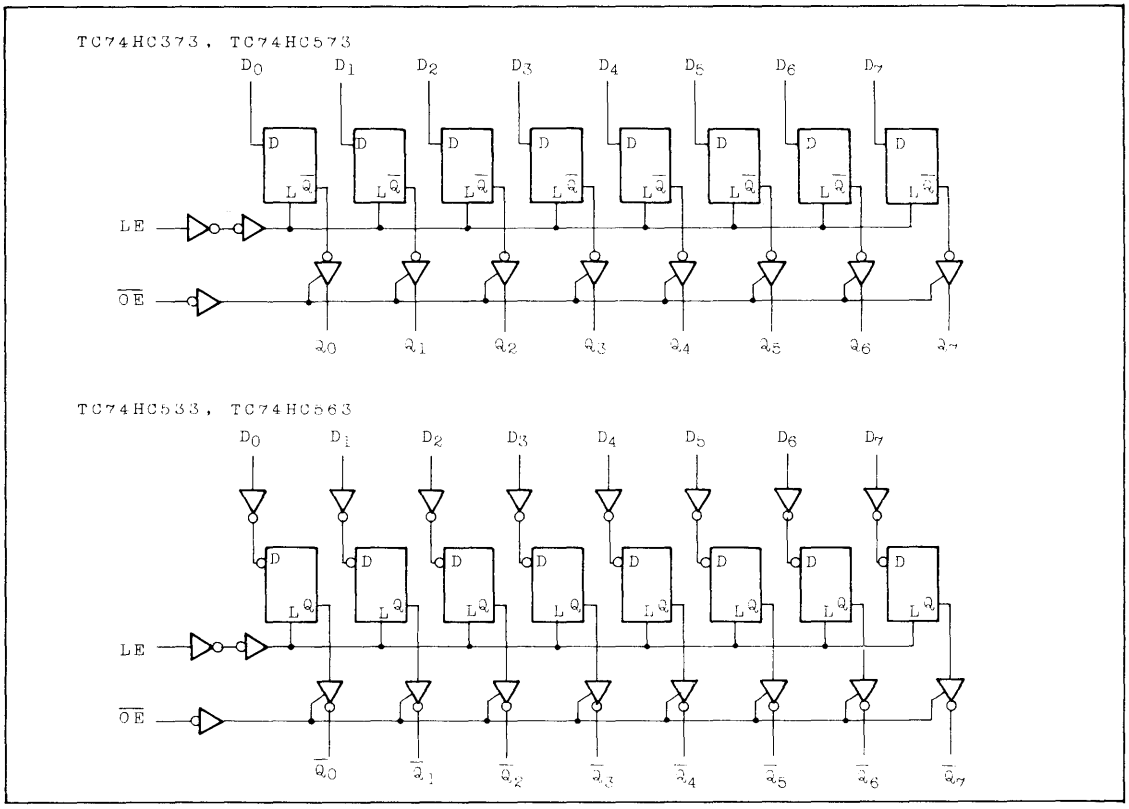
X : Don't care

Z : High impedance

• : Q/$\overline{Q}$ outputs are latched at the time when the LE input is taken low logic level.

TC74HC373P/F•TC74HC533P/F
TC74HC563P/F•TC74HC573P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

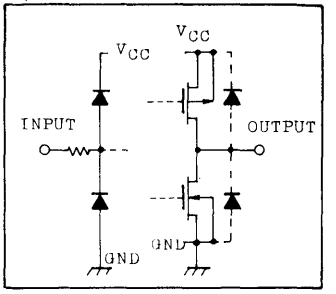
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC373P/F・TC74HC533P/F
TC74HC563P/F・TC74HC573P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (LE - Q, $\overline{Q}$) *	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (D - Q, $\overline{Q}$) *	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time (LE - Q, $\overline{Q}$) **	t_{pLH} t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Propagation Delay Time (D - Q, $\overline{Q}$) **	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Minimum Pulse Width (LE)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time	t_h		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Output Enable Time *	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Output Disable Time *	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Output Enable Time **	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	64	140	-	175	
			4.5	-	16	28	-	35	
			6.0	-	14	24	-	30	
Output Disable Time **	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	84	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	41	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

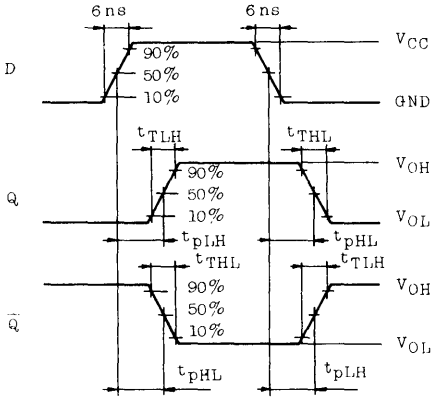
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Latch)}$$

(2) *: for TC74HC373/533
**: for TC74HC563/573

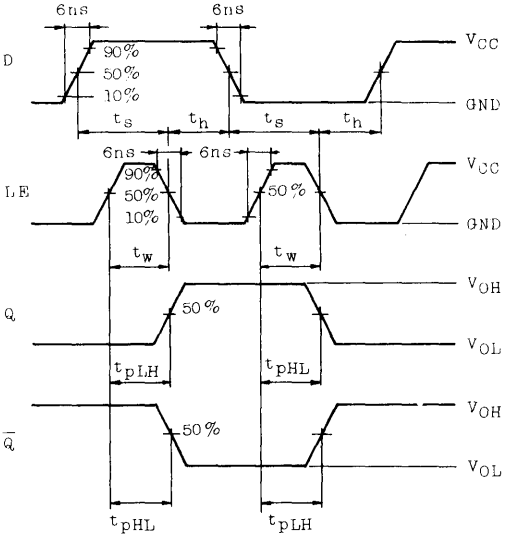
TC74HC373P/F • TC74HC533P/F
TC74HC563P/F • TC74HC573P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL} (D - Q,$\overline{Q}$)



t_{pLH}, t_{pHL} (LE - Q,$\overline{Q}$), t_s, t_h, t_w

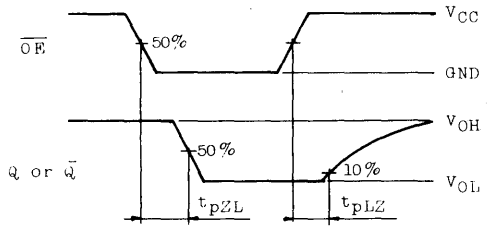


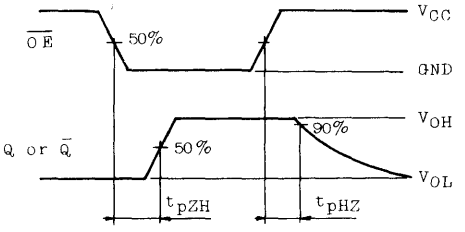
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{pHZ}, t_{pZH}

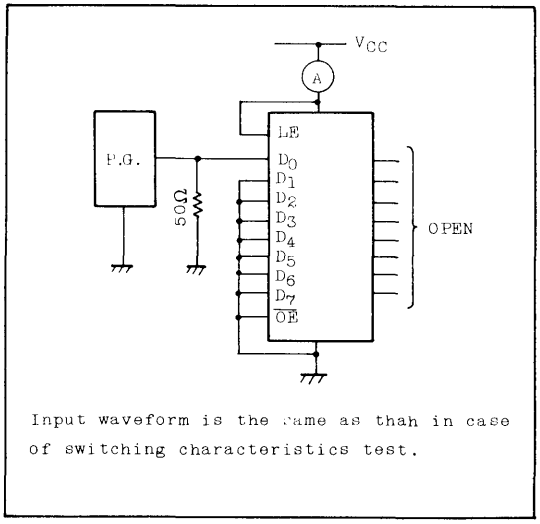
The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TC74HC373P/F•TC74HC533P/F
TC74HC563P/F•TC74HC573P/F

$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as thah in case of switching characteristics test.

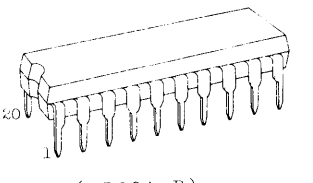
TC74HCT373P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

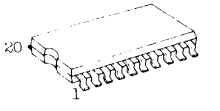
PRELIMINARY

TC74HCT373P/F OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT

The TC74HCT373 is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
It may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT373 is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data.
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The TC74HCT373 and the TC74HCT573 have the same function and the same characteristics respectively, but have the different pin layouts. The three-state output configuration and the wide choise of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)

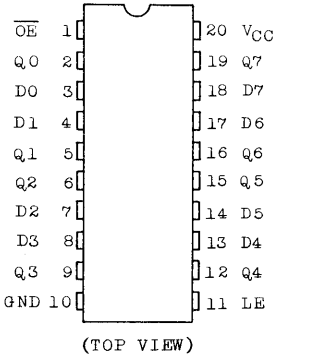


MFP20(F20GA-P)

FEATURES:

- High speed ..... t_{pd}=19ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V (Min.), V_{IL}=0.8V(Max.)
- Wide interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS373

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE}$	LE	D	Q(HCT373)
H	X	X	Z
L	L	X	No change*
L	H	L	L
L	H	H	H

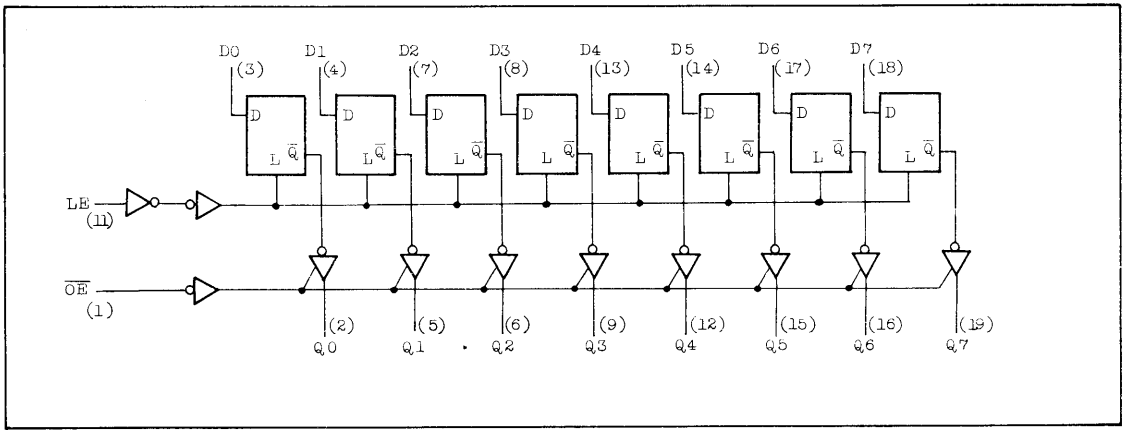
X: Don't care

Z: High impedance

*: Q output was latched at the time when the LE input is taken low logic level.

TC74HCT373P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

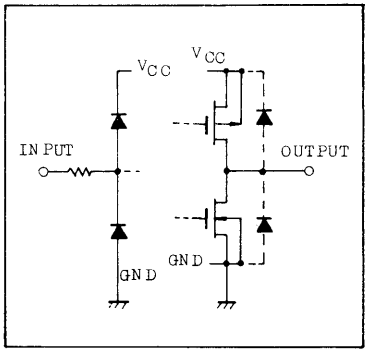
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT373P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (LE - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Propagation Delay Time (D - Q)	t_{pLH} t_{pHL}		4.5	-	23	35	-	44	ns
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	ns

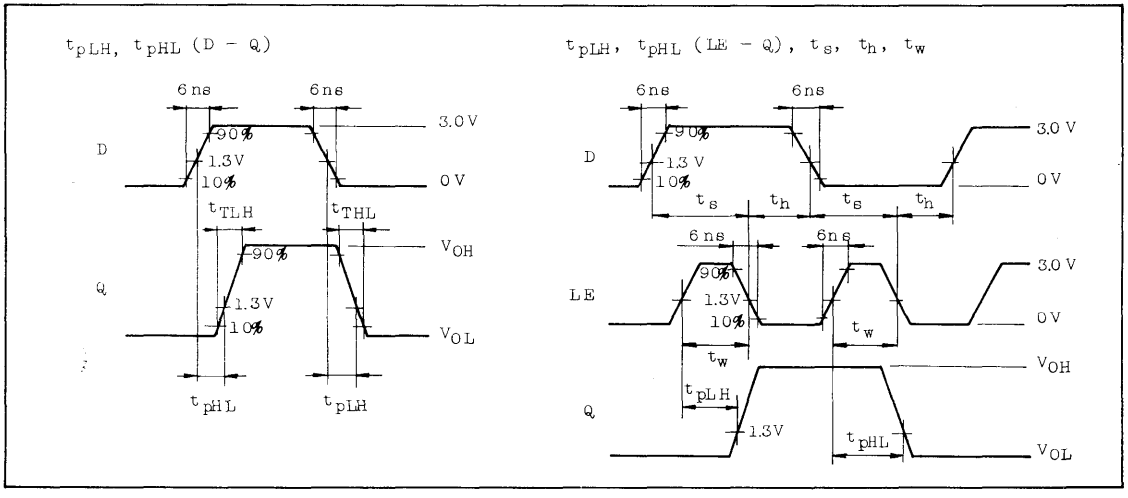
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Set-up Time	t_s		4.5	-	0	5	-	6	ns
Minimum Hold Time	t_h		4.5	-	3	10	-	13	
Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	23	35	-	44	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	21	30	-	38	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	55	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumpiton without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HCT373P/F

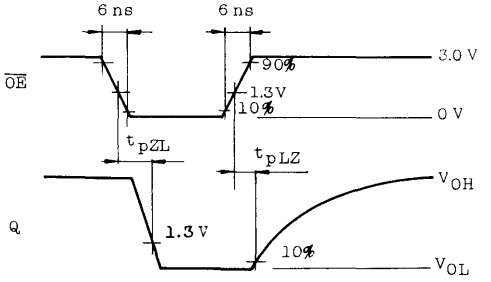
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)

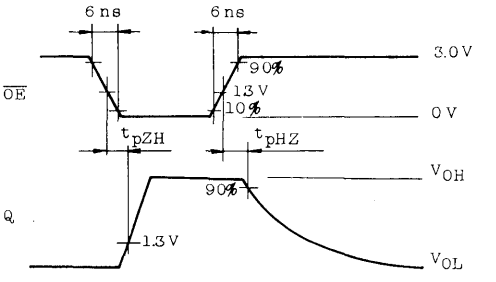
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line to GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

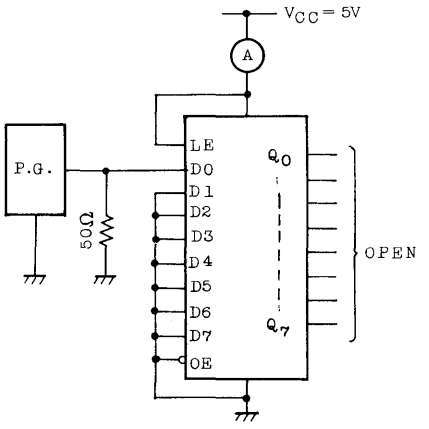
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.

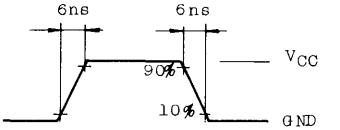




I_{CC}(Opr.) TEST CIRCUIT



INPUT WAVEFORM



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

PRELIMINARY

OCTAL D-TYPE FLIP-FLIP WITH 3-STATE OUTPUT

TC74HC374P/F NON-INVERTING
TC74HC534P/F INVERTING
TC74HC564P/F INVERTING
TC74HC574P/F NON-INVERTING

The TC74HC374P, TC74HC534P, TC74HC564P and TC74HC574P are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.

These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input ($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely (HC374 and HC574) or inversely (HC534 and HC564) to the logic state that were setup at the D inputs.

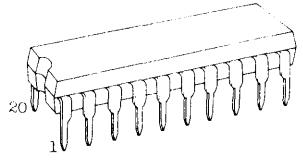
While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

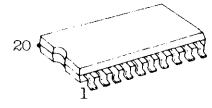
The TC74HC374 and the TC74HC574, the TC74HC534 and the TC74HC564 are identical respectively except the pin layout. The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....f_{MAX}=45MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..V_{CC}(opr)=2V ~ 6V
- Pin and Function Compatible with 74LS374/534/564/574



DIP20(3D20A-P)

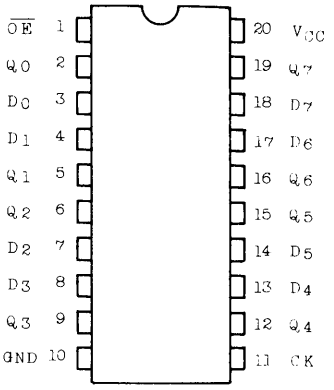


MFP20(F20GA-P)

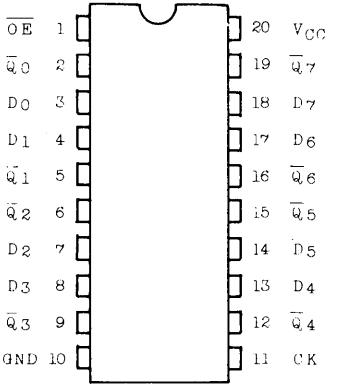
TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

PIN ASSIGNMENT

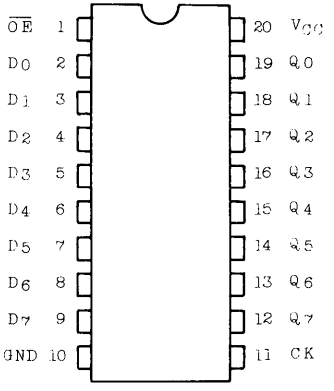
TC74HC374



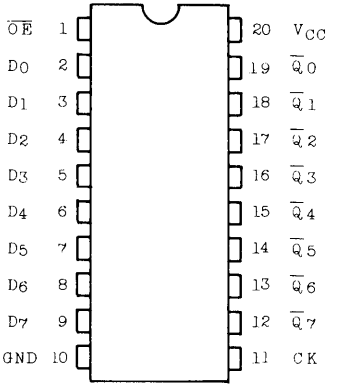
TC74HC534



TC74HC574



TC74HC564



TRUTH TABLE

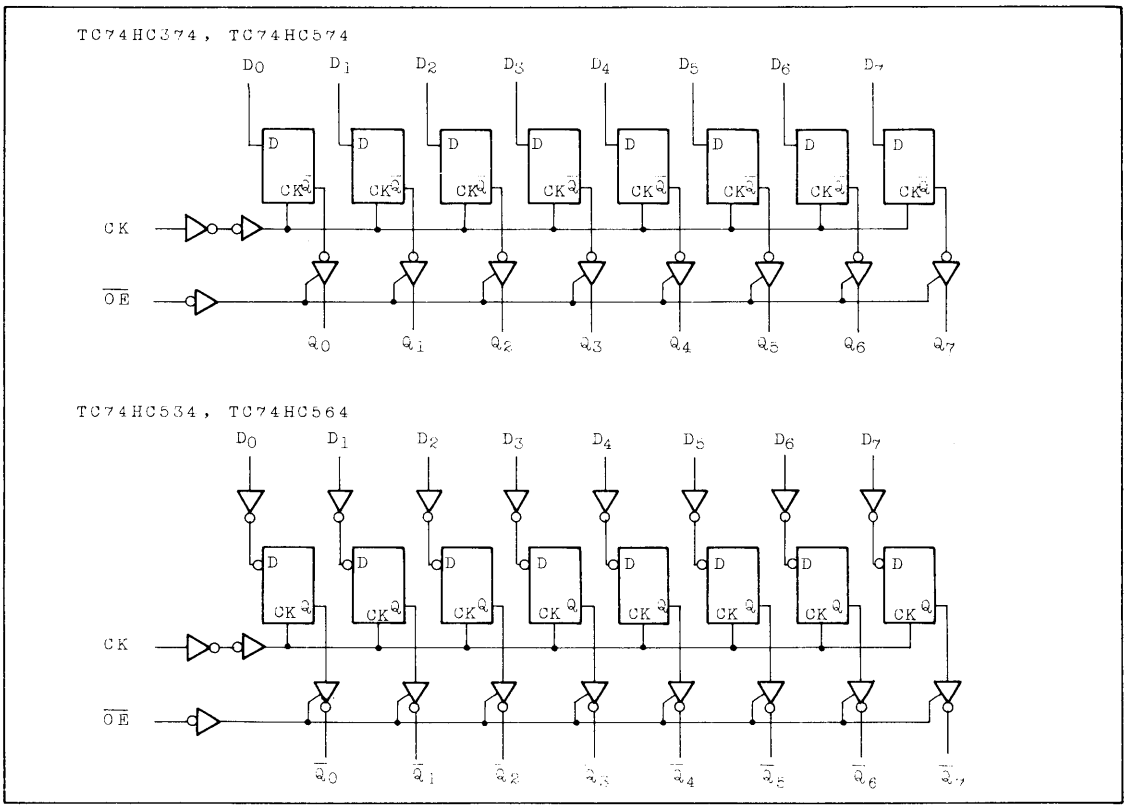
INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q (HC374,HC574)	$\overline{Q}$ (HC534,HC564)
H	X	X	Z	Z
L	↓	X	No change	No change
L	↑	L	L	H
L	↑	H	H	L

X : Don't care

Z : High impedance

TC74HC374P/F·TC74HC534P/F
TC74HC564P/F·TC74HC574P/F

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

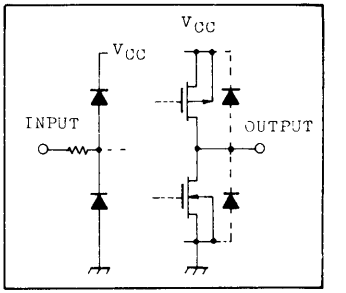
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CK - Q, $\overline{Q}$) *	t_{pLH}		2.0	-	88	175	-	220	
	t_{pHL}		4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (CK - Q, $\overline{Q}$) **	t_{pLH}		2.0	-	76	150	-	190	
	t_{pHL}		4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	24	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (CK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
	$t_{w(H)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time *	t_s		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Minimum Hold Time *	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Minimum Set up Time **	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time **	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Enable Time *	t_{pZL}	R_L=1kΩ	2.0	-	72	150	-	190	
	t_{pZH}		4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Output Disable Time *	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
	t_{pHZ}		4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Output Enable Time **	t_{pZL}	R_L=1kΩ	2.0	-	64	140	-	175	
	t_{pZH}		4.5	-	16	28	-	35	
			6.0	-	14	24	-	30	
Output Disable Time **	t_{pLZ}	R_L=1kΩ	2.0	-	84	150	-	190	
	t_{pHZ}		4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	$C_{PD(1)}$			-	51	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Flip-Flop)}$$

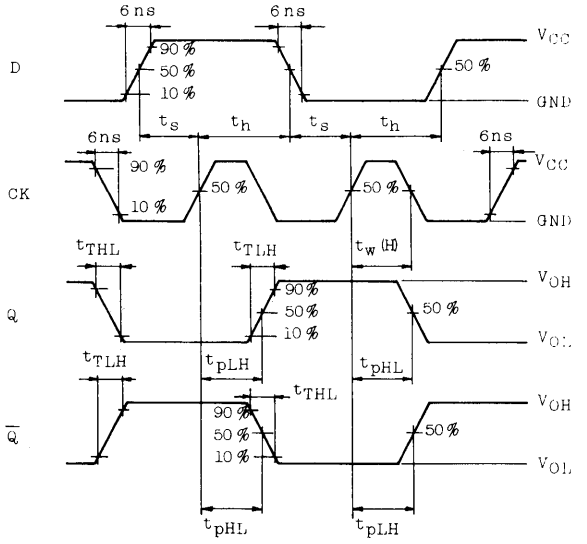
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation. $C_{PD(TOTAL)} = 34 + 17 \times N$ [pF]

(2) *: for TC74HC374/534
**: for TC74HC564/574

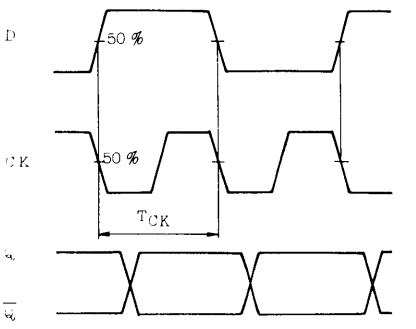
TC74HC374P/F • TC74HC534P/F
TC74HC564P/F • TC74HC574P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



f_{MAX}



Duty cycle of CK: 50%

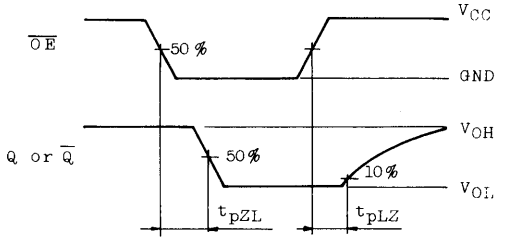
$$f_{MAX} = \frac{1}{T_{CK}}$$

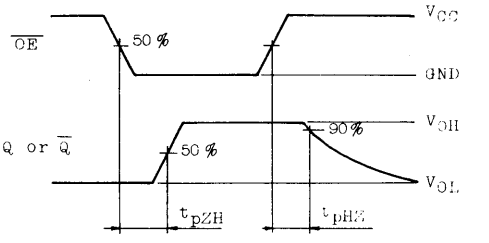
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

t_{pHZ}, t_{pZH}

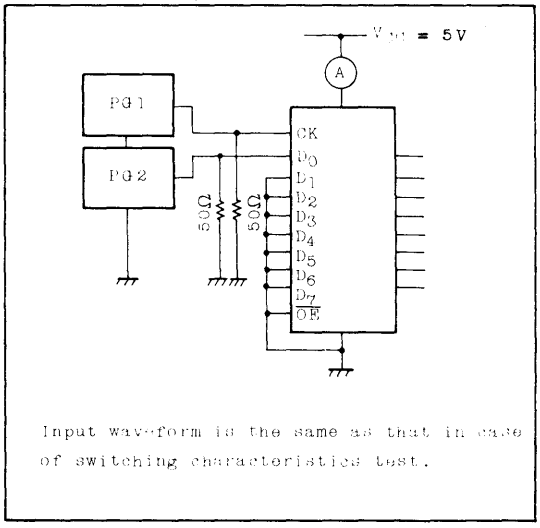
The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ input is held low.





TC74HC374P/F•TC74HC534P/F
TC74HC564P/F•TC74HC574P/F

$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HCT374P/F CMOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HCT374P/F OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The TC74HCT374 is high speed CMOS OCTAL FLIP-FOLP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

This IC achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

This IC is controlled by a clock input (CK) and a output enable input ($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely to the logic state that were setup at the D inputs.

While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off.

The application engineer has a choice of combination of inverting and non-inverting outputs, symmetrical and neighboring input/output pin layout.

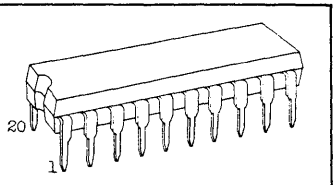
The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

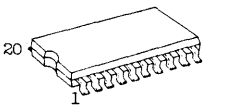
- High Speed ..... f_{MAX}=41MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Wide interfacing ability ..... LSTTL, NMOS, CMOS
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS374

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).



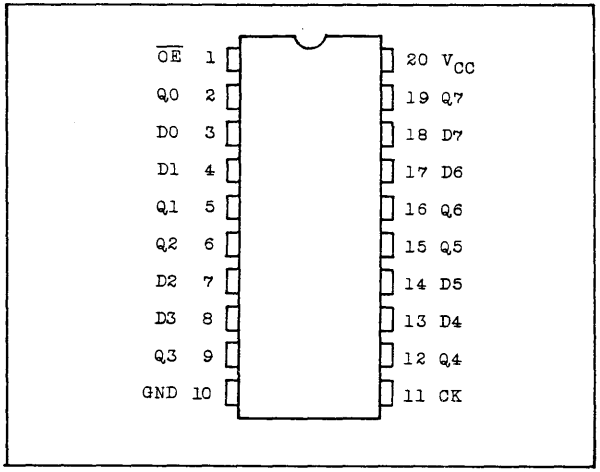
DIP20(3D20A-P)



MFP20(F20GA-P)

TC74HCT374P/F

PIN ASSIGNMENT



TRUTH TABLE

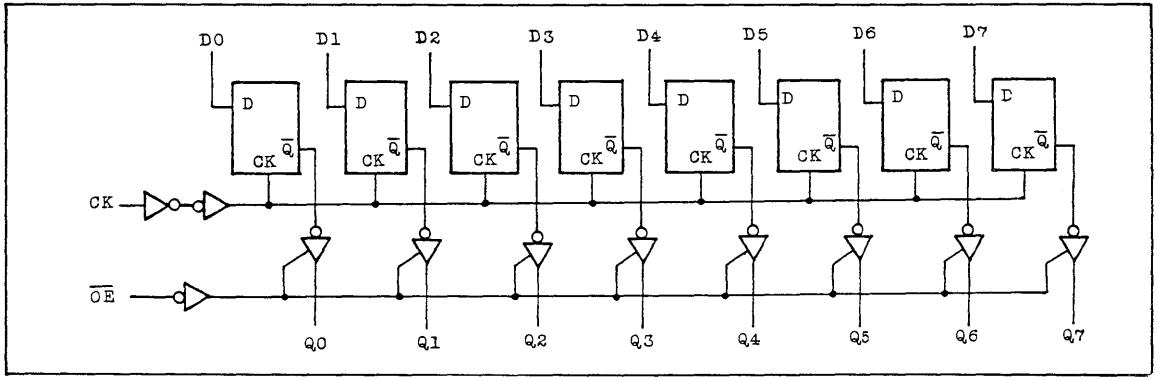
INPUTS			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't care

Z: High impedance

Qn: No change

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500 (DIP)* 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

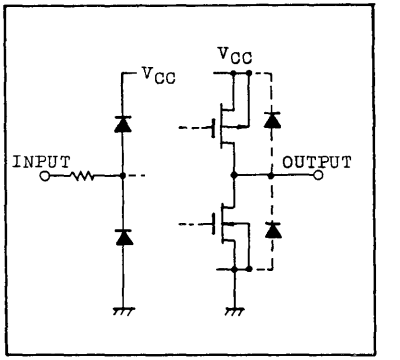
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C to 85°C derating factor of -10mW/°C shall be applied until 300mW.

TC74HCT374P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=0.5V or 2.4V Other inputs: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (CK - Q)	t_{pLH} t_{pHL}		4.5	-	26	40	-	50	ns
Maximum Clock Frequency	f_{MAX}		4.5	25	38	-	20	-	MHz
Minimum Pulse Width (CLOCK)	$t_{w(L)}$ $t_{w(H)}$		4.5	-	13	25	-	32	ns
Minimum Set-up Time	t_s		4.5	-	6	15	-	19	ns
Minimum Hodl Time	t_h		4.5	-	-	0	-	0	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	27	42	-	53	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	22	32	-	40	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	60	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Flip-Flop)}$$

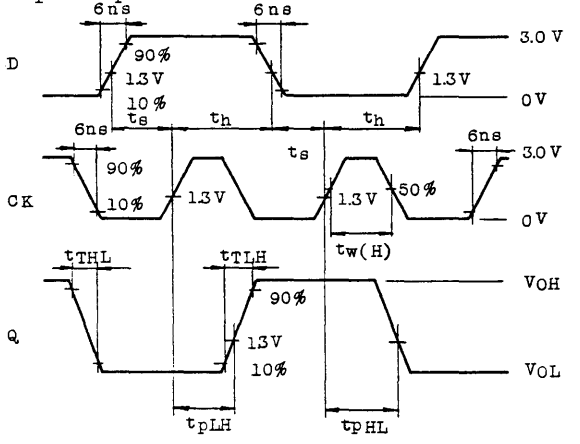
And the C_{PD} when n circuits of FLIP-FLOP operate, can be gained by the following equation.

$$C_{PD}(TOTAL)=42+18 \cdot n \text{ (pF)}$$

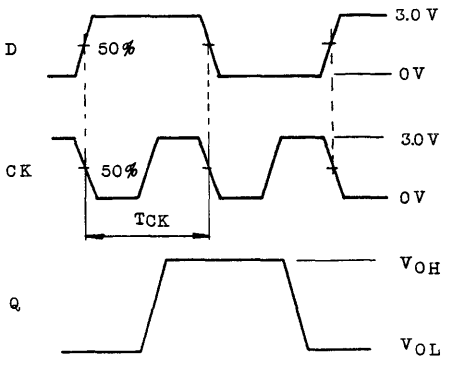
TC74HCT374P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



f_{MAX}.



Duty cycle of CK: 50%

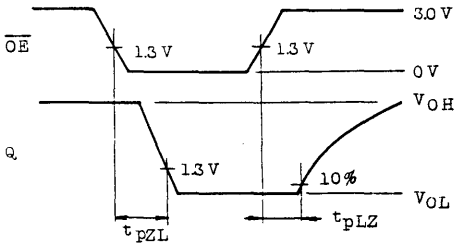
$$f_{MAX}=\frac{1}{T_{CK}}$$

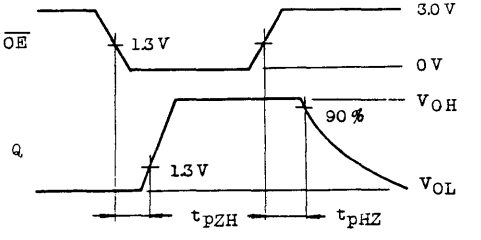
t_{pLZ}, t_{pZL}

The 1kΩ load resistors should be connected between outputs and V_{CC} line and the 50pF load capacitors should be connected between outputs and GND line.
All inputs except $\overline{OE}$ input should be connected to V_{CC} line or GND line such that outputs will be in low logic level while $\overline{OE}$ input is held low.

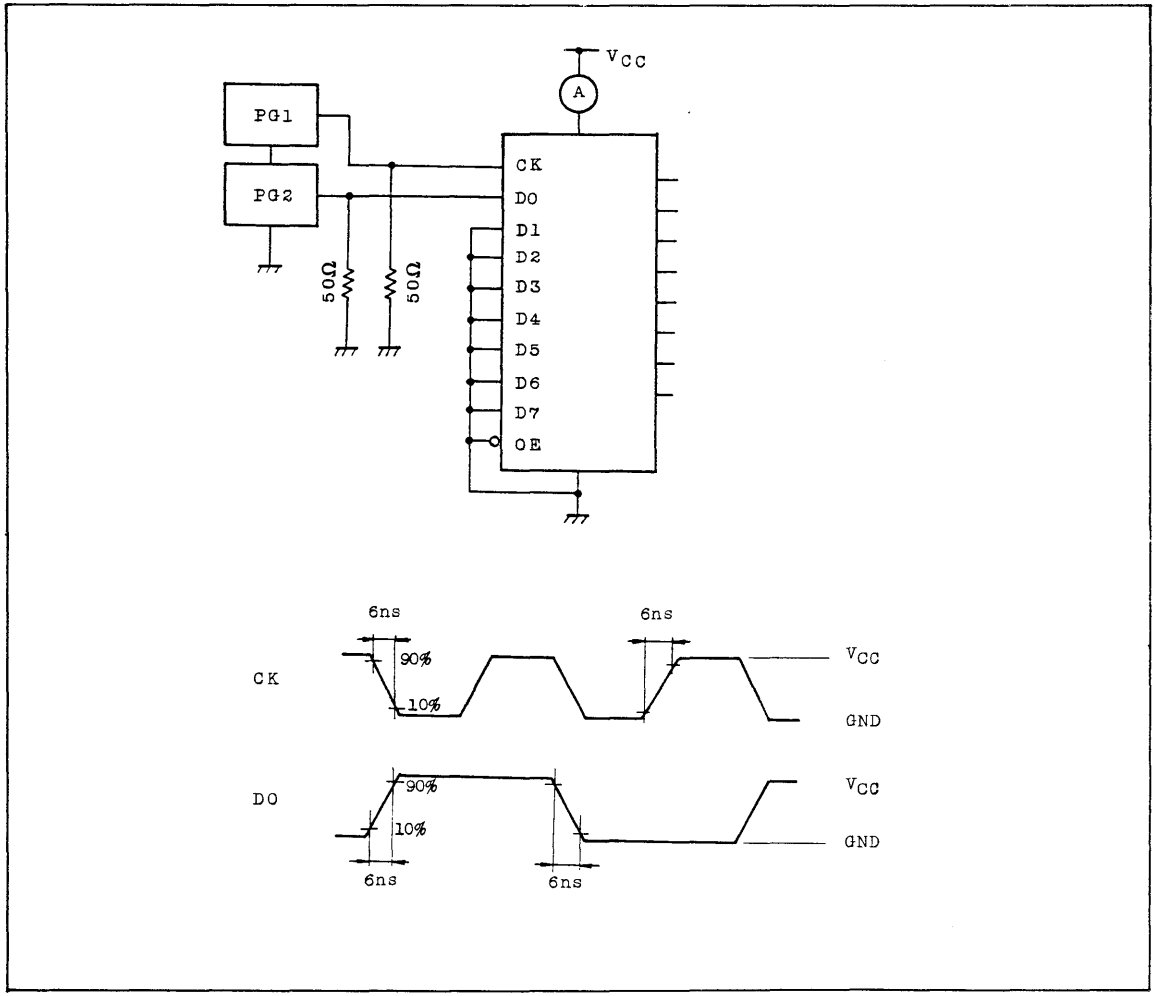
t_{pHZ}, t_{pZH}

The 1kΩ load resistors and the 50pF load capacitors should be connected between each output and GND line.
All inputs except $\overline{OE}$ input shuld be connected to V_{CC} or GND line such that output will be in high logic level while $\overline{OE}$ inputs is held low.





$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC375P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

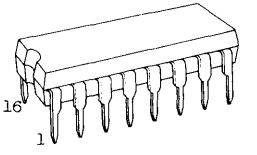
TC74HC375P/F 4-BIT D-TYPE LATCH

GENERAL DESCRIPTION

The TC74HC375 is a high speed CMOS 4-BIT D-TYPE LATCH fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contains two groups of 2-bit latches controlled by a enable input (G1·2 or G3·4). And those two latch groups can be used in the different circuits. Each latch has Q and $\overline{Q}$ outputs (1Q thru 4Q and $1\overline{Q}$ thru $4\overline{Q}$). The data applied to the data input is transfered to the Q and $\overline{Q}$ outputs when the enable input is taken high and the outputs will follow the data input as long as the enable input is kept high. When the enable input is taken low, the information data applied to the data input at a time is retained at the outputs.
All inputs are equipped with protection circuits against static discharge of transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=16ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS375



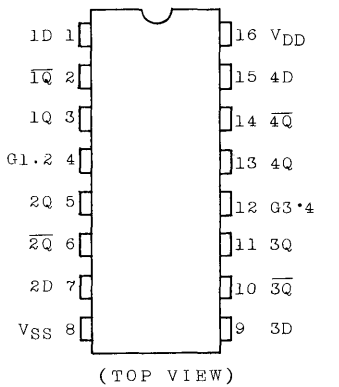
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

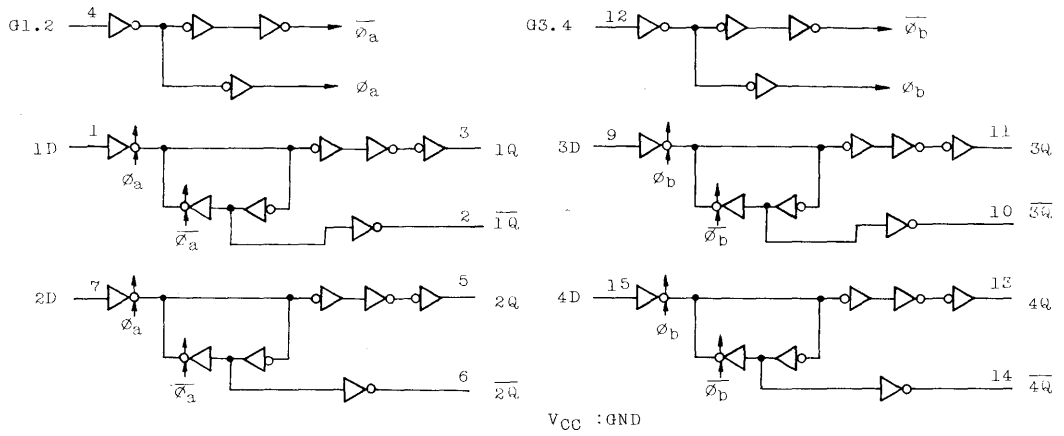
TC74HC375P/F

TRUTH TABLE

INPUTS		OUTPUTS		FUNCTION
D	G	Q	$\bar{Q}$	
L	H	L	H	–
H	H	H	L	–
X	L	Qn	$\bar{Q}$n	LATCH

X : DON'T CARE

LOGIC DIAGRAM

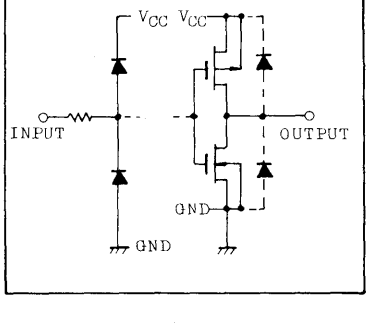


V_{CC} :GND

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC375P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (DATA - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Propagation Delay Time (G - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	80	160	-	200	
			4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	
Minimum Enable Pulse Width (G)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

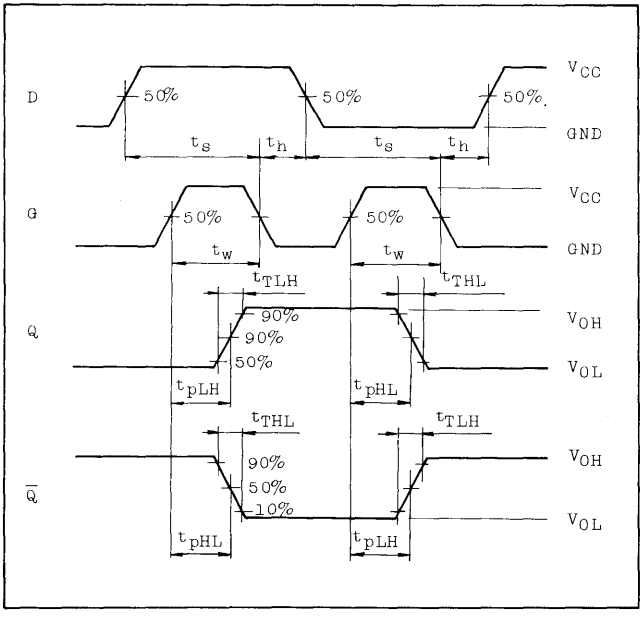
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time	t_s		2.0	-	10	50	-	65	ns
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
Minimum Hold Time	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	48	-	-	-	

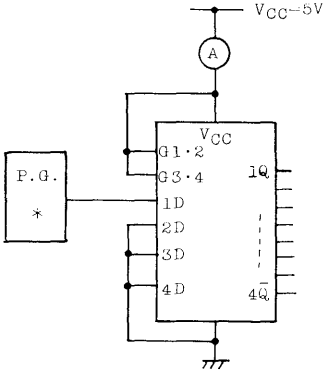
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC386P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC386P/F QUAD EXCLUSIVE-OR GATE

The TC74HC386 is a high speed CMOS EXCLUSIVE-OR GATE fabricated with silicon gate C²MOS technology.

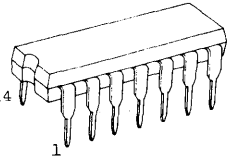
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Output buffer is equiped, which enables high noise immunity and stable output.

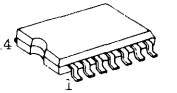
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=12ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS386

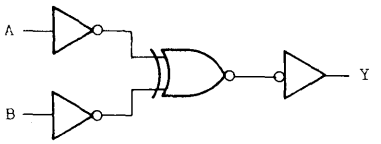


DIP14(3D14A-P)

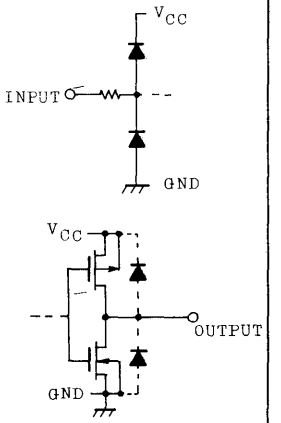


MFPi4(F14GB-P)

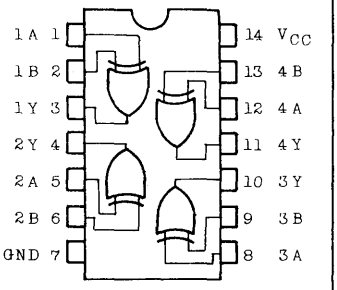
LOGIC DIAGRAM (PER GATE)



INPUT and OUTPUT EQUIVALENT CIRCUIT



PIN ASSIGMENT



(Top View)

TC74HC386P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC386P/F

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

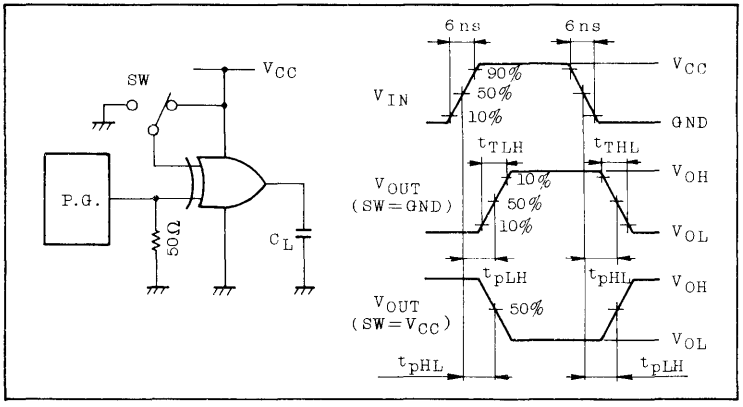
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	ns
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)		-	33	-	-	-	

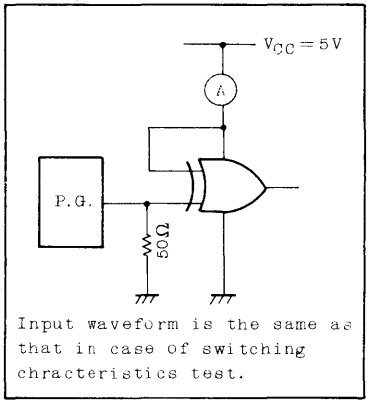
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

TC74HC386P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr) TEST CIRCUIT



Input waveform is the same as that in case of switching chracteristics test.

TC74HC390P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

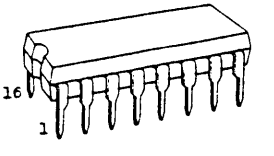
PRELIMINARY

TC74HC390P/F DUAL DECADE COUNTER

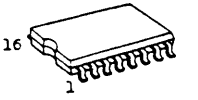
The TC74HC390P is a high speed CMOS DUAL DECADE COUNTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of two independent 4-bit counters, each composed of a divide-by-two and divide-by-five counter. A divide-by-two counter is incremented on the negative going transition of $\overline{CLOCKA}$. A divide-by-five counter is incremented on the negative going transition of $\overline{CLOCKB}$. The counter can be cascaded to form decade, bi-quinary, or various combinations up to a divide-by-100 counter. When the CLEAR input is set high, all Q outputs are set to low level independent of the clock input.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=63MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS390



DIP 16(3D16A-P)



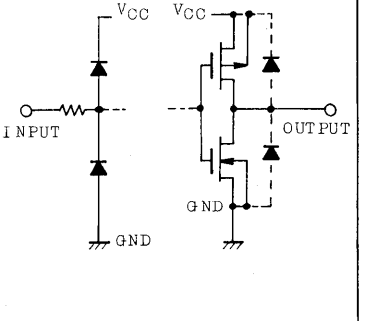
MFP 16(F16QC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	Tstg	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

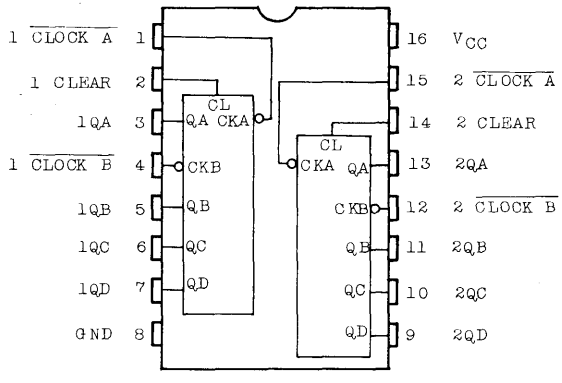
* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



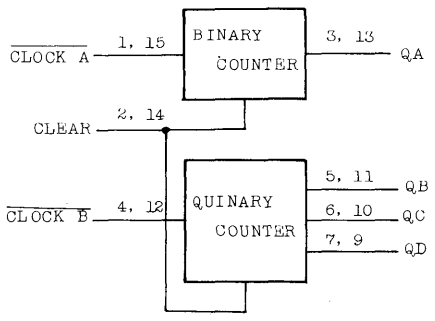
TC74HC390P/F

PIN ASSIGNMENT



(TOP VIEW)

BLOCK DIAGRAM



V_{CC} = 16, GND = 8

TRUTH TABLE

COUNT	OUTPUTS							
	BCD COUNT*				BI-QUINARY**			
	QD	QC	QB	QA	QA	QD	QC	QB
0	L	L	L	L	L	L	L	L
1	L	L	L	H	L	L	L	H
2	L	L	H	L	L	L	H	L
3	L	L	H	H	L	L	H	H
4	L	H	L	L	L	H	L	L
5	L	H	L	H	H	L	L	L
6	L	H	H	L	H	L	L	H
7	L	H	H	H	H	L	H	L
8	H	L	L	L	H	L	H	H
9	H	L	L	H	H	H	L	L

INPUTS			OUTPUTS			
$\overline{\text{CLOCK A}}$	$\overline{\text{CLOCK B}}$	CLEAR	QA	QB	QC	QD
X	X	H	L	L	L	L
↓	X	L	BINARY COUNT UP			
X	↓	L	QUINARY COUNT UP			

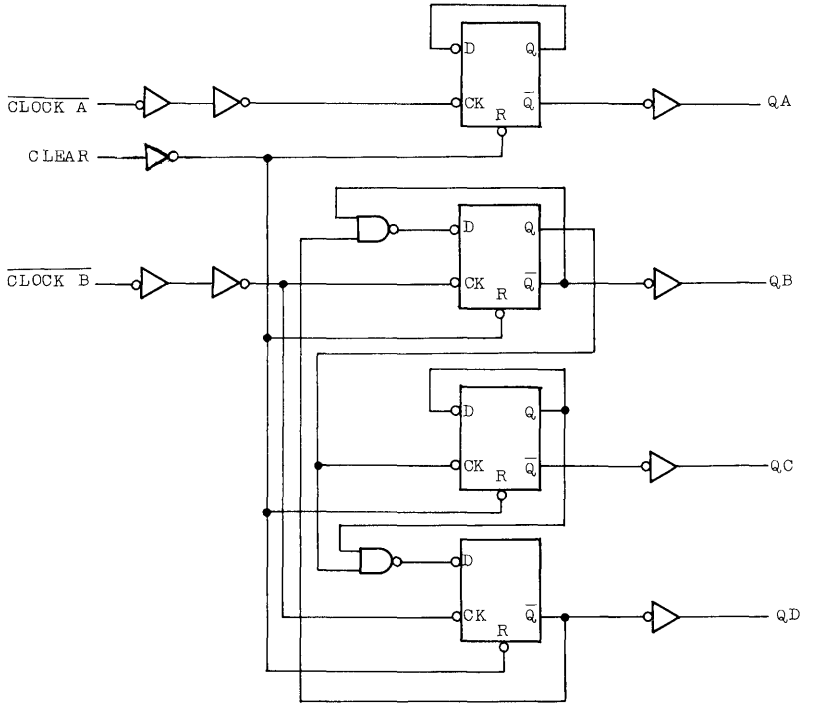
X : DON'T CARE

NOTE * : OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$ FOR BCD COUNT.

** : OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCK A}}$ FOR BI-QUINARY COUNT.

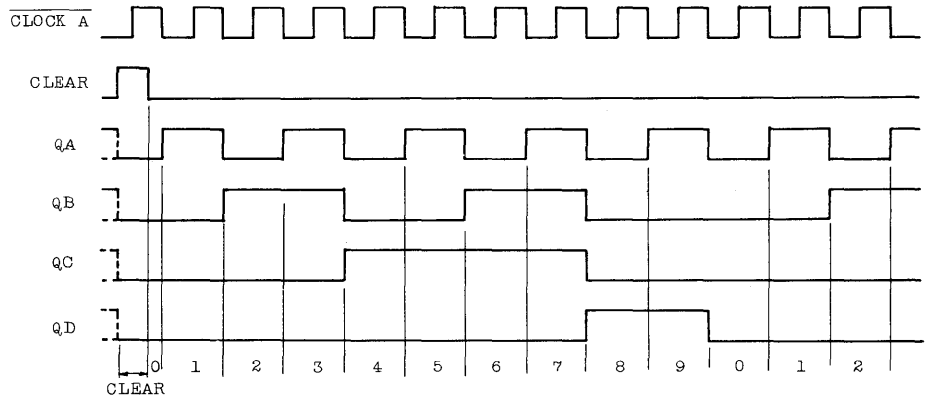
TC74HC390P/F

LOGIC DIAGRAM



TIMING CHART

(1) BCD COUNT SEQUENCE *

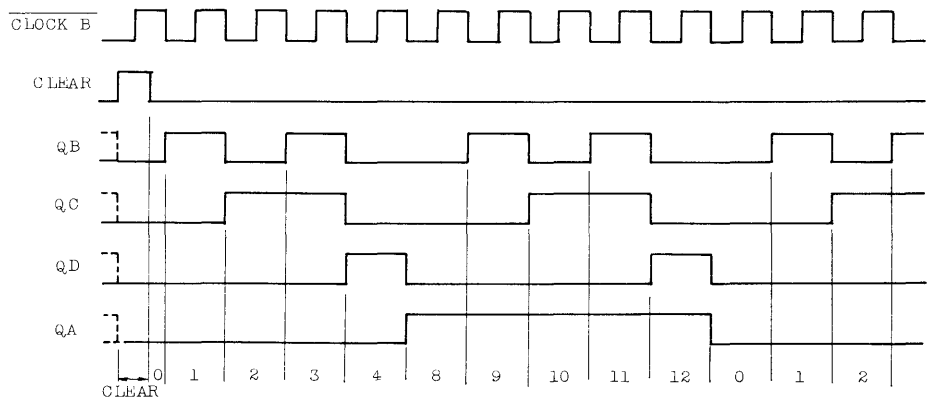


* OUTPUT QA IS CONNECTED TO INPUT $\overline{\text{CLOCK B}}$

TC74HC390P/F

TIMING CHART

(2) BI-QUINARY COUNT SEQUENCE **



** OUTPUT QD IS CONNECTED TO INPUT $\overline{\text{CLOCKA}}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}		2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}		2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	

TC74HC390P/F-

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK\ A}$ - Q_A)	t_{pLH} t_{pHL}		2.0	-	64	130	-	165	
			4.5	-	16	26	-	33	
			6.0	-	14	22	-	28	
Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_B, Q_D)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{CLOCK\ B}$ - Q_C)	t_{pLH} t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	

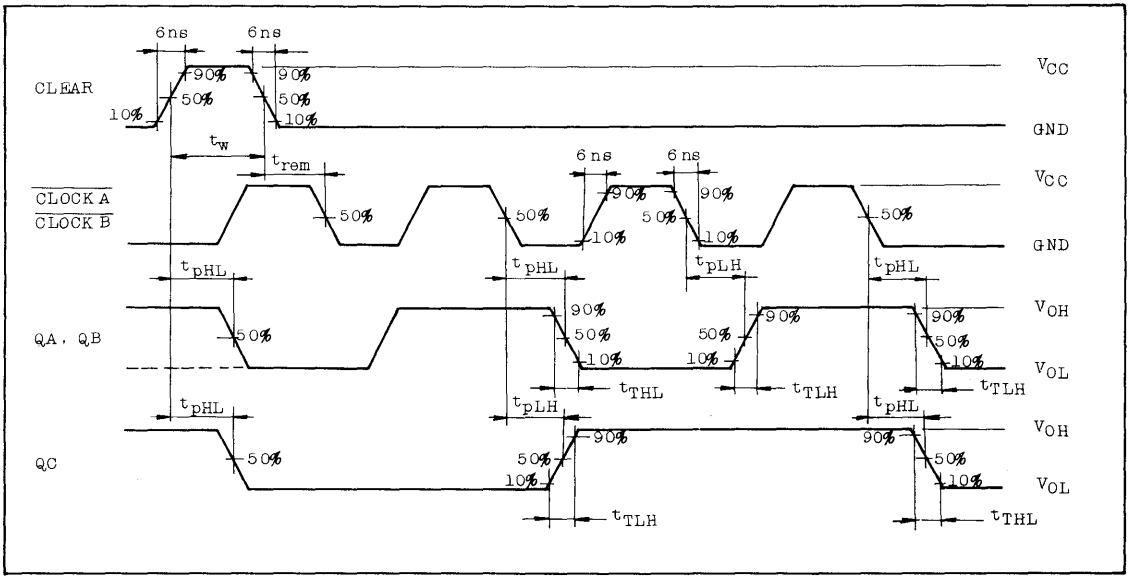
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Max. Clock Frequency $\overline{CLOCK\ A}$ - Q_A	f_{MAX}		2.0	6	15	-	5	-	MHz
			4.5	32	58	-	27	-	
			6.0	38	68	-	32	-	
Max. Clock Frequency $\overline{CLOCK\ B}$ - Q_B	f_{MAX}		2.0	5	10	-	4	-	
			4.5	27	41	-	22	-	
			6.0	32	48	-	26	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	44	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

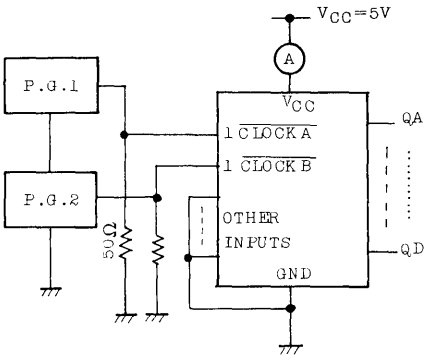
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per Circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

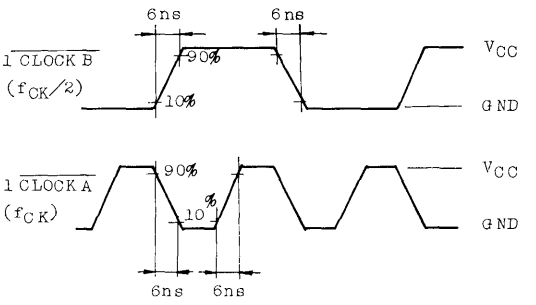


TC74HC390P/F

$I_{CC(opr.)}$ TEST CIRCUIT



INPUT WAVEFORM



WHEN THE OUTPUTS DRIVE CAPACITIVE LOAD, TOTAL CURRENT CONSUMPTION IS TO BE A SUM OF THE VALUE CALCULATED FROM C_{PD} AND ΔI_{CC} OBTAINED FROM THE FOLLOWING FORMULA.

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \frac{Ca}{2} + \frac{f_{CK}}{2} \cdot V_{CC} \left(\frac{2Cb}{5} + \frac{Cc}{5} + \frac{Cd}{5} \right)$$

Ca～Cd ARE THE CAPACITANCE AT QA～QD OUTPUT.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC393P/F

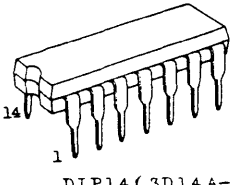
PRELIMINARY

TC74HC393P/F DUAL BINARY COUNTER

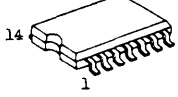
The TC74HC393 is a high speed CMOS DUAL 4-BIT BINARY COUNTER fabricated with silicon C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It contain two independent circuits of counter with same functions in one package, counting or frequency division of eight binary bits can be achieved with one IC.
This device changes state on negative going transition of the clock pulse. The counter can be reset to "0" ($Q0 \sim Q3$="L") by giving "H" level signal to CLEAR input regardless of other inputs.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=68MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS393



DIP14(3D14A-P)



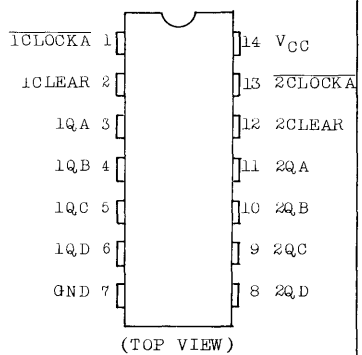
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



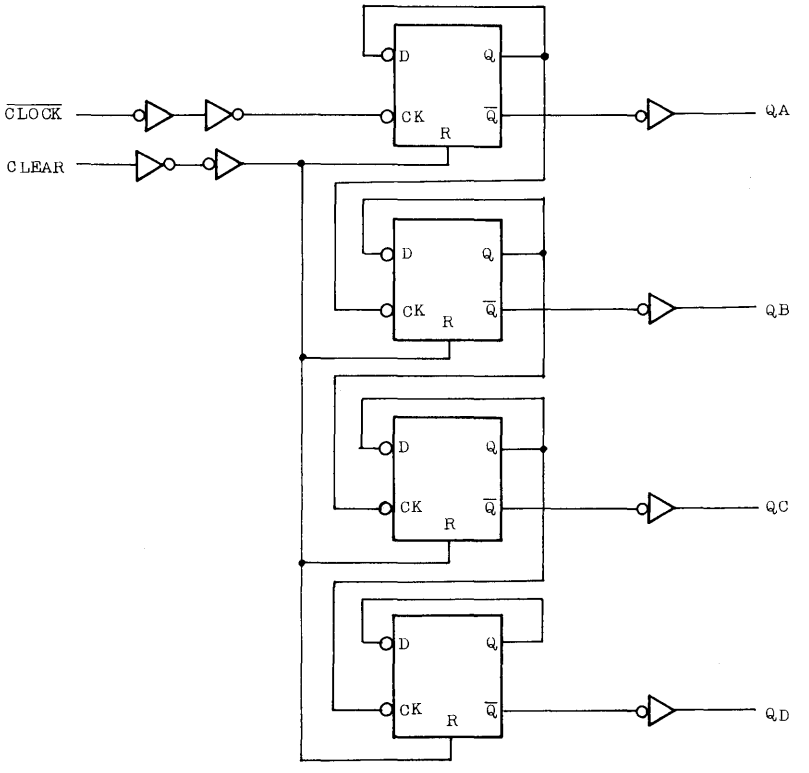
TC74HC393P/F

TRUTH TABLE

COUNT	OUTPUT			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

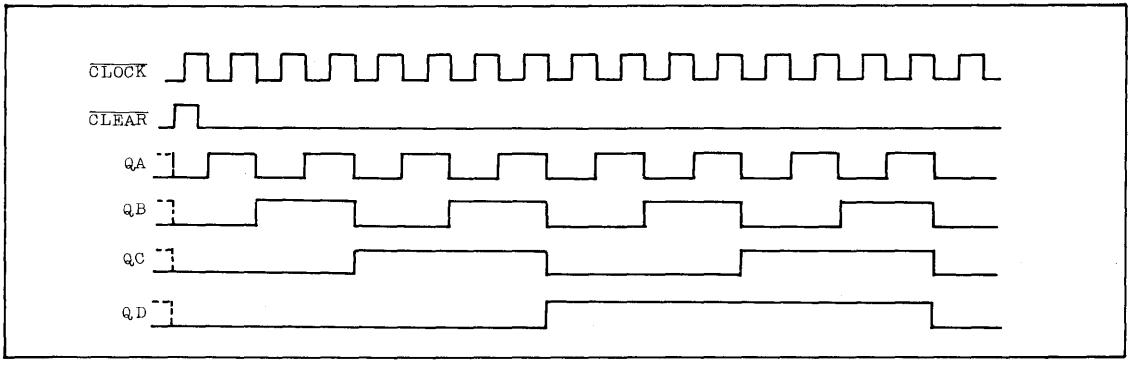
INPUTS		OUTPUTS			
$\overline{CLOCK}$	CLEAR	QA	QB	QC	QD
X	H	L	L	L	L
↓	L	COUNT UP			
↑	L	NO CHANGE			

LOGIC DIAGRAM



TC74HC393P/F

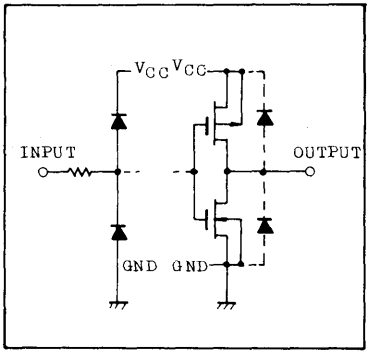
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC393P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	μA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - QA)	t_{pLH} t_{pHL}		2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
Propagation Delay Time ($\overline{CLOCK}$ - QB)	t_{pLH} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time ($\overline{CLOCK}$ - QC)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Propagation Delay Time ($\overline{CLOCK}$ - QD)	t_{pLH} t_{pHL}		2.0	-	140	270	-	340	
			4.5	-	35	54	-	68	
			6.0	-	30	46	-	58	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
Maximum Clock Frequency	f_{MAX}		2.0	6	16	-	5	-	MHz
			4.5	32	62	-	27	-	
			6.0	38	73	-	32	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

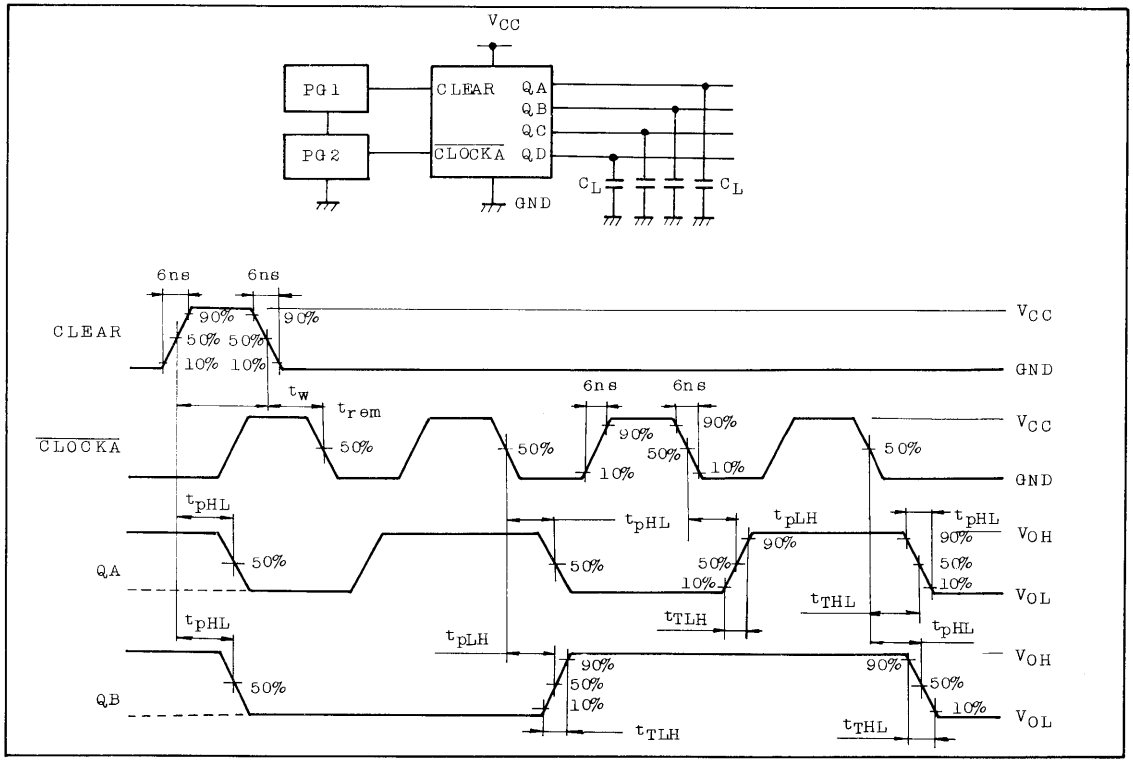
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∼85°C MIN.	Ta=-40∼85°C MAX.	UNIT
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	5	25	-	30	
			4.5	-	0	5	-	6	
			6.0	-	0	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	41	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

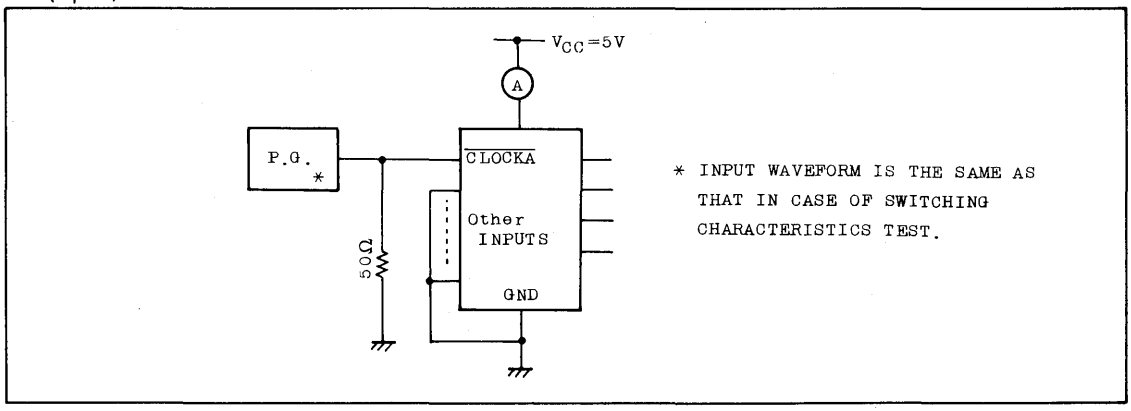
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC393P

I_{CC}(opr.) TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC423P

PRELIMINARY

TC74HC423P DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC423 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is $\overline{A}$ INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CL}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... No limitation

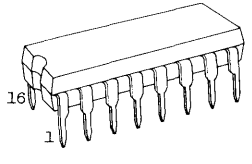
External resistor Rx ..... V_{CC} = 2.0V from 5KΩ to 1MΩ

$V_{CC} \geq$ 3.0V from 1KΩ to 1MΩ

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=28ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range ... t_w(OUT)=120nS ∿ 60s over at V_{CC}=4.5V



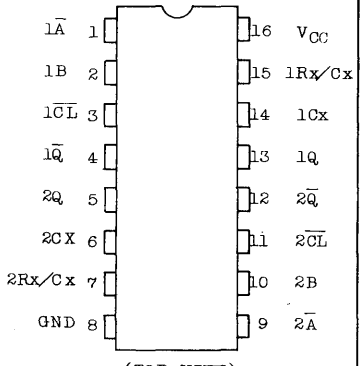
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



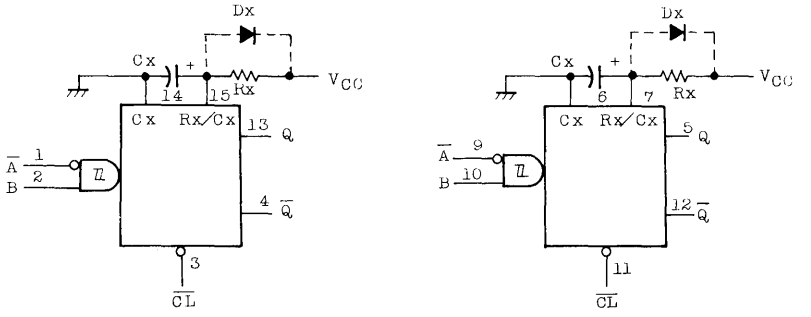
TC74HC423P

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⊓	⊔	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↓	H	⊓	⊔	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

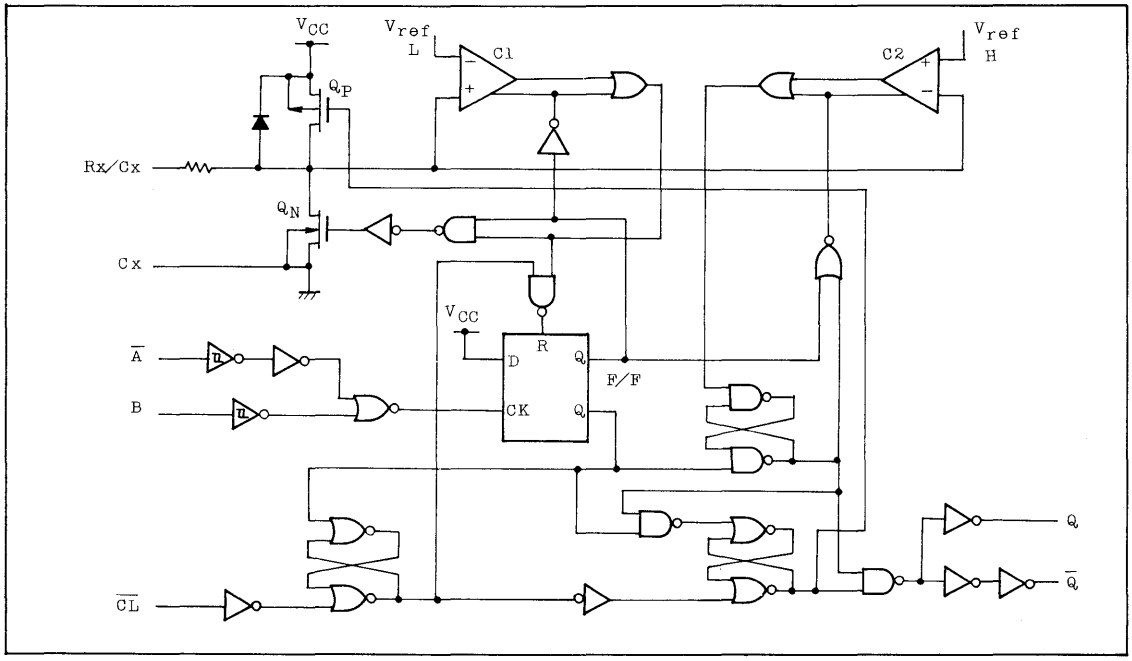
$$t_f \geq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning of to level of voltage supply becoming 0.4 V_{CC})

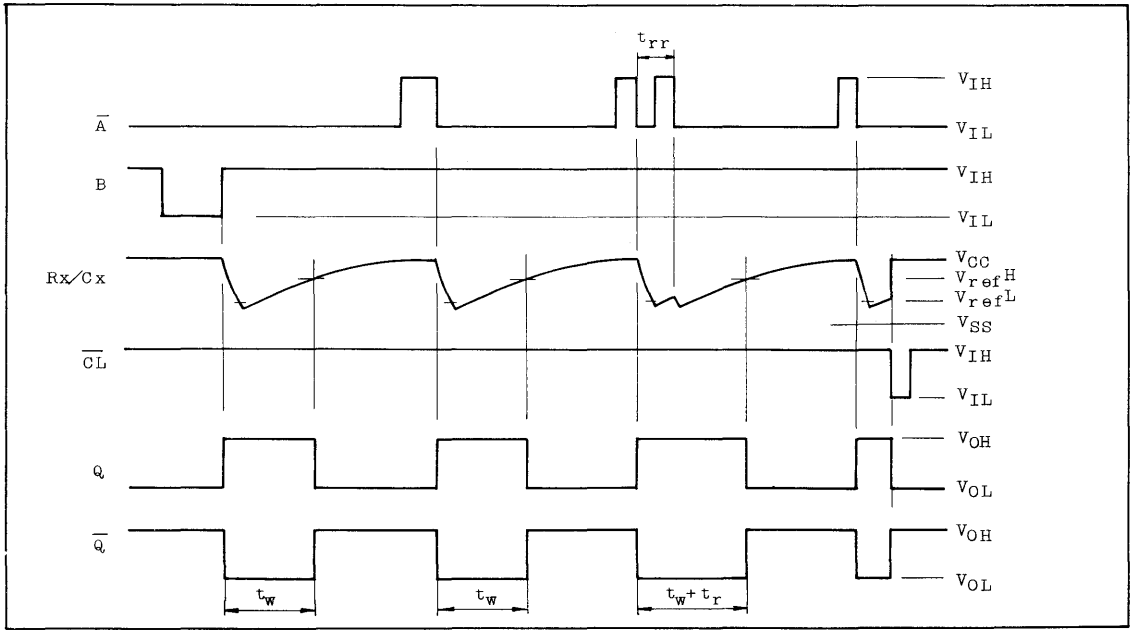
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

TC74HC423P

SYSTEM DIAGRAM



TIMING CHART



TC74HC423P

FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.
After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.
By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{w(OUT)}$ is as follows.

$$t_{w(OUT)} = 0.46 \quad Cx \; Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of Rx/Cx falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(min.) depends on V_{CC} and Cx.

(4) Reset operation

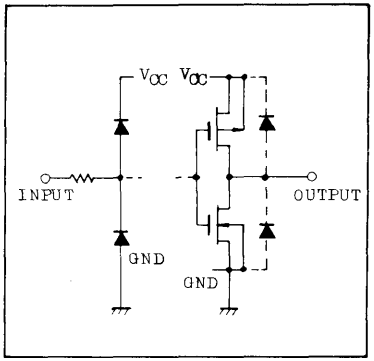
$\overline{CL}$ is normally "H". If $\overline{CL}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CL}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC423P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	Topr	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CL}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) ($V_{CC}\geq$3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/C_{ext}=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

* : Per Circuit

TC74HC423P

AC ELECTRICAL CHARACTERISTICS ($t_r=t_f=6ns$, $C_L=50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$, B - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Minimum Pulse Wdith ($\overline{A}$, B)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Output Pulse Width Error Between Circuits In Same Package	ΔT_{wOUT}			-	±1	-	-	-	%
Minimum Retrigger Time	t_{rr}	Cx=100pF Rx=1kΩ	2.0	-	412	-	-	-	ns
			4.5	-	74	-	-	-	
			6.0	-	63	-	-	-	
		Cx=0.01uF Rx=1kΩ	2.0	-	4.9	-	-	-	μs
			4.5	-	1.1	-	-	-	
			6.0	-	1.0	-	-	-	
Minimum Output Pulse Width	T_{out} (MIN)	Cx=0 Rx=1kΩ	4.5	-	118	-	-	-	ns
Output Pulse Width	T_{out}	Cx=100pF Rx=10kΩ	4.5	-	1.0	-	-	-	μs
		Cx=0.1uF Rx=100kΩ	4.5	-	4.7	-	-	-	ms
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	113	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

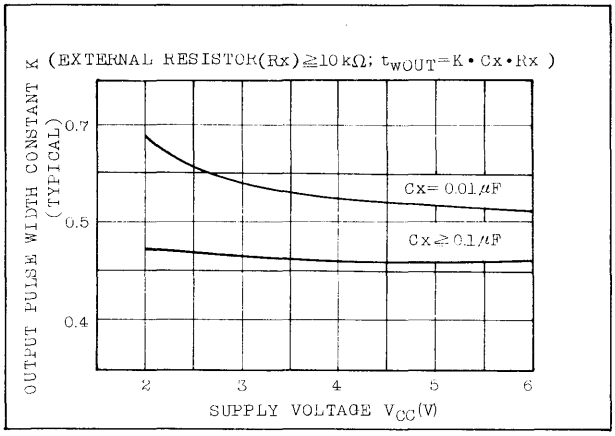
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2 \quad \text{(per monostable)}$$

(I_{CC}': Active Supply Current)

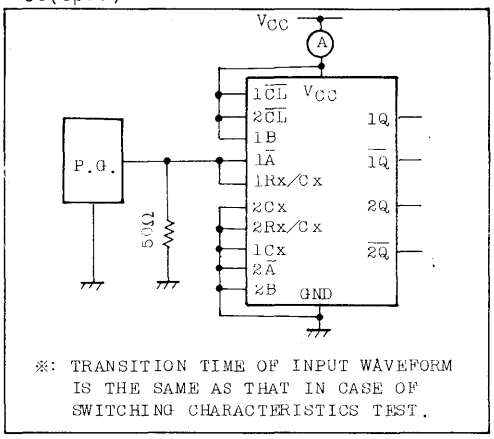
(Duty: %)

TC74HC423P

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

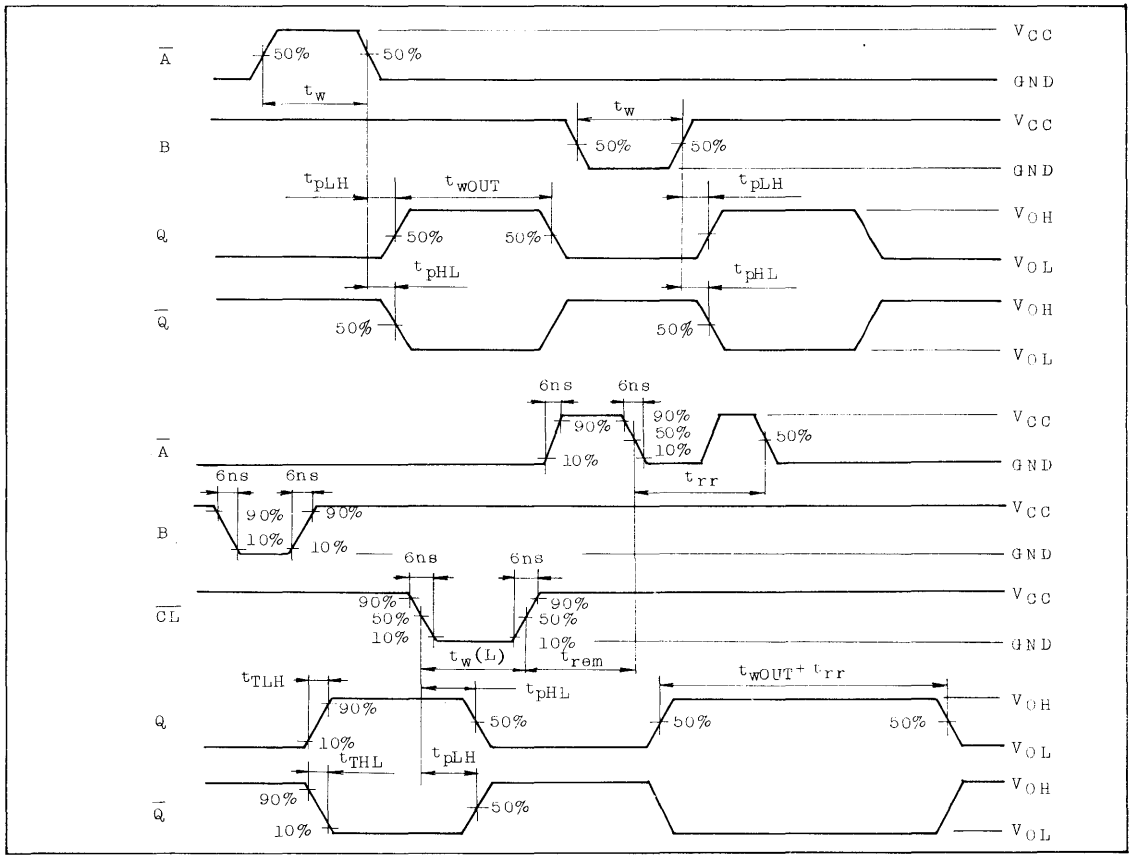


I_{CC}(opr.) TEST WAVEFORM



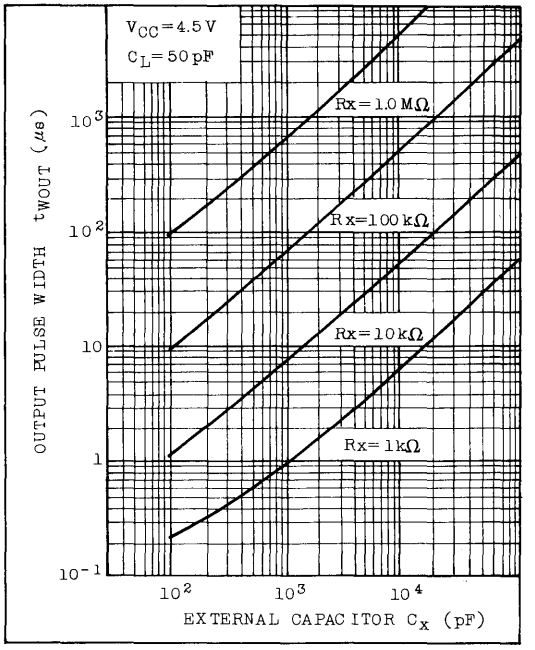
※: TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM

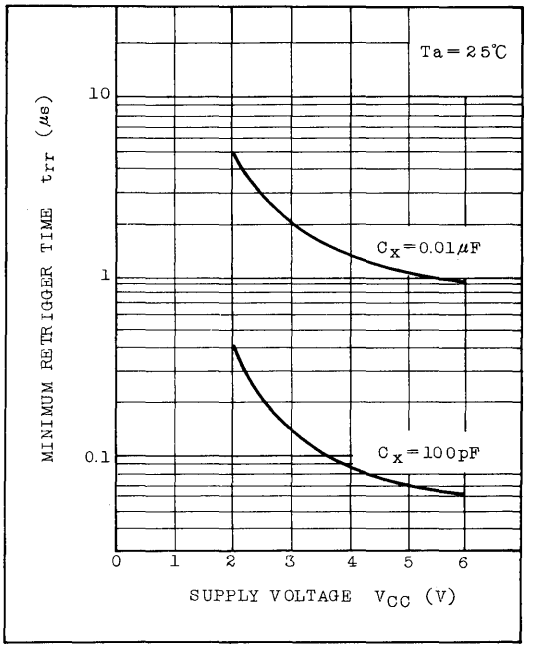


TC74HC423P

t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



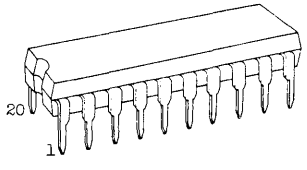
TC74HC540P/F
TC74HC541P/F

CMOS DIGITAL INTEGRATED CIRCUIT

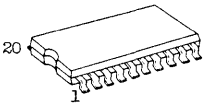
PRELIMINARY

TC74HC540P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HC541P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

The TC74HC540 and TC74HC541 are high speed CMOS OCTAL BUS BUFFER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC540 is non-inverting type. The TC74HC541 is inverting type. If either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)



MFP20(F20GA-P)

FEATURES:

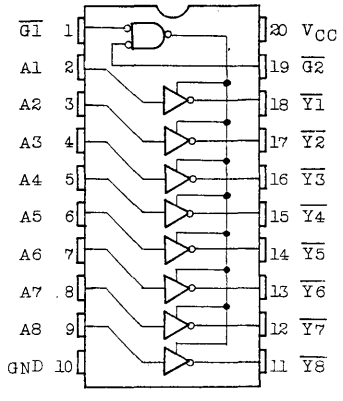
- High Speed ..... t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS540/541

NOTICE FOR APPLICATION

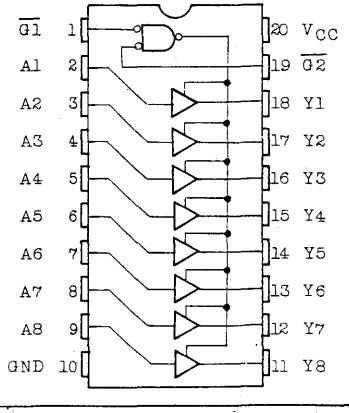
It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

PIN ASSIGNMENT (TOP VIEW)

TC74HC540



TC74HC541



TRUTH TABLE

INPUTS			OUTPUT	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

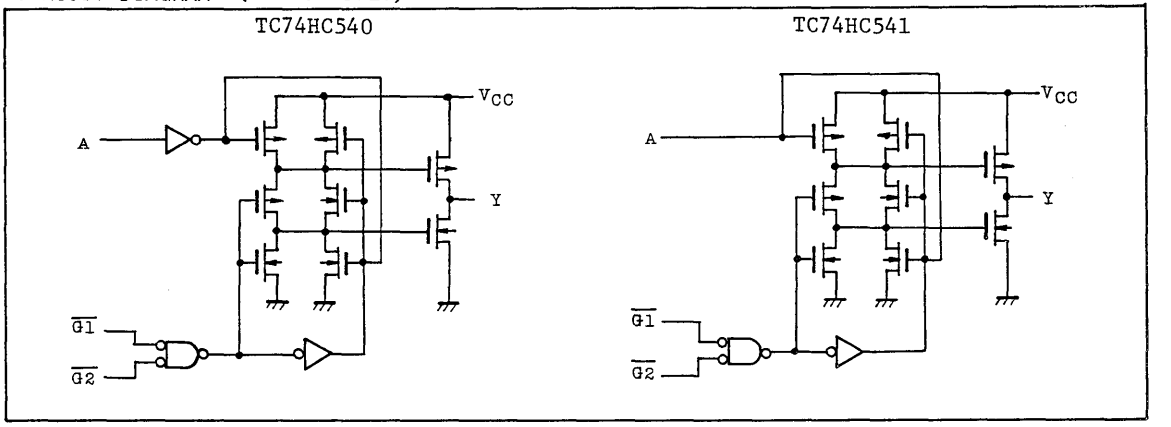
X: Don't Care

Z: High Impedance

*: Yn HC541
$\overline{Yn}$ HC540

TC74HC540P/F
TC74HC541P/F

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

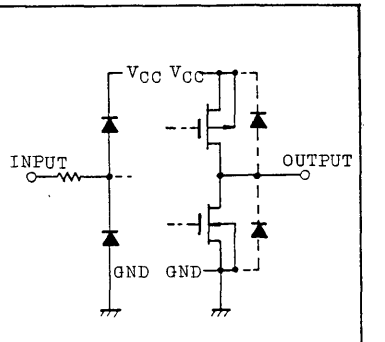
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-7.8mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=7.8mA$	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HC540	2.0	-	52	105	-	130	
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HC541	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	

TC74HC540P/F
TC74HC541P/F

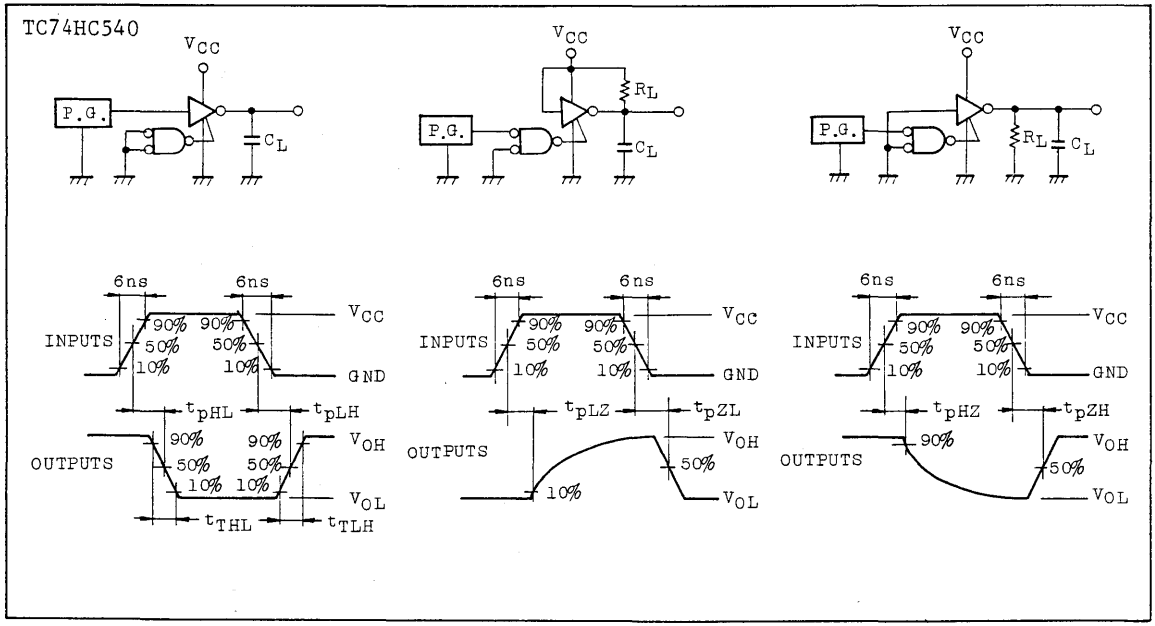
AC ELECTIRCAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Enable Time	t_{pLZ} t_{pZH}	R_L=1kΩ	2.0	-	72	145	-	180	ns
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	88	160	-	200	
			4.5	-	22	32	-	40	
			6.0	-	19	27	-	34	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC540		-	33	-	-	-	
		TC74HC541		-	36	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

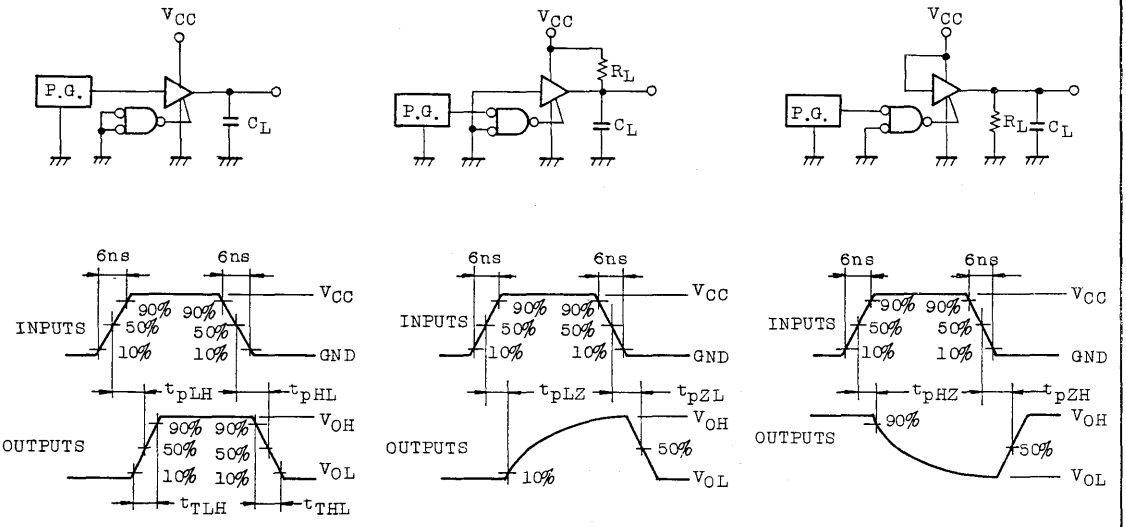
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM



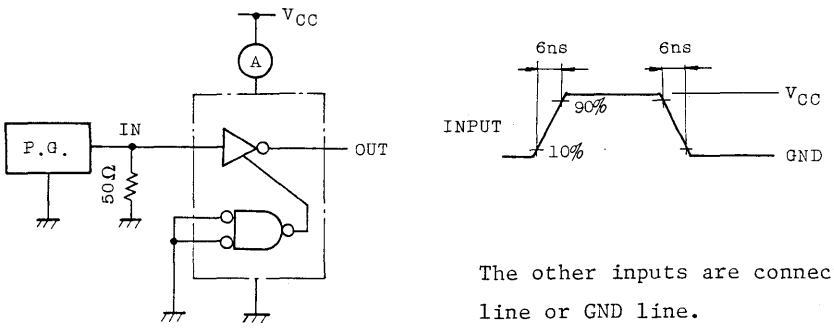
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM (Continued)

TC74HC541



$I_{CC(Opr.)}$ TEST CIRCUIT

TC74HC540



The other inputs are connected V_{CC} line or GND line.

Test circuit of the TC74HC541 is the same as this.

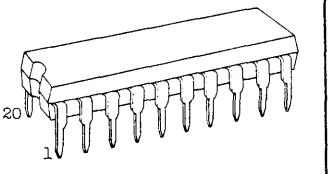
TC74HCT540P/F
TC74HCT541P/F

CMOS DIGITAL INTEGRATED CIRCUIT

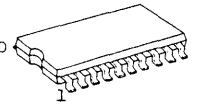
PRELIMINARY

TC74HCT540P/F OCTAL BUS BUFFER WITH INVERTED 3-STATE OUTPUTS
TC74HCT541P/F OCTAL BUS BUFFER WITH NONINVERTED 3-STATE OUTPUTS

The TC74HCT540 and TC74HCT541 are high speed CMOS OCTAL BUS BUFFER fabricated with silicon gate C^2MOS technology.
This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HCT540 is non-inverting type. The TC74HCT541 is inverting type. If either $\overline{G1}$ or $\overline{G2}$ are high, the terminal outputs are in the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP20(3D20A-P)



MFP20(F20GA-P)

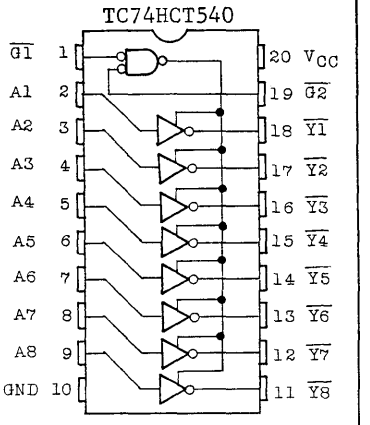
FEATURES:

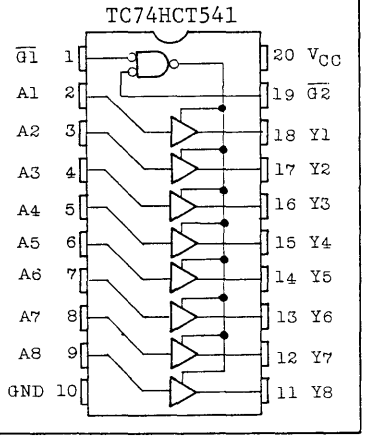
- High Speed ..... t_{pd}=13ns(T540) at V_{CC}=5V
  16ns(T541)
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS540/541

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

PIN ASSIGNMENT (TOP VIEW)





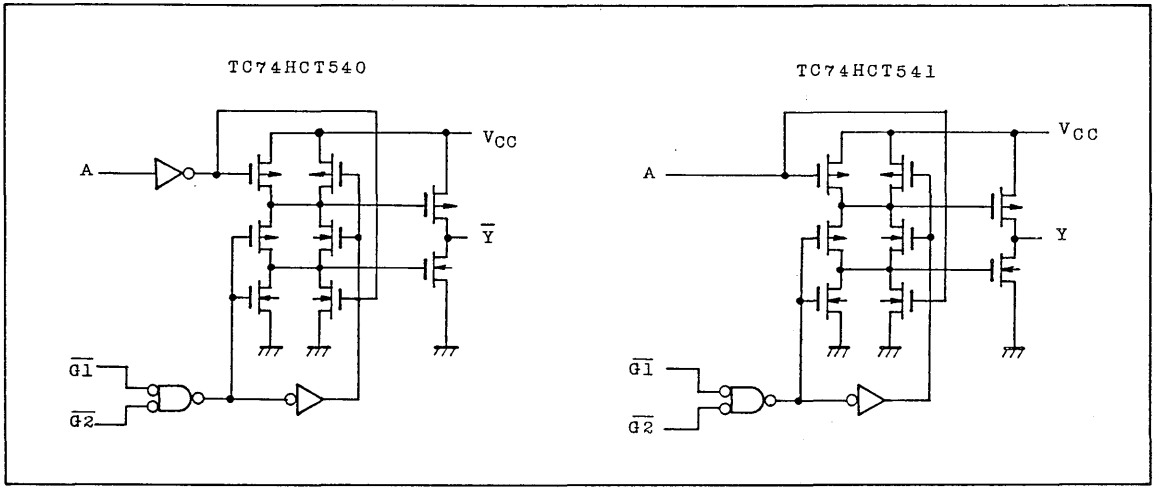
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{G1}$	$\overline{G2}$	An	Yn*	$\overline{Yn}$*
H	X	X	Z	Z
X	H	X	Z	Z
L	L	H	L	L
L	L	L	L	H

X: Don't Care
Z: High Impedance
*: Yn HCT541
$\overline{Yn}$ HCT540

TC74HCT540P/F
TC74HCT541P/F

CIRCUIT DIAGRAM (Per Circuit)



ABSOLUTE MAXIMUM RATINGS

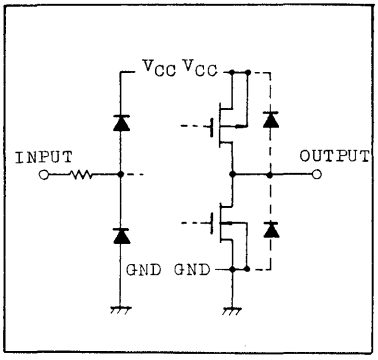
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HCT540P/F
TC74HCT541P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		5.5	-	-	4.0	-	40.0	
	I_C	Per Input: V_{IN}=2.4V or 0.5V Other Input: V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT540	4.5	-	16	26	-	32	
Propagation Delay Time	t_{pLH} t_{pHL}	TC74HCT541	4.5	-	19	30	-	36	
Output Enable Time	t_{pLZ} t_{pZH}	R_L=1kΩ	4.5	-	23	36	-	44	

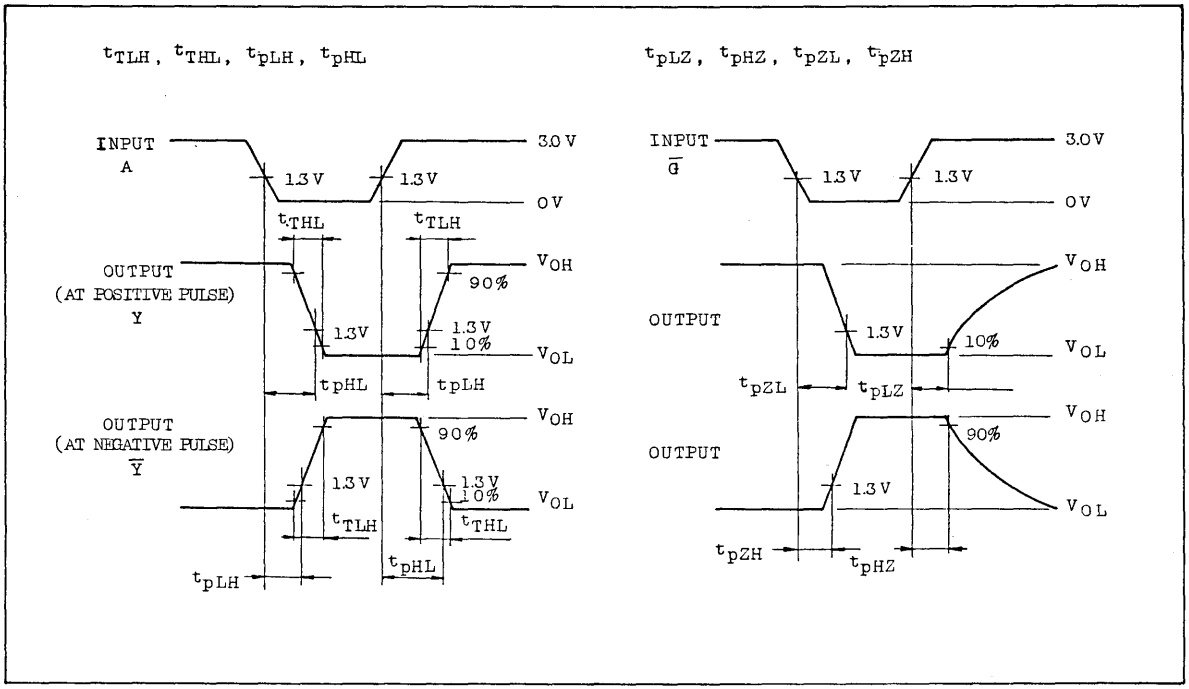
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	23	33	-	39	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT540		-	37	-	-	-	
		TC74HCT541		-	39	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Gate)}$$

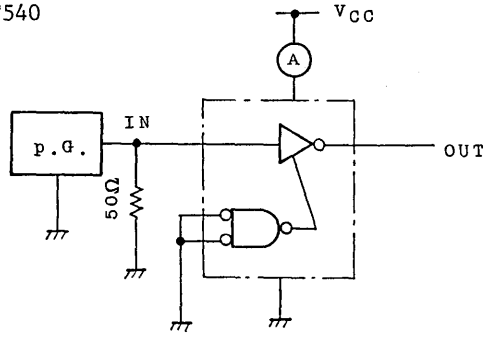
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM

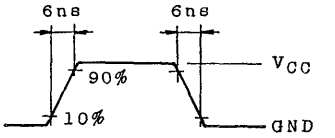


TC74HCT540P/F
TC74HCT541P/F

I_{CC}(Opr.) TEST CIRCUIT

TC74HCT540





The other inputs are connected V_{CC} line or GND line.

Test circuit of the TC74HCT541 is the same as this.

TC74HCT563P
TC74HCT573P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

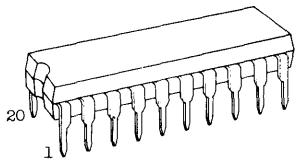
OCTAL D-TYPE LATCH WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT563P INVERTING
TC74HCT573P NON-INVERTING

The TC74HCT563 and TC74HCT573 are high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C²MOS technology.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These 8-bit D-type latches are controlled by a latch enable input(LE) and a output enable input($\overline{OE}$). While the LE input is held in high level, the Q outputs will follow the data input precisely or inversely. When the LE is take low, the Q outputs will be latched precisely or inversely at the logic level of D input data. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.
The application designer has a choice of combination of inverting and non-inverting outputs.
The three-state output configuration and the wide choice of outline will make the bus-organized system simple.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

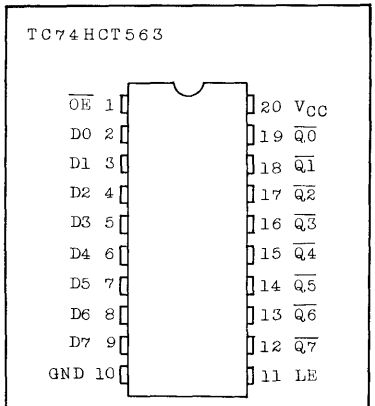
FEATURES:

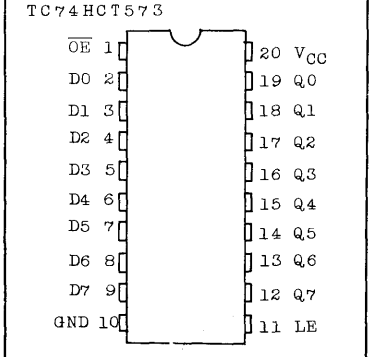
- High Speed ..... t_{pd}=20ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA
- Pin and Function Compatible with 74LS563/573



DIP20(3D20A-P)

PIN ASSIGNMENT (TOP VIEW)





TRUTH TABLE

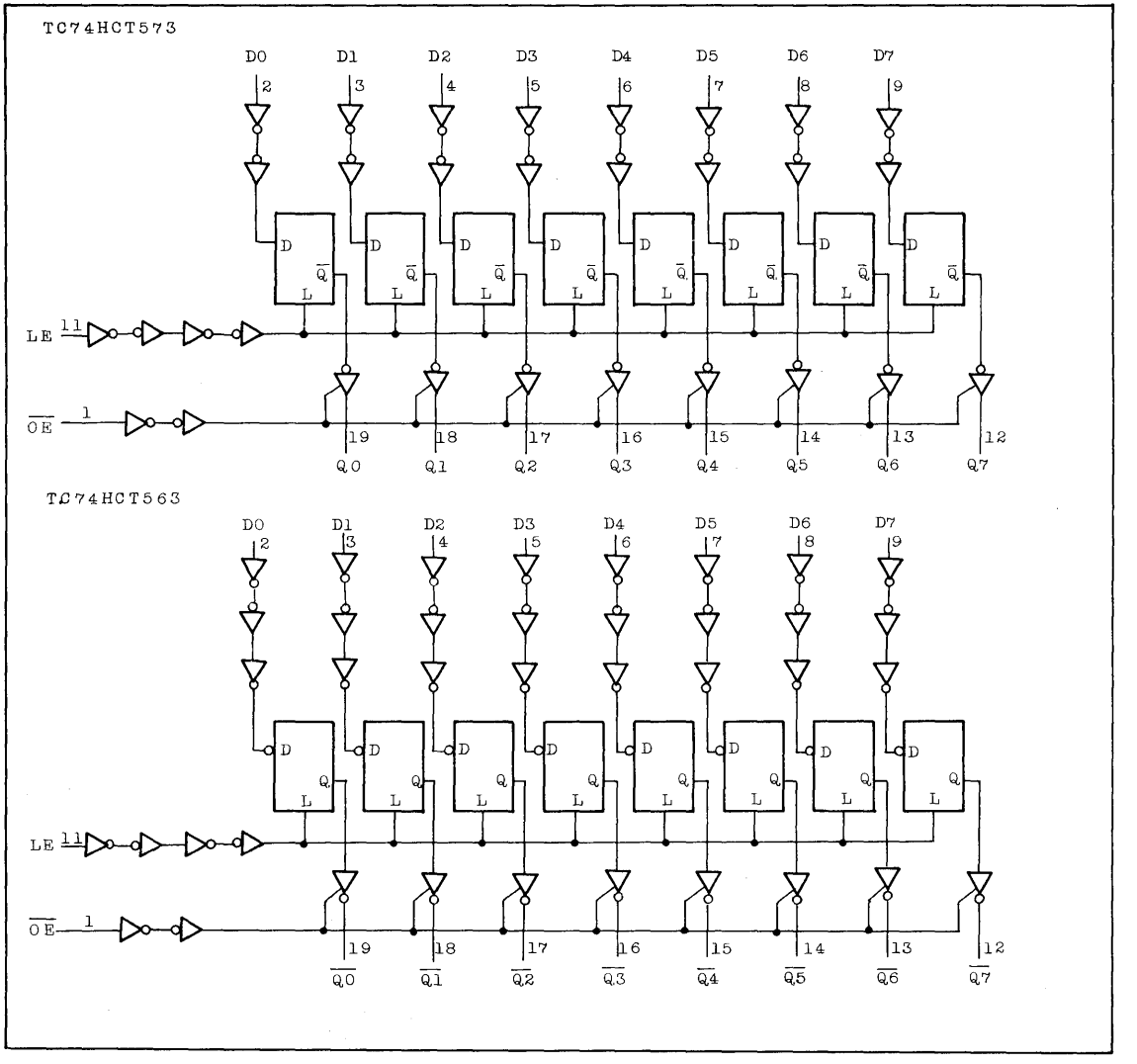
INPUTS			OUTPUTS	
$\overline{OE}$	LE	D	Q(HCT573)	$\overline{Q}$(HCT563)
H	X	X	HZ	HZ
L	L	X	Qn	$\overline{Qn}$
L	H	L	L	H
L	H	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE

Qn : Q/$\overline{Q}$ OUTPUTS ARE LATCHED AT THE TIME WHEN THE LE INPUT IS TAKEN LOW LOGIC LEVEL.

TC74HCT563P
TC74HCT573P

LOGIC DIAGRAM

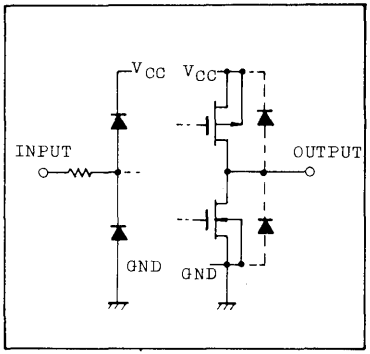


TC74HCT563P
TC74HCT573P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 500 (V_{CC}=4.5V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ~ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-		-		mA

TC74HCT563P
TC74HCT573P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	19	ns
Propagation Delay Time (LE - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	24	38	-	48	
Propagation Delay Time (D - Q, $\bar{Q}$)	t_{pLH} t_{pHL}		4.5	-	22	35	-	44	
Minimum Pulse Width (LE)	$t_{w(H)}$		4.5	-	8	15	-	19	
Minimum Set-up Time	t_s		4.5	-	2	10	-	13	
Minimum Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT563		-	41	-	-	-	
		TC74HCT573		-	41	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

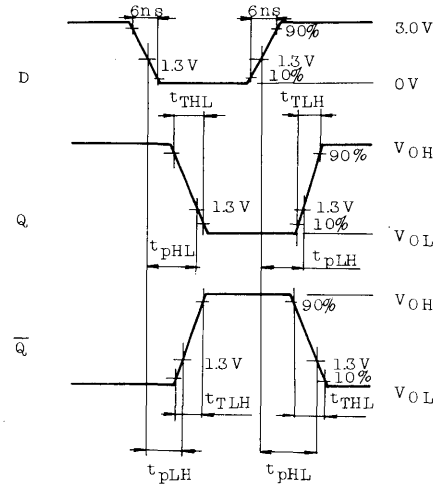
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Latch)}$$

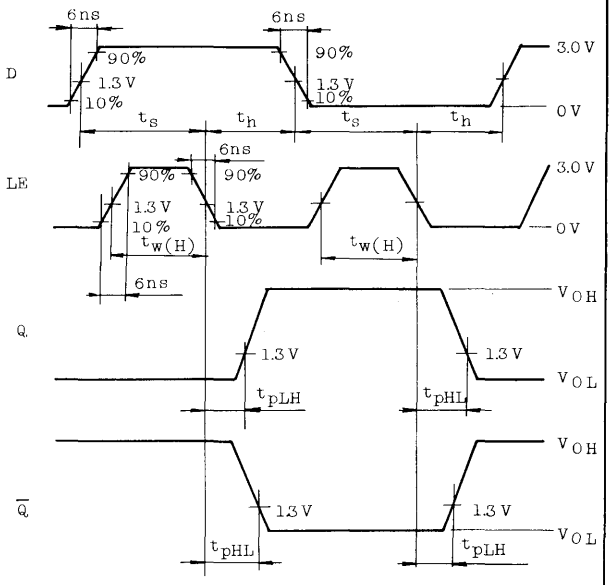
TC74HCT563P
TC74HCT573P

SWITCHING CHARACTERISTICS TEST WAVEFORM

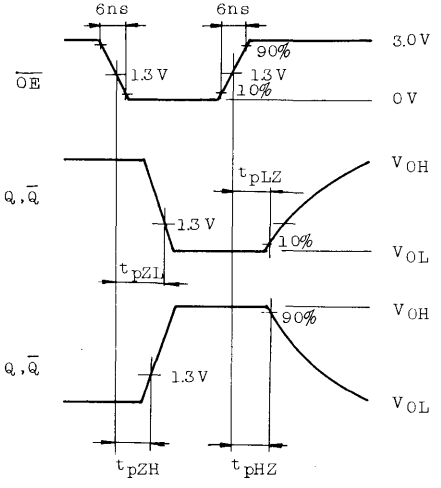
t_{TLH}, t_{THL}, t_{pLH}, t_{pHL}

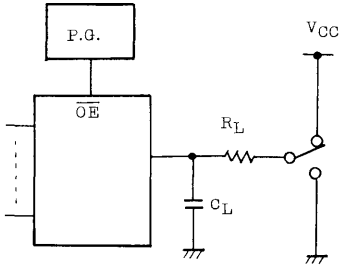


t_{pLH}, t_{pHL}(LE-Q, $\overline{Q}$), t_s, t_h, t_w



t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

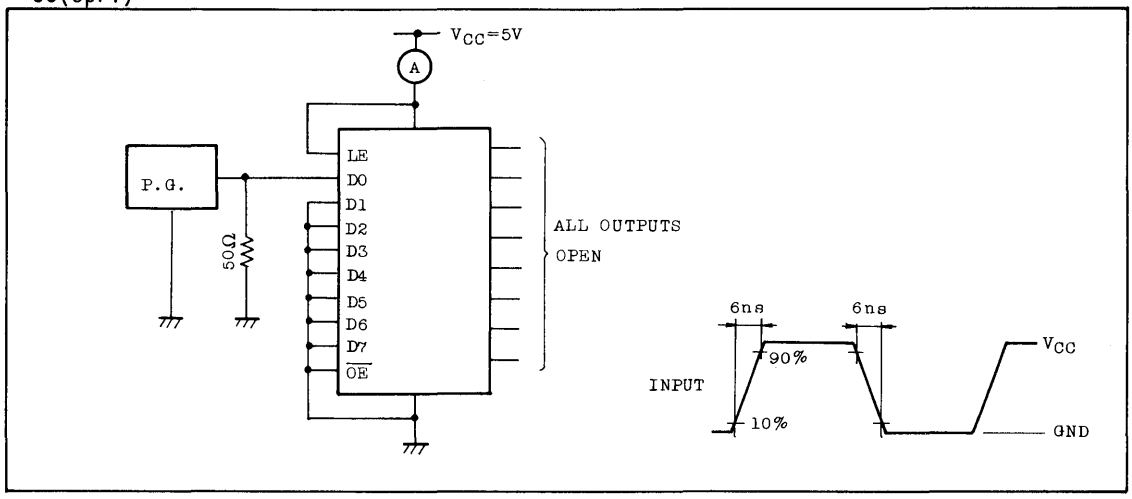




(NOTE)
EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TC74HCT563P
TC74HCT573P

$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HCT564P
TC74HCT574P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

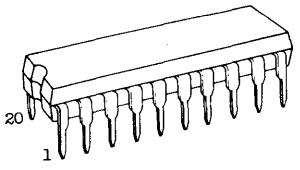
OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT (TTL INPUT LEVEL)

TC74HCT564P INVERTING
TC74HCT574P NON-INVERTING

The TC74HCT564 and TC74HCT574 are high speed CMOS OCTAL FLIP-FLOP with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology. These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels. These ICs achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These 8-bit D-type flip-flops are controlled by a clock input(CK) and a output enable input($\overline{OE}$). On the positive transition of clock, the Q outputs will be set precisely (HCT574) or inversely (HCT564) to the logic state that were setup at the D inputs. While the $\overline{OE}$ input is at low level, the eight outputs will be in a normal logic state (high or low logic level), and while high level, the outputs will be in a high impedance state. The output control does not affect the internal operation of flip-flops. That is, the old data can be retained or the new data can be entered even while the outputs are off. The application engineer has a choice of combination of inverting and non-inverting outputs. The 3-state output configuration and the wide choice of outline will make the bus-organized systems simple. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

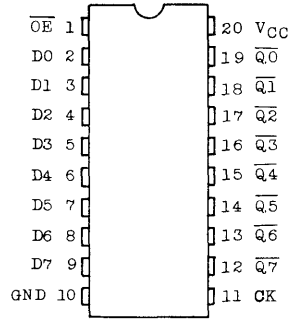
- High Speed ..... f_{MAX}=41MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation ..... I_{CC}=4μA(Max.)(Ta=25°C)
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=6mA(Min.)
- Pin and Function Compatible with 74LS564/574



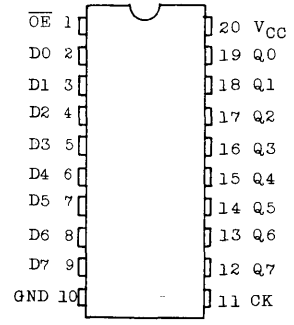
DIP20(3D20A-P)

PIN ASSIGNMENT (TOP VIEW)

TC74HCT564



TC74HCT574



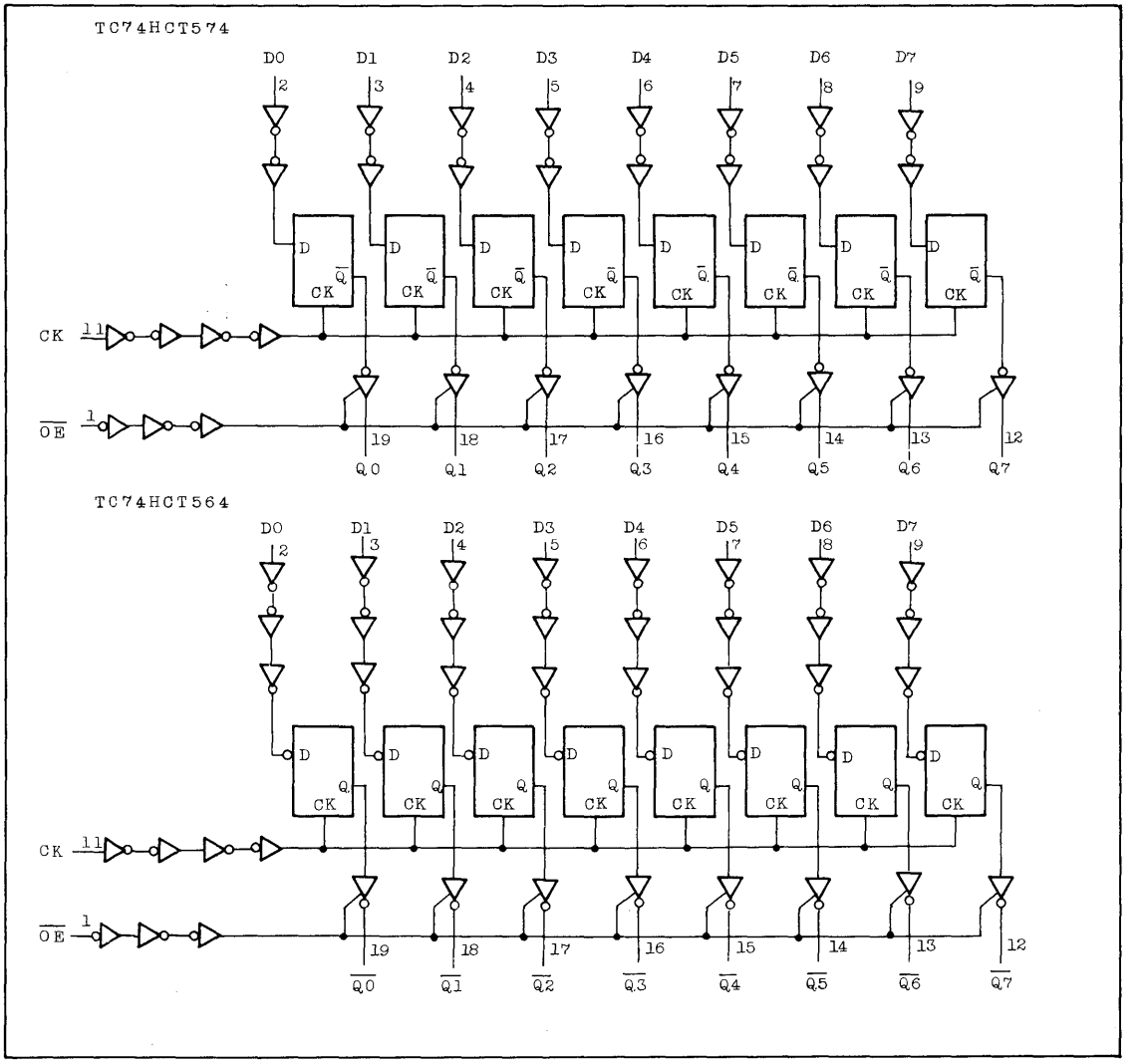
TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{OE}$	CK	D	Q(HCT574)	$\overline{Q}$(HCT564)
H	X	X	HZ	HZ
L	↑	X	Qn	$\overline{Qn}$
L	↓	L	L	H
L	↓	H	H	L

X : DON'T CARE
HZ : HIGH IMPEDANCE
Qn : NO CHANGE

TC74HCT564P
TC74HCT574P

LOGIC DIAGRAM

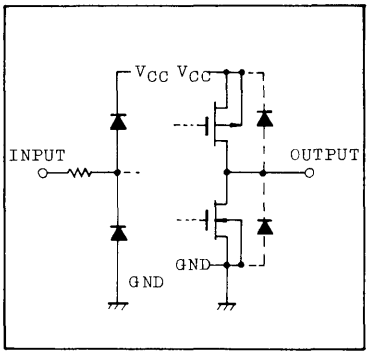


TC74HCT564P
TC74HCT574P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500(V_{CC}=4.5V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	V
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	4.0	-	40.0	μA
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND		5.5	-	-		-		mA

TC74HCT564P
TC74HCT574P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40∿85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		4.5	-	26	41	-	51	ns
Maximum Clock Frequency	f_{MAX}		4.5	22	38	-	18	-	MHz
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		4.5	-	8	15	-	19	ns
Minimum Set-up Time	t_s		4.5	-	1	10	-	13	ns
Minimum Hold Time	th		4.5	-	-	5	-	5	ns
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	18	35	-	44	ns
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	37	-	46	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	pF
Quiescent Supply Current	C_{PD}(1)	TC74HCT564		-	60	-	-	-	pF
		TC74HCT574		-	57	-	-	-	pF

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per Flip-Flop)}$$

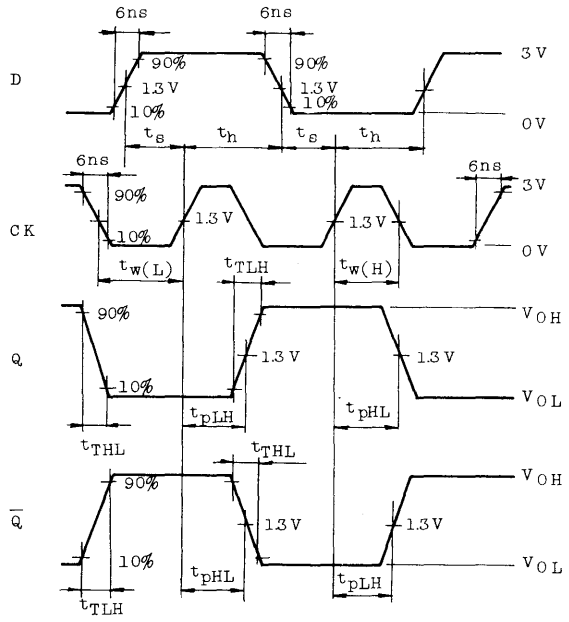
And the C_{PD} when N pcs of FLIP-FLOP operate, can be gained by the following equation.

$$C_{PD}(TOTAL)=40+20\times N \ [pF] \quad (TC74HCT564)$$
$$C_{PD}(TOTAL)=37+20\times N \ [pF] \quad (TC74HCT574)$$

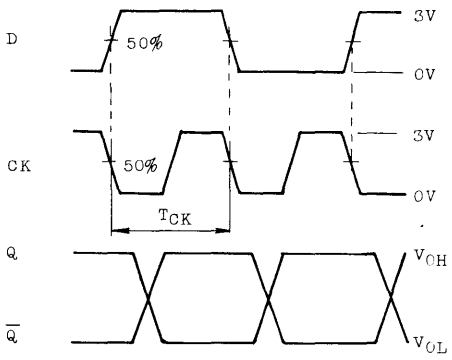
TC74HCT564P
TC74HCT574P

SWITCHING CHARACTERISTICS TEST WAVEFORM

t_{pLH}, t_{pHL}, t_s, t_h, t_w



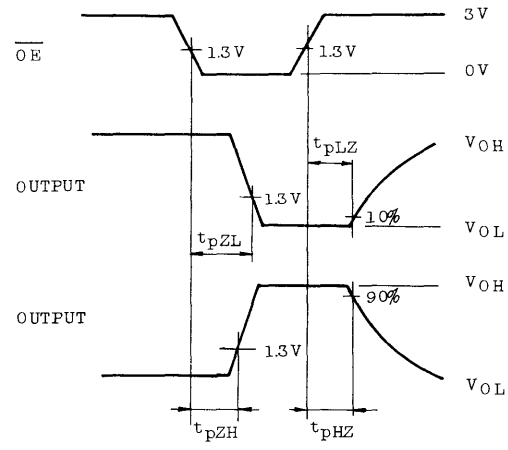
f_{MAX}.

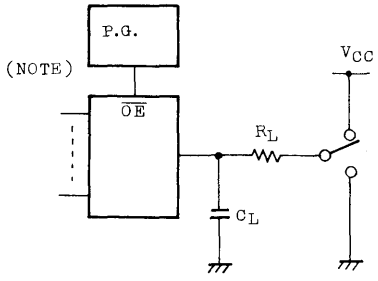


{CLOCK DUTY : 50%

$f_{MAX} = \frac{1}{T_{CK}}$

t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



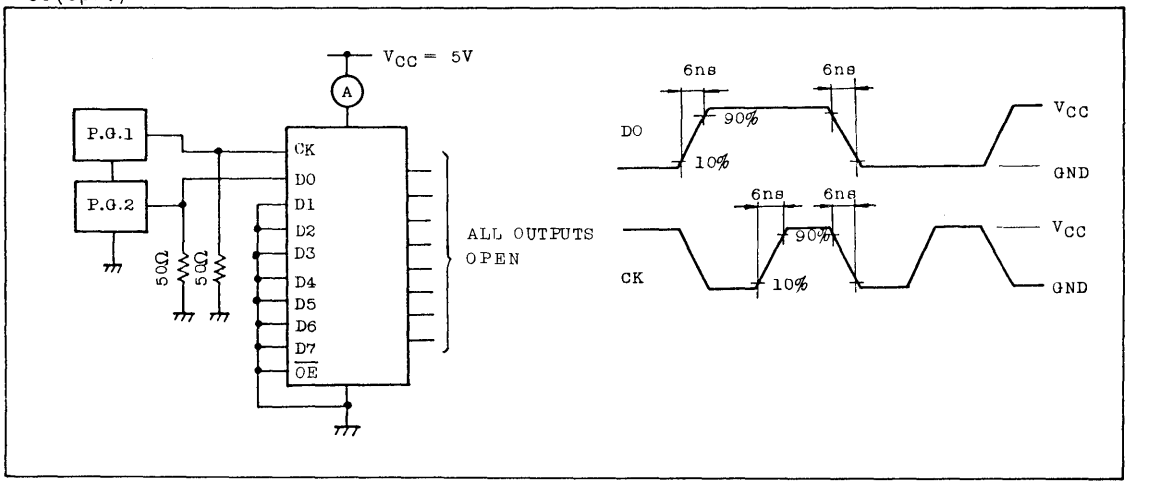


(NOTE)

EACH FLIP-FLOP SHALL BE SET HIGH WHEN SWITCH IS CONNECTED TO GND LINE AND IT SHALL BE SET LOW WHEN SWITCH IS CONNECTED TO V_{CC} LINE.

TC74HCT564P
TC74HCT574P

I_{CC}(Opr.) TEST CIRCUIT



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC595P

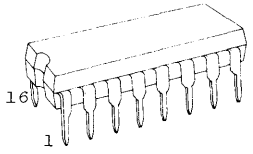
PRELIMINARY

TC74HC595P 8-BIT SHIFT REGISTER / LATCH (3-STATE)

The TC74HC595 is a high speed CMOS 8-BIT SHIFT REGISTER 1 LATCH fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. The TC74HC595P contains an 8-bit static shift register which feeds an 8-bit storage register. Shift operation is accomplished with the positive going transition of the SCK input. The output register is loaded with the contents of the shift register on the positive going transition of the RCK input. Since RCK and SCK signal are independently, parallel outputs can be held a stable data during the shift operation. And, since the parallel outputs have 3-state construction, it can be directly connnected to 8-bit busline. This register can be applied to serial-to-parallel conversion, data receivers, etc. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=55MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ... 15 LSTTL Loads For QA ∿ QH
  10 LSTTL Loads For QH'
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=6mA(Min.) For QA ∿ QH
  $|I_{OH}|=I_{OL}$=4mA(Min.) For QH'
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS595



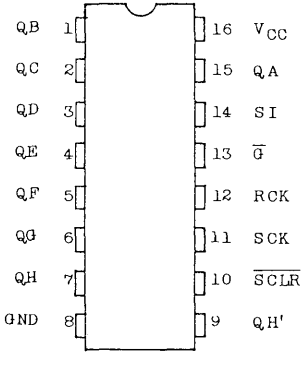
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current(QH')	I_{OUT}	±25	mA
DC Output Current(QA ∿ QH)	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{STG}	-65 ∿ 150	°C
Lead Temperature (10sec)	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

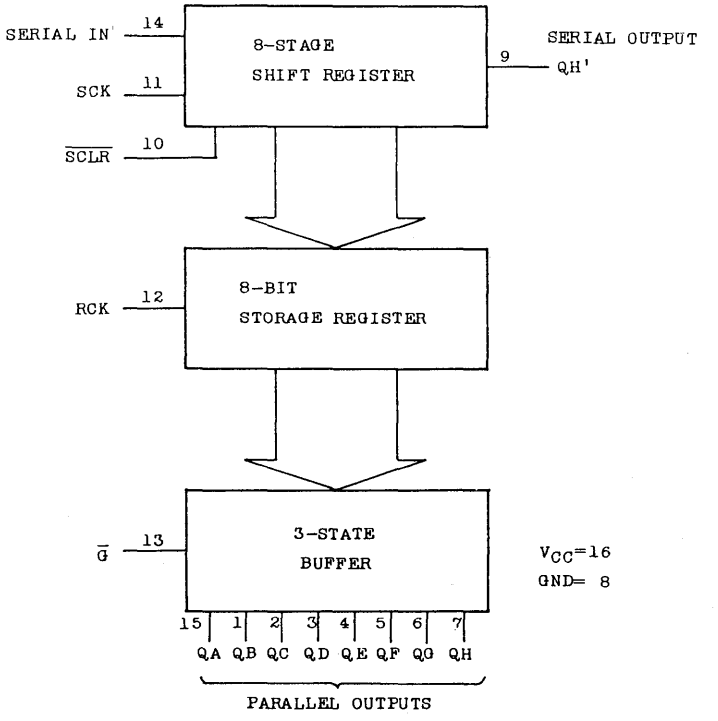
TC74HC595P

TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	RCK	$\overline{G}$	
X	X	X	X	H	QA thru QH outputs disable
X	X	X	X	L	QA thru QH outputs enable
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	X	X	State of S.R. is not changed.
X	X	X	↑	X	S.R. data is stored into storage register.
X	X	X	↓	X	Storage register state is not changed.

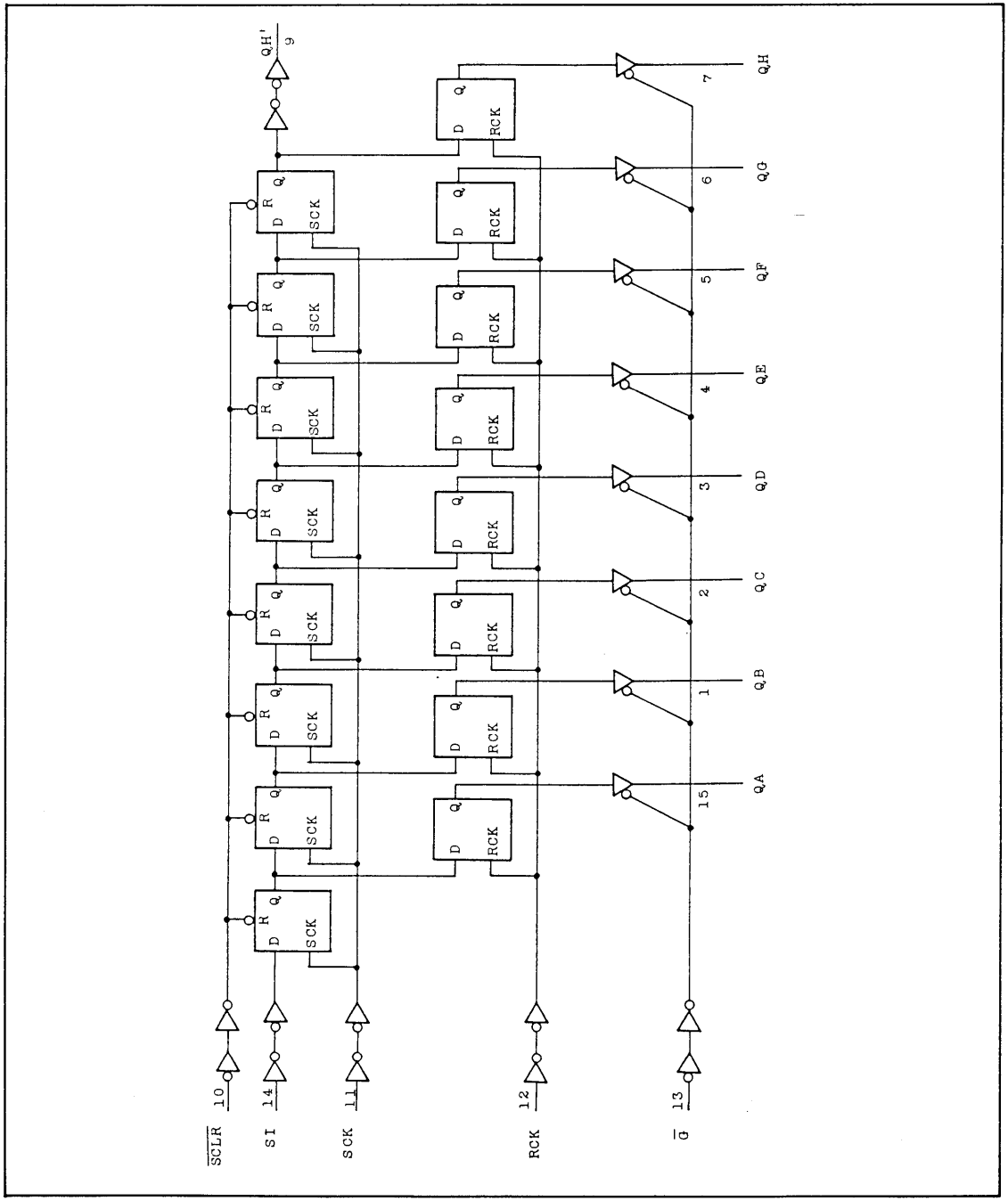
X : DON'T CARE

BLOCK DIAGRAM



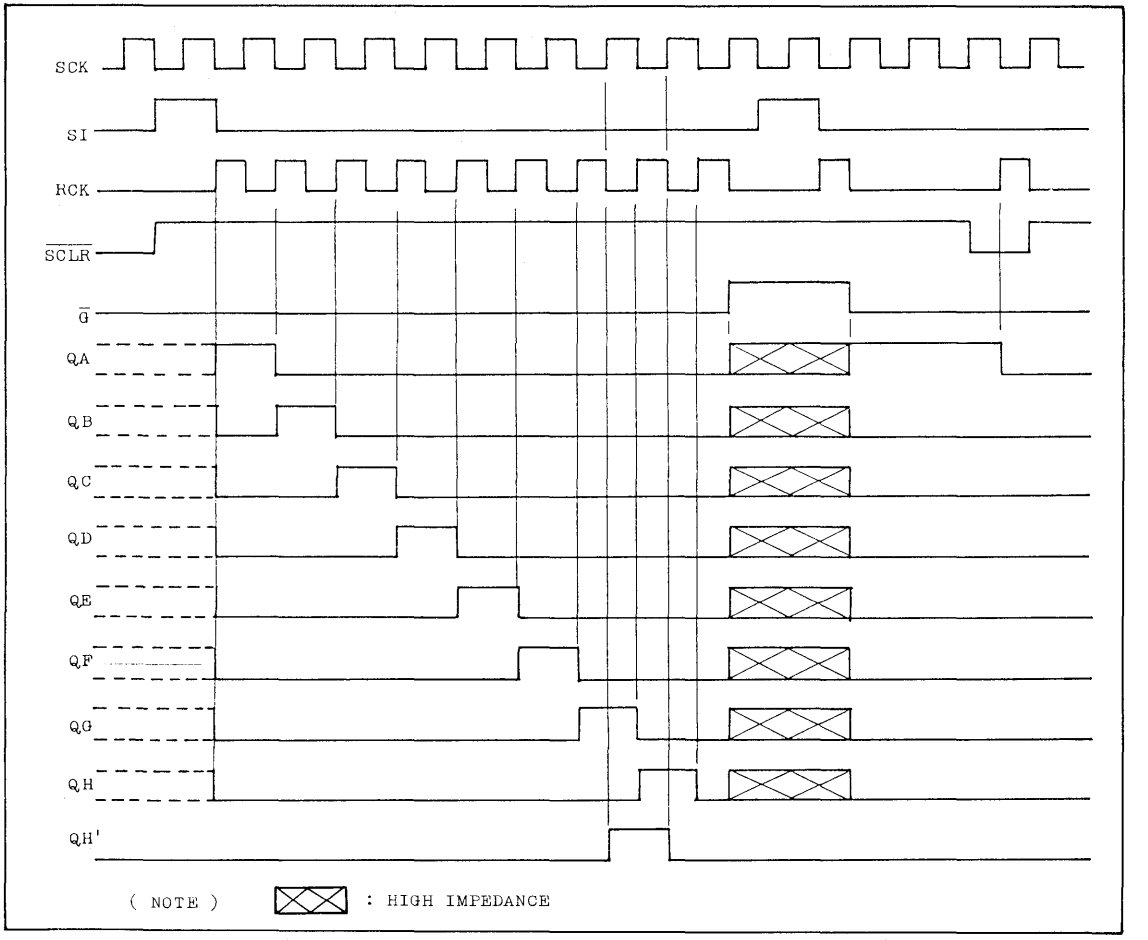
TC74HC595P

LOGIC DIAGRAM



TC74HC595P

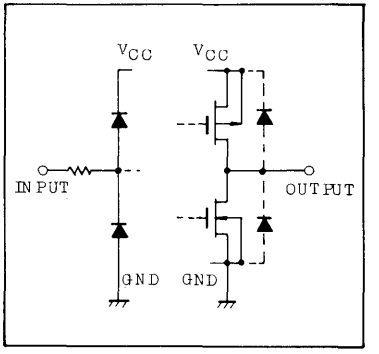
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC595P

DC ELECTRICAL CHARACTERITICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
		QA ∿ QH	I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
		QH'	I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
		QA ∿ QH	I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
		QH'	I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Bus Terminal 3-State Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time (Qn)	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0		6	10	-	13	
Output Transition Time (QH')	t_{TLH}		2.0	-	30	75	-	95	
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (SCK - QH')	t_{pLH}		2.0	-	80	160	-	200	
	t_{pHL}		4.5	-	20	32	-	40	
			6.0	-	17	27	-	34	

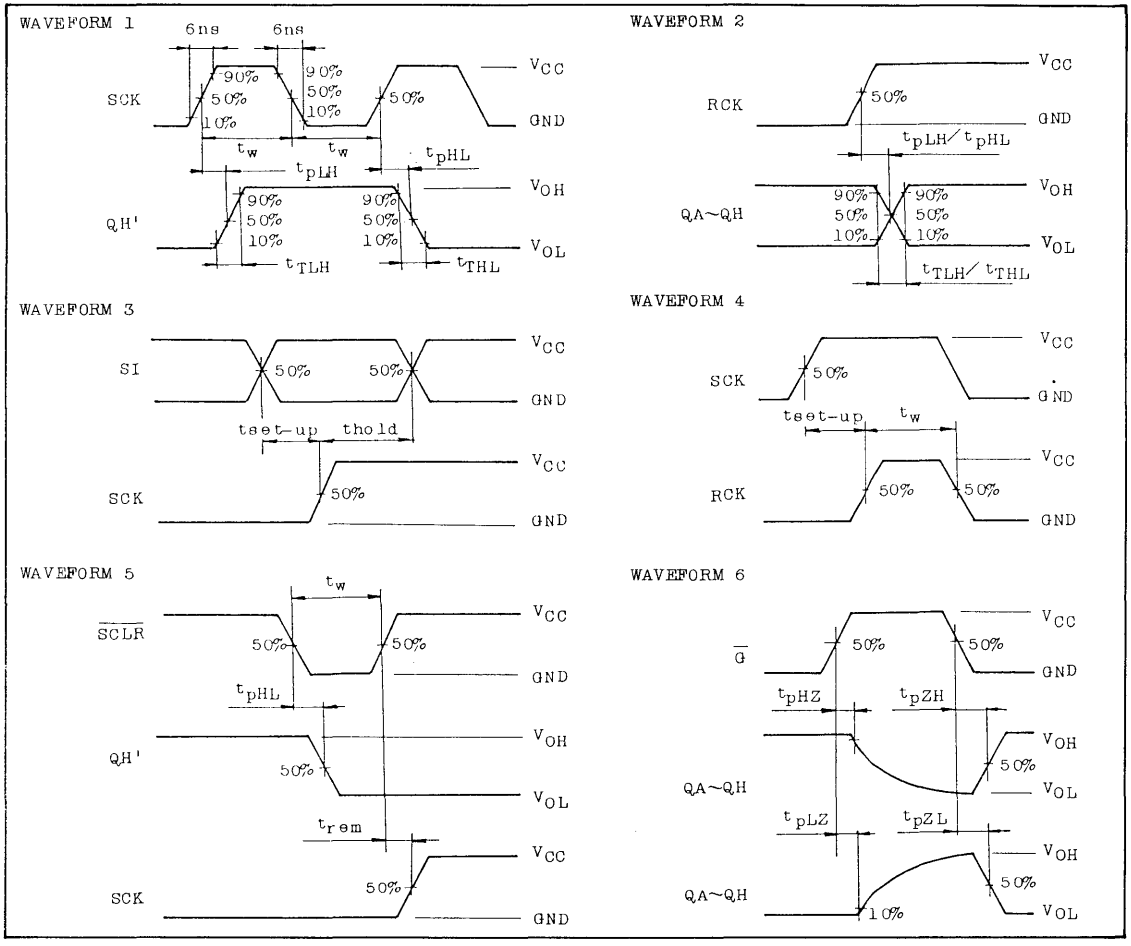
TC74HC595P

AC ELECTRICAL CHARACTERISTICS (Continued)

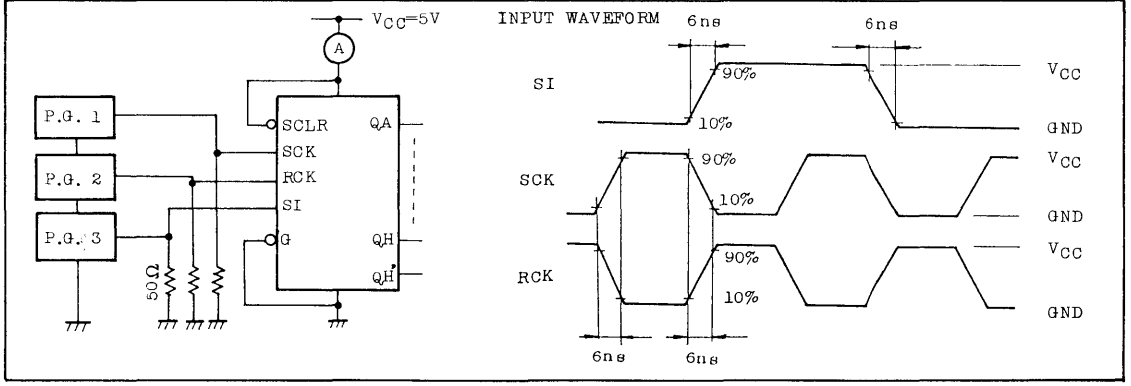
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{SCLR}$ - QH')	t_{pHL}		2.0	-	88	175	-	220	ns
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (RCK - Qn)	t_{pLH} t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Maximum Clock Frequency	f_{MAX}		2.0	6	12	-	5	-	MHz
			4.5	30	50	-	25	-	
			6.0	35	59	-	28	-	
Minimum Pulse Width (SCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	6	13	-	16	
Minimum Set-up Time (SI - SCK)	t_s		2.0	-	20	50	-	65	
			4.5	-	5	10	-	13	
			6.0	-	4	9	-	11	
Minimum Set-up Time (SCK - RCK)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Clear Removal Time	t_{rem}		2.0	-	10	50	-	65	
			4.5	-	2	10	-	13	
			6.0	-	2	9	-	11	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	68	135	-	170	
			4.5	-	17	27	-	34	
			6.0	-	14	23	-	29	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	64	150	-	190	
			4.5	-	21	30	-	38	
			6.0	-	18	26	-	33	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}			-	254	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST WAVEFORM



TC74HC597P/F C²MOS DIGITAL INTEGRATED CIRCUIT

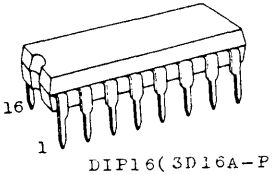
PRELIMINARY

TC74HC597P/F 8-BIT LATCH/SHIFT REGISTER

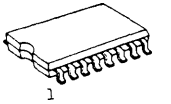
The TC74HC597 is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN SERIAL-OUT LATCH/SHIFT REGISTER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of an 8-bit data register feeding an 8-bit shift register.
The parallel data of A∿H inputs is stored in the input register on the positive going transition of RCK. When the $\overline{SLOAD}$ input is held low, the input register data is stored into shift register. When $\overline{SLOAD}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on the positive transition of SCK. A direct clear inputs sets 8-bit shift register to zero.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balnaced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V∿6V
- Pin and Function Compatible with 74LS597



DIP16(3D16A-P)



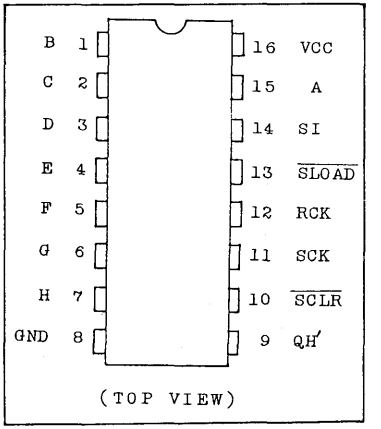
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	Tstg	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

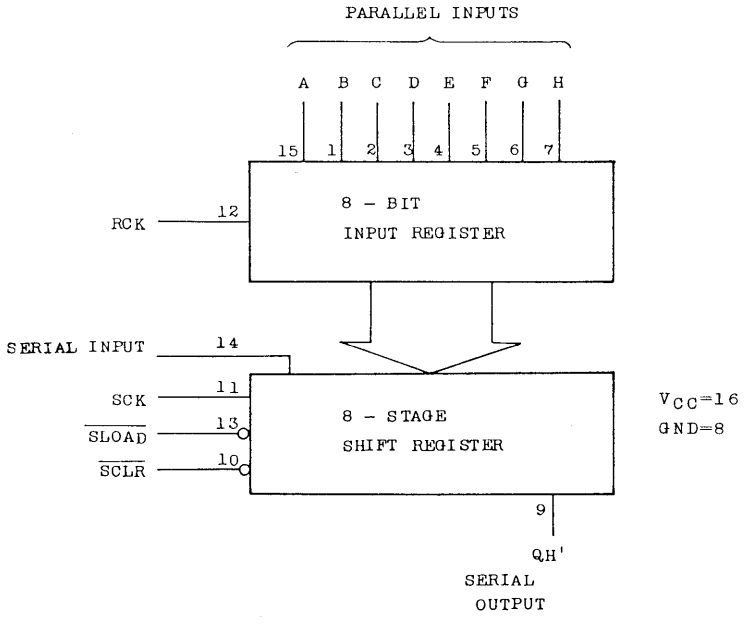
TC74HC597P/F

TRUTH TABLE

INPUTS					FUNCTION
SI	SCK	$\overline{SCLR}$	$\overline{SLOAD}$	RCK	
X	X	L	H	X	S.R. is cleared to "L"
X	X	H	L	X	Input register data is stored into S.R.
L	↑	H	H	X	First stage of S.R. becomes "L". Other stages store the data of previous stage, respectively.
H	↑	H	H	X	First stage of S.R. becomes "H". Other stages store the data of previous stage, respectively.
X	↓	H	H	X	State of S.R. is not changed.
X	X	X	X	↑	Input data on A~H line is stored into input register
X	X	X	X	↓	Storage register state is not changed.

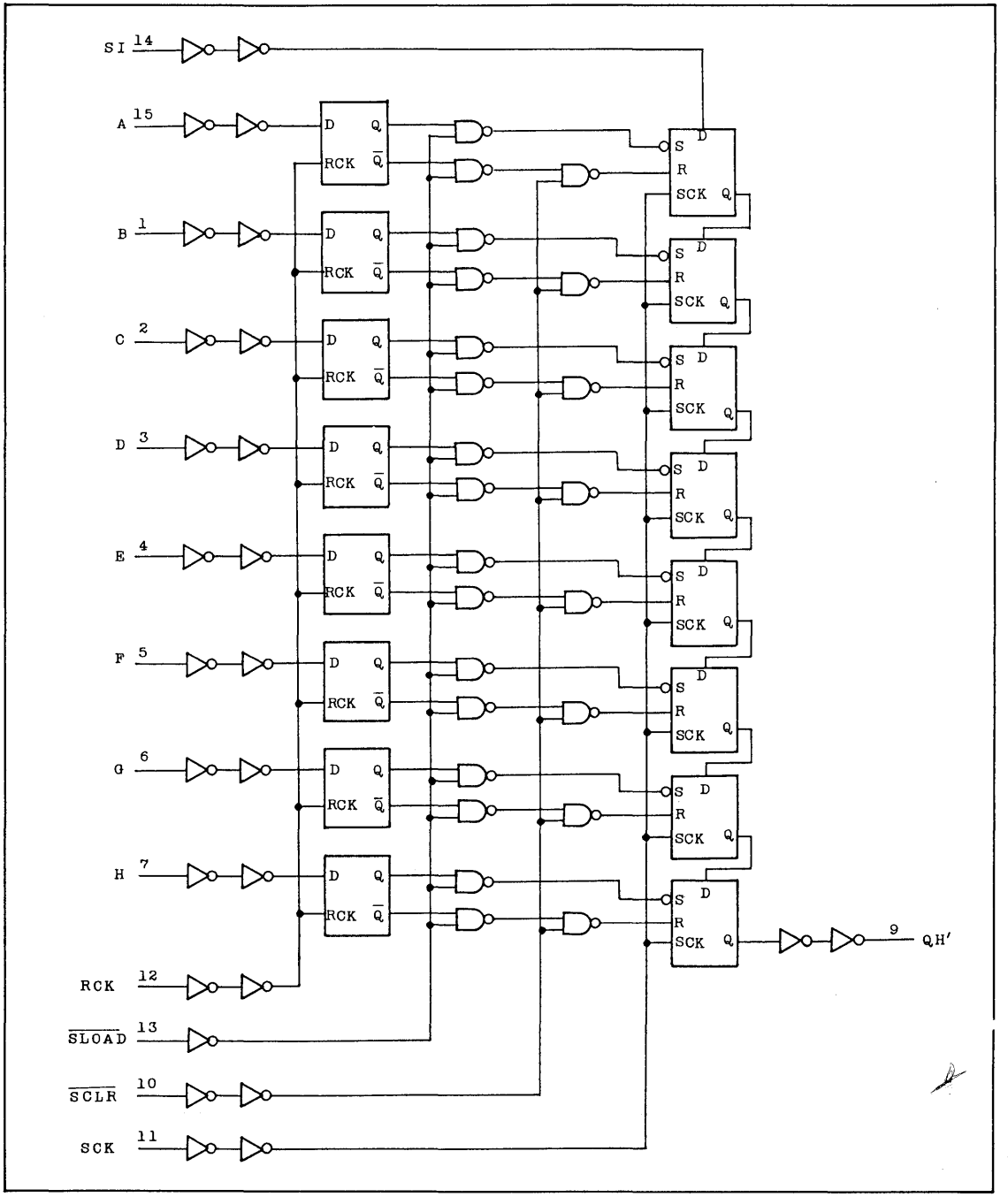
X; Don't Care

BLOCK DIAGRAM



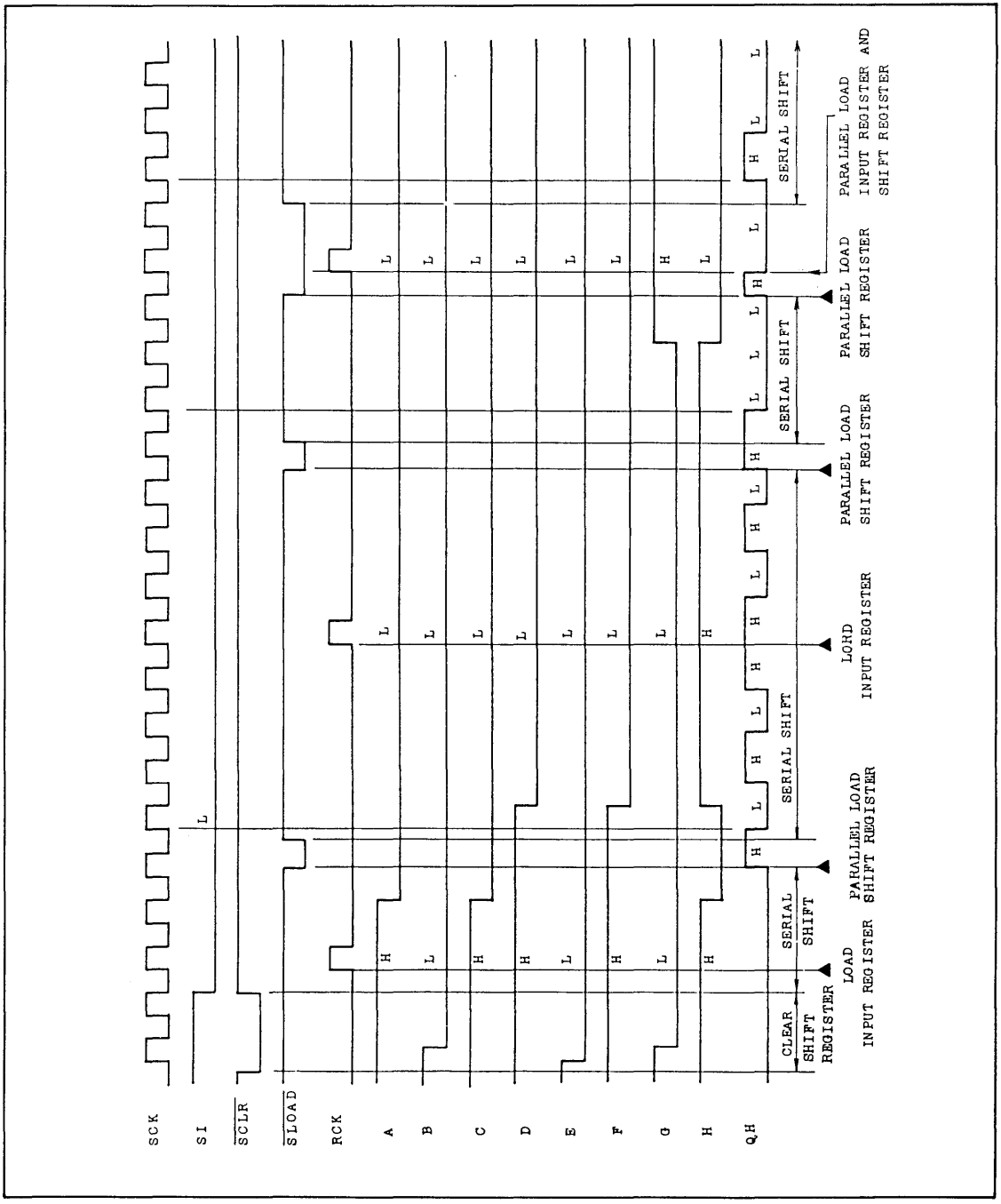
TC74HC597P/F

LOGIC DIAGRAM



TC74HC597P/F

TIMING CHART

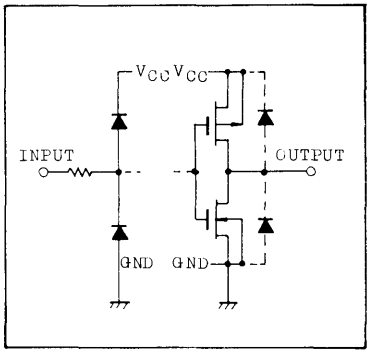


TC74HC597P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC597P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (SCK - QH')	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time ($\overline{SCLR}$ - QH')	t_{pHL}		2.0	-	92	175	-	220	
			4.5	-	23	35	-	44	
			6.0	-	20	30	-	37	
Propagation Delay Time ($\overline{SLOAD}$ - QH')	t_{pHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Propagation Delay Time (RCK - QH')	t_{pLH} t_{pHL}	$\overline{SLOAD}$="L"	2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width (SCK, RCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SCLR}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{SLOAD}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (RCK - $\overline{SLOAD}$)	t_s		2.0	-	50	125	-	155	
			4.5	-	13	25	-	31	
			6.0	-	11	21	-	26	
Minimum Set-up Time (SI - SCK)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set-up Time (A ... H - RCK)	t_s		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{SCLR}$, $\overline{SLOAD}$)	t_{rem}		2.0	-	10	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	

TC74HC597P/F

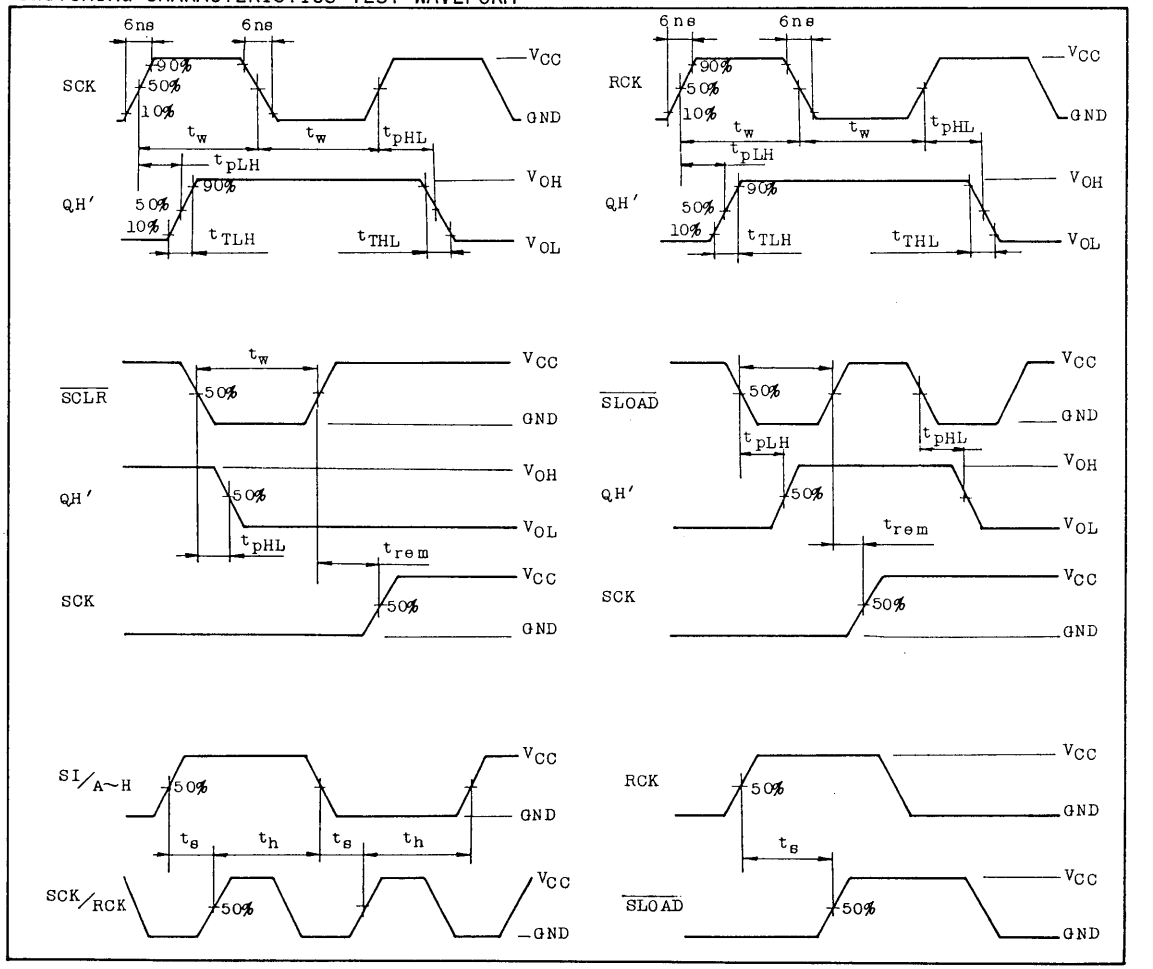
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	76	-	-	-	

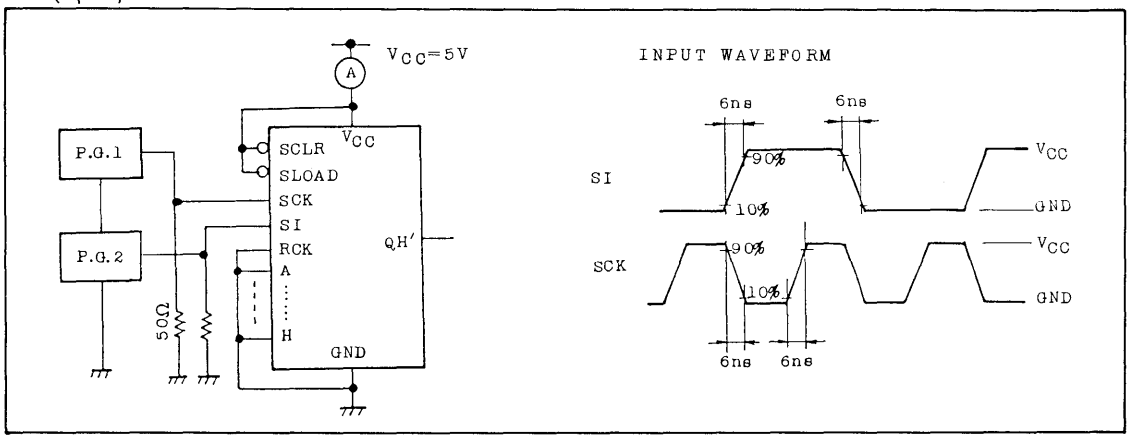
Note 1 C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



I_{CC}(Opr.) TEST CIRCUIT



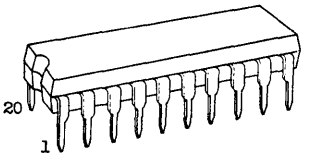
TC74HC620P
TC74HC623P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

OCTAL BUS TRANCEIVER
TC74HC620P 3-STATE, INVERTING
TC74HC623P 3-STATE, NON-INVERTING

The TC74HC620 and TC74HC623 are high speed CMOS QUAD TRANSCEIVER fabricated with silicon gate C^2MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These IC's are intended for two-way asynchronous communication between data buses, and direction of data transmission is determined by GAB, $\overline{GBA}$, GAB and $\overline{GBA}$ inputs are equipped with protection circuits against static discharge or transient excess voltage.



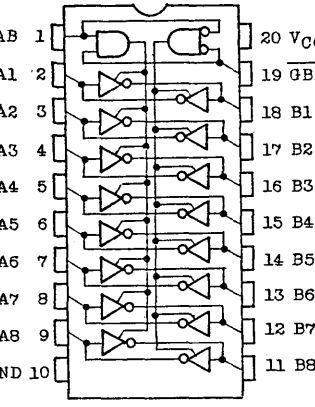
DIP20(3D20A-P)

FEATURES:

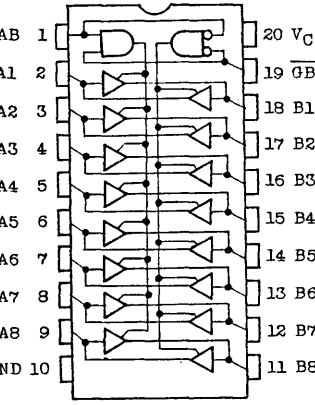
- High Speed ..... t_{pd}=10ns[620], t_{dp}=8ns[623] (Typ.) at V_{CC}=5V
- Low Power Disspation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance ..$|I_{OH}|=I_{OL}$=6mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 74LS620/623

PIN ASSIGNMENT (TOP VIEW)

TC74HC620



TC74HC623



NOTICE FOR APPLICATION

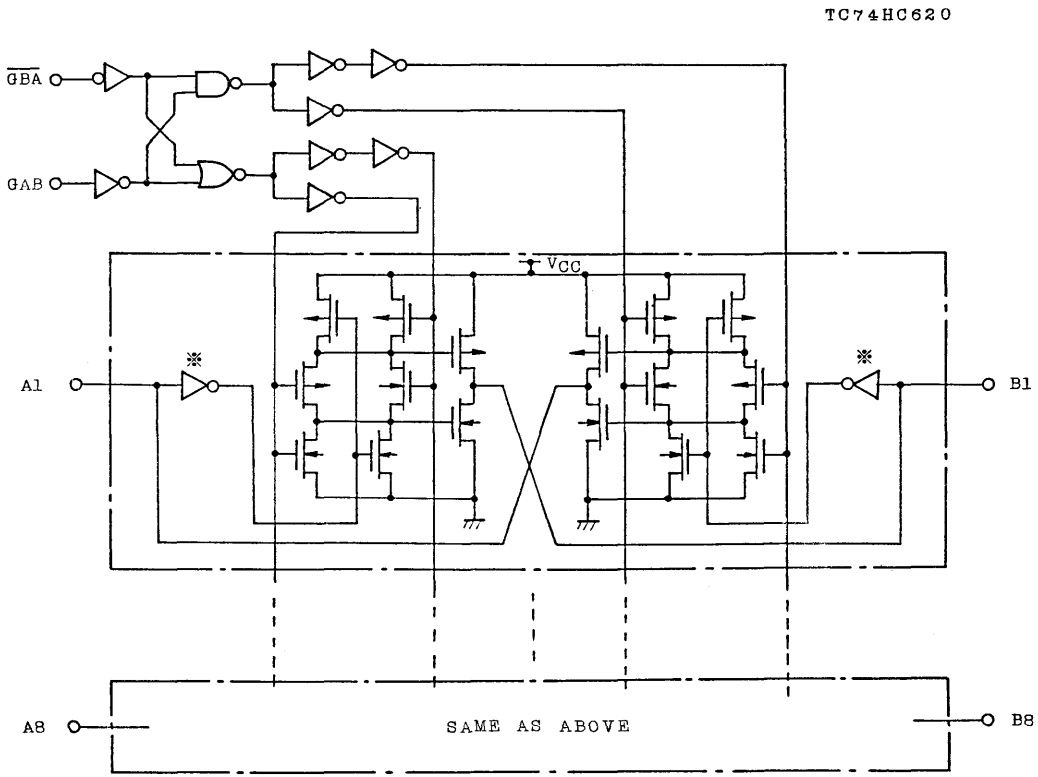
It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TC74HC620P
TC74HC623P

TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS	
GAB	$\overline{GBA}$	A Bus	B Bus	HC620	HC623
L	L	Output	Input	$A = \overline{B}$	A = B
H	H	Input	Output	$B = \overline{A}$	B = A
L	H	High Impedance		Z	Z
H	L	High Impedance		Z	Z

LOGIC DIAGRAM



Note: In case of TC74HC623, input inverters marked ※ at A bus and B bus are eliminated respectively.

TC74HC620P
TC74HC623P

ABSOLUTE MAXIMUM RATINGS

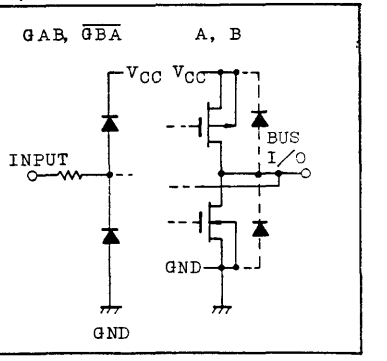
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
Bus Terminal Voltage	$V_{I/O}$	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Bus Terminal Voltage	$V_{I/O}$	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

TC74HC620P
TC74HC623P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Bus Terminal 3-State Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL}, $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Lekage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND *		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to GAB, $\overline{GBA}$ input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	11	-	13	
Propagation Delay Time *	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Propagation Dealy Time **	t_{pLH} t_{pHL}		2.0	-	40	85	-	105	
			4.5	-	10	17	-	21	
			6.0	-	9	14	-	18	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	74	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	10	26	-	33	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	100	180	-	225	
			4.5	-	25	36	-	45	
			6.0	-	21	31	-	38	
Input Capacitance	C_{IN}	GAB, $\overline{GBA}$		-	5	10	-	10	pF
Bus Terminal Input Capacitance	$C_{I/O}$	An, Bn		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HC620		-	40	-	-	-	
		TC74HC623		-	35	-	-	-	

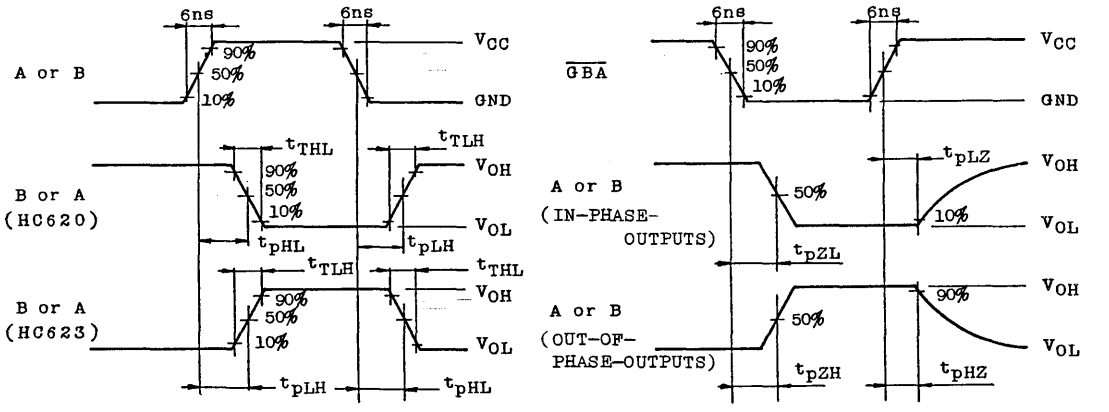
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN}$$

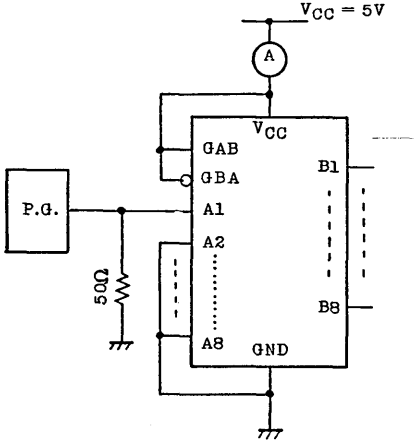
(2) * TC74HC620 ** TC74HC623

TC74HC620P
TC74HC623P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(Opr.)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(Opr.)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

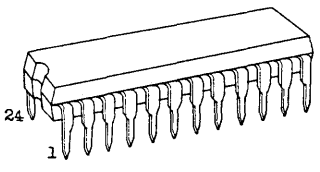
TC74HC646P
TC74HC648P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

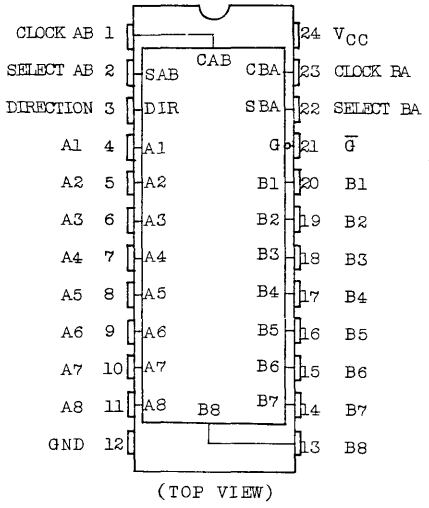
TC74HC646P OCTAL BUS TRANSCEIVER/REGISTER
TC74HC648P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)

The TC74HC646/648 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C²MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are bus tranceiver with 3-state outputs, D type flip-flops, and control circuitry arranged for multiplexed transmission of data directrly from the input bus or from the internal registers. If DIR input is held "H", A1 thru 8 become inputs and B1 thru 8 become outputs. If DIR input is held "L", A1 thru 8 become outputs.
Enable input $\overline{G}$ is held "H", both of A bus and B bus become high impedance.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of internal flip-flops. These flip-flops change state state on positive going transition of the clock pulse (CAB, CBA).
The TC74HC646 is non-inverting output type while the TC74HC648 is inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance .$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS646/648

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

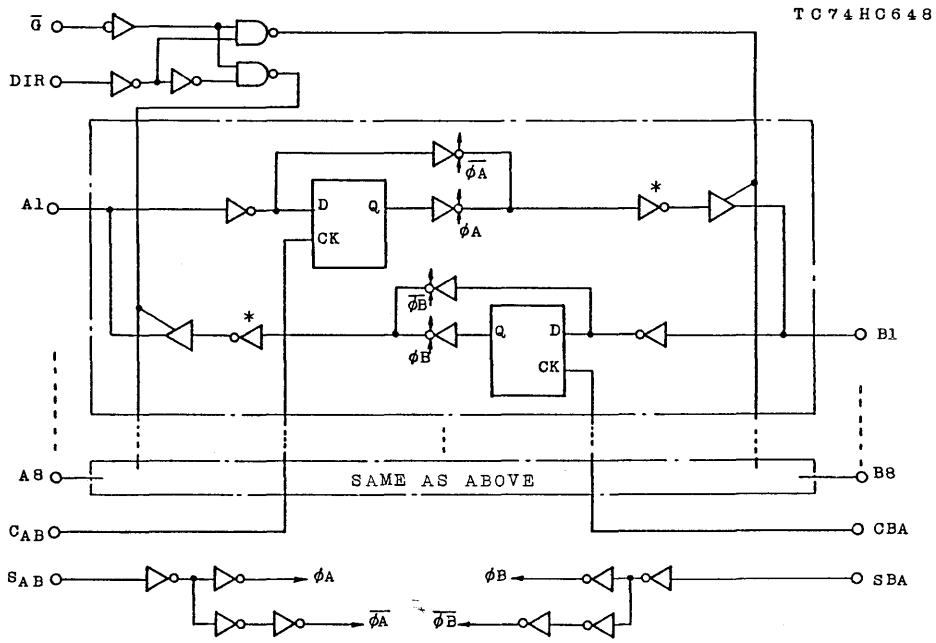
TC74HC646 (The truth table for TC74HC648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the A bus displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
L	L					OUTPUTS	INPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the B bus.
		X*	↓	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

Note: X; Don't Care
Qn; The data stored to the internal flip-flops by most recent low to high transition of the clock inputs.
Z; High Impedance
* The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

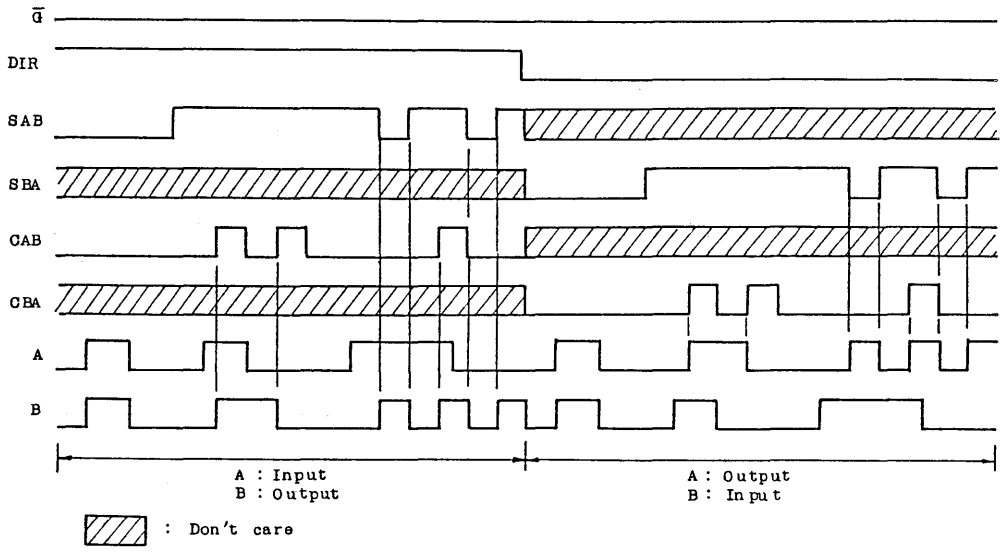
TC74HC646P
TC74HC648P

LOGIC DIAGRAM



Note: In case of TC74HC646 output inverter maked ※ at A bus and B bus are eliminated.

TIMING CHART



TC74HC646P
TC74HC648P

ABSOLUTE MAXIMUM RATINGS

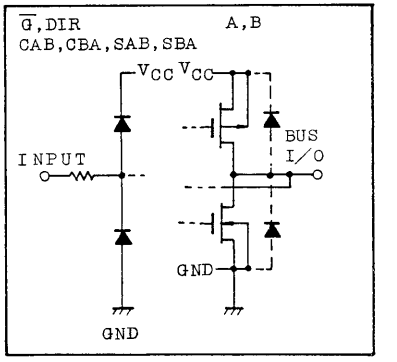
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
Bus Terminal Voltage	$V_{I/O}$	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 00mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Bus Terminal Voltage	$V_{I/O}$	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	25	60	-	75	ns
	t_{THL}		4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (BUS - BUS)	t_{pLH}		2.0	-	92	180	-	225	
	t_{pHL}		4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - BUS)	t_{pLH}		2.0	-	124	240	-	300	
	t_{pHL}		4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (SELECT - BUS)	t_{pLH}		2.0	-	112	220	-	275	
	t_{pHL}		4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	30	75	-	95	
	$t_{w(L)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Data Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	

TC74HC646P
TC74HC648P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40 85°C MIN.	Ta=-40 85°C MAX.	UNIT
3-State Output Enable Time ($\overline{G}$, DIR)	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	104	205	-	250	ns
			4.5	-	26	41	-	50	
			6.0	-	22	35	-	43	
3-State Output Disable Time ($\overline{G}$, DIR)	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	104	210	-	250	
			4.5	-	29	42	-	50	
			6.0	-	25	36	-	43	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

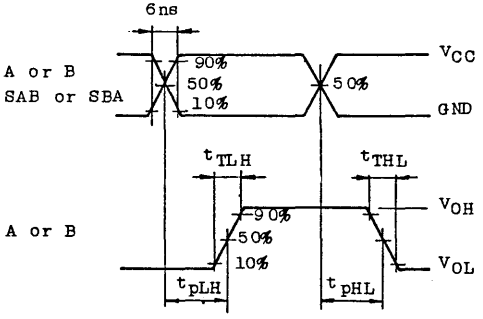
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

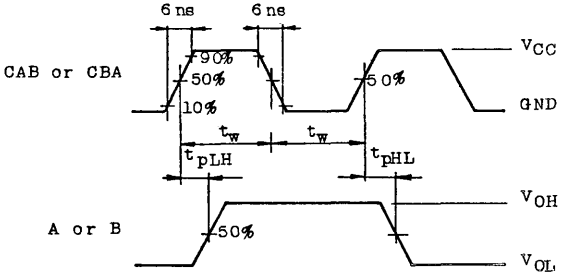
TC74HC646P
TC74HC648P

SWITCHING CHARACTERISTICS TEST WAVEFORM

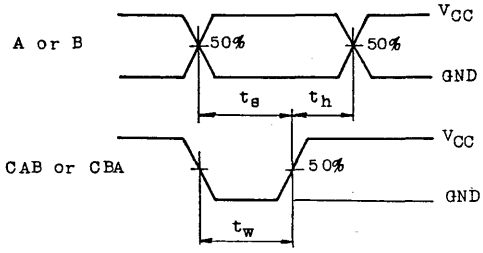
WAVEFORM 1



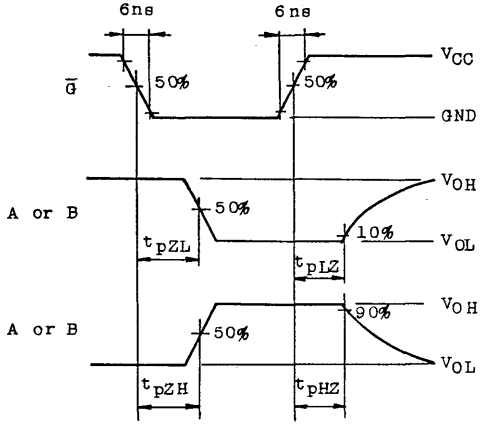
WAVEFORM 2



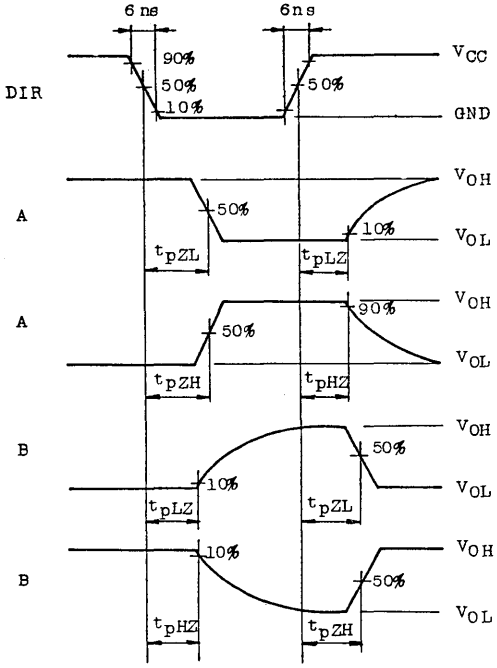
WAVEFORM 3



WAVEFORM 4

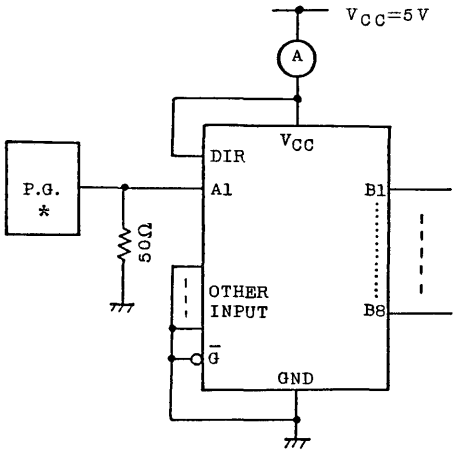


WAVEFORM 5



TC74HC646P
TC74HC648P

I_{CC}(Opr.) TEST CIRCUIT



* Input transition time is the same as that in case of switching characteristics test.

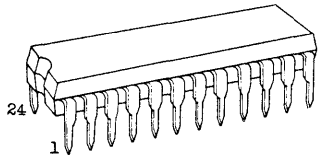
TC74HCT646P
TC74HCT648P

CMOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

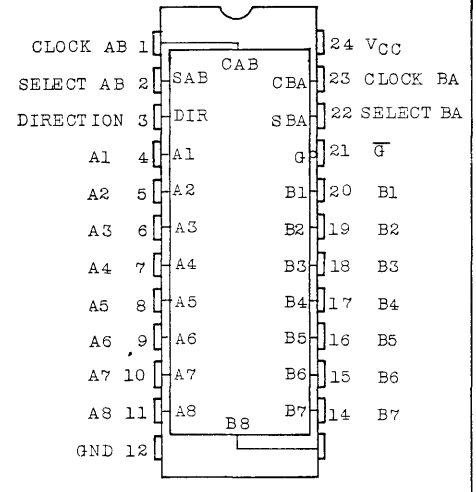
TC74HCT646P OCTAL BUS TRANSCEIVER/REGISTER
TC74HCT648P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)

The TC74HCT646/648 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These devices are bus tranceiver with 3-stete outputs, D type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If DIR input is held "H", A1 thru 8 become inputs and B1 thru 8 become outputs. If DIR input is held "L", A1 thru 8 become outputs.
Enable input $\overline{G}$ is held "H", both of A bus and B bus become high impedance.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of internal flip-flops. These flip-flops change state on positive going transition of the clock pulse (CAB, CBA).
The TC74HCT646 is non-inverting output type while the TC74HCT648 is inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.. I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL output ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability .....15 LSTTL Loads
- Symmetrical Output Impedance .$|I_{OH}|$=I_{OL}=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS646/648

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

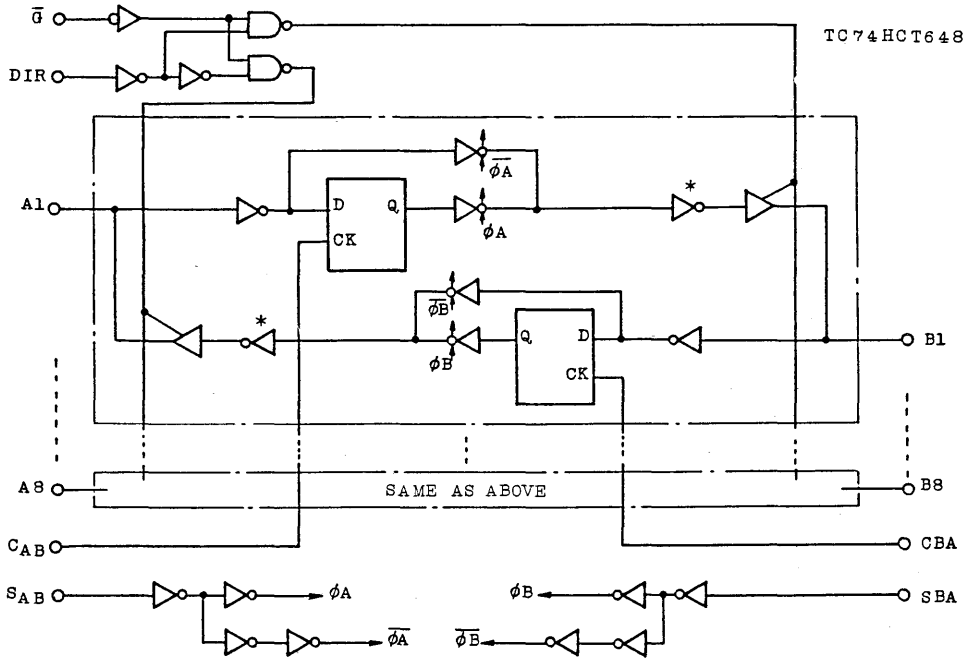
TC74HCT646 (The truth table for TC74HCT648 is the same as this, but with the outputs inverted)

$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A	B	Function
H	X					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↓	↓	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↓	X*	L	X	L H	L H	The data at the A bus displayed at the B bus. The data of A bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↓	X*	H	X	L H	L H	The data at the A bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
L	L					OUTPUTS	OUTPUTS	The B bus are inputs and the A bus are outputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↓	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flop-flops are displayed at the B bus.
		X*	↓	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.

Note: X; Don't care
Qn; The data stored to the internal flip-flops by most recent low to high transition of the clock inputs.
Z; High Impedance
* The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

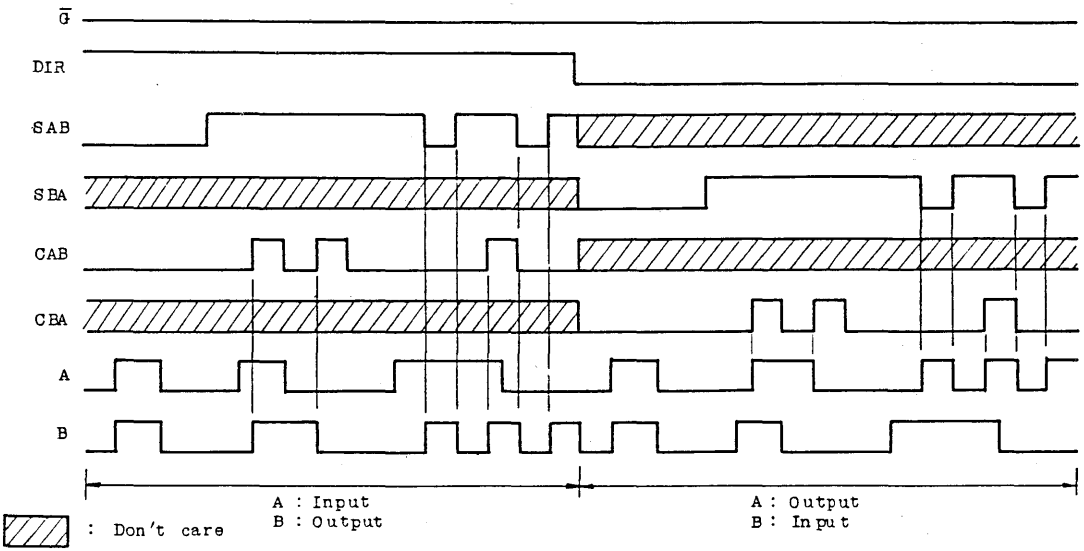
TC74HCT646P
TC74HCT648P

LOGIC DIAGRAM



Note: In case of TC74HCT646, output inverter marked ※ at A bus and B bus are eliminated.

TIMING CHART (TC74HCT646P)



TC74HCT646P
TC74HCT648P

ABSOLUTE MAXIMUM RATINGS

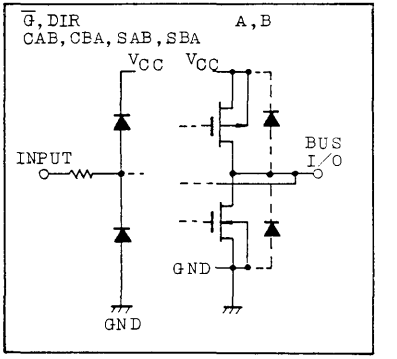
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of 10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ∿ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ∿ 5.5	-	-	0.8	-	0.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	V_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	4.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (BUS - BUS)	t_{pLH} t_{pHL}		4.5	-	20	31	-	39	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		4.5	-	30	46	-	58	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		4.5	-	31	48	-	60	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		4.5	-	11	20	-	25	
Minimum Data Set-up Time	t_s		4.5	-	4	10	-	13	
Minimum Data Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time ($\overline{G}$ - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	26	38	-	48	
3-State Output Disable Time ($\overline{G}$ - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	38	-	48	

TC74HCT646P
TC74HCT648P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time (DIR - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	28	40	-	50	ns
3-State Output Disable Time (DIR - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	28	40	-	50	ns
Input Capacitance	C_{IN}	*		-	5	10	-	10	pF
Output Capacitance	C_{OUT}	An, Bn		-	13	-	-	-	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC646		-	55	-	-	-	pF
		TC74HC648		-	52	-	-	-	pF

* Applicable only to DIR, $\overline{G}$, CAB, CBA, SAB, SBA input.

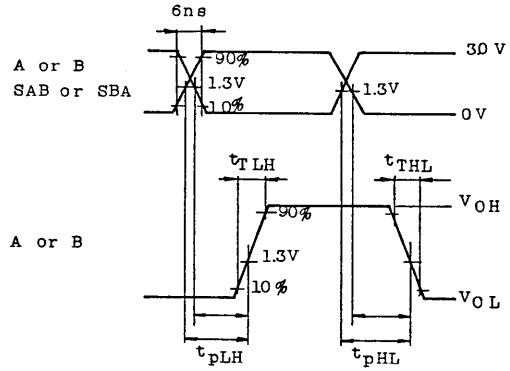
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \quad \text{(per bit)}$$

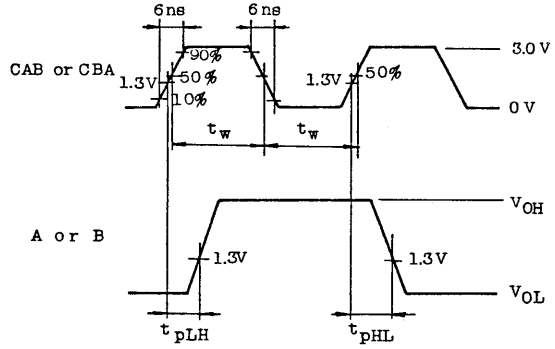
TC74HCT646P
TC74HCT648P

SWITCHING CHARACTERISTICS TEST WAVEFORM

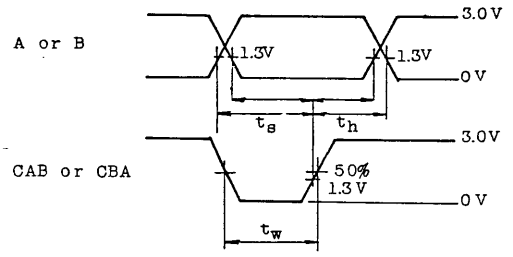
WAVEFORM 1



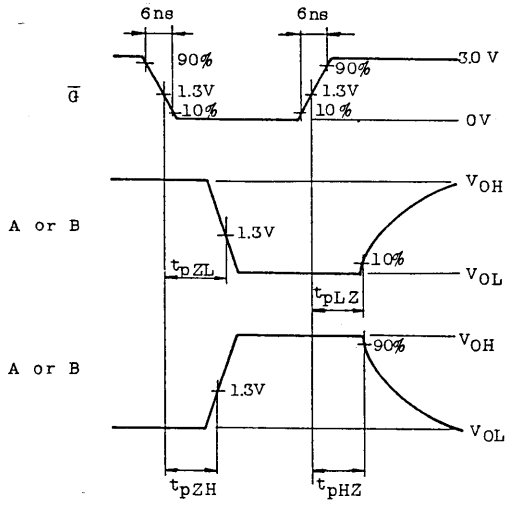
WAVEFORM 2



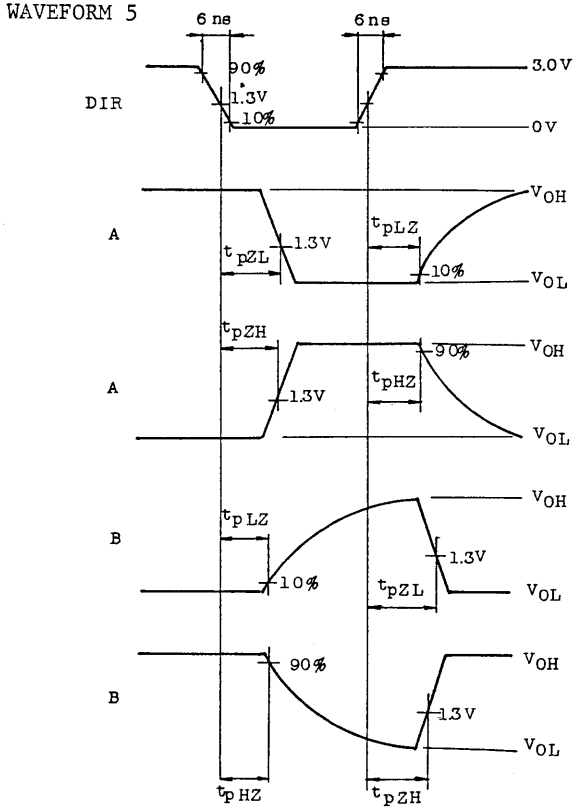
WAVEFORM 3



WAVEFORM 4

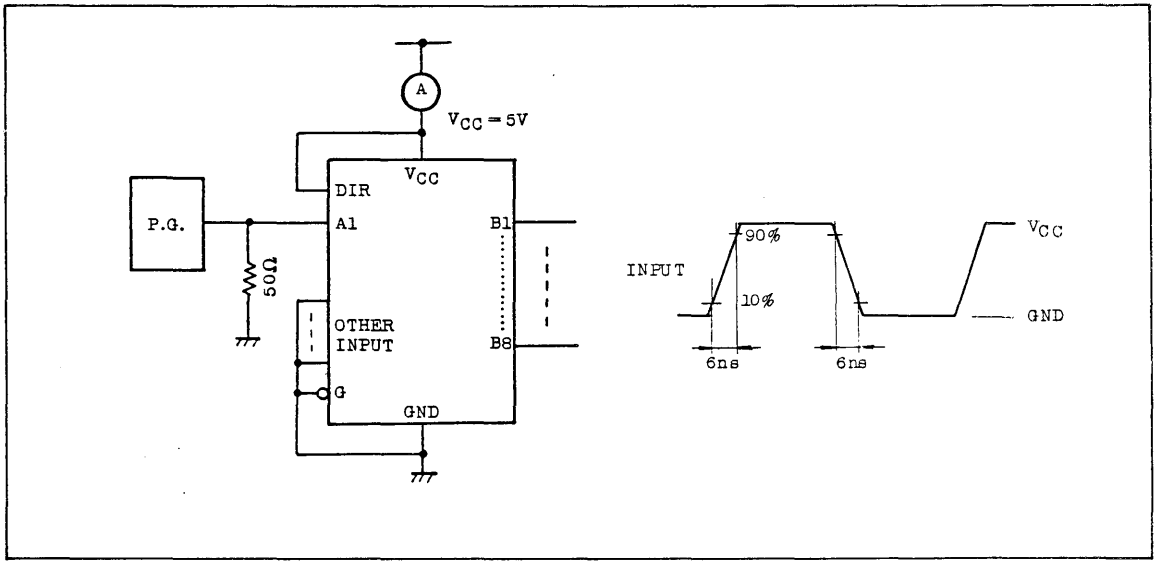


WAVEFORM 5



TC74HCT646P
TC74HCT648P

$I_{CC(Opr.)}$ TEST CIRCUIT



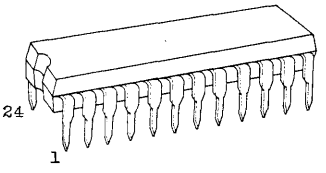
TC74HC651P
TC74HC652P

CMOS DIGITAL INTEGRATED CIRCUIT

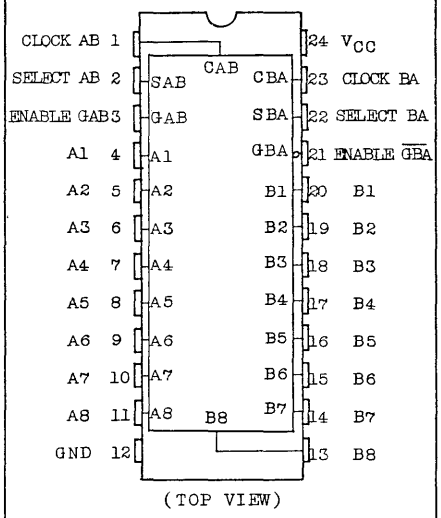
PRELIMINARY

TC74HC651P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)
TC74HC652P OCTAL BUS TRANSCEIVER/REGISTER

The TC74HC651 and TC74HC652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices are bus tranceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If enable inputs GAB and $\overline{GBA}$ are held "H", A bus are inputs and B bus are outputs, and if GAB and $\overline{GBA}$ are held "L", B bus are inputs and A bus are outputs.
Enable input GAB is held "L" and either $\overline{GBA}$ is held "H", respectively, A bus and B bus are isolated.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of the internal flip-flops. These flip-flops change state on positive going transition of the clock pulses (CAB, CBA). The TC74HC651 is inverting output type while the TC74HC652 is non-inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 15 LSTTL Loads
- Symmetrical Output Impedance.. $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ....V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS651/652

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode. And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

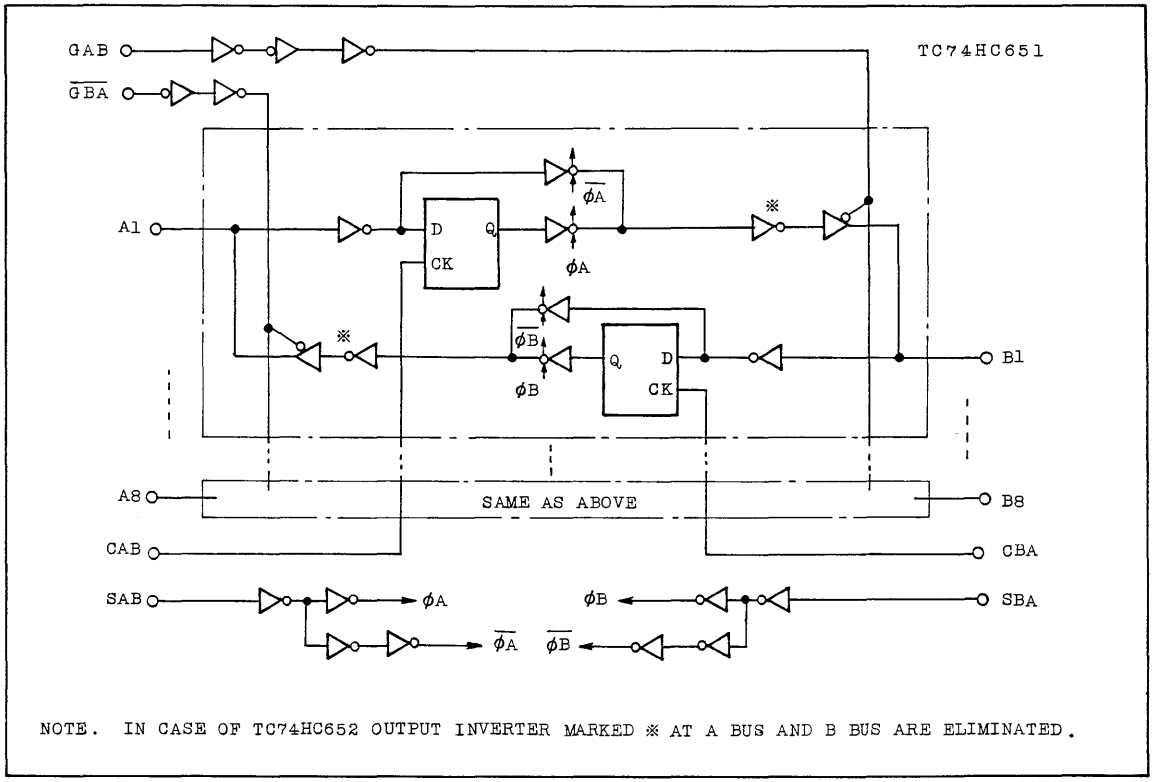
TC74HC652 (The truth table for TC74HC651 is the same as this, but with the outputs inverted)

GAB	$\overline{CBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to internal Flip-flops. Data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↑	↑	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively.

X: Don't Care Qn: The data stored to the internal flip-flops by most recent low to high transition of the clock inputs. Z: High Impedance *: The data at the A and B bus will be stored to the internal flip-flops on every low to high transition of the clock inputs.

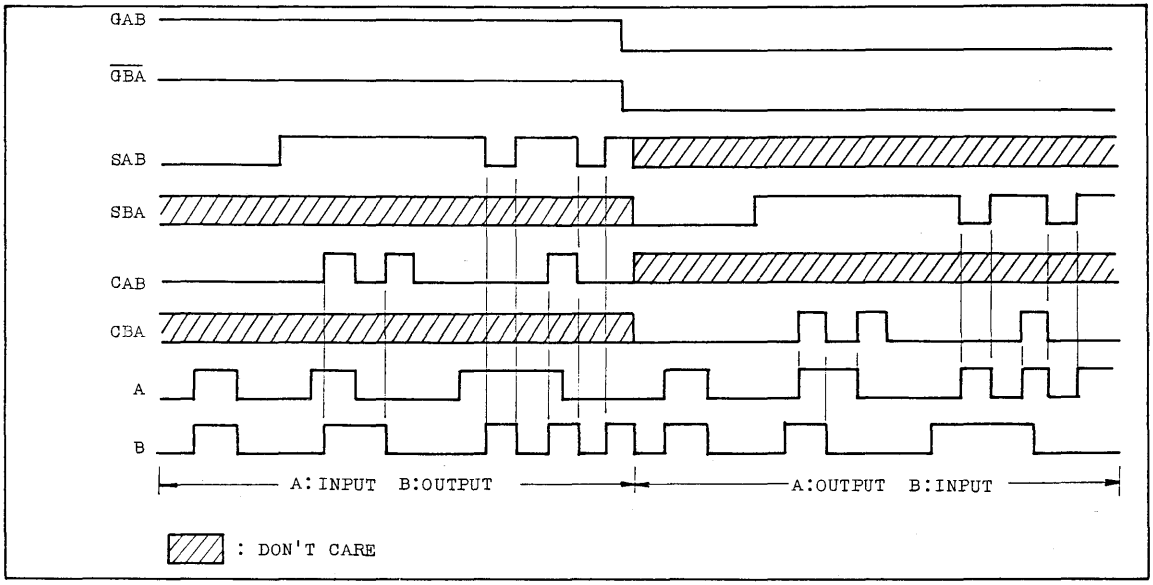
TC74HC651P
TC74HC652P

LOGIC DIAGRAM



NOTE. IN CASE OF TC74HC652 OUTPUT INVERTER MARKED ※ AT A BUS AND B BUS ARE ELIMINATED.

TIMING CHART



TC74HC651P
TC74HC652P

ABSOLUTE MAXIMUM RATINGS

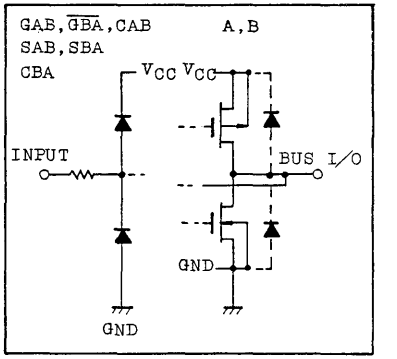
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
Bus Terminal Voltage	$V_{I/O}$	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$2 \sim 6$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Bus Terminal Voltage	$V_{I/O}$	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 1000$ (V_{CC}=2.0V) $0 \sim 500$ (V_{CC}=4.5V) $0 \sim 400$ (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC651P
TC74HC652P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current*	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Suppy Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

* Applicable onlt to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (BUS - BUS)	t_{pHL} t_{pHL}		2.0	-	92	180	-	225	
			4.5	-	23	36	-	45	
			6.0	-	20	31	-	38	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
			6.0	-	26	41	-	51	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Minimum Clock Pulse Width	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	5	50	-	65	
			4.5	-	1	10	-	13	
			6.0	-	1	9	-	11	
Minimum Data Hold Time	t_h		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	

TC74HC651P
TC74HC652P

AC CHARACTERISTICS (Continued)

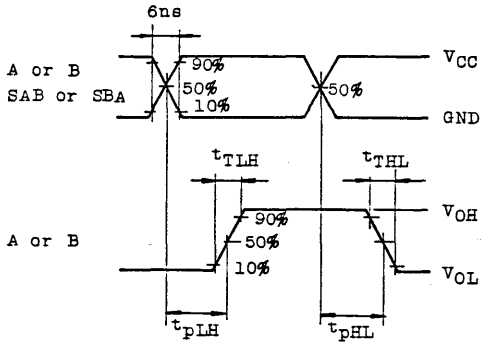
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time	t_{PZL} / t_{PZH}	R_L=1kΩ	2.0	-	100	180	-	225	ns
			4.5	-	25	36	-	45	
			6.0	-	21	31	-	38	
3-State Output Disable Time	t_{PLZ} / t_{PHZ}	R_L=1kΩ	2.0	-	88	170	-	215	
			4.5	-	22	34	-	43	
			6.0	-	19	29	-	37	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	46	-	-	-	

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

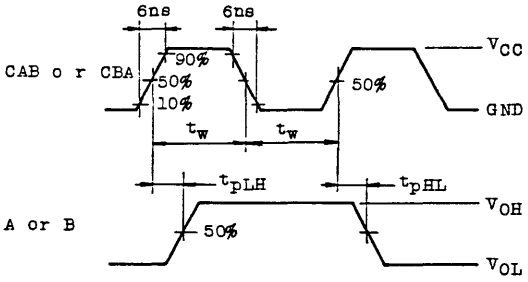
TC74HC651P
TC74HC652P

SWITCHING CHARACTERISTICS TEST WAVEFORM

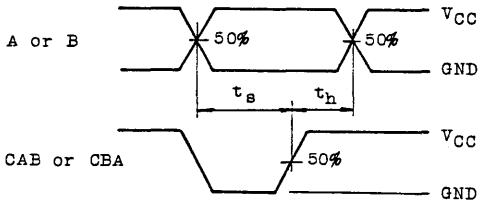
WAVEFORM 1



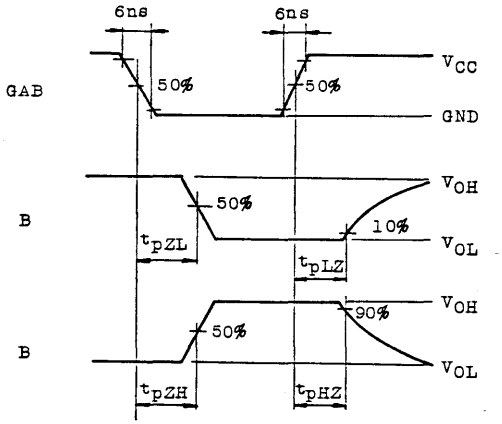
WAVEFORM 2



WAVEFORM 3

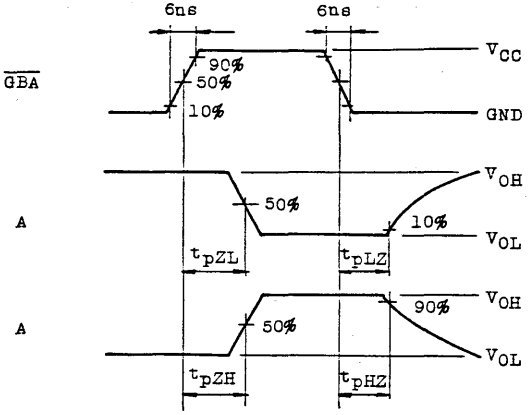


WAVEFORM 4



$\overline{GBA}$="H"

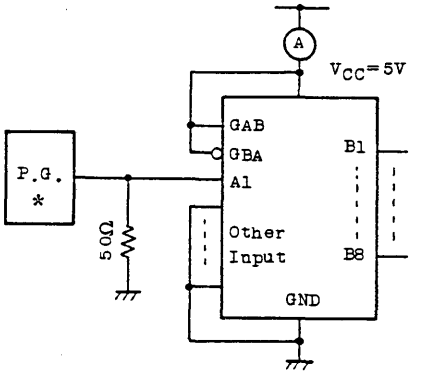
WAVEFORM 5



GAB="L"

TC74HC651P
TC74HC652P

$I_{CC(Opr.)}$ TEST WAVEFORM



* Input transition time is the same as that in case of switching characteristics test.

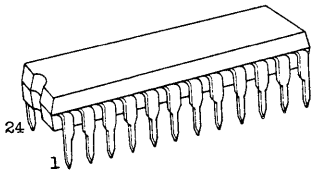
TC74HCT651P
TC74HCT652P

CMOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

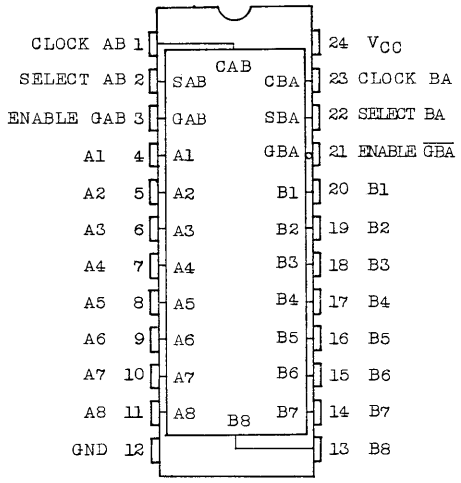
TC74HCT651P OCTAL BUS TRANSCEIVER/REGISTER (INVERTING)
TC74HCT652P OCTAL BUS TRANSCEIVER/REGISTER

The TC74HCT651 and TC74HCT652 are high speed CMOS OCTAL BUS TRANSCEIVER/REGISTER fabricated with silicon gate C^2MOS technology.
They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
These devices may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.
These devices are bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. If enable inputs GAB and $\overline{GBA}$ are held "H", A bus are inputs and B bus are outputs, and if GAB and $\overline{GBA}$ are held "L", B bus are inputs and A bus are outputs.
Enable input GAB is held "L" and either $\overline{GBA}$ is held "H", respectively, A bus and B bus are isolated.
If the select inputs (SAB, SBA) are held "L", these bus outputs real-time. If the select inputs are held "H", these bus outputs the state of the internal flip-flops. These flip-flops change state on positive going transition of the clock pulses (CAB, CBA). The TC74HCT651 is inverting output type while the TC74HCT652 is non-inverting output type.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP24(3D24A-P)

PIN ASSIGNMENT



(TOP VIEW)

FEATURES:

- High Speed ..... t_{pd}=27ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .. I_{CC}=4μA(Max.) at Ta=25°C
- Compatible with TTL Output ..... V_{IH}=2V(Min.)
  V_{IL}=0.8V(Max.)
- Output Drive Capability .....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS651/652

NOTICE FOR APPLICATION

It is prohibited to apply a signal to a bus terminal when it is in output mode.
And when a bus terminal is floating (high impedance state), it is requested to fix the input level by means of external pull down or pull up resistor or BUS TERMINATOR IC (TC40117BP).

TRUTH TABLE

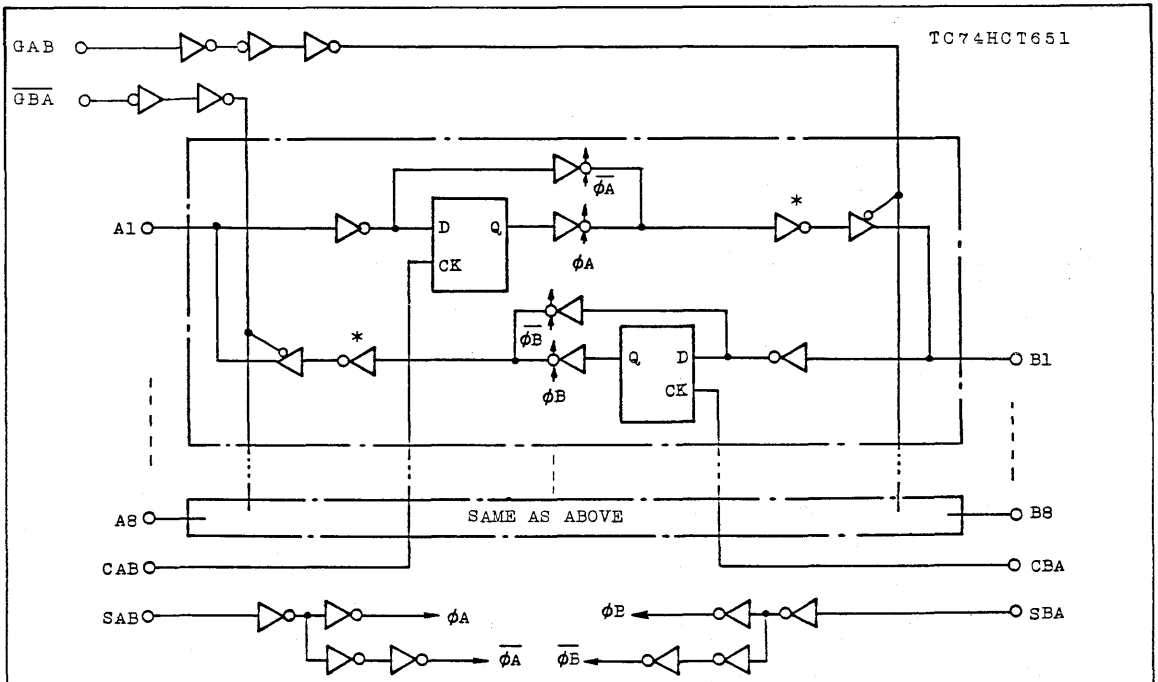
TC74HCT652 (The truth table for TC74HCT651 is the same as this, but with the outputs inverted)

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs.
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled.
		↑	↑	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to internal Flip-flops. The data at the bus will be stored on low to high transition of the clock inputs.
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs.
		X*	X	X	L	L H	L H	The data at the B bus are displayed at the A bus.
		X*	↑	X	L	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X*	X	X	H	Qn	X	The data stored to the internal flip-flops are displayed at the A bus.
		X*	↑	X	H	L H	L H	The data at the B bus are stored to the internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus.
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs.
		X	X*	L	X	L H	L H	The data at the A bus are displayed at the B bus.
		↑	X*	L	X	L H	L H	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flops on low to high transition of the clock pulse.
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus.
		↑	X*	H	X	L H	L H	The data at the A bus are stored to internal flip-flops on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus.
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs.
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively.
		↑	↑	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively.

X: Don't care Qn: The data stored to the internal flip-flops by most recent low to high transition of the clock inputs. Z: High Impedance *: The data at the A and B bus will be stored to the internal flip-flops on every low to high trnsition of the clock inputs.

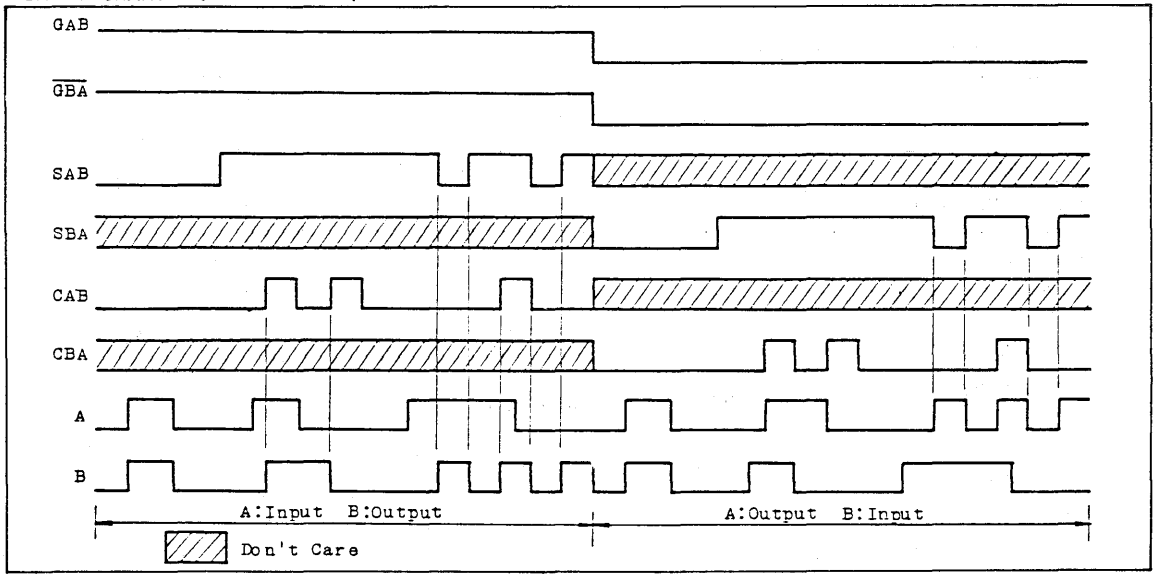
TC74HCT651P
TC74HCT652P

LOGIC DIAGRAM



Note: In case of TC74HCT652, Output inverter marked * at A bus and B bus are eliminated.

TIMING CHART (TC74HCT652P)



TC74HCT651P
TC74HCT652P

ABSOLUTE MAXIMUM RATINGS

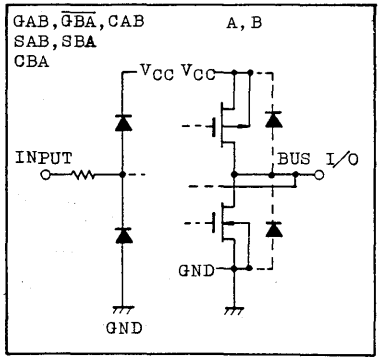
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
DC Input Voltage	V_{IN}	$-0.5 \sim V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC}+0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied unitl 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	$4.5 \sim 5.5$	V
Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Output Voltage	V_{OUT}	$0 \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise and Fall Time	t_r, t_f	$0 \sim 500$	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			4.5 ⟨ 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 ⟩ 5.5	-	-	0.8	-	0.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5	-	4.4	-	
			$I_{OH}=-6mA$	4.5	4.18	4.31	-	4.13	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5	-	0.0	0.1	-	0.1	
			$I_{OL}=6mA$	4.5	-	0.17	0.26	-	0.33	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Off-State Current	I_{OZ}	$V_{IN}=V_{IH}$ or V_{IL} $V_{OUT}=V_{CC}$ or GND	5.5	-	-	±0.5	-	±5.0	μA
Input Leakage Current *	I_{IN}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	5.5	-	-	4.0	-	40.0	
	I_C	Per input: V_{IN}=2.4V or 0.5V Other input: V_{CC} or GND	5.5	-	-	2.0	-	2.9	mA

* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

AC ELECTRICAL CHARACTERISTICS (CL=50pF, INPUT tr=tf=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	7	12	-	15	ns
Propagation Delay Time (BUS - BUS)	t_{pLH} t_{pHL}		4.5	-	20	31	-	39	
Propagation Delay Time (CLOCK - BUS)	t_{pLH} t_{pHL}		4.5	-	30	47	-	59	
Propagation Delay Time (SELECT - BUS)	t_{pLH} t_{pHL}		4.5	-	31	48	-	60	
Minimum Clock Pulse Widht	$t_{w(H)}$ $t_{w(L)}$		4.5	-	11	20	-	25	
Minimum Data Set-up Time	t_s		4.5	-	4	10	-	13	
Minimum Data Hold Time	t_h		4.5	-	-	5	-	5	
3-State Output Enable Time ($\overline{GBA}$ - BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	21	30	-	38	
3-State Output Disable Time ($\overline{GBA}$ - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	26	38	-	48	

TC74HCT651P
TC74HCT652P

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40∿85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Enable Time(GAB -BUS)	t_{pZL} t_{pZH}	R_L=1kΩ	4.5	-	25	36	-	45	ns
3-State Output Disable Time(GAB - BUS)	t_{pLZ} t_{pHZ}	R_L=1kΩ	4.5	-	25	36	-	45	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}	BUS I/O		-	13	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT651		-	52	-	-	-	
		TC74HCT652		-	52	-	-	-	

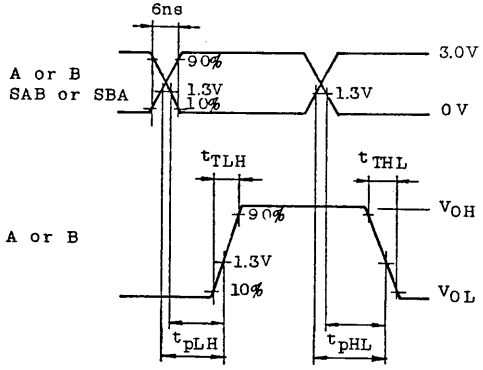
* Applicable only to GAB, $\overline{GBA}$, CAB, CBA, SAB, SBA inputs.

Note (1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

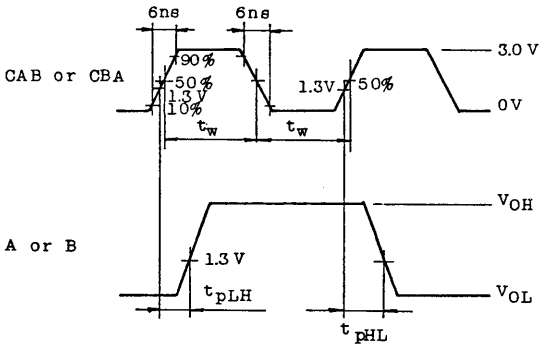
$$I_{PD(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

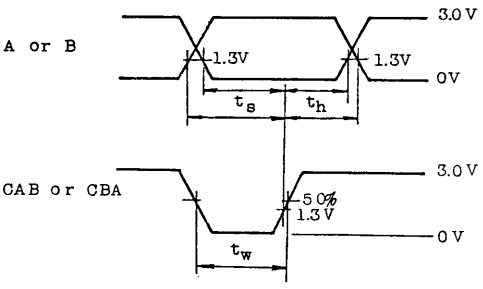
WAVEFORM 1



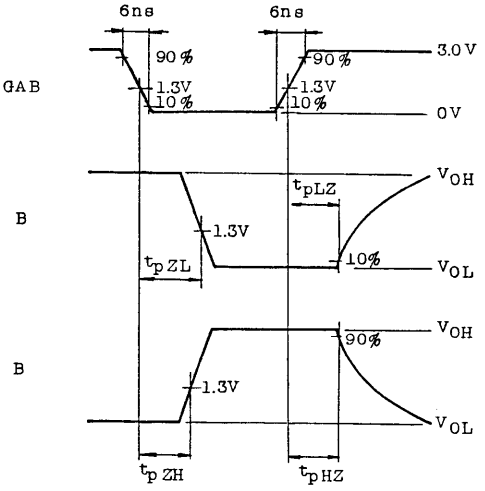
WAVEFORM 2



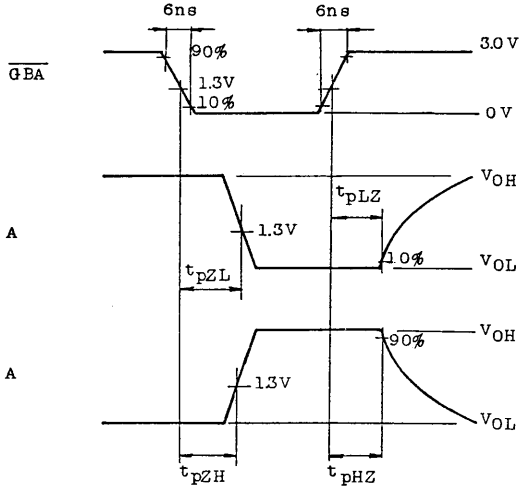
WAVEFORM 3



WAVEFORM 4 $\overline{GBA}$="H"

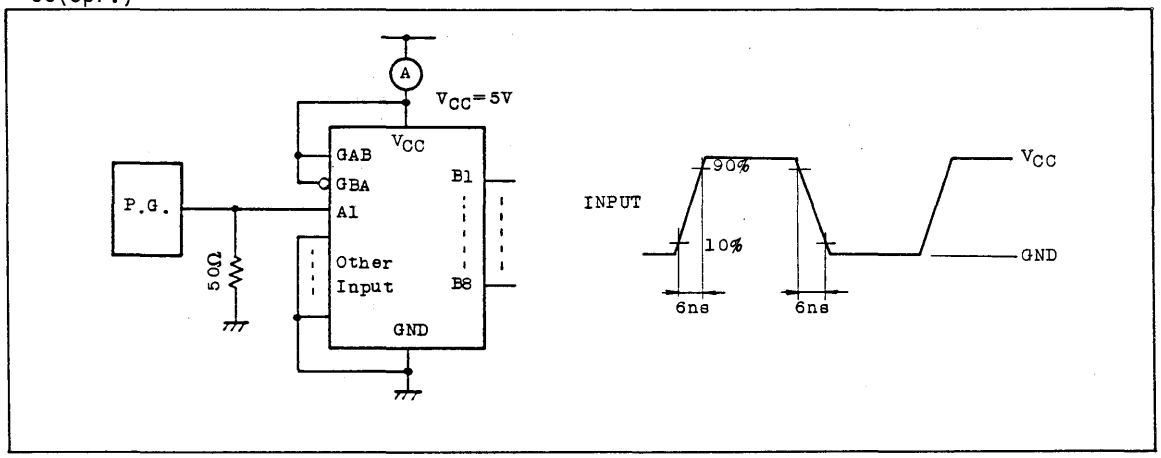


WAVEFORM 5 GAB="L"



TC74HCT651P
TC74HCT652P

$I_{CC(Opr.)}$ TEST WAVEFORM



TC74HCT651P
TC74HCT652P

TC74HC670P

C²MOS DIGITAL INTEGRATED CIRCUIT

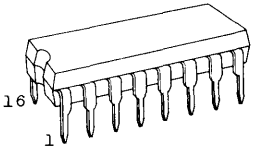
PRELIMINARY

TC74HC670P 4-WORD x 4-BIT REGISTER FILE (3-STATE)

The TC74HC670 is a high speed CMOS 4-WORD × 4-BIT REGISTER FILE fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.
Four data inputs are avairable which are used to supply the 4-bit word to be stored. Location of the word is determined by the A and B inputs. When the WRITE-ENABLE input is "H", the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the READ-ENABLE input "H", the data outputs are inhibited and go into the high-impedance state.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=21ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 74LS670



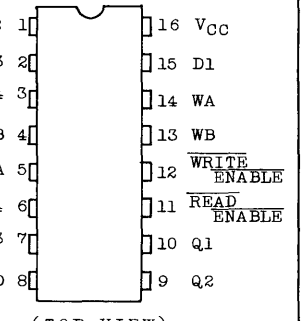
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC670P

TRUTH TABLE

WRITE FUNCTION TABLE

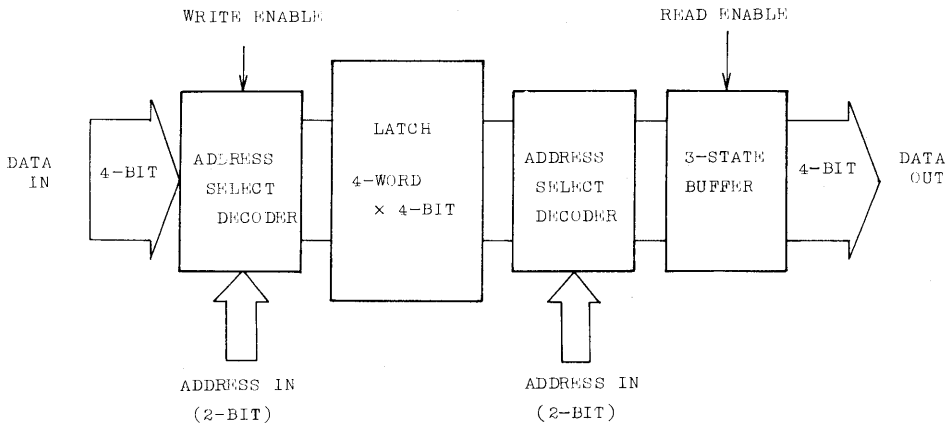
WRITE INPUTS			WORDS			
WB	WA	$\overline{WE}$	0	1	2	3
L	L	L	Q=D	Q0	Q0	Q0
L	H	L	Q0	Q=D	Q0	Q0
H	L	L	Q0	Q0	Q=D	Q0
H	H	L	Q0	Q0	Q0	Q=D
X	X	H	Q0	Q0	Q0	Q0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
RB	RA	$\overline{RE}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

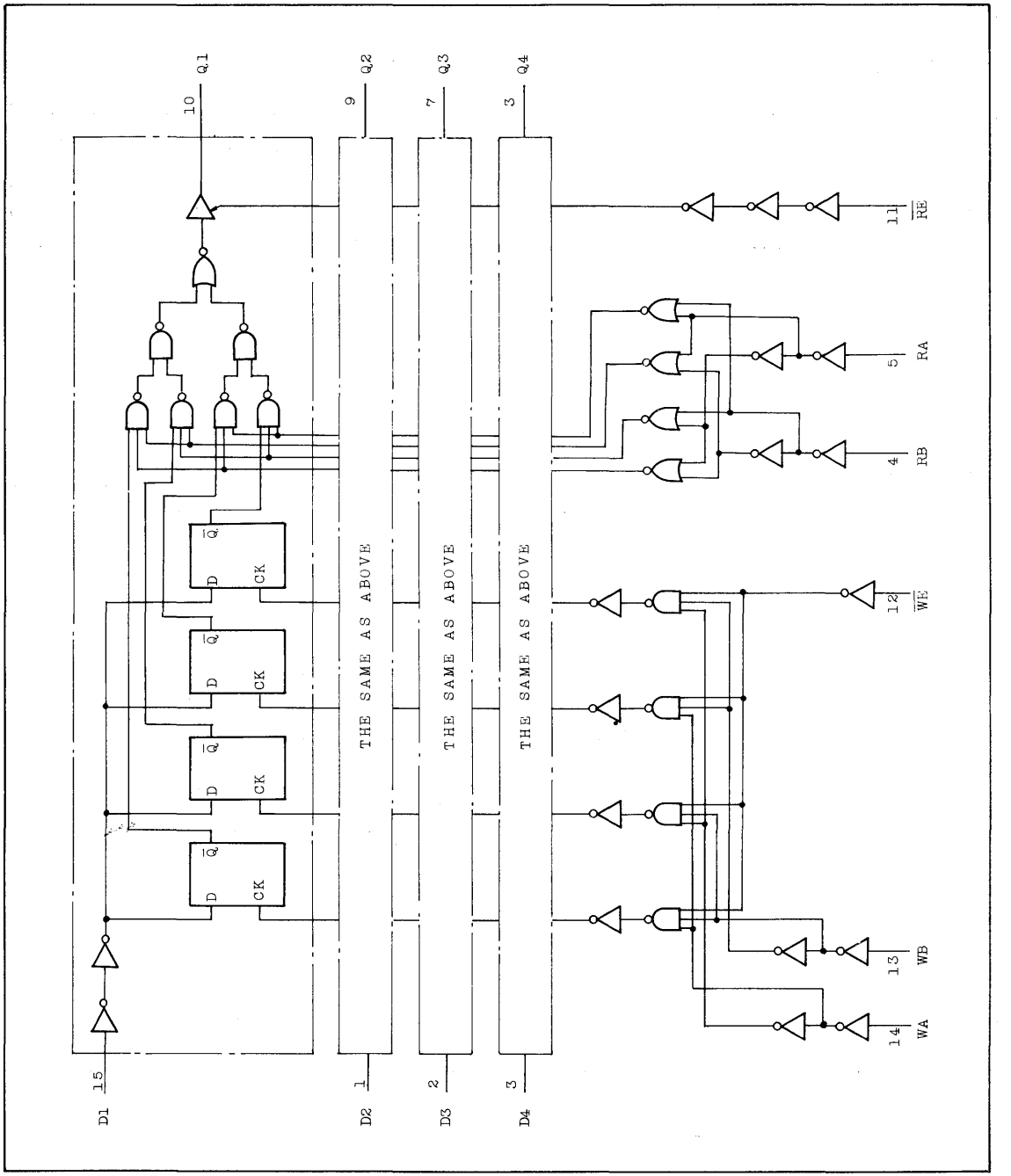
NOTES
1. X : DON'T CARE Z : HIGH IMPEDANCE
2. (Q=D) = THE FOUR SELECTED INTERNAL FLIP-FLOP OUTPUTS WILL ASSUME THE STATES APPLIED TO THE FOUR EXTERNAL DATA INPUTS.
3. Q0 = THE LEVEL OF Q BEFORE THE INDICATED INPUT CONDITIONS WERE ESTABLISHED.
4. W0B1 = THE FIRST BIT OF WORD 0, etc.

BLOCK DIAGRAM



TC74HC670P

LOGIC DIAGRAM

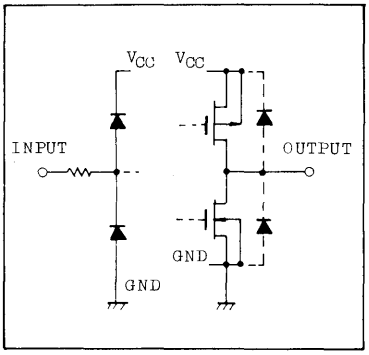


TC74HC670P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC670P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

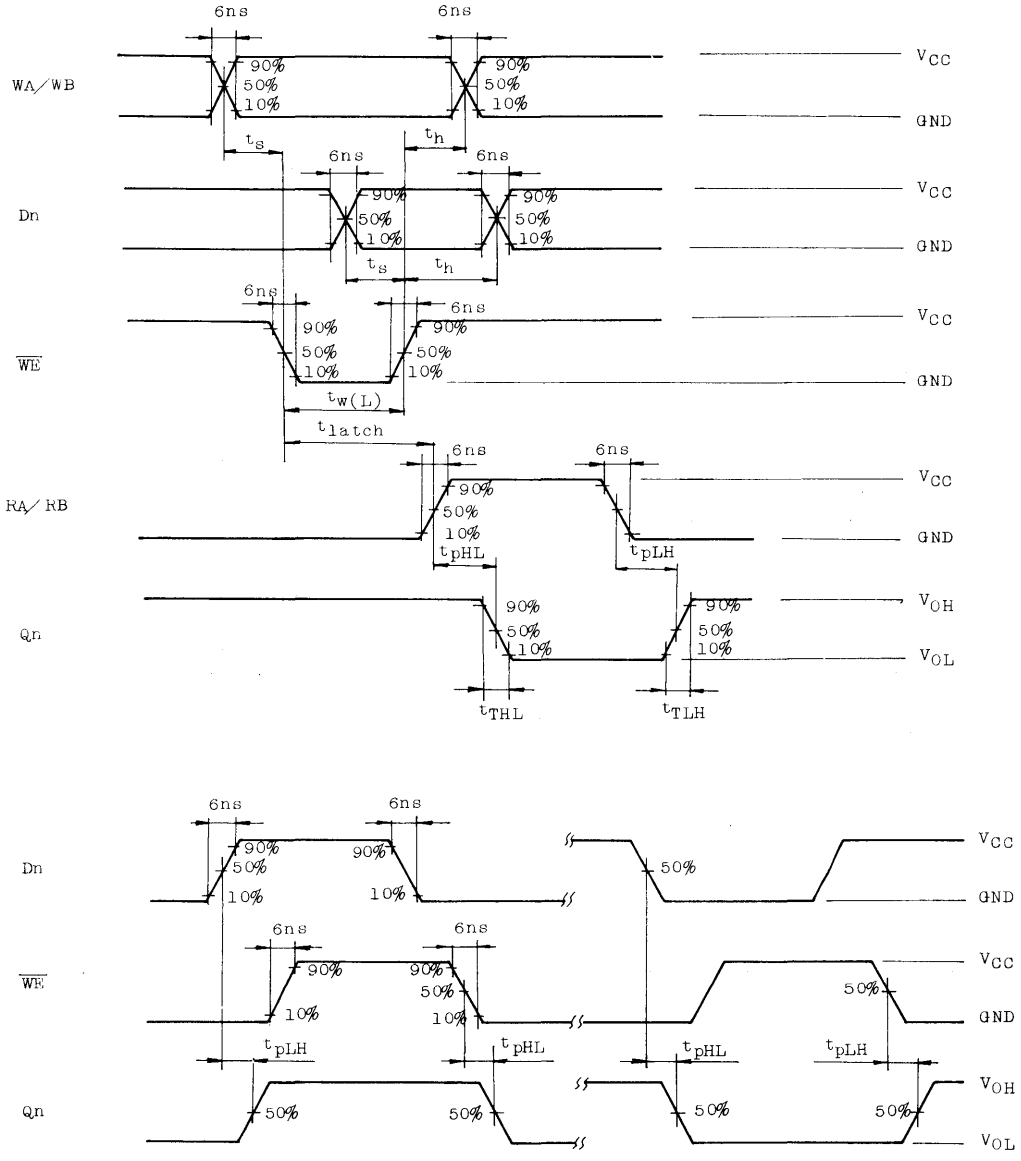
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (RA, RB - Qn)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time ($\overline{WE}$ - Qn)	t_{pLH} t_{pHL}		2.0	-	112	220	-	275	
			4.5	-	28	44	-	55	
			6.0	-	24	37	-	47	
Propagation Delay Time (Dn - Qn)	t_{pLH} t_{pHL}		2.0	-	92	185	-	230	
			4.5	-	23	37	-	46	
			6.0	-	20	31	-	39	
Minimum Pulse Width ($\overline{WE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time (Dn - $\overline{WE}$)	t_s		2.0	-	-	25	-	30	
			4.5	-	-	5	-	6	
			6.0	-	-	5	-	5	
Minimum Set-up Time (WA, WB - $\overline{WE}$)	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time (Dn - $\overline{WE}$)	t_h		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time (WA, WB - $\overline{WE}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Latch Time ($\overline{WE}$ - RA, RB)	(1) t_{latch}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
3-State Output Enable Time	t_{pZL} t_{pZH}	R_L=1kΩ	2.0	-	52	110	-	140	
			4.5	-	13	22	-	28	
			6.0	-	11	19	-	24	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	68	120	-	150	
			4.5	-	17	24	-	30	
			6.0	-	14	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Output Capacitance	C_{OUT}			-	10	-	-	-	
Power Dissipation Capacitance	C_{PD}(2)			-	44	-	-	-	

Note(1): t_{latch} is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

(2): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

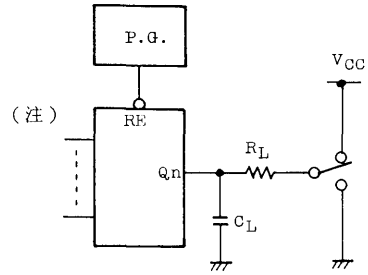
$$I_{CC(Opr.)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

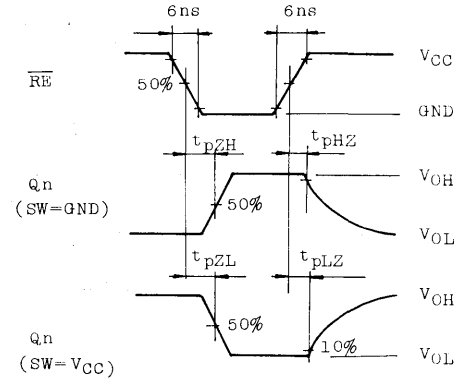
SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC670P

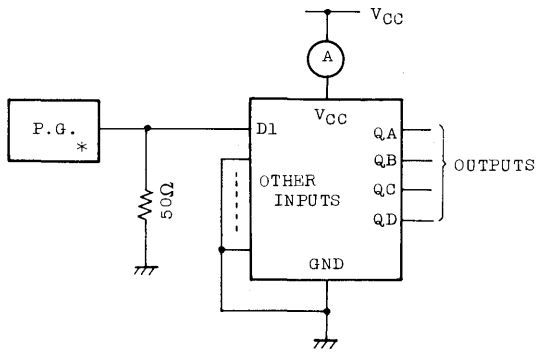
SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)





(NOTE)
SUCH A LOGIC LEVEL SHALL BE APPLIED TO EACH INPUT THAT THE OUTPUT VOLTAGE STAYS IN THE APPOSITE SIDE TO THE SWITCH CONNECTION LEVEL. WHEN THE OUTPUT IS ENABLED.

$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC688P

PRELIMINARY

TC74HC688P 8-BIT EQUALITY COMPARATOR

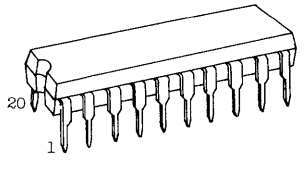
The TC74HC688 utilizes silicon gate C^2MOS technology to achieve operating speeds equivalent to LSTTL parts. Along with the low power dissipation and high noise immunity of standard C^2MOS integrated circuit, it possesses the driving capability of 10 LSTTL loads.

The TC74HC688 compares bit for bit two 8-bit words applied input $P_0 \sim P_7$ and input $Q_0 \sim Q_7$ and indicate whether or not they are equal.

A single active low enable is provided to facilitate cascading of several packages to enable comparison of words greater than 8 bits. All inputs are equipped with protection circuit against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=25ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 74LS688.



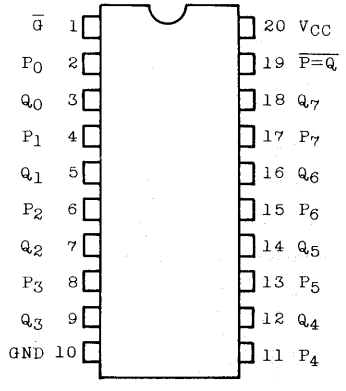
DIP20(3D20A-P)

TRUTH TABLE

INPUT		OUTPUT
P,Q	$\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P ≠ Q	L	H
*	H	H

* Don't care

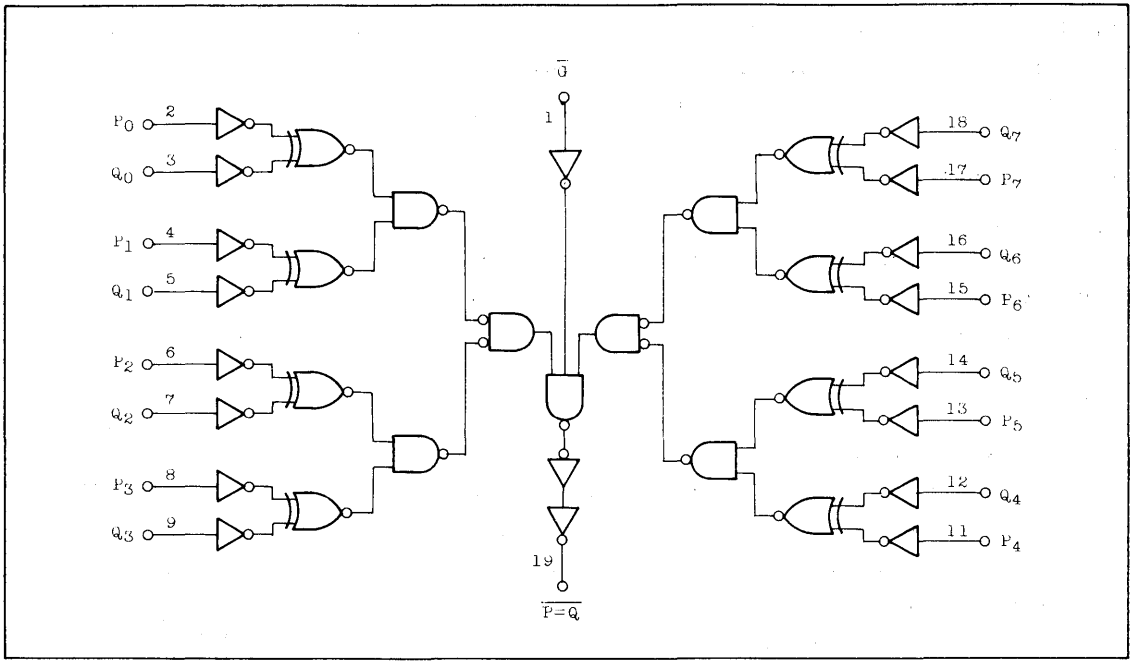
PIN ASSIGNMENT



(TOP VIEW)

TC74HC688P

LOGIC DIAGRAM

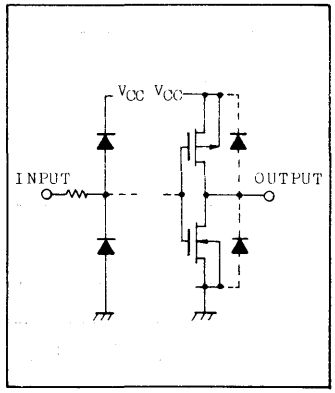


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC688P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC688P

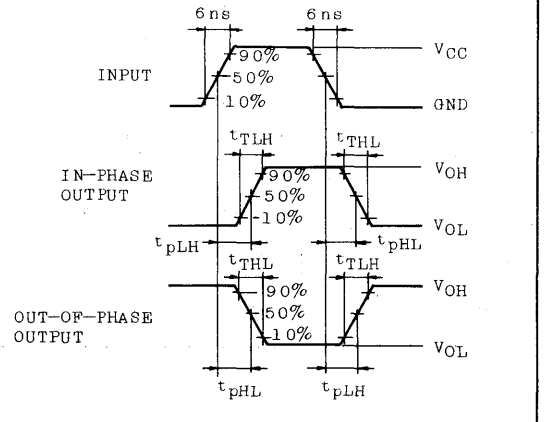
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (P_n,Q_n - $\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	-	104	195	-	245	
			4.5	-	26	39	-	49	
			6.0	-	22	33	-	42	
Propagation Delay Time ($\overline{G}$ - $\overline{P=Q}$)	t_{pLH} t_{pHL}		2.0	-	60	120	-	150	
			4.5	-	15	24	-	30	
			6.0	-	13	20	-	26	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	40	-	-	-	

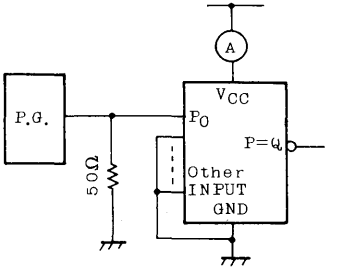
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4002P

PRELIMINARY

TC74HC4002P DUAL 4-INPUT NOR GATE

The TC74HC4002 is a high speed CMOS 4-INPUT NOR GATE fabricated with silicon gate C²MOS technology.

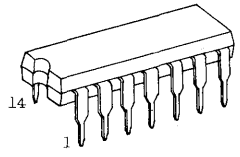
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuit against static discharge or transient excess voltage.

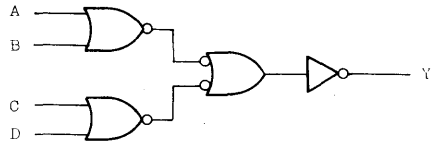
FEATURES:

- High Speed.....t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \doteqdot t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4002B

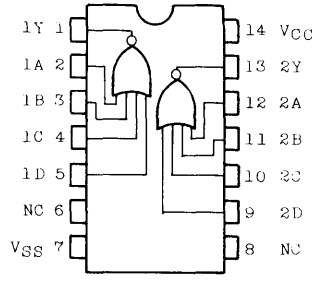


DIP14(3D14A-P)

LOGIC DIAGRAM (PER GATE)



PIN ASSIGNMENT



(TOP VIEW)

TC74HC4002P

ABSOLUTE MAXIMUM RATINGS

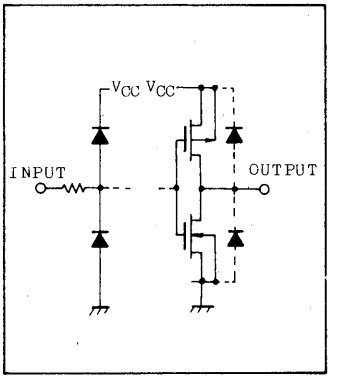
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC4002P

DC ELECTRICAL CHARACTERISTICS

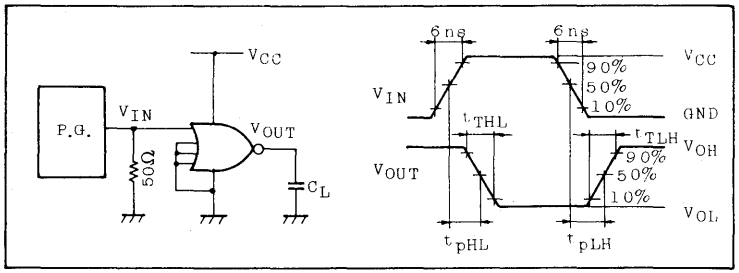
PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

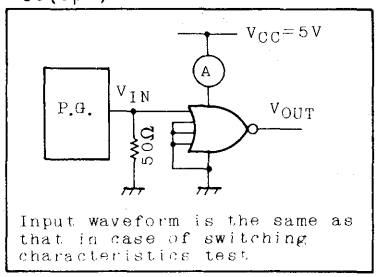
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	52	105	-	130	ns
			4.5	-	13	21	-	26	
			6.0	-	11	18	-	22	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	26	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC4017P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

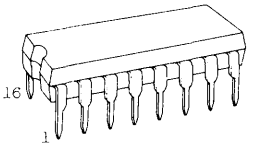
PRELIMINARY

TC74HC4017P/F DECADE COUNTER/DIVIDER

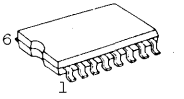
The TC74HC 4017 is a high speed CMOS DECADE JOHNSON COUNTER fabricated with silicon C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 5-stage divided-by-10 Johnson counter with 10 decoded output (Q0 - Q10) and carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{CE}$ input is held low, or it is advanced on the negative edge of the clock enable signal ($\overline{CE}$) when CLOCK input is held high, and selected one of ten outputs goes high. Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=45MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability .....10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4017B



DIP16(3D16A-P)



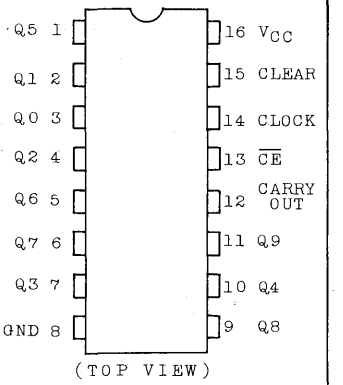
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

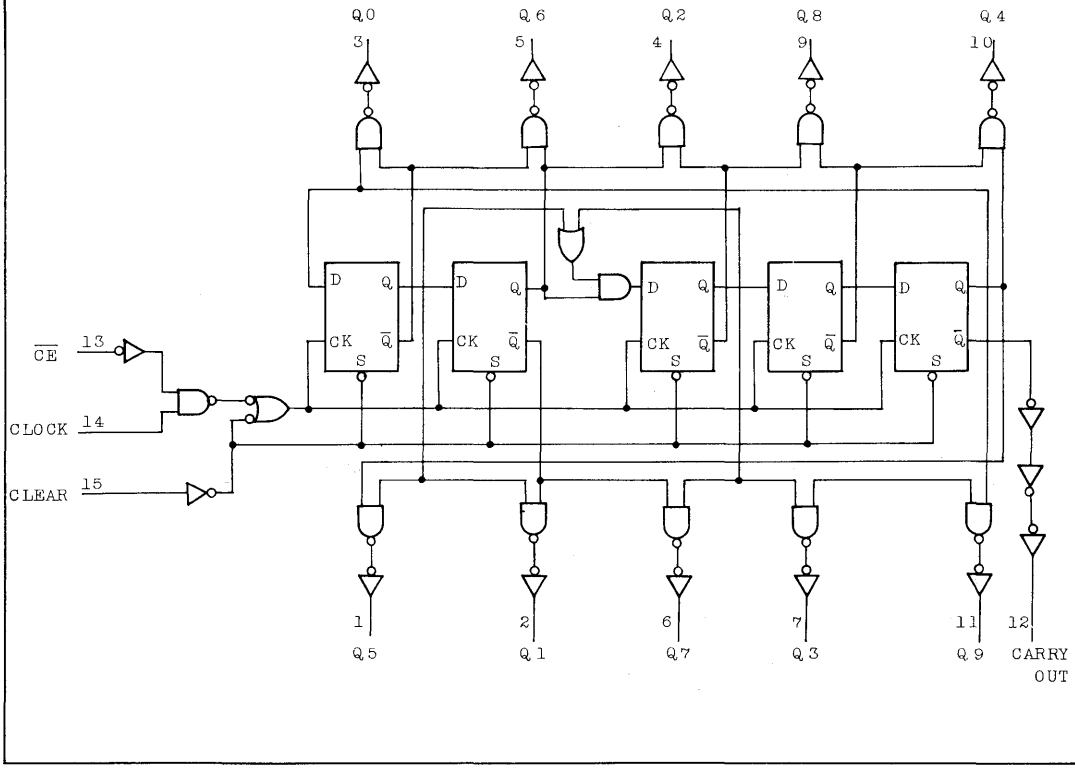
TC74HC4017P/F

TRUTH TABLE

CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↑	L	L	Qn+1
↓	L	L	Qn
H	↑	L	Qn
H	↓	L	Qn+1

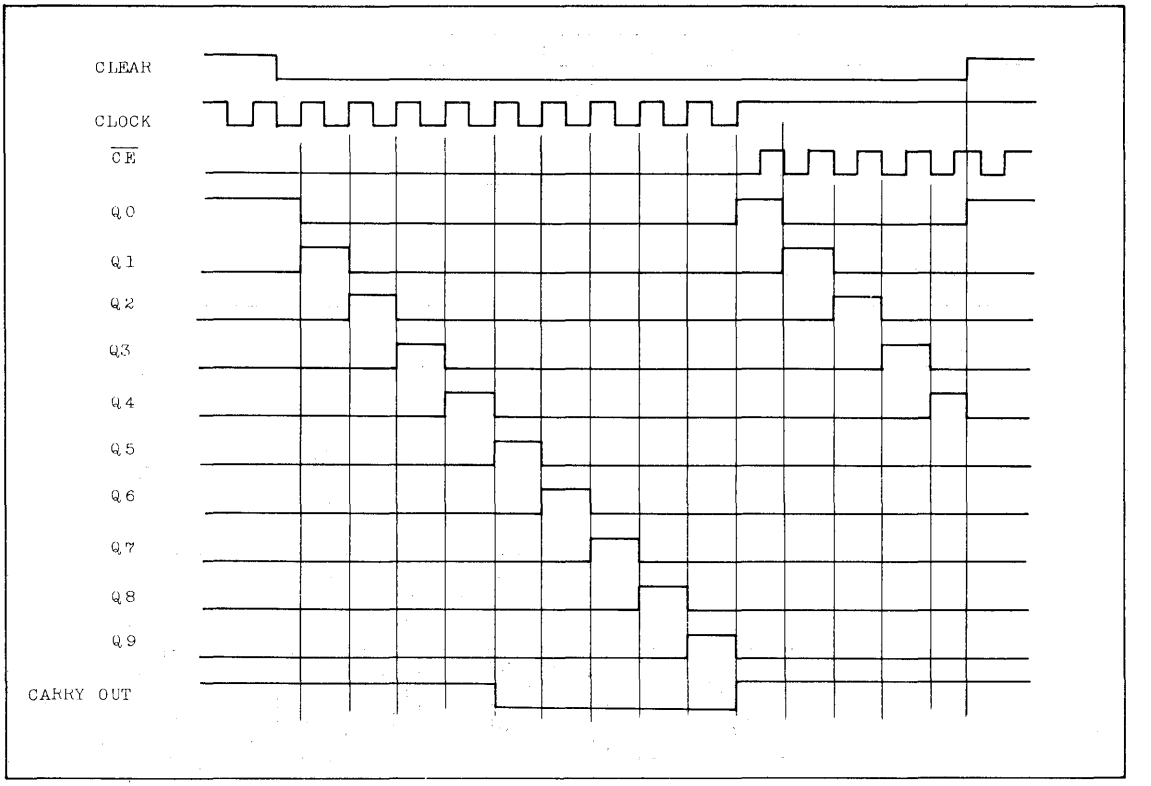
X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



TC74HC4017P/F

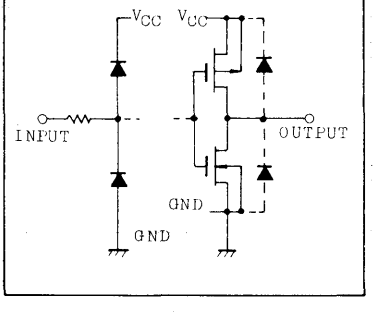
TIMING DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT
EQUIVALENT CIRCUIT



TC74HC4017P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK, $\overline{CE}$ - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

TC74HC4017P/F

AC ELECTRICAL CAHRACTERISTICS (Continued)

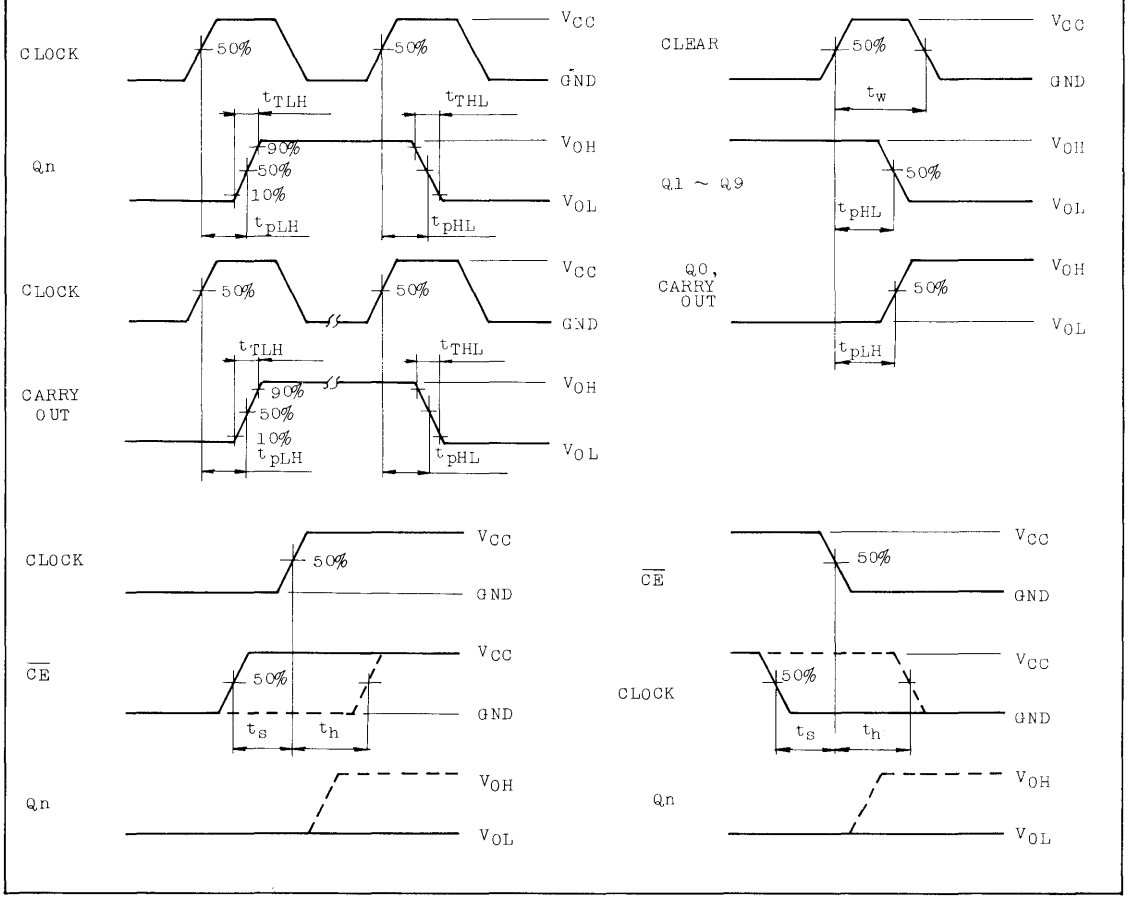
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Maximum Clock Frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	41	-	20	-	
			6.0	29	48	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
	$t_{w(H)}$		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	74	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

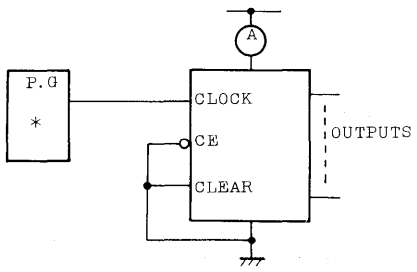
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4017P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4020P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

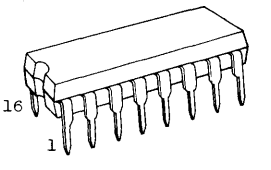
PRELIMINARY

TC74HC4020P/F 14-STAGE BINARY COUNTER

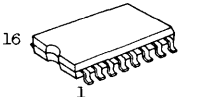
The TC74HC4020 is a high speed CMOS 14-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4020B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accoumplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. Twelve kinds of divided output are provided; 1'st and 4 stage thru 14 stage. And at the last stage, 1/16384 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V∿6V
- Pin and Function Compatible with 4020B.



DIP16(3D16A-P)



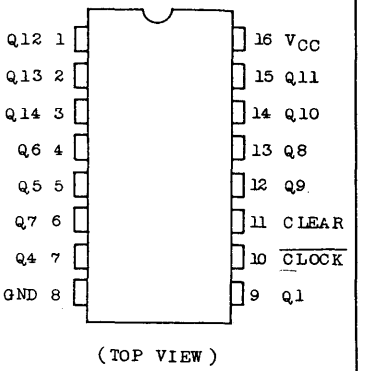
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

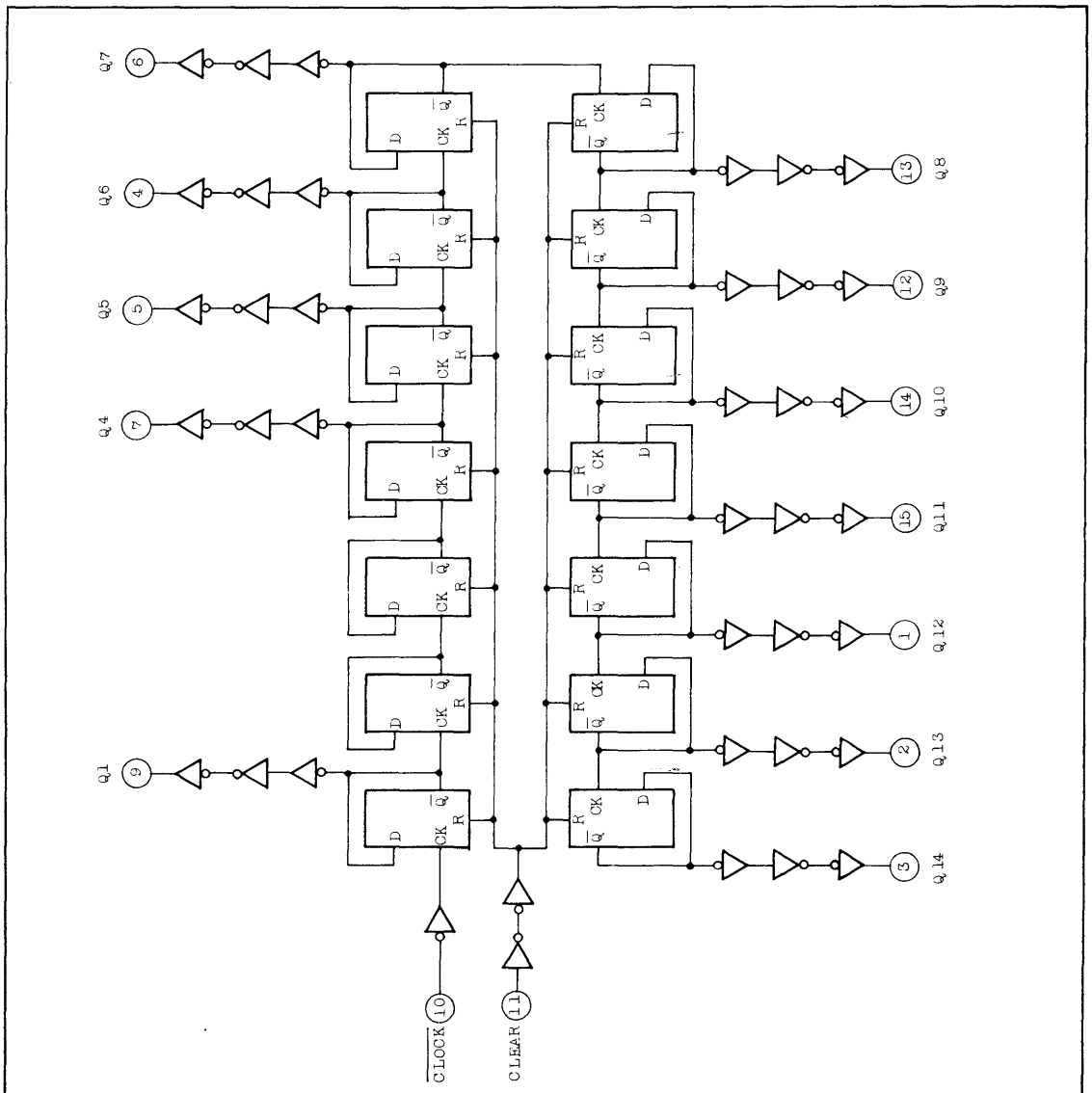
TC74HC4020P/F

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↓	L	ADVANCE TO NEXT STATE

X : DON'T CARE

LOGIC DIAGRAM

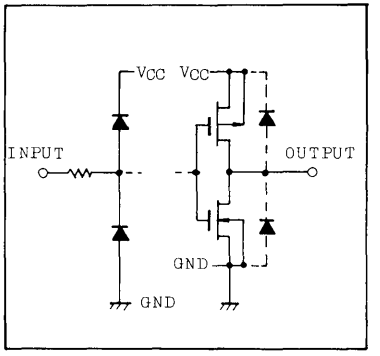


TC74HC4020P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

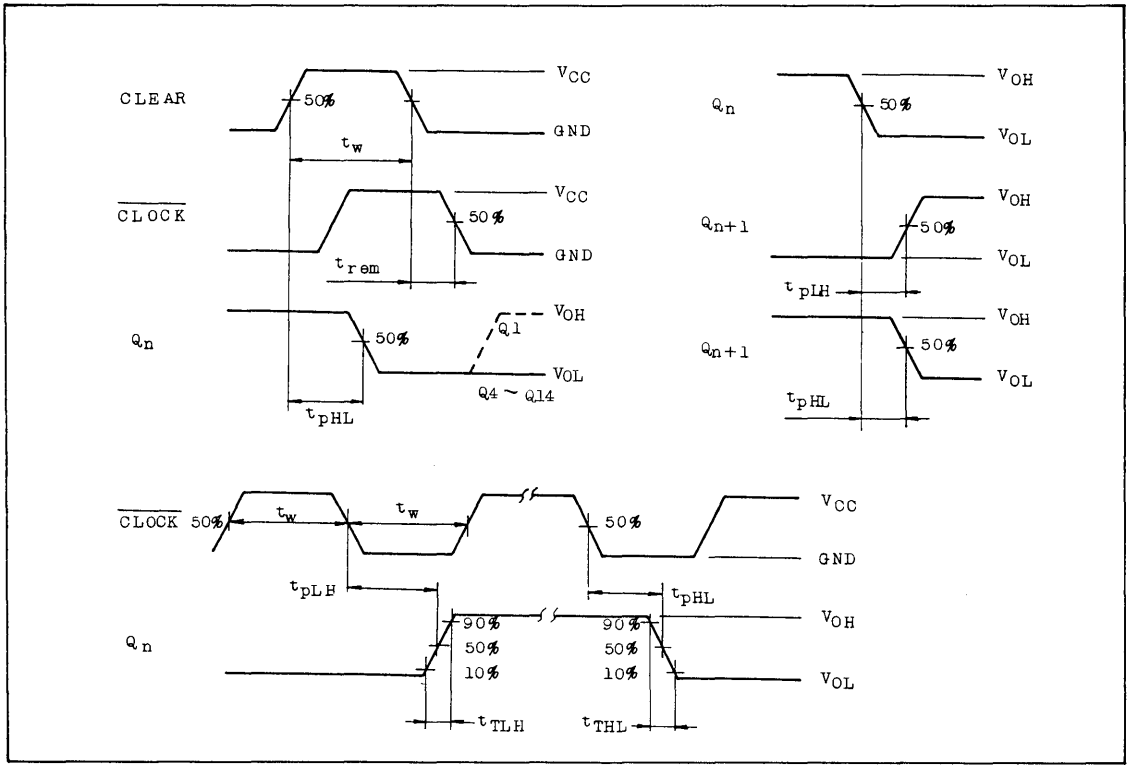
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
($\overline{CLOCK}$ - Q_1)	t_{pHL}		6.0	-	15	25	-	31	
Propagation Delay Time	t_{pLH}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
(Q_n - Q_{n+1})	t_{pHL}		6.0	-	8	13	-	16	
Propagation Delay Time	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	50	
(CLEAR)			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
($\overline{CLOCK}$)	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
(CLEAR)			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	23	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

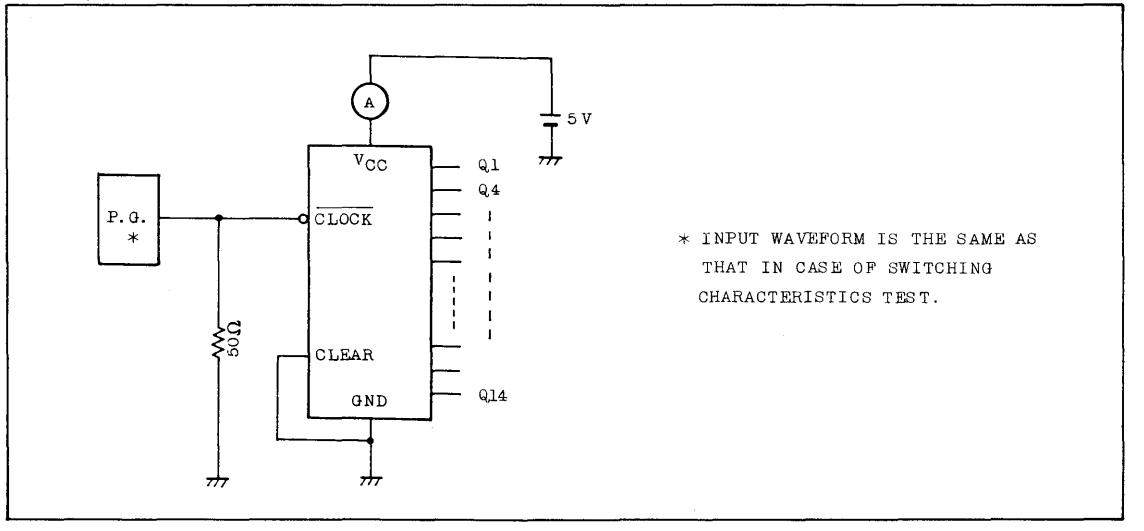
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4020P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4022P

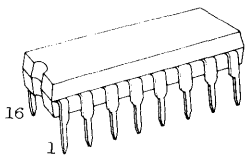
PRELIMINARY

TC74HC4022P OCTAL COUNTER/DIVIDER

The TC74HC4022 is a high speed CMOS OCTAL COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. It contains 4-stage divide-by-8 Johnson counter with 8 decoded output ($Q_0 - Q_7$) and Carry-out bit.
This counter is advanced on the positive edge of clock signal when $\overline{\text{CLOCK ENABLE}}$ input is held low, or is advanced on the negative edge of clock enable signal when CLOCK input is held high, and the selected one of eight outputs goes high.
Holding high the CLEAR input, this counter is cleared to its zero state without regard to the other input conditions.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=43MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}= 4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4022B



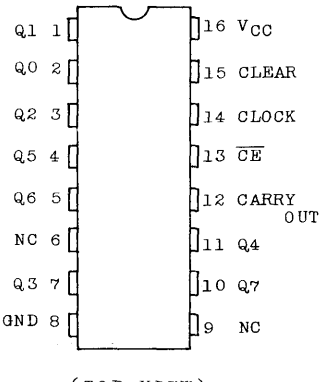
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

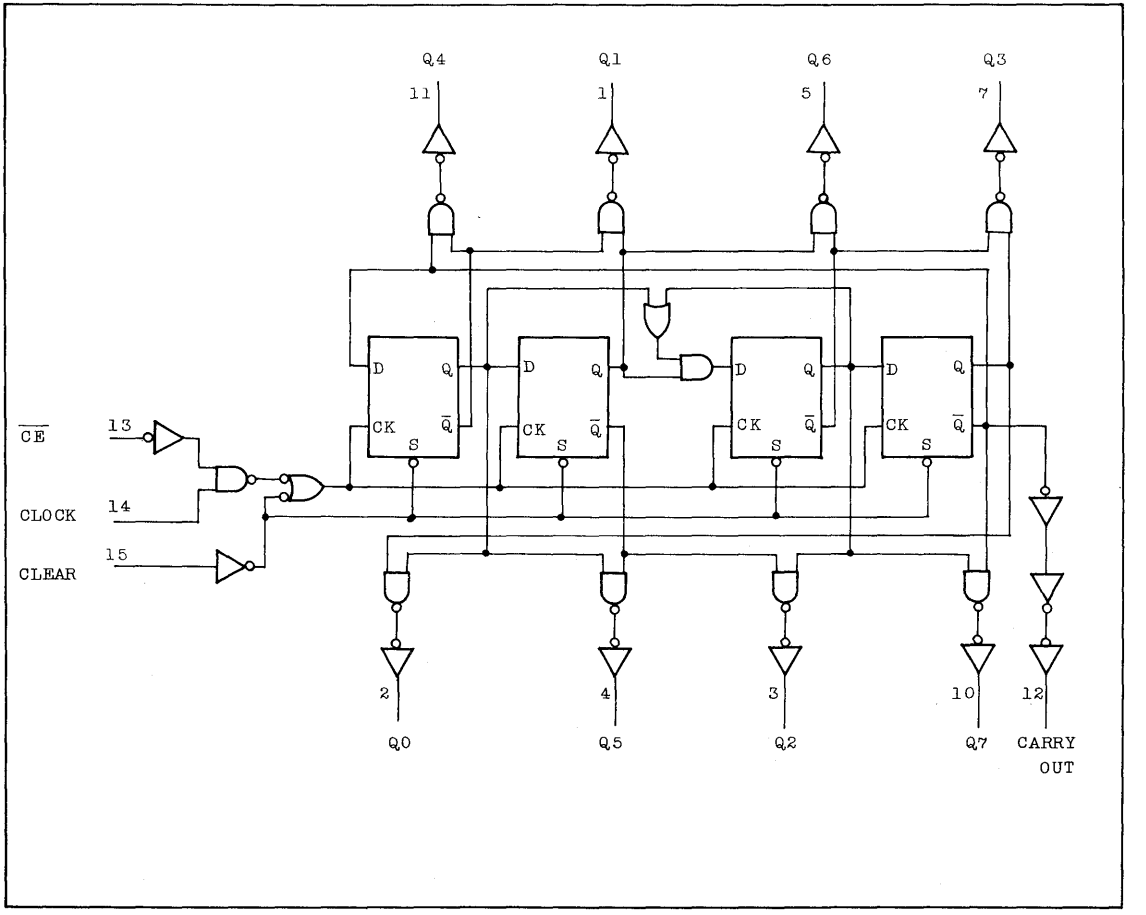
TC74HC4022P

TRUTH TABLE

CLOCK	$\overline{CE}$	CLEAR	DECODE OUTPUT (H)
X	X	H	Q0
L	X	L	Qn
X	H	L	Qn
↓	L	L	Qn+1
↑	L	L	Qn
H	↓	L	Qn
H	↑	L	Qn+1

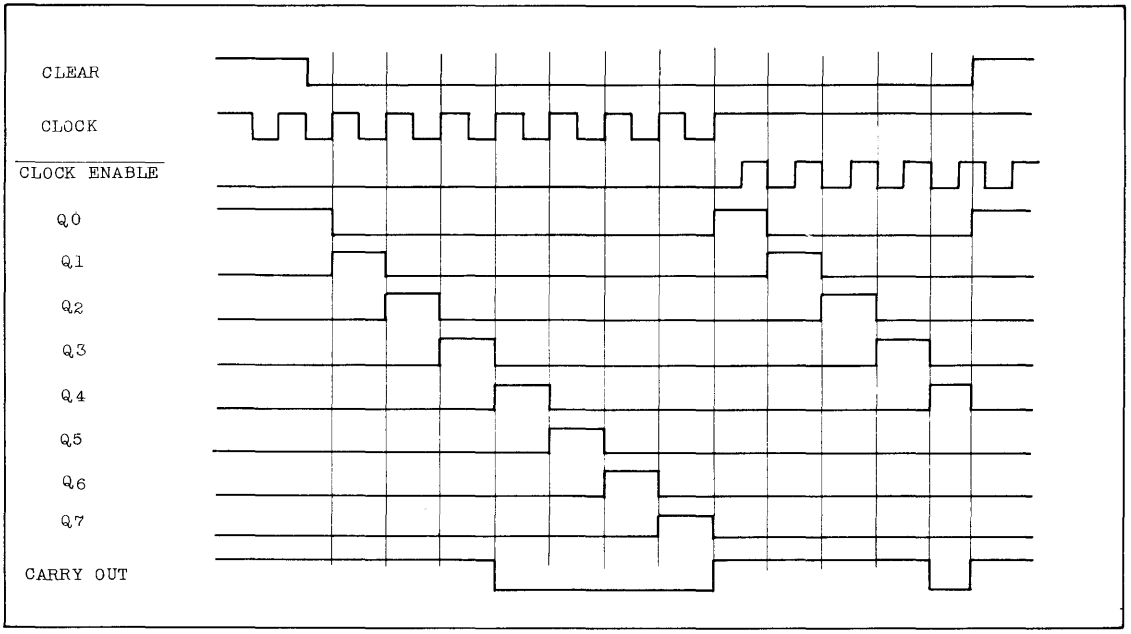
X : DON'T CARE
Qn : NO CHANGE

LOGIC DIAGRAM



TC74HC4022P

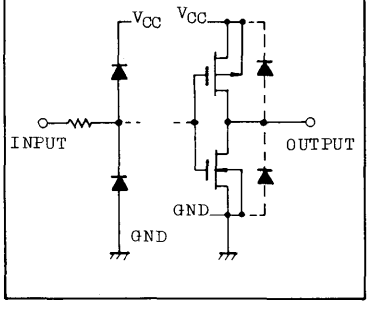
TIMING CHART



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4022P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Suppl Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ∿ 85°C MIN.	-40 ∿ 85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Propagation Delay Time (CLEAR - Q, CARRY)	t_{PLH} t_{PHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	

AC ELECTRICAL CHARACTERISTICS (Continued)

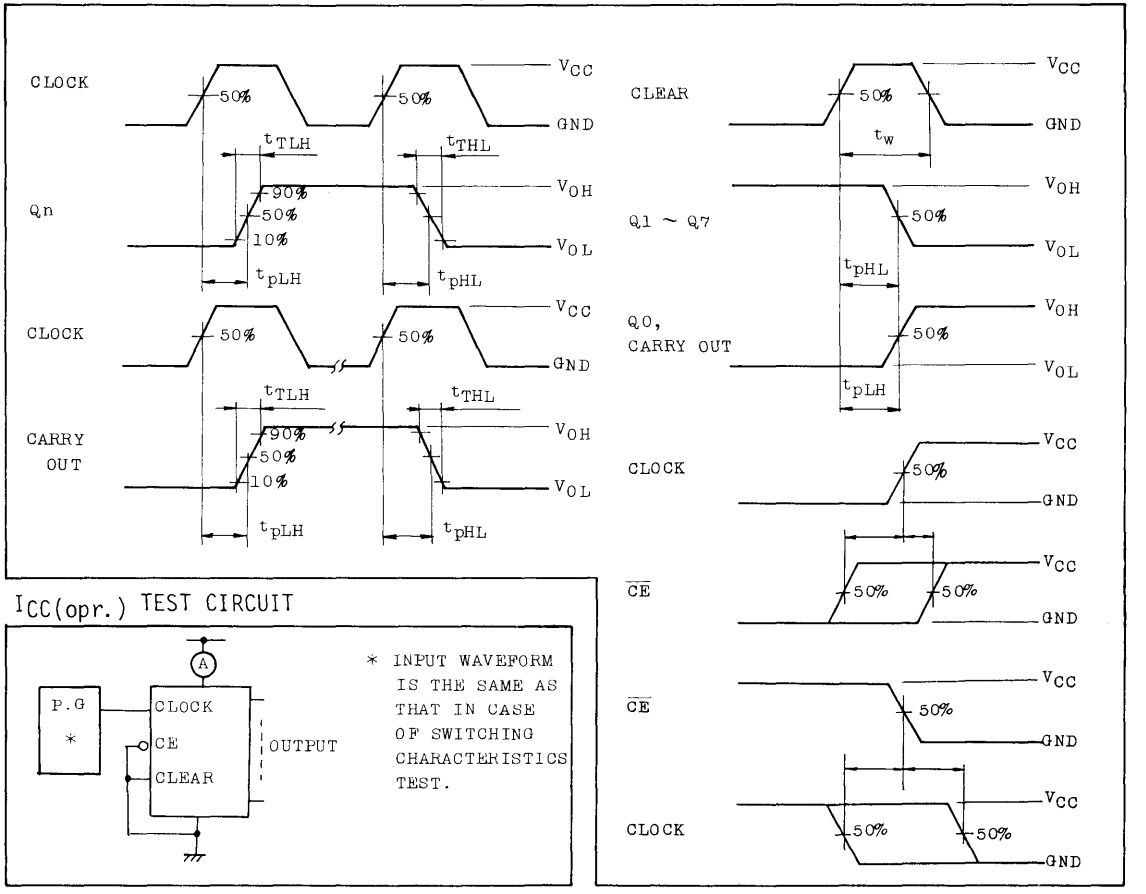
PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ∿ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock frequency	f_{MAX}		2.0	5	10	-	4	-	MHz
			4.5	25	40	-	20	-	
			6.0	29	47	-	24	-	
Minimum Pulse Width (CLOCK)	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Set-up Time	t_s		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Hold Time	t_h		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	52	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4022P

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT

* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4024P

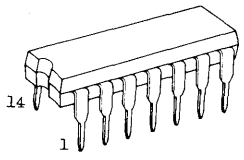
PRELIMINARY

TC74HC4024P 7-STAGE BINARY COUNTER

The TC74HC4024 is a high speed CMOS 7-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4024B) with the same power dissipation.
A clear input is used to reset the counter to the all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the $\overline{CLOCK}$ input brings one increment to the counter. Seven kinds of divided output are provided; 1'st and 4 stage thru 7 stage. And at the last stage, 1/128 divided frequency will be obtained.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 4024B.



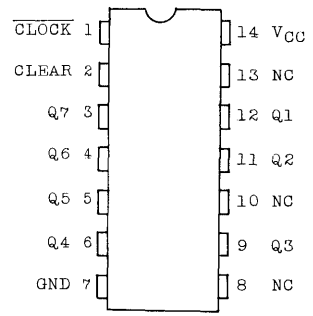
DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

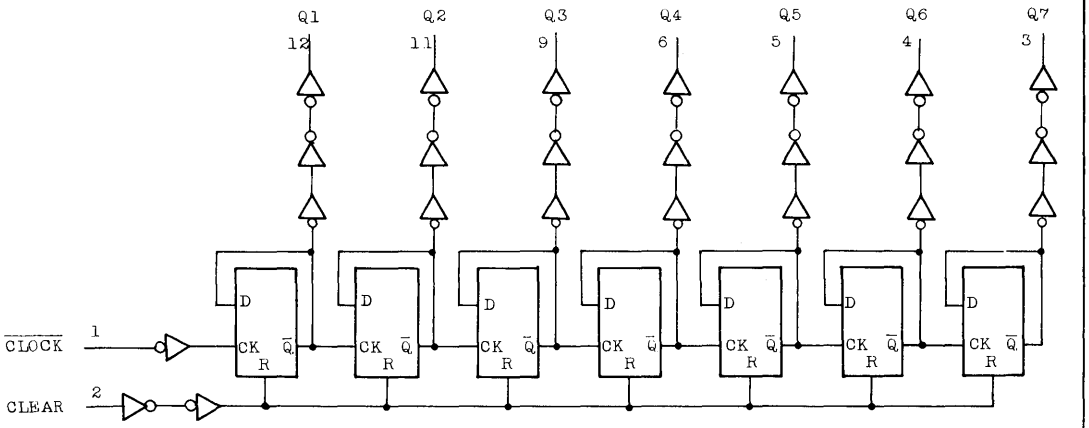
TC74HC4024P

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADVANCE TO NEXT STATE

X : DON'T CARE

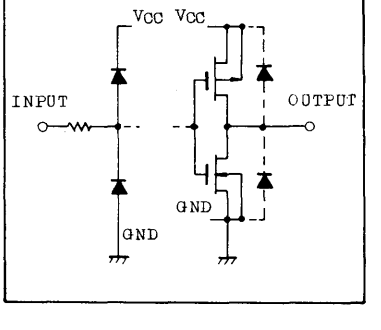
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4024P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{CLOCK}$ - Q1)	t_{pLH} t_{pHL}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
			6.0	-	15	25	-	31	
Propagation Delay Time (Qn - Qn+1)	t_{pLH} t_{pHL}		2.0	-	28	60	-	75	
			4.5	-	7	12	-	15	
			6.0	-	6	10	-	13	
Propagation Delay Time (CLEAR - Qn)	t_{pHL}		2.0	-	96	185	-	230	
			4.5	-	24	37	-	46	
			6.0	-	20	31	-	39	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width ($\overline{CLOCK}$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	

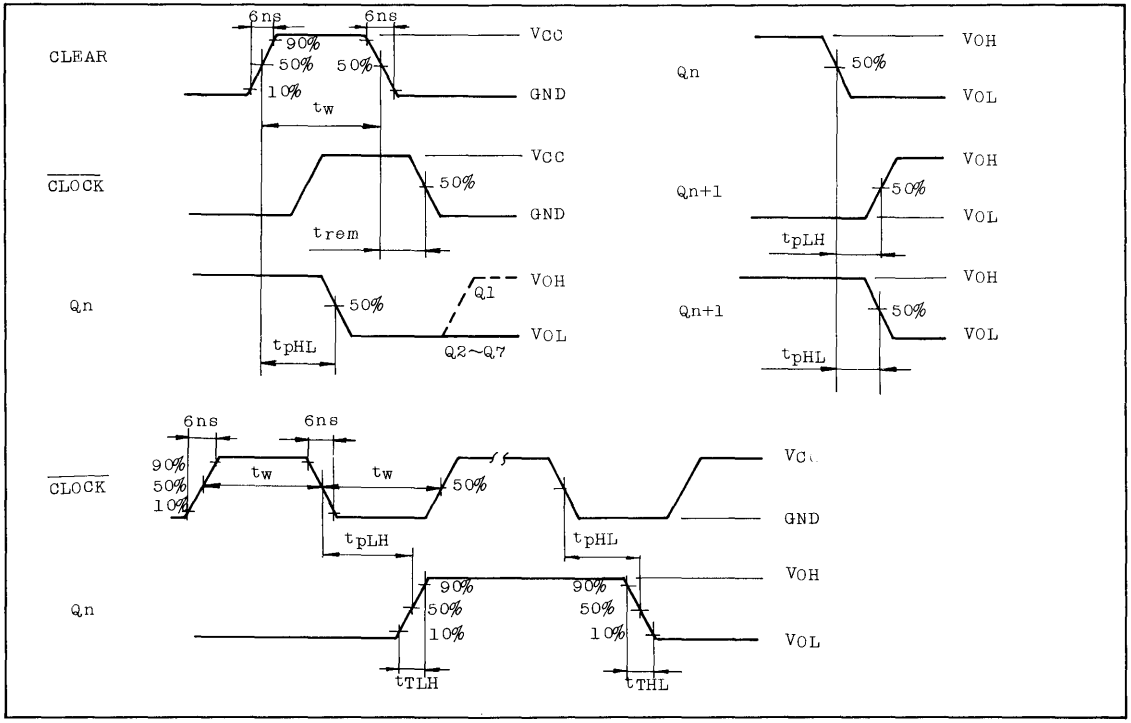
TC74HC4024P

AC ELECTRICAL CHARACTERISTICS (Continued)

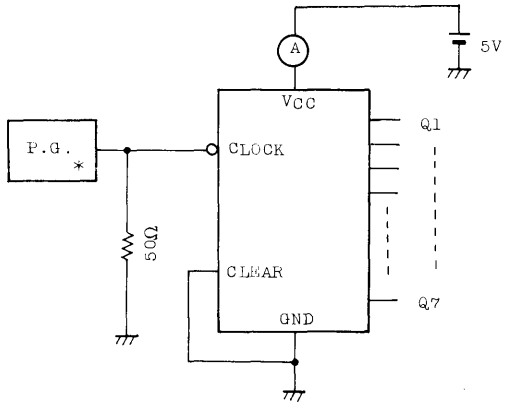
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time	t_{rem}		2.0	-	15	50	-	65	
			4.5	-	3	10	-	13	
			6.0	-	3	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	42	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder. $I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4028P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

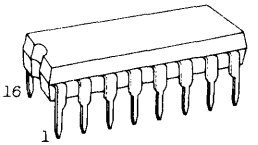
PRELIMINARY

TC74HC4028P/F BCD-TO-DECIMAL DECODER

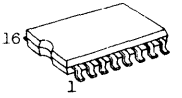
The TC74HC4028 is a high speed CMOS DECIMAL DECODER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
A BCD code applied to the four input (A thru D) provides a high level at the selected one of the decimal decoded outputs. A illegal BCD code such as eleven to fifteen gives a low level at all outputs.
The device also can be used as 3-to-8 LINE DECODER, when D input is assigned as a disable input.
The device is useful for code conversion, address decoding, memory selection, demultiplexing, or read out decoding.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed.....t_{pd}=25ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays.....$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range....$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4028B

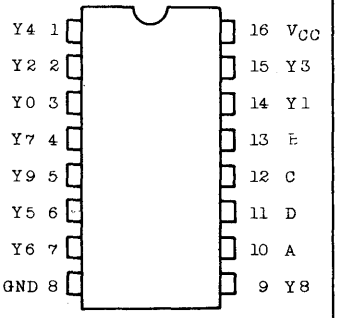


DIP16(3D16A-P)



MFP16(F16GC-P)

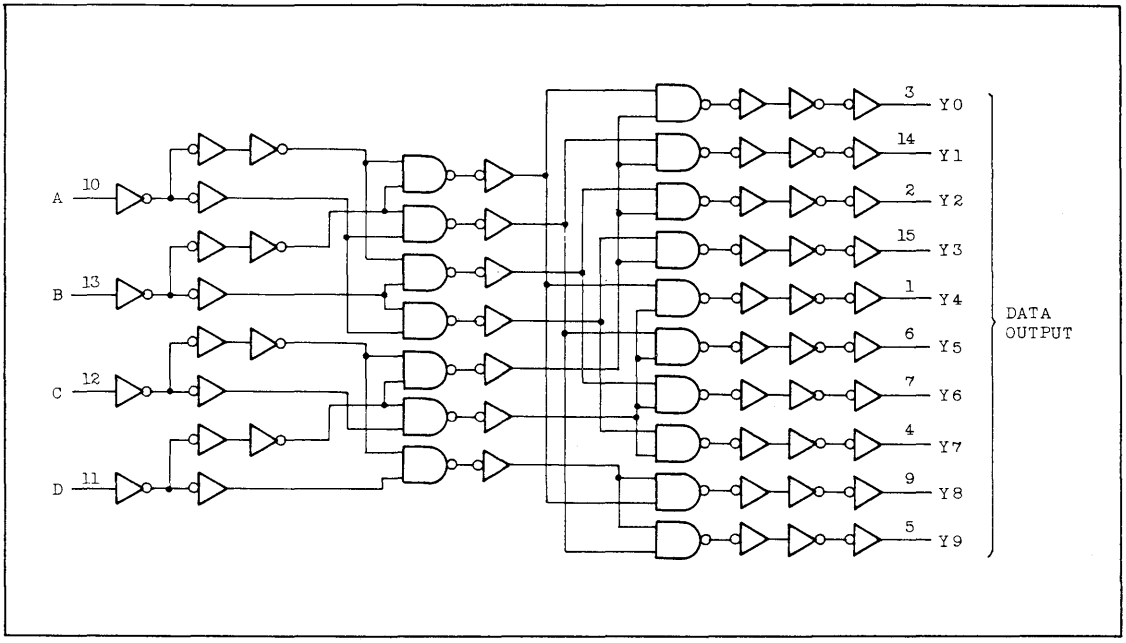
PIN ASSIGNMENT



(Top View)

TC74HC4028P/F

LOGIC DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS										SELECTED OUTPUT
D	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	Y_0
L	L	L	H	L	H	L	L	L	L	L	L	L	L	Y_1
L	L	H	L	L	L	H	L	L	L	L	L	L	L	Y_2
L	L	H	H	L	L	L	H	L	L	L	L	L	L	Y_3
L	H	L	L	L	L	L	L	H	L	L	L	L	L	Y_4
L	H	L	H	L	L	L	L	L	H	L	L	L	L	Y_5
L	H	H	L	L	L	L	L	L	L	H	L	L	L	Y_6
L	H	H	H	L	L	L	L	L	L	L	H	L	L	Y_7
H	L	L	L	L	L	L	L	L	L	L	L	H	L	Y_8
H	L	L	H	L	L	L	L	L	L	L	L	L	H	Y_9
H	X	H	X	L	L	L	L	L	L	L	L	L	L	NOTE
H	H	X	X	L	L	L	L	L	L	L	L	L	L	NOTE

X : Don't care

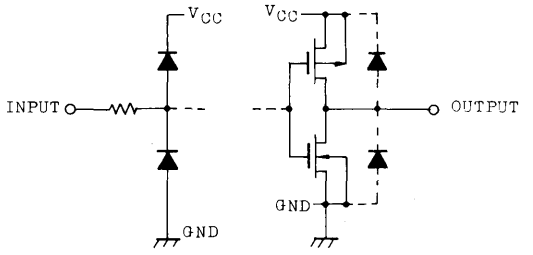
TC74HC4028P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	Topr	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

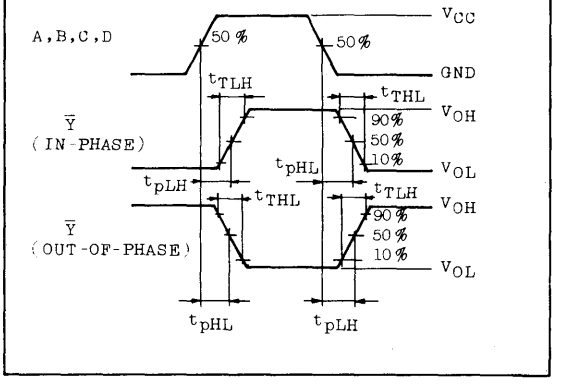
TC74HC4028P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

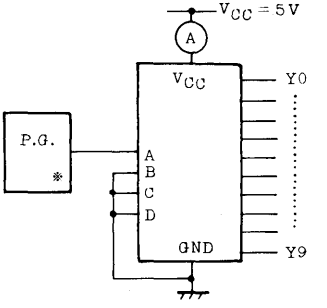
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (A,B,C,D)	t_{pLH} t_{pHL}		2.0	-	116	225	-	280	
			4.5	-	29	45	-	56	
			6.0	-	25	38	-	48	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	58	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



* Input transition time is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4040P/F

PRELIMINARY

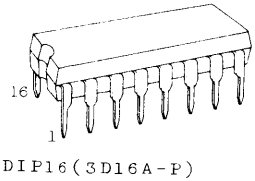
TC74HC4040P/F 12-STAGE BINARY COUNTER

GENERAL DESCRIPTION

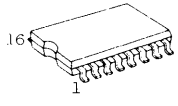
The TC74HC4040 is a high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C^2MOS technology.
It operates approximately ten times as fast as that of metal-gate CMOS IC (4040B) with the same power dissipation.
A clear input is used to reset the counter to all low level state. A high level at CLEAR accomplishes the reset function. A negative transition on the CLOCK input brings one increment to the counter. All divided output stages are provided, and 1/4096 divided frequency will obtained at the last stage.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{max}=60MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ... $|I_{OH}|=I_{OL}$=4mA (Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr)}$=2V ∿ 6V
- Pin and Functional Compatible with 4040B.



DIP16(3D16A-P)



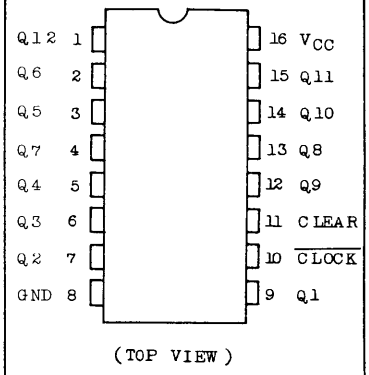
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

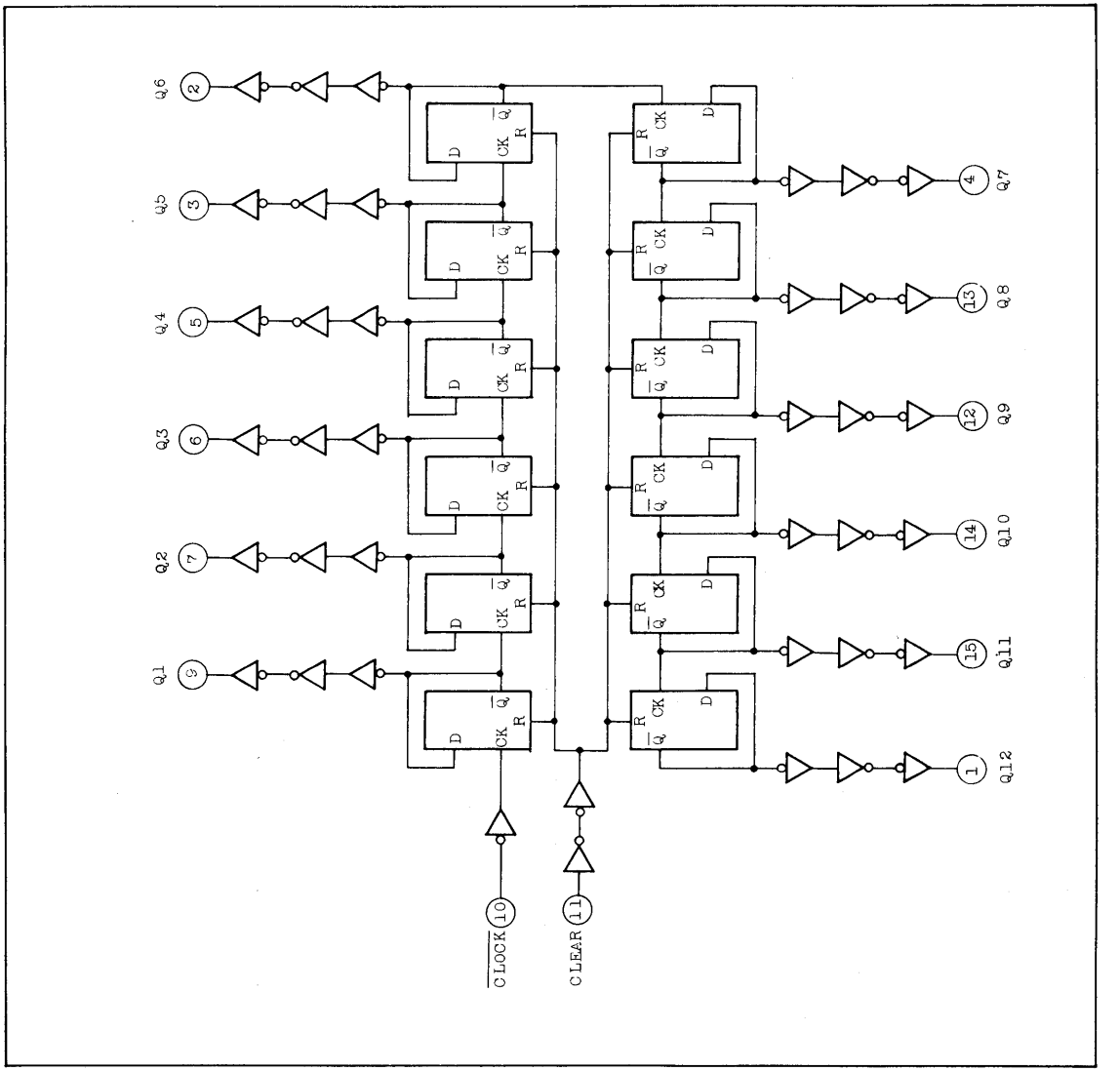
TC74HC4040P/F

TRUTH TABLE

$\overline{CLOCK}$	CLEAR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↑	L	NO CHANGE
↓	L	ADVANCE TO NEXT STATE

X : DON'T CARE

LOGIC DIAGRAM

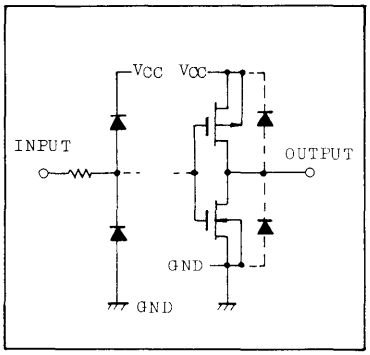


TC74HC4040P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC4040P/F

AC ELECTRICAL CHARACTERISITCS (C_L=50pF, Input $t_r=t_f$=6ns)

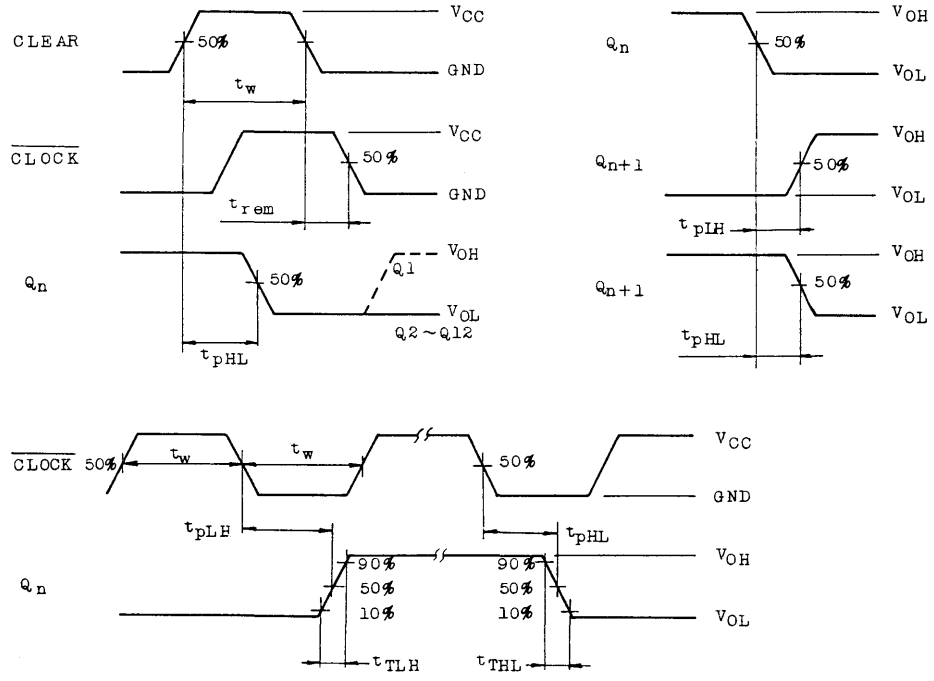
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	72	145	-	180	
			4.5	-	18	29	-	36	
($\overline{CLOCK}$ - Q_1)	t_{pHL}		6.0	-	15	25	-	31	
Propagation Delay Time	t_{pLH}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
(Q_n - Q_{n+1})	t_{pHL}		6.0	-	8	13	-	16	
Propagation Delay Time	t_{pHL}		2.0	-	104	205	-	225	
			4.5	-	26	41	-	50	
(CLEAR)			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	
Minimum Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
($\overline{CLOCK}$)	$t_{w(H)}$		6.0	-	7	13	-	16	
Minimum Pulse Width	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
(CLEAR)			6.0	-	13	21	-	26	
Minimum Removal Time	t_{rem}		2.0	-	-	50	-	65	
			4.5	-	-	10	-	13	
			6.0	-	-	9	-	11	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	32	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

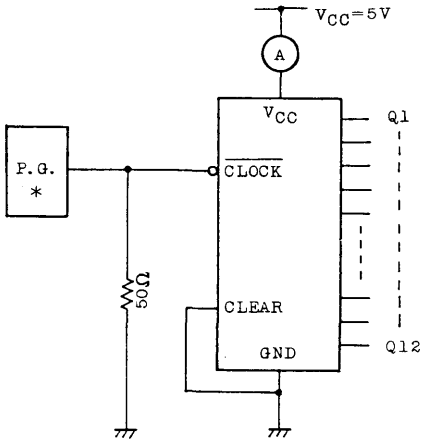
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4040P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

TC74HC4049P/F
TC74HC4050P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

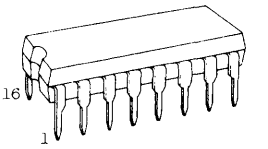
TC74HC4049 P/ F HEX BUFFER/CONVERTER (INVERTING)

TC74HC4050 P/ F HEX BUFFER CONVERTER

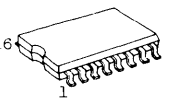
The TC74HC4049 and the TC74HC4050 are high speed CMOS HEX BUFFER fabricated with silicon gate C²MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The TC74HC4049 is an inverting buffer, while the TC74HC4050 is a non-inverting buffer.
The internal circuit is composed of 3-stage or 2-stage inverters, which enables high noise immunity and stable output.
Input protection circuits are different from those of the high speed CMOS IC's.
They eliminate diodes of V_{CC} side and enable logic-level conversion from high-level voltage (up to 8V) to low-level voltage.
These IC's are useful for battery back up circuits, because input voltage can be appled on IC's which is not biased by V_{CC}.

FEATURES:

- High Speed.....t_{pd}=10ns(Typ.) at V_{CC}=5V
- Low Power Dissipation.....I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity.....$V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability.....15 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with 4049B, 4050B.



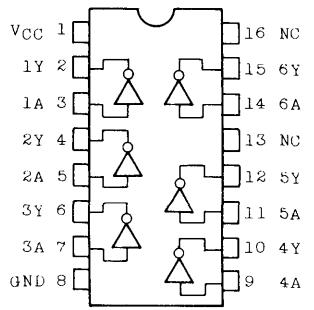
DIP16(3D16A-P)



MFP16(F16GC-P)

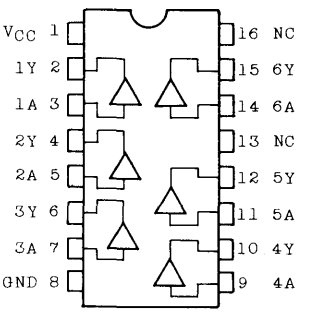
PIN ASSIGNMENT

TC74HC4049



(TOP VIEW)

TC74HC4050

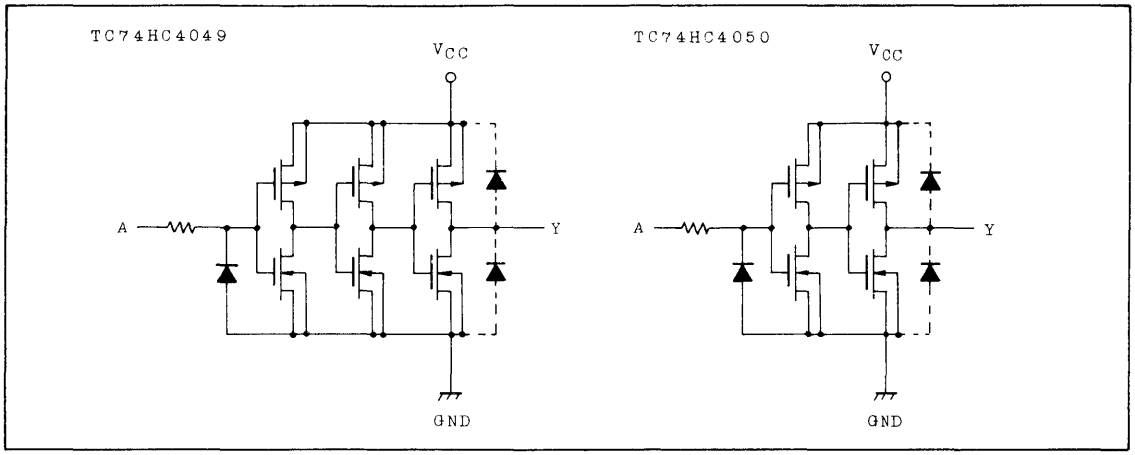


(TOP VIEW)

NC : No Connection

TC74HC4049P/F
TC74HC4050P/F

CIRCUIT SCHEMATIC (per Gate)



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ 10*	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±35	mA
DC V_{CC}/Ground Current	I_{CC}	±70	mA
Power Dissipation	P_D	500(DIP)**/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

Note.
*DC input voltage is able to impress -0.5V to 10V based on GND without any relation to voltage of V_{CC}. Recommended operating condition is from 0V to 8V and it is possible to vonvert logic-level from 8V to 5V or 5V to 2V.

**500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

TC74HC4049P/F
TC74HC4050P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-7.8mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=6mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=7.8mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	1.0	-	10.0	

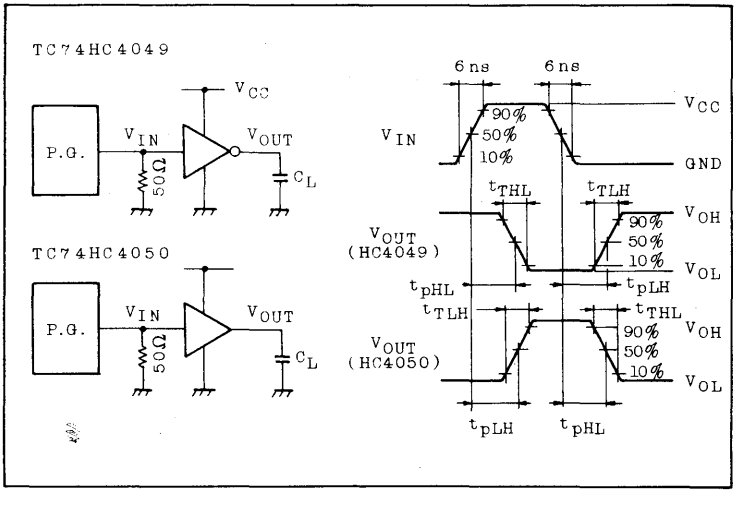
TC74HC4049P/F
TC74HC4050P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

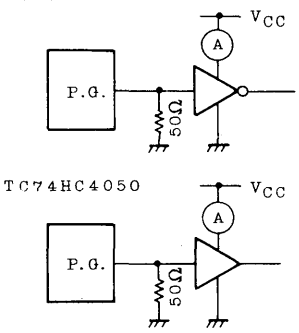
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	25	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/6$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(opr)}$ TEST CIRCUIT



Input waveform is the same as that in case of switching characteristics test.

TC74HC4060P/F C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC4060P/F 14-STAGE BINARY COUNTER/DIVIDER WITH OSCILLATOR

The TC74HC4060 is a high speed CMOS 14-STAGE BINARY COUNTER fabricated with silicon gate C²MOS technology.

It operates ten times as fast as that of metal-gate C²MOS IC (4060BP) with the same power dissipation.

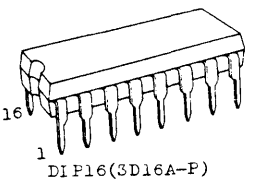
The oscillator configuration allows designs of either RC or crystal oscillator circuits. A clear input is used to reset the counter to the all low level state and disable the oscillator. A high level at CLEAR accomplishes the reset function.

A negative transition on the clock input incliments the counter. Ten kinds of divided output are provided; 4 stage thru 10 stage and 12 stage thru 14 stage. And at the last stage, 1/16384 **divided** frequency is obtained.

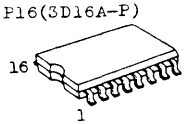
The $\overline{\phi}_I$ input and the CLEAR input are equipped with protection circuits against static dischage or transient excess voltage.

FEATURES:

- High Speed.....f_{max}=60MHz(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=4μA(Max.) (Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance..$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays...$t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range..$V_{CC(opr)}$=2V ~ 6V
- Oscillator Configulation .....RC or Crystal Oscillator
- Schmitt Trigger Clock Input
- Pin and Function Compatible with 4060B



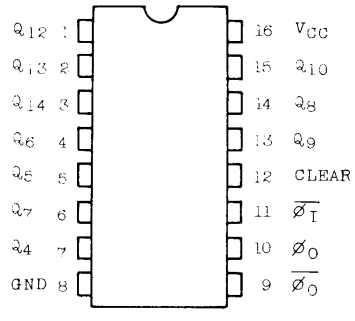
DIP16(3D16A-P)



MFP16(F16GC-P)

TC74HC4060P/F

PIN ASSIGNMENT



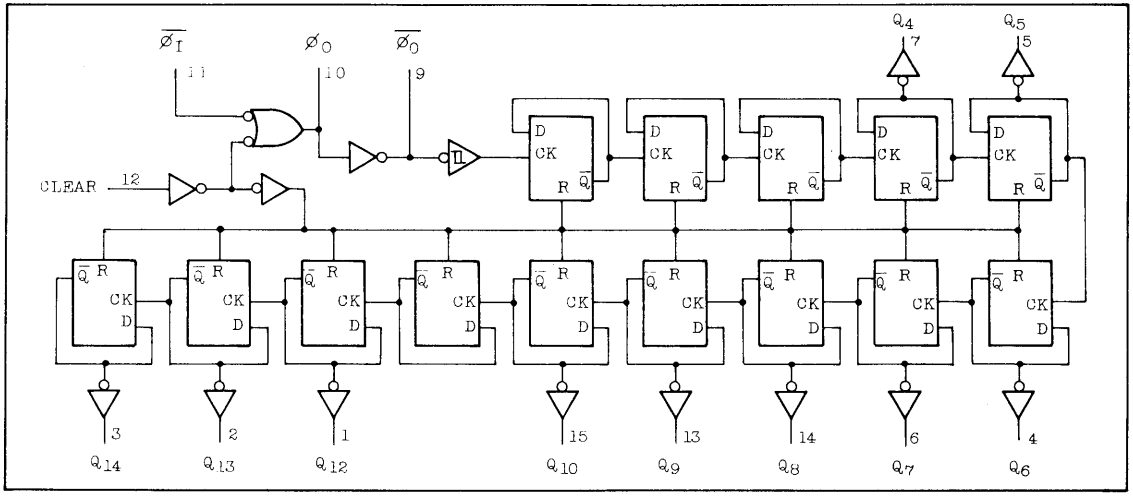
(Top View)

TRUTH TABLE

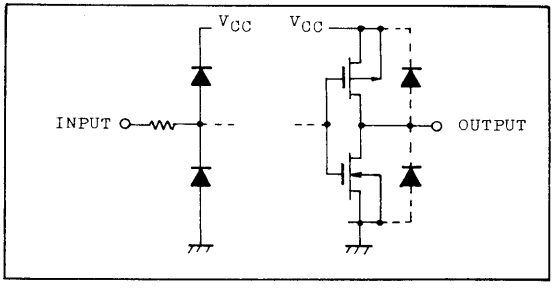
INPUTS		FUNCTION
$\overline{\phi}_I$	CLEAR	
x	H	Counter is reset to zero state. ϕ_0 output goes to high level $\overline{\phi}_0$ output goes to low level
↓	L	Count up one step.
↑	L	No change.

x Don't care

LOGIC DIAGRAM



INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4060P/F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q Outputs)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.8	2.0	-	1.8	-	V
				4.5	4.0	4.5	-	4.0	-	
				6.0	5.5	5.9	-	5.5	-	
Low-Level Output Voltage (Q Outputs)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Low-Level Output Voltage (ϕ_O, $\overline{\phi}_O$ Output)	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.2	-	0.2	V
				4.5	-	0.0	0.5	-	0.5	
				6.0	-	0.1	0.5	-	0.5	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time (Q Outputs)	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time $\overline{\phi}_I$ - Q_4	t_{pLH} t_{pHL}		2.0	-	196	370	-	465	
			4.5	-	49	74	-	93	
			6.0	-	42	63	-	79	
Q_n - Q_{n+1}	t_{pLH} t_{pHL}		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
CLEAR - Q_n	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Maximum Clock Frequency	f_{MAX}		2.0	6	14	-	5	-	MHz
			4.5	30	55	-	24	-	
			6.0	35	65	-	28	-	

TC74HC4060P/F

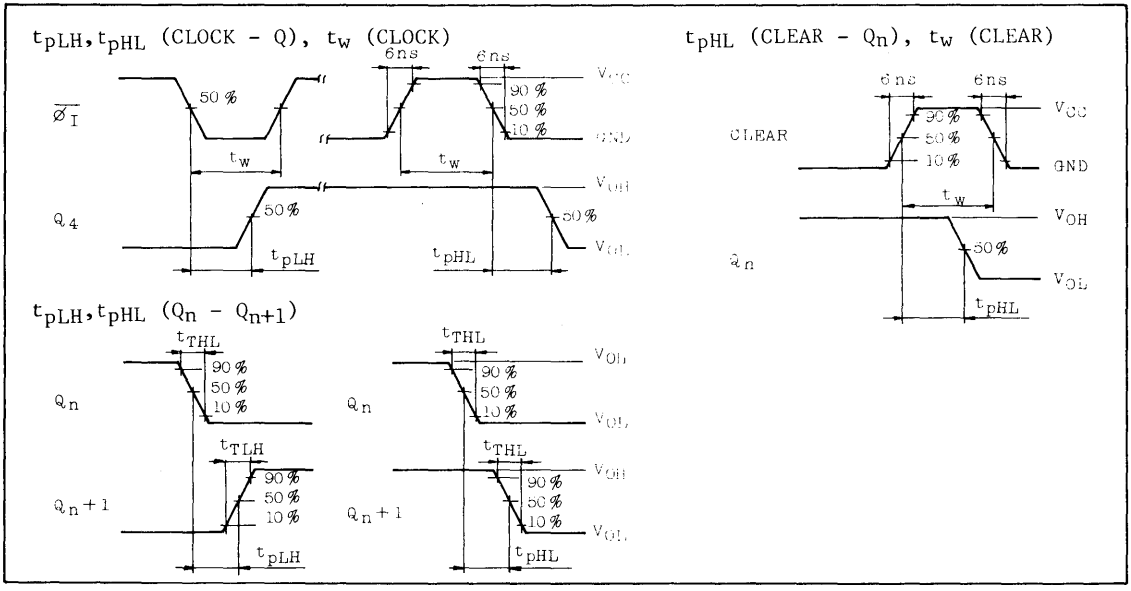
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns) (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width CLOCK ($\overline{\phi}_I$)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
CLEAR	$t_{w(H)}$		2.0	-	60	125	-	155	
			4.5	-	15	25	-	31	
			6.0	-	13	21	-	26	
Minimum Removal Time CLEAR	t_{rem}		2.0	-	40	100	-	125	
			4.5	-	10	20	-	25	
			6.0	-	9	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	33	-	-	-	

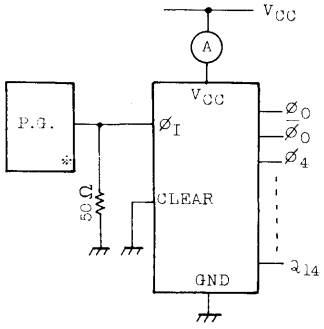
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



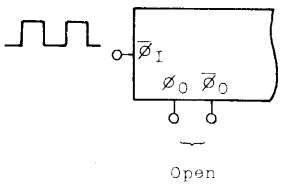
* $\overline{\phi}_I$ input $t_r=t_f=6ns$ Duty=50%

Note

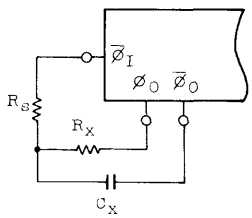
When CR or crystal oscillation circuit is adopted, the dynamic power dissipation will be greater than the measured value from the test circuit shown left, because these oscillion circuits spend much supply current.

TYPICAL CLOCK DRIVE CIRCUITS

EXTERNAL CLOCK DRIVE

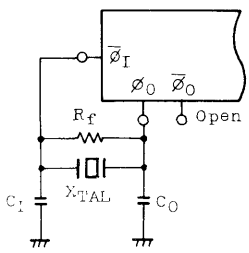


TYPICAL RC CIRCUIT



R_S : $2R_X \sim 10R_X$

TYPICAL CRYSTAL CIRCUIT



TC74HC4066P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC4066P/F QUAD BILATERAL SWITCH

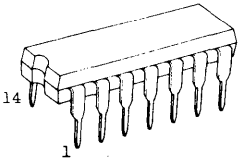
The TC74HC4066 is a high speed CMOS QUAD BILATERAL SWITCH fabricated with silicon gate C²MOS technology.

It consists of four independent high speed switches capable of controlling either digital or analog signals with as low power dissipation as that of metal-gate C²MOS IC.

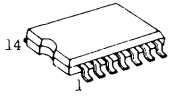
C input is provided to control the switch; the switch is ON while the C input is maintained at high level, and the switch is OFF while at low level.

FEATURES:

- High Speed.....t_{pd}=12ns(Typ.) (V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.) (Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Low ON Resistance.....R_{ON}=80Ω(Typ.) (V_{CC}=5V)
- High Degree of Liniarity.....DISTORTION=0.05%(Typ.) (V_{CC}=5V)
- Pin and Function Compatible with 4066B

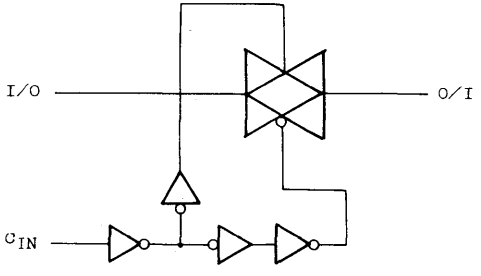


DIP14(3D14A-P)

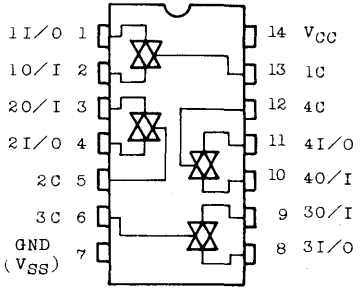


MFP14(F14GB-P)

LOGIC DIAGRAM (PER CHANNEL)



PIN ASSIGNMENT



(Top View)

TC74HC4066P/F

ABSOLUTE MAXIMUM RATINGS

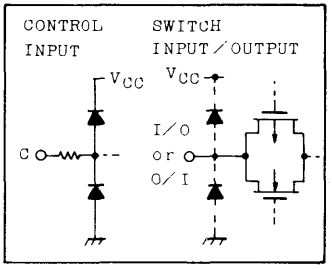
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Control Input Voltage	V_{IH}	Refer to R_{ON} specification	2.0	1.5	-	-	1.5	-	V
			4.5	3.15	-	-	3.15	-	
			6.0	4.2	-	-	4.2	-	
Low-Level Control Input Voltage	V_{IL}	$\|I_{OFF}\| \leqq 1.0\mu A$	2.0	-	-	0.5	-	0.5	V
			4.5	-	-	1.35	-	1.35	
			6.0	-	-	1.8	-	1.8	
ON Resistance	R_{ON}	$V_C=V_{IHC}$ $V_{I/O}=0 \sim V_{CC}$ $I_{I/O}=100\mu A$	2.0	-	2000	-	-	-	Ω
			4.5	-	100	200	-	250	
			6.0	-	60	170	-	210	
Difference of ON Resistance Between Any Two of Four Switches	ΔR_{ON}	$V_C=V_{IHC}$ $I_{I/O}=100\mu A$	2.0	-	50	-	-	-	
			4.5	-	3	-	-	-	
			6.0	-	2	-	-	-	

TC74HC4066P/F

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Input/Output Leakage Current (Switch OFF)	I_{OFF}	$V_C=V_{ILC}$ $V_{I/O}=6V$, $V_{O/I}=0V$ or $V_{I/O}=0V$, $V_{O/I}=6V$	6.0	-	-	±0.1	-	±0.1	μA
Input Leakage Current	I_{IN}		6.0	-	-	±0.1	-	±1.0	
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND	6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

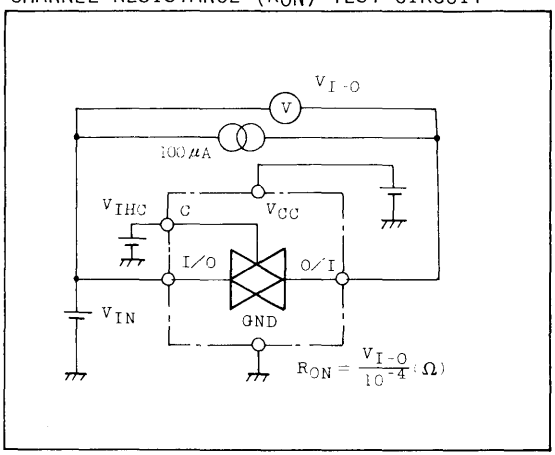
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (Input to Output)	t_{pLH} t_{pHL}	R_L=10kΩ	2.0	-	13	50	-	65	ns
			4.5	-	5	10	-	13	
			6.0	-	4	9	-	11	
Output Enable Time	t_{pZH} t_{pZL}	R_L=1kΩ	2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Output Disable Time	t_{pLZ} t_{pHZ}	R_L=1kΩ	2.0	-	64	115	-	145	
			4.5	-	16	23	-	29	
			6.0	-	14	20	-	25	
Sine Wave Distortion		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=10kΩ f=1kHz	2.5	-	0.05	-	-	-	%
Frequency Response (Switch ON) $20\log_{10}\frac{V_{out}}{V_{in}}$=-3dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	30	-	-	-	MHz
Feedthrough Attenuation (Switch OFF) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V V_{in}=0.88V_{RMS} R_L=1kΩ	2.5	-	1.0	-	-	-	
Crosstalk (Control Input to Signal Output)		R_{IN}=1kΩ R_L=10kΩ	2.0	-	25	-	-	-	mV
			4.5	-	60	-	-	-	
			6.0	-	75	-	-	-	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns) (CONTINUED)

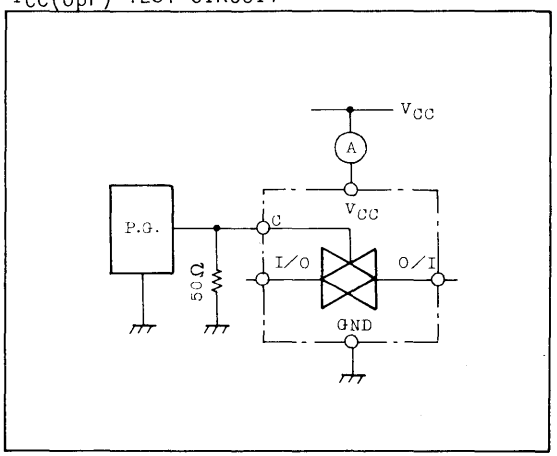
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Cross talk (Between any two switches) $20\log_{10}\frac{V_{out}}{V_{in}}$=-50dB		V_{SS}=-2.5V V_{in}=0.88VRMS R_L=1kΩ	2.5	-	1.5	-	-	-	MHz
Maximum Control Input Frequency		R_L=1kΩ C_L=15pF V_{OUT}=1/2 V_{CC}	2.0	-	20	-	-	-	
			4.5	-	30	-	-	-	
			6.0	-	30	-	-	-	
Control Input Capacitance	C_{IN}			-	5	10	-	10	pF
Switch Input/Output Capacitance	$C_{I/O}$			-	6	-	-	-	
Feedthrough Capacitance	C_{I-O}			-	0.5	-	-	-	
Power Dissipation Capacitance	C_{PD}(1)			-	13	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/4$ (per CHANNEL)

CHANNEL RESISTANCE (R_{ON}) TEST CIRCUIT



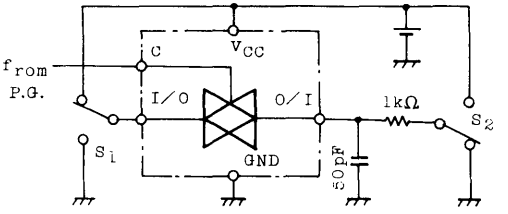
$I_{CC(opr)}$ TEST CIRCUIT

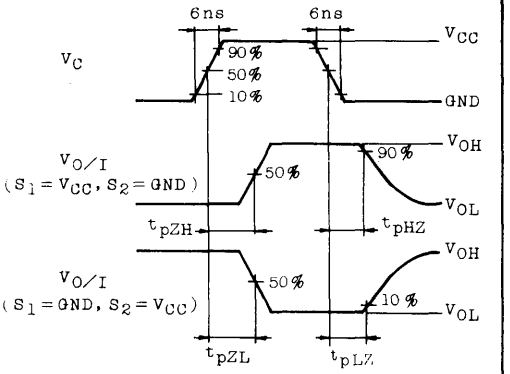


TC74HC4066P/F

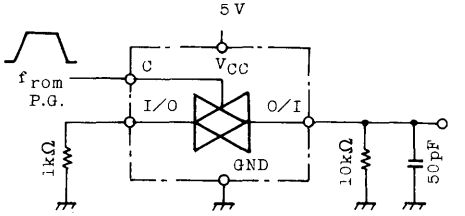
SWITCHING CHARACTERISTICS TEST CIRCUIT

1. t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

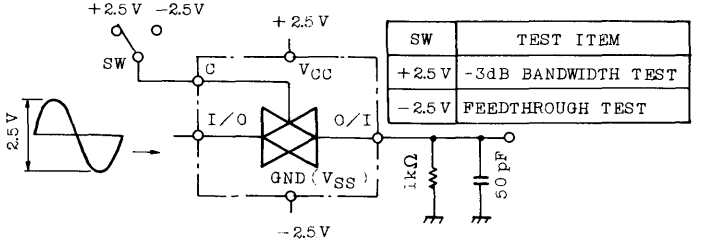




2. CROSSTALK (CONTROL TO OUTPUT)

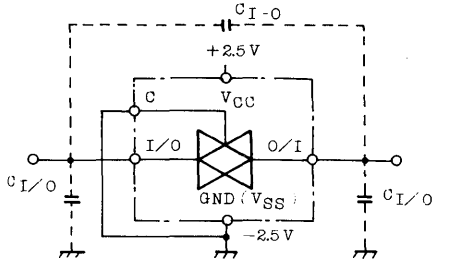


3. BANDWIDTH AND FEEDTHROUGH ATTENUATION

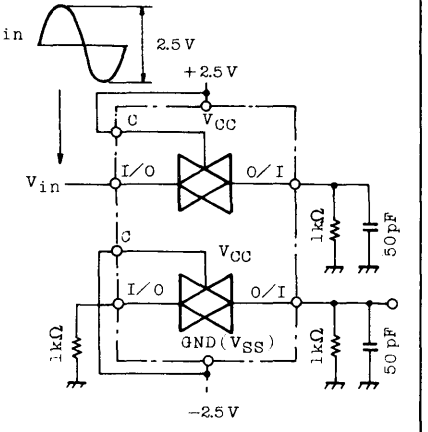


SW	TEST ITEM
+2.5 V	-3dB BANDWIDTH TEST
−2.5 V	FEEDTHROUGH TEST

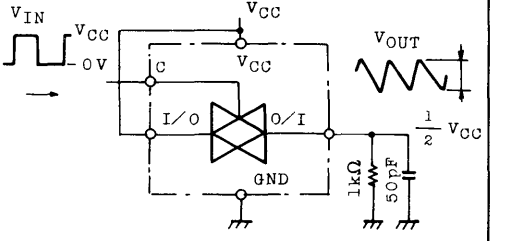
4. C_{I-O}, $C_{I/O}$



5. CROSSTALK BETWEEN ANY TWO SWITCHES



6. MAXIMUM CONTROL FREQUENCY



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4072

PRELIMINARY

TC74HC4072P DUAL 4-INPUT OR GATE

The TC74HC4072 is a high speed CMOS 4-INPUT OR GATE fabricated with silicon gate C²MOS technology.

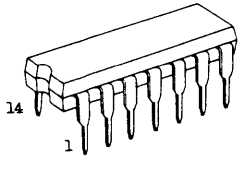
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 3 stage including buffer output, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or excess voltage.

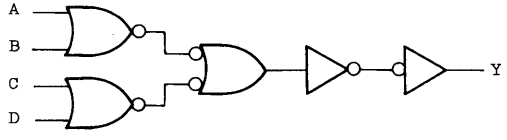
FEATURES:

- High Speed.....t_{pd}=11ns(Typ.)(V_{CC}=5V)
- Low Power Dissipation.....I_{CC}=1μA(Max.)(Ta=25°C)
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance...|I_{OH}|=I_{OL}=4mA(Min.)
- Balanced Propagation Delays....t_{pLH}≒t_{pHL}
- Wide Operating Voltage Range...V_{CC}(opr)=2V～6V
- Pin and Function Compatible with 4072B

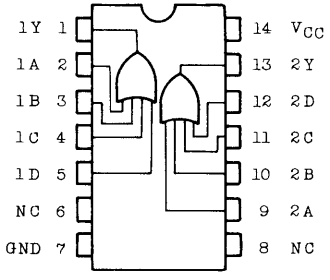


DIP14(3D14A-P)

LOGIC DIAGRAM (1/2 OF DEVICE SHOWN)



PIN ASSIGNMENT



(Top View)

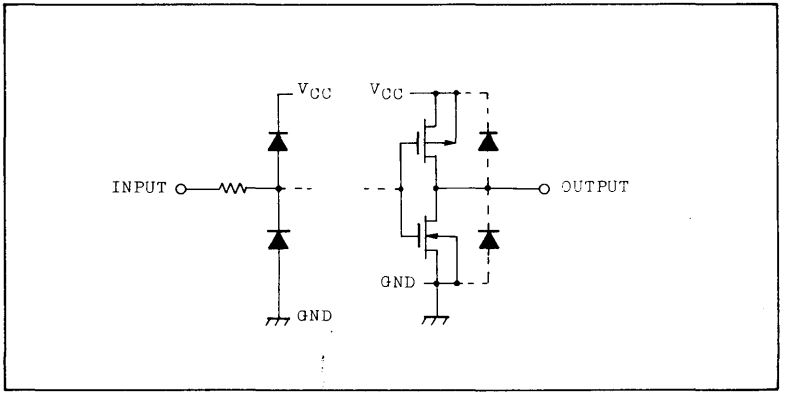
TC74HC4072P

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40 ~ 65°C. and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4072P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	**1.0**	-	**10.0**	

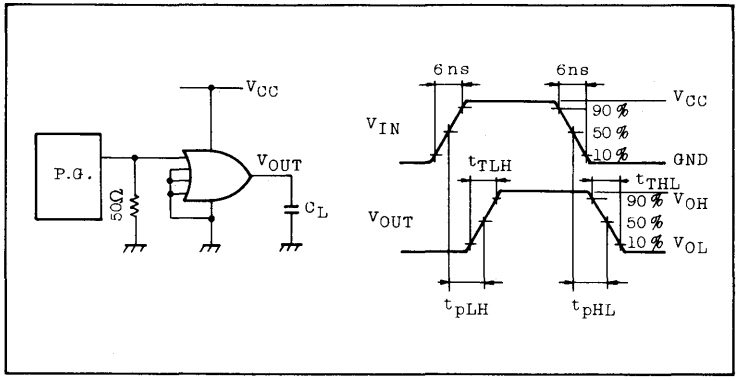
TC74HC4072P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

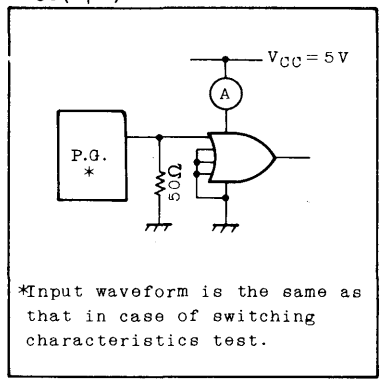
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	56	110	-	140	
			4.5	-	14	22	-	28	
			6.0	-	12	19	-	24	
Input Capacitance	CIN			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.
$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/2$ (per Gate)

SWITCHING CHARACTERISTICS TEST CIRCUIT and WAVEFORM



$I_{CC(opr)}$ TEST CIRCUIT



*Input waveform is the same as that in case of switching characteristics test.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4075P/F

PRELIMINARY

TC74HC4075P/FTRIPLE 3-INPUT OR GATE

The TC74HC4075 is a high speed CMOS 3- INPUT OR GATE fabricated with silicon gate C^2MOS technology.

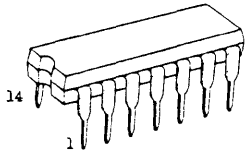
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

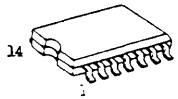
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}= 9 ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... t_{pLH}≒t_{PHL}
- Wide Operating Voltage Range ..... V_{CC}(Opr.)=2V∿6V
- Pin and Function Compatible with 4075B



DIP14(3D14A-P)

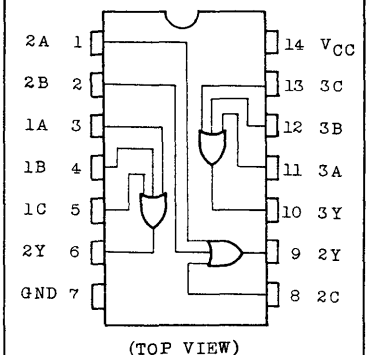


ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

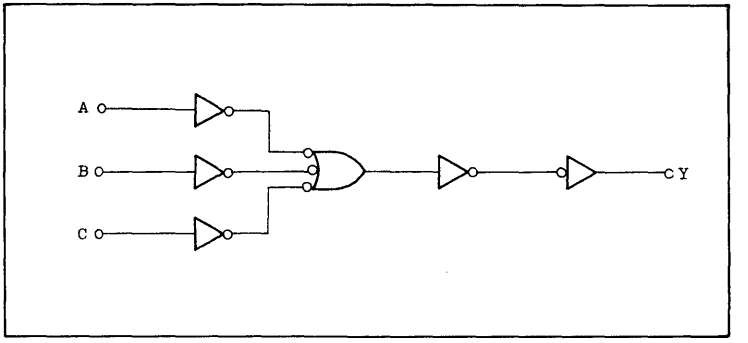
PIN ASSIGNMENT



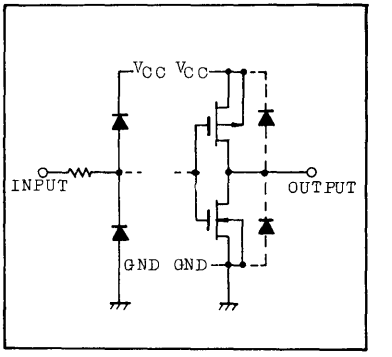
(TOP VIEW)

TC74HC4075P

LOGIC DIAGRAM



INPUT and OUTPUT
EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISITCS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IL}$	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{PLH} t_{PHL}		2.0	-	48	100	-	125	ns
			4.5	-	12	20	-	25	
			6.0	-	10	17	-	21	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$			-	30	-	-	-	

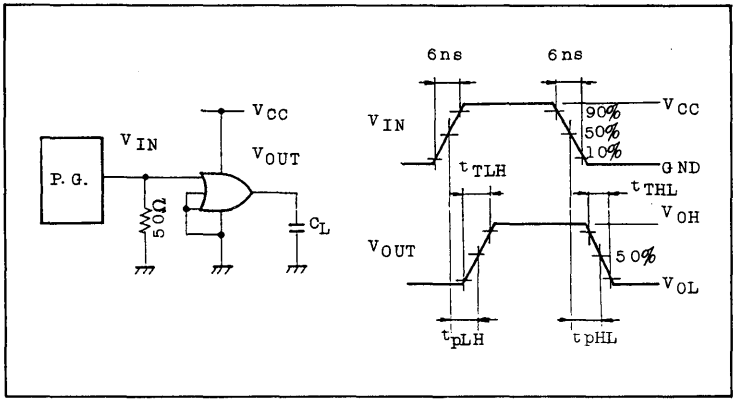
Note (1) CPD is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

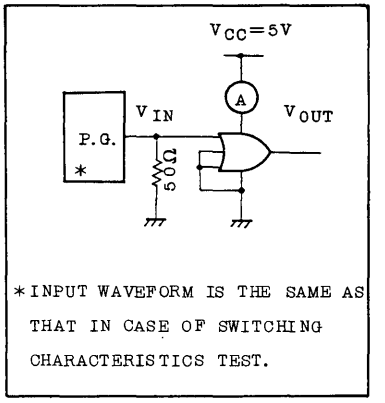
$$I_{CC(opr.)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}/3 \quad \text{(per gate)}$$

TC74HC4075P/F

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr.) TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4078P

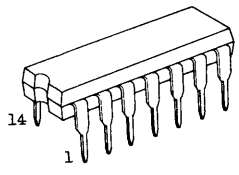
PRELIMINARY

TC74HC4078P 8-INPUT OR/NOR GATE

The TC74HC4078 is a high speed CMOS 8-INPUT NOR GATE fabricated with silicon gate C²MOS technology.
It operates ten times as fast as that of metal-gate C²MOS IC (4078B) with the same power dissipation.
Output X is 8-INPUT NOR, output Y is 8-INPUT OR. Both outputs are buffered, which enables high noise immunity and stable output.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=14ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... V_{NIH}=V_{NIL}=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|$=I_{OL}=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4078B



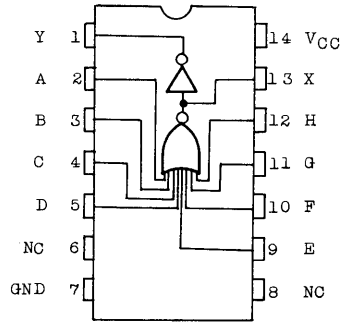
DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

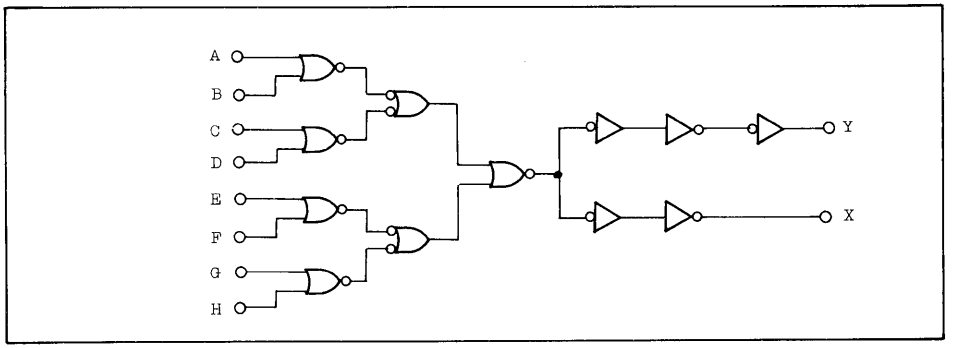
PIN ASSIGNMENT



(TOP VIEW)
NC:No Connection

TC74HC4078P

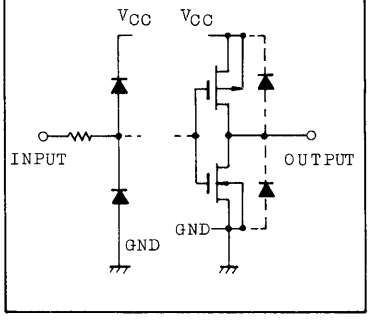
LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH} t_{pHL}		2.0	-	68	130	-	165	
			4.5	-	17	26	-	33	
			6.0	-	14	22	-	28	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	73	-	-	-	

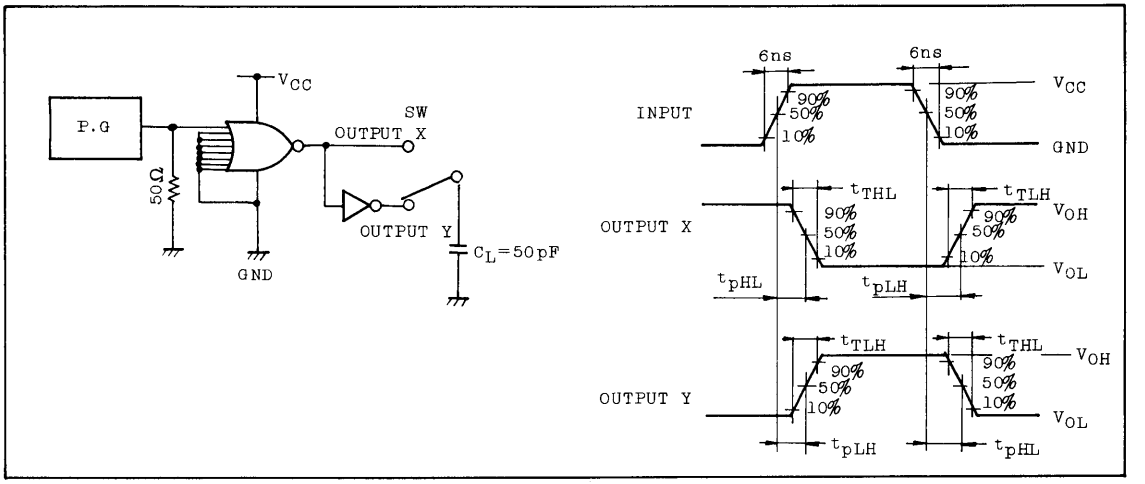
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

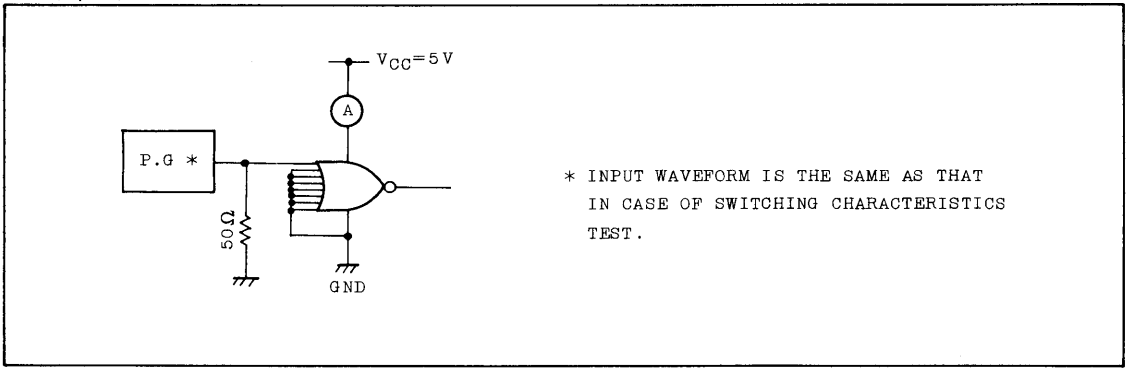
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4078P

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(Opr.)}$ TEST CIRCUIT



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4094P/F

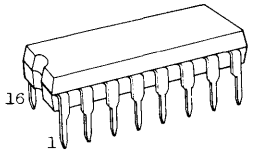
PRELIMINARY

TC74HC4094P/F 8-BIT SHIFT AND STORE REGISTER (3-STATE)

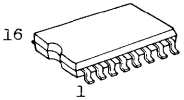
The TC74HC4094 is a high speed CMOS 8-STAGE SHIFT-AND-STORE REGISTER fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. This device consists of an 8-bit shift register and a 8-bit latch with 3-state output buffer. Data is shifted serially through the shift register on the positive going transition of the clock input signal. The output of the last stage (Qs) can be used to cascade several devices. Data on the Qs output is transferred to a second output (Qs') on the following negative transition of the clock input signal. The data of each stage of the shift register is provided to a latch, which latches data on the negative going transition of the STROBE input signal. When STROBE input is held high, data propagates through the latch to a 3-state output buffer. This buffer is enabled when OUTPUT ENABLE input is taken high. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... f_{MAX}=42MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Oerating Voltage Range ..... $V_{CC(opr.)}$=2V∿6V
- Pin and Function Compatible with 4094B



DIP16(3D16A-P)



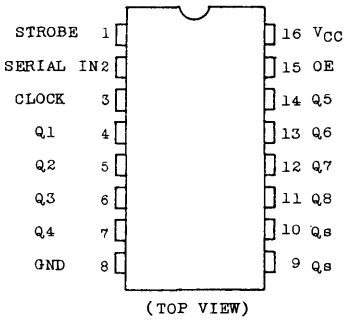
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5∿7	V
DC Input Voltage	V_{IN}	-0.5∿V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5∿V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65∿150	°C
Lead Temperature 10sec	T_L	300	°C

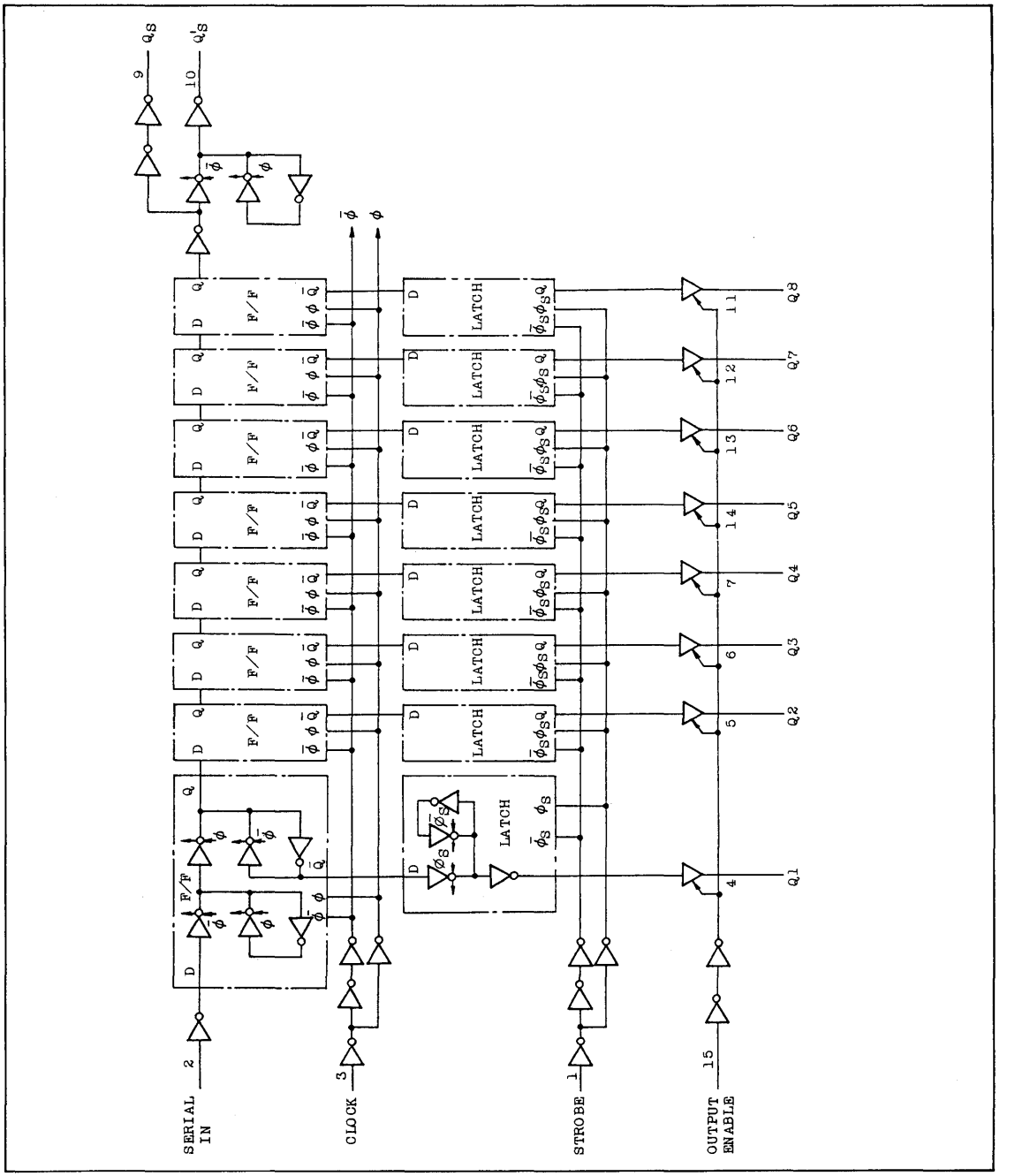
* 500mW in the range of Ta=-40°∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



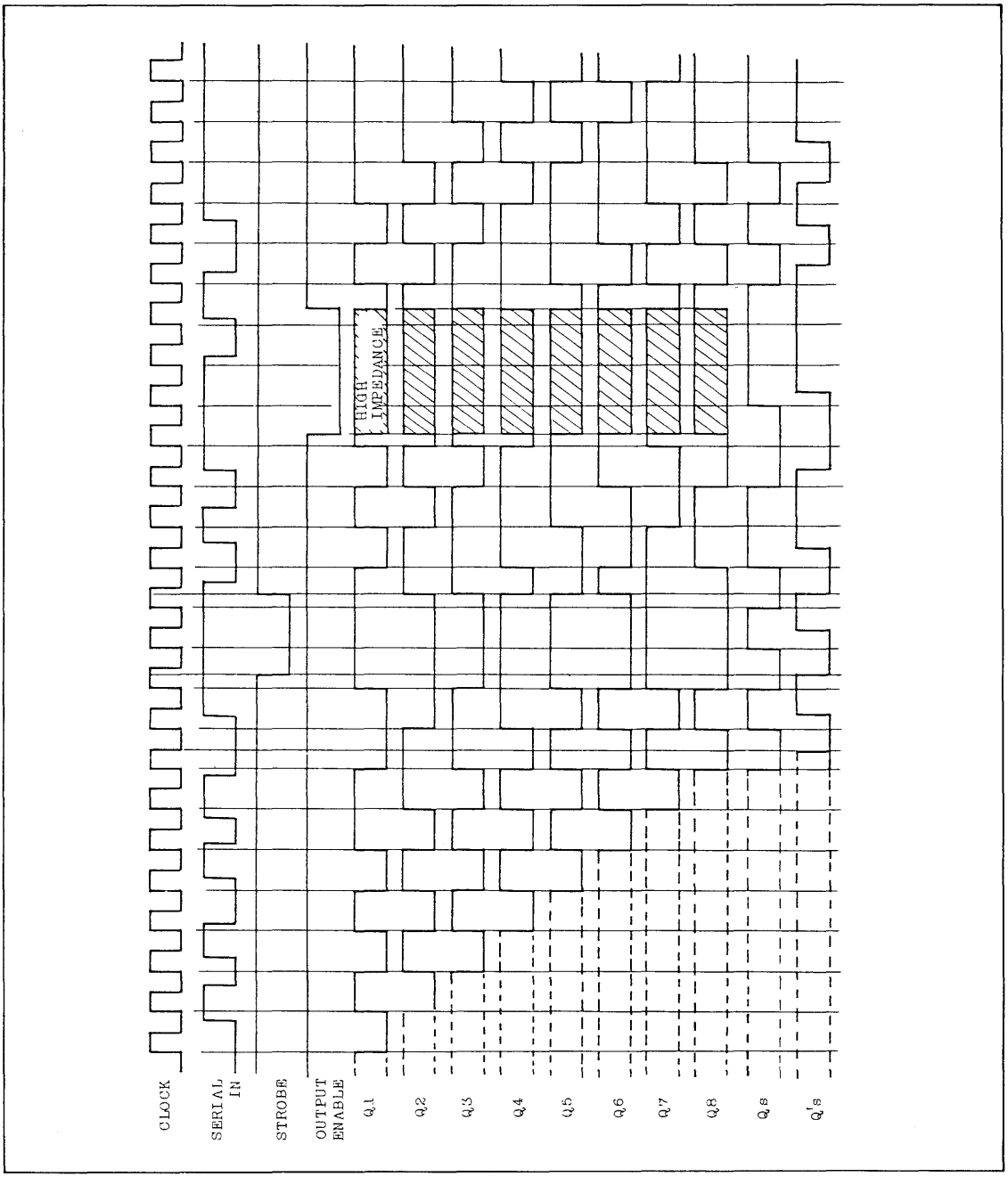
TC74HC4094P/F

LOGIC DIAGRAM



TC74HC4094P/F

TIMING CHART



TC74HC4094P/F

TRUTH TABLE

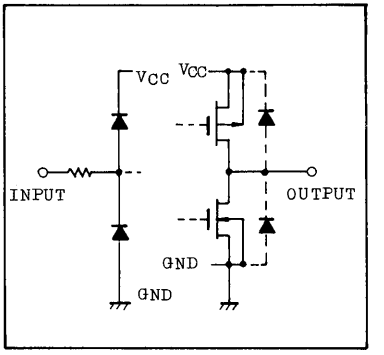
CK	OE	ST	SI	PARA.OUT		SERI.OUT	
				Q_1	Q_n	Q_s	Q_s'
↑	H	H	L	L	Qn-1	Q7	NC
↑	H	H	H	H	Qn-1	Q7	NC
↑	H	L	X	NC	NC	Q7	NC
↑	L	X	X	Z	Z	Q7	NC
↓	H	X	X	NC	NC	NC	Qs
↓	L	X	X	Z	Z	NC	Qs

X : DON'T CARE
NC: NO CHANGE
Z : HIGH IMPEDANCE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
	t_{THL}		4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - Qn)	t_{PLH}		2.0	-	140	270	-	340	
	t_{PHL}		4.5	-	35	54	-	68	
			6.0	-	30	46	-	58	
Propagation Delay Time (CLOCK - Qs, Qs')	t_{PLH}		2.0	-	104	200	-	250	
	t_{PHL}		4.5	-	26	40	-	50	
			6.0	-	22	34	-	43	
Propagation Delay Time (STROBE - Qn)	t_{PLH}		2.0	-	135	210	-	265	
	t_{PHL}		4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Maximum Clock Frequency	f_{MAX}		2.0	4	10	-	3	-	MHz
			4.5	20	38	-	16	-	
			6.0	24	45	-	19	-	
Minimum Clock Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	ns
	$t_{w(L)}$		4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Strobe Pulse Width	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	

TC74HC4094P/F

AC ELECTRICAL CHARACTERISTICS (Continued)

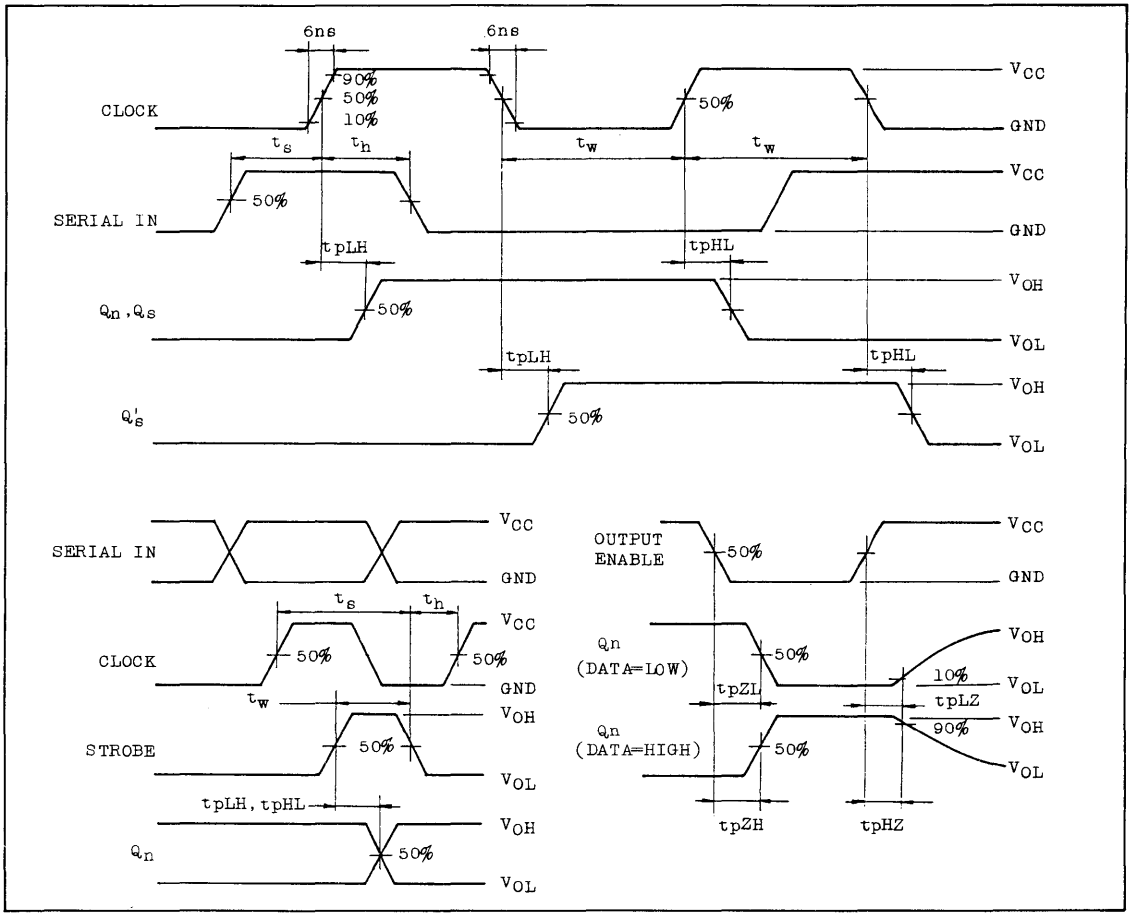
PARAMETER	SYMBOL	TEST CONDITION		25°C			-40 ~ 85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Minimum Serial In Set-up Time	t_s		2.0	-	25	75	-	95	ns
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Strobe Set-up Time	t_s		2.0	-	50	150	-	190	
			4.5	-	13	30	-	38	
			6.0	-	11	26	-	33	
Minimum Serial In Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Strobe Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
3-State Output Enable Time	t_{PZL} t_{PZH}	R_L=1kΩ	2.0	-	76	150	-	190	
			4.5	-	19	30	-	38	
			6.0	-	16	26	-	33	
3-State Output Disable Time	t_{PLZ} t_{PHZ}	R_L=1kΩ	2.0	-	84	165	-	205	
			4.5	-	21	33	-	41	
			6.0	-	18	28	-	35	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	167	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

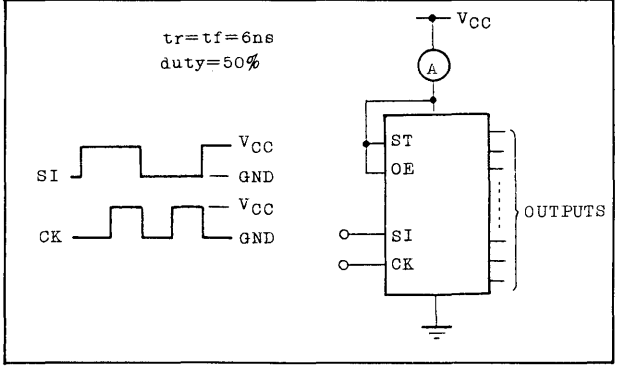
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TC74HC4094P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM



$I_{CC(opr.)}$ TEST WAVEFORM



C_{PD} CALCULATION

C_{PD} is to be calculated with the formula hereunder by using the measured value of $I_{CC(opr)}$ in the test circuit drawn left side.

$$C_{PD} = \frac{I_{CC(opr)}}{f_{IN} \cdot V_{CC}}$$

At determining the typical value of C_{PD}, a relatively high frequency 1MHz was applied for f_{IN}, in order to eliminate the error from the quiescent supply current.

TC74HC40102P
TC74HC40103P

CMOS DIGITAL INTEGRATED CIRCUIT

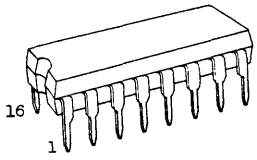
PRELIMINARY

TC74HC40102P DUAL BCD PROGRAMMABLE DOWN COUNTER
TC74HC40103P 8-BIT BINARY PROGRAMMABLE DOWN COUNTER

The TC74HC40102 and TC74HC40103 are high speed CMOS PROGRAMMABLE DOWN COUNTER fabricated with silicon gate C^2MOS technology.
They operate ten times as fast as that of metal-gate C^2MOS IC (40102/40103B) with the same power dissipation. Output terminal $\overline{CO/ZD}$ is placed in active mode at "L" level when the contents of count become zero. As the TC74HC40102 adopts BCD binary coded decimal notation, setting up to 99 counts is possible. The 74HC40103 with 8-bits binary construction, can set up to 255 counts. Each type has $\overline{CI/CE}$ inhibiting clock, $\overline{APE}$ asynchronous preset control input, $\overline{SPE}$ synchronous preset control input and $\overline{CLR}$ control input setting counter to maximum counting mode.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=36MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Operating Voltage Range .....V_{CC}(Opr.)=2V ∿ 6V
- Pin and Function Compatible with 40102B, 40103B



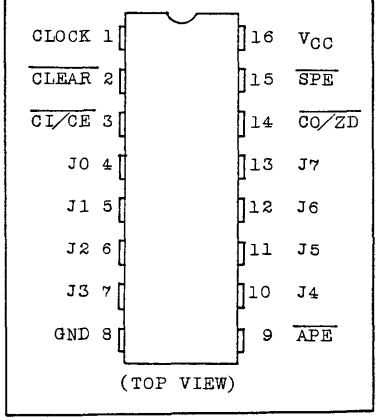
DIP16(3D16A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



TC74HC40102P
TC74HC40103P

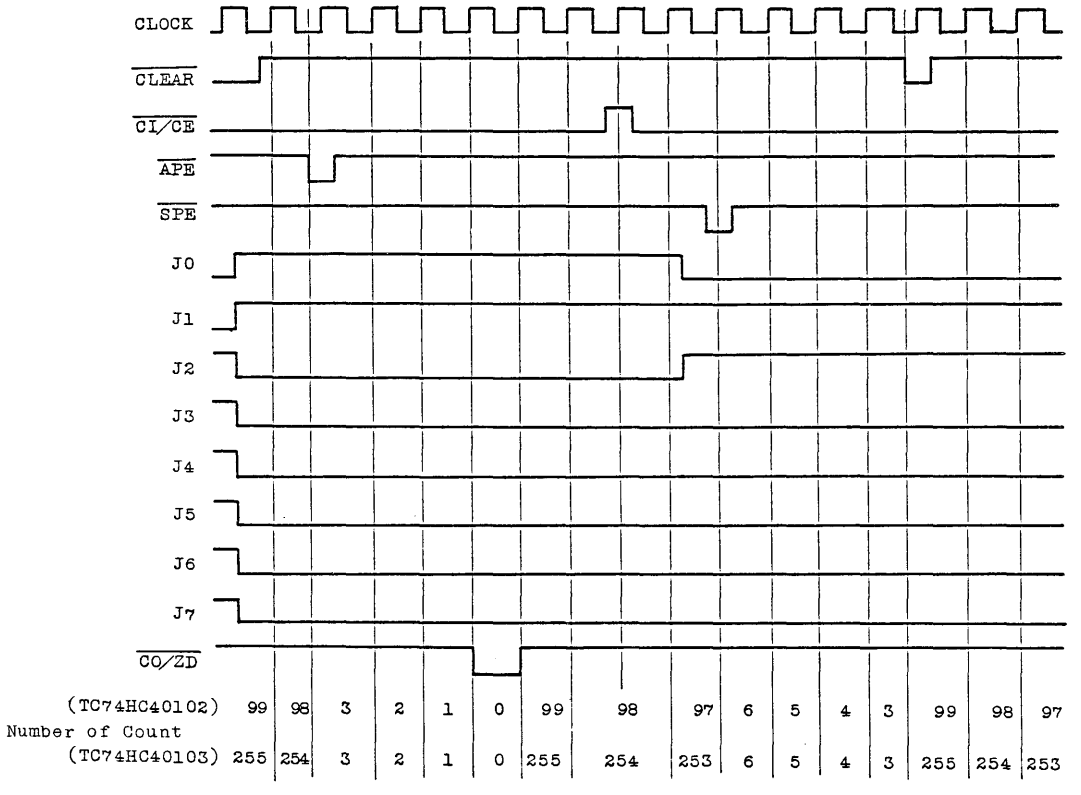
TRUTH TABLE

CONTROL INPUT				MODE	FUNCTIONAL DESCRIPTION
$\overline{CLEAR}$	$\overline{APE}$	$\overline{SPE}$	$\overline{CI/CE}$		
H	H	H	H	Count inhibit	Even if clock is given, no count is made.
H	H	H	L	Regular count	Down count at rising edge of clock.
H	H	L	X	Synchronous preset	Data of PI terminal is preset at rising edge of clock.
H	L	X	X	Asynchronous preset	Data of PI terminal is asynchronously preset to clock.
L	X	X	X	Clear	Counter is set to maximum count.

Note 1. X: Don't care

2. Maximum count: "99" for TC74HC40102 and "255" for TC74HC40103.

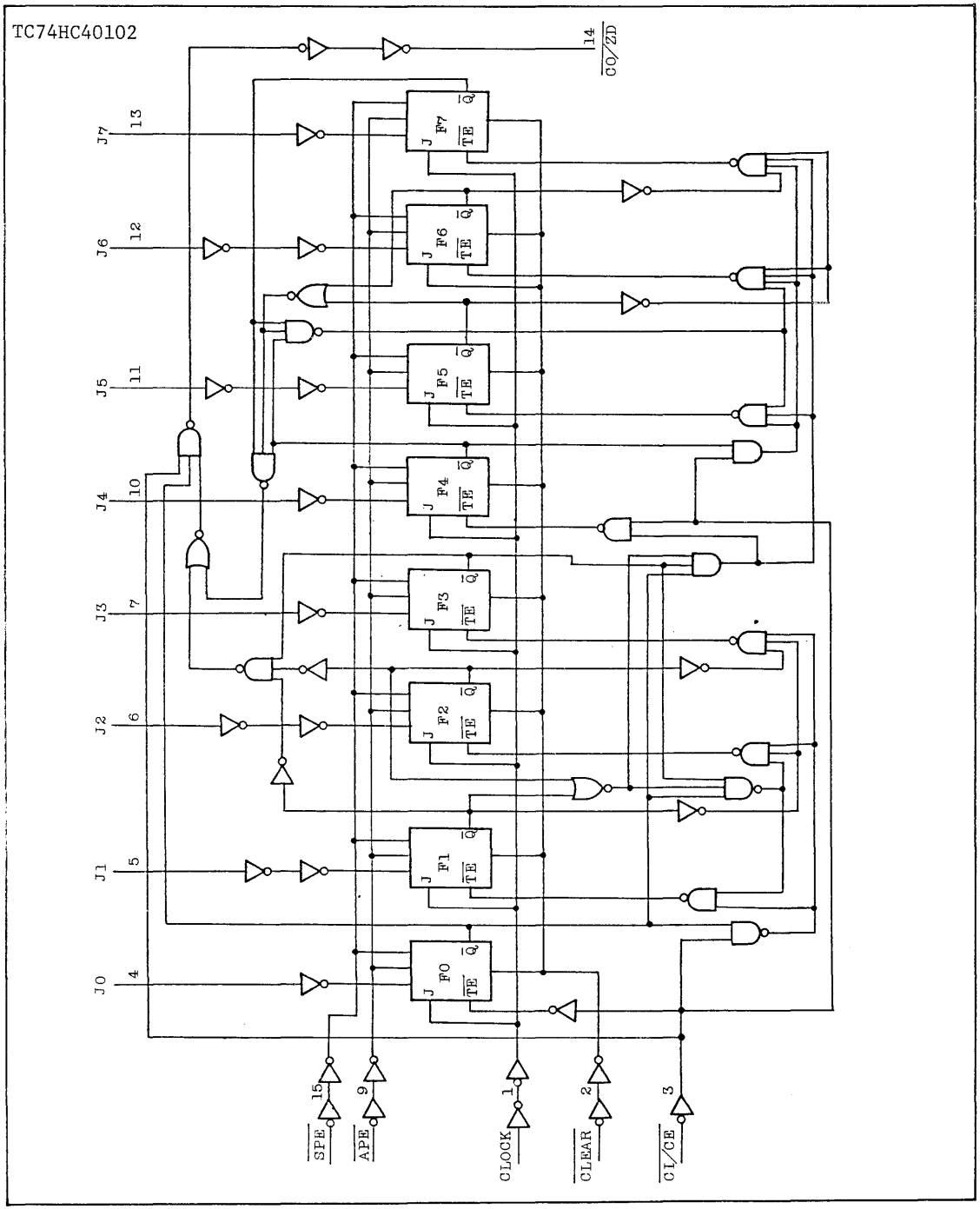
TIMING CHART



TC74HC40102P
TC74HC40103P

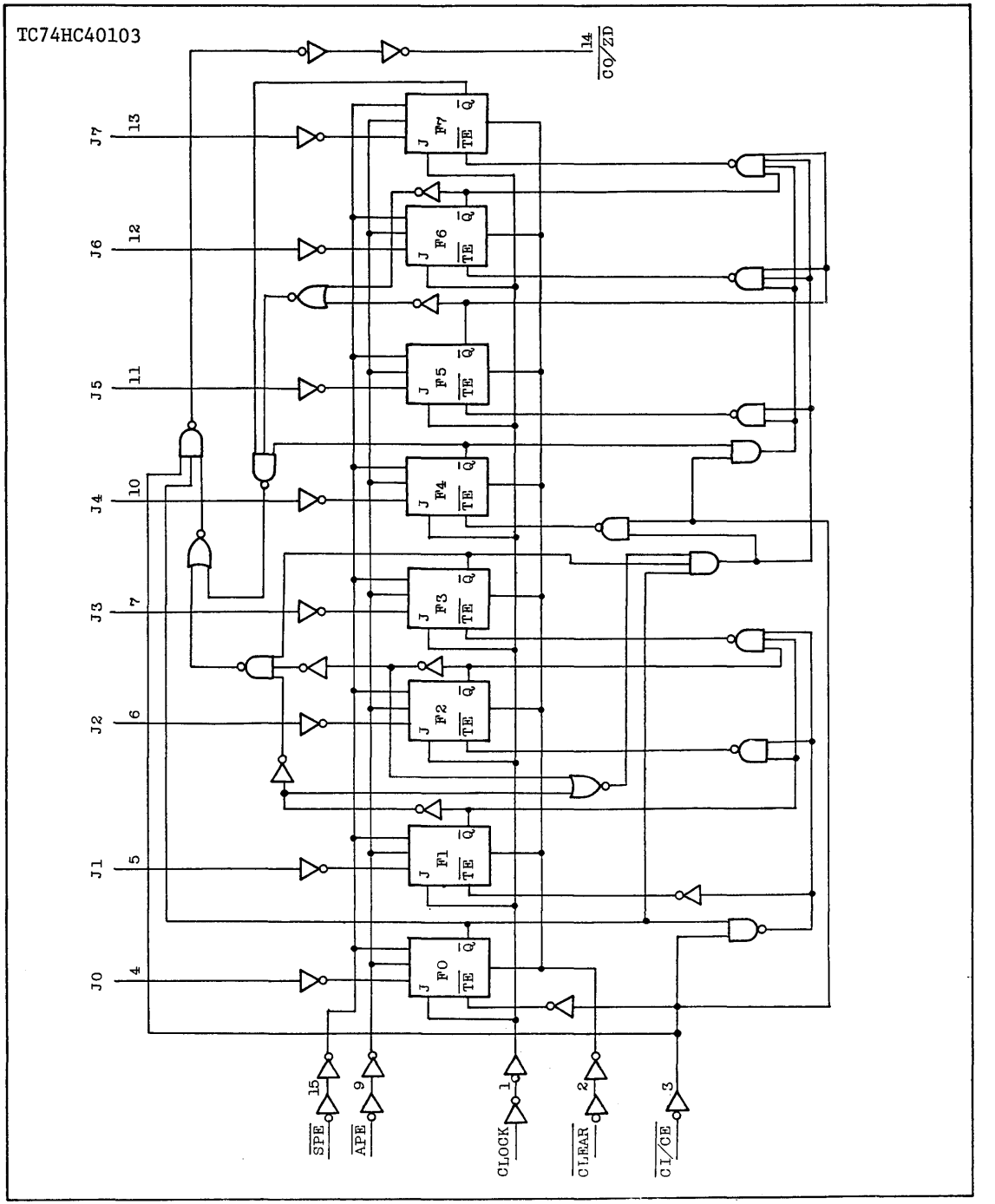
LOGIC DIAGRAM

TC74HC40102

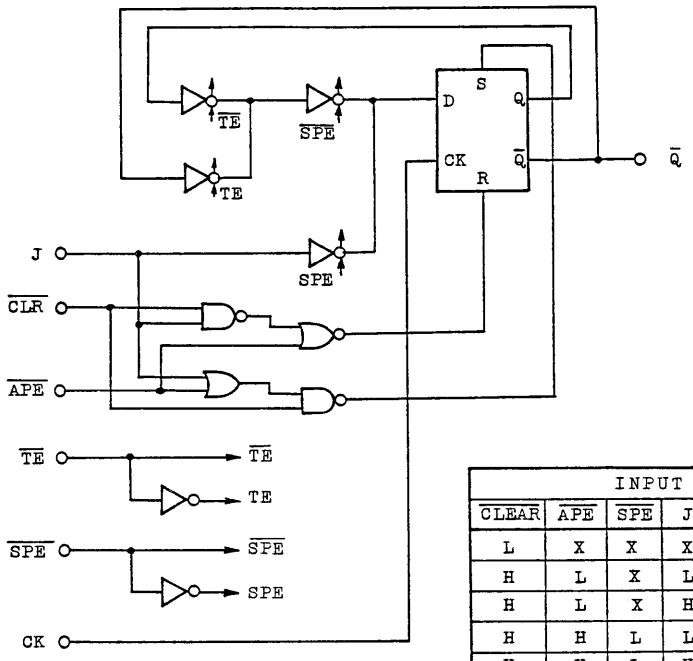


TC74HC40102P
TC74HC40103P

LOGIC DIAGRAM



TC74HC40102P
TC74HC40103P



INPUT						OUTPUT
CLEAR	APE	SPE	J	TE	CLOCK	$\overline{Q_n}+1$
L	X	X	X	X	X	L
H	L	X	L	X	X	L
H	L	X	H	X	X	H
H	H	L	L	X	↓	L
H	H	L	H	X	↓	H
H	H	L	X	X	↑	$\overline{Q_n}$
H	H	H	X	L	↓	Q_n
H	H	H	X	H	X	$\overline{Q_n}$

FUNCTIONAL DESCRIPTION

The TC74HC40102 and TC74HC40103 are 8-stage presettable synchronous down counters. Carry Out/Zero Detect ($\overline{CO/ZD}$) is output at the "L" level for the period of 1 bit when the readout becomes "0". The TC74HC40102 adopts binary coded decimal notation, making setting up to 99 counts possible. While the TC74HC40103 adopts 8-bit binary counter and can set up to 255 counts.

COUNT OPERATION

At the "H" level of control input of $\overline{CLEAR}$, $\overline{SPE}$ and $\overline{APE}$, the counter carries out down count operation one by one at the rise of pulse given to CLOCK input. Count operation can be inhibited by setting Carry Input/Clock Enable ($\overline{CI/CE}$) to the "H" level.

TC74HC40102P
TC74HC40103P

(Continued)

$\overline{CO/ZD}$ is output at the "L" level when the readout becomes "0", but is not output even if the readout becomes "0" when $\overline{CI/CE}$ is at the "H" level, thus maintaining the "H" level.

Synchronous cascade operation can be carried out by using $\overline{CI/CE}$ input and $\overline{CO/ZD}$ output.

The contents of count jump to maximum count (99 for the TC74HC40102 and 255 for the TC74HC40103) if clock is given when the readout is "0". Therefore, operation of 100-frequency division and that of 256-frequency division are carried out for the TC74HC40102 and TC74HC40103, respectively, when clock input alone is given without various kinds of preset operations.

PRESET OPERATION AND RESET OPERATION

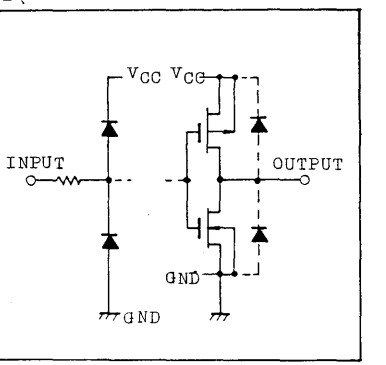
When Clear ($\overline{CLEAR}$) input is set to the "L" level, the readout is set to the maximum count independently of other inputs. When Asynchronous Preset Enable ($\overline{APE}$) input is set to the "L" level, readouts given on J0 to J7 can be preset asynchronously to counter independently of inputs other than $\overline{CLEAR}$ input. When Synchronous Preset Enable ($\overline{SPE}$) is set to the "L" level, the readouts given on J0 to J7 can be preset to counter synchronously with the rise of clock.

As to these operation modes, refer to the truth table.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC40102P
TC74HC40103P

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CLOCK - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	128	245	-	305	
			4.5	-	32	49	-	61	
			6.0	-	27	42	-	52	
Propagation Delay Time ($\overline{APE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	156	300	-	375	
			4.5	-	39	60	-	75	
			6.0	-	33	51	-	64	

TC74HC40102P
TC74HC40103P

AC ELECTRICAL CHARACTERISTICS (Continued)

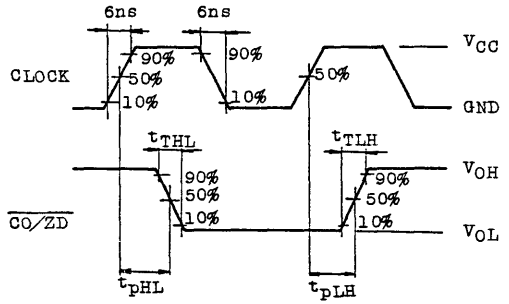
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CLEAR}$ - $\overline{CO/ZD}$)	t_{pLH}		2.0	-	124	240	-	300	ns
			4.5	-	31	48	-	60	
			6.0	-	27	41	-	51	
Propagation Delay Time ($\overline{CI/CE}$ - $\overline{CO/ZD}$)	t_{pLH} t_{pHL}		2.0	-	56	115	-	145	
			4.5	-	14	23	-	29	
			6.0	-	12	20	-	25	
Maximum Clock Frequency	f_{MAX}		2.0	4	8	-	3	-	MHz
			4.5	20	31	-	16	-	
			6.0	24	36	-	19	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Pulse Width ($\overline{CLEAR}$, $\overline{APE}$)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Removal Time ($\overline{CLEAR}$, $\overline{APE}$)	t_{rem}		2.0	-	20	75	-	95	
			4.5	-	5	15	-	19	
			6.0	-	4	13	-	16	
Minimum Set up Time ($\overline{SPE}$ - CK)	t_s		2.0	-	30	75	-	95	
			4.5	-	7	15	-	19	
			6.0	-	6	13	-	16	
Minimum Set up Time ($\overline{CI/CE}$ - CK)	t_s		2.0	-	56	125	-	160	
			4.5	-	14	25	-	32	
			6.0	-	12	21	-	27	
Minimum Set up Time (Jn - CK)	t_s		2.0	-	25	75	-	95	
			4.5	-	6	15	-	19	
			6.0	-	5	13	-	16	
Minimum Set up Time (Jn - $\overline{APE}$)	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time (All Inputs)	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD(1)}$	74HC40102		-	110	-	-	-	
		74HC40103		-	128	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

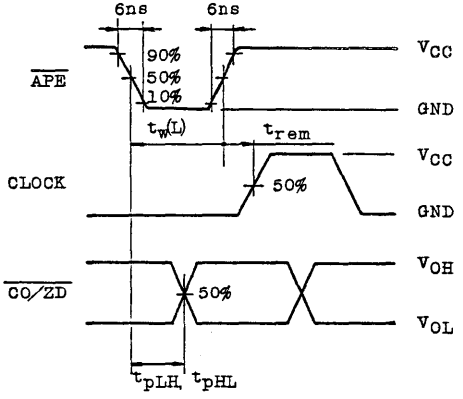
$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

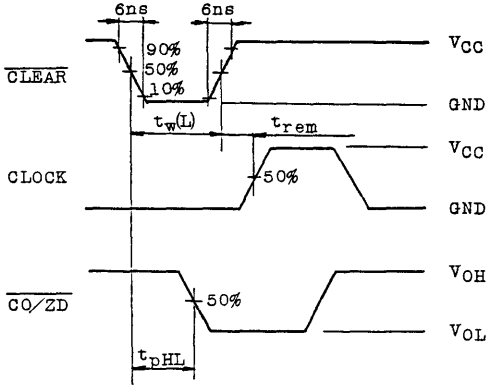
WAVEFORM 1



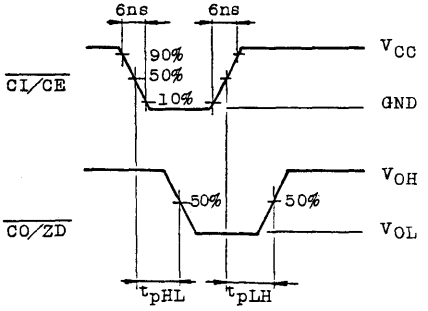
WAVEFORM 2



WAVEFORM 3

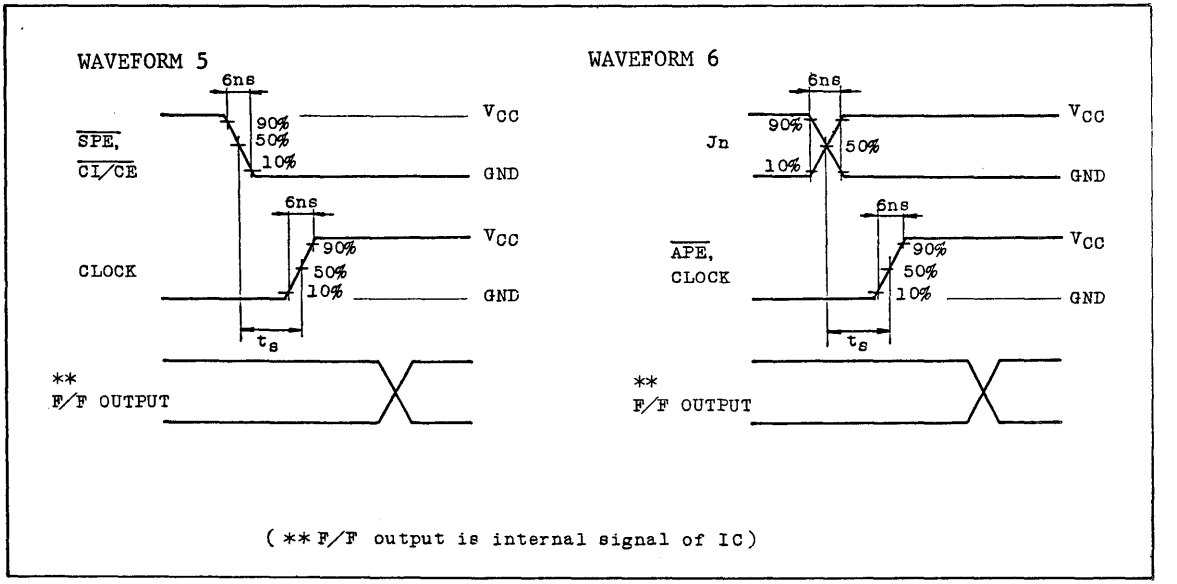


WAVEFORM 4



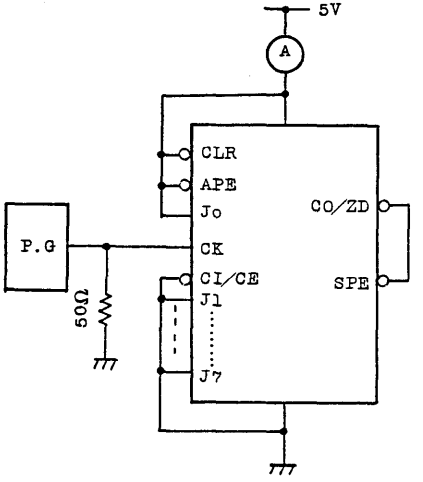
TC74HC40102P
TC74HC40103P

SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



(** F/F output is internal signal of IC)

I_{CC}(Opr.) TEST CIRCUIT

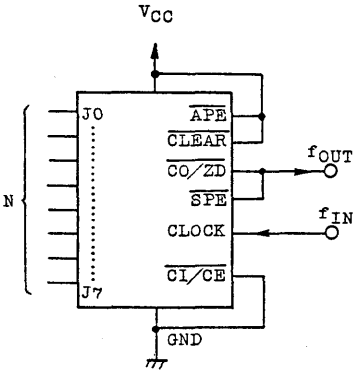


Input transition time is the same as that in case of switching characteristics test.

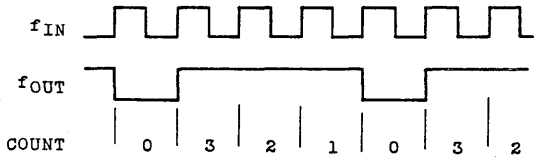
TC74HC40102P
TC74HC40103P

EXAMPLE OF TYPICAL APPLICATION

PROGRAMMABLE DIVIDE-BY-N COUNTER

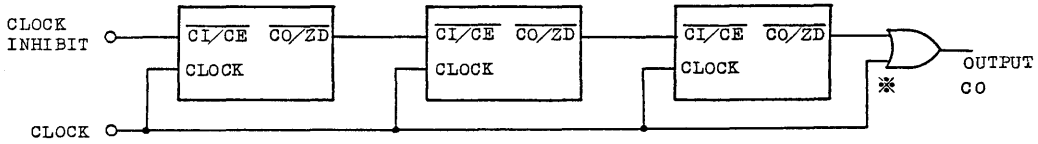


- $f_{OUT} = \frac{f_{IN}}{N+1}$
- Timing chart when N="3" (J0, J1=V_{CC}, J2 ∿ J7=GND)



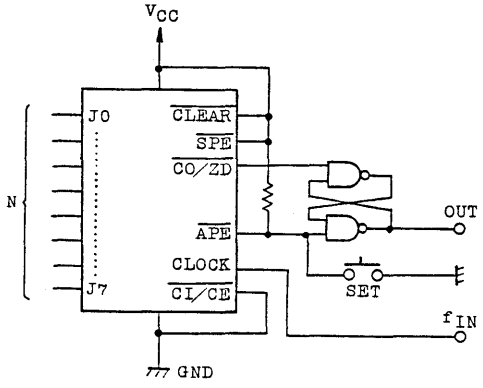
- TC74HC40102P .... 1/2 to 1/100 are dividable.
- TC74HC40103P .... 1/2 to 1/256 are dividable.

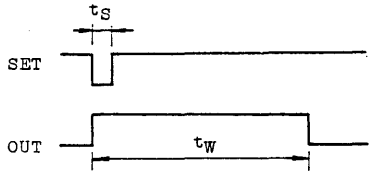
PARALLEL CARRY CASCADING



※ At synchronous cascade connection, huzzerd occurs at CO output after its second stage when digit place changes, due to delay arrival. Therefore, take gate from TC74HC32 or the like, not from CO output at the rear stage directly.

PROGRAMMABLE TIMER





$$t_W = \left(\frac{N}{f_{IN}} + t_S\right)$$

Note: The above formula does not take into account the phase of clock input. Therefore, the real pulse width is the distance between the above formula-$1/f_{IN}$ ∿ the above formula.

TC74HC4511P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC4511P/F BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER

The TC74HC4511 is a high speed CMOS BCD-TO-7 SEGMENT LATCH/DECODER/DRIVER fablicated with silicon gate C²MOS technology. It enables high speed latch and decode operation with identical pin connection and function to standard CMOS 4511B.

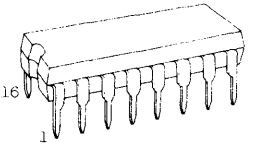
The segment output driver, which is CMOS construction, has large I_{OH} capability which enables to drive cathode common LED directly.

When lamp test ($\overline{LT}$) is taken "L", all segment outputs will go to "H", and when blanking ($\overline{BI}$) is taken "L" and $\overline{LT}$ is taken "H" all segment outputs will go to "L". These functions are regardless of other inputs and used to test display.

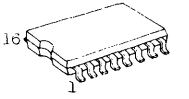
BI input is used to pulse-modulate the brightness of the display.

When error input code (over 10) is applied to BCD input, all segment outputs will go "L" (turn off).

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



DIP16(3D16A-P)

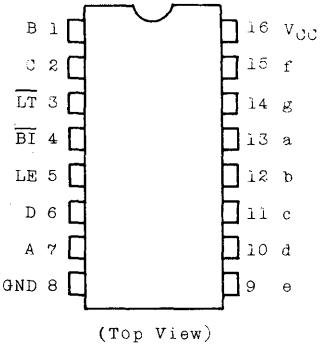


MFP16(F16GC-P)

FEATURES:

- High Speed.....t_w=15ns(Max.) at V_{CC}=4.5V
- Low Power Dissipation.....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity.....V_{NIH}=V_{NIL}=28% V_{CC} (Min.)
- Output Drive Capability.....10 LSTTL Loads
- High Output Current.....$|I_{OH}|$=20mA
- Wide Operating Voltage Range.$V_{CC(opr)}$=2V ~ 6V
- Pin and Function Compatible with standard CMOS 4511B.

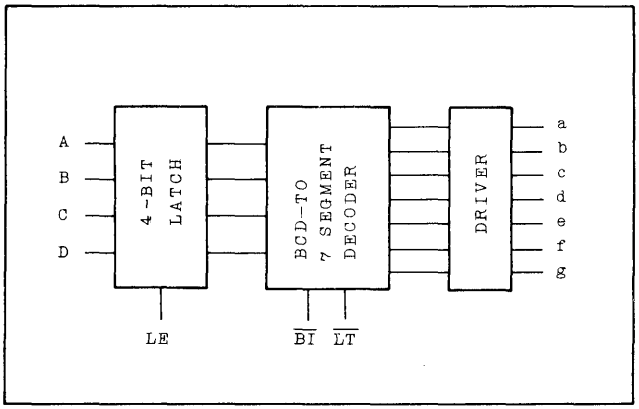
PIN ASSIGNMENT



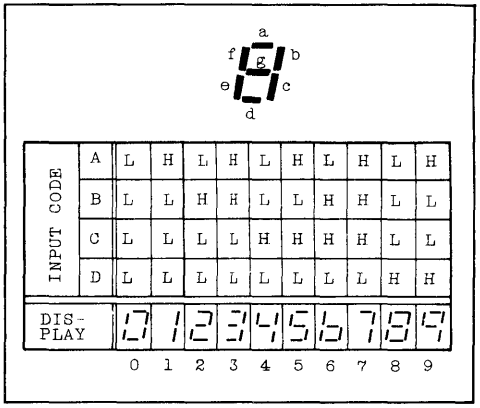
(Top View)

TC74HC4511P/F

BLOCK DIAGRAM

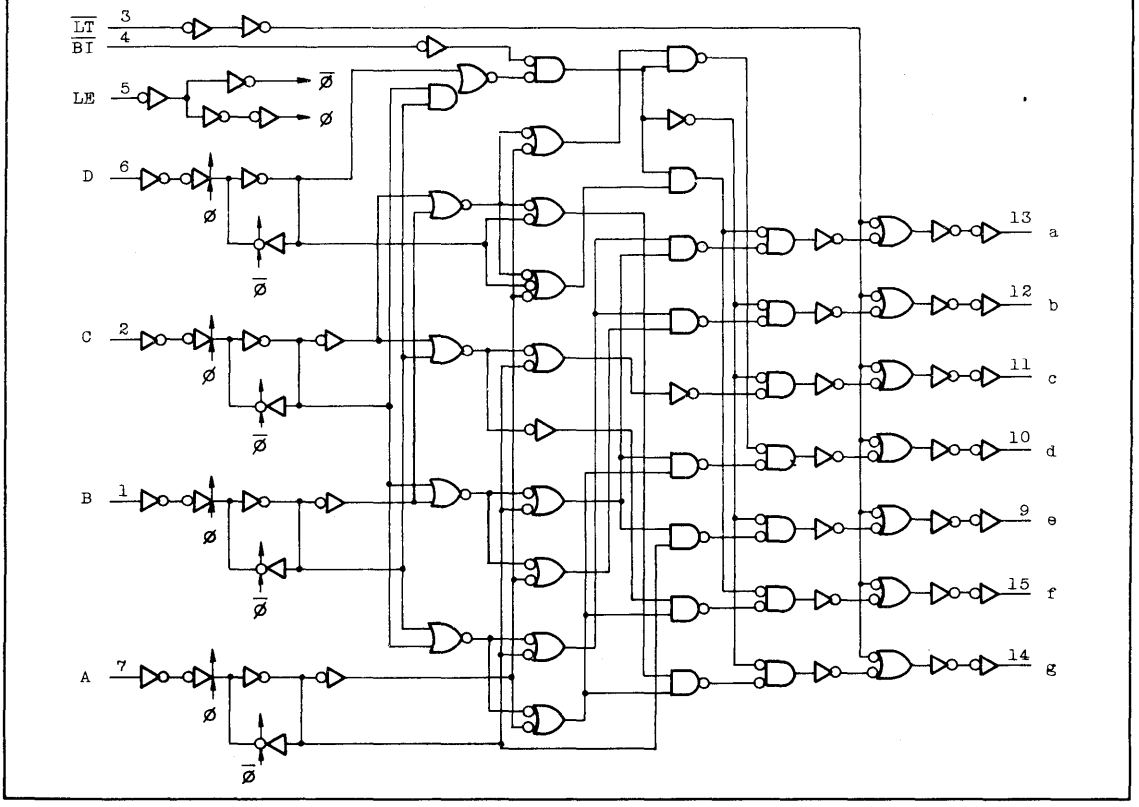


DISPLAY MODE



INPUT CODE										
A	L	H	L	H	L	H	L	H	L	H
B	L	L	H	H	L	L	H	H	L	L
C	L	L	L	L	H	H	H	H	L	L
D	L	L	L	L	L	L	L	L	H	H
DISPLAY	0	1	2	3	4	5	6	7	8	9

LOGIC DIAGRAM



TC74HC4511P/F

TRUTH TABLE

INPUTS							OUTPUTS							DISPLAY MODE
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	BLANK
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	X	L	L	L	L	L	L	L	BLANK
L	H	H	H	H	X	X	L	L	L	L	L	L	L	BLANK
H	H	H	X	X	X	X	Hold the stage at the leading edge of LE							

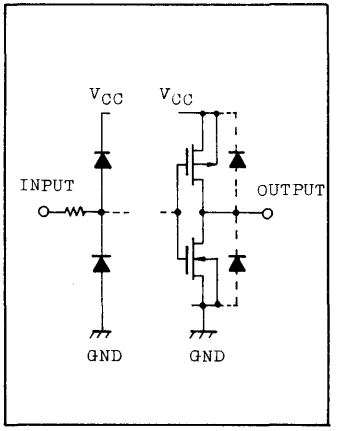
X: Don't care.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	+25 / -35	mA
DC V_{CC}/Ground Current	I_{CC}	+150 / -50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ~ 65°C.
and from Ta=65°C up to 85°C derating factor of -10mW/°C
shall be applied until 300mW.

INPUT and OUTPUT
EQUIVALENT CIRCUIT



TC74HC4511P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000(V_{CC}=2.0V) 0 ∿ 500(V_{CC}=4.5V) 0 ∿ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40~85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-6mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-20mA	4.5	3.20	3.80	-	2.90	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}= V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC4511P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

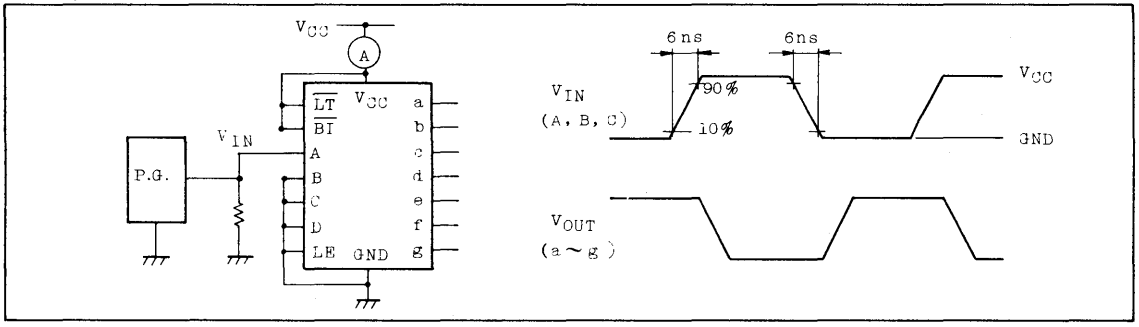
PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=-40~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time Low to High	t_{TLH}		2.0	-	25	60	-	75	ns
			4.5	-	6	12	-	15	
			6.0	-	5	10	-	13	
Output Transition Time High to Low	t_{THL}		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (BCD-Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Propagation Delay Time ($\overline{BI}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	116	250	-	315	
			4.5	-	29	50	-	63	
			6.0	-	25	43	-	54	
Propagation Delay Time ($\overline{LT}$ - Segment)	t_{pLH} t_{pHL}		2.0	-	72	150	-	190	
			4.5	-	18	30	-	38	
			6.0	-	15	26	-	33	
Propagation Delay Time (LE - Segment)	t_{pLH} t_{pHL}		2.0	-	192	400	-	500	ns
			4.5	-	48	80	-	100	
			6.0	-	41	68	-	85	
Minimum Pulse Width (LE)	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Data Set-up Time	t_s		2.0	-	35	75	-	95	
			4.5	-	9	15	-	19	
			6.0	-	8	13	-	16	
Minimum Data Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	136	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).
Average operating current can be obtained by the equation hereunder.

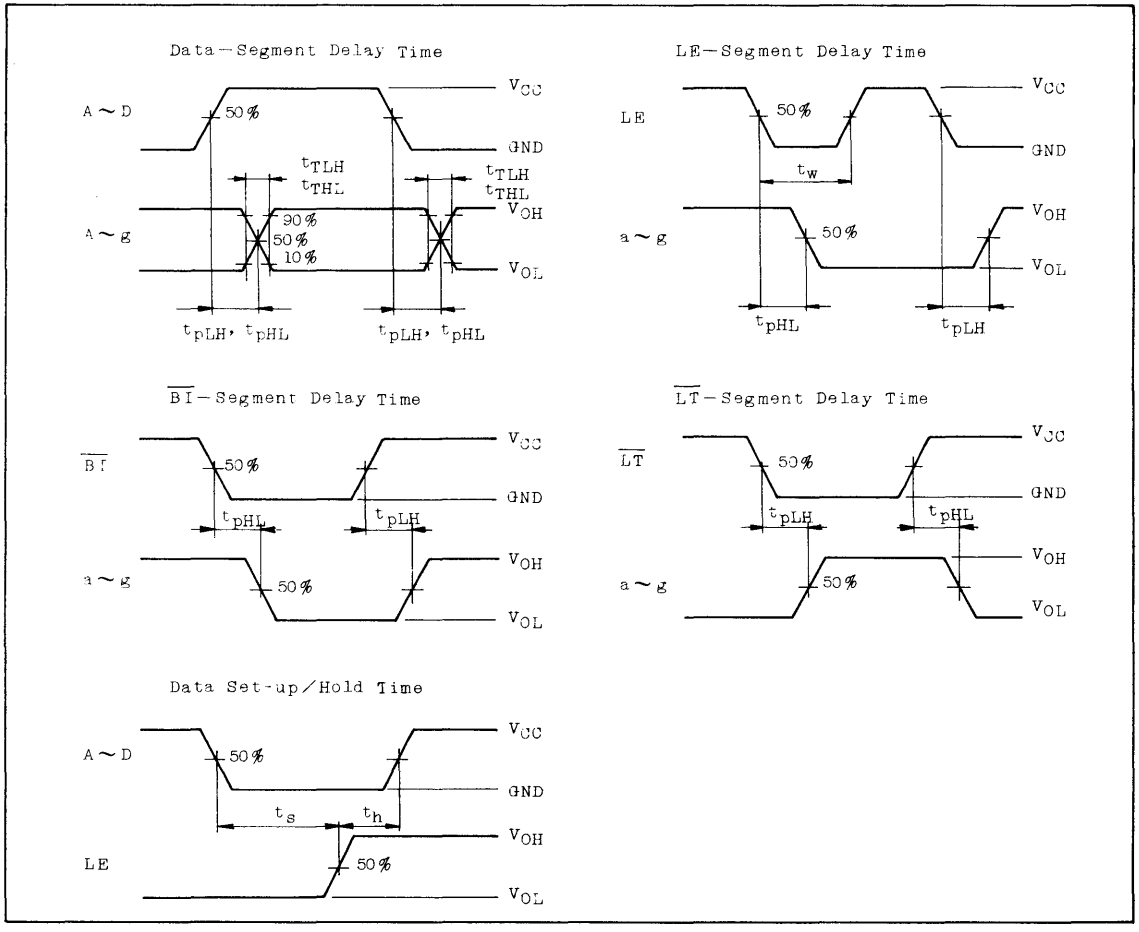
$$I_{CC(opr)}=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}$$

TC74HC4511P/F

$I_{CC(opr)}$ TEST CIRCUIT



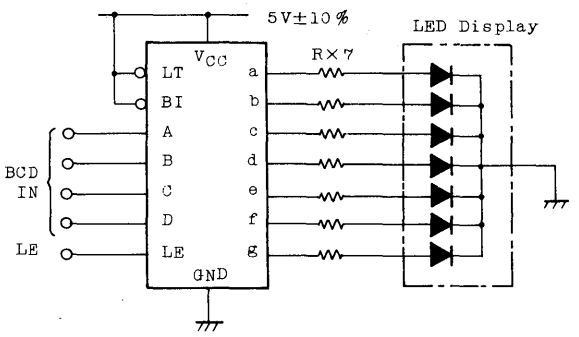
SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC4511P/F

APPLICATION CIRCUIT

Static Display Circuit



Recommended Resistance R

DISPLAY	COLOR	LETTER HIGHT	R
TLR358	Red	13.4mm	390Ω
TLR362	"	14.2	"
TLR332	"	7.6	"
TLR342	"	10.9	"
TLG358	Green	13.4mm	160Ω
TLG362	"	14.2	"
TLG332	"	7.6	"
TLG342	"	10.9	"

TC74HC4514P
TC74HC4515P

C²MOS DIGITAL INTEGRATED CIRCUIT

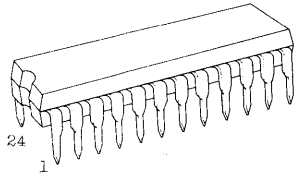
PRELIMINARY

TC74HC4514P 4-TO-16 LINE DECODER/LATCH
TC74HC4515P 4-TO-16 LINE DECODER/LATCH (INV.)

The TC74HC4514 and TC74HC4515 are high speed CMOS 4-LINE TO 16-LINE DECODER WITH LATCHED INPUTS fabricated with silicon gate C²MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. A binary code stored in the four input latches (A thru D) provides a high level (HC4514) or a low level (HC4515) at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input (INHIBIT) is held low. When the inhibit input is held high, all outputs are kept low level (HC4514) or high level (HC4515), while the latch function is available. The data applied to the data inputs are transfered to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of latches. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=22ns (Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA (Max.) at 25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC} (Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC} (opr.)=2V ∿ 6V
- Pin and Function Compatible with 4514B/4515B



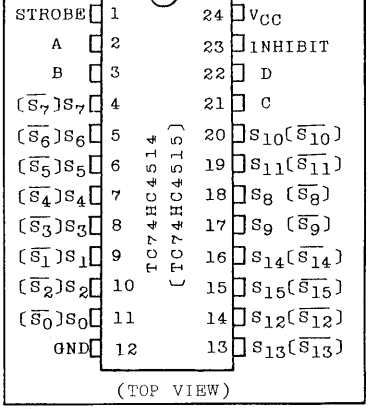
DIP24(3D24A-P)
0.300INCH(7.62mm)ROW SPACING

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

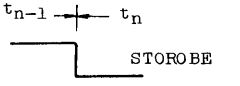
TC74HC4514P
TC74HC4515P

TRUTH TABLE

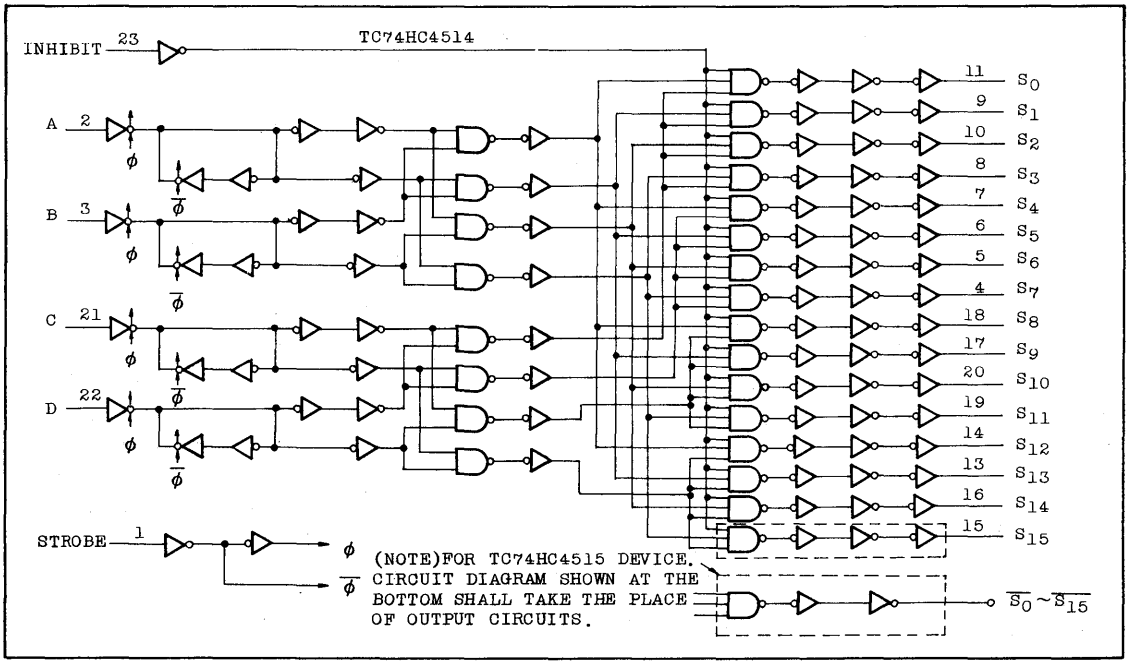
INPUTS					SELECTED OUTPUT TC74HC4514P — 'H' (TC74HC4515P — 'L')
INHIBIT	A	B	C	D	
L	L	L	L	L	S_0 ($\overline{S_0}$)
L	H	L	L	L	S_1 ($\overline{S_1}$)
L	L	H	L	L	S_2 ($\overline{S_2}$)
L	H	H	L	L	S_3 ($\overline{S_3}$)
L	L	L	H	L	S_4 ($\overline{S_4}$)
L	H	L	H	L	S_5 ($\overline{S_5}$)
L	L	H	H	L	S_6 ($\overline{S_6}$)
L	H	H	H	L	S_7 ($\overline{S_7}$)
L	L	L	L	H	S_8 ($\overline{S_8}$)
L	H	L	L	H	S_9 ($\overline{S_9}$)
L	L	H	L	H	S_{10} ($\overline{S_{10}}$)
L	H	H	L	H	S_{11} ($\overline{S_{11}}$)
L	L	L	H	H	S_{12} ($\overline{S_{12}}$)
L	H	L	H	H	S_{13} ($\overline{S_{13}}$)
L	L	H	H	H	S_{14} ($\overline{S_{14}}$)
L	H	H	H	H	S_{15} ($\overline{S_{15}}$)
H	X	X	X	X	TC74HC4514 — ALL OUTPUTS 'L' (TC74HC4515 — ALL OUTPUTS 'H')

- X : DON'T CARE
- STROBE='H' ; REFER TO TRUTH TABLE
- STROBE='L'

  DATA AT THE NEGATIVE GOING TRANSITION OF STROBE SHALL BE PROVIDED ON THE EACH OUTPUT WHILE STROBE IS HELD LOW.



LOGIC DIAGRAM

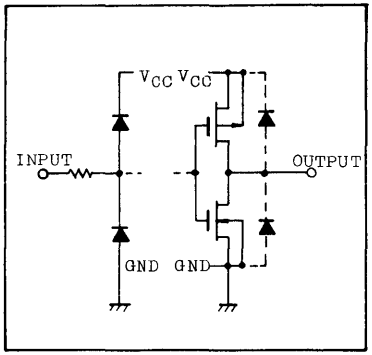


TC74HC4514P
TC74HC4515P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	

TC74HC4514P
TC74HC4515P

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6nS)

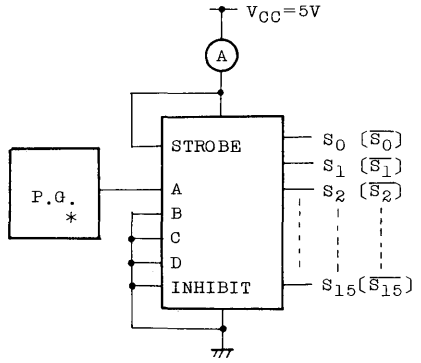
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Output Rise, Fall Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	nS
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time DATA - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	108	215	-	270	
			4.5	-	27	43	-	54	
			6.0	-	23	37	-	46	
STROBE - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	124	245	-	305	
			4.5	-	31	49	-	61	
			6.0	-	26	42	-	52	
INHIBIT - S_n, $\overline{S_n}$	t_{PLH} t_{PHL}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
			6.0	-	19	30	-	37	
Mininum Pulse Width STROBE	$t_{w(H)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time DATA	t_s		2.0	-	10	50	-	65	
			4.5	-	4	10	-	13	
			6.0	-	3	9	-	11	
Minimum Hold Time DATA	t_h		2.0	-	-	5	-	5	
			4.5	-	-	5	-	5	
			6.0	-	-	5	-	5	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4514P		-	69	-	-	-	
		[TC74HC4515P]		-	[72]	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

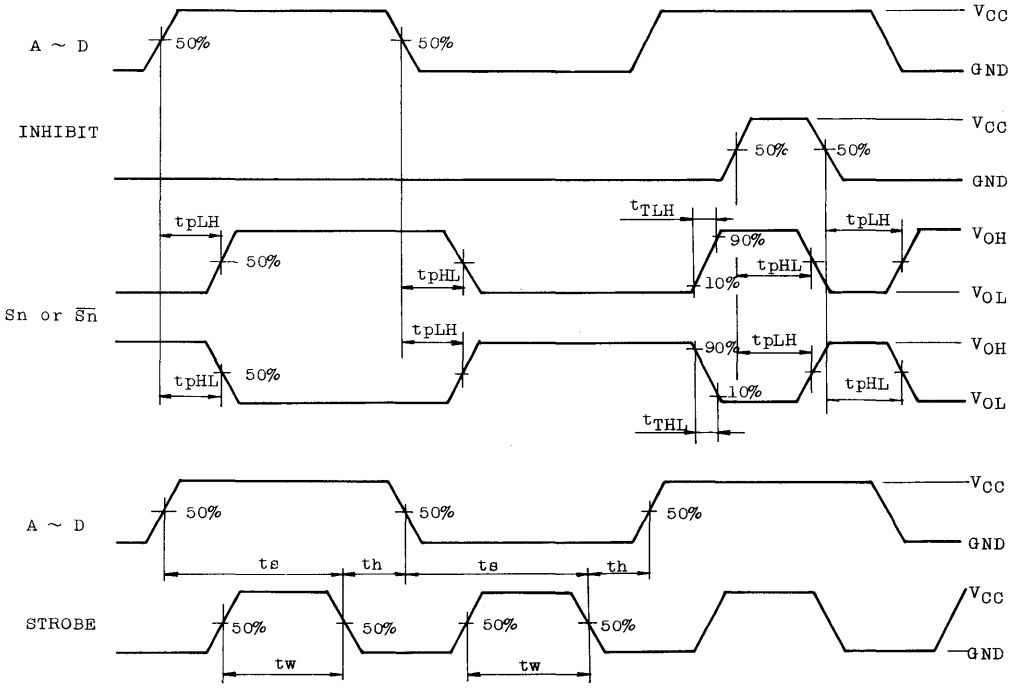
TC74HC4514P
TC74HC4515P

$I_{CC(opr.)}$ TEST WAVEFORM



* INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISITCS TEST WAVEFORM



TC74HC4518P
TC74HC4520P/F

C²MOS DIGITAL INTEGRATED CIRCUIT

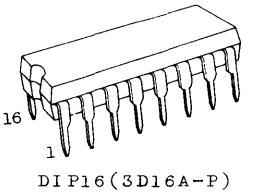
PRELIMINARY

TC74HC4518P DUAL BCD COUNTER
TC74HC4520P/F DUAL 4-BIT BINARY COUNTER

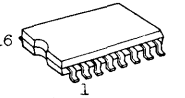
The TC74HC4518 and TC74HC4520 are high speed CMOS DUAL BCD/4-BIT BINARY COUNTER fabricated with silicon gate C^2MOS technology.
It operates ten times as fast as that of metal-gate C^2MOS IC (4518B/4520B) with the same power dissipation.
Since both of TC74HC4518 and TC74HC4520 contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" ($Q_0 \sim Q_3$="L") by giving "H" level signal to CLEAR input regardless of other inputs. The counting condition is changed by the positive going transition of CLOCK input if CE="H" or by the negative going transition of CE if CLOCK="L".
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=53MHz(Typ.) at V_{CC}=5V
- Low Power Dissipation .....I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(Opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 4518B/4520B



DIP16(3D16A-P)



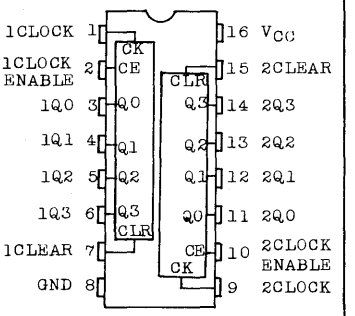
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

TC74HC4518P
TC74HC4520P/F

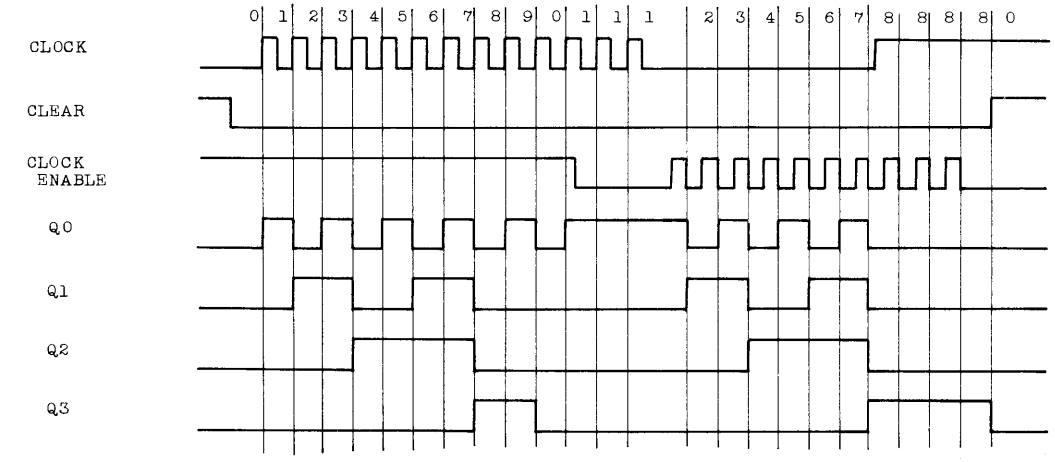
TRUTH TABLE

INPUTS			FUNCTION
CLOCK	CLOCK ENABLE	CLEAR	
↑	H	L	INCLEMENT COUNTER
L	↓	L	INCLEMENT COUNTER
↓	X	L	NO CHANGE
X	↑	L	NO CHANGE
↑	L	L	NO CHANGE
H	↓	L	NO CHANGE
X	X	H	Q0 THRU Q3 = L

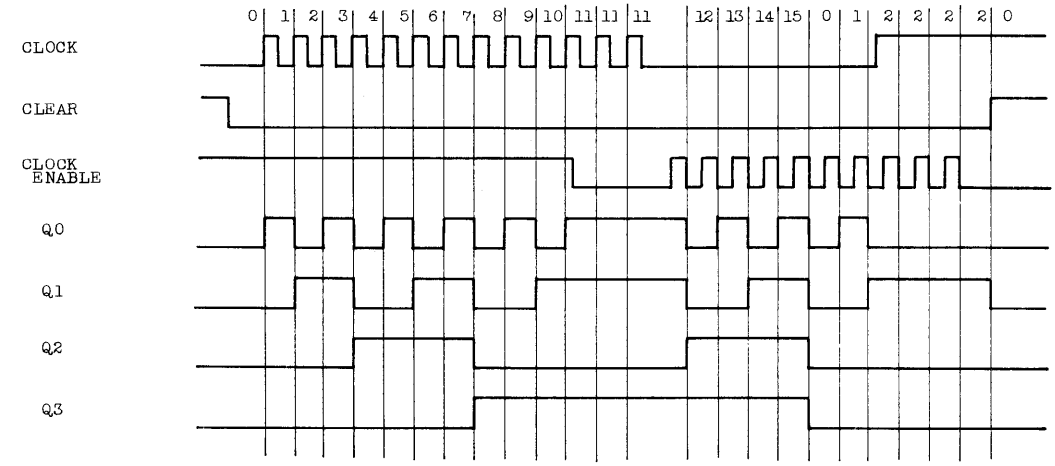
X : DON'T CARE

TIMING CHART

TC74HC4518



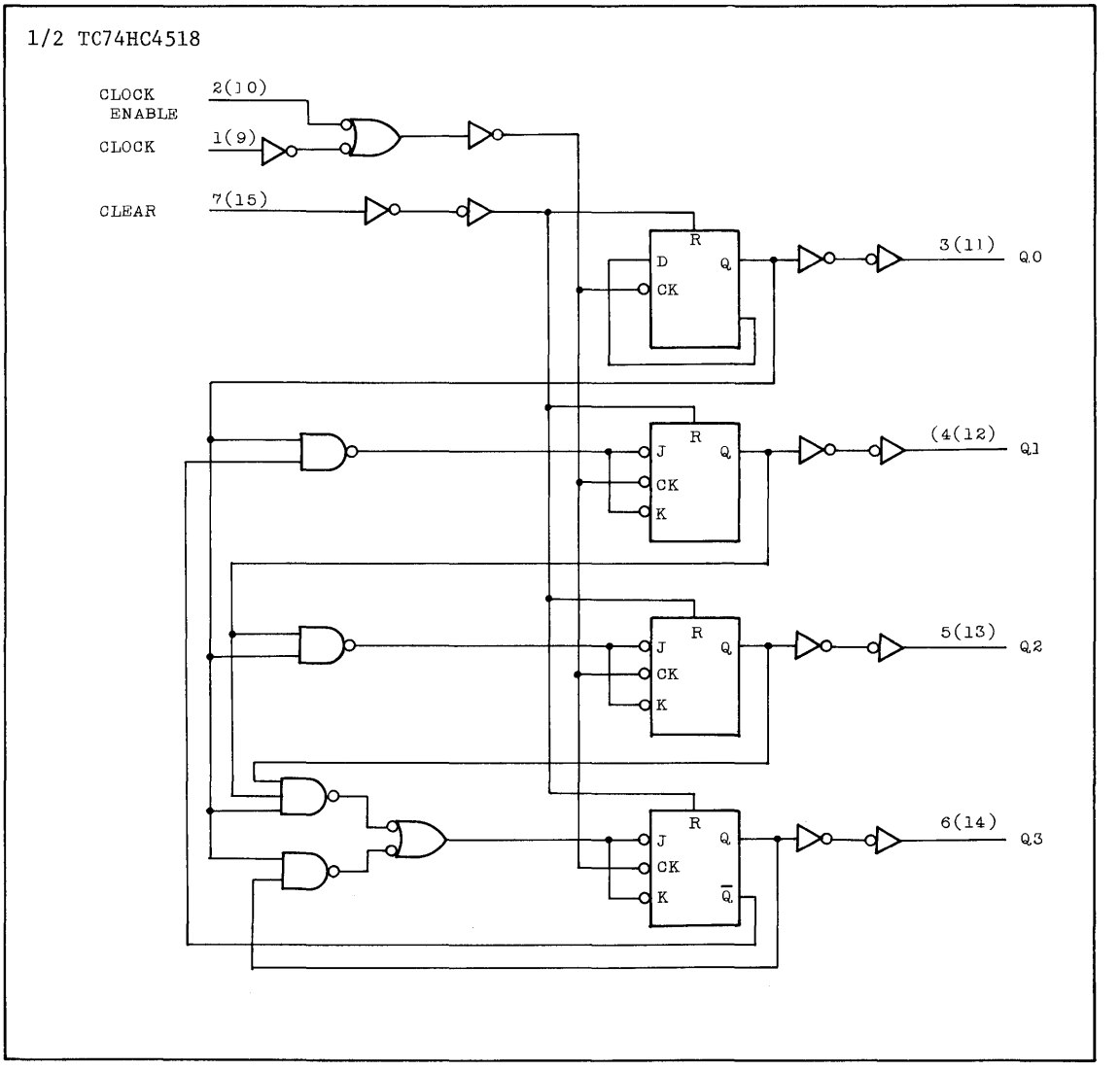
TC74HC4520



TC74HC4518P
TC74HC4520P/F

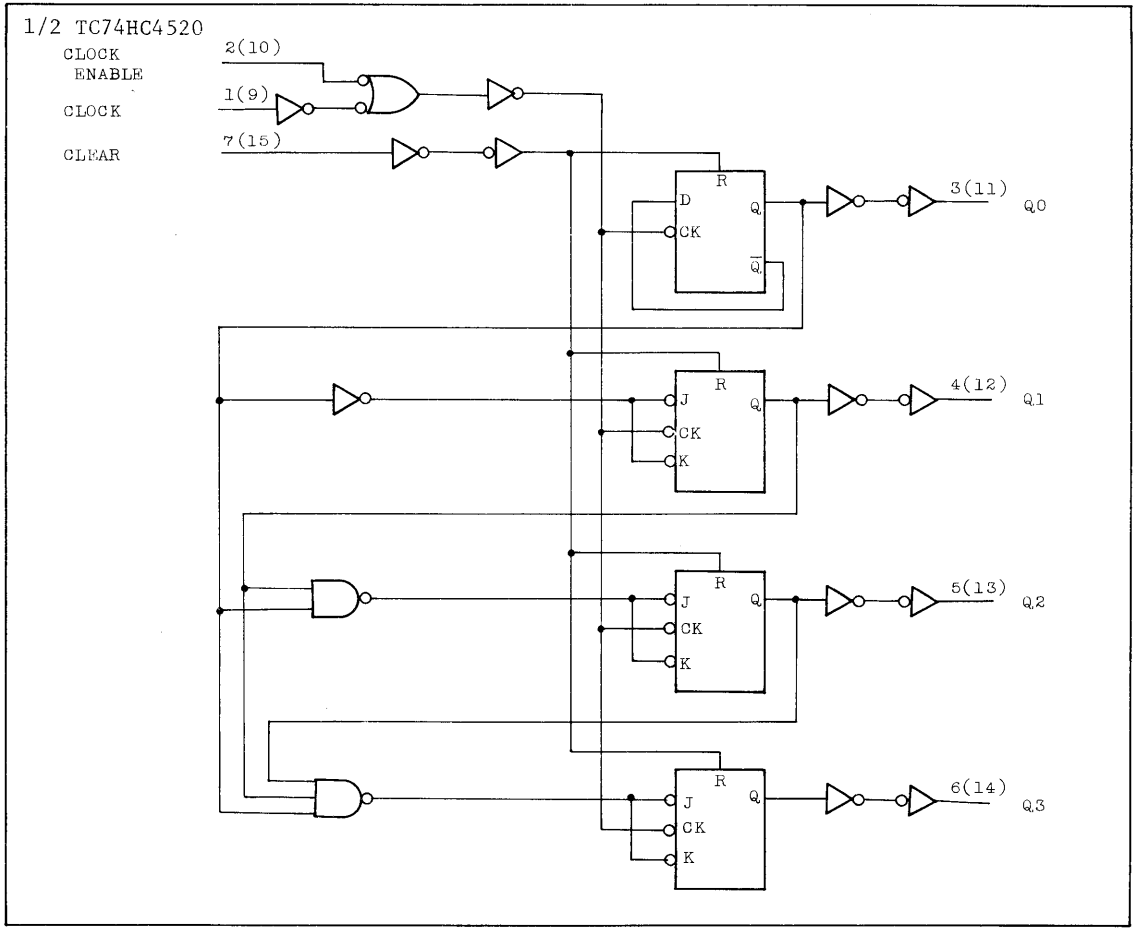
LOGIC DIAGRAM

1/2 TC74HC4518



TC74HC4518P
TC74HC4520P/F

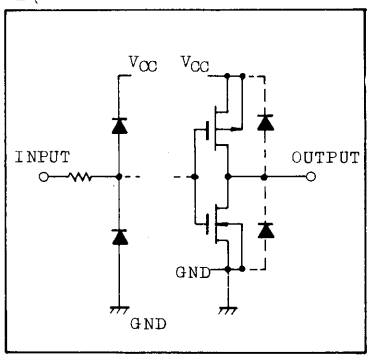
LOGIC DIAGRAM (Continued)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4518P
TC74HC4520P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time (CK, CE - Qn)	t_{pLH} t_{pHL}		2.0	-	100	190	-	240	
			4.5	-	25	38	-	48	
			6.0	-	21	32	-	41	
Propagation Delay Time (CLR - Qn)	t_{pHL}		2.0	-	104	205	-	255	
			4.5	-	26	41	-	51	
			6.0	-	22	35	-	43	
Maximum Clock Frequency	f_{MAX}		2.0	5	12	-	4	-	MHz
			4.5	25	48	-	20	-	
			6.0	29	56	-	24	-	

TC74HC4518P
TC74HC4520P/F

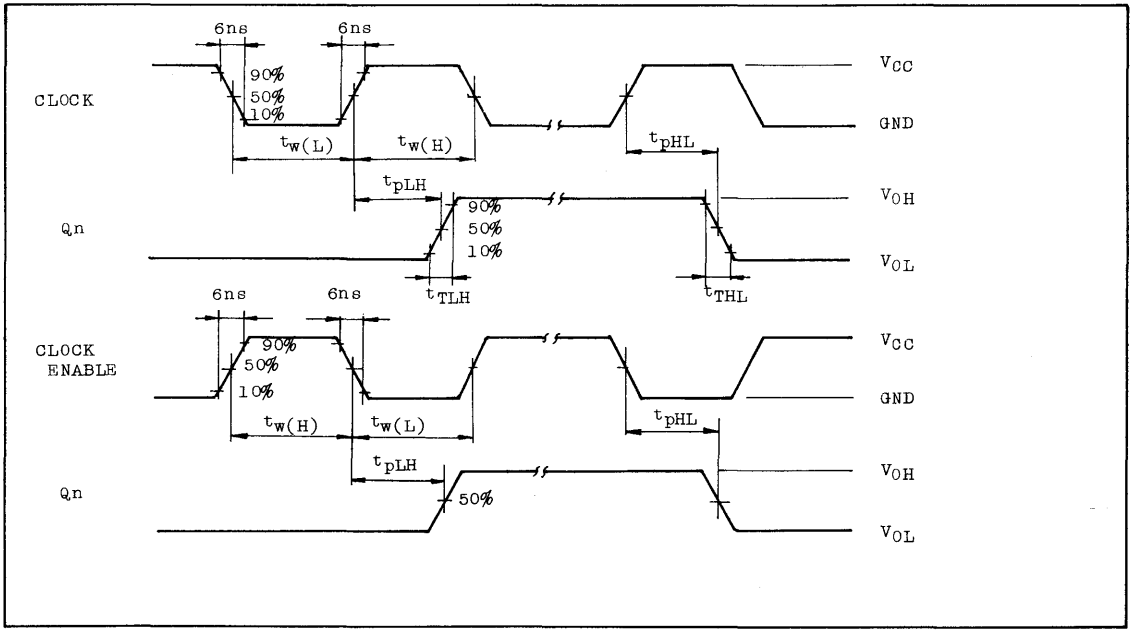
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Pulse Width (CK, CE)	$t_{w(L)}$ $t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum PUlse Width (CLR)	$t_{w(H)}$		2.0	-	35	100	-	125	
			4.5	-	9	20	-	25	
			6.0	-	8	17	-	21	
Minimum Removal Time (CLR)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC4518		-	145	-	-	-	
		TC74HC4520		-	145	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

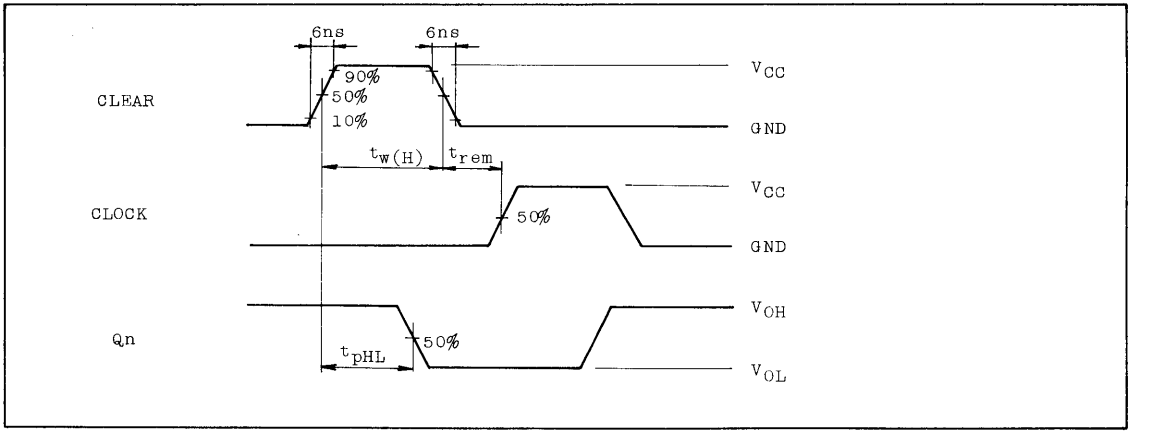
$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad \text{(per circuit)}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM

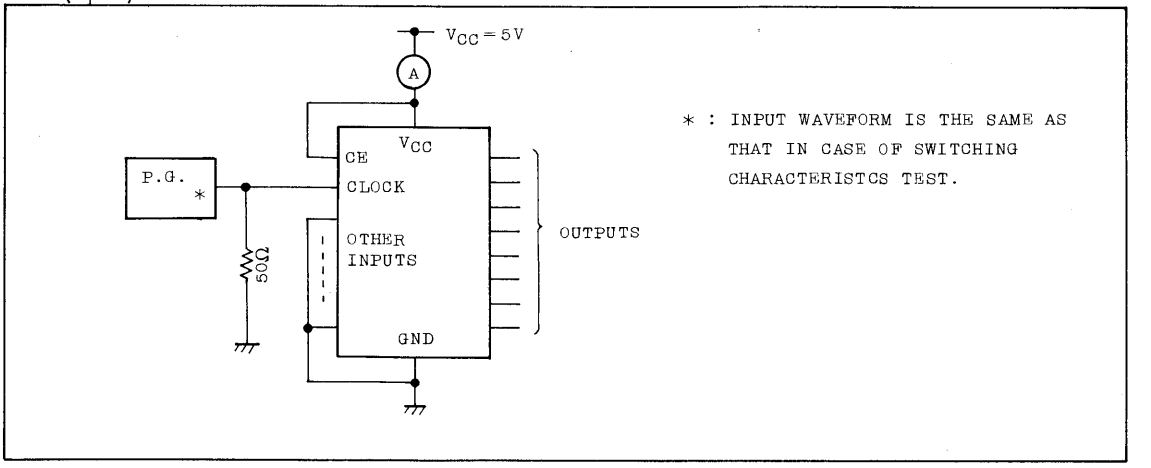


TC74HC4518P
TC74HC4520P/F

SWITCHING CHARACTERISTICS TEST WAVEFORM (Continued)



$I_{CC(Opr.)}$ TEST CIRCUIT



* : INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTCS TEST.

TC74HC4538P/F

PRELIMINARY

TC74HC4538P/F DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

The TC74HC4538 is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology. It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation. There are two trigger inputs. One is A INPUT (Positive-edge input), another is $\overline{B}$ INPUT (Negative-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. After triggering, Output keeps MONO STABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CD}$ input breaks this STABLE STATE. Next coming new trigger in MONO STABLE period is effective, and make MONO STABLE period longer. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation

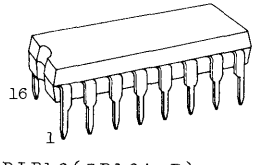
External resistor Rx ..... V_{CC} = 2.0V from 5kΩ to 1MΩ

$V_{CC} \geqq$ 3.0V from 1kΩ to 1MΩ

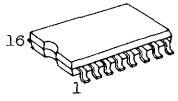
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=27nS(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at V_{CC}=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Wide Output Pulse Width Range ..... t_w(OUT)=120ns ∿ 60s over at V_{CC}=4.5V



DIP16(3D16A-P)



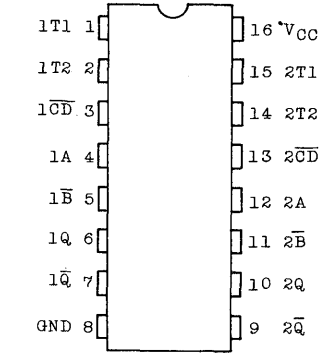
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

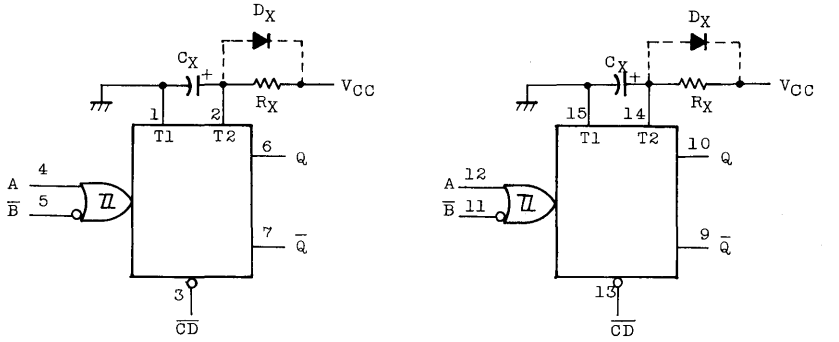
TC74HC4538P/F

TRUTH TABLE

INPUTS			OUTPUTS		NOTE
A	$\overline{B}$	$\overline{CD}$	Q	$\overline{Q}$	
↓	H	H	⌐¬	¬⌐	OUTPUT ENABLE
X	L	H	L	H	INHIBIT
H	X	H	L	H	INHIBIT
L	↑	H	⌐¬	¬⌐	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X : DON'T CARE

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls down rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA.
In the case of large Cx, limitation of falling down time of voltage supply is as follows

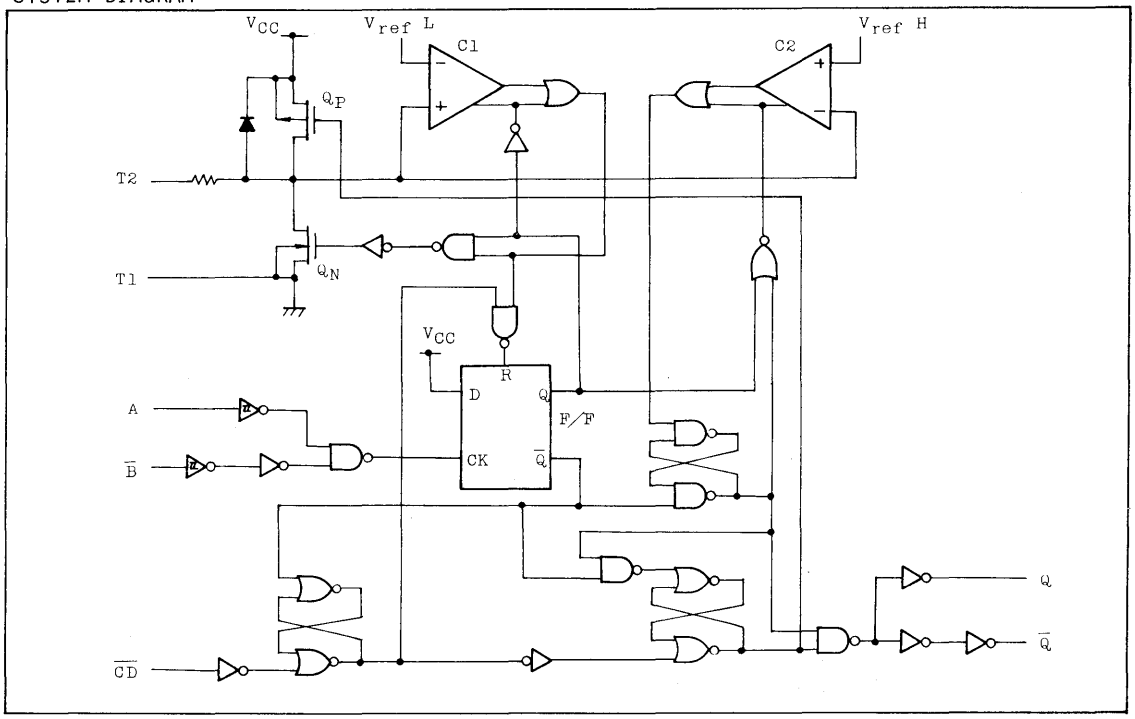
$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC}.)

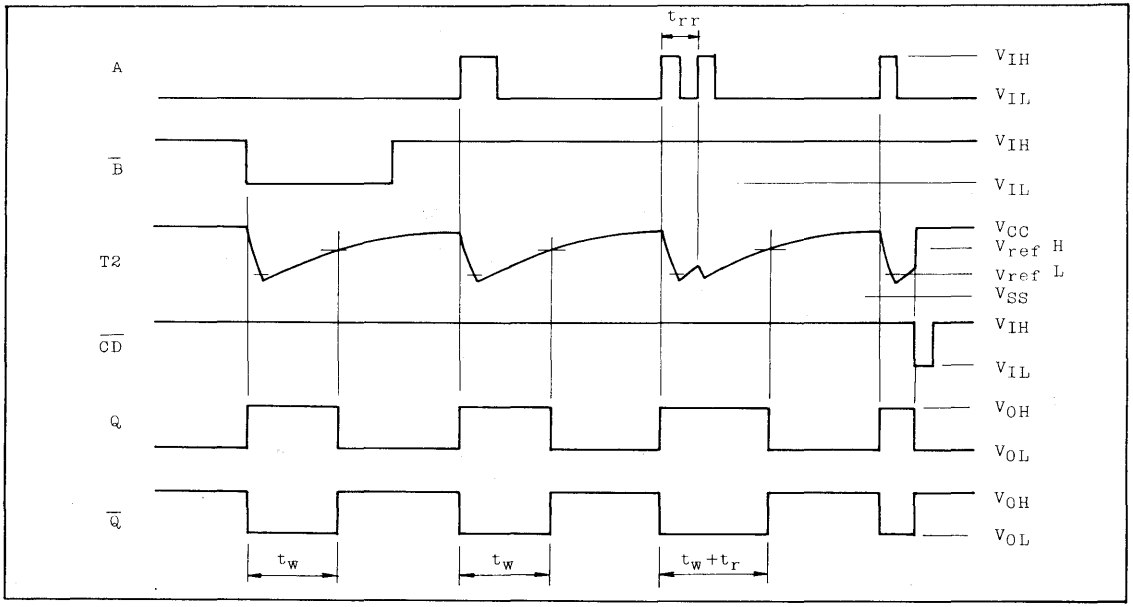
In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current.
See figure.

TC74HC4538P/F

SYSTEM DIAGRAM



TIMING CHART



TC74HC4538P/F

FUCNTIONAL DESCRIPTION

(1) Stand-by State

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (connected to T2 node) are in off state.
Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following two cases. Under the condition A INPUT is "L" level and $\overline{B}$ INPUT have falling down signal. Under the condition $\overline{B}$ INPUT is "H" level and A INPUT has rising up signal.
After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of T2 node becomes lower. If voltage level of T2 falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of T2 starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of T2 changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations.
That means, after triggering the voltage level of T2 becomes VrefH, IC keeps its MONO STABLE STATE.
In the case Cx·Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_{w(OUT)}$ is as follows.

$$t_{w(OUT)} = 0.72\ Cx\ Rx$$

(3) Re-trigger operation

In the case another new trigger in MONO STABLE STATE, the trigger is effective, if IC is in the condition charging capacitor. And the voltage level of T2 falls down to VrefL level again. So that output Q keeps "H" level when next trigger comes in shorter time period than designed period by Cx Rx. In the case 2nd trigger is very close to privious trigger, trigger is not effective, if 2nd trigger comes in the discharge cycle. The minimum time for effective 2nd trigger t_{rr}(Min.) depends on V_{CC} and Cx.

(4) Reset operation

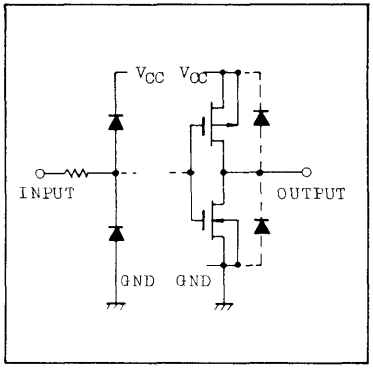
$\overline{CD}$ is normally "H". If $\overline{CD}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level.
This means if $\overline{CD}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

TC74HC4538P/F

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CD}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	3.68	5.80	-	5.63	-	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	-	-	±0.5	-	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	-	-	4.0	-	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/Cext=0.5V_{CC}		2.0	-	40	120	-	160	μA
				4.5	-	0.1	0.3	-	0.4	mA
				6.0	-	0.2	0.6	-	0.8	mA

*: per circuit

TC74HC4538P/F

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($A, \overline{B}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	128	250	-	315	
			4.5	-	32	50	-	63	
			6.0	-	27	43	-	54	
Propagation Delay Time ($\overline{CD}$ - Q, $\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	100	195	-	245	
			4.5	-	25	39	-	49	
			6.0	-	21	33	-	42	
Output Pulse Width	t_{wOUT}	Cx=12pF Rx=1kΩ	3.0	-	210	-	-	-	ns
			5.0	-	140	-	-	-	
		Cx=100pF Rx=10kΩ	3.0	-	1.45	-	-	-	μs
			5.0	-	1.40	-	-	-	
		Cx=1000pF Rx=10kΩ	3.0	-	10.5	-	-	-	
			5.0	-	10.0	-	-	-	
Output Pulse Width Error Between Circuits (In same Package)	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Trigger Pulse Width	$t_{w(H)}$ $t_{w(L)}$	A_{IN} $\overline{B}_{IN}$	2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Removal Time	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{OUT}			-	5	10	-	10	pF
Power Dissipation Capacitance (1)	C_{PD}			-	90	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

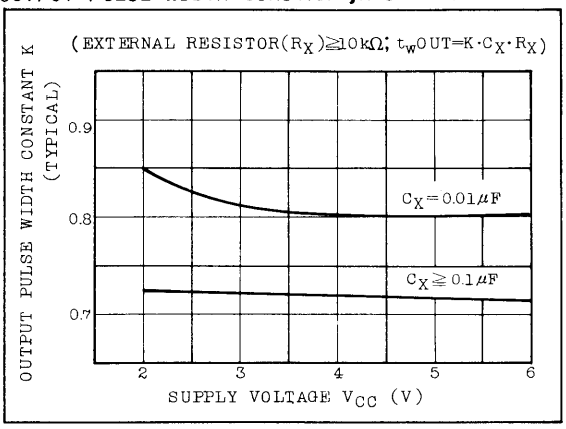
$I_{CC}(opr.)=C_{PD}\cdot V_{CC}\cdot f_{IN}+I_{CC}'\cdot Duty/100+I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current)

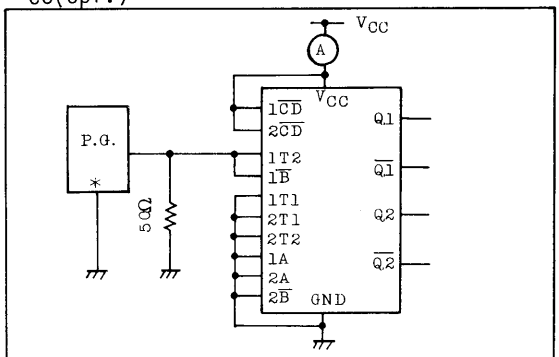
(Duty: %)

TC74HC4538P/F

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE

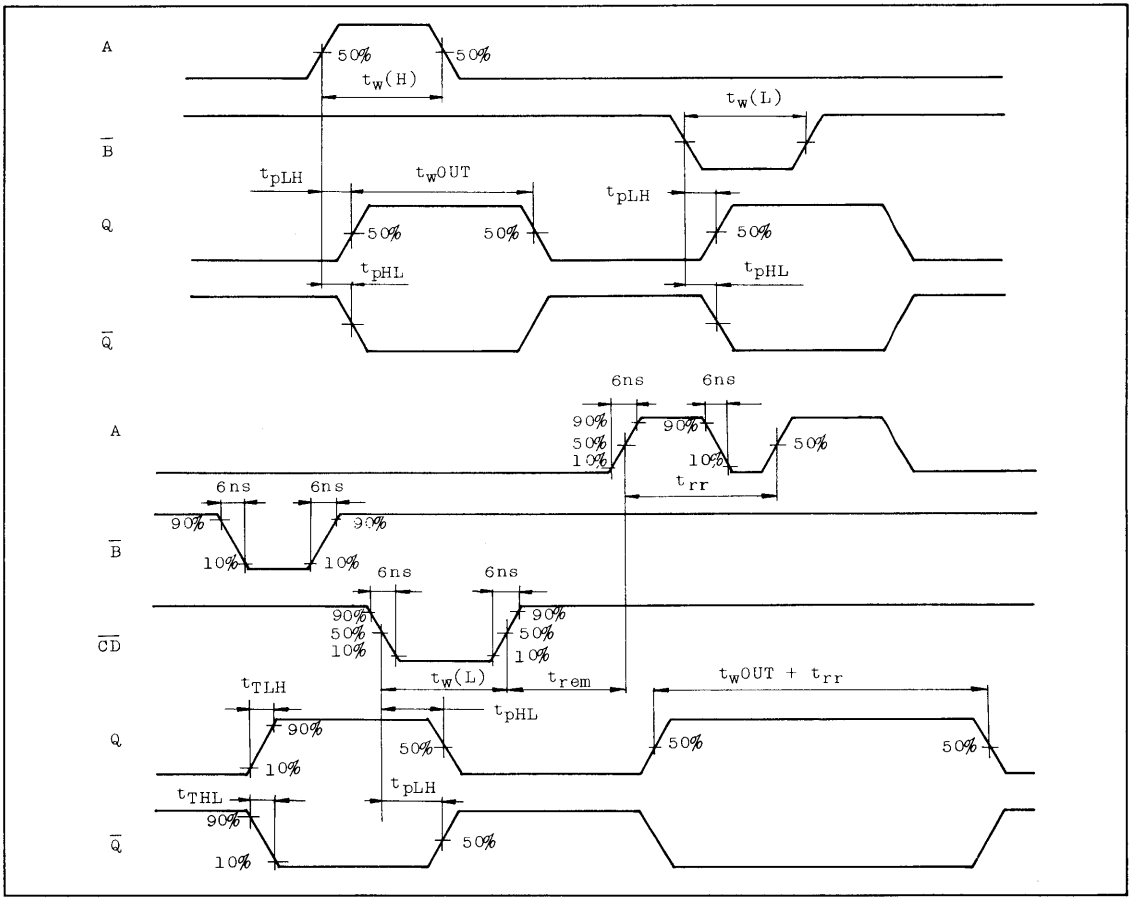


$I_{CC(opr.)}$ TEST WAVEFORM



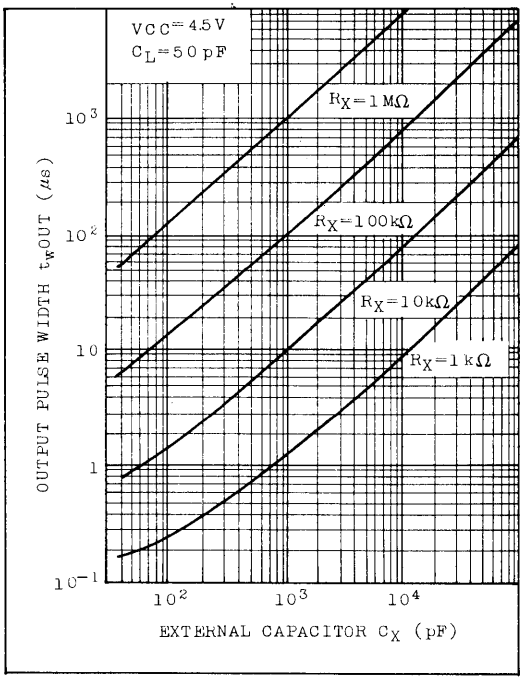
*: INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

SWITCHING CHARACTERISTICS TEST WAVEFORM

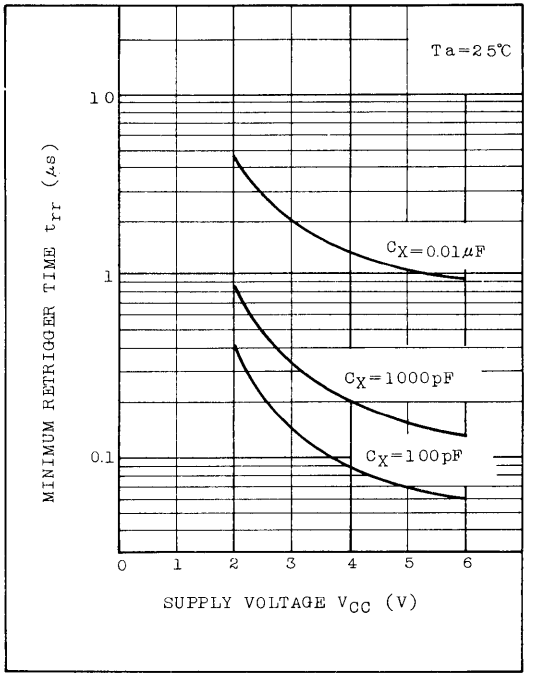


TC74HC4538P/F

t_{wOUT} - Cx CHARACTERISTICS (TYP.)



t_{rr} - V_{CC} CHARACTERISTICS (TYP.)



C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HC4543P/F

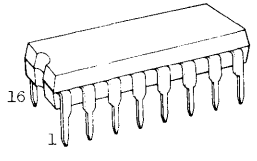
PRELIMINARY

TC74HC4543P/F BCD-TO-7 SEGMENT LATCH/DECODER/LCD DRIVER

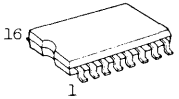
The TC74HC4543 is a high speed CMOS BCD-TO-7 SEGMENT DECODER WITH LCD DRIVER fabricated with silicon gate C^2MOS technology. It achieves the high speed latch and decode operation twenty times as fast as the standard CMOS 4511B while maintaining the CMOS low power dissipation. This device consists of BCD-TO-7 segment decoder with a BCD input latch and a 7-segment driver for the liquid crystal display (LCD). When any illegal BCD input signal is applied or BI input is held high, the display is blanked. In case of driving LCD, a common square wave signal should be applied not only to the PH input of this device but also to the electrically common backplane of the display. For other types of readouts, such as light-emitting diode (LED), some additional drivers, such as transistor array is required. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_w=8ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range ..... V_{CC}(opr.)=2V ∿ 6V
- Pin and Function Compatible with 4543B



DIP16(3D16A-P)



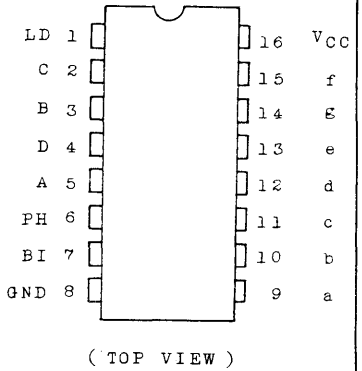
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)* 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

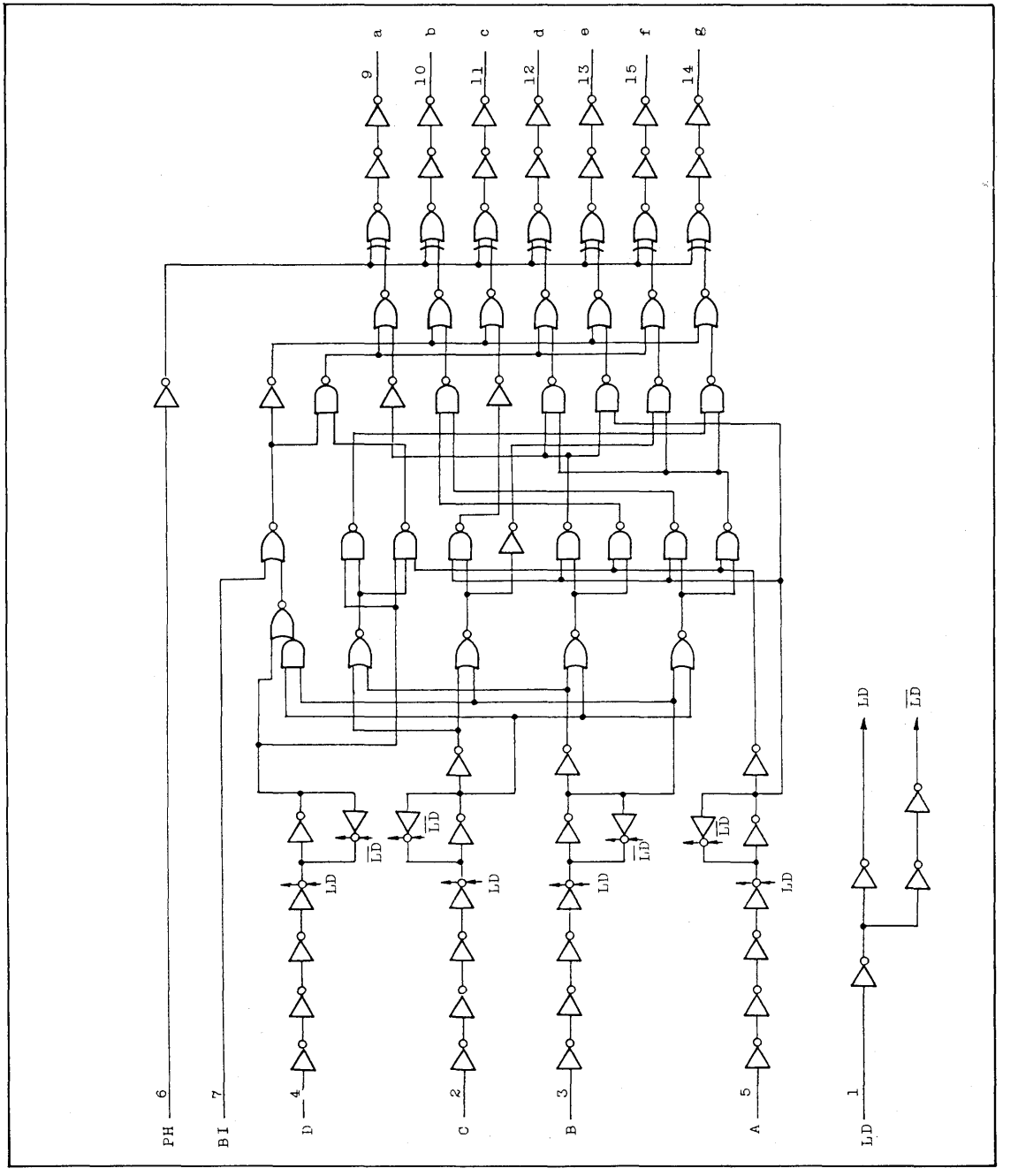
PIN ASSIGNMENT



(TOP VIEW)

TC74HC4543P/F

LOGIC DIAGRAM



TC74HC4543P/F

TRUTH TABLE

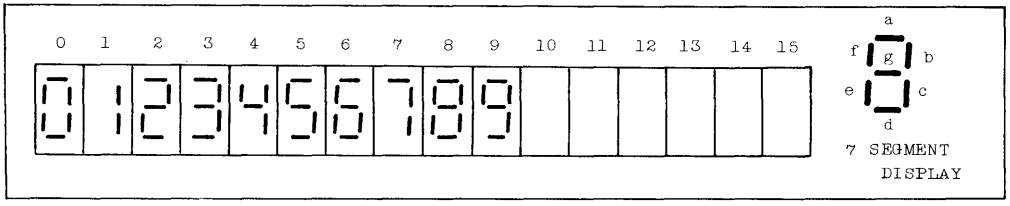
INPUTS							OUTPUTS							DISPLAY
LD	BI	PH	D	C	B	A	a	b	c	d	e	f	g	
X	H	L	X	X	X	X	L	L	L	L	L	L	L	BLANK
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	X	H	X	L	L	L	L	L	L	L	BLANK
H	L	L	H	H	X	X	L	L	L	L	L	L	L	BLANK
L	L	L	X	X	X	X	###							###
↑	↑	H		↑			INVERSE OF ABOVE OUTPUT LEVEL							DISPLAY AS ABOVE

X : DON'T CARE

↑ : SAME AS ABOVE COMBINATIONS

: DEPENDS UPON THE BCD CODE PREVIOUSLY APPLIED WHEN LD="H"

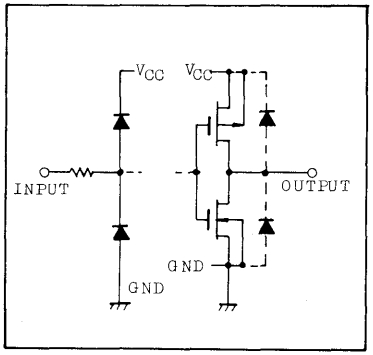
DISPLAY MODE



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



TC74HC4543P/F

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			$I_{OH}=-4mA$	4.5	4.18	4.31	-	4.13	-	
			$I_{OH}=-5.2mA$	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			$I_{OL}=4mA$	4.5	-	0.17	0.26	-	0.33	
			$I_{OL}=5.2mA$	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	4.0	-	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time BCD - OUT	t_{pLH}		2.0	-	200	385	-	480	
			4.5	-	50	77	-	96	
	t_{pHL}		6.0	-	43	65	-	82	
BI - OUT	t_{pLH}		2.0	-	124	240	-	300	
			4.5	-	31	48	-	60	
	t_{pHL}		6.0	-	26	41	-	51	
PH - OUT	t_{pLH}		2.0	-	88	175	-	220	
			4.5	-	22	35	-	44	
	t_{pHL}		6.0	-	19	30	-	37	

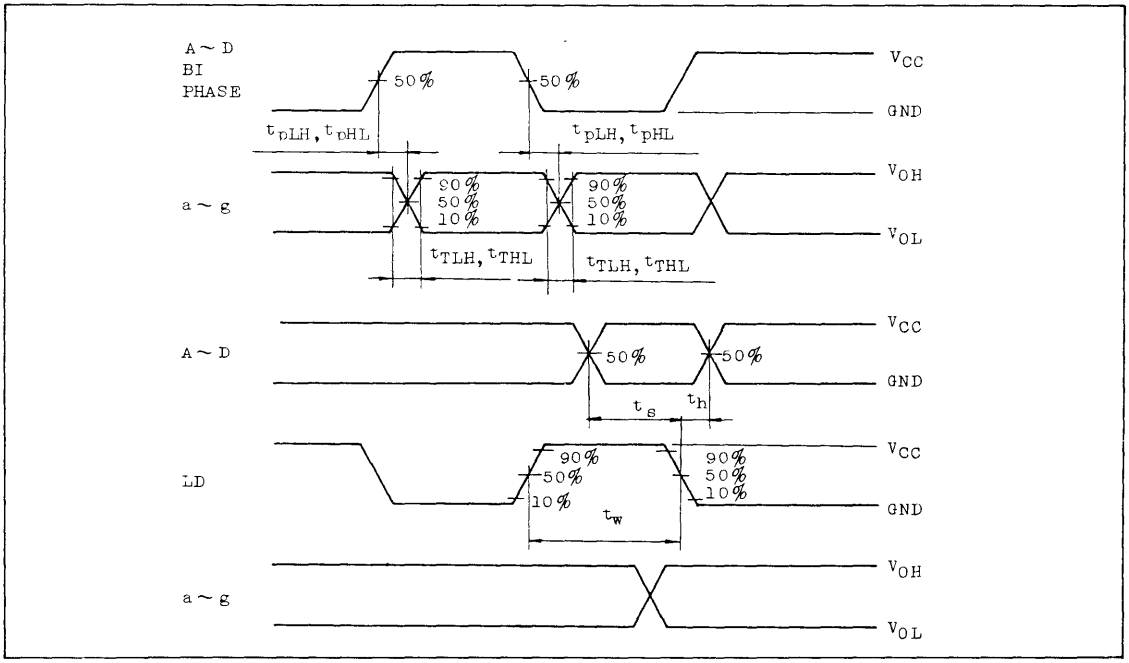
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	25°C MIN.	25°C TYP.	25°C MAX.	-40 ~ 85°C MIN.	-40 ~ 85°C MAX.	UNIT
Minimum Pulse Width (LD)	$t_{w(H)}$		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t_s		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Hold Time	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	$C_{PD}(1)$			-	30	-	-	-	

Note(1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).. Average operating current can be obtained by the equation hereunder.

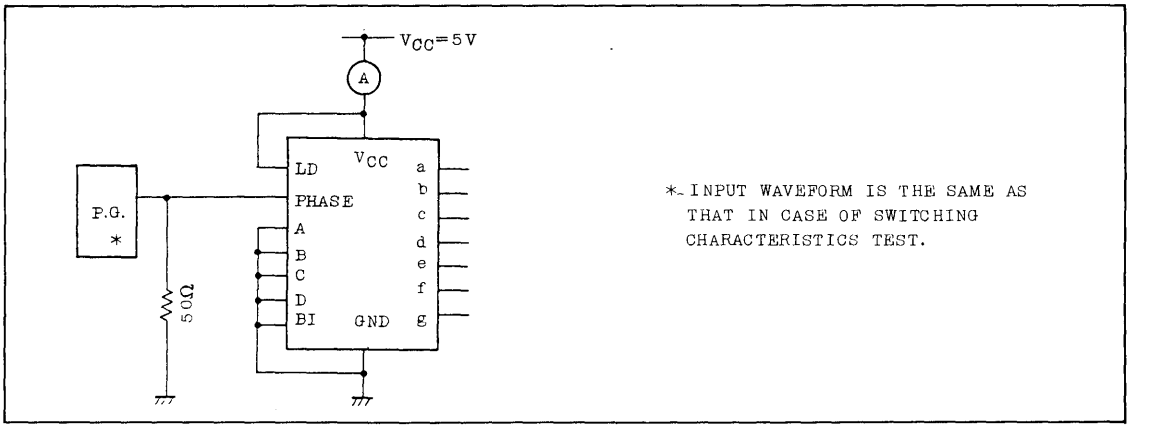
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

SWITCHING CHARACTERISTICS TEST WAVEFORM



TC74HC4543P/F

I_{CC}(opr.) TEST CIRCUIT



*: INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

C²MOS DIGITAL INTEGRATED CIRCUIT

TC74HCT7007P/F

PRELIMINARY

TC74HCT7007P/F HEX BUFFER (TTL INPUT LEVEL)

The TC74HCT07 is a high speed CMOS BUFFER fabricated with silicon gate C^2MOS technology.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

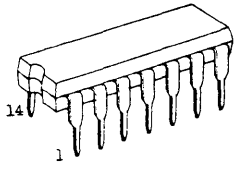
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The internal circuit is composed of 4 stages including buffer output, which enables high noise immunity and stable output.

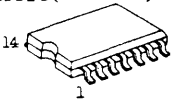
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES

- High Speed ..... t_{pd}=13ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- Compatible with TTL outputs ..... V_{IH}=2V(Min.), V_{IL}=0.8V(Max.)
- Output Drive Capability ..... 10LSTTL Loads
- Symmetrical Output Impedance ..... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS07



DIP14(3D14A-P)



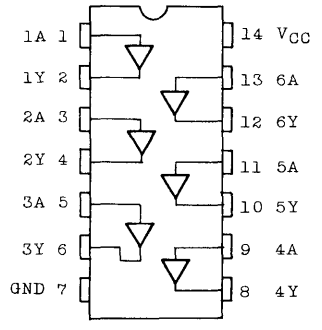
MFP14(F14GB-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*(DIP) 180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

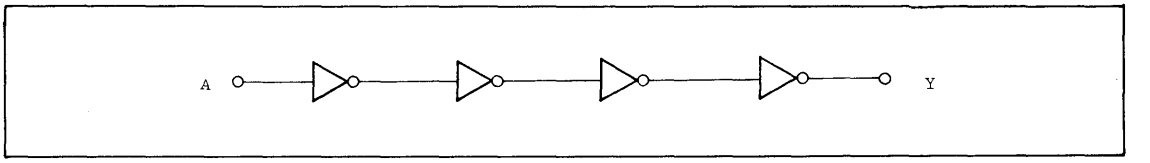
PIN ASSIGNMENT



(TOP VIEW)

TC74HCT7007P/F

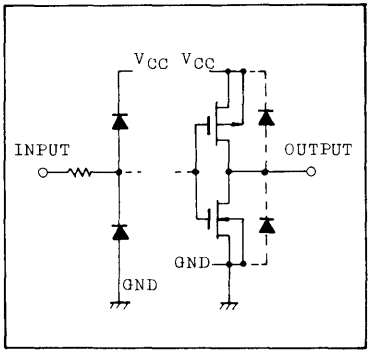
CIRCUIT DIAGRAM (per Circuit)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	4.5 ∿ 5.5	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 500 (V_{CC}=4.5V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			4.5 to 5.5	2.0	-	-	2.0	-	V
Low-Level Input Voltage	V_{IL}			4.5 to 5.5	-	-	0.8	-	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH}	I_{OH}=-20μA	4.5	4.4	4.5	-	4.4	-	V
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	V
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IL}	I_{OL}=20μA	4.5	-	0.0	0.1	-	0.1	V
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	V
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		5.5	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		5.5	-	-	1.0	-	10.0	μA
	I_C	per V_{IN}=0.5V or 2.4V other inputs V_{CC} or GND		5.5	-	-	2.0	-	2.9	mA

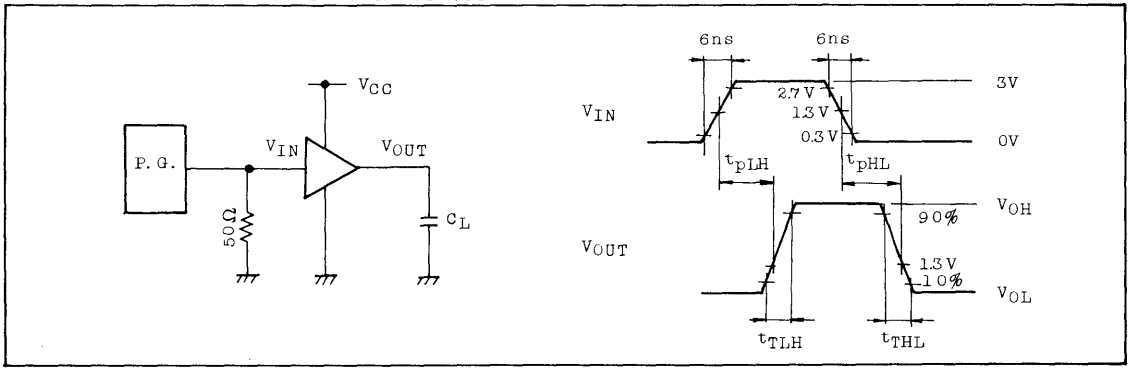
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C			Ta=-40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	-	8	15	-	19	ns
Propagation Delay Time	t_{pLH} t_{pHL}		4.5	-	16	26	-	33	ns
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	28	-	-	-	

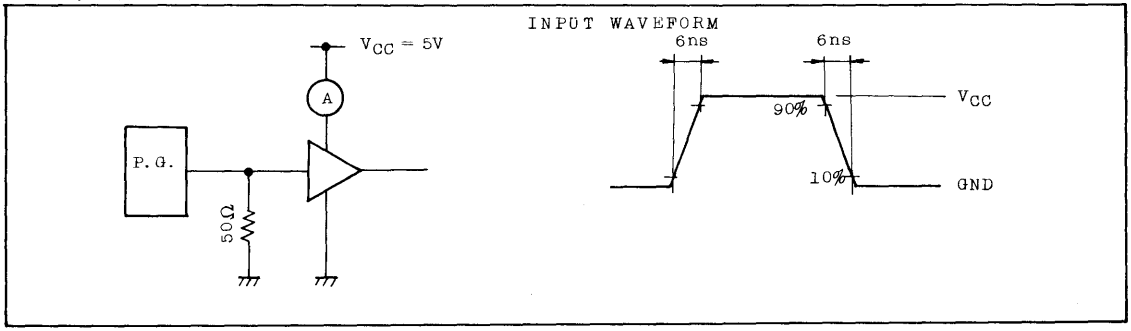
Note 1: C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

$$I_{CC(Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \quad \text{(per gate)}$$

SWITCHING CHARACTERISTICS TEST CIRCUIT



$I_{CC(Opr.)}$ TEST CIRCUIT



TC74HC7266P

C²MOS DIGITAL INTEGRATED CIRCUIT

PRELIMINARY

TC74HC7266P QUAD EXCLUSIVE NOR GATE

The TC74HC266 is a high speed CMOS QUAD EXCLUSIVE NOR GATE fabricated with silicon gate C^2MOS technology.

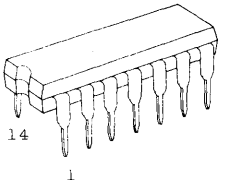
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Input and output buffer are installed, which enables high noise immunity and stable output.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=11ns(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=1μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH} \fallingdotseq t_{pHL}$
- Wide Operating Voltage Range .....$V_{CC(opr.)}$=2V ∿ 6V
- Pin and Function Compatible with 74LS266



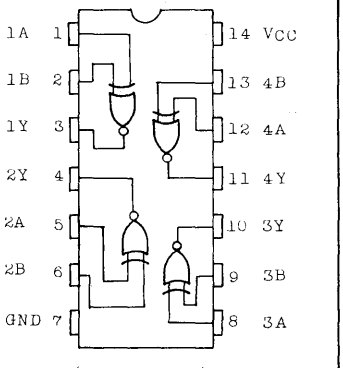
DIP14(3D14A-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ∿ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

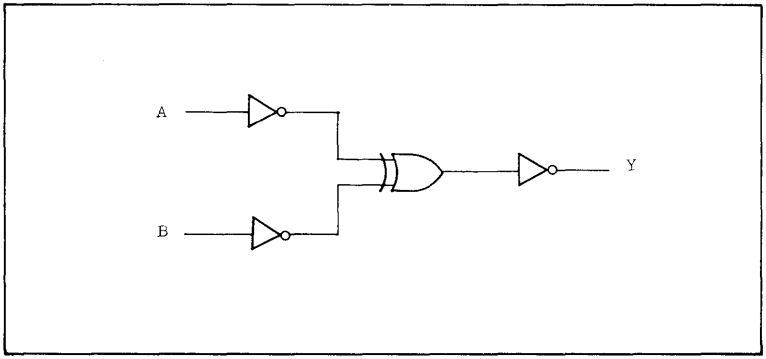
PIN ASSIGNMENT



(TOP VIEW)

TC74HC7266P

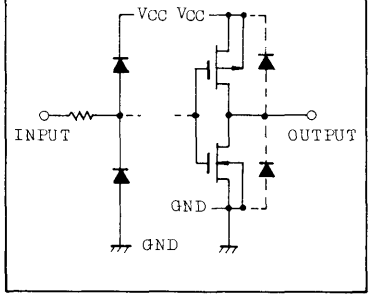
LOGIC DIAGRAM (per Gate)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	-40 ∿ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION			Ta=25°C			Ta=-40∿85°C		UNIT
				V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V_{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I_{OH}=-4mA	4.5	4.18	4.31	-	4.13	-	
			I_{OH}=-5.2mA	6.0	5.68	5.80	-	5.63	-	

TC74HC7266P

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL}	I_{OL}=20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I_{OL}=4mA	4.5	-	0.17	0.26	-	0.33	
			I_{OL}=5.2mA	6.0	-	0.18	0.26	-	0.33	
Input Leakage Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND		6.0	-	-	1.0	-	10.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40∿85°C MIN.	Ta=-40∿85°C MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
	t_{THL}		6.0	-	7	13	-	16	
Propagation Delay Time	t_{pLH}		2.0	-	52	115	-	145	
			4.5	-	13	23	-	29	
	t_{pHL}		6.0	-	11	20	-	25	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	34	-	-	-	

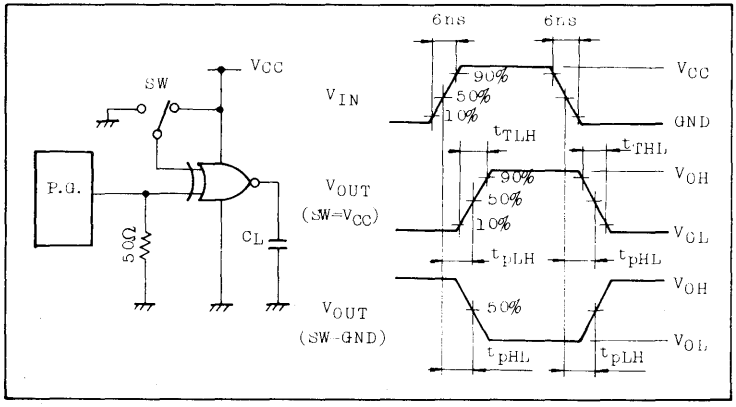
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

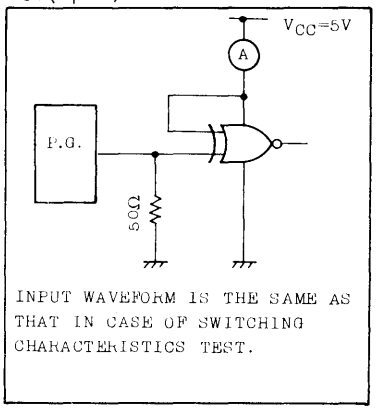
$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \quad \text{(per Gate)}$$

TC74HC7266P

SWITCHING CHARACTERISTICS TEST CIRCUIT



I_{CC}(opr.) TEST CIRCUIT

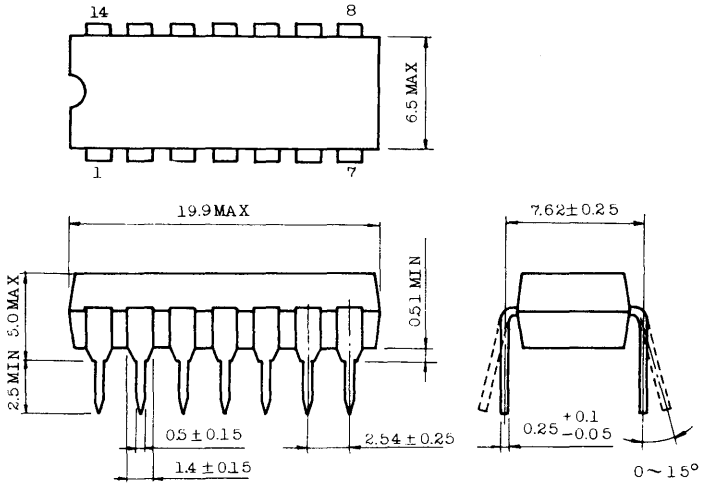


INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

4. OUTLINE DRAWINGS

DIP 14 PIN OUTLINE DRAWING (3D14A-P)

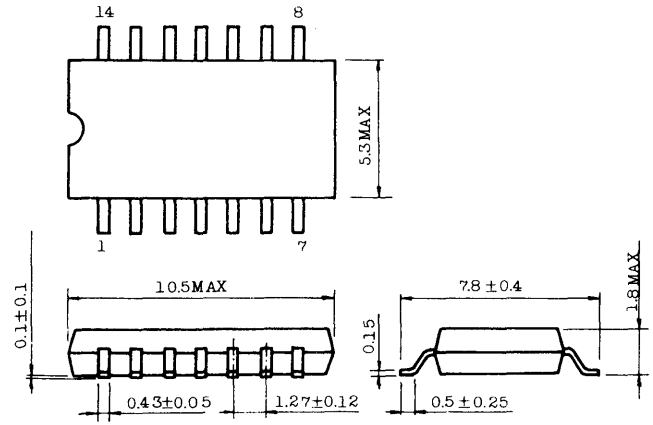
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

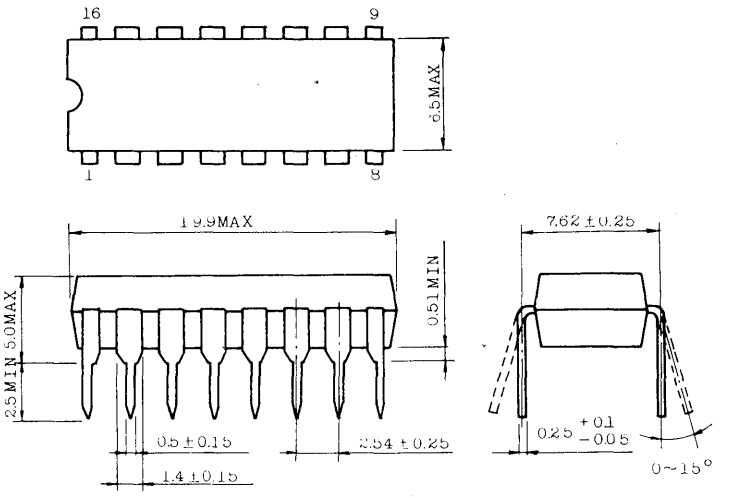
MFP 14 PIN OUTLINE DRAWING (F14GB-P) JEDEC-MO-46-AA

Unit in mm



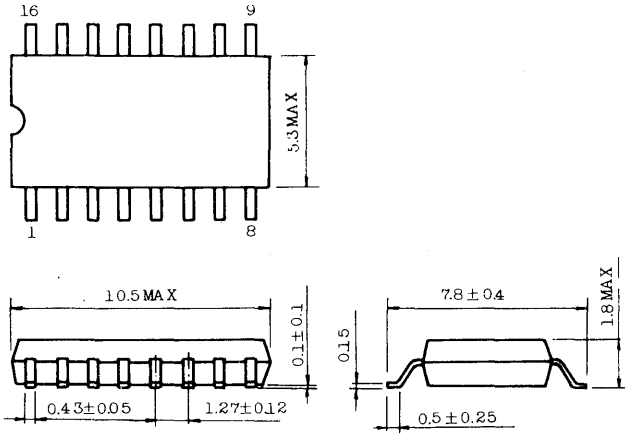
Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.14 leads.

DIP 16 PIN OUTLINE DRAWING (3D16A-P) Unit in mm



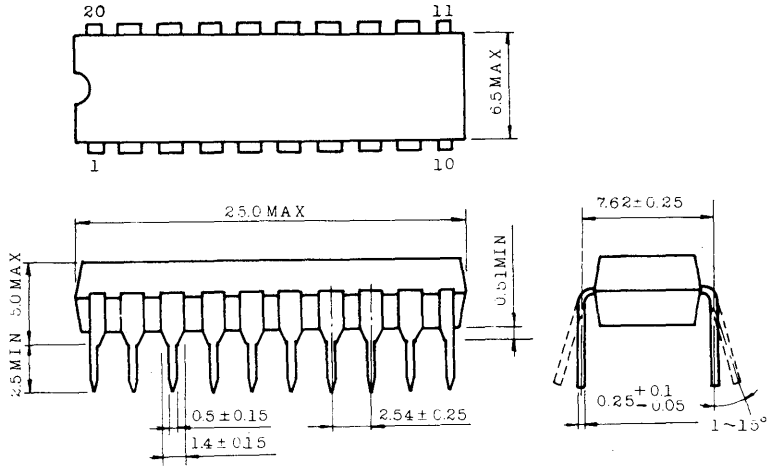
Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

MFP 16 PIN OUTLINE DRAWING (F16GC-P) JEDEC-MO-46-AB Unit in mm



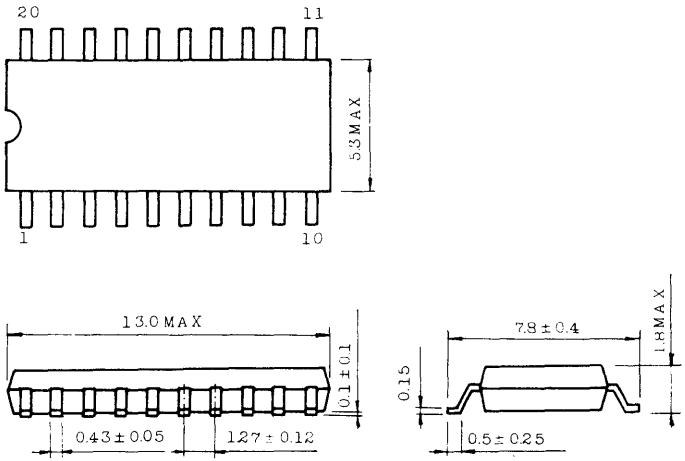
Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

DIP 20 PIN OUTLINE DRAWING (3D20A-P) Unit in mm



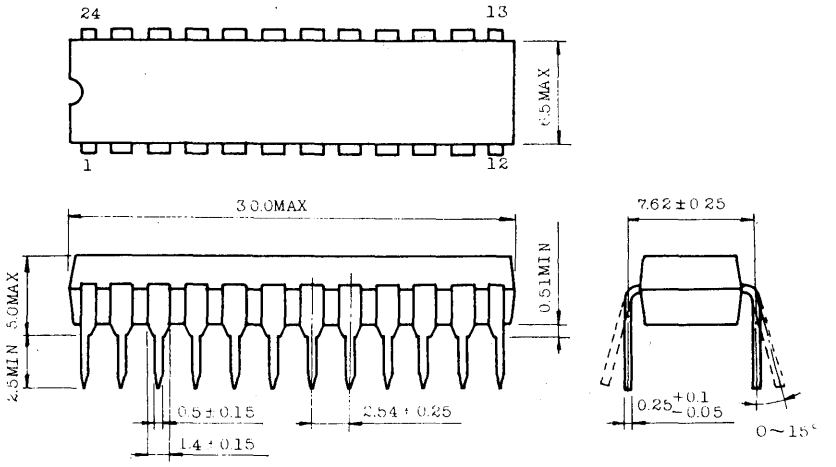
Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.20 leads.

MFP 20 PIN OUTLINE DRAWING (F20GA-P) JEDEC-MO-46-AC Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.20 leads.

DIP 24 PIN OUTLINE DRAWING (3D24A-P) Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.