TOSHIBA AMERICA, INC.

MOS
MEMORY

1988

TOSHIBA

MOS MEMORY PRODUCTS

DATA BOOK

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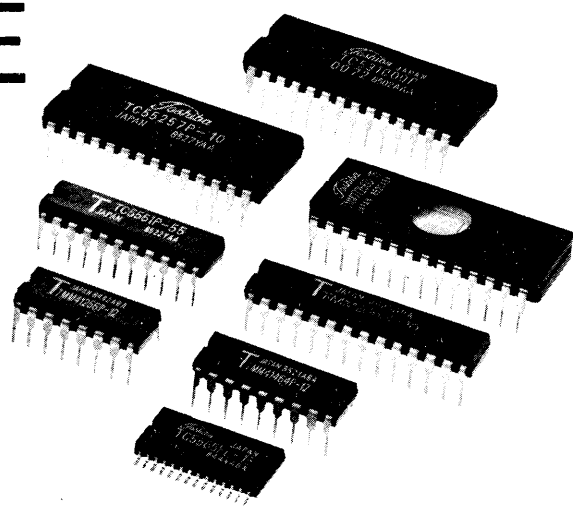
STATIC RANDOM ACCESS MEMORIES

NON-VOLATILE MEMORIES

MEMORY
PRODUCT
GUIDE



A. Dynamic RAM

1. Standard DRAM

Capacity	Part Number	Organization	Access Time Max (ns)		Cycle Time Min (ns)	Process	Power Dissipation Max S/B (mW)		Pins	Operating Mode
			tRAC	tCAC			Active	Standby		
256K Bit	TMM41256AP/AT/AZ-10 TMM41256AP/AT/AZ-12 TMM41256AP/AT/AZ-15	262,144×1	100 120 150	50 60 75	190 220 260	NMOS	440 396 358	28	16/18/16	Page
	TMM41257AP/AT/AZ-10 TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15	262,144×1	100 120 150	50 60 75	190 220 260	NMOS	440 396 358	28	16/18/16	Nibble
	TMM41464AP/AT/AZ-10 TMM41464AP/AT/AZ-12 TMM41464AP/AT/AZ-15	65,536×4	100 120 150	50 60 75	190 220 260	NMOS	440 396 358	28	18/18/20	Page

Note: Package Type P: Plastic Dip; T: PLCC; Z: Zip

1. Standard DRAM (Continued)

Capacity	Part Number	Organization	Access Time Max (ns)		Cycle Time Min (ns)	Process	Power Dissipation Max S/B (mW)		Pins	Operating Mode
			tRAC	tCAC			Active	Standby		
1M Bit	TC511000P/J/Z-85 TC511000P/J/Z-10 TC511000P/J/Z-12	1,048,576×1	85 100 120	25 25 30	165 190 220	CMOS	385 330 275	5.5	18/26/20	Fast Page
	TC511000PL/JL/ZL-85 TC511000PL/JL/ZL-10 TC511000PL/JL/ZL-12	1,048,576×1	85 100 120	25 25 30	165 190 220	CMOS	385 330 275	1.7	18/26/20	Fast Page Low Power
	TC511000AP/AJ/AZ-70 TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-100	1,048,576×1	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	5.5	18/26/20	Fast Page
	TC511000APL/AJL/AZL-70 TC511000APL/AJL/AZL-80 TC511000APL/AJL/AZL-10	1,048,576×1	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	1.1	18/26/20	Fast Page Low Power
	TC511001P/J/Z-85 TC511001P/J/Z-10 TC511001P/J/Z-12	1,048,576×1	85 100 120	30 35 40	165 190 220	CMOS	385 330 275	5.5	18/26/20	Nibble
	TC511001AP/AJ/AZ-70 TC511001AP/AJ/AZ-80 TC511001AP/AJ/AZ-10	1,048,576×1	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	5.5	18/26/20	Nibble
	TC511002P/J/Z-85 TC511002P/J/Z-10 TC511002P/J/Z-12	1,048,576×1	85 100 120	25 25 30	165 190 220	CMOS	385 330 275	5.5	18/26/20	Static Column
	TC511002AP/AJ/AZ-70 TC511002AP/AJ/AZ-80 TC511002AP/AJ/AZ-10	1,048,576×1	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	5.5	18/26/20	Static Column
	TC514256P/J/Z-85 TC514256P/J/Z-10 TC514256P/J/Z-12	262,144×4	85 100 120	30 30 35	165 190 220	CMOS	413 358 303	5.5	20/26/20	Fast Page
	TC514256PL/JL/ZL-85 TC514256PL/JL/ZL-10 TC514256PL/JL/ZL-12	262,144×4	85 100 120	30 30 35	165 190 220	CMOS	413 358 303	1.7	20/26/20	Fast Page Low Power
	TC514256AP/AJ/AZ-70 TC514256AP/AJ/AZ-80 TC514256AP/AJ/AZ-10	262,144×4	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	5.5	20/26/20	Fast Page
	TC514256APL/AJL/AZL-70 TC514256APL/AJL/AZL-80 TC514256APL/AJL/AZL-10	262,144×4	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	1.1	20/26/20	Fast Page Low Power
	TC514266AP/AJ/AZ-70 TC514266AP/AJ/AZ-80 TC514266AP/AJ/AZ-10	262,144×4	70 80 100	20 20 25	130 150 180	CMOS	440 385 330	5.5	20/26/20	Fast Page Write-Per-Bit
	TC514258P/J/Z-85 TC514258P/J/Z-10 TC514258P/J/Z-12	262,144×4	85 100 120	30 30 35	165 190 220	CMOS	413 358 303	5.5	20/26/20	Static Column
	TC514258AP/AJ/AZ-70 TC514258AP/AJ/AZ-80 TC514258AP/AJ/AZ-10	262,144×4	70 80 100	25 25 30	130 150 180	CMOS	440 385 330	5.5	20/26/20	Static Column
	TC514268AP/AJ/AZ-70 TC514268AP/AJ/AZ-80 TC514268AP/AJ/AZ-10	262,144×4	70 80 100	25 25 30	130 150 180	CMOS	440 385 330	5.5	20/26/20	Static Column, Write-Per-Bit

2. Video RAM

Capacity	Part Number	Organization	Random Port Access Time		Serial Port Access Time	Cycle Time Min (ns)	Power Dissipation Max (mW)		Pins	Operating Mode
			tRAC	tCAC			Active	Standby		
1M Bit	TC521000P	32K×8×4	—	—	20	190	550	110	40	Serial-In Serial-Out
	TC524256P/Z-10	RAM Port: 256×4 SAM Port: 512×4	100	50	25	190	550	110	28	Random Port: Page Mode Write-Per-Bit Serial Port: Serial Input-Output
	TC524256J-10								32	
	TC524256P/Z-12		120	60	35	220	495	110	28	
	TC524256J-12								32	

Note: Package P :Plastic Dip; Z: Plastic Zip; J: SOJ

3. DRAM Modules

Organization	Part Number	Access time	Pins	Assembly side	Pin type	Height max (mm)	Comment
1M×4	THM41000L-85 THM41000L-10 THM41000L-12	85 100 120	25	Single	Pin	12.64	Fast Page
	THM41001L-85 THM41001L-10 THM41001L-12	85 100 120					Nibble
	THM41002L-85 THM41002L-10 THM41002L-12	85 100 120					Static Column
512K×8	THM8512S-85 THM8512S-10 THM8512S-12	85 100 120	30	Single	Socket	15.24	Fast Page
	THM8512L-85 THM8512L-10 THM8512L-12	85 100 120			Pin	17.52	
	THM8514S-85 THM8514S-10 THM8514S-12	85 100 120			Socket	15.24	Static Column
	THM8514L-85 THM8514L-10 THM8514L-12	85 100 120			Pin	17.52	
1M×8	THM81000S-85 THM81000S-10 THM81000S-12	85 100 120	30	Single	Socket	20.45	Fast Page
	THM81000L-85 THM81000L-10 THM81000L-12	85 100 120			Pin	22.6	
	THM81001S-85 THM81001S-10 THM81001S-12	85 100 120			Socket	20.45	Nibble
	THM81001L-85 THM81001L-10 THM81001L-12	85 100 120			Pin	22.6	
	THM81002S-85 THM81002S-10 THM81002S-12	85 100 120			Socket	20.45	Static Column
	THM81002L-85 THM81002L-10 THM81002L-12	85 100 120			Pin	22.6	
	* THM81020L-85 * THM81020L-10 * THM81020L-12	85 100 120	30	Double	Pin	12.64	Fast Page
	* THM81021L-85 * THM81021L-10 * THM81021L-12	85 100 120					Nibble
	* THM81022L-85 * THM81022L-10 * THM81022L-12	85 100 120					Static Column

* : Under Development

3. DRAM Modules (Continued)

Organization	Part Number	Access time	Pins	Assembly side	Pin type	Height max (mm)	Comment
1M×9	THM91000S-85 THM91000S-10 THM91000S-12	85 100 120	30	Single	Socket	20.45	Fast Page
	THM91000L-85 THM91000L-10 THM91000L-12	85 100 120			Pin	22.6	
	THM91001S-85 THM91001S-10 THM91001S-12	85 100 120			Socket	20.45	Nibble
	THM91001L-85 THM91001L-10 THM91001L-12	85 100 120			Pin	22.6	
	THM91002S-85 THM91002S-10 THM91002S-12	85 100 120			Socket	20.45	Static Column
	THM91002L-85 THM91002L-10 THM91002L-12	85 100 120			Pin	22.6	
	THM91010S-85 THM91010S-10 THM91010S-12	85 100 120	30	Single	Socket	20.45	Fast Page 9 I/O Common
	THM91010L-85 THM91010L-10 THM91010L-12	85 100 120			Pin	22.6	
	THM91020L-85 THM91020L-10 THM91020L-12	85 100 120	30	Double	Pin	12.64	Fast Page
	THM91021L-85 THM91021L-10 THM91021L-12	85 100 120					Nibble
	THM91022L-85 THM91022L-10 THM91022L-12	85 100 120					Static Column
256K×36	* THM362500S-85 * THM362500S-10 * THM362500S-12	85 100 120	72	Single	Socket	25.53	Fast Page

* : New Product

B. Static RAMs

1. Standard SRAM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Process	Power Dissipation Max (mW)		Pins	Package Width (inch)
						Active	Standby		
64K Bit	TMM2063P-10 TMM2063P-12 TMM2063P-15	8,192×8	100 120 150	100 120 150	NMOS	440	55	28	0.3
	TMM2063AP-70 TMM2063AP-10 TMM2063AP-12	8,192×8	70 100 120	70 100 120	NMOS	440	55	28	0.3
	TMM2064P-10 TMM2064P-12 TMM2064P-15	8,192×8	100 120 150	100 120 150	NMOS	440	55	28	0.6
	TMM2064AP-70 TMM2064AP-10 TMM2064AP-12	8,192×8	70 100 120	70 100 120	NMOS	440	55	28	0.6
	TC5563APL-10 TC5563APL-12 TC5563APL-15	8,192×8	100 120 150	100 120 150	CMOS	27.5	0.55	28	0.3
	TC5563APL-10L TC5563APL-12L TC5563APL-15L		100 120 150	100 120 150			0.165		
	TC5565APL/AFL-10 TC5565APL/AFL-12 TC5565APL/AFL-15	8,192×8	100 120 150	100 120 150	CMOS	27.5	0.55	28	0.6 (P) 0.45 (F)
	TC5565APL/AFL-10L TC5565APL/AFL-12L TC5565APL/AFL-15L		100 120 150	100 120 150			0.165		
	TC5564APL/AFL-15 TC5565APL/AFL-20	8,192×8	120 150	120 150	CMOS	27.5	0.005	28	0.6 (P) 0.45 (F)
256K Bit	TC55257APL/AFL-85 TC55257APL/AFL-10 TC55257APL/AFL-12	32,768×8	85 100 120	85 100 120	CMOS	60	0.55	28	0.6 (P) 0.45 (F)
	TC55257APL/AFL-85L TC55257APL/AFL-10L TC55257APL/AFL-12L		85 100 120	85 100 120			0.165		
	* TC55256PL/FL-10 * TC55256PL/FL-12	32,768×8	100 120	100 120	CMOS	60	0.005	28	0.6 (P) 0.45 (F)
1M Bit	**TC551001P/F-70 **TC551001P/F-10 **TC551001P/F-12	131,072×8	70 100 120	70 100 120	CMOS	60	0.55	32	0.6 (P) 0.45 (F)

Note: Package Material: P :Plastic Dip; F: Flat Package (SOP)
* : New Product ** : Under Development

2. CMOS Pseudo Static RAM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Power Dissipation Max (mW)		Pins	Package Width (inch)
						Active	Standby		
256K Bit	TC51832P/SP/F-85	32,768×8	85	135	+5±10%	303	5.5	28	0.6 (P) 0.3 (SP) 0.45 (F)
	TC51832P/SP/F-10		100	160		248			
	TC51832P/SP/F-12		120	190		220			
	TC51832PL/SPL/FL-85		85	135		303	0.55		
	TC51832PL/SPL/FL-10		100	160		248			
	TC51832PL/SPL/FL-12		120	190		220			
1M Bit	* TC518128P-10	131,072×8	PS 100 VS 160	160 220	+5±10%	330	5.5	32	0.6 (P) 0.45 (F)
	* TC518128P-12		PS 120 VS 190	190 260		275			
	* TC518128PL-10		PS 100 VS 160	160 220		330	0.55		
	* TC518128PL-12		PS 120 VS 190	190 260		275			
	**TC518128F-10		PS 100 VS 160	160 220		330	5.5		
	**TC518128F-12		PS 120 VS 190	190 260		275			
	**TC518128FL-10		PS 100 VS 160	160 220		330	0.55		
	**TC518128FL-12		PS 120 VS 190	190 260		275			

Note: Package material P: Plastic Dip; SP: Slim Plastic DIP; F: Flat Package (SOP)
Function: PS: Pseudo Static Mode; VS: Virtually Static Mode
*: New Product; **: Under Development

3. High Speed Static RAM

Capacity	Part No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Process	Power Dissipation max (mW)		Pins	Package Width (inch)
						Active	Standby		
16K Bit	TMM2018AP-25 TMM2018AP-35 TMM2018AP-45	2,048×8	25 35 45	25 35 45	NMOS	825 742.5	110	24	0.3
	TMM2068AP-25 TMM2068AP-35 TMM2068AP-45	2,048×8	25 35 45	25 35 45	NMOS	742.5 660	110	20	0.3
	TMM2088P-35 TMM2088P-45	8,192×8	35 45	35 45	NMOS	742.5	82.5	28	0.3
	TMM2089P-35 TMM2089P-45	8,192×9	35 45	35 45	NMOS	742.5	82.5	28	0.3
	TC5561P/J-45 TC5561P/J-55	65,536×1	45 55	45 55	CMOS	550	0.55	22(P) 24(J)	0.3 (P) 0.3 (J)
	TC5562P/J-35 TC5562P/J-45	65,536×1	35 45	35 45	CMOS	550	11	22(P) 24(J)	0.3 (P) 0.3 (J)
	TC55416P/J-25 TC55416P/J-35	16,384×4	25 35	25 35	CMOS	660	110	22(P) 24(J)	0.3 (P) 0.3 (J)
	TC55417P/J-25 TC55417P/J-35	16,384×4	25 35	25 35	CMOS	660	110	24(P) 24(J)	0.3 (P) 0.3 (J)
	* TC5588P/J-20 * TC5588P/J-25	8,192×8	20 25	20 25	CMOS	550	110	28	0.3
	* TC5589P/J-20 * TC5589P/J-25	8,192×8	20 25	20 25	CMOS	550	110	28	0.3

Note: Package Type P: Plastic Dip; J: SOJ Package
*: Under Development

C. Non-volatile

1. EPROM

Capacity	Type No.	Organization & Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max (mW) Active	Power Dissipation Max (mW) Standby	Pins	Programming Algorithm
64K Bit	TMM2764AD-15 TMM2764AD-20	8,192×8 NMOS	150 200	150 200	5V±5%	0~70	525	158	28	I or II
	TMM2764ADI-15 TMM2764ADI-20		150 200	150 200		−40~85	630	184		
	TMM2764AD-150 TMM2764AD-200		150 200	150 200	5V±10%	0~70	660	193		
128K Bit	TMM27128AD-15 TMM27128AD-20	16,384×8 NMOS	150 200	150 200	5V±5%	0~70	525	158	28	I or II
	TMM27128ADI-15 TMM27128ADI-20		150 200	150 200		−40~85	630	184		
	TMM27128AD-150 TMM27128AD-200		150 200	150 200	5V±10%	0~70	660	193		
256K Bit	TMM27256AD-15 TMM27256AD-20	32,768×8 NMOS	150 200	150 200	5V±5%	0~70	525	158	28	I or II
	TMM27256ADI-15 TMM27256ADI-20		150 200	150 200		−40~85	630	184		
	TMM27256AD-150 TMM27256AD-200		150 200	150 200	5V±10%	0~70	660	193		
	TMM27256BD-15 TMM27256BD-20		150 200	150 200	5V±5%	0~70	525	158		
	TMM27256BDI-15 TMM27256BDI-20		150 200	150 200		−40~85	630	184		
	TC57256AD-15 TC57256AD-20	32,768×8 CMOS	150 200	150 200		0~70	158	0.525		
512K Bit	TMM27512D-20 TMM27512D-25	65,536×8 NMOS	200 250	200 250	5V±5%	0~70	630	184	28	I or II
	TMM27512DI-20 TMM27512DI-25		200 250	200 250		−40~85	683	210		
	TMM27512D-200 TMM27512D-250		200 250	200 250	5V±10%	0~70	715	220		
	* TMM27512AD-20 * TMM27512AD-25		200 250	200 250	5V±5%	0~70	630	184		
	* TMM27512ADI-20 * TMM27512ADI-25		200 250	200 250		−40~85	683	210		
1M Bit	TC571000D-20 TC571000D-25	131,072×8 CMOS	200 250	200 250	5V±5%	−40~85	158	0.525	32	II
	TC571001D-20 TC571001D-25		200 250	200 250						
	* TC571024D-20 * TC571024D-25	65,536×16 CMOS	200 250	200 250					40	

Note: Package D: Cerdip; * : New Product

2. Flash EEPROM

Capacity	Part No.	Organization & Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max (mW)		Pins	Programming & Erase Voltage
							Active	Standby		
256K Bit	* TMM28257P-30 * TMM28257P-25 * TMM28257P-20	32K×8 NMOS	300 250 200	300 250 200	5V±5%	0~70	525	132	28	21V ±0.25V
	**TC58257AP-25 **TC58257AP-20 **TC58257AP-17	32K×8 CMOS	250 200 170	250 200 170	5V±5%	0~70	TBD	TBD	28	12.5V ±0.25V

3. One Time PROM

Capacity	Type No.	Organization & Process	Access Time Max. (ns)	Cycle Time Min. (ns)	Power Supply (V)	Temperature Range (°C)	Power Dissipation Max (mW)		Pins	Programming Algorithm
							Active	Standby		
64K Bit	TMM2464AP/AF	8,192×8 NMOS	200	200	5V±5%	0~70	525	158	28	I or II
128K Bit	TMM24128AP/AF	16,384×8 NMOS	200	200	5V±5%	0~70	525	158	28	I or II
256K Bit	TMM24256AP/AF	32,768×8 NMOS	200	200	5V±5%	0~70	525	158	28	I or II
	* TMM24256BP/BF-20 * TMM24256BP/BF-17		200 170	200 170						
	TC54256AP/AF	32,768×8 CMOS	200	200		−40~85	158	0.525		
512K Bit	TMM24512P/F	65,536×8 NMOS	250	250	5V±5%	0~70	630	184	28	I or II
	* TMM24512AP/AF-25 * TMM24512AP/AF-20		250 200	250 200						
	* TC54512AP/AF-20 * TC54512AP/AF-17		200 170	200 170		−40~85	158	0.525		
1M Bit	* TC541000P/F-25 * TC541000P/F-20	131,072×8 CMOS	250 200	250 200	5V±5%	−40~85	158	0.525	32	II
	* TC541001P/F-25 * TC541001P/F-20		250 200	250 200						
	* TC541024P-25 * TC541024P-20	65,536×16 CMOS	250 200	250 200					40	

4. Mask ROM

Capacity	Type No.	Organization	Access Time Max. (ns)	Cycle Time Min. (ns)	Process	Power Dissipation Max. (mW)		Pins
						Active	Standby	
256K Bit	TC53257P/F	32,766×8	150	150	CMOS	138	0.11	28
512K Bit	TC53512AP/AF	65,536×8	150	150	CMOS	138	0.11	28
1M Bit	TC531000AP/AF	131,072×8	150	150	CMOS	138	0.11	28
	TC531001AP		150	150				
	TC531024P	65,536×16	150	150				40
4M Bit	* TC534000P	524,288×8	250	250	CMOS	220	0.11	32

Note: Package Type P: Plastic Dip; F: Flat Package (SOP)

*: New Product
**: Under Development

PRODUCT LINE CROSS REFERENCE

1. 256K Bit Dynamic RAM

Organization	256K×1 (page mode)	256K×1 (nibble mode)	64K×4 (page mode)
TOSHIBA	TMM41256AP/AT/AZ	TMM41257AP/AT/AZ	TMM41464AP/AT/AZ
FUJITSU	MB81256	MB81257	MB81464
HITACHI	HM50256	HM50257	HM50464
MITSUBISHI	M5M4256	M5M4257	M5M4464
NEC	μPD41256	μPD41257	μPD41464
OKI	MSM41256	MSM41257	MSM41464
TI	TMS4256	TMS4257	TMS4464
NMB	AAA2801		

2. 1M×1 CMOS Dynamic RAM

Organization	1MB×1 (Fast page mode)	1MB×1 (Nibble mode)	1MB×1 (Static column mode)
SUPPLIER	PART#	PART#	PART#
TOSHIBA	TC511000	TC511001	TC511002
FUJITSU	MB81C1000	MB81C1001	MB81C1002
HITACHI	HM511000	HM511001	HM511002
MITSUBISHI	M5M4C1000	M5M4C1001	M5M4C1002
NEC	μPD421000	μPD421001	μPD421002
TI	TMS4C1024	TMS4C1025	TMS4C1027
NMB	AAA1M100	AAA1M101	AAA1M102
SAMSUNG	KM41C1000	KM41C1001	KM41C1002
OKI	MSM511000	MSM511001	MSM511002
MOTOROLA	MCM511000	MCM511001	MCM511002

3. 256K×4 CMOS Dynamic RAM

Organization	256K×4 (Fast page mode)	256K×4 (Static column mode)	256K×4 (Fast page, WPB)	256K×4 (Static column, WPB)
SUPPLIER	PART#	PART#	PART#	PART#
TOSHIBA	TC514256	TC514258	TC514266A	TC514268A
FUJITSU	MB81C4256	—		
HITACHI	HM514256	HM514258		
MITSUBISHI	M5M44C256	M5M44C258		
NEC	μPD424256	μPD424258		
TI	TMS44C256	TMS44C257		
SHARP	LH64257	LH64256		
NMB	AAA1M104	AAA1M105		
OKI	MSM514256	MSM514258		
MOTOROLA	MCM514256	MCM514258		

4. 256K×4 CMOS Video RAM

Organization	256K×4 (w/O Raster)	256K×4 (w/Raster)	256K×4 (Field Memory)
SUPPLIER	PART#	PART#	PART#
TOSHIBA	TC524256	TC524257	TC521000
FUJITSU	MB81C4251	(MB81C4252)	
MITSUBISHI	M5M442256		
HITACHI	HM534251	HM534252	
TI	TMS44C251		
NEC	μPD42274		

PRODUCT LINE CROSS REFERENCE (continued)

5. DRAM Hybrid Module

Organization	1M×4	4M×1	512K×8	1M×8
TOSHIBA	THM41000	THM14000	THM8512/4	THM81000/1/2
HITACHI				HB56A18
MITSUBISHI				MH1M08
OKI				MSC2311YS8/KS8

Organization	1M×8 (Low profile)	1M×9	1M×9 (Common I/O)	1M×9 (Low profile)	256K×36
TOSHIBA	THM81020/1/2	THM91000/1/2	THM91010/1/2	THM91020/1/2	THM362500
HITACHI		HB56A19			
MITSUBISHI		MH1M09J			
OKI		MSC2310YS9/KS9			

6. High-Speed Static RAM

1) NMOS

Organization	2K×8	4K×4	8K×8	8K×9
Package Width	0.3 inch			
TOSHIBA	TMM2018AP	TMM2068AP	TMM2088P	TMM2089
FUJITSU		MB8168	MB81C78	MB81C79
HITACHI		HM6168		
INMOS		IMS1420/1421		
MITSUBISHI		M5M2168	M5M5178	M5M5179
MOTOROLA	MCM2016H/18	MCM6168	MCM6164	
NEC		μPD4314C		
AMD	AM9128	AM2168		

2) CMOS

Organization	64K×1	16K×4 (w/O $\overline{OE}$)	16K×4 (w/$\overline{OE}$)	8K×8	8K×9
Package Width	0.3 inch				
TOSHIBA	TC5561/2	TC55416	TC55417	TC5588	TC5589
CYPRESS	CY7C187	CY7C164	CY7C166	CY7C185	CY71C186
FUJITSU	MB81C71A	MB81C74		MB81C78	MB81C79
HITACHI	HM6287	HM6288			
IDT	IDT7187	IDT7188	IDT7198	IDT7164	
INMOS	IMS1600/1	IMS1620	IMS1624	IMS51630	
MITSUBISHI	M5M5187	M5M5188		M5M5178	M5M5179
MOTOROLA	MCM6287	MCM6288/9	MCM6290	MCM6164	
NEC	μPD4361	μPD4362	μPD4363		
OKI		MSM5188US			
SARATOGA	SSM7187	SSM7188	SSM7166	SSM7164	SSM7169
PERFORMANCE	P4C187	P4C188			

PRODUCT LINE CROSS REFERENCE (continued)

7. Standard Static RAM

Organization	8K×8					32K×8		128K×8
NMOS/CMOS	NMOS	CMOS						
Package Width	0.3 inch	0.6 inch				0.6 inch/0.45 inch		
TOSHIBA	TMM2063P/AP	TMM2064P/AP	TC5564AP/AF/L	TC5565APL/AFL	TC5563APL	TC55257AP/AF	TC55256PL/FL	TC551001P/F
FUJITSU		MB8464		MB8464		MB84256		
HITACHI	HM6264AS	HM6264		HM6264	HM6264ASP	HM62256		
MITSUBISHI			M5M5164	M5M5165		M5M5256		
NEC			μPD4464	μPD4364		μPD43256	μPD44256	
OKI		MSM5165	MSM5164	MSM5165				
IDT				IDT7164				

8 Pseudo Static RAM

Organization	32K×8	128K×8	
TYPE	PSRAM	VS/PSRAM	PSRAM
NMOS/CMOS	CMOS	CMOS	CMOS
Package Width	0.6 inch/0.3 inch/.45 inch	0.6 inch/0.45 inch	0.6 inch/0.3 inch/0.45 inch
TOSHIBA	TC51832P/PL/SP/SPL/F/FL	TC518128P/F	TC518128AP/APL/ASP/ASPL/AF/AFL
HITACHI	HM65256		HM658128
NEC	μPD42832		
SHARP	LH62258		

9. 64K/128K Bit NMOS EPROM/OTP

Organization	8K×8		16K×8	
EPROM/OTP	EPROM	OTP	EPROM	OTP
Pins	28	28	28	28
TOSHIBA	TMM2764AD	TMM2464AP/AF	TMM27128AD	TMM24128AP/AF
AMD	Am2764A		Am27128AD	
FUJITSU	MBM2764		MBM27128A	
HITACHI	HN482764	HN482764	HM4827128G	HN4827128
INTEL	i2764A	P2764A	i27128A	P27128A
MITSUBISHI	M5L2764K	M5M2764P	M5L27128K	M5M27128P
NEC	μPD2764	μPD2764C	μPD27128	μPD27128C
OKI	MSM2764		MSM27218	
TI	TMS2764			

PRODUCT LINE CROSS REFERENCE (continued)

10. 256K/512K/1M BIT EPROM/OTP

Organization	32K×8				64K×8		128K×8		64K×16
EPROM/OTP	EPROM		OTP		EPROM	OTP	EPROM		EPROM
NMOS/CMOS	NMOS	CMOS	NMOS	CMOS	NMOS		CMOS		CMOS
TOSHIBA	TMM27256AD TMM27256BD	TC57256AD	TMM24256AP/AF TMM24256BP/BF	TC54256AP/AF	TMM27512D TMM27512AD	TMM24512AP/AF	TC571000D	TC571001D	TC571024D
AMD	Am27256	AM27C256			Am27512				AM27C1024
FUJITSU	MBM27256	MBM27C256			—	—	MBM27C1000	MBM27C1001	MBM27C1028
HITACHI	HN27256G	HN27C256G	HN4827256P		HN27512G		HN27C101	HN27C301	HN27C1024AG
INTEL	i27256	i27C256	P27256A	P27C256	i27512	P27512	27010	—	27210
MITSUBISHI	M5L27256K	M5M27C256	M5M27256P	M5M27C256P	M5L27512	M5M27512P	M5M27C100	M5M27C101	M5M27C102
NEC	μPD27256	μPD27C256A	μPD27256C	μPD27256C		—	μPD27C100	μPD27C101	μPD27C1024
OKI	MSM27C256	MSM27C256			MSM27512		MSM271000		MSM271024
NSC	—	NMC27C256	—		NMC27C512		NMC27C1023		NMC27C1024
TI	—	TMS27C256			TMS27C512				

11. 256K/1M Bit/2M Bit/4M Bit CMOS MROM

Organization	32K×8	64K×8	128K×8	512K×8
TOSHIBA	TC53257P/F	TC53512AP/AF	TC531000AP/AF	TC534000P
TI	TMS47C256		TMS47C1024	
FUJITSU	MB83256	MB83512	MB831124	
HITACHI	HN613256P		HN62301	
MOTOROLA	MCM65256A			
MITSUBISHI	—	μPD23C512	M5M23C100	M5M23C400
NEC	μPD23C256		μPD23C1000	
OKI	MSM53256	RO9512XES	MSM531000	
GI	ROC256D		R09100XD	

MEMORY SELECTION GUIDE (1) — ACCESS TIME VS. CAPACITY

*Preliminary

	16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	4M Bit
250						TMM27512-25 TMM27512A-25 TMM24512 TMM24512A-25	TC571000/1-25 TC571024-25 TC541000/1-25	TC534000
200		TC5564A-20 TMM2764A-20 TMM2764A-200 TMM2464A		TMM27128A-20	TC57256A-20 TMM27256A-20 TMM27256B-20 TC57256-20 TMM24256A TMM24256B-17/20 TC54256A TC53257	TMM27512-20 TMM27512A-17/20 TMM24512A-20	TC571000/1-20 TC571024-20 TC541000/1-20	
150		TMM2063-12/15 TMM2064-12/15 TMM2063A-12 TC5563A-12/15 TC5564A-15 TC5565A-12/15 TMM2764A-15 TMM2764A-150		TMM27128A-15	TMM41256A-12/15 TMM41257A-12/15 TMM41464-12/15 TC55257A-12 TC55256-12/15 TC51832-12 TMM27256A-15 TMM27256B-15 TC57256A-12/15 TC55256-12		TC524256-12 TC524257-12 TC518128-12 TC571000/1-15 TC531000/1A	
100		TMM2063-10 TMM2064-10 TMM2063A-70/10 TC5563A-10 TC5565A-10 TC5561-55/70			TMM41256A-10 TMM41257A-10 TMM41464A-10 TC55257A-85/10 TC55256-10 TC51832-85/10		TC511000-70/80/10 TC511001-70/80/10 TC511002-70/80/10 TC514256-70/80/10 TC514266-70/80/10 TC514258-70/80/10 TC514268-70/80/10 TC524256-10 TC524257-10 TC551001-70/80/10 TC518128-10	
55	TMM2018A-25/35 TMM2068A-25/35	TMM2088-35/45 TC5588-20/25 TC5561-45 TC5562-35/45 TC55416-25/35 TC55417-25/35	TMM2089-35/45 TC5589-20/25				TC521000P	

MEMORY SELECTION GUIDE (2) — TYPE OF MEMORY VS. CAPACITY

*Preliminary

Memory	Type	Memory Capacity							
		16K Bit	64K Bit	72K Bit	128K Bit	256K Bit	512K Bit	1M Bit	4M Bit
RAM	NMOS Dynamic RAM					TMM41256AP/AT/AZ TMM41257AP/AT/AZ TMM41464AP/AT/AZ			
	CMOS Dynamic RAM							TC511000P/J/Z TC511001P/J/Z TC511002P/J/Z TC514256P/J/Z TC514258P/J/Z TC511000AP/AJ/AZ TC511001AP/AJ/AZ TC511002AP/AJ/AZ TC514256AP/AJ/AZ TC514266AP/AJ/AZ TC514258AP/AJ/AZ TC514268AP/AJ/AZ TC524256P/J/Z TC524257P/J/Z TC51D00P	
	NMOS Static RAM	TMM2018AP TMM2068AP	TMM2063P TMM2063AP TMM2064AP TMM2064P TMM2068P	TMM2089P					
	CMOS Static RAM		TC5564APL/FL TC5563APL TC5565APL/AFL TC5561P/J TC5562P/J TC55416P/J TC55417P/J TC5588P/J	TC5589P/J		TC55257AP/AF TC55256P/F TC51832P/SP/F TC51832PL/SPL/FL		TC518128P TC551001P	
ROM	NMOS EPROM		TMM2764AD/ADI		TMM27128AD/ADI	TMM27256AD/ADI TMM27256BD/BDI	TMM27512D/DI TMM27512AD/ADI		
	NMOS E²PROM					TMM28257P			
	CMOS EPROM					TC57256AD		TC571000/1D TC571024D	
	CMOS Mask ROM					TC53257P/F		TC531000/1AP/AF	TC534000P
	NMOS OTP		TMM2464AP/AF		TMM24128AP/AF	TMM24256AP/AF TMM24256BP/BF	TMM24512P/F TMM24512AP/AF		
	CMOS OTP					TC54256AP/AF		TC541000/1-P	

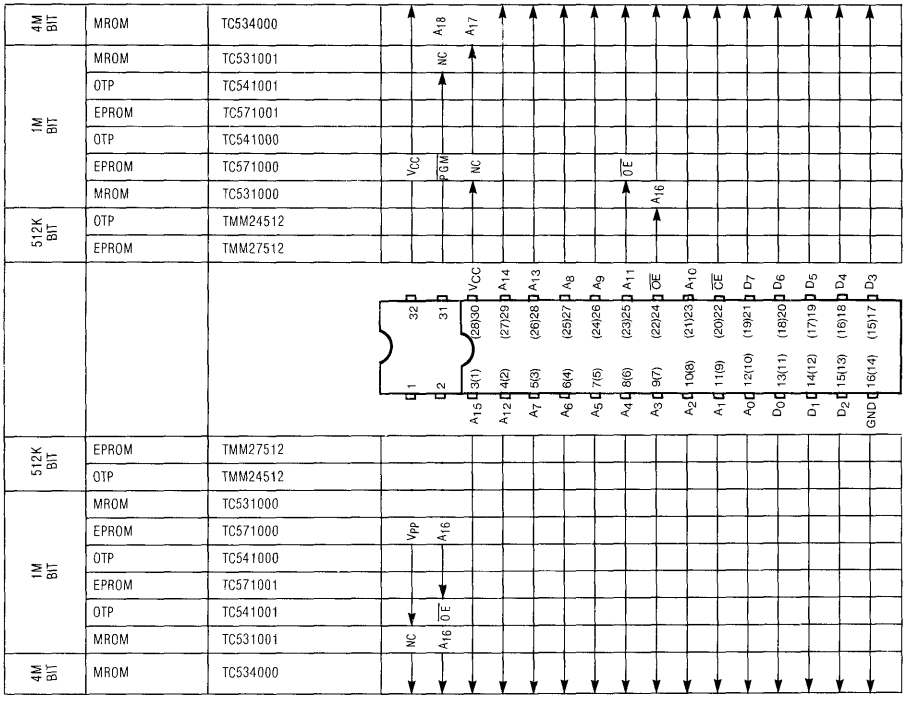
MEMORY SELECTION GUIDE (3) — WORD BY BIT

Word \ Bit	1	3	8	9
2K			TMM2018AP	
4K		TMM2068AP		
8K			TMM2063P/AP TMM2064P TC5564APL/AFL TC5563APL TC5565APL/AFL TMM2088P TC5588P/J TMM2464AP/AF TMM2764AD/ADI	TMM2089P TC5589P/J
16K		TC55416P/J TC55417P/J	TMM24128AP/AF TMM27128AD/ADI	
32K			TC55256P/F TC55257AP/AFL TC51832P/PL/SP/F TC54256AP/AF TMM24256AP/AF/BP/BF TMM27256AD/ADI/BD/BDI TC53257P/F T57256AD TMM28257P	
64K	TC5561P/J TC5562P/J	TMM41464AP	TMM24512P/F/AP/AF TMM27512D/DI/AD/ADI	
128K			TC518128P TC551001P TC571000/ID TC541000/1P TC571024D TC531000AP TC531001AP/AF	
256K	TMM41256AP/AT/AZ TMM41257AP/AT/AZ	TC514256P/J/Z/AP/AJ/AZ TC514258P/J/Z/AP/AJ/AZ TC514266AP/AJ/AZ TC515268AP/AJ/AZ TC524256P/J/Z TC524257P/J/Z TC521000P		
512K			TC534000P	
1M	TC511000P/J/Z TC511001P/J/Z TC511002P/J/Z TC511000AP/AJ/AZ TC511001AP/AJ/AZ TC511002AP/AJ/AZ			

MEMORY SELECTION GUIDE (4) — HIGH DENSITY PACKAGE

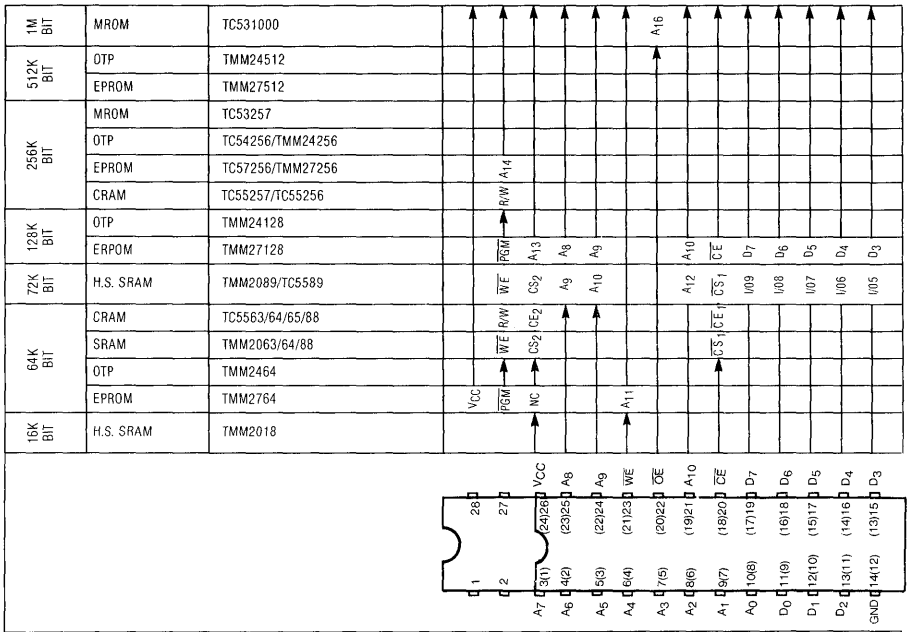
PACKAGE		PLCC	SOJ				ZIP			SOG
PIN		18	24	26/20	28	32	16	20/19	28	28
Dynamic RAM	256K	TMM41256AT TMM41257AT TMM41464AT			TMM41256AZ TMM41257AZ TMM41464AZ					
	1M			TC511000J/AJ TC511001J/AJ TC511002J/AJ TC514256J/AJ TC514258J/AJ TC514266AJ TC514268AJ				TC511000Z/AZ TC511001Z/AZ TC511002Z/AZ TC514256Z/AZ TC514258Z/AZ TC514266AZ TC514268AZ		
Static RAM	64K		TC5561J TC5562J TC55416J TC55417J		TC5588J					TC5564AFL TC5565AFL
	72K				TC5589J					
	256K									TC55256FL TC55257AFL
Mask ROM	256K									TC53257F
	1M									TC531000AF
OTP	64K									TMM2464AF
	128K									TMM24128AF
	256K									TMM24256AF/BF TC54256AF
	512K									TMM24512F/AF
DRAM	1M					TC524256J TC524257J			TC524256Z TC524257Z	

TOSHIBA BYTE-WISE MEMORY PIN OUT FOR 28/32 PIN DEVICES

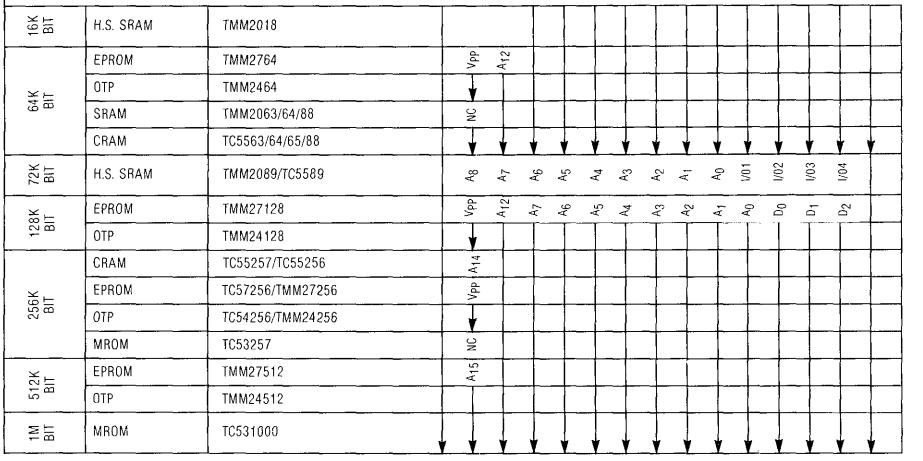


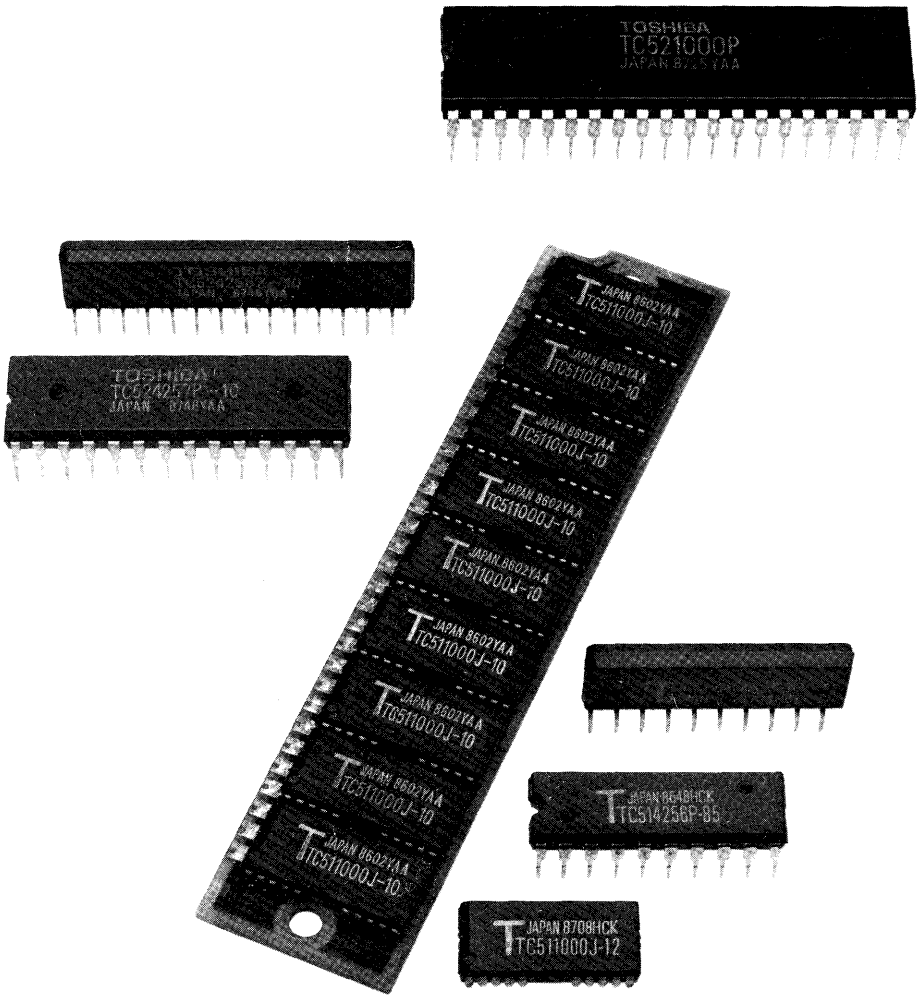
TOSHIBA BYTE-WIDE MEMORY PIN OUT FOR 24/28 PIN DEVICES

1M BIT	MROM	TC531000
512K BIT	OTP	TMM24512
	EPROM	TMM27512
256K BIT	MROM	TC53257
	OTP	TC54256/TMM24256
	EPROM	TC57256/TMM27256
	CRAM	TC55257/TC55256
128K BIT	OTP	TMM24128
	EPROM	TMM27128
72K BIT	H.S. SRAM	TMM2089/TC5589
64K BIT	CRAM	TC5563/64/65/88
	SRAM	TMM2063/64/88
	OTP	TMM2464
	EPROM	TMM2764
16K BIT	H.S. SRAM	TMM2018



16K BIT	H.S. SRAM	TMM2018
64K BIT	EPROM	TMM2764
	OTP	TMM2464
	SRAM	TMM2063/64/88
	CRAM	TC5563/64/65/88
72K BIT	H.S. SRAM	TMM2089/TC5589
128K BIT	EPROM	TMM27128
	OTP	TMM24128
256K BIT	CRAM	TC55257/TC55256
	EPROM	TC57256/TMM27256
	OTP	TC54256/TMM24256
	MROM	TC53257
512K BIT	EPROM	TMM27512
	OTP	TMM24512
1M BIT	MROM	TC531000





Dynamic RAMs

Standard DRAM

TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD×1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41256AP/AT/AZ-10, TMM41256AP/AT/AZ-12
TMM41256AP/AT/AZ-15

DESCRIPTION

The TMM41256AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41256AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41256AP/AT/AZ high speed operation.

Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode and a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh are available. Another special feature of TMM41256AP/AT/AZ is page mode, allowing the user to access at a high data rate.

FEATURES

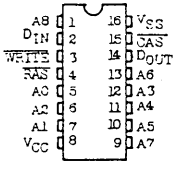
- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41256AP/AT/AZ-10/-12/-15
$\overline{RAS}$ Access Time	100ns/120ns/150ns
$\overline{CAS}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns

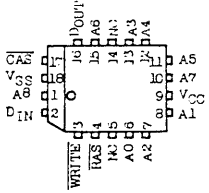
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power:
  440mW MAX. Operating (TMM41256AP/AT/AZ-10)
  396mW MAX. Operating (TMM41256AP/AT/AZ-12)
  358mW MAX. Operating (TMM41256AP/AT/AZ-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Page Mode capability
- All inputs and output TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41256AP
  Plastic Leaded Chip Carrier: TMM41256AT
  Plastic ZIP : TMM41256AZ

PIN CONNECTION (TOP VIEW)

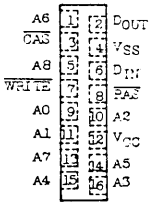
TMM41256AP



TMM41256AT



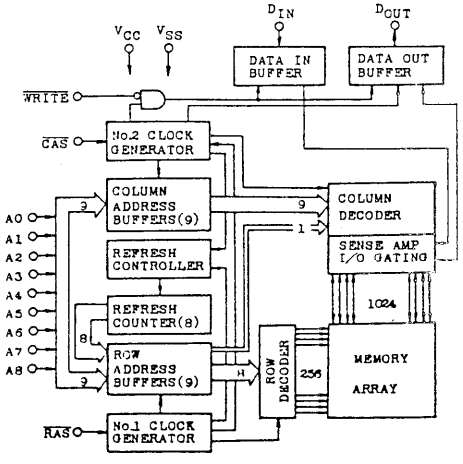
TMM41256AZ



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	
Operating Temperature	T_{OPR}	0 ~ 70	°C	
Storage Temperature	T_{STG}	−55 ~ 150	°C	
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	
Power Dissipation	P_D	600	mW	
Short Circuit Output Current	I_{OUT}	50	mA	

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC}MIN.)	TMM41256AP/AT/AZ-10	–	80	mA	3, 4
		TMM41256AP/AT/AZ-12	–	72	mA	
		TMM41256AP/AT/AZ-15	–	65	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC}MIN.)	TMM41256AP/AT/AZ-10	–	70	mA	3
		TMM41256AP/AT/AZ-12	–	62	mA	
		TMM41256AP/AT/AZ-15	–	55	mA	
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)	TMM41256AP/AT/AZ-10	–	60	mA	3, 4
		TMM41256AP/AT/AZ-12	–	55	mA	
		TMM41256AP/AT/AZ-15	–	50	mA	
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC} = t_{RC}MIN.)	TMM41256AP/AT/AZ-10	–	70	mA	3
		TMM41256AP/AT/AZ-12	–	62	mA	
		TMM41256AP/AT/AZ-15	–	55	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, ALL Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ + 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}= 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM41256AP/AT/AZ-10		TMM41256AP/AT/AZ-12		TMM41256AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	–	220	–	260	–	ns	
t_{RWC}	Read-Write Cycle Time	200	–	240	–	285	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	–	260	–	310	–	ns	
t_{PC}	Page Mode Cycle Time	100	–	120	–	145	–	ns	
t_{PRWC}	Page Mode Read-Write Cycle Time	110	–	140	–	170	–	ns	
t_{PRMW}	Page Mode Read-Modify Write Cycle Time	130	–	160	–	195	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	100	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	50	–	60	–	75	ns	9, 10
t_{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	–	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	–	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	20	–	25	–	ns	
t_{CP}	Page Mode $\overline{CAS}$ Precharge Time	40	–	50	–	60	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	25	–	30	–	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	–	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	20	–	25	–	30	–	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{WP}	Write Command Pulse Width	20	–	25	–	30	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	20	–	25	–	30	–	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41256AP/AT/AZ-10		TMM41256AP/AT/AZ-12		TMM41256AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	–	40	–	50	–	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	–	100	–	125	–	ns	15
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	–	50	–	60	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

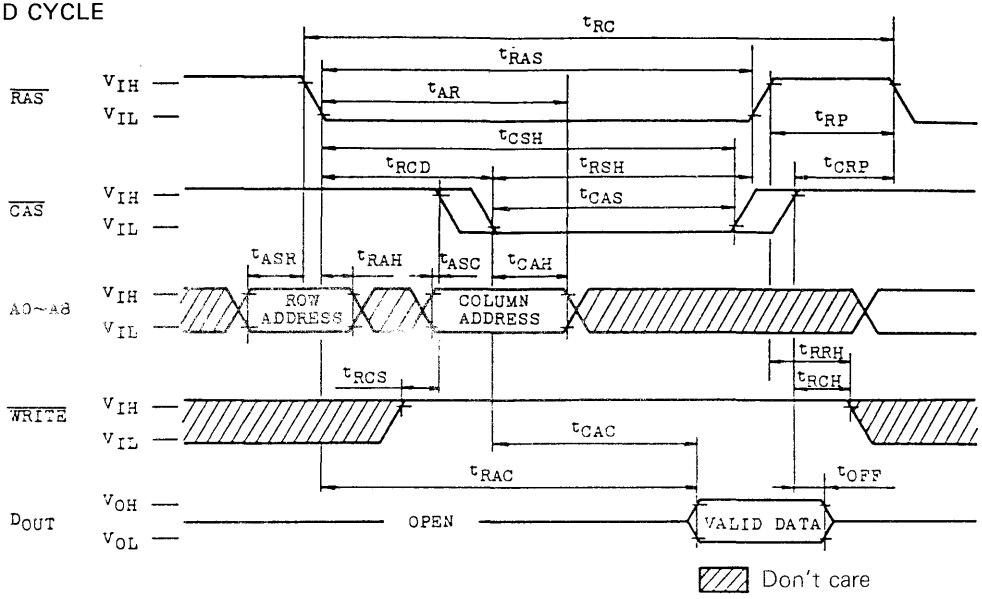
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

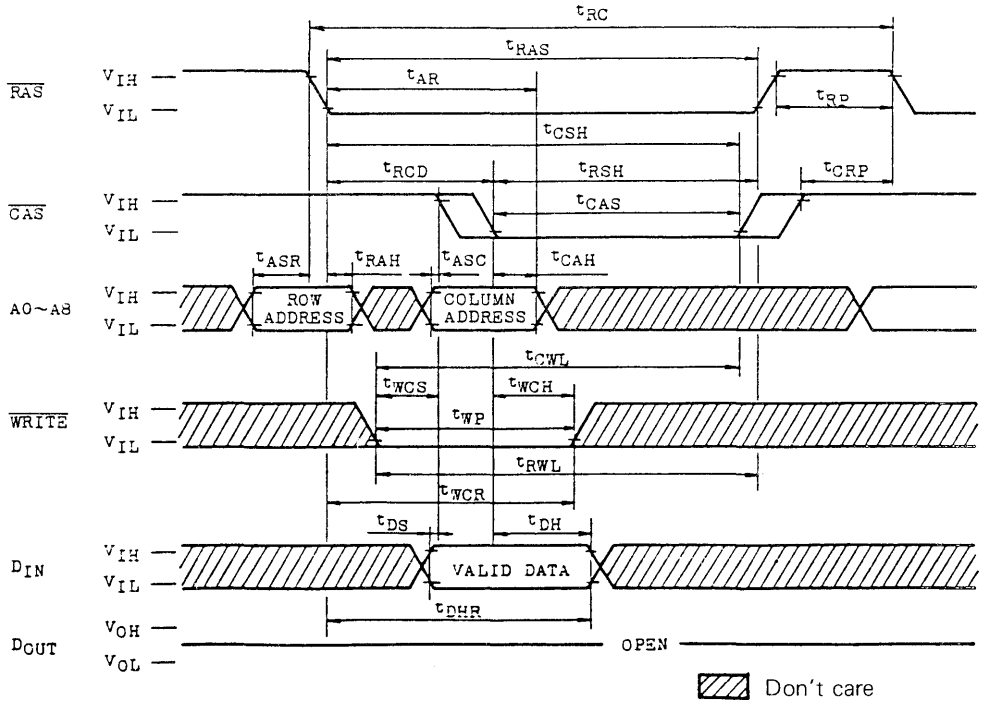
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assume that $t_{RCD} \geq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain dataread from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

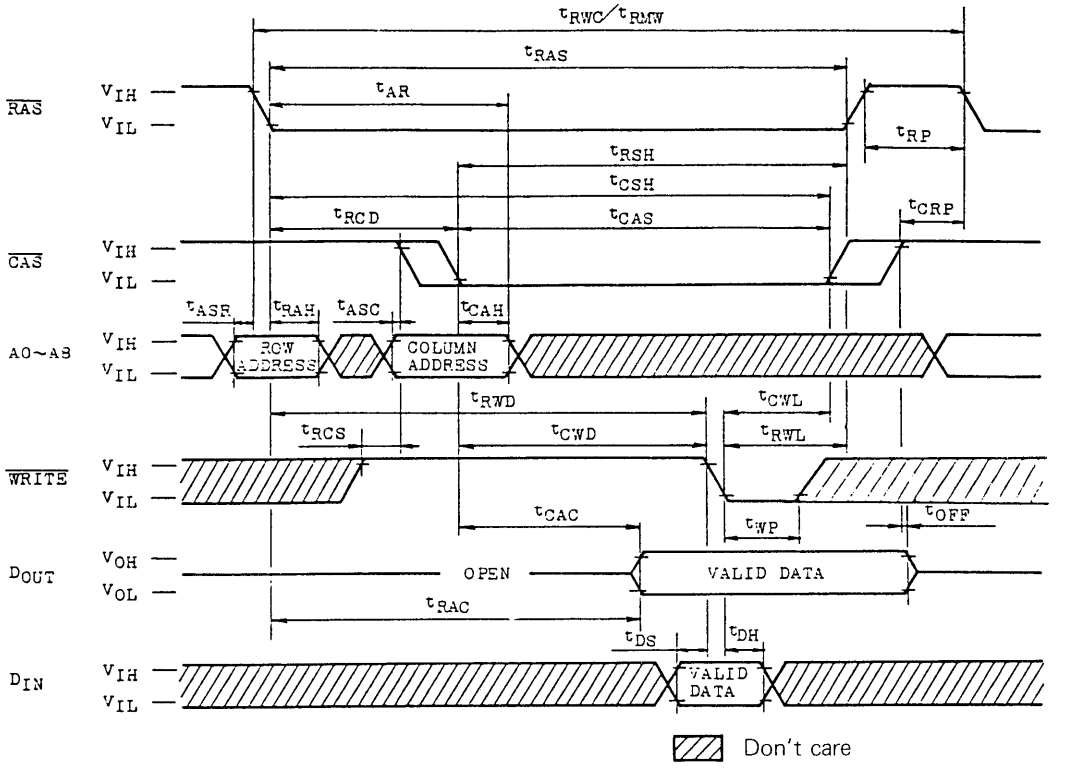
- READ CYCLE



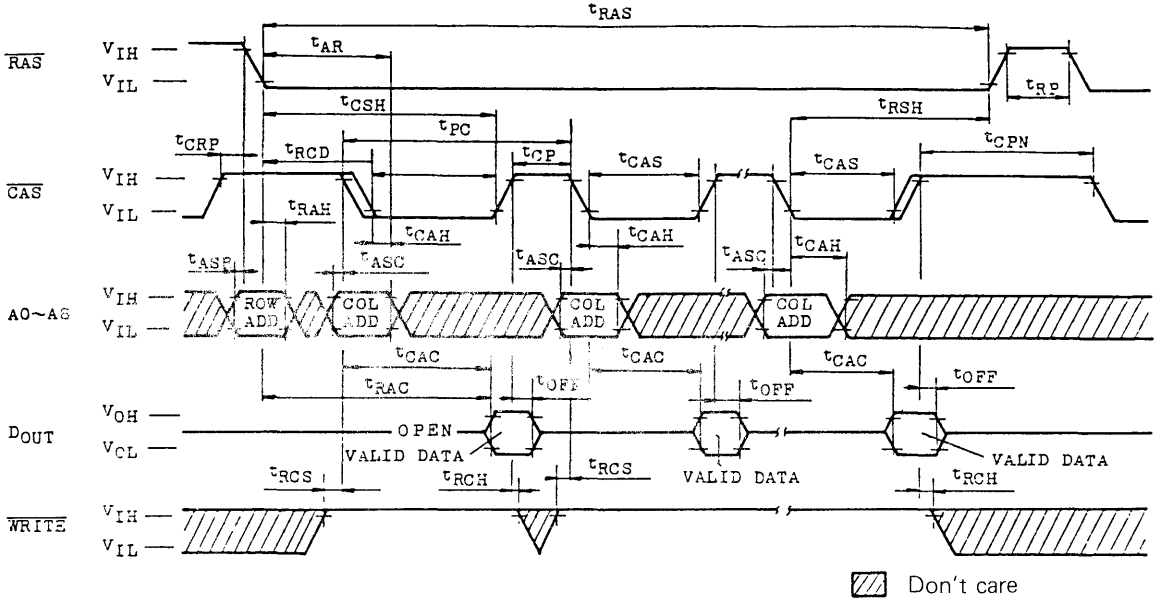
- WRITE CYCLE (EARLY WRITE)



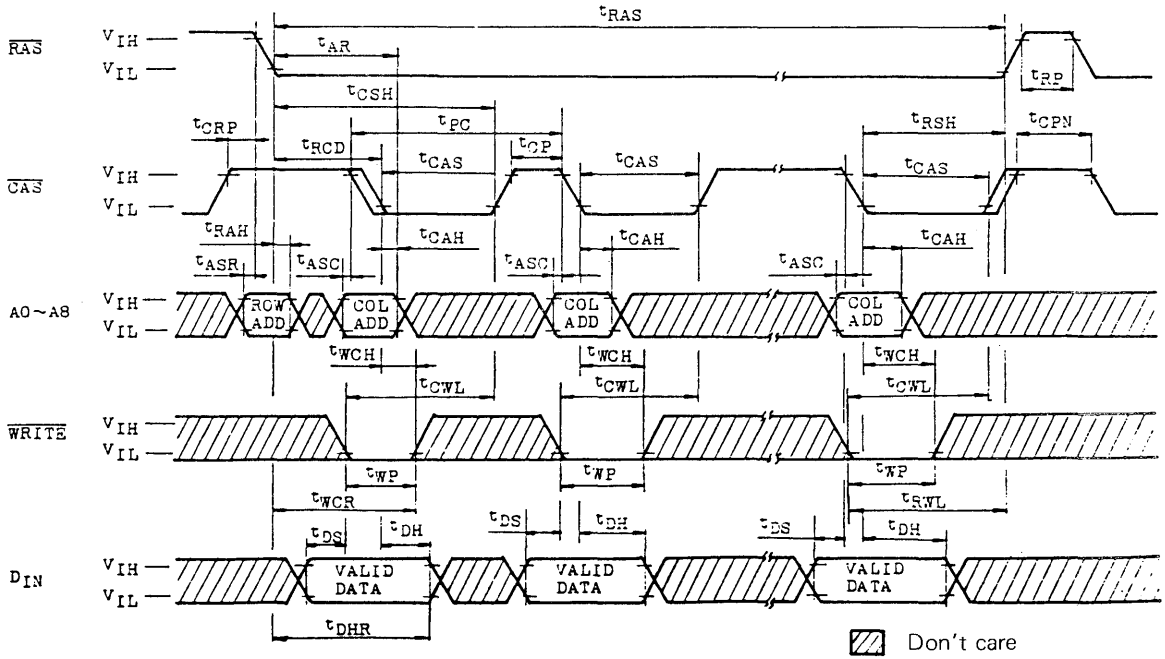
- READ-WRITE/READ-MODIFY-WRITE CYCLE



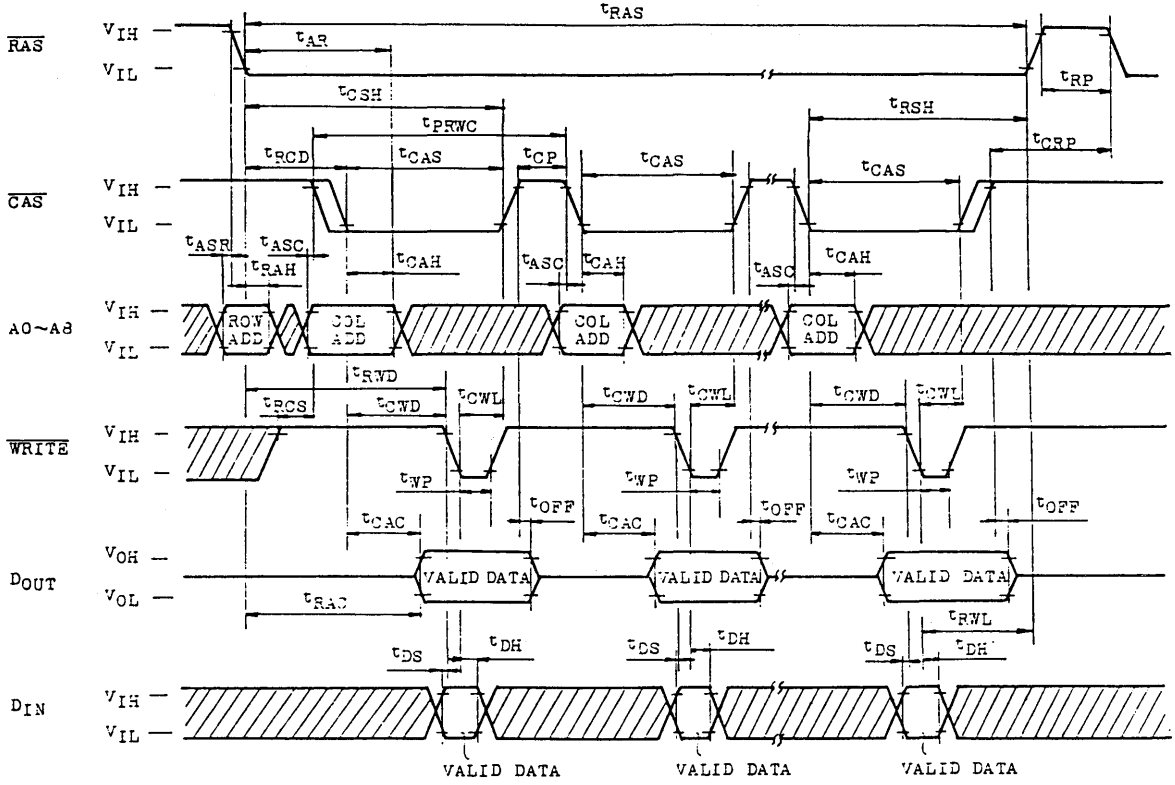
- PAGE MODE READ CYCLE



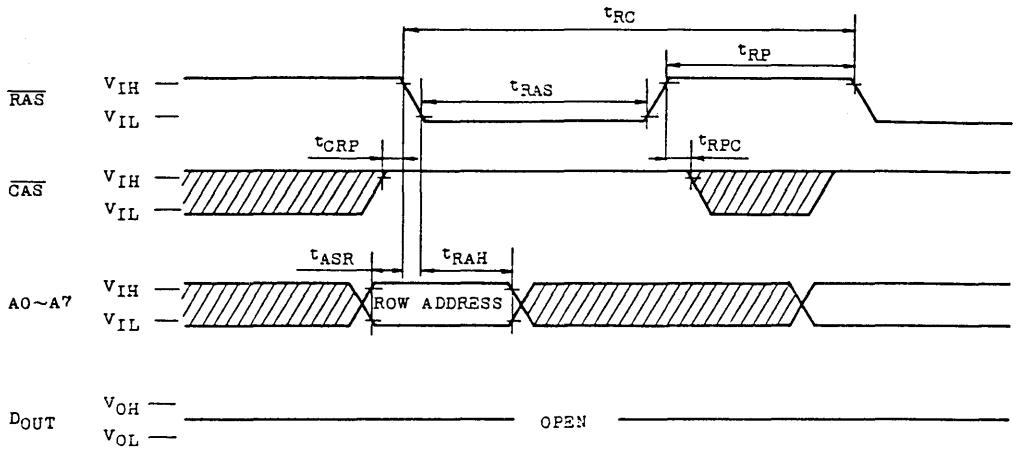
- PAGE MODE WRITE CYCLE (EARLY WRITE)



- PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



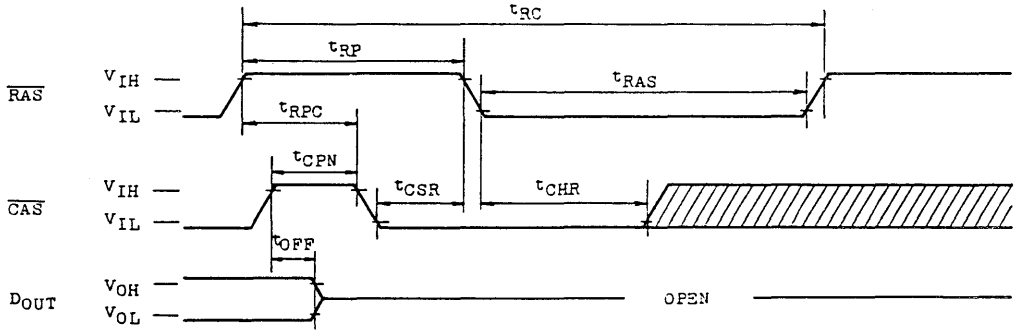
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$ = Don't care, A8 = Don't care

Don't care

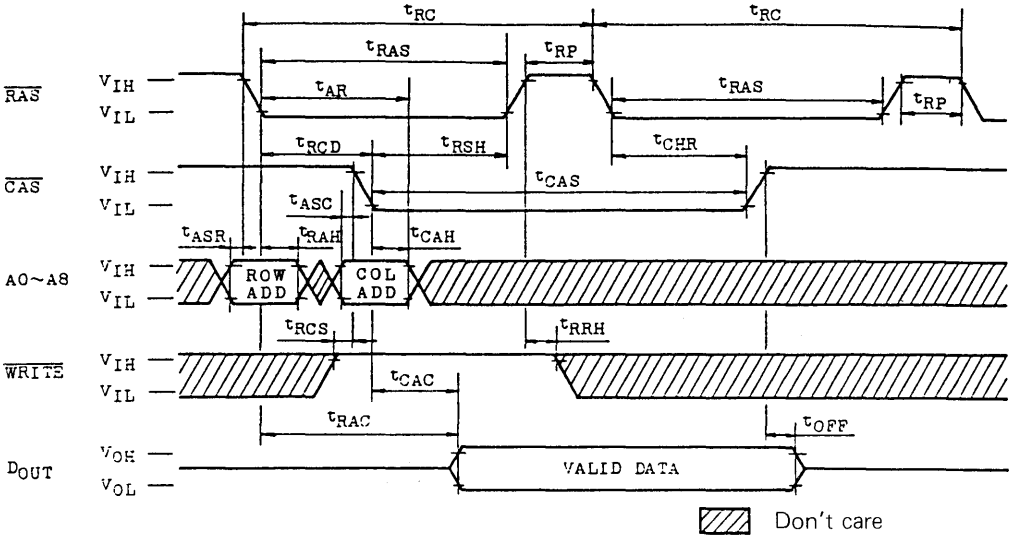
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



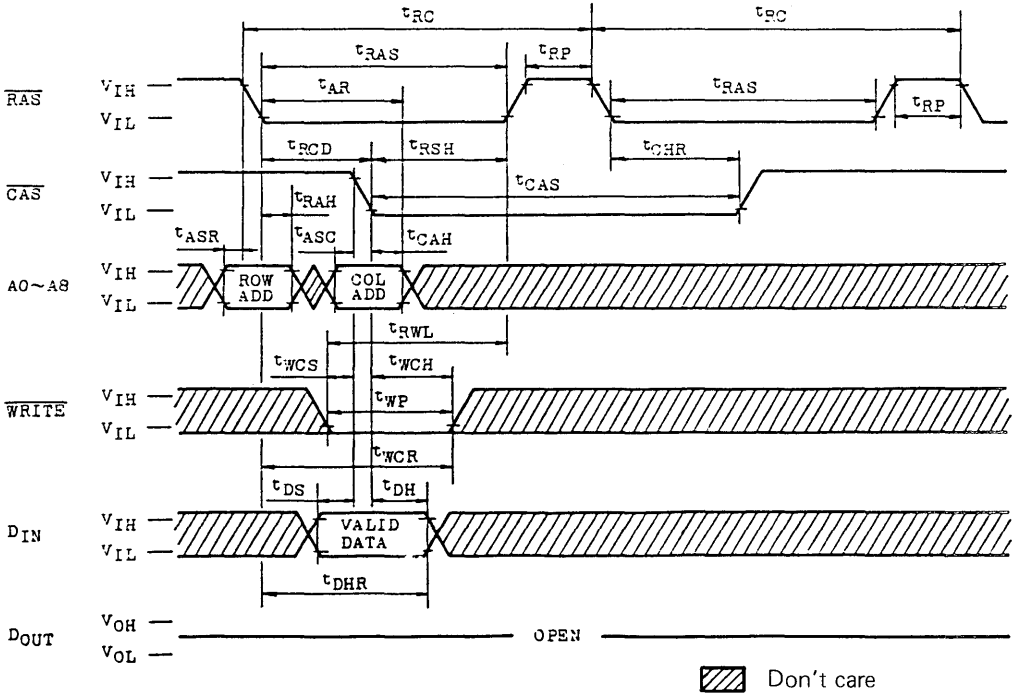
NOTE: $\overline{WRITE}$ = Don't care, A0 ~ A8 = Don't care

Don't care

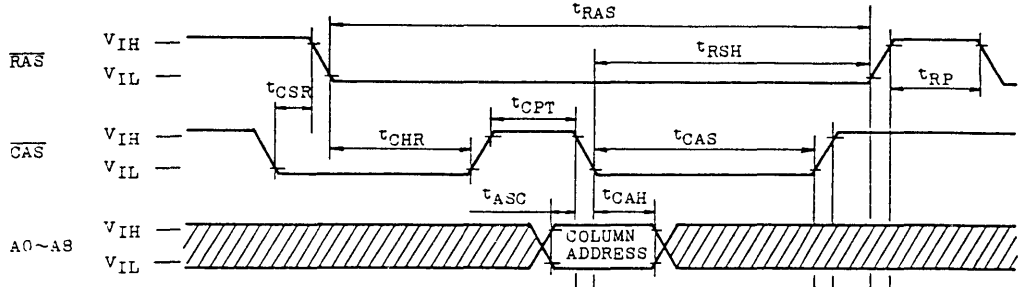
- HIDDEN REFRESH CYCLE (READ)



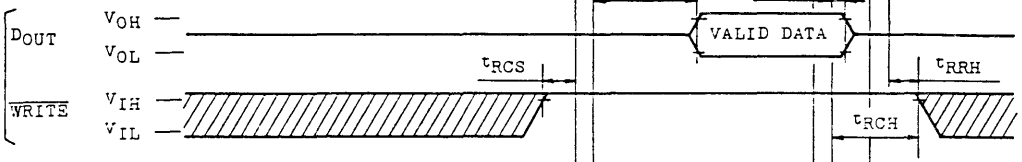
- HIDDEN REFRESH CYCLE (WRITE)



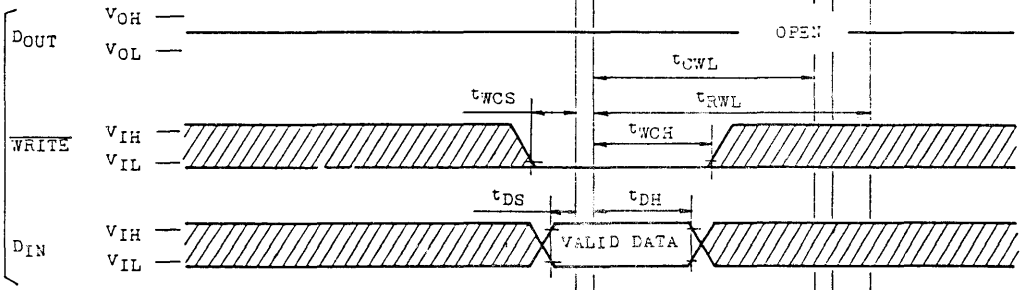
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



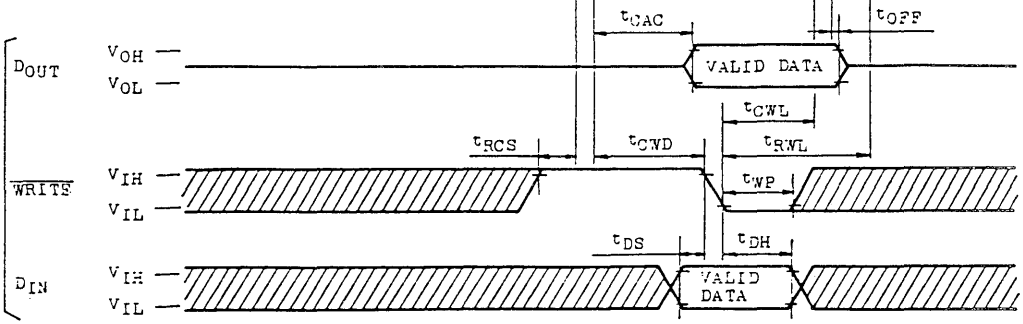
- READ CYCLE



- WRITE CYCLE



- READ-WRITE/READ-MODIFY-WRITE CYCLE



Don't care

APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41256AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41256AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid form access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

PAGE MODE

The "Page-Mode" feature of the TMM41256AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address (A0 ~ A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

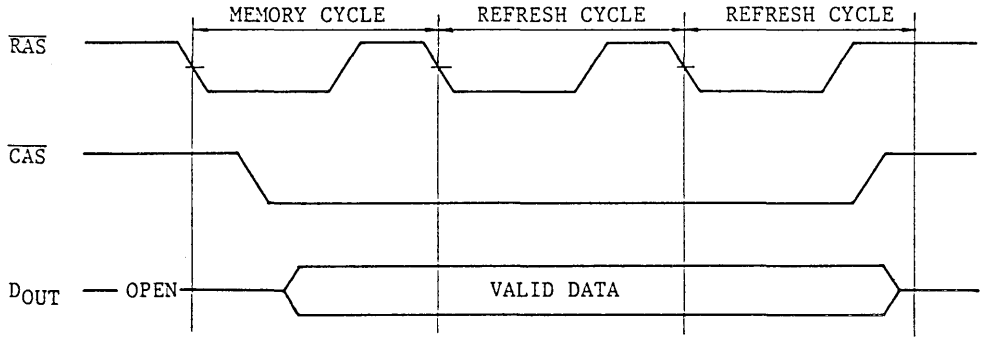
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41256AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed,

the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41256AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41256AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 256 times.

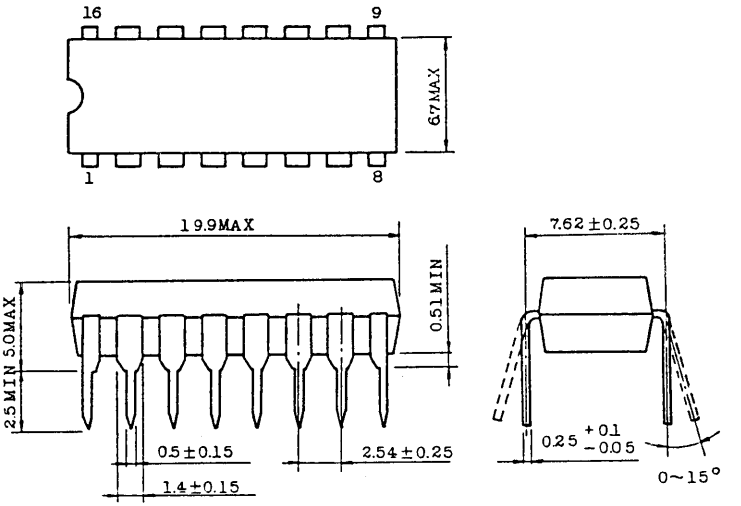
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

- Plastic DIP

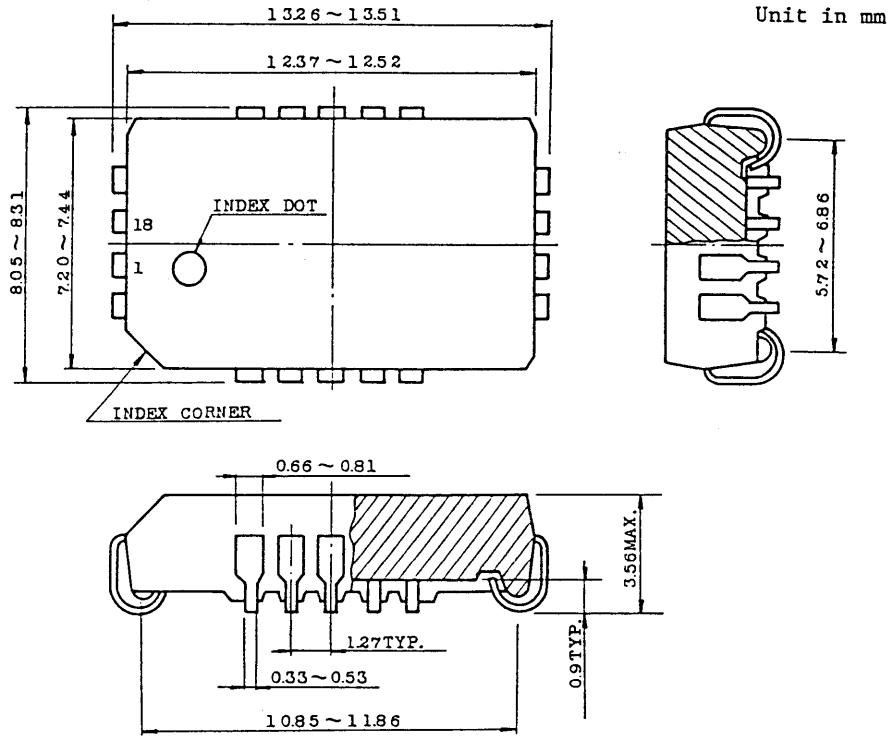
Unit in mm



NOTE: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

- Plastic LCC

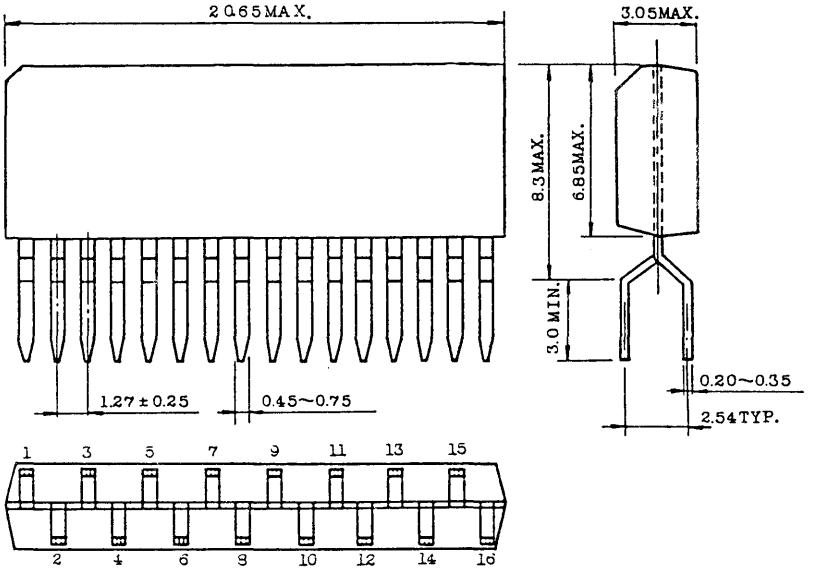
Unit in mm



NOTE: Each lead pitch is 1.27mm. All dimensions are in millimeters.

- Plastic ZIP

Unit in mm



NOTE: Each lead pitch is 1.27mm. All dimensions are in millimeters.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD×1 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41257AP/AT/AZ-10, TMM41257AP/AT/AZ-12 TMM41257AP/AT/AZ-15

DESCRIPTION

The TMM41257AP/AT/AZ is the N-channel dynamic RAM organized 262,144 words by 1 bit. Multiplexed address inputs permit the TMM41257AP/AT/AZ to be packaged in a standard 16 pin plastic DIP, 18 pin PLCC and 16 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. The double layered MOS technology with polycide and poly Si permits the TMM41257AP/AT/AZ high speed operation.

Also, the advanced circuit techniques have realized low power dissipation. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capacibility with high performance logic families such as schottky TTL. In addition to the $\overline{RAS}$ only refresh mode, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is available. Another special feature of TMM41257AP/AT/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

- 262,144 words by 1 bit organization
- Fast access time and cycle time

	TMM41257AP/AT/AZ-10/-12/-15
$\overline{RAS}$ Access Time	100ns/120ns/150ns
$\overline{CAS}$ Access Time	50ns/ 60ns/ 75ns
Cycle Time	190ns/220ns/260ns
Nibble Mode Access Time	25ns/ 30ns/ 40ns
Nibble Mode Cycle Time	50ns/ 60ns/ 70ns

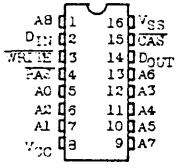
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power:
  440mW MAX. Operating (TMM41257AP/AT/AZ-10)
  396mW MAX. Operating (TMM41257AP/AT/AZ-12)
  358mW MAX. Operating (TMM41257AP/AT/AZ-15)
  28mW MAX. Standby

Output unlatched at cycle end allows two-dimensional chip selection
Common I/O capability using "EARLY WRITE" operation
Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Nibble Mode capability
All inputs and output TTL compatible
256 refresh cycles/4ms
Package

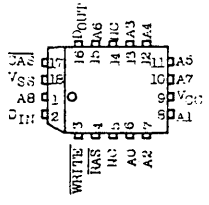
Plastic DIP	: TMM41257AP
Plastic Leaded Chip Carrier	: TMM41257AT
Plastic ZIP	: TMM41257AZ

PIN CONNECTION (TOP VIEW)

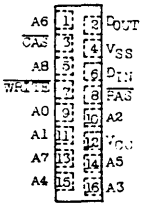
TMM41257AP



TMM41257AT



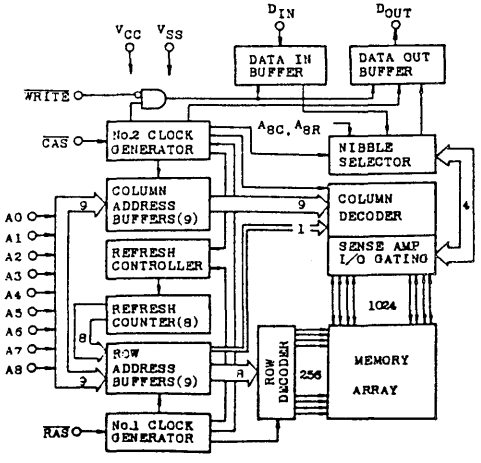
TMM41257AZ



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	80	mA	3, 4
		TMM41257AP/AT/AZ-12	–	72		
		TMM41257AP/AT/AZ-15	–	65		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, RAS Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	70	mA	3
		TMM41257AP/AT/AZ-12	–	62		
		TMM41257AP/AT/AZ-15	–	55		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{NC} = t_{NC} MIN.)	TMM41257AP/AT/AZ-10	–	50	mA	3, 4
		TMM41257AP/AT/AZ-12	–	48		
		TMM41257AP/AT/AZ-15	–	45		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC} = t_{RC} MIN.)	TMM41257AP/AT/AZ-10	–	70	mA	3
		TMM41257AP/AT/AZ-12	–	62		
		TMM41257AP/AT/AZ-15	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41257AP/AT/AZ-10		TMM41257AP/AT/AZ-12		TMM41257AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	–	220	–	260	–	ns	
t_{RWC}	Read-Write Cycle Time	200	–	240	–	285	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	220	–	260	–	310	–	ns	
t_{NC}	Nibble Mode Cycle Time	50	–	60	–	70	–	ns	
t_{NRWC}	Nibble Mode Read-Write/Read-Modify Write Cycle Time	75	–	90	–	105	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	100	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	50	–	60	–	75	ns	9, 10
t_{NCAC}	Nibble Mode Access Time	–	25	–	30	–	40	ns	10
t_{OFF}	Output Buffer Turn-Off Delay	5	25	5	30	5	35	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	–	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	–	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	20	–	25	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	25	–	30	–	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	–	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	20	–	25	–	30	–	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{WP}	Write Command Pulse Width	20	–	25	–	30	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	20	–	25	–	30	–	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	70	–	85	–	105	–	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	–	40	–	50	–	ns	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41257AP/AT/AZ-10		TMM41257AP/AT/AZ-12		TMM41257AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	80	–	100	–	125	–	ns	15
t_{NCAS}	Nibble Mode $\overline{CAS}$ Pulse Width	25	–	30	–	40	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	15	–	20	–	20	–	ns	
t_{NRRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Read)	20	–	25	–	30	–	ns	
t_{NWRSH}	Nibble Mode $\overline{RAS}$ Hold Time (Write)	40	–	45	–	50	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	30	–	40	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	–	50	–	60	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

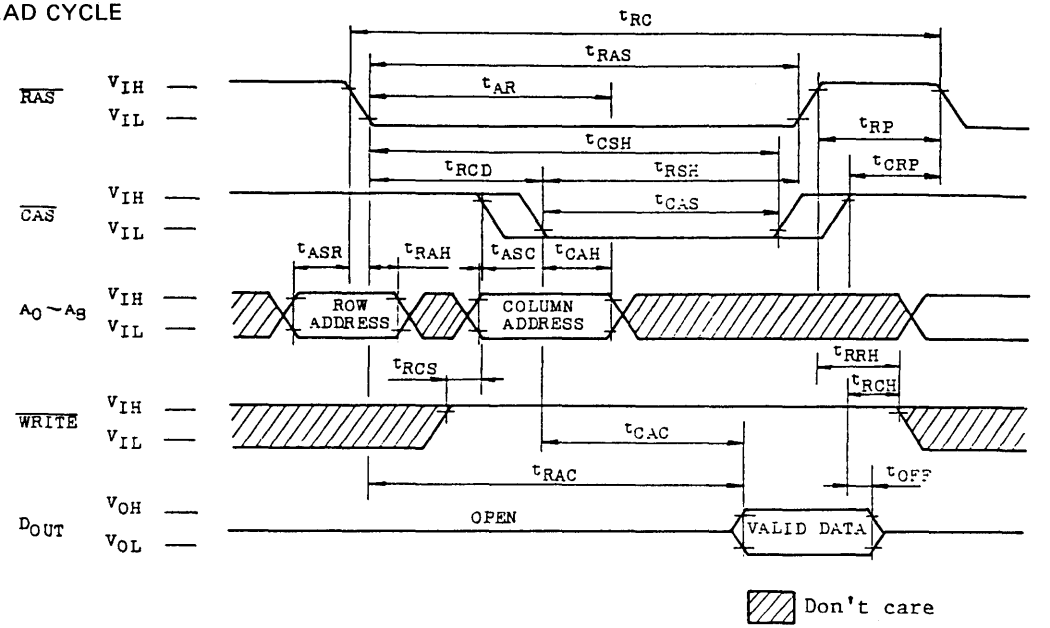
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance ($A_0 \sim A_8$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

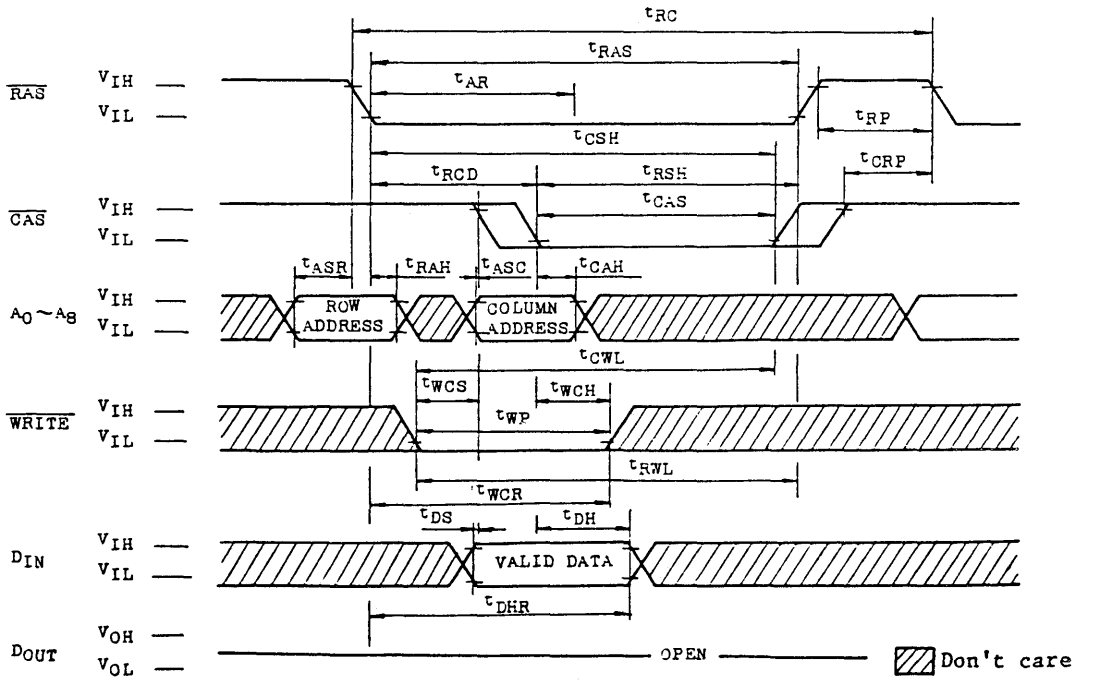
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.)
10. Measured with a load equivalent to 2 TTL loads and 100 pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAC} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

TIMING WAVEFORMS

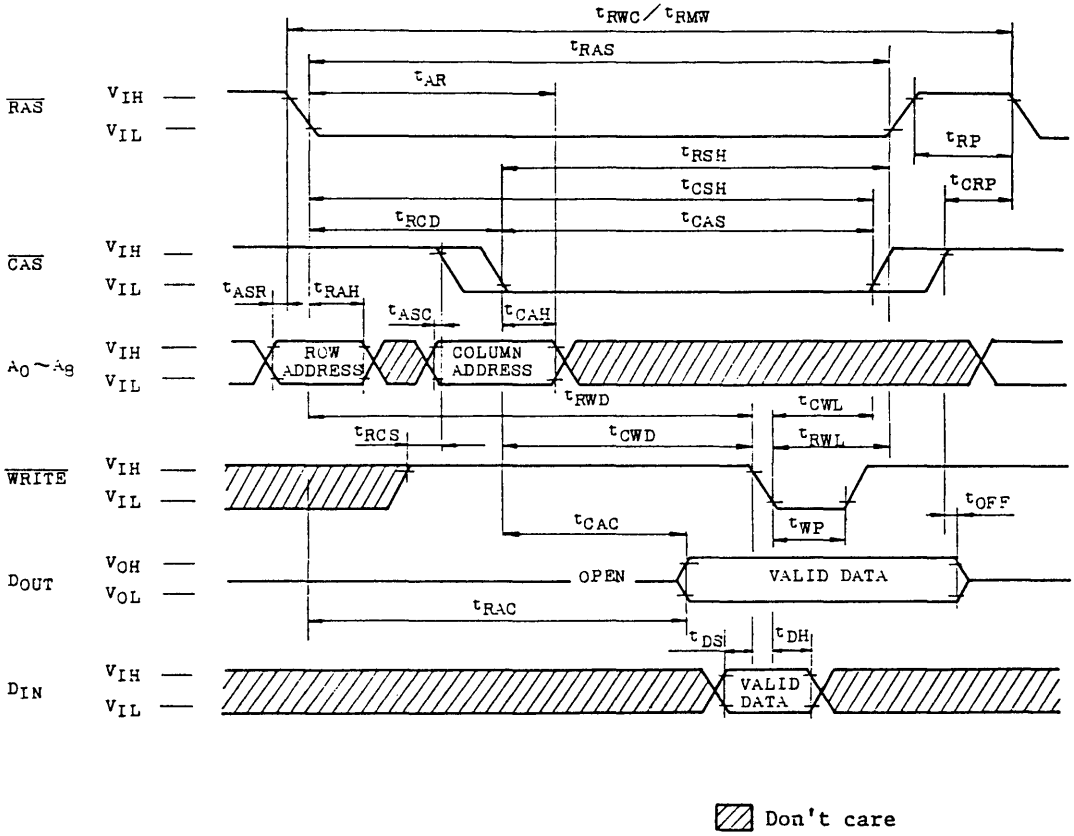
- READ CYCLE



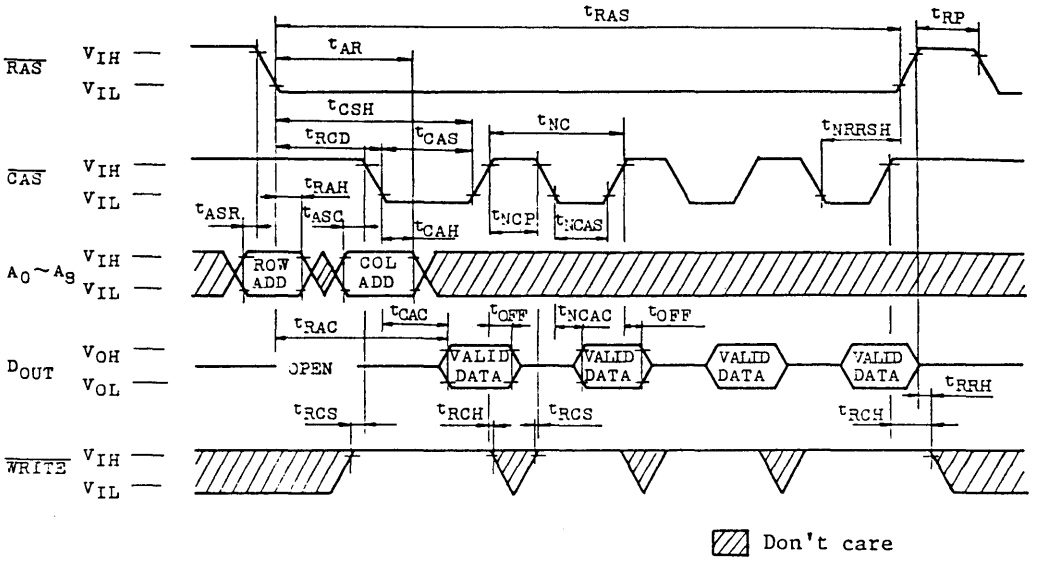
- WRITE CYCLE (EARLY WRITE)



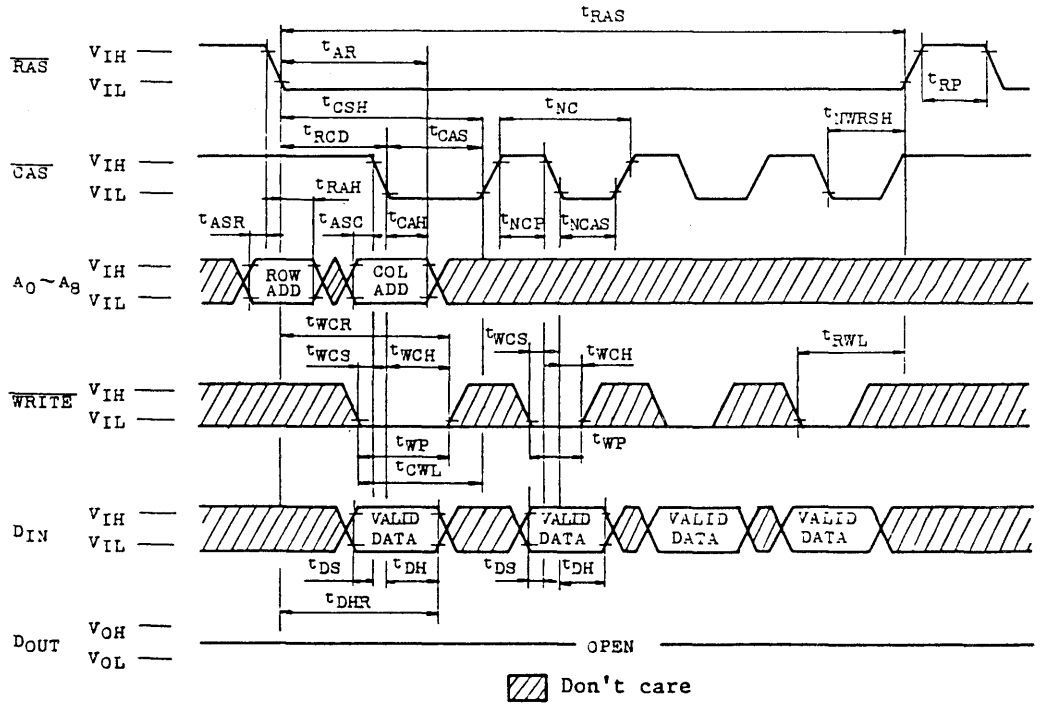
- READ-WRITE/READ-MODIFY-WRITE CYCLE



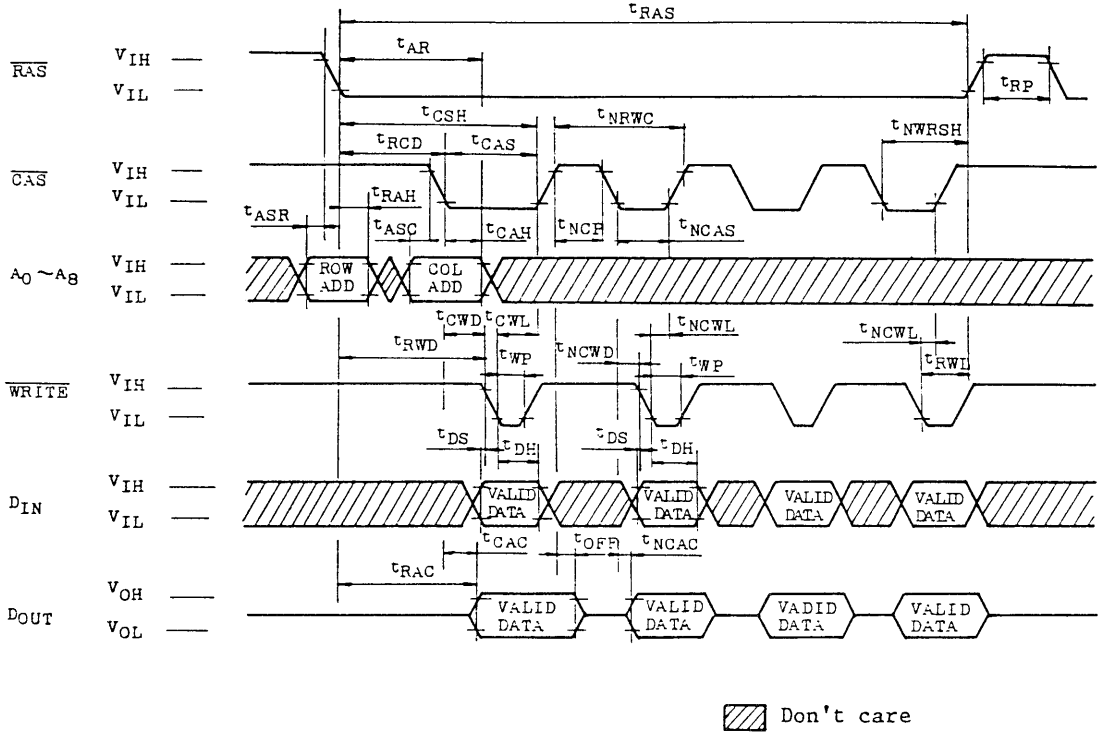
- NIBBLE MODE READ CYCLE



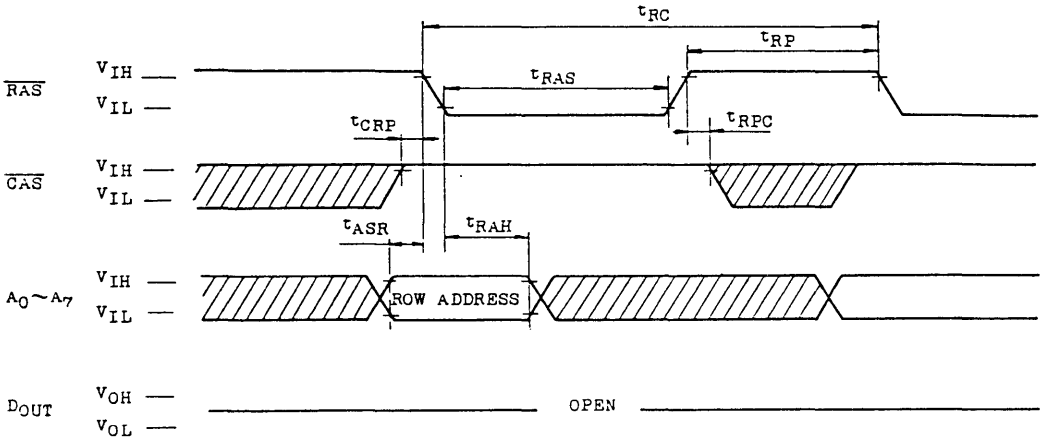
- NIBBLE MODE WRITE CYCLE (EARLY WRITE)



- NIBBLE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



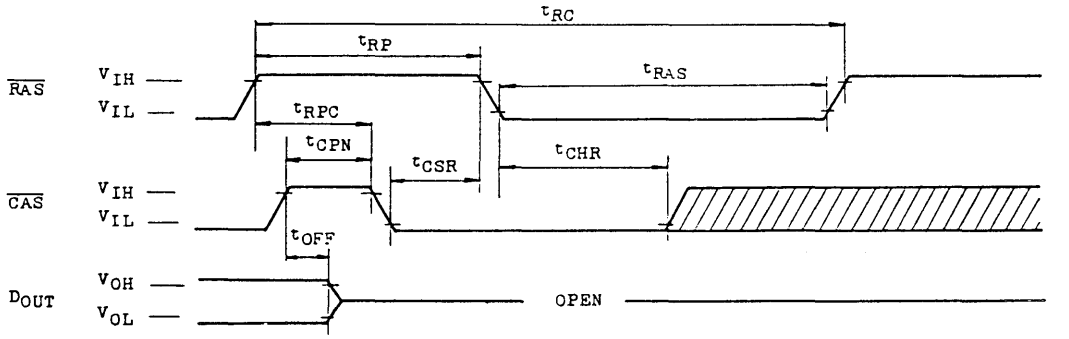
- $\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$=Don't care, A8=Don't care

Don't care

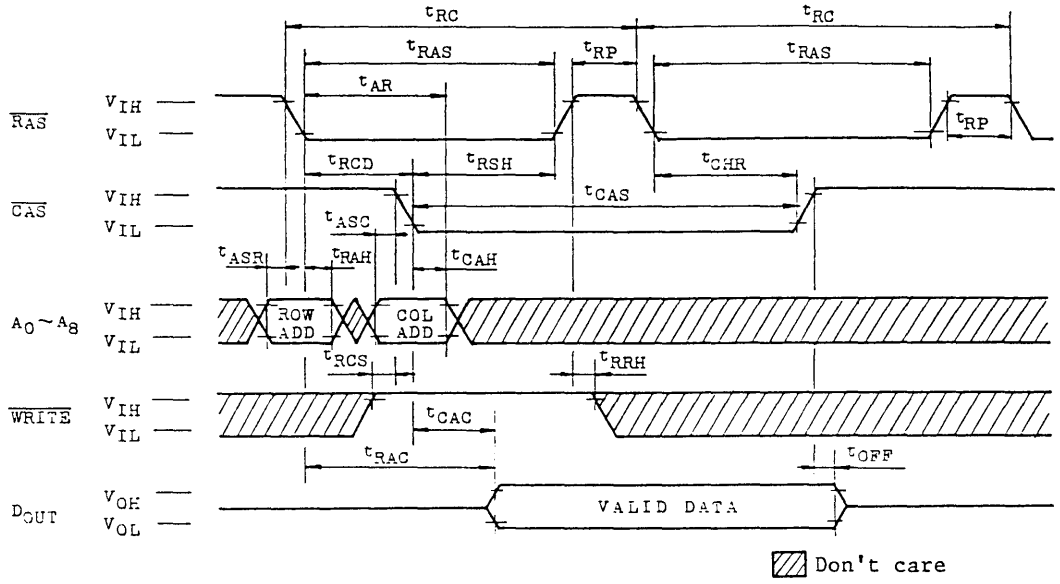
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



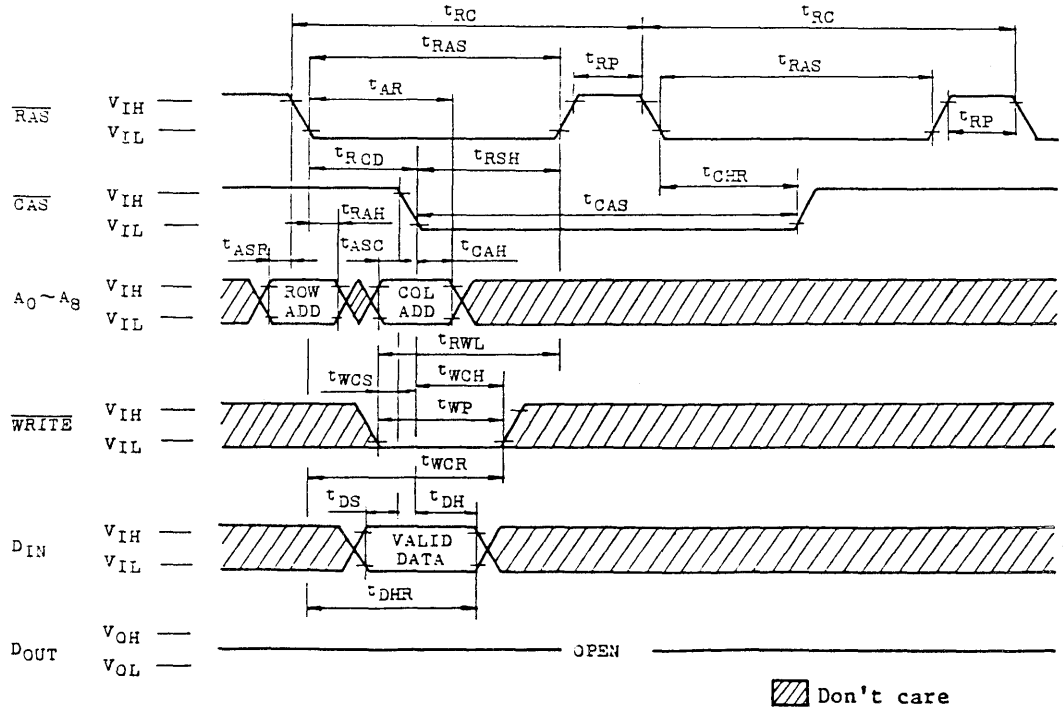
Note: $\overline{WRITE}$=Don't care, A0 ∿ A8=Don't care

Don't care

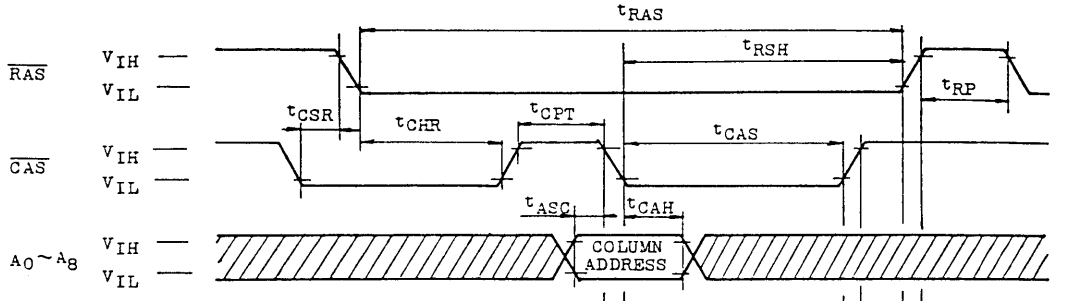
- HIDDEN REFRESH CYCLE (READ)



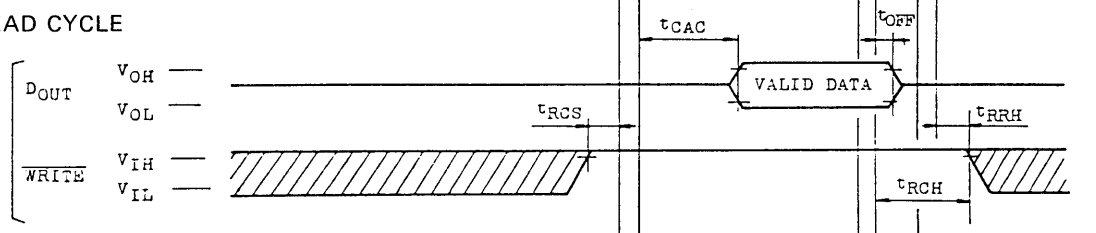
- HIDDEN REFRESH CYCLE (WRITE)



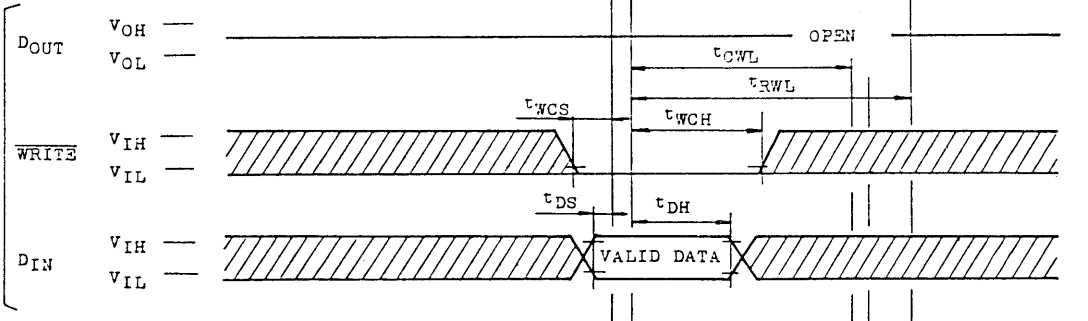
- $\overline{CAS}$ BEFORE RAS REFRESH COUNTER TEST CYCLE



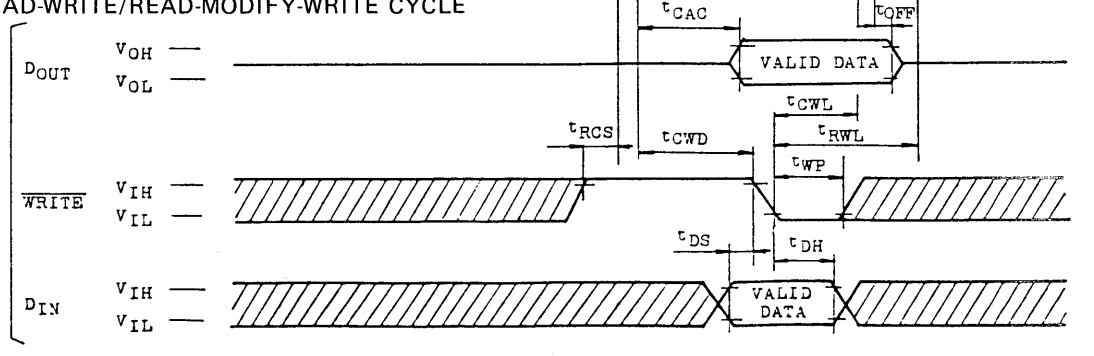
- READ CYCLE



- WRITE CYCLE



- READ-WRITE/READ-MODIFY-WRITE CYCLE



Don't care

APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TMM41257AP/AT/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

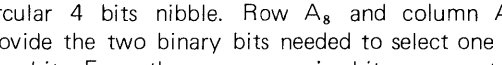
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TMM41257AP/AT/AZ is the high impedance (open circuit) state. This is to say, anytime CAS is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around) method).



Pin one (A_8) determines the starting point of the circular 4 bits nibble. Row A_8 and column A_8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A_8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond

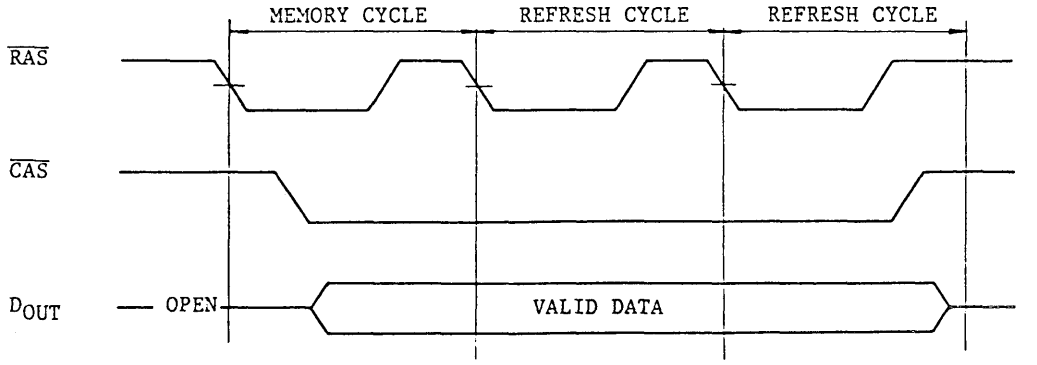
time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41257AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TMM41257AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_R), excuting a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41257AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

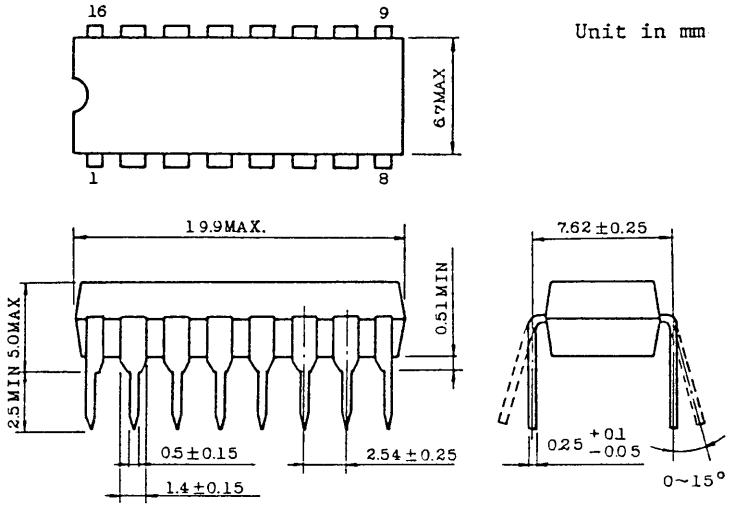
The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS

- Plastic DIP

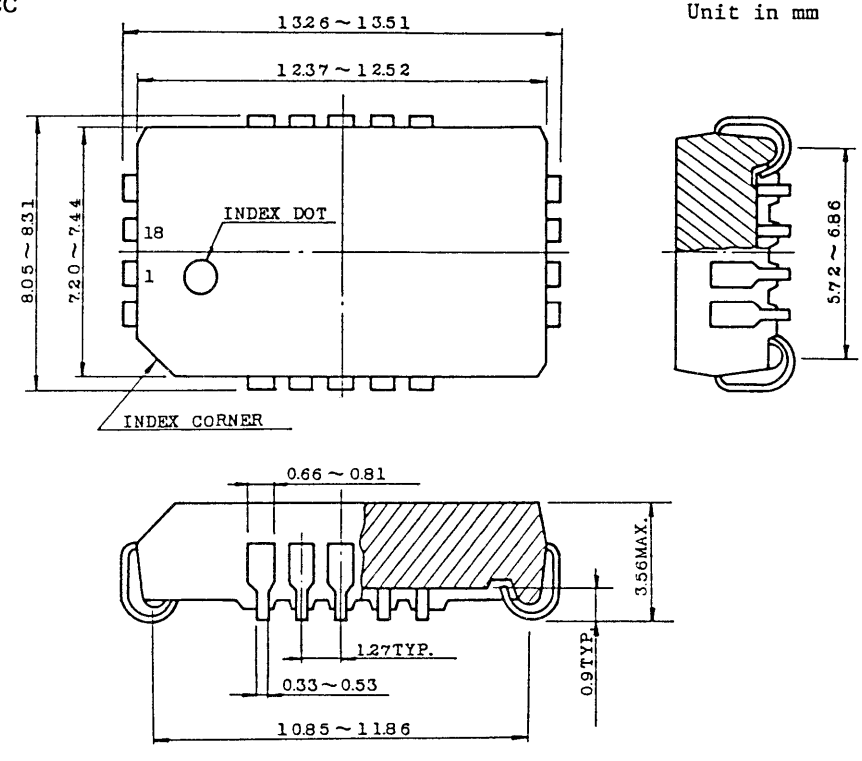
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 16 leads. All dimensions are in millimeters.

- Plastic LCC

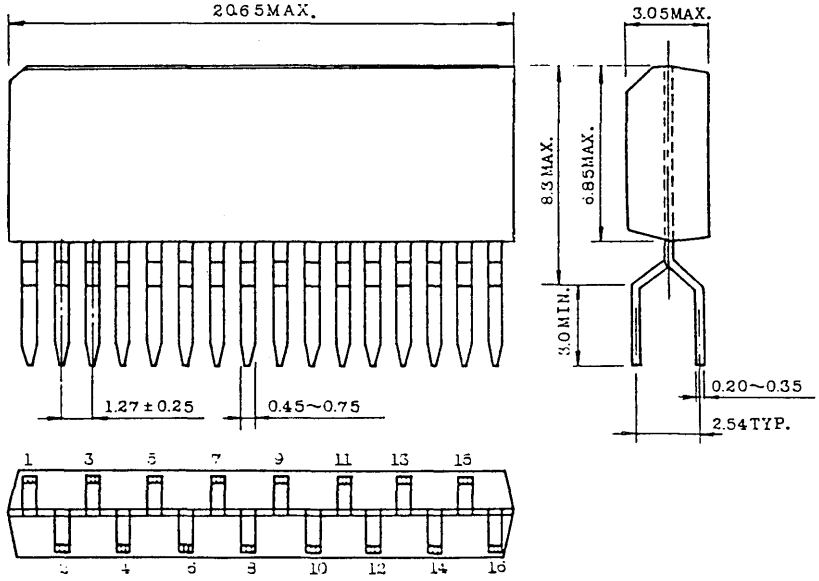
Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

- Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD×4 BIT DYNAMIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS

TMM41464AP/AT/AZ-10, TMM41464AP/AT/AZ-12 TMM41464AP/AT/AZ-15

DESCRIPTION

The TMM41464AP/AT/AZ is N-channel dynamic RAM organized 65,536 words by 4 bit. The TMM41464 AP/AT/AZ utilizes TOSHIBA's N-channel/Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TMM41464AP/AT/AZ to be package in a standard 18 pin plastic DIP, 18 pin PLCC and 20 pin ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic familes such as schottky TTL.

FEATURES

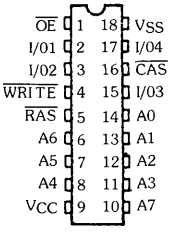
- 65,536 words by 4 bit organization
- Fast access time and cycle time

DEVICE	tRAC	tCAC	tRC
TMM41464AP/AT/AZ-10	100ns	50ns	190ns
TMM41464AP/AT/AZ-12	120ns	60ns	220ns
TMM41464AP/AT/AZ-15	150ns	75ns	260ns

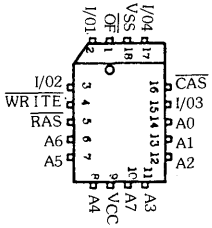
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Lower Power:
  440mW MAX. Operating (TMM41464AP/AT/AZ-10)
  396mW MAX. Operating (TMM41464AP/AT/AZ-12)
  358mW MAX. Operating (TMM41464AP/AT/AZ-15)
  28mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{RAS}$ only refresh, Hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package
  Plastic DIP : TMM41464AP
  Plastic Leaded Chip Carrier : TMM41464AT
  Plastic ZIP : TMM41464AZ

PIN CONNECTION

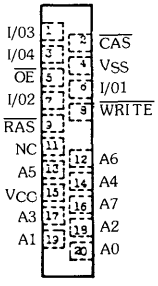
TMM41464AP



TMM41464AT



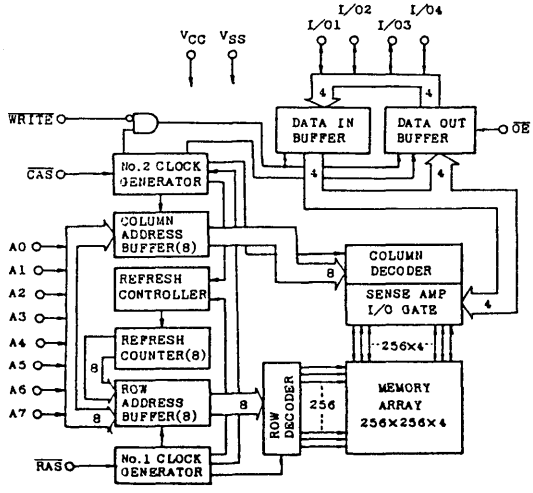
TMM41464AZ



PIN NAMES

A0 ~ A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
I/01 ~ I/04	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input and Output Voltage	V_{IN}, V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	
Operating Temperature	T_{OPR}	0 ~ 70	°C	
Storage Temperature	T_{STG}	−55 ~ 150	°C	
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	
Power Dissipation	P_D	1	W	
Short Circuit Output Current	I_{OUT}	50	mA	

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	80	mA	3, 4
		TMM41464AP/AT/AZ-12	–	72		
		TMM41464AP/AT/AZ-15	–	65		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	70	mA	3
		TMM41464AP/AT/AZ-12	–	62		
		TMM41464AP/AT/AZ-15	–	55		
I_{CC4}	PAGE MODE CURRENT Average Power Supply Current, Page Mode ($\overline{RAS}$ = V_{IL} , $\overline{CAS}$ Cycling: t_{PC} = t_{PC} MIN.)	TMM41464AP/AT/AZ-10	–	60	mA	3, 4
		TMM41464AP/AT/AZ-12	–	55		
		TMM41464AP/AT/AZ-15	–	50		
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$: t_{RC} = t_{RC} MIN.)	TMM41464AP/AT/AZ-10	–	70	mA	3
		TMM41464AP/AT/AZ-12	–	62		
		TMM41464AP/AT/AZ-15	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Unter Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ + 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TMM41464AP/AT/AZ-10		TMM41464AP/AT/AZ-12		TMM41464AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	–	220	–	260	–	ns	
t_{RMW}	Read-Modify Write Cycle Time	260	–	300	–	355	–	ns	
t_{PC}	Page Mode Cycle Time	100	–	120	–	145	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	100	–	120	–	150	ns	8, 10
t_{CAC}	Access Time from $\overline{CAS}$	–	50	–	60	–	75	ns	9, 10
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	0	40	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	–	90	–	100	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	150	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	50	–	60	–	75	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	–	120	–	150	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	50	10,000	60	10,000	75	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	60	25	75	ns	13
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	20	–	20	–	25	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	40	–	50	–	60	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	25	–	35	–	ns	
t_{AR}	Column Address Hold Time Reference to $\overline{RAS}$	70	–	85	–	110	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time Reference to $\overline{CAS}$	0	–	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time Reference to $\overline{RAS}$	10	–	15	–	20	–	ns	12
t_{WCH}	Write Command Hold Time	30	–	35	–	45	–	ns	
t_{WCR}	Write Command Hold Time Reference to $\overline{RAS}$	80	–	95	–	120	–	ns	
t_{WP}	Write Command Pulse Width	30	–	35	–	45	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30	–	35	–	45	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30	–	35	–	45	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	14
t_{DH}	Data-In Hold Time	30	–	35	–	45	–	ns	14
t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	80	–	95	–	120	–	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	15
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	85	–	100	–	120	–	ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	135	–	160	–	195	–	ns	15
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	–	40	ns	9, 10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TMM41464AP/AT/AZ-10		TMM41464AP/AT/AZ-12		TMM41464AP/AT/AZ-15		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{OED}	$\overline{OE}$ to Data Delay	25	–	30	–	40	–	ns	
t_{OEZ}	Output Buffer Turn-Off Delay Time from $\overline{OE}$	0	25	0	30	0	40	ns	
t_{OEH}	$\overline{OE}$ command Hold Time	25	–	30	–	40	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	30	–	30	–	30	–	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	10	–	10	–	10	–	ns	
t_{RPC}	$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	20	–	25	–	35	–	ns	
t_{ROH}	$\overline{OE}$ Command Hold Time	10	–	10	–	10	–	ns	

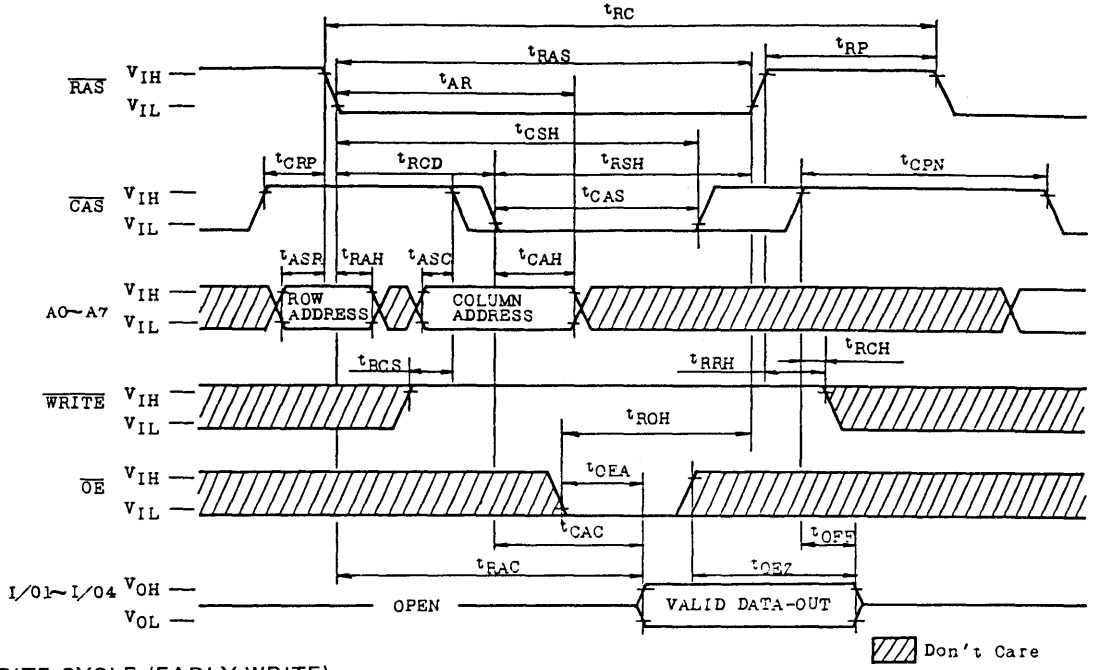
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
CI1	Input Capacitance (A0 ~ A7)	——	5	pF
CI2	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	——	7	
C_o	Input/Output Capacitance (I/01 ~ I/04)	——	7	

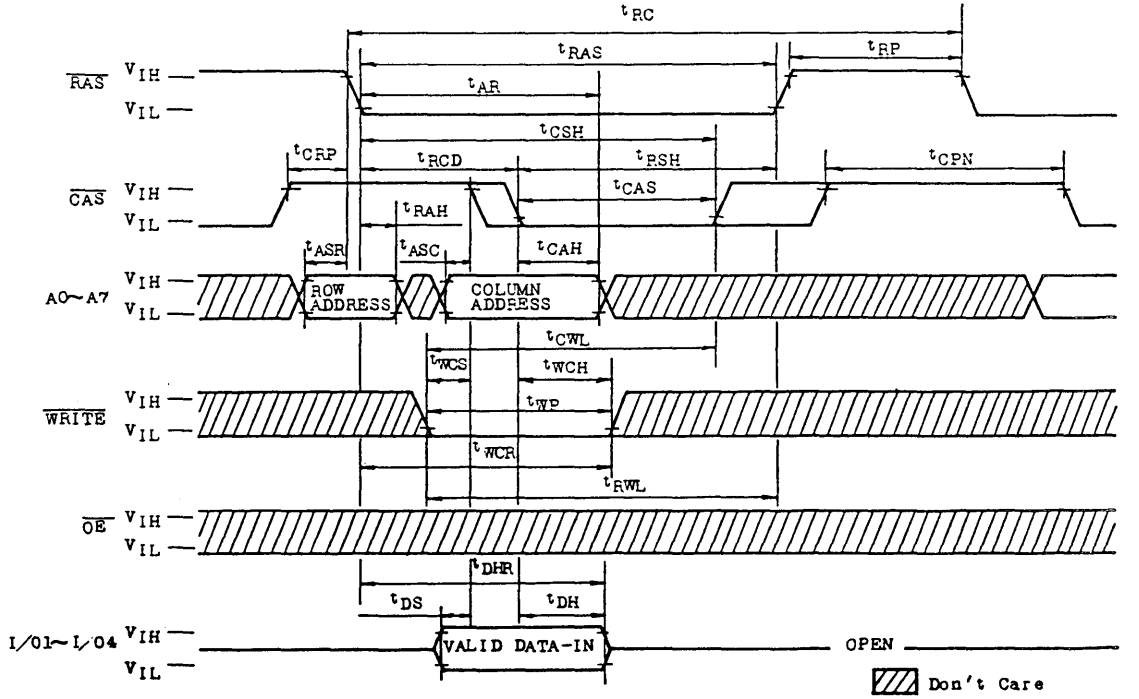
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC5} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5 ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
10. Measured with a load equivalent to 2 TTL loads and 100 pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write or read-modify-write cycles.
15. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the input/output pin will remain open circuits (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle or read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

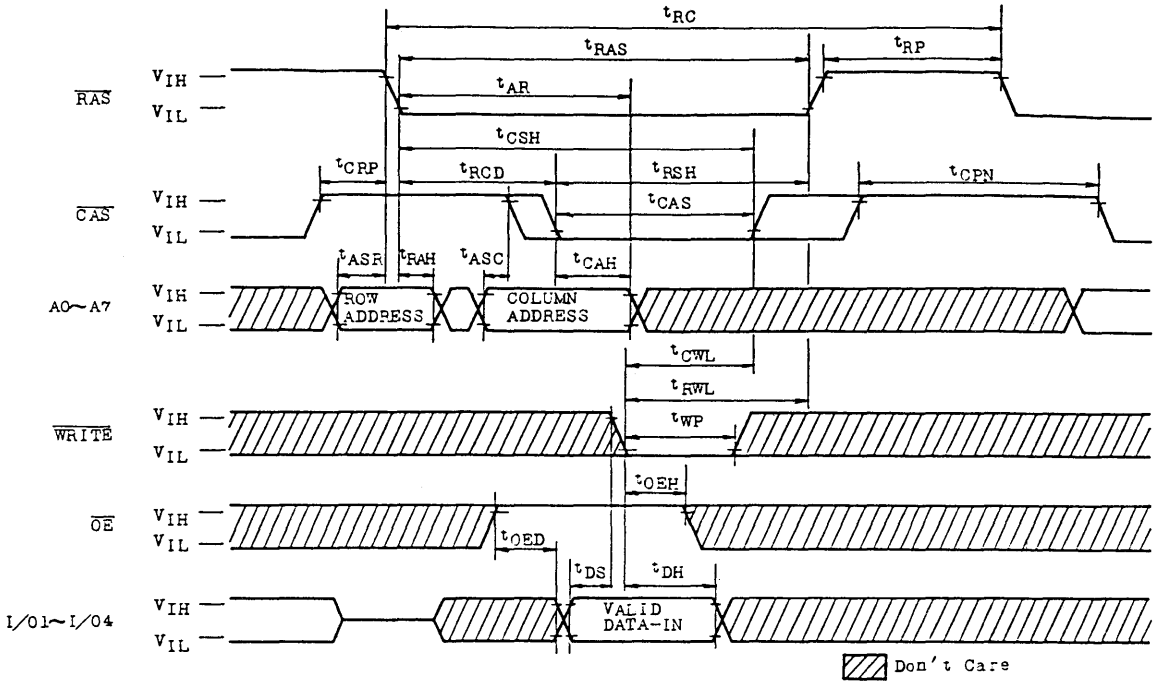
- READ CYCLE



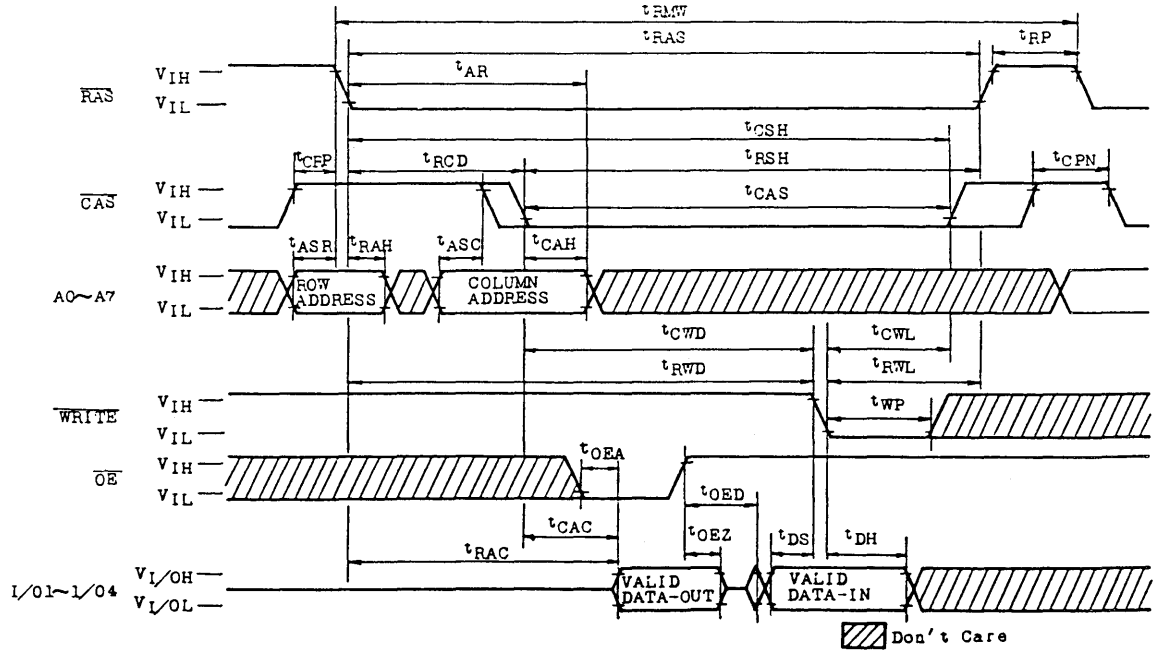
- WRITE CYCLE (EARLY WRITE)



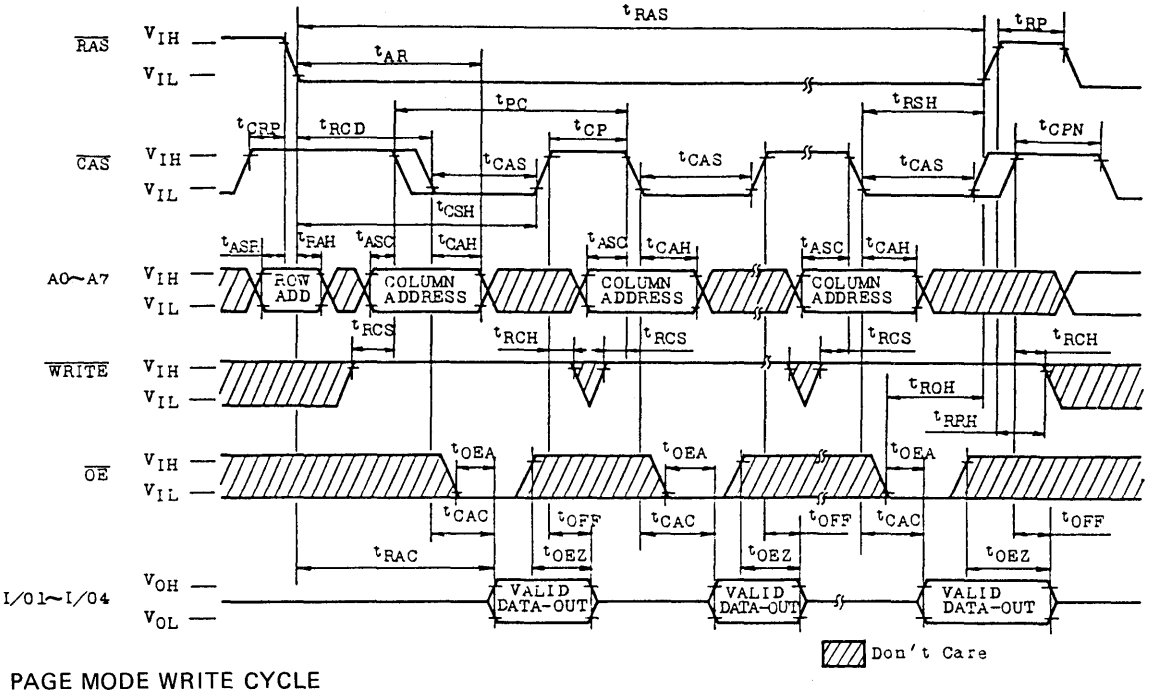
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



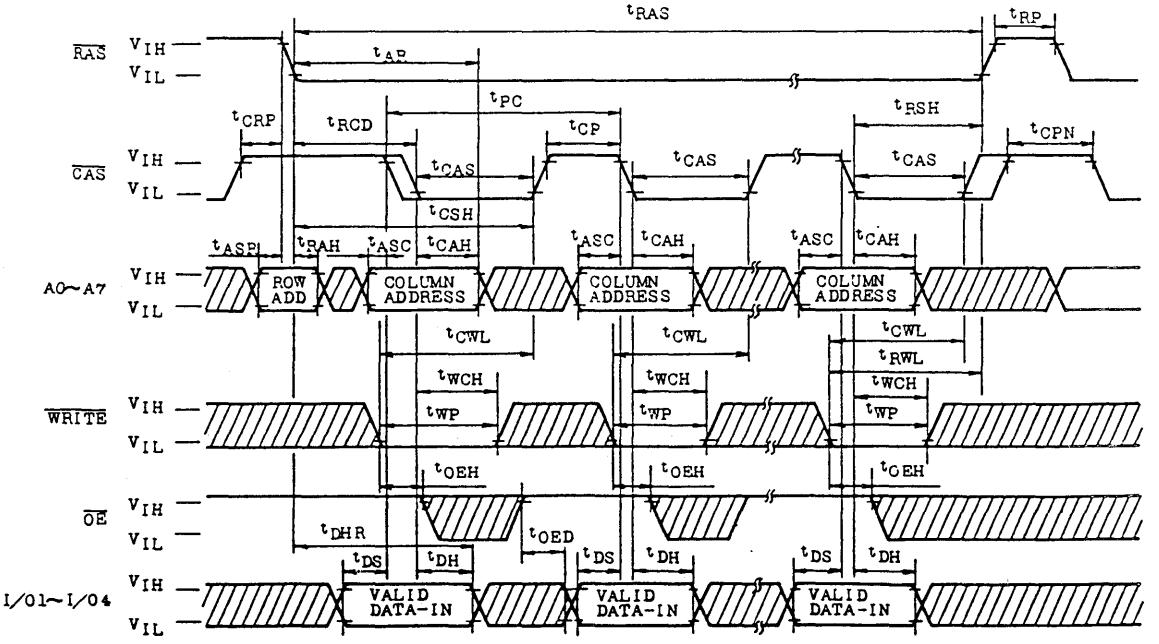
- READ-WRITE/READ-MODIFY-WRITE CYCLE



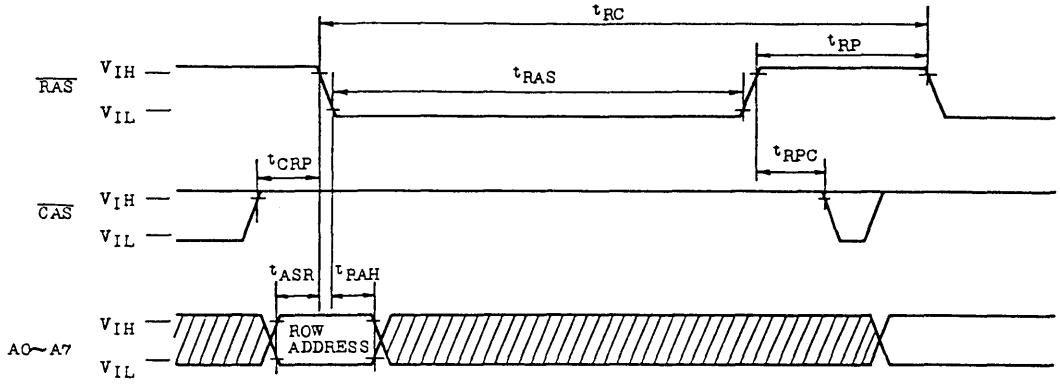
- PAGE MODE READ CYCLE



- PAGE MODE WRITE CYCLE

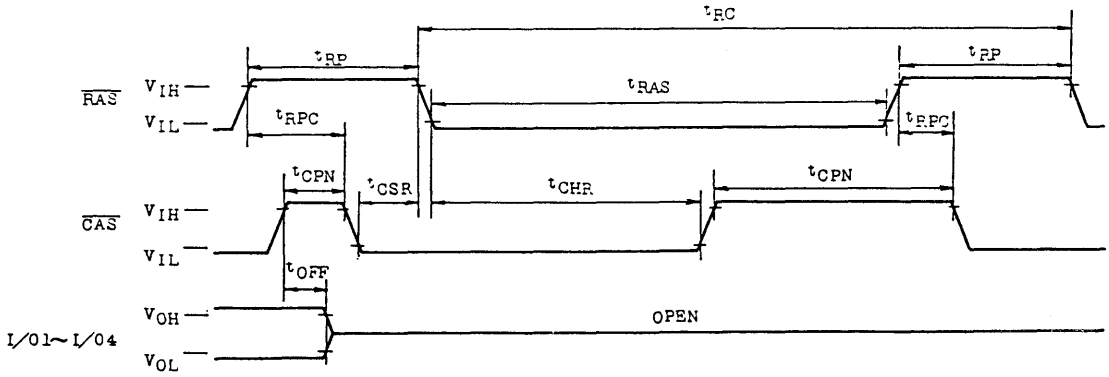


- $\overline{RAS}$ ONLY REFRESH CYCLE



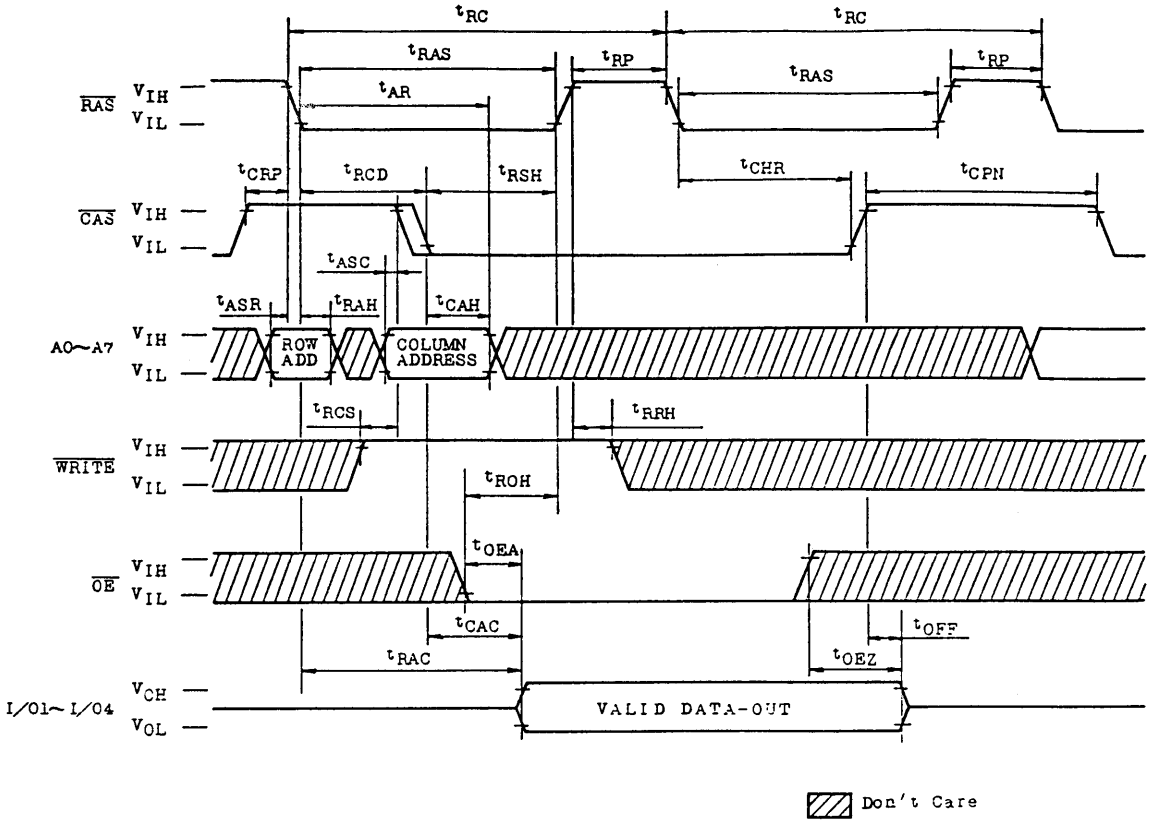
Notes: $\overline{WRITE}$, $\overline{OE}$=Don't Care Don't Care

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

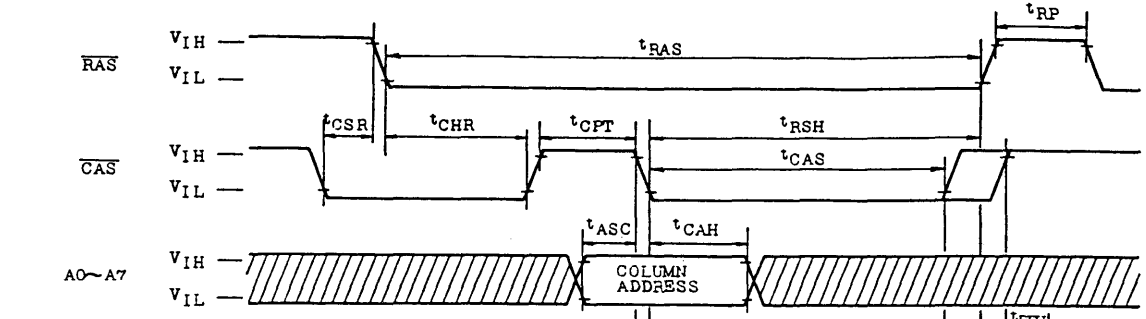


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A7=Don't Care

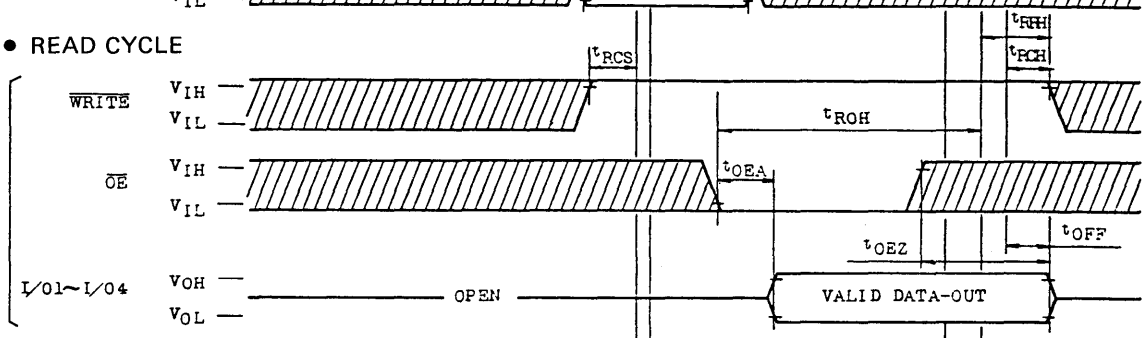
- HIDDEN REFRESH CYCLE



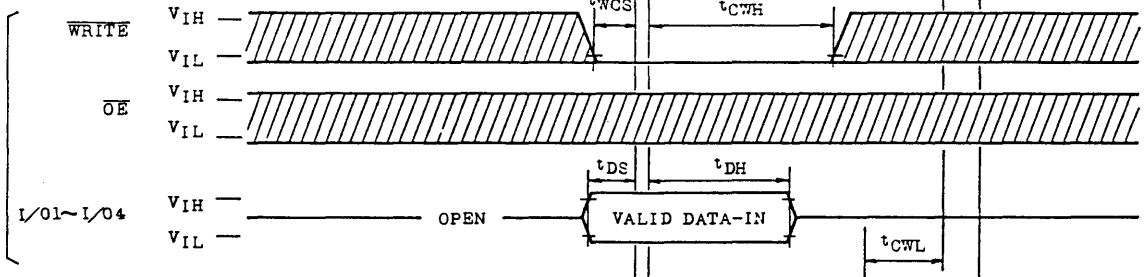
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



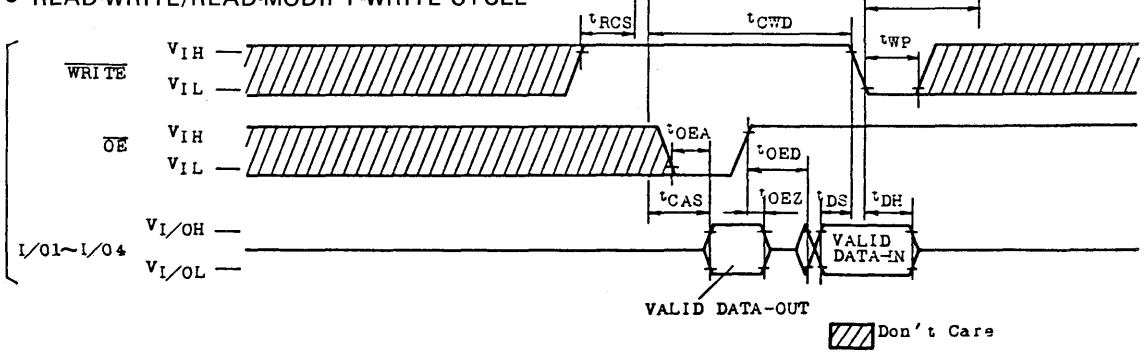
- READ CYCLE



- WRITE CYCLE



- READ-WRITE/READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TMM41464AP/AT/AZ are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Data is written during a write or read-modify-write cycle.

The falling edge of $\overline{CAS}$ or $\overline{WRITE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WRITE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WRITE}$ with setup and hold times referenced to this signal.

In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffer to high impedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid which $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logic low level, the output buffer are enabled. Both $\overline{CAS}$ and OE can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row address ($A_0 \sim A_7$) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TMM41464AP/AT/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

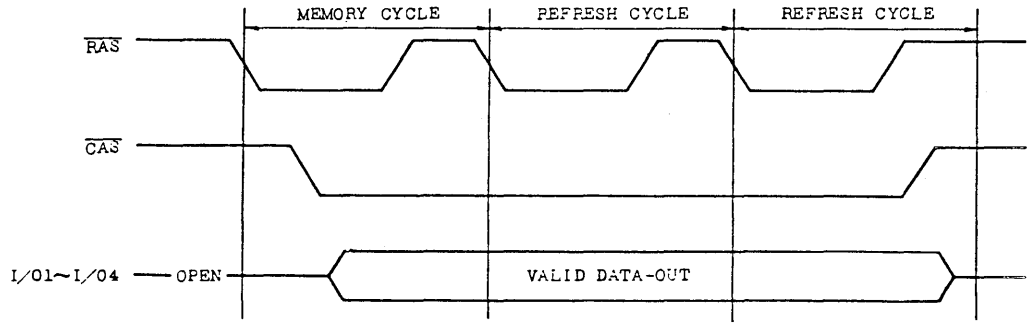
PAGE MODE

The "Page-Mode" feature of the TMM41464AP/AT/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the

chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TMM41464AP/AT/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TMM41464AP/AT/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

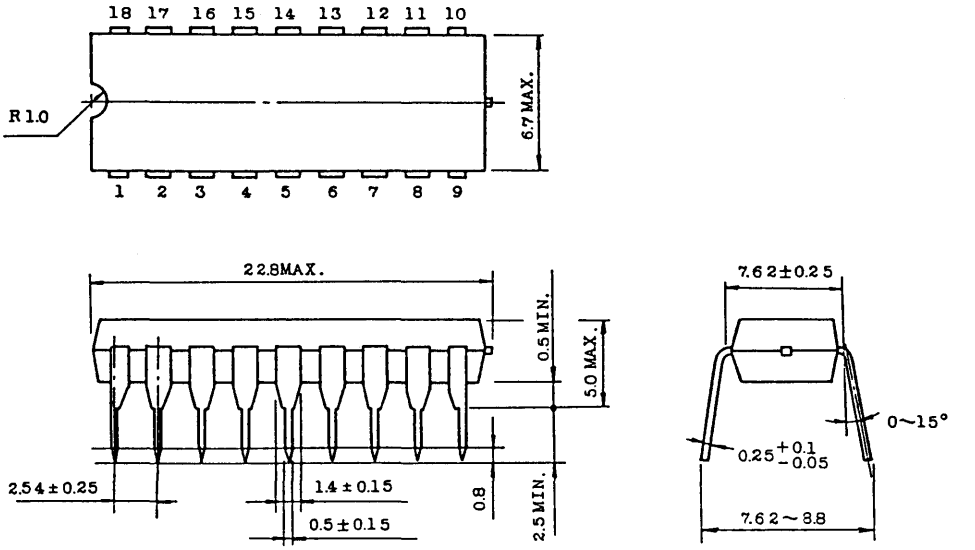
The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ to the complement data.

OUTLINE DRAWINGS

- Plastic DIP

Unit in mm

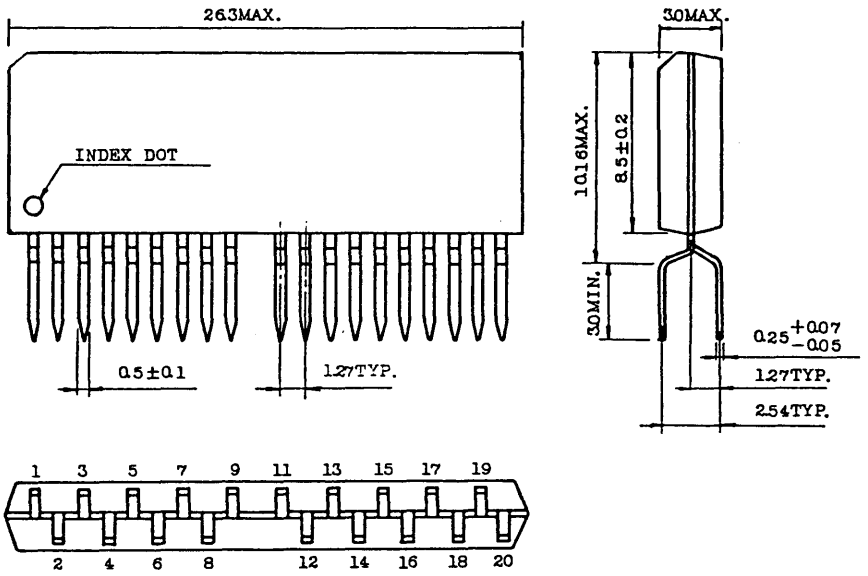


Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads. All dimensions are in millimeters.

Note: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

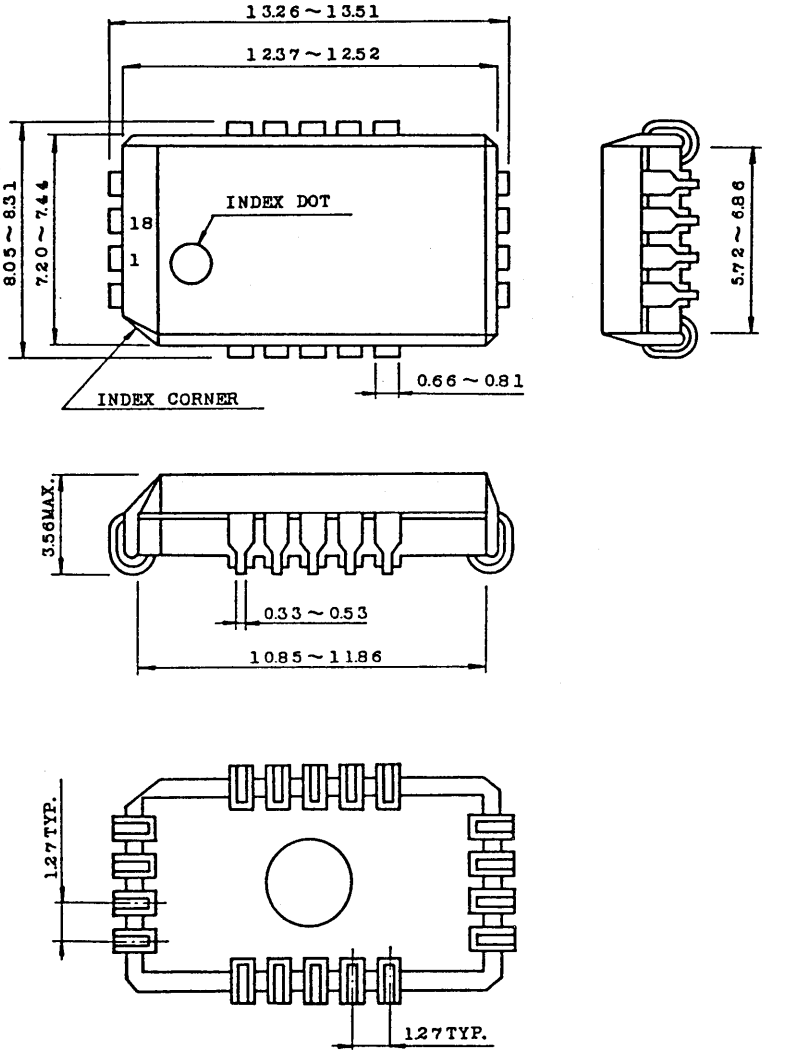
- Plastic ZIP

Unit in mm



- Plastic LCC

Unit in mm



TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD × 1 BIT DYNAMIC RAM

SILICON GATE CMOS

TC511000P/J/Z-85, TC511000P/J/Z-10 TC511000P/J/Z-12

DESCRIPTION

The TC511000P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

FEATURES

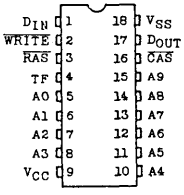
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85 ns	100 ns	120 ns
t_{AA}	Column Address Access Time	45 ns	50 ns	60 ns
t_{CAC}	$\overline{CAS}$ Access Time	25 ns	25 ns	30 ns
t_{RC}	Cycle Time	165 ns	190 ns	220 ns
t_{PC}	Fast Page Mode Cycle Time	50 ns	55 ns	70 ns

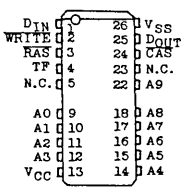
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating (TC511000P/J/Z-85)
  330mW MAX. Operating (TC511000P/J/Z-10)
  275mW MAX. Operating (TC511000P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8 ms
- Package Plastic DIP : TC511000P
  Plastic SOJ : TC511000J
  Plastic ZIP : TC511000Z

PIN CONNECTION (TOP VIEW)

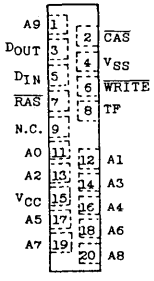
Plastic DIP



Plastic SOJ



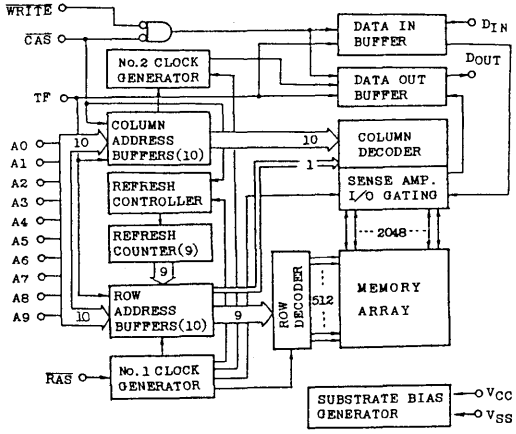
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	−1 ~ 10.5	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC} +4.5	–	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0	–	V_{CC} +1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling : t_{RC} = t_{RC} MIN.)	TC511000P/J/Z-85	–	70	mA	3, 4
		TC511000P/J/Z-10	–	60		
		TC511000P/J/Z-12	–	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511000P/J/Z-85	–	70	mA	3
		TC511000P/J/Z-10	–	60		
		TC511000P/J/Z-12	–	50		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511000P/J/Z-85	–	50	mA	3, 4
		TC511000P/J/Z-10	–	40		
		TC511000P/J/Z-12	–	30		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511000P/J/Z-85	–	70	mA	3
		TC511000P/J/Z-10	–	60		
		TC511000P/J/Z-12	–	50		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ V_{IN} (TF) ≦ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} =−5 mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2 mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P J/Z-10		TC511000P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RWC}	Read-Write Cycle Time	190	–	220	–	255	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	70	–	ns	
t_{PRWC}	Fast Page Mode Read-Write Cycle Time	75	–	85	–	105	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	–	5	–	5	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data Hold Time	20	–	20	–	25	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000P/J/Z-85		TC511000P/J/Z-10		TC511000P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	25	–	30	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	–	100	–	120	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1 MHz, Ta = 0 ~ 70°C)

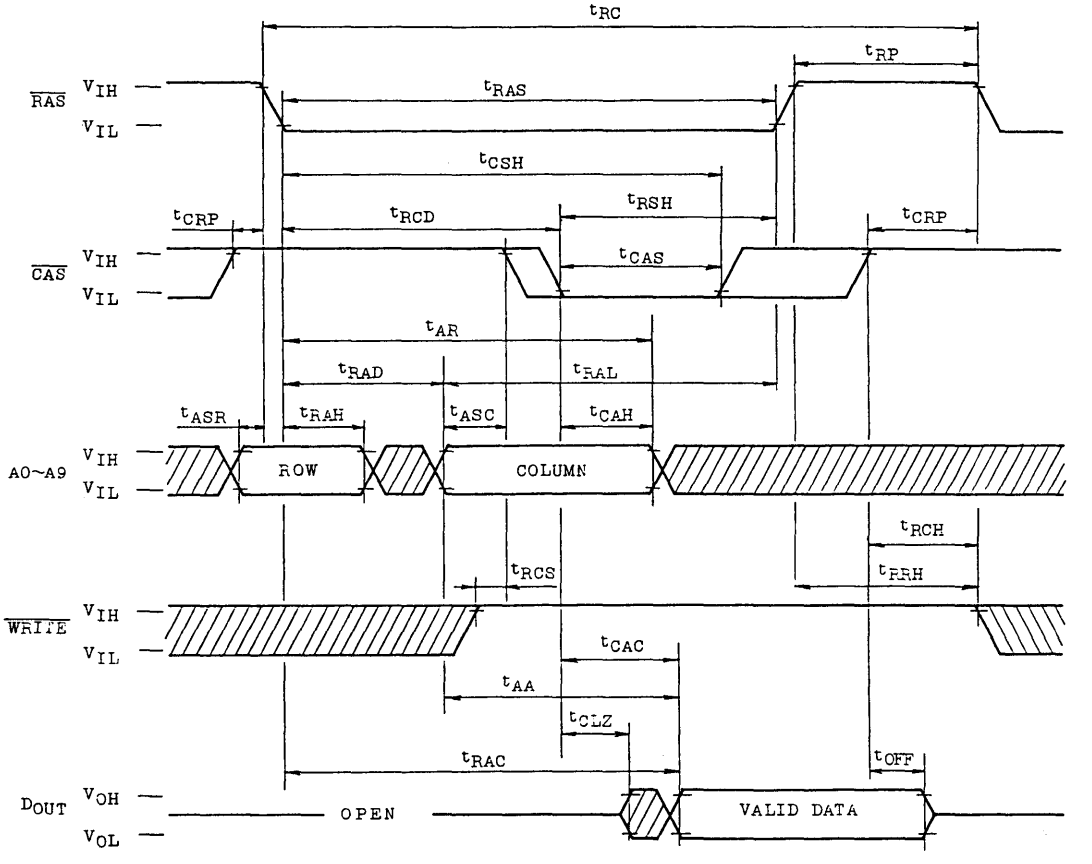
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

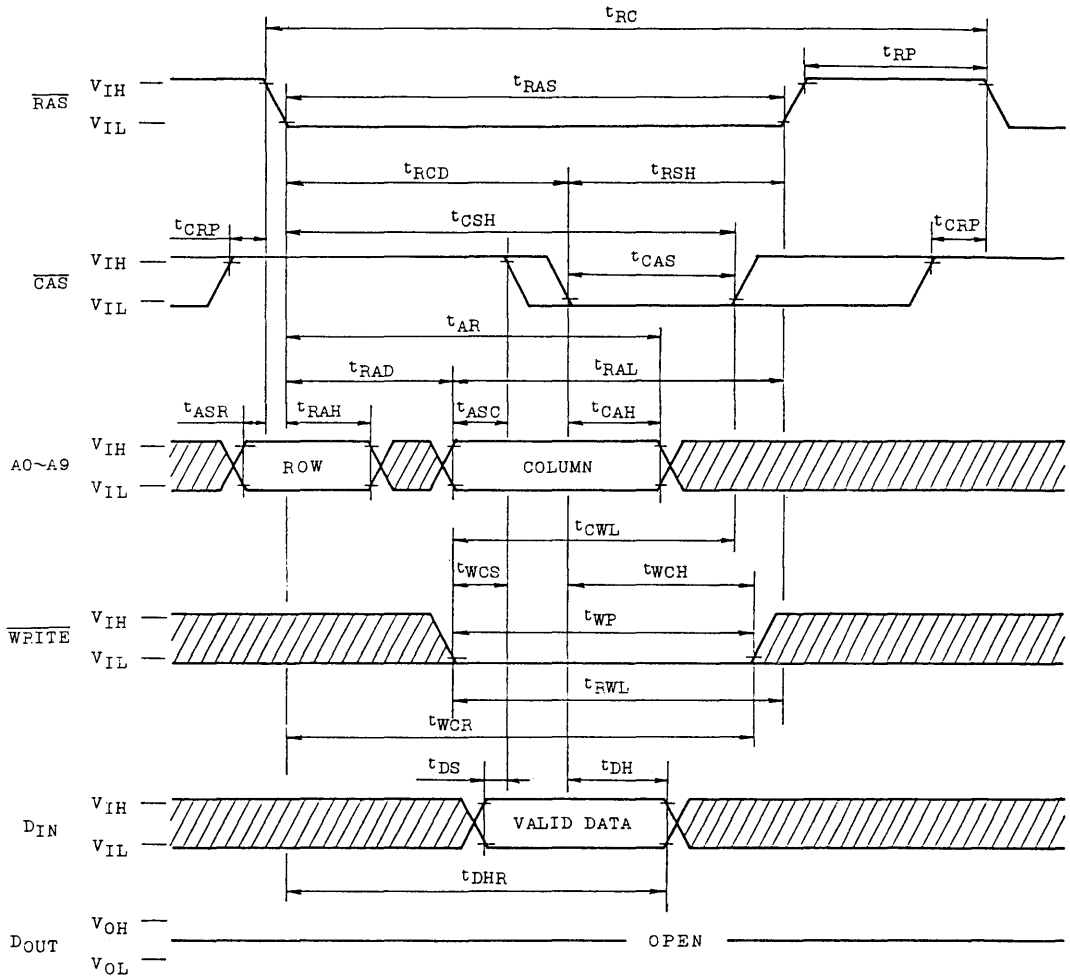
- READ CYCLE



: "H" or "L"

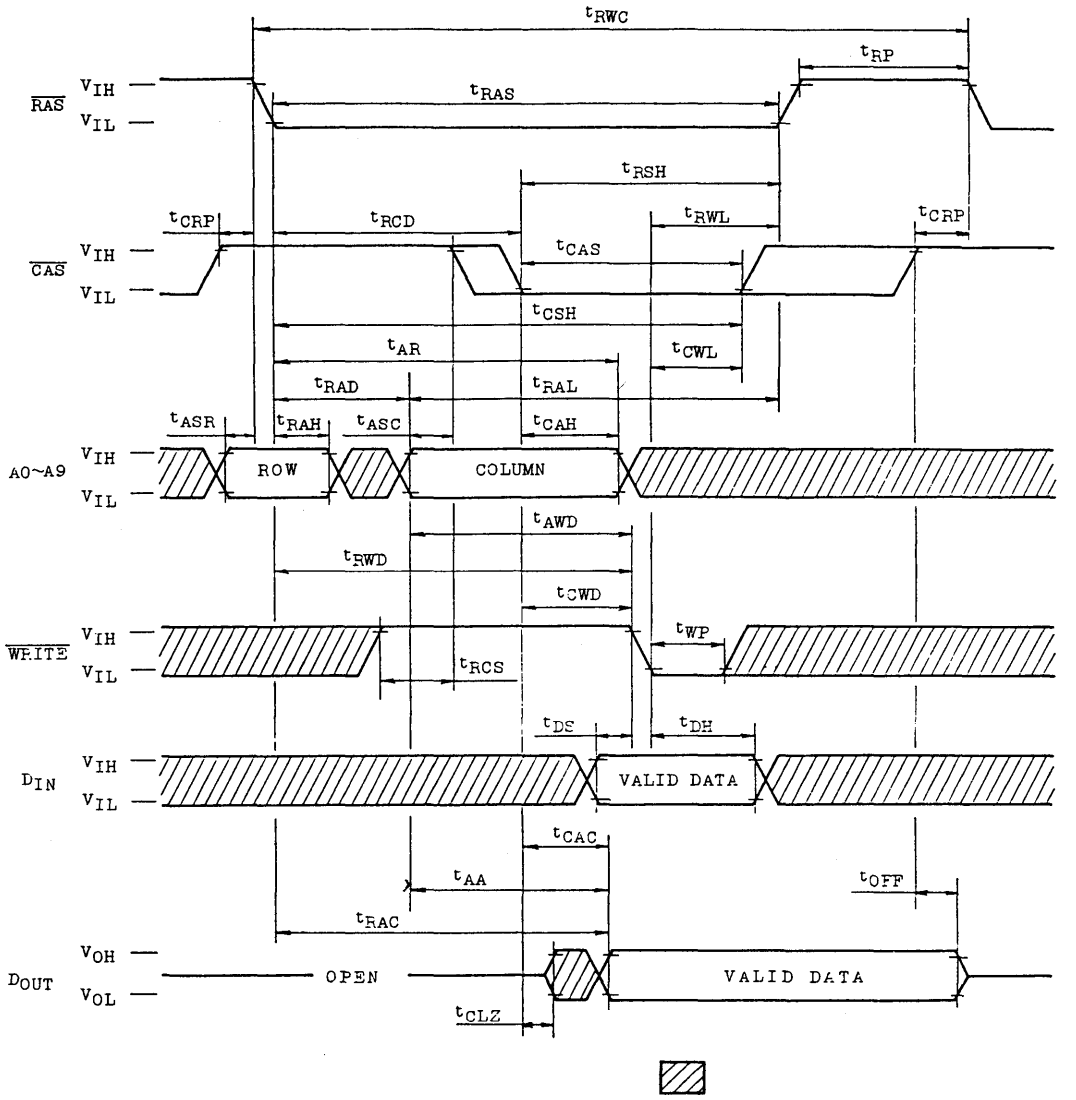
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- WRITE CYCLE (EARLY WRITE)



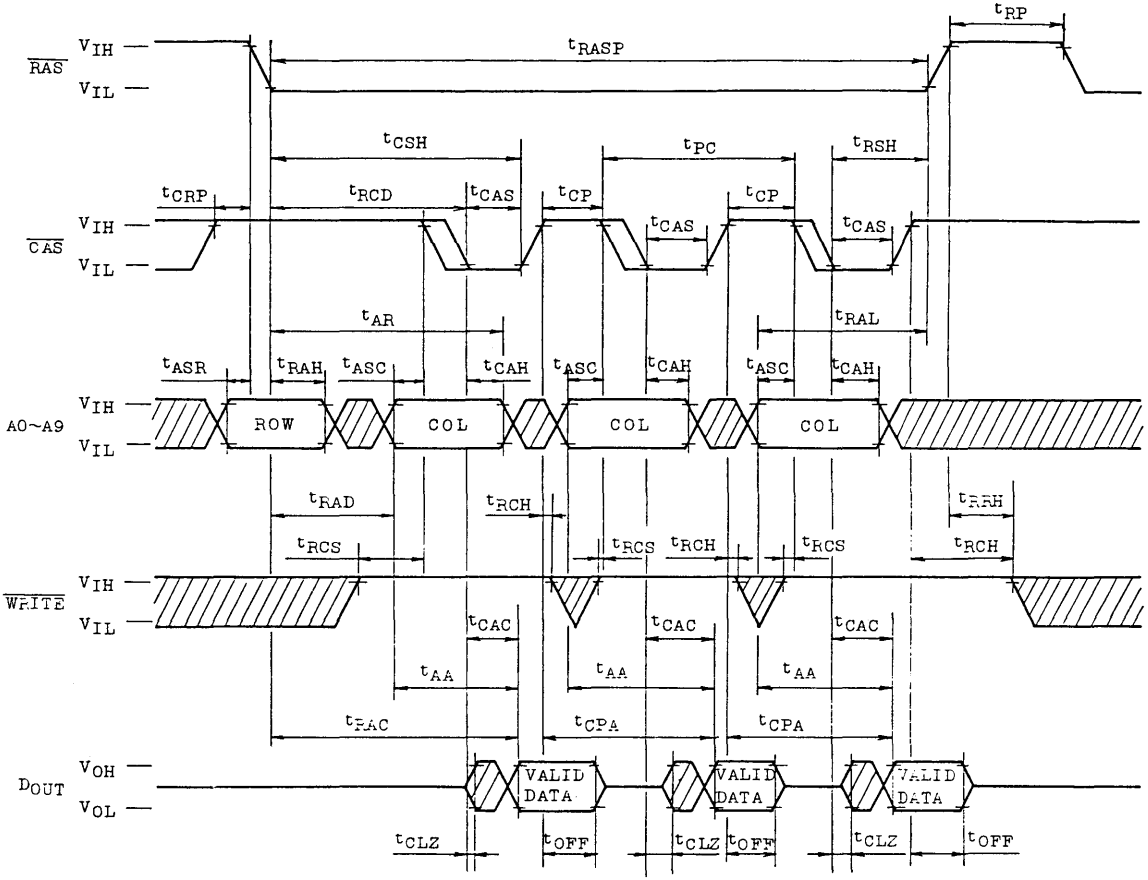
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- READ-WRITE CYCLE



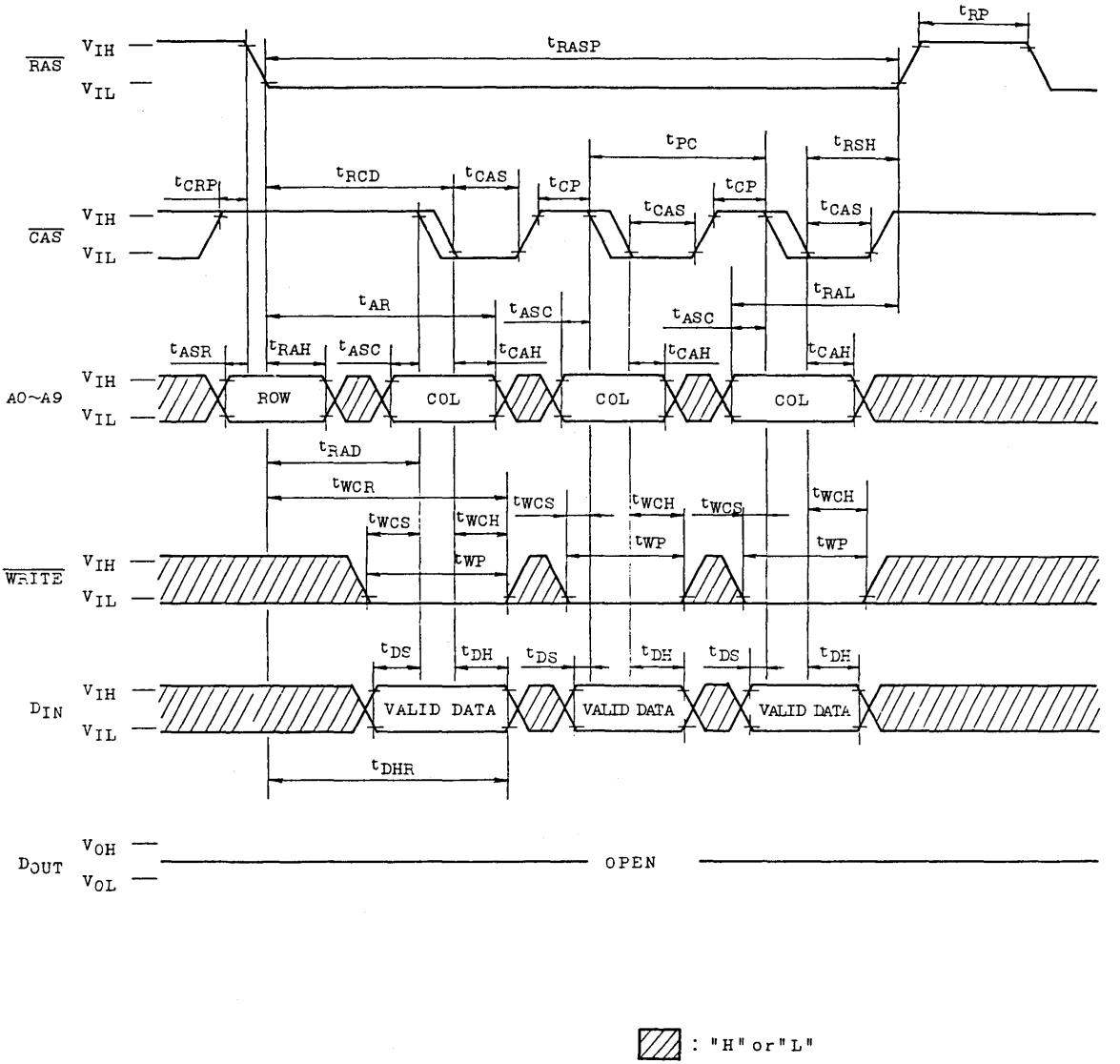
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- FAST PAGE MODE READ CYCLE



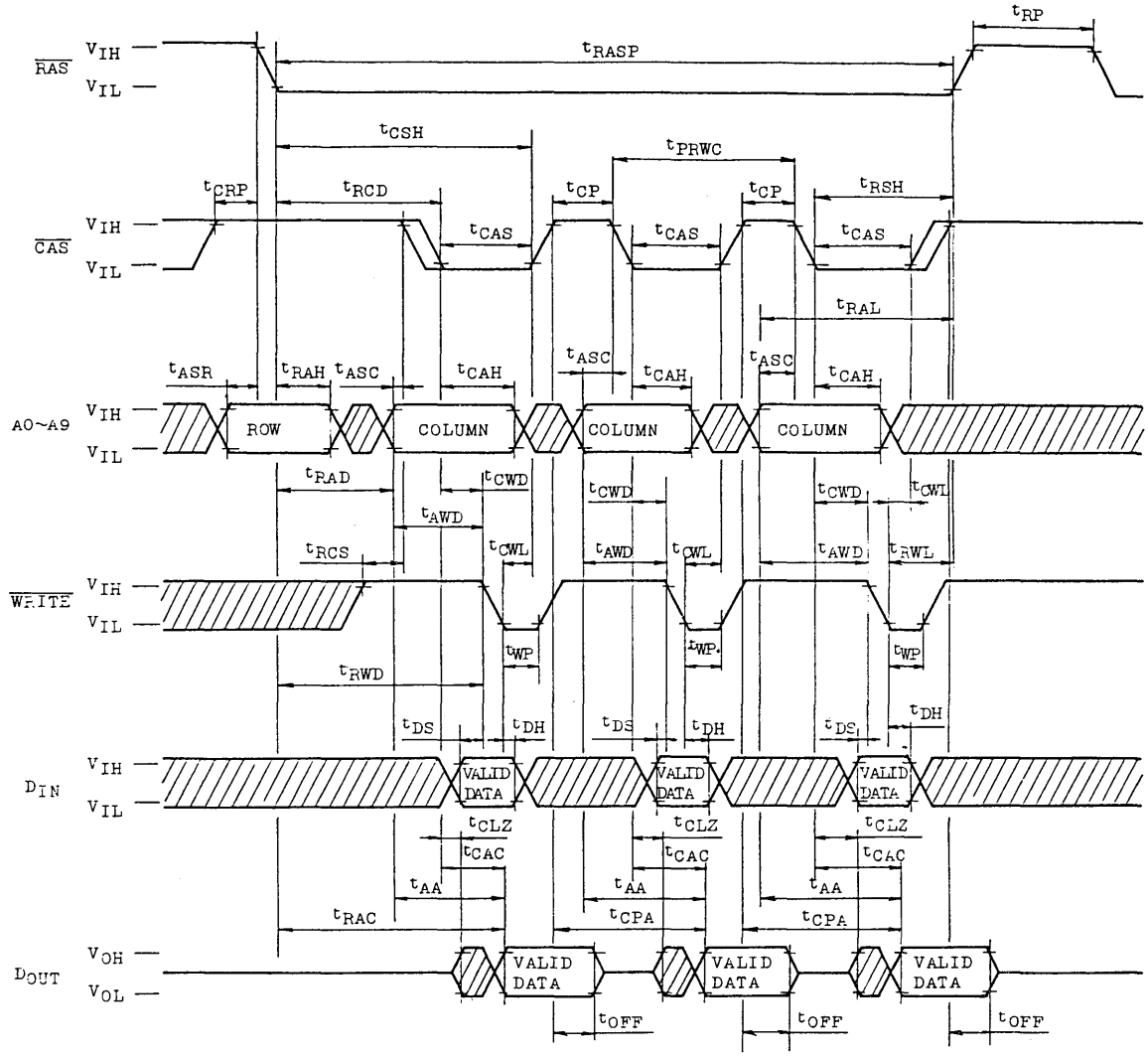
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



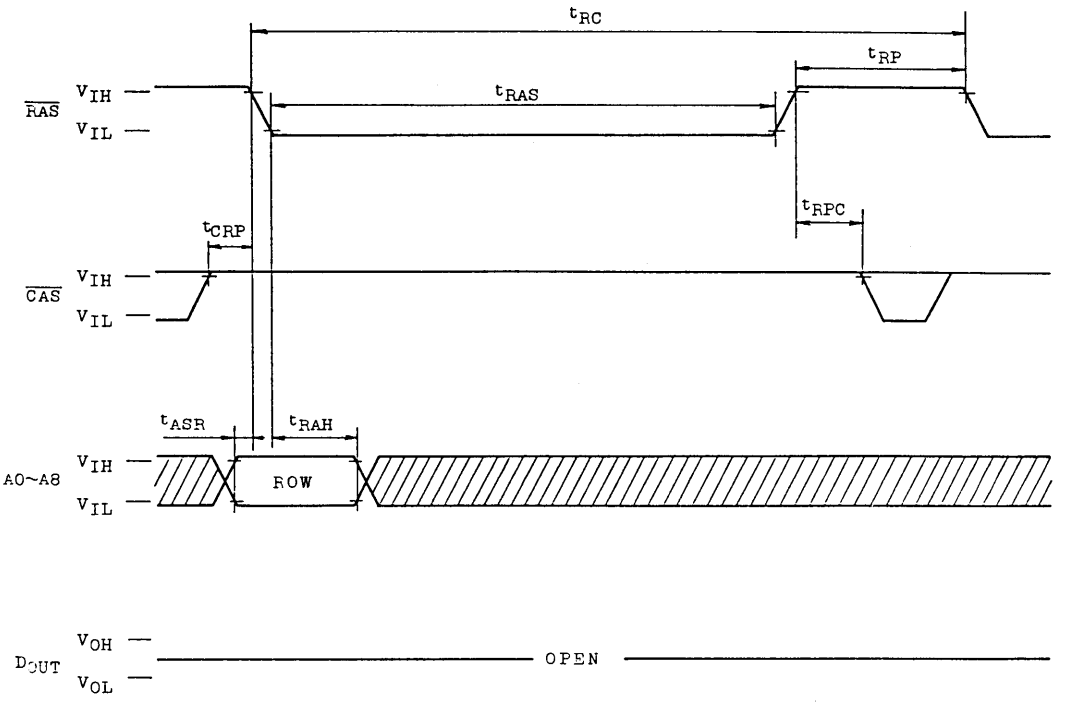
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- FAST PAGE MODE READ-WRITE CYCLE



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- $\overline{RAS}$ ONLY REFRESH CYCLE

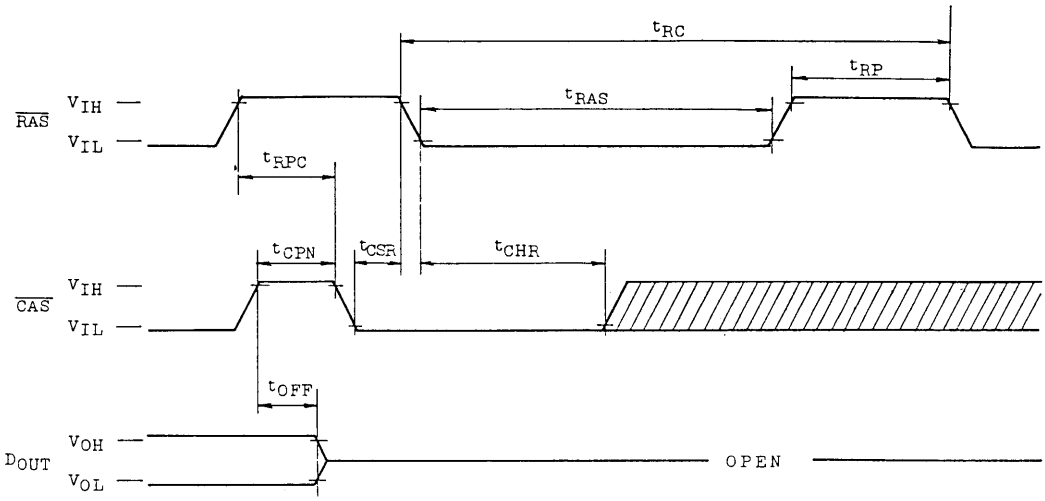


▨ : "H" or "L"

NOTE: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

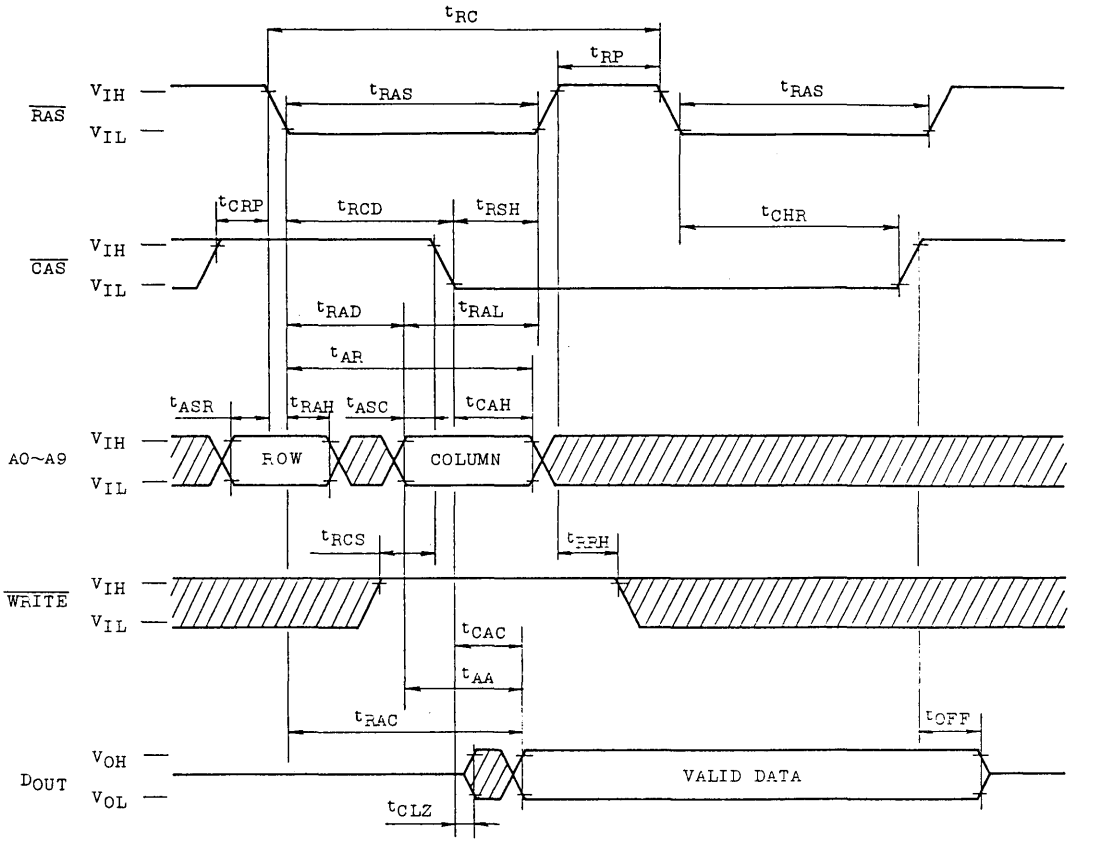


▨: "H" or "L"

NOTE: $\overline{WRITE}$ = "H" or "L", A0 ~ A9 = "H" or "L"

"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

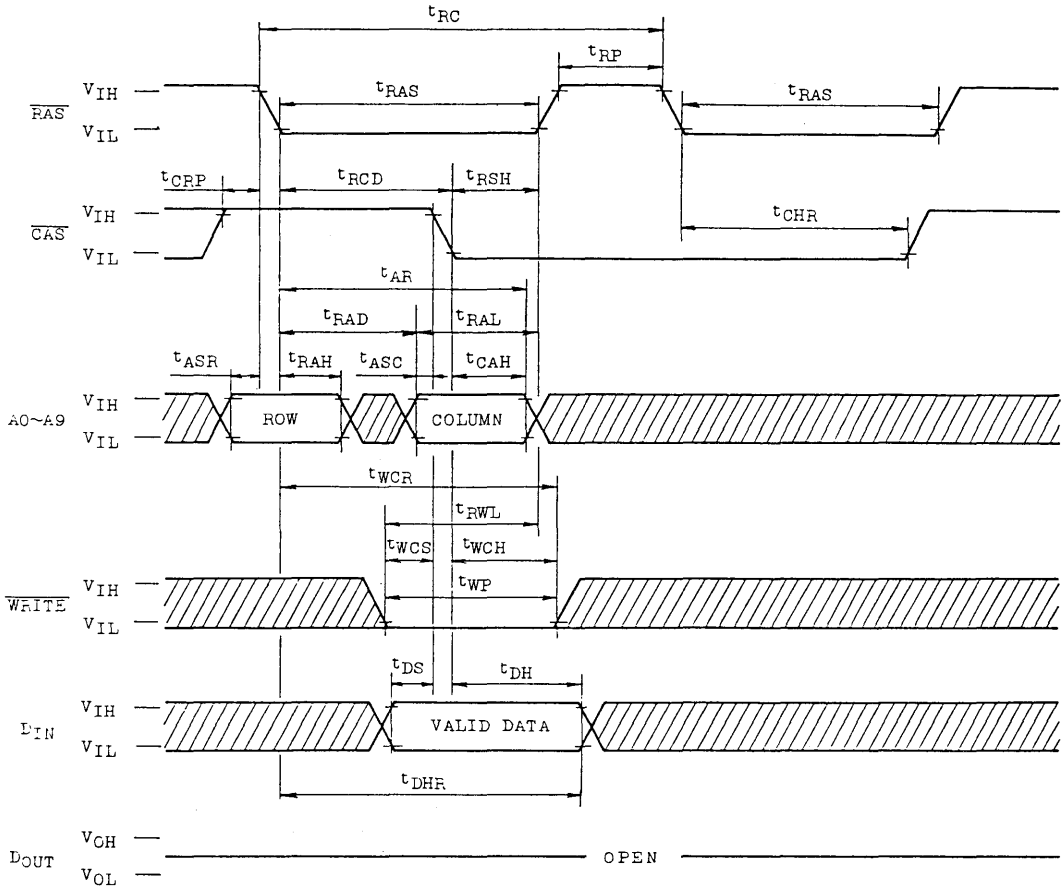
- HIDDEN REFRESH CYCLE (READ)



▨ : "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

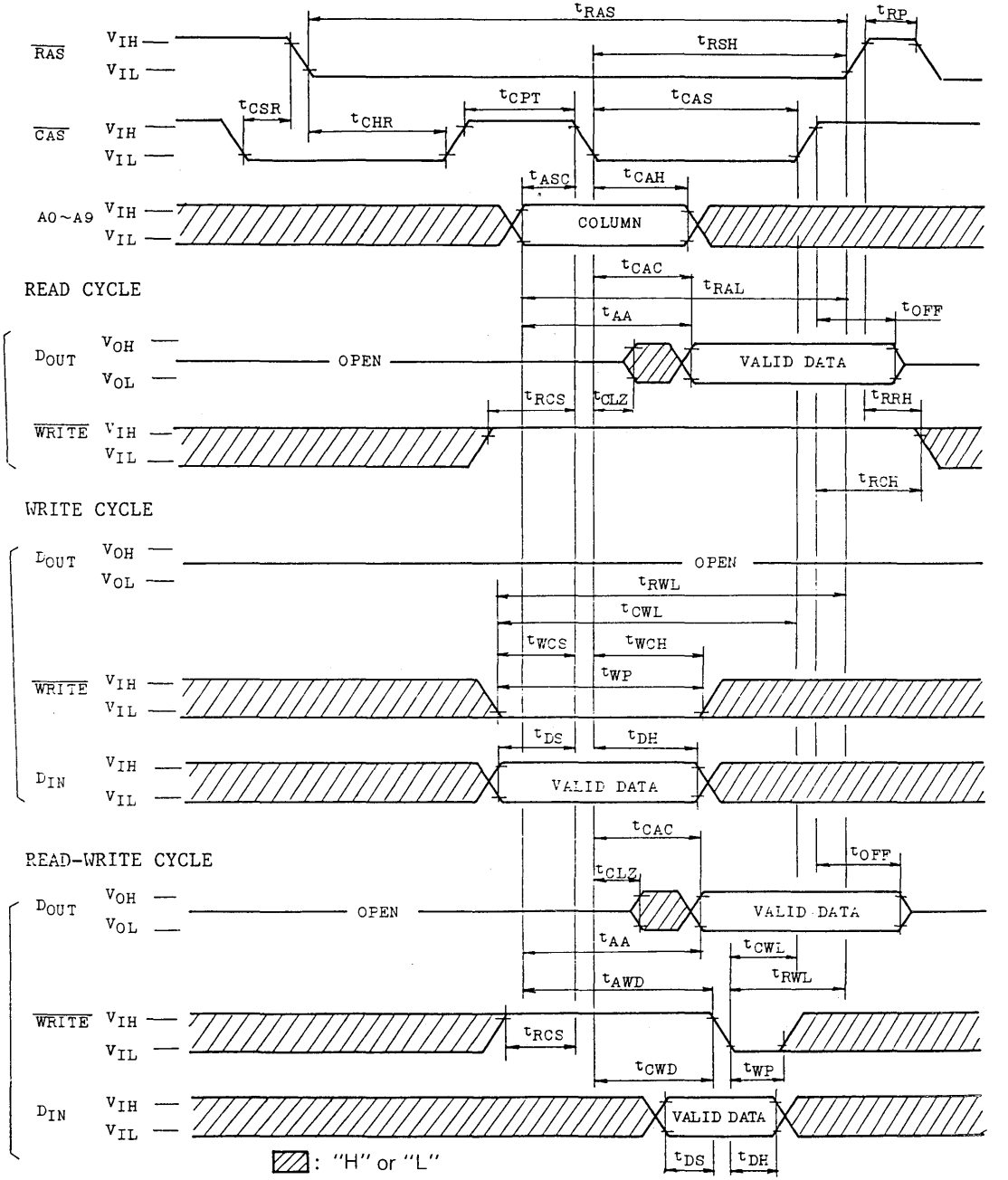
- HIDDEN REFRESH CYCLE (WRITE)



▨ : "H" or "L"

NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

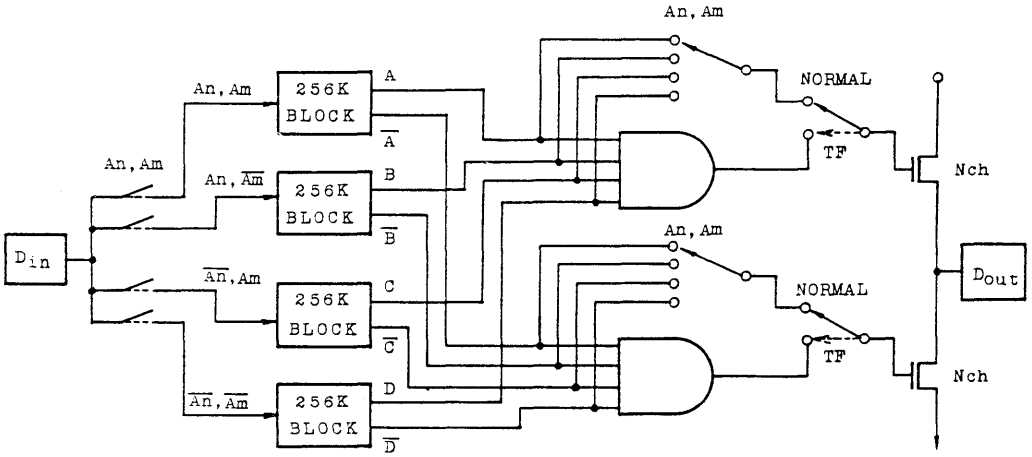
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = Low level or Hi-Z; Normal

Truth Table in Test mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enable by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

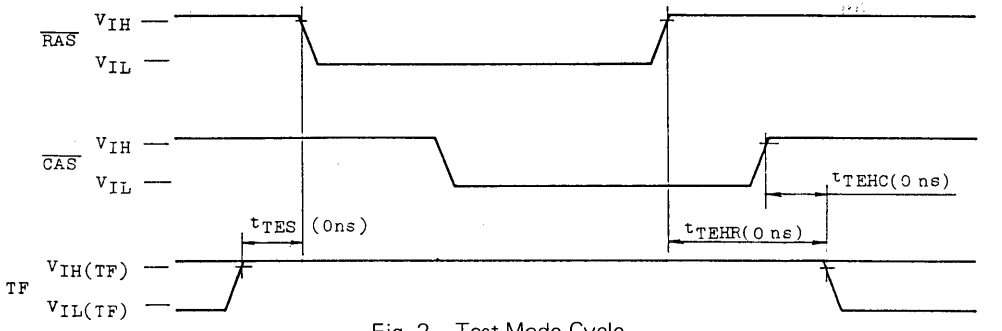
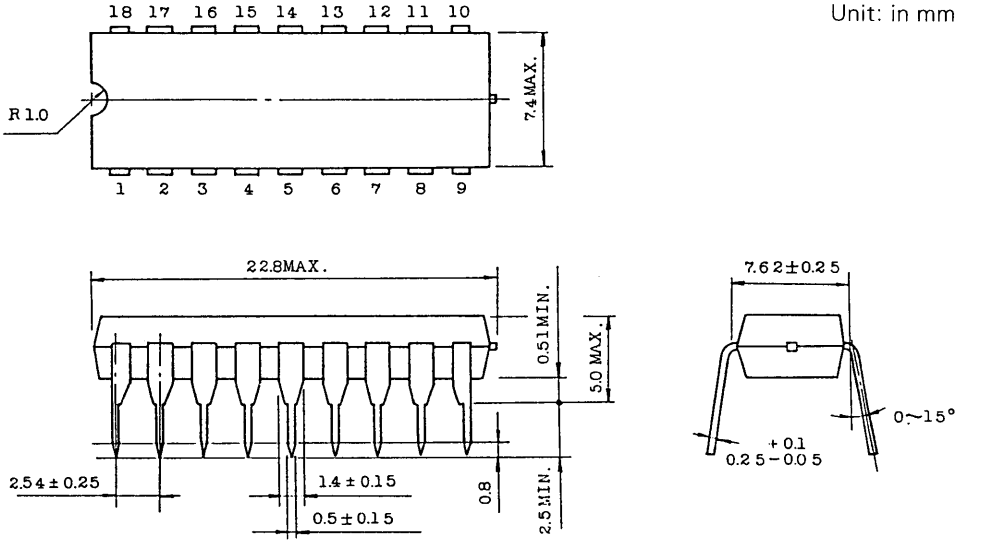


Fig. 2 Test Mode Cycle

OUTLINE DRAWINGS

- Plastic DIP

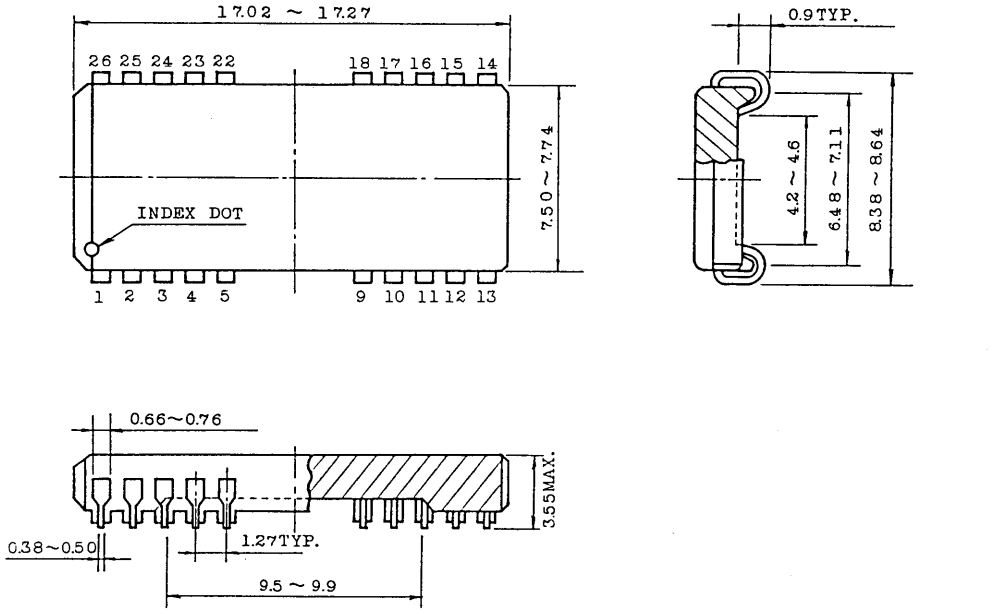
Unit: in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

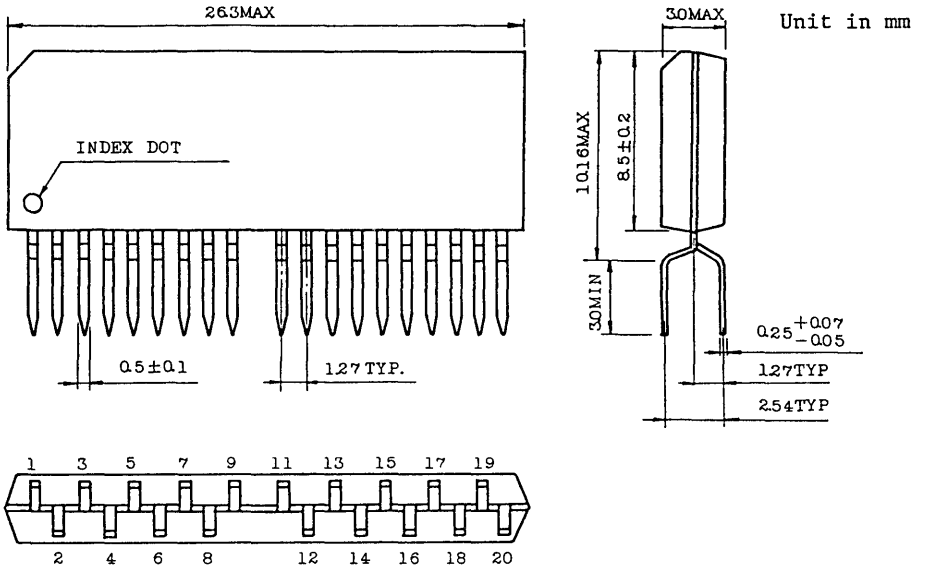
- Plastic SOJ

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

- Plastic ZIP



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORDS×1 BIT DYNAMIC RAM

SILICON GATE CMOS

TC511000PL/JL/ZL-85, TC511000PL/JL/ZL-10
TC511000PL/JL/ZL-12

DESCRIPTION

The TC511000PL/JL/ZL is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000PL/JL/ZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000PL/JL/ZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

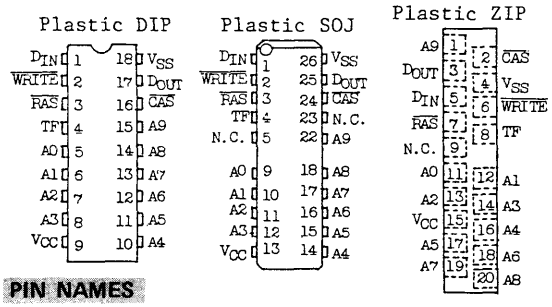
FEATURES

- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000PL/JL/ZL-85/-10/-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating (TC511000PL/JL/ZL-85)
  330mW MAX. Operating (TC511000PL/JL/ZL-10)
  275mW MAX. Operating (TC511000PL/JL/ZL-12)
  1.7mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/64ms
- Package Plastic DIP : TC511000PL
  Plastic SOJ : TC511000JL
  Plastic ZIP : TC511000ZL

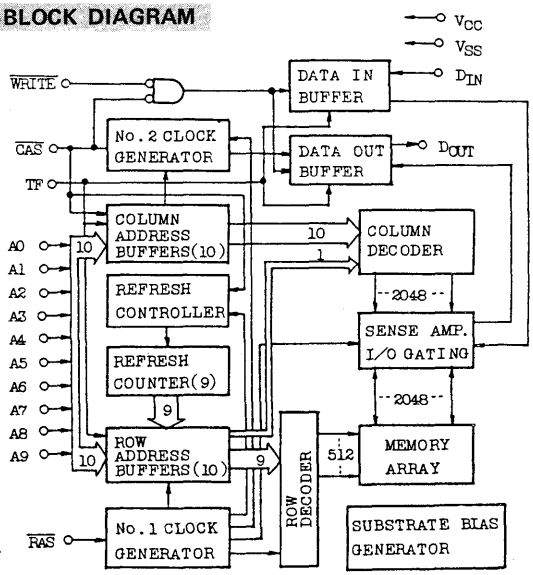
PINCONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	−1 ~ 10.5	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	–	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0	–	V_{CC} +1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511000PL/JL/ZL-85	–	70	mA	3, 4
		TC511000PL/JL/ZL-10	–	60		
		TC511000PL/JL/ZL-12	–	50		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511000PL/JL/ZL-85	–	70	mA	3
		TC511000PL/JL/ZL-10	–	60		
		TC511000PL/JL/ZL-12	–	50		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511000PL/JL/ZL-85	–	50	mA	3, 4
		TC511000PL/JL/ZL-10	–	40		
		TC511000PL/JL/ZL-12	–	30		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		–	300	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511000PL/JL/ZL-85	–	70	mA	3
		TC511000PL/JL/ZL-10	–	60		
		TC511000PL/JL/ZL-12	–	50		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, BATTERY BACK UP MODE $\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC}-0.2V or 0.2V, A0 ~ 9 = V_{CC}-0.2V or 0.2V, D_{IN} = V_{CC}-0.2V, 0.2V or OPEN: t_{RC} = 125μs, t_{RAS} = t_{RAS} MIN. ~ 1μs)		–	300	μA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{out} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511000PL/JL/ZL-85		TC511000PL/JL/ZL-10		TC511000PL/JL/ZL-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RWC}	Read-Write Cycle Time	190	–	220	–	255	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	70	–	ns	
t_{PRWC}	Fast Page Mode Read-Write Cycle Time	75	–	85	–	105	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	9, 14
t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	9, 14
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	9, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	65	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	–	5	–	5	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	20	–	20	–	25	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	64	–	64	–	64	ms	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000PL/JL/ZL-85		TC511000PL/JL/ZL-10		TC511000PL/JL/ZL-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	25	–	25	–	30	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	–	100	–	120	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

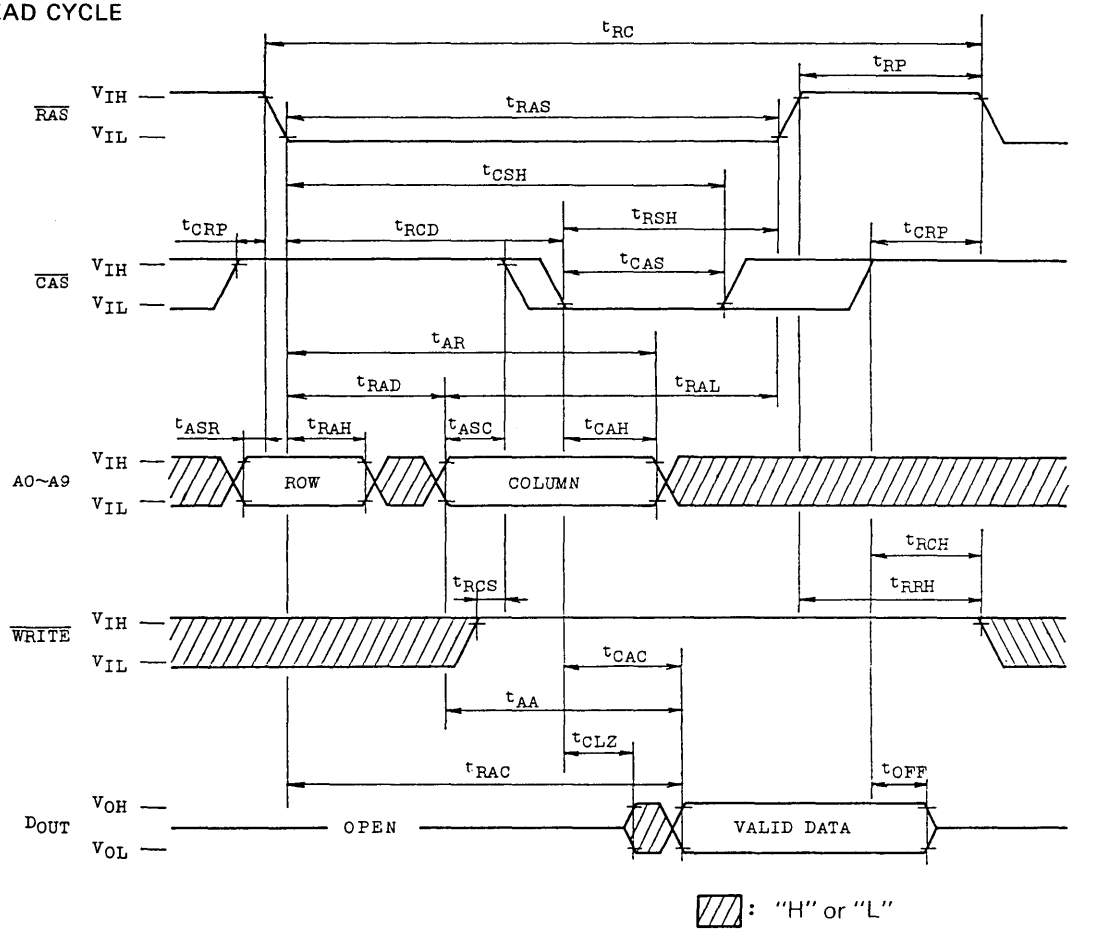
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_9$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	pF
Co	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. t_{RAS}(max.) = 1μs is only applied to refresh of battery-back up. t_{RAS}(max.) = 10μs is applied to functional operating.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume t_T= 5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

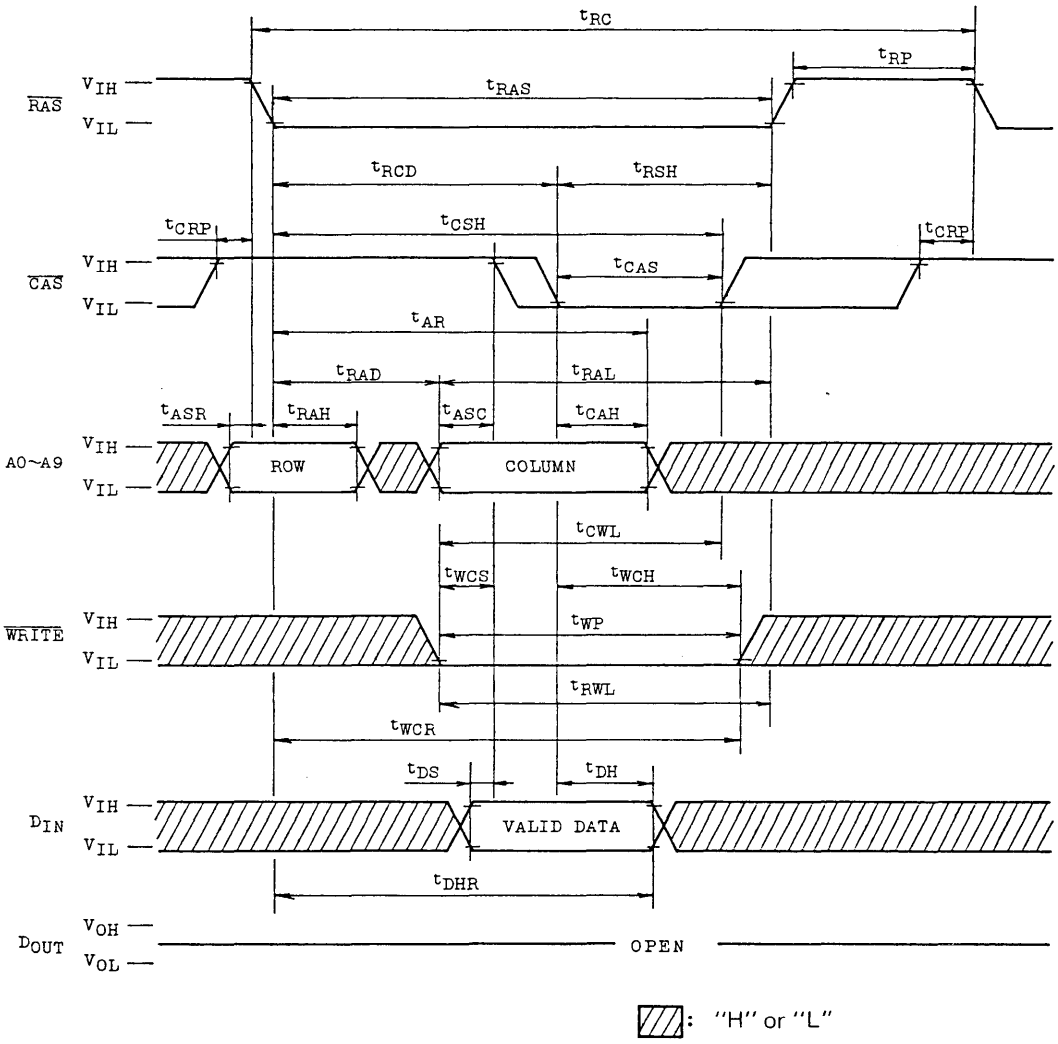
TIMING WAVEFORMS

- READ CYCLE



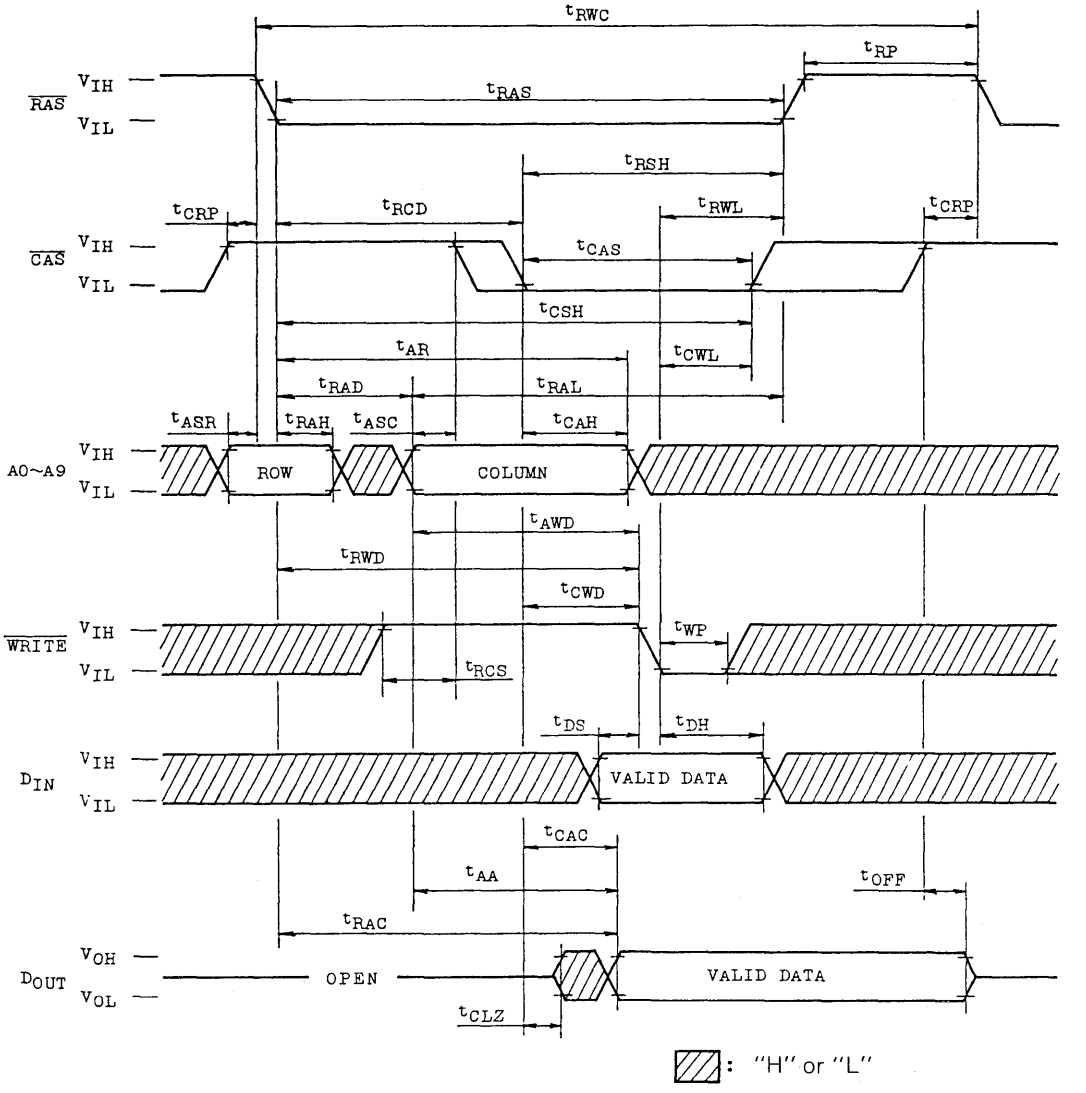
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- WRITE CYCLE (EARLY WRITE)



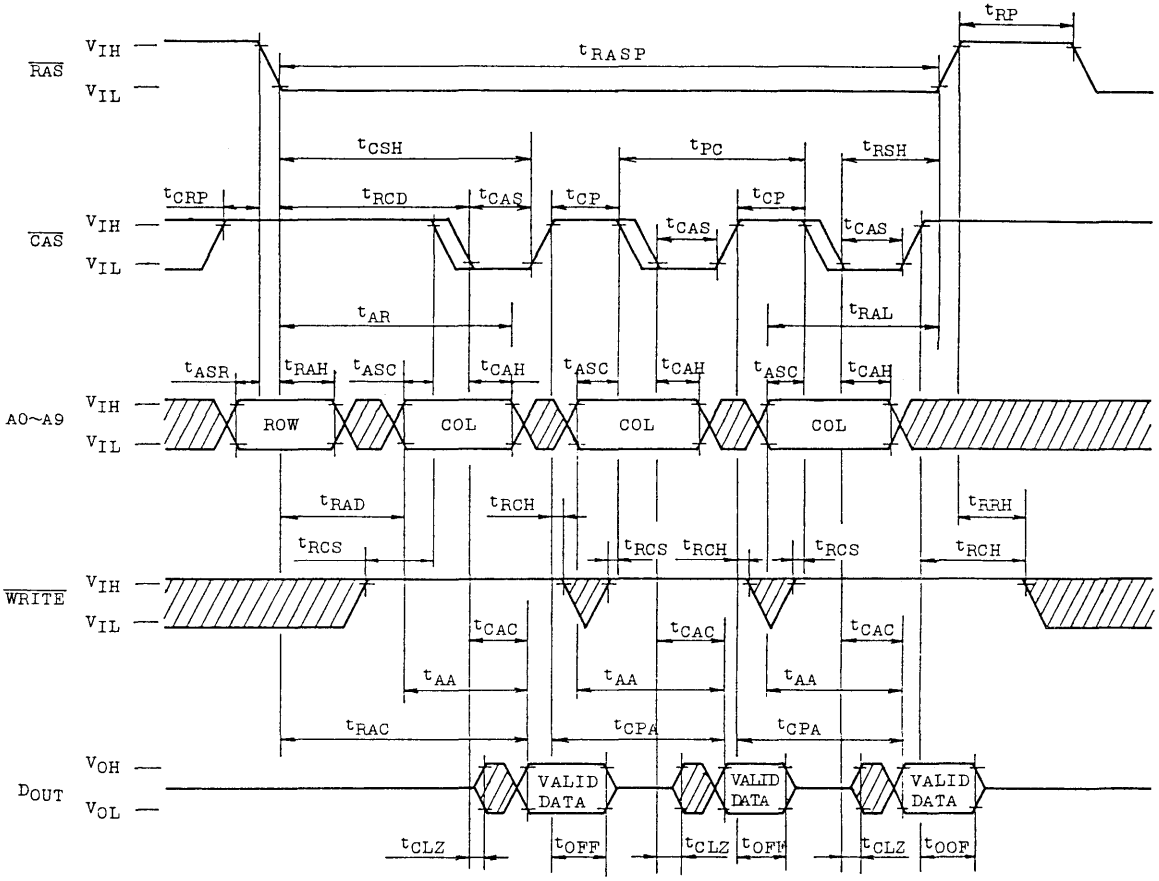
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- READ-WRITE CYCLE



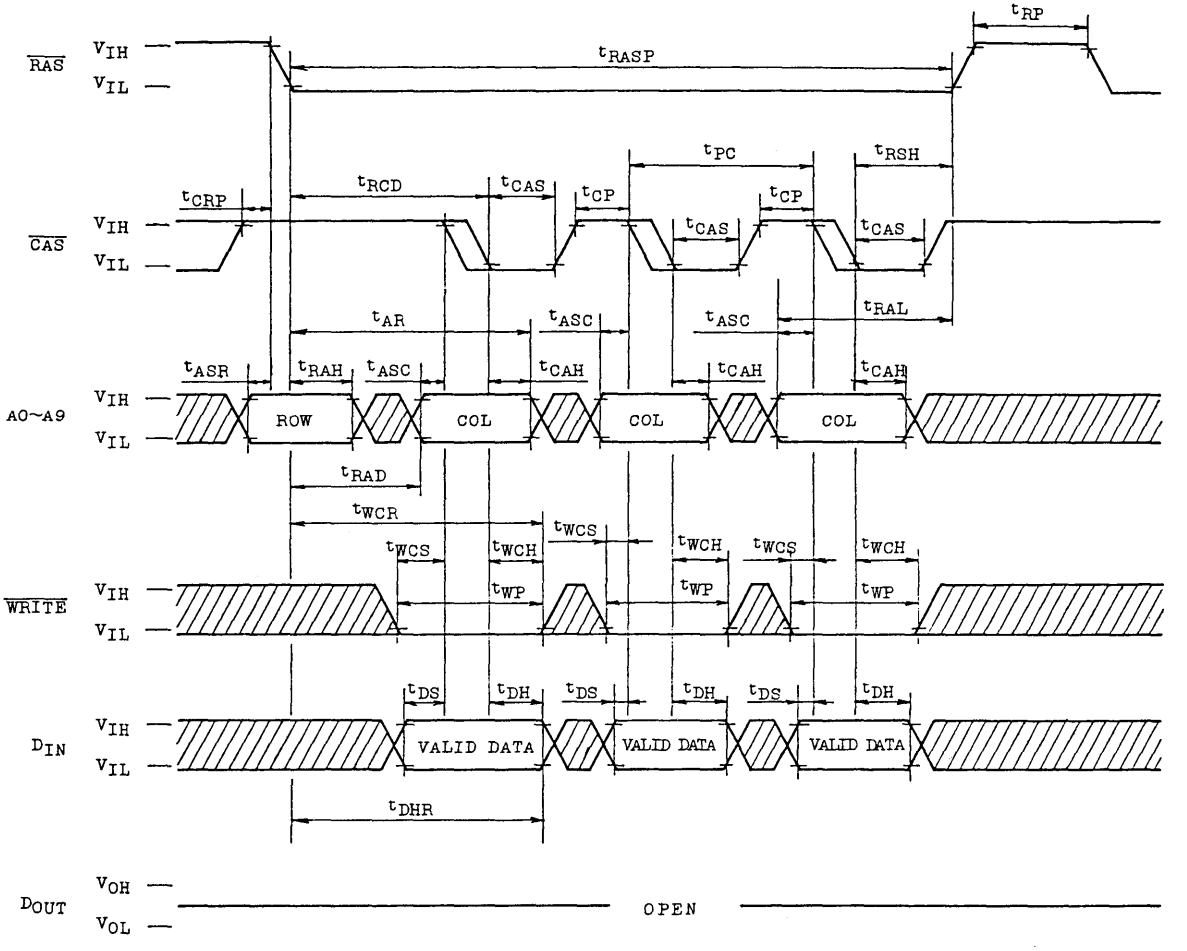
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- **FAST PAGE MODE READ CYCLE**



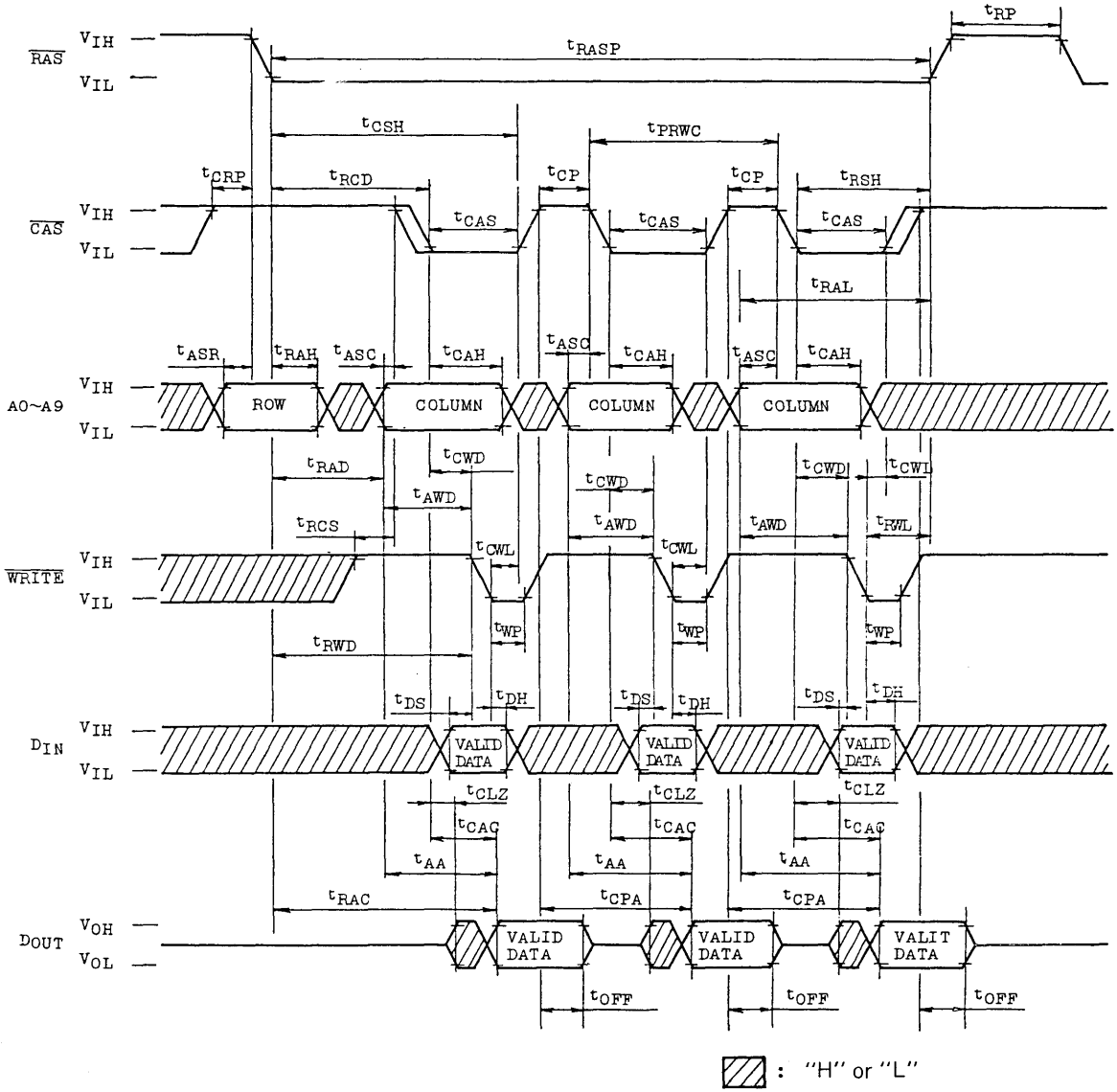
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



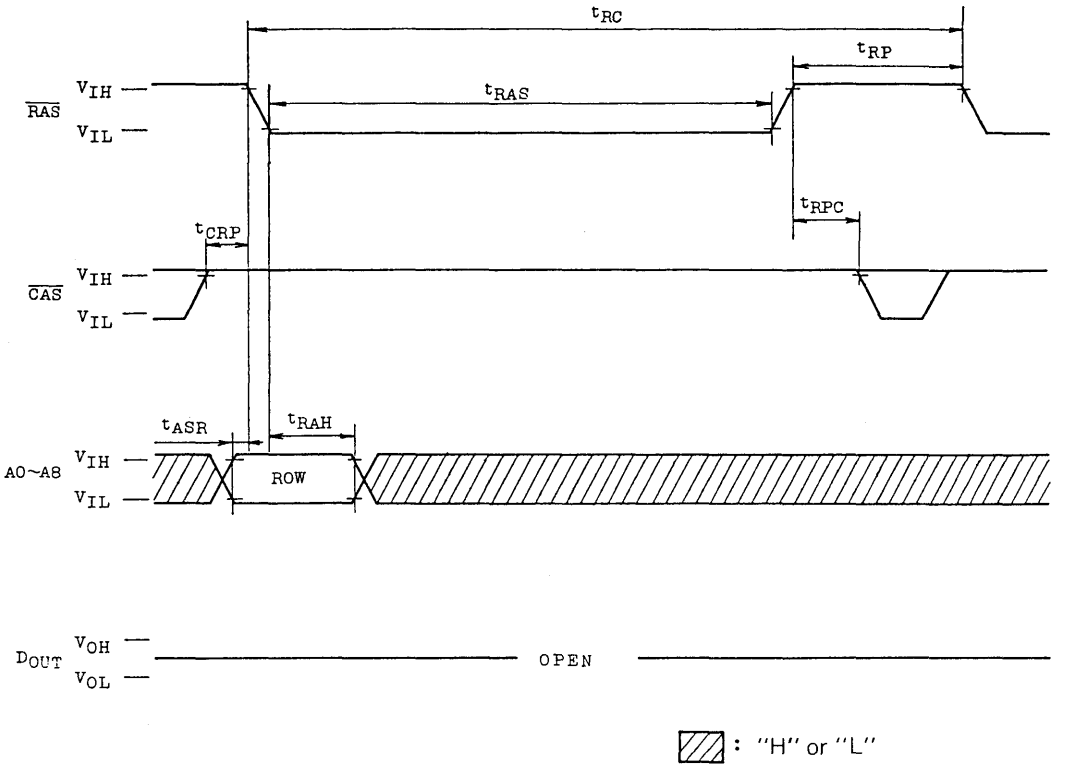
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- FAST PAGE MODE READ-WRITE CYCLE



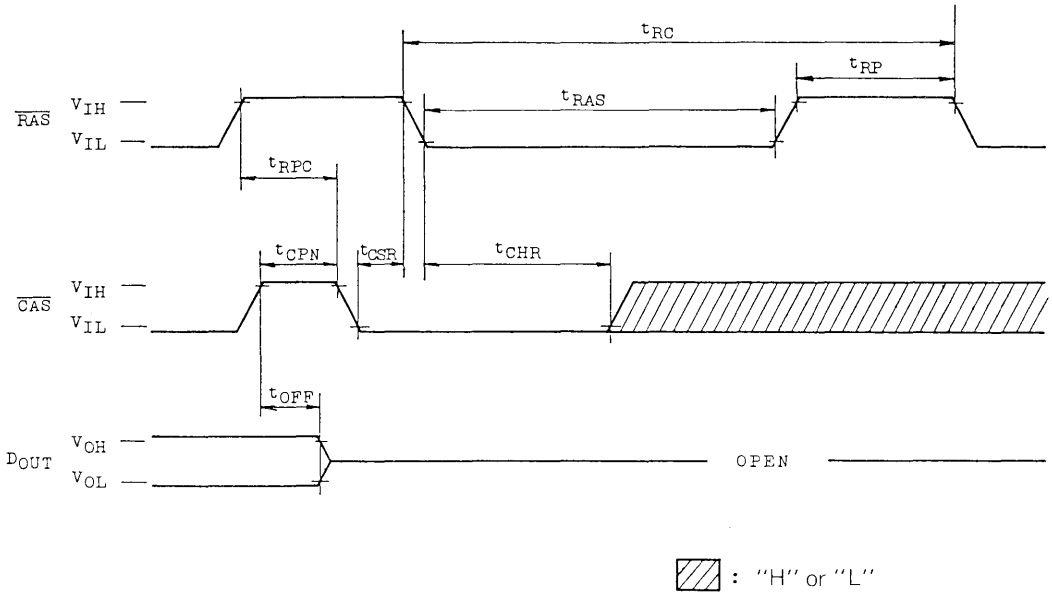
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- $\overline{RAS}$ ONLY REFRESH CYCLE



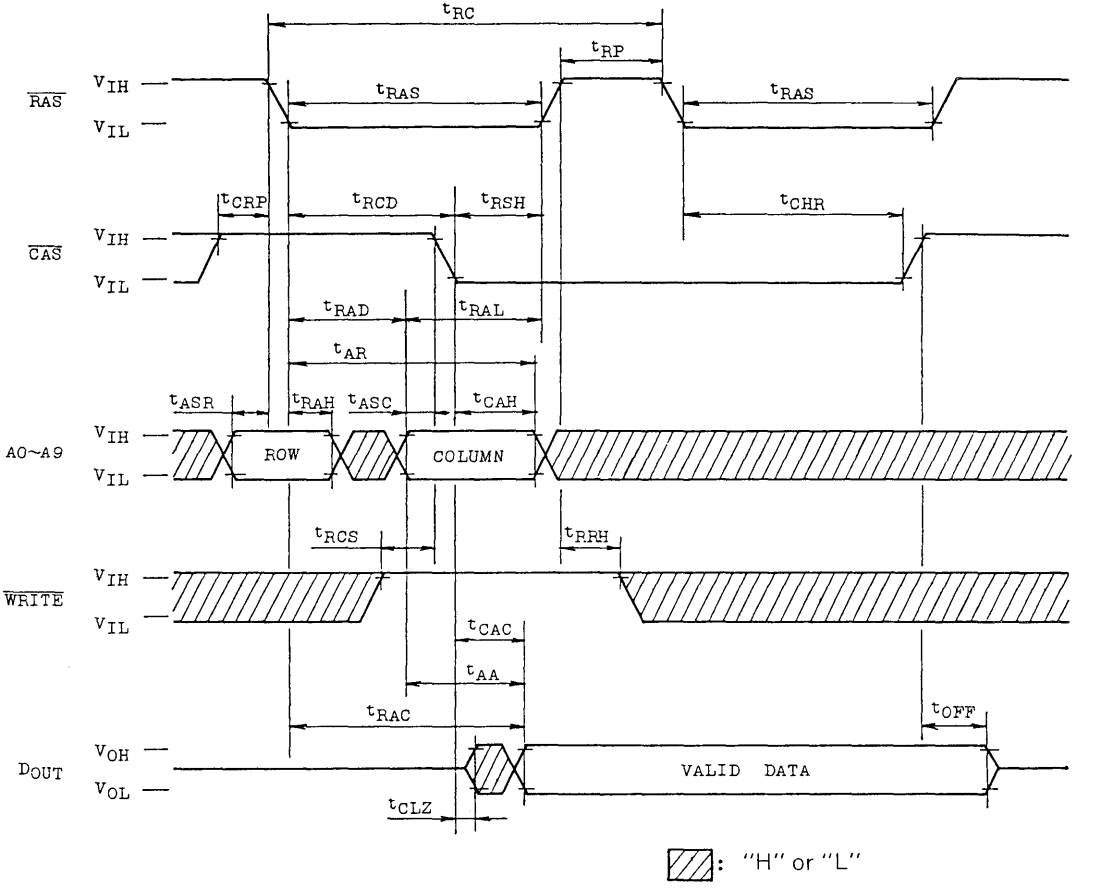
NOTE: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\ (TF)}$ level or open, if "Test Mode" is not used.

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



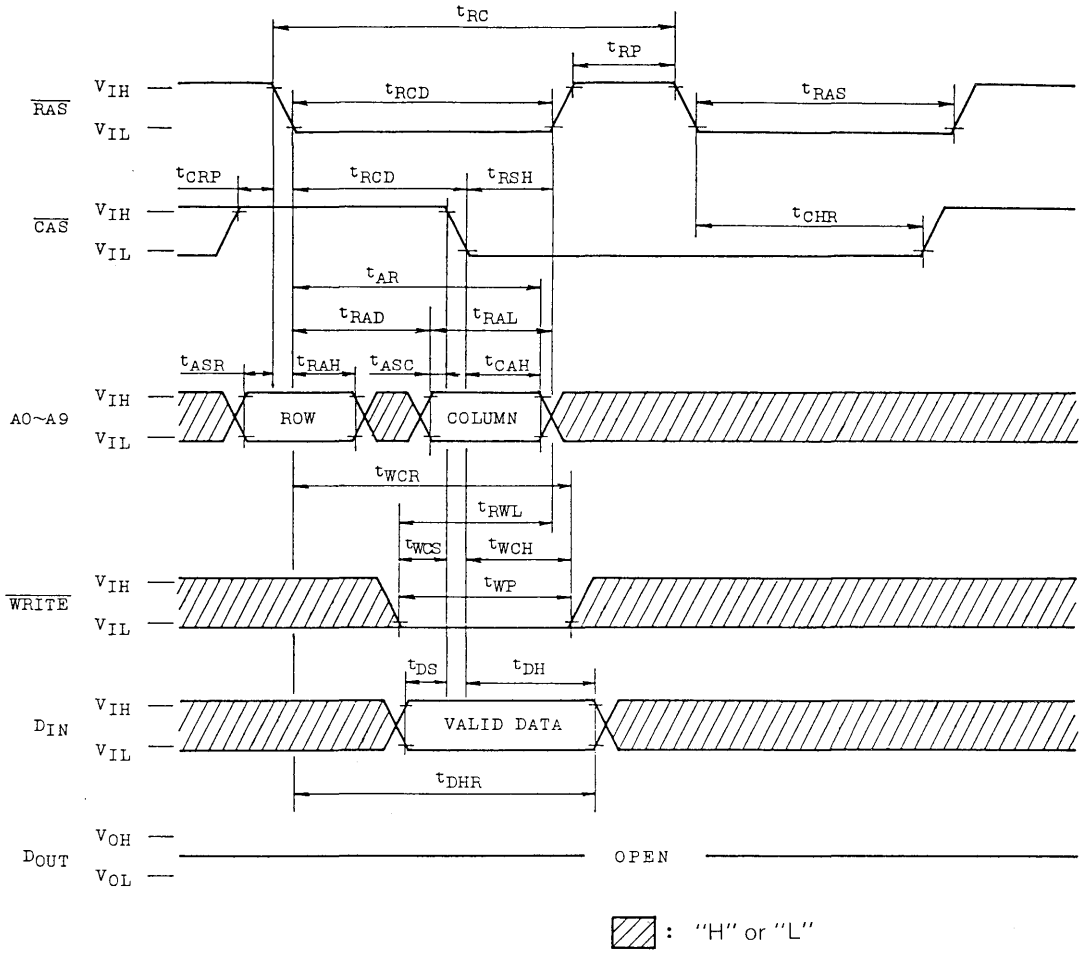
NOTE: $\overline{WRITE}$ = "H" or "L", A0 ~ A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- HIDDEN REFRESH CYCLE (READ)



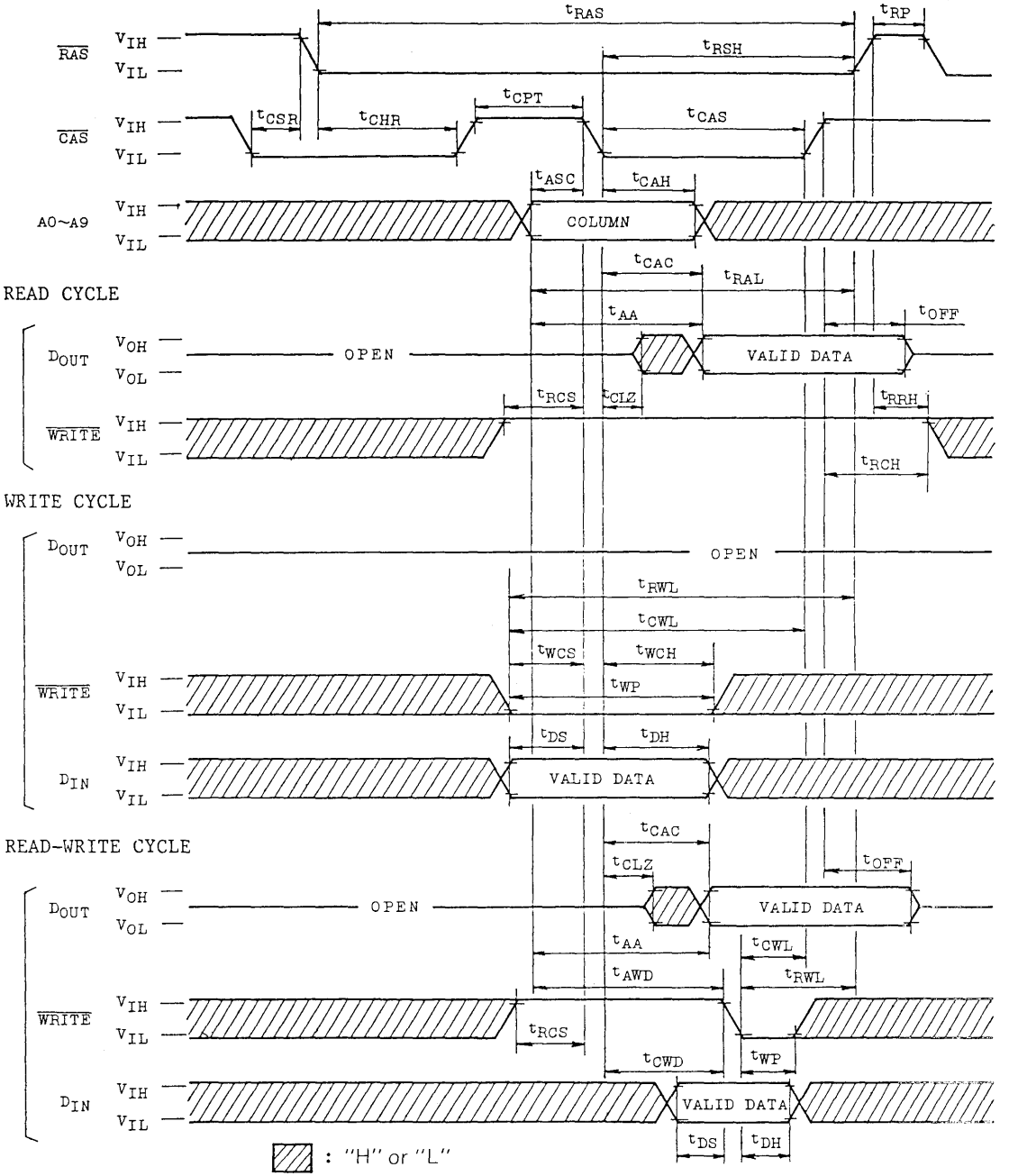
NOTE: "TF" pin should be connected to $V_{IL\ (TF)}$ level or open, if "Test Mode" is not used.

- HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to $V_{IL\ (TF)}$ level or open, if "Test Mode" is not used.

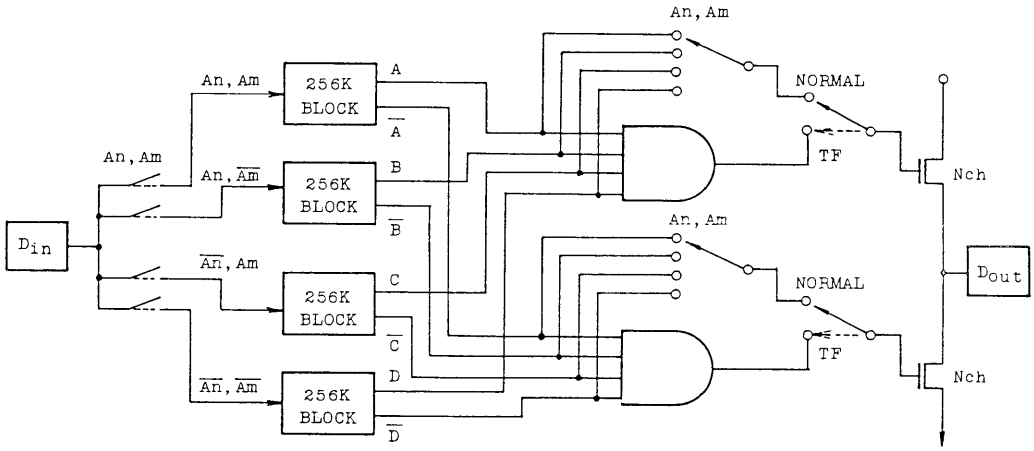
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = $V_{IL(TF)}$ level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enable by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

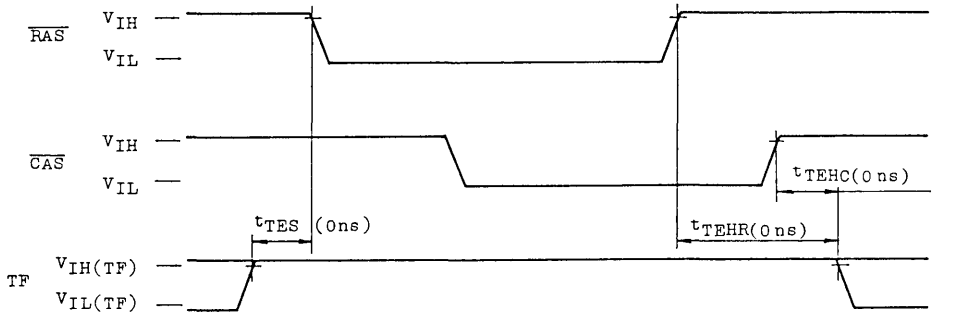
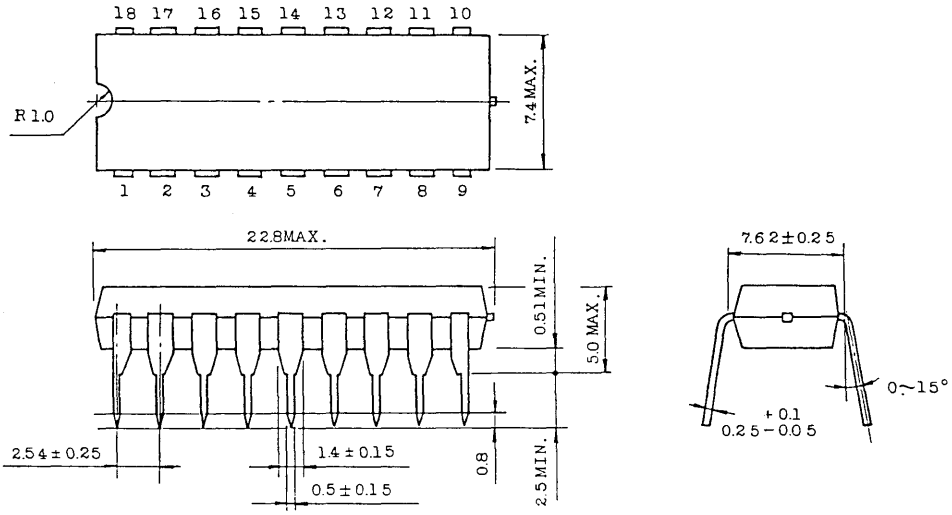


Fig. 2 Test Mode Cycle

OUTLINE DRAWINGS

- Plastic DIP

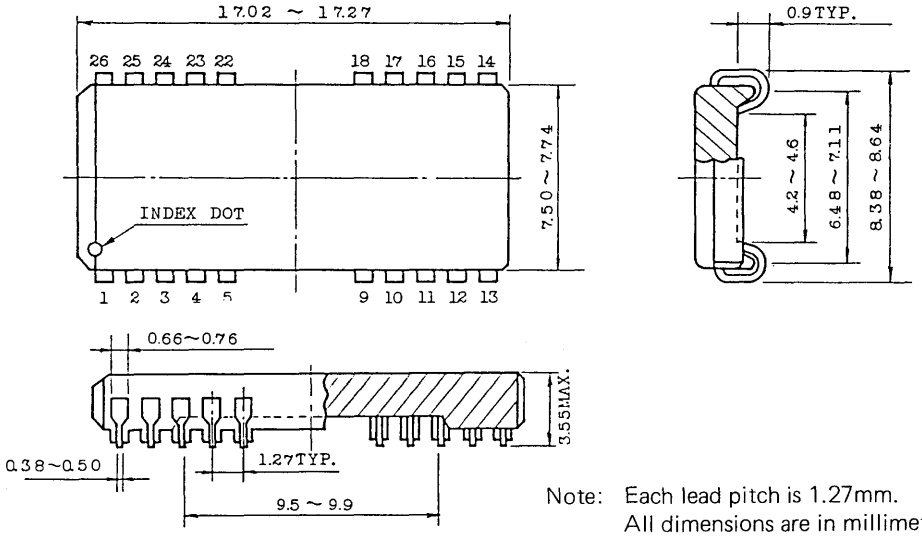
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

- Plastic SOJ

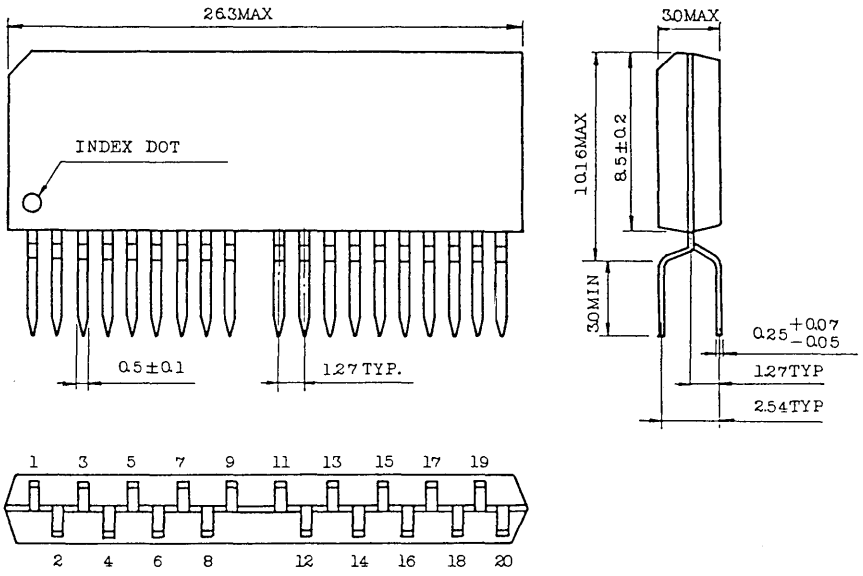
Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

- Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC511000AP/AJ/AZ-70, TC511000AP/AJ/AZ-80 TC511000AP/AJ/AZ-10

DESCRIPTION

The TC511000AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

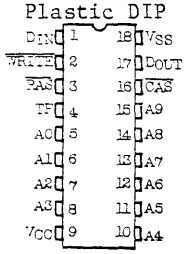
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000AP/AJ/AZ-70/80/10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

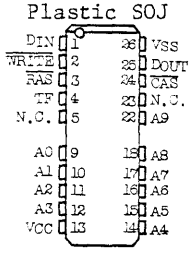
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  440mW MAX. Operating(TC511000AP/AJ/AZ-70)
  385mW MAX. Operating(TC511000AP/AJ/AZ-80)
  330mW MAX. Operating(TC511000AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511000AP
  Plastic SOJ: TC511000AJ
  Plastic ZIP: TC511000AZ

PIN CONNECTION

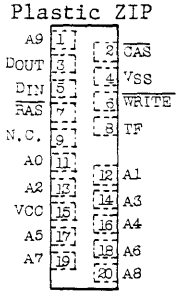
Plastic DIP



Plastic SOJ



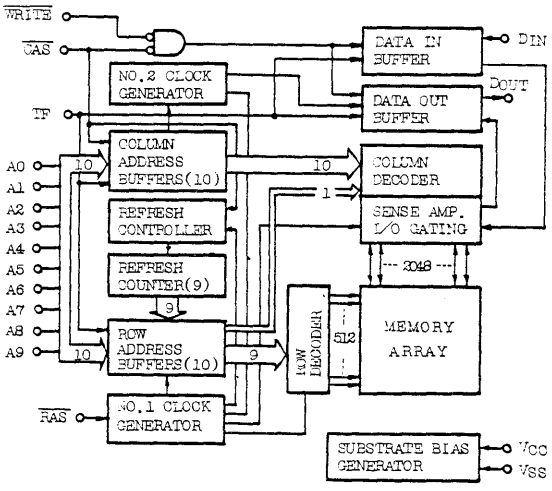
Plastic ZIP



PIN NAMES

A0 ∿ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	-1.0	-	V_{CC}+1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511000AP/AJ/AZ-70	-	80	mA	3,4
		TC511000AP/AJ/AZ-80	-	70		
		TC511000AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511000AP/AJ/AZ-70	-	80	mA	3
		TC511000AP/AJ/AZ-80	-	70		
		TC511000AP/AJ/AZ-10	-	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fas Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycleing: t_{PC}=t_{PC} MIN.)	TC511000AP/AJ/AZ-70	-	60	mA	3,4
		TC511000AP/AJ/AZ-80	-	50		
		TC511000AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycleing: t_{RC}=t_{RC} MIN.)	TC511000AP/AJ/AZ-70	-	80	mA	3
		TC511000AP/AJ/AZ-80	-	70		
		TC511000AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ V_{CC}+0.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511000AP/AJ/AZ-70		TC511000AP/AJ/AZ-80		TC511000AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RWC}	Read-Write Cycle Time	155	-	175	-	210	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{PRWC}	Fast Page Mode Read-Write Cycle Time	65	-	70	-	85	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511000AP/AJ/AZ-70		TC511000AP/AJ/AZ-80		TC511000AP/AJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	25	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	-	80	-	100	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	-	40	-	50	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

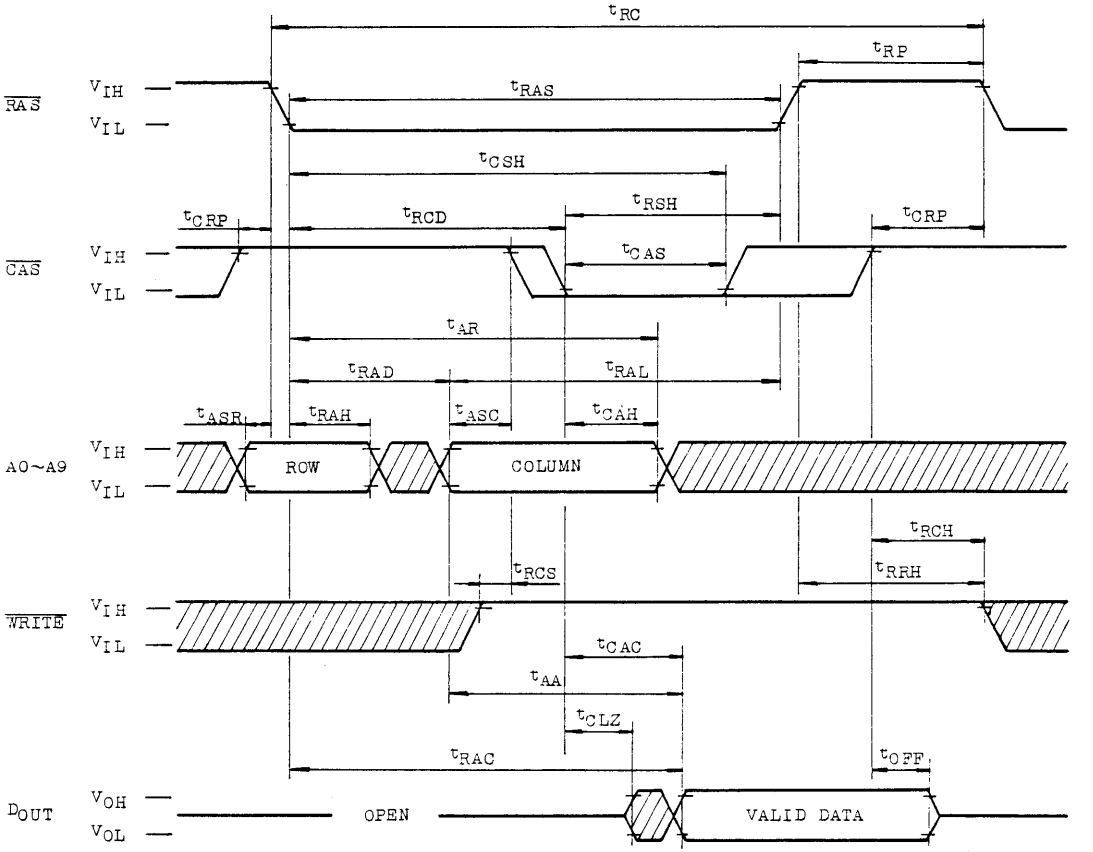
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early wirte cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

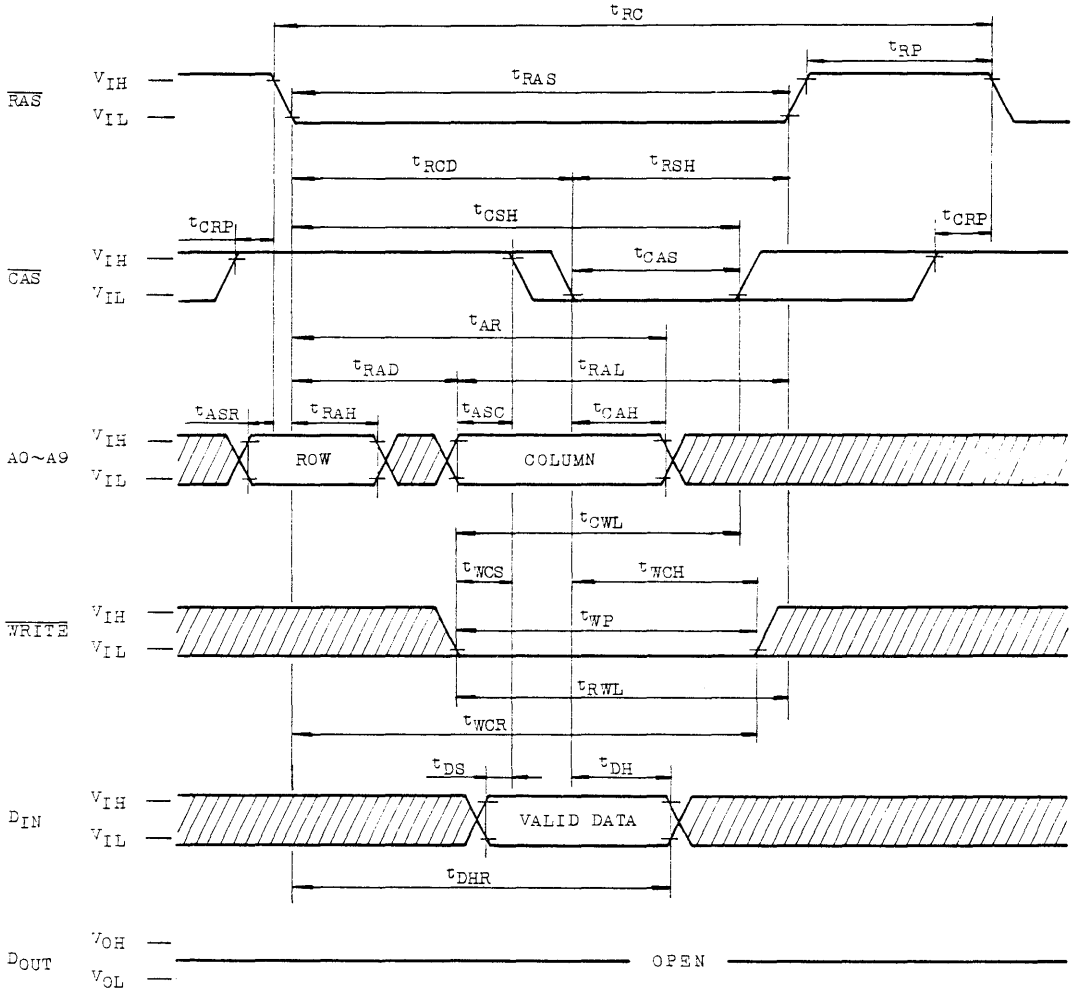
READ CYCLE



▨: "H" or "L"

NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

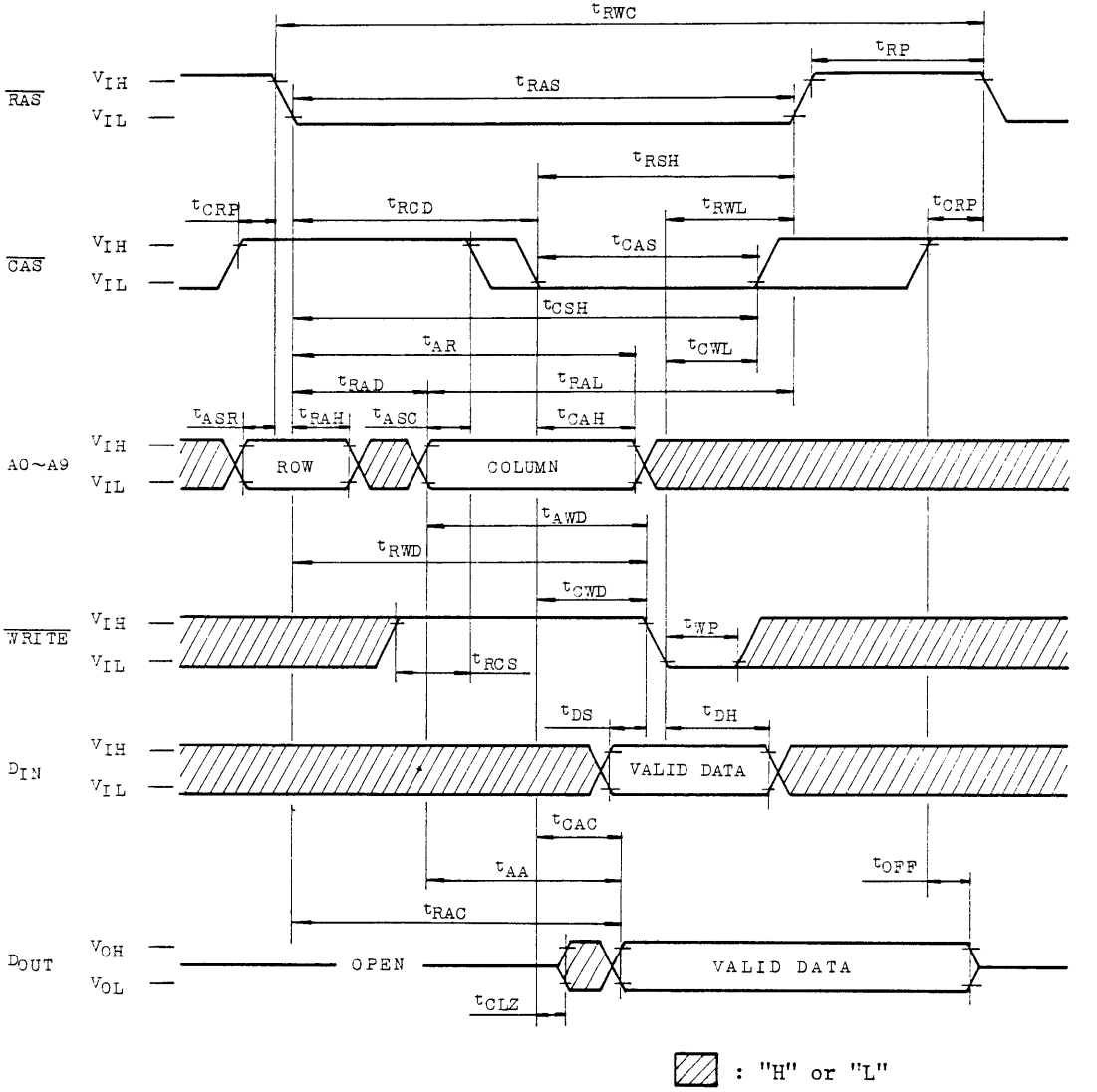
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

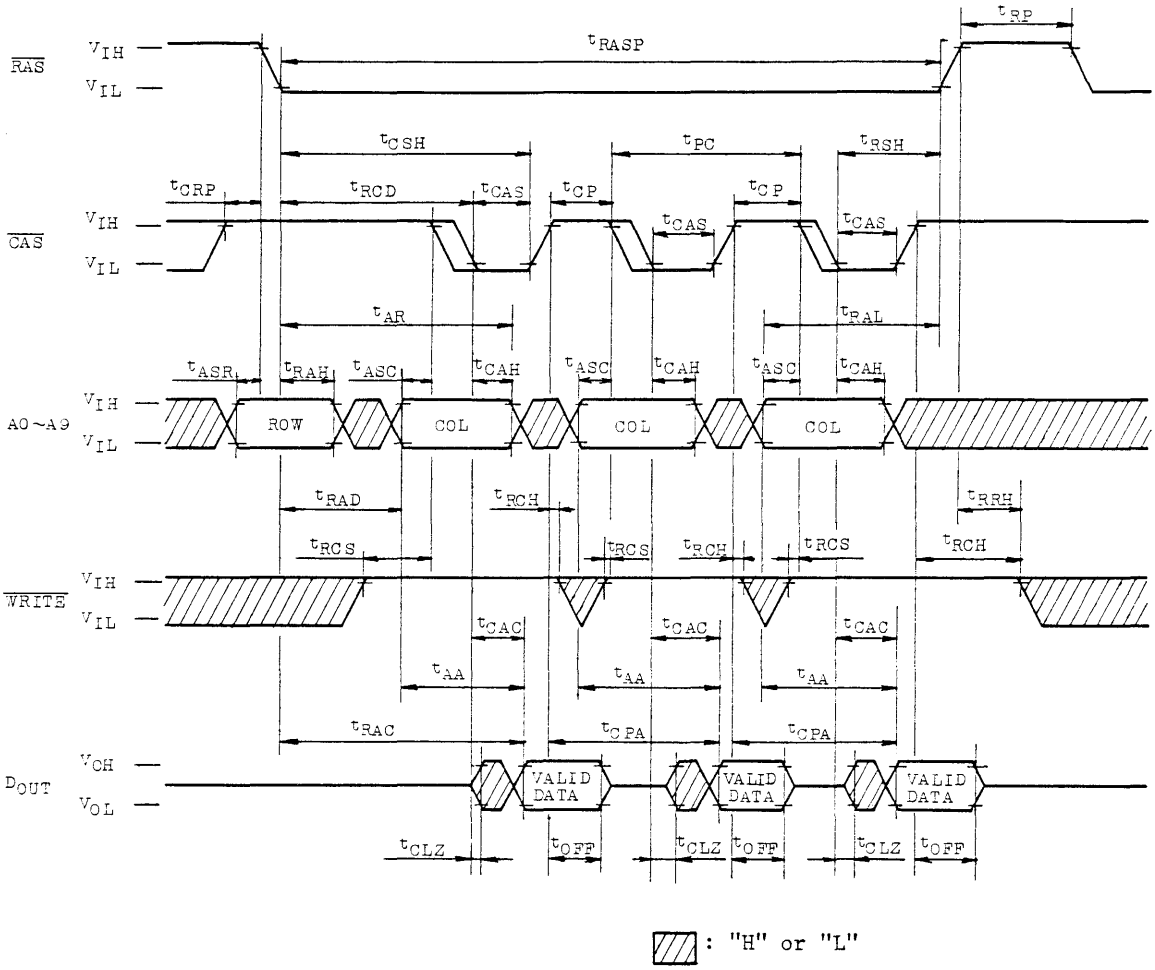
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

READ-WRITE CYCLE



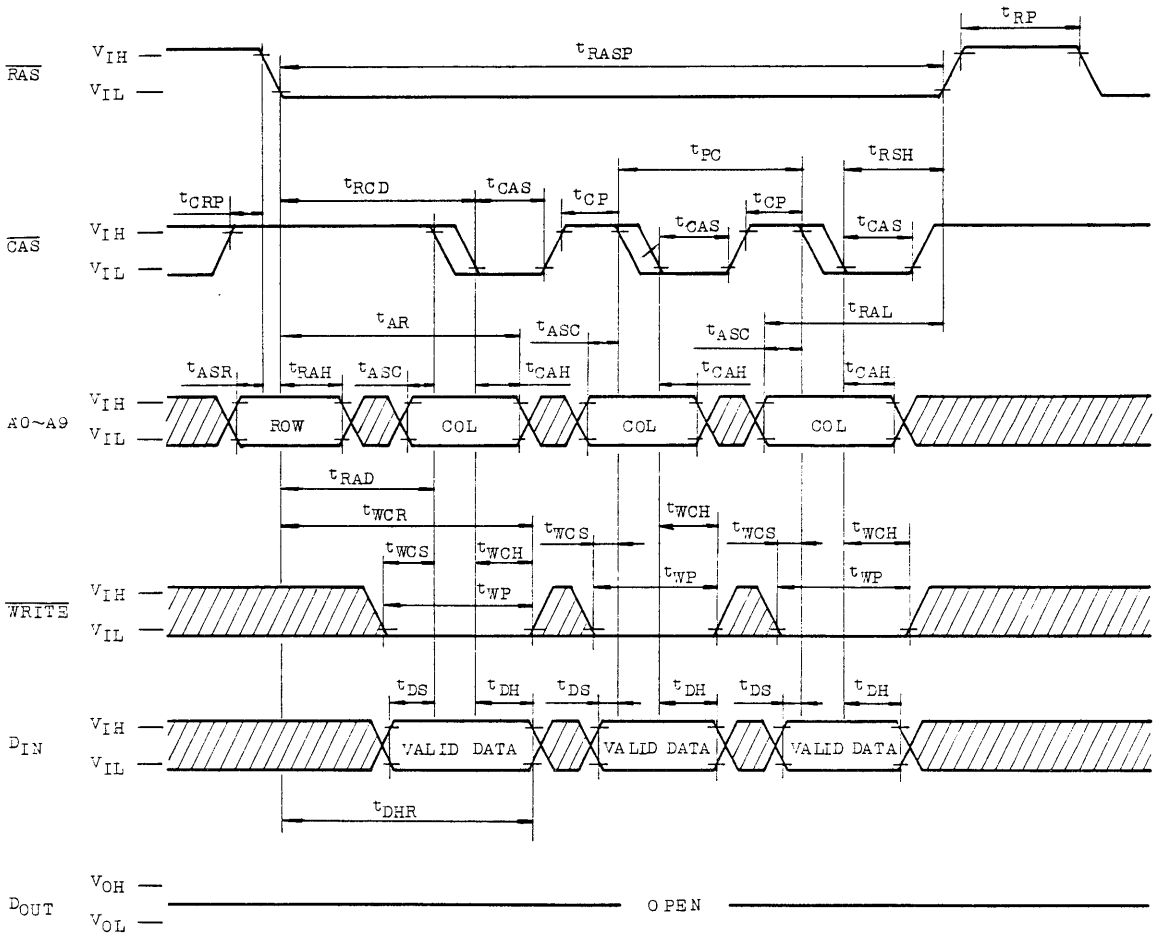
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



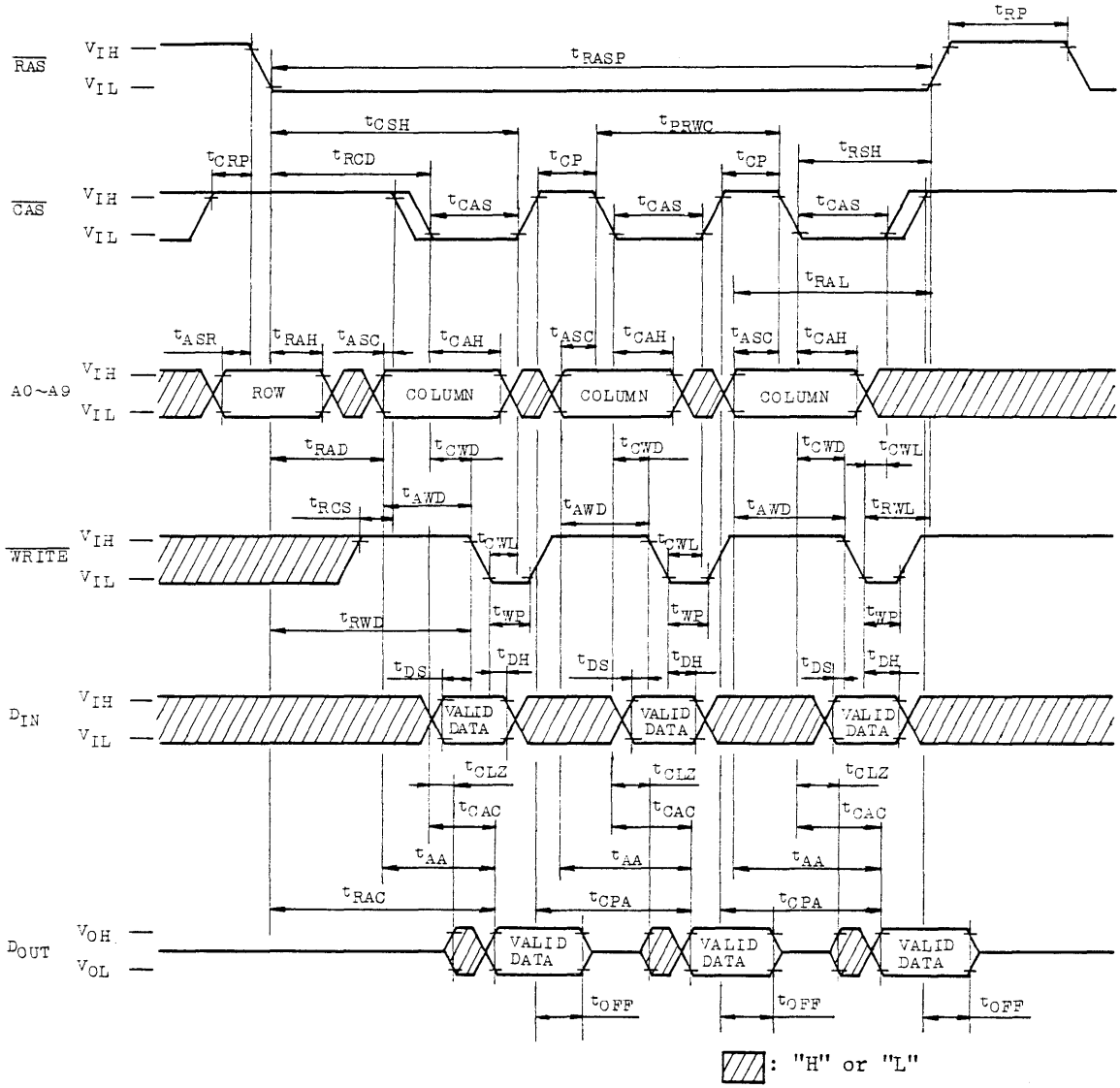
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



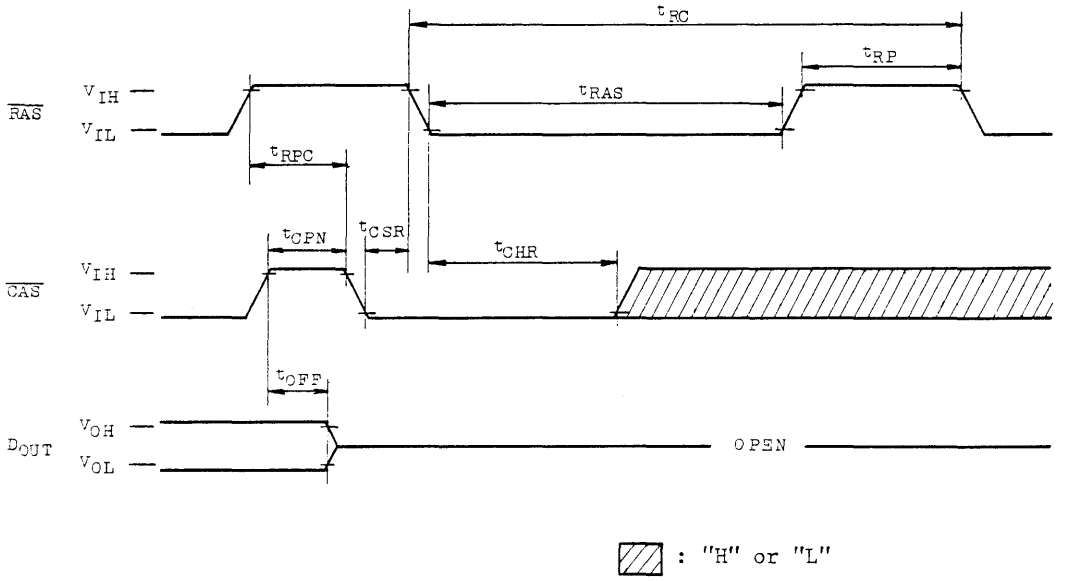
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-WRITE CYCLE



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

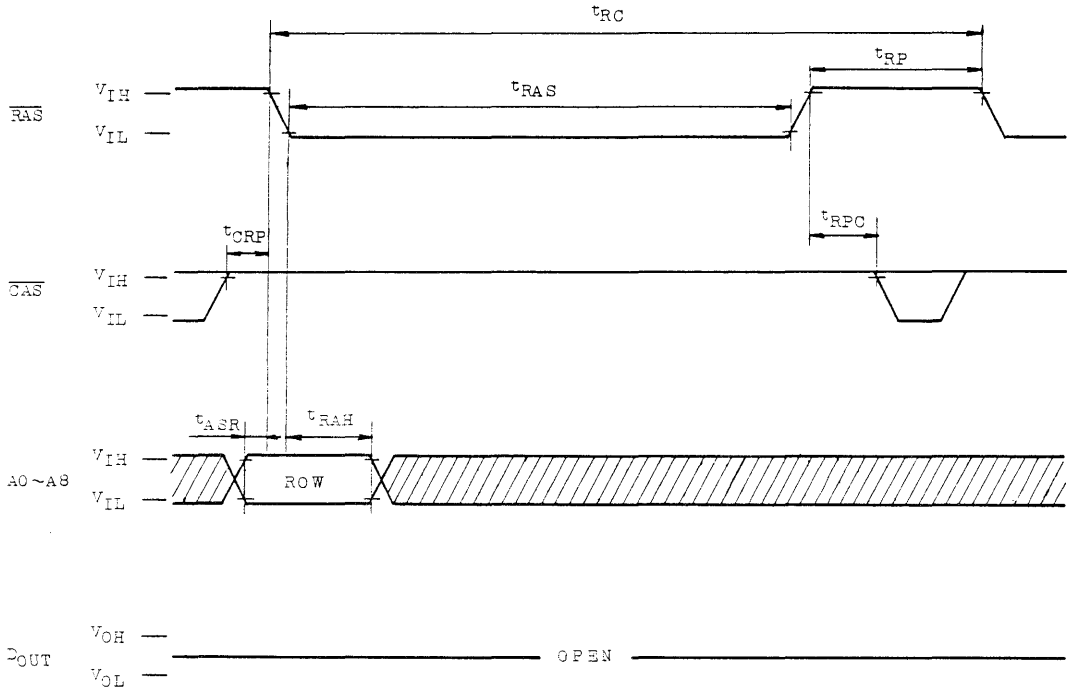


▨ : "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

"TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE

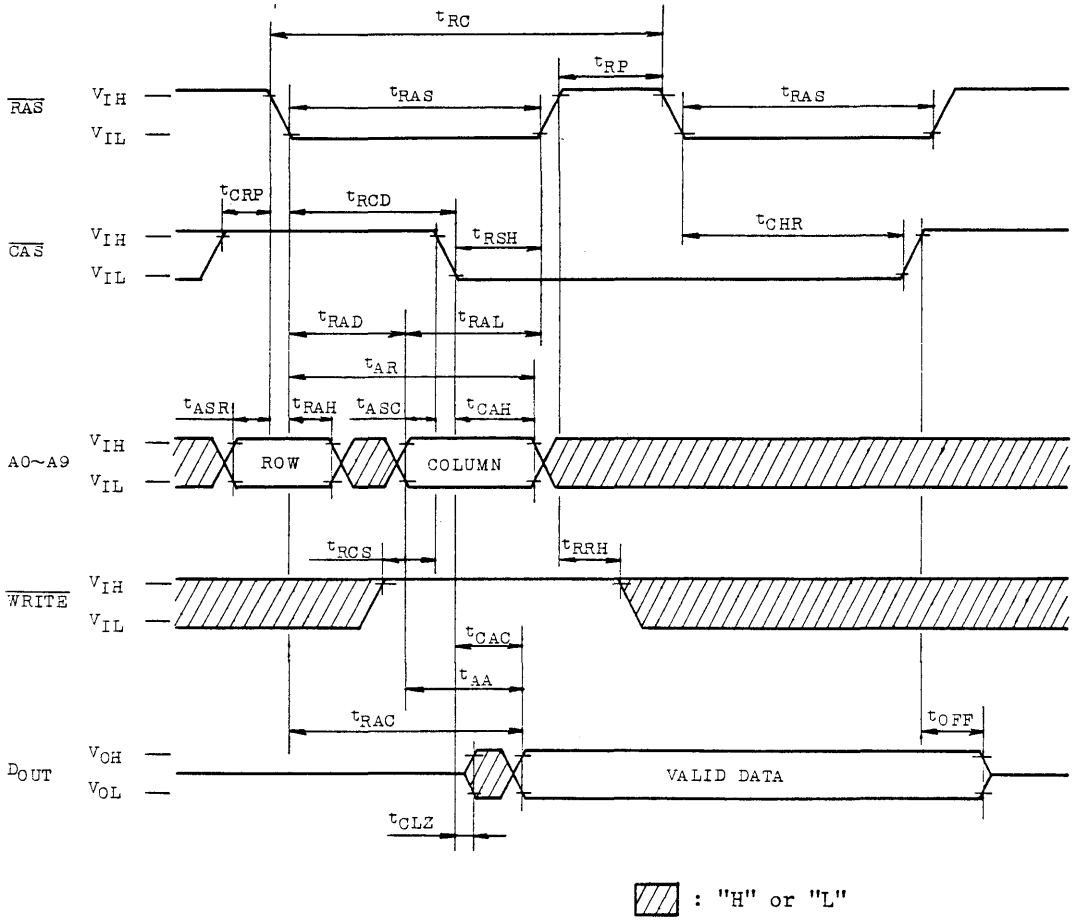


▨ : "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L" A9="H" or "L"

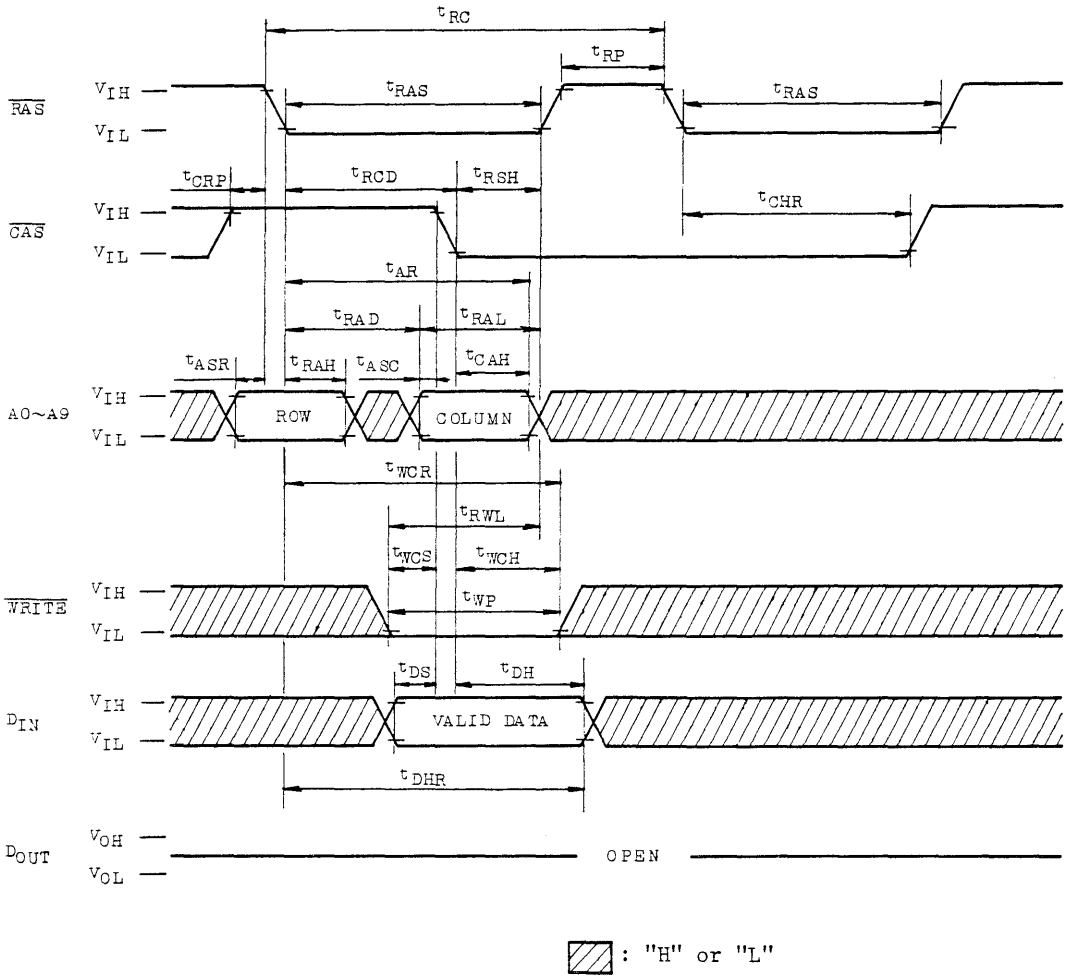
"TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



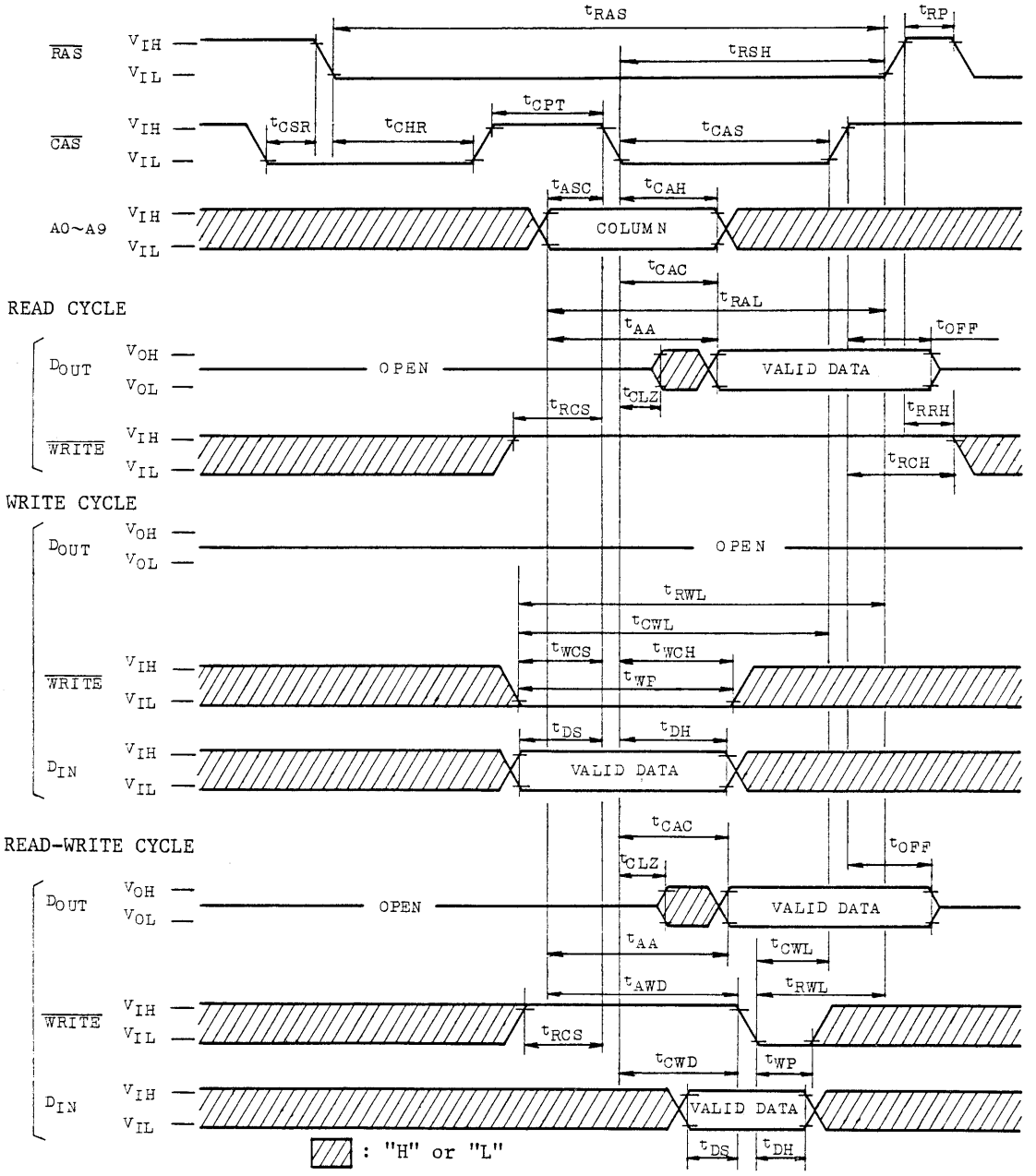
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

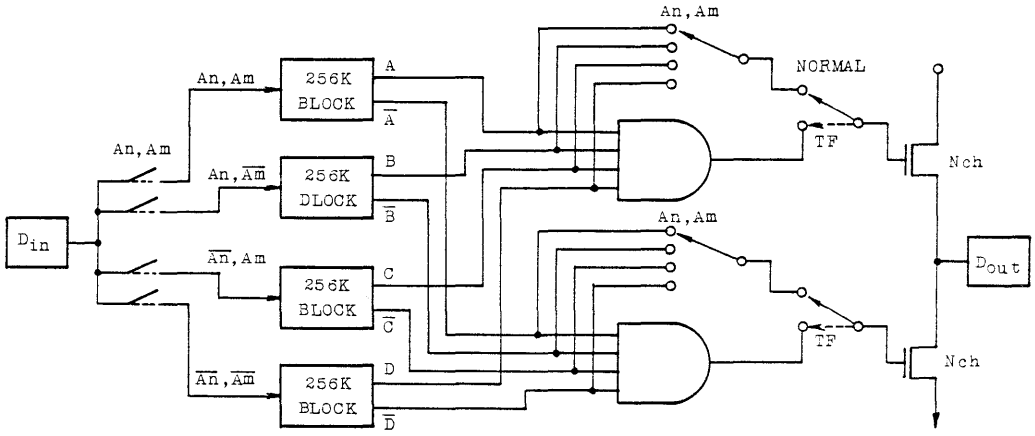
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000A/1A/2A is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bit.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin=Super voltage; Test Mode
TF Pin=V_{IL}(TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

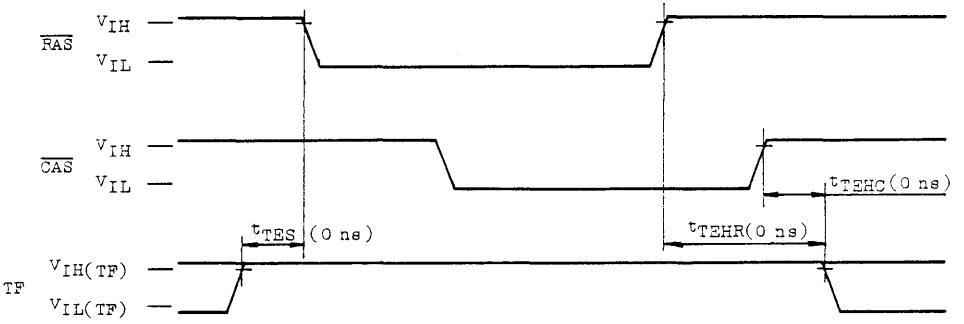
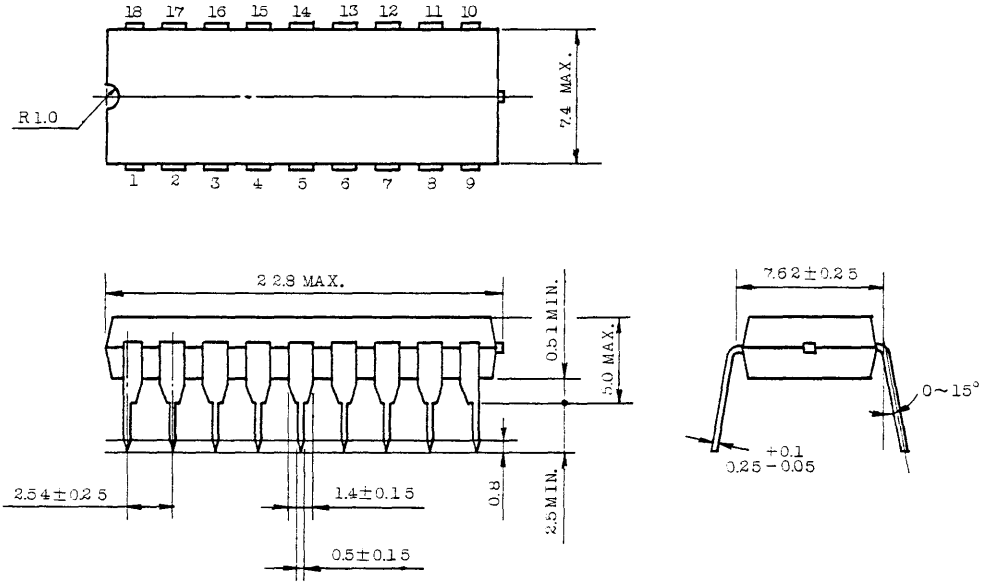


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

• Plastic DIP

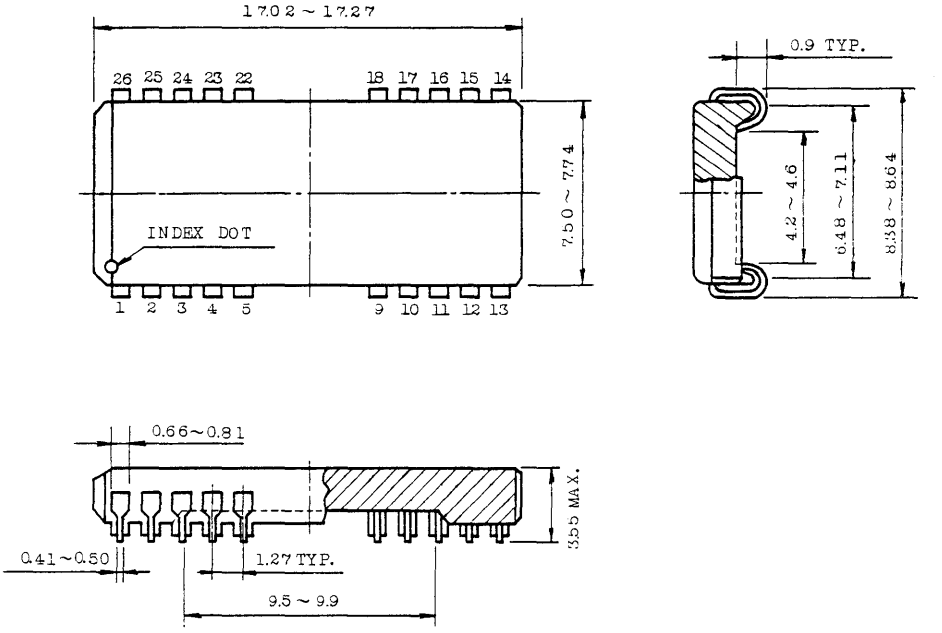
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

• Plastic SOJ

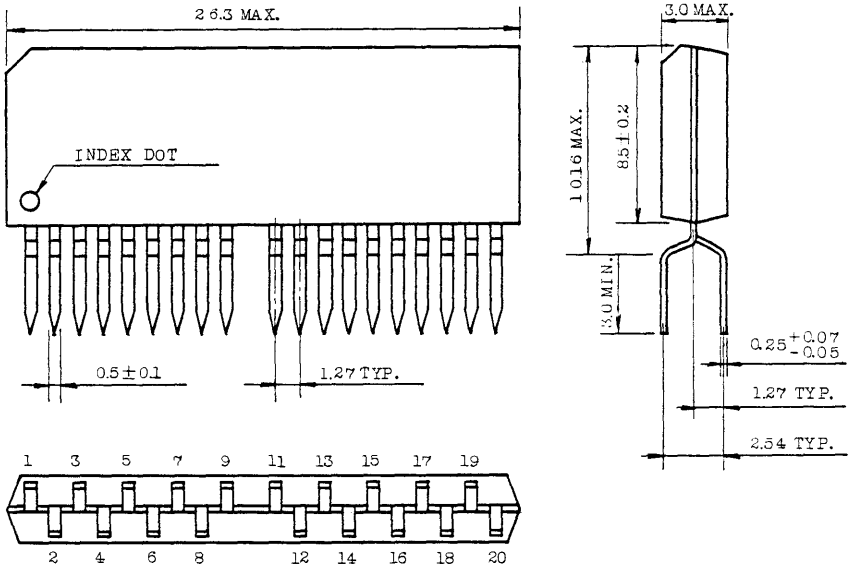
Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC511000APL/AJL/AZL-70, TC511000APL/AJL/AZL-80
TC511000APL/AJL/AZL-10

DESCRIPTION

The TC511000APL/AJL/AZL is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000APL/AJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000APL/AJL/AZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

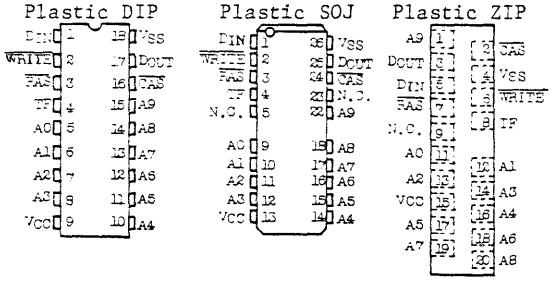
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000APL/AJL/AZL-70/80/10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator

- **Low standby current : 200μA max.**
- **Extended Refresh Period : 512 cycles/64ms**
- Low Power
  440mW MAX. Operating (TC511000APL/AJL/AZL-70)
  385mW MAX. Operating (TC511000APL/AJL/AZL-80)
  330mW MAX. Operating (TC511000APL/AJL/AZL-10)
  1.1mW MAX. Standby
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible

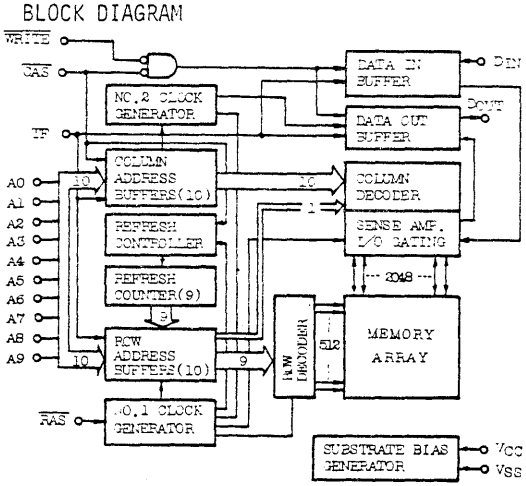
PIN CONNECTION



PIN NAMES

A0 ∿ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



1,048,576 WORD×1 BIT DYNAMIC RAM

SILICON GATE CMOS

TC511001P/J/Z-85, TC511001P/J/Z-10 TC511001P/J/Z-12

DESCRIPTION

The TC511001P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001P/J/Z is nibble mode, allowing the user to serially access 4 bits of data at a high data rate. "Test Mode" function is implemented from Revision C.

FEATURES

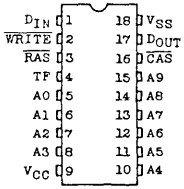
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511001P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

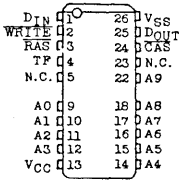
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power:
  385mW MAX. Operating (TC511001P/J/Z-85)
  330mW MAX. Operating (TC511001P/J/Z-10)
  275mW MAX. Operating (TC511001P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional clip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Packing Plastic DIP : TC511001P
  Plastic SOJ : TC511001J
  Plastic ZIP : TC511001Z

PIN CONNECTION (TOP VIEW)

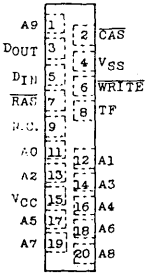
Plastic DIP



Plastic SOJ



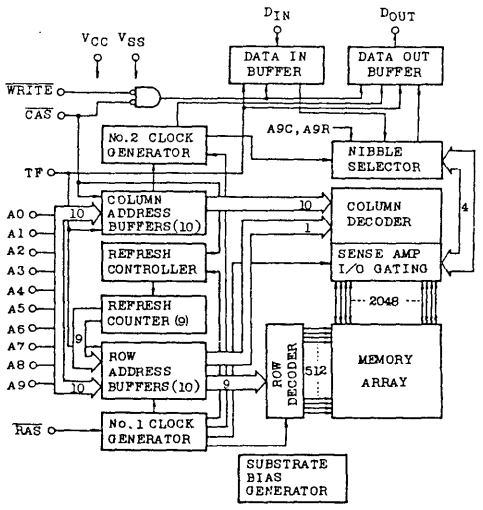
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Test Mode Input Voltage	$V_{IN(TF)}$	−1 ~ 10.5	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC} +4.5	–	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0	–	V_{CC} +1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511001P/J/Z-85	–	70	mA	3, 4
		TC511001P/J/Z-10	–	60	mA	
		TC511001P/J/Z-12	–	50	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	3
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TC511001P/J/Z-85	–	70	mA	3
		TC511001P/J/Z-10	–	60	mA	
		TC511001P/J/Z-12	–	50	mA	
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{NC} = t_{NC} MIN.)	TC511001P/J/Z-85	–	50	mA	3, 4
		TC511001P/J/Z-10	–	40	mA	
		TC511001P/J/Z-12	–	30	mA	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC}-0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511001P/J/Z-85	–	70	mA	3
		TC511001P/J/Z-10	–	60	mA	
		TC511001P/J/Z-12	–	50	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RWC}	Read-Write Cycle Time	190	–	220	–	255	–	ns	
t_{NC}	Nibble Mode Cycle Time	40	–	40	–	50	–	ns	
t_{NRMW}	Nibble Mode Read-Write Cycle Time	65	–	65	–	80	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	35	–	40	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	8, 14
t_{NCAC}	Nibble Mode Access Time	–	20	–	20	–	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	–	5	–	5	–	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	35	–	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to RAS	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data-In Hold Time	20	–	20	–	25	–	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001P/J/Z-85		TC511001P/J/Z-10		TC511001P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	30	–	35	–	40	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	85	–	100	–	120	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	–	50	–	60	–	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	–	20	–	25	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	–	10	–	15	–	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

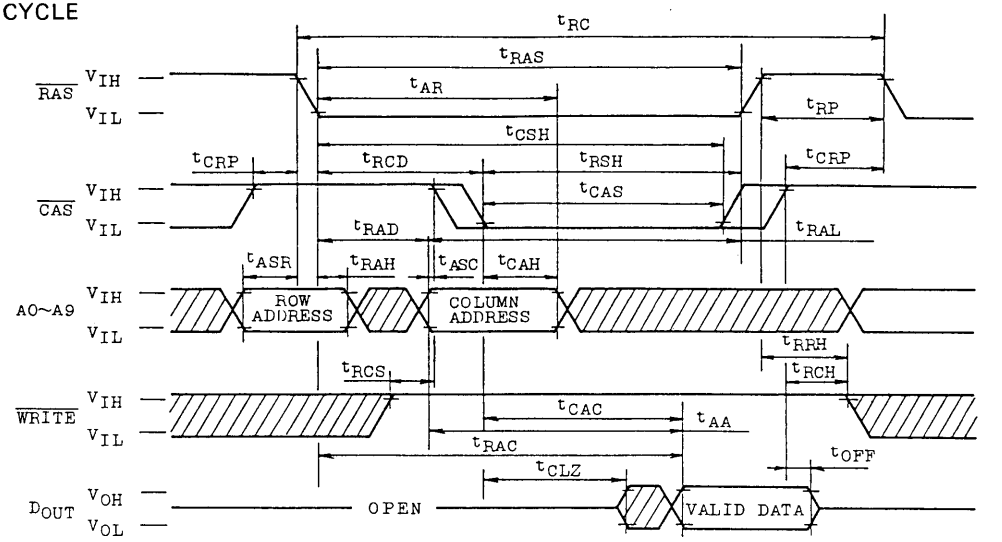
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_9$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

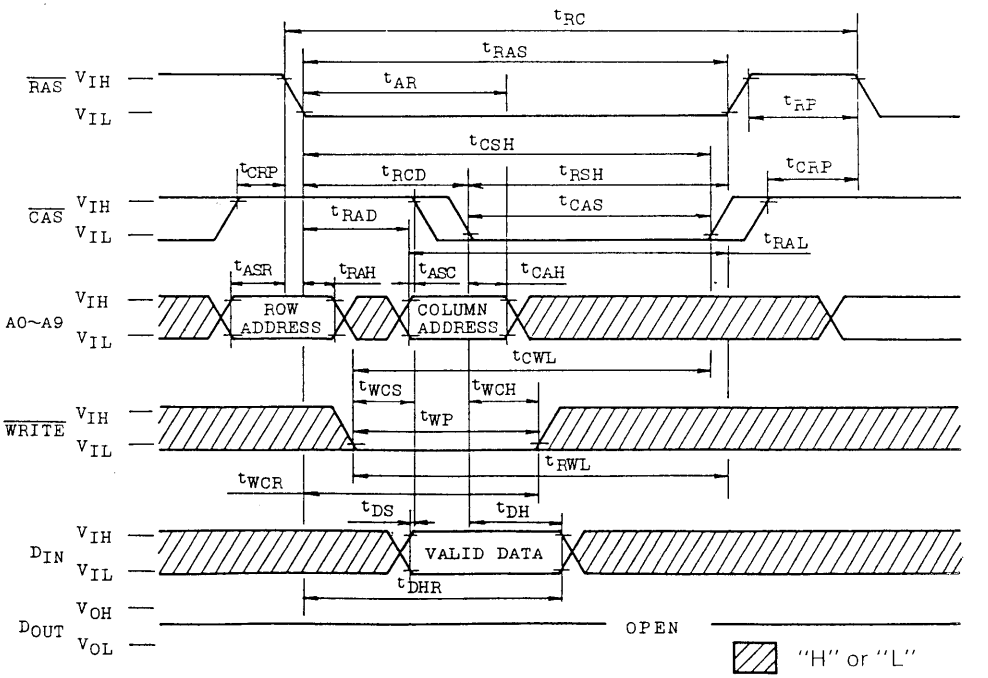
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

- READ CYCLE

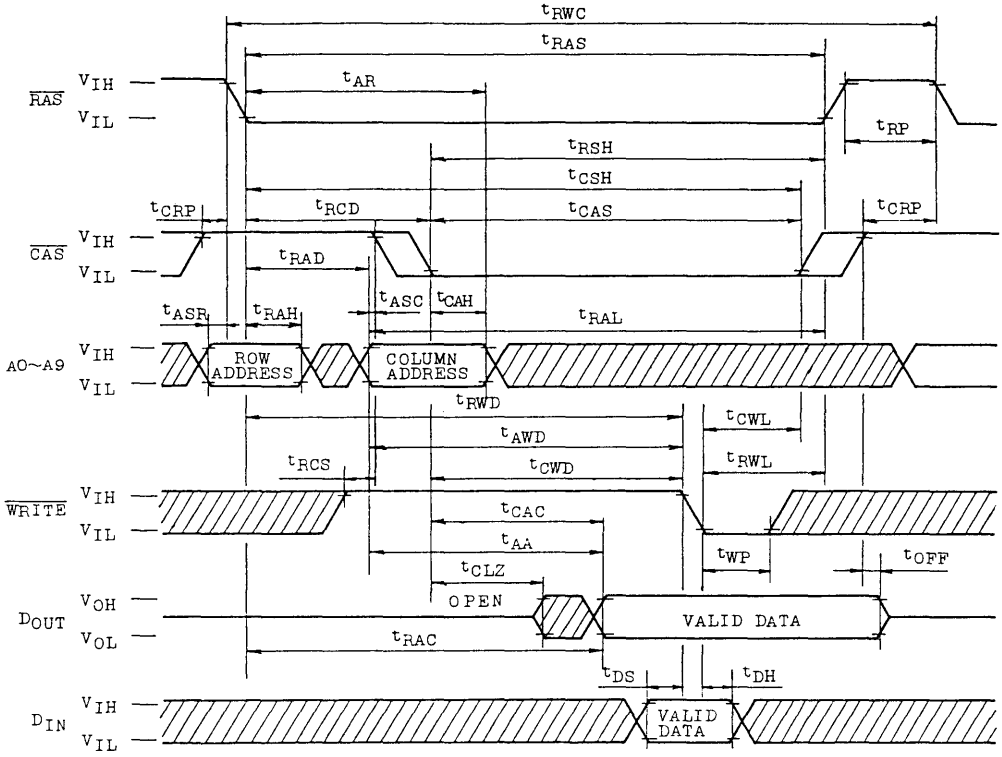


- WRITE CYCLE (EARLY WRITE)



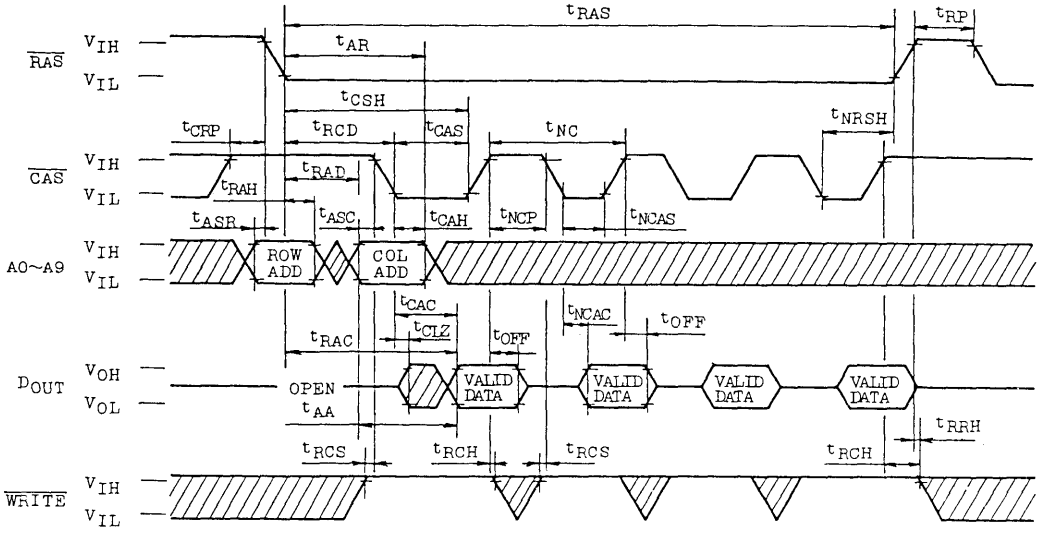
NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- READ-WRITE CYCLE

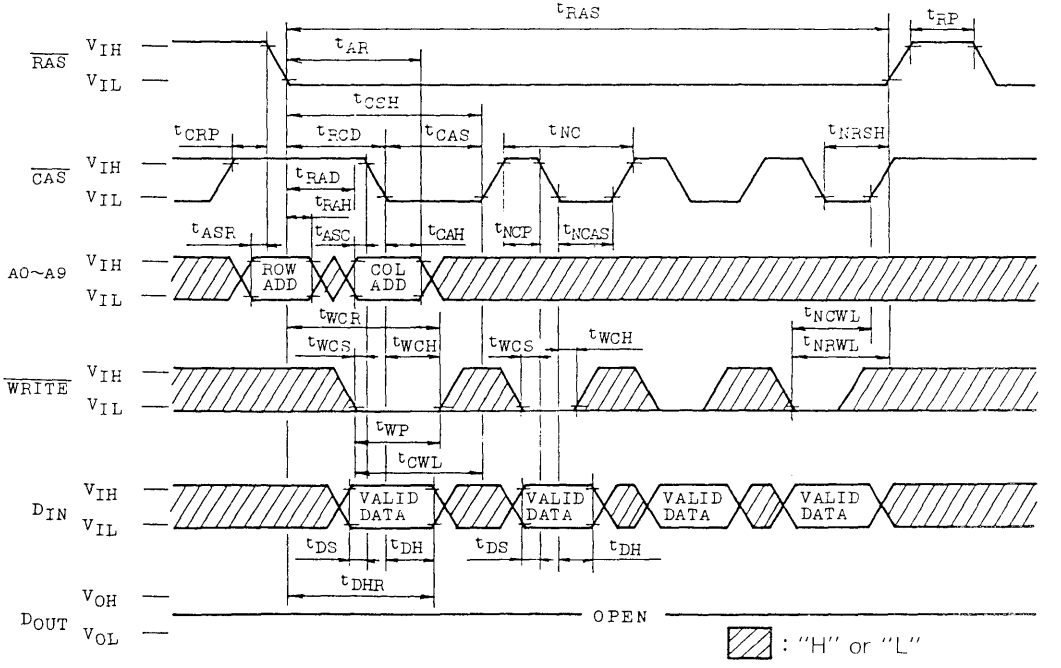


NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- NIBBLE MODE READ CYCLE

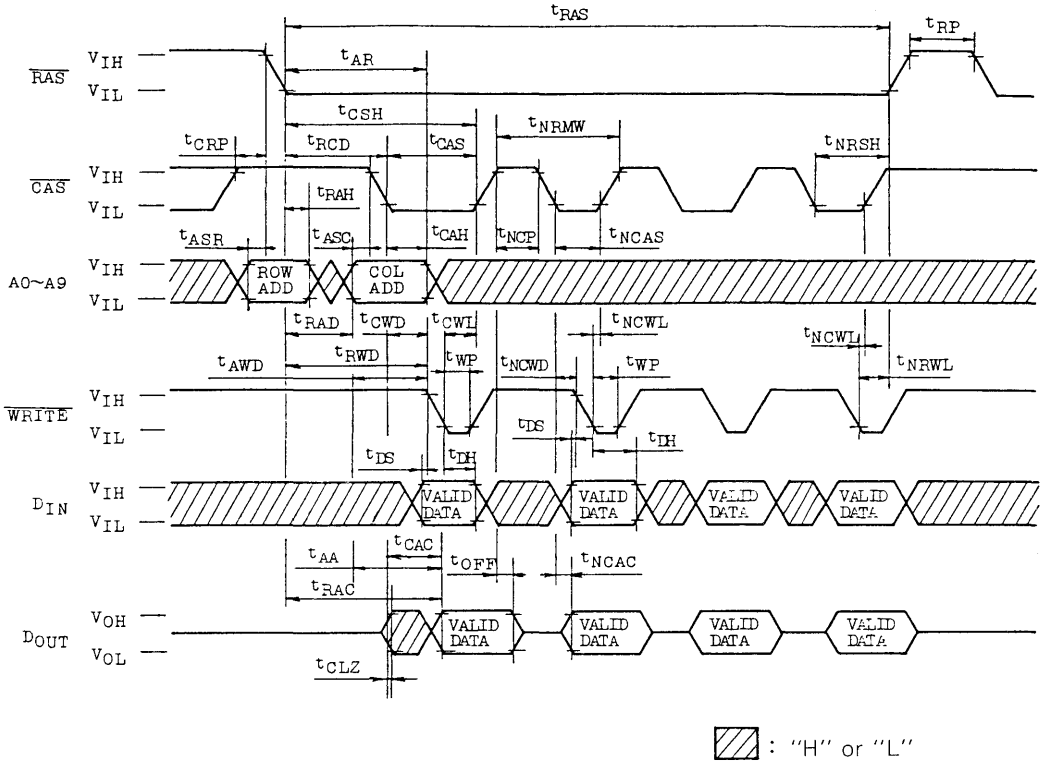


- NIBBLE MODE WRITE CYCLE (EARLY WRITE)



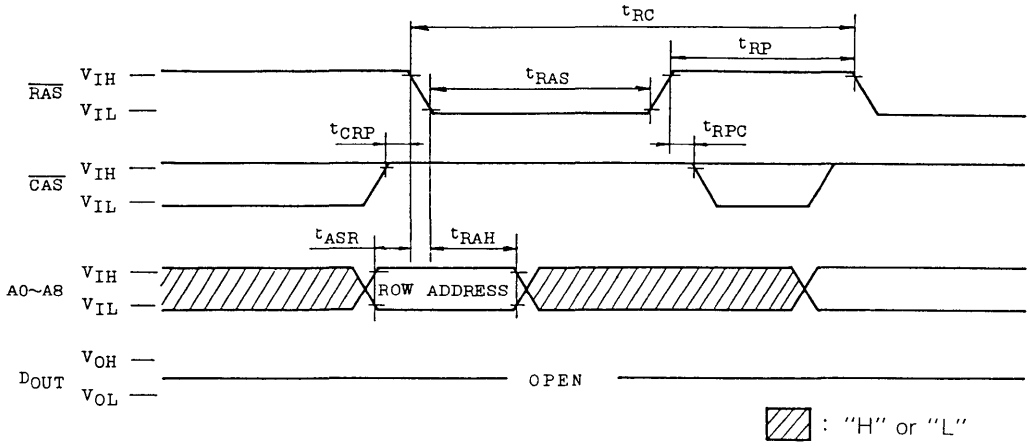
NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open.

- NIBBLE MODE READ-WRITE CYCLE



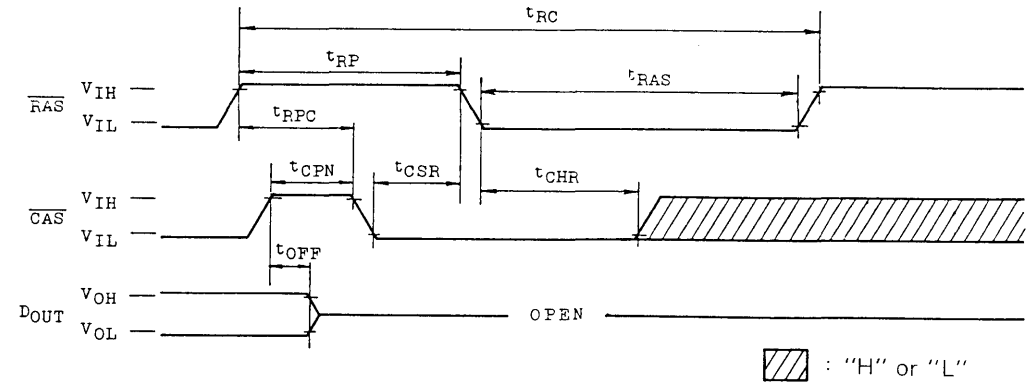
NOTE: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open.

- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

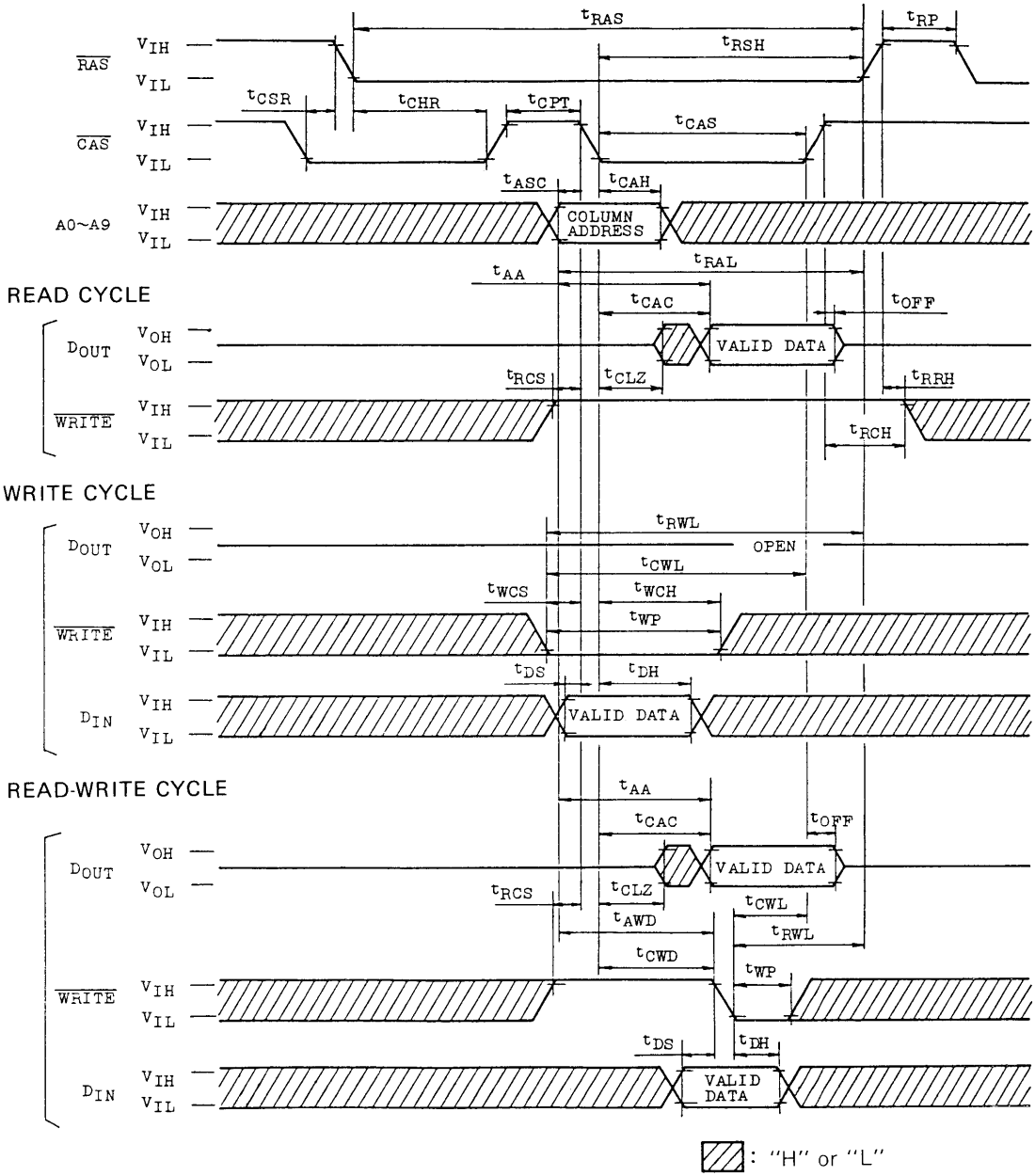
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



NOTE: $\overline{WRITE}$ = "H" or "L", A0 ~ A9 = "H" or "L"

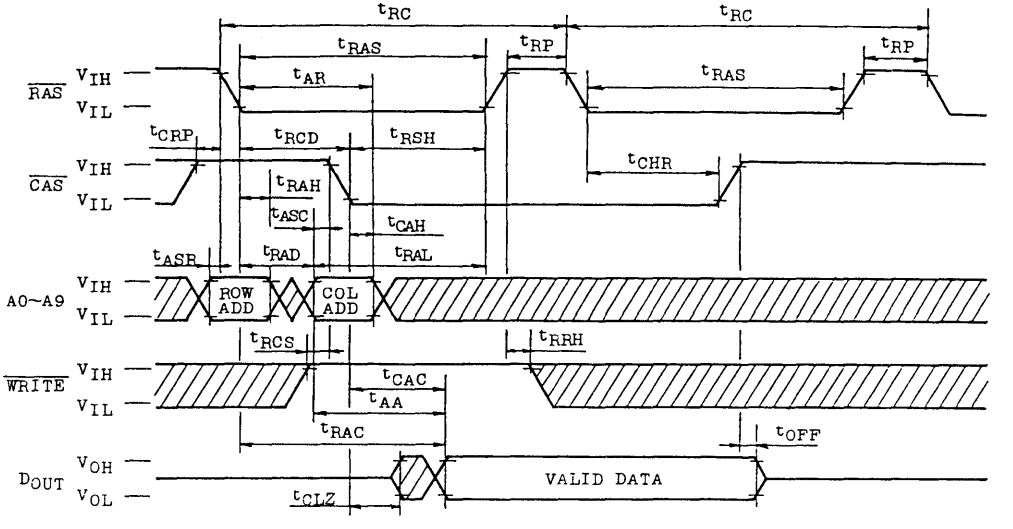
"TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

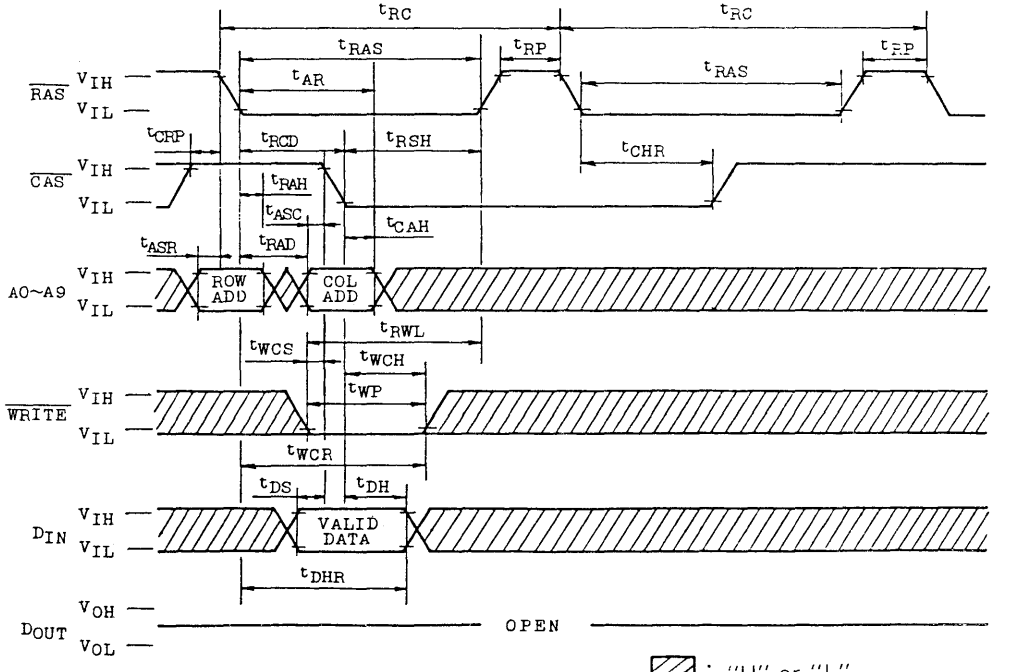


NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- HIDDEN REFRESH CYCLE (READ)



- HIDDEN REFRESH CYCLE (WRITE)



▨ : "H" or "L"

NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001P/J/Z are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle is a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

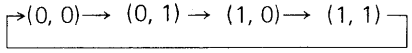
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active(low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001P/J/Z is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ~ A8) within each 8 millisecond time interval. Although any normal memory cycle

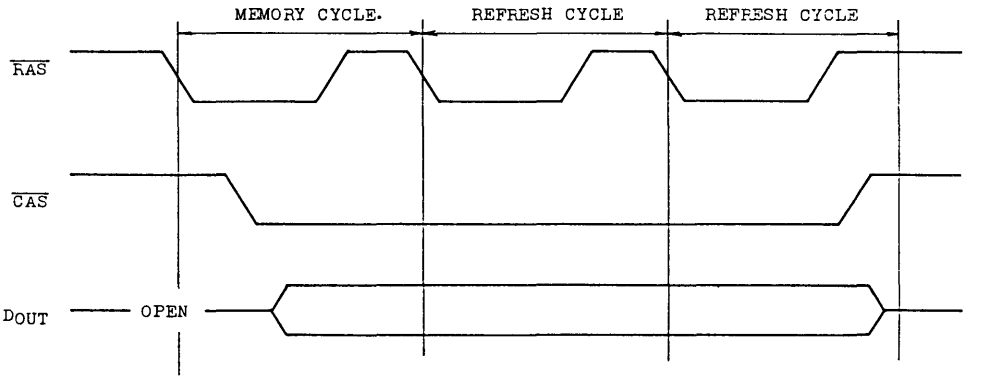
will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001P/J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in perparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001P/J/Z is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001P/J/Z can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST.
Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④

⑥ Perform the above ① to ⑤ the complement data.

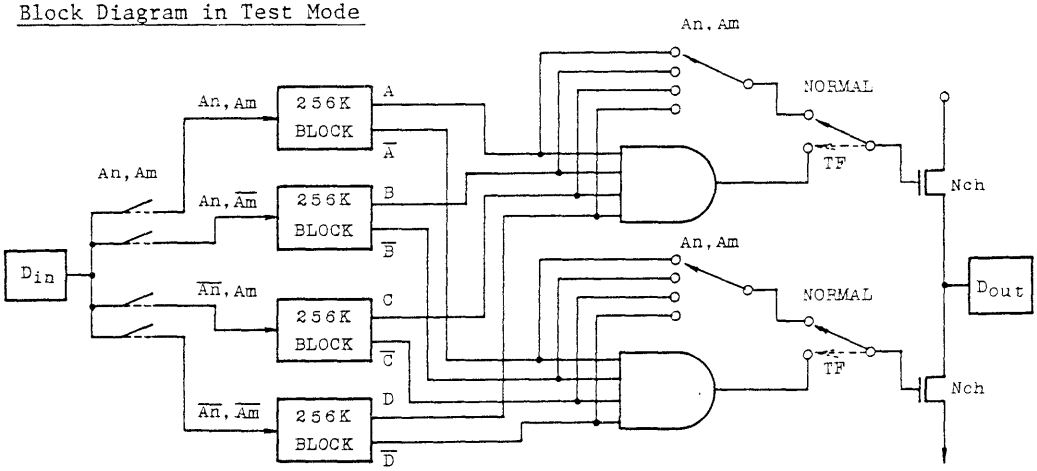
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super Voltage; Test Mode

TF Pin = Low Level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

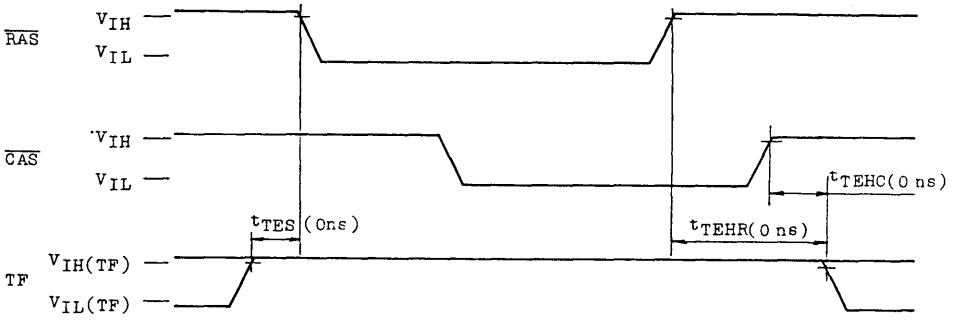
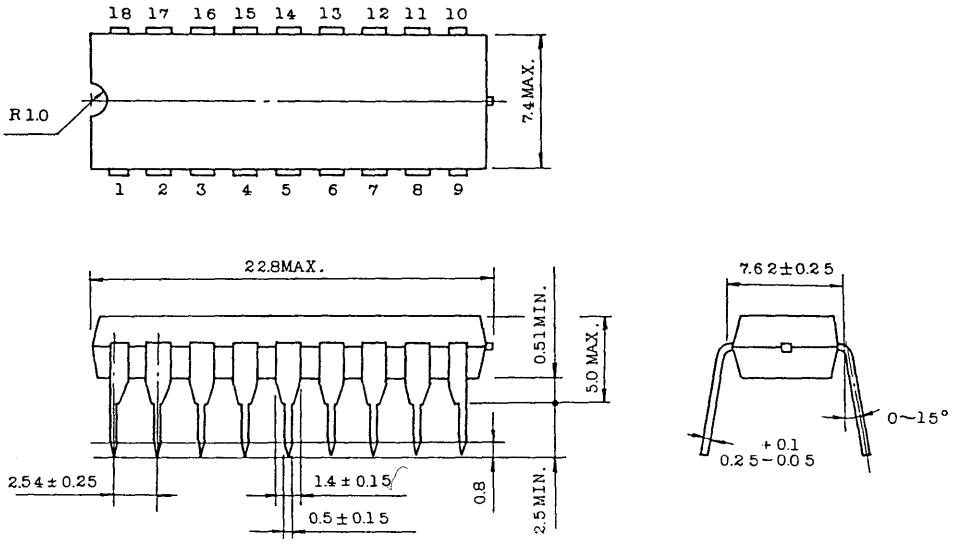


Fig. 2 Test Mode Cycle

OUTLINE DRAWINGS

- Plastic DIP

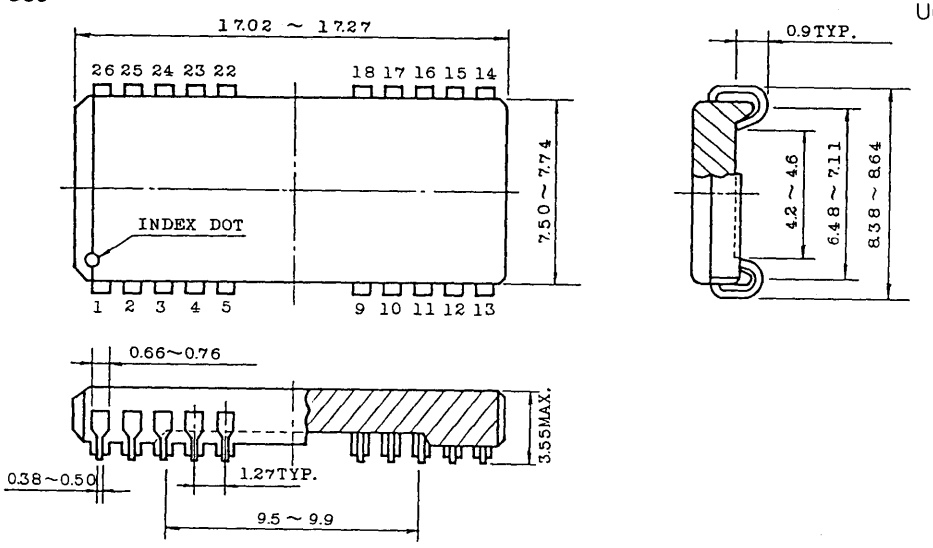
Unit: in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

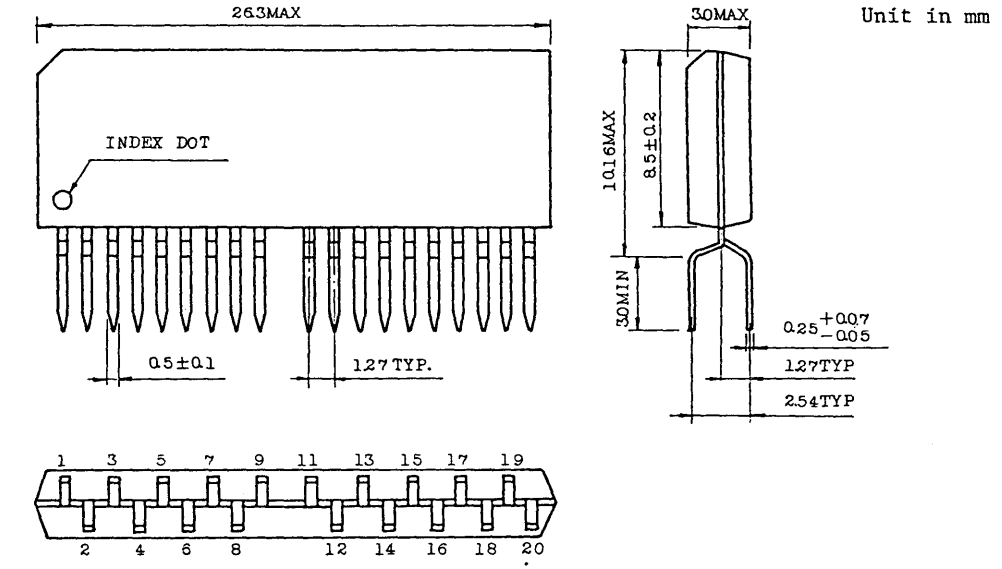
- Plastic SOJ

Unit: in mm



- Plastic ZIP

Unit in mm



NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC511001AP/AJ/AZ-70, TC511001AP/AJ/AZ-80
TC511001AP/AJ/AZ-10

DESCRIPTION

The TC511001AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001AP/AJ/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

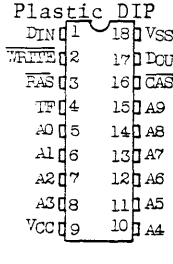
- 1,048,576 words by 1 bit organization
- Fast access time and cycle time

		TC511001AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{NCAC}	Nibble Mode Access Time	15ns	15ns	20ns
t_{NC}	Nibble Mode Cycle Time	35ns	35ns	40ns

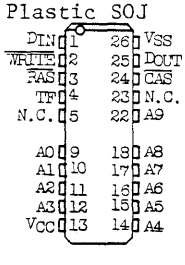
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power:
  440mW MAX. Operating(TC511001AP/AJ/AZ-70)
  385mW MAX. Operating(TC511001AP/AJ/AZ-80)
  330mW MAX. Operating(TC511001AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511001AP
  Plastic SOJ: TC511001AJ
  Plastic ZIP: TC511001AZ

PIN CONNECTION (TOP VIEW)

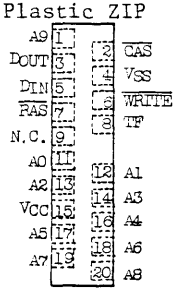
Plastic DIP



Plastic SOJ



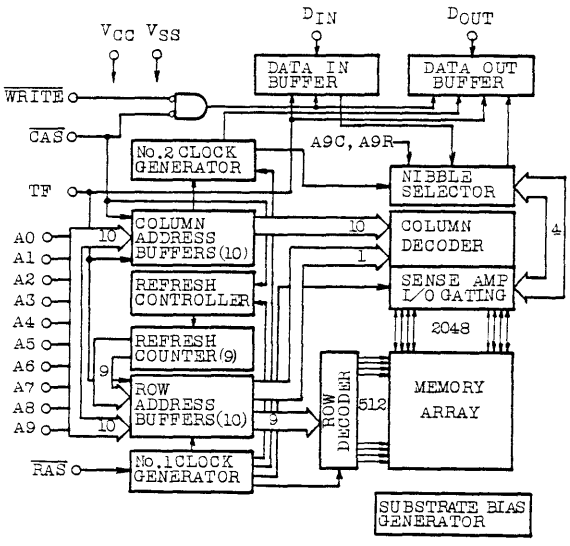
Plastic ZIP



PIN NAMES

A0~A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1∿7	V	1
Test Mode Input Voltage	$V_{IN(TF)}$	-1∿10.5	V	1
Ootput Voltage	V_{OUT}	-1∿7	V	1
Power Supply Voltage	V_{CC}	-1∿7	V	1
Operating Temperature	T_{OPR}	0∿70	°C	1
Storage Temperature	T_{STG}	-55∿150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	-1.0	-	V_{CC}+1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10% Ta=0∿70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511001AP/AJ/AZ-70	-	80	mA	3,4
		TC511001AP/AJ/AZ-80	-	70		
		TC511001AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	3
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511001AP/AJ/AZ-70	-	80	mA	3
		TC511001AP/AJ/AZ-80	-	70		
		TC511001AP/AJ/AZ-10	-	60		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	TC511001AP/AJ/AZ-70	-	60	mA	3,4
		TC511001AP/AJ/AZ-80	-	50		
		TC511001AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511001AP/AJ/AZ-70	-	80	mA	3
		TC511001AP/AJ/AZ-80	-	70		
		TC511001AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V≦$V_{IN(TF)}$≦V_{CC}+0.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦+5.5V)		-10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V≦$V_{IN(TF)}$≦10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511001AP/AJ/AZ-70		TC511001AP/AJ/AZ-80		TC511001AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RWC}	Read-Write Cycle Time	155	-	175	-	210	-	ns	
t_{NC}	Nibble Mode Cycle Time	35	-	35	-	40	-	ns	
t_{NRMW}	Nibble Mode Read-Write Cycle Time	55	-	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	15	-	15	-	20	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511001AP/AJ/AZ-70		TC511001AP/AJ/AZ-80		TC511001AP/AJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data-In Hold Time reference to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	20	-	25	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	-	80	-	100	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	-	40	-	50	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	-	40	-	50	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	15	-	15	-	20	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	15	-	15	-	20	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	15	-	15	-	20	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	15	-	15	-	20	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	15	-	15	-	20	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	pF
C_O	Output Capacitance (D_{OUT})	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are refernce levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.

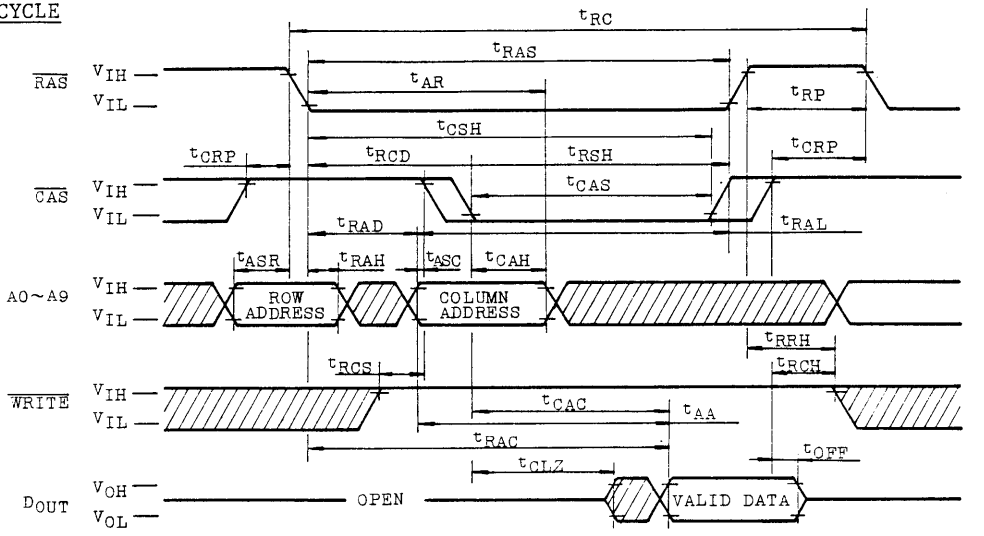
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

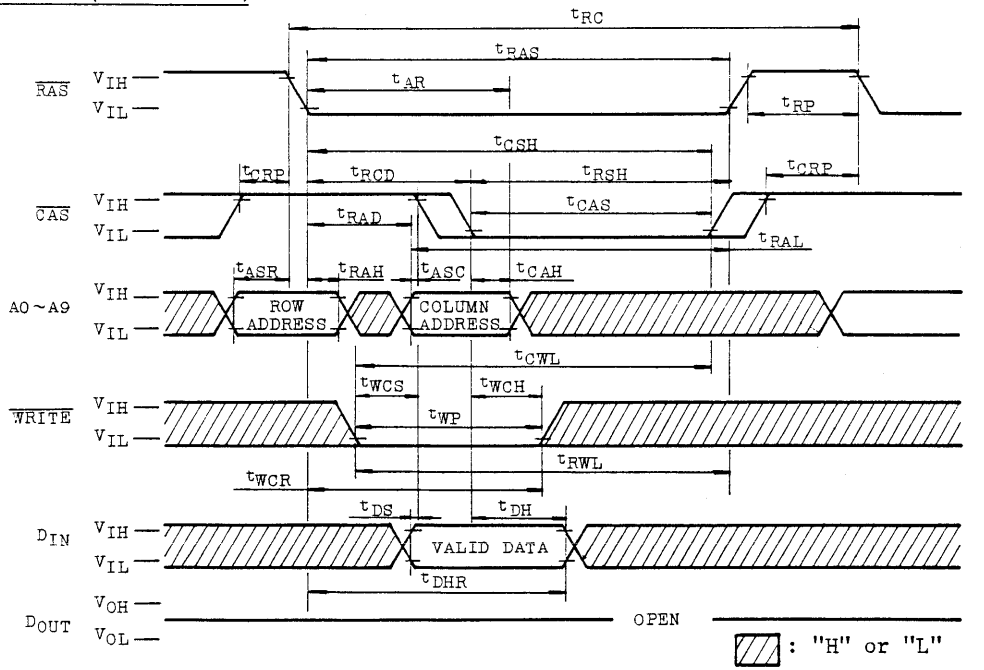
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

READ CYCLE

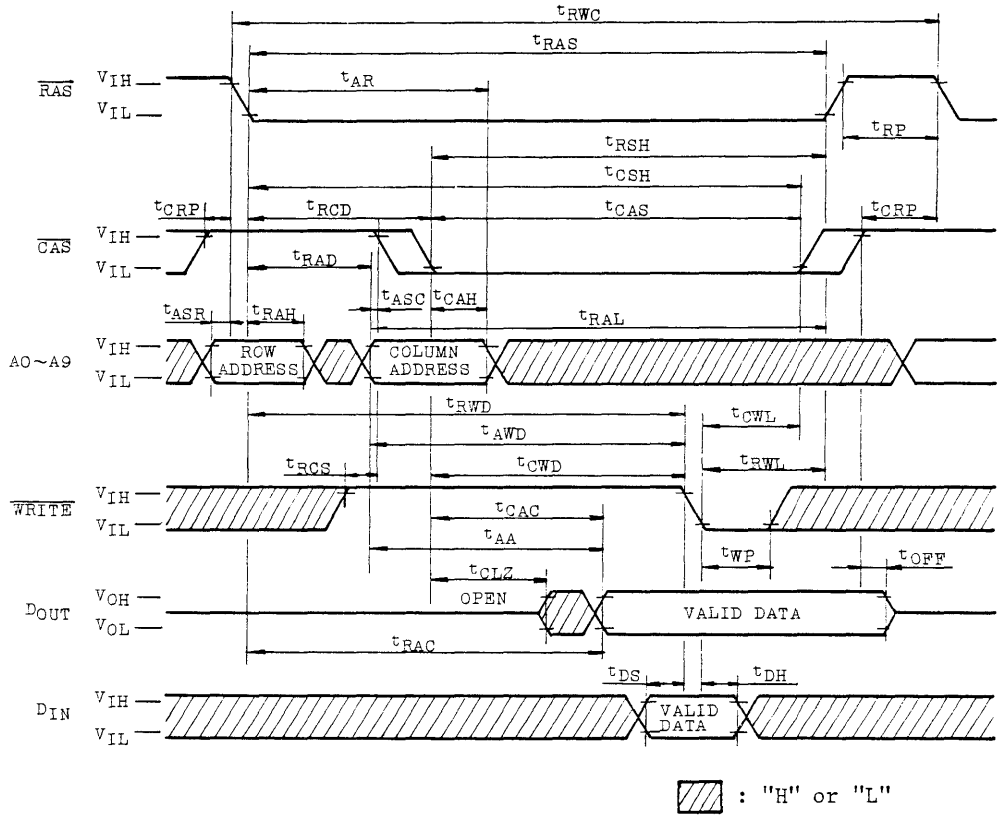


WRITE CYCLE (EARLY WRITE)



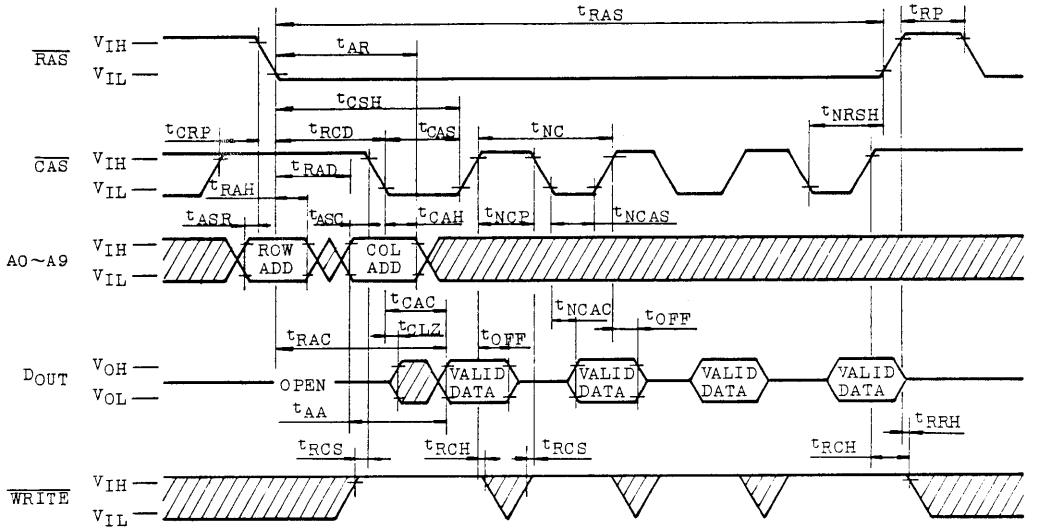
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

READ-WRITE CYCLE

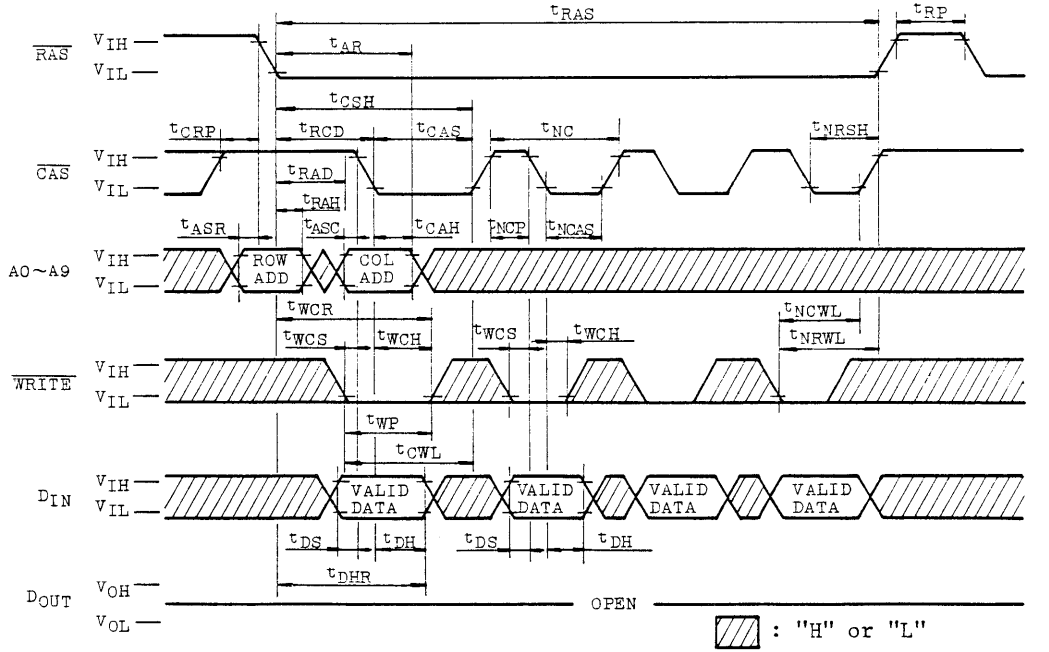


NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

NIBBLE MODE READ CYCLE

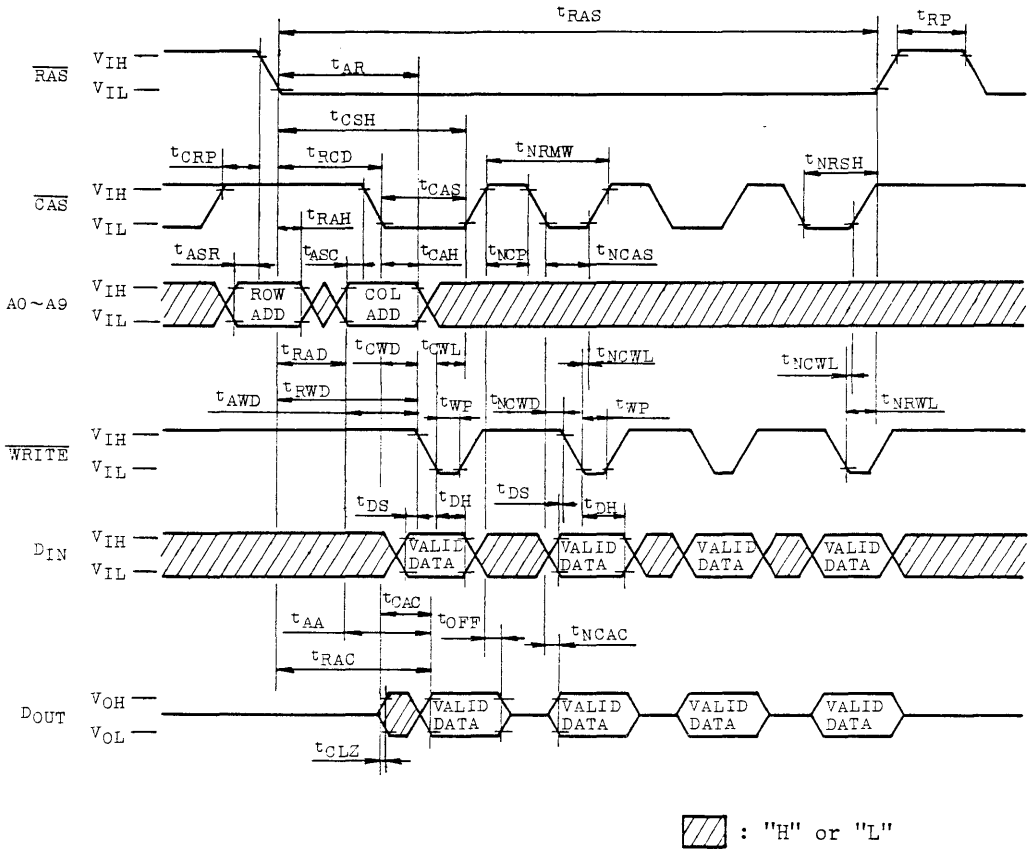


NIBBLE MODE WRITE CYCLE (EARLY WRITE)



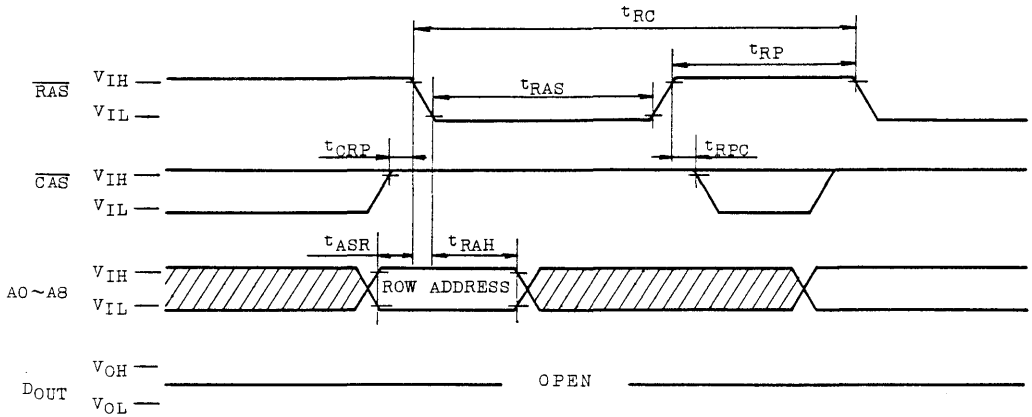
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open.

NIBBLE MODE READ-WRITE CYCLE



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open.

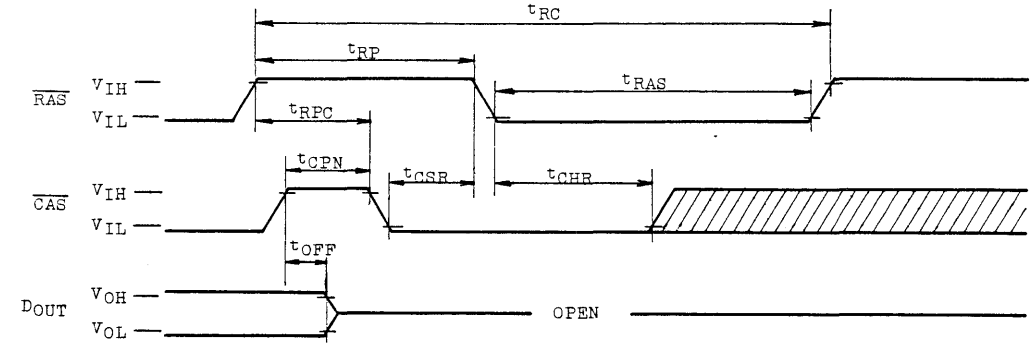
$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

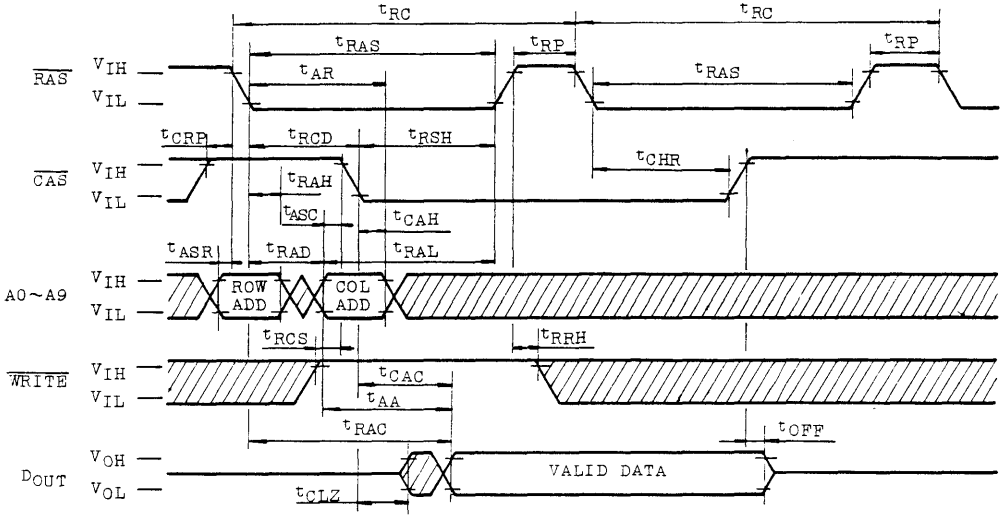


▨: "H" or "L"

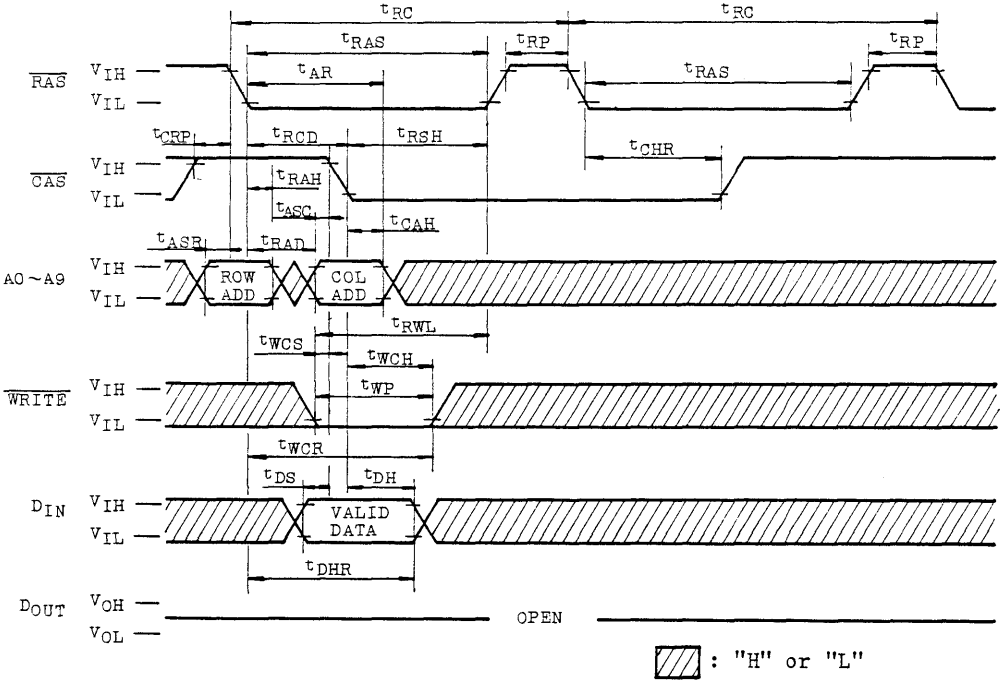
NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

"TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)

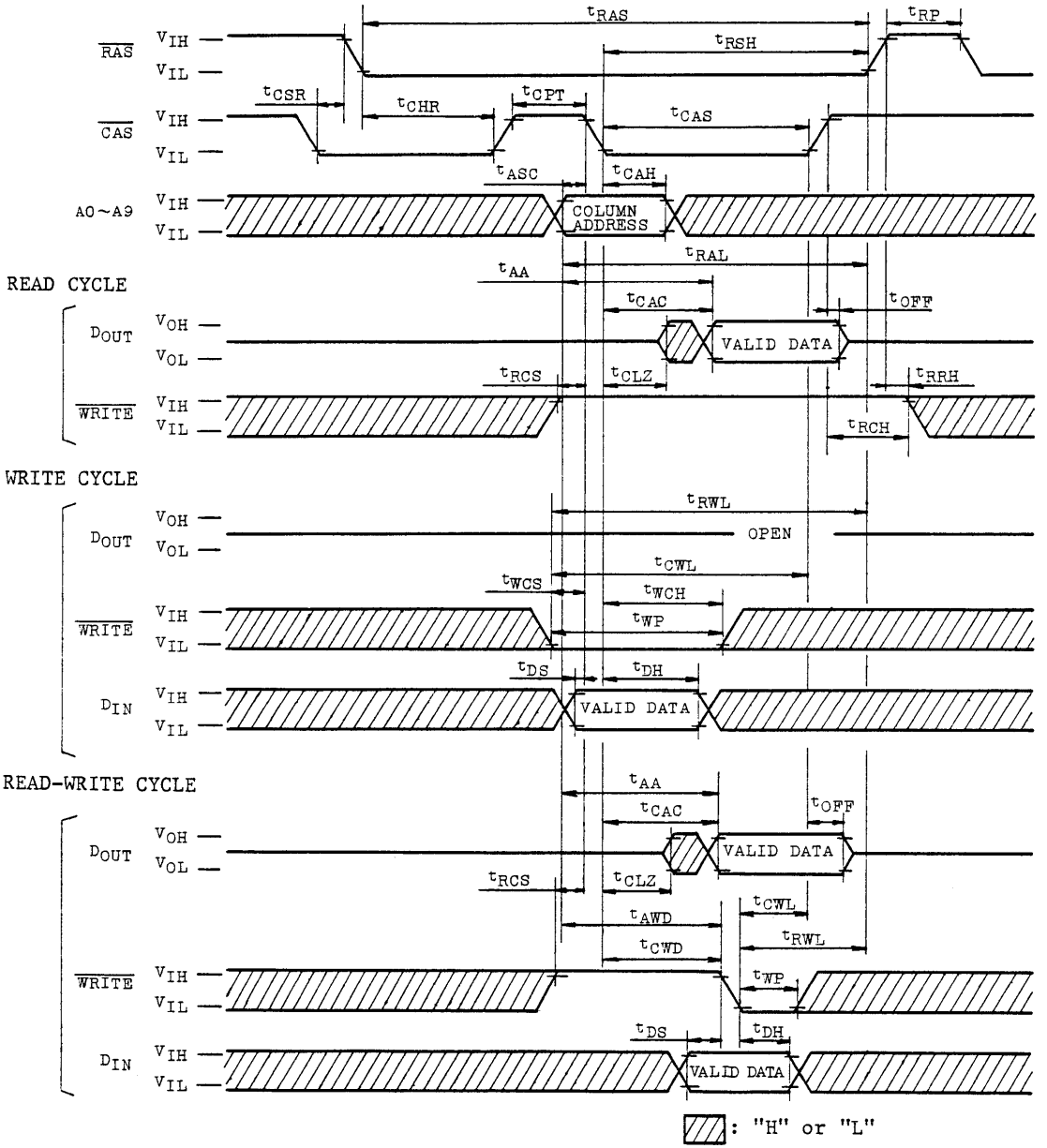


HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001AP/AJ/AZ are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made is negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and nibble mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

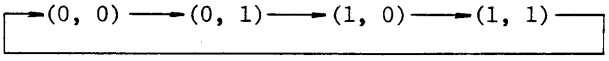
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be avilable at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001AP/AJ/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits.
From then on, successive bits come out in a binary fashion; 00 → 01 → 10 → 11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

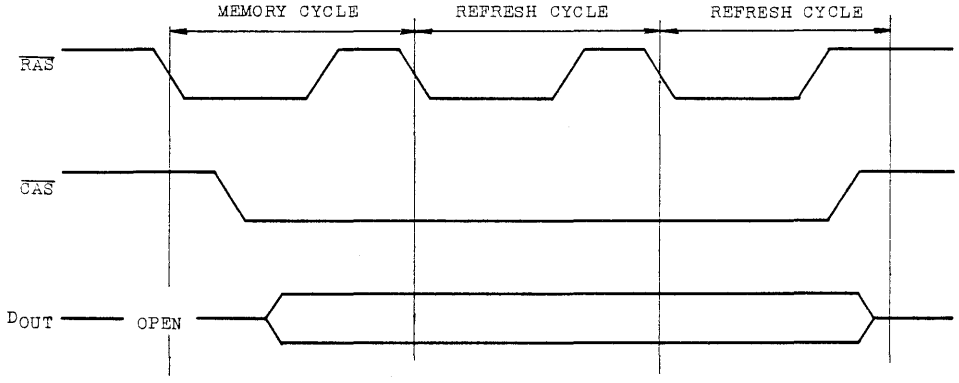
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ∿ A8) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing availalbe on the TC511001AP/AJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in perparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001AP/AJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data avilability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001AP/AJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one cartain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE).
Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST.
Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

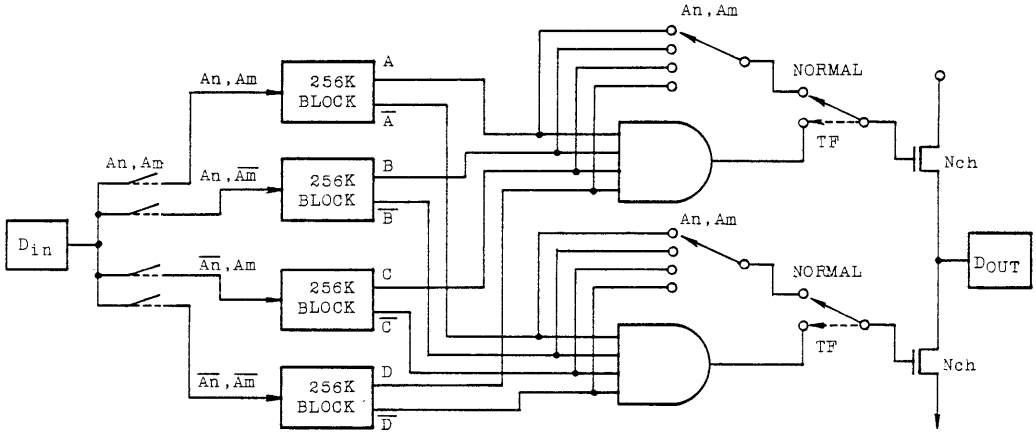
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000A/1A/2A is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bit.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin=Super Voltage; Test Mode
TF Pin=V_{IL}(TF) level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

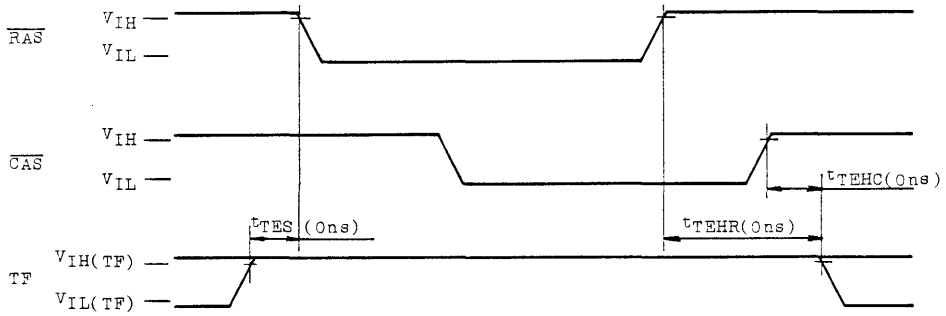
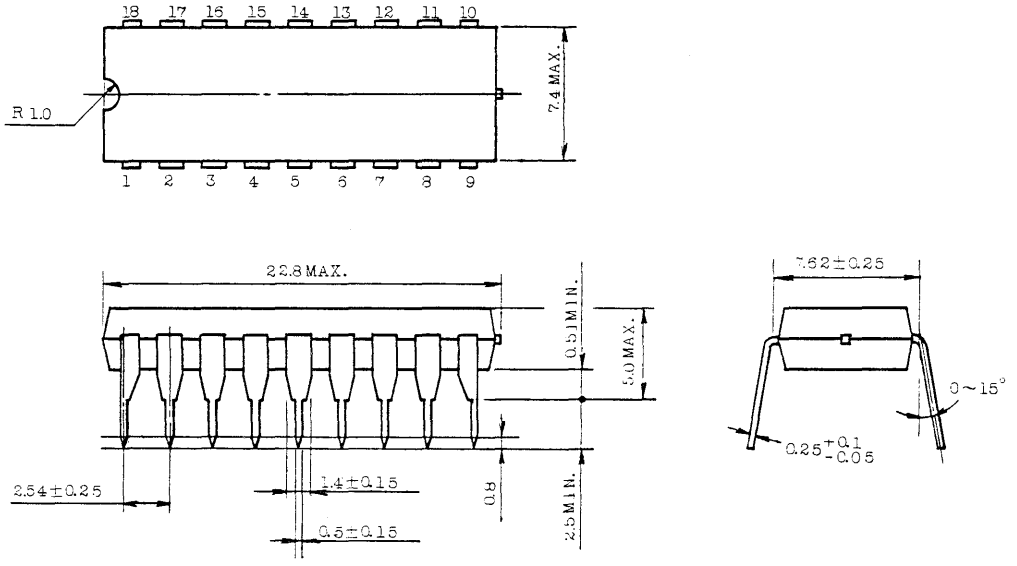


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

• Plastic DIP

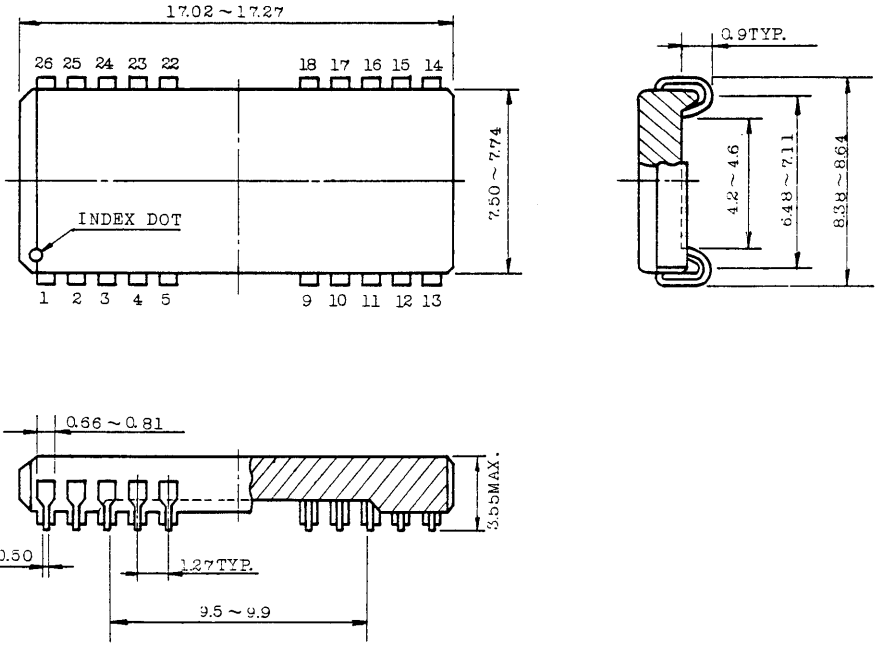
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads.
All dimensions are in millimeters.

• Plastic SOJ

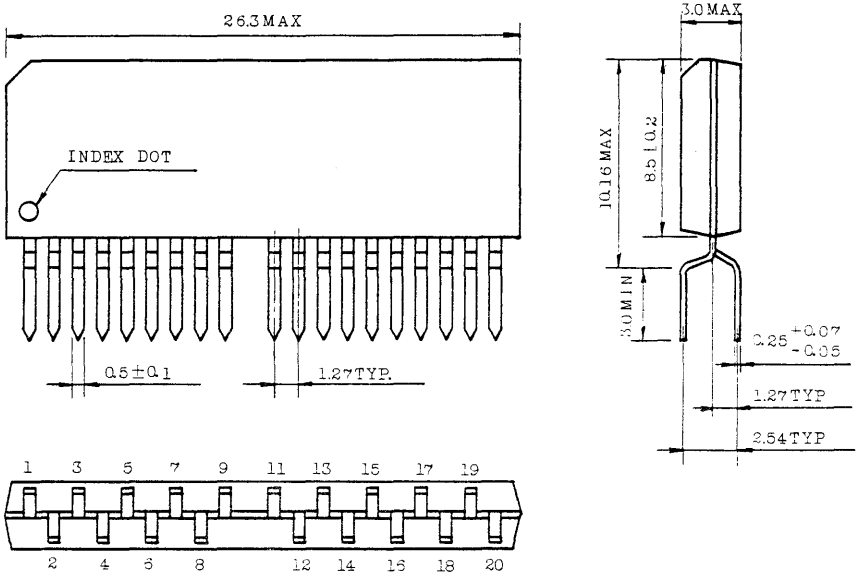
Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

1,048,576 WORD×1 BIT DYNAMIC RAM

SILICON GATE CMOS

TC511002P/J/Z-85, TC511002P/J/Z-10 TC511002P/J/Z-12

DESCRIPTION

The TC511002P/J/Z is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002 P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002P/J/Z to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. "Test Mode" function is implemented from Revision C.

FEATURES

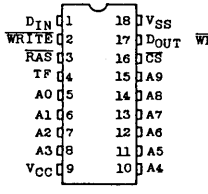
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511002P/J/Z-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	CS Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

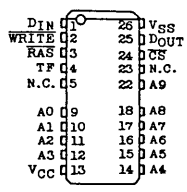
- Sincle power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  385mW MAX. Operating (TC511002P/J/Z-85)
  330mW MAX. Operating (TC511002P/J/Z-10)
  275mW MAX. Operating (TC511002P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511002P
  Plastic SOJ: TC511002J
  Plastic ZIP: TC511002Z

PIN CONNECTION (TOP VIEW)

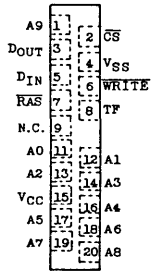
Plastic DIP



Plastic SOJ



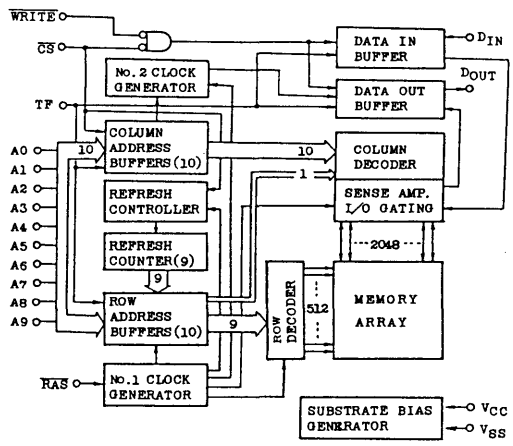
Plastic ZIP



PIN NAMES

A0 ~ A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
DIN	Data In
DOUT	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
VCC	Power (+5V)
VSS	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	−1 ~ 10.5	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC} +4.5	–	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0	–	V_{CC} +1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5 ± 10%, T_a = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511002P/J/Z-85	–	70	mA	3, 4
		TC511002P/J/Z-10	–	60	mA	
		TC511002P/J/Z-12	–	50	mA	
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH}: t_{RC} = t_{RC}, MIN.)	TC511002P/J/Z-85	–	70	mA	3
		TC511002P/J/Z-10	–	60	mA	
		TC511002P/J/Z-12	–	50	mA	
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$ = $\overline{CS}$ = V_{IL} , Address Cycling: t_{SC} = t_{SC} MIN.)	TC511002P/J/Z-85	–	50	mA	3, 4
		TC511002P/J/Z-10	–	40	mA	
		TC511002P/J/Z-12	–	30	mA	
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC}-0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511002P/J/Z-85	–	70		3
		TC511002P/J/Z-10	–	60	mA	
		TC511002P/J/Z-12	–	50	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IH} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ + 5.5V)		−10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RWC}	Read-Write Cycle Time	190	–	220	–	255	–	ns	
t_{SC}	Static Column Mode Cycle Time	50	–	55	–	65	–	ns	
t_{SRWC}	Static Column Mode Read Write Cycle Time	90	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CS}$	–	25	–	25	–	30	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	8, 14
t_{ALW}	Access Time from Last Write	–	85	–	95	–	115	ns	8, 15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	–	5	–	5	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	–	5	–	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	25	–	25	–	30	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	–	0	–	0	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	–	115	–	140	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	–	10	–	15	–	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	25	–	30	–	ns	
t_{LWAD}	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	15

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511002P/J/Z-85		TC511002P/J/Z-10		TC511002P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AHLW}	Last Write to Column Address Hold Time	85	–	95	–	115	–	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	–	0	–	0	–	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data-In Hold Time	20	–	20	–	25	–	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	25	–	25	–	30	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	85	–	100	–	120	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	45	–	50	–	60	–	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	–	50	–	60	–	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

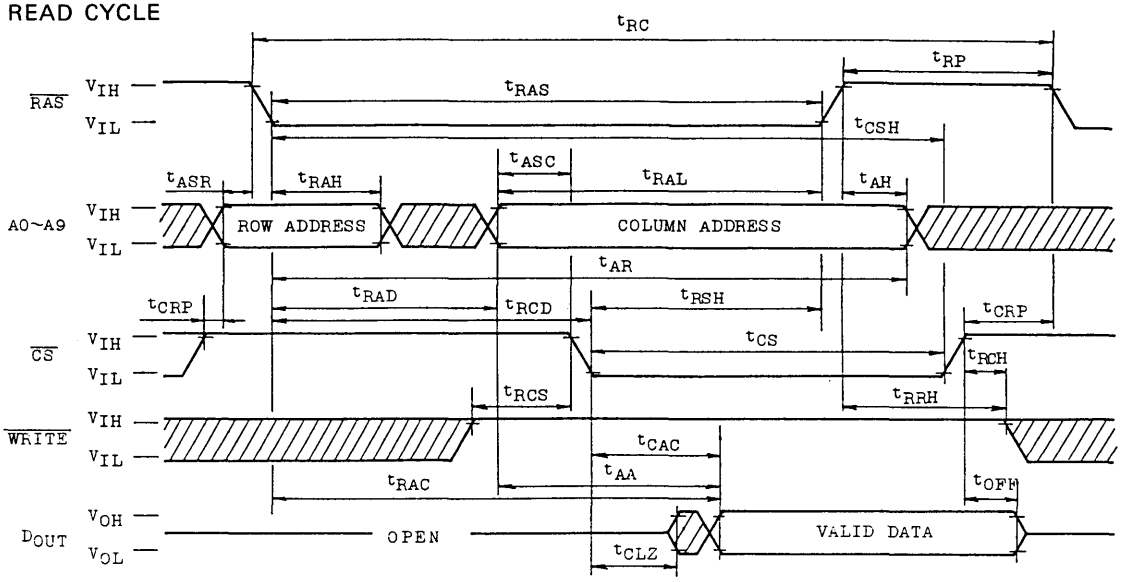
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_9$, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	–	7	pF
C_O	Output Capacitance (D_{OUT})	–	7	pF

NOTES:

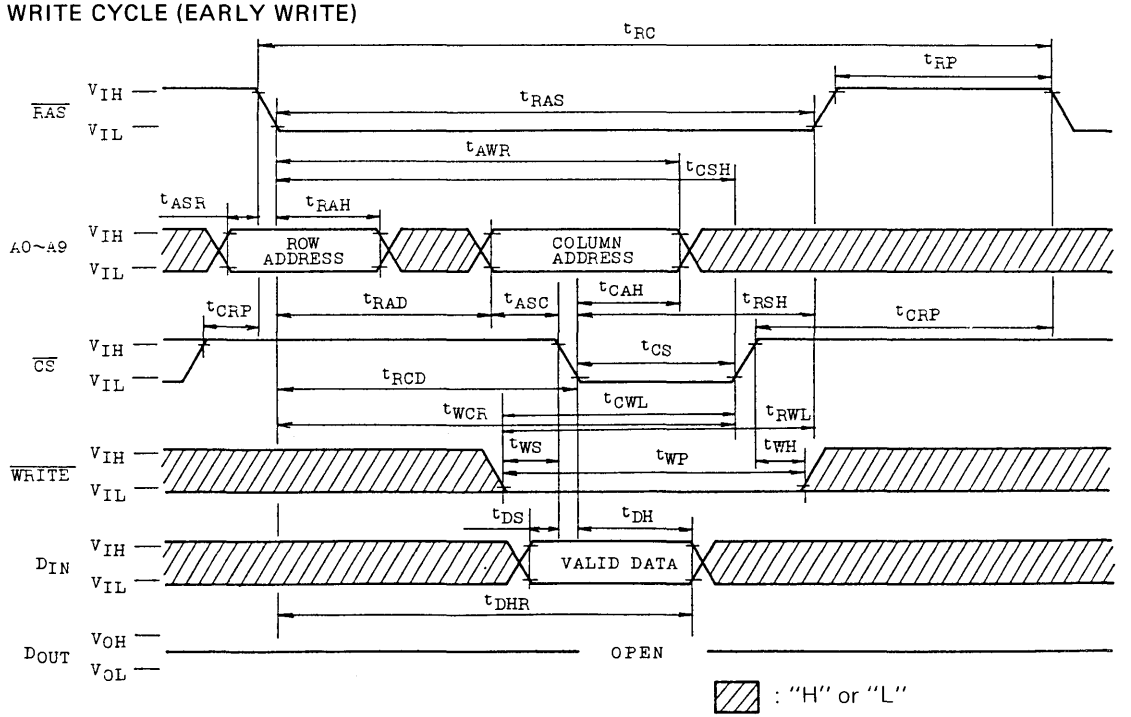
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T= 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AwD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater then the specified t_{RAD}(max.) limit, then access time is controlled by exclusively by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

- READ CYCLE

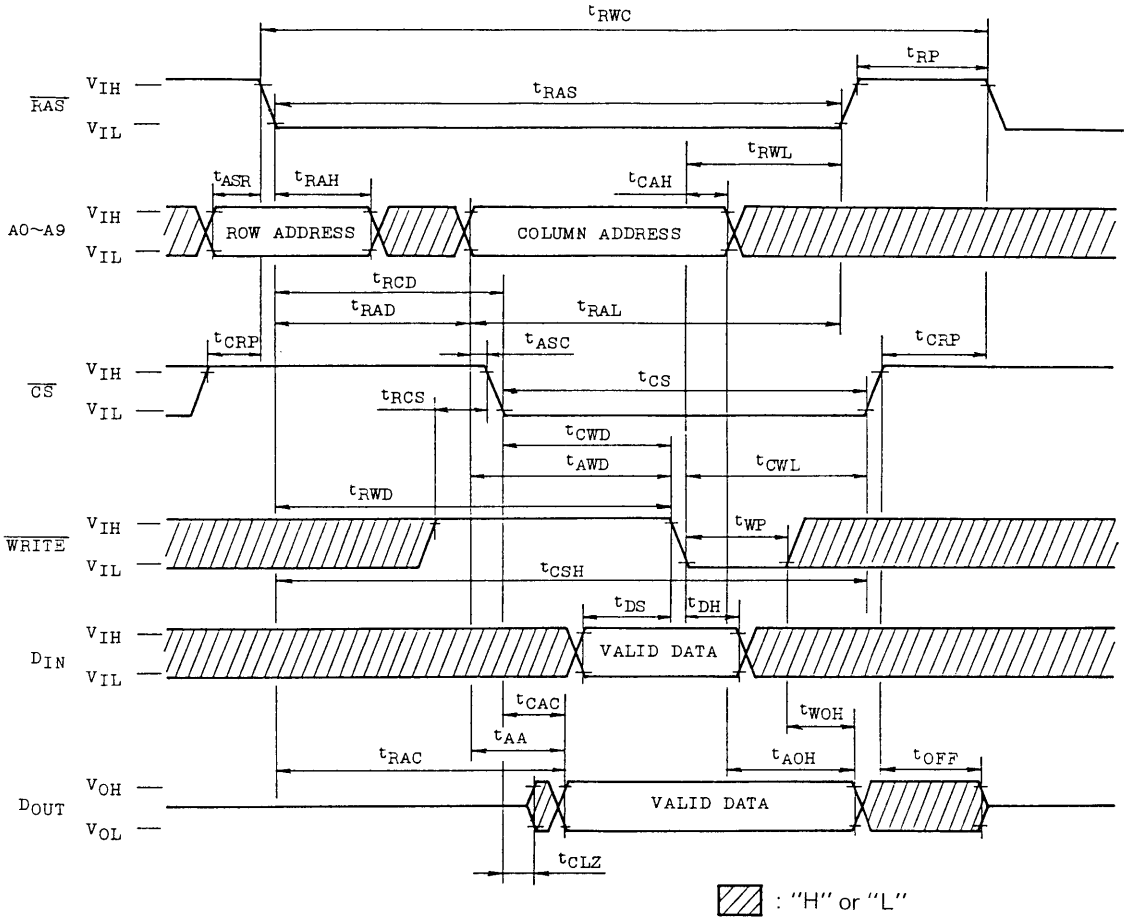


- WRITE CYCLE (EARLY WRITE)



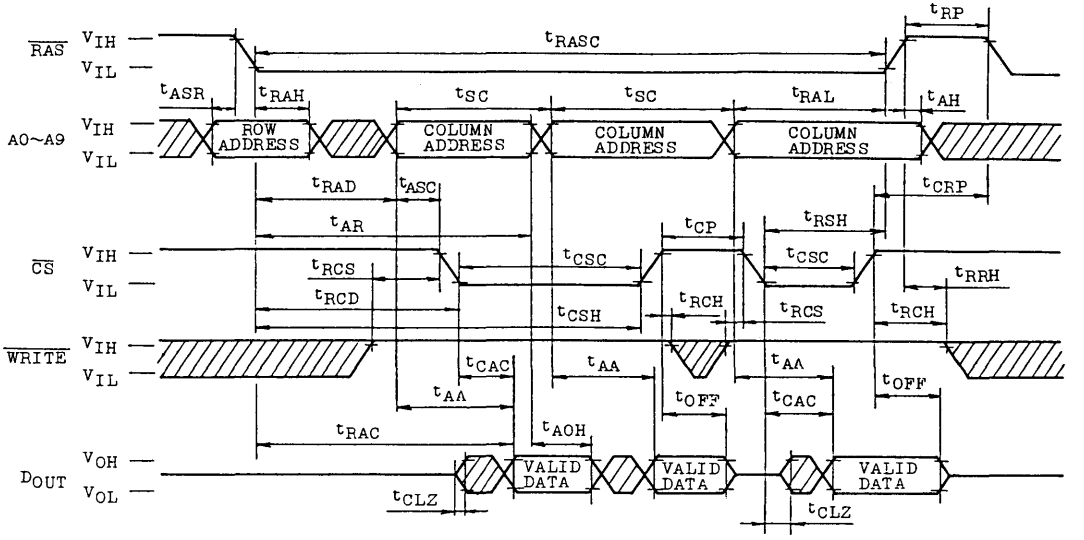
NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- READ-WRITE CYCLE

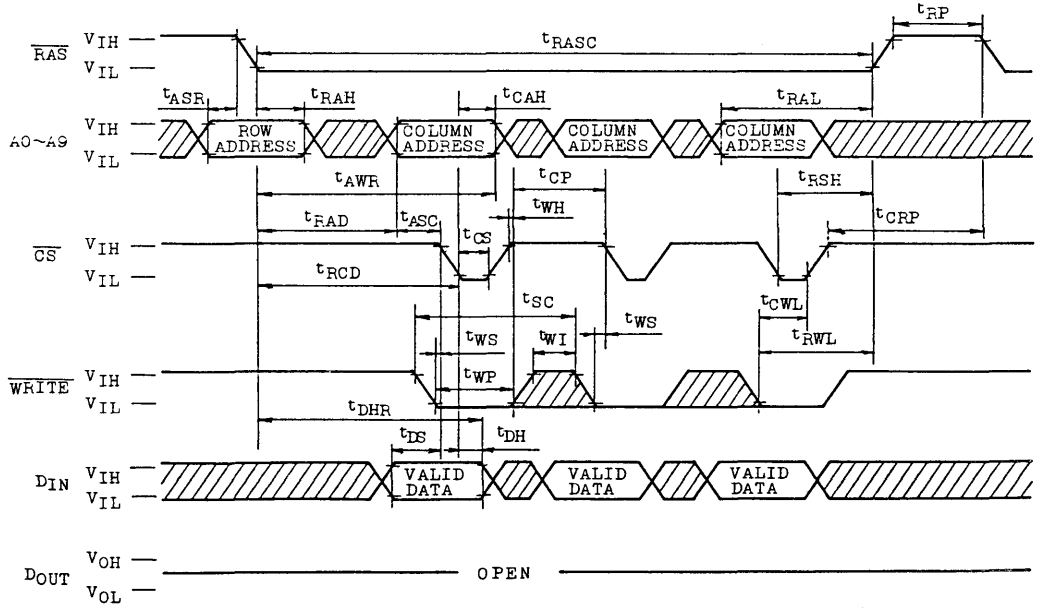


NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- STATIC COLUMN MODE READ CYCLE



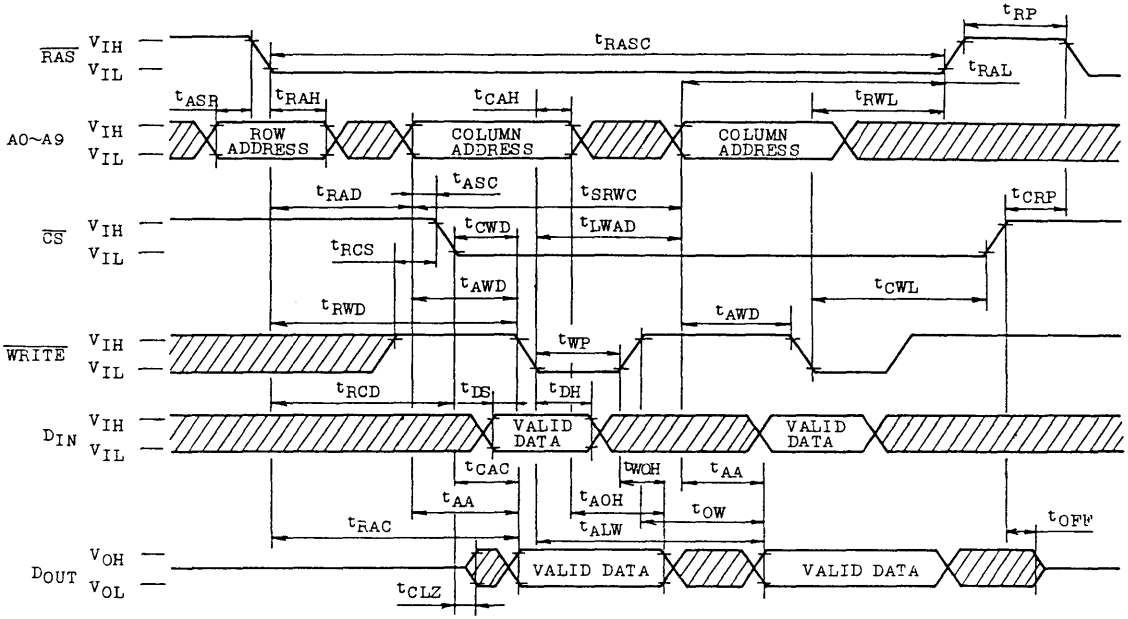
- STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



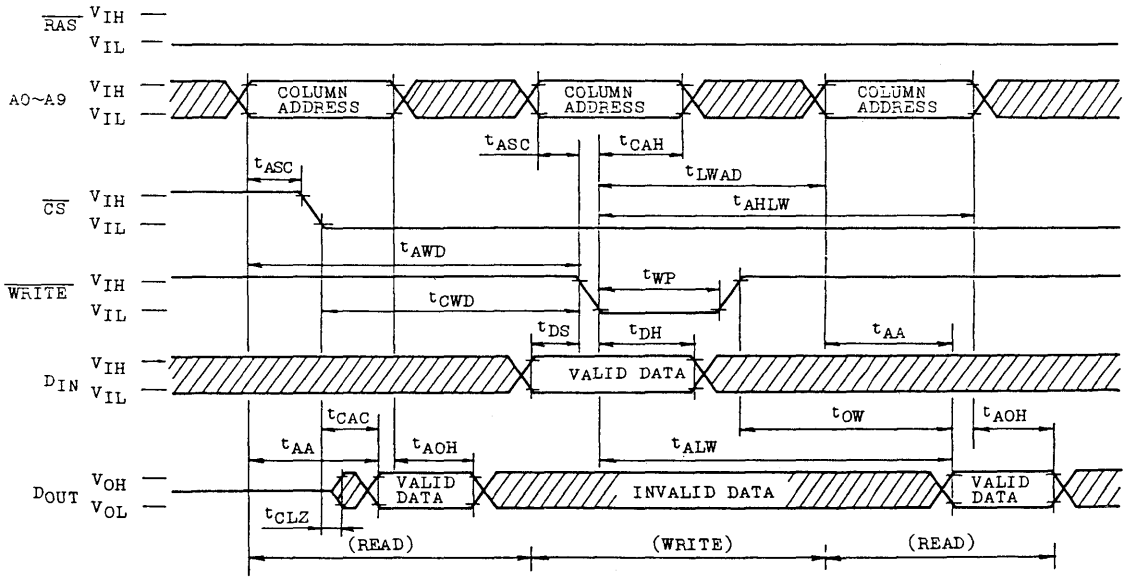
▨ : "H" or "L"

NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- STATIC COLUMN MODE READ-WRITE CYCLE



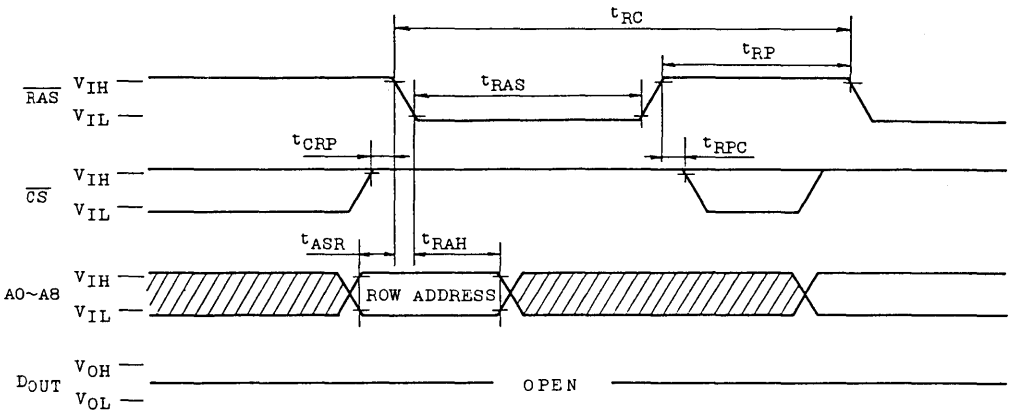
- STATIC COLUMN MODE READ/WRITE MIXED CYCLE



▨ : "H" or "L"

NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

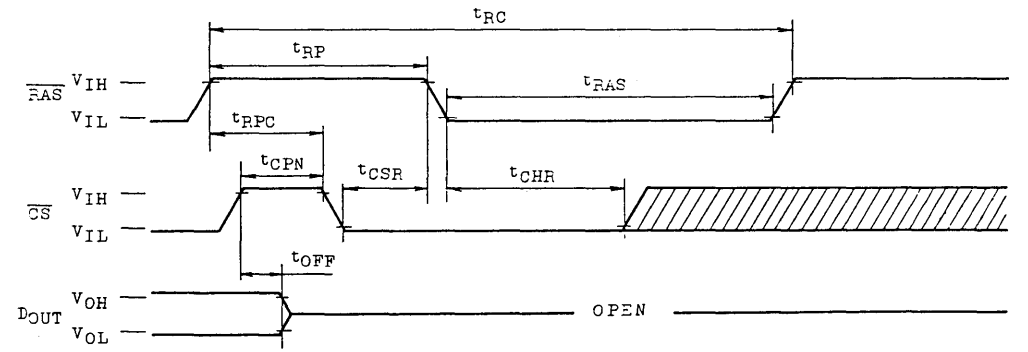
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

▨ : "H" or "L"

- $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

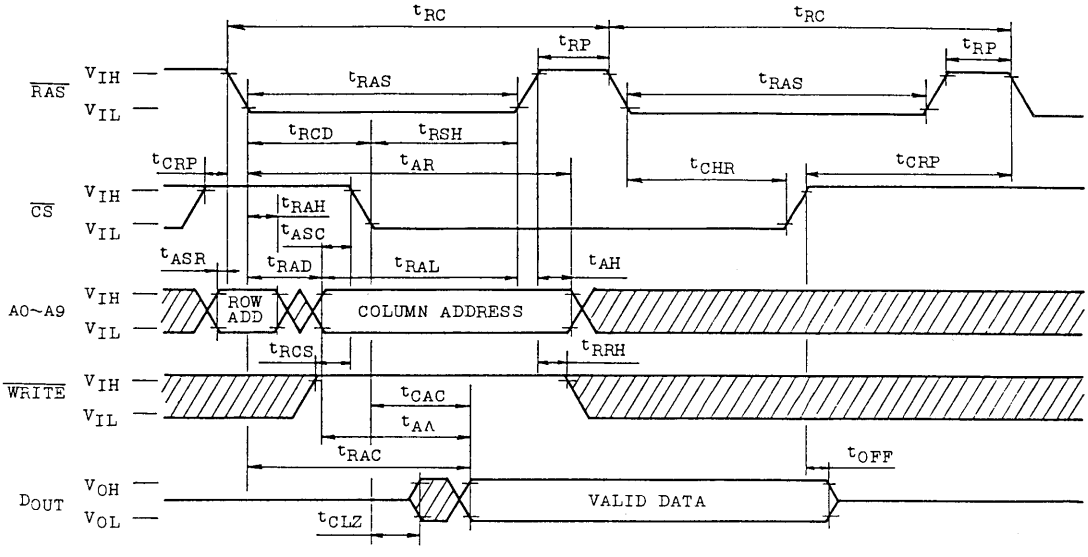


▨ : "H" or "L"

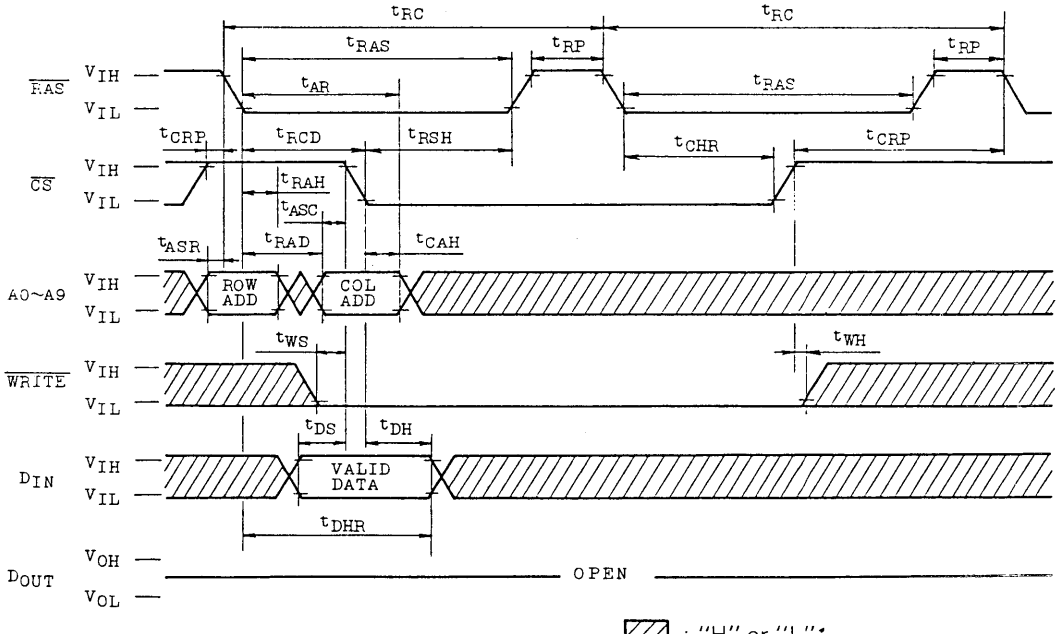
NOTE: $\overline{WRITE}$ = "H" or "L", A0 ~ A9 = "H" or "L"

"TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

- HIDDEN REFRESH CYCLE (READ)



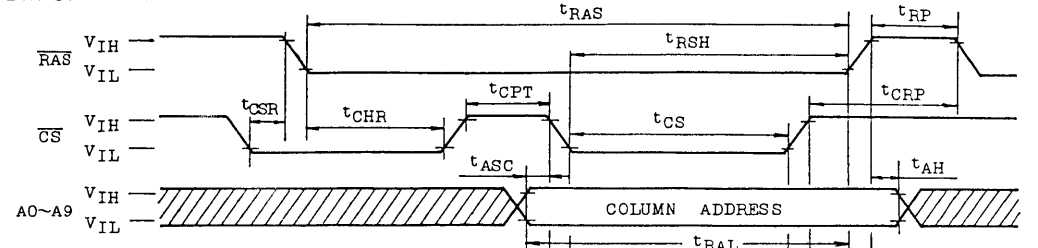
- HIDDEN REFRESH CYCLE (WRITE)



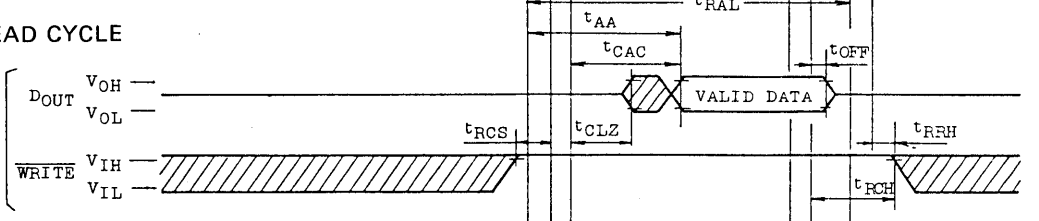
▨ : "H" or "L"

NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

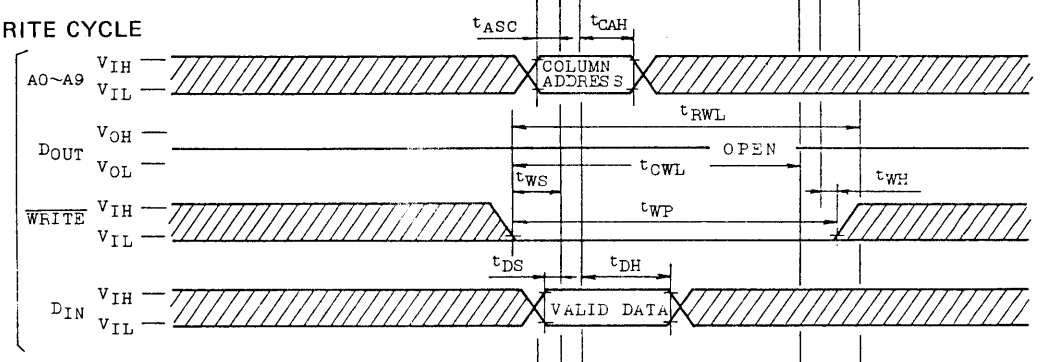
- $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



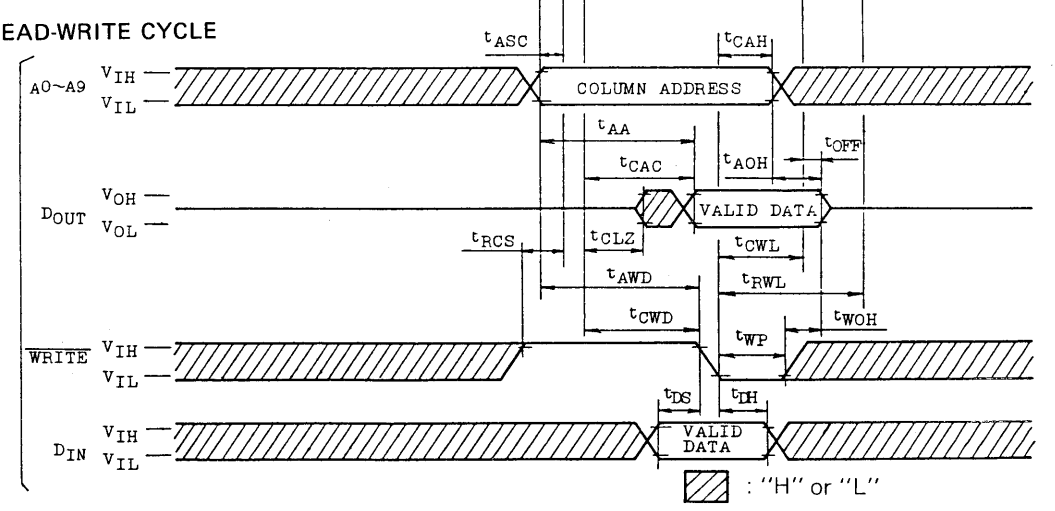
- READ CYCLE



- WRITE CYCLE



- READ-WRITE CYCLE



NOTE: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

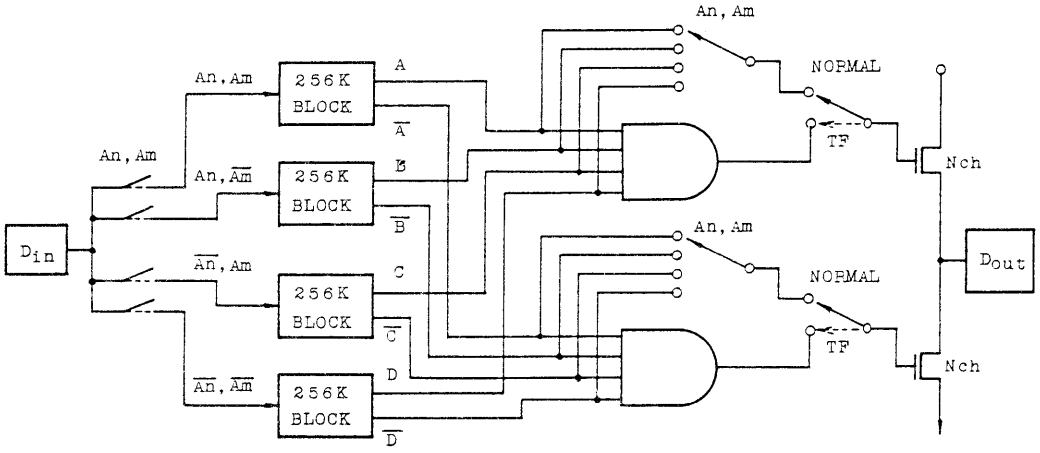
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000/1/2 is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bits.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode

TF Pin = Low level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

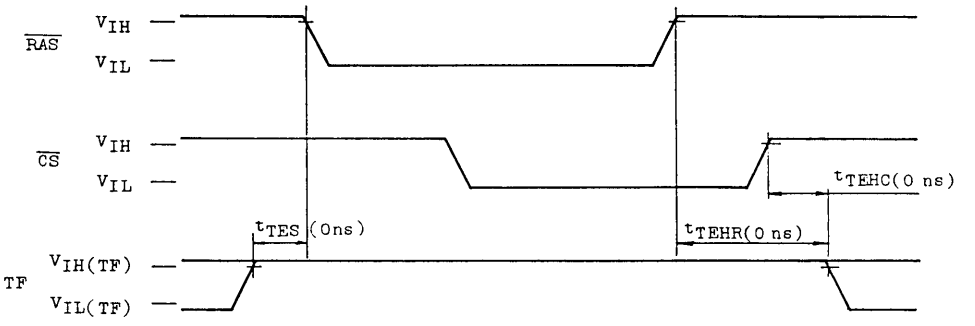
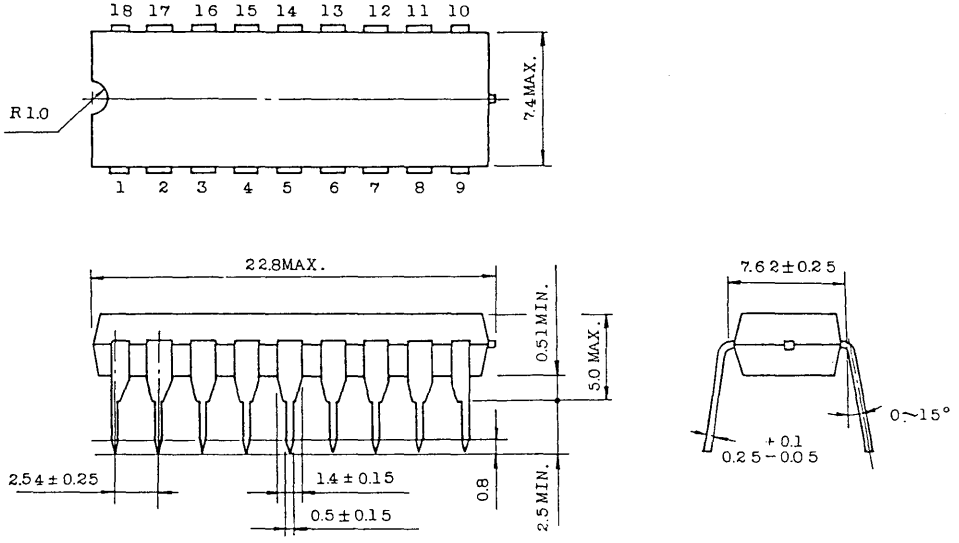


Fig. 2 Test Mode Cycle

OUTLINE DRAWINGS

- Plastic DIP

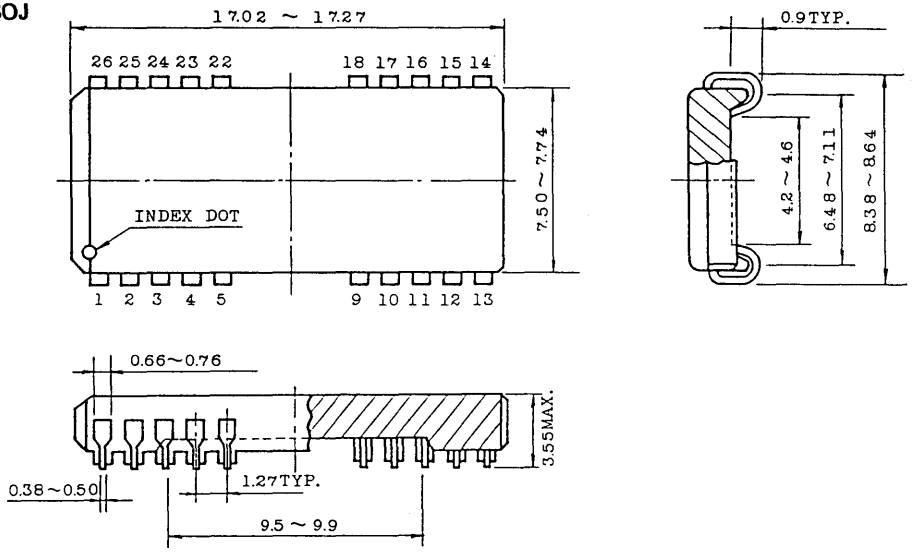
Unit in mm



NOTE: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.
All dimensions are in millimeters.

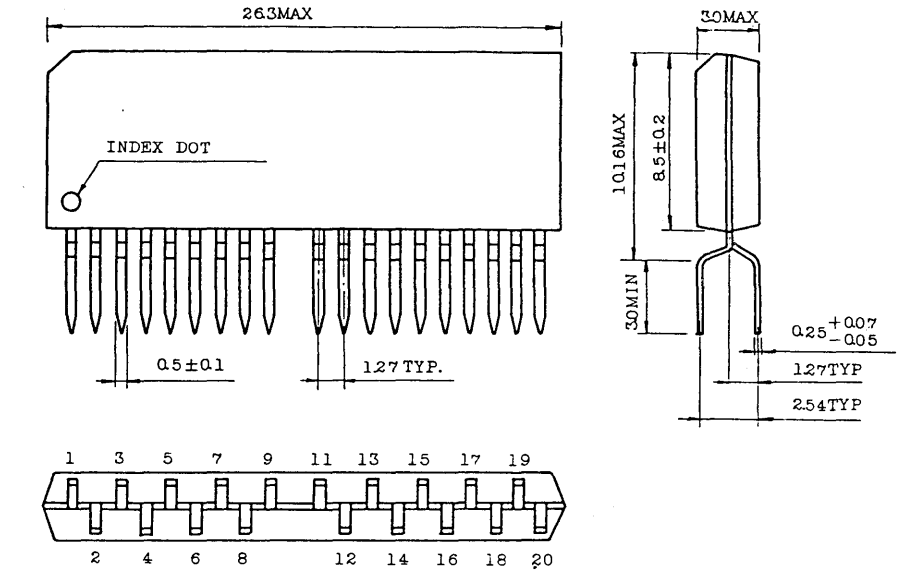
Unit in mm

- **Plastic SOJ**



- **Plastic ZIP**

Unit in mm



NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC511002AP/AJ/AZ-70, TC511002AP/AJ/AZ-80
TC511002AP/AJ/AZ-10

DESCRIPTION

The TC511002AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advnaced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ nad 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

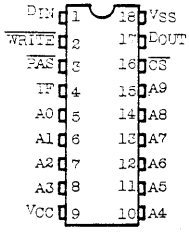
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511002AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

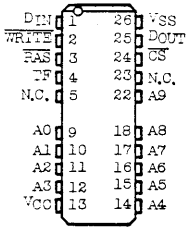
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  440mW MAX. Operating (TC511002AP/AJ/AZ-70)
  385mW MAX. Operating (TC511002AP/AJ/AZ-80)
  330mW MAX. Operating (TC511002AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC511002AP
  Plastic SOJ: TC511002AJ
  Plastic ZIP: TC511002AZ

PIN CONNECTION (TOP VIEW)

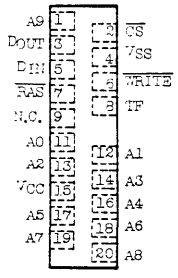
Plastic DIP



Plastic SOJ



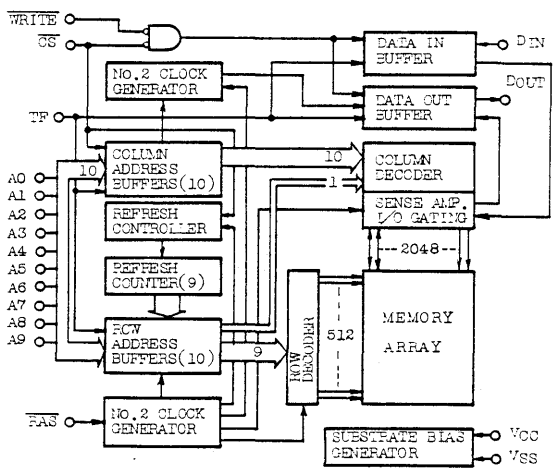
Plastic ZIP



PIN NAMES

A0∿A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	-1 ∿ 10.5	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC}+4.5	-	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	-1.0		V_{CC}+0.1	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC511002AP/AJ/AZ-70	-	80	mA	3,4
		TC511002AP/AJ/AZ-80	-	70		
		TC511002AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC511002AP/AJ/AZ-70	-	80	mA	3
		TC511002AP/AJ/AZ-80	-	70		
		TC511002AP/AJ/AZ-10	-	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC511002AP/AJ/AZ-70	-	60	mA	3,4
		TC511002AP/AJ/AZ-80	-	50		
		TC511002AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC511002AP/AJ/AZ-70	-	80	mA	3
		TC511002AP/AJ/AZ-80	-	70		
		TC511002AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IH} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN(TF)}$ ≦ V_{CC}+0.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ +5.5V)		-10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC}+4.5V ≦ $V_{IN(TF)}$ ≦ 10.5V)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C)(Notes 5, 6, 7)

SYMBOL	PARAMETER	TC511002 AP/AJ/AZ-70		TC511002 AP/AJ/AZ-80		TC511002 AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RWC}	Read-Write Cycle Time	155	-	155	-	210	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	50	-	ns	
t_{SRWC}	Static Column Mode Read Write Cycle Time	70	-	80	-	100	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	-	20	-	25	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	100,000	20	100,000	25	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	80	-	90	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC511002 AP/AJ/AZ-70		TC511002 AP/AJ/AZ-80		TC511002 AP/AJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	5	-	10	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	20	-	25	-	ns	
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	15
t_{AHLW}	Last Write to Column Address Hold Time	65	-	75	-	95	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	20	-	20	-	25	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-WRITE CYCLE)	70	-	80	-	100	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	-	40	-	50	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	40	-	40	-	50	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

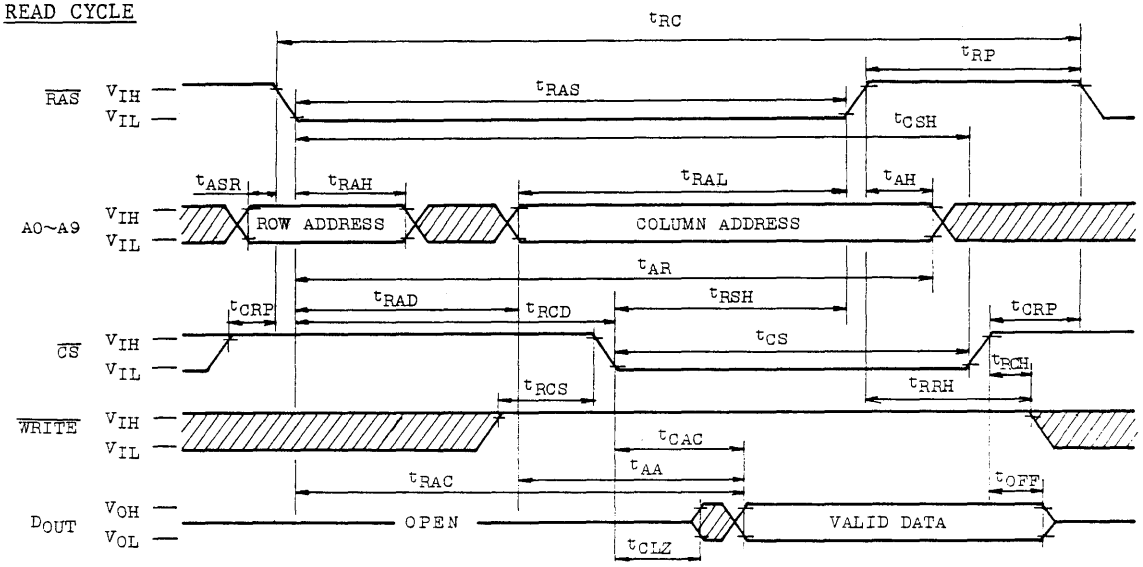
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

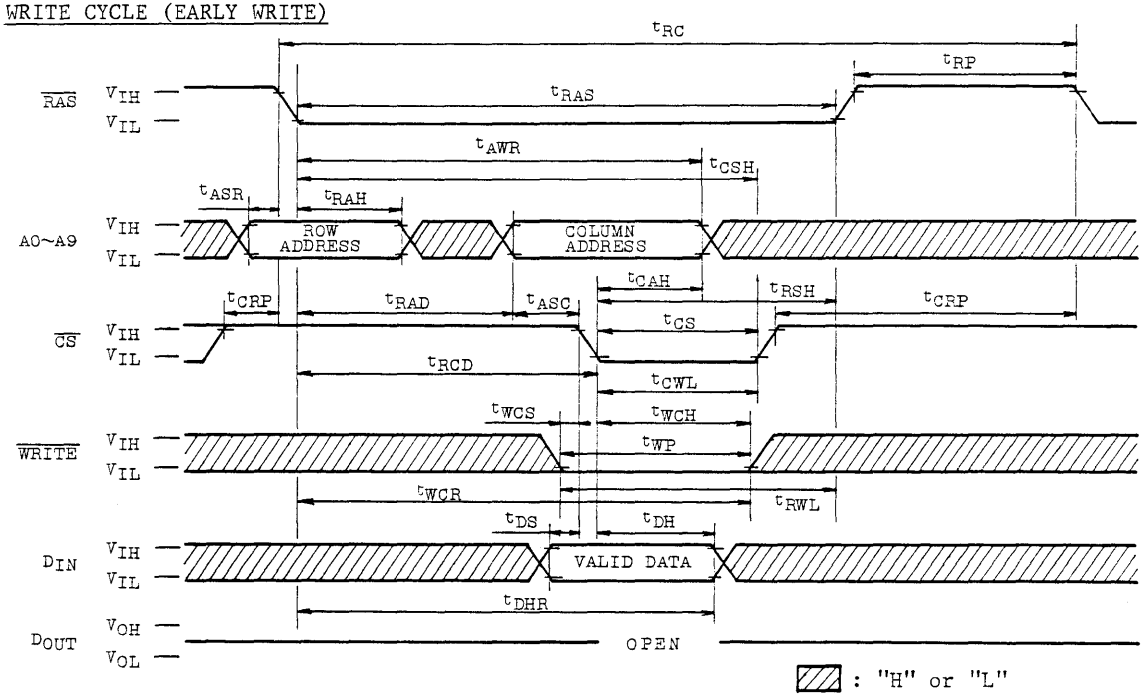
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
   In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-write cycles.
12. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.) and $t_{WCH} \geqq t_{WCH}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither or the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(min.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

READ CYCLE



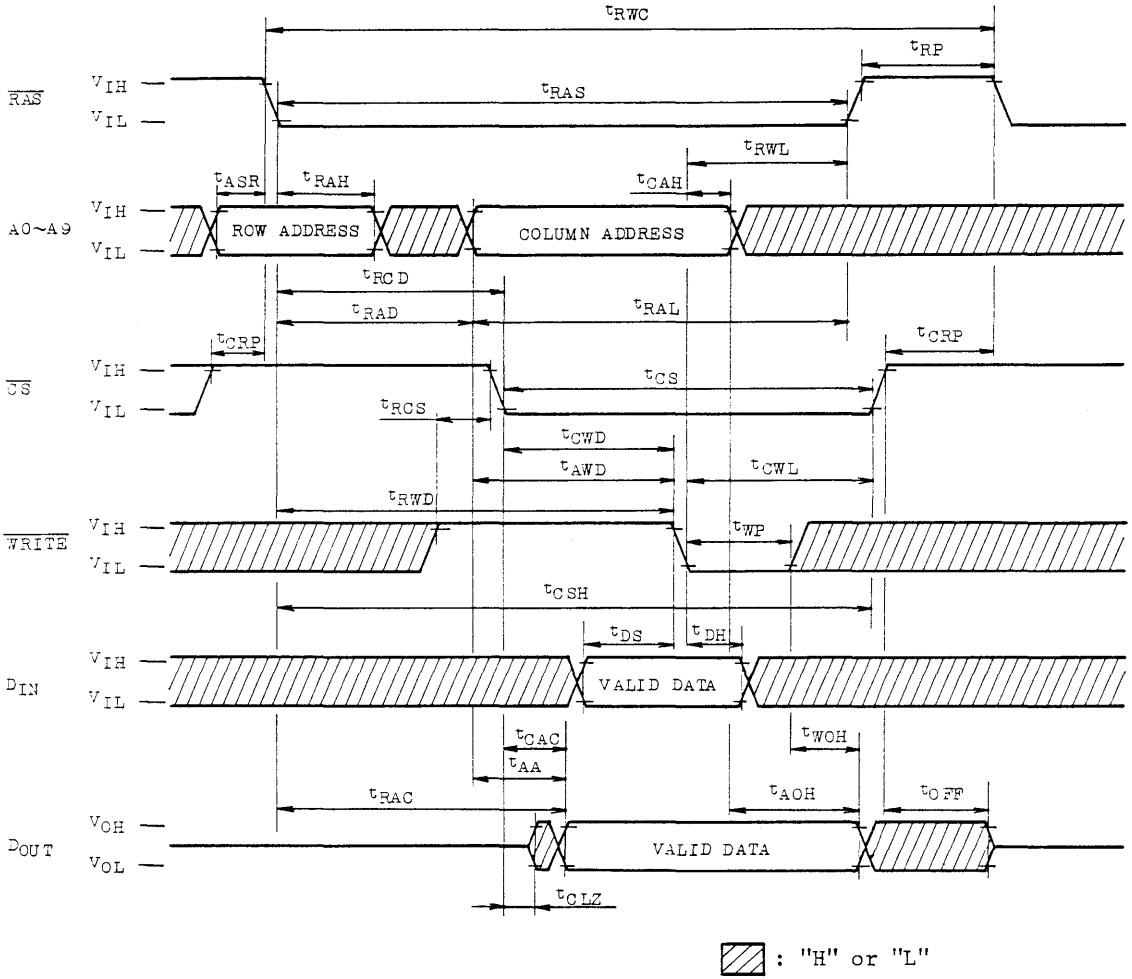
WRITE CYCLE (EARLY WRITE)



▨ : "H" or "L"

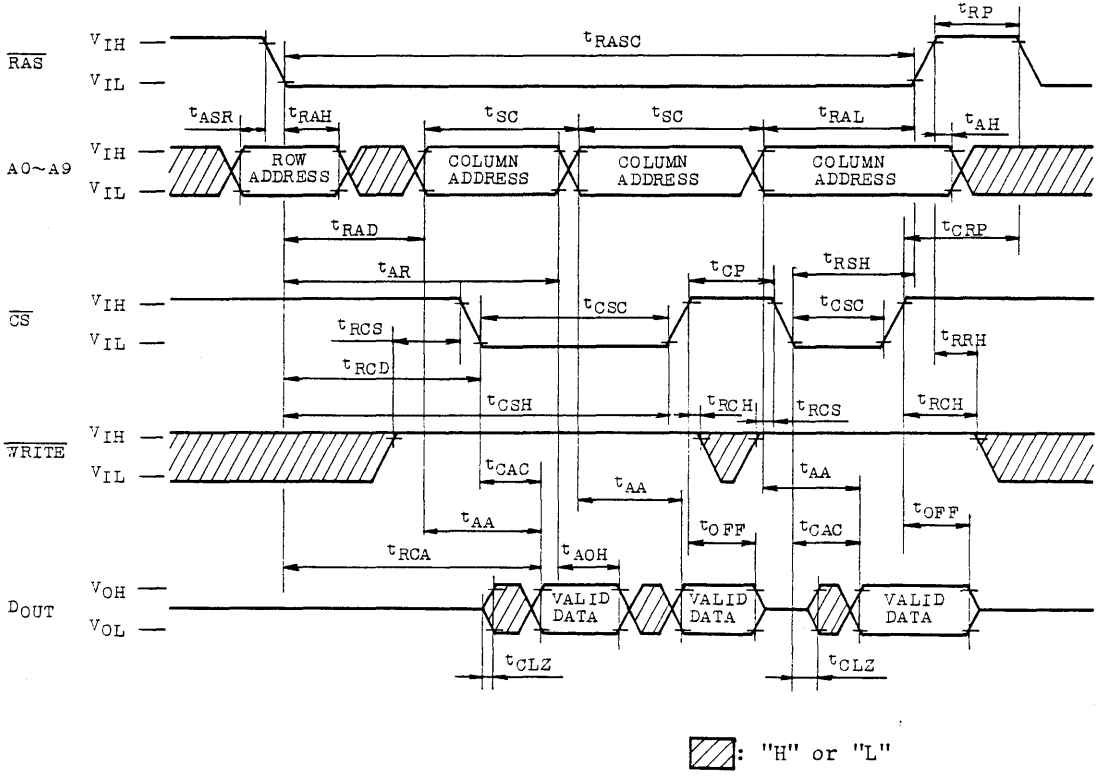
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

READ-WRITE CYCLE



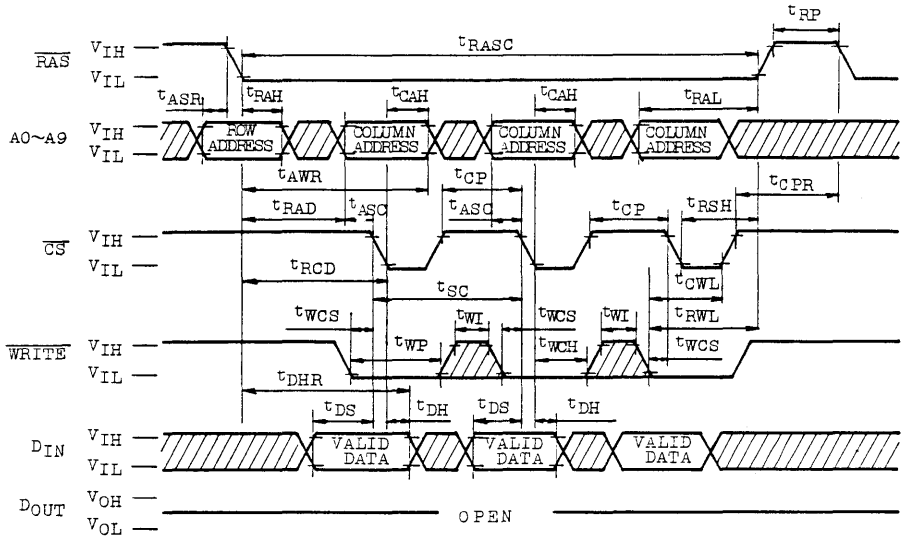
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ CYCLE

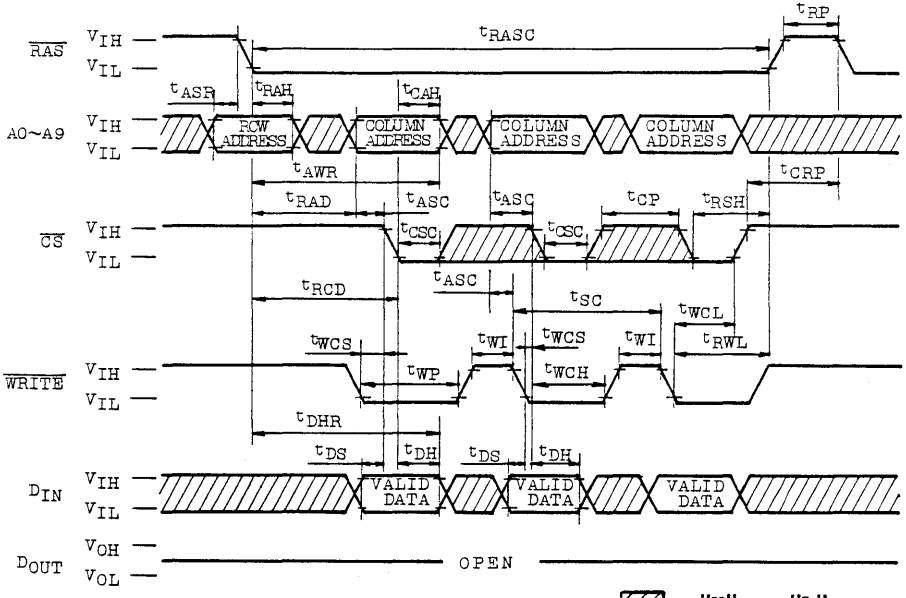


NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

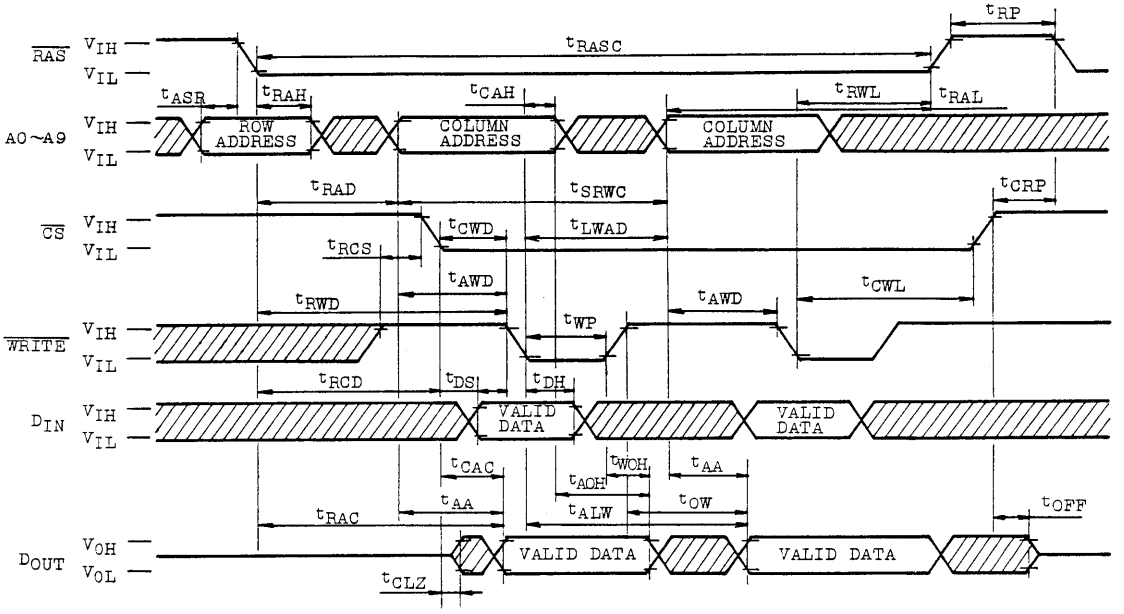


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

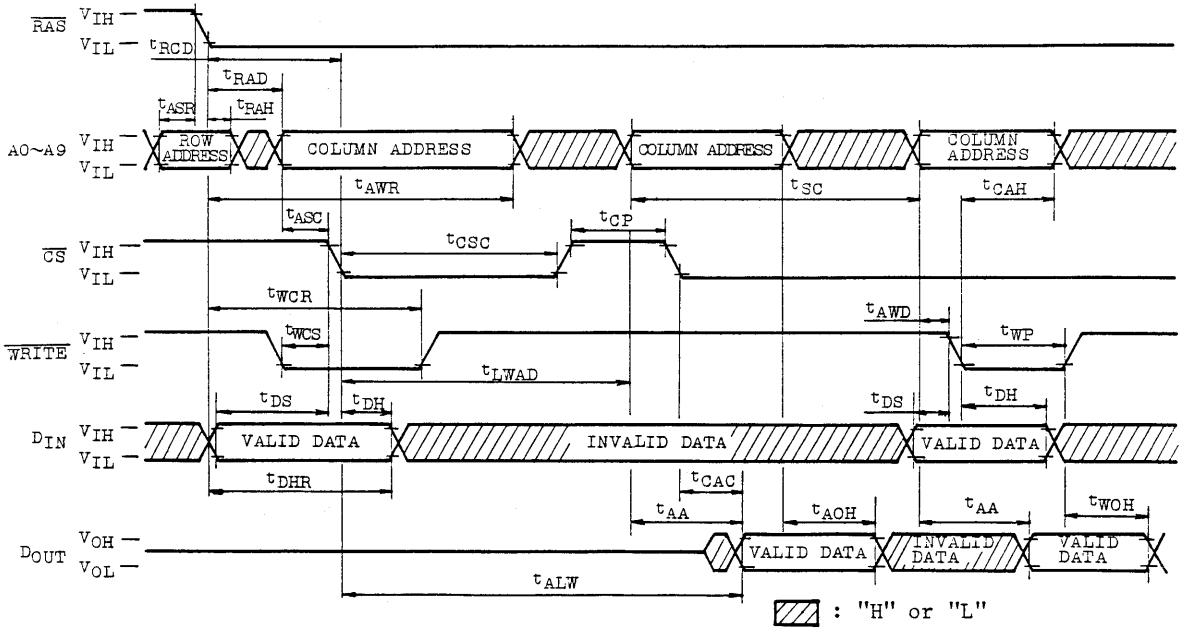


NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-WRITE CYCLE

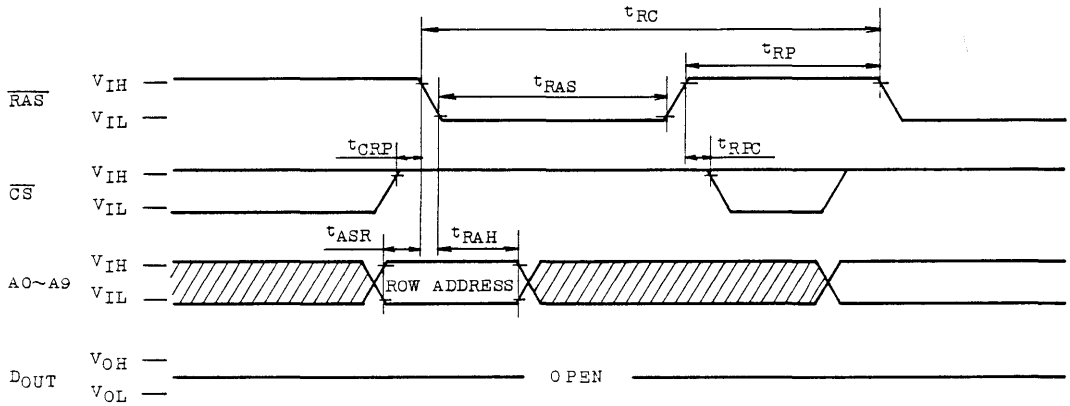


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



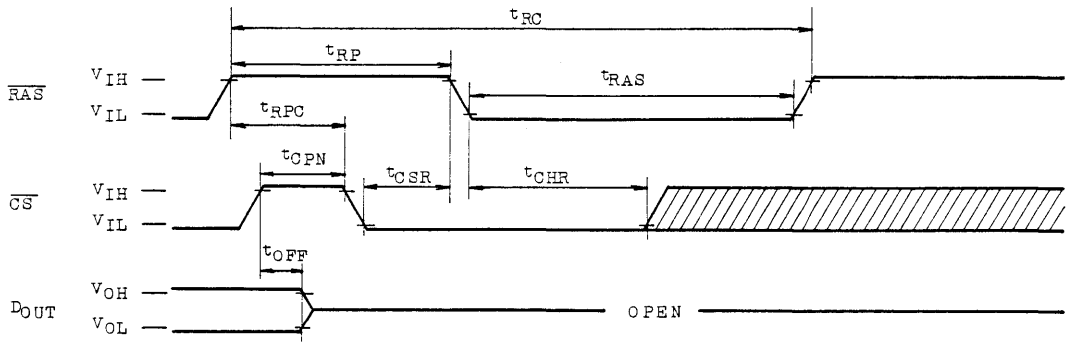
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨: "H" or "L"

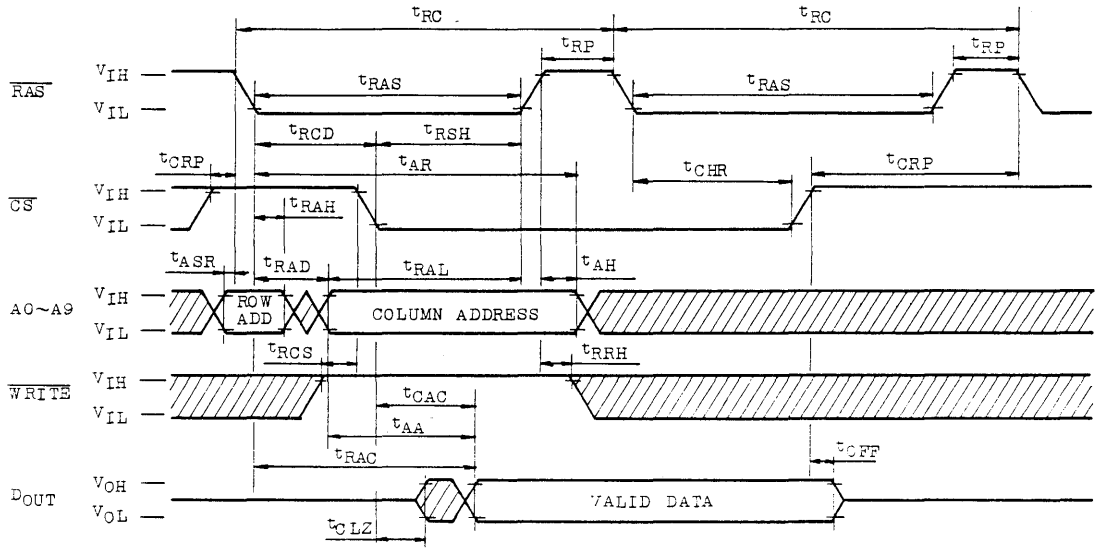
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



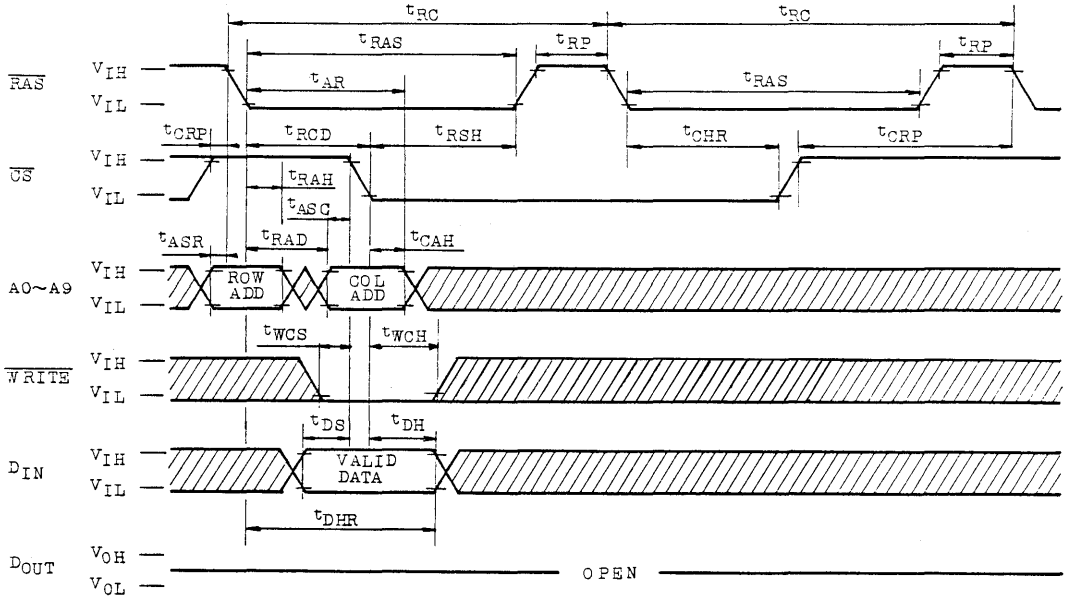
NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L" ▨ : "H" or "L"

"TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



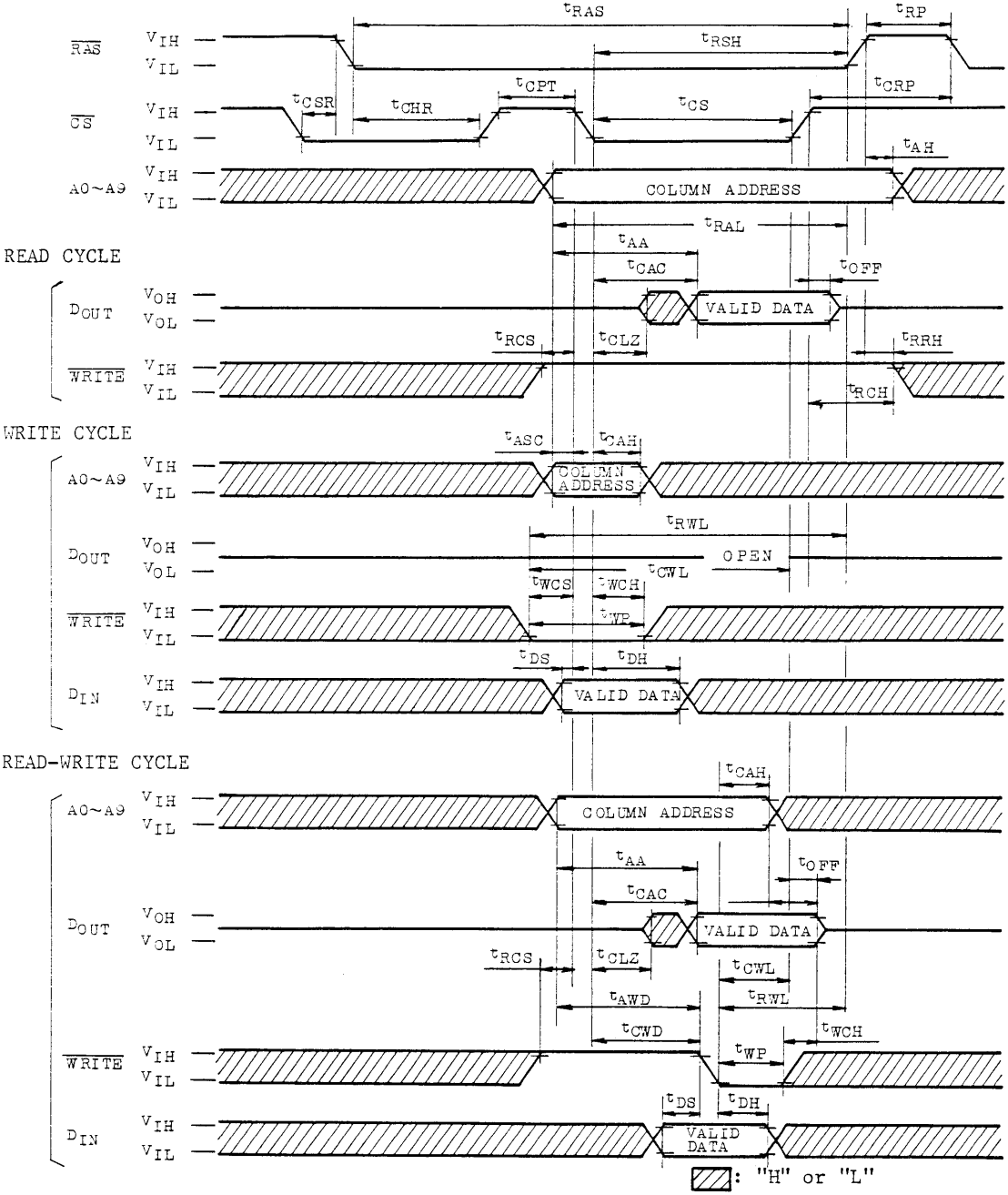
HIDDEN REFRESH CYCLE (WRITE)



▨: "H" or "L"

NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not sued.

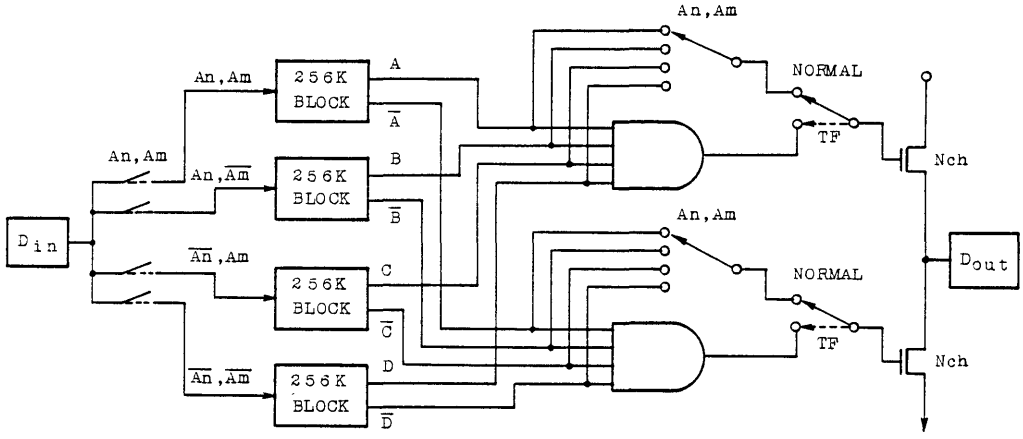
DESCRIPTION OF THE TEST MODE FOR 1M DRAMS

The TC511000A/1A/2A is a CMOS DRAM organized as 1,048,576 words by 1-bit. It is internally organized as 262,144 words by 4-bit.

The "Test Mode" function allows for a 1M DRAM to be tested virtually as if it were a 256K DRAM. Figure 1 shows the block diagram of the "Test Mode" circuit. Data is written into the four 256K blocks in parallel and is retrieved the same way. A logical "and" operation is performed on the outputs of the four internal 256K blocks.

- o For a good device, the output data of the four internal blocks are identical to the input data (all "H" or all "L") and consequently the same data will appear on the output pin.
- o For a bad device, the output data of one or more of the internal blocks will differ from the input data and a high impedance state will be detected on the output pin.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode

TF Pin = V_{IL}(TF) level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	DOUT
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

The "Test Mode" function is enabled by applying a "Super Voltage" (VCC+4.5V, max. voltage=10.5V) on the "TF" pin for a specified period (tTES, tTEHR, and tTEHC as shown in figure 2). It can be used while operating in any mode, including static column and fast page modes. It achieves a 4:1 reduction in test time for N patterns and a 16:1 reduction in test time for N^2 patterns. The A9 address input is ignored during the "Test Mode".

During normal operation or when the "Test Mode" function is not used, the "TF" pin must be connected to VSS or TTL Logic Low Level, or left unconnected on the printed wiring board.

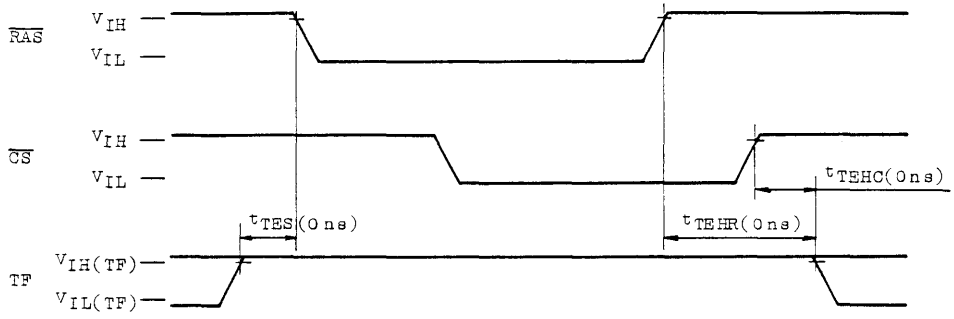
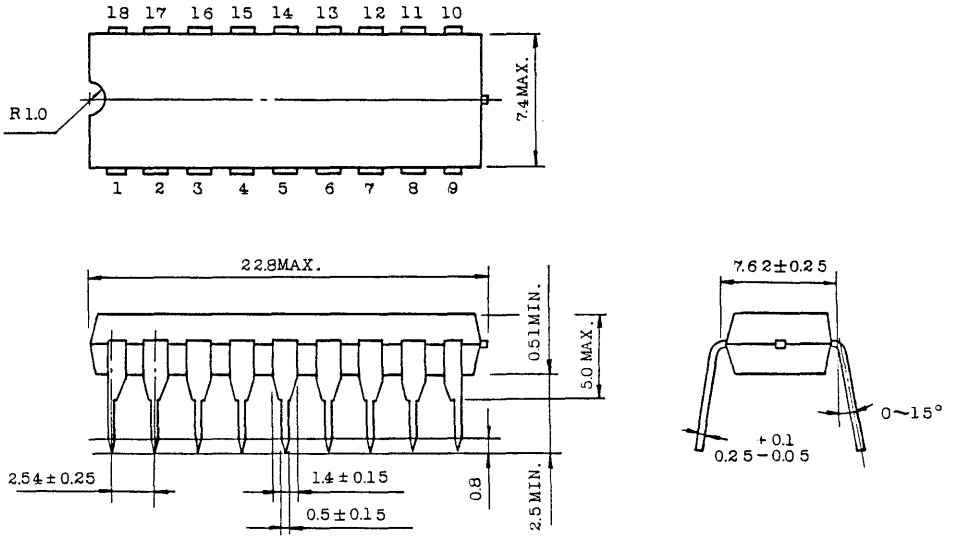


Fig.2 Test Mode Cycle

OUTLINE DRAWINGS

Plastic DIP

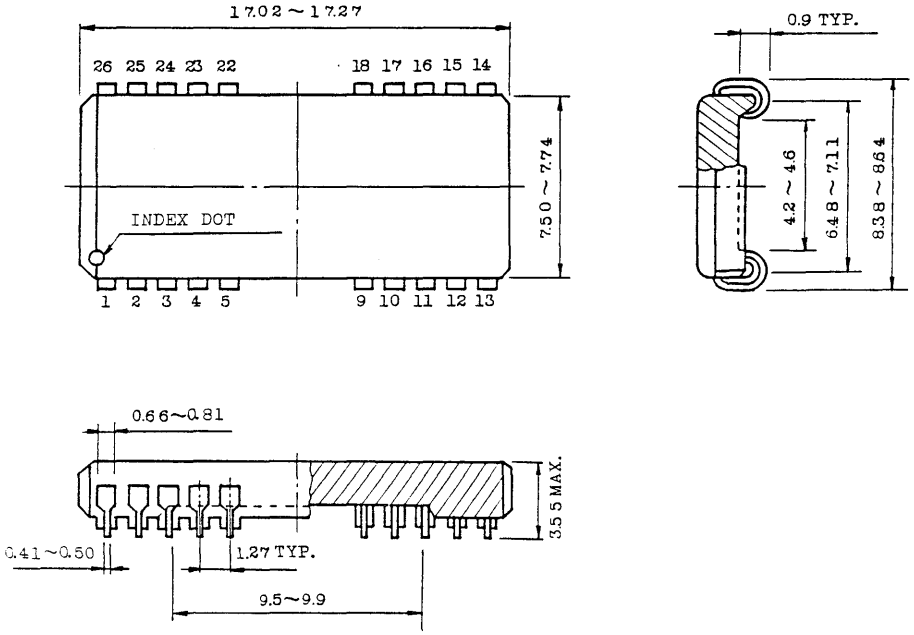
Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.18 leads. All dimensions are in millimeters.

Plastic SOJ

Unit in mm

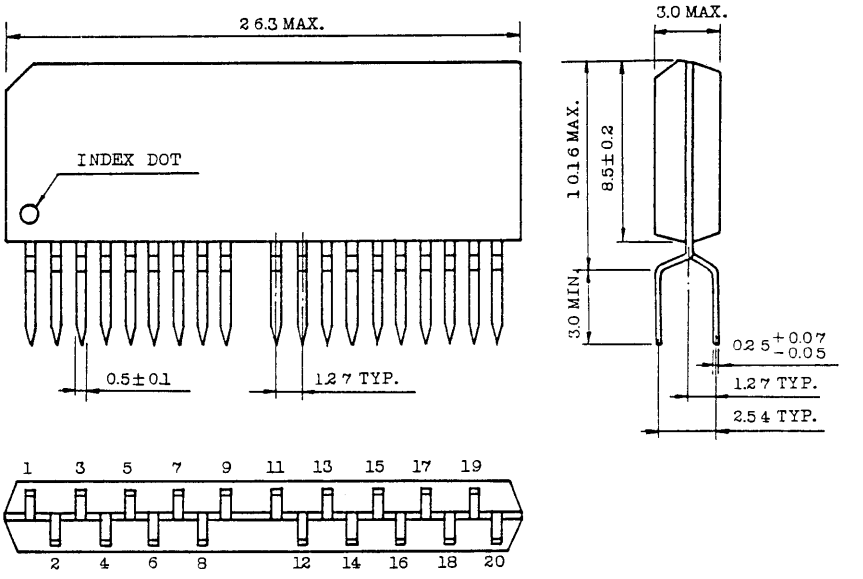


Note: Each lead pitch 1.27mm.

All dimensions are in millimeters.

Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry

262,144 WORD×4 BIT DYNAMIC RAM

SILICON GATE CMOS

TC514256P/J/Z-85, TC514256P/J/Z-10 TC514256P/J/Z-12

DESCRIPTION

The TC514256P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256 P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256P/J/Z to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

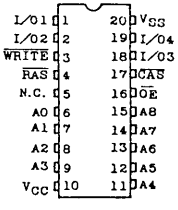
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256P/J/Z-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

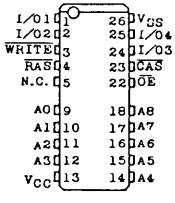
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  413mW MAX. Operating (TC514256P/J/Z-85)
  358mW MAX. Operating (TC514256P/J/Z-10)
  303mW MAX. Operating (TC514256P/J/Z-12)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP : TC514256P
  Plastic SOJ : TC514256J
  Plastic ZIP : TC514256Z

PIN CONNECTION (TOP VIEW)

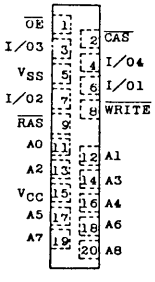
Plastic DIP



Plastic SOJ



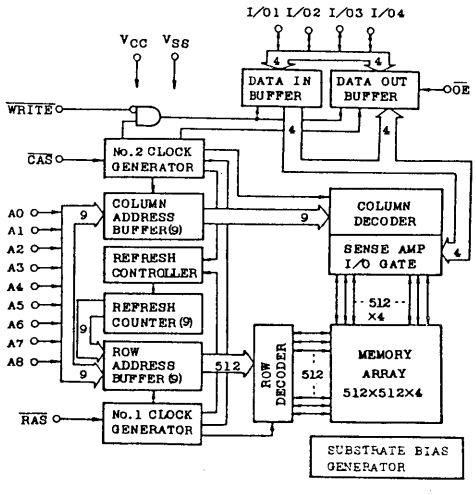
Plastic ZIP



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01 ~ I/04	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta = 0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $Ta = 0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514256P/J/Z-85	–	75	mA	3, 4
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514256P/J/Z-85	–	75	mA	3
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC514256P/J/Z-85	–	55	mA	3, 4
		TC514256P/J/Z-10	–	45		
		TC514256P/J/Z-12	–	35		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC}$-0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE RAS REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before RAS Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514256P/J/Z-85	–	75	mA	3
		TC514256P/J/Z-10	–	65		
		TC514256P/J/Z-12	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq V_{CC}$)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE ($I_{OUT} = -5mA$)		2.4	–	V	
I_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE ($I_{OUT} = 4.2mA$)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514256P/J/Z-85		TC514256P/J/Z-10		TC514256P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	–	255	–	295	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	70	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	–	115	–	140	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	30	–	35	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	65	ns	8, 14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	–	5	–	5	–	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to RAS	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data Hold Time	20	–	20	–	25	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514256P/J/Z-85		TC514256P/J/Z-10		TC514256P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CAS}$ to WRITE Delay Time	65	–	65	–	75	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	120	–	135	–	160	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	–	85	–	100	–	ns	12
t_{CSR}	CAS Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to OE	20	–	20	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

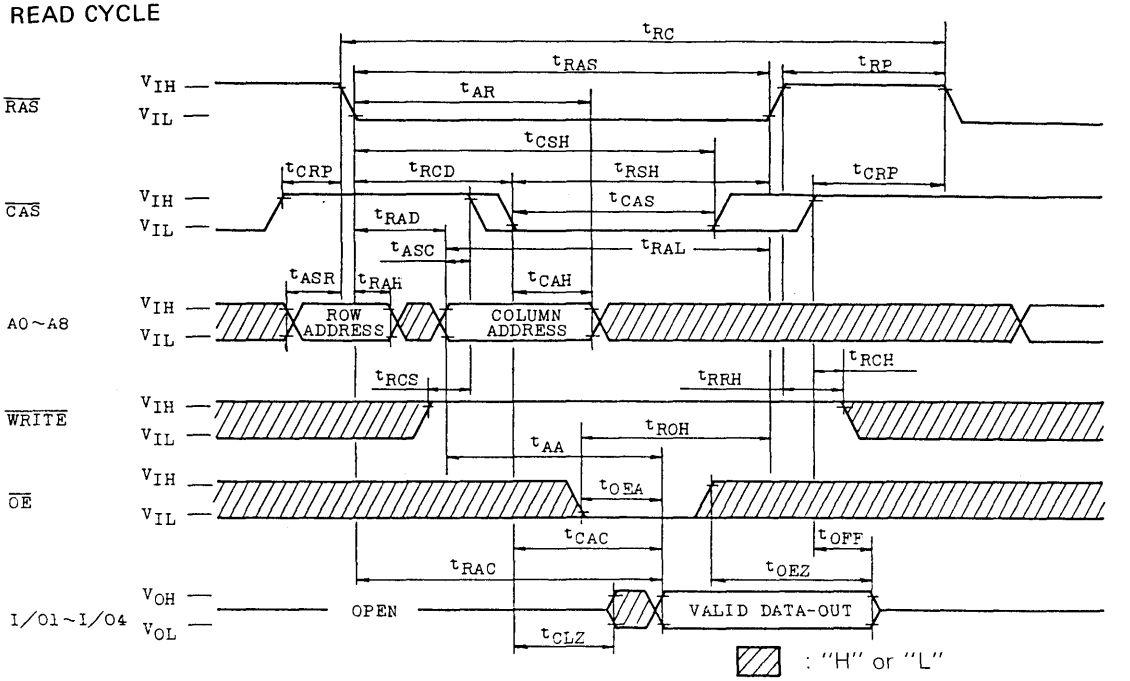
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1 MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 - A_8$)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Output Capacitance ($I/O_1 - I/O_4$)	–	7	pF

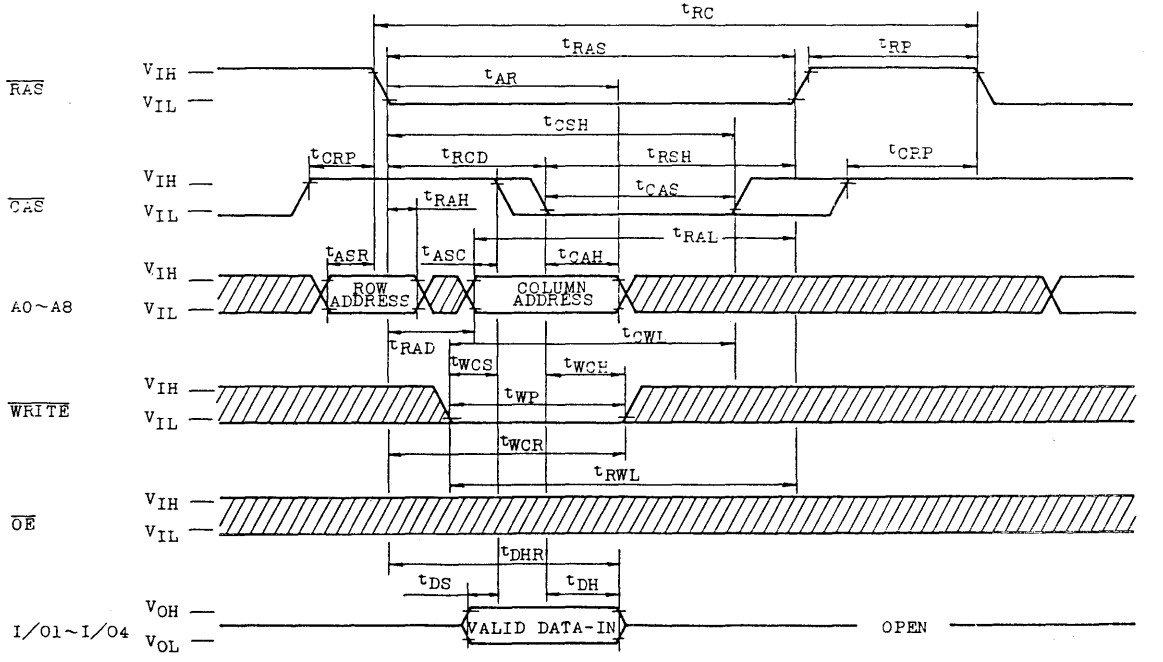
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

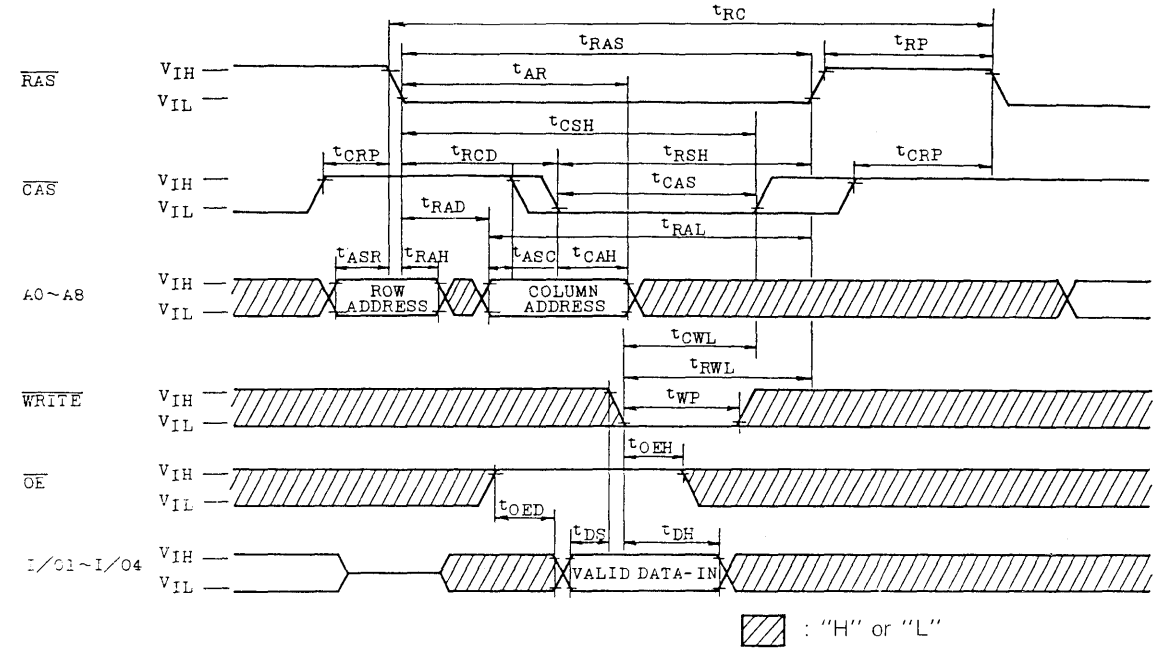
- READ CYCLE



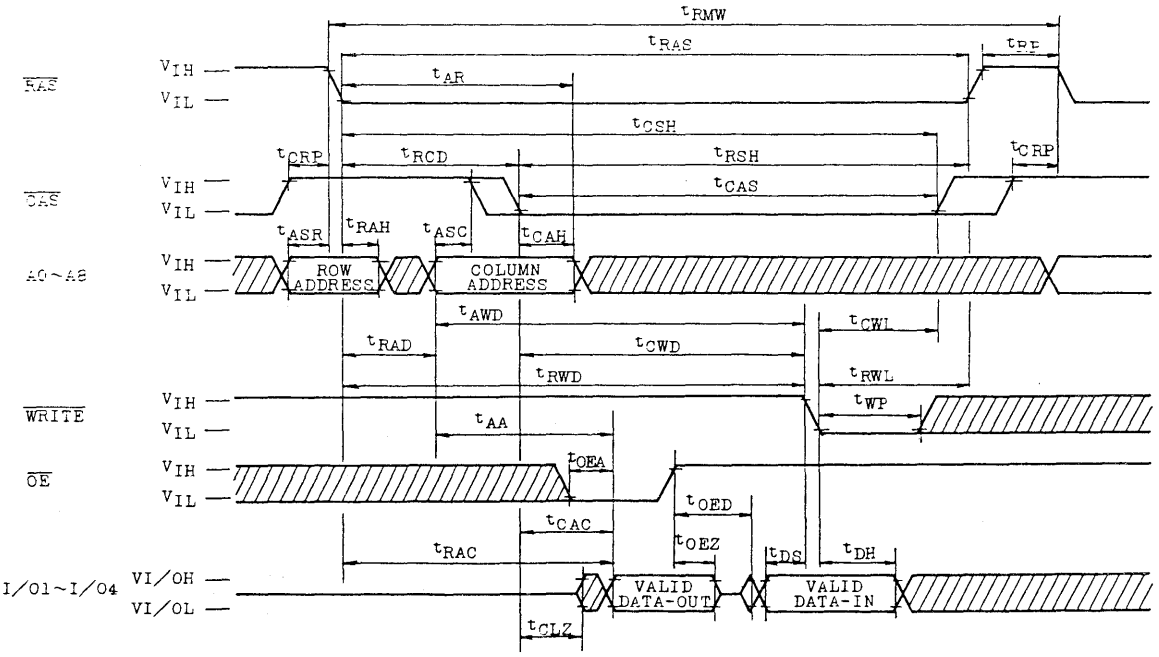
- WRITE CYCLE (EARLY WRITE)



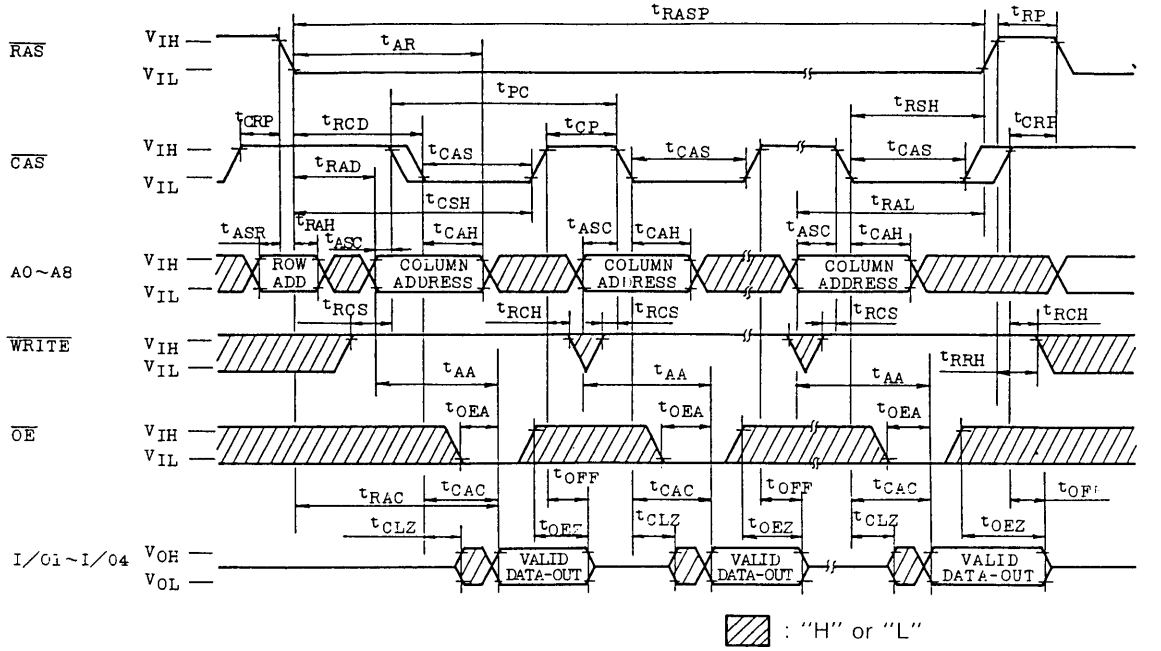
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



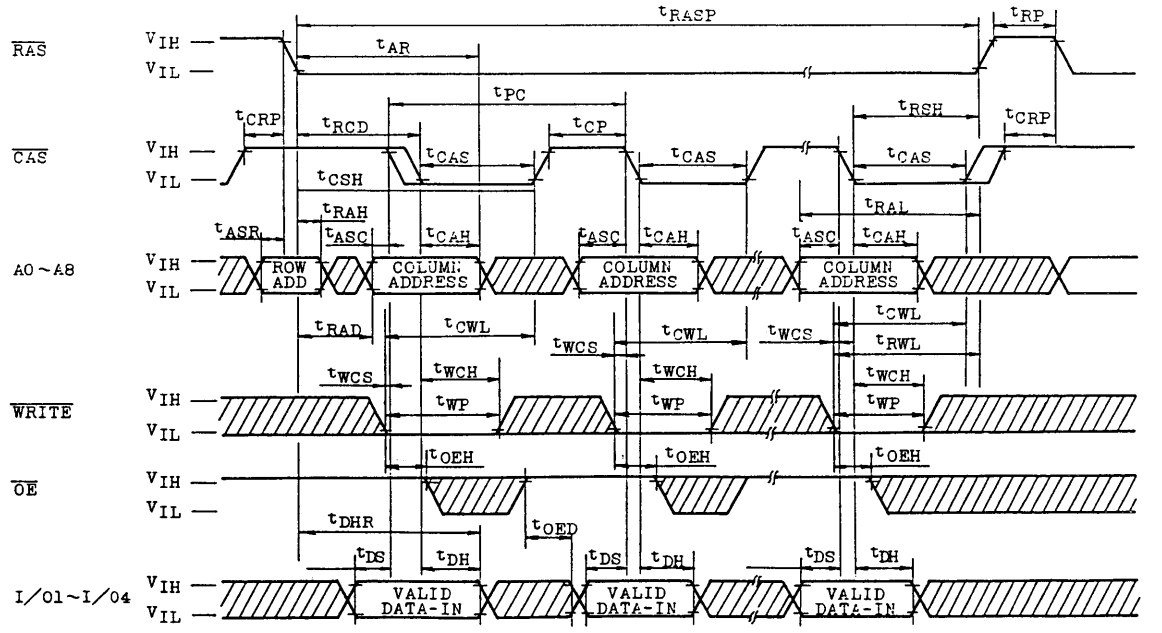
- READ-MODIFY-WRITE CYCLE



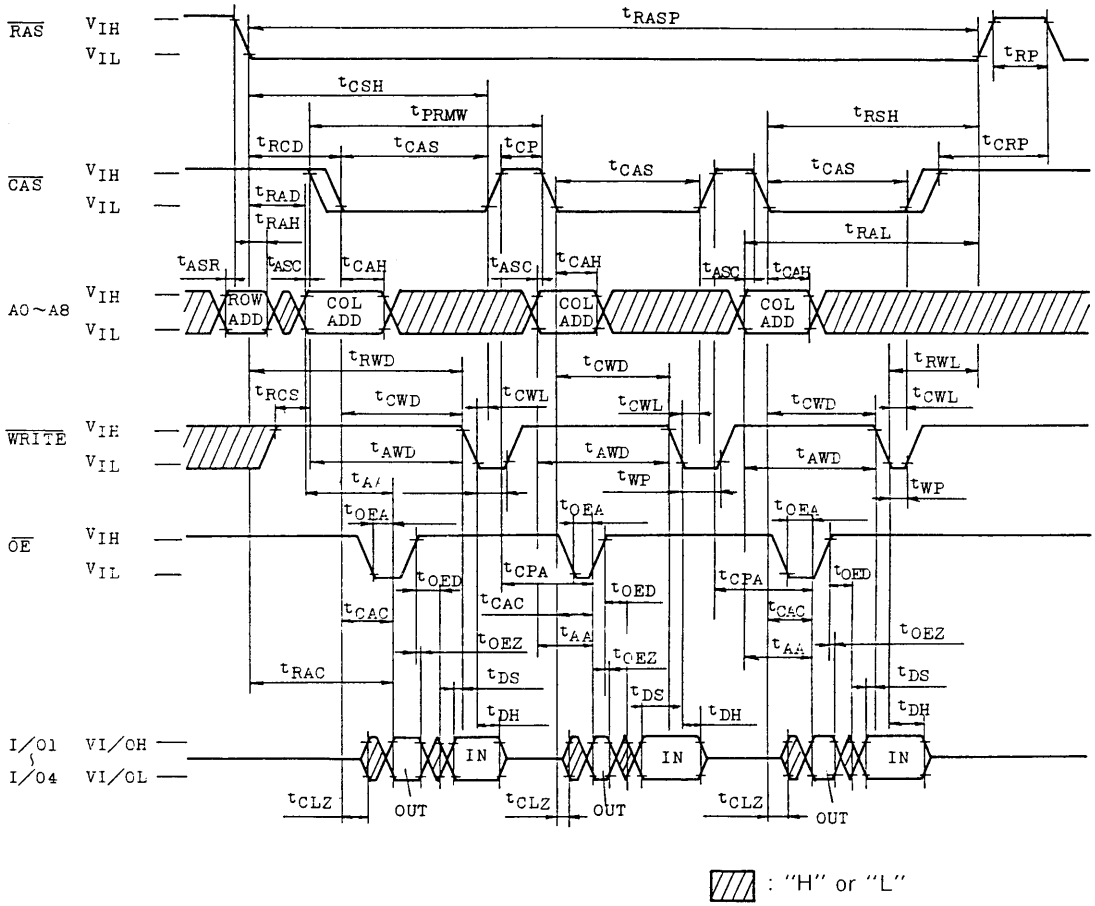
- FAST PAGE MODE READ CYCLE



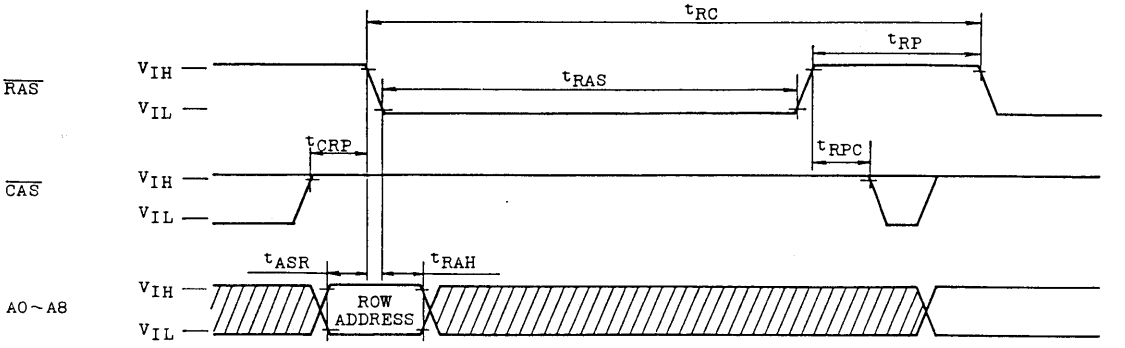
- FAST PAGE MODE WRITE CYCLE



- FAST PAGE MODE READ-MODIFY-WRITE CYCLE



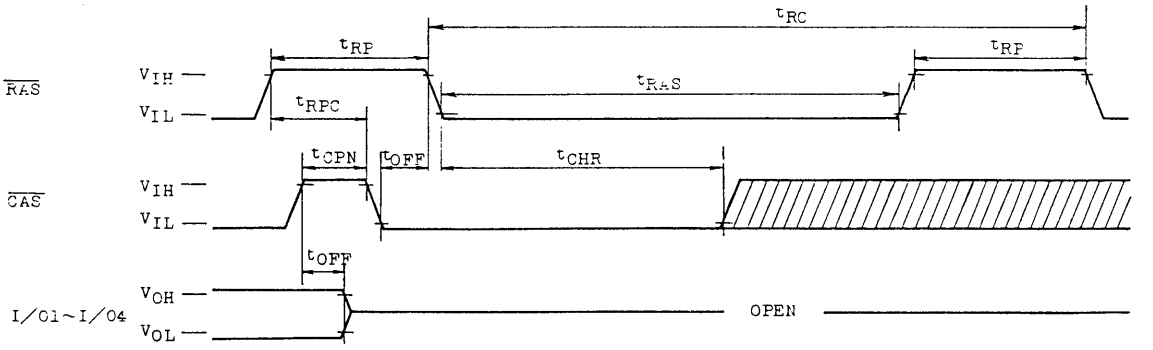
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: WRITE, OE = Don't care

▨ : "H" or "L"

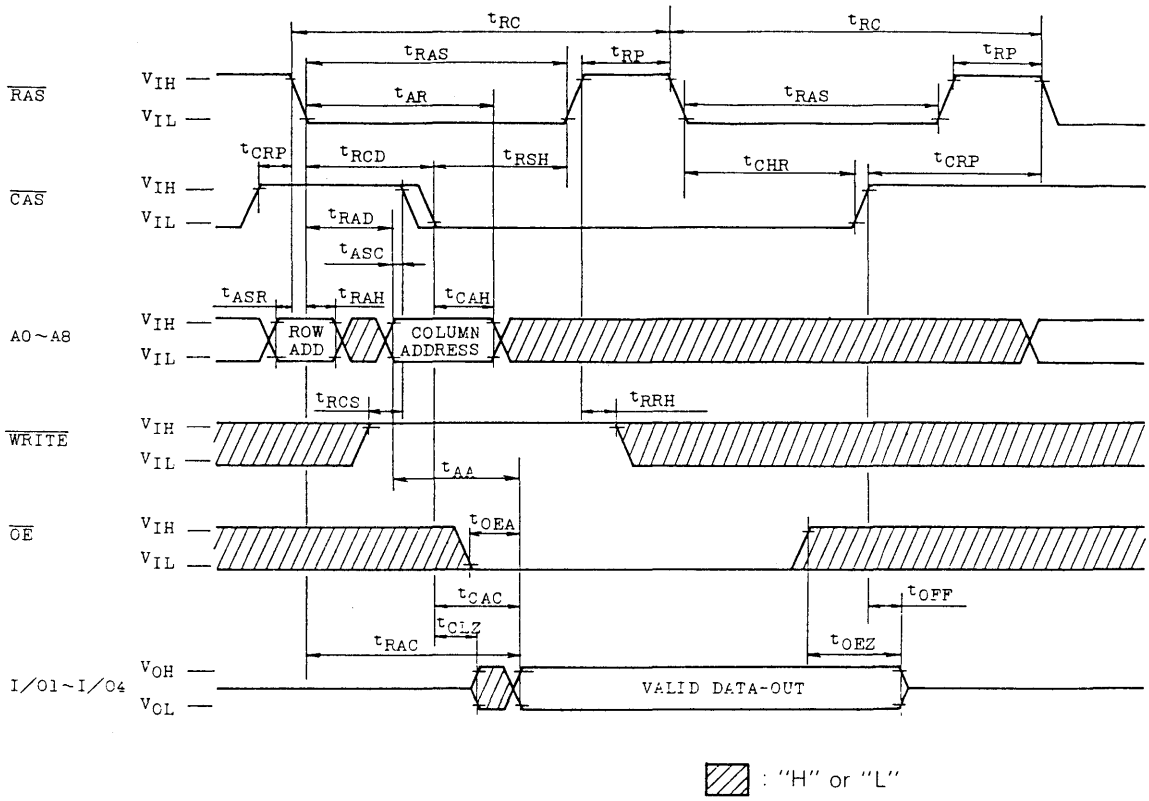
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



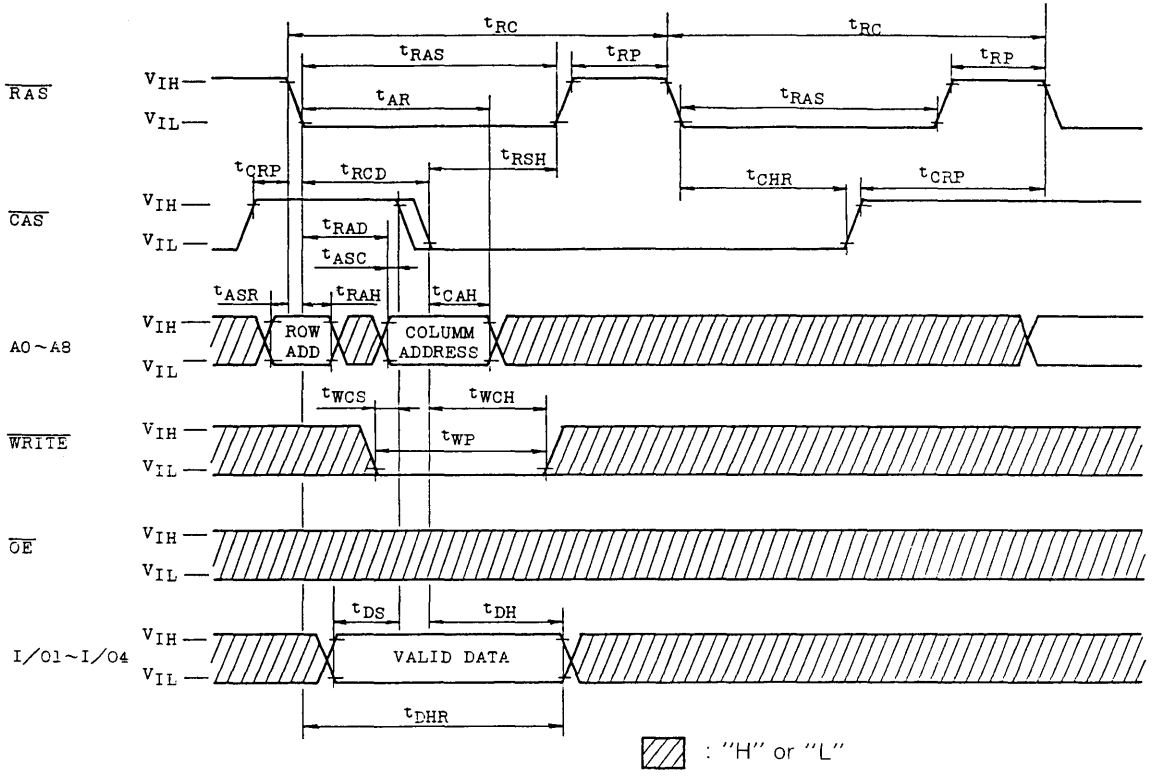
NOTE: WRITE, OE, A0 ~ A8 = "H" or "L"

▨ : "H" or "L"

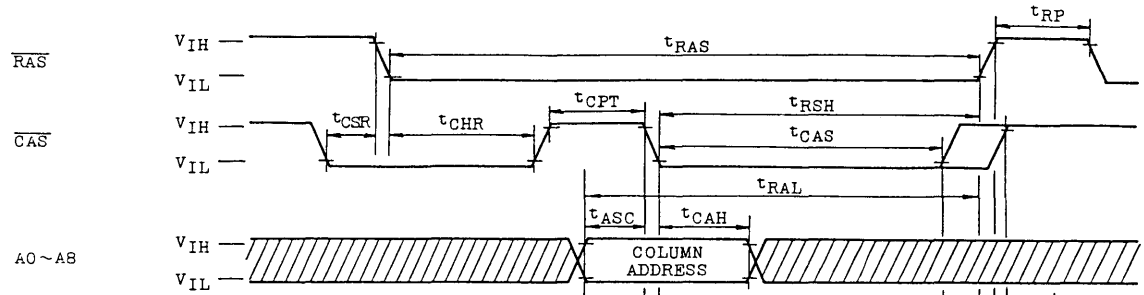
- HIDDEN REFRESH CYCLE (READ)



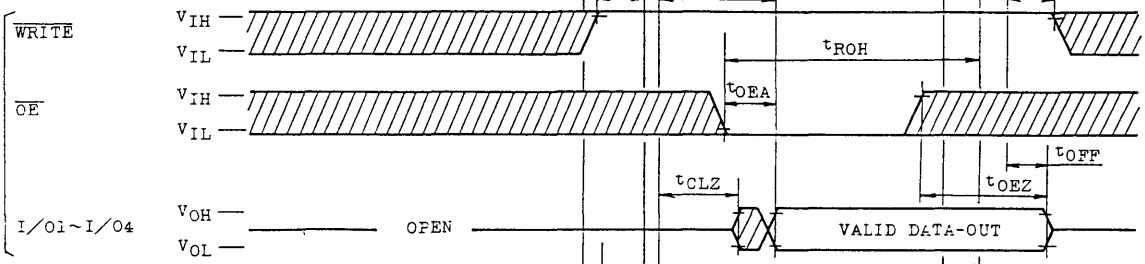
- HIDDEN REFRESH CYCLE (WRITE)



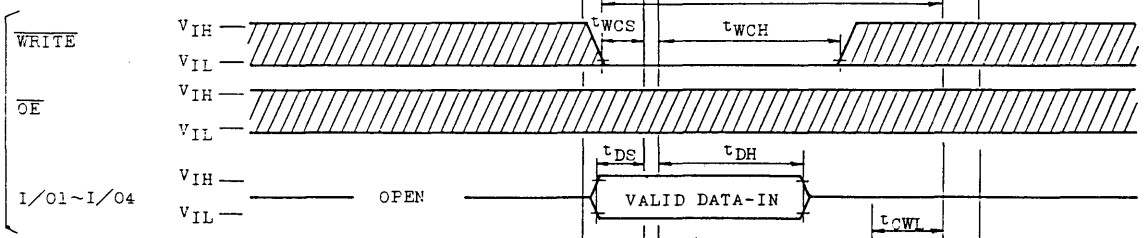
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



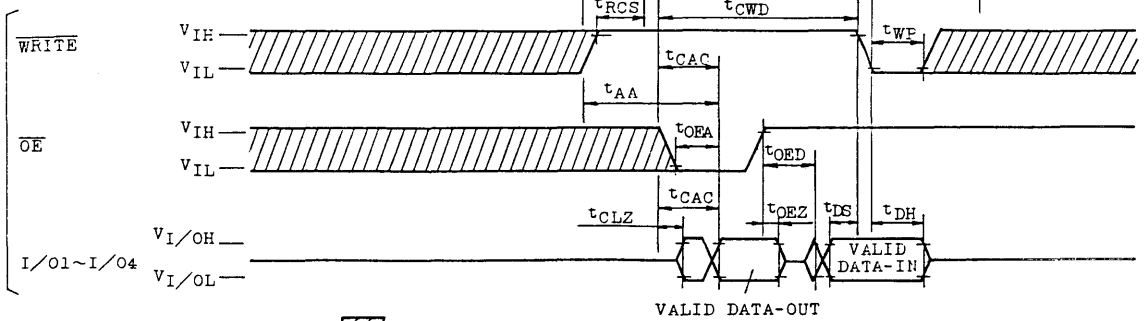
- READ CYCLE



- WRITE CYCLE



- READ-MODIFY-WRITE CYCLE

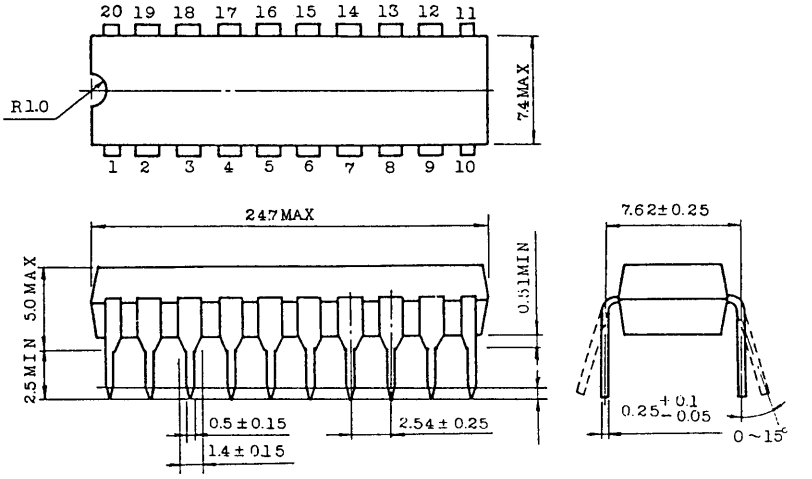


: "H" or "L"

OUTLINE DRAWINGS

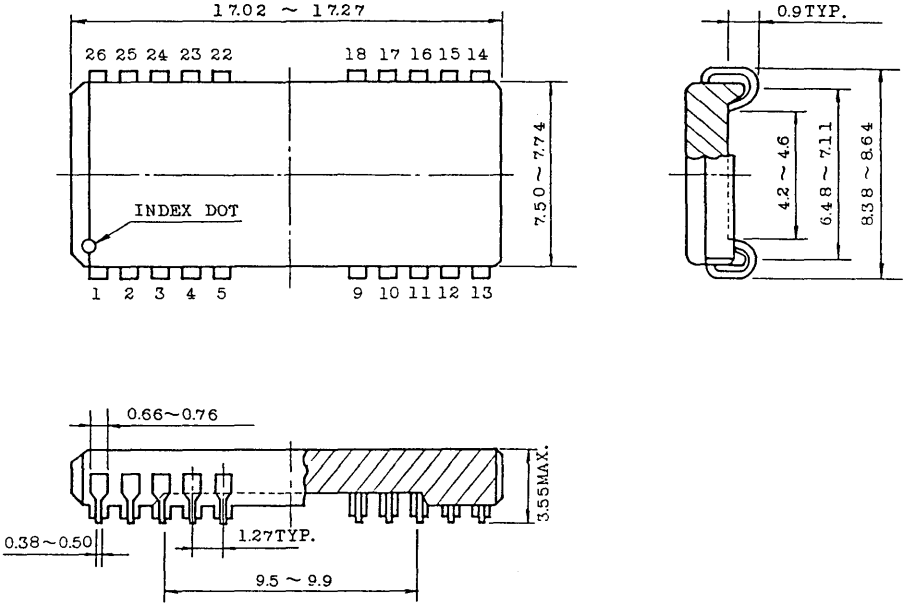
- Plastic DIP

Unit in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 20 leads.
All dimensions are in millimeters.

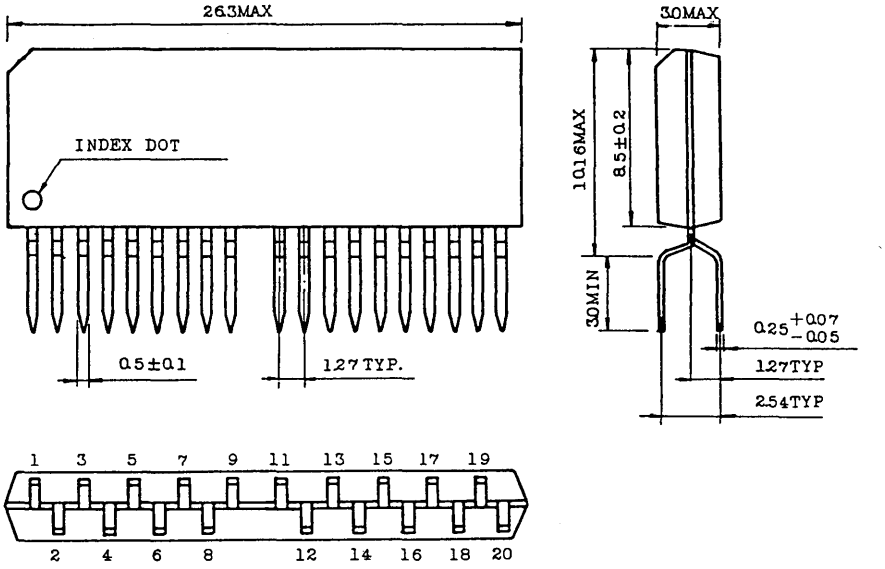
- Plastic SOJ



NOTE: Each lead pitch 1.27mm.
All dimensions are in millimeters.

- **Plastic ZIP**

Unit in mm



NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TOSHIBA MOS MEMORY PRODUCTS

262,144 WORD×4 BIT DYNAMIC RAM

SILICON GATE CMOS

TC514256PL/JL/ZL-85, TC514256PL/JL/ZL-10 TC514256PL/JL/ZL-12

DESCRIPTION

The TC514256PL/JL/ZL is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256PL/JL/ZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The TC514256PL/JL/ZL is suited for use in low power applications where battery operation and battery back up for nonvolatility are required. Multiplexed address inputs permit the TC514256PL/JL/ZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

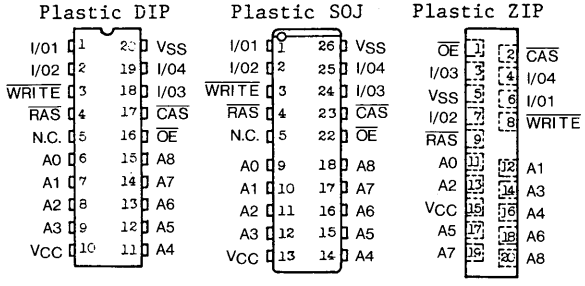
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256P/J/Z-85	-10	-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Lower Power
  413mW MAX. Operating (TC514256PL/JL/ZL/85)
  358mW MAX. Operating (TC514256PL/JL/ZL-10)
  303mW MAX. Operating (TC514256PL/JL/ZL-12)
  1.7mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/64ms
- Package Plastic DIP : TC514256PL
  Plastic SOJ : TC514256JL
  Plastic ZIP : TC514256ZL

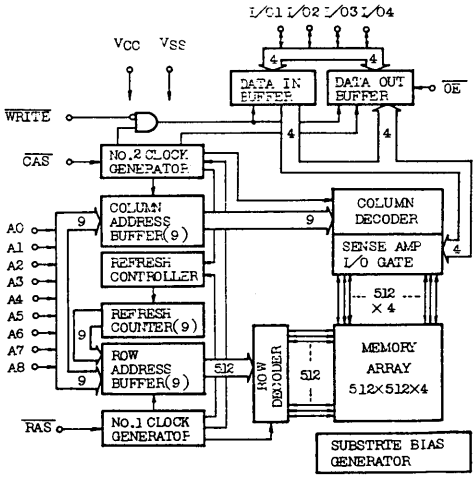
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01 ~ I/04	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256PL/JL/ZL-85	–	75	mA	3, 4
		TC514256PL/JL/ZL-10	–	65		
		TC514256PL/JL/ZL-12	–	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH} : t_{RC} = t_{RC} MIN.)	TC514256PL/JL/ZL-85	–	75	mA	3
		TC514256PL/JL/ZL-10	–	65		
		TC514256PL/JL/ZL-12	–	55		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL} , $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256PL/JL/ZL-85	–	55	mA	3, 4
		TC514256PL/JL/ZL-10	–	45		
		TC514256PL/JL/ZL-12	–	35		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = Vcc-0.2V)		–	300	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256PL/JL/ZL-85	–	75	mA	3
		TC514256PL/JL/ZL-10	–	65		
		TC514256PL/JL/ZL-12	–	55		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, BATTERY BACK UP Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} -0.2V $\overline{WRITE}$ = V_{CC} -0.2V or 0.2V, A_{0-8} = V_{CC} -0.2V or 0.2V, I/O_{1-4} = V_{CC} -0.2V, 0.2V or OPEN: t_{RC} = 125μs, t_{RAS} = t_{RAS} MIN. ~ 1μs)		–	300	μA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ V_{CC})		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE (I_{OUT}=−5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514256PL/JL/ZL-85		TC514256PL/JL/ZL-10		TC514256PL/JL/ZL-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	–	255	–	295	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	55	–	70	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	110	–	115	–	140	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	9, 14
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	30	–	35	ns	9, 14
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	9, 15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	50	–	65	ns	9, 15
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	5	–	5	–	5	–	ns	6
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	70	25	85	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	20	–	20	–	25	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	Write Command Pulse Width	20	–	20	–	25	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	20	–	20	–	25	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514256PL/JL/ZL-85		TC514256PL/JL/ZL-10		TC514256PL/JL/ZL-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	64	–	64	–	64	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	65	–	65	–	75	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	120	–	135	–	160	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	–	85	–	100	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	20	–	20	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

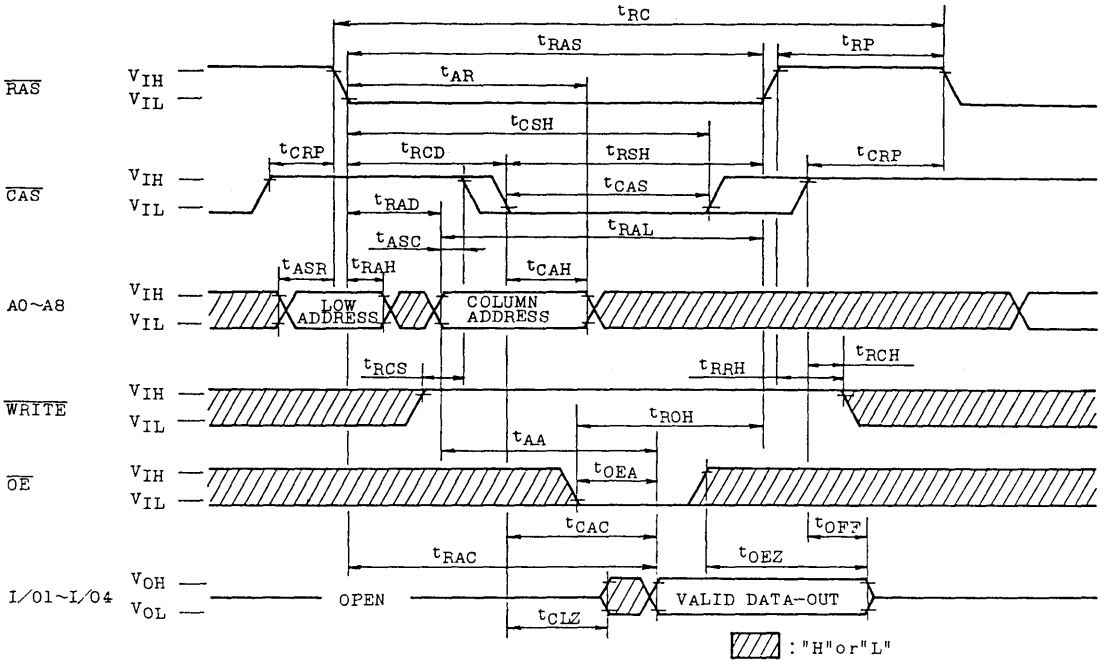
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_8$)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Output Capacitance ($I/O_1 \sim I/O_4$)	–	7	pF

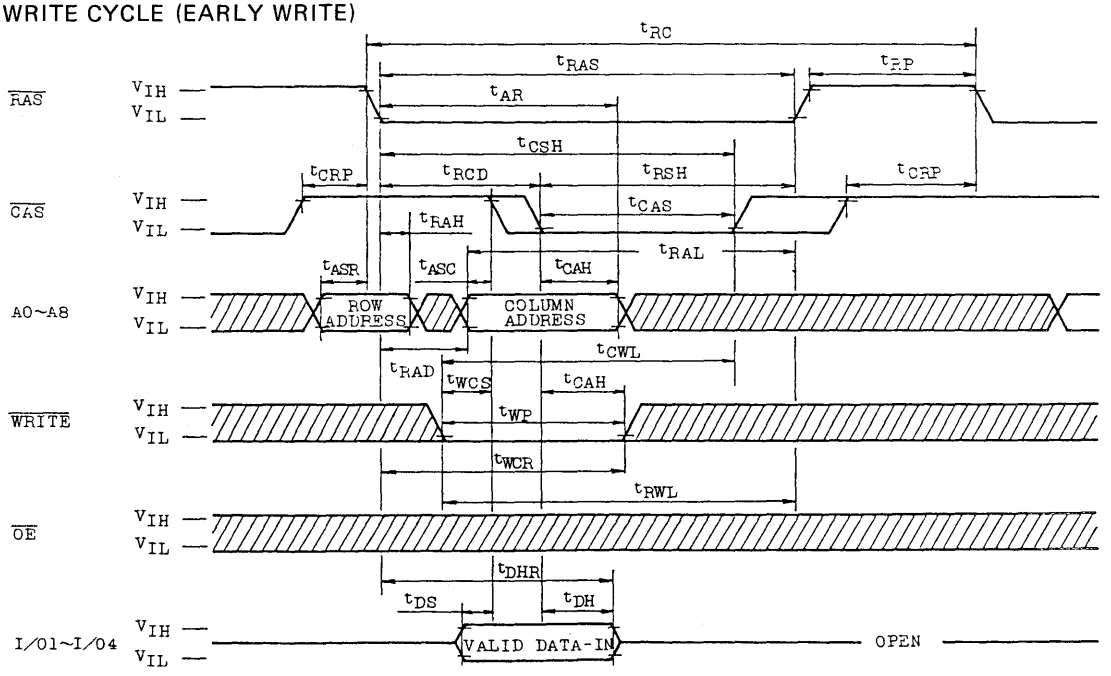
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All Voltages are referenced to V_{SS} .
3. I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} , I_{CC7} depend on cycle rate.
4. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. t_{RAS}(max.) = 1μs is only applied to refresh of battery-back up. t_{RAS}(max.) = 10μs is applied to functional operating.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume t_T = 5ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

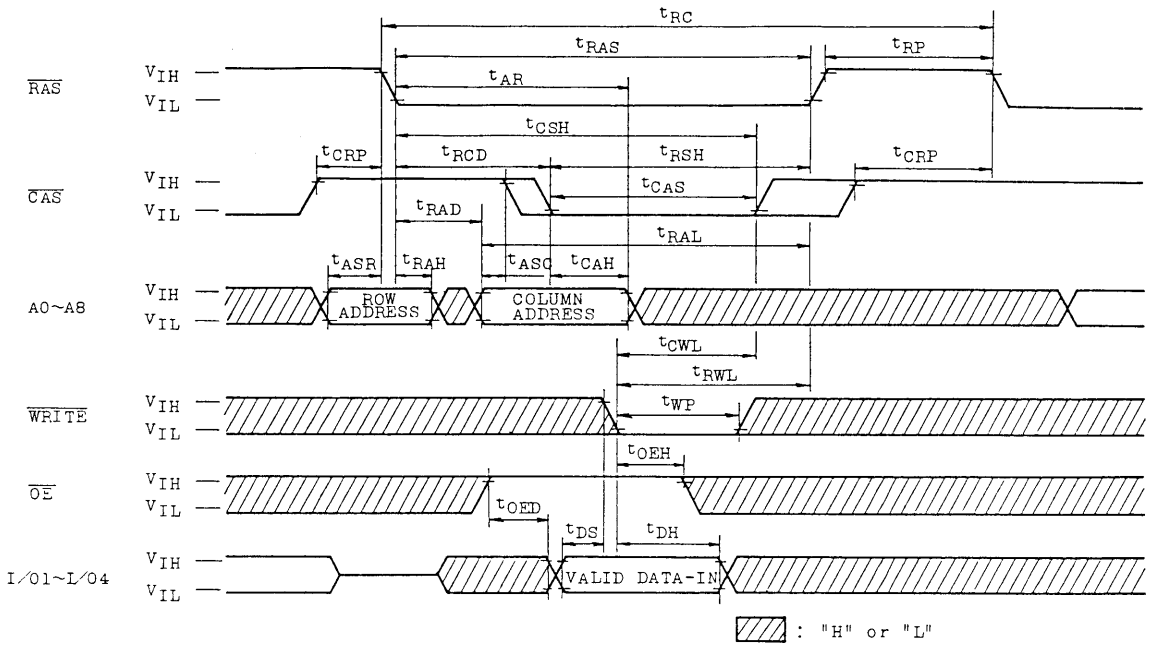
- READ CYCLE



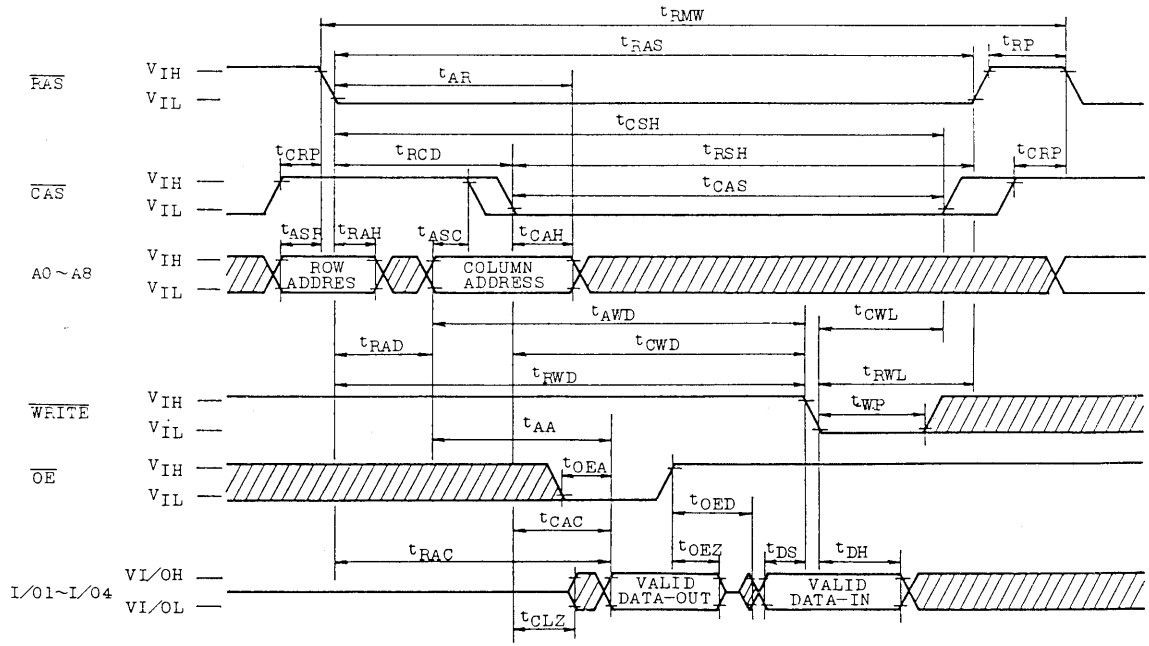
- WRITE CYCLE (EARLY WRITE)



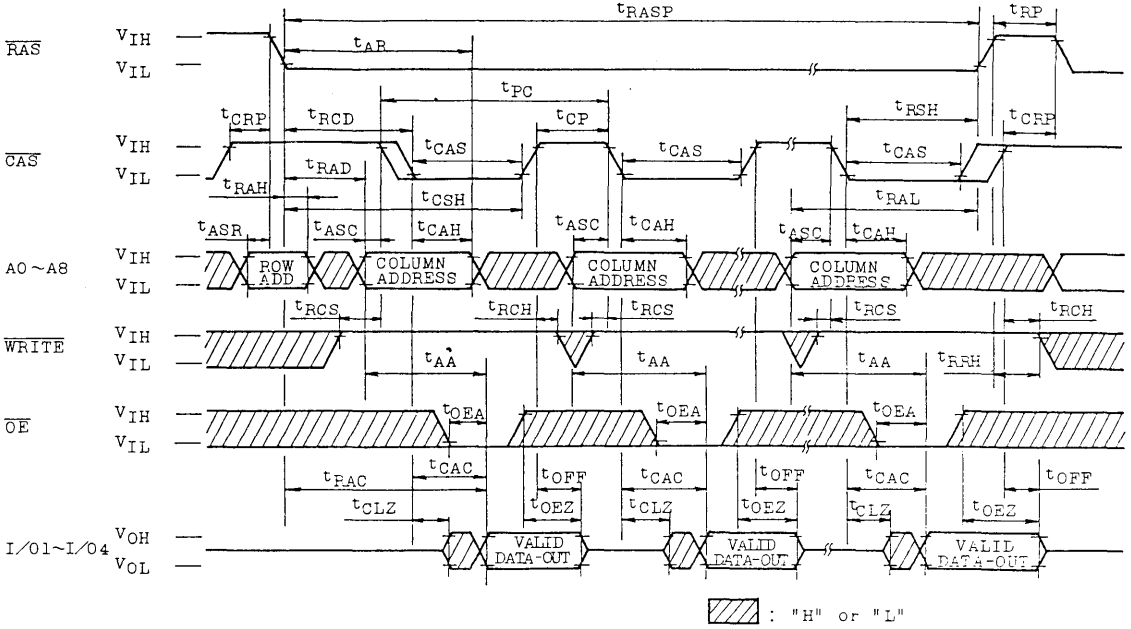
- WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



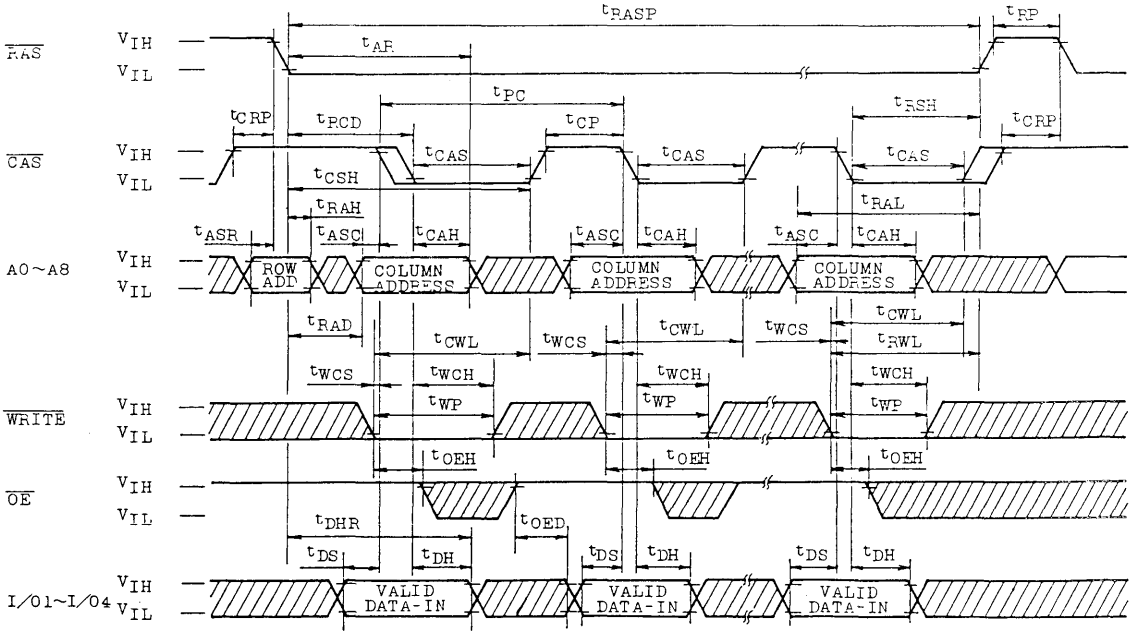
- READ-MODIFY-WRITE CYCLE



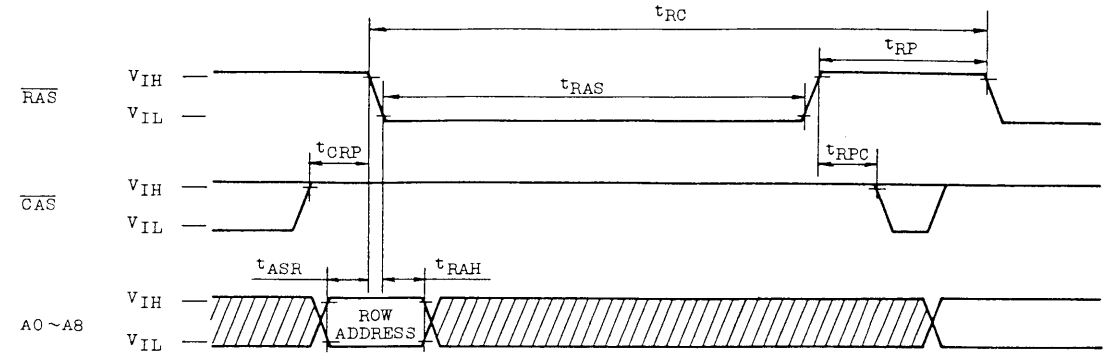
- FAST PAGE MODE READ CYCLE



- FAST PAGE MODE WRITE CYCLE



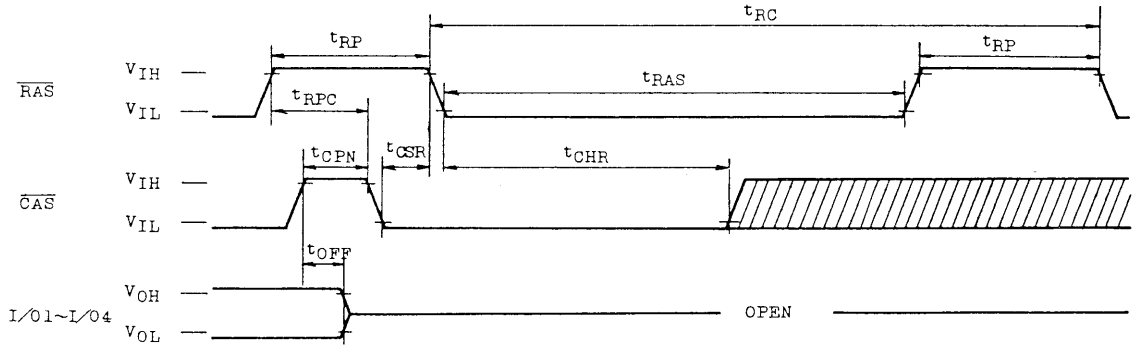
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$, $\overline{OE}$: "H" or "L"

▨ : "H" or "L"

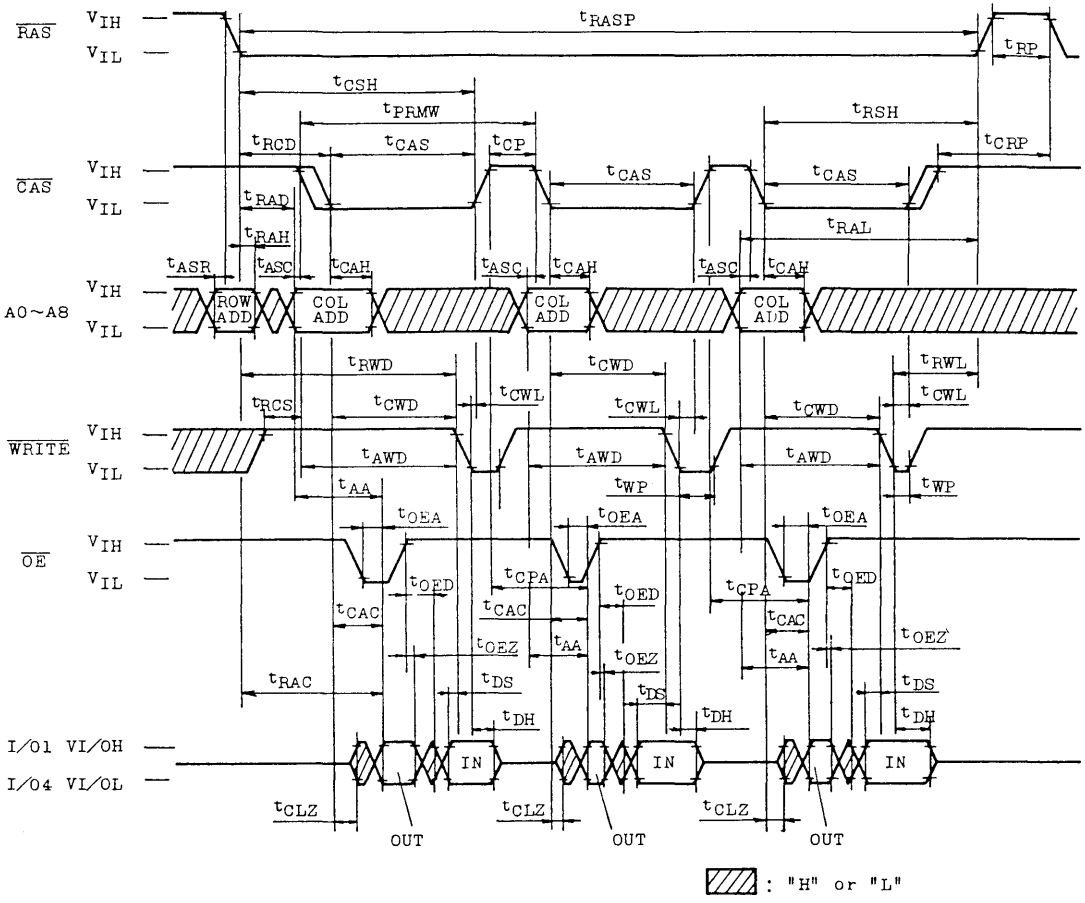
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



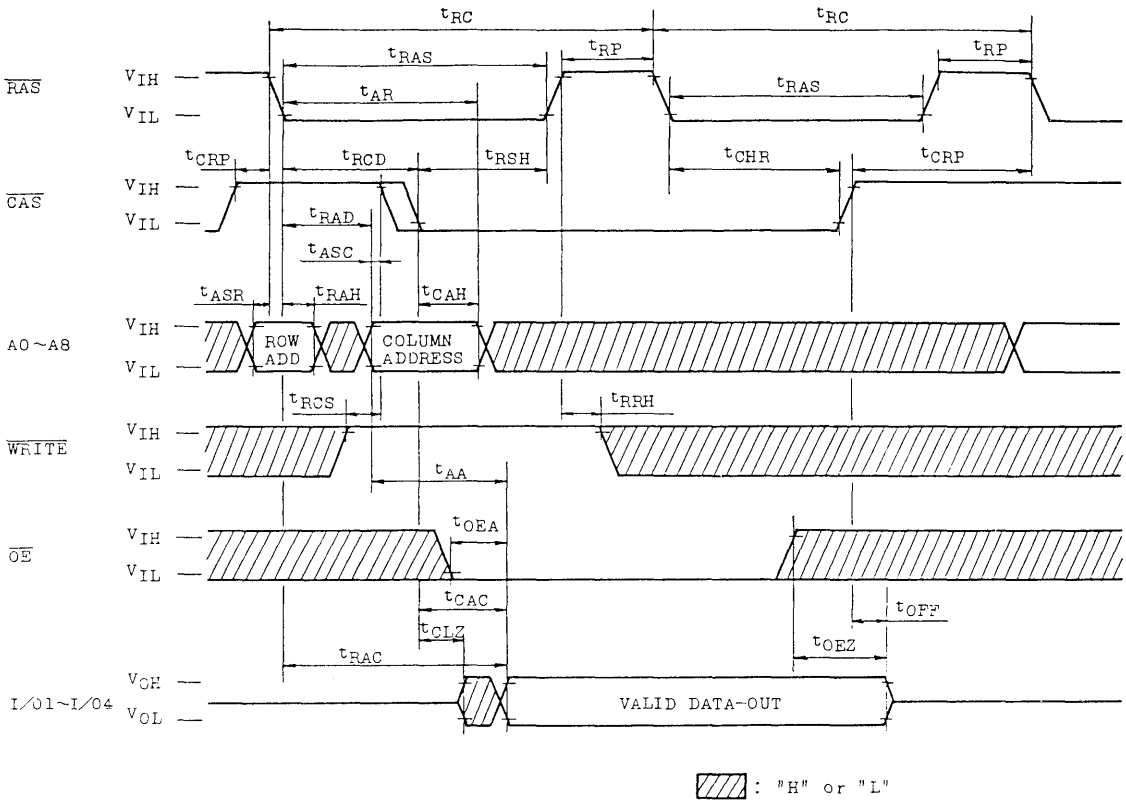
NOTE: $\overline{WRITE}$, $\overline{OE}$, A0 ~ A8: "H" or "L"

▨ : "H" or "L"

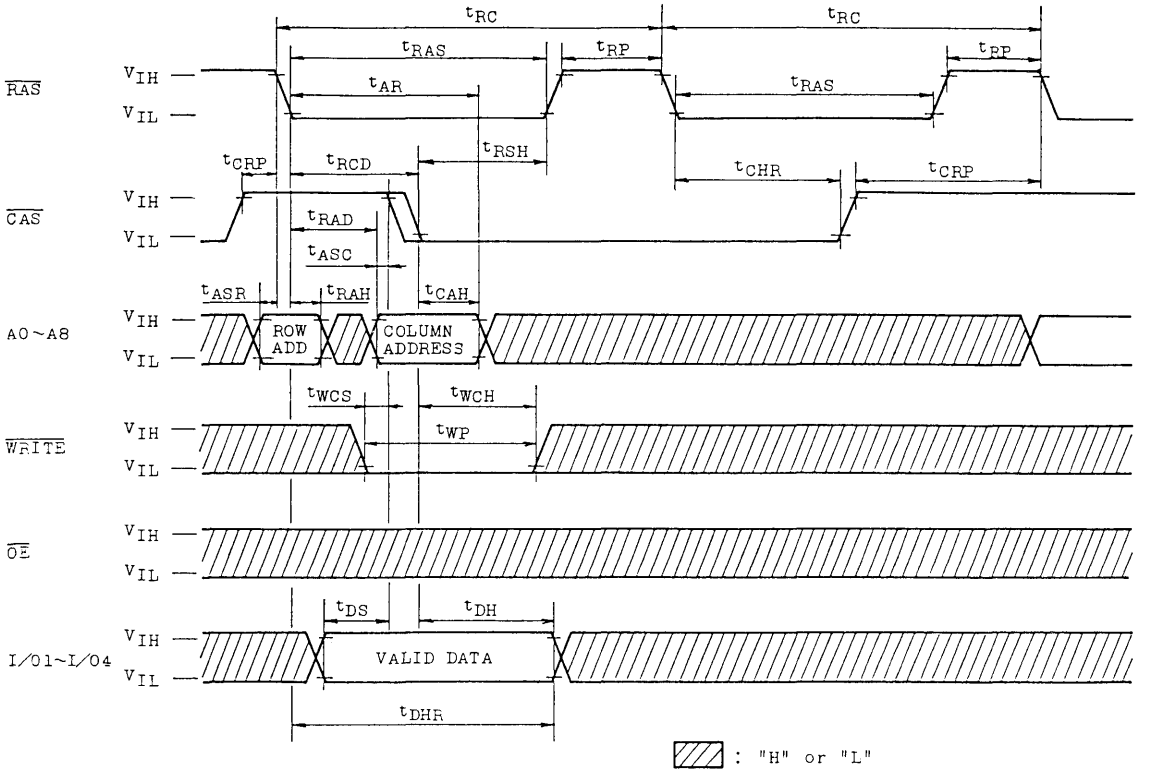
- FAST PAGE MODE READ-MODIFY-WRITE CYCLE



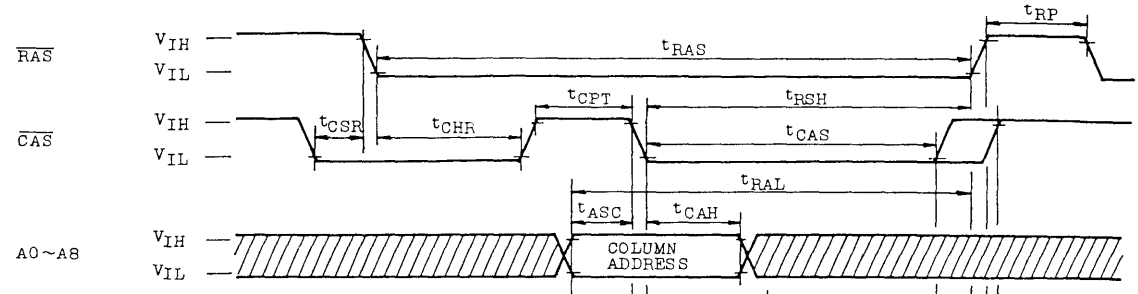
- HIDDEN REFRESH CYCLE (READ)



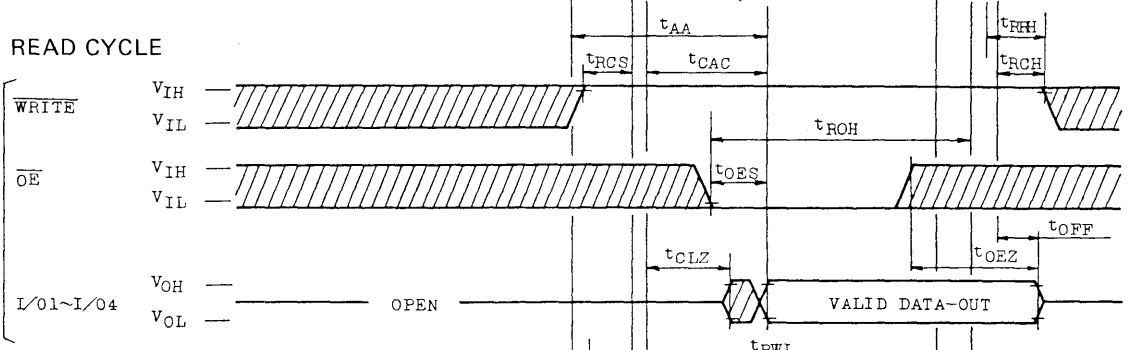
- HIDDEN REFRESH CYCLE (WRITE)



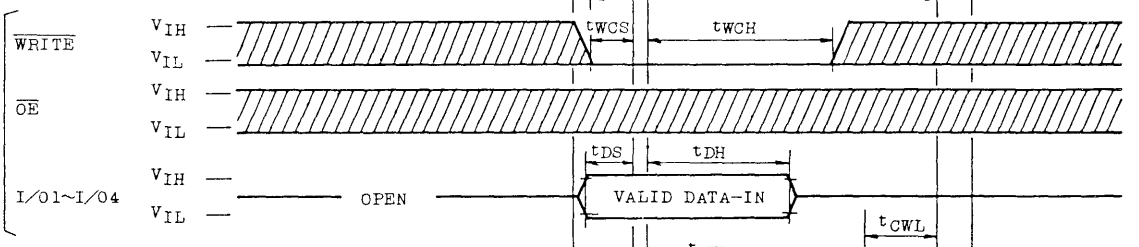
- $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



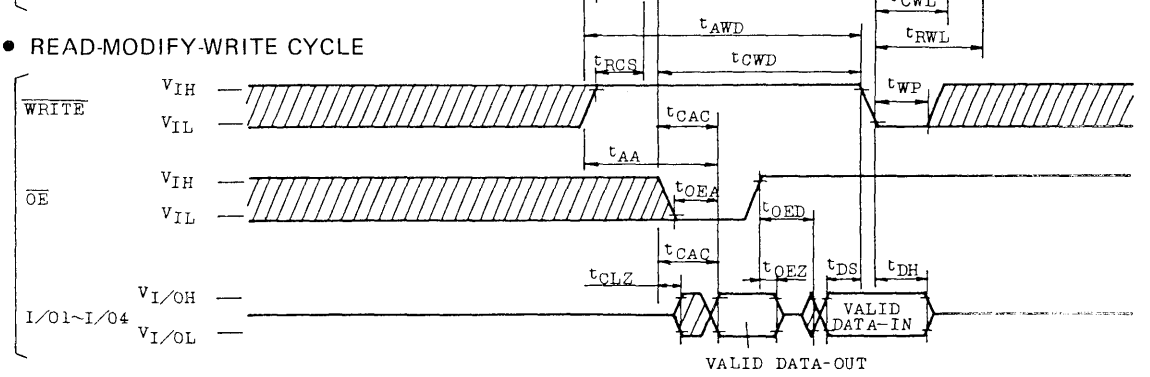
- READ CYCLE



- WRITE CYCLE



- READ-MODIFY-WRITE CYCLE

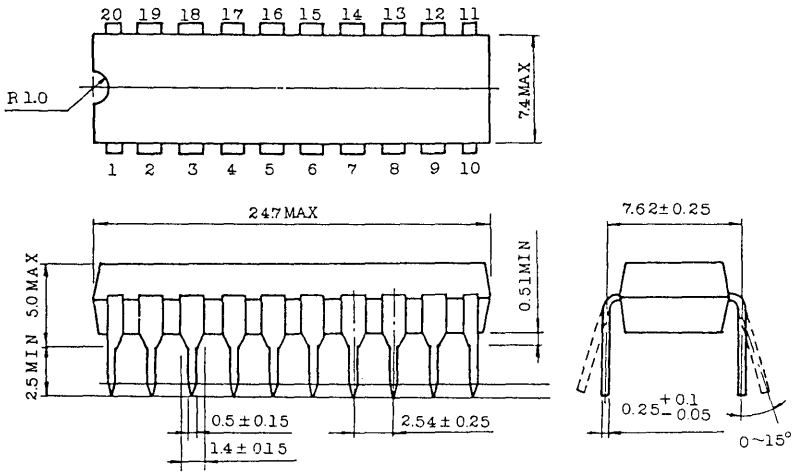


▨ : "H" or "L"

OUTLINE DRAWINGS

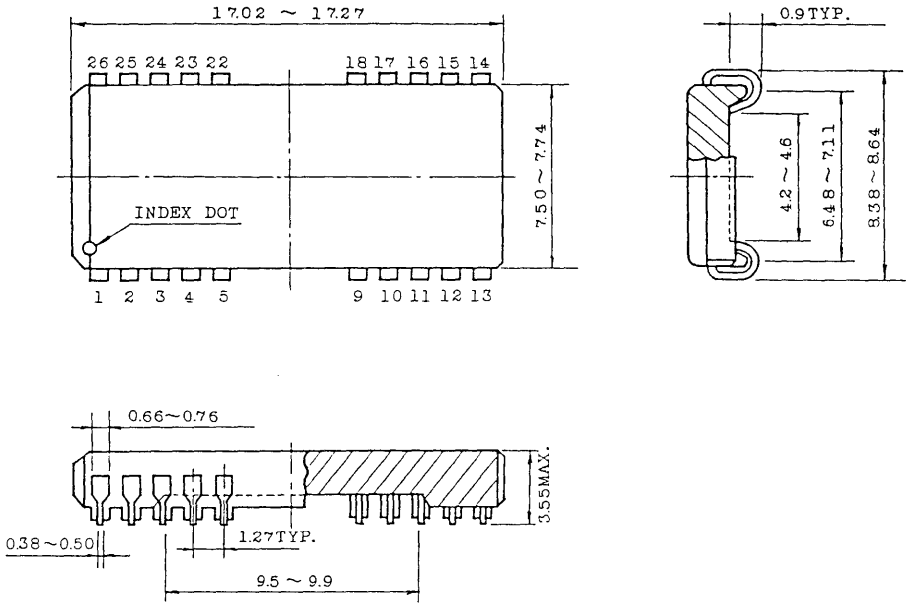
- Plastic DIP

Unit in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 20 leads.
All dimensions are in millimeters.

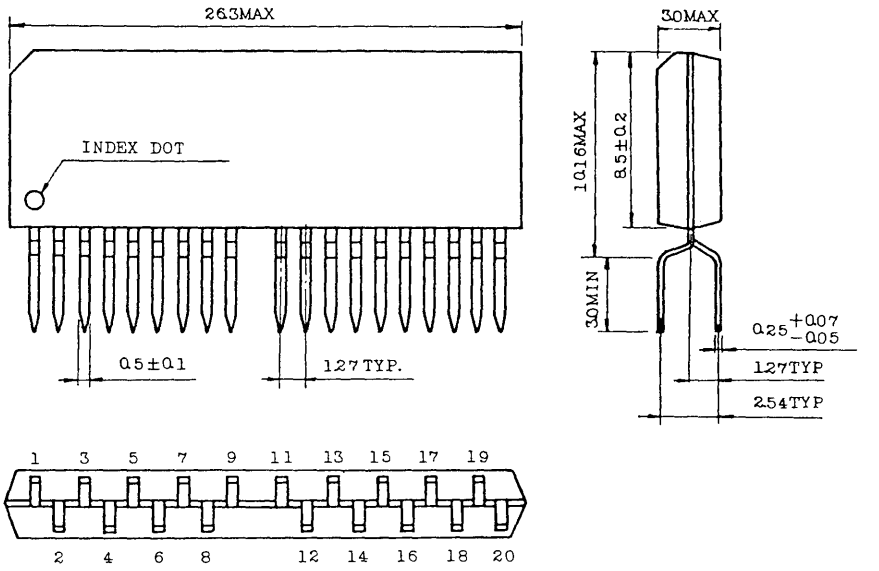
- Plastic SOJ



NOTE: Each lead pitch 1.27mm.
All dimensions are in millimeters.

- **Plastic ZIP**

Unit in mm



NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC514256AP/AJ/AZ-70, TC514256AP/AJ/AZ-80
TC514256AP/AJ/AZ-10

DESCRIPTION

The TC514256AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

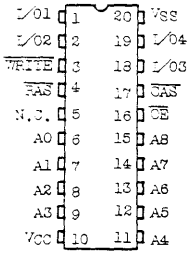
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	190ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

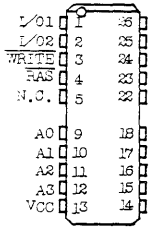
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  440mW MAX. Operating(TC514256AP/AJ/AZ-70)
  385mW MAX. Operating(TC514256AP/AJ/AZ-80)
  330mW MAX. Operating(TC514256AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514256AP
  Plastic SOJ: TC514256AJ
  Plastic ZIP: TC514256AZ

PIN CONNECTION (TOP VIEW)

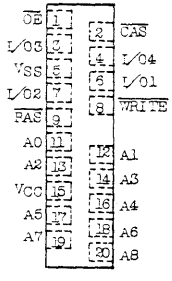
Plastic DIP



Plastic SOJ



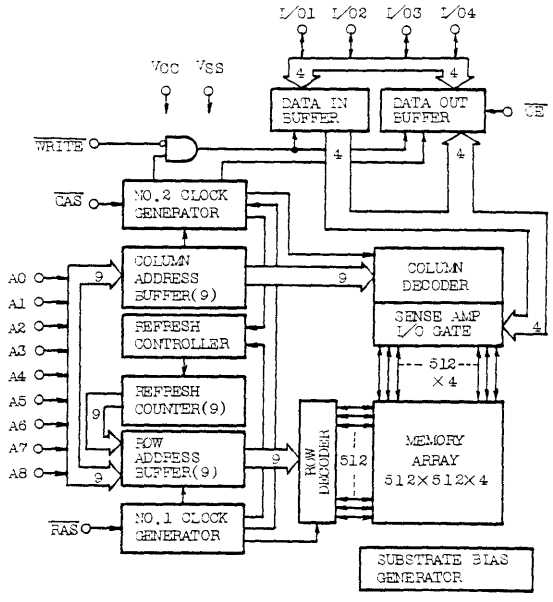
Plastic ZIP



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514256AP/AJ/AZ-70	-	80	mA	3,4
		TC514256AP/AJ/AZ-80	-	70		
		TC514256AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514256AP/AJ/AZ-70	-	80	mA	3
		TC514256AP/AJ/AZ-80	-	70		
		TC514256AP/AJ/AZ-10	-	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514256AP/AJ/AZ-70	-	60	mA	3,4
		TC514256AP/AJ/AZ-80	-	50		
		TC514256AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514256AP/AJ/AZ-70	-	80	mA	3
		TC514256AP/AJ/AZ-80	-	70		
		TC514256AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ V_{CC})		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514256AP -70		TC514256AP -80		TC514256AP -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	100	-	115	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	8,14
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	0	-	0	-	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514256AP -70		TC514256AP -80		TC514256AP -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	60	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	135	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	85	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1 ∿ I/O4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified value output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

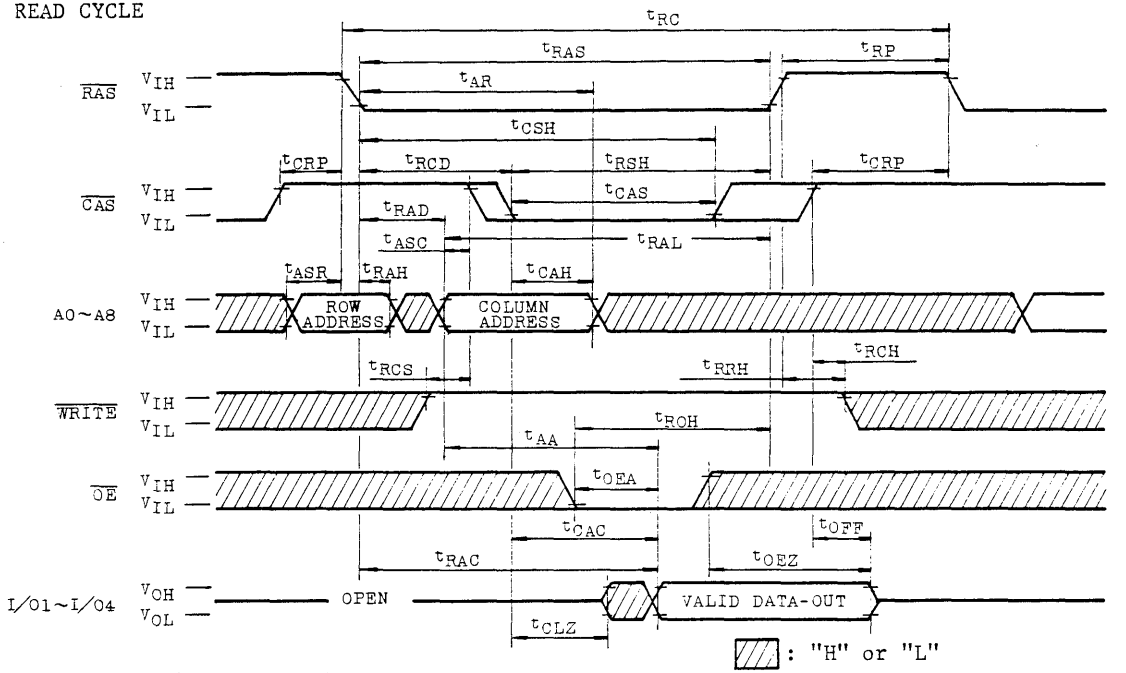
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.

12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.) the cycle is an early wirte cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

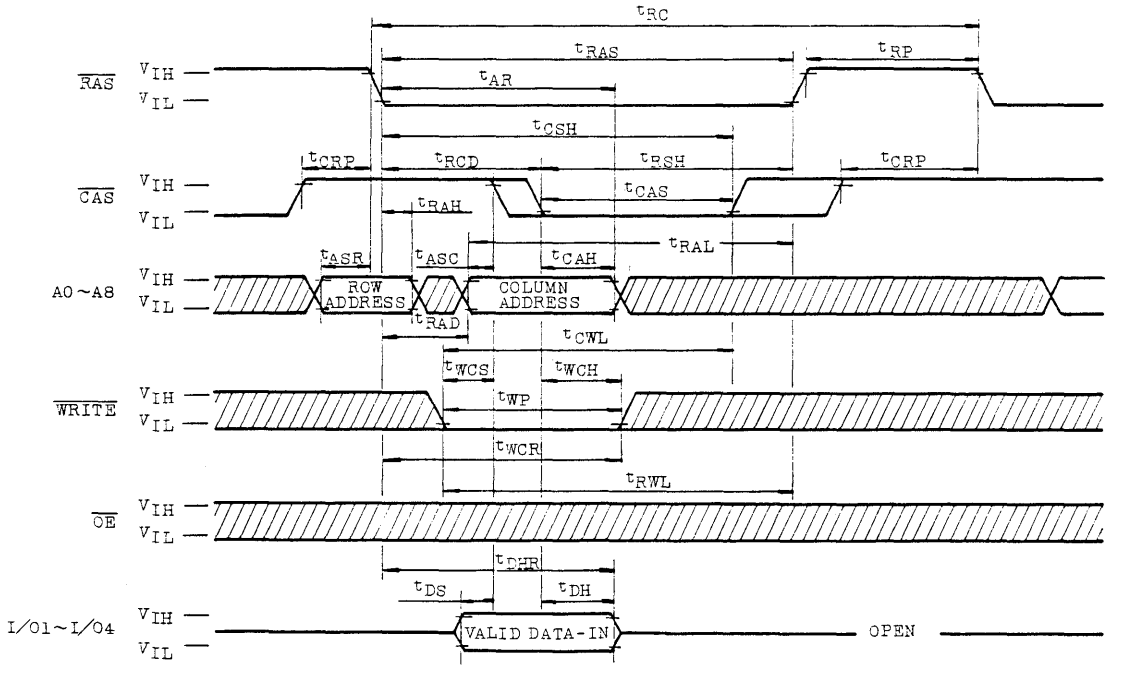
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

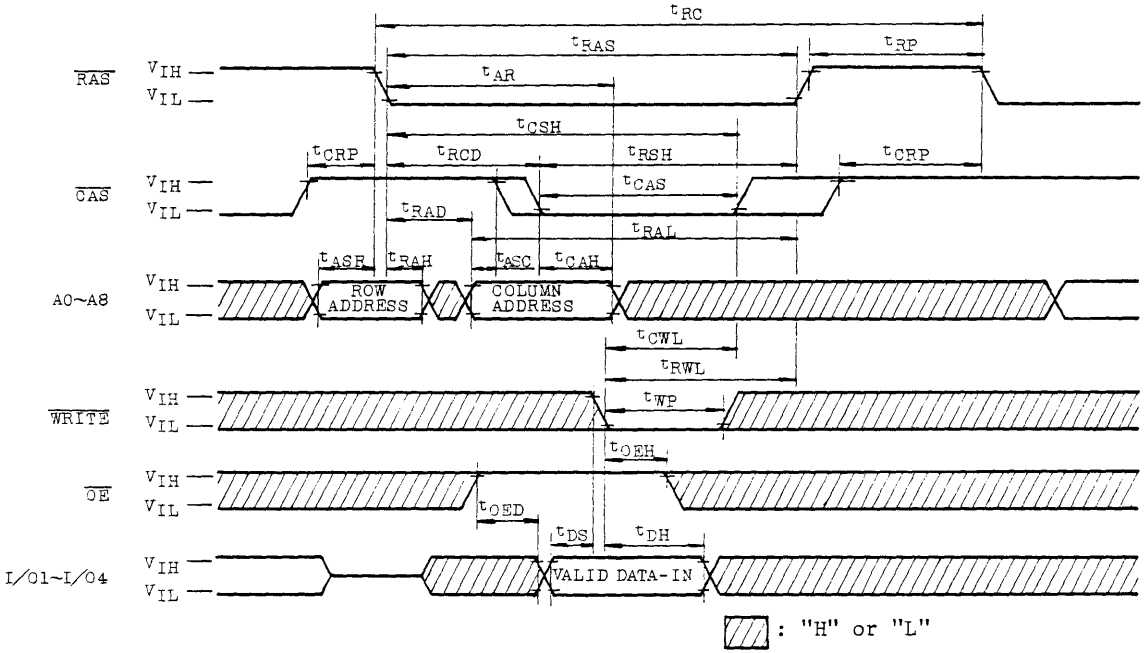
READ CYCLE



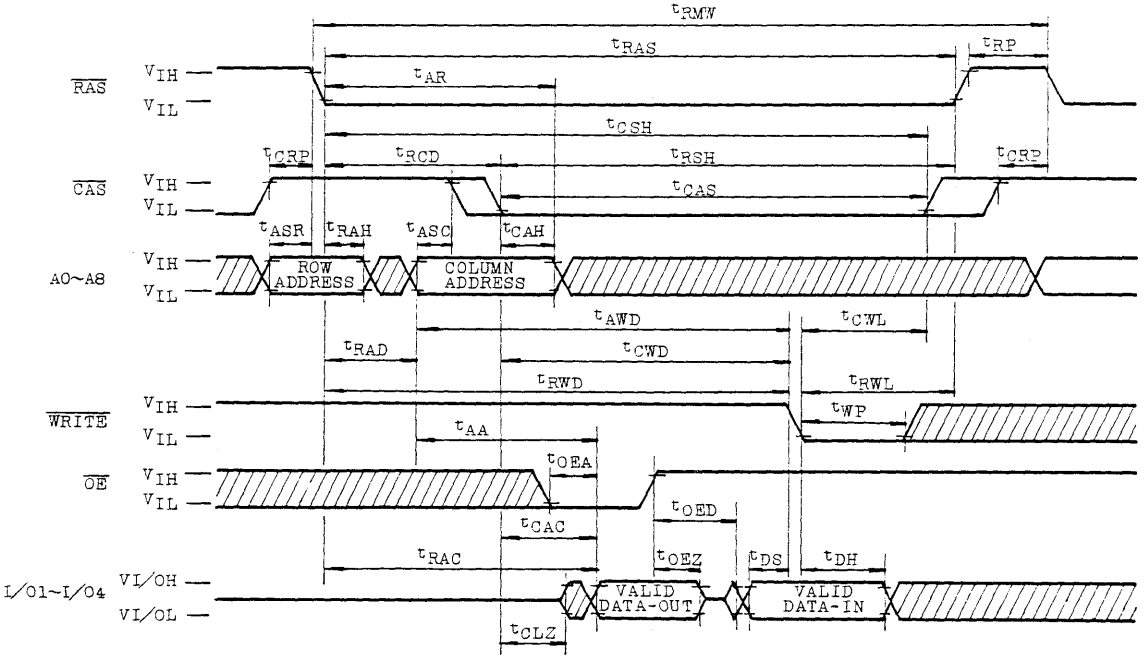
WRITE CYCLE (EARLY WRITE)



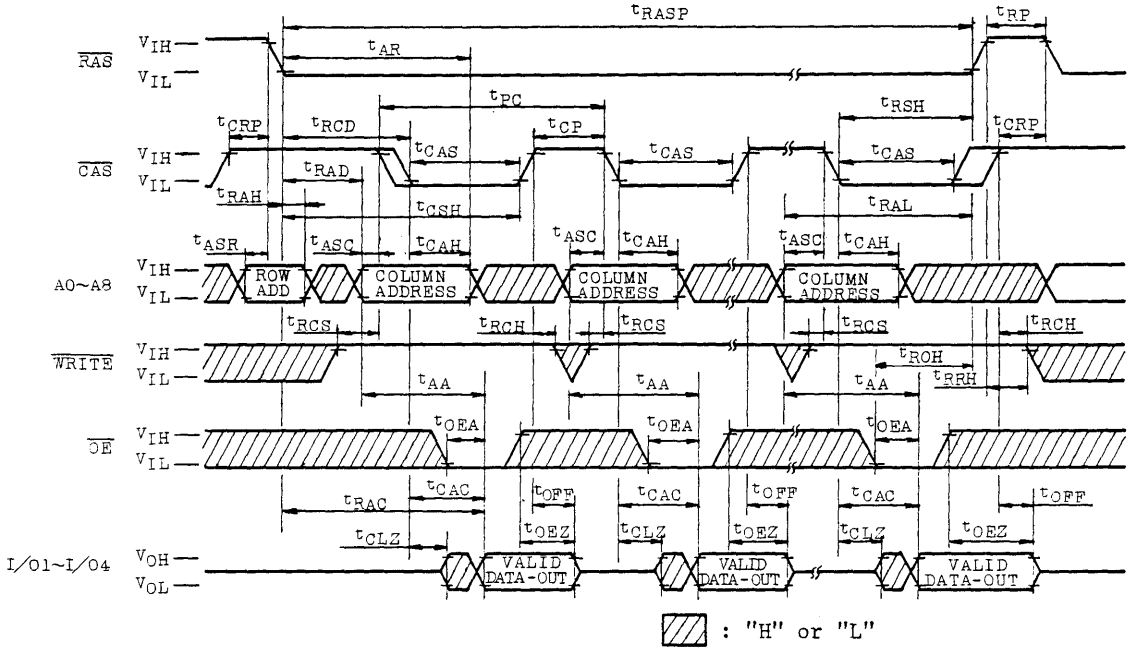
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



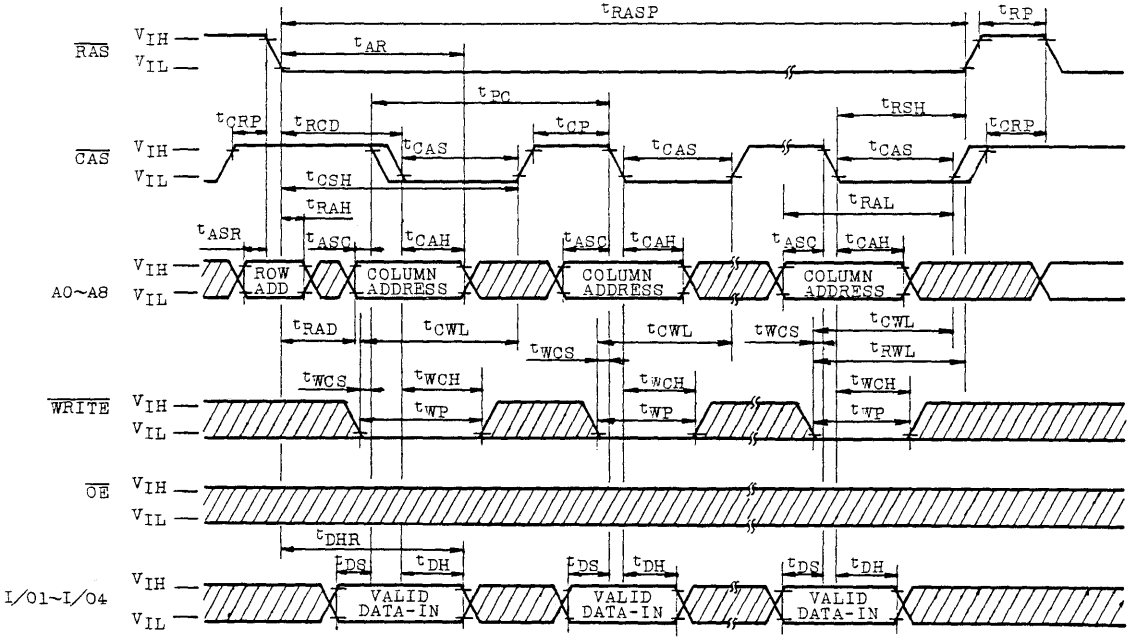
READ-MODIFY-WRITE CYCLE



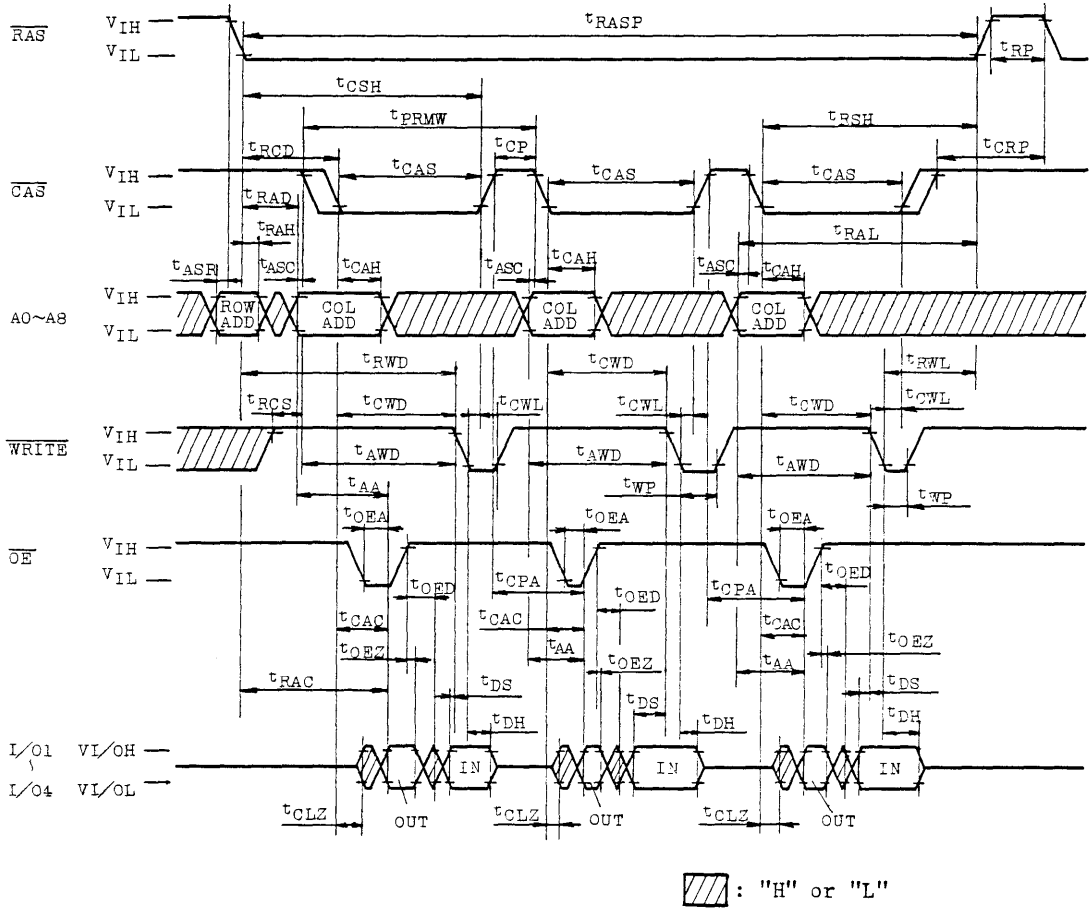
FAST PAGE MODE READ CYCLE



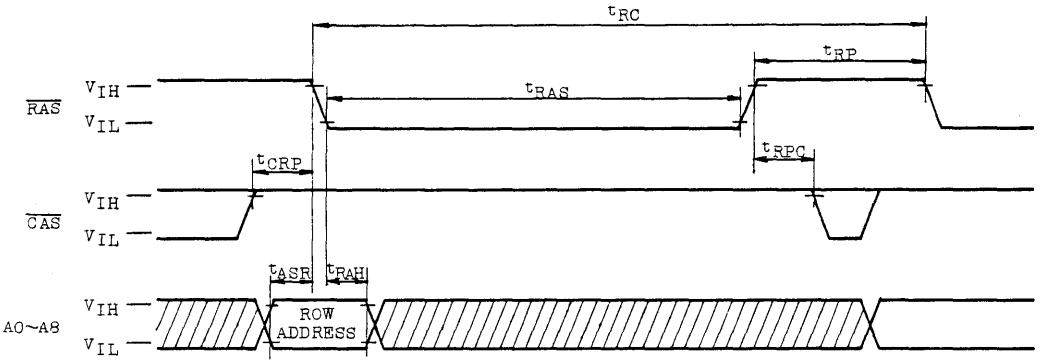
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

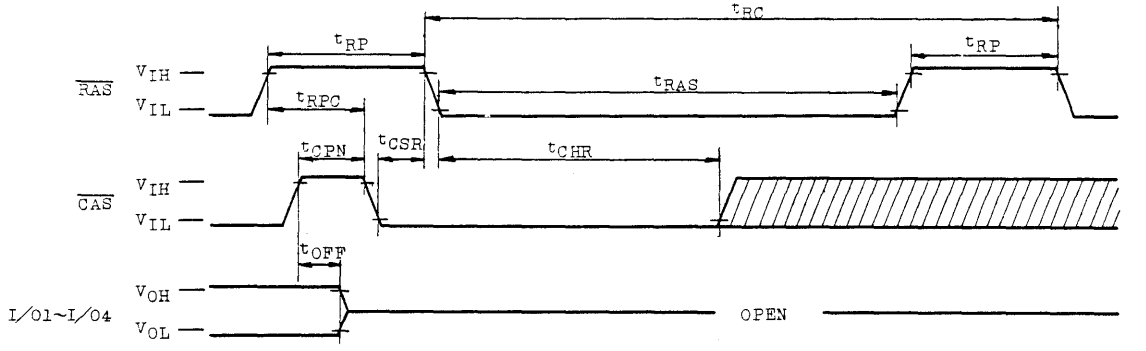


$\overline{RAS}$ ONLY REFRESH CYCLE



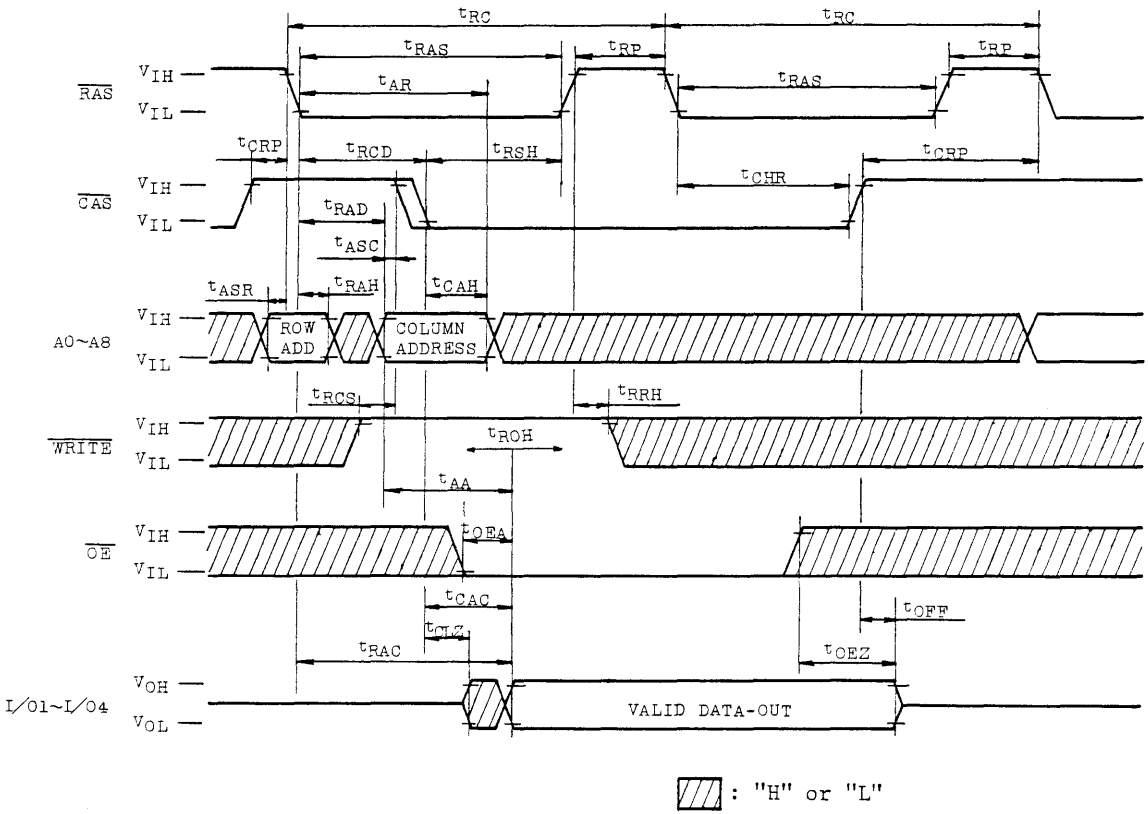
Note: $\overline{WRITE}$, $\overline{OE}$="H" or "L" ▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

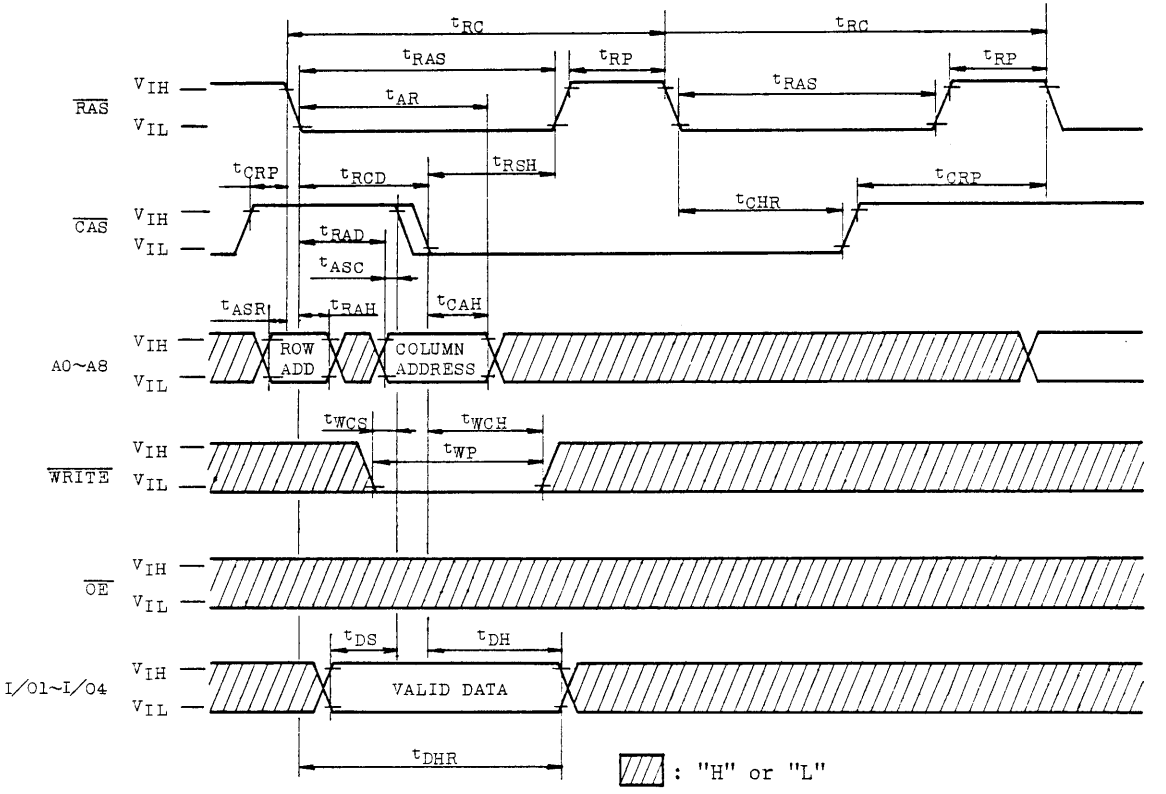


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8="H" or "L" ▨ : "H" or "L"

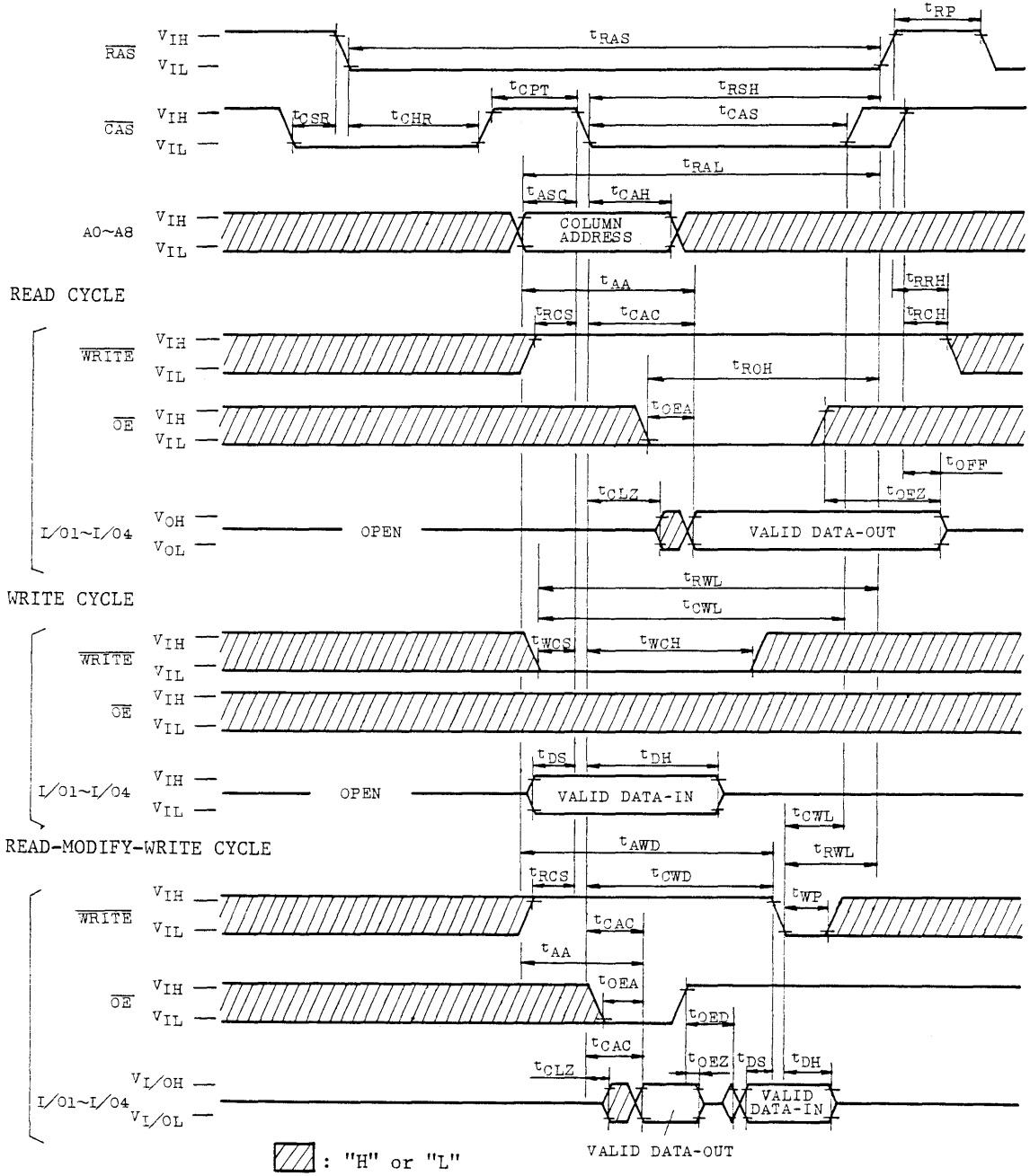
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



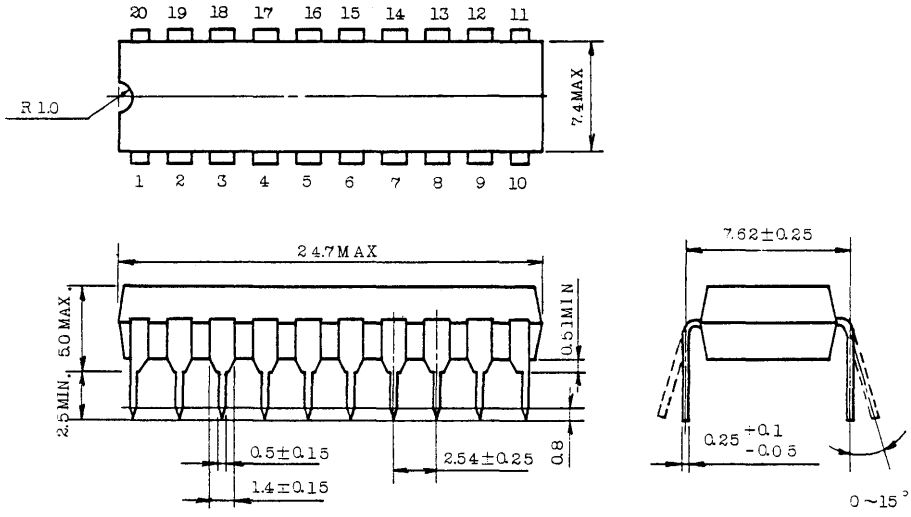
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

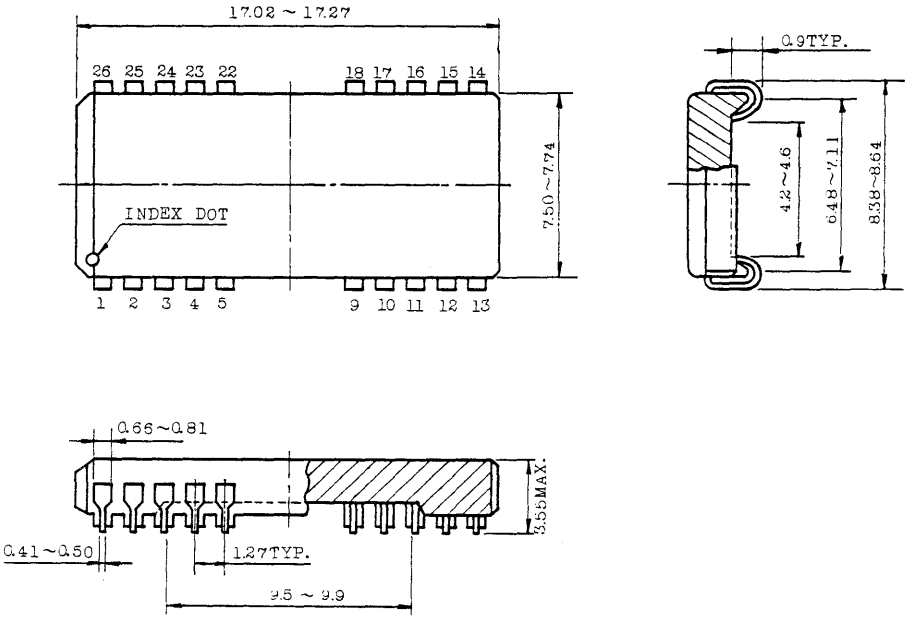
• Plastic DIP

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.
All dimensions are in millimeters.

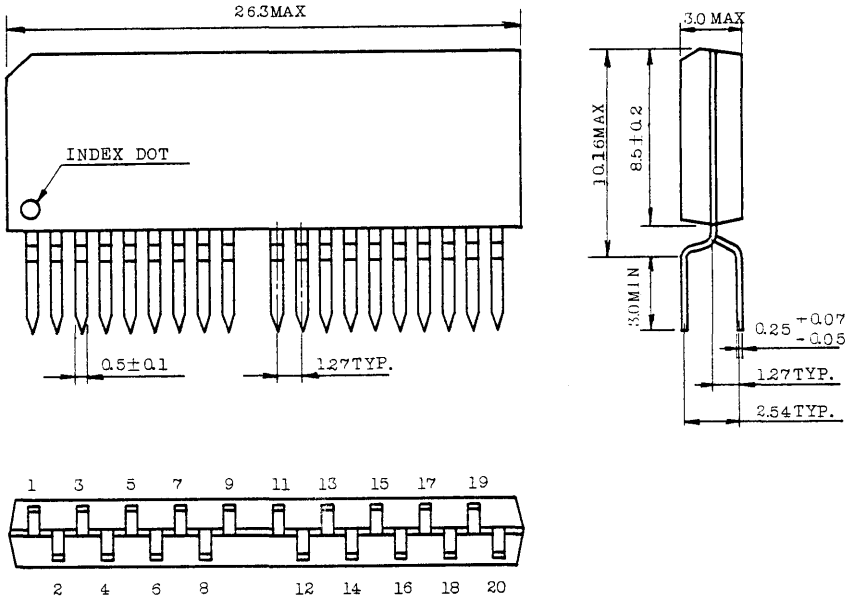
• Plastic SOJ



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC514256APL/AJL/AZL-70, TC514256APL/AJL/AZL-80
TC514256APL/AJL/AZL-10

DESCRIPTION

The TC514256APL/AJL/AZL is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256APL/AJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256APL/AJL/AZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

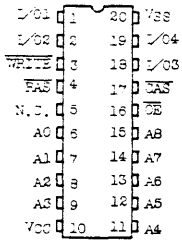
		TC514256AB/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	190ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator

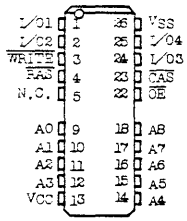
- **Low Standby Current : 200μA max.**
- **Extended Refresh Period : 512 cycles/64ms**
- Low Power
  440mW MAX. Operating (TC51425APL/AJL/AZL-70)
  385mW MAX. Operating (TC51425APL/AJL/AZL-80)
  330mW MAX. Operating (TC51425APL/AJL/AZL-10)
  1.1mW MAX. Standby
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible

PIN CONNECTION (TOP VIEW)

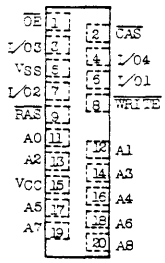
Plastic DIP



Plastic SOJ



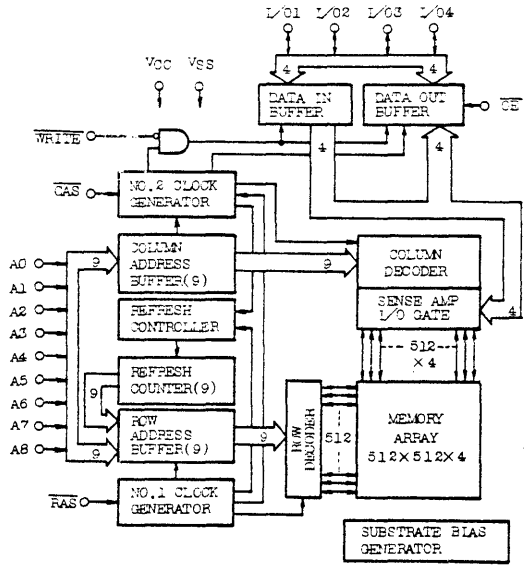
Plastic ZIP



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



TC514266AP/AJ/AZ-70, TC514266AP/AJ/AZ-80
TC514266AP/AJ/AZ-10

DESCRIPTION

The TC514266AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bit. The TC514266AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514266AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

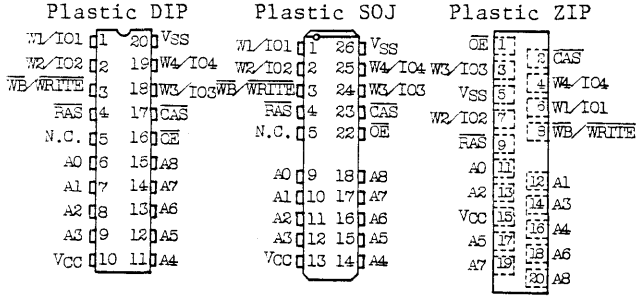
FEATURES

- 262,144 words by 4 bit organization
- Fast access time and cycle time

		TC514266AP/AJ/AZ -70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating(TC514266AP/AJ/AZ-70)
  - 385mW MAX. Operating(TC514266AP/AJ/AZ-80)
  - 330mW MAX. Operating(TC514266AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write Per Bit and Fast Page Mode capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514266AP
  Plastic SOJ: TC514266AJ
  Plastic ZIP: TC514266AZ

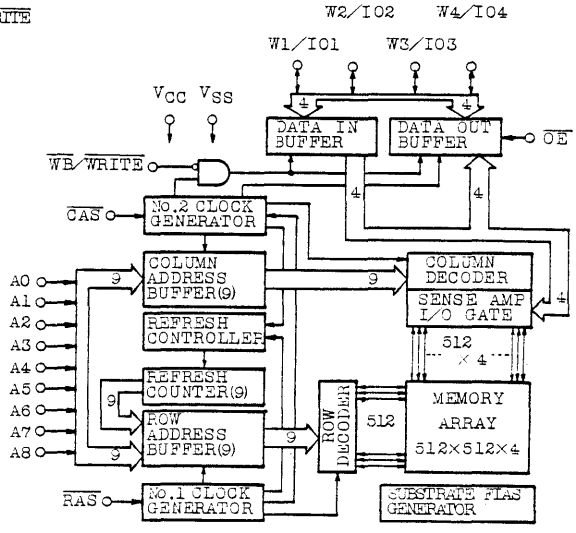
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WRITE}$	Write Per Bit/Read/ Write Input
$\overline{OE}$	Output Enable
W1/IO1∿W4/IO4	Write Select/Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature . Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514266AP/AJ/AZ-70	-	80	mA	3,4
		TC514266AP/AJ/AZ-80	-	70		
		TC514266AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514266AP/AJ/AZ-70	-	80	mA	3
		TC514266AP/AJ/AZ-80	-	70		
		TC514266AP/AJ/AZ-10	-	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	TC514266AP/AJ/AZ-70	-	60	mA	3,4
		TC514266AP/AJ/AZ-80	-	50		
		TC514266AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514266AP/AJ/AZ-70	-	80	mA	3
		TC514266AP/AJ/AZ-80	-	70		
		TC514266AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514266AP -70		TC514266AP -80		TC514266AP -10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	100	-	115	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	8,14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	5
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514266AP -70		TC514266AP -80		TC514266AP -10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	-	50	-	65	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	-	110	-	135	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	85	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	-	20	-	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
t_{OEZ}	Output Buffer Turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	10	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}$/$\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (W1/IO1 ∿ W4/IO4)	-	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. Icc1, Icc3, Icc4, Icc6 depend on cycle rate.

4. Icc1, Icc4 depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measurement with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

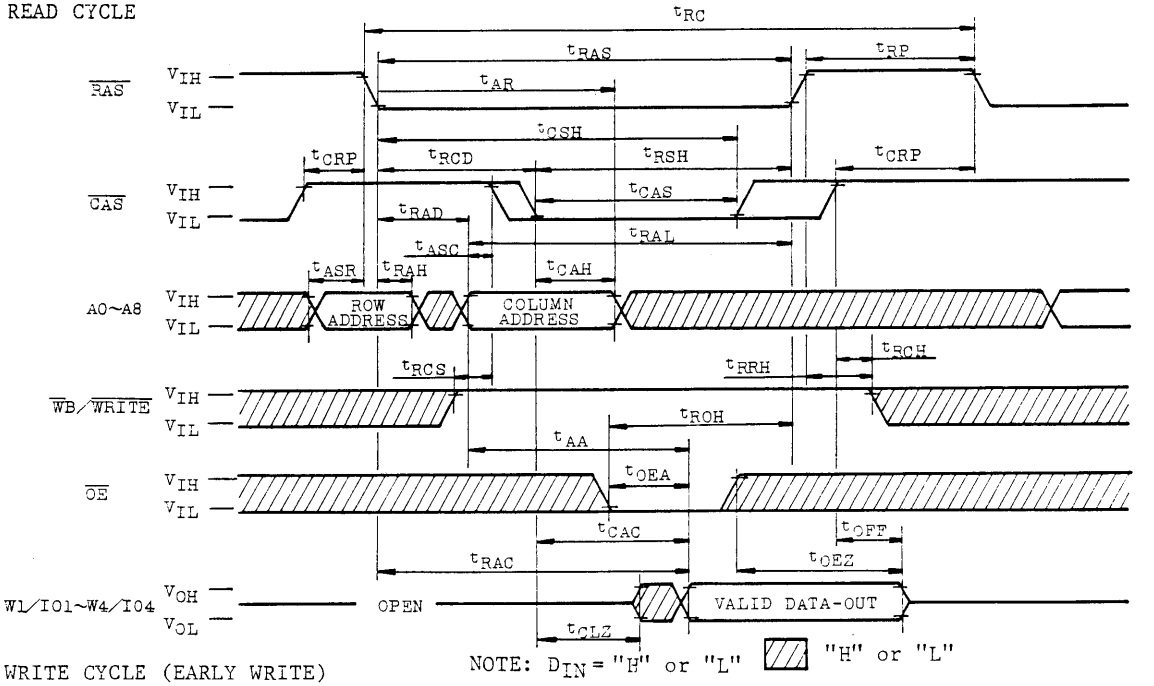
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}/\overline{WRITE}$ leading edge in read-modify-write cycles.

12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modify-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

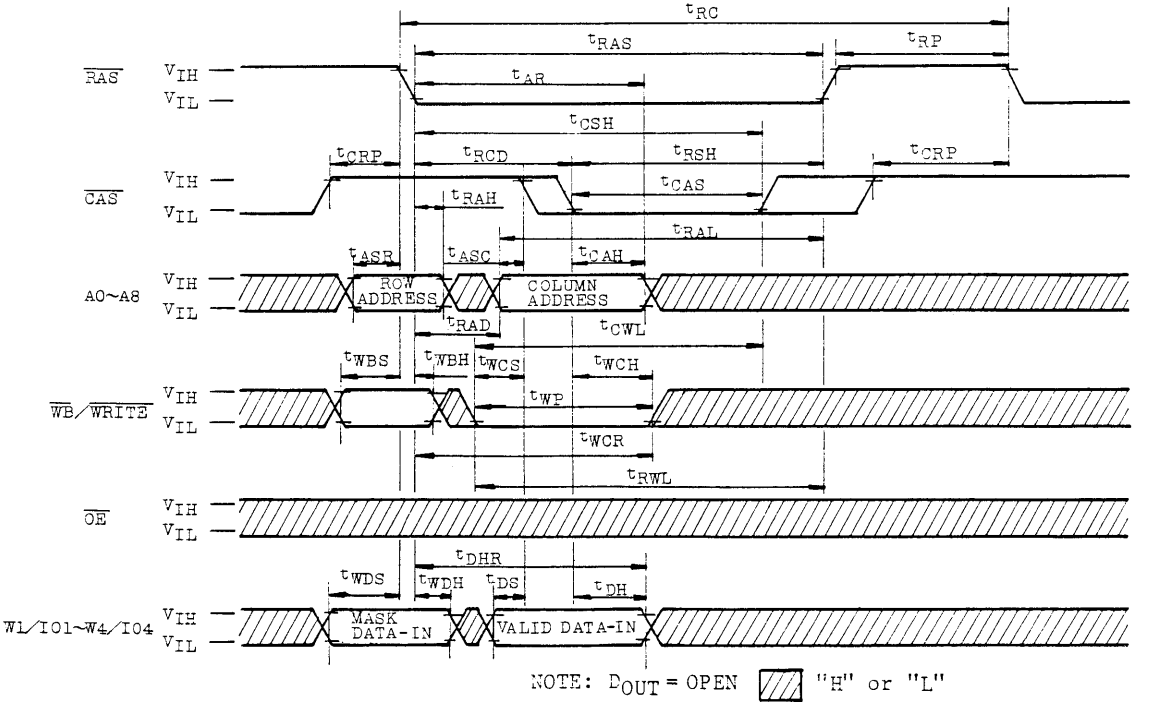
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



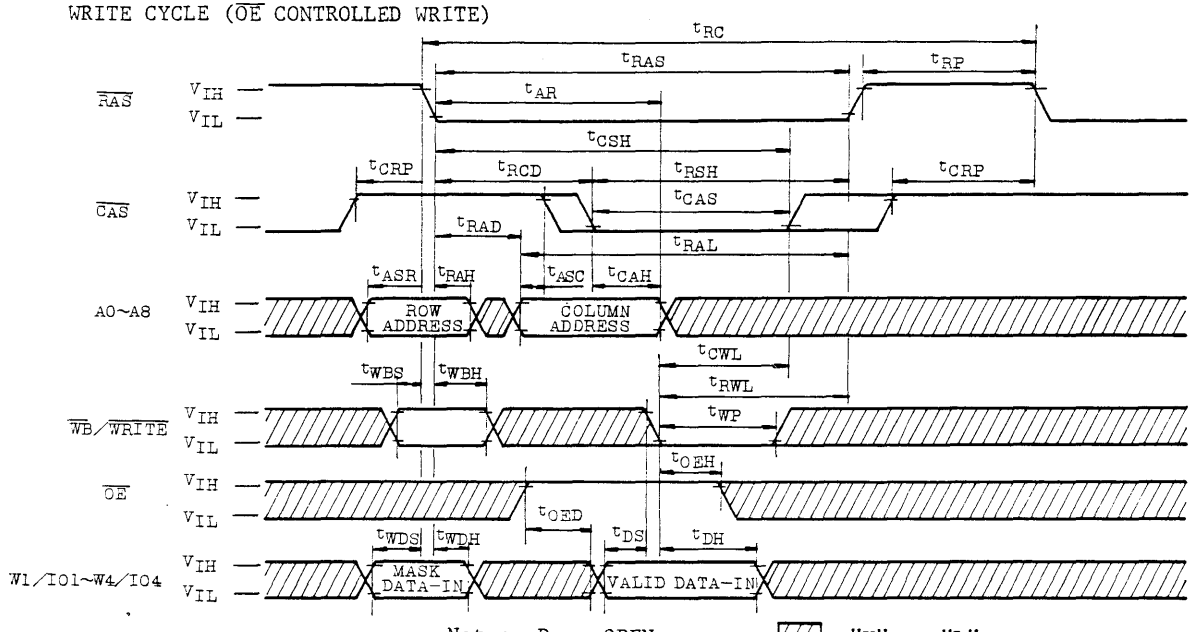
NOTE: D_{IN} = "H" or "L" ▨ "H" or "L"

WRITE CYCLE (EARLY WRITE)



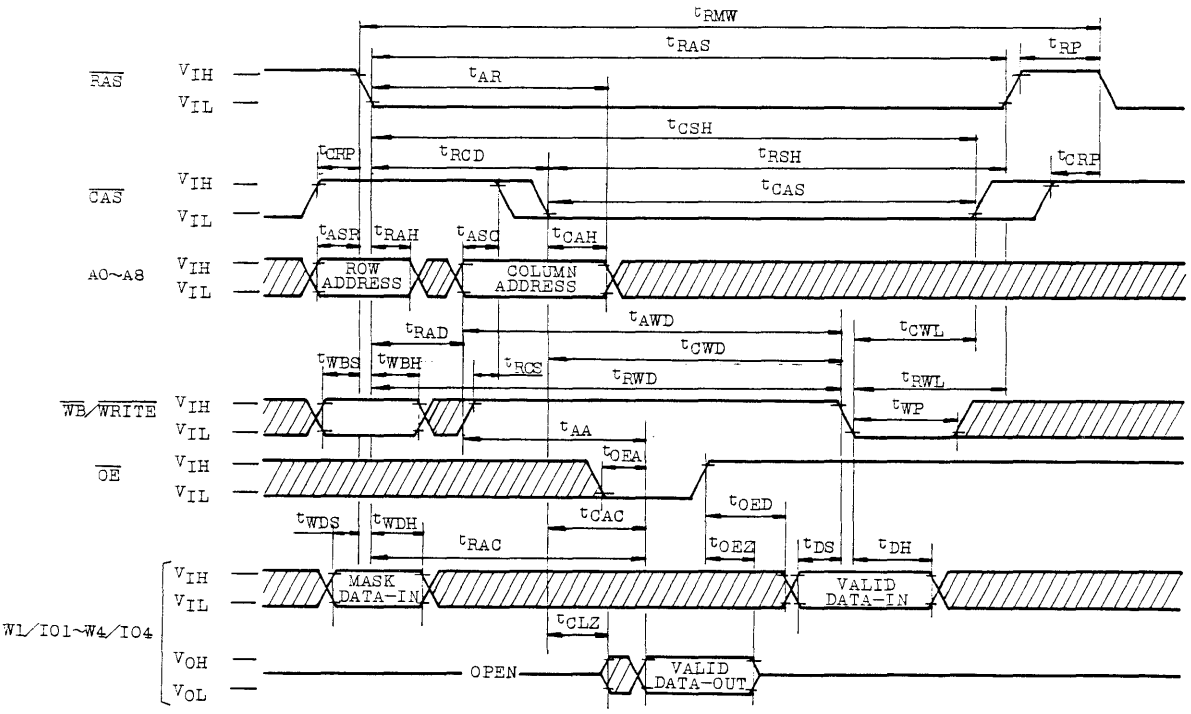
NOTE: D_{OUT} = OPEN ▨ "H" or "L"

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

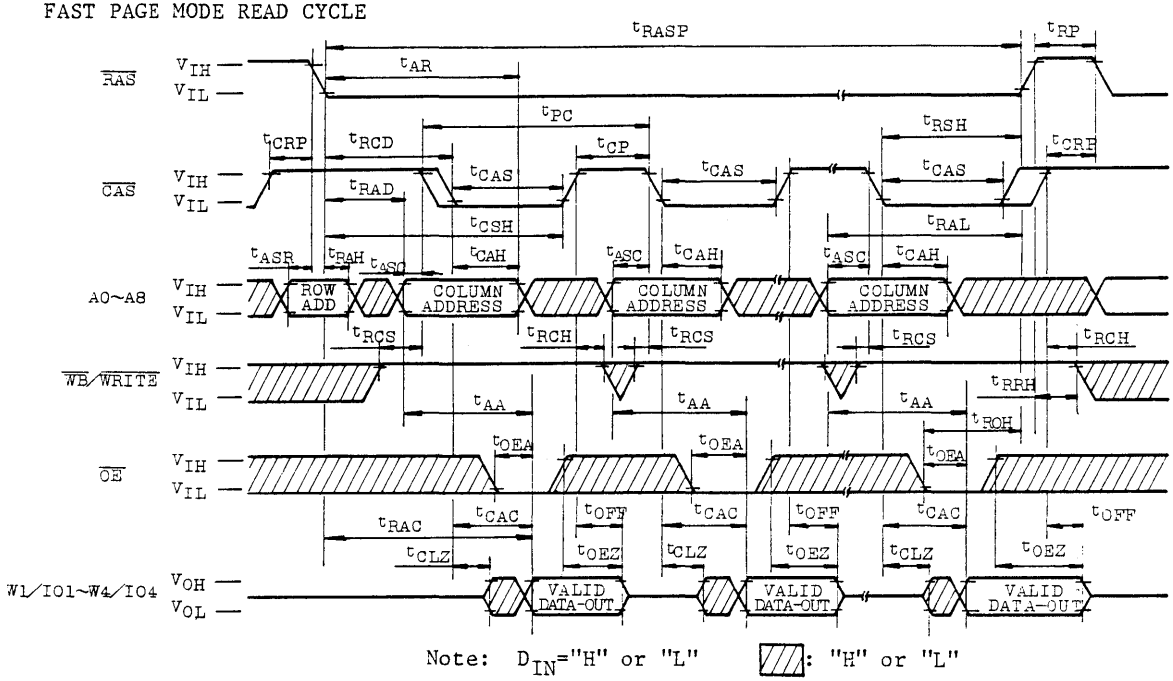


Note: D_{OUT}=OPEN ▨: "H" or "L"

READ-MODIFY-WRITE CYCLE

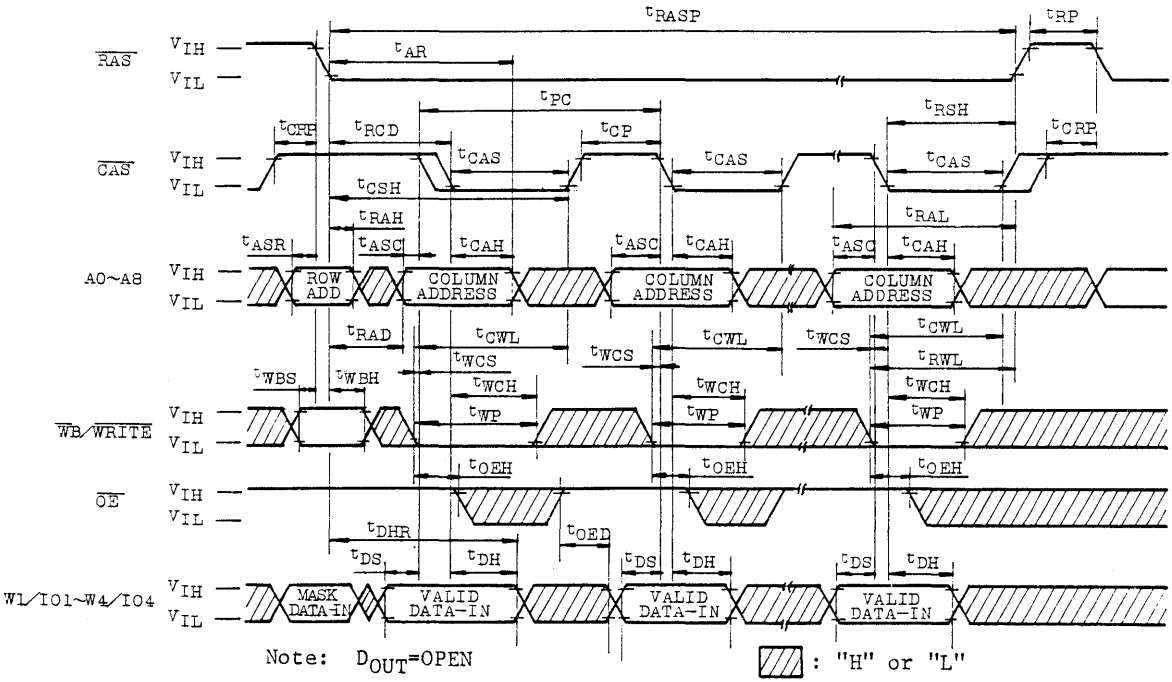


FAST PAGE MODE READ CYCLE



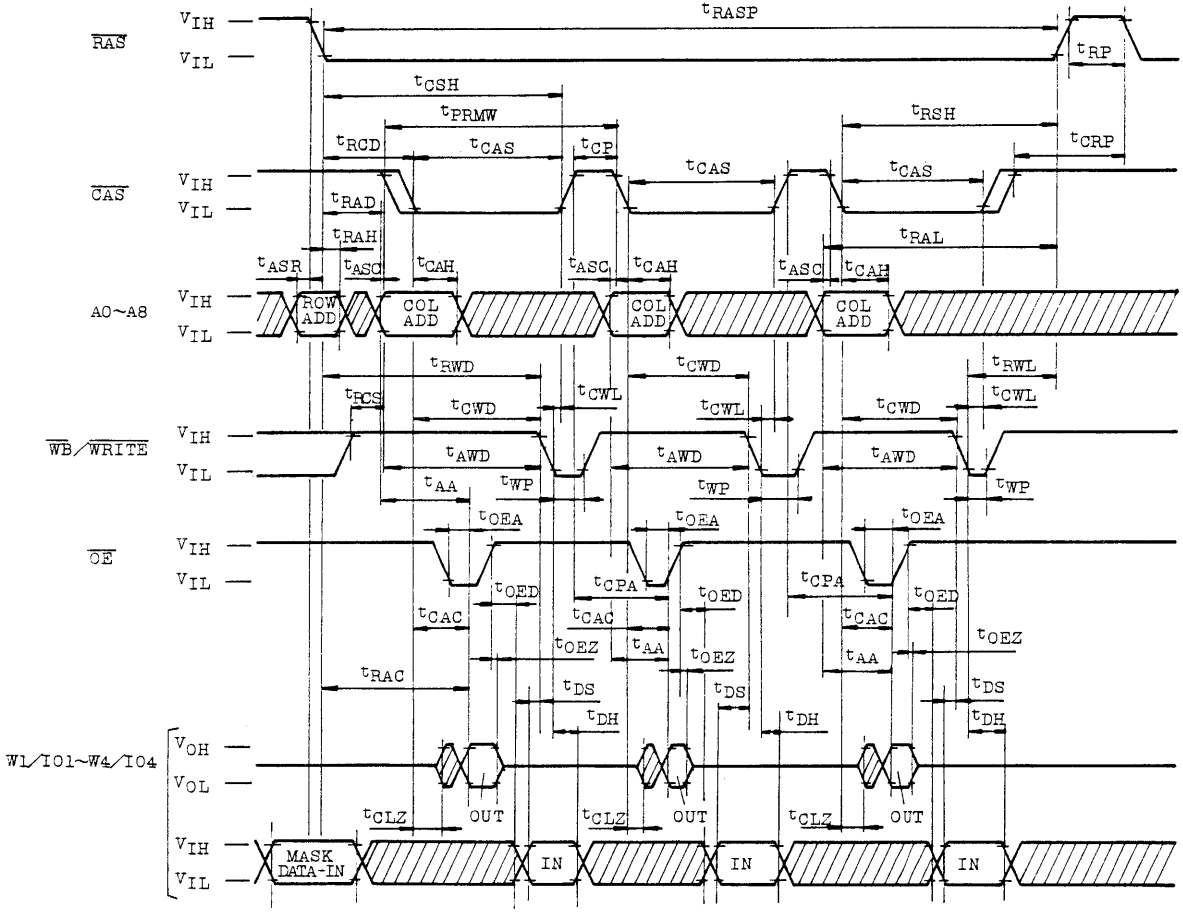
Note: D_{IN}="H" or "L" ▨: "H" or "L"

FAST PAGE MODE WRITE CYCLE

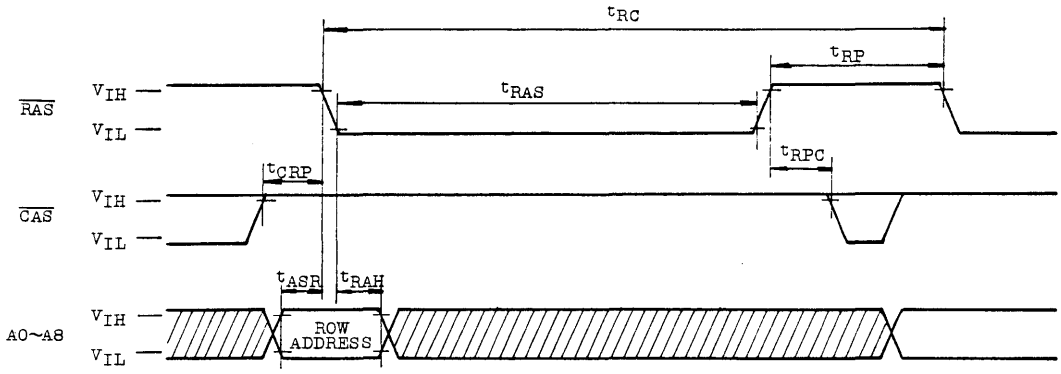


Note: D_{OUT}=OPEN ▨: "H" or "L"

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

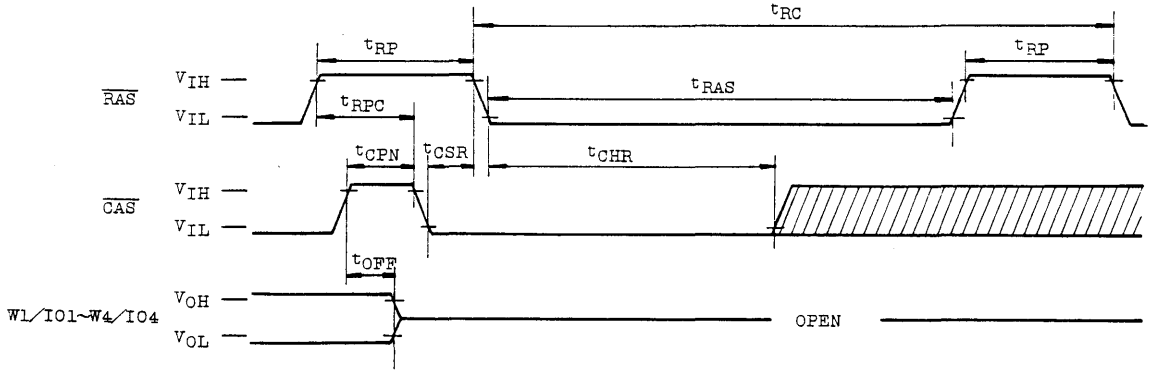


$\overline{RAS}$ ONLY REFRESH CYCLE



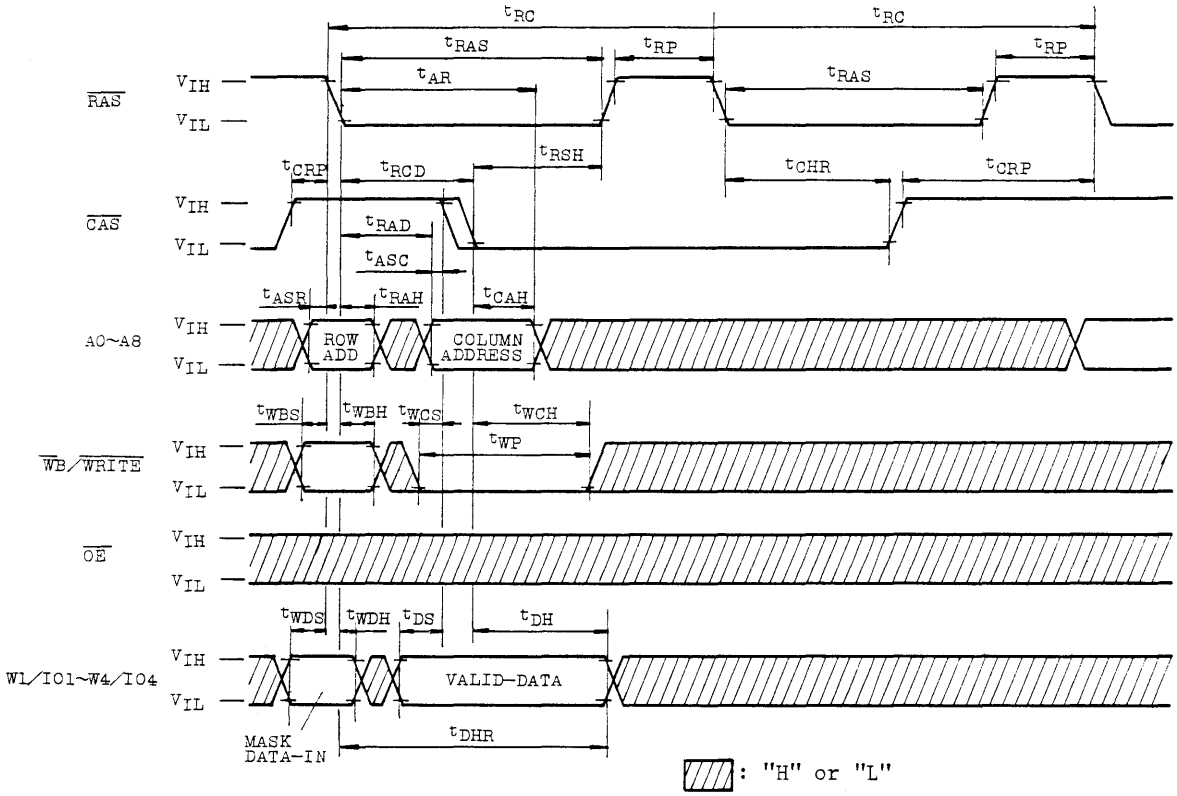
Note: $\overline{WB}/\overline{WRITE}$, $\overline{OE}$ = Don't Care ▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



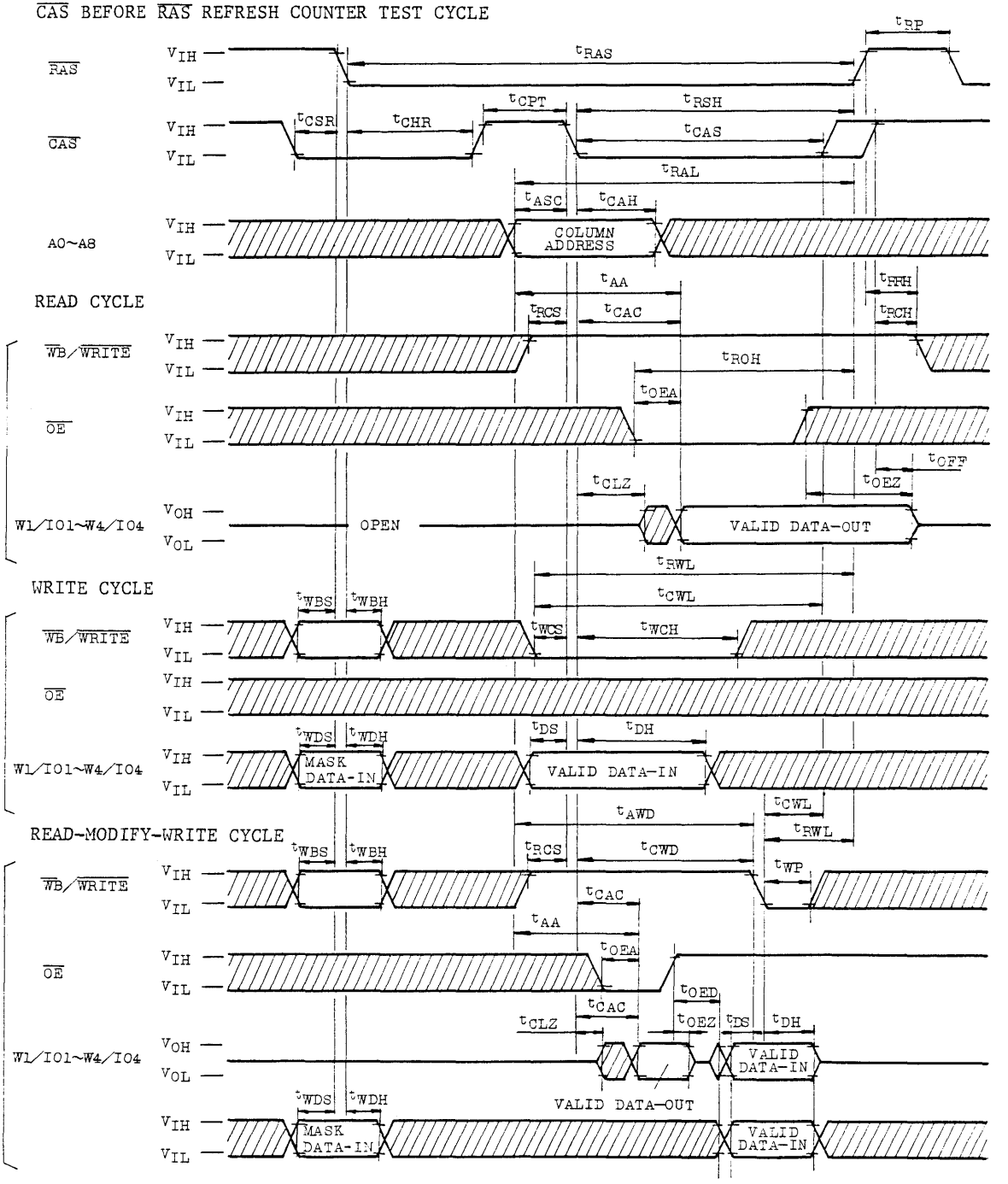
Note: $\overline{WB}/\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8 = "H" or "L" ▨: "H" or "L"

HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT}=OPEN

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TC514266AP/AJ/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, RAS, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hole Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Write Cycle. A write cycle is performed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes data on (Wi)IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi(/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.
For those data bits of Wi(/IOi) that are kept low as $\overline{RAS}$ talls the write operation is inhibited on the chip if $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0 ∿ A8) within each 8 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

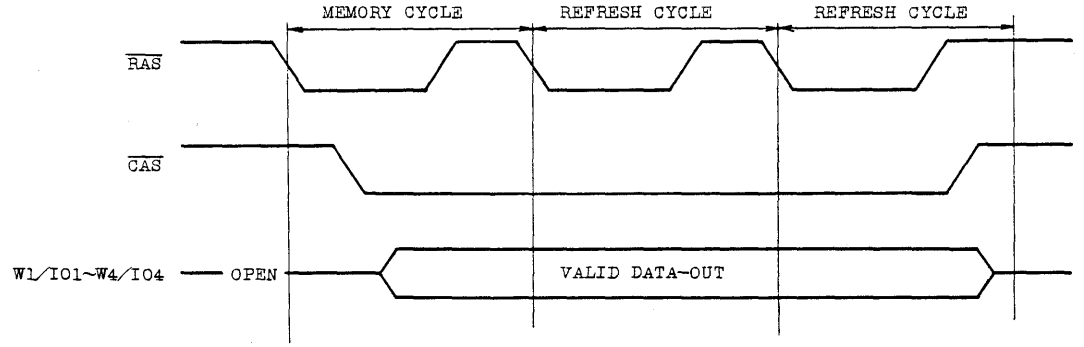
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514266AP/AJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514266AP/AJ/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514266AP/AJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of TC514266AP/AJ/AZ can be tested by $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

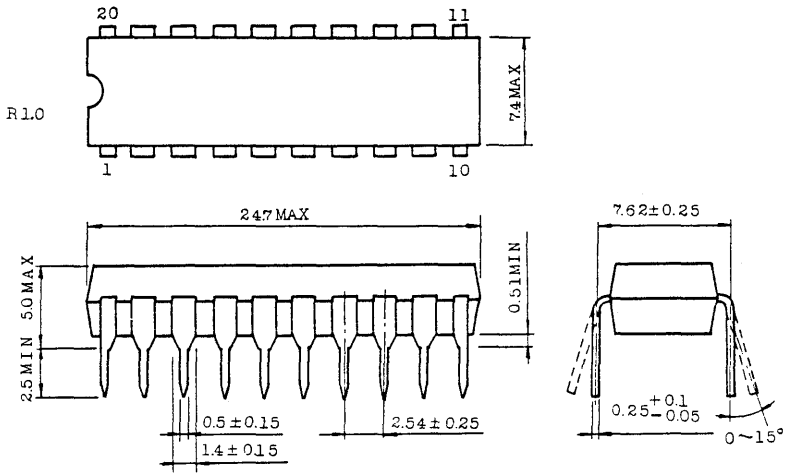
⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

OUTLINE DRAWINGS

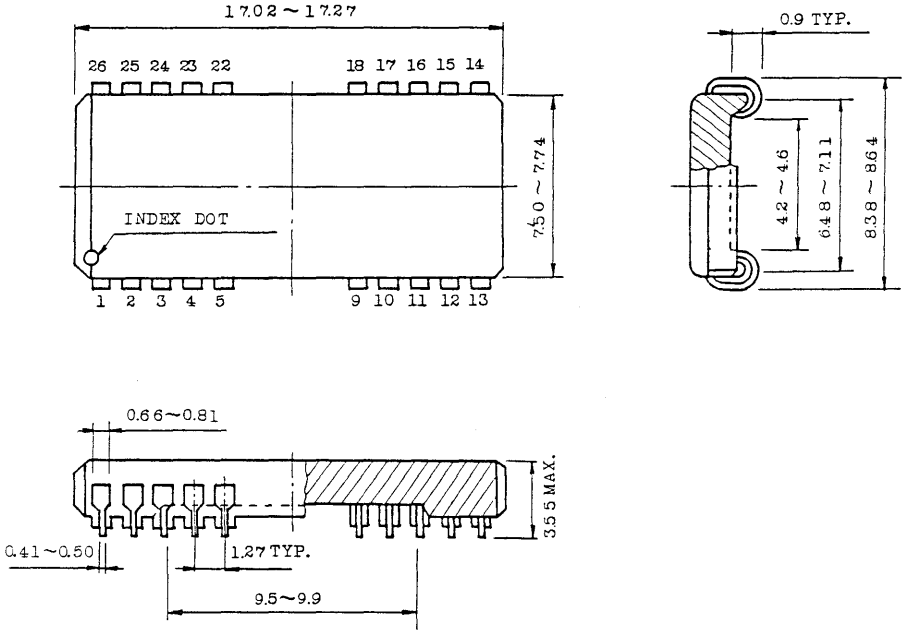
• Plastic DIP

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.29 leads.
All dimensions are in millimeters.

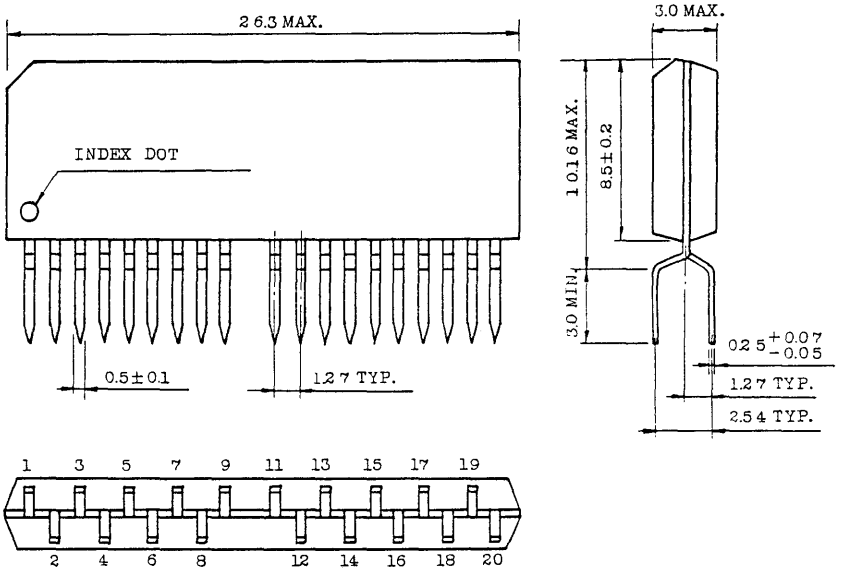
- Plastic SOJ



Note: Each lead pitch 1.27mm.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

262,144 WORD×4 BIT DYNAMIC RAM

SILICON GATE CMOS

TC514258P/J/Z-85, TC514258P/J/Z-10 TC514258P/J/Z-12

DESCRIPTION

The TC514258P/J/Z is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514258 P/J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514258P/J/Z to be packaged in a standard 20 pin plastic DIP and 20/26 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

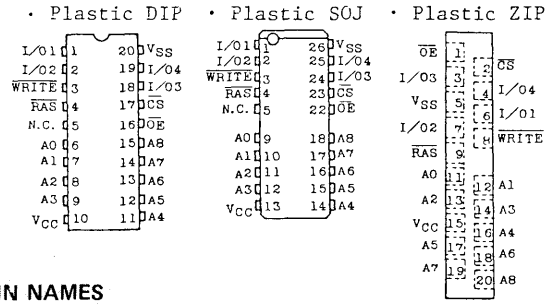
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514258P/J/Z-85-10-12		
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	30ns	30ns	35ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  413mW MAX. Operating (TC514258P/J/Z-85)
  358mW MAX. Operating (TC514258P/J/Z-10)
  303mW MAX. Operating (TC514258P/J/Z-12)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Static Column Mode capability
- All inputs and outputs TTL complatible
- 512 refresh cycles/8ms
- Package Plastic DIP : TC514258P
  Plastic SOJ : TC514258J
  Plastic ZIP : TC514258Z

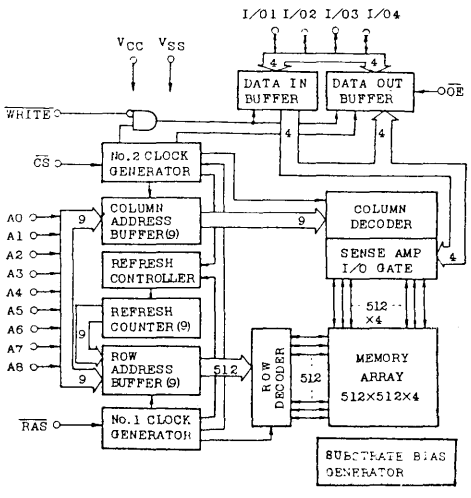
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/01 ~ I/04	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1 ~ 7	V	1
Output Voltage	V_{OUT}	−1 ~ 7	V	1
Power Supply Voltage	V_{CC}	−1 ~ 7	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	−55 ~ 150	°C	1
Soldering Temperature•Time	T_{SOLDER}	260•10	°C•sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta = 0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $Ta = 0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	UNIT	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514258P/J/Z-85	–	75	mA	3, 4
		TC514258P/J/Z-10	–	65		
		TC514258P/J/Z-12	–	55		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514258P/J/Z-85	–	75	mA	3
		TC514258P/J/Z-10	–	65		
		TC514258P/J/Z-12	–	55		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC514258P/J/Z-85	–	55	mA	3, 4
		TC514258P/J/Z-10	–	45		
		TC514258P/J/Z-12	–	35		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC}$-0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514258P/J/Z-85	–	75	mA	
		TC514258P/J/Z-10	–	65		
		TC514258P/J/Z-12	–	55		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, $0V \leqq V_{OUT} \leqq 5.5V$)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	–	190	–	220	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	225	–	255	–	295	–	ns	
t_{SC}	Static Column Mode Cycle Time	50	–	55	–	65	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	125	–	135	–	160	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	85	–	100	–	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CS}$	–	30	–	30	–	35	ns	8, 13
t_{AA}	Access Time from Column Address	–	45	–	50	–	60	ns	9, 14
t_{ALW}	Access Time from Last Write	–	85	–	95	–	115	ns	8, 15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	–	5	–	5	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	–	5	–	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	30	–	30	–	35	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	30	–	30	–	35	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	–	100	–	120	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	30	10,000	30	10,000	35	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	30	100,000	30	100,000	35	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	55	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	–	15	–	20	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	–	10	–	15	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	20	–	20	–	25	–	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	–	115	–	140	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	50	–	60	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	–	10	–	15	–	ns	16
t_{LWAD}	Last Write to Column Address Delay Time	25	40	25	45	30	55	ns	17
t_{AHLW}	Last Write to Column Address Hold Time	85	–	95	–	115	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514258P/J/Z-85		TC514258P/J/Z-10		TC514258P/J/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	–	0	–	0	–	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{WP}	$\overline{WRITE}$ Pulse Width	20	–	20	–	25	–	ns	
t_{WI}	$\overline{WRITE}$ Inactive Time	10	–	10	–	15	–	ns	
t_{RWL}	$\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	–	25	–	30	–	ns	
t_{CWL}	$\overline{WRITE}$ Command to $\overline{CS}$ Lead Time	20	–	25	–	30	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data-In Hold Time	20	–	20	–	25	–	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	–	75	–	90	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WS}	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	–	0	–	0	–	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	65	–	65	–	75	–	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	120	–	135	–	160	–	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	80	–	85	–	100	–	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	–	10	–	10	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	–	30	–	30	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	50	–	50	–	60	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	–	20	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	30	–	30	–	35	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	25	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

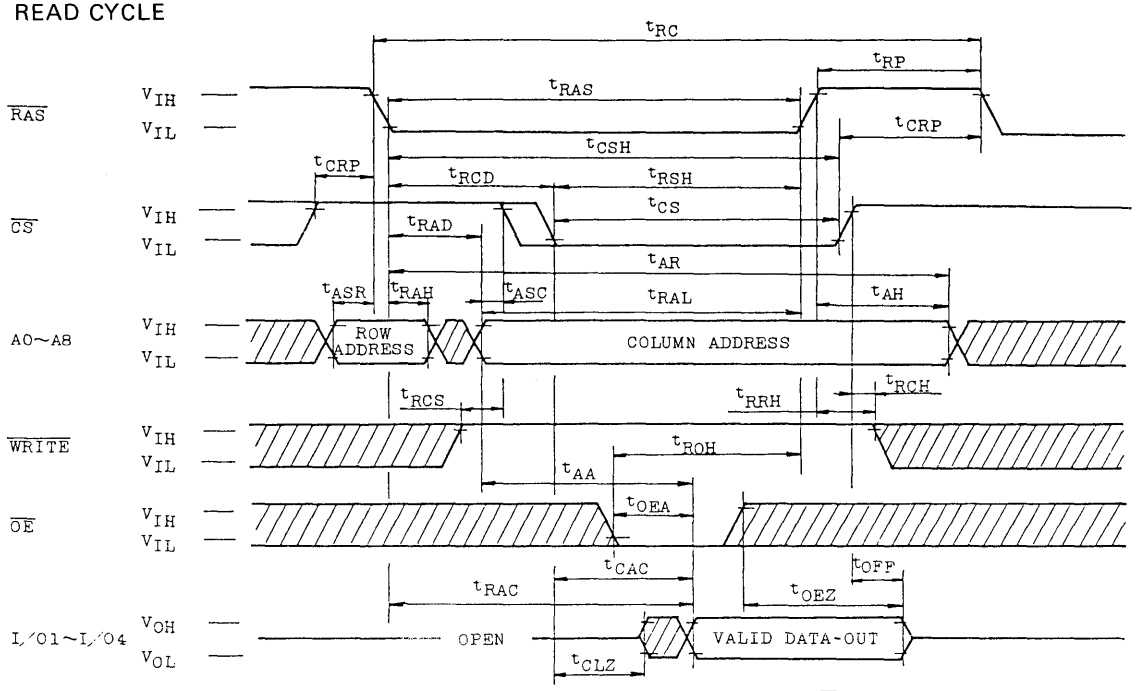
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{11}	Input Capacitance ($A_0 \sim A_8$)	–	5	pF
C_{12}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_0	Output Capacitance ($I/O_1 \sim I/O_4$)	–	7	pF

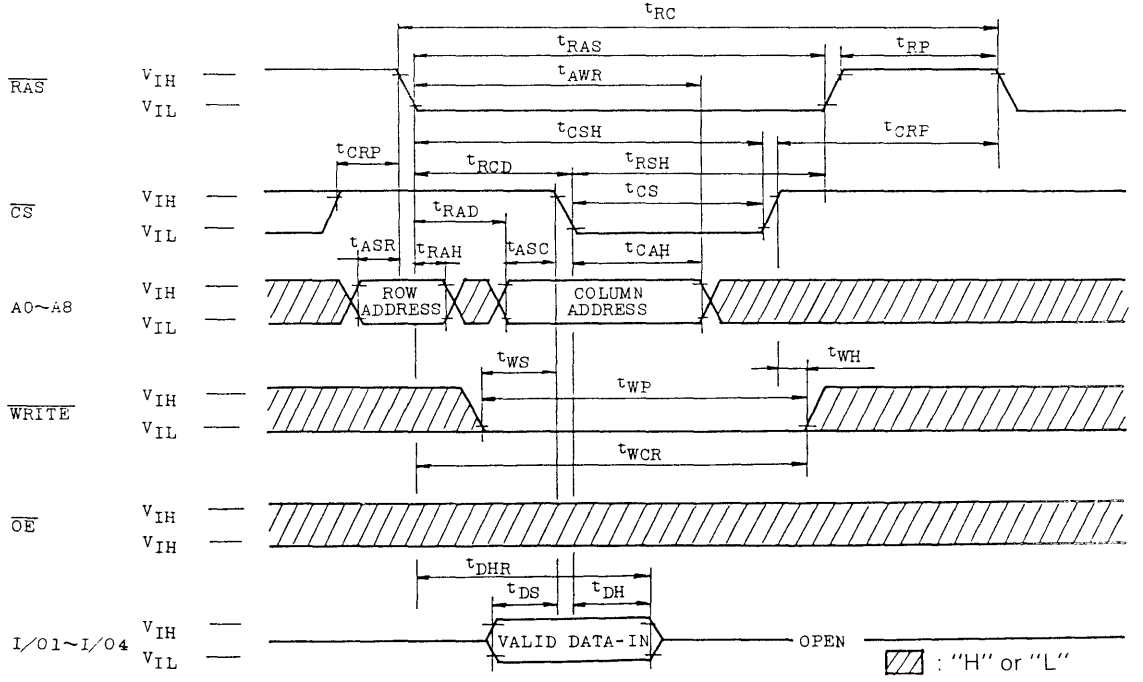
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T= 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a Read-Modify-Wrete cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater then the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

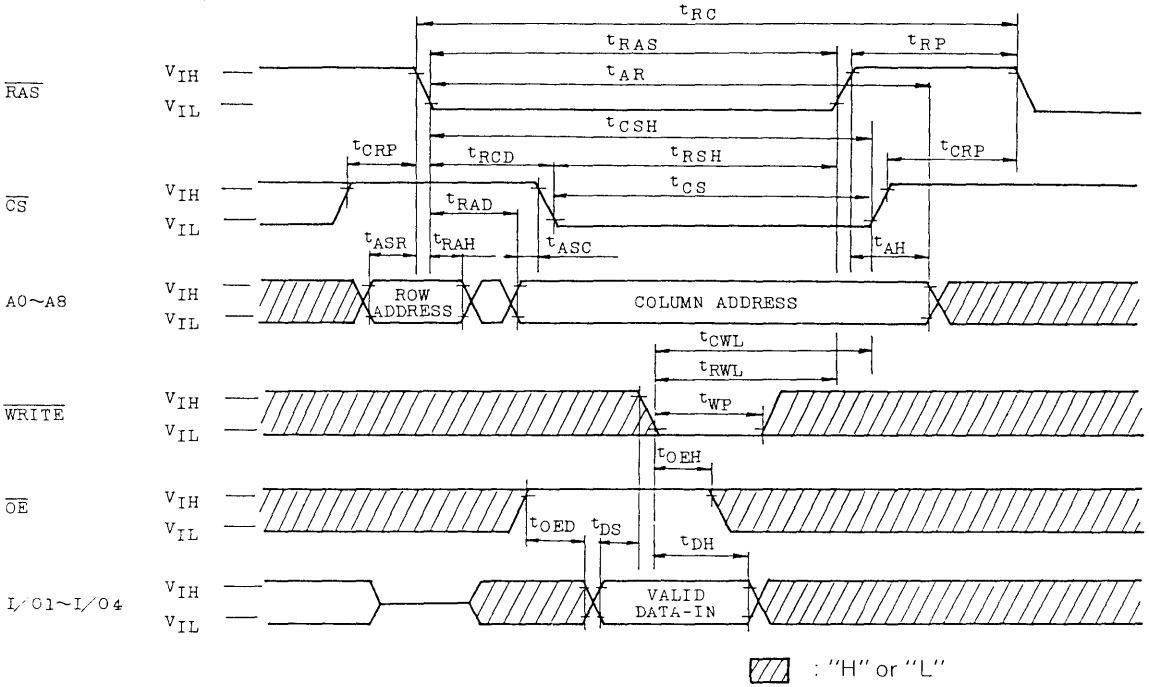
- READ CYCLE



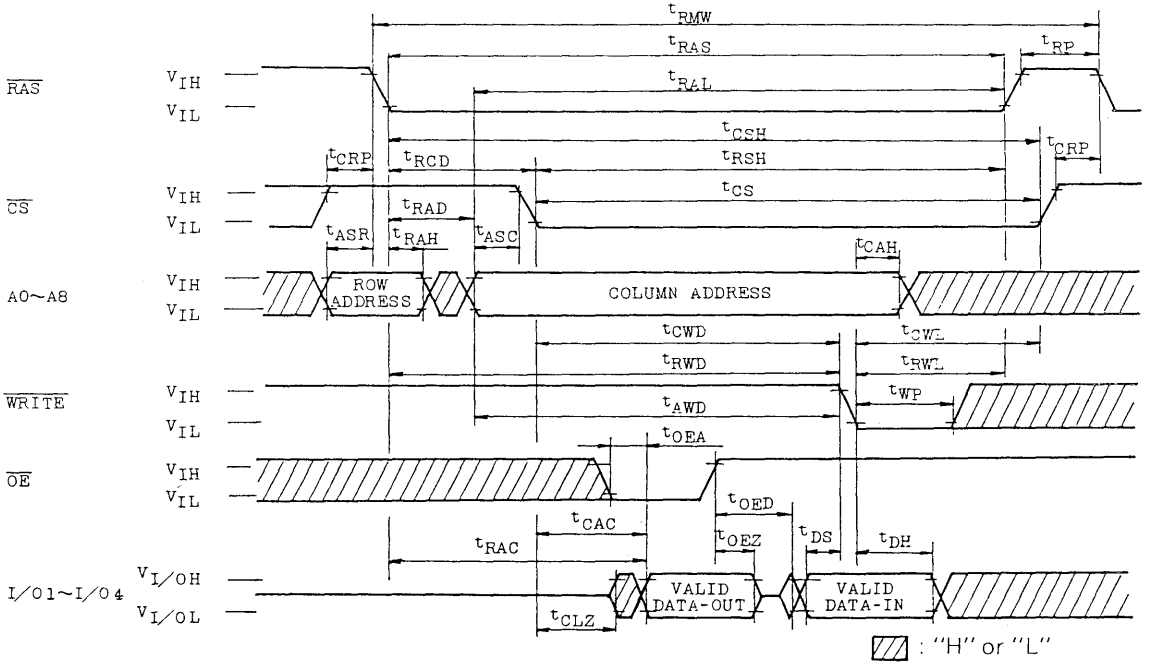
- WRITE CYCLE (EARLY WRITE)



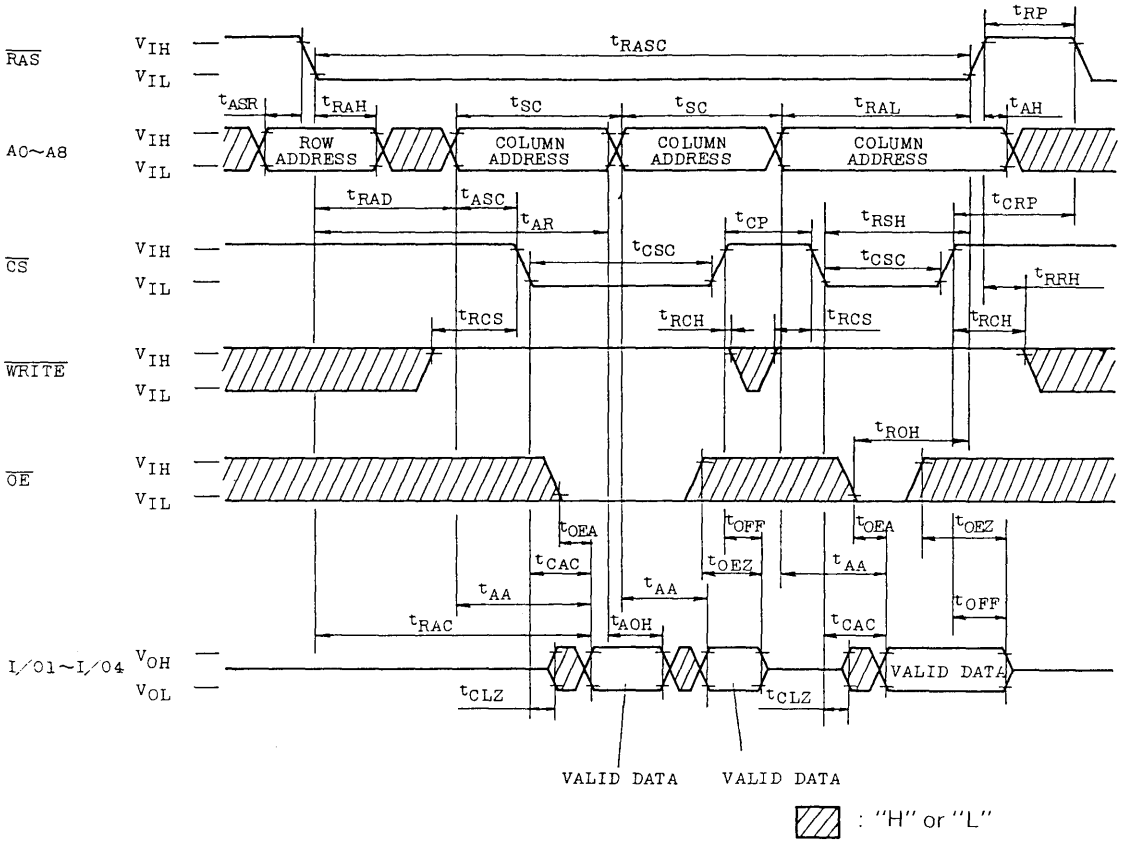
● WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



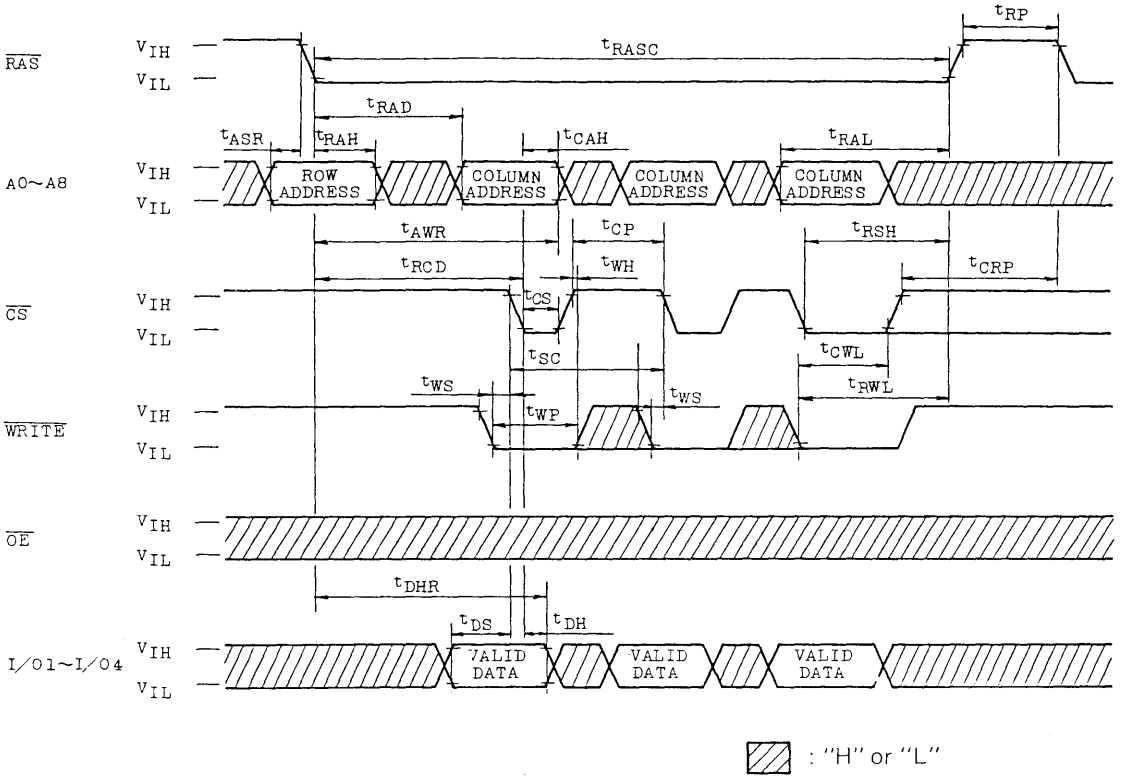
● READ-MODIFY-WRITE CYCLE



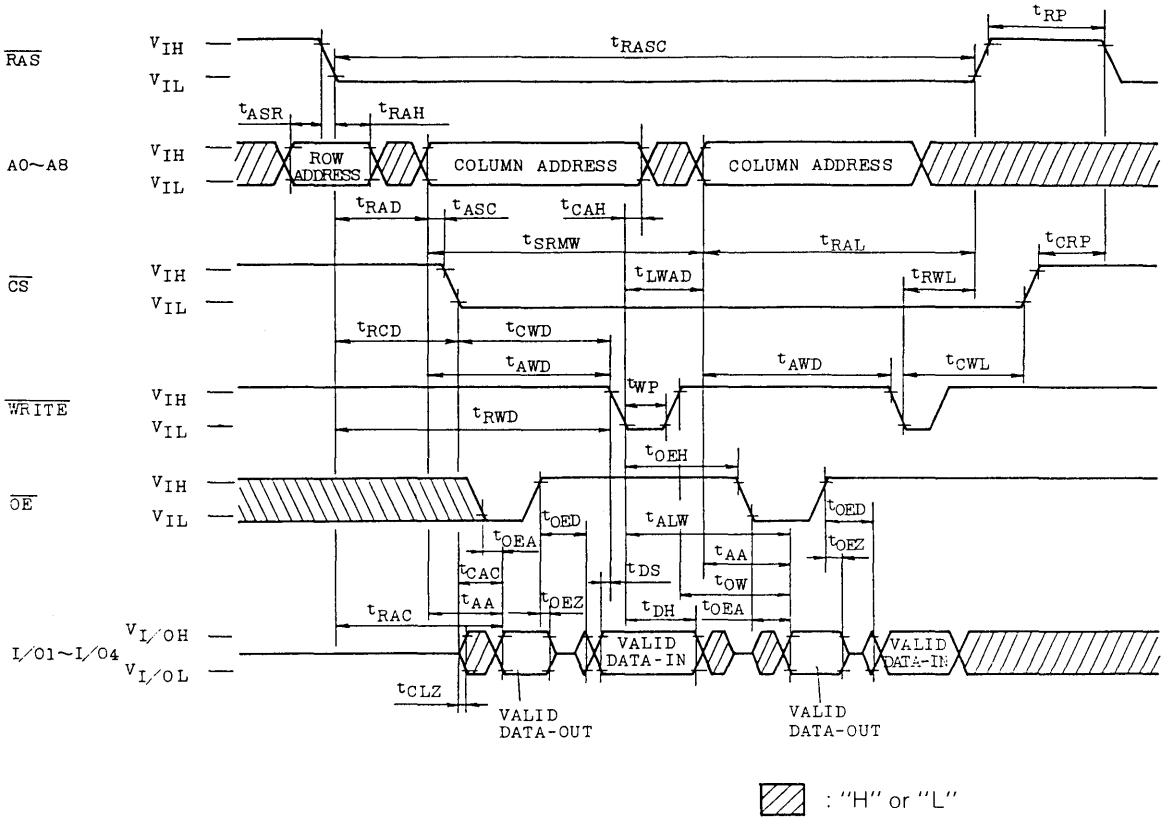
- STATIC COLUMN MODE READ CYCLE



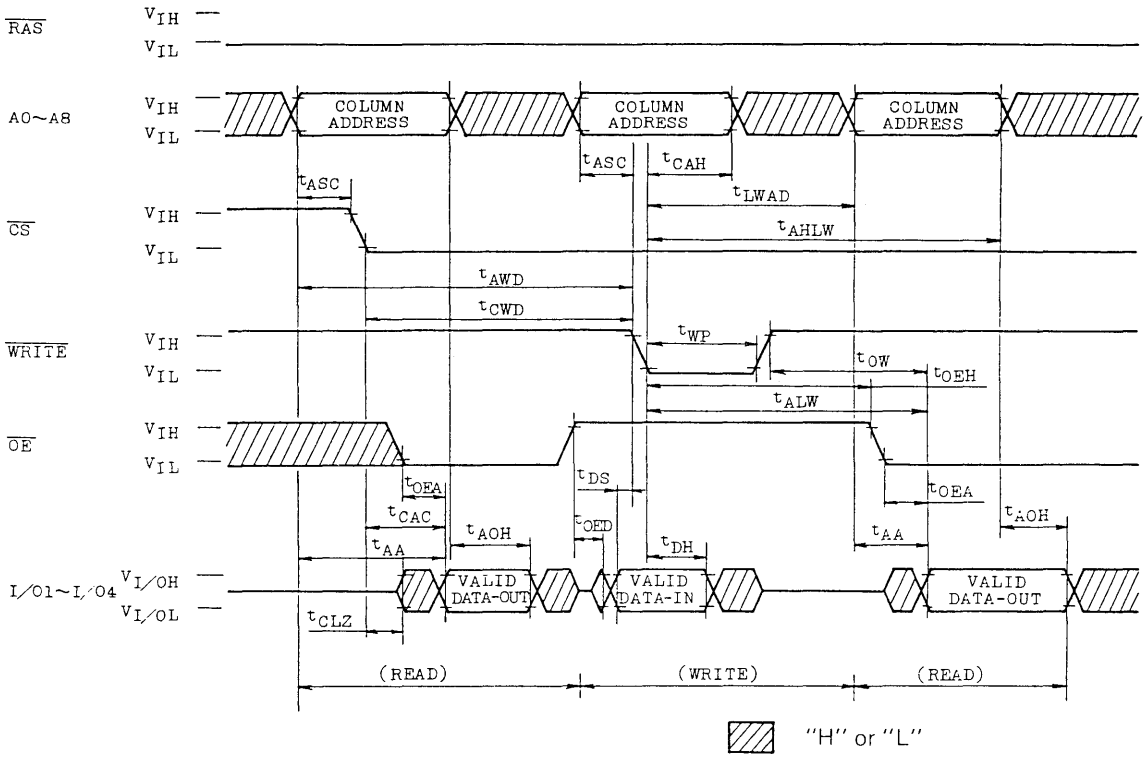
- STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



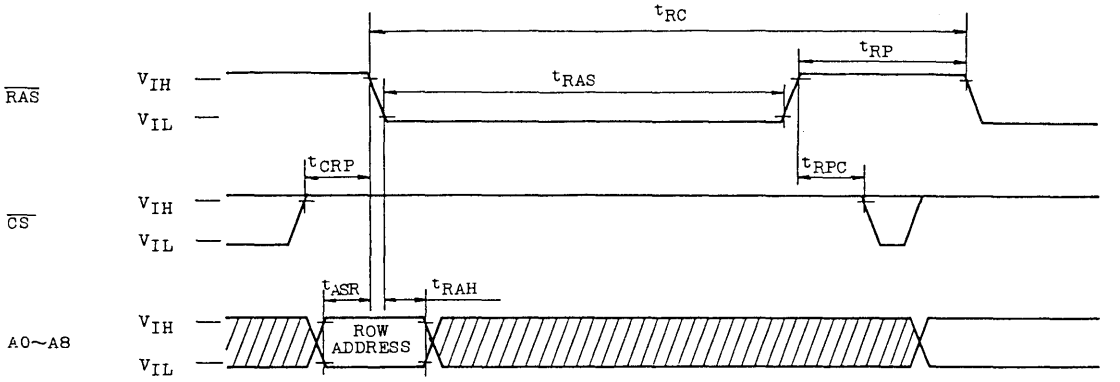
- STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



- STATIC COLUMN MODE READ/WRITE MIXED CYCLE



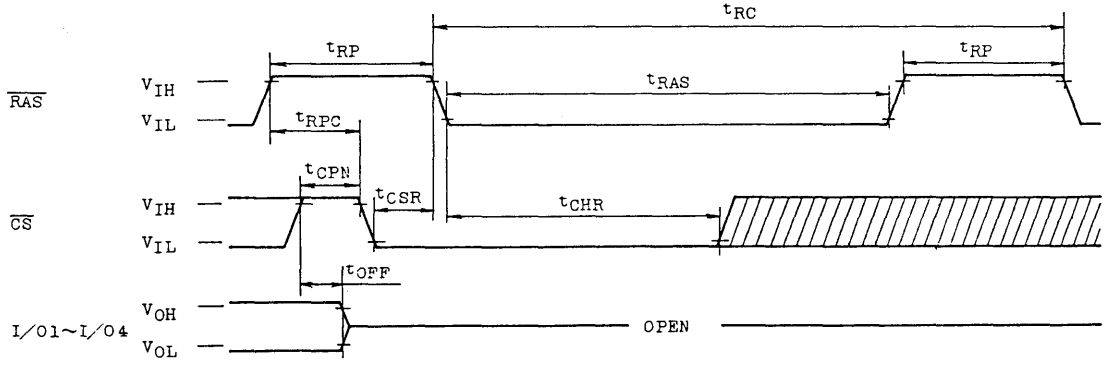
- $\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

▨ "H" or "L"

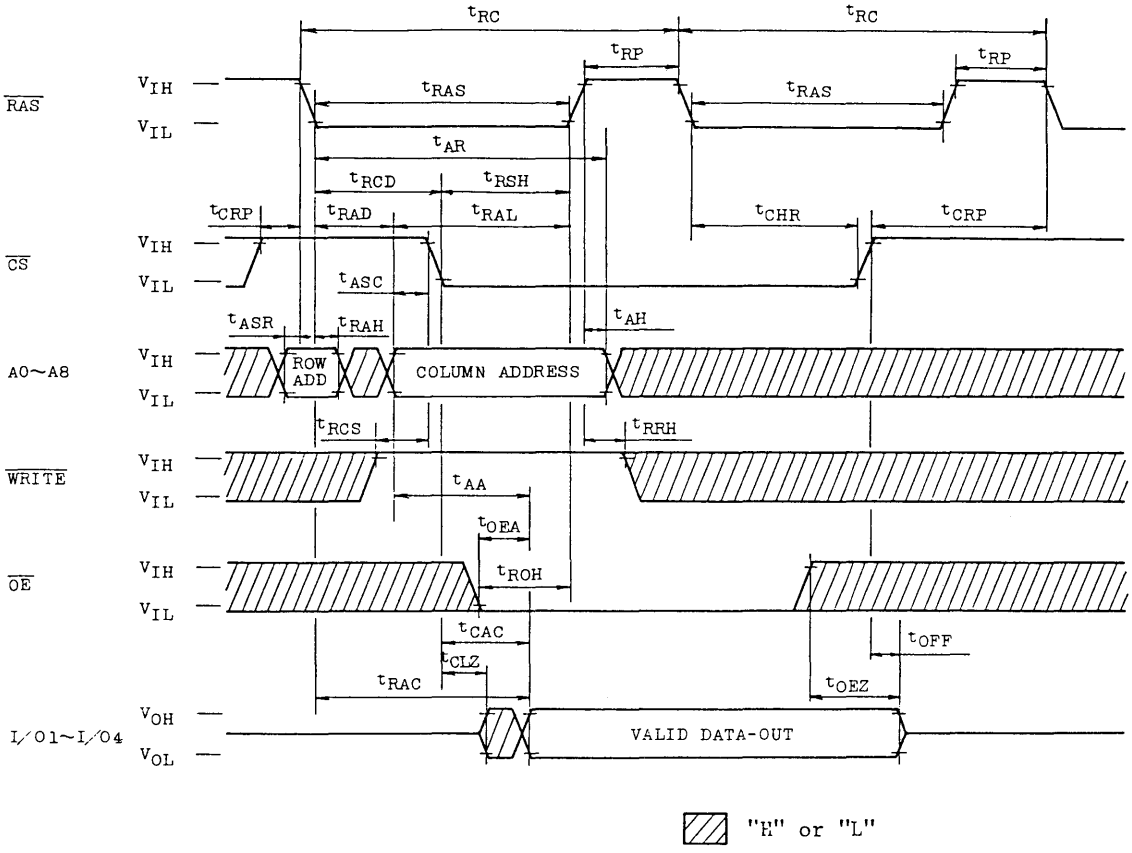
- $\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



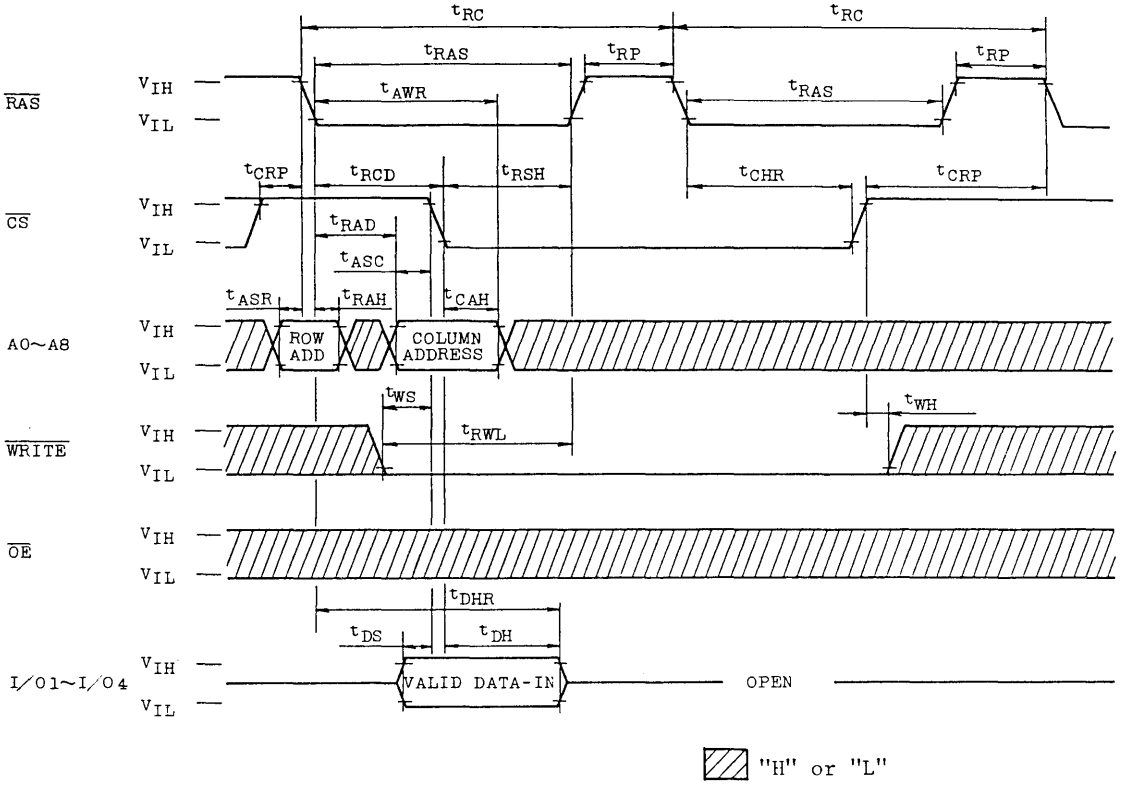
NOTE: $\overline{WRITE}$, $\overline{OE}$, A0 ~ A8 = "H" or "L"

▨ "H" or "L"

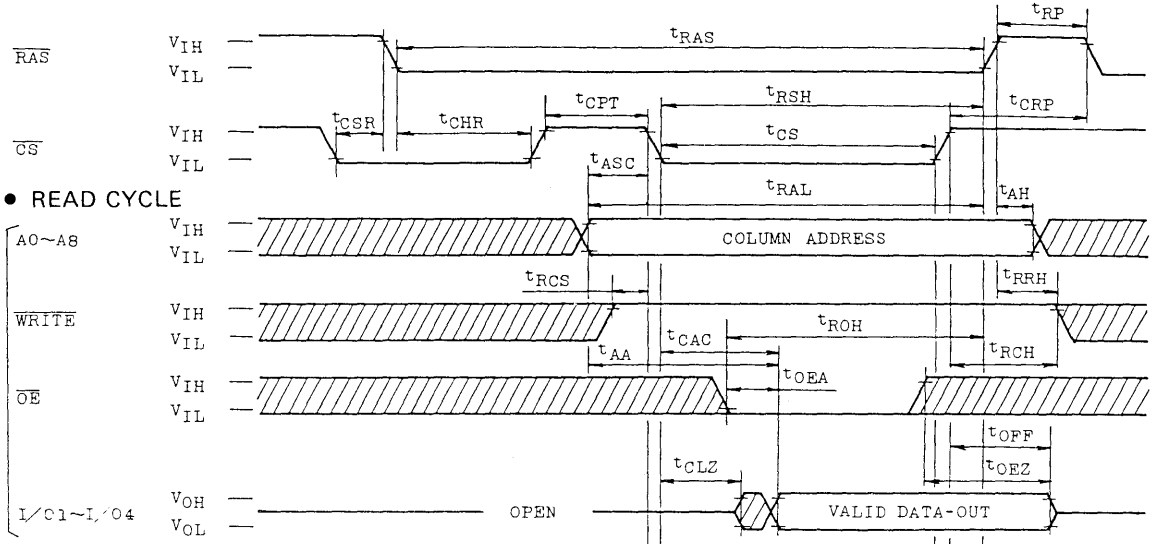
- HIDDEN REFRESH CYCLE (READ)



- HIDDEN REFRESH CYCLE (WRITE)

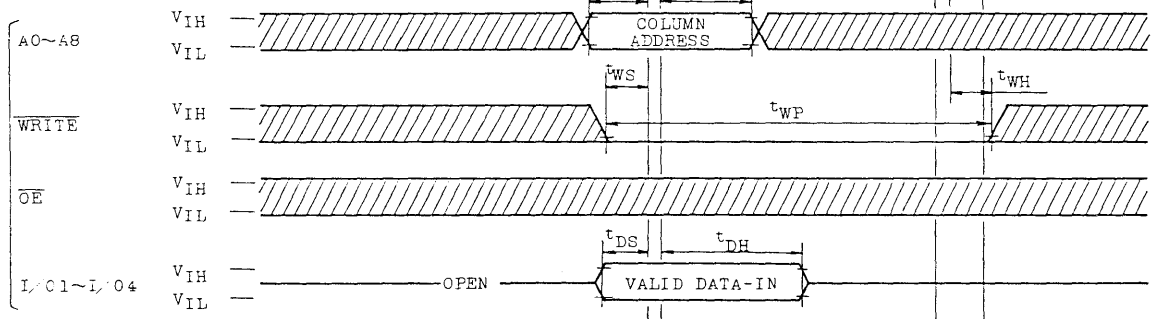


- $\overline{CS}$ BEFORE RAS REFRESH COUNTER TEST CYCLE

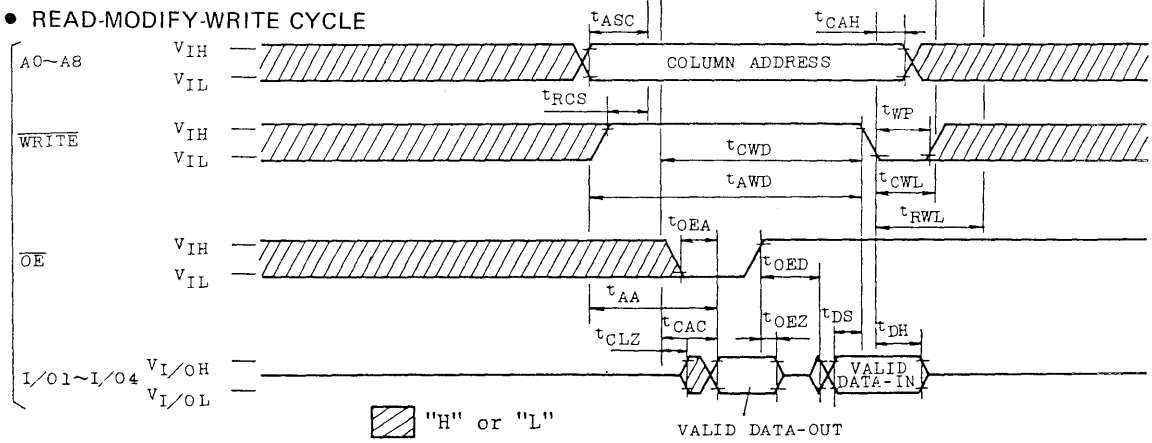


- READ CYCLE

- WRITE CYCLE



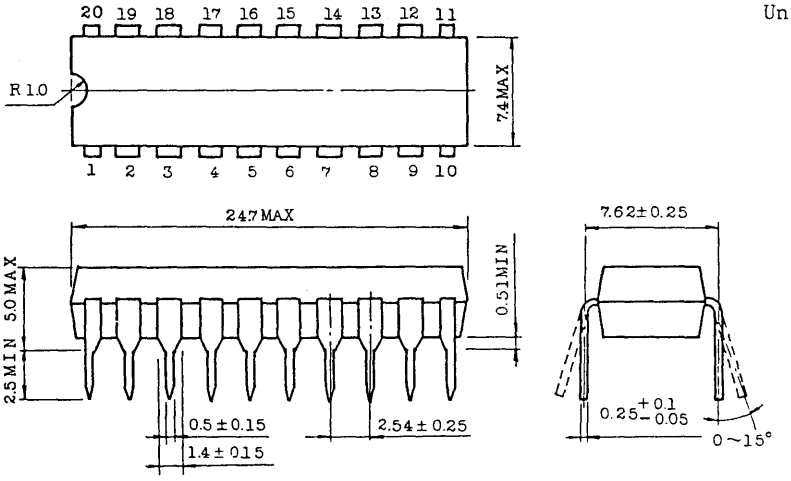
- READ-MODIFY-WRITE CYCLE



OUTLINE DRAWINGS

- Plastic DIP

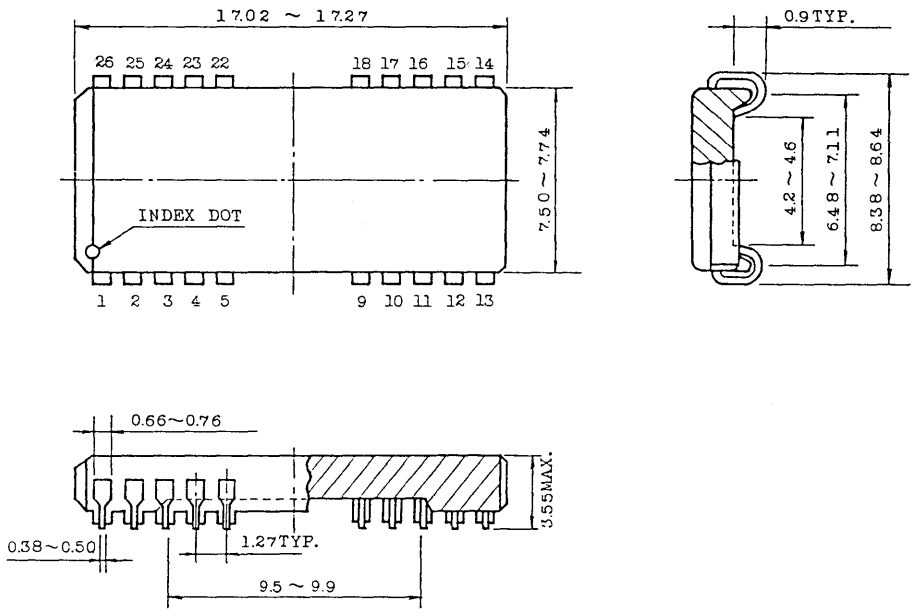
Unit in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 20 leads.
All dimensions are in millimeters.

- Plastic SOJ

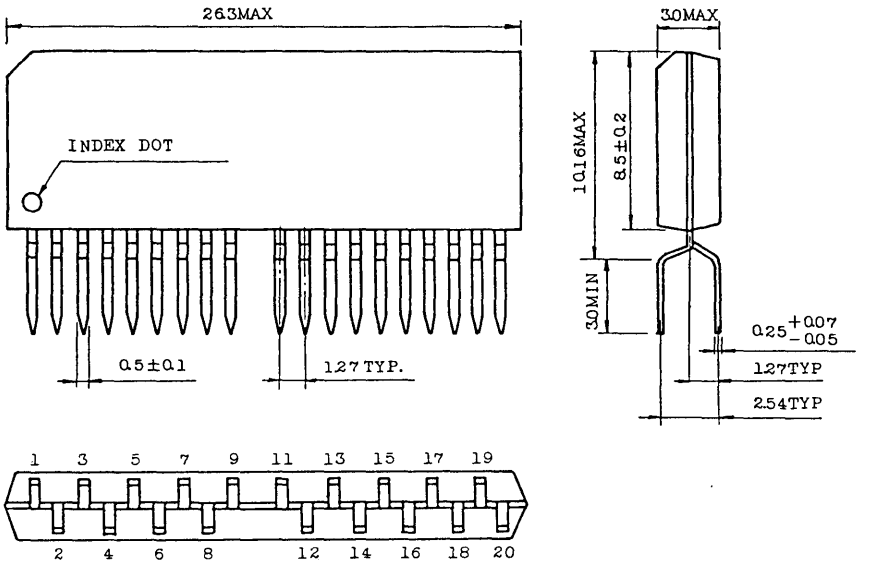
Unit in mm



NOTE: Each lead pitch 1.27mm. All dimensions are in millimeters.

- **Plastic ZIP**

Unit in mm



NOTE: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC514258AP/AJ/AZ-70, TC514258AP/AJ/AZ-80
TC514258AP/AJ/AZ-10

DESCRIPTION

The TC514258AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514258AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514258AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

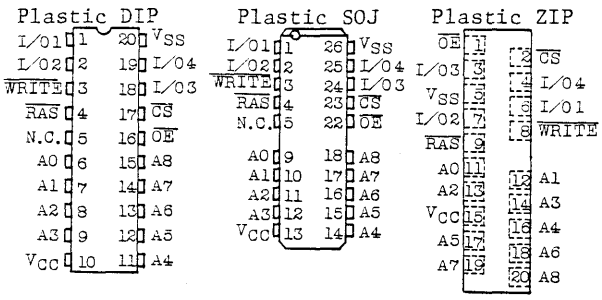
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514258AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  440mW MAX. Operating(TC514258AP/AJ/AZ-70)
  385mW MAX. Operating(TC514258AP/AJ/AZ-80)
  330mW MAX. Operating(TC514258AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514258AP
  Plastic SOJ: TC514258AJ
  Plastic ZIP: TC514258AZ

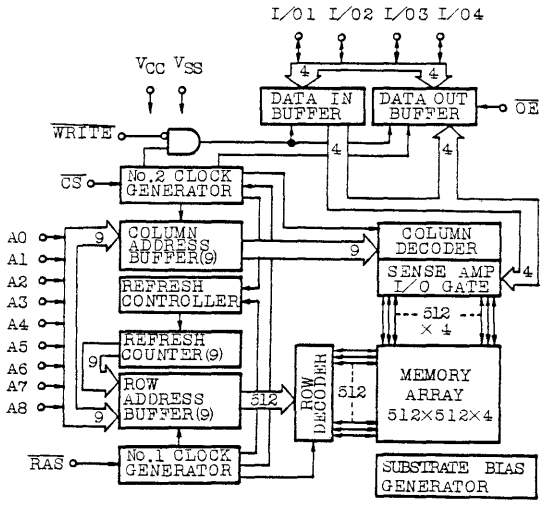
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	UNIT	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	TC514258AP/AJ/AZ-70	-	80	mA	3,4
		TC514258AP/AJ/AZ-80	-	70		
		TC514258AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514258AP/AJ/AZ-70	-	80	mA	3
		TC514258AP/AJ/AZ-80	-	70		
		TC514258AP/AJ/AZ-10	-	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514258AP/AJ/AZ-70	-	60	mA	3,4
		TC514258AP/AJ/AZ-80	-	50		
		TC514258AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514258AP/AJ/AZ-70	-	80	mA	3
		TC514258AP/AJ/AZ-80	-	70		
		TC514258AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V≦V_{IN}≦6.5V, All Other Pins Not Under Test = 0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V≦V_{OUT}≦5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ~ 70°C)(Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514258AP/AJ/AZ-70		TC514258AP/AJ/AZ-80		TC514258AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycl Time	100	-	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	8,15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	30	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	-	20	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width(Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	45	20	55	25	70	ns	13
t_{RAD}	$\overline{RAS}$ to Column Addre s Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0		0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	85	-	95	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10	-	10	-	10	-	ns	16

SYMBOL	PARAMETER	TC514258AP/AJ/AZ-70		TC514258AP/AJ/AZ-80		TC514258AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	17
t_{AHLW}	Last Write to Column Address Hold Time	65	-	75	-	95	-	ns	
t_{RCS}	Read Command Set-up Time Referenced to CS	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	-	15	-	20	-	ns	12
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	$\overline{WRITE}$ Pulse Width	15	-	15	-	20	-	ns	
t_{WI}	$\overline{WRITE}$ Inactive Time	10	-	10	-	10	-	ns	
t_{RWL}	$\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	$\overline{WRITE}$ Command to $\overline{CS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	55	-	55	-	65	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	100	-	110	-	135	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	85	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	-	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	25	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	9
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	

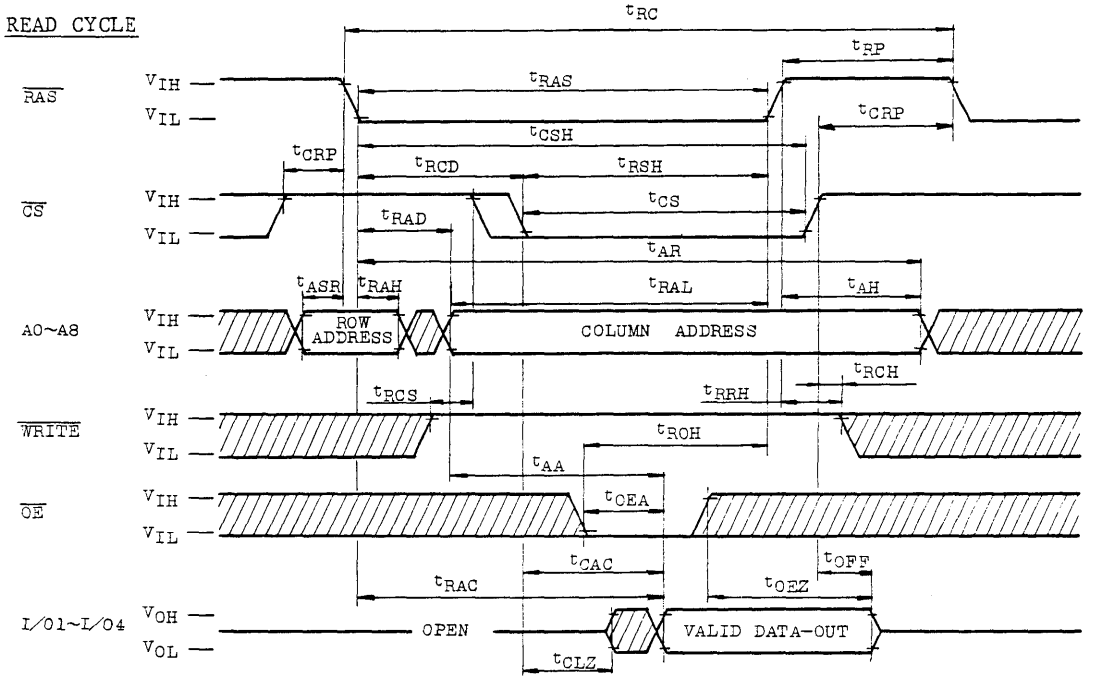
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance ($A_0 \sim A_8$)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Input Output Capacitance (I/O1 ∿ I/O4)	-	7	

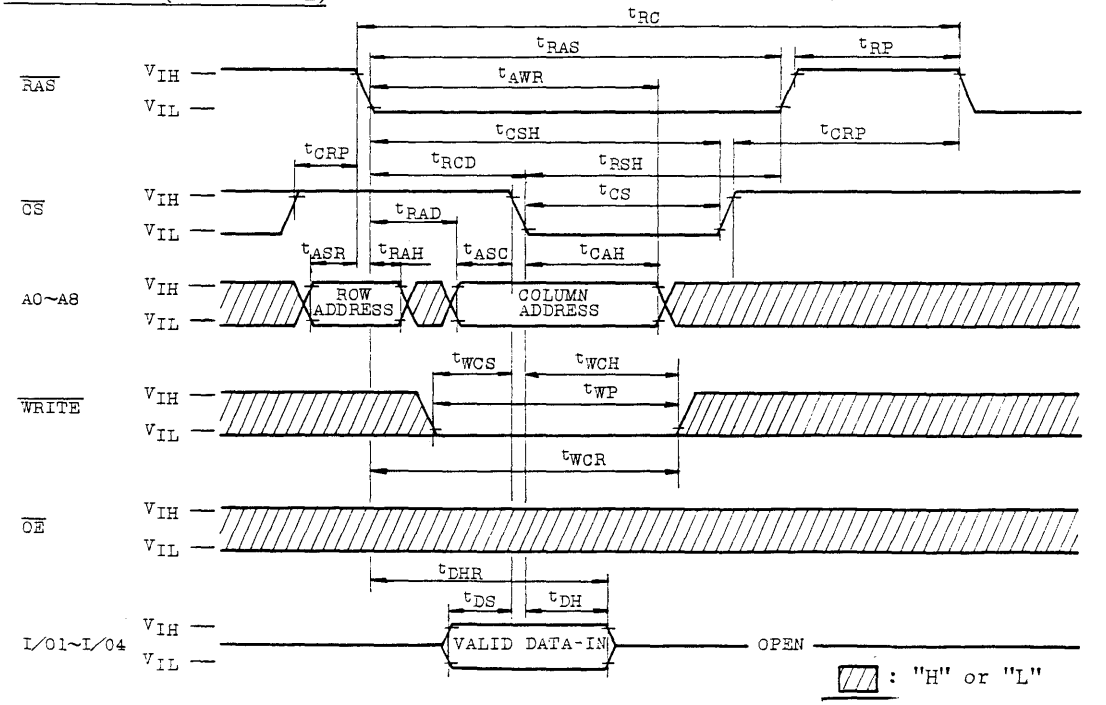
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. Icc1, Icc3, Icc4, Icc6 depend on cycle rate.
4. Icc1, Icc4 depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RPH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
12. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

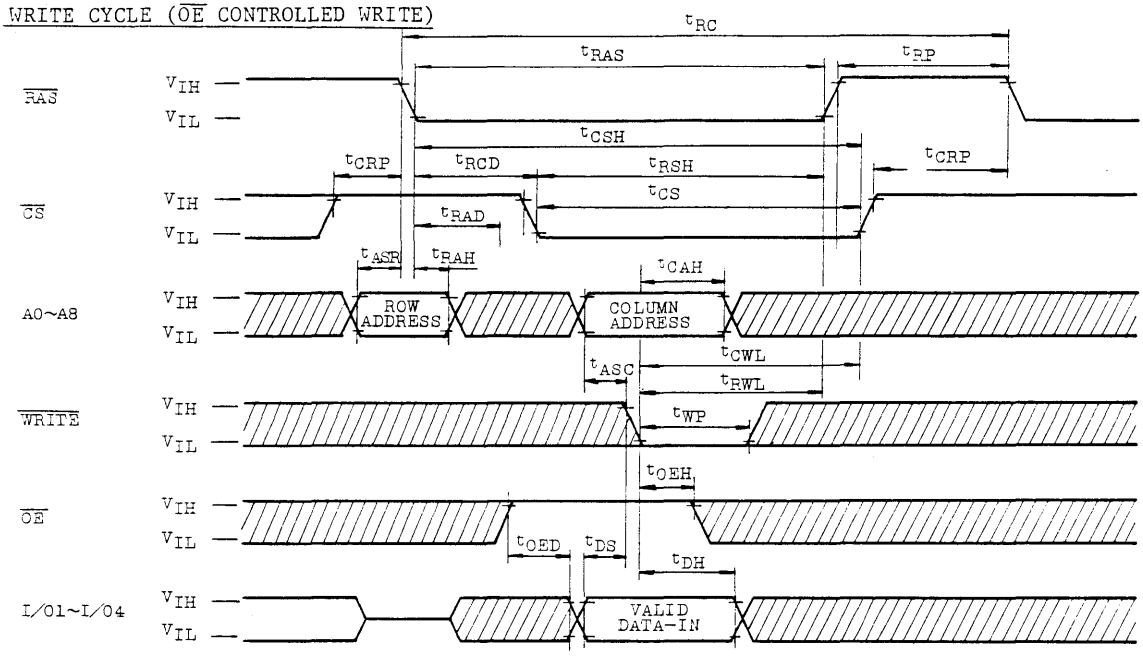
READ CYCLE



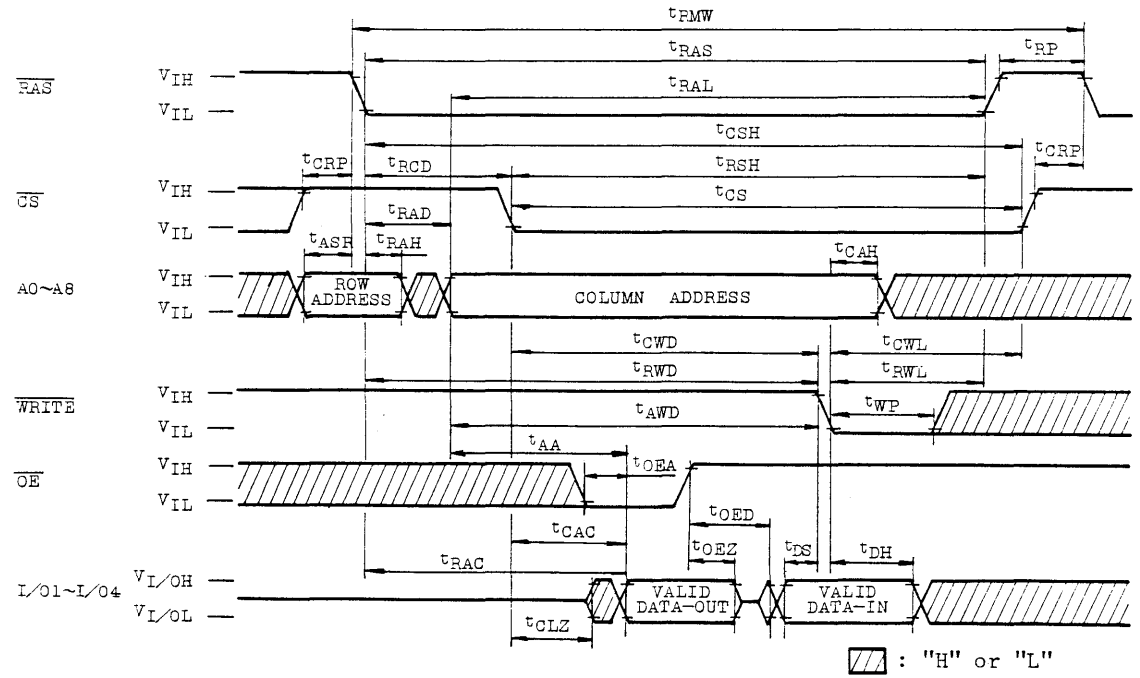
WRITE CYCLE (EARLY WRITE)



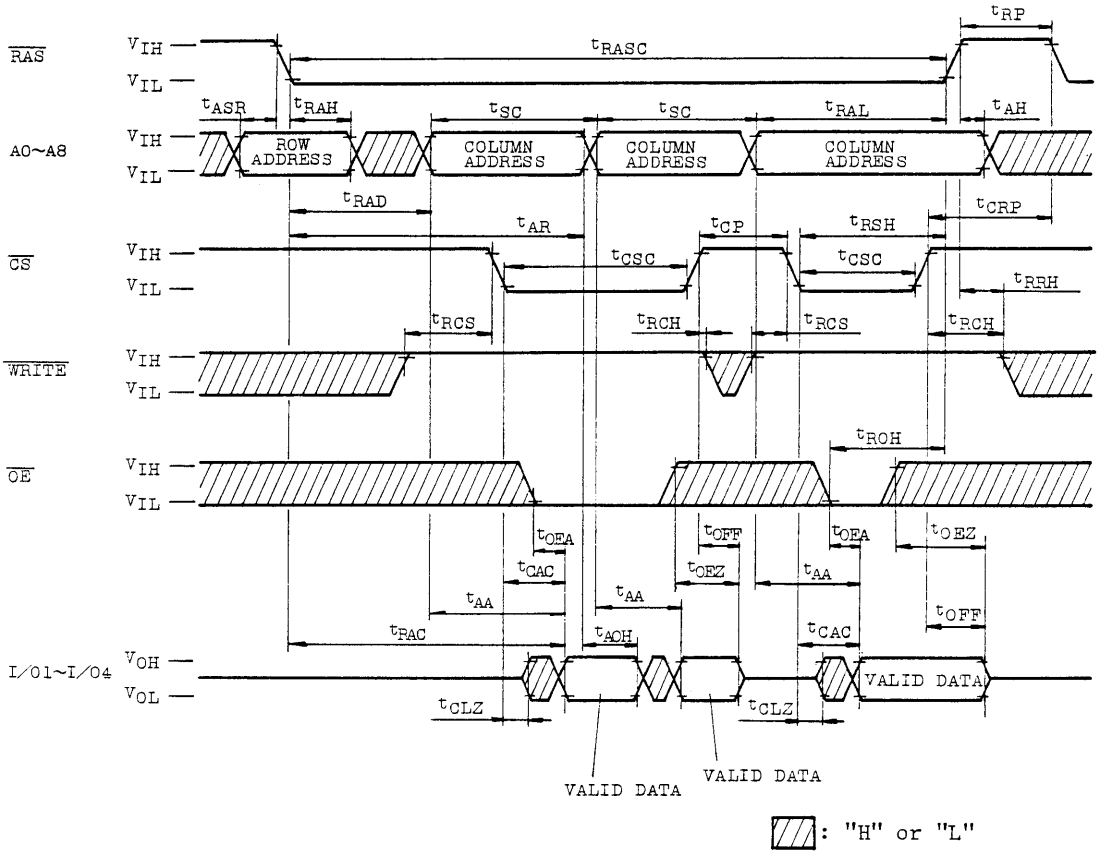
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



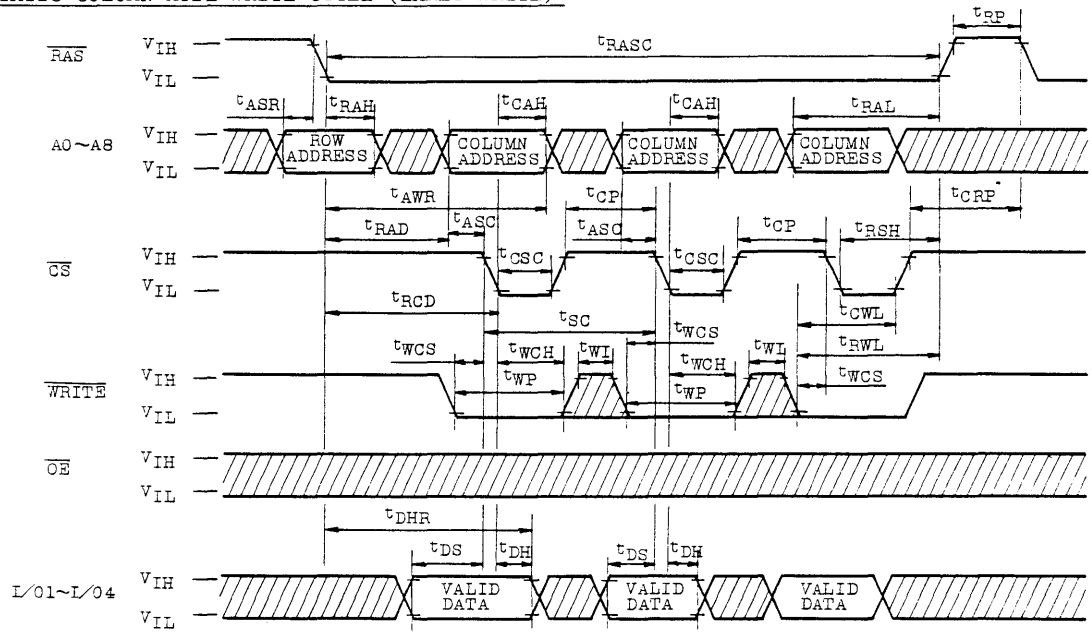
READ-MODIFY-WRITE CYCLE



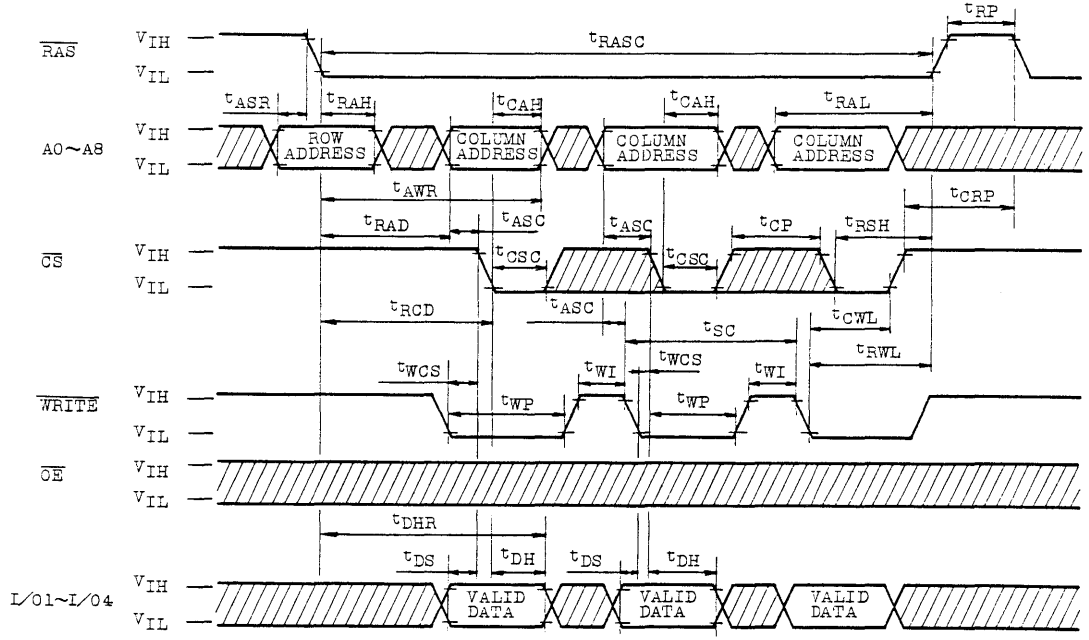
STATIC COLUMN MODE READ CYCLE



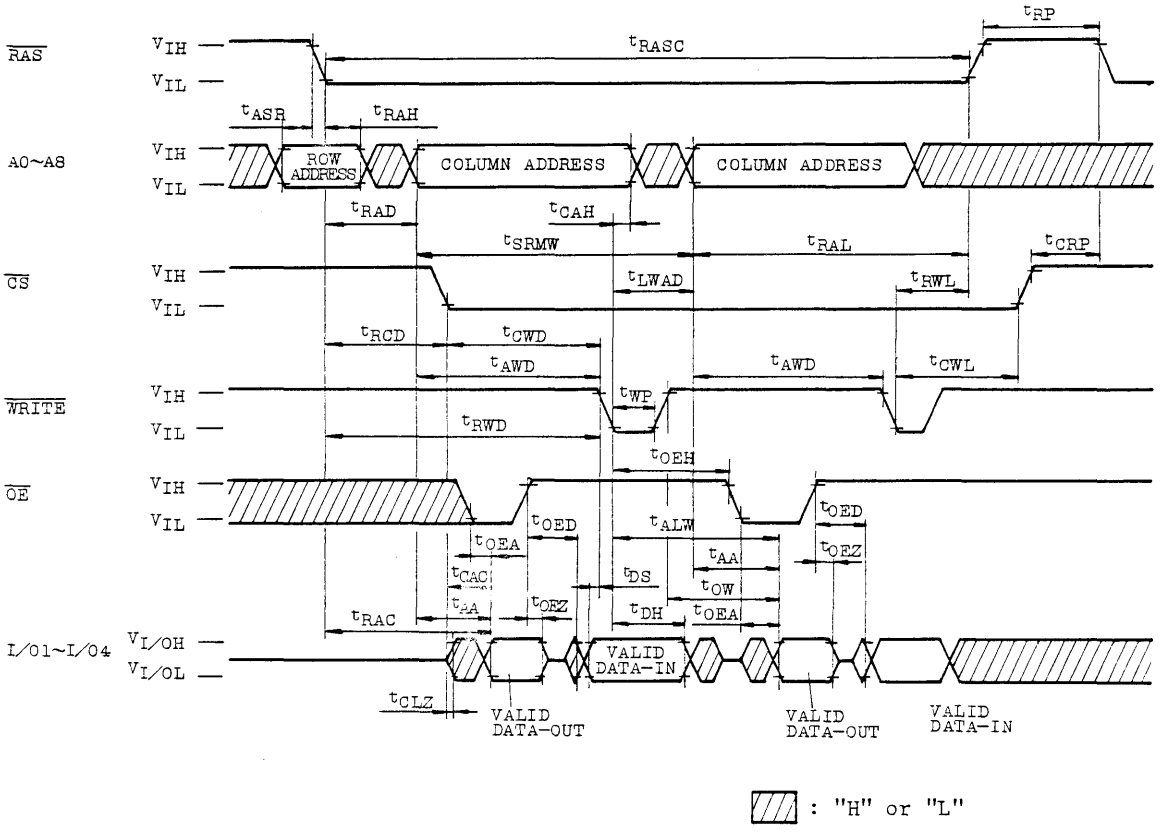
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

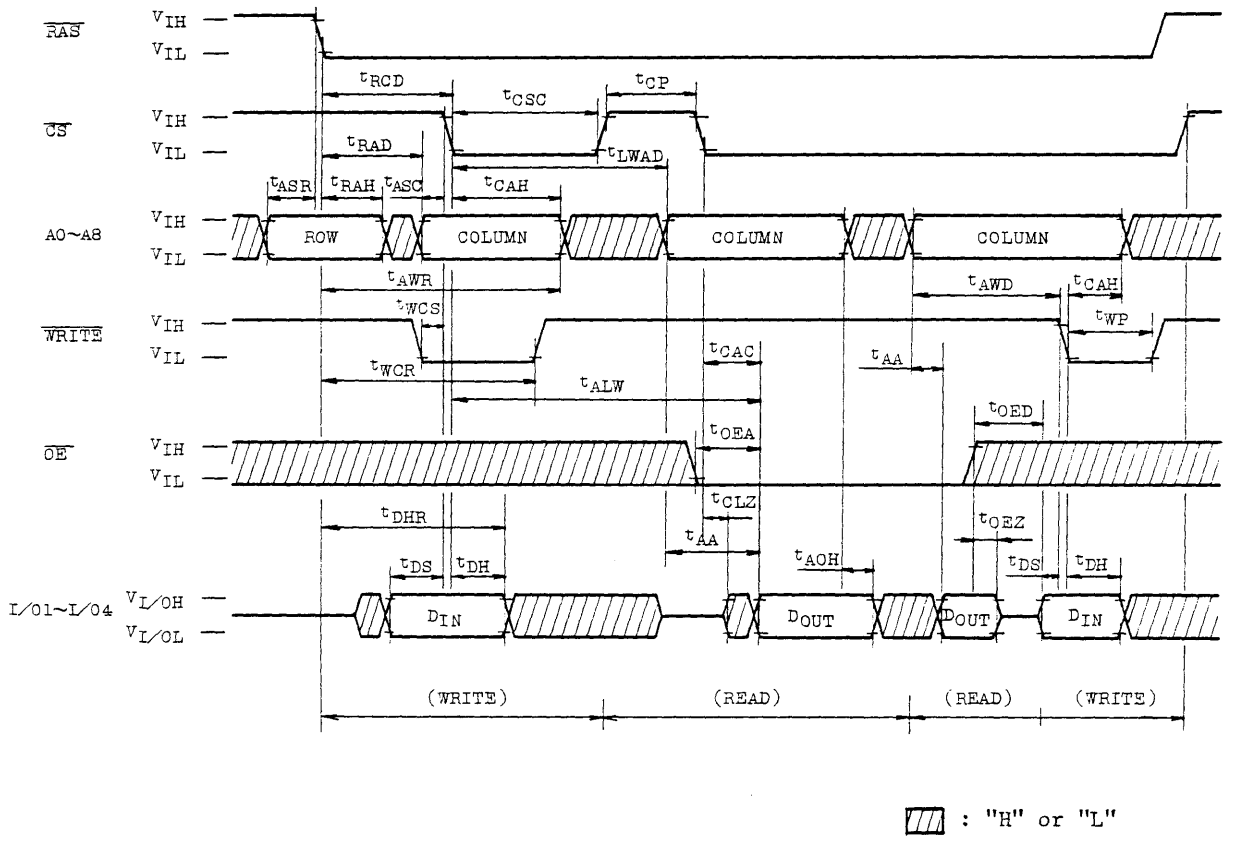


STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



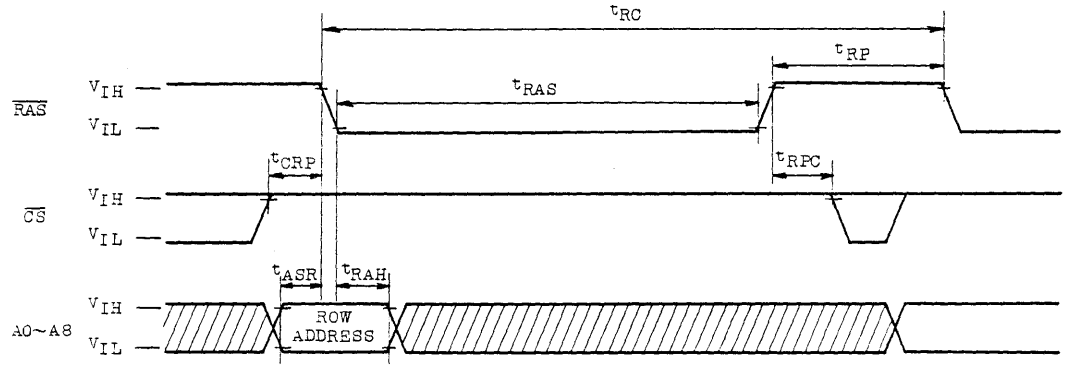
: "H" or "L"

STATIC COLUMN MODE READ/WRITE MIXED CYCLE



▨ : "H" or "L"

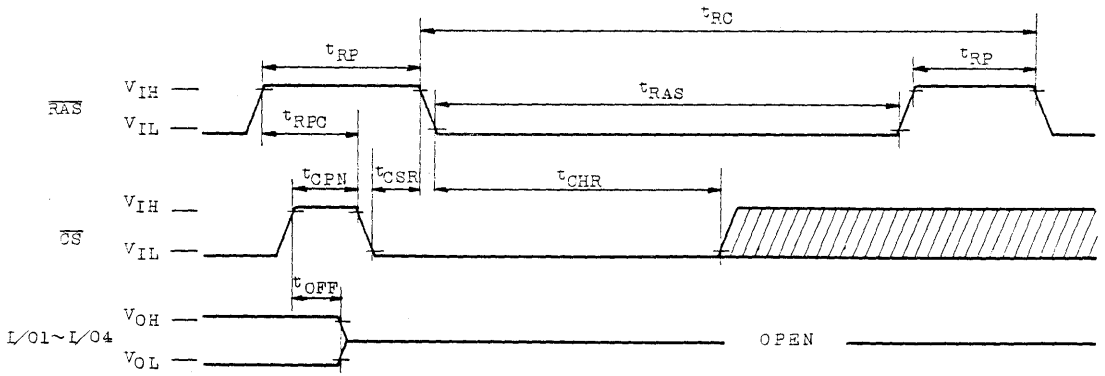
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$=Don't Care

▨ : "H" or "L"

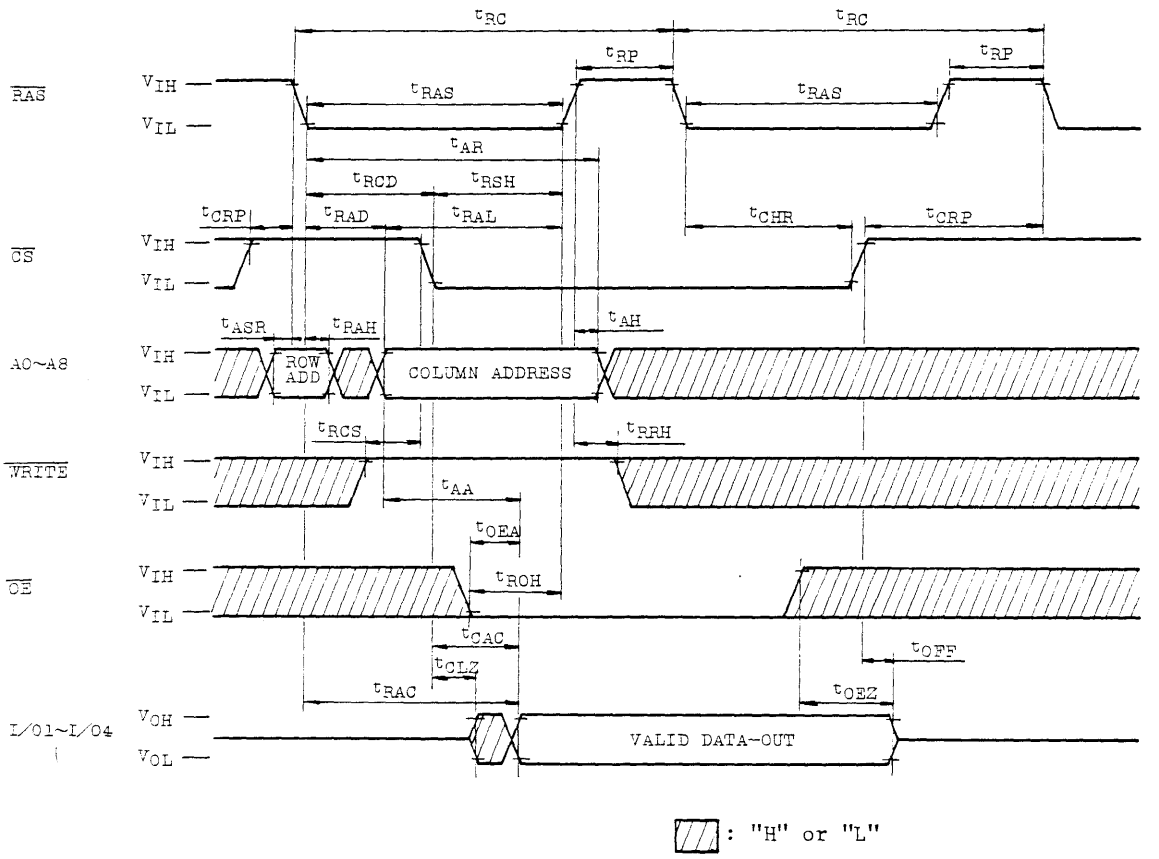
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



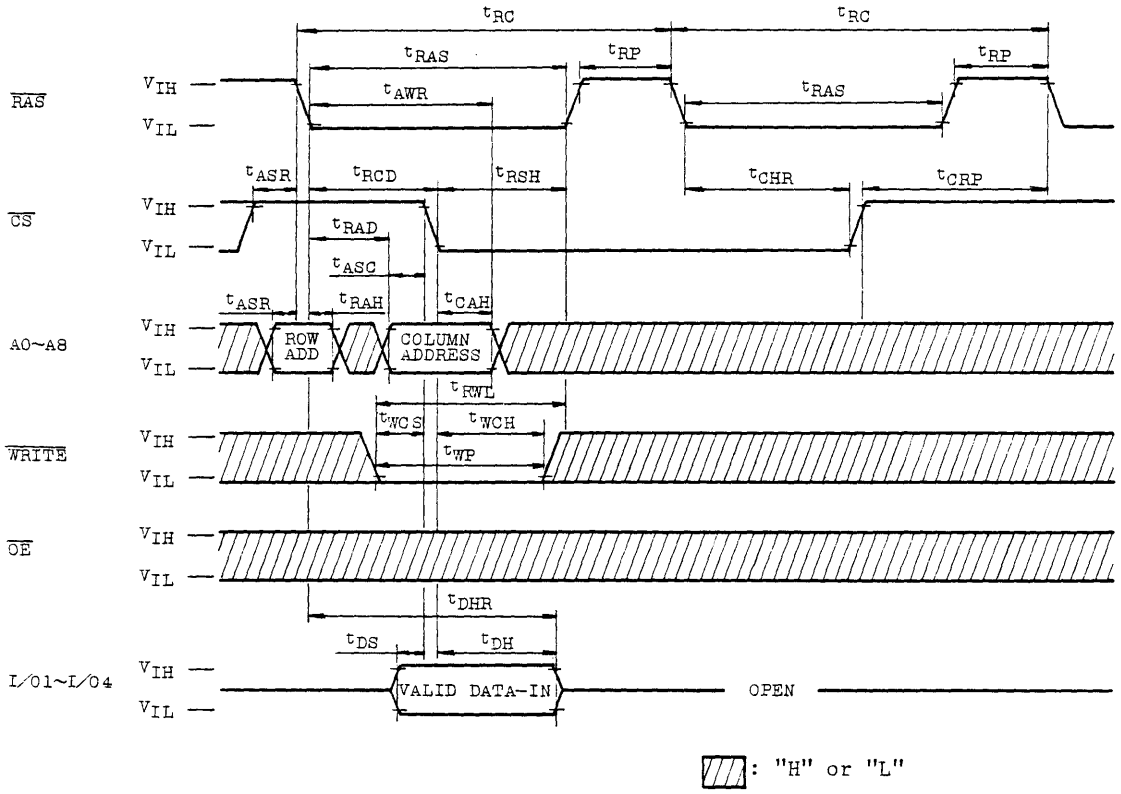
Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8="H" or "L"

▨ : "H" or "L"

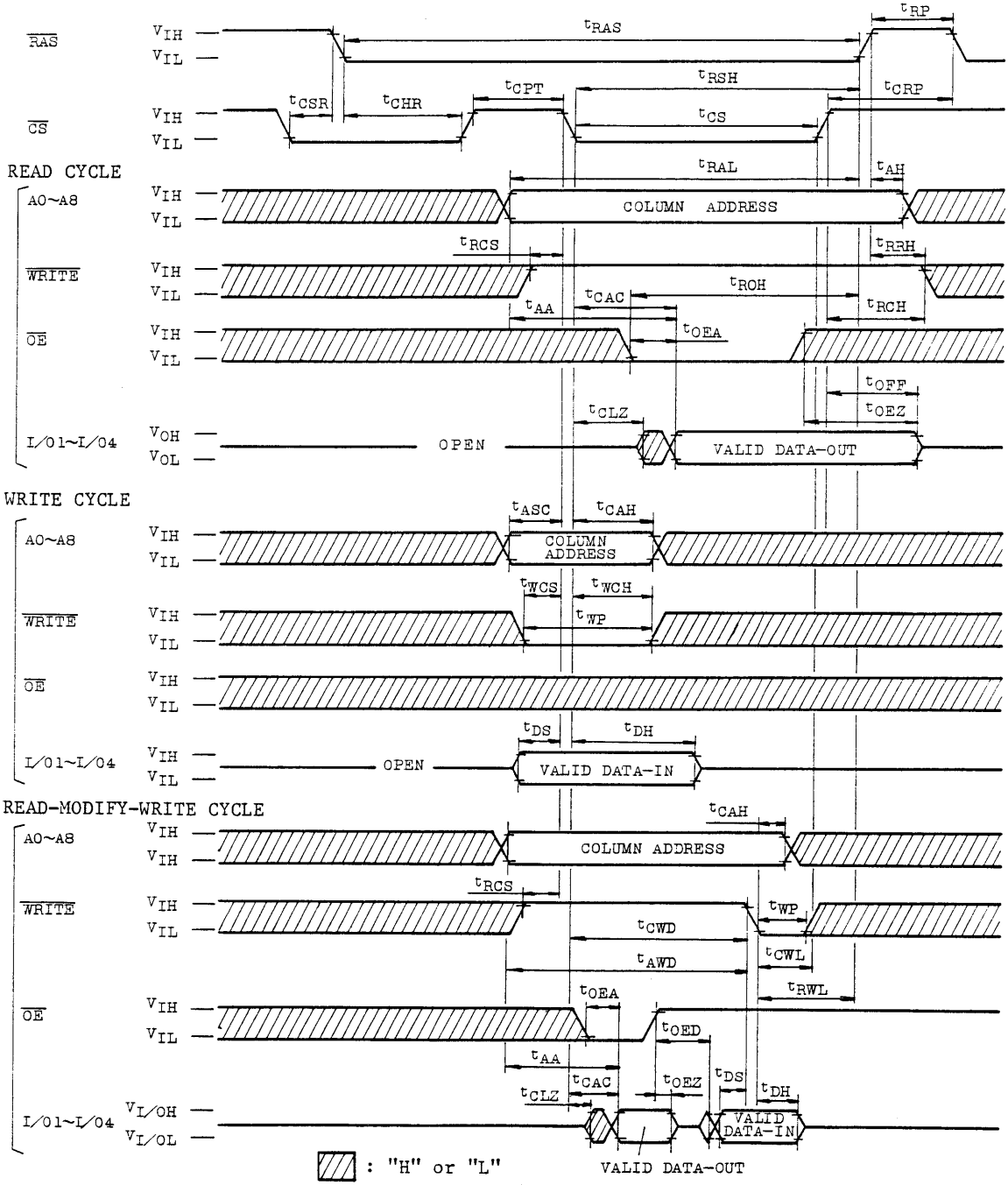
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



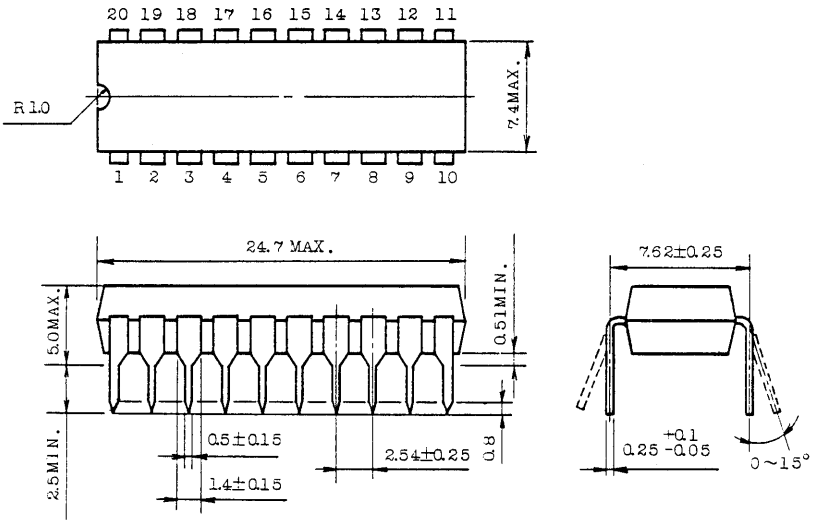
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

• Plastic DIP

Unit in mm



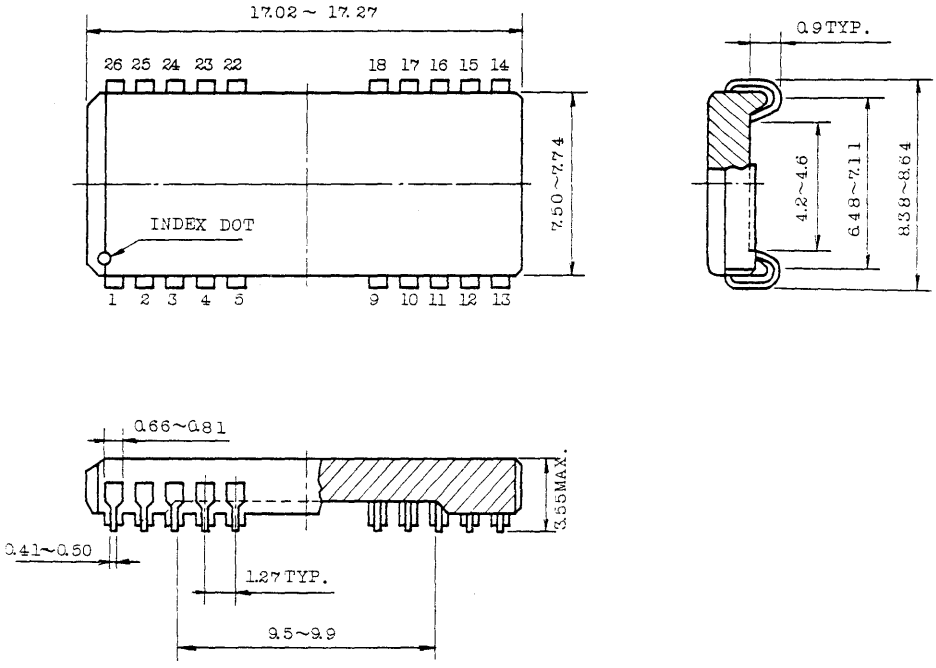
Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.

All dimensions are in millimeters.

• Plastic SOJ

Unit in mm

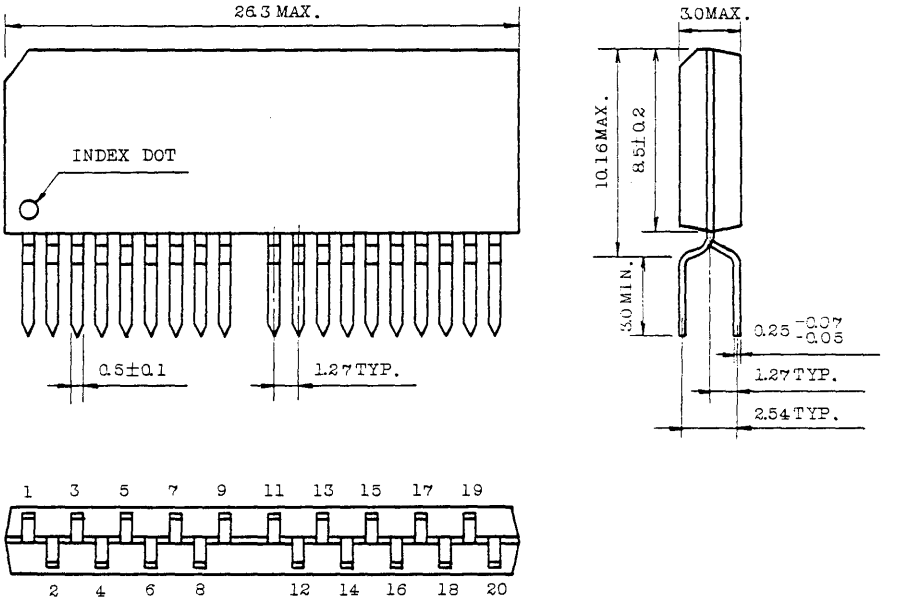


Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC514268AP/AJ/AZ-70, TC514268AP/AJ/AZ-80
TC514268AP/AJ/AZ-10

DESCRIPTION

The TC514268AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514268AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514268AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP and 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

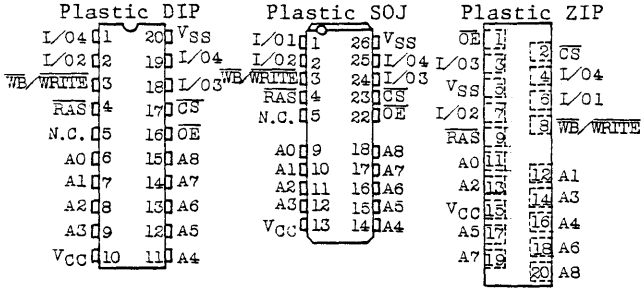
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514268AP/AJ/AZ -70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low power
  - 440mW MAX. Operating(TC514268AP/AJ/AZ-70)
  - 385mW MAX. Operating(TC514268AP/AJ/AZ-80)
  - 330mW MAX. Operating(TC514268AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh Write Per Bit, and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package Plastic DIP: TC514268AP
  Plastic SOJ: TC514268AJ
  Plastic ZIP: TC514268AZ

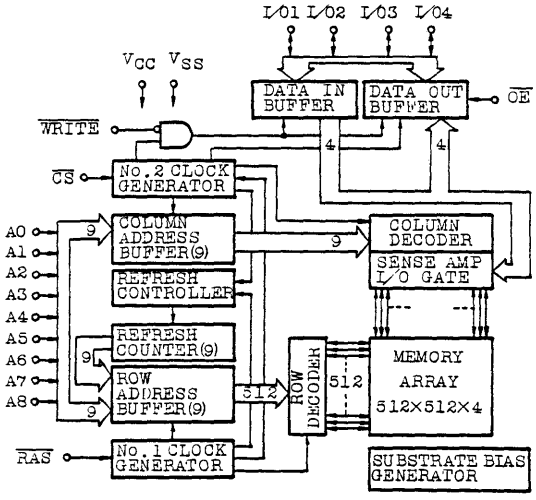
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WB}/\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1 ∿ I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 150	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	UNIT
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycleing: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3, 4
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	TC514268AP/AJ/AZ-70	-	60	mA	3, 4
		TC514268AP/AJ/AZ-80	-	50		
		TC514268AP/AJ/AZ-10	-	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	TC514268AP/AJ/AZ-70	-	80	mA	3
		TC514268AP/AJ/AZ-80	-	70		
		TC514268AP/AJ/AZ-10	-	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (DOUT is disable, 0V ≦ V_{OUT} ≦ 5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514258AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cyclt Time	100	-	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8, 13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8, 14
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	8, 15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	0	-	0	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	30	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	-	20	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width(Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	45	20	55	25	70	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	10	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514268AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	85	-	95	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10	-	10	-	10	-	ns	16
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	17
t_{AHLW}	Last Write to Column Address Hold Time	65	-	75	-	95	-	ns	
t_{RCS}	Read Command Set-up Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	-	15	-	20	-	ns	12
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	$\overline{WRITE}$ Pulse Width	15	-	15	-	20	-	ns	
t_{WI}	$\overline{WRITE}$ Inactive Time	10	-	10	-	10	-	ns	
t_{RWL}	$\overline{WRITE}$ Command to RAS Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	$\overline{WRITE}$ Command to CS Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	55	-	55	-	65	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	100	-	110	-	135	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	-	70	-	85	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	TC514268AP/AJ/AZ-70		TC514268AP/AJ/AZ-80		TC514268AP/AJ/AZ-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10	-	10	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	25	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	20	-	25	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	9
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	20	-	25	-	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	-	0	-	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	10	-	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	0	-	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	10	-	10	-	ns	

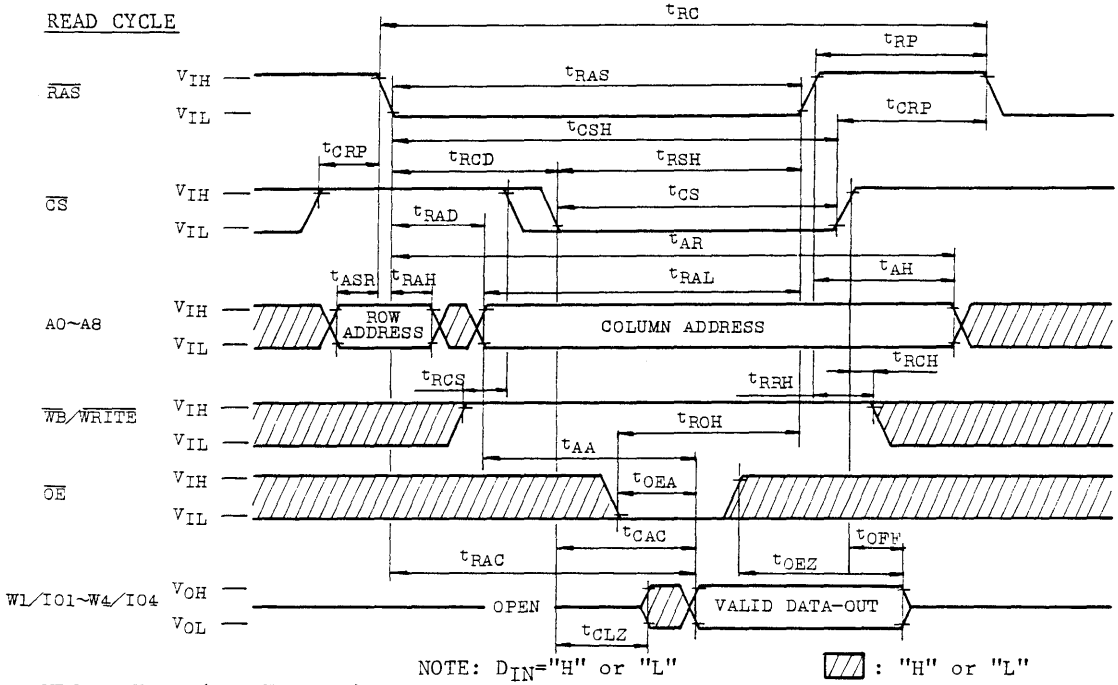
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	
C_O	Input/Output Capacitance (I/O1 ∿ I/O4)	-	7	

NOTES:

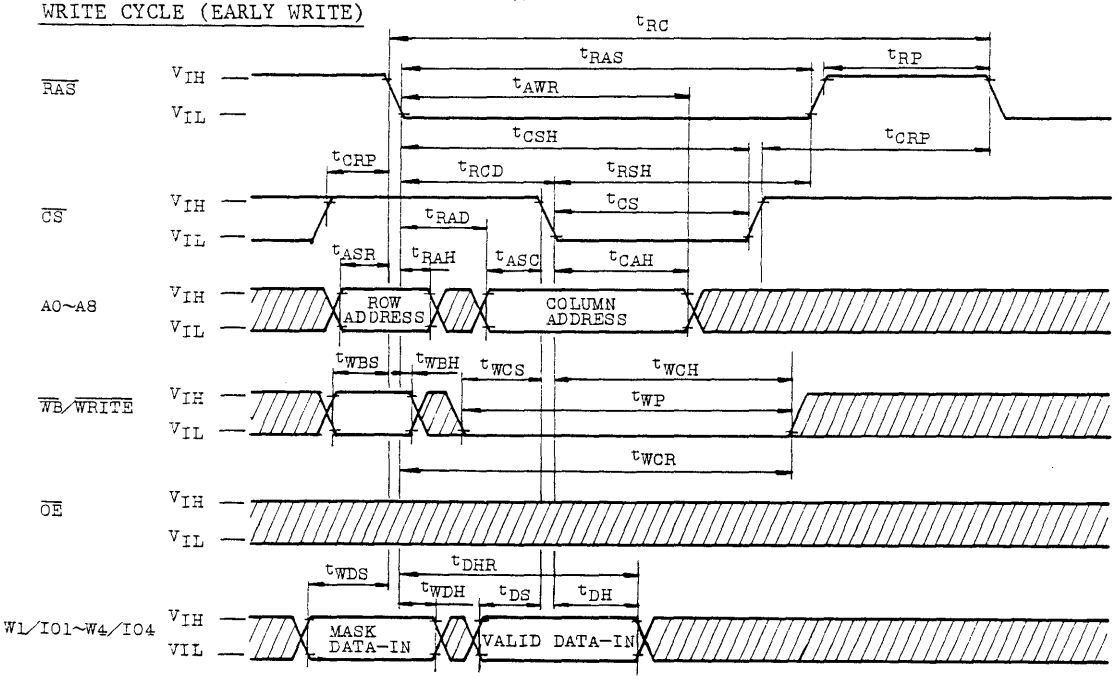
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
12. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

READ CYCLE



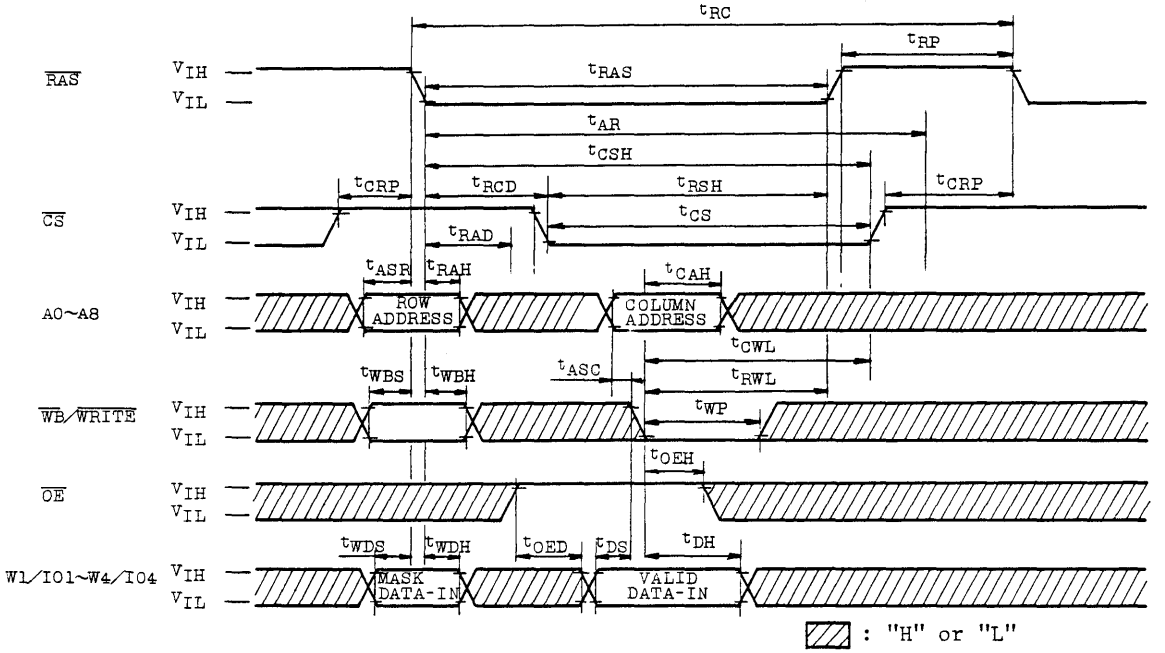
NOTE: D_{IN}="H" or "L" ▨ : "H" or "L"

WRITE CYCLE (EARLY WRITE)

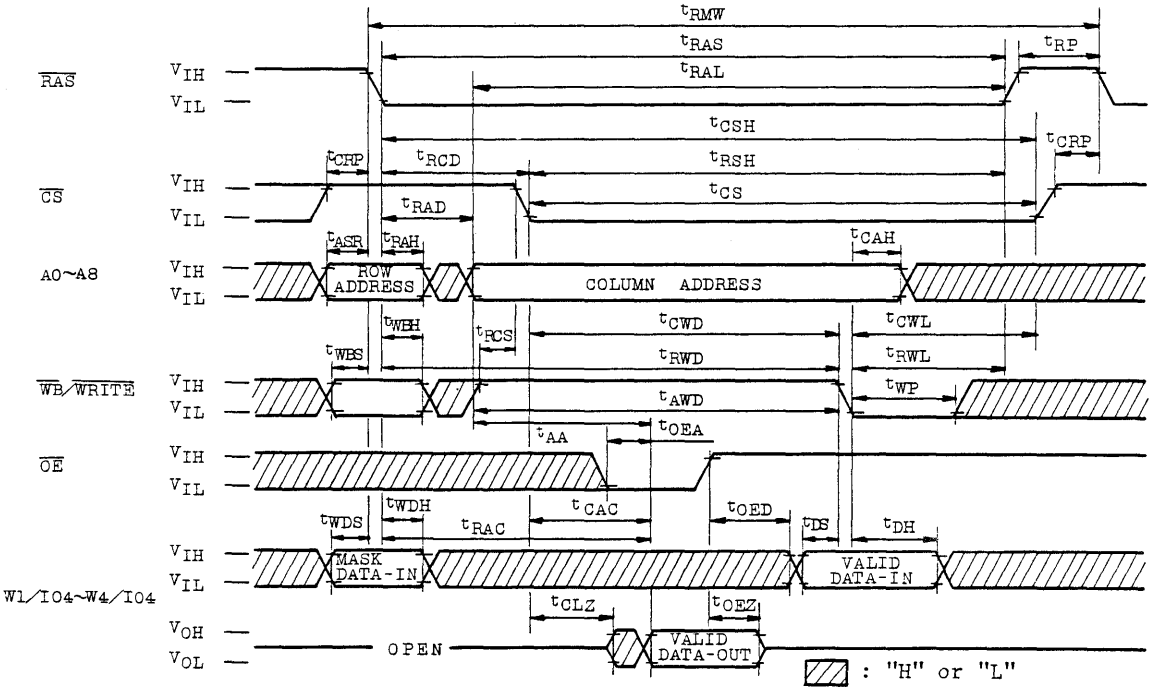


NOTE: D_{OUT}=OPEN ▨ : "H" or "L"

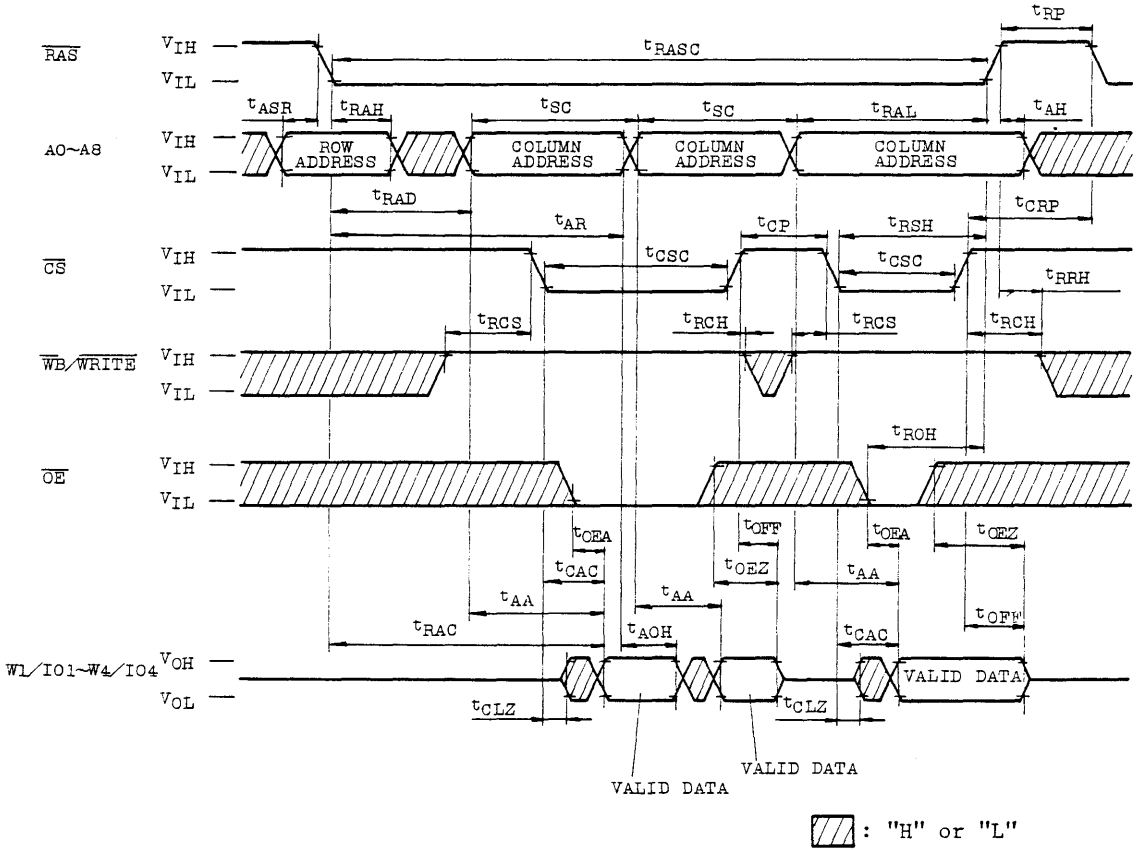
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE

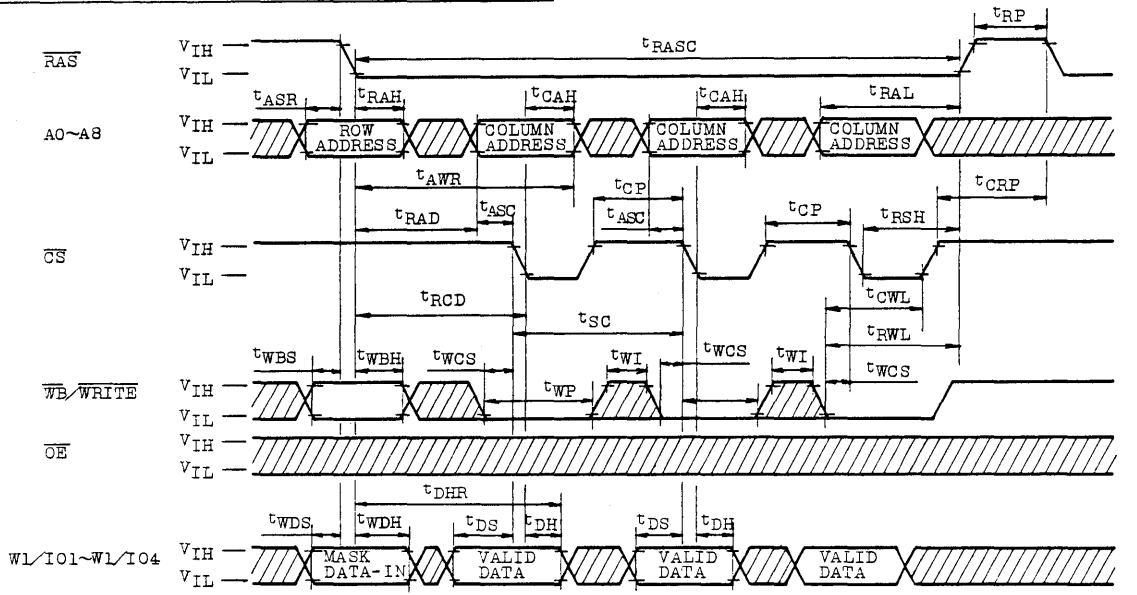


STATIC COLUMN MODE READ CYCLE

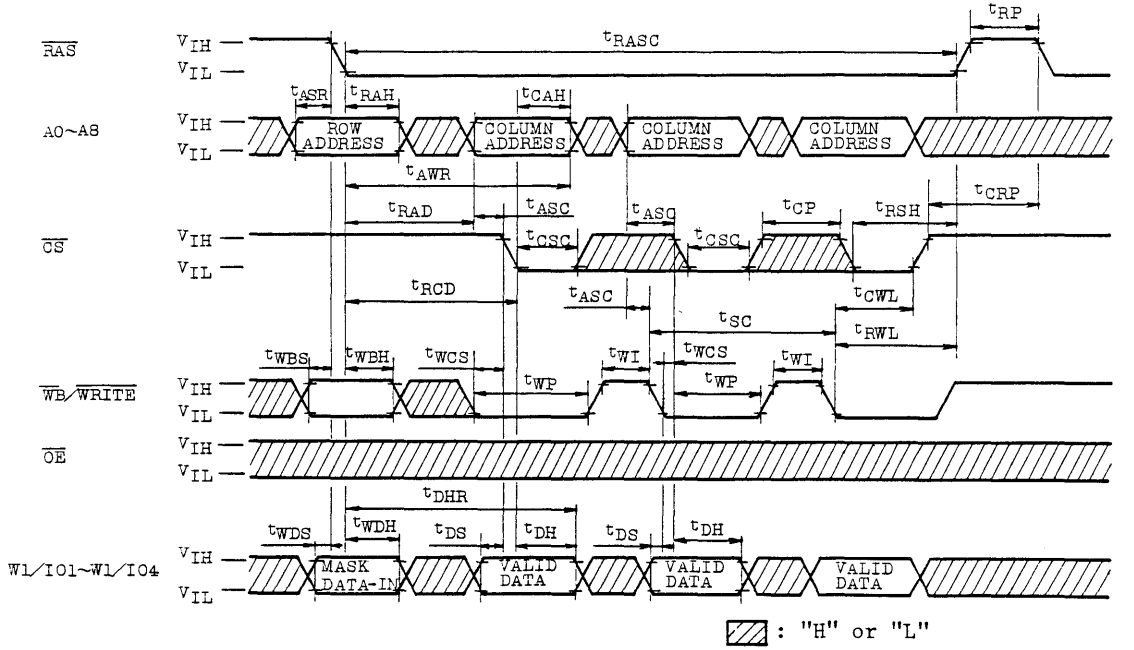


NOTE: D_{IN}="H" or "L"

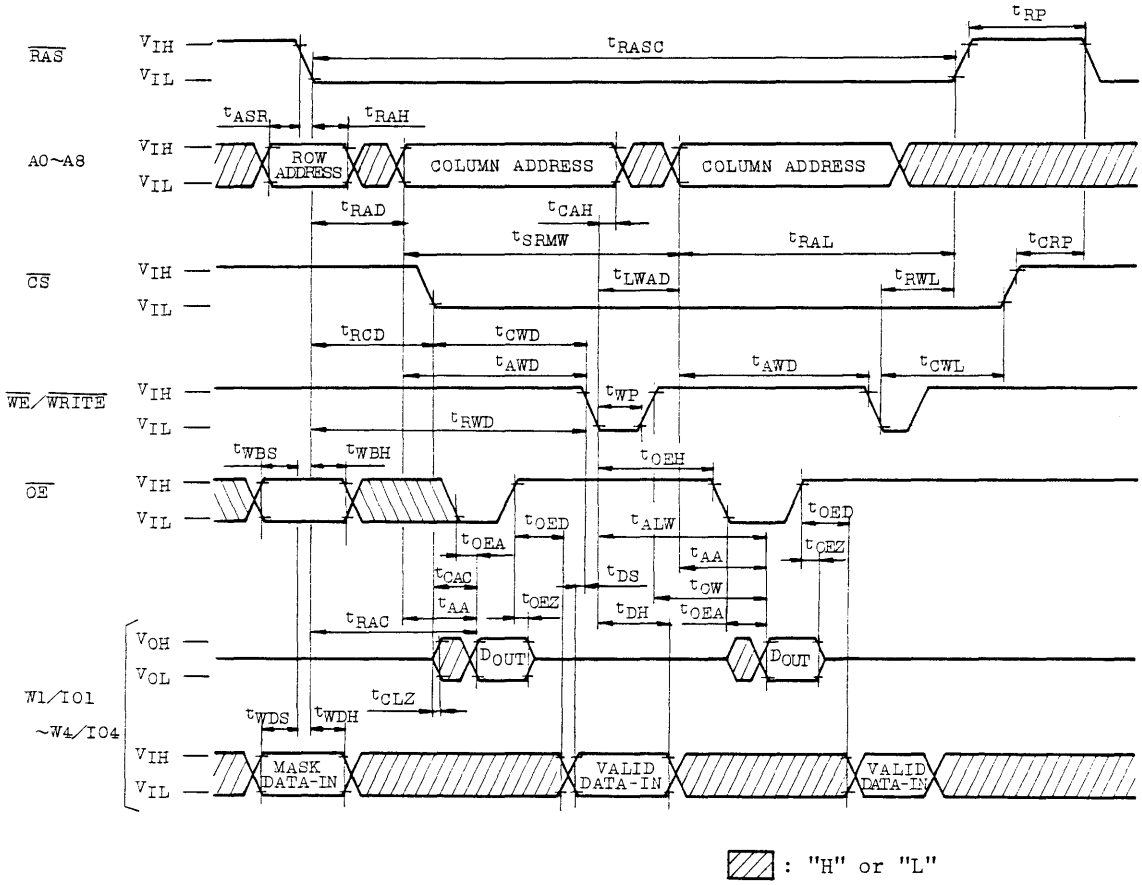
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



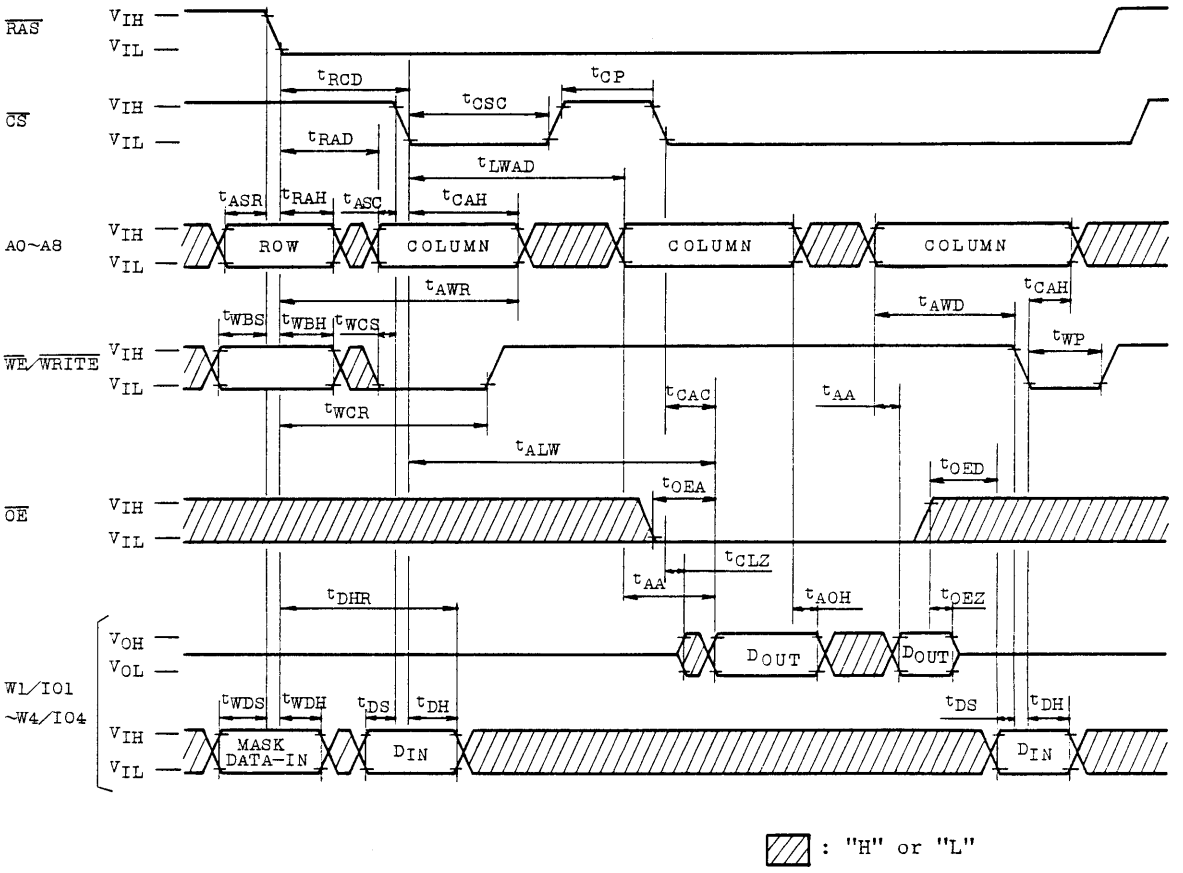
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

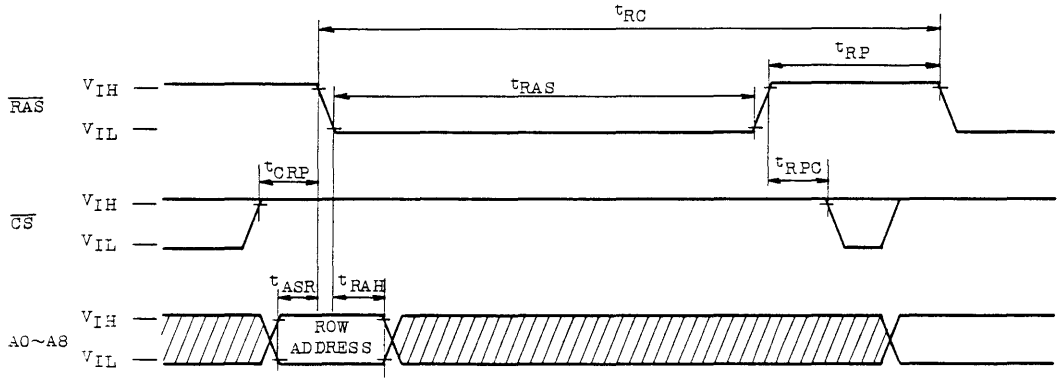


STATIC COLUMN MODE MIXED CYCLE



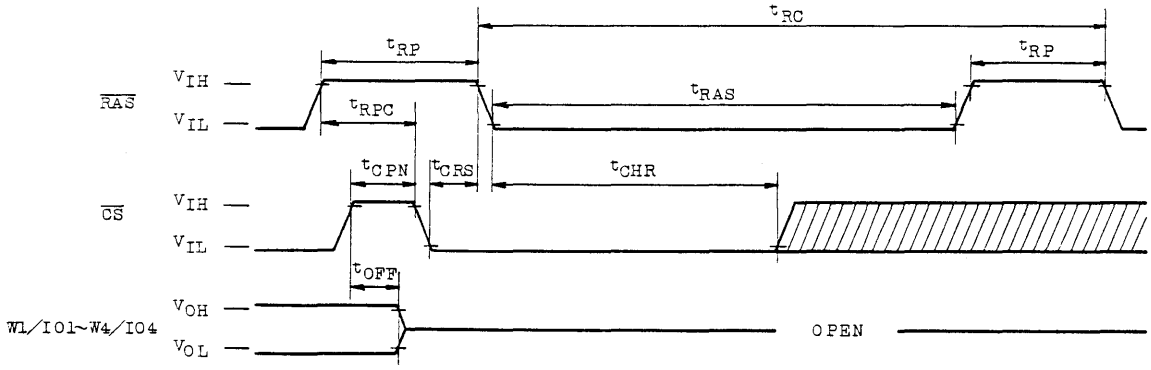
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



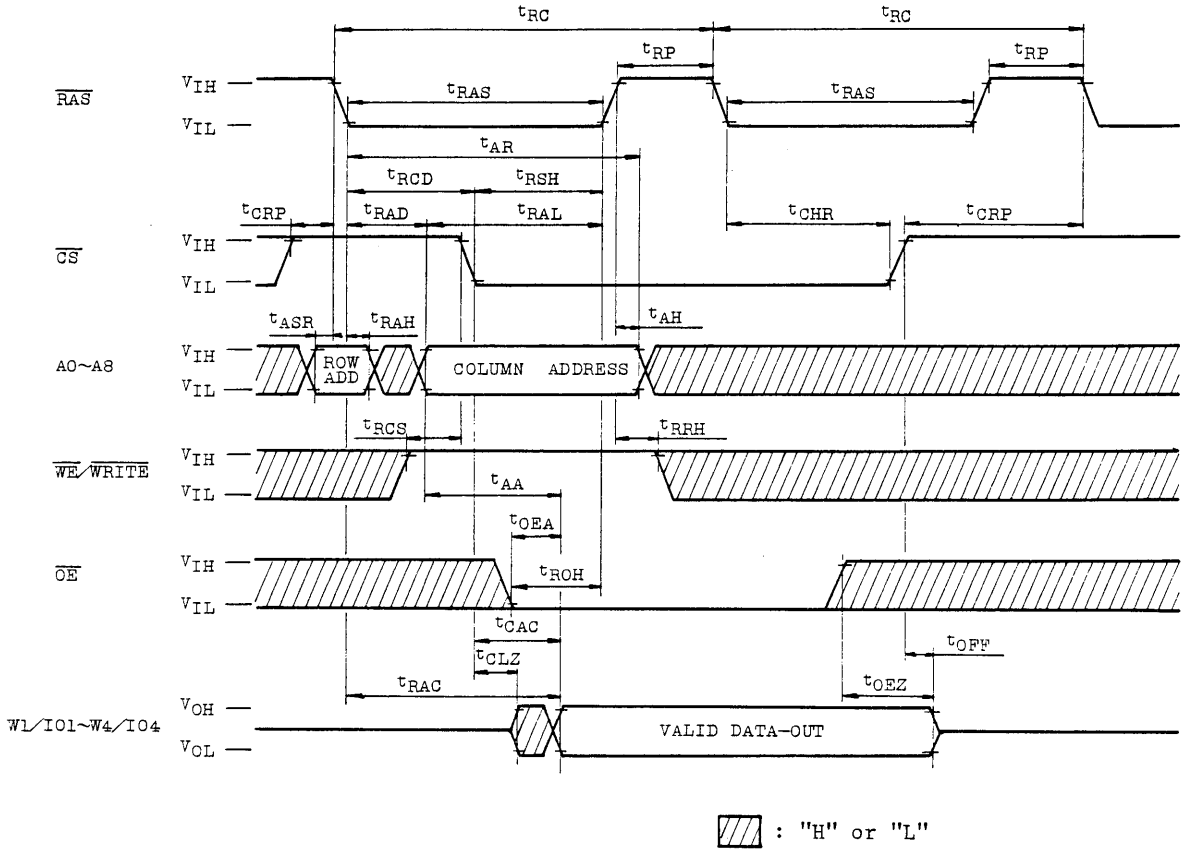
Note: $\overline{WB}/\overline{WRITE}$, $\overline{OE}$=Don't Care ▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

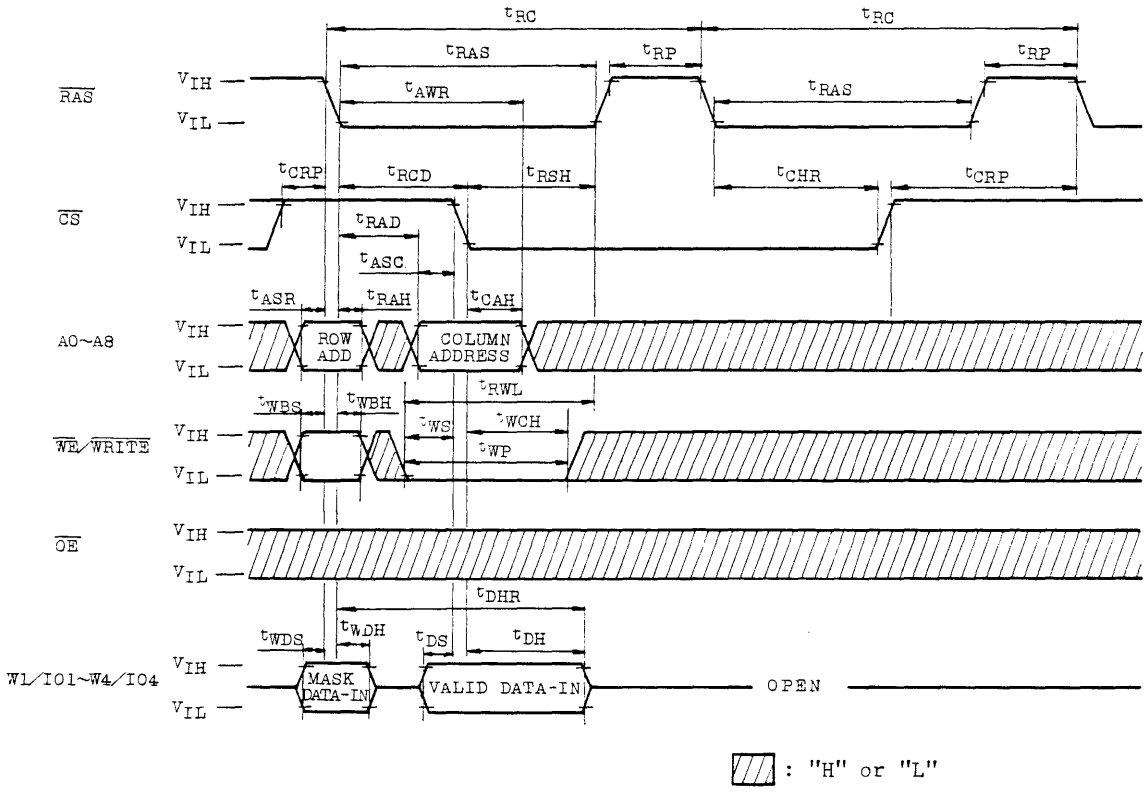


Note: $\overline{WB}/\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8="H" or "L" ▨: "H" or "L"

HIDDEN REFRESH CYCLE (READ)

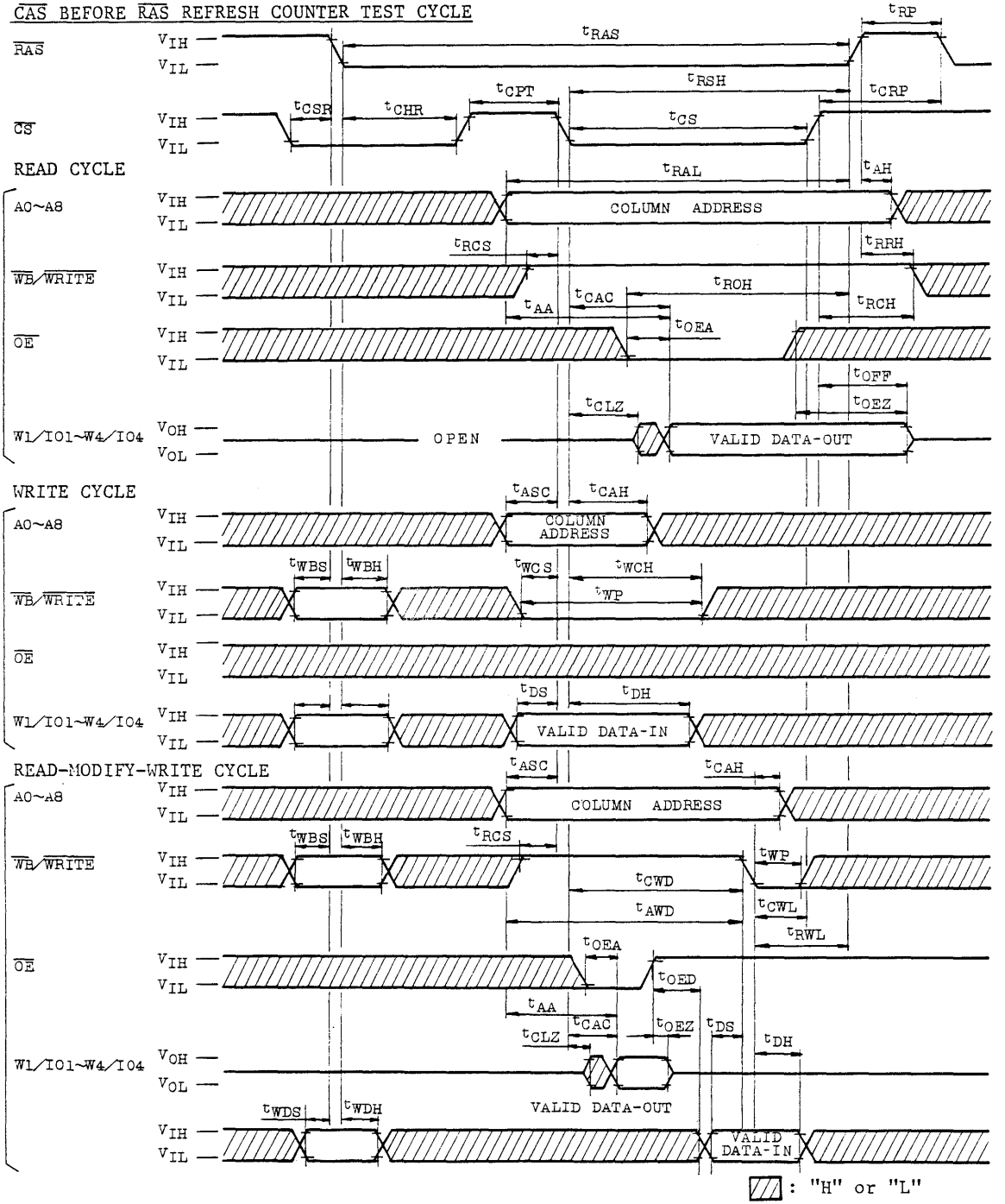


HIDDEN REFRESH CYCLE (WRITE)



NOTE: D_{OUT}=OPEN

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262,144 cell locations within the TC514268AP/AJ/AZ are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, in a read cycle column-address must be held stable until the access time. In a write cycle column-address are latched at the last falling of edge of $\overline{WRITE}$ or $\overline{CS}$.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CS}$" feature allows the $\overline{CS}$ clock to be externally activated as soon as the Row Address Hole Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

Write Cycle. A write cycle is performed by bringing ($\overline{WB}$/)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CS}$ operation. The falling edge of $\overline{CS}$ or ($\overline{WB}$/)$\overline{WE}$ strobes data on (Wi)IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi(/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.
For those data bits of Wi(/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip if $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

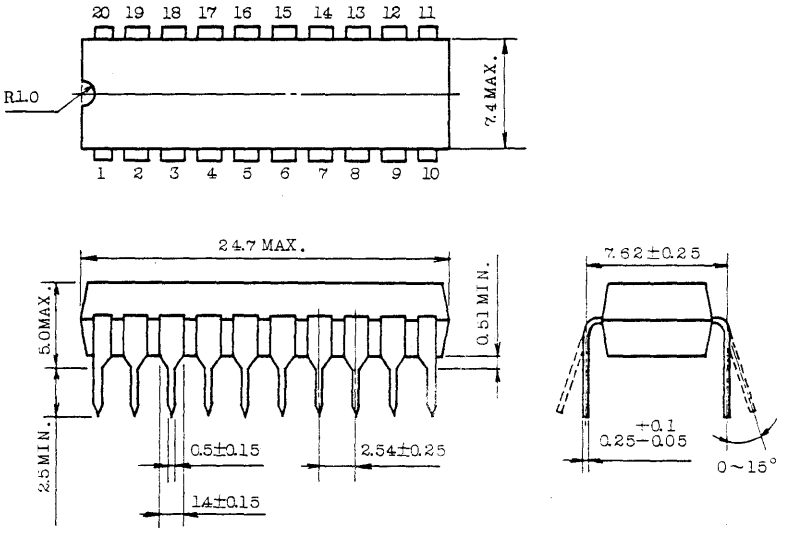
The outputs become valid after the access time has elapsed and remains valid while $\overline{CS}$ and $\overline{OE}$ are low. $\overline{CS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CS}$ returning high forces the outputs into the high impedance state.

OUTLINE DRAWINGS

• Plastic DIP

Unit in mm



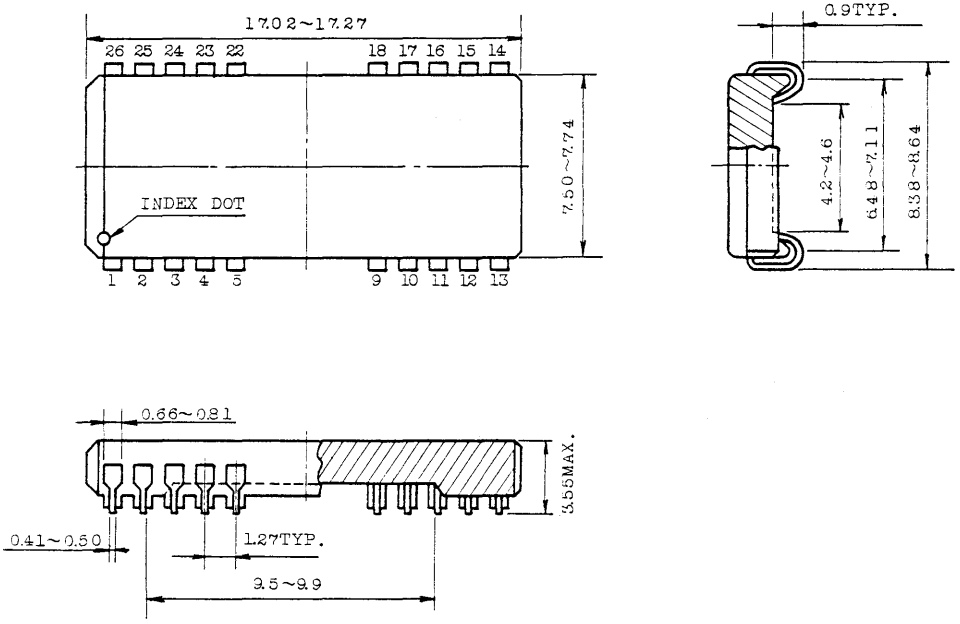
Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.20 leads.

All dimensions are in millimeters.

• Plastic SOJ

Unit in mm



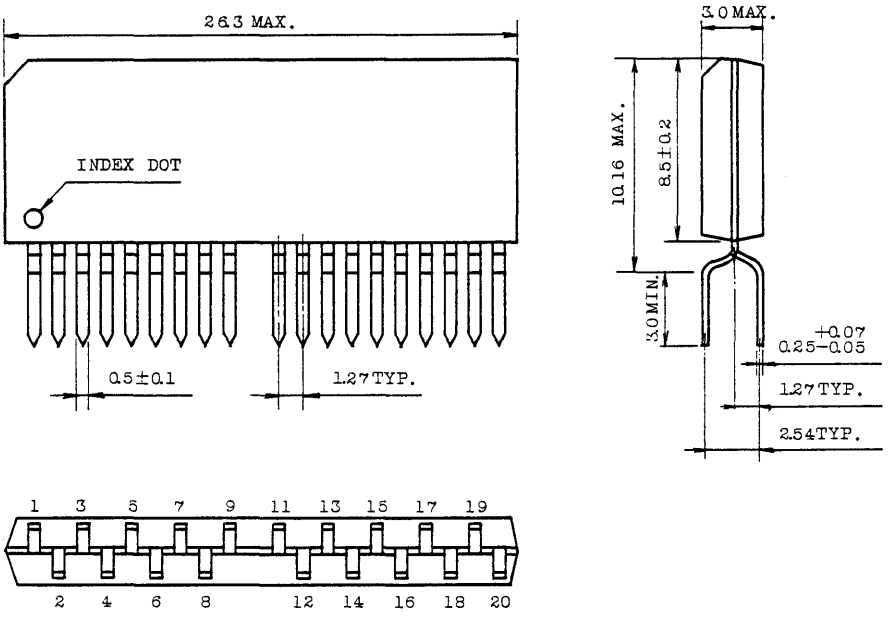
Note: Each lead pitch 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility ofr use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.

Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

Video RAM

TOSHIBA MOS MEMORY PRODUCTS

1MBit (256K×4) Field Memory
SILICON GATE CMOS

TC521000P

PRELIMINARY

DESCRIPTION

The TC521000P is a CMOS 1Mbit Field Memory organized as 256K word by 4 bits, and features separate inputs/outputs equipped with each 8 bit serial shift register (32K words x 8 bit shift register x 4 bits), and also features a high speed operation with a clock rate of 33MHz (serial cycle time: 30ns). The TC521000P is a high speed serial read/write memory with a random access capability per 8 words, and is suitable for use in field/frame memory in digital TV, VCR and other video application systems which requires the improvement in picture quality and enhancement of performance.

The TC521000P is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margins.

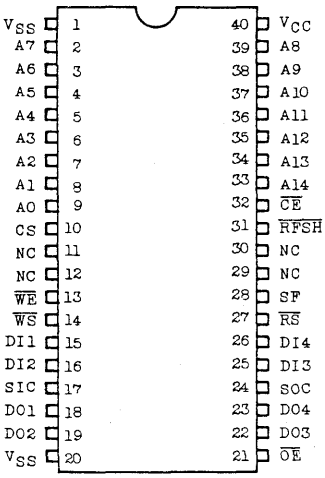
FEATURES

- High speed and low power

Serial Access Time		20ns
Serial Read Cycle Time		30ns
Serial Write Cycle Time		30ns
Read, Write Cycle Time		190ns
Read-Modify-Write Cycle Time		240ns
Read-Read-Write Cycle Time		480ns
Power Dissipation	Operating Power	550mW
	Standby Power	110mW

- Organization: 32K word x 8 bit shift register 4 bit
- Single 5V power supply: 5V ± 10%
- On-chip 8 bit shift registers
- Separate inputs and outputs
- Serial read/write, Read/Write, Read/Modify-Write, High Speed Read-Read-Write capability
- Random Access Capability per 8 word
- 512/8 ms refresh cycles
- On-chip refresh counter
- All inputs and outputs: TTL compatible
- Package: 40 pin 600 mils wide standard plastic DIP

PIN CONNECTION

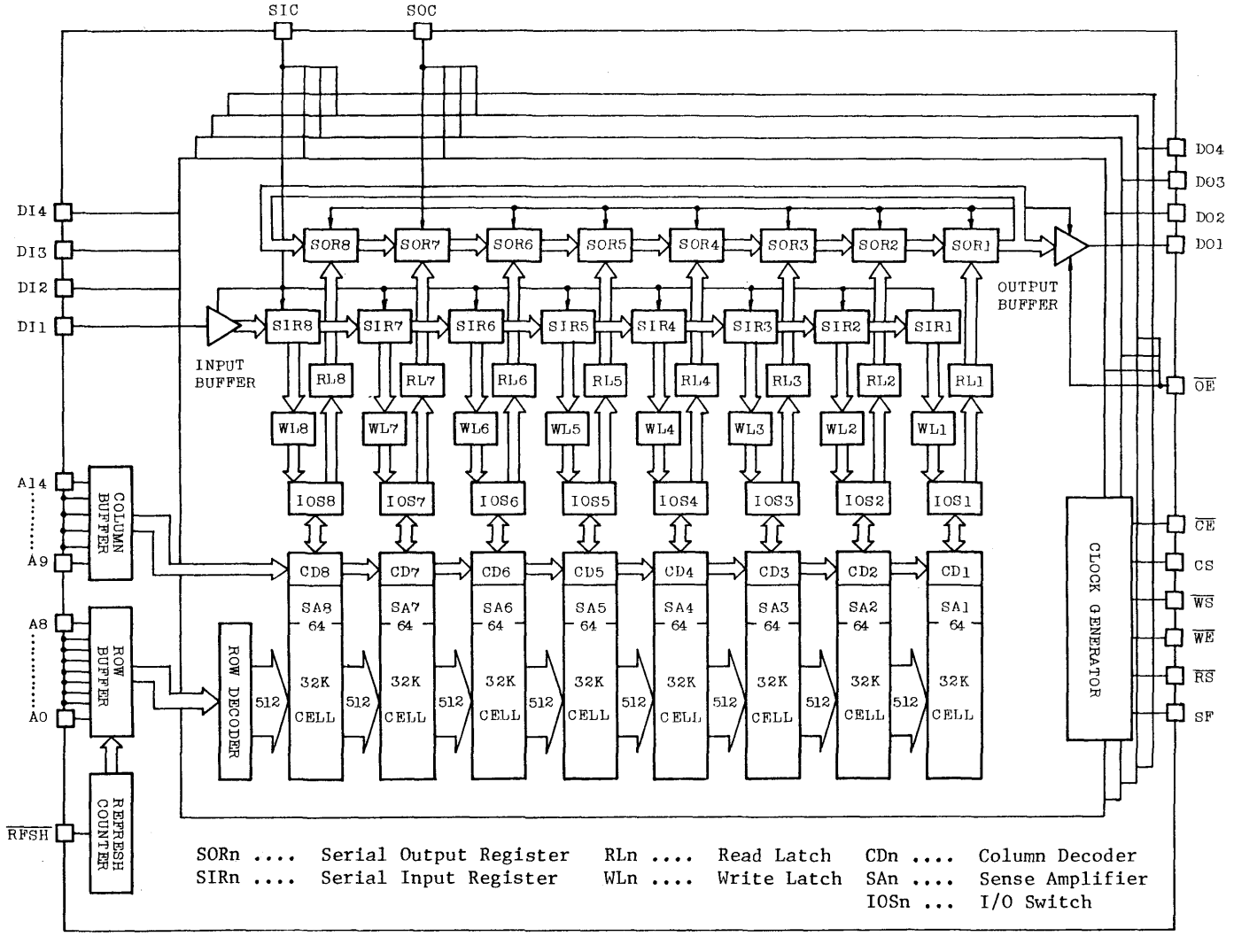


40PIN 600MILS PLASTIC DIP

PIN NAMES

SYMBOL	NAME
A0 ~ A14	Address Input
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{WS}$	Write Strobe Input
$\overline{RS}$	Read Strobe Input
CS	Chip Select Input
SIC	Serial Input Clock Input
SOC	Serial Output Clock Input
DI1 ~ DI4	Data Input
DO1 ~ DO4	Data Output
$\overline{RFSH}$	Refresh Control Input
SF	Special Function Input
V_{CC}	Power (5V)
V_{SS}	Ground (0V)
NC	Non Connection

BLCOK DIAGRAM



PIN NAMES AND FUNCTIONS

SYMBOL	NAME	FUNCTION
A0 ∿ A8	Row Address Inputs	Row Addresses
A9 ∿ A14	Column Address Inputs	Column Addresses The A14 is a column LSB address and is controlled internally by SF signal.
$\overline{CE}$	Chip Enable Input	The falling edge of $\overline{CE}$ latches the A0 ∿ A14 and CS. The read data is retained in Read Latch (RL), even if the $\overline{CE}$ goes high.
CS	Chip Select Input	The low CS forbid the memory cell access operation, but allows the refresh operation. ($\overline{CE}$ ONLY REFRESH)
$\overline{RS}$	Read Strobe Input	The $\overline{RS}$ controls the transfer operation to Output Shift Register from Read Latch (RL).
SF	Special Function	The SF controls the column LSB A14 internally.
$\overline{WS}$	Write Strobe Input	The $\overline{WS}$ controls the transfer operation to Write Latch (WL) from Input Shift Register.
$\overline{WE}$	Write Enable Input	The $\overline{WE}$ controls the write operation into the memory cell.
$\overline{OE}$	Output Enable Input	The $\overline{OE}$ enables the DO1 ∿ DO4 output buffers.
$\overline{RFSH}$	Refresh Control Input	The $\overline{RFSH}$ controls the auto refresh operation.
SOC	Serial Output Clock Input	The SOC is a shift clock input to Output Shift Register.
SIC	Serial Input Clock Input	The SIC is a shift clock input to Input Shift Register.
DO1 ∿ DO4	Data Outputs	Serial Output Terminals.
DI1 ∿ DI4	Data Inputs	Serial Input Terminals.

ABSOLUTE MAXIMUM RATINGS (Note: 1)

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}•V_{OUT}	Input • Output Voltage	-1 ∿ 7	V	2
V_{CC}	Power Supply Voltage	-1 ∿ 7	V	2
T_{opr}	Operating Temperature	0 ∿ 70	°C	
T_{stg}	Storage Temperature	-55 ∿ 150	°C	
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec	
P_D	Power Dissipation	1	W	
I_{OUT}	Short Circuit Output Current	50	mA	

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	(10) TYP.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT ($\overline{CE}$, SIC, SOC Cycling: t_C, t_{SIC}, t_{SOC}=min.)	-	65	100	mA	3, 4
I_{CC2}	STANDBY CURRENT ($\overline{CE}$=$\overline{OE}$=V_{IH}, SIC=SOC=V_{IL})	-	3	20	mA	
I_{CC3}	REFRESH CURRENT ($\overline{RFSH}$ Cycling: t_{FC}=t_{FC} min.)	-	50	100	mA	3
$I_{I1(L)}$	INPUT LEAKAGE CURRENT (Except for SF Pin) (0V ≤ V_{IN} ≤ 6.5V, All other pins not under test=0V)	-10	-	10	µA	
$I_{I2(L)}$	INPUT LEAKAGE CURRENT (SF Pin ONLY) (0V ≤ V_{IN} ≤ 6.5V, All other pins not under test=0V)	-50	-	50	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (0V ≤ V_{OUT} ≤ V_{CC}, Output is disabled)	-10	-	10	µA	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE (I_{OUT}=-5mA)	2.4	-	-	V	
V_{OL}	OUTPUT LOW LEVEL VOLTAGE (I_{OUT}=4.2mA)	-	-	0.4	V	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
C_{I1}	Input Capacitance (A0 ∿ A14)	-	7	pF	
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{CS}$, $\overline{RS}$, $\overline{WS}$, $\overline{WE}$, $\overline{OE}$, SF, $\overline{RFSH}$, SIC, SOC)	-	7	pF	
C_{I3}	Input Capacitance (DI1 ∿ DI4)	-	7	pF	
C_O	Output Capacitance (DO1 ∿ DO4)	-	9	pF	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Note: 5, 6, 7)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_C	Read, Write Cycle Time	190		ns	
t_{RMW}	Read-Modify-Write Cycle Time (=8x t_{SOC}, t_{SIC})	240		ns	
t_{RRW}	Read-Read-Write Cycle Time (=16x t_{SOC})	480		ns	
t_{CE}	$\overline{CE}$ Pulse Width	100	2,000	ns	
t_P	$\overline{CE}$ Precharge Time	80		ns	
t_{ASC}	Address, CS Set-up Time	0		ns	
t_{AHC}	Address, CS Hold Time	50		ns	
t_{SOC}	Serial Output Cycle Time	30		ns	
t_{SO}	SOC Low Pulse Width	10		ns	
t_{SOP}	SOC High Pulse Width	10		ns	
t_{SOA}	SOC Access Time		20	ns	8
t_{SOH}	SOC Output Data Hold Time	5		ns	
t_{SIC}	Serial Input Cycle Time	30		ns	
t_{SI}	SIC Low Pulse Width	10		ns	
t_{SIP}	SIC High Pulse Width	10		ns	
t_{RCS}	Read Command Set-up Time	0		ns	
t_{RCH}	Read Command Hold Time	0		ns	
t_{CRD}	$\overline{CE}$-$\overline{RS}$ Delay Time	85		ns	
t_{RS}	$\overline{RS}$ Pulse Width	20		ns	
t_{RCP}	$\overline{RS}$-$\overline{CE}$ Precharge Time	0		ns	
t_{RSP}	$\overline{RS}$ Precharge Time	30		ns	
t_{SOS}	SOC-$\overline{RS}$ Set-up Time	0		ns	
t_{SOV}	SOC-$\overline{RS}$ Hold Time	15		ns	
t_{RSL}	SIC-$\overline{RS}$ Lead Time	0		ns	
t_{OE}	$\overline{OE}$ Pulse Width	30		ns	
t_{OEP}	$\overline{OE}$ Precharge Time	30		ns	
t_{OEA}	$\overline{OE}$ Access Time		25	ns	8
t_{OEZ}	$\overline{OE}$ Output Buffer Turn-off Delay Time	0	30	ns	9
t_{RWD}	$\overline{RS}$-$\overline{WE}$ Delay Time	0		ns	
t_{CWD}	$\overline{CE}$-$\overline{WE}$ Delay Time (Read-Modify-Write Cycle)	90		ns	
t_{WHC}	$\overline{WE}$ Hold Time	70		ns	
t_{WP}	$\overline{WE}$ Pulse Width	30		ns	
t_{CWL}	$\overline{WE}$-$\overline{CE}$ Lead Time	40		ns	

(Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	NOTES
t_{SWE}	$\overline{WS}$-$\overline{WE}$ Set-up Time	20		ns	
t_{WS}	$\overline{WS}$ Pulse Width	20		ns	
t_{WSP}	$\overline{WS}$ Precharge Time	30		ns	
t_{WIH}	$\overline{WS}$ Inhibit Time referenced to $\overline{WE}$	50		ns	
t_{WIHC}	$\overline{WS}$ Inhibit Time referenced to $\overline{CE}$	100		ns	
t_{SIV}	SIC-$\overline{WS}$ Set-up Time	5		ns	
t_{SIH}	SIC-$\overline{WS}$ Hold Time	10		ns	
t_{DS}	Data Input Set-up Time	5		ns	
t_{DH}	Data Input Hold Time	5		ns	
t_{SFS}	SF-$\overline{CE}$ Set-up Time	0		ns	
t_{SFH}	SF-$\overline{CE}$ Hold Time	0		ns	
t_{CSL}	SF-$\overline{CE}$ Lead Time (Read-Read-Write Cycle)	50		ns	
t_{SSH}	SOC-SF Hold Time (Read-Read-Write Cycle)	20		ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	7
t_{REF}	Refresh Period		8	ms	
t_{FC}	Refresh Cycle Time	190		ns	
t_{CFD}	$\overline{CE}$ Precharge-$\overline{RFSH}$ Delay Time	80		ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width	100	2,000	ns	
t_{FP}	$\overline{RFSH}$ Precharge Time	80		ns	
t_{FSC}	$\overline{RFSH}$ Precharge-$\overline{CE}$ Delay Time	80		ns	

Note

(1) Stress greater than those listed under "Absolute maximum ratings" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}.

(3) I_{CC1} and I_{CC2} depend on cycle time. These values are specified at the condition of minimum cycle time.

(4) I_{CC1} depends on output loading. Specified value is obtained with the output open.

(5) An initial pause of 200μs is required after power up followed by 8 $\overline{CE}$ cycles before proper device operation is achieved. In case of using auto refresh, a minimum of 8 $\overline{RFSH}$ cycle are required.

(6) AC measurements assume t_T=5ns.

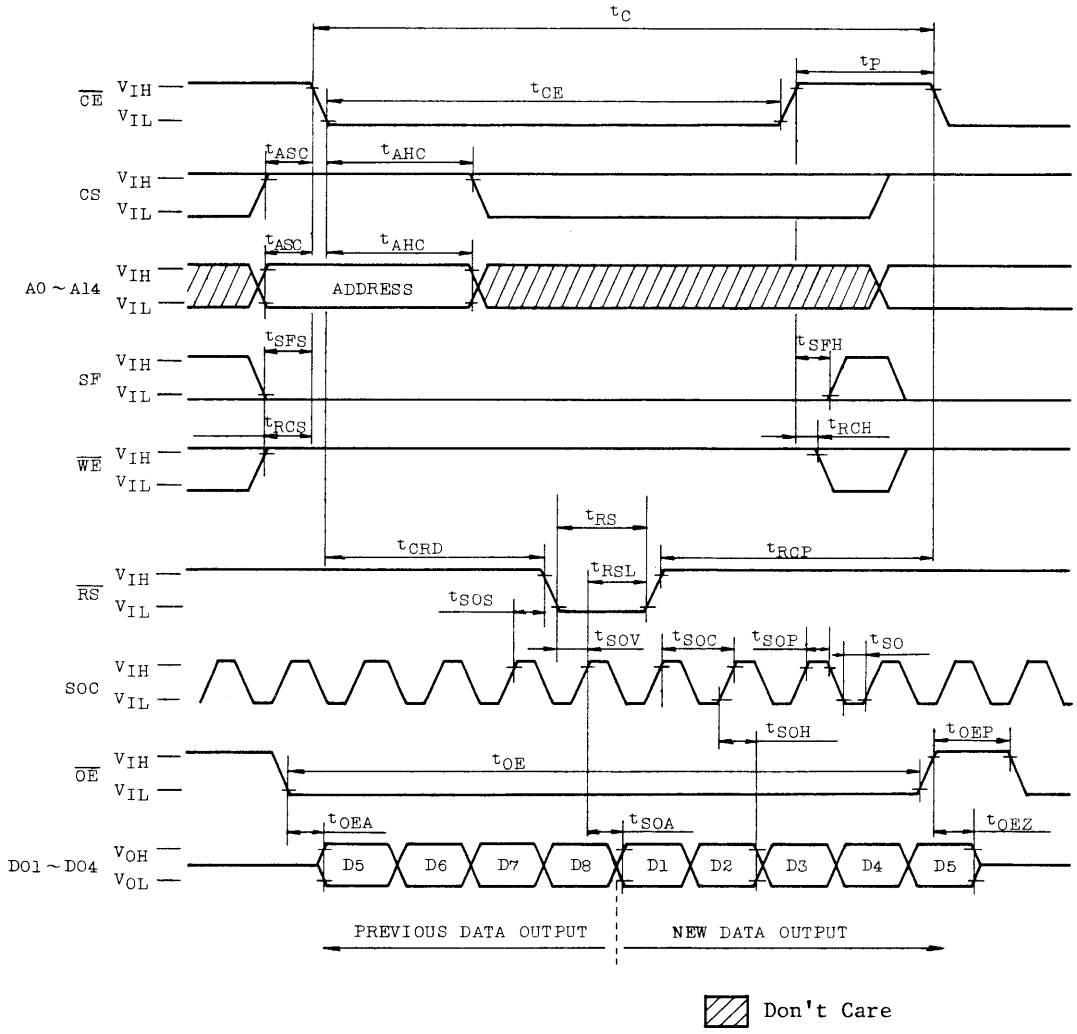
(7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.

(8) Output timings are measured with a load equivalent to 2 TTL load and 50pF.

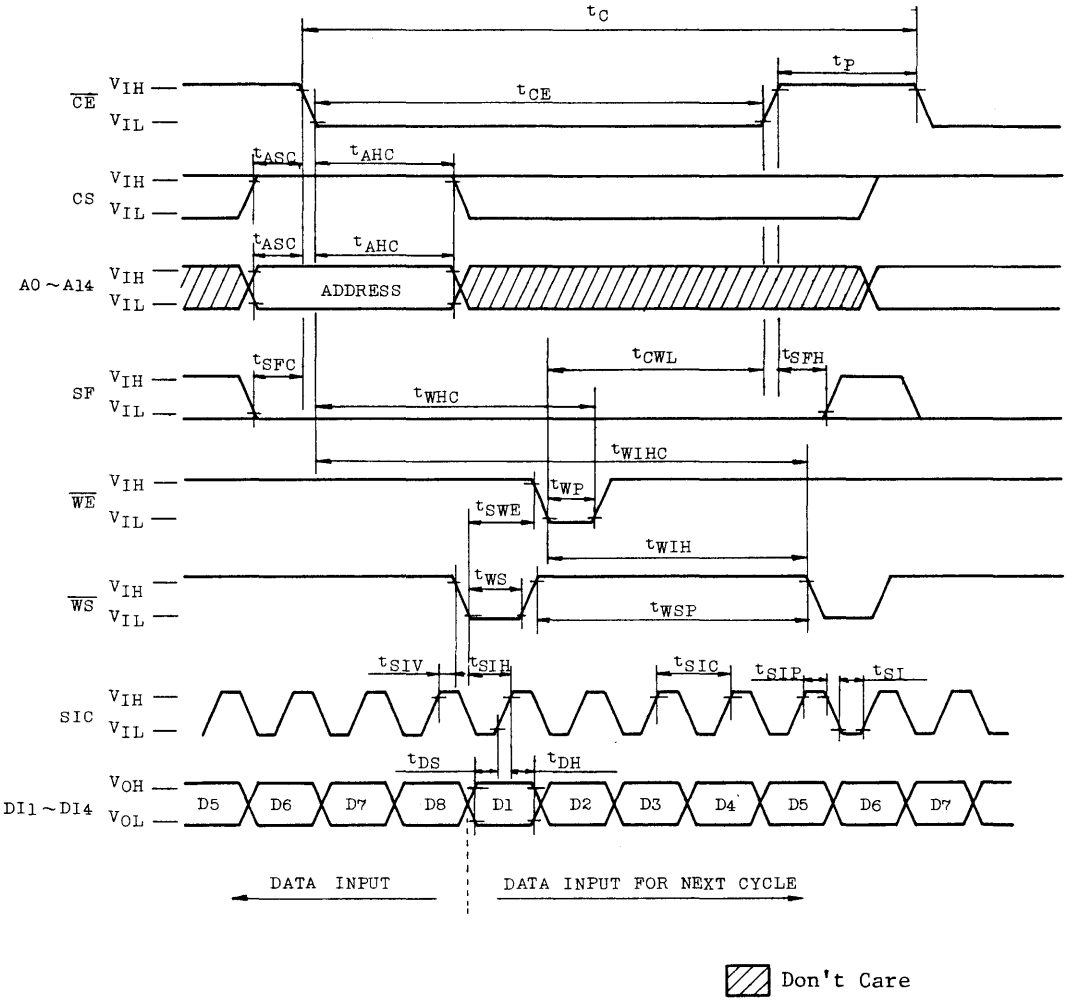
(9) t_{OEZ}(max.) defines the time at which the output achieve the open state.

(10) Typical values are at Ta=25°C and V_{CC}=5.0V.

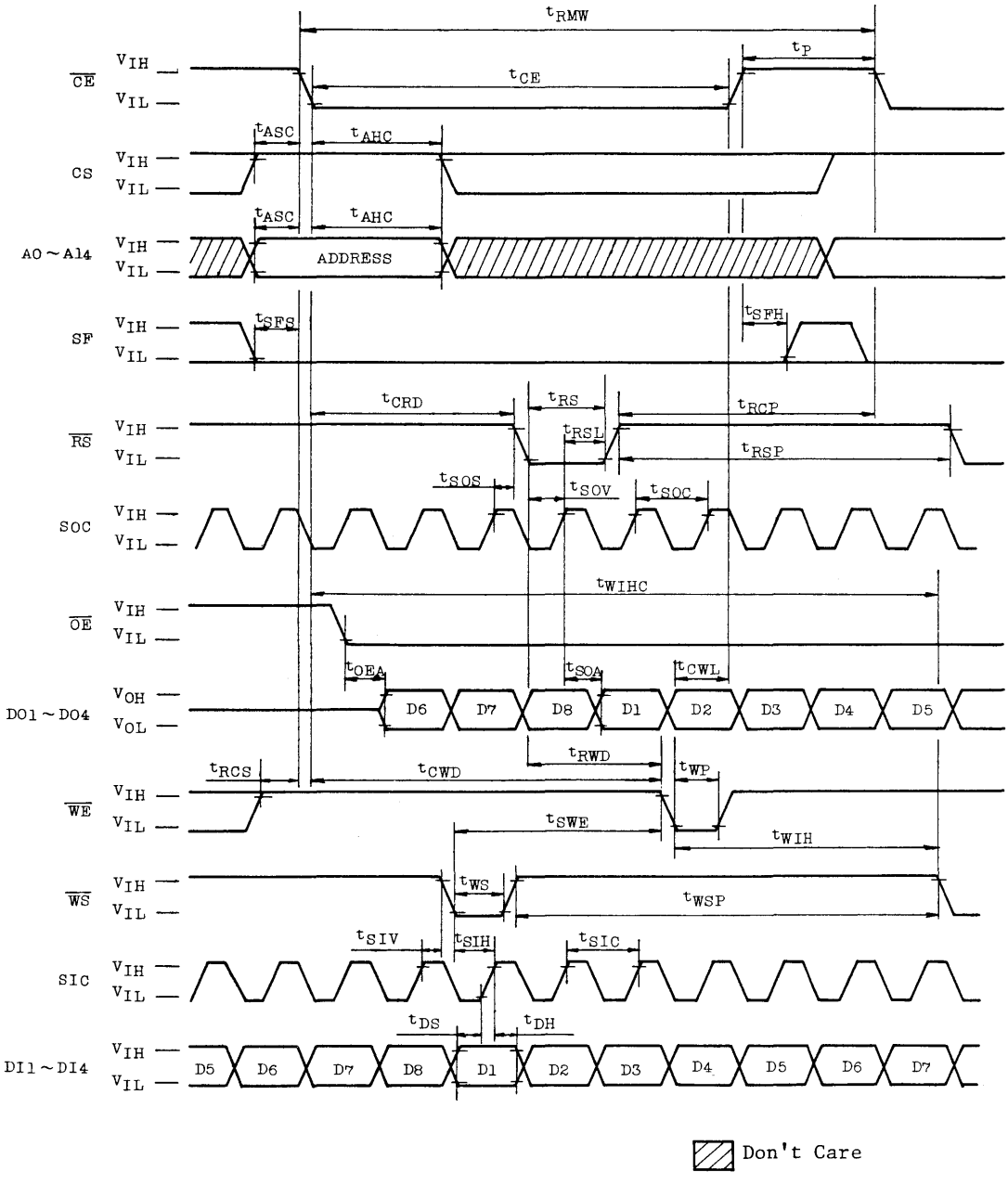
READ/SERIAL READ CYCLE



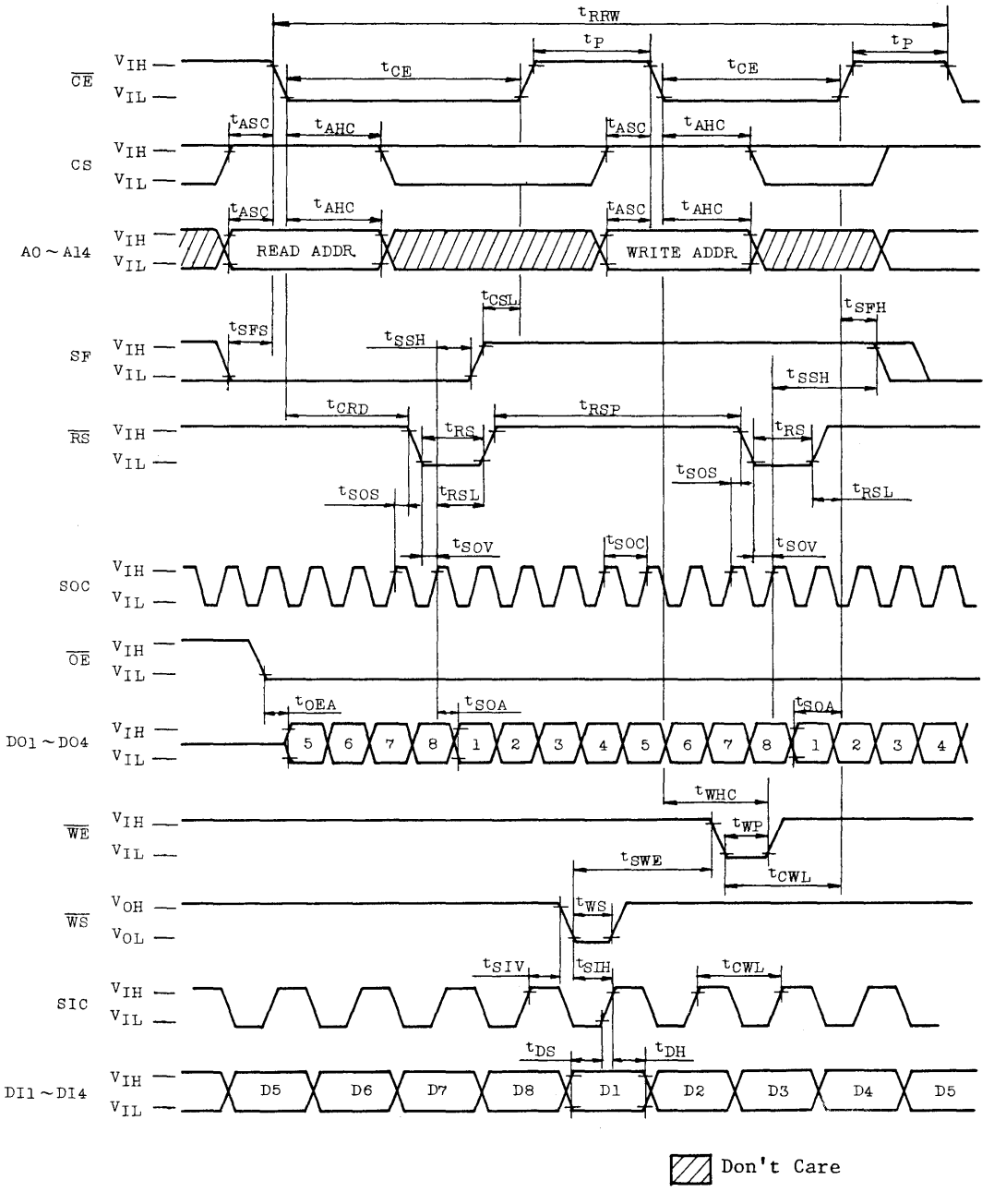
WRITE/SERIAL WRITE CYCLE



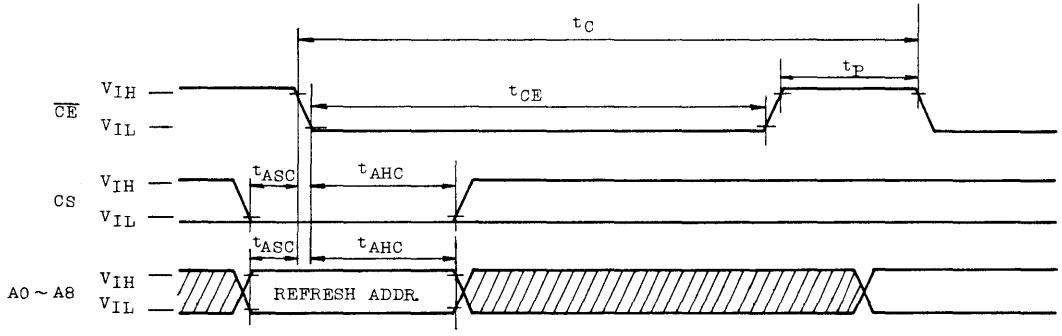
READ MODIFY WRITE CYCLE



READ-READ-WRITE CYCLE

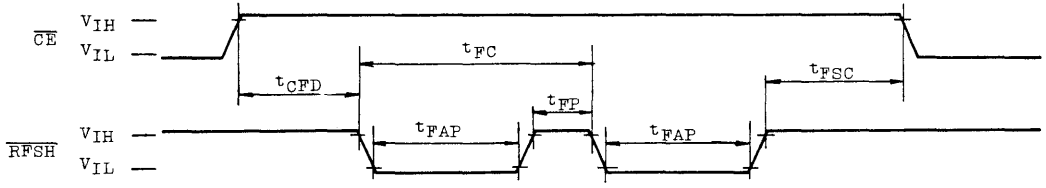


$\overline{CE}$ ONLY REFRESH



$\overline{WE}$, A9 ∿ 14 ..... Don't Care

$\overline{RFSH}$ AUTO REFRESH



$\overline{WE}$, A9 ∿ 14 ..... Don't Care

Don't Care

OPERATION INFORMATION

(1) READ/SERIAL READ CYCLE

i) SERIAL READ CYCLE (Refer to Fig. 1, 2)

[1] The read address is latched at the falling edge of $\overline{CE}$. The 8 bit data read out are transferred to and latched into the read latch (RL).

[2] The data latched at the RL are transferred to serial output register (SOR) at the first rising edge of SOC after the $\overline{RS}$ goes low.

[3] The 8 bit data transferred to the SOR are shifted and output sequentially synchronized with SOC from the first rising edge of SOC after the $\overline{RS}$ falls.

Fig.1 Block Diagram

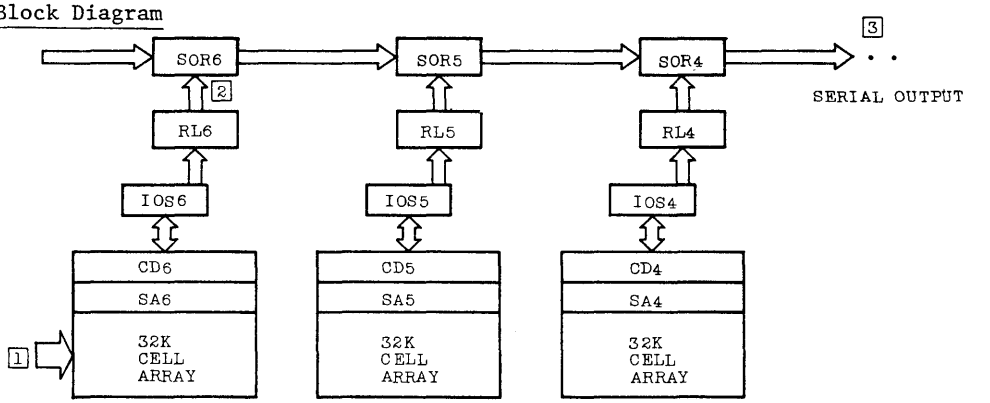
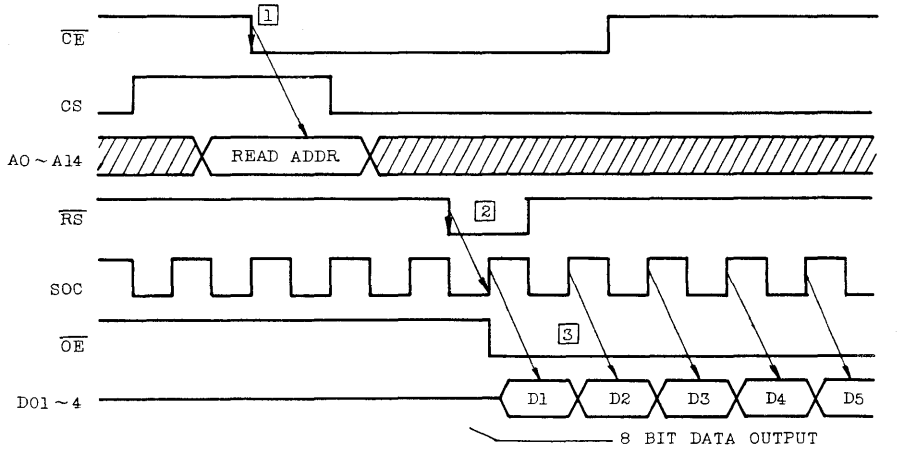


Fig.2 Timing Diagram



(2) WRITE/SERIAL WRITE CYCLE (Refer to Fig. 3, 4)

[1] The 8 bit input data are latched into the 8 bit serial input register (SIR) sequentially synchronized with SIC.

[2] The 8 bit input data latched into the SIR are transferred to the write latch (WL) at the falling edge of $\overline{WS}$.

[3] The write address is latched at the falling edge of $\overline{CE}$, same as read operation. Then the data stored in selected address to be written are read out and latched into the RL independent of this write operation, so the read data latched there can be read out through SOR by using $\overline{RS}$ and SOC (Read-Modify-Write).

[4] The 8 bit input data latched into the WL are written into the selected address location at the falling edge of $\overline{WE}$.

Fig.3 Block Diagram

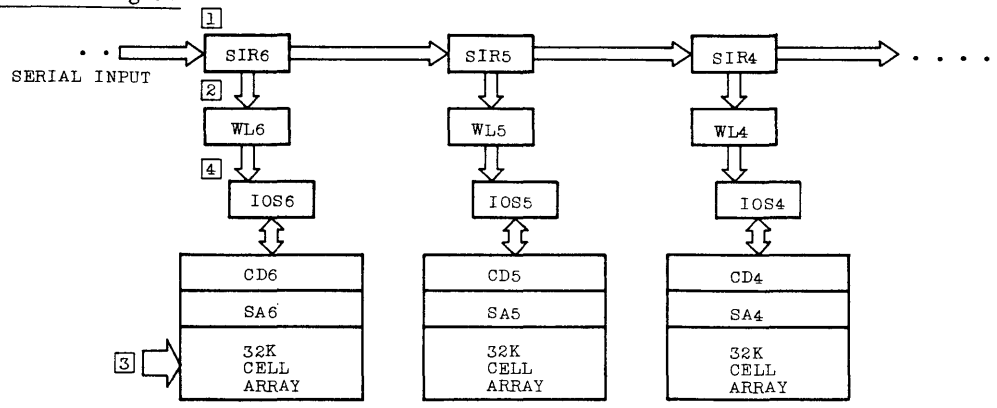
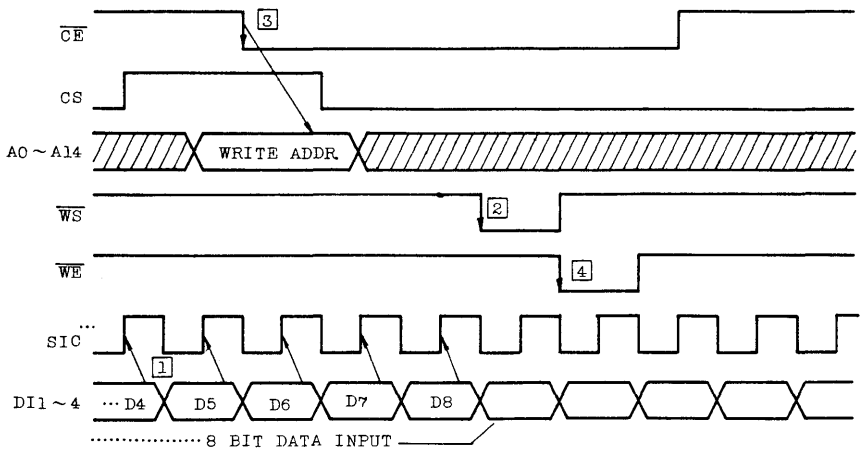


Fig.4 Timing Diagram



(3) READ-MODIFY-WRITE CYCLE

This operation is to execute write just after read in one $\overline{CE}$ cycle.

(4) READ-READ-WRITE CYCLE (Special operation) (Refer to Fig. 5, 6)

By using SF signal, three operations - the read operation for consecutive two address (16 bit data output) and write operation into the different address from read (8 bit data input) - can be performed asynchronously in two $\overline{CE}$ cycles (480ns). In this operation, the read start address must be even. This operation capability allows the field double scan in order to improve the picture quality in TV applications.

[1] The read address (even) is latched at the falling edge of $\overline{CE}$ under the condition of SF=low. Then the 8 bit read out data are transferred to and latched into the RL.

[2] The 8 bit data latched into the RL are transferred to SOR by the $\overline{RS}$, and then the data latched into the SOR are shifted and output from the first rising edge of SOC after the $\overline{RS}$ falls.

[3] Then when SF goes high, the LSB bit (A14) of coulumn addresses is changed to "1" from "0" automatically, and the data in the next column address are transferred to and latched into the RL.

[4] When the $\overline{CE}$ goes high, only memory cell array its peripheral area except for the latch and serial registers are placed in a precharge state. Then the data latched into the RL and SOR are maintained there, so the $\overline{WS}$ and $\overline{RS}$ can be input.

[5] On the other hand, the 8 bit input data are latched into the SIR sequentially synchronized with the SIC and then transferred to and latched into the WL by the $\overline{WS}$.

[6] The write address is latched at the falling edge of $\overline{CE}$, and then the data stored in the selected address is read out, but the data already latched into the RL are protected and retained there because of maintaining the SF "high".

[7] The 8 bit data latched into the RL (in [3]) are transferred to and latched into the SOR by the $\overline{RS}$.

[8] The 8 bit data latched into the WL (in [5]) are written into the selected cell locations by the $\overline{WE}$.

Fig.5 Block Diagram

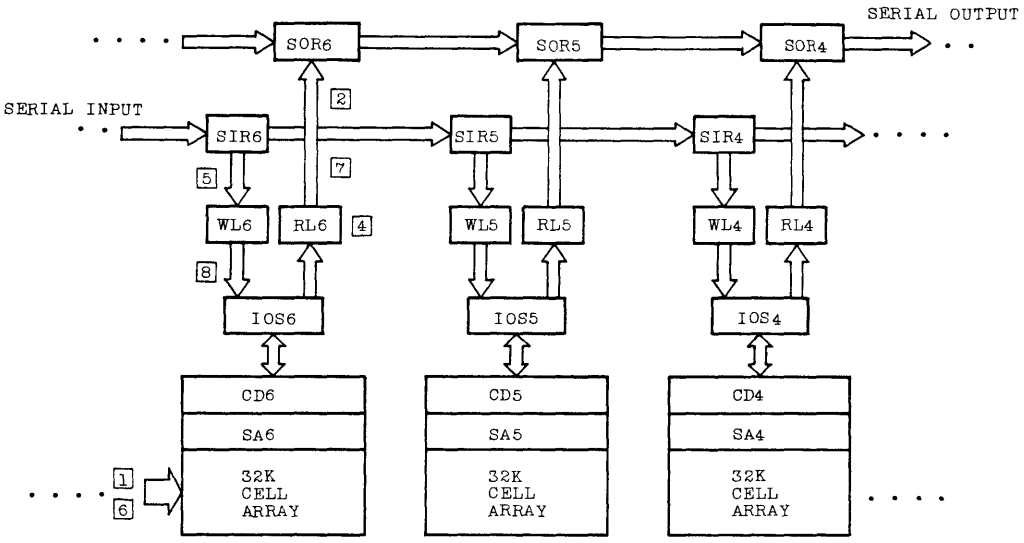
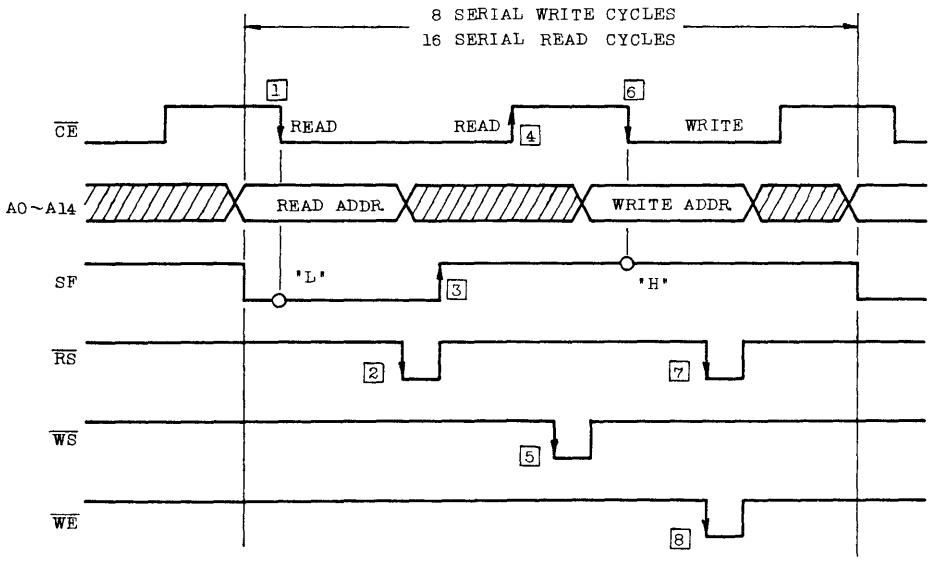


Fig.6 Timing Diagram



(5) REFRESH

The TC521000P's refresh period is 8ms/512 cycles.

Two types of refresh operation - $\overline{CE}$ only refresh and $\overline{RFSH}$ auto refresh - are allowed.

5-1: $\overline{CE}$ only refresh

The refresh is accomplished by performing a $\overline{CE}$ cycle at each of the 512 low address (A0 ∿ A8) within each 8ms time interval.

5-2: $\overline{RFSH}$ auto refresh

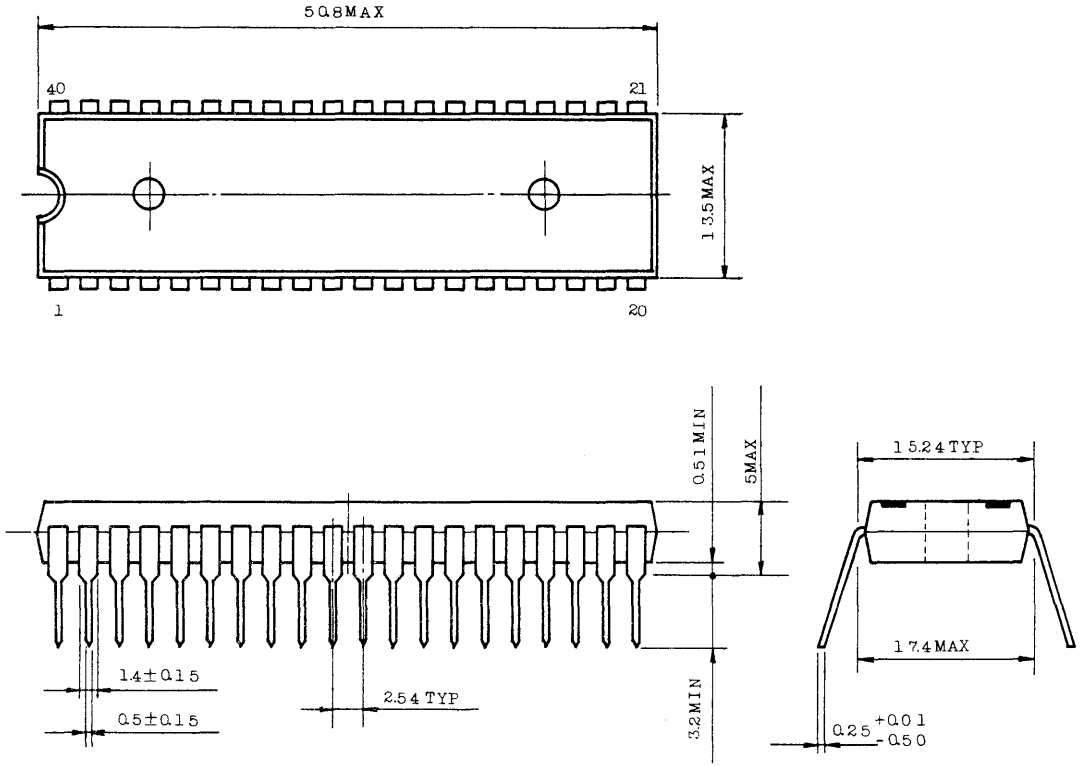
The $\overline{RFSH}$ auto refreshis available on the TC521000P.

When the $\overline{RFSH}$ goes low under the condition of $\overline{CE}$=high, on chip refresh control clock generator and refresh address counters are enabled.

Then, the refresh is accomplished by applying 512 clocks to the $\overline{RFSH}$ input within 8ms time interval.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.40 leads.

262,144 WORDS×4 BITS MULTIPORT DYNAMIC RAM
SILICON GATE CMOS

TC524256P/Z-10, TC524256P/Z-12

PRELIMINARY

DESCRIPTION

The TC524256P/Z is a CMOS Multiport memory equipped with a 262,144-word x 4 bit dynamic random access memory (RAM) port and a 512-word x 4 bit static serial access memory (SAM) port. In addition to the conventional DRAM operation modes, the TC524256P/Z features a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

The TC524256P/Z is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplexed address inputs and a common input/output organization allow the TC524256P/Z to be housed in a standard 28-pin, 400-mil wide plastic DIP and 400-mil height ZIP. System oriented features include a single 5V ± 10% power supply operation and compatibility with high performance schottky TTL logic.

FEATURES

ITEM		TC524256P/Z	
		−10	−12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time (Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	60mA	55mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	40mA	35mA
I_{CC2}	RAM/SAM Standby Current	3mA	

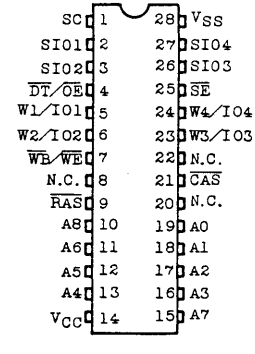
- Organization
  RAM port: 262,144 words x 4 bits
  SAM port : 512 words x 4 bits
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, Page mode, Write-Per-Bit, Read transfer, Write transfer, Serial read, Serial Write capability
- All inputs and outputs TTL compatible
- 512 refresh cycle/8ms
- Package TC524256P: 0.4 inches 28 pins standard Plastic DIP
  TC524256Z: 0.4 inches 28 pins standard Plastic ZIP

PIN NAMES

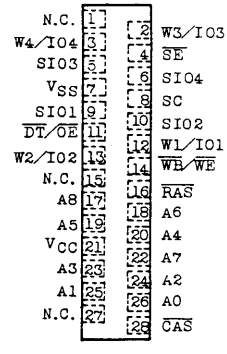
A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
W1/I01 ~ W4/I04	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SI01 ~ SI04	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

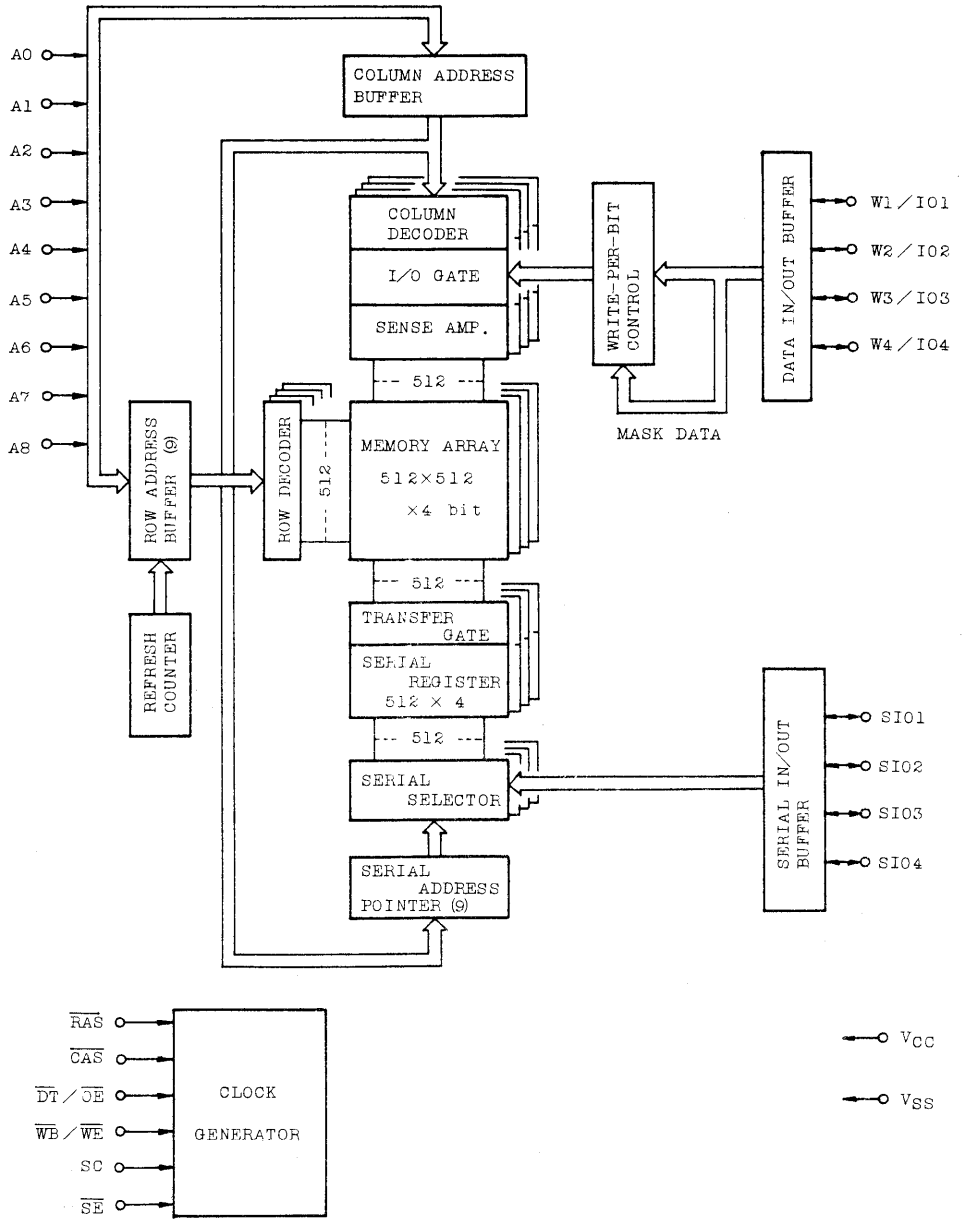
Plastic DIP



Plastic ZIP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}, V_{OUT}	Input Output Voltage	-1.0 ∿ 7.0	V	1
V_{CC}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{opr}	Operating Temperature	0 ∿ 70	°C	1
T_{stg}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITION (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	ITEM (RAM Port)	SAM Port	TC524256P/Z-10		TC524256P/Z-12		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
I_{CC1}	OPERATING CURRENT	Standby	-	60	-	55	mA	3,4
I_{CC1A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	Active	-	100	-	90		3,4
I_{CC2}	STANDBY CURRENT	Standby	-	3	-	3	mA	
I_{CC2A}	($\overline{RAS}$, $\overline{CAS}$=V_{IH})	Active	-	40	-	35		3,4
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT	Standby	-	60	-	55	mA	3
I_{CC3A}	($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	Active	-	100	-	90		3,4
I_{CC4}	PAGE MODE CURRENT	Standby	-	50	-	45	mA	3,4
I_{CC4A}	($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=t_{PC} MIN.)	Active	-	90	-	80		3,4
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT	Standby	-	60	-	55	mA	3
I_{CC5A}	($\overline{CAS}$ Before $\overline{RAS}$ Cycling: t_{RC}=t_{RC}MIN.)	Active	-	100	-	90		3,4
I_{CC6}	DATA TRANSFER CURRENT	Standby	-	60	-	55	mA	3
I_{CC6A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	Active	-	100	-	90		3,4

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNITS	NOTES
$I_{I(L)}$	INPUT LEAKAGE CURRENT ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test=0V)	-10	0	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (Output is disabled, $0V \leq V_{OUT} \leq 5.5V$)	-10	0	10	μA	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE (Wi/IOi, SIOi ..... I_{OUT}=-5mA)	2.4	-	-	V	
V_{OL}	OUTPUT LOW LEVEL VOLTAGE (Wi/IOi, SIOi ..... I_{OUT}=+4.2mA)	-	-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (NOTES 5, 6, 7)

SYMBOL	PARAMETER	TC524256P/Z-10		TC524256P/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{RWC}	Read-Write Cycle Time	250		290			
t_{PC}	Page Mode Cycle Time	90		105			
t_{PRWC}	Page Mode Read-Write Cycle Time	150		175			
t_{RAC}	Access Time from $\overline{RAS}$		100		120		8,14
t_{CAC}	Access Time from $\overline{CAS}$		50		60		8,14
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90			
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000		
t_{RSH}	$\overline{RAS}$ Hold Time	50		60			
t_{CSH}	$\overline{CAS}$ Hold Time	100		120			
t_{CAS}	$\overline{CAS}$ Pulse Width	50		60			
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	60		
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20			
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode)	30		35			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		15			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	20		25			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	70		85			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10			11
t_{WCH}	Write Command Hold Time	20		25			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	70		85			
t_{WP}	Write Command Pulse Width	20		25			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35			
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	20		25			12
t_{RASP}	$\overline{RAS}$ Pulse Width (Page Mode)	190	100,000	225	100,000		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION (Continued)

SYMBOL	PARAMETER	TC524256P/Z-10		TC524256P/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	70		85			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	125		150			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	75		90			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		25		30		
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	20	0	25	ns	10
t_{OED}	$\overline{OE}$ to Data Input Delay Time	20		25			
t_{OEH}	$\overline{OE}$ Command Hold Time	20		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	20		20			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	20		20			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	40		50			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	10		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	10		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	10		15		ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	80		95			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	30		35			
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	10		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	80		90			
t_{RP}	$\overline{DT}$ Precharge Time	30		35			
t_{RSD}	$\overline{RAS}$ to First $\overline{SC}$ Delay Time (Read Transfer)	100		120			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION

SYMBOL	PARAMETER	TC524256P/Z-10		TC524256P/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	50		60		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		10			
t_{TSD}	$\overline{DT}$ to Frist SC Delay Time (Read Transfer)	15		20			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		40			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		30			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		60			
t_{SDZ}	Serial Output Buffer Trun-Off Delay Time $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	60		10
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SCC}	SC Cycle Time	30		40			
t_{SC}	SC Pulse Width (SC High Time)	10		15			
t_{SCP}	SC Precharge Time (SC Low Time)	10		15			
t_{SCA}	Access Time from SC		25		35		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	20		30			
t_{SEA}	Access Time from $\overline{SE}$		25		35		9
t_{SE}	$\overline{SE}$ Pulse Width	25		35			
t_{SEP}	$\overline{SE}$ Precharge Time	25		35			
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	30		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	5		10			
t_{SEH}	Serial Write Enable Hold Time	15		20			
t_{SWIS}	Serial Write Disable Set-Up Time	5		10			
t_{SWIH}	Serial Write Disable Hold Time	15		20			

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$)	-	5	
C_{IO1}	Input/Output Capacitance (W1/IO1∿W4/IO4)	-	7	
C_{IO2}	Input/Output Capacitance (SIO1∿SIO4)	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.

9. SAM port outputs are measured with a load equivalent to 2 TTL loads and 50pF.

10. t_{OFF}(max.), t_{OEZ}(max.) t_{SDZ}(max.) and t_{SEZ}(max.) define the time at which the output achieve the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in read-write cycles.

13. t_{WCS}, t_{RWD} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.) and $t_{CWD} \geq t_{CWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

DEVICE INFORMATION

RAM PORT OPERATION

Operation Truth Table

All operation modes of TC524256P/Z are determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, and $\overline{SE}$ at the falling edge of $\overline{RAS}$. They are shown in the following table 1.

$\overline{RAS}$	$\overline{CAS}$	ADDRESS	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION
H	H	*	*	*	*	Standby
↓	H	Valid	H→L	H	*	Read
	H	Valid	H	H→L	*	Write
	H	Valid(Row add.)	H	*	*	$\overline{RAS}$ only refresh
	L	*	H(1)	H	*	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
	H	Valid	H	L	*	Write-per-Bit
	H	Valid	L	H	*	Read Transfer
	H	Valid	L	L	L	Write Transfer
	H	Valid	L	L	H	Pseudo-Write Transfer

Note; H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

(1) The input level of $\overline{DT}/\overline{OE}$ in the $\overline{CAS}$ before $\overline{RAS}$ timing is not ristricted. However it is recommended that $\overline{DT}/\overline{OE}$ be held 'High' because this input will be used for future expansion of the operation mode.

ADDRESSING

The 18 address bits required to decode 4-bits of the 1,048,576 cell locations within the Dynamic RAM memory array of the TC524256P/Z, are multiplexed onto 9 address input pins (A0 ∿ A8). Nine row-address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

DATA TRANSFER/OUTPUT ENABLE ($\overline{DT}/\overline{OE}$)

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is 'High' at the falling edge of $\overline{RAS}$, a normal DRAM cycle is performed and this input is used as an output enable. When $\overline{DT}/\overline{OE}$ is 'Low' at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE-PER-BIT/WRITE-ENABLE ($\overline{WB}/\overline{WE}$)

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. For conventional DRAM cycle, the $\overline{WB}/\overline{WE}$ input is used in the same manner as standard DRAMs except when the write-per-bit function is used. When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the bit write-mask is enabled. When $\overline{WB}/\overline{WE}$ and $\overline{CAS}$ are 'low' at the falling edge of $\overline{RAS}$, the raster operation set-up cycle is executed.

The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the DRAM memory array and the serial register. When $\overline{WB}/\overline{WE}$ is 'high' at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read-transfer cycle). When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write-transfer cycle).

WRITE-MASK DATA/DATA INPUT/OUTPUT (W1/IO1 to W4/IO4)

When the write-per-bit function is enabled, the mask data on the W1/IO1 pins is latched into the write-mask register WM1 at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic '1'. Writing is inhibited on data lines where the write-mask data is a logic '0'. The write-mask data is valid for only one cycle.

PAGE MODE

The page mode feature of the TC524256P/Z allows data to be transferred into of multiple column locations of the same row by having multiple column cycles during a single active $\overline{RAS}$ cycle.

For the initial page mode access, the output data is valid after the specified access time from $\overline{RAS}$. For all subsequent page mode read operations, the output data is valid after the specified access time from $\overline{CAS}$. As a result, page mode operation reduces power dissipation and improves data access time.

When the write-per-bit function is enabled, the mask data specified in the first write operation, at the falling edge of $\overline{RAS}$, is maintained throughout the page mode write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM cycle requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with '$\overline{RAS}$-ONLY' cycles.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

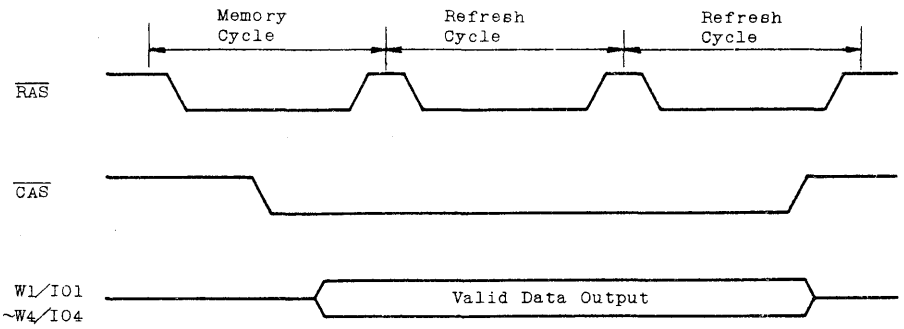
The TC524256P/Z also offers an internal refresh function. When $\overline{CAS}$ is held 'low' for a specified period (t_{CSR}) before $\overline{RAS}$ goes low, an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$.

During a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{WB}/\overline{WE}$ must be 'high' at the falling edge of $\overline{RAS}$ to prevent a false raster operation set-up cycle from occurring.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ 'low' from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (refer to figure 1).

Figure 1: Hidden refresh cycle



WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/IOi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/IOi pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in table 2.

Table 2: Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/IOi (i=1∿4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in figures 2 and 3.

Figure 2: Write-per-bit timing cycle

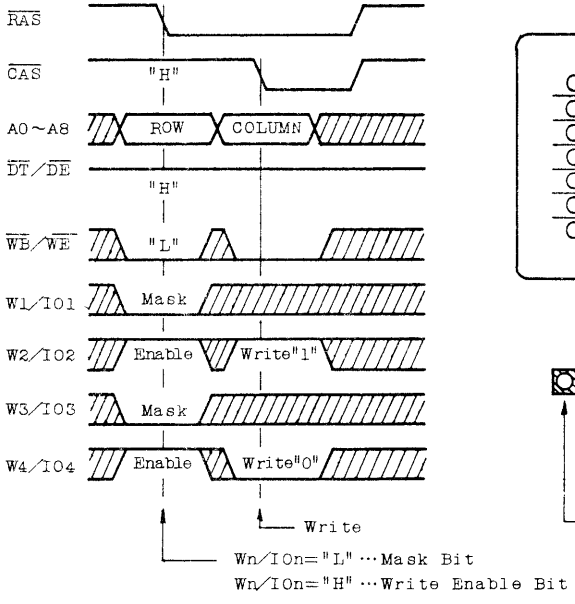
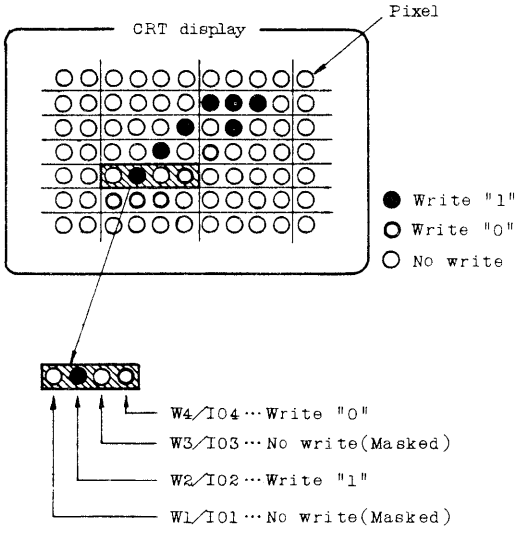


Figure 3: Corresponding bit-map



TRANSFER OPERATION

The TC524256P/Z features bi-directional transfer capability form RAM to SAM and from SAM to RAM. A transfer consists of loading 512 words by 4-bits of data from one port into the other. During a transfer cycle, RAM port and SAM port operations are restricted.

There are three types of transfer operations: read transfer, write transfer and pseudo-write transfer. As shown in table 3, the type of transfer operation is determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Table 3: Truth table of transfer operation

At the falling edge of $\overline{RAS}$					Transfer direction
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$		
H	L	H	*	Read/real-time read transfer cycle	RAM → SAM
H	L	L	L	Write-transfer cycle	SAM → RAM
H	L	L	H	Pseudo-write transfer cycle	-

*: high or low

READ-TRANSFER CYCLE

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM.

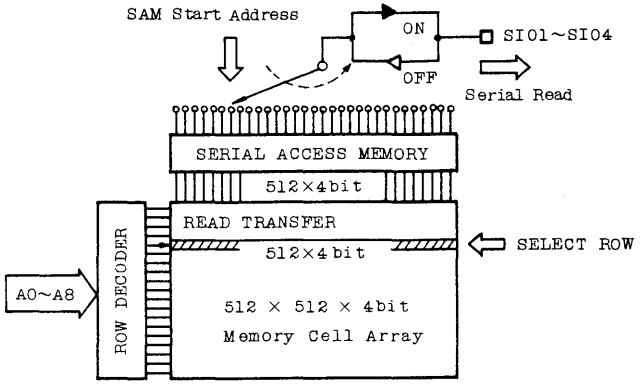
The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$.

When the transfer is completed, the SIO lines are set into the output mode.

In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock(SC) cycle.

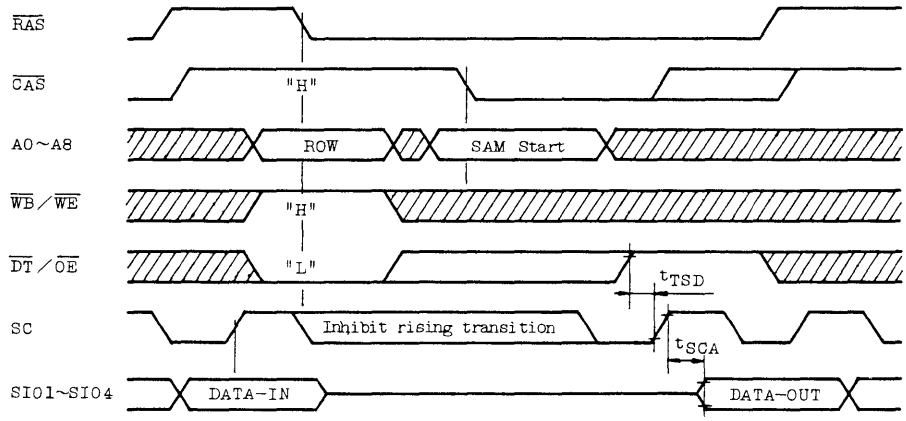
The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$. (refer to figure 4).

Figure 4: Block diagram of RAM port and SAM port during read transfer



In a read-transfer cycle (which is preceded by a write-transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ (refer to Figure 5).

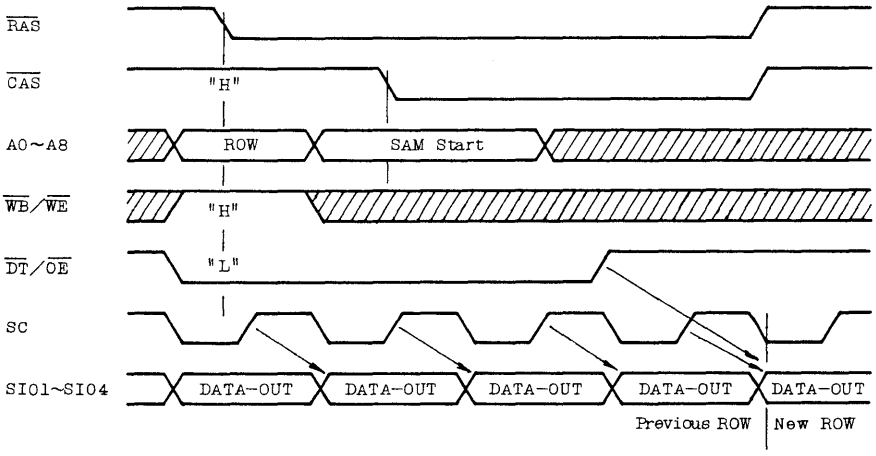
Figure 5: Read-transfer cycle (preceded by a write-transfer cycle)



In a real-time read-transfer cycle (which is preceded by another read-transfer cycle), the previous row data appears on the SIO lines until the specified t_{SCA} access time from the same rising edge of SC.

This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed, without any timing loss. To make this continuous data flow possible: the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (refer to Figure 6).

Figure 6: Real-time read transfer cycle

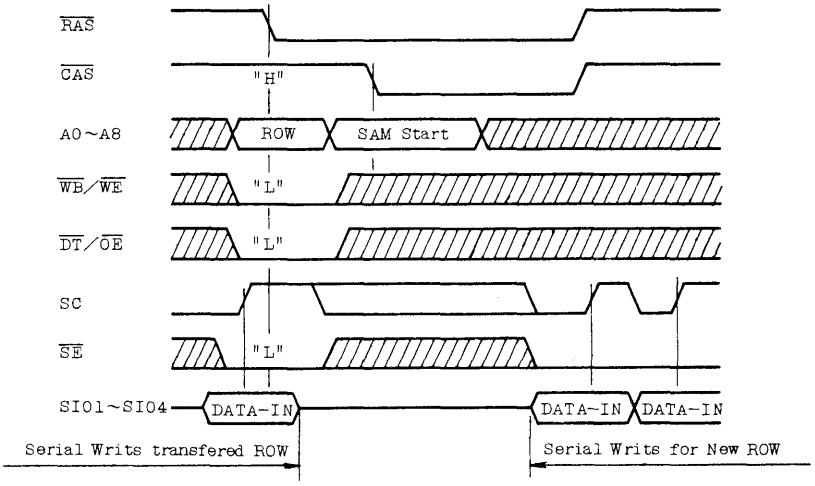


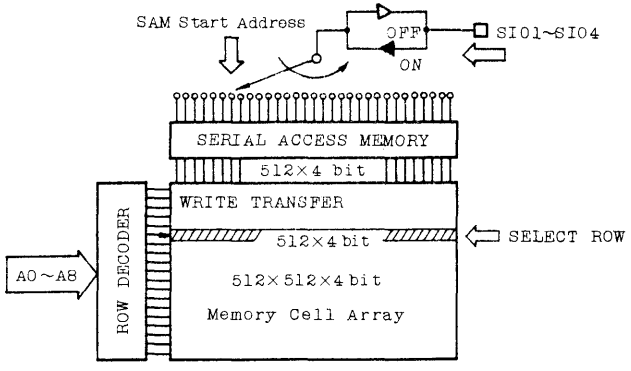
WRITE-TRANSFER CYCLE

A write-transfer cycle consists of loading the content of the SAM data register into a selected row or the RAM array. A write-transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write-transfer is completed, the SIO lines are in the input mode so that serial data synchronized with SC can be loaded.

When two consecutive write-transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SC} has seen satisfied, a rising edge of the SC clock until after a specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to figure 7).

Figure 7: Write-transfer cycle



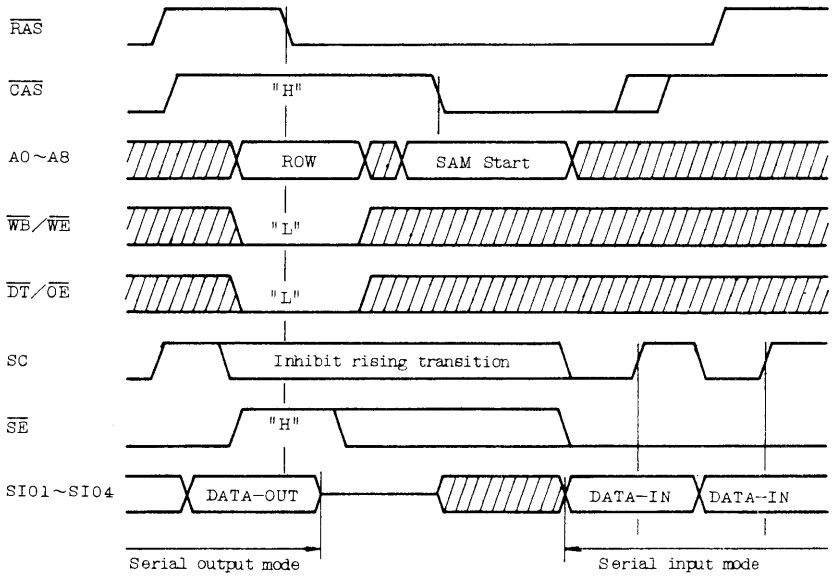


PSEUDO-WRITE-TRANSFER CYCLE

The pseudo-write-transfer cycle switches SIO lines from serial output mode to serial input mode. A pseudo-write-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo-write-transfer cycle must be performed after a read-transfer cycle if the subsequent operation is a write-transfer cycle.

There is a timing delay associated with the switching of the SIO lines from serisl output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to Figure 8).

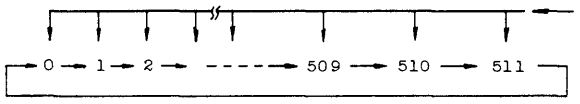
Figure 8: Pseudo-write-transfer cycle



SAM PORT OPERATION

The TC524256P/Z is provided with a 512-word by 4-bit serial access memory (SAM). High-speed read and write operation may be performed through the SAM port independent of the RAM port operations, except during transfer operations. The preceding transfer operation determines the direction of data flow through the SAM registers.

Data may be read out of the SAM port after a read-transfer cycle (RAM → SAM) has been performed. Data can be shifted out of the SAM port starting at any of the 512-bit locations. This tap location corresponds to the column address selected a the falling edge of $\overline{CAS}$ during the read-transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit.



Tap location determined by column address of read-transfer cycle.

Subsequent real-time-read-transfer may be performed on-the-fly as many times as desired within the refresh constrainst of the DRAM memory array.

A pseudo-write-transfer cycle must be performed in order to write data into the SAM port. This cycle switches the SAM port operation from output mode to input mode. Data is not transferred during a pseudo-write-transfer cycle. A write-transfer cycle (SAM → RAM) may then be performed. The data in the SAM registers is loaded into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The start address of SAM registers is determined by the column address selected at the falling edge of $\overline{CAS}$.

Table 4: Truth table for SAM operation

Preceding Transfer Cycle	SAM port operation	$\overline{DT}/\overline{OE}$ (at the falling edge of $\overline{RAS}$)	SC	$\overline{SE}$	Function
read-transfer	serial output mode	H*	⎍	L	enable serial read
				H	disable serial read
write-transfer	serial input mode		⎍	L	enable serial write
				H	disable serial write

* When simultaneous operation are being performed on the RAM port and the SAM port, $\overline{DT}/\overline{OE}$ must be held high at the falling edge of $\overline{RAS}$ so as not to perform a false transfer cycle.

SERIAL CLOCK (SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial-read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.

The serial clock SC also increments the 9-bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read-transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).

SERIAL ENABLE ($\overline{SE}$)

The $\overline{SE}$ input is used to enable serial access operation. In a serial-read cycle, $\overline{SE}$ is used as an output control. In a serial-write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is high, serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is high.

SERIAL INPUT/OUTPUT (SIO1 ∿ SIO4)

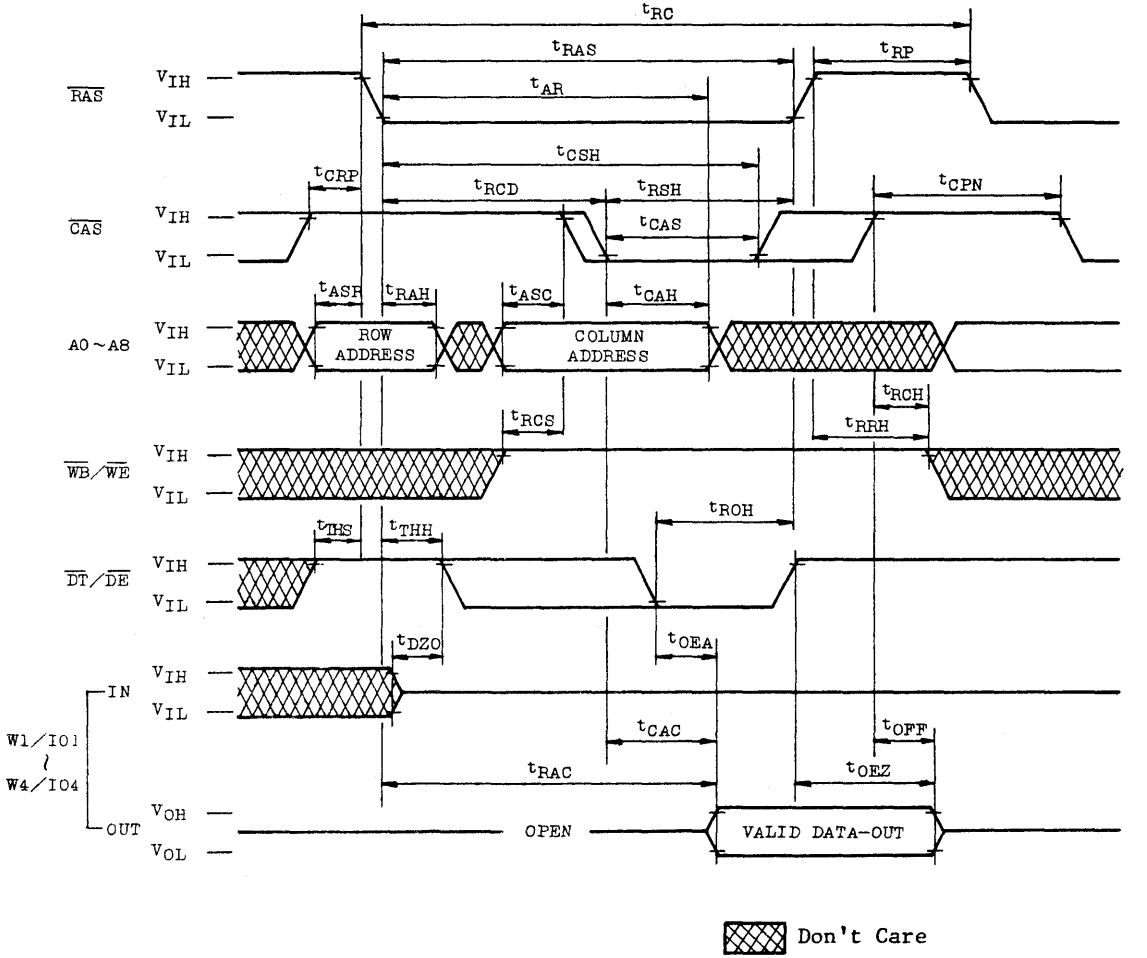
Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read-transfer cycle is performed, the SAM port is in the output mode. When a pseudo-write cycle is performed, the SAM port operation is switched from output mode to input mode.
During subsequent write-transfer cycle, the SAM port remains in the input mode.

REFRESH

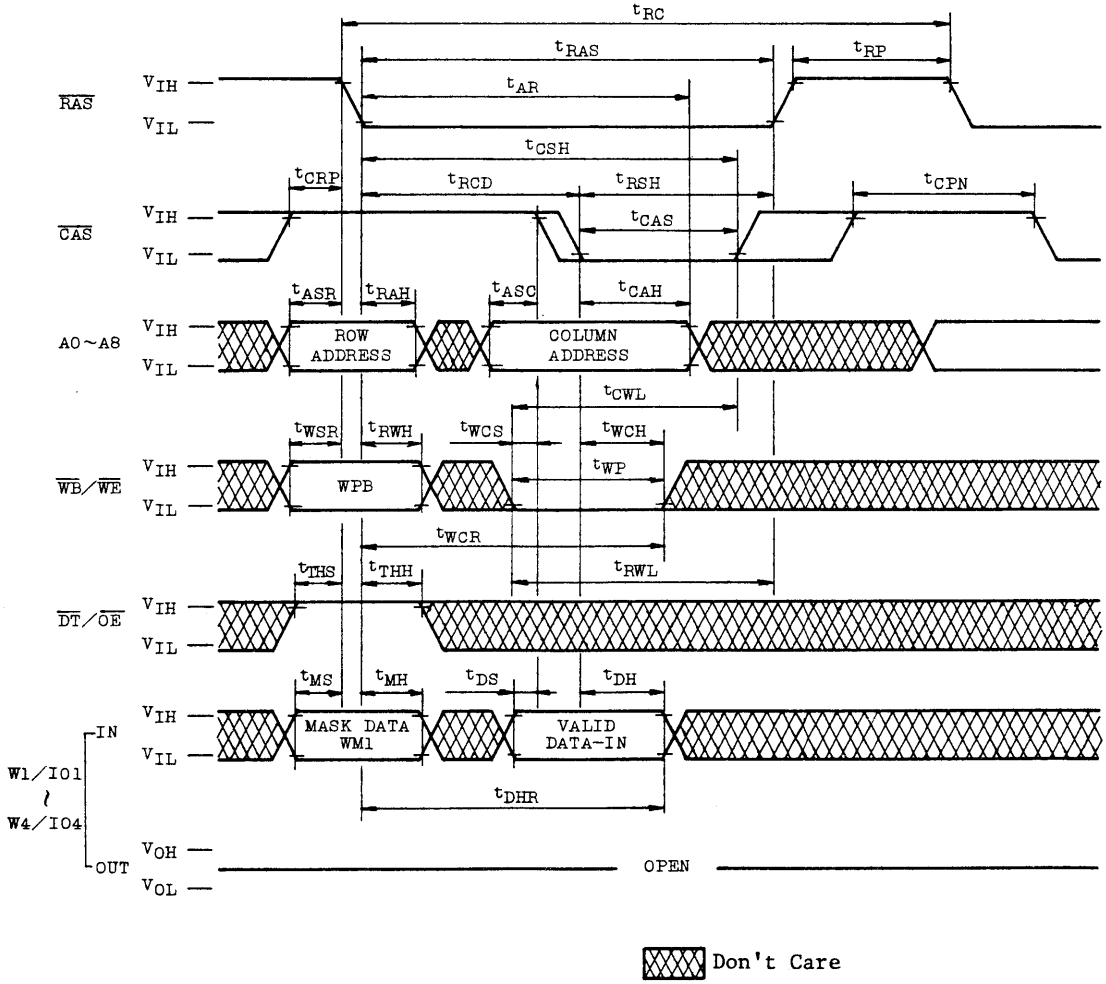
The SAM data registers are static flip-flops therfore a refresh is not required.

TIMING WAVEFORMS

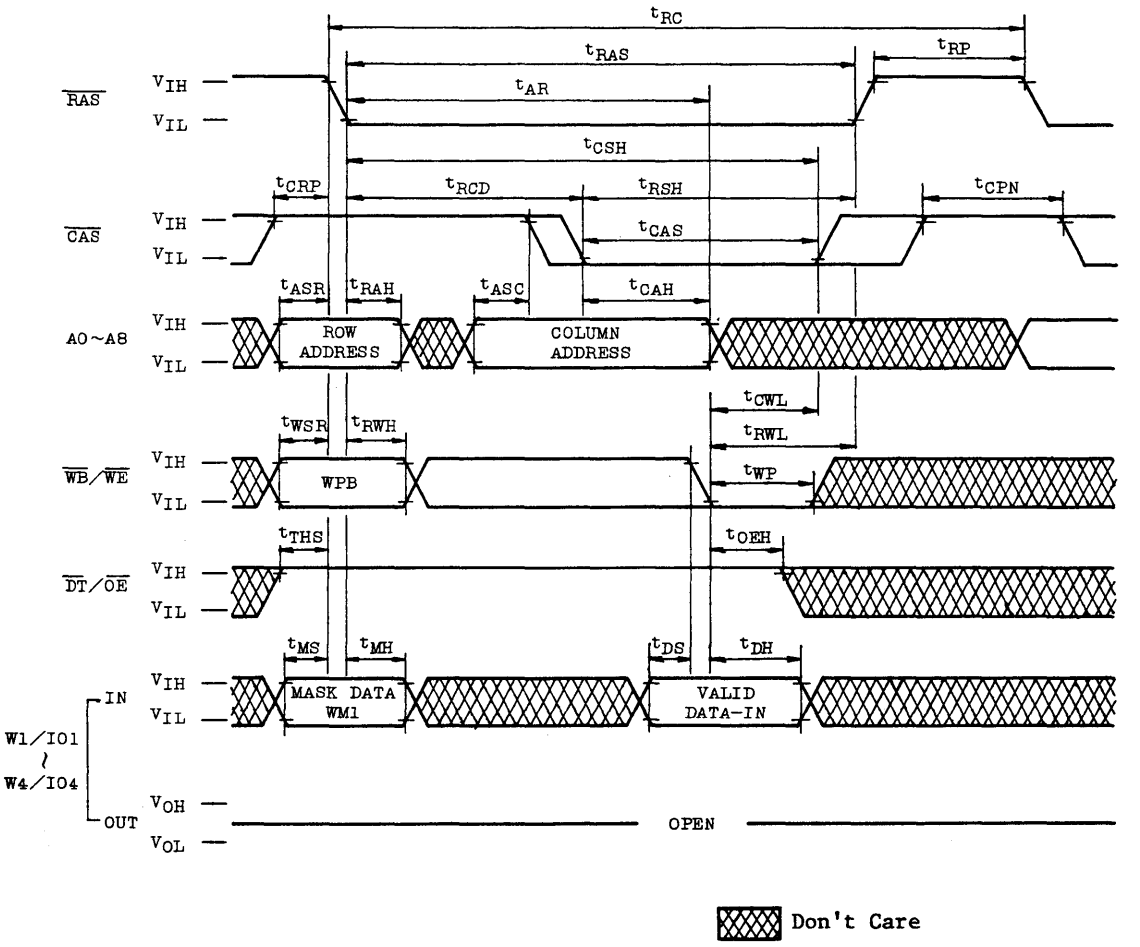
READ CYCLE



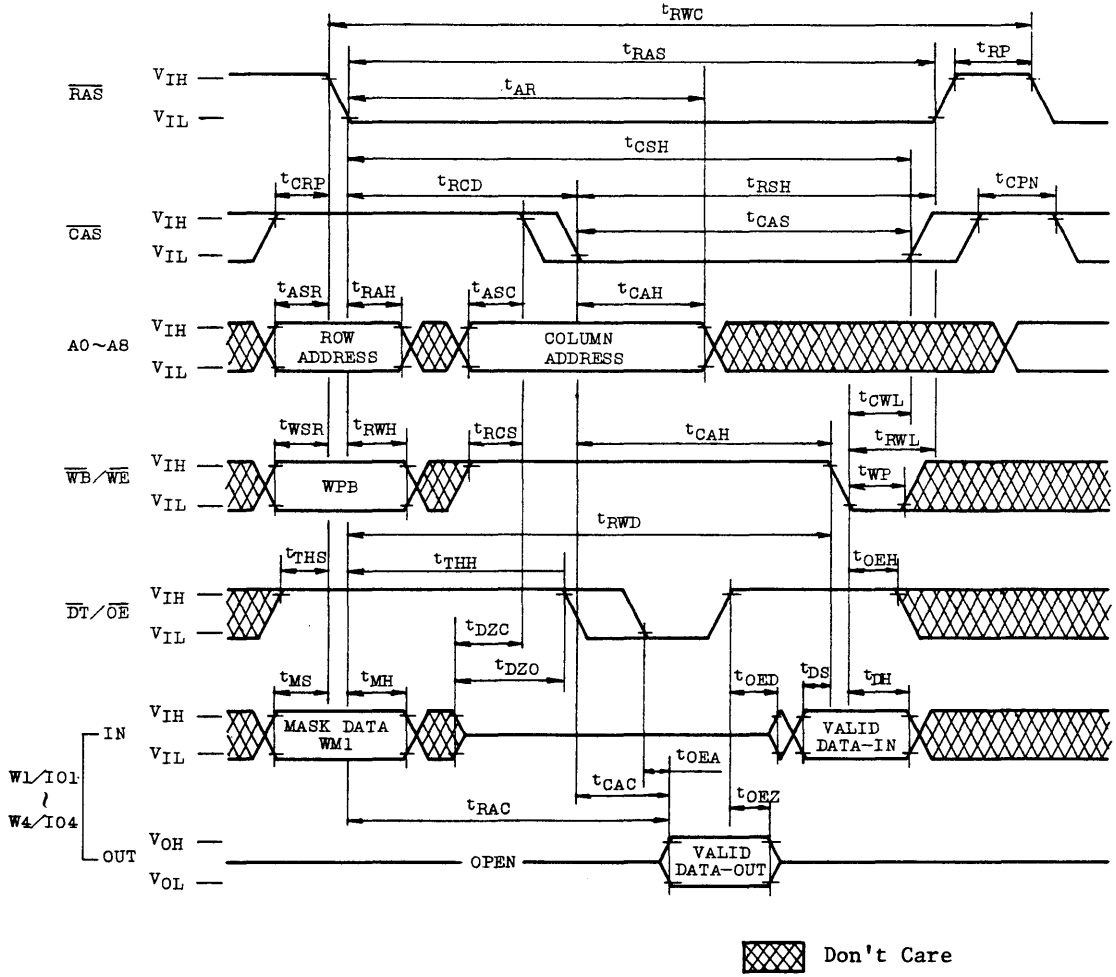
WRITE CYCLE (EARLY WRITE)



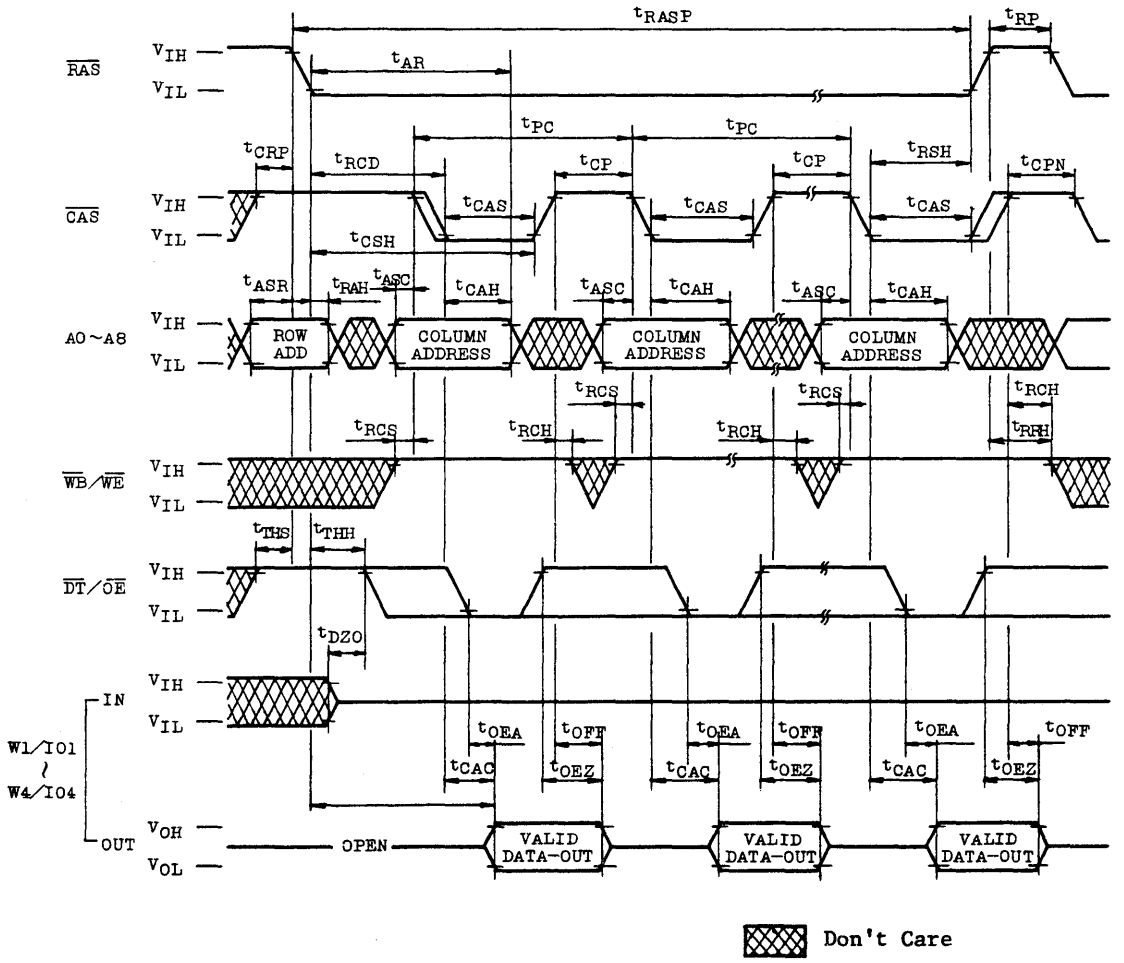
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



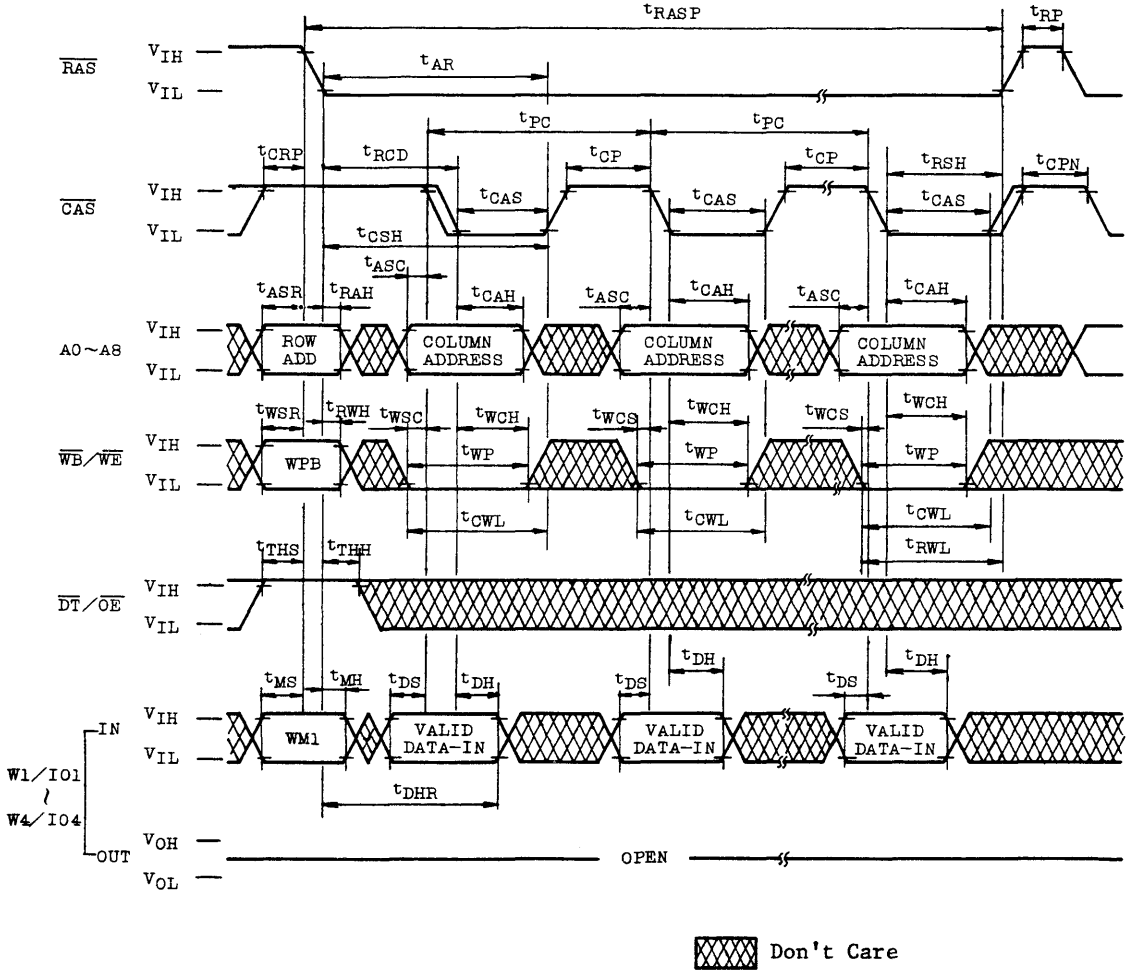
READ-WRITE/READ-MODIFY-WRITE CYCLE



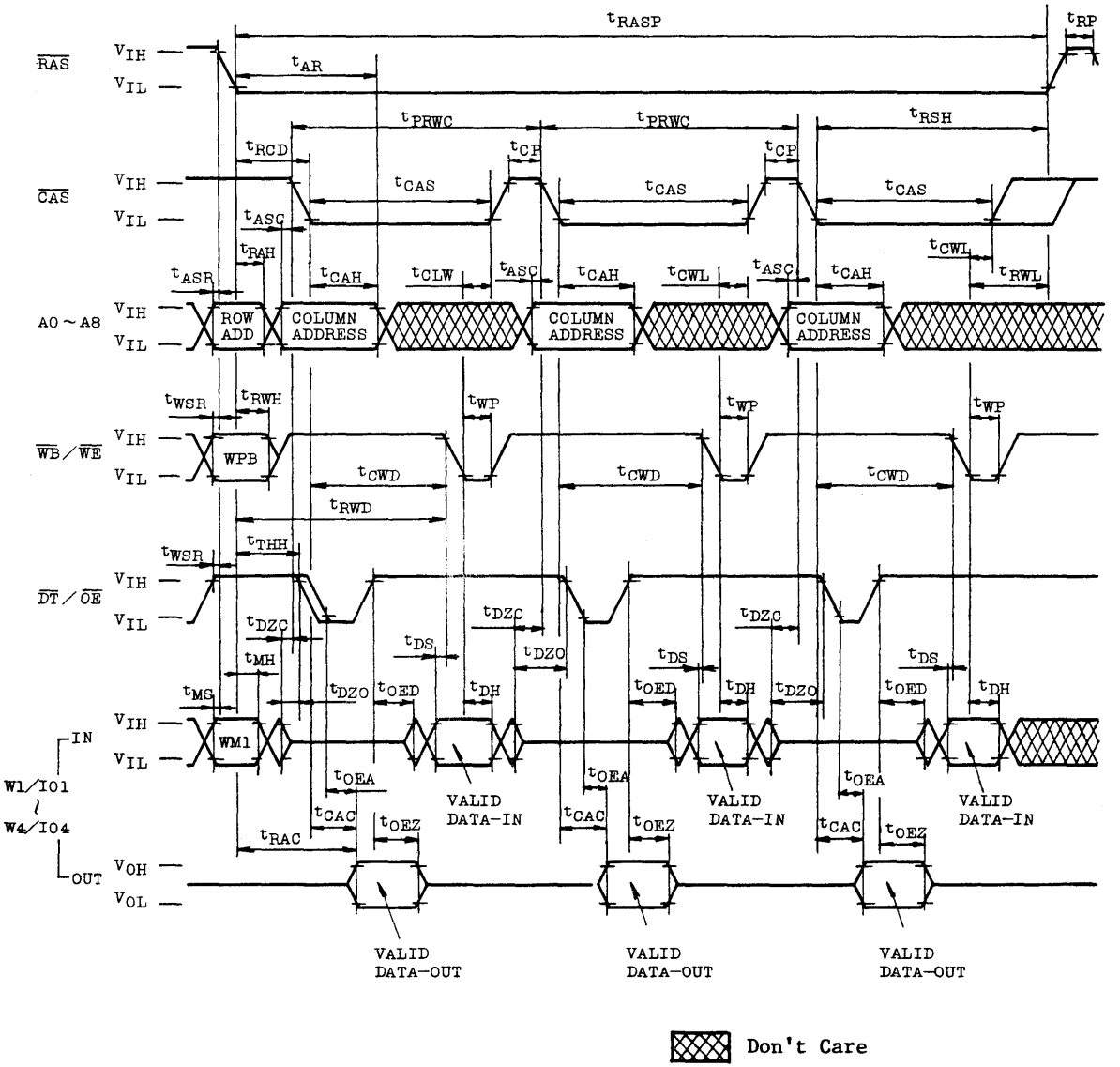
PAGE MODE READ CYCLE



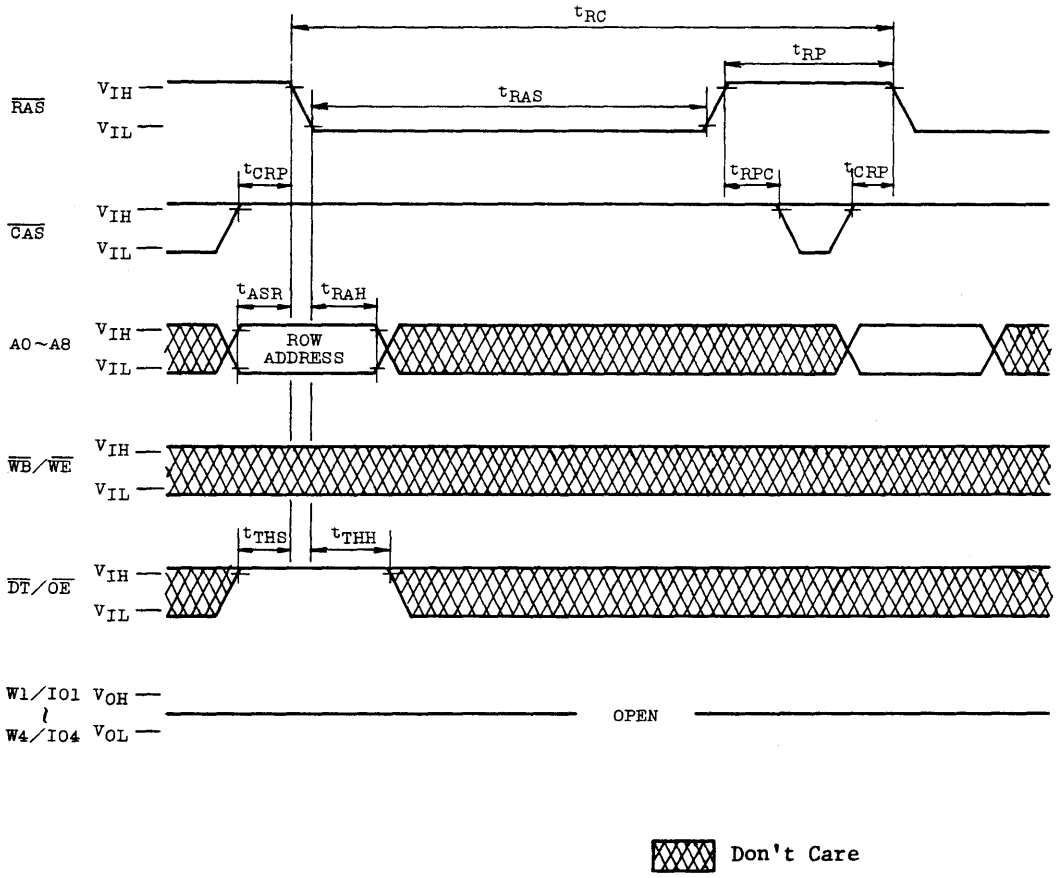
PAGE MODE WRITE CYCLE (EARLY WRITE)



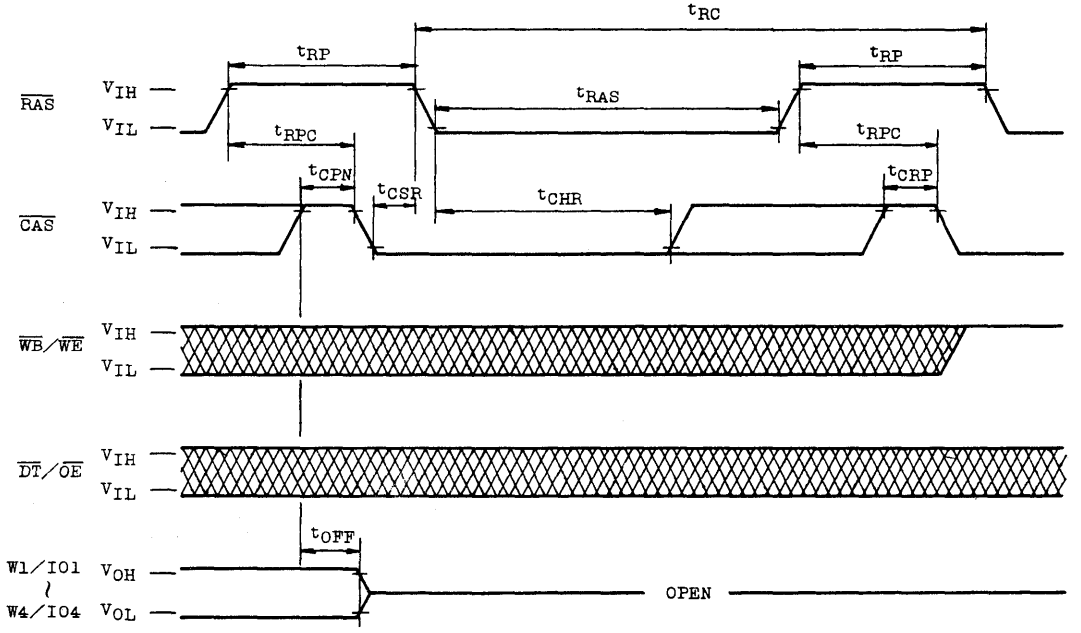
PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



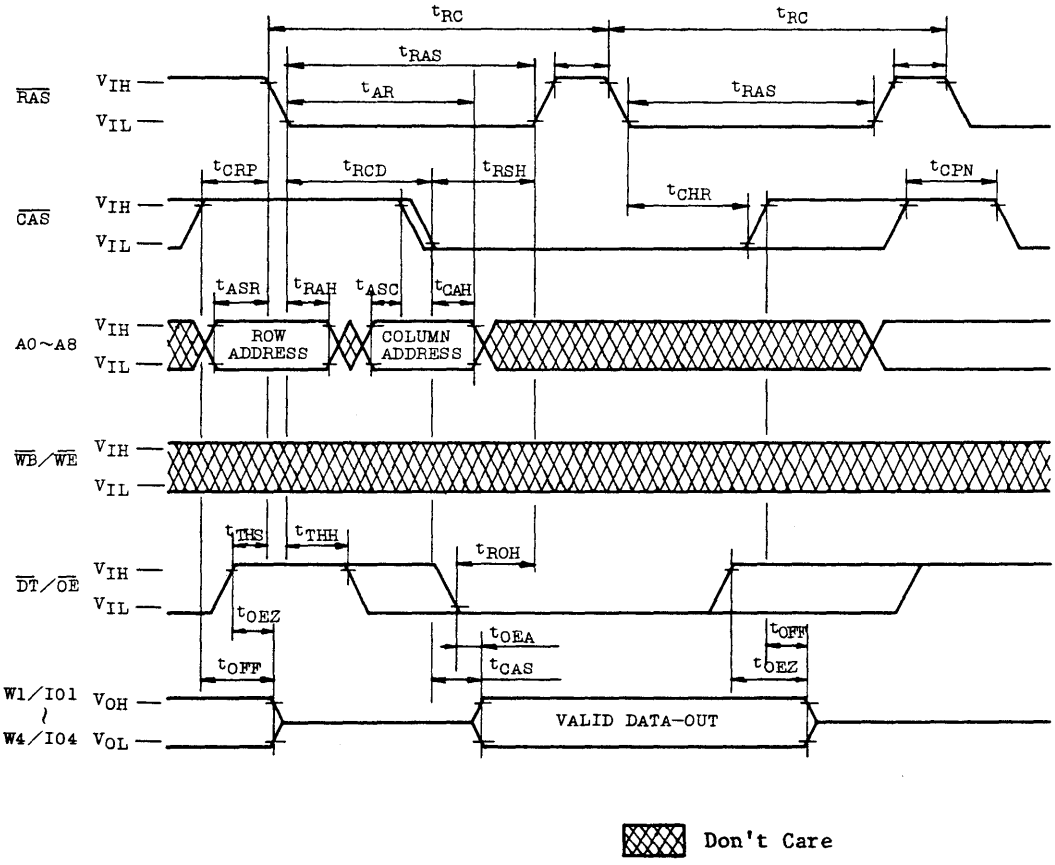
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



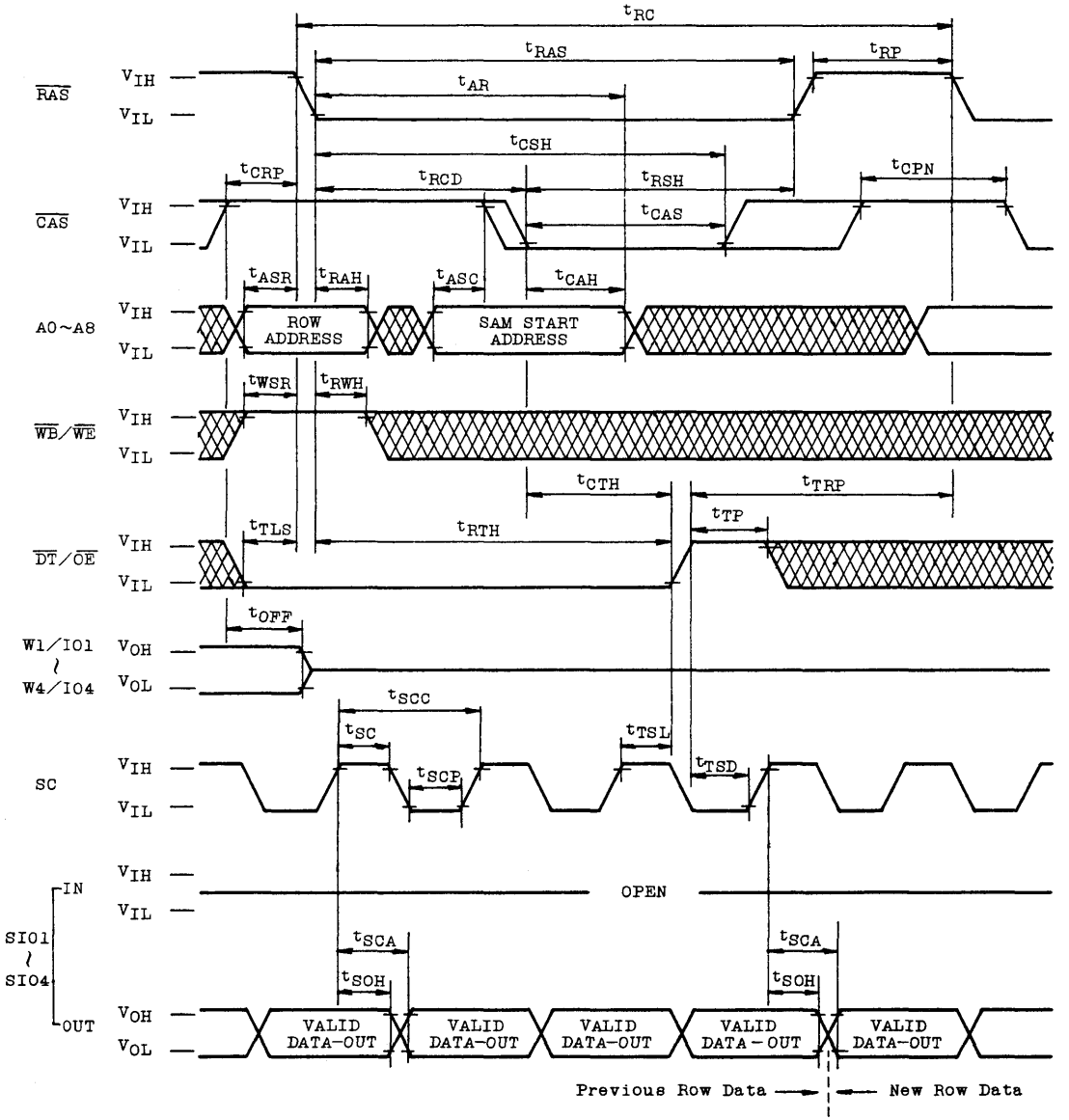
Note: A0 ∿ A8=Don't Care

Don't Care

HIDDEN REFRESH CYCLE



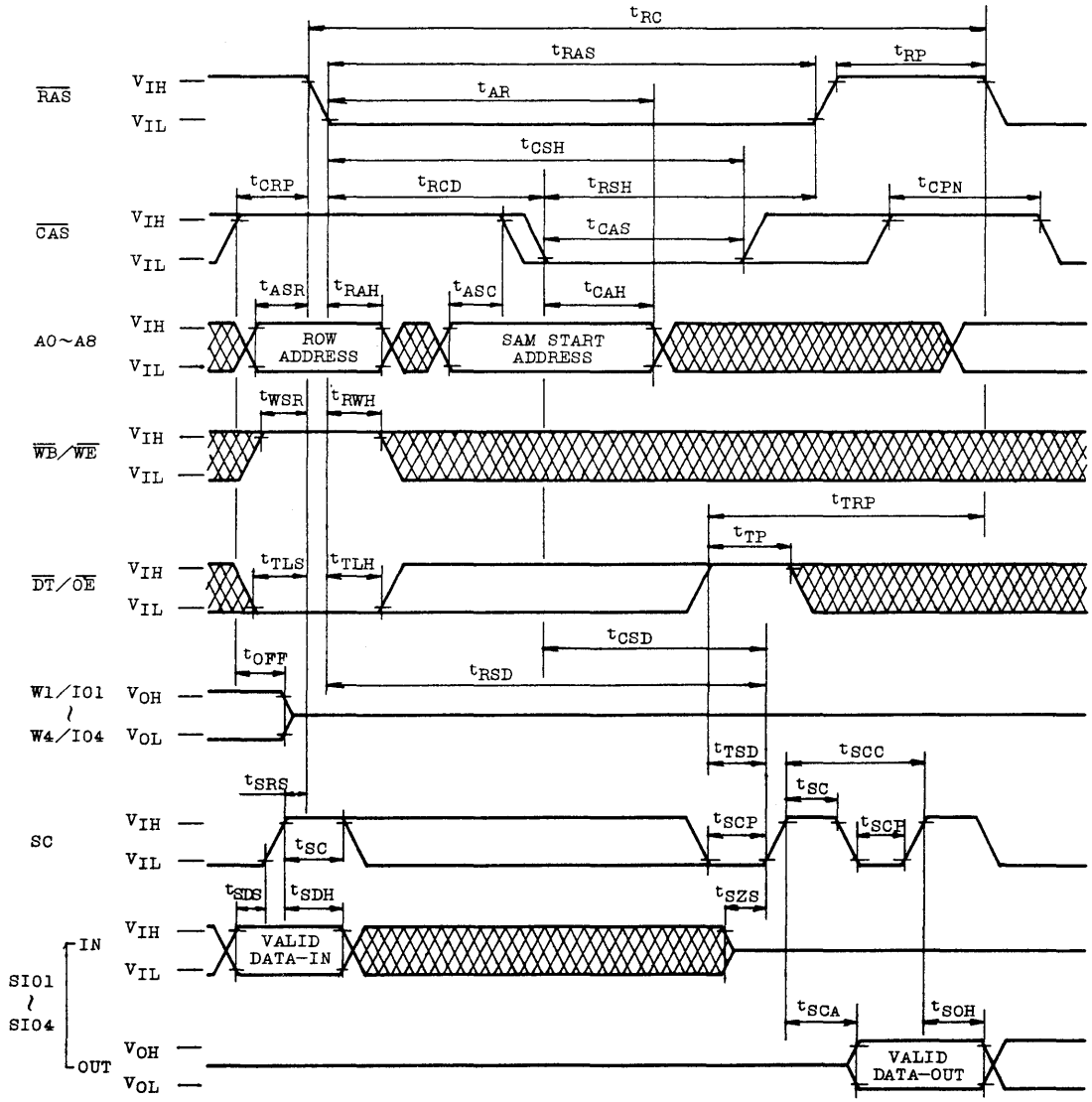
REAL TIME READ TRANSFER CYCLE



Note: $\overline{SE}=V_{IL}$

Don't Care

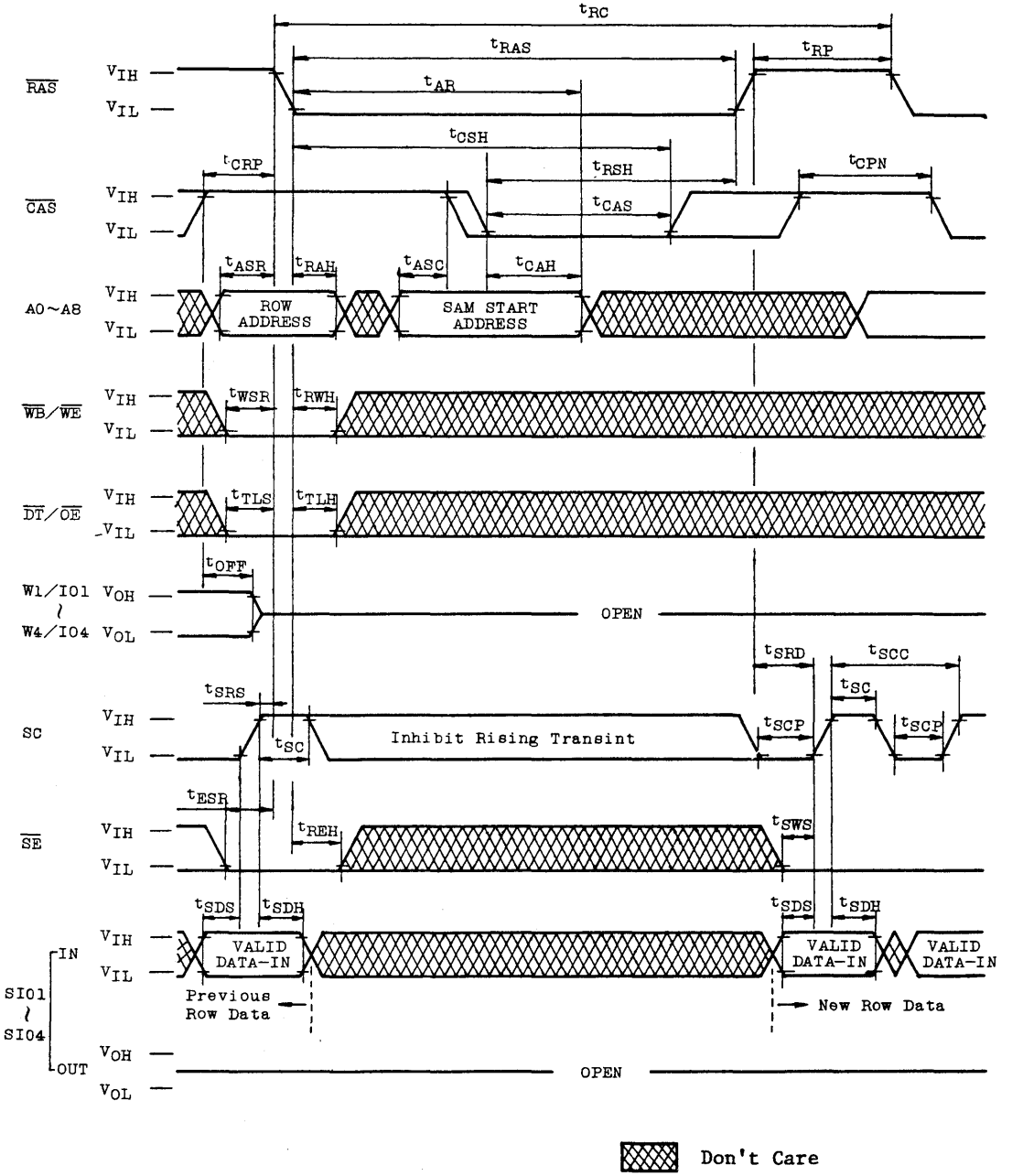
READ TRANSFER CYCLE (Previous transfer is write transfer)



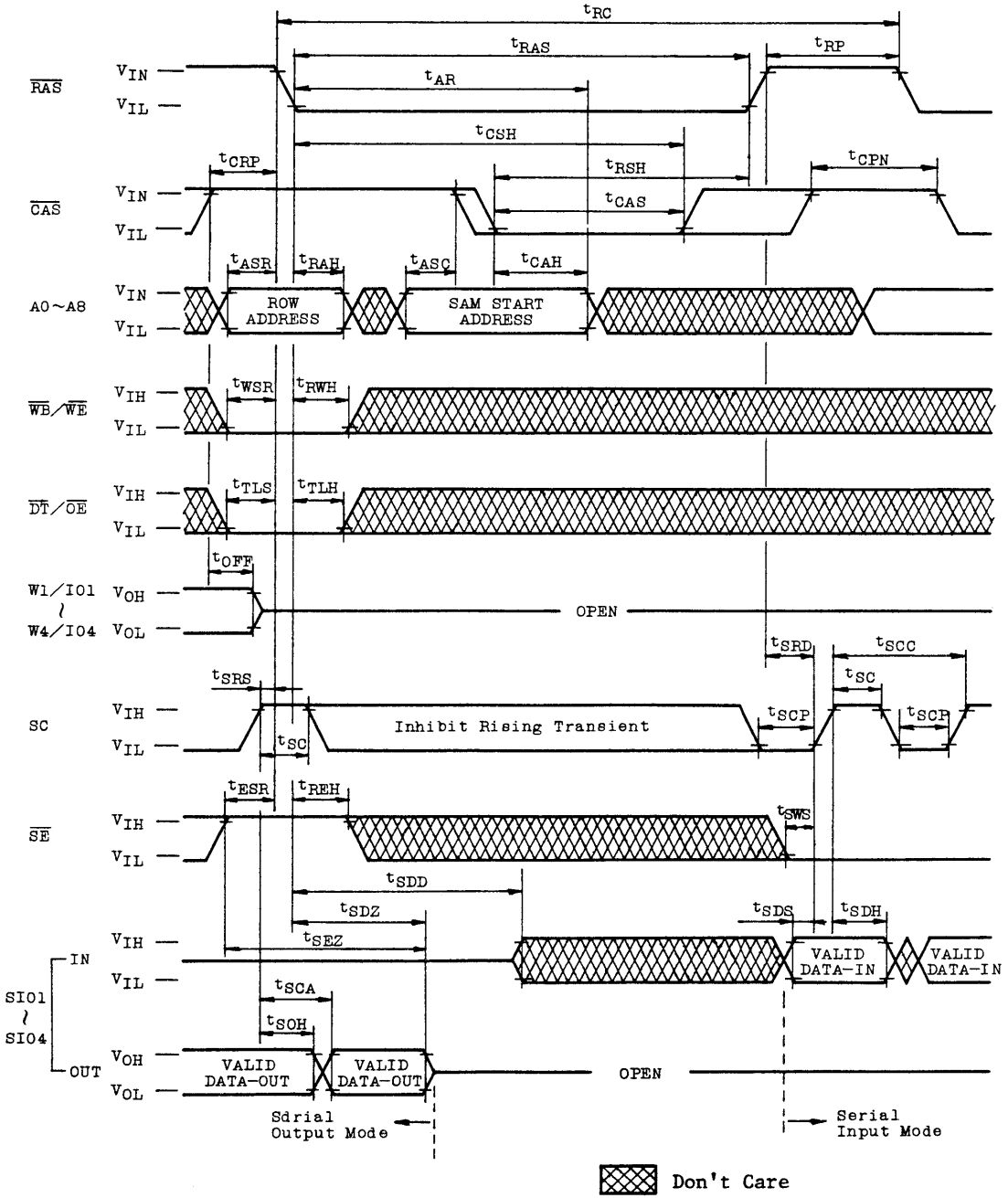
Note: $\overline{SE}=V_{IL}$

Don't Care

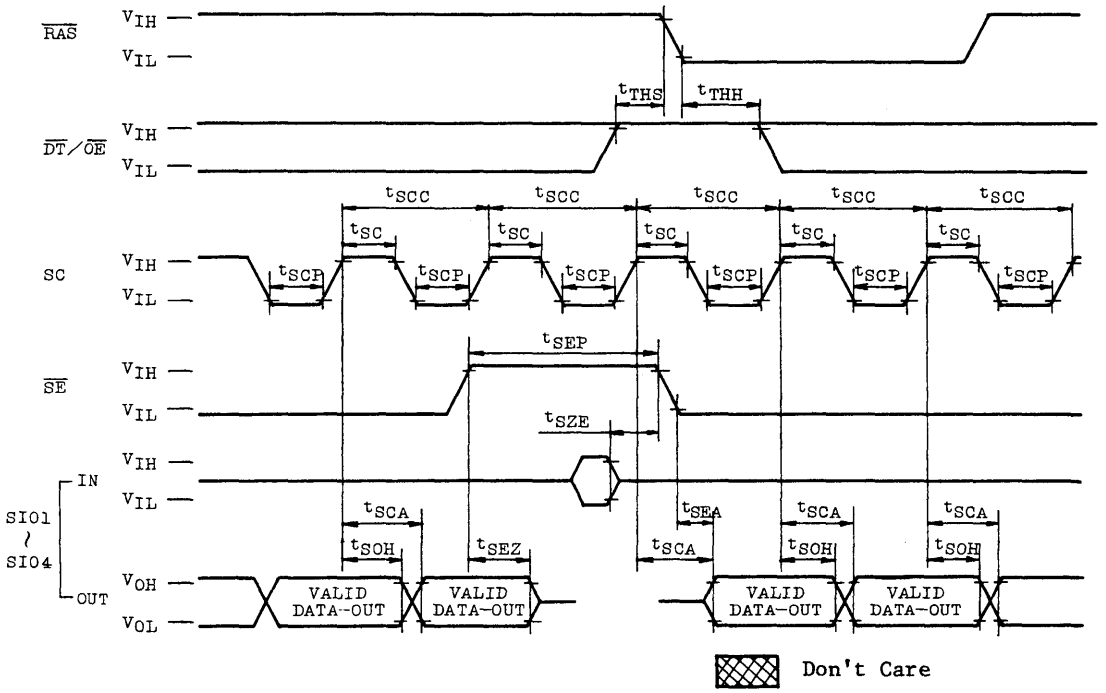
WRITE TRANSFER CYCLE



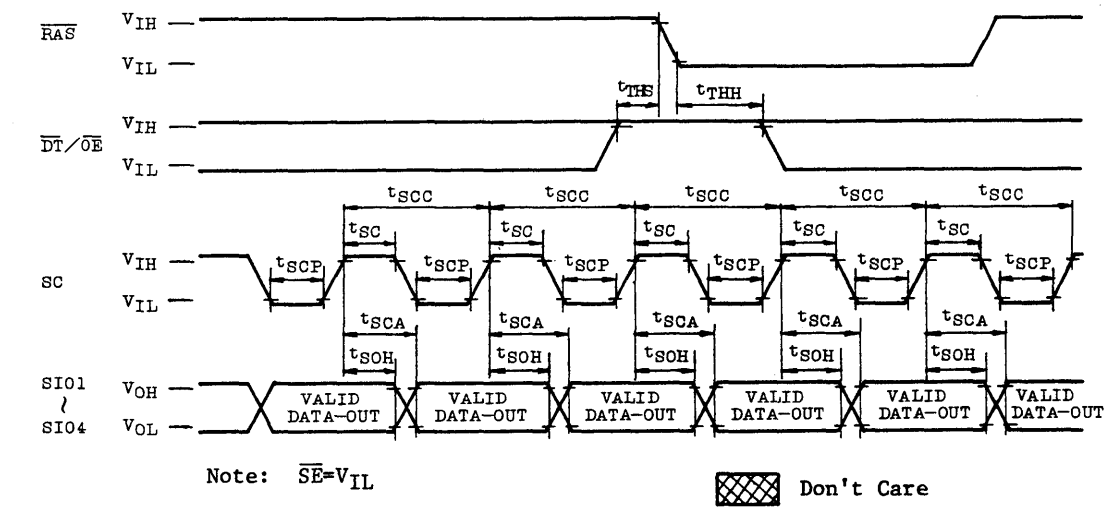
PSEUDO WRITE TRANSFER CYCLE



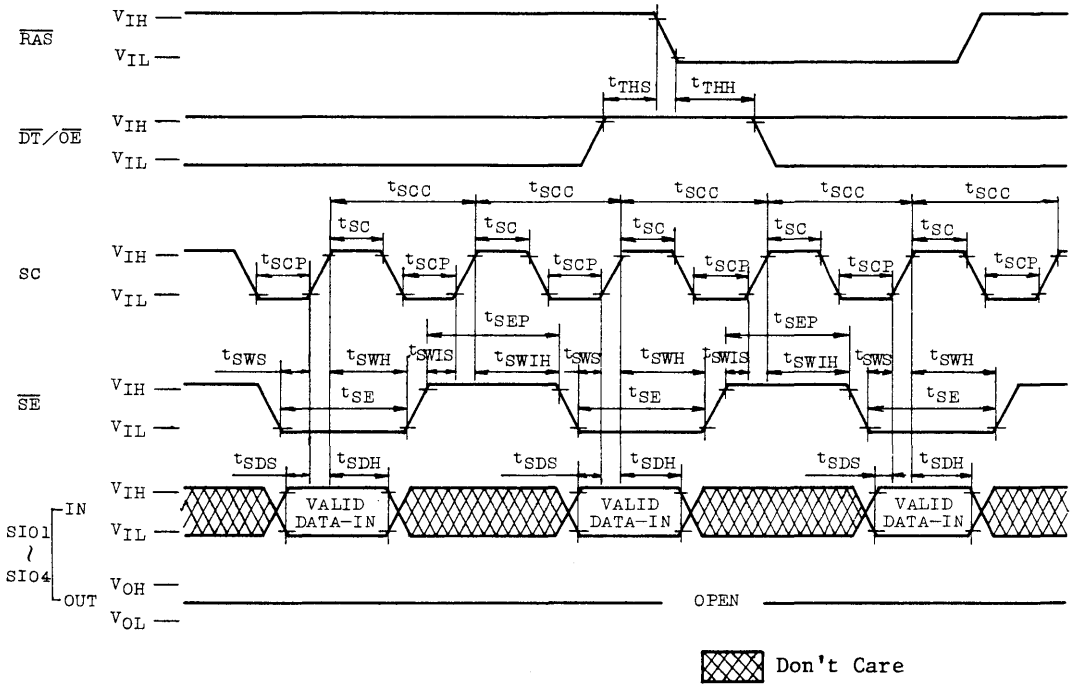
SERIAL READ CYCLE ($\overline{SE}$ CONTROLLED OUTPUTS)



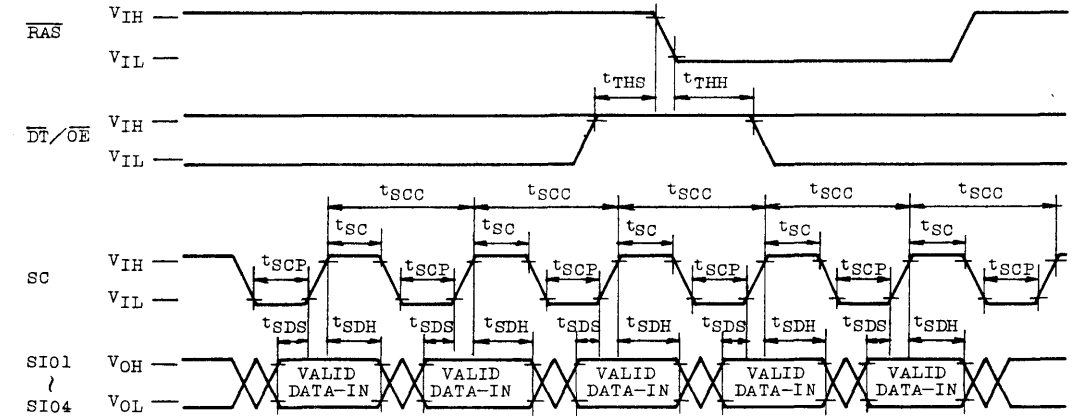
SERIAL READ CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ CONTROLLED WRITE)



SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})

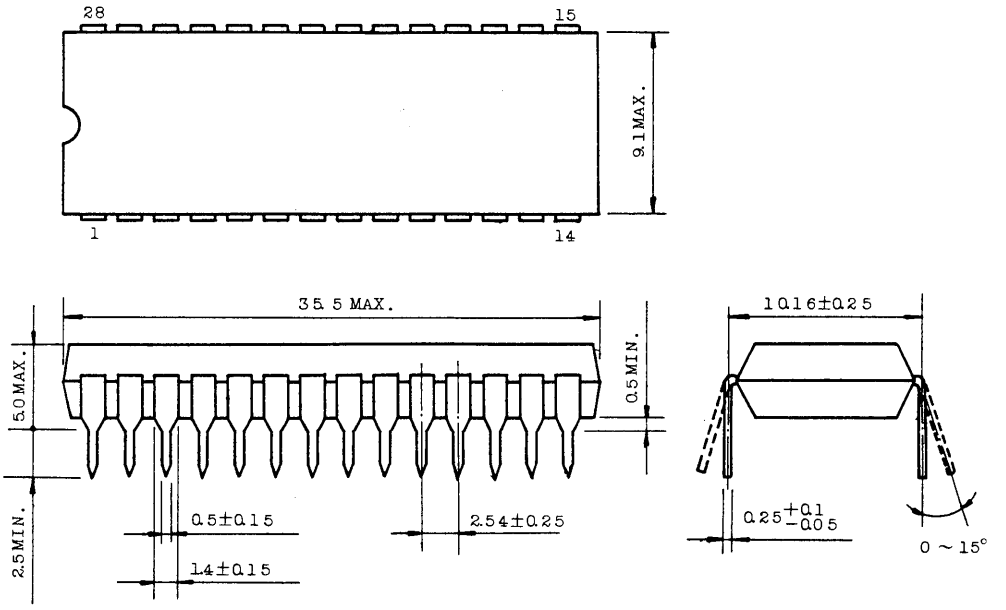


Note: SE=V_{IL}

OUTLINE DRAWINGS

• Plastic DIP

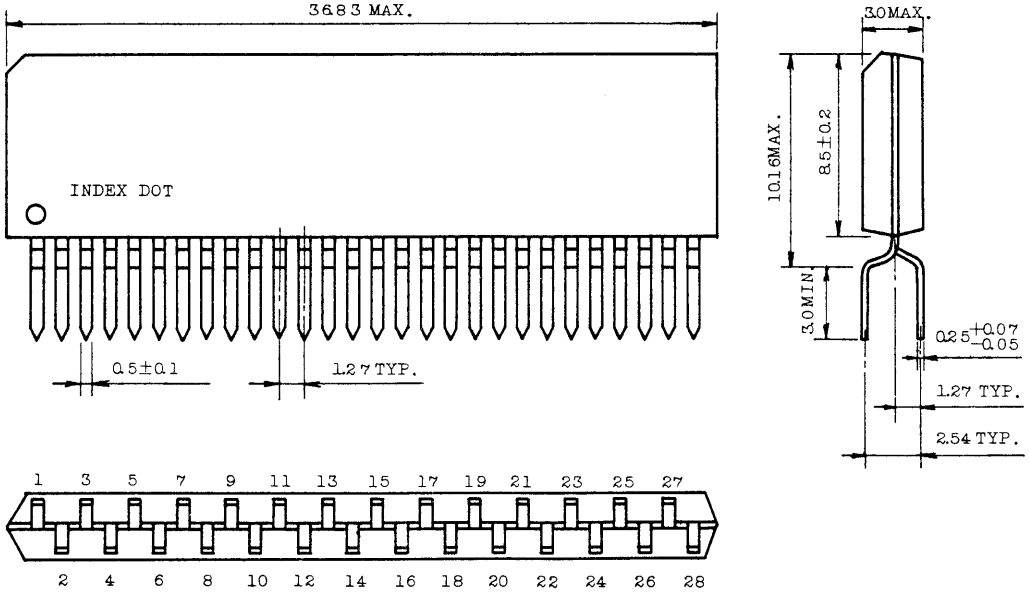
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC524256J-10
TC524256J-12

PRELIMINARY

DESCRIPTION

The TC524256J is a CMOS Multiport memory equipped with a 262,144-word × 4 bit dynamic random access memory(RAM) port and a 512-word × 4 bit static serial access memory(SAM) port. In addition to the conventional DRAM operation modes, the TC524256J features a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

The TC524256J is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplixed address inputs and a common input/output organization allow the TC524256J to be housed in a standard 32-pin, 400-mil wide plastic SOJ.

System oriented featrues include a single 5V±10% power supply operation and compatibility with high performance schottky TTL logic.

FEATURES

ITEM		TC524256J -10	TC524256J -12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time(Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	60mA	55mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	40mA	35mA
I_{CC2}	RAM/SAM Standby Current	3mA	

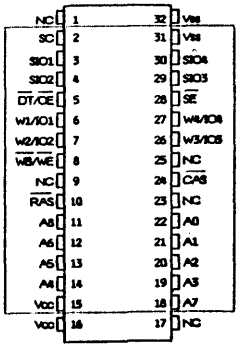
- Organization
  RAM port: 262,144 words × 4 bits
  SAM port: 512 words × 4 bits
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, Page mode, Write-Per-Bit, Read transfer, Write transfer, Serial read, Serial Write capability
- All inputs and outputs TTL compatible
- 512 refresh cycle/8ms
- Package TC524256J: 0.4 inches 32 pins standard Plastic SOJ

PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
W1/IO1 ∿ W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1 ∿ SIO4	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

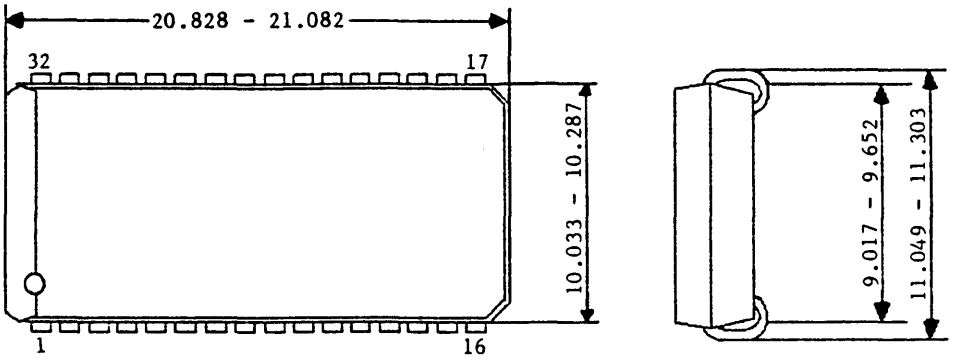
Plastic SOJ

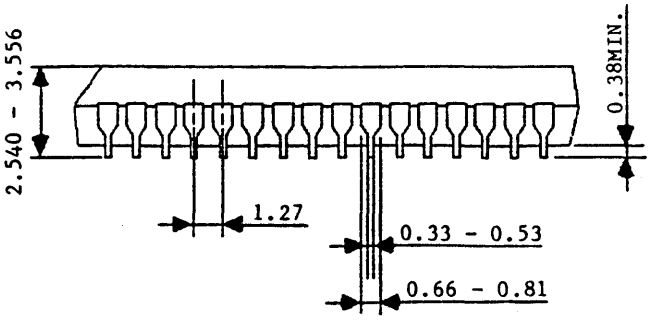


OUTLINE DRAWINGS

• Plastic SOJ

Unit in mm





Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

262,144 WORDS×4 BITS MULTIPORT DYNAMIC RAM
SILICON GATE CMOS

TC524257P/Z-10, TC524257P/Z-12

PRELIMINARY

DESCRIPTION

The TC524257P/Z is a CMOS Multiport memory equipped with a 262,144-word x 4 bit dynamic random access memory (RAM) port and a 512-word x 4 bit static serial access memory (SAM) port. In addition to the conventional DRAM operation modes, the TC524257P/Z features a logic function and a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

The TC524257P/Z is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplexed address inputs and a common input/output organization allow the TC524257P/Z to be housed in a standard 28-pin, 400-mil wide plastic DIP and 400-mil height ZIP. System oriented features include a single 5V ± 10% power supply operation and compatibility with high performance schottky TTL logic.

FEATURES

ITEM		TC524257P/Z	
		−10	−12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time (Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	60mA	55mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	40mA	35mA
I_{CC2}	RAM/SAM Standby Current	3mA	

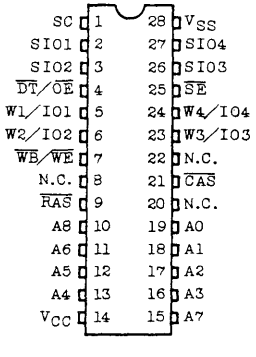
- Organization
  RAM port: 262,144 words x 4 bits
  SAM port : 512 words x 4 bits
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, Page mode, Write-Per-Bit, Raster operation, Read transfer, Write transfer, Serial read, Serial write capability
- All inputs and outputs TTL compatible
- 512 refresh cycle/8ms
- Package TC524257P: 0.4 inches 28 pins standard Plastic DIP
  TC524257Z: 0.4 inches 28 pins standard Plastic ZIP

PIN NAMES

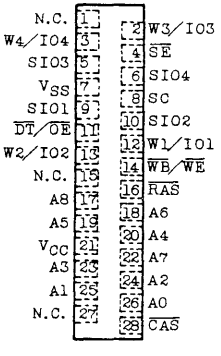
A0 ~ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
W1/I01 ~ W4/I04	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SI01 ~ SI04	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

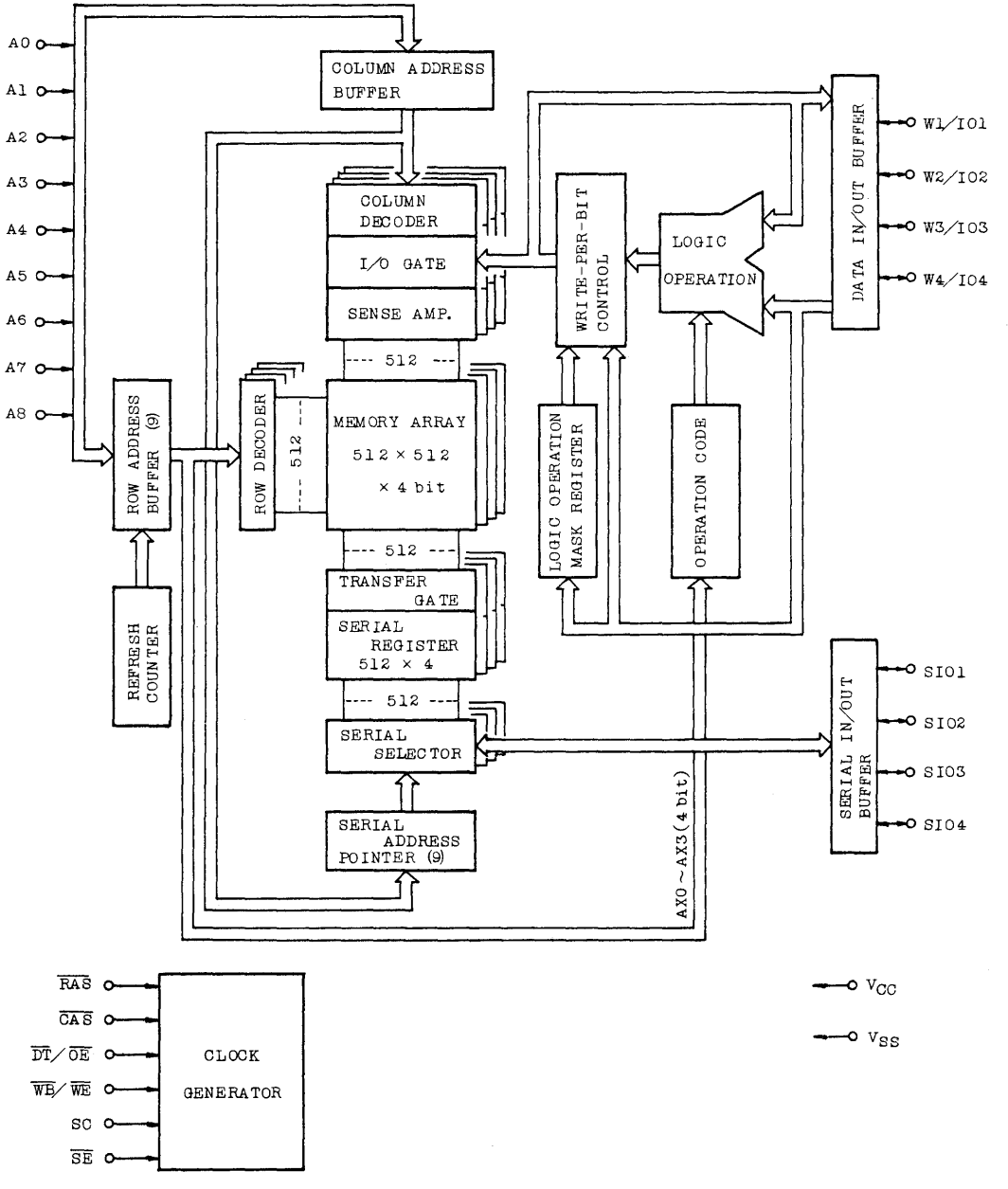
Plastic DIP



Plastic ZIP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN} V_{OUT}	Input Output Voltage	-1.0 ∿ 7.0	V	1
V_{CC}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{opr}	Operating Temperature	0 ∿ 70	°C	1
T_{stg}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITION ($Ta=0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $Ta=0 \sim 70°C$)

SYMBOL	ITEM (RAM Port)	SAM Port	TC524257P/Z-10		TC524257P/Z-12		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
I_{CC1}	OPERATING CURRENT	Standby	-	60	-	55	mA	3,4
I_{CC1A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	Active	-	100	-	90		3,4
I_{CC2}	STANDBY CURRENT	Standby	-	3	-	3	mA	
I_{CC2A}	($\overline{RAS}$, $\overline{CAS}=V_{IH}$)	Active	-	40	-	35		3,4
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT	Standby	-	60	-	55	mA	3
I_{CC3A}	($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	Active	-	100	-	90		3,4
I_{CC4}	PAGE MODE CURRENT	Standby	-	50	-	45	mA	3,4
I_{CC4A}	($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling: $t_{PC}=t_{PC}$ MIN.)	Active	-	90	-	80		3,4
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT	Stadnby	-	60	-	55	mA	3
I_{CC5A}	($\overline{CAS}$ Before $\overline{RAS}$ Cycling:$t_{RC}=t_{RC}$ MIN.)	Active	-	100	-	90		3,4
I_{CC6}	DATA TRANSFER CURRENT	Standby	-	60	-	55	mA	3
I_{CC6A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	Active	-	100	-	90		3,4

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNITS	NOTES
$I_{I(L)}$	INPUT LEAKAGE CURRENT ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test=0V)	-10	0	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (Output is disabled, $0V \leq V_{OUT} \leq 5.5V$)	-10	0	10	μA	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE (Wi/IOi, SIOi .... $I_{OUT}=-5mA$)	2.4	-	-	V	
V_{OL}	OUTPUT LOW LEVEL VOLTAGE (Wi/IOi, SIOi .... $I_{OUT}=+4.2mA$)	-	-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (NOTES 5, 6, 7)

SYMBOL	PARAMETER	TC524257P/Z-10		TC524257P/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{RWC}	Read-Write Cycle Time	250		290			
t_{PC}	Page Mode Cycle Time	90		105			
t_{PRWC}	Page Mode Read-Write Cycle Time	150		175			
t_{RAC}	Access Time from $\overline{RAS}$		100		120		8,14
t_{CAC}	Access Time from $\overline{CAS}$		50		60		8,14
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90			
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000		
t_{RSH}	$\overline{RAS}$ Hold Time	50		60			
t_{CSH}	$\overline{CAS}$ Hold Time	100		120			
t_{CAS}	$\overline{CAS}$ Pulse Width	50		60			
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	60		
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20			
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode)	30		35			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		15			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	20		25			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	70		85			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10			11
t_{WCH}	Write Command Hold Time	20		25			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	70		85			
t_{WP}	Write Command Pulse Width	20		25			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35			
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	20		25			12
t_{RASP}	$\overline{RAS}$ Pulse Width (Page Mode)	190	100,000	225	100,000		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION (Continued)

SYMBOL	PARAMETER	TC524257P/Z-10		TC524257P/Z-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	70		85		ns	
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	125		150			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	75		90			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		25		30		
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	20	0	25		10
t_{OED}	$\overline{OE}$ to Data Input Delay Time	20		25			
t_{OEH}	$\overline{OE}$ Command Hold Time	20		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	20		20			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	20		20			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{CPT}	$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	40		50			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	10		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	10		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	10		15			
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	80		95			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	30		35			
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0			
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	10		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	80		90			
t_{RP}	$\overline{DT}$ Prechaege Time	30		35			
t_{RSD}	$\overline{RAS}$ to First $\overline{SC}$ Delay Time (Read Transfer)	100		120			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION (Continued)

SYMBOL	PARAMETER	TC524257P/Z-10		TC524257P/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CSD}	$\overline{CAS}$ to First SC Dealy Time (Read Transfer)	50		60		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		10			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		20			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		40			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		30			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		60			
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	60		10
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SCC}	SC Cycle Time	30		40			
t_{SC}	SC Pulse Width (SC High Time)	10		15			
t_{SCP}	SC Precharge Time (SC Low Time)	10		15			
t_{SCA}	Access Time from SC		25		35		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	20		30			
t_{SEA}	Access Time from $\overline{SE}$		25		35		9
t_{SE}	$\overline{SE}$ Pulse Width	25		35			
t_{SEP}	$\overline{SE}$ Precharge Time	25		35			
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	30		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	5		10			
t_{SEH}	Serial Write Enable Hold Time	15		20			
t_{SWIS}	Serial Write Disable Set-Up Time	5		10			
t_{SWIH}	Serial Write Disable Hold Time	15		20			

RASTER OPERATION WRITE CYCLE

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (NOTES 5, 6, 7)

SYMBOL	PARAMETER	TC524257P/Z-10		TC524257P/Z-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{FRC}	Write Cycle Time	220		260		ns	15
t_{FRWC}	Read-Write Cycle Time	280		330			15
t_{FPC}	Page Mode Write Cycle Time	120		145			15
t_{FPRWC}	Page Mode Read-Write Cycle Time	180		215			15
t_{FRAS}	$\overline{RAS}$ Pulse Width	130		160			15
t_{FRSH}	$\overline{RAS}$ Hold Time	80		100			15
t_{FCSH}	$\overline{CAS}$ Hold Time	130		160			15
t_{FCAS}	$\overline{CAS}$ Pulse Width	80		100			15
t_{FRWL}	Write Command to $\overline{RAS}$ Lead Time	60		75			15
t_{FCWL}	Write Command to $\overline{CAS}$ Lead Time	60		75			15

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$)	-	5	
C_{IO1}	Input/Output Capacitance (WI/IO1 ∿ W4/IO4)	-	7	
C_{IO2}	Input/Output Capacitance (SIO1 ∿ SIO4)	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltage are referenced to V_{SS}.

3. These parameters depend on cycle rate.

4. These parameters depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.

9. SAM port outputs are measured with a load equivalent to 2 TTL loads and 50pF.

10. t_{OFF}(max.), t_{OEZ}(max.) t_{SDZ}(max.) and t_{SEZ}(max.) define the time at which the output achieve the open circuit condition and are not referenced to output voltage levels.

11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in read-write cycles.

13. t_{WCS}, t_{RWD} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.) and $t_{CWD} \geqq t_{CWD}$(min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

14. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

15. These parameters are applied to the write cycles with raster operation using logic function expect for "THROUGH", "ZERO", "ONE" and "INV1".

DEVICE INFORMATION

RAM PORT OPERATION

Operation Truth Table

All operation modes of TC524257P/Z are determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, and $\overline{SE}$ at the falling edge of $\overline{RAS}$. They are shown in the following tabel 1.

Table 1: Functional Truth Table

$\overline{RAS}$	$\overline{CAS}$	ADDRESS	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION
H	H	*	*	*	*	Standby
↓	H	Valid	H→L	H	*	Read
	H	Valid	H	H→L	*	Write
	H	Valid(Row add.)	H	*	*	$\overline{RAS}$ only refresh
	L	*	H(1)	H	*	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
	H	Valid	H	L	*	Write-per-Bit
	L	Valid(A0∿A3)	H(1)	L	*	Raster Operation Set-up
	H	Valid	L	H	*	Read Transfer
	H	Valid	L	L	L	Write Transfer
	H	Valid	L	L	H	Pseudo-Write Transfer

Note; H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

(1) The input level of $\overline{DT}/\overline{OE}$ in the $\overline{CAS}$ before $\overline{RAS}$ timing is not ristricted. However it is recommended that $\overline{DT}/\overline{OE}$ be held 'High' because this input will be used for future expansion of the operation mode.

ADDRESSING

The 18 address bits required to decode 4-bits of the 1,048,576 cell locations within the Dynamic RAM memory array of the TC524257P/Z, are multiplexed onto 9 address input pins (A0∿A8). Nine row-address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

The row address inputs AX0∿AX3 are also used as operation code input signals in the raster operation set-up cycle.

DATA TRANSFER/OUTPUT ENABLE ($\overline{DT}/\overline{OE}$)

The $\overline{DT}/\overline{OE}$ input is a multifucntion pin. When $\overline{DT}/\overline{OE}$ is 'High' at the falling edge of $\overline{RAS}$, a normal DRAM cycle is performed and this input is used as an output enable. When $\overline{DT}/\overline{OE}$ is 'Low' at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE-PER-BIT/WRITE-ENABLE ($\overline{WB}/\overline{WE}$)

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. For conventional DRAM cycle, the $\overline{WB}/\overline{WE}$ input is used in the same manner as standard DRAMs except when the write-per-bit function or the raster operation are used. When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the bit write-mask is enabled. When $\overline{WB}/\overline{WE}$ and $\overline{CAS}$ are 'low' at the falling edge of $\overline{RAS}$, the raster operation set-up cycle is executed.

The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the DRAM memory array and the serial register. When $\overline{WB}/\overline{WE}$ is 'high' at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read-transfer cycle). When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write-transfer cycle).

WRITE-MASK DATA/DATA INPUT/OUTPUT (W1/IO1 to W4/IO4)

When the write-per-bit function is enabled, the mask data on the W1/IO1 pins is latched into the write-mask register WM1 at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic '1'. Writing is inhibited on data lines where the write-mask data is a logic '0'. The write-mask data is valid for only one cycle except for during raster operation. In the raster operation set-up cycle, the mask data is latched into the write-mask register WM2 at the falling edge of $\overline{RAS}$. The write-mask selected during the raster operation set-up cycle remains valid for all subsequent raster operation write, read-modify-write or page-mode write cycles.

PAGE MODE

The page mode feature of the TC524257P/Z allows data to be transferred into or multiple column locations of the same row by having multiple column cycles during a single active $\overline{RAS}$ cycle.

For the initial page mode access, the output data is valid after the specified access time from $\overline{RAS}$. For all subsequent page mode read operations, the ouptut data is valid after the specified access time from $\overline{CAS}$. As a result, page mode operation reduces power dissipation and improves data access time.

When the write-per-bit function is enabled, the mask data specified in the first write operation, at the falling edge of $\overline{RAS}$, is maintained throughout the page mode write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM cycle requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with '$\overline{RAS}$-ONLY' cycles.

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH

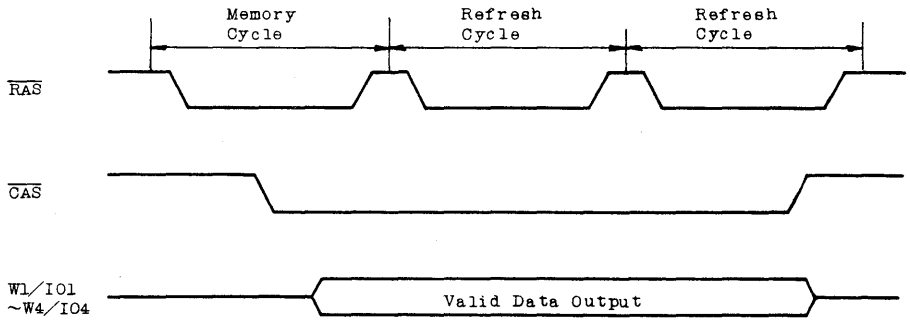
The TC524257P/Z also offers an internal refresh function. When $\overline{\text{CAS}}$ is held 'low' for a specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes low, an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle. For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$.

During a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle, $\overline{\text{WB}}/\overline{\text{WE}}$ must be 'high' at the falling edge of $\overline{\text{RAS}}$ to prevent a false raster operation set-up cycle from occurring.

HIDDEN REFRESH

A hidden refresh is a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh performed by holding $\overline{\text{CAS}}$ 'low' from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{\text{RAS}}$ after the specified $\overline{\text{RAS}}$-precharge period (refer to figure 1).

Figure 1: hidden refresh cycle



WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/IOi pins, their corresponding write circuits are disabled and new data will not be wirtten.

When a '1' is sensed on any of the Wi/IOi pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in table 2.

Table 2: Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	Wi/IOi (i=1∿4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in figures 2 and 3.

Figure 2: write-per-bit timing cycle

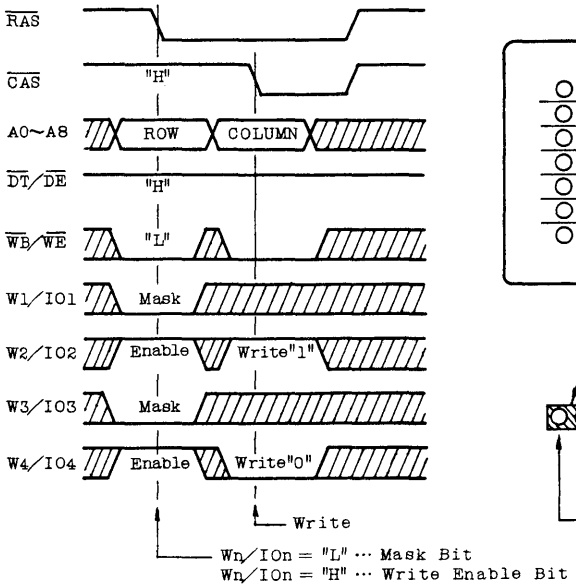
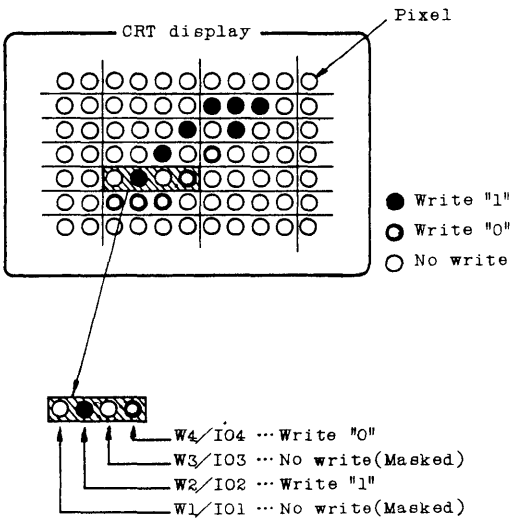
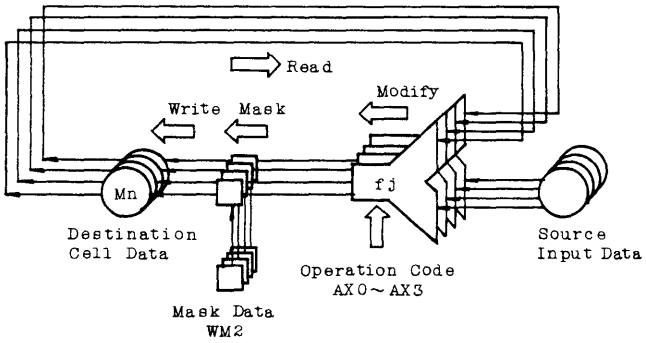


Figure 3: corresponding bit-map



RASTER OPERATION

The TC524257P/Z features a logic function which provides 16 modes of raster operation. The desired logic function mode is selected during the raster operation set-up cycle and remains in effect until another selection is made. During raster operation, the TC524257P/Z performs internal logic operations when data is written through the RAM port. As shown in figure 4, the result (fj) of the logic operation, between the input data and the data residing in the accessed memory location is stored back in the accessed memory location.



Mn ← fj(Mn, Dn)

fj: Logic Operation (j=0~15)
Mn: Destination Cell Data
Dn: Source Input Data
n: Number of W/IO

Figure 4: block diagram of raster operation

The row address inputs AX0 thru AX3 are used as operation code input signals in the raster operation set-up cycle.

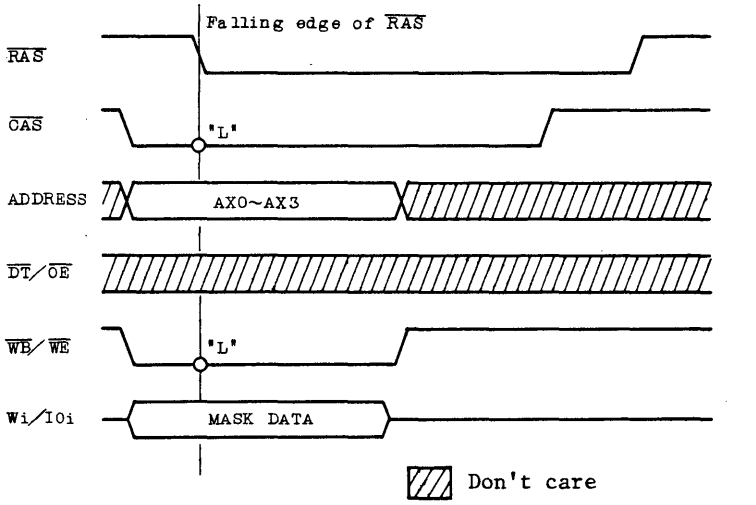
Table 3 lists the operation assigned to the sixteen logic function modes.

Table 3: Truth table of raster operation

Operation Code				Symbol	Operation	Note	Operation Code				Symbol	Operation	Note
AX3	AX2	AX1	AX0				AX3	AX2	AX1	AX0			
0	0	0	0	ZERO	0	*1	1	0	0	0	NOR	$\overline{Dn+Mn}$	*2
0	0	0	1	AND1	$Dn \cdot Mn$	*2	1	0	0	1	ENOR	$\overline{Dn \oplus Mn}$	*2
0	0	1	0	AND2	$\overline{Dn} \cdot Mn$	*2	1	0	1	0	INV1	$\overline{Dn}$	*1
0	0	1	1	INHIBIT	Mn	*2	1	0	1	1	OR2	$\overline{Dn} \cdot Mn$	*2
0	1	0	0	AND3	$Dn \cdot \overline{Mn}$	*2	1	1	0	0	INV2	$\overline{Mn}$	*2
0	1	0	1	*3THROUGH	Dn	*1	1	1	0	1	OR3	$Dn+\overline{Mn}$	*2
0	1	1	0	EOR	$Dn \oplus Mn$	*2	1	1	1	0	NAND	$\overline{Dn \cdot Mn}$	*2
0	1	1	1	OR1	$Dn+Mn$	*2	1	1	1	1	ONE	1	*1

Note: *1 Normal write cycle timing is applied.
*2 Raster operation write cycle timing must be applied.
*3 The 'THROUGH' operation mode allows input data to be written directly into the selected memory location without raster operation. Therefore, 'THROUGH' is used to reset the raster operation.

Figure 5: Raster operation set-up cycle



AX0 ∿ AX3 ..... RASTER OPERATION SELECTION CODE
(16 functions)

MASK DATA ..... RASTER OPERATION MASK DATA
(Wi/IOi=1 ..... Non masked bit)
(Wi/IOi=0 ..... Masked bit)

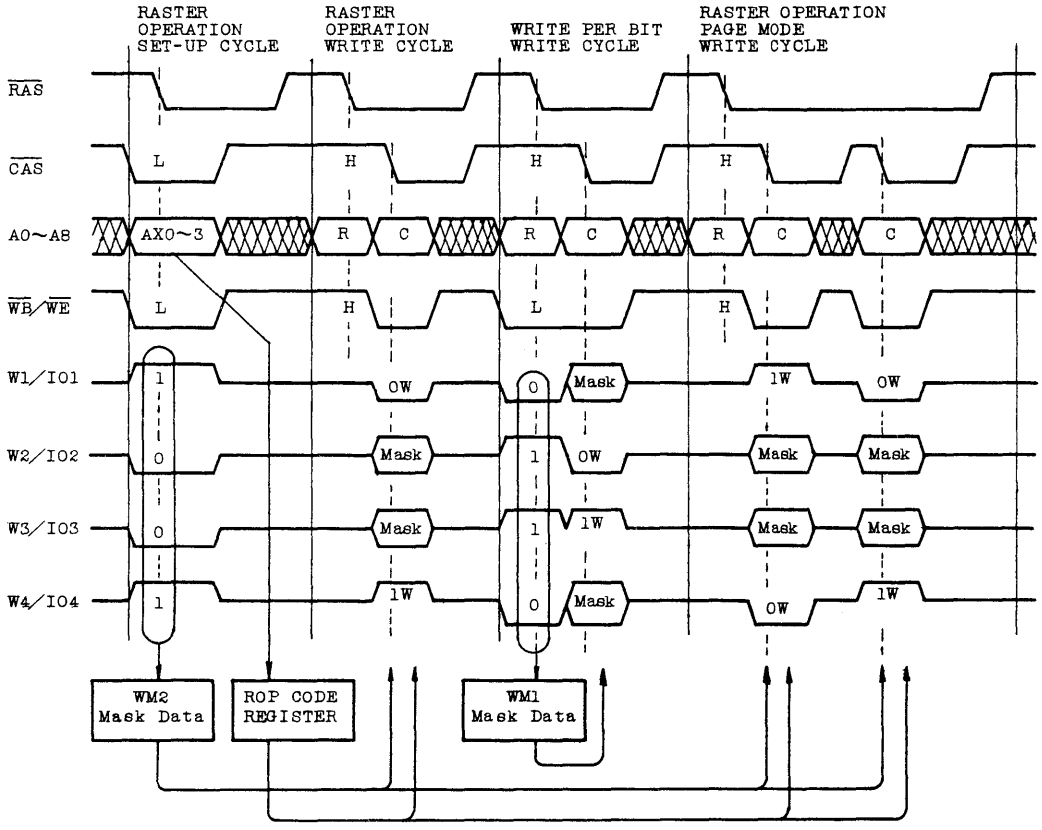
Figure 5 shows the timing diagram for the raster operation set-up cycle.

Both $\overline{CAS}$ and $\overline{WB}/\overline{WE}$ must be low at the falling edge of $\overline{RAS}$. At this point, the operation code specified by row addresses AX0 thru AX3 determines the logic function to be performed and the mask data is latched into the write-mask register WM2. The logic function and mask data specified during the raster operation set-up cycle will remain in effect during all subsequent raster operation cycles, till another raster operation set-up cycle is executed to change the logic operation mode and mask data.

When the 'THROUGH' operation mode is selected, a logic operation is not performed but the mask data specified during the raster operation set-up cycle remains in effect during all subsequent raster operation cycles (persistent write per bit function).

Figure 6 shows an example of raster operation cycles with a write-per-bit cycle mixed in the sequence. During the write-per-bit cycle, the raster operation is inhibited and the mask data in register WM1 is used while the mask data in register WM2 is ignored. In the subsequent raster operation page mode cycle, the raster operation is reactivated and the mask data in register WM2 is used again.

Figure 6: Example of raster operation



TRANSFER OPERATION

The TC524257P/Z features bi-directional transfer capability from RAM to SAM and from SAM to RAM. A transfer consists of loading 512 words by 4-bits of data from one port into the other. During a transfer cycle, RAM port and SAM port operations are restricted.

There are three types of transfer operations: read transfer, write transfer and pseudo-write transfer. As shown in table 4, the type of transfer operation is determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Table 4: Truth table of transfer operation

At the falling edge of $\overline{RAS}$					Transfer direction
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$		
H	L	H	*	Read/real-time read transfer cycle	RAM → SAM
H	L	L	L	Write-transfer cycle	SAM → RAM
H	L	L	H	Pseudo-write transfer cycle	-

*: high or low

READ-TRANSFER CYCLE

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM.

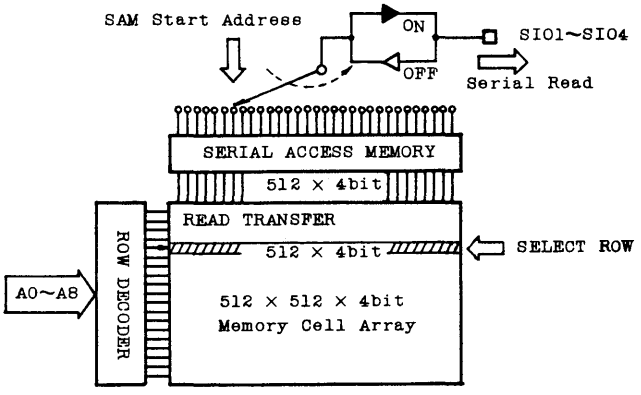
The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$.

When the transfer is completed, the SIO lines are set into the output mode.

In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock(SC) cycle.

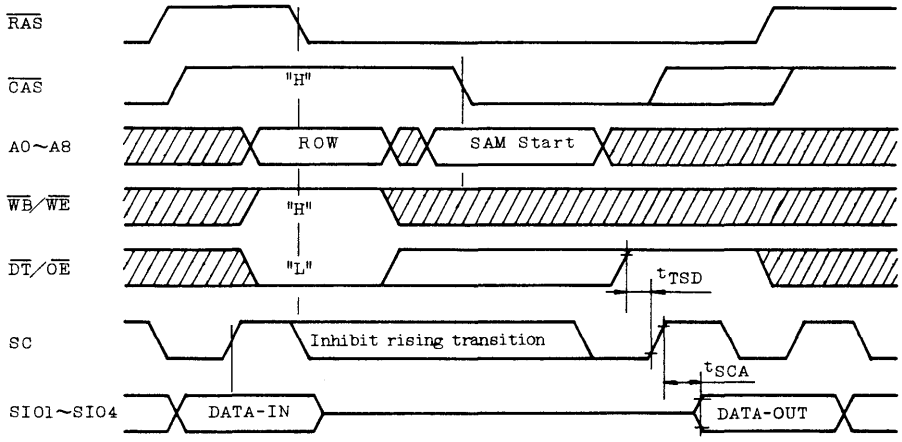
The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$. (refer to figure 7).

Figure 7: block diagram of RAM port and SAM port during read transfer



In a read-transfer cycle (which is preceded by a write-transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ (refer to Figure 8).

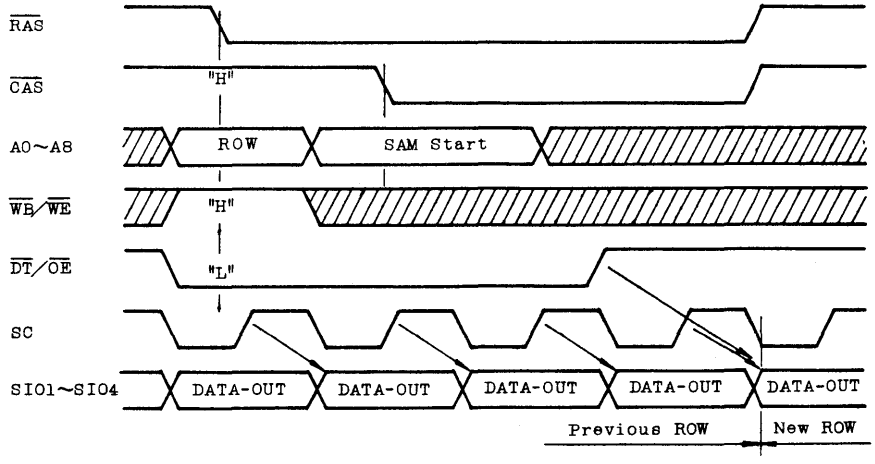
Figure 8: Read-transfer cycle (preceded by a write-transfer cycle)



In a real-time read-transfer cycle (which is preceded by another read-transfer cycle), the previous row data appears on the SIO lines until the specified t_{SCA} access time from the same rising edge of SC.

This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed, without any timing loss. To make this continuous data flow possible: the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (refer to Figure 9).

Figure 9: Real-time read transfer cycle

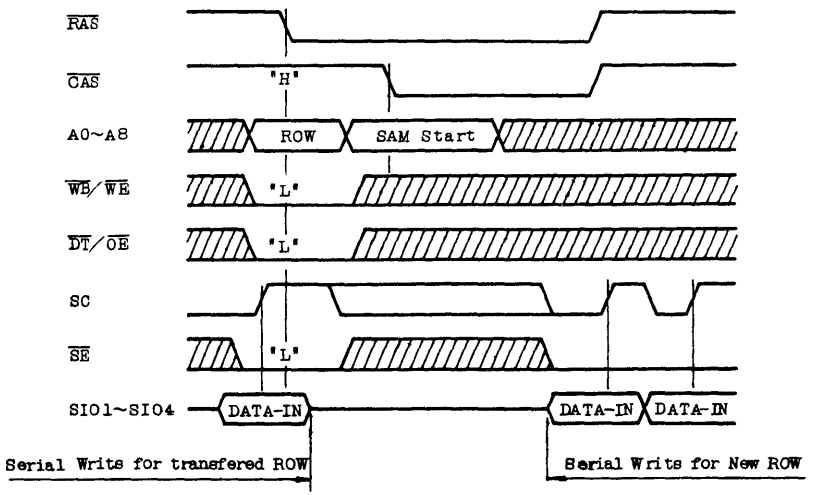


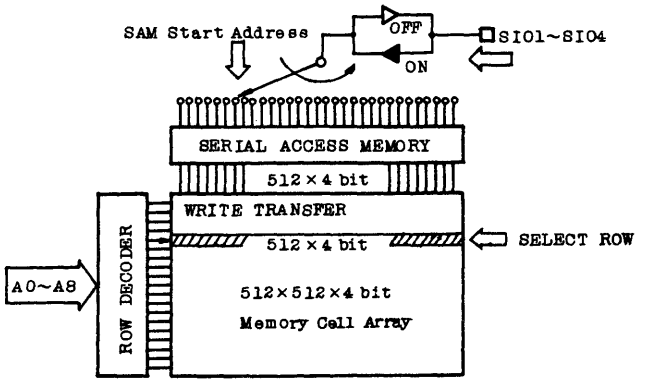
WRITE-TRANSFER CYCLE

A write-transfer cycle consists of loading the content of the SAM data register into a selected row of the RAM array. A write-transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write-transfer is completed, the SIO lines are in the input mode so that serial data synchronized with SC can be loaded.

When two consecutive write-transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SC} has seen satisfied, a rising edge of the SC clock until after a specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to figure 10).

Figure 10: Write-transfer cycle



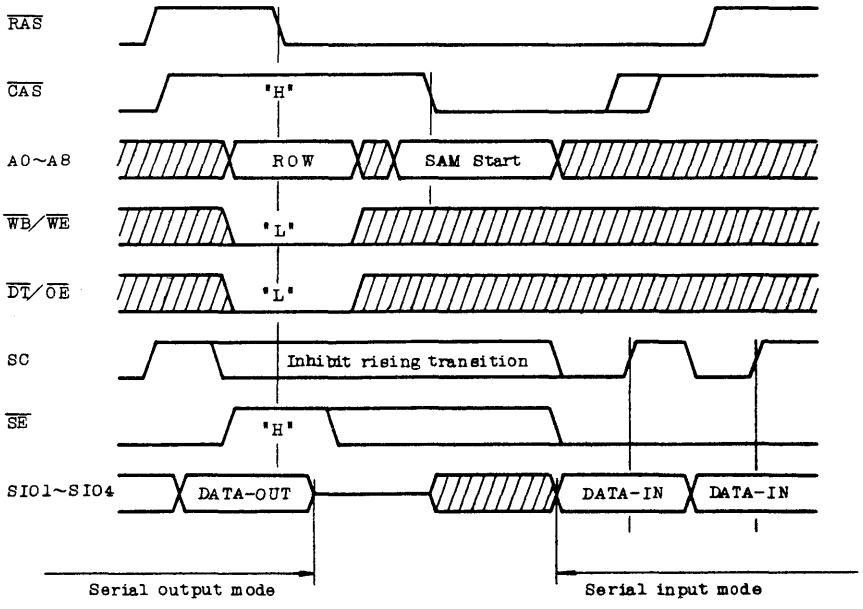


PSEUDO-WRITE-TRANSFER CYCLE

The pseudo-write-transfer cycle switches SIO lines from serial output mode to serial input mode. A pseudo-write-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo-write-transfer cycle must be performed after a read-transfer cycle if the subsequent operation is a write-transfer cycle.

There is a timing delay associated with the switching of the SIO lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to Figure 11).

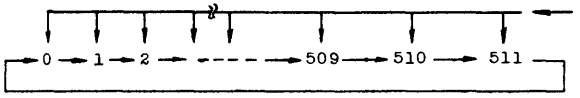
Figure 11: Pseudo-write-transfer cycle



SAM PORT OPERATION

The TC524257P/Z is provided with a 512-word by 4-bit serial access memory (SAM). High-speed read and write operation may be performed through the SAM port independent of the RAM port operations, except during transfer operations. The preceding transfer operation determines the direction of data flow through the SAM registers.

Data may be read out of the SAM port after a read-transfer cycle (RAM→ SAM) has been performed. Data can be shifted out of the SAM port starting at any of the 512-bit locations. This tap location corresponds to the column address selected a the falling edge of $\overline{CAS}$ during the read-transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit.



Tap location determined by column address of read-transfer cycle.

Subsequent real-time-read-transfer may be performed on-the-fly as many times as desired within the refresh constrainst of the DRAM memory array.

A pseudo-write-transfer cycle must be performed in order to write data into the SAM port. This cycle switches the SAM port operation from output mode to input mode. Data is not transferred during a pseudo-write-transfer cycle. A write-transfer cycle (SAM→ RAM) may then be performed. The data in the SAM registers is loaded into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The start address of SAM registers is determined by the column address selected at the falling edge of $\overline{CAS}$.

Table 5: Truth table for SAM operation

Preceding Transfer Cycle	SAM port operation	$\overline{DT}/\overline{OE}$ (at the falling edge of $\overline{RAS}$)	SC	$\overline{SE}$	Function
read-transfer	serial output mode	H*	⎍	L	enable serial read
				H	disable serial read
write-transfer	serial input mode		⎍	L	enable serial write
				H	disable serial write

* When simultaneous operation are being performed on the RAM port and the SAM port, $\overline{DT}/\overline{OE}$ must be held high at the falling edge of $\overline{RAS}$ so as not to perform a false trasnfer cycle.

SERIAL CLOCK (SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial-read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.

The serial clock SC also increments the 9-bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read-transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).

SERIAL ENABLE ($\overline{SE}$)

The $\overline{SE}$ input is used to enable serial access operation. In a serial-read cycle, $\overline{SE}$ is used as an output control. In a serial-write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is high, serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is high.

SERIAL INPUT/OUTPUT (SIO1 ∿ SIO4)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read-transfer cycle is performed, the SAM port is in the output mode. When a pseudo-write cycle is performed, the SAM port operation is switched from output mode to input mode.

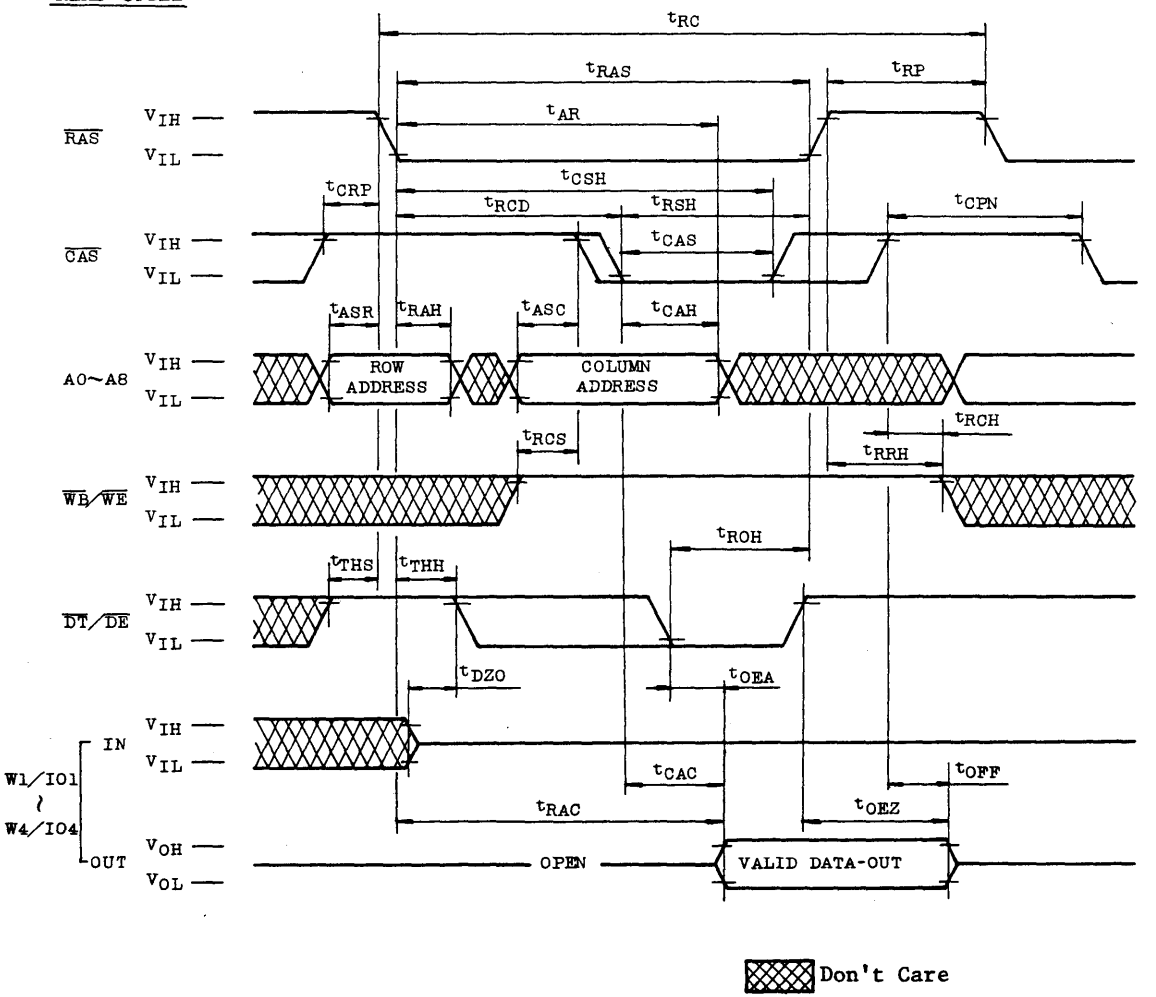
During subsequent write-transfer cycle, the SAM port remains in the input mode.

REFRESH

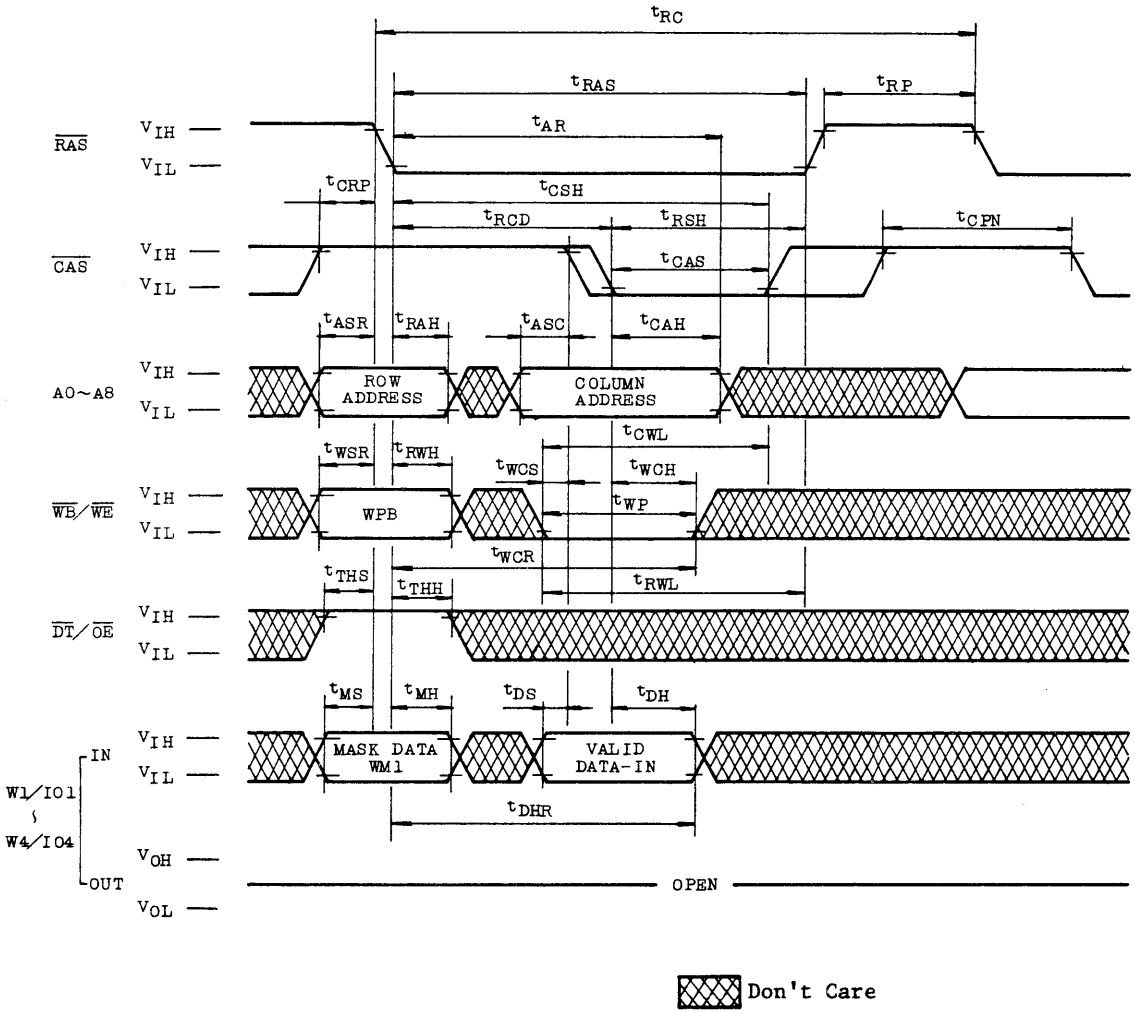
The SAM data registers are static flip-flops therefore a refresh is not required.

TIMING WAVEFORMS

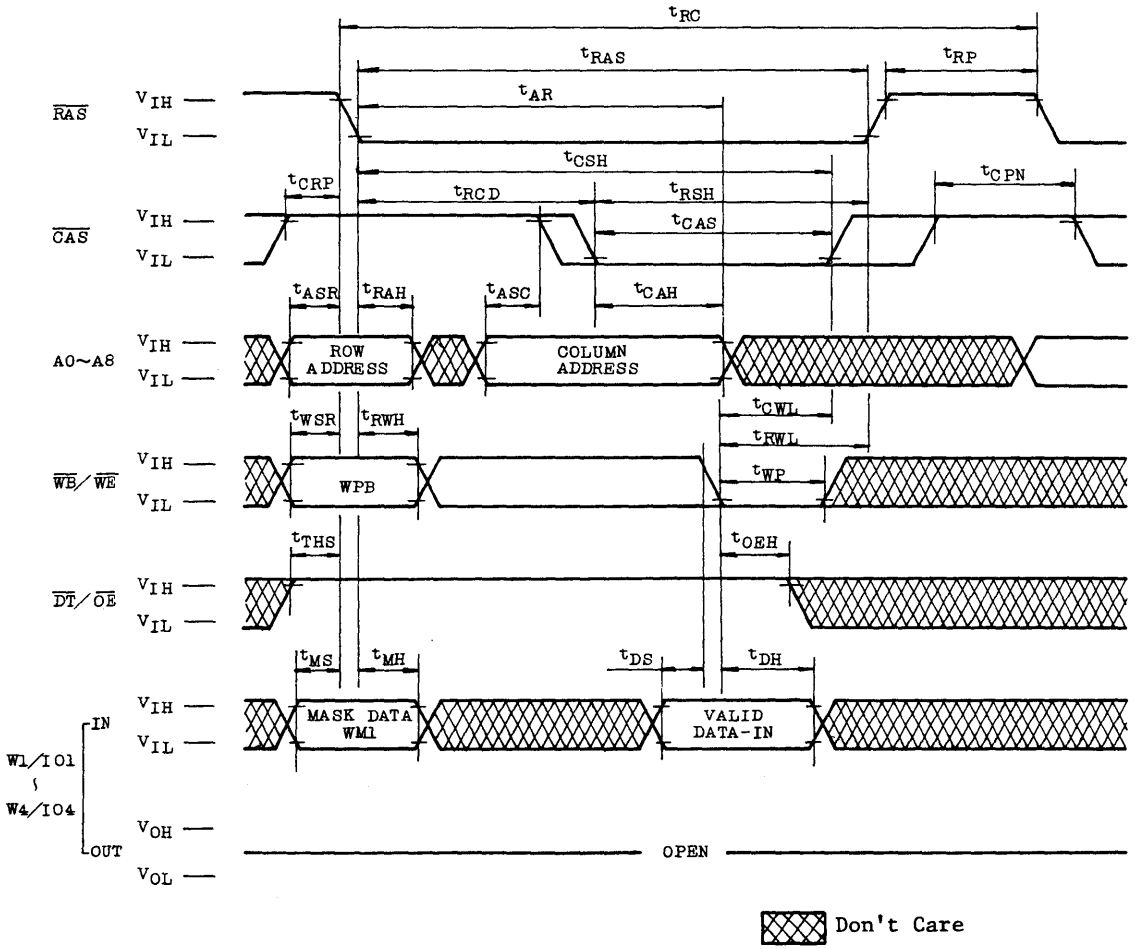
READ CYCLE



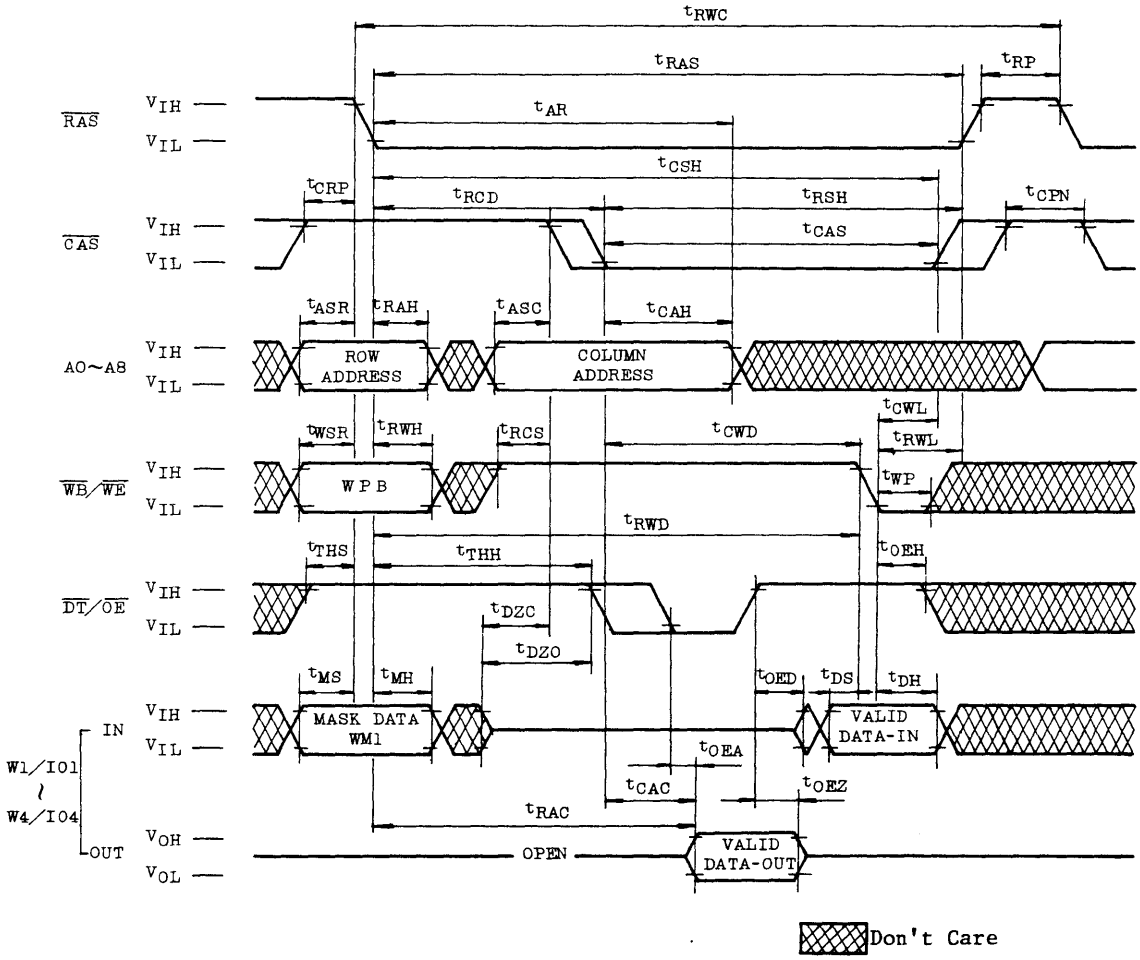
WRITE CYCLE (EARLY WRITE)



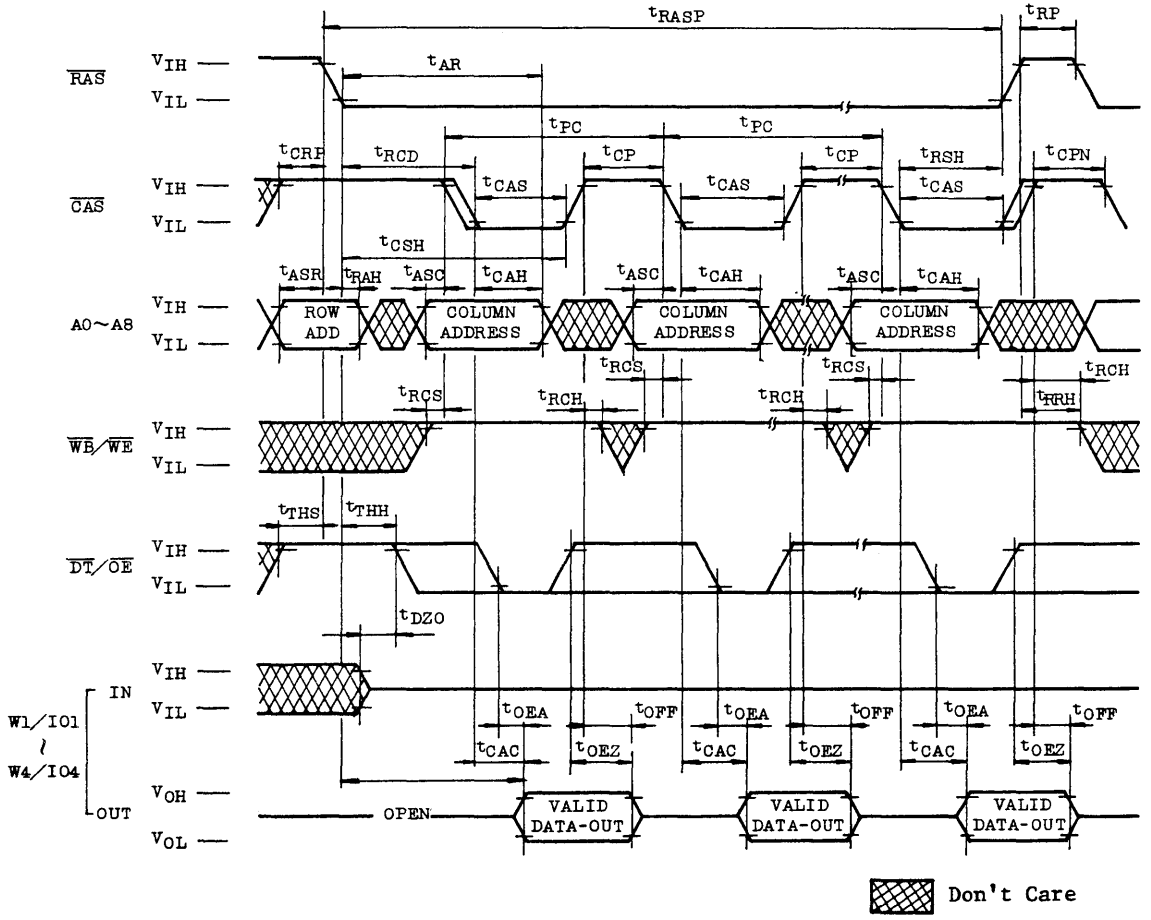
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



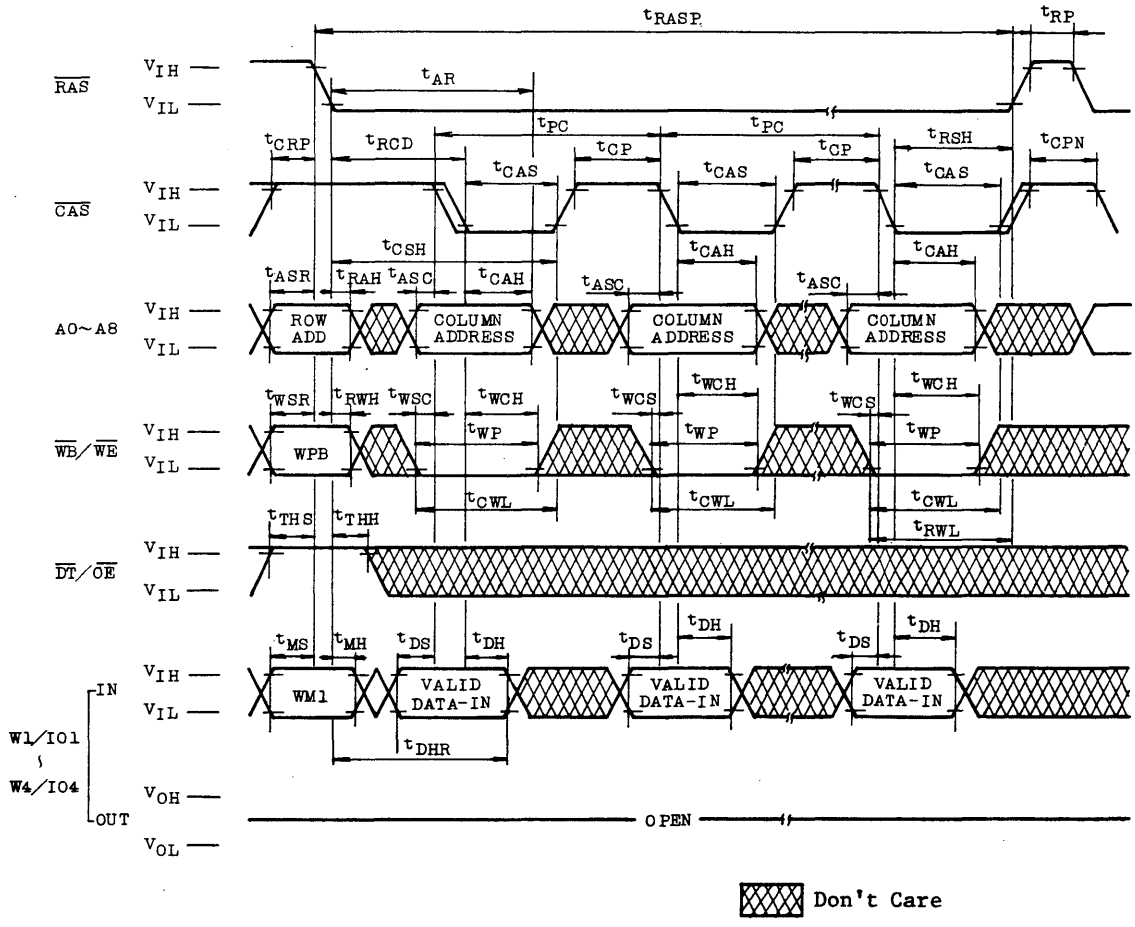
READ-WTITE/READ-MODIFY-WRITE CYCLE



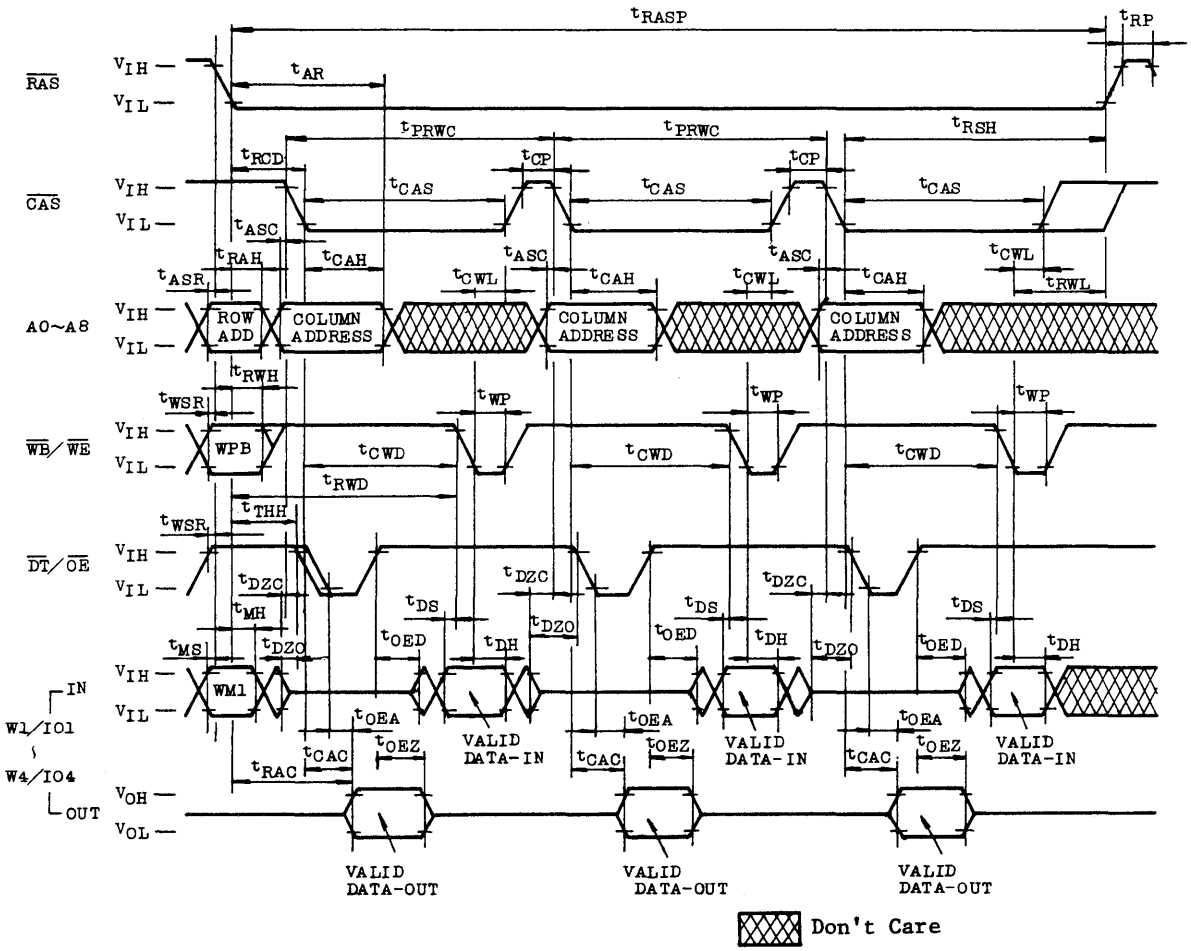
PAGE MODE READ CYCLE



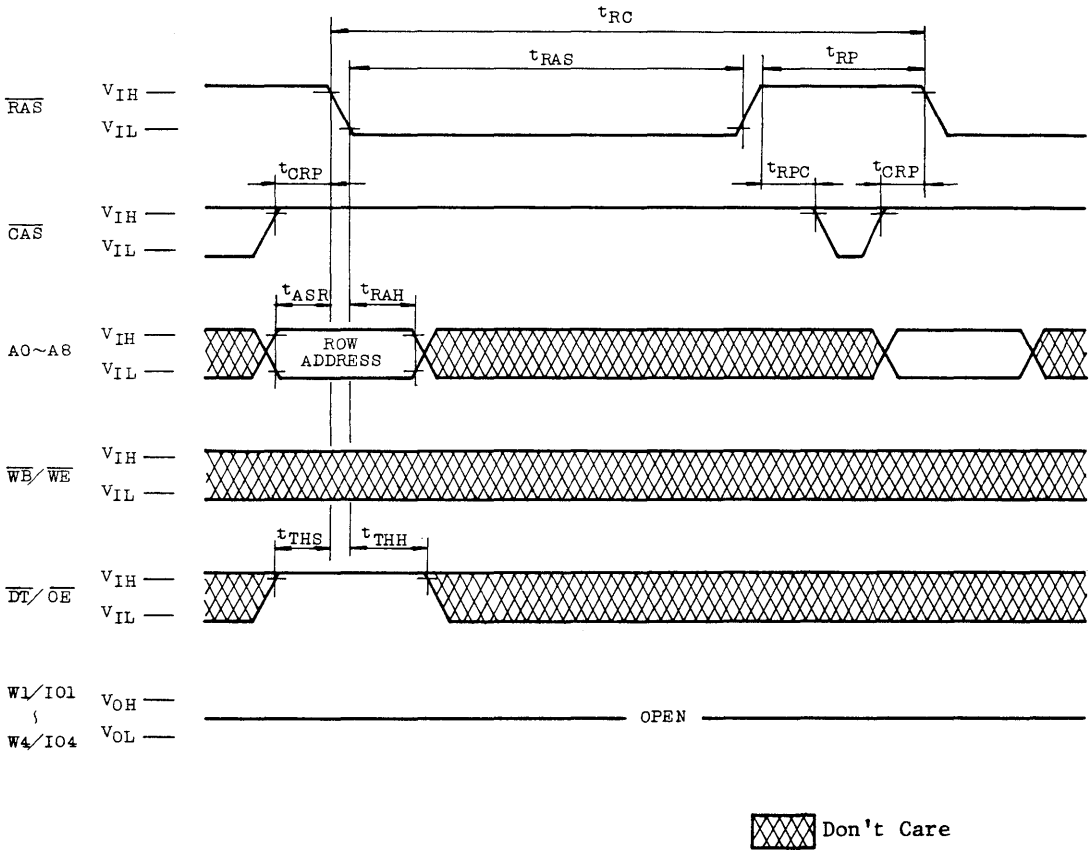
PAGE MODE WRITE CYCLE (EARLY WRITE)



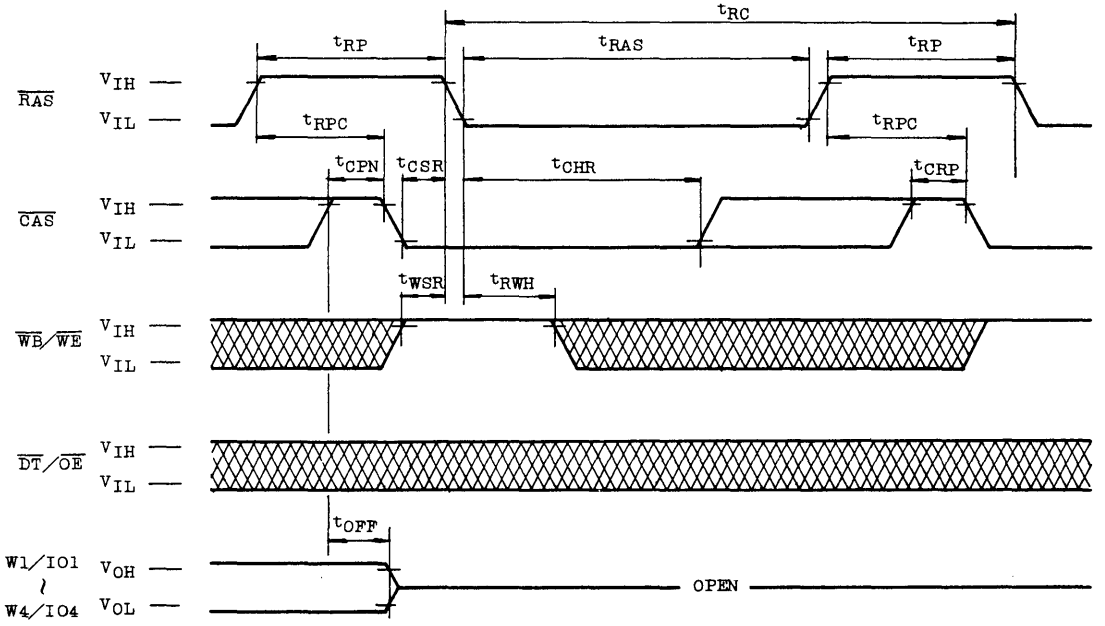
PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE



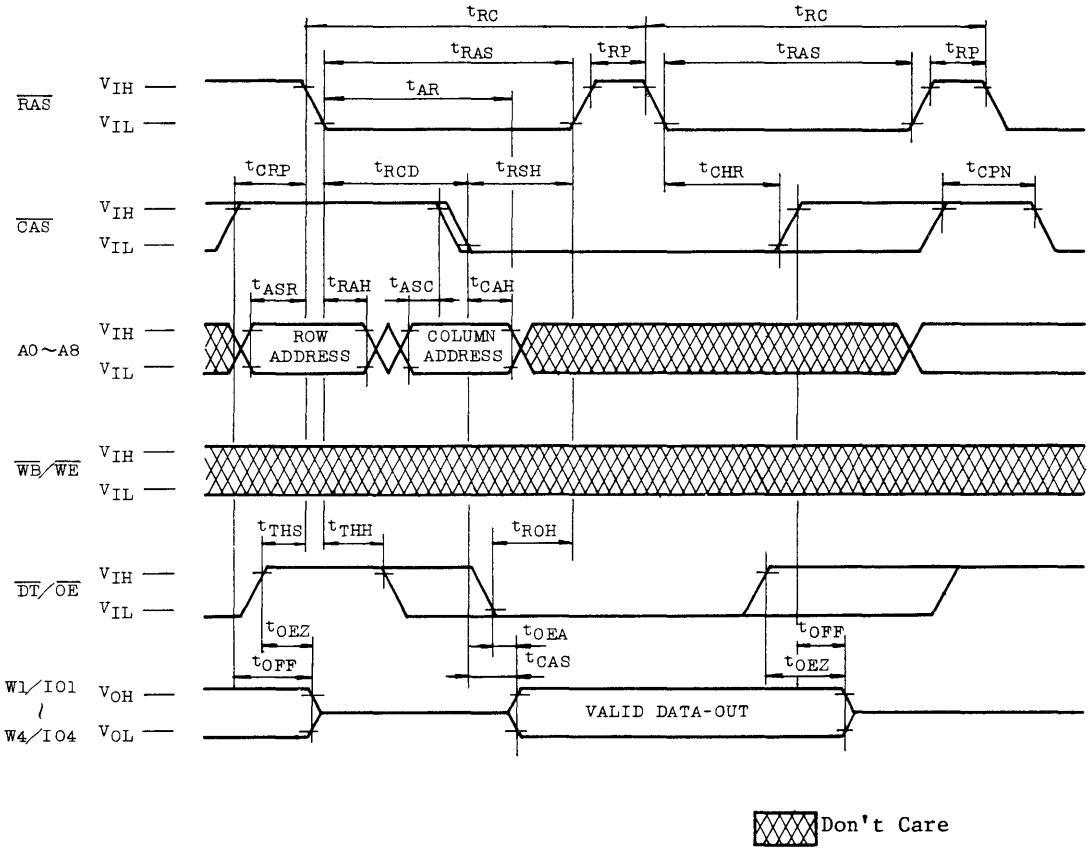
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



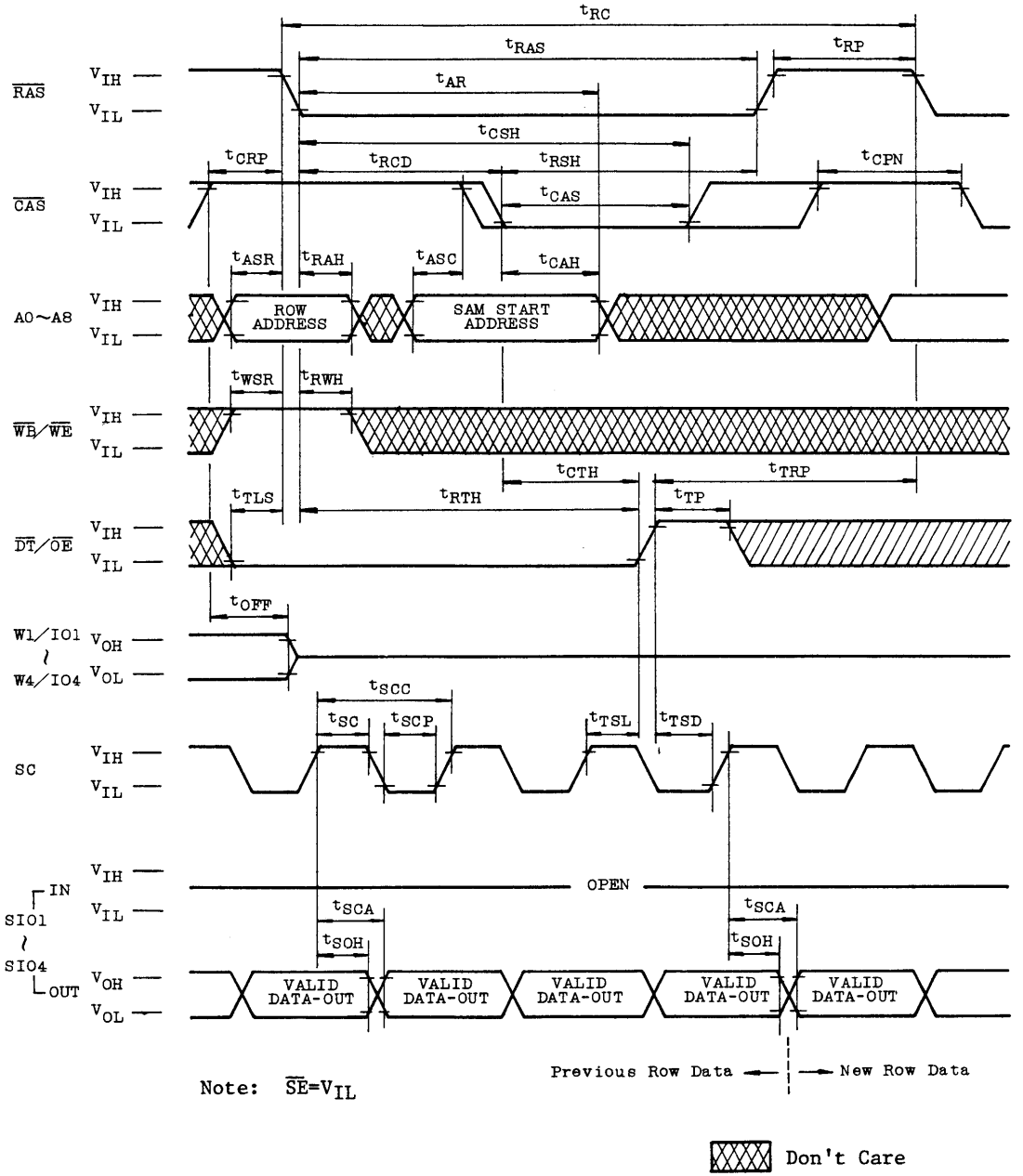
Note: A0 ∿ A8=Don't Care

Don't Care

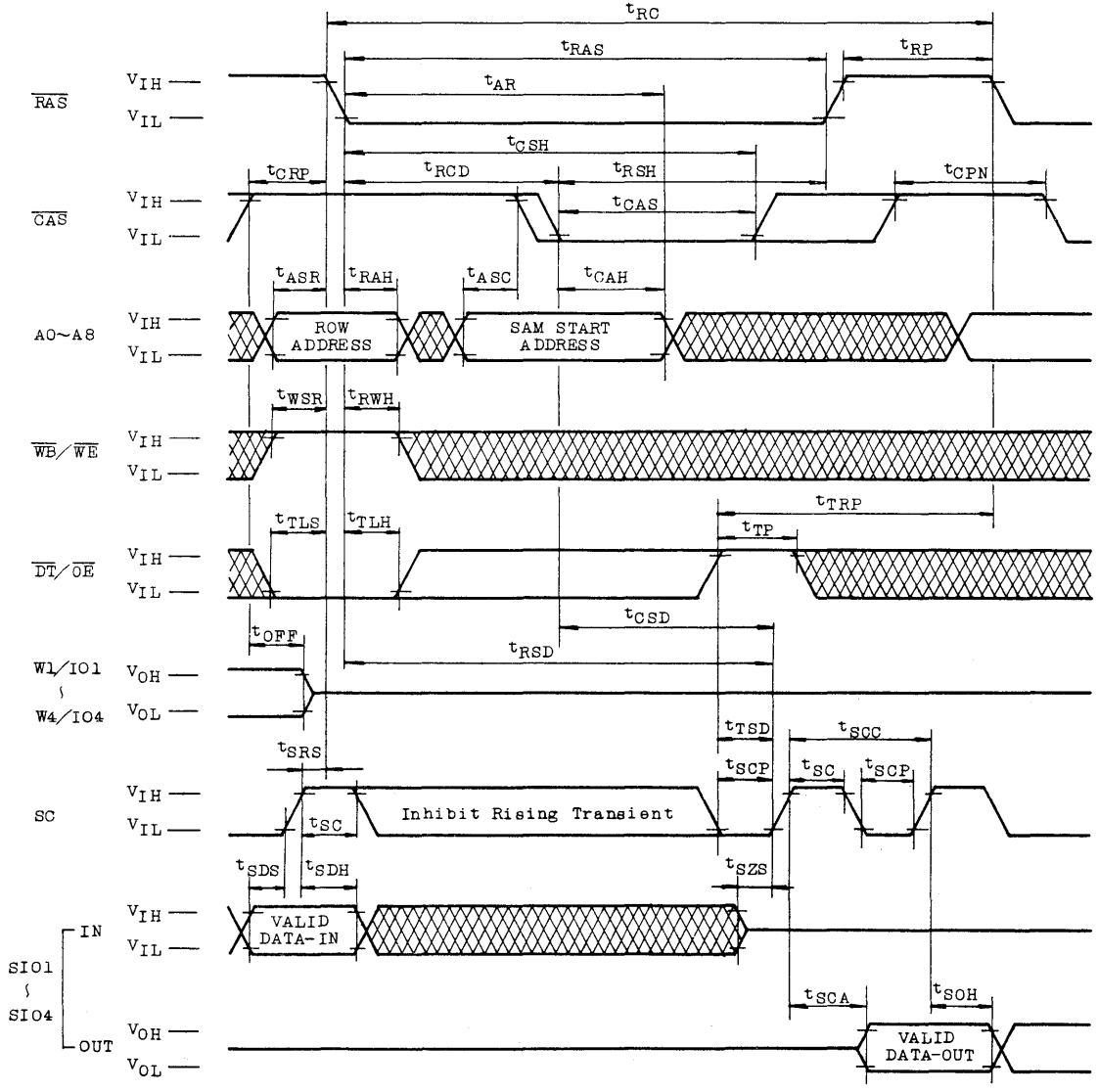
HIDDEN REFRESH CYCLE



REAL TIME READ TRANSFER CYCLE



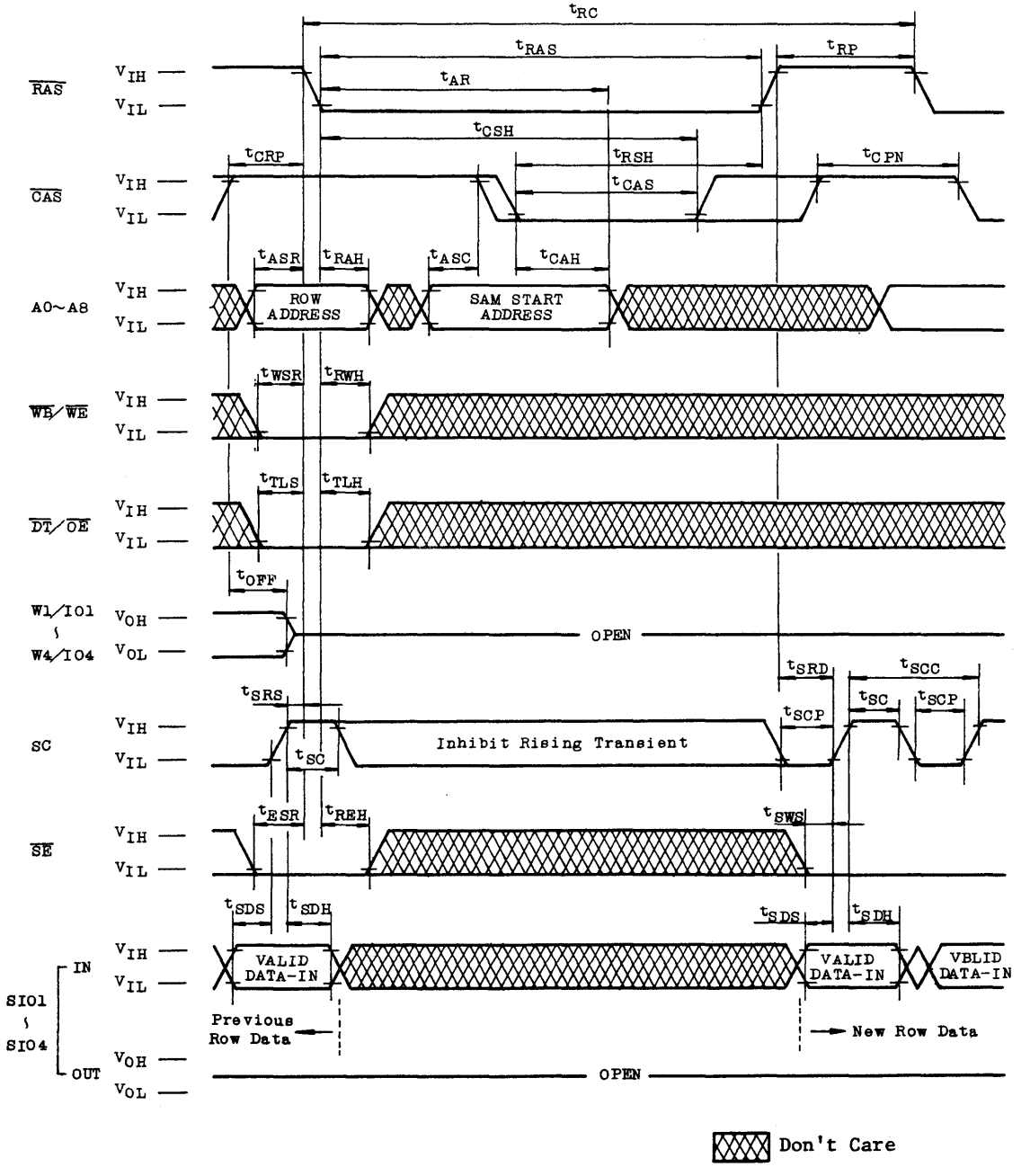
READ TRANSFER CYCLE (Previous transfer is write transfer)



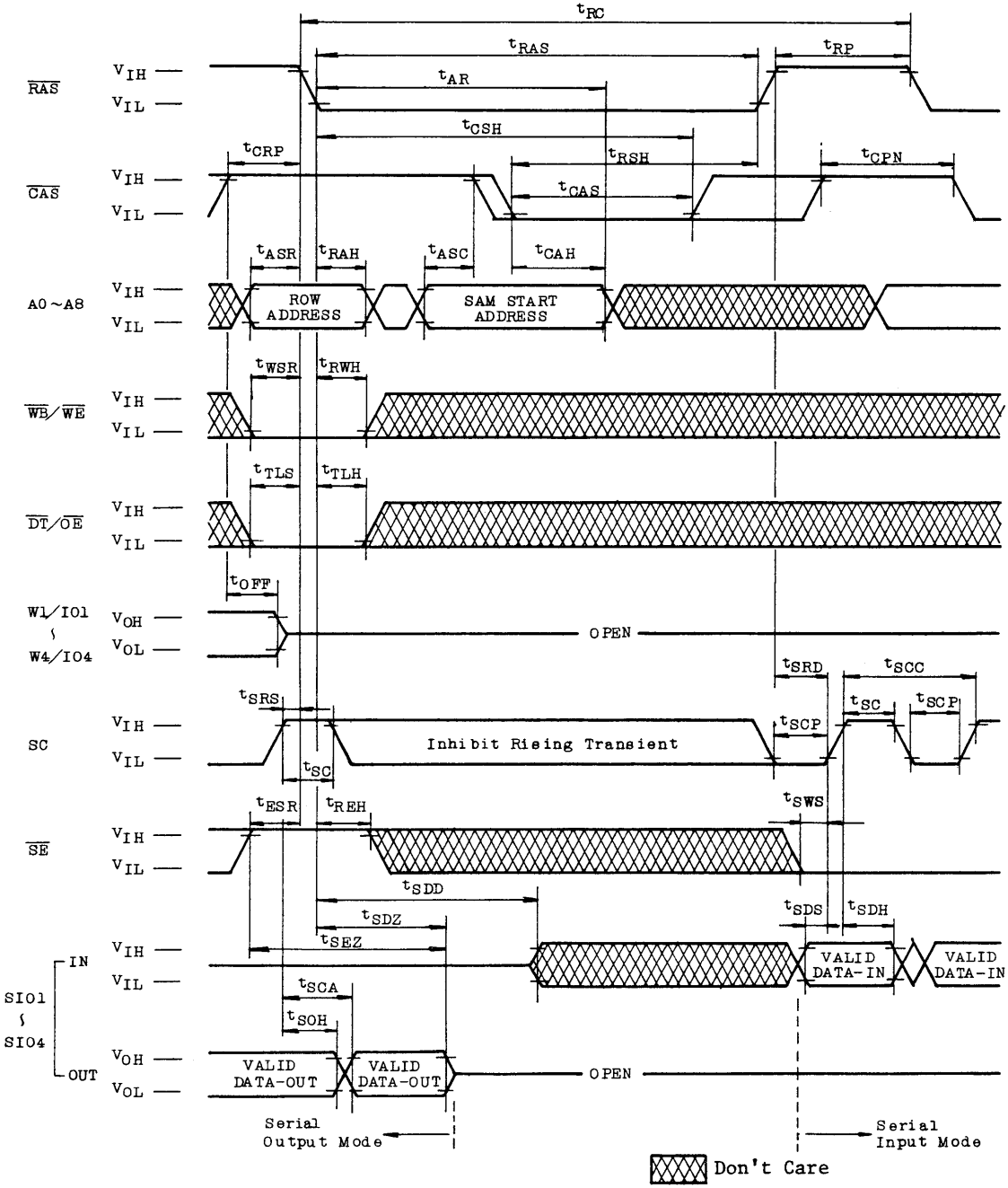
Note: $\overline{SE}=V_{IL}$

Don't Care

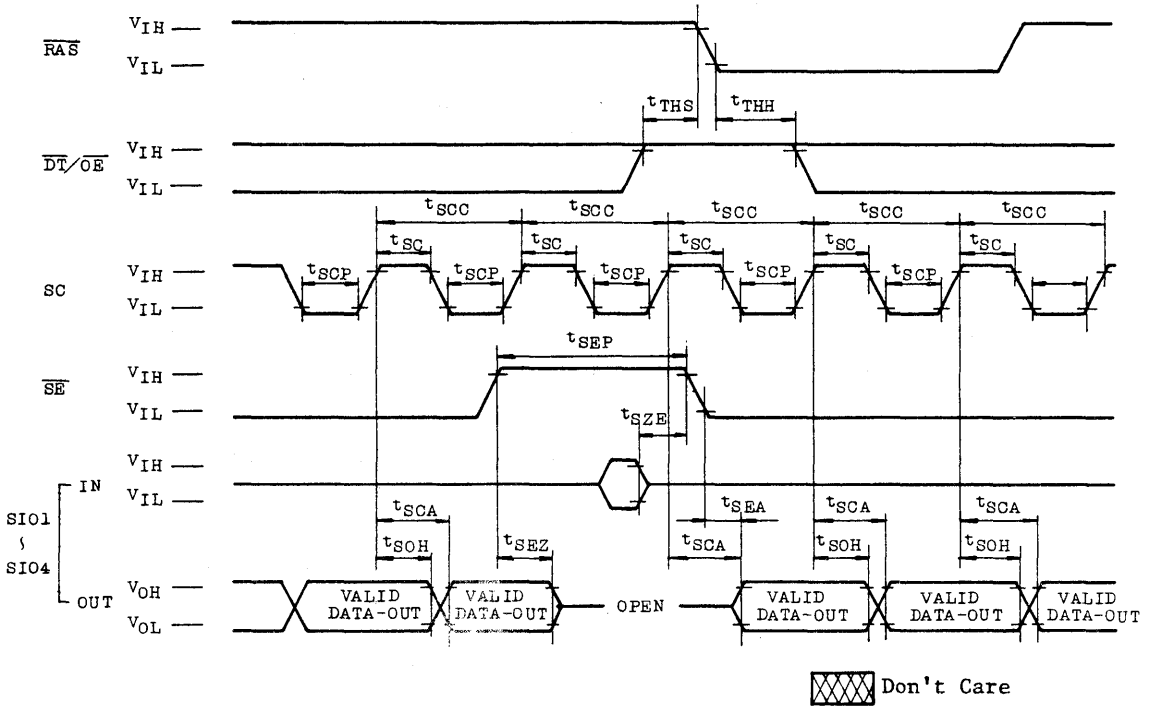
WRITE TRANSFER CYCLE



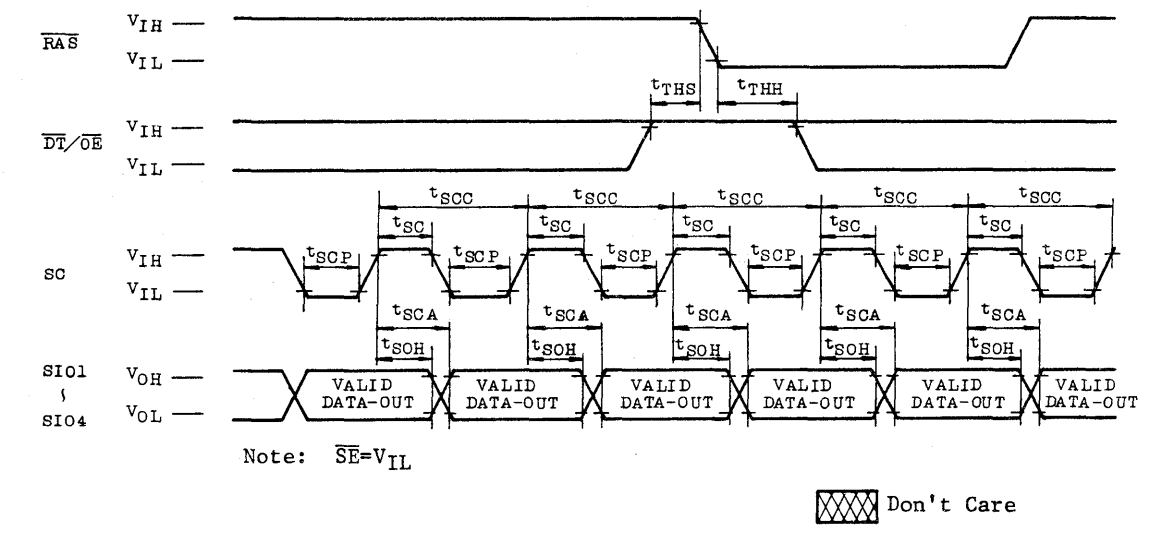
PSEUDO WRITE TRANSFER CYCLE



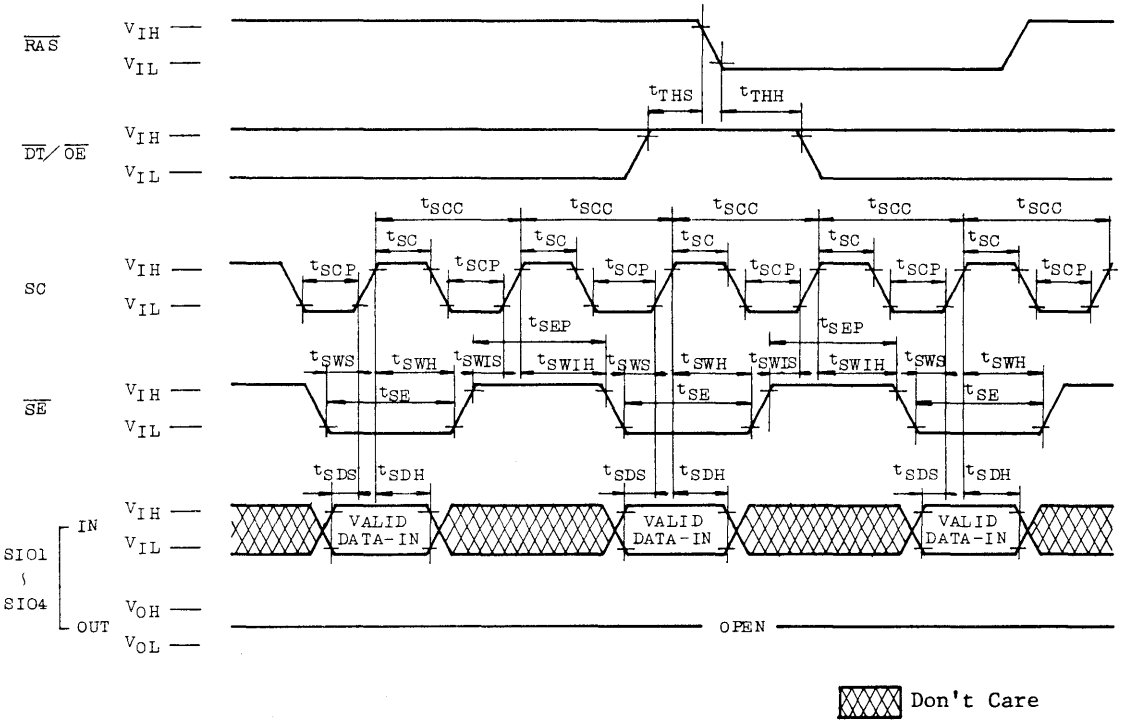
SERIAL READ CYCLE ($\overline{SE}$ CONTROLLED OUTPUTS)



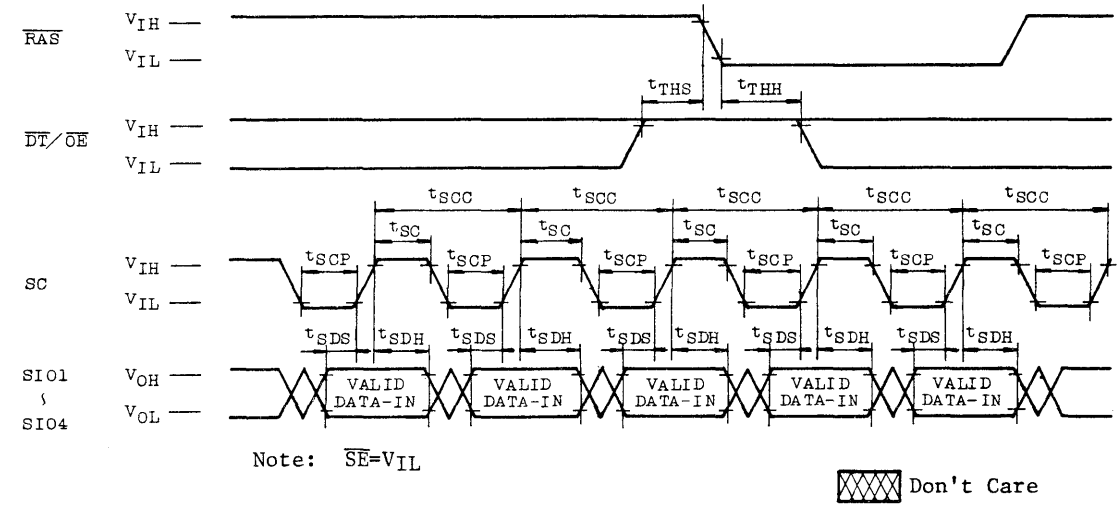
SERIAL READ CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ CONTROLLED WRITE)

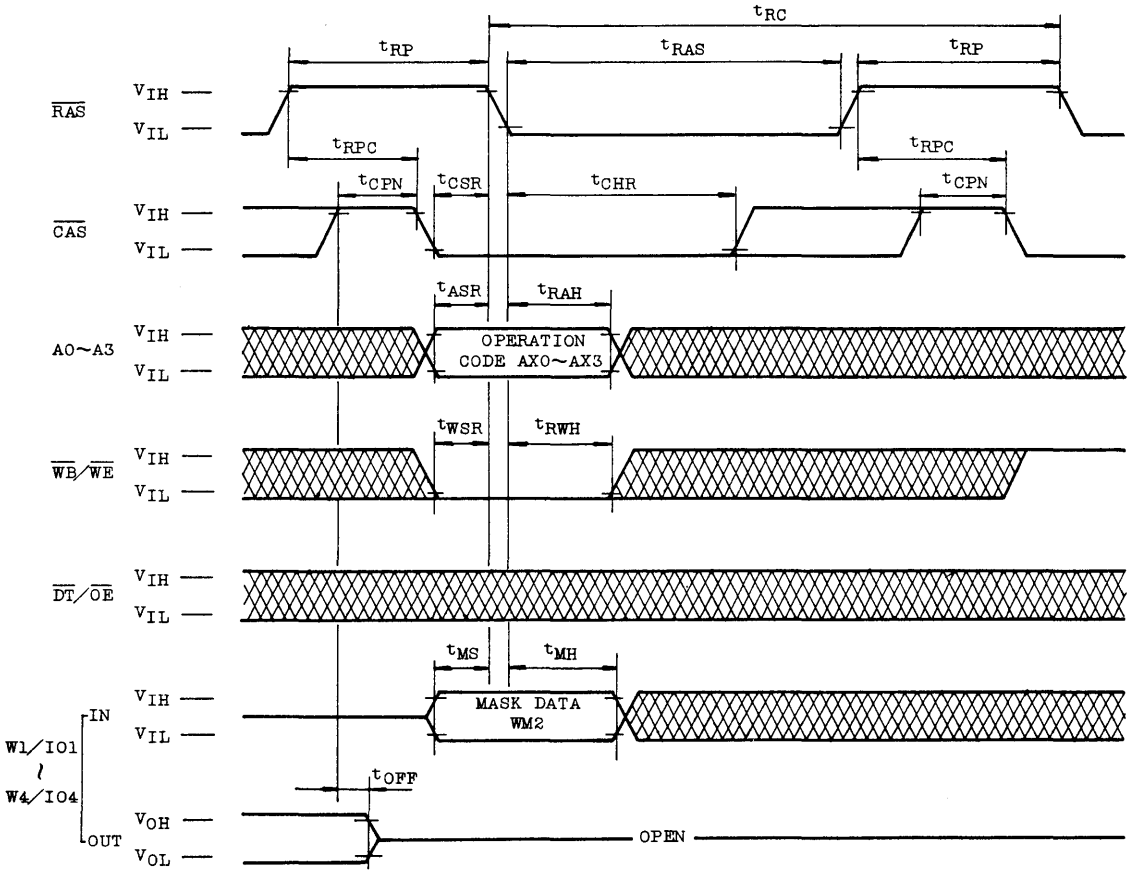


SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})



Note: $\overline{SE}$=V_{IL}

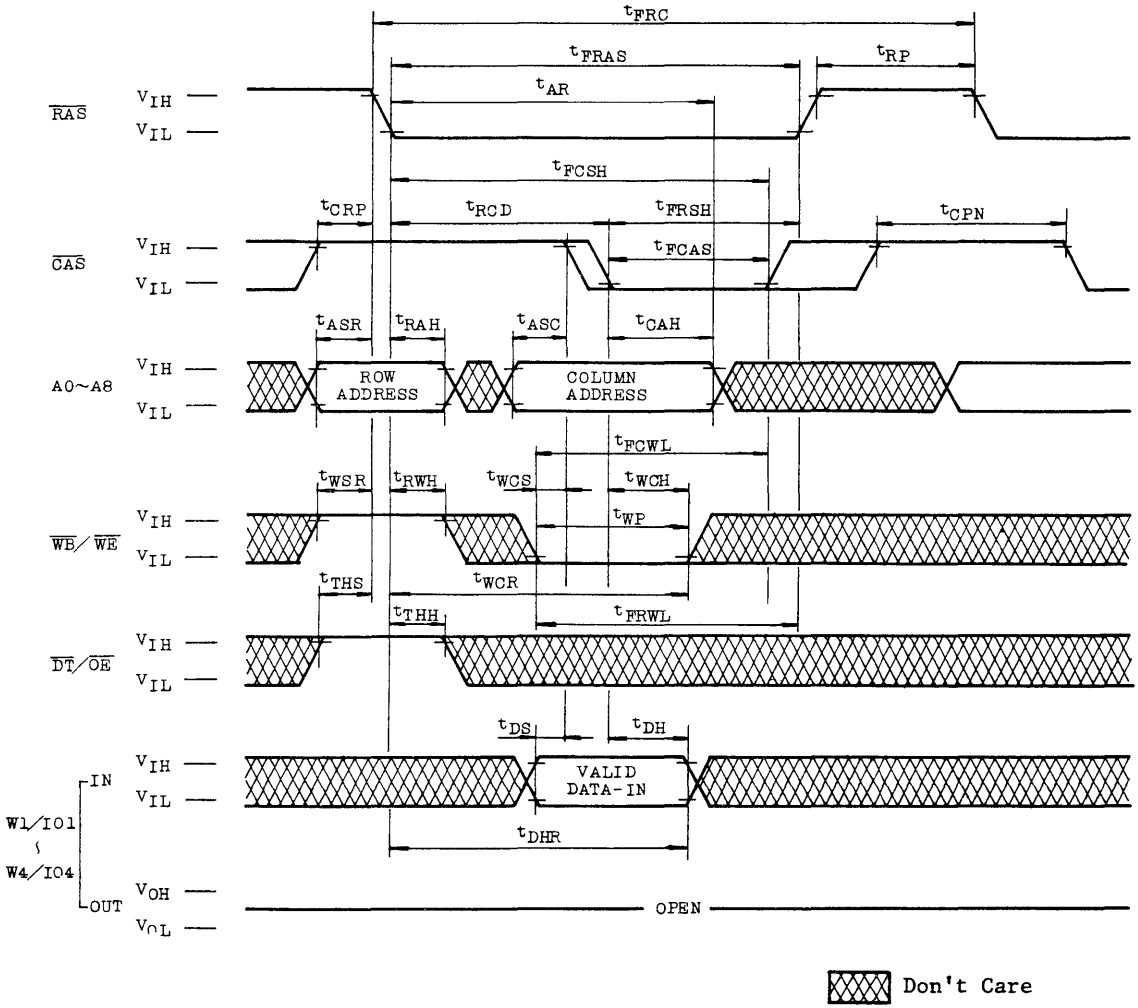
RASTER OPERATION SET-UP CYCLE



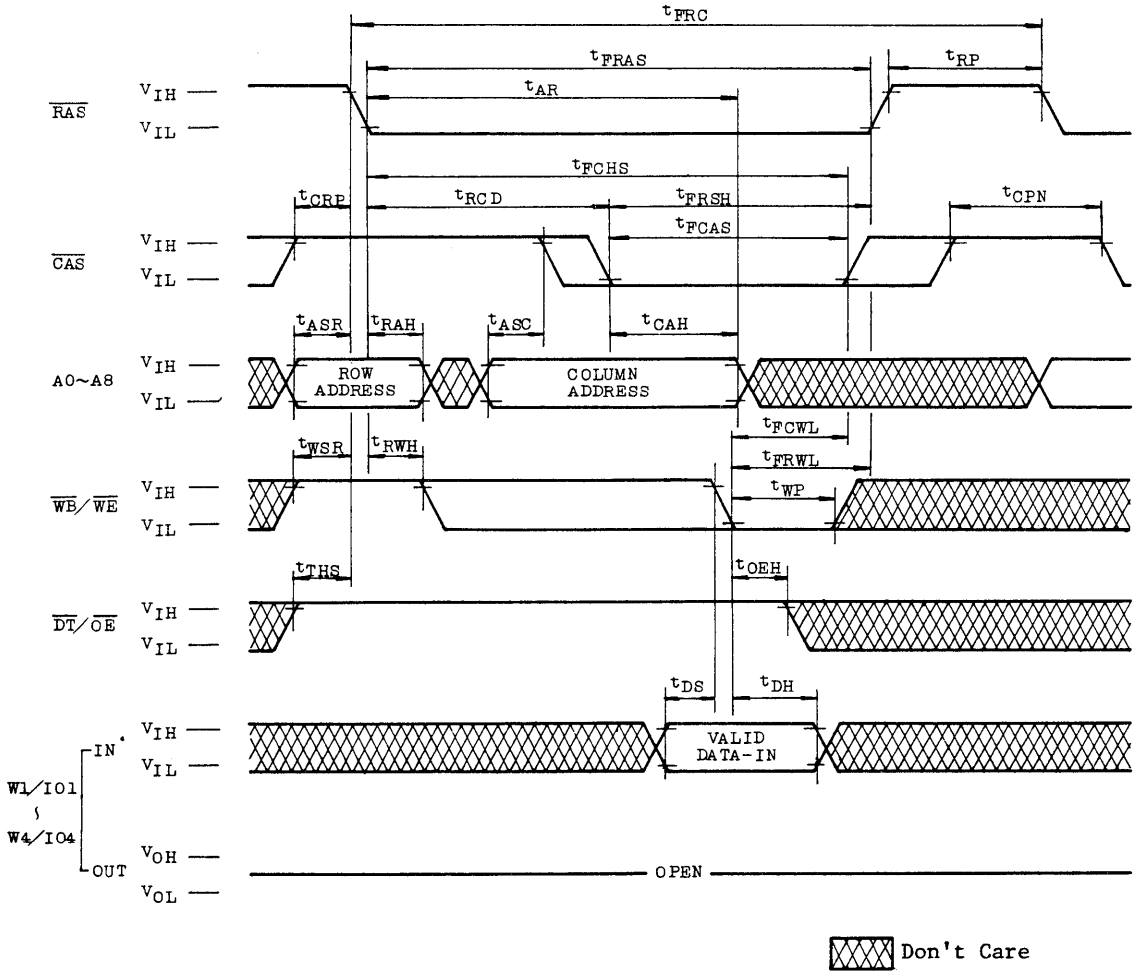
Note: A4 ∿ A8 Don't Care

Don't Care

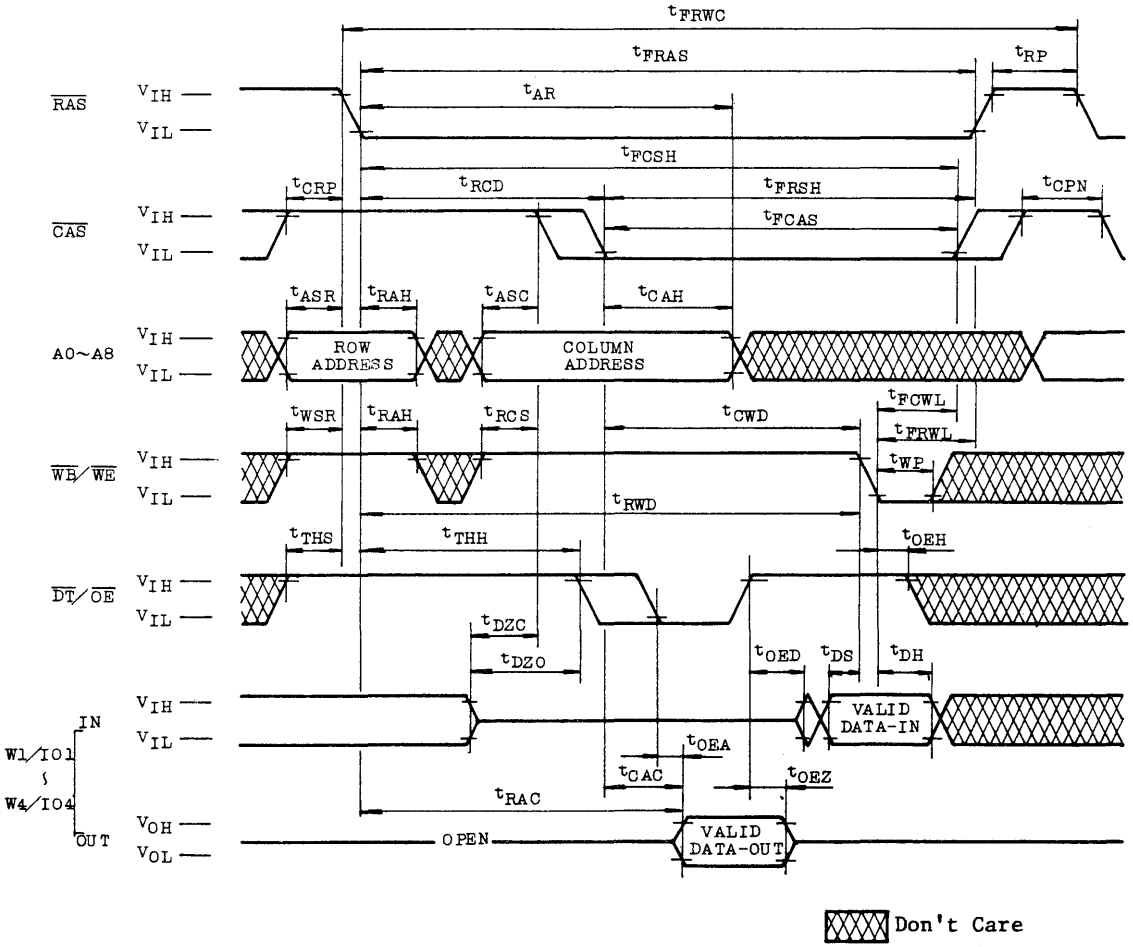
RASTER OPERATION WRITE CYCLE (EARLY WRITE)



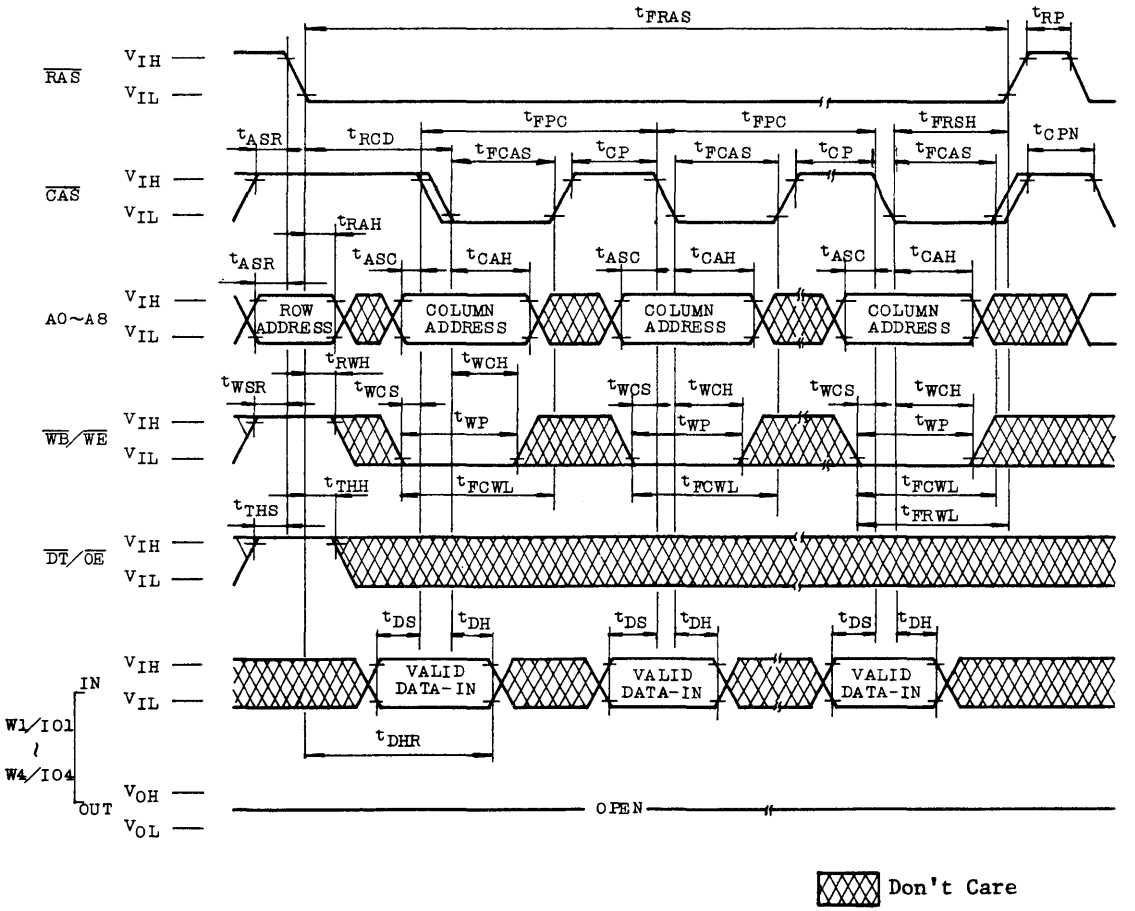
RASTER OPERATION WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



RASTER OPERATION READ-WRITE/READ-MODIFY-WRITE CYCLE



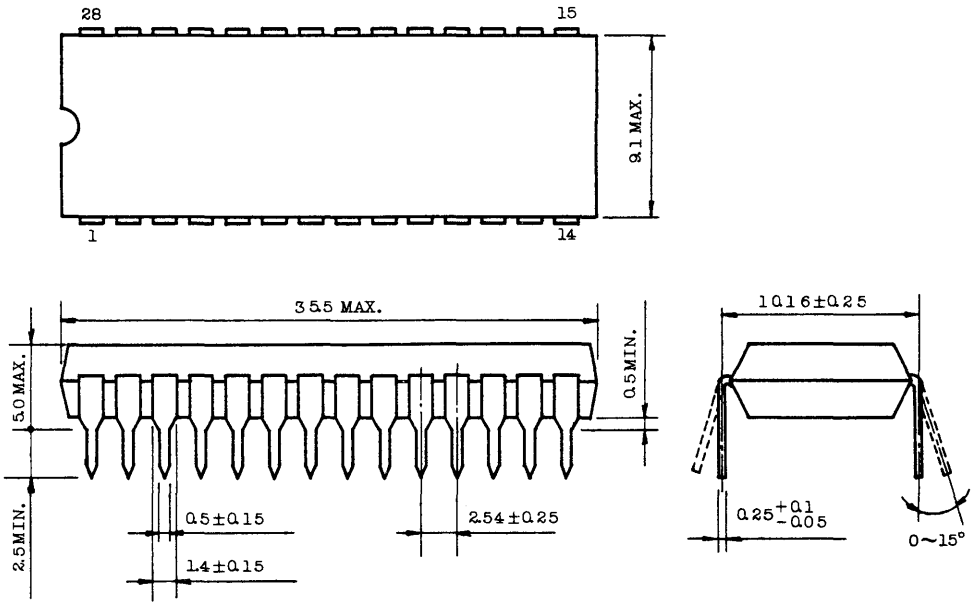
RASTER OPERATION PAGE MODE WRITE CYCLE



OUTLINE DRAWINGS

Plastic DIP

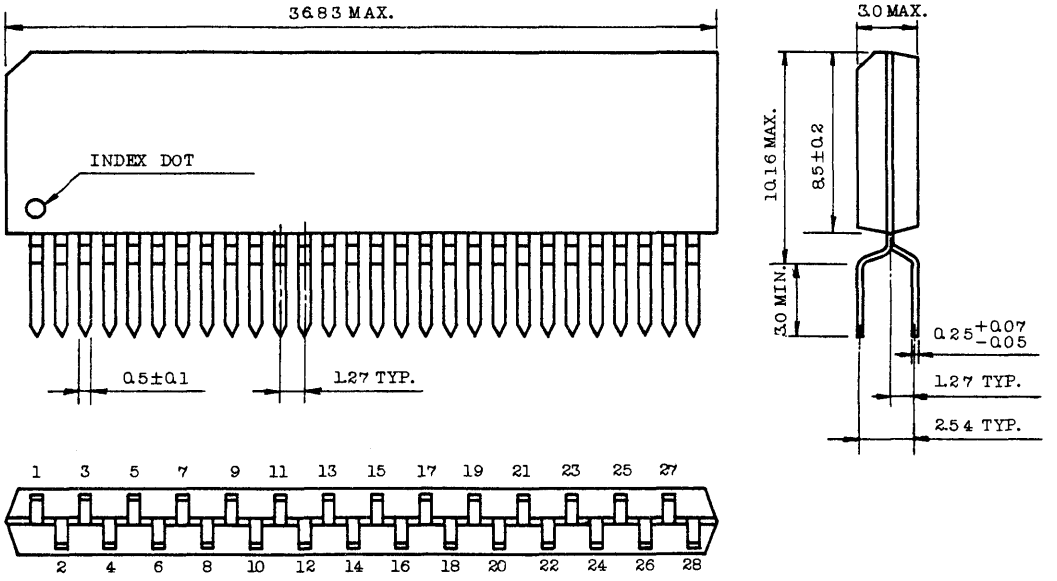
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.
All dimensions are in millimeters.

Plastic ZIP

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

TC524257J-10
TC524257J-12

PRELIMINARY

DESCRIPTION

The TC524257J is a CMOS Multiport memory equipped with a 262,144-word × 4 bit dynamic random access memory (RAM) port and a 512-word × 4 bit static serial access memory (SAM) port. In addition to the conventional DRAM operation modes, the TC524257J features a logic function and a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC524257J is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplexed address inputs and a common input/output organization allow the TC524257J to be housed in a standard 32-pin, 400-mil wide plastic SOJ.
System oriented features include a single 5V±10% power supply operation and compatibility with high performance schottky TTL logic.

FEATURES

ITEM		TC524257J	
		-10	-12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time(Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	60mA	55mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	40mA	35mA
I_{CC2}	RAM/SAM Standby Current	3mA	

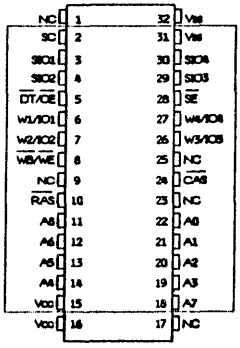
- Organization
  RAM port: 262,144 words × 4 bits
  SAM port: 512 words × 4 bits
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, Page mode, Write-Per-Bit, Raster operation, Read transfer, Write transfer, Serial read, Serial write capability
- All inputs and outputs TTL compatible
- 512 refresh cycle/8ms
- Package TC524257J : 0.4 inches 32 pins standard Plastic SOJ

PIN NAMES

A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Ouptut Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
W1/IO1 ∿ W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1 ∿ SIO4	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)

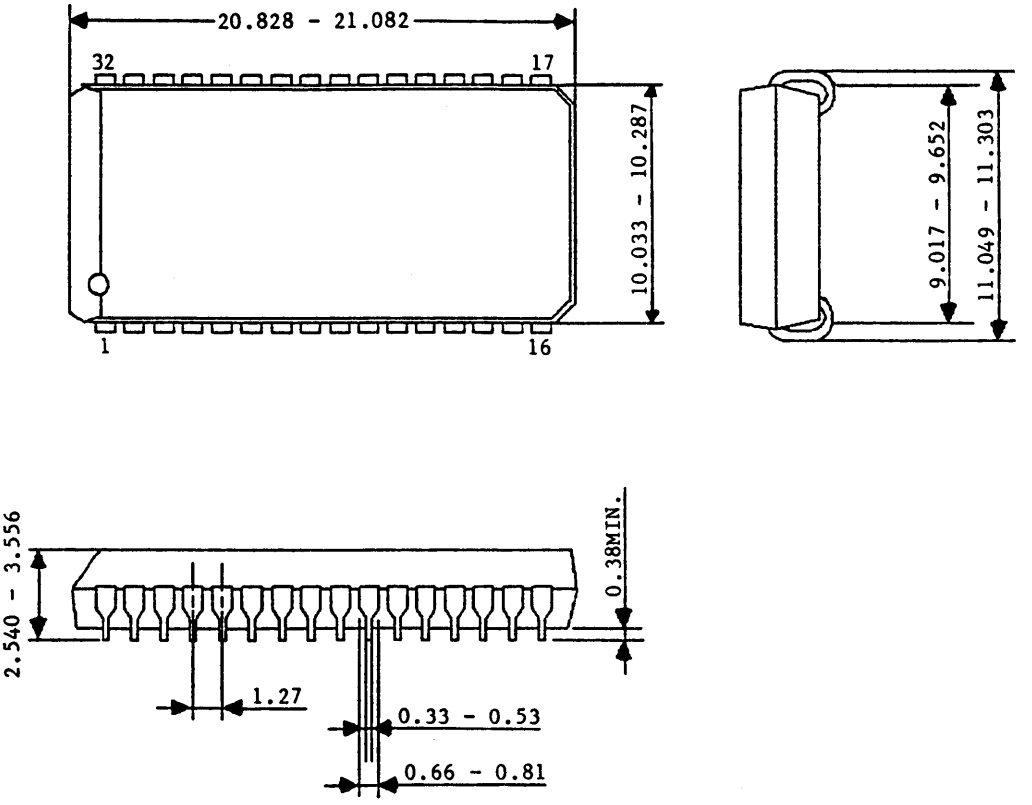
Plastic SOJ



OUTLINE DRAWINGS

- Plastic SOJ

Unit in mm



Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.

Module

1,048,576 WORDS×4 BIT
FAST PAGE MODE
DYNAMIC RAM MODULE

THM41000L-10,12

PRELIMINARY

DESCRIPTION

The THM41000L is a 1,048,576 words by 4 bits dynamic RAM module which assembled 4 pcs of TC511000J on the printed circuit board.

The THM41000L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

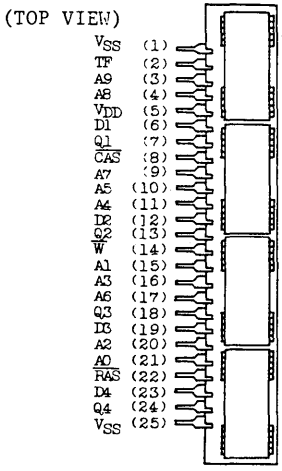
FEATURES

- 1,048,576 words by 4 bits organization
- Fast access time

		THM41000L-10	THM41000L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	30ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V ± 10%
- Low power
  1,320mW MAX. Operating (THM41000L-10)
  1,100mW MAX. Operating (THM41000L-12)
  22mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Assembly Height

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A9	Address Inputs
D1 ~ D4	Data Input
Q1 ~ Q4	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground

1,048,576 WORDS×4 BIT
NIBBLE MODE
DYNAMIC RAM MODULE

THM41001L-10,12

PRELIMINARY

DESCRIPTION

The THM41001L is a 1,048,576 words by 4 bits dynamic RAM module which assembled 4 pcs of TC511001J on the printed circuit board.

The THM41001L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

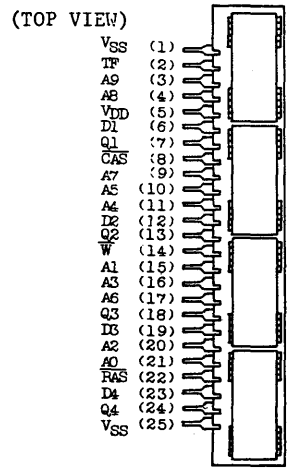
FEATURES

- 1,048,576 words by 4 bits organization
- Fast access time

		THM41001L-10	THM41001L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	40ns
t_{RC}	Cycle Time	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	50ns

- Single power supply of 5V ± 10%
- Low power
  1,320mW MAX. Operating (THM41001L-10)
  1,100mW MAX. Operating (THM41001L-12)
  22mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Nibble Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Assembly Height

PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A9	Address Inputs
D1 ~ D4	Data Input
Q1 ~ Q4	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
TF	Test Function
Vcc	Power (+5V)
Vss	Ground

1,048,576 WORDS×4 BIT
STATIC COLUMN MODE
DYNAMIC RAM MODULE

THM41002L-10,12

PRELIMINARY

DESCRIPTION

The THM41002L is a 1,048,576 words by 4 bits dynamic RAM module which assembled 4 pcs of TC511002J on the printed circuit board.

The THM41002L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

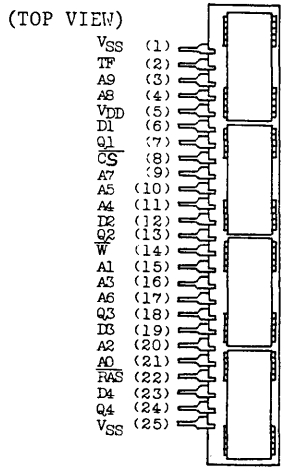
FEATURES

- 1,048,576 words by 4 bits organization
- Fast access time

		THM41002L-10	THM41002L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	30ns
t_{RC}	Cycle Time	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	55ns	65ns

- Single power supply of 5V ± 10%
- Low power
  1,320mW MAX. Operating (THM41002L-10)
  1,100mW MAX. Operating (THM41002L-12)
  22mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Assembly Height

PIN CONNECTION (TOP VIEW)

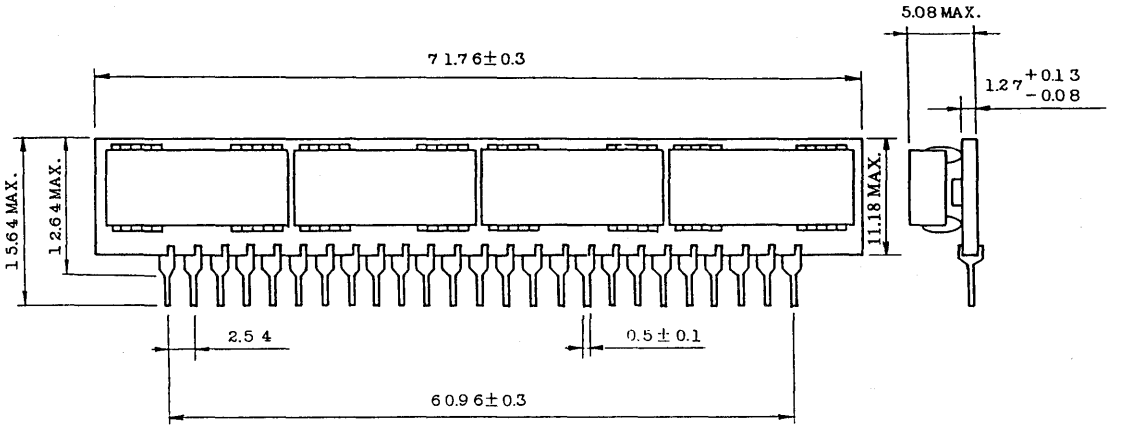


PIN NAMES

A0 ~ A9	Address Inputs
D1 ~ D4	Data Input
Q1 ~ Q4	Data Output
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
TF	Test Function
V_{CC}	Power (+5V)
V_{SS}	Ground

- OUTLINE DRAWINGS

Unit im mm



TOSHIBA MOS MEMORY PRODUCTS

524,288 WORDS×8 BIT
FAST PAGE MODE
DYNAMIC RAM MODULE

THM8512S/L-10,12

PRELIMINARY

DESCRIPTION

The THM8512S/L is a 524,288 words by 8 bits dynamic RAM module which assembled 4 pcs of TC514256J on the printed circuit board.

The THM8512S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

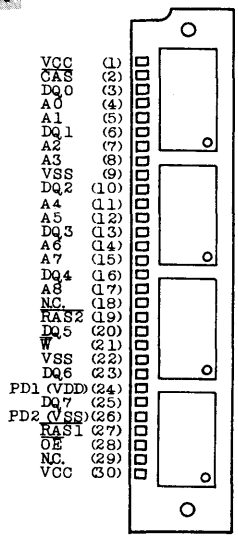
- 524,288 words by 8 bits organization
- Fast access time

		THM8512S/L-10	THM8512S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	55ns	70ns

- Single power supply of 5V ± 10%
- Low power
  737mW MAX. Operating (THM8512S/L-10)
  627mW MAX. Operating (THM8512S/L-12)
  22mW MAX. Standby
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

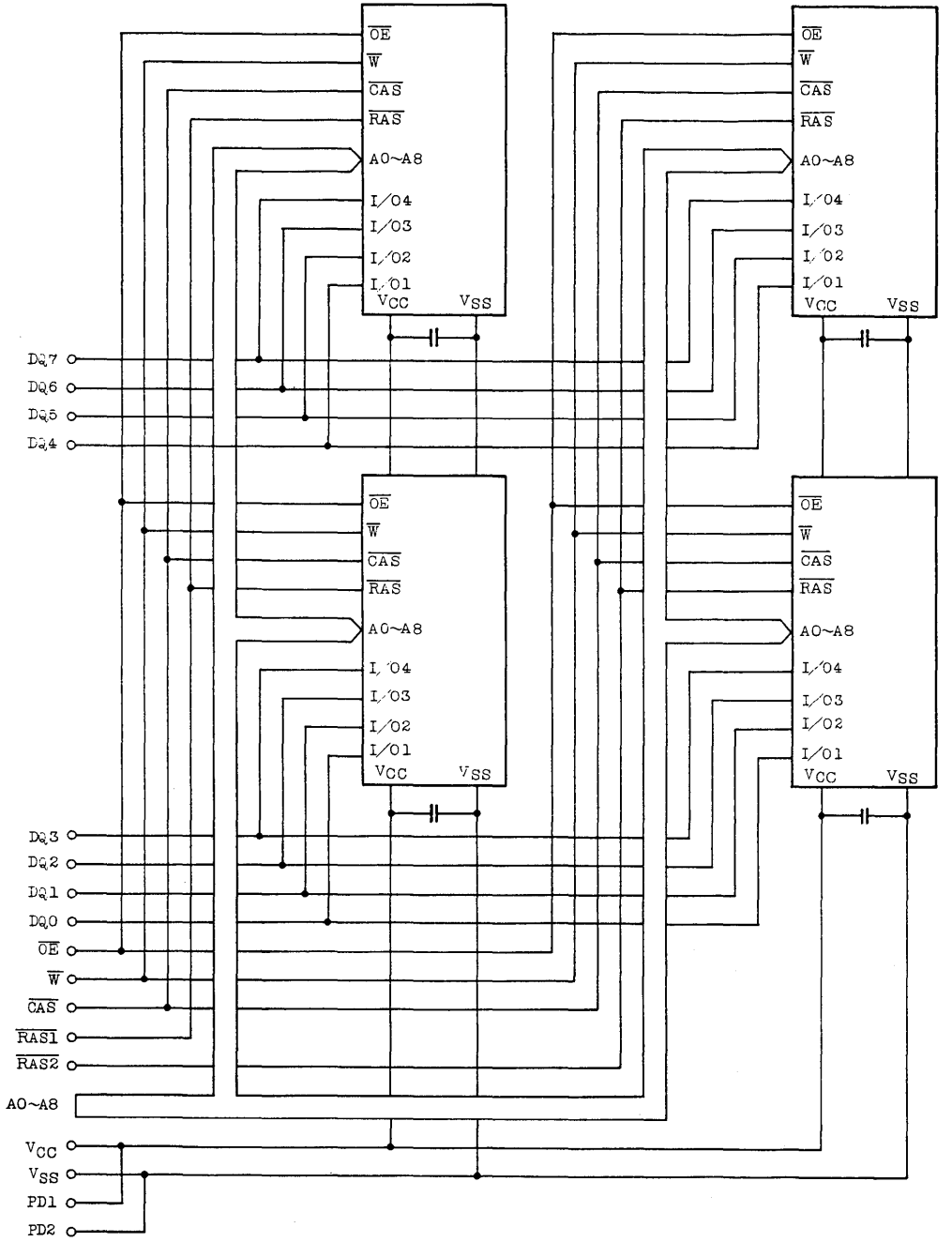
(TOP VIEW)



PIN NAMES

A0 ~ A8	Address Inputs
DQ0 ~ DQ7	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$1, 2	Row Address Strobe
PD1	Presence Detect (Power)
PD2	Presence Detect (Ground)
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	2.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM8512S/L-10	-	134	mA	3, 4
		THM8512S/L-12	-	114		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	8	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM8512S/L-10	-	260	mA	3
		THM8512S/L-12	-	220		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC}=t_{PC} MIN.)	THM8512S/L-10	-	94	mA	3, 4
		THM8512S/L-12	-	74		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	4	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM8512S/L-10	-	260	mA	3
		THM8512S/L-12	-	220		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-40	40	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level VOLTAGE (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level VOLTAGE (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7, 15)

SYMBOL	PARAMETER	THM8512S/L-10		THM8512S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	255	-	295	-	ns	
t_{PC}	Fast Page Mode Cycle Time	55	-	70	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	115	-	140	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-		-	35	ns	8,13
t_{AA}	Access Time from Column Address	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	50	-	65	ns	8,14
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	5	-	5	-	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	ns	9
t_T	Trnasition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	100	100,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	20	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	ns	10

SYMBOL	PARAMETER	THM8512S/L-10		THM8512S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	ns	12
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	65	-	75	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	135	-	160	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	85	-	100	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	60	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	20	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	25	-	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	-	30	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	25	0	30	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	25	-	30	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, $\overline{W}$, $\overline{CAS}$, $\overline{OE}$)	-	40	pF
C_{I2}	Input Capacitance ($\overline{RAS1}$, $\overline{RAS2}$)	-	20	pF
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)	-	20	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" May cause permanent damage to the device.

2. All voltage are reference to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measurement with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-wirte cycles.

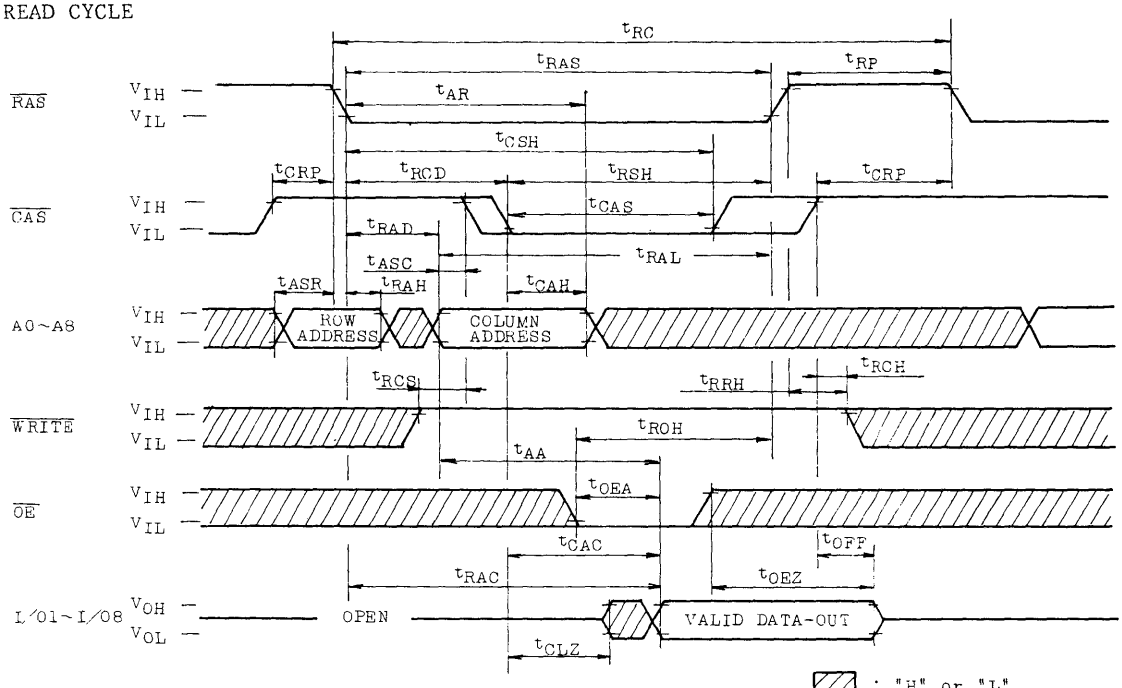
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.), the cycle is a read-modiry-write cycle and data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

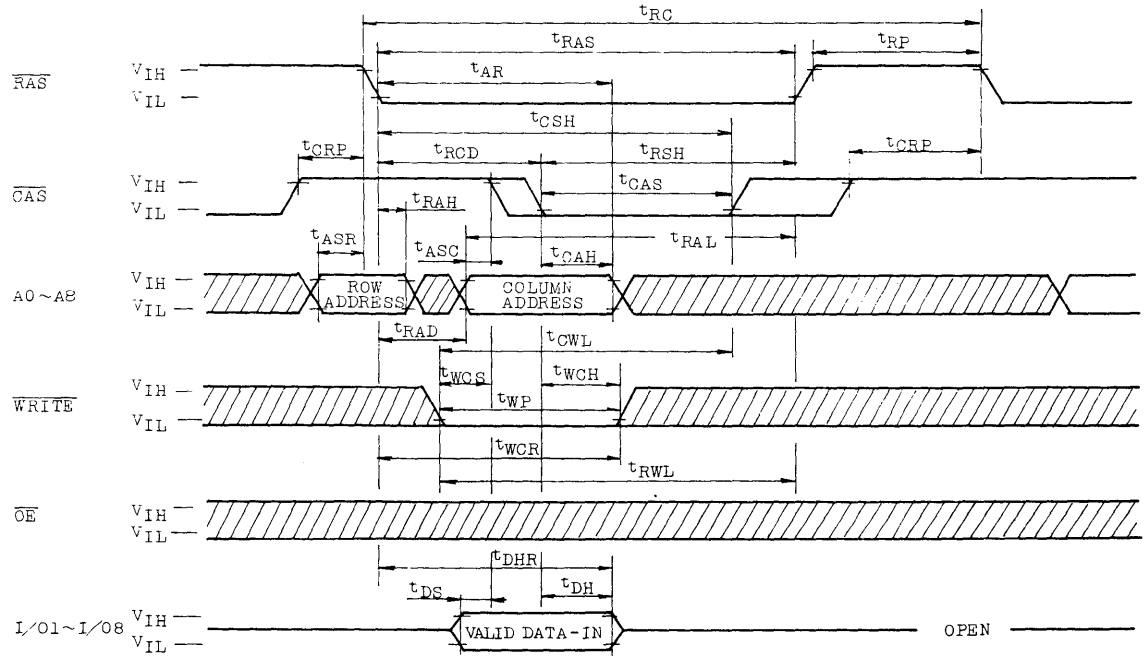
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

15. To prevent from the bus contention, please avoid such timing that both $\overline{RAS1}$ and $\overline{RAS2}$ are activating.

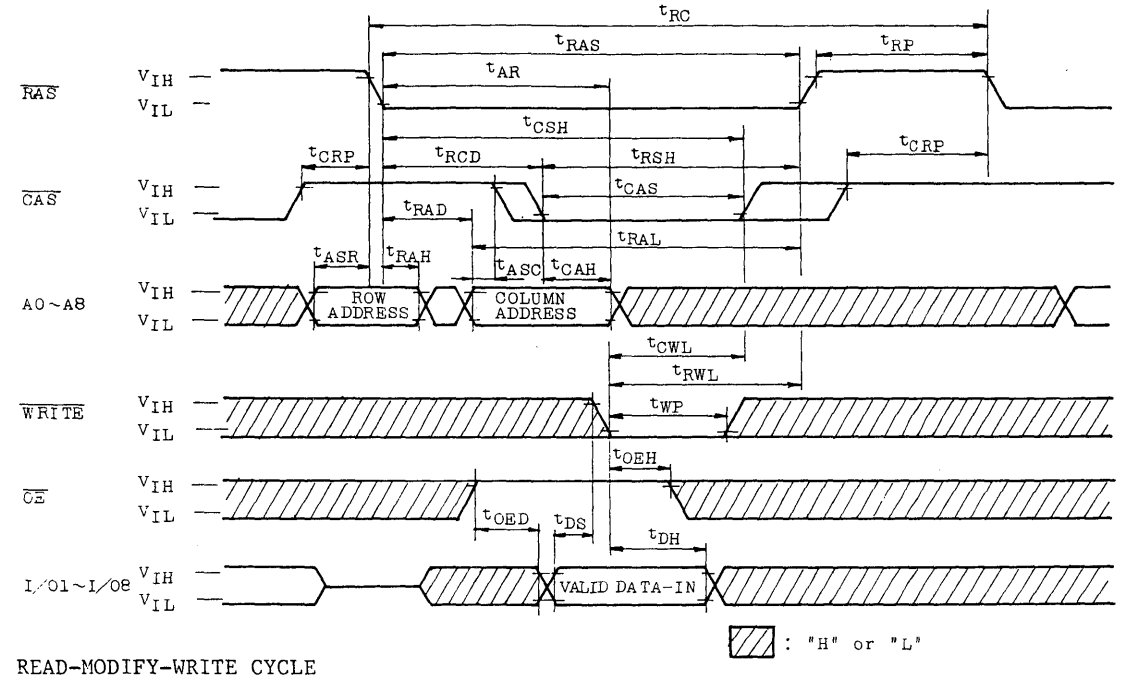
READ CYCLE



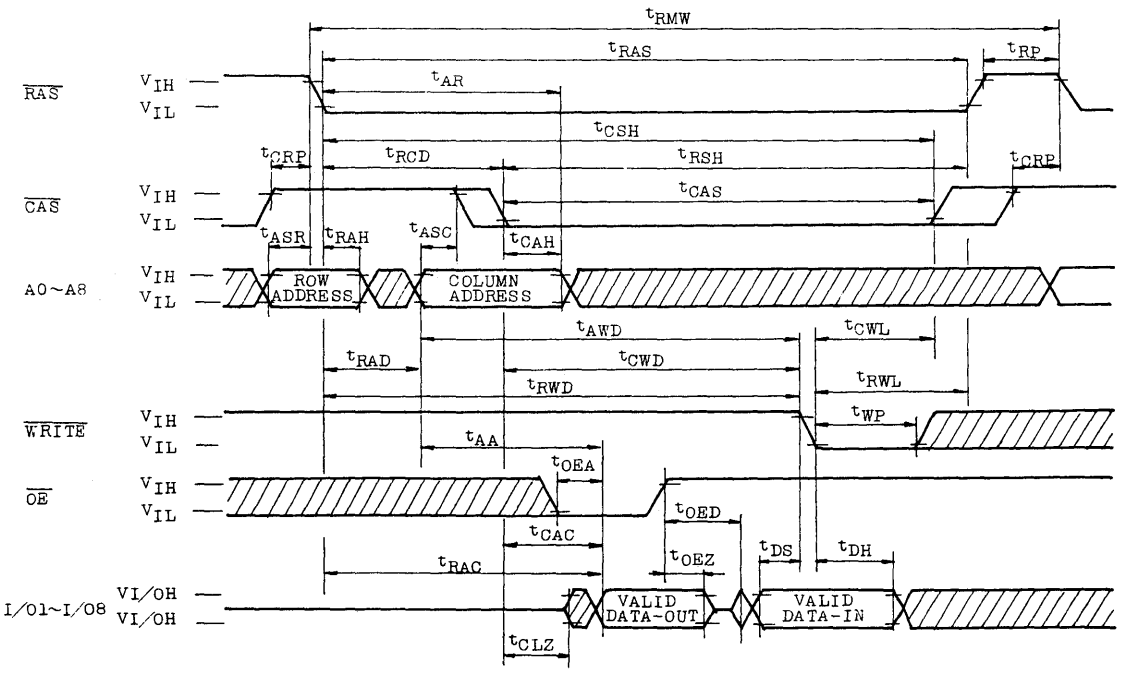
WRITE CYCLE (EARLY WRITE)



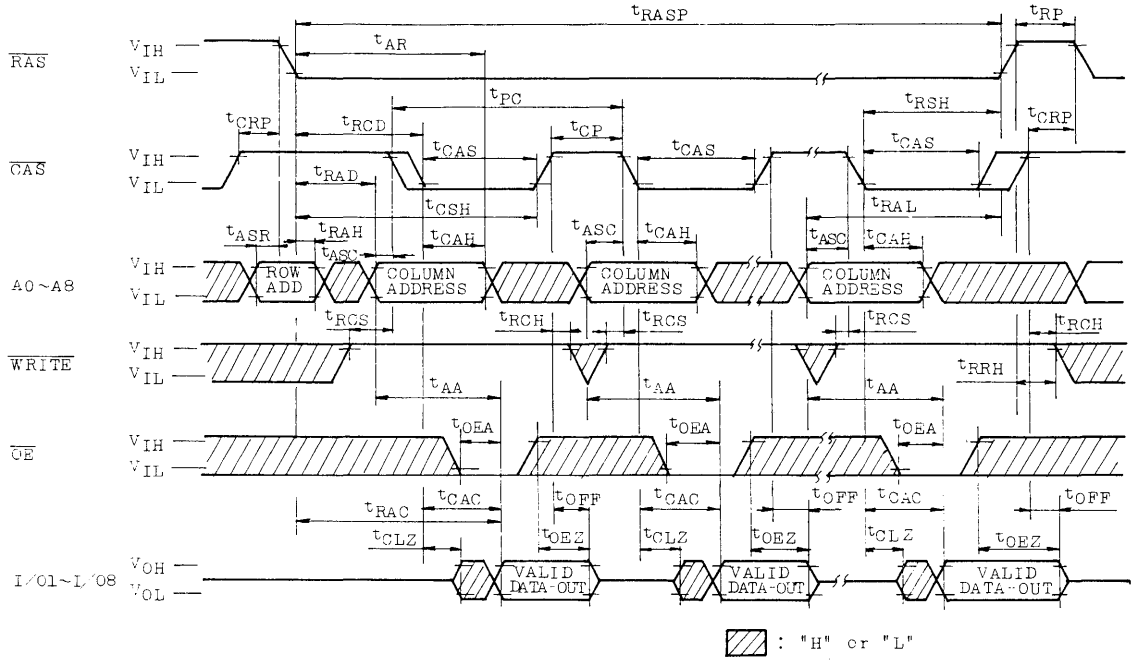
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



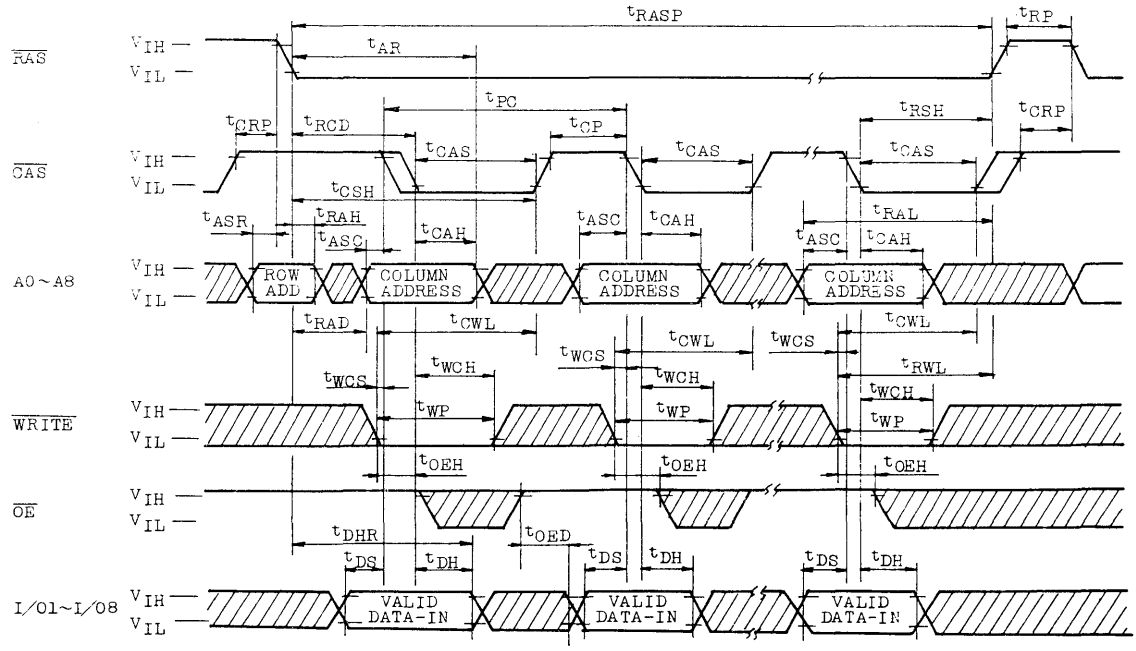
READ-MODIFY-WRITE CYCLE



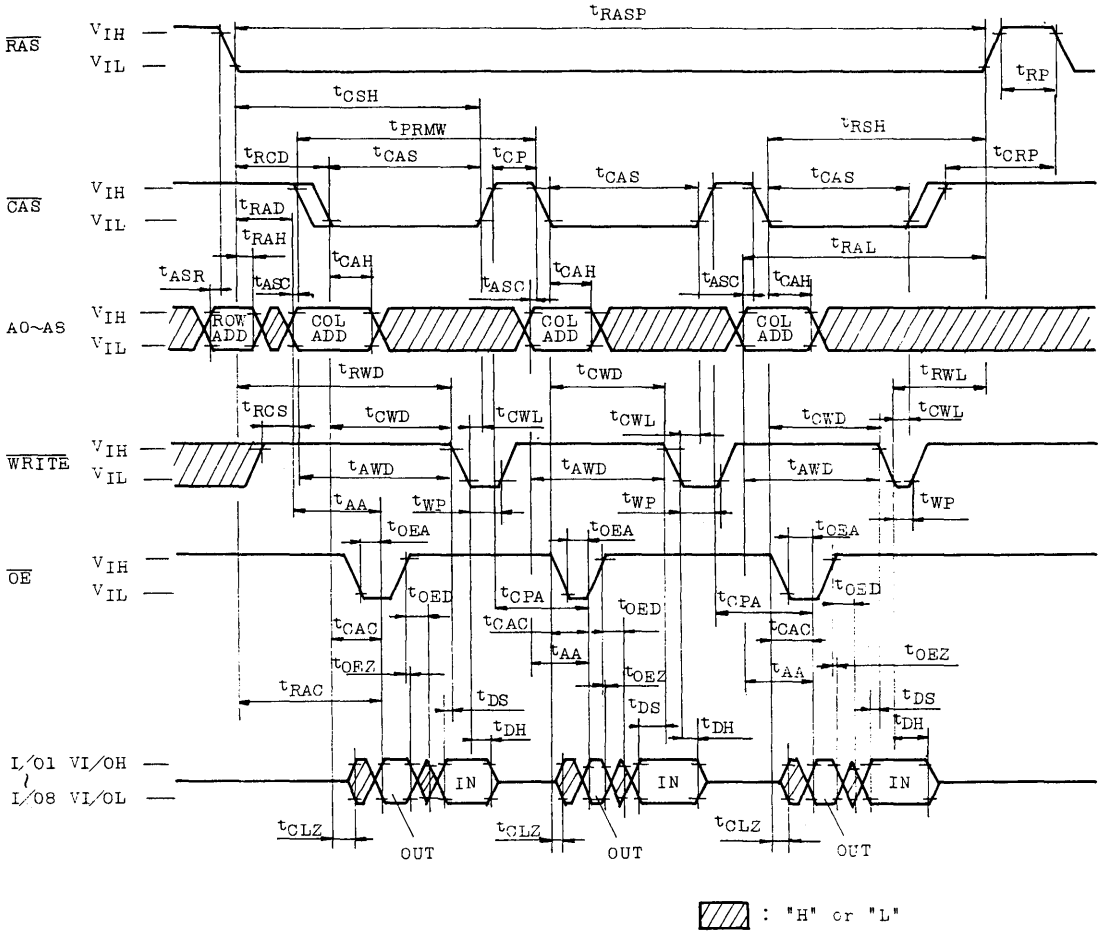
FAST PAGE MODE READ CYCLE



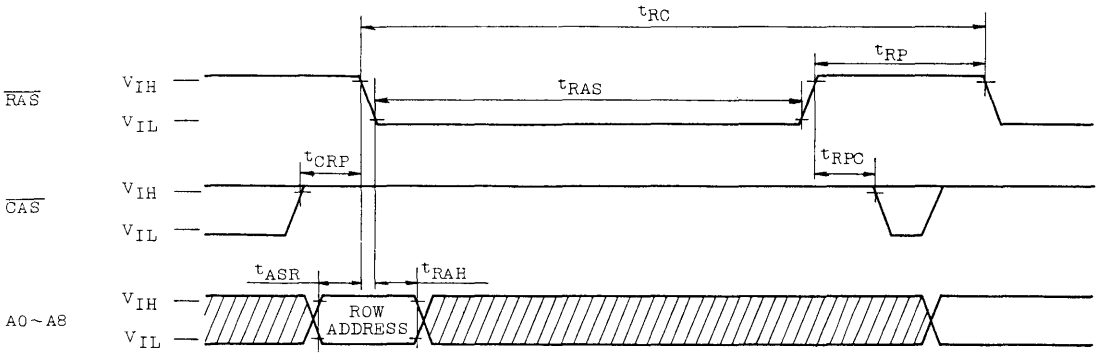
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



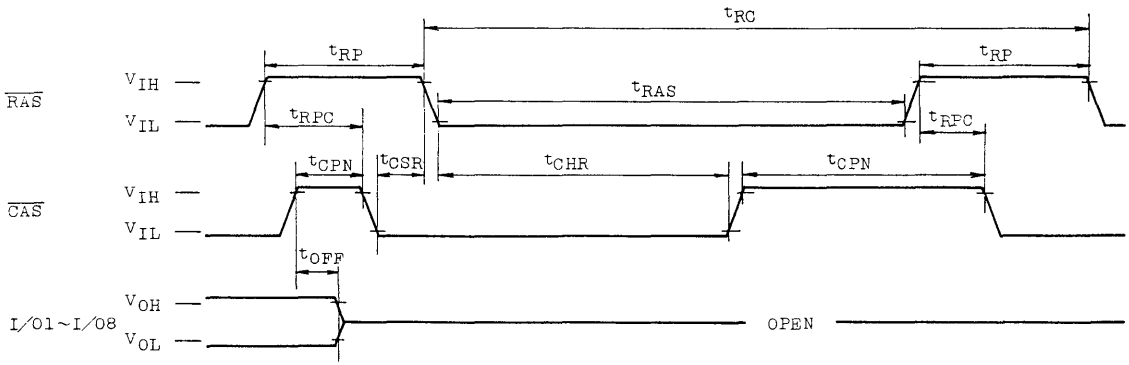
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$, $\overline{OE}$: "H" or "L"

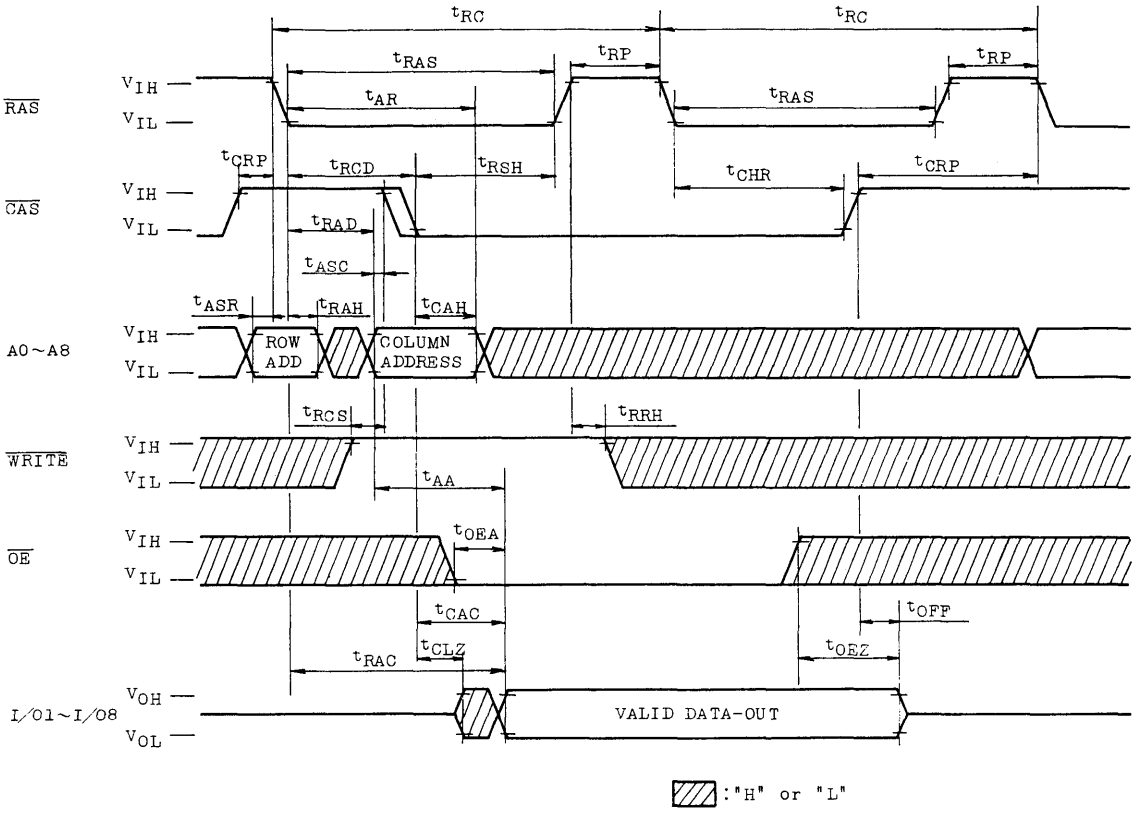
▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

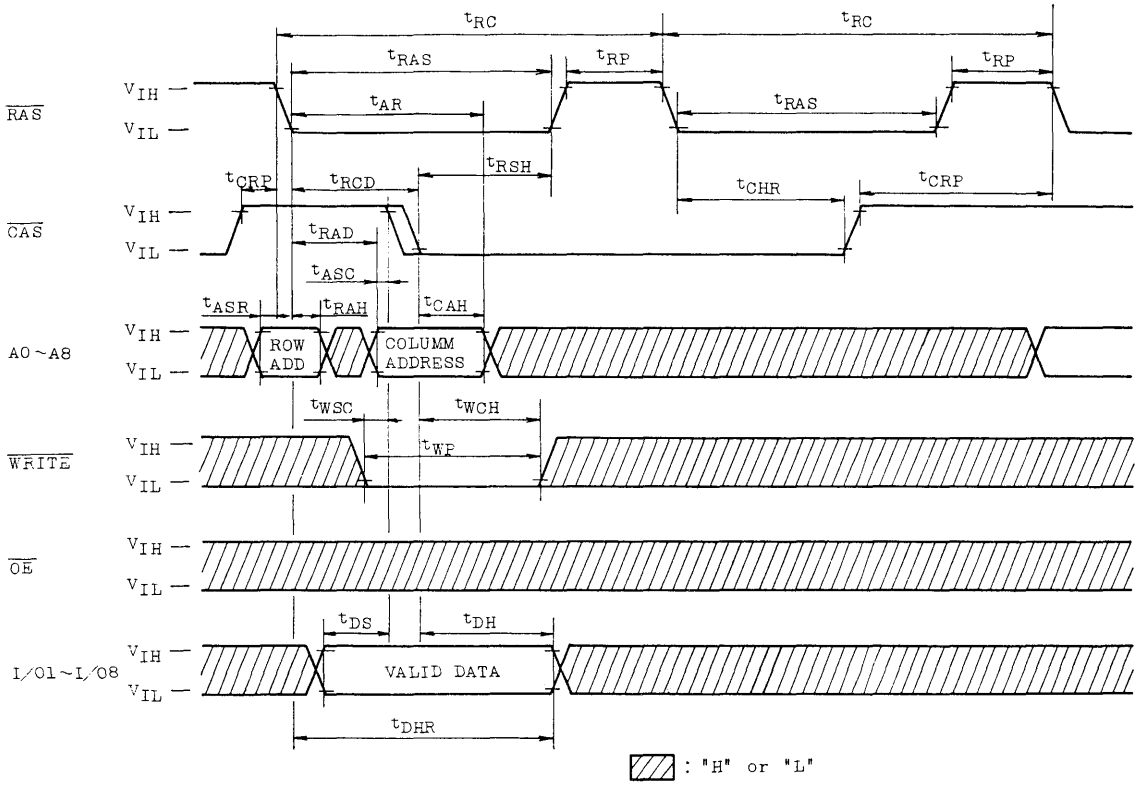


Note: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8: "H" or "L"

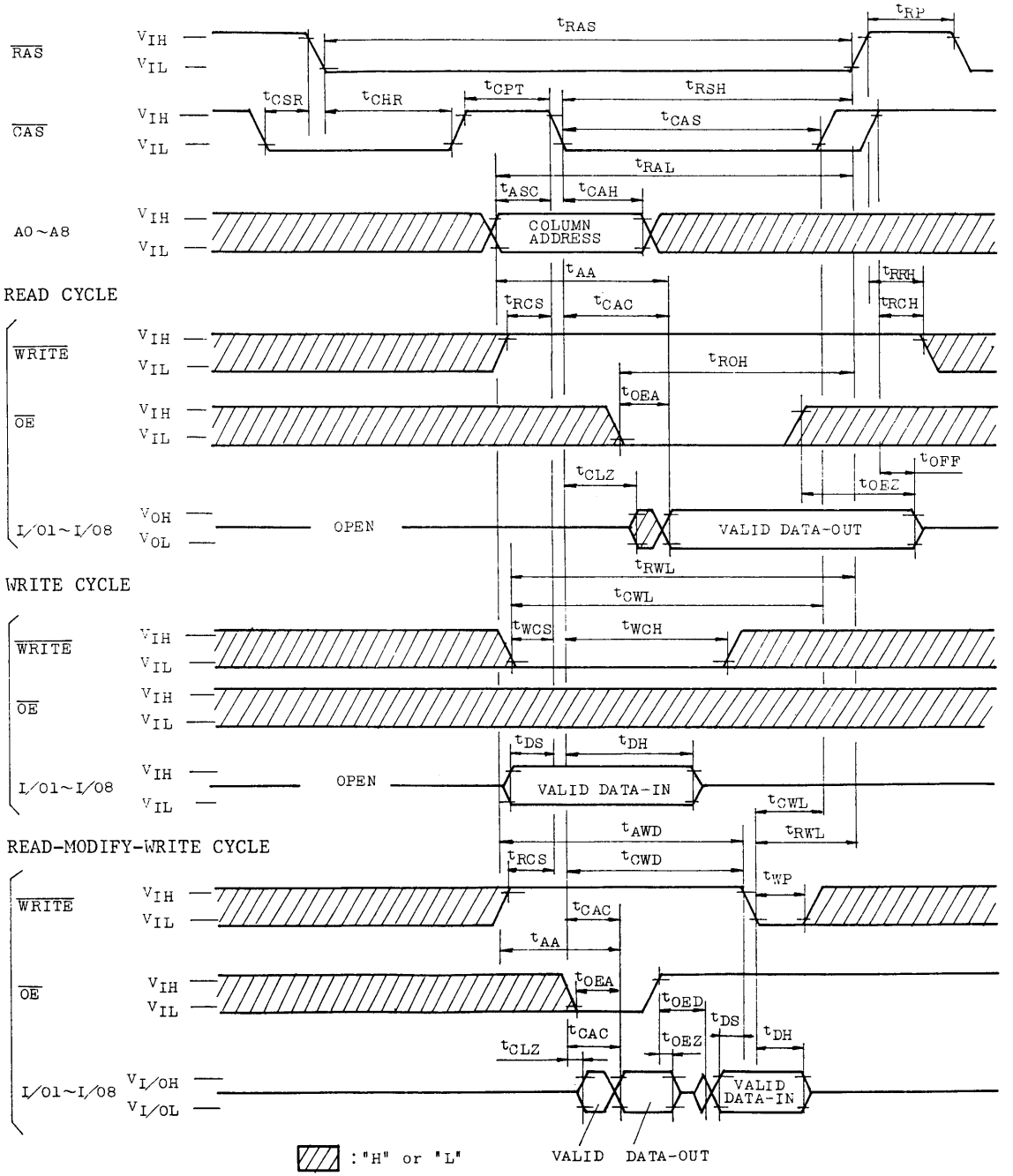
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



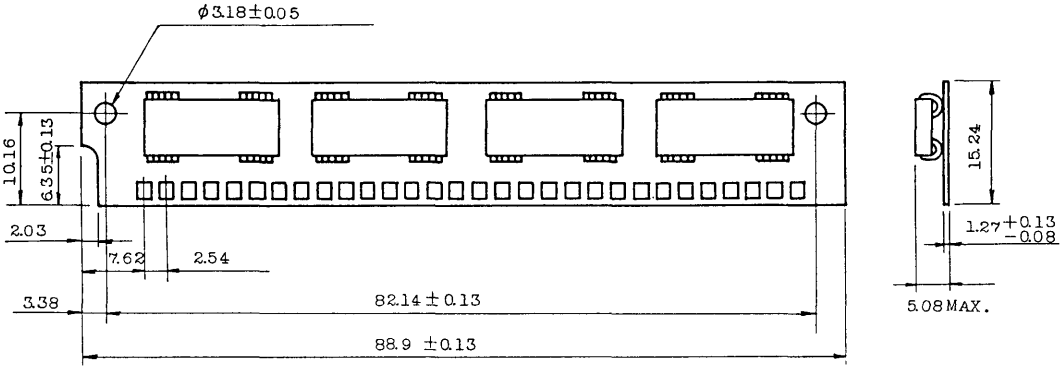
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



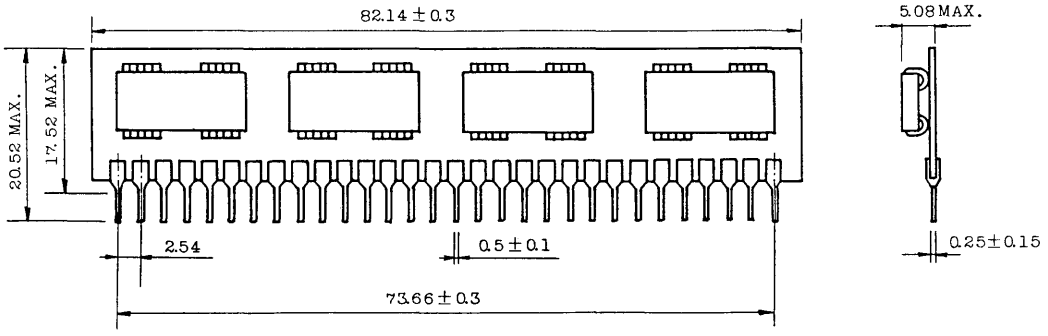
OUTLINE DRAWINGS

• THM8512S

Unit in mm



• THM8512L



524,288 WORDS×8 BIT DYNAMIC RAM MODULE
STATIC COLUMN MODE
DYNAMIC RAM MODULE

THM8514S/L-10,12

DESCRIPTION

The THM8514S/L is a 524,288 words by 8 bits dynamic RAM module which assembled 4 pcs of TC514258J on the printed circuit board.

The THM8514S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

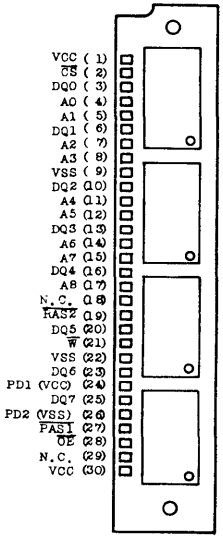
- 524,288 words by 8 bits organization
- Fast access time

		THM8514S/L-10	THM8514S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	100ns	120ns
t_{AA}	Column Address Access Time	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	55ns	65ns

- Single power supply of 5V ± 10%
- Low power
  737mW MAX. Operating (THM8514S/L-10)
  627mW MAX. Operating (THM8514S/L-12)
  22mW MAX. Standby
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

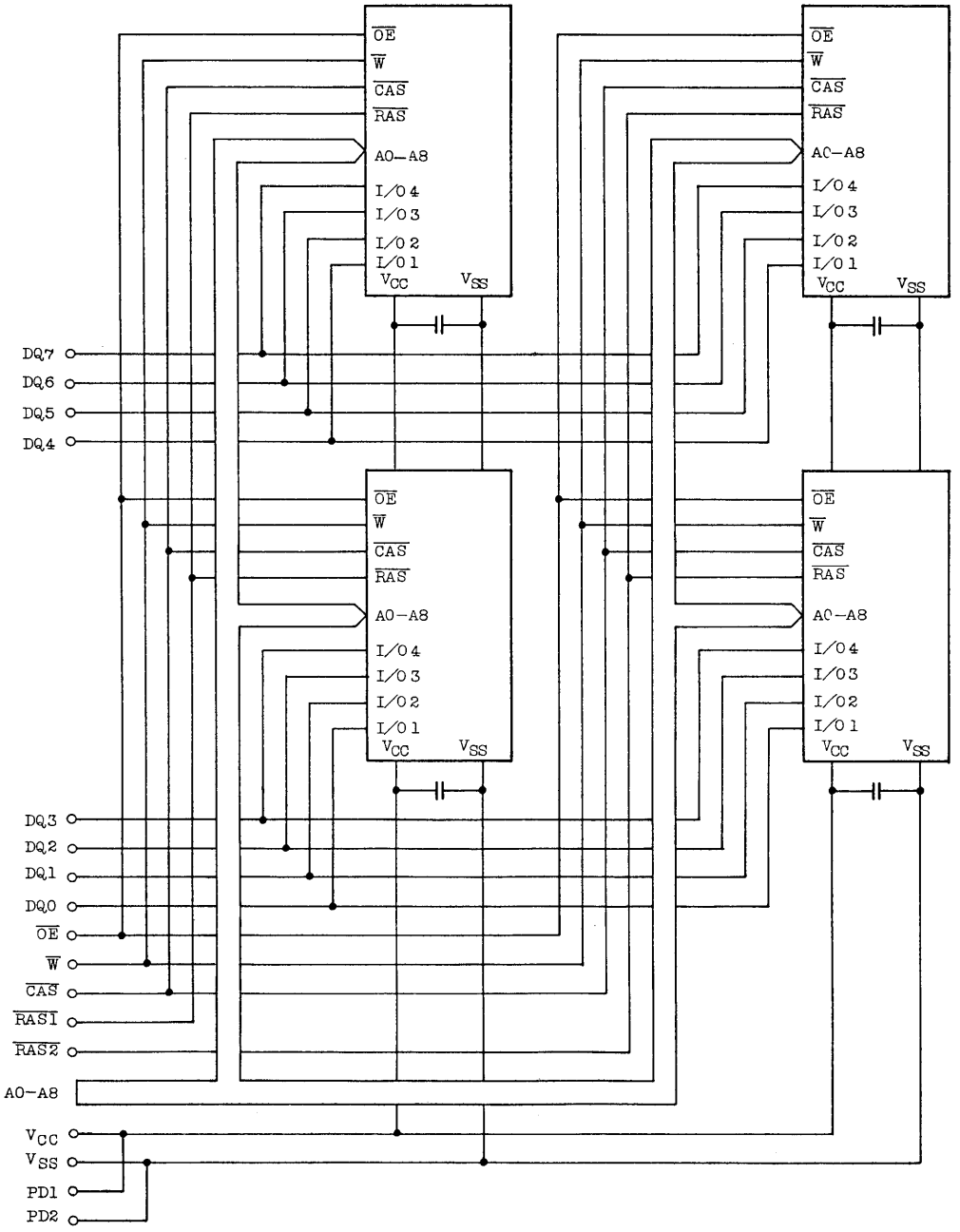
(TOP VIEW)



PIN NAMES

A0 ~ A8	Address Inputs
DQ0 ~ DQ7	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{CS}$	Chip Select Input
$\overline{RAS1}$, 2	Row Address Strobe
PD1	Presence Detect (Power)
PD2	Presence Detect (Ground)
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	2.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM8514S/L-10	-	134	mA	3, 4
		THM8514S/L-12	-	114		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	8	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFERSH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM8514S/L-10	-	260	mA	3
		THM8514S/L-12	-	220		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IL}, Address Cycling: t_{SC}=t_{SC} MIN.)	THM8514S/L-10	-	94	mA	3, 4
		THM8514S/L-12	-	74		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	4	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM8514S/L-10	-	260	mA	3
		THM8514S/L-12	-	220		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test=0V)		-40	40	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7, 17)

SYMBOL	PARAMETER	THM8514S/L-10		THM8514S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190	-	220	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	255	-	295	-	ns	
t_{SC}	Static Column Mode Cycle Time	55	-	65	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	115	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	100	-	120	ns	8, 13
t_{CAC}	Access Time from $\overline{CS}$	-	30	-	35	ns	8, 13
t_{AA}	Access Time from Column Address	-	50	-	60	ns	8, 14
t_{ALW}	Access Time from Last Write	-	95	-	115	ns	8, 15
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	35	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	30	-	35	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	30	100,000	35	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	70	25	85	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	20	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	15	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time Referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	50	-	60	-	ns	
t_{AH}	Column Address Hold Time Referenced to $\overline{RAS}$ Rise	10	-	15	-	ns	16
t_{LWAD}	Last Write to Column Address Delay Time	25	45	30	55	ns	15

SYMBOL	PARAMETER	THM8514S/L-10		THM8514S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{AHLW}	Last Write to Column Address Hold Time	95	-	115	-	ns	
t_{RCS}	Read Command Set-Up Time Referenced to $\overline{CS}$	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time Referenced to $\overline{CS}$	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{WP}	$\overline{WRITE}$ Pulse Width	20	-	25	-	ns	
t_{WI}	$\overline{WRITE}$ Inactive Time	10	-	15	-	ns	
t_{RWL}	$\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	25	-	30	-	ns	
t_{CWL}	$\overline{WRITE}$ Command to $\overline{CS}$ Lead Time	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	ms	
t_{WS}	$\overline{WRITE}$ Command Set-Up Time (Output Data Disable)	0	-	0	-	ns	12
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	65	-	75	-	ns	12
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	135	-	160	-	ns	12
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	85	-	100	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ counter Test Cycle)	50	-	60	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20	-	20	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	45	ns	
t_{OED}	$\overline{OE}$ to Data Delay	25	-	30	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	25	0	30	ns	9
t_{OEH}	$\overline{OE}$ Command Hold Time	25	-	30	-	ns	

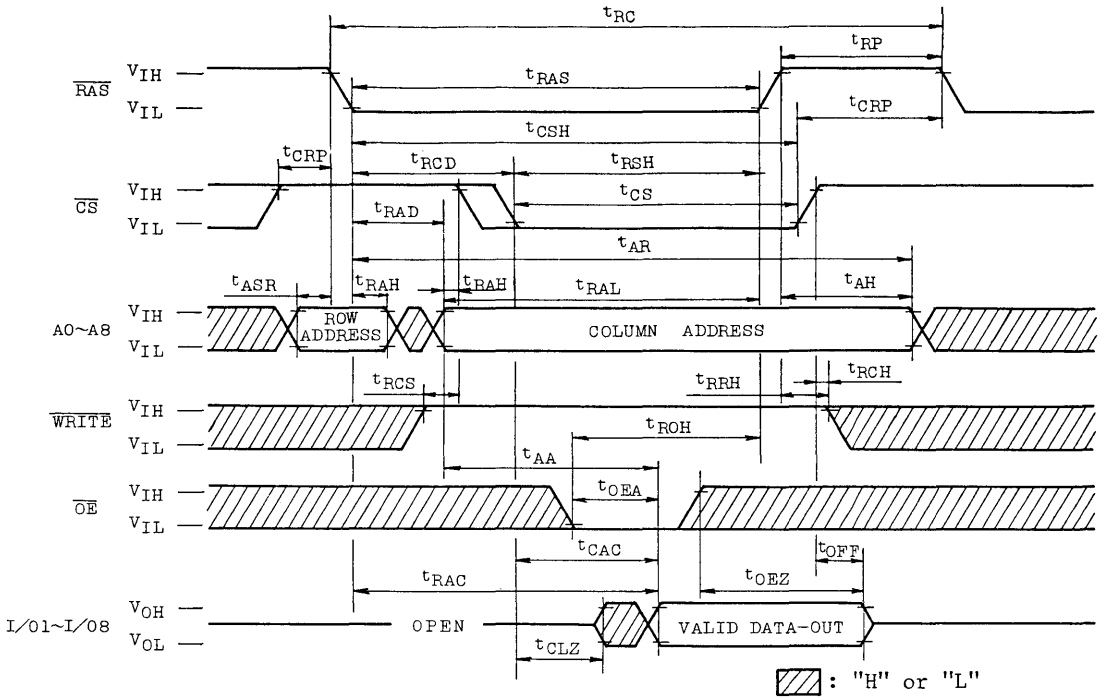
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A8, $\overline{W}$, $\overline{CS}$, $\overline{OE}$)	-	40	pF
C_{I2}	Input Capacitance ($\overline{RAS1}$, $\overline{RAS2}$)	-	20	
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)	-	20	

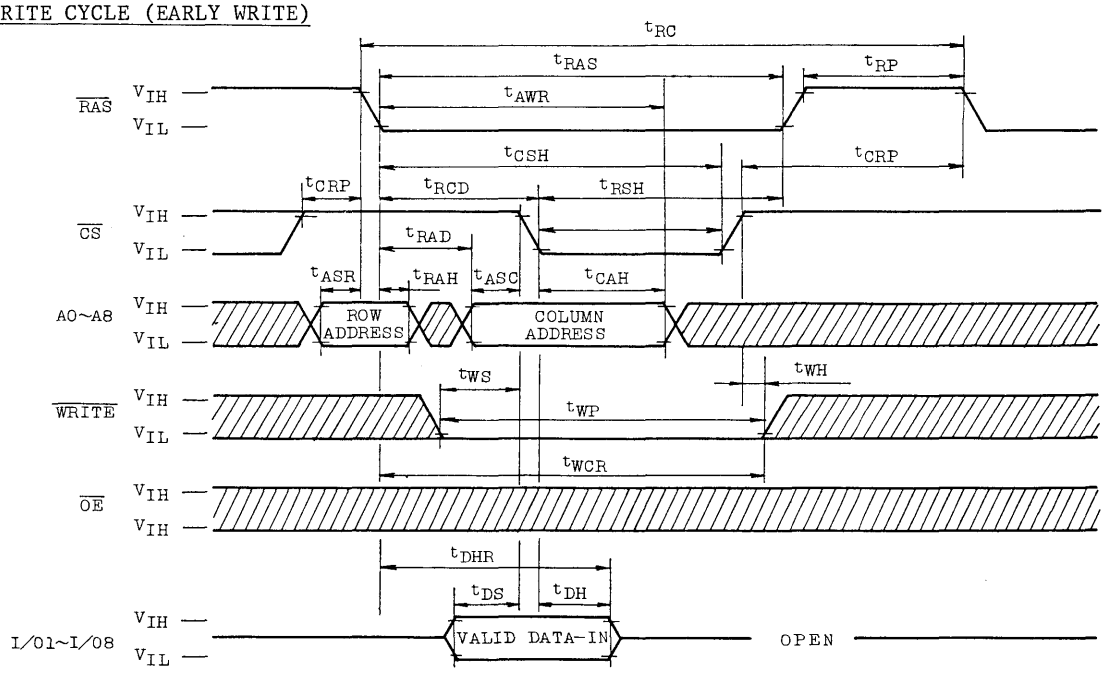
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
12. t_{WS}, t_{WH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$(min.), $t_{CWD} \geqq t_{CWD}$(min.) and $t_{AWD} \geqq t_{AWD}$(min.), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is contorolled by t_{AA}.
15. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
16. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.
17. To prevent from the bus contention, please avoid such timing that both $\overline{RAS1}$ and $\overline{RAS2}$ are activation.

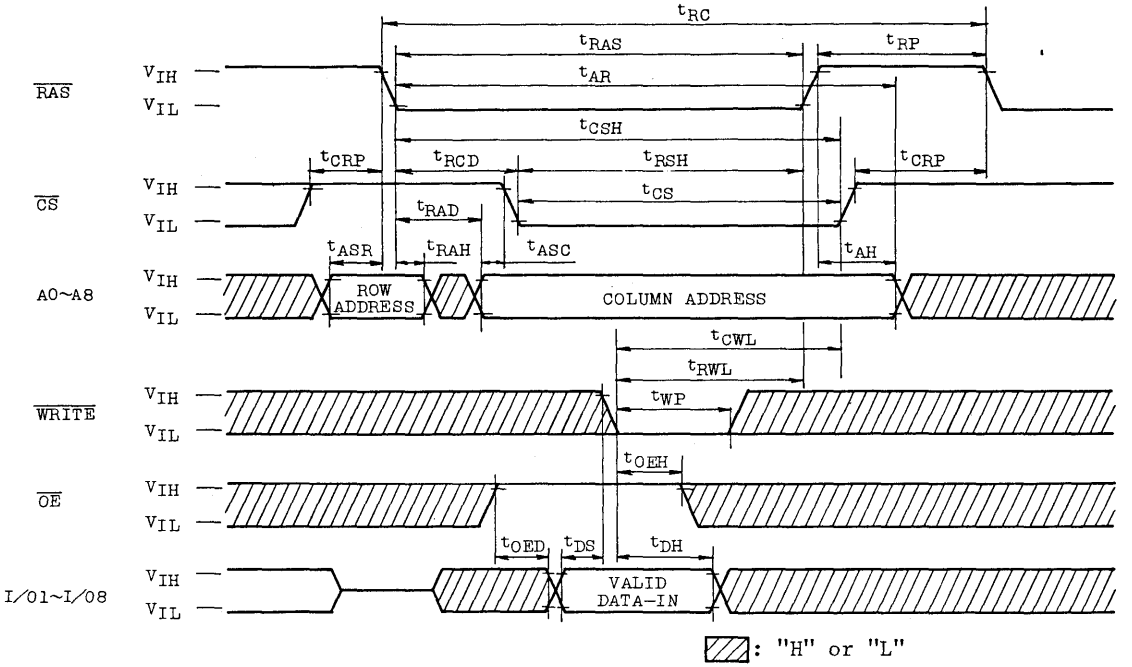
READ CYCLE



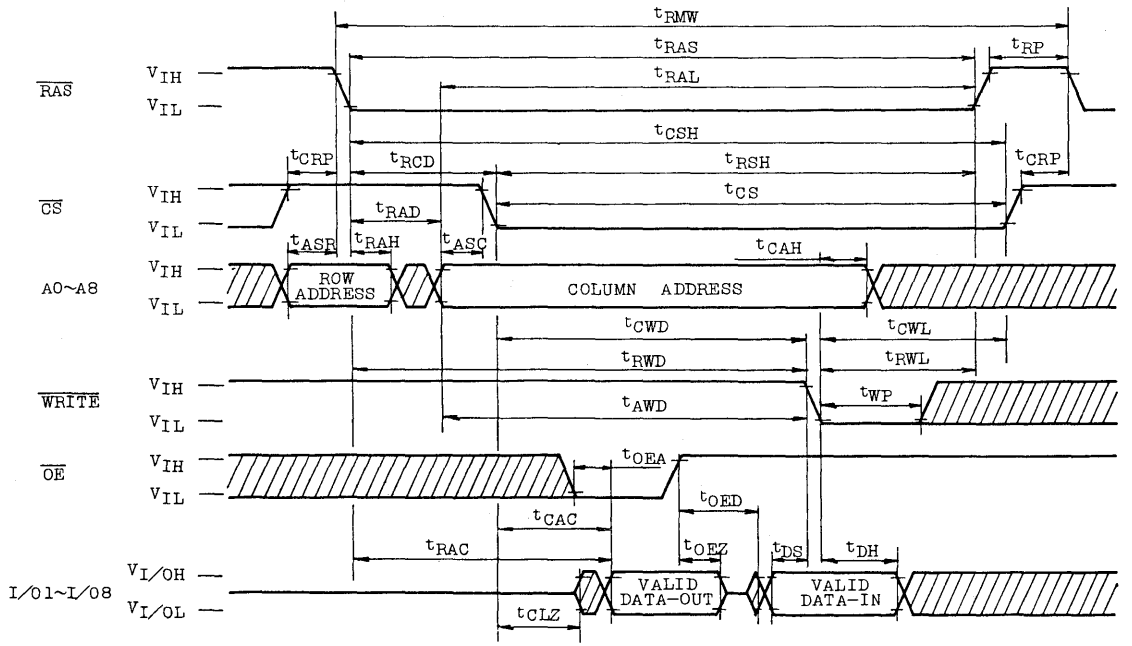
WRITE CYCLE (EARLY WRITE)



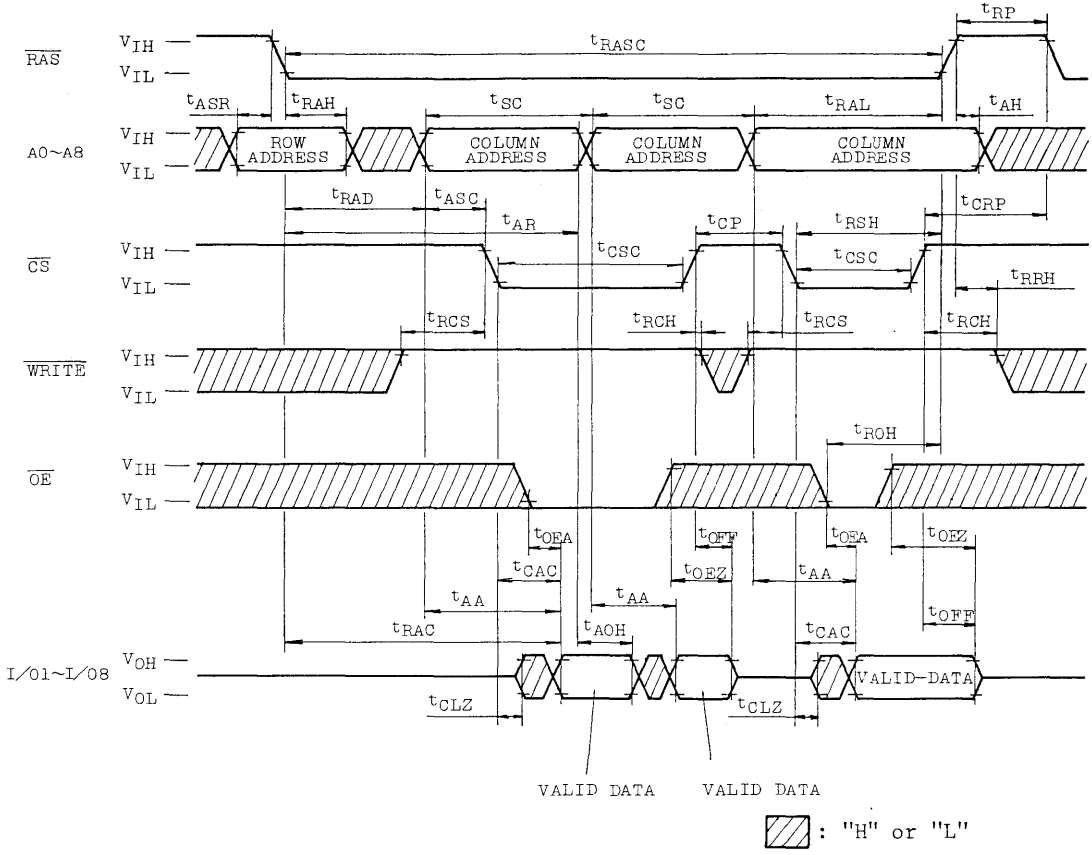
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



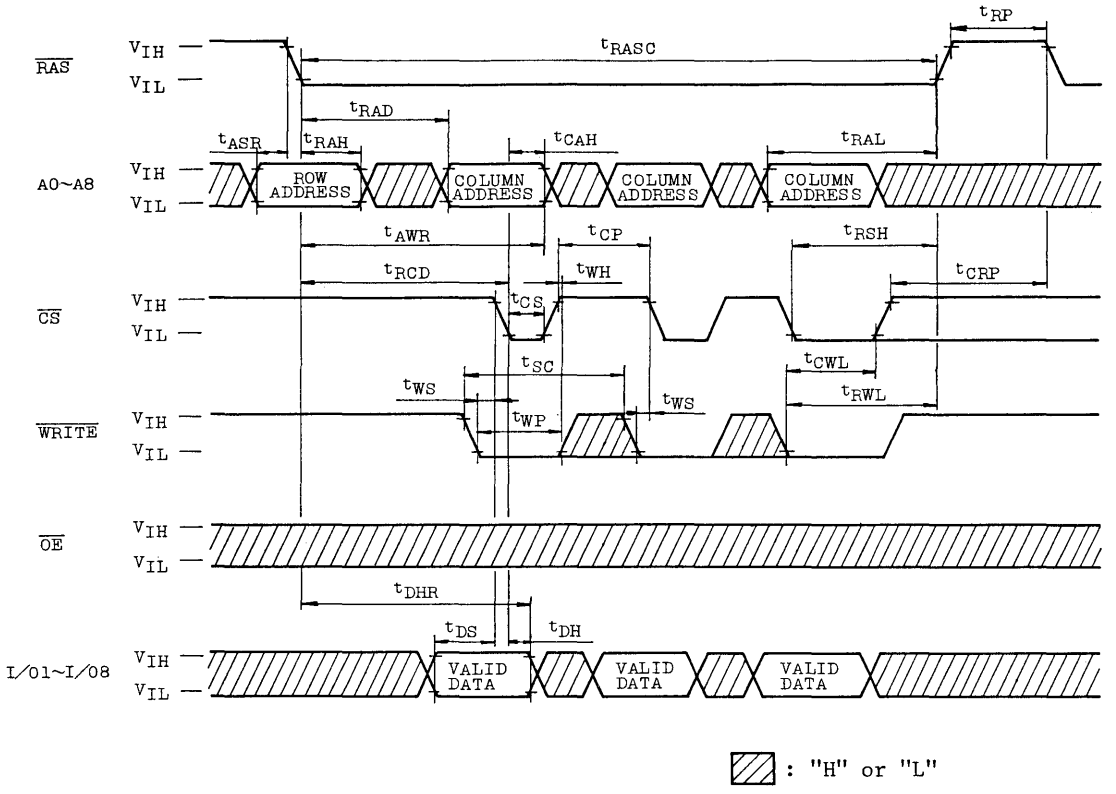
READ-MODIFY-WRITE CYCLE



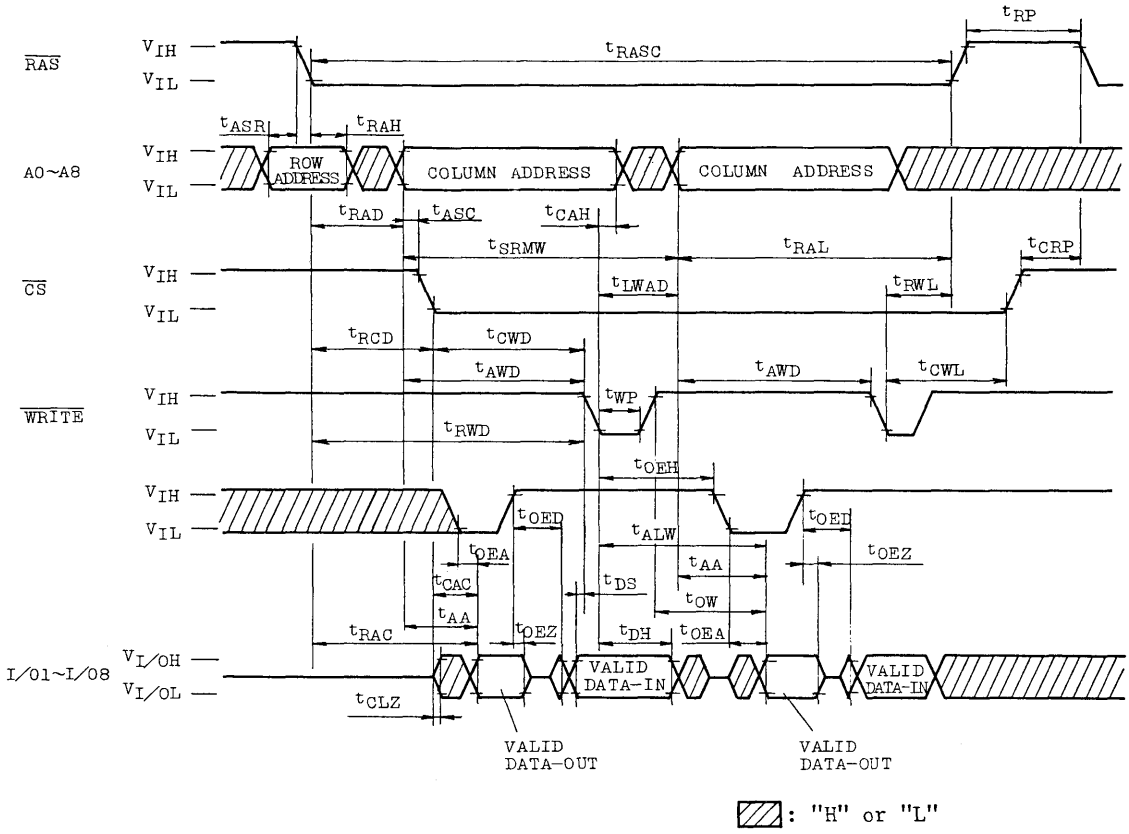
STATIC COLUMN MODE READ CYCLE



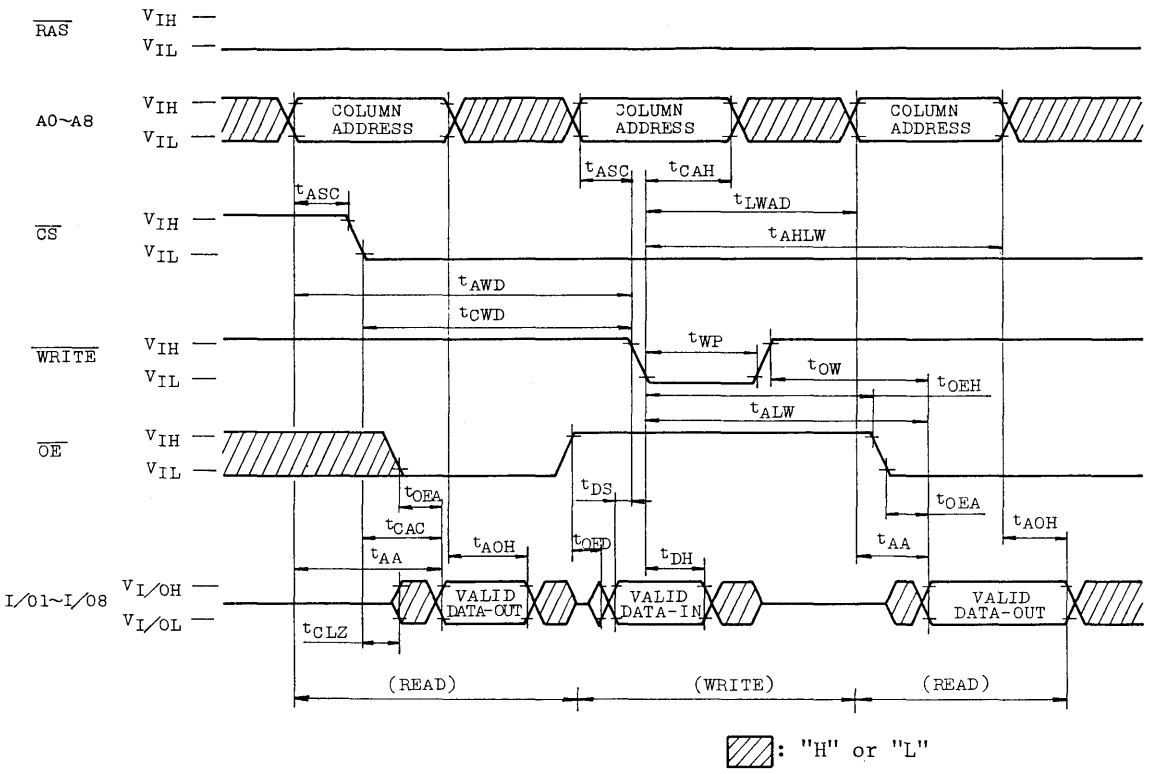
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



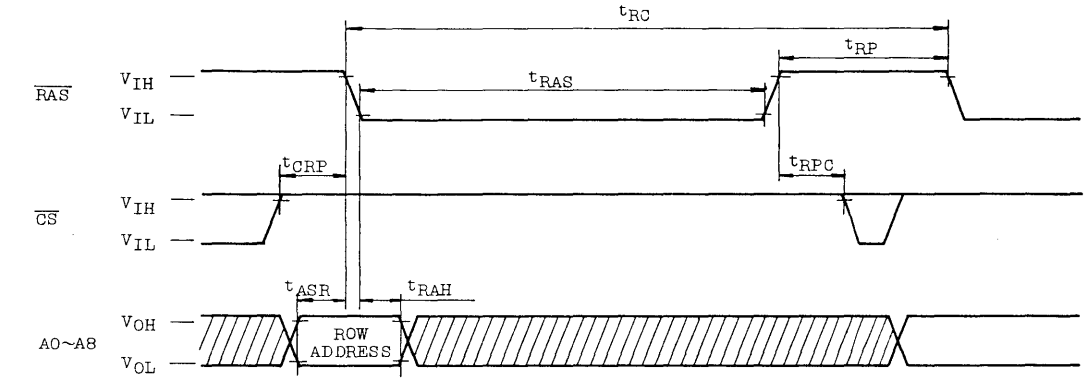
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



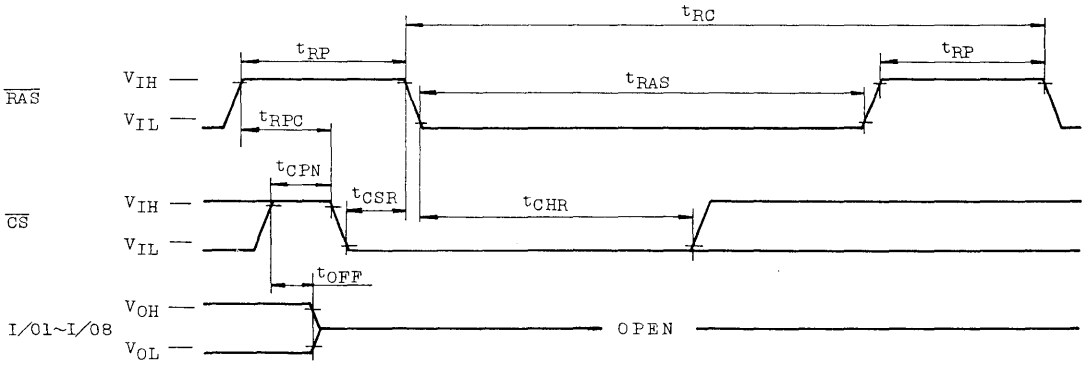
$\overline{RAS}$ ONLY REFRESH CYCLE



Notes: $\overline{WRITE}$, $\overline{OE}$: "H" or "L"

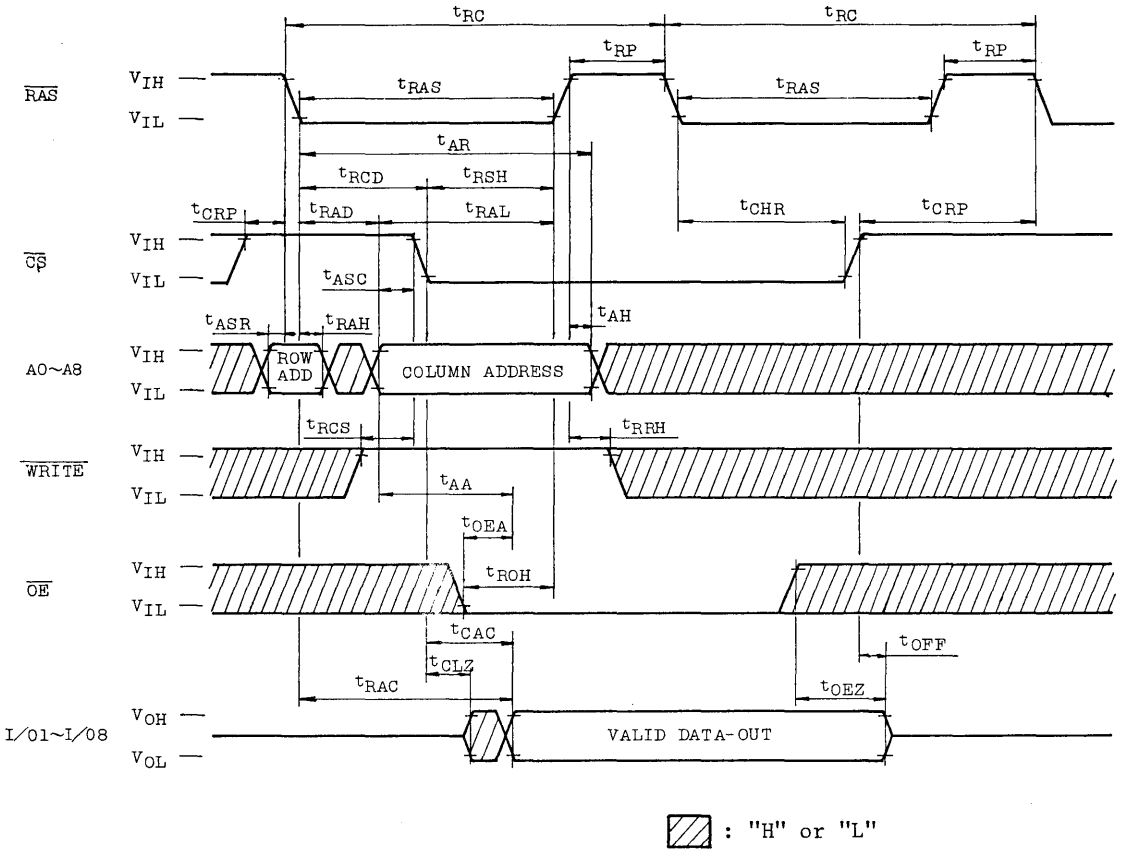
▨: "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

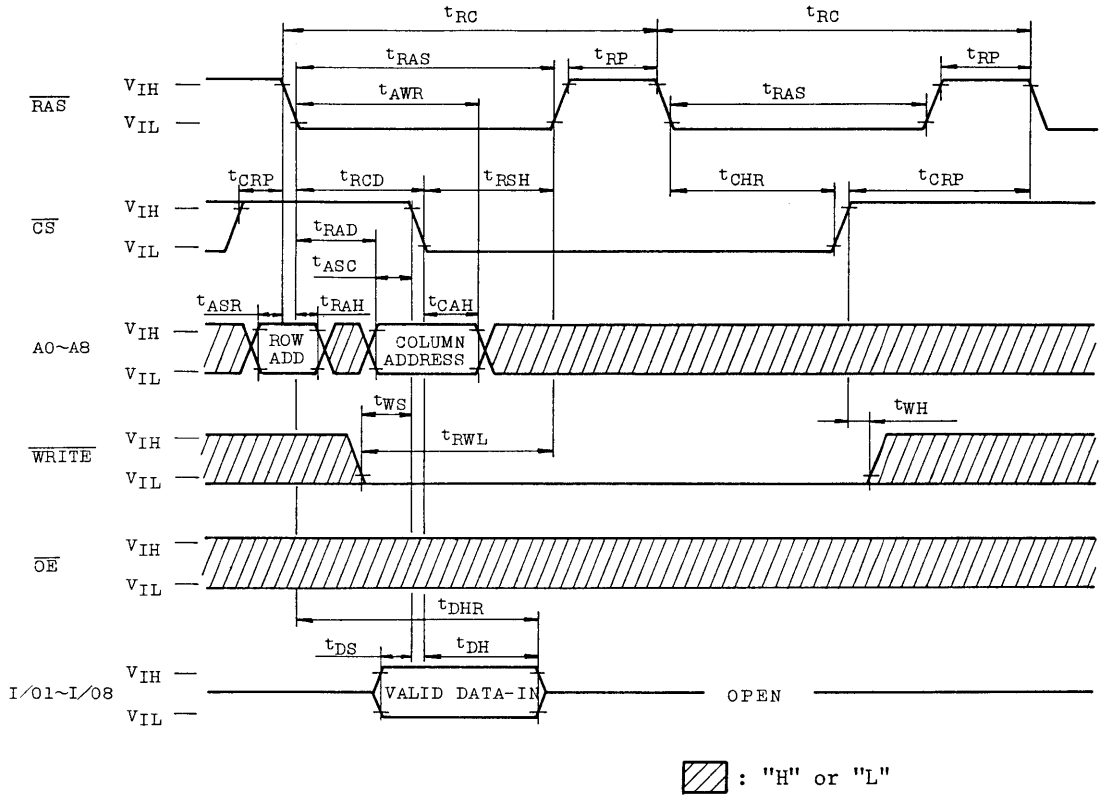


Notes: $\overline{WRITE}$, $\overline{OE}$, A0 ∿ A8: "H" or "L"

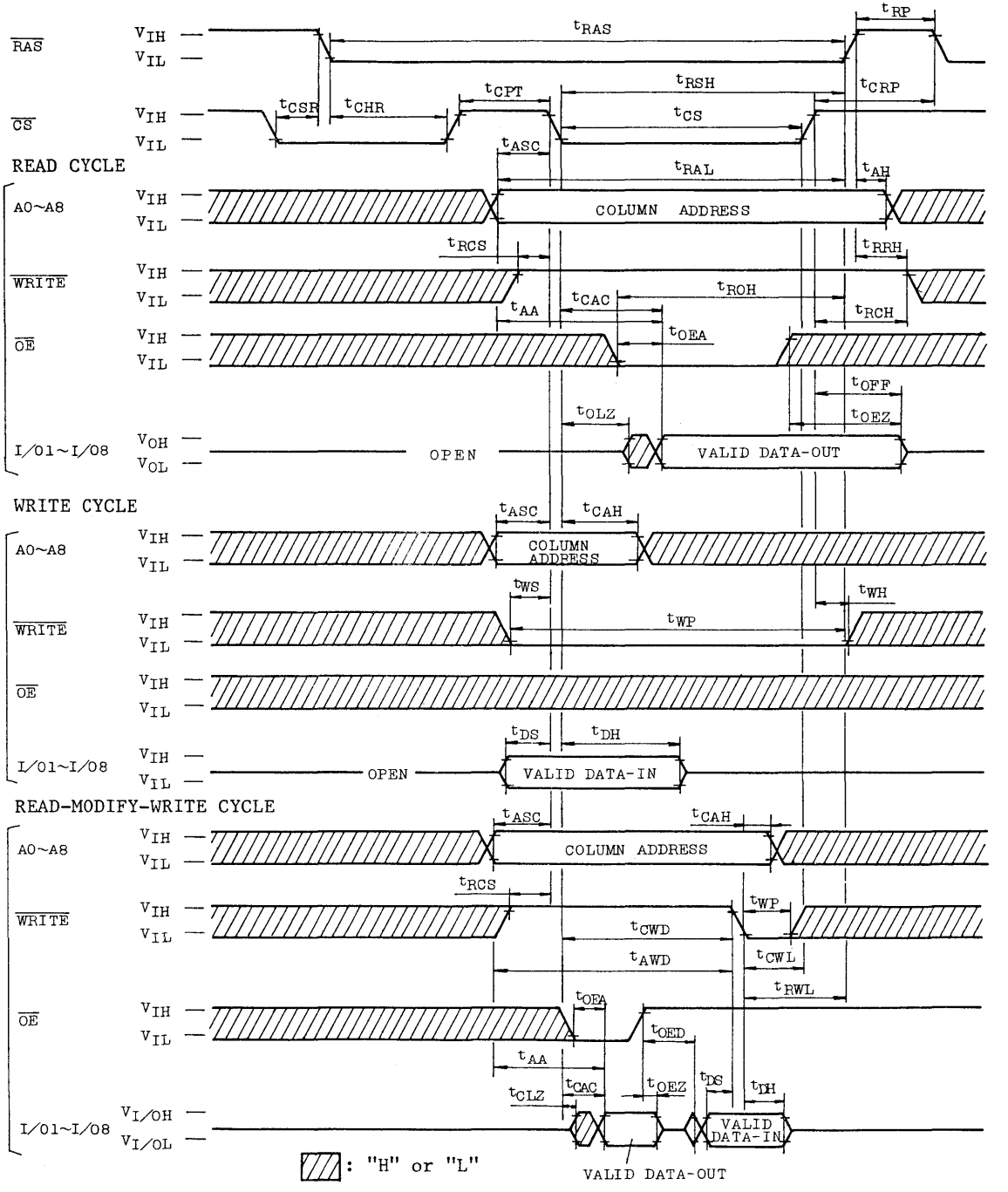
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



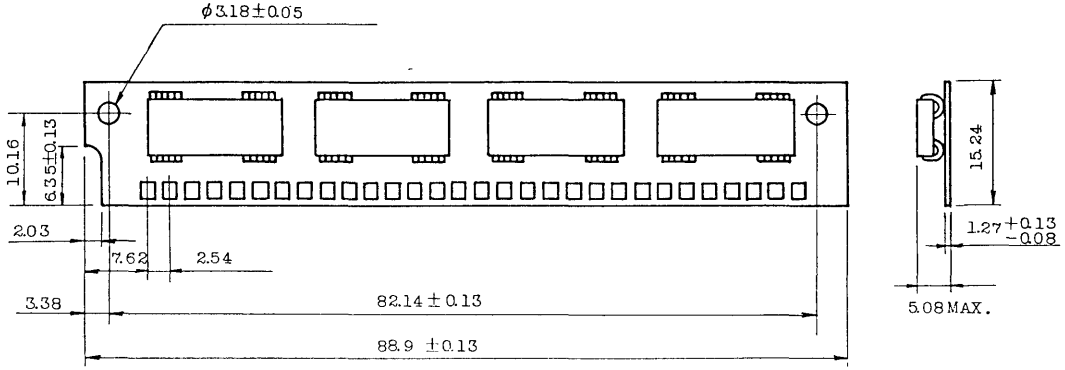
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



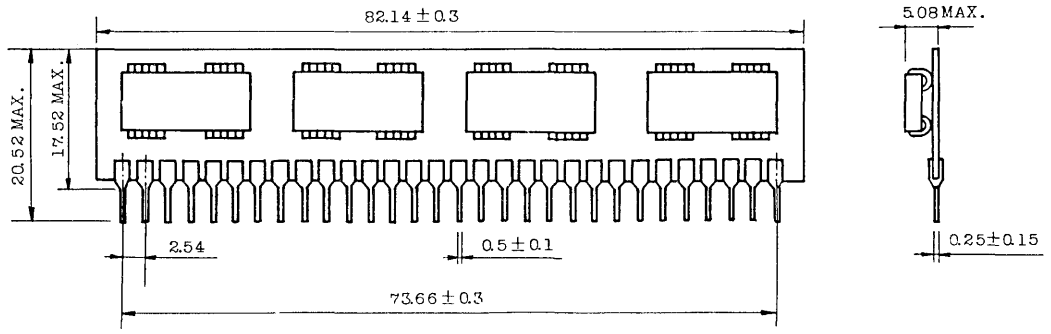
OUTLINE DRAWINGS

• THM8514S

Unit in mm



• THM8514L



THM81000S/L-85, 10, 12

DESCRIPTION

The THM81000S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000J on the printed circuit board.

The THM81000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

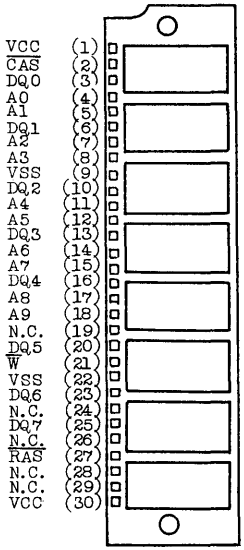
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81000S/L-85	THM81000S/L-10	THM81000S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V±10%
- Low power 3,080mW MAX. Operating (THM81000S/L-85)
  2,640mW MAX. Operating (THM81000S/L-10)
  2,200mW MAX. Operating (THM81000S/L-12)
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

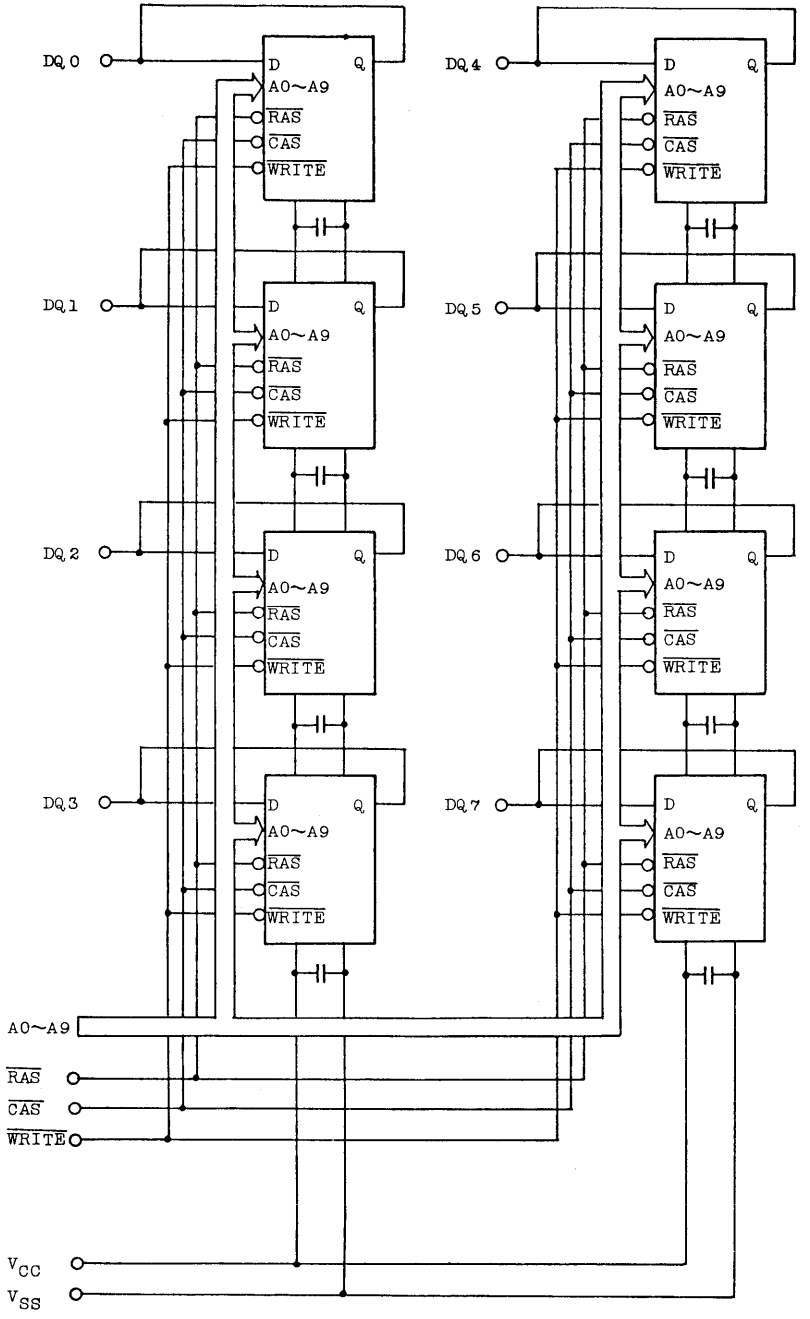
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature . Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-85	-	560	mA	3, 4
		THM81000S/L-10	-	480		
		THM81000S/L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81000S/L-85	-	560	mA	3
		THM81000S/L-10	-	480		
		THM81000S/L-12	-	400		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM81000S/L-85	-	400	mA	3, 4
		THM81000S/L-10	-	320		
		THM81000S/L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)			8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81000S/L-85	-	560	mA	3
		THM81000S/L-10	-	480		
		THM81000S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81000S/L-85		THM81000S/L-10		THM81000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81000S/L-85		THM81000S/L-10		THM81000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Referesh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

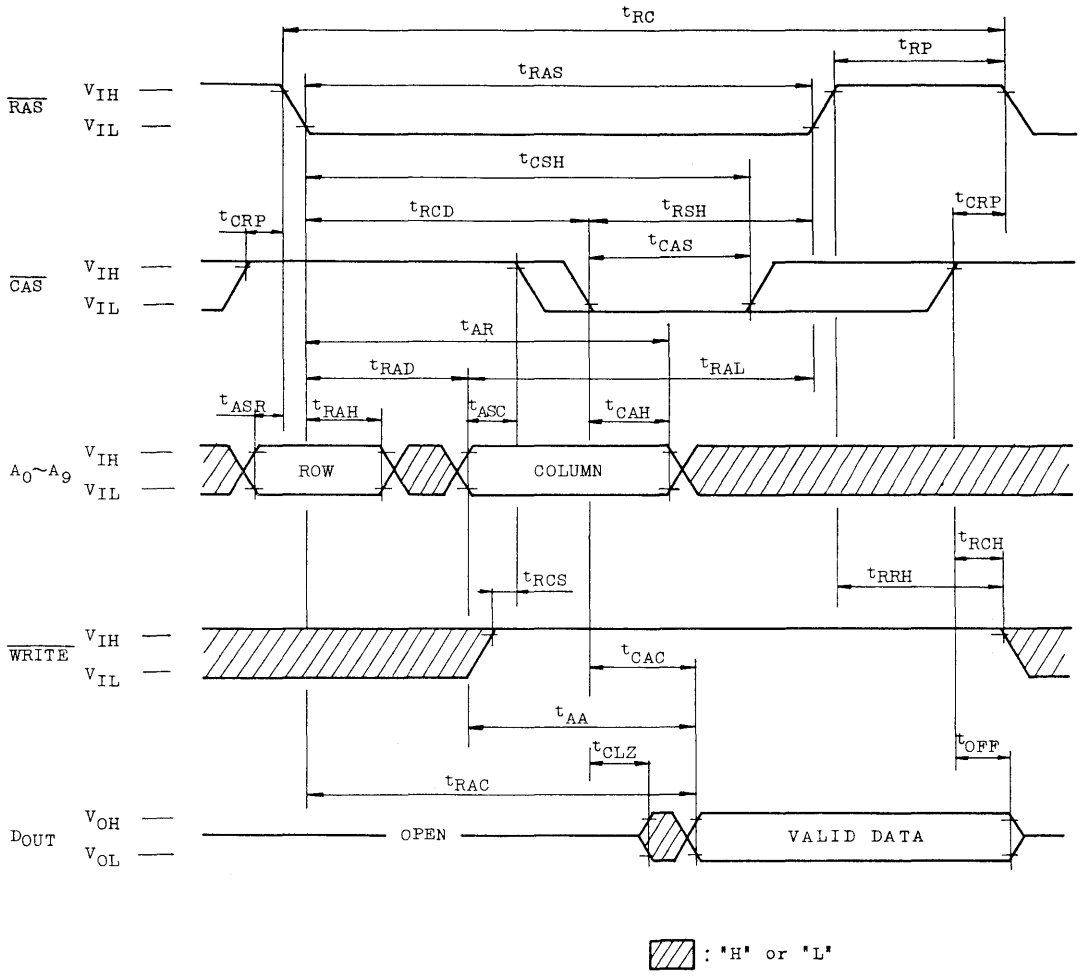
11. These parameters are referenced to $\overline{CAS}$ leading edge.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

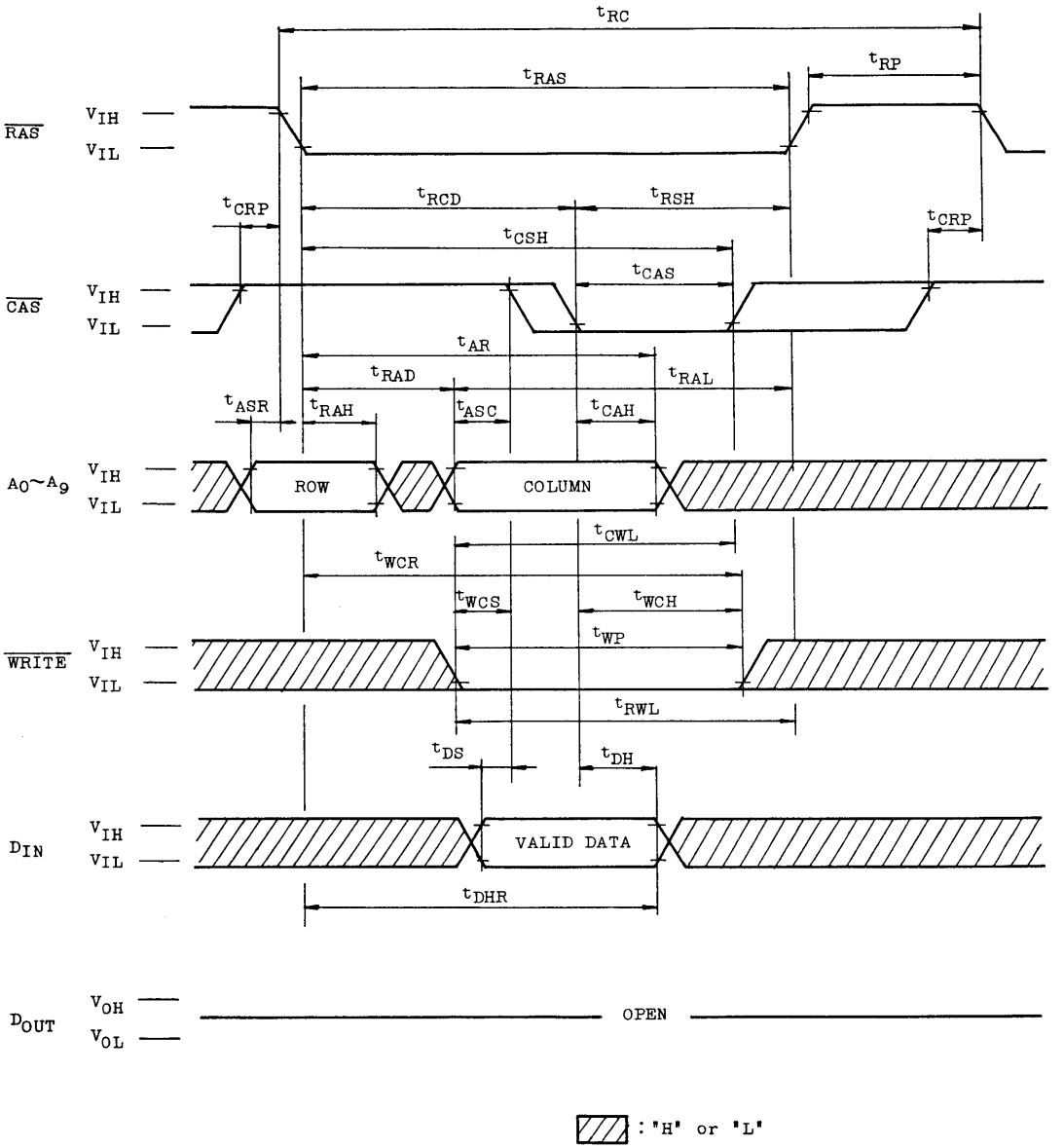
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

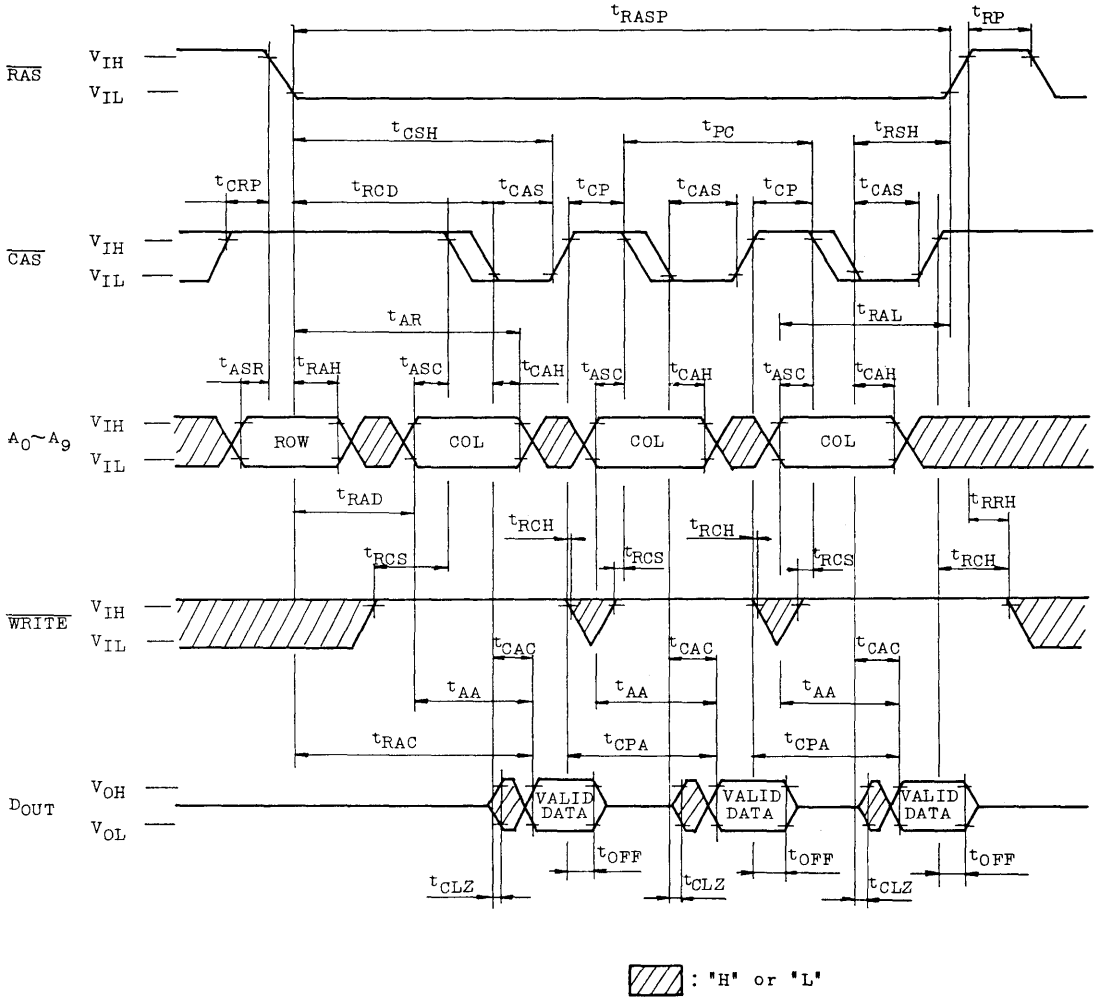
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"

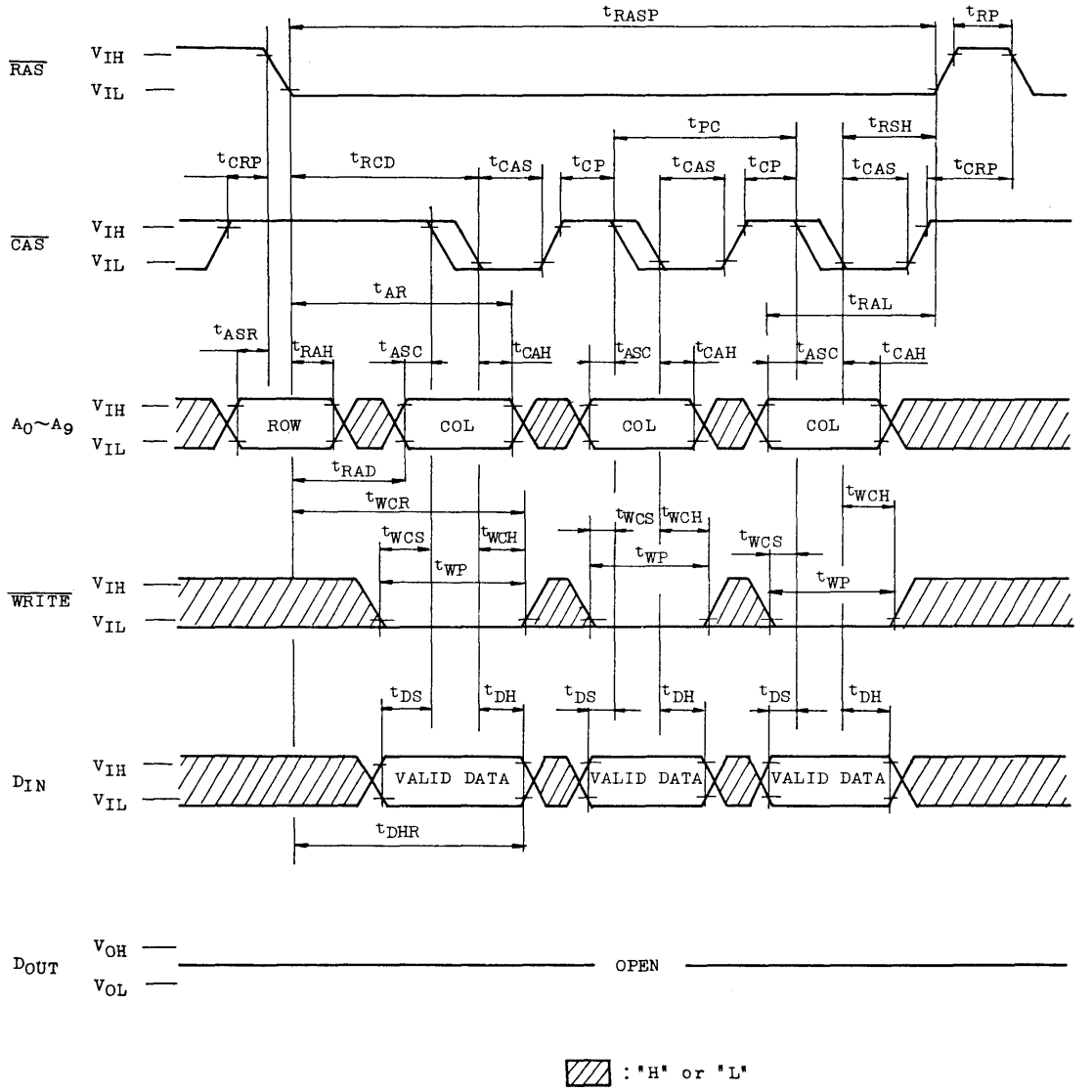
EARLY WRITE CYCLE



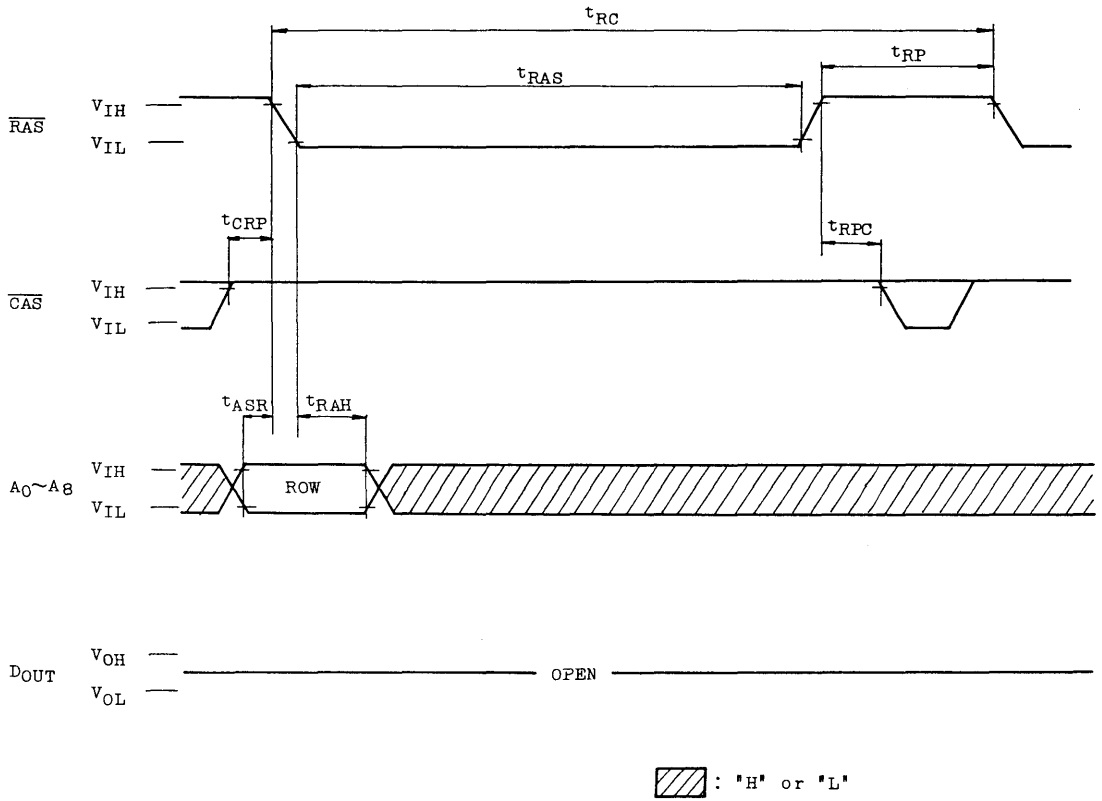
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

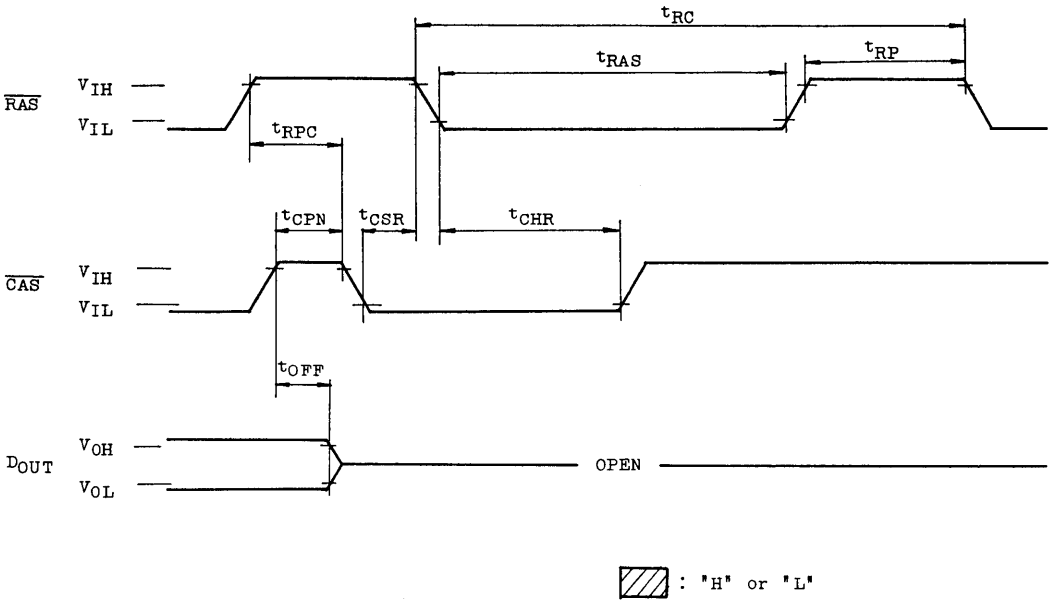


$\overline{RAS}$ ONLY REFRESH CYCLE



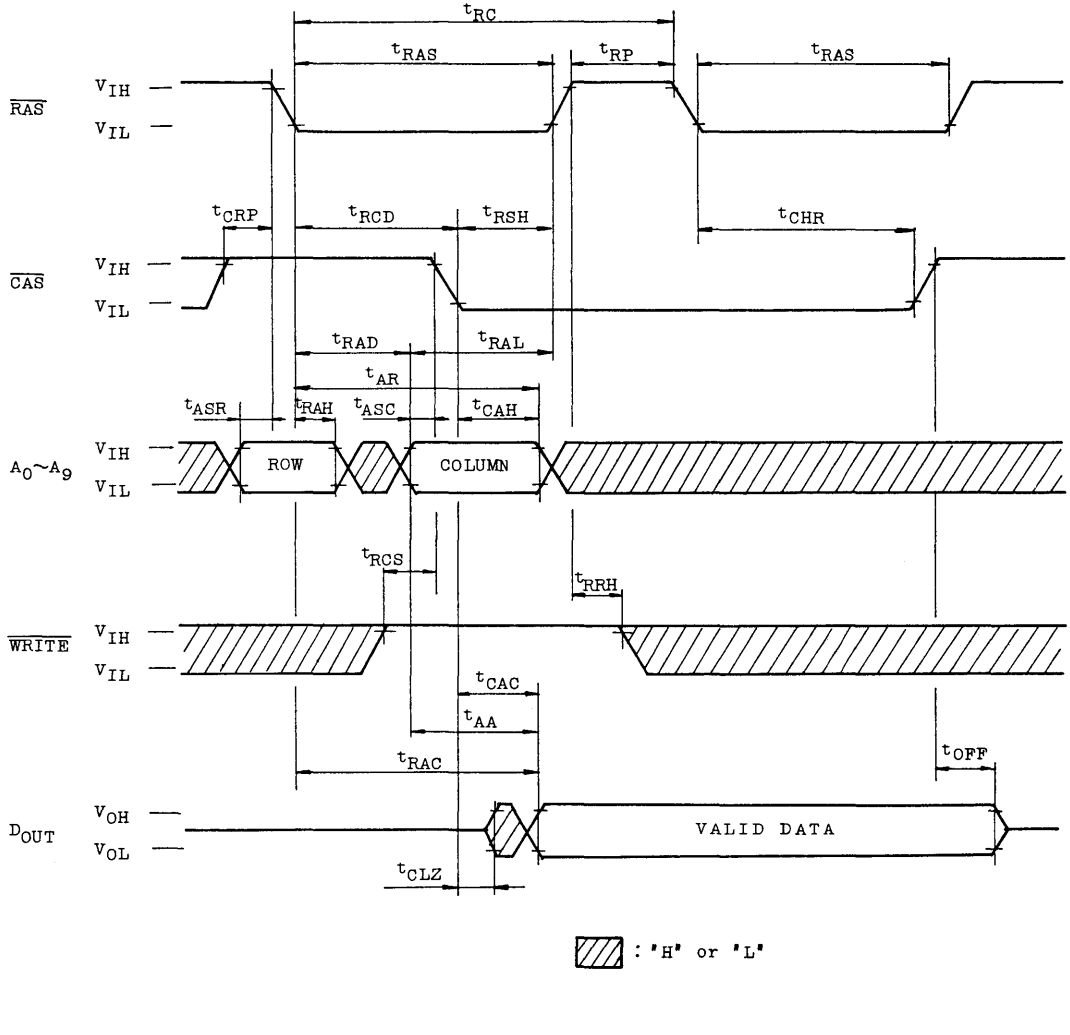
Note: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

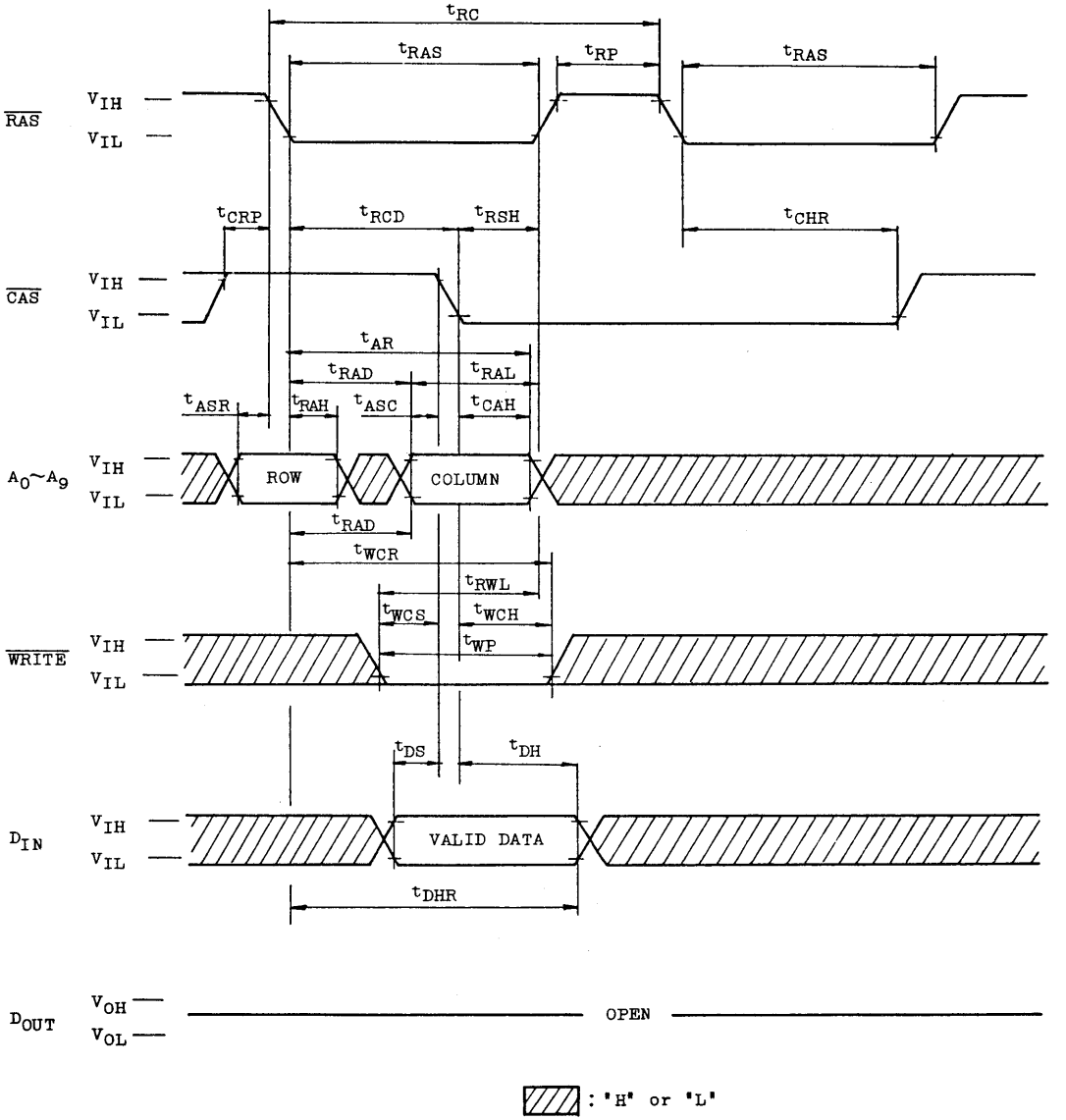


Note: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

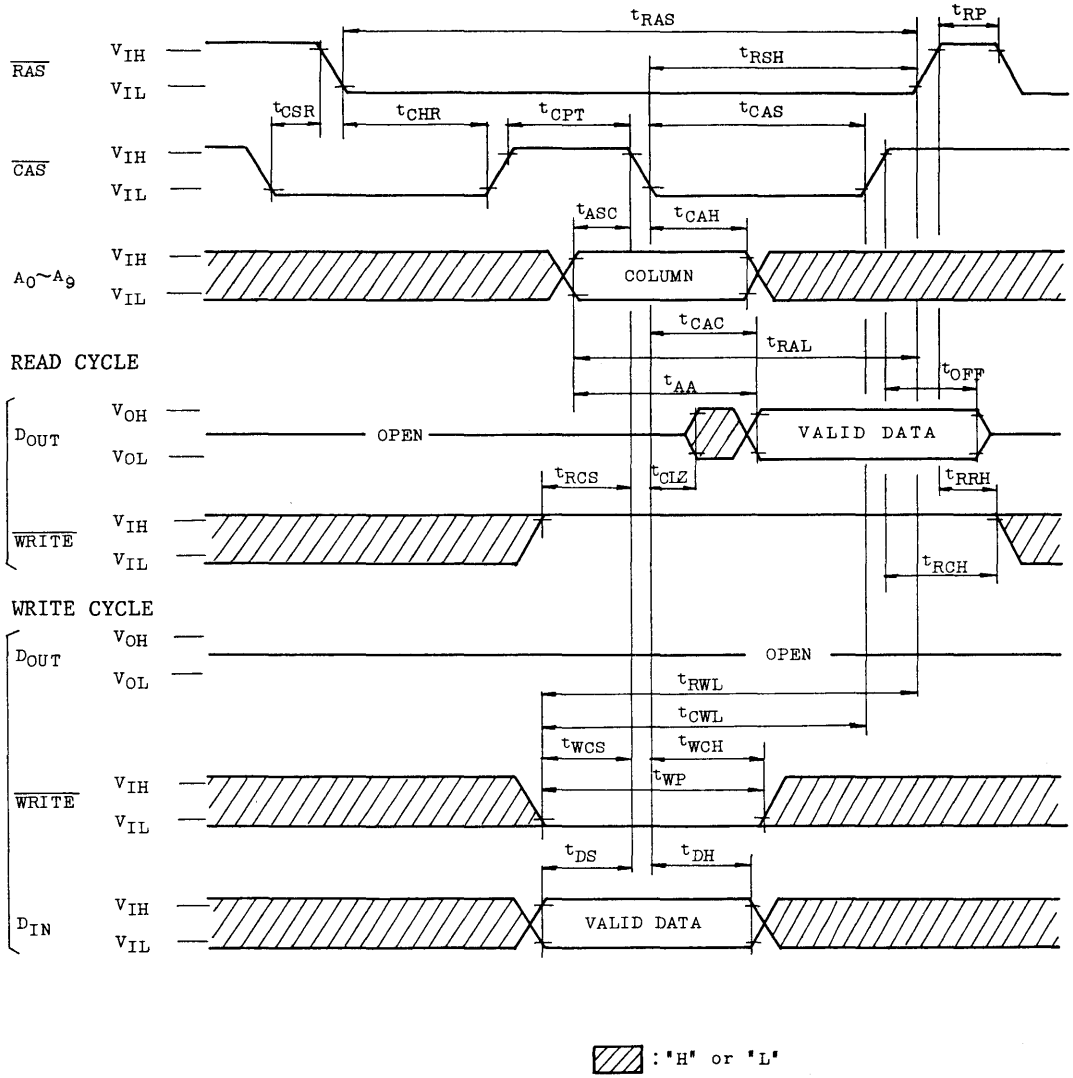
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



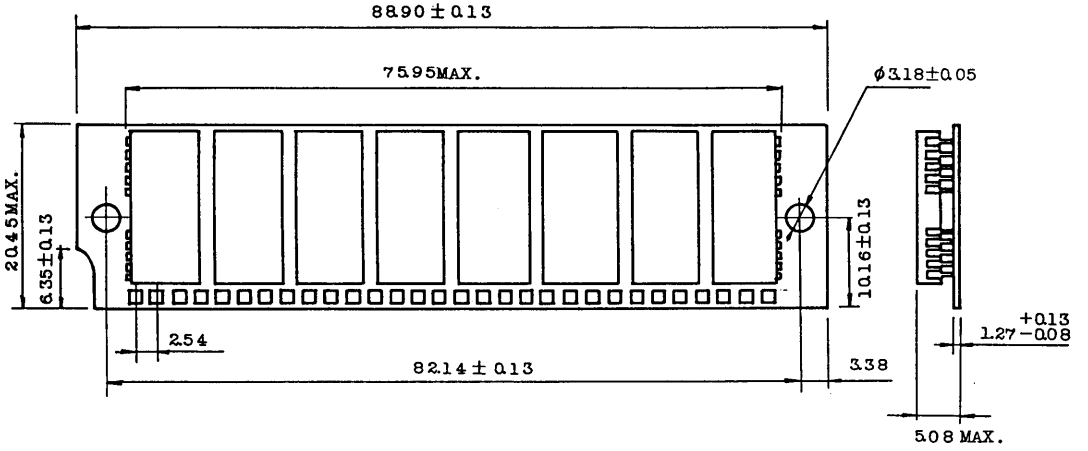
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



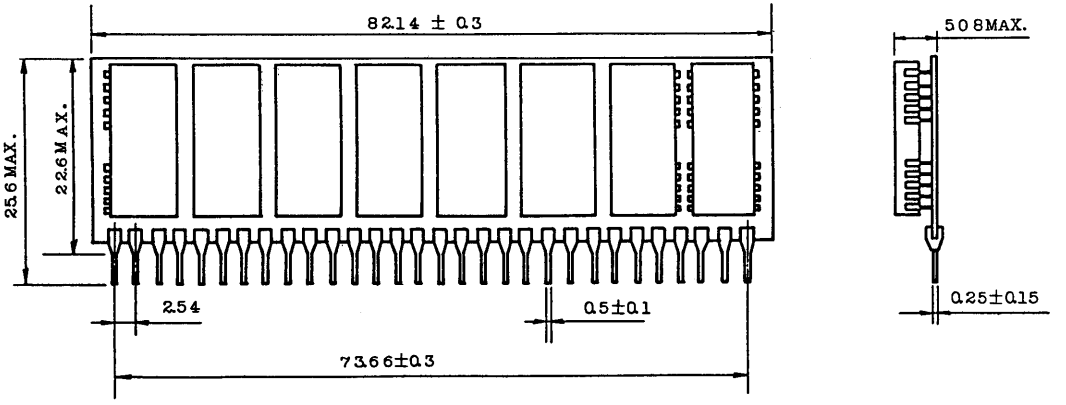
OUTLINE DRAWINGS

• THM81000S

Unit in mm



• THM81000L



THM81001S/L-85, 10, 12

DESCRIPTION

The THM81001S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511001J on the printed circuit board.

The THM81001S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

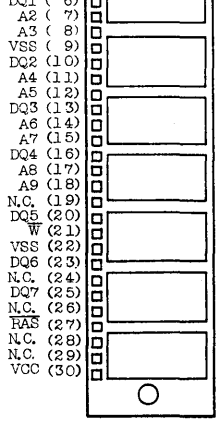
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81001S/L-85	THM81001S/L-10	THM81001S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

- Single power supply of 5V±10%
- Low power
  - 3,080mW MAX. Operating (THM81001S/L-85)
  - 2,640mW MAX. Operating (THM81001S/L-10)
  - 2,200mW MAX. Operating (THM81001S/L-12)
  - 44mW MAX. Standby
- CAS before RAS refresh, RAS only refresh, Hidden refresh, and Nibble Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

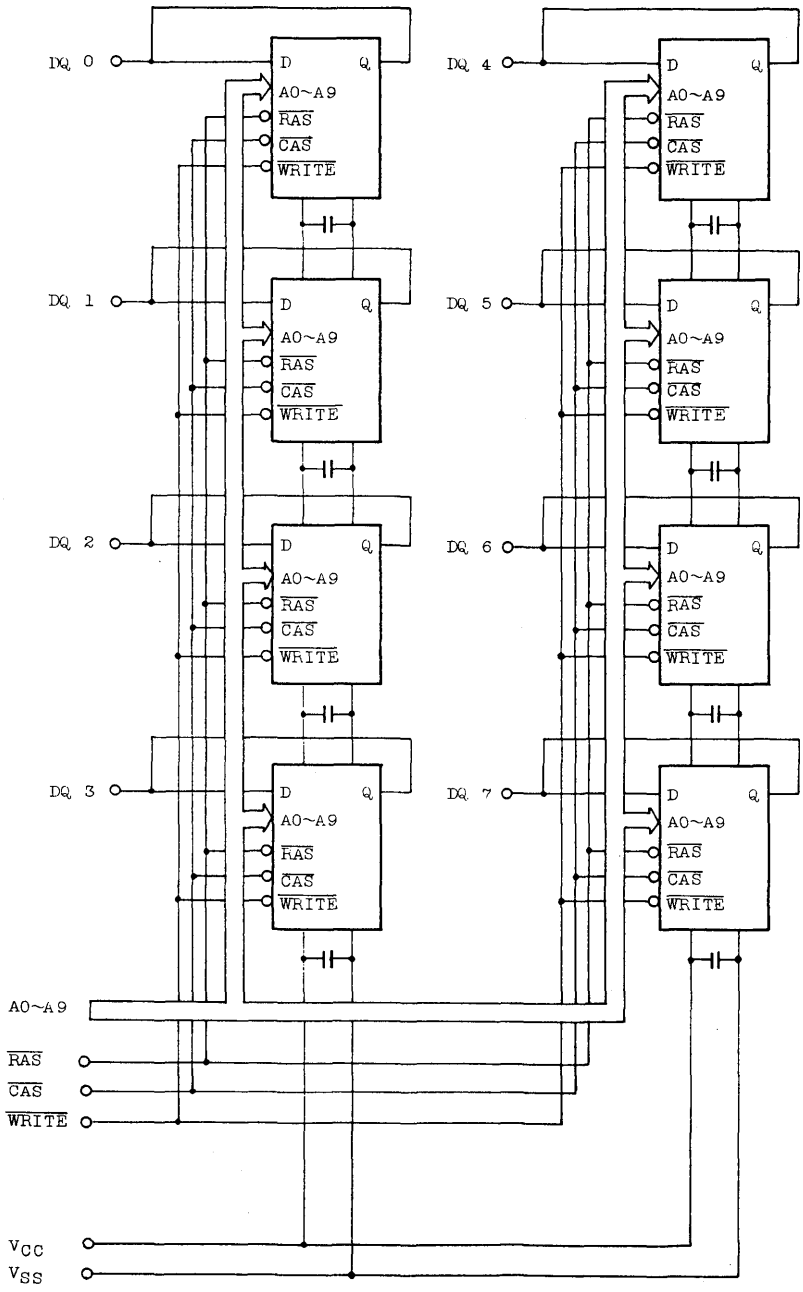
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81001S/L-85	-	560	mA	3, 4
		THM81001S/L-10	-	480		
		THM81001S/L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81001S/L-85	-	560	mA	3
		THM81001S/L-10	-	480		
		THM81001S/L-12	-	400		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	THM81001S/L-85	-	400	mA	3, 4
		THM81001S/L-10	-	320		
		THM81001S/L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81001S/L-85	-	560	mA	3
		THM81001S/L-10	-	480		
		THM81001S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81001S/L-85		THM81001S/L-10		THM81001S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81001S/L-85		THM81001S/L-10		THM81001S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	

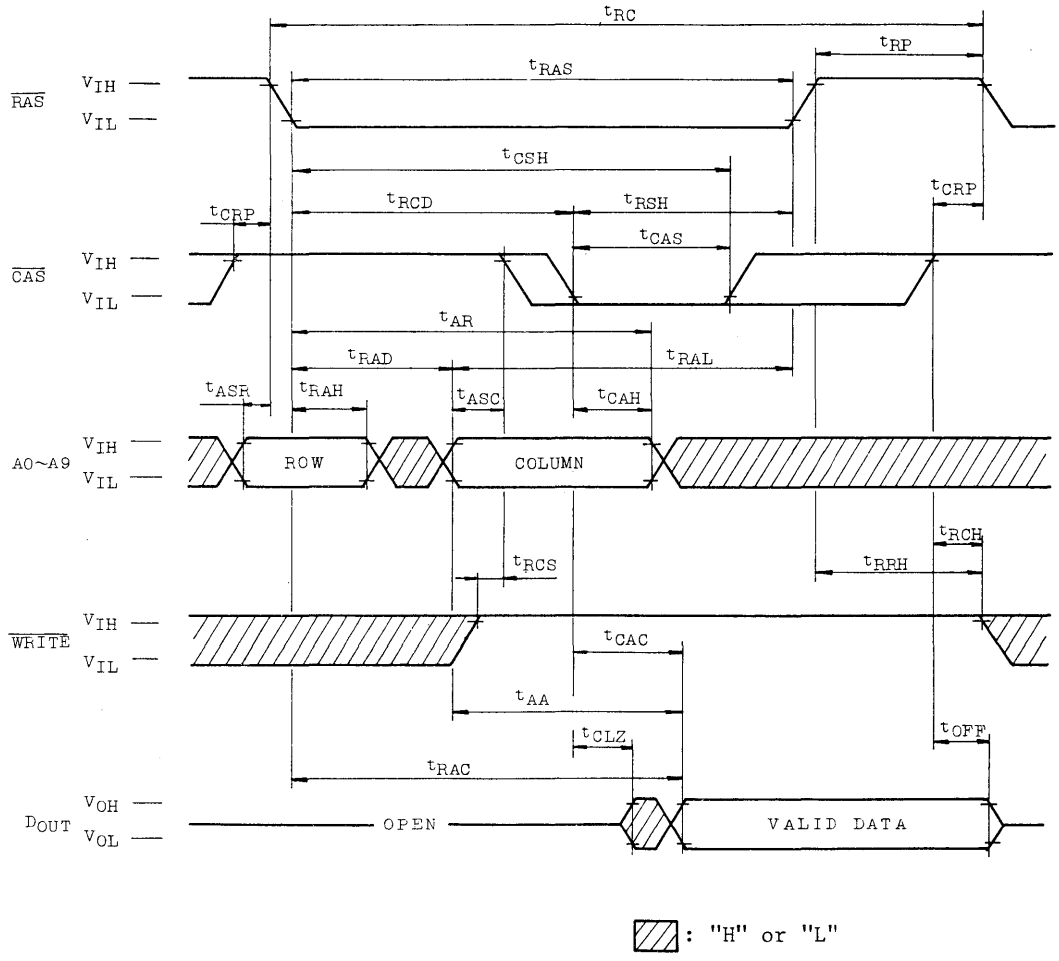
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF

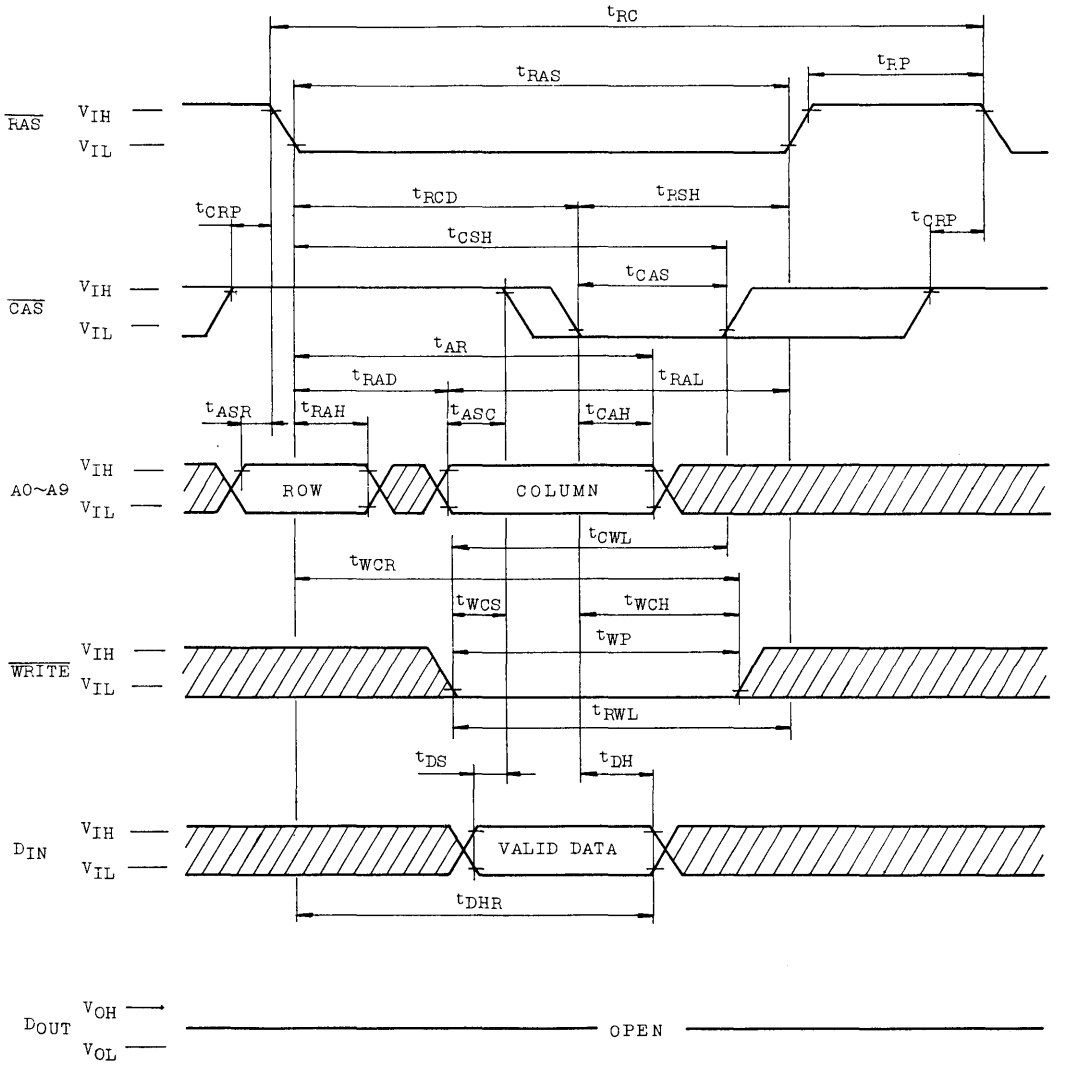
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(MAX.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

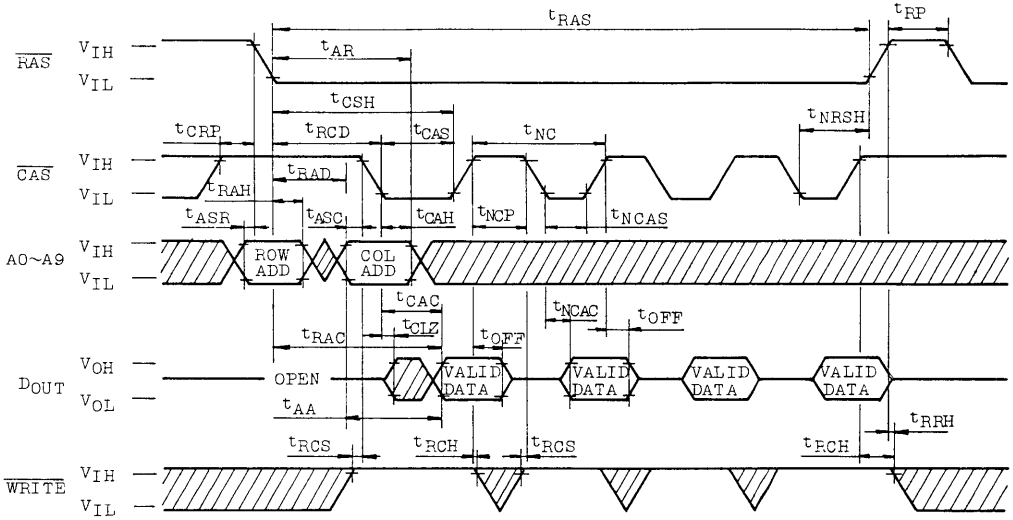

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"

EARLY WRITE CYCLE

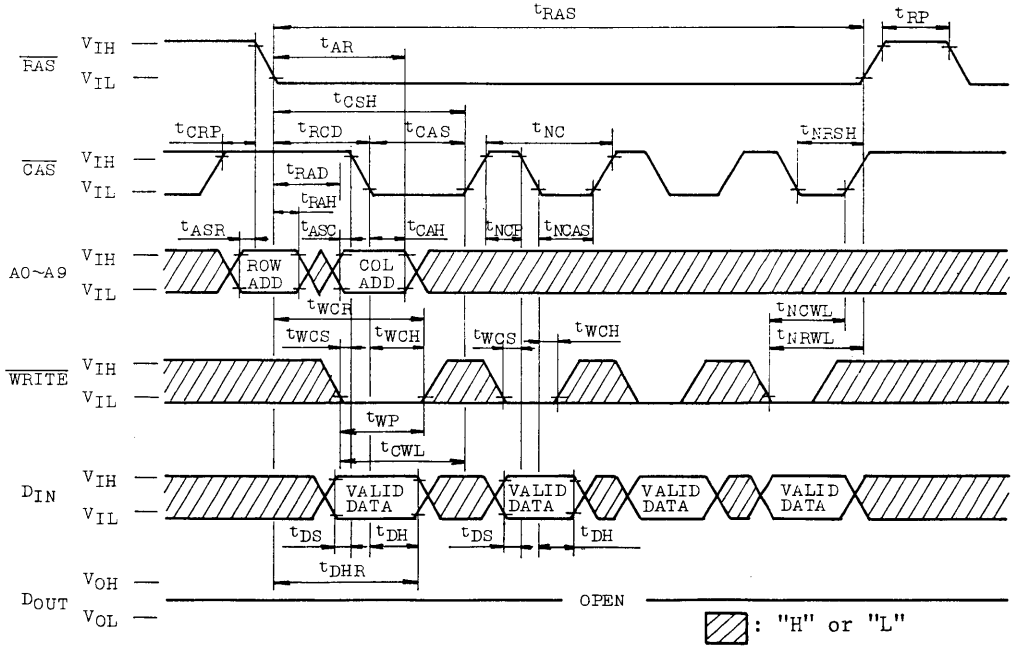


▨: "H" or "L"

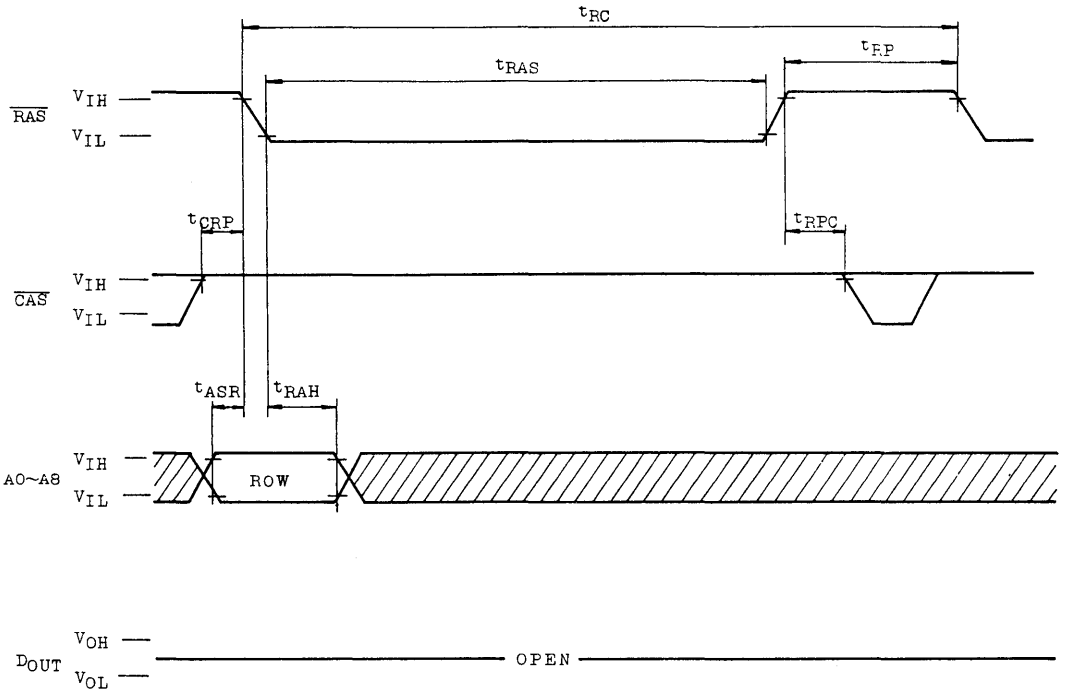
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

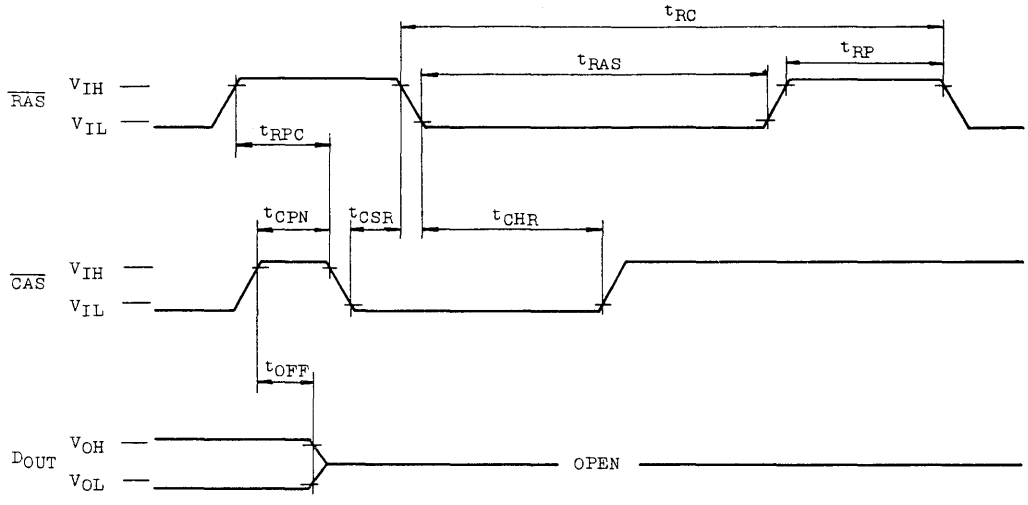


$\overline{RAS}$ ONLY REFRESH CYCLE



NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

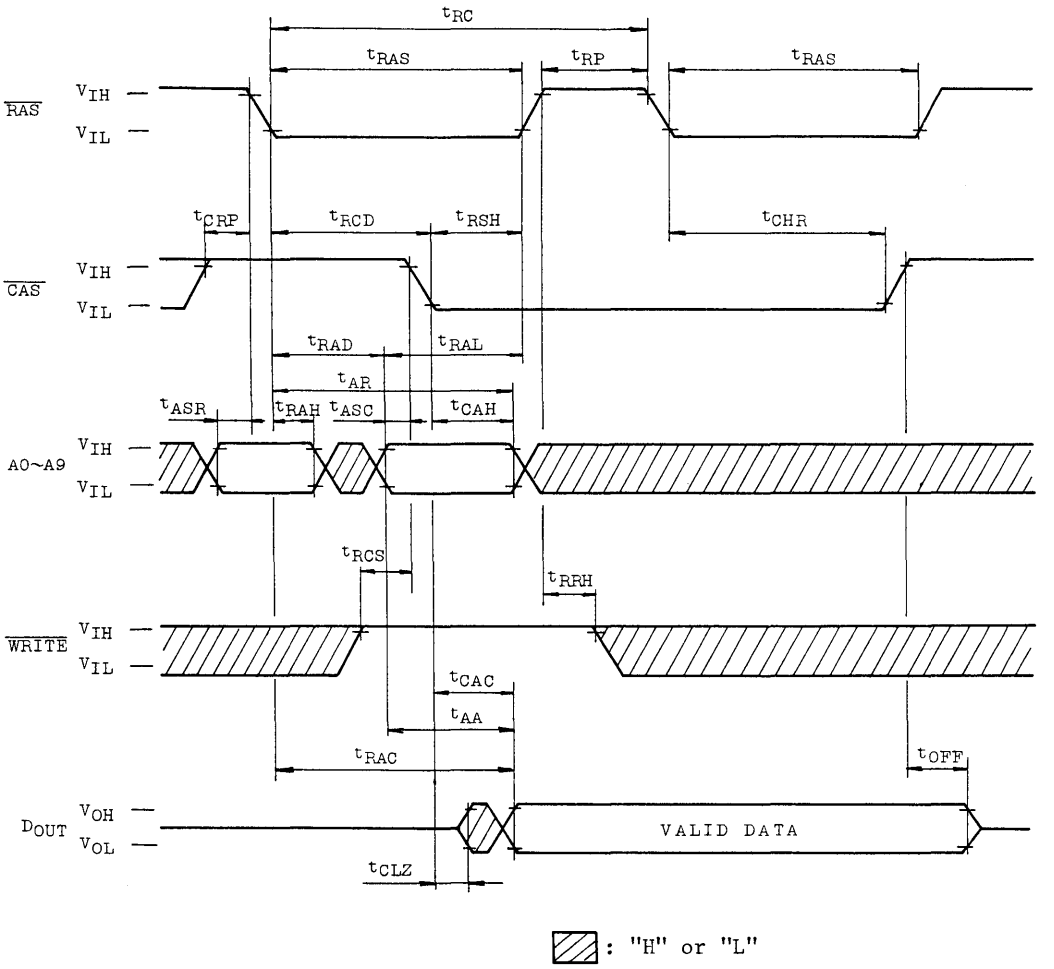
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



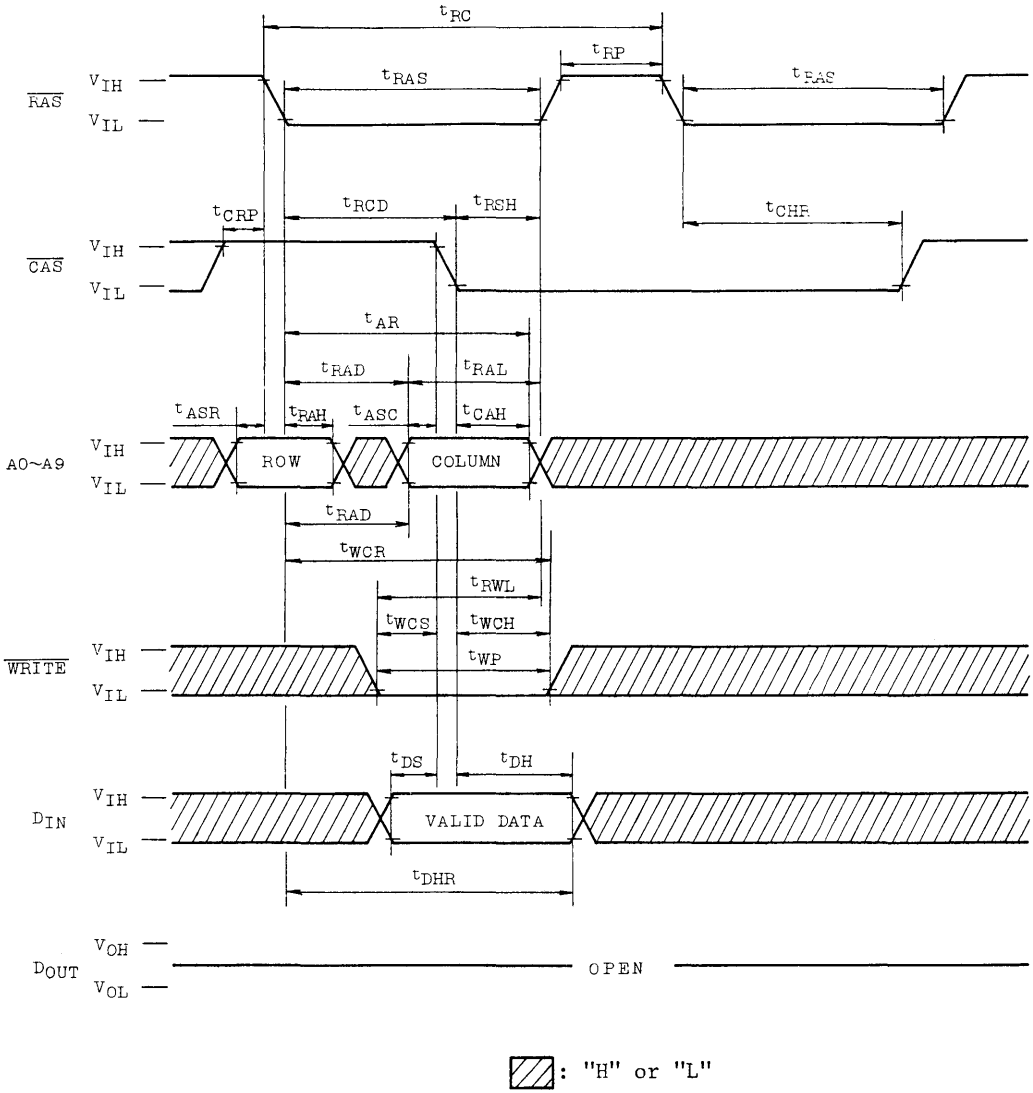
▨ : "H" or "L"

NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

HIDDEN REFRESH CYCLE (READ)

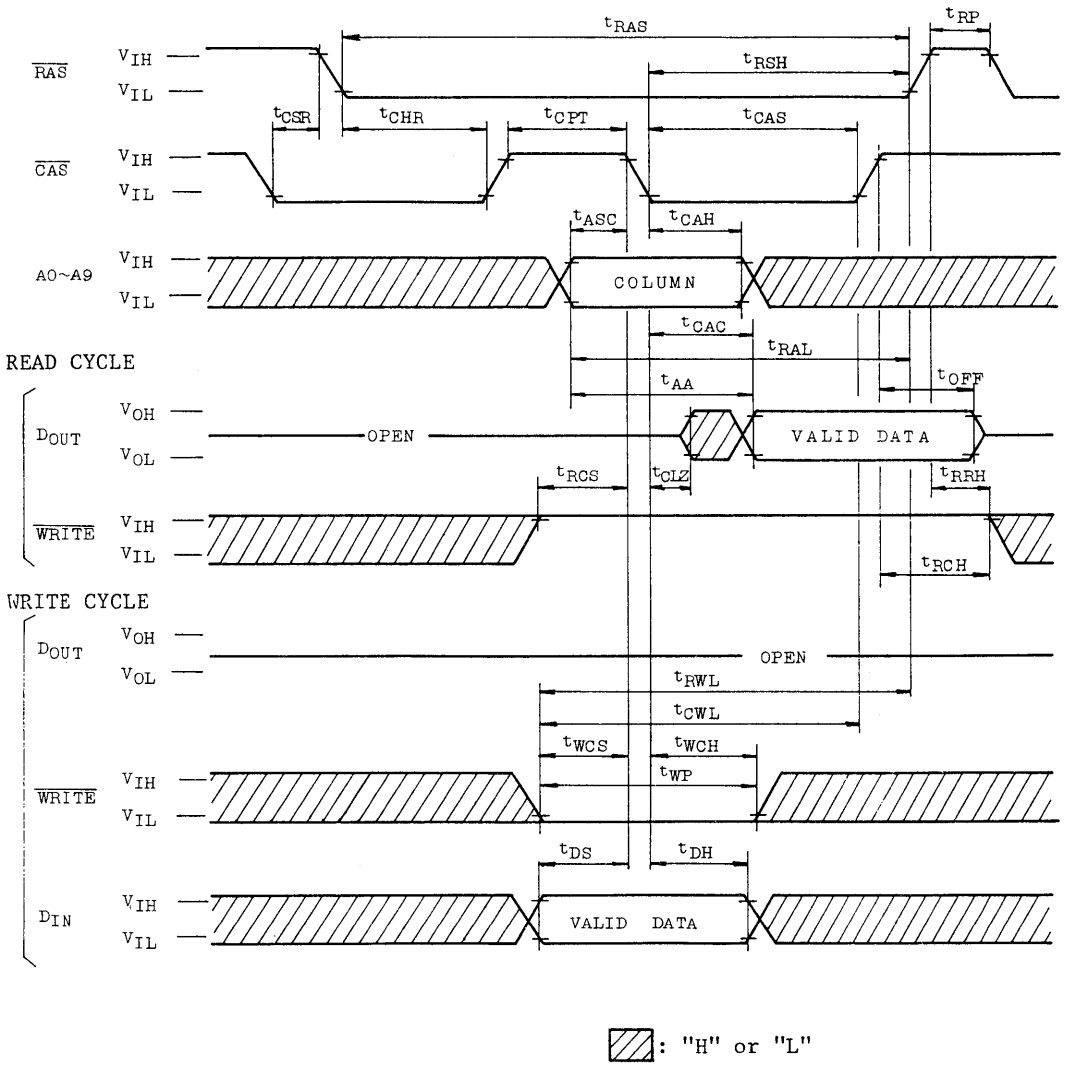


HIDDEN REFRESH CYCLE (WRITE)



▨: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

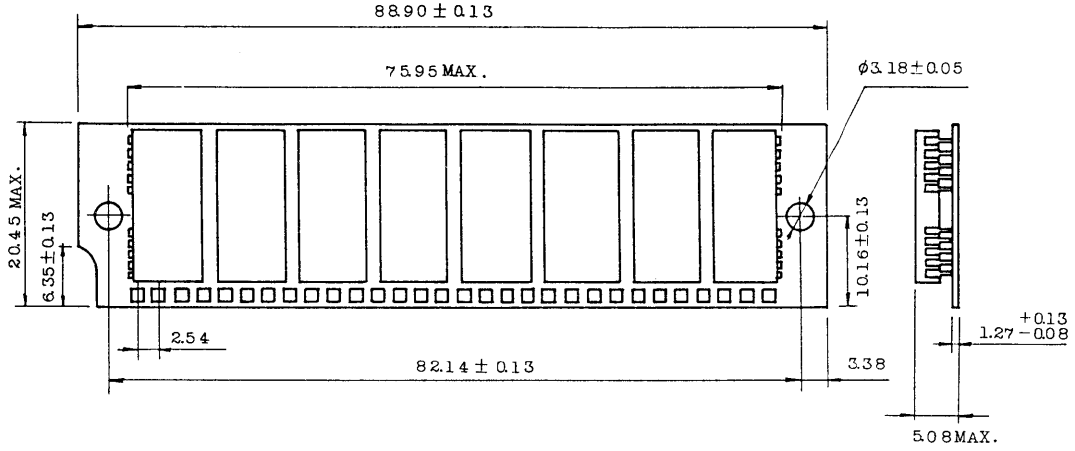


▨: "H" or "L"

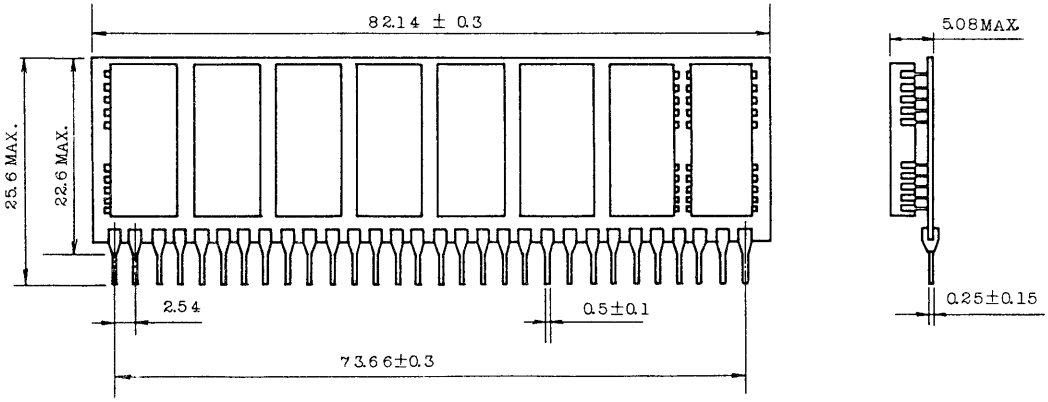
OUTLINE DRAWINGS

• THM81001S

Unit in mm



• THM81001L



THM81002S/L-85, 10, 12

DESCRIPTION

The THM81002S/L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511002J on the printed circuit board.
The THM81002S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

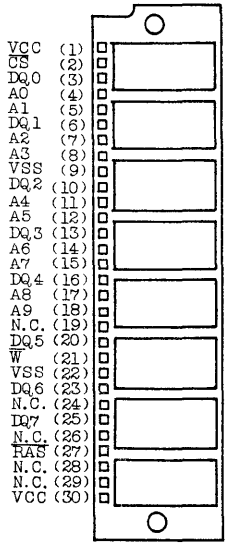
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81002S/L-85	THM81002S/L-10	THM81002S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10%
- Low power 3,080mW MAX. Operating (THM81002S/L-85)
  2,640mW MAX. Operating (THM81002S/L-10)
  2,200mW MAX. Operating (THM81002S/L-12)
  44mW MAX. Standby
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability.
- All Inputs and Outputs TTL Compatible
- 512 refresh cycles/8ms

PIN CONNECTION

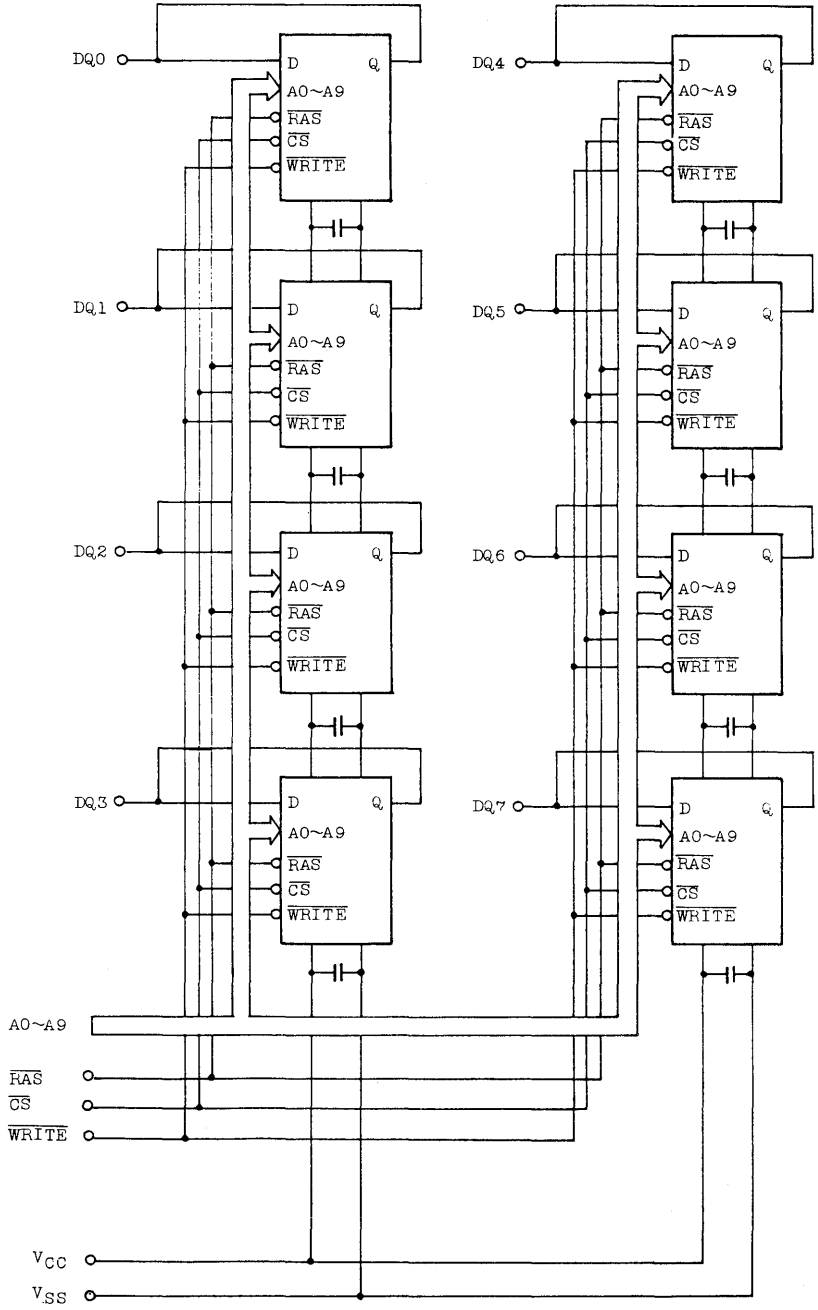
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81002S/L-85	-	560	mA	3, 4
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81002S/L-85	-	560	mA	3
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IH}, Address Cycling: t_{SC}=t_{SC} MIN.)	THM81002S/L-85	-	400	mA	3, 4
		THM81002S/L-10	-	320		
		THM81002S/L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81002S/L-85	-	560	mA	3
		THM81002S/L-10	-	480		
		THM81002S/L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81002S/L-85		THM81002S/L-10		THM81002S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81002S/L-85		THM81002S/L-10		THM81002S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∼70°C)

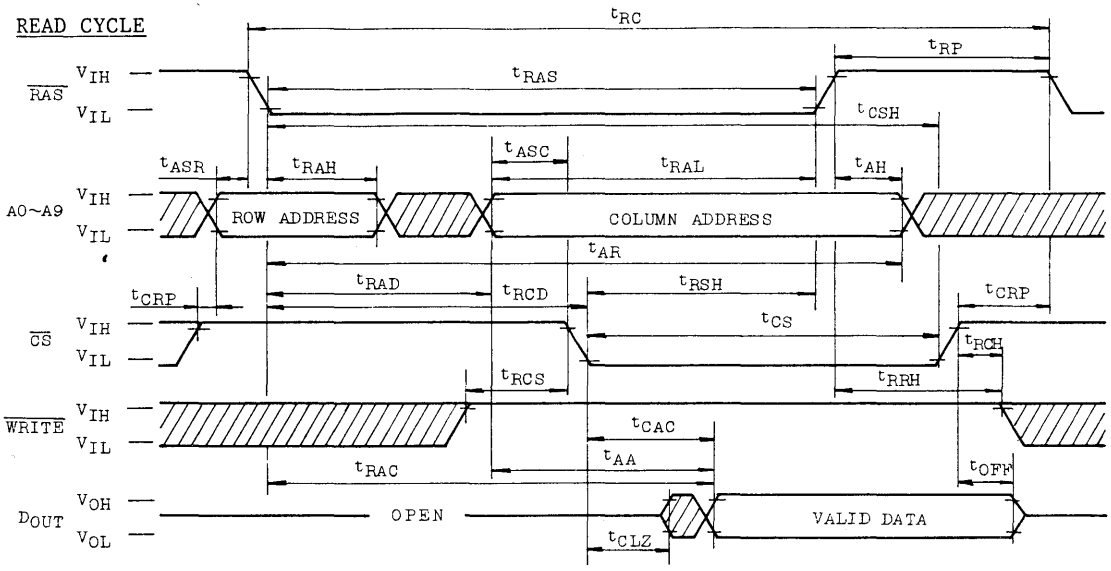
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∼A9, $\overline{W}$, $\overline{CS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∼DQ7)	-	15	pF

NOTES:

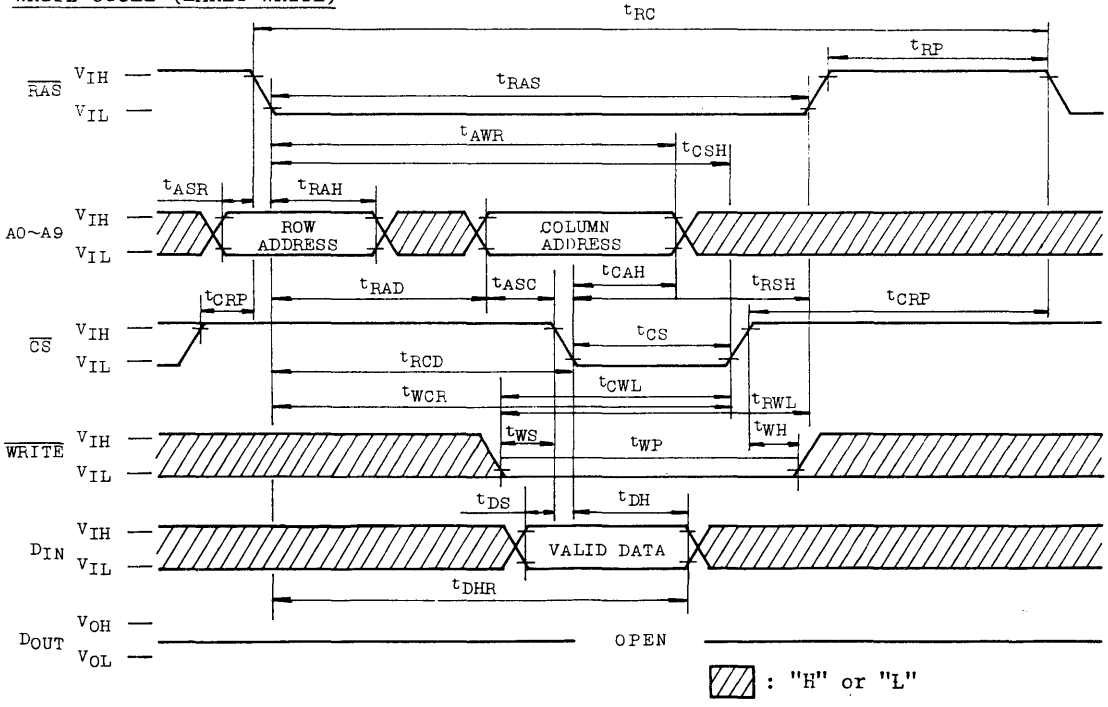
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge.
12. t_{WS}, t_{WH} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$(min.) and $t_{WH} \geqq t_{WH}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

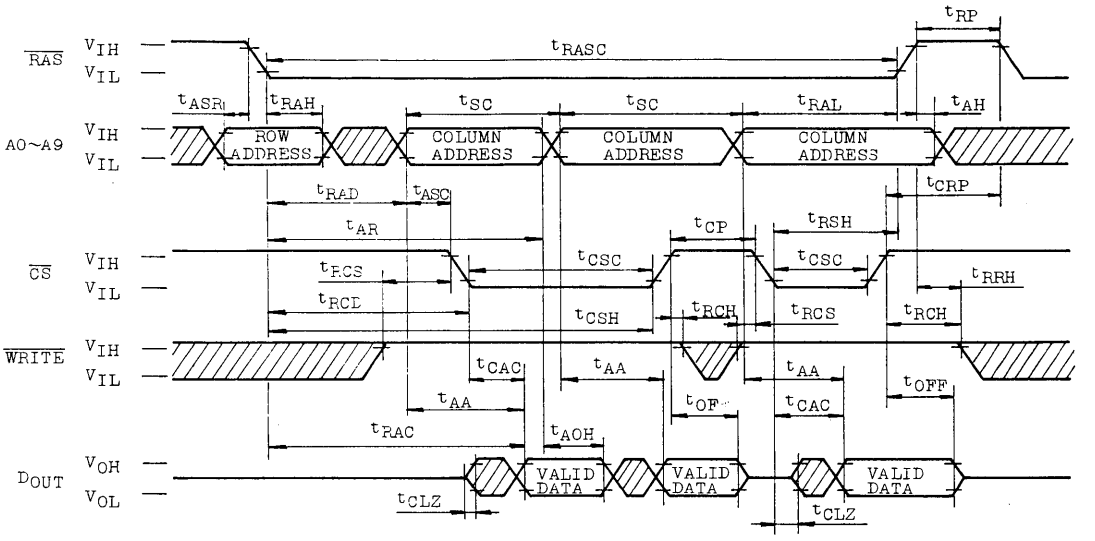
READ CYCLE



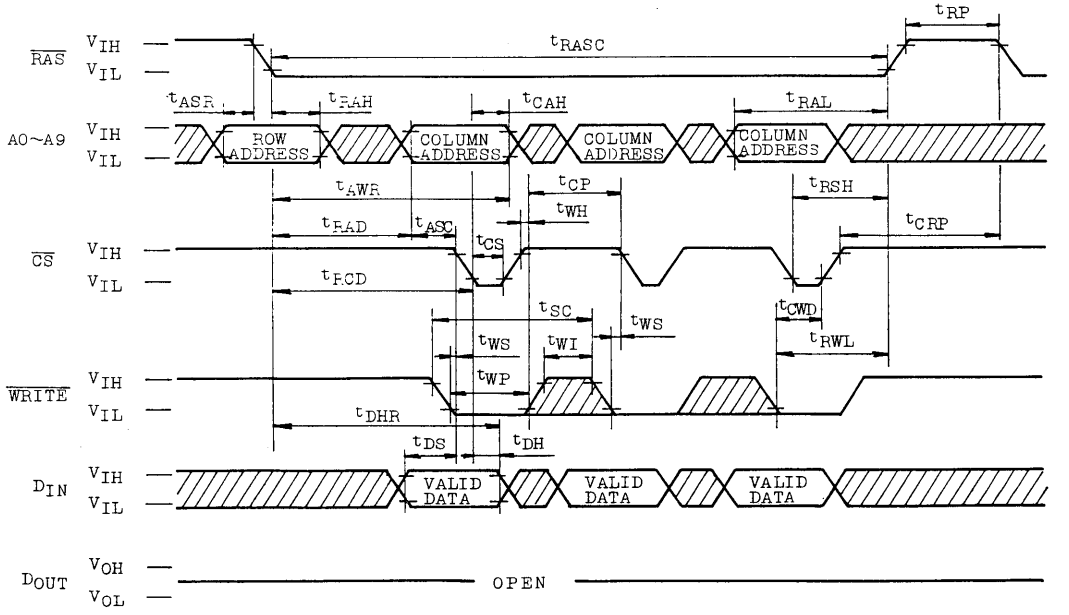
WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE READ CYCLE

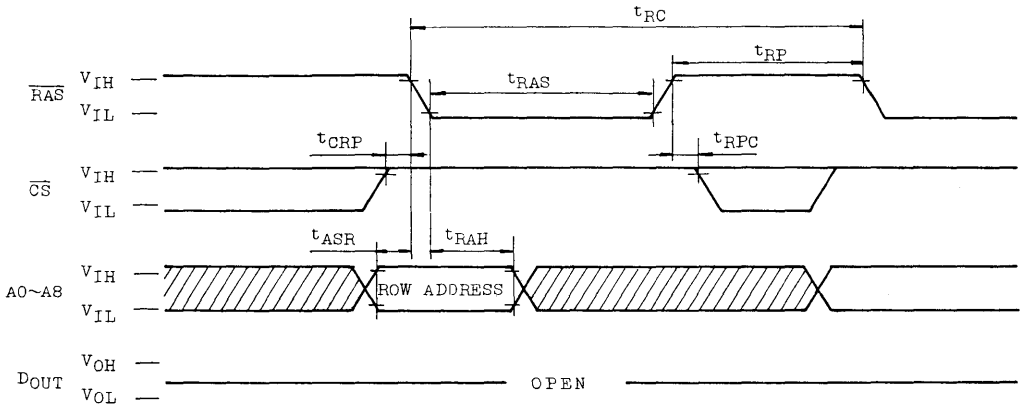


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



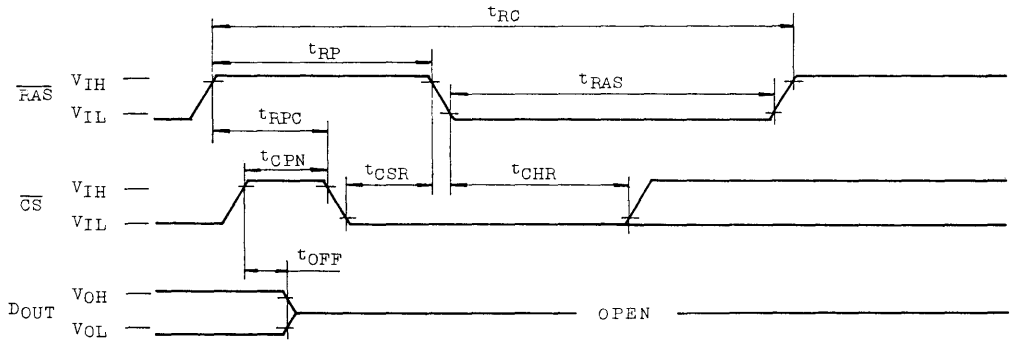
▨: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



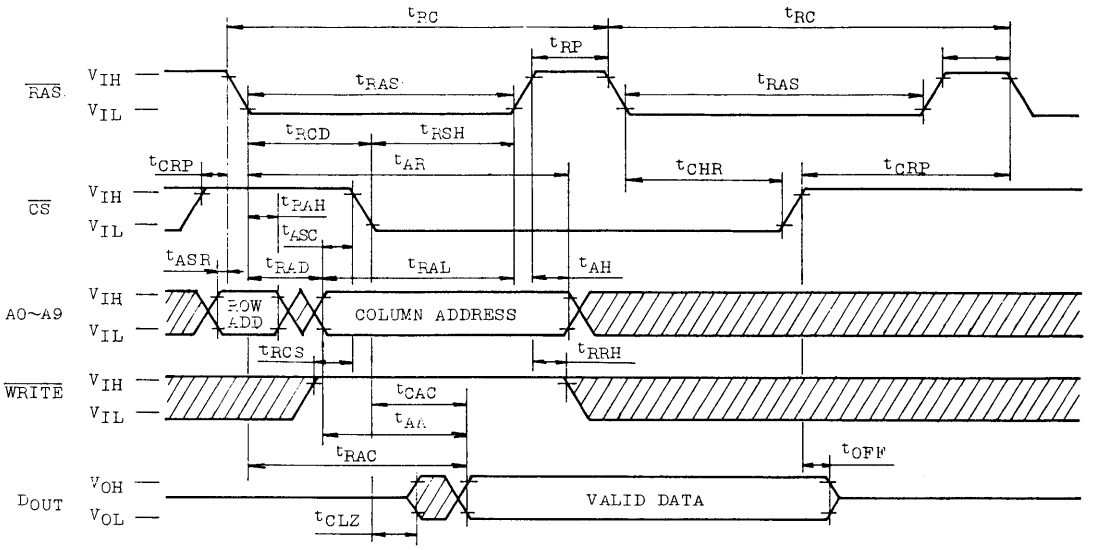
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

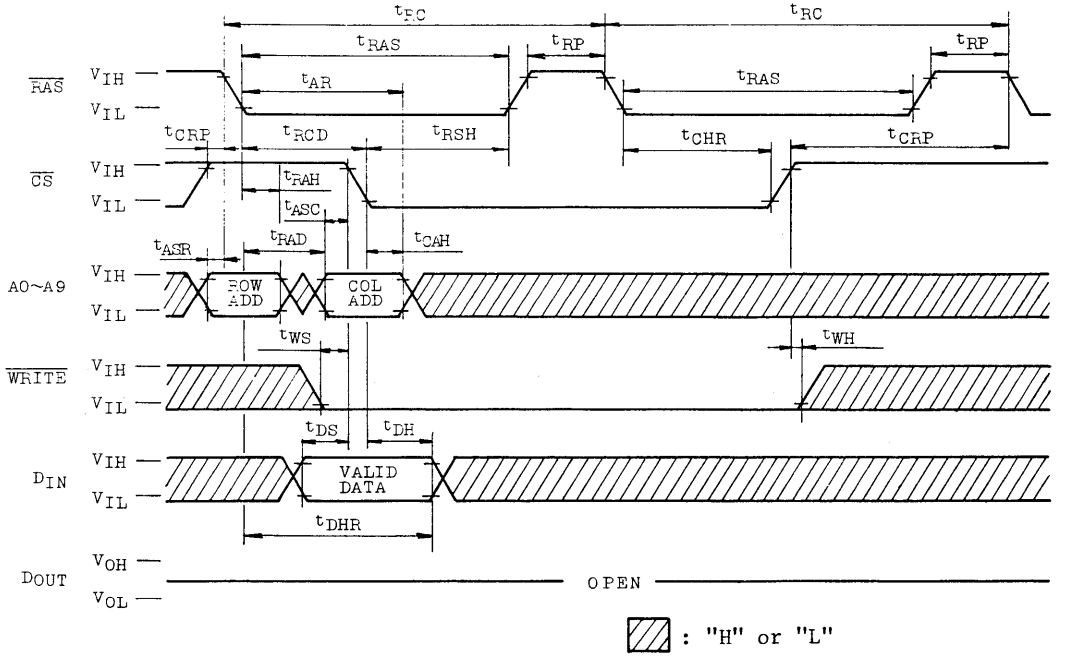


NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

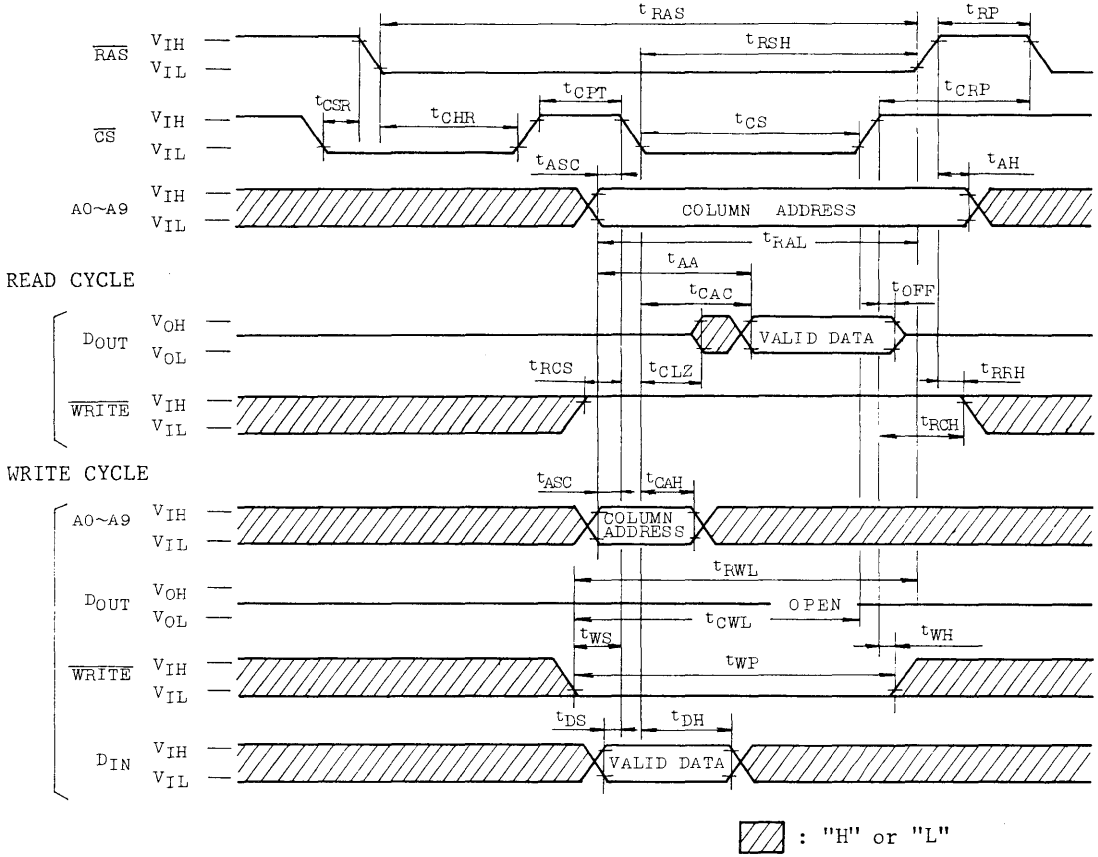
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



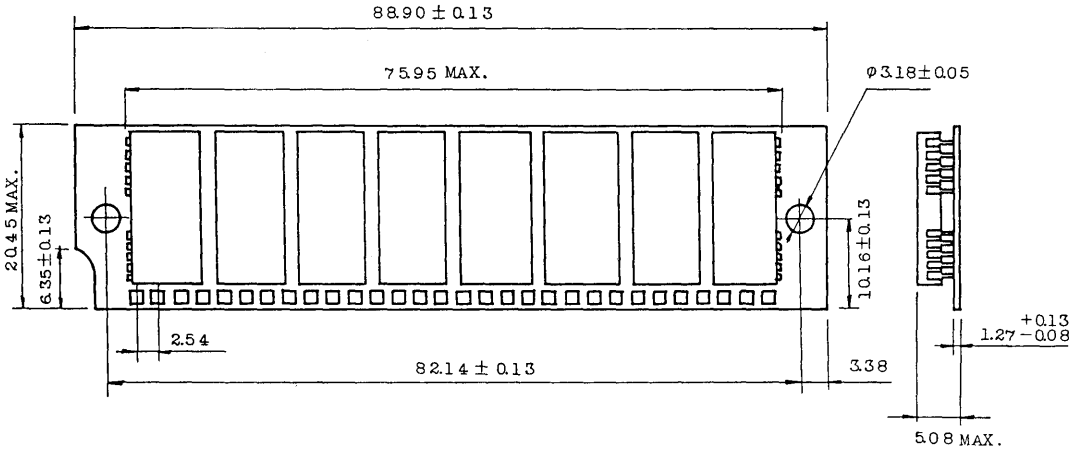
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



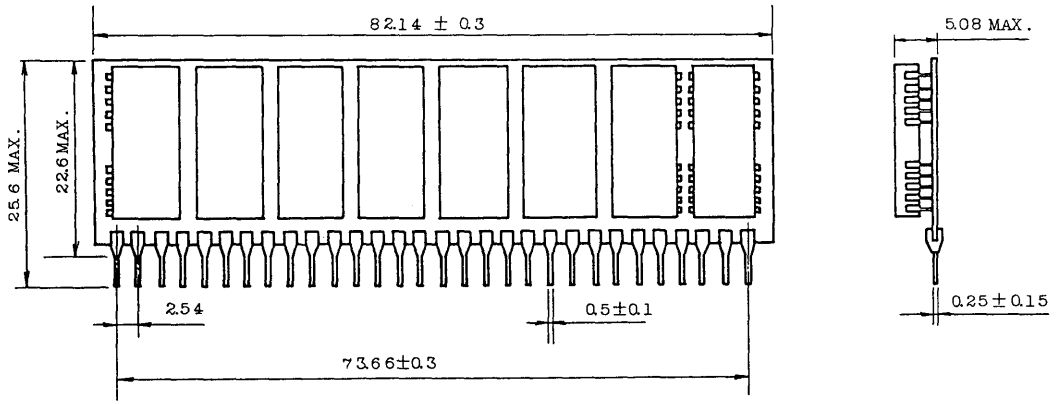
OUTLINE DRAWINGS

• THM81002S

Unit in mm



• THM81002L



THM81020L-85, 10, 12

DESCRIPTION

The THM81020L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000J both sides of the printed circuit board.

The THM81020L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

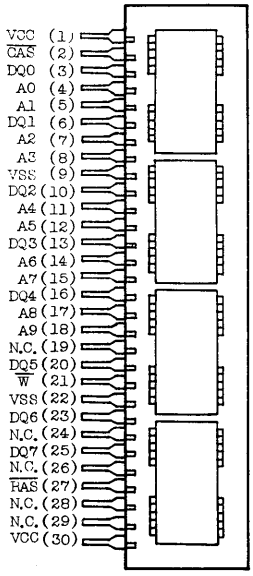
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81020L-85	THM81020L-10	THM81020L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V±10%
- Low power
  - 3,080mW MAX. Operating (THM81020L-85)
  - 2,640mW MAX. Operating (THM81020L-10)
  - 2,200mW MAX. Operating (THM81020L-12)
  - 44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

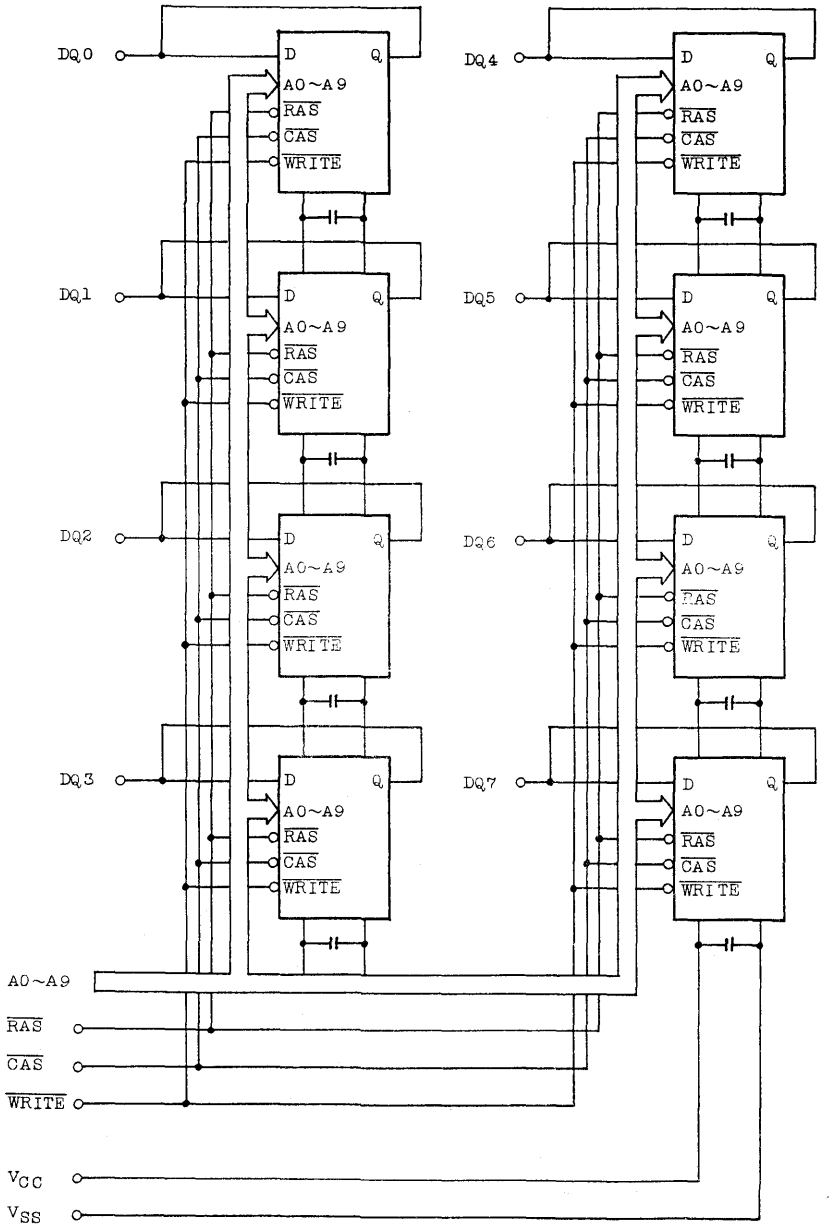
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, T_a=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATINC CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81020L-85	-	560	mA	3,4
		THM81020L-10	-	480		
		THM81020L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81020L-85	-	560	mA	3
		THM81020L-10	-	480		
		THM81020L-12	-	400		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM81020L-85	-	400	mA	3,4
		THM81020L-10	-	320		
		THM81020L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81020L-85	-	560	mA	3
		THM81020L-10	-	480		
		THM81020L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81020L-85		THM81020L-10		THM81020L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

SYMBOL	PARAMETER	THM81020L-85		THM81020L-10		THM81020L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

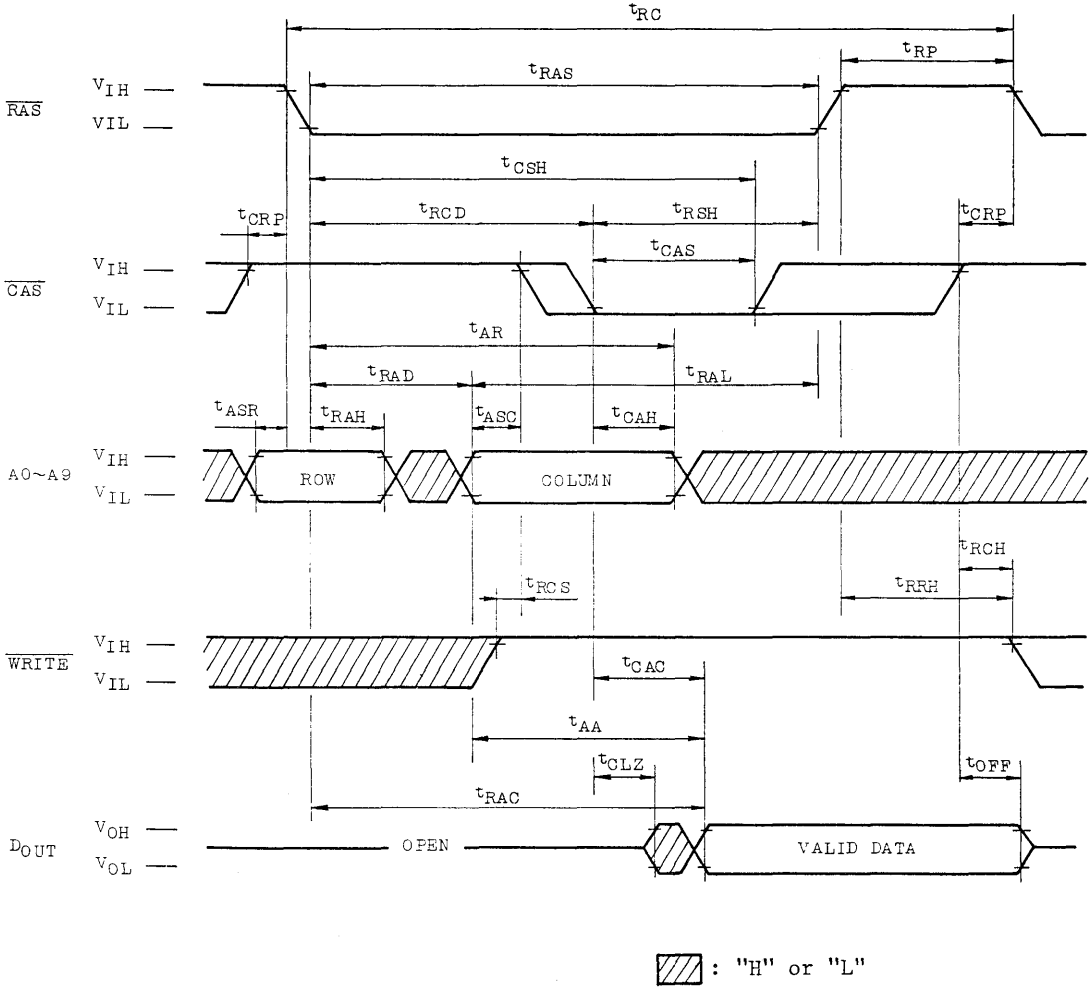
11. These parameters are referenced to $\overline{CAS}$ leading edge.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

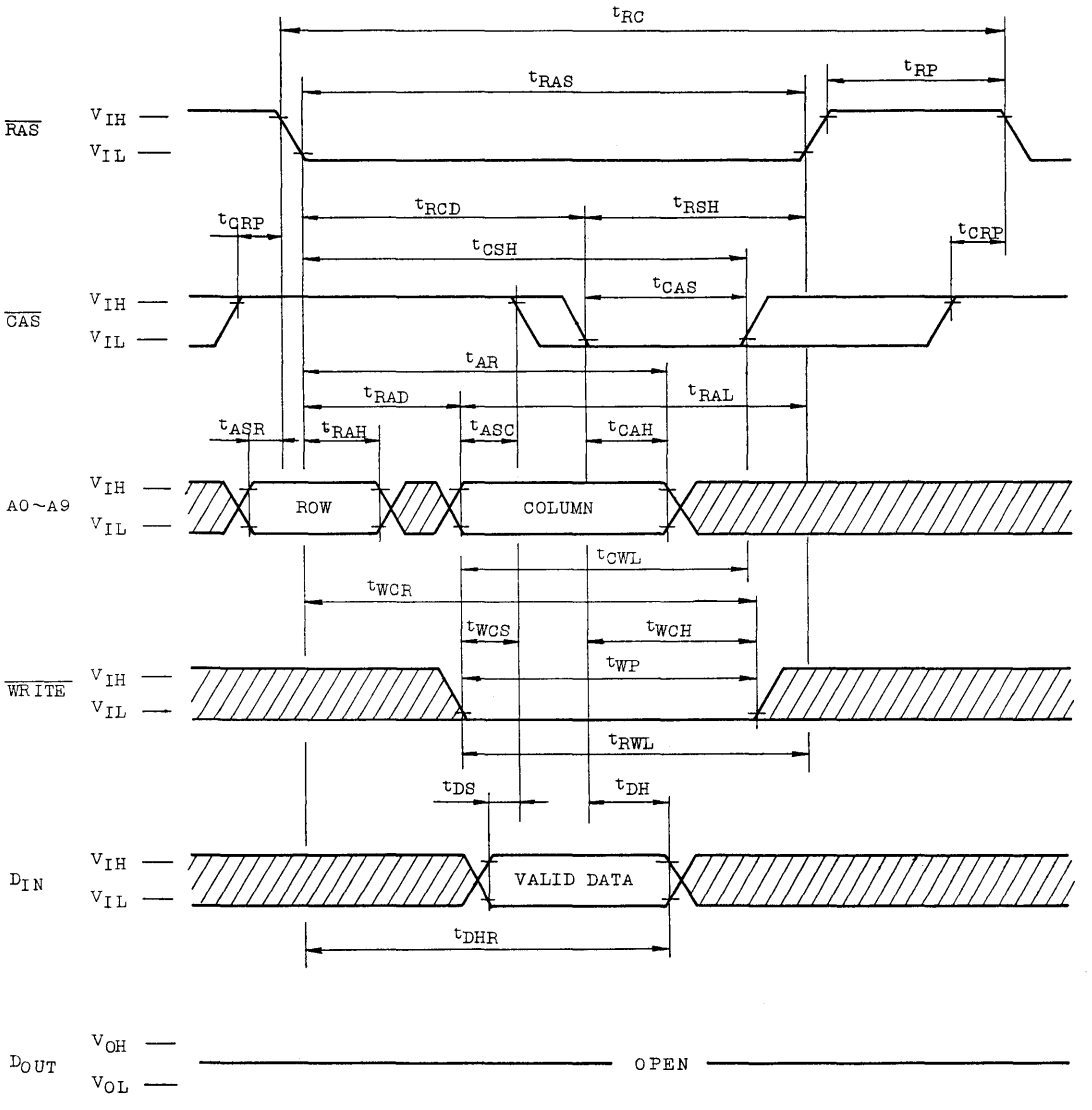
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



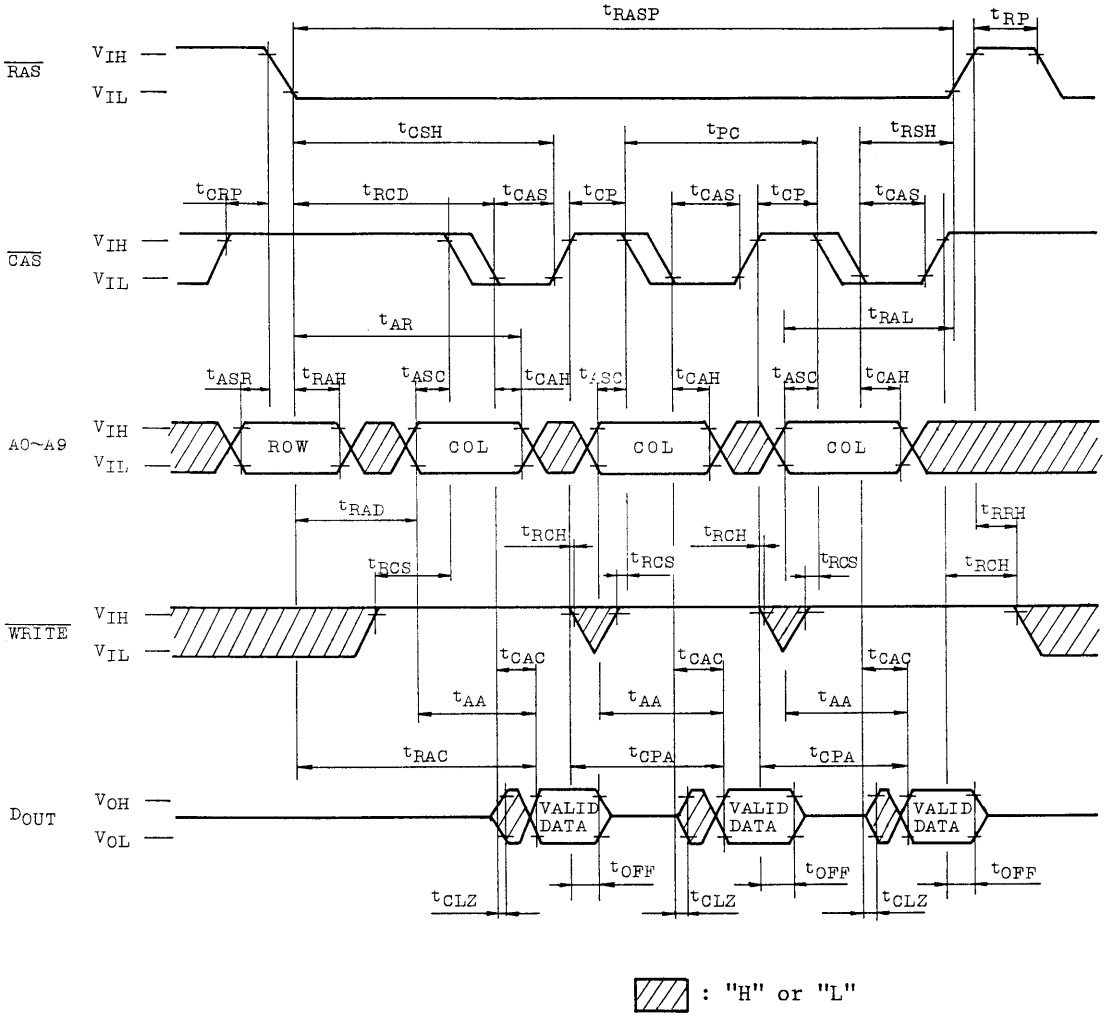
▨ : "H" or "L"

EARLY WRITE CYCLE

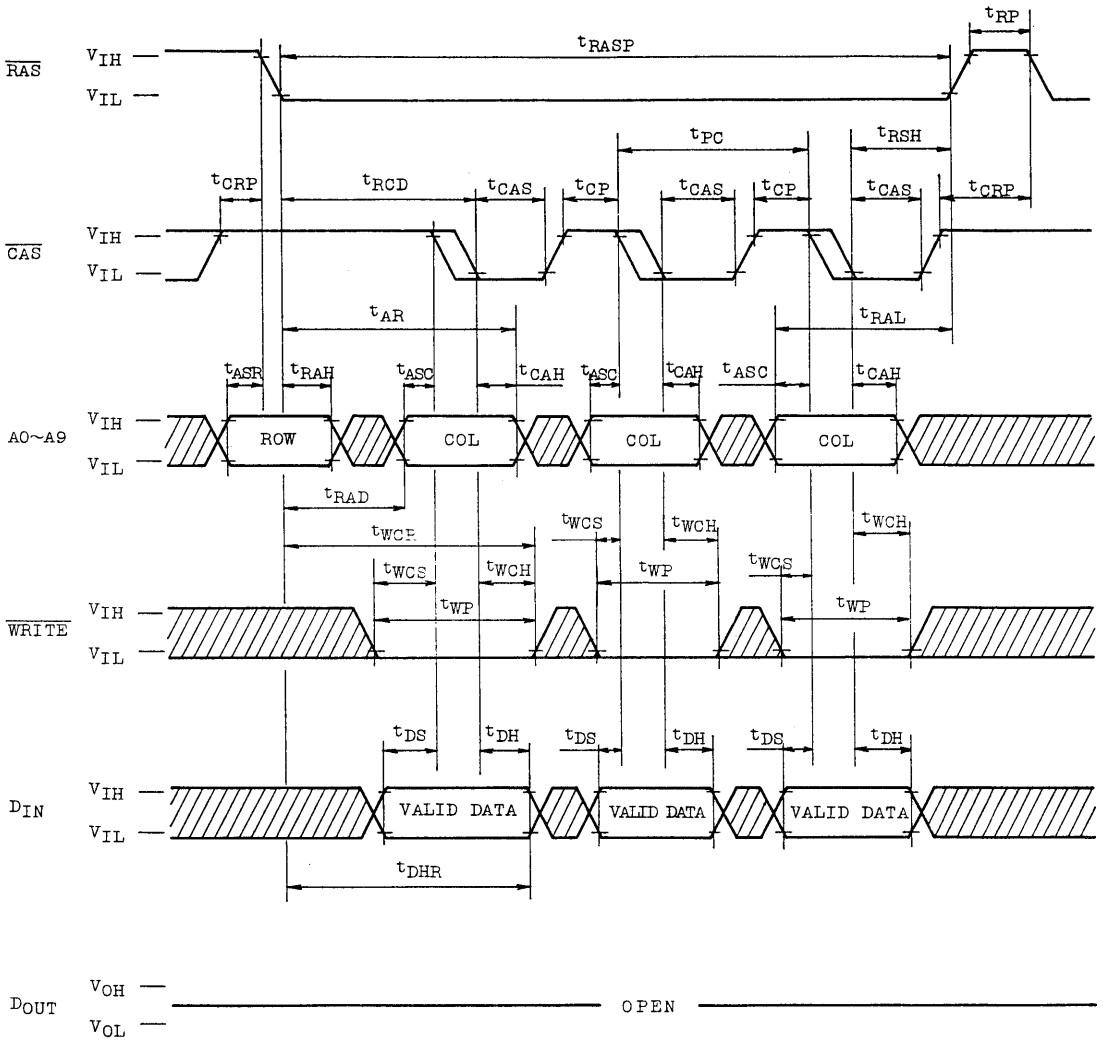


▨: "H" or "L"

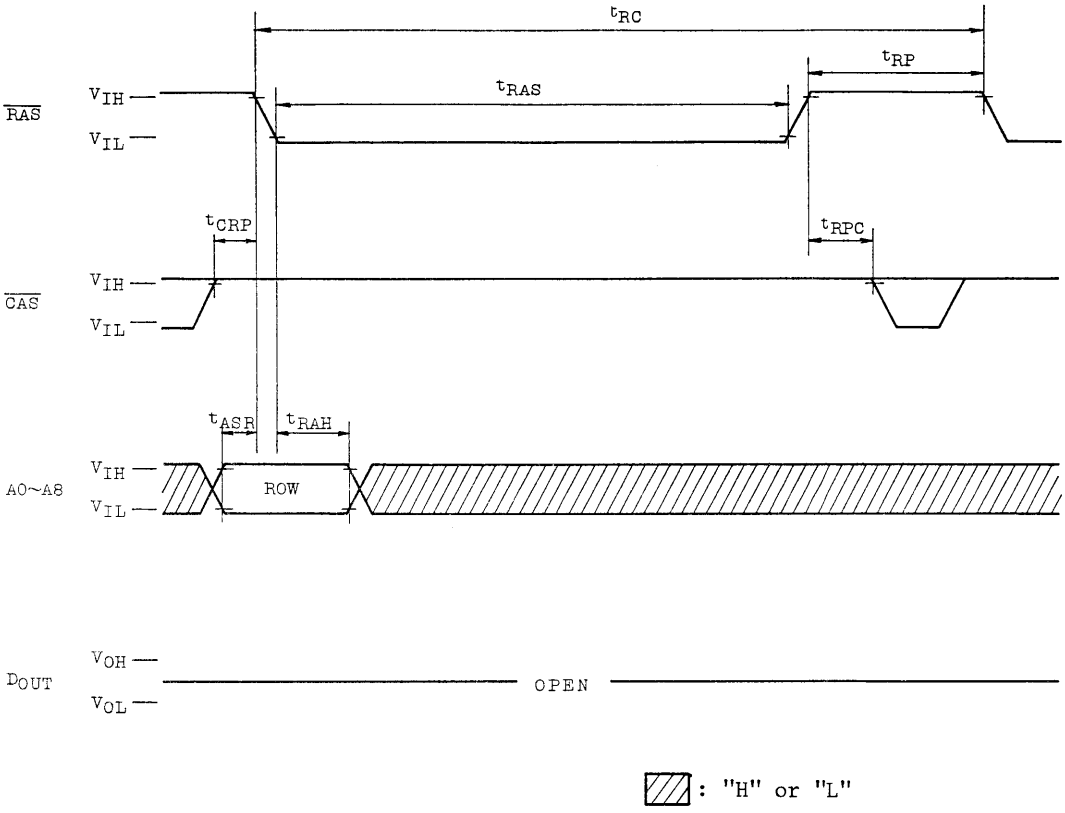
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

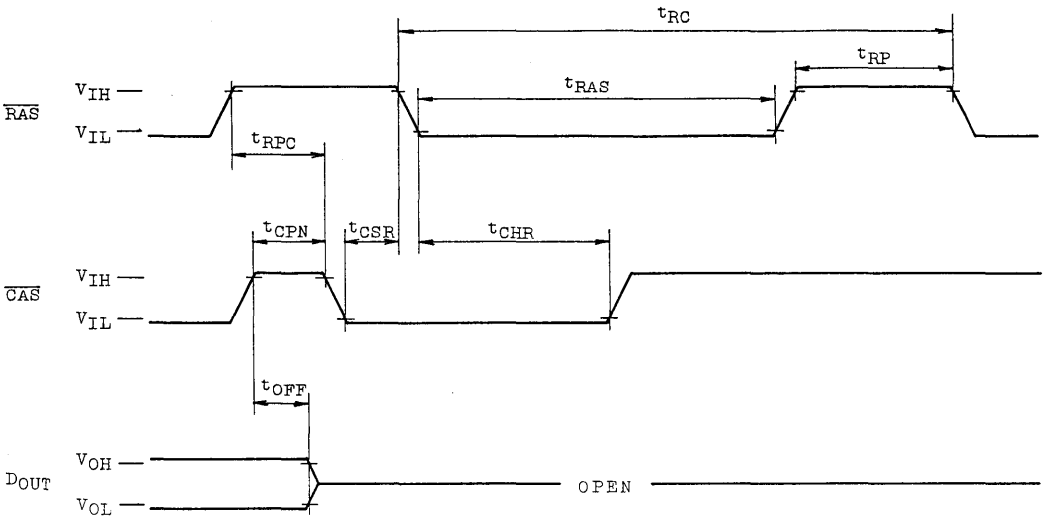


$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$="H" or "L", A9="H" or "L"

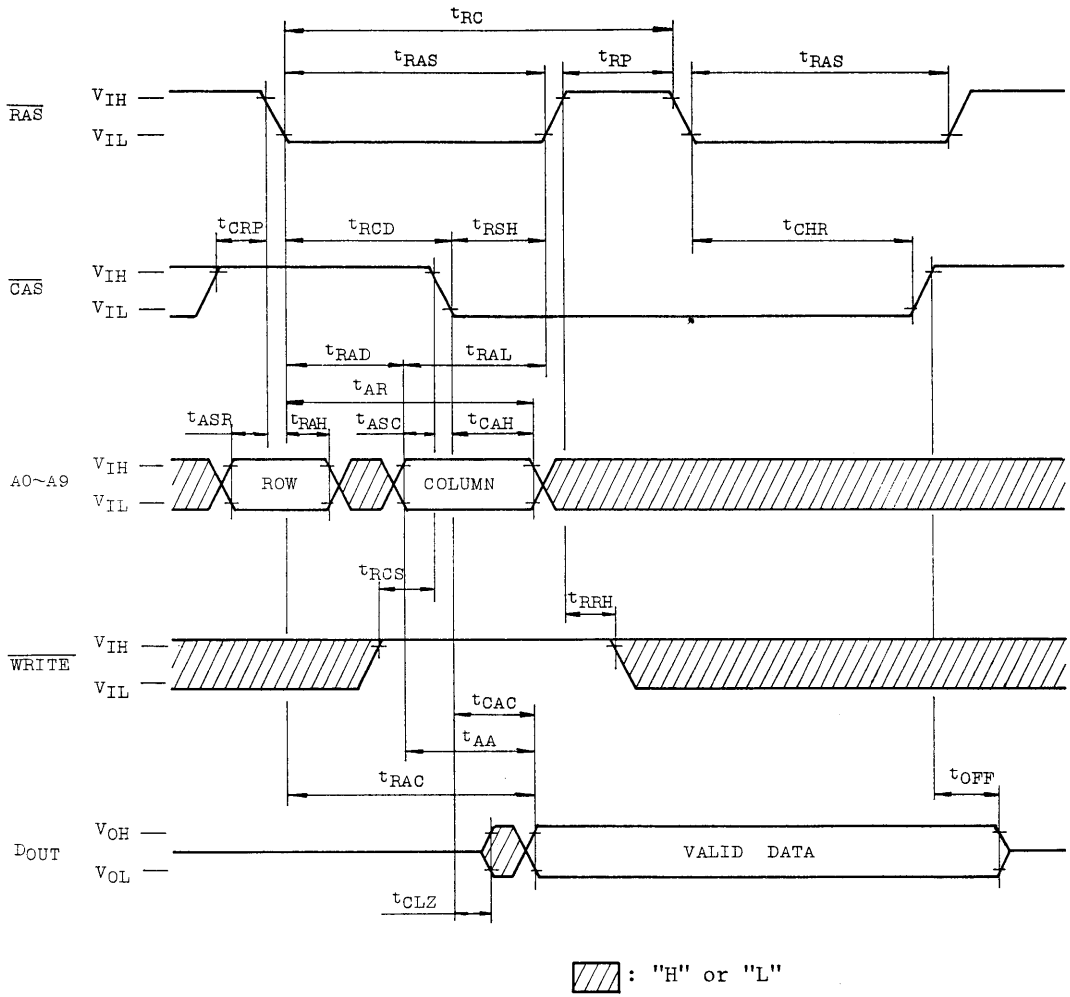
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



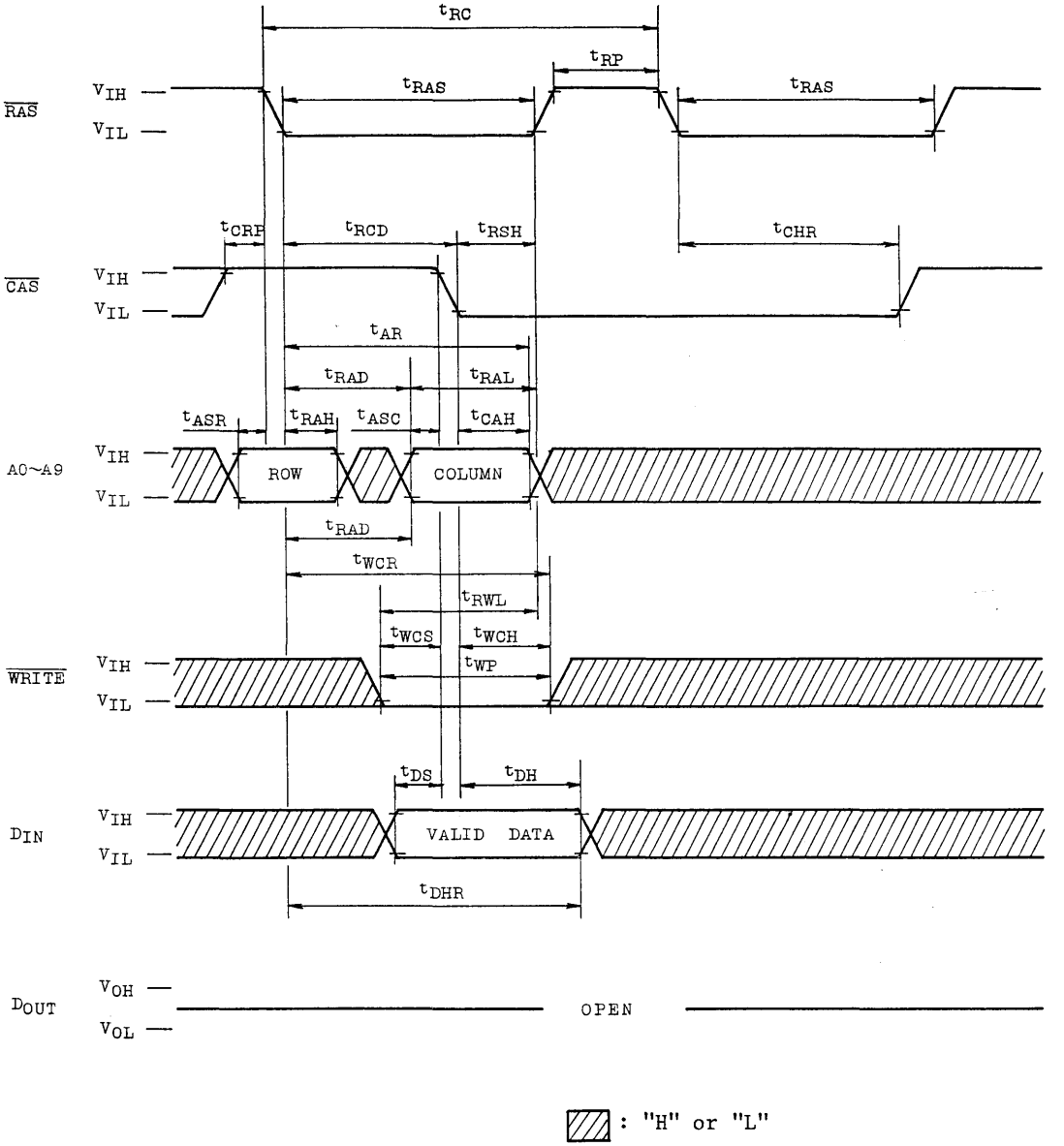
▨ : "H" or "L"

Note: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

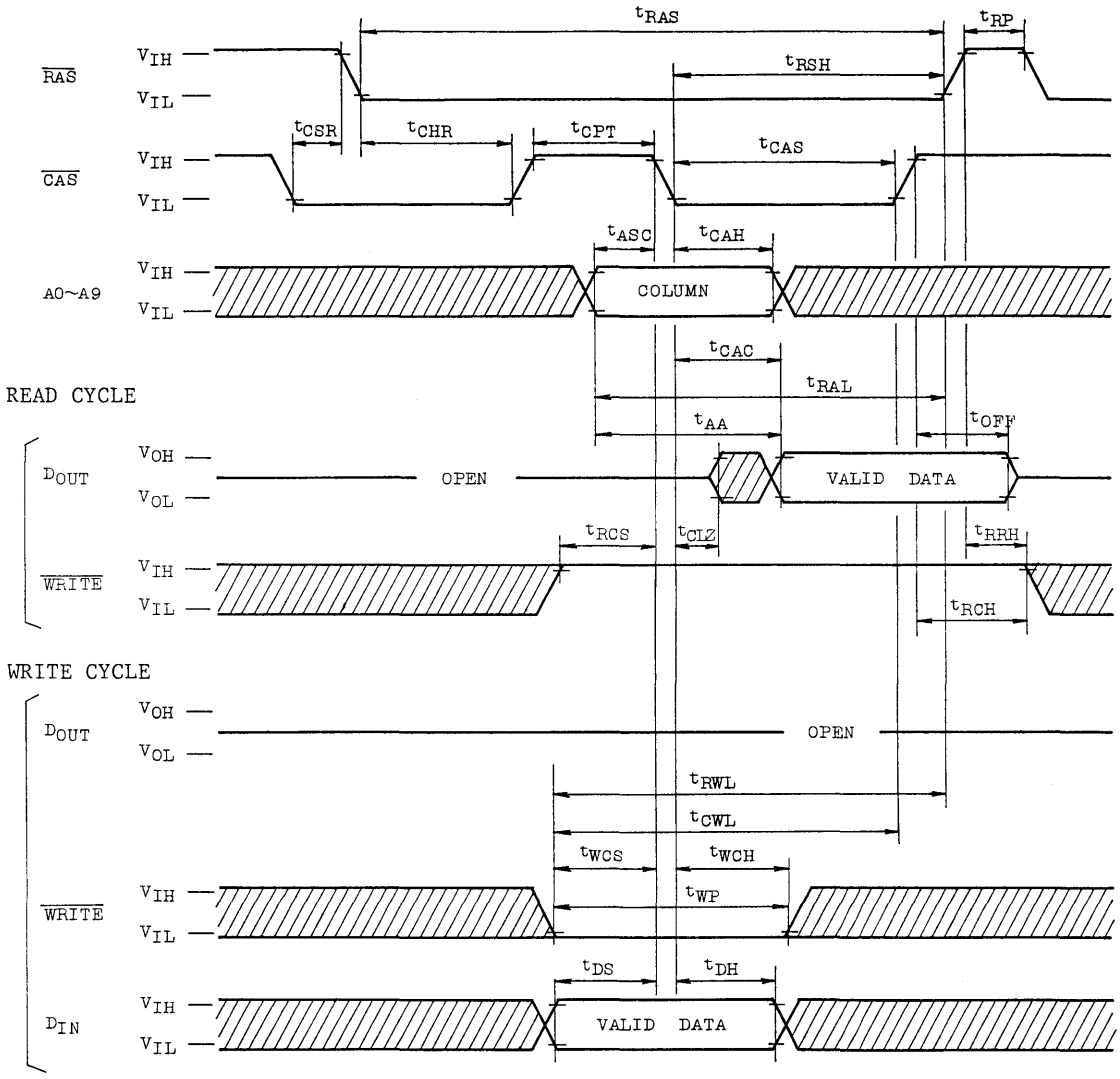
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



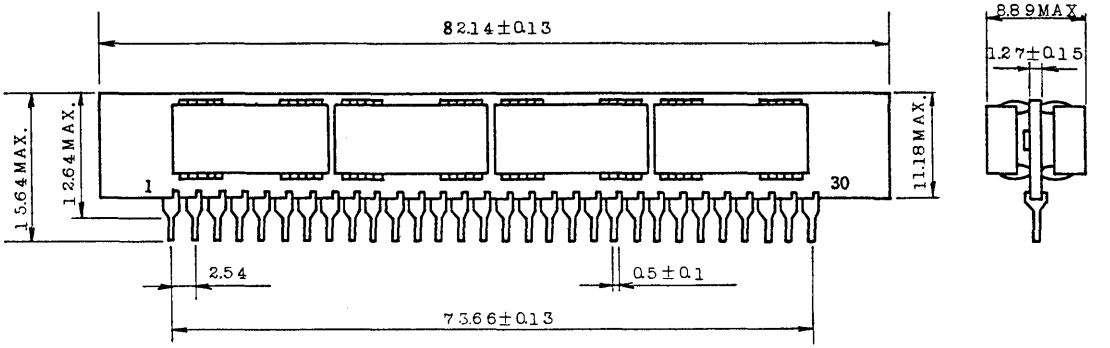
▨: "H" or "L"

OUTLINE DRAWINGS

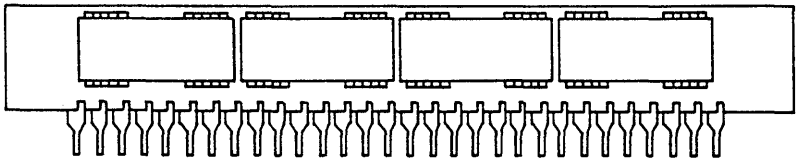
• THM81020L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



THM81021L-85, 10, 12

DESCRIPTION

The THM81021L is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511001J on both sides of the printed circuit board.

The THM81021L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

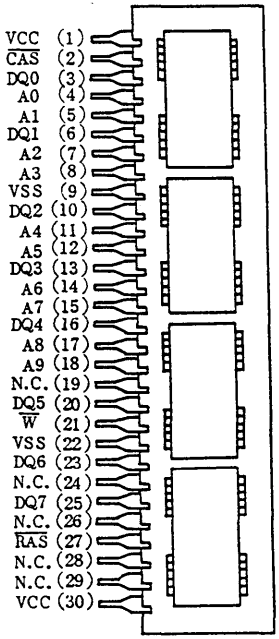
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81021L-85	THM81021L-10	THM81021L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

- Single power supply of 5V±10%
- Low power
  - 3,080mW MAX. Operating(THM81021L-85)
  - 2,649mW MAX. Operating(THM81021L-10)
  - 2,200mW MAX. Operating(THM81021L-12)
  - 44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ Only refresh, Hidden refresh, and Nibble Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Package Height

PIN CONNECTION

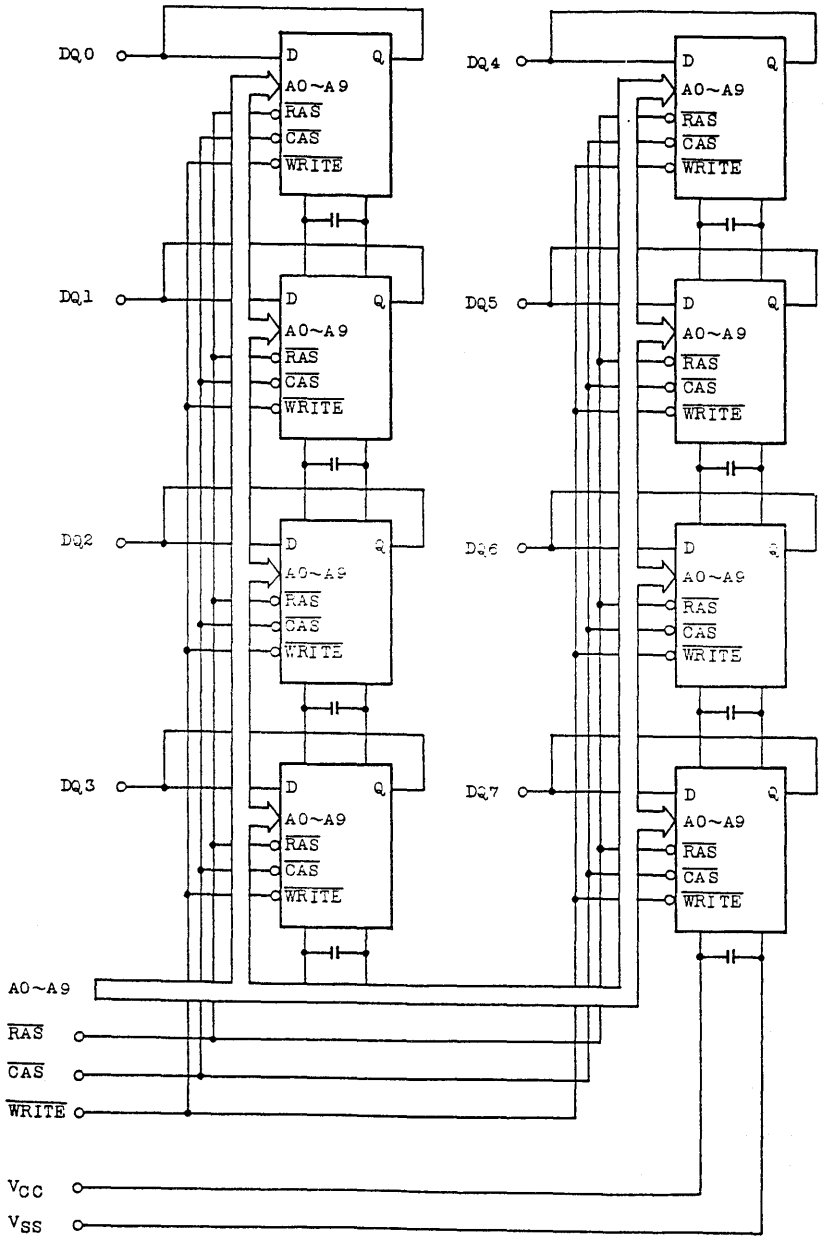
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C•sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta=0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM81021L-85	-	560	mA	3, 4
		THM81021L-10	-	480		
		THM81021L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	THM81021L-85	-	560	mA	3
		THM81021L-10	-	480		
		THM81021L-12	-	400		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling: $t_{NC}=t_{NC}$ MIN.)	THM81021L-85	-	400	mA	3, 4
		THM81021L-10	-	320		
		THM81021L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM81021L-85	-	560	mA	3
		THM81021L-10	-	480		
		THM81021L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT}=-5mA$)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT}=4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81021L-85		THM81021L-10		THM81021L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81021L-85		THM81021L-10		THM81021L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Wisth	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to RAS Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to CAS Lead Time	20	-	20	-	25	-	ns	

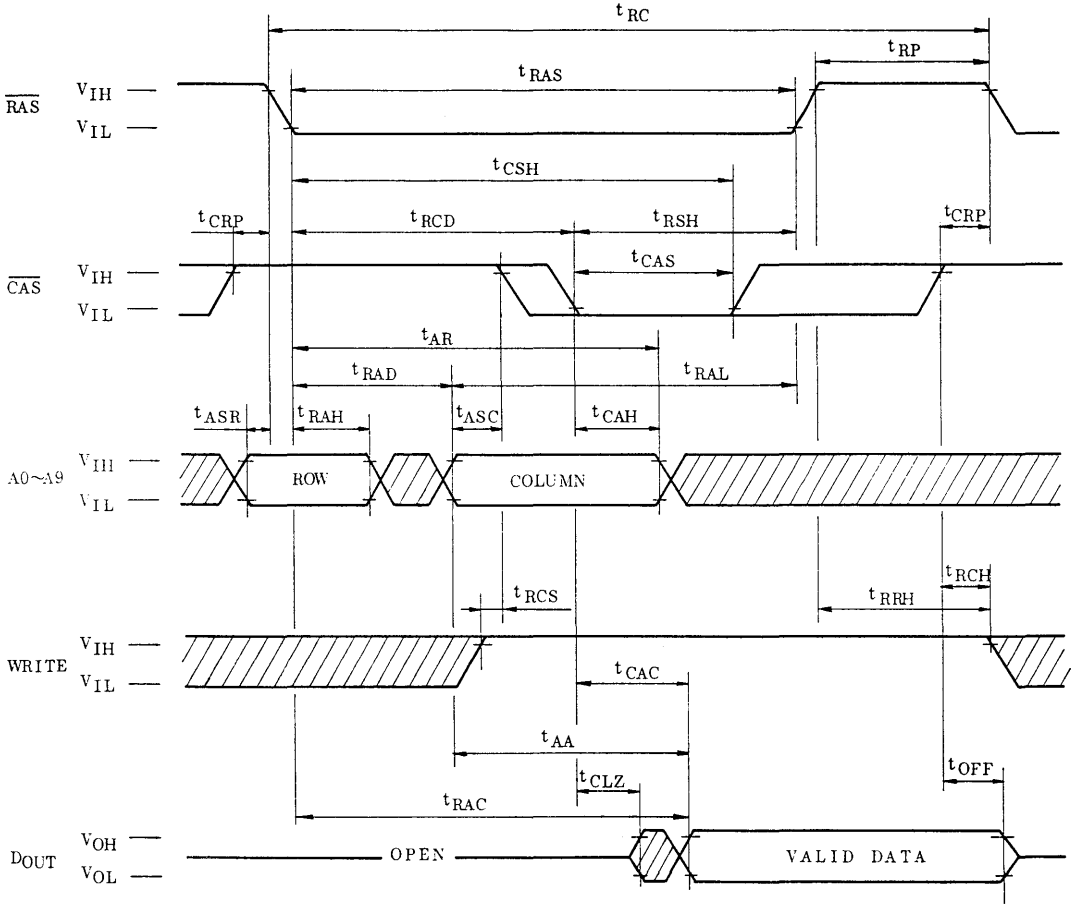
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF

NOTES:

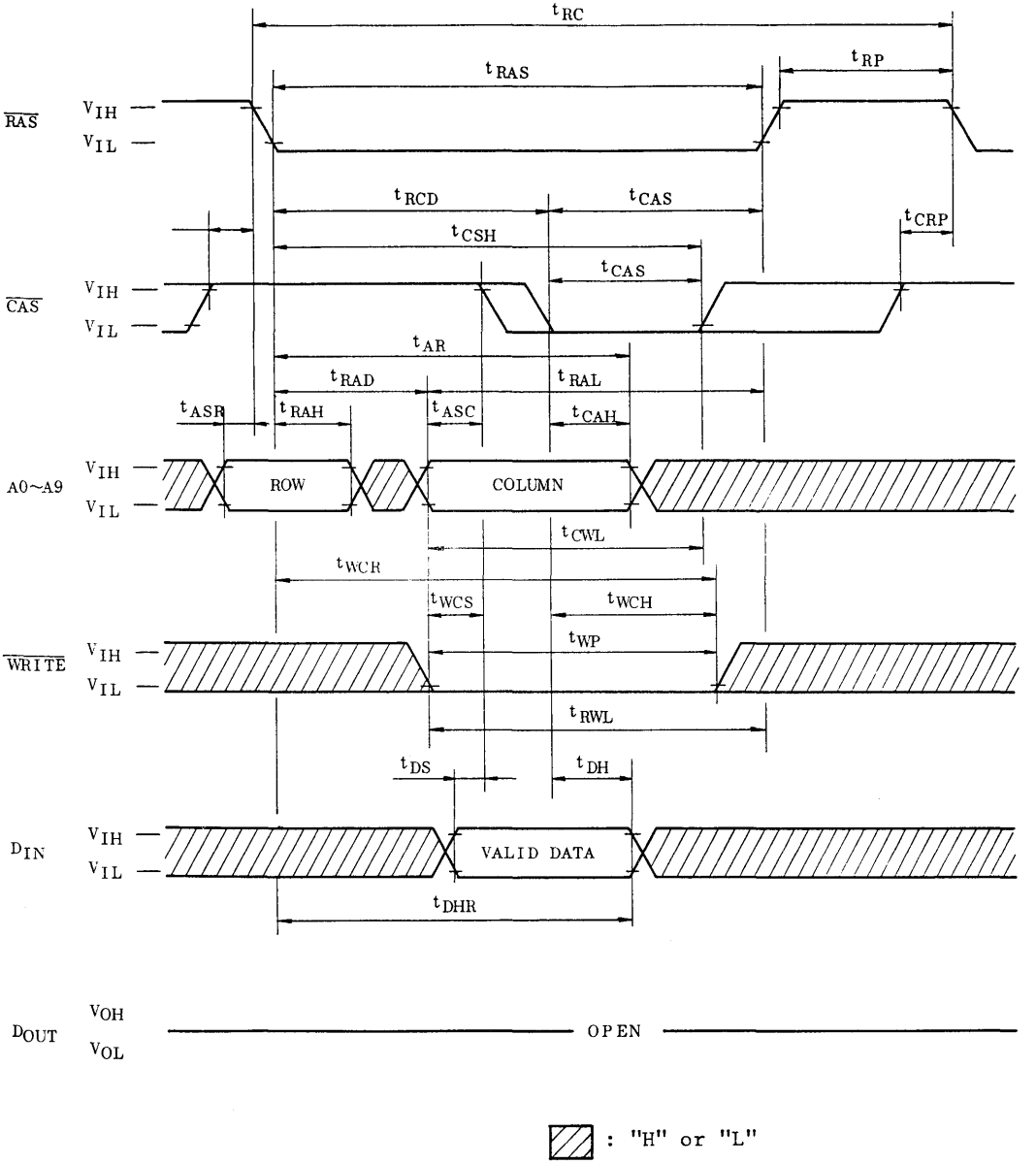
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

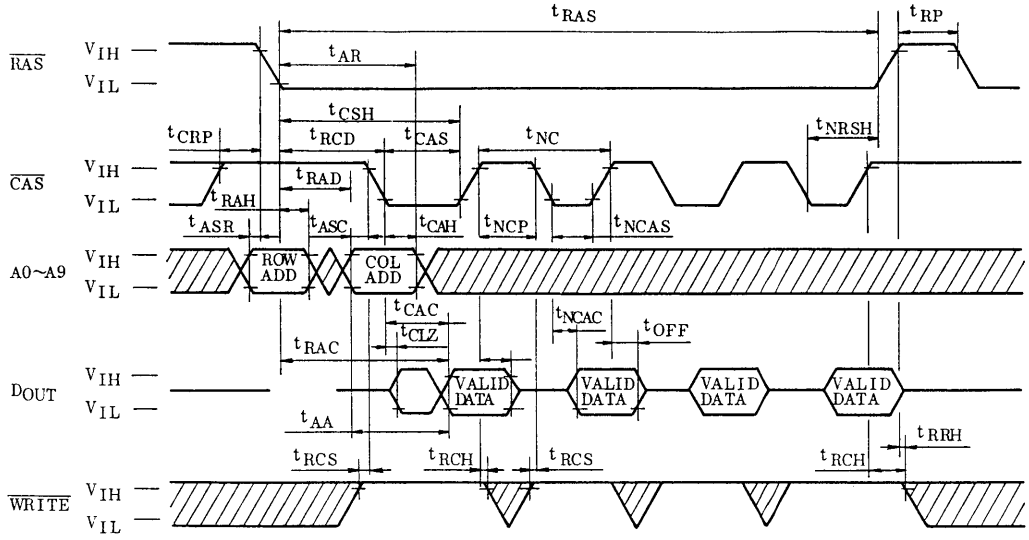


▨ : "H" or "L"

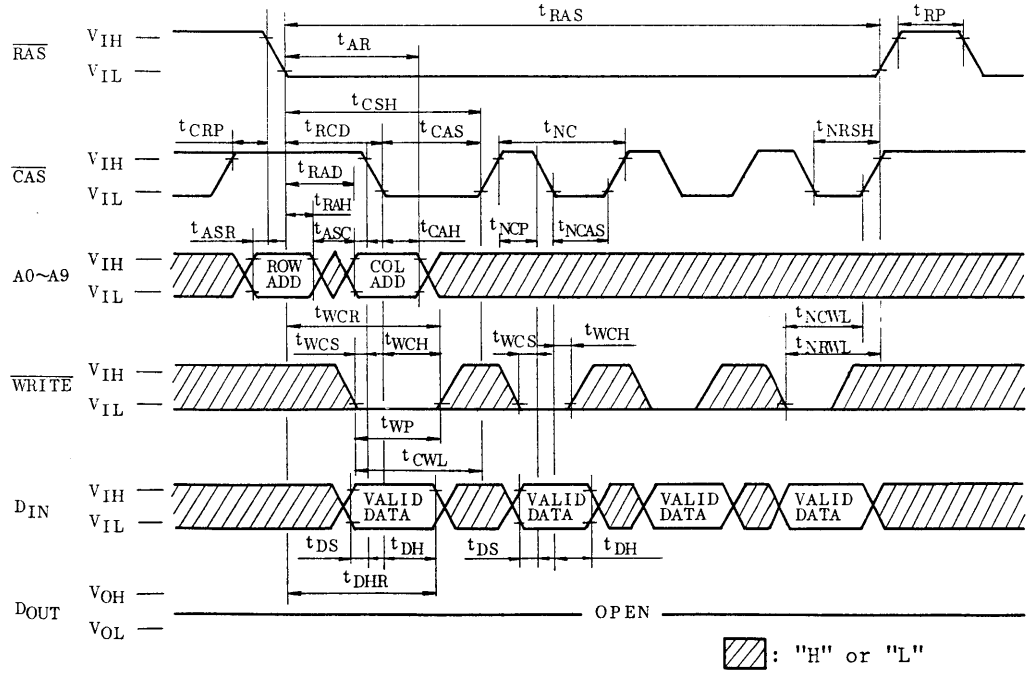
EARLY WRITE CYCLE



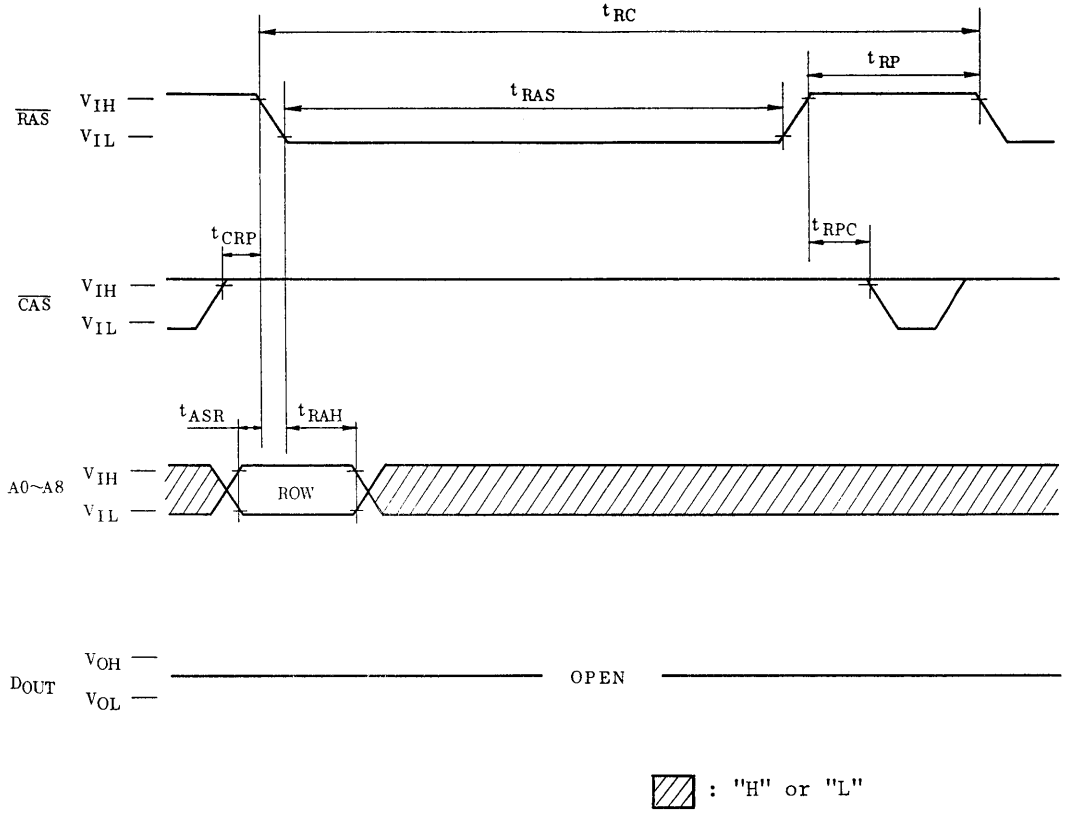
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

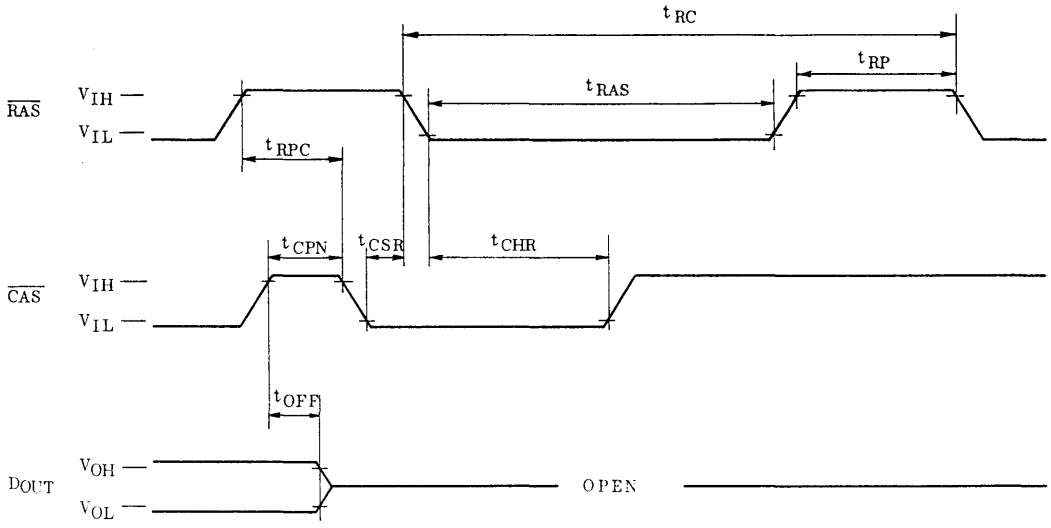


$\overline{RAS}$ ONLY REFRESH CYCLE



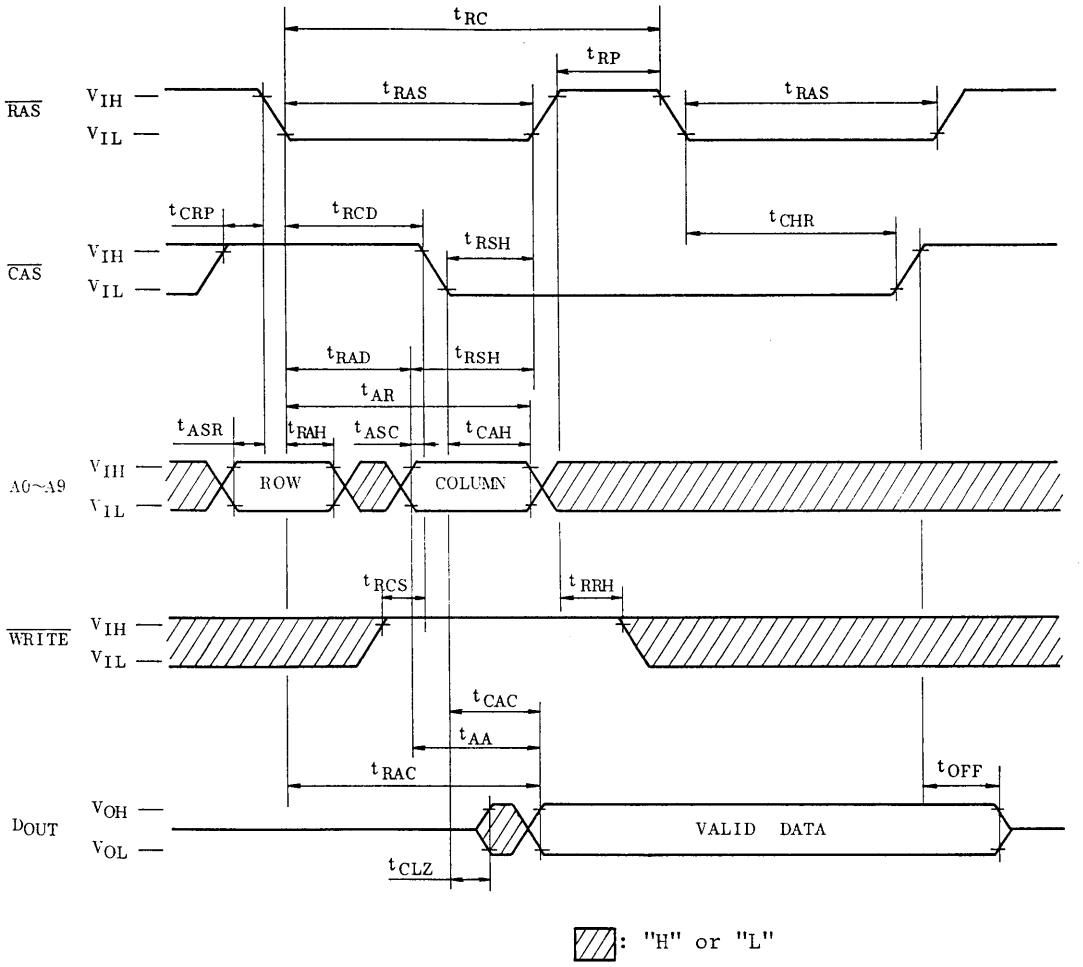
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

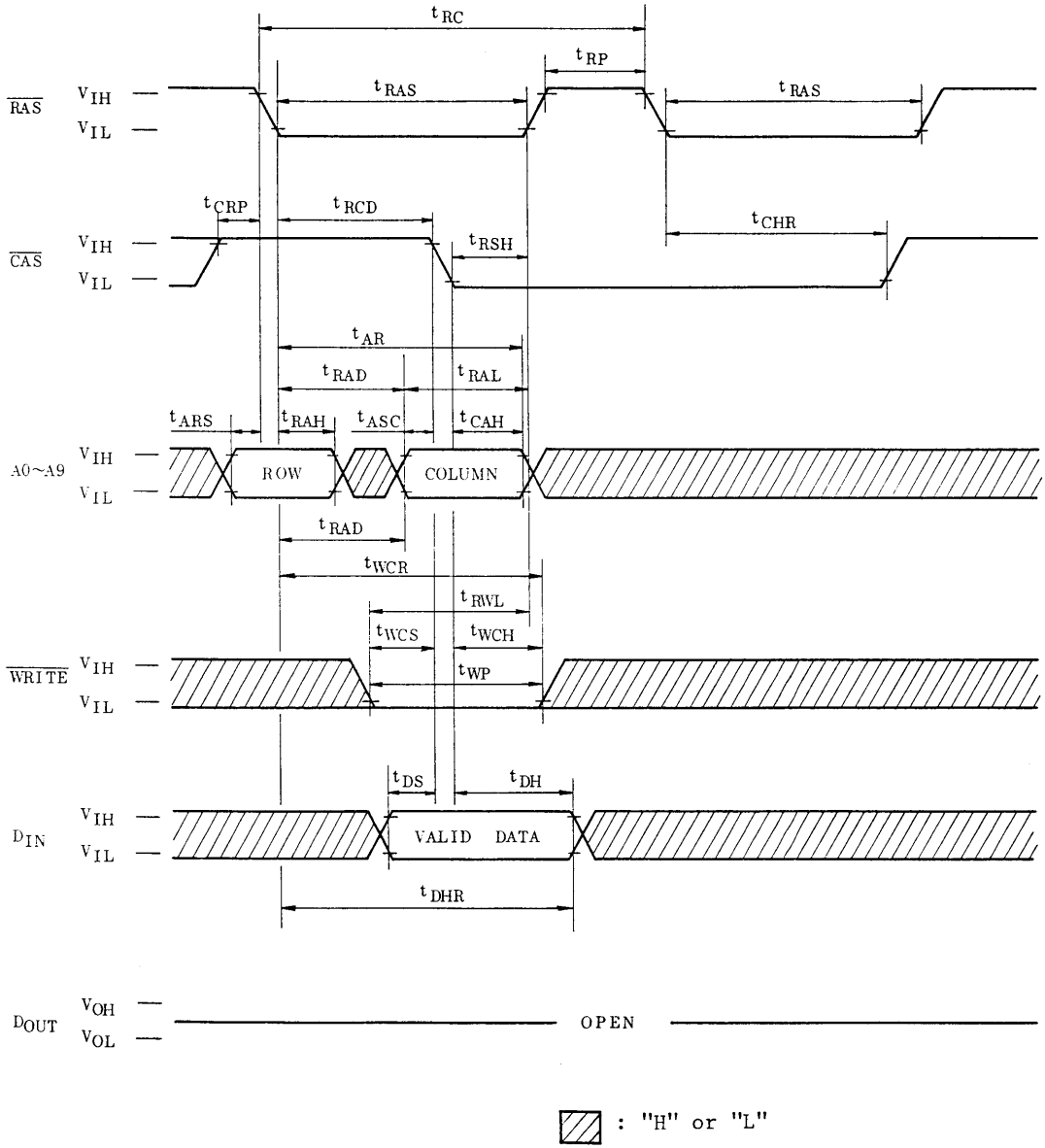


NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

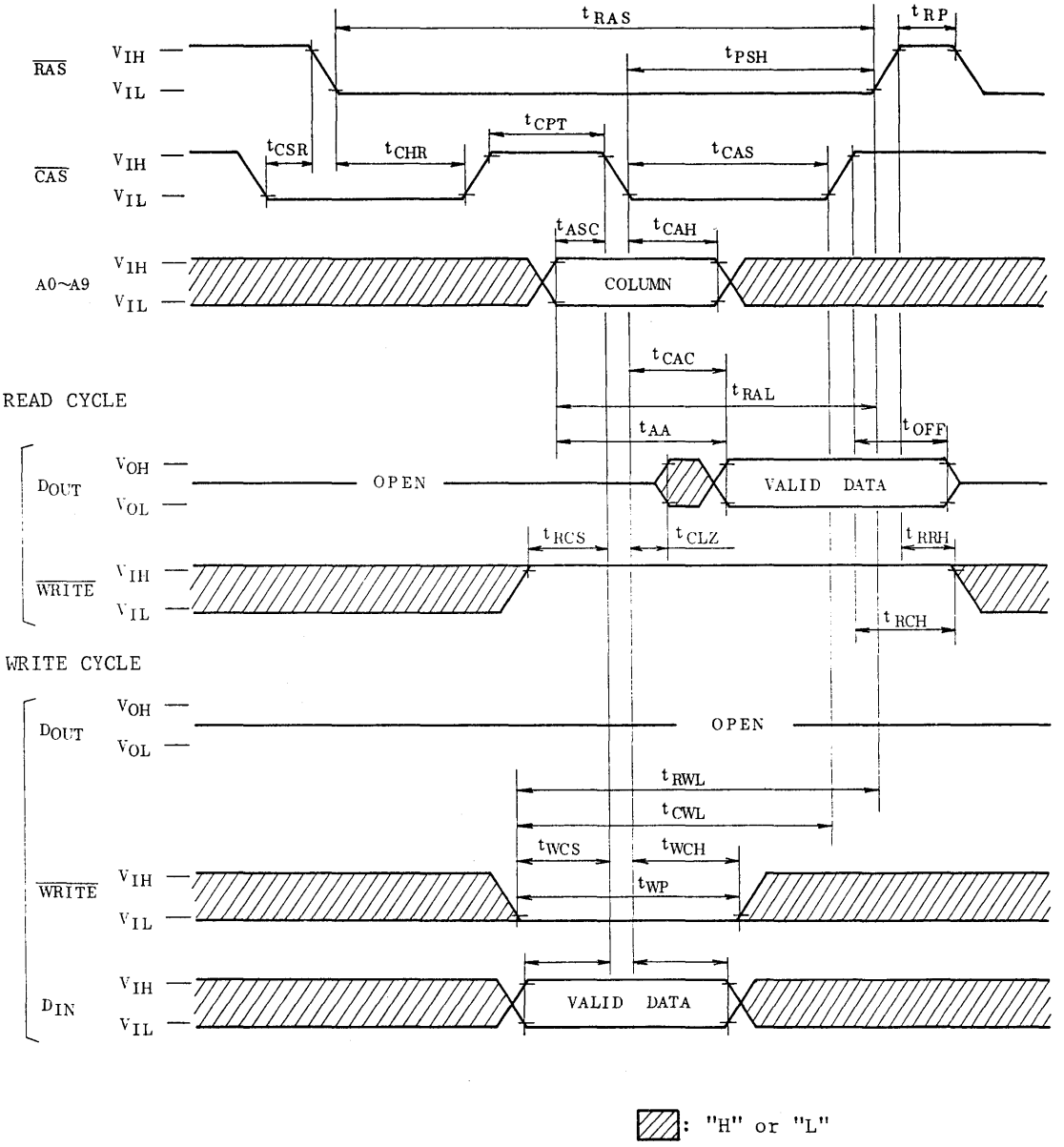
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

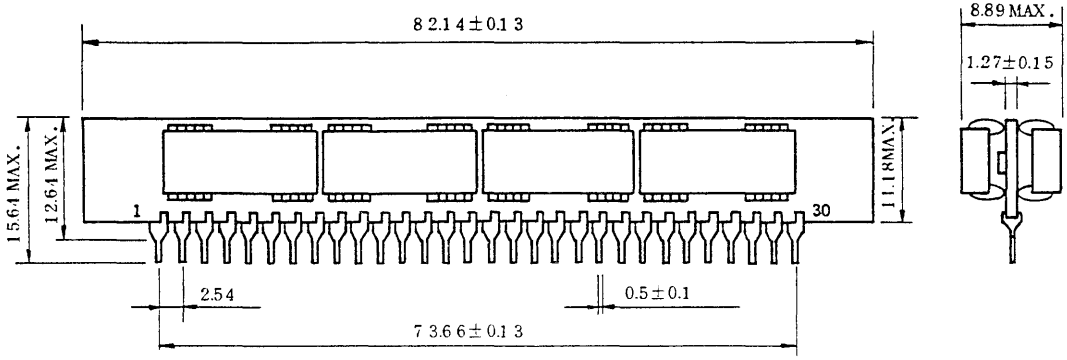


OUTLINE DRAWINGS

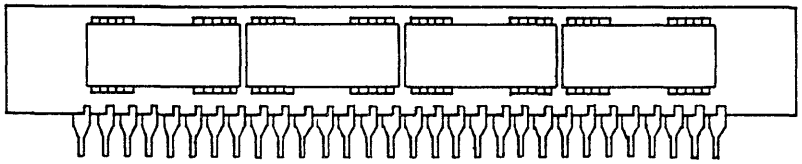
• THM81021L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



THM81022L-85, 10, 12

DESCRIPTION

The THM81022 is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511002J on both sides of the printed circuit board.

The THM81022 is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

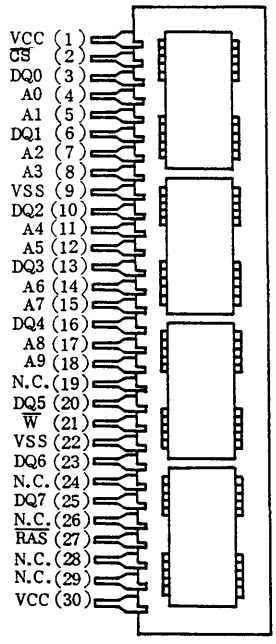
- 1,048,576 words by 8 bits organization
- Fast access time

		THM81022L-85	THM81022L-10	THM81022L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10%
- Low power
  - 3,080mW MAX. Operating(THM81022L-85)
  - 2,640mW MAX. Operating(THM81022L-10)
  - 2,200mW MAX. Operating(THM81022L-12)
  - 44mW MAX. Standby
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Package Height

PIN CONNECTION

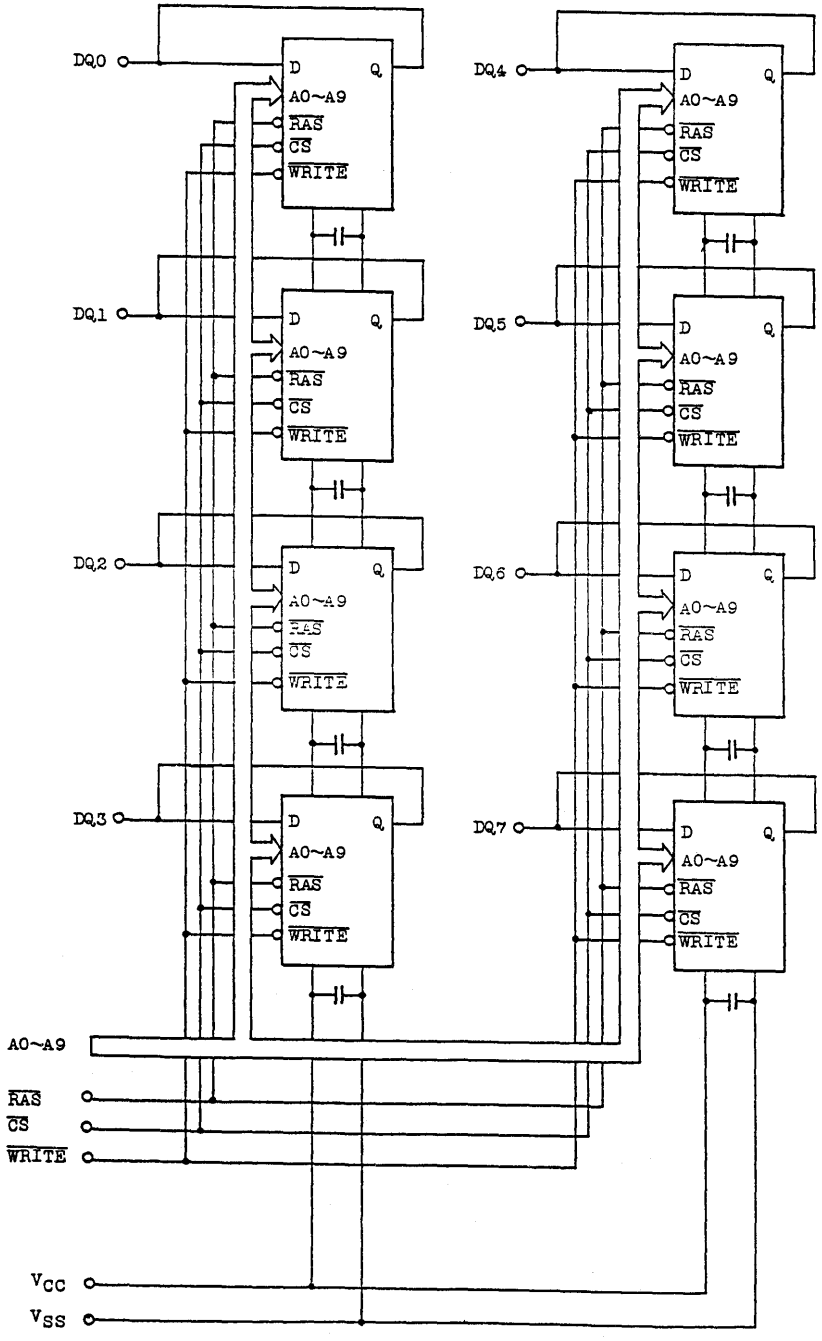
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM81022L-85	-	560	mA	3,4
		THM81022L-10	-	480		
		THM81022L-12	-	400		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM81022L-85	-	560	mA	3
		THM81022L-10	-	480		
		THM81022L-12	-	400		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IH}, Address Cycleing: t_{SC}=t_{SC} MIN.)	THM81022L-85	-	400	mA	3,4
		THM81022L-10	-	320		
		THM81022L-12	-	240		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM81022L-85	-	560	mA	3
		THM81022L-10	-	480		
		THM81022L-12	-	400		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81022L-85		THM81022L-10		THM81022L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Accsss Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	CS to RAS Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	CS Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM81022L-85		THM81022L-10		THM81022L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

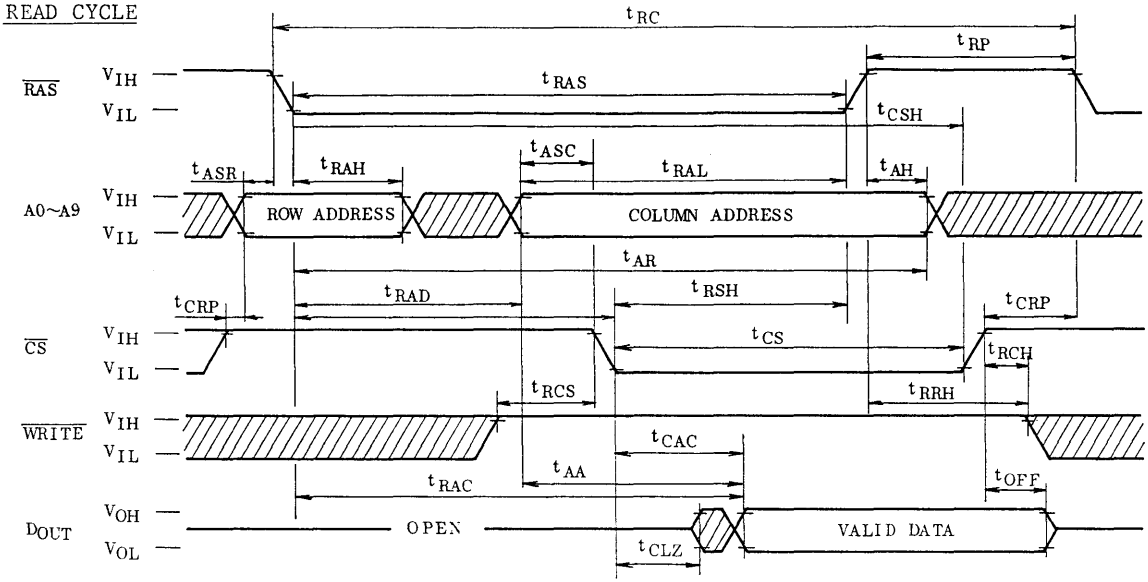
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF

NOTES:

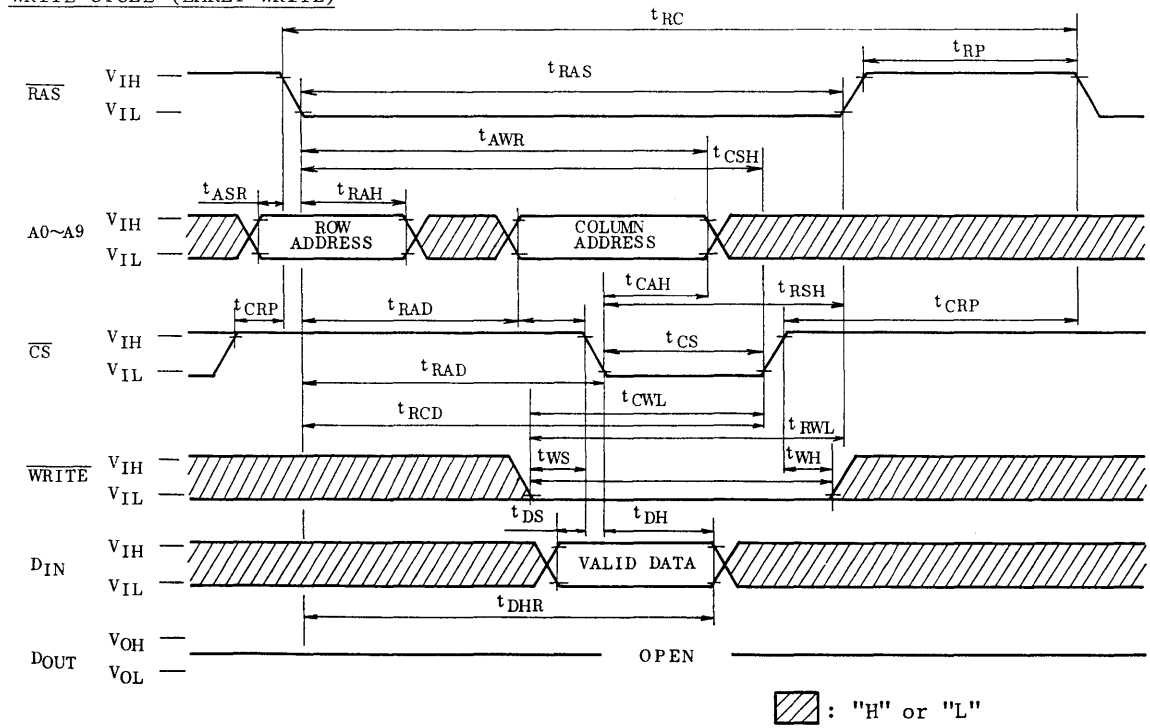
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cuase permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge.
12. t_{WS}, t_{WH} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$(min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be ment. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

READ CYCLE

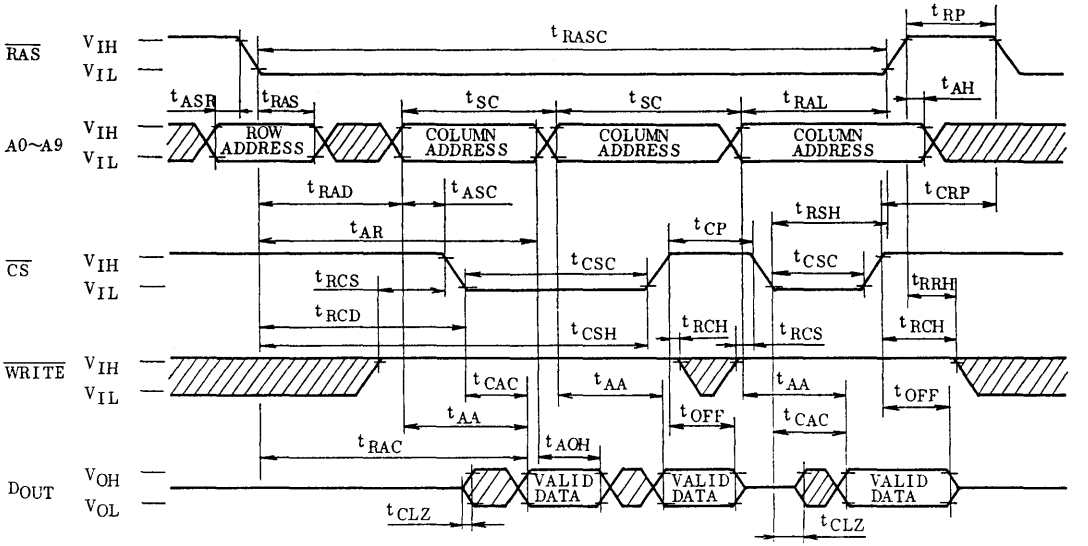


WRITE CYCLE (EARLY WRITE)

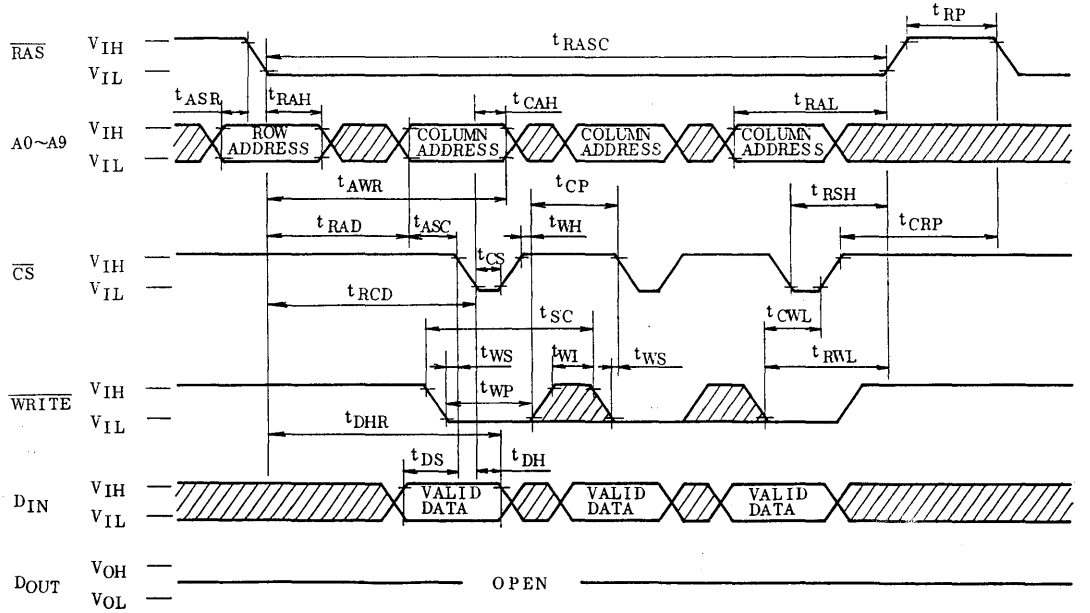


▨ : "H" or "L"

STATIC COLUMN MODE READ CYCLE

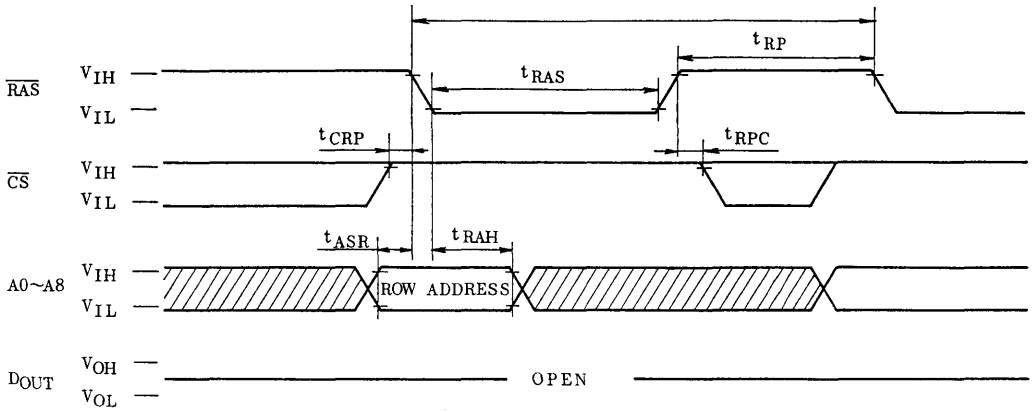


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



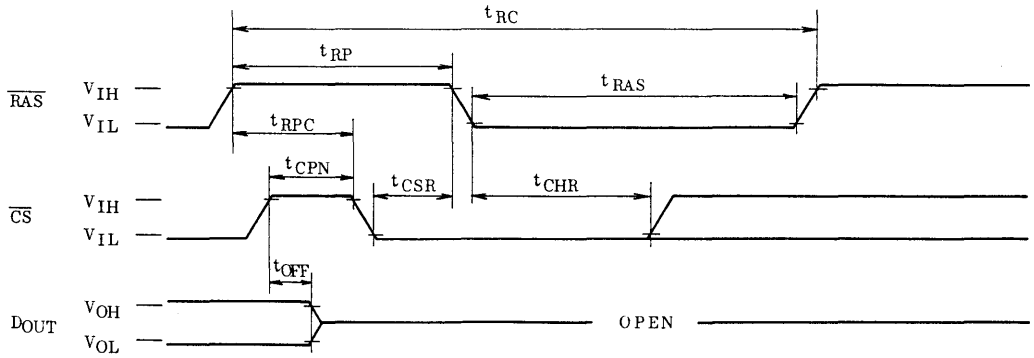
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



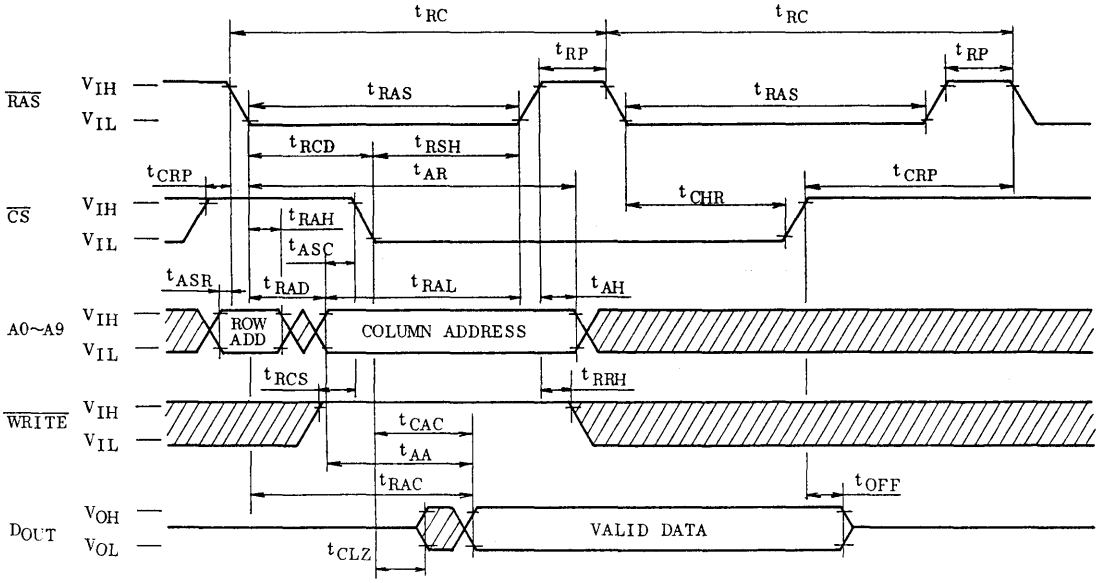
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

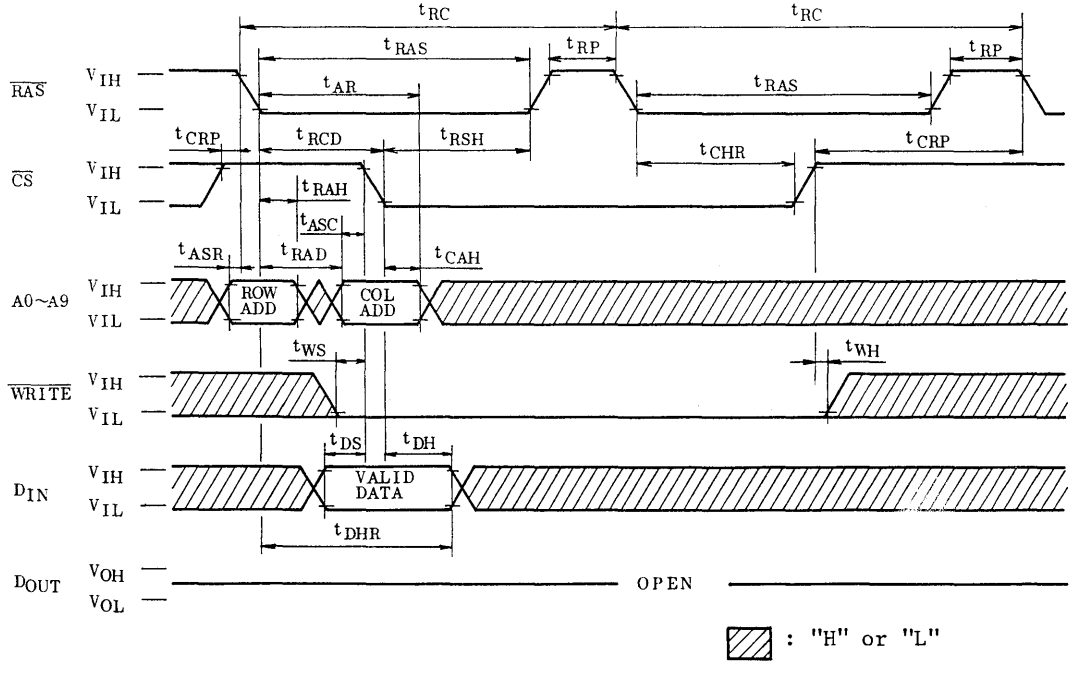


NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

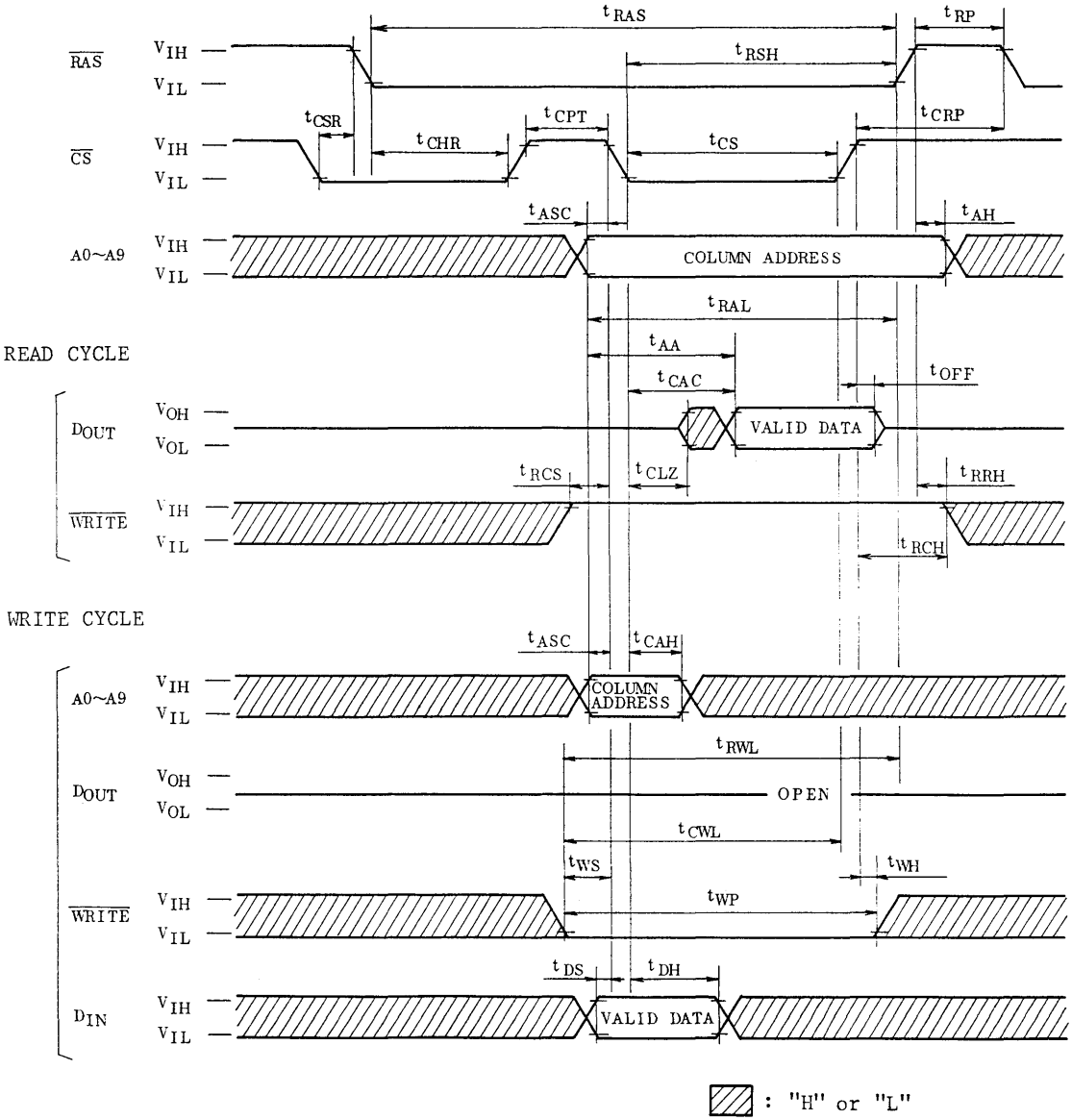
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

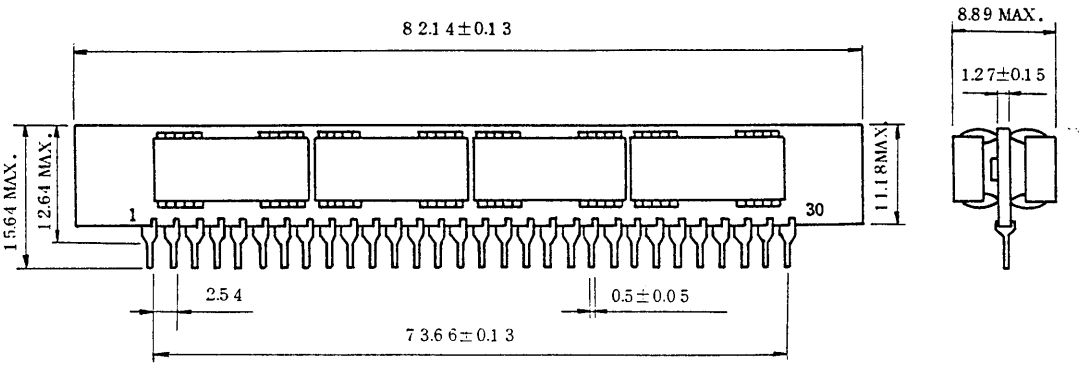


OUTLINE DRAWINGS

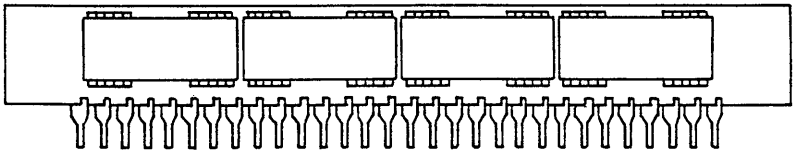
• THM81022L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



THM91000S/L-85, 10, 12

DESCRIPTION

The THM91000S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000J on the printed circuit board.

The THM91000S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

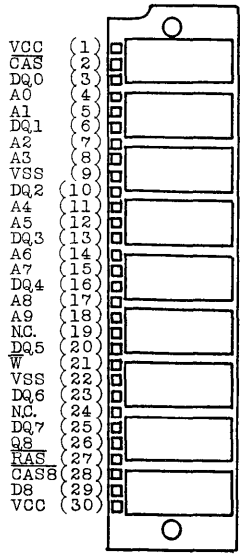
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91000S/L-85	THM91000S/L-10	THM91000S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V±10%
- Low power
  - 3,465mW MAX. Operating (THM91000S/L-85)
  - 2,970mW MAX. Operating (THM91000S/L-10)
  - 2,475mW MAX. Operating (THM91000S/L-12)
  - 49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

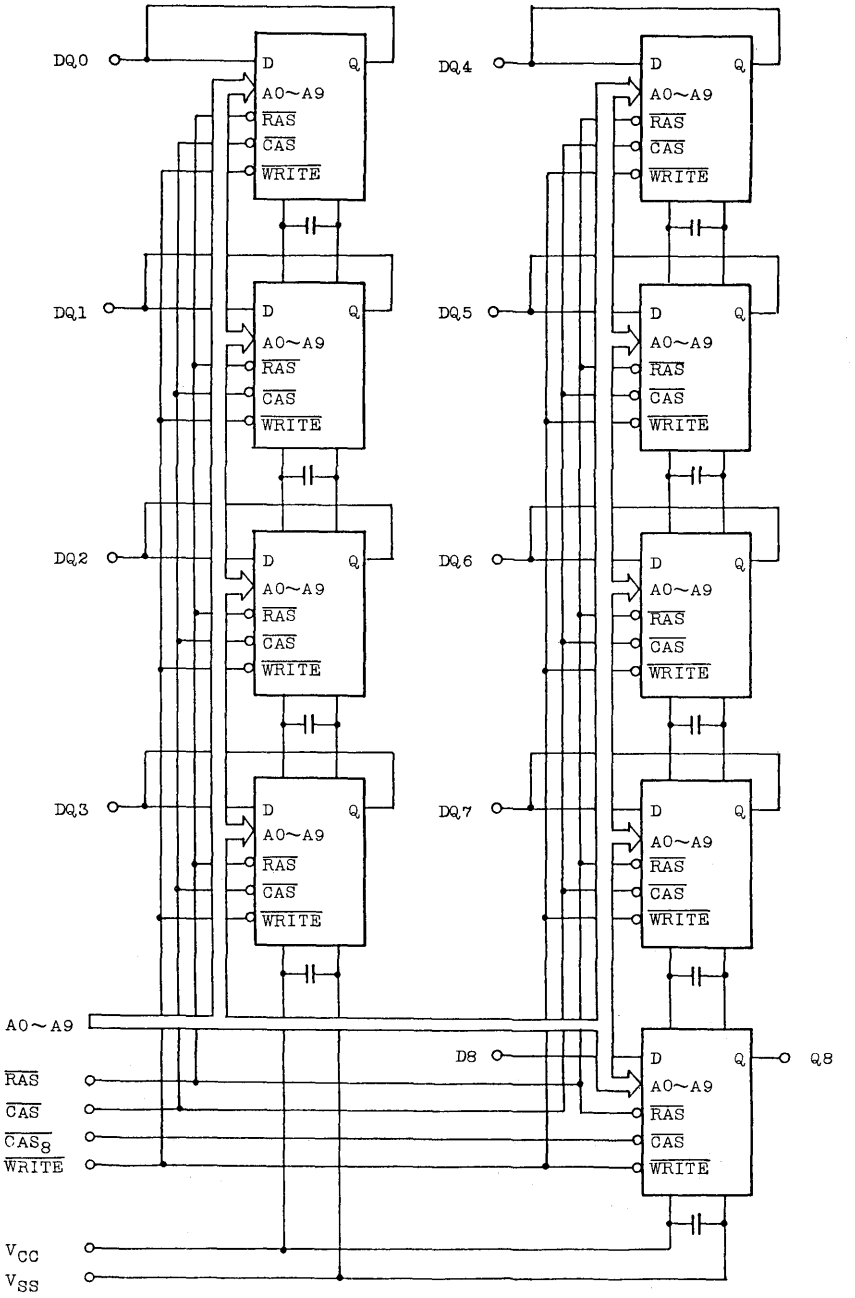
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-85	-	630	mA	3, 4
		THM91000S/L-10	-	540		
		THM91000S/L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-85	-	630	mA	3
		THM91000S/L-10	-	540		
		THM91000S/L-12	-	450		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: $t_{PC}=t_{PC}$ MIN.)	THM91000S/L-85	-	450	mA	3, 4
		THM91000S/L-10	-	360		
		THM91000S/L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91000S/L-85	-	630	mA	3
		THM91000S/L-10	-	540		
		THM91000S/L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C)(Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91000S/L-85		THM91000S/L-10		THM91000S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	30	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91000S/L-85		THM91000S/L-10		THM91000S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF
C_{Q}	Output Capacitance (Q8)	-	10	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

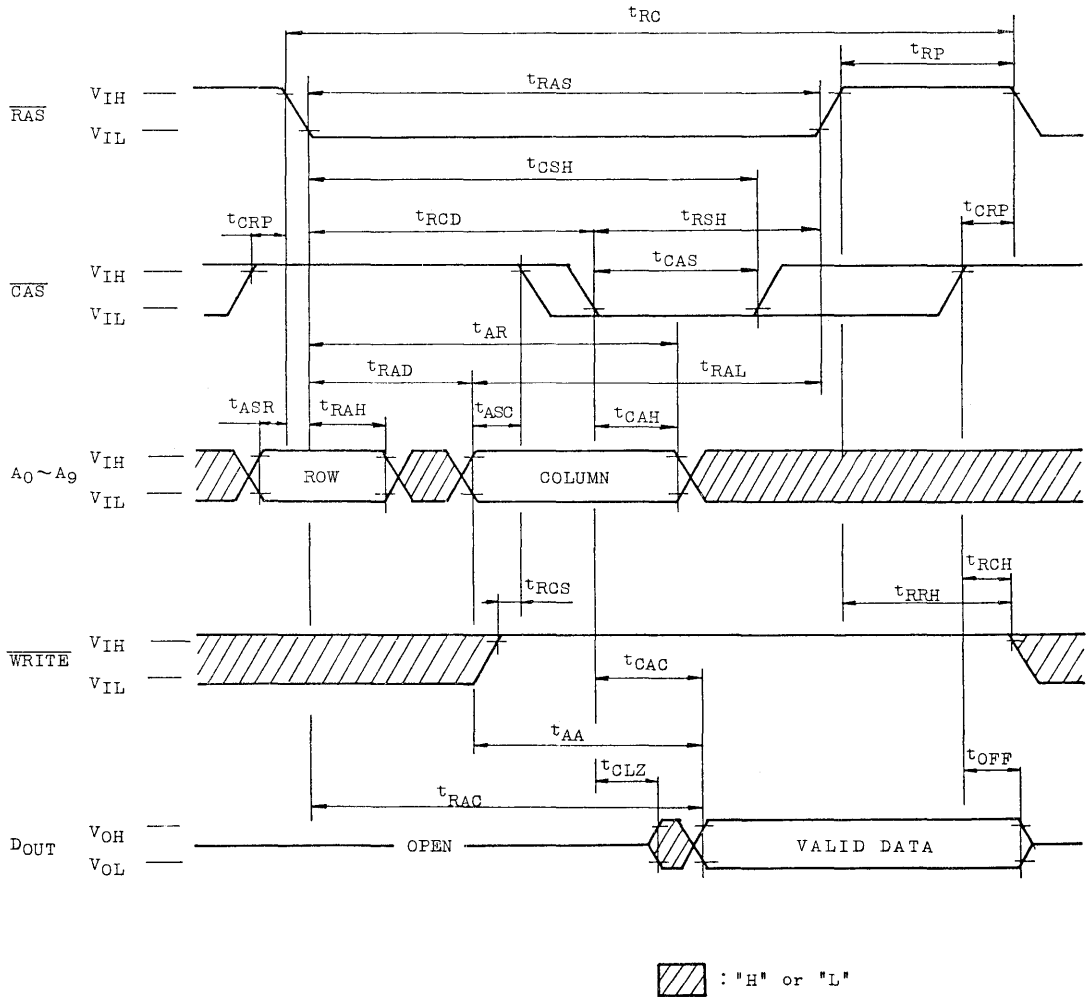
11. These parameters are referenced to $\overline{CAS}$ leading edge.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

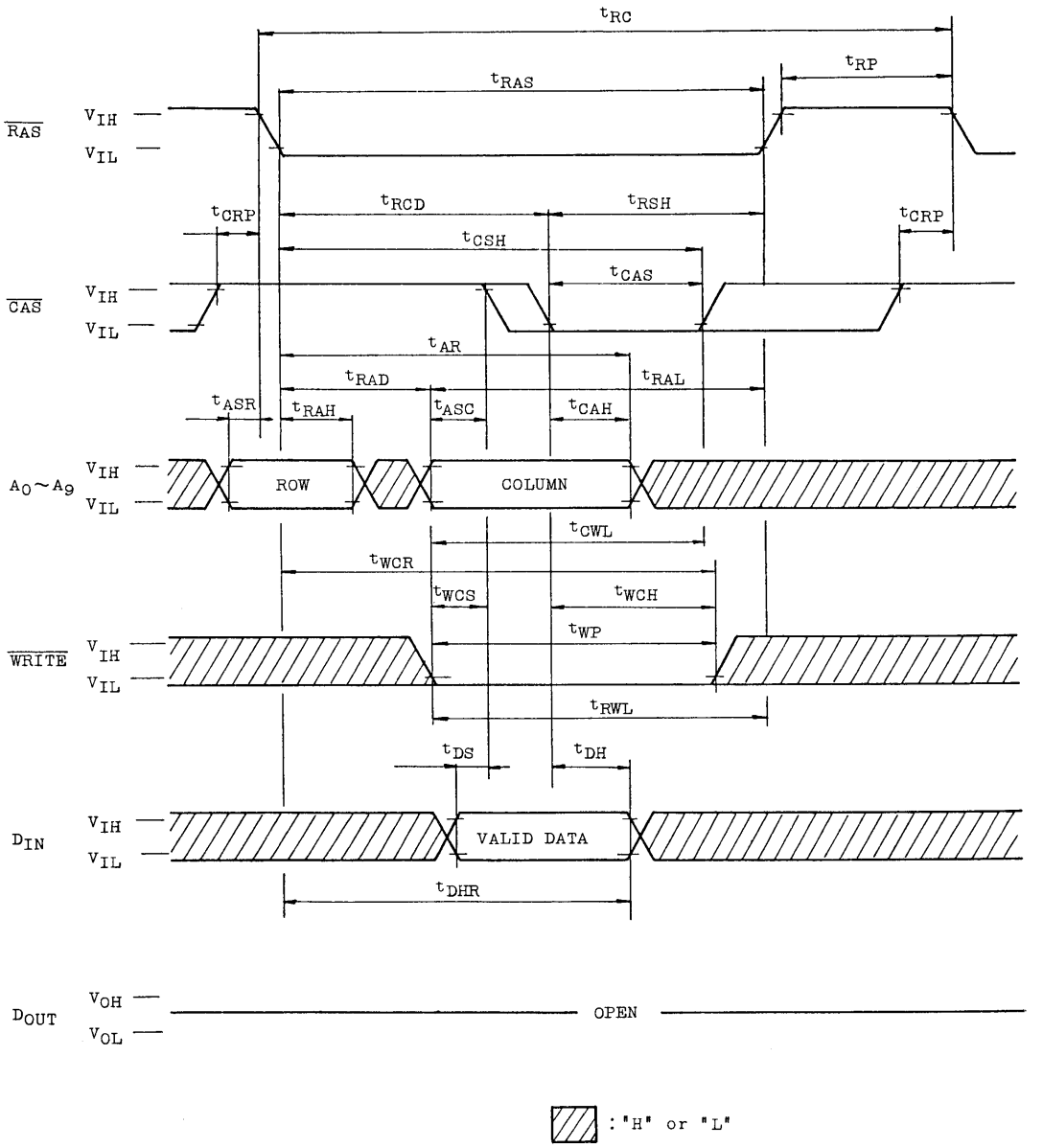
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

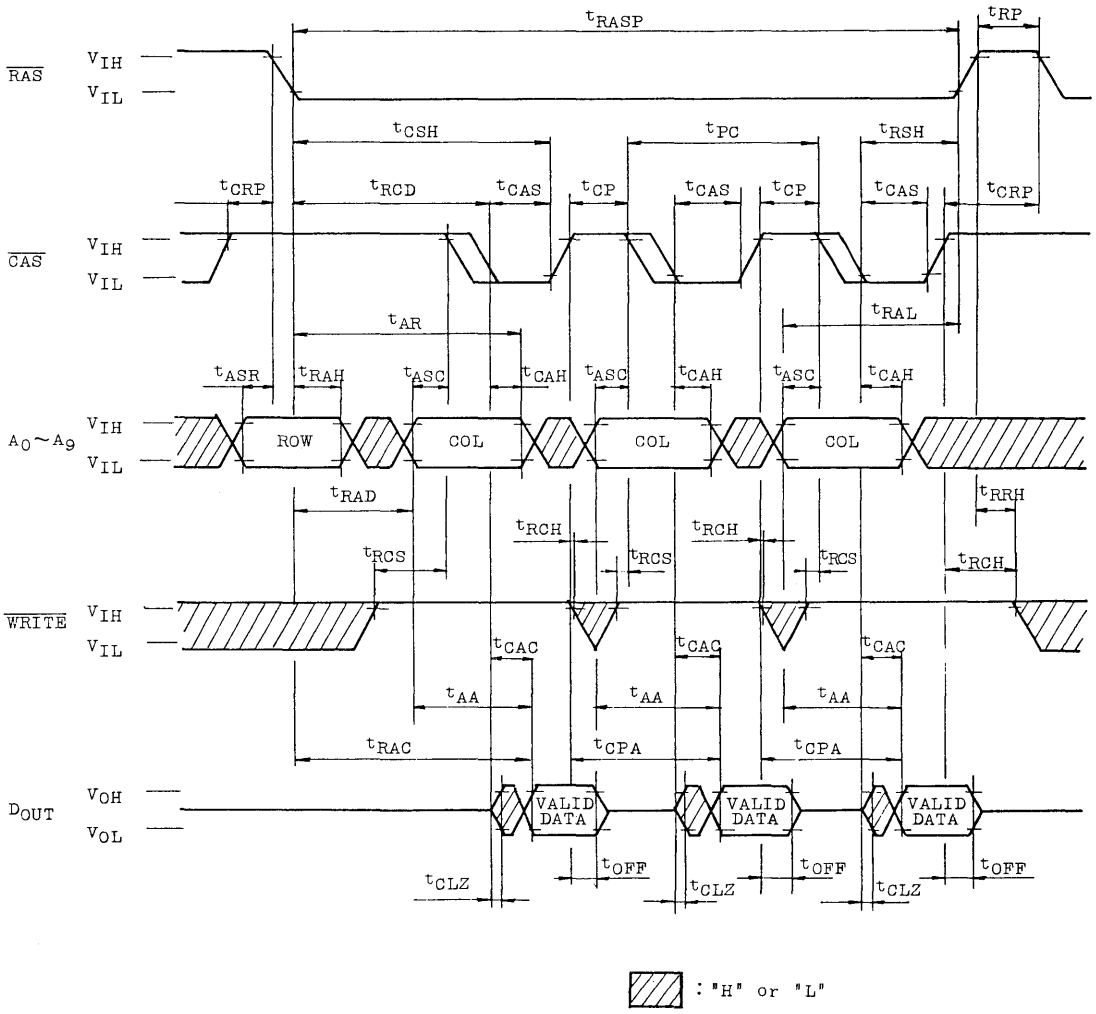
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"

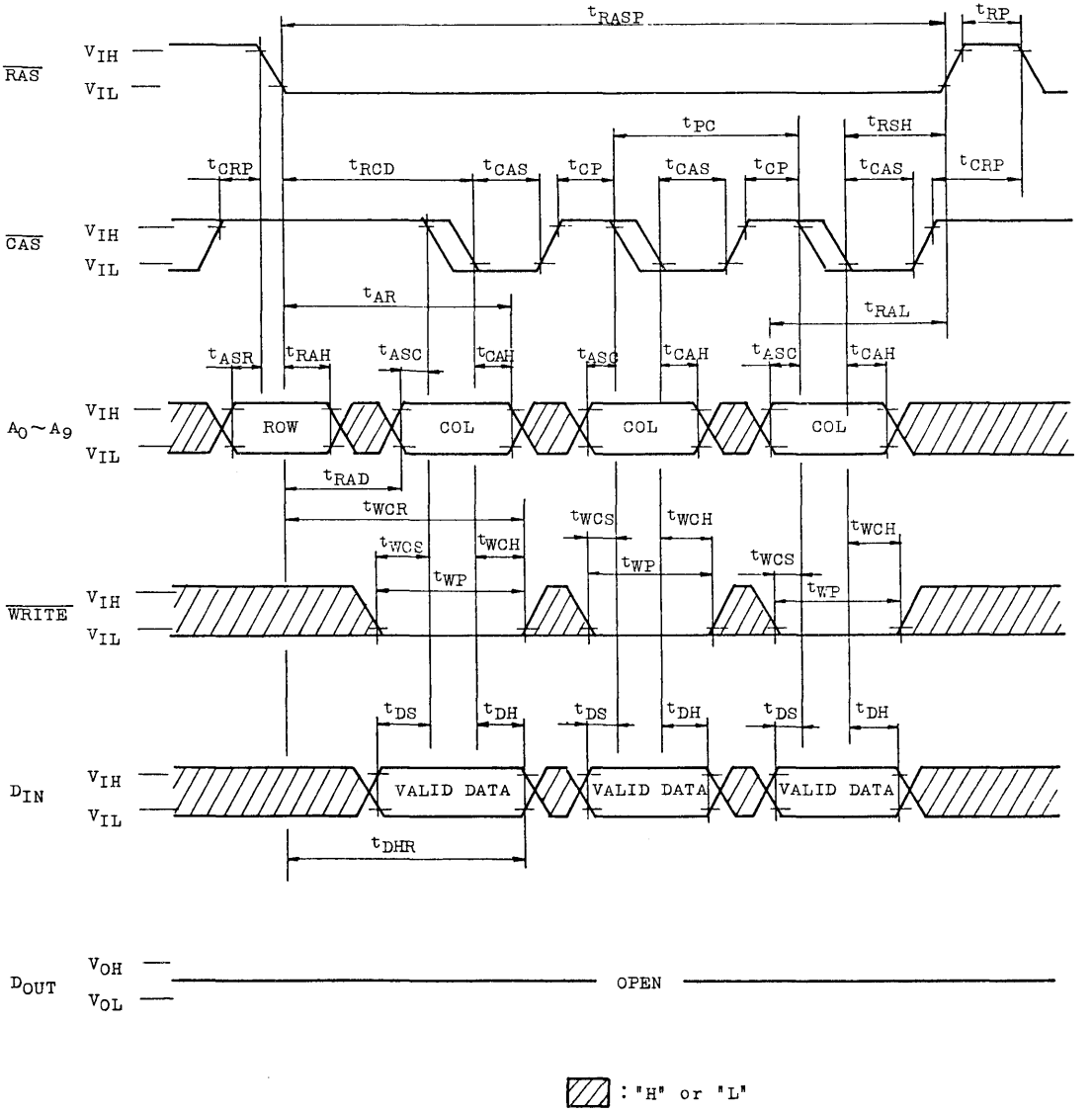
EARLY WRITE CYCLE



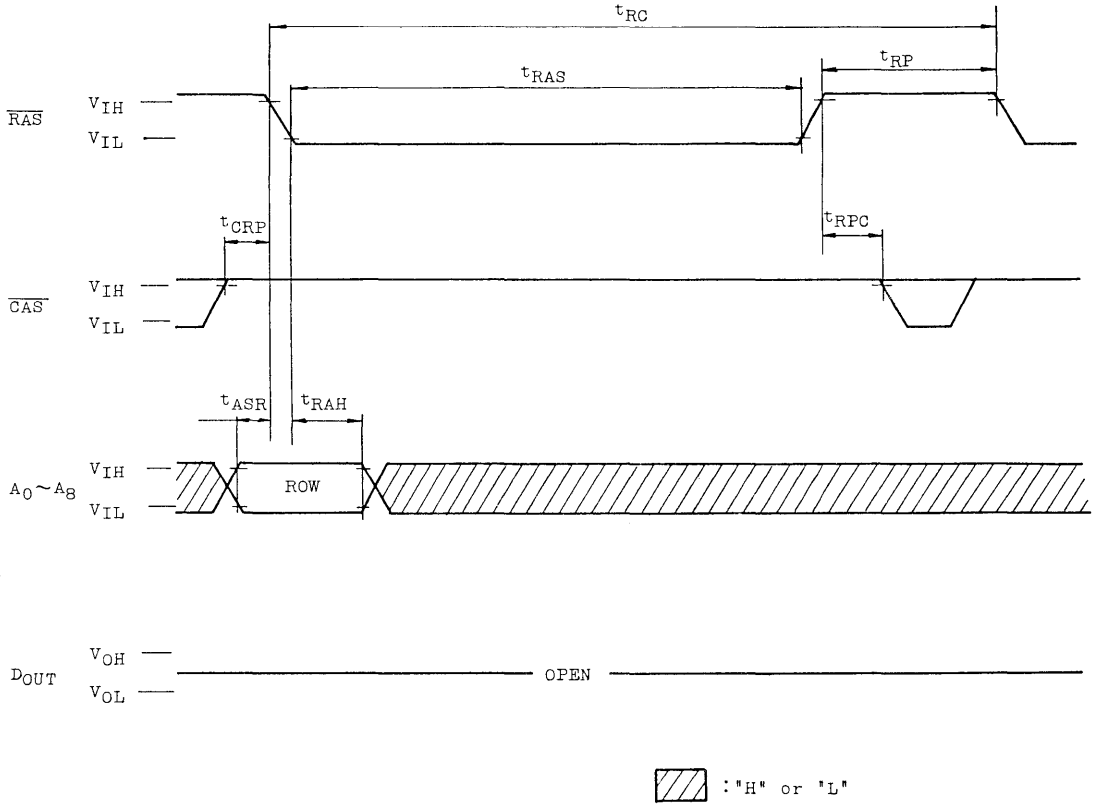
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

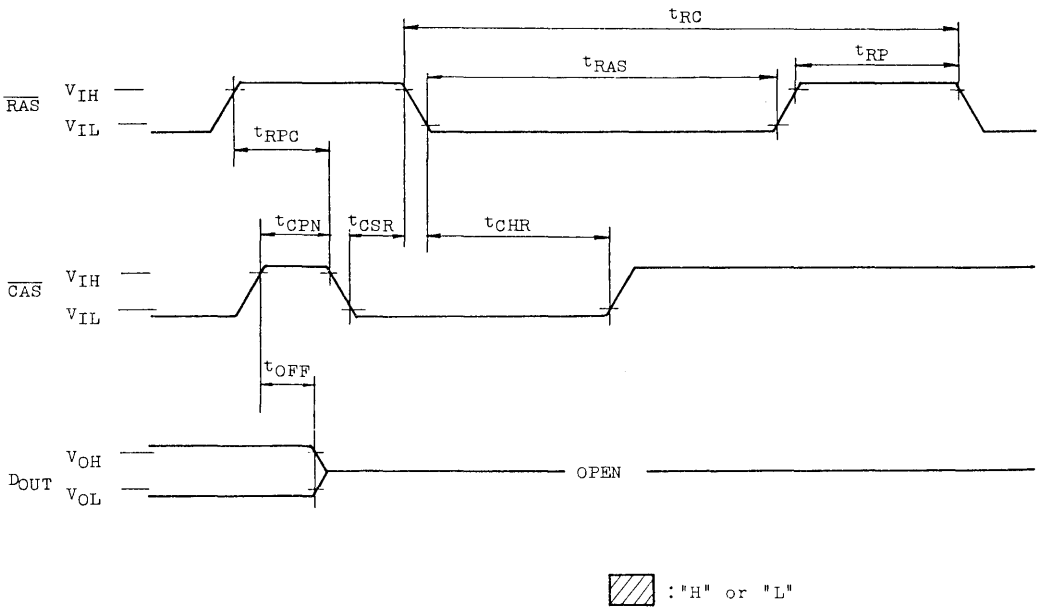


$\overline{RAS}$ ONLY REFRESH CYCLE



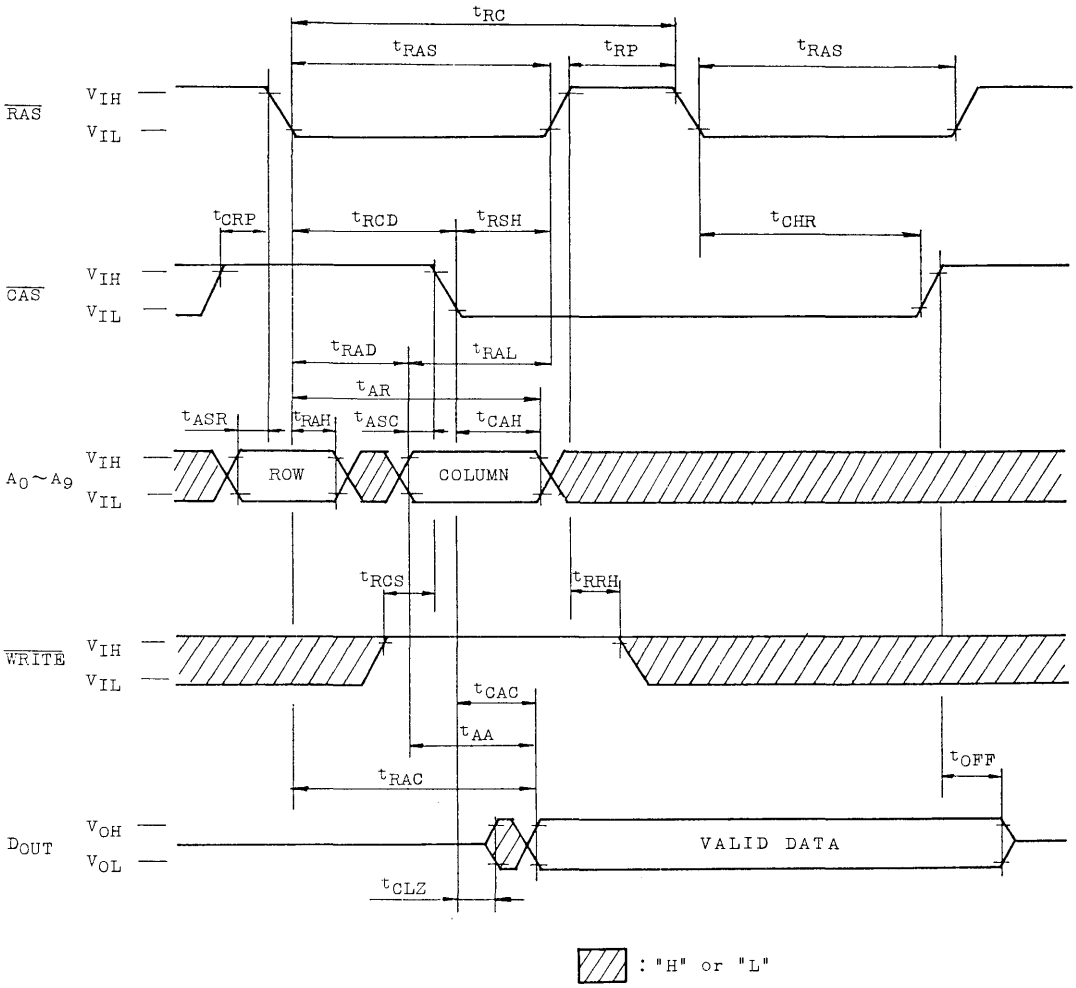
Note: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

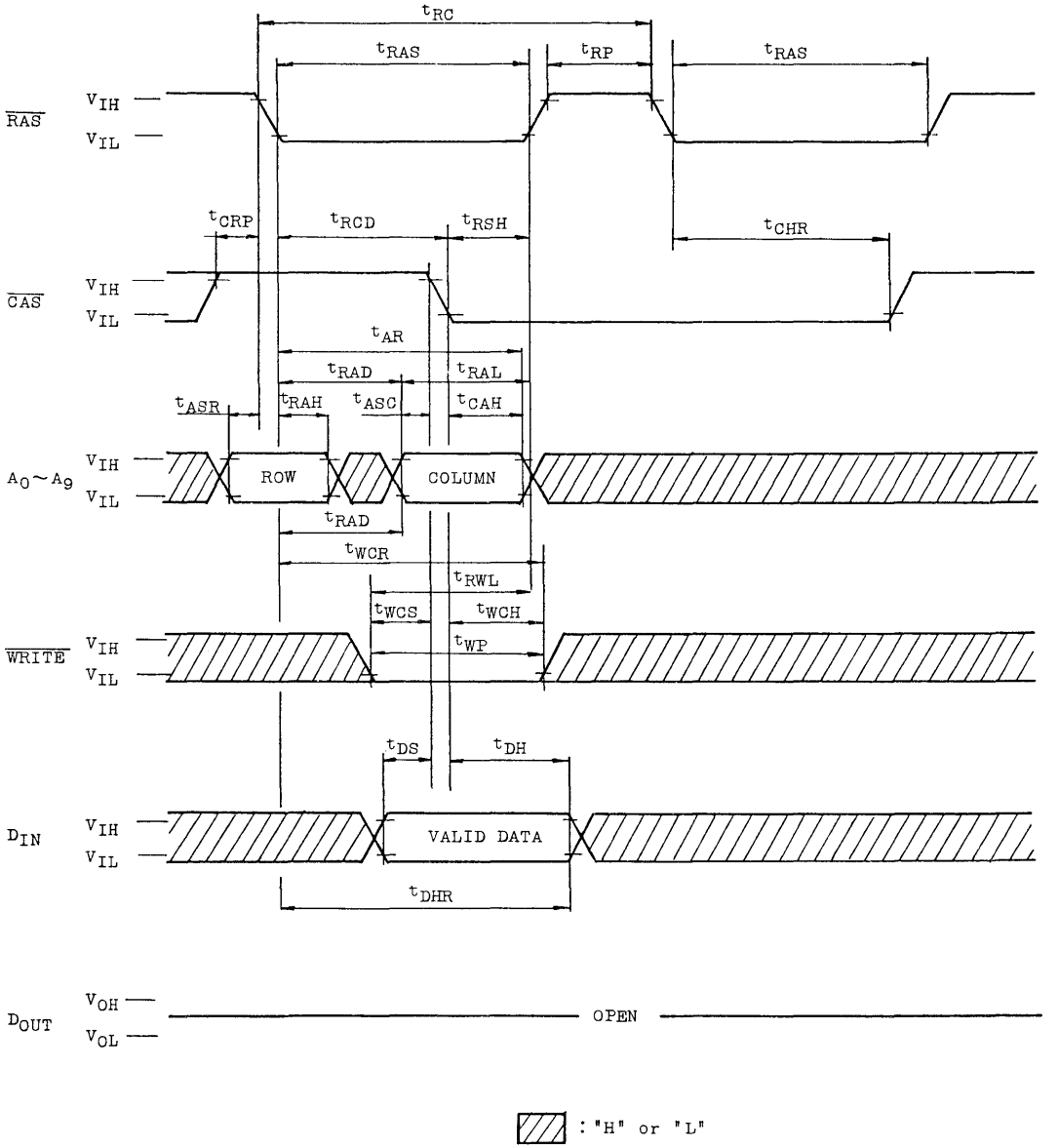


Note: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

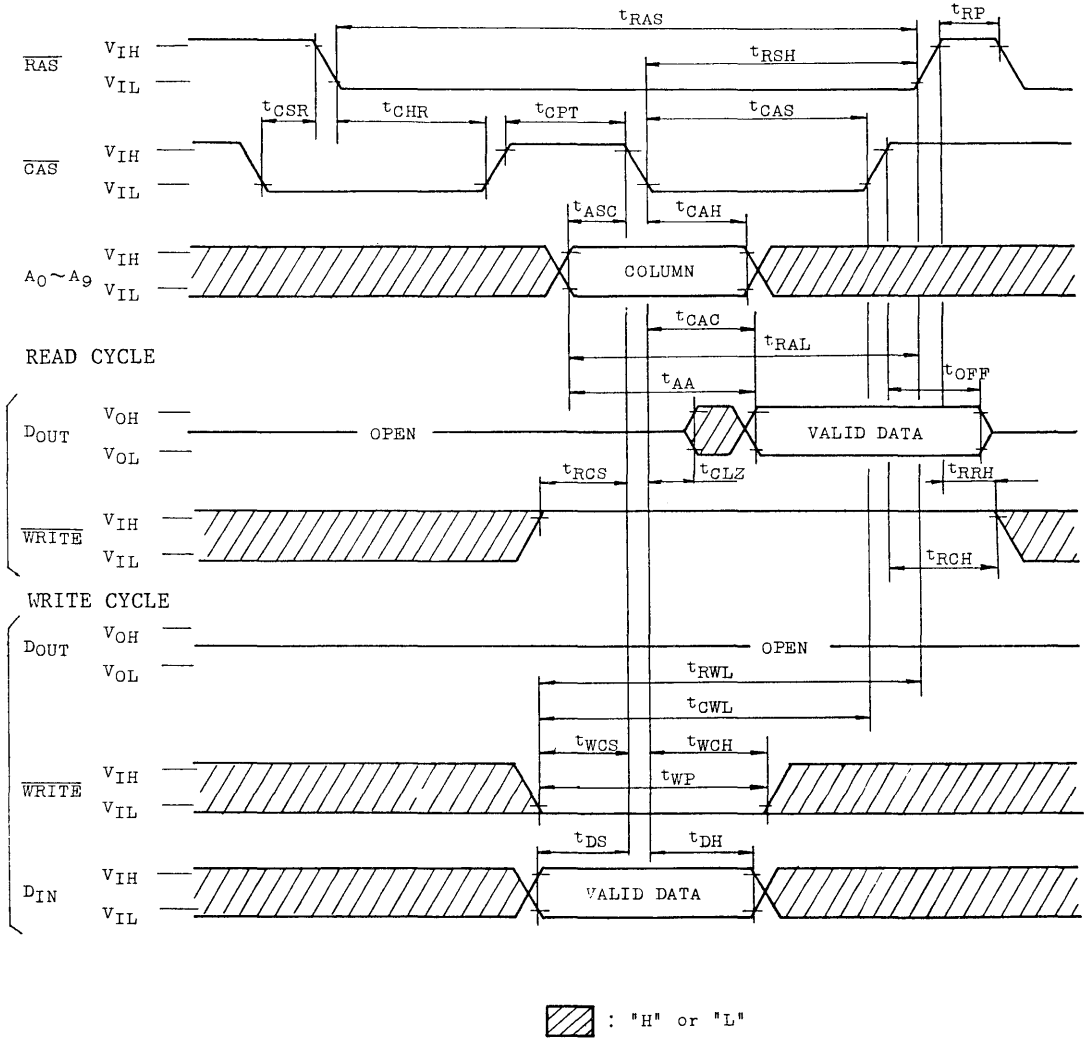
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

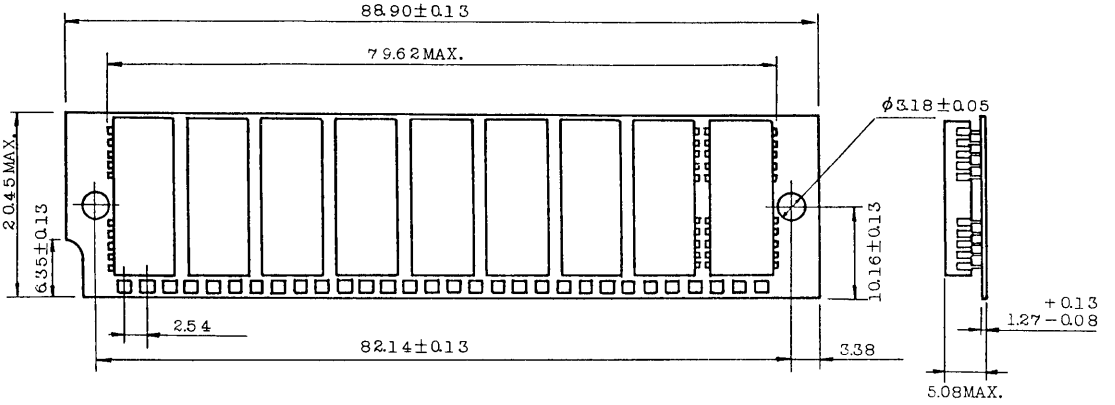


: "H" or "L"

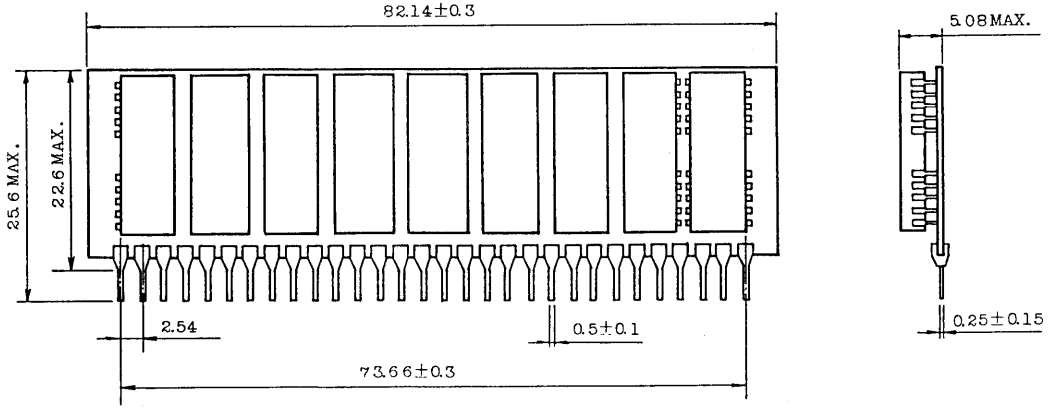
OUTLINE DRAWINGS

• THM91000S

Unit in mm



• THM91000L



THM91001S/L-85, 10, 12

DESCRIPTION

The THM91001S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511001J on the printed circuit board.

The THM91001S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

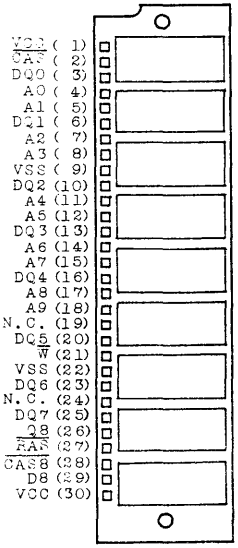
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91001S/L-85	THM91001S/L-10	THM91001S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

- Single power supply of 5V+10%
- Low power
  3,465mW MAX. Operating (THM91001S/L-85)
  2,970mW MAX. Operating (THM91001S/L-10)
  2,475mW MAX. Operating (THM91001S/L-12)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Nibble Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

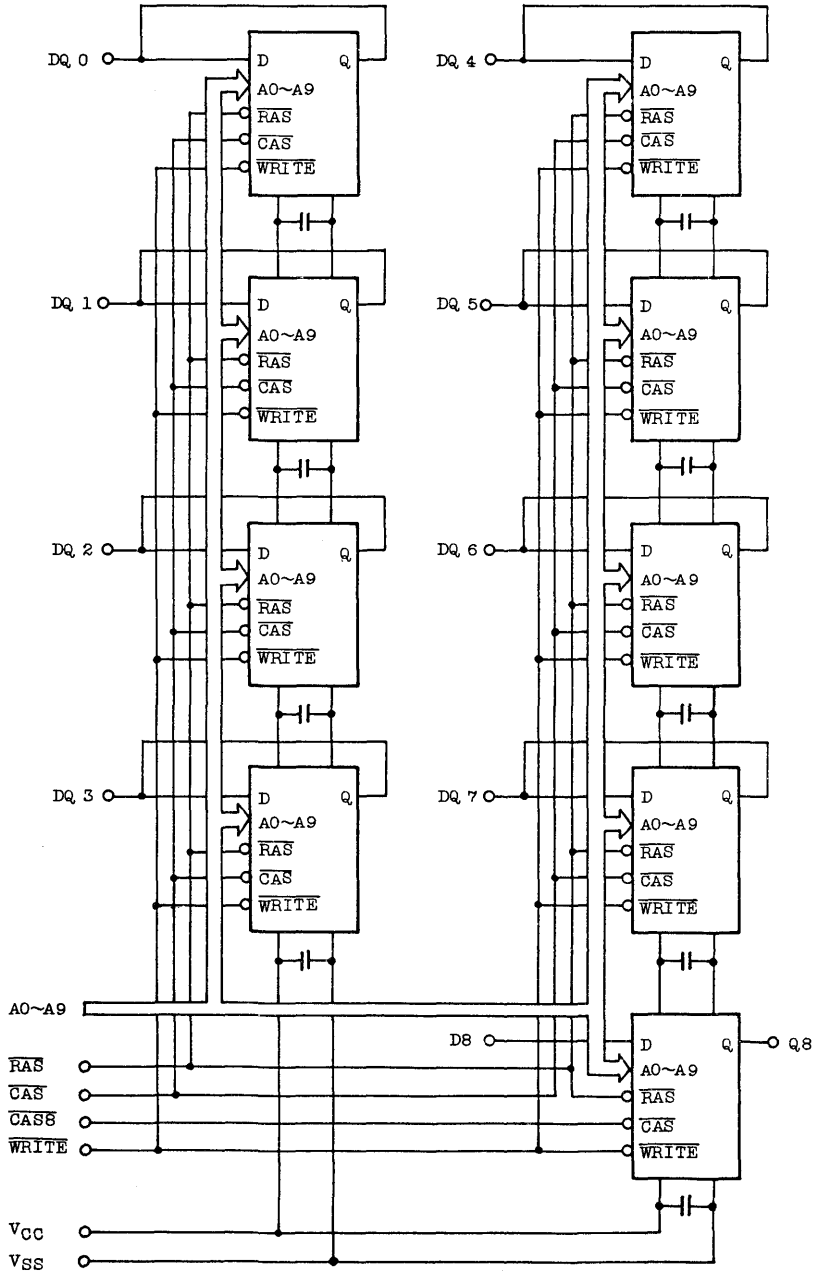
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91001S/L-85	-	630	mA	3, 4
		THM91001S/L-10	-	540		
		THM91001S/L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	THM91001S/L-85	-	630	mA	3
		THM91001S/L-10	-	540		
		THM91001S/L-12	-	450		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Cycling: $t_{NC}=t_{NC}$ MIN.)	THM91001S/L-85	-	450	mA	3, 4
		THM91001S/L-10	-	360		
		THM91001S/L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}$-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91001S/L-85	-	630	mA	3
		THM91001S/L-10	-	540		
		THM91001S/L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91001S/L-85		THM91001S/L-10		THM91001S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91001S/L-85		THM91001S/L-10		THM91001S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	

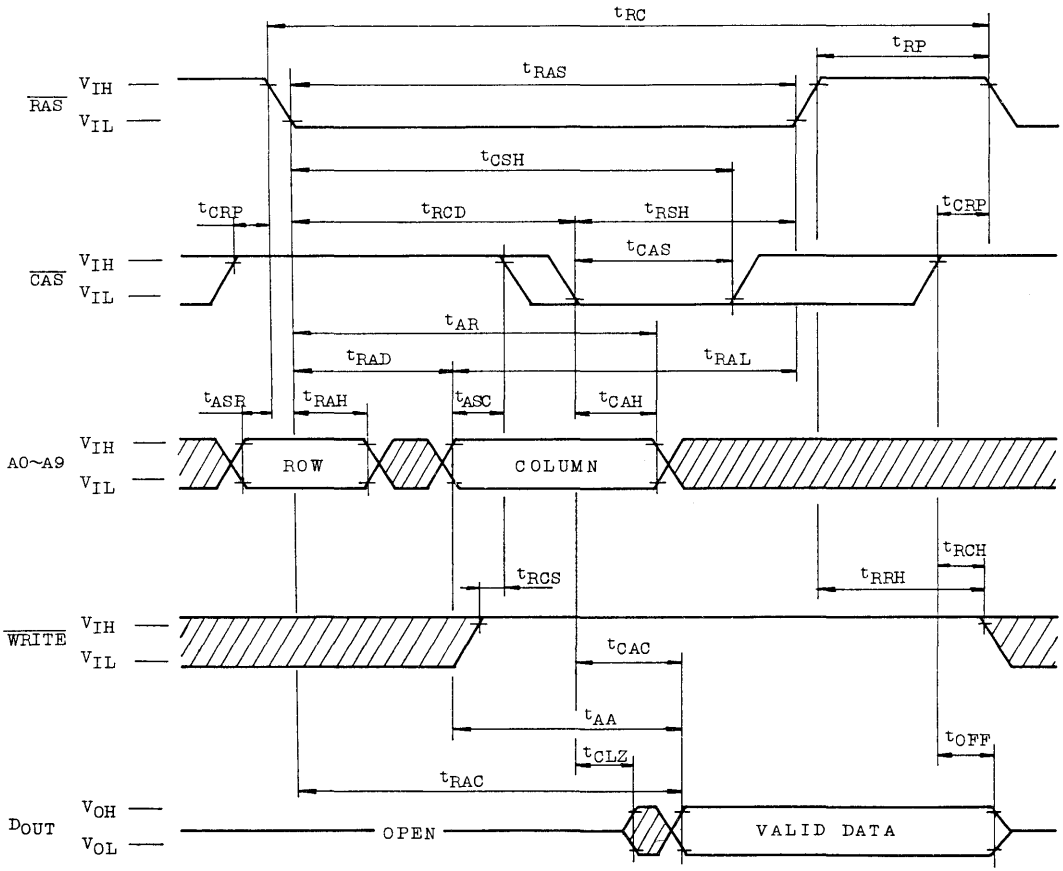
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF
C_{Q}	Output Capacitance (Q8)	-	10	pF

NOTES:

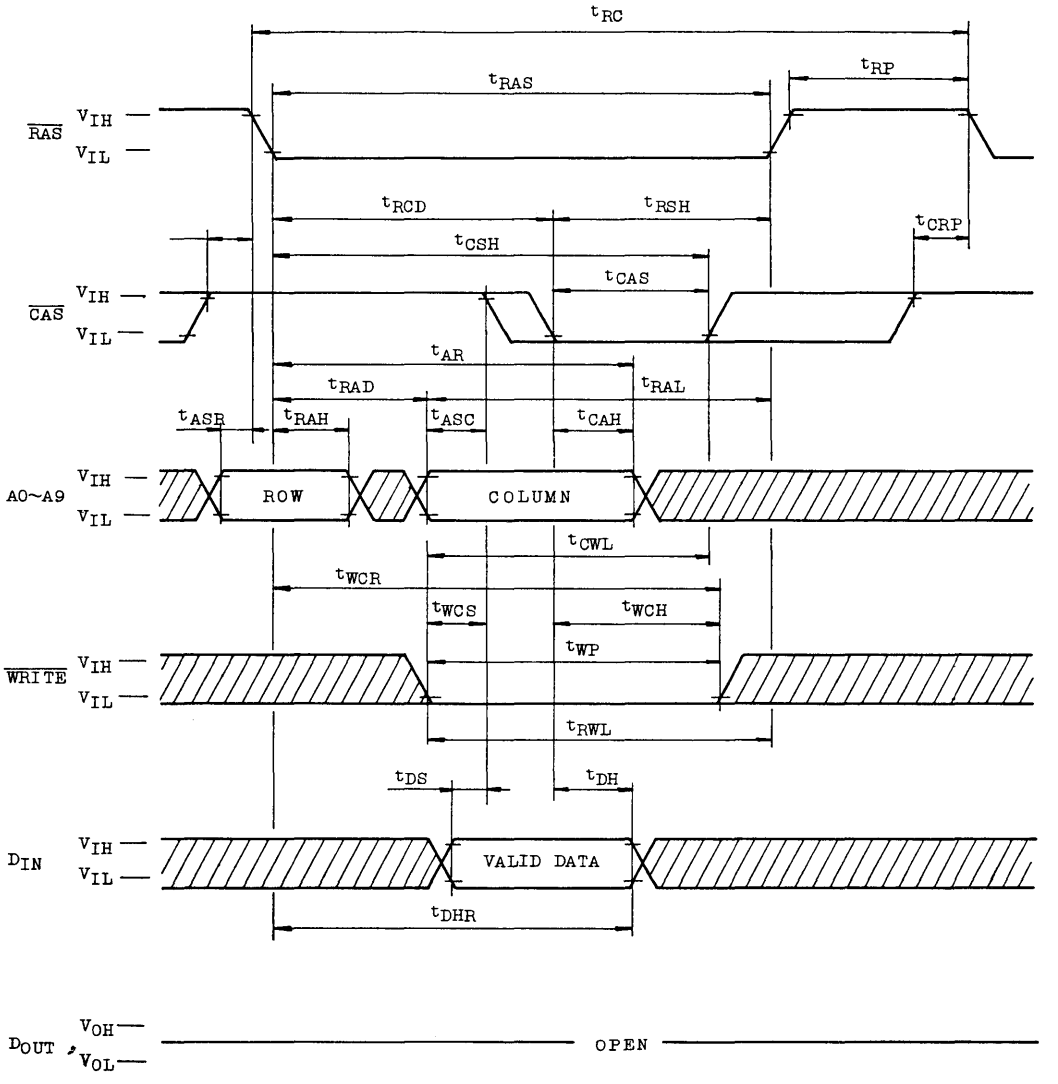
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



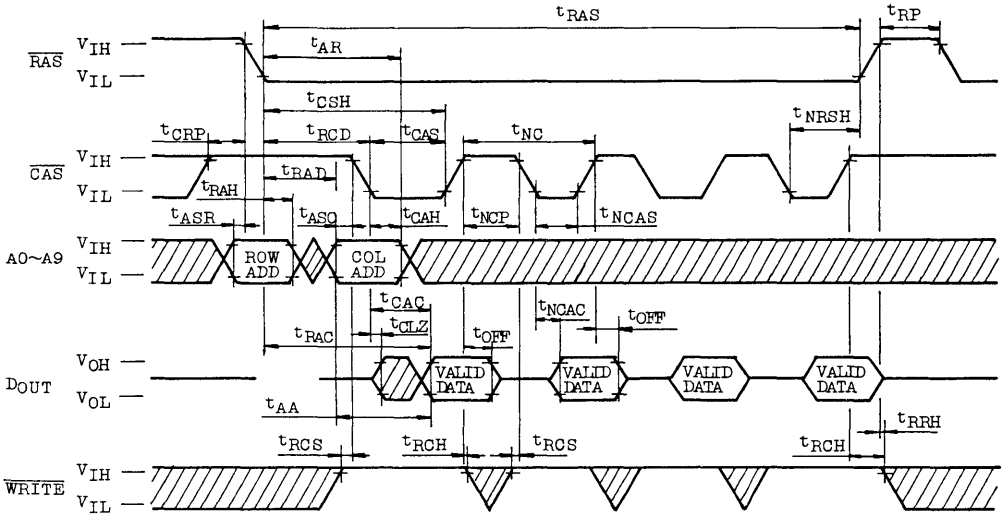
: "H" or "L"

EARLY WRITE CYCLE

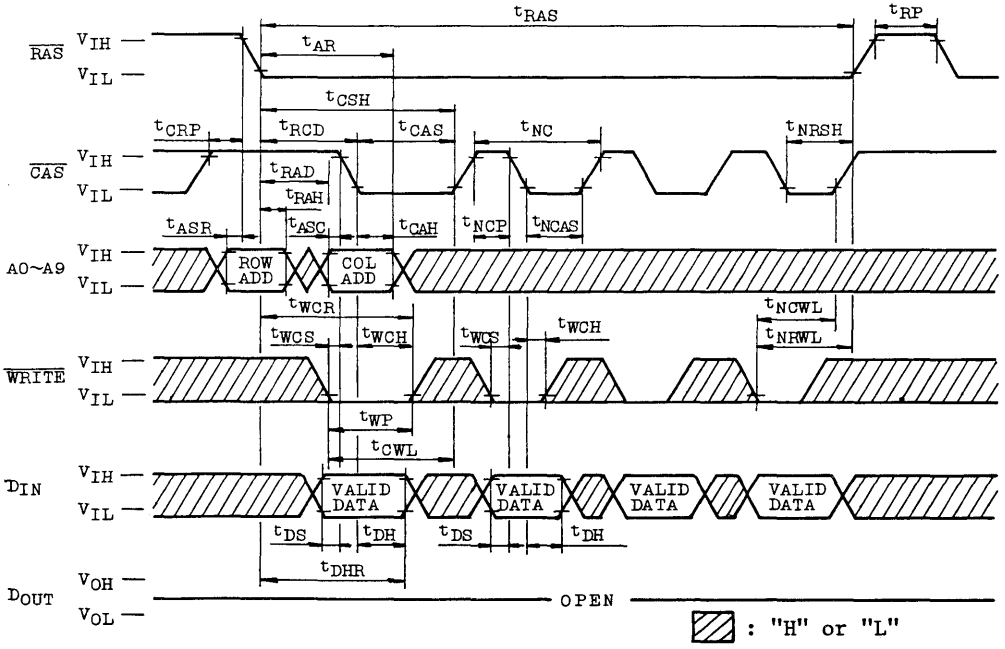


▨ : "H" or "L"

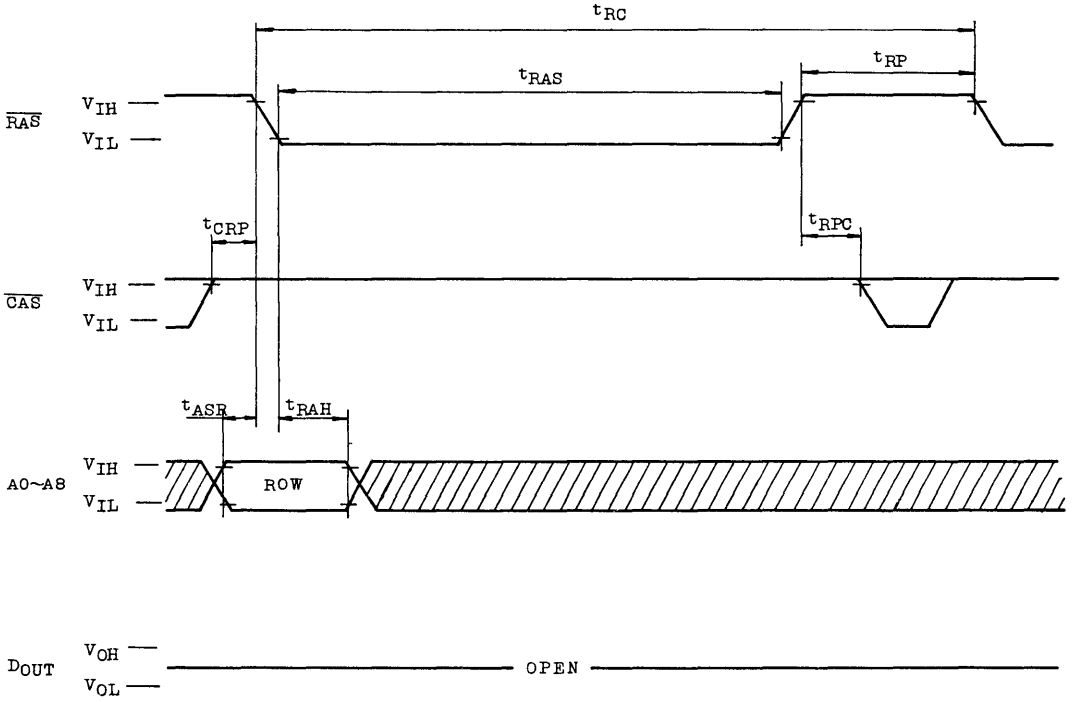
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

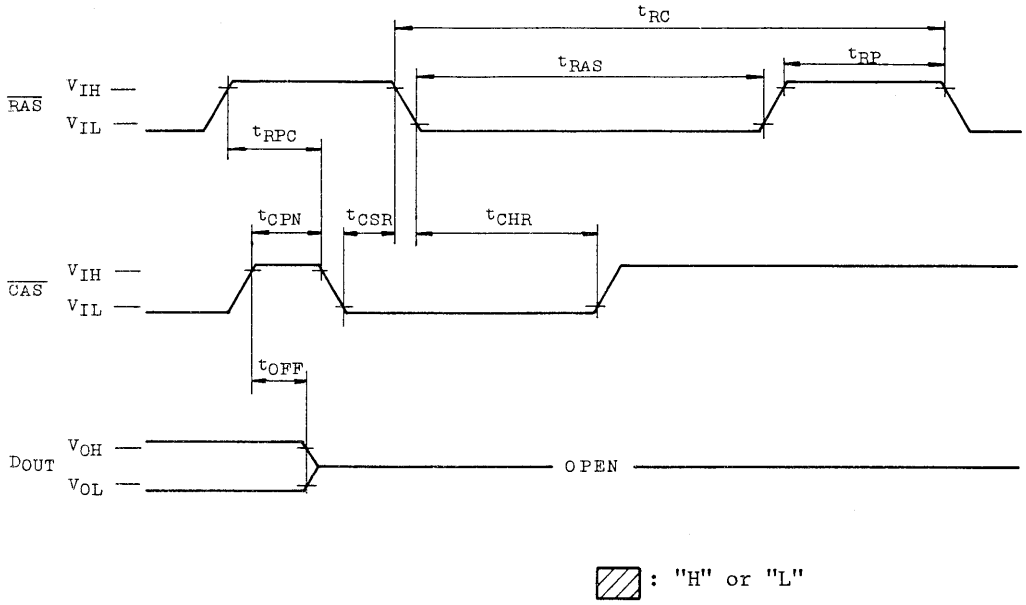


$\overline{RAS}$ ONLY REFRESH CYCLE



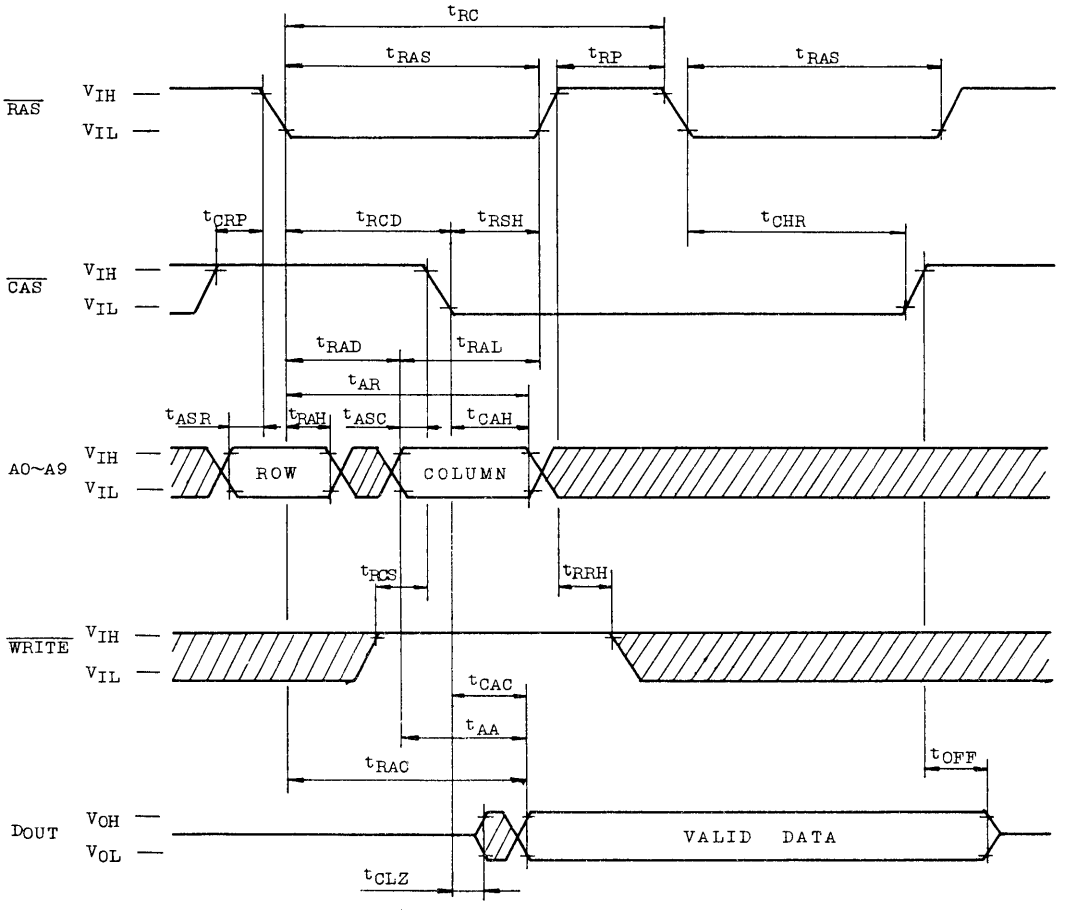
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



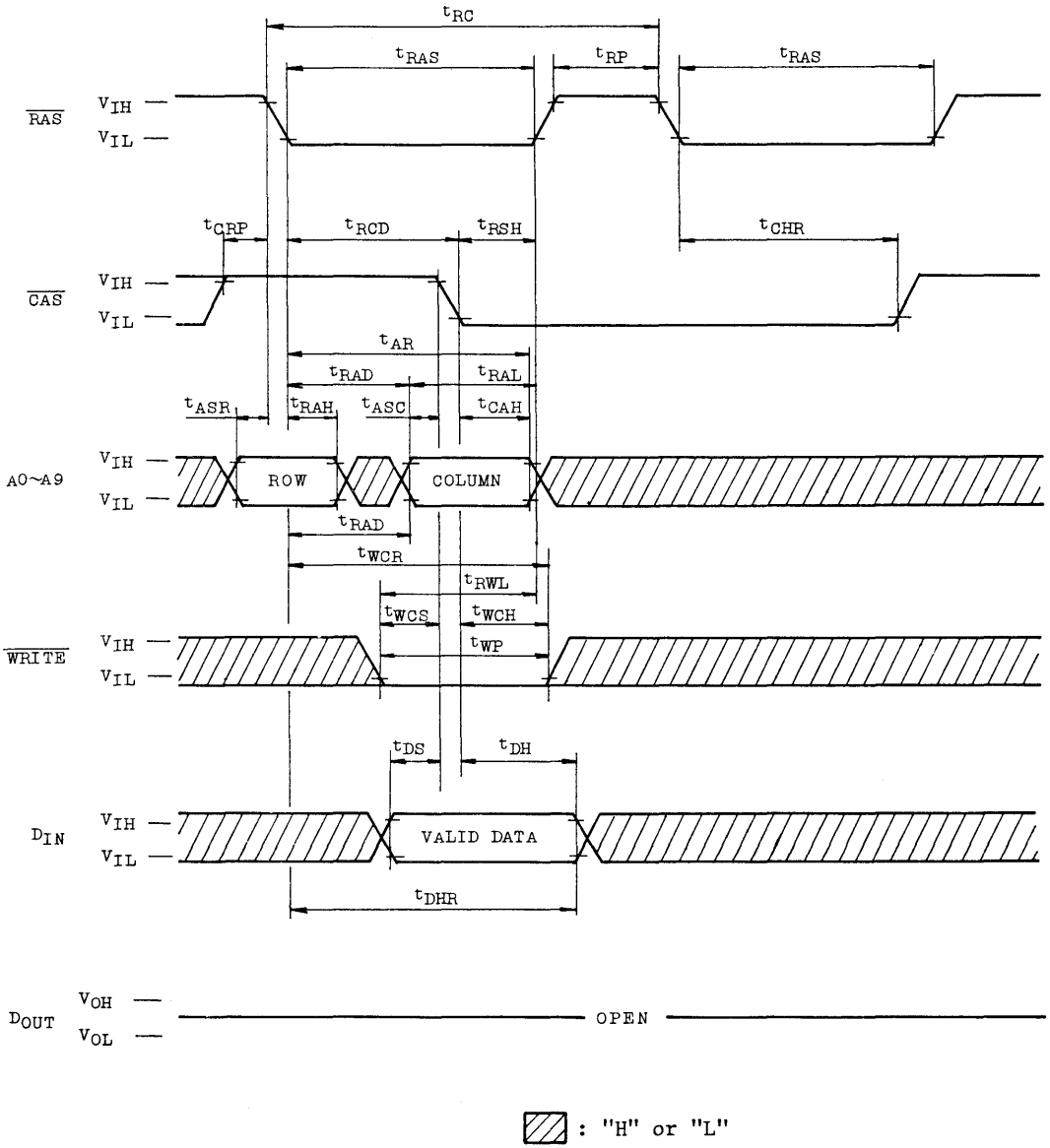
NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

HIDDEN REFRESH CYCLE (READ)



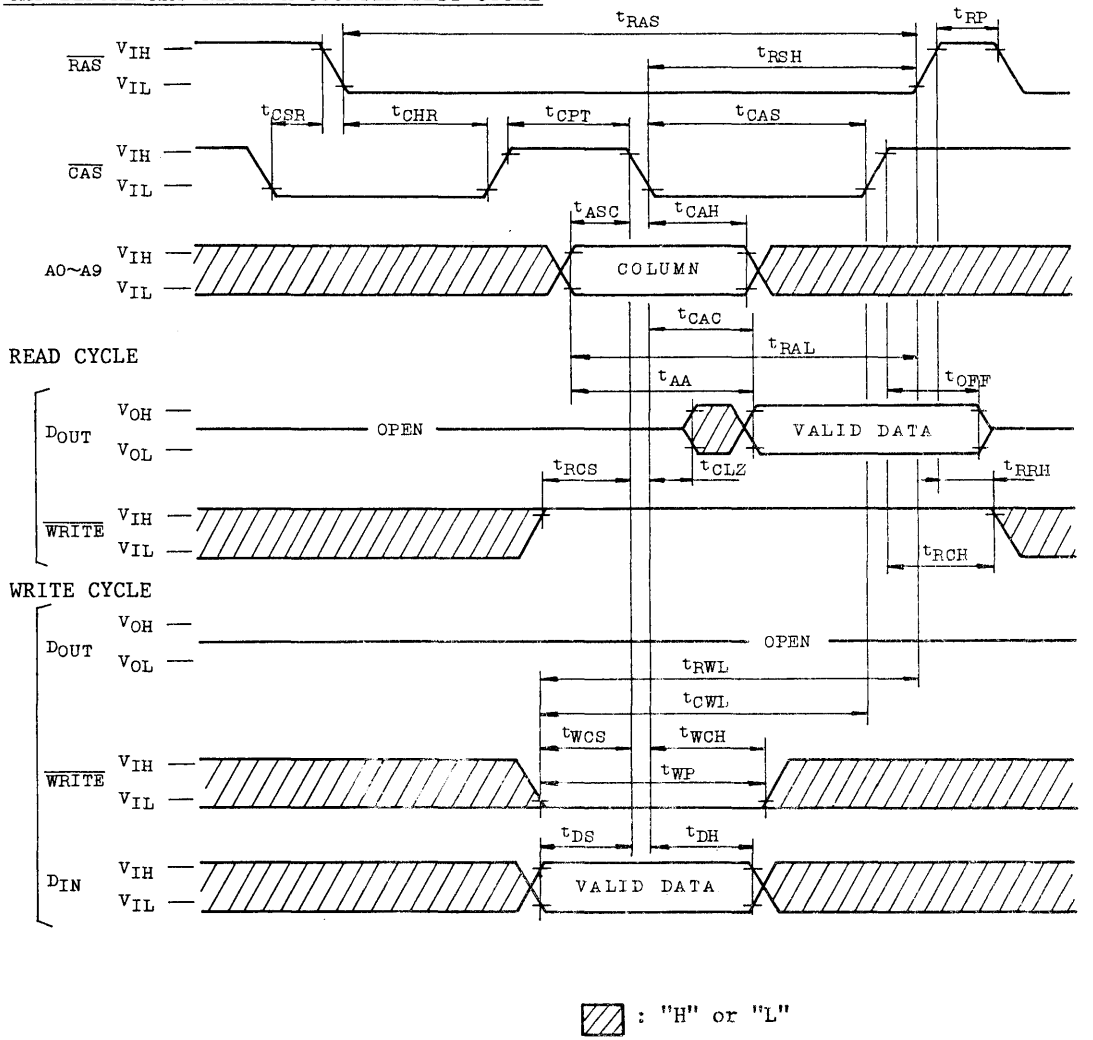
▨ : "H" or "L"

HIDDEN REFRESH CYCLE (WRITE)



▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

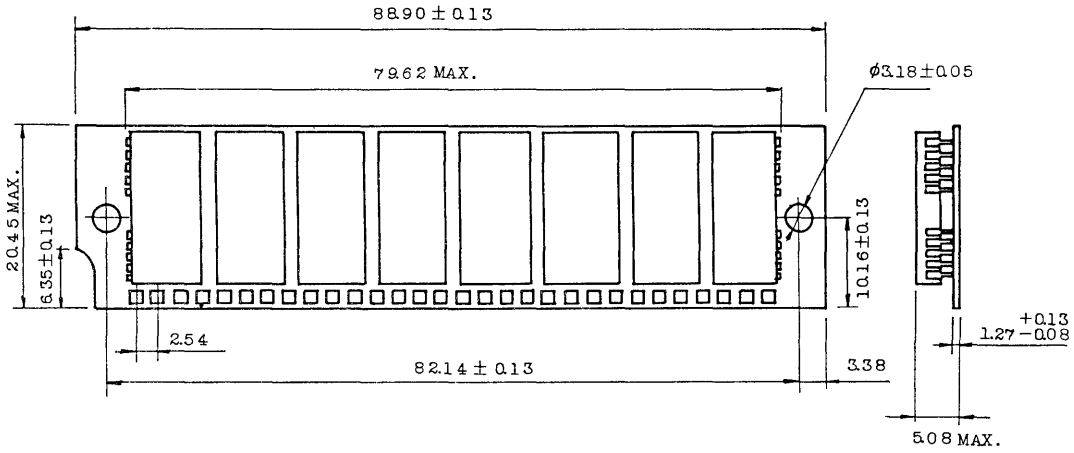


▨ : "H" or "L"

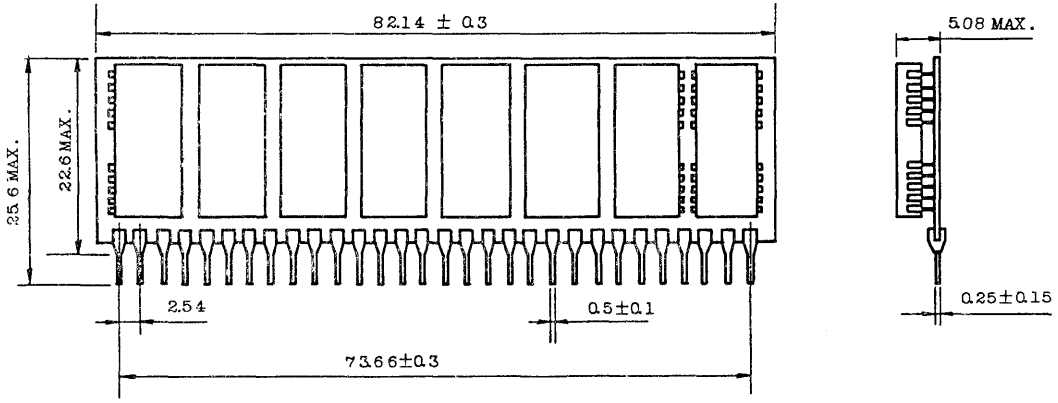
OUTLINE DRAWINGS

• THM91001S

Unit in mm



• THM91001L



THM91002S/L-85, 10, 12

DESCRIPTION

The THM91002S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511002J on the printed circuit board.

The THM91002S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

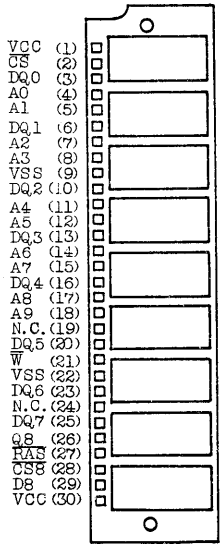
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91002S/L-85	THM91002S/L-10	THM91002S/L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10%
- Low power
  - 3,465mW MAX. Operating (THM91002S/L-85)
  - 2,970mW MAX. Operating (THM91002S/L-10)
  - 2,475mW MAX. Operating (THM91002S/L-12)
  - 49.5mW MAX. Standby
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

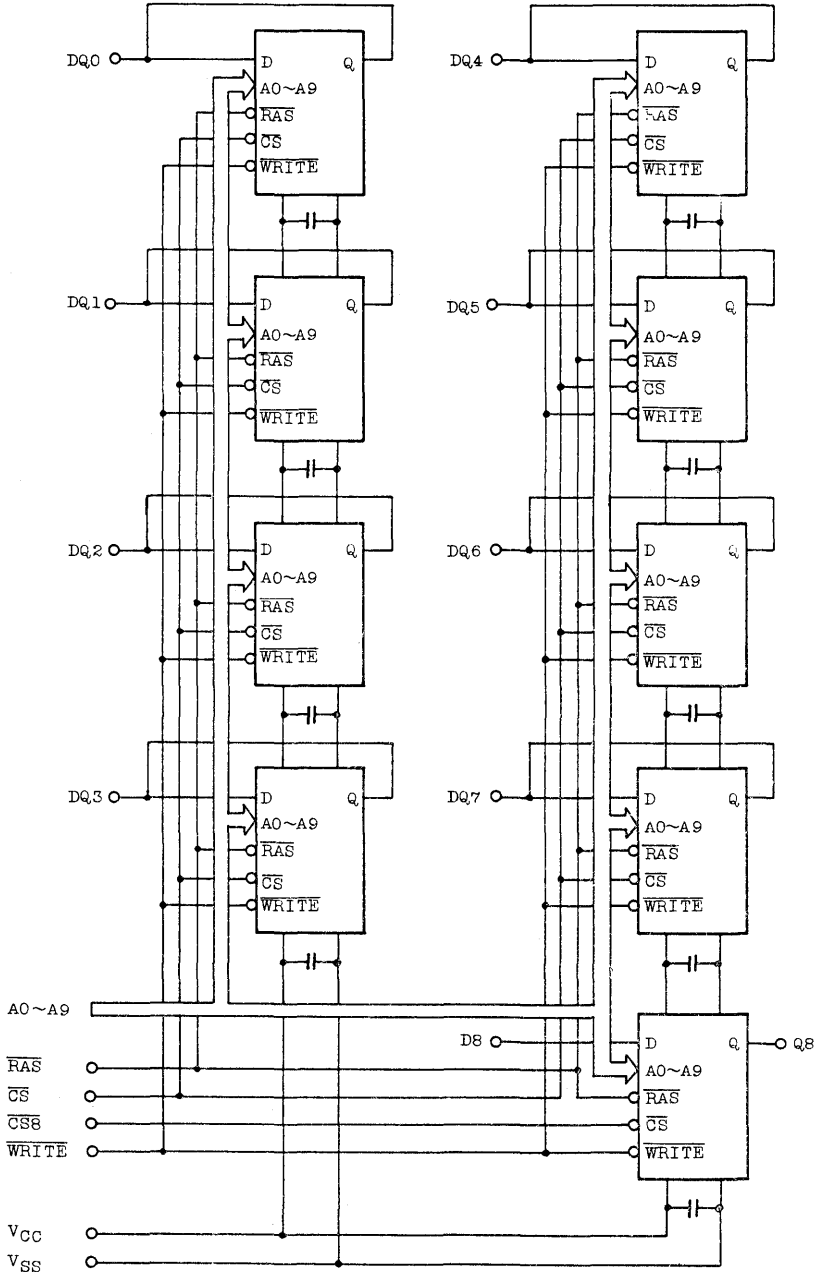
(TOP VIEW)



PIN NAMES

A0 ∿ 9	Address Inputs
DQ0 ∿ 7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CS8}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM91002S/L-85	-	630	mA	3, 4
		THM91002S/L-10	-	540		
		THM91002S/L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM91002S/L-85	-	630	mA	3
		THM91002S/L-10	-	540		
		THM91002S/L-12	-	450		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IH}, Address Cycling: t_{SC}=t_{SC} MIN.)	THM91002S/L-85	-	450	mA	3, 4
		THM91002S/L-10	-	360		
		THM91002S/L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM91002S/L-85	-	630	mA	3
		THM91002S/L-10	-	540		
		THM91002S/L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91002S/L-85		THM91002S/L-10		THM91002S/L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91002S/L-85		THM91002S/L-10		THM91002S/L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∼70°C)

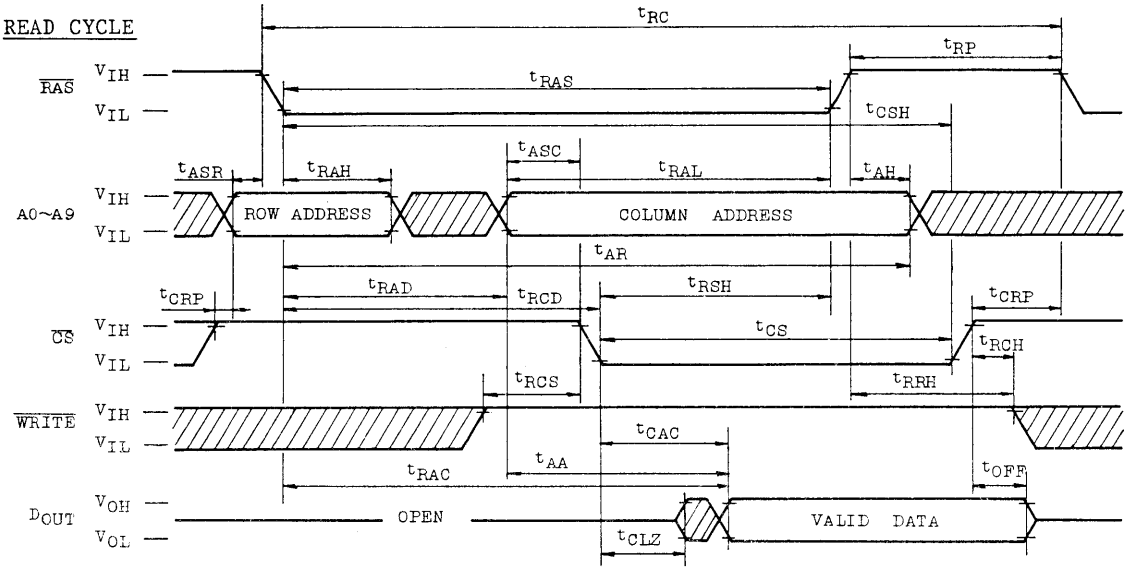
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∼A9, $\overline{W}$, $\overline{CS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0∼DQ7)	-	15	pF
C_{Q}	Output Capacitance (Q8)	-	10	pF

NOTES:

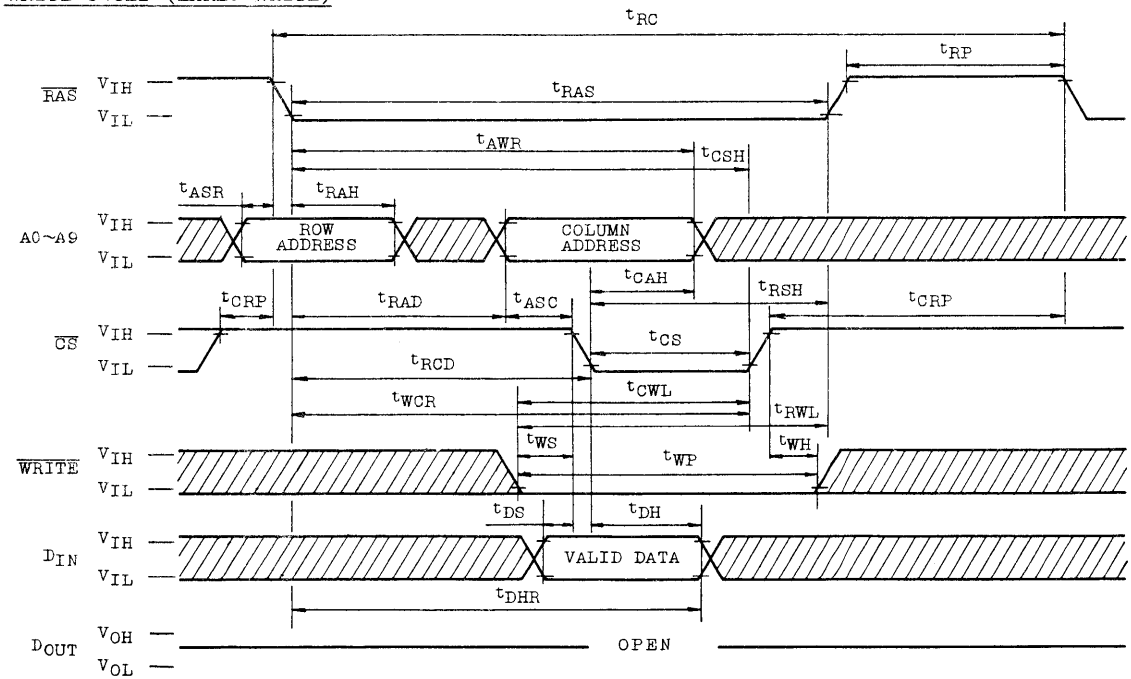
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of useing internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge.
12. t_{WS}, t_{WH} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geqq t_{WS}$(min.) and $t_{WH} \geqq t_{WH}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. t_{AH} is the condition to latch column address when $\overline{RAS}$ has rised up.

TIMING WAVEFORMS

READ CYCLE

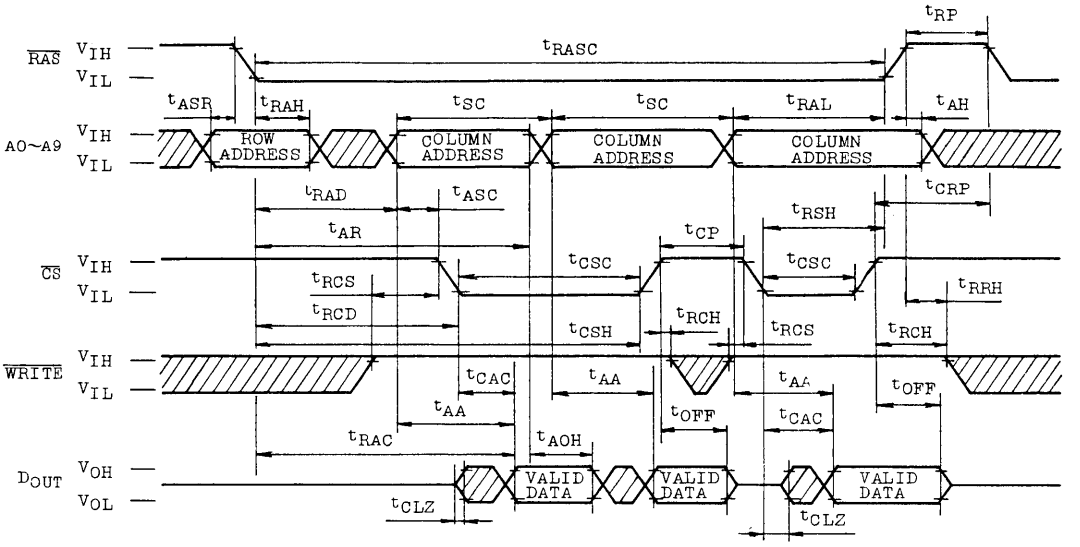


WRITE CYCLE (EARLY WRITE)

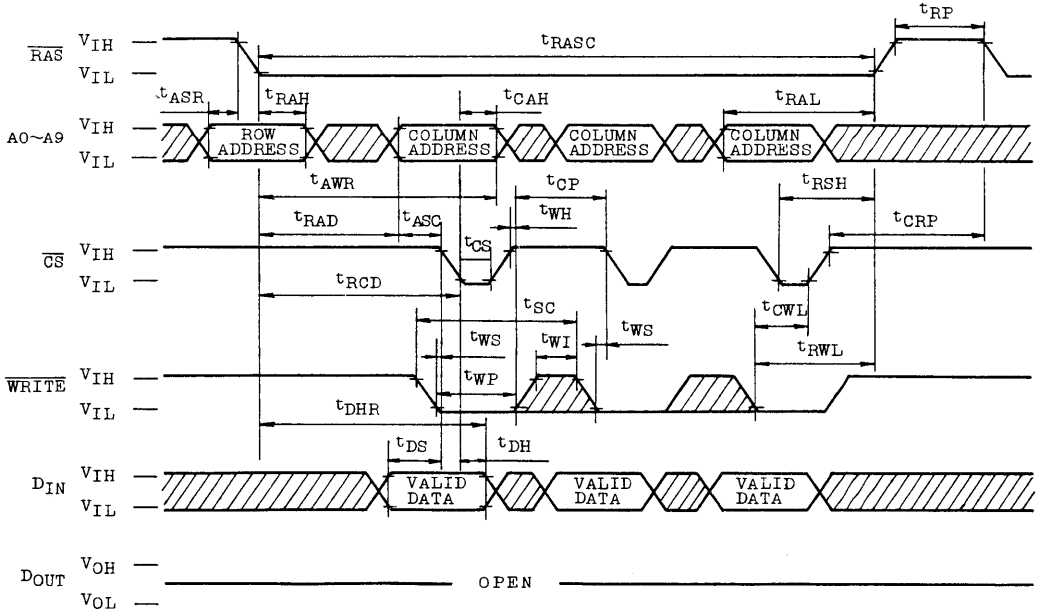


▨ : "H" or "L"

STATIC COLUMN MODE READ CYCLE

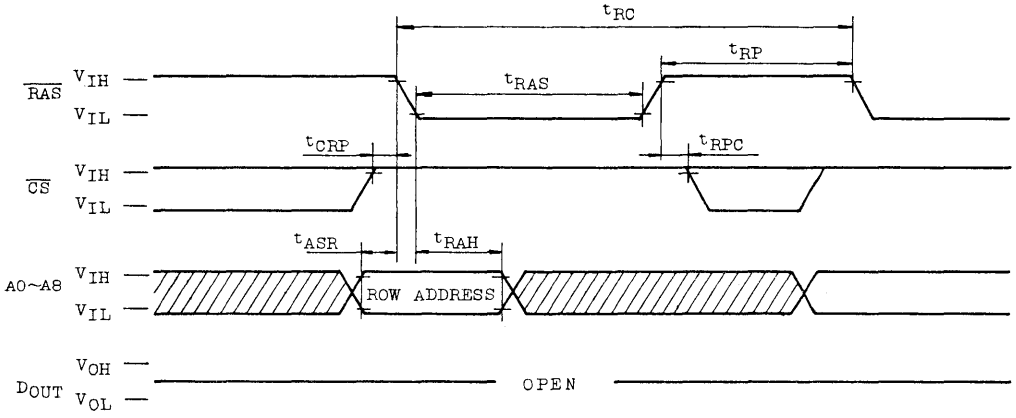


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



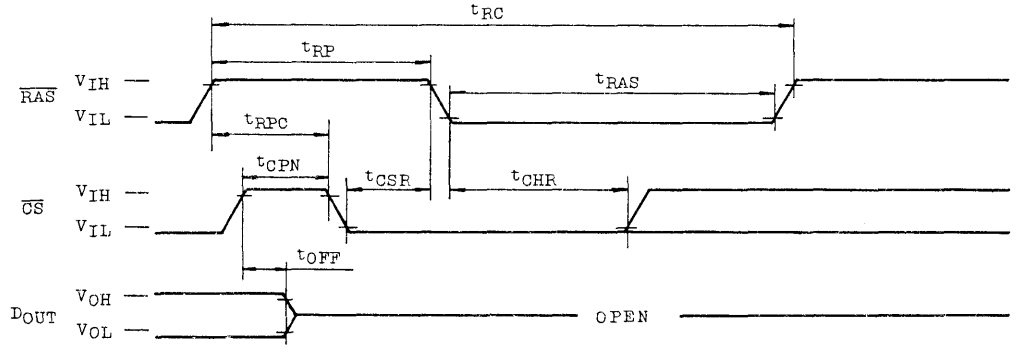
: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



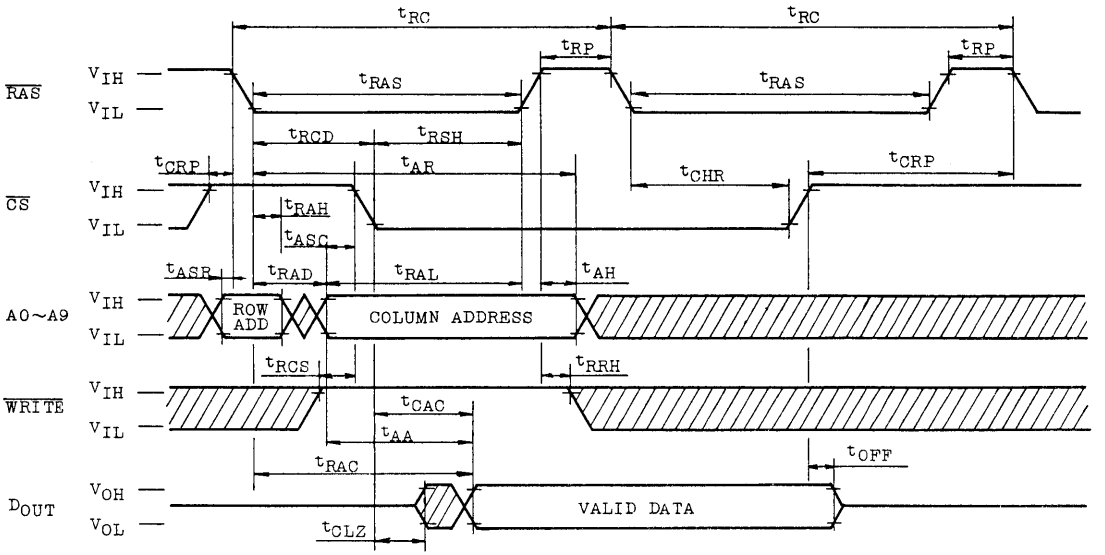
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨ : "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

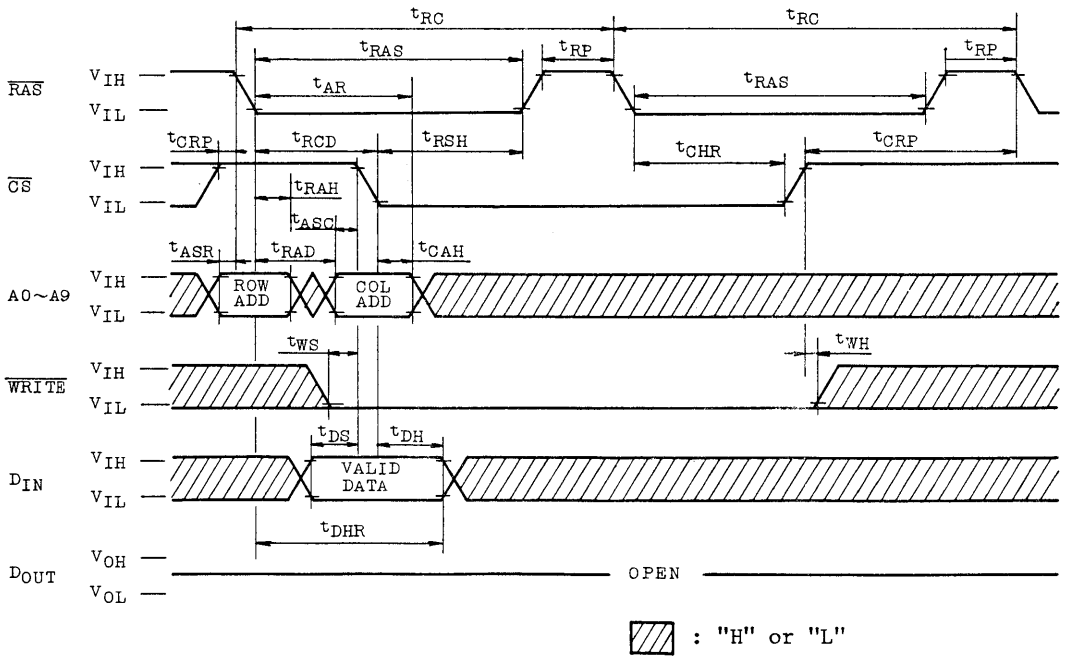


NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

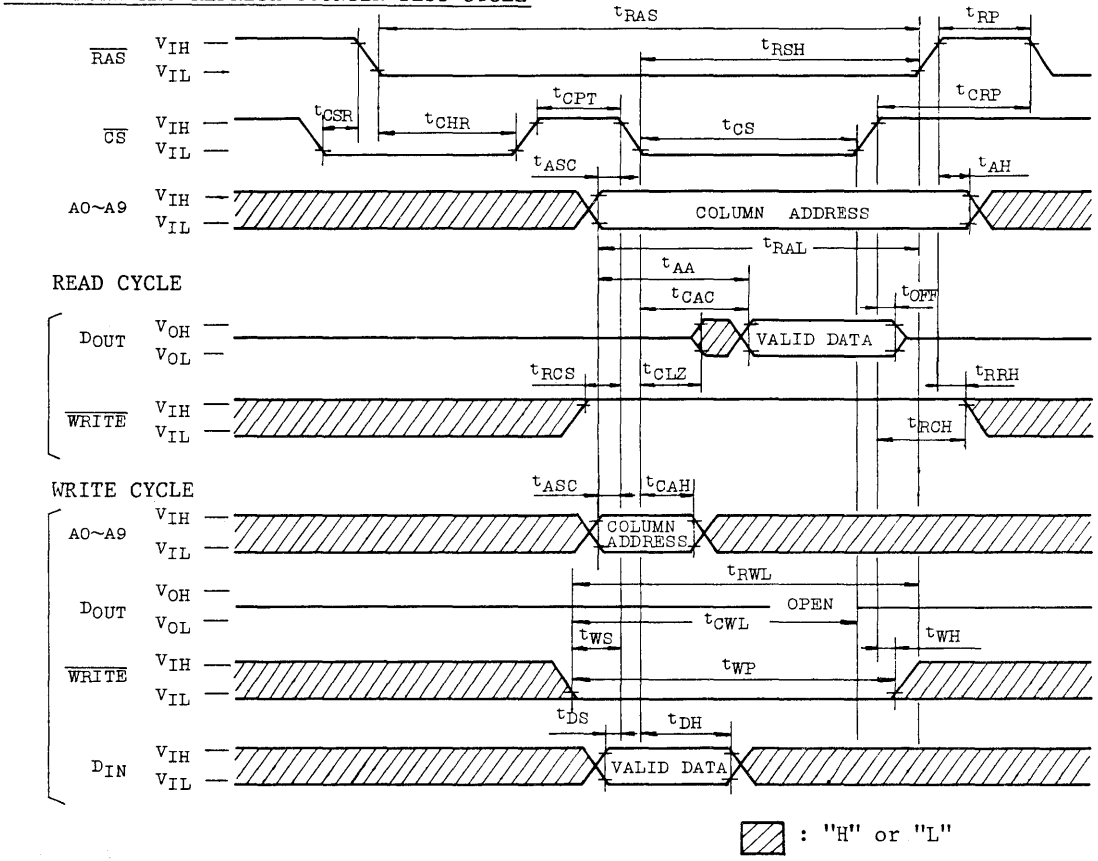
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



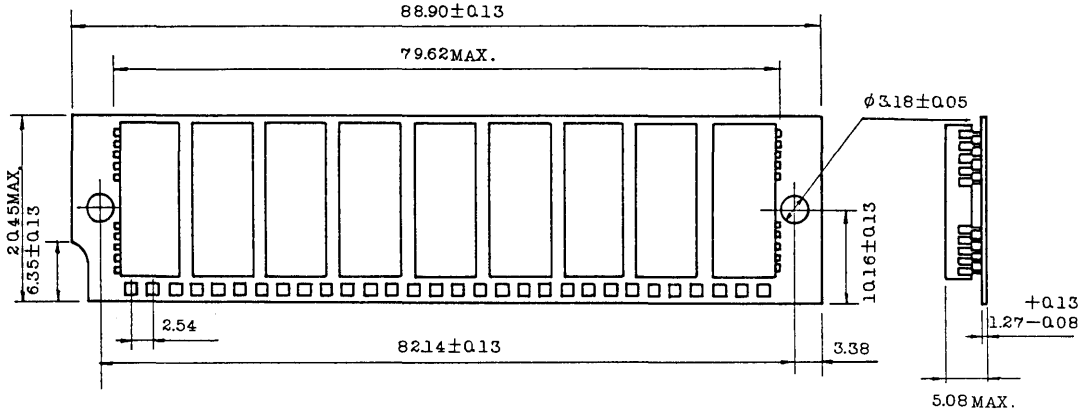
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



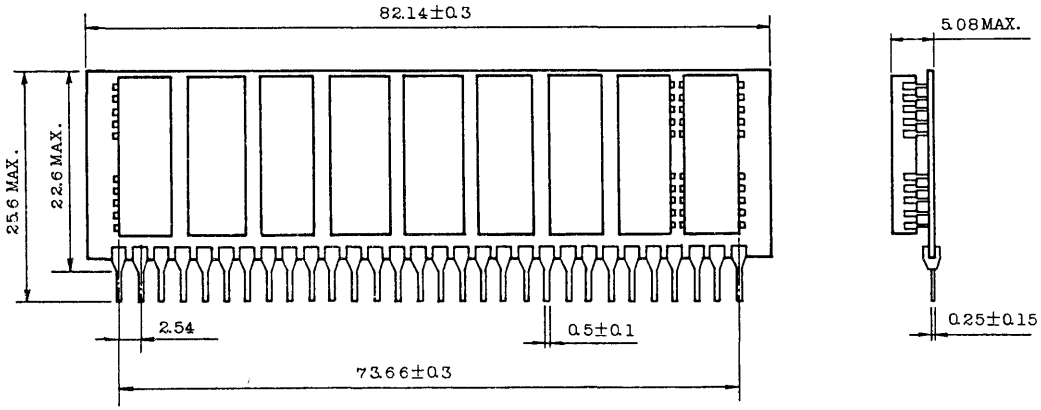
OUTLINE DRAWINGS

THM91002S

Unit in mm



• THM91002L



THM91010S-85, 10, 12

DESCRIPTION

The THM91010S is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000J on the printed circuit board.

The THM91010S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

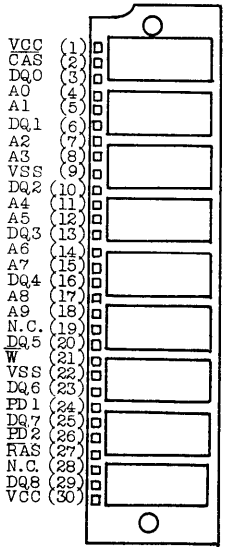
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91010S-85	THM91010S-10	THM91010S-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	25ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Single power supply of 5V±10%
- Low power 3,465mW MAX. Operating (THM91010S-85)
  2,970mW MAX. Operating (THM91010S-10)
  2,475mW MAX. Operating (THM91010S-12)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and ouptuts TTL compatible
- 512 refresh cycles/8ms

PIN CONNECTION

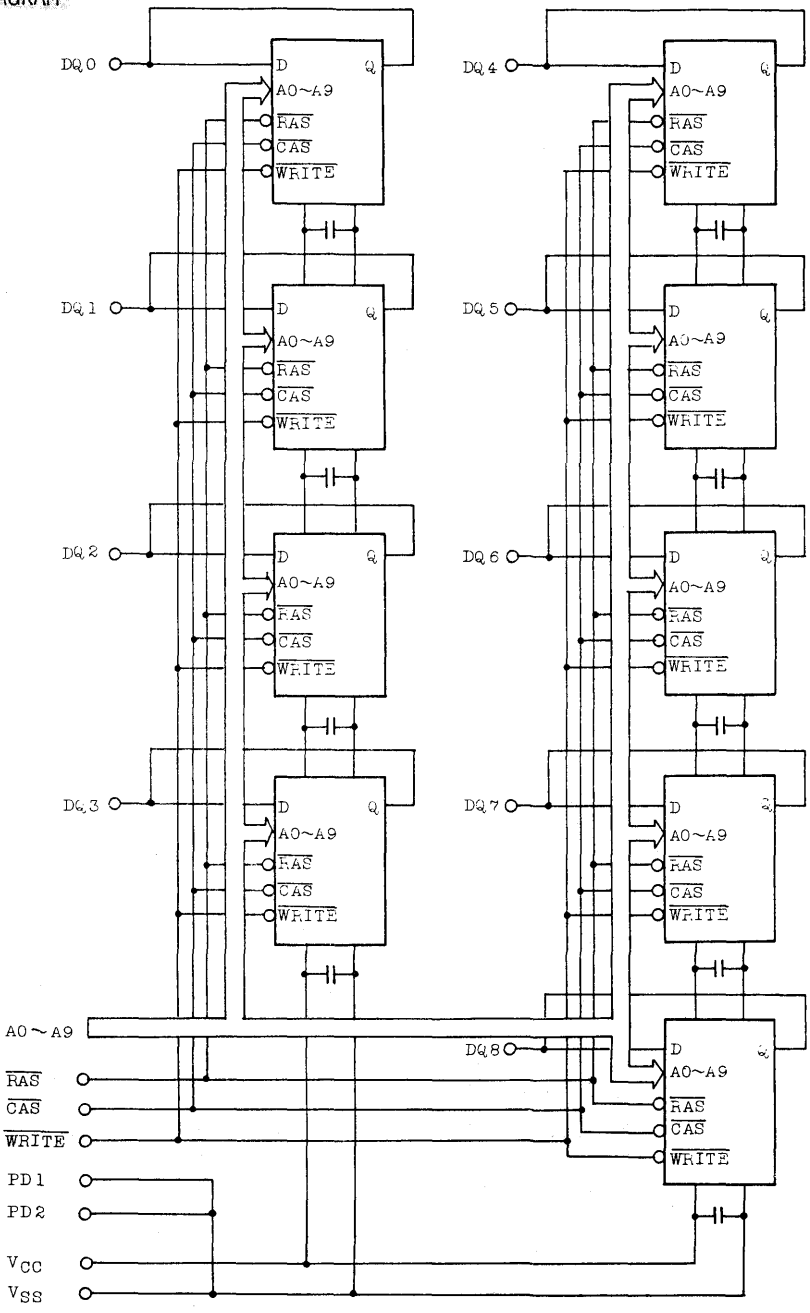
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ8	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
PD1, 2	Presence Detect (Ground)
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS ($Ta=0 \sim 70°C$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4		6.5	V	2
V_{IL}	Input Low Voltage	-1.0		0.8	V	2

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V\pm10\%$, $Ta=0 \sim 70°C$)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91010S-85	-	630	mA	3, 4
		THM91010S-10	-	540		
		THM91010S-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{IH}$)		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}=V_{IH}$: $t_{RC}=t_{RC}$ MIN.)	THM91010S-85	-	630	mA	3
		THM91010S-10	-	540		
		THM91010S-12	-	450		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}=V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC}=t_{PC}$ MIN.)	THM91010S-85	-	450	mA	3, 4
		THM91010S-10	-	360		
		THM91010S-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC}=t_{RC}$ MIN.)	THM91010S-85	-	630	mA	3
		THM91010S-10	-	540		
		THM91010S-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT}=-5mA$)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT}=4.2mA$)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91010S-85		THM91010S-10		THM91010S-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91010S-85		THM91010S-10		THM91010S-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ8)	-	15	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

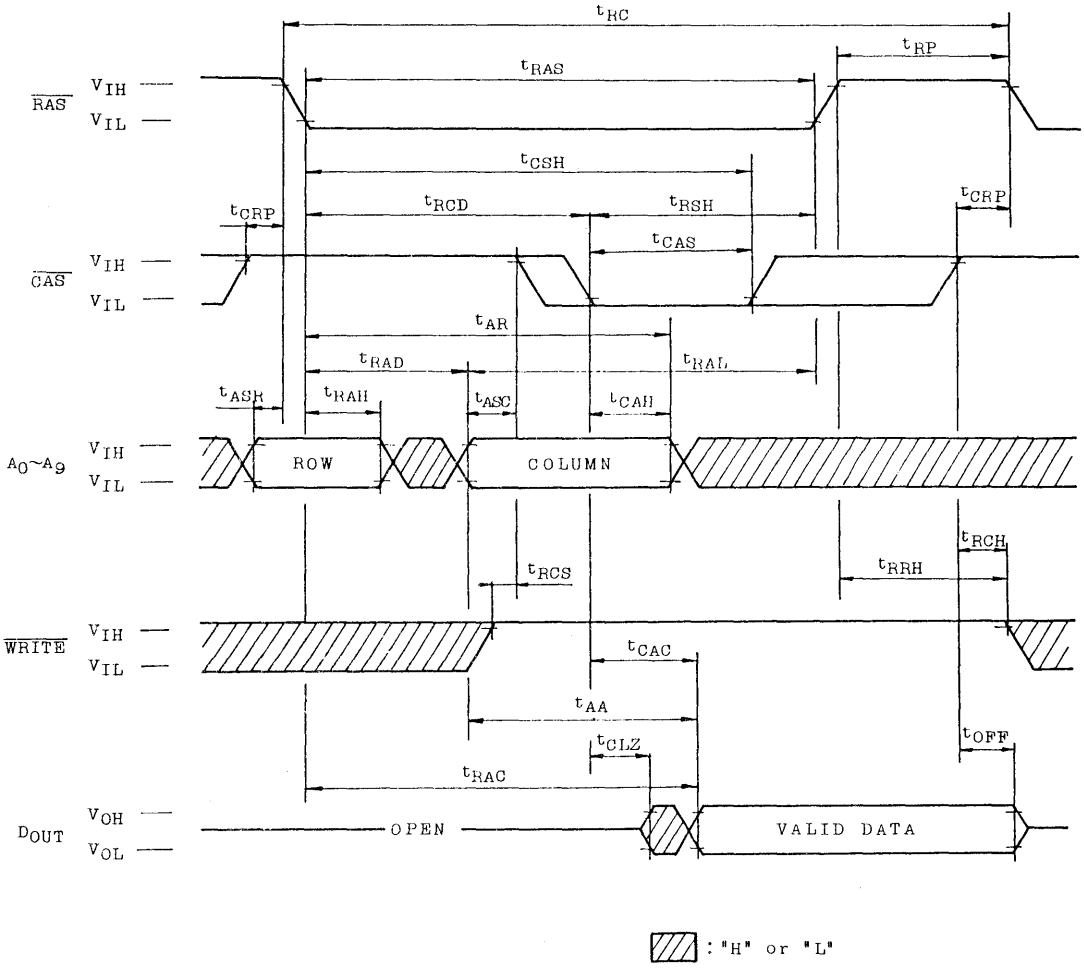
11. These parameters are referenced to $\overline{CAS}$ leading edge.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

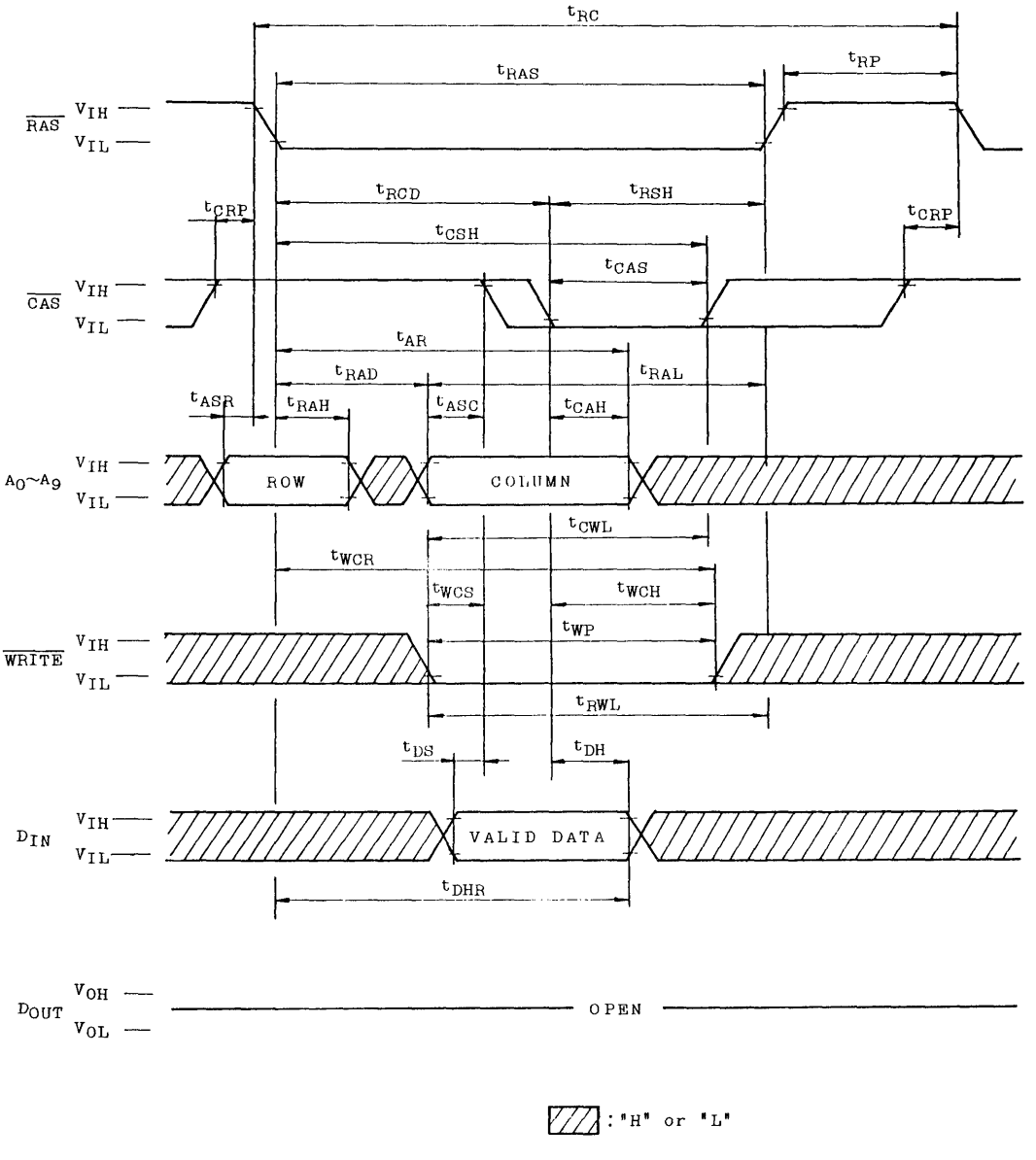
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

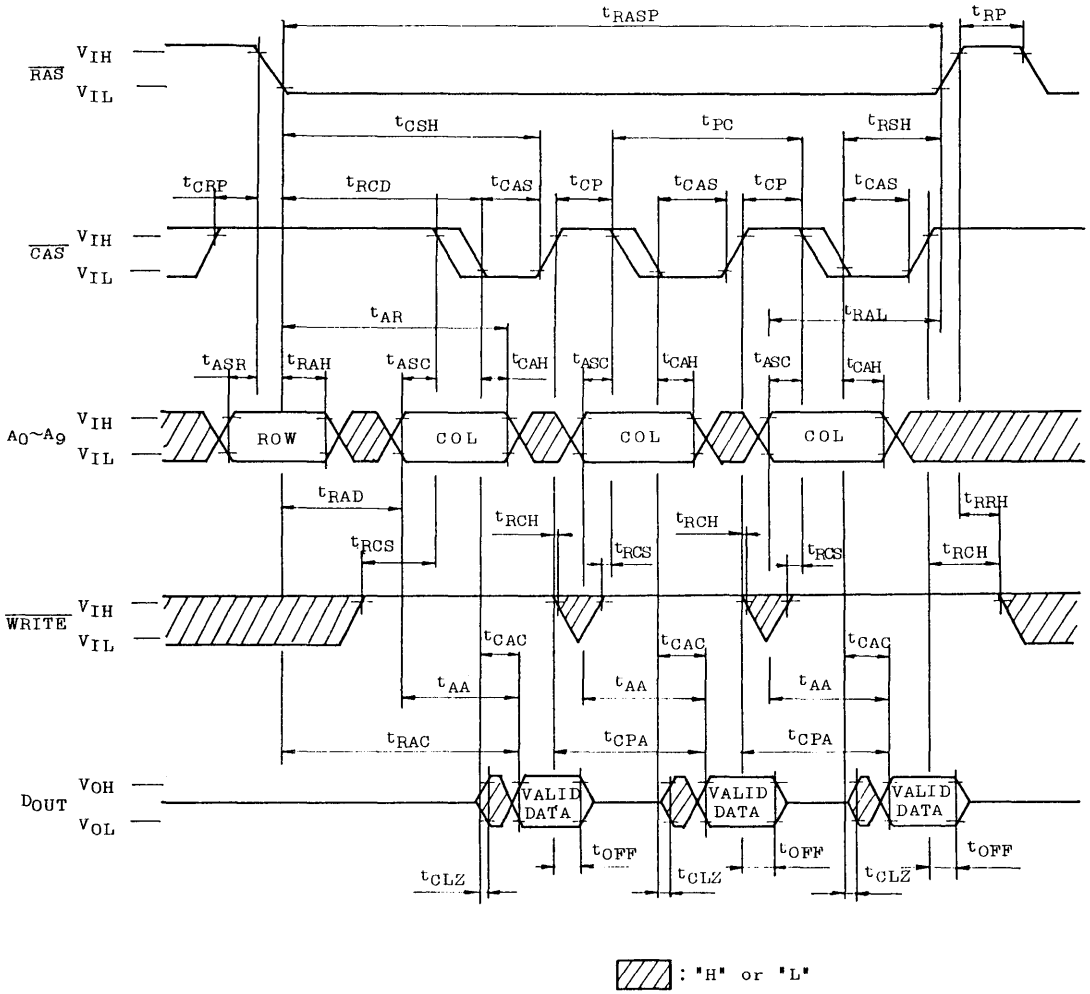
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H" or "L"

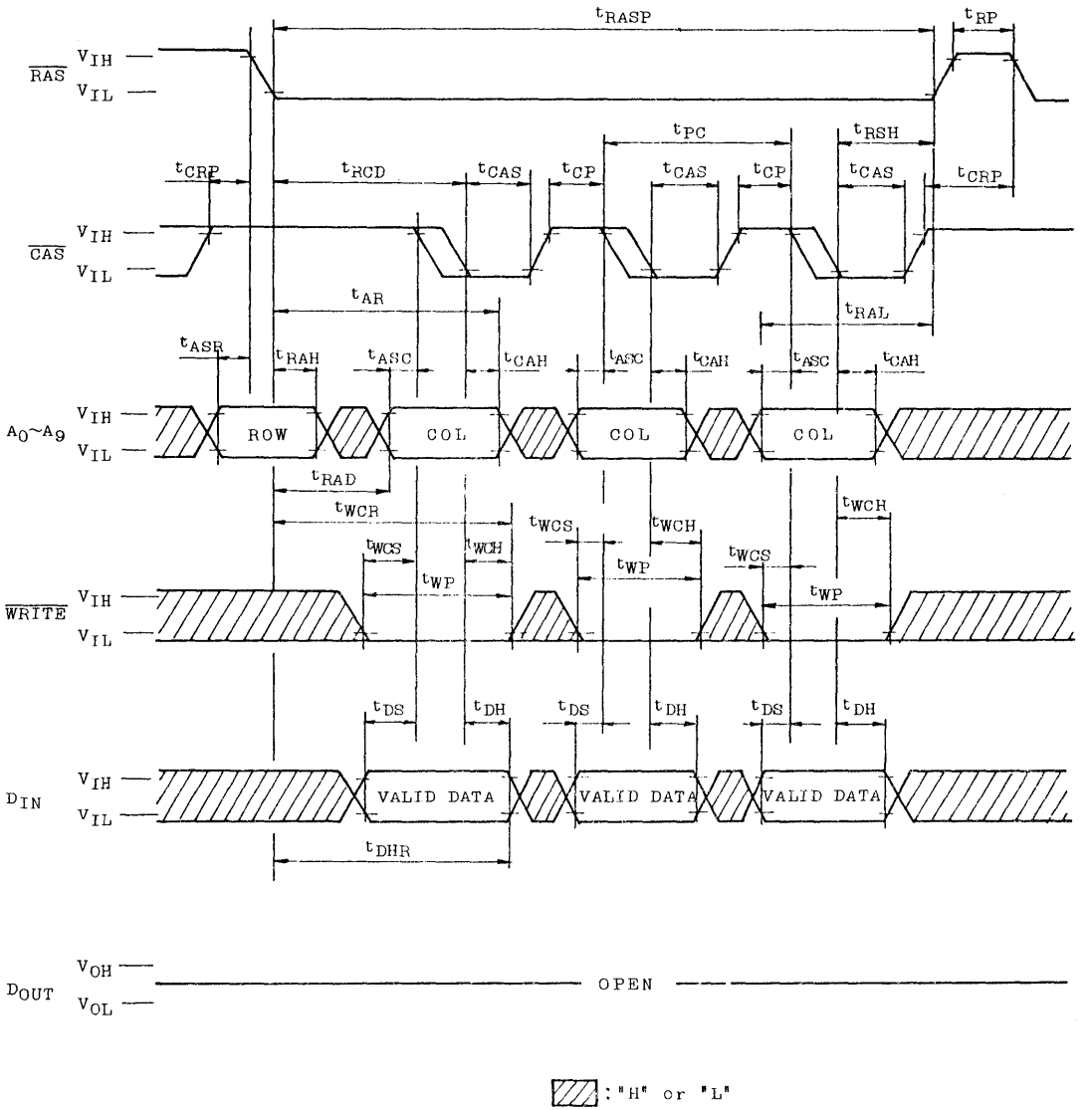
EARLY WRITE CYCLE



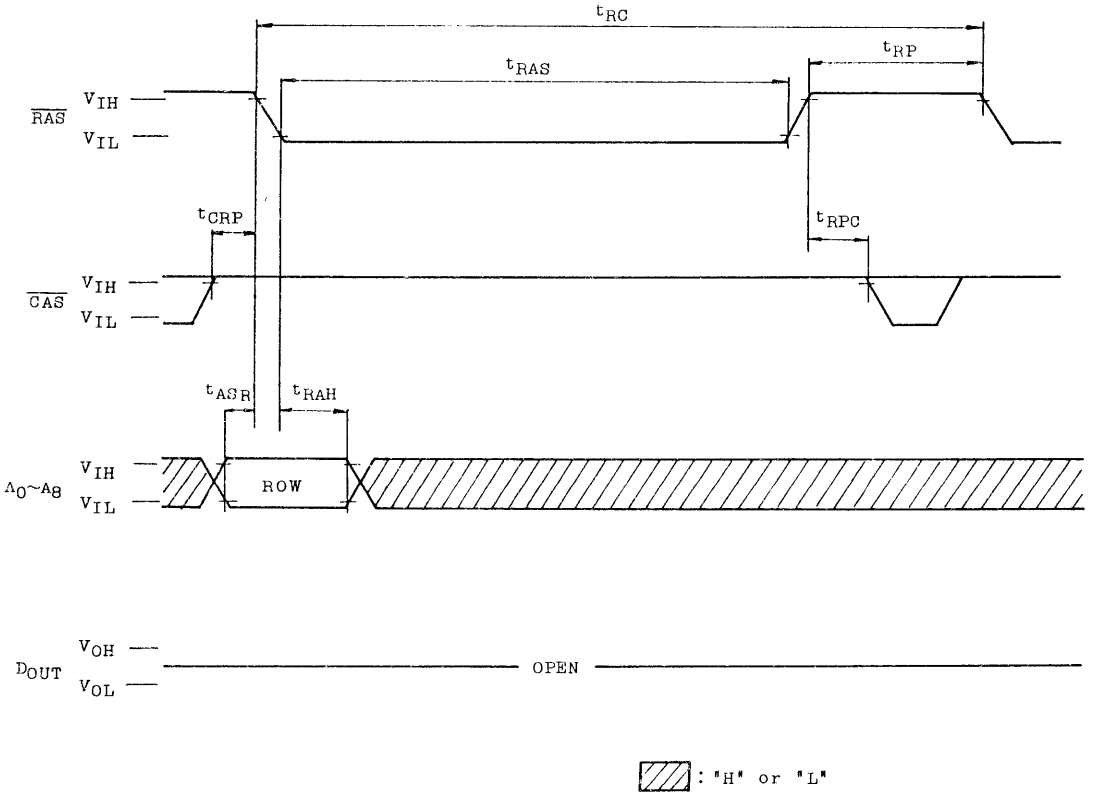
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

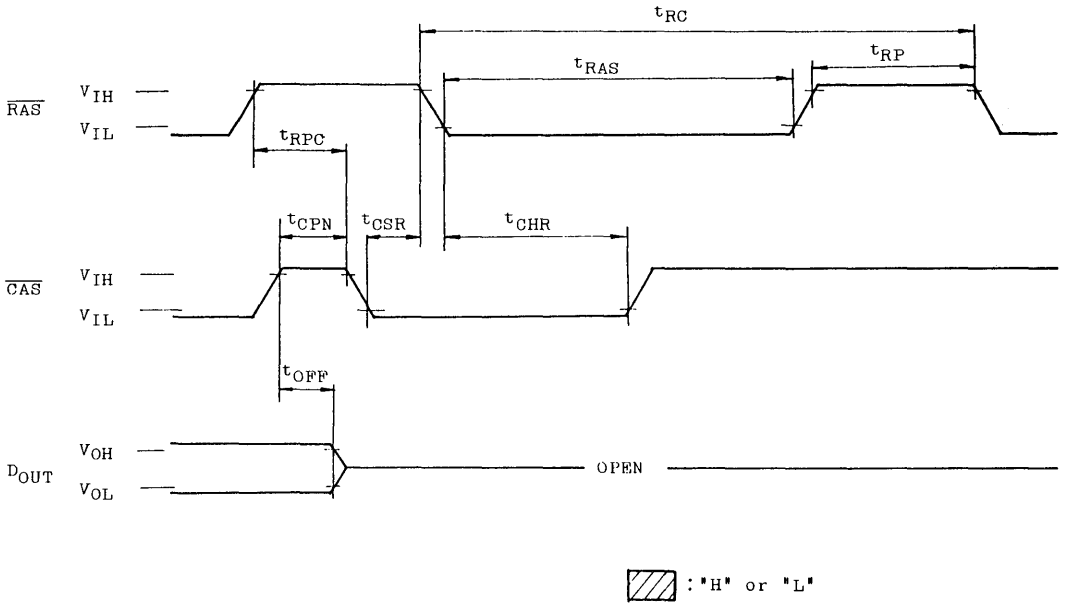


$\overline{RAS}$ ONLY REFRESH CYCLE



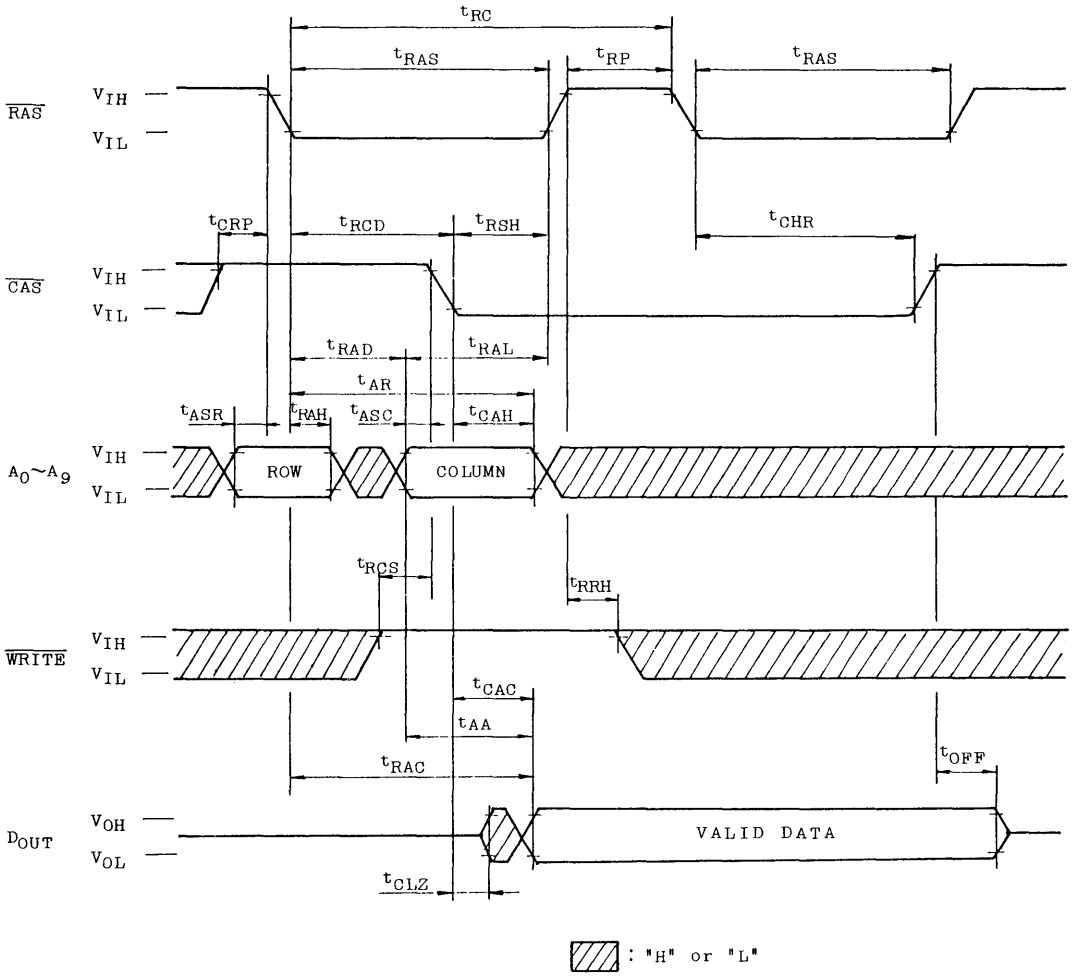
Note: $\overline{WRITE}$="H" or "L" , A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

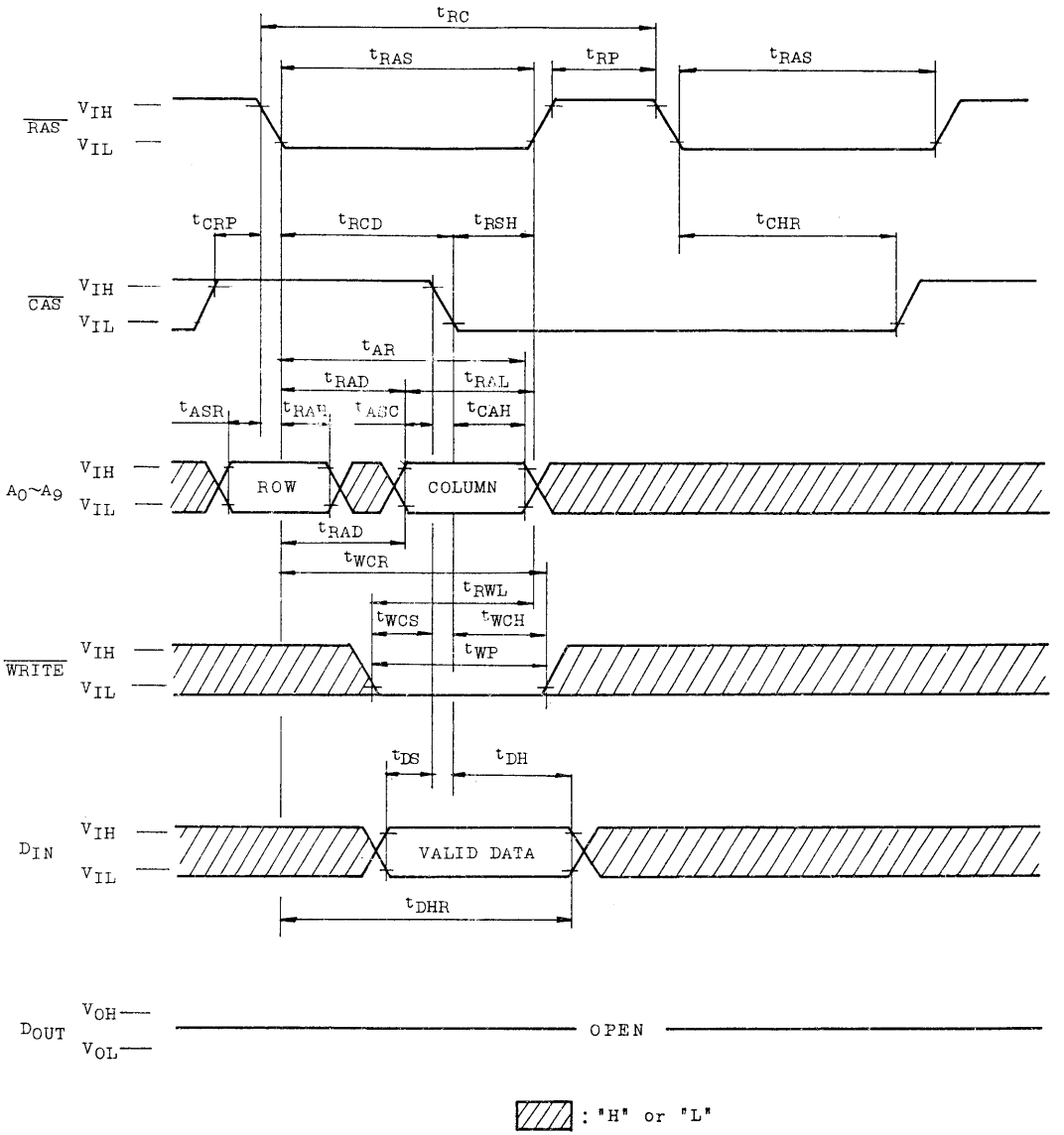


Note: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

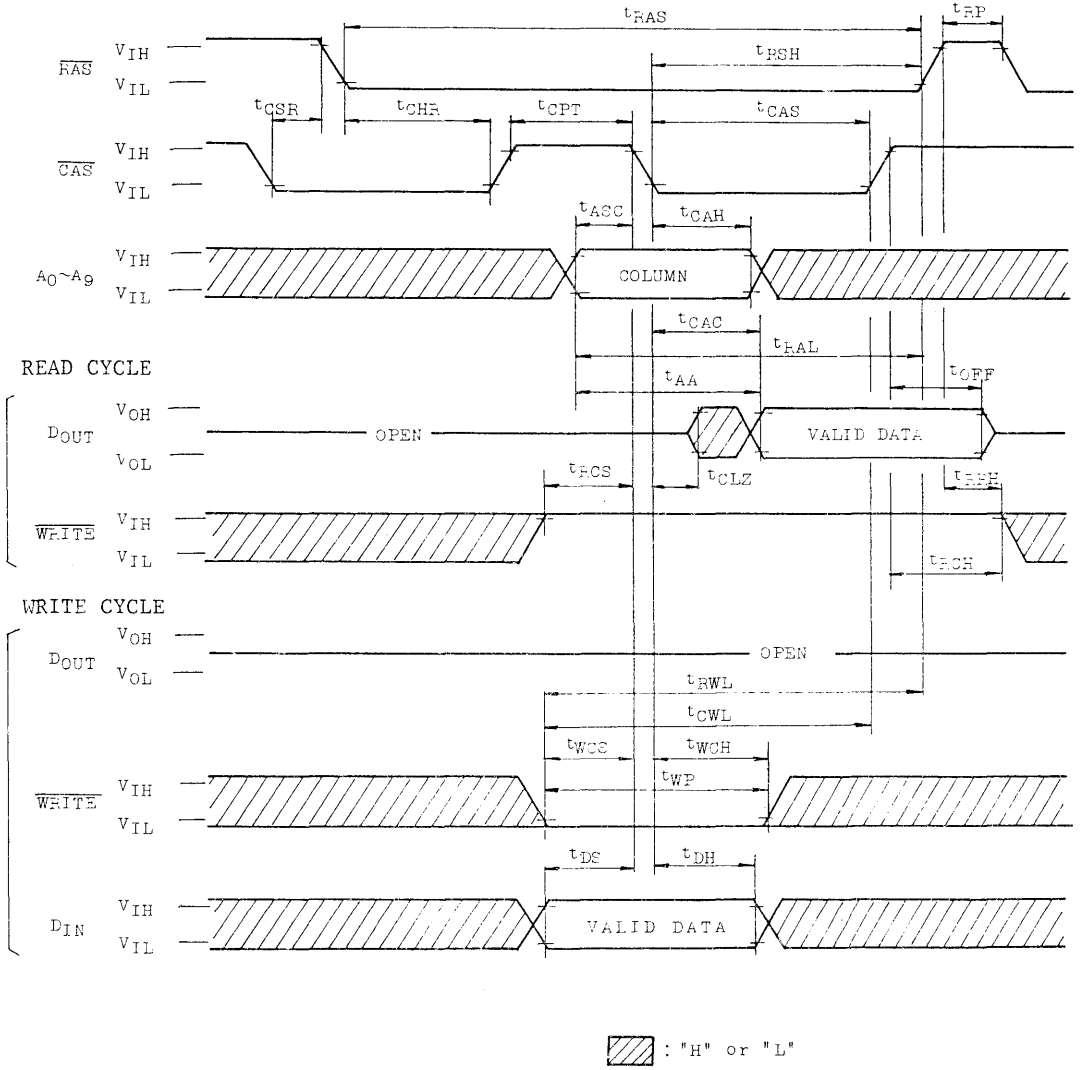
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



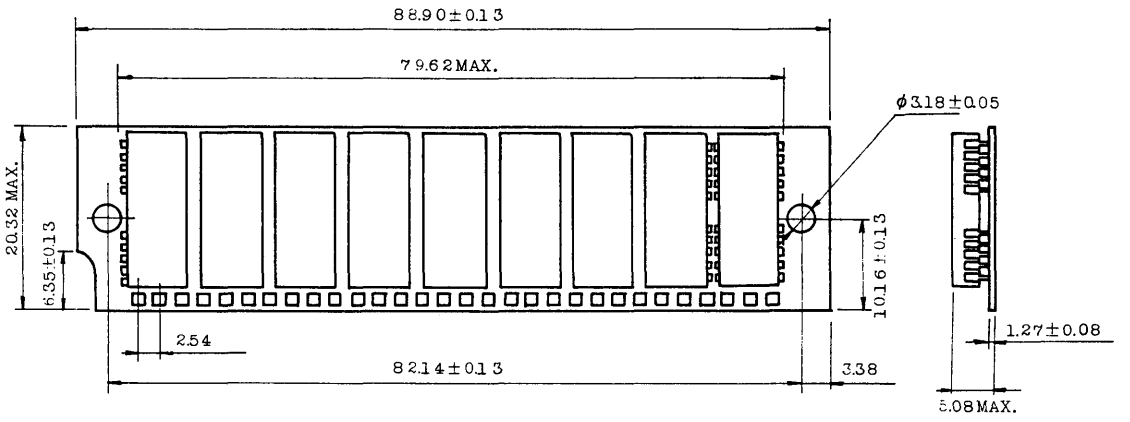
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



▨ : "H" or "L"

OUTLINE DRAWINGS

Unit in mm



THM91020L-85, 10, 12

DESCRIPTION

The THM91020L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000J on both sides of the printed circuit board.

The THM91020L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

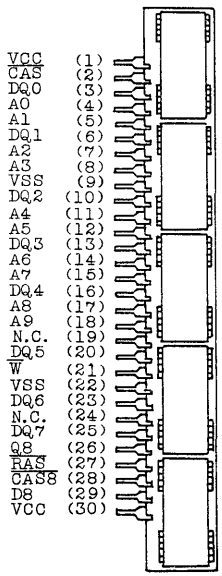
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91020L-85	THM91020L-10	THM91020L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{PC}	Fast Page Mode Cycle Time	50ns	55ns	70ns

- Sinlge power supply of 5V±10%
- Low power
  - 3,465mW MAX. Operating(THM91020L-85)
  - 2,970mW MAX. Operating(THM91020L-10)
  - 2,475mW MAX. Operating(THM91020L 12)
  - 49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Package Height

PIN CONNECTION

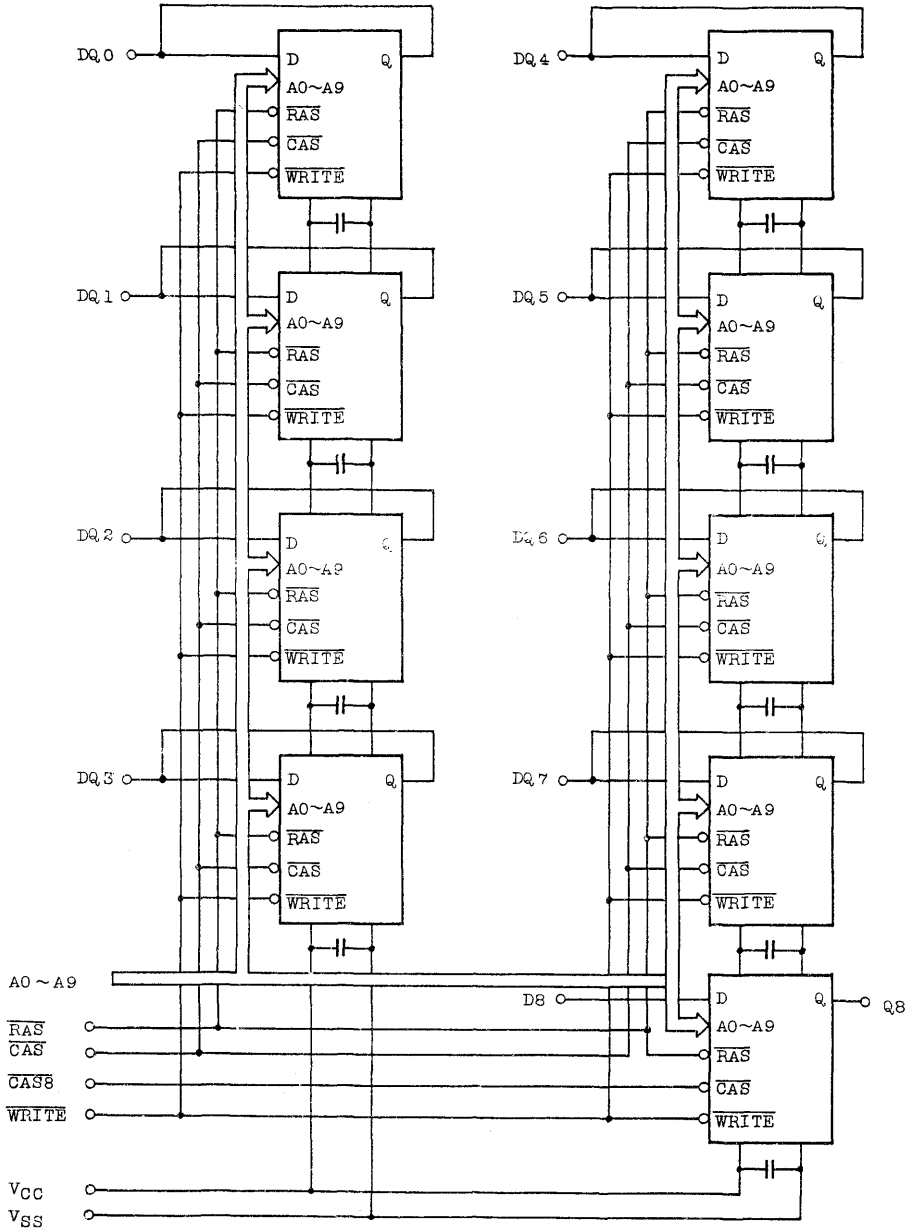
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM91020L-85	-	630	mA	3,4
		THM91020L-10	-	540		
		THM91020L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})				mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM91020L-85	-	630	mA	3
		THM91020L-10	-	540		
		THM91020L-12	-	450		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM91020L-85	-	450	mA	3,4
		THM91020L-10	-	360		
		THM91020L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM91020L-85	-	630	mA	3
		THM91020L-10	-	540		
		THM91020L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0 ∿ 70°C) (Notes 5, 6, 7)

SYSTEM	PARAMETER	THM91020L-85		THM91020L-10		THM91020L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{PC}	Fast Page Mode Cycle Time	50	-	55	-	70	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	45	-	50	-	65	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91020L-85		THM91020L-10		THM91020L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

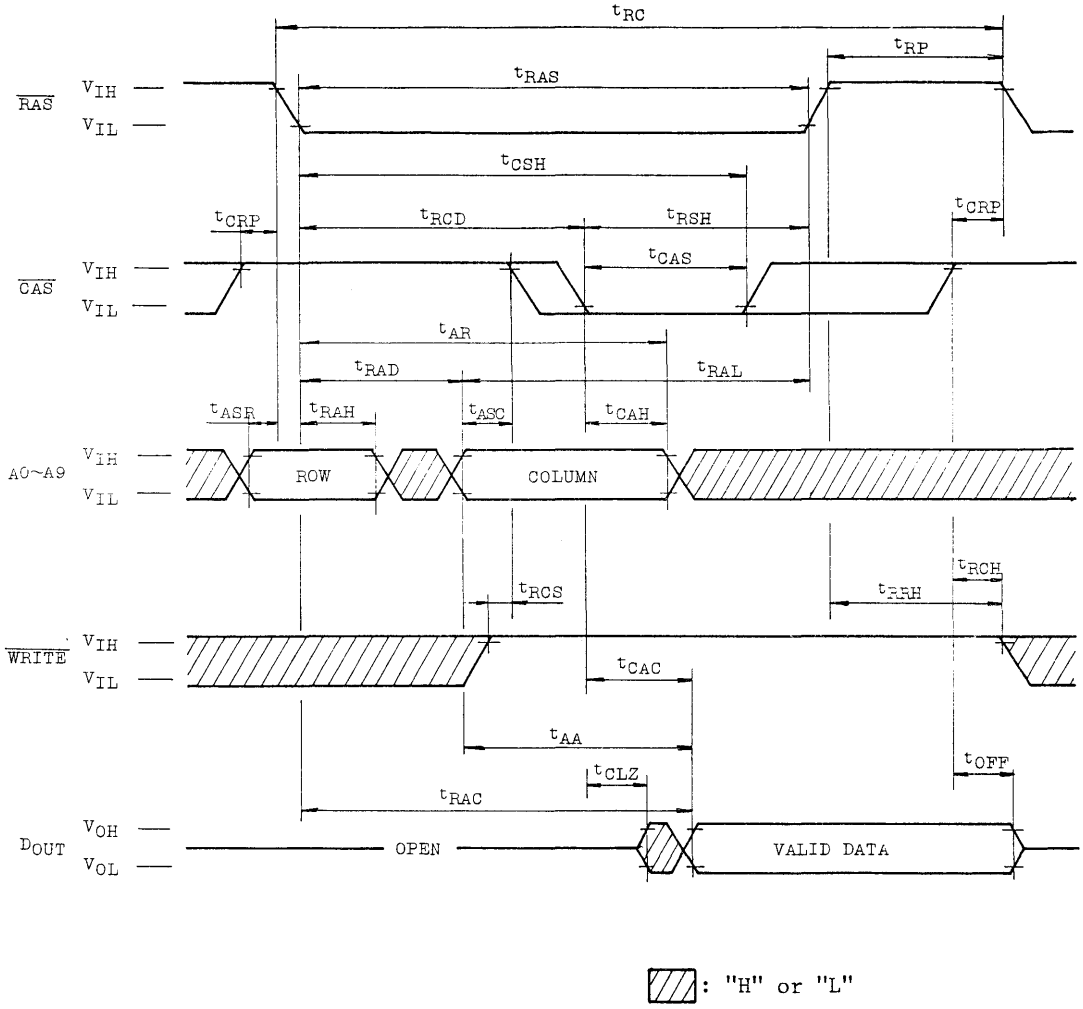
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ∿ A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0 ∿ DQ7)	-	15	pF
C_Q	Output Capacitance (Q8)	-	10	pF

NOTES:

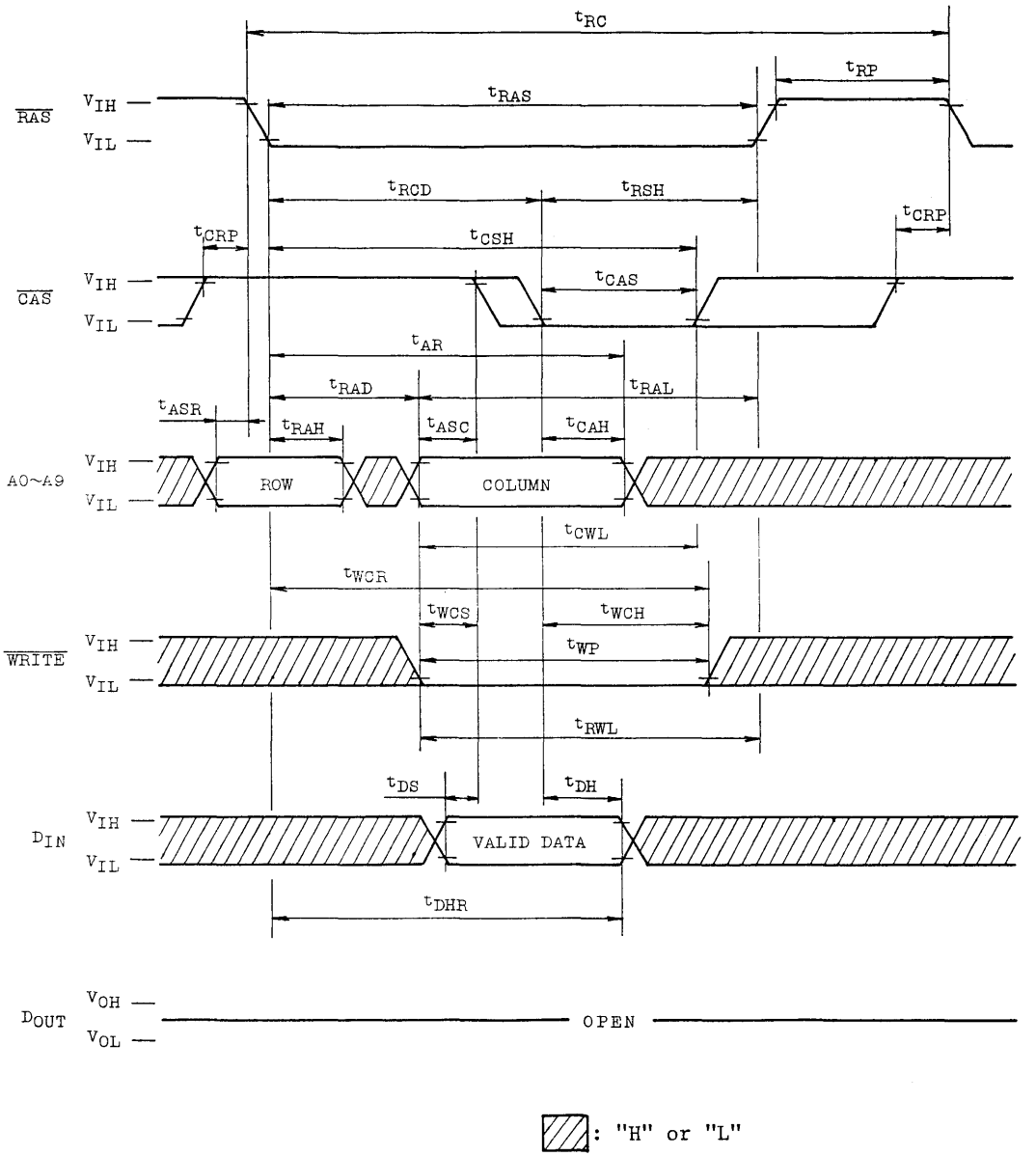
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



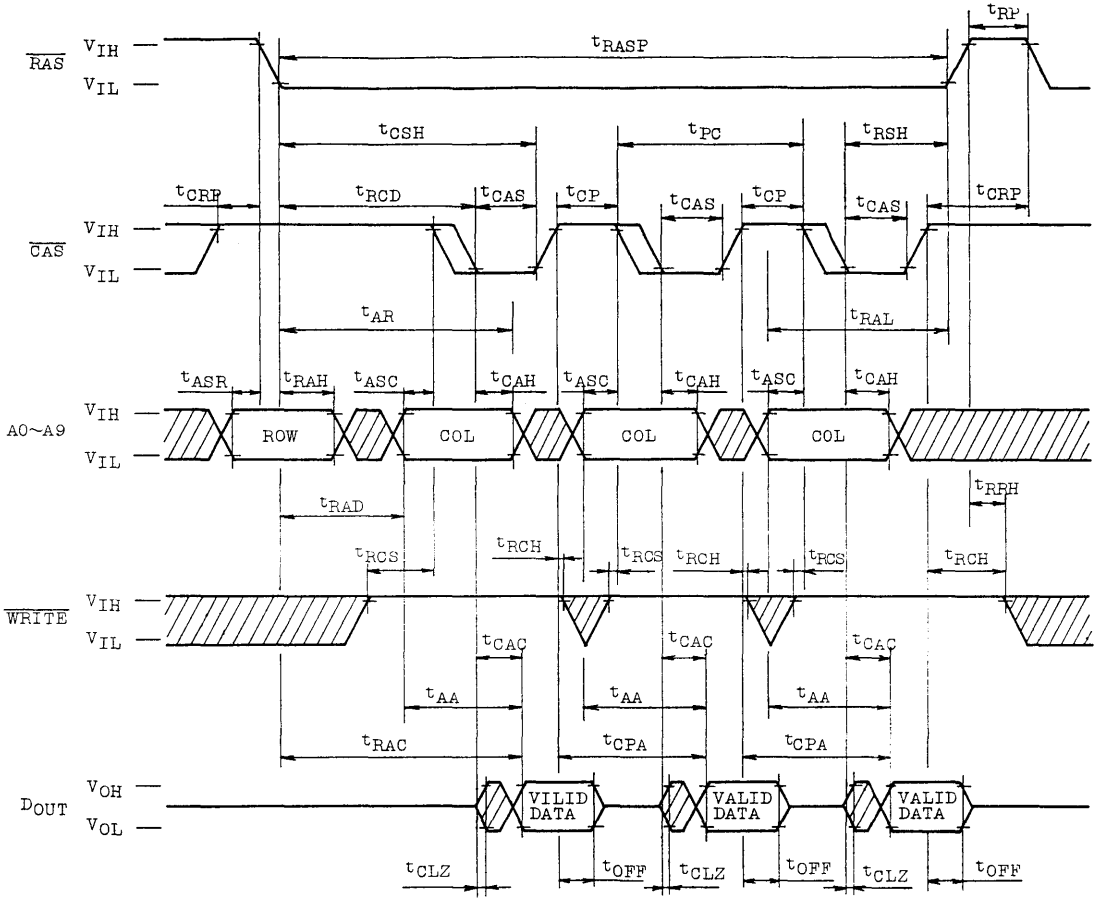
: "H" or "L"

EARLY WRITE CYCLE

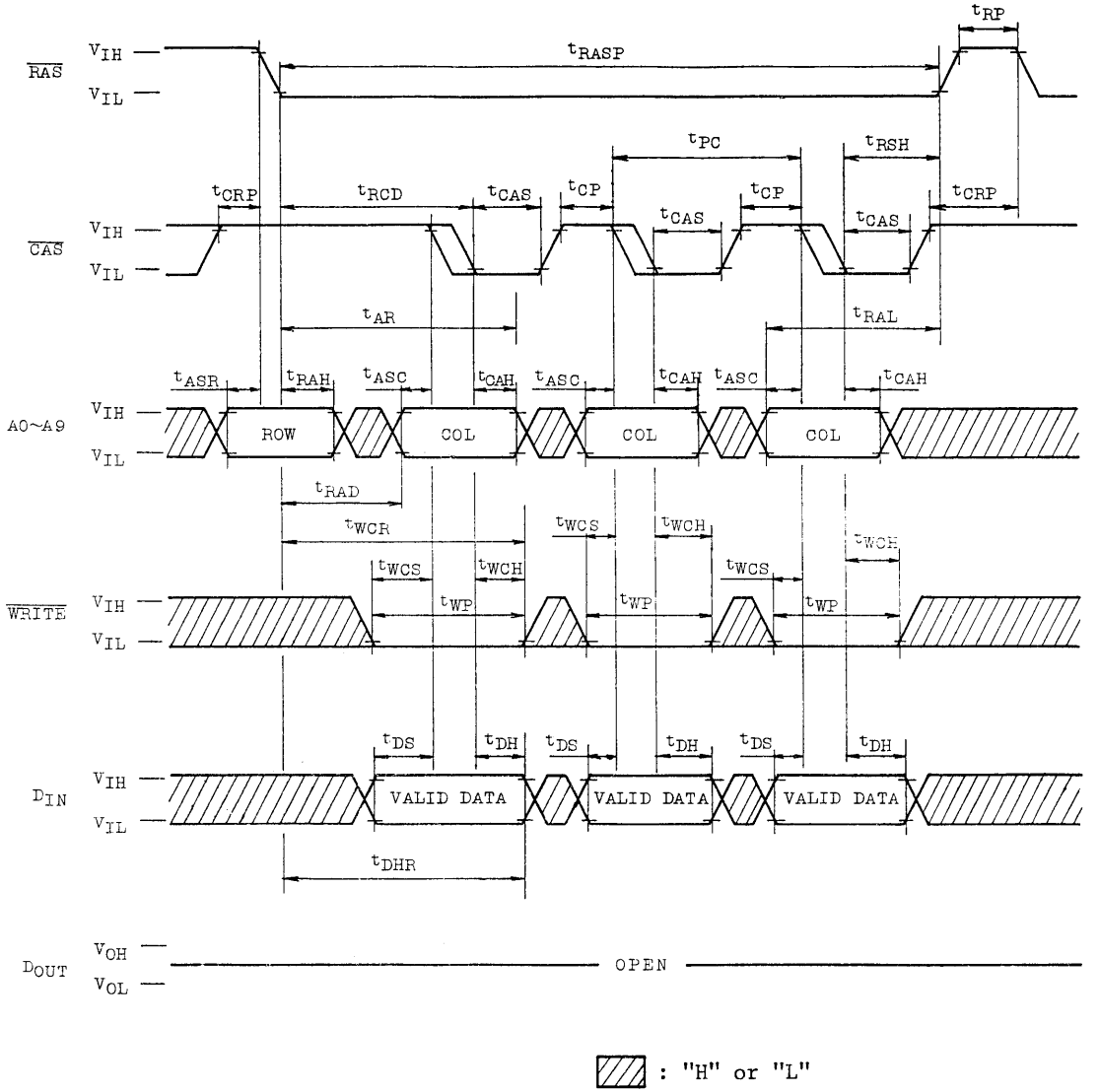


▨: "H" or "L"

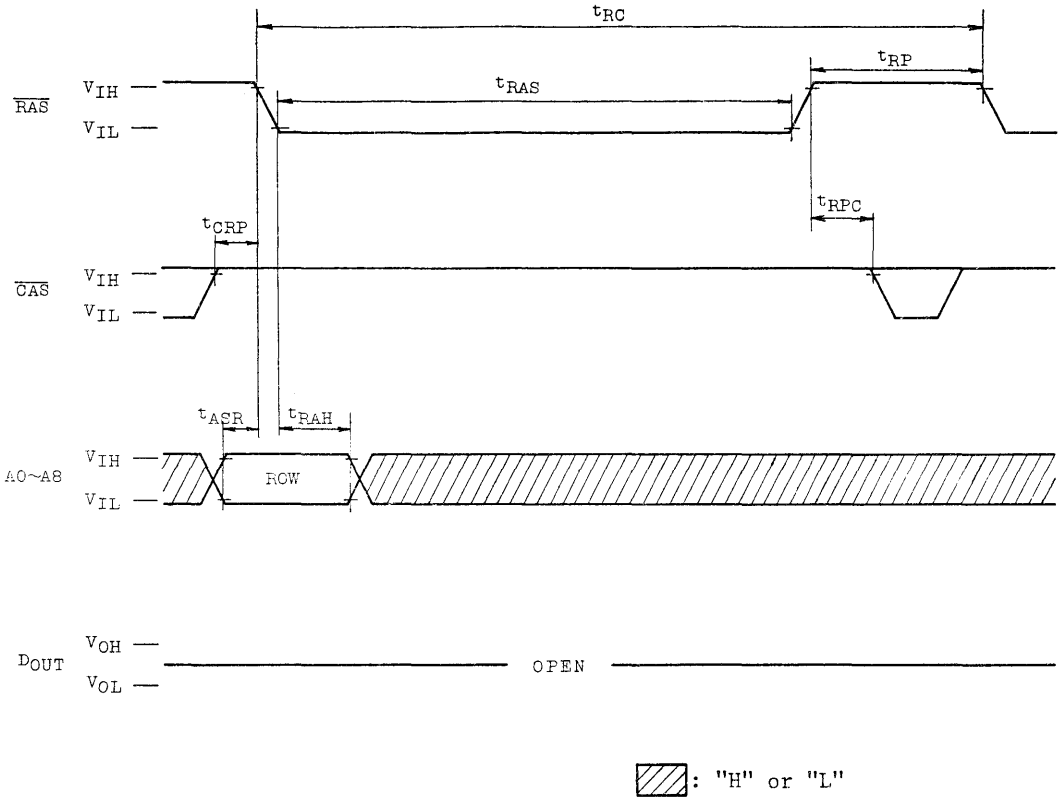
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

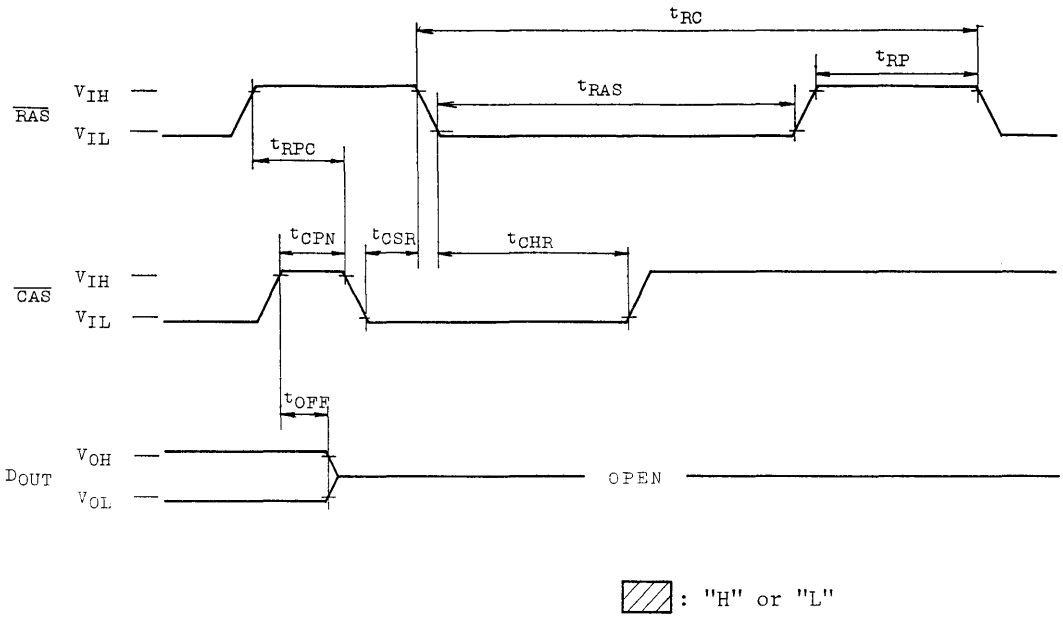


$\overline{RAS}$ ONLY REFRESH CYCLE



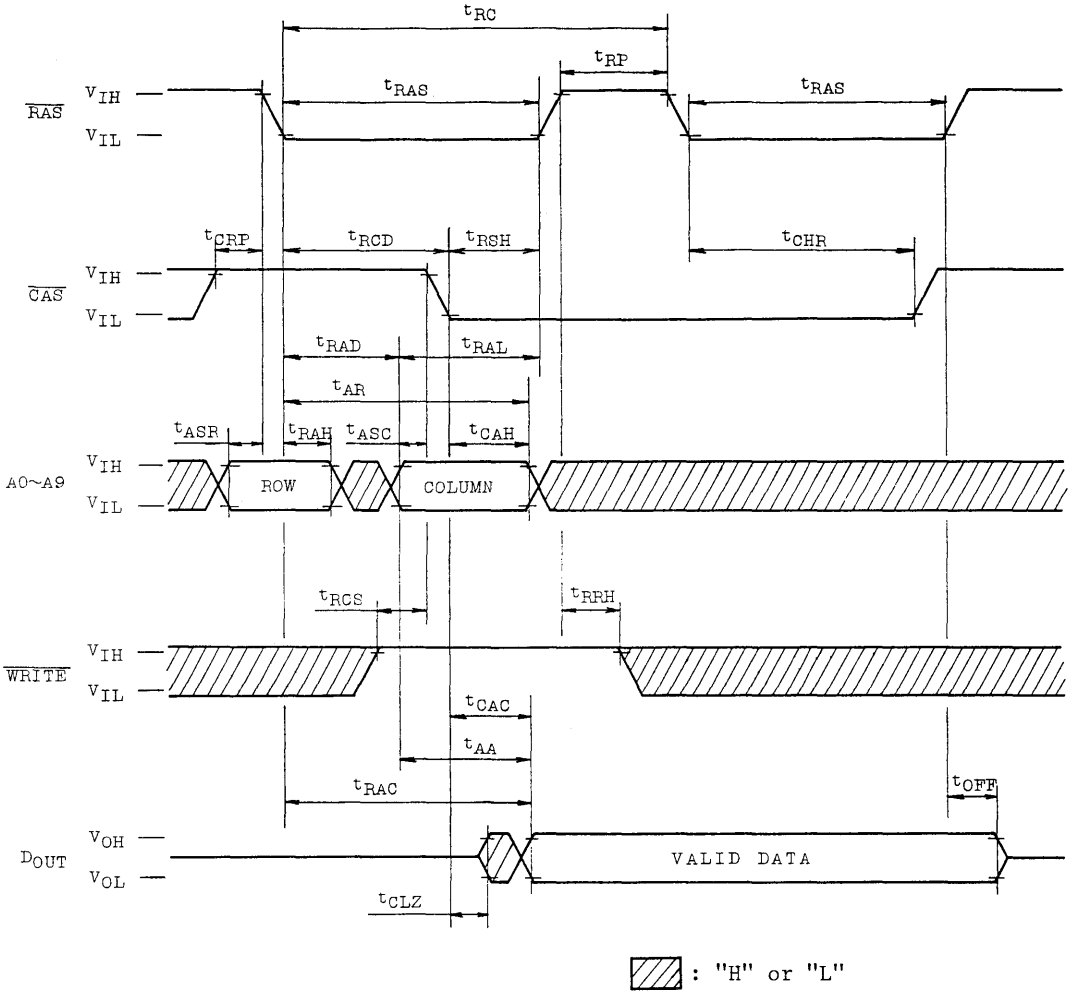
Note: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

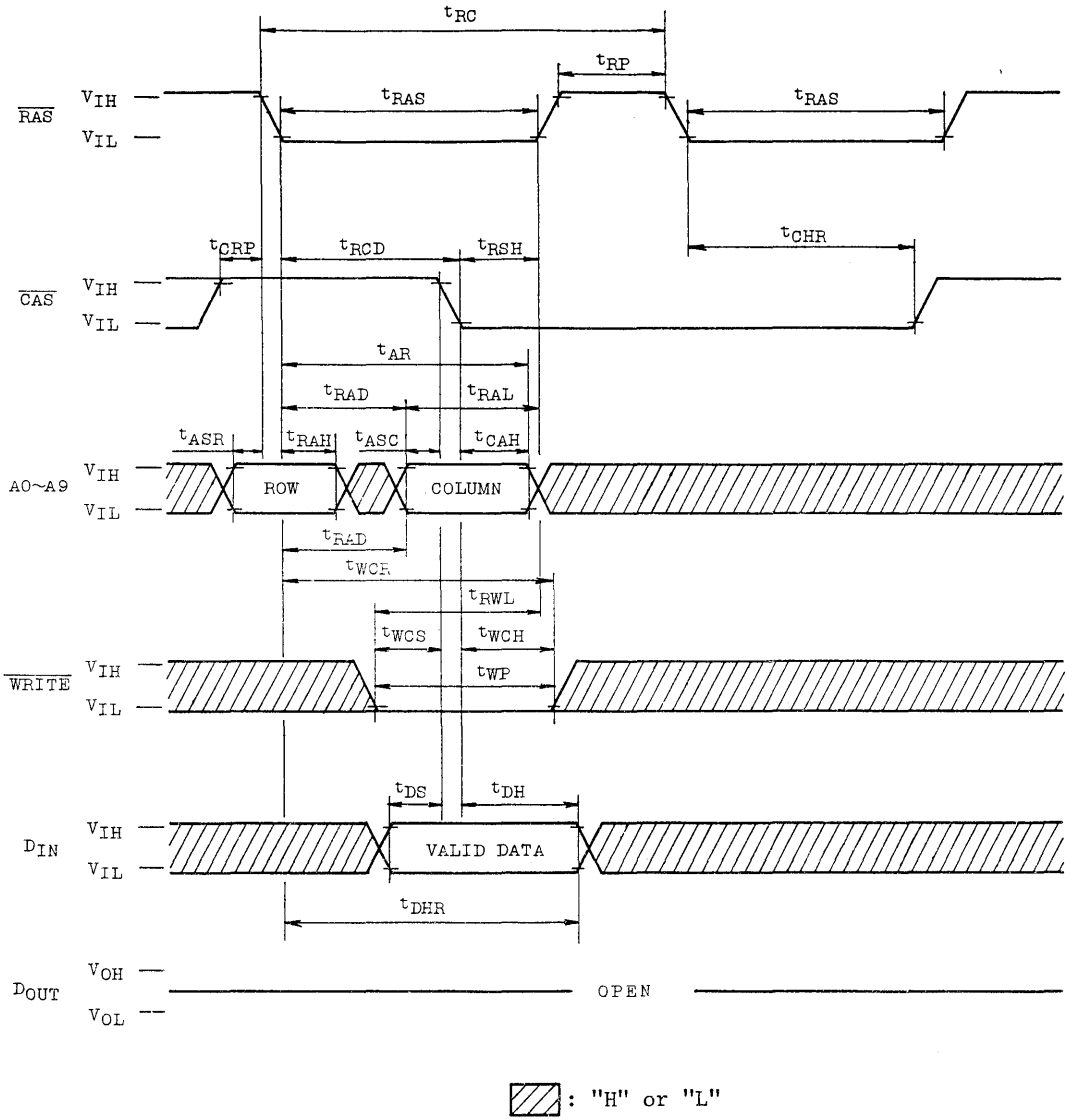


Note: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

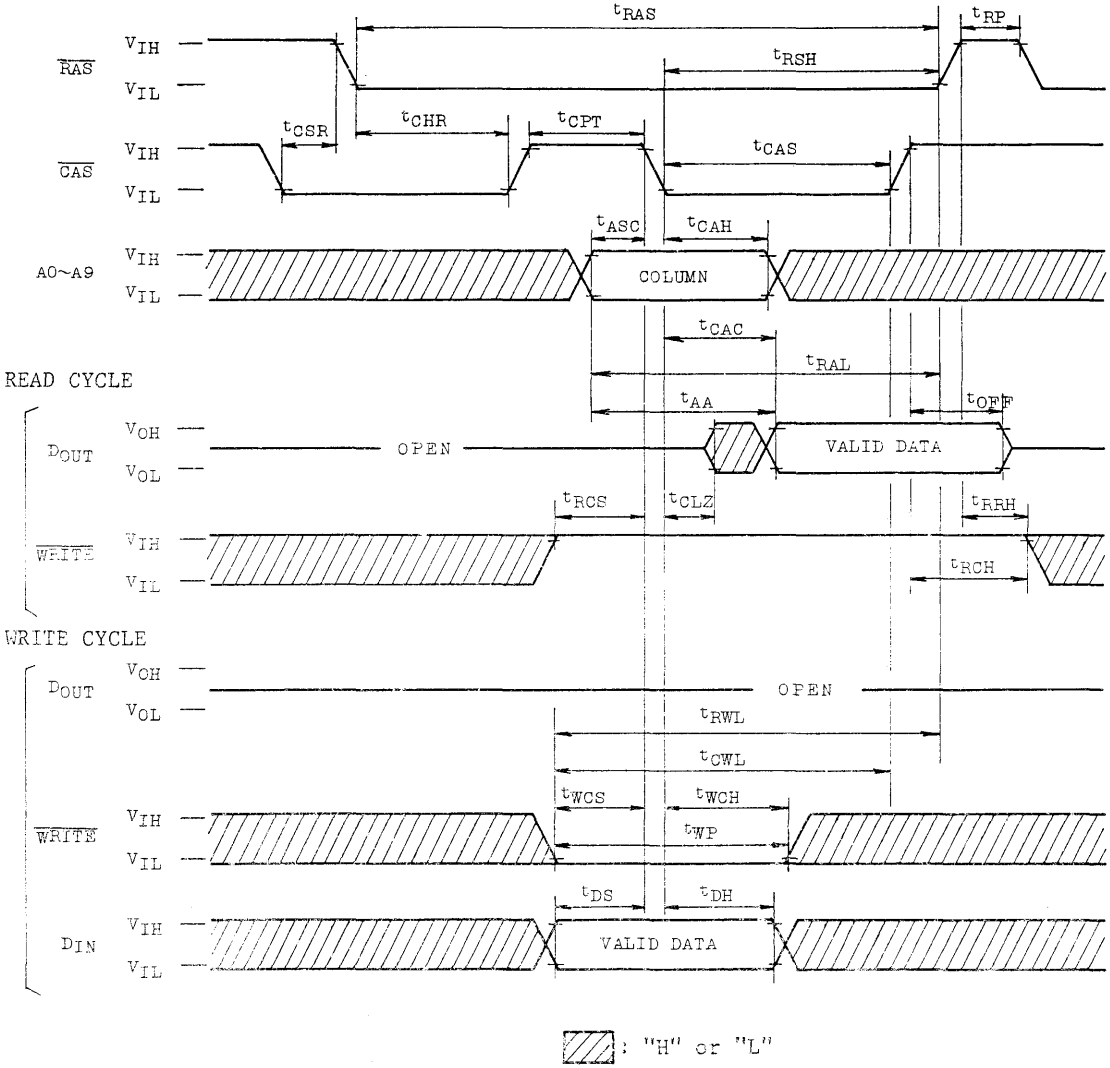
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

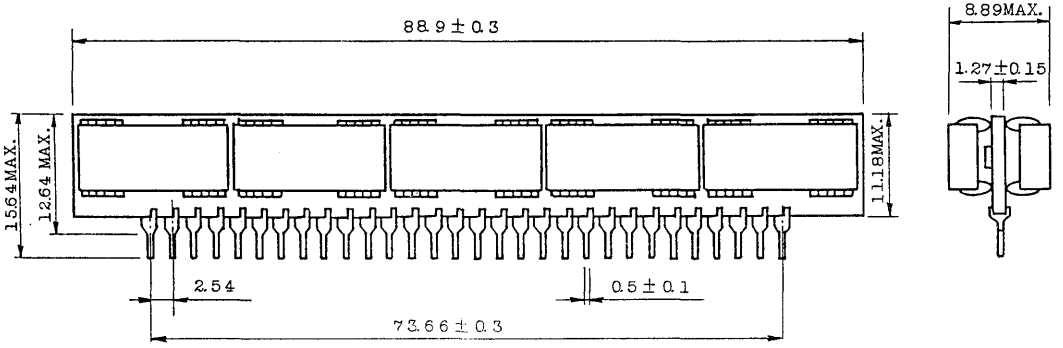


OUTLINE DRAWINGS

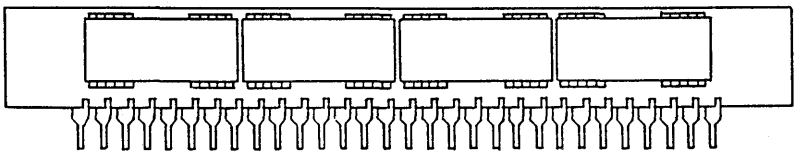
• THM91020L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



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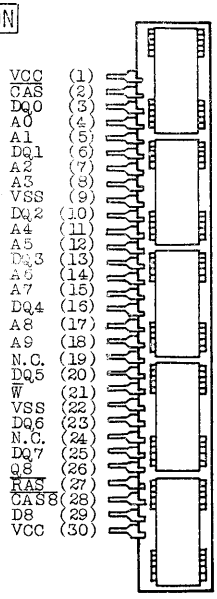
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns	40ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	25ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	50ns

- Single power supply of 5V±10%
- Low power
  - 3,465mW MAX. Operating (THM91021L-85)
  - 2,970mW MAX. Operating (THM91021L-10)
  - 2,475mW MAX. Operating (THM91021L-12)
  - 49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Nibble Mode capability,
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Package Height

PIN CONNECTION

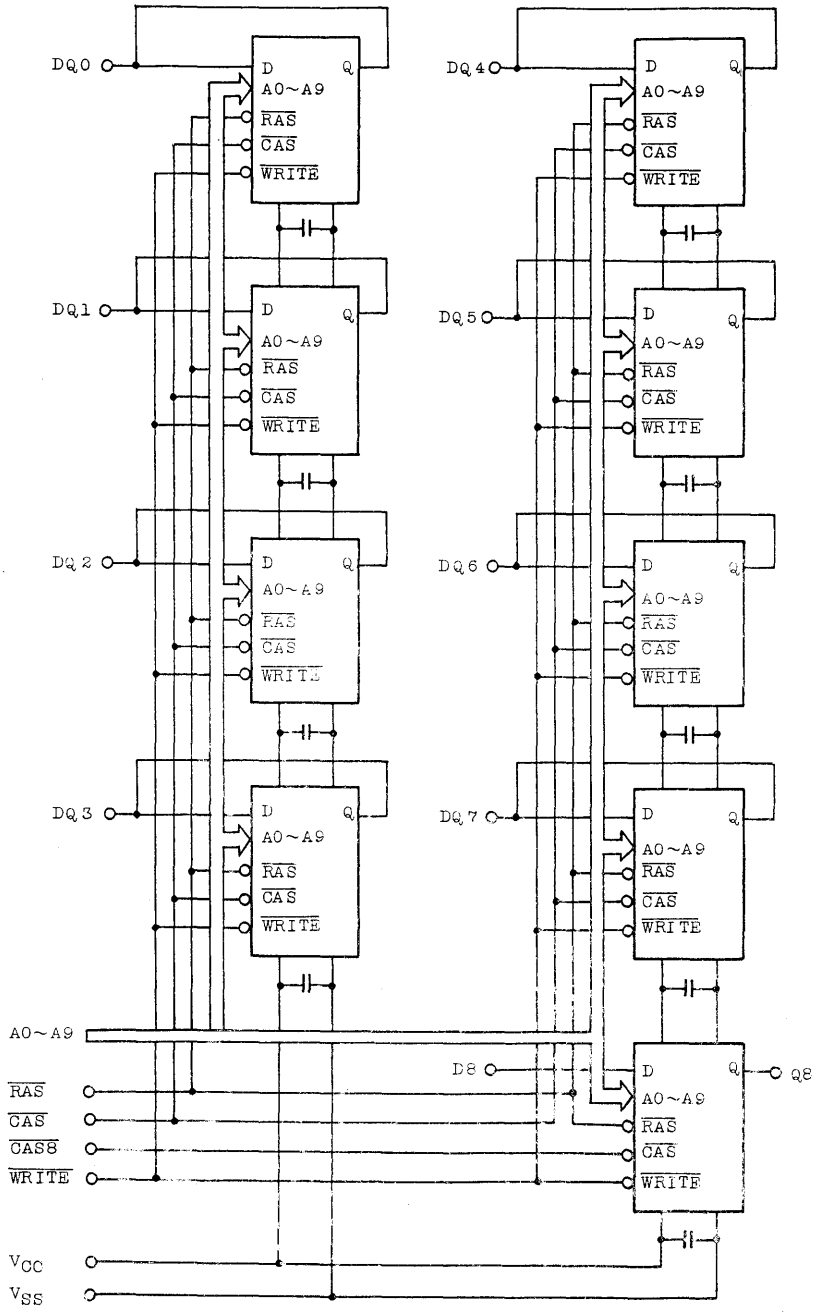
(TOP VIEW)



PIN NAMES

A0 ∿ A9	Address Inputs
DQ0 ∿ DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{CC}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ~ 7.0	V	1
Output Voltage	V_{OUT}	-1 ~ 7.0	V	1
Power Supply Voltage	V_{CC}	-1 ~ 7.0	V	1
Operating Temperature	T_{OPR}	0 ~ 70	°C	1
Storage Temperature	T_{STG}	-55 ~ 125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM91021L-85	-	630	mA	3,4
		THM91021L-10	-	540		
		THM91021L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM91021L-85	-	630	mA	3
		THM91021L-10	-	540		
		THM91021L-12	-	450		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{NC}=t_{NC} MIN.)	THM91021L-85	-	450	mA	3,4
		THM91021L-10	-	360		
		THM91021L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM91021L-85	-	630	mA	3
		THM91021L-10	-	540		
		THM91021L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91021L-85		THM91021L-10		THM91021L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	165	-	190	-	220	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	50	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	30	-	35	-	40	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	25	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	-	35	-	40	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	65	25	80	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	25	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	25	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91021L-85		THM91021L-10		THM91021L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	20	-	25	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	

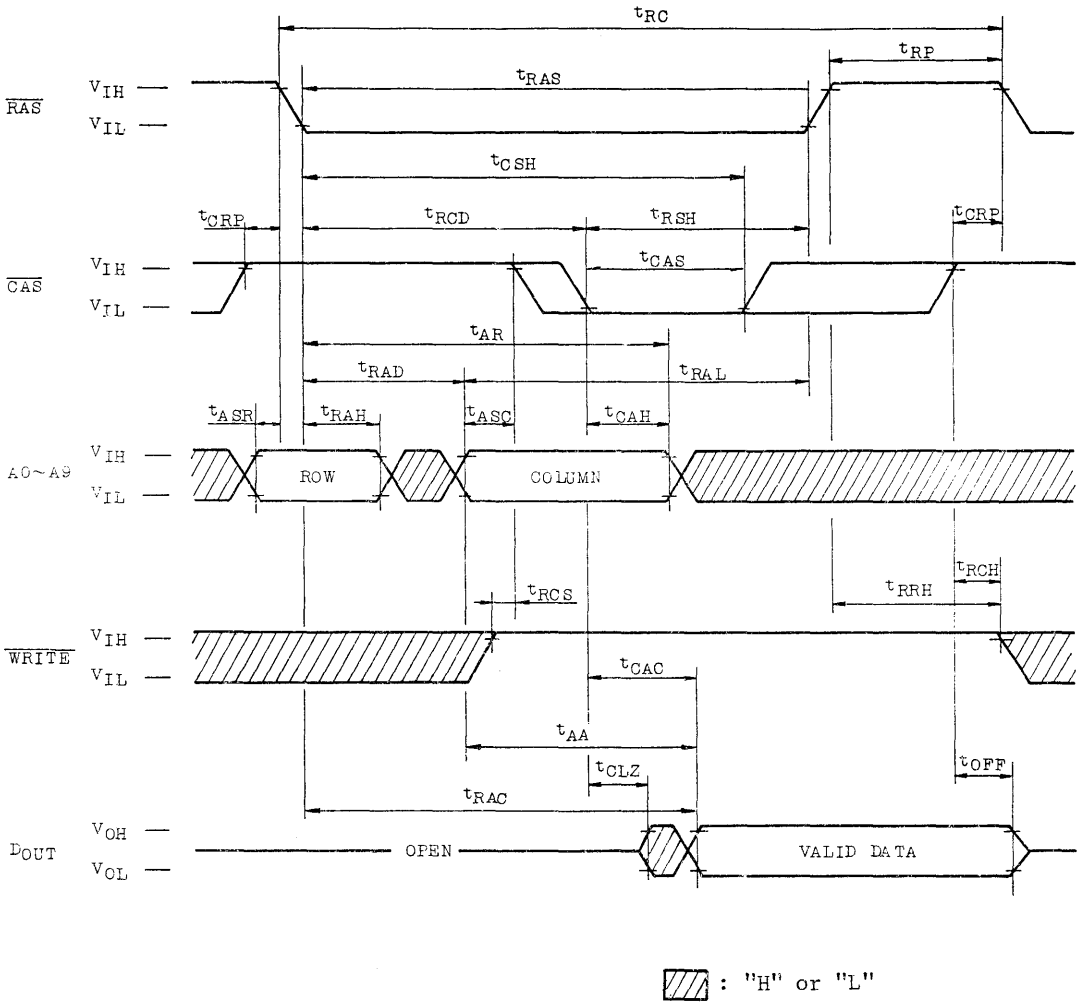
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7)	-	15	pF
C_{Q}	Output Capacitance (Q8)	-	10	pF

NOTES:

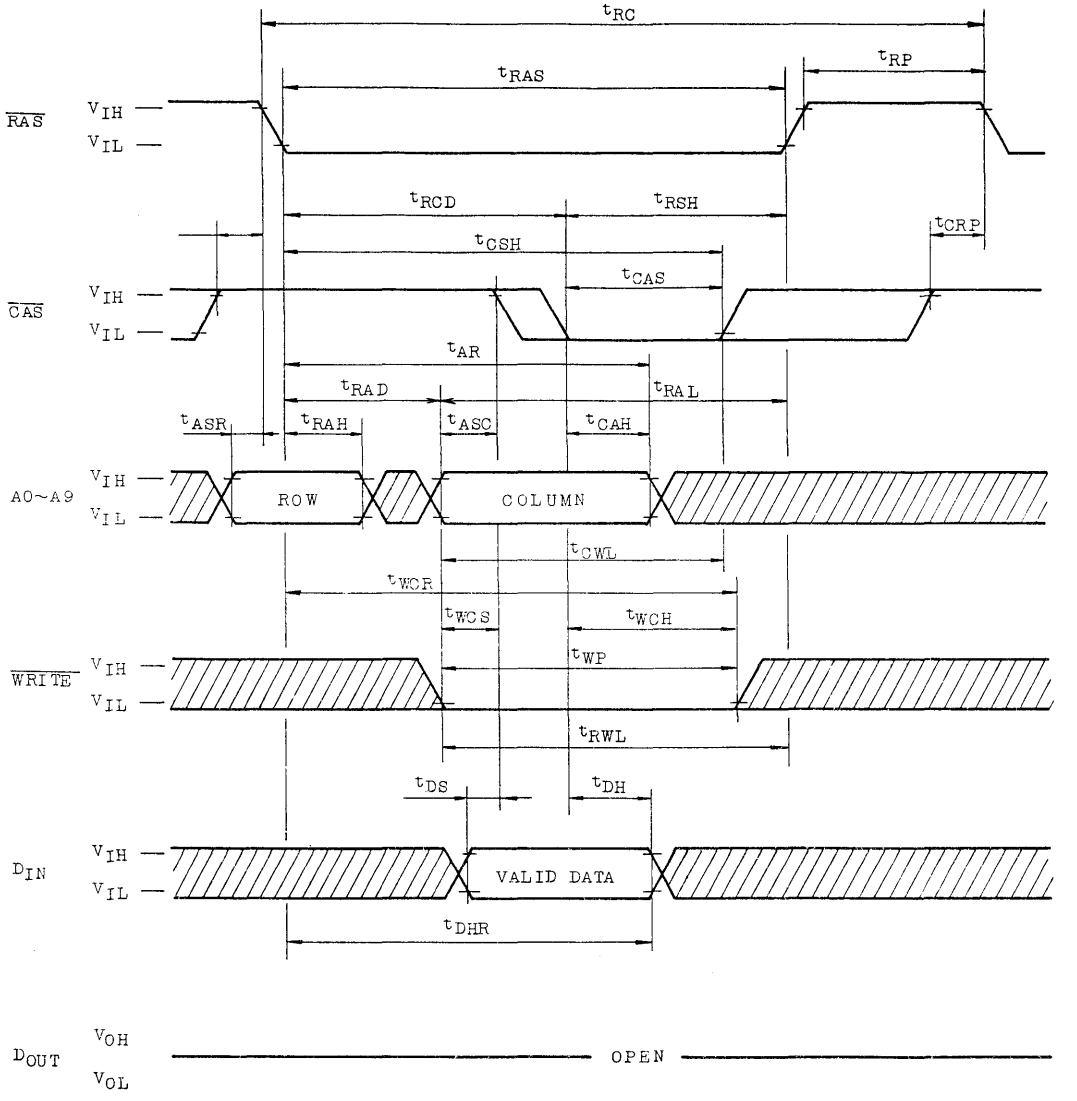
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

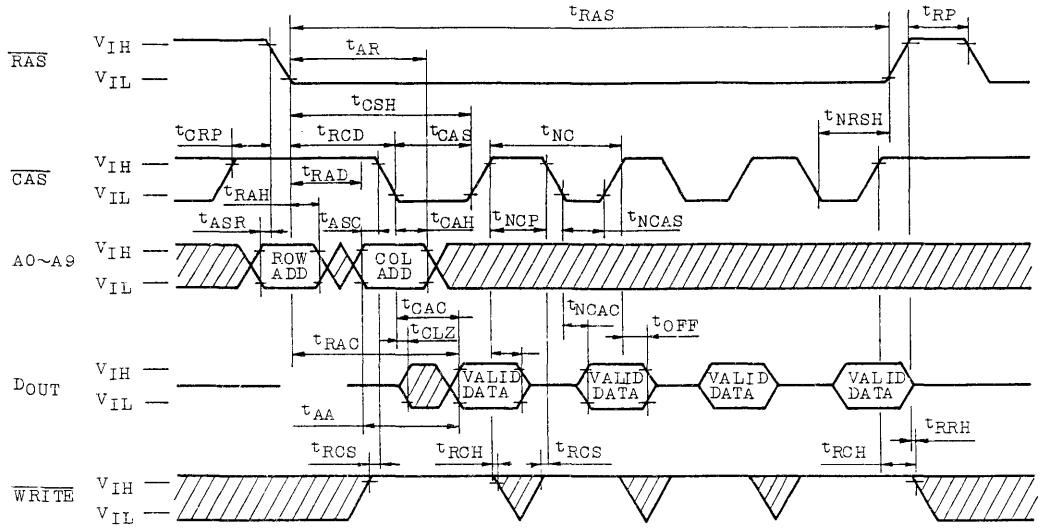


▨ : "H" or "L"

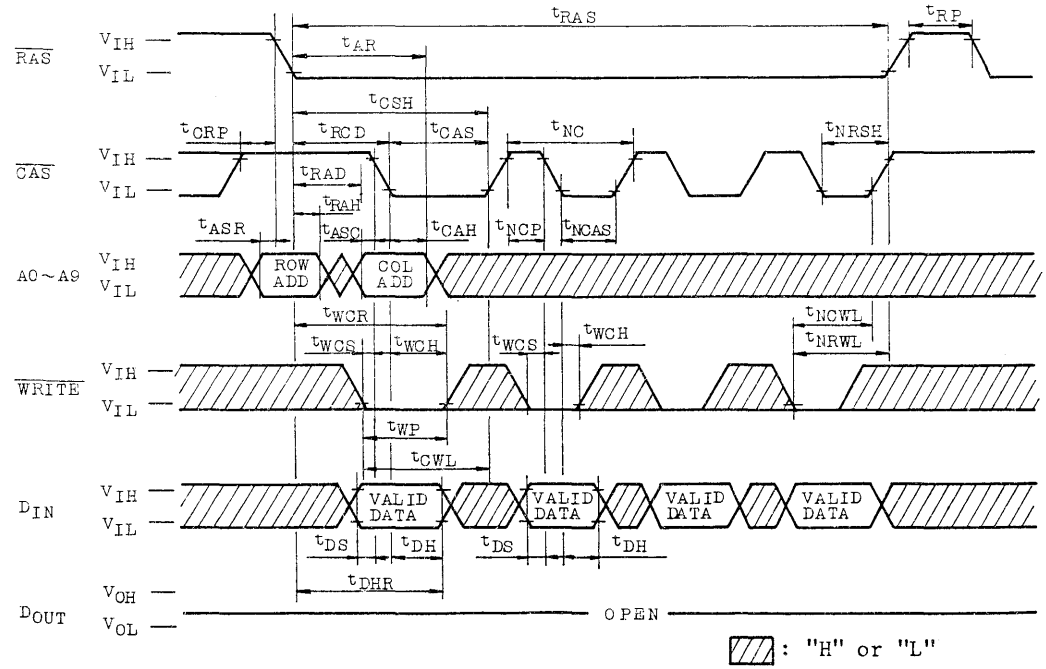
EARLY WRITE CYCLE



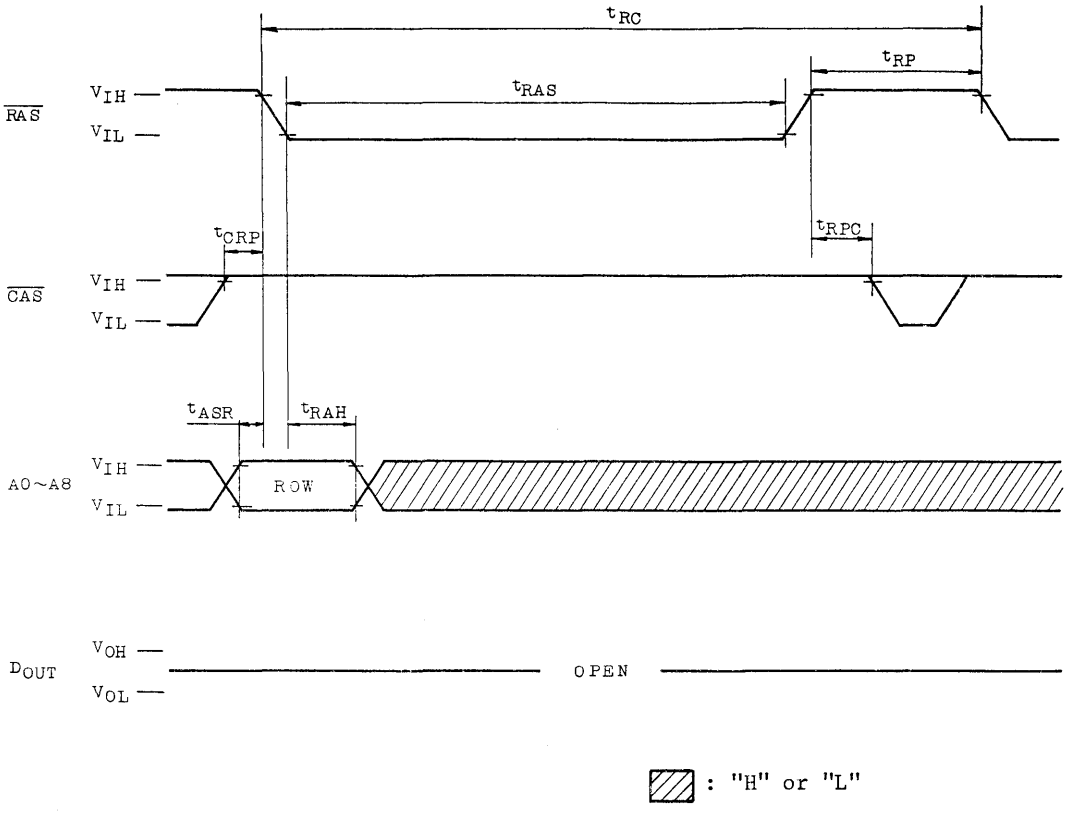
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

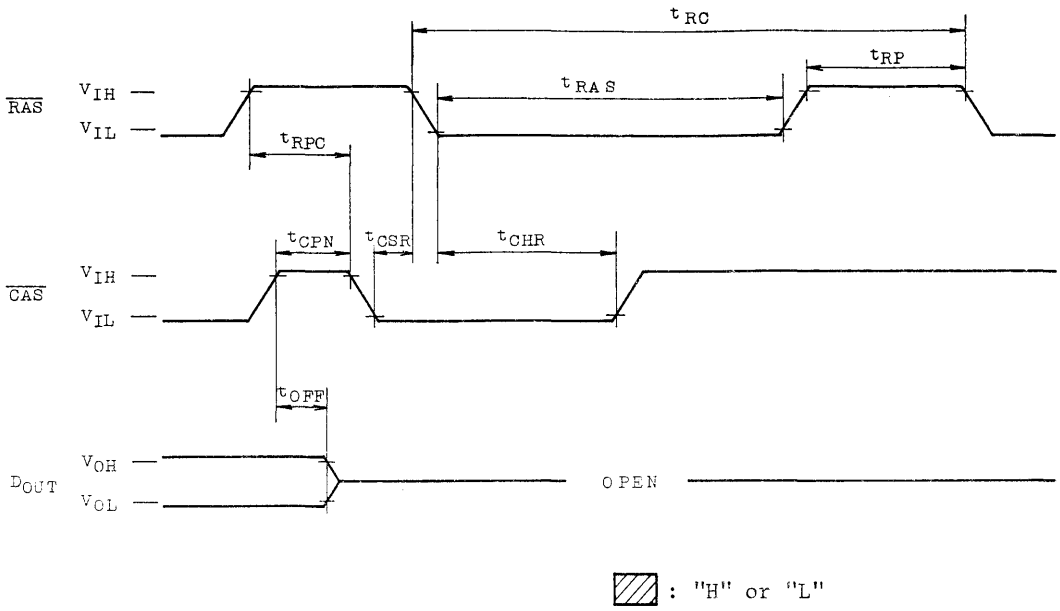


$\overline{RAS}$ ONLY REFRESH CYCLE



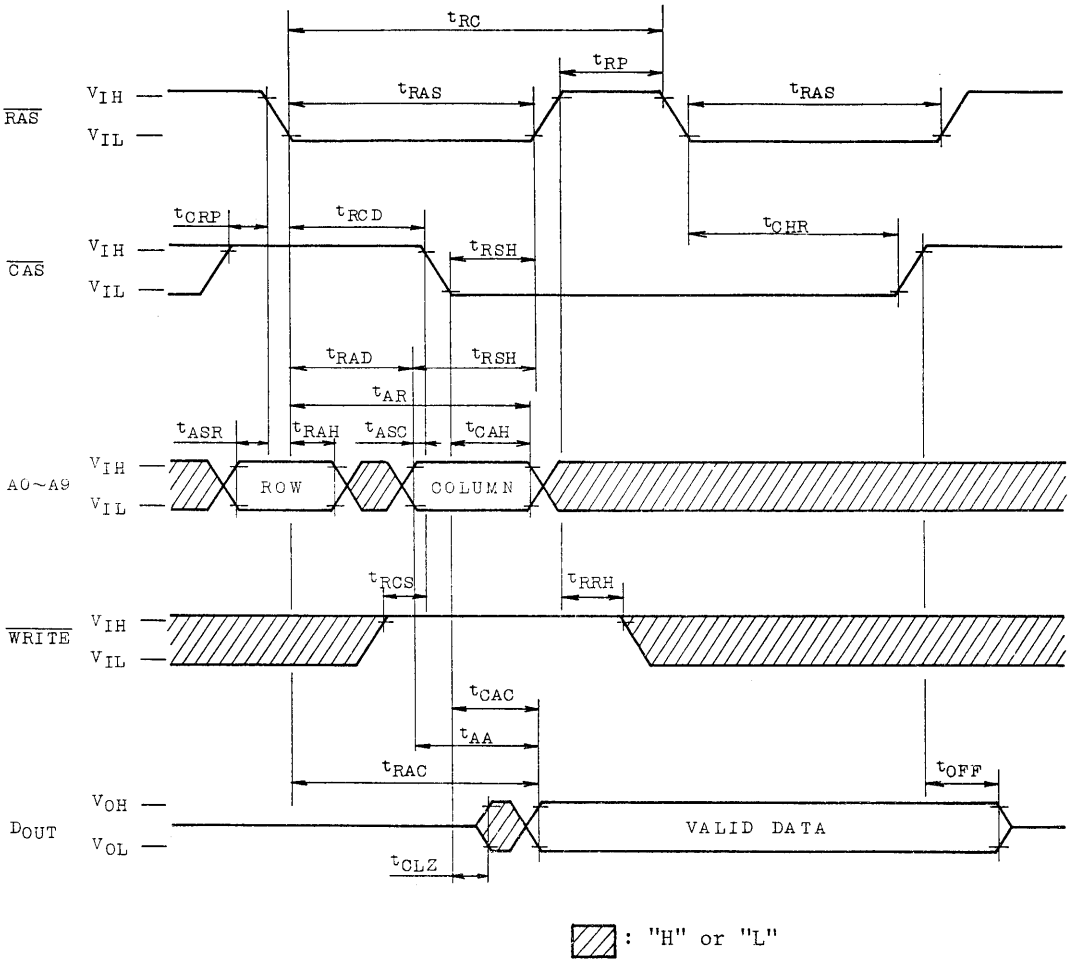
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

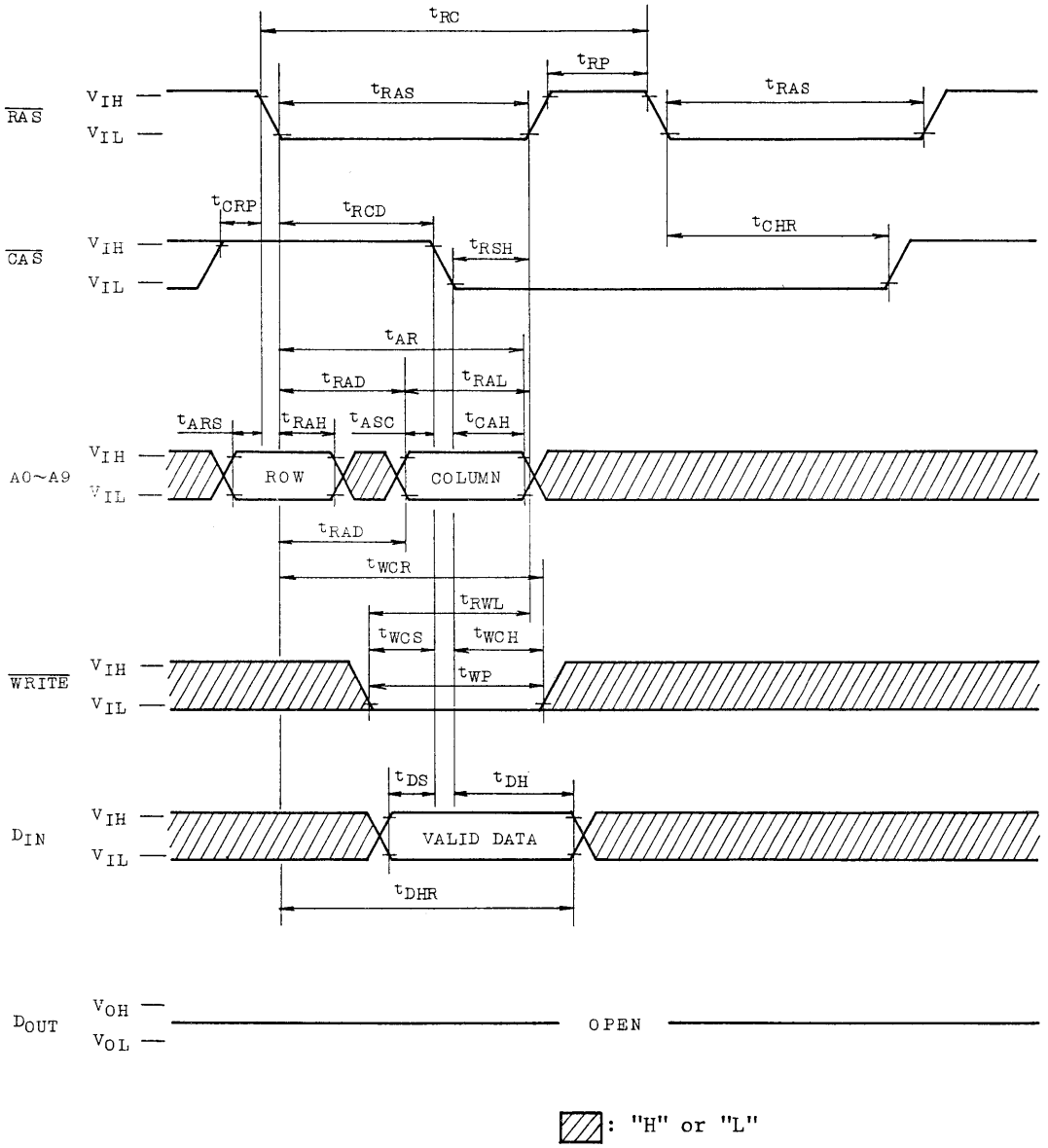


NOTE: $\overline{WRITE}$="H" or "L", A0 ∿ A9="H" or "L"

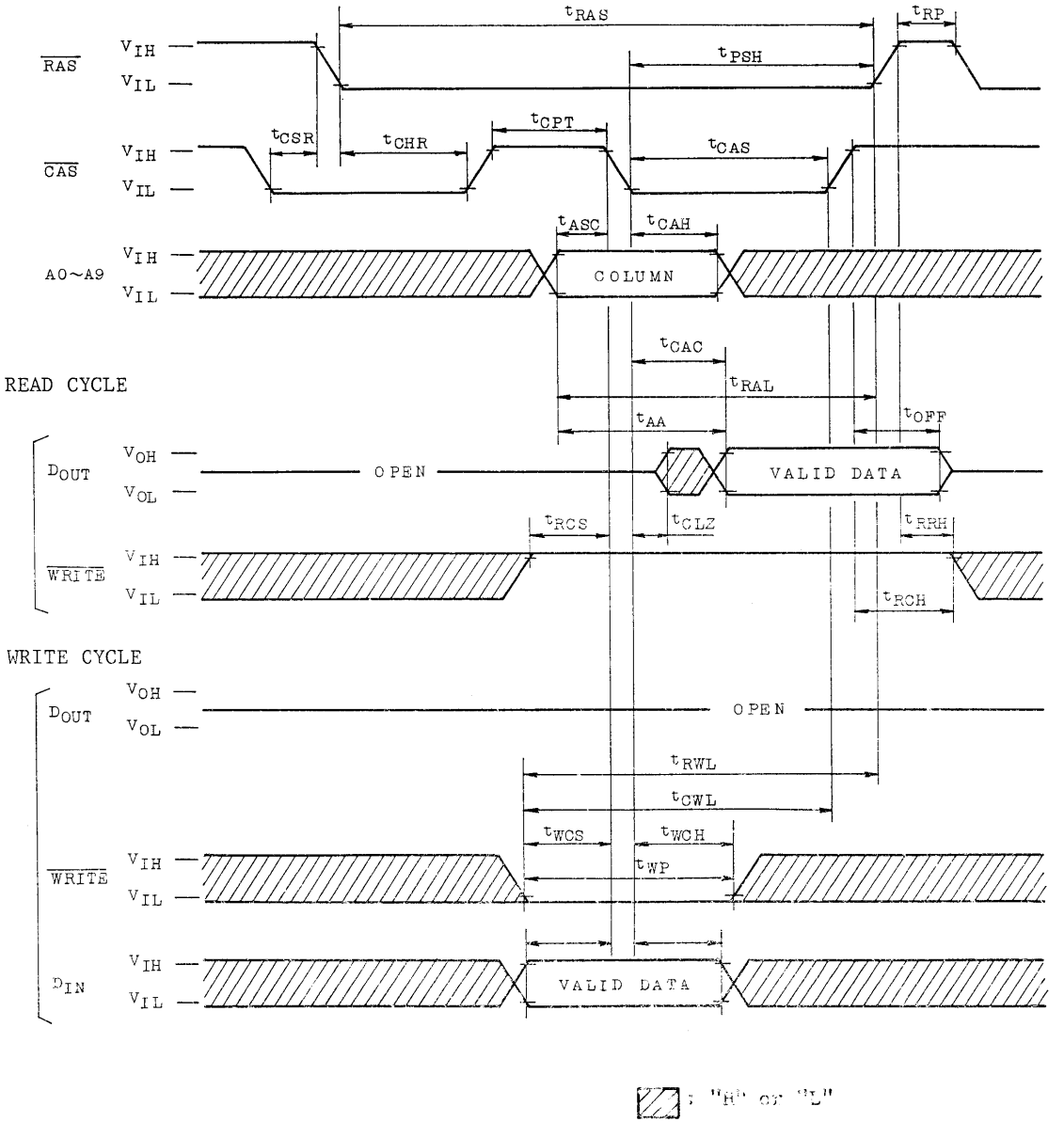
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

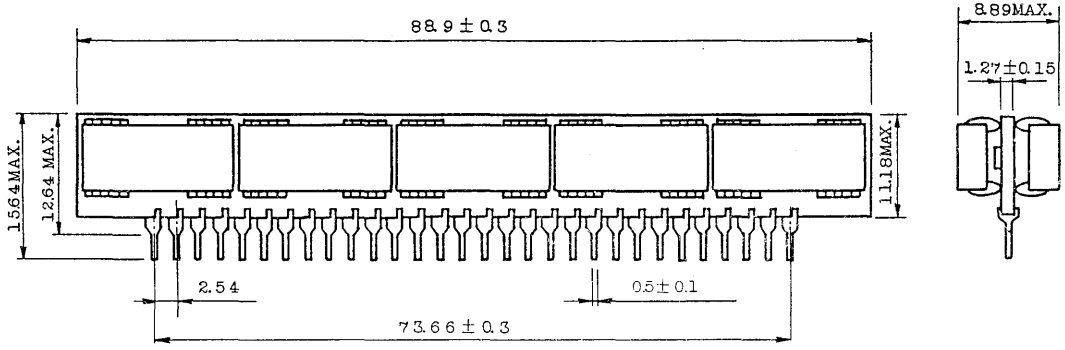


OUTLINE DRAWINGS

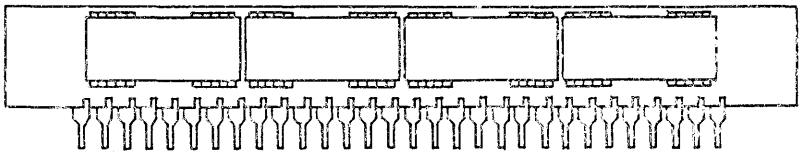
• THM91021L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



THM91022L-85, 10, 12

DESCRIPTION

The THM91022L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511002J on both sides of the printed circuit board.

The THM91022L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

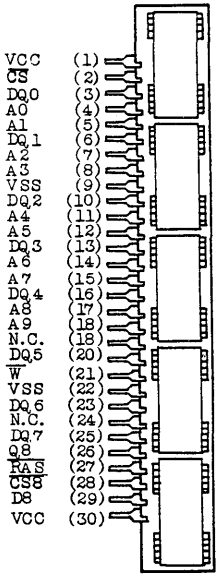
- 1,048,576 words by 9 bits organization
- Fast access time

		THM91022L-85	THM91022L-10	THM91022L-12
t_{RAC}	$\overline{RAS}$ Access Time	85ns	100ns	120ns
t_{AA}	Column Address Access Time	45ns	50ns	60ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	165ns	190ns	220ns
t_{SC}	Static Column Mode Cycle Time	50ns	55ns	65ns

- Single power supply of 5V±10%
- Low power 3,465mW MAX. Operating (THM91022L-85)
  2,970mW MAX. Operating (THM91022L-10)
  2,475mW MAX. Operating (THM91022L-12)
  49.5mW MAX. Standby
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Static Column Mode capability.
- All inputs and outputs TTL comatible
- 512 refresh cycles/8ms
- 12.64mm MAX. Package Height

PIN CONNECTION

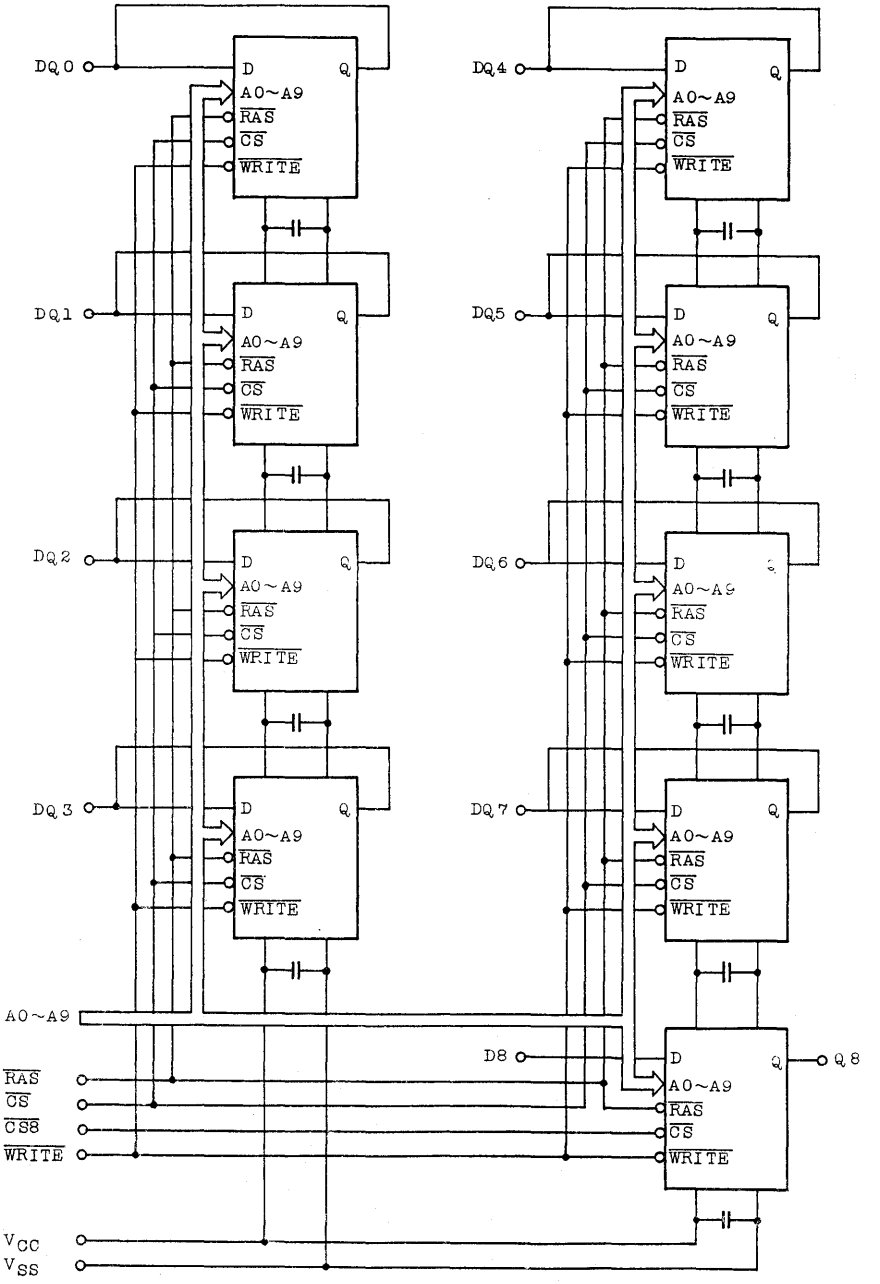
(TOP VIEW)



PIN NAMES

A0 ∿ 9	Address Inputs
DQ0 ∿ 7	Data Input/Outpus
D8	Data Input
Q8	Data Output
$\overline{CS}$	Chip Select Input
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CS8}$	Chip Select Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLCOK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1 ∿ 7	V	1
Output Voltage	V_{OUT}	-1 ∿ 7	V	1
Power Supply Voltage	V_{CC}	-1 ∿ 7	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C·sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM91022L-85	-	630	mA	3,4
		THM91022L-10	-	540		
		THM91022L-12	-	450		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{IH})		-	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM91022L-85	-	630	mA	3
		THM91022L-10	-	540		
		THM91022L-12	-	450		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS}$=$\overline{CS}$=V_{IH}, Address Cycling: t_{SC}=t_{SC} MIN.)	THM91022L-85	-	450	mA	3,4
		THM91022L-10	-	360		
		THM91022L-12	-	270		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CS}$=V_{CC}-0.2V)		-	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM91022L-85	-	630	mA	3
		THM91022L-10	-	540		
		THM91022L-12	-	450		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Lekage Current, any Input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins not under Test=0V)		-90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V = V_{OUT} = 5.5V)		-20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91022L-85		THM91022L-10		THM91022L-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cylce Time	165	-	190	-	220	-	ns	
t_{SC}	Static Column Mode Cycle Time	50	-	55	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	85	-	100	-	120	ns	8,13
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	8,13
t_{AA}	Access Time from Column Address	-	45	-	50	-	60	ns	8,14
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	5	-	5	-	5	-	ns	8
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	30	0	35	ns	9
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	30	-	30	-	35	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	0	-	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	70	-	80	-	90	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	85	100,000	100	100,000	120	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	85	-	100	-	120	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	25	60	25	75	25	90	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address delay Time	20	40	20	50	20	60	ns	14
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time (Static Column Mode)	10	-	10	-	15	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	15	-	15	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	20	-	20	-	20	-	ns	
t_{AWR}	Write Address Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	100	-	115	-	140	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	-	50	-	60	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM91022L-85		THM91022L-10		THM91022L-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	10	-	10	-	15	-	ns	16
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	25	-	30	-	ns	
t_{RCS}	Read Command Set-Up Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WH}	Write Command Hold Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{WI}	Write Command Inactive Time	10	-	10	-	15	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-In Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WS}	Write Command Set-Up Time (Output Data Disable)	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∼70°C)

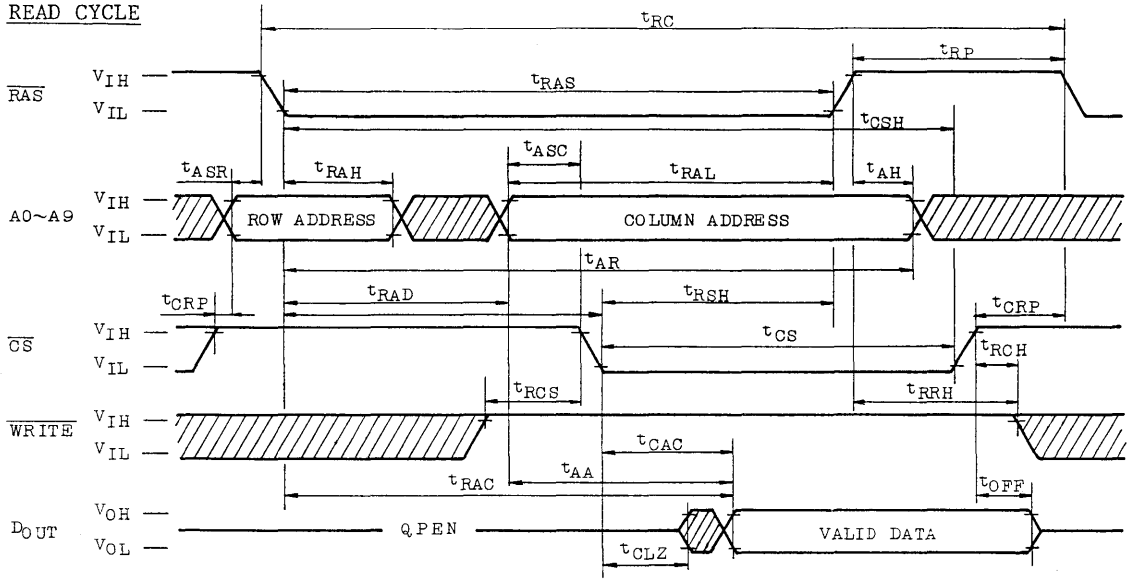
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∼A9, $\overline{W}$, $\overline{CS}$, $\overline{RAS}$)	-	60	pF
C_{I2}	Input Capacitance (D8, $\overline{CS8}$)	-	7	pF
C_{DQ}	I/O Capacitance (DQ0∼DQ7)	-	15	pF
C_{Q}	Output Capacitance (Q8)	-	10	pF

NOTES:

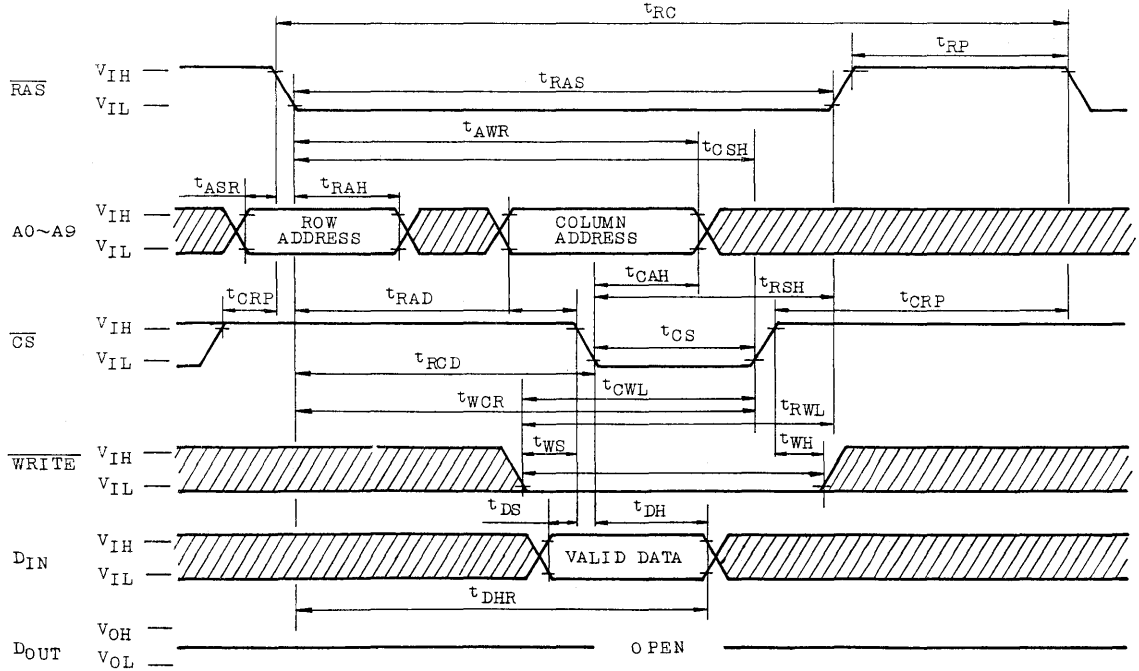
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 RAS cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CS}$ leading edge.
12. t_{WS}, t_{WH} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$(min.) and $t_{WH} \geq t_{WH}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycles.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
15. t_{AH} is the condition to latch column address when $\overline{RAS}$ ahs rised up.

TIMING WAVEFORMS

READ CYCLE

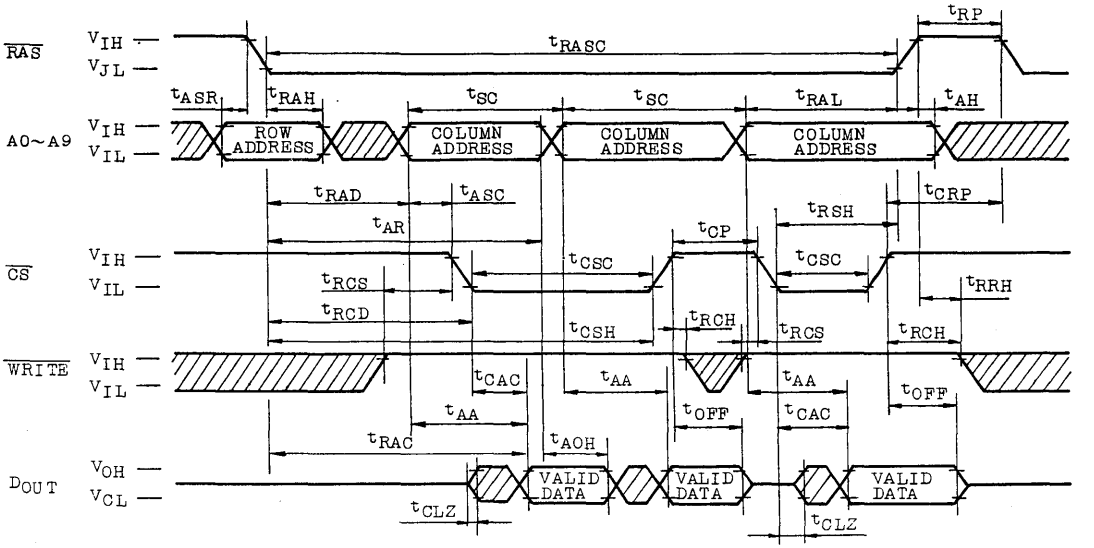


WRITE CYCLE (EARLY WRITE)

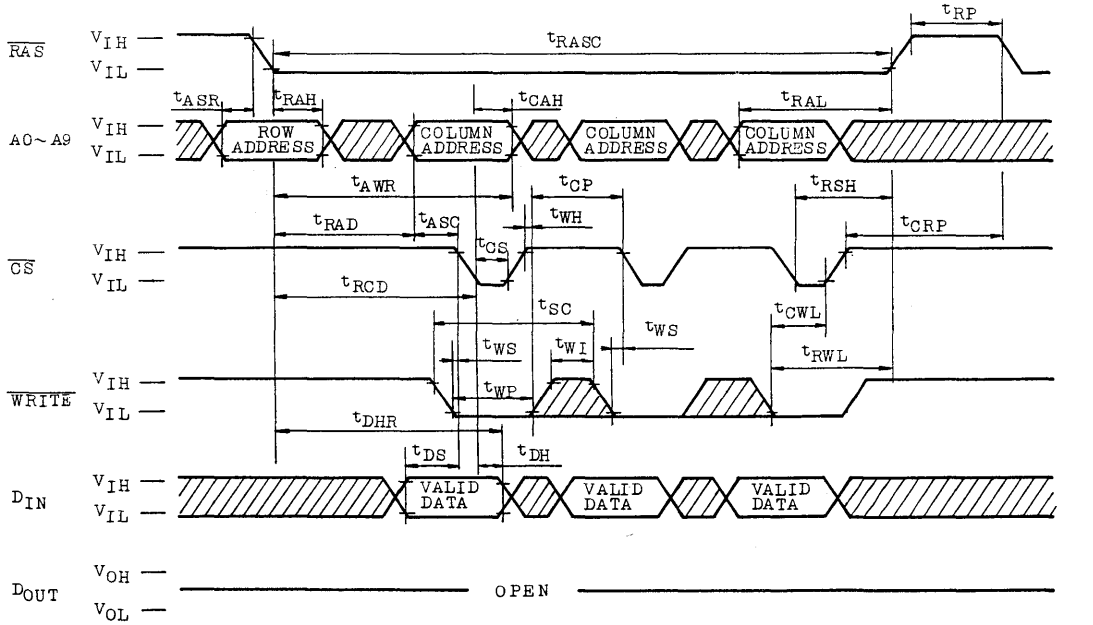


▨: "H" or "L"

STATIC COLUMN MODE READ CYCLE

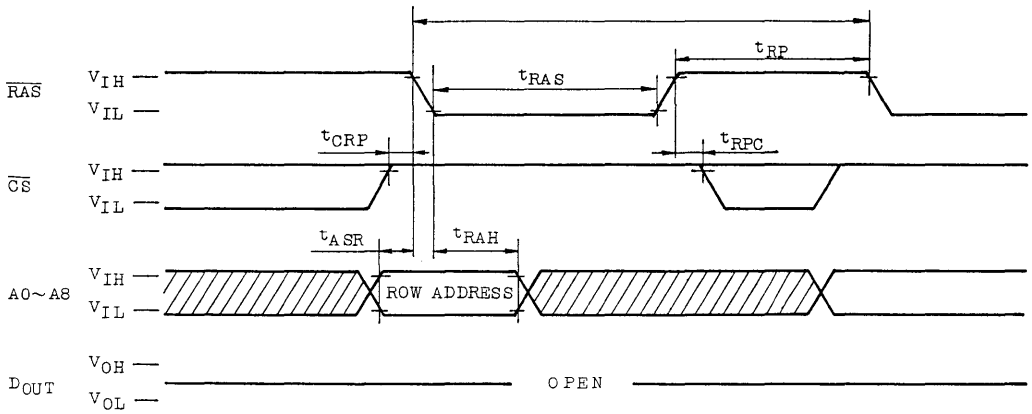


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



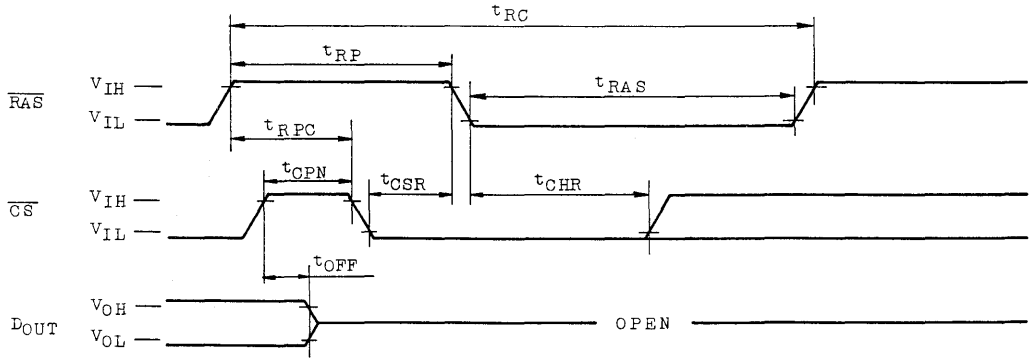
▨: "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



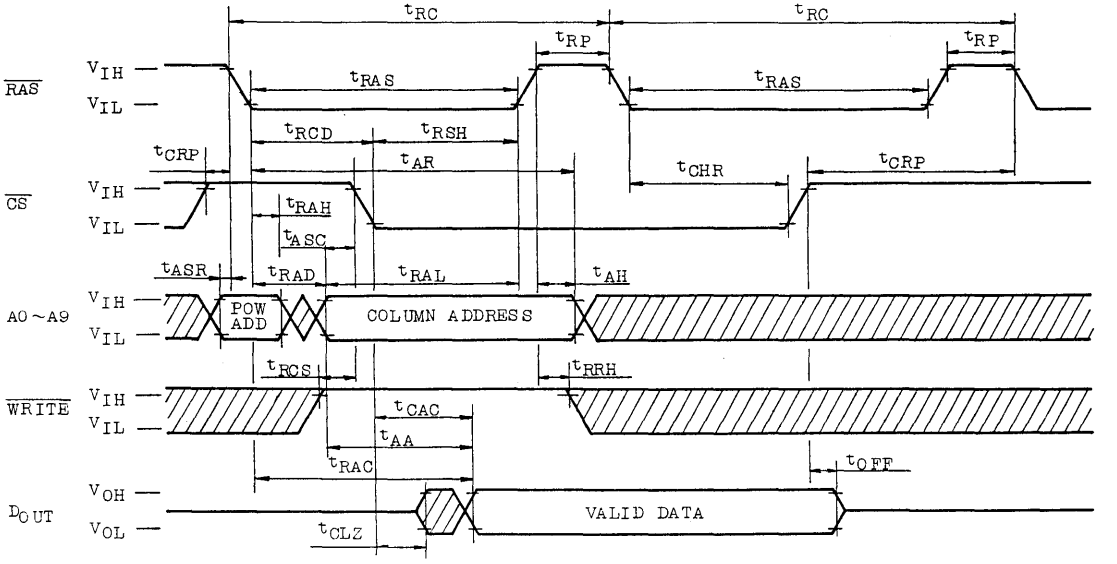
NOTE: $\overline{WRITE}$="H" or "L", A9="H" or "L" ▨: "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

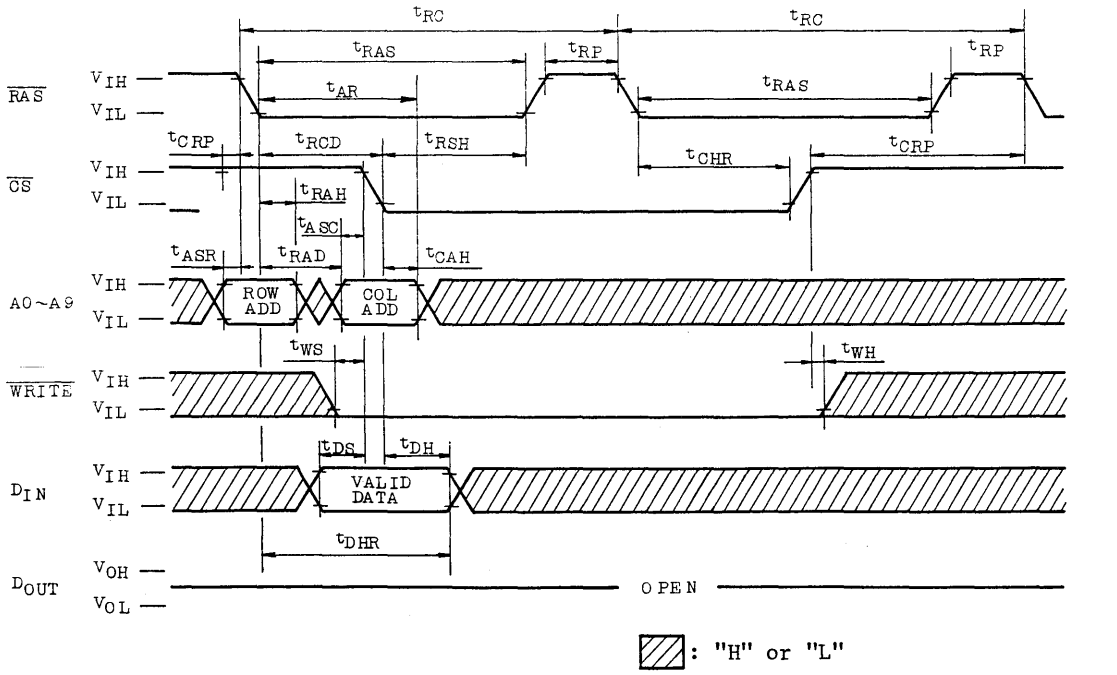


NOTE: $\overline{WRITE}$="H" or "L", A0∿A9="H" or "L"

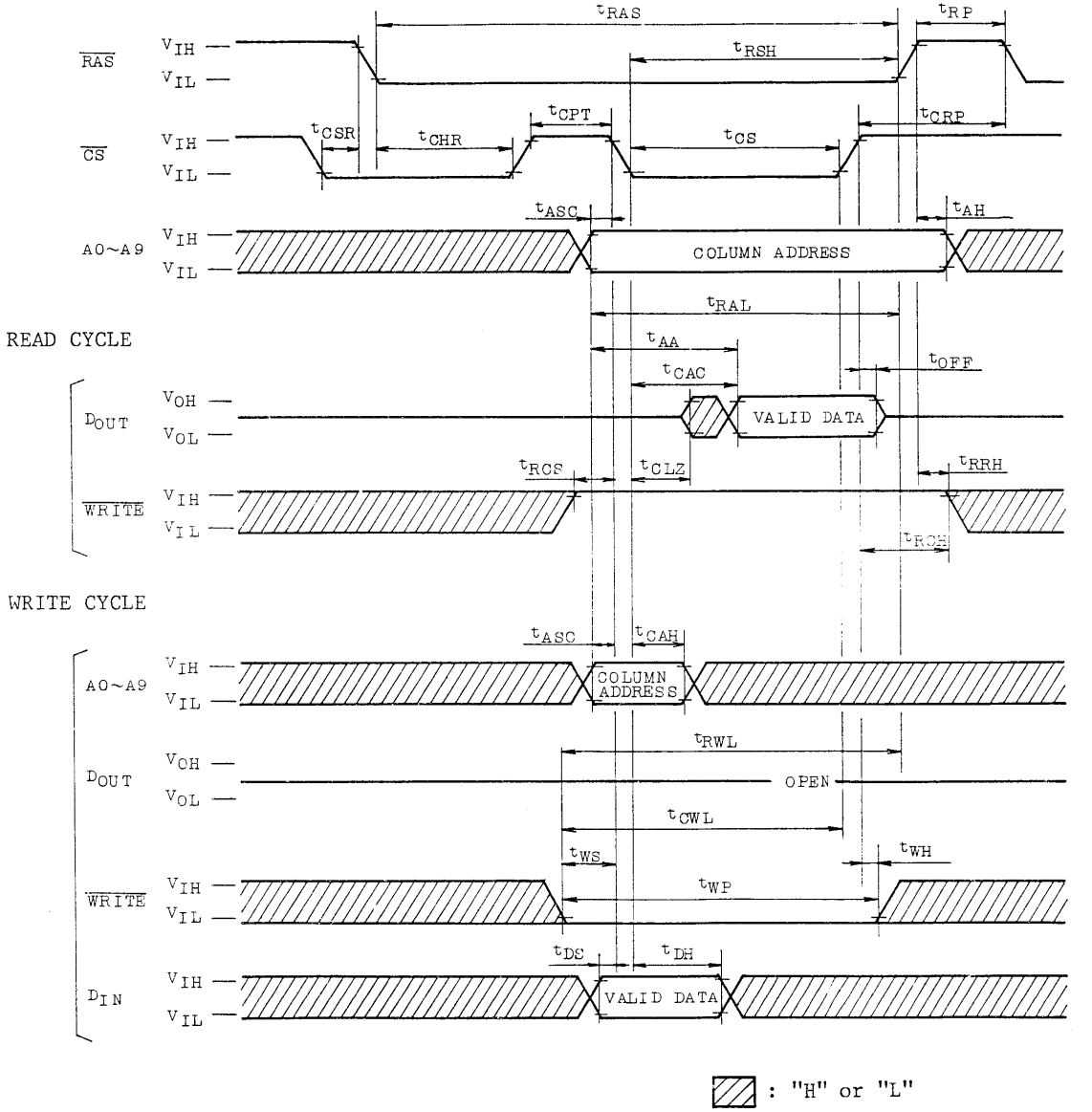
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



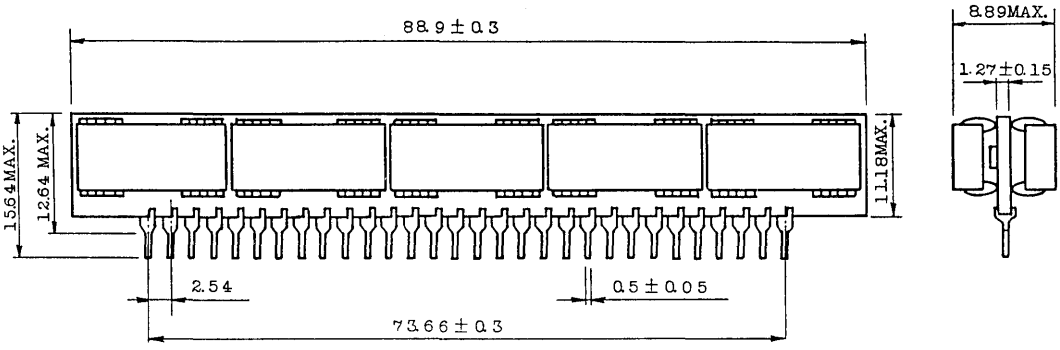
: "H" or "L"

OUTLINE DRAWINGS

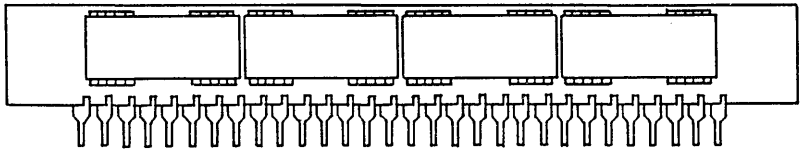
• THM91022L

Unit in mm

THE FRONT SIDE



THE BACK SIDE



THM362500S-85, 10, 12

DESCRIPTION

The THM362500S is a 262,144 words by 36 bits dynamic RAM module which assembled 8 pcs of TC511000J and 4pcs of THM41256AT on the printed circuit board.

The THM362500S is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

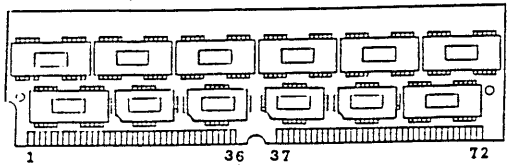
FEATURES

262,144 Words by 36 bits organization
Fast access time

	THM362500S-85	THM362500S-10	THM362500S-12
tRAC $\overline{RAS}$ Access Time	85ns	100ns	120ns
tAA Column Address Access Time	45ns	50ns	60ns
tCAC $\overline{CAS}$ Access Time	45ns	50ns	60ns
tRC Cycle Time	165ns	190ns	220ns
tPC Fast Page Mode Cycle Time	70ns	85ns	105ns

Single power supply of 5V ± 5%
Low power 5,280mW MAX. Operating (THM362500S-85)
4,620mW MAX. Operating (THM362500S-10)
3,960mW MAX. Operating (THM362500S-12)
154mW MAX. Standby
CAS before RAS refresh, RAS only refresh, Hidden refresh, and Fast Page Mode capability.
All inputs and outputs TTL compatible
512 refresh cycle/4ms

PIN CONNECTION (TOP VIEW)



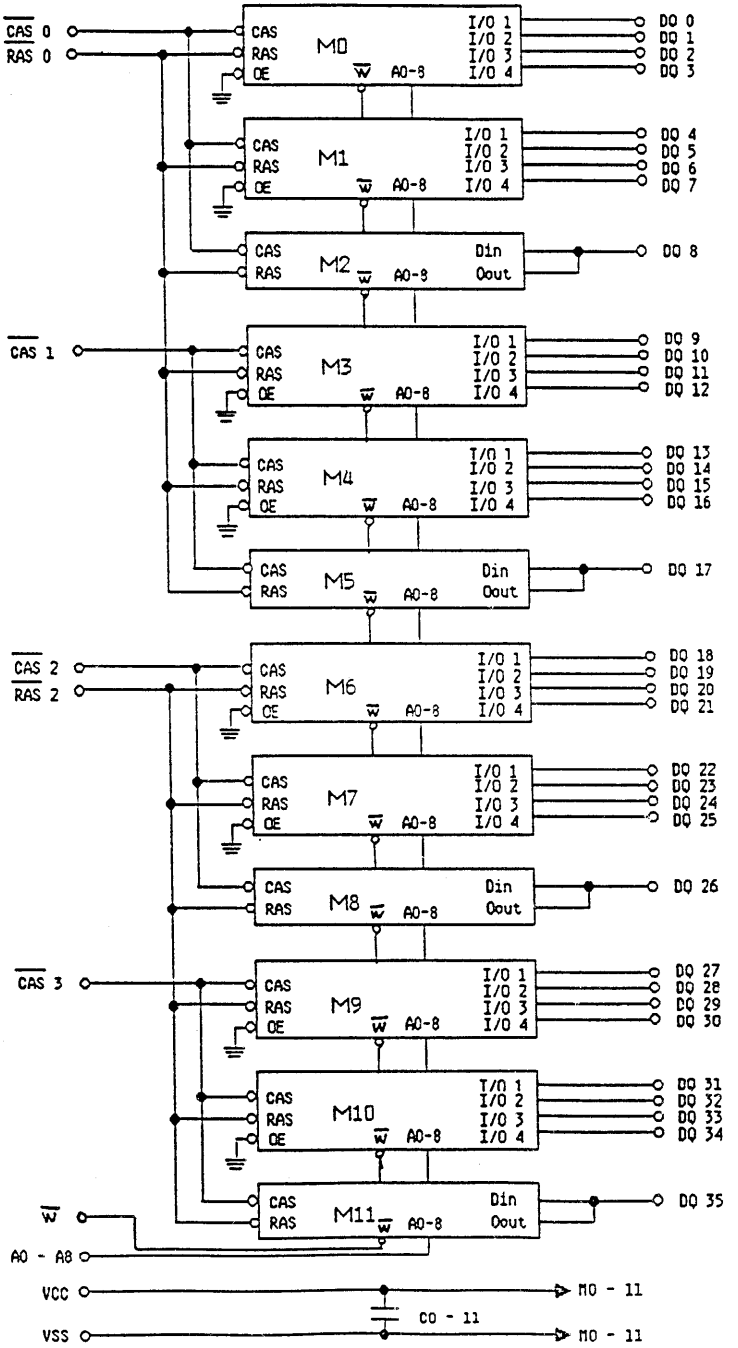
1	Vss	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	Vss	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	Vcc	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	Vcc	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	Vcc	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	Vss

PIN NAME

A0-A8	Address Inputs
DQ0-DQ35	Data Input/Outputs
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$, $\overline{RAS2}$	Row Address strobe
$\overline{W}$	Read/Write Input
Vcc	Power(+5V)
Vss	Ground
NC	No Connection
PD0 - PD3	Presence Detect

	-85	-10	-12
PD0	GND	GND	GND
PD1	NC	NC	NC
PD2	NC	GND	NC
PD3	GND	GND	NC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0 ∿ 7.0	V	1
Output Voltage	V_{OUT}	-1.0 ∿ 7.0	V	1
Power Supply Voltage	V_{CC}	-1.0 ∿ 7.0	V	1
Operating Temperature	T_{OPR}	0 ∿ 70	°C	1
Storage Temperature	T_{STG}	-55 ∿ 125	°C	1
Soldering Temperature . Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	7.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_c=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	2
V_{IH}	Input High Voltage	2.4	—	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (Vcc=5V ± 5%, Tc=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
ICC1	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: tRC=tRC MIN.)	THM362500S-85 THM362500S-10 THM362500S-12	— — —	960 840 720	mA	3,4
ICC2	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=VIH)		—	36	mA	
ICC3	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=VIH: tRC=tRC MIN.)	THM362500S-85 THM362500S-10 THM362500S-12	— — —	960 840 720	mA	3
ICC4	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=VIL, $\overline{CAS}$ Address Cycling: tPC=tPC MIN.)	THM362500S-85 THM362500S-10 THM362500S-12	— — —	750 655 560	mA	3,4
ICC5	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=VCC-0.2V)		—	28	mA	
ICC6	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: tRC=tRC MIN.)	THM362500S-85 THM362500S-10 THM362500S-12	— — —	960 840 720	mA	3
II(L)	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≦ VIN ≦ 6.5V, All Other Pins not under Test=0V)		-10	10	μA	
IO(L)	OUTPUT LEAKAGE CURRENT (DOUT is disabled, 0V ≦ VOUT ≦ 5.25V)		-10	10	μA	
VOH	OUTPUT LEVEL Output "H" Level Voltage (IOUT=-5mA)		2.4	—	V	
VOL	OUTPUT LEVEL Output "L" Level Voltage (IOUT=4.2mA)		—	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(VCC=5V ± 5%, Tc=0 ~ 70°C) (Notes 5,6,7)

SYMBOL	PARAMETER	THM362500S-85		THM362500S-10		THM362500S-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
tRC	Random Read or Write Cycle Time	165	—	190	—	220	—	ns	
tPC	Fast Page Mode Cycle Time	70	—	85	—	105	—	ns	
tRAC	Access Time from $\overline{RAS}$	—	85	—	100	—	120	ns	8,13
tCAC	Access Time from $\overline{CAS}$	—	40	—	50	—	60	ns	8,13
tAA	Access Time from Column Address	—	45	—	50	—	60	ns	8,14
tCPA	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	65	ns	8
tCLZ	$\overline{CAS}$ to Output in Low-Z	5	—	5	—	5	—	ns	8
tOFF	Output Buffer Turn-off Delay	0	25	0	25	0	30	ns	9
tT	Transition Time (Rise and Fall)	3	30	3	30	3	30	ns	7
tRP	$\overline{RAS}$ Precharge Time	70	—	80	—	90	—	ns	
tRAS	$\overline{RAS}$ Pulse Width	85	16,000	100	16,000	120	16,000	ns	
tRASP	$\overline{RAS}$ Pulse width (Fast Page Mode)	85	100,000	100	100,000	120	100,000	ns	
tRSH	$\overline{RAS}$ Hold Time	40	—	50	—	60	—	ns	
tCSH	$\overline{CAS}$ Hold Time	85	—	100	—	120	—	ns	
tCAS	$\overline{CAS}$ Pulse Width	40	10,000	50	10,000	60	10,000	ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	45	25	50	25	60	ns	13
tRAD	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	20	60	ns	14
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
tCP	$\overline{CAS}$ Precharge Time (Fast Page Mode)	20	—	25	—	35	—	ns	
tASR	Row Address Set-Up Time	0	—	0	—	0	—	ns	
tRAH	Row Address Hold Time	15	—	15	—	15	—	ns	
tASH	Column Address Set-Up Time	0	—	0	—	0	—	ns	
tCAH	Column Address Hold Time	20	—	20	—	25	—	ns	
tAR	Column Address Hold Time referenced to $\overline{RAS}$	65	—	75	—	90	—	ns	
tRAL	Column Address to $\overline{RAS}$ Lead Time	45	—	50	—	60	—	ns	
tRCS	Read Command Set-Up time	0	—	0	—	0	—	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM362500S-85		THM362500S-10		THM362500S-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10	-	10	-	15	-	ns	10
t_{WCH}	Write Command Hold Time	20	-	20	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{WP}	Write Command Pulse Width	20	-	20	-	25	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	25	-	30	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	20	-	20	-	25	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	65	-	75	-	90	-	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	50	-	50	-	60	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	15	-	15	-	20	-	ns	

CAPACITANCE (VCC=5V ± 5%, f=1MHz, Tc=0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ~ A8)	—	88	pF
CI2	Input Capacitance ($\overline{W}$)	—	84	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	—	42	pF
CI4	Input Capacitance ($\overline{CAS0}$ ~ $\overline{CAS3}$)	—	36	pF
CDQ1	I/O Capacitance (DQ0 ~ 7,9 ~ 16,18 ~ 25,27 ~ 34)	—	17	pF
CDQ2	I/O Capacitance (DQ8,17,26,35)	—	22	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2. All voltages are referenced to V_{SS}.

3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.

4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.

5. An initial pause of 200us is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6. AC measurements assume t_T=5ns.

7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8. Measured with a load equivalent to 2 TTL loads and 100pF.

9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

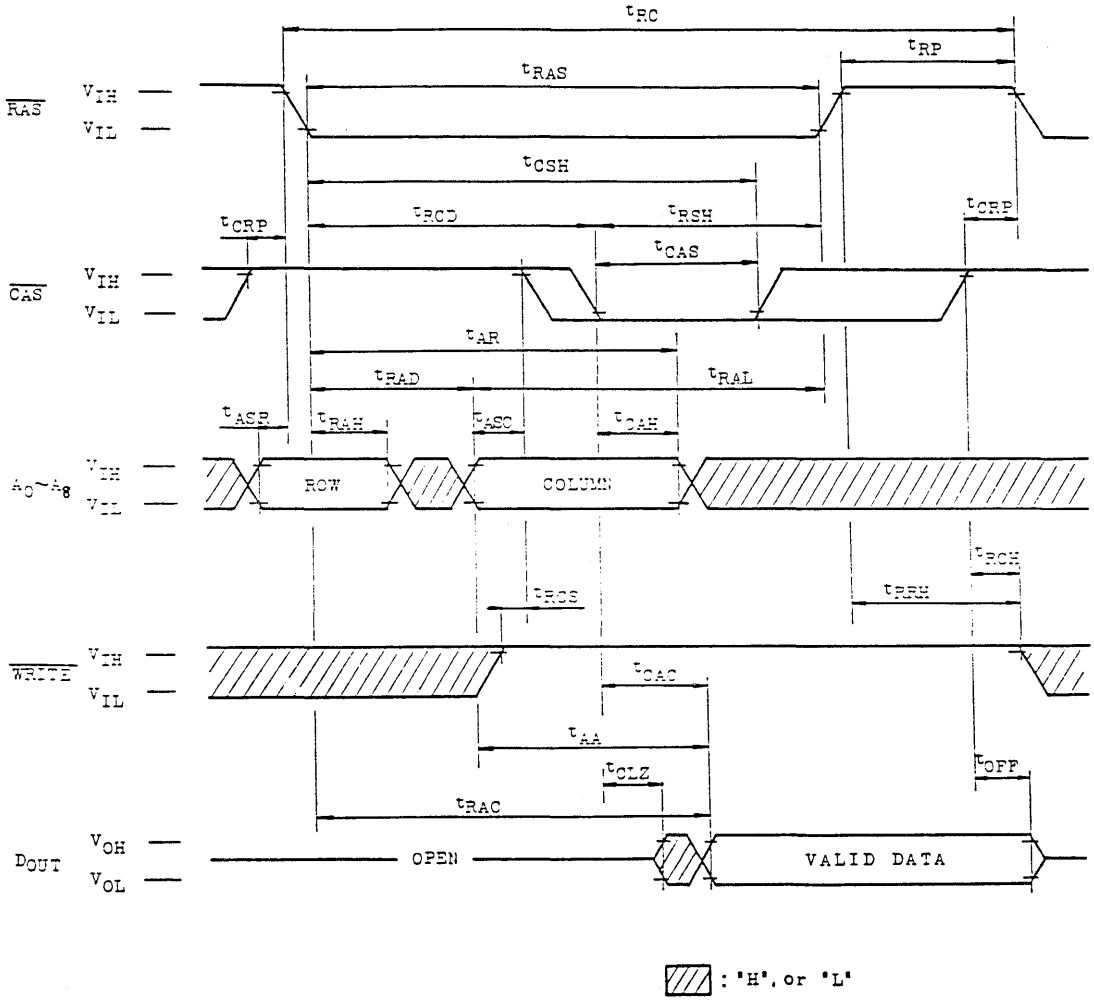
11. These parameters are referenced to $\overline{CAS}$ leading edge.

12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).

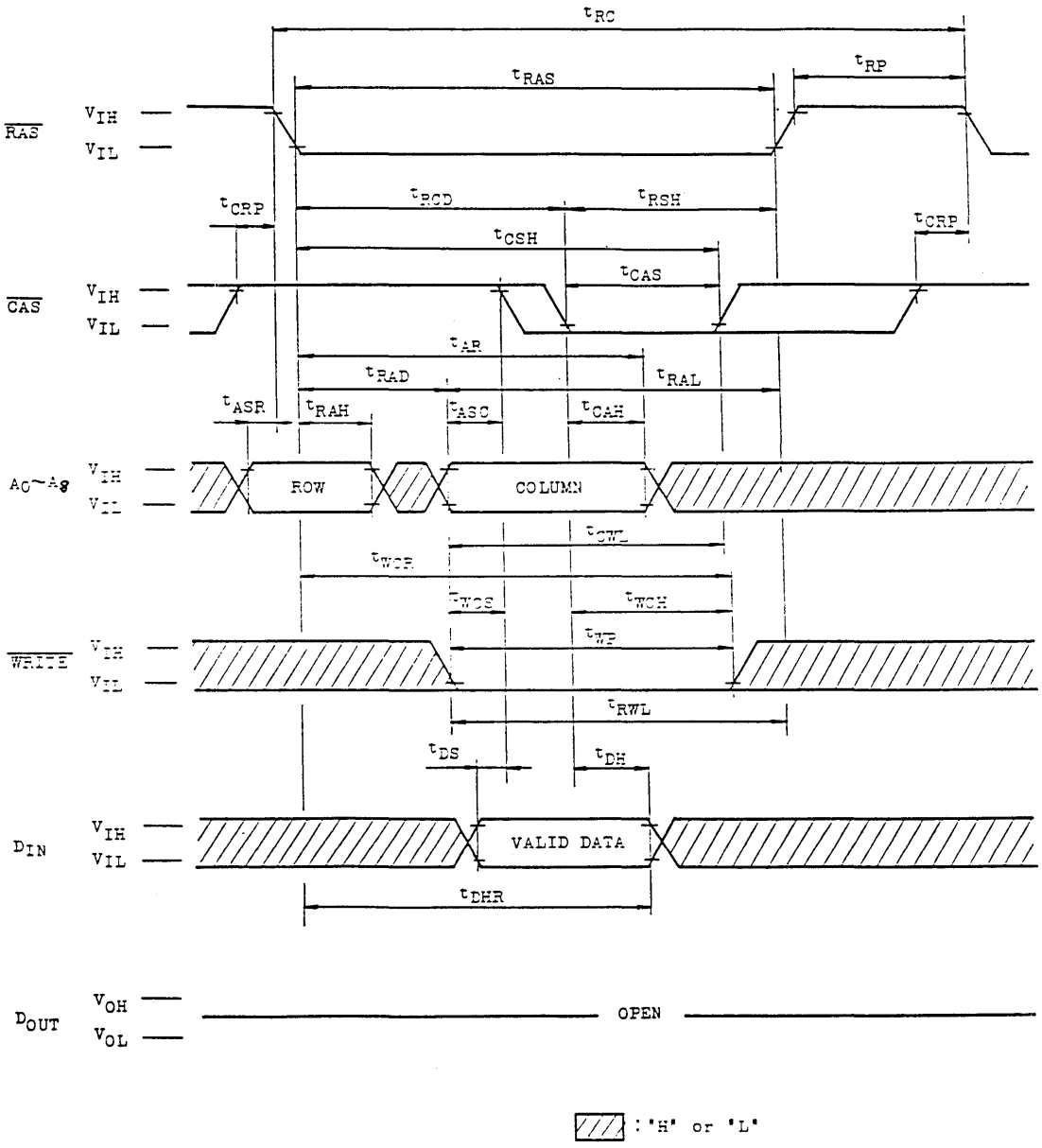
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.

14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

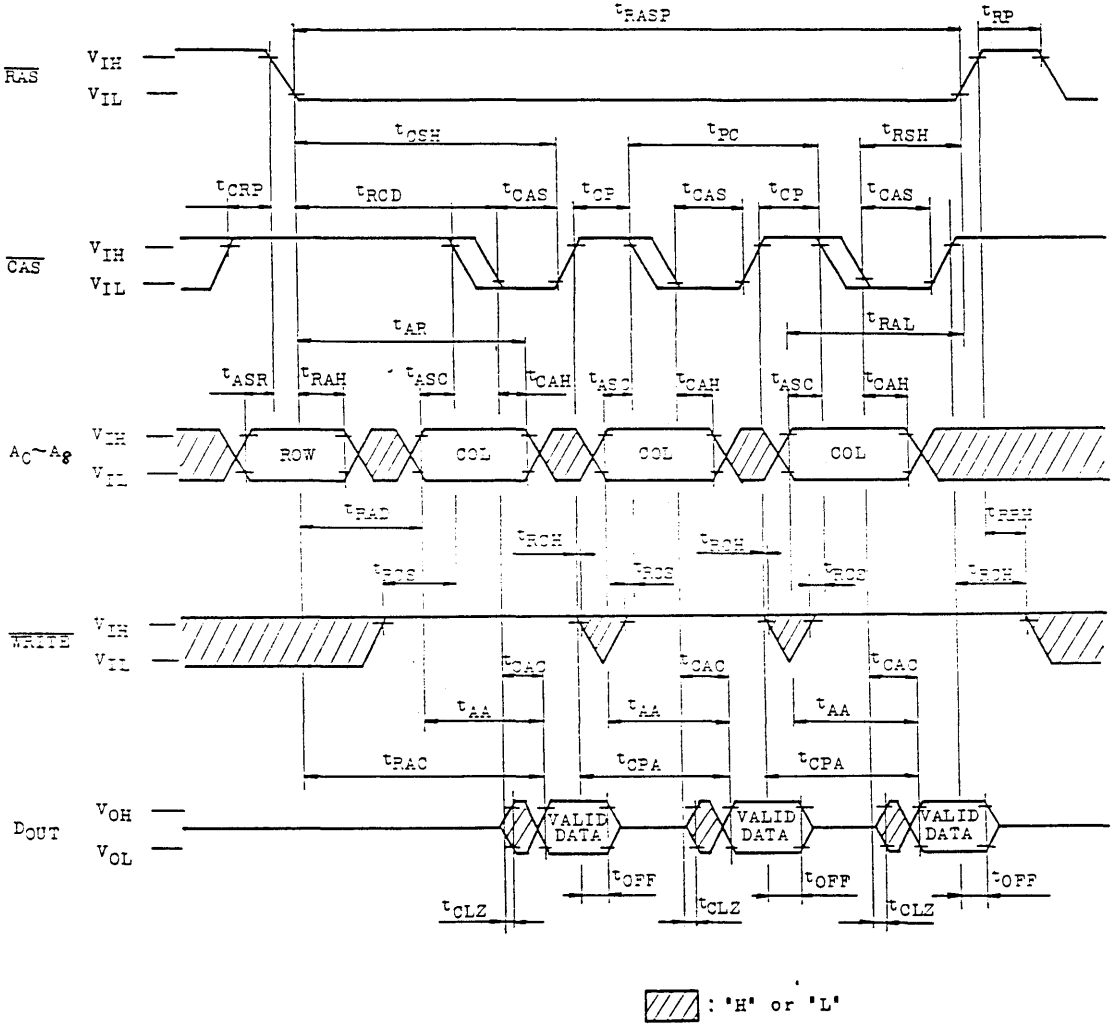
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
tCAS
CAS
VIH
VIL
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A8
VIH
VIL
ROW
COLUMN
tRCH
tRCS
tRRH
WRITE
VIH
VIL
tCAC
tAA
tOFF
tCLZ
tRAC
DOUT
VOH
VOL
OPEN
VALID DATA
: "H", or "L"

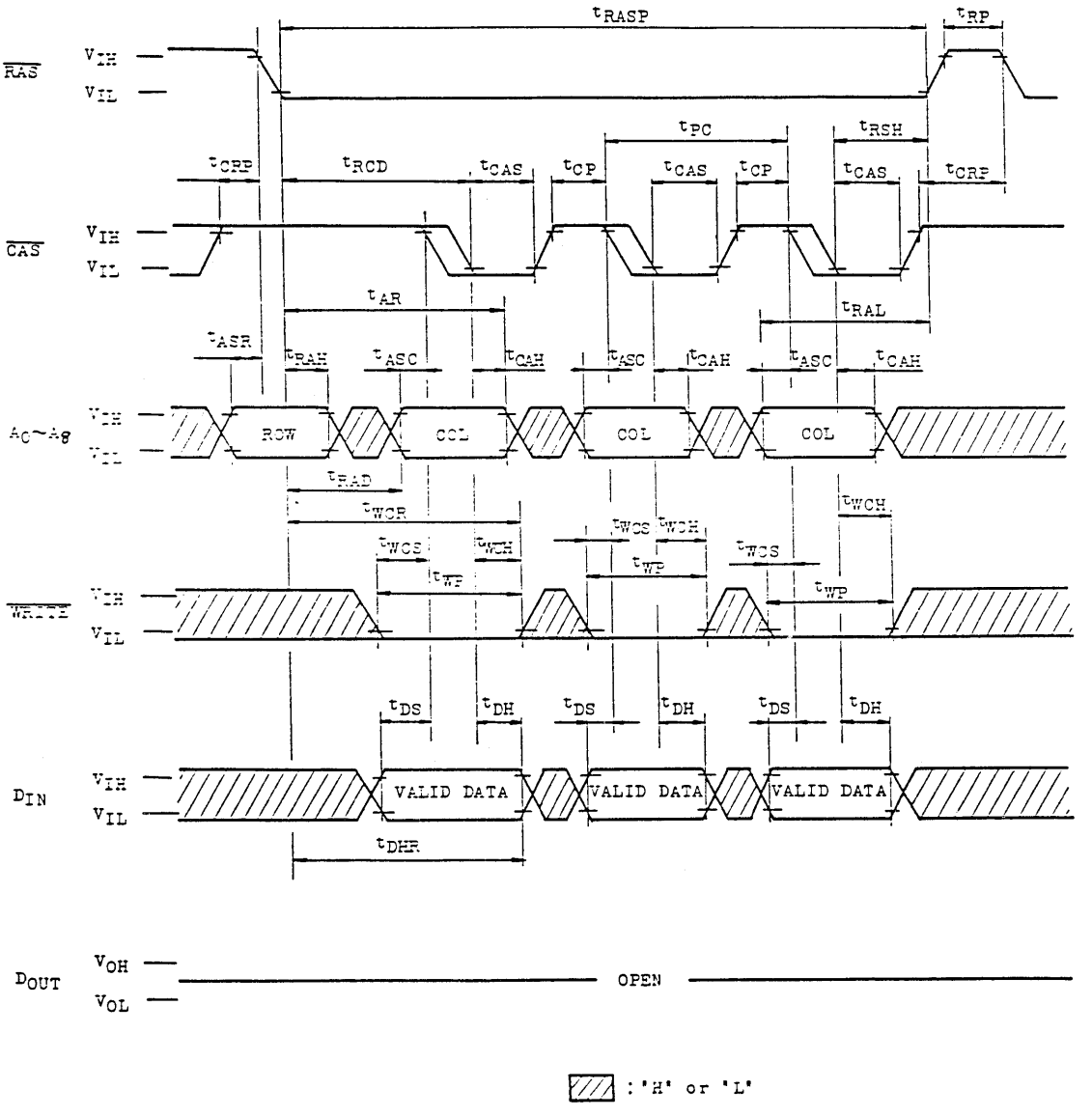
EARLY WRITE CYCLE



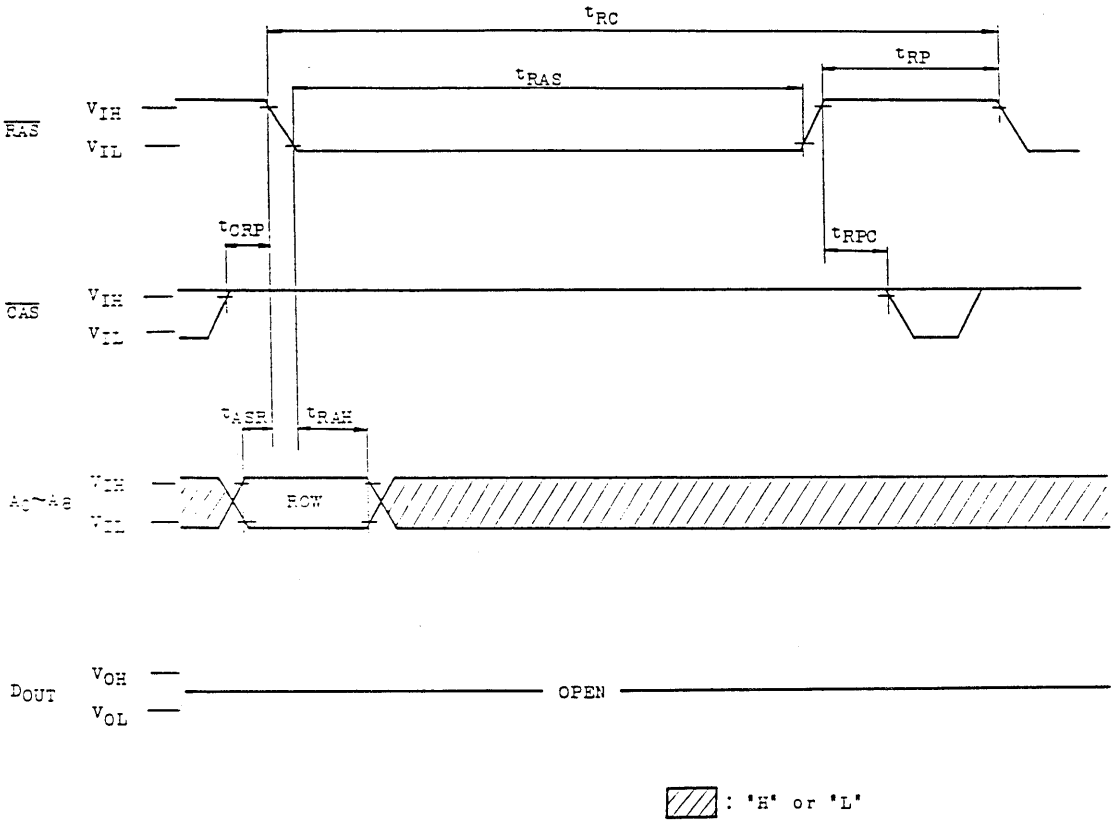
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

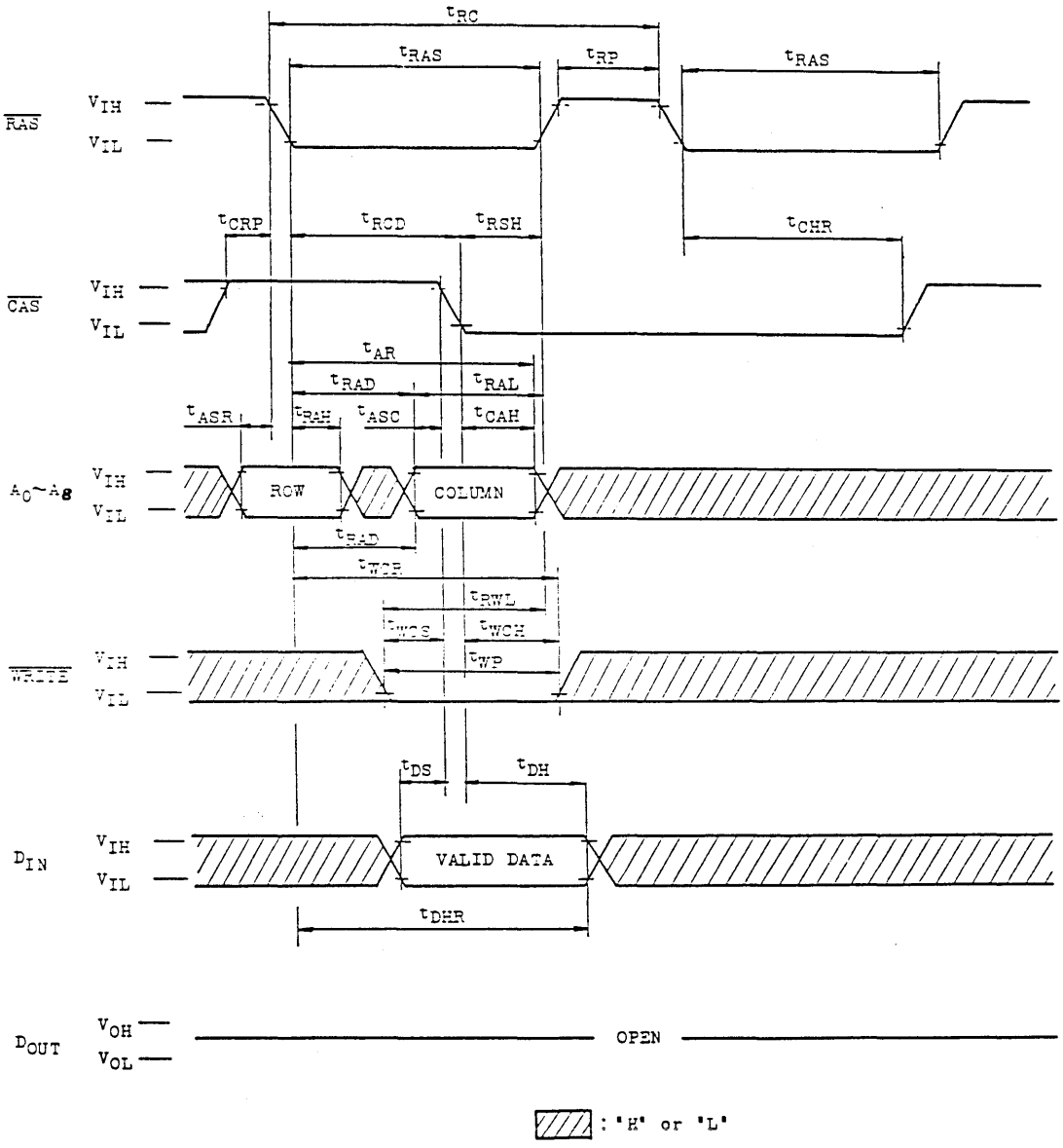


$\overline{RAS}$ ONLY REFRESH CYCLE

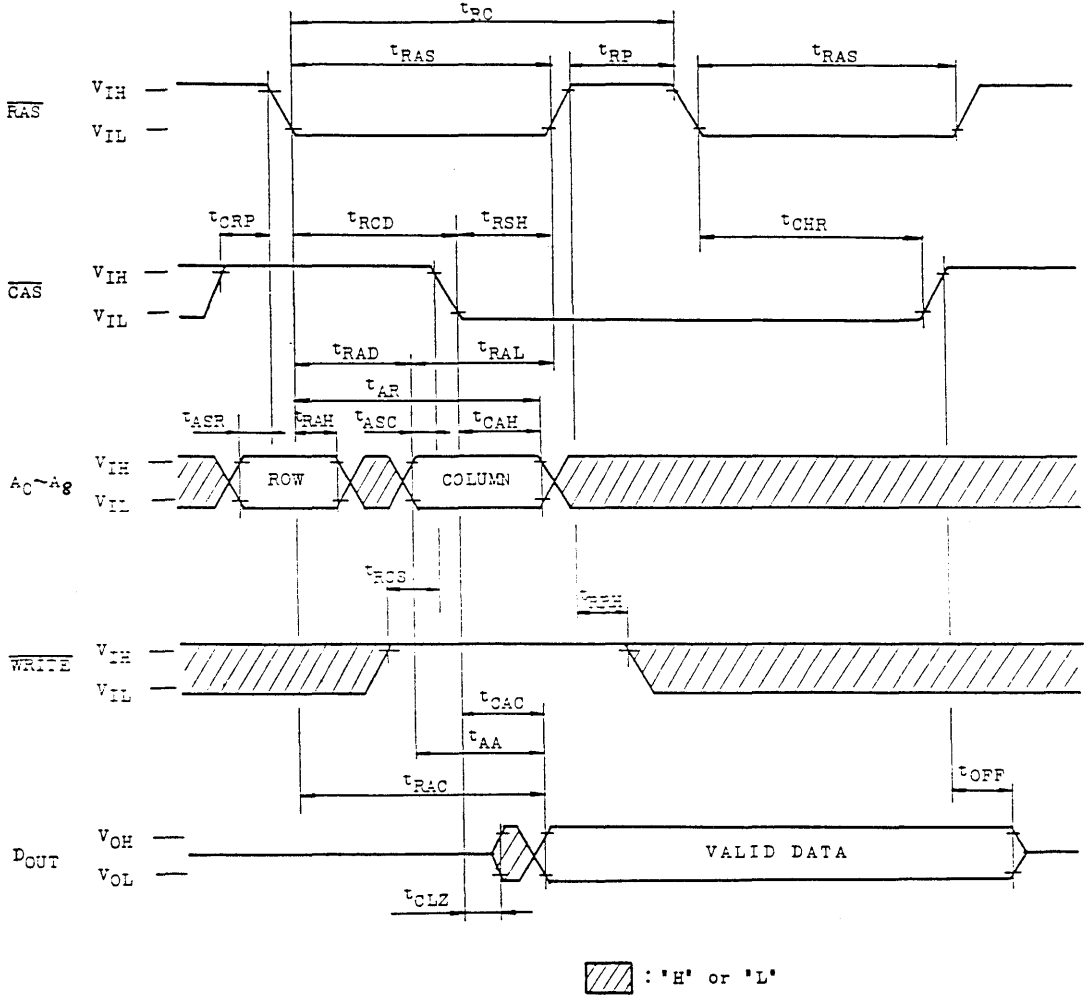


Note: $\overline{WRITE}$="H" or "L"

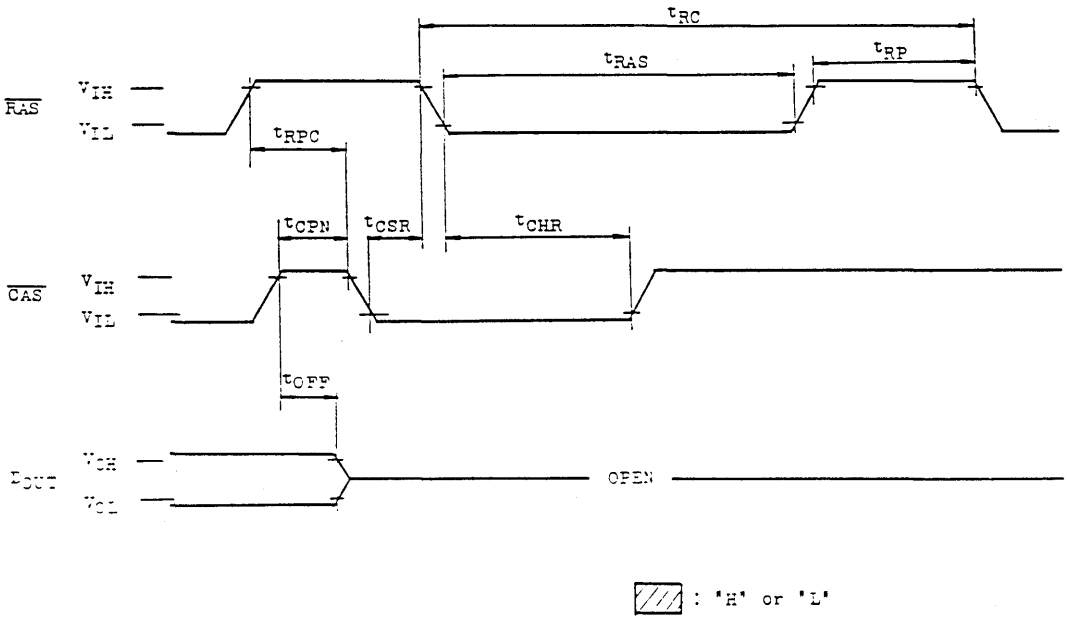
HIDDEN REFRESH CYCLE (WRITE)



HIDDEN REFRESH CYCLE (READ)

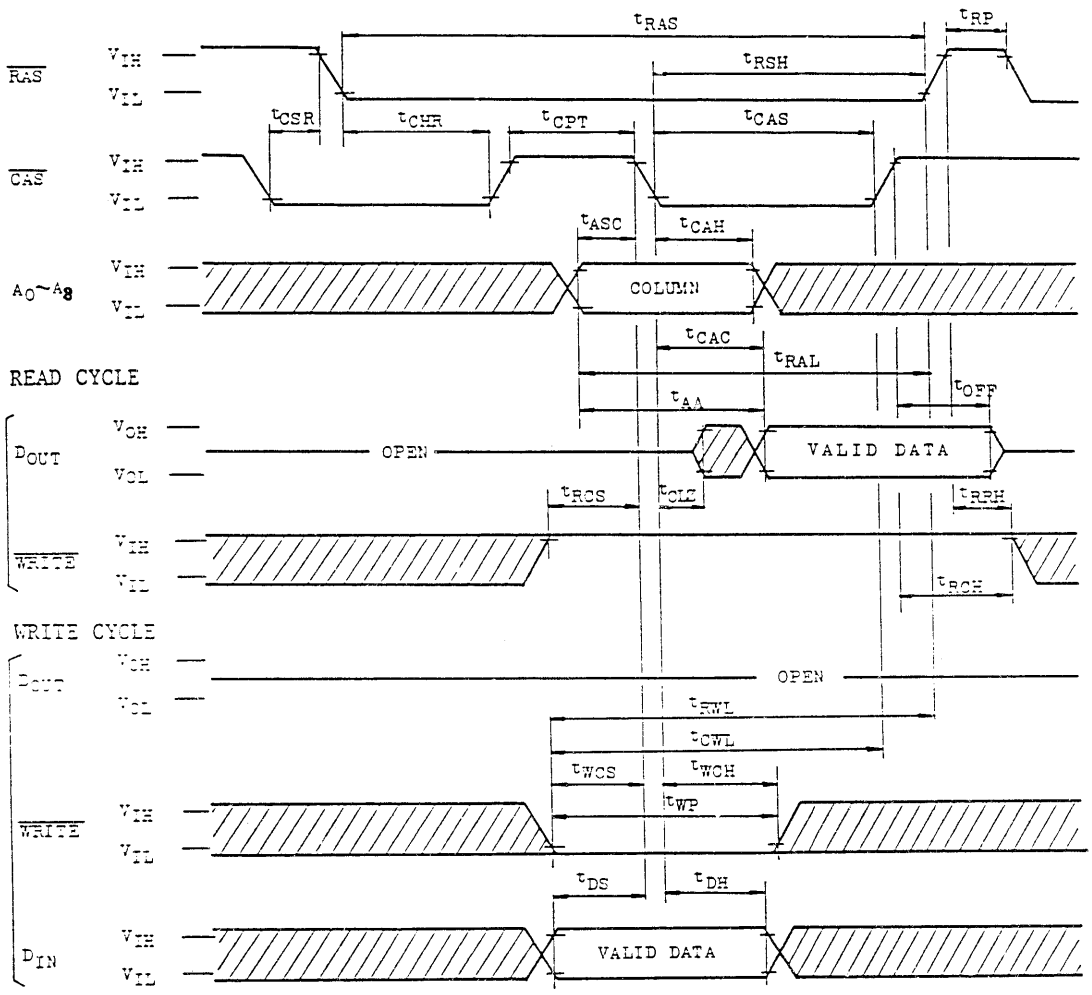


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WRITE}$="H" or "L", A0 ∿ A8="H" or "L"

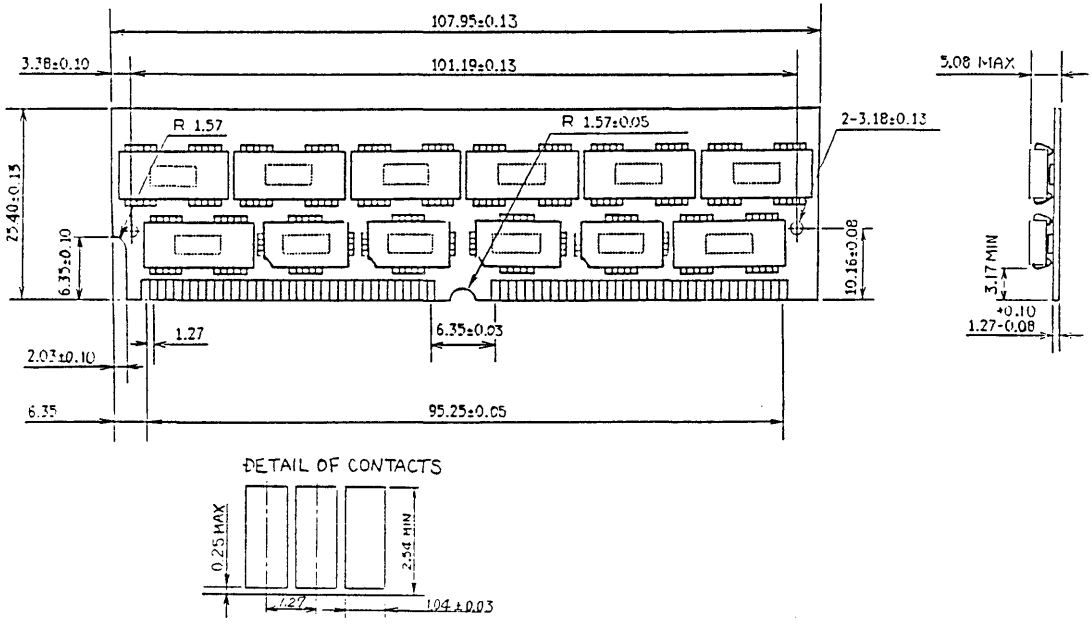
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

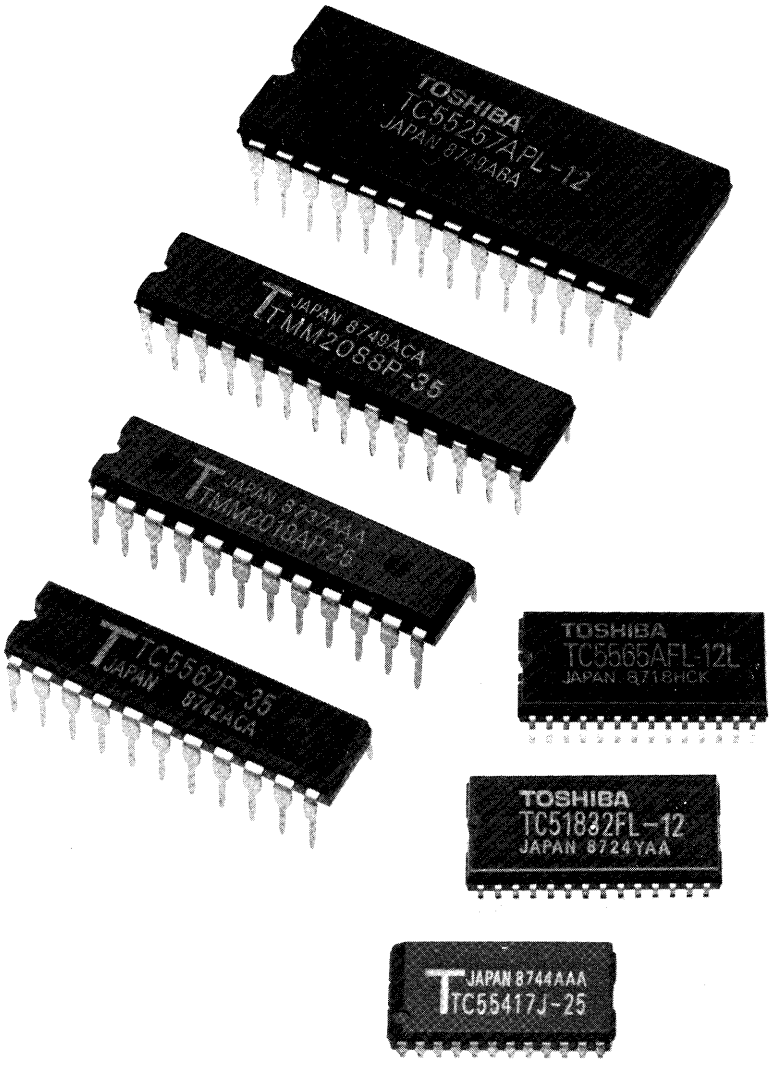


OUTLINE DRAWINGS

• THM362500S

Unit in mm




TOSHIBA
TC55257APL-12
JAPAN 8718A6A
JAPAN 8749ACA
TMM2088P-35
JAPAN 8737AAA
TMM2016AP-25
TC5562P-35
JAPAN 8742ACA
TOSHIBA
TC5565AFL-12L
JAPAN 8718HCK
TOSHIBA
TC51832FL-12
JAPAN 8724YAA
JAPAN 8744AAA
TC55417J-25

Static RAMs

Standard SRAM

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2063P-10, TMM2063P-12 TMM2063P-15

DESCRIPTION

The TMM2063P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2063P is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063P is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

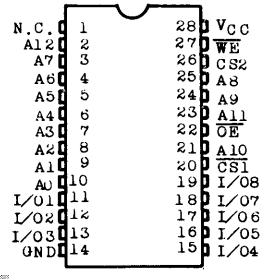
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063P-10	100ns	80mA	10mA
TMM2063P-12	120ns	80mA	10mA
TMM2063P-15	150ns	80mA	10mA

- High Density Assembly Capability : 0.3 inch width package (28 pin plastic DIP)
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$, CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge

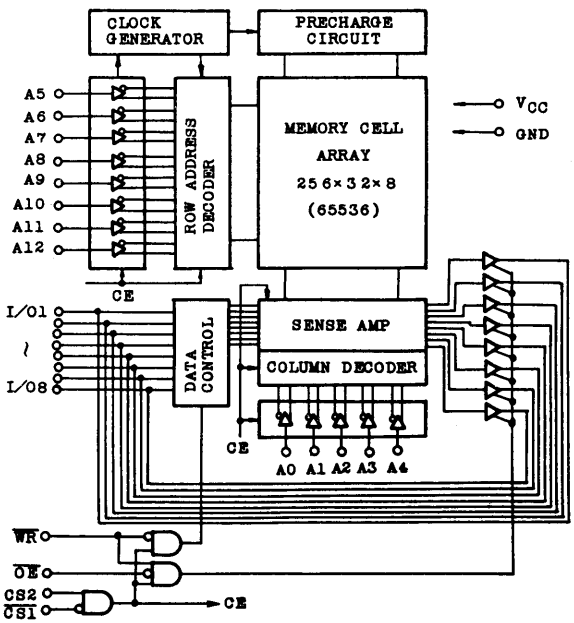
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_4$	Column Address Inputs
$A_5 \sim A_{12}$	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	0.8	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

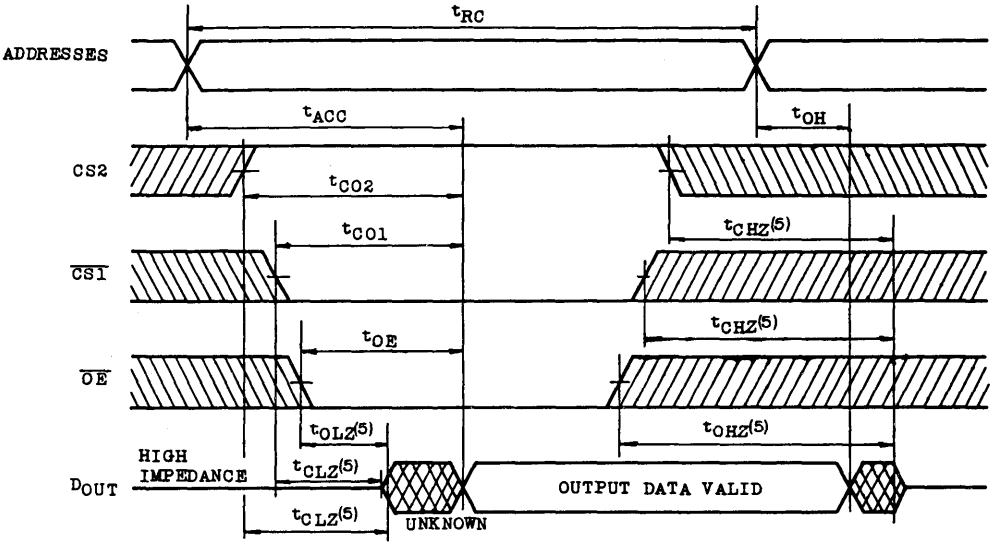
SYMBOL	PARAMETER	TMM2063P-10		TMM2063P-12		TMM2063P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

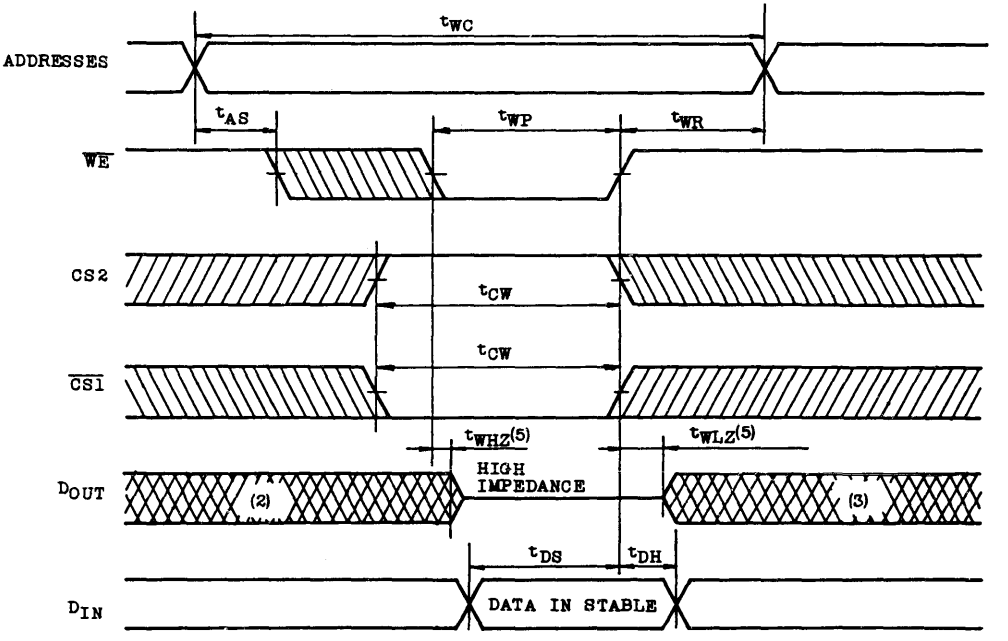
Input Pulse Levels	V_{IH}=2.2V, V_{IL}=0.6V
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & C_L=100pF

TIMING WAVEFORMS

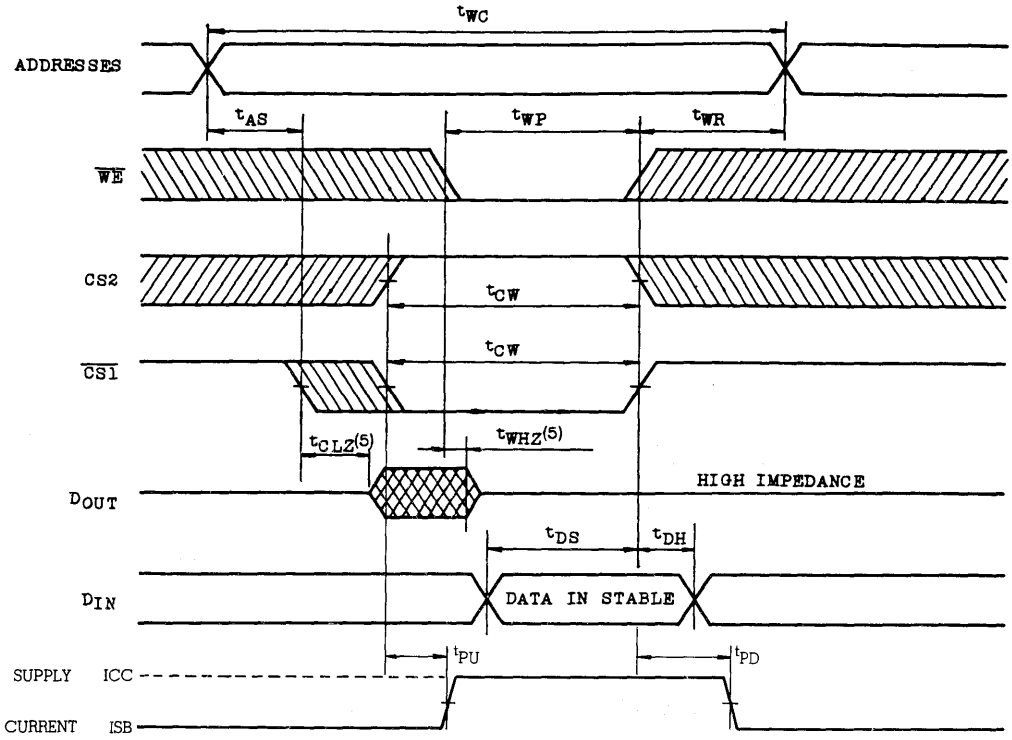
- READ CYCLE (1)



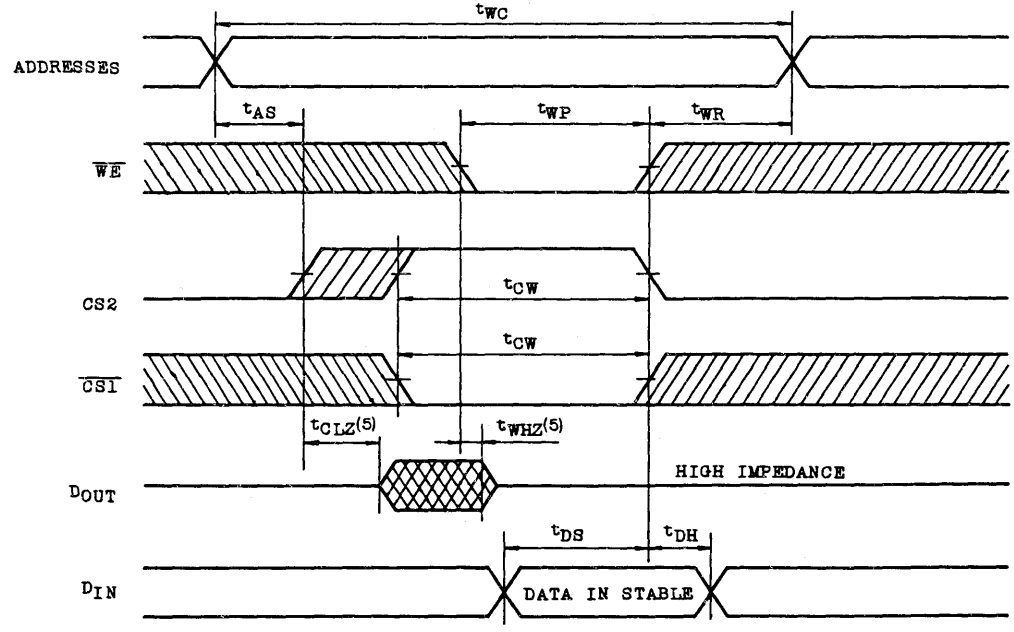
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

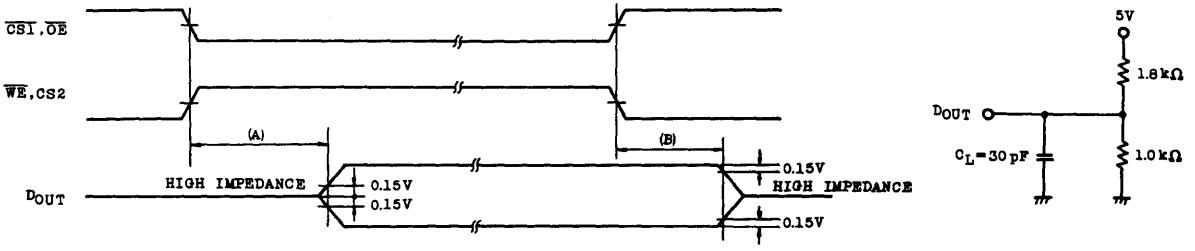
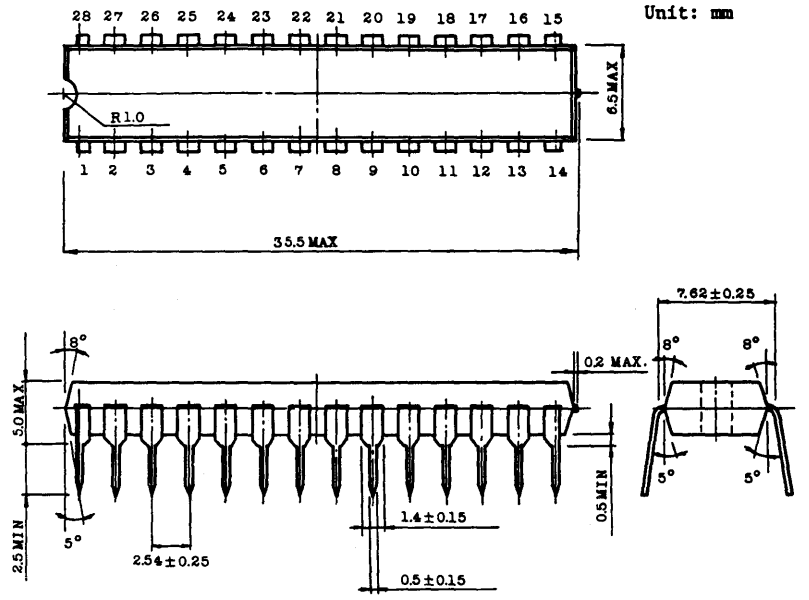


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TMM2063AP-70, TMM2063AP-10
TMM2063AP-12

DESCRIPTION

The TMM2063AP is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 70ns/100ns/120ns and maximum operating current of 80mA. When $\overline{CS1}$ is logical high or CS2 is a logical low, the device is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2063AP is most suitable for use in microcomputer peripheral memory where the low power applications are required, moreover, suitable for use in high density assembly as 0.3 inch width package is use for. The TMM2063AP is fabricated with ion implanted N channel silicon gate MOS technology for high preformance and high reliability.

FEATURES

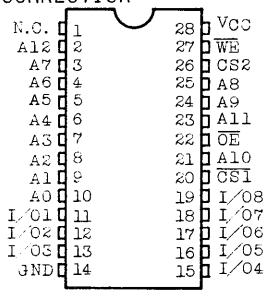
- Access Time and Current

Parameter / Part Number	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2063AP-70	70ns	80mA	10mA
TMM2063AP-10	100ns	80mA	10mA
TMM2063AP-12	120ns	80mA	10mA

- High Density Assembly Capability:
  0.3 inch width package
  (28 pins plastic DIP)

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: $\overline{CS1}$, CS2
- Output Buffer Control: $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs: Directly TTL Compatible
- Inputs Protected: All inputs have protection against static charge.

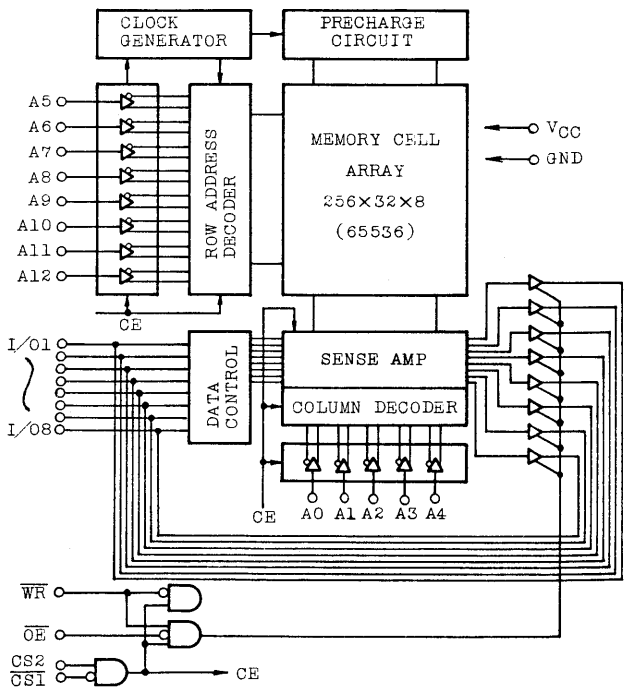
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
A0 ∿ A4	Column Address Inputs
A5 ∿ A12	Row Address Inputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
I/O1 ∿ I/O8	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXUMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-0.5*1 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	0.8	W

*1 -3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITION (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.5*2	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

*2 -3.0V at pulse width 50ns

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-10	-	10	μA
V_{OH}	Output High Voltage	I_{OUT}=-1.0mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OUT}=4.0mA	-	-	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V ∿ 5.5V	-10	-	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	-	20	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}, I_{OUT}=0mA	-	-	10	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, CS2=V_{IH}, I_{OUT}=0mA	-	-	80	mA

CAPACITANCE * (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TMM2063AP-70		TMM2063AP-10		TMM2063AP-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	70	-	100	-	120	-	ns
t_{ACC}	Address Access Time	-	70	-	100	-	120	
t_{CO1}	$\overline{CS1}$ Access Time	-	70	-	100	-	120	
t_{CO2}	$\overline{CS2}$ Access Time	-	70	-	100	-	120	
t_{OE}	$\overline{OE}$ Access Time	-	35	-	40	-	50	
t_{OH}	Output Data Hold Time from Address Change	5	-	10	-	10	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	10	-	10	-	10	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2.	-	30	-	40	-	40	
t_{OLZ}	Output Enable Time from $\overline{OE}$	5	-	5	-	5	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	30	-	35	-	35	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	40	-	50	-	60	

WRITE CYCLE

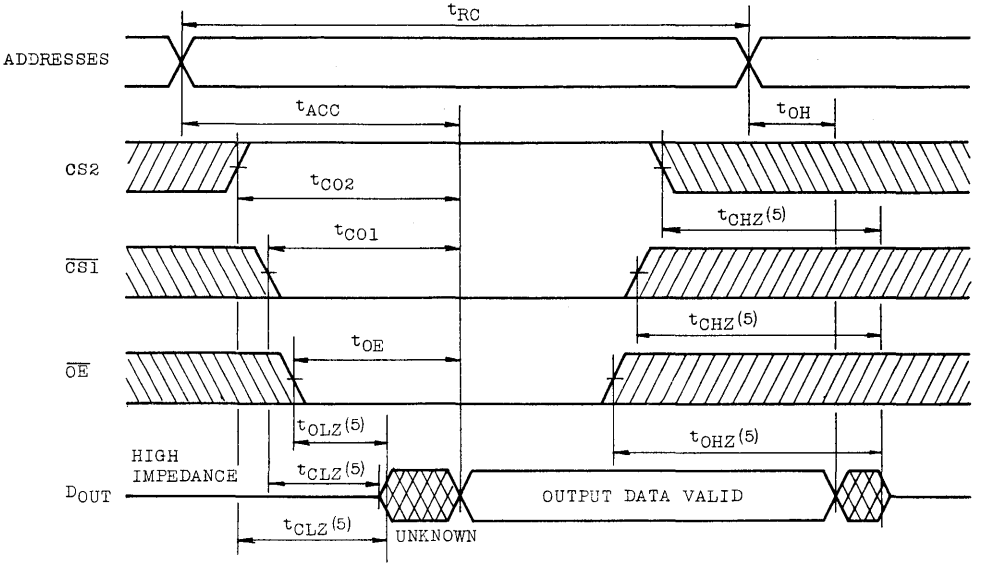
SYMBOL	PARAMETER	TMM2063AP-70		TMM2063AP-10		TMM2063AP-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	-	100	-	120	-	ns
t_{CW}	Chip Selection to End of Write	60	-	80	-	100	-	
t_{AS}	Address Set Up Time	10	-	10	-	10	-	
t_{WP}	Write Pulse Width	50	-	70	-	85	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	30	-	40	-	50	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	5	-	5	-	5	-	
t_{WHZ}	Output Disable Time from $\overline{WE}$	-	25	-	30	-	35	

A.C. TEST CONDITIONS

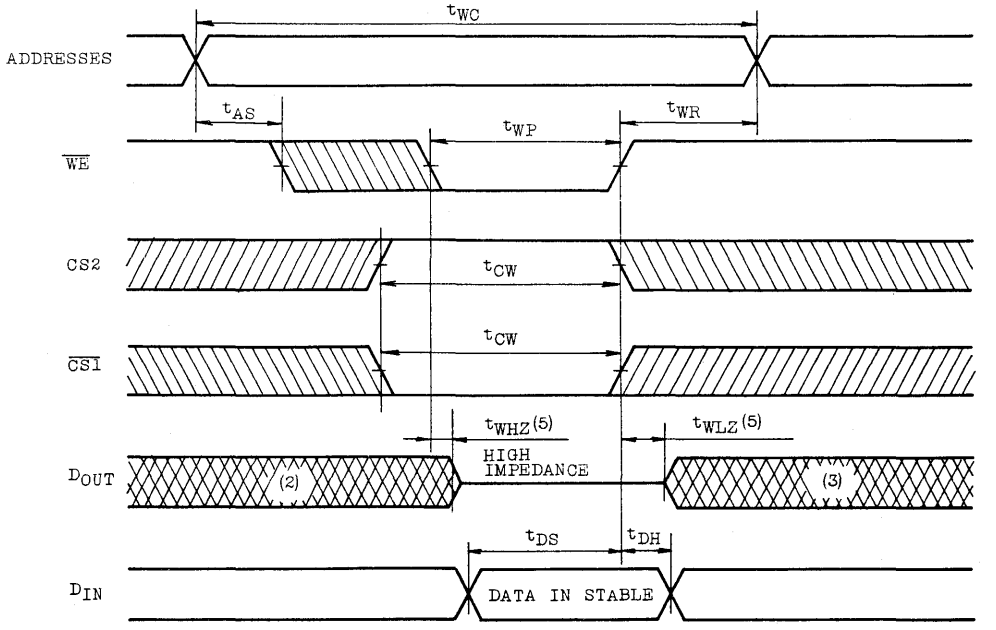
Input Pulse Levels	$V_{IH}=2.2V$, $V_{IL}=0.6V$
Input Rise and Fall Time	5NS
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L=100pF$

TIMING WAVEFORMS

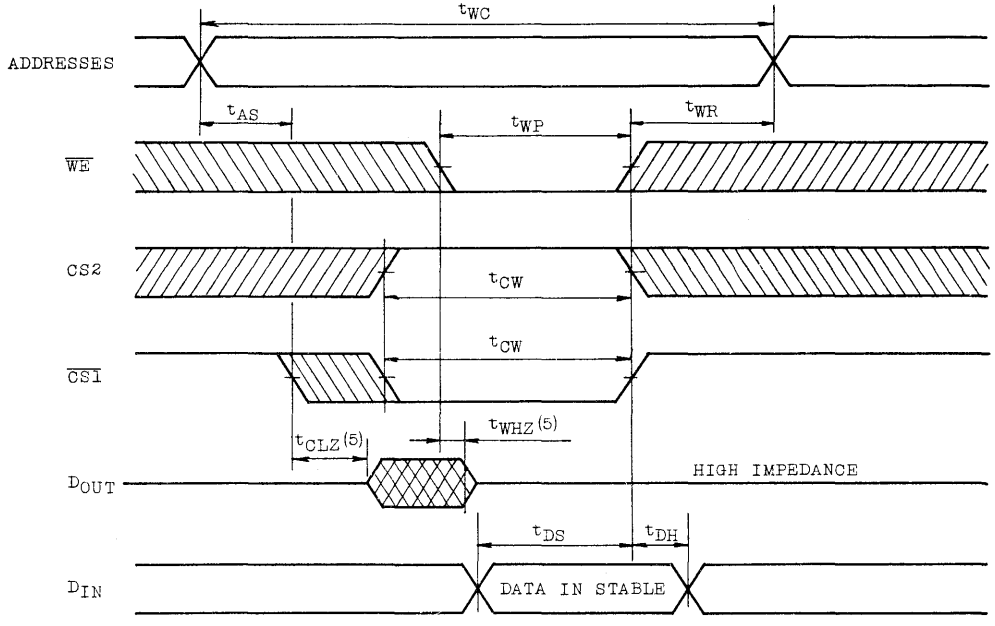
READ CYCLE (1)



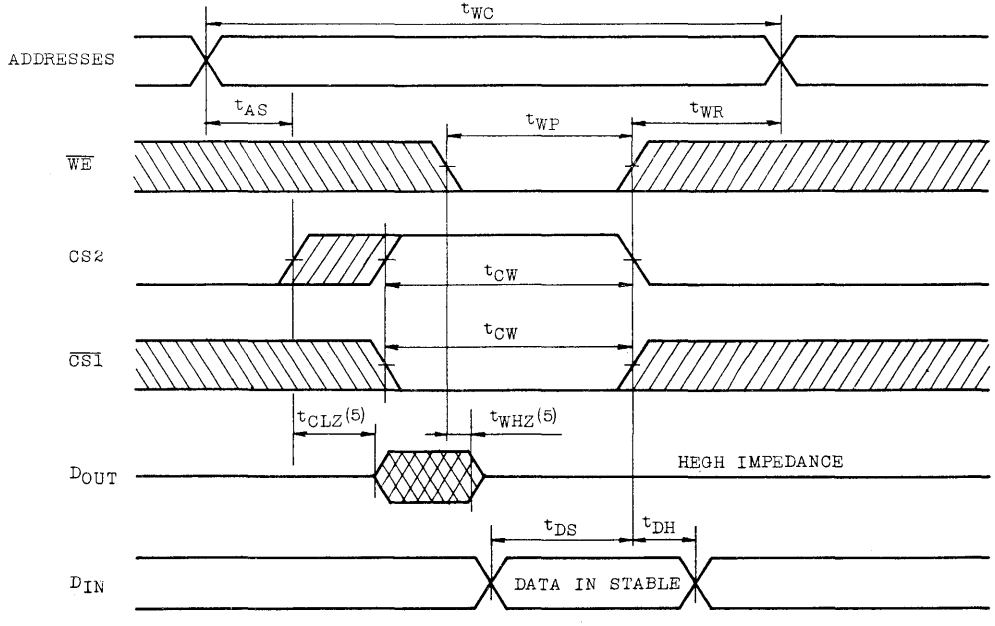
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

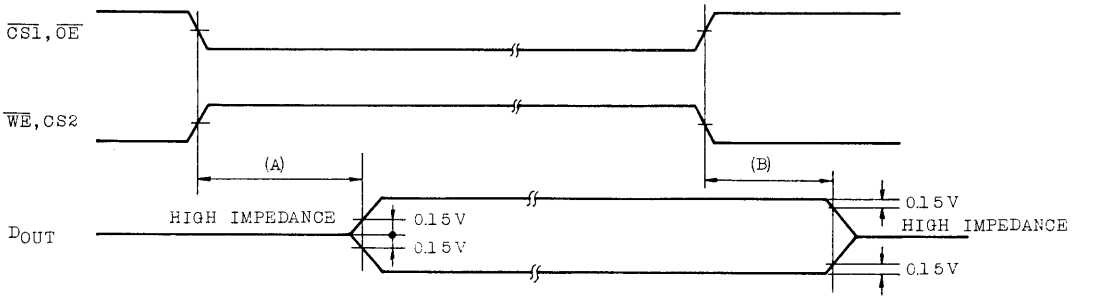
3. Assuming that $\overline{CE1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



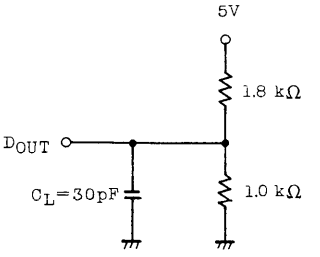
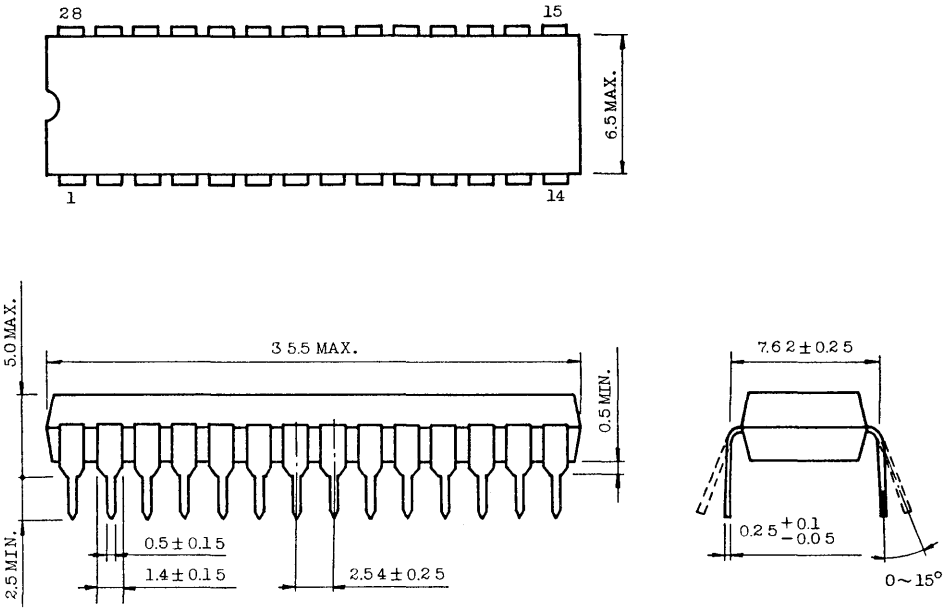


Fig.1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



Note: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2064P-10, TMM2064P-12 TMM2064P-15

DESCRIPTION

The TMM2064P is a 65,536 bits high speed and low power static random access memory organized as 8,192 words by 8 bits and operates from a single 5V supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 100ns/120ns/150ns and maximum operating current of 80mA. When $\overline{CS_1}$ is a logical high or CS_2 is a logical low, the deivce is placed in a low power standby mode in which maximum standby current is 10mA. Thus the TMM2064P is most suitable for use in microcomputer peripheral memory where the low power applications are required. The TMM2064P is fabricated with ion implanted N channel silicon gate MOS technology for high perfomance and high reliability.

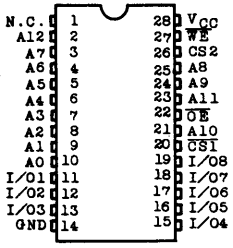
FEATURES

- Access Time and Current

Part Number \ Parameter	Access Time (Max.)	Operating Current (Max.)	Standby Current (Max.)
TMM2064P-10	100ns	80mA	10mA
TMM2064P-12	120ns	80mA	10mA
TMM2064P-15	150ns	80mA	10mA

- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature : $\overline{CS_1}$ CS_2
- Output Buffer Control : $\overline{OE}$
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Inputs Protected : All inputs have protection against static charge.

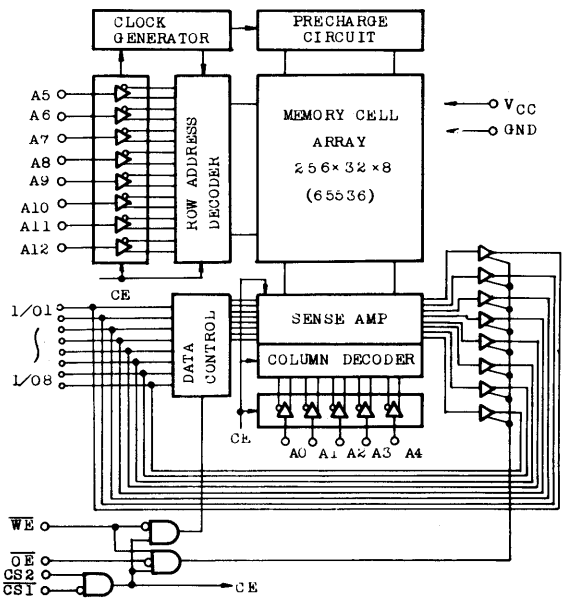
PIN CONNECTION



PIN NAMES

SYMBOL	NAME
$A_0 \sim A_4$	Column Address Inputs
$A_5 \sim A_{12}$	Row Address Inputs
$\overline{CS_1}$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$I/O_1 \sim I/O_8$	Data Input/Output
$\overline{OE}$	Output Enable Input
V_{CC}	Power (5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.5~7.0	V
V_{IN}, V_{OUT}	Input/Output Voltage	−0.5*~7.0	V
T_{OPR}	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−55~150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

* −3.0V at Pulse width 50ns

D. C. RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5**	—	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

** −3.0V at Pulse width 50ns

D. C. CHARACTERISTICS (Ta=0~70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V~5.5V	−10	—	10	μA
V_{OH}	Output High Voltage	I_{OUT}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OUT}=2.1mA	—	—	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V~5.5V	−10	—	10	μA
I_{SBP}	Peak Power-on Current	$\overline{CS_1}$=V_{CC}, CS_2=0V I_{OUT}=0mA	—	—	20	mA
I_{SB}	Standby Current	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL}, I_{OUT}=0mA	—	—	10	mA
I_{CC}	Operating Current	$\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, I_{OUT}=0mA	—	—	80	mA

CAPACITANCE*** (Ta=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

*** Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

($T_a = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CS_1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CS_2 Access Time	—	100	—	120	—	150	
t_{OE}	$\overline{OE}$ Access Time	—	40	—	50	—	60	
t_{OH}	Output Data Hold Time from Address Change	10	—	10	—	10	—	
t_{CLZ}	$\overline{CS_1}$ or CS_2 to Output in Low-Z	10	—	10	—	10	—	
t_{CHZ}	$\overline{CS_1}$ or CS_2 to Output in High-Z	—	40	—	40	—	55	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{OHZ}	$\overline{OE}$ to Output in High-Z	—	35	—	35	—	50	
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	
t_{PD}	Chip Deselection to Power Down Time	—	50	—	60	—	60	

Write Cycle

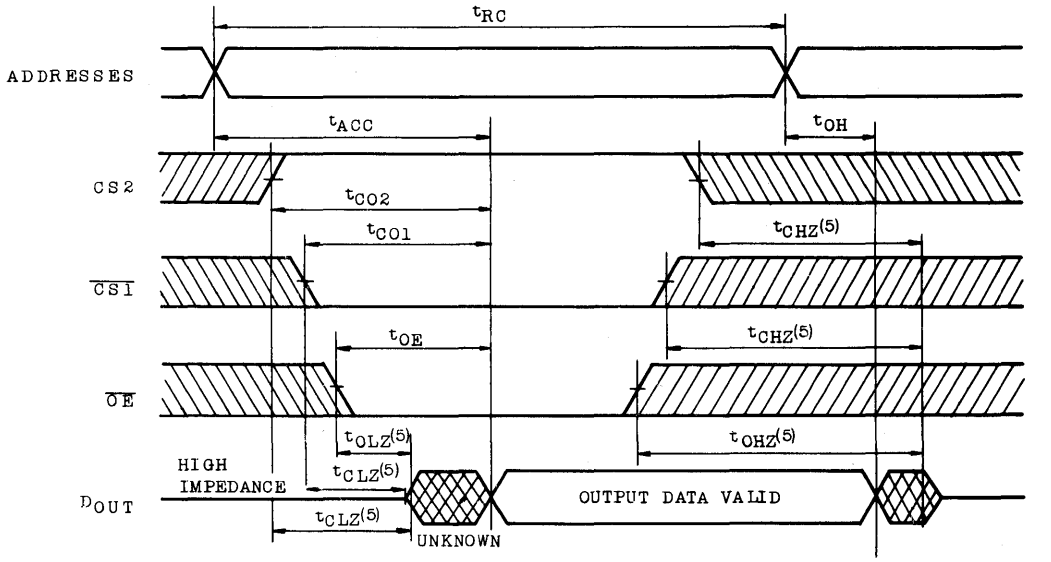
SYMBOL	PARAMETER	TMM2064P-10		TMM2064P-12		TMM2064P-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{CW}	Chip Selection to End of Write	80	—	100	—	120	—	
t_{AS}	Address Set Up Time	10	—	10	—	10	—	
t_{WP}	Write Pulse Width	70	—	85	—	100	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	—	5	—	5	—	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	—	30	—	35	—	40	

A. C. TEST CONDITIONS

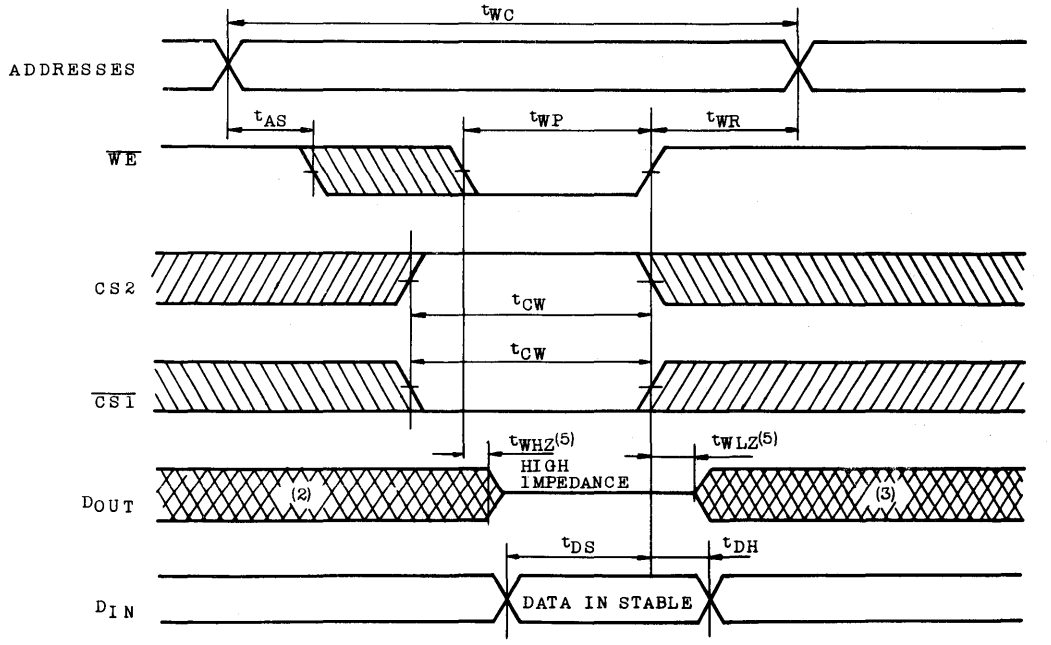
Input Pulse Levels	$V_{IH} = 2.2V$, $V_{IL} = 0.6V$
Input Rise and Fall Time	10ns
Input and Output Reference Levels	1.5V
Output Load	1 TTL Gate & $C_L = 100pF$

TIMING WAVEFORMS

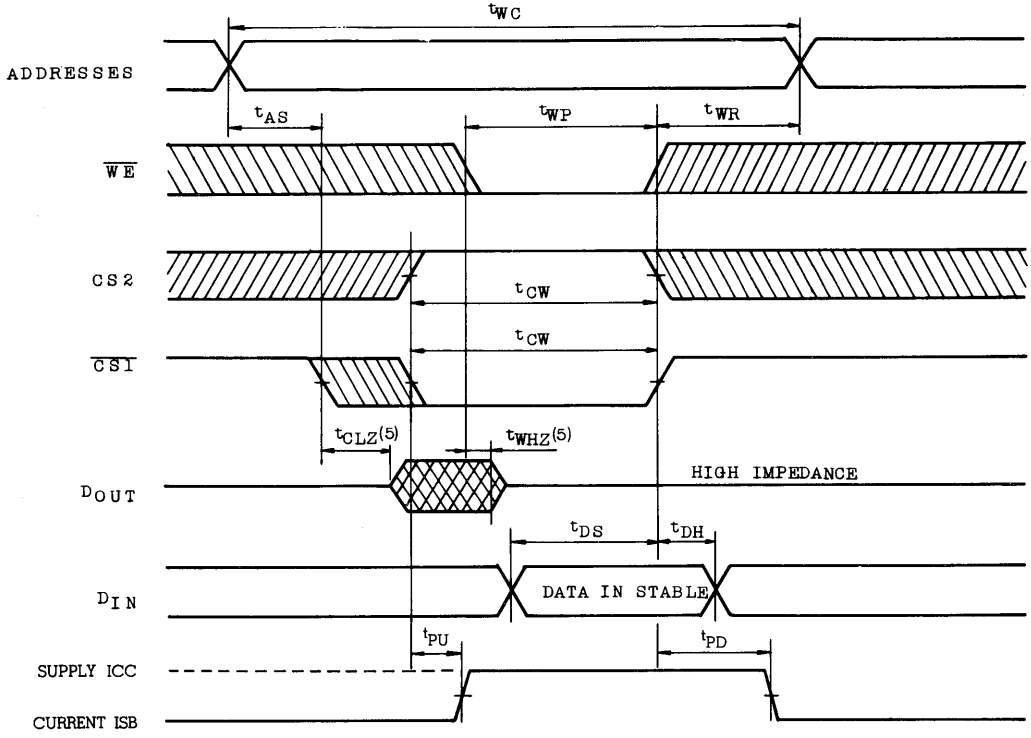
- READ CYCLE (1)



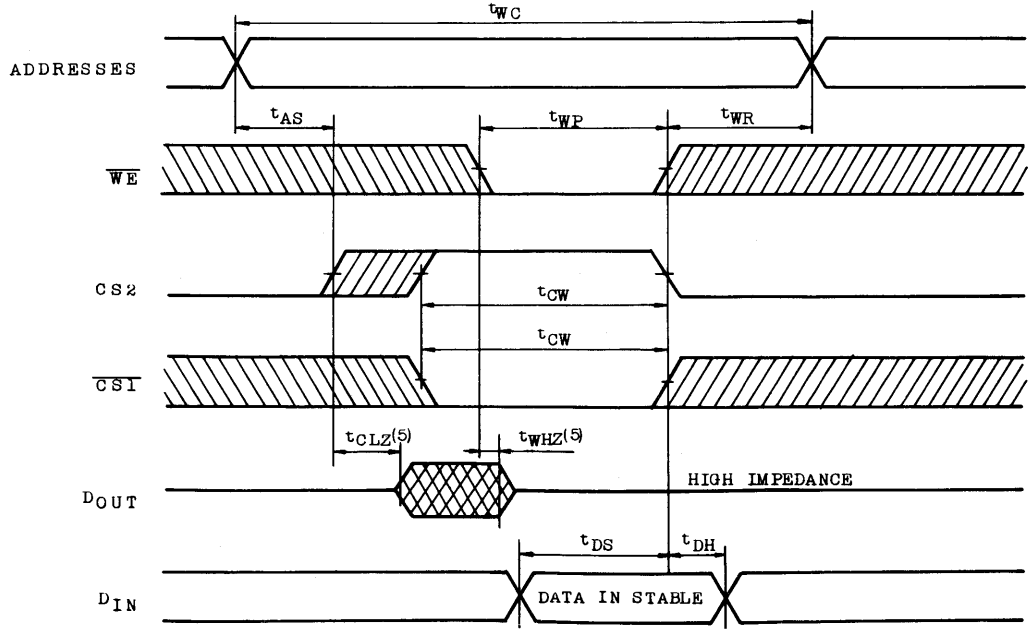
- WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



● WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



● WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS_1}$ Low transition or CS_2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CS_1}$ High transition or CS_2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.
5. These parameters are specified as follows and measured by using the load shown in Fig. 1.
   (A) t_{CLZ}, t_{OLZ}, t_{WLZ}·····Output Enable Time
   (B) t_{CHZ}, t_{OHZ}, t_{WHZ}·····Output Disable Time

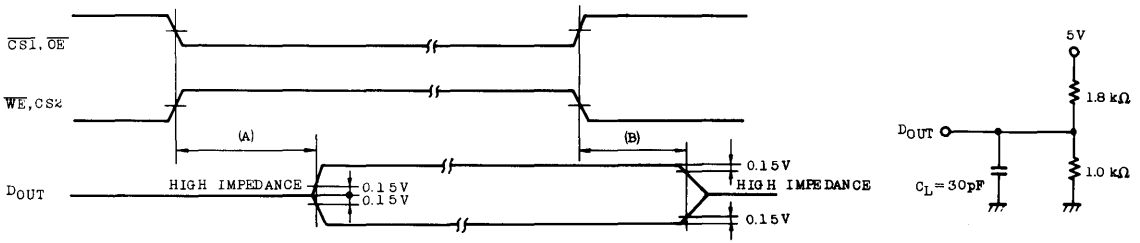
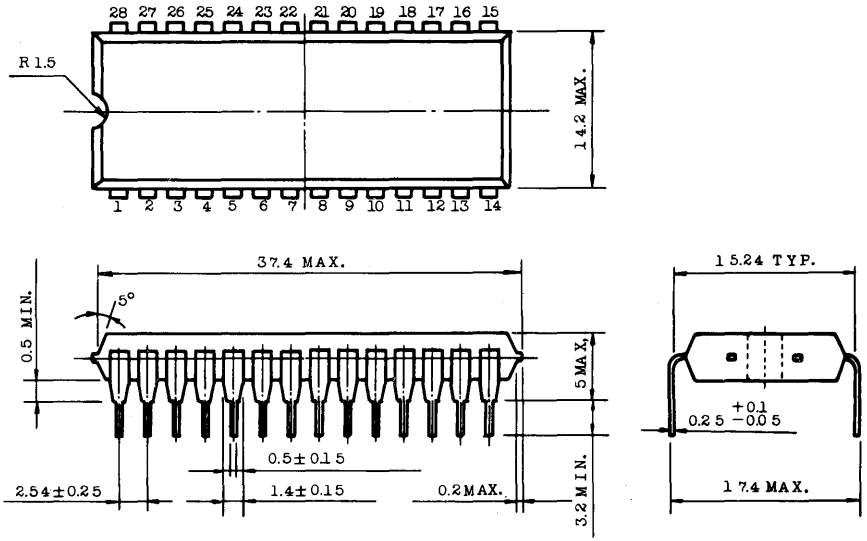


Fig. 1 Output load condition for enable disable time measurement.

OUTLINE DRAWINGS

Unit: mm



NOTES : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM **TC5563APL-10, TC5563APL-12**
SILICON GATE CMOS **TC5563APL-15**

PRELIMINARY

DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

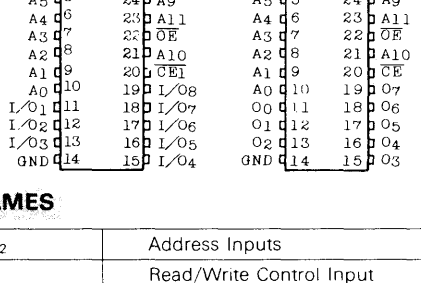
FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 100μA (Max.) Ta=70°C
- Access Time
  TC5563APL-10 : 100ns (Max.)
  TC5563APL-12 : 120ns (Max.)
  TC5563APL-15 : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

*) See TC5565APL Technical Date.

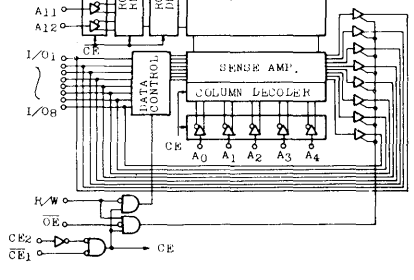
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$		—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		−1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$ or R/W=V_{IL} or $\overline{OE}=V_{IH}$ $V_{OUT}=0\sim V_{DD}$		—	—	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$ Iout=0mA $\overline{CE_1}=V_{IL}$ $CE_2=V_{IH}$ Other Input $=V_{IH}/V_{IL}$	$t_{CYCLE}=1\mu s$	—	—	10	mA
			t_{CYCLE}= Min. cycle	—	—	45	mA
I_{DDO2}	Operating Current	$V_{DD}=5.5V$ $\overline{CE_1}=0.2V$ $CE_2=V_{DD}-0.2V$ Other Input Iout=0mA $=V_{DD}-0.2V/0.2V$	$t_{CYCLE}=1\mu s$	—	—	5	mA
			t_{CYCLE}= Min. cycle	—	—	40	mA
I_{DDS1}	Standby Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}=V_{DD}-0.2V$ or $CE_2=0.2V$ $V_{DD}=2.0\sim5.5V$		—	2	100	μA

* : In standby mode with $\overline{CE_1}\geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2\geqq V_{DD}-0.2V$ or $CE_2\leqq 0.2V$.

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	ns
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	ns
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	ns
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	ns
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	ns
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	ns
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	ns
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	ns
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	ns

Write Cycle

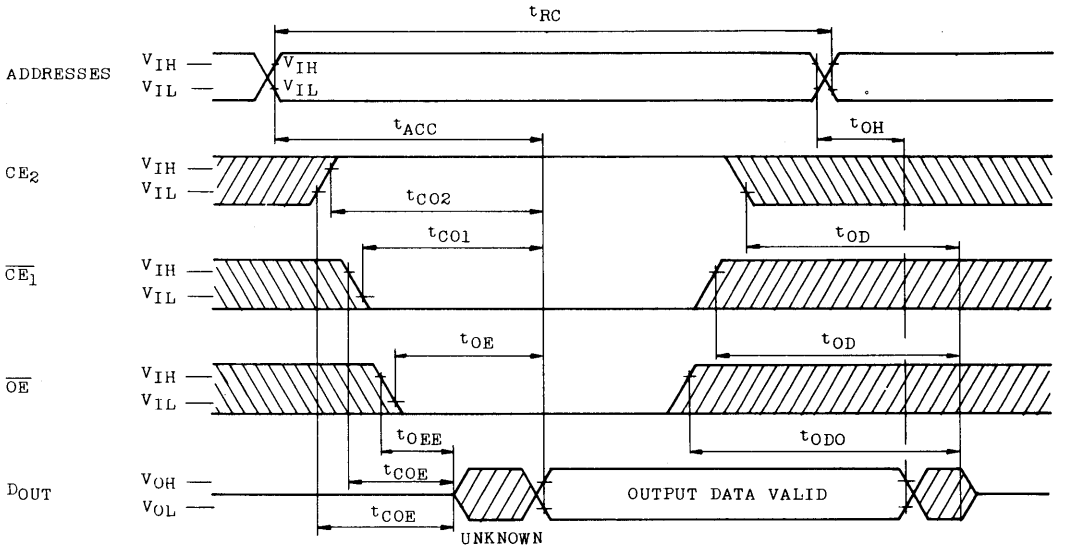
SYMBOL	PARAMETER	TC5563APL-10		TC5563APL-12		TC5563APL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	ns
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	ns
t_{AS}	Address Set up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	ns
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	ns
t_{DS}	Data Set Up Time	40	—	50	—	60	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns

A. C. TEST CONDITIONS

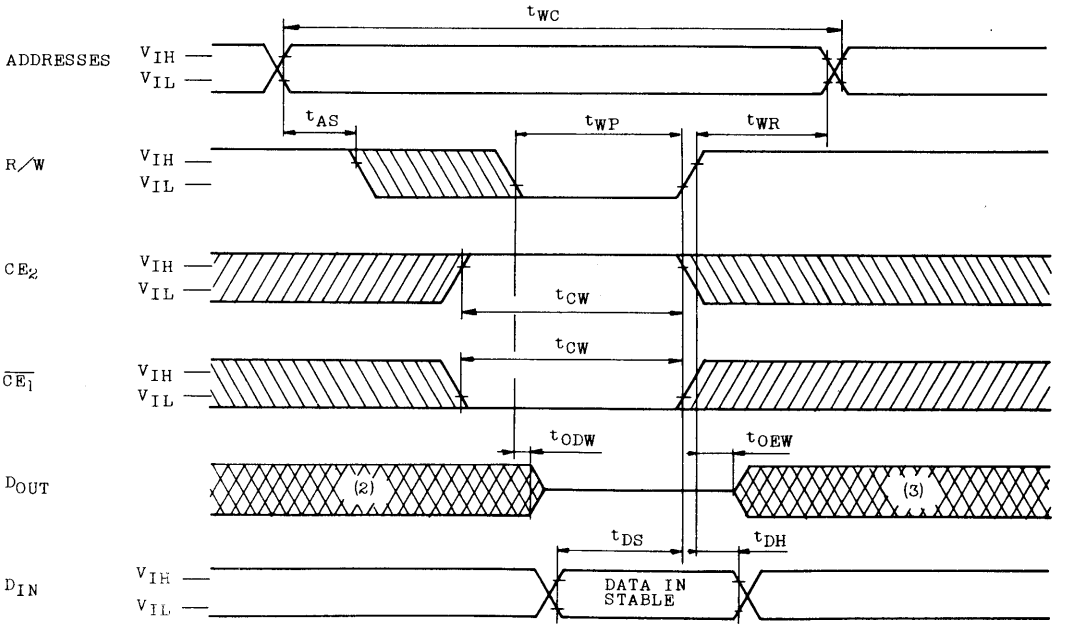
Output Load	: 100pF + 1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement Reference Level	V_{IN} : 0.8V, 2.2V V_{OUT} : 0.8V, 2.2V
	: 5ns

TIMING WAVEFORMS

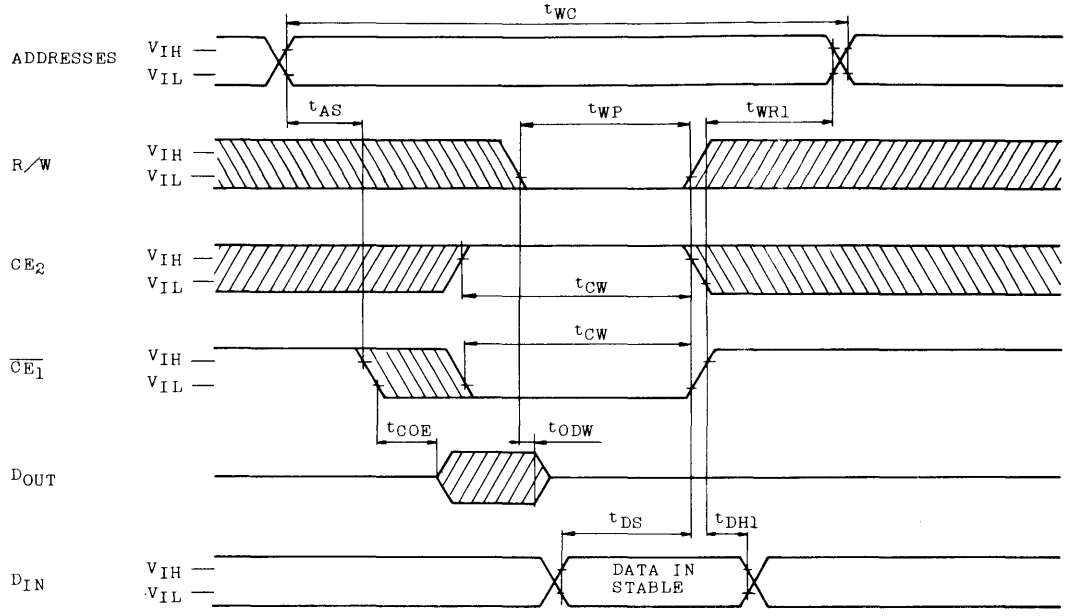
- READ CYCLE (1)



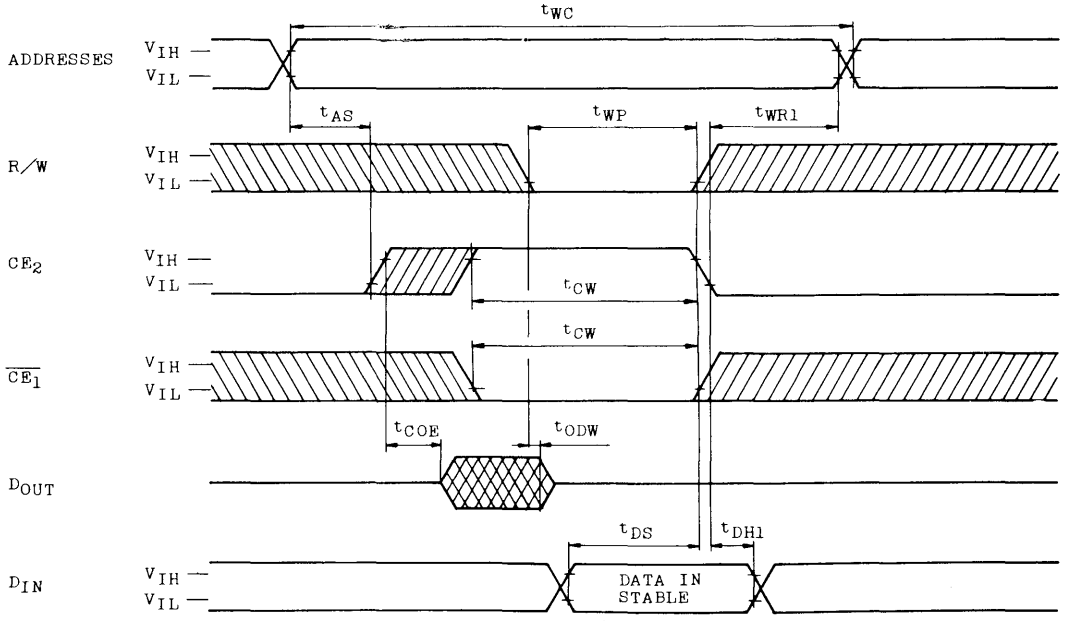
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



- WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note :

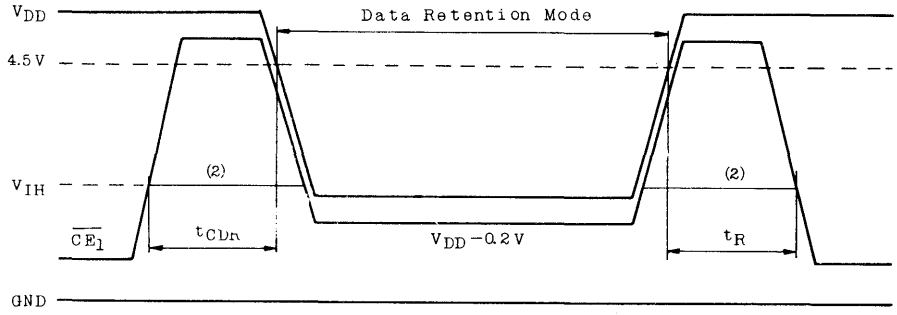
1. R/W is High for Read cycle,
2. Assuming that $\overline{CE_1}$ low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

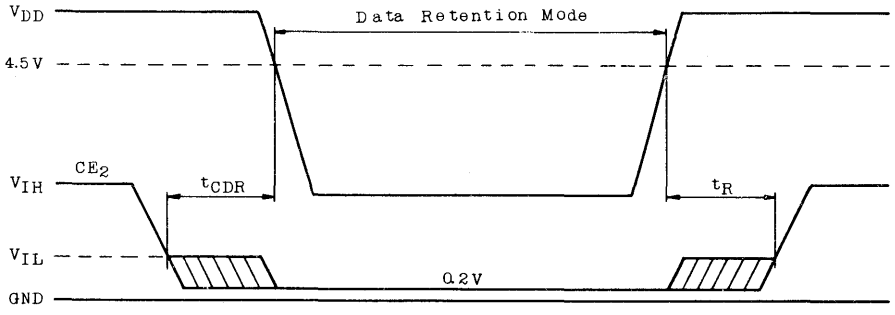
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	—	—	50	μA
		V_{DD}=5.5V	—	—	100	μA
t_{CDR}	Chip Deselection to Data Retntion Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	ns

* : Read cycle time.

- $\overline{CE1}$ Controlled Data Retention Mode (1)



- CE2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS_1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF. decoupling capacitor for every device is recommended to eliminate such noise.

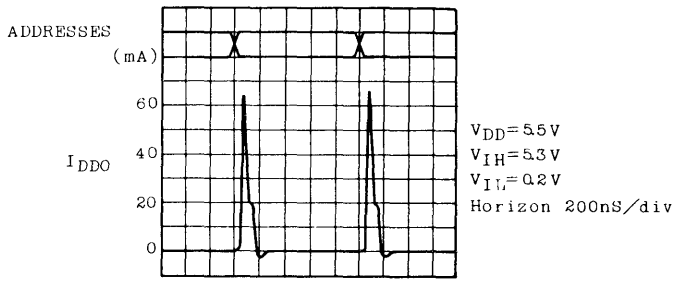
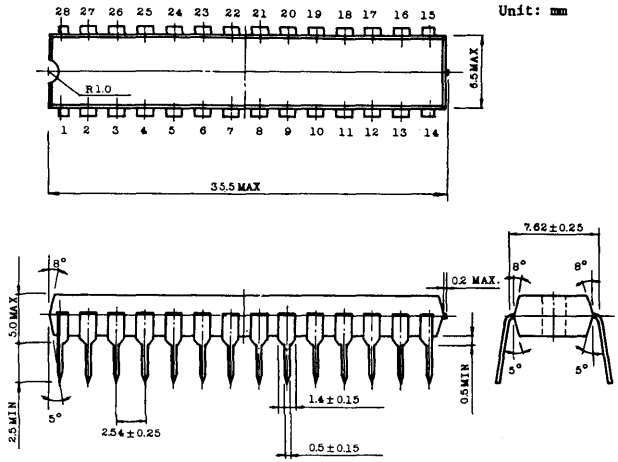


Fig. TYPICAL CURRENT WAVEFORMS

OUTLINE DRAWINGS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5563APL-10L, TC5563APL-12L TC5563APL-15L

PRELIMINARY

DESCRIPTION

The TC5563APL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

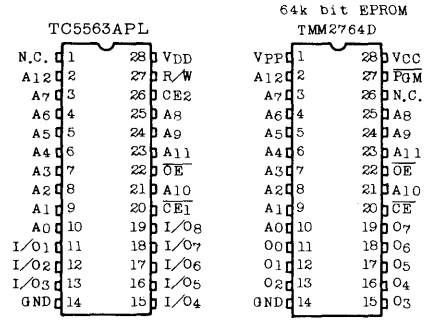
The TC5563APL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5563APL is offered in a dual-in-line 28 pin 0.3 inch width plastic package.

FEATURES

- Low Power Dissipation
  27.5mW/MHz (MAx.) Operating
- Standby Current : 1μA (Max.) Ta=25°C
- Access Time
  TC5563APL-10L : 100ns (Max.)
  TC5563APL-12L : 120ns (Max.)
  TC5563APL-15L : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

PIN CONNECTION (TOP VIEW)



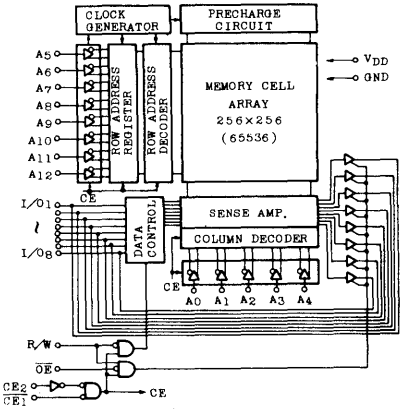
PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package(SOP)	*TC5565AFL

* : See TC5565APL/AFL Technical Date.

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	$-0.5 \sim V_{DD}+0.5$	V
P_D	Power Dissipation	0.8	W
T_{SOLDER}	Soldering Temperature	260·10	°C·Sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns

D. C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL} or R/W=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0~V_{DD}		—	—	±1.0	μA
I_{DDO1}	operating Current	V_{DD}=5.5V Iout=0mA $\overline{CE_1}$=V_{IL} CE_2=V_{IH} Other Input=V_{IH}/V_{IL}	t_{CYCLE}=1μs	—	—	10	mA
			t_{CYCLE}=Min. cycle	—	—	45	
I_{DDO2}	Operating Current	V_{DD}=5.5V $\overline{CE_1}$=0.2V CE_2=V_{DD}−0.2V Other Input Iout=0mA =V_{DD}−0.2V/0.2V	t_{CYCLE}=1μs	—	—	5	mA
			t_{CYCLE}=Min. cycle	—	—	40	
I_{DDS1}	Standby Current	$\overline{CE_1}$=V_{IH} or CE_2=V_{IL}		—	—	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1}$=V_{DD}−0.2V or CE_2=0.2V	Ta=25°C	—	0.6	1.0	μA
			Ta=0~70°C	—	—	30	

* : In standby mode with $\overline{CE_1}$≧V_{DD}−0.2V, these specification limits are guaranteed under the condition of CE_2≧V_{DD}−0.2V or CE_2≦0.2V

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	

Write Cycle

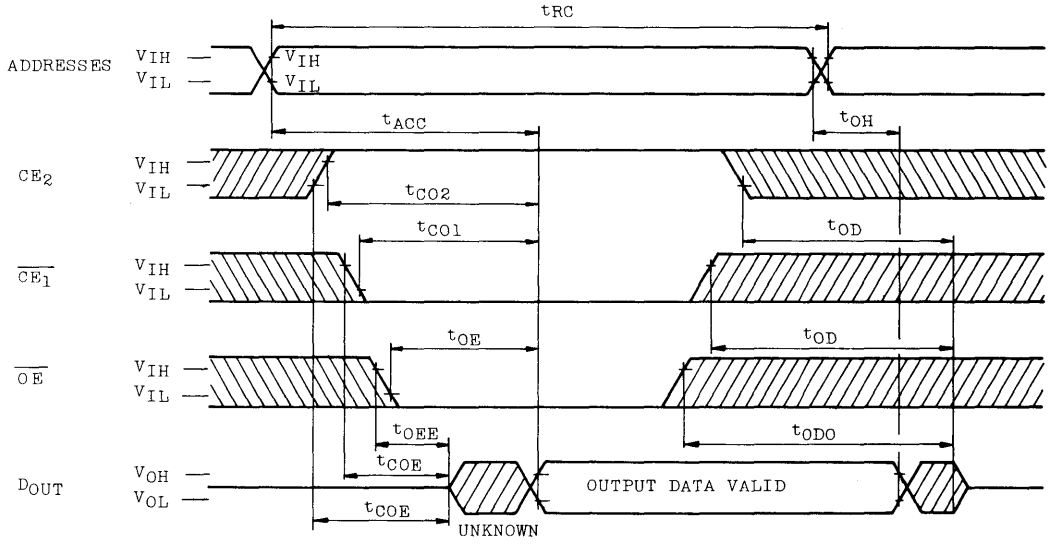
SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	
t_{AS}	Address Set up Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

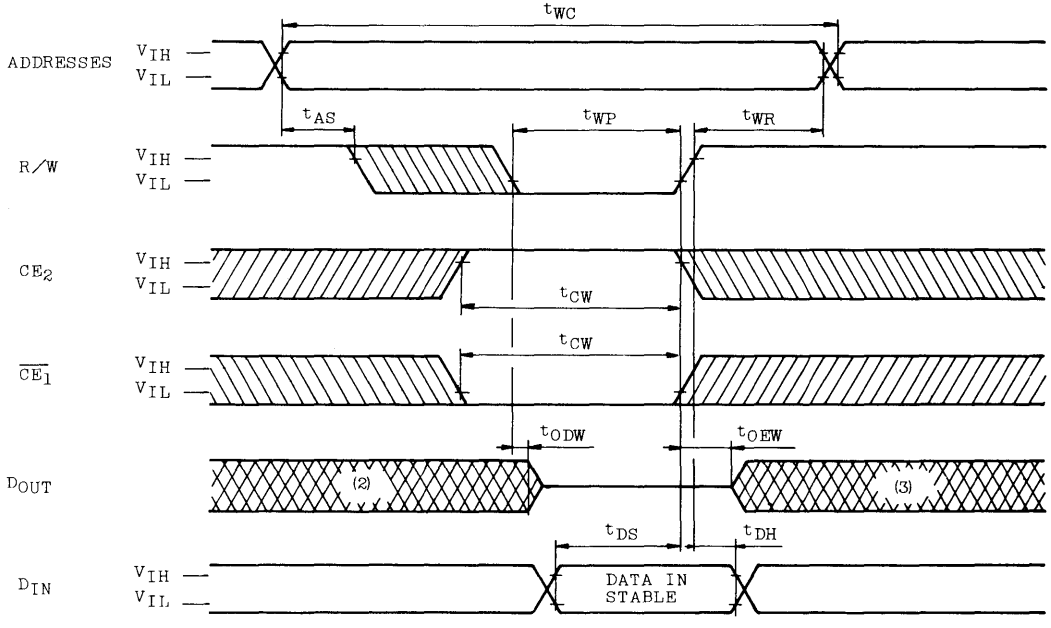
Output Load	: 100pF+1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement Reference Level	V_{IN} : 0.8V, 2.2V V_{OUT} : 0.8V, 2.2V
t_r, t_f	: 5ns

TIMING WAVEFORMS

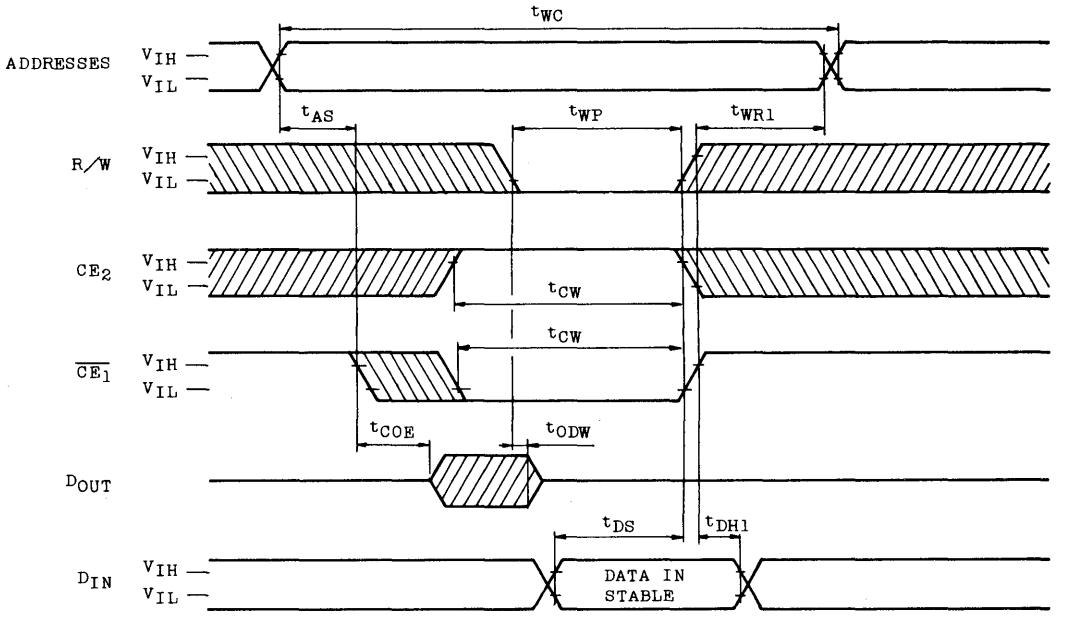
- READ CYCLE (1)



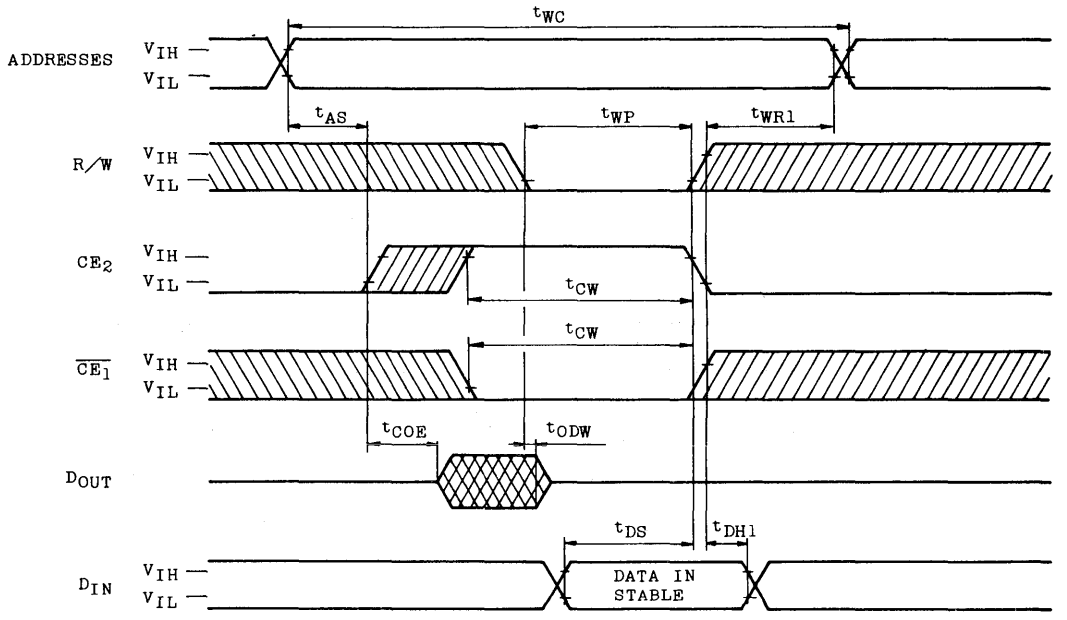
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

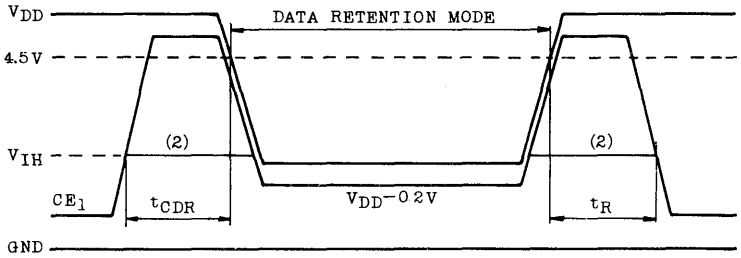
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occures coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

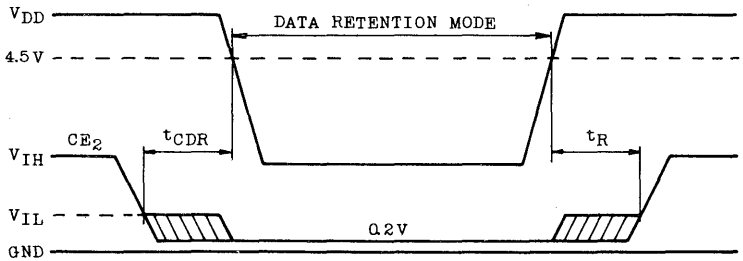
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	—	—	15	μA
		V_{DD}=5.5V	—	—	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	ns

* : Read cycle time.

● $\overline{CE1}$ Controlled Data Retention Mode (1)



● CE2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5563APL/F is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

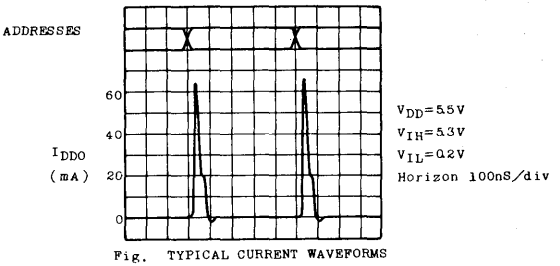
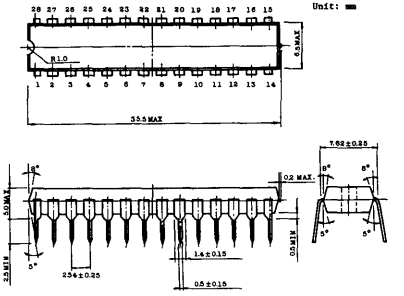


Fig. TYPICAL CURRENT WAVEFORMS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TC5565APL-10, TC5565APL-12, TC5565APL-15
TC5565AFL-10, TC5565AFL-12, TC5565AFL-15

DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.
When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565APL/AFL has three control inputs. Two chip enable ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.
The TC5565APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini Flat Package.

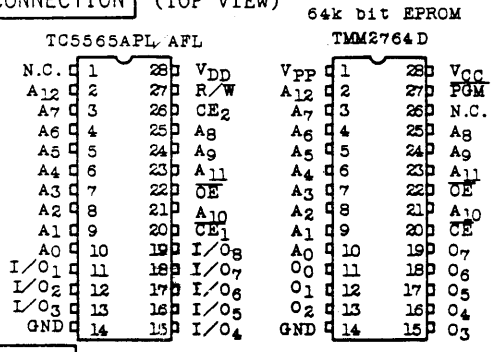
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current : 100μA(Max.) Ta=70°C
- Access Time
  TC5565APL/AFL-10 : 100ns(Max.)
  TC5565APL/AFL-12 : 120ns(Max.)
  TC5565APL/AFL-15 : 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

*) See TC5563APL Technical Data.

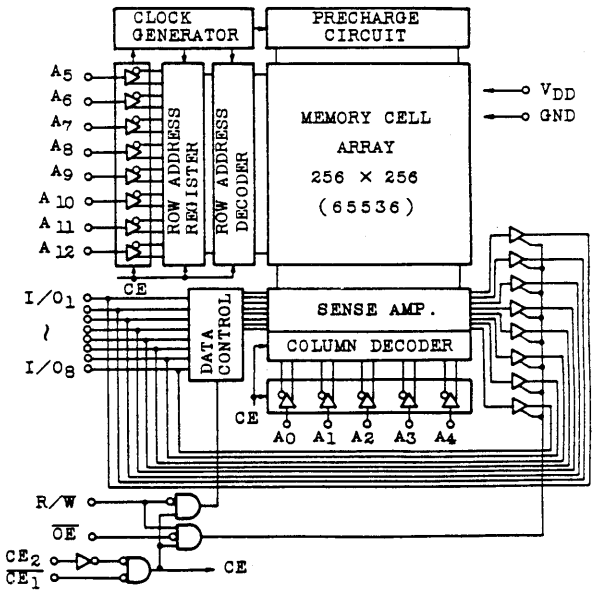
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Input/Output
VDD	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}_1$	CE2	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	*-0.3~7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	-55~150	°C
T_{opr}	Operating Temperature	0~70	°C

* -3.0V at pulse width 50ns MAX. ** Flat package

D.C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C and OPERATING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$			-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$			-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}_1=V_{IH}$ or $CE_2=V_{OL}$ or $R/\overline{W}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0\sim V_{DD}$			-	-	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$ $\overline{CE}_1=V_{IL}$ $CE_2=V_{IH}$ Other input= V_{IH}/V_{IL}	$t_{cycle}=1.0\mu s$		-	-	10	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	45	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	40	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	35	mA
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE}_1=0.2V$ $CE_2=V_{DD}-0.2V$ Other input= $V_{DD}-0.2V/0.2V$	$t_{cycle}=1.0\mu s$		-	-	5	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	40	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	35	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE}_1=V_{IH}$ or $CE_2=V_{IL}$			-	-	3	mA
*I_{DDS2}		$\overline{CE}_1=V_{DD}-0.2V$ or $CE_2=0.2V$		$V_{DD}=5.5V$	-	2	100	μA
				$V_{DD}=3.0V$	-	1	50	μA

Note * : In standby mode with $\overline{CE}_1\geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2\geqq V_{DD}-0.2V$ or $CE_2\leqq 0.2V$.

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	-	-	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	-	-	10	pF

Note : This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	ns
t_{CO1}	$\overline{CE}_1$ Access Time	-	100	-	120	-	150	ns
t_{CO2}	CE_2 Access Time	-	100	-	120	-	150	ns
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	ns
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z	10	-	10	-	15	-	ns
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	ns
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z	-	35	-	40	-	50	ns
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	ns
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	ns

Write Cycle

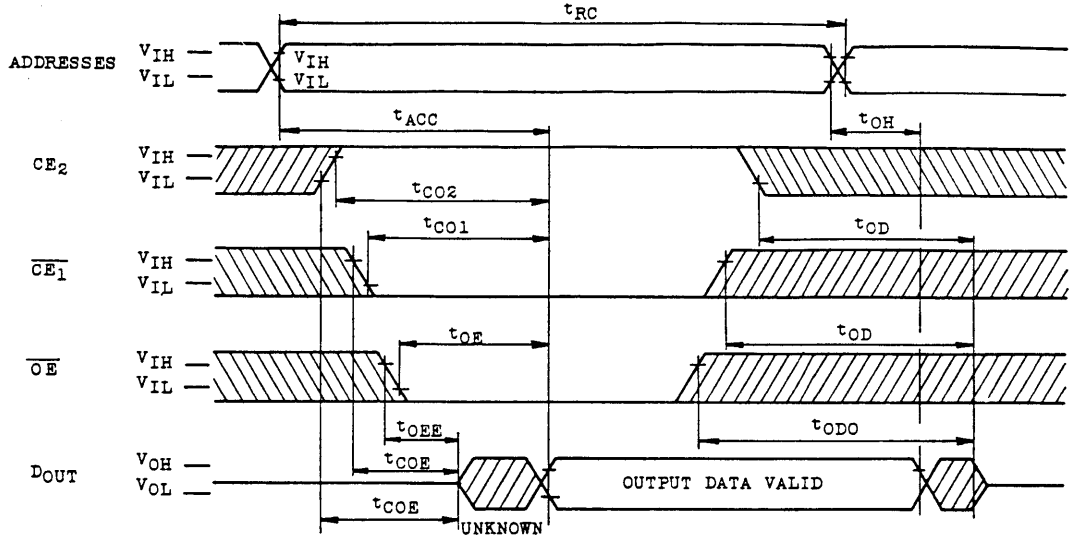
SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	ns
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	ns
t_{AS}	Address Set up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	R/W to Output High-Z	-	35	0	40	-	50	ns
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	ns
t_{DS}	Data Set up Time	40	-	50	-	60	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITION

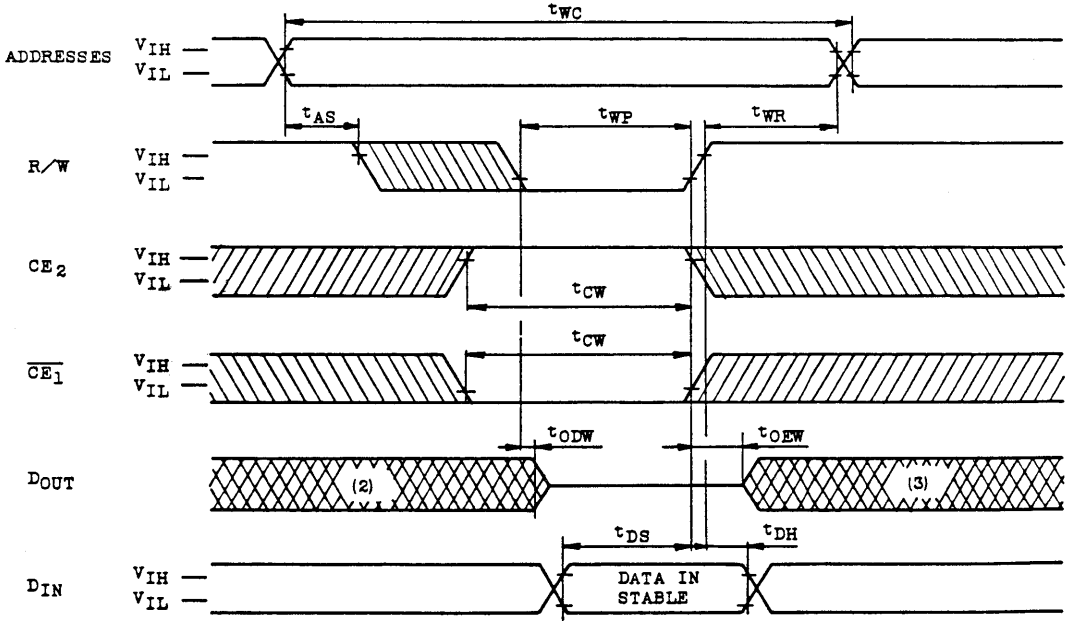
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

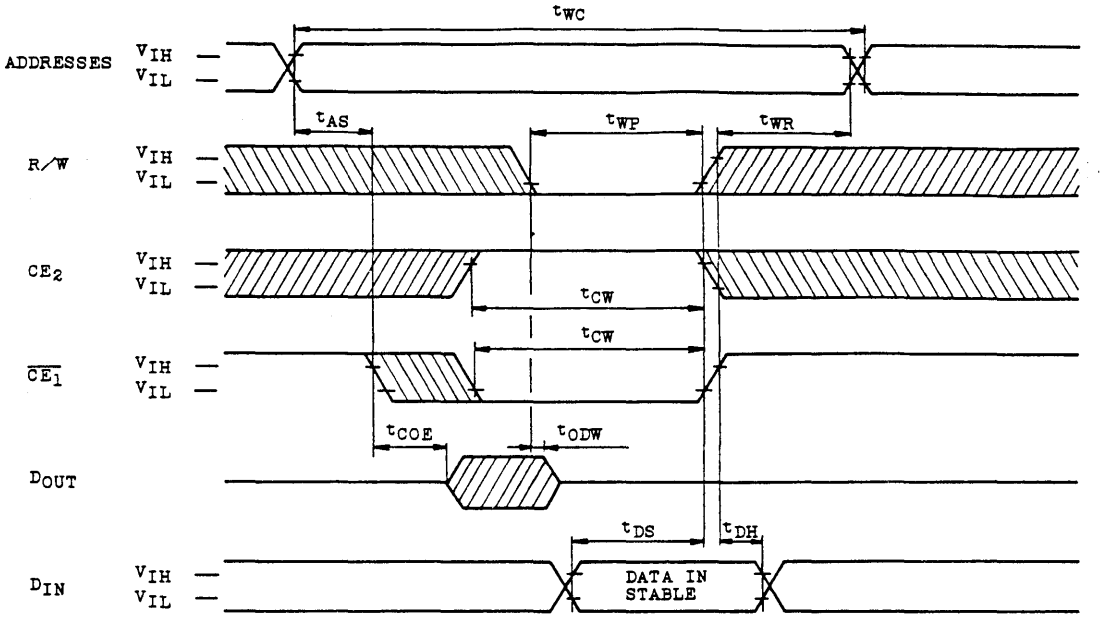
READ CYCLE (1)



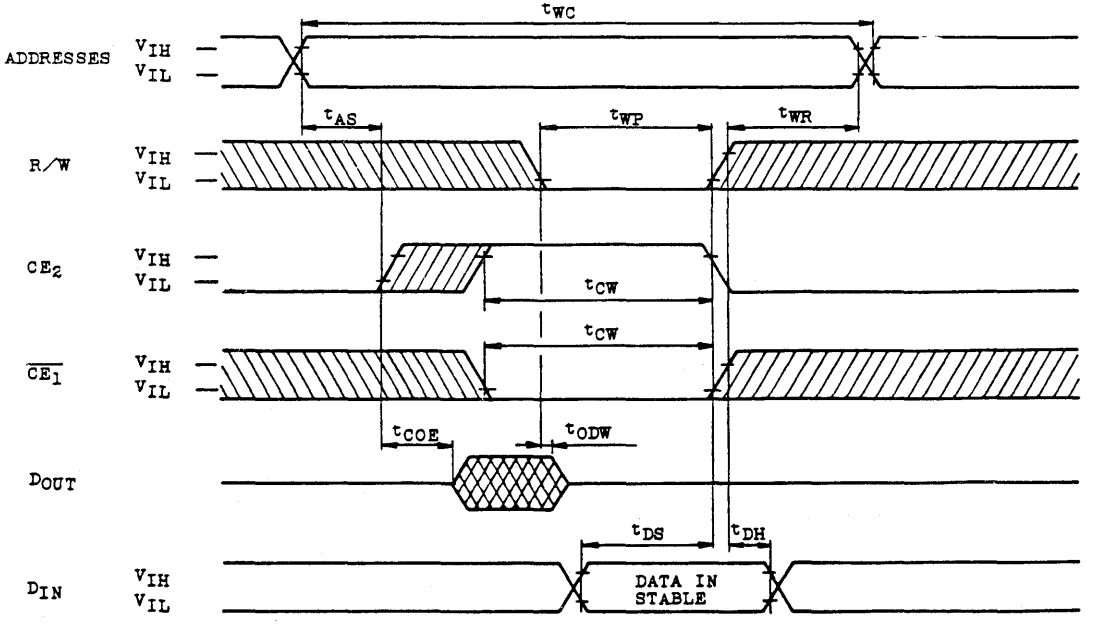
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}_1$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

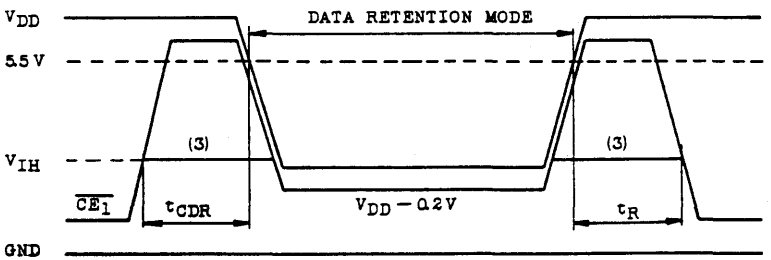
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

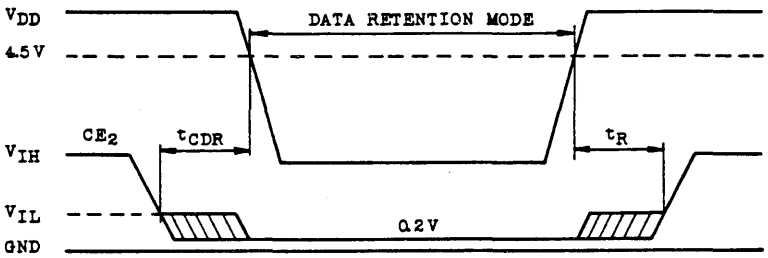
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}(1)	-	-	μs

Note (1) : Read cycle time.

$\overline{CE}_1$ Controlled Data Retention Mode (2)



CE_2 Controlled Data Retention Mode (4)



Note 2 : In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD}-0.2V$.

3 : If the V_{IH} of $\overline{CE}_1$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

4 : In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an synchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

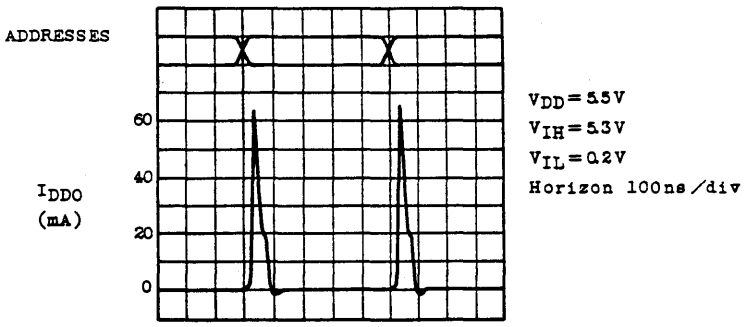
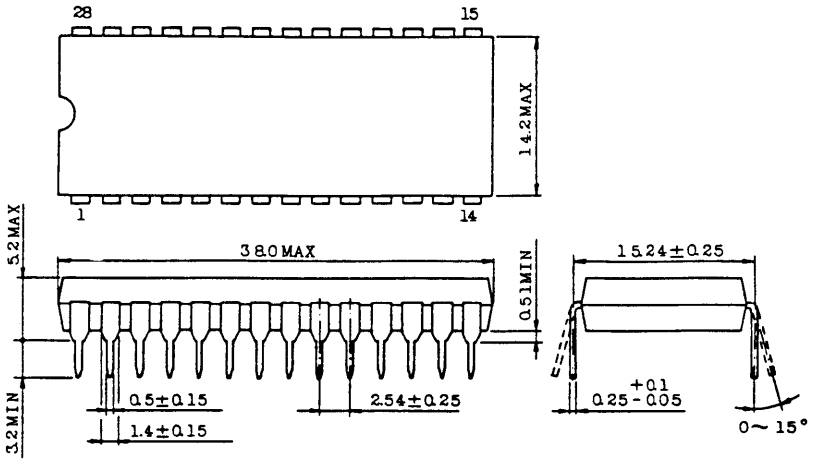


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

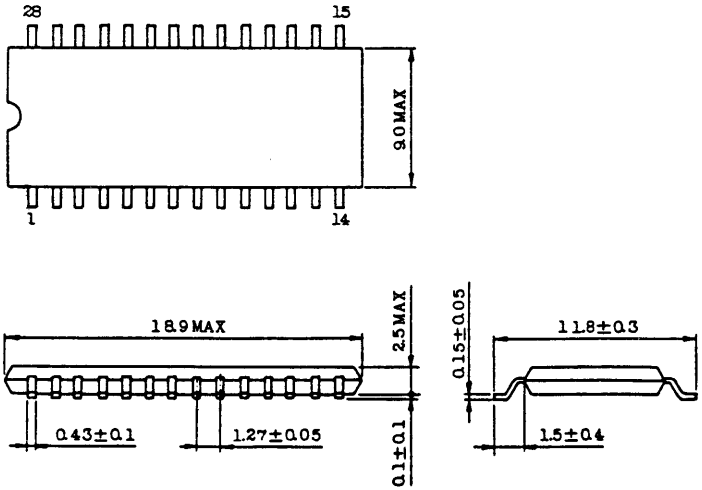
Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

MFP 28 PIN OUTLINE DRAWING (F28GC-P)

Unit in mm



Note) Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5565APL-10L, TC5565APL-12L, TC5565APL-15L
TC5565AFL-10L, TC5565AFL-12L, TC5565AFL-15L

DESCRIPTION

The TC5565APL/AFL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns. When CE_2 is a logical low or $\overline{CE_1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE_1}$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL/AFL also features pin compatibility with the 64k bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

The TC5565APL is offered in a dual-in-line 28 pin standard plastic package. The TC5565AFL is offered in 28 pin mini flat package.

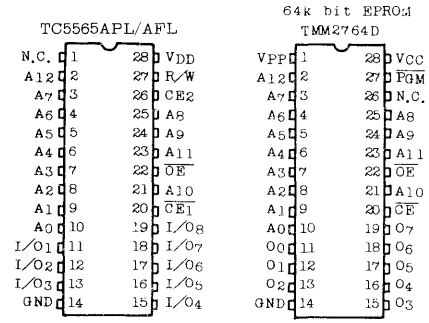
FEATURES

- Low Power Dissipation
  27.5mW/MHz (Max.) Operating
- Standby Current : 1μA (Max.) Ta=25°C
- Access Time
  TC5565APL/AFL-10L : 100ns (Max.)
  TC5565APL/AFL-12L : 120ns (Max.)
  TC5565APL/AFL-15L : 150ns (Max.)
- 5V Single Power Supply
- Power Down Features : CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage : 2.0~5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package(SOP)	TC5565AFL

* : See TC5563APL Technical Date.

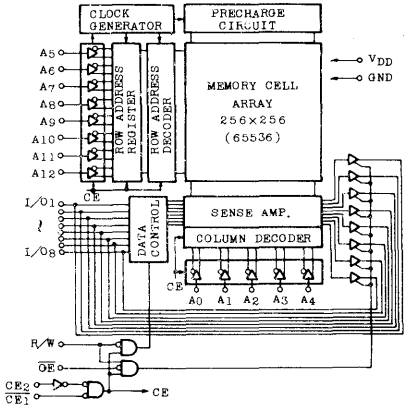
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE_1}$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	$I/O_1 \sim I/O_8$	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	$-0.5 \sim V_{DD}+0.5$	V
P_D	Power Dissipation	1.0/0.6**	W
Tsolder	Soldering Temperature	260·10	C·Sec
Tstg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

* : −3.0V at Pulse width 50ns Max.
** : Flat package

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	$V_{DD}+0.3$	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* : −3.0V at Pulse width 50ns Max.

D. C. and OPERATING CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$			–	–	± 10	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$			−10	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$			4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$			–	–	± 1.0	μA
I_{DDO1}	Operating Current	$V_{DD} = 5.5V$ $\overline{CE_1} = V_{IL}$ $CE_2 = V_{IH}$ Other input = V_{IH}/V_{IL} $I_{OUT} = 0mA$	$t_{cycle} = 1.0\mu s$		–	–	10	mA
			TC5563APL-10 TC5563AFL-10	t_{cycle} = 100ns	–	–	45	mA
			TC5563APL-12 TC5563AFL-12	t_{cycle} = 120ns	–	–	40	mA
			TC5563APL-15 TC5563AFL-15	t_{cycle} = 150ns	–	–	35	mA
I_{DDO2}		$V_{DD} = 5.5V$ $\overline{CE_1} = 0.2V$ $CE_2 = V_{DD}-0.2V$ Other input = $V_{DD}-0.2V/0.2V$ $I_{OUT} = 0mA$	$t_{cycle} = 1.0\mu s$		–	–	5	mA
			TC5563APL-10 TC5563AFL-10	t_{cycle} = 100ns	–	–	40	mA
			TC5563APL-12 TC5563AFL-12	t_{cycle} = 120ns	–	–	35	mA
			TC5563APL-15 TC5563AFL-15	t_{cycle} = 150ns	–	–	30	mA
I_{DDS1}	Standby Current	$\overline{CE_1} = V_{IH}$ or $CE_2 = V_{IL}$			–	–	3	mA
*I_{DDS2}	Standby Current	$\overline{CE_1} = V_{DD}-0.2V$ or $CE_2 = 0.2V$		Ta = 25°C	–	0.6	1.0	μA
				Ta = 0 ~ 70°C	–	–	30	

* : In standby mode with $\overline{CE_1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geqq V_{DD}-0.2V$ or $CE_2 \leqq 0.2V$.

CAPACITANCE ($Ta = 25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

(Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{ACC}	Address Access Time	—	100	—	120	—	150	
t_{CO1}	$\overline{CE1}$ Access Time	—	100	—	120	—	150	
t_{CO2}	CE2 Access Time	—	100	—	120	—	150	
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	—	10	—	15	—	
t_{OEE}	Output Enable to Output in Low-Z	5	—	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	—	35	—	40	—	50	
t_{ODO}	Output Enable to Output in High-Z	—	35	—	40	—	50	
t_{OH}	Output Data Hold Time	20	—	20	—	20	—	

Write Cycle

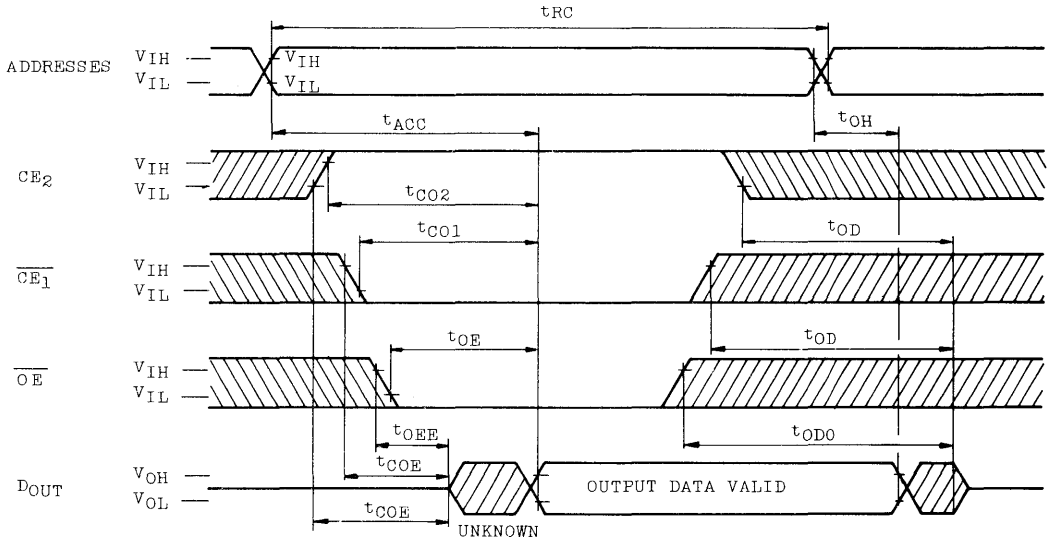
SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{WP}	Write Pulse Width	60	—	70	—	90	—	
t_{CW}	Chip Selection to End of Write	80	—	85	—	100	—	
t_{AS}	Address Set up Time	0	—	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	0	—	
t_{ODW}	R/W to Output in High-Z	—	35	—	40	—	50	
t_{OEW}	R/W to Output in Low-Z	5	—	5	—	10	—	
t_{DS}	Data Set Up Time	40	—	50	—	60	—	
t_{DH}	Data Hold Time	0	—	0	—	0	—	

A. C. TEST CONDITIONS

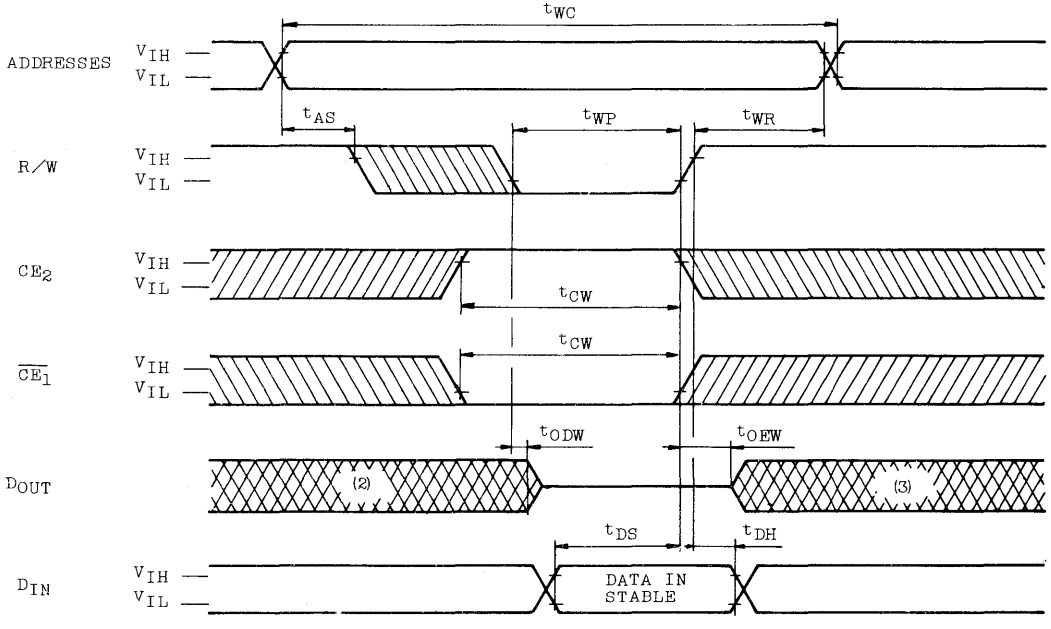
Output Load	: 100pF+1 TTL Gate
Input Pulse Level	: 0.6V, 2.4V
Timing Measurement	V_{IN} : 0.8V, 2.2V
Reference Level	V_{OUT} : 0.8V, 2.2V
t_r, t_f	: 5ns

TIMING WAVEFORMS

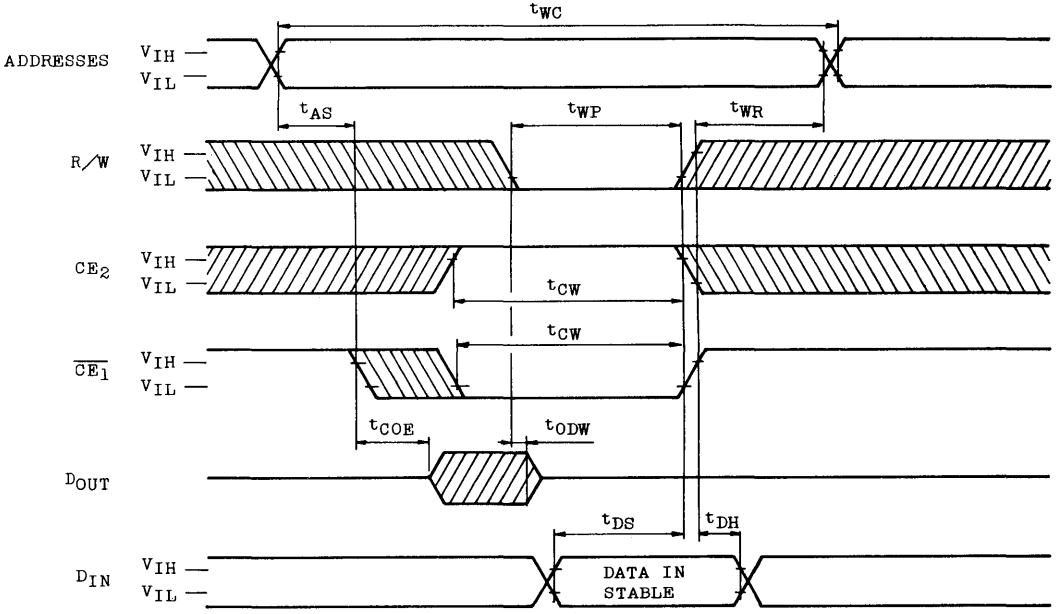
- READ CYCLE (1)



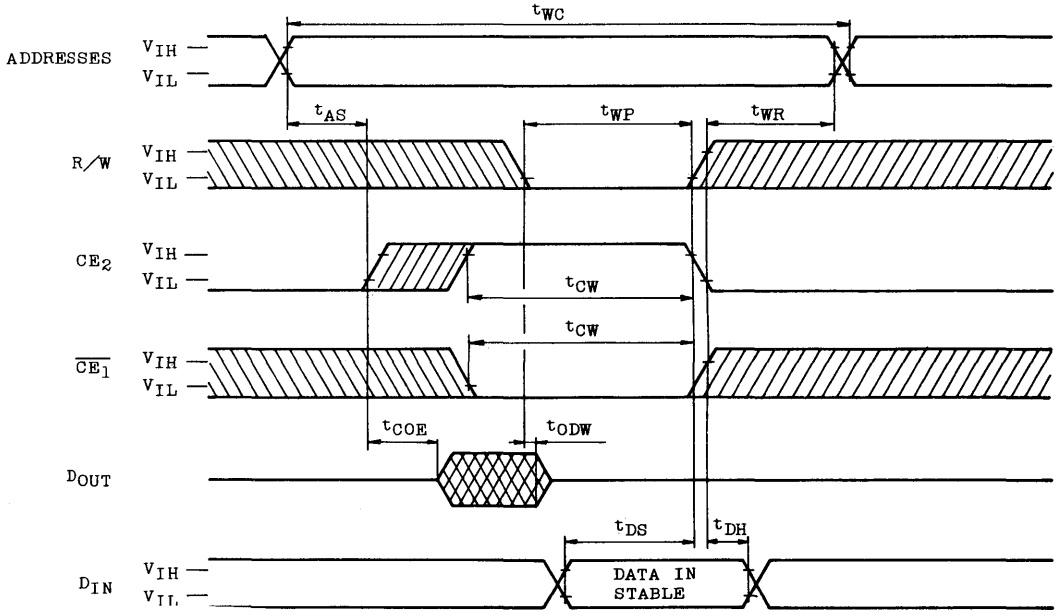
- WRITE CYCLE 1 (4) (R/W Controlled Write)



- WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



- WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note :

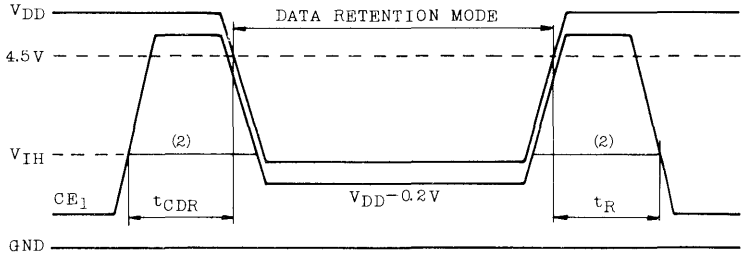
1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE_1}$ Low transition of CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE_1}$ High transition or CE_2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0~70°C)

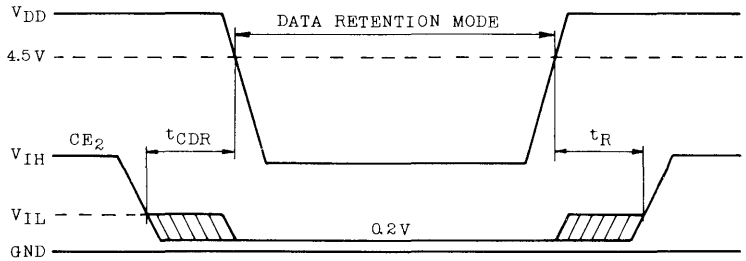
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Stand by Supply Current	V_{DD}=3.0V	—	—	15	μA
		V_{DD}=5.5V	—	—	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}*	—	—	μs

* : Read cycle time.

● $\overline{CE_1}$ Controlled Data Retention Mode (1)



● CE_2 Controlled Data Retention Mode (3)



Note :

1. In $\overline{CE_1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$ or $CE_2 \geqq V_{DD} - 0.2V$.
2. If the V_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.
3. In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leqq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure. This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

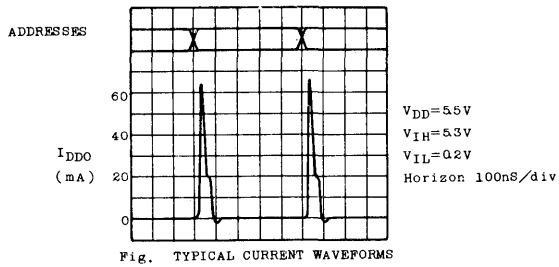
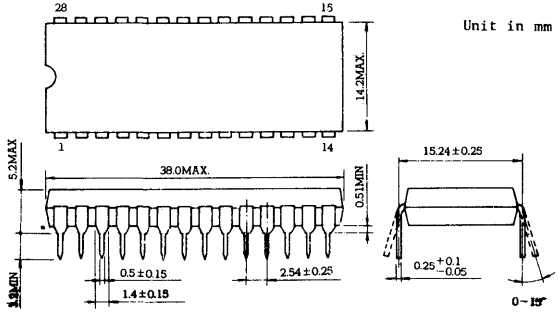


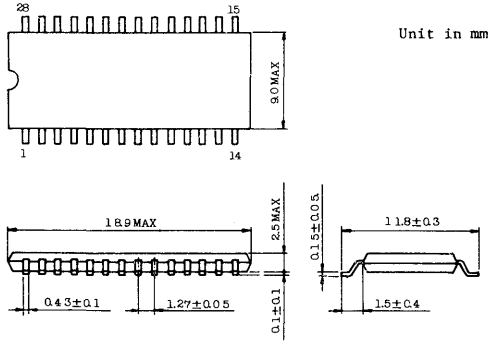
Fig. TYPICAL CURRENT WAVEFORMS

- DIP 28 PIN OUTLINE DRAWING (6D28A-P)



Note : Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

- MFP 28 PIN OUTLINE DRAWING (F28GA-P)



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

8,192 WORD × 8 BIT CMOS STATIC RAM

TC5564APL-15, TC5564APL-20
TC5564AFL-15, TC5564AFL-20

PRELIMINARY

DESCRIPTION

TC5564APL is 65536 bits static random access memory organized as 8192 words by 8 bits using CMOS technology, and operates with a single 5V power supply.

Advanced circuit techniques provides low power feature with a maximum operating of 5mA/MHz. Operation current depends on cycle time.

TC5564APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control. Output enable ($\overline{OE}$) input provides fast memory access. When device is placed in standby mode with chip off state, standby current is typically 0.01μA. So the TC5564APL is suitable for use in various microprocessor application systems where low power and battery back up are required. Ultra low standby power allow not only battery but capacitance backup.

Pin assignment of TC5564APL is pin-compatible with the 64K bits EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems.

TC5564APL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

FEATURES

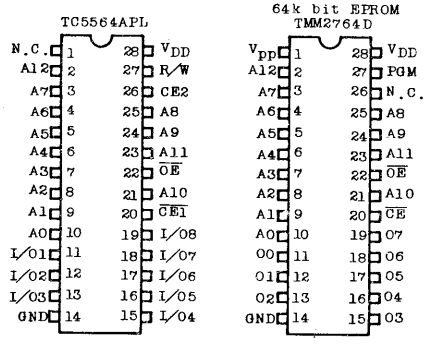
- Low Power Dissipation
  5mA/MHz (MAX.) Operating
  0.2μA (MAX.) at Ta=25°C Standby
  1.0μA (MAX.) at Ta=60°C Standby
- 5V Single Power Supply
- Fully Static Operation
- Data Retention Voltage : 2.0~5.5V
- Plastic DIP and Plastic Flat Package
- Pin Compatible with 2764 type EPROM

- Access Time

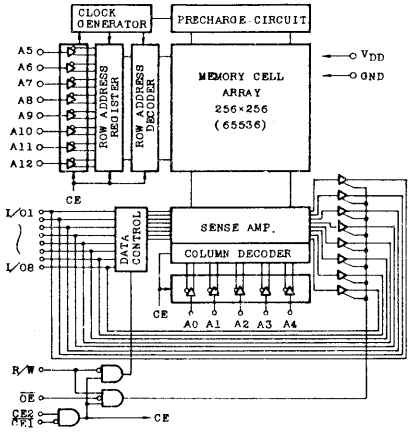
	TC5564APL-15 TC5564AFL-15	TC5564APL-20 TC5564AFL-20
Address Access Time (MAX.)	150ns	200ns
$\overline{CE1}$ Access Time (MAX.)	150ns	200ns
CE2 Access Time (MAX.)	150ns	200ns
$\overline{OE}$ Access Time (MAX.)	70ns	100ns

- Directly TTL Compatible : All Inputs and Outputs
- Wide Temperature Operation : −40~85°C

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N. C.	No Connection

OPERATING MODE

Operation Mode	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	Power
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	
Output Deselect	*	*	H	*	High-Z	
Standby	H	*	*	*	"	I_{DDS}
	*	L	*	*	"	I_{DDS}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
*V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3**~V_{DD}	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0(0.6)***	W
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C

* 8.5V at 100ns.
** −3.0V Pulse width 50ns
*** SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

* −3.0V Pulse width 50ns

D. C and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10% Unless other wise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN} = 0~V_{DD}	—	—	±1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	4.0	—	—	mA
V_{OH}	Output High Voltage	I_{OH} = −20μA	V_{DD}−0.1	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 20μA	—	—	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or R/W = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	—	—	±1.0	μA

SYMBOL	PARAMETER	CONDITIONS			MIN.	TYP.	MAX.	UNIT
I_{DDO1}	Operating Current	$\overline{CE1}=V_{IL}$ and CE2 = V_{IH} Other Input = V_{IH}/V_{IL} I_{OUT}=0mA	$t_{cycle}=1\mu s$		—	—	10	mA
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	—	—	40	
				TC5564APL-20 TC5564AFL-20	—	—	35	
I_{DDO2}	Operating Current	$\overline{CE1}$=0.2V and CE2=V_{DD}−0.2V, Other Input =V_{DD}−0.2V/0.2V I_{OUT} = 0mA duty 100%	$t_{cycle}=1\mu s$		—	—	5	mA
			MIN CYCLE	TC5564APL-15 TC5564AFL-15	—	—	35	
				TC5564APL-20 TC5564AFL-20	—	—	30	
I_{DDS1}	Standby Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL}			—	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE_1}=V_{DD}$−0.2V or CE2=0.2V V_{DD}=2.0~5.5V		Ta=25°C	—	0.01	0.2	μA
				Ta=60°C	—	—	1.0	

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 $\geqq V_{DD}-0.2V$ or CE2 $\leqq$ 0.2V.
(2) All voltage is measured from GND.

CAPACITANCE (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

READ CYCLE

SYMBOL	PARAMETER	TC5564APL-15 TC5564AFL-15		TC5564APL-20 TC5564AFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	—	200	—	ns
t_{ACC}	Address Access Time	—	150	—	200	
t_{CO1}	$\overline{CE1}$ Access Time	—	150	—	200	
t_{CO2}	CE2 Access Time	—	150	—	200	
t_{OE}	Output Enable to Output in Valid	—	70	—	100	
t_{COE}	Chip Enable to ($\overline{CE1}$, CE2) Output in Low-Z	10	—	10	—	
t_{OEE}	Output Enable to Output Low-Z	5	—	5	—	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) Output in High-Z	—	70	—	100	
t_{ODO}	Output Enable to Output High-Z	—	60	—	80	
t_{OH}	Output Data Hold Time	20	—	20	—	

WRITE CYCLE

SYMBOL	PARAMETER	TC5564APL-15 TC5564AFL-15		TC5564APL-20 TC5564AFL-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	150	—	200	—	ns
t_{WP}	Write Pulse Width	100	—	150	—	
t_{CW}	Chip Selection to End of Write	120	—	180	—	
t_{AS}	Address Set up Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{ODW}	R/W to Output High-Z	—	70	—	100	
t_{OEW}	R/W to Output Low-Z	10	—	10	—	
t_{DS}	Data Set Up Time	60	—	80	—	
t_{DH}	Data Hold Time	0	—	0	—	

A.C. TEST CONDITIONS

- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels : 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Times : 5ns
- Output Load : See Fig. 1

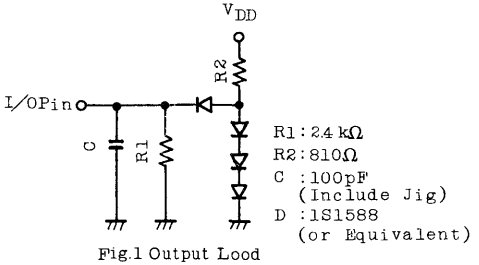
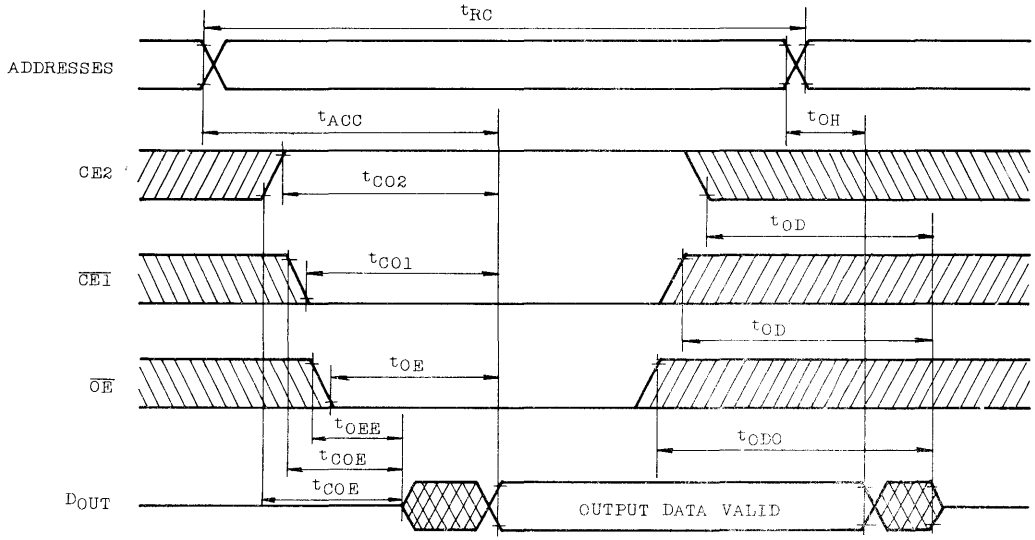


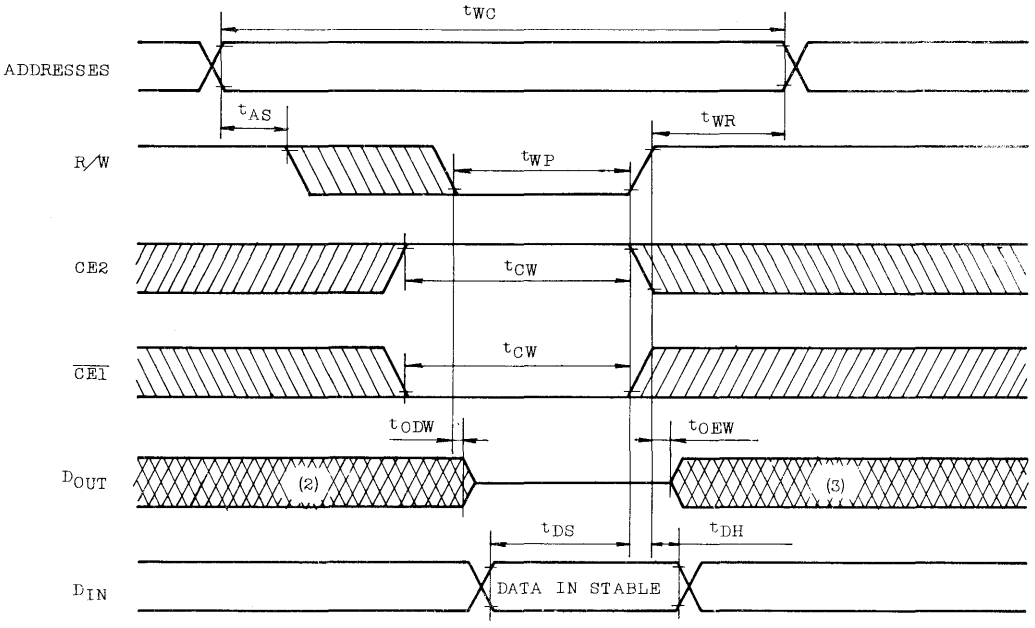
Fig.1 Output Lood

TIMING WAVEFORMS

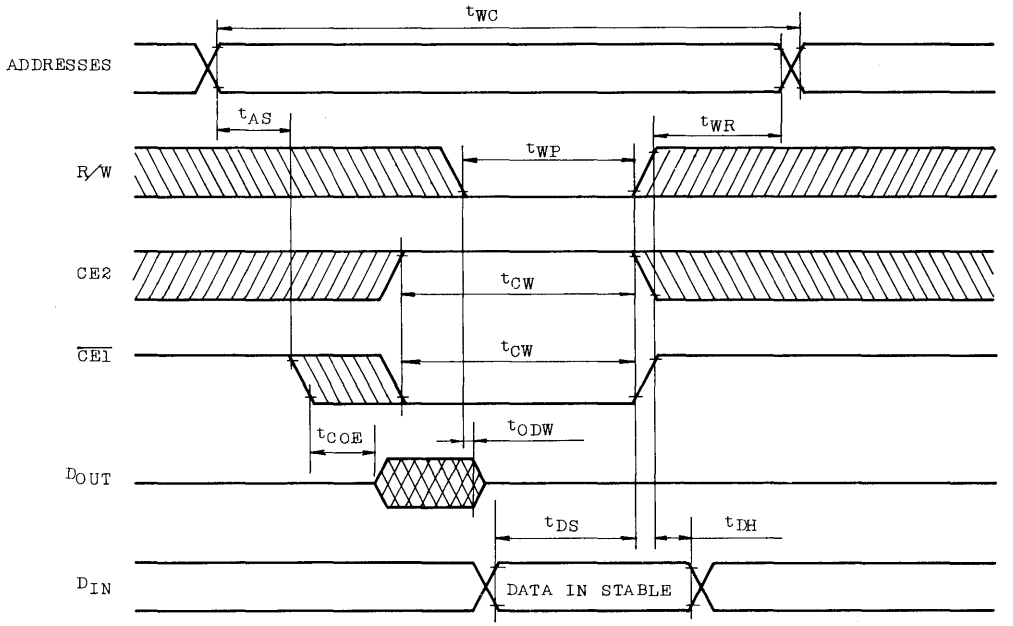
READ CYCLE (1)



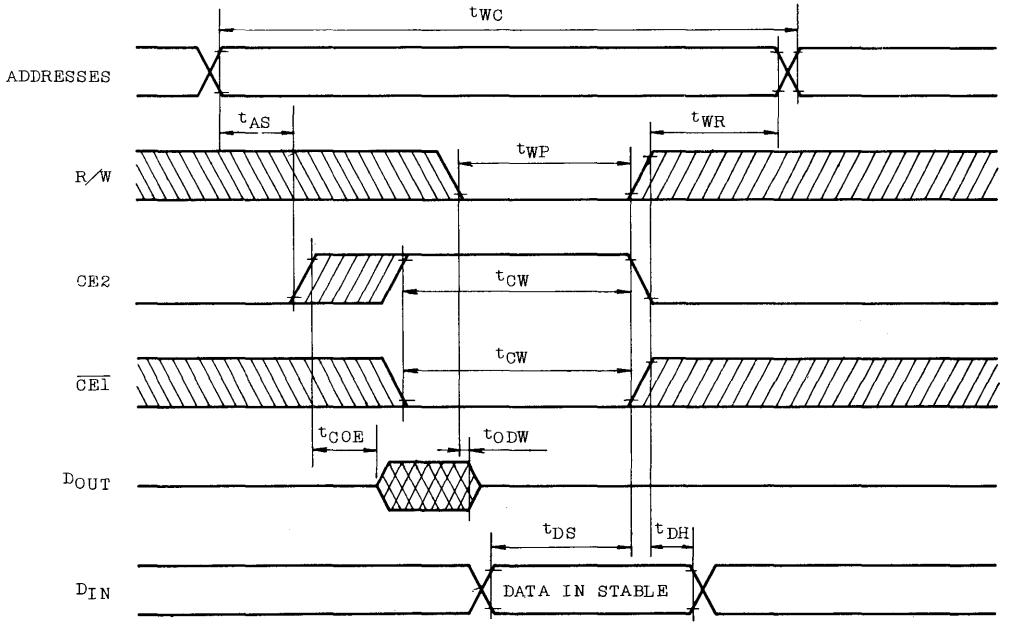
WRITE CYCLE (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)

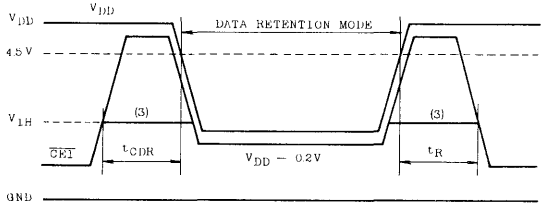


Note : (1) R/W is High for Read Cycle. (2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W low transition, Outputs remain in a high impedance state. (3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state. (4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

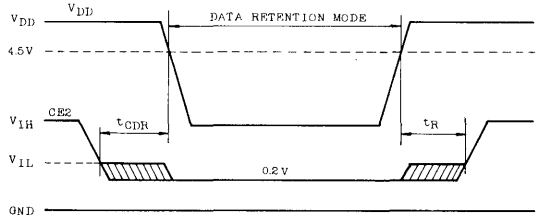
DATA RETENTION CHARACTERISTICS (Ta = −40~85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Current	Ta=25°C	—	0.01	0.2	μA
		Ta=60°C	—	—	1.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs

$\overline{CE1}$ Controlled Data Retention Mode (2)



CE2 Controlled Data Retention Mode (4)



Note : (1) T_{RC} : Read Cycle Time (2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2≦0.2V or CE2≧V_{DD}−02V. (3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} Voltage is going down from 4.5 to 2.4V, I_{DDS1} current flows. (4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2≦0.2V.

DEVICE INFORMATION

The TC5564APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation executed by internal pulse generated from row address transient. Therefore the peak current flows after only row address change, as is shown in the following figure.

This peak current may induce the noise on V_{DD}/GND line. Thus the use of about 0.1μF decoupling capacitor every device is recommended to eliminate such noise.

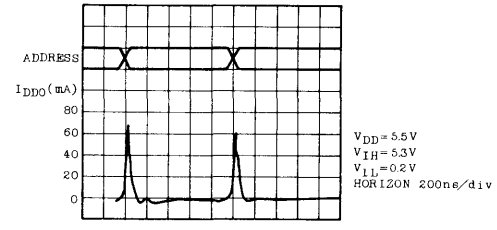
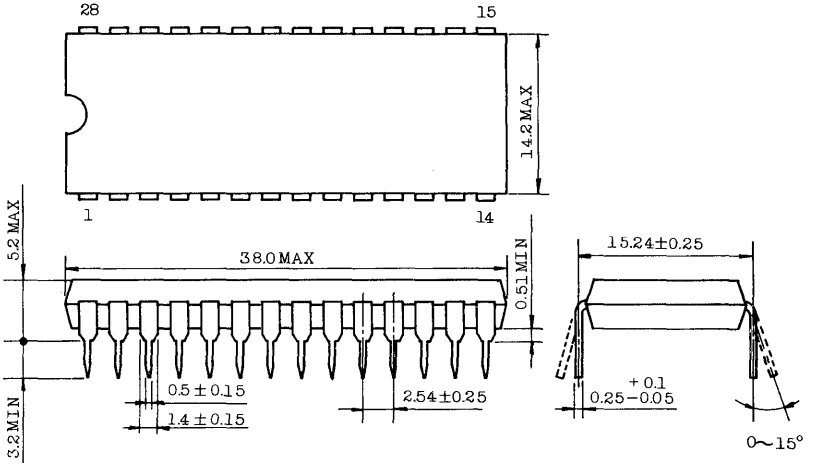


Fig. TYPICAL CURRENT WAVEFORMS

DIP 28 PIN OUTLINE DRAWING (6D28A-P)

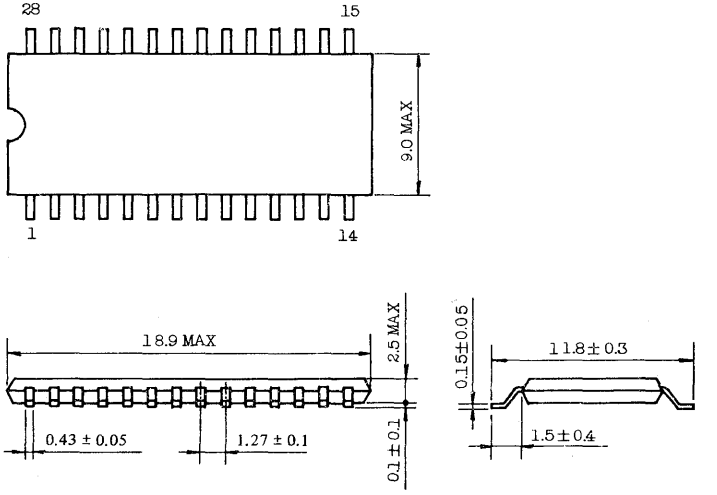
Unit in mm



Note : Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

32,768 WORD×8 BIT STATIC RAM
SILICON GATE CMOS

TC55257APL-85/APL-10/APL-12
TC55257AFL-85/AFL-10/AFL-12

PRELIMINARY

DESCRIPTION

The TC55257APL/AFL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257 APL/AFL has two control inputs. Chip enable ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC55257APL/AFL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

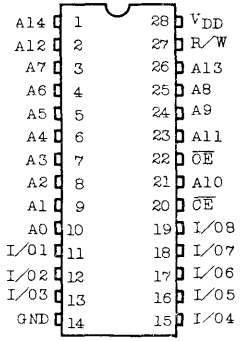
FEATURES

- Low Power Dissipation
  27.5mW/MHz (Typ.) Operating
- Standby Current
  100μA (Max.): TC55257APL-85/AFL-85
  APL-10/AFL-10
  APL-12/AFL-12
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC55257APL-85 TC55257AFL-85	TC55257APL-10 TC55257AFL-10	TC55257APL-12 TC55257AFL-12
Access Time (Max.)	85ns	100ns	120ns
Chip Enable Access Time (Max.)	85ns	100ns	120ns
Output Enable Time (Max.)	45ns	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package

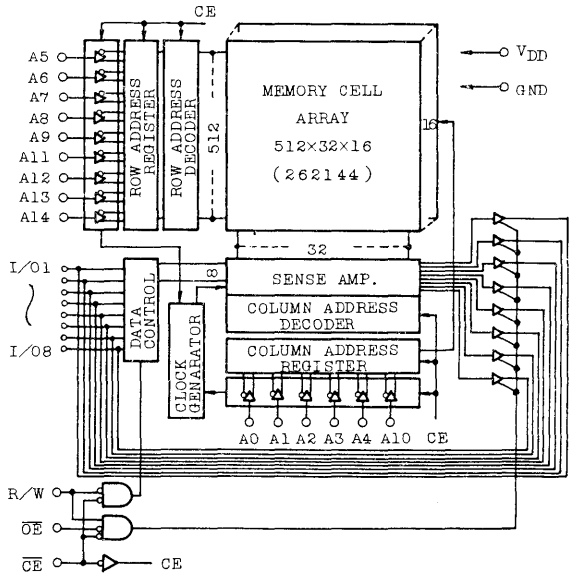
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/01 ~ I/08	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/01 ~ I/08	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{strg}	Storage Temperature	−55 ~ 150	°C
T_{opr}	Operating Temperature	0 ~ 70	°C

*) −3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3*	–	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	V

*) −3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		−1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/\overline{W} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{DD01}	Operating Current	$V_{DD} = 5.5V$ $\overline{CE} = V_{IL}$, $R/\overline{W} = V_{IH}$ Other Input $= V_{IH}/V_{IL}$ $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	–	10	–	mA
			tcycle = Min. cycle	–	–	70	
I_{DD02}		$V_{DD} = 5.5V$ $\overline{CE} = 0.2V$, $R/\overline{W} = V_{DD}-0.2V$ Other Input $= V_{DD}-0.2V/0.2V$ $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	–	5	–	mA
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		–	–	3	mA
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD}-0.2V$ $V_{DD} = 2.0 \sim 5.5V$	$Ta = 0 \sim 70°C$	–	2	100	μA

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC55257APL-85 TC55257AFL-85		TC55257APL-10 TC55257AFL-10		TC55257APL-12 TC55257AFL-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	ns
t_{ACC}	Address Access Time	–	85	–	100	–	120	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	–	120	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	–	60	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	–	60	
t_{OD0}	Output Enable to Output in High-Z	–	30	–	40	–	50	
t_{OH}	Output Data Hold Time	5	–	10	–	10	–	

Write Cycle

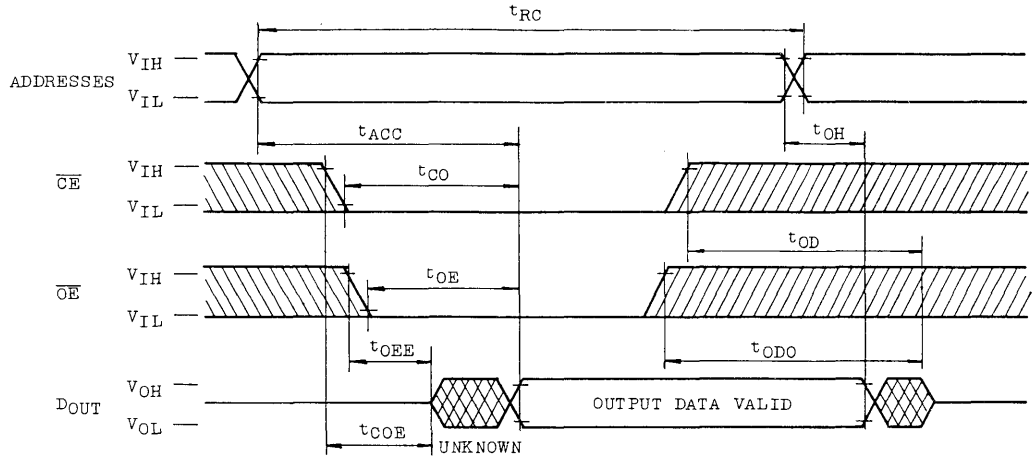
SYMBOL	PARAMETER	TC55257APL-85 TC55257AFL-85		TC55257APL-10 TC55257AFL-10		TC55257APL-12 TC55257AFL-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	120	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	80	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	100	–	
t_{AS}	Address Set up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	5	–	
t_{ODW}	R/W to Output High-Z	–	30	–	50	–	60	
t_{OEW}	R/W to Output Low-Z	10	–	10	–	10	–	
t_{DS}	Data Set up Time	40	–	40	–	50	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

A.C. TEST CONDITIONS

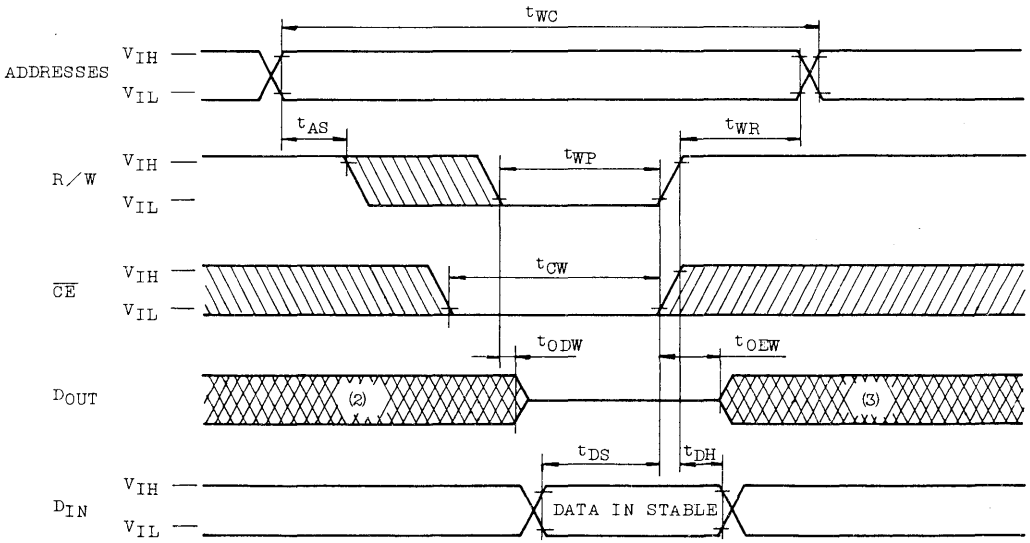
Output Load : 100pF + 1TTL Gate
Input Pulse Level : 0.6V, 2.4V
Timing Measurement : 0.8V, 2.2V
Reference Level : 0.8V, 2.2V
t_r, t_f : 5ns

TIMING WAVEFORMS

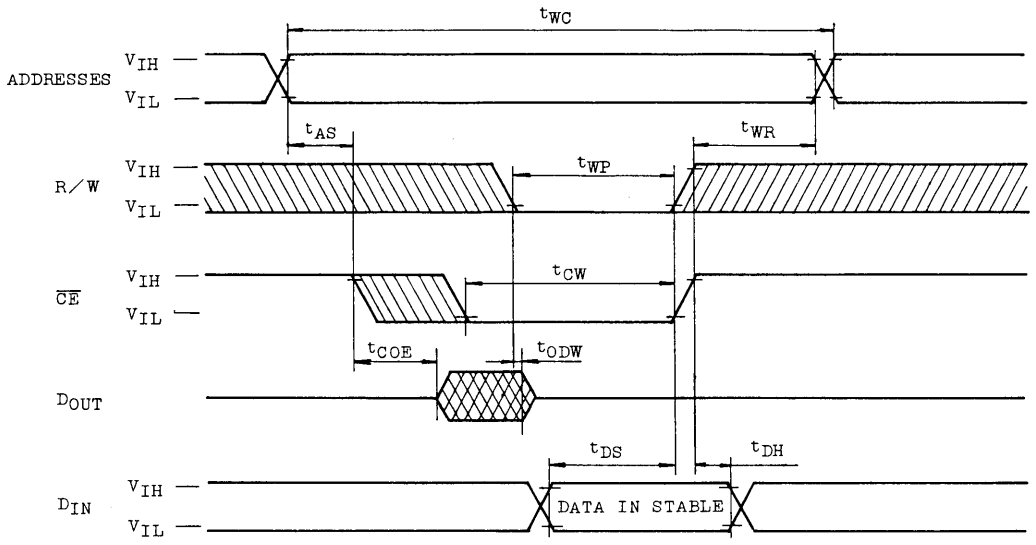
- READ CYCLE[1]



- WRITE CYCLE 1[4] (R/W Controlled Write)



- WRITE CYCLE 2[4] ($\overline{CE}$ Controlled Write)



NOTE: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Output remain in a high impedance state.

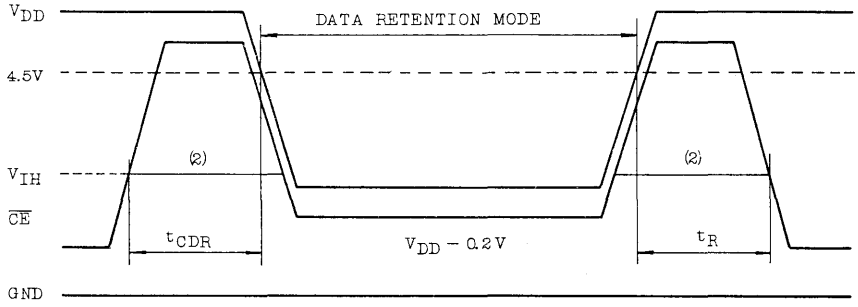
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	–	–	50	μA
		V_{DH} = 5.5V	–	–	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μs
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time.

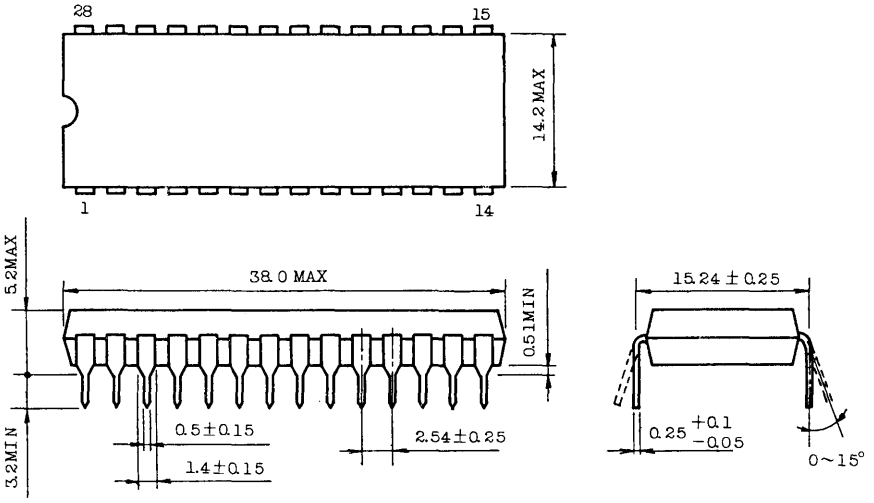
- $\overline{CE}$ Controlled Data Retention Mode



NOTE (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

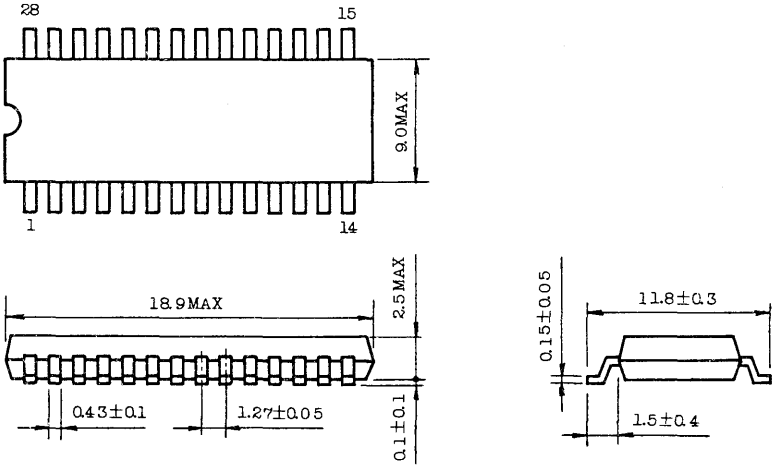
- DIP 28 PIN OUTLINE DRAWING (6D28A-P)

Unit in mm



NOTE: Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

- MFP 28 PIN OUTLINE DRAWING (F28GA-P)



NOTE: Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

32,768 WORD×8 BIT STATIC RAM
SILICON GATE CMOS

TC55257APL-85L/APL-10L/APL-12L
TC55257AFL-85L/AFL-10L/AFL-12L

PRELIMINARY

DESCRIPTION

The TC55257APL/AFL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA (Ta = 25°C). The TC55257APL/AFL has two control inputs. Chip enable ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC55257APL/AFL is offered in both a standard dual-in-line 28 pins plastic package (0.6 inch width) and small-out-line plastic flat package.

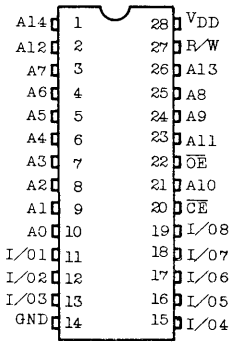
FEATURES

- Low Power Dissipation
  27.5mW/MHz (Typ.) Operating
- Standby Current
  2μA (Max.): TC55257APL-85L/AFL-85L
  (Ta = 25°C) APL-10L/AFL-10L
  APL-12L/AFL-12L
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC55257APL-85L TC55257AFL-85L	TC55257APL-10L TC55257AFL-10L	TC55257APL-12L TC55257AFL-12L
Access Time (Max.)	85ns	100ns	120ns
Chip Enable Access Time (Max.)	85ns	100ns	120ns
Output Enable Time (Max.)	45ns	50ns	60ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package

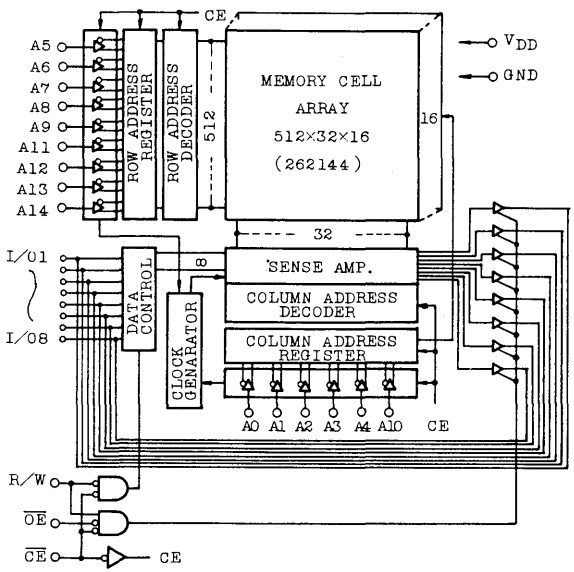
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/01 ~ I/08	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/01 ~ I/08	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature • Time	260 • 10	°C • sec
T_{strg}	Storage Temperature	−55 ~ 150	°C
T_{opr}	Operating Temperature	0 ~ 70	°C

*) −3.0V at pulse width 50ns

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3*	–	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	V

*) −3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		−1.0	–	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	–	–	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		–	–	± 1.0	μA
I_{DD01}	Operating Current	$V_{DD} = 5.5V$ $\overline{CE} = V_{IL}$, $R/W = V_{IH}$ Other Input $= V_{IH}/V_{IL}$ $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	–	10	–	mA
			t_{cycle} = Min. cycle	–	–	70	
I_{DD02}		$V_{DD} = 5.5V$ $\overline{CE} = 0.2V$, $R/W = V_{DD}-0.2V$ Other Input $= V_{DD}-0.2V/0.2V$ $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	–	5	–	mA
			t_{cycle} = Min. cycle	–	–	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		–	–	3	mA
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD}-0.2V$ $V_{DD} = 2.0 \sim 5.5V$	$Ta = 0 \sim 70°C$	–	–	30	μA
			$Ta = 25°C$	–	–	2	

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC55257APL-85L TC55257AFL-85L		TC55257APL-10L TC55257AFL-10L		TC55257APL-12L TC55257AFL-12L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	ns
t_{ACC}	Address Access Time	–	85	–	100	–	120	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	–	120	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	–	60	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	10	–	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	–	60	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	–	50	
t_{OH}	Output Data Hold Time	5	–	10	–	10	–	

Write Cycle

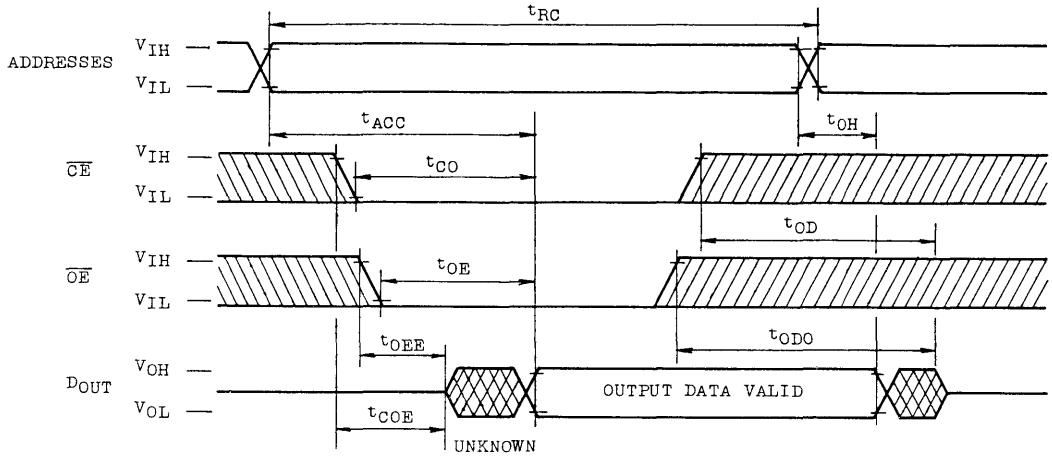
SYMBOL	PARAMETER	TC55257APL-85L TC55257AFL-85L		TC55257APL-10L TC55257AFL-10L		TC55257APL-12L TC55257AFL-12L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	120	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	80	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	100	–	
t_{AS}	Address Set up Time	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	5	–	
t_{ODW}	R/W to Output High-Z	–	30	–	50	–	60	
t_{OEW}	R/W to Output Low-Z	10	–	10	–	10	–	
t_{DS}	Data Set up Time	40	–	40	–	50	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	

A.C. TEST CONDITIONS

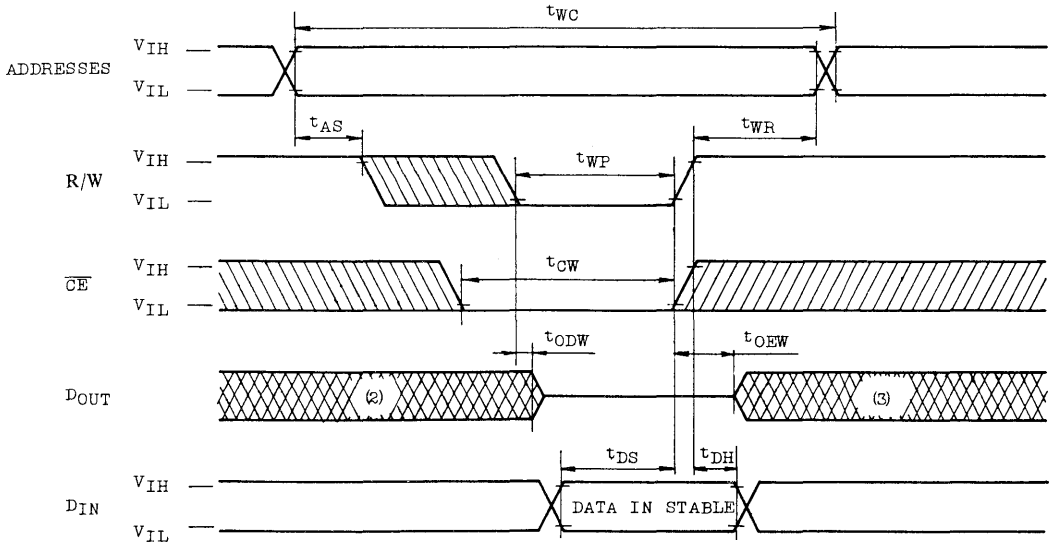
Output Load : 100pF + 1TTL Gate
Input Pulse Level : 0.6V, 2.4V
Timing Measurement : 0.8V, 2.2V
Reference Level : 0.8V, 2.2V
t_r , t_f : 5ns

TIMING WAVEFORMS

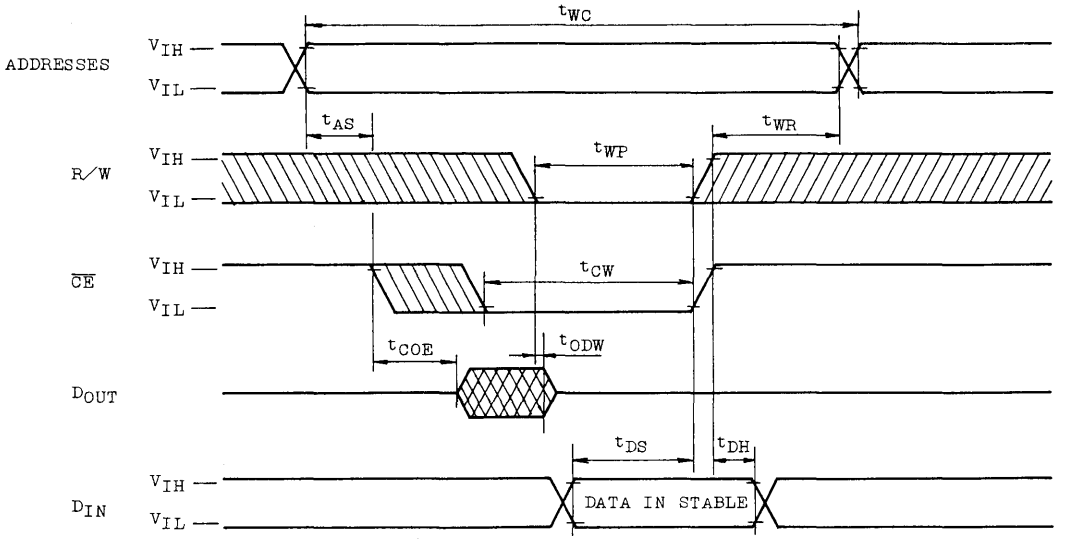
- READ CYCLE[1]



- WRITE CYCLE 1[4] (R/W Controlled Write)



- WRITE CYCLE 2[4] ($\overline{CE}$ Controlled Write)



NOTE: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

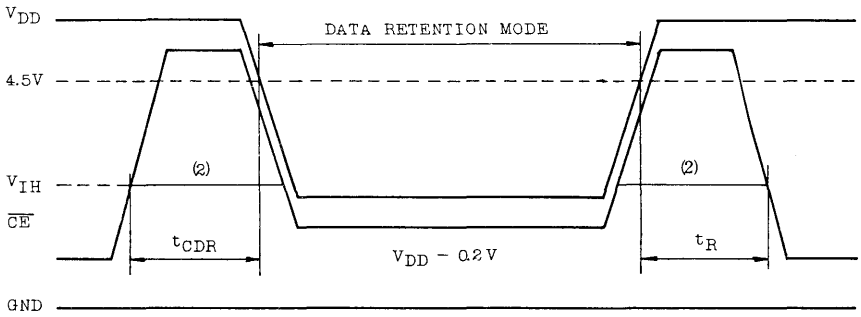
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	–	–	20	μA
		V_{DH} = 5.5V	–	–	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μs
t_R	Recovery Time		$t_{RC(1)}$	–	–	

Note (1): Read Cycle Time.

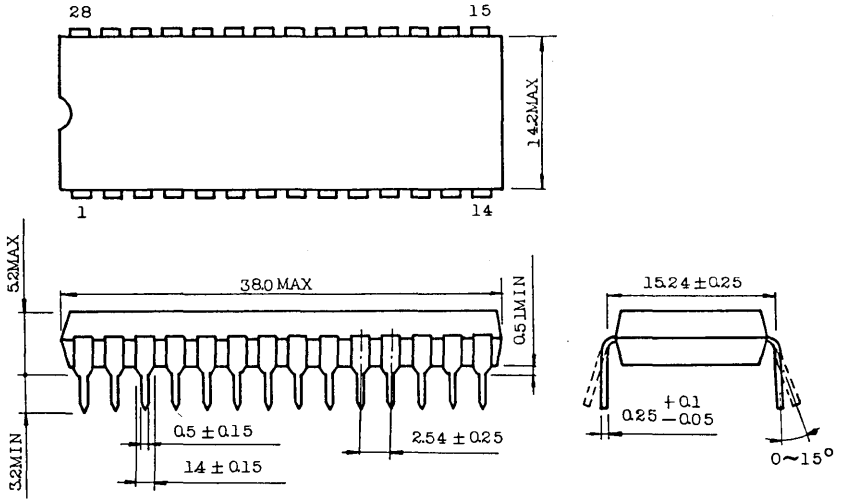
- $\overline{CE}$ Controlled Data Retention Mode



NOTE (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

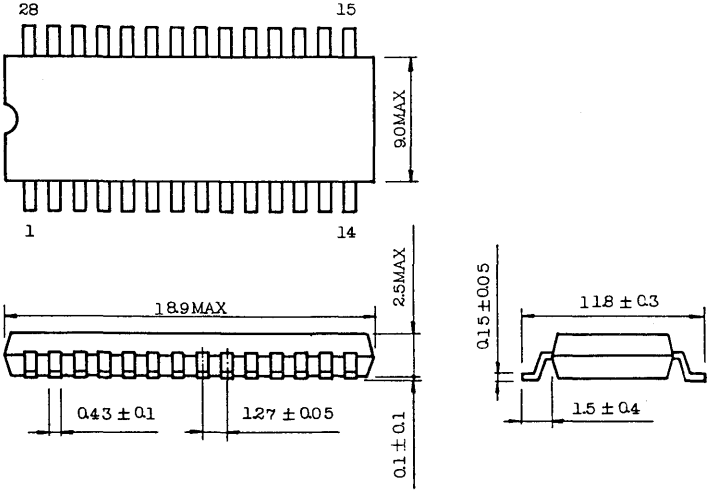
- DIP 28 PIN OUTLINE DRAWING (6D28A-P)

Unit in mm



NOTE: Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

- MFP 28 PIN OUTLINE DRAWING (F28GA-P)



NOTE: Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Preliminary

TC55256PL-10/PL-12/PL-15
TC55256FL-10/FL-12/FL-15

DESCRIPTION

The TC55256PL/FL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz(TYP.) and minimum cycle time of 100ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.01μA typically. The TC55256PL/FL has two control inputs. Chip enable ($\overline{CE}$) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55256PL/FL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. Ultra low standby power allow not only battery but capacitance backup. The TC55256PL/FL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

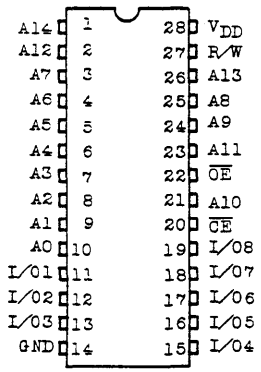
FEATURES

- Low Power Dissipation
  27.5mW/MHz(TYP.) Operating
- Standby Current
  0.2μA(MAX.) at Ta=25°C
  1.0μA(MAX.) at Ta=60°C
  10.0μA(MAX.) at Ta=85°C
- 5V Single Power Supply
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Access Time

	TC55256PL -10/FL-10	TC55256PL -12/FL-12	TC55256PL -15/FL-15
Access Time (Max.)	100ns	120ns	150ns
Chip Enable Access Time (Max.)	100ns	120ns	150ns
Output Enable Time(Max.)	50ns	60ns	70ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package
- Wide Temperature Operation: -40 ∿ 85°C

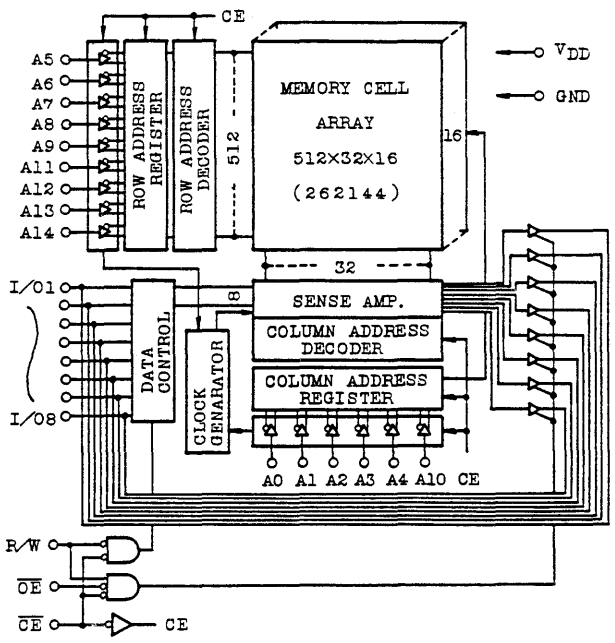
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 ∿ I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*) H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-0.3* ∿ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	1.0 (0.6)**	W
T_{solder}	Soldering Temperature	260 • 10	°C•sec
T_{strg}	Storage Temperature	-55 ∿ 150	°C
T_{opr}	Operaring Temperature	-40 ∿ 85	°C

*) -3.0V at pulse width 50ns
**) SOP

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=-40 ∿ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

*) -3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS

($Ta=-40 \sim 85°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		4.0	-	-	mA
V_{OH}	Output High Voltage	$I_{OH}=-20\mu A$		V_{DD} -0.1	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=20\mu A$		-	-	0.1	V
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $R/\overline{W}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current (Read Cycle)*	$V_{DD}=5.5V$, $\overline{CE}=V_{IL}$, $R/\overline{W}=V_{IH}$ Other Input= V_{IH}/V_{IL}, $I_{OUT}=0mA$	$t_{cycle}=1\mu s$	-	10	-	mA
			t_{cycle}= Min. cycle	-	-	70	
I_{DDO2}		$V_{DD}=5.5V$, $\overline{CE}=0.2V$, $R/\overline{W}=V_{DD}-0.2V$ Other Input= $V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	$t_{cycle}=1\mu s$	-	5	-	mA
			t_{cycle}= Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE}=V_{DD}-0.2V$ $V_{DD}=2.0 \sim 5.5V$	Ta=25°C	-	0.01	0.2	μA
			Ta=60°C	-	-	1.0	
			Ta=85°C	-	-	10.0	

* Assuming that R/W is Low for Write Cycle, the current consumption is twice as much as that when R/W is high for Write Cycle.

CAPACITANCE

($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS

($Ta=-40 \sim 85°C$, $V_{DD}=5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55256PL -10/FL-10		TC55256PL -12/FL-12		TC55256PL -15/FL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO}	$\overline{CE}$ Access Time	-	100	-	120	-	150	
t_{OE}	Output Enable to Output in Valid	-	50	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low-Z	5	-	5	-	5	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	-	50	-	60	-	70	
t_{ODO}	Output Enable to Output in High-Z	-	40	-	50	-	60	
t_{OH}	Output Data Hold Time	10	-	10	-	15	-	

WRITE CYCLE

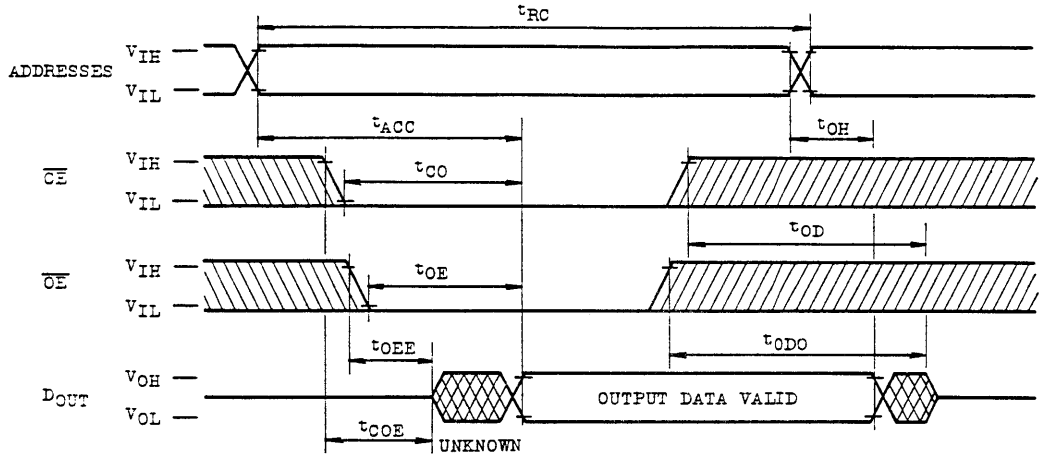
SYMBOL	PARAMETER	TC55256PL -10/FL-10		TC55256PL -12/FL-12		TC55256PL -15/FL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	70	-	80	-	100	-	
t_{CW}	Chip Selection to End of Write	90	-	100	-	120	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	50	-	60	-	70	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	5	-	
t_{DS}	Data Set Up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

AC TEST CONDITION

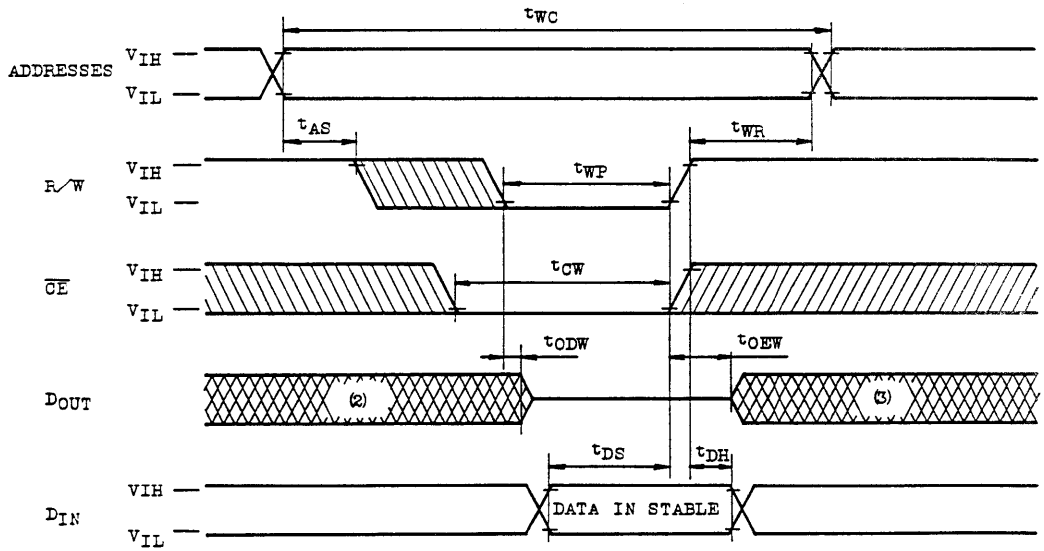
- Input Pulse Levels : 2.4V/0.6V
- Timing Measurement Reference Levels: 2.2V/0.8V
- Output Reference Levels : 2.2V/0.8V
- Input Pulse Rise and Fall Time : 5ns
- Output Load : 100pF + 1TTL Gate

TIMING WAVEFORMS

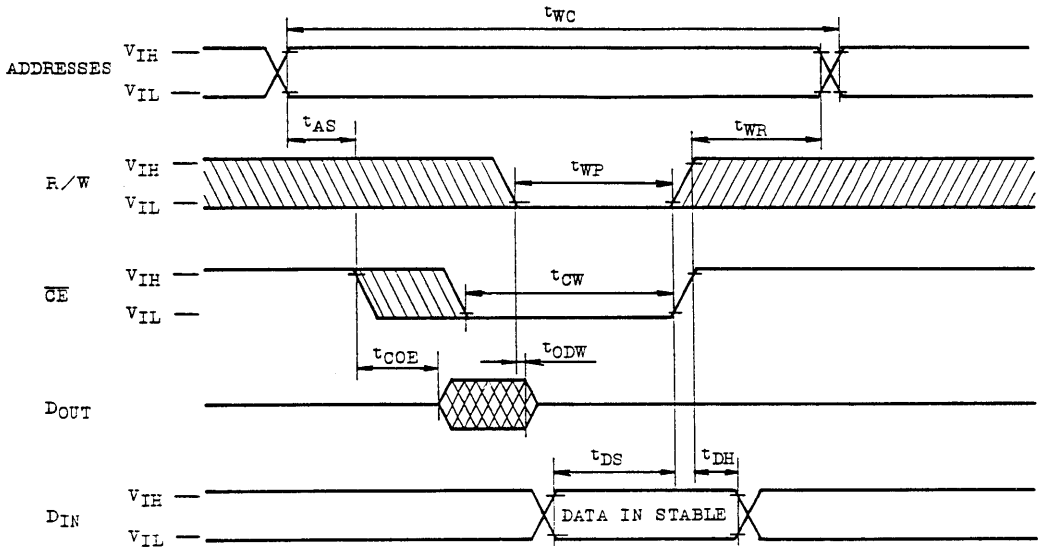
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

3V OPERATE SPECIFICATION

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=-10 ∿ 60°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	2.7	3.0	3.3	V
V_{IH}	Input High Voltage	V_{DD}-0.2	-	V_{DD}	V
V_{IL}	Input Low Voltage	0	-	0.2	V

D.C. and OPERATING CHARACTERISTICS (Ta=-10 ∿ 60°C)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{IN}	Input Leakage Current	V_{IN}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or R/W=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0 ∿ V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=V_{DD}-0.2V		-100	-	-	μA
I_{OL}	Output Low Current	V_{OL}=0.2V		100	-	-	μA
V_{OH}	Output High Voltage	I_{OH}=-20μA		V_{DD}-0.1	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=20μA		-	-	0.1	V
I_{DDO}*	Operating Current	$\overline{CE}$=V_{IL} Other input= V_{DD}-0.2V/0.2V I_{OUT}=0mA, duty 100%	t_{cycle} =1μs	-	3.0	5.0	mA
I_{DDS}	Standby Current	$\overline{CE}$=V_{IH}	Ta=25°C	-	0.01	0.2	μA
			Ta=60°C	-	-	1.0	

All voltage is measured from GND.

* I_{DDO} is slightly depending on input pulse t_r, t_f. If long t_r, t_f pulse is applied, there are some transient current at input stage. These specification is guaranteed with t_r, $t_f \leq$ 20ns.

3V OPERATE SPECIFICATION

A.C. CHARACTERISTICS

($Ta=-10 \sim 60°C$, $V_{DD}=3V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{RC}	Read Cycle Time	1000	-	-	ns
t_{ACC}	Address Access Time	-	300	1000	
t_{CO}	CE Access Time	-	300	1000	
t_{OE}	Output Enable to Output Valid	-	150	500	
t_{OH}	Output Data Hold Time	20	-	-	
t_{COE}	Chip Enable to Output in Low Z	10	-	-	
t_{OEE}	Output Enable to Output in Low Z	5	-	-	
t_{OD}	Chip Enable to Output in High Z	-	-	200	
t_{ODO}	Output Enable to Output in High Z	-	-	150	

WRITE CYCLE

SYMBOL	PARAMETER	MIN.	TYP.*	MAX.	UNIT
t_{WC}	Write Cycle Time	1000	-	-	ns
t_{WP}	Write Pulse Width	500	-	-	
t_{CW}	Chip Selection to End of Write	800	-	-	
t_{AS}	Address Set Up Time	100	-	-	
t_{WR}	Write Recovery Time	100	-	-	
t_{DS}	Data Set Up Time	400	-	-	
t_{DH}	Data Hold Time	50	-	-	
t_{ODW}	R/W to Output High Z	-	-	200	
t_{OEW}	R/W to Output Low Z	10	-	-	

* Type. condition is $Ta=25°C$, $V_{DD}=3V$

A.C. TEST CONDITIONS

- $V_{IN}=V_{DD}-0.2V/0.2V$
- Output Reference Level : 1.5V/1.5V
- Timing Measurement Level : 1.5V/1.5V
- Input Pulse Rise and Fall Time: ≦20ns
- Output Load : 100pF (Include Jig)

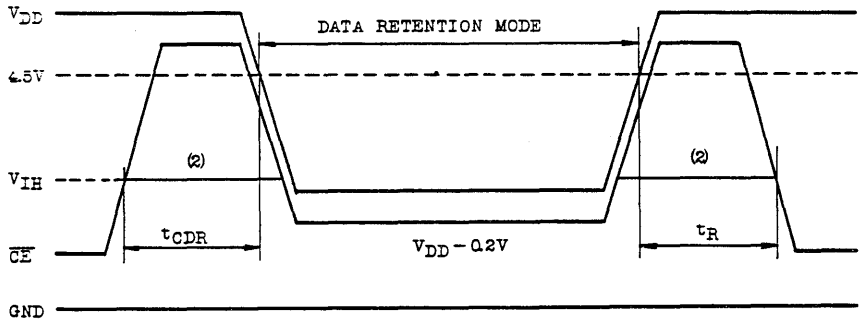
DATA RETENTION CHARACTERISTICS (Ta=-40 ~ 85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	Ta=25°C	-	0.01	0.2	μA
		Ta=60°C	-	-	1.0	
		Ta=85°C	-	-	10.0	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μS
t_R	Recovery Time		t_{RC}(1)	-	-	

Note: (1) Read cycle time.

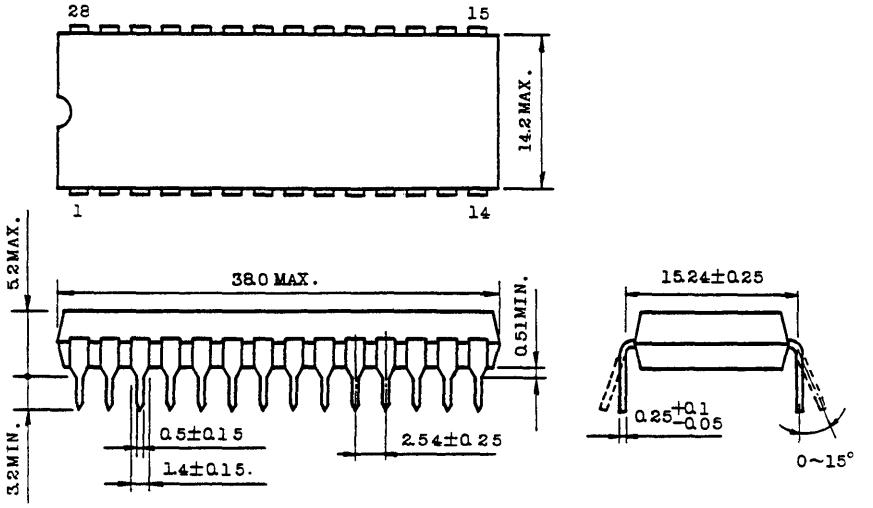
(2) If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

$\overline{CE}$ Controlled Data Retention Mode



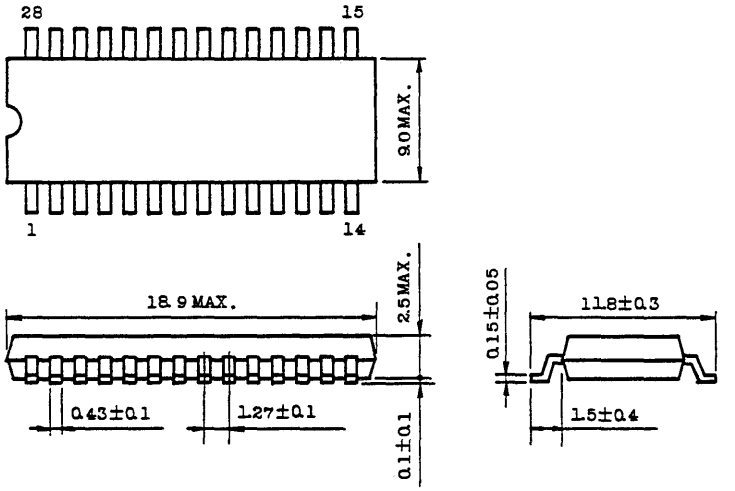
DIP 28 PIN OUTLINE DRAWING (DIP28-P-600)

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

SOP 28 PIN OUTLINE DRAWING (SOP28-P-450)



Mote: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

Preliminary

TC55258PL-10/PL-12/PL-15
TC55258FL-10/FL-12/FL-15

DESCRIPTION

The TC55258PL/FL is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a operating current of 5mA/MHz (TYP.) and minimum cycle time of 100ns. The TC55258PL/FL has two control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control. When the device is placed in standby mode, the standby current is typically 0.01μA. Thus the TC55258PL/FL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. Ultra low standby power allow not only battery but capacitance backup. The TC55258PL/FL is offered in both a standard dual-in-line 28 pin plastic package (0.6 inch width) and small-out-line plastic flat package.

flat package.

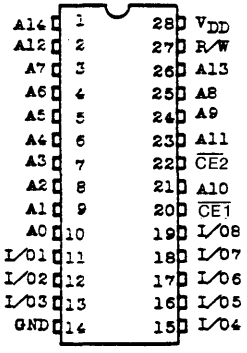
FEATURES

- Low Power Dissipation
  27.5mW/MHz(TYP.) Operating
- Standby Current
  0.2uA(MAX.) at Ta=25°C
  1.0uA(MAX.) at Ta=60°C
  10.0uA(MAX.) at Ta=85°C
- 5V Single Power Supply
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC55258PL -10/FL-10	TC55258PL -12/FL-12	TC55258PL -15/FL-15
Access Time (Max.)	100ns	120ns	150ns
Chip Enable Access Time (Max.)	100ns	120ns	150ns
Output Enable Time(Max.)	50ns	60ns	70ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP and Plastic Flat Package
- Wide Temperature Operation: -40 ~ 85°C

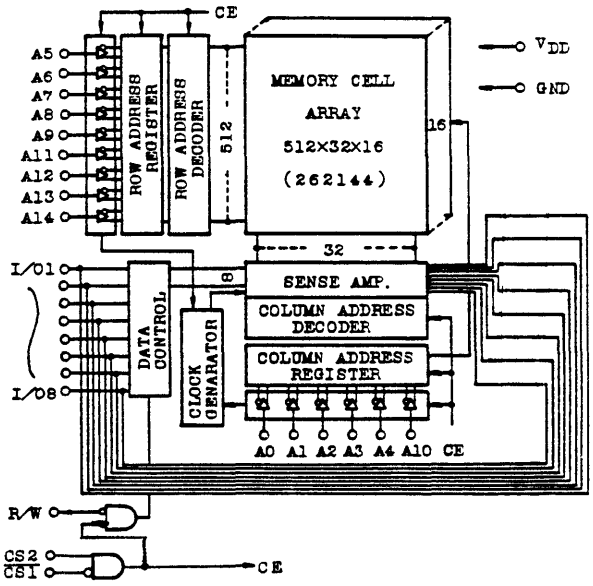
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A14	Address Inputs
R/W	Read/Write Control Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Input/Output
VDD	Power (+5V)
GND	Ground

BLOCK DIAGRAM



TOSHIBA MOS MEMORY PRODUCTS

Preliminary **TC551001PL-70/PL-85/PL-10**

DESCRIPTION

The TC551001PL is 1,048,576 bits static random access memory organized as 131,072 words by 8bits using CMOS technology,and operated a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz(Typ.) and minimum cycle time of 70/85/100ns. When $\overline{CE1}$ is a logical high or CE2 is low, the device is placed in low power standby mode in which standby current is 2uA typically.The TC551001PL has three control inputs.Chip enable inputs($\overline{CE1}$,CE2) allow for device selection and data retention control,and an output enable input ($\overline{OE}$) provides fast memory access.Thus the TC551001PL is suitable for use in various microprocessor application system where high speed,low power,and battery back up are required.

The TC551001PL is offered in a dual-in-line 32pin standard plastic package.

FEATURES

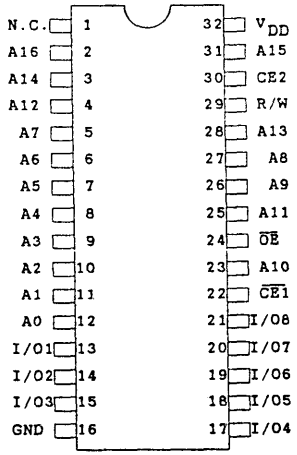
- Low Power Dissipation
  27.5mW/MHz(Typ.)
- Standby Current:100uA(Max.)
- 5V Single Power Supply
- Power Down Feature:$\overline{CE1}$,CE2
- Data Retention Supply Voltage
  :2.0~5.5V

- Access Time

	TC551001PL-70	TC551001PL-85	TC551001PL-10
Access Time(Max.)	70ns	85ns	100ns
$\overline{CE1}$ Access Time(Max.)	70ns	85ns	100ns
CE2 Access Time(Max.)	70ns	85ns	100ns
$\overline{OE}$ Access Time(Max.)	35ns	45ns	50ns

- Directly TTL Compatible : All Inputs and Outputs

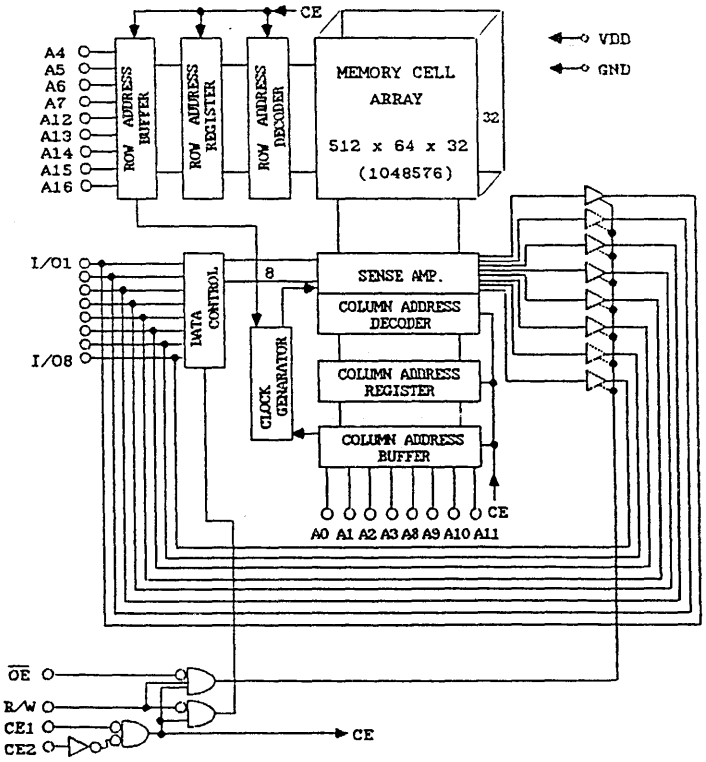
PIN CONNECTION (TOP VIEW)



PIN NAMES

$A_0 \sim A_{16}$	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Inputs
$I/O_1 \sim I/O_8$	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	*	*	H	*	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ~ 7.0	V
V_{IN}	Input Voltage	-0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature	260 • 10	°C•sec
$T_{strg.}$	Storage Temperature	-55 ~ 150	°C
Topr	Operating Temperature	0 ~ 70	°C

* : -3.0V at pulse width 50ns MAX.

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3*	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

* : -3.0V at pulse width 50ns MAX.

D.C. and OPERATING CHARACTERISTICS (Ta=0 ~ 70°C, VDD=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0 ~ V_{DD}	-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0 ~ V_{DD}	-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1}$=VIL and CE2=VIH and R/W=V_{IH}, I_{OUT}=0mA Other Input=V_{IH}/V_{IL} tcycle=Min.cycle	-	-	60	mA
I_{DDO2}		$\overline{CE1}$=0.2V and CE2=V_{DD}-0.2V R/W=V_{DD}-0.2V, I_{OUT}=0mA Other Input=V_{DD}-0.2V/0.2V tcycle=Min.cycle	-	-	70	mA
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}	-	-	3	mA
I_{DDS2}		$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V V_{DD}=2.0V ~ 5.5V, Ta=0 ~ 70°C	-	-	100	μA

CAPACITANCE (Ta=25°C f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CARACTERISTICS (Ta=0 ~ 70°C, VDD=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-70		TC551001PL-85		TC551001PL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tRC	Read Cycle Time	70	-	85	-	100	-	ns
tACC	Address Access Time	-	70	-	85	-	100	
tCO1	$\overline{CE1}$ Access Time	-	70	-	85	-	100	
tCO2	CE2 Access Time	-	70	-	85	-	100	
tOE	Output Enable to Output in Valid	-	35	-	45	-	50	
tCOE	Chip Enable ($\overline{CE1}$,CE2)to Output in Low-Z	5	-	10	-	10	-	
tOEE	Output Enable to Output in Low-Z	0	-	5	-	5	-	
tOD	Chip Enable ($\overline{CE1}$,CE2)to Output in High-Z	-	30	-	30	-	35	
tODO	Output Enable to Output in High-Z	-	30	-	30	-	35	
tOH	Output Data Hold Time	5	-	10	-	10	-	

Write Cycle

SYMBOL	PARAMETER	TC551001PL-70		TC551001PL-85		TC551001PL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	-	85	-	100	-	ns
t_{WP}	Write Pulse Width	45	-	50	-	60	-	
t_{CW}	Chip Selection to End of Write	55	-	70	-	80	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	30	-	35	-	40	
t_{OEW}	R/W to Output Low-Z	0	-	0	-	5	0	
t_{DS}	Data Set up Time	30	-	30	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

D.C. TEST CONDITION

Output Load : 100pF + 1 TTL Gate

Input Pulse Level : 0.6V, 2.4V

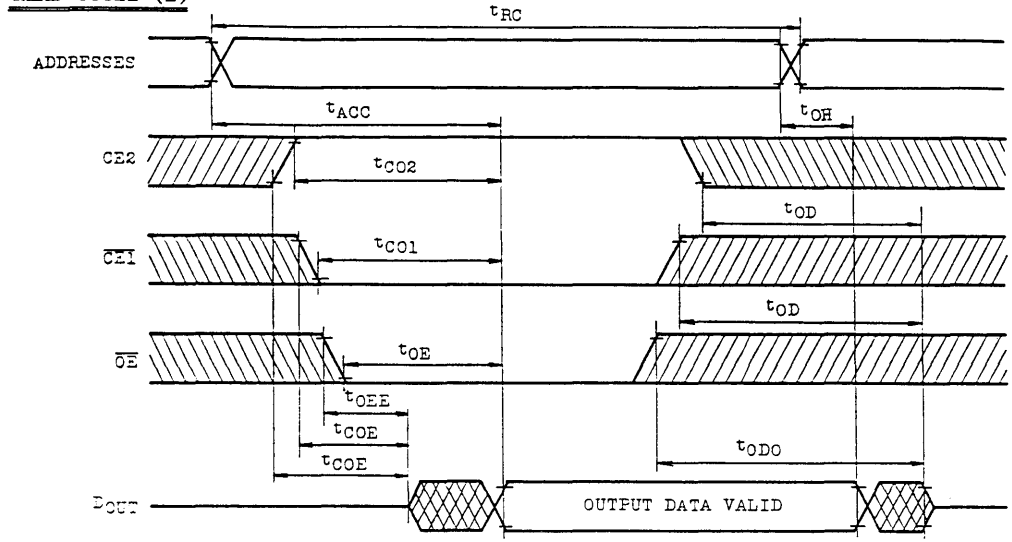
Timing Measurement V_{IN} : 0.8V, 2.2V

Reference Level V_{OUT} : 0.8V, 2.2V

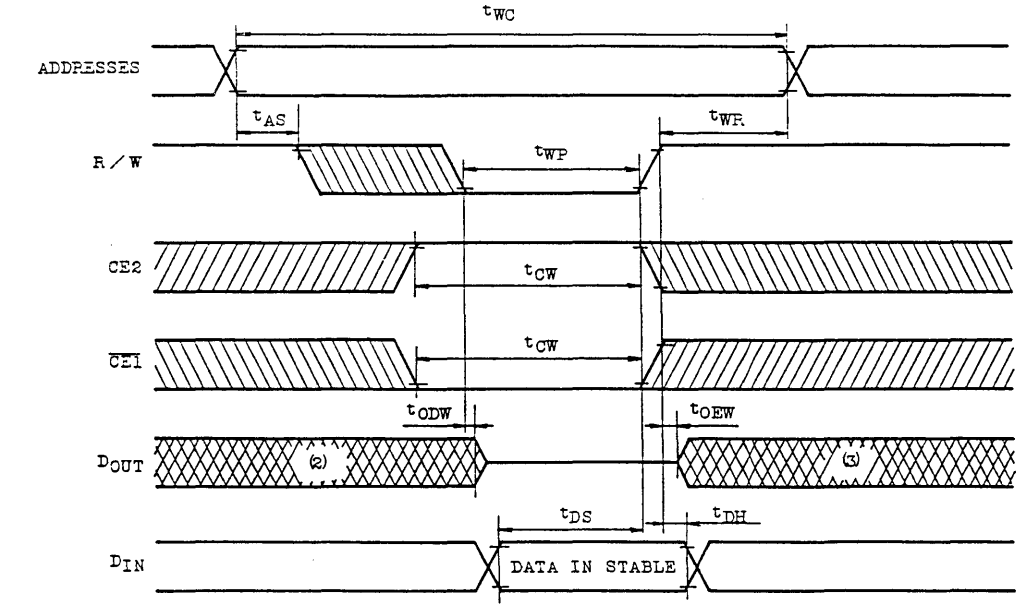
t_r, t_f : 5ns

TIMING WAVEFORMS

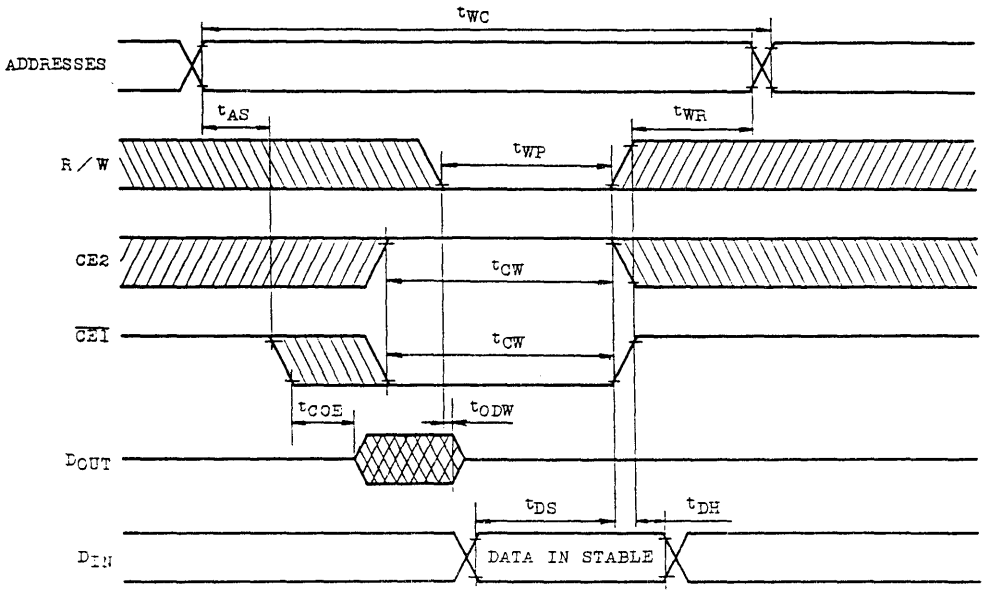
READ CYCLE (1)



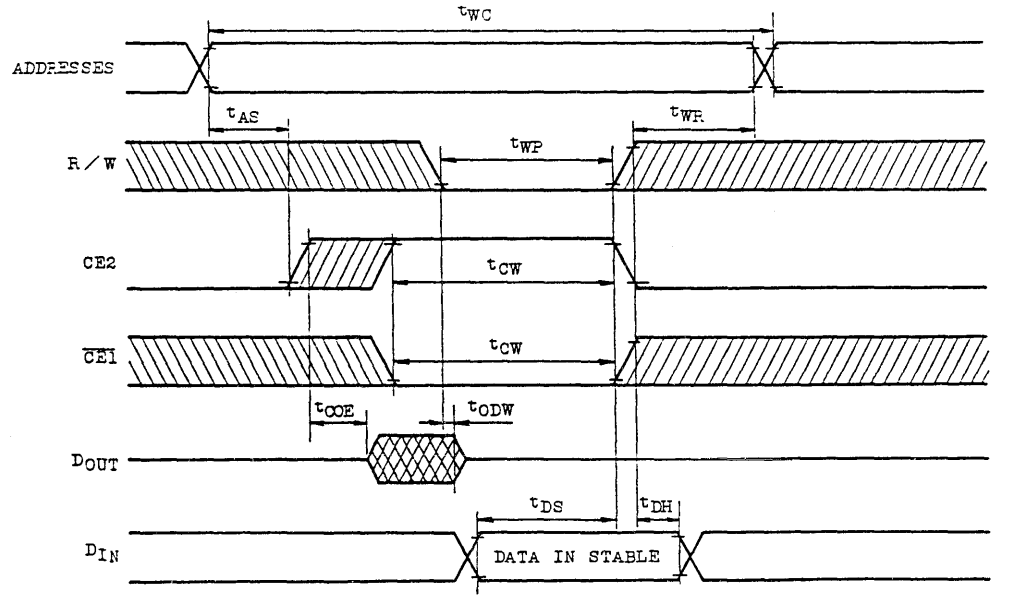
WRITE CYCLE 1 (R/W Controlled Write)



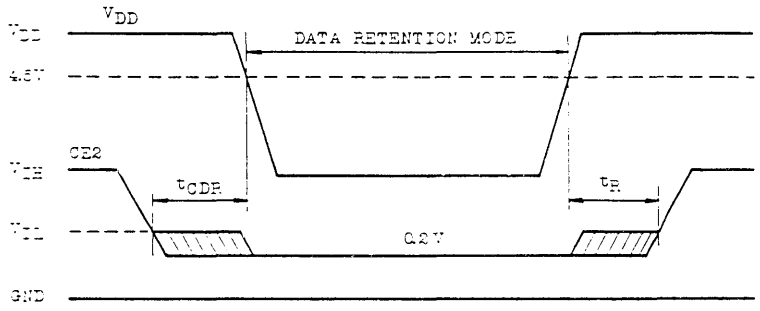
WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



CE2 Controlled Data Retention Mode (4)



NOTE: (1) t_{RC}: Read Cycle Time

(2) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq V_{DD}$-0.2V.

(3) If the V_{IH} of $\overline{CE1}$ is 2.2V in operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(4) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

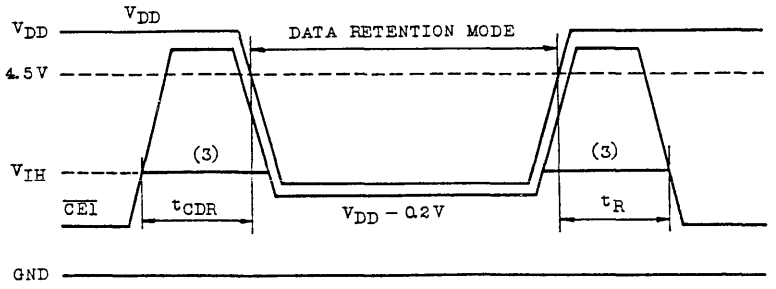
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ~ 70°C)

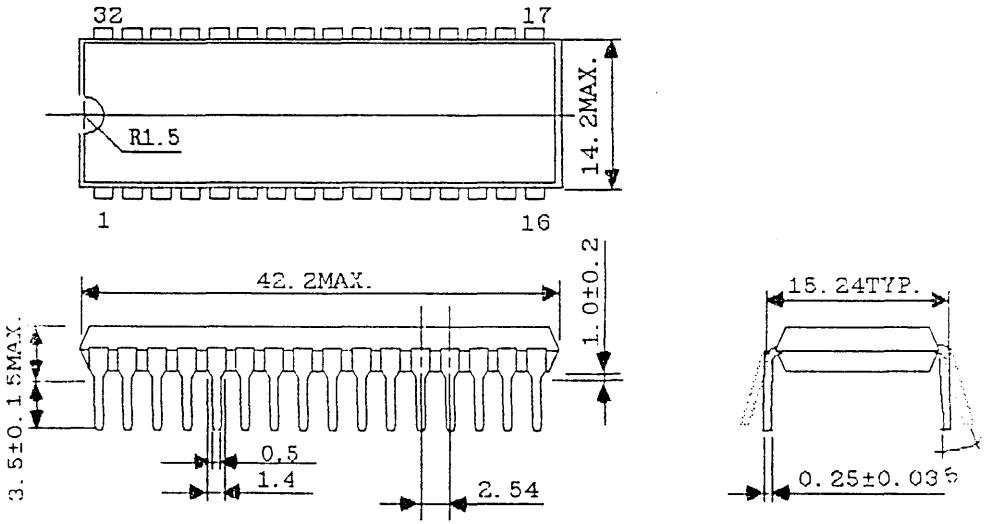
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	–	5.5	V
I_{DDS2}	Standby Current	V_{DD}=3.0V	–	–	50	μA
		V_{DD}=5.5V	–	–	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	–	–	μS
t_R	Recovery Time		tRC(1)	–	–	nS

$\overline{CE1}$ Controlled Data Retention Mode (2)



DIP 32 PIN OUTLINE DRAWING

Unit in mm



Note:Lead pitch is 2.54 and tolerance is +0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.32 leads.

Pseudo-Static RAMs

32,768 WORD×8 BIT CMOS PSEUDO STATIC RAM

SILICON GATE CMOS

TC51832P/SP/F-85, TC51832P/SP/F-10 TC51832P/SP/F-12

DESCRIPTION

The TC51832P/SP/F is a 256K high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832P/SP/F utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. System oriented features include single power supply of 5V ± 10% tolerance. The $\overline{OE}$/$\overline{RFSH}$ input allows two types of refresh operation — auto refresh and self refresh. The TC51832P/SP/F also features static RAM like write function that the input data is written into the memory cell at the rising edge of R/$\overline{W}$, thus being easy to interface with microprocessor. The TC51832P/SP/F is a pin-compatible with 256K bit CMOS static RAM — TC55257P and is moulded a standard 0.6 inch and 0.3 inch width plastic DIP and small-out line plastic flat package.

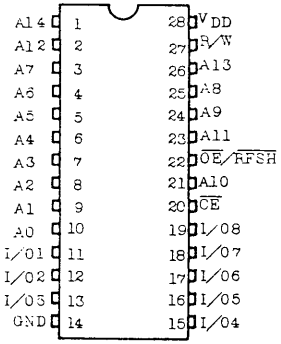
FEATURES

- Organization: 32,768 word x 8 bit
- Fast Access Time and Cycle Time

		TC51832P/SP/F-85	TC51832P/SP/F-10	TC51832P/SP/F-12
t_{CEA}	$\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA}	$\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC}	Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V ± 10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  Operating: (Max.)
  303mW (TC51832P/SP/F-85)
  248mW (TC51832P/SP/F-10)
  220mW (TC51832P/SP/F-12)
  Standby: 5.5mW (Max.)
  Self Refresh: 5.5mW (Max.)
- Two types of Refresh Operation Capability
  Auto Refresh
  Self Refresh
- Pin Compatible with 256K bit CMOS Static RAM TC55257P

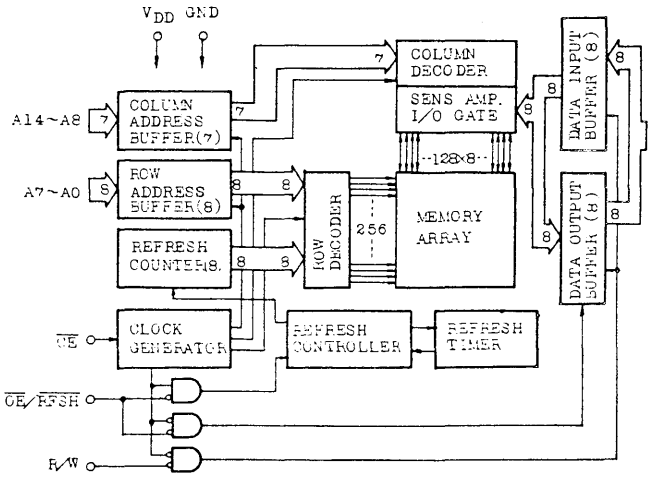
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
R/$\overline{W}$	Read/Write Control Input
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/01 ~ I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	−1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	−1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	−1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STG}	Storage Temperature	−55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature•Time	260•10	°C•sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{DD0}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{CE}$, Address Cycling: t_{RC} = t_{RC}MIN)	TC51832P/SP/F-85	–	55	mA	3, 4
		TC51832P/SP/F-10	–	45		
		TC51832P/SP/F-12	–	40		
I_{DDS1}	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ($\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH})		–	1	mA	
I_{DDF}	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ($\overline{CE}$ = V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$ = 0.2V)		–	1	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ V_{DD}, All Other Inputs not under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≤ V_{OUT} ≤ V_{DD})		−10	10	μA	
V_{OH}	OUTPUT HIGH LEVEL Output "H" Level Voltage (I_{OUT}=−5mA)		2.4	–	V	
V_{OL}	OUTPUT LOW LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTCS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832P/SP/F-85		TC51832P/SP/F-10		TC51832P/SP/F-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	160	–	190	–	ns	
t_{RMW}	Read Write Cycle Time	200	–	240	–	280	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	85	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	–	10	–	10	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	R/W to Output in Low-Z	0	–	0	–	0	–	ns	
t_{CHZ}	$\overline{CE}$ to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHZ}	$\overline{OE}$ to Output in High-Z	0	25	0	30	0	35	ns	10
t_{WHZ}	R/W to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	–	70	–	85	–	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	–	70	–	85	–	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	–	40	–	50	–	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	–	40	–	50	–	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	–	0	–	0	–	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	11
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	12
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	12
t_{FC}	Auto Refresh Cycle Time	135	–	160	–	190	–	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	13
t_{FCE}	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	–	190	–	225	–	ns	13
t_{FSR}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Auto Refresh Cycle)	65	–	80	–	95	–	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	–	8,000	–	8,000	–	ns	13
t_{FRS}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	–	190	–	225	–	ns	13
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{T}	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ~ A14)	–	5	pF
CI2	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	–	7	pF
CI0	Input/Output Capacitance (I/O1 ~ I/O8)	–	7	pF

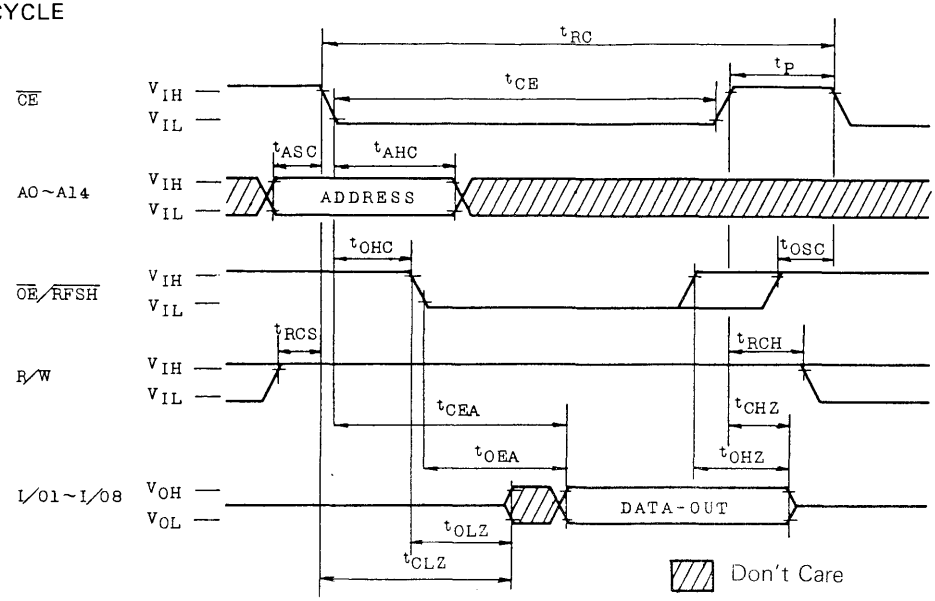
NOTE: This parameter is periodically sampled and is not 100% tested.

NOTES:

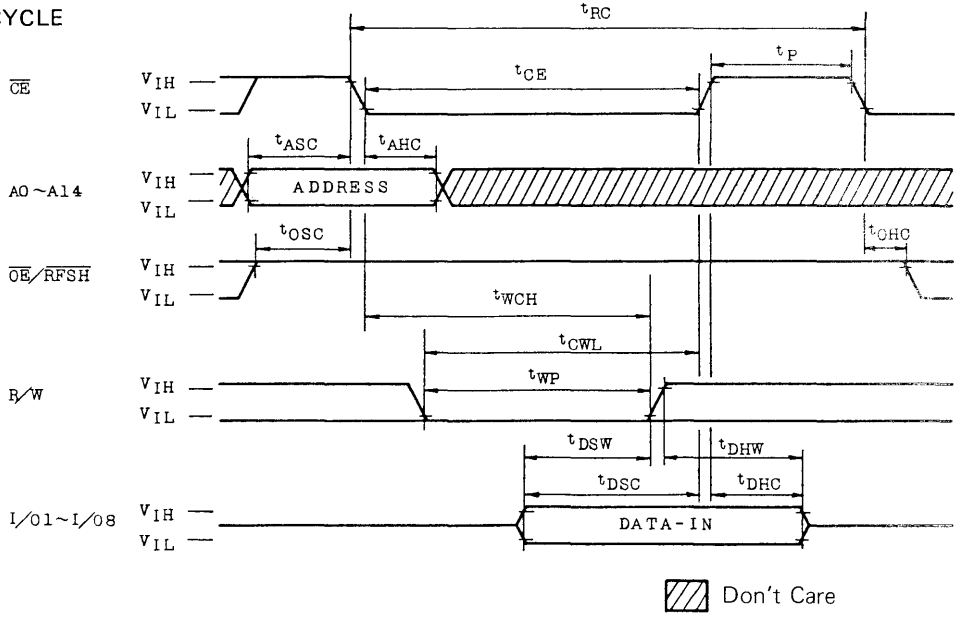
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are reference to GND.
3. I_{DDO} depend on cycle rate.
4. I_{DDO} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}$/$\overline{RFSH}$ is required after power-up before proper device operation is achieved.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
8. Measured with a load equivalent to 2 TTL laods and 100pF.
9. The $\overline{OE}$/$\overline{RFSH}$ input operates as the output enable input ($\overline{OE}$) and refresh control input ($\overline{RFSH}$) under the condition of that $\overline{CE}$ = V_{IL} and $\overline{CE}$ = V_{IH} , respectively.
10. t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
11. In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).
12. All address are latched at the falling edge of $\overline{CE}$, and must be valid during t_{ASC} and t_{AHC} .
13. Two refresh operation – auto refresh and self refresh are determined by the $\overline{OE}$/$\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH} .
    Auto refresh: $\overline{OE}$/$\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh: $\overline{OE}$/$\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The following timing parameter must be kept before device proper operation is achieved after refresh.
    Auto refresh: t_{FCE} and t_{FSR}
    Self refresh: t_{FRS}

TIMING WAVEFORMS

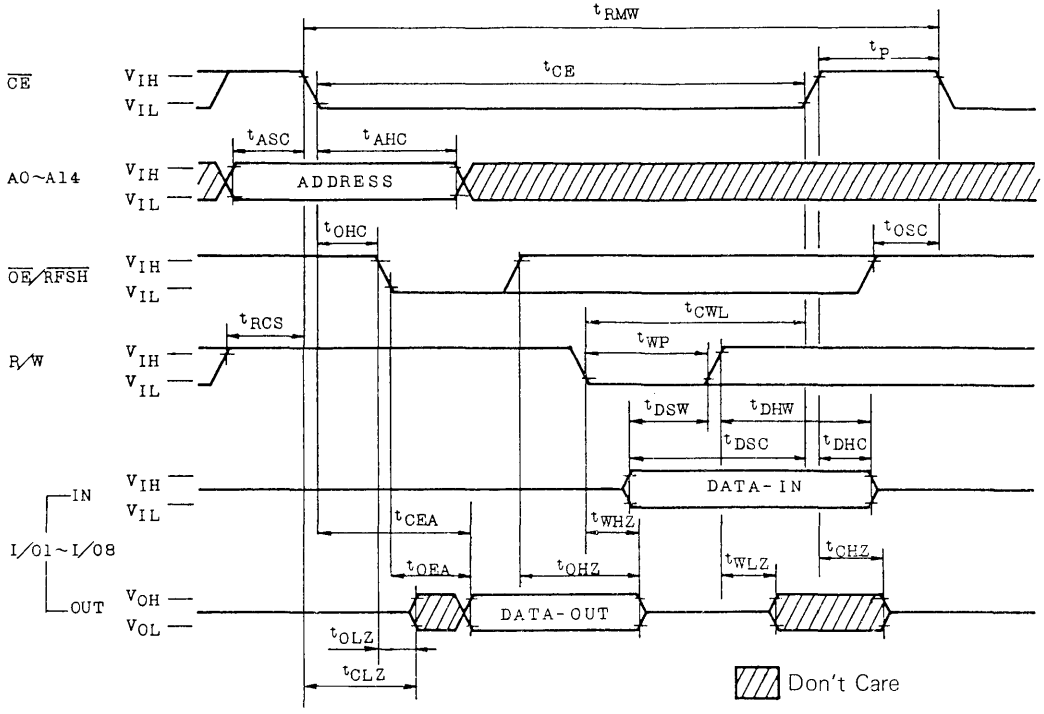
- READ CYCLE



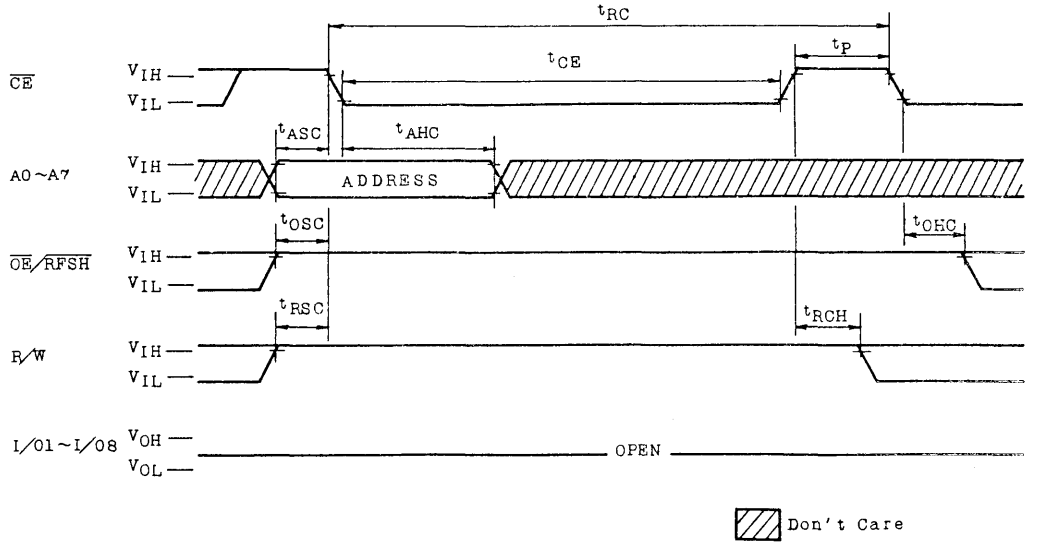
- WRITE CYCLE



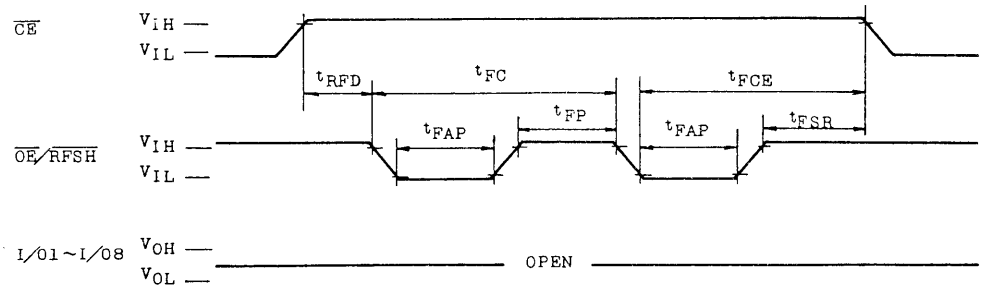
- READ WRITE CYCLE



- $\overline{CE}$ ONLY REFRESH CYCLE

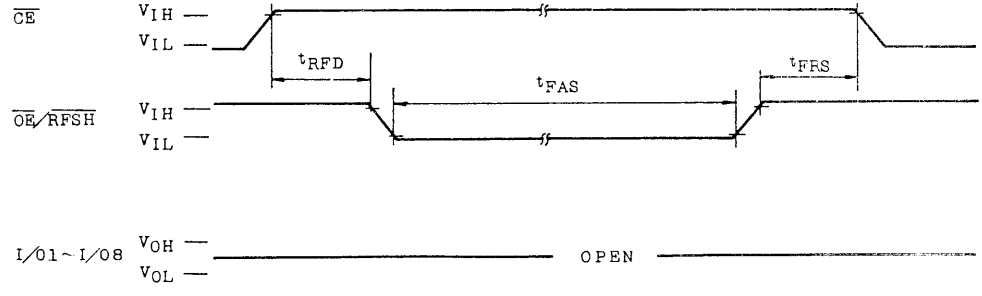


- AUTO REFRESH CYCLE



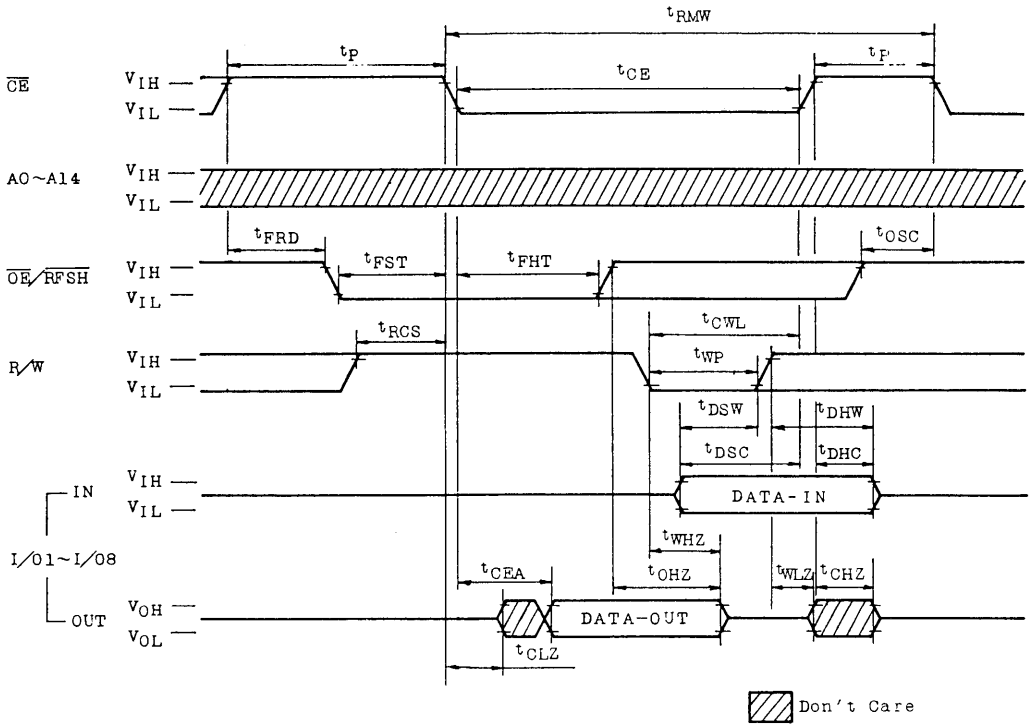
NOTE: A0 ~ A14, R/W = Don't Care

- SELF REFRESH CYCLE



NOTE: A0 ~ A14, R/W = Don't Care

- REFRESH COUNTER TEST CYCLE (READ WRITE)



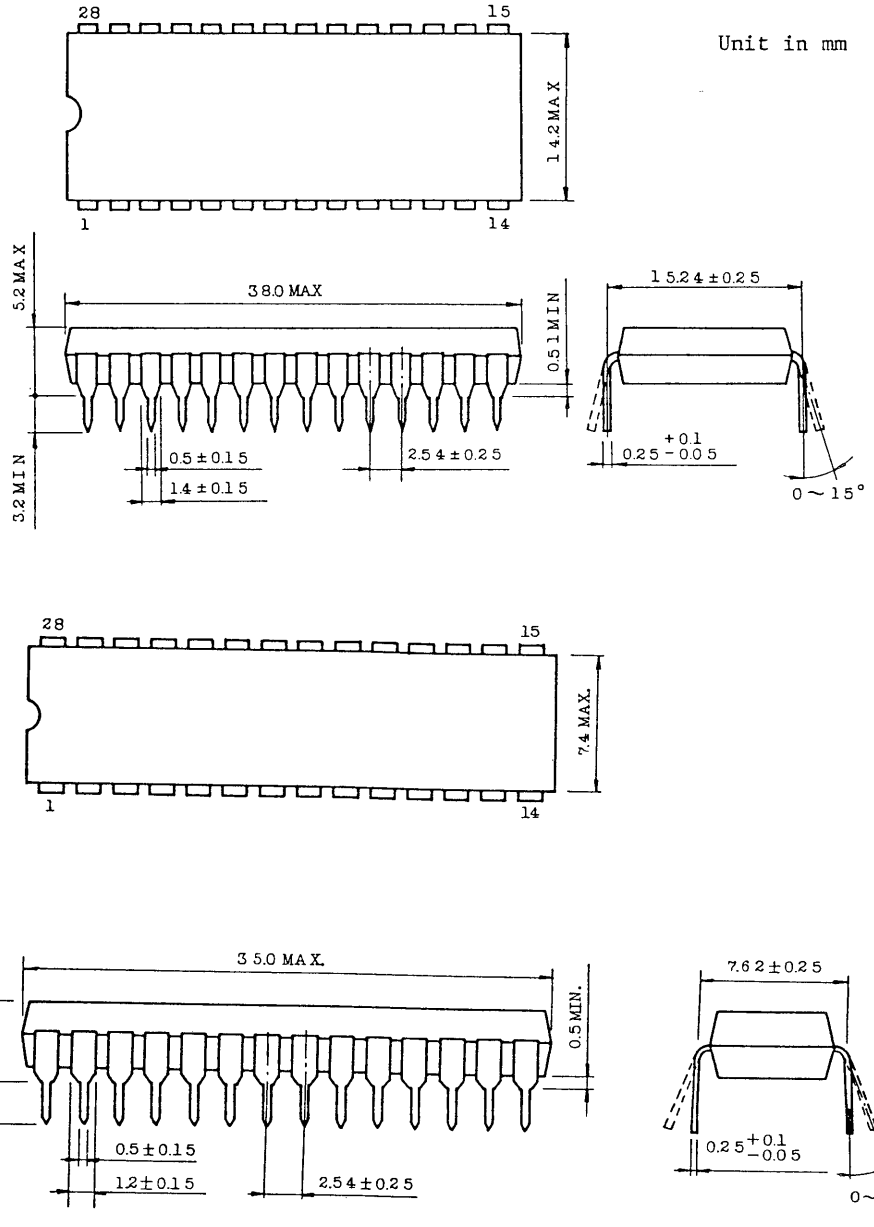
REFRESH COUNTER TEST

The internal refresh operation of TC51832P/SP/F can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.
The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (6D28A-P)

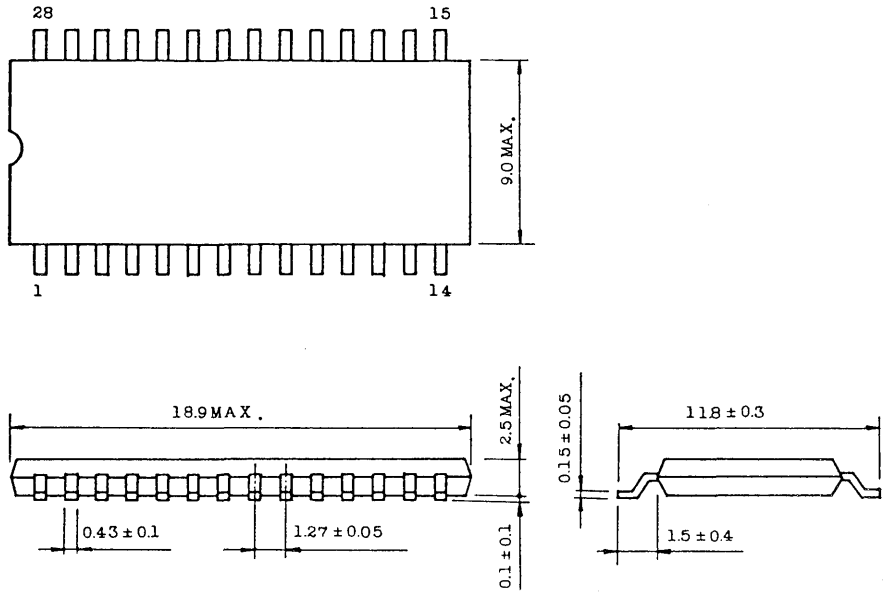
Unit in mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

- MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



NOTE: Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No. 28 leads.

32,768 WORD×8 BIT CMOS PSEUDO STATIC RAM

SILICON GATE CMOS

TC51832PL/SPL/FL-85, TC51832PL/SPL/FL-10 TC51832PL/SPL/FL-12

DESCRIPTION

The TC51832PL/SPL/FL is a 256K bit high speed CMOS pseudo static RAM organized as 32,768 words by 8 bits. The TC51832PL/SPL/FL utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. System oriented features include single power supply of 5V ± 10% tolerance. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operation — auto refresh and self refresh. The TC51832PL/SPL/FL also features static RAM like write function that the input data is written into the momory cell at the rising edge of R/W, thus being easy to interface with microprocessor. The TC51832PL/SPL/FL is a pin-compatible with 256K bit CMOS static RAM — TC55257P and is moulded a standard 0.6 inch and 0.3 inch width plastic DIP and small out-line plastic flat package.

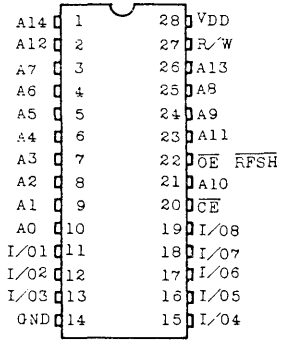
FEATURES

- Organization: 32,768 word x 8 bit
- Fast Access Time and Cycle Time

		TC51832PL/ SPL/FL-85	TC51832PL/ SPF/FL-10	TC51832PL/ SPF/FL-12
t_{CEA}	$\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA}	$\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC}	Cycle Time	135ns	160ns	190ns

- Single Power Supply: 5V ± 10%
- Static RAM like Write Function
- All inputs and outputs: TTL Compatible
- Low Power Dissipation
  - Operating: (Max.)
    - 303mW (TC51832PL/SPL/FL-85)
    - 248mW (TC51832PL/SPL/FL-10)
    - 220mW (TC51832PL/SPL/FL-12)
  - Standby: 1.1mW (Max.)
  - Self Refresh: 1.1mW (Max.)
- Two types of Refresh Operation Capability
  - Auto Refresh
  - Self Refresh
- Pin Compatible with 256K bit CMOS Static RAM TC55257P

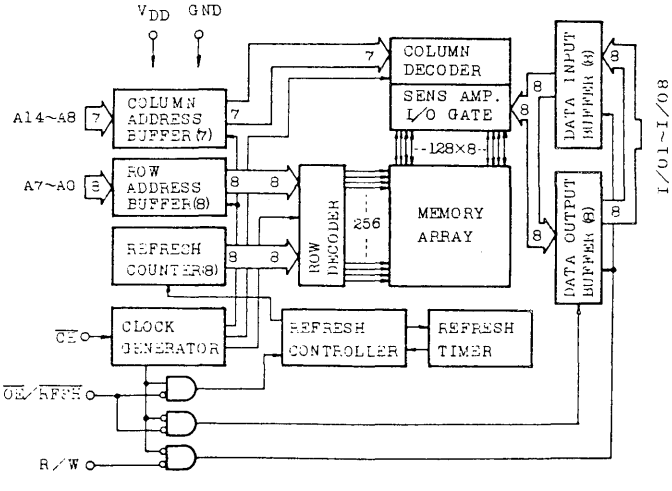
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/Refresh Input
$\overline{CE}$	Chip Enable Input
I/01 ~ I/08	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	−1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	−1.0 ~ 7.0	V	1
V_{DD}	Power Supply Voltage	−1.0 ~ 7.0	V	1
T_{OPR}	Operating Temperature	0 ~ 70	°C	1
T_{STG}	Storage Temperature	−55 ~ 150	°C	1
T_{SOLDER}	Soldering Temperature•Time	260•10	°C•sec	1
P_D	Power Dissipation	600	mW	1
I_{OUT}	Short Circuit Output Current	50	mA	1

D.C. RECOMMENDED OPERATING CONDITIONS ($Ta = 0 \sim 70°C$)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{DD0}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{CE}$, Address Cycling: $t_{RC} = t_{RC}$ MIN)	TC51832PL/SPL/FL-85	–	55	mA	3, 4
		TC51832PL/SPL/FL-10	–	45		
		TC51832PL/SPL/FL-12	–	40		
I_{DDS1}	STANDBY CURRENT 1 Power Supply Standby Current, TTL Level Input ($\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH})		–	1	mA	
I_{DDS2}	STANDBY CURRENT 2 Power Supply Standby Current, CMOS Level Input ($\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{DD}-0.2V)		–	0.2	mA	
I_{DDF}	SELF REFRESH CURRENT Average Power Supply Self Refresh Current ($\overline{CE}$ = V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$ = 0.2V)		–	0.2	mA	
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ V_{DD}, All Other Inputs not under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disable, 0V ≤ V_{OUT} ≤ V_{DD})		−10	10	μA	
V_{OH}	OUTPUT HIGH LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	–	V	
V_{OL}	OUTPUT LOW LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0 ~ 70°C) (Notes 5, 6, 7, 8, 9)

SYMBOL	PARAMETER	TC51832SPL/SPL/FL-85		TC51832PL/SPL/FL-10		TC51832PL/SPL/FL-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	160	–	190	–	ns	
t_{RMW}	Read Write Cycle Time	200	–	240	–	280	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	85	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	–	10	–	10	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	R/W to Output in Low-Z	0	–	0	–	0	–	ns	
t_{CHZ}	$\overline{CE}$ to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHZ}	$\overline{OE}$ to Output in High-Z	0	25	0	30	0	35	ns	10
t_{WHZ}	R/W to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	–	70	–	85	–	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	–	70	–	85	–	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	–	40	–	50	–	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	–	40	–	50	–	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	–	0	–	0	–	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	–	0	–	0	–	ns	11
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	12
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	12
t_{FC}	Auto Refresh Cycle Time	135	–	160	–	190	–	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh Cycle)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	13
t_{FCE}	$\overline{RFSH}$ Active to $\overline{CE}$ Delay Time	160	–	190	–	225	–	ns	13
t_{FSR}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Auto Refresh Cycle)	65	–	80	–	95	–	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh Cycle)	8,000	–	8,000	–	8,000	–	ns	13
t_{FRS}	$\overline{RFSH}$ Precharge to $\overline{CE}$ Delay Time (Self Refresh Cycle)	160	–	190	–	225	–	ns	13
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test Cycle)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test Cycle)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	–	4	–	4	–	4	ms	
t_{T}	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0 ~ A14)	–	5	pF
CI2	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	–	7	pF
CI0	Input/Output Capacitance (I/O1 ~ I/O8)	–	7	pF

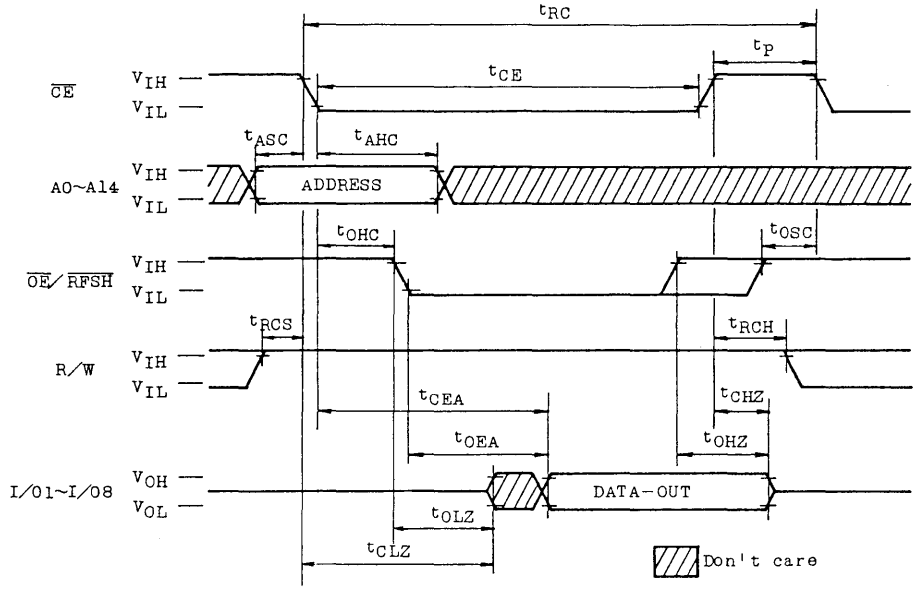
NOTE: This parameter is periodically sampled and is not 100% tested.

NOTES:

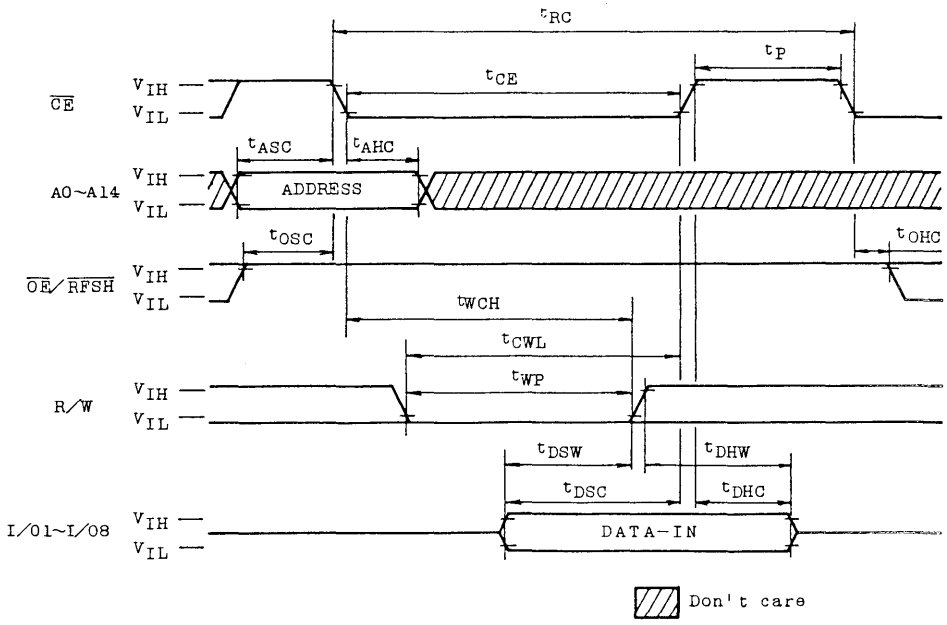
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are reference to GND.
3. I_{DDO} depend on cycle rate.
4. I_{DDO} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}$/$\overline{RFSH}$ is required after power-up before proper device operation is achieved.
6. AC measurements assume t_T = 5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. The $\overline{OE}$/$\overline{RFSH}$ input operates as the output enable input ($\overline{OE}$) and refresh control input ($\overline{RFSH}$) under the condition of that $\overline{CE}$ = V_{IL} and $\overline{CE}$ = V_{IH} , respectively.
10. t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.
11. In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).
12. All address are latched at the falling edge of $\overline{CE}$, and must be valid during t_{ASC} and t_{AHC}.
13. Two refresh operation – auto refresh and self refresh are determined by the $\overline{OE}$/$\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH} .
    Auto refresh: $\overline{OE}$/$\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh: $\overline{OE}$/$\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The following timing parameter must be kept before device proper operation is achieved after refresh.
    Auto refresh: t_{FCE} and t_{FSR}
    Self refresh: t_{FRS}

TIMING WAVEFORMS

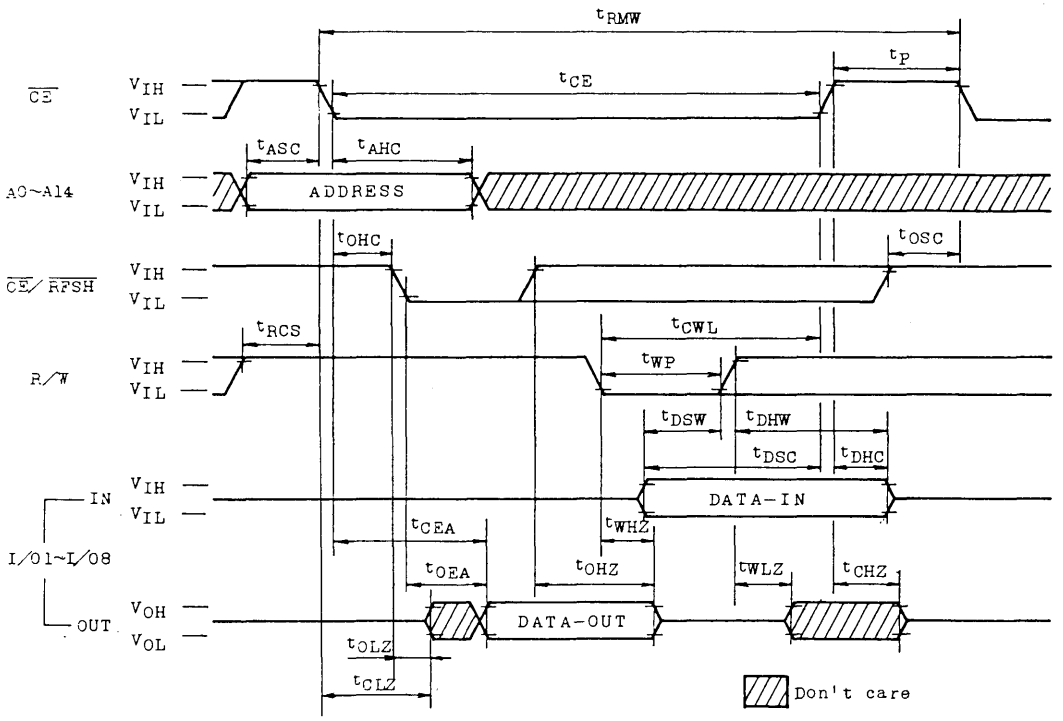
- READ CYCLE



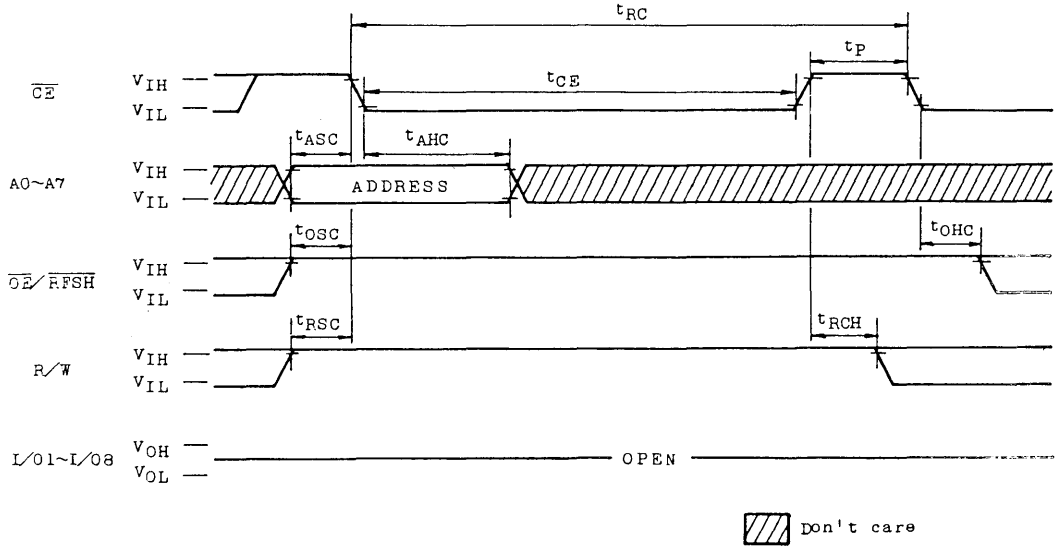
- WRITE CYCLE



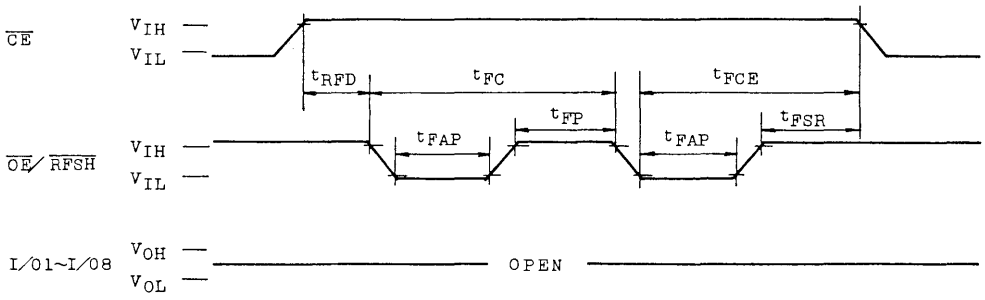
- READ WRITE CYCLE



- CE ONLY REFRESH CYCLE

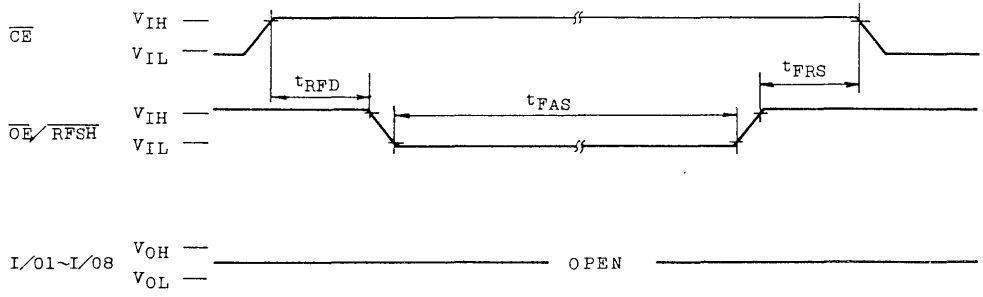


- AUTO REFRESH CYCLE



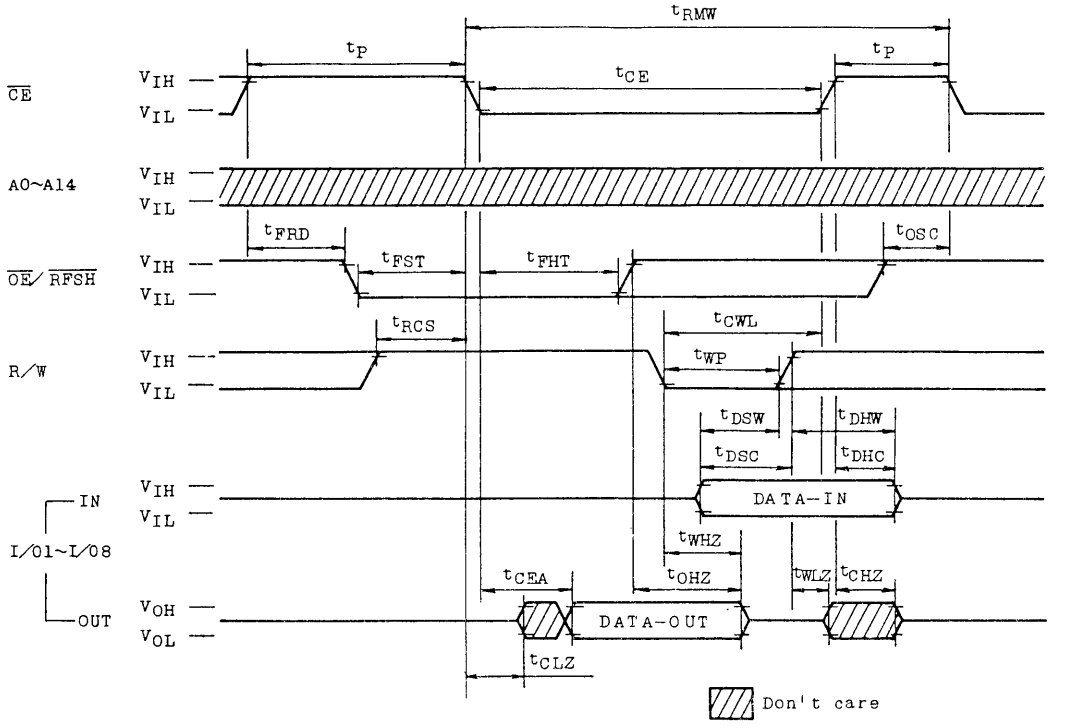
NOTE: A0 ~ A14, R/W = Don't care

- SELF REFRESH CYCLE



NOTE: A0 ~ A14, R/W = Don't care

- REFRESH COUNTER TEST CYCLE (READ WRITE)



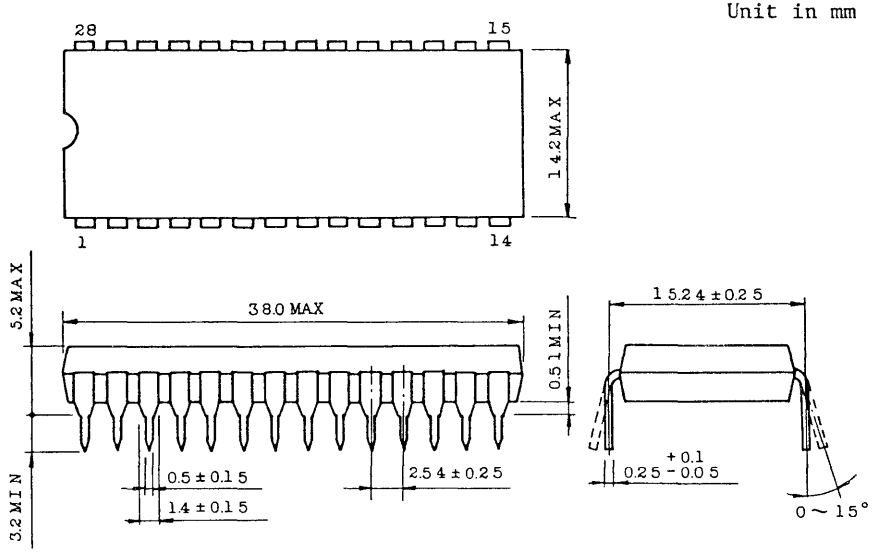
REFRESH COUNTER TEST

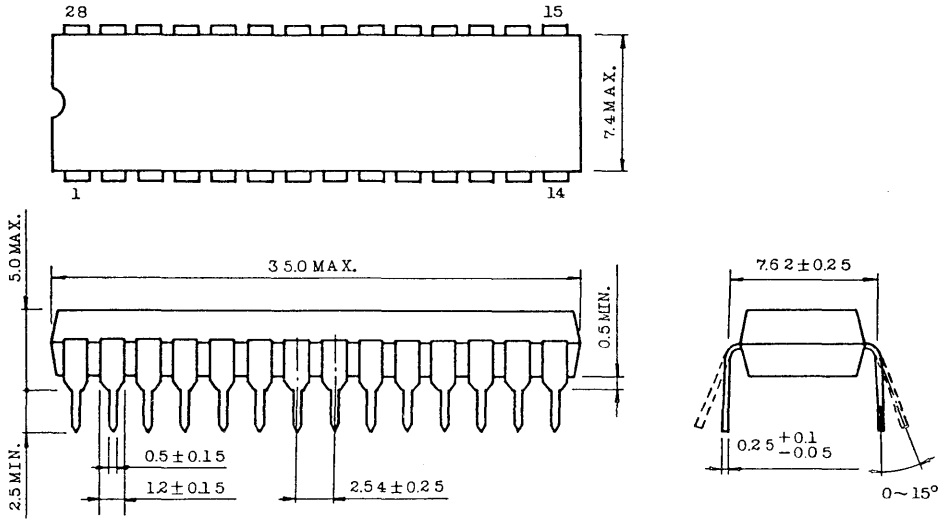
The internal refresh operation of TC51832PL/SPL/FL can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.
The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.
② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
③ Check "1" out of 256 bits at normal read mode, which was written at ②.
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.
⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.
⑥ Perform the above ① to ⑤ the complement data.

- OUTLINE DRAWINGS (6D28A-P)

Unit in mm

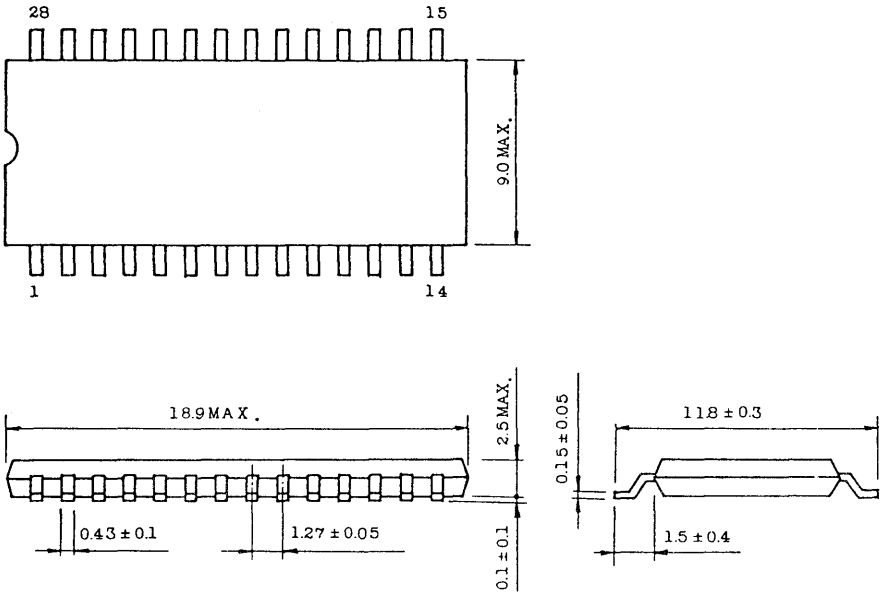




NOTES: Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No. 28 leads.
All dimensions are in millimeters.

- MFP 28 PIN OUTLINE DRAWINGS (F28GA-P)

Unit in mm



NOTE: Lead pitch is 1.27 and tolerance is ± 0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TC518128P-10, P-12, PL-10, PL-12
TC518128F-10, F-12, FL-10, FL-12

DESCRIPTION

The TC518128P/F is a 1Mbit high speed CMOS Virtually and Pseudo Static RAM organized as 131,072 words by 8 bits. The TC518128P/F utilizing one transistor dynamic memory cell with CMOS peripheral circuit provides large capacity, high speed and low power features. The feature includes single power supply of 5V±10%.

The TC518128P/F has Virtually Static RAM mode (VS mode) and Pseudo Static RAM mode (PS mode). PS mode has control of refresh operation determined by $\overline{RFSH}$ input. This refresh operation is easy to operate because of having two types of refresh operation -- Auto Refresh and Self Refresh. As VS mode controls all refresh operation on chip by fixing "L" on $\overline{RFSH}$ pin, it is usable static RAM.

The TC518128P/F is a pin-compatible with 1M bit CMOS Static RAM-JEDEC standard and is moulded in a 32pin standard 0.6 inches width plastic DIP and small-out line plastic flat package.

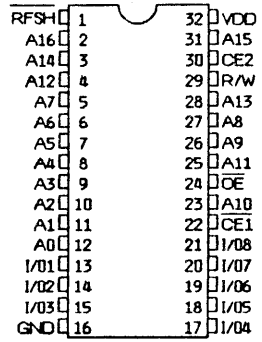
FEATURES

- Organization: 1Mbit (131,072wordx8bit)
- Fast Access Time and Cycle Time

	PS mode		VS mode	
	-10	-12	-10	-12
tCEA $\overline{CE}$ Access Time	100	120	160	190
tOEA $\overline{OE}$ Access Time	40	40	40	40
tRC Cycle Time	160	190	220	260

- Single Power Supply: 5V±10%
- Data Retention Voltage: 3~5.5V (L-Version)
- All inputs and outputs: TTL Compatible
- 1,024 Refresh Cycle/16ms
- Low Power Dissipation
- Operating: 330mW(MAX): P/PL/F/FL-10
  : 275mW(MAX): P/PL/F/FL-12
- Self Refresh: 0.28mW(MAX) VDD=5.5V
  (L-Version): 0.09mW(MAX) VDD=3V
- VS mode: No Refresh control required.
- PS mode: Two types of Refresh operation capability.
  Auto Refresh: by internal counter
  Self Refresh: by internal timer
- 32pin standard plastic package (DIP)
- 32pin mini flat plastic package (SOP)

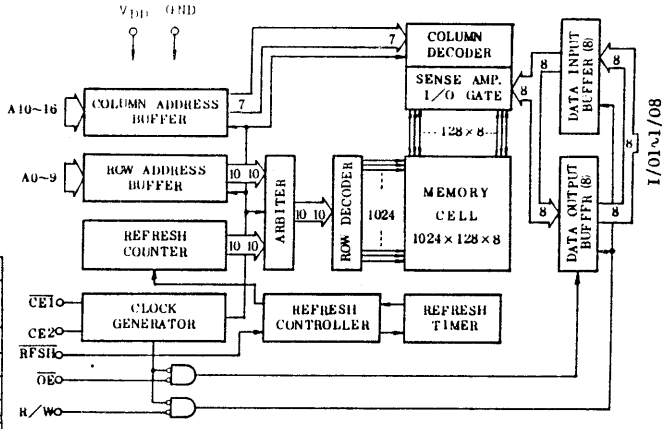
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1~I/O8	Data Inputs/Outputs
VDD	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0~A16	I/O1~8	CONDITION
L	H	L	H	H/L	V*	OUT	Read
L	H	*	L	H/L	V*	IN	Write
L	H	H	H	H/L	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H -- High Level Input (VIN=VDD+0.5V~VIH min)
L -- Low Level Input (VIN=VIL max~-0.5V)
* -- Don't care (VDD+0.5V~-0.5V)
V* - At $\overline{CE1}$ falling edge (CE2=H) or CE2 rising edge ($\overline{CE1}$=L), all address inputs are "IN", and at the other condition, the address input are "*".
HZ - High Impedance
H/L - H:PS mode
L:VS mode

VS mode and PS mode

No refresh control is achieved by VS mode and high speed accessing is achieved by PS mode.

VS mode and PS mode are chosen by controlling refresh terminal. VS mode is chosen by fixing "L" on $\overline{RFSH}$ pin, and PS mode is chosen by clock operation.

MAXIMUM RATIMG

SYMBOL	ITEM	RATING	UNITS	NOTE
VIN	Input Voltage	-1.0~7.0	V	
VOUT	Output Voltage	-1.0~VDD+0.5	V	
VDD	Power Supply Voltage	-1.0~7.0	V	
TOPR	Operating Temperature	0~70	°C	1
TSTG	Storage Temperature	-55~150	°C	
TSOLDER	Soldering Temperature·Time	260·10	°C·sec	
PD	Power Dissipation	600	mW	
IOUT	Short Circuit Output Current	50	mA	

D.C.RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
VDD	Power Supply Volage	4.5	5.0	5.5	V	
VIH	Input High Voltage	2.2	-	VDD+0.5V	V	
VIL	Input Low Voltage	-0.5	-	0.8	V	2
VDH	Data Retention Voltage (L-Version only)	3.0	5.0	5.5	V	

D.C.ELECTRICAL CHARACTERISTICS (VDD=5V±10%, Ta=0~70°C)

SYMBOL	PARAMETER			PERIOD	MIN.	MAX.	UNITS	NOTES
IDDO	Operating Current (Average Power Supply Operating Current) VDD=5.5V (Involved CE only Refresh and Auto Refresh)			160ns	-	60	mA	3,4
				190ns	-	50		
				1μs	-	10		
IDDSB1	Standby Current $\overline{CE1}$=VIH or CE2=VIL, $\overline{RFSH}$=VIH	TC518128P/F			-	2	mA	
		TC518128PL/FL			-	1		
*IDDSB2	Standby Current $\overline{CE1}$=VDD-0.2V or CE2=0.2V $\overline{RFSH}$=VDD-0.2V	TC518128P/F	V_{DD}	5.5V	-	1	mA	
		TC518128PL/FL	V_{DH}	5.5V	-	50	μA	
				3.0V	-	30		
IDDF1	Self Refresh Current $\overline{CE1}$=VIH or CE2=VIL, $\overline{RFSH}$=VIL Fix	TC518128P/F			-	2	mA	
		TC518128PL/FL			-	1		
*IDDF2	Self Refresh Current $\overline{CE1}$=VDD-0.2V or CE2=0.2V $\overline{RFSH}$=0.2V Fix	TC518128P/F	V_{DD}	5.5V	-	1	mA	
		TC518128PL/FL	V_{DH}	5.5V	-	50	μA	
				3.0V	-	30		
II(L)	Input Leakage Current 0V≤VIN≤VDD				-1	1	μA	
IO(L)	Output Leakage Current Output Disable ($\overline{CE1}$=VIH or CE2=VIL or $\overline{OE}$=VIH or R/W=VIL), 0V≤VOUT≤VDD				-1	1	μA	
VOH	Output High Level IOH=-5mA				2.4	-	V	
VOL	Output Low Level IOL=4.2mA				-	0.4	V	

NOTE*) In standby mode and self refresh with $\overline{CE1}$≥VDD-0.2V, these specification limits are guaranteed under the condition of CE2≥VDD-0.2V, or CE2≤0.2V.

CAPACITANCE (f=1MHZ, Ta=25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A16)	-	5	pF
CI2	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
CIO	Input/Output Capacitance	-	7	pF

NOTE) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMENDED AC OPERATION CONDITIONS

PS mode (VDD=5V±10%, Ta=0~70 °C) (NOTES:5,6,7,8)

SYMBOL	PARAMETER	-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
tRC	Random Read,Write Cycle Time	160	-	190	-	ns	
tRMW	Read Modify Write Cycle Time	250	-	295	-	ns	
tCE	CE Pulse Width	100	tREF	120	tREF	ns	
tP	CE Precharge Time	50	-	60	-	ns	
tCEA	CE Access Time	-	100	-	120	ns	
tOEA	$\overline{OE}$ Access Time	-	40	-	40	ns	
tCLZ	Chip Enable to Output in Low-Z	10	-	10	-	ns	
tOLZ	Output Enable to Output in Low-Z	0	-	0	-	ns	
tWLZ	Output Active from End of Write	0	-	0	-	ns	
tCHZ	Chip Disable to Output in High-Z	0	30	0	35	ns	9
tOHZ	$\overline{OE}$ Disable to Output in High-Z	0	30	0	35	ns	9
tWHZ	Write Enable to Output in High-Z	0	30	0	35	ns	9
tODS	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	ns	
tODH	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	ns	
tRCS	Read Command Set-Up Time	0	-	0	-	ns	
tRCH	Read Command Hold Time	0	-	0	-	ns	
tWP	Write Pulse Width	70	-	85	-	ns	
tWCH	Write Comand Hold Time	70	10000	85	10000	ns	
tCWL	Write Command to CE Lead Time	70	-	85	-	ns	
tDSW	Data Set-Up Time from R/W	60	-	75	-	ns	10
tDSC	Data Set-Up Time from CE	60	-	75	-	ns	10
tDHW	Data Hold Time from R/W	0	-	0	-	ns	10
tDHC	Data Hold Time from CE	0	-	0	-	ns	10
tASC	Address Set-Up Time	0	-	0	-	ns	11
tAHC	Address Hold Time	25	-	30	-	ns	11
tFC	Auto Refresh Cycle Time	160	-	190	-	ns	
tRFD	$\overline{RFSH}$ Delay Time from CE	50	-	60	-	ns	
tFAP	$\overline{RFSH}$ Pulse Width(Auto Refresh)	80	8,000	80	8000	ns	12
tFP	$\overline{RFSH}$ Precharge Time	30	-	30	-	ns	12
tFCE	$\overline{RFSH}$ to CE Active Delay Time	190	-	225	-	ns	12
tFSR	CE Delay Time from $\overline{RFSH}$ (Auto Refresh)	80	-	95	-	ns	12
tFAS	$\overline{RFSH}$ Pulse Width(Self Refresh)	8000	-	8,000	-	ns	12
tFRS	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	190	-	225	-	ns	12
tREF	Refresh Period (1,024 cycle, A0~A9)	-	16	-	16	ms	
tT	Transition Time(Rise and Fall)	3	50	3	50	ns	

ELECTRICAL CHARACTERISTICS AND RECOMENDED AC OPERATION CONDITIONS

VS mode (VDD=5V±10%, Ta=0~70°C) (NOTES:5,6,7,8)

SYMBOL	PARAMETER	-10		-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
tVRC	Random Read,Write Cycle Time	220	-	260	-	ns	
tVRMW	Read Modify Write Cycle Time	310	-	365	-	ns	
tVCE	CE Pulse Width	160	∞	190	∞	ns	
tP	CE Precharge Time	50	-	60	-	ns	
tVCA	$\overline{CE}$ Access Time	-	160	-	190	ns	
tOEA	$\overline{OE}$ Access Time	-	40	-	40	ns	
tCLZ	Chip Enable to Output in Low-Z	10	-	10	-	ns	
tOLZ	Output Enable to Output in Low-Z	0	-	0	-	ns	
tWLZ	Output Active from End of Write	0	-	0	-	ns	
tCHZ	Chip Disable to Output in High-Z	0	30	0	35	ns	9
tOHZ	$\overline{OE}$ Disable to Output in High-Z	0	30	0	35	ns	9
tWHZ	Write Enable to Output in High-Z	0	30	0	35	ns	9
tODS	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	ns	
tODH	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	ns	
tRCS	Read Command Set-Up Time	0	-	0	-	ns	
tRCH	Read Command Hold Time	0	-	0	-	ns	
tWP	Write Pulse Width	130	-	155	-	ns	
tVWH	Write Comand Hold Time	130	10000	155	10000	ns	
tVWL	Write Command to CE Lead Time	130	-	155	-	ns	
tDSW	Data Set-Up Time from R/W	60	-	75	-	ns	10
tDSC	Data Set-Up Time from CE	60	-	75	-	ns	10
tDHW	Data Hold Time from R/W	0	-	0	-	ns	10
tDHC	Data Hold Time from CE	0	-	0	-	ns	10
tASC	Address Set-Up Time	0	-	0	-	ns	11
tAHC	Address Hold Time	25	-	30	-	ns	11
tVRS	VS mode Set-Up Time	0	-	0	-	ns	
tVRH	VS mode Hold Time	0	-	0	-	ns	
tT	Transition Time(Rise and Fall)	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are reference to GND.

3) IDD0 depend on cycle rate.

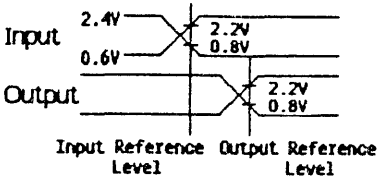
4) IDD0 depend on output loading. Specified value are obtained with the output open.

5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.

6) AC measurements assume tT=5ns.

7) Timing Reference Level

Input Level	:	VIH=2.4V
		VIL=0.6V
Reference Level	:	VIH=2.2V
		VIL=0.8V
	:	VOH=2.2V
		VOL=0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) tCHZ, tOHZ, tWHZ define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 faling edge. Therefore the inut data must be valid during set-up time (tDSW,tDSC) and hold time (tDHW,tDHC).

11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during tASC and tAHC.

12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1}$=VIH or CE2=VIL.

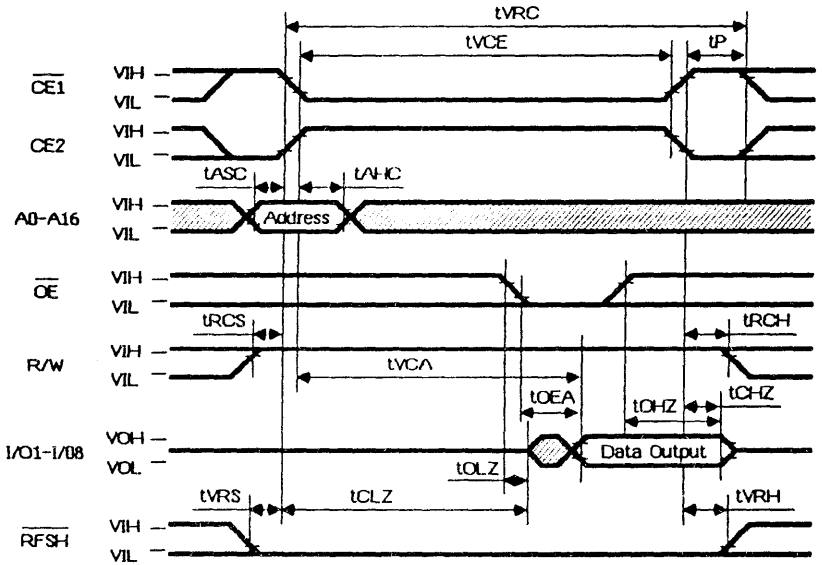
Auto refresh:$\overline{RFSH}$ pulse width$\leq$tFAP (max.)
Self refresh:$\overline{RFSH}$ pulse width$\geq$tFAS (min.)

In case of using PS mode, the following timing parameter must be kept for device proper operation after refresh.

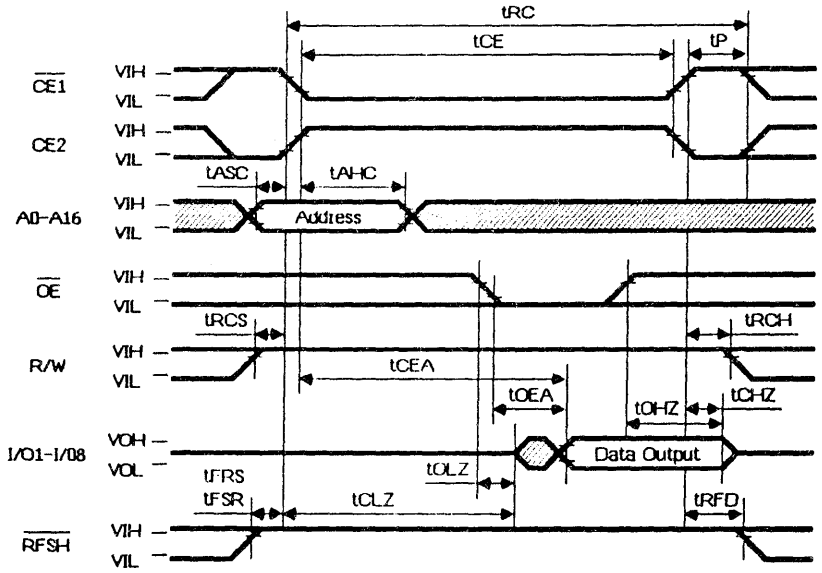
Auto refresh:tFCE and tFSR
Self refresh:tFRS

TIMING WAVEFORMS

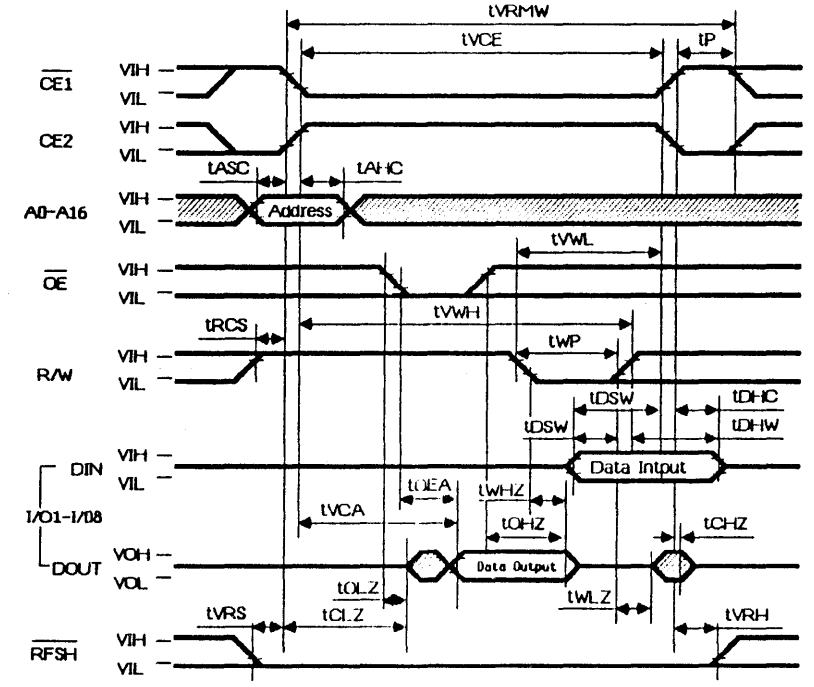
VS MODE READ CYCLE



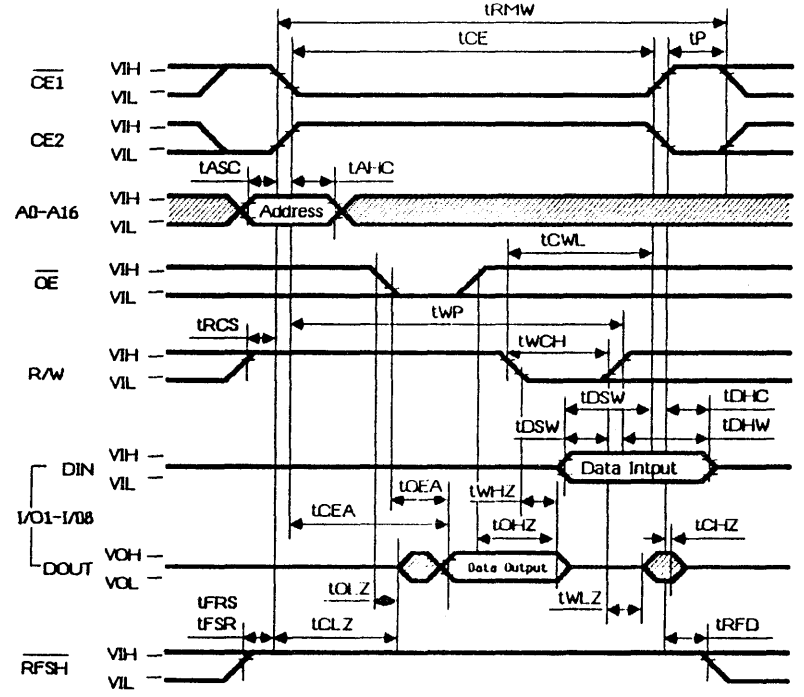
PS MODE READ CYCLE



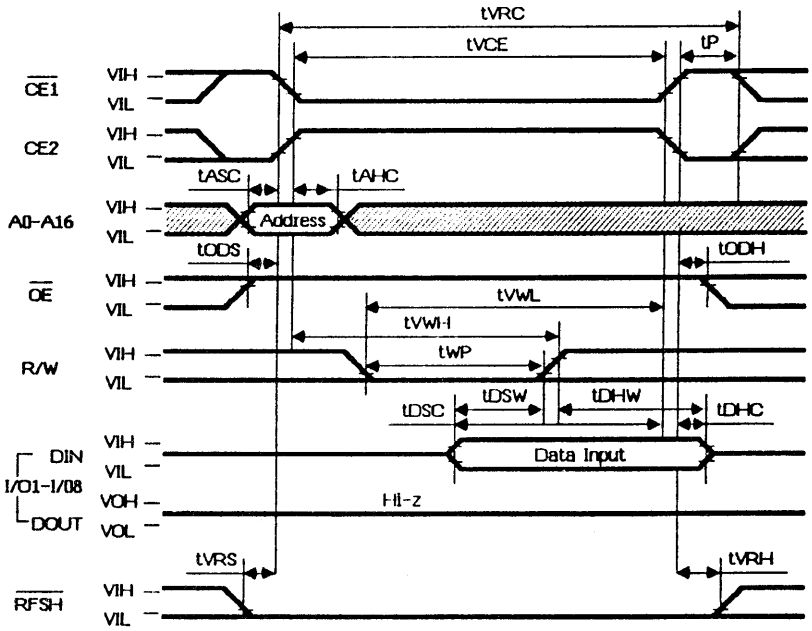
VS MODE READ MODIFY WRITE CYCLE



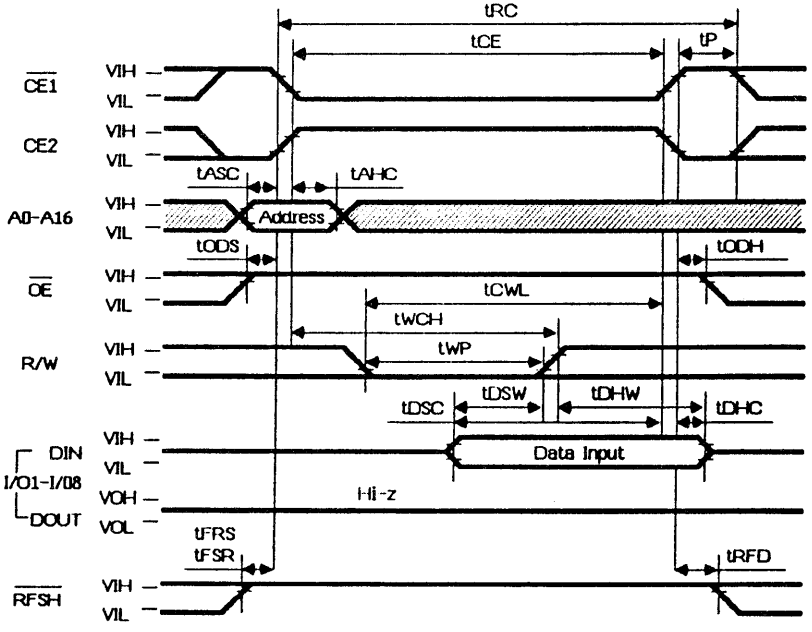
PS MODE READ MODIFY WRITE CYCLE



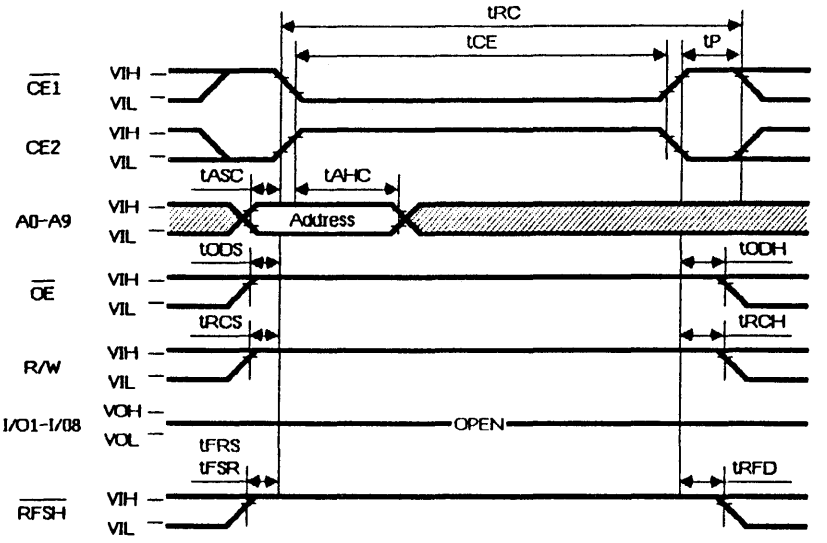
VS MODE WRITE CYCLE



PS MODE WRITE CYCLE

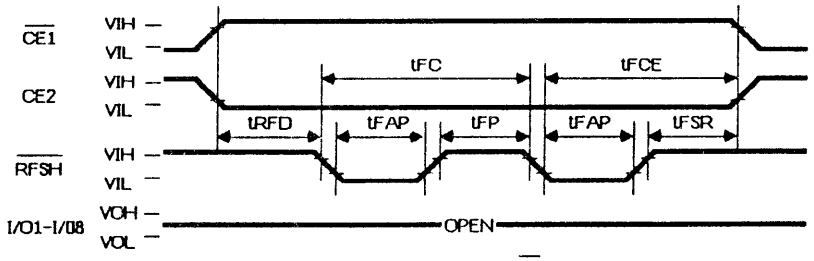


CE ONLY REFRESH



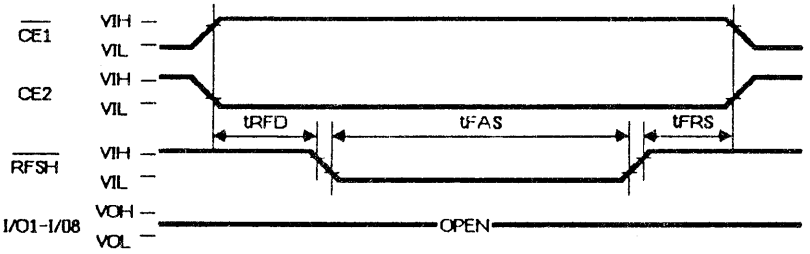
NOTE : $\overline{OE}$, R/W, A10-A16 ••• Don't Care

AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0-A16 ••• Don't Care

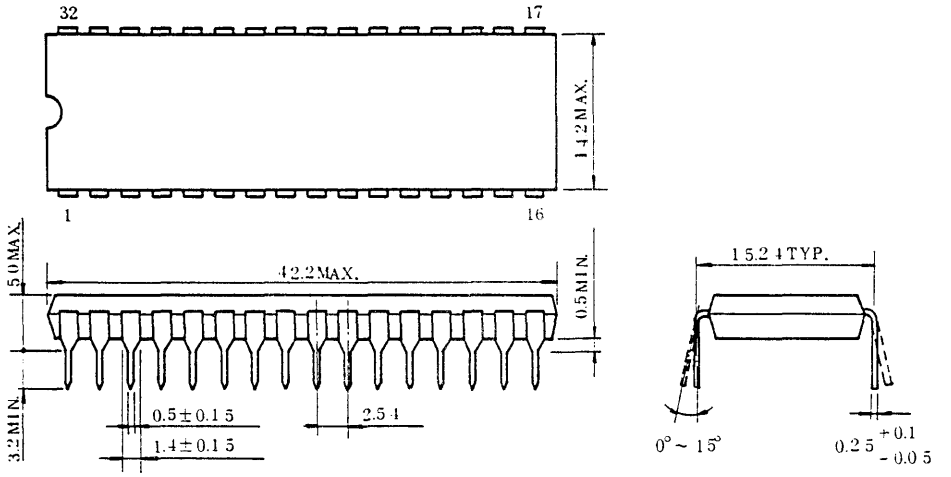
SELF REFRESH



NOTE : $\overline{OE}$, R/W, A0-A16 ••• Don't Care

OUTLIME DRAWINGS DIP 32PIN

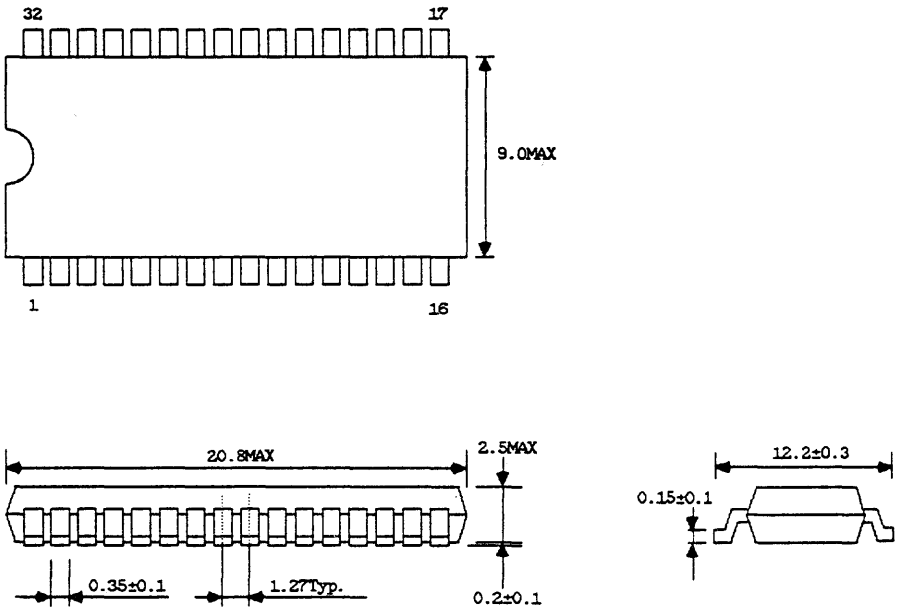
Unit: mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.32 leads.

SOP 32PIN

Unit: mm



Note: Lead pitch is 1.27mm and tolerance is ±0.12mm against theoretical center of each lead that is obatined on the basis of No.1 and No.32 leads.

High Speed Static RAM

2,048 WORD × 8 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2018AP-25, TMM2018AP-35
TMM2018AP-45

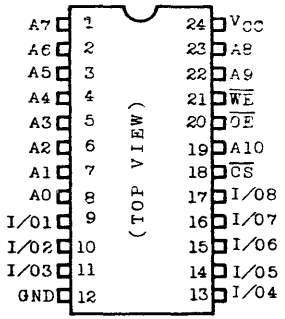
DESCRIPTION

The TMM2018AP is a 16,384 bits high speed and low power static random access memory organized as 2,048 words by 8 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 150mA/135mA/135mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2018AP is most suitable for use in cache memory and high speed storage.
The TMM2018AP is offered in a 24 pin standard plastic package with 0.3 inch width for high density assembly.
The TMM2018AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  - t_{ACC}=25ns: TMM2018AP-25
  - t_{ACC}=35ns: TMM2018AP-35
  - t_{ACC}=45ns: TMM2018AP-45
- Low power dissipation
  - I_{CC}=150mA: TMM2018AP-25
  - I_{CC}=135mA: TMM2018AP-35
  - I_{CC}=135mA: TMM2018AP-45
  - I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature: $\overline{CS}$=V_{IH}
- Output buffer control: $\overline{OE}$
- Three state outputs
- Inputs protected: All inputs protection against static charge.
- Package: 24 pin standard plastic package, 0.3 inch width.

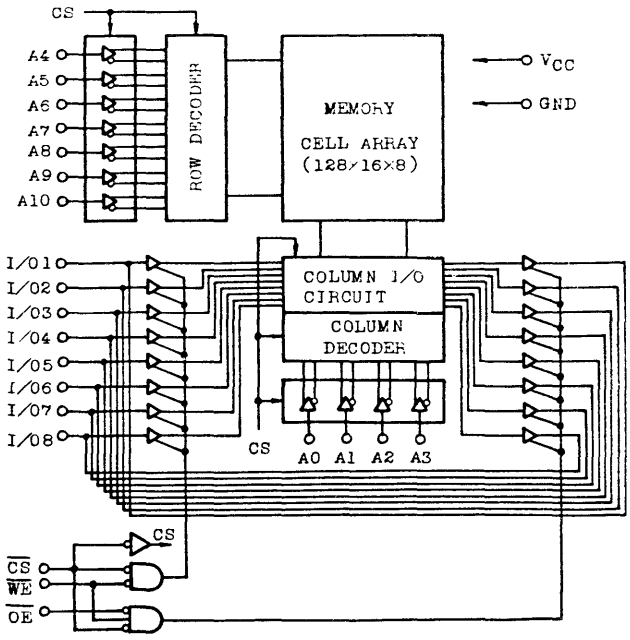
PIN CONNECTION



PIN NAMES

A0 ∿ A10	Address Inputs
I/01 ∿ I/08	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}	Input Voltage	-3.5 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5 ∿ 7.0	V
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
P_D	Power Dissipation	0.9	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	

* Pulse Width: 10ns, DC: -0.5V (MIN.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0 ∿ V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0 ∿ V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	150	mA
			-35	-	135	
			-45	-	135	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0 ∿ 5.5V		-	40	

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{OE}	Output Enable to Output Valid	-	15	-	20	-	20	
t_{CLZ}	Chip Selection to Output in Low-Z	0	-	0	-	0	-	
t_{CHZ}	Chip Deselection to Output in High-Z	-	15	-	20	-	20	
t_{OLZ}	Output Enable to Output in Low-Z	0	-	0	-	0	-	
t_{OHZ}	Output Disable to Output in High-Z	-	12	-	15	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2018AP-25		TMM2018AP-35		TMM2018AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	12	-	15	-	15	
t_{DS}	Data Set Up Time	12	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

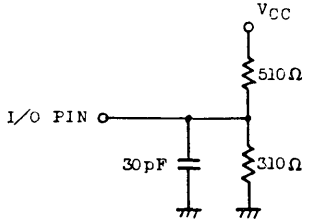
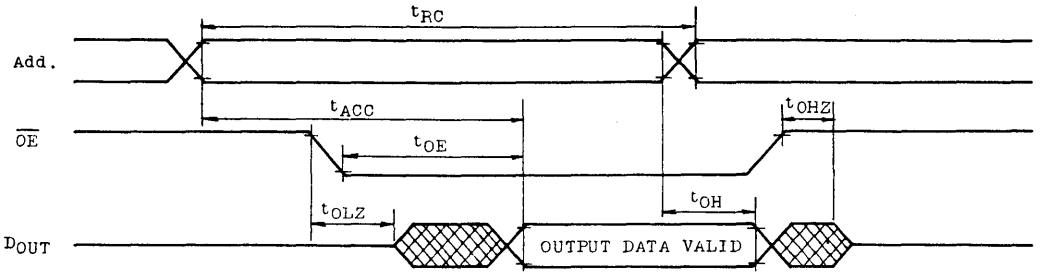


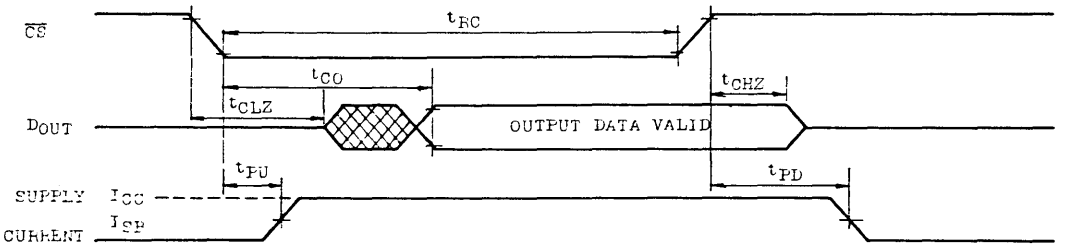
Fig.1 OUTPUT LOAD

TIMING WAVEFORMS

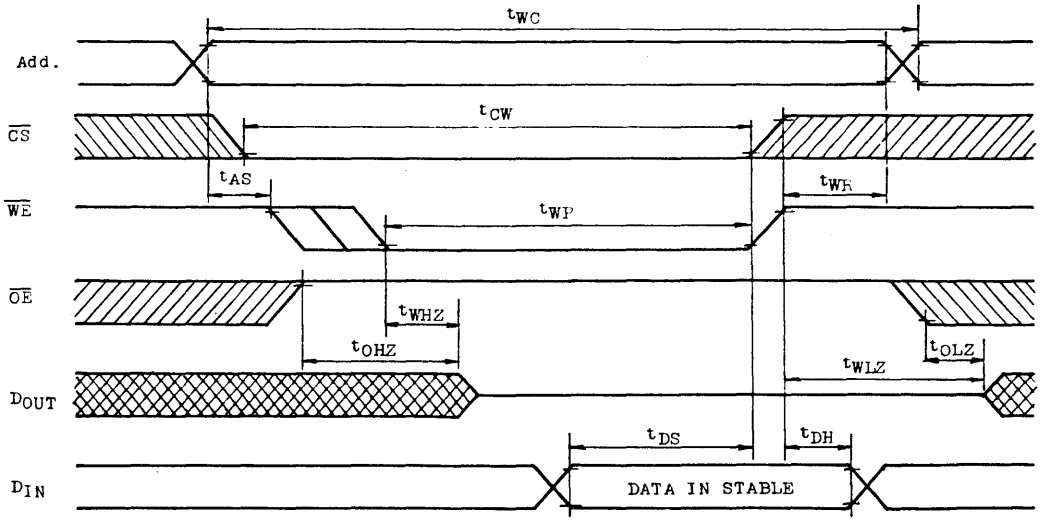
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



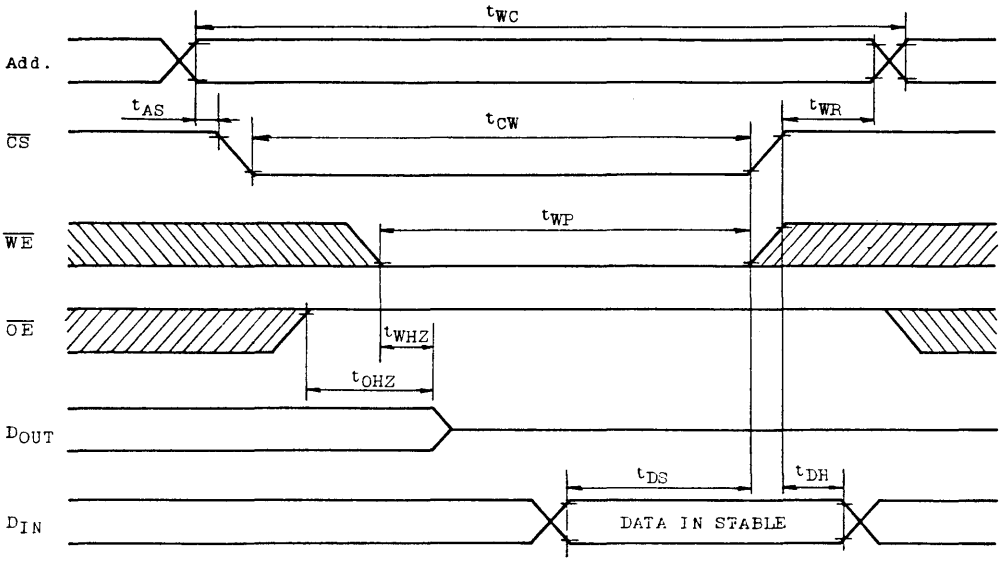
READ CYCLE 2. ($\overline{WE}$=V_{IH}, $\overline{OE}$=V_{IL})



WRITE CYCLE 1.



WRITE CYCLE 2.

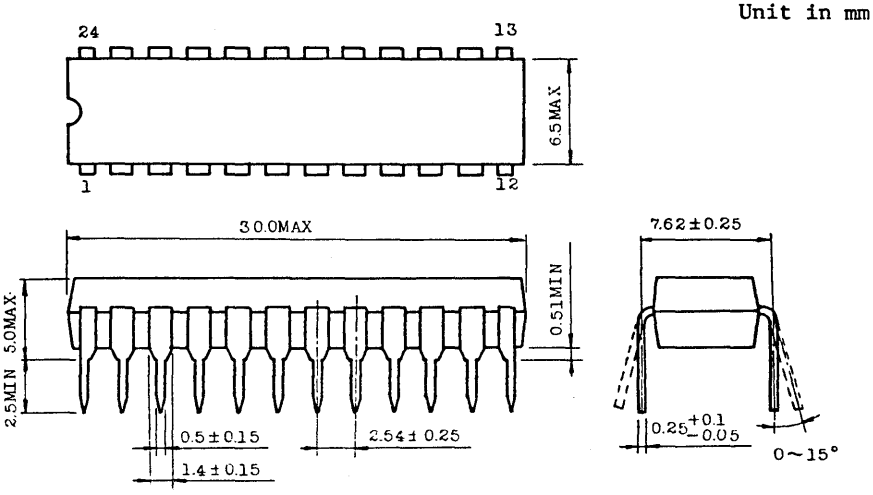


Note: 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCTS

4,096 WORD × 4 BIT STATIC RAM
SILICON MONOLITHIC
N-CHANNEL SILICON GATE MOS PROCESS

TMM2068AP-25, TMM2068AP-35
TMM2068AP-45

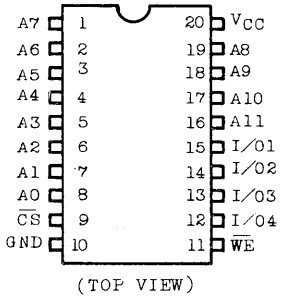
DESCRIPTION

The TMM2068AP is a 16,384 bits high speed and low power static random access memory organized as 4,096 words by 4 bits and operates from a single 5V supply.
Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 135/120/120mA. When $\overline{CS}$ goes high, the device is deselected and placed in a low power standby mode in which maximum standby current is 20mA.
Thus the TMM2068AP is most suitable for us in cache memory and high speed storage.
The TMM2068AP is offered in a 20 pin standard plastic package with 0.3 inch width for high density assembly.
The TMM2068AP is fabricated with ion implanted N channel silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time
  t_{ACC}=25ns: TMM2068AP-25
  t_{ACC}=35ns: TMM2068AP-35
  t_{ACC}=45ns: TMM2068AP-45
- Low power dissipation
  I_{CC}=135mA: TMM2068AP-25
  I_{CC}=120mA: TMM2068AP-35
  I_{CC}=120mA: TMM2068AP-45
  I_{SB}=20mA
- Single 5V power supply
- Fully static operation
- All inputs and outputs: Directly TTL compatible
- Power down feature : $\overline{CS}$=V_{IH}
- Three state outputs
- Inputs protected: All inputs protection aganist static charge.
- Package: 20 pins standard plastic package, 0.3 inch width.

PIN CONNECTION

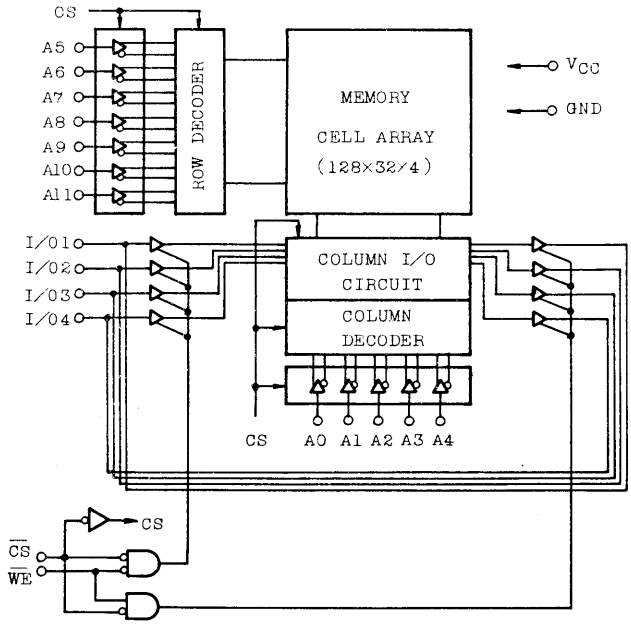


(TOP VIEW)

PIN NAMES

A0 ∿ A11	Address Inputs
I/O1 ∿ I/O4	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}	Input Voltage	-3.5 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-3.5 ∿ 7.0	V
T_{opr}	Operating Temperature	0 ∿ 70	°C
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
P_D	Power Dissipation	1.0	W
I_{OUT}	D.C. Output Current	20	mA

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	MAX.	UNIT
I_{IL}	Input Current	V_{IN}=0 ∿ V_{CC}		-	±1.0	μA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA		2.4	-	V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA		-	0.4	V
I_{LO}	Output Leakage Current	V_{OUT}=0 ∿ V_{CC}, $\overline{CS}$=V_{IH}		-	±1.0	μA
I_{CC}	Operating Current	$\overline{CS}$=V_{IL}	-25	-	135	mA
			-35	-	120	
			-45	-	120	
I_{SB}	Standby Current	$\overline{CS}$=V_{IH}		-	20	mA
I_{SBP}	Peak Power-on Current	$\overline{CS}$=V_{CC}, V_{CC}=0 ∿ 5.5V		-	40	mA

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	8	

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	45	-	ns
t_{ACC}	Address Access Time	-	25	-	35	-	45	
t_{CO}	Chip Select Access Time	-	25	-	35	-	45	
t_{CLZ}	Chip Selection to Output in Low-Z	5	-	5	-	5	-	
t_{CHZ}	Chip Deselection to Output in High-Z	0	15	0	20	-	20	
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	20	-	30	-	30	

Write Cycle

SYMBOL	PARAMETER	TMM2068AP-25		TMM2068AP-35		TMM2068AP-45		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	20	-	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	20	-	30	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	0	-	0	-	0	-	
t_{WHZ}	$\overline{WE}$ to Output in High-Z	0	10	0	15	0	15	
t_{DS}	Data Set Up Time	10	-	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	2.0V/0.8V
Output Load	See Fig.1

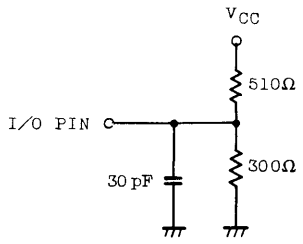
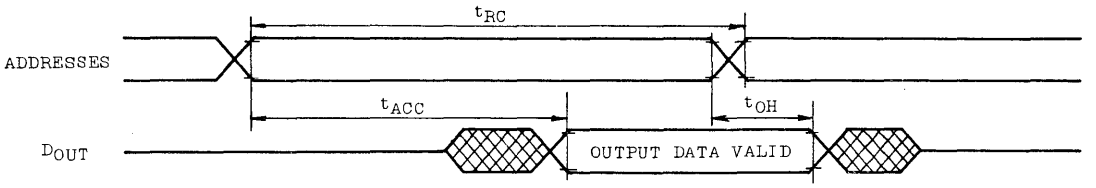


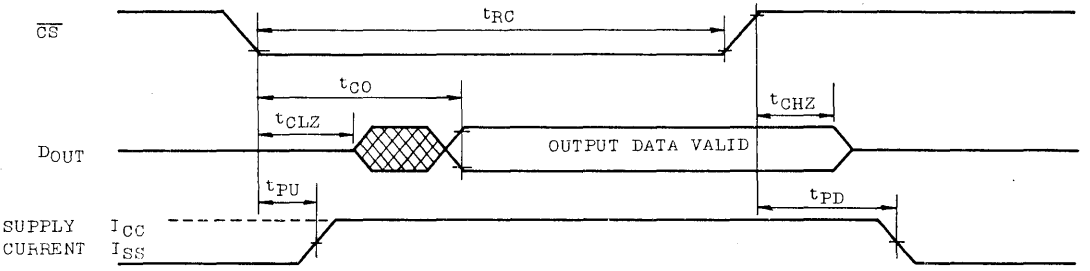
Fig.1 OUTPUT LOAD

TIMING WAVEFORMS

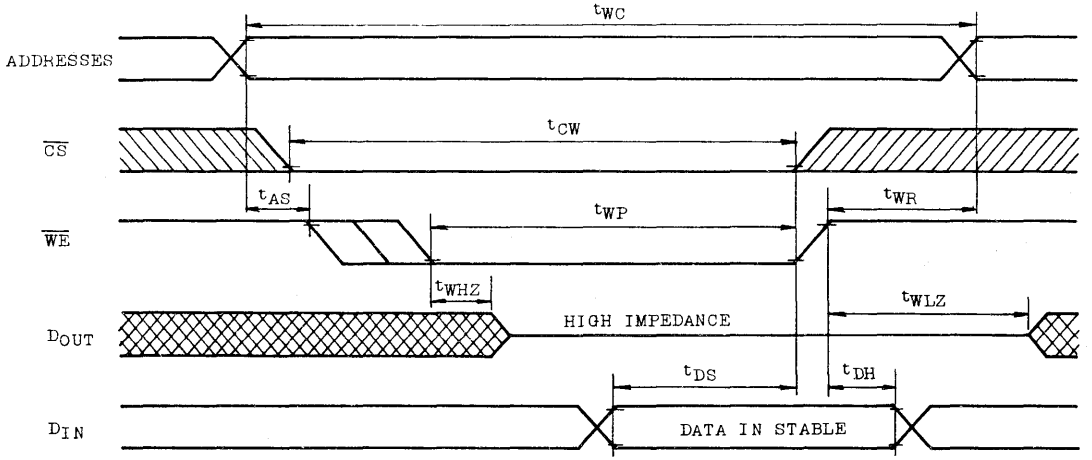
READ CYCLE 1. ($\overline{WE}$=V_{IH}, $\overline{CS}$=V_{IL})



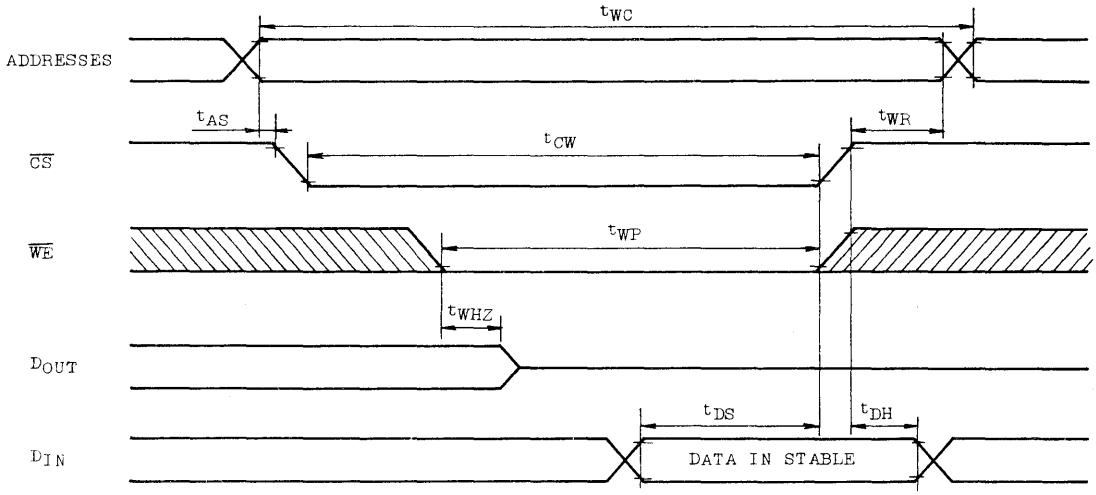
READ CYCLE 2. ($\overline{WE}$=V_{IH})



WRITE CYCLE 1.



WRITE CYCLE 2.

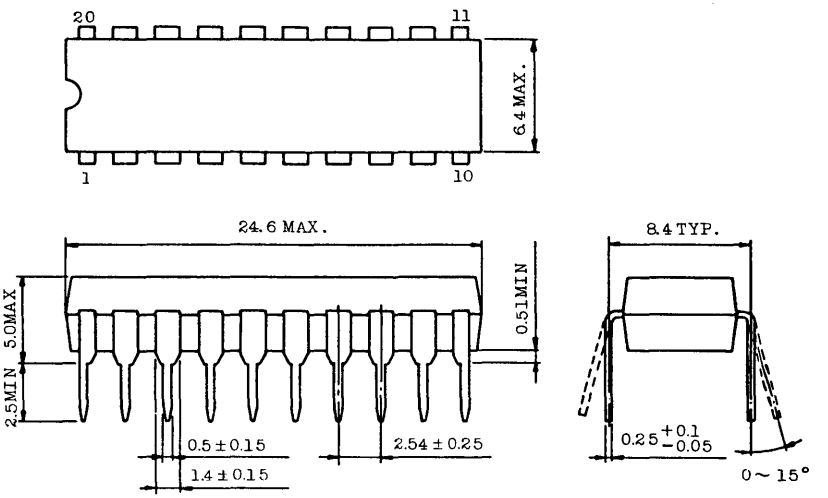


Note 1. In read cycle 2, all addresses are valid prior to or coincident with $\overline{CS}$ transition low.

2. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm



Note: Each lead pitch is 2.54mm.

All leads are located within 0.25mm of their longitudinal position with respect to No.1 and No.20 leads.

8,192 WORD × 8 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2088P-35, TMM2088P-45

DESCRIPTION

The TMM2088P is a 65,536 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 8 bits and operates from a single 5-volt supply. The TMM2088P is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2088P suitable for use in cache memory and high speed storage. The TMM2088P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

FEATURES

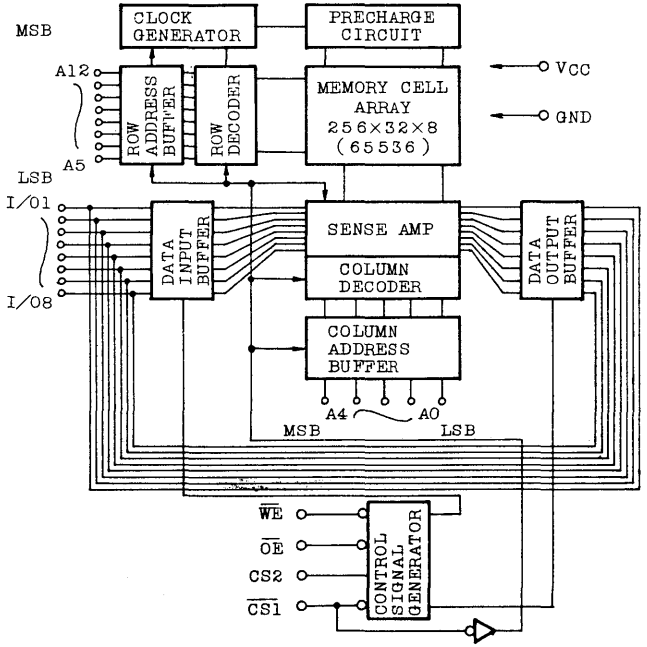
• Access Time and Current

Part Number \ Parameter	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2088P-35	35ns	135mA	15mA
TMM2088P-45	45ns	135mA	15mA

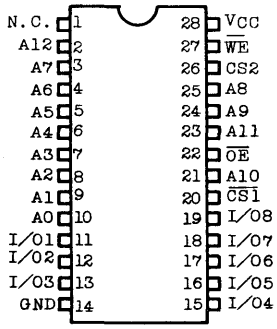
• Single 5V Power Supply
• Fully Static Operation
• Power Down Feature: ($\overline{CS1}$)
• Output Buffer Control: ($\overline{OE}$)
• Three State Outputs
• All Inputs and Outputs:
(Directly TTL Compatible)

• Inputs Protected: (All inputs have protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0 ∿ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground
N.C.	No Connection

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ∿ 8	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-3.5 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V (Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	-	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V∿5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	-	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	pF

* Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	ns
t_{ACC}	Address Access Time	-	35	-	45	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	15	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	
t_{PD}	Chip Deselection to POwer Down Time	-	30	-	30	

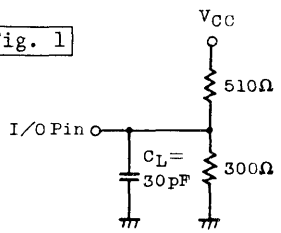
WRITE CYCLE

SYMBOL	PARAMETER	TMM2088P-35		TMM2088P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	ns
t_{CW}	Chip Selection to End of Write	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	
t_{WHZ}	Output Disable Time from $\overline{WE}$	-	15	-	15	

A.C. TEST CONDITIONS

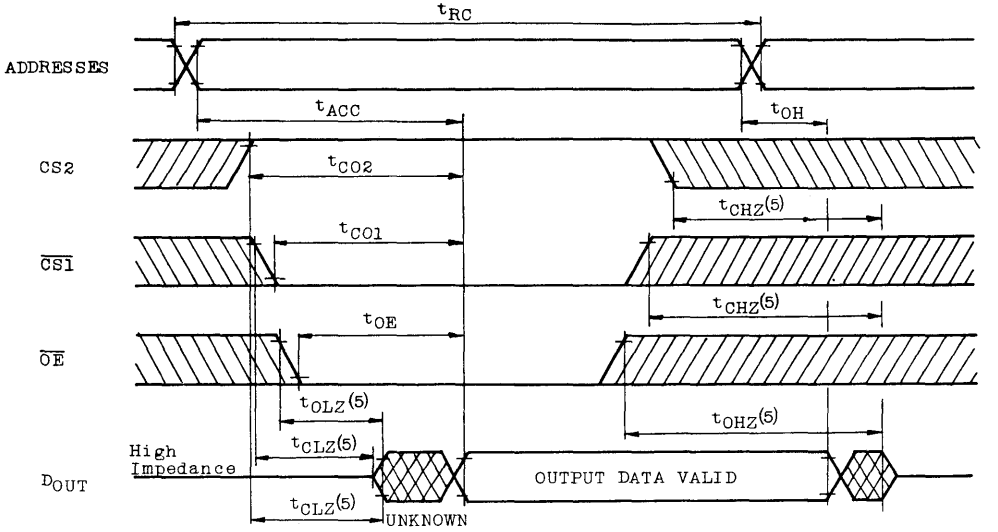
Input Pulse Levels	0.0 ∿ 3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levels	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

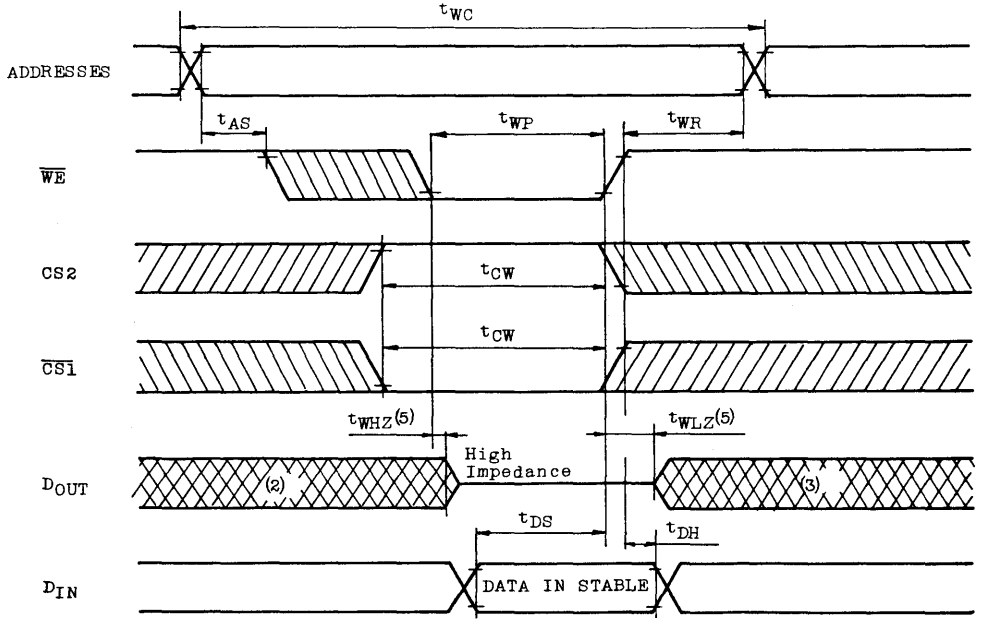


TIMING WAVEFORMS

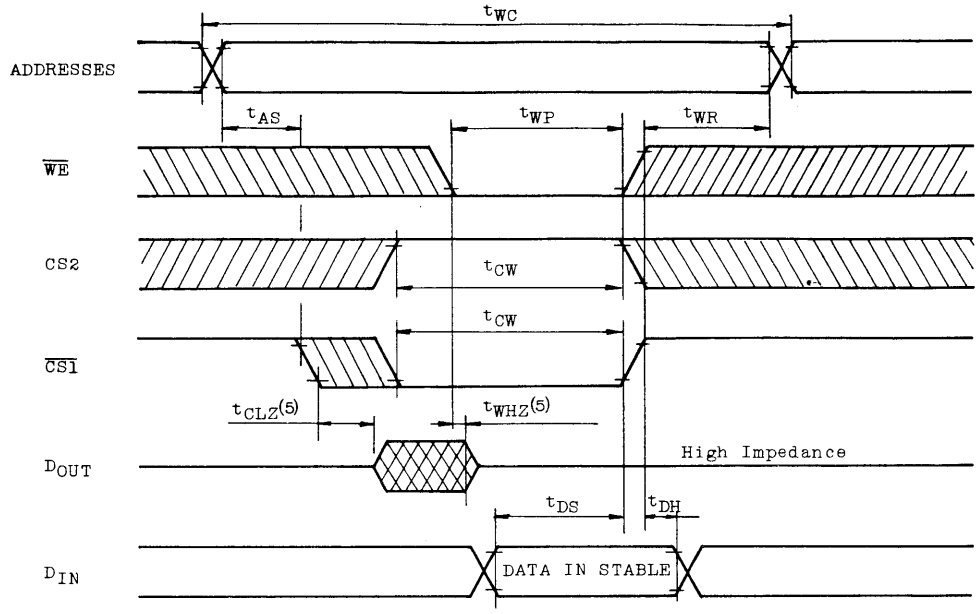
READ CYCLE (1)



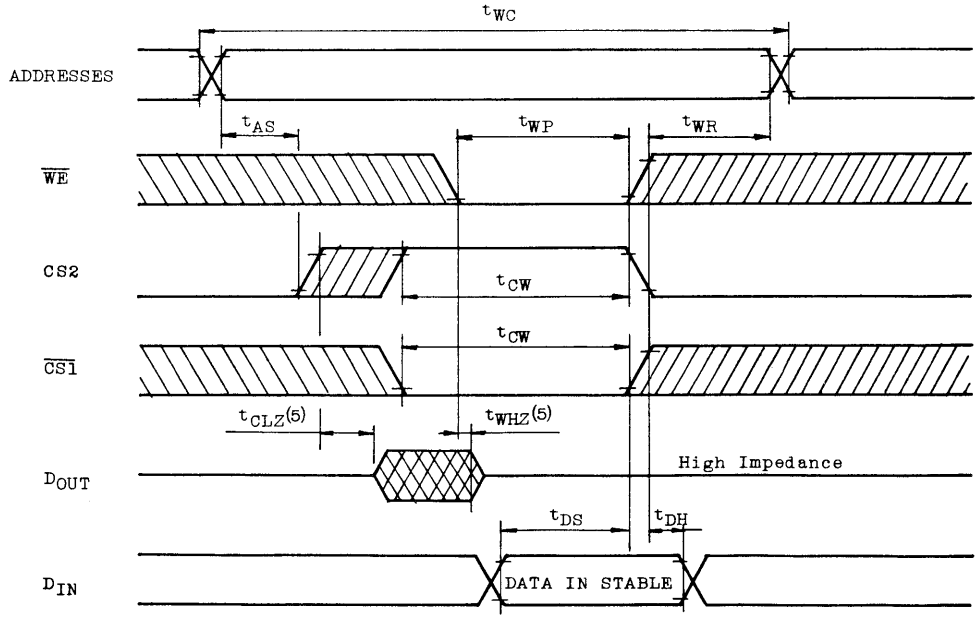
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

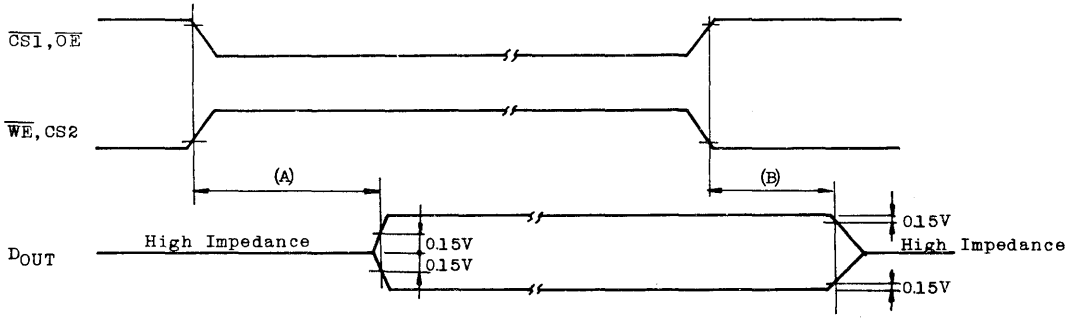
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

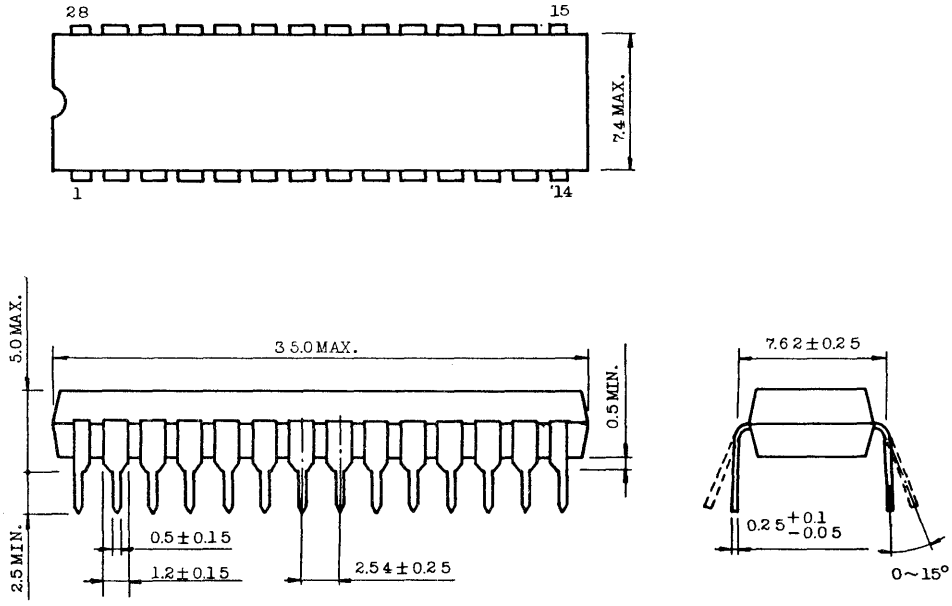
(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note: Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

8,192 WORD × 9 BIT STATIC RAM
N-CHANNEL SILICON GATE MOS

TMM2089P-35, TMM2089P-45

DESCRIPTION

The TMM2089P is a 73,728 bits high speed N-channel silicon gate MOS static random access memory organized as 8,192 words by 9 bits and operates from a single 5-volt supply. The TMM2089P is features an automatic stand-by mode when deselect by $\overline{CS1}$ signal. Thus the TMM2089P is suitable for use in cache memory and high speed storage. TheTMM2089P has nine I/O terminals, therefore it is most suitable for MEMORY SYSTEM with Parity bit. The TMM2089P is offered in a 28 pin standard plastic dual in-line package with 0.3 inch width for high density assembly.

FEATURES

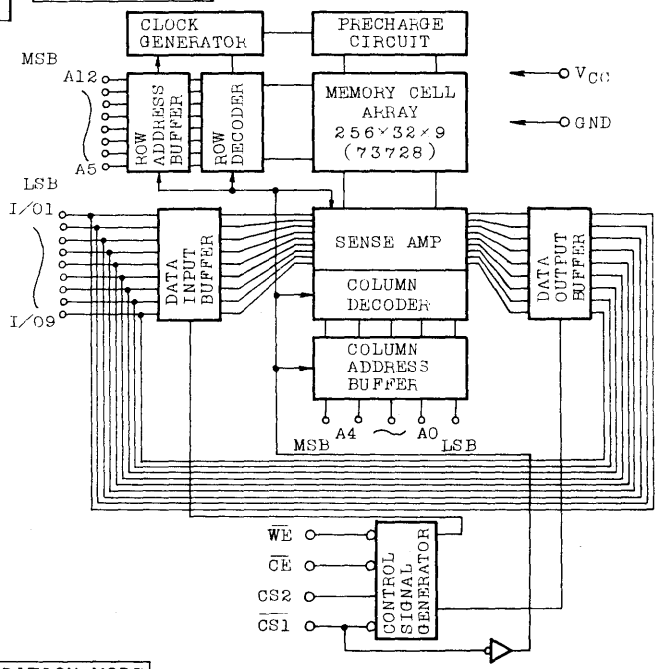
• Access Time and Current

Parameter / Part Number	Access Time (MAX.)	Operating Current (MAX.)	Standby Current (MAX.)
TMM2089P-35	35ns	135mA	15mA
TMM2089P-45	45ns	135mA	15mA

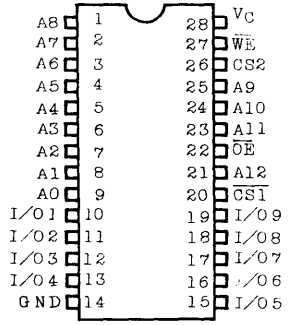
- Single 5V Power Supply
- Fully Static Operation
- Power Down Feature: ($\overline{CS1}$)
- Output Buffer Control: ($\overline{OE}$)
- Three State Outputs
- All Inputs and Outputs: (Directly TTL Compatible)

• Inputs Protected: (All inputs have protection against static charge.)

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0 ∿ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS1}$, CS2	Chip Select Inputs
I/O1 ∿ I/O9	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

OPERATION MODE

MODE	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	I/O1 ∿ 9	Power
Write	L	H	*	L	In	Active
Read	L	H	L	H	Out	Active
Standby	H	*	*	*	High-Z	Standby
Standby	L	L	*	*	High-Z	Active
Output Buffer Disable	L	H	H	H	High-Z	Active

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-3.5 ∿ 7.0	V
V_{IN}, V_{OUT}	Input Output Voltage	-3.5 ∿ 7.0	V
$T_{opr.}$	Operating Temperature	0 ∿ 70	°C
$T_{stg.}$	Storage Temperature	-55 ∿ 150	°C
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
P_D	Power Dissipation (Ta=70°C)	1.0	W

D.C. RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-3.0*	-	0.8	V
V_{CC}	Supply Voltage	4.5	5.0	5.5	V

* Pulse Width: 10ns, DC: -0.5V(Min.)

D.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5.0V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0V ∿ 5.5V	-1.0	1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V	-4.0	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V	8.0	-	mA
I_{LO}	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, V_{OUT}=0V ∿ 5.5V	-1.0	1.0	μA
I_{SBP}	Peak Power-on Current	$\overline{CS1}$=V_{CC}, CS2=0V, I_{OUT}=0mA	-	30	mA
I_{SB}	Standby Current	$\overline{CS1}$=V_{IH}, I_{OUT}=0mA	-	15	mA
I_{CC}	Operating Current	$\overline{CS1}$=V_{IL}, I_{OUT}=0mA	-	135	mA

CAPACITANCE* (Ta=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{OUT}	Output Capacitance	V_{IN}=0V	10	

* Note: This parameter is periodically smapled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ~ 70°C, V_{CC}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TMM2080P-35		TMM2089P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	ns
t_{ACC}	Address Access Time	-	35	-	45	
t_{CO1}	$\overline{CS1}$ Access Time	-	35	-	45	
t_{CO2}	CS2 Access Time	-	25	-	25	
t_{OE}	$\overline{OE}$ Access Time	-	20	-	20	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	
t_{CLZ}	Output Enable Time from $\overline{CS1}$ or CS2	0	-	5	-	
t_{CHZ}	Output Disable Time from $\overline{CS1}$ or CS2	-	20	-	20	
t_{OLZ}	Output Enable Time from $\overline{OE}$	0	-	0	-	
t_{OHZ}	Output Disable Time from $\overline{OE}$	-	15	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	30	-	30	

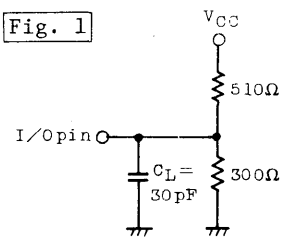
WRITE CYCLE

SYMBOL	PARAMETER	TMM2089P-35		TMM2089P-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	ns
t_{CS}	Chip Selection to End of Write	30	-	40	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WP}	Write Pulse Width	25	-	35	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{DS}	Data Set Up Time	15	-	20	-	
t_{DH}	Data Hold Time	0	-	0	-	
t_{WLZ}	Output Enable Time from $\overline{WE}$	0	-	0	-	
t_{WHZ}	Output Disable Timf from $\overline{WE}$	-	15	-	15	

A.C. TEST CONDITIONS

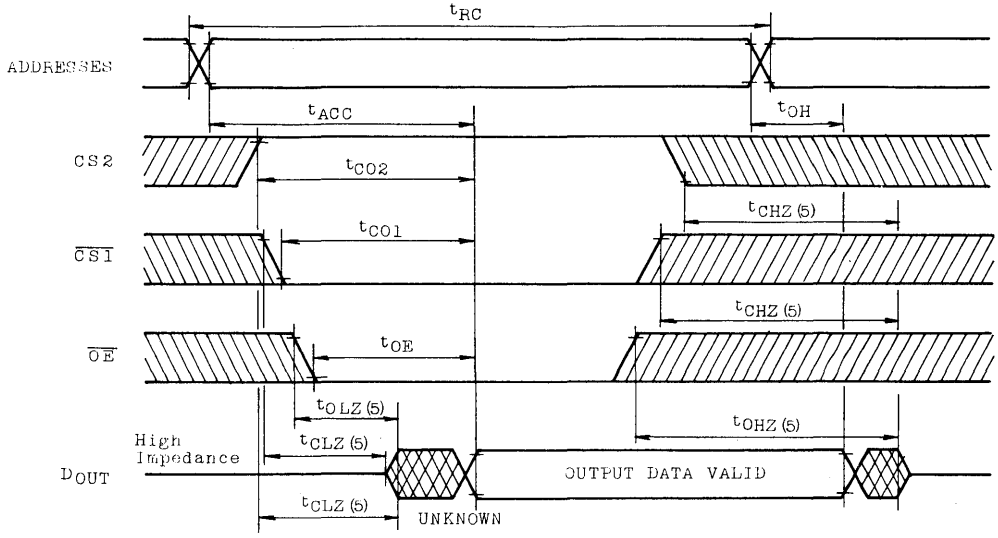
Input Pulse Levels	0.0V/3.0V
Input Rise and Fall Time	5ns
Input and Output Reference Levles	2.0V/0.8V
Output Load	Fig. 1

Fig. 1

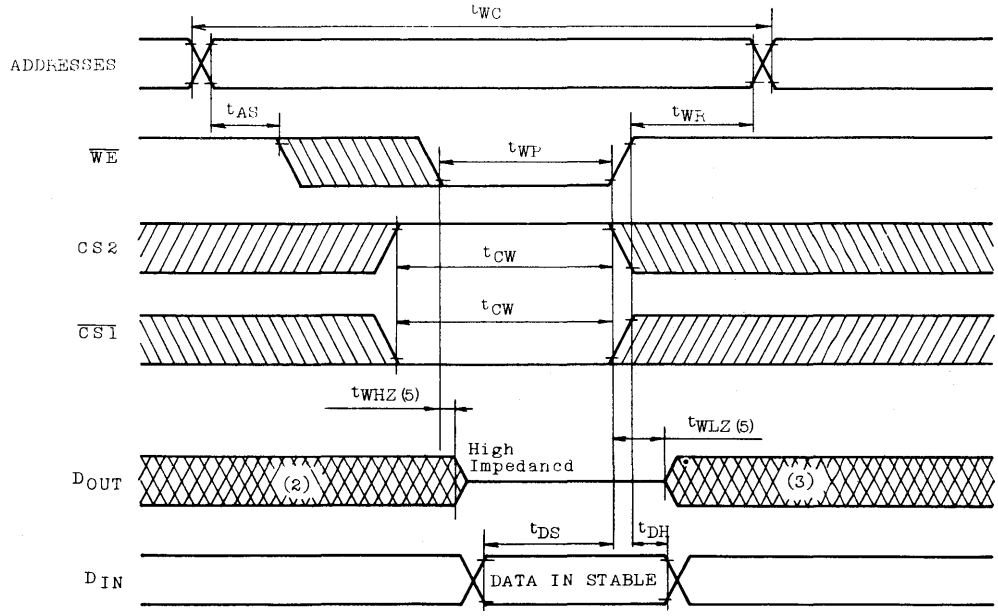


TIMING WAVEFORMS

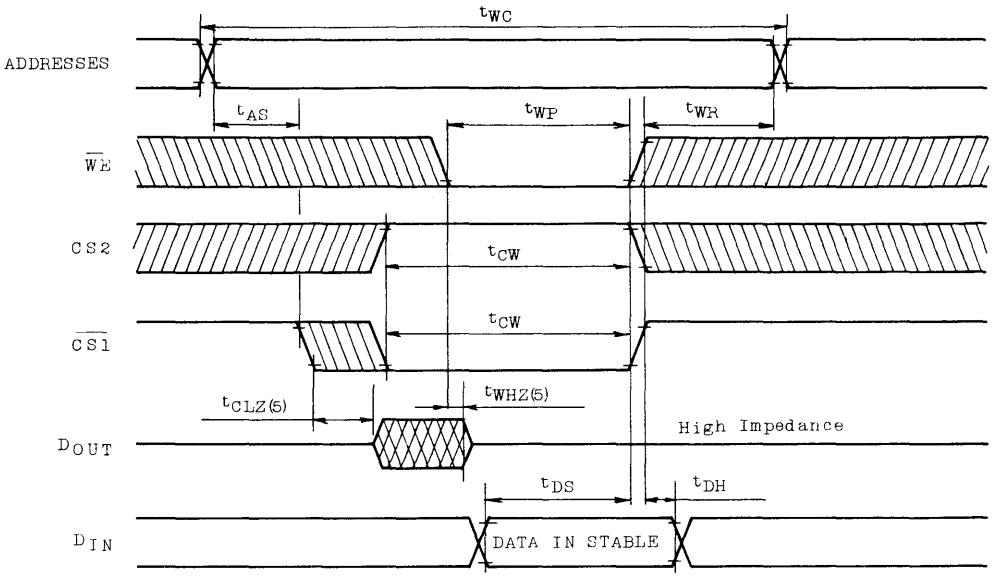
READ CYCLE (1)



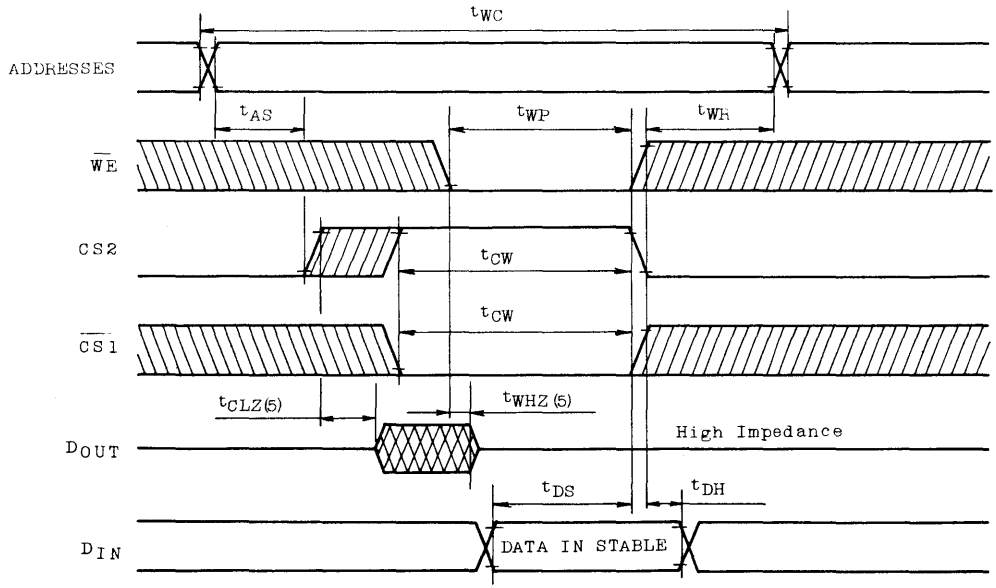
WRITE CYCLE 1 (4) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CS1}$ Controlled Write)



WRITE CYCLE 3 (4) (CS2 Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

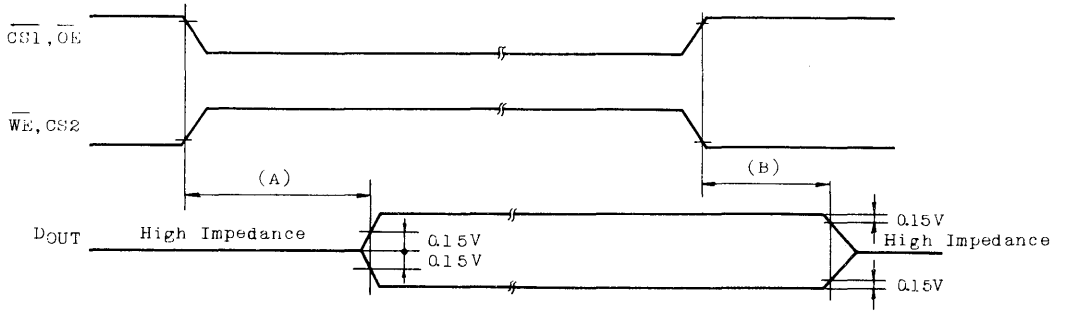
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

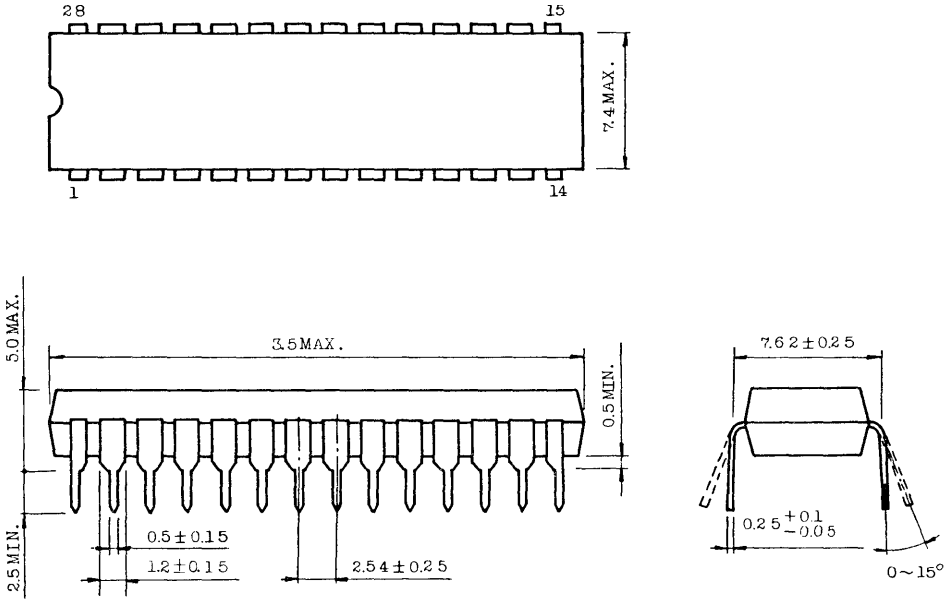
(A) t_{CLZ}, t_{OLZ}, t_{WLZ} ..... Output Enable Time

(B) t_{CHZ}, t_{OHZ}, t_{WHZ} ..... Output Disable Time



DIP 28 PIN OUTLINE DRAWING

Unit in mm



Note) Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

8,192 WORD×8 BIT CMOS STATIC RAM

TC5588P/J-20, TC5588P/J-25, TC5588P/J-35

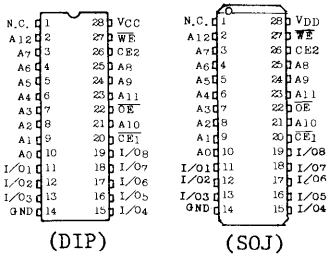
DESCRIPTION

The TC5588P/J is a 65,536 bit high speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 20ns/25ns/35ns and maximum operating current of 120mA at maximum cycle time. The TC5588P/J also features an automatic stand-by mode. The TC5588P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC5588P/J is moulded in a 28 pin standard plastic DIP and a 28 pin plastic SOJ, with 0.3 inch width for high density assembly. The TC5588P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time:
  - TC5588P/J-20 20ns (MAX.)
  - TC5588P/J-25 25ns (MAX.)
  - TC5588P/J-35 35ns (MAX.)
- Power dissipation: Operation 120mA (MAX.)
  Standby 20mA (MAX.)
- 5V single power supply
- Full static operation
- Directly TTL compatible: All input and output
- Package: 28 pin plastic 300 mil DIP (TC5588P)
  28 pin plastic 300 mil SOJ (TC5588J)

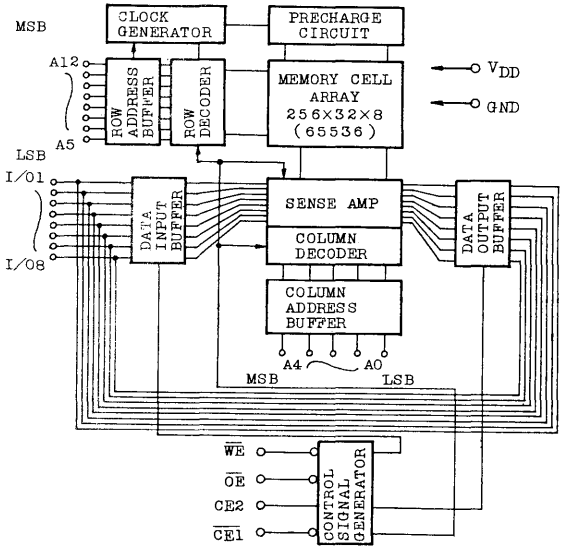
PIN CONNECTION



PIN NAME

A0 ~ A12	Address Input
I/01 ~ I/08	Data Input/Output
CE1, CE2	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
V	Power (5V)
GND	Ground

BLOCK DIAGRAM



8,192 WORD×9 BIT CMOS STATIC RAM

TC5589P/J-20, TC5589P/J-25, TC5589P/J-35

DESCRIPTION

The TC5589P/J is a 65,536 bit high speed static random access memory organized as 8,192 words by 9bits

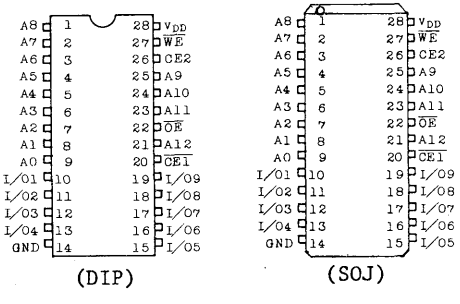
DESCRIPTION

The TC5589P/J is a 65,536 bit high speed static random access memory organized as 8,192 words by 9bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 20ns/25ns/35ns and maximum operating current of 120mA at maximum cycle time. The TC5589P/J also features an automatic stand-by mode. The TC5589P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC5589P/J is moulded in a 28 pin standard plastic DIP and a 28 pin plastic SOJ, with 0.3 inch width for high density assembly. The TC5589P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

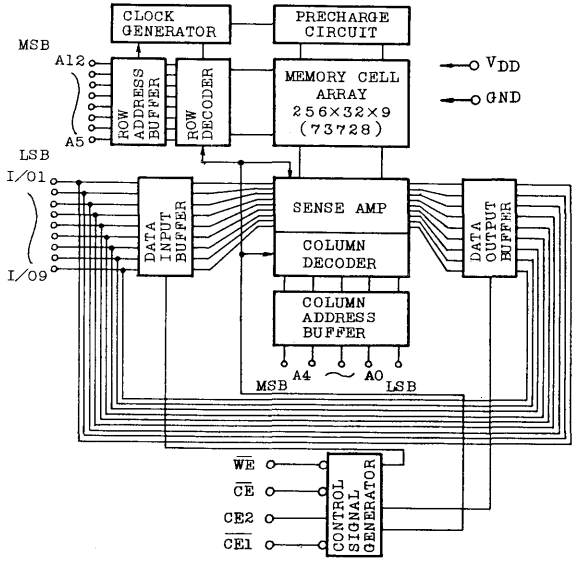
FEATURES

- Fast access time:
  - TC5589P/J-20 20ns (MAX.)
  - TC5589P/J-25 25ns (MAX.)
  - TC5589P/J-35 35ns (MAX.)
- Power dissipation: Operation 120mA (MAX.)
  Stand by 20mA (MAX.)
- 5V single power supply
- Full static operation
- Directly TTL compatible: All input and output
- Package: 28 pin plastic 300 mil DIP (TC5589P)
  28 pin plastic 300 mil SOJ (TC5589J)

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A13	Address Inputs
I/01 ~ I/04	Data Input/Output
CE1, CE2	Chip Enable Input
WE	Write Enable Input
OE	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5561P/J-45, TC5561P/J-55

DESCRIPTION

The TC5561P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and Operated from a single 5-volt supply.

Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45/55/70ns and maximum operating current of 100mA at minimum cycle time.

The TC5561P/J also features an automatic stand-by mode. When deselected by Chip Enable (CE), the operating current is reduced from 100mA to 100μA.

The TC5561P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required.

The TC5561P is moulded in a 22 pin standard plastic SOJ with 300 ml width for high density surface assembly.

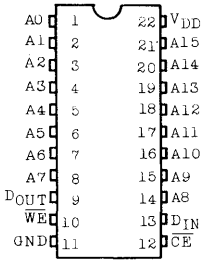
The TC5561P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time : TC5561P/J-45 45ns (MAX.)
  TC5561P/J-55 55ns (MAX.)
- Low power dissipation : Operation100mA(MAX.)
  Standby100μA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible : All Input and Output
- I/O separate
- Package : 22 pin standard plastic package, 300mil width: TC5561P
  24 pin plastic 300 mil SOJ : TC5561J

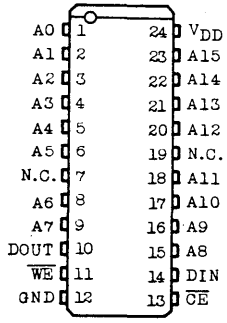
PIN CONNECTION (TOP VIEW)

TC5561P



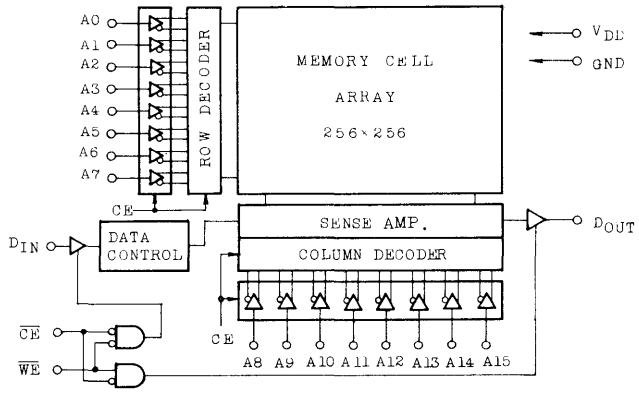
(300mil DIP)

TC5561J
(TOP VIEW)



(SOJ)

BLOCK DIAGRAM



PIN NAMES

A_0~A_{15}	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V

D. C. and OPERATING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	2	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$	—	—	100	μA

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5561P/J-45		TC5561P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	–	55	–	ns
t_{ACC}	Address Access Time	–	45	–	55	
t_{CO}	Chip Enable Access Time	–	45	–	55	
t_{COE}	Chip Enable to Output in Low-Z	10	–	10	–	
t_{COD}	Chip Disable to Output in High-Z	–	15	–	15	
t_{OH}	Output Data Hold Time	5	–	5	–	

Write Cycle

SYMBOL	PARAMETER	TC5561P/J-45		TC5561P/J-55		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	45	–	55	–	ns
t_{WP}	Write Pulse Width	30	–	35	–	
t_{CW}	Chip Enable to End of Write	30	–	35	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{OEW}	WE to Output Low-Z	0	–	0	–	
t_{ODW}	WE to Output High-Z	–	15	–	15	
t_{DS}	Data Set up Time	25	–	25	–	
t_{DH}	Data Hold Time	0	–	0	–	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

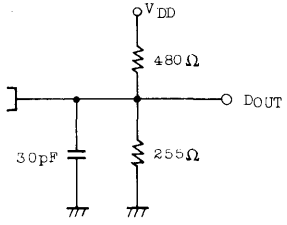
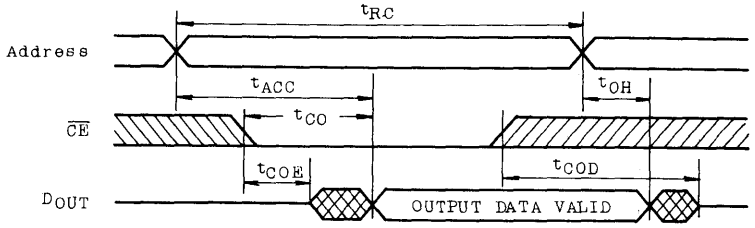


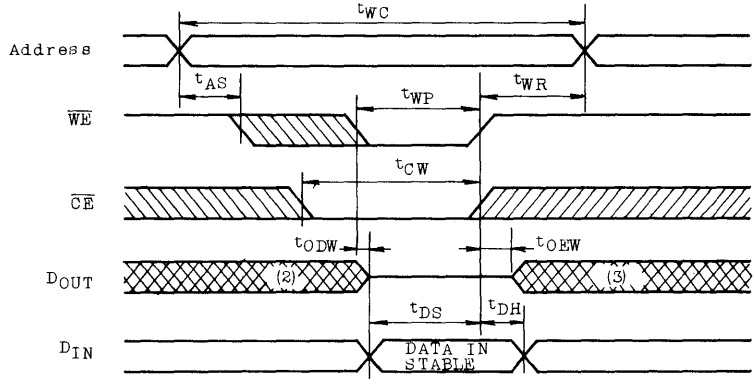
Fig.1 Output Load

TIMING WAVEFORMS

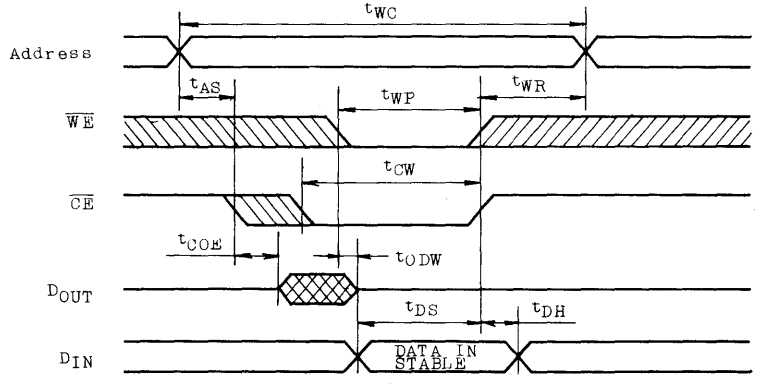
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

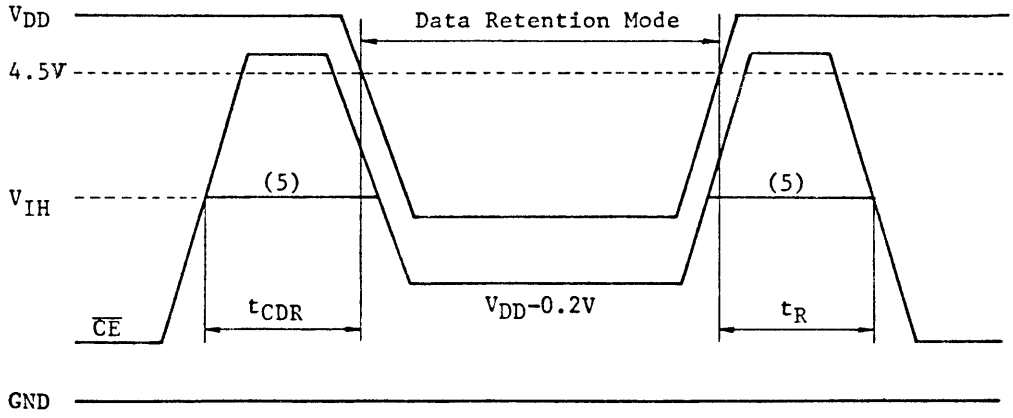


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

DATA RETENTION CHARACTERISTICS (Ta = −40~50°C)

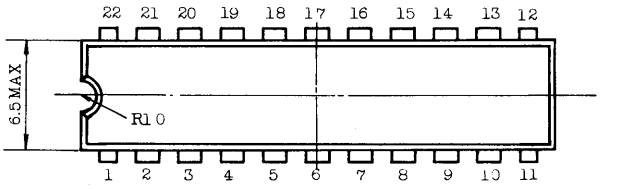
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	—	—	50	μA
		V_{DD}=5.5V	—	—	100	μA
t_{CDH}	Chip Deselection to Data Retntion Mode		0	—	—	μs
t_R	Recovery Time		t_{RC}(1)	—	—	μs

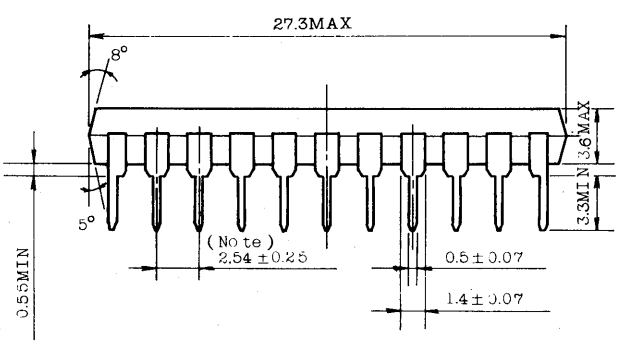


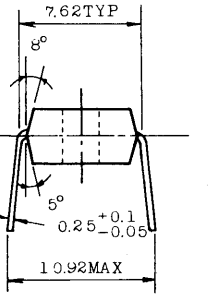
5. If the v_{IH} of $\overline{CE_1}$ is 2.2V in operation, I_{DDS1} current flows the period that v_{DD} voltage is going down from 4.5V to 2.5V.

OUTLINE DRAWINGS

Unit in mm



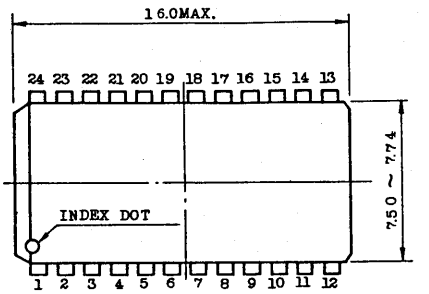


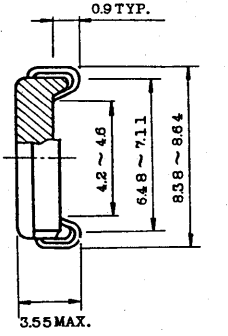


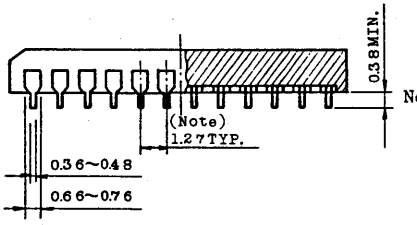
Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

• **Plastic SOJ**

Unit in mm







Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the ture longitudinal position with respect to No.1 and No.24 leads.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 1 BIT CMOS STATIC RAM
SILICON GATE CMOS

TC5562P/J-35, TC5562P/J-45

DESCRIPTION

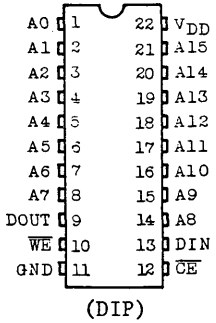
The TC5562P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns/55ns and maximum operating current of 100mA at minimum cycle time. The TC5562P/J also features and automatic standby mode. When deselected by chip Enable (CE), the operating current is reduced from 100mA to 20mA. The TC5562P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/high density are required. The TC5562P is moulded in a 22 pin plastic DIP with 300 mil width for high density surface assembly and the TC5562J is moulded in a 24 pin plastic SOJ with 300 mil width for high density surface assembly. The TC5562P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time: TC5562P/J-35 35ns(MAX.)
  TC5562P/J-45 45ns(MAX.)
- Low power dissipation:
  Operation 100mA (MAX.)
  Standby 20mA (MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- I/O separate
- Package: 22 Pin Plastic 300 mil DIP : TC5562P
  24 Pin Plastic 300 mil SOJ : TC5562J

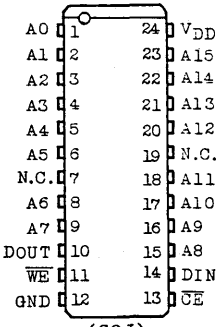
PIN CONNECTION

TC5562P
(TOP VIEW)



(DIP)

TC5562J
(TOP VIEW)

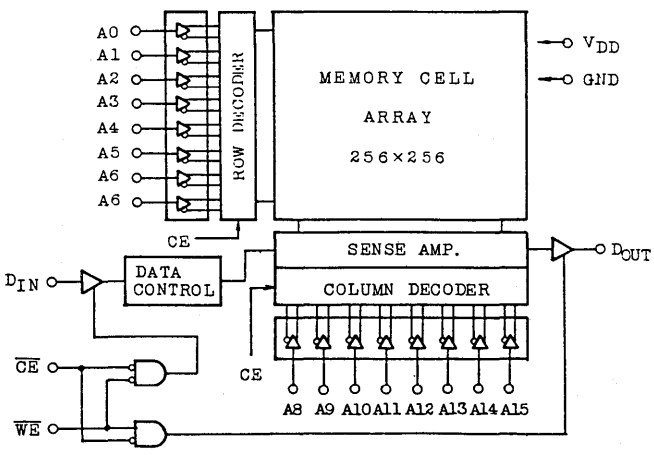


(SOJ)

PIN NAMES

A0 ∿ A15	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{SOLDER}	Soldering Temperature	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~150	°C
T_{OPR}	Operating Temperature	0~70	°C

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−3.0	—	0.8	V

D. C and OPERATING CHARACTERISTICS

($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$	—	—	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	−8	—	—	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0\sim V_{DD}$	—	—	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, tcycle=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	—	—	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	—	—	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or 0.2V	—	—	2	

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	pF

Note : This parameter periodically sampled is not 100% tested.

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	–	45	–	ns
t_{ACC}	Address Access Time	–	35	–	45	
t_{CO}	Chip Enable Access Time	–	35	–	45	
t_{COE}	Chip Enable to Output in Low-Z	5	–	5	–	
t_{COD}	Chip Disable to Output in High-Z	–	15	–	15	
t_{OH}	Output Data Hold Time	5	–	5	–	

Write Cycle

SYMBOL	PARAMETER	TC5562P/J-35		TC5562P/J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	–	45	–	ns
t_{WP}	Write Pulse Width	25	–	30	–	
t_{CW}	Chip Enable to End of Write	25	–	30	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	
t_{OEW}	WE to Output Low-Z	0	–	0	–	
t_{ODW}	WE to Output High-Z	–	15	–	15	
t_{DS}	Data Set up Time	20	–	25	–	
t_{DH}	Data Hold Time	0	–	0	–	

A. C. TEST CONDITIONS

Input Pulse Levels	2.4V/0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

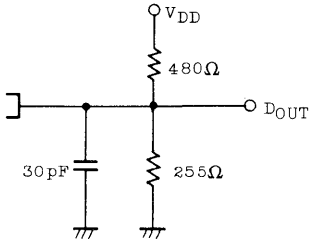
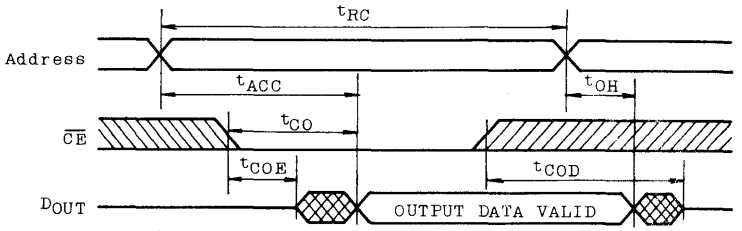


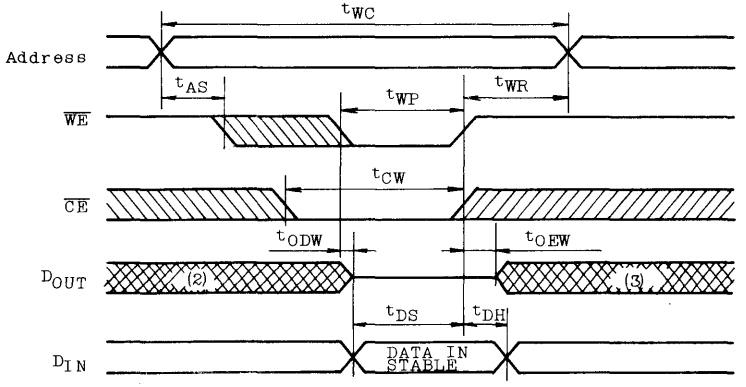
Fig.1 Output Load

TIMING WAVEFORMS

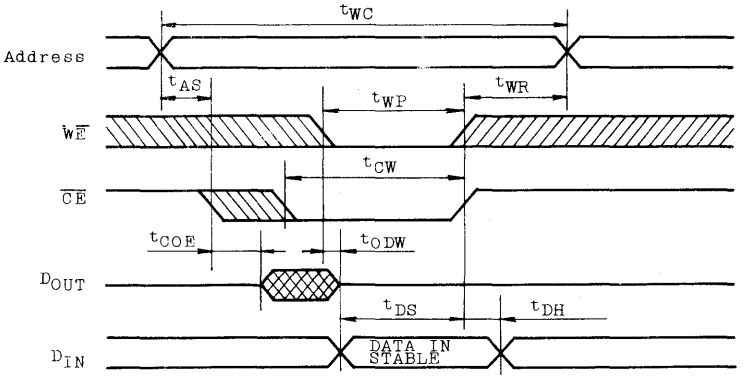
- READ CYCLE (1)



- WRITE CYCLE 1 ($\overline{WE}$ Controled Write)



- WRITE CYCLE 2 ($\overline{CE}$ Controled Write)

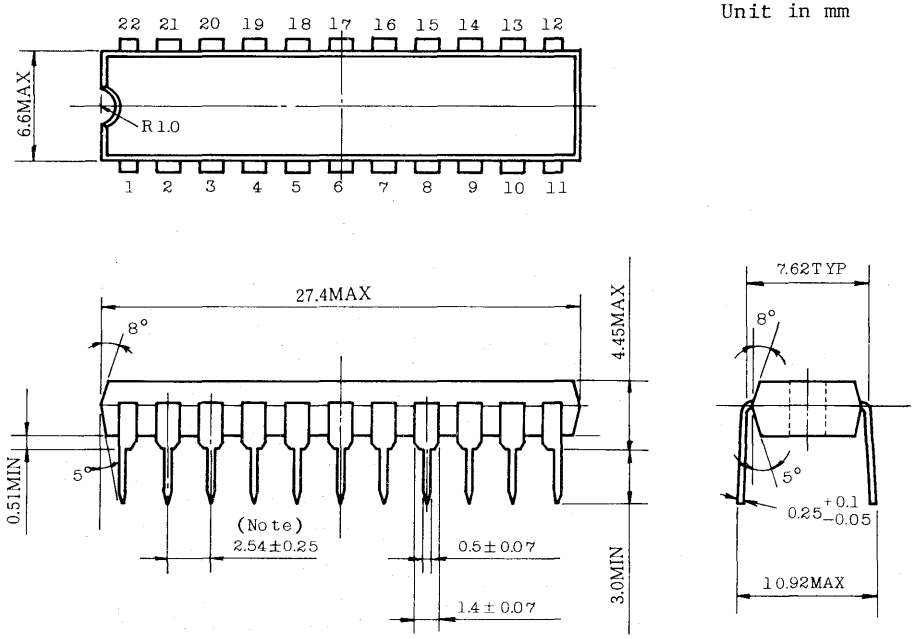


Note :

1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The operating temperature(Ta) in guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

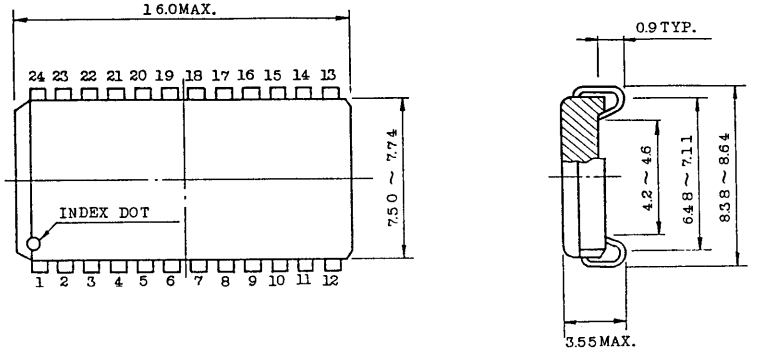
Unit in mm

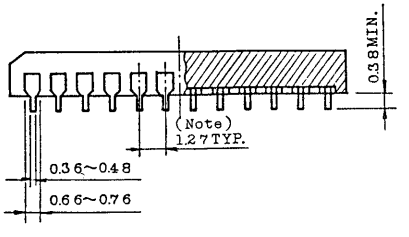


Note : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

• Plastic SOJ

Unit in mm





Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the ture longitudinal position with respect to No. 1 and No. 24 leads.

TC55416P/J-25, TC55416P/J-35

DESCRIPTION

The TC55416P/J is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns and maximum operating current of 120mA/100mA at minimum cycle time.

The TC55416P/J also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 20mA.

The TC55416P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required.

The TC55416P/J is moulded in a 22 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

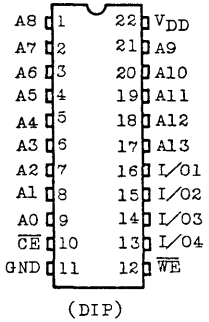
The TC55416P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time:
  - TC55416P/J-25 25ns(MAX.)
  - TC55416P/J-35 35ns(MAX.)
- Low power dissipation:
  - Operation TC55416P/J-25 120mA(MAX.)
  - TC55416P/J-35 100mA(MAX.)
  - Standby 20mA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- Package:
  - 22 pin plastic 300mil DIP (TC55416P)
  - 24 pin plastic 300mil SOJ (TC55416J)

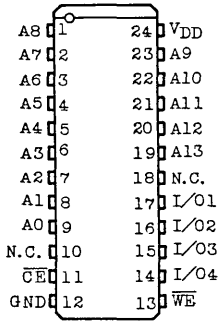
PIN CONNECTION

TC55416P



(DIP)

TC55416J

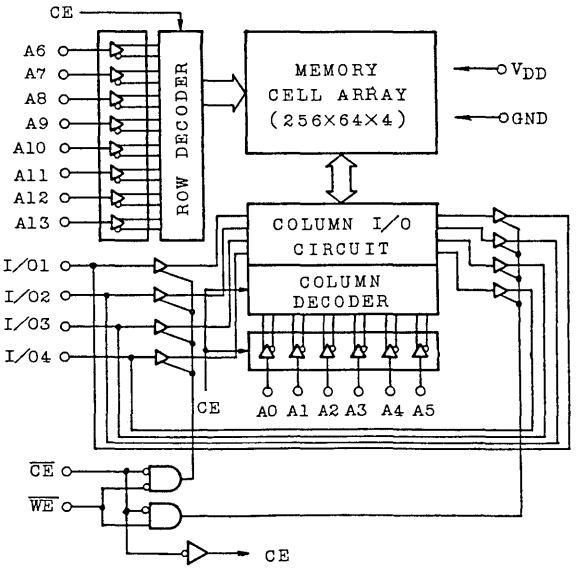


(SOJ)

PIN NAMES

A0 ∿ A13	Address Inputs
I/O1 ∿ I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature	260·10	°C·sec
T_{stg}	Storage Temperature	-65~150	°C
T_{opr}	Operating Temperature	0~70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0~V_{DD}		-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=0~V_{DD}		-	-	±1.0	μA
I_{DDO}	Operating Current	V_{DD}=5.5V t_{cycle}=Min cycle	-25	-	-	120	mA
		$\overline{CE}$=V_{IL} Other Input=V_{IH}/V_{IL}	-35	-	-	100	
I_{DDS1}	Standby Current	V_{DD}=5.5V, t_{cycle}=Min cycle $\overline{CE}$=V_{IH}, Other Input=V_{IH}/V_{IL}		-	-	20	mA
I_{DDS2}		$\overline{CE}$=V_{DD}-0.2V Other Input=V_{DD}-0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	7	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	9	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC55416P-25 TC55416J-25		TC55416P-35 TC55416J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	ns
t_{ACC}	Address Access Time	-	25	-	35	ns
t_{CO}	Chip Enable Access Time	-	25	-	35	ns
t_{COE}	Chip Enable to Output in Low-Z	0	-	0	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	15	ns
t_{OH}	Output Data Hold Time	5	-	5	-	ns

Write Cycle

SYMBOL	PARAMETER	TC55416P-25 TC55416J-25		TC55416P-35 TC55416J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	ns
t_{WP}	Write Pulse Width	20	-	30	-	ns
t_{CW}	Chip Enable to End of Write	20	-	30	-	ns
t_{AS}	Address Set Up Time	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	10	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t_{DS}	Data Set Up Time	12	-	15	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.0V, 3.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig.1

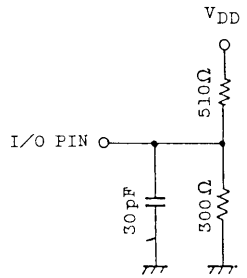
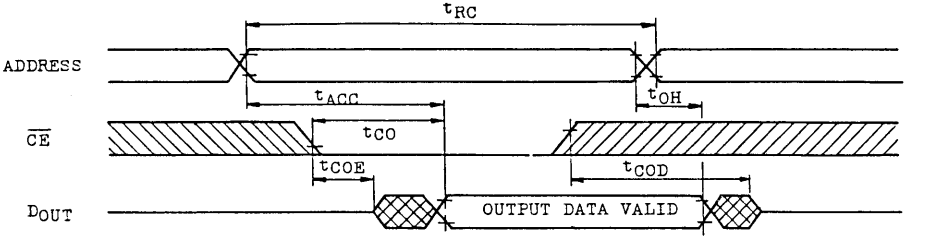


Fig.1 OUTPUT LOAD

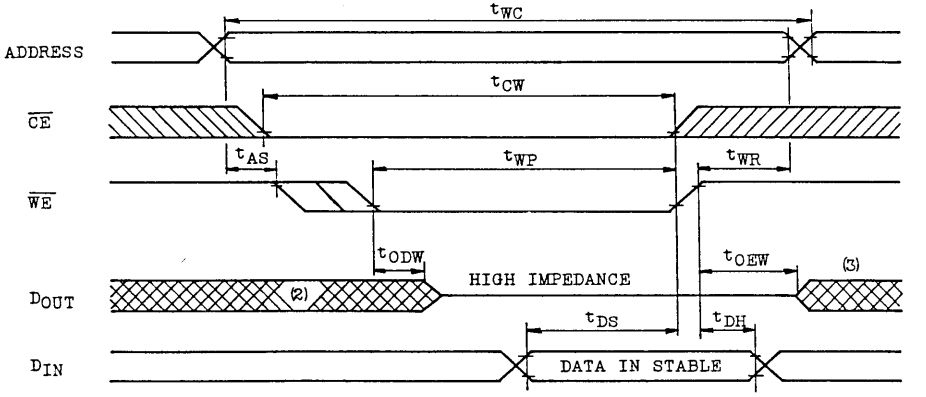
Note: In all condition, t_{COD} max is less than t_{COE} min both for a given device and from device to device.

TIMING WAVEFORMS

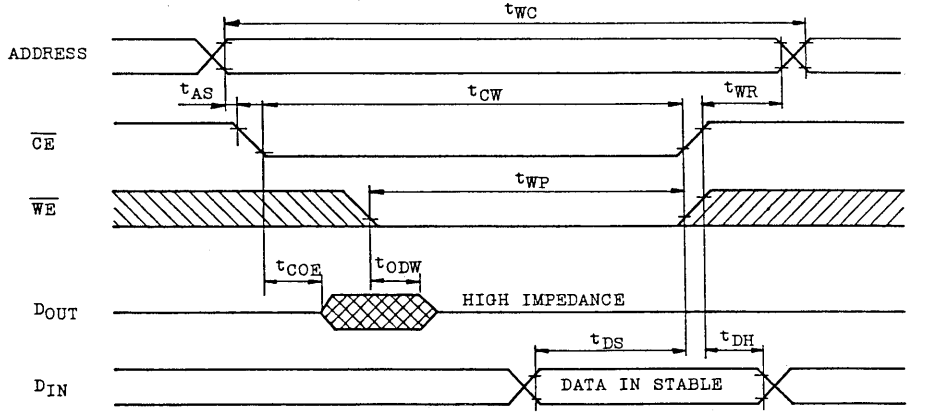
READ CYCLE(1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

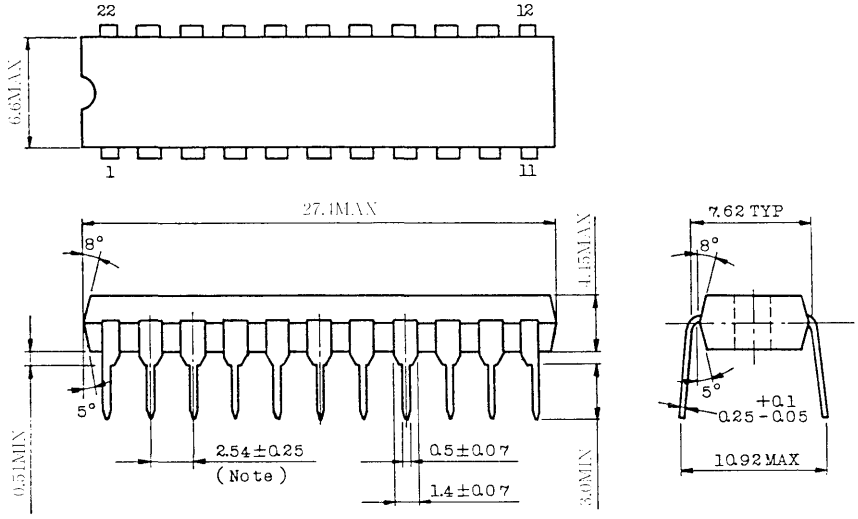


Note: 1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

Unit in mm

∘ Plastic DIP

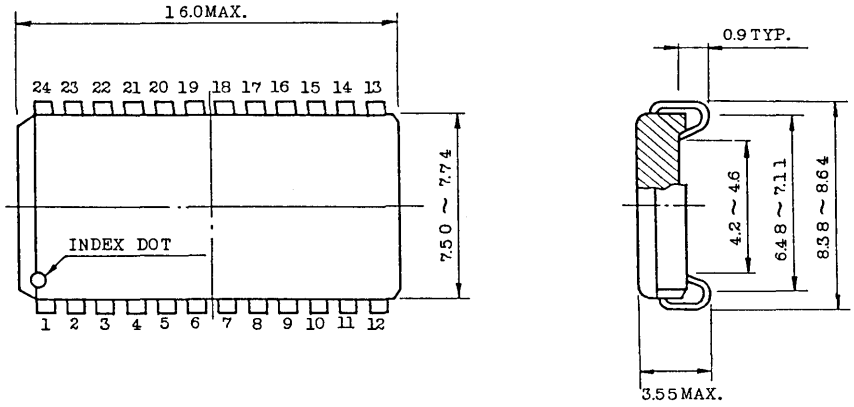


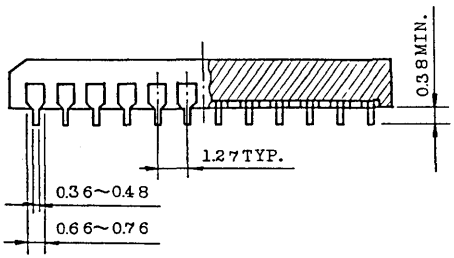
Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.22 leads.

OUTLINE DRAWINGS

∘ Plastic SOJ

Unit in mm





Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the true longitudinal position with respect to No.1 and No.24 leads.

TC55417P/J-25
TC55417P/J-35

DESCRIPTION

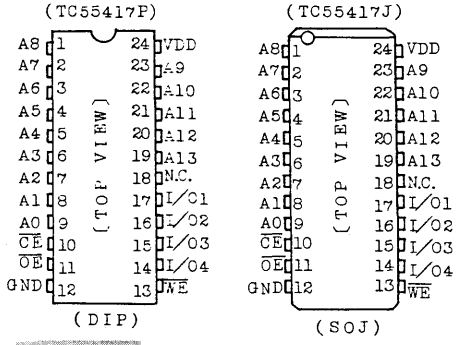
The TC55417P/J is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operated from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 25ns/35ns/45ns and maximum operating current of 120mA/100mA/100mA at maximum cycle time. The TC55417P/J also features an automatic stand-by mode. When deselected by Chip Enable($\overline{CE}$), the operating current is reduced to 20mA. The TC55417P/J is suitable for use in cache memory and high speed storage, where high speed/high density are required. The TC55417P/J is moulded in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly. The TC55417P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time: TC55417P/J-25 25ns(MAX.)
  TC55417P/J-35 35ns(MAX.)

- Low power dissipation: Operation TC55417P/J-25 120mA(MAX.)
  TC55417P/J-35 100mA(MAX.)
  Standby 20mA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Input and Output
- Output buffer control: $\overline{OE}$
- Package: 24 Pin plastic 300 mil DIP (TC55417P)
  24 Pin plastic 300 mil SOJ (TC55417J)

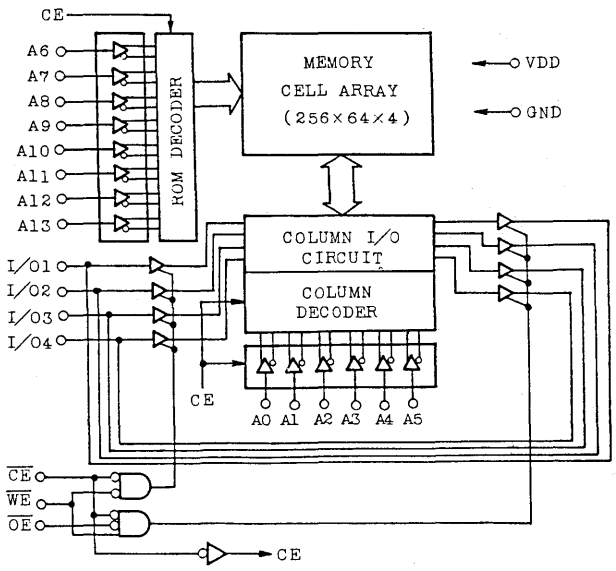
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-2.0 ∿ 7.0	V
V_{OUT}	Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature • Time	260 • 10	°C•sec
T_{stg}	Storage Temperature	-65 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		-4	-	-	mA
I_{OL}	Output low Current	$V_{OL}=0.4V$		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$ tcycle=Min cycle $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	-25	-	-	120	mA
			-35	-	-	100	
I_{DDS1}	Standby Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle $\overline{CE}=V_{IH}$, Other Input=V_{IH}/V_{IL}		-	-	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or 0.2V		-	-	1	

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	7	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	9	pF

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

Read Cycle

SYMBOL	PARAMETER	TC55417P/J-25		TC55417P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	25	-	35	-	ns
t_{ACC}	Address Access Time	-	25	-	35	
t_{CO}	Chip Enable Access Time	-	25	-	35	
t_{OE}	Output Enable to Output Valid	-	15	-	20	
t_{COE}	Chip Enable to Output in Low-Z	0	-	0	-	
t_{COD}	Chip Enable to Output in High-Z	-	15	-	15	
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	
t_{ODO}	Output Enable to Output in High-Z	-	10	-	15	
t_{OH}	Output Data Hold Time	5	-	5	-	

Write Cycle

SYMBOL	PARAMETER	TC55417P/J-25		TC55417P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	25	-	35	-	ns
t_{WP}	Write Pulse Width	20	-	30	-	
t_{CW}	Chip Enable to End of Write	20	-	30	-	
t_{AS}	Address Set Up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	$\overline{WE}$ to Output High-Z	-	10	-	15	
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	
t_{DS}	Data Set Up Time	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

Input Pulse Levels	0.0V, 3.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	0.8V, 2.0V
Output Load	See Fig. 1

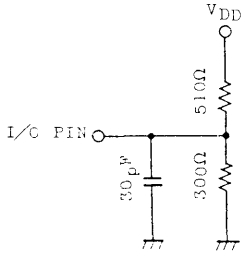
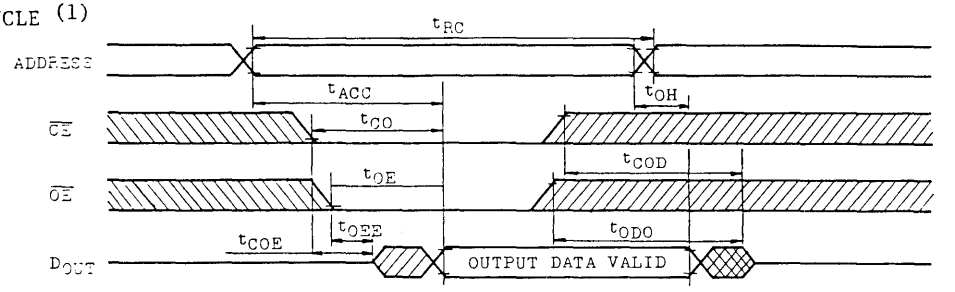


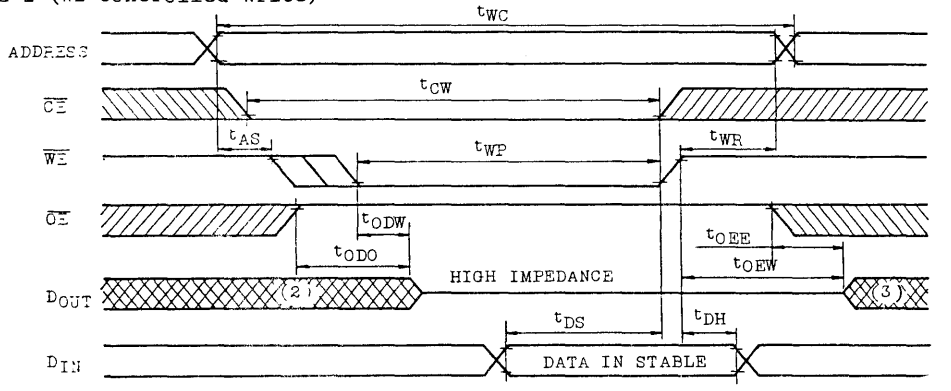
Fig.1 OUTPUT LOAD

Note: In all condition, t_{COD} max is less than t_{COE} min both for a given device and from device to device.

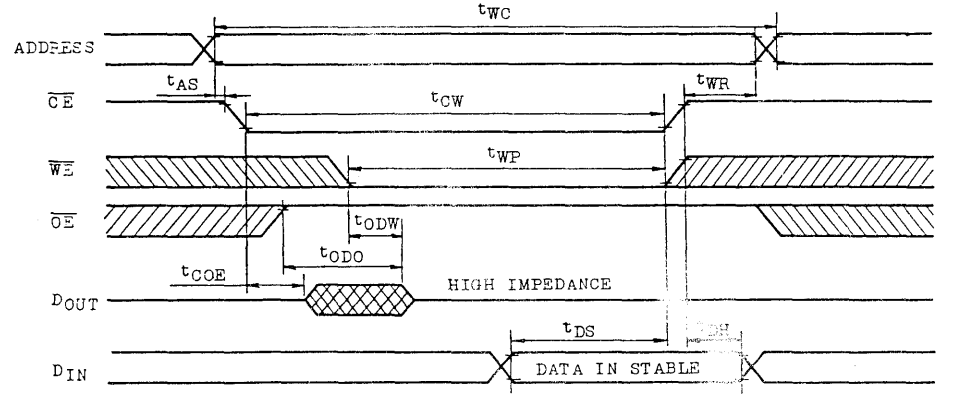
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

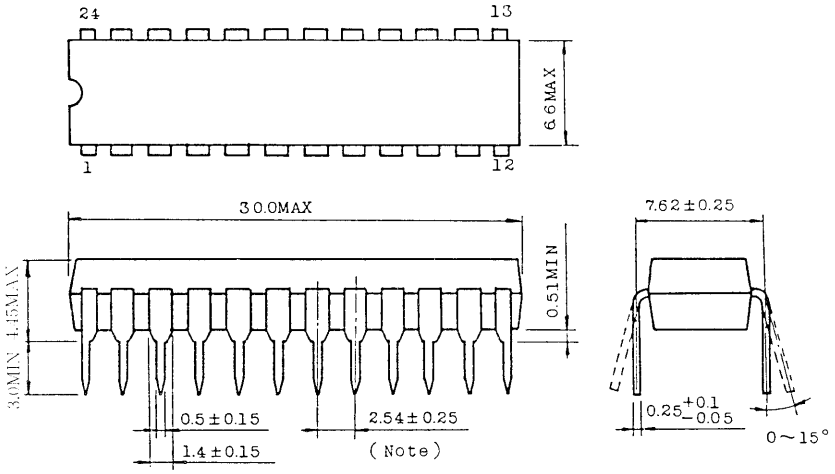


Note: 1. $\overline{WE}$ is High for Read cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

• Plastic DIP

Unit in mm

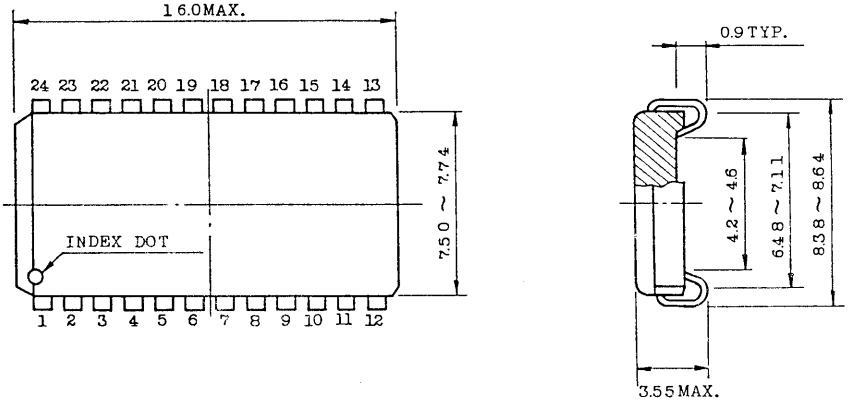


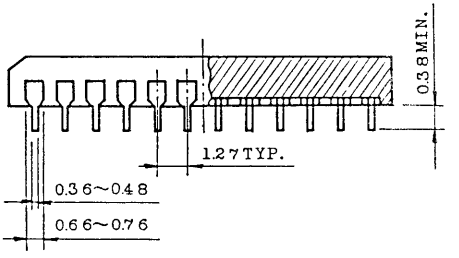
Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of the true longitudinal position with respect to No.1 and No.24 leads.

OUTLINE DRAWINGS

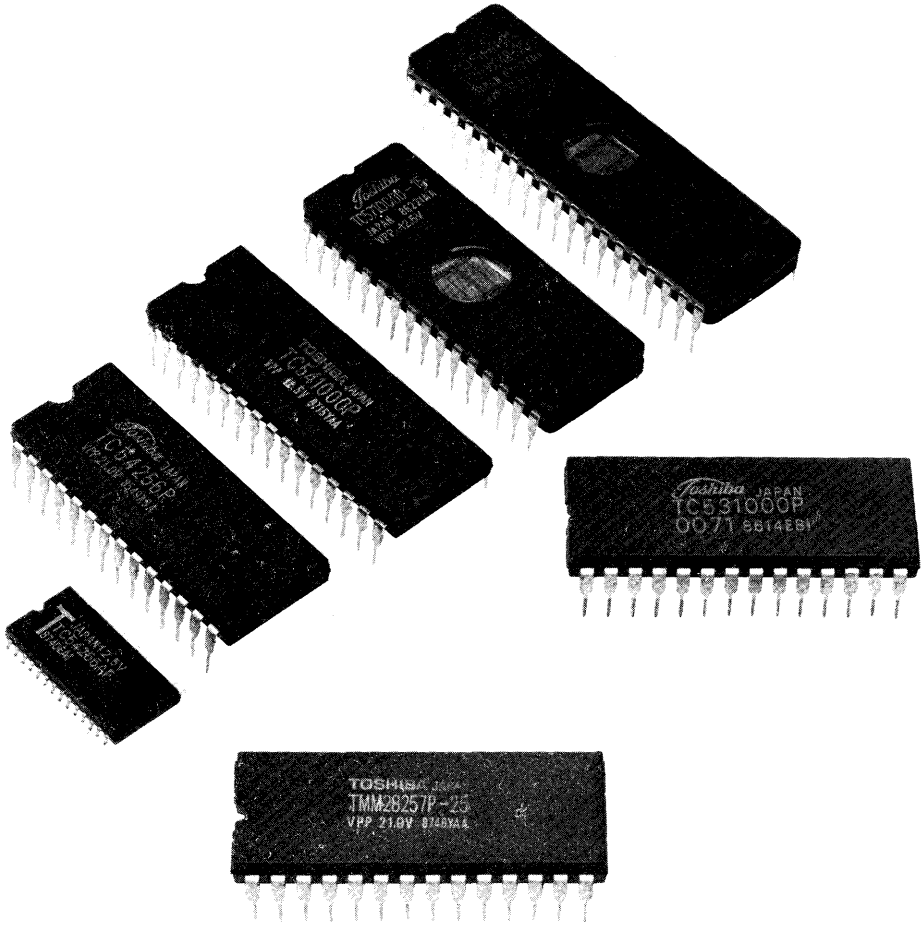
• Plastic SOJ

Unit in mm





Note: Each lead pitch is 1.27mm.
All leads are located within 0.12mm of the true longitudinal position with respect to No.1 and No.24 leads.



Non-Volatile Memory

Standard EPROM

HIGH SPEED PROGRAMMING MODE

FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI/BD/BDI	TMM24256AP/AF/BP/BF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI/AD/ADI	TMM24512P/F/AP/AF	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

1. For the Manufacturer Code:
   Set A9=12V±0.5V, Aϕ=ViL, Other Addresses=ViL
   Note: The manufacturer code is consistent with the E.I.A. standard.
2. For the Device Code:
   Set A9=12V±0.5V, Aϕ=ViH, Other Addresses=ViL.
   Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI/BD/BDI	TMM24256AP/AF/BP/BF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI/AD/ADI	TMM24512P/F/AP/AF	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

Figure 1

HIGH SPEED PROGRAM I FLOW CHART

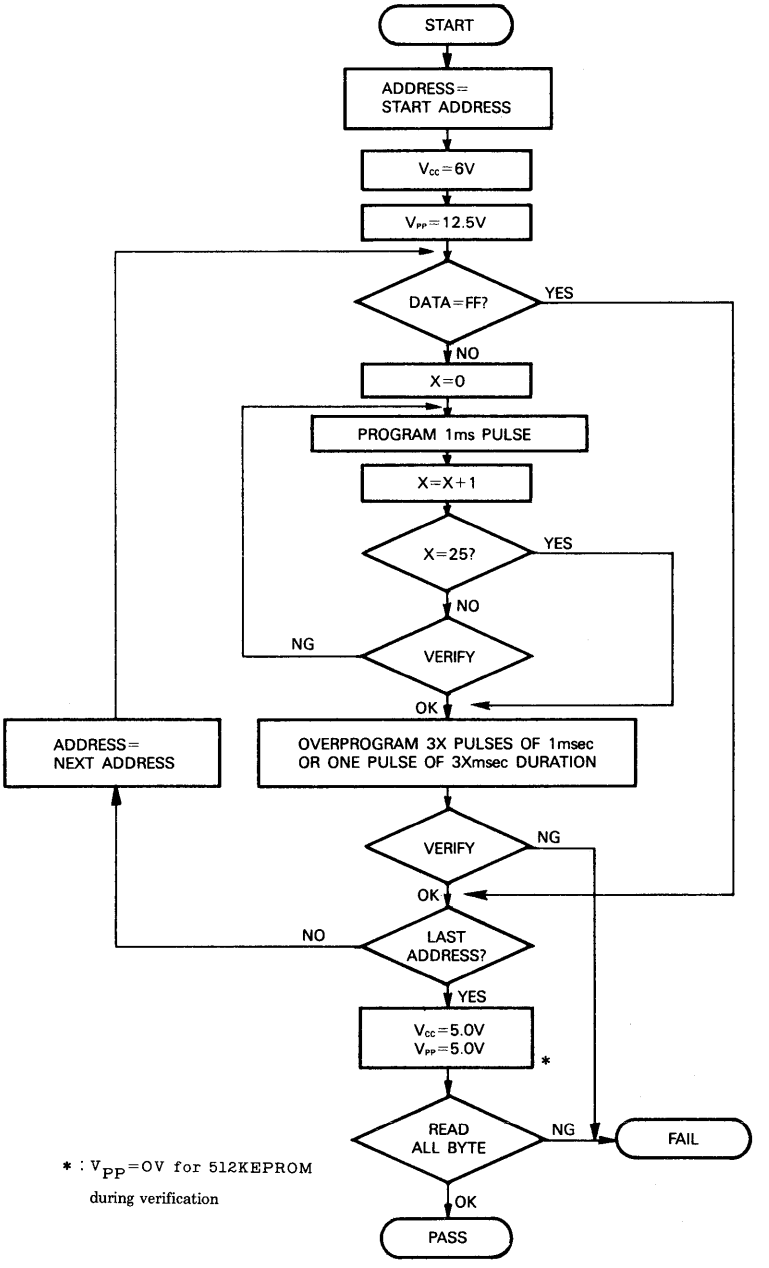
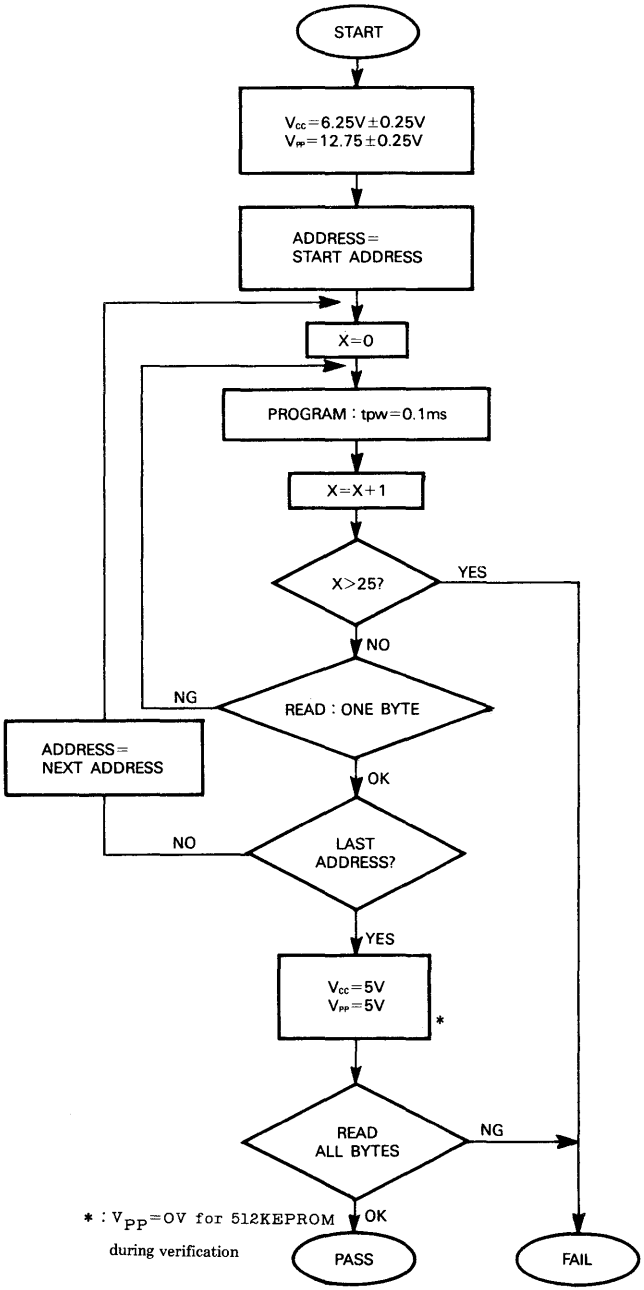


Figure 2

HIGH SPEED PROGRAM II FLOW CHART



8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764AD-15, TMM2764AD-150
TMM2764AD-20, TMM2764AD-200

DESCRIPTION

The TMM2764AD is a 8192 word ×8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150ns/200ns, and the TMM2764AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.
For program operation, the programming is achieved by using the high speed programming mode.

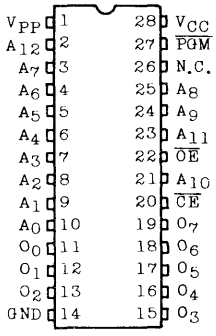
The TMM2764AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

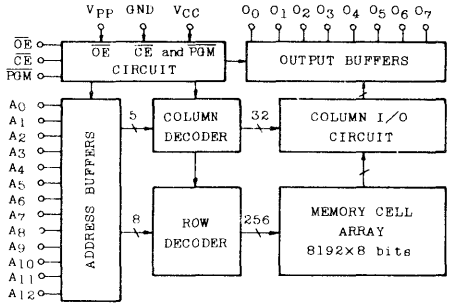
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−65~125	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764AD-15/20	TMM2764AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764AD-15/150		TMM2764AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

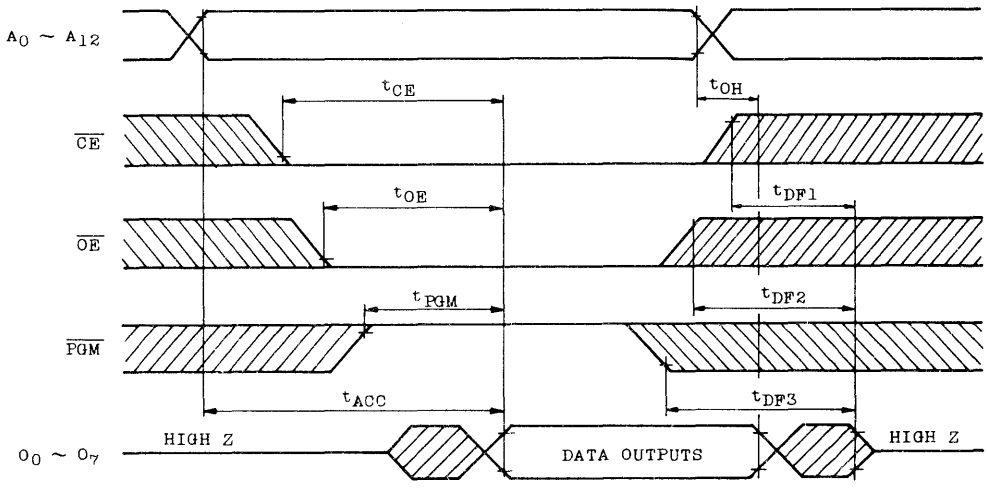
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25C°, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=OV.	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=OV	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

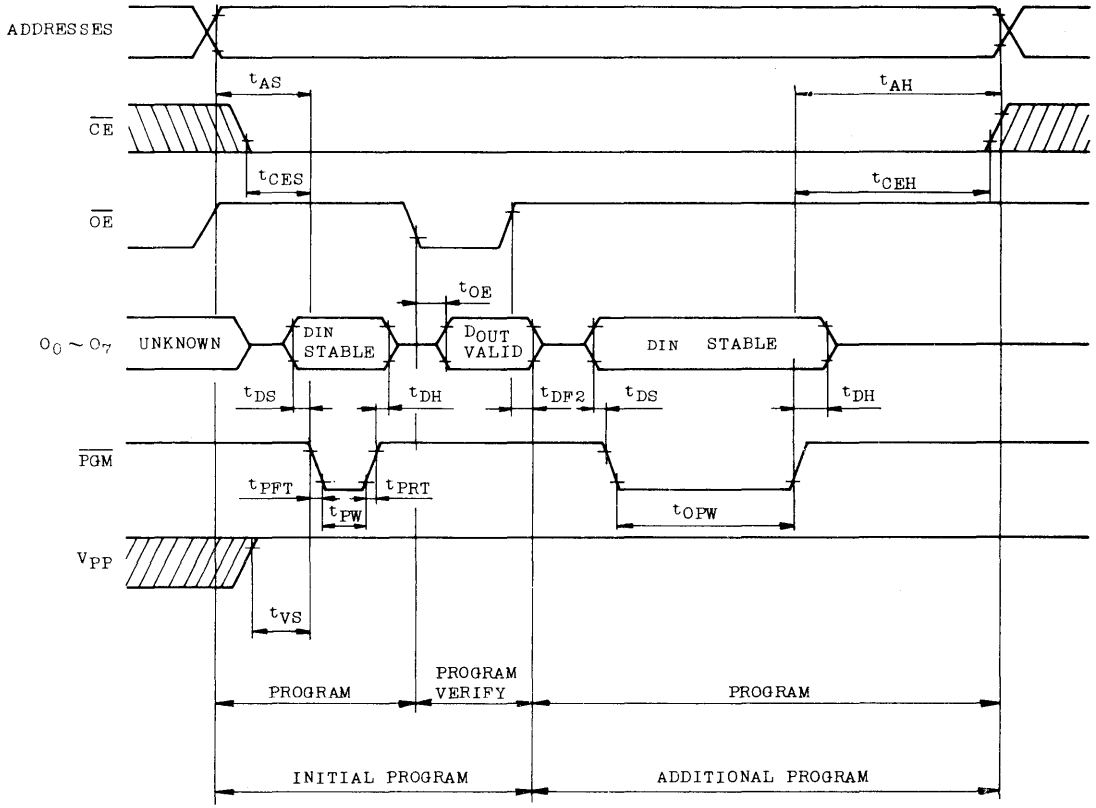
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45 to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{opw} depeds on the program pulse width which is required in the initial Program.

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM2764AD's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM2764AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM2764AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL

		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764AD can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764AD has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764AD is placed in the standby mode which reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764AD are in the "1" state which is erased state.

Therefore the program operation is to introduce "Os" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL.

The TMM2764AD can be programmed any location at anytime——either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764AD from being programmed.

Programming of two or more TMM2764AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage(+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$ =V_{IH}.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

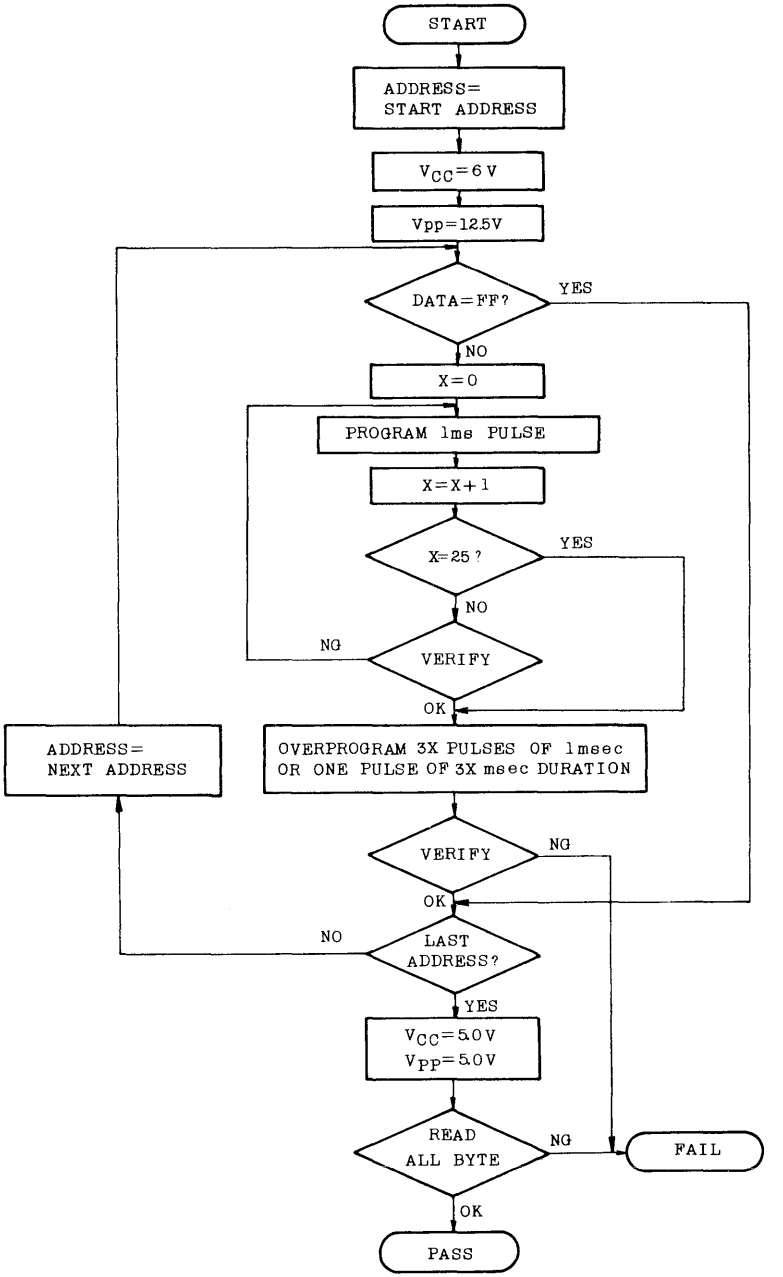
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP} =5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2764AD which identifies its manufacture and device type.

The programming equipent may read out manufacurer code and device code from TMM2764AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

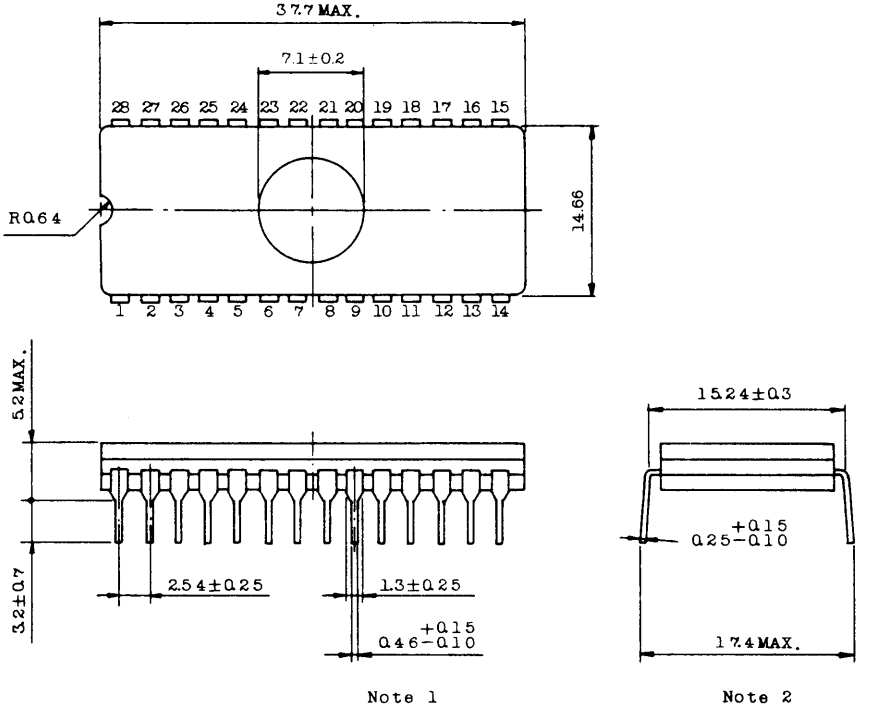
The following table shows electric signature of TMM2764AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes : A9 = 12V ± 0.5V
A1 ~ A8, A10 ~ A12, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

8,192 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM2764ADI-15
TMM2764ADI-20

DESCRIPTION

The TMM2764ADI is a 8192 word × 8bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM2764AD's access time is 150/200ns and the TMM2764ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

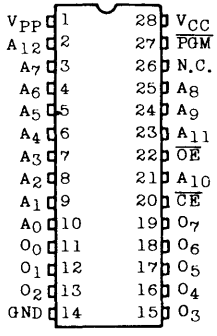
The TMM2764ADI is fabricated with the Nchannel silicon double layer gate MOS technology.

FEATURES

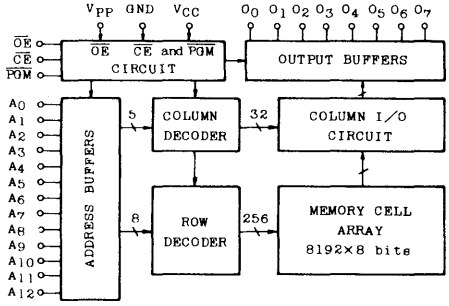
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i2764A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N. C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM2764ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.2~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	+10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM2764ADI-15		TMM2764ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

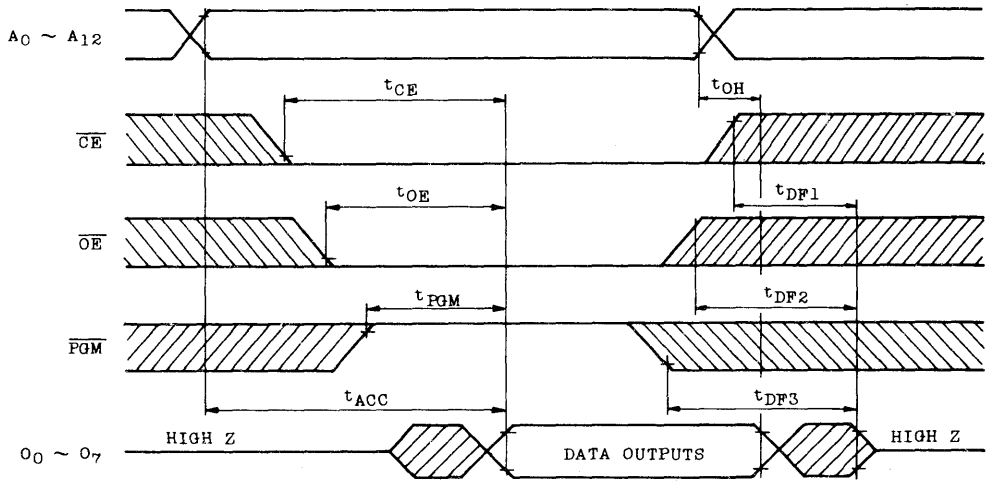
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25C°, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$.	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

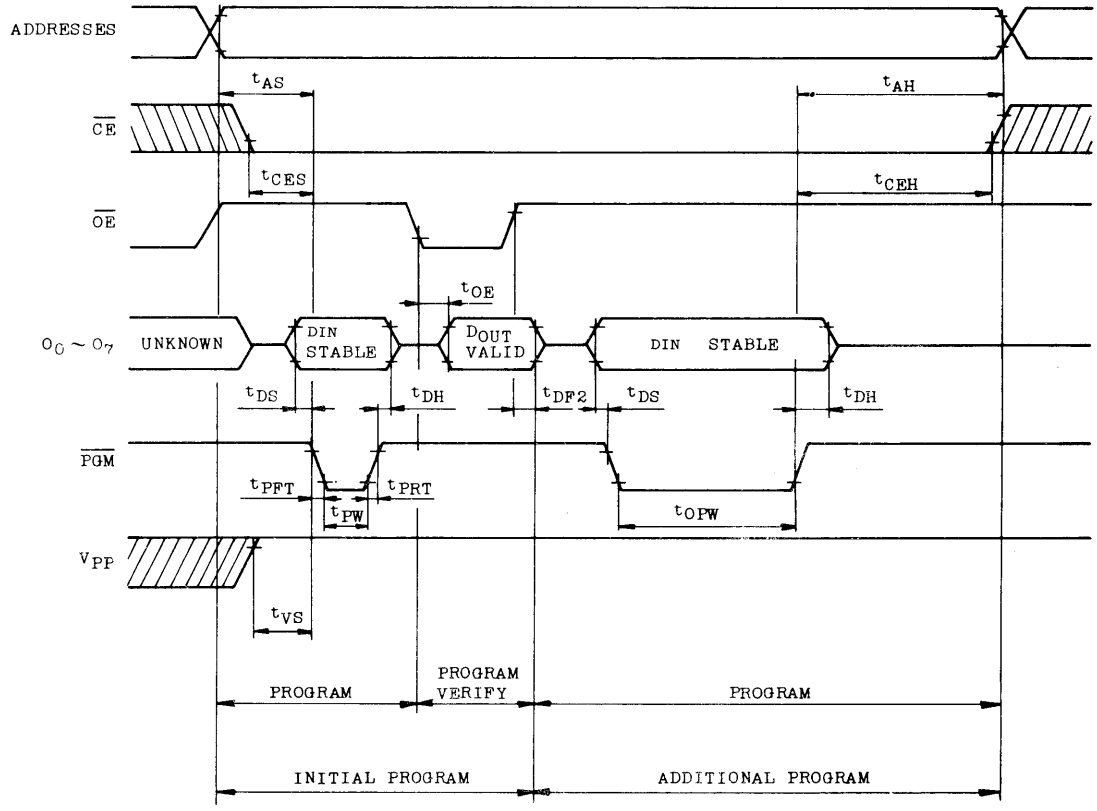
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	—	78.75	ms
t_{PRT}	Program Pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. Test Conditions

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 1V and 2V ; Output 0.8V and 2.0V

Note : 1. t_{opw} depeds on the program pulse width which is required in the initial Program

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V

ERASURE CHARACTERISTICS

The TMM2764ADI's erasure is achieved by applying shortwave ultraviolet light which has a wave length of 2537Å (Angstroms) to the chip through the transparent window.

The integrated dose (Ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM2764ADI's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM 2764ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NOMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=−40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IL}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM2764ADI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM2764ADI can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2764ADI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM2764ADI is placed in the standby mode which reduce 70% of the operating current and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM2764ADI are in the "1" state which is erased state. The programming operation is introduces "Os" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL.

The TMM2764ADI can be programmed any location at anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2764ADI from being programmed.

Programming of two or more TMM2764ADI's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

The device is set up in the high speed programming mode when the programming voltage(+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$ =V_{IH}.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

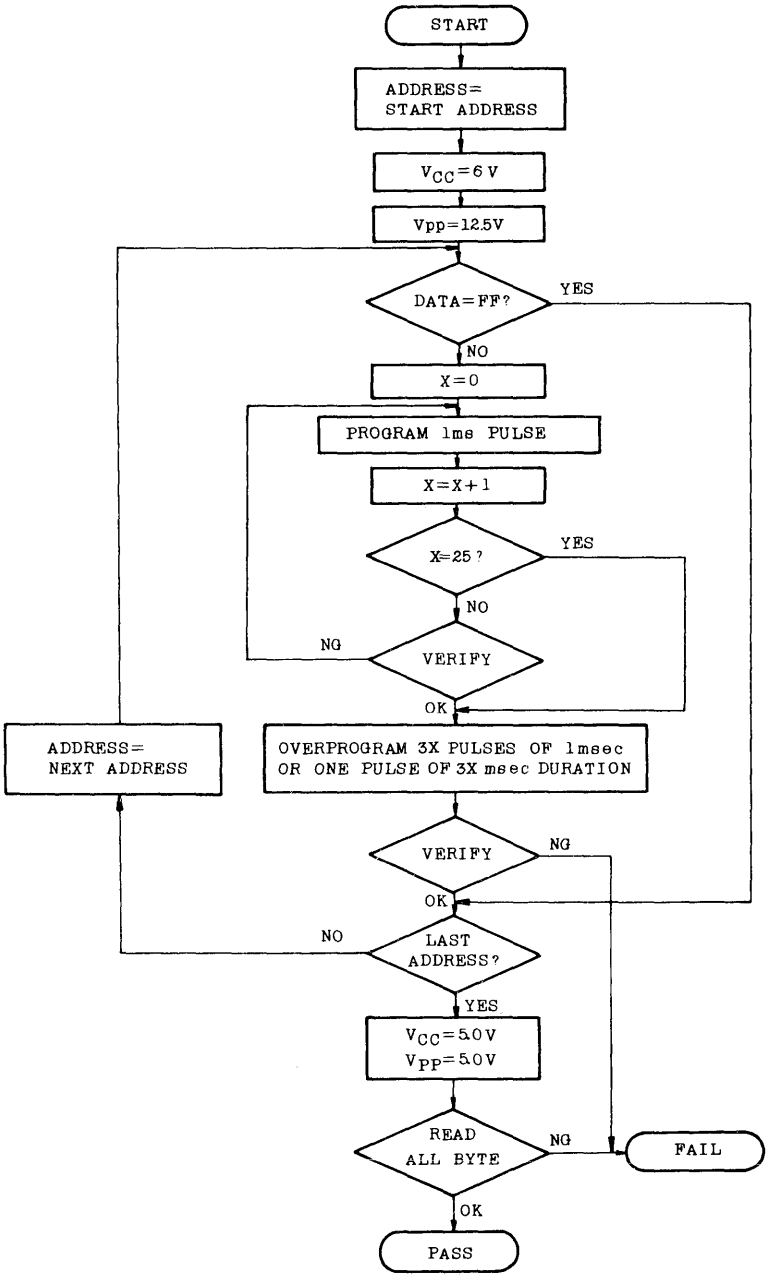
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max.25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP} =5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM2764ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764ADI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

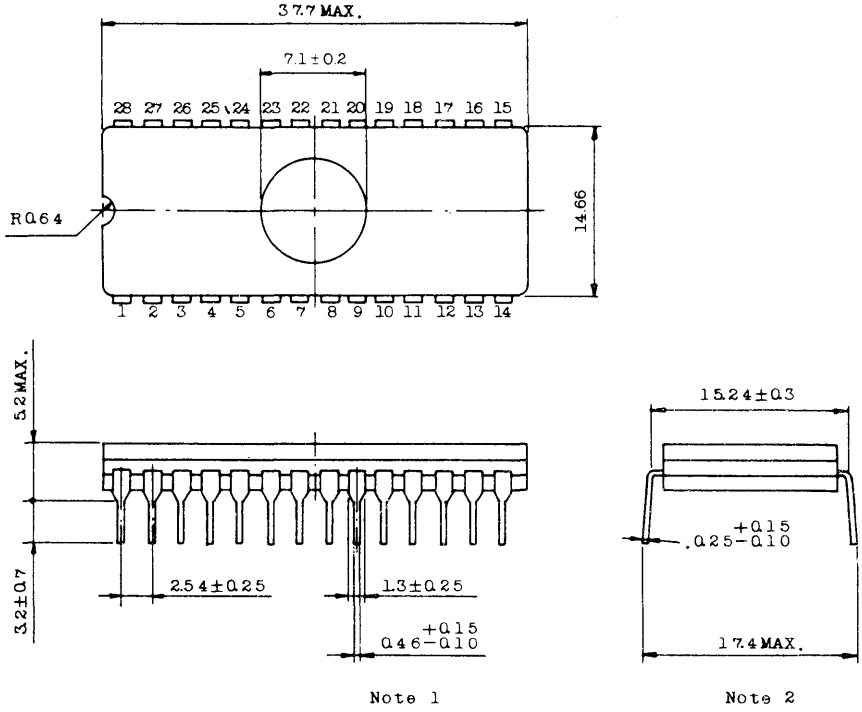
The following table shows electric signature of the TMM2764ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes : A9 = 12V±0.5V
A1~A8, A10~A12, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note: 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128AD-15, TMM27128AD-150
TMM27128AD 20, TMM27128AD-200

DESCRIPTION

The TMM27128AD is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128AD's access time is 150ns/200ns, and the TMM27128AD operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the program is achieved by using the high speed programming mode.

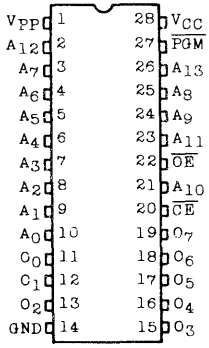
The TMM27128AD is fabricated with the N-channel silicon double layer gate MOS technolgy.

FEATURES

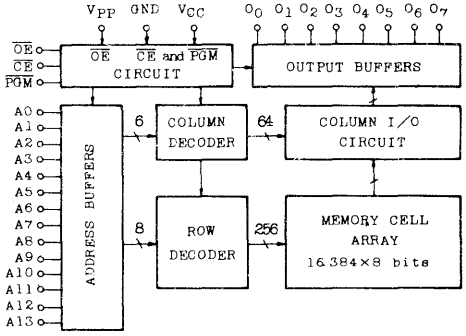
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Fully static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128AD-15/20	TMM27128AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128AD-15/150		TMM27128AD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

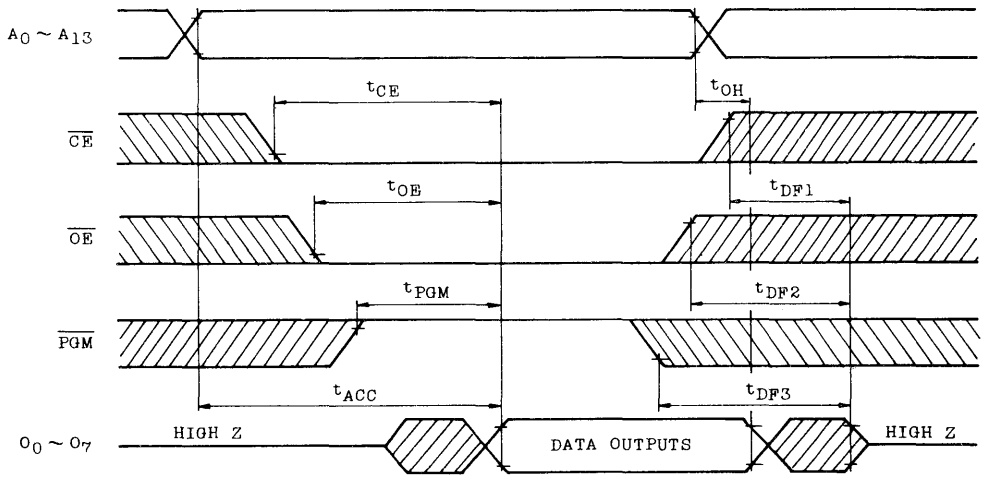
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

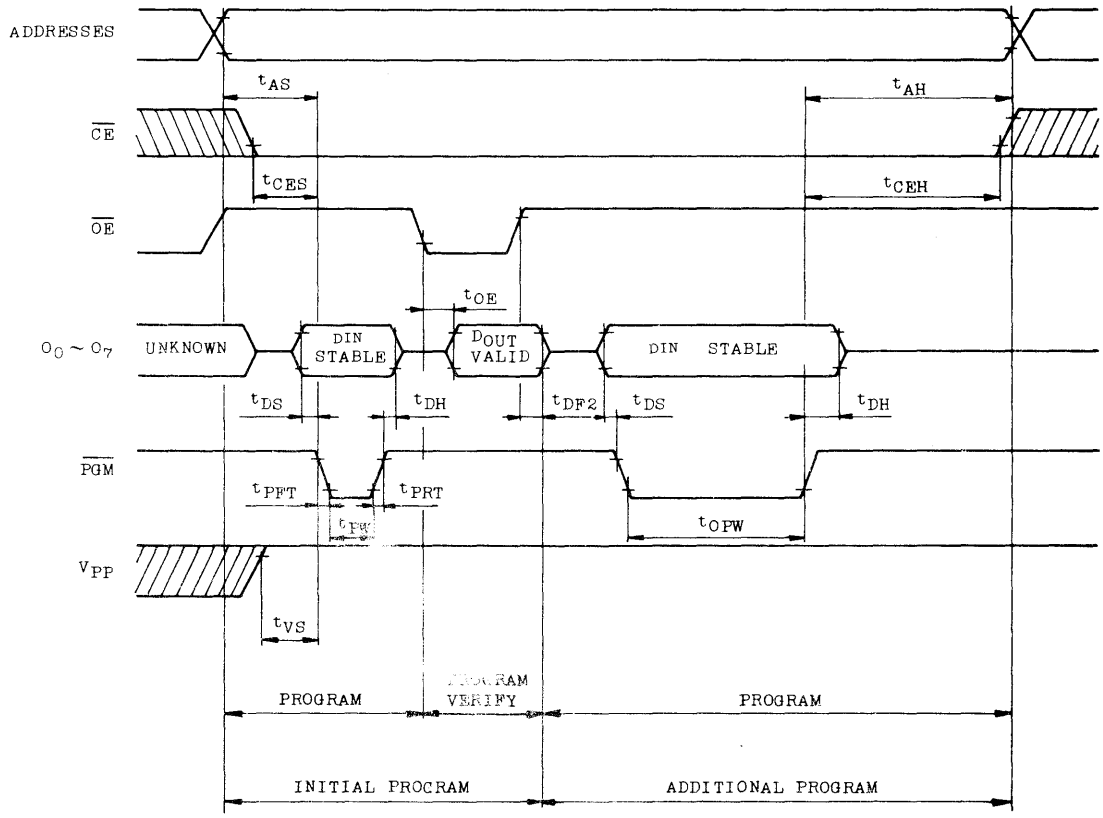
(Ta = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output is High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27128AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27128AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27128AD's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES (NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128AD has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.

Thus, two or more TMM27128AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128AD has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128AD is placed in the standby mode which reduces 70% of operating current. The outputs are in a high impedence state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128AD are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128AD can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128AD from being programmed.

Programming of two or more TMM27128AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

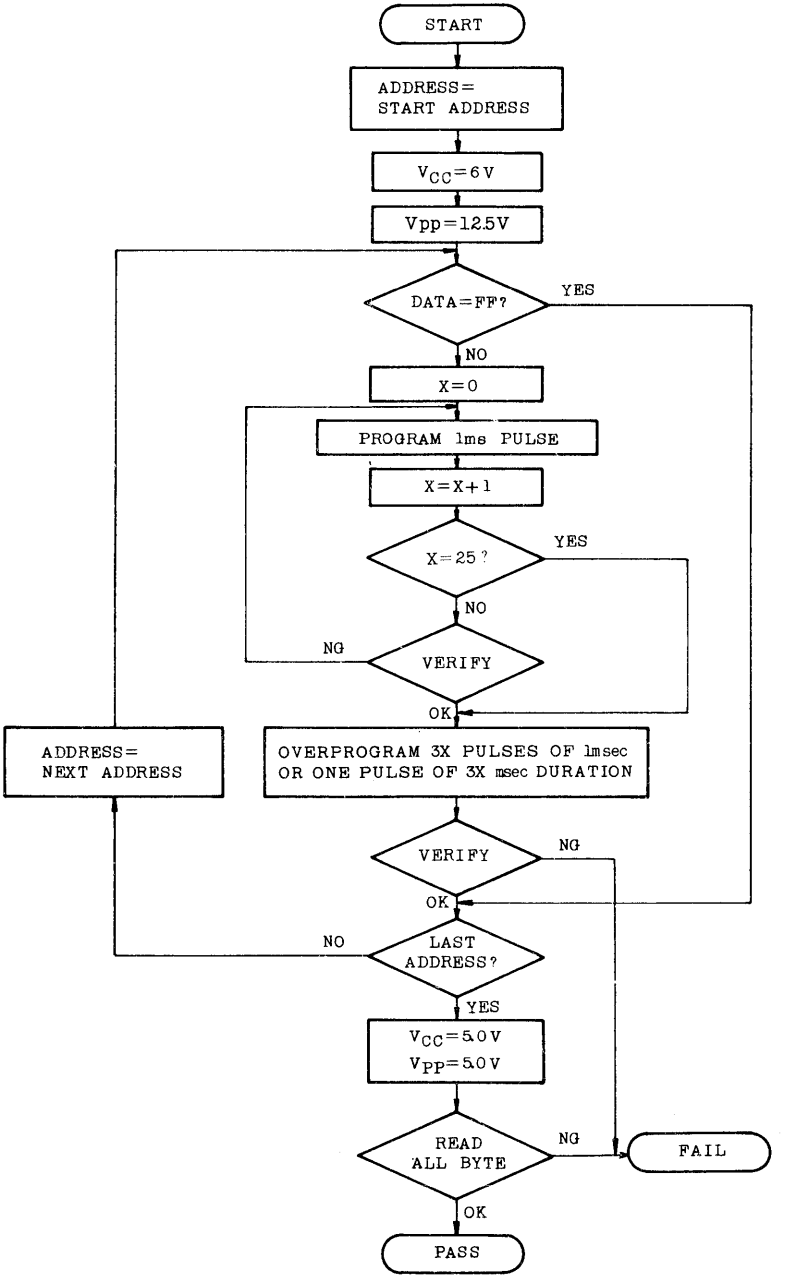
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM2764AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

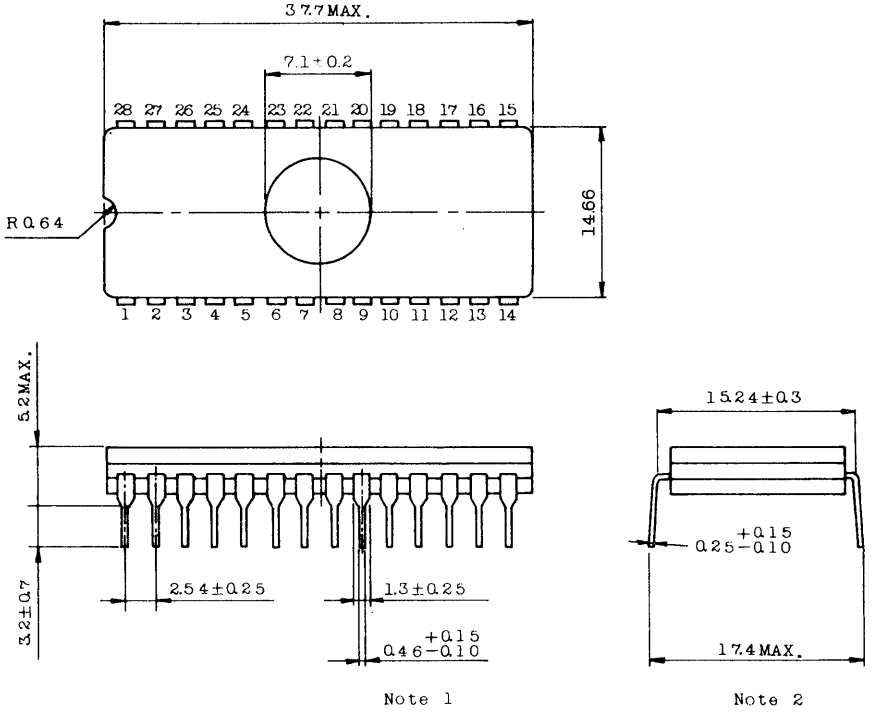
The following table shows electric signature of the TMM27128AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V±0.5V
A1 ~ A8, A10 ~ A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

Note : Toshiba does not assume any responsibility for use of any circuitry described : no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

16,384 WORD × 8 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
N-CHANNEL SILICON STACKED GATE MOS

TMM27128ADI-15
TMM27128ADI-20

DESCRIPTION

The TMM27128ADI is a 16,384 word × 8 bit ultraviolet light erasable and electrically programmable read only memory. For read operation, the TMM 27128ADI's access time is 150ns/200ns, and the TMM27128ADI operates from a single 5-volt power supply and has a low power standby mode which reduces the power dissipation without increasing access time.

The standby mode is achieved by applying a TTL high level signal to the $\overline{CE}$ input.

For program operation, the program is achieved by using the high speed programming mode.

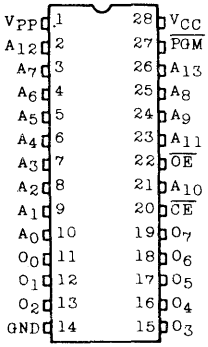
The TMM27128ADI is fabricated with the N-channel silicon double layer gate MOS technolgy.

FEATURES

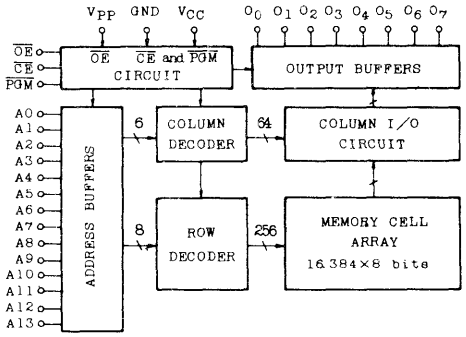
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Pin compatible with i27128A

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{13}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27128ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27128ADI-15		TMM27128ADI-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

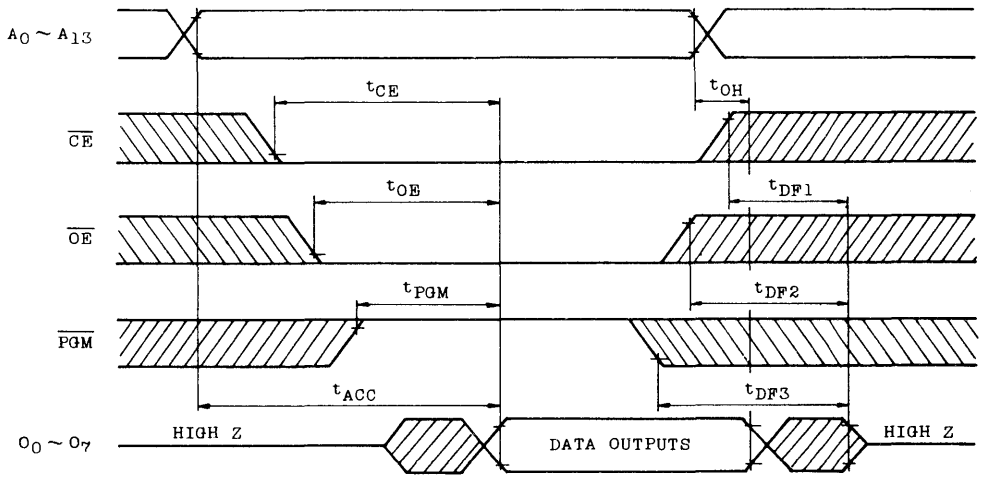
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	—	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	8	12	pF

* This paramater is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

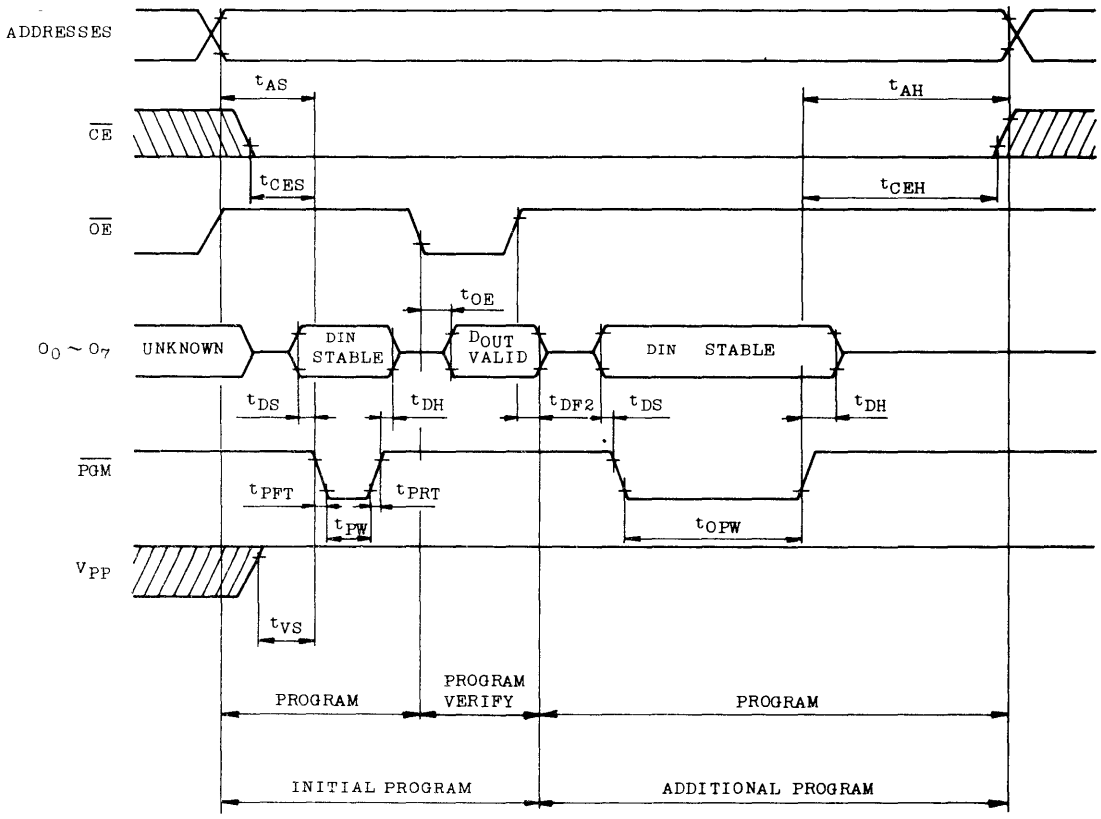
($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3	78.75	ms
t_{PRT}	Program pulse Rise Time	—	5	—	—	ns
t_{PFT}	Program Pulse Fall Time	—	5	—	—	ns
t_{OE}	$\overline{OE}$ to Output Valid Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output is High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.

   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27128ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [W.sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27128ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27128ADI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAME (MODE)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
READ OPERATION (Ta=−40~85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27128ADI has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in high impedance state.

So two or more TMM27128ADI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27128ADI has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a TTL high level to the $\overline{CE}$ input, the TMM27128ADI is placed in the standby mode which reduces 70% of operating current. The outputs are then in a high impedence state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27128ADI are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The levels required for all inputs are TTL.

The TMM27128ADI can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM27128ADI from being programmed.

Programming of two or more TMM27128ADI's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V and $\overline{PGM}$ = V_{IH}.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

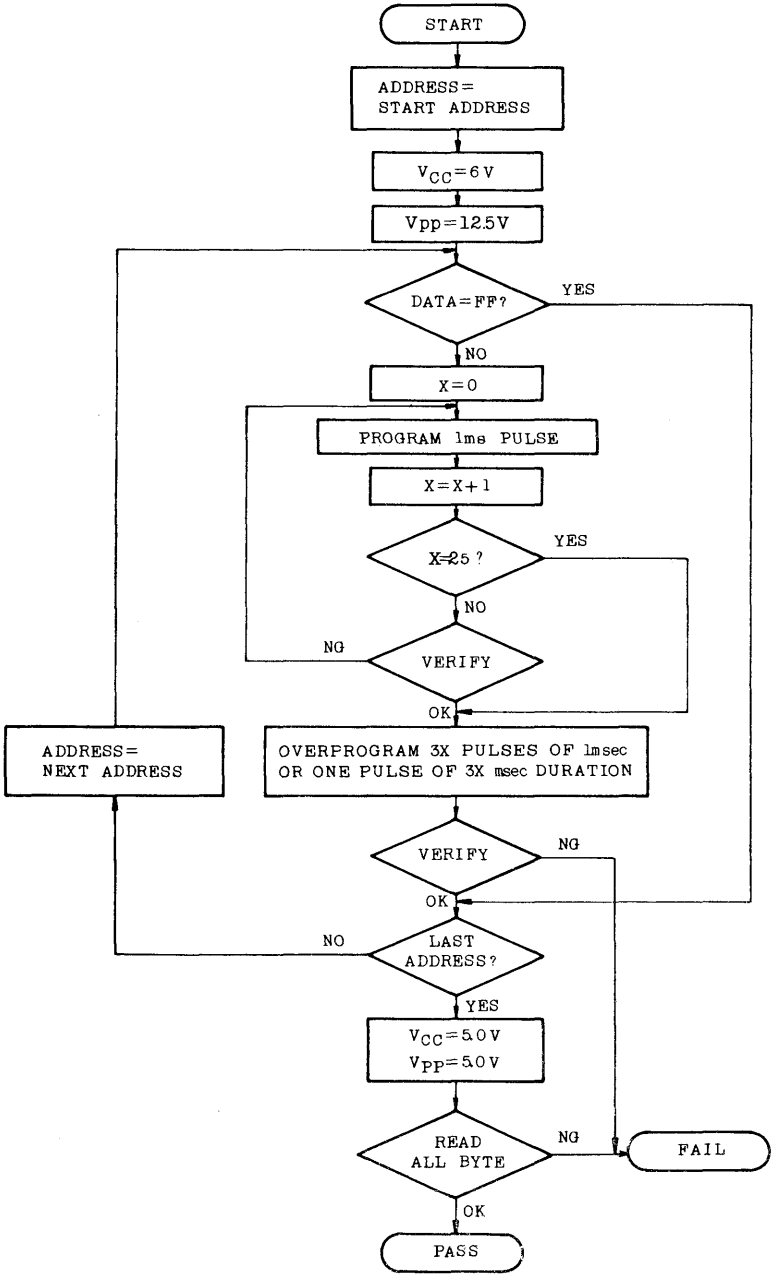
If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC} = V_{PP}$ = 5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27128ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27128ADI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output is this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

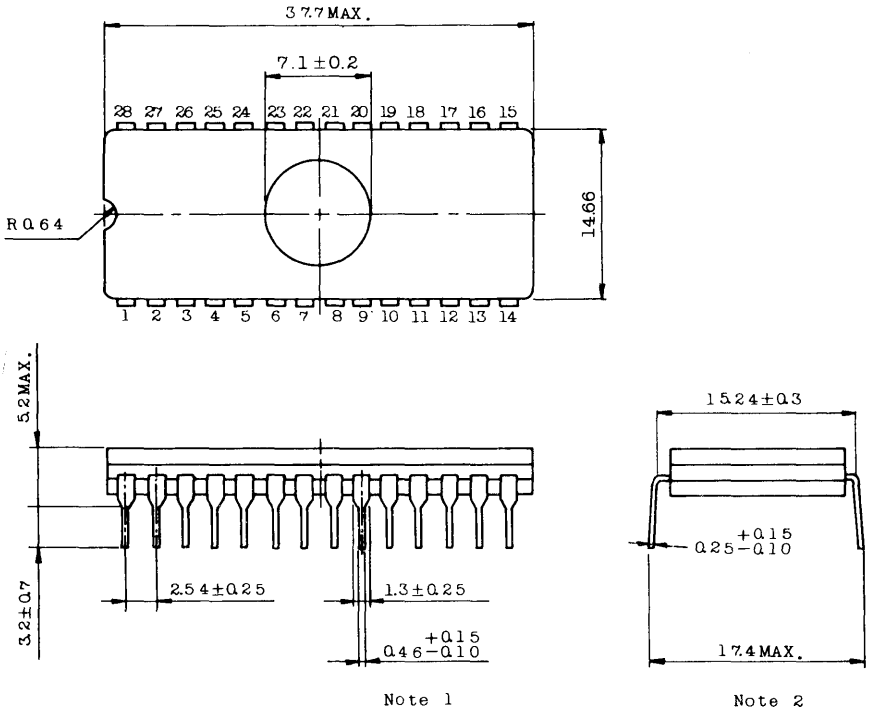
The following table shows electric signature of TMM27128ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

Notes : A9 = 12V±0.5V
A1 ~ A8, A10 ~ A13, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1 Note 2

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256AD-15, TMM27256AD-150
TMM27256AD-20, TMM27256AD-200

DESCRIPTION

The TMM27256AD is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256AD's access time is 150ns/200ns, and the TMM27256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

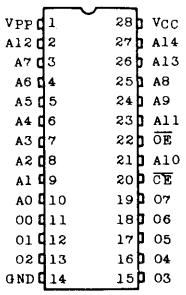
The TMM27256AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

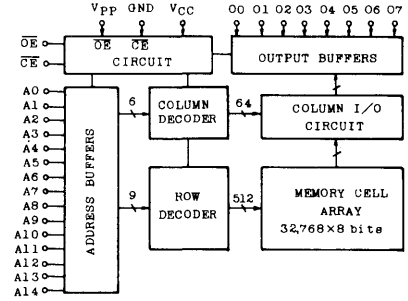
	−15	−20	−150	−200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i 27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	*	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256AD-15/20	TMM27256AD-150/200
Ta	Operating Temperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0~V_{CC}±0.6V	2.0~V_{CC}+0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}		—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−15/20	—	—	30	mA
			−150/200	—	—	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−15/20	—	—	100	mA
			−150/200	—	—	120	
V_{IH}	Input High Voltage	—		2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA		2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6		—	—	±10	μA

A.C. CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256AD-15/150		TMM27256AD-20/200		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ =$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	ns

A.C. Test Conditions

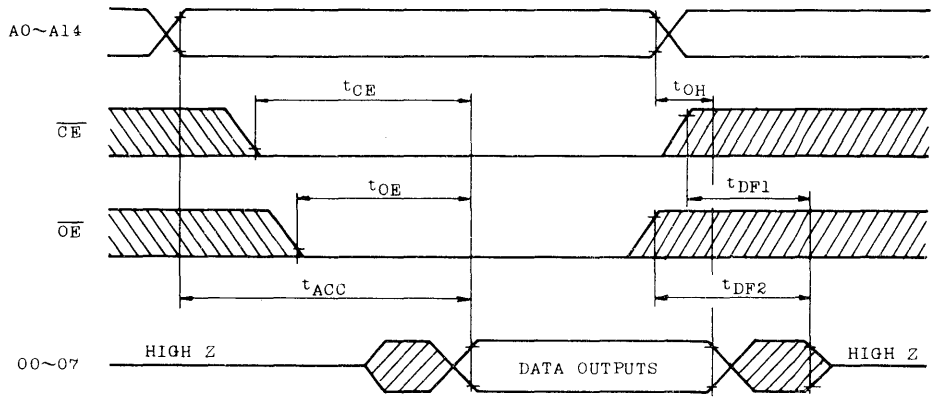
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $OE=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

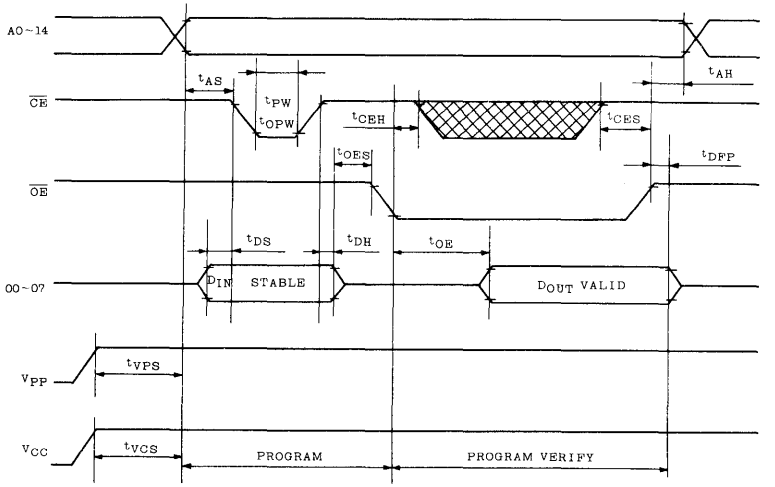
A C Test Conditions

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V

ERASURE CHARACTERISTICS

The TMM27256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) through the chips transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps whose ultraviolet light intensity is 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27256AD's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$.the outputs will be in a high impedance state.

So two or more TMM27256AD's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256AD has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256AD is placed in standby mode which reduces the operating current by 70%. The outputs are then in a high impedence state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256AD are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27256AD is in the programming mode when the V input is at 12.5V and $\overline{CE}$ is at TTL-Low with $\overline{OE}=V_{IH}$.

The TMM27256AD can be programmed at any location, anytime — either individually, sequentially or at randomly.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ of V_{IL} and $\overline{CE}$ V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM27256AD from being programmed.

Programming of two or more TMM27256ADs in parallel with different data is easily accomplished. That is , all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC} =6V.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

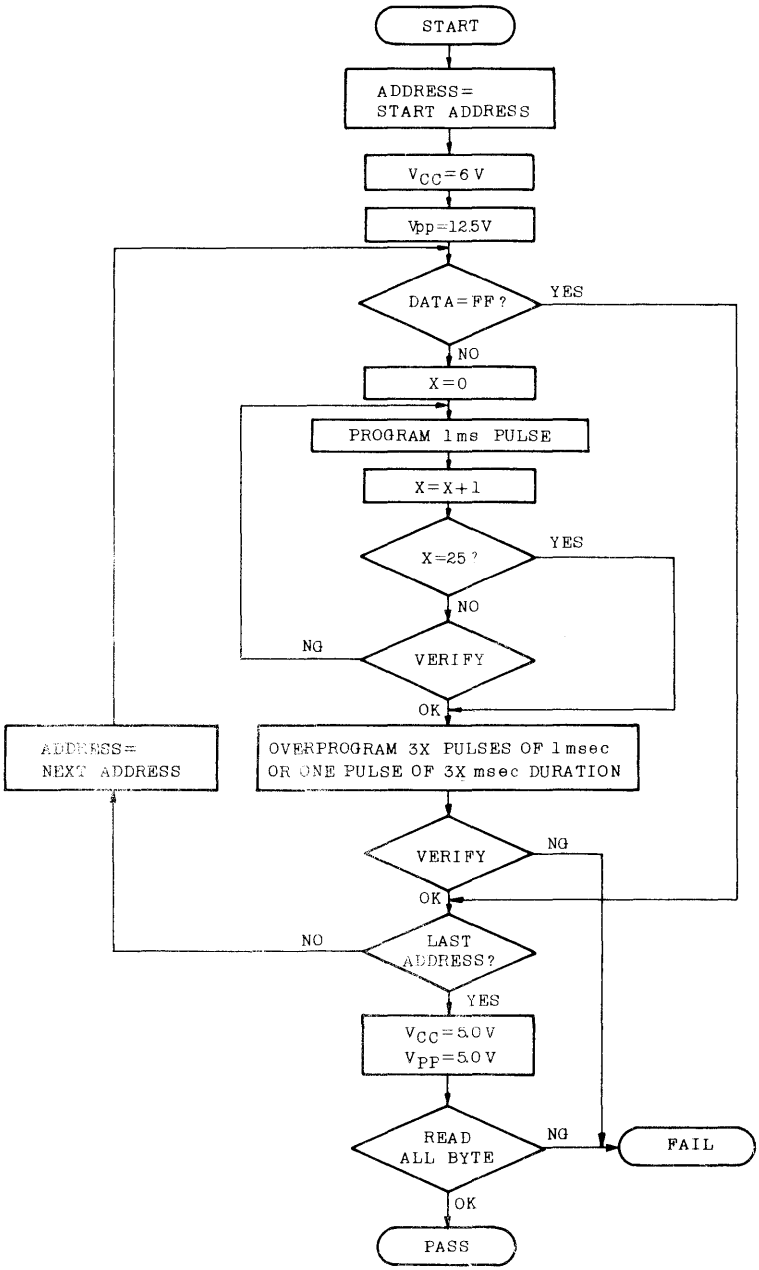
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}$ =5V.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256AD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

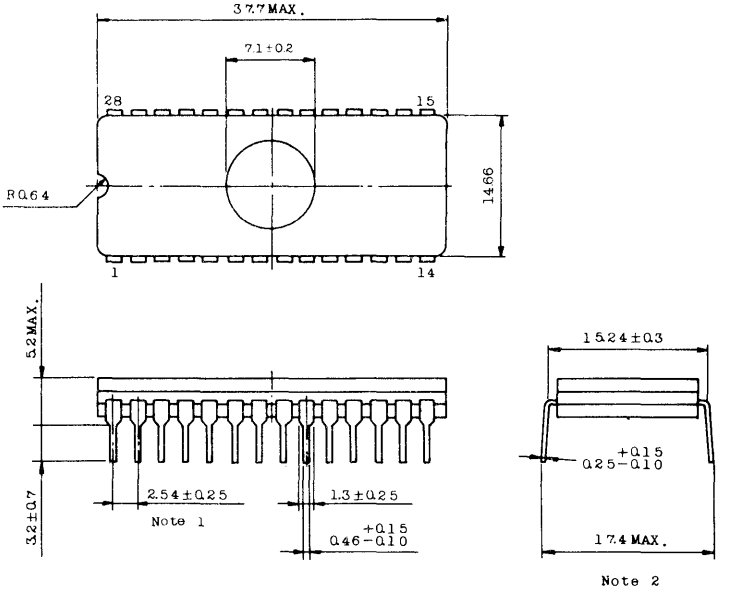
The following table shows electric signature of the TMM27256AD.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes : $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM27256ADI-15
TMM27256ADI-20

DESCRIPTION

The TMM27256ADI is a 32,768 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, The TMM27256ADI's access time is 150ns/200ns, and the TMM27256ADI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

For program operation, the programming is achieved by using the high speed programming mode.

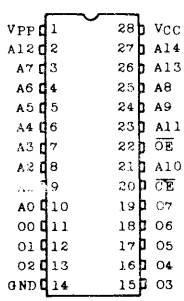
The TMM27256ADI is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

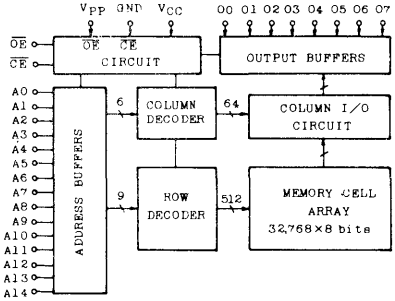
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	100mA	
I_{CC1}	30mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A_0~A_{14}	Address Inputs
O_0~O_7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	*			High Impedance	
Program Verify	*	L			Data Out	

Note * : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85°C	°C

READ OPERATION

D. C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256ADI-15/20
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%
V_{PP}	V_{PP} Power Supply Voltage	2.2~V_{CC}±0.6V

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	120	mA
V_{IH}	Input High Voltage	—	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6	—	—	±10	μA

A.C. CHARACTERISTICS

(Ta=−40~85°C, V_{CC}=5V±5%, V_{PP}=2.0V~V_{CC}+0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TMM27256AD-15		TMM27256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$ =$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	—	150	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	—	70	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	—	0	—	ns

A C Test Conditions

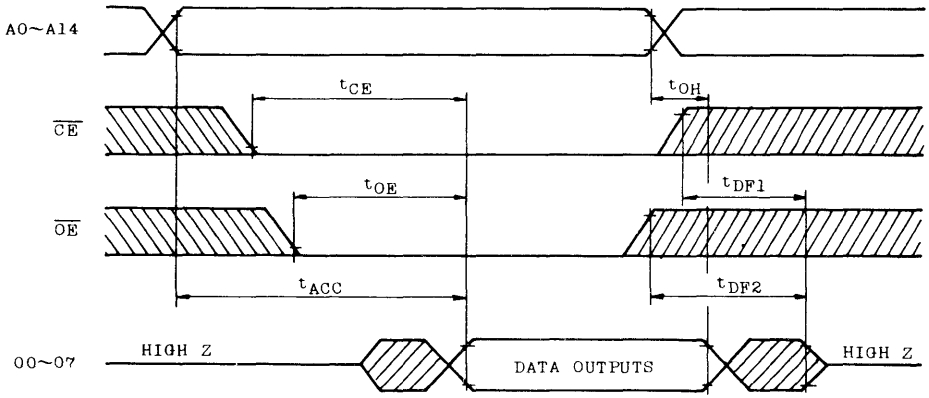
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $OE=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFF}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

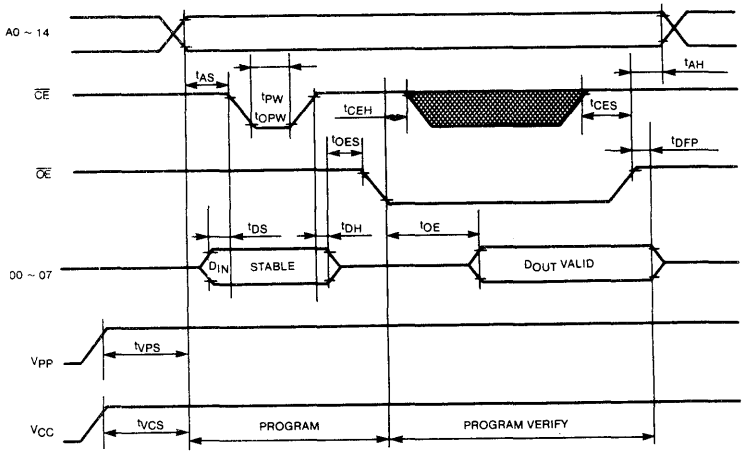
A C Test Conditions

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V

ERASURE CHARACTERISTICS

The TMM27256ADI's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) of the chip through the transparent window.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.

And using commercial lamps with an ultraviolet light intensity of 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (20×60) [sec] ≅ 15 [w·sec/cm²].)

The TMM27256ADI's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Both Sunlight and flourescent lamps include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27256ADI's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=−40~85°C)	Read	L	L	5 V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	*			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

READ MODE

The TMM27256ADI has two control functions.

The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after the address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) time is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{CE}$.

OUTPUT DESELECT MODE

With $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, outputs will be in high impedance state.

Therefore two or more TMM27256ADI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256ADI has a low power standby mode conntrolled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27256ADI is placed in the standby mode which reduces 70% of operating current by applying TTL-high level (V_{CC}). The outputs are in a high impedence state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256ADI are in the "1" state which is the erased state.

The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27256ADI is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM27256ADI can be programmed at any location, anytime — either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ of V_{IL} and $\overline{CE}$ V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM27256ADI from being programmed.

Programming of two or more TMM27256ADI's in parallel with different data is easily accomplished.

That is , all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

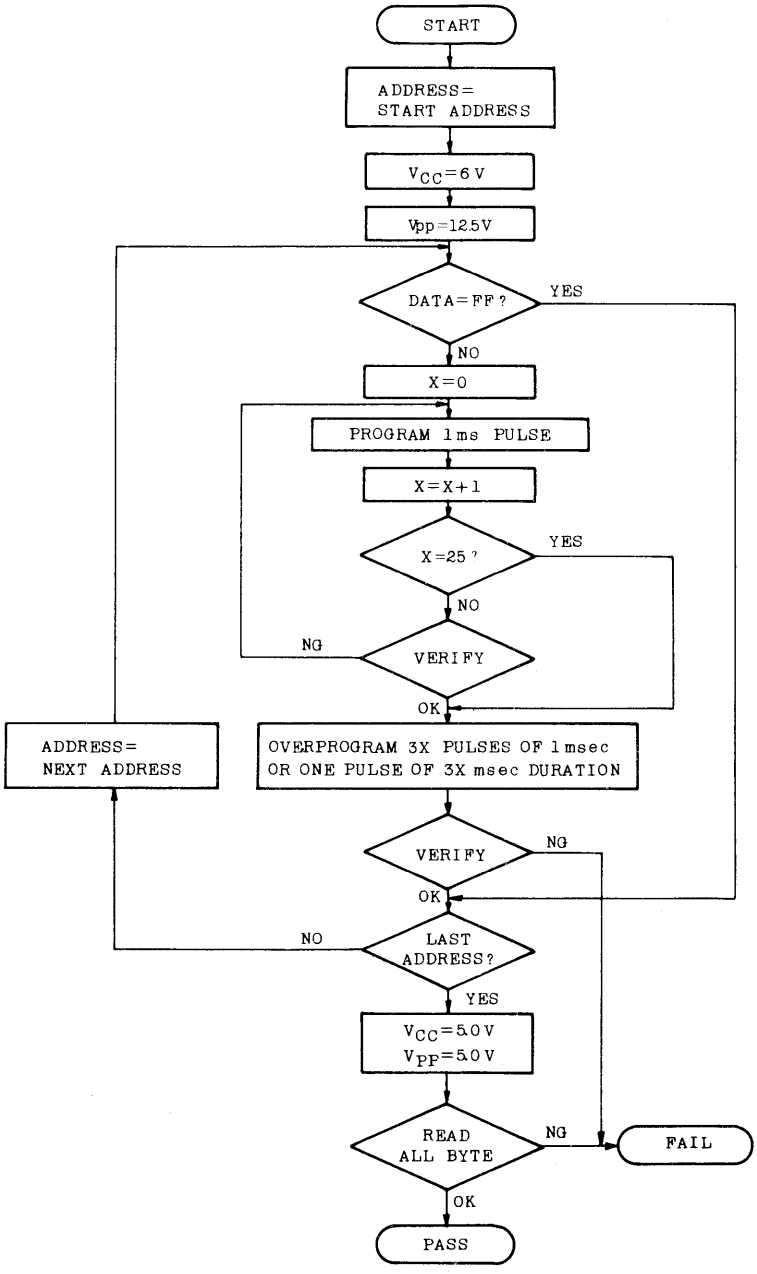
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

The High Speed Program II Algorithm (shown in figure 2, page G-5) may also be used to reduce the programming time further.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27256ADI which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from the TMM27256ADI by using this mode before program operation and automatically set program voltage (Vpp) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two code possess an odd parity with the parity bit of MSB (07).

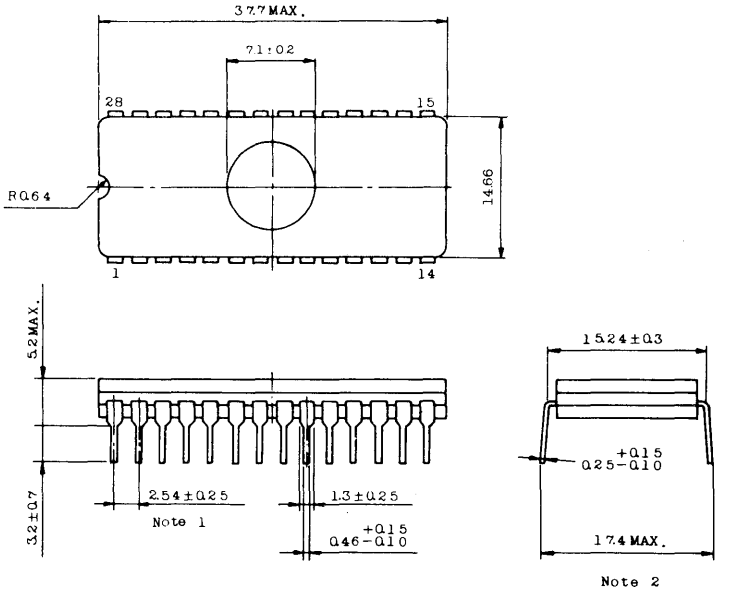
The following table shows electric signature of the TMM27256ADI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes : $A_9 = 12V \pm 0.5V$
A_1-A_8, A_{10}-A_{14}, $\overline{CE}$, $\overline{OE} = V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

PRELIMINARY

TMM27256BD-15, TMM27256BD-150
TMM27256BD-20, TMM27256BD-200

DESCRIPTION

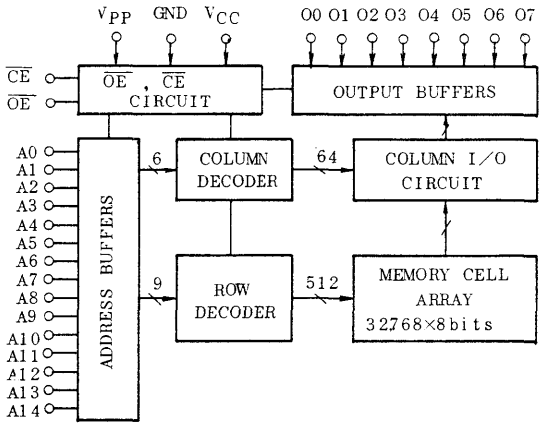
The TMM27256BD is a 32,768 words × 8 bits ultraviolet light erasable and electrically programmable read only memory.
For read operation, the TMM27256BD's access time is 150ns/200ns, and the TMM27256BD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.
For program operation, the programming is achieved by using the high speed programming mode. The TMM27256BD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

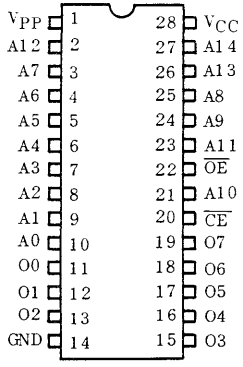
	-15	-20	-150	-200
V_{CC}	5V±5%		5V±10%	
t_{ACC}	150ns	200ns	150ns	200ns
I_{CC2}	100mA		120mA	
I_{CC1}	30mA		35mA	

- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

BLOCK DIAGRAM



PIN CONNECTION



PIN NAMES

A0∿A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11∿13, 15∿19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	1) 12.5V	1) 6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L	2) 12.75V	2) 6.25V	Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. AND A.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27256BD-15/20	TMM27256BD-150/200
Ta	Operating Temperature	0 ∿ 70°C	0 ∿ 70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%
V_{PP}	V_{PP} Power Supply Voltage	2.0 ∿ V_{CC}+0.6V	2.0 ∿ V_{CC}+0.6V

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}		-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-15/20	-	-	30	mA
			-150/200	-	-	35	
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-15/20	-	-	100	mA
			-150/200	-	-	120	
V_{IH}	Input High Voltage	-		2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	Vpp Current	Vpp=0 ∿ V_{CC}+0.6		-	-	±10	μA

A.C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27256BD-15/150		TMM27256BD-20/200		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	ns
t_{OH}	Output Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

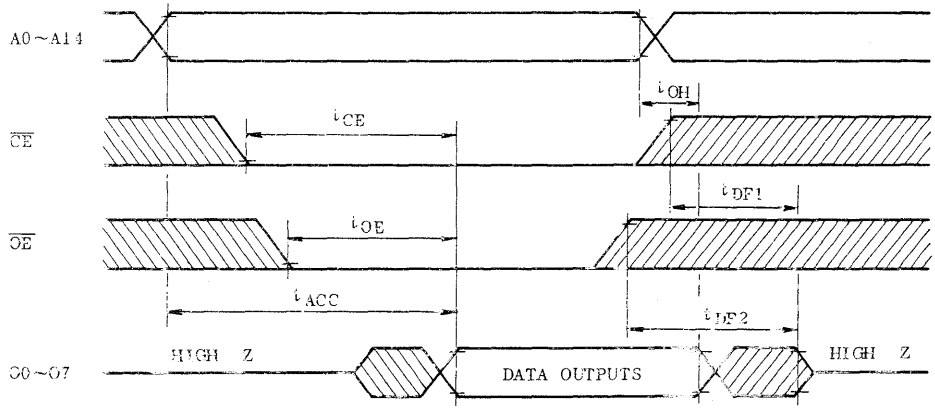
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE I)

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0∿V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V∿2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

PROGRAM OPERATION (HIGH SPEED PROGRAMMING MODE II)

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	6.0	6.25	6.5	V
V_{PP}	Vpp Power Supply Voltage	12.5	12.75	13.0	V

D.C. AND OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, Vpp=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6.25V±0.25V, Vpp=12.75V±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	Vpp Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

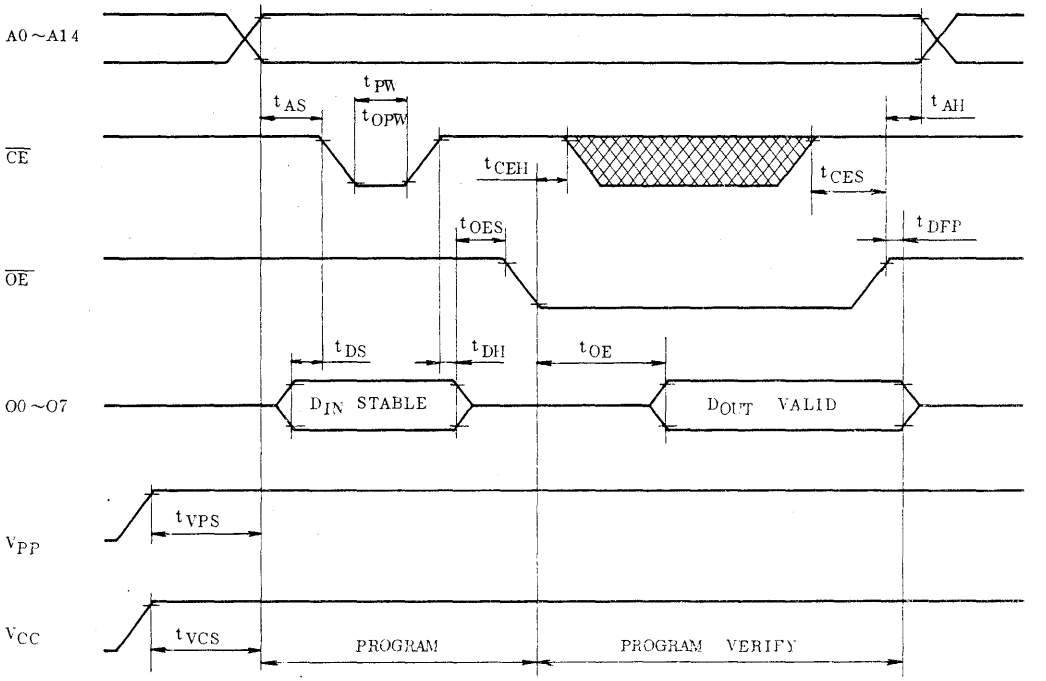
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

TIMING WAVEFORMS (PROGRAM)

HIGH SPEED PROGRAMMING MODE I (V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

HIGH SPEED PROGRAMMING MODE II (V_{CC}=6.25V±0.25V, V_{PP}=12.75V±0.25V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V±0.5V or V_{PP}=12.75V±0.25V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27256BD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w•sec/cm^2].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm^2] × (20 × 60) [sec] ≃ 15 [w•sec/cm^2].)
The TMM27256BD's erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27256BD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=0 ∿ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V[1)]	6V[1)]	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L	12.75V[2)]	6.25V[2)]	Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

1); HIGH SPEED PROGRAMMING MODE I

2); HIGH SPEED PROGRAMMING MODE II

READ MODE

The TMM27256BD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM27256BD's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27256BD has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM27256BD is placed in the standby mode which reduce 70% of the operating current by applying TTL-high level and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27256BD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TMM27256BD is in the programming mode when the V_{PP} input is at 12.5V or 12.75V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TMM27256BD can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (12.5V or 12.75V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27256BD from being programmed. Programming of two or more TMM27256BD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE I

This high speed programming mode I is performed at V_{CC}=6.0V and V_{PP}=12.5V. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

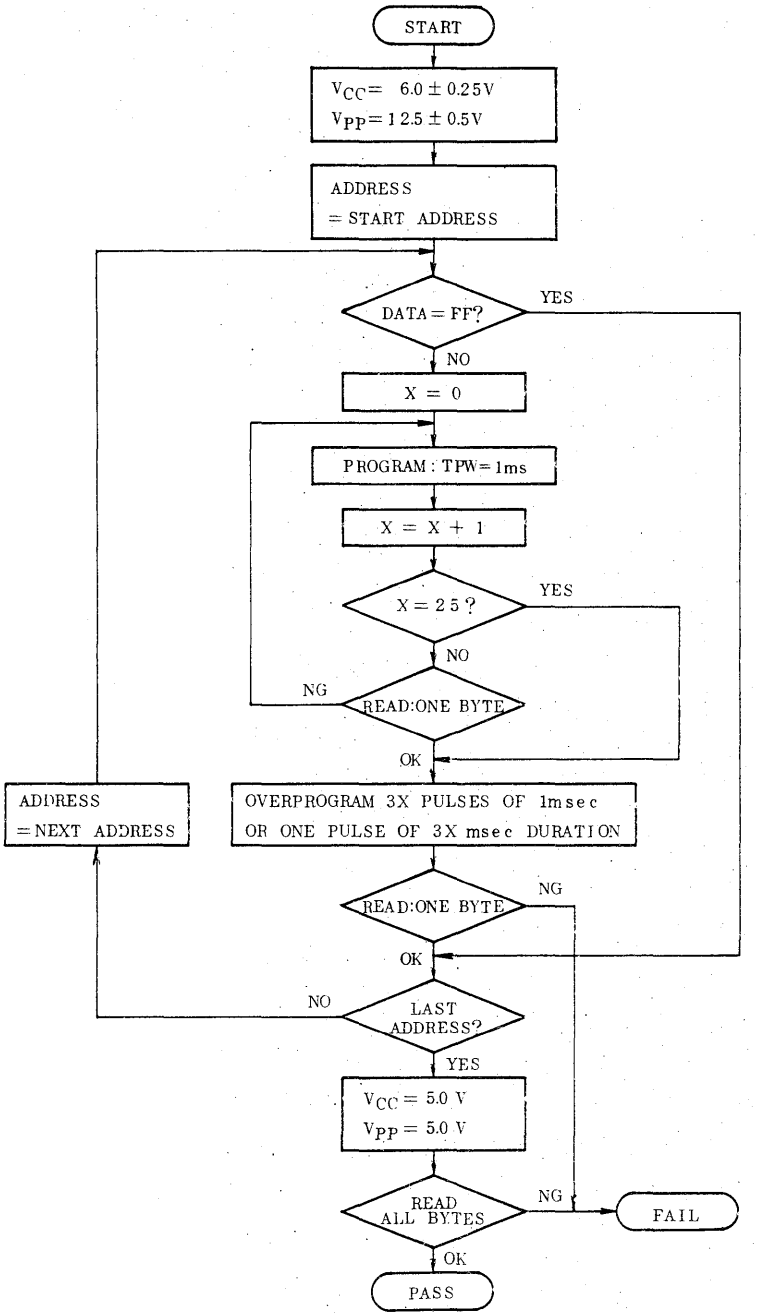
HIGH SPEED PROGRAMMING MODE II

The program time can be greatly decreased by using this high speed programming mode II. This high speed programming mode II is performed at V_{CC}=6.25V and V_{PP}=12.75V. The programming is achieved by applying a single TTL low level 0.1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

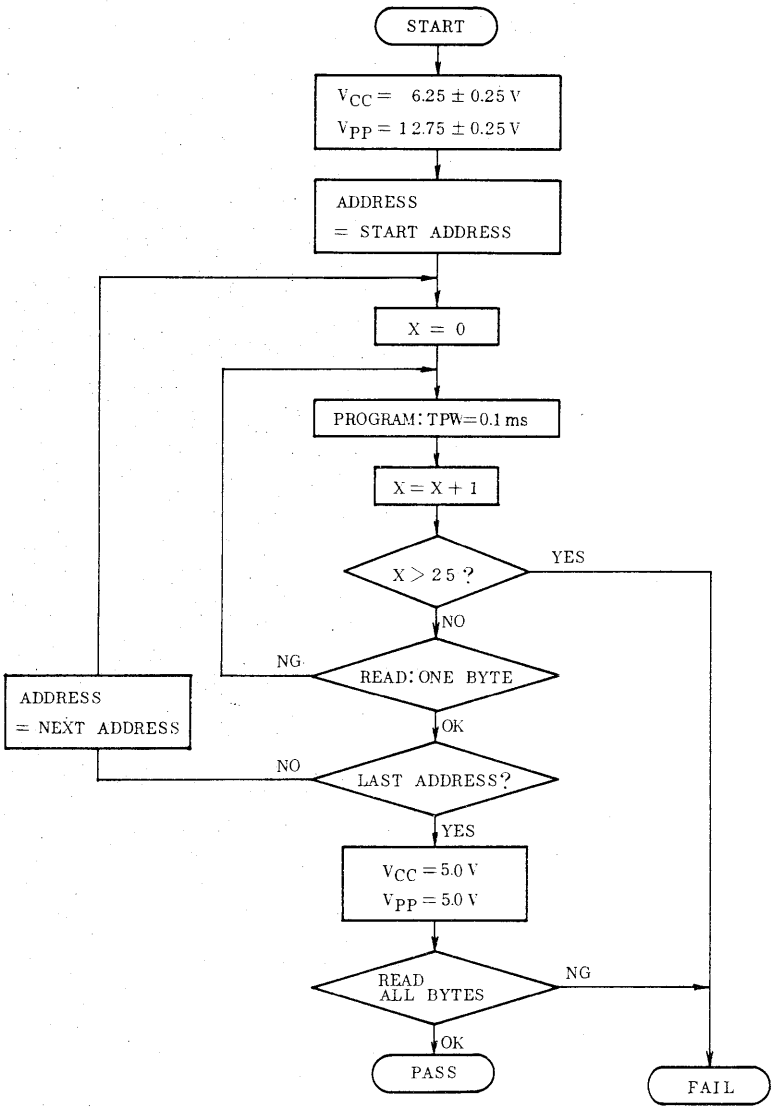
If the programmed data is not correct, another program pulse of 0.1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAMMING MODE I FLOW CHART



HIGH SPEED PROGRAMMING MODE Ⅱ FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27256BD which identifies its manufacture and device type.

The programming equipment may read out manufacturer code and device code from TMM27256BD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM27256BD.

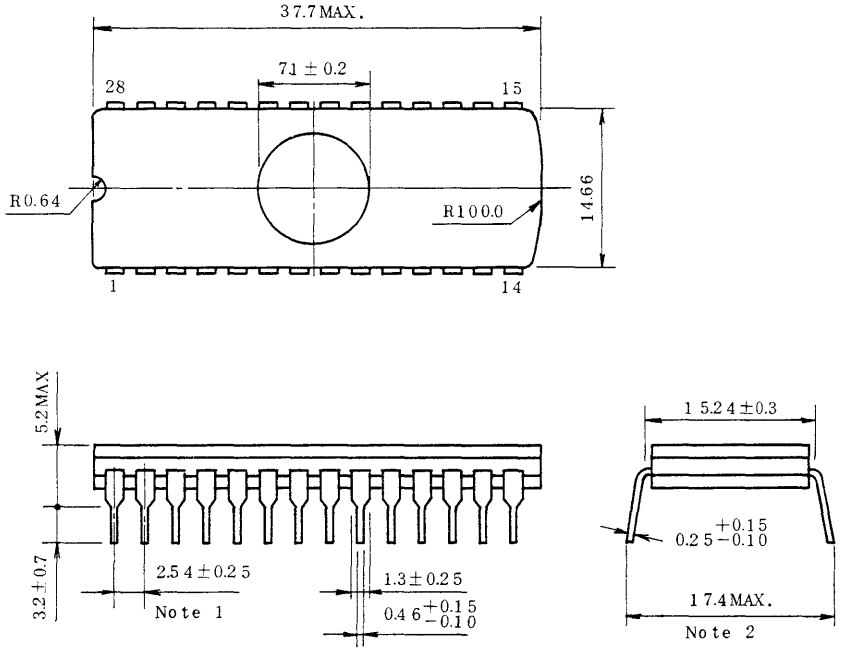
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

32,768 WORD×8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM27256BDI-15, TMM27256BDI-20

PRELIMINARY

DESCRIPTION

The TMM27256BDI is a 32,768 word x 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27256BDI's access time is 150ns/200ns, and the TMM27256BDI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

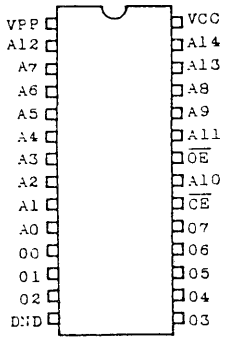
For program operation, the programming is achieved by using the high speed programming mode. The TMM 27256BDI is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

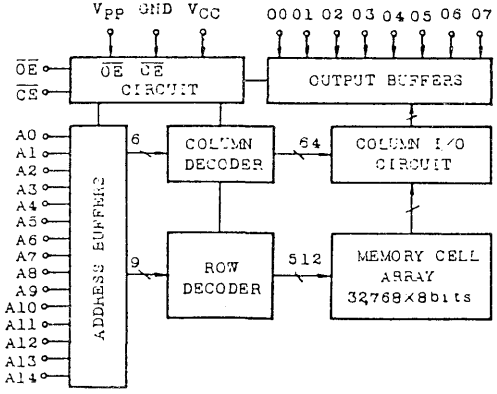
	−15	−20
V_{CC}	5V ± 5%	
t_{ACC}	150ns	200ns
I_{CC2}	120mA	
I_{CC1}	35mA	

- Wide operating temperature range −40 ~ 85°C
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with i27256
- Standard 28 pin DIP cerdip package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V[1] 12.75V[2]	6V[1] 6.25V[2]	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

1): HIGH SPEED PROGRAMMING MODE I

2): HIGH SPEED PROGRAMMING MODE II

TC57256AD-12

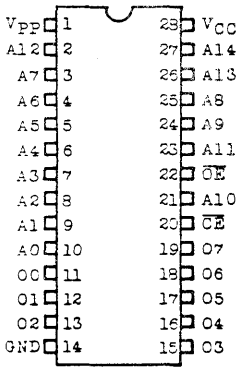
DESCRIPTION

The TC57256AD is a 32,768 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC57256AD's access time is 120ns,and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technology reduces the maximum active current to 30mA/8.3MHz and standby current to 100uA. For program operation, the programming is achieved by using the high speed programming mode. For program operation, the programming is achieved by using high speed programming mode. TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

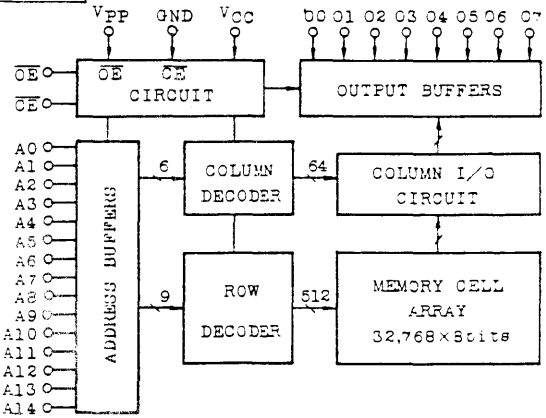
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 30mA/8.3MHz
  Standby: 100uA
- Fast access time:
  TC57256AD-12 120ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, TMM27256AD and TC57256D
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ∿ A14	Address Inputs
O0 ∿ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	Vpp Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V

D.C. and OPERATING CHARACTERISTICS (Ta= 0 ~ 70 °C, V_{CC}=5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ~ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=8.3MHz	-	-	30	mA
I_{CC02}		I_{OUT}=0mA	f=1MHz	-	-	10	mA
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{CC} Current	V_{PP}=V_{CC} + 0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ~ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (Ta= 0 ~ 70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-12		UNIT
			MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	120	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	120	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	60	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	50	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	50	
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	

A.C. TEST CONDITIONS

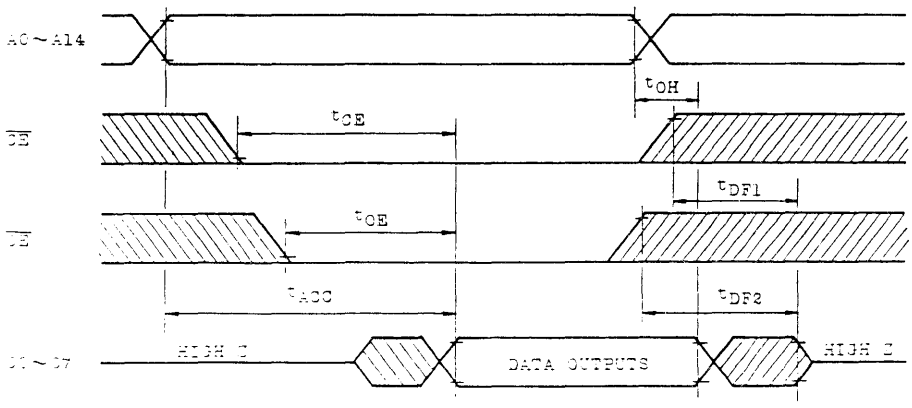
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

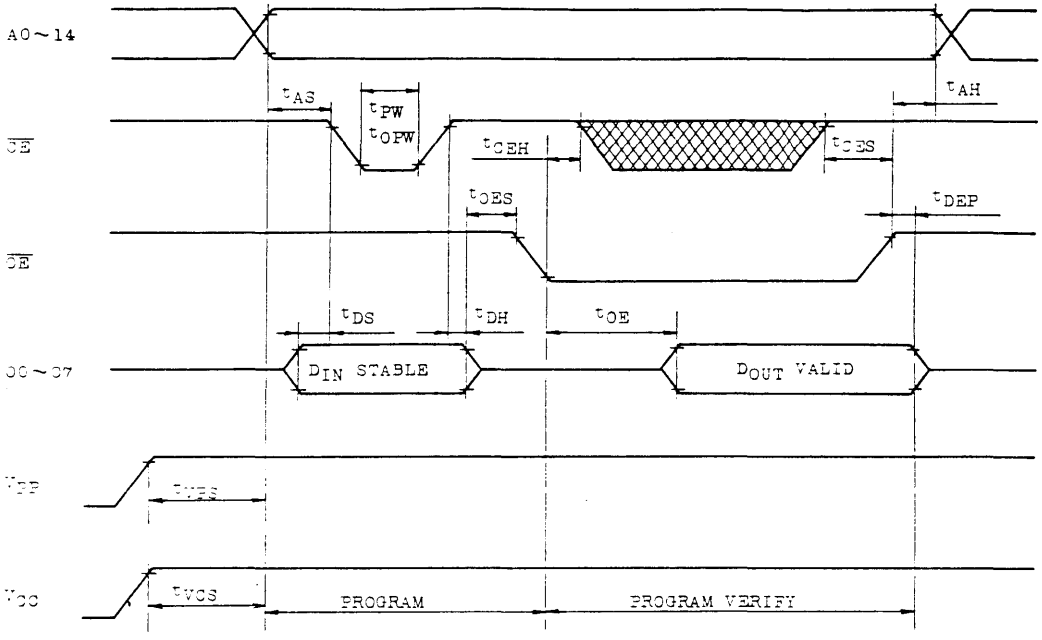
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.
Then intergrated does (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm^2].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes.
And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm^2] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [μw/cm^2] × (20 × 60) [sec] ≅ 15 [w · sec/cm^2].)
The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta= 0 ∿ 70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25 ± 5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57256AD's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57256AD is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.
The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

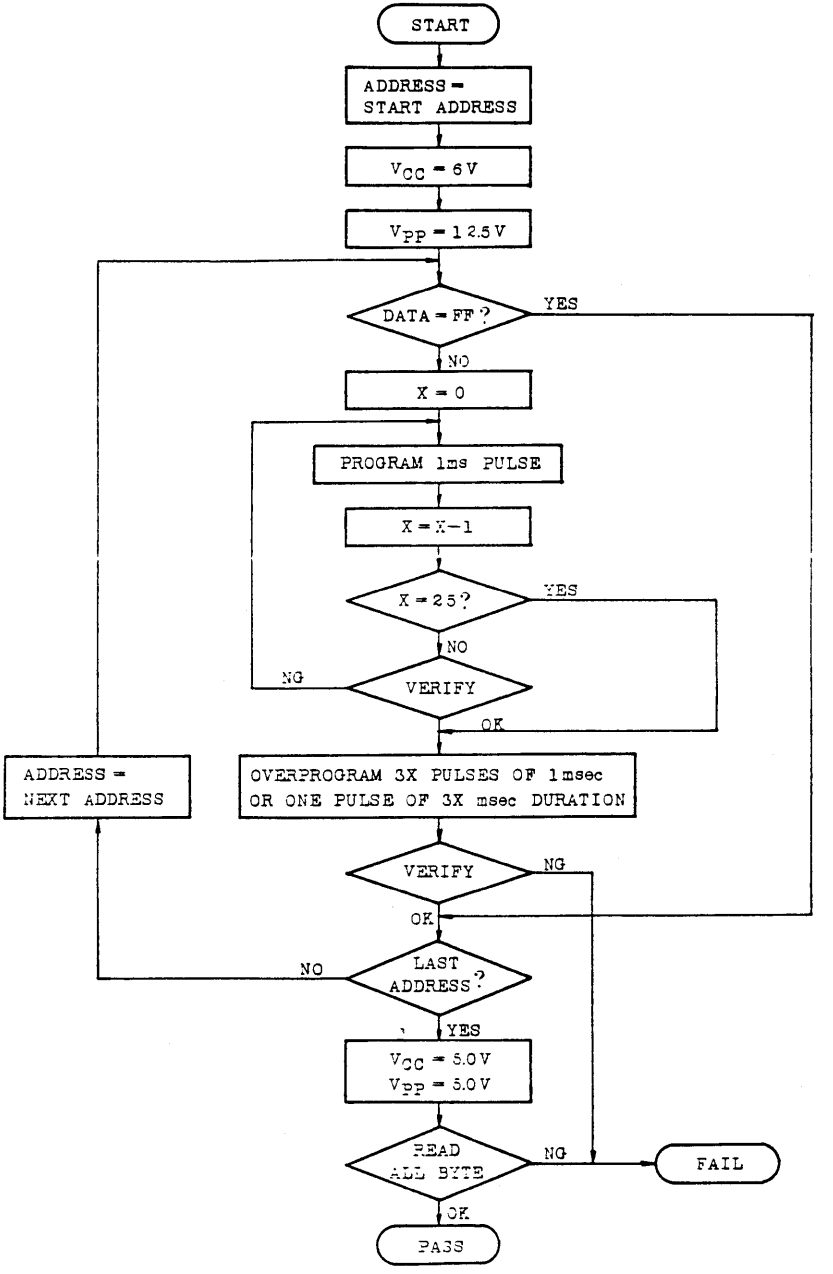
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.
Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electirc signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electirc signature of TC57256AD.

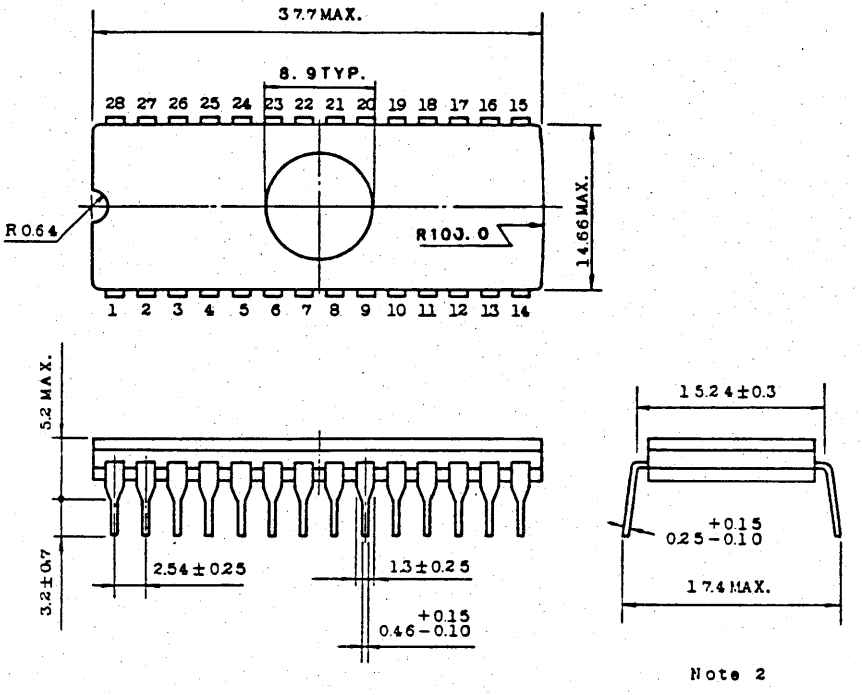
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note 1

Note 2

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD X 8 BIT CMOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

SILICON STACKED GATE MOS

TC57256AD-15
TC57256AD-20

DESCRIPTION

The TC57256AD is a 32,768 word x 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory. For read operation, the TC 57256AD's access time is 150ns, and the TC57256AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. Advanced CMOS technnology reduces the maximum active current to 30 mA/6.7MHz and standby current to 100μA

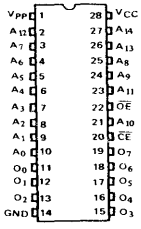
For program operation, the programming is achieved by using the high speed programming mode.

TC57256AD is fabricated with the CMOS technology and the N-channel silicon double layer gate MOS technology.

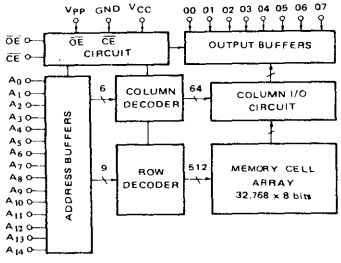
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Low power dissipation
  30mA/6.7MHZ (atcive)
  100μA (standby)
- Fast access time TC57256AD-15 150ns
  TC57256AD-20 200ns
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P and TMM23256P EPROM i27256
- Standard 28 pin DIP cerdip Package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

PIN / MODE	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H		5V	High Impedance	
Standby	H	*		5V	High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS ($Ta=-40 \sim 85°C$, $V_{CC}=5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0V \sim V_{CC}$		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}=0V$	f=6.7MHz	-	-	30	mA
I_{CC02}		$I_{OUT}=0mA$	f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}=V_{IH}$		-	-	1	mA
I_{CCS2}		$\overline{CE}=V_{CC}-0.2V$		-	-	100	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		-	-	0.4	V
I_{PP1}	V_{CC} Current	$V_{PP}=V_{CC} \pm 0.6V$		-	-	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4V \sim V_{CC}$		-	-	±10	μA

A.C. CHARACTERISTICS ($Ta=-40 \sim 85°C$, $V_{CC}=5V \pm 5\%$, $V_{PP}=V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	TC57256AD-15		TC57256AD-20		UNIT
			MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}=\overline{OE}=V_{IL}$	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IL}$	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	0	60	0	60	
t_{OH}	Output Data Hold Time	$\overline{CE}=\overline{OE}=V_{IL}$	0	-	0	-	

A.C. TEST CONDITIONS

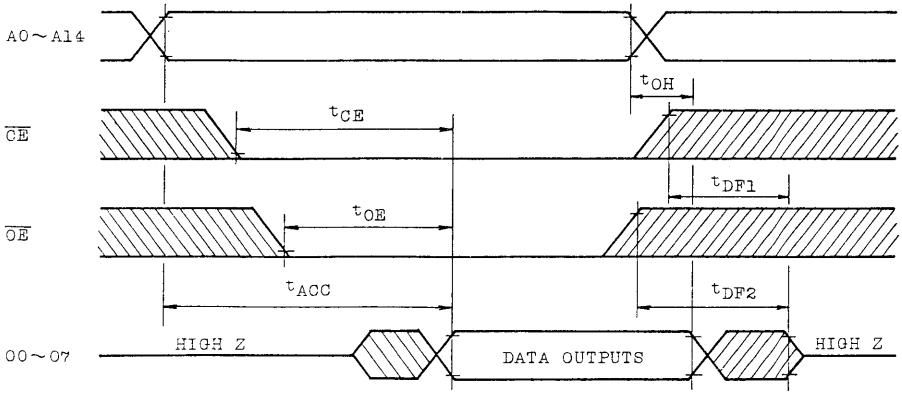
- Output Load : 1 TTL Gate and $C_L=100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE *($Ta=25°C$, $f=1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=0V$	-	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TESTCONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta=25 \pm 5°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=12.5V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	-	-	130	ns

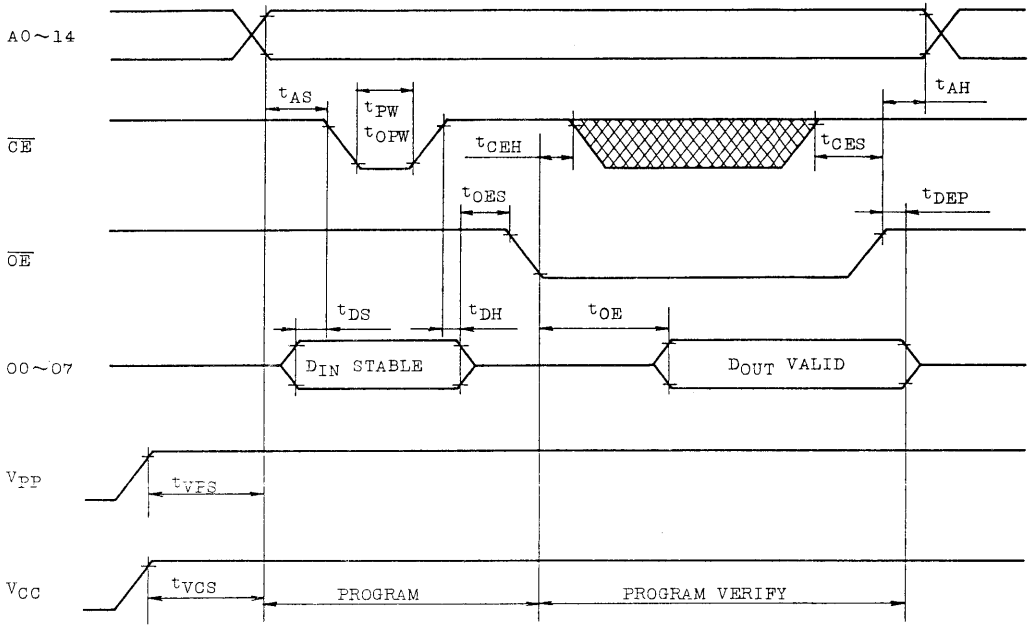
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC57256AD's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window.
Then intergrated does (ultraviolet light intensity [w/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [$w \cdot sec/cm^2$].
When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu w/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated does is 12000 [$\mu w/cm^2$] × (20 × 60) [sec] ≅ 15 [$w \cdot sec/cm^2$].)
The TC57256AD's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opaque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TC57256AD's six operation modes are listed in the following table.
Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25 ± 5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC57256AD has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more TC57256AD's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC57256AD has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC57256AD is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC57256AD are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC57256AD is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low under $\overline{OE}$=V_{IH}.
The TC57256AD can be programmed any location at any time either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL}.

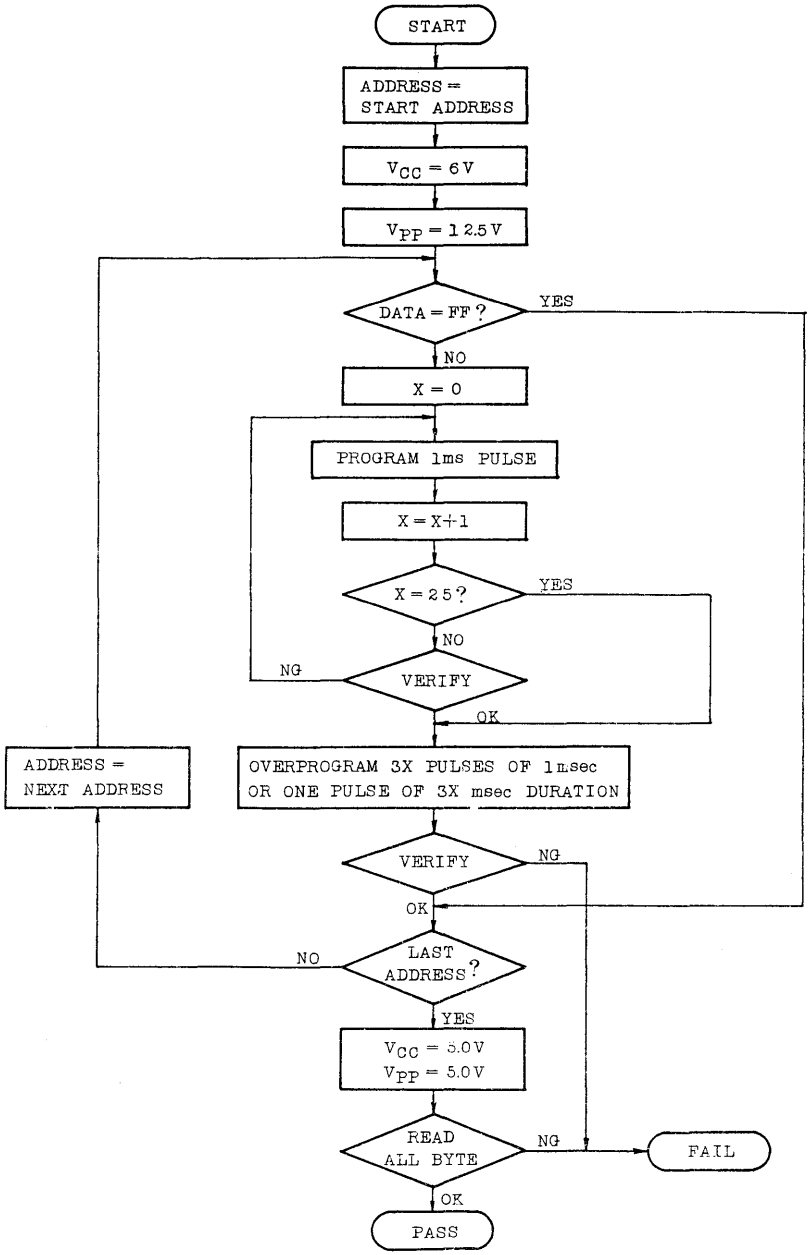
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to Vpp terminal, a high level $\overline{CE}$ input inhibits the TC57256AD from being programmed.
Programming of two or more TC57256AD's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V.
The programming is achieved by applying a single TTL low level lms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of lms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times)
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with V_{CC}=Vpp=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC57256AD which identifies its manufacturer and device type.

The programming equipment may reads out manufacturer code and device code from TC57256AD by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electirc signature of TC57256AD.

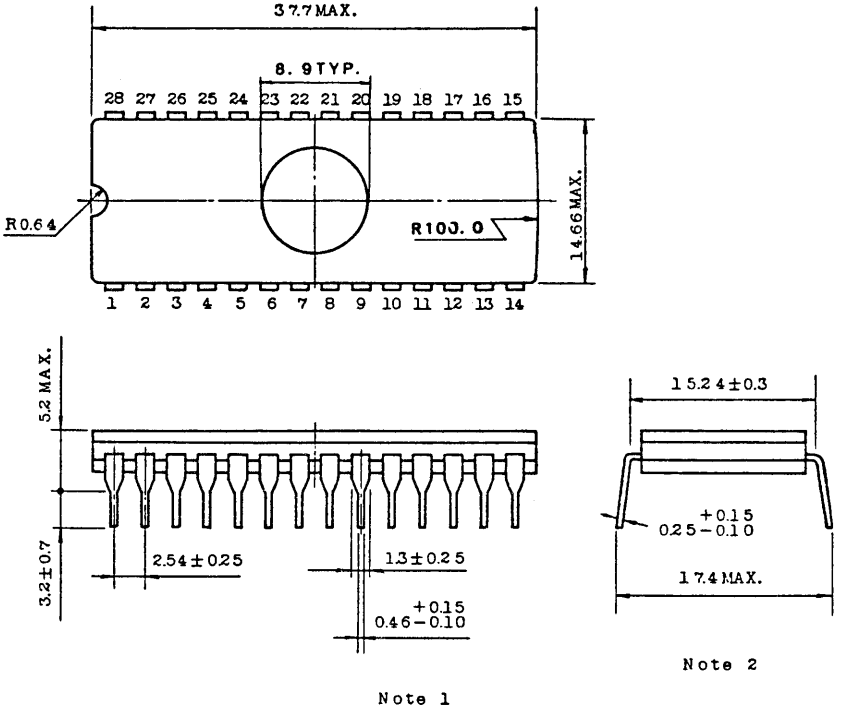
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS

Unit in mm



Note 1

Note 2

Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512D-20,TMM27512D-200
TMM27512D-25,TMM27512D-250

DESCRIPTION

The TMM27512D is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read memory.

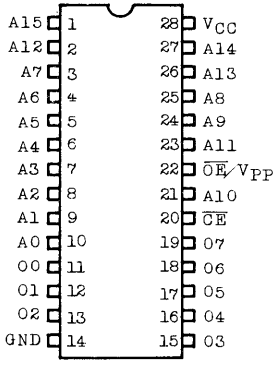
For read operation, the TMM27512D's access time is 200ns/250ns. The TMM27512D operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input. For program operation, the programming is achieved by using the high speed prgramming mode. The TMM27512D is fabricated with N-channel silicon double layer gate MOS technology.

FEATURES

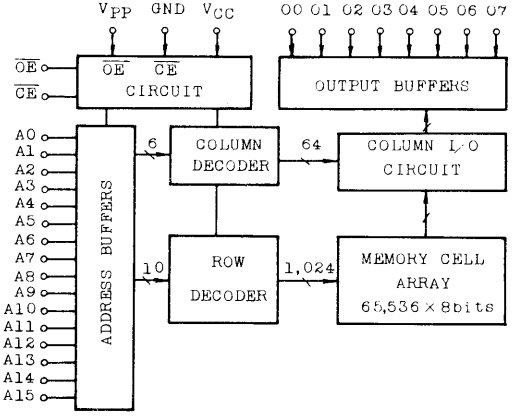
	−20	−25	−200	−250
V_{CC}	5V±5%		5V±10%	
t_{ACC}	200ns	250ns	200ns	250ns
I_{CC2}	120mA		130mA	
I_{CC1}	35mA		40mA	

- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512D-20/25	TMM27512D-200/250
Ta	Operating Tamperature	0~70°C	0~70°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%	5V±10%

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$		—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4\sim V_{CC}$		—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	-20/25	—	—	35	mA
			−200/250	—	—	40	
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	−20/25	—	—	120	mA
			−20/250	—	—	130	
V_{IH}	Input High Voltage	—		2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	—		−0.3	—	0.8	V
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$		2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$		—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6$		—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512D-20/200		TMM27512D-25/250		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

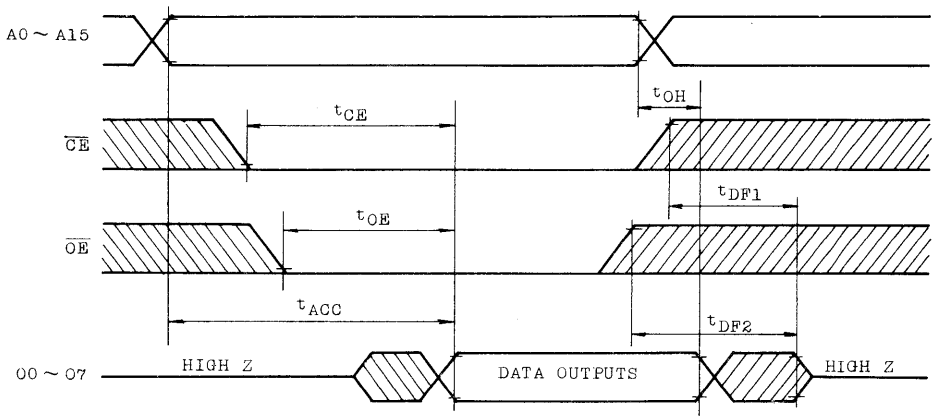
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	—	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	—	—	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	—	—	130	ns

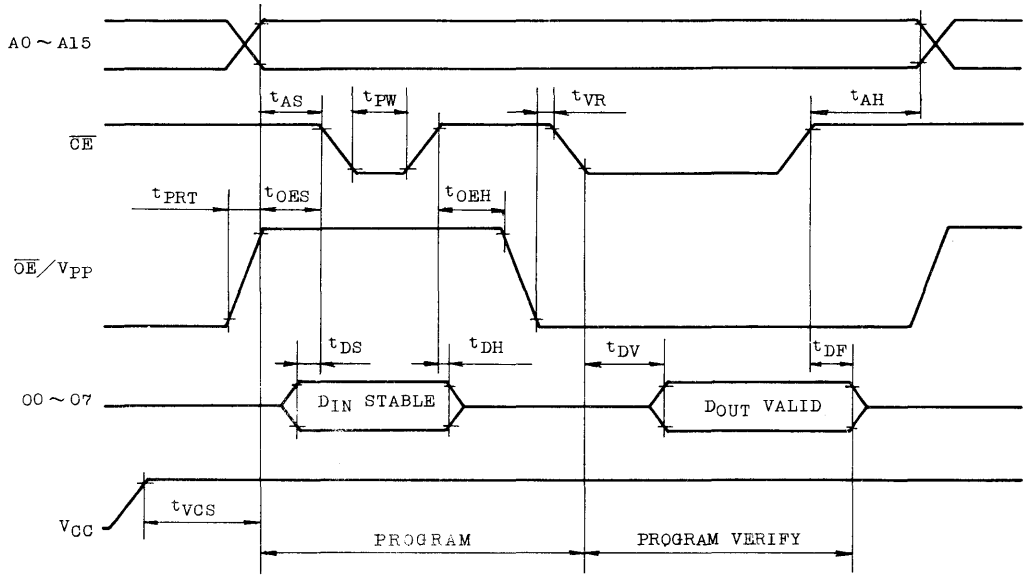
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note: (1) V_{CC} must be applied simultaneously with or before V_{PP} and cut off simultaneously with or after V_{PP}.
(2) Removing the device from the socket and setting the device in the socket with V_{PP}=12.5 V may cause permanent damage to the device.
(3) The V_{PP} supply voltage is permitted up to 14V for program operation; Voltages over 14V should be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not exceed 14V.

ERASURE CHARACTERISTICS

The TMM27512D's erasure is achieved by applying shortwave ultraviolet light with a wavelength of 2537Å (Angstroms) through the transparent window of the chip.

The integrated dose (ultraviolet light intensity [w/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w · sec/cm²].

When the Toshiba GL-15 sterilizing lamp is used and the device is exposed at a distance of 1cm from the lamp surface, erasure will be achieved within 60 minutes.

Using a commercial lamp with an ultraviolet light intensity of 12000 [μw/cm²] reduces the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] × (10×60) [sec] ≅ 15 [w · sec/cm²].)

The TMM27512D's erasure begins to occur when exposed to light with wavelengths shorter than 4000Å. Sunlight and flourescent lamps both include 3000~4000Å wavelength components. Therefore when used under such lighting for extended periods of time, opaque seals-Toshiba EPROM Protect Seal AC901-are available

OPERATION INFORMATION

The TMM27512D's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE	PIN NAMES(NUMBER)	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM27512D has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addressess.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

With $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, outputs will be in a high impedance state, so two or more TMM27512D's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512D has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27512D is placed in the standby mode which reduces 70% of the operating current. The outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512D are in the "1" state which is the erased state. The programming operation introduces "Os" data into the desired bit locations by electrical programming.

The TMM27512D is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level

The TMM27512D can be programmed at any location, anytime, either individually, sequentially or at random.

PROGRAM VERIFY MODE

The verify mode verifies that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and at $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512D from being programmed.

Programming of two or more TMM27512D's in parallel with different data is easily accomplished: all inputs except for $\overline{CE}$ are commonly connected, a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only, and TTL high level signals are applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programming mode is performed at V_{CC}=6.0V and $\overline{OE}/V_{PP}$=12.5V

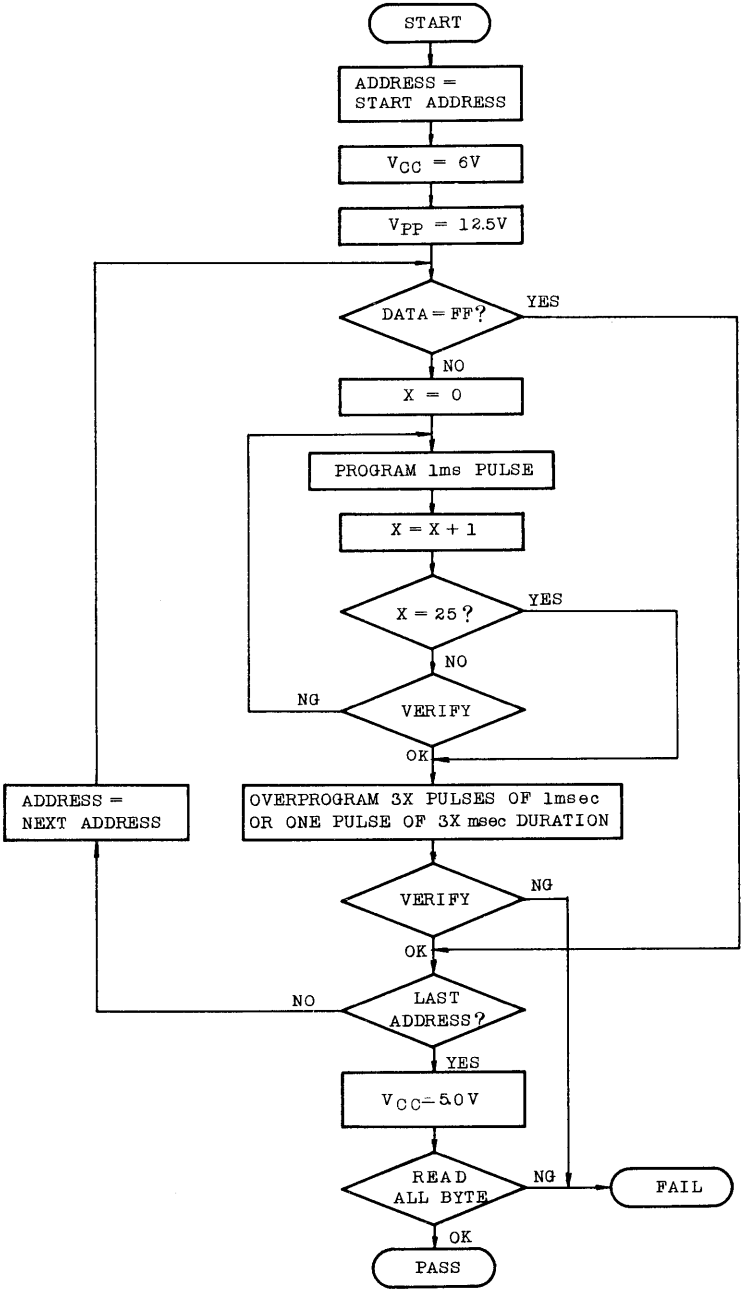
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. The programmed data is then verified by using the Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and the programmed data is reverified. This should be repeated until the programmed data is correct. (max. 25 times)

After correctly programming the selected address, an additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=5V.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows a code to be read from the TMM27512D which identifies its manufacture and device type.

The programming equipment may be used to read out the manufacturer code and device code from the TMM27512D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines are set to V_{IL} in read operation. Data output under these conditions is the manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

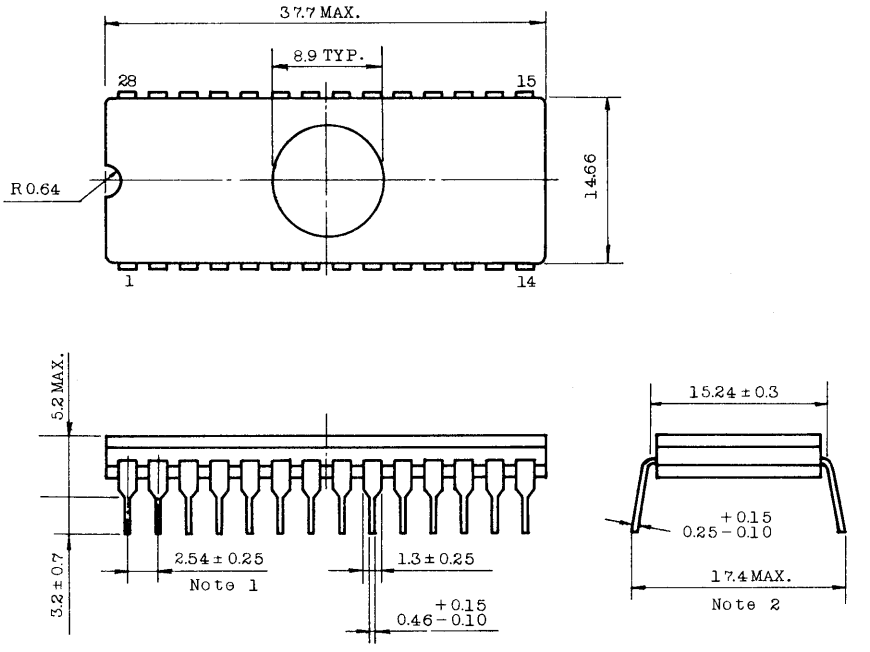
The following table shows electric signature of the TMM27512D.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V±0.5V
A1~A8, A10~A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD × 8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY
PRELIMINARY

TMM27512DI-20
TMM27512DI-25

DESCRIPTION

The TMM27512DI is a 65,536 word × 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27512DI's access time is 200ns/250ns. The TMM27512DI operates from a single 5-volt power supply and has a low power standby mode which reduces power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

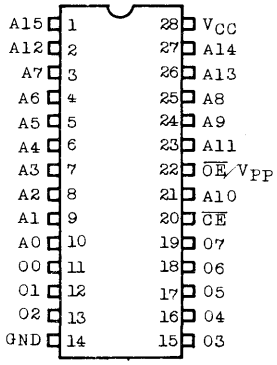
For program operation, the programming is achieved by using the high speed prgramming mode. TMM27512DI is fabricated with N-channel silicon double layer gate MOS technology.

FEATURES

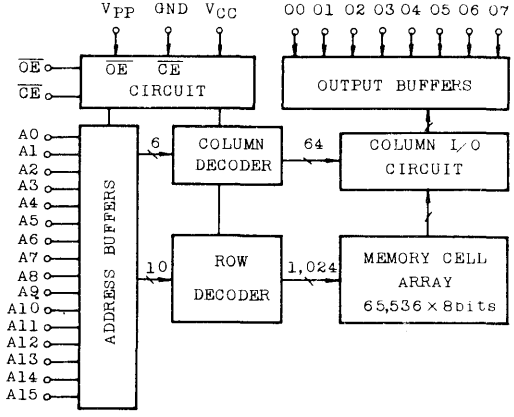
	−15	−20
V_{CC}	5V±5%	
t_{ACC}	150ns	200ns
I_{CC2}	120mA	
I_{CC1}	35mA	

- Wide operating temparature range −40~85°C
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{15}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
P_{STG}	Storage Temperature	−65~125	°C
T_{OPR}	Operating Temperature	−40~85	°C

READ OPERATION

D. C. AND RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TMM27512DI-20/25
Ta	Operating Temperature	−40~85°C
V_{CC}	V_{CC} Power Supply Voltage	5V±5%

D. C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0.4\sim V_{CC}$	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}=V_{IH}$	—	—	40	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}=V_{IL}$	—	—	130	mA
V_{IH}	Input High Voltage	—	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	—	−0.3	—	0.8	V
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP}=0\sim V_{CC}+0.6$	—	—	±10	μA

A. C. CHARACTERISTICS

SYMBOL	PARAMETER	TMM27512DI-20		TMM27512DI-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	—	200	—	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	—	250	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	—	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns

A. C. TEST CONDITIONS

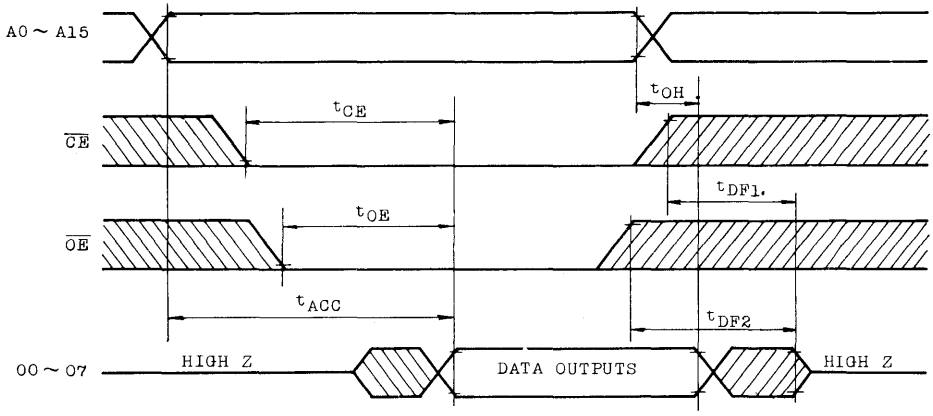
- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	$V_{IN}=0V$	—	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN}=0V$	—	50	60	pF
C_{OUT}	Output Capacitance	$V_{OUT}=0V$	—	8	12	pF

* This paramater is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Outpu Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	130	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	—	2	—	—	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	—	2	—	—	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	—	50	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}/V_{PP}=V_{PP}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}=V_{IL}$	—	—	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}=V_{IL}$	—	—	130	ns

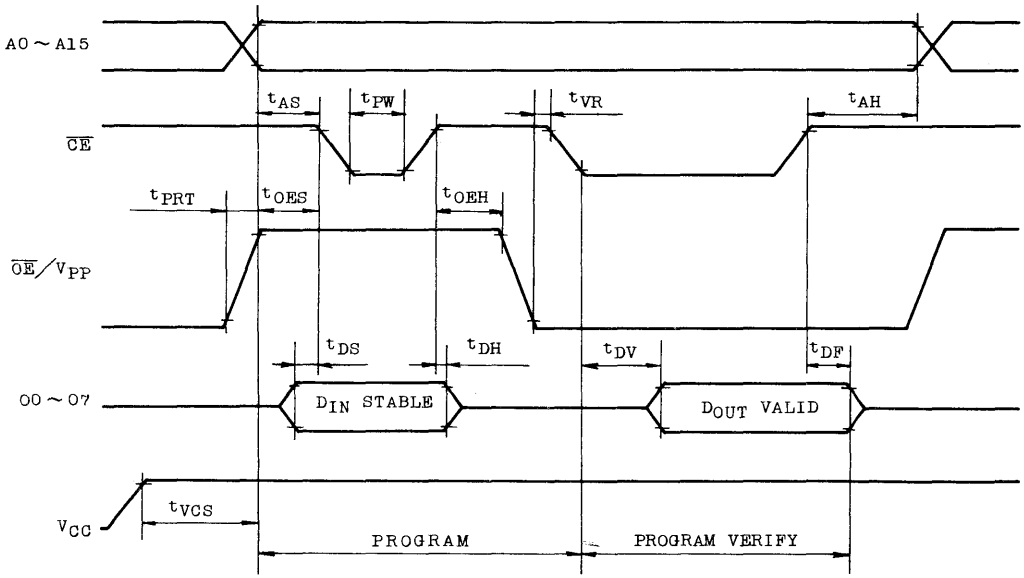
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should be aplied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TMM27512DI's erasure is achieved by applying shortwave ultraviolet light which has a wavelegth of 2537A (Angstroms) to the Chip through the transparent window. Then integrated dose (ultraviolet light intensity [W/cm²] × exposure time [sec.]) for erasure should be a minimum of 15 [w·sec/cm²]

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [μw/cm²] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [μw/cm²] ×(10×60) [sec] ≅15 [w·sec/cm²] .)

The TMM27512DI's erasure begins to occur when exposed to light with wavelength shorter than 4000A. The sunlight and the flourescent lamps will include 3000~4000A wevelength components. Therefore when used under such lighting for extended periods of time, the opeque seals-Toshiba EPROM Protect Seal AC901-are available.

OPERATION INFORMATION

The TMM27512DI's six operation modes are listed in the following table.

Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O_0~O_7 (11~13, 15~19)	POWER
Read Operation (Ta=−40~85°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	Active
	Standby	H	*		High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	Active
	Program Verify	L	L		Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM27512DI has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state.

So two or more TMM27512DI's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM27512DI has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a high level to the $\overline{CE}$ input, the TMM27512DI is placed in the standby mode which reduce 70% of the operating current by applying TTL-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM27512DI are in the "1" state which is erased state.

Therefore the program operation is to introduce "O's" data into the desired bit locations by electrically programming.

The TMM27512DI is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level.

The TMM27512DI can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}/V_{PP}$ at V_{IL} and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM27512DI from being programmed.

Programming of two or more TMM27512DI's is parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode.

This high speed programing mode is performed at $V_{CC}=6.0V$ and $\overline{OE}/V_{PP}=12.5V$

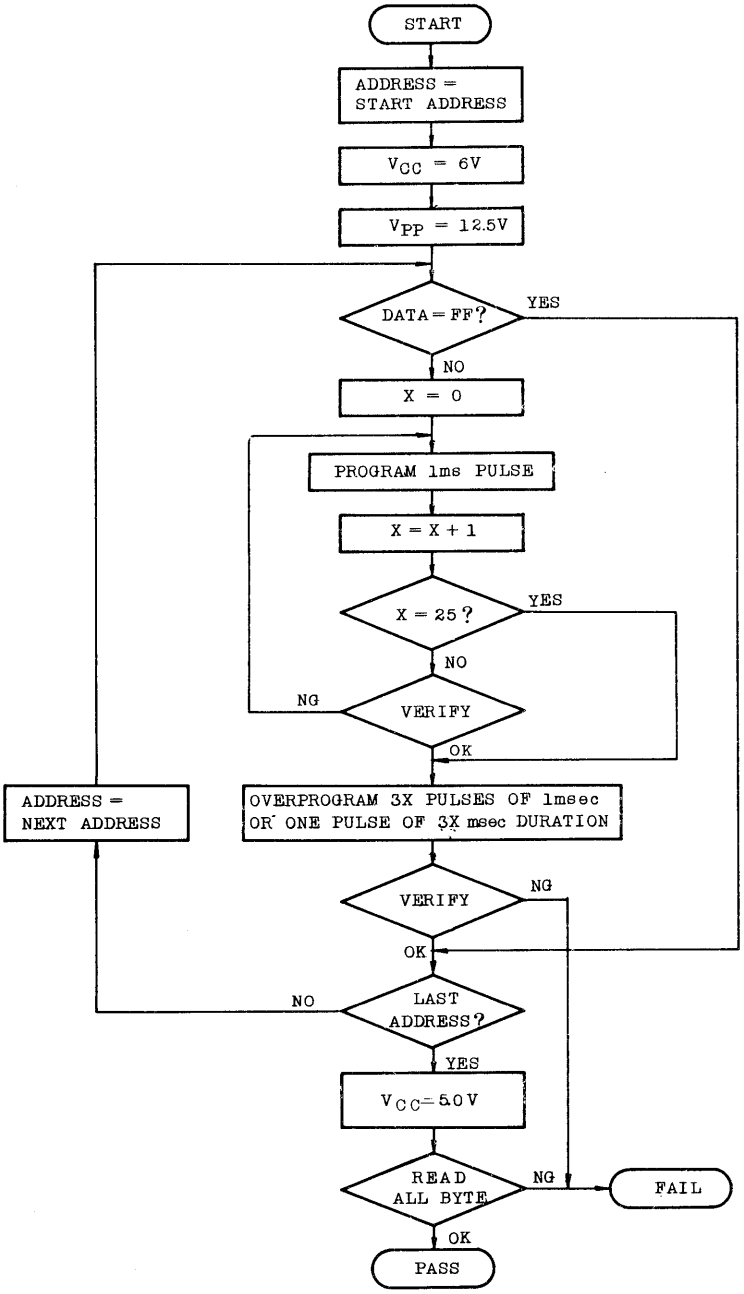
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width 3 times that needed for initial programming is applied.

When programming has been completd, the data in all addresses should be verified with $V_{CC}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM27512DI which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM27512DI by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

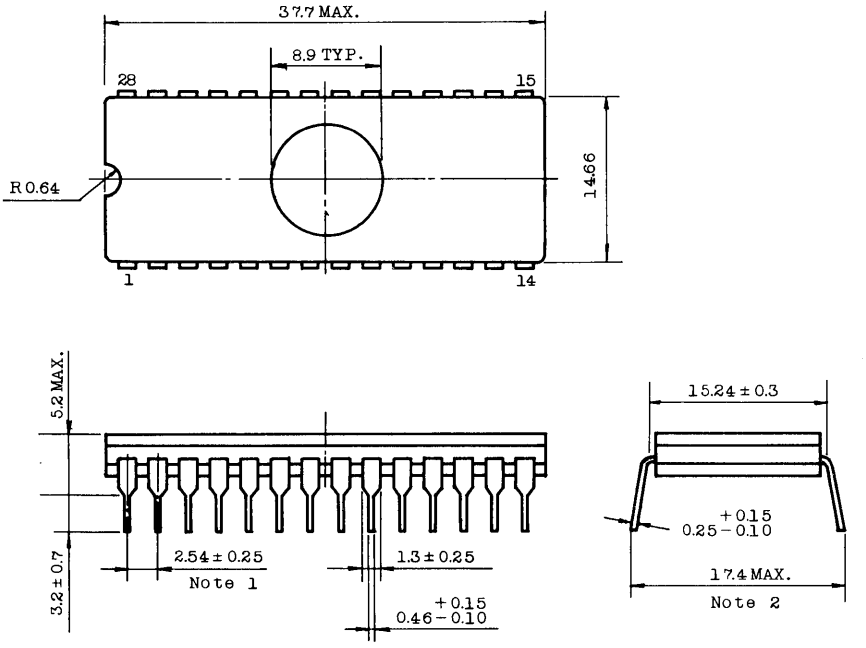
The following table shows electric signature of TMM27512DI.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes : A9 = 12V ± 0.5V
A1 ~ A8, A10 ~ A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS

Unit in mm



Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in milimeters.

65,536 WORD×8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM27512AD-17
TMM27512AD-20, TMM27512AD-200
TMM27512AD-25, TMM27512AD-250

PRELIMINARY

DESCRIPTION

The TMM27512AD is a 65,536 word x 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27512AD's access time is 170ns/200ns/250ns, and the TMM27512AD operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

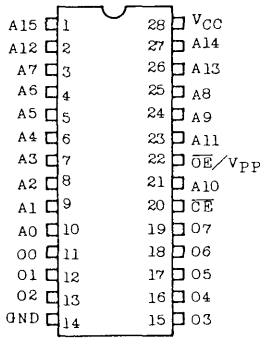
For program operation, the programming is achieved by using the high speed programming mode. The TMM 27512AD is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

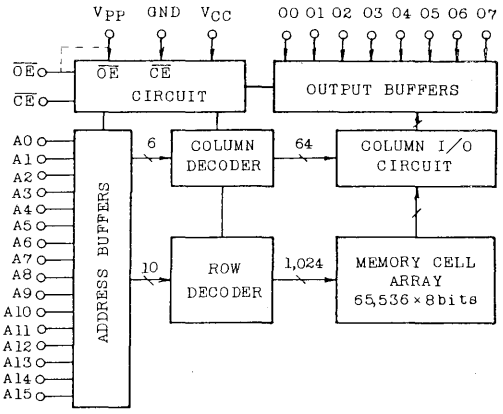
	−17	−20	−25	−200	−250
V_{CC}	5V ± 5%			5V ± 10%	
t_{ACC}	170ns	200ns	250ns	200ns	250ns
I_{CC2}	120mA			130mA	
I_{CC1}	35mA			40mA	

- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V[1] 6.25V[2]	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

TOSHIBA MOS MEMORY PRODUCTS

65,536 WORD×8 BIT N-MOS UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

TMM27512ADI-17, TMM27512ADI-20, TMM27512ADI-25

PRELIMINARY

DESCRIPTION

The TMM27512ADI is a 65,536 word x 8 bit ultraviolet light erasable and electrically programmable read only memory.

For read operation, the TMM27512ADI's access time is 170ns/200ns/250ns, and the TMM27512ADI operates from a single 5-volt power supply and has low power standby mode which reduces the power dissipation without increasing access time. The standby mode is achieved by applying a TTL-high level signal to the $\overline{CE}$ input.

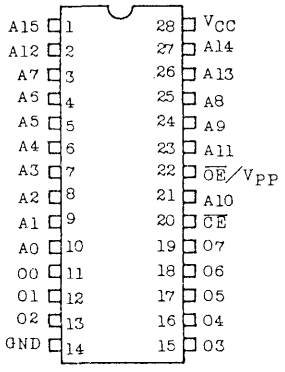
For program operation, the programming is achieved by using the high speed programming mode. The TMM 27512ADI is fabricated with the N-channel silicon double layer gate MOS technology.

FEATURES

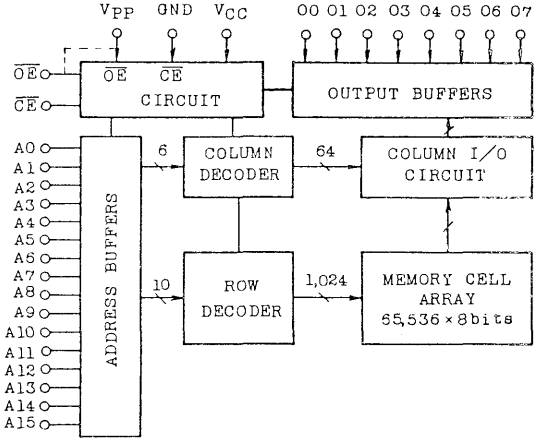
	−17	−20	−25
V_{CC}	5V ± 5%		
t_{ACC}	170ns	200ns	250ns
I_{CC2}	130mA		
I_{CC1}	40mA		

- Wide operating temperature range −40 ~ 85°C
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with i27512
- Standard 28 pin DIP cerdip package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V[1)] 6.25V[2)]	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I

2): HIGH SPEED PROGRAMMING MODE II

TC571000D-15, -20, -200, -25
TC571001D-15, -20, -200, -25

DESCRIPTION

The TC571000D/TC571001D is a 131,072 word × 8 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571000D is JEDEC standard pin configuration and the TC571001D is compatible with 28 pin 1M bit Mask ROM. Both products are packed in 32 pin standard cerdip package.

TC571000D/TC571001D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 30mA/6.7MHz and access time of 150ns/200ns/250ns.

The programming times of the TC571000D/TC571001D except overhead times of EPROM programmer is only 14 seconds by using the high speed programming algorithm.

FEATURES

- Peripheral circuit: CMOS

  Memory cell : N-MOS

- Access Time

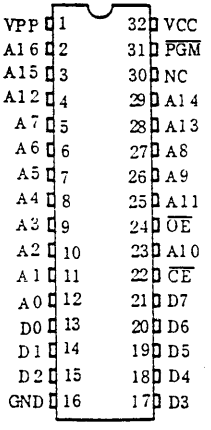
	-15	-20	-25	-200
V_{CC}	5V±5%			5V±10%
Temp	0∿70°C	-40 ∿ 85°C		0 ∿ 70°C
t_{ACC}	150ns	200ns	250ns	200ns

- Low power dissipation

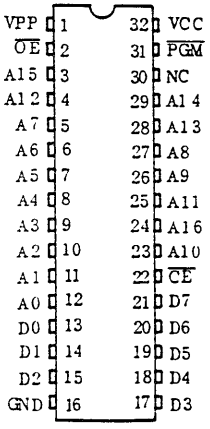
  Active : 30mA/6.7MHz
  Standby: 100μA(Ta=85°C)

- Single 5V power supply
- Full static operation
- High speed programming operation: t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC571000D
- 1M MROM compatible : TC571001D
- Standard 32 pin DIP cerdip package

PIN CONNECTION (TOP VIEW)

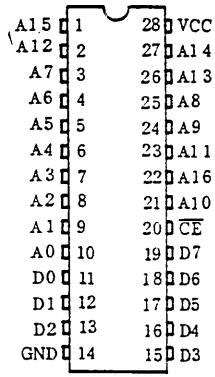


TC571000D



TC571001D

(Reference)

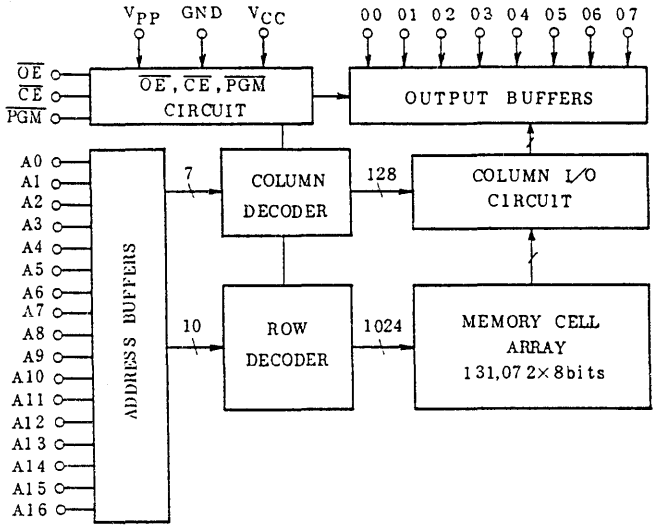


(1M Mask ROM TC531000P)

PIN NAMES

A0 ∿ A16	Address Inputs
D0 ∿ D7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	V_{CC} Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	PGM	CE	OE	VPP	VCC	O0 ~ O7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	V
V_{IN}	Input Voltage	-0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	-40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571000D/1001D-15,-20,-25			TC571000D/1001D-200			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	4.50	5.00	5.50	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. AND OPERATING CHARACTERISTICS (Ta=-40 ~ 85°C)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ~ V_{CC}		-	-	±10	uA
I_{CC01}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CC02}		I_{OUT}=0mA	f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	uA
V_{OH}	Output High Voltage	I_{OH}=-400uA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	uA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ~ V_{CC}		-	-	10	uA

Ta=0 ~ 70°C for TC571000D/TC571001D-15, -200

A.C. CHARACTERSITICS (Ta=-40 ~ 85°C, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TC571000D/1001D -15		TC571000D/1001D -20,-200		TC571000D/1001D -25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	-	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	-	250	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	-	100	
t_{PGM}	$\overline{PGM}$ to Output Valid	-	70	-	70	-	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	0	90	
t_{DF3}	PGM to Output in High-Z	0	60	0	60	0	90	
t_{OH}	Output Data Hold Time	0	-	0	-	0	-	

Ta=0 ~ 70°C for TC571000D/TC571001D-15, -200

A.C. TEST CONDITIONS

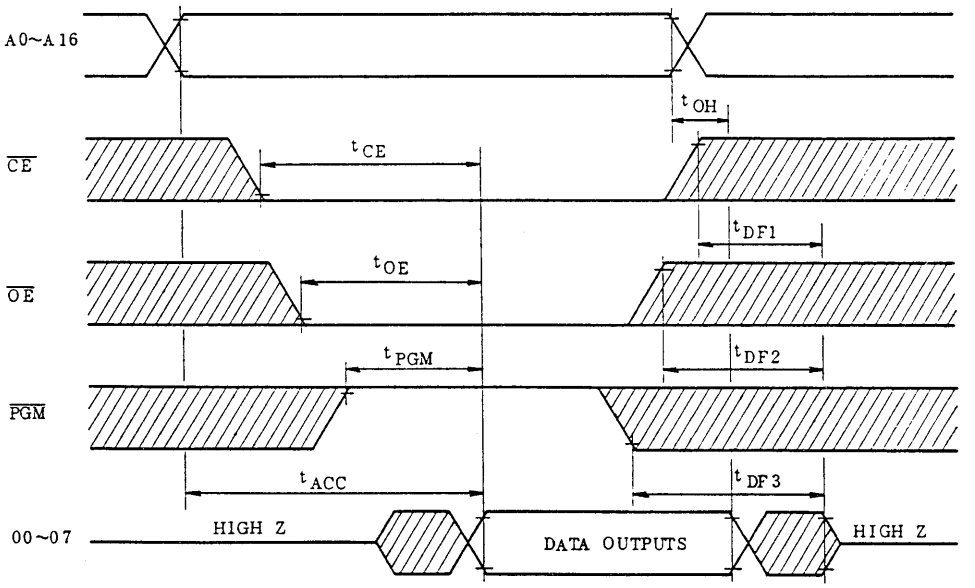
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V 5o 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE* (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	30	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

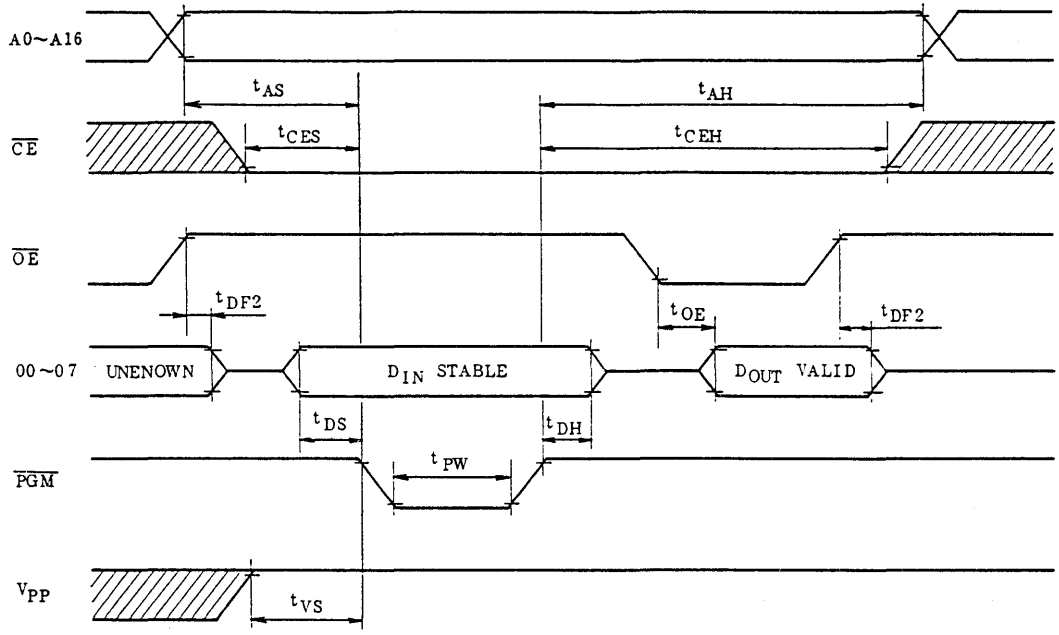
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	-	-	-	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	CE=V_{IL}	-	-	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571000D/TC571001D's erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [$W \cdot sec/cm^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu W/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [$\mu W/cm^2$] × (10 × 60) [sec] ≅ 15 [$W \cdot sec/cm^2$].)

The TC571000D/TC571001D's erasure begins to occur when exposed to light with wavelength shorter then 4000Å. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571000D/TC571001D's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0 ∿ O7	POWER
READ OPERATION (Ta=-40 ∿ 85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC571000D/TC571001D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers. independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.
And assuming that $\overline{CE}$=$\overline{OE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two ormore ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571000D/TC571001D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC571000D/TC571001D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571000D/TC571001D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC571000D/TC571001D can be programmed any location at anytime —— either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571000D/TC571001D from being programmed. Programming of two or more EPROMs in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.

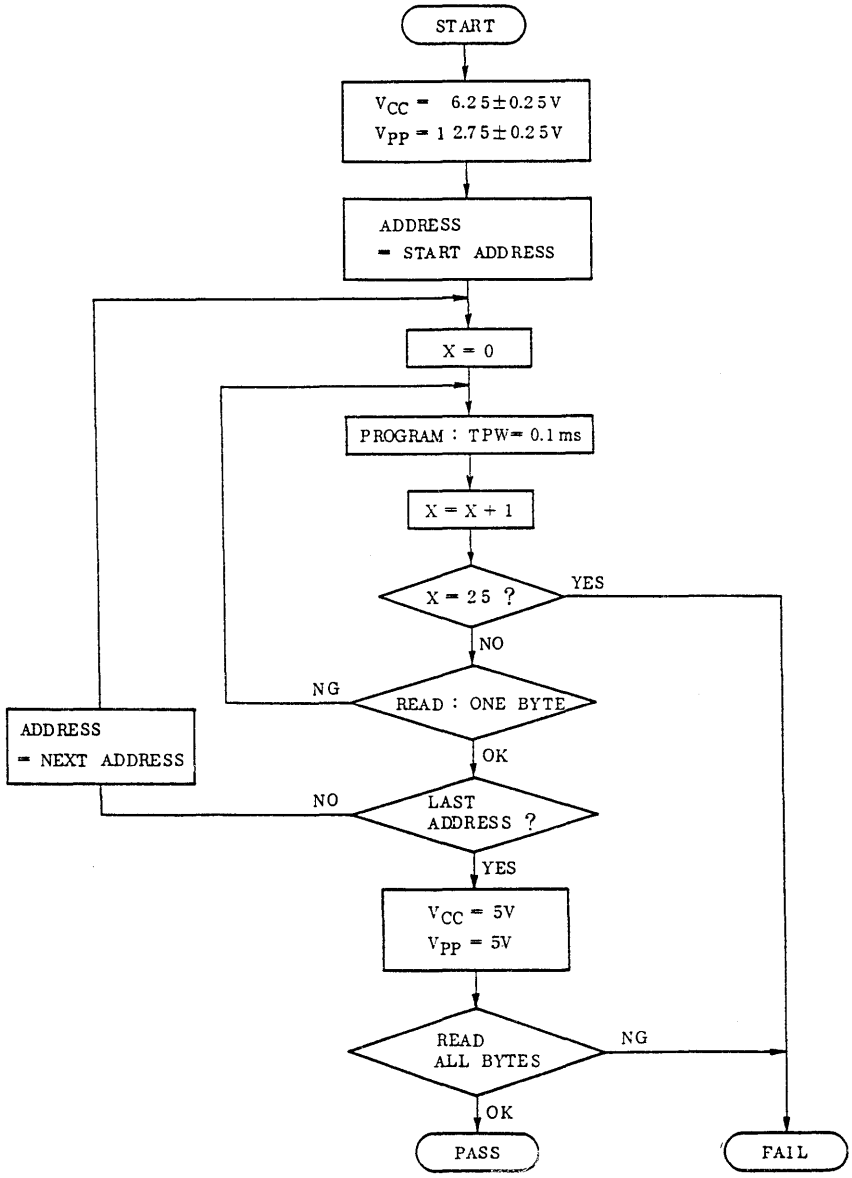
The programming is achieved by applying a single TTL low level 0.1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571000D/TC571001D which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571000D/TC571001D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TC571000D/TC571001D.

SIGNATURE \ PINS		A0	O7	O6	O5	O4	O3	O2	O1	O0	HEX. DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC571000D	V_{IH}	1	0	0	0	0	1	1	0	86
	TC571001D		0	0	0	0	0	1	1	1	07

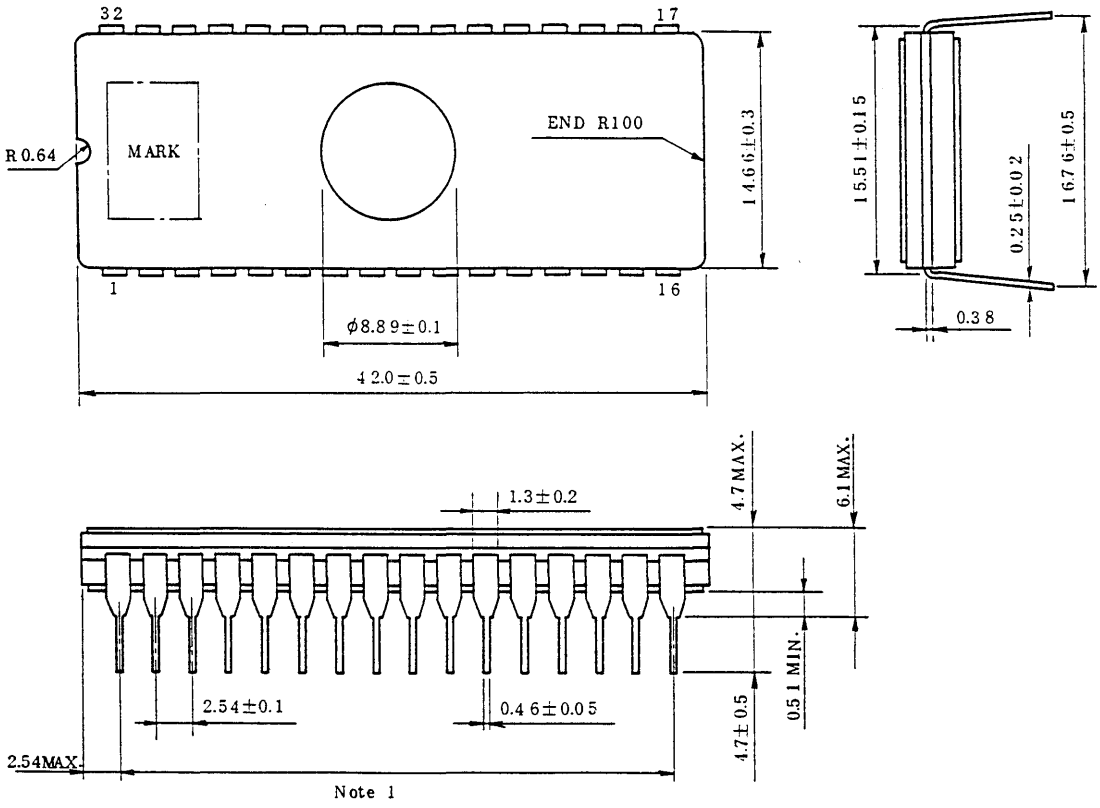
Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A16, $\overline{CE}$, $\overline{OE}$=V_{IL}

$\overline{PGM}$=V_{IH}

OUTLINE DRAWINGS

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.32 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

TC571024D-15, TC571024D-200
TC571024D-20

DESCRIPTION

The TC571024D is a 65,536 word × 16 bit CMOS ultraviolet light erasable and electrically programmable read only memory.

The TC571024D is JEDEC standard pin configuration. This product is packed in 40 pin standard cerdip package.

TC571024D is fabricated with the CMOS technology. Advanced circuit techniques provide both high speed and lowpower features with a maximum operating current of 40mA/6.7MHz and access time of 150ns/200ns.

The programming times of the TC571024D except overhead times of EPROM programmer is only 7 seconds by using the high speed programming algorithm.

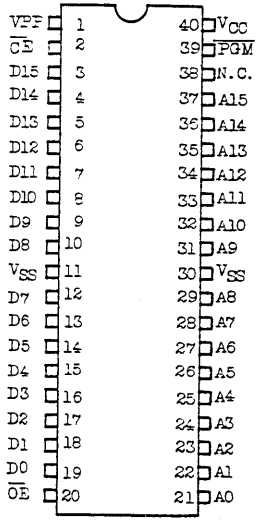
FEATURES

- Peripheral circuit: CMOS
  Memory cell : N-MOS
- Fast access time

	TC571024D-15	TC571024D-20	TC571024D-200
Ta	0 ∿ 70°C	-40 ∿ 85°C	
V_{CC}	5V±5%		5V±10%
t_{ACC}	150ns	200ns	

- Low power dissipation
  Active : 40mA/6.7MHz
  Standby: 100μA
- Single 5V power supply
- Full static operation
- High speed programming operation:
  t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 40 pin: TC571024D
- Standard 40 pin DIP cerdip package

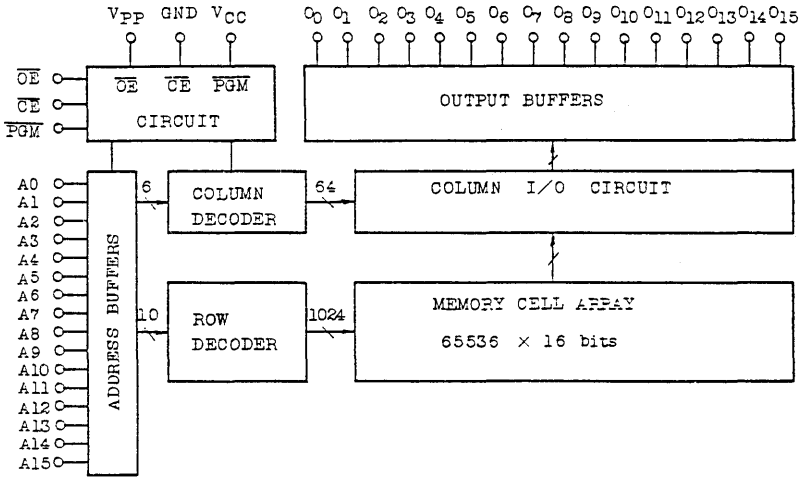
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A15	Address Inputs
D0 ∿ D15	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	VCC Supply Voltage
V_{PP}	Program Supply Voltage
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	$D_0 \sim D_{15}$	POWER
Read	L	L	H	5V	5V	Data Out	Active
Output Deselect	*	H	*			High Impedance	
Standby	H	*	*			High Impedance	Standby
Program	L	*	L	12.75V	6.25V	Data In	Active
Program Inhibit	H	*	*			High Impedance	
	L	H	H				
Program Verify	L	L	H			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
V_{IN} (A9)	Input Voltage (A9)	-0.6 ∿ 13.5	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 • 10	°C•sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

AC/DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TC571024D-15	TC571024D-20	TC571024D-200
Ta	Ambient Temperature	0 ~ 70°C	-40 ~ 85°C	
V_{CC}	V_{CC} Power Supply Voltage	5V±5%		5V±10%
V_{PP}	V_{PP} Power Supply Voltage	V_{CC}-0.6V ~ V_{CC}+0.6V		V_{CC}-0.6V ~ V_{CC}+0.6V

D.C. and OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ~ V_{CC}		-	-	±10	μA
I_{CC01}	Operating Current	$\overline{CE}$=0V	t_{cycle}=150ns	-	-	40	mA
I_{CC02}		I_{OUT}=0mA	t_{cycle}=1μs	-	-	20	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{IH}	Input High Voltage	-		2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-		-0.3	-	0.8	V
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ~ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TC571024D-15		TC571024D-200/-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	-	150	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	-	150	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	-	70	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	60	
t_{OH}	Output Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

Output Load : 1 TTL Gate and C_L=100pF

Input Pulse Rise and Fall Times : 10ns Max.

Input Pulse Levels : 0.45V to 2.4V

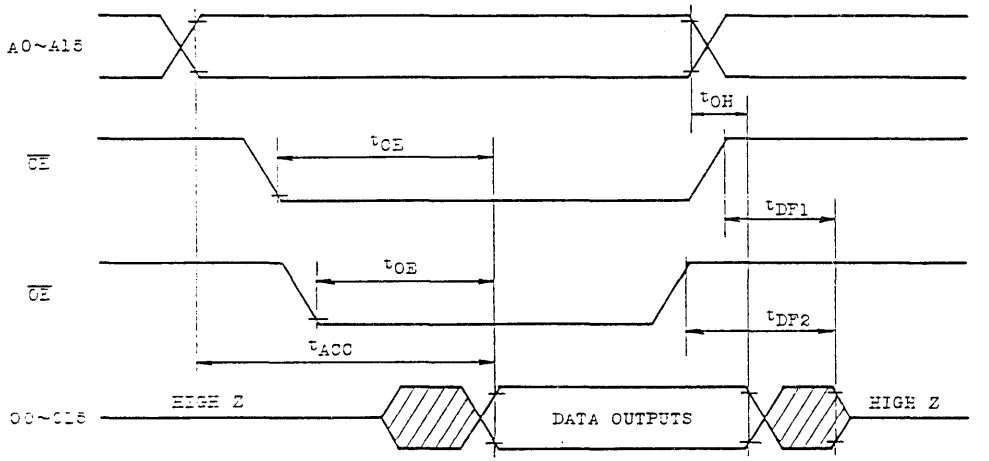
Timing Measurement Reference Level: Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	100	mA

A.C. PROGRAMMING CHARACTERISTICS (T_a=25±5°C, V_{CC}=6.25±0.25V, V_{PP}=12.75±0.25V)

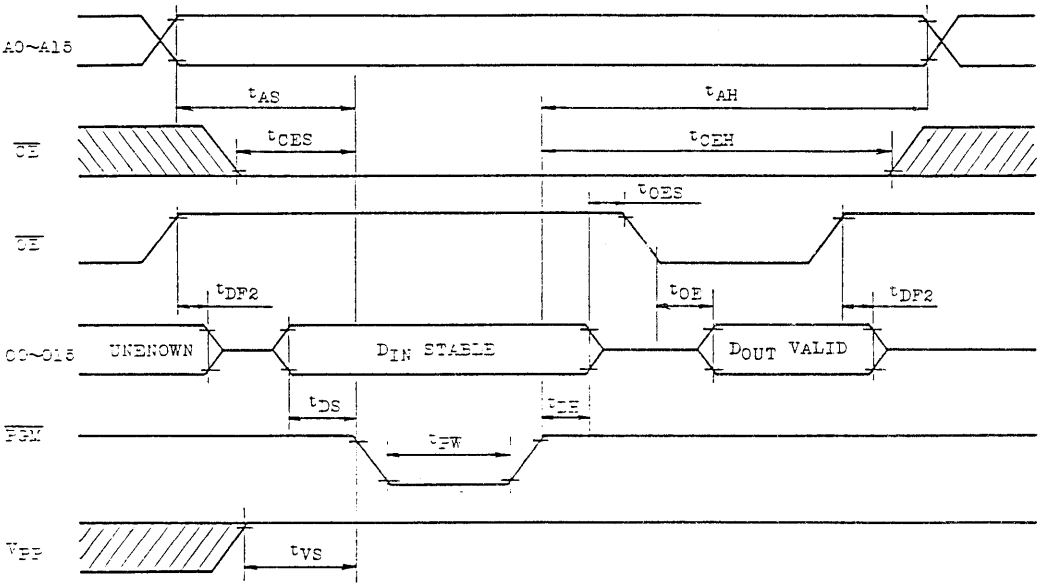
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
T_{PW}	Program Pulse Width	-	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid		-	-	500	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	-	-	150	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2.0	-	-	μs

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level: Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

TIMING CHART



Note: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with Vpp=12.75V may cause permanent damage to the device.

3. The Vpp supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the Vpp terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 14V.

ERASURE CHARACTERISTICS

The TC571024D erasure is achieved by applying shortwave ultraviolet light which has a wavelength of 2537Å (Angstroms) to the chip through the transparent window. Then integrated dose (Ultraviolet light intensity [W/cm^2] × exposure time [sec.]) for erasure should be a minimum of 15 [$W \cdot sec/cm^2$].

When the Toshiba sterilizing lamp GL-15 is used and the device is exposed at a distance of 1cm from the lamp surface, the erasure will be achieved within 60 minutes. And using commercial lamps whose ultraviolet light intensity is a 12000 [$\mu W/cm^2$] will reduce the exposure time to about 20 minutes. (In this case, the integrated dose is 12000 [$\mu W/cm^2$] × (20 × 60) [sec] ≅ 15 [$W \cdot sec/cm^2$].)

The TC571024D erasure begins to occur when exposed to light with wavelength shorter than 4000Å. The sunlight and the flourescent lamps will include 3000 ∿ 4000Å wavelength components. Therefore when used under such lighting for extended periods of time, the opeque seals - Toshiba EPROM Protect Seal AC901 - are available.

OPERATION INFORMATION

The TC571024D six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

	PIN / MODE	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	D0 ∿ D15	POWER
READ OPERATION	Read	L	L	H	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
PROGRAM OPERATION (Ta=25±5°C)	Program	L	*	L	12.75V	6.25V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
		L	H	H				
	Program Verify	L	L	H			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC571024D has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) control the output buffers, independent of device selection.
Assuming in that $\overline{CE}$=$\overline{OE}$=V_{IL} and $\overline{PGM}$=V_{IH}, the output data is valid at the output after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL}, $\overline{PGM}$=V_{IH} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.
So two or more ROMs can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC571024D has a low power standby mode controlled by the $\overline{CE}$ signal.
By applying a high level to the $\overline{CE}$ input, the TC571024D is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC571024D are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The levels required for all inputs are TTL. The TC571024D can be programmed any location at anytime——either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

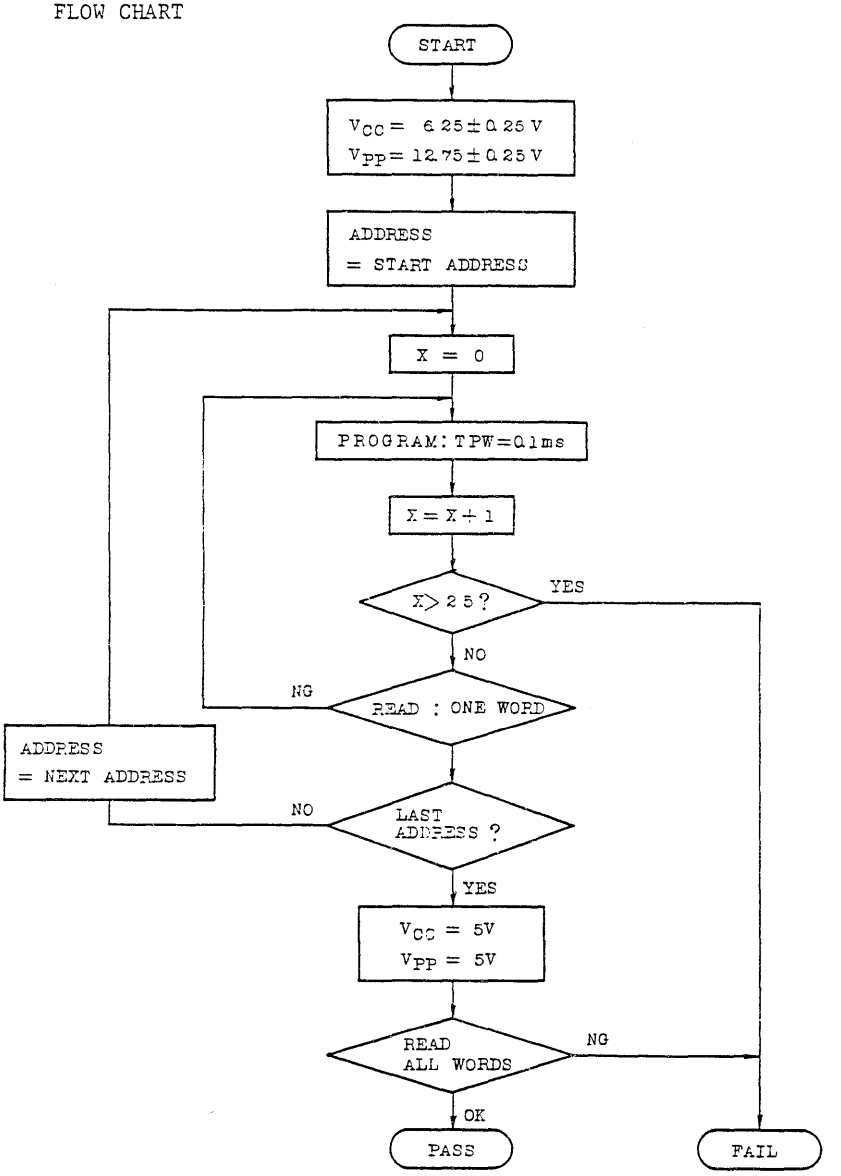
Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC571024D from being programmed.
Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC}=6.25V and $\overline{PGM}$=V_{IH}.
The programming is achieved by applying a single TTL low level 0.1 ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

HIGH SPEED PROGRAM OPERATION

FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC571024D which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC571024D by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of (O_7).

The following table shows electric signature of TC571024D.

PINS / SIGNATURE	A_0	O_{15}	O_{14}	O_{13}	O_{12}	O_{11}	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX. DATA
Manufacture Code	V_{IL}	*	*	*	*	*	*	*	*	1	0	0	1	1	0	0	0	**98
Device Code	V_{IH}	*	*	*	*	*	*	*	*	0	0	0	0	1	0	0	0	**08

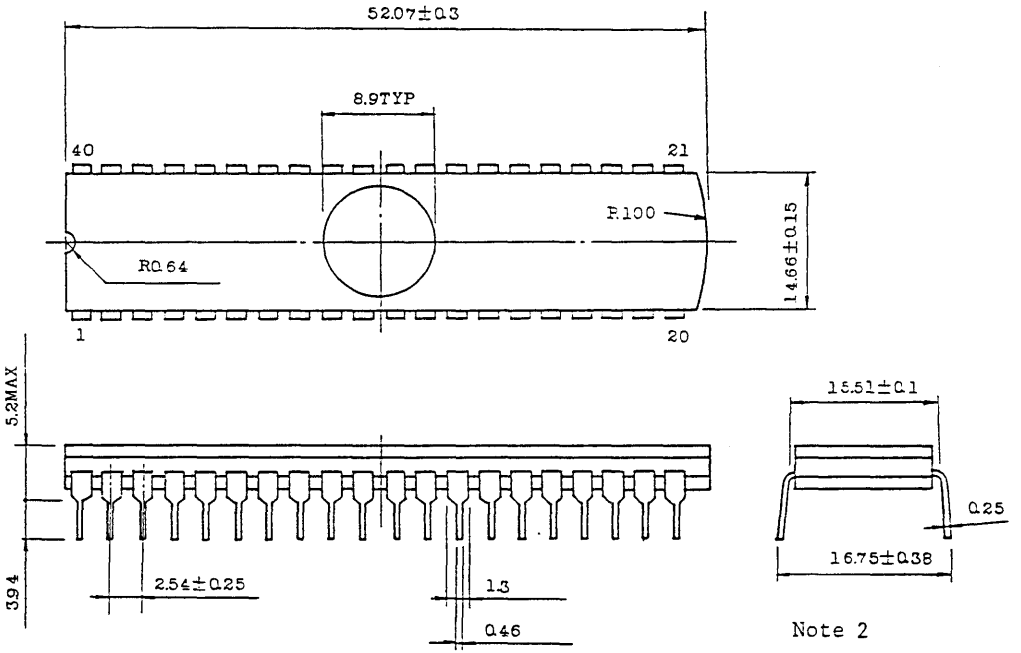
Notes: A9=12V±0.5V, A1 ∿ A8, A10 ∿ A15, $\overline{CE}$, $\overline{OE}$=V_{IL}, $\overline{PGM}$=V_{IH} *: Don't Care

D.C. AND OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{ID}	A9 Auto Select Voltage	11.5	12.0	12.5	V

OUTLINE DRAWINGS

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.40 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

FEEPROM

TOSHIBA MOS MEMORY PRODUCTS

PRELIMINARY

TMM28257P-20, TMM28257P-25
TMM28257P-30

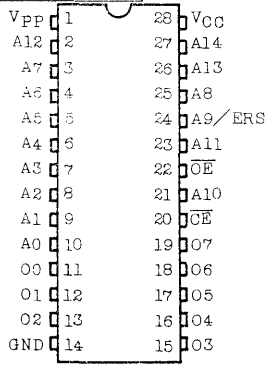
DESCRIPTION

TMM28257P is a 32,768 word × 8 bit electrically chip erasable and programmable read only memory, and molded in a 28 pin standard plastic DIP.
The TMM28257P's access time is 200ns/250ns/300ns, and has low power standby mode which reduces the power dissipation without increasing access time.
The electrical characteristics are the same as U.V.EPROM TMM27256D's. For program operation, the programming is achieved by using the high speed programming mode.
The TMM28257P has an electrically chip erasing mode which can erase whole bits at the same time.

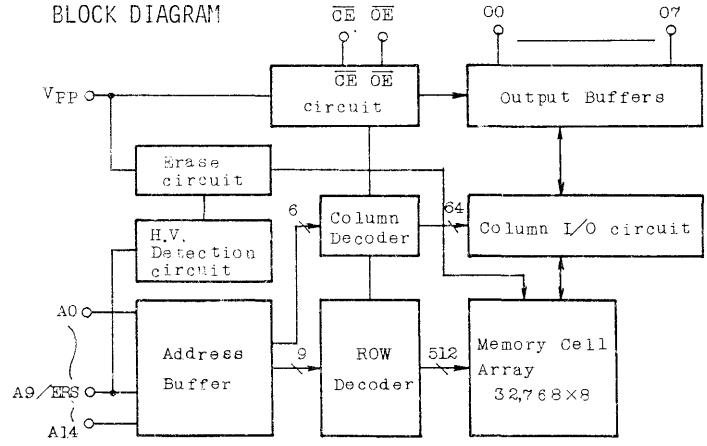
FEATURES

- Fast access time: TMM28257P-20 200ns
  TMM28257P-25 250ns
  TMM28257P-30 300ns
- Low power dissipation
  Active : 100mA
  Standby: 25mA
- Full static operation
- High speed programming mode
- Electrically chip erasing mode
- Inputs and outputs TTL compatible
- Pin compatible with MASK ROM TC53257P, TMM23256P, EPROM TMM27256D and TC57256D
- Standard 28 pin DIP plastic package

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0~A14	Address Inputs
O0 ~ O7	Output(Input)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
A9/ERS	Address And Erase Control Input
V_{PP}	Program And Erase Power Supply Voltage
V_{CC}	VCC Power Supply Voltage
GND	Ground

MODE SELECTION

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	A0~A8 (10~14)	O0 ~ O7	Power
Read	L	L	*	5V	5V	*	Data Out	Active
Output Deselect	*	H	*			*	High Impedance	
Standby	H	*	*			*	High Impedance	Standby
Program	L	H	*	21V	6V	*	Data Input	Active
Program Inhibit	H	*	*			*	High Impedance	
Program Verify	L	L	*			*	Data Out	
Chip Erase	L	H	12V	21V	5V	*	Data FF(H) Input	Active
Chip Erase Inhibit	H	*				*	High Impedance	

*: V_{IH} or V_{IL}

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 22.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ 7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec
T_{STG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	0 ∿ 70	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D.C. AND OPERATING CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	-	-	25	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	-	-	100	mA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0 ∿ V_{CC}+0.6	-	-	±2	mA
I_{LO}	Output Leakage Current	V_{OUT}=0.4 ∿ V_{CC}	-	-	±10	μA

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V±5%, V_{PP}=2.0V ∿ V_{CC}+0.6V)

SYMBOL	PARAMETER	TEST CONDITION	-20		-25		-30		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	200	-	250	-	300	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	200	-	250	-	300	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	-	100	-	100	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	0	90	0	90	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	0	90	0	90	ns
t_{OH}	Output Data Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	0	-	0	-	ns

A.C. TEST CONDITIONS

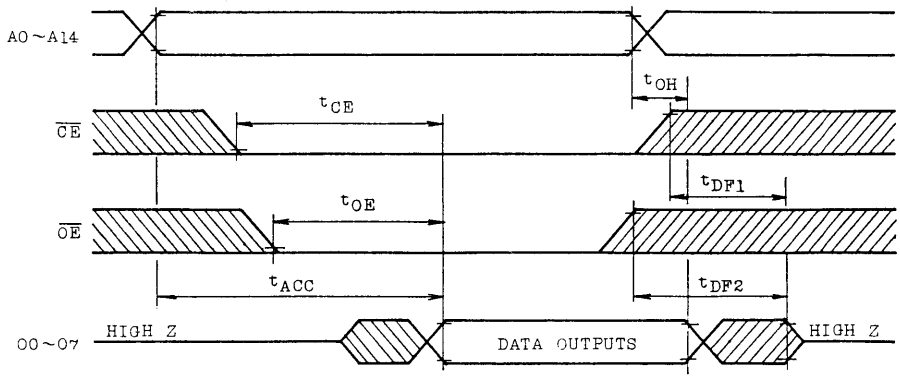
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level: Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE *(Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V

D.C. AND OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=21V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0 \sim V_{CC}$	-	-	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	-	-	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=21.5V$	-	-	30	mA

A.C. PROGRAMMING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{CC}=6V \pm 0.25V$, $V_{PP}=21V \pm 0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$ Hold Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	0.95	1	21	ms
t_{DV}	$\overline{CE}$ to Output Valid	$\overline{OE}=V_{IL}$	-	-	1	μs
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}=V_{IL}$	-	-	150	ns

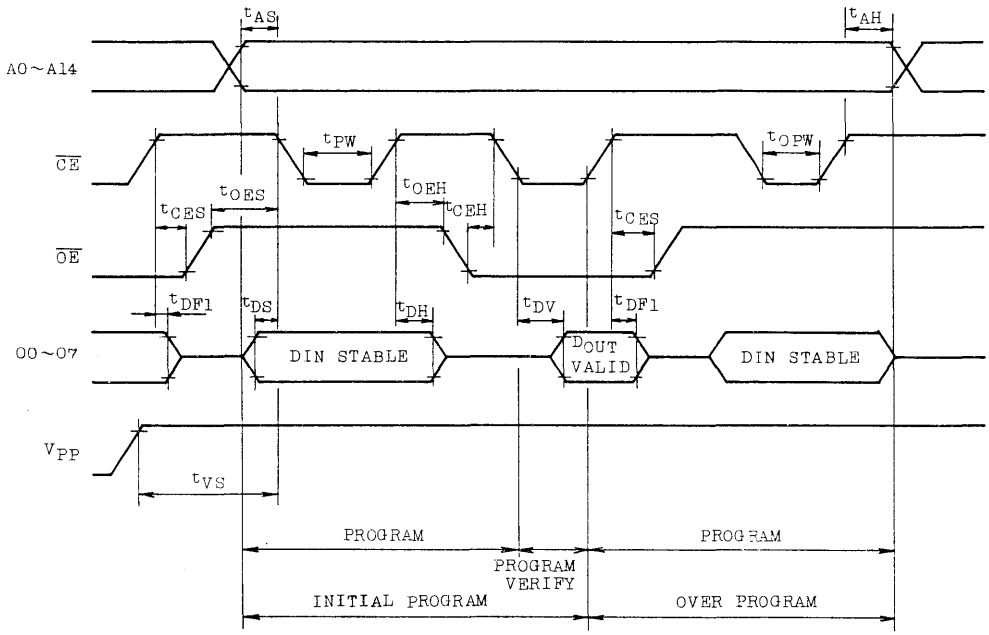
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : $0.45V \sim 2.4V$
- Timing Measurement Reference Level: Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 22V for program operation. So the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 22V.

ERASE OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.0	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	20.5	21.0	21.5	V
V_{IHH}	Input High Voltage H	11.5	12.0	12.5	V
N_{EW}	Erase Write Endurance	100			cycles

D.C. AND OPERATING CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V+0.25V,

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
I_{LIE}	A9/ERS Input Current	A9/ERS=0 ∿ V_{IHH}	-	-	±10	μA
I_{CC}	V_{CC} Supply Current	-	-	-	100	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=21.5V	-	-	30	mA

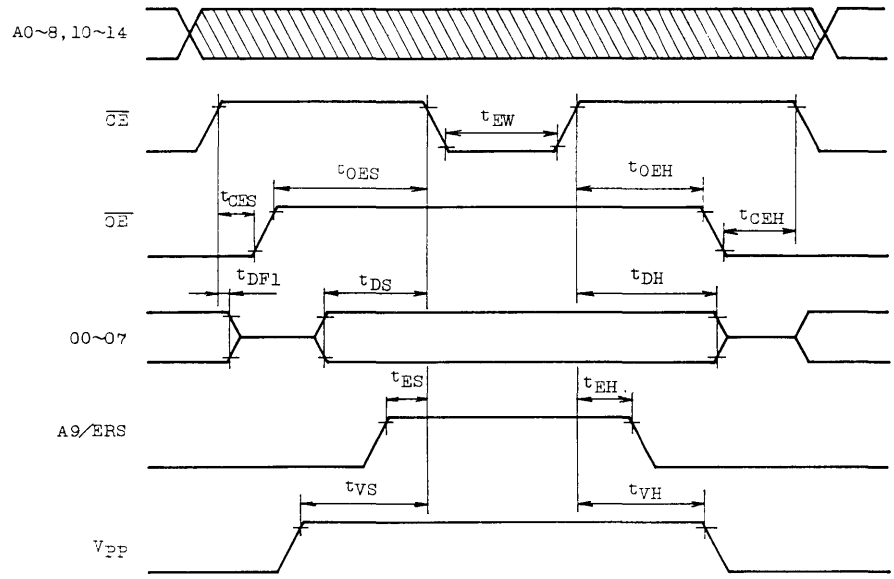
A.C. ERASING CHARACTERISTICS (Ta=0 ∿ 70°C, V_{CC}=5V+0.25V, V_{PP}=21V+0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{CES}	$\overline{CE}$ Setup Time	-	2	-	-	μs
t_{CEH}	$\overline{CE}$ Hold Time	-	2	-	-	μs
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{OEH}	$\overline{OE}$ Hold Time	-	500	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	500	-	-	μs
t_{VS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VH}	V_{PP} Hold Time	-	500	-	-	μs
t_{ES}	A9/ERS Setup Time	-	2	-	-	μs
t_{EH}	A9/ERS Hold Time	-	2	-	-	μs
t_{EW}	Erase Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, A9=V_{IHH}	950	1000	1050	ms
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	-	-	150	ns

Input Pulse Rise and Fall Time: 10ns Max.
Input Pulse Levels: 0.45V ∿ 2.4V

TIMING WAVEFORMS (ERASE)

(V_{CC}=5V±0.25V, V_{PP}=21V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after Vpp.

2. Removing the device from socket and setting the device in socket with V_{PP}=21V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 22V for erase operation. So the voltage over 22V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the Vpp terminal, the overshoot voltage of its pulse should not be exceeded 22V.

Mode \ Pin		$\overline{CE}$	$\overline{OE}$	A9	V_{PP}	V_{CC}	O0 ∿ 7	Power
Read Operation	Read	L	L	*	5V	5V	Data Out	Active
	Output Deselect	*	H	*			High Impedance	
	Standby	H	*	*			High Impedance	Standby
Program Operation	Program	L	H	*	21V	6V	Data In	Active
	Program Inhibit	H	*	*			High Impedance	
	Program Verify	L	L	*			Data Out	
Erase Operation	Erase	L	H	12V	21V	5V	Data FF(H) Input	Active
	Erase Inhibit	H	*				High Impedance	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TMM28257P has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state.

So two or more TMM28257P's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM28257P has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM28257P is placed in the standby mode which reduce the operating current to 25mA from 100mA (about 75% reduction) by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM28257P are in the "1" state which is erased state.

Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The TMM28257P is in the programming mode when the V_{PP} input is at 21V and $\overline{CE}$ is at TTL-Low under $\overline{OE}=V_{IH}$.

The TMM28257P can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+21V) is applied to V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TMM28257P from being programmed.

Programming of two or more TMM28257P's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+21V) is applied to the V_{PP} terminal with $V_{CC}=6V$.

The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 20 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.
This high speed program algorithm allows the programming of the TMM28257P to be accomplished without one and a half minutes (Typ.).

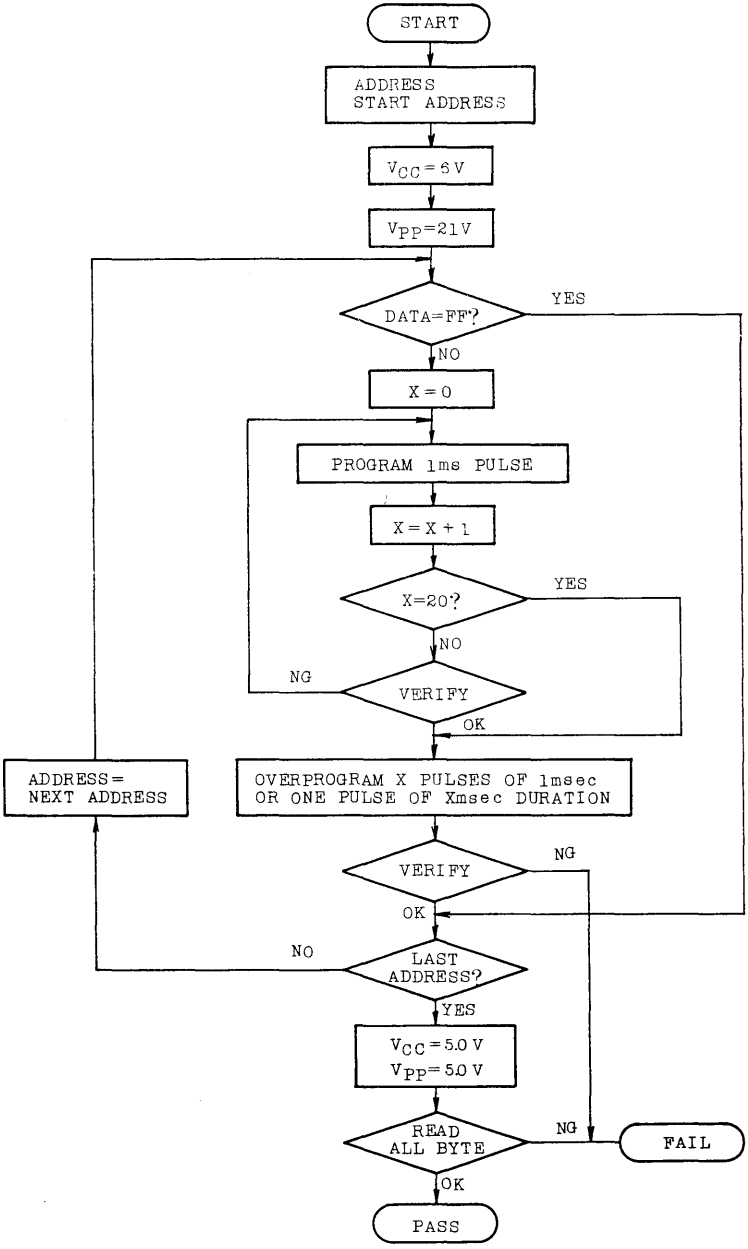
CHIP ERASE MODE

The TMM28257P is in chip erase mode when the V_{PP} input is 21V and $\overline{CE}$ is at TTL-Low level under the condition of A9=12V, $\overline{OE}=V_{IH}$ and Data inputs=V_{IH}. The chip erase pulse width is only 1 sec.
Once chip is erased, all bits of the device are in "1" state.

ERASE INHIBIT

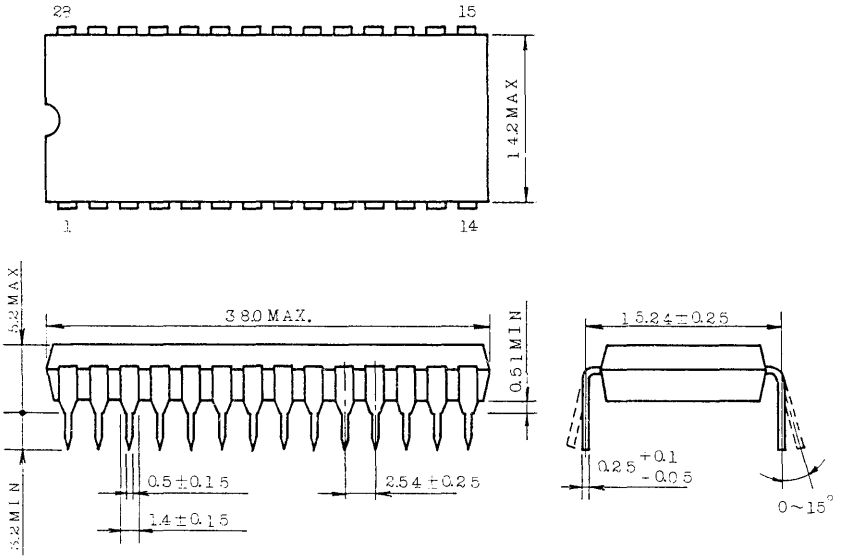
Under the condition that the erase voltage (21V) is applied to V_{PP} terminal and 12V is to A9 input, TTL-High level $\overline{CE}$ input inhibits the TMM28257P from being erased.

HIGH SPEED PROGRAM MODE FLOW CHART



OUTLINE DRAWINGS (TMM28257P)

Unit in mm



Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OTP

HIGH SPEED PROGRAMMING MODE

FEATURES

The High Speed Programming I or High Speed Programming II Algorithms may be used to program 64K through 512K devices. The 1MEGABIT devices may be programmed using the High Speed Programming II Algorithm.

The High Speed Programming I Algorithm uses 1ms programming pulse and the flow chart is shown in Figure 1.

The High Speed Programming II Algorithm uses 0.1ms programming pulse and the flow chart is shown in Figure 2.

APPLICABLE DEVICES

Device Name		Theoretical Programming Time	
EPROM	One Time PROM	I	II
TMM2764AD/ADI	TMM2464AP/AF	33 sec	0.8 sec
TMM27128AD/ADI	TMM24128AP/AF	66 sec	1.7 sec
TMM27256AD/ADI/BD/BDI	TMM24256AP/AF/BP/BF	131 sec	3.3 sec
TC57256AD	TC54256AP/AF	131 sec	3.3 sec
TMM27512D/DI/AD/ADI	TMM24512P/F/AP/AF	262 sec	7.0 sec
TC571000D	TC541000P	N/A	14 sec
TC571001D	TC541001P	N/A	14 sec

IDENTIFICATION MODE

The identification mode allows the reading of an electrical signature from the device that will identify the manufacturer and device type. The identification mode is activated using the following conditions:

1. For the Manufacturer Code:
   Set A9=12V±0.5V, Aϕ=ViL, Other Addresses=ViL
   Note: The manufacturer code is consistent with the E.I.A. standard.
2. For the Device Code:
   Set A9=12V±0.5V, Aϕ=ViH, Other Addresses=ViL.
   Note: The Device Code is manufacturer dependent.

The following table shows the Electrical Signatures of Toshiba devices.

ELECTRICAL DEVICES

Device Name		Signature	
EPROM	One Time PROM	Manufacture Code	Device Code
TMM2764AD/ADI	TMM2464AP/AF	98	52
TMM27128AD/ADI	TMM24128AP/AF	98	D3
TMM27256AD/ADI/BD/BDI	TMM24256AP/AF/BP/BF	98	54
TC57256AD	TC54256AP/AF	98	C4
TMM27512D/DI/AD/ADI	TMM24512P/F/AP/AF	98	15
TC571000D	TC541000P	98	86
TC571001D	TC541001P	98	07

Figure 1

HIGH SPEED PROGRAM I FLOW CHART

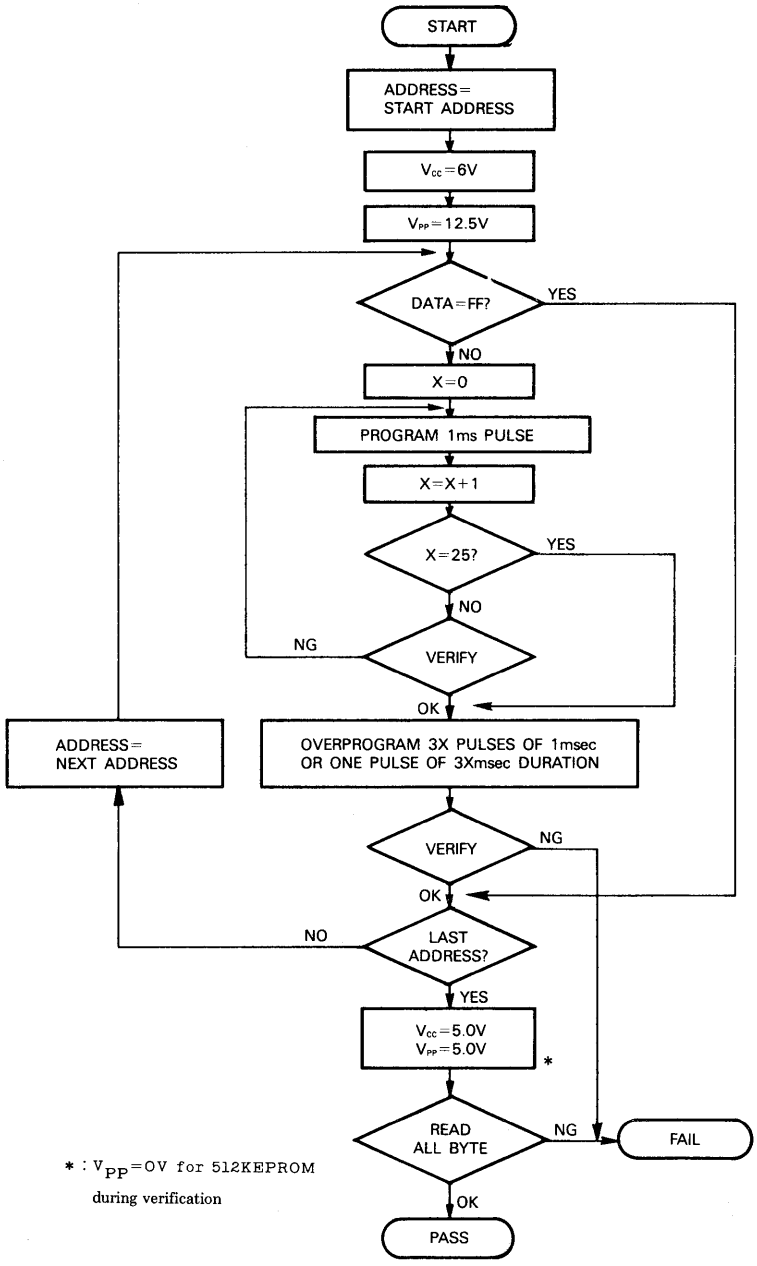
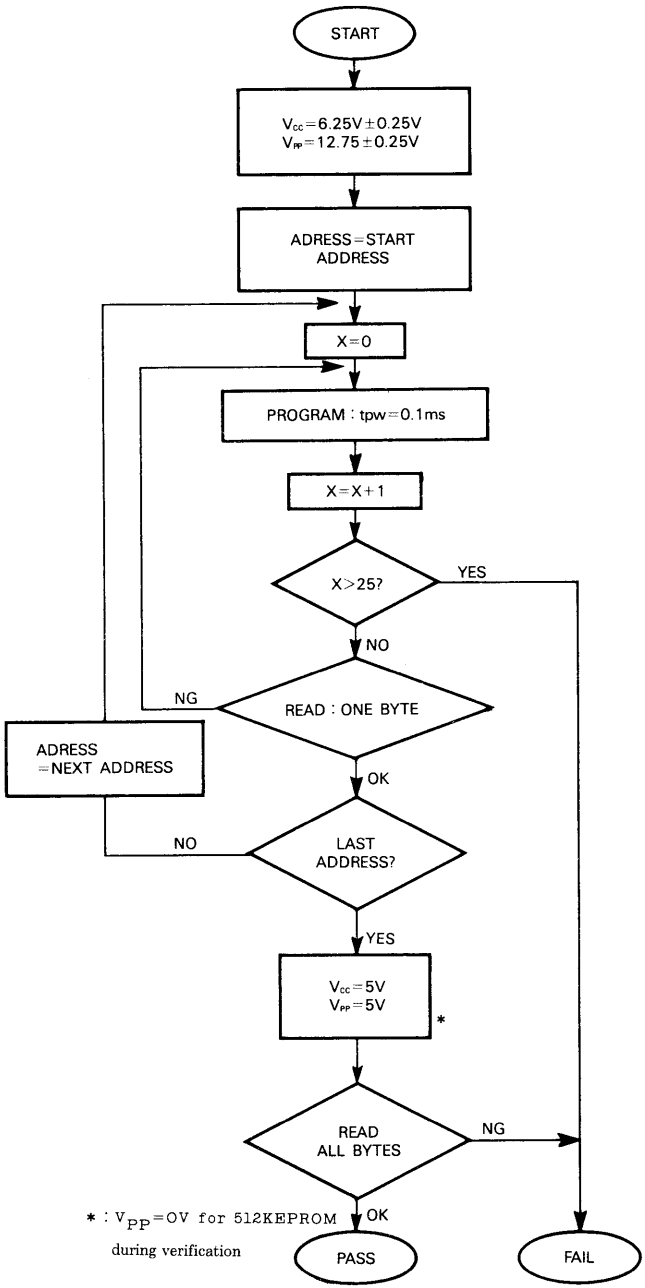


Figure 2

HIGH SPEED PROGRAM II FLOW CHART



TOSHIBA MOS MEMORY PRODUCTS

TMM2464AP/AF 8,192 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
N CHANNEL SILICON STACKED GATE MOS

TMM2464AP/AF

DESCRIPTION

The TMM2464AP/AF is a 8,192 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP.

The TMM2464AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.

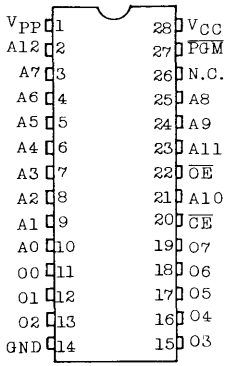
The electrical characteristics and programming method are the same as U. V. EPROM TMM-2764AD's.

Once programed, the TMM2464AP/AF can not be erased because of using plastic DIP without transparent window.

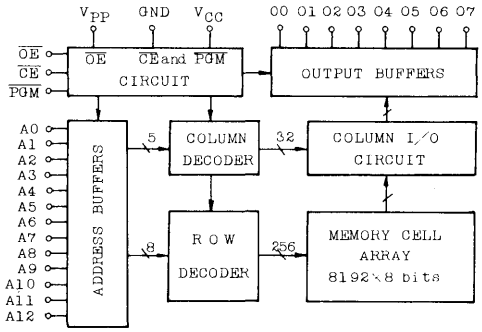
FEATURES

- Single 5 volt power supply
- Fast access time: 200ns (Max.)
- Power dissipation : 100mA(active current) Max.
  : 30mA(standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Full static operation
- High speed programming mode
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM2764AD and ROM TMM2365P, TC5365P.
- 28 PIN standard plastic package: TMM2464AP
- 28 PIN flat package : TMM2464AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{12}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
N.C.	No Connection
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STRG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	2.2	V_{CC}	V_{CC}+0.6	

D. C. and OPERATING CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

(Ta = 0 ~ 70 C, V_{CC} = 5V ± 5%, V_{PP} = 2.0V ~ V_{CC} + 0.6V, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	—	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	—	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	—	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	—	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	—	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

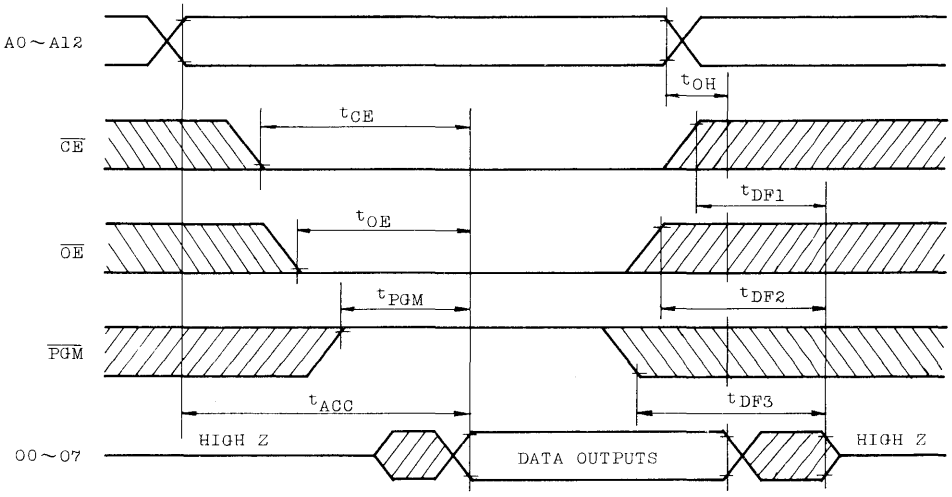
CAPACITANCE

* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	—	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5$ C, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

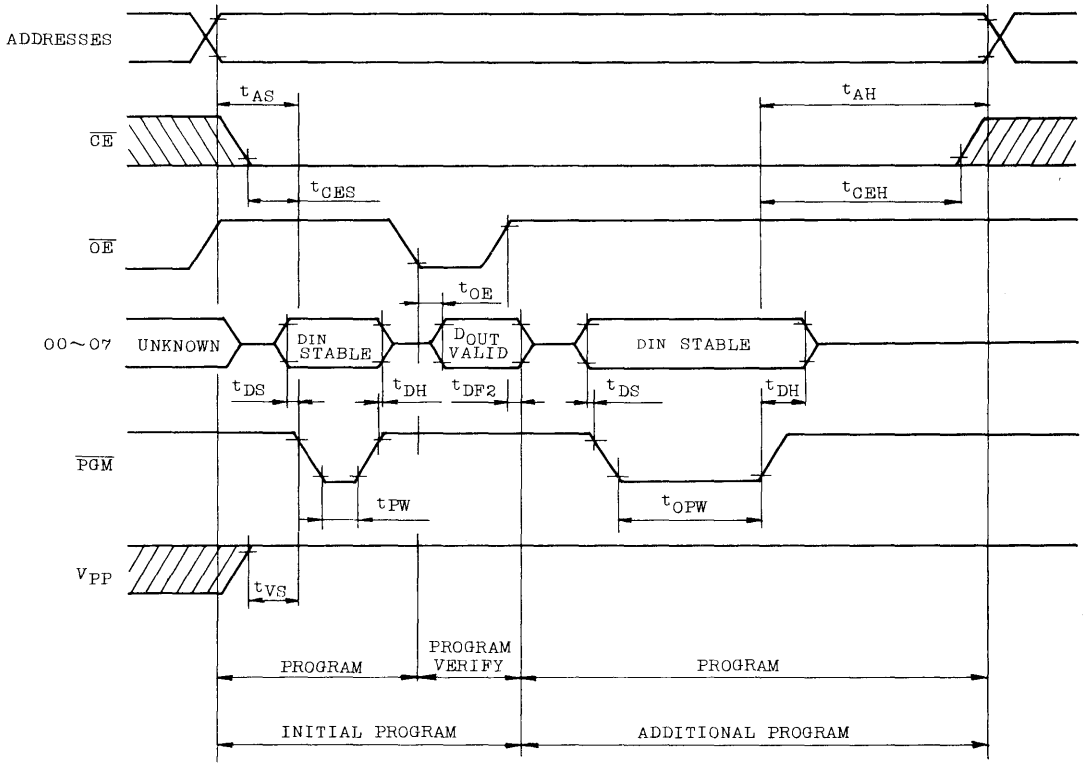
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_l (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. t_{OPW} depend on the program pulse width which is reguired in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.
2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.
3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM2464AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs. In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES(NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM2464AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the outpus after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM2464AP/AF can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM2464AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a TTL high level to the $\overline{CE}$ input, the TMM2464AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM2464AP/AF from being programmed. Programming of two or more TMM2464AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}. The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

The High Speed Program II Algorithm (shown in figure 2, page I-5) may also be used to reduce the programming time further.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM2464AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM2464AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

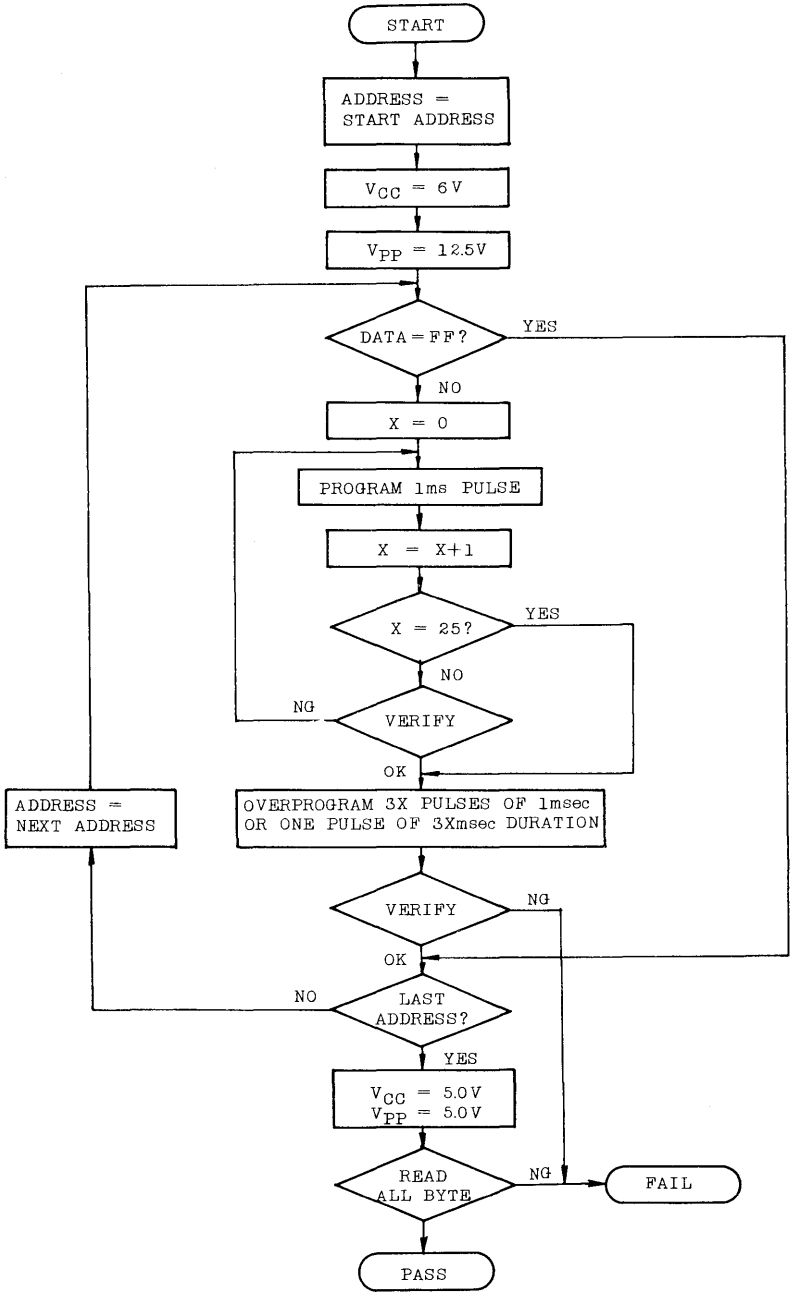
Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

The following table shows electric signature of TMM2464AP/AF

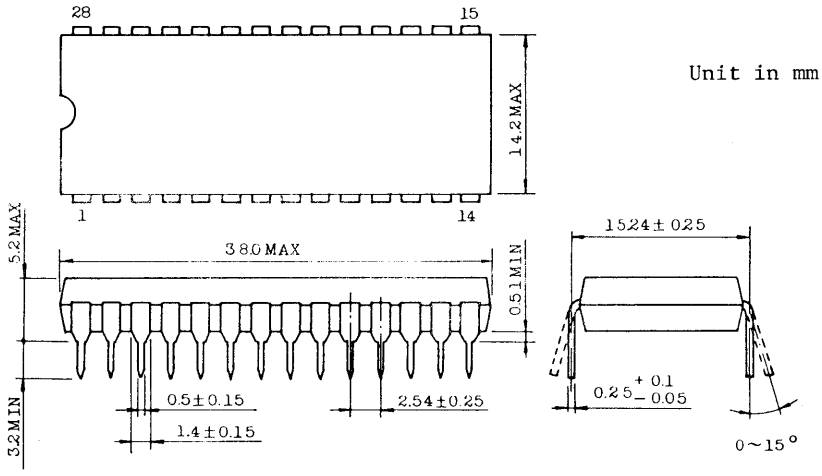
PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	0	1	0	52

Notes: A9=12V±0.5V
A1~A8, A10~A12, $\overline{CE}$, $\overline{OE}$=V_{IL} $\overline{PGM}$=V_{IH}

HIGH SPEED PROGRAM MODE FLOW CHART



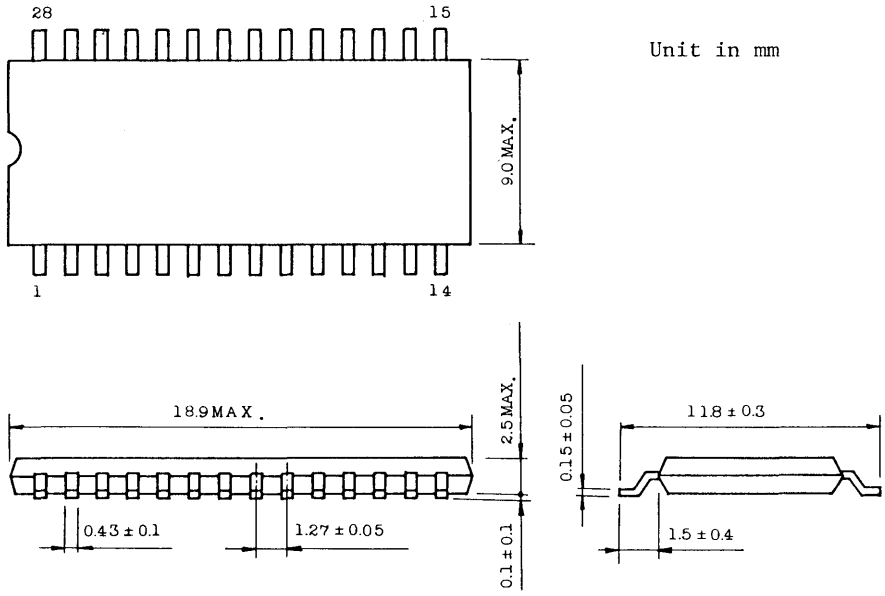
OUTLINE DRAWINGS (TMM2464AP)



Unit in mm

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal positson with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM2464AF)



Note : Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TMM24128AP/AF 16,384 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
N CHANNEL SILICON STACKED GATE MOS

TMM24128AP/AF

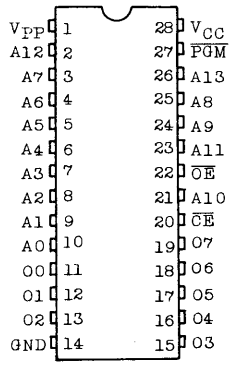
DESCRIPTION

The TMM24128AP/AF is a 16,384 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic DIP. TMM24128AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27128AD's. Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

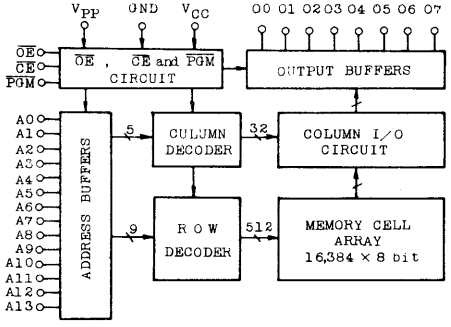
FEATURES

- Single 5 volt power supply
- Fast access time : 200ns(Max.)
- Power dissipation : 100mA(active current) Max.
  30mA(standby current) Max.
- Low power standby mode : $\overline{CE}$
- Output buffer control : $\overline{OE}$
- Full static operation
- High speed programming mode
- Single location programming
- Three state outputs
- Inputs and outputs TTL compatible
- Compatible with TMM27128AD and MASK ROM TMM23128P
- 28 PIN standard plastic package: TMM24128AP
- 28 PIN flat package : TMM24128AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{13}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	*	12.5V	6V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
$T_{STRG.}$	Storage Temperature	−55~150	°C
$T_{OPR.}$	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS

(Ta=0~70°C, V_{CC}=5V±5%, Unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	−	−	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	−	−	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	−	−	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	−	−	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	−	−	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	−	−	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	−	−	±10	μA

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 2.0V \sim V_{CC} + 0.6V$, Unless otherwise noted)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	–	70	ns
t_{PGM}	$\overline{PGM}$ to Output Valid	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	ns
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	ns
t_{OH}	Output Data Hold Time	0	–	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

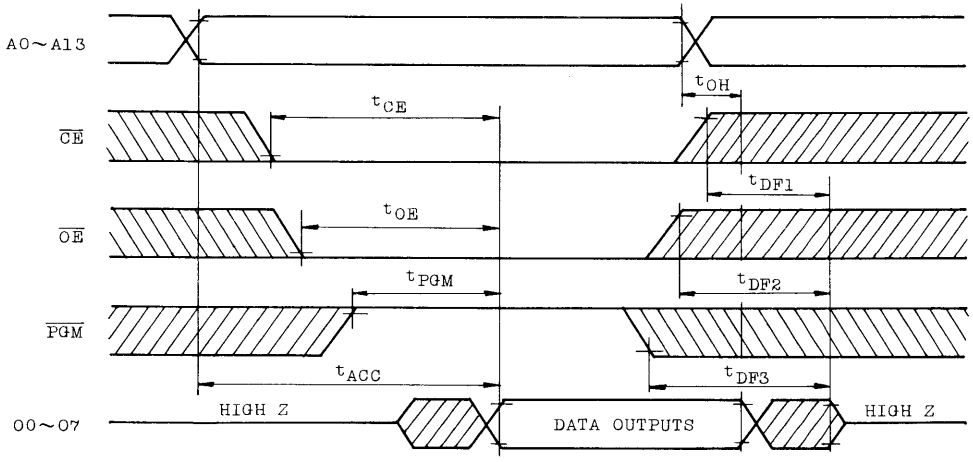
CAPACITANCE

* ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	100	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

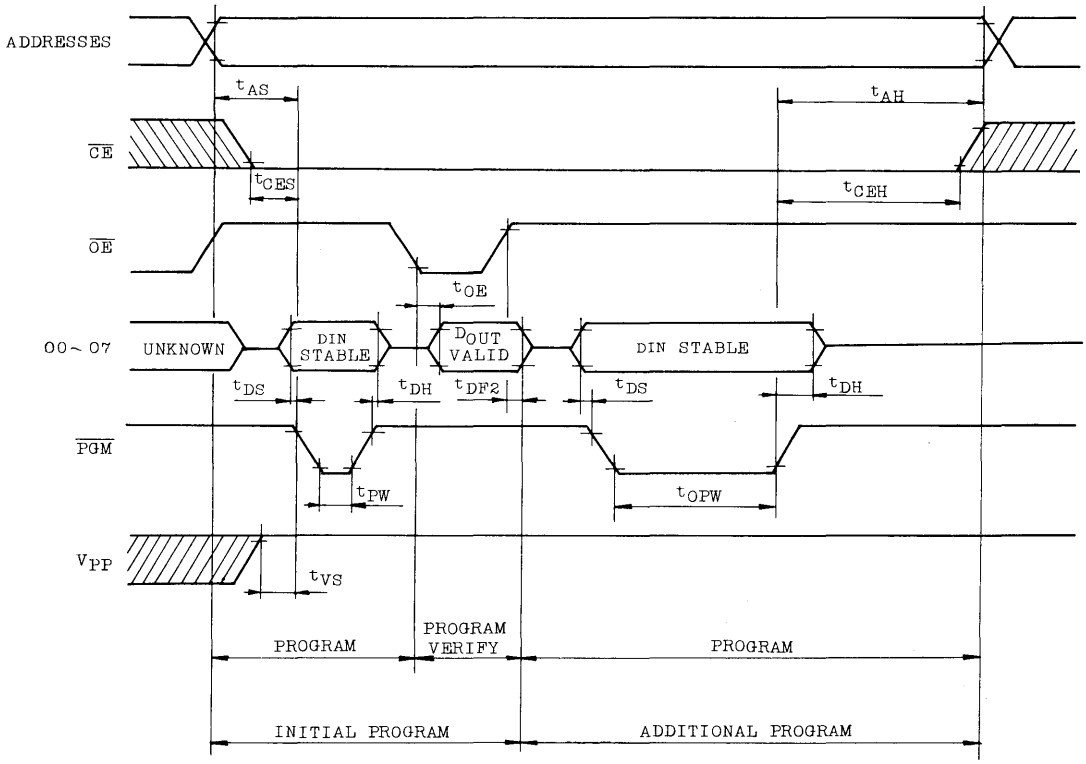
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	2	—	—	μs
t_{CEH}	$\overline{CE}$ Hold Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VS}	V_{PP} Setup Time	—	2	—	—	μs
t_{PW}	Program Pulse Width	—	0.95	1.0	1.05	ms
t_{OPW}	Additional Program Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	—	—	—	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IL}$	—	—	90	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note : 1. t_{OPW} depend on the program pulse width which is reguired in the initial program.

TIMING WAVEFORMS (HIGH SPEED PROGMAM)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24128AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

In the read operation mode, a single 5V power supply is required and the levels required for all inputs are TTL.

MODE \ PIN NAMES(NUMBER)		$\overline{PGM}$ (27)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	Active
	Standby	*	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	L	*	12.5V	6V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	Active
		H	L	H			High Impedance	Active
	Program Verify	H	L	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24128AP/AF has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming that $\overline{CE}=\overline{OE}=V_{LL}$ and $\overline{PGM}=V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{LL}$, $\overline{PGM}=V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

And assuming that $\overline{CE}=\overline{OE}=V_{IL}$ and addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM24128AP/AF can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24128AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying TTL high level to the $\overline{CE}$ input, the TMM24128AP/AF is placed in the standby mode which reduce the operating current from 100mA to 30mA, and then the outputs are in a high impedance state, independent of the $\overline{OE}$ and the $\overline{PGM}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TMM24128AP/AF from being programmed. Programming of two or more TMM24128AP/AF in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V and $\overline{PGM}$=V_{IH}. The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

The High Speed Program II Algorithm (shown in figure 2, page I-5) may also be used to reduce the programming time further.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24128AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24128AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

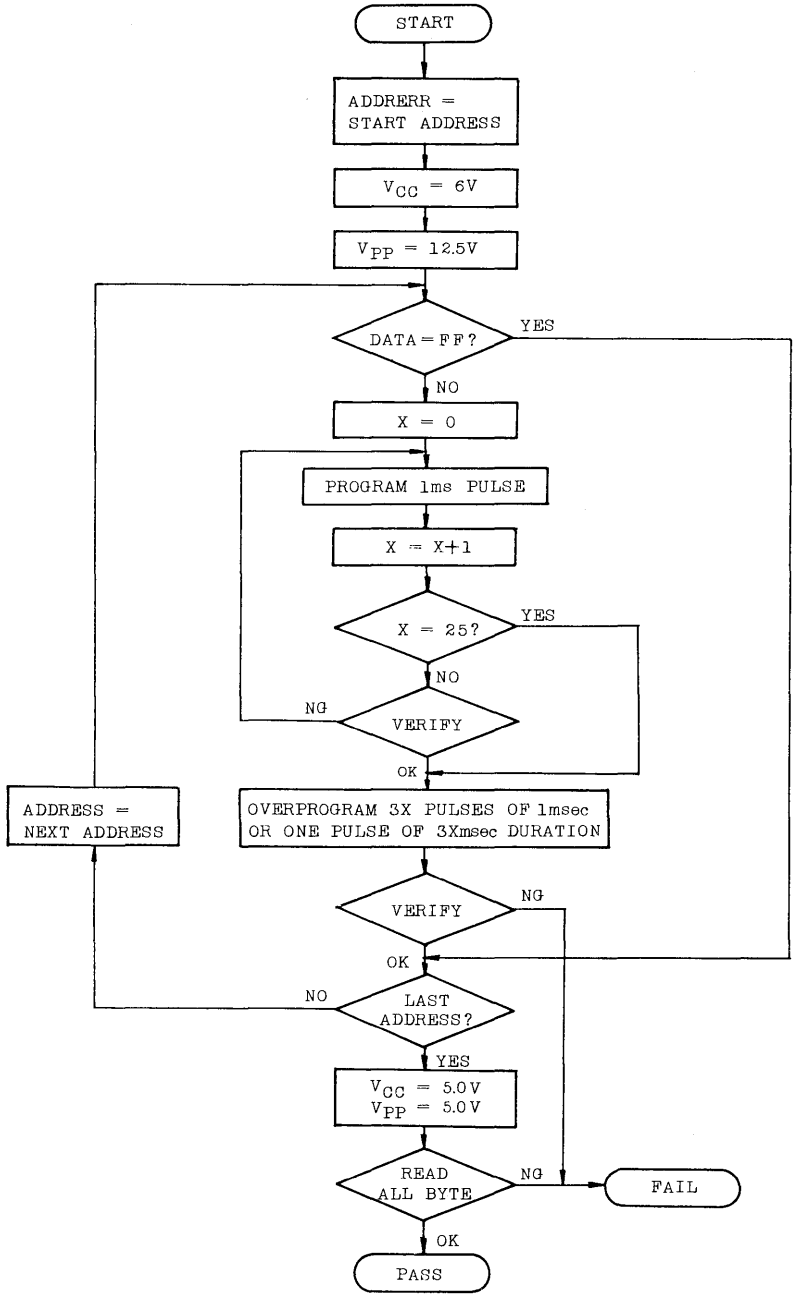
The following table shows electric signature of TMM24128AP/AF.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	1	0	0	1	1	D3

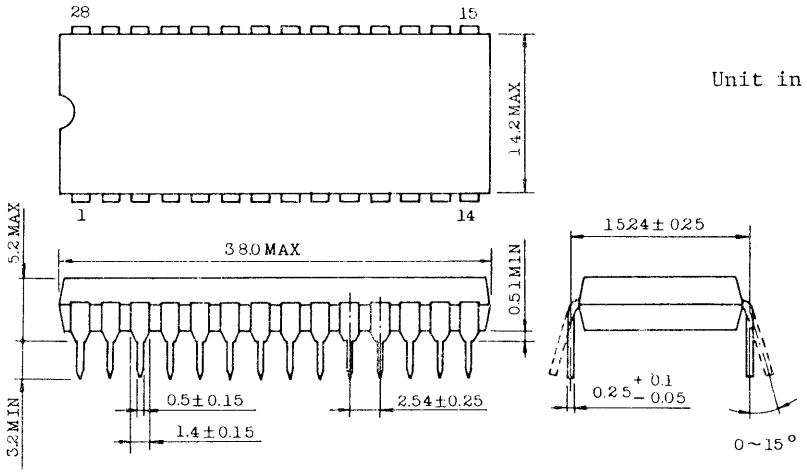
Notes: A9=12V±0.5V

A1~A8, A10~A13, $\overline{CE}$, $\overline{OE}$=V_{IL} $\overline{PGM}$=V_{IH}

HIGH SPEED PROGRAM MODE FLOW CHART



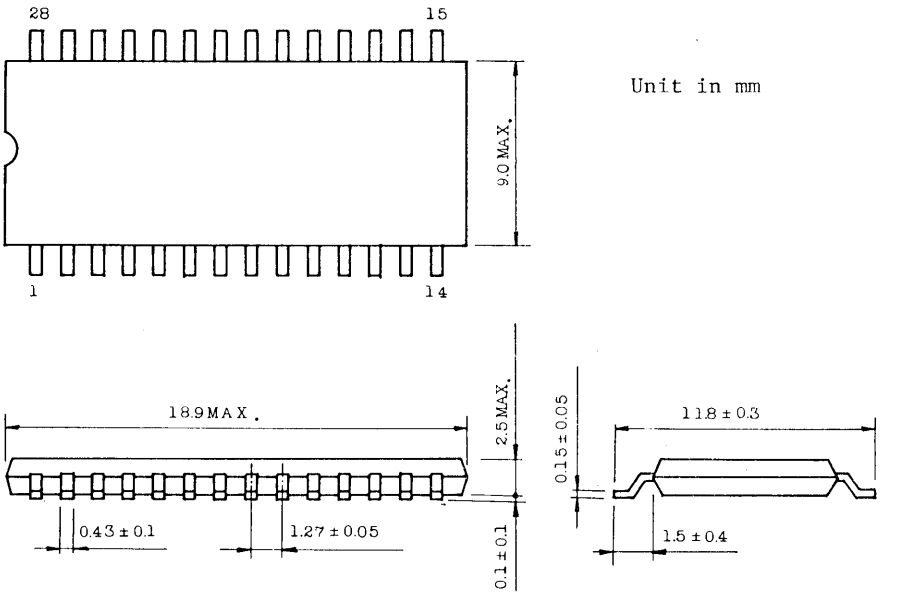
OUTLINE DRAWINGS (TMM24128AP)



Unit in mm

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24128AF)



Note: Lead picth is 1.27 and tolerance is±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TMM24256AP/AF 32,763 WORD × 8 BIT
ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24256AP/AF

DESCRIPTION

The TMM24256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic Package.

The TMM24256AP/AF's access time is 200ns and has low power standby mode which reduces the power dissipation without increasing access time.

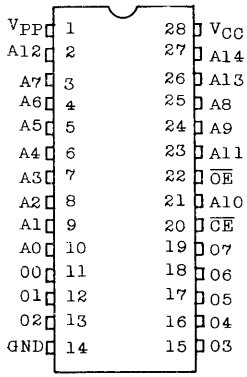
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256AD's.

Once programed, the TMM24128AP/AF can not be erased because of using plastic DIP without transparent window.

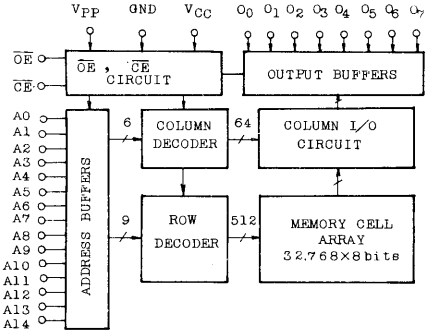
FEATURES

- Fast access time : 200ns
- Low power dissipation
  Active : 100mA
  Standby : 30mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD and TC57256D
- Standard 28 pin DIP plastic package : TMM24256AP
- Plastic Flat Package : TMM24256AF

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	V_{CC} Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	V_{CC} Power Supply Voltage	−0.6~7.0	V
V_{PP}	Program Supply Voltage	−0.6~14.0	V
V_{IN}	Input Voltage	−0.6~7.0	V
V_{OUT}	Output Voltage	−0.6~7.0	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C·sec
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	0~70	°C

READ OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	−	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.3	−	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	V
V_{PP}	V_{PP} Power Supply Voltage	2.0	V_{CC}	V_{CC}+0.6	V

D. C. and OPERATING CHARACTERISTICS (Ta=0~70°C, V_{CC}=5V±5%,)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0~V_{CC}	—	—	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE}$=V_{IH}	—	—	30	mA
I_{CC2}	Supply Current (Active)	$\overline{CE}$=V_{IL}	—	—	100	mA
V_{OH}	Output High Voltage	I_{OH}=−400μA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
I_{PP1}	V_{PP} Current	V_{PP}=0~V_{CC}+0.6V	—	—	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V~V_{CC}	—	—	±10	μA

A. C. CHARACTERISTICS

($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 2.0V \sim V_{CC} + 0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	–	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	–	200	ns
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	–	70	ns
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	ns
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	ns

A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and $C_L = 100pF$
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

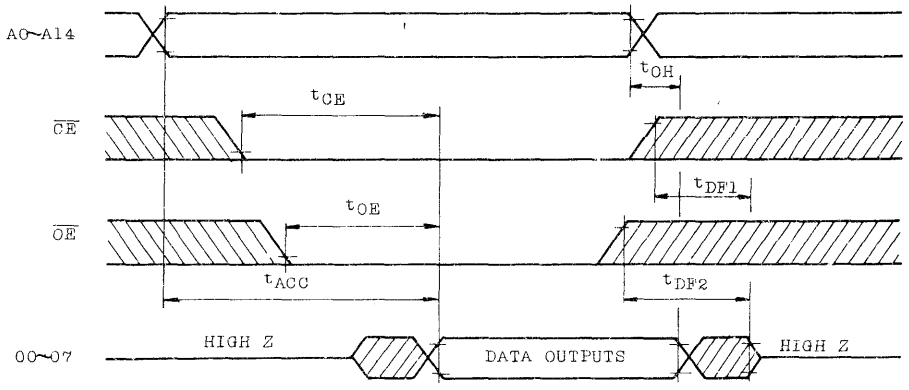
CAPACITANCE

* ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	8	12	pF

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D. C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	—	$V_{CC}+1.0$	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	V
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	V

D. C. and OPERATING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN}=0\sim V_{CC}$	—	—	±10	μA
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4	—	—	V
V_{OL}	Output Low Voltage	$I_{OL}=2.1mA$	—	—	0.4	V
I_{CC}	V_{CC} Supply Current	—	—	—	120	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP}=13.0V$	—	—	50	mA
V_{ID}	A_9 Auto Select Voltage	—	11.5	12.0	12.5	V

A. C. PROGRAMMING CHARACTERISTICS

($Ta=25\pm5°C$, $V_{CC}=6V\pm0.25V$, $V_{PP}=12.5V\pm0.5V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	—	2	—	—	μs
t_{AH}	Address Hold Time	—	2	—	—	μs
t_{CES}	$\overline{CE}$ Setup Time	—	0	—	—	ns
t_{CEH}	$\overline{CE}$ Hold Time	—	0	—	—	ns
t_{OES}	$\overline{OE}$ Setup Time	—	2	—	—	μs
t_{DS}	Data Setup Time	—	2	—	—	μs
t_{DH}	Data Hold Time	—	2	—	—	μs
t_{VPS}	V_{PP} Setup Time	—	2	—	—	μs
t_{VCS}	V_{CC} Setup Time	—	2	—	—	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}=V_{IL}$, $\overline{OE}=V_{IH}$	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}=V_{IH}$	—	—	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}=V_{IH}$	—	—	130	ns

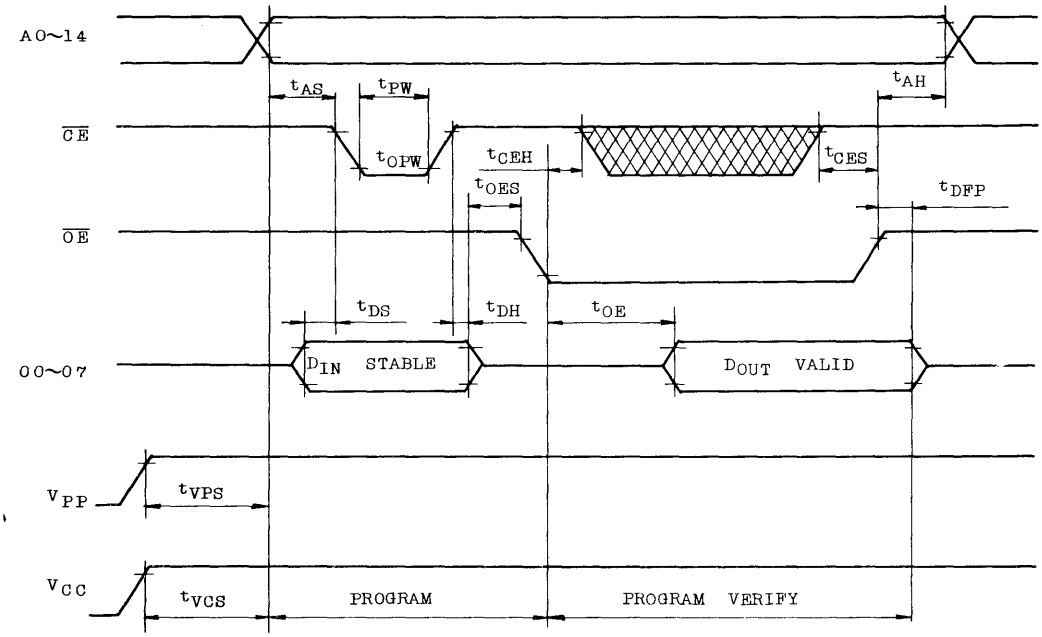
A. C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L(100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V to 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1 : The length of the overprogram pulse may very as a fumction of the counter value X.

TIMING WAVEFORMS(PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note : 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal.
   When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES(NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read Operation (Ta=0~70°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	Active
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	Active
	Program Verify	*	L			Data Out	Active

Note : H ; V_{IH}, L ; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.

The output enable ($\overline{OE}$) control the output buffers, independent of device selection.

Assuming the $\overline{CE}=\overline{OE}=V_{IL}$, the output data is valid at the outputs after address access time from stabilizing of all addresses.

The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE}=V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$, the outputs will be in a high impedance state. So two or more TMM24256AP/AF's can be connected together on a common bus line.

When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24256AP/AF is placed in the standby mode which reduce the operating current to 30mA from 100mA (about 70% reduction) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.

The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24256AP/AF from being programmed.

Programming of two or more TMM24256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC}=6V.

The programming is achieved by applying a single TTL low level 1ms pulse the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

After correctly programming the selected address, the additional program pulse with width equal to that needed for initial programming is applied.

When programming has been completed, the data in all addresses should be verified with V_{CC}=V_{PP}=5V.

The High Speed Program II Algorithm (shown in figure 2, page I-5) may also be used to reduce the programming time further.

ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7).

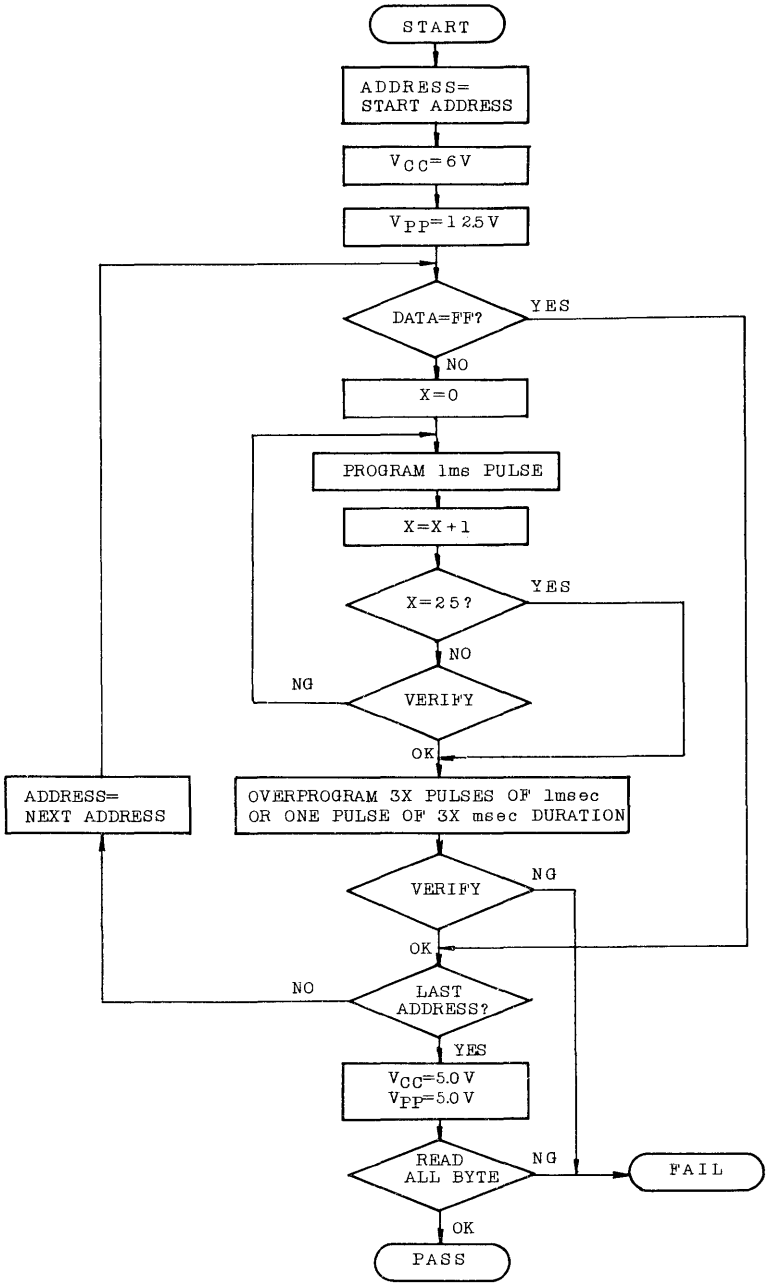
The following table shows electric signature of TMM24256AP/AF.

PINS / SIGNATURE	A_0 (10)	O_7 (19)	O_6 (18)	O_5 (17)	O_4 (16)	O_3 (15)	O_2 (13)	O_1 (12)	O_0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	1	0	1	0	1	0	0	54

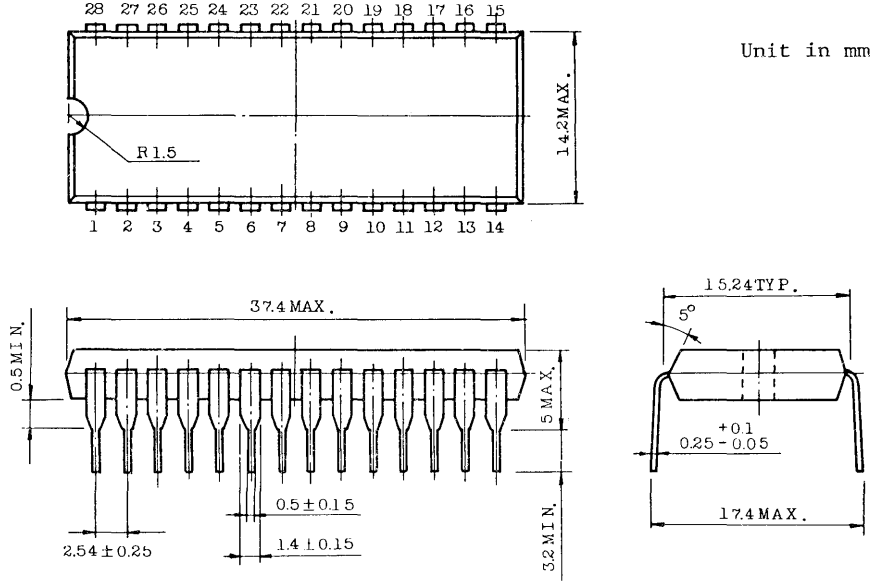
Notes: A9=12V±0.5V

A1~A8, A10~A14, $\overline{CE}$, $\overline{OE}$=V_{IL}

HIGH SPEED PROGRAM MODE FLOW CHART



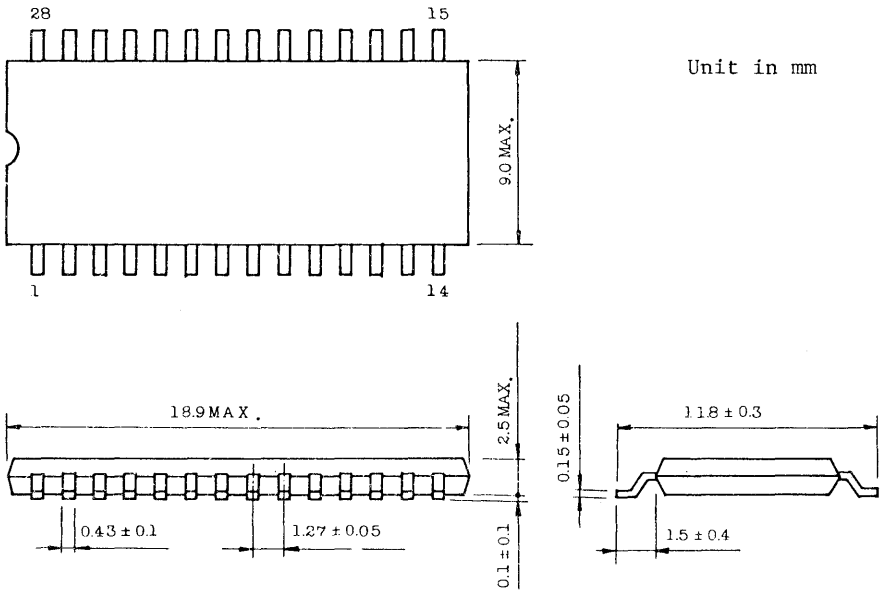
OUTLINE DRAWINGS (TMM24256AP)



Unit in mm

Note : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.
2. This value is measured at the end of leads.
3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24256AF)



Note: Lead picth is 1.27 and tolerance is±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

TMM24256BP/BF 32,763 WORD×8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24256BP/BF-17/20

PRELIMINARY

DESCRIPTION

The TMM24256BP/BF is a 32,768 word x 8 bit one time programmable read only memory and molded in a 28 pin plastic Package.

The TMM24256BP/BF's access time is 170ns/200ns, and has low power standby mode which reduces the power dissipation without increasing access time.

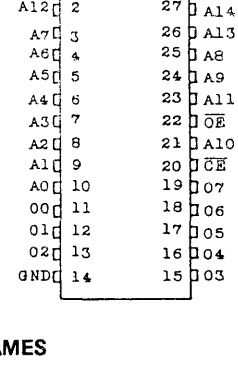
The electrical characteristics and programming method are the same as U.V. EPROM TMM27256BD's.

Once programed, the TMM24256BP/BF can not be erased because of using plastic DIP without transparent window.

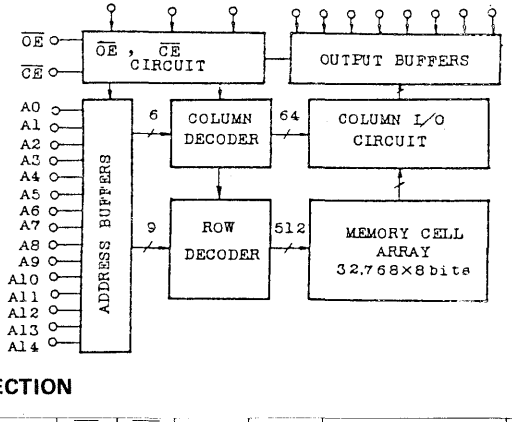
FEATURES

- Fast access time: 170ns, 200ns
- Low power dissipation
  - Active: 100mA
  - Standby: 30mA
- Single 5V power supply
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD/BD and TC57256D/AD
- Standard 28 pin DIP plastic package : TMM24256BP
- Plastic Flat Package : TMM24256BF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A14	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V (1)	V (28)	$O_0 \sim O_7$ (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V[1] 12.75V[2]	6V[1] 6.25V[2]	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

TMM24512P/F 65,536 WORD×8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24512P/F

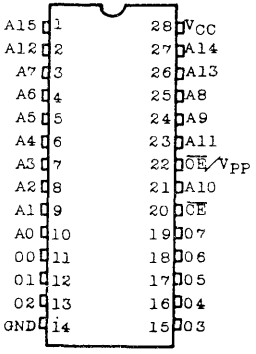
DESCRIPTION

The TMM24512P/F is a 65,536 word x 8 bit one time programmable read only memory, and molded in a 28 pin plastic package. The TMM24512P/F's access time is 250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27512D's. Once programmed, the TMM24512P/F can not be erased because of using plastic DIP without transparent window.

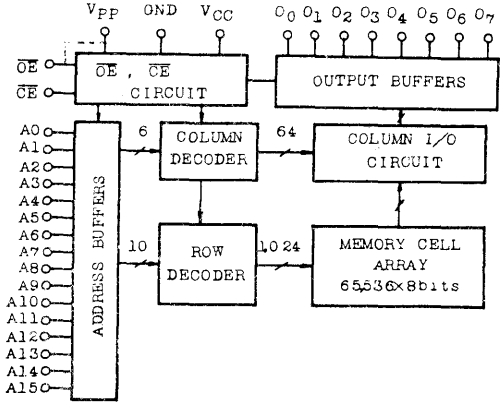
FEATURES

- Fast access time: 250ns
- Low power dissipation
  - Active: 120mA
  - Standby: 35mA
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with TMM27512D
- Standard 28 pin DIP plastic package: TMM24512P
- Plastic Flat Package: TMM24512F

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A15	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$/VPP	Output Enable Input / Program Supply Voltage
VCC	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$/VPP (22)	VCC (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	VPP	6V	Data In	Active
Program Inhibit	H	VPP		High Impedance	
Program Verify	L	L		Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 14.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6 ~ 7.0	V
P_D	Power Dissipation	1.0/0.6*	W
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	0 ~ 70	°C

* : Plastic Flat Package

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	±10	μA
I_{CC1}	Supply Current (Standby)	$\overline{CE} = V_{IH}$	–	–	35	mA
I_{CC2}	Supply Current (Active)	$\overline{CE} = V_{IL}$	–	–	120	mA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = 0 \sim V_{CC} + 0.6V$	–	–	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$	–	–	±10	μA

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 5%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$ = V_{IL}	–	250	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$ = V_{IL}	–	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$ = V_{IL}	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$ = V_{IL}	0	90	
t_{OH}	Output Data in Hold Time	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0	–	

A.C. TEST CONDITIONS

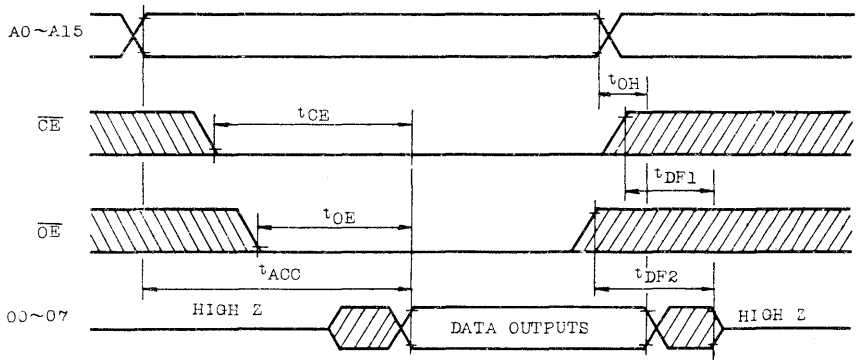
- Output Load : 1 TTL Gate and C_L = 100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.0V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance	V_{IN} = 0V	–	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	V_{IN} = 0V	–	50	60	
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (T_a = 25 ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN} = 0 ~ V_{CC}	–	–	±10	μA
V_{OH}	Output High Voltage	I_{OH} = −400μA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	120	mA
I_{PP2}	V_{PP} Supply Current	V_{PP} = 13.0V	–	–	50	mA

A.C. PROGRAMMING CHARACTERISTICS (T_a = 25 ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{OES}	$\overline{OE}/V_{PP}$ Setup Time	–	2	–	–	μs
t_{OEH}	$\overline{OE}/V_{PP}$ Hold Time	–	2	–	–	μs
t_{PRT}	$\overline{OE}/V_{PP}$ Pulse Rise Time	–	50	–	–	ns
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VR}	$\overline{OE}/V_{PP}$ Recovery Time	–	2	–	–	μs
t_{VCS}	V_{CC} Setup Time	–	2	–	–	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$ = V_{IL}, $\overline{OE}/V_{PP}$ = V_{PP}	0.95	1.0	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3.0	78.75	ms
t_{DV}	Data Valid from $\overline{CE}$	$\overline{OE}/V_{PP}$ = V_{IL}	–	–	1	μs
t_{DF}	$\overline{CE}$ to Output in High-Z	$\overline{OE}/V_{PP}$ = V_{IL}	–	–	130	ns

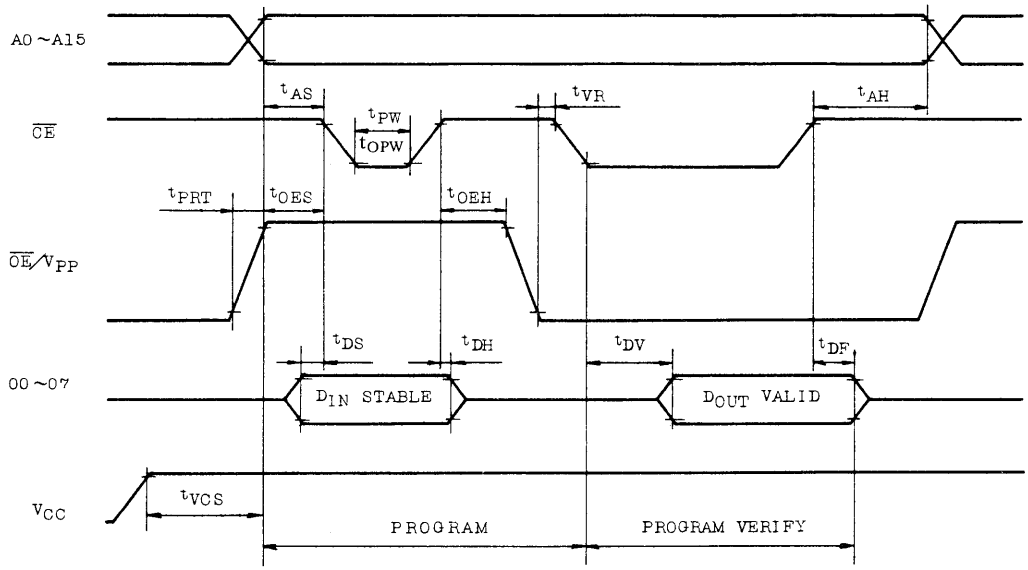
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.0V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (HIGH SPEED PROGRAM)

(V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.5V)



NOTE 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP} = 12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TMM24512P/F's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	O0 ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = 0 ~ 70°C)	Read	L	L	5V	Data Out	Active
	Output Deselect	*	H		High Impedance	
	Standby	H	*		High Impedance	Standby
Program Operation (Ta = 25 ± 5°C)	Program	L	V_{PP}	6V	Data In	Active
	Program Inhibit	H	V_{PP}		High Impedance	
	Program Verify	L	L		Data Out	

Note: H; V_{IH}, L; V_{IL}, * ; V_{IH} or V_{IL}

READ MODE

The TMM24512P/F has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) control the output buffers, independent of device selection. Assuming the $\overline{CE}$ = $\overline{OE}$ = V_{IL} , the output data is valid at the outputs after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}). Assuming that $\overline{CE}$ = V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} , the outputs will be in a high impedance state. So two or more TMM24512P/F's can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TMM24512P/F has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TMM24512P/F is placed in the standby mode which reduce the operating current to 35mA from 120mA (about 70% reduction) by applying TTL high level and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TMM24512P/F are in the "1" state which is erased state. Therefore the program operation is to introduce "0" data into the desired bit locations by electrically programming. The TMM24512P/F is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low level. The TMM24512P/F can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{CE}$ at V_{IL} and $\overline{OE}/V_{PP}$ at V_{IL} .

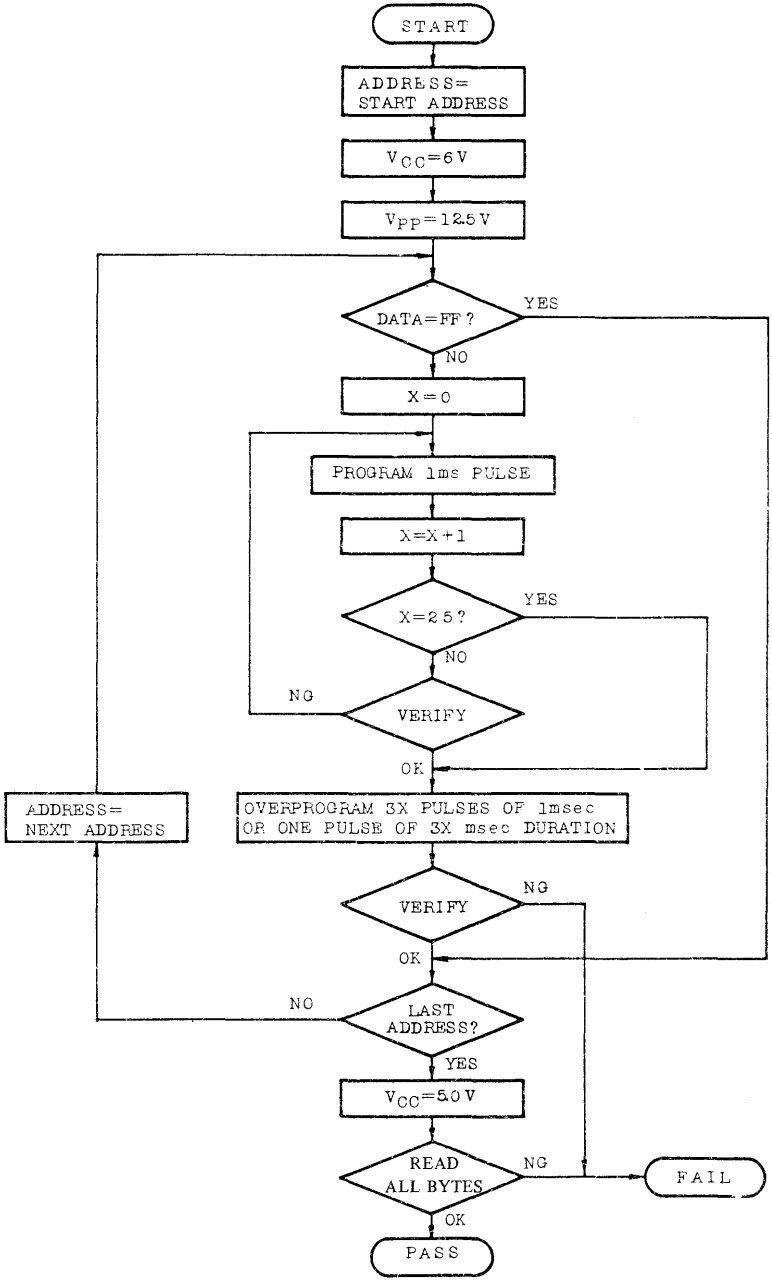
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TMM24512P/F from being programmed. Programming of two or more TMM24512P/F's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{CC} = 6V. The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times). After correctly programming the selected address, the additional program pulse with pulse width 3 times that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with V_{CC} = 5V.

- HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TMM24512P/F which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TMM24512P/F by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07).

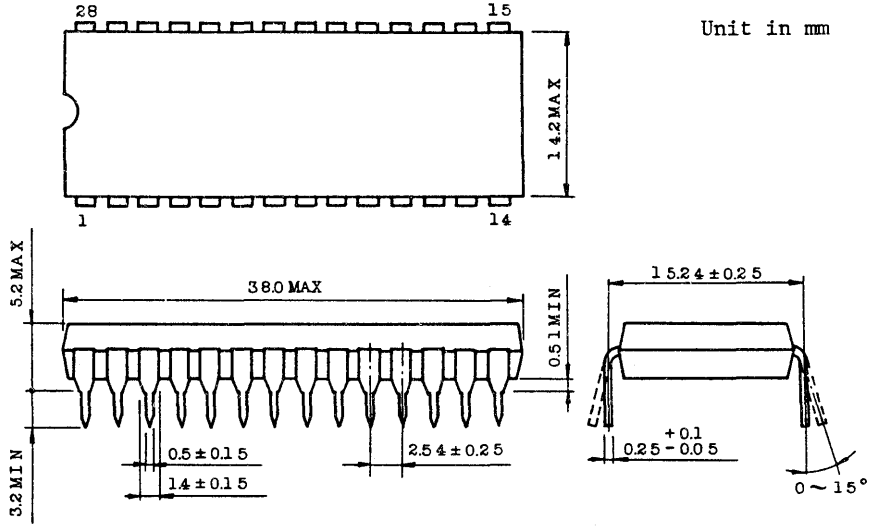
The following table shows electric signature of TMM24512P/F.

PINS / SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	0	0	0	1	0	1	0	1	15

Notes: A9 = 12V ± 0.5V
A1 ~ A8, A10 ~ A15, $\overline{CE}$, $\overline{OE}$ = V_{IL}

OUTLINE DRAWINGS (TMM24512P)

Unit in mm

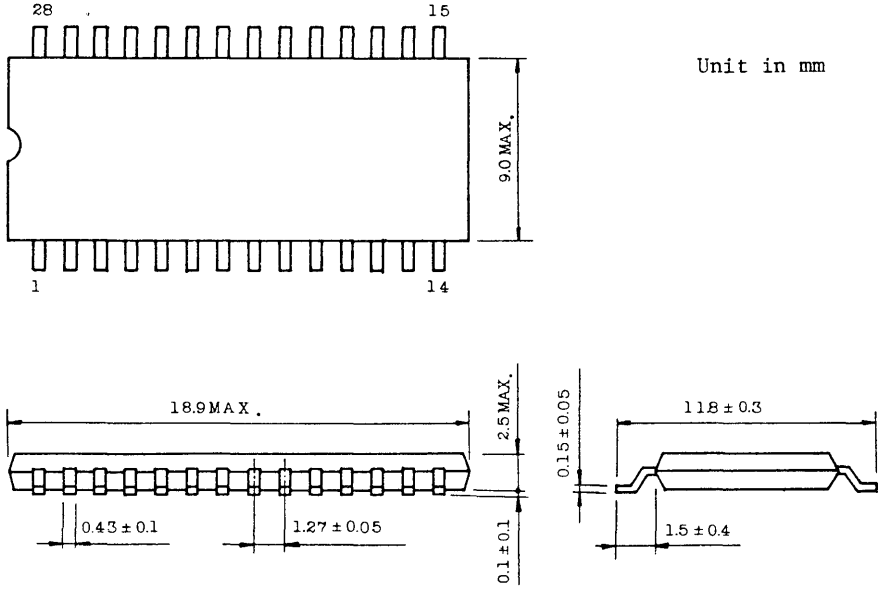


NOTE 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No. 1 and No. 28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TMM24512F)



NOTE: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No. 1 and No. 28 leads.

TMM24512AP/AF 65,536 WORD×8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TMM24512AP/AF-20/25

PRELIMINARY

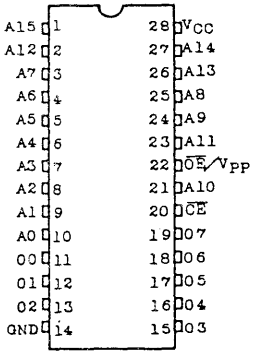
DESCRIPTION

The TMM24512AP/AF is a 65,536 word x 8 bit one time programmable read only memory and molded in a 28 pin plastic Package. The TMM24512AP/AF's access time is 200ns/250ns, and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TMM27512 AD's. Once programmed, the TMM24512AP/AF can not be erased because of using plastic DIP without transparent window.

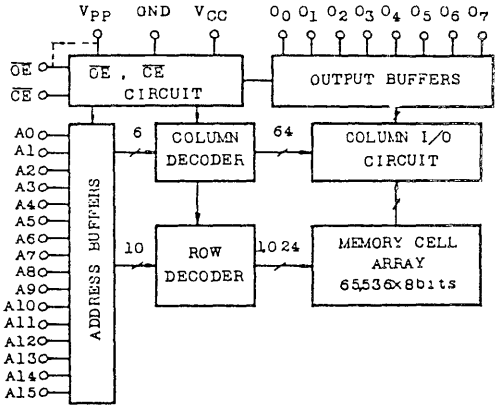
FEATURES

- Fast access time: 200ns, 250ns
- Low power dissipation
  Active: 120mA
  Standby: 35mA
- Single 5V power supply
- Full static operation
- High speed programming mode I, II
- Inputs and outputs TTL compatible
- Pin compatible with TMM27512D/AD
- Standard 28 pin DIP plastic package : TMM24512AP
- Plastic Flat Package : TMM24512AF

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

A0 ~ A15	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}/V_{PP}$	Output Enable Input / Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{OE}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	00 ~ 07 (11 ~ 13, 15 ~ 19)	POWER
Read	L	L	5V	Data Out	Active
Output Deselect	*	H		High Impedance	
Standby	H	*		High Impedance	Standby
Program	L	V_{PP}	6V[1] / 6.25V[2]	Data In	Active
Program Inhibit	H	V_{PP}		High Impedance	
Program Verify	L	L		Data Out	

*: H or L

1): HIGH SPEED PROGRAMMING MODE I
2): HIGH SPEED PROGRAMMING MODE II

TOSHIBA MOS MEMORY PRODUCTS

32,768 WORD × 8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE CMOS

TC54256AP/AF

DESCRIPTION

The TC54256AP/AF is a 32,768 word × 8 bit one time programmable read only memory, and molded in a 28 pin plastic package.

The TC54256AP/AF's access time is 200ns, and has low power standby mode which reduces the power dissipation without increasing access time.

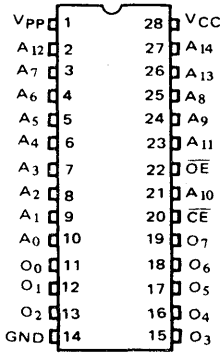
The electrical characteristics and programming method are the same as U. V. EPROM TC57256AD's.

Once programmed, the TC54256AP/AF can not be erased because of using plastic DIP without transparent window.

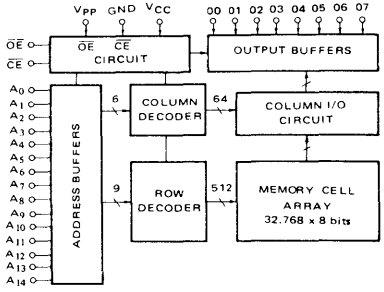
FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Low power dissipation
  Active : 30mA/5MHz
  Standby: 100μA
- Fast access time : 200ns
- Program voltage : 12.5V
- Single 5V power supply
- Full static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P EPROM TMM27256D/AD and TC57256D/AD
- TC54256AP : 28PIN standard plastic package
- TC54256AF : 28PIN flat package

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_{14}$	Address Inputs
$O_0 \sim O_7$	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{CC}	Power Supply Voltage (+5V)
GND	Ground

MODE SELECTION

MODE \ PIN	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	$O_0 \sim O_7$ (11~13, 15~19)	POWER
Read	L	L	5V	5V	Data Out	Active
Output Deselect	*	H			High Impedance	
Standby	H	*			High Impedance	Standby
Program	L	H	12.5V	6V	Data In	Active
Program Inhibit	H	H			High Impedance	
Program Verify	*	L			Data Out	

* H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	-0.6 ∿ 7.0	V
V_{PP}	Program Supply Voltage	-0.6 ∿ 14.0	V
V_{IN}	Input Voltage	-0.6 ∿ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ∿ V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ∿ 125	°C
T_{OPR}	Operating Temperature	-40 ∿ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	Vpp Power Supply Voltage	V_{CC}-0.6	V_{CC}	V_{CC}+0.6	

D.C. and OPERATING CHARACTERISTICS (Ta=-40 ∿ 85°C, V_{CC}=5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0V ∿ V_{CC}		-	-	±10	μA
I_{CCO1}	Operating Current	$\overline{CE}$=0V	f=6.7MHz	-	-	30	mA
I_{CCO2}			f=1MHz	-	-	10	
I_{CCS1}	Standby Current	$\overline{CE}$=V_{IH}		-	-	1	mA
I_{CCS2}		$\overline{CE}$=V_{CC}-0.2V		-	-	100	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA		2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		-	-	0.4	V
I_{PP1}	Vpp Current	V_{PP}=V_{CC}±0.6V		-	-	±10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0.4V ∿ V_{CC}		-	-	±10	μA

A.C. CHARACTERISTICS (Ta=-40 ~ 85°C, V_{CC}=5V±5%, V_{PP}=V_{CC}±0.6V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	-	200	ns
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE}$=V_{IL}	-	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IL}	-	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE}$=V_{IL}	0	60	
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IL}	0	60	
t_{OH}	Output Data in Hold Time	$\overline{CE}$=$\overline{OE}$=V_{IL}	0	-	

A.C. TEST CONDITIONS

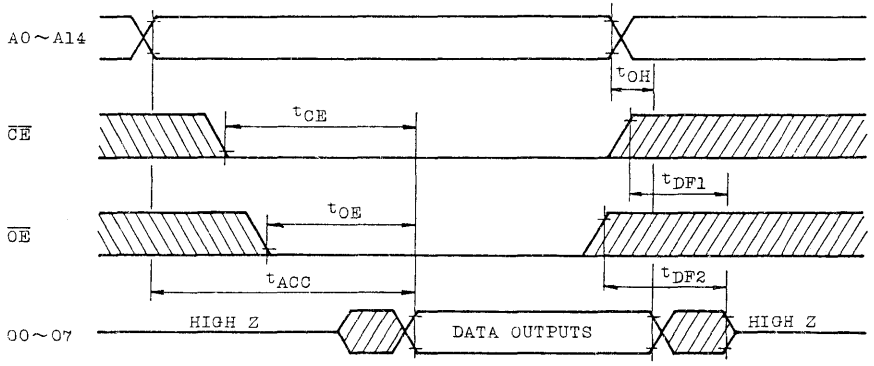
- Output Load : 1 TTL Gate and C_L=100pF
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ~ 2.4V
- Timing Measurement Reference Level : Inputs 0.8V and 2.2V, Outputs 0.8V and 2.0V

CAPACITANCE * (Ta=25°C, f=1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	-	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	-	8	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	-	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	
V_{CC}	V_{CC} Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	V_{PP} Power Supply Voltage	12.0	12.5	13.0	

D.C. and OPERATING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	V_{IN}=0 ∿ V_{CC}	-	-	±10	μA
V_{OH}	Output High Voltage	I_{OH}=-400μA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	-	-	0.4	V
I_{CC}	V_{CC} Supply Current	-	-	-	40	mA
I_{PP2}	V_{PP} Supply Current	V_{PP}=13.0V	-	-	50	mA
V_{ID}	A9 Auto Select Voltage	-	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS (Ta=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	-	2	-	-	μs
t_{AH}	Address Hold Time	-	2	-	-	μs
t_{CES}	$\overline{CE}$ Setup Time	-	0	-	-	ns
t_{CEH}	$\overline{CE}$ Hold Time	-	0	-	-	ns
t_{OES}	$\overline{OE}$ Setup Time	-	2	-	-	μs
t_{DS}	Data Setup Time	-	2	-	-	μs
t_{DH}	Data Hold Time	-	2	-	-	μs
t_{VPS}	V_{PP} Setup Time	-	2	-	-	μs
t_{VCS}	V_{CC} Setup Time	-	2	-	-	μs
t_{PW}	Initial Program Pulse Width	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	ms
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE}$=V_{IH}	-	-	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE}$=V_{IH}	-	-	130	ns

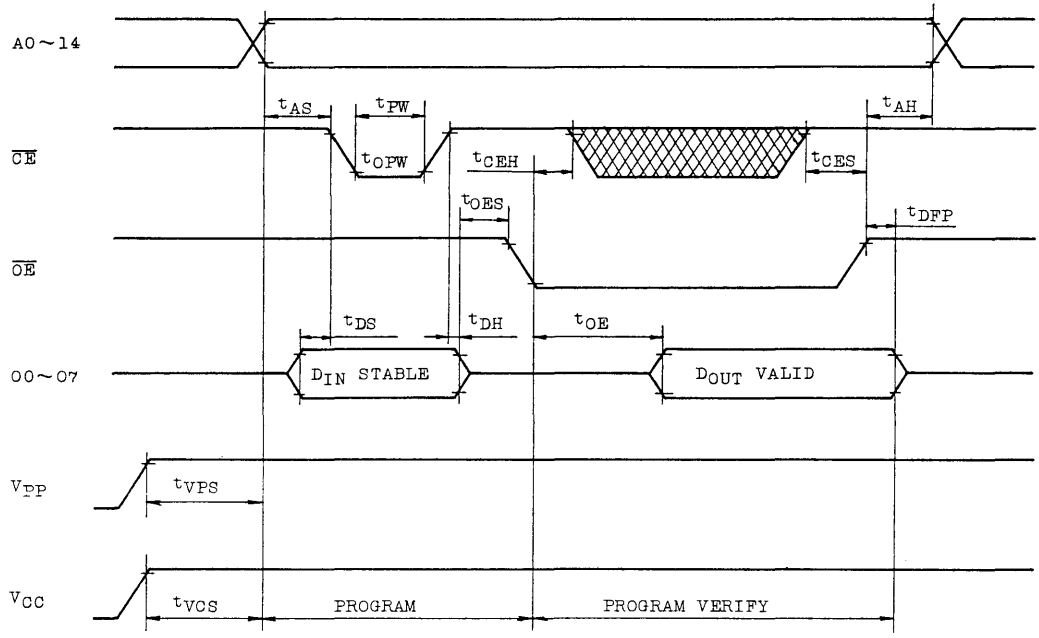
A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Times : 10ns Max.
- Input Pulse Levels : 0.45V ∿ 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

TIMING WAVEFORMS (PROGRAM)

(V_{CC}=6V±0.25V, V_{PP}=12.5V±0.5V)



Note 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP}=12.5V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation. So the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC54256AP/AF's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

MODE \ PIN NAMES (NUMBER)		$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	O0 ∿ O7 (11 ∿ 13, 15 ∿ 19)	POWER
Read Operation (Ta=-40 ∿ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta=25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC54256AP/AF has two control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection.
The output enable ($\overline{OE}$) controls the output buffers, independent of device selection.
Assuming that $\overline{CE}$=$\overline{OE}$=V_{IL}, the output data is valid at the outputs after address access time from stabilizing of all addresses.
The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).
Assuming that $\overline{CE}$=V_{IL} and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE}$=V_{IH} or $\overline{OE}$=V_{IH}, the outputs will be in a high impedance state. So two or more TC54256AP/AF's can be connected together on a common bus line.
When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduce the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC54256AP/AF are in the "1" state which is erased state.
Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.
The TC54256AP/AF is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low level under $\overline{OE}=V_{IH}$.
The TC54256AP/AF can be programmed any location at anytime either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that desired data is correctly programmed on the programmed bits.
The verify is accomplished with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} or V_{IL}.

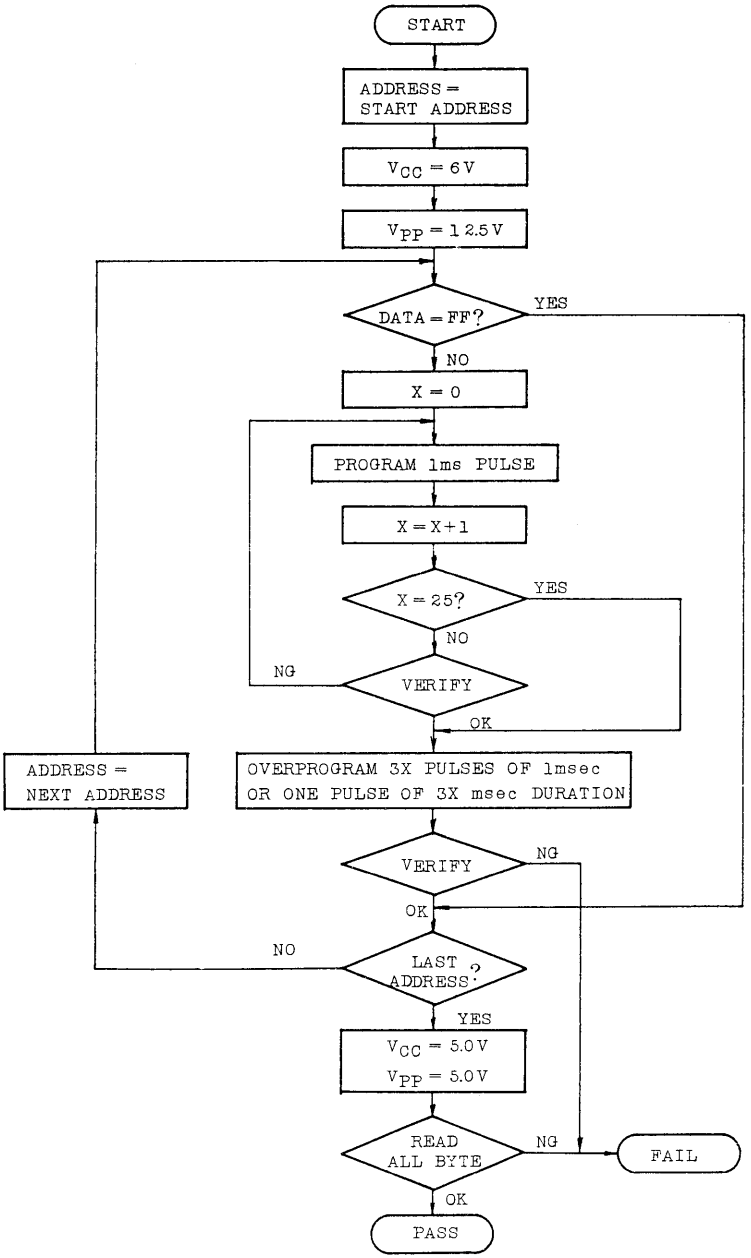
PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.5V) is applied to V_{PP} terminal, a TTL high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed. Programming of two or more TC54256AP/AF's in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, and a TTL Low level program pulse is applied to the $\overline{CE}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAMMING MODE

The program time can be greatly decreased by using this high speed programming mode. The device is set up in the high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with $V_{CC}=6V$.
The programming is achieved by applying a single TTL low level 1ms pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.
If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).
After correctly programming the selected address, the additional program pulse with width of 3 times more than that needed for initial programming is applied.
When programming has been completed, the data in all addresses should be verified with $V_{CC}=V_{PP}=5V$.

HIGH SPEED PROGRAM MODE FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC54256AP/AF by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (O7). The following table shows electric signature of TC54256AP/AF.

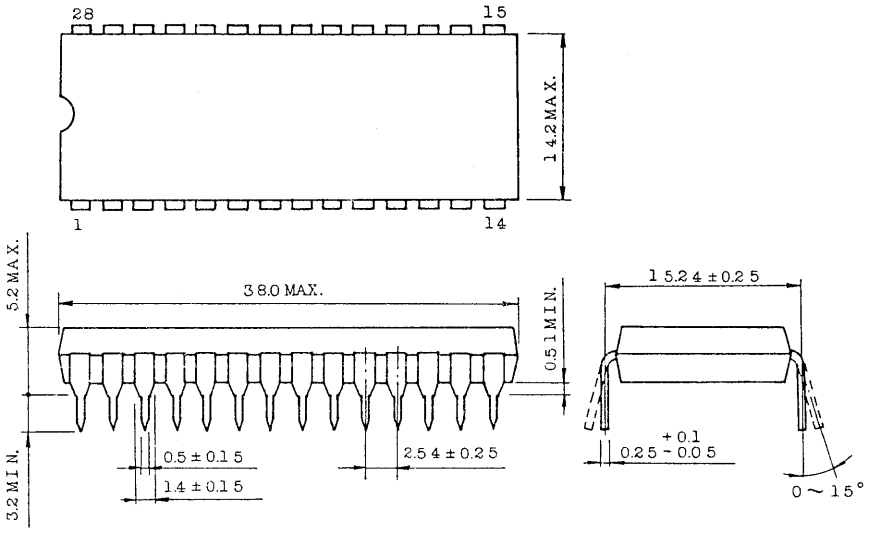
PINS / SIGNATURE	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	HEX. DATA
Manufacture Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9=12V±0.5V

A1 ∿ A8, A10 ∿ A14, $\overline{CE}$, $\overline{OE}=V_{IL}$

OUTLINE DRAWINGS (TC54256AP)

Unit in mm



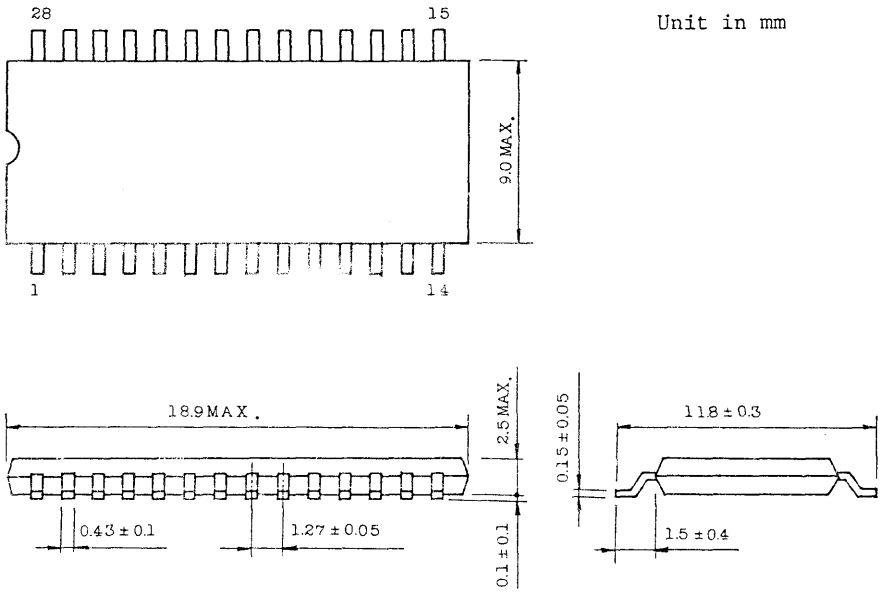
Note 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.28 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

OUTLINE DRAWINGS (TC54256AF)

Unit in mm



Note: Lead pitch is 1.27 and tolerance is ±0.12 against theoretical center of each lead that is obtained on the basis of No.1 and No.28 leads.

131,072 WORD×8 BIT CMOS ONE TIME PROGRAMMABLE READ ONLY MEMORY
SILICON STACKED GATE MOS

TC541000P-20, TC541000P-25
TC541001P-20, TC541001P-25

DESCRIPTION

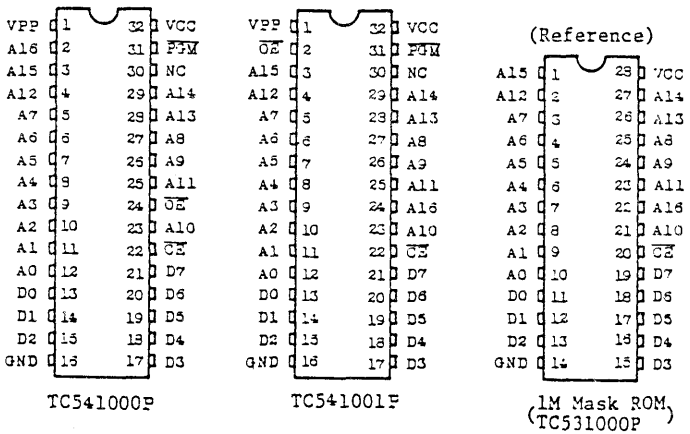
The TC541000P/TC541001P is a 131,072 word x 8 bit one time programmable read only memory, and molded in a 32 pin plastic package.

The TC541000P/TC541001P's access time is 200ns/250ns and has low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as U.V. EPROM TC571000D/TC571001D's. Once programed, the TC541000P/TC541001P can not be erased because of using plastic DIP without transparent window.

FEATURES

- Peripheral circuit : CMOS
  Memory cell : N-MOS
- Fast access Time
  TC541000P-20/TC541001P-20: 200ns
  TC541000P-25/TC541001P-25: 250ns
- Low power dissipation
  Active : 30mA/5.0MHz
  Standby: 100 μA (Ta = 85°C)
- Single 5V power supply
- Wide operating temperature range: −40 ~ 85°C
- Full static operation
- High speed programming operation: t_{PW} 0.1ms
- Input and output TTL compatible
- JEDEC standard 32 pin: TC541000P
- 1M MROM compatible : TC541001P
- Standard 32 pin DIP plastic package

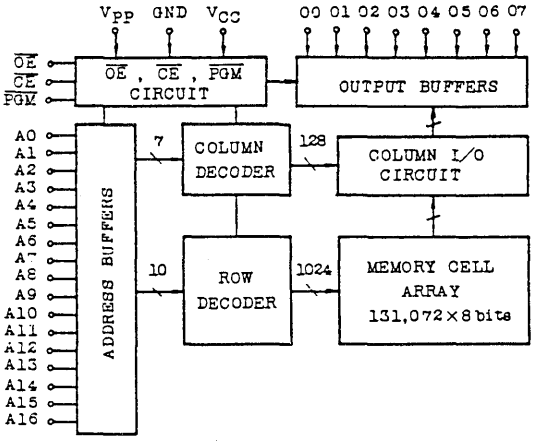
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
D0 ~ D7	Output (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Program Control Input
V_{CC}	Power Supply Voltage
V_{PP}	Program Supply Voltage
GND	Ground
NC	No Connection

BLOCK DIAGRAM



MODE SELECTION

MODE \ PIN	$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	O0 ~ O7	POWER
Read	H	L	L	5V	5V	Data Out	Active
Output Deselect	*	*	H			High Impedance	
Standby	*	H	*			High Impedance	Standby
Program	L	L	H	12.75V	6.25V	Data In	Active
Program Inhibit	*	H	*			High Impedance	
	H	L	H			High Impedance	
Program Verify	H	L	L			Data Out	

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Power Supply Voltage	−0.6 ~ 7.0	V
V_{PP}	Program Supply Voltage	−0.6 ~ 14.0	V
V_{IN}	Input Voltage	−0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.6 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec
T_{STRG}	Storage Temperature	−65 ~ 125	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C

READ OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	
V_{CC}	V_{CC} Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	V_{PP} Power Supply Voltage	V_{CC} − 0.6	V_{CC}	V_{CC} + 0.6	

D.C. AND OPERATING CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{CC} = 5V \pm 5\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$		–	–	±10	μA
I_{CC01}	Operating Current	$\overline{CE} = 0V$	f = 5.0 MHz	–	–	30	mA
I_{CC02}		$I_{OUT} = 0$ mA	f = 1 MHz	–	–	10	
I_{CCS1}	Standby Current	$\overline{CE} = V_{IH}$		–	–	1	mA
I_{CCS2}		$\overline{CE} = V_{CC} - 0.2V$		–	–	100	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$		2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		–	–	0.4	V
I_{PP1}	V_{PP} Current	$V_{PP} = V_{CC} \pm 0.6V$		–	–	±10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{CC}$		–	–	10	μA

A.C. CHARACTERISTICS ($Ta = -40 \sim 85°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6V$)

SYMBOL	PARAMETER	TC541000P-20/ TC541001P-20		TC541000P-25/ TC541001P-25		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{ACC}	Address Access Time	–	200	–	250	ns
t_{CE}	$\overline{CE}$ to Output Valid	–	200	–	250	
t_{OE}	$\overline{OE}$ to Output Valid	–	70	–	100	
t_{PGM}	$\overline{PGM}$ to Output Valid	–	70	–	100	
t_{DF1}	$\overline{CE}$ to Output in High-Z	0	60	0	90	
t_{DF2}	$\overline{OE}$ to Output in High-Z	0	60	0	90	
t_{DF3}	$\overline{PGM}$ to Output in High-Z	0	60	0	90	
t_{OH}	Output Data Hold Time	0	–	0	–	

A.C. TEST CONDITIONS

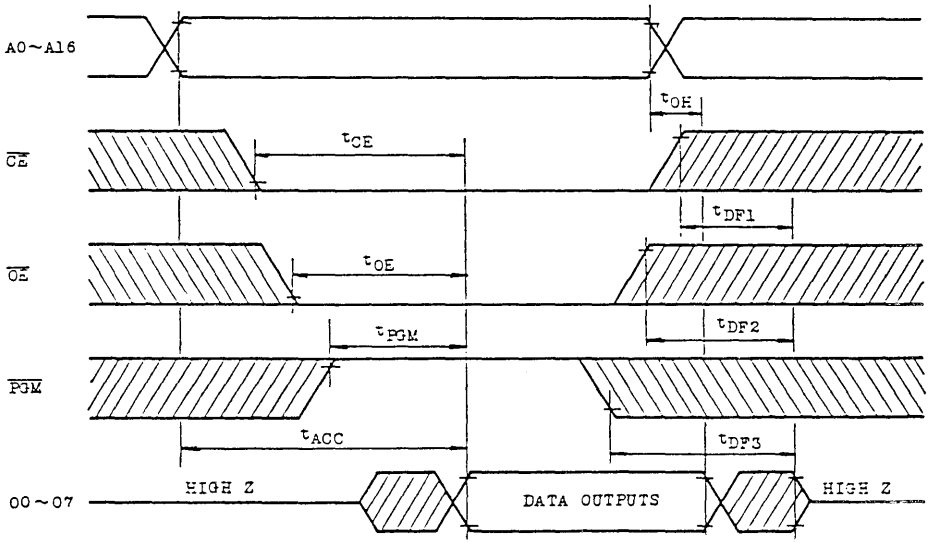
Output Load : 1 TTL Gate and C_L = 100pF
Input Pulse Rise and Fall Times : 10ns Max.
Input Pulse Levels : 0.45V and 2.4V
Timing Measurement Reference Level : Inputs 0.8V and 2.2V Outputs 0.8V and 2.0V

CAPACITANCE * (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	–	4	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	10	12	

* This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS (READ)



HIGH SPEED PROGRAM OPERATION

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage	–0.3	–	0.8	
V_{CC}	V_{CC} Power Supply Voltage	6.00	6.25	6.50	
V_{PP}	V_{PP} Power Supply Voltage	12.50	12.75	13.00	

D.C. AND OPERATING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.75 \pm 0.25V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Current	$V_{IN} = 0 \sim V_{CC}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\ \mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA	–	–	0.4	V
I_{CC}	V_{CC} Supply Current	–	–	–	30	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0V$	–	–	50	mA
V_{ID}	A9 Auto Select Voltage	–	11.5	12.0	12.5	V

A.C. PROGRAMMING CHARACTERISTICS ($Ta = 25 \pm 5°C$, $V_{CC} = 6.25 \pm 0.25V$, $V_{PP} = 12.75 \pm 0.25V$)

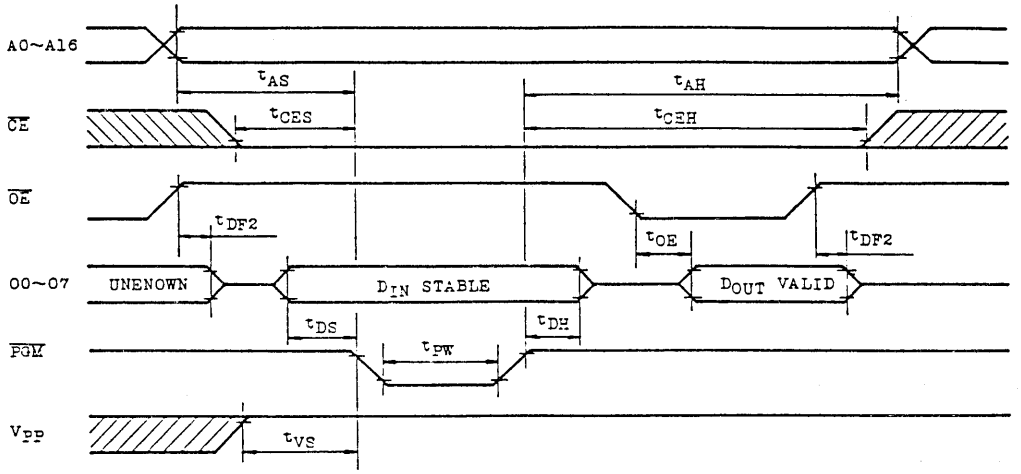
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	μs
t_{CES}	$\overline{CE}$ Setup Time	–	2	–	–	μs
t_{CEH}	$\overline{CE}$ Hold Time	–	2	–	–	μs
t_{DS}	Data Setup Time	–	2	–	–	μs
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VS}	V_{PP} Setup Time	–	2	–	–	μs
t_{PW}	Program Pulse Width	–	0.095	0.1	0.105	ms
t_{OE}	$\overline{OE}$ to Output Valid	–	–	–	100	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	–	–	90	ns

A.C. TEST CONDITIONS

- Output Load : 1 TTL Gate and C_L (100pF)
- Input Pulse Rise and Fall Time : 10ns Max.
- Input Pulse Levels : 0.45V and 2.4V
- Timing Measurement Reference Level : Input 0.8V and 2.2V, Output 0.8V and 2.0V

HIGH SPEED PROGRAM OPERATION

- TIMING CHART



NOTE: 1. V_{CC} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}.

2. Removing the device from socket and setting the device in socket with V_{PP} = 12.75V may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted up to 14V for program operation, so the voltage over 14V should not be applied to the V_{PP} terminal. When the switching pulse voltage is applied to the V_{PP} terminal, the overshoot voltage of its pulse should not be exceeded 14V.

OPERATION INFORMATION

The TC541000P/TC541001P's six operation modes are listed in the following table. Mode selection can be achieved by applying TTL level signal to all inputs.

		$\overline{PGM}$	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	$O_0 \sim O_7$	POWER
READ OPERATION (Ta = −40 ~ 85°C)	Read	H	L	L	5V	5V	Data Out	Active
	Output Deselect	*	*	H			High Impedance	
	Standby	*	H	*			High Impedance	Standby
PROGRAM OPERATION (Ta = 25 ± 5°C)	Program	L	L	H	12.75V	6.25V	Data In	Active
	Program Inhibit	*	H	*			High Impedance	
		H	L	H			High Impedance	
	Program Verify	H	L	L			Data Out	

Note: H; V_{IH}, L; V_{IL}, *; V_{IH} or V_{IL}

READ MODE

The TC541000P/TC541001P has three control functions. The chip enable ($\overline{CE}$) controls the operation power and should be used for device selection. The output enable ($\overline{OE}$) and the program control ($\overline{PGM}$) control the output buffers, independent of device selection.

Assuming in that $\overline{CE} = \overline{OE} = V_{IL}$ and $\overline{PGM} = V_{IH}$, the output data is valid at the output after address access time from stabilizing of all addresses. The $\overline{CE}$ to output valid (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$ and all addresses are valid, the output data is valid at the outputs after t_{OE} from the falling edge of $\overline{OE}$. And assuming that $\overline{CE} = \overline{OE} = V_{IL}$ and all addresses are valid, the output data is valid at the outputs after t_{PGM} from the rising edge of $\overline{PGM}$.

OUTPUT DESELECT MODE

Assuming that $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state. So two or more ROMs can be connected together on a common bus line. When $\overline{CE}$ is decoded for device selection, all deselected devices are in low power standby mode.

STANDBY MODE

The TC541000P/TC541001P has a low power standby mode controlled by the $\overline{CE}$ signal. By applying a high level to the $\overline{CE}$ input, the TC541000P/TC541001P is placed in the standby mode which recude the operating current to 100μA by applying MOS-high level (V_{CC}) and then the outputs are in a high impedance state, independent of the $\overline{OE}$ inputs.

PROGRAM MODE

Initially, when received by customers, all bits of the TC541000P/TC541001P are in the "1" state which is erased state. Therefore the program operation is to introduce "0's" data into the desired bit locations by electrically programming.

The levels required for all inputs are TTL. The TC541000P/TC541001P can be programmed any location at anytime —— either individually, sequentially, or at random.

PROGRAM VERIFY MODE

The verify mode is to check that the desired data is correctly programmed on the programmed bits. The verify is accomplished with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and PGM at V_{IH}.

PROGRAM INHIBIT MODE

Under the condition that the program voltage (+12.75V) is applied to V_{PP} terminal, a high level $\overline{CE}$ or $\overline{PGM}$ input inhibits the TC541000P/TC541001P from being programmed. Programming of two or more EPROMS in parallel with different data is easily accomplished. That is, all inputs except for $\overline{CE}$ or $\overline{PGM}$ may be commonly connected, and a TTL low level program pulse is applied to the $\overline{CE}$ and $\overline{PGM}$ of the desired device only and TTL high level signal is applied to the other devices.

HIGH SPEED PROGRAM OPERATION

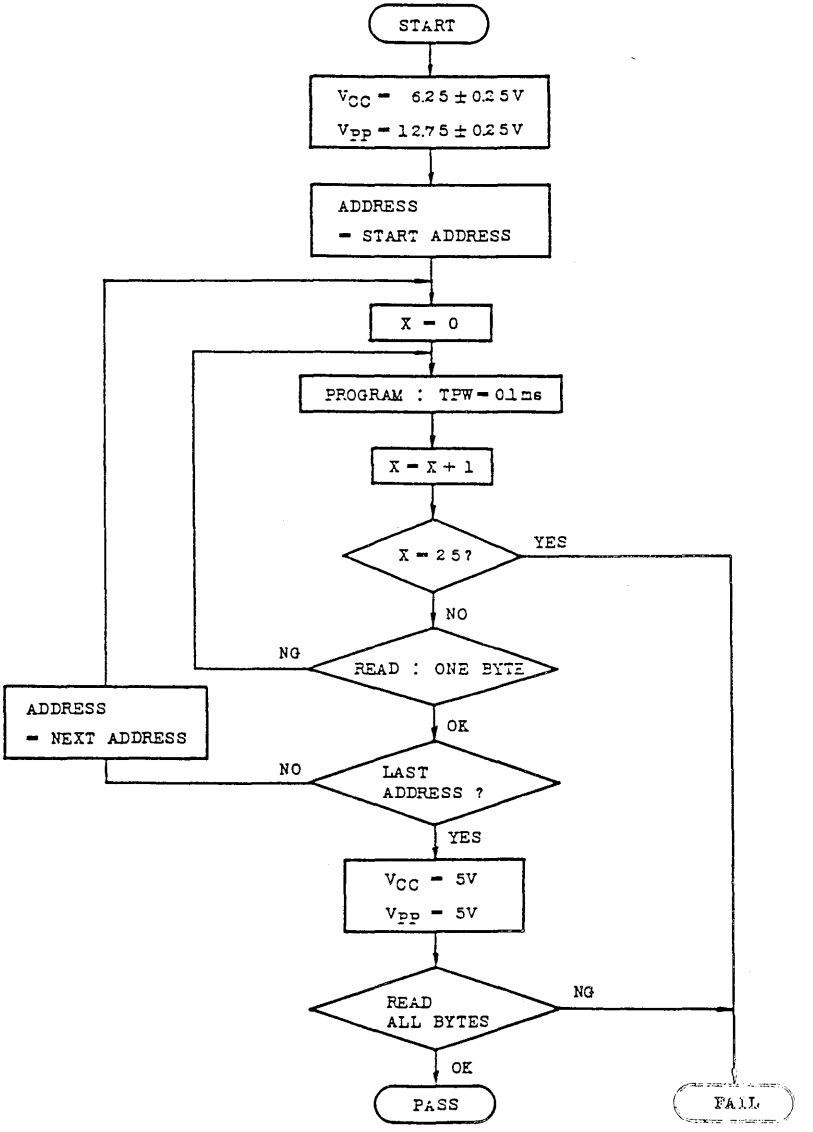
The device is set up in the high speed programming mode when the programming voltage (+12.75V) is applied to the V_{PP} terminal with V_{CC} = 6.25V and $\overline{PGM} = V_{IH}$.

The programming is achieved by applying a single TTL low level 0.1 ms pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify Mode.

If the programmed data is not correct, another program pulse of 0.1ms is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times).

When programming has been completed, the data in all addresses should be verified with V_{CC} = V_{PP} = 5V.

- FLOW CHART



ELECTRIC SIGNATURE MODE

Electric signature mode allows to read out a code from TC541000P/TC541001P which identifies it's manufacturer and device type.

The programming equipment may read out manufacturer code and device code from TC541000P/TC541001P by using this mode before program operation and automatically set program voltage (V_{PP}) and algorithm.

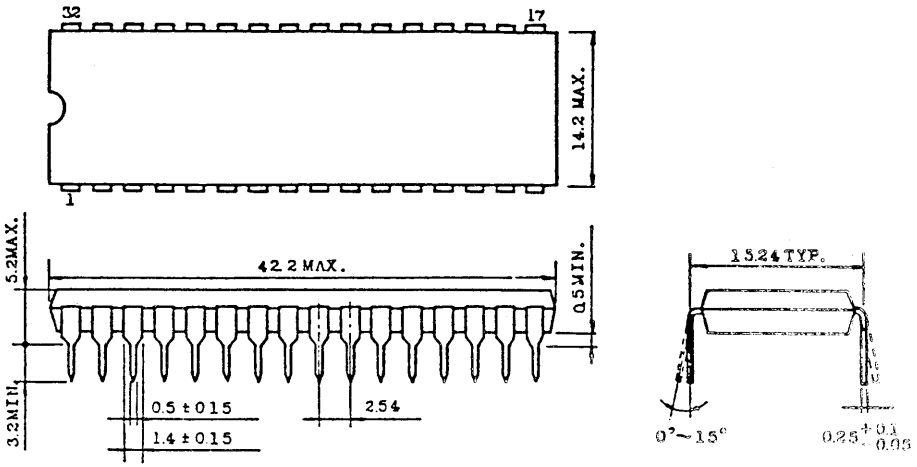
Electric Signature mode is set up when 12V is applied to address line A9 and the rest of address lines is set to V_{IL} in read operation. Data output in this conditions is manufacturer code. Device code is identified when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit of MSB (07). The following table shows electric signature of TC541000P/TC541001P.

PINS / SIGNATURE		A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	HEX. DATA
Manufacture Code		V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	TC541000P	V_{IH}	1	0	0	0	0	1	1	0	86
	TC541001P		0	0	0	0	0	1	1	1	07

Notes: A9 = 12V ± 0.5V
A1 ~ A8, A10 ~ A16, $\overline{CE}$, $\overline{OE}$ = V_{IL}
$\overline{PGM}$ = V_{IH}

OUTLINE DRAWINGS

Unit in mm



NOTE : 1. Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect No.1 and No.32 leads.

2. This value is measured at the end of leads.

3. All dimensions are in millimeters.

MROM

TOSHIBA MOS MEMORY PRODUCTS

256K BIT (32K WORD × 8 BIT) CMOS MASK ROM
SILICON GATE MOS

TC53257P
TC53257F

DESCRIPTION

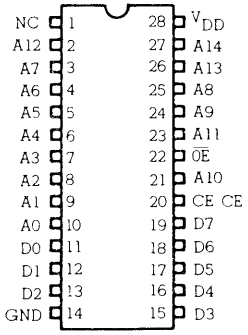
The TC53257P/F is a 262,144 bit read only memory organized as 32,768 words by 8 bits with a low bit cost, this being suitable for use in program memory of microprocessor, and in character generator. The TC53257P/F using CMOS technology is most suitable for low power applications where battery operation is required.

The TC53257P/F has one programmable chip enable input $\overline{CE}$/CE, for device selection and one output enable input ($\overline{OE}$) for fast memory access and output control.

FEATURES

- Single 5V Power Supply
- Access Time: 200ns(Max.)
- Power Dissipation
  Operating Current : 25mA(Max.)
  Standby Current : 20μA(Max.)
- Pin Compatible with 256K EPROM TC57256AD/ADI
- Pin Compatible with 256K OTPROM TC54256AP/AF
- Full Static Operation
- Programmable Chip Enable
- All Inputs and Outputs : TTL Compatible
- Three State Outputs
- Package
  Plastic DIP : TC53257P
  Plastic FP : TC53257F

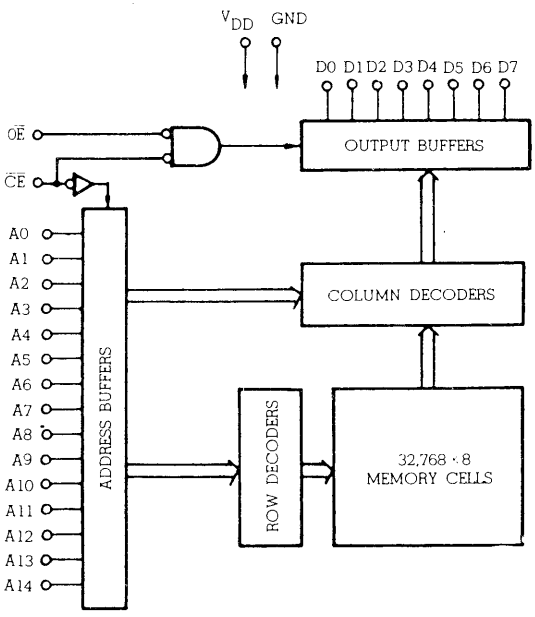
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{14}	Address Inputs
D_0~D_7	Data Outputs
NC	No connection
$\overline{CE}$/CE	Chip enable input
$\overline{OE}$	Output enable input
V_{DD}	Power supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−0.5~7.0	V
V_{OUT}	Output Voltage	0~V_{DD}	V
P_D	Power Dissipation	1.0 0.6*	W
T_{STG}	Storage Temperature	−55~150	°C
T_{OPR}	Operating Temperature	−40~85	°C
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : *Plastic FP

D. C. OPERATING CONDITINS (Ta = −40~85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V

D. C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V~V_{DD}	—	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} V_{OUT} = 0V~V_{DD}	—	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	—	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	—	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH} CE = V_{IL}	—	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} − 0.2V, CE = 0.2V	—	20	μA
I_{DDO1}	Operating Current	V_{IH} = $V_{IH\ VIL}$, t_{CYCLE} = 200ns	—	40	mA
I_{DDO2}		V_{IN} = V_{DD} − 0.2V/0.2V, t_{CYCLE} = 200ns	—	25	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	—	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	—	10	pF

Note : This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS

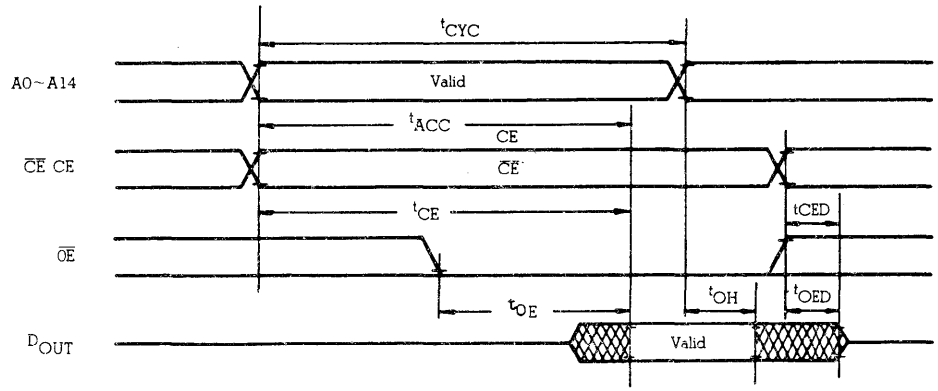
($Ta = -40 \sim 85°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	200	—	ns
t_{ACC}	Access Time	—	200	ns
t_{CE}	Chip Enable Access Time from CE/$\overline{CE}$	—	200	ns
t_{OE}	Output Enable Access Time from $\overline{OE}$	—	70	ns
t_{CED}, t_{OED}	Output Disable Time from CE/$\overline{CE}$, $\overline{OE}$	0	60	ns
t_{OH}	Output Hold Time	0	—	ns

A. C. TEST CONDITIONS

Output Load : 100pF + 1TTL
Input Levels : 0.6V, 2.4V
Timing Measurement Reference Levels
Input : 0.8V, 2.2V
Output : 0.8V, 2.2V
Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



OPERATION MODE

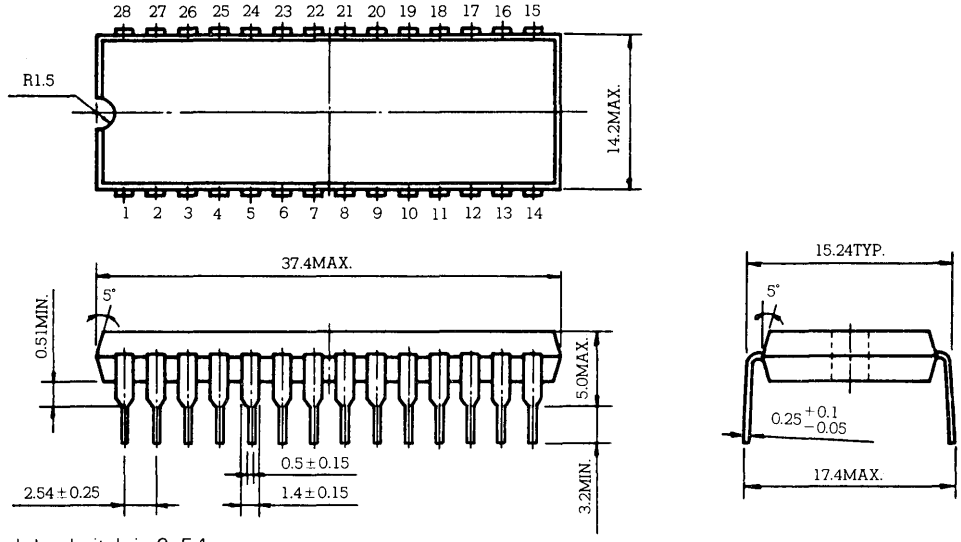
H : V_{IH}, L : V_{IL}, * : V_{IH} or V_{IL}

MODE	$\overline{CE}$(CE)	$\overline{OE}$	$A_{0 \sim 14}$	Outputs	Power
Read	L(H)	L	Valid	Data out	Operating
Output Deselect	L(H)	H	*	High-Z	Operating
	H(L)	*	*		Standby

OUTLINE DRAWINGS

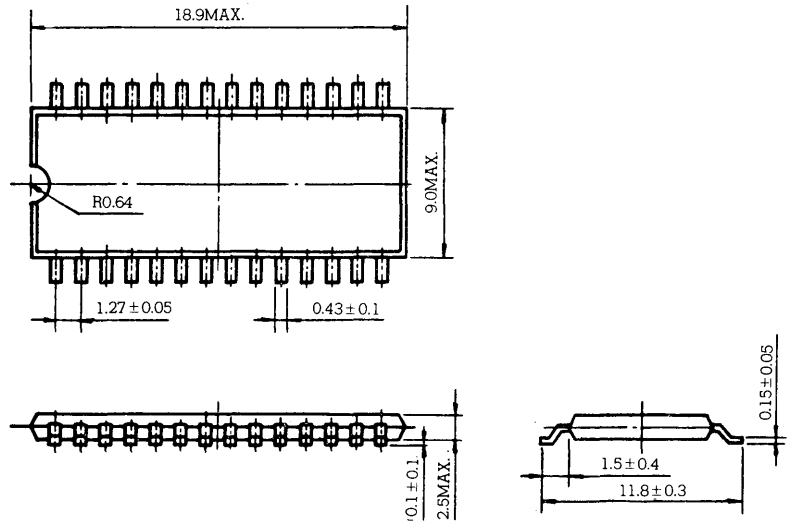
- Plastic DIP

Unit: mm



NOTE : Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.

- Plastic FP



NOTE : Each lead pitch is 1.27mm.
All leads are located within 0.12mm of their true longitudinal position with respect to No.1 and No.28 leads.

1M BIT (128K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC531000AP,TC531000AF

DESCRIPTION

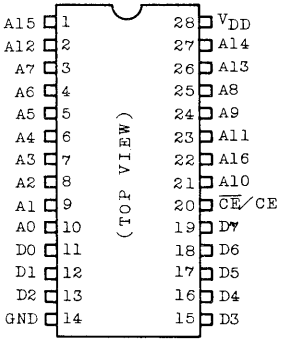
The TC531000AP/AF is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, especially character generator. The TC531000AP/AF using CMOS technology is most suitable for low power applications where battery operation are required.

The TC531000AP/AF has one chip enable input $\overline{CE}$/CE, programmable for device selection.

FEATURES

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  - Operating Current: 40mA (Max.)
  - Standby Current: 20μA (Max.)
- All Inputs and Outputs: TTL Compatible
- Three State Outputs
- Fully Static Operation
- Programmable Chip Enable
- Package
  - Plastic DIP: TC531000AP
  - Plastic FP: TC531000AF

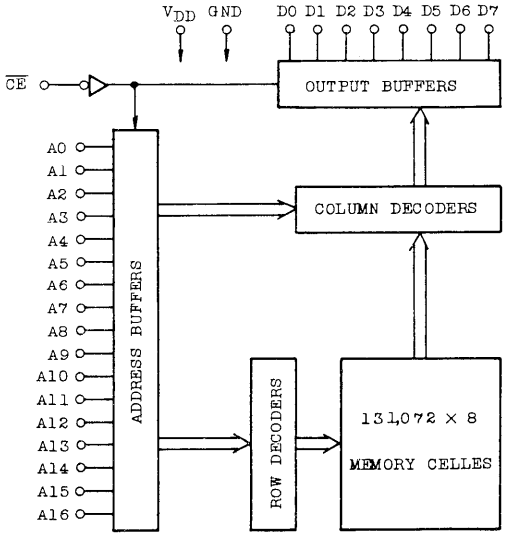
PIN CONNECTION



PIN NAMES

A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
$\overline{CE}$/CE	Chip Enable Input
V_{DD}	Power Supply
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ V_{DD}	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0/0.6*	W
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−40 ~ 70	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note: * Plastic FP

D.C. OPERATING CONDITIONS (Ta = −40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	−0.3	–	0.8	V

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 ~ V_{DD}	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} and V_{IN} = 0V (V_{DD})	–	20	μA
I_{DD01}	Operating Current	V_{IN} = V_{IH} /V_{IL} , t_{cycle} = 150ns	–	50	mA
I_{DD02}		V_{IN} = V_{DD}/0V, t_{cycle} = 150ns	–	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	–	10	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	–	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

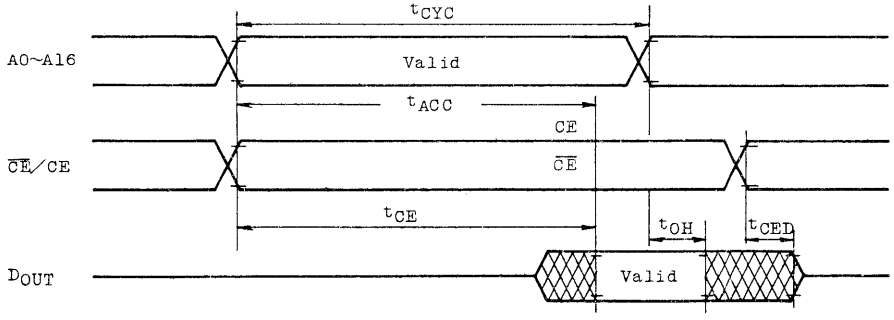
A.C. CHARACTERISTICS (V_{DD} = 5V ± 5V ± 10%, Ta = −40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Access Time	—	150	ns
t_{CE}	Chip Enable Access Time	—	150	ns
t_{CED}	Output Disable Time	—	50	ns
t_{OH}	Output Hold Time	10	—	ns

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input : 0.8V, 2.2V
  Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



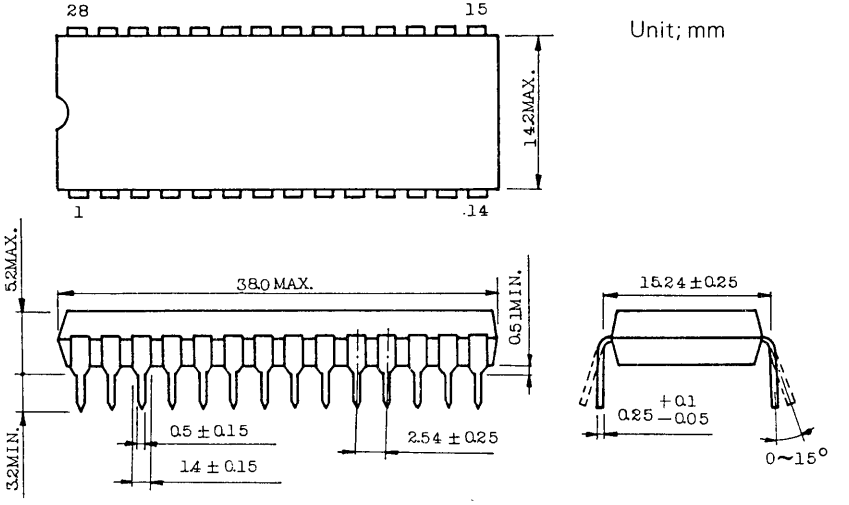
OPERATION MODE

MODE	$\overline{CE}$(CE)	A0 ~ 16	Outputs	Power
Read	L(H)	Valid	Data Out	Operating
Output Deselect	H(L)	*	High-Z	Standby

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

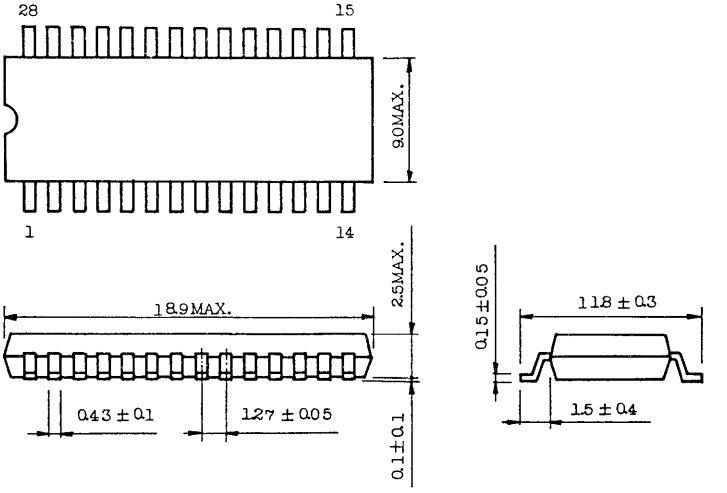
- OUTLINE DRAWINGS

Plastic DIP



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

Plastic FP



NOTE: Each lead pitch is 1.27mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 28 leads.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserve the right, at any time without notice, to change said circuitry.

1M BIT (128K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC531001AP

DESCRIPTION

The TC531001AP is a 1,048,576 bits read only memory organized as 131,072 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, and data memory, especially character generator. The TC531001AP using CMOS technology is most suitable for low power applications where battery operations are required.

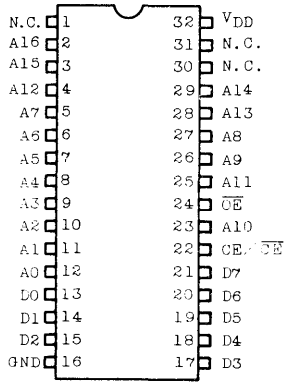
The TC531001AP has one programmable chip enable input $\overline{CE}$/CE for device selection.

The TC531001AP is moulded in a 32 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V Power Supply
- Access Time: 150ns (Max.)
- Power Dissipation
  Operating Current: 40mA (Max.)
  Standby Current: 20μA (Max.)
- All inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

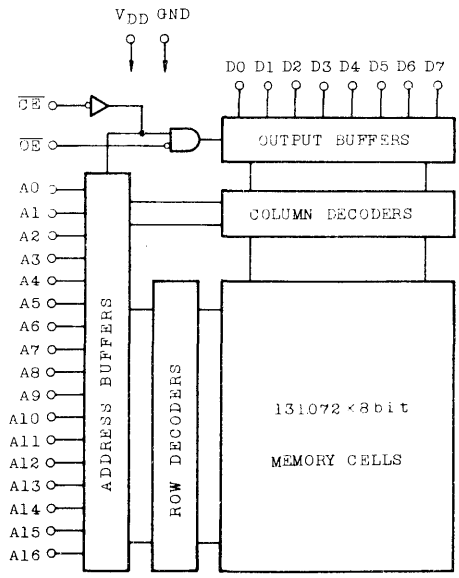
PIN CONNECTION



PIN NAMES

A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
$\overline{OE}$	Output Enable Input
$\overline{CE}$/CE	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ V_{DD}	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−40 ~ 70	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3	–	0.8	

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	–	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V ~ V_{DD}	–	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	–	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	3.2	–	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	–	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD}-0.2V and V_{IN} = 0V (V_{DD})	–	20	μA
I_{DD01}	Operating Current	V_{IN} = V_{IH} /V_{IL}, t_{cycle} = 150ns	–	50	mA
I_{DD02}		V_{IN} = V_{DD}-0.2V/0.2V, t_{cycle} = 150ns	–	40	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	–	10	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	–	10	

Note: This parameter is periodically sampled and is not 100% tested.

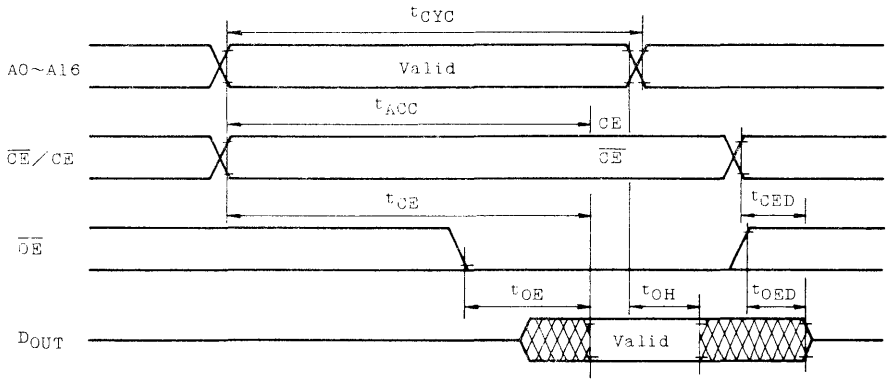
A.C. CHARACTERISTICS (Ta = −40 ~ 70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	150	—	ns
t_{ACC}	Access Time	—	150	
t_{CE}	Chip Enable Access Time	—	150	
t_{OE}	Output Enable Access Time	—	70	
t_{CED}	Output Disable Time	—	50	
t_{OED}	Output Disable Time from OE	—	50	
t_{OH}	Output Hold Time	0	—	

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input : 0.8V, 2.2V
  Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



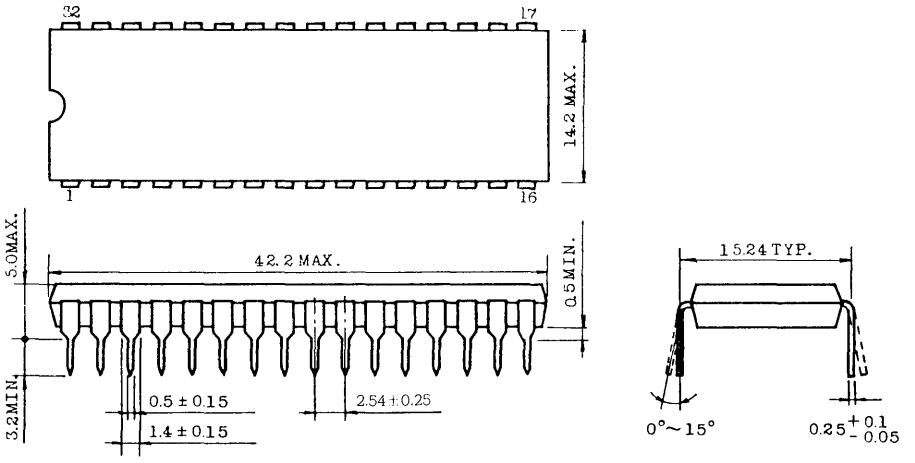
OPERATION MODE

MODE	$\overline{CE}$(CE)	$\overline{OE}$	A0 ~ 16	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

• OUTLINE DRAWINGS

Unit: mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 32 leads.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

4M BIT (512K WORD×8 BIT) CMOS MASK ROM
SILICON GATE CMOS

TC534000P

DESCRIPTION

The TC534000P is a 4,194,304 bits read only memory organized as 524,288 words by 8 bits with a low bit cost, thus being suitable for use in program memory of microprocessor, and data memory, especially character generator. The TC534000P using CMOS technology is most suitable for low power applications where battery operations are required.

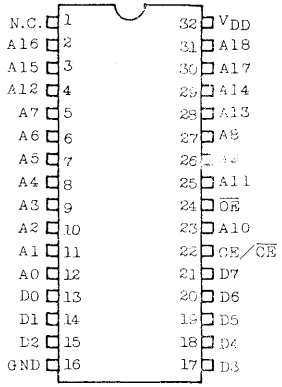
The TC534000P has one programmable chip enable input $\overline{CE}$/CE for device selection.

The TC534000P is moulded in a 32 pin standard plastic package, 0.6 inch in width.

FEATURES

- Single 5V Power Supply
- Access Time: 250ns (Max.)
- Power Dissipation
  Operating Current: 30mA (Max.)
  Standby Current: 20μA (Max.)
- All inputs and Outputs: TTL Compatible
- Three State Outputs
- 32 pin 600 mil width Plastic DIP
- Fully Static Operation
- Programmable Chip Enable

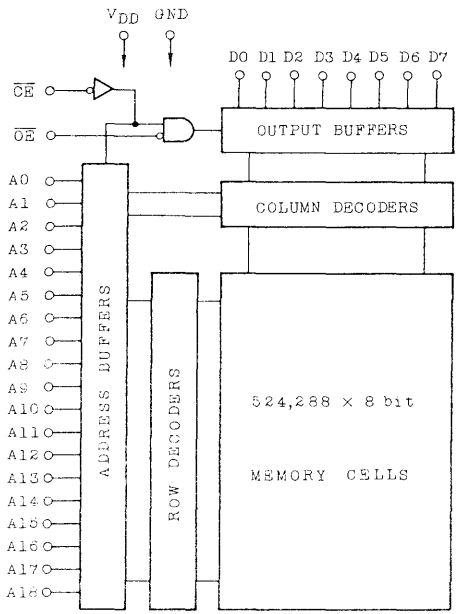
PIN CONNECTION



PIN NAMES

A0 ~ A18	Address Inputs
D0 ~ D7	Data Outputs
$\overline{OE}$	Output Enable Input
CE/$\overline{CE}$	Chip Enable Input
V_{DD}	Power Supply
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5 ~ 7.0	V
V_{IN}	Input Voltage	−0.5 ~ V_{DD}	V
V_{OUT}	Output Voltage	0 ~ V_{DD}	V
P_D	Power Dissipation	1.0	W
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{OPR}	Operating Temperature	−40 ~ 85	°C
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

D.C. OPERATING CONDITIONS (Ta = −40 ~ 85°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3	−	0.8	

D.C. and OPERATING CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}	−	±1.0	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V ~ V_{DD}	−	±5.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−1.0	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	2.0	−	mA
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}	−	2	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD}-0.2V and V_{IN} = 0V (V_{DD})	−	20	μA
I_{DD01}	Operating Current	V_{IN} = V_{IH} /V_{IL} , t_{cycle} = 250ns	−	40	mA
I_{DD02}		V_{IN} = V_{DD}-0.2V/0.2V, t_{cycle} = 250ns	−	30	mA

CAPACITANCE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	f = 1MHz, Ta = 25°C	−	8	pF
C_{OUT}	Output Capacitance	f = 1MHz, Ta = 25°C	−	10	

Note: This parameter is periodically sampled and is not 100% tested.

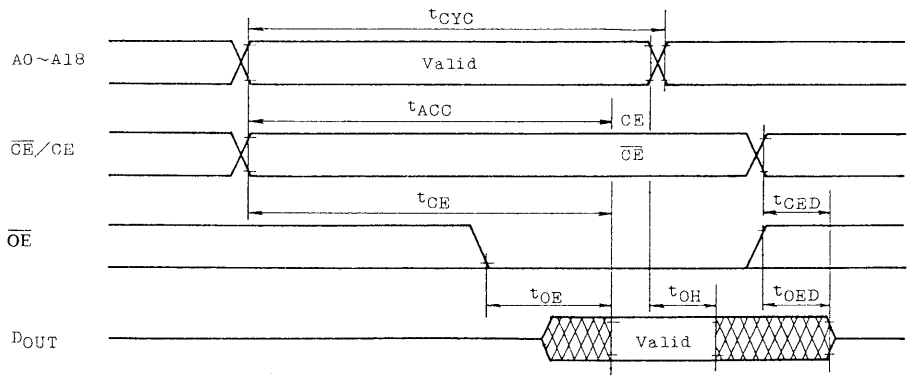
A.C. CHARACTERISTICS (Ta = −40 ~ 85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{CYC}	Cycle Time	250	—	ns
t_{ACC}	Access Time	—	250	
t_{CE}	Chip Enable Access Time	—	250	
t_{OE}	Output Enable Access Time	—	100	
t_{CED}	Output Disable Time	—	80	
t_{OED}	Output Disable Time from OE	—	80	
t_{OH}	Output Hold Time	10	—	

AC TEST CONDITIONS

- Output Load : 100pF + 1TTL
- Input Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels Input : 0.8V, 2.2V
  Output : 0.8V, 2.0V
- Input Rise and Fall Time : 5ns

TIMING WAVEFORMS



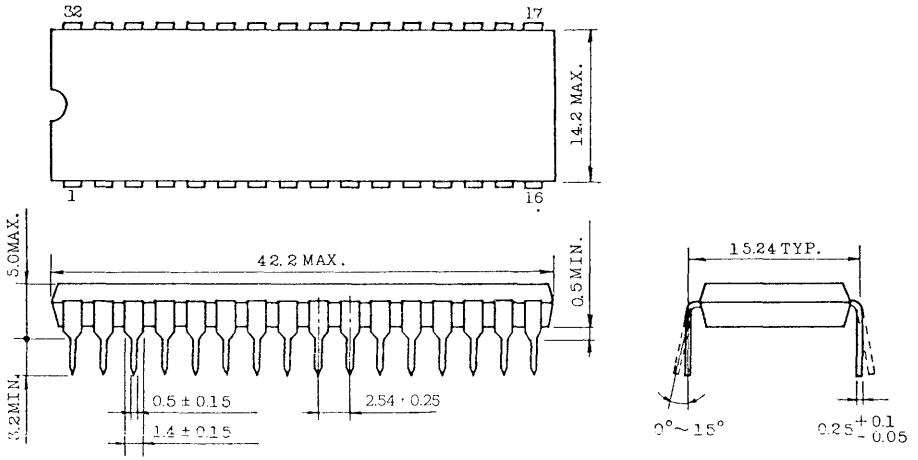
OPERATING MODE

MODE	$\overline{CE}$(CE)	$\overline{OE}$	A0 ~ 18	Outputs	Power
Read	L(H)	L	Valid	Data Out	Operating
Standby	H(L)	*	*	High-Z	Standby
Output Deselect	L(H)	H	*	High-Z	Operating

H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

- OUTLINE DRAWINGS

Unit: mm



NOTE: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 32 leads.

NOTE: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.