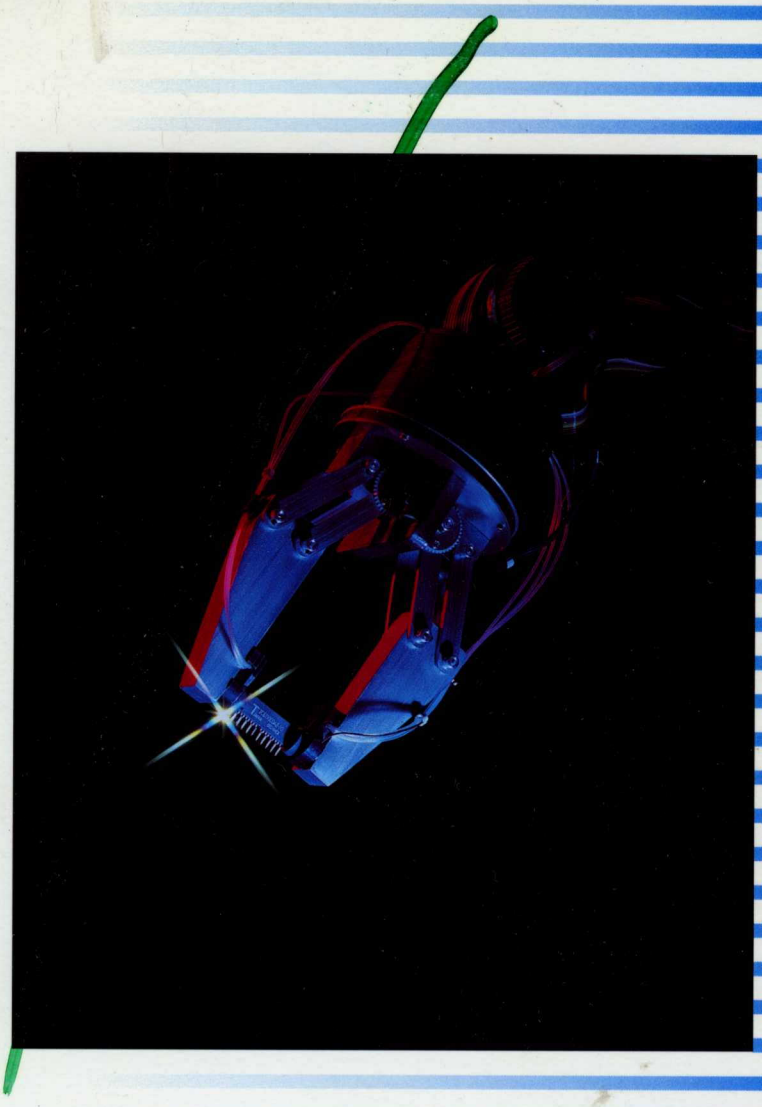
TOSHIBA

1M DRAM
1M VRAM
1991



TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA

1M DRAM
1M VRAM
1991

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DRAM PRODUCT GUIDE

1. CMOS DYNAMIC RAM

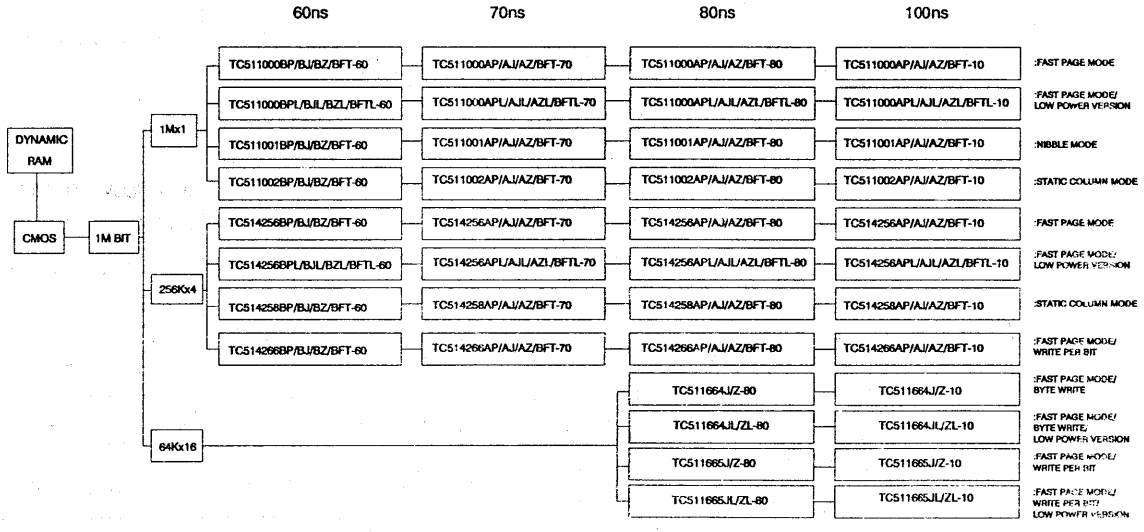
CAPACITY	PART NUMBER	ORGANIZATION, OPERATING MODE	$\overline{RAS}$ ACCESS TIME MAX (ns)	$\overline{CAS}$ ACCESS TIME MAX (ns)	POWER DISSIPATION MAX (mW) ACTIVE	POWER DISSIPATION MAX (mW) STANDBY	PIN COUNT	PACKAGE P	PACKAGE J	PACKAGE Z	PACKAGE FT	PACKAGE WIDTH (P,J,FT) OR HEIGHT (Z) (inch)
1M	TC511000AP/AJ/AZ-70	1M x 1, FAST PAGE MODE	70	20	440	5.5	18(P) 26/20(J) 20(Z) 24(FT)	■	■	■		0.300 (P) 0.300 (J) 0.400 (Z) 0.616 (FT)
	TC511000AP/AJ/AZ-80		80		385			■	■	■		
	TC511000AP/AJ/AZ-10		100	25	330			■	■	■		
	TC511000APL/AJL/AZL-70		70	20	440	1.1		■	■	■		
	TC511000APL/AJL/AZL-80		80		385			■	■	■		
	TC511000APL/AJL/AZL-10		100	25	330			■	■	■		
	TC511000BP/BJ/BZ/BFT-60		60	20	495	5.5		■	■	■	■	
	TC511000BPL/BJL/BZL/BFTL-60					1.1		■	■	■	■	
	TC511001AP/AJ/AZ-70	1M x 1, NIBBLE MODE	70		440	5.5		■	■	■		
	TC511001AP/AJ/AZ-80		80		385			■	■	■		
	TC511001AP/AJ/AZ-10		100	25	330			■	■	■		
	TC511001BP/BJ/BZ/BFT-60		60	20	495			■	■	■	■	
	TC511002AP/AJ/AZ-70	1M x 1, STATIC COLUMN MODE	70		440			■	■	■		
	TC511002AP/AJ/AZ-80		80		385			■	■	■		
	TC511002AP/AJ/AZ-10		100	25	330			■	■	■		
	TC511002BP/BJ/BZ/BFT-60		60	20	495			■	■	■	■	
	TC514256AP/AJ/AZ-70	256K x 4, FAST PAGE MODE	70		440		20(P) 26/20(Z) 20(Z) 24(FT)	■	■	■		
	TC514256AP/AJ/AZ-80		80		385			■	■	■		
	TC514256AP/AJ/AZ-10		100	25	330			■	■	■		
	TC514256APL/AJL/AZL-70		70	20	440	1.1		■	■	■		
	TC514256APL/AJL/AZL-80		80		385			■	■	■		
	TC514256APL/AJL/AZL-10		100	25	330			■	■	■		
	TC514256BP/BJ/BZ/BFT-60		60	20	495	5.5		■	■	■	■	
	TC514256BPL/BJL/BZL/BFTL-60					1.1		■	■	■	■	
	TC514258AP/AJ/AZ-70	256K x 4, STATIC COLUMN MODE	70		440	5.5		■	■	■		
	TC514258AP/AJ/AZ-80		80		385			■	■	■		
	TC514258AP/AJ/AZ-10		100	25	330			■	■	■		
	TC514258BP/BJ/BZ/BFT-60		60	20	495			■	■	■	■	
	TC514266AP/AJ/AZ-70	256K x 4, WRITE PER BIT	70		440			■	■	■		
	TC514266AP/AJ/AZ-80		80		385			■	■	■		
	TC514266AP/AJ/AZ-10		100	25	330			■	■	■		
	TC514266BP/BJ/BZ/BFT-60		60	20	495			■	■	■	■	

P = PLASTIC DIP, J = PLASTIC SOJ, Z = PLASTIC ZIP, FT = PLASTIC TYPE I TSOP

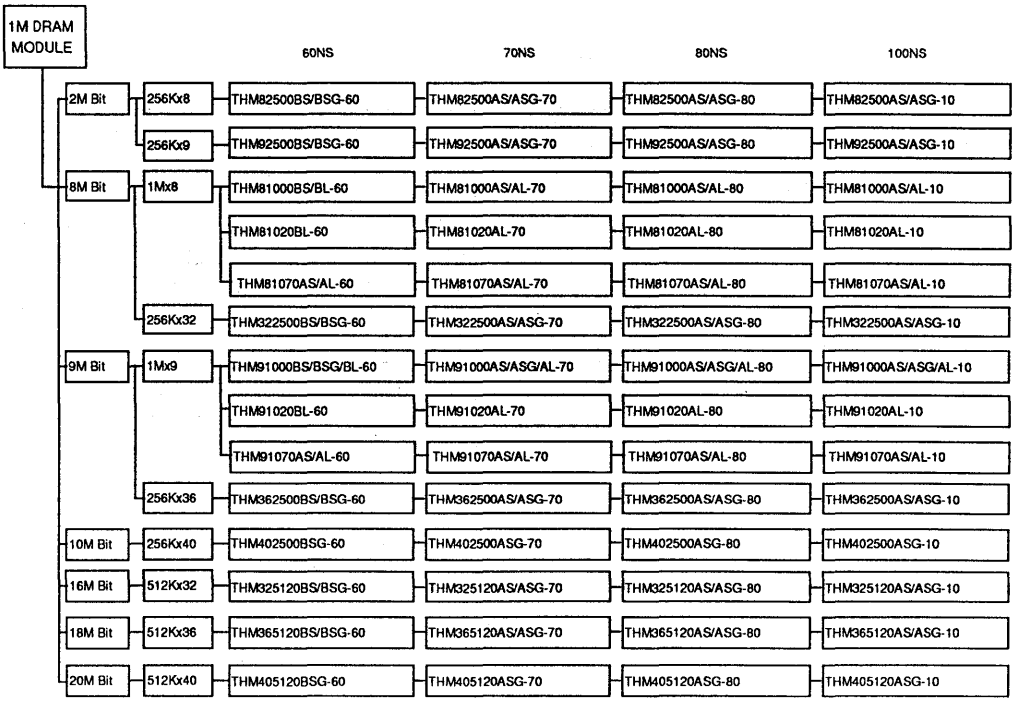
2. MODULES

CAPACITY	TYPE NO.	ORGANIZATION	ACCESS TIME tRAC	NO. OF PINS	DIMENSIONS (mm)			COMMENTS
					HEIGHT	LENGTH	WIDTH	
2MBIT	THM82500AS/ASG-70/80/10	256Kx8	70,80,100ns	30	17.9	88.9	5.08	USING 1M DRAM
	THM82500BS/BSG-60		60ns					
	THM92500AS/ASG-70/80/10	256Kx9	70,80,100ns					
	THM92500BS/BSG-60		60ns					
8MBIT	THM81000AS/AL-70/80/10	1Mx8	70,80,100ns	30	20.45/22.60	88.9/79.75	5.08	
	THM81000BS/BL-60		60ns					
	THM81020AL-70/80/10		70,80,100ns		12.64	82.14	8.89	LOW PROFILE
	THM81020BL-60		60ns					
	THM81070AS/AL-60/70/80/10		60,70,80,100ns		15.24	88.9	5.08	USING 4M DRAM
	THM322500AS/ASG-70/80/10	256Kx32	70,80,100ns	72	25.4	107.95	5.08	SINGLE-SIDED
	THM322500BS/BSG-60		60ns					
9MBIT	THM91000AS/ASG/AL-70/80/10	1Mx9	70,80,100ns	30	20.45/22.60	88.9/82.14	5.08	
	THM91000BS/BSG/BL-60		60ns					
	THM91020AL-70/80/10		70,80,100ns		12.64	88.9	8.89	LOW PROFILE
	THM91020AL-60		60ns					
	THM91070AS/AL-60/70/80/10		60,70,80,100ns		15.24	88.9	5.08	USING 4M DRAM
	THM362500AS/ASG-70/80/10	256Kx36	70,80,100ns	72	25.4	107.95	5.08	SINGLE-SIDED
	THM362500BS/BSG-60		60ns					
10MBIT	THM402500ASG-70/80/10	256Kx40	70,80,100ns	72	25.4	107.95	5.08	SINGLE-SIDED
	THM402500BSG-60		60ns					
16MBIT	THM325120AS/ASG-70/80/10	512Kx32	70,80,100ns	72	25.4	107.95	8.89	DOUBLE-SIDED
	THM325120BS/BSG-60		60ns					
18MBIT	THM365120AS/ASG-70/80/10	512Kx36	70,80,100ns	72	25.4	107.95	8.89	DOUBLE-SIDED
	THM365120BS/BSG-60		60ns					
20MBIT	THM405120ASG-70/80/10	512Kx40	70,80,100ns	72	25.4	107.95	8.89	DOUBLE-SIDED
	THM405120BSG-60		60ns					

1M DRAM COMPONENTS



1M DRAM MODULES



DRAM CROSS REFERENCE

1. 1M x 1 DYNAMIC RAM

FUNCTION	FAST PAGE	NIBBLE	STATIC COLUMN
TOSHIBA	**TC511000BP/BJ/BZ/BFT**	**TC511001BP/BJ/BZ/BFT**	**TC511002BP/BJ/BZ/BFT**
HITACHI	HM511000AP/AJP/AZP	HM511001AP/AJP/AZP	HM511002AP/AJP/AZP
NEC	uPD421000C/LA/V	uPD421001C/LA/V	uPD421002C/LA/V
MITSUBISHI	M5M41000AP/AJ/AL	M5M41001AP/AJ/AL	M5M41002AP/AJ/AL
OKI	MSM511000RS/JS/ZS	MSM511001RS/JS/ZS	MSM511002RS/JS/ZS
FUJITSU	MB81C1000P/PJ/PSZ	MB81C1001P/PJ/PSZ	MB81C1002P/PJ/PSZ
MICRON	MT4C1024PD/DJA/ZB	MT4C1025PD/DJA/ZB	MT4C1026PD/DJA/ZB
TI	TMS4C1024N/DJ	TMS4C1025N/DJ	TMS4C1026N/DJ
SIEMENS	HYB511000		HYB511002
VITELIC	V53C100		V53C102

2. 256K x 4 DYNAMIC RAM

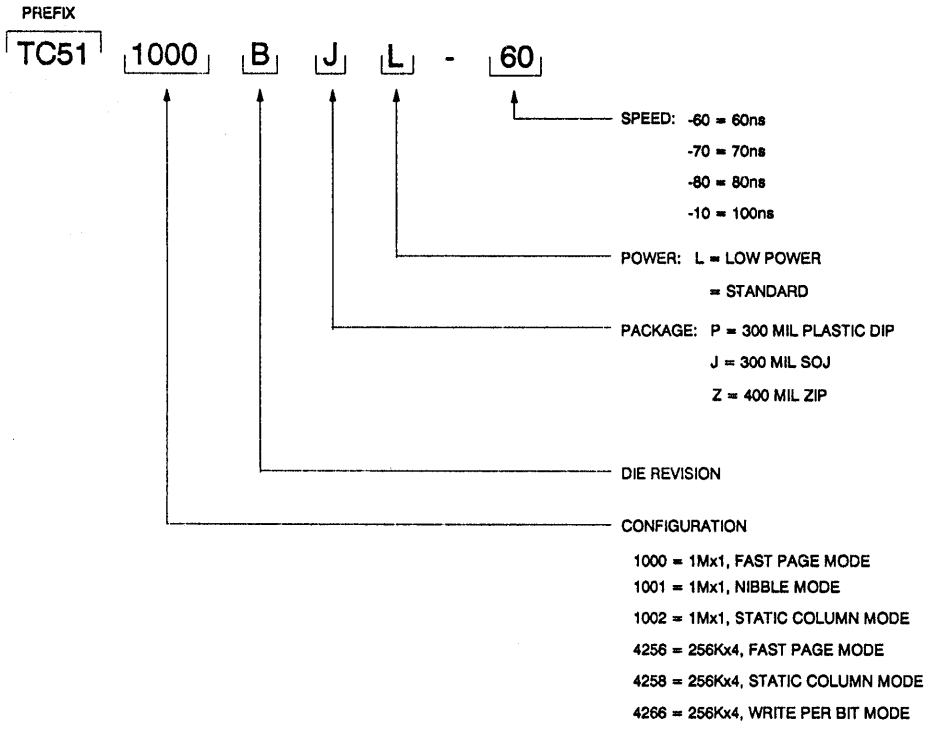
FUNCTION	FAST PAGE	STATIC COLUMN	FAST PAGE WRITE PER BIT
TOSHIBA	TC514256BP/BJ/BZ/BFT	TC514258BP/BJ/BZ/BFT	TC514266BP/BJ/BZ/BFT
HITACHI	HM514256AP/AJP/AZP	HM514258AP/AJP/AZP	HM514266AP/AJP/AZP
NEC	uPD424256C/LA/V	uPD424258C/LA/V	uPD424266C/LA/V
MITSUBISHI	M5M44256BP/BJ/BL/BVP/BRV	M5M44258/BP/BJ/BL/BVP/BRV	M5M44266BP/BJ/BL/BVP/BRV
OKI	MSM514256RS/JS/ZS	MSM514258RS/JS/ZS	
FUJITSU	MB81C4256P/PJ/PSZ	MB81C4258P/PJ/PSZ	
MICRON	MT4C4256PD/DJA/ZB	MT4C4258PD/DJA/ZB	
TI	TMS44C256N/DJ		
VITELIC	V53C104	V53C106	V53C105

3. DRAM MODULE

ORGANIZATION	256Kx8	256Kx9	1Mx8	256Kx32	1Mx9	256Kx36	256Kx40	512Kx32	512Kx36	512Kx40
TOSHIBA	THM82500	THM92500	THM81000	THM322500	THM91000	THM362500	THM402500	THM325120	THM365120	THM405120
FUJITSU		MB85240	MB85230		MB85235	MB85236				MB85254
HITACHI	HB561008	HB561003	HB56A18		HB56A19	HB56D25636			HB56D51236	
MITSUBISHI	MH25608	MH25609	MH1M08AOJ		MH1M09AOJ	MH25636AJ			MH51236AJ	
NEC	MC157	MC41256A9	MC42100A8		MC421000A9	MC424256A36			MC424512A36	
OKI	MSC2328	MSC2331	MSC2313	MSC2327	MSC2312	MSC2320		MSC2333	MSC2321	
NMB			MM1M100J8		MM1M100J9					
TI	TM4256GU8	TM42566U9	TM024GAD8		TM024EAD9					
MICRON	MT8C8256	MT8C9256	MT8C8024		MT8C9024	MT8C36256			MT8C36512	

PART NUMBER GUIDE

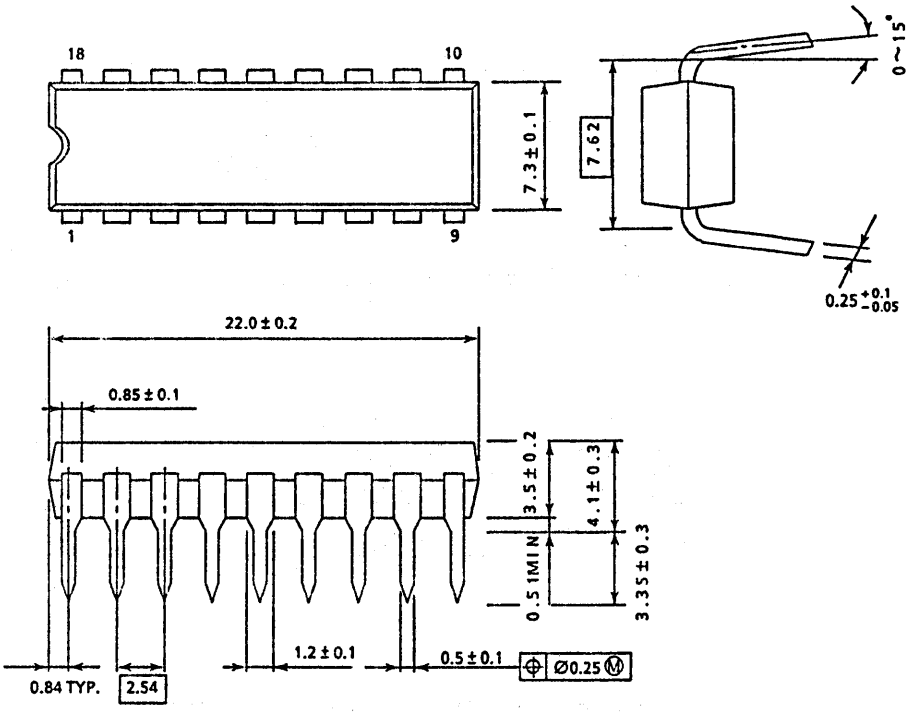
1M DRAM PART NUMBER GUIDE



COMPONENT MECHANICAL DIMENSIONS

300 MIL WIDTH DIP OUTLINE DRAWING

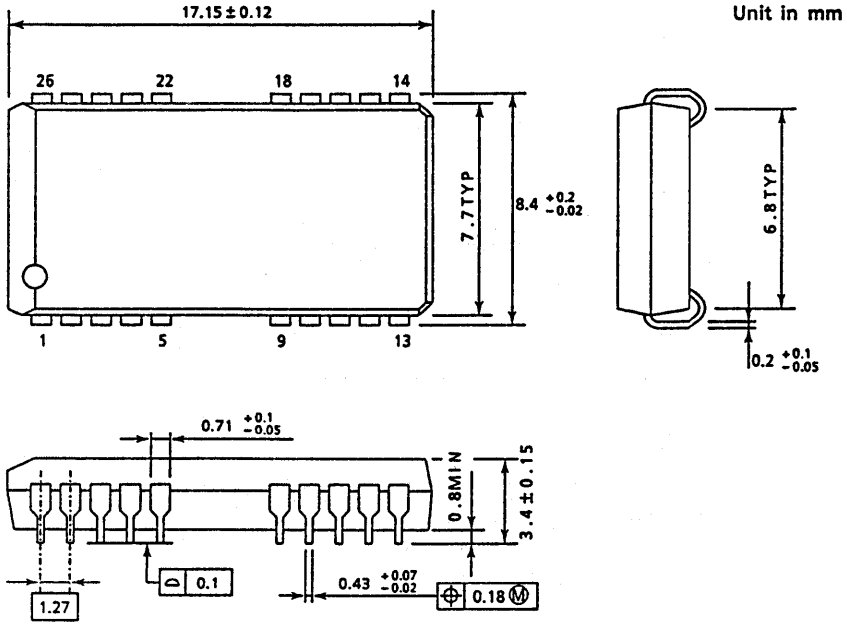
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

300 MIL WIDTH SOJ OUTLINE DRAWING

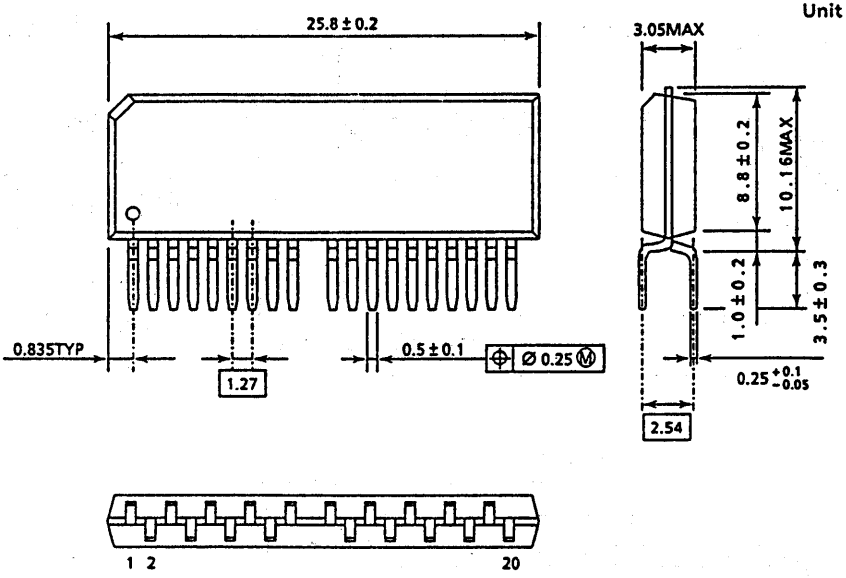
Unit in mm



Note: Package width and length do not include mold protrustion, allowable mold protrusion is 0.15mm.

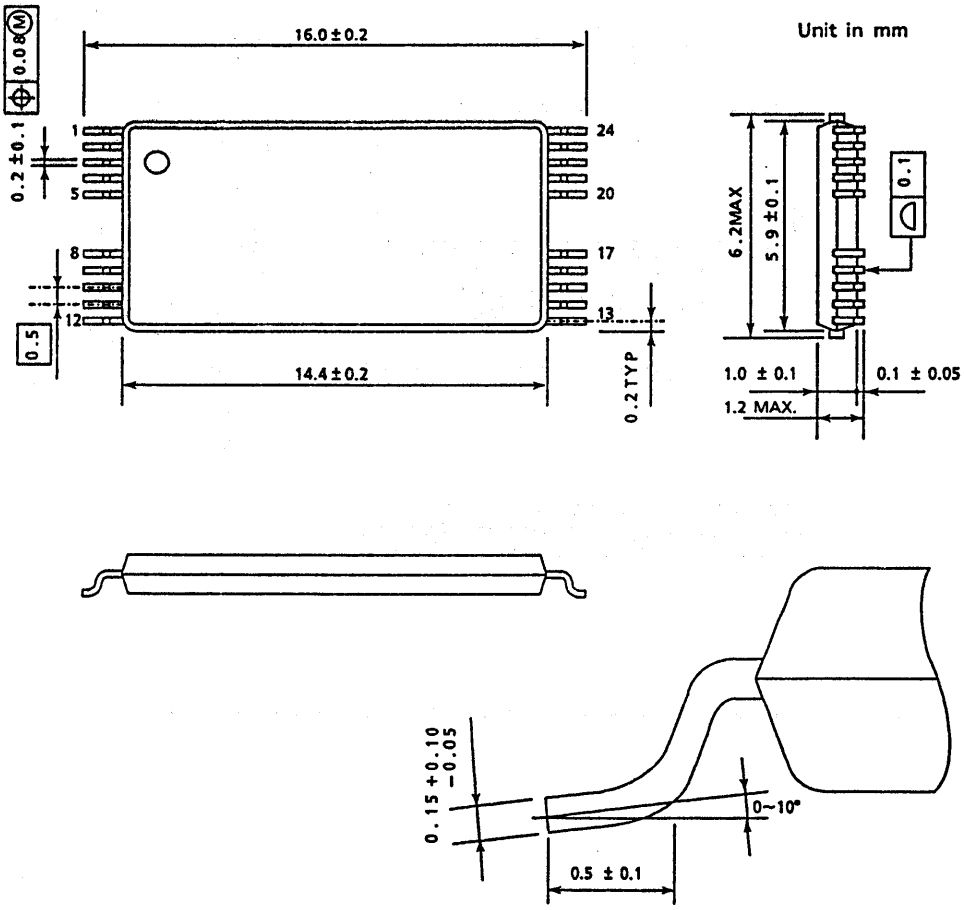
400 MIL HEIGHT ZIP OUTLINE DRAWING

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

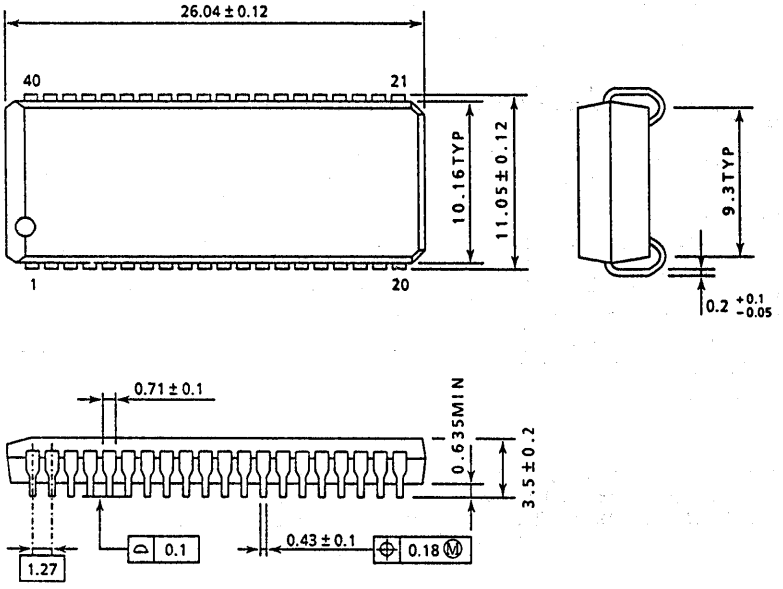
TSOP TYPE-I OUTLINE DRAWING



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

400 MIL WIDTH SOJ OUTLINE DRAWING FOR 64Kx16 DRAM'S AND 128Kx8 VRAM'S

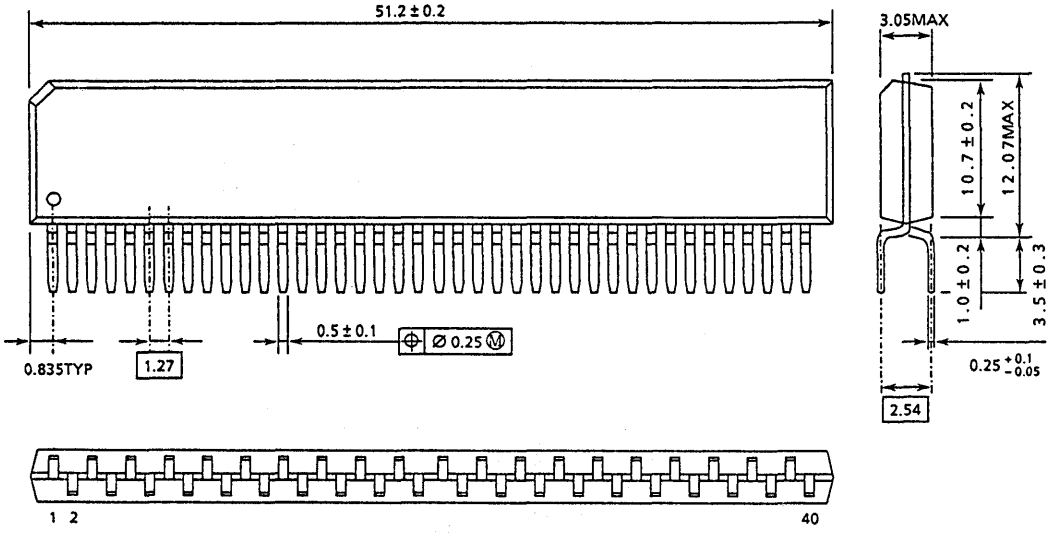
Unit in mm



Weight : 1.54g (TYP.)

475 MIL HEIGHT ZIP OUTLINE DRAWING FOR 64Kx16 DRAM'S AND 128Kx8 VRAM'S

Unit in mm



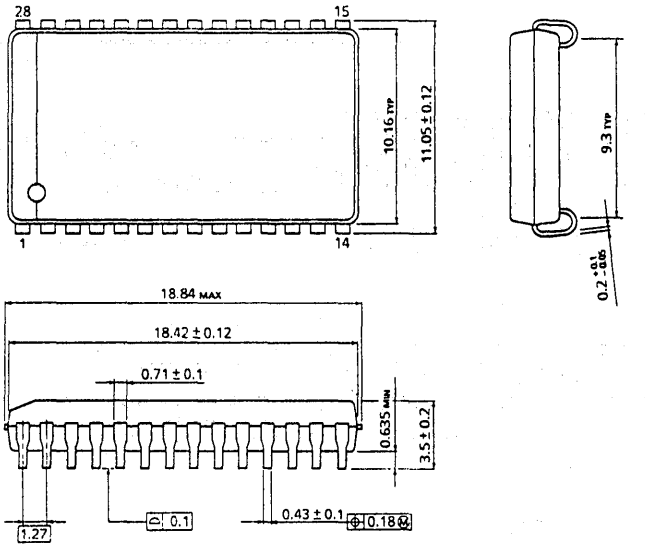
Weight : 3.35g (TYP.)

400 MIL WIDTH SOJ OUTLINE DRAWING FOR 256Kx4 VRAM'S

• Plastic SOJ

SOJ28 - P - 400

Unit : mm



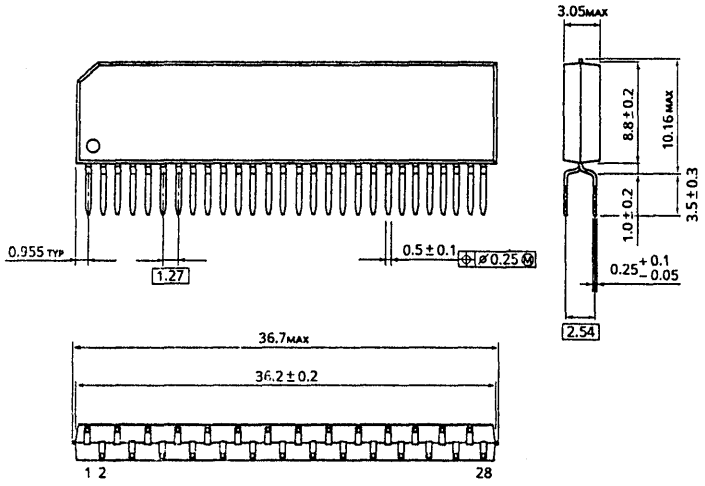
Weight : 1.13g (TYP.)

400 MIL HEIGHT ZIP OUTLINE DRAWING FOR 256Kx4 VRAM'S

• Plastic ZIP

ZIP28 - P - 400

Unit : mm



Weight : 2.01g (TYP.)

DYNAMIC RAM

1,048,576 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC511000BP/BJ/BZ/BFT is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC511000BP/BJ/BZ/BFT to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

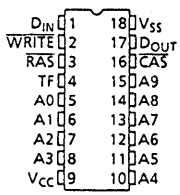
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

	TC511000BP/BJ/BZ/BFT-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CAS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{PC} Fast Page Mode Cycle Time	40ns

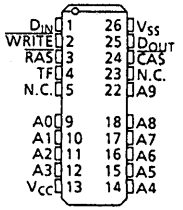
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511000BP : DIP18-P-300C
  TC511000BJ : SOJ26-P-300
  TC511000BZ : ZIP20-P-400
  TC511000BFT : TSOP24-P-0616

PIN CONNECTION

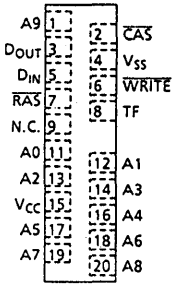
Plastic DIP



Plastic SOJ



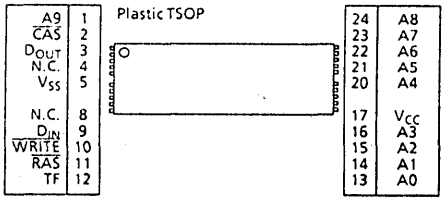
Plastic ZIP



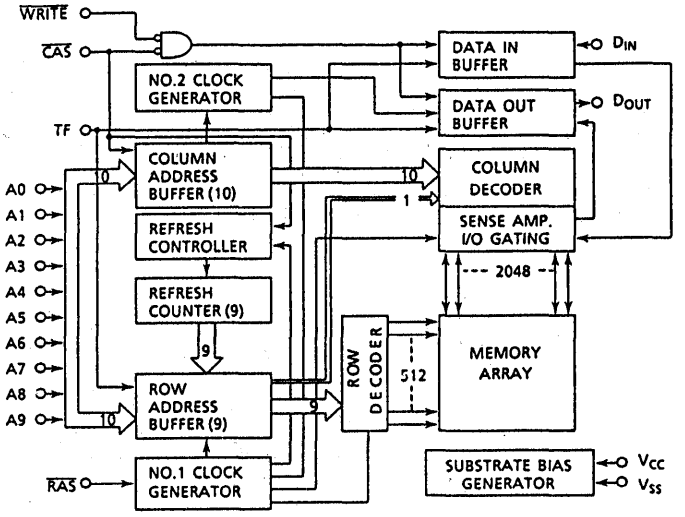
PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0	−	V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511000BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511000BP/BJ/BZ/BFT-60	–	90	mA	3,5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511000BP/BJ/BZ/BFT-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511000BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≤ $V_{IN\ (TF)}$ ≤ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≤ $V_{IN\ (TF)}$ ≤ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511000BP/BJ/BZ/BFTL-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	65	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	9,14
t_{AA}	Access Time from Column Address	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC511000BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	35	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

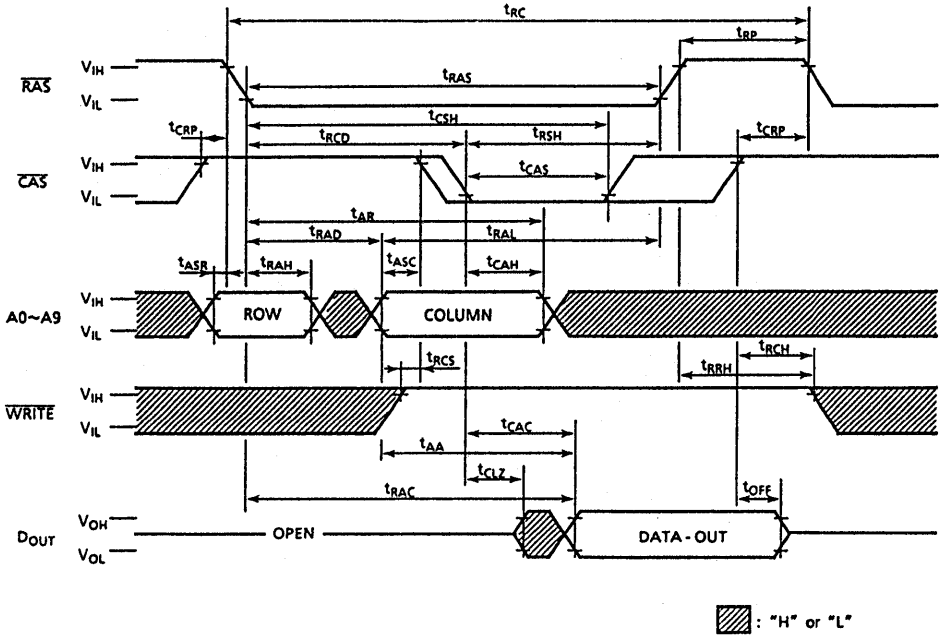
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

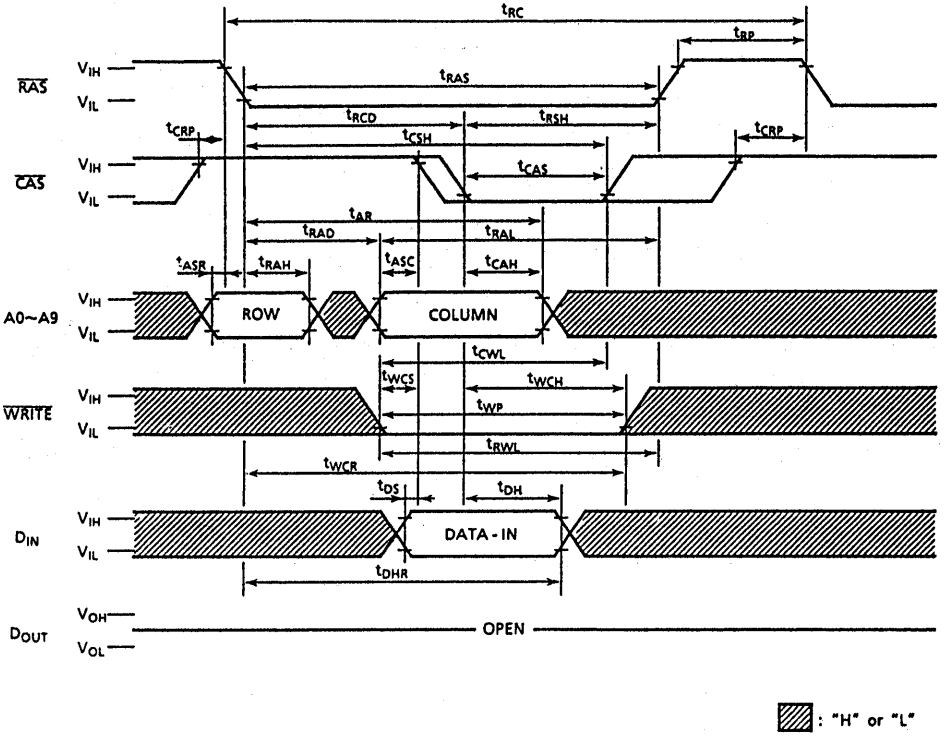
TIMING WAVEFORMS

READ CYCLE



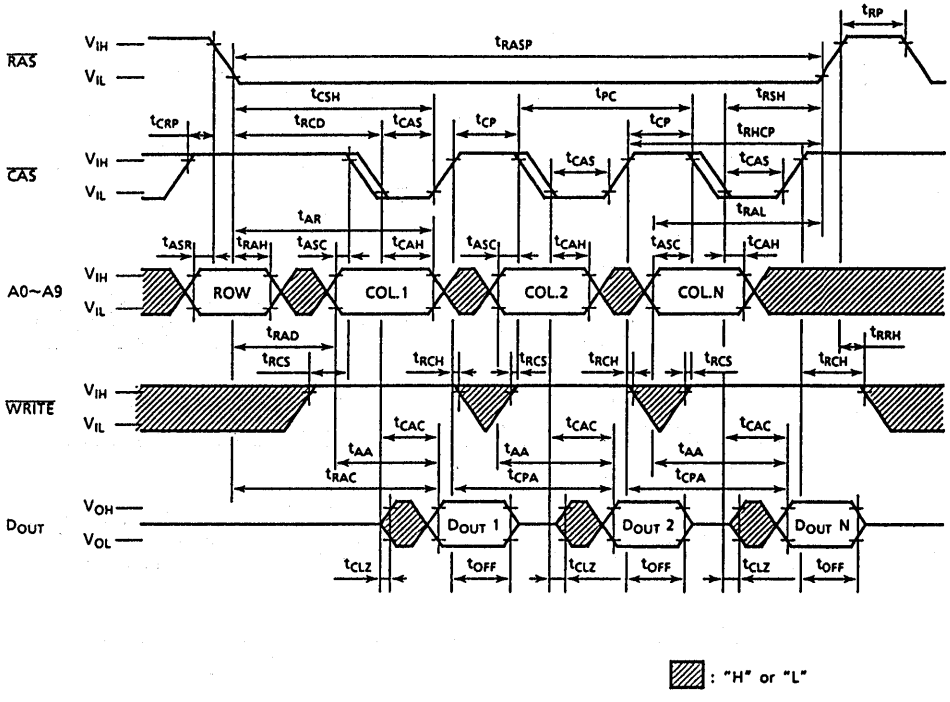
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



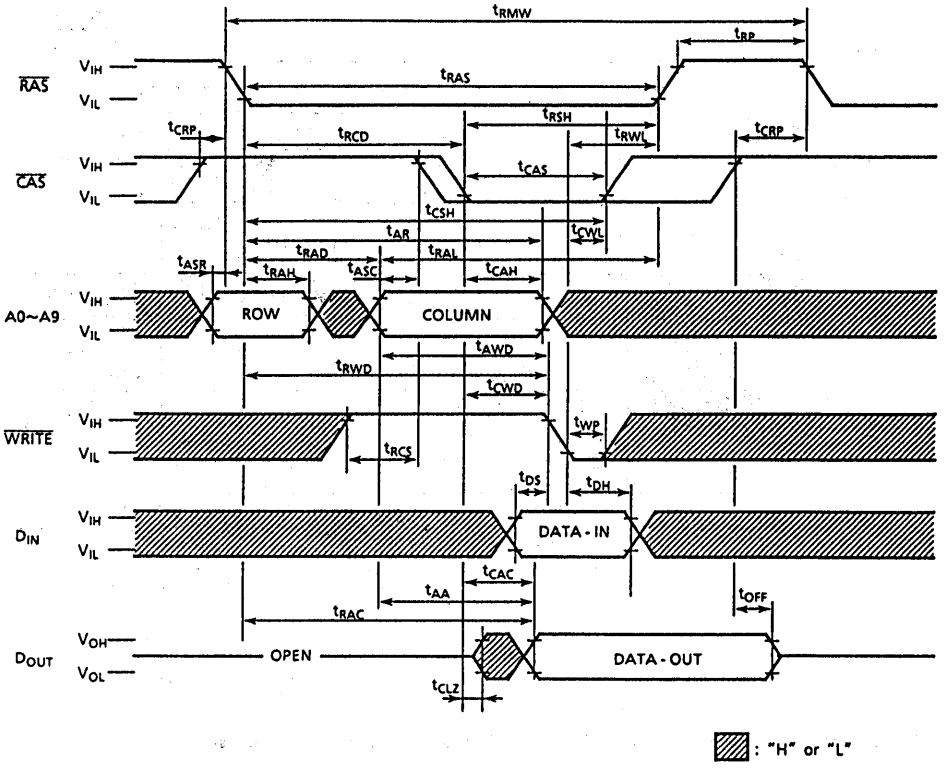
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



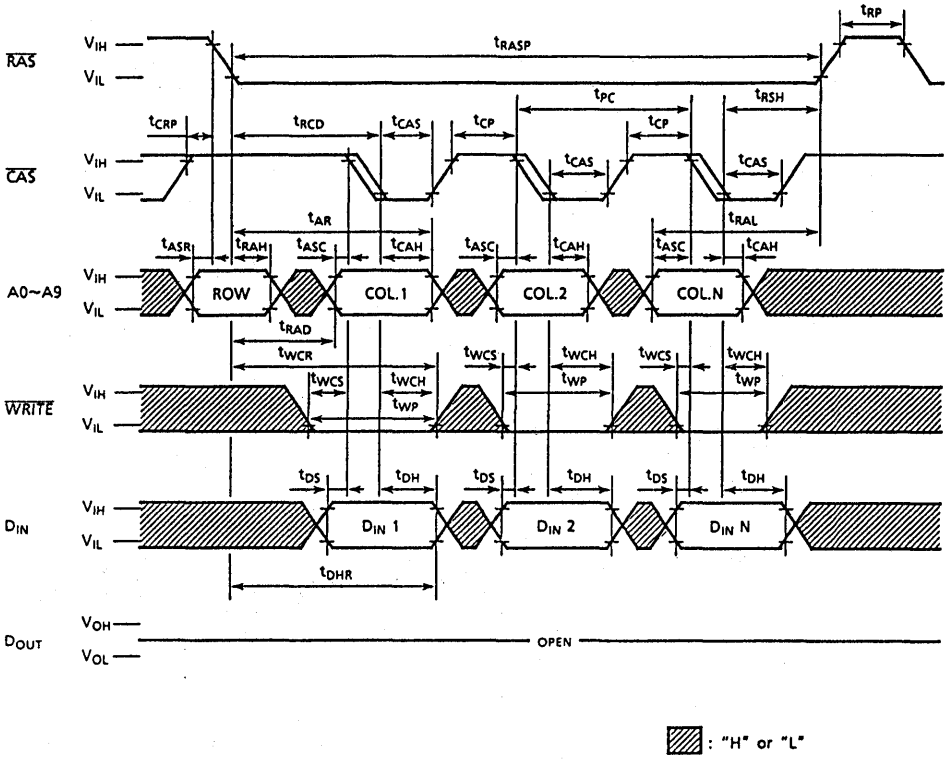
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE



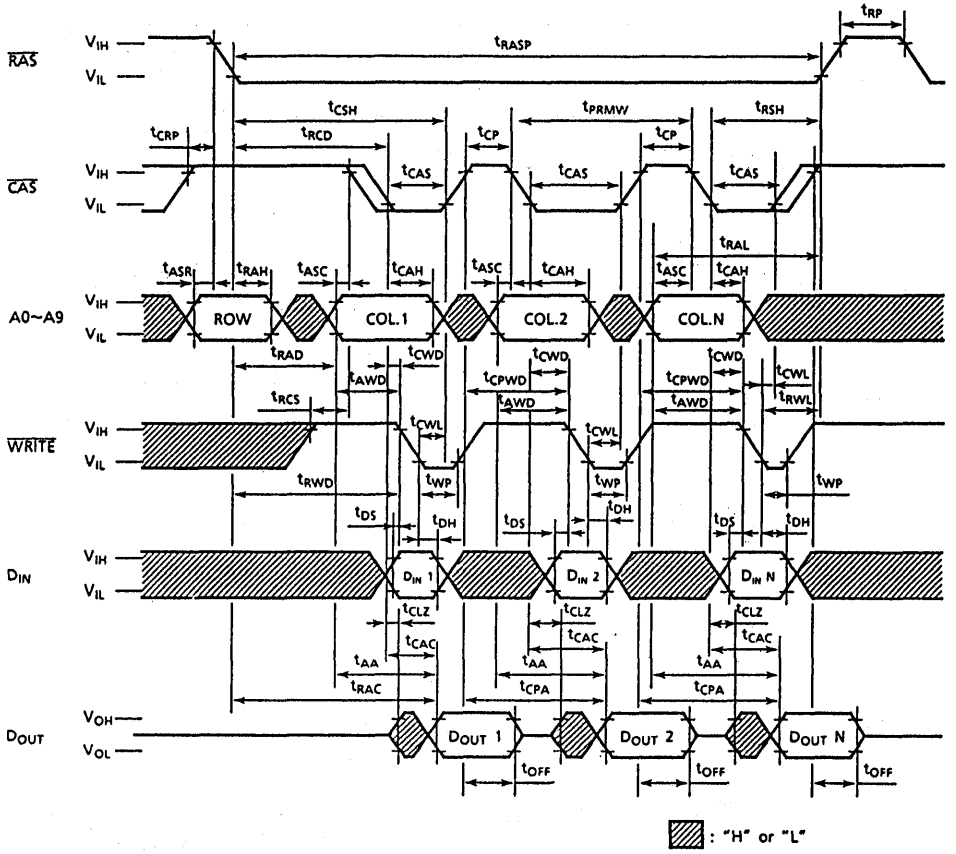
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



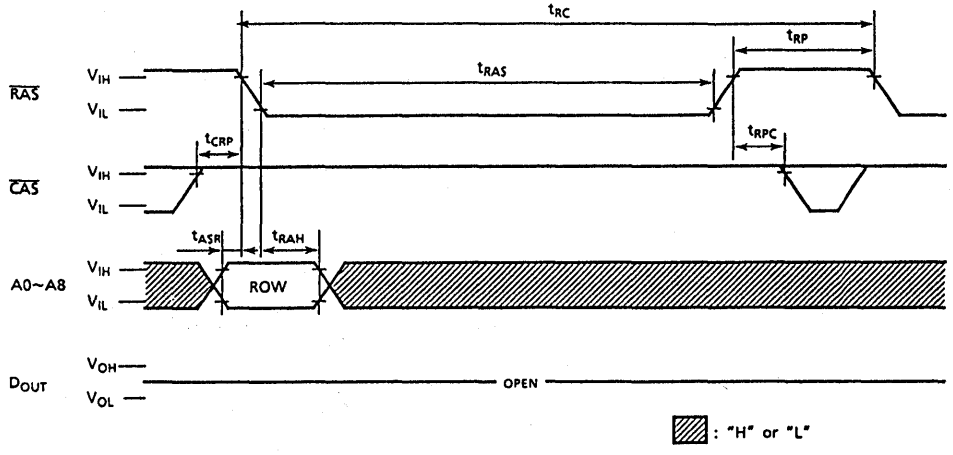
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



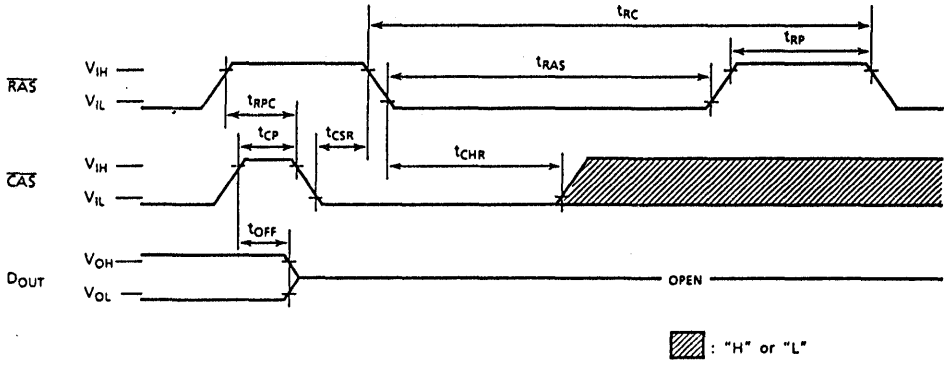
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



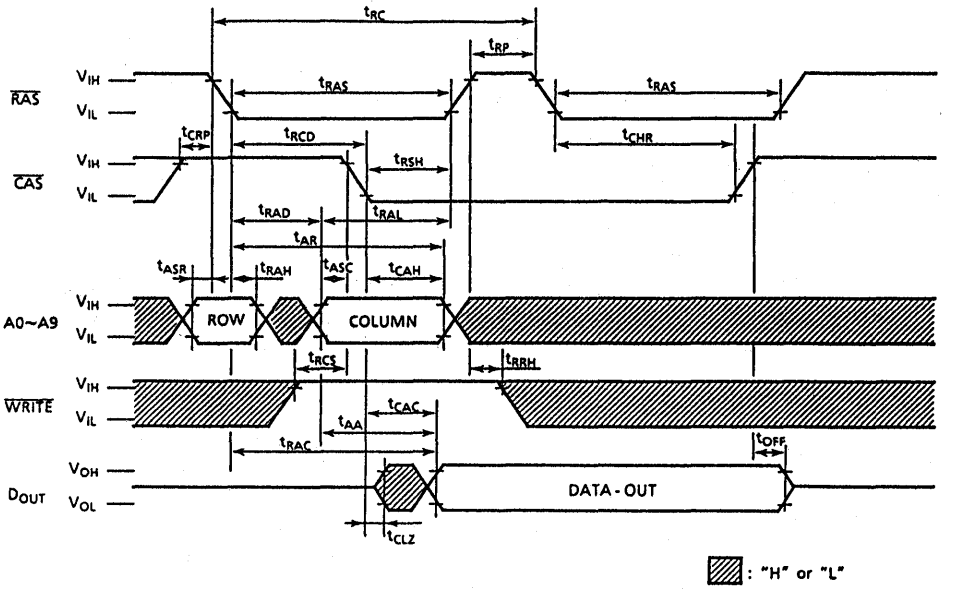
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



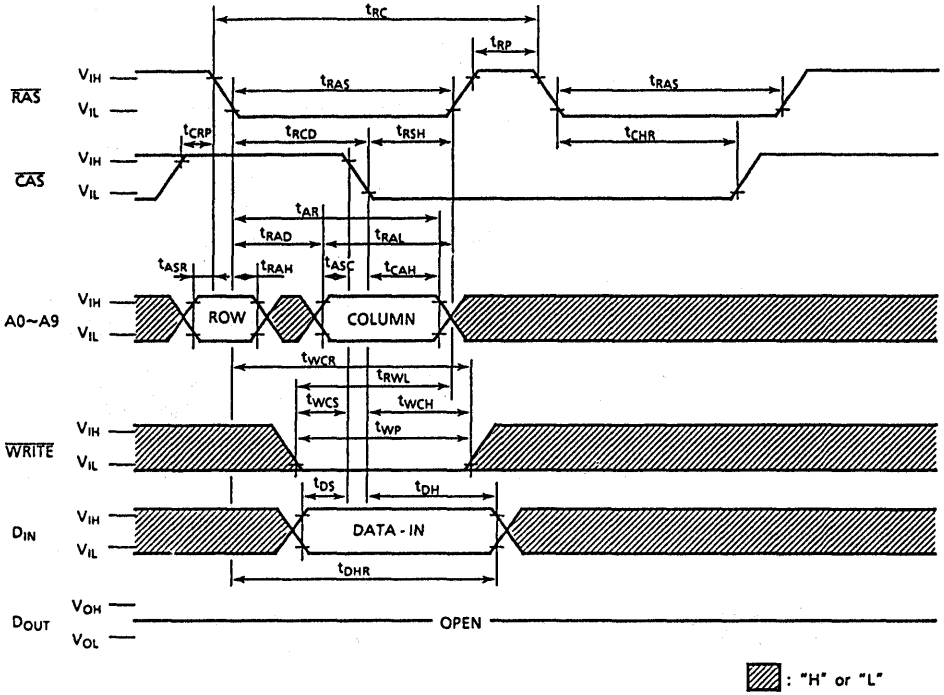
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



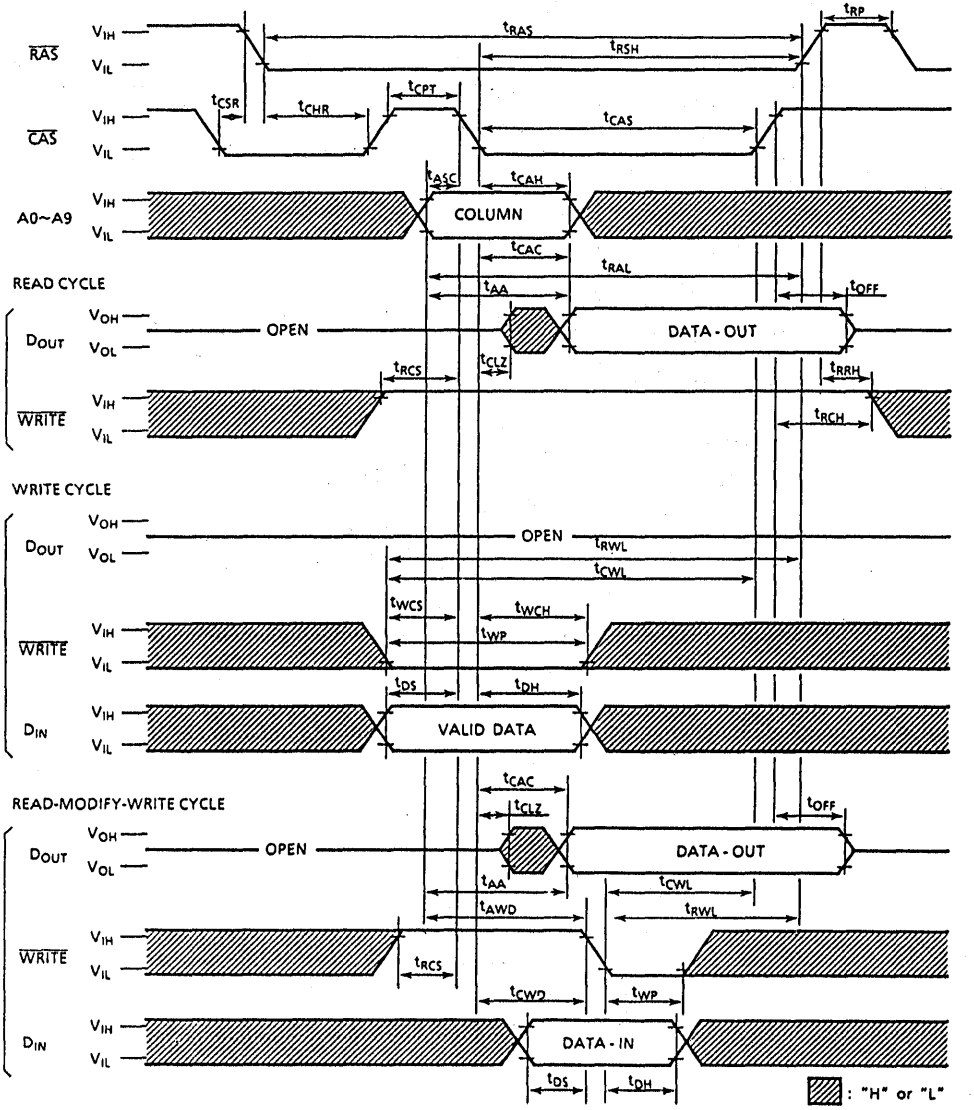
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



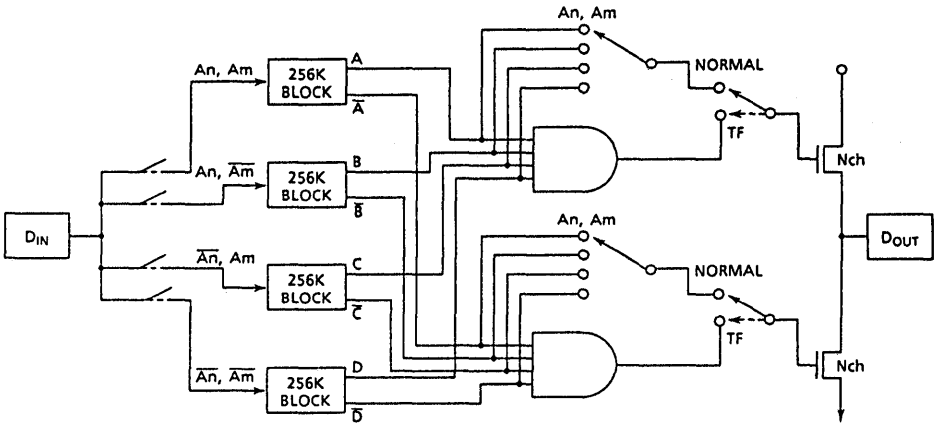
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

TEST MODE

The TC511000BP/BJ/BZ/BFT is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511000BP/BJ/BZ/BFT including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Fast Page Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

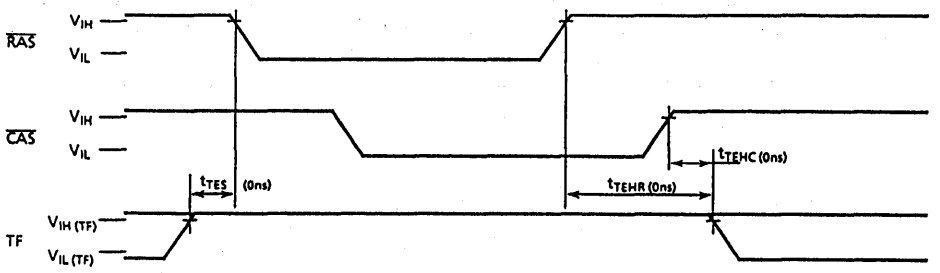


Fig. 2 Test Mode Cycle

PRELIMINARY

DESCRIPTION

The TC511000BPL/BJL/BZL/BFTL is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000BPL/BJL/BZL/BFTL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000BPL/BJL/BZL/BFTL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

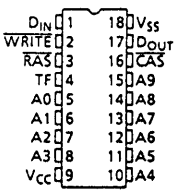
- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000BPL/BJL/BZL/BFTL-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

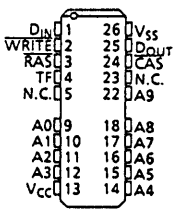
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  1.1mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test capability
- All inputs and output TTL compatible
- 512 refresh cycles/64ms
- Package TC511000BPL : DIP18-P-300C
  TC511000BJL : SOJ26-P-300
  TC511000BZL : ZIP20-P-400
  TC511000BFTL: TSOP24-P-0616

PIN CONNECTION

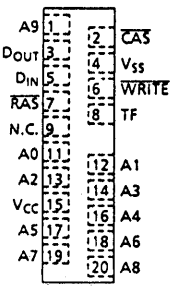
Plastic DIP



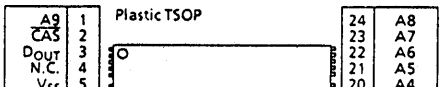
Plastic SOJ



Plastic ZIP



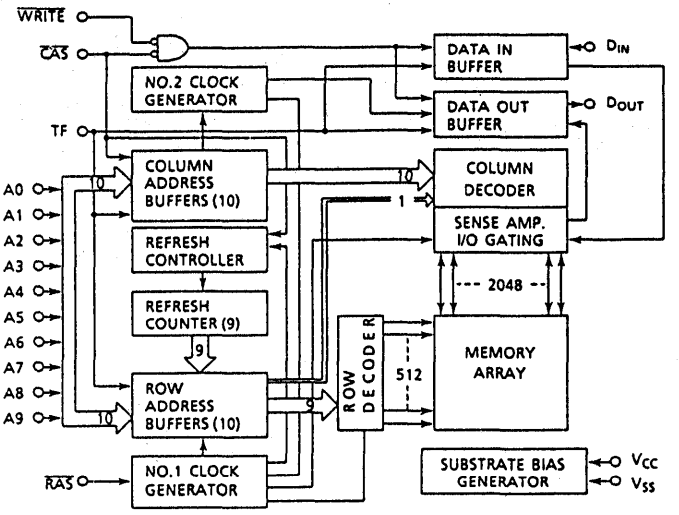
Plastic TSOP



PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0	−	V_{CC} + 1.0	V	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC5110008PL/BJL/BZL/BFTL-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	10,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	30	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	12
t_{WCH}	Write Command Hold Time	10	-	ns	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511000BPL/BJL/BZL/BFTL-60	-	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511000BPL/BJL/BZL/BFTL-60	-	90	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC511000BPL/BJL/BZL/BFTL-60	-	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		-	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511000BPL/BJL/BZL/BFTL-60	-	90	mA	3
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, BATTERY BACK UP MODE ($\overline{CAS} = \overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE} = V_{CC} - 0.2V$ or 0.2V, A0~9 = $V_{CC} - 0.2V$ or 0.2V, $D_{IN} = V_{CC} - 0.2V$ or OPEN : t_{RC} = 125µs, $t_{RAS} = t_{RAS}$ MIN. ~1µs)		-	300	µA	3, 6
$I_I(L)$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		- 10	10	µA	
$I_{ITF}(L)$	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN}$ (TF) $\leq V_{CC} + 0.5V$, All Other Pins Not Under Test = 0V)		- 10	10	µA	
$I_O(L)$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		- 10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN}$ (TF) $\leq 10.5V$)		-	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = - 5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC511000BPL/BJL/BZL/BFTL-60		UNITS	NOTES
		MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	ns	13
t_{DH}	Data Hold Time	15	-	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{REF}	Refresh Period	-	64	ms	
t_{WCS}	Write Command Set-Up Time	0	-	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	35	-	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

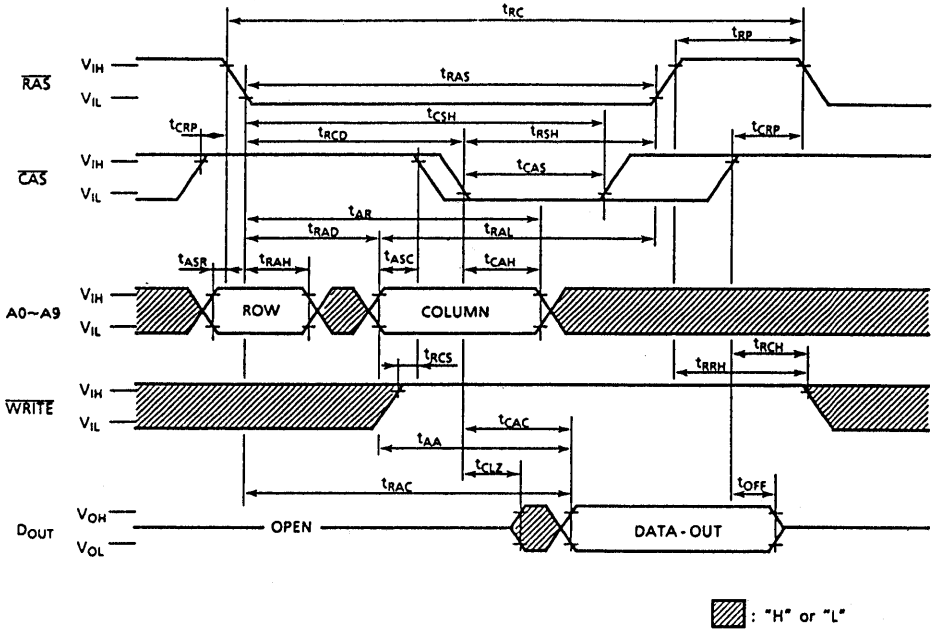
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
8. AC measurements assume t_T = 5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

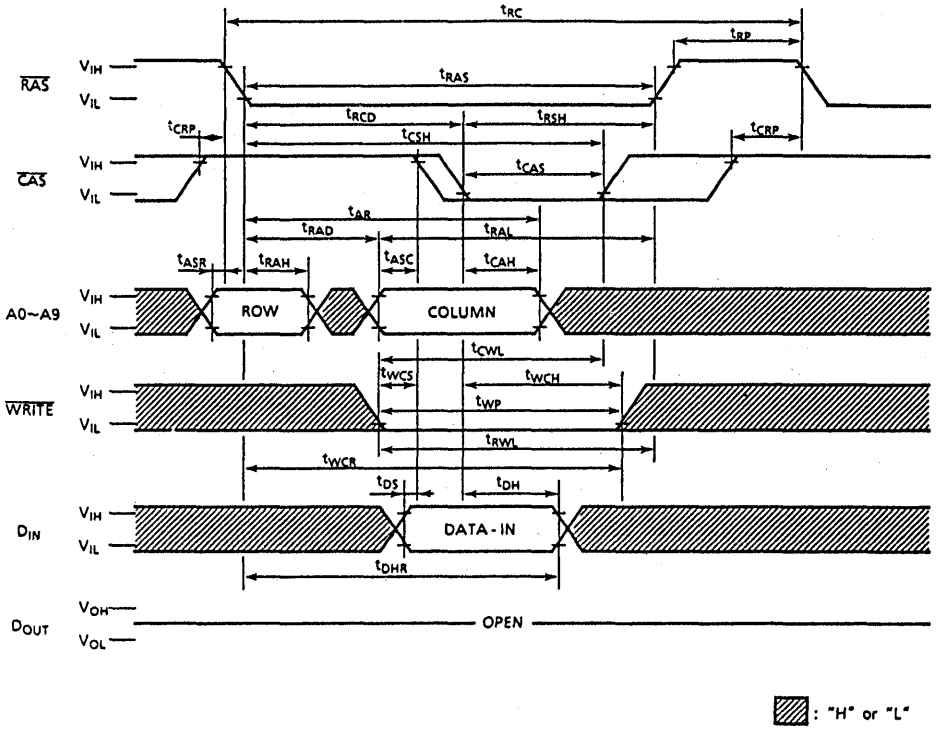
TIMING WAVEFORMS

READ CYCLE



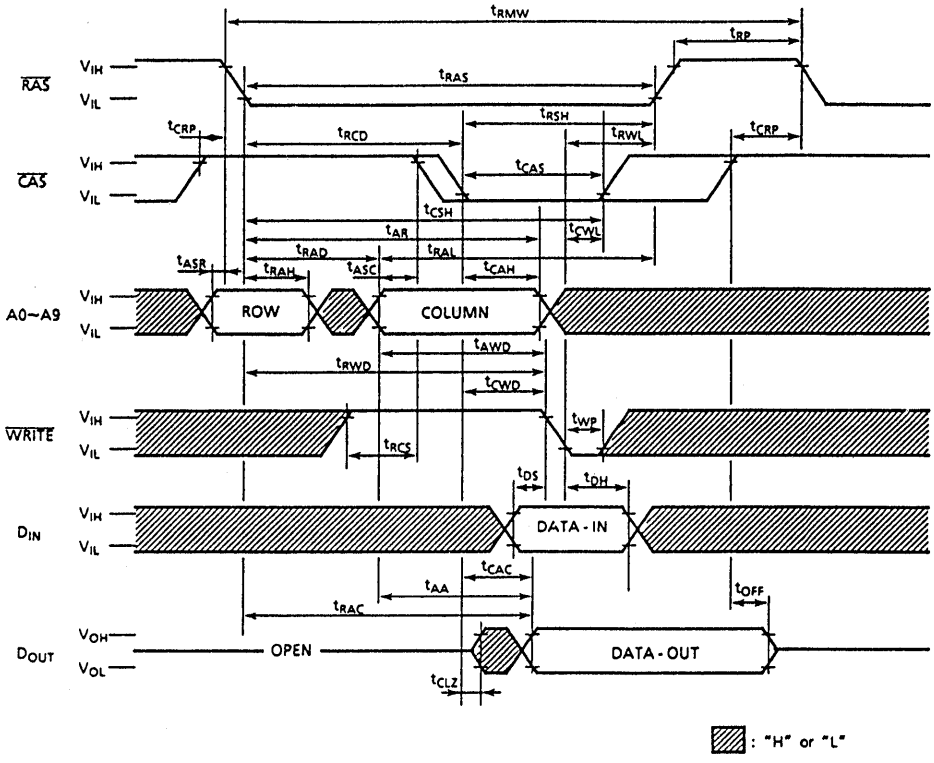
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



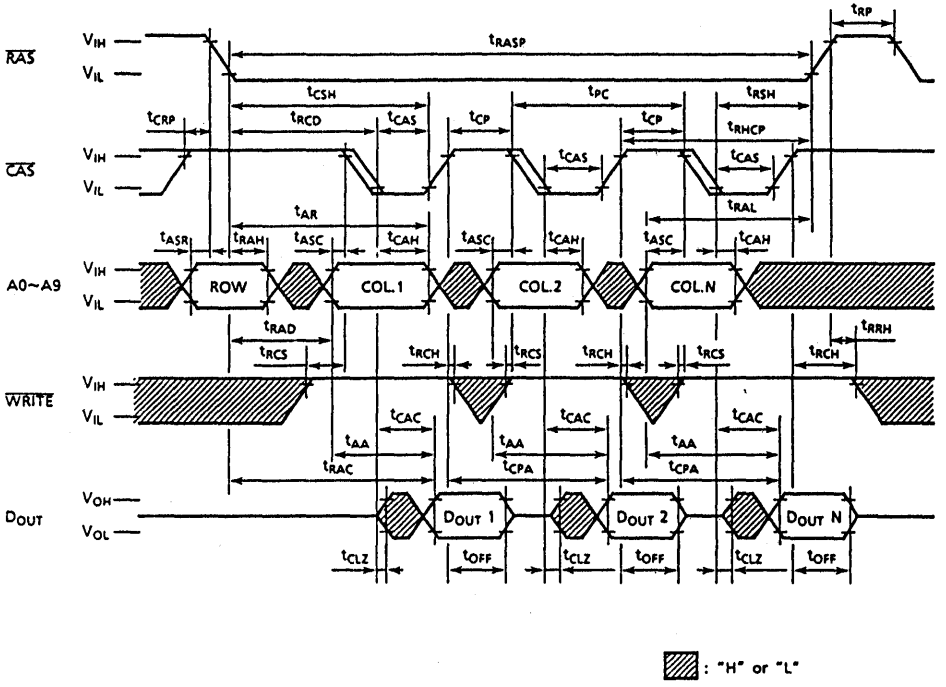
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE



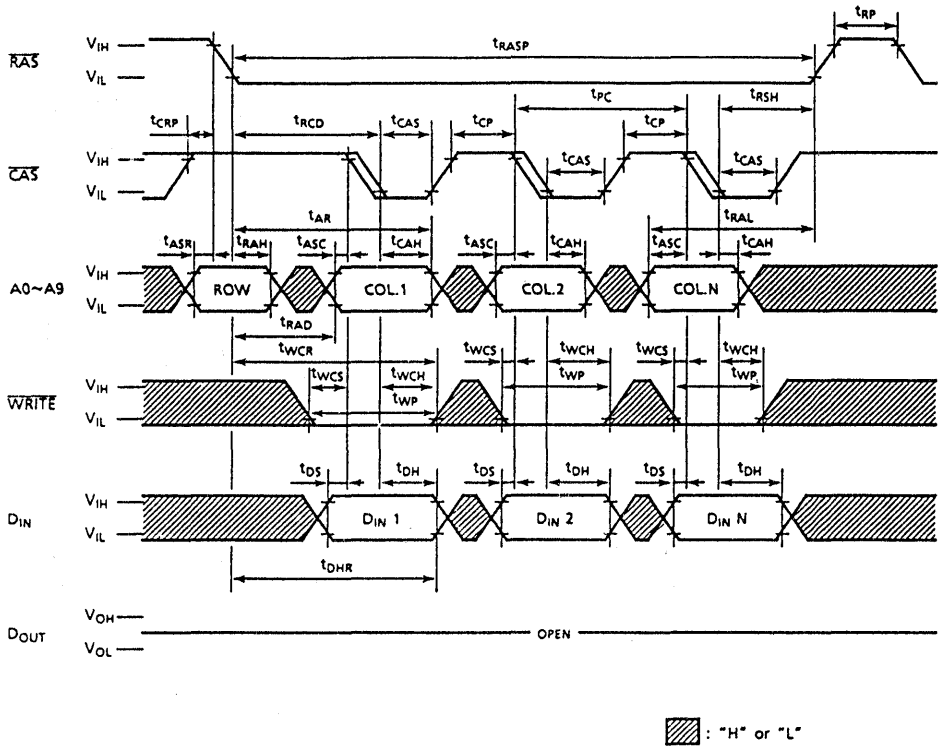
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



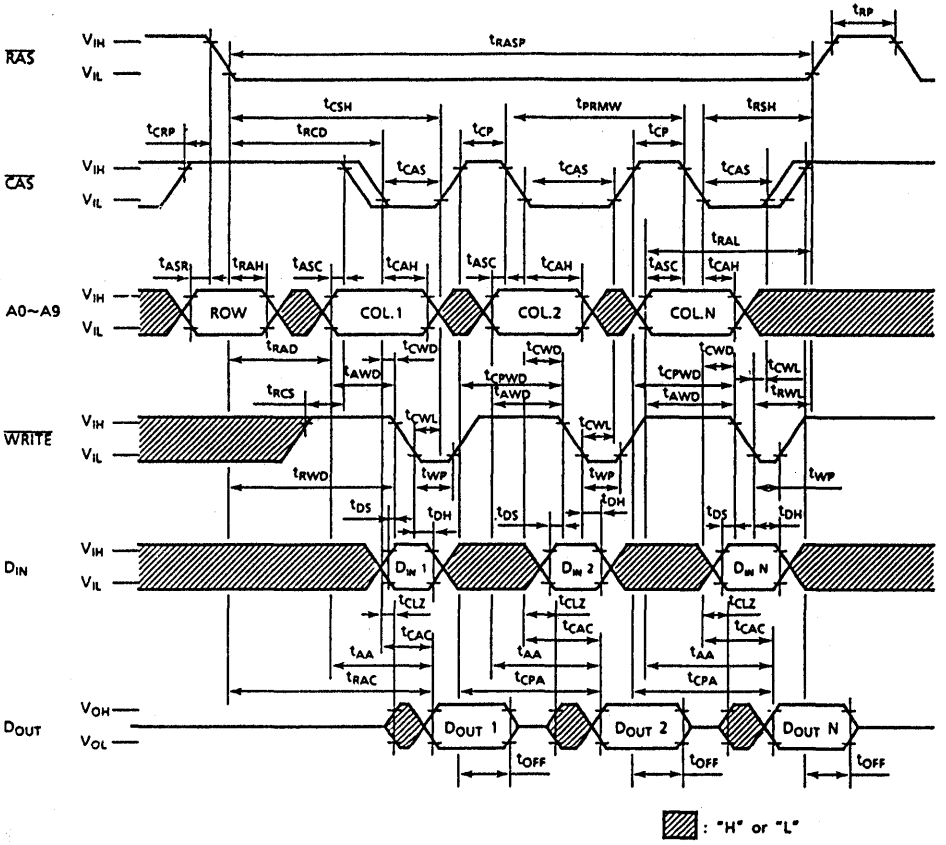
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



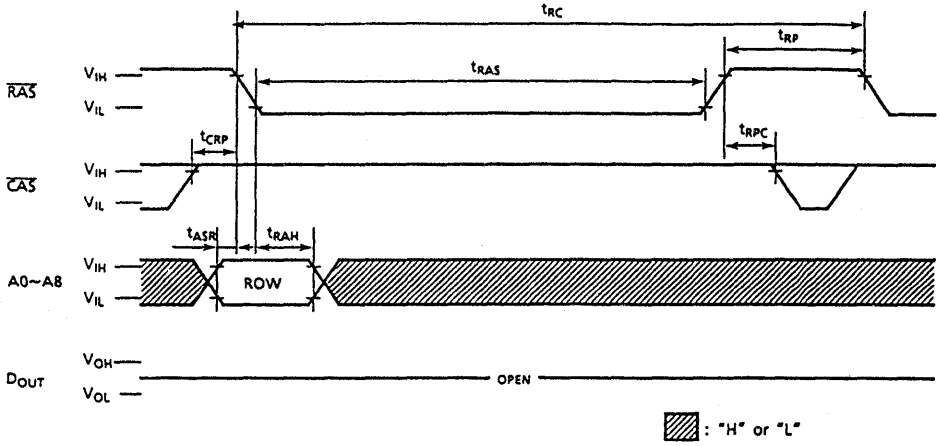
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



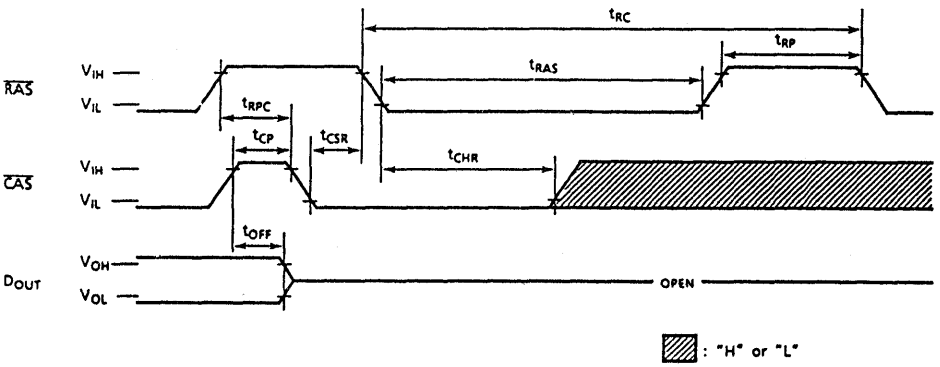
NOTE: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



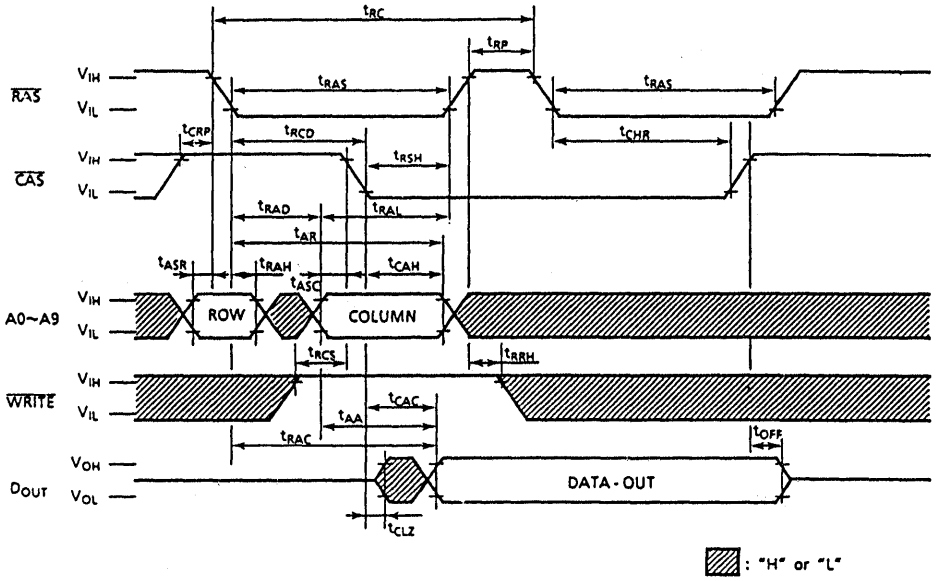
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



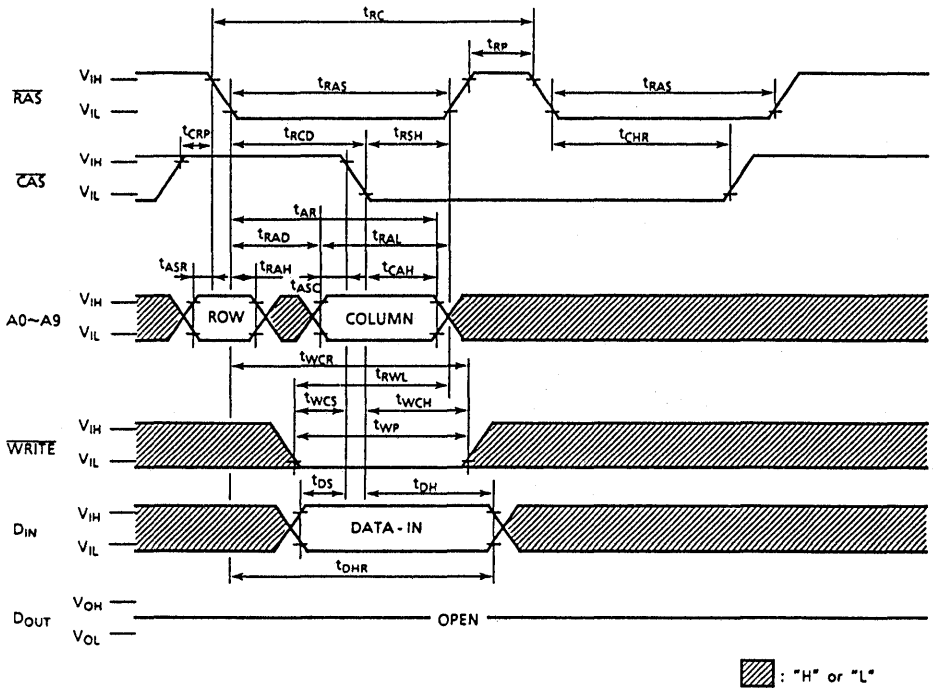
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



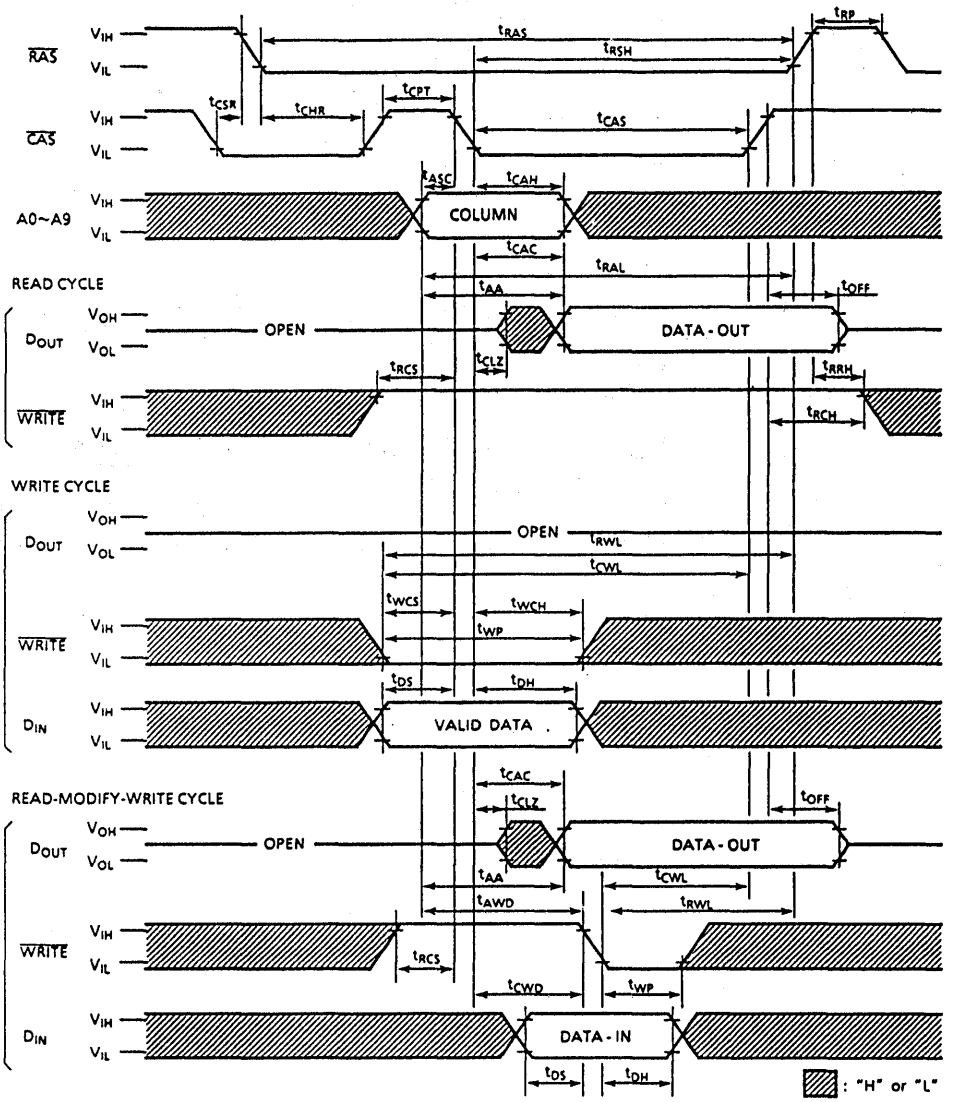
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



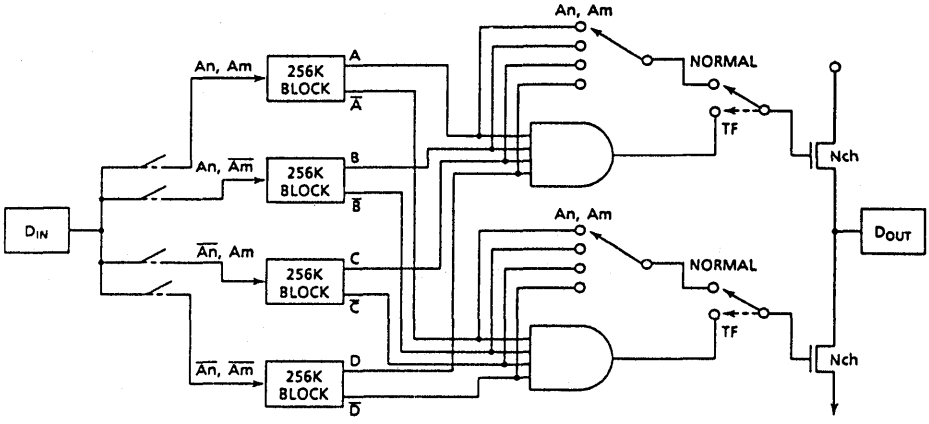
Note: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

TEST MODE

The TC511000BPL/BJL/BZL/BFTL is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H"or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511000BPL/BJL/BZL/BFTL including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi – Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Fast Page Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

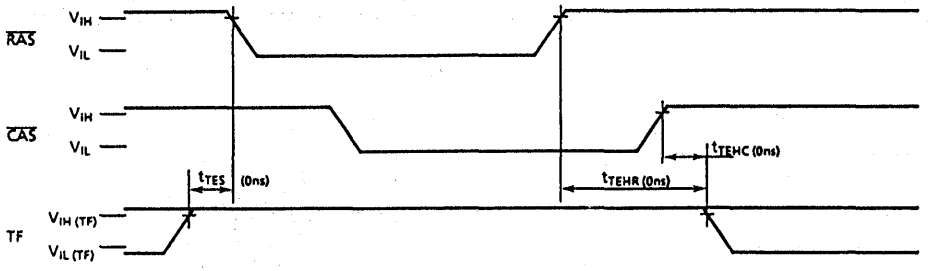


Fig. 2 Test Mode Cycle

TENTATIVE DATA
1,048,576 WORD × 1 BIT DYNAMIC RAM

DESCRIPTION

The TC511000AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511000AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 1bit organization
- Fast access time and cycle time

		TC511000AP/AJ/AZ-70/80/10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator

Low Power
440mW MAX. Operating (TC511000AP/AJ/AZ-70)
385mW MAX. Operating (TC511000AP/AJ/AZ-80)
330mW MAX. Operating (TC511000AP/AJ/AZ-10)
5.5mW MAX. Standby

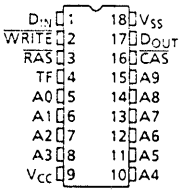
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511000AP : DIP18-P-300C
  TC511000AJ : SOJ26-P-300
  TC511000AZ : ZIP20-P-400

PIN NAMES

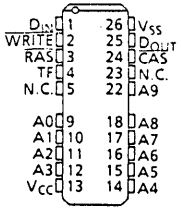
A0~A9	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	TF	Test Function
$\overline{CAS}$	Column Address Strobe	N.C.	No Connection

PIN CONNECTION

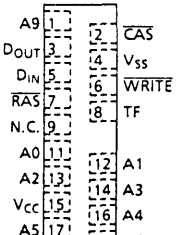
Plastic DIP



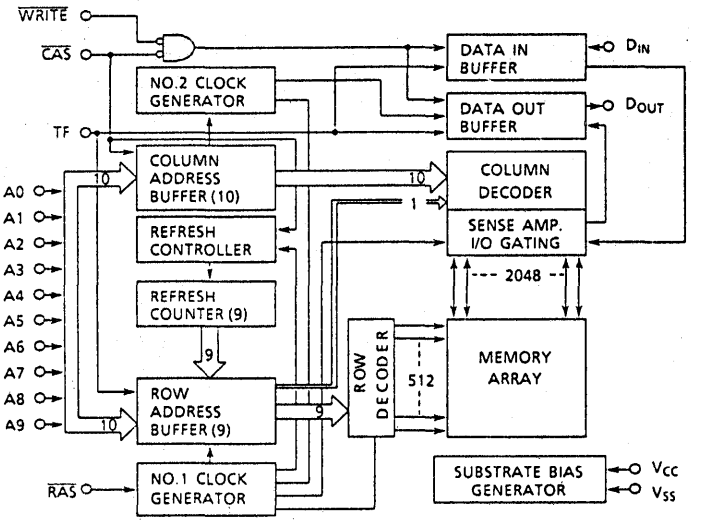
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0	−	V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511000AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC511000AP/AJ/AZ-80	–	70		
		TC511000AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511000AP/AJ/AZ-70	–	80	mA	3, 5
		TC511000AP/AJ/AZ-80	–	70		
		TC511000AP/AJ/AZ-10	–	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511000AP/AJ/AZ-70	–	60	mA	3, 4, 5
		TC511000AP/AJ/AZ-80	–	50		
		TC511000AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511000AP/AJ/AZ-70	–	80	mA	3
		TC511000AP/AJ/AZ-80	–	70		
		TC511000AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≦ $V_{IN\ (TF)}$ ≦ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≦ $V_{IN\ (TF)}$ ≦ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC511000AP/ AJ/AZ-70		TC511000AP/ AJ/AZ-80		TC511000AP/ AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	65	–	70	–	85	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	50	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	CHARACTERISTIC	TC511000AP/AJ/AZ-70		TC511000AP/AJ/AZ-80		TC511000AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

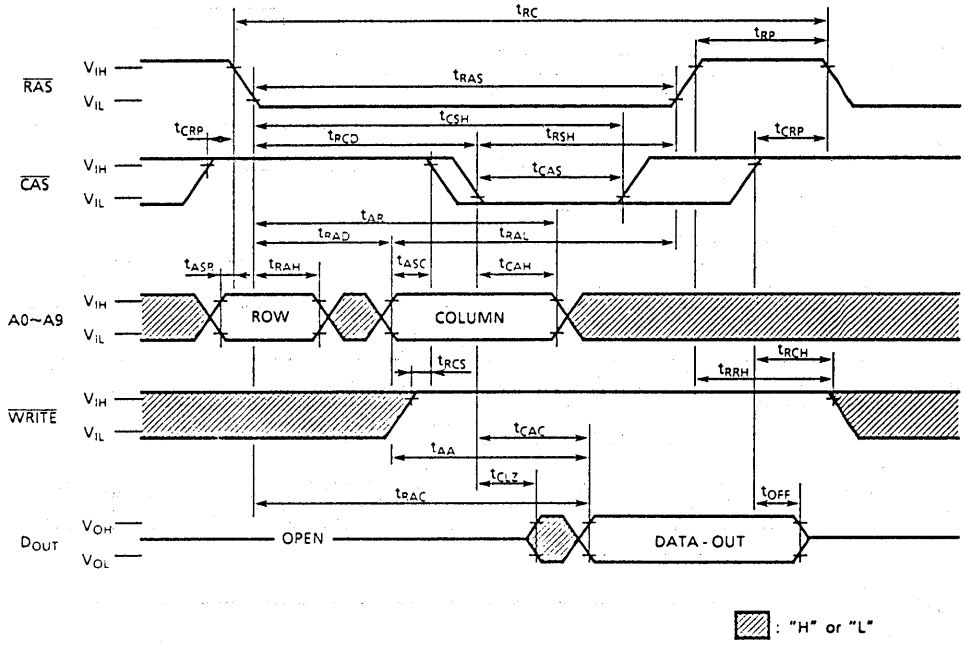
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

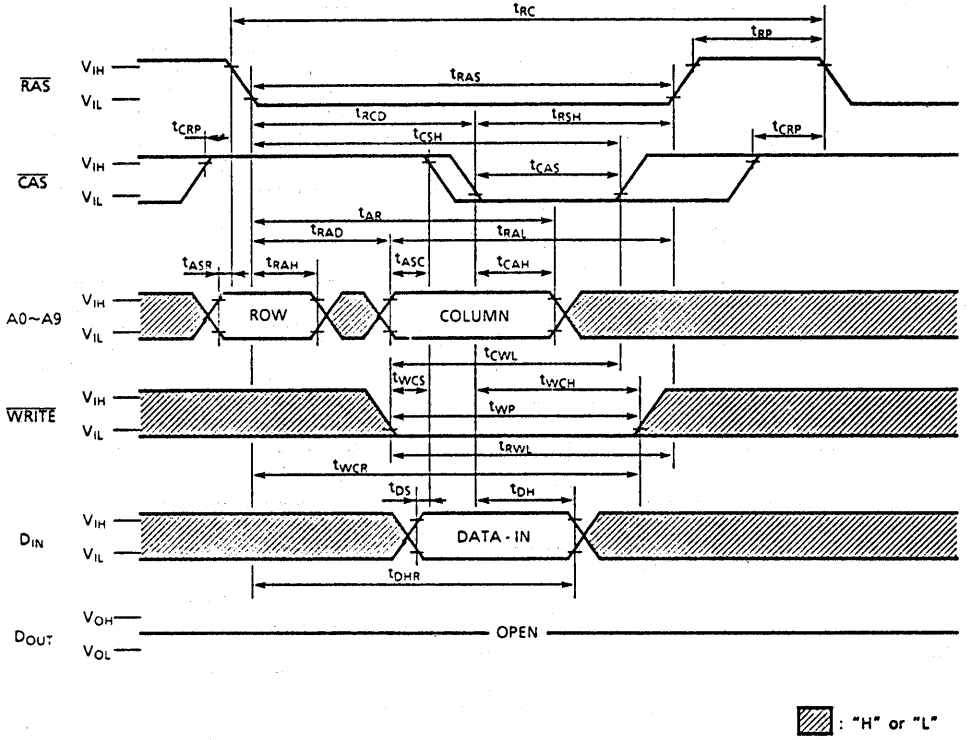
TIMING WAVEFORMS

READ CYCLE



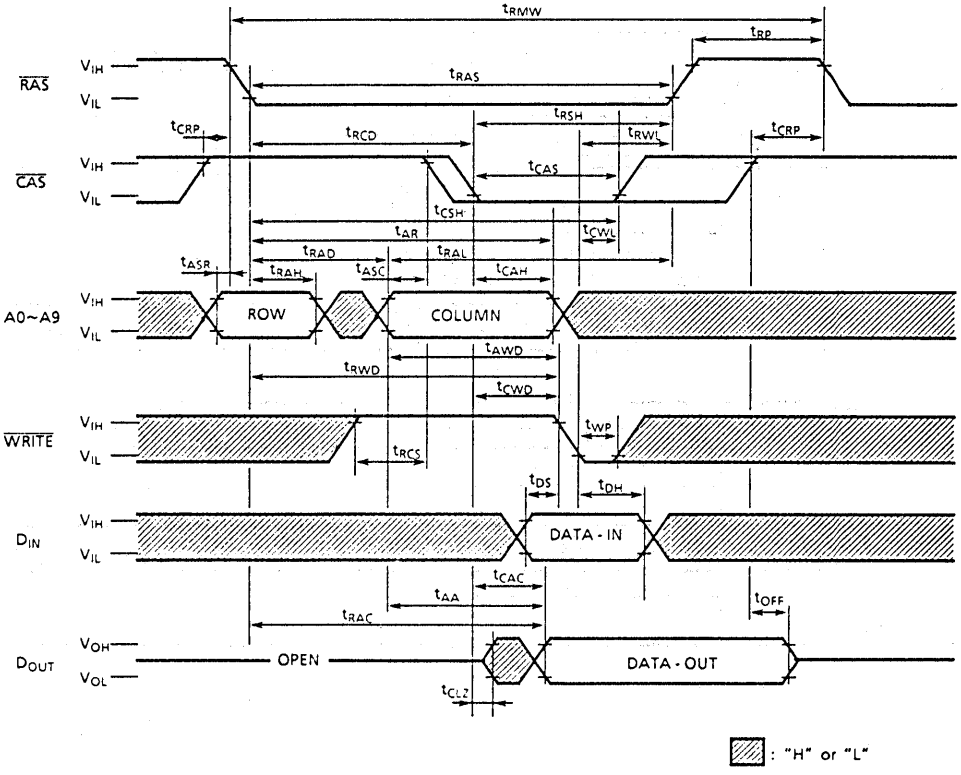
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



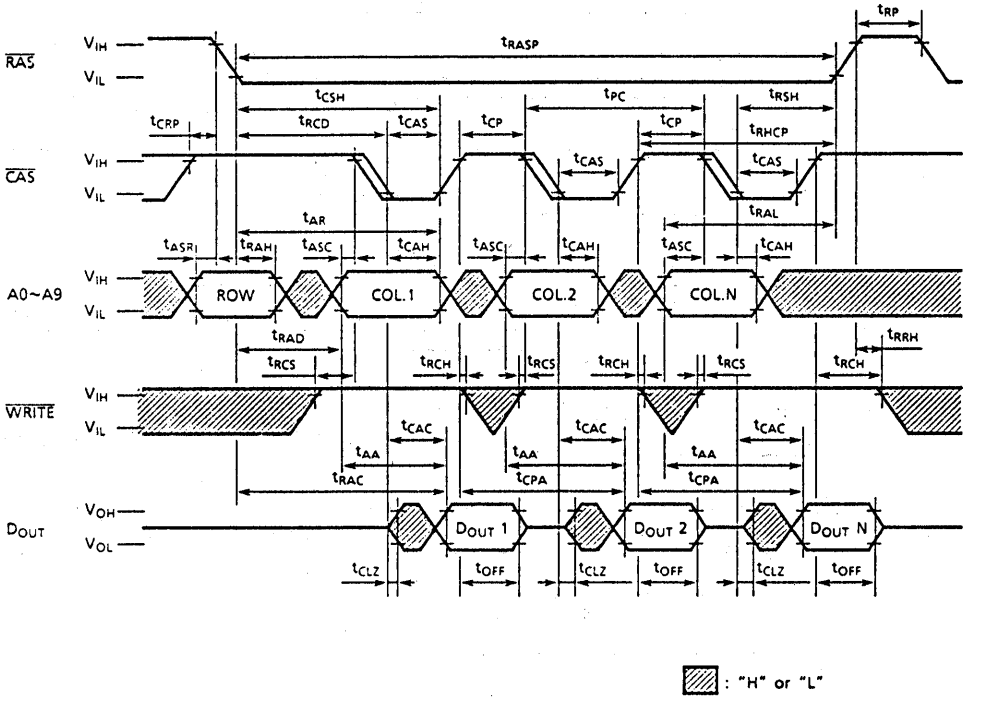
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE



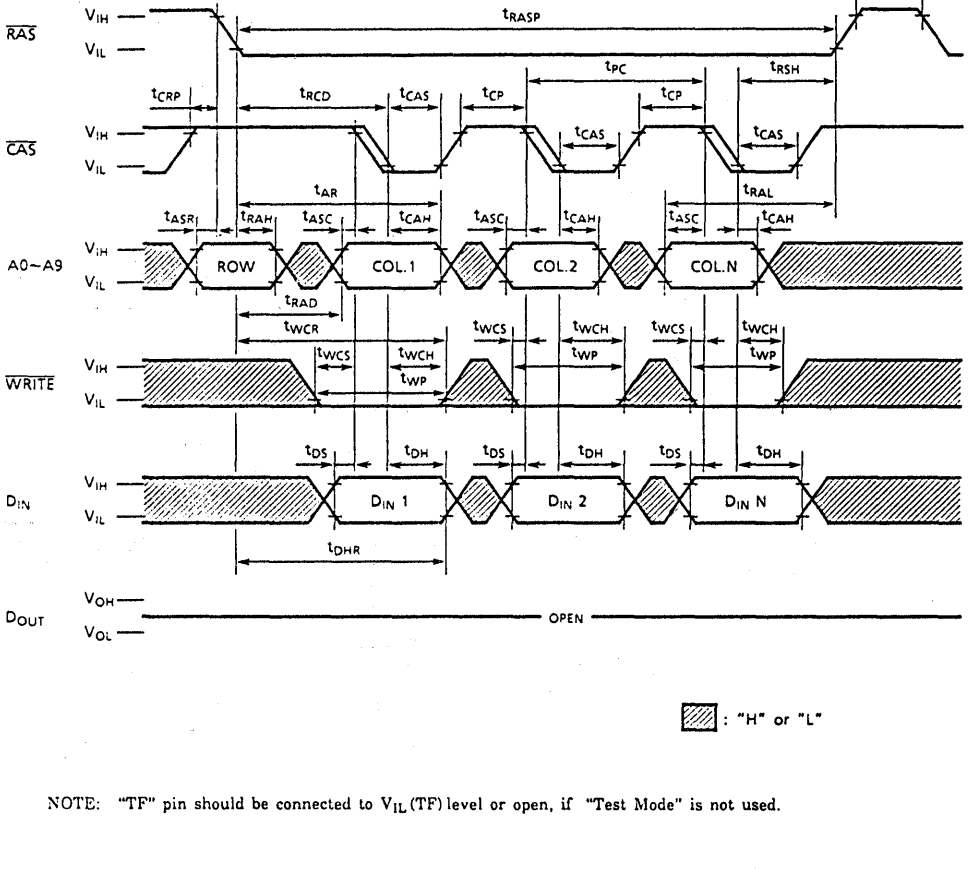
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



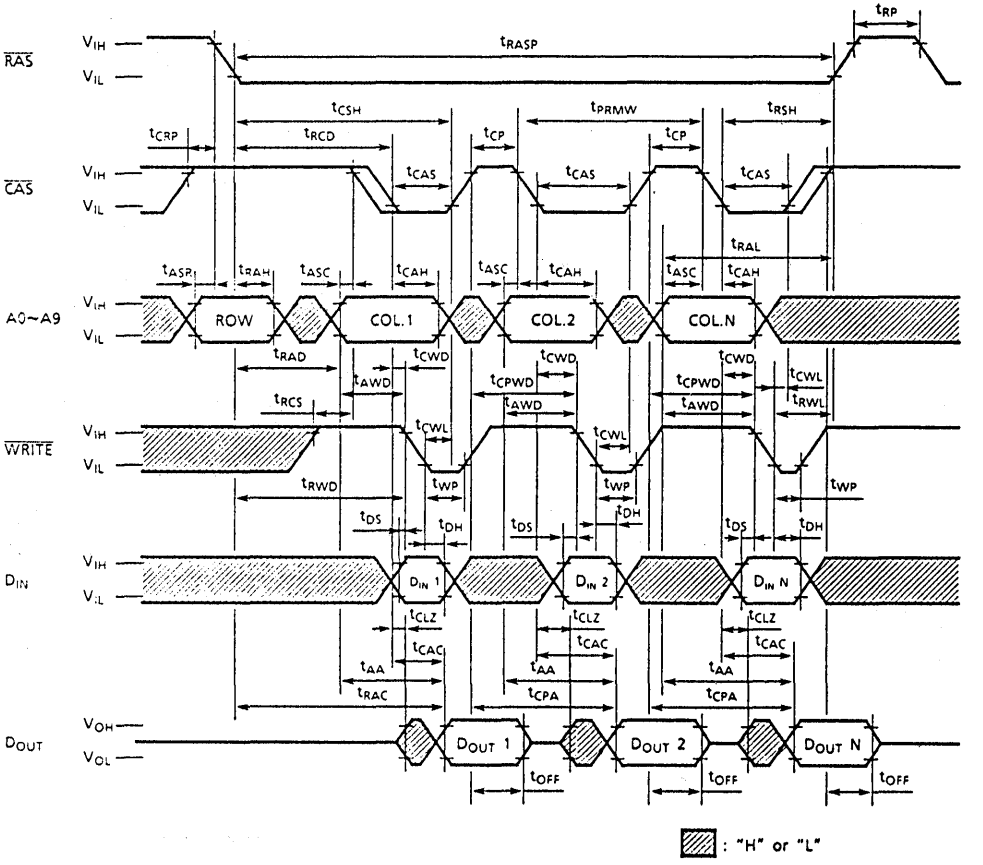
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



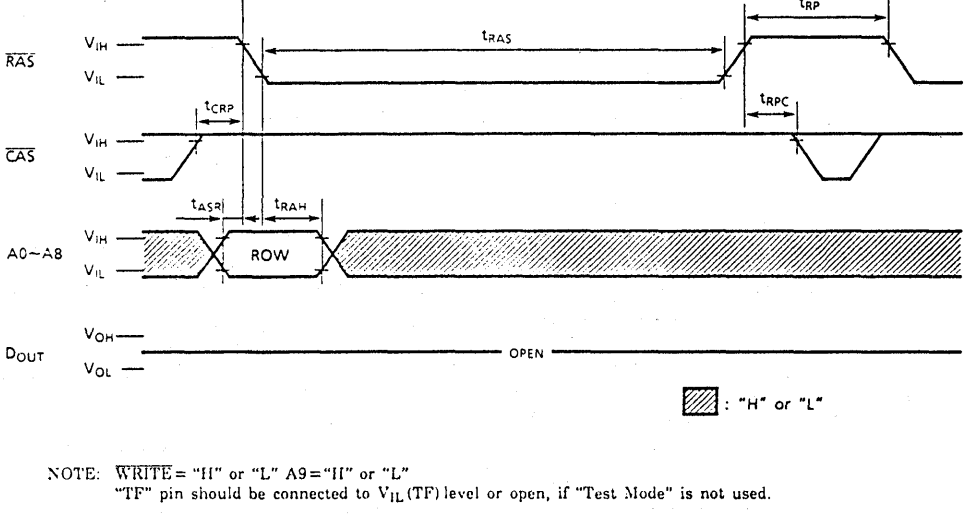
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



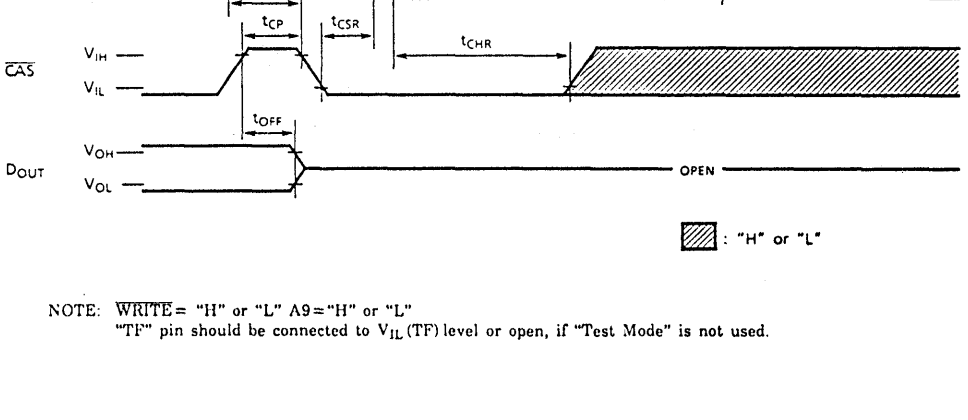
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



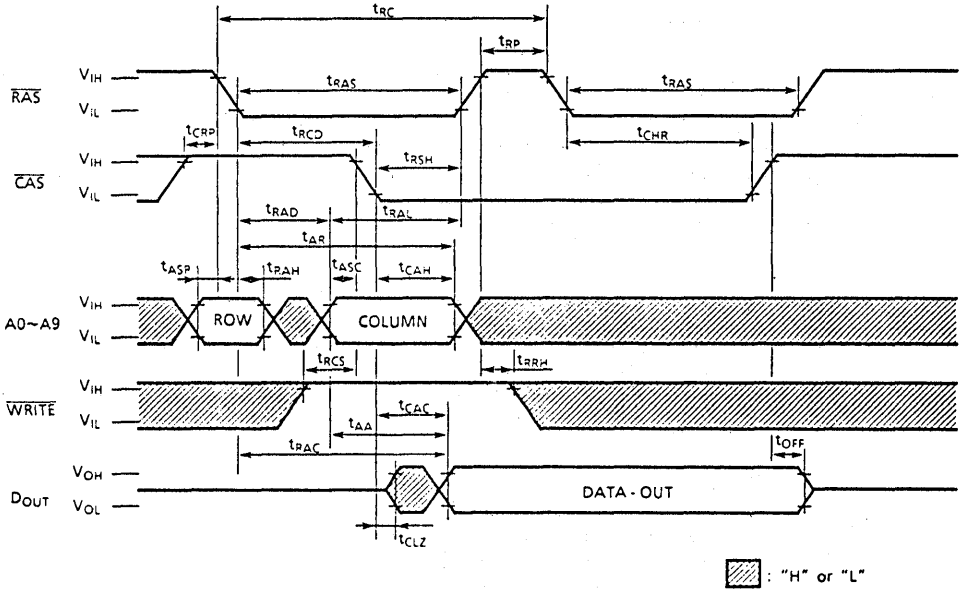
NOTE: $\overline{WRITE}$ = "H" or "L" A9="H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



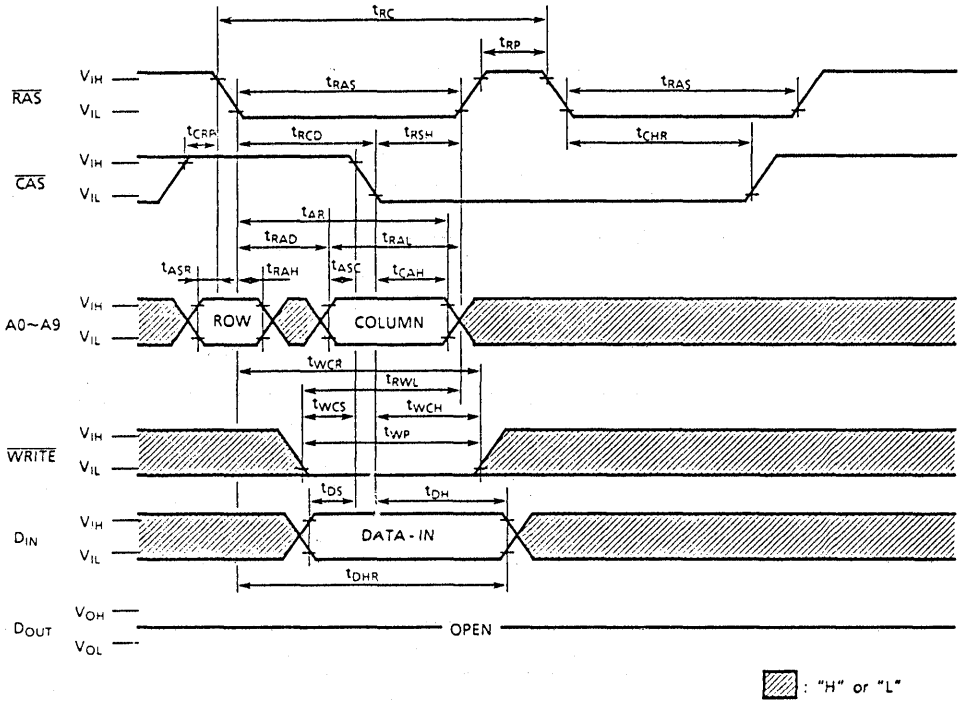
NOTE: $\overline{WRITE}$ = "H" or "L" A9="H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



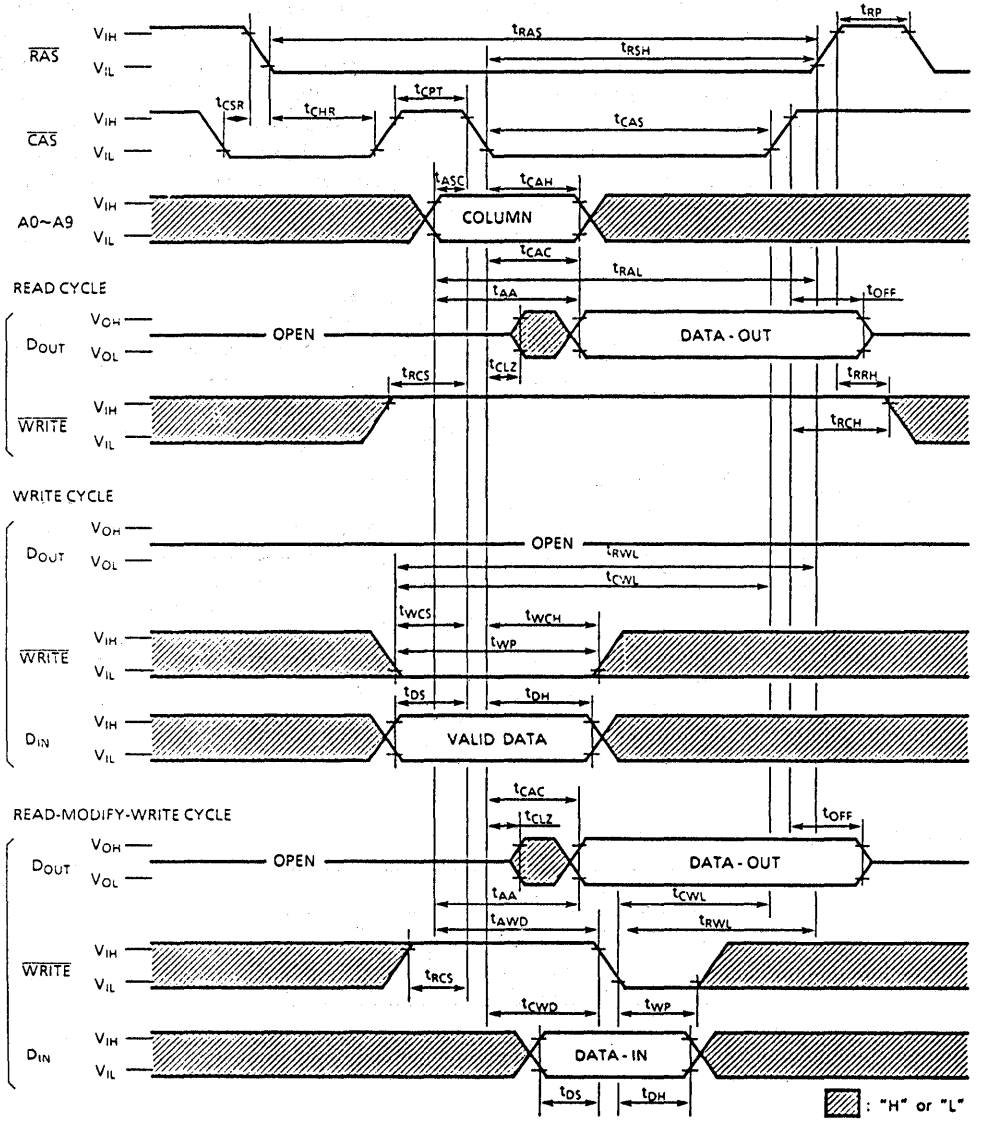
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



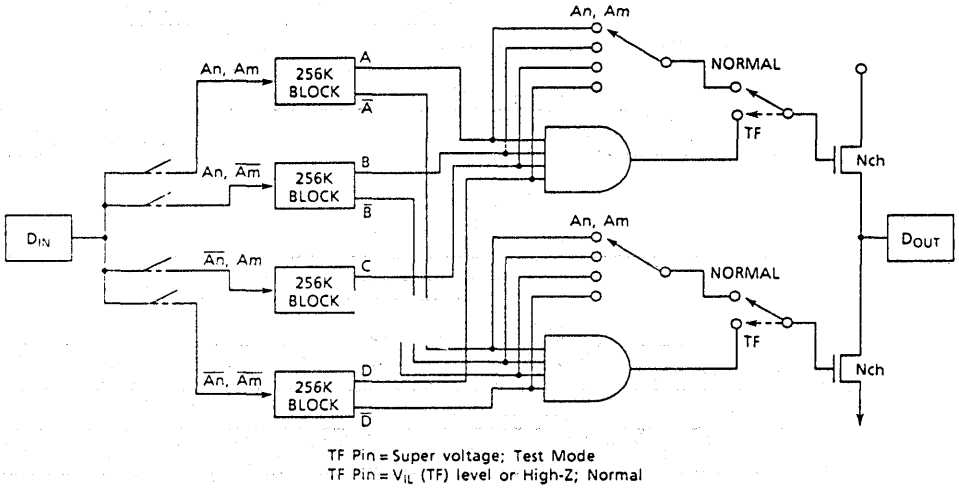
Note: "TF" pin should be connected to V_{IL}(TF) level or open, if "Test Mode" is not used.

TEST MODE

The TC511000AP/AJ/AZ is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511000AP/AJ/AZ including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Fast Page Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

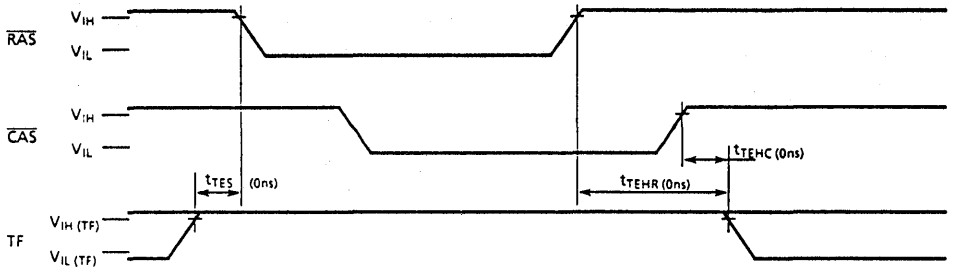


Fig. 2 Test Mode Cycle

TENTATIVE DATA
1,048,576 WORD × 1 BIT DYNAMIC RAM

DESCRIPTION

The TC511000APL/AJL/AZL is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511000APL/AJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC511000APL/AJL/AZL to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 1 bit organization
- Fast access time and cycle time

		TC511000APL/AJL/AZL-70/80/10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

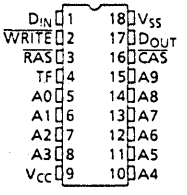
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating (TC511000APL/AJL/AZL-70)
  - 385mW MAX. Operating (TC511000APL/AJL/AZL-80)
  - 330mW MAX. Operating (TC511000APL/AJL/AZL-10)
  - 1.1mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Fast Page Mode and Test capability
- All inputs and output TTL compatible
- 512 refresh cycles/64ms
- Package TC511000APL : DIP18-P-300C
  TC511000AJL : SOJ26-P-300
  TC511000AZL : ZIP20-P-400

PIN NAMES

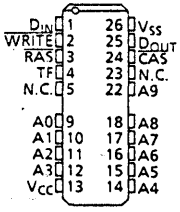
A0~A9	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	TF	Test Function
$\overline{CAS}$	Column Address Strobe	N.C.	No Connection

PIN CONNECTION

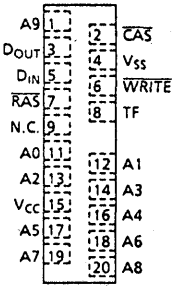
Plastic DIP



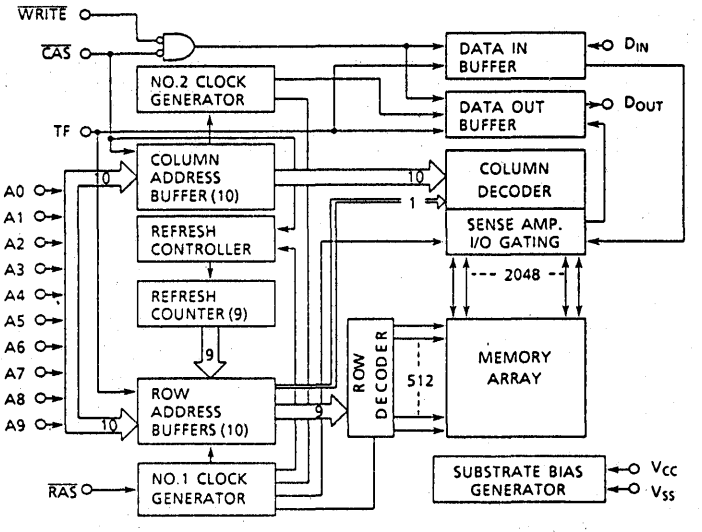
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	-	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	-	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0	-	V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511000APL/AJL/AZL-70	–	80	mA	3, 4, 5
		TC511000APL/AJL/AZL-80	–	70		
		TC511000APL/AJL/AZL-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511000APL/AJL/AZL-70	–	80	mA	3, 5
		TC511000APL/AJL/AZL-80	–	70		
		TC511000APL/AJL/AZL-10	–	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511000APL/AJL/AZL-70	–	60	mA	3, 4, 5
		TC511000APL/AJL/AZL-80	–	50		
		TC511000APL/AJL/AZL-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511000APL/AJL/AZL-70	–	80	mA	3
		TC511000APL/AJL/AZL-80	–	70		
		TC511000APL/AJ/LAZL-10	–	60		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, BATTERY BACK UP MODE ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V or 0.2V, A0~9 = V_{CC} – 0.2V or 0.2V, D_{IN} = V_{CC} – 0.2V or OPEN : t_{RC} = 125μs, t_{RAS} = t_{RAS} MIN. ~1μs)		–	300	μA	3, 6
I_I (L)	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
I_{ITF} (L)	INPUT LEAKAGE CURRENT (only TF) (0V ≤ V_{IN} (TF) ≤ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
I_O (L)	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≤ V_{IN} (TF) ≤ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)			0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	CHARACTERISTIC	TC511000APL/AJL/AZL-70		TC511000APL/AJL/AZL-80		TC511000APL/AJL/AZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	-	175	-	210	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	65	-	70	-	85	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	10,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	50	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	12
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	CHARACTERISTIC	TC511000APL/AJL/AZL-70		TC511000APL/AJL/AZL-80		TC511000APL/AJL/AZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	64	–	64	–	64	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

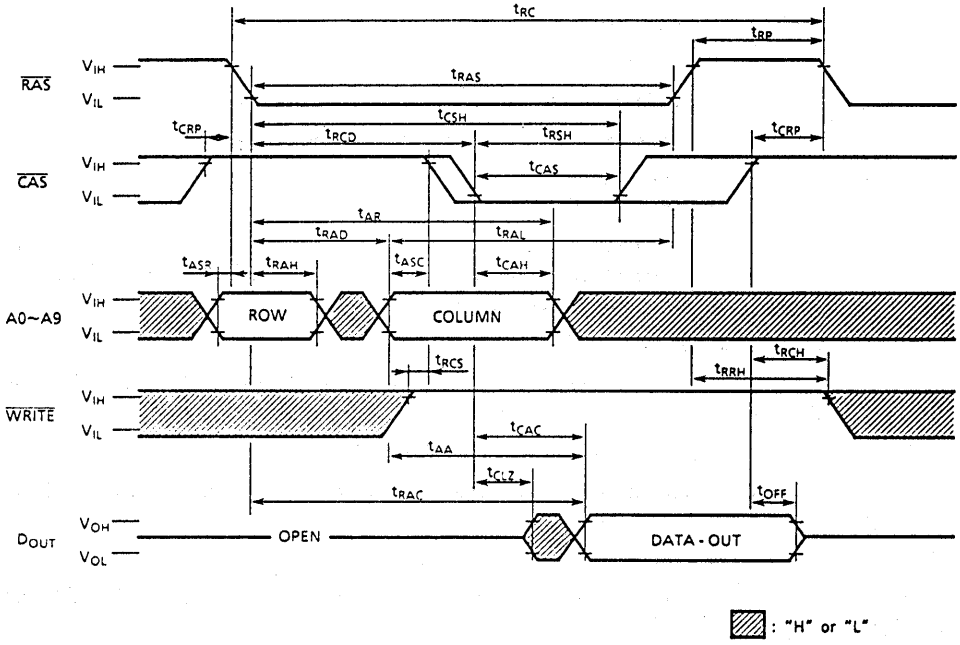
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
8. AC measurements assume t_T = 5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

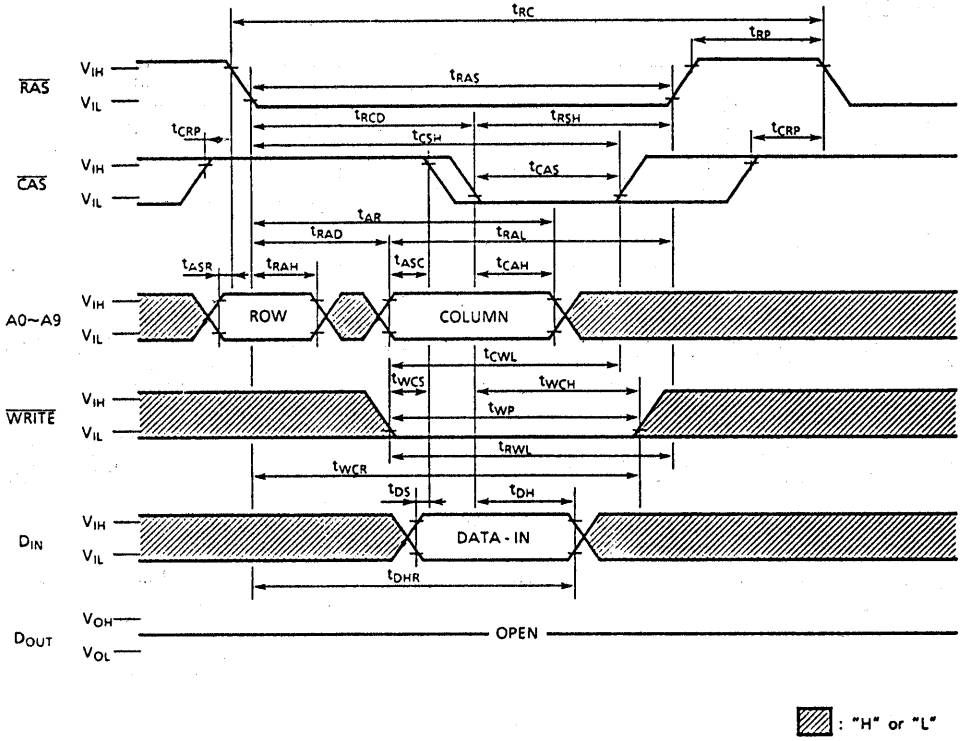
TIMING WAVEFORMS

READ CYCLE



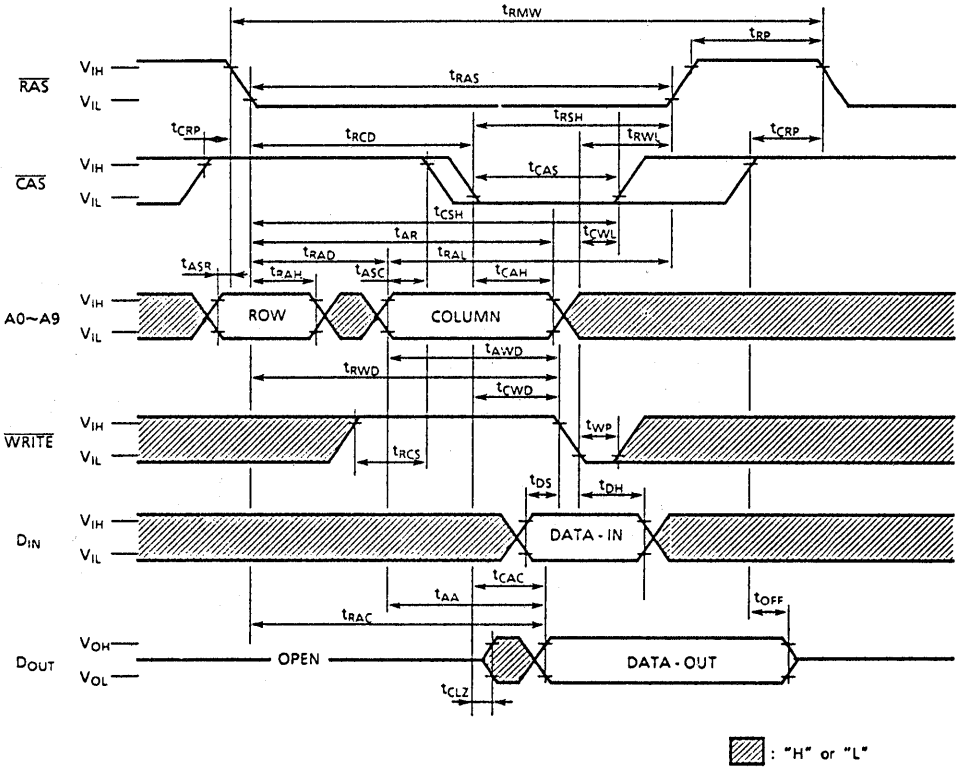
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



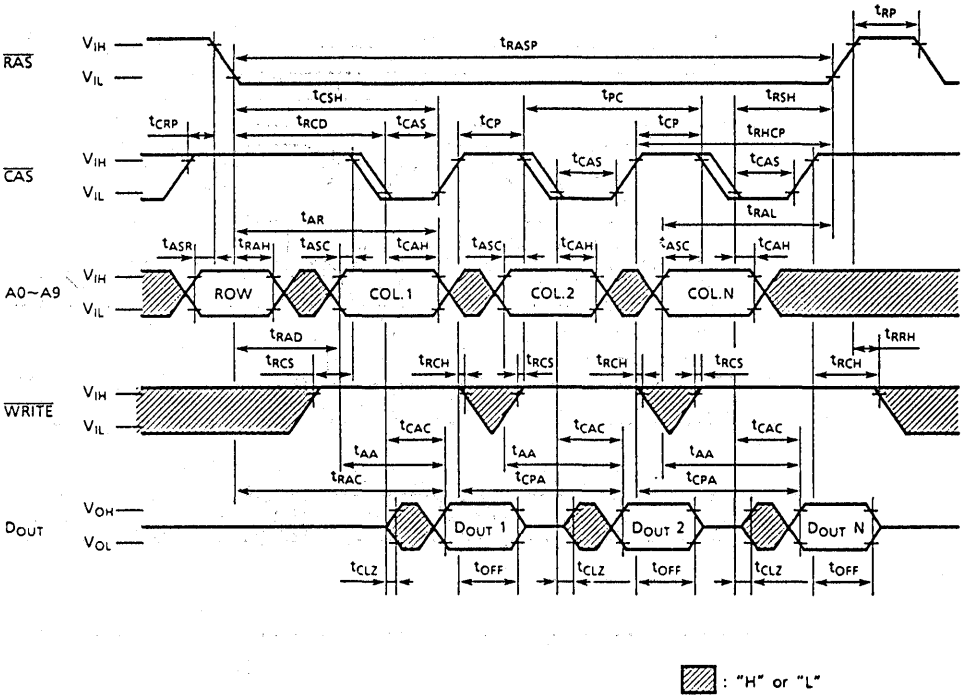
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE



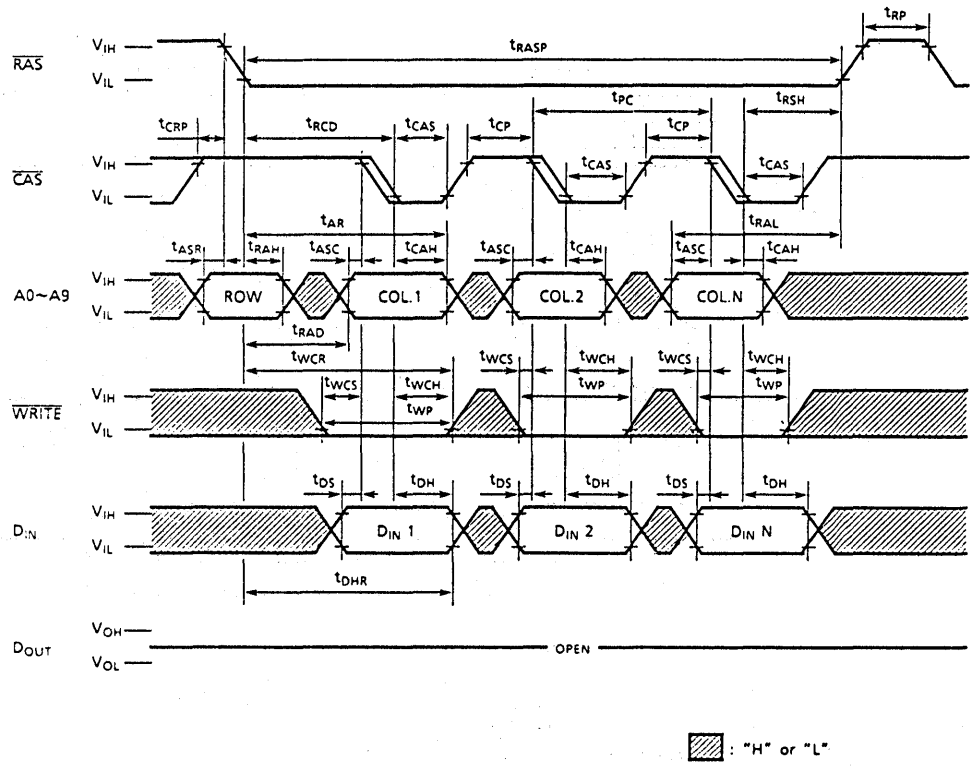
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ CYCLE



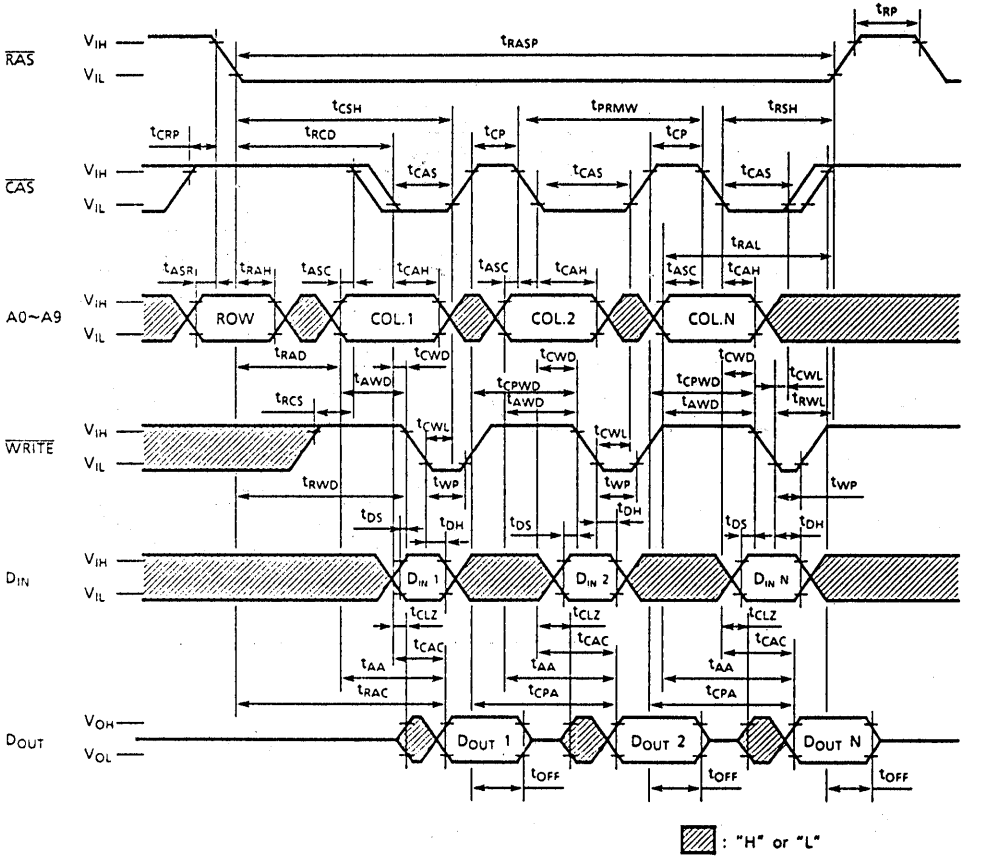
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



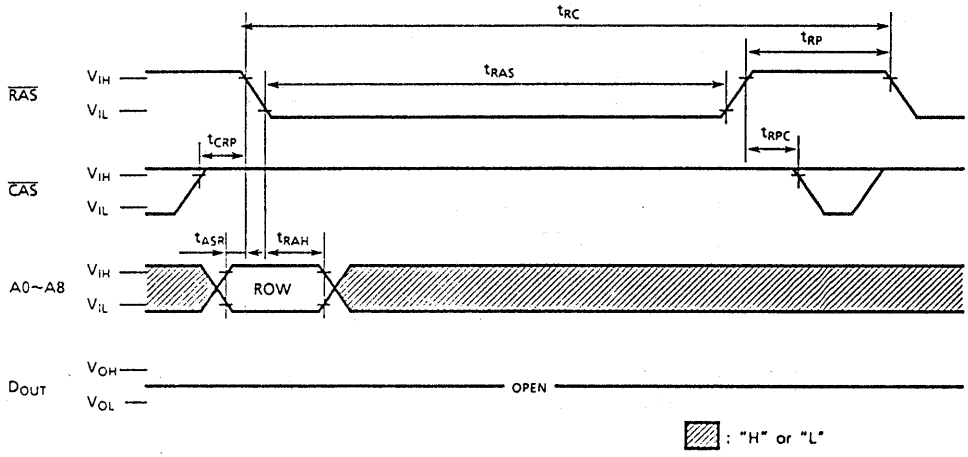
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



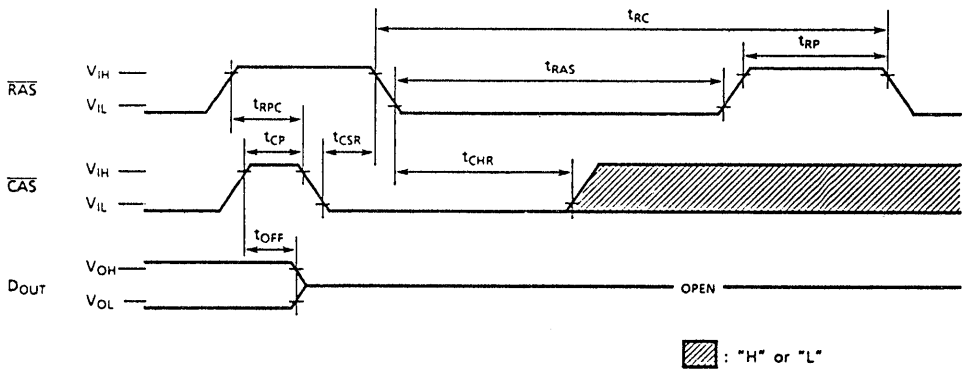
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



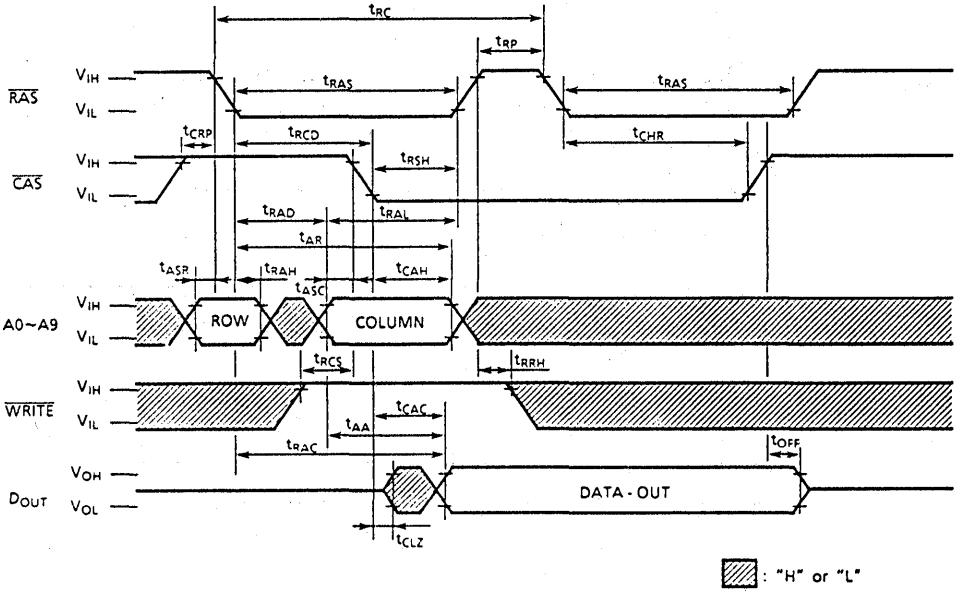
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



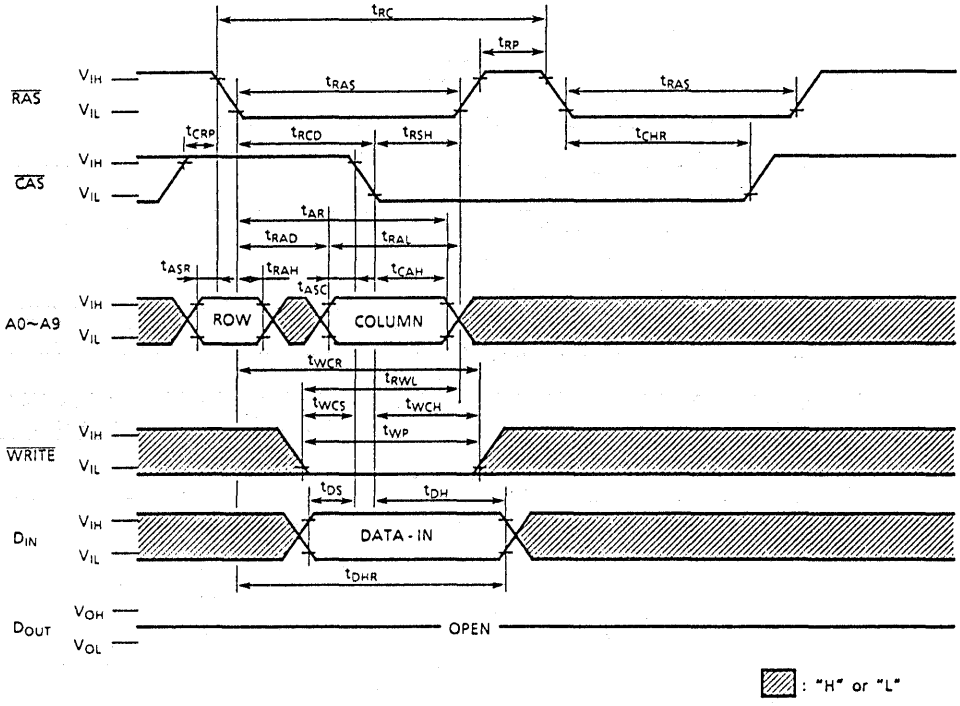
NOTE: $\overline{WRITE}$ = "H" or "L" A9 = "H" or "L"
"TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



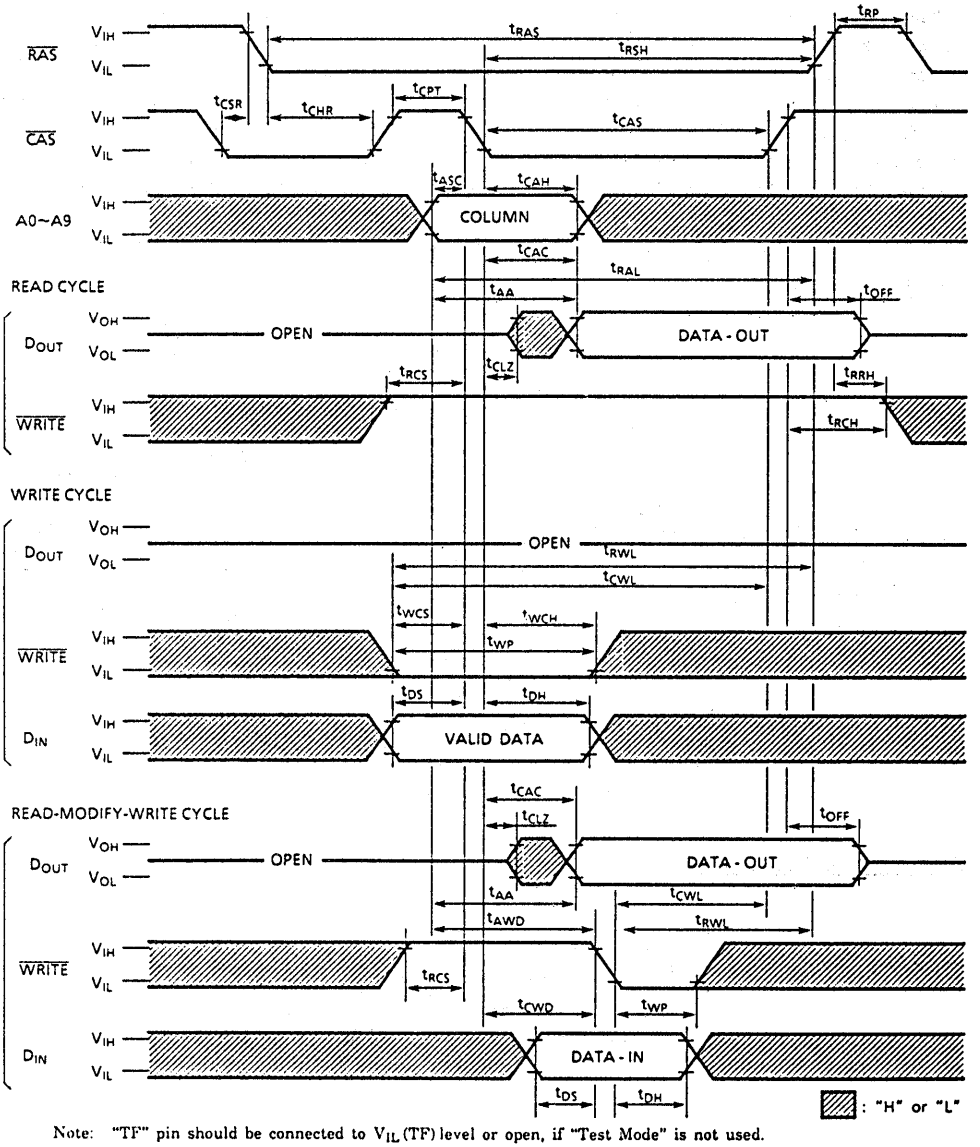
NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



NOTE: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



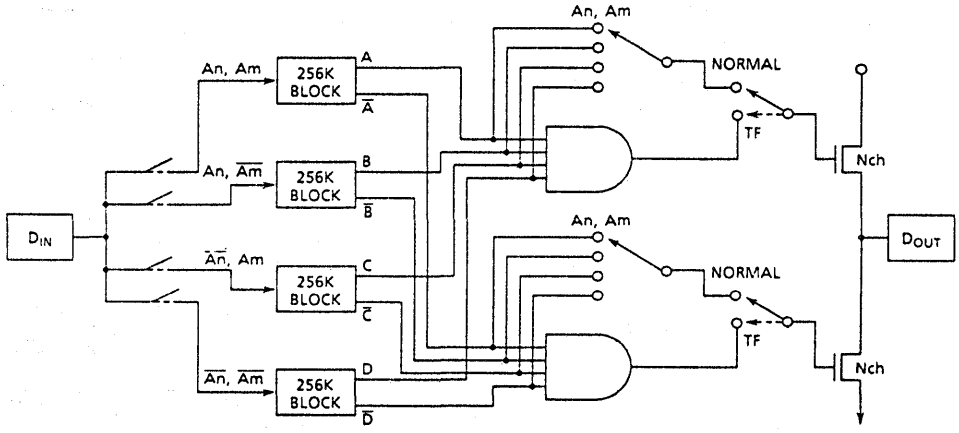
Note: "TF" pin should be connected to V_{IL} (TF) level or open, if "Test Mode" is not used.

TEST MODE

The TC511000APL/AJL/AZL is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H"or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511000APL/AJL/AZL including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Fast Page Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

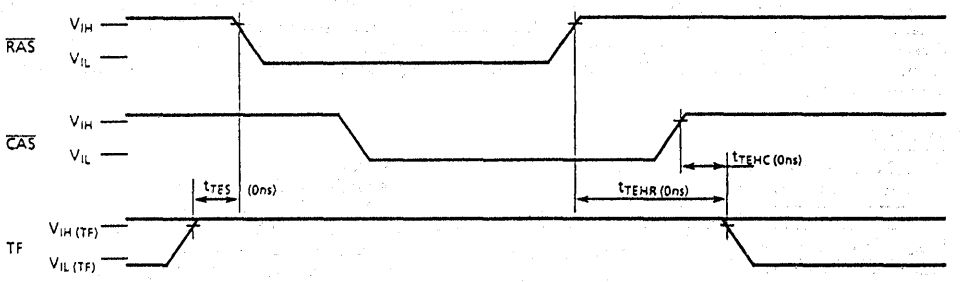


Fig. 2 Test Mode Cycle

1,048,576 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC511001BP/BJ/BZ/BFT is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC511001BP/BJ/BZ/BFT to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001BP/BJ/BZ/BFT is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

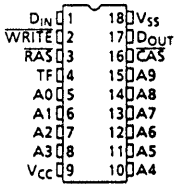
- 1,048,576 word by 1bit organization
- Fast access time and cycle time

		TC511001BP/BJ/BZ/BFT – 60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{NCAC}	Nibble Mode Access Time	20ns
t_{NC}	Nibble Mode Cycle Time	40ns

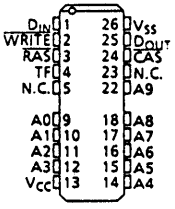
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511001BP : DIP18-P-300C
  TC511001BJ : SOJ26-P-300
  TC511001BZ : ZIP20-P-400
  TC511001BFT : TSOP24-P-0616

PIN CONNECTION

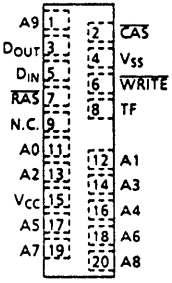
Plastic DIP



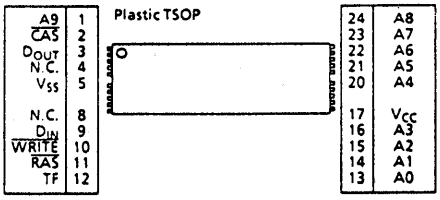
Plastic SOJ



Plastic ZIP



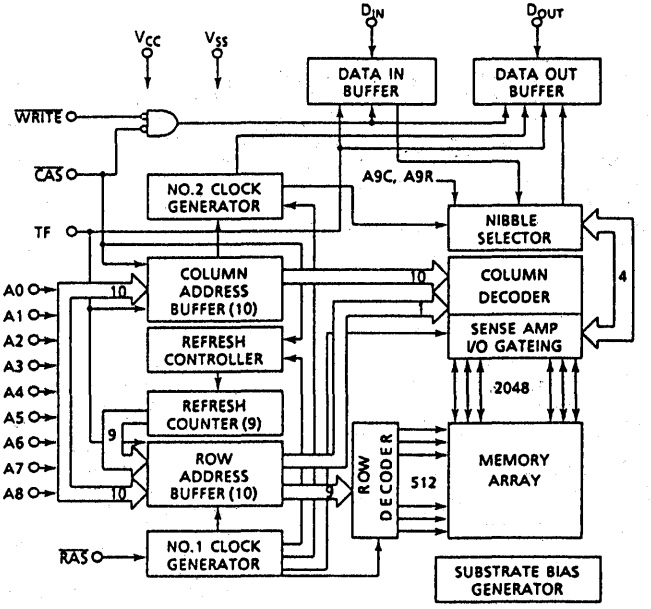
Plastic TSOP



PIN NAMES

A0~A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Test Mode Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0	−	V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511001BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511001BP/BJ/BZ/BFT-60	–	90	mA	3,5
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Cycling: t_{NC} = t_{NC} MIN.)	TC511001BP/BJ/BZ/BFT-60	–	40	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511001BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) (0V ≤ $V_{IN\ (TF)}$ ≤ V_{CC} + 0.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT (V_{CC} + 4.5V ≤ $V_{IN\ (TF)}$ ≤ 10.5V)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC51001BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RWC}	Read-Modify-Write Cycle Time	135	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	ns	
t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{NCAC}	Nibble Mode Access Time	-	20	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC511001BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{DH}	Data-In Hold Time	15	-	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{REF}	Refresh Period	-	8	ms	
t_{WCS}	Write Command Set-UP Time	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	15	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	30	-	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	-	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	-	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	-	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	-	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	-	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	-	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	-	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

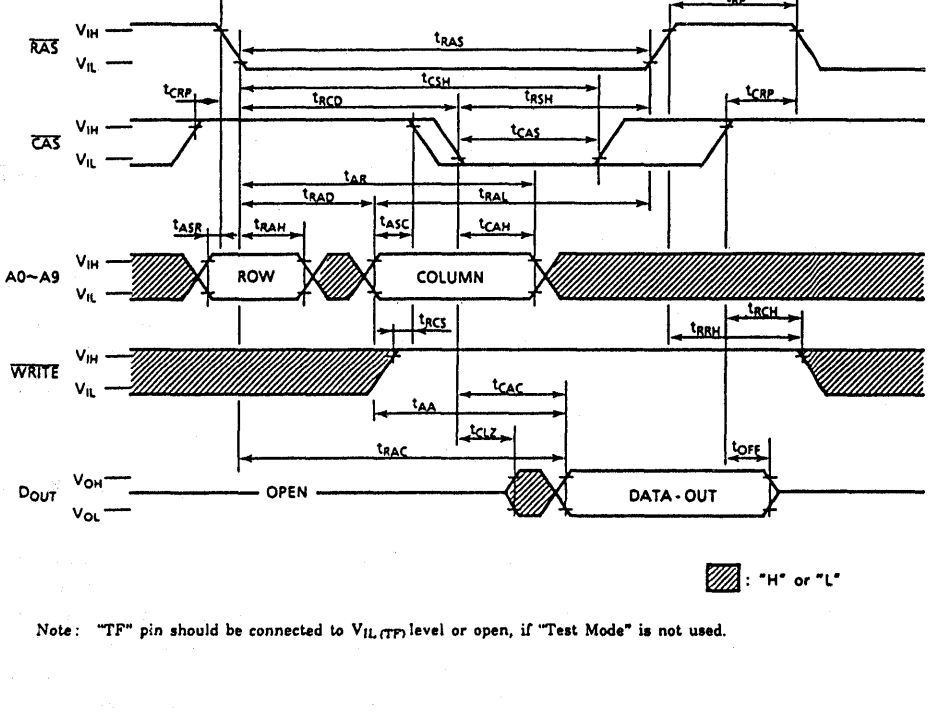
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	-	7	
C_O	Output Capacitance (D_{OUT})	-	7	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

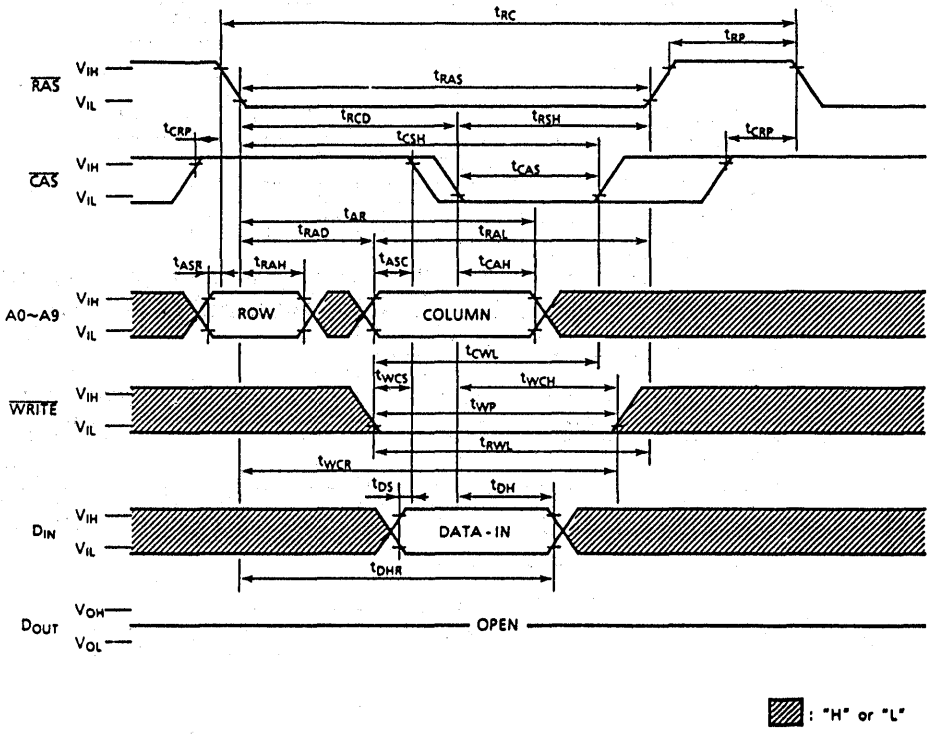
TIMING WAVEFORMS

READ CYCLE



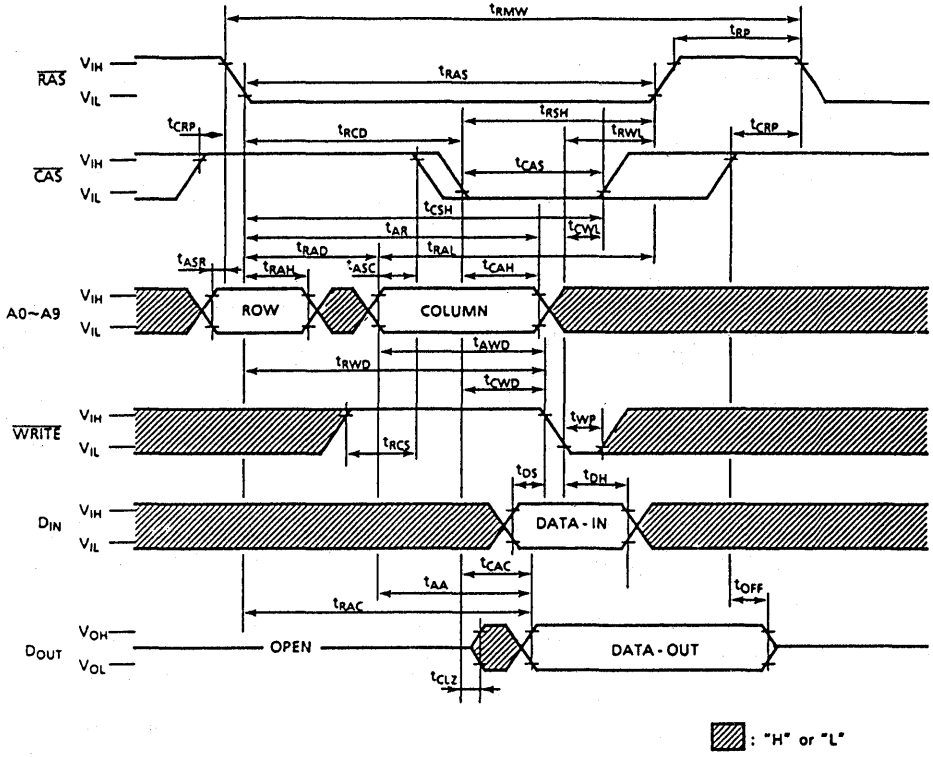
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



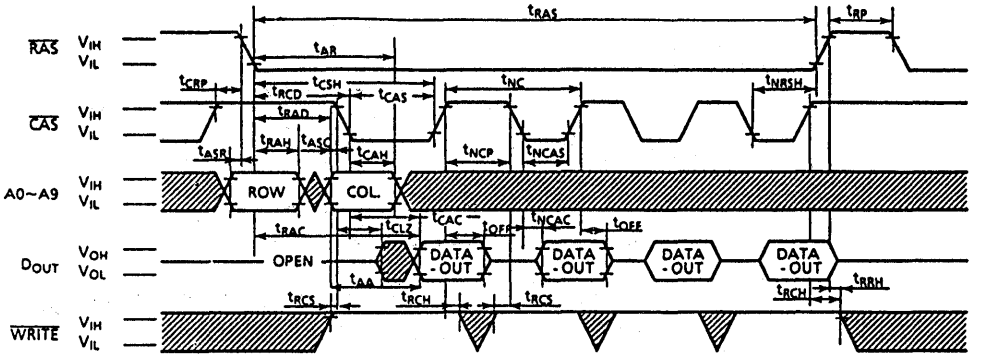
Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE

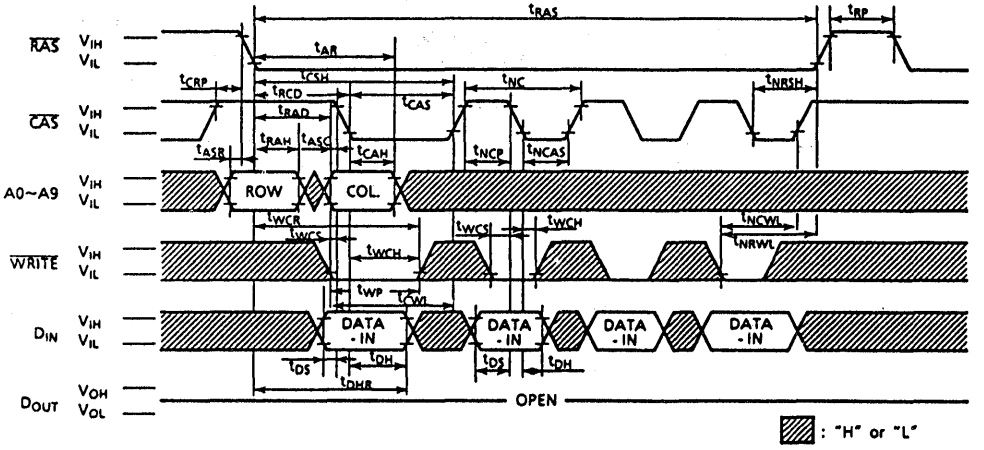


Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

NIBBLE MODE READ CYCLE

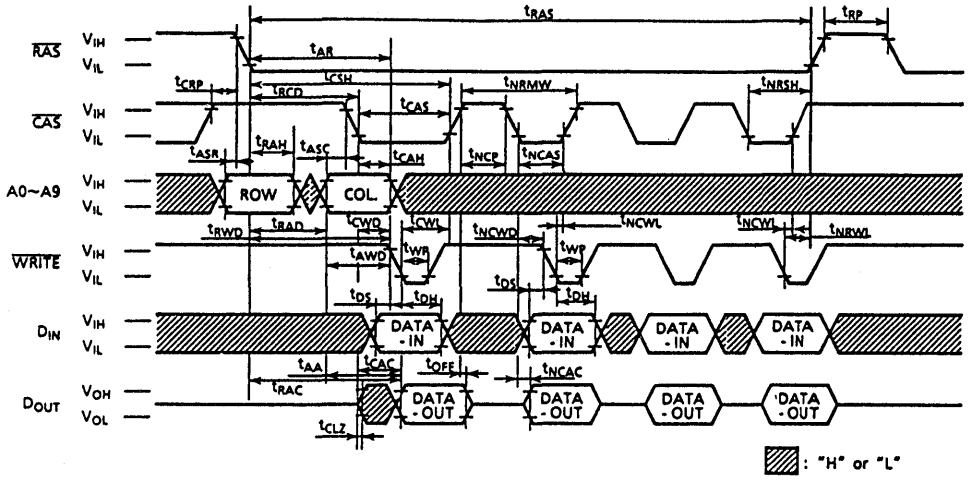


NIBBLE MODE WRITE CYCLE(EARLY WRITE)



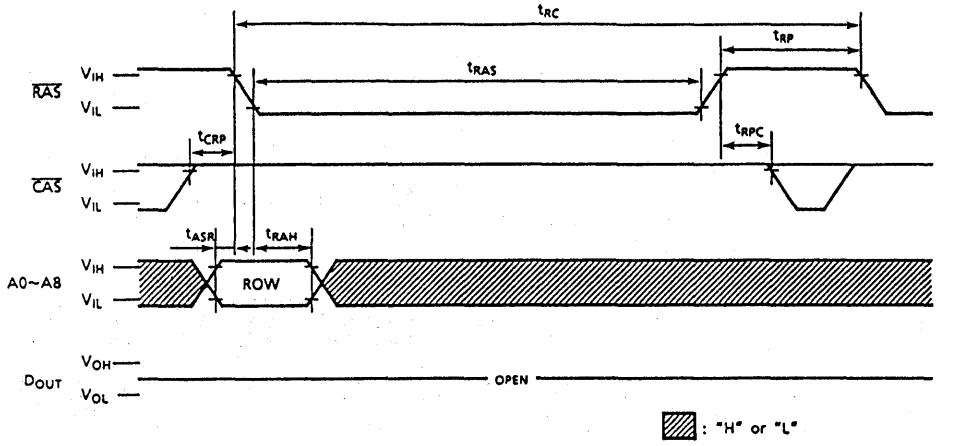
Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open.

NIBBLE MODE READ - MODIFY - WRITE



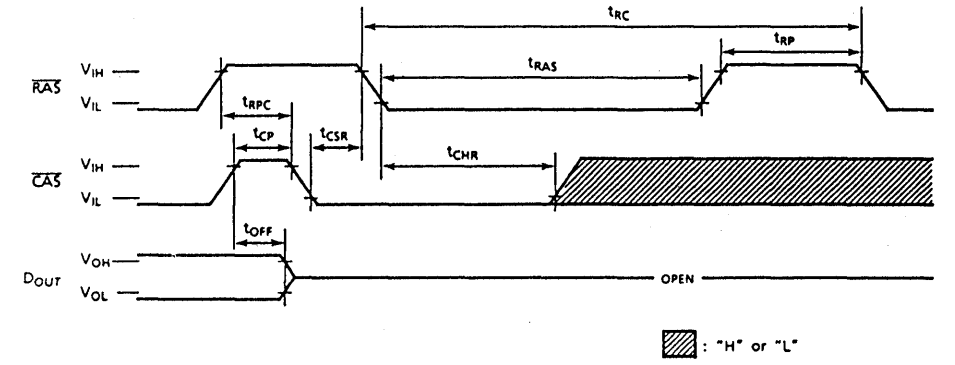
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open.

$\overline{RAS}$ ONLY REFRESH CYCLE



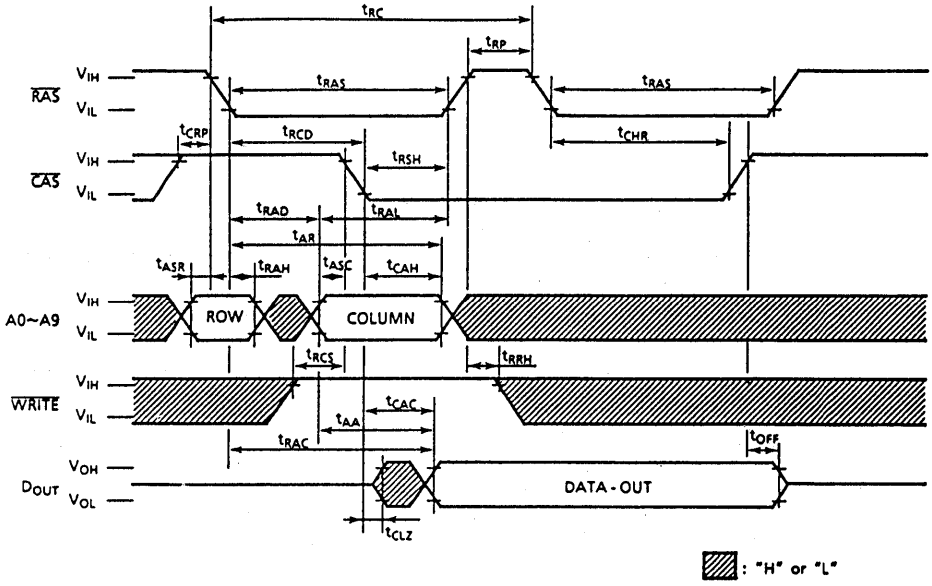
Note: WRITE = "H" or "L", A9 = "H" or "L"
"TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



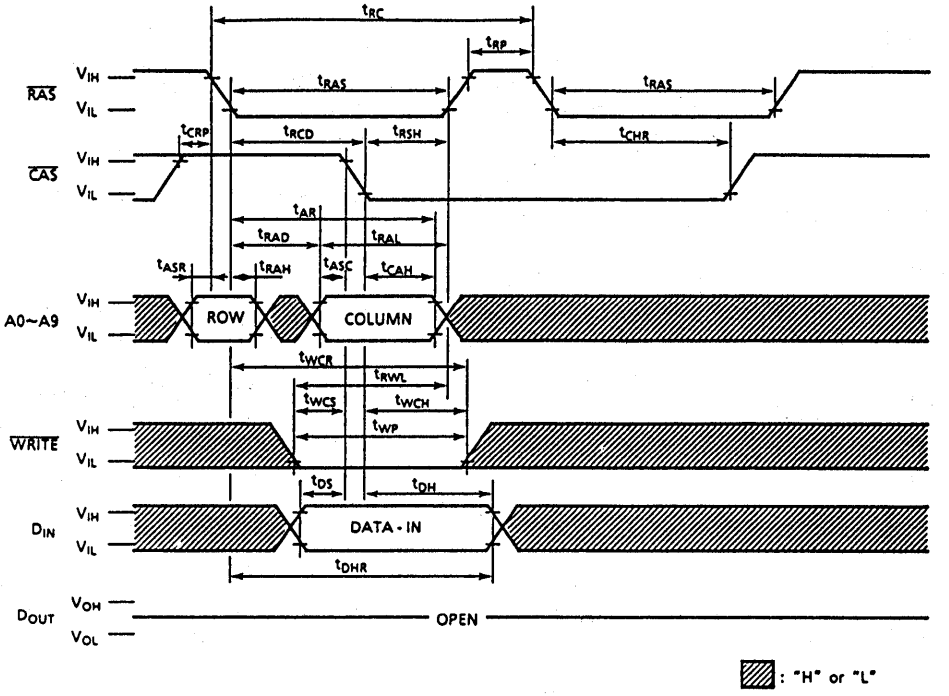
Note: WRITE = "H" or "L", A9 = "H" or "L"
"TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



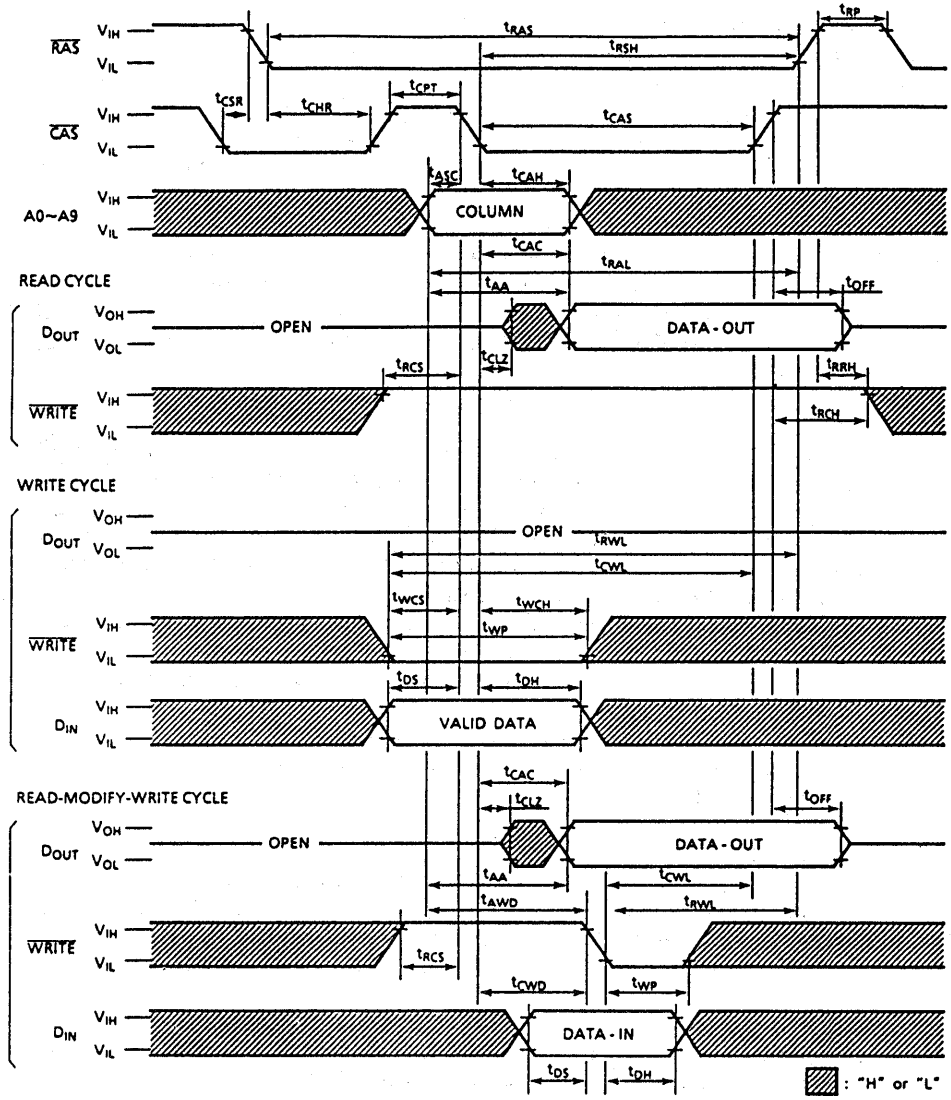
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001BP/BJ/BZ/BFT are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ While $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-modify-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle"the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-modify-write and nibble mode write cycles while the "early write"cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

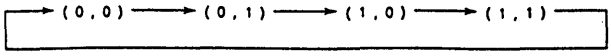
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001BP/BJ/BZ/BFT is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits.
From then on, successive bits come out in a binary fashion; 00→01→10→11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

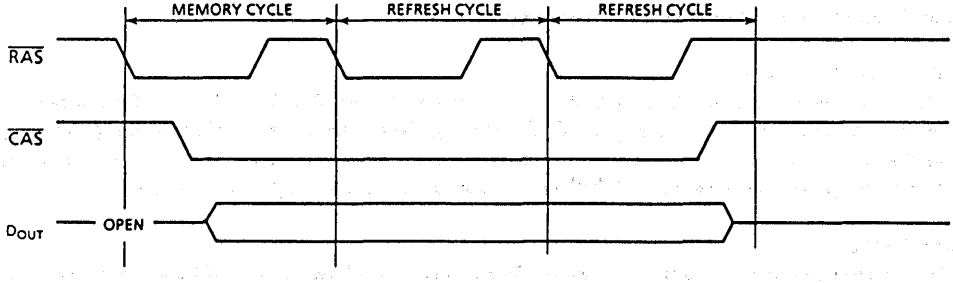
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A8) within each 8 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001BP/BJ/BZ/BFT offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001BP/BJ/BZ/BFT is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data avilability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001BP/BJ/BZ/BFT can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ② .

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④ .

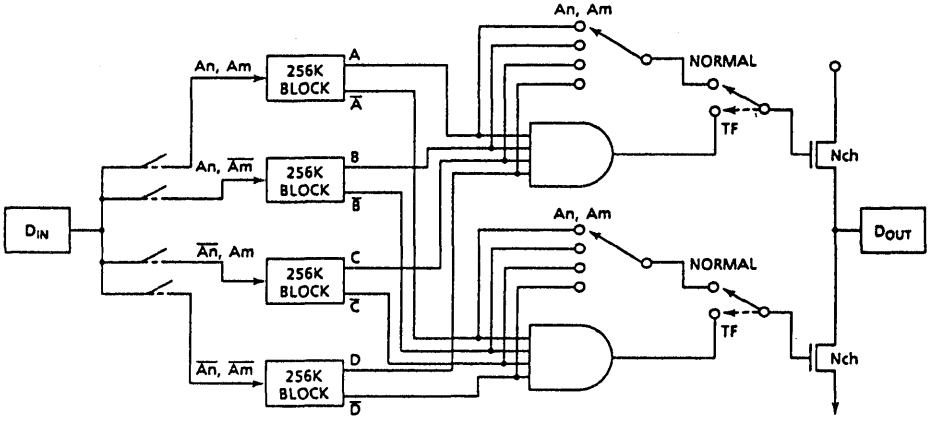
⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC511001BP/BJ/BZ/BFT is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511001BP/BJ/BZ/BFT including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles except Nibble Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

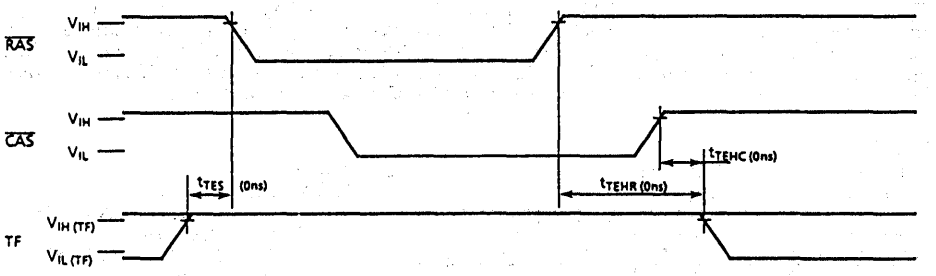


Fig. 2 Test Mode Cycle

TENTATIVE DATA
1,048,576 WORD × 1 BIT DYNAMIC RAM

DESCRIPTION

The TC511001AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511001AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511001AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL. The special feature of TC511001AP/AJ/AZ is nibble mode, allowing the user to serially access 4 bits of data at a high data rate.

FEATURES

- 1,048,576 word by 1bit organization
- Fast access time and cycle time

		TC511001AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{NCAC}	Nibble Mode Access Time	20ns	20ns	20ns
t_{NC}	Nibble Mode Cycle Time	40ns	40ns	40ns

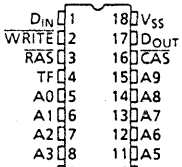
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  440mW MAX. Operating (TC511001AP/AJ/AZ-70)
  385mW MAX. Operating (TC511001AP/AJ/AZ-80)
  330mW MAX. Operating (TC511001AP/AJ/AZ-10)
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability using "EARLY WRITE" operation
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Nibble Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511001AP : DIP18-P-300C
  TC511001AJ : SOJ26-P-300
  TC511001AZ : ZIP20-P-400

PIN NAMES

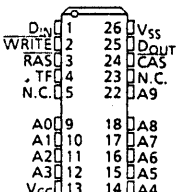
A0~A9	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	TF	Test Function
$\overline{RAS}$	Row Address Strobe	N.C.	No Connection

PIN CONNECTION (TOP VIEW)

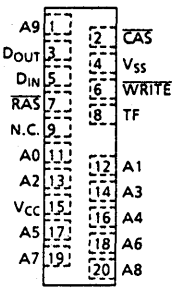
Plastic DIP



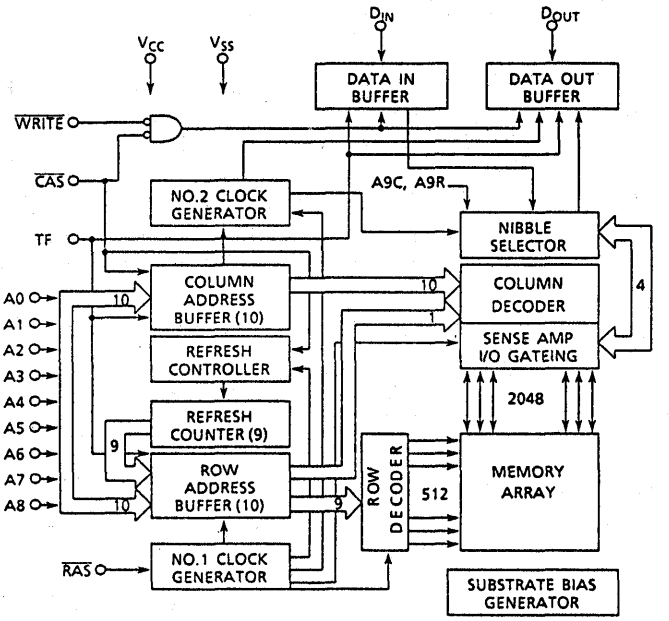
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Test Mode Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	$V_{CC}+4.5$	−	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0	−	$V_{CC}+1.0$	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511001AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC511001AP/AJ/AZ-80	–	70		
		TC511001AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511001AP/AJ/AZ-70	–	80	mA	3, 5
		TC511001AP/AJ/AZ-80	–	70		
		TC511001AP/AJ/AZ-10	–	60		
I_{CC4}	NIBBLE MODE CURRENT Average Power Supply Current, Nibble Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Cycling: $t_{NC} = t_{NC}$ MIN.)	TC511001AP/AJ/AZ-70	–	40	mA	3, 4, 5
		TC511001AP/AJ/AZ-80	–	40		
		TC511001AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511001AP/AJ/AZ-70	–	80	mA	3
		TC511001AP/AJ/AZ-80	–	70		
		TC511001AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN(TF)} \leq V_{CC} + 0.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN(TF)} \leq 10.5V$)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC51001AP/ AJ/AZ-70		TC51001AP/ AJ/AZ-80		TC51001AP/ AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	-	175	-	210	-	ns	
t_{NC}	Nibble Mode Cycle Time	40	-	40	-	40	-	ns	
t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	65	-	65	-	65	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	9,15
t_{NCAC}	Nibble Mode Access Time	-	20	-	20	-	20	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	11
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	CHARACTERISTIC	TC51001AP/AJ/AZ-70		TC51001AP/AJ/AZ-80		TC51001AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test)	40	–	40	–	50	–	ns	
t_{NCAS}	Nibble Mode Pulse Width	20	–	20	–	20	–	ns	
t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20	–	20	–	20	–	ns	
t_{NCWD}	Nibble Mode $\overline{CAS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	20	–	ns	
t_{NRWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	ns	
t_{NCWL}	Nibble Mode $\overline{WRITE}$ Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

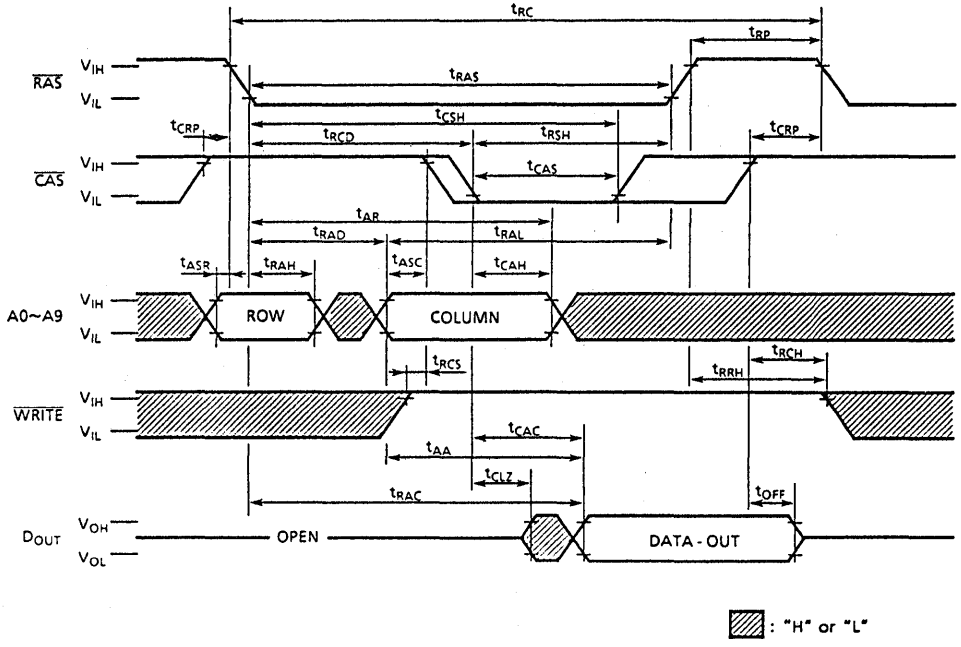
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

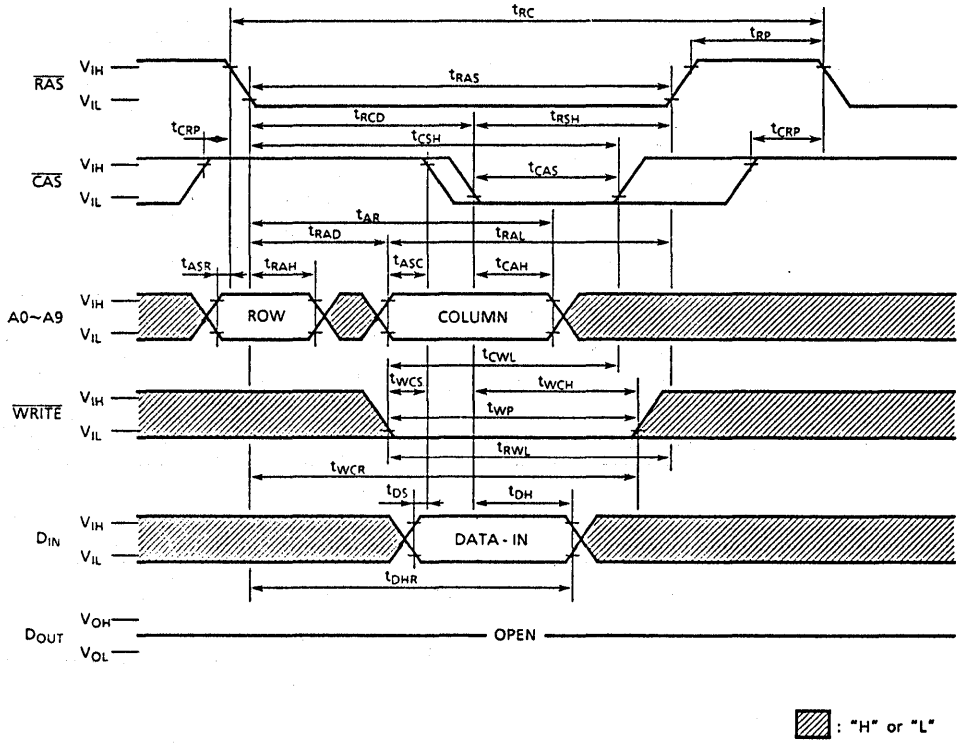
TIMING WAVEFORMS

READ CYCLE



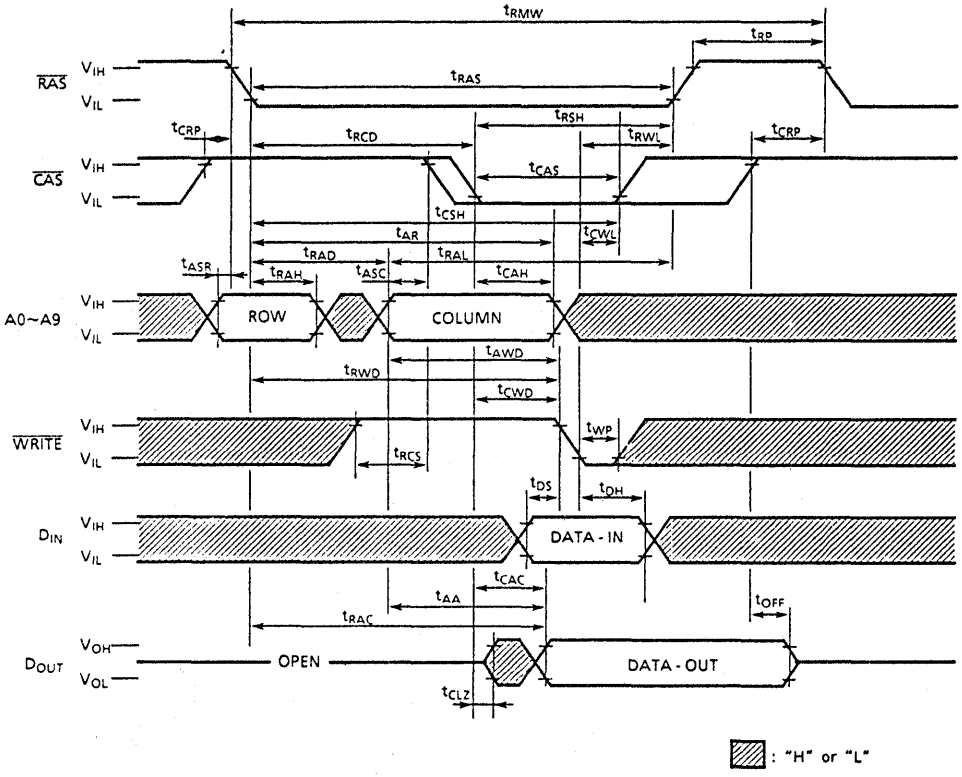
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

WRITE CYCLE (EARLY WRITE)



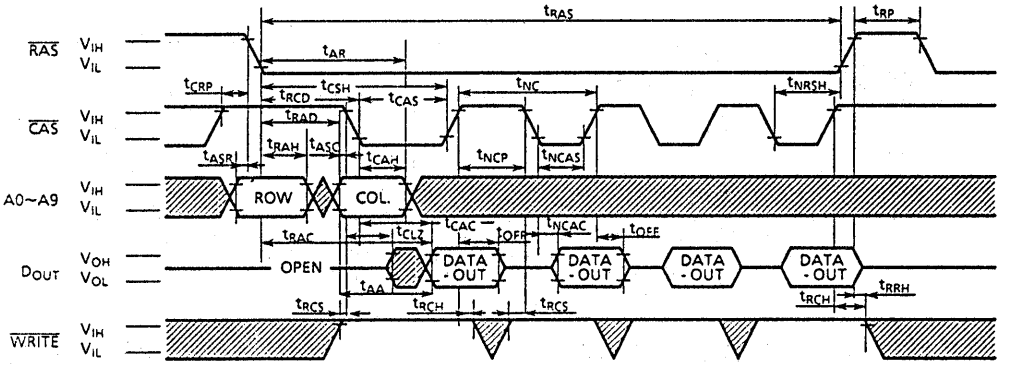
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

READ-MODIFY-WRITE CYCLE

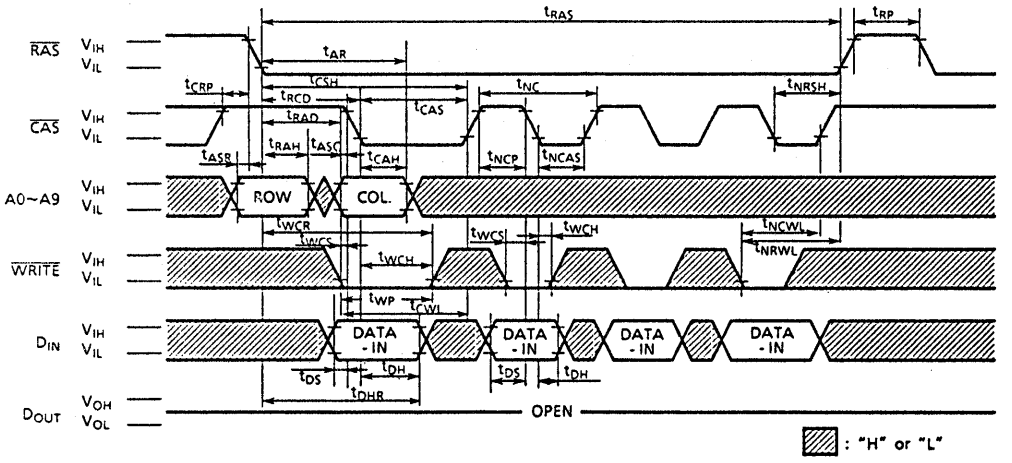


Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

NIBBLE MODE READ CYCLE

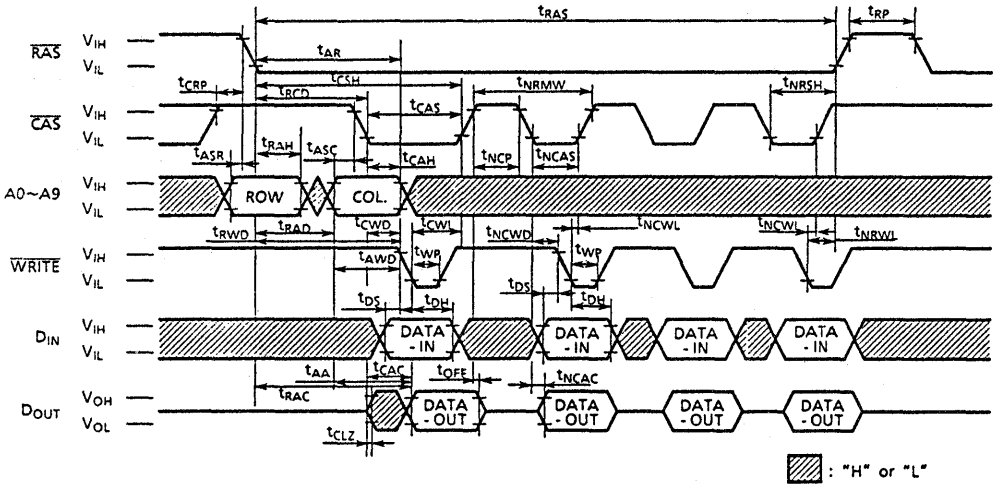


NIBBLE MODE WRITE CYCLE(EARLY WRITE)



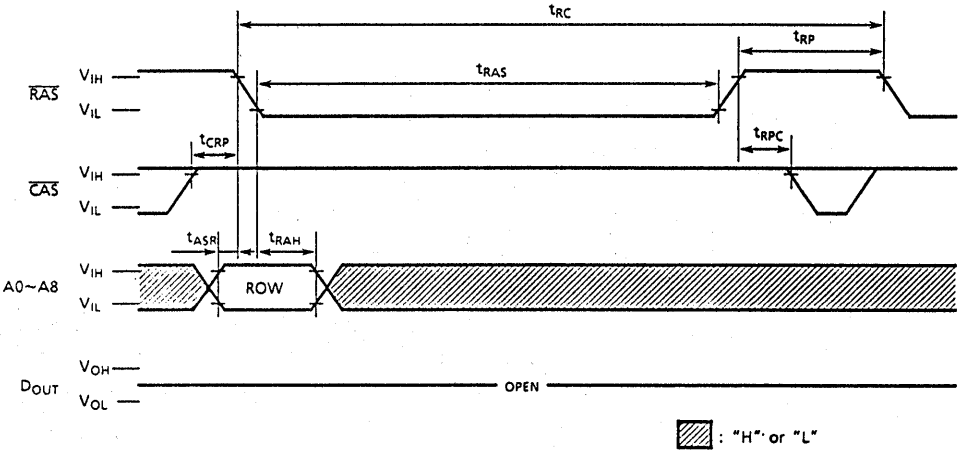
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open.

NIBBLE MODE READ - MODIFY - WRITE



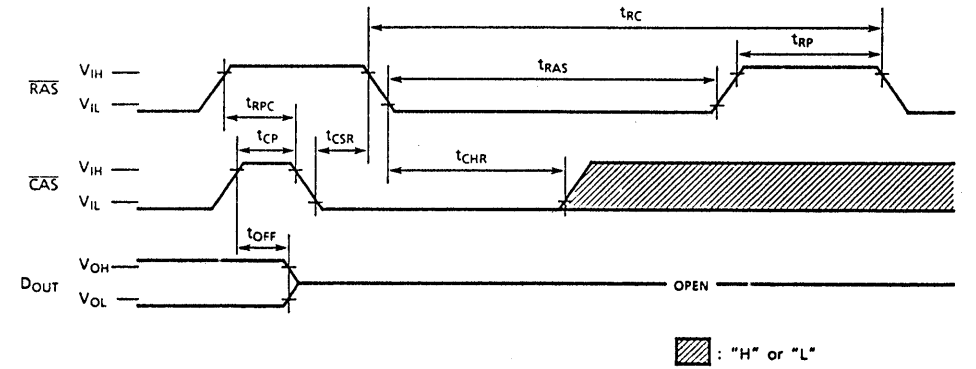
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open.

$\overline{RAS}$ ONLY REFRESH CYCLE



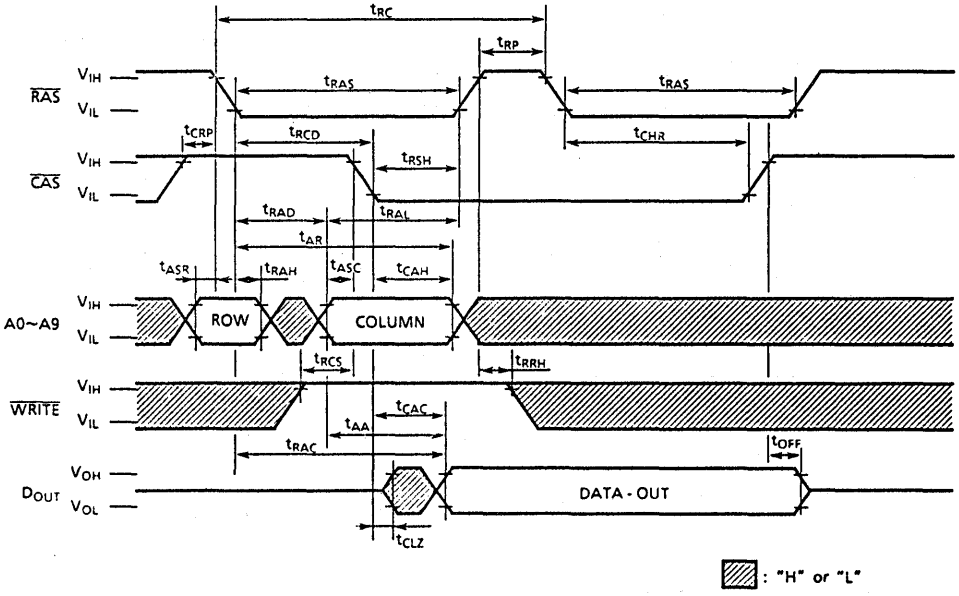
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



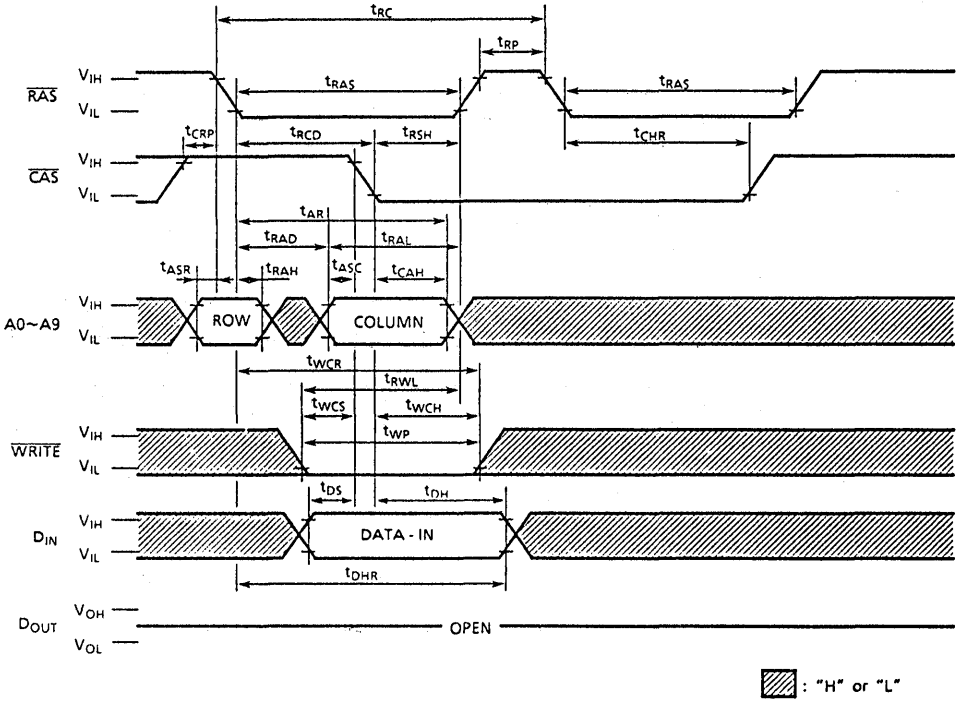
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)



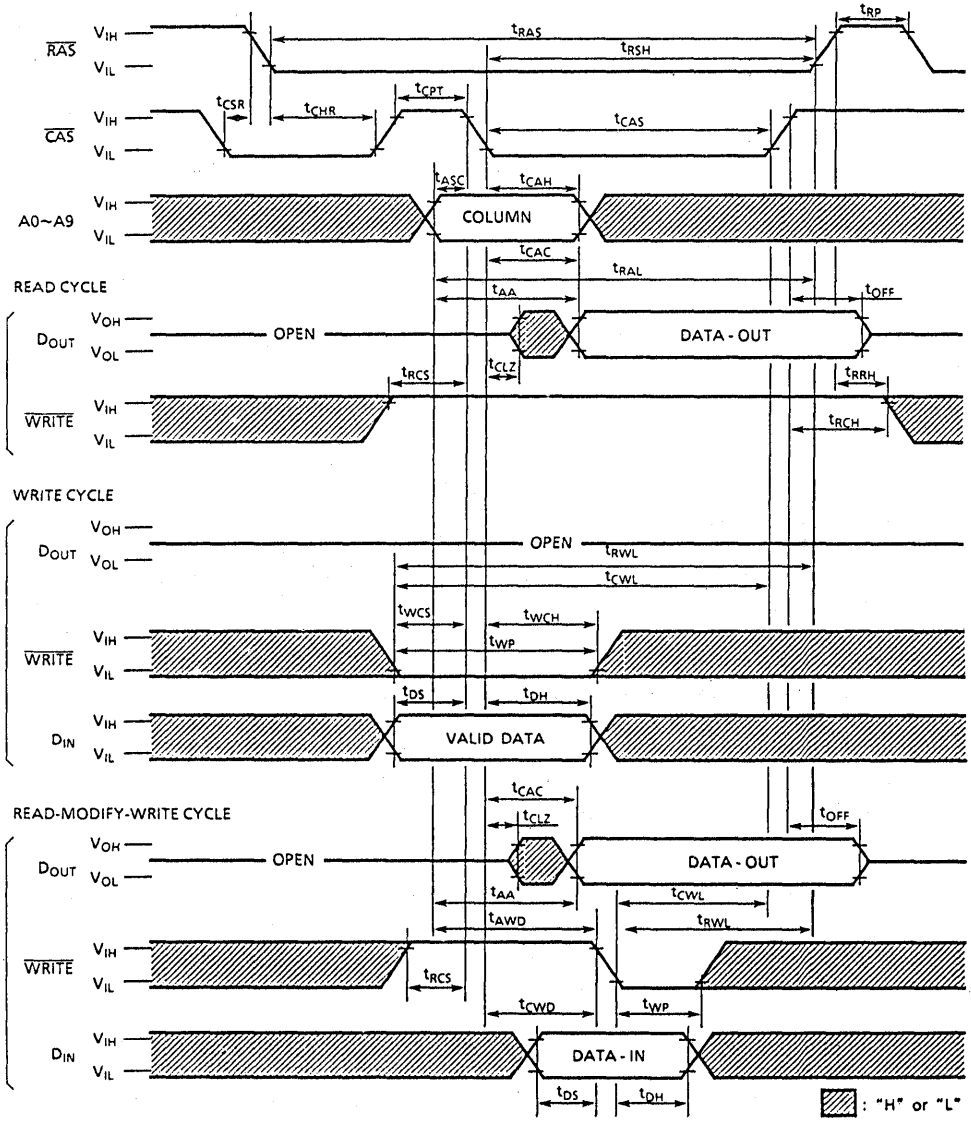
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (WRITE)



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

APPLICATION INFORMATION

ADDRESSING

The 20 address bits required to decode 1 of the 1,048,576 cell locations within the TC511001AP/AJ/AZ are multiplexed onto the 10 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 10 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 10 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ While $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-modify-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle"the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-modify-write and nibble mode write cycles while the "early write"cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

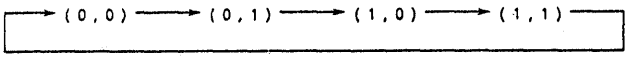
Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the TC511001AP/AJ/AZ is the high impedance (open circuit) state. This is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

NIBBLE MODE

Nibble mode operation allows faster successive data operation on 4 bits. The first of 4 bits is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three pages at high data rate (faster than t_{CAC}). Row and column addresses need only be supplied for the first access of the cycles. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Address A9 determines the starting point of the circular 4 bits nibble. Row A9 and column A9 provide the two binary bits needed to select one of four bits.
From then on, successive bits come out in a binary fashion; 00→01→10→11 with A9 row being the least significant address.

A nibble cycle can be a read, write, or delayed write cycle. Any conbinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

$\overline{RAS}$ ONLY REFRESH

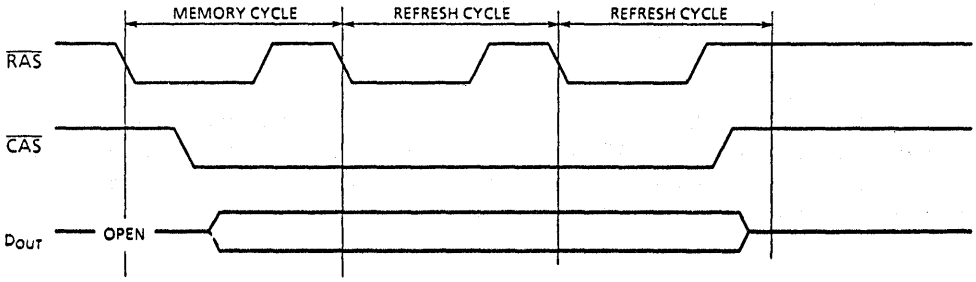
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A8) within each 8 millisecond time interval.
Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511001AP/AJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

HIDDEN REFRESH

An optional feature of the TC511001AP/AJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "hidden" among data cycles without affecting the data avilability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511001AP/AJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ② .

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④ .

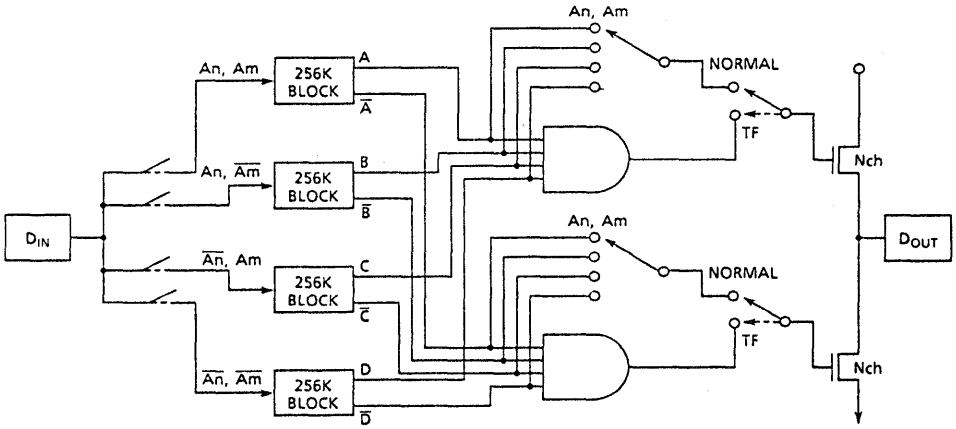
⑥ Perform the above ① to ⑤ to the complement data.

TEST MODE

The TC511001AP/AJ/AZ is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511001AP/AJ/AZ including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = V_{IL} (TF) level or High-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi – Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles except Nibble Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to V_{IL} (TF) level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

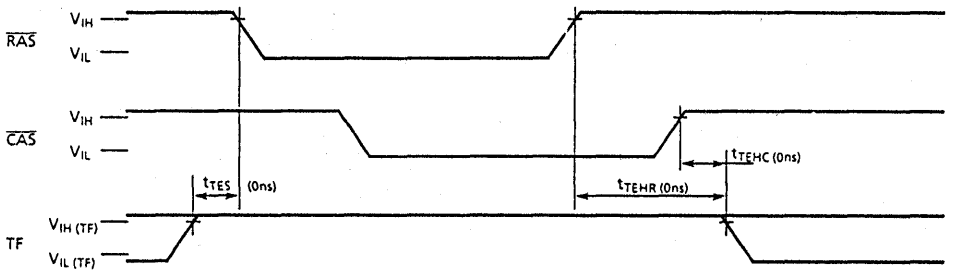


Fig. 2 Test Mode Cycle

1,048,576 WORD × 1 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC511002BP/BJ/BZ/BFT is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC511002BP/BJ/BZ/BFT to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

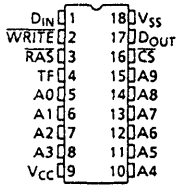
- 1,048,576 word by 1bit organization
- Fast access time and cycle time

	TC511002BP/BJ/BZ/BFT-60
t_{RAC} $\overline{RAS}$ Access Time	60ns
t_{AA} Column Address Access Time	30ns
t_{CAC} $\overline{CS}$ Access Time	20ns
t_{RC} Cycle Time	110ns
t_{SC} Static Column Mode Cycle Time	35ns

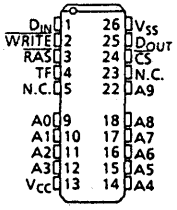
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511002BP : DIP18-P-300C
  TC511002BJ : SOJ26-P-300
  TC511002BZ : ZIP20-P-400
  TC511002BFT : TSOP24-P-0616

PIN CONNECTION

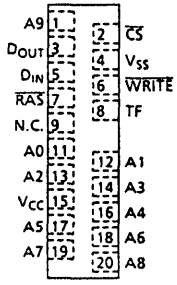
Plastic DIP



Plastic SOJ



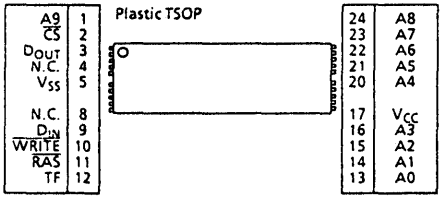
Plastic ZIP



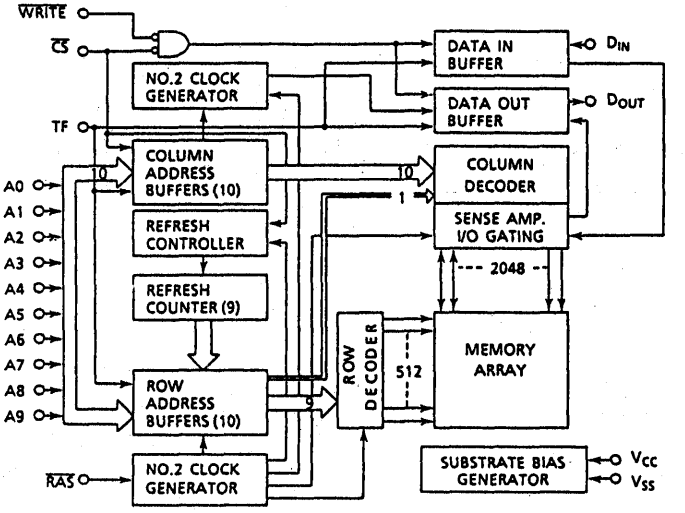
PIN NAMES

A0~A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{CS}$	Chip Select Input
$\overline{WRITE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
TF	Test Function
N.C.	No Connection

Plastic TSOP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL(TF)}$	Test Disable Input Low Voltage	−1.0		V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/BZ/BFT-60	–	90	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC511002BP/BJ/BZ/BFT-60	–	70	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN\ (TF)} \leq V_{CC} + 0.5V$, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)		– 10	10	µA	
I_{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN\ (TF)} \leq 10.5V$)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(VCC = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511002BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	135	-	ns	
t_{SC}	Static Column Mode Cycle Time	35	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	60	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9, 14
t_{CAC}	Access Time from $\overline{CS}$	-	20	ns	9, 14
t_{AA}	Access Time from Column Address	-	30	ns	9, 15
t_{ALW}	Access Time from Last Write	-	55	ns	9, 16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-Off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	-	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	50	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	70	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	ns	17
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC511002BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	55	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{WI}	Write Command Inactive Time	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	20	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	30	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	15	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	30	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CS}$	0	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

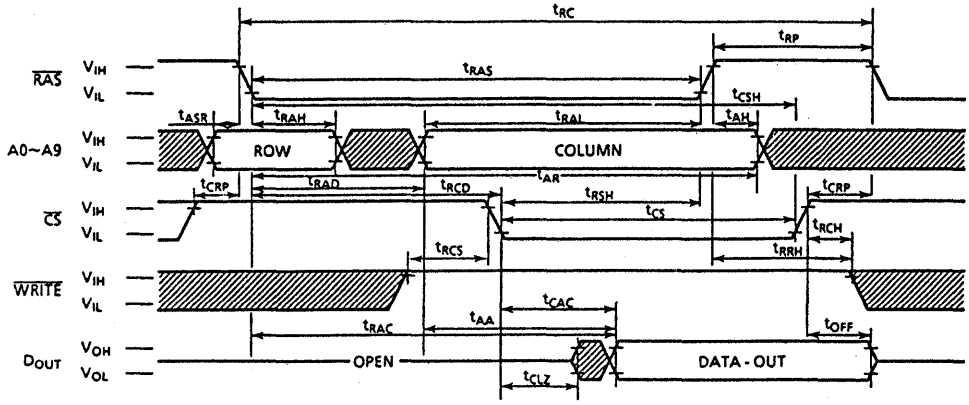
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

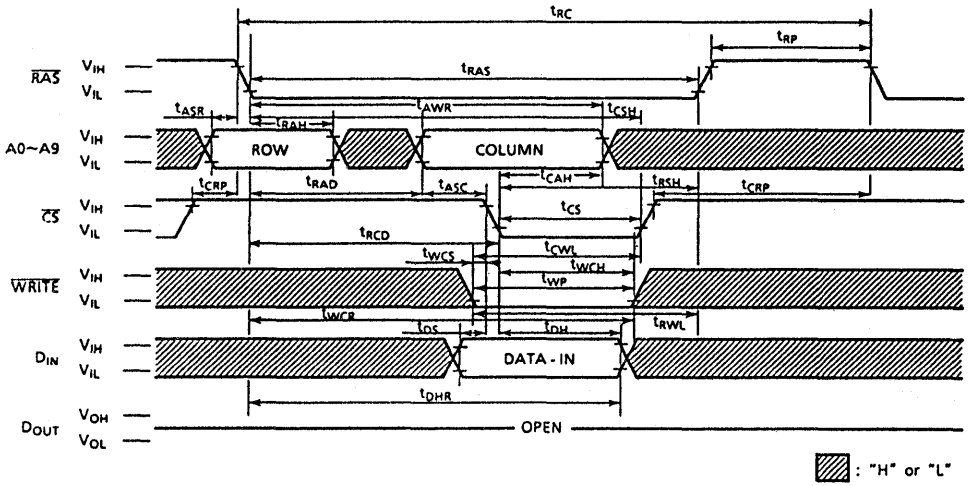
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (min.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met.
    t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has risen up.

TIMING WAVEFORMS

READ CYCLE

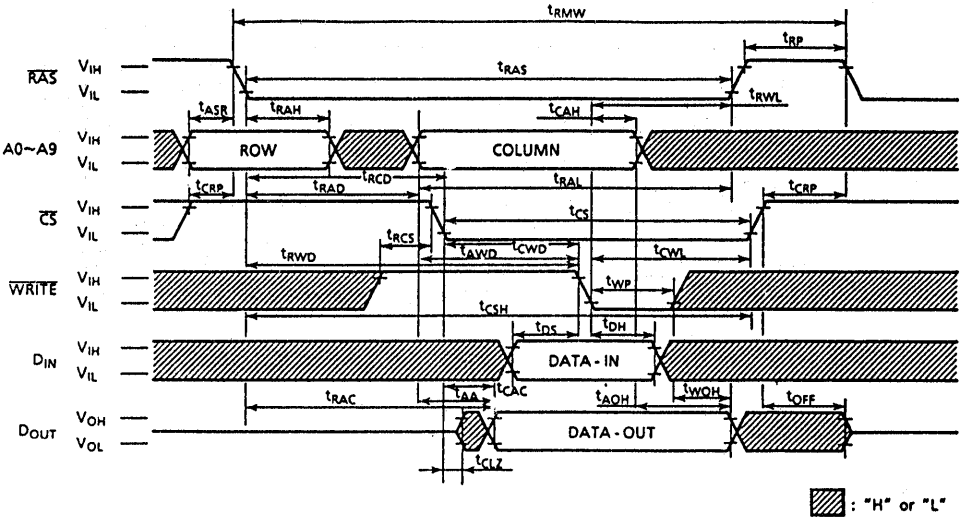


WRITE CYCLE (EARLY WRITE)



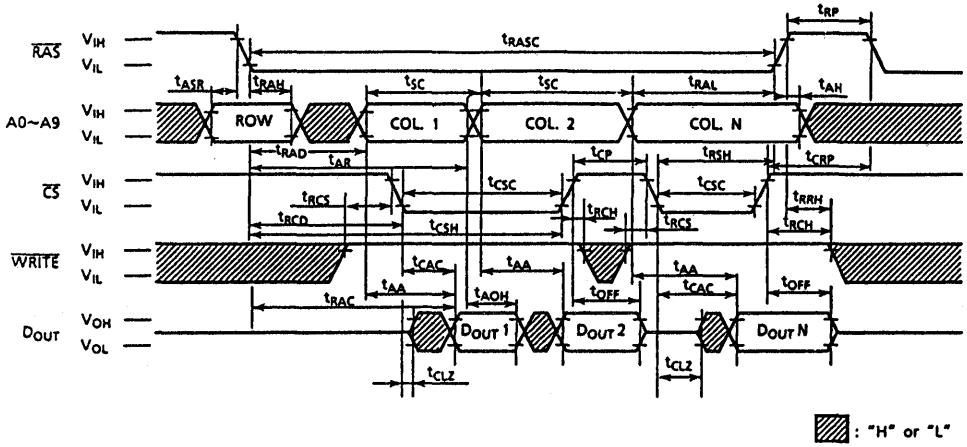
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

READ - MODIFY - WRITE CYCLE



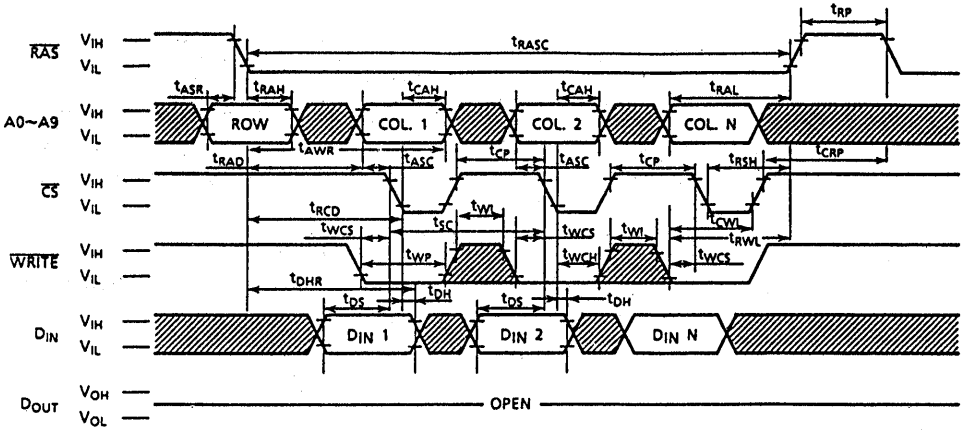
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ CYCLE

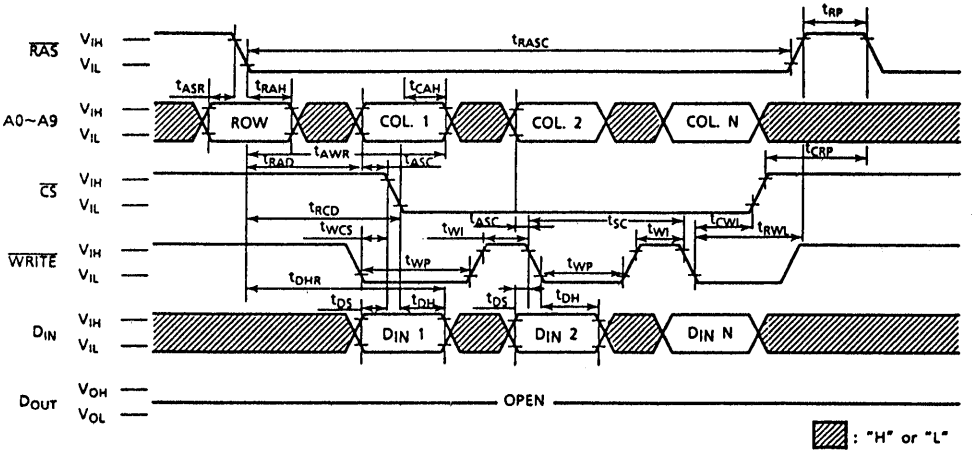


Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

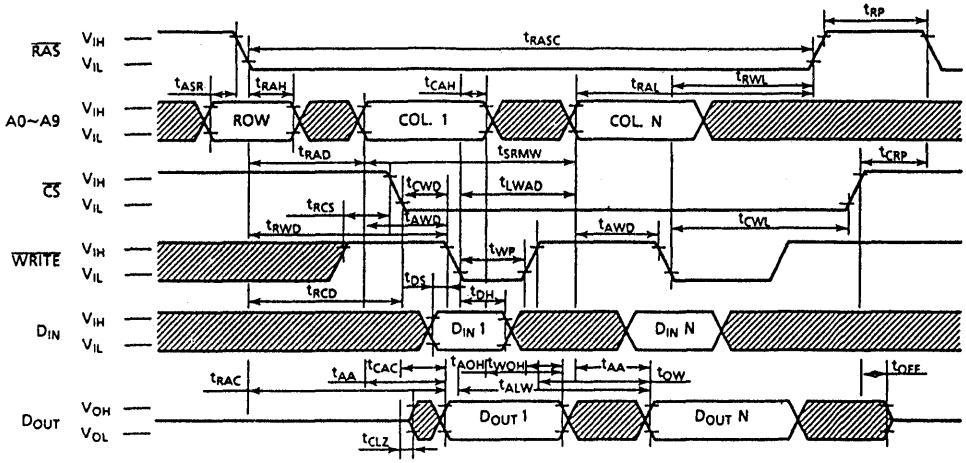


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

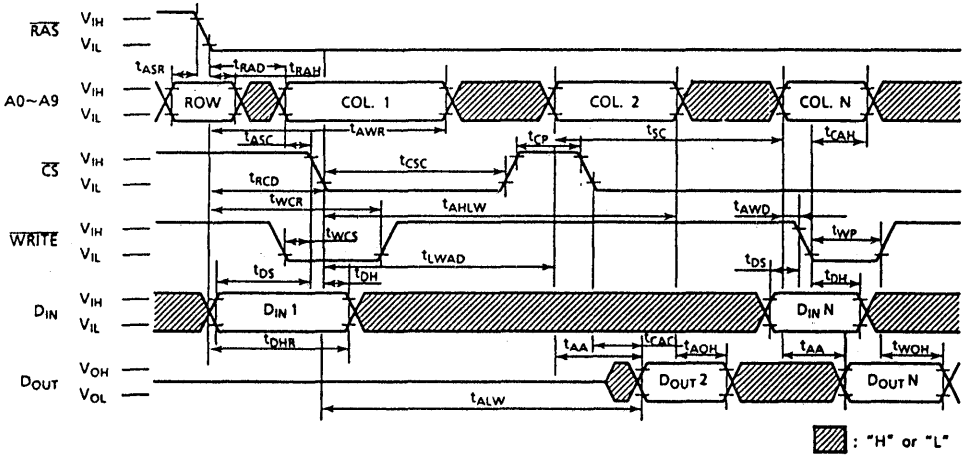


Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

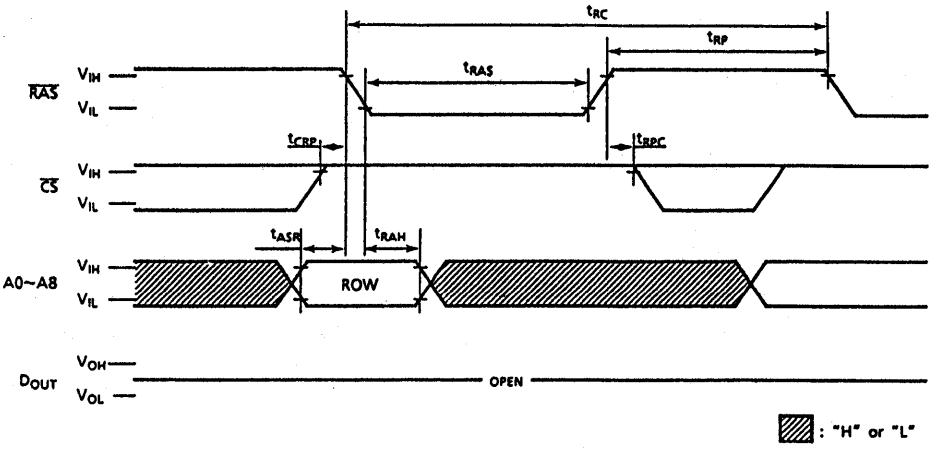


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



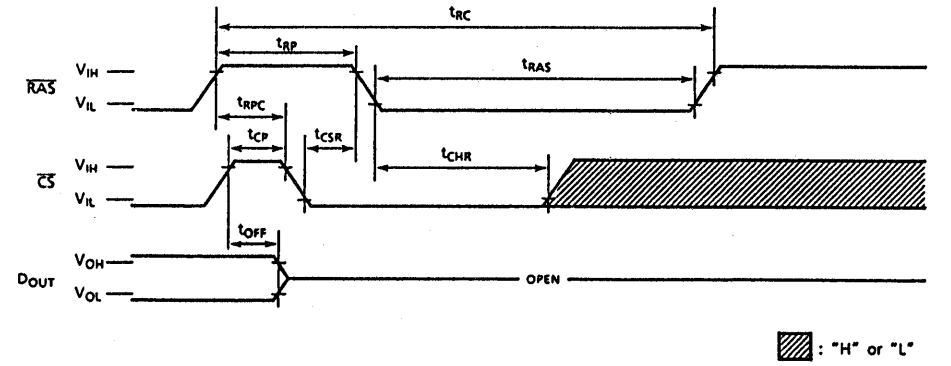
Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



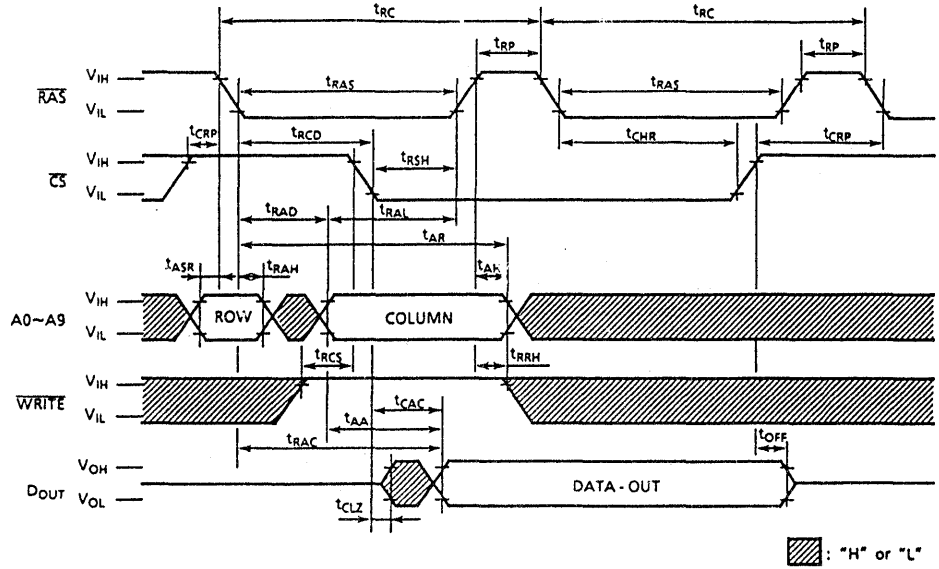
Note: WRITE = "H" or "L", A9 = "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

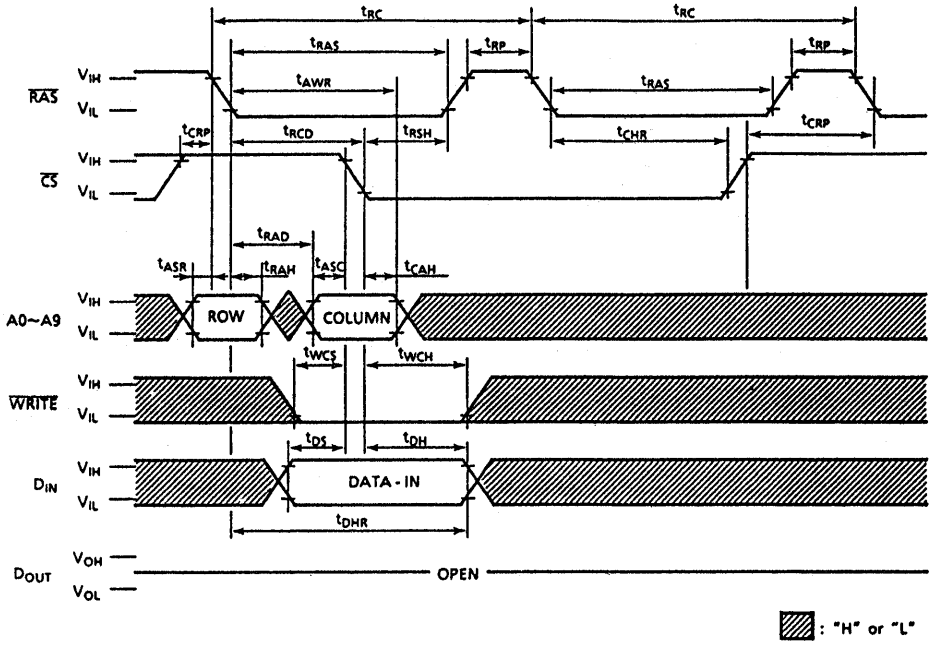


Note: WRITE = "H" or "L", A0~A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)

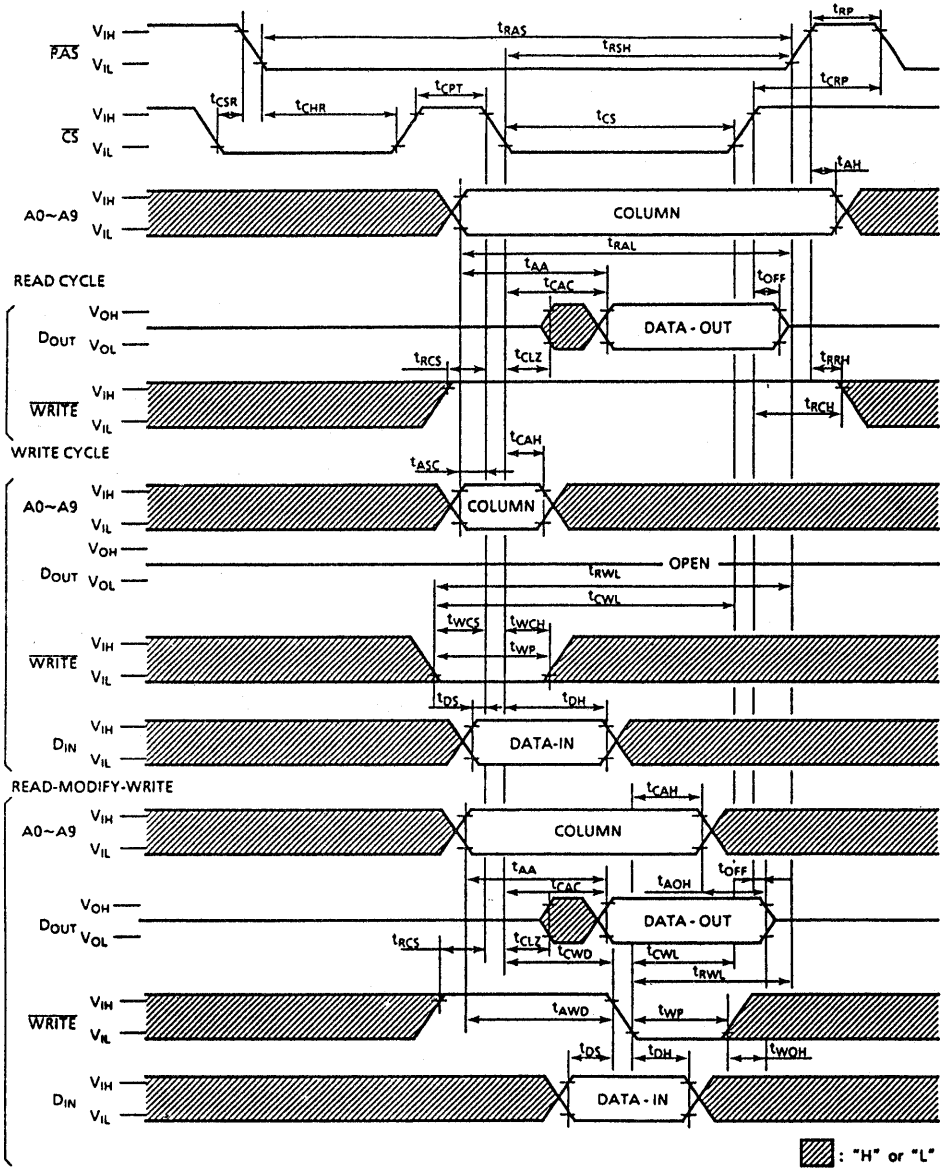


HIDDEN REFRESH CYCLE (WRITE)



Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



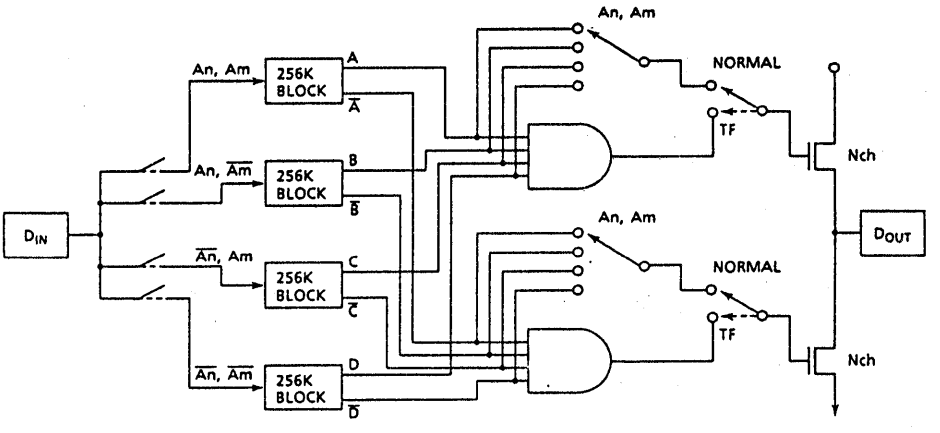
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

TEST MODE

The TC511002BP/BJ/BZ/BFT is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or "L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511002BP/BJ/BZ/BFT including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = $V_{IL\ (TF)}$ level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi - Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Static Column Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to $V_{IL\,(TF)}$ level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

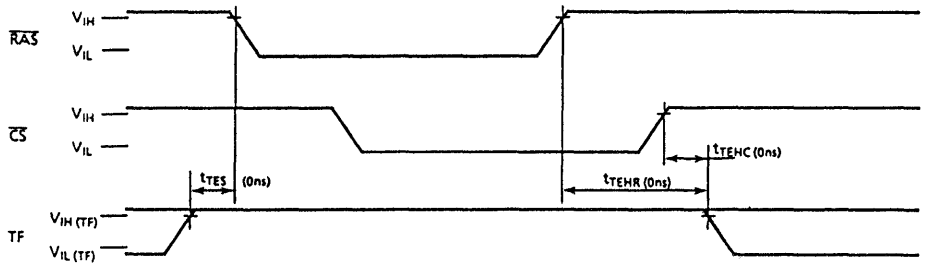


Fig. 2 Test Mode Cycle

TENTATIVE DATA
1,048,576 WORD × 1 BIT DYNAMIC RAM

DESCRIPTION

The TC511002AP/AJ/AZ is the new generation dynamic RAM organized 1,048,576 words by 1 bit. The TC511002AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511002AP/AJ/AZ to be packaged in a standard 18 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 1,048,576 word by 1bit organization
- Fast access time and cycle time

		TC511002AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static Column Mode Cycle Time	40ns	45ns	55ns

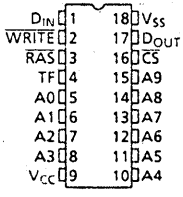
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating (TC511002AP/AJ/AZ-70)
  - 385mW MAX. Operating (TC511002AP/AJ/AZ-80)
  - 330mW MAX. Operating (TC511002AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Output unlatched at cycle end allows two-dimensional chip selection
- Common I/O capability
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Static Column Mode and Test Mode capability
- All inputs and output TTL compatible
- 512 refresh cycles/8ms
- Package TC511002AP : DIP18-P-300C
  TC511002AJ : SOJ26-P-300
  TC511002AZ : ZIP20-P-400

PIN NAMES

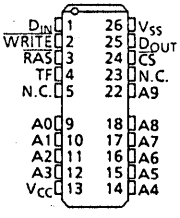
A0~A9	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
D_{IN}	Data In	V_{SS}	Ground
D_{OUT}	Data Out	TF	Test Function
$\overline{CS}$	Chip Select Input	N.C.	No Connection

PIN CONNECTION (TOP VIEW)

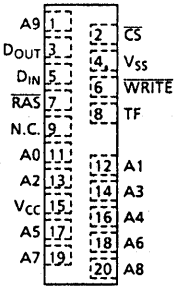
Plastic DIP



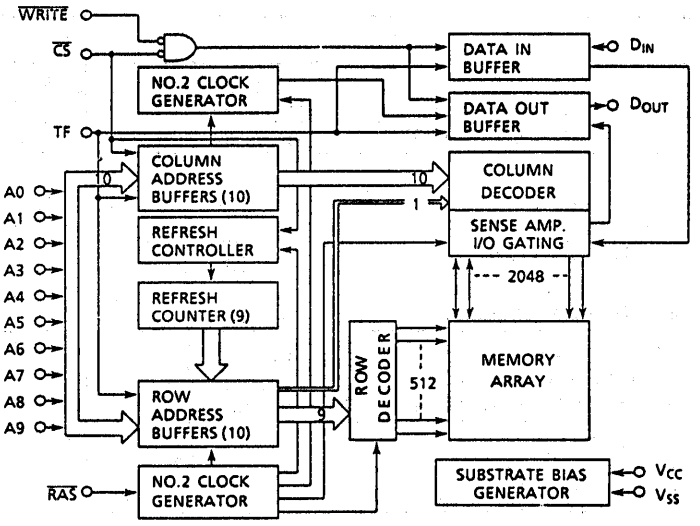
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Test Function Input Voltage	$V_{IN\,(TF)}$	−1~10.5	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2
$V_{IH\,(TF)}$	Test Enable Input High Voltage	V_{CC} + 4.5	−	10.5	V	2
$V_{IL\,(TF)}$	Test Disable Input Low Voltage	−1.0		V_{CC} + 1.0	V	2

DC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC511002AP/AJ/AZ-80	–	70		
		TC511002AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511002AP/AJ/AZ-70	–	80	mA	3, 5
		TC511002AP/AJ/AZ-80	–	70		
		TC511002AP/AJ/AZ-10	–	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, Static Column Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC511002AP/AJ/AZ-70	–	60	mA	3, 4
		TC511002AP/AJ/AZ-80	–	50		
		TC511002AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511002AP/AJ/AZ-70	–	80	mA	3
		TC511002AP/AJ/AZ-80	–	70		
		TC511002AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT (any input except TF) Input Leakage Current, any input ($0V \leq V_{IH} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{ITF(L)}$	INPUT LEAKAGE CURRENT (only TF) ($0V \leq V_{IN(TF)} \leq V_{CC} + 0.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq +5.5V$)		– 10	10	μA	
I_{TF}	TEST FUNCTION INPUT CURRENT ($V_{CC} + 4.5V \leq V_{IN(TF)} \leq 10.5V$)		–	1	mA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage ($I_{OUT} = -5mA$)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage ($I_{OUT} = 4.2mA$)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(VCC = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC511002AP/AJ/AZ-70		TC511002AP/AJ/AZ-80		TC511002AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	155	–	175	–	210	–	ns	
t_{SC}	Static Column Mode Cycle Time	40	–	45	–	55	–	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	70	–	80	–	100	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9, 14
t_{CAC}	Access Time from $\overline{CS}$	–	20	–	20	–	25	ns	9, 14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9, 15
t_{ALW}	Access Time from Last Write	–	65	–	75	–	95	ns	9, 16
t_{CLZ}	$\overline{CS}$ to Output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	–	5	–	5	–	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	–	20	–	20	–	25	ns	
t_{WOH}	Output Data Hold Time from $\overline{WRITE}$	0	–	0	–	0	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	100,000	20	100,000	25	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	CHARACTERISTIC	TC511002AP/ AJ/AZ-70		TC511002AP/ AJ/AZ-80		TC511002AP/ AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ SYCLE)	80	–	90	–	115	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	–	5	–	10	–	ns	17
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	20	–	25	–	ns	
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	65	–	75	–	95	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	13
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time	20	–	20	–	25	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	70	–	80	–	100	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	35	–	40	–	50	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time ($\overline{CS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time ($\overline{CS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	0	–	0	–	0	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	CHARACTERISTIC	TC511002AP/AJ/AZ-70		TC511002AP/AJ/AZ-80		TC511002AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test)	40	–	40	–	50	–	ns	
t_{TES}	Test Mode Enable Set-Up Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHR}	Test Mode Enable Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	
t_{TEHC}	Test Mode Enable Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	

CAPACITANCE (VCC = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

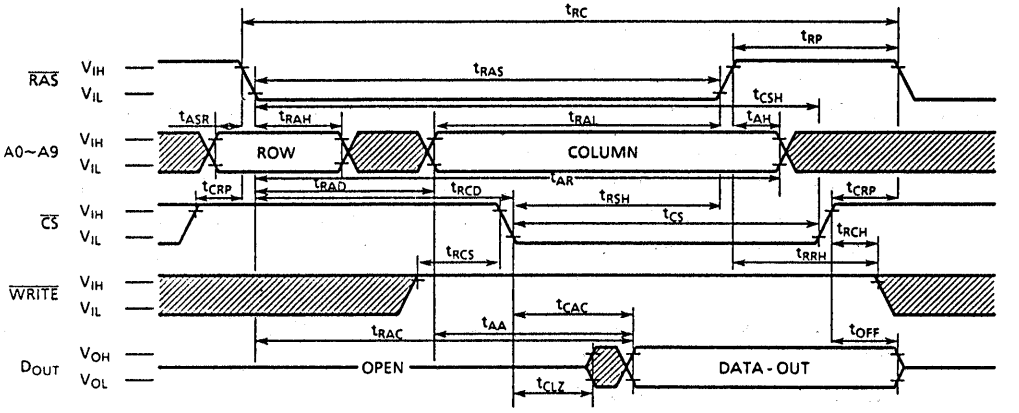
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, D_{IN})	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, TF)	–	7	
C_O	Output Capacitance (D_{OUT})	–	7	

NOTES:

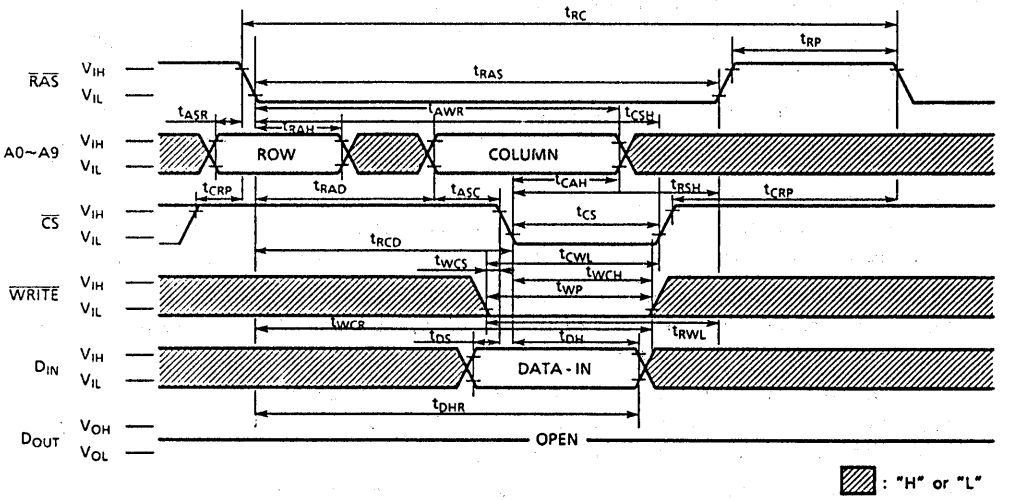
1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ Before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in read-modify-write.
13. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (min.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
16. Operation within the t_{LWAD}(max.) limit insures that t_{ALW}(max.) can be met. t_{LWAD}(max.) is specified as a reference point only: If t_{LWAD} is greater than the specified t_{LWAD}(max.) limit, then access time is controlled exclusively by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has risen up.

TIMING WAVEFORMS

READ CYCLE

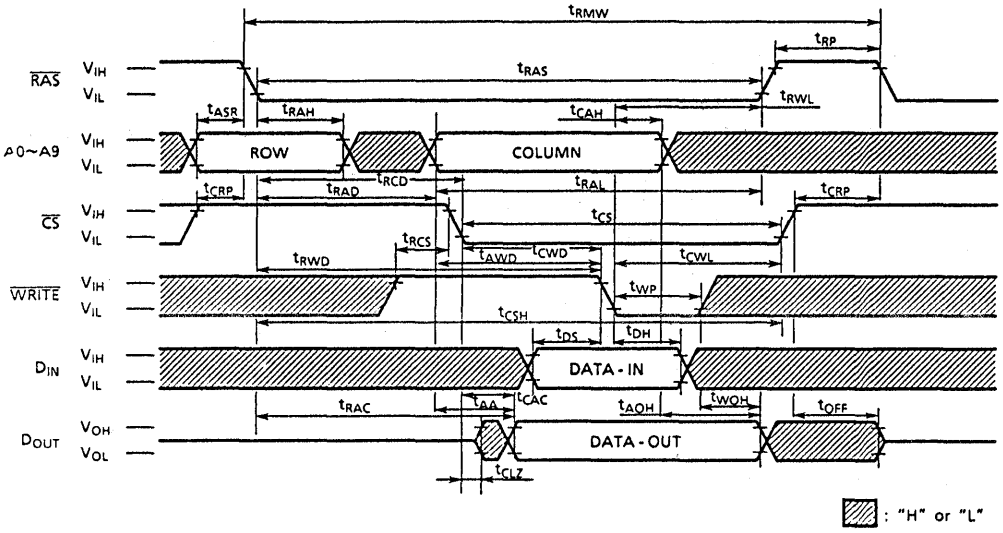


WRITE CYCLE (EARLY WRITE)



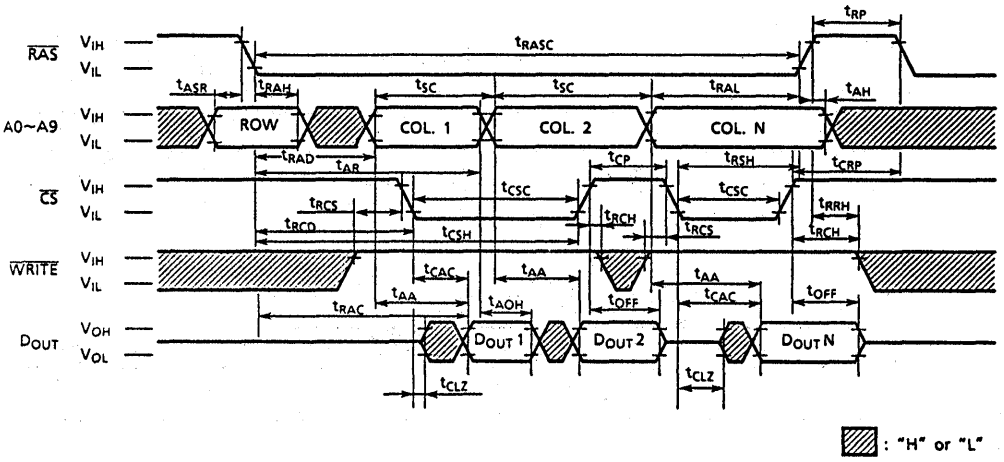
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

READ - MODIFY - WRITE CYCLE



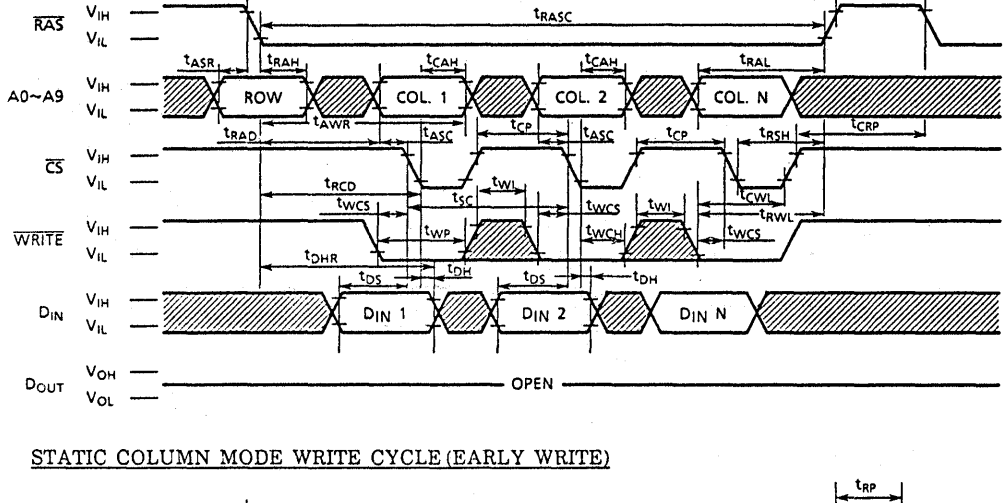
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ CYCLE

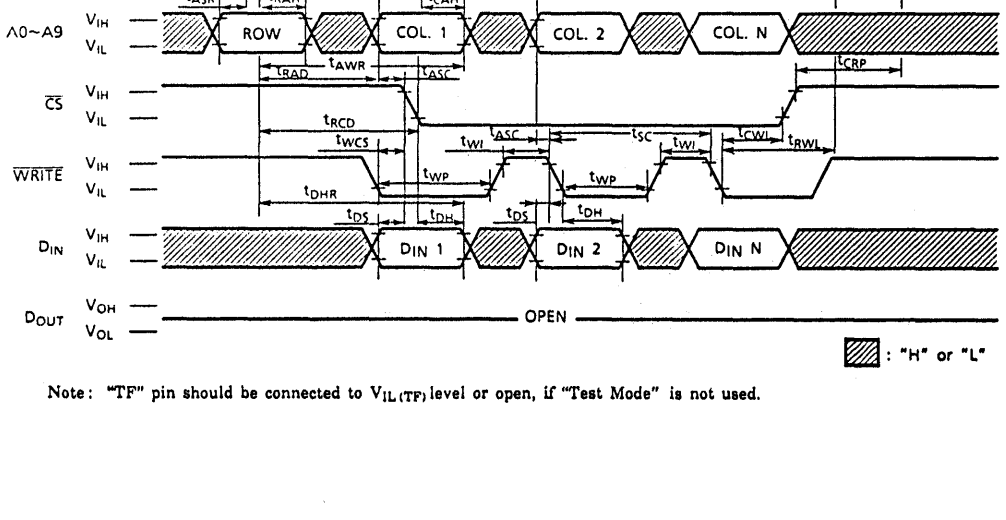


Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

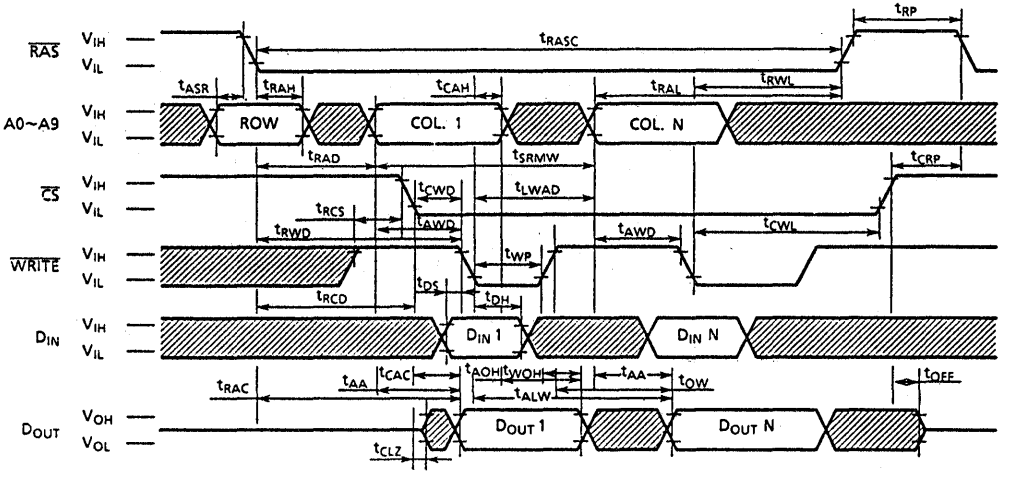


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

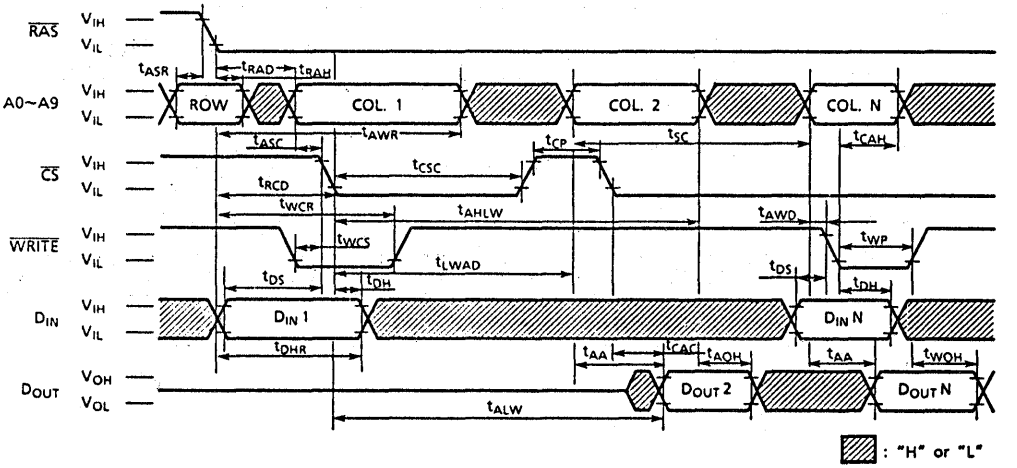


Note: "TF" pin should be connected to $V_{IL(TF)}$ level or open, if "Test Mode" is not used.

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE

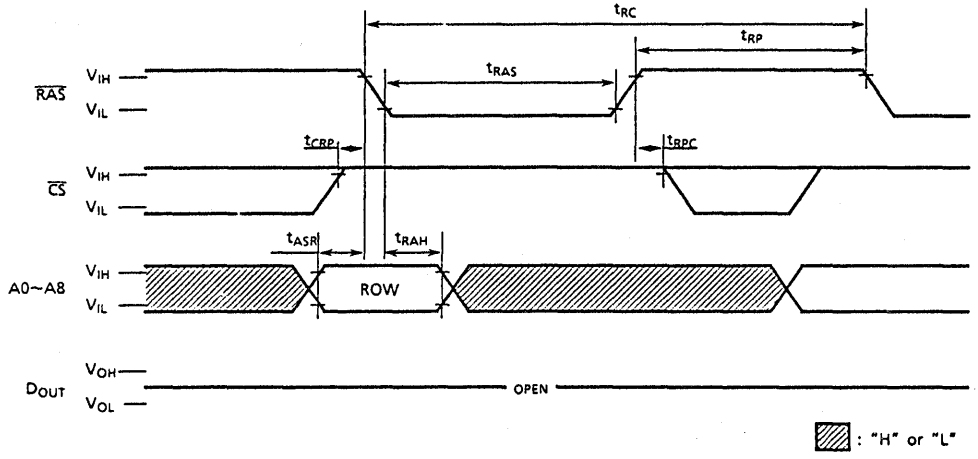


STATIC COLUMN MODE READ/WRITE MIXED CYCLE



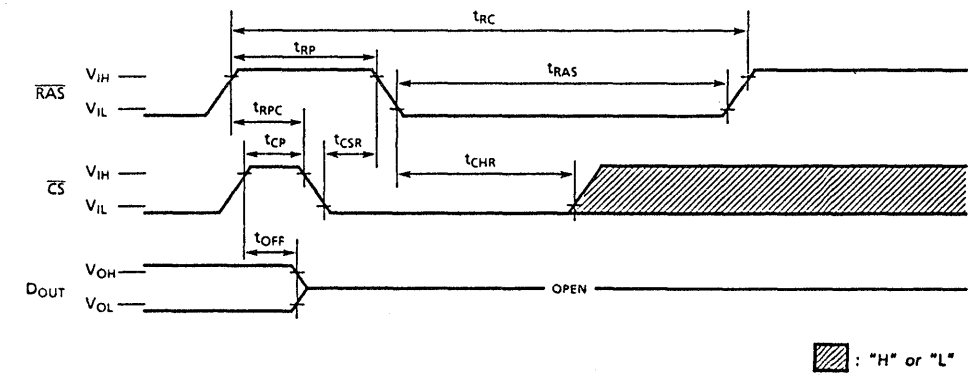
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

$\overline{RAS}$ ONLY REFRESH CYCLE



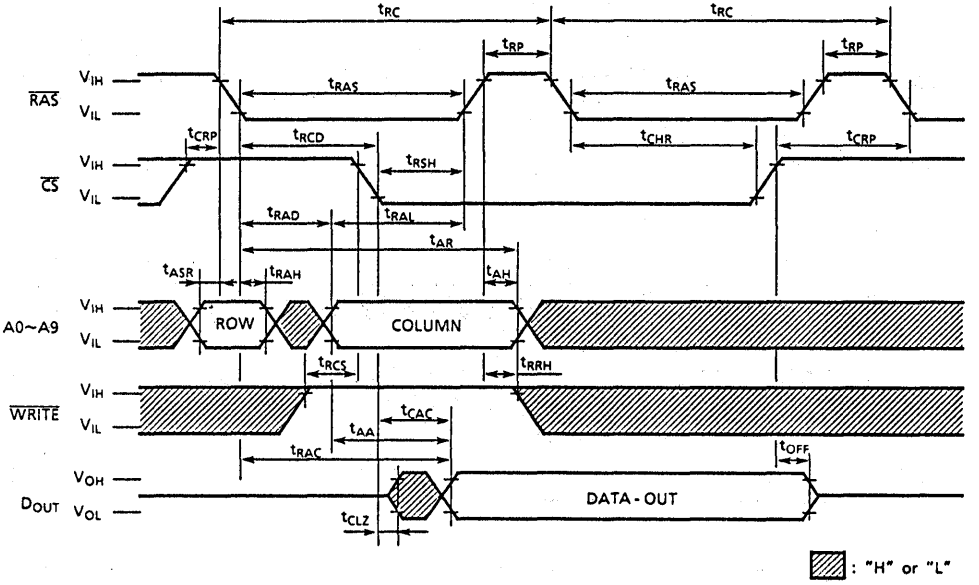
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

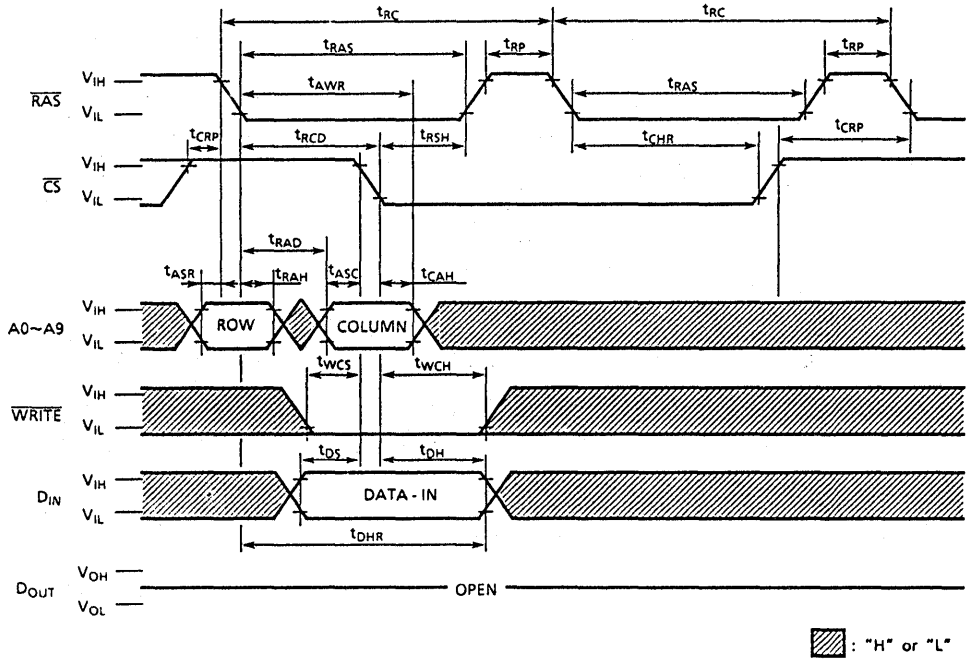


Note: $\overline{WRITE}$ = "H" or "L", A0~A9 = "H" or "L"
"TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

HIDDEN REFRESH CYCLE (READ)

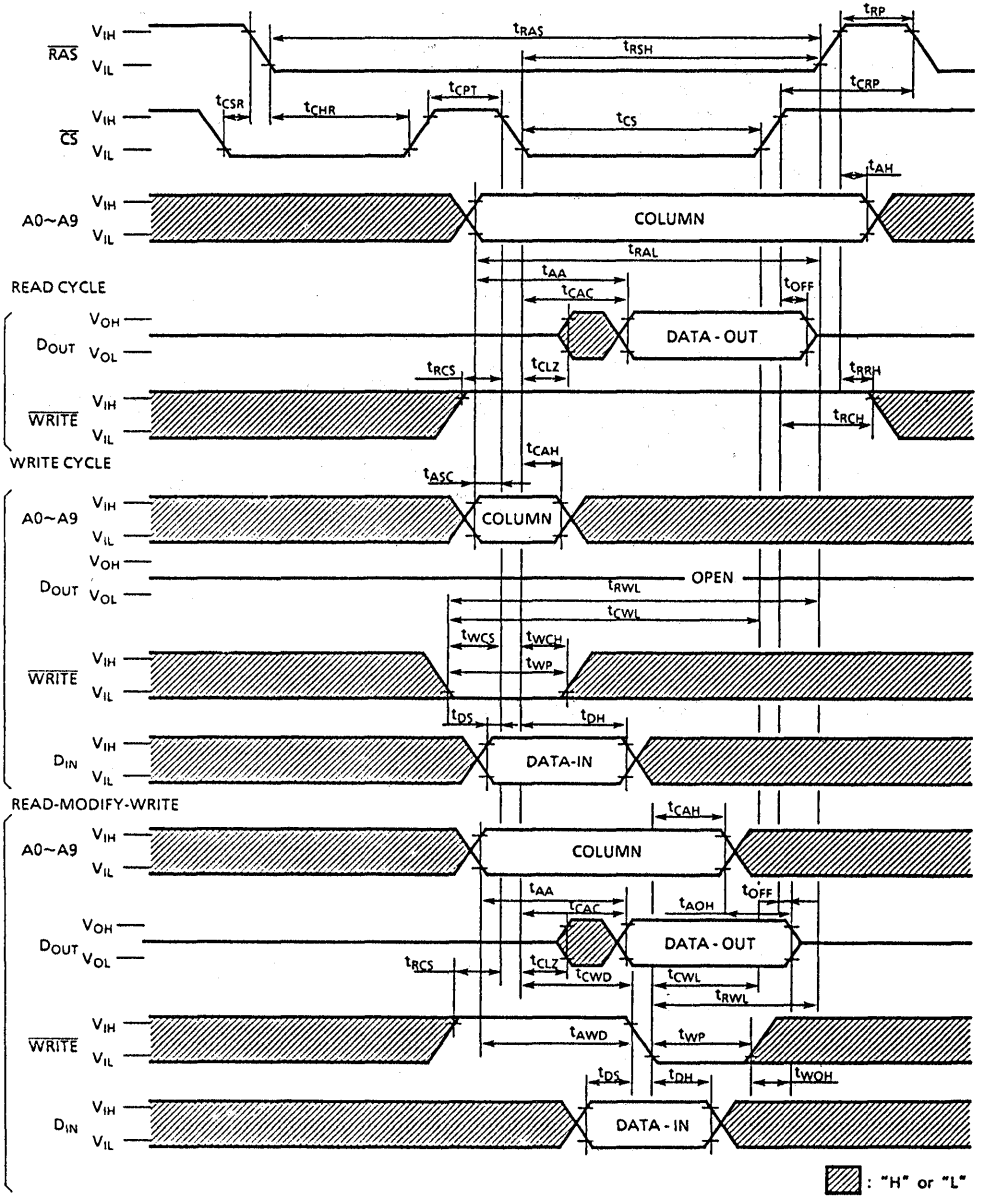


HIDDEN REFRESH CYCLE (WRITE)



Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



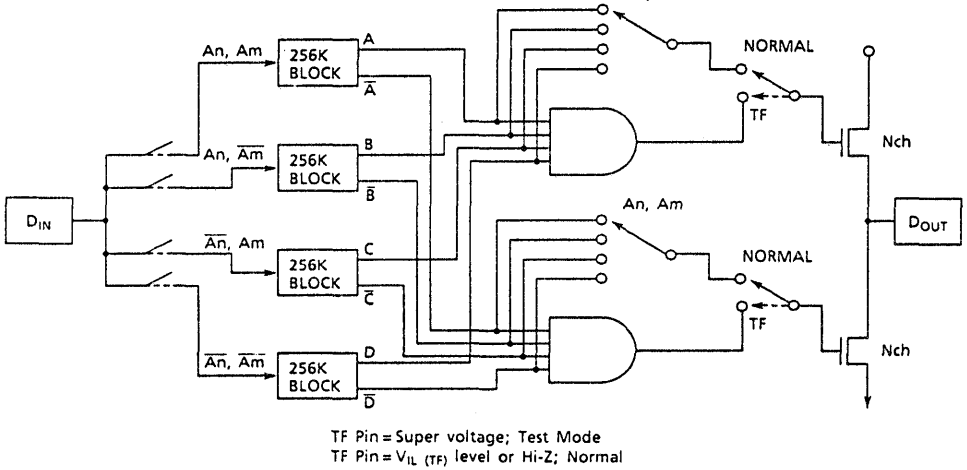
Note: "TF" pin should be connected to $V_{IL\,(TF)}$ level or open, if "Test Mode" is not used.

TEST MODE

The TC511002AP/AJ/AZ is the RAM organized 1,048,576 words by 1 bit, it is internally organized 262,144 words by 4 bits. In "Test Mode", data is written into a number of sectors (4 sectors) in parallel and retrieved the same way. If, upon reading, all bits are equal (all "H" or"L"), the data output pin indicates a same data as all bits. In this case, the data output pin indicates an expected data for good parts, the data output pin indicates a complementary data for bad parts. And also, if any of the bits differed, the data output pin would indicate a high impedance state for bad parts. Fig. 1 shows the block diagram of TC511002AP/AJ/AZ including its truth table when "Test Mode" is used.

In test mode, 1MDRAM can be tested as if it were 256K DRAM by the following method.

Block Diagram in Test Mode



TF Pin = Super voltage; Test Mode
TF Pin = $V_{IL\ (TF)}$ level or Hi-Z; Normal

Truth Table in Test Mode Function

A	B	C	D	D_{OUT}
0	0	0	0	0
1	1	1	1	1
Otherwise				Hi-Z

Fig. 1

"Test Mode" function is performed on any of the timing cycles including Static Column Mode when "TF" pin is held on "super voltage (V_{CC}+4.5V (V_{CC}=5V±10%), max. voltage=10.5V)" for the specified period (t_{TES}, t_{TEHR} and t_{TEHC}; see Fig. 2). The address input of A9 is ignored in the "Test Mode".

On the other hand, normal operation requires the "TF" pin be connected to $V_{IL\ (TF)}$ level, or left unconnected on the printed wiring board.

The "Test Mode" function reduces test times (1/4; in case of using N test pattern).

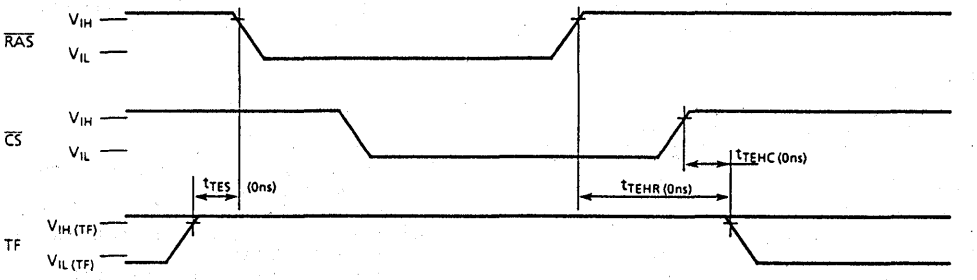


Fig. 2 Test Mode Cycle

262,144 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514256BP/BJ/BZ/BFT is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514256BP/BJ/BZ/BFT to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.

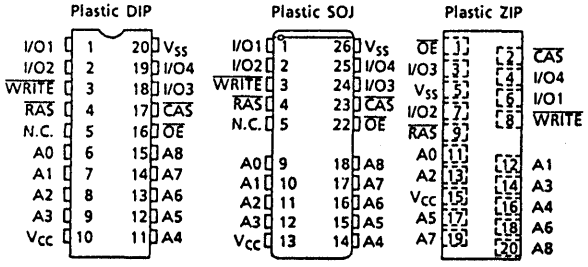
FEATURES

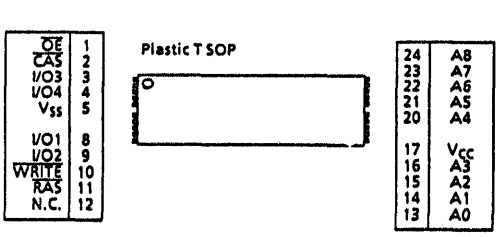
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256BP/BJ/BZ/BFT - 60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode Capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/8ms
- Package TC514256BP : DIP20-P-300B
  TC514256BJ : SOJ26-P-300
  TC514256BZ : ZIP20-P-400
  TC514256BFT : TSOP24-P-0616

PIN CONNECTION

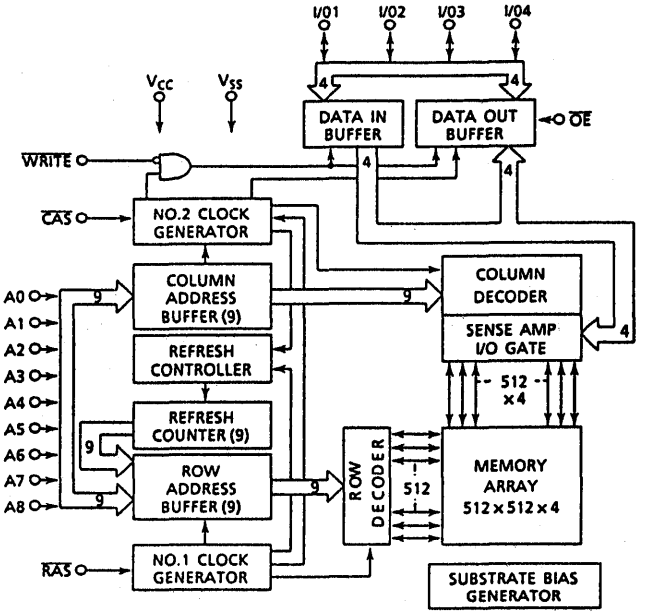




PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514256BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	ns	

ELECTRICAL CHARACTGERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514256BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	12
t_{DH}	Data Hold Time	15	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	

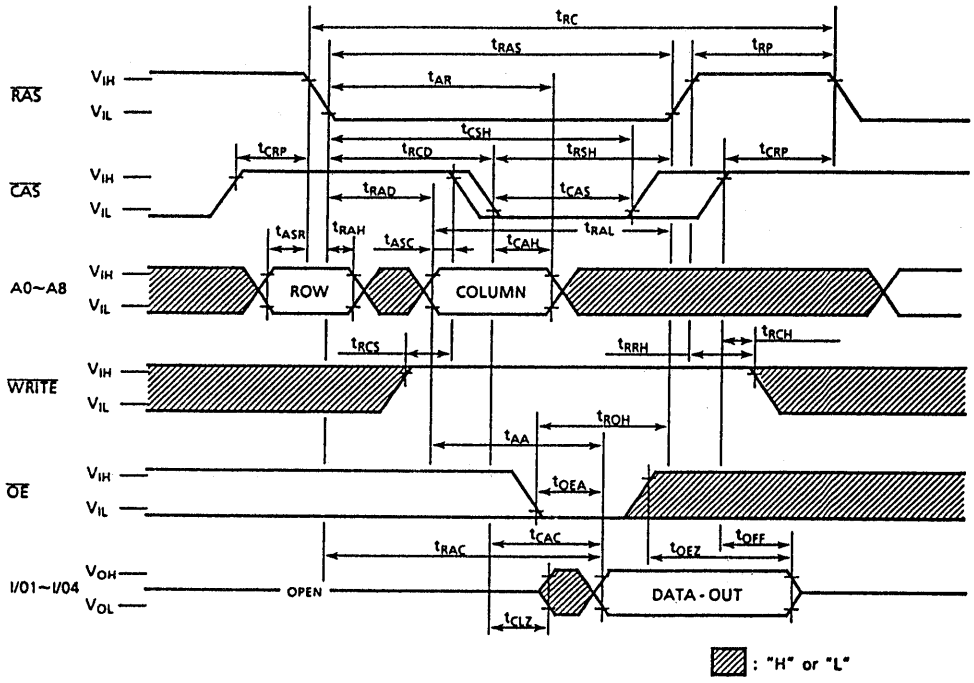
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

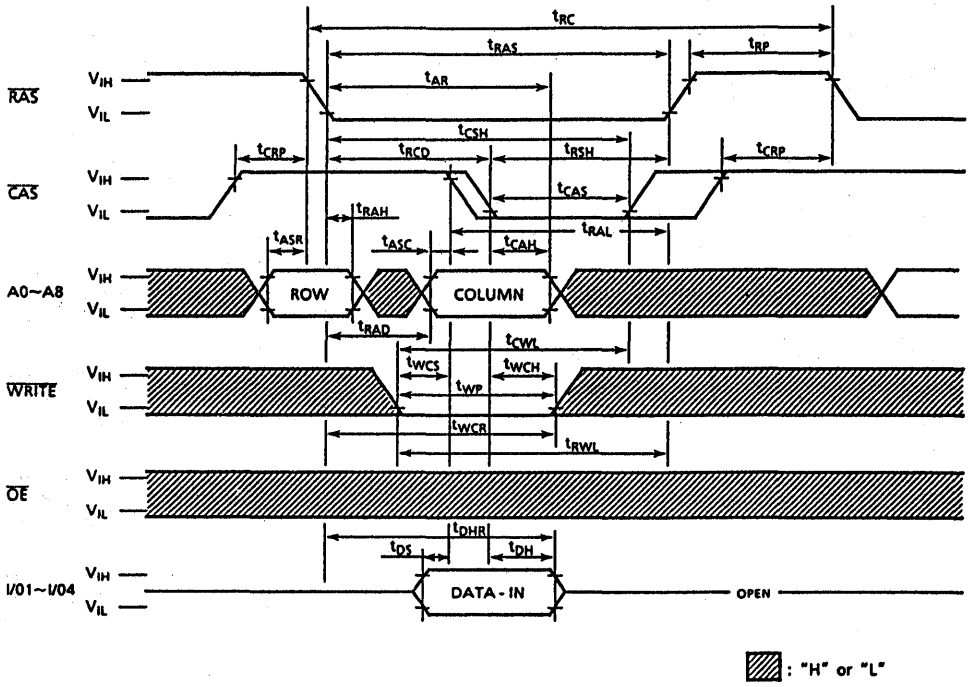
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

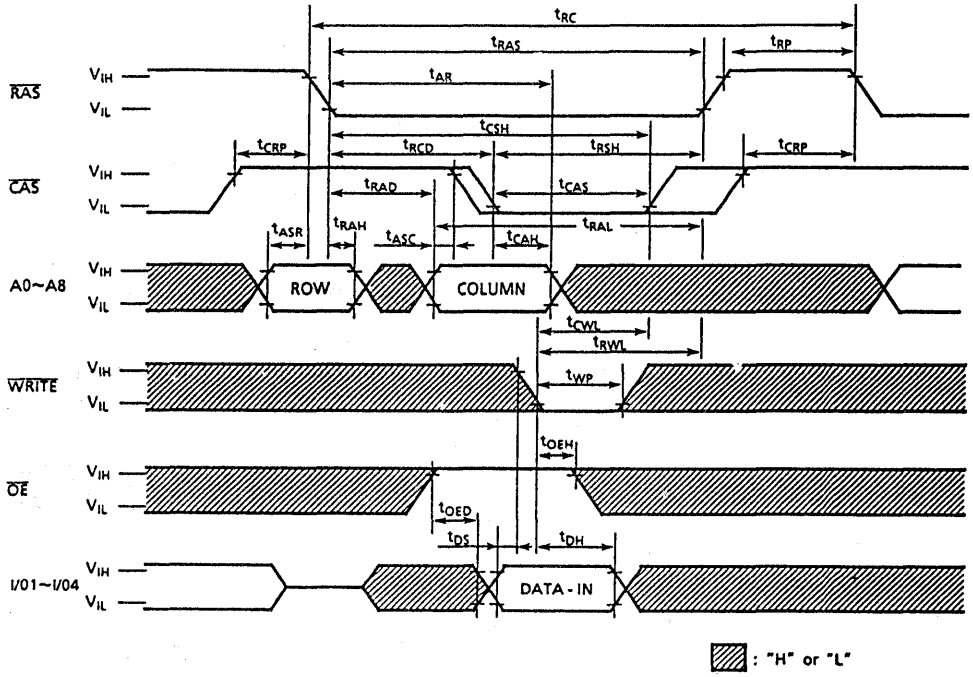
READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tRAD
tCAS
tRAL
tASR
tRAH
tASC
tCAH
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
OE
tOEA
tCAC
tRAC
tOEZ
tOFF
I/O1~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

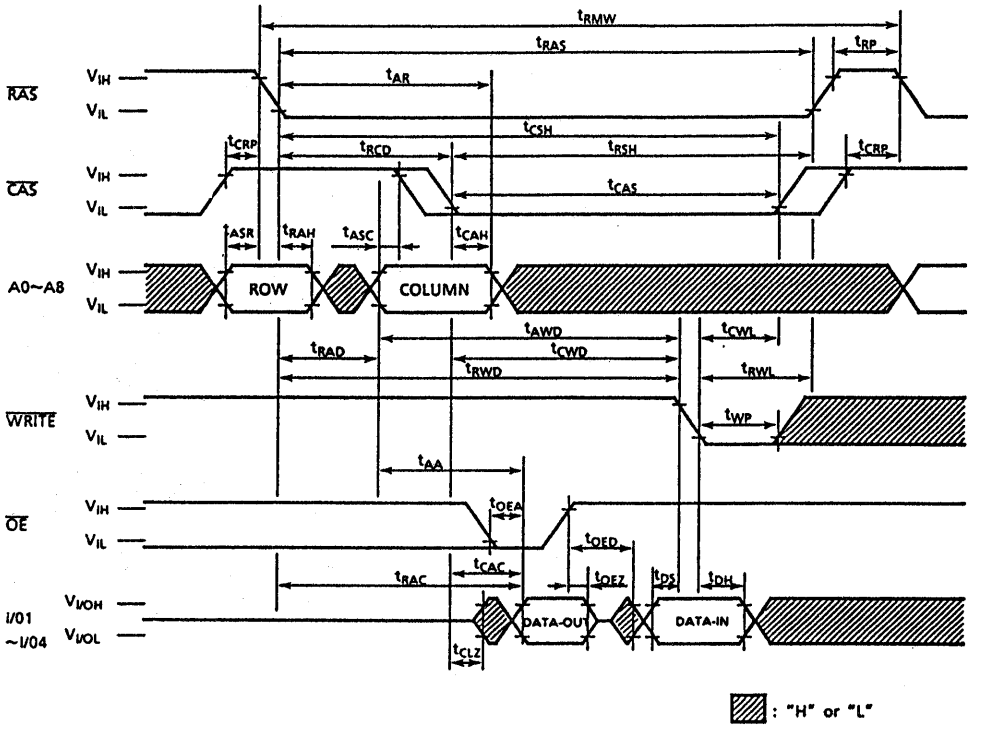
WRITE CYCLE (EARLY WRITE)



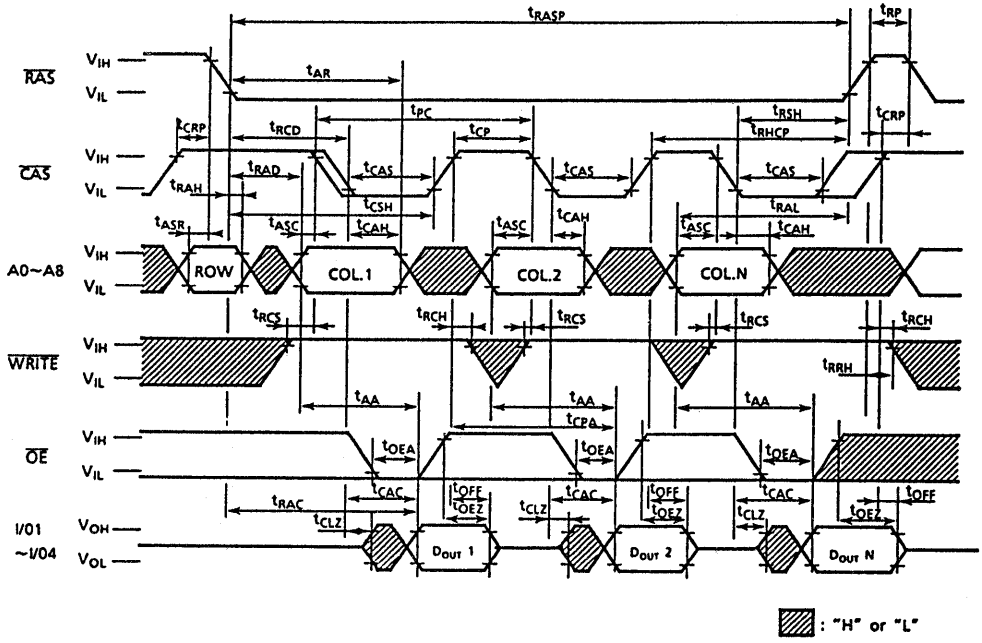
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



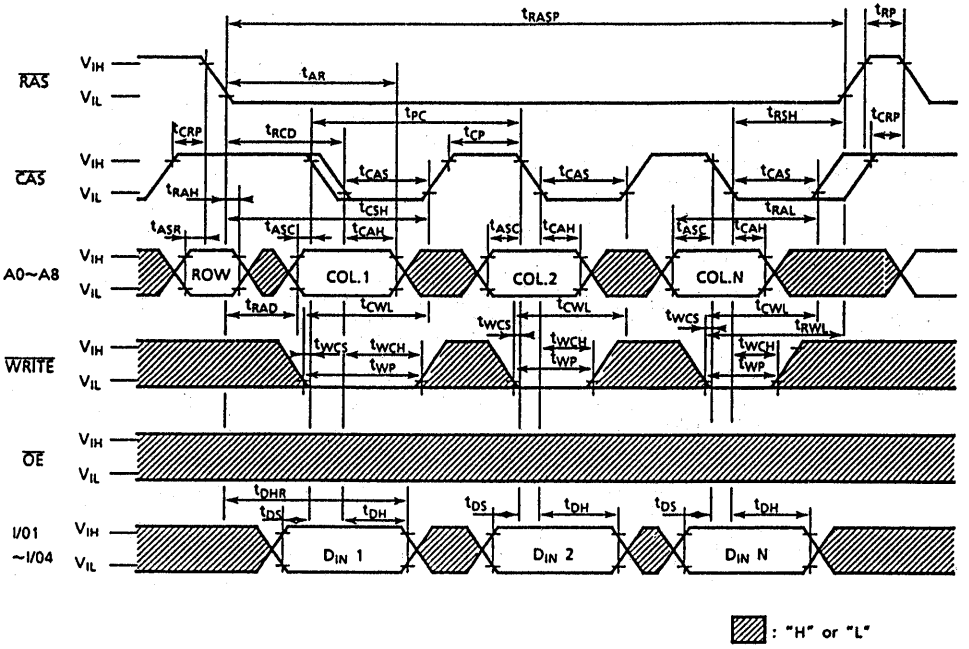
READ-MODIFY-WRITE CYCLE



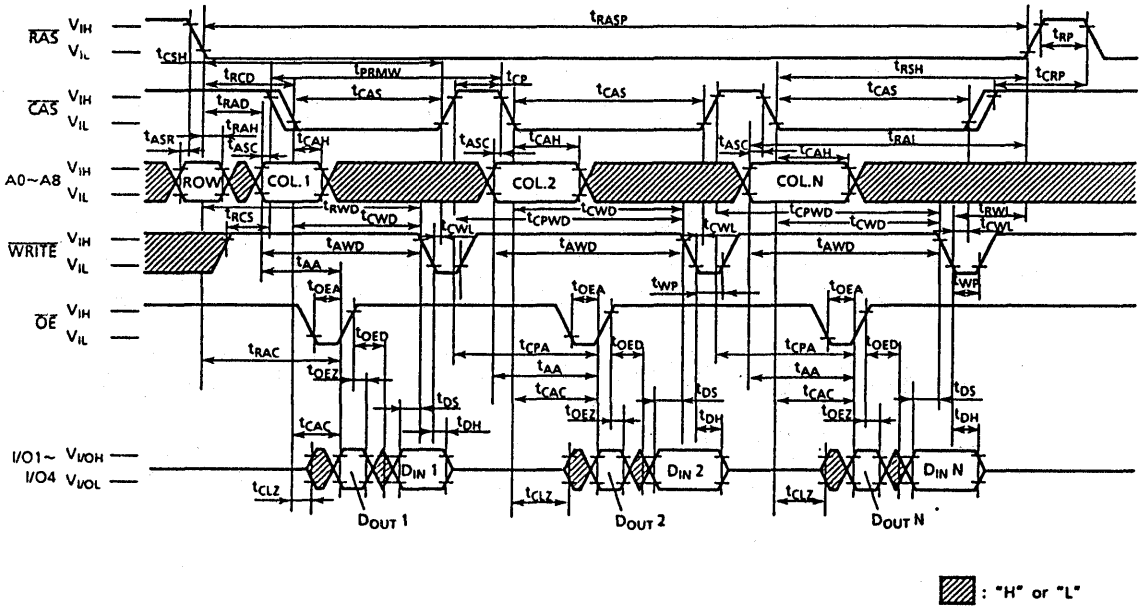
FAST PAGE MODE READ CYCLE



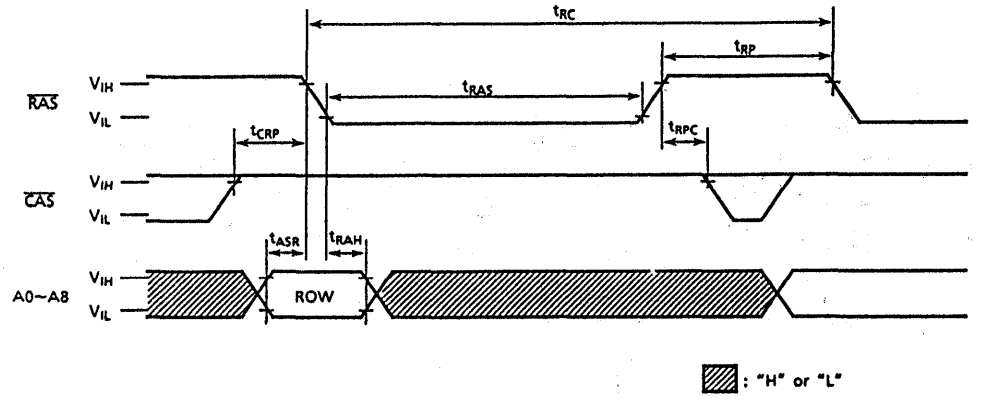
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

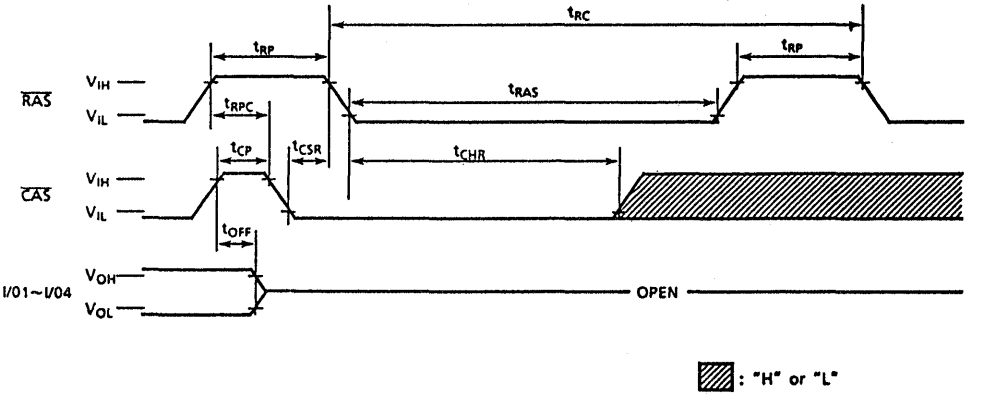


$\overline{RAS}$ ONLY REFRESH CYCLE



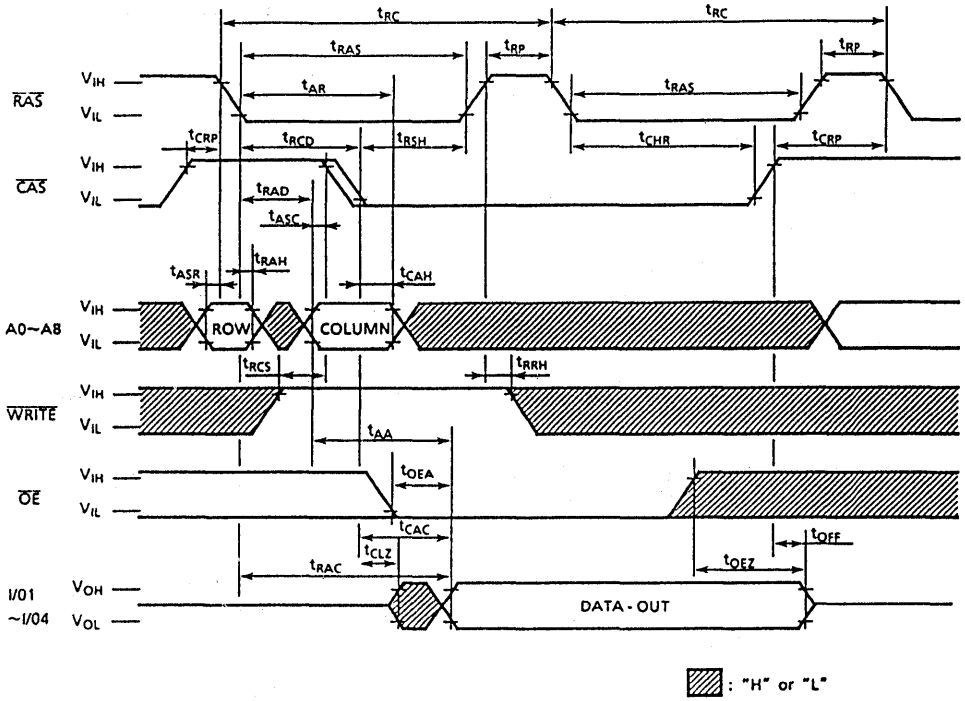
Note: WRITE, $\overline{OE}$="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

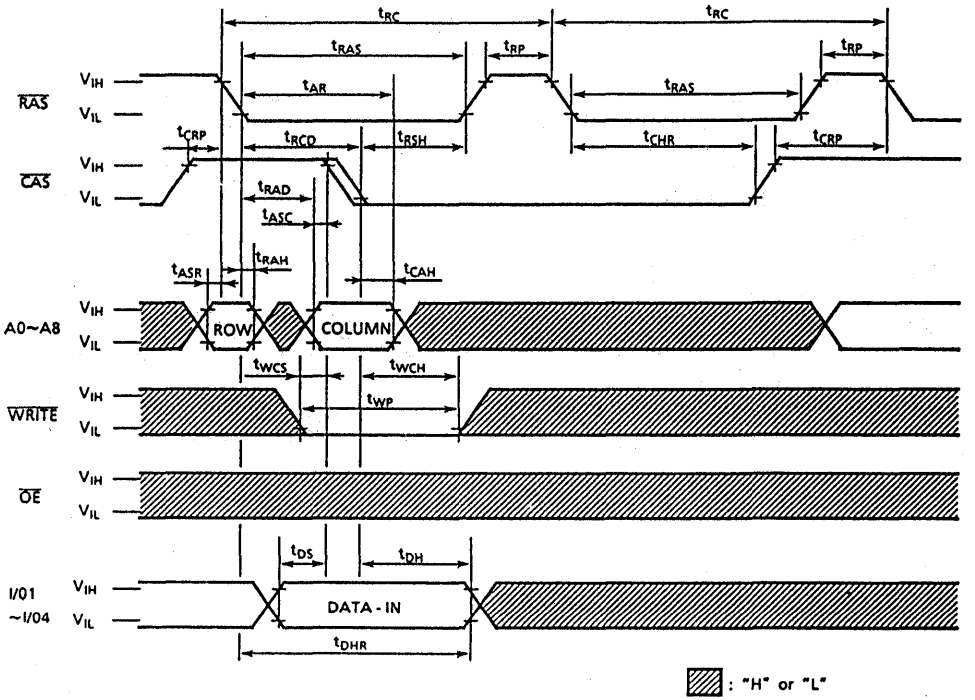


Note: WRITE, $\overline{OE}$=A0~A8="H" or "L"

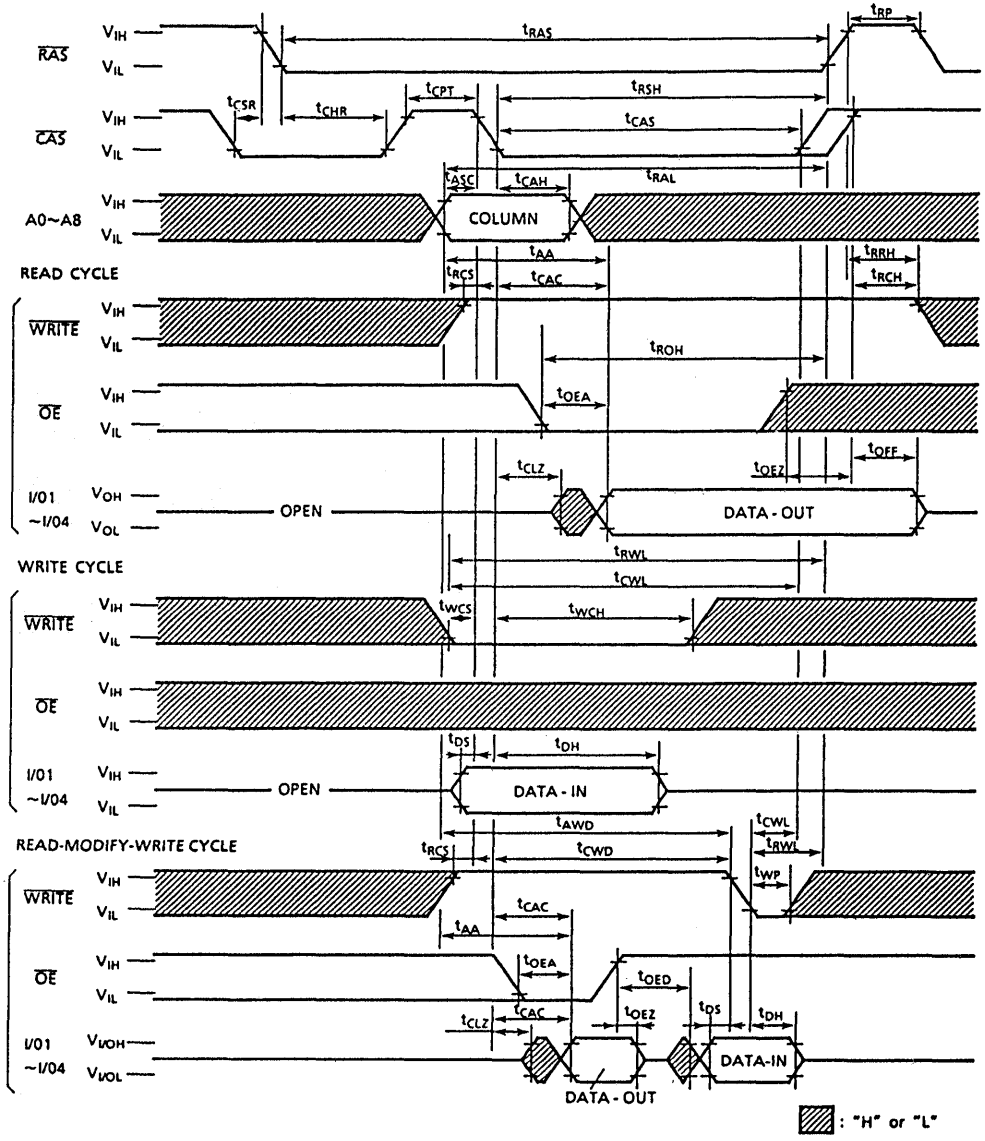
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTES

262,144 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514256BPL/BJL/BZL/BFTL is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256BPL/BJL/BZL/BFTL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514256BPL/BJL/BZL/BFTL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.

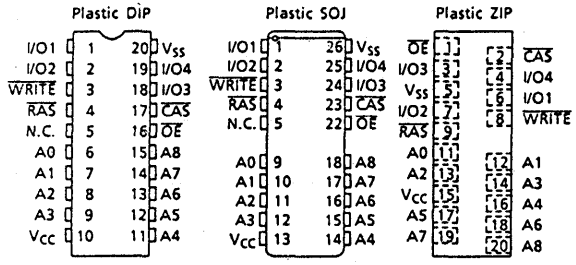
FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256BPL/BJL/BZL/BFTL-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

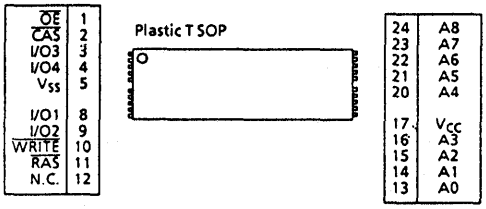
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode Capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/64ms
- Package TC514256BPL : DIP20-P-300B
  TC514256BJL : SOJ26-P-300
  TC514256BZL : ZIP20-P-400
  TC514256BFTL: TSOP24-P-0616

PIN CONNECTION

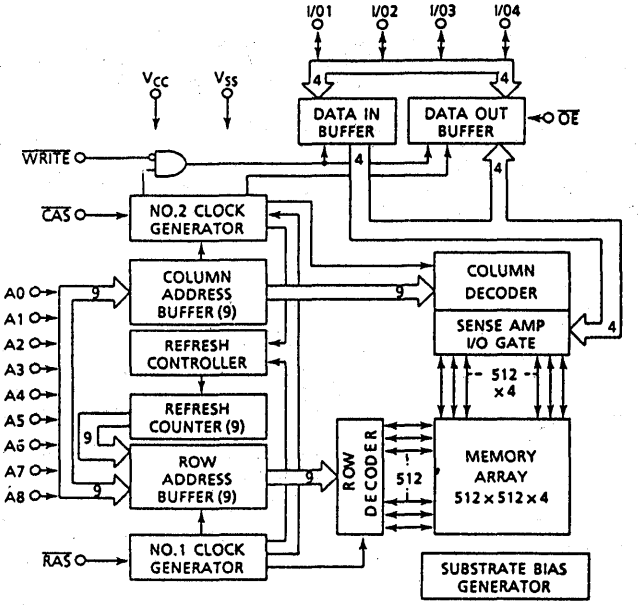


PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1~7	V	1
Output Voltage	V_{OUT}	-1~7	V	1
Power Supply Voltage	V_{CC}	-1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256BPL/BJL/BZL/BFTL-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514256BPL/BJL/BZL/BFTL-60	–	90	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256BPL/BJL/BZL/BFTL-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256BPL/BJL/BZL/BFTL-60	–	90	mA	3
I_{CC7}	BATTERY BACK UP CURRENT Avarage Power Supply Current, BATTERY BACK UP MODE ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V or 0.2V, A0~8 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN. ~1µs)		–	300	µA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 7, 8, 9)

SYMBOL	PARAMETER	TC514256BPL/BJL/BZL/BFTL-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	10,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	10,15
t_{AA}	Access Time from Column Address	-	30	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	ns	10,16
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	12
t_{WCH}	Write Command Hold Time	10	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514256BPL/BJL/BZL/BFTL-60		UNITS	NOTES
		MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	13
t_{DH}	Data Hold Time	15	–	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	64	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	ns	

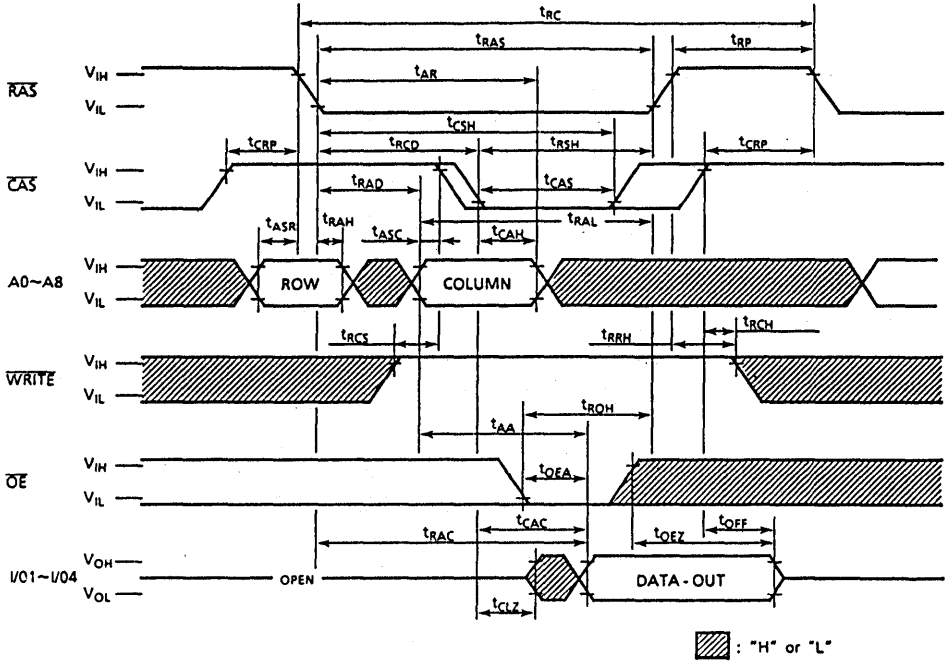
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

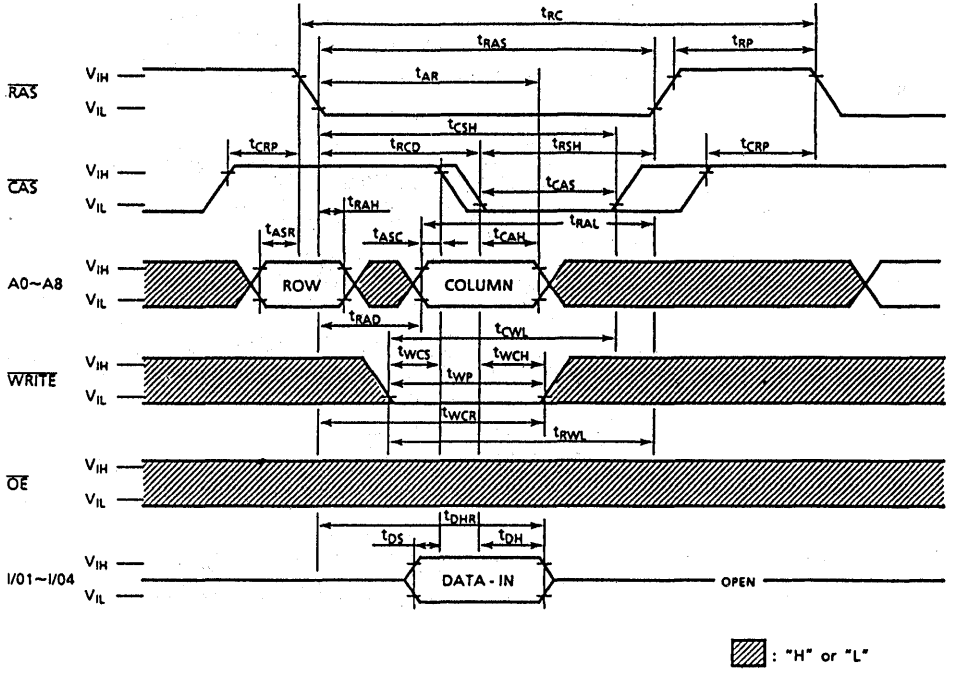
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
8. AC measurements assume t_T = 5ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

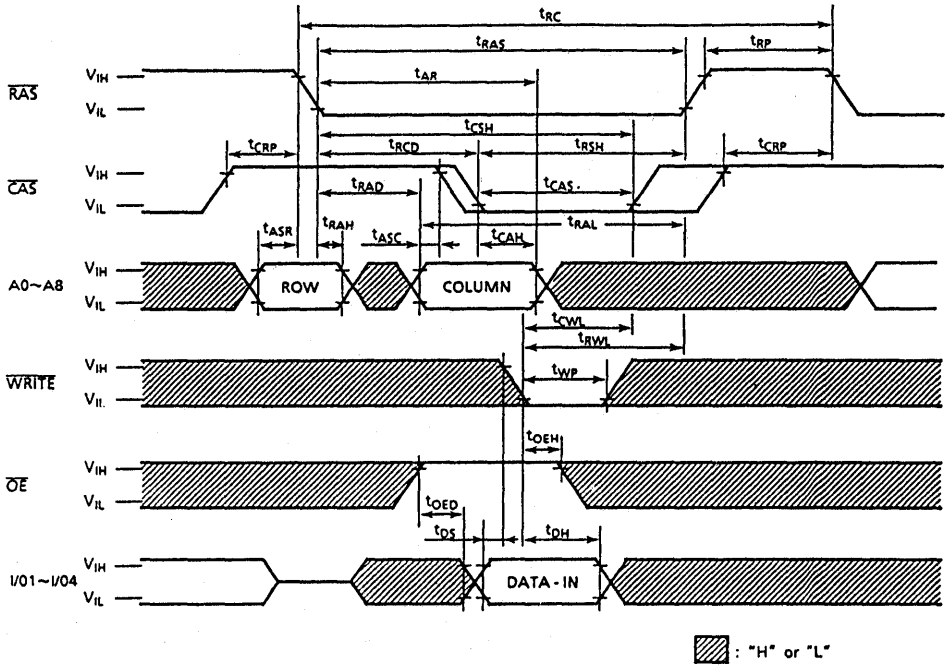
READ CYCLE


tRC
tRAS
tRP
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
ROW
COLUMN
tRCS
tRRH
tRCH
tROH
tAA
tOEA
tCAC
tRAC
tOEZ
tOFF
tCLZ
OPEN
DATA-OUT
RAS
CAS
A0~A8
WRITE
OE
I/O1~I/O4
VIH
VIL
VOH
VOL
: "H" or "L"

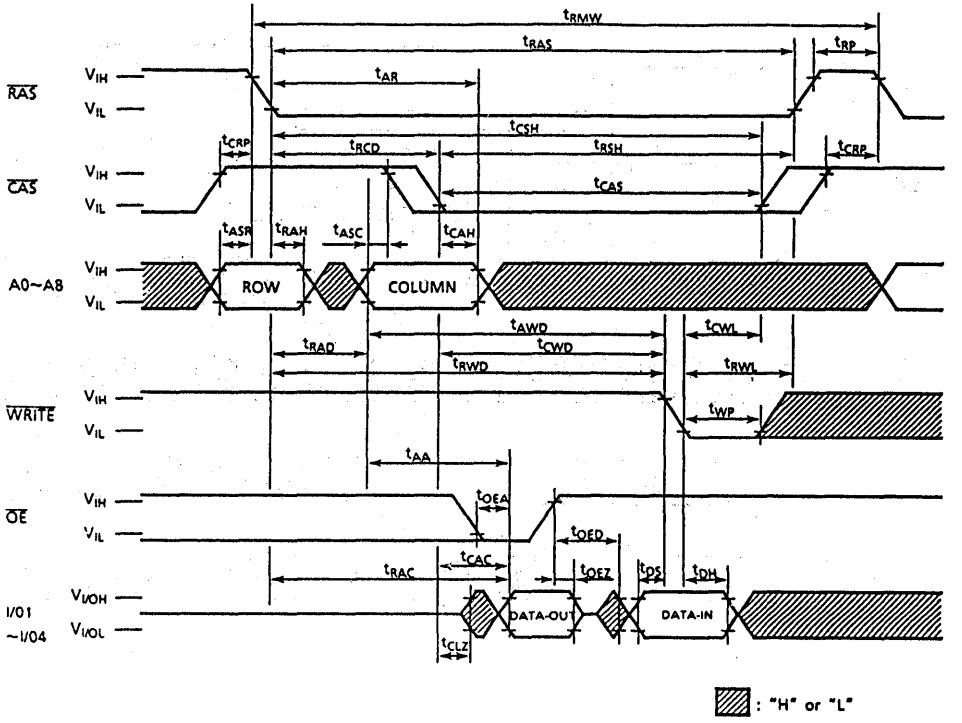
WRITE CYCLE (EARLY WRITE)



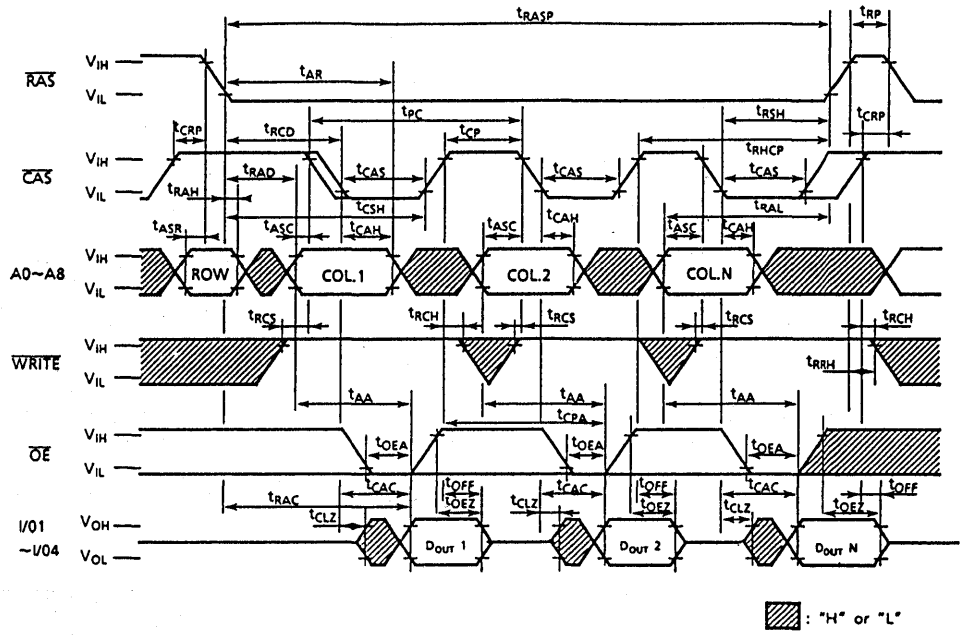
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



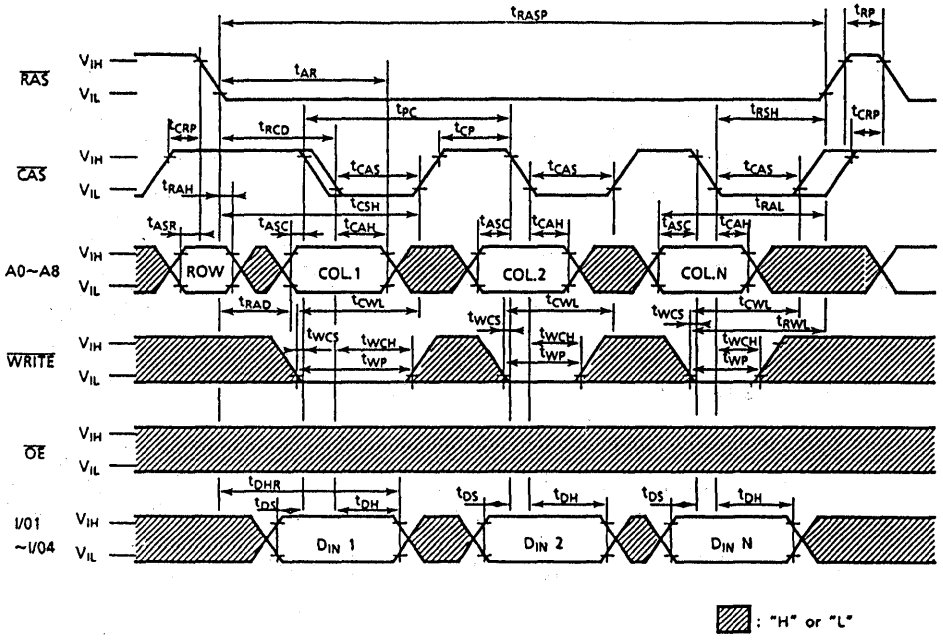
READ-MODIFY-WRITE CYCLE



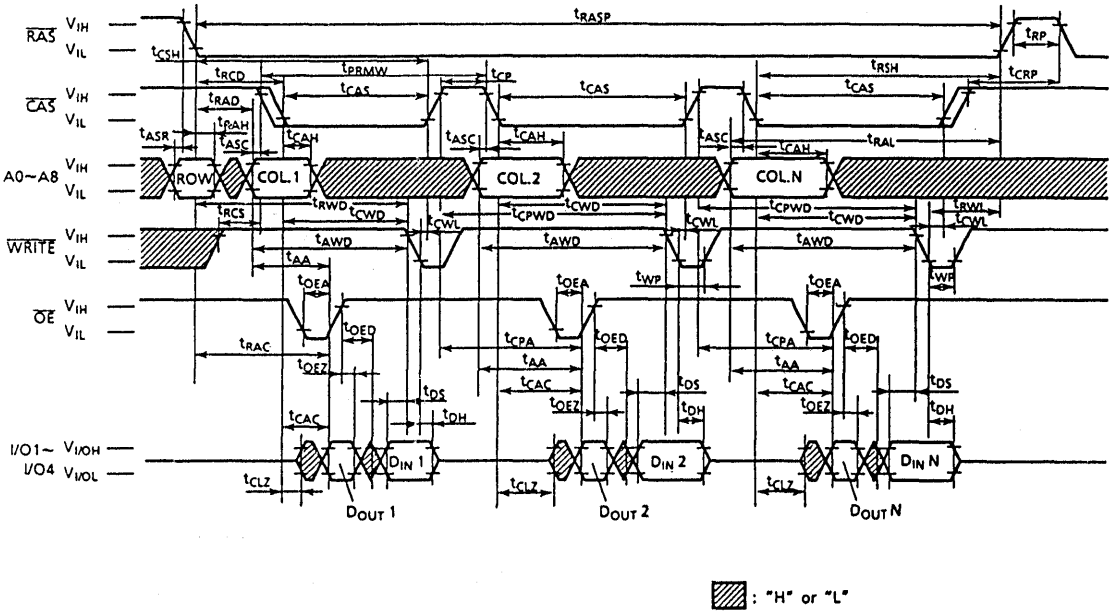
FAST PAGE MODE READ CYCLE



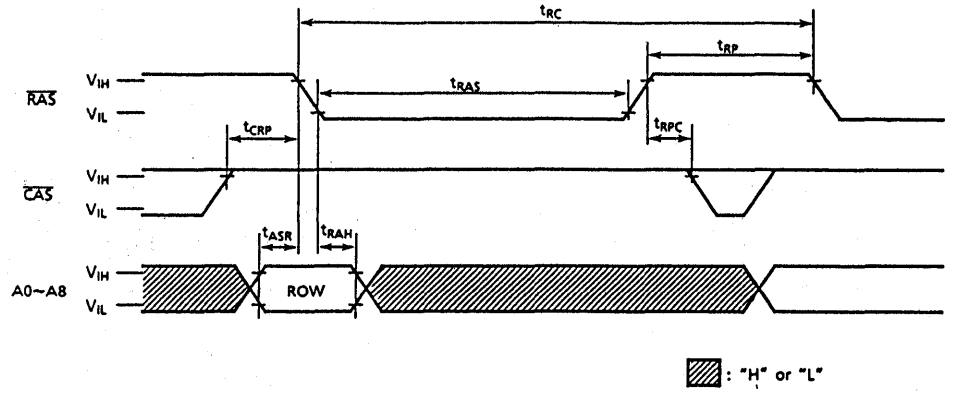
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

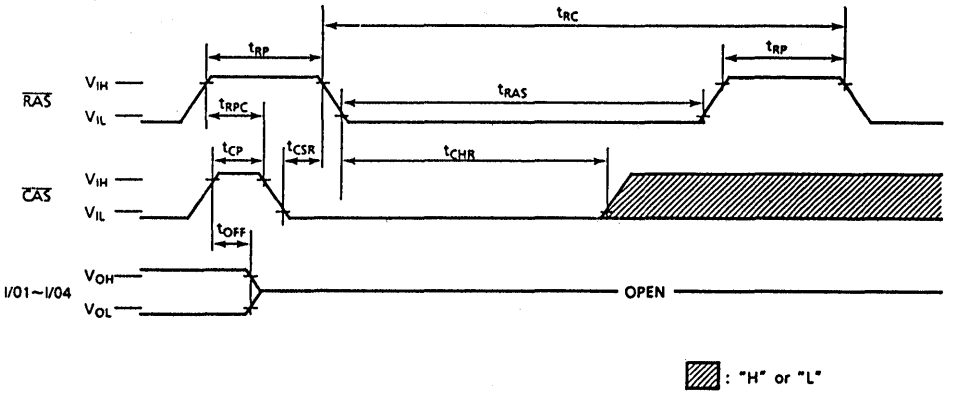


$\overline{RAS}$ ONLY REFRESH CYCLE



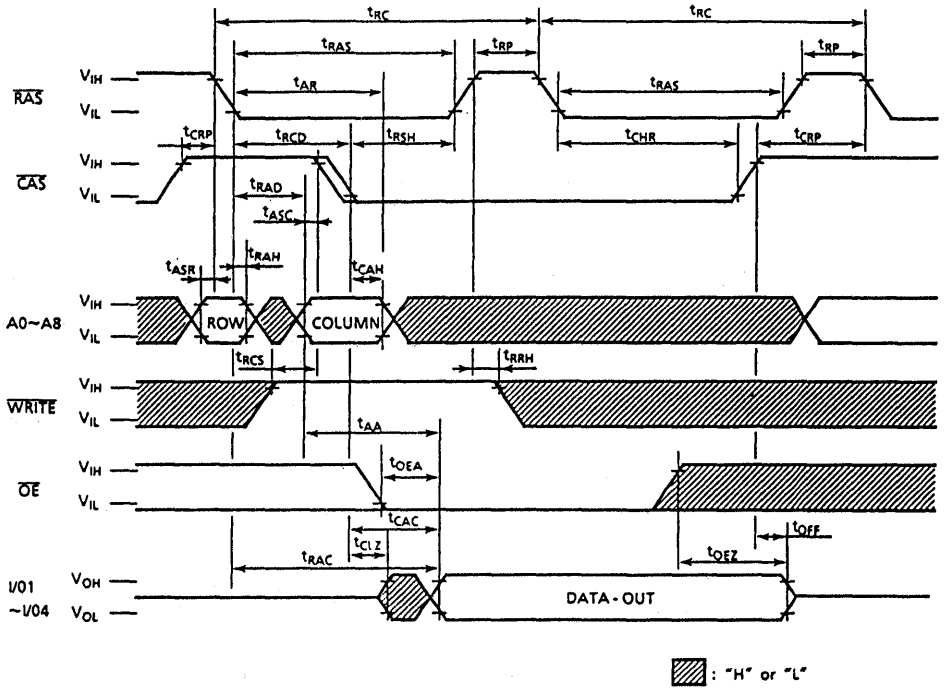
Note: WRITE, $\overline{OE}$="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

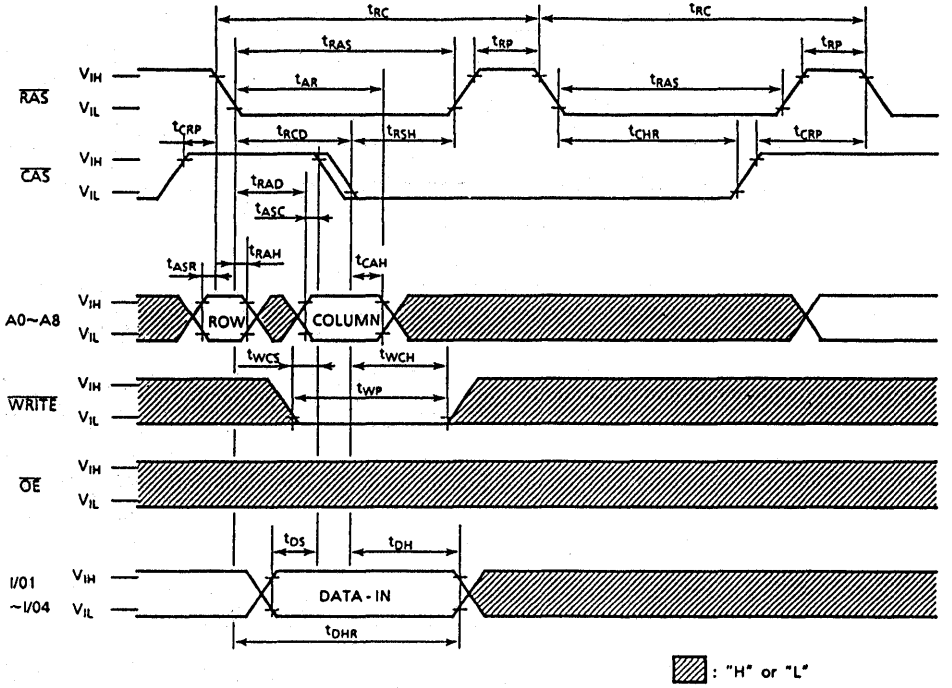


Note: WRITE, $\overline{OE}$=A0~A8="H" or "L"

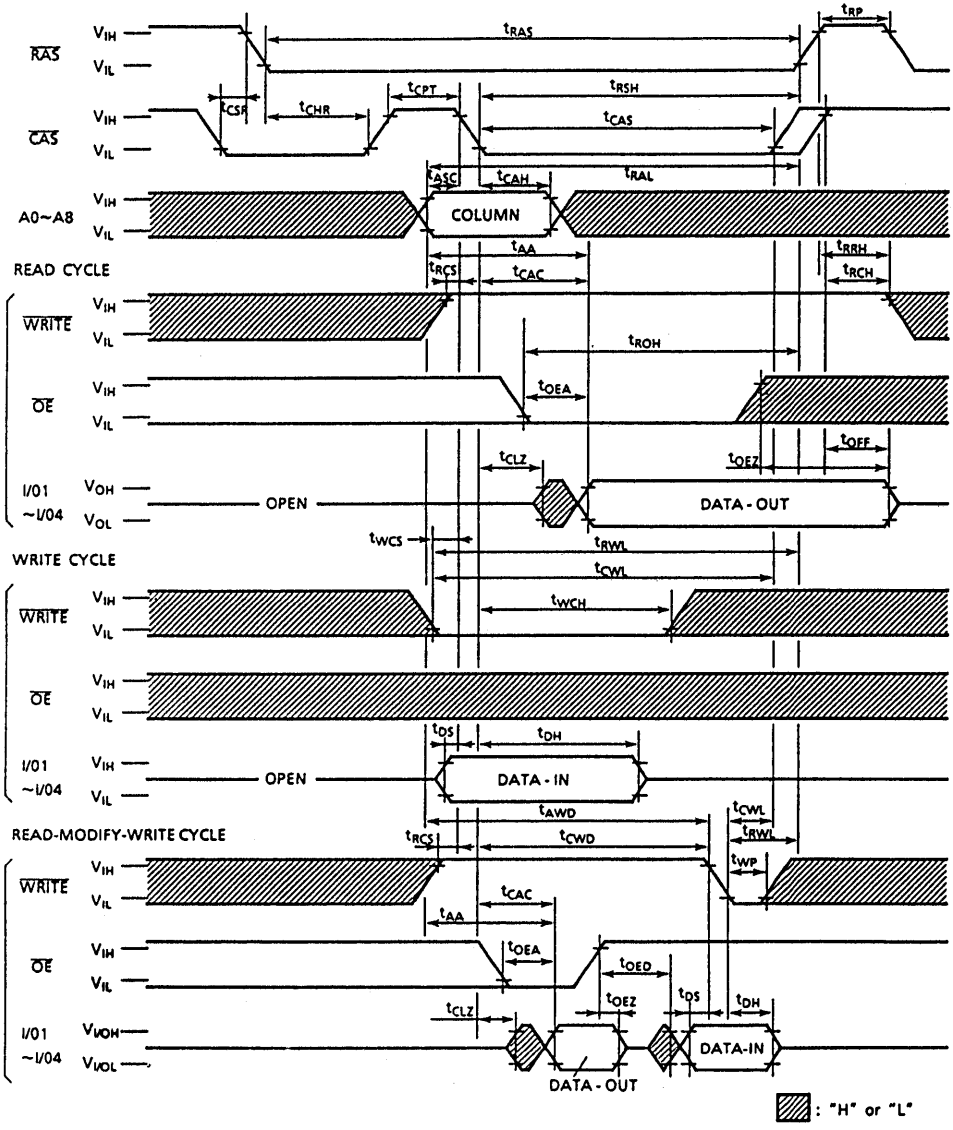
HIDDEN REFRESH CYCLE (READ)



HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTES

TENTATIVE DATA
262,144 WORD ×4 BIT DYNAMIC RAM

DESCRIPTION

The TC514256AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514256AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

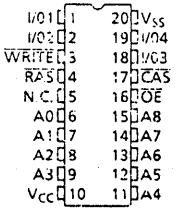
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating (TC514256AP/AJ/AZ-70)
  - 385mW MAX. Operating (TC514256AP/AJ/AZ-80)
  - 330mW MAX. Operating (TC514256AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package TC514256AP : DIP20-P-300B
  TC514256AJ : SOJ26-P-300
  TC514256AZ : ZIP20-P-400

PIN NAMES

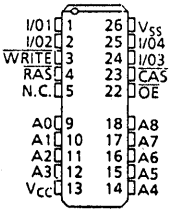
A0~A8	Address Inputs	I/O1~I/O4	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WRITE}$	Read/Write Input	N.C.	No Connection
$\overline{OE}$	Output Enable		

PIN CONNECTION (TOP VIEW)

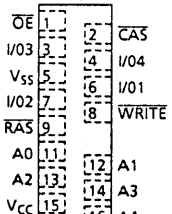
Plastic DIP



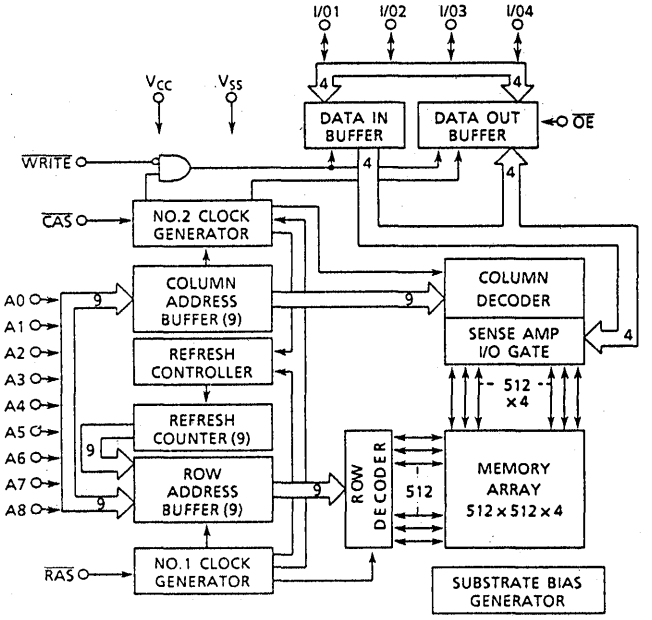
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC514256AP/AJ/AZ-80	–	70		
		TC514256AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514256AP/AJ/AZ-70	–	80	mA	3, 5
		TC514256AP/AJ/AZ-80	–	70		
		TC514256AP/AJ/AZ-10	–	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256AP/AJ/AZ-70	–	60	mA	3, 4, 5
		TC514256AP/AJ/AZ-80	–	50		
		TC514256AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256AP/AJ/AZ-70	–	80	mA	3
		TC514256AP/AJ/AZ-80	–	70		
		TC514256AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC514256AP/AJ/AZ-70		TC514256AP/AJ/AZ-80		TC514256AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	50	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	CHARACTERISTIC	TC514256AP/AJ/AZ-70		TC514256AP/AJ/AZ-80		TC514256AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	

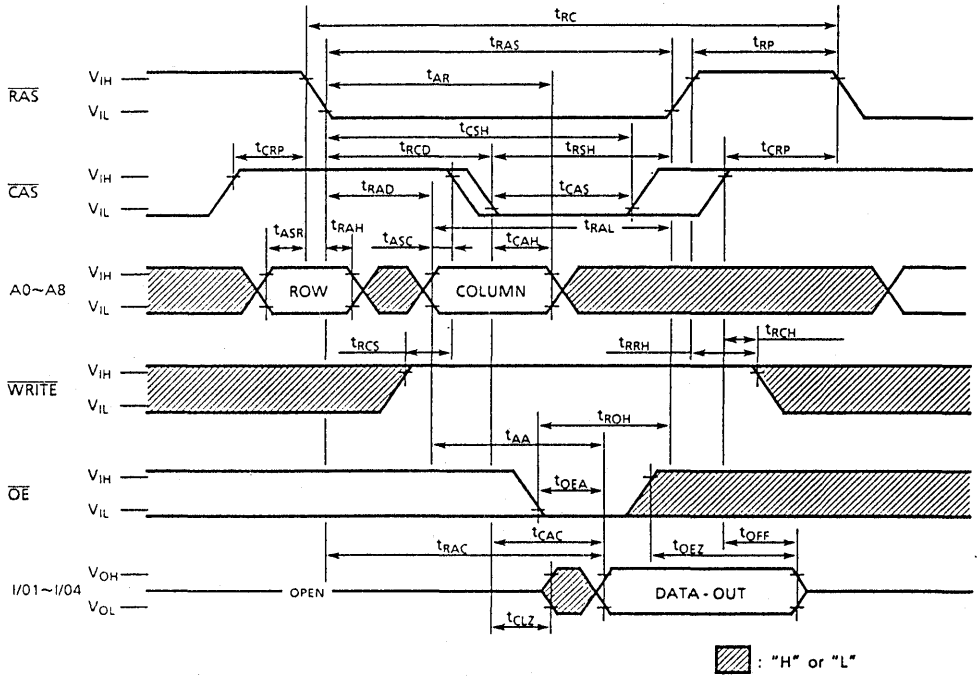
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/01~I/04)	–	7	pF

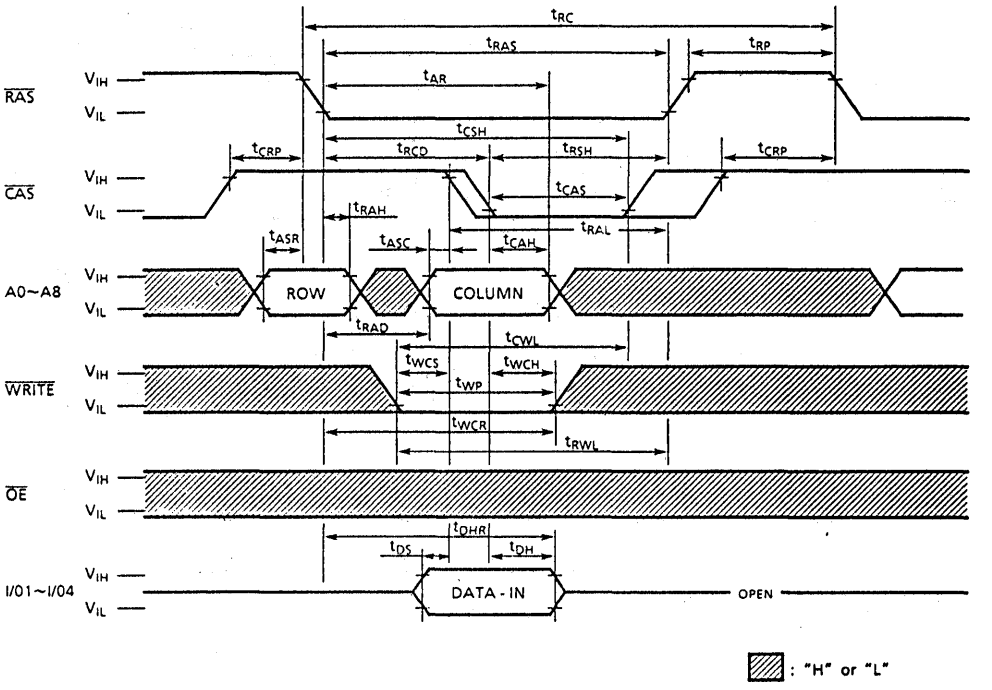
NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4}, I_{CC6} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

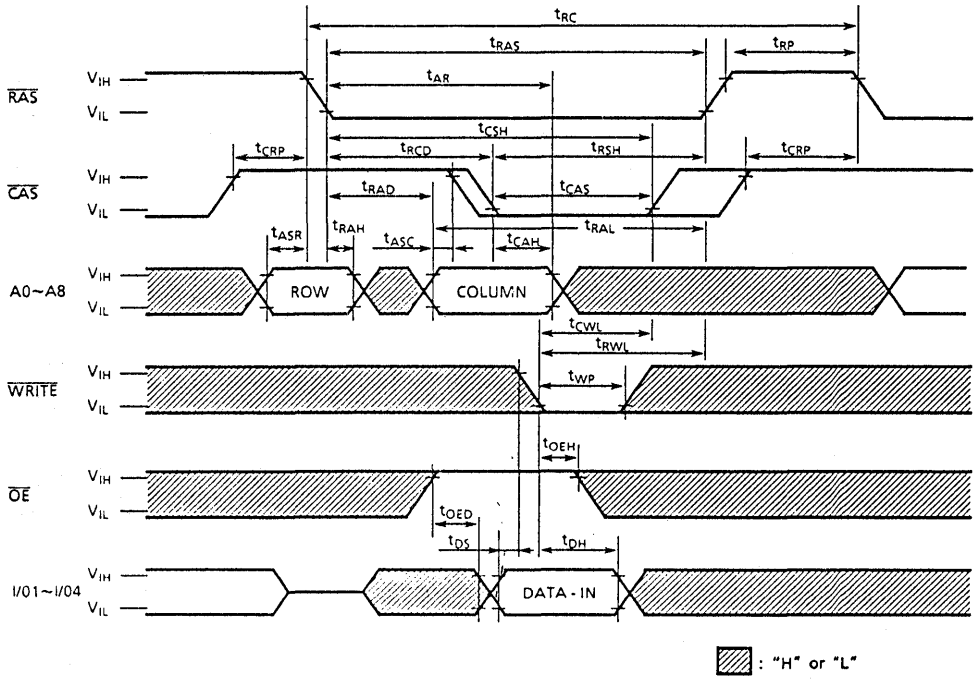
READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
OE
tOEA
tCAC
tOFF
tRAC
tOEZ
I/O1~I/O4
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

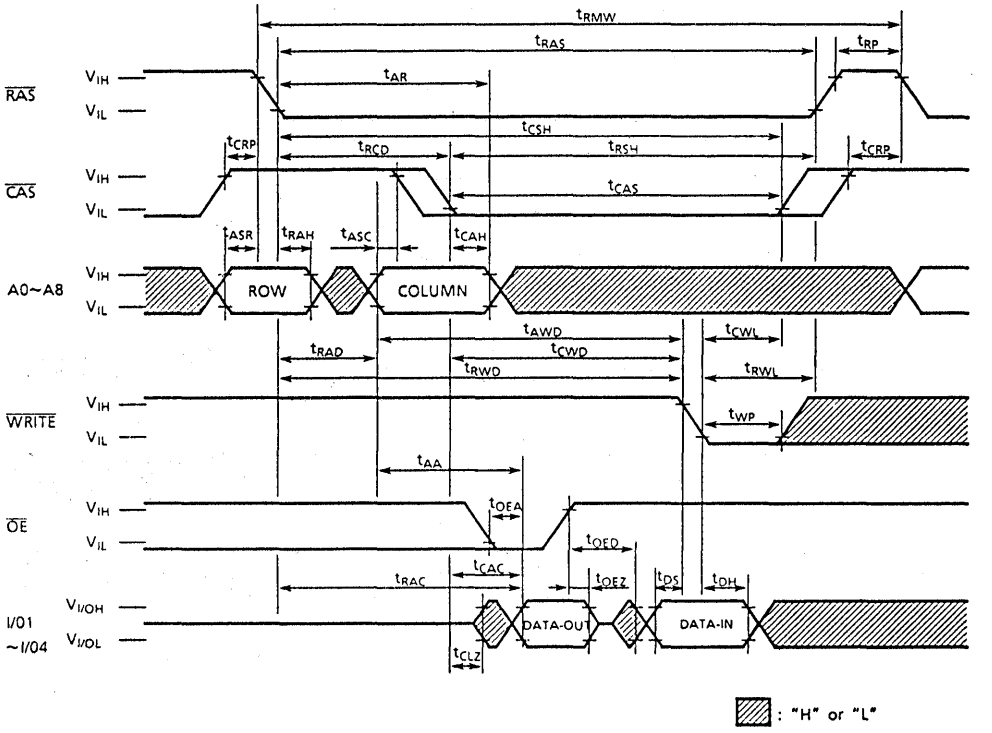
WRITE CYCLE (EARLY WRITE)



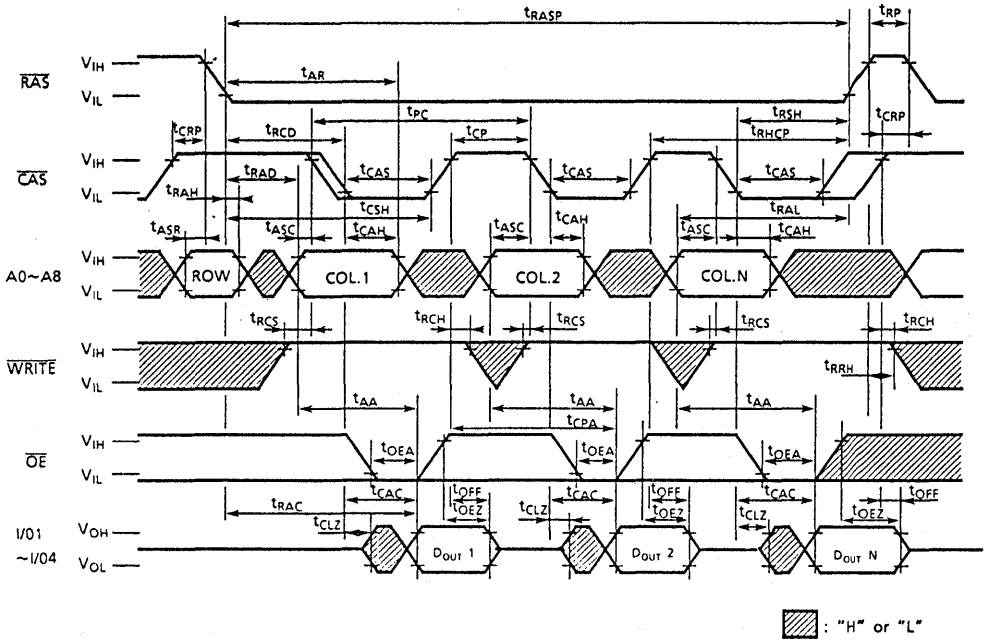
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



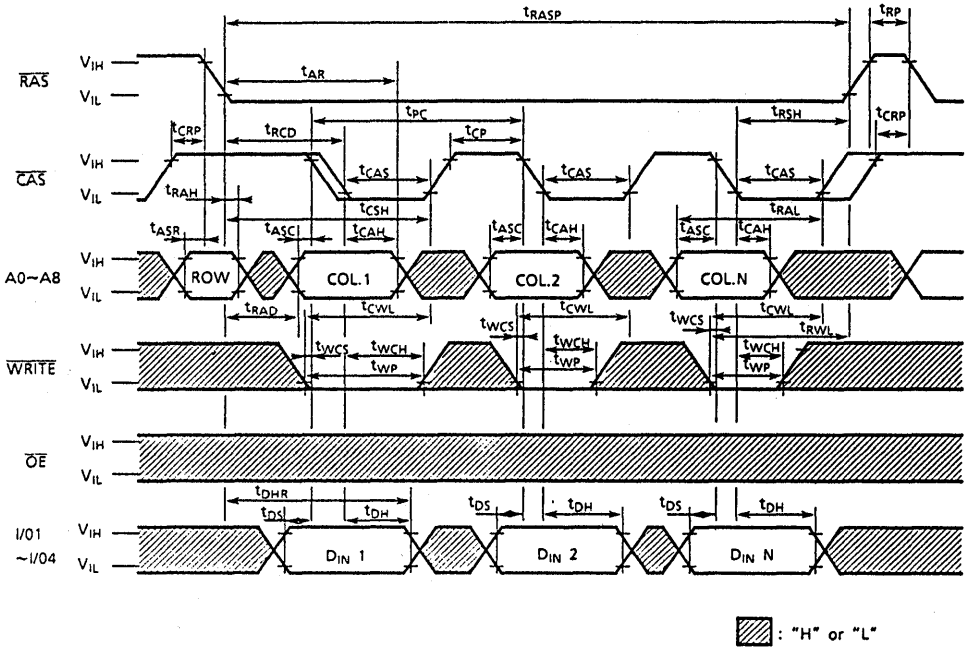
READ-MODIFY-WRITE CYCLE



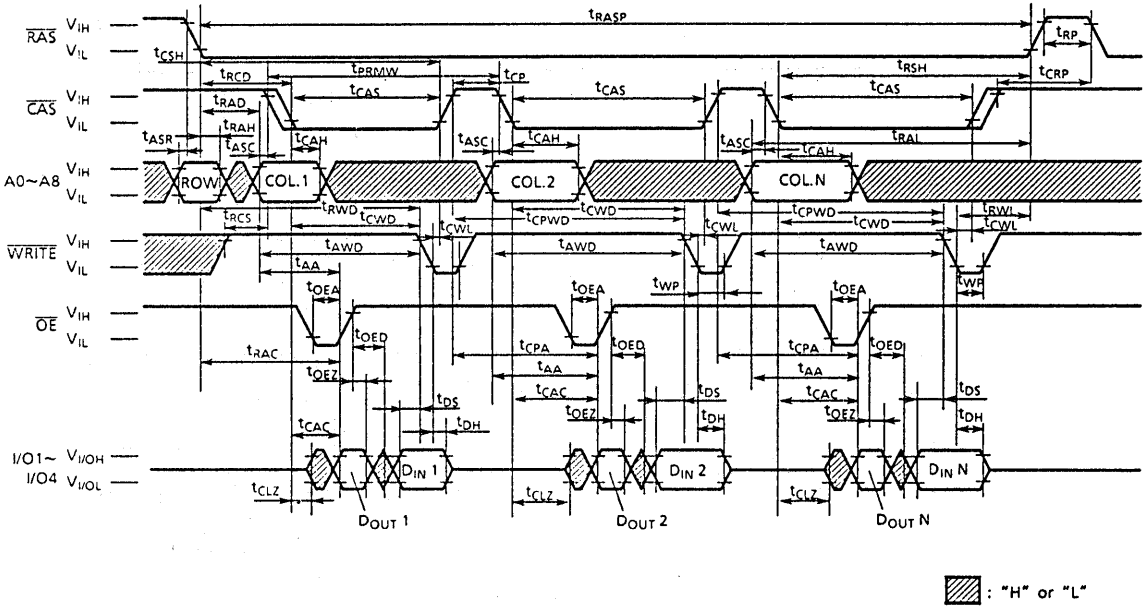
FAST PAGE MODE READ CYCLE



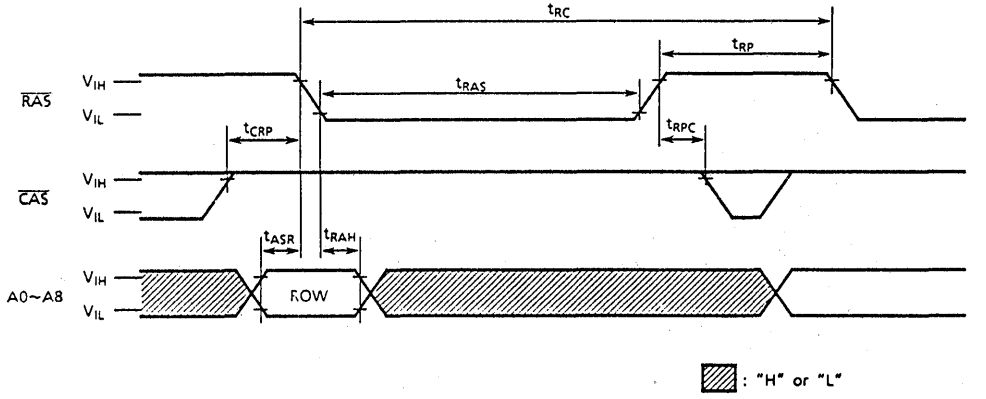
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

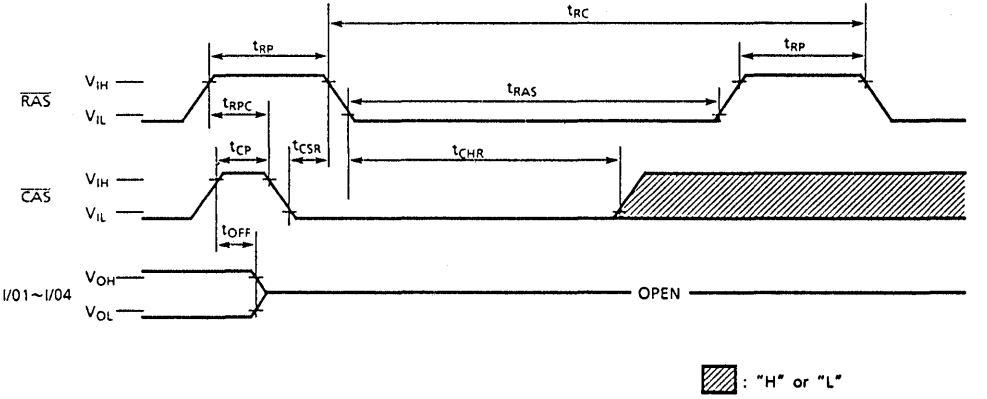


$\overline{RAS}$ ONLY REFRESH CYCLE



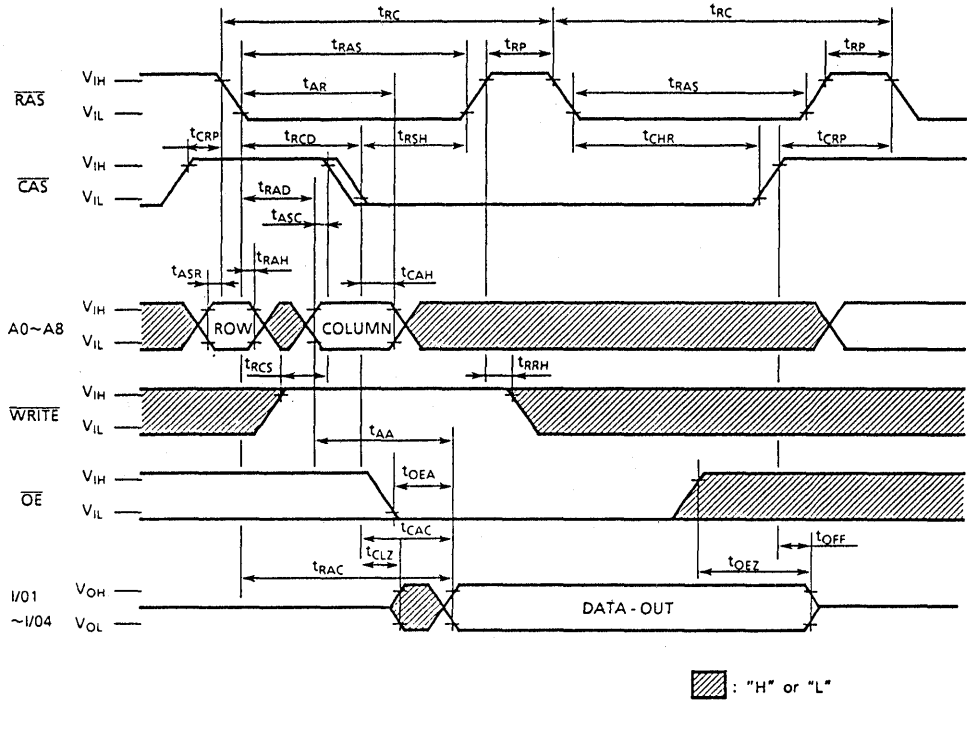
Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

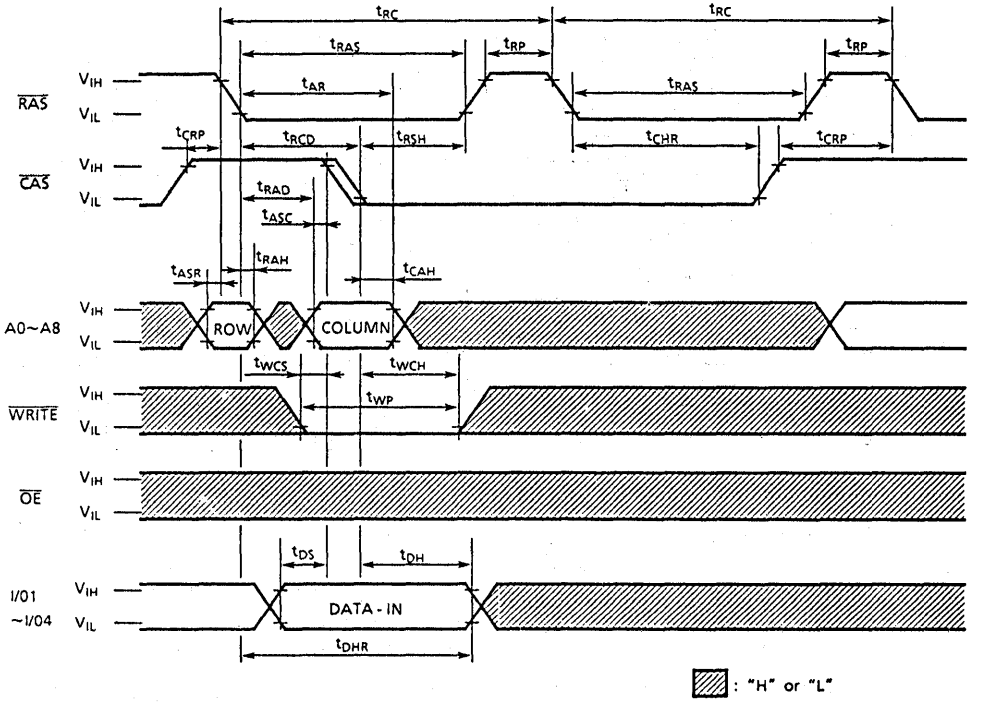


Note: $\overline{WRITE}$, $\overline{OE}$ = A0~A8 = "H" or "L"

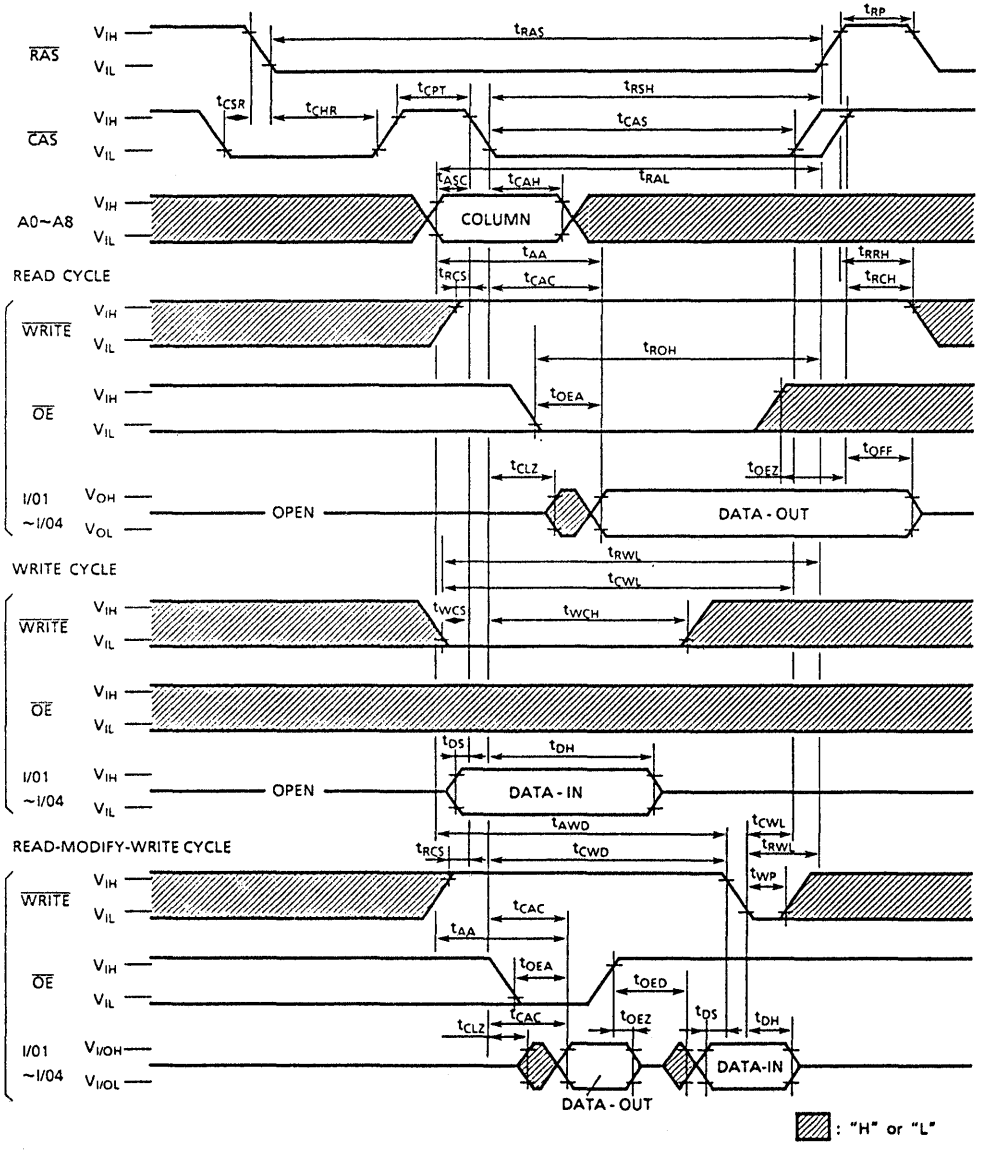
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTES

TENTATIVE DATA
262,144 WORD ×4 BIT DYNAMIC RAM

DESCRIPTION

The TC514256APL/AJL/AZL is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514256APL/AJL/AZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514256APL/AJL/AZL to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514256APL/AJL/AZL-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator

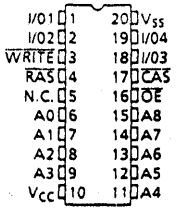
PIN NAMES

A0~A8	Address Inputs	I/O1~I/O4	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WRITE}$	Read/Write Input	N.C.	No Connection
$\overline{OE}$	Output Enable		

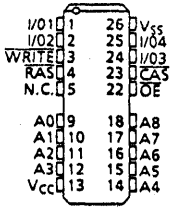
- Low Power
  - 440mW MAX. Operating (TC514256APL/AJL/AZL-70)
  - 385mW MAX. Operating (TC514256APL/AJL/AZL-80)
  - 330mW MAX. Operating (TC514256APL/AJL/AZL-10)
  - 1.1mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Fast Page Mode Capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/64ms
- Package TC514256APL : DIP20-P-300B
  TC514256AJL : SOJ26-P-300
  TC514256AZL : ZIP20-P-400

PIN CONNECTION (TOP VIEW)

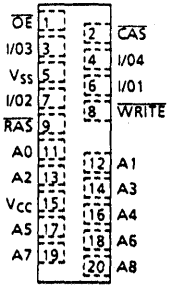
Plastic DIP



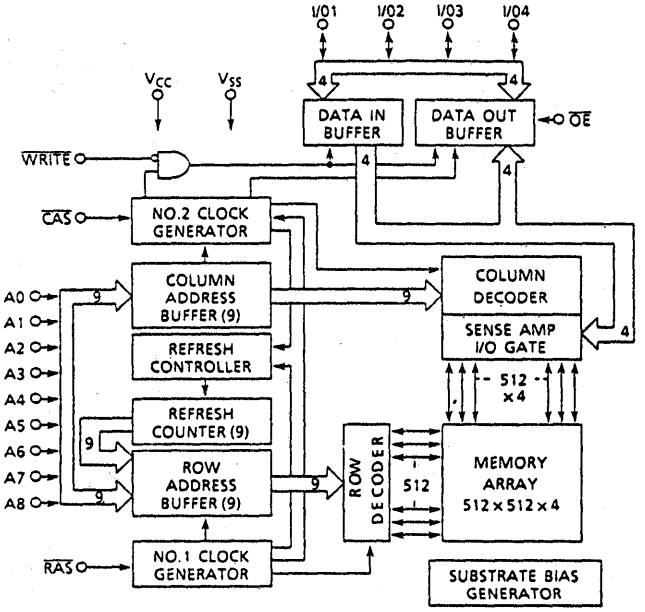
Plastic SOJ



Plastic ZIP



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514256APL/AJL/AZL-70	–	80	mA	3, 4 5
		TC514256APL/AJL/AZL-80	–	70		
		TC514256APL/AJL/AZL-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514256APL/AJL/AZL-70	–	80	mA	3, 5
		TC514256APL/AJL/AZL-80	–	70		
		TC514256APL/AJL/AZL-10	–	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514256APL/AJL/AZL-70	–	60	mA	3, 4 5
		TC514256APL/AJL/AZL-80	–	50		
		TC514256APL/AJL/AZL-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	200	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514256APL/AJL/AZL-70	–	80	mA	3
		TC514256APL/AJL/AZL-80	–	70		
		TC514256APL/AJL/AZL-10	–	60		
I_{CC7}	BATTERY BACK UP CURRENT Avarage Power Supply Current, BATTERY BACK UP MODE ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WRITE}$ = V_{CC} – 0.2V or 0.2V, A0~8 = V_{CC} – 0.2V or 0.2V, I/O1~4 = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125μs, t_{RAS} = t_{RAS} MIN. ~1μs)		–	300	μA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 7, 8, 9)

SYMBOL	CHARACTERISTIC	TC514256APL/AJL/AZL-70		TC514256APL/AJL/AZL-80		TC514256APL/AJL/AZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	100	-	120	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	10,15
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	10,15
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	10,16
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	0	-	0	-	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	40	-	50	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	CHARACTERISTIC	TC514256APL/AJL/AZL-70		TC514256APL/AJL/AZL-80		TC514256APL/AJL/AZL-10		UNIT	NOTE
		MIN	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	13
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	64	–	64	–	64	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	60	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	100	–	110	–	135	–	ns	14
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	

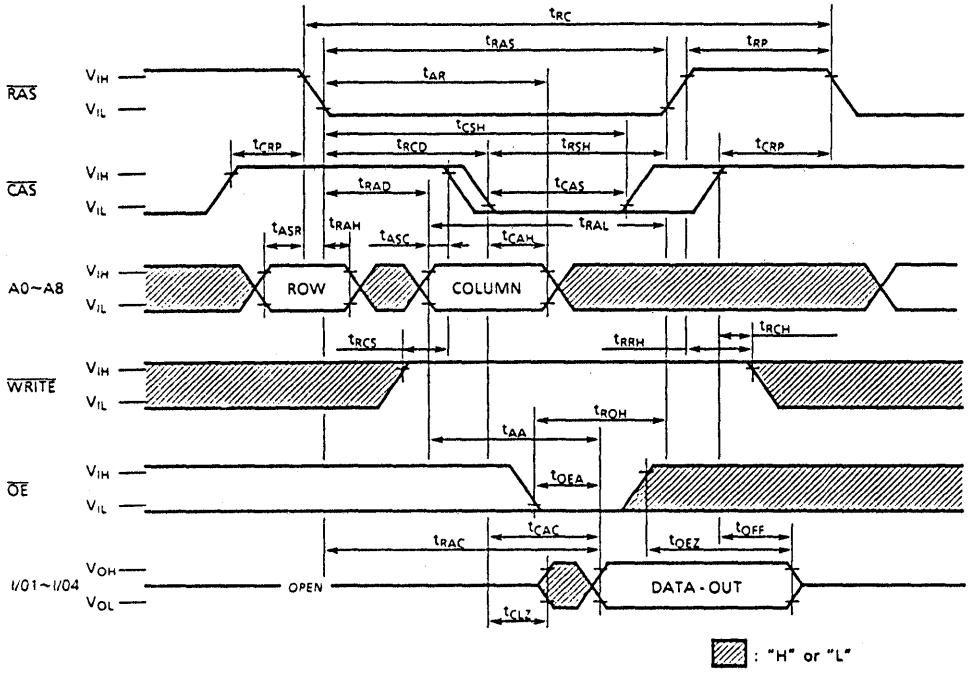
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	–	7	pF

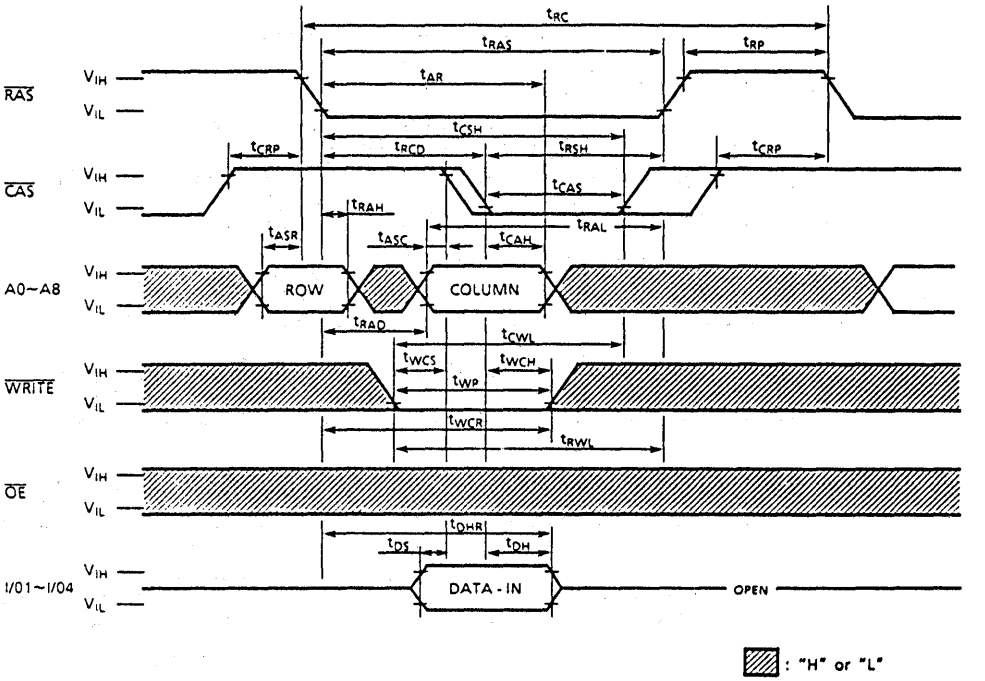
NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4} depend on cycle rate.
4. I_{CC1}, I_{CC4}, I_{CC6} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
8. AC measurements assume $t_T = 5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

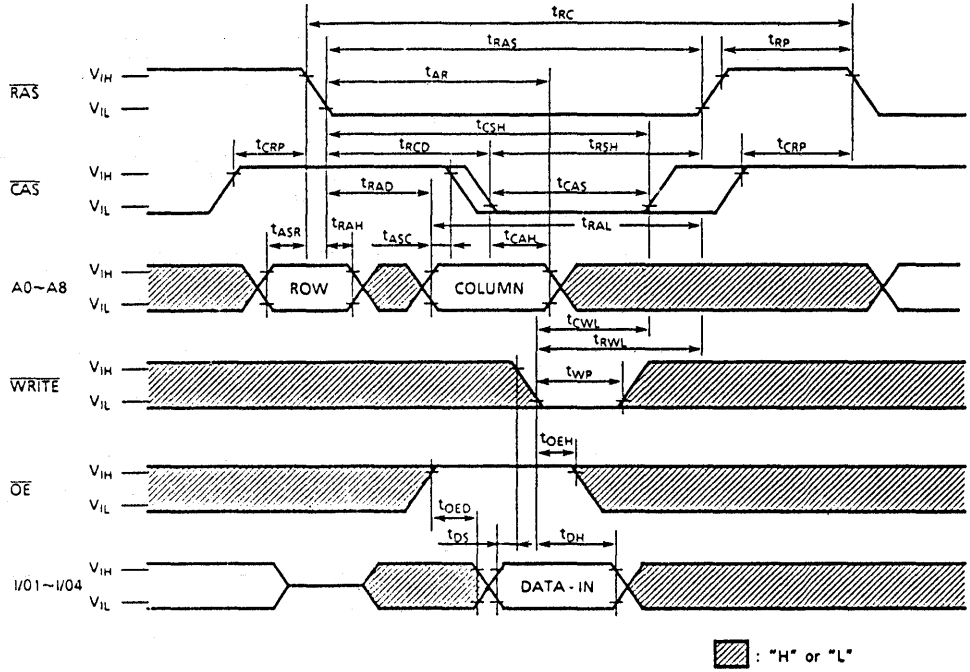
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A8
VIH
VIL
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
VIH
VIL
tRQH
tAA
OE
VIH
VIL
tOEA
tRAC
tCAC
tOEZ
tOFF
I/O1~I/04
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

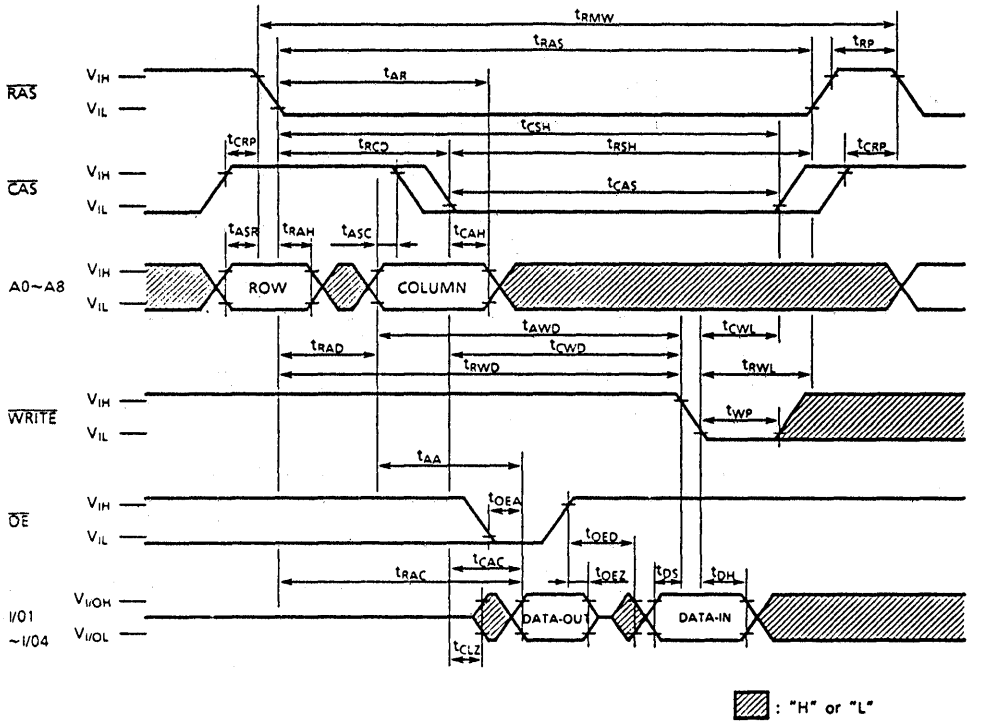
WRITE CYCLE (EARLY WRITE)



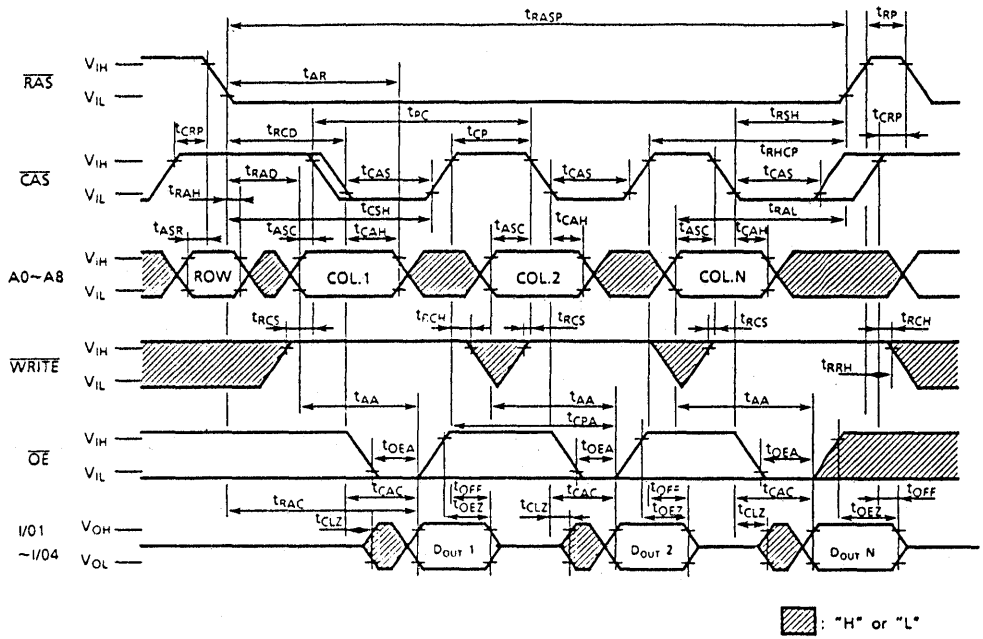
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



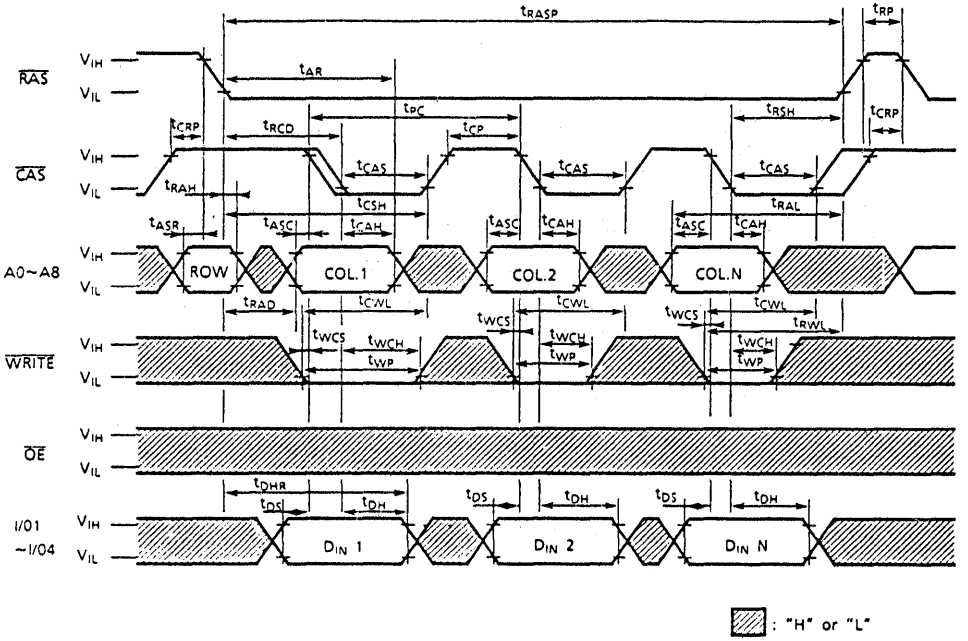
READ-MODIFY-WRITE CYCLE



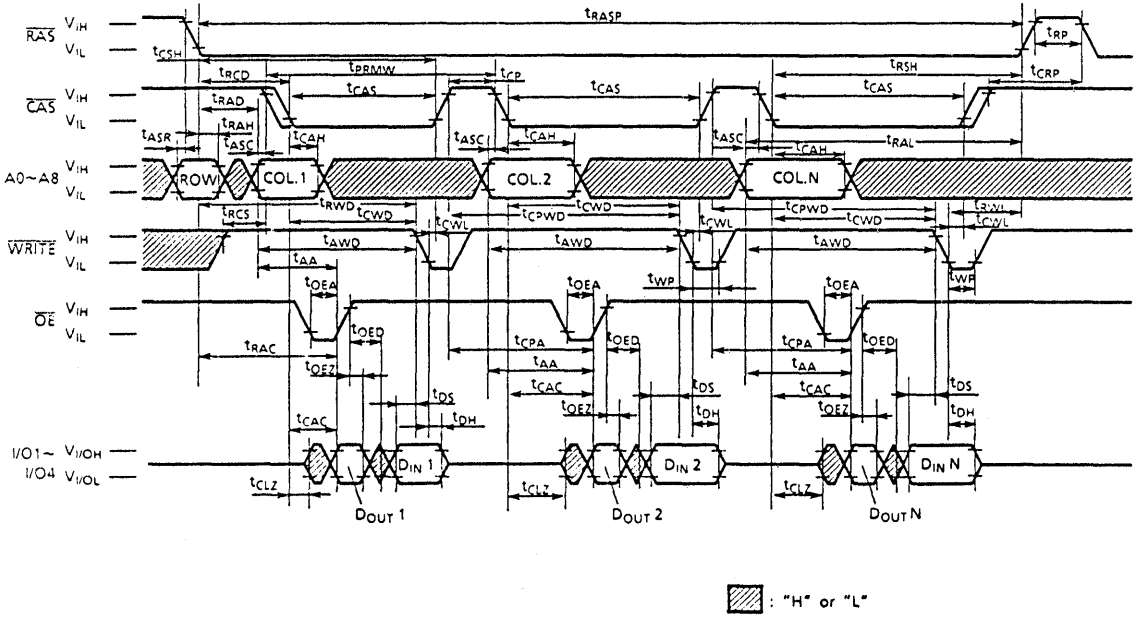
FAST PAGE MODE READ CYCLE



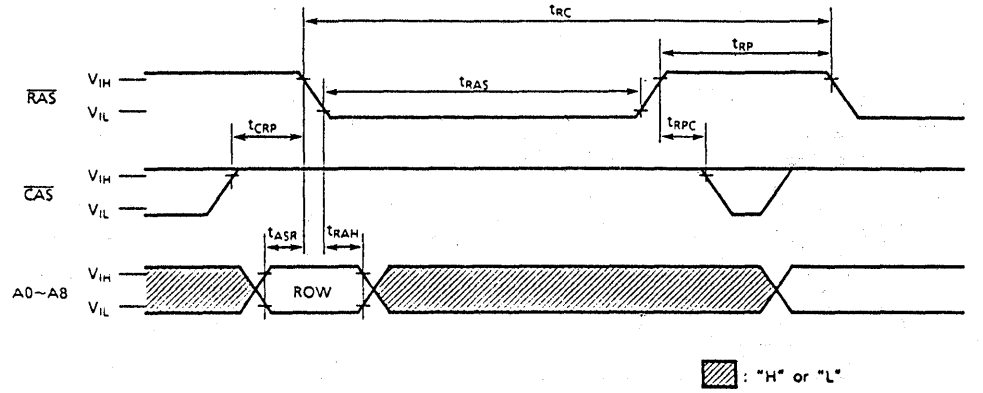
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

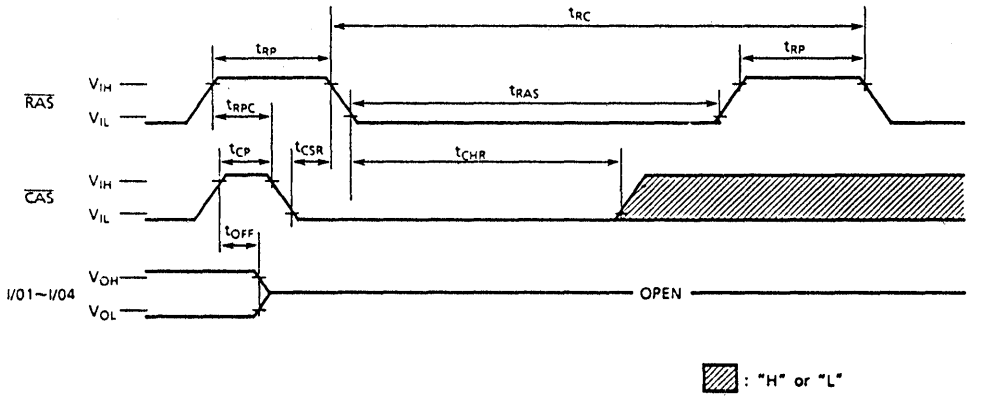


$\overline{RAS}$ ONLY REFRESH CYCLE



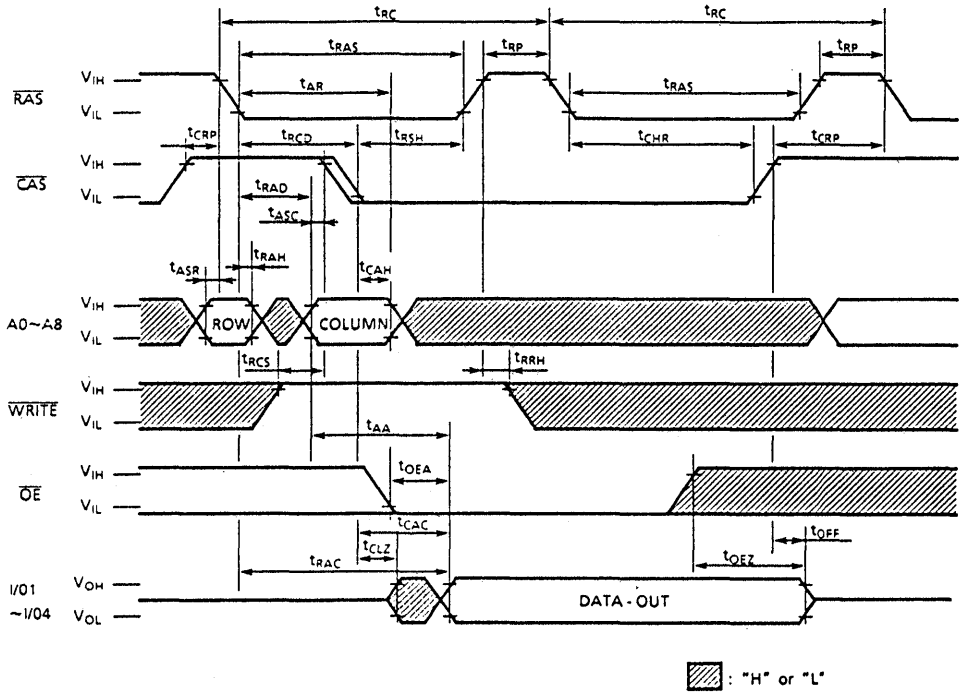
Note: WRITE, $\overline{OE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

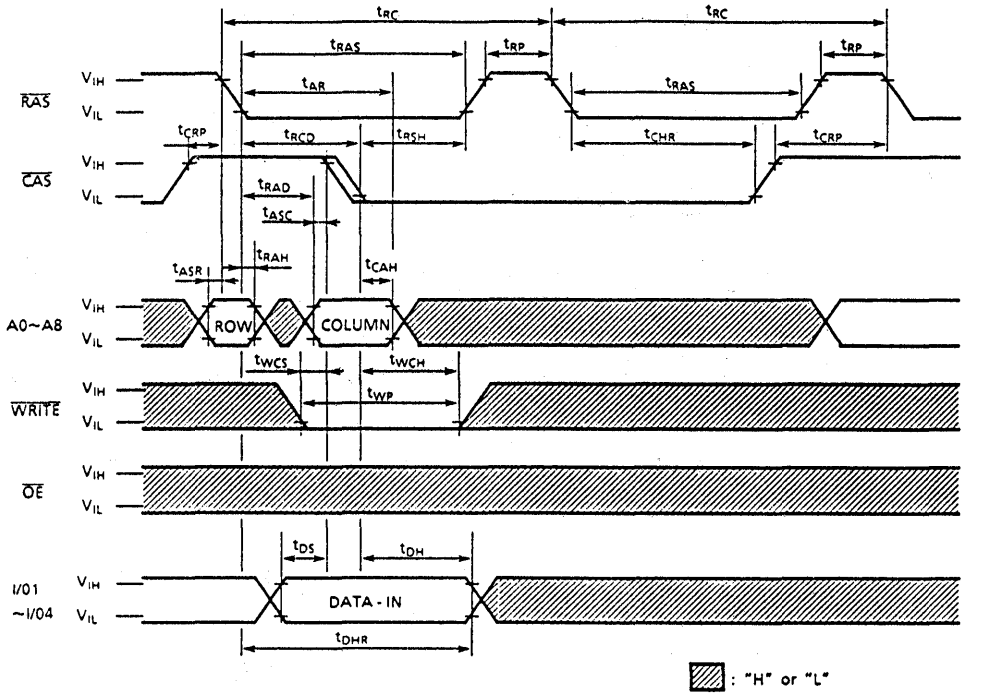


Note: WRITE, $\overline{OE}$ = A0~A8 = "H" or "L"

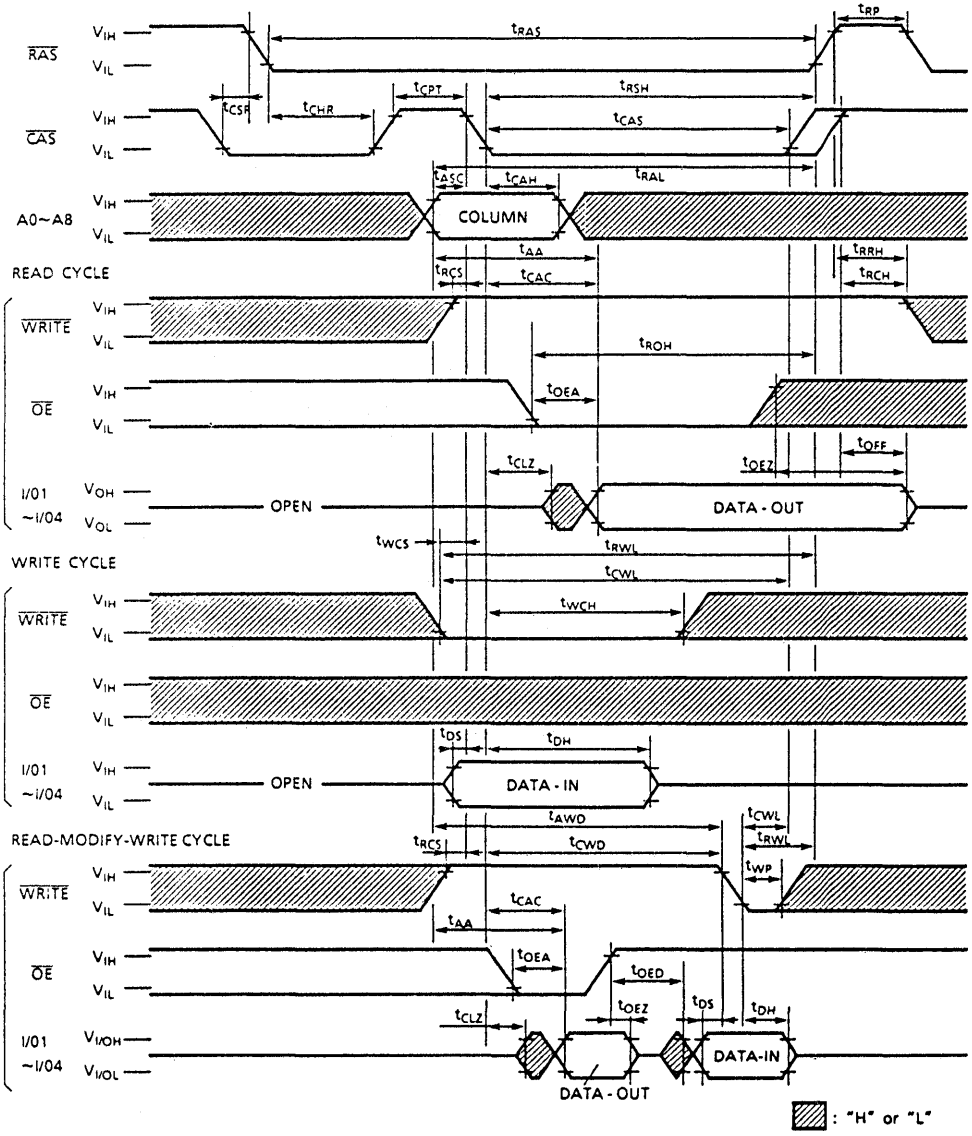
HIDDEN REFRESH CYCLE (READ)



HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTES

262,144 WORD ×4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514258BP/BJ/BZ/BFT is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514258BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514258BP/BJ/BZ/BFT to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

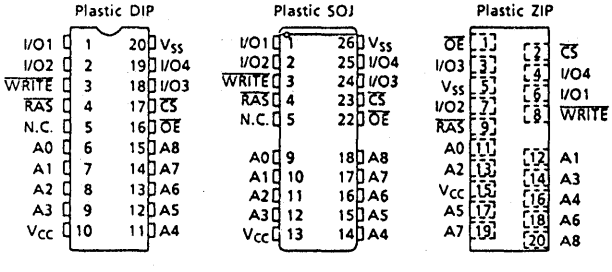
FEATURES

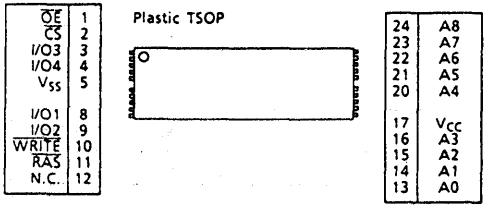
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514258BP/BJ/BZ/BFT-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{SC}	Static column Mode Cycle Time	35ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package
  TC514258BP : DIP20-P-300B
  TC514258BJ : SOJ26-P-300
  TC514258BZ : ZIP20-P-400
  TC514258BFT : TSOP24-P-0616

PIN CONNECTION

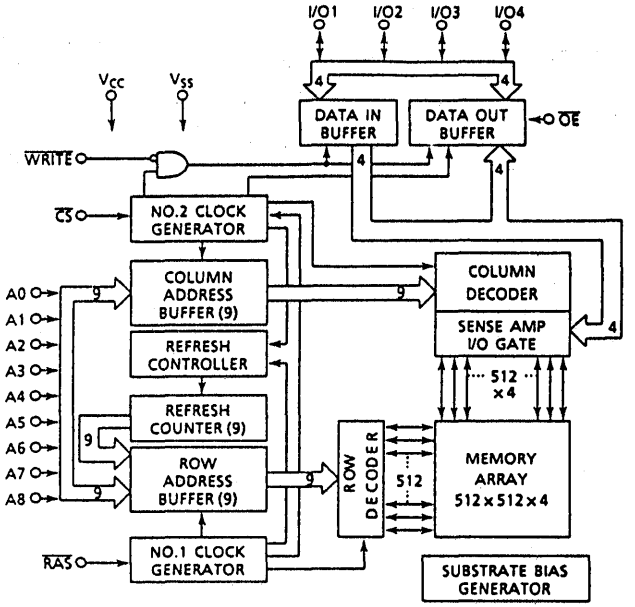




PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WRITE}$	Read/Write Input
$\overline{OE}$	Output Enable
I/O1~I/O4	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514258BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514258BP/BJ/BZ/BFT-60	–	90	mA	3, 5
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS}$ = $\overline{CS}$ = V_{IL}, Address Cycling: t_{SC} = t_{SC} MIN.)	TC514258BP/BJ/BZ/BFT-60	–	70	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514258BP/BJ/BZ/BFT-60	–	90	mA	3, 5
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(VCC = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514258BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{SC}	Static Column Mode Cycle Time	35	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	90	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9,14
t_{CAC}	Access Time from $\overline{CS}$	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{ALW}	Access Time from Last Write	-	55	ns	9,16
t_{CLZ}	$\overline{CS}$ to output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Addres	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	20	ns	
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	60	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	20	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	60	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	20	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	20	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	50	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	85	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	ns	17
t_{LWAD}	Last Write to Column Address Delay Time	20	25	ns	16
t_{AHLW}	Last Write to Column Address Delay Time	55	-	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	-	ns	

SYMBOL	PARAMETER	TC514258BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	-	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time (Output Data Disable)	10	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	
t_{WP}	Write Command Pulse Width	10	-	ns	
t_{WI}	Write Command Inactive Time	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	-	ns	
t_{DS}	Data-In Set-Up Time	0	-	ns	12
t_{DH}	Data-In Hold Time	15	-	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{REF}	Refresh Period	-	8	ms	
t_{WCS}	Write Command Set-UP Time (Output Data Disable)	0	-	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE Cycle)	90	-	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	-	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time($\overline{CS}$ before $\overline{RAS}$)	5	-	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	-	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	ns	

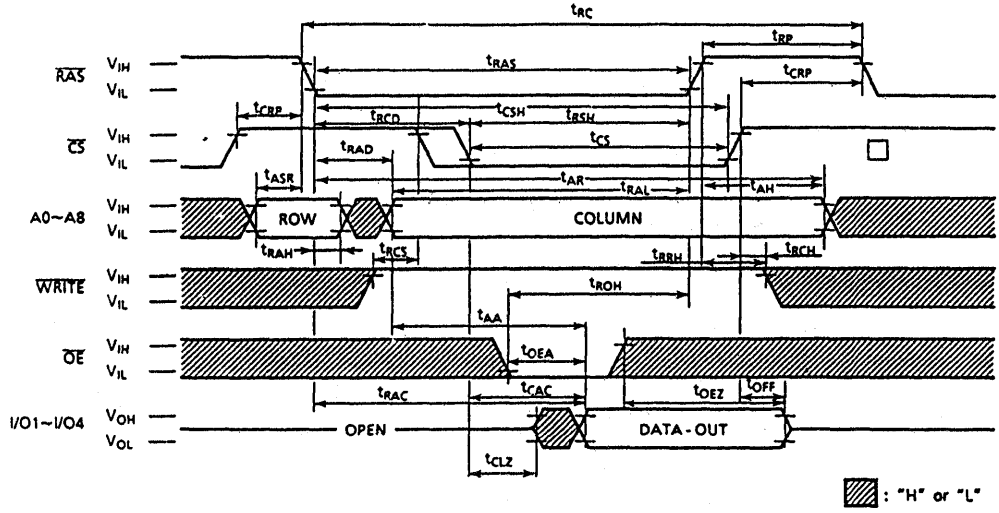
CAPACITANCE (VCC = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	-	7	pF

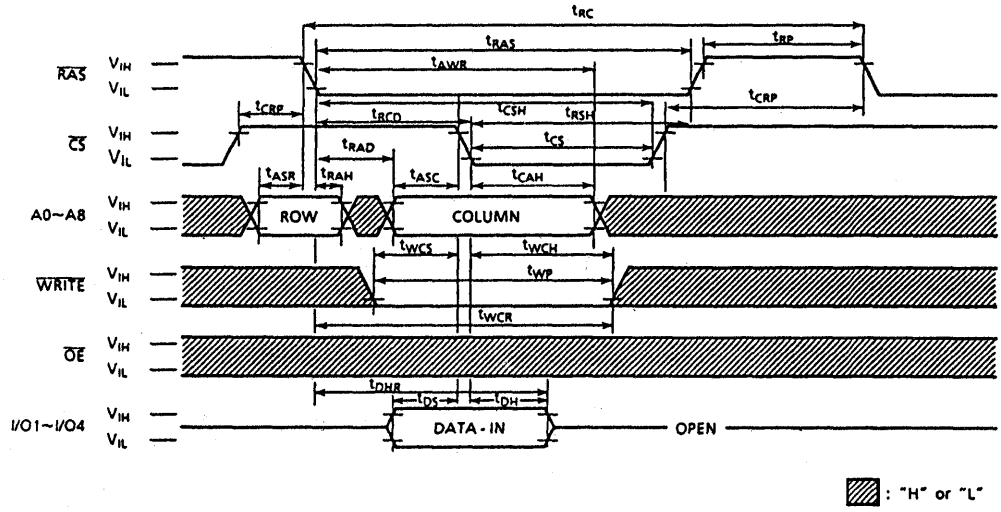
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has risen up.

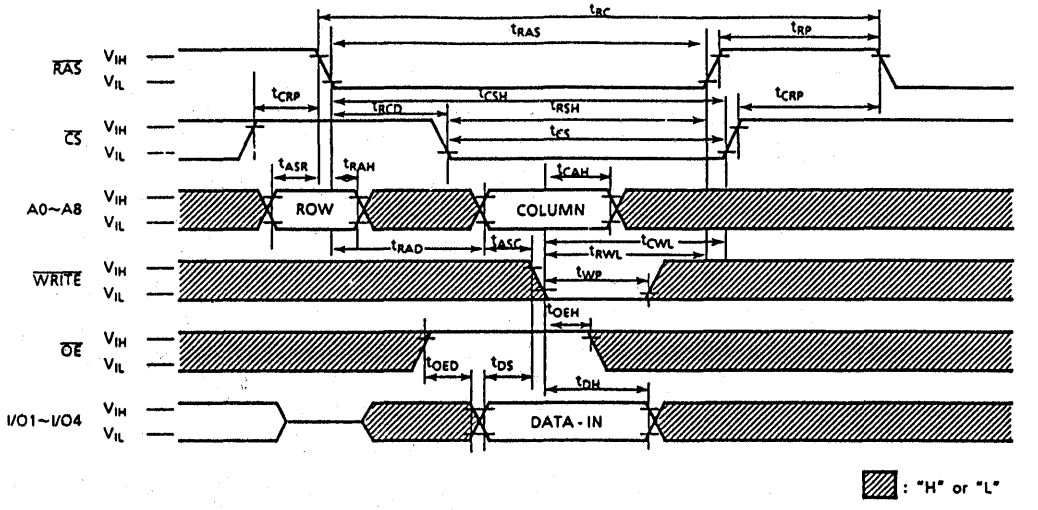
READ CYCLE



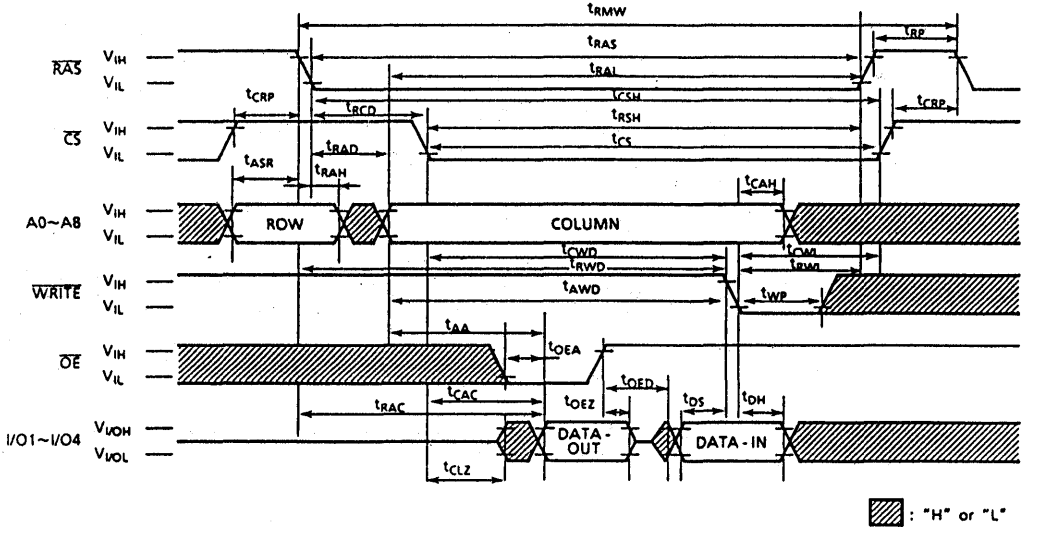
WRITE CYCLE (EARLY WRITE)



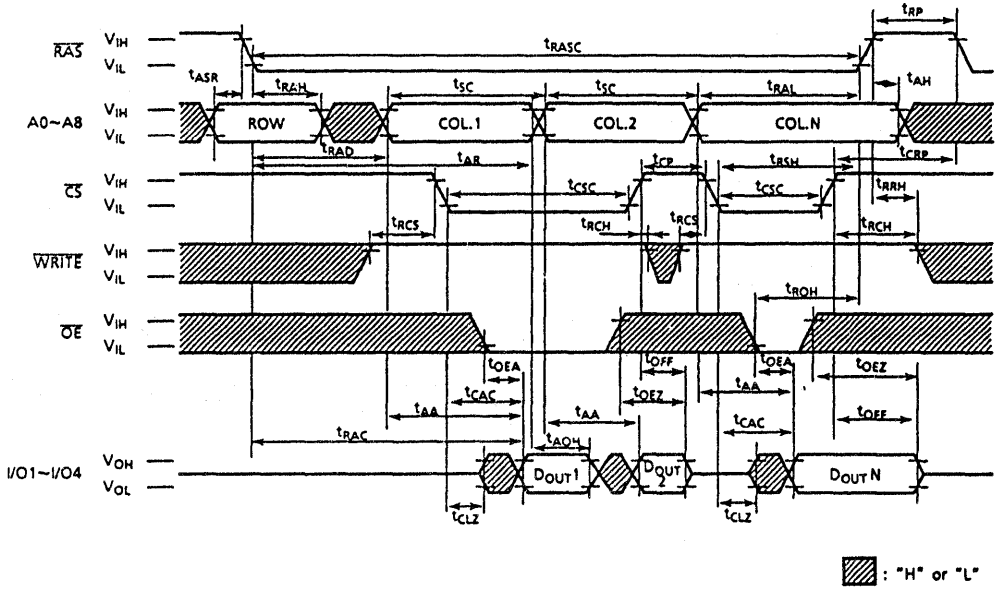
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



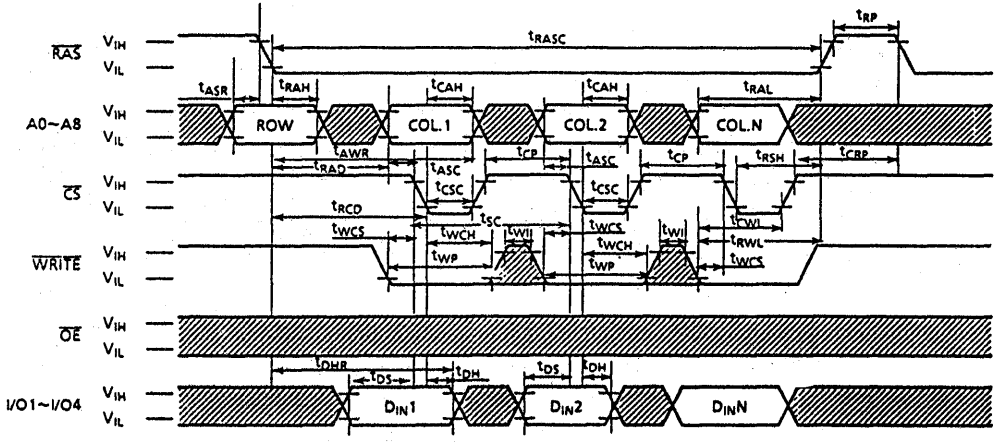
READ - MODIFY - WRITE CYCLE



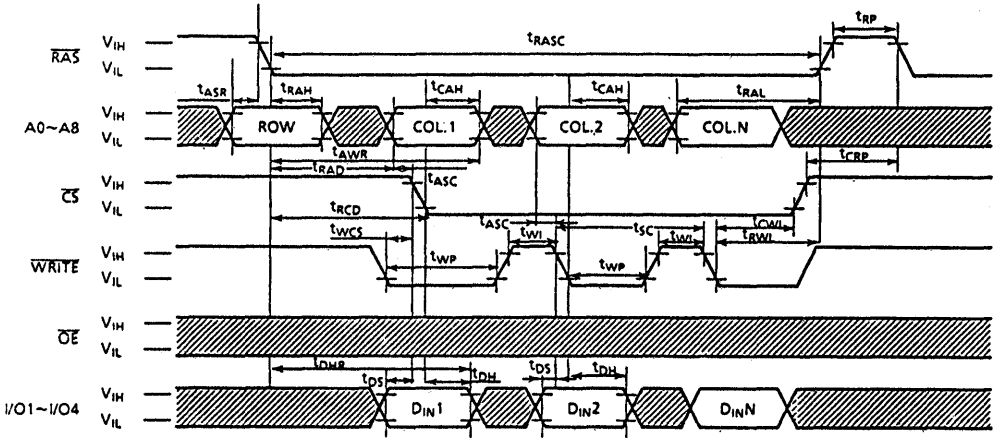
STATIC COLUMN MODE READ CYCLE



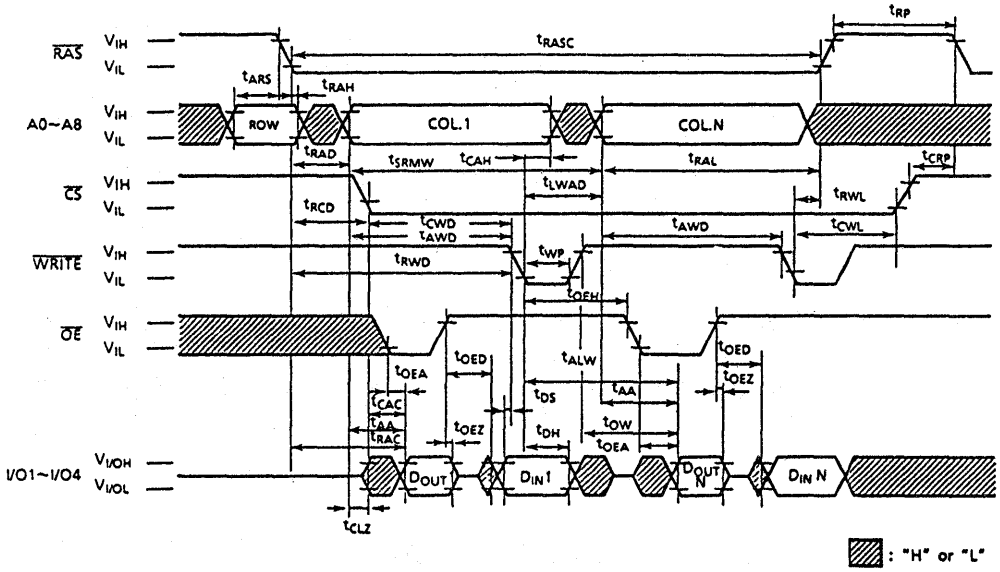
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



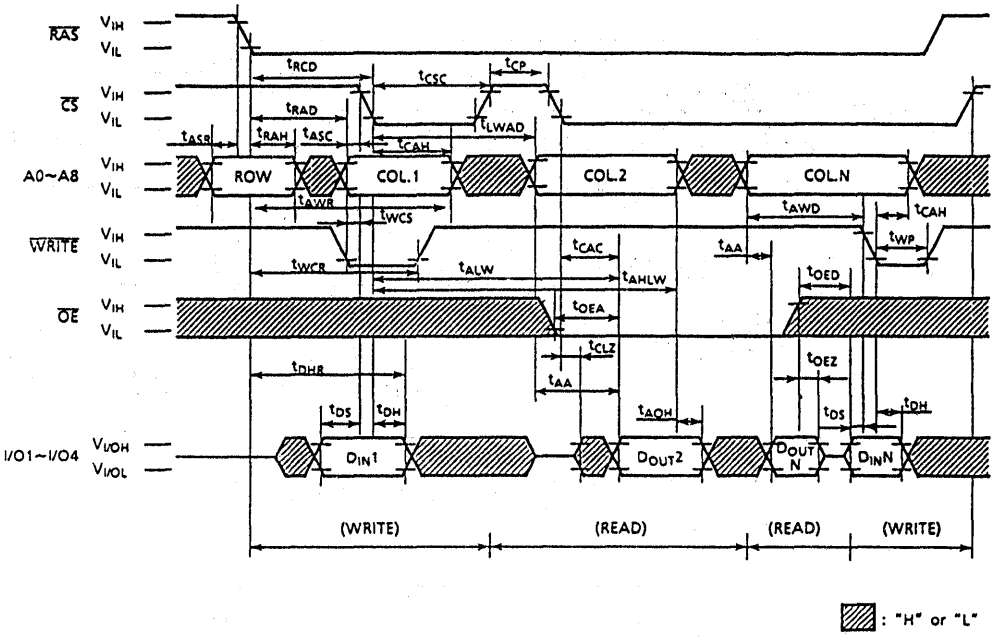
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



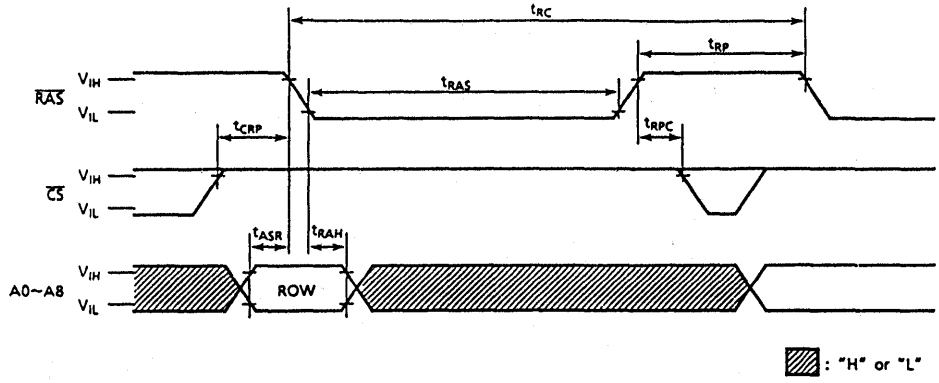
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

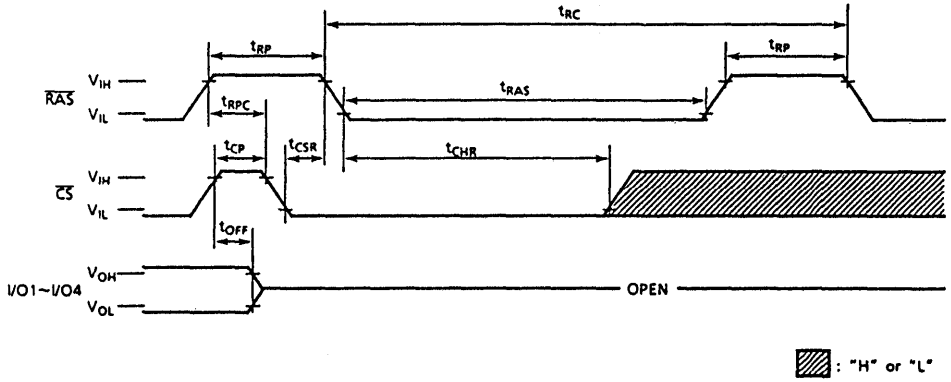


$\overline{RAS}$ ONLY REFRESH CYCLE



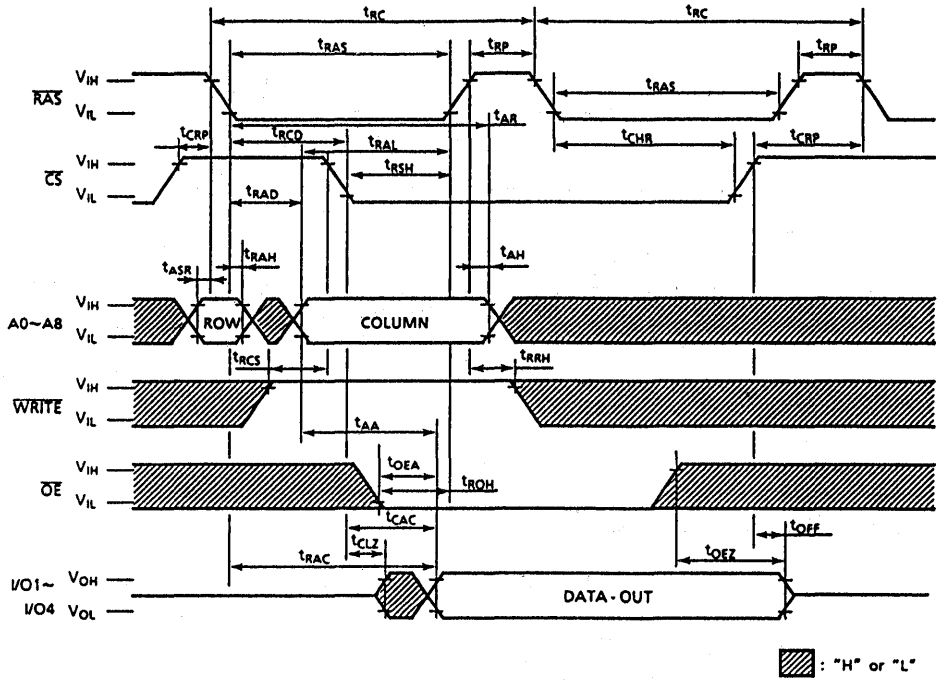
Note: WRITE, $\overline{OE}$="H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

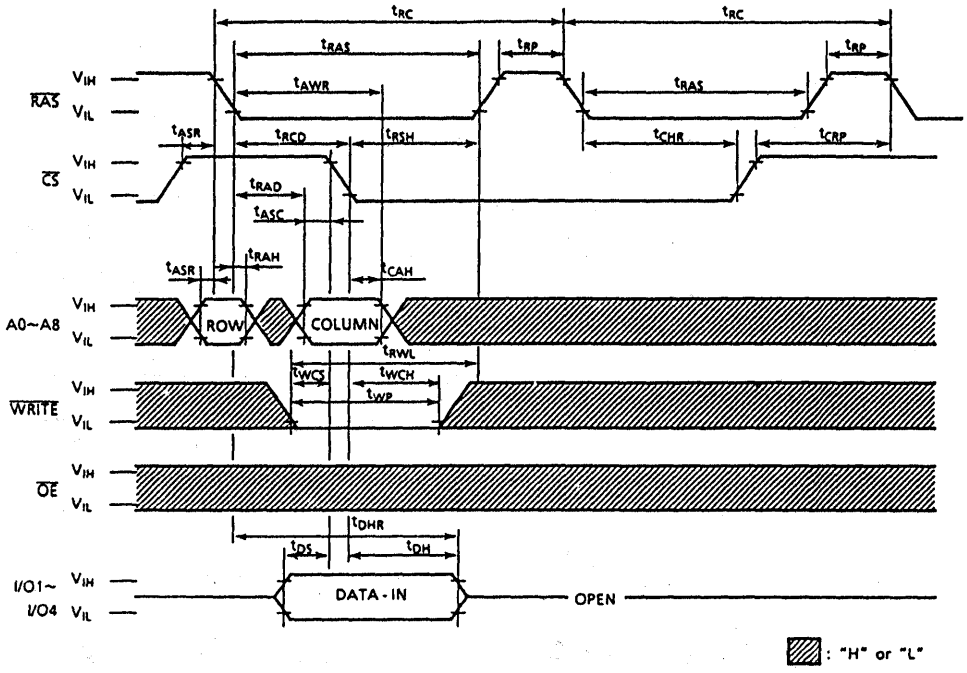


Note: WRITE, $\overline{OE}$, A0~A8="H" or "L"

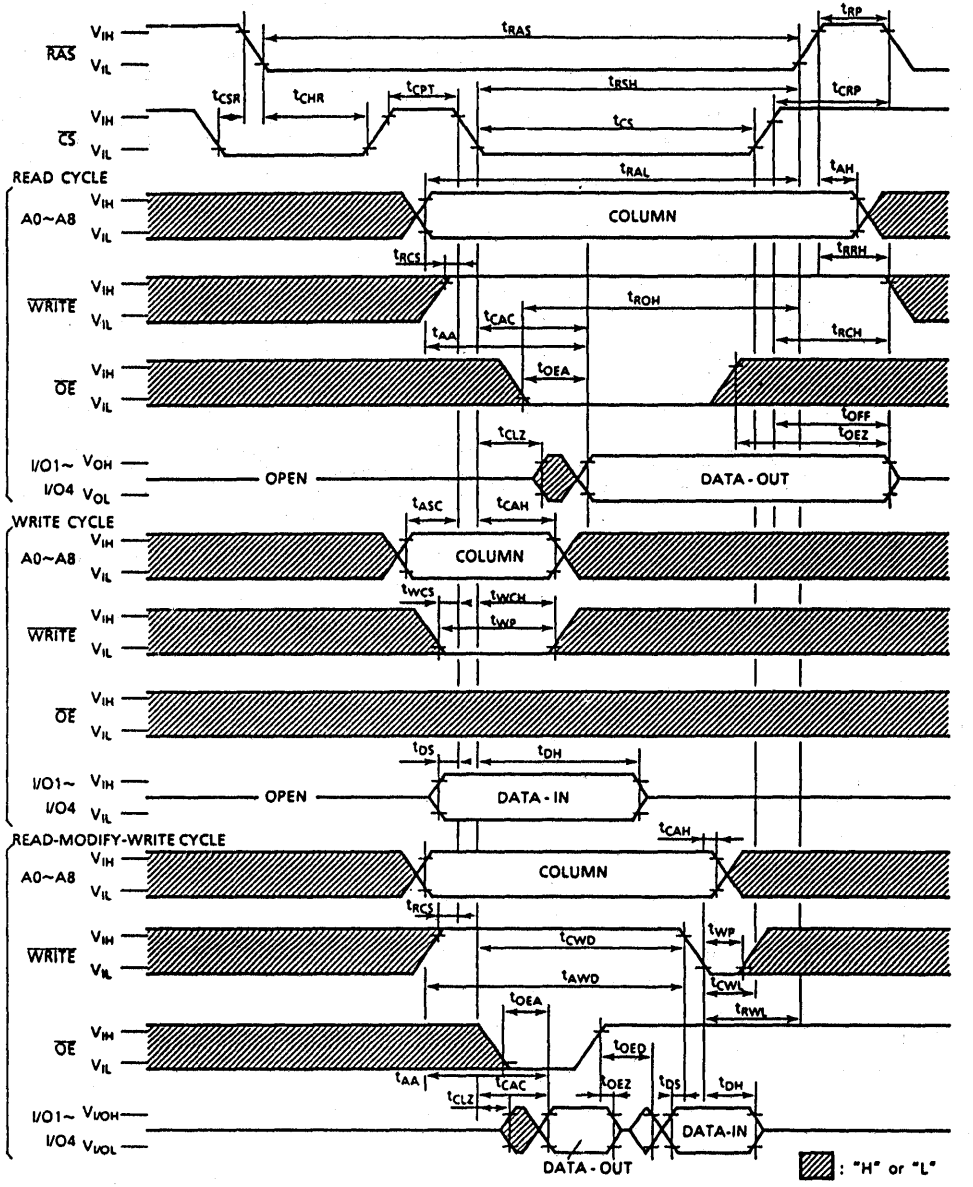
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TENTATIVE DATA
262,144 WORD ×4 BIT DYNAMIC RAM

DESCRIPTION

The TC514258AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514258AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514258AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

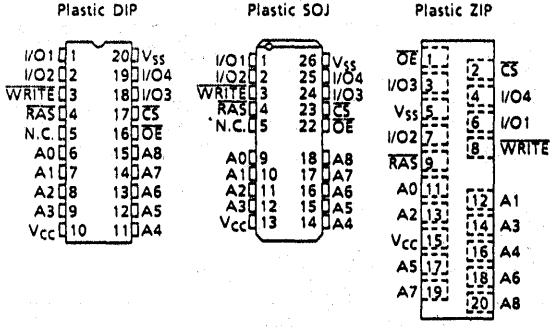
		TC514258AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CS}$ Access Time	25ns	25ns	30ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{SC}	Static column Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating (TC514258AP/AJ/AZ-70)
  - 385mW MAX. Operating (TC514258AP/AJ/AZ-80)
  - 330mW MAX. Operating (TC514258AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, and Static Column Mode capability
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- Package TC514258AP : DIP20-P-300B
  TC514258AJ : SOJ26-P-300
  TC514258AZ : ZIP20-P-400

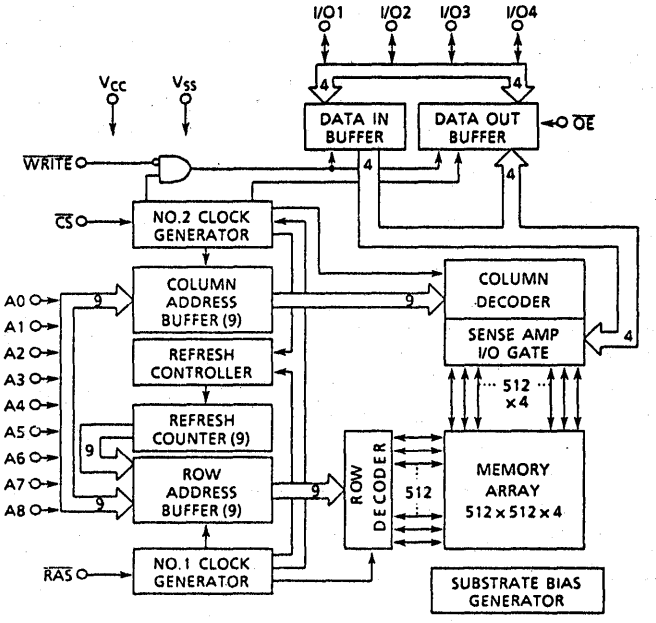
PIN NAMES

A0~A8	Address Inputs	I/O1~I/O4	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CS}$	Chip Select	V_{SS}	Ground
$\overline{WRITE}$	Read/Write Input	N.C.	No Connection
$\overline{OE}$	Output Enable		

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (VCC = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514258AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC514258AP/AJ/AZ-80	–	70		
		TC514258AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514258AP/AJ/AZ-70	–	80	mA	3, 5
		TC514258AP/AJ/AZ-80	–	70		
		TC514258AP/AJ/AZ-10	–	60		
I_{CC4}	STATIC COLUMN MODE CURRENT Average Power Supply Current, STATIC COLUMN Mode ($\overline{RAS} = \overline{CS} = V_{IL}$, Address Cycling: $t_{SC} = t_{SC}$ MIN.)	TC514258AP/AJ/AZ-70	–	60	mA	3, 4
		TC514258AP/AJ/AZ-80	–	50		
		TC514258AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514258AP/AJ/AZ-70	–	80	mA	3
		TC514258AP/AJ/AZ-80	–	70		
		TC514258AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(VCC = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC514258AP/AJ/AZ-70		TC514258AP/AJ/AZ-80		TC514258AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	-	205	-	245	-	ns	
t_{SC}	Static Column Mode Cycle Time	40	-	45	-	55	-	ns	
t_{SRMW}	Static Column Mode Read-Modify-Write Cycle Time	100	-	110	-	135	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	9,14
t_{CAC}	Access Time from $\overline{CS}$	-	25	-	25	-	30	ns	9,14
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	9,15
t_{ALW}	Access Time from Last Write	-	65	-	75	-	95	ns	9,16
t_{CLZ}	$\overline{CS}$ to output in Low-Z	0	-	0	-	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_{AOH}	Output Data Hold Time from Column Address	5	-	5	-	5	-	ns	
t_{OW}	Output Data Enable Time from $\overline{WRITE}$	-	25	-	25	-	30	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASC}	$\overline{RAS}$ Pulse Width (Static Column Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{CS}$ to $\overline{RAS}$ Hold Time	25	-	25	-	30	-	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CS}	$\overline{CS}$ Pulse Width	25	10,000	25	10,000	30	10,000	ns	
t_{CSC}	$\overline{CS}$ Pulse Width (Static Column Mode)	25	100,000	25	100,000	30	100,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CS}$ Delay Time	20	45	20	55	25	70	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AWR}	Column Address Hold Time referenced to $\overline{RAS}$ (WRITE CYCLE)	55	-	60	-	75	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$ (READ CYCLE)	80	-	90	-	115	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{AH}	Column Address Hold Time referenced to $\overline{RAS}$ Rise	5	-	5	-	10	-	ns	17

SYMBOL	CHARACTERISTIC	TC514258AP/AJ/AZ-70		TC514258AP/AJ/AZ-80		TC514258AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{LWAD}	Last Write to Column Address Delay Time	20	30	20	35	25	45	ns	16
t_{AHLW}	Last Write to Column Address Hold Time	65	–	75	–	95	–	ns	
t_{RCS}	Read Command Set-up Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time referenced to $\overline{CS}$	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time (Output Data Disable)	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{WI}	Write Command Inactive Time	10	–	10	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data-In Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time (Output Data Disable)	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	55	–	55	–	65	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time (READ-MODIFY-WRITE CYCLE)	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CS}$ Set-Up Time($\overline{CS}$ before $\overline{RAS}$)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CS}$ Hold Time($\overline{CS}$ before $\overline{RAS}$)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CS}$ Precharge Time ($\overline{CS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output Buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	

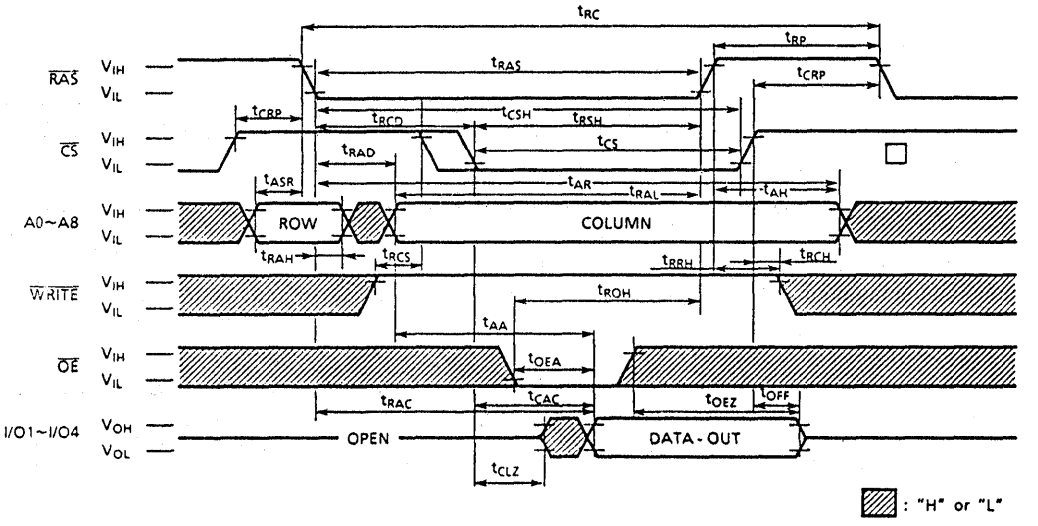
CAPACITANCE (VCC = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WRITE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O4)	-	7	pF

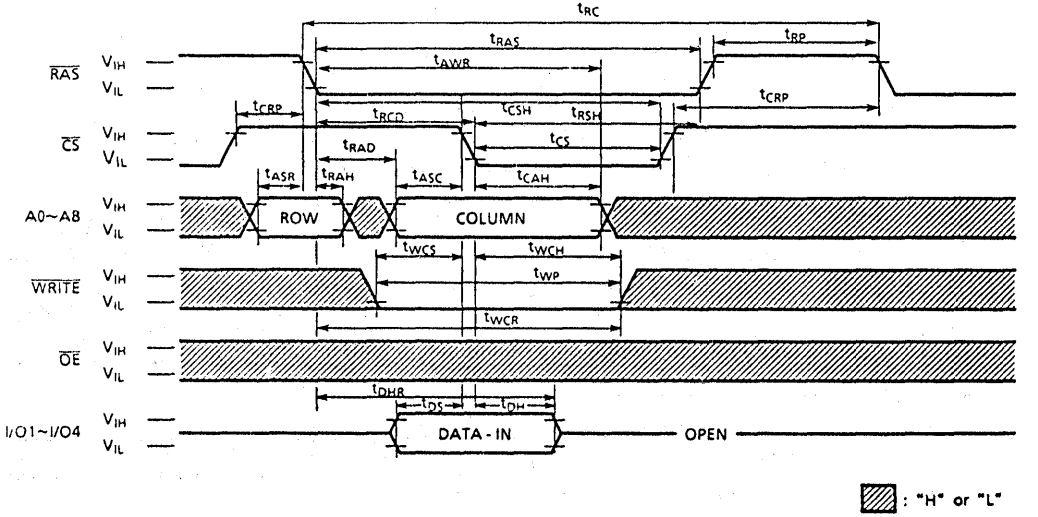
NOTES:

1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
16. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled by t_{AA}.
17. t_{AH} is the condition to latch column address when $\overline{RAS}$ has risen up.

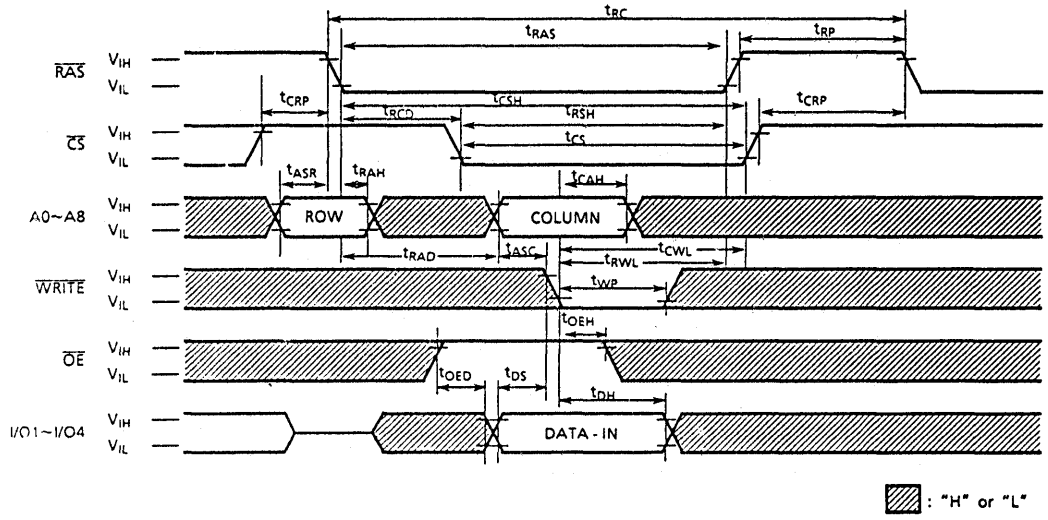
READ CYCLE



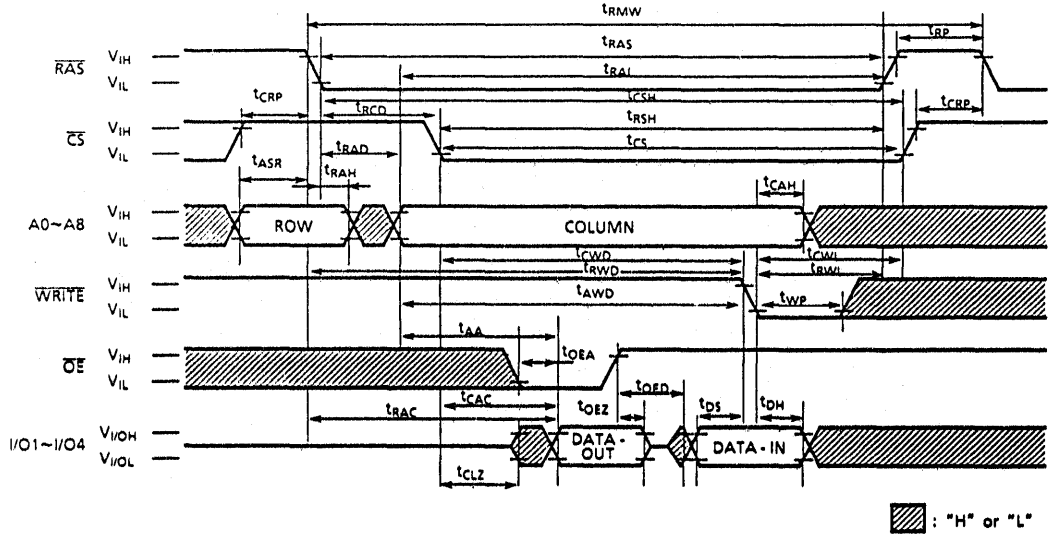
WRITE CYCLE (EARLY WRITE)



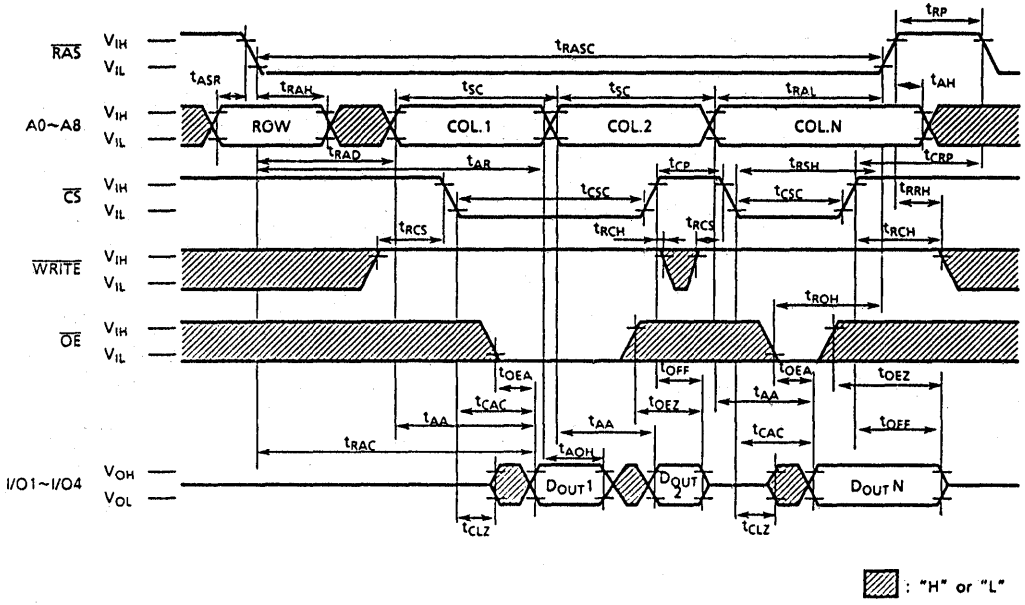
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



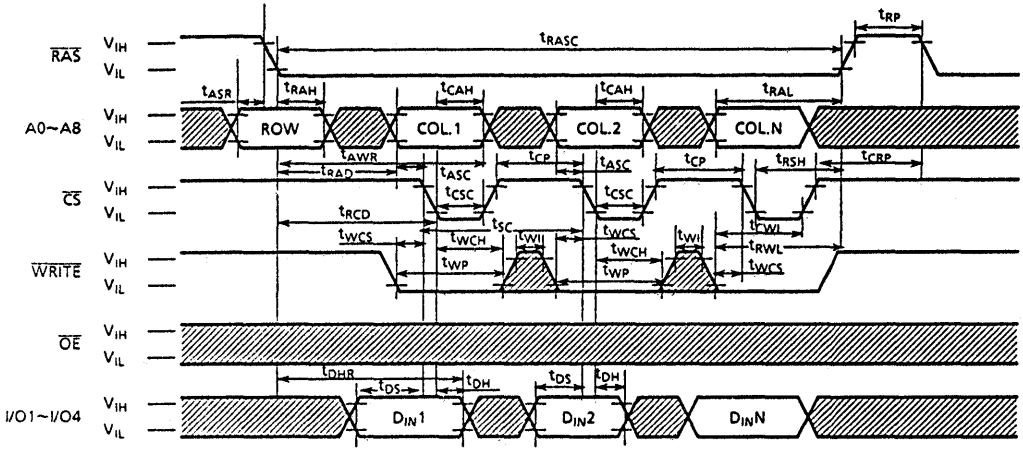
READ - MODIFY - WRITE CYCLE



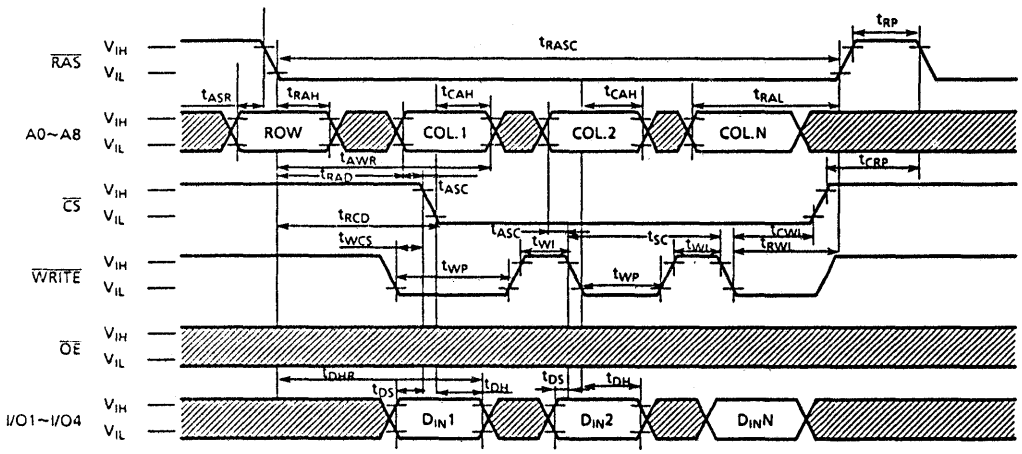
STATIC COLUMN MODE READ CYCLE



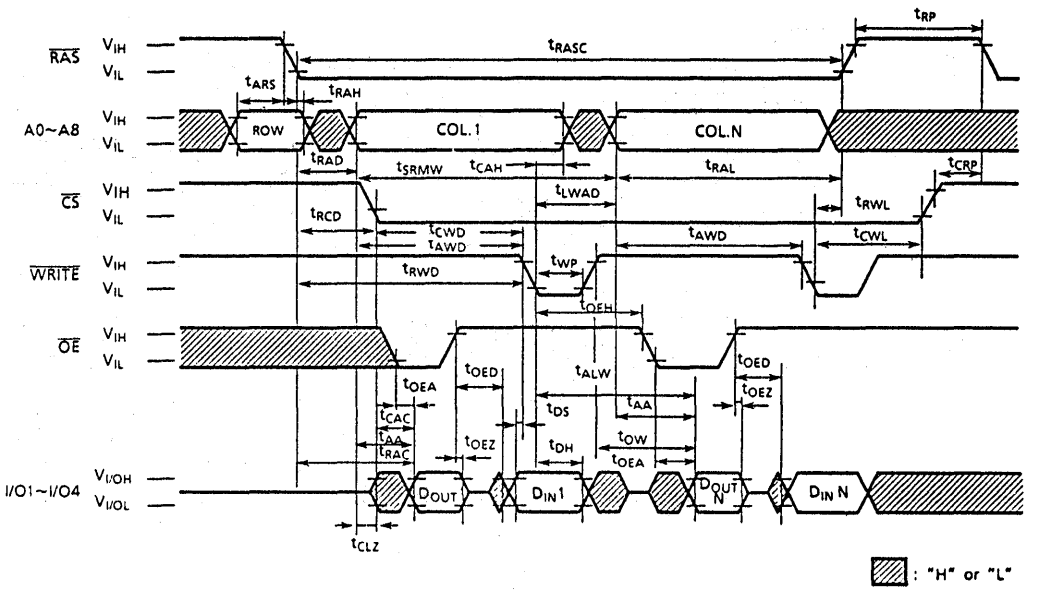
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



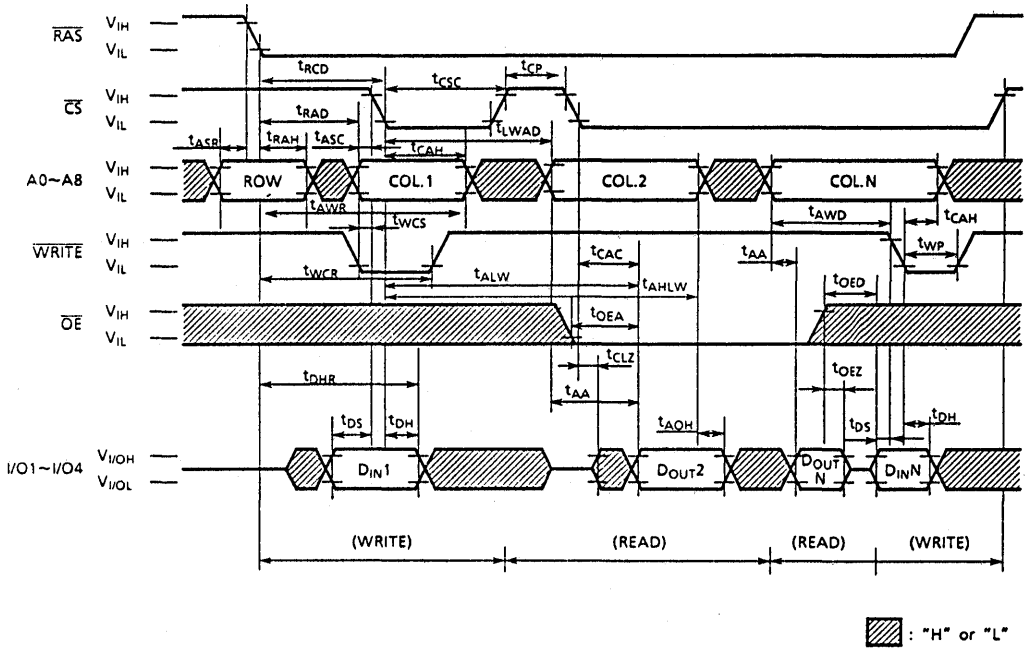
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



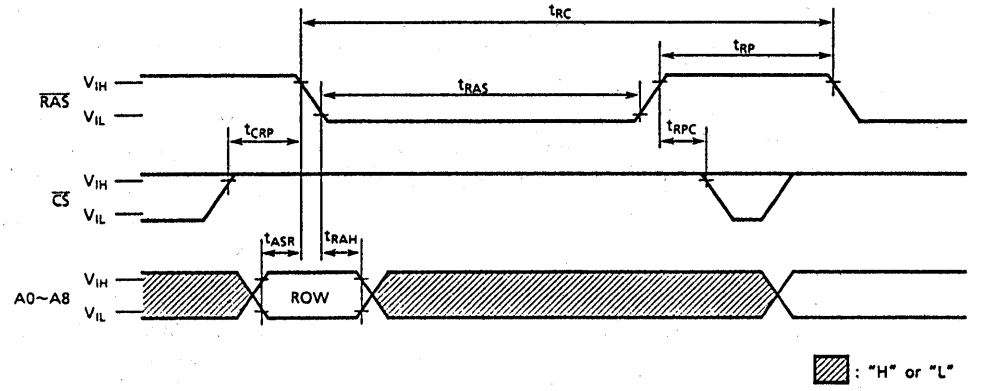
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

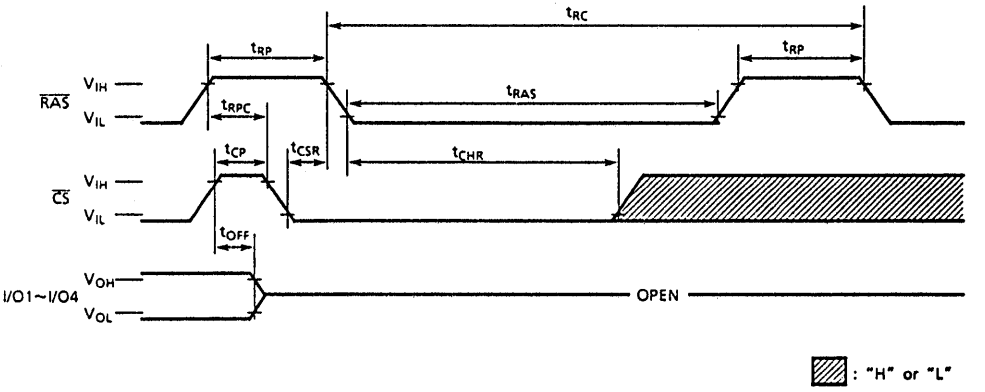


$\overline{RAS}$ ONLY REFRESH CYCLE



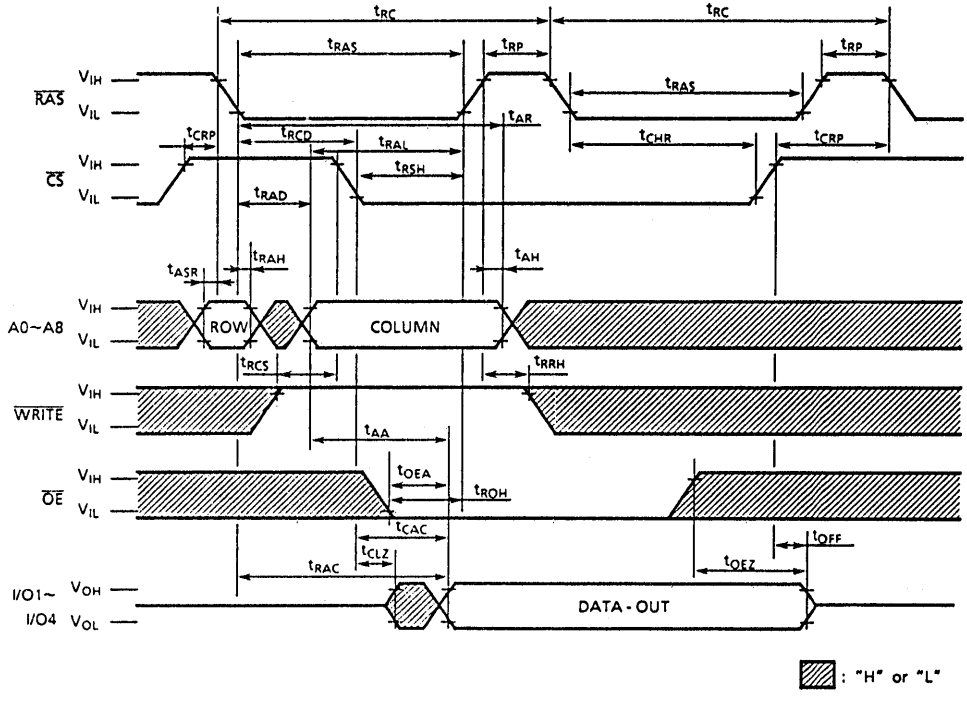
Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

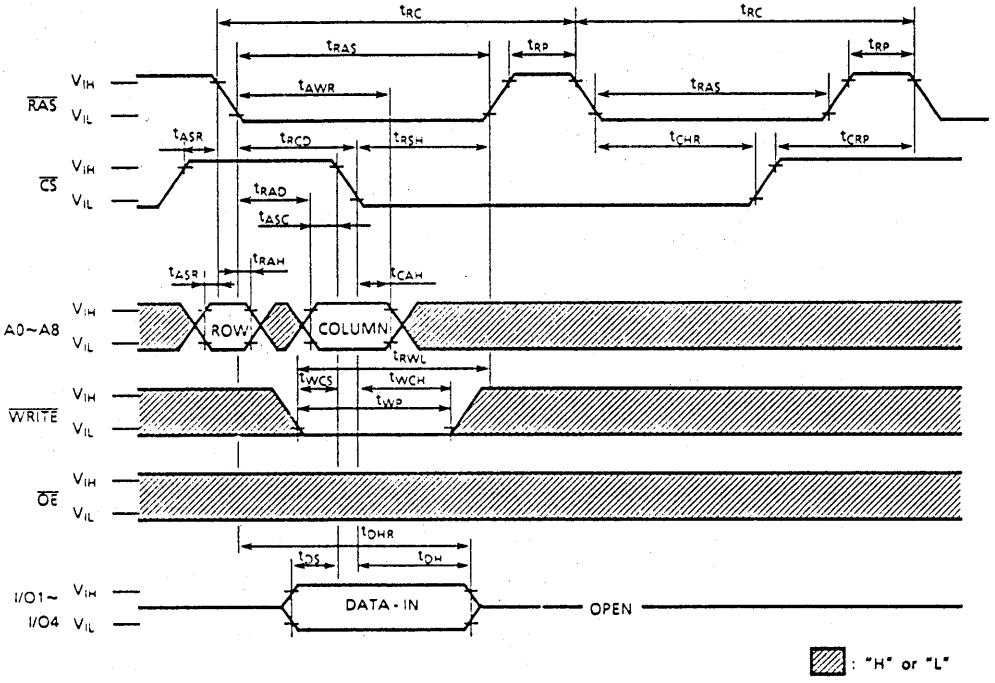


Note: $\overline{WRITE}$, $\overline{OE}$, A0~A8 = "H" or "L"

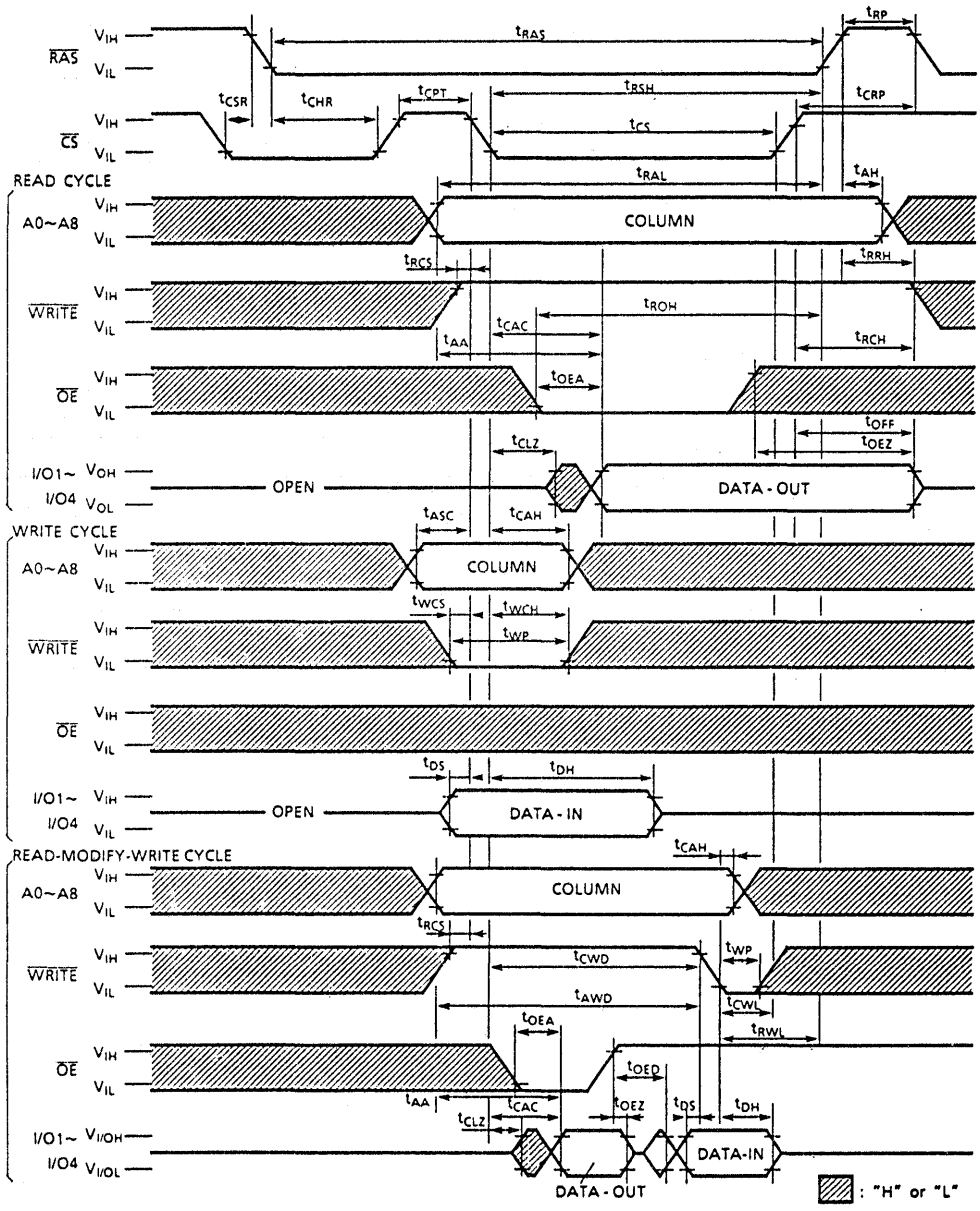
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



NOTES

262,144 WORD × 4 BIT DYNAMIC RAM

PRELIMINARY

DESCRIPTION

The TC514266BP/BJ/BZ/BFT is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514266BP/BJ/BZ/BFT utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user.

Multiplexed address inputs permit the TC514266BP/BJ/BZ/BFT to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ, 20/19 pin plastic ZIP, 24/20 pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

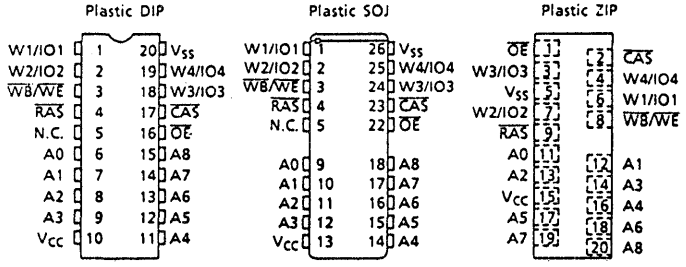
FEATURES

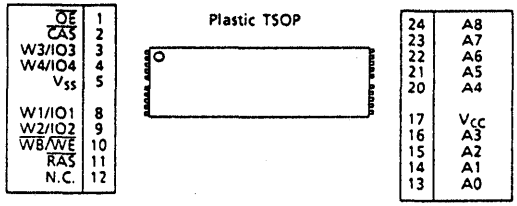
- 262,144 word by 4 bit organization
- Fast access time and cycle time

		TC514266BP/BJ/BZ/BFT-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  495mW MAX. Operating
  5.5mW MAX. Stand by
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write per Bit and Fast Page Mode capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/8ms
- Package
  TC514266BP : DIP20-P-300B
  TC514266BJ : SOJ26-P-300
  TC514266BZ : ZIP20-P-400
  TC514266BFT : TSOP24-P-0616

PIN CONNECTION

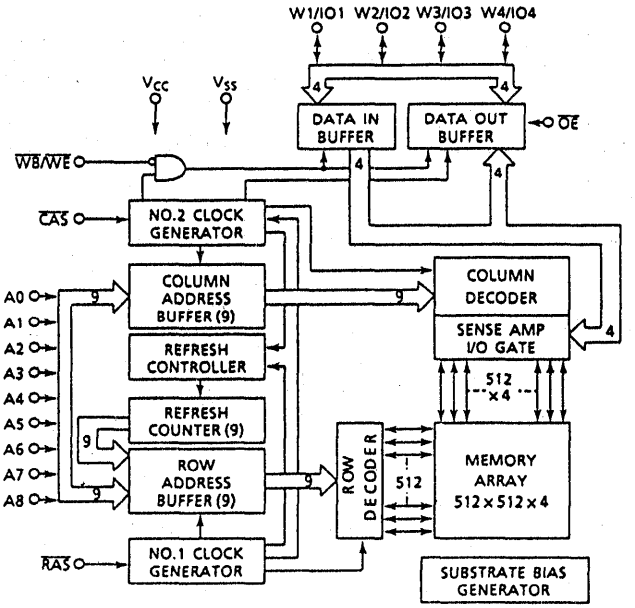




PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
$\overline{WB/WE}$	Write Per Bit/Read/Write Inpı
$\overline{OE}$	Output Enable
W1/IO1~W4/IO4	Write Select/Date Input/Outp
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514266BP/BJ/BZ/BFT-60	–	90	mA	3, 4 5
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC514266BP/BJ/BZ/BFT-60	–	90	mA	3, 5
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC514266BP/BJ/BZ/BFT-60	–	60	mA	3, 4 5
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC514266BP/BJ/BZ/BFT-60	–	90	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins not under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC514266BP/BJ/BZ/BFT-60		UNIT	NOTES
		MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	-	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	60	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	-	20	ns	9,14
t_{AA}	Access Time from Column Address	-	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	-	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	ns	
t_{ASR}	Row Address Set-Up Time	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	ns	11
t_{RRH}	,Read Command Hold Time referenced to $\overline{RAS}$	0	-	ns	11
t_{WCH}	Write Command Hold Time	10	-	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	-	ns	
t_{WP}	Write Command Pulse Width	10	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	TC514266BP/BJ/BZ/BFT-60		UNITS	NOTES
		MIN.	MAX.		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	ns	
t_{DS}	Data Set-Up Time	0	-	ns	12
t_{DH}	Data Hold Time	15	-	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	-	ns	
t_{REF}	Refresh Period	-	8	ms	
t_{WCS}	Write Command Set-UP Time	0	-	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	-	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	-	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	-	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	-	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	-	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	-	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	20	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	-	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	20	-	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	-	ns	
t_{WBH}	Write Per Bit Hold Time	10	-	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	-	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	-	ns	

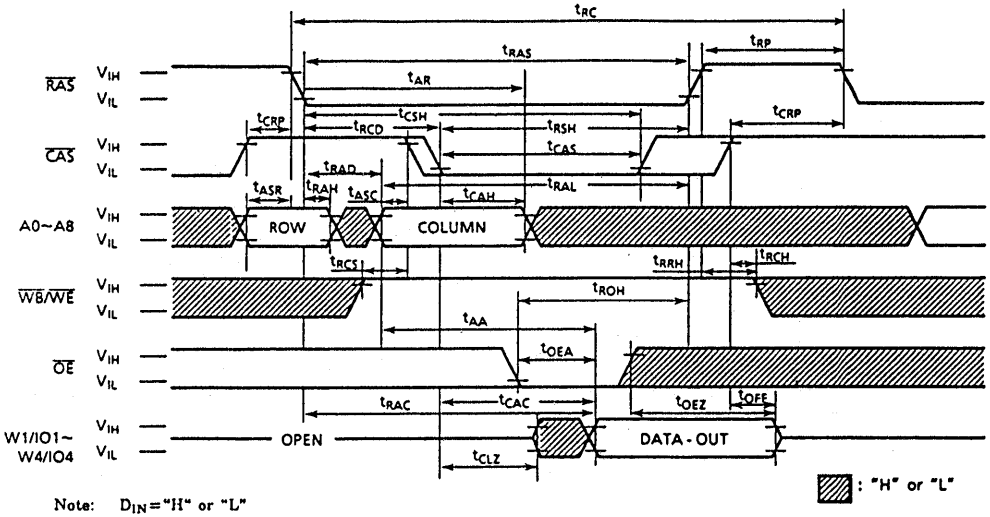
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	-	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W8}/\overline{WE}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (W1/I01~W4/I04)	-	7	pF

NOTES:

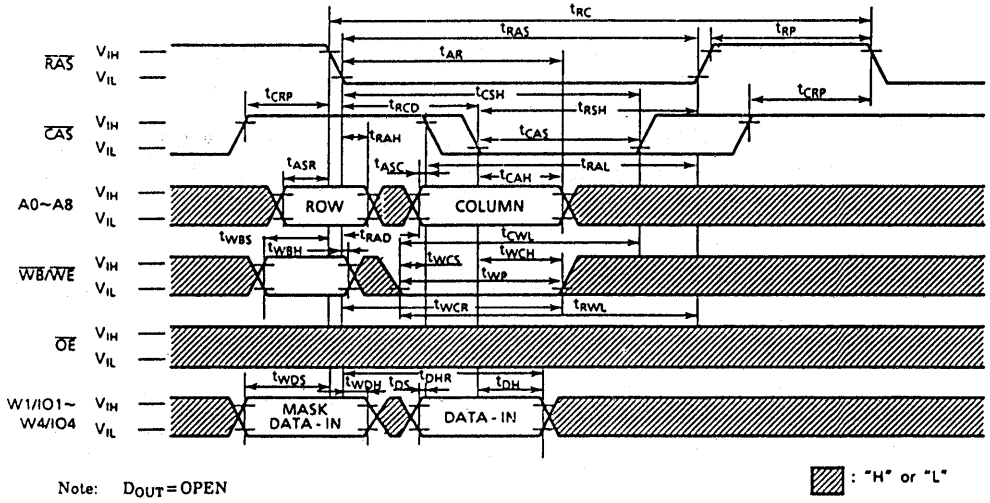
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB/WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



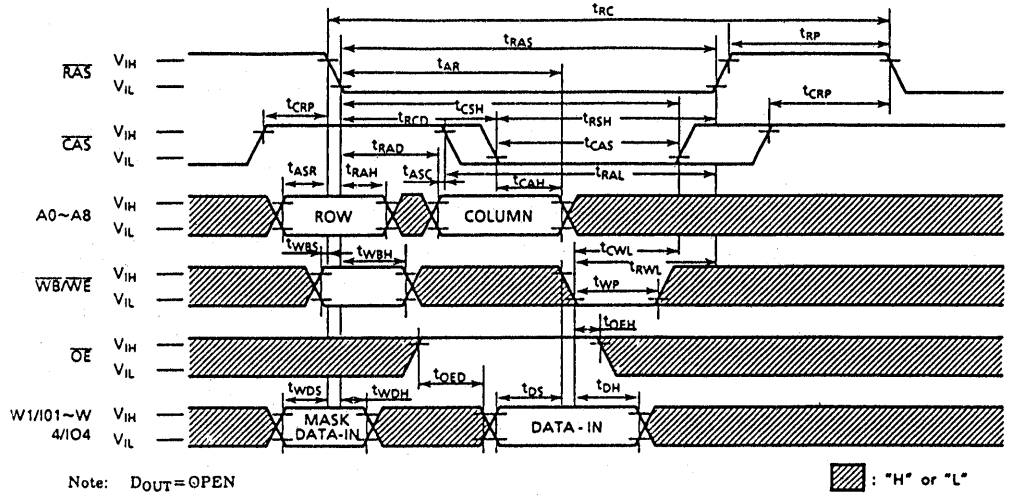
Note: D_{IN} = "H" or "L"

WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

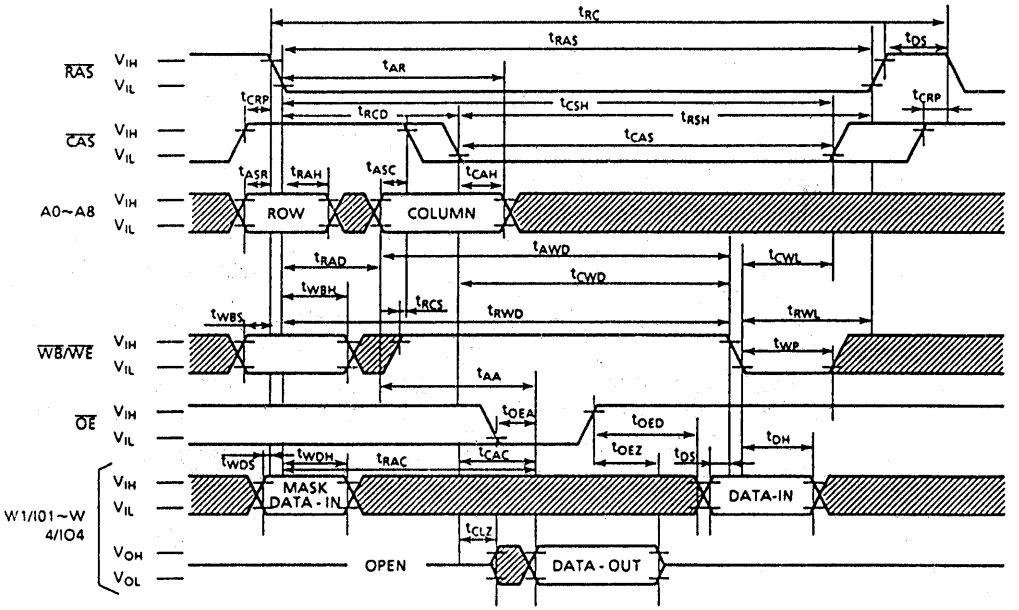
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



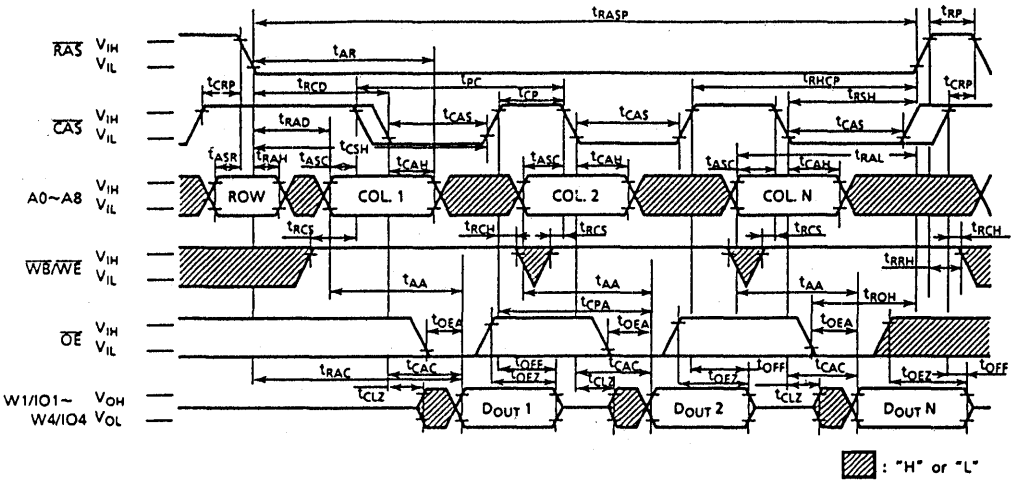
Note: D_{OUT} = OPEN

▨ : "H" or "L"

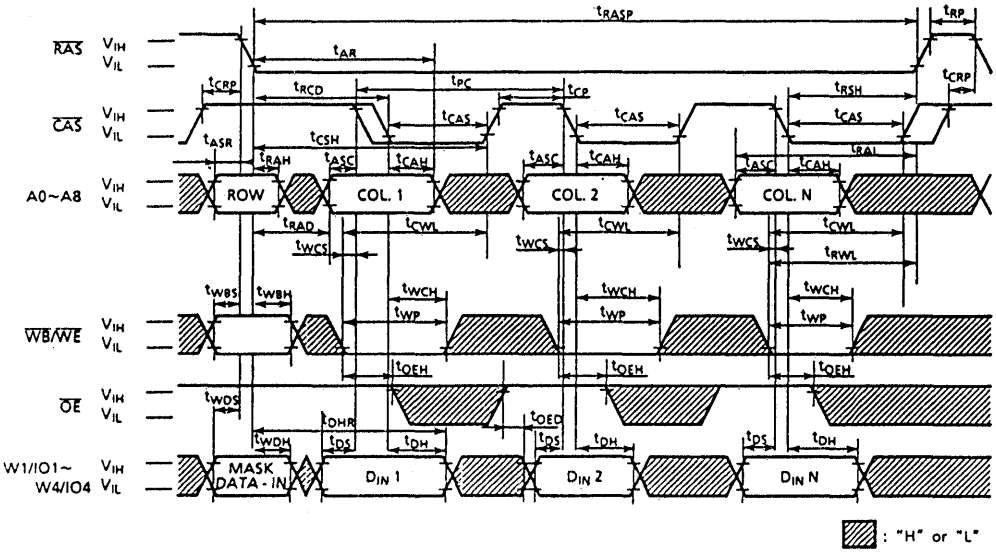
READ-MODIFY-WRITE CYCLE



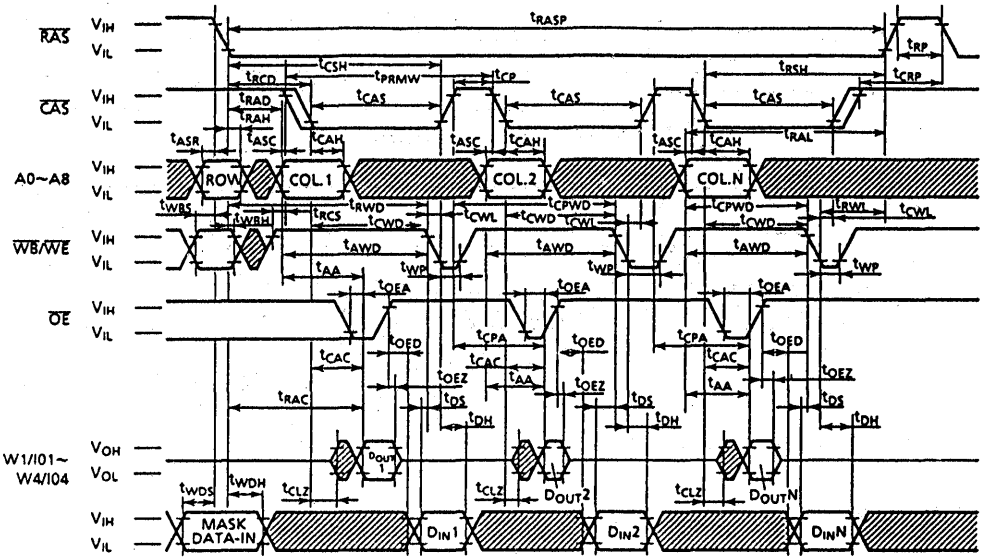
FAST PAGE MODE READ CYCLE



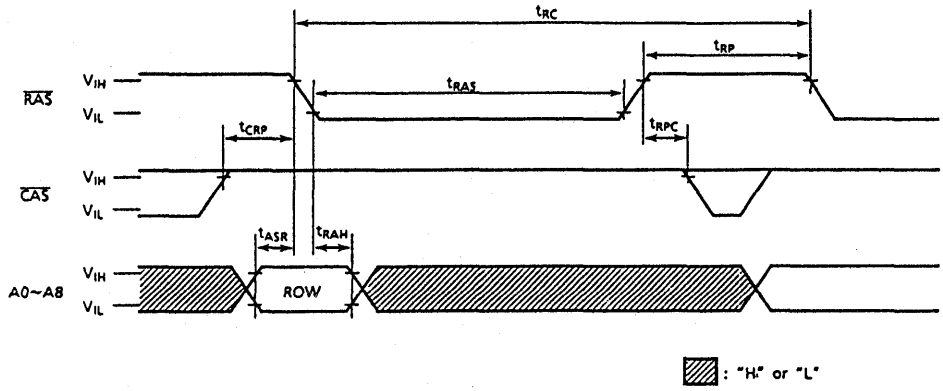
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

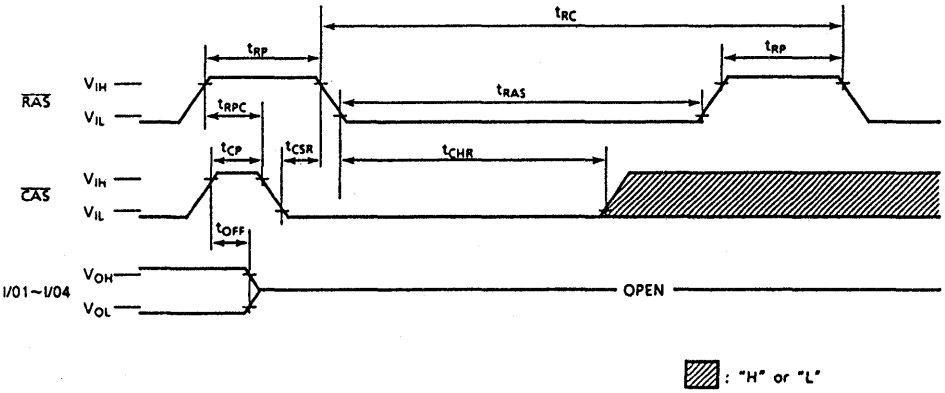


$\overline{RAS}$ ONLY REFRESH CYCLE



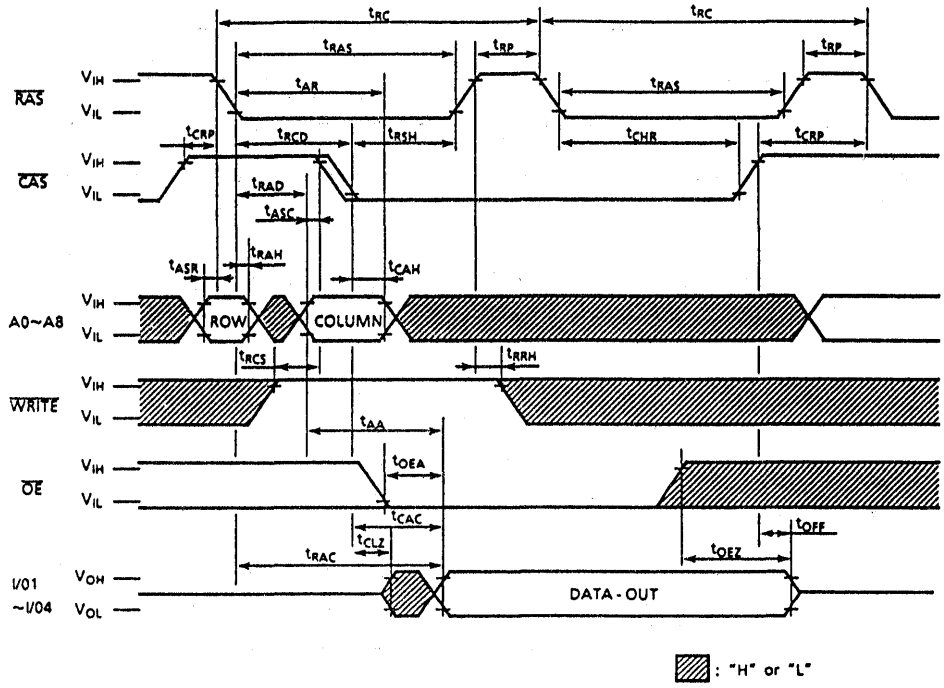
Note: WRITE, $\overline{OE}$="H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

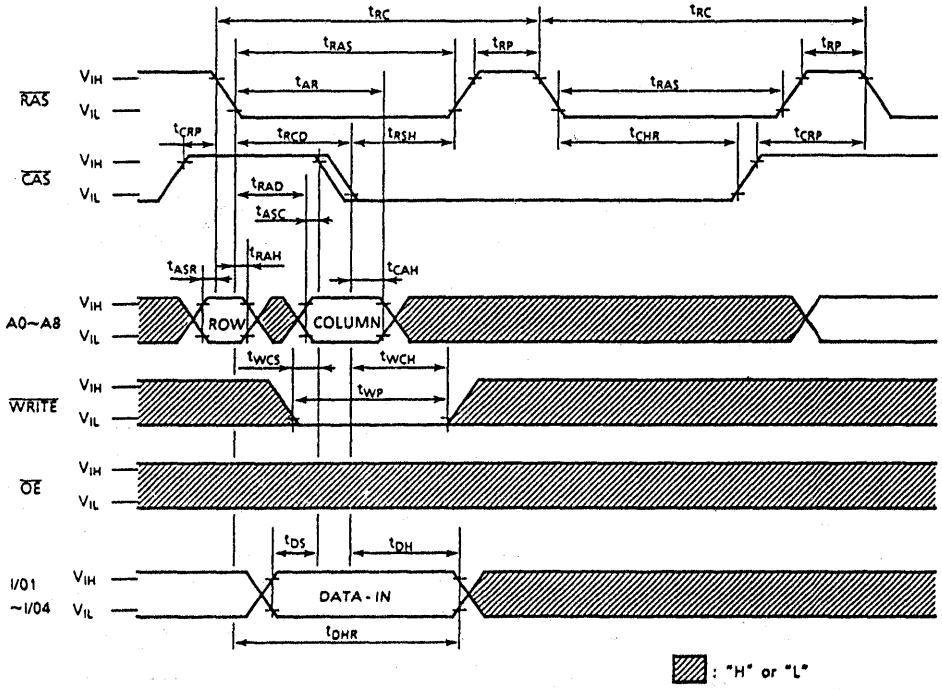


Note: WRITE, $\overline{OE}$=A0~A8="H" or "L"

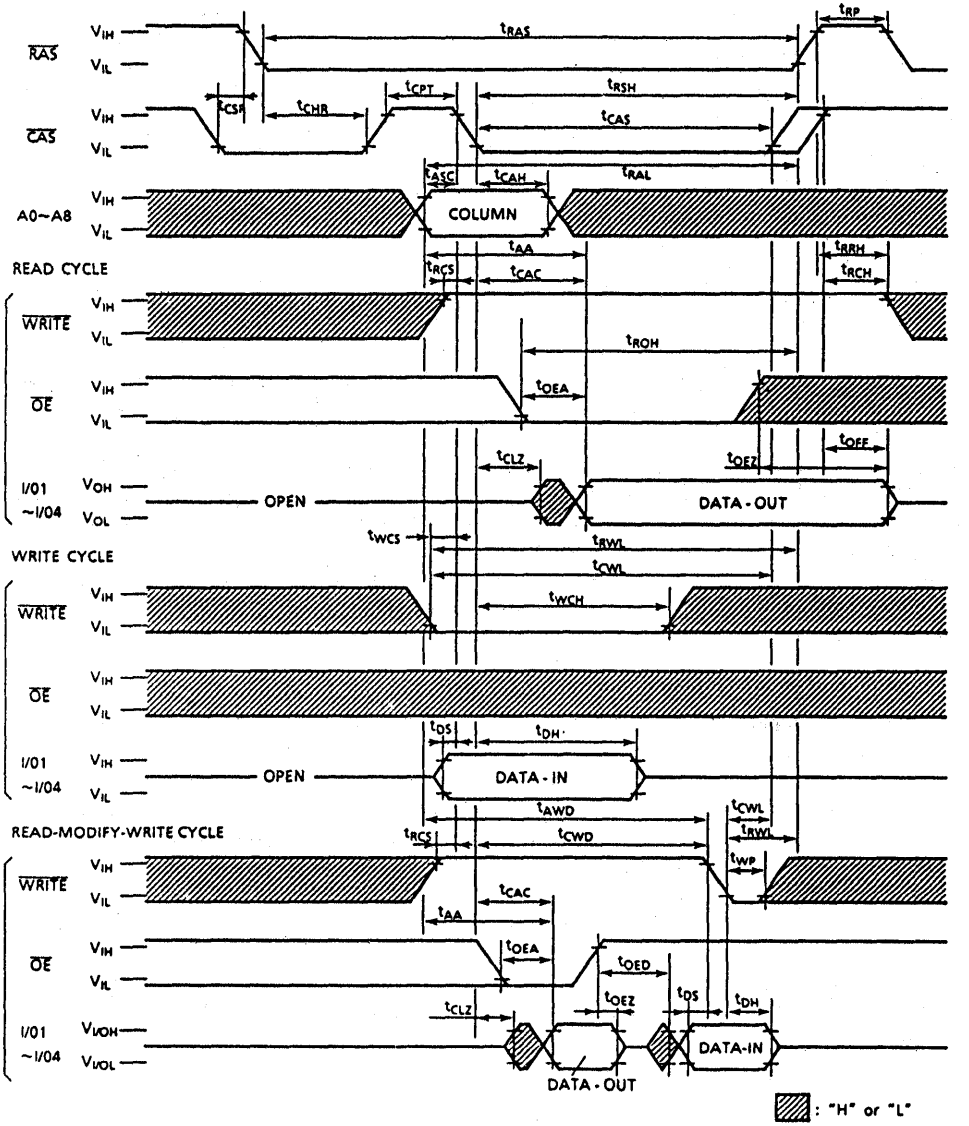
HIDDEN REFRESH CYCLE (READ)



HIDDEN REEFRESH CYCLE (WRITE)



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262, 144 cell locations within the TC514266BP/BJ/BZ/BFT are multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

Write Cycle. A write cycle is performed by bringing ($\overline{WB}$ /)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$ /)$\overline{WE}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/ $\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/ IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.

For those data bits of Wi (/ IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip if $\overline{WB}$(/ $\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valied after the access time has elapsed and remains valied while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A8) within each 8 millisecond time interval.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

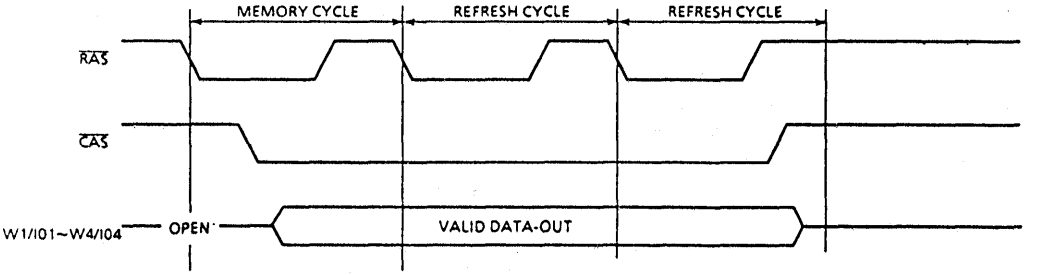
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514266BP/BJ/BZ/BFT offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514266BP/BJ/BZ/BFT allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514266BP/BJ/BZ/BFT is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514266BP/BJ/BZ/BFT can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

TENTATIVE DATA
262,144 WORD × 4 BIT DYNAMIC RAM

DESCRIPTION

The TC514266AP/AJ/AZ is the new generation dynamic RAM organized 262,144 words by 4 bits. The TC514266AP/AJ/AZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC514266AP/AJ/AZ to be packaged in a standard 20 pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- 262,144 word by 4 bit organization
- Fast access time and cycle time

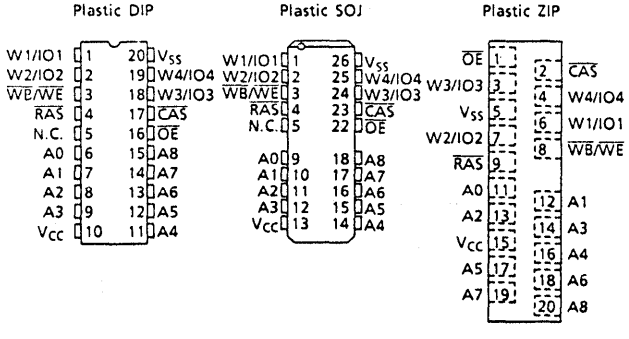
		TC514266AP/AJ/AZ-70/-80/-10		
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  - 440mW MAX. Operating (TC514266AP/AJ/AZ-70)
  - 385mW MAX. Operating (TC514266AP/AJ/AZ-80)
  - 330mW MAX. Operating (TC514266AP/AJ/AZ-10)
  - 5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write per Bit and Fast Page Mode capability
- All inputs and outputs TTL Compatible
- 512 refresh cycles/8ms
- Package TC514266AP : DIP20-P-300B
  TC514266AJ : SOJ26-P-300
  TC514266AZ : ZIP20-P-400

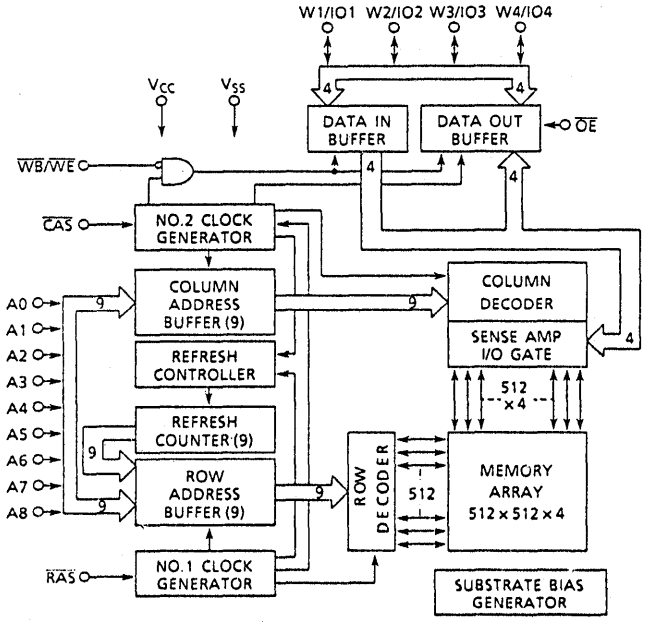
PIN NAMES

A0~A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB}/\overline{WE}$	Write Per Bit/Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~W4/IO4	Write Select/Date Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature·Time	T_{SOLDER}	260·10	°C·sec	1
Power Dissipation	P_D	600	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC514266AP/AJ/AZ-70	–	80	mA	3, 4, 5
		TC514266AP/AJ/AZ-80	–	70		
		TC514266AP/AJ/AZ-10	–	60		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC514266AP/AJ/AZ-70	–	80	mA	3, 5
		TC514266AP/AJ/AZ-80	–	70		
		TC514266AP/AJ/AZ-10	–	60		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC514266AP/AJ/AZ-70	–	60	mA	3, 4, 5
		TC514266AP/AJ/AZ-80	–	50		
		TC514266AP/AJ/AZ-10	–	40		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC514266AP/AJ/AZ-70	–	80	mA	3
		TC514266AP/AJ/AZ-80	–	70		
		TC514266AP/AJ/AZ-10	–	60		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c) (Notes 6, 7, 8)

SYMBOL	CHARACTERISTIC	TC514266AP/AJ/AZ-70		TC514266AP/AJ/AZ-80		TC514266AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	50	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	CHARACTERISTIC	TC514266AP/AJ/AZ-70		TC514266AP/AJ/AZ-80		TC514266AP/AJ/AZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	10	–	ns	

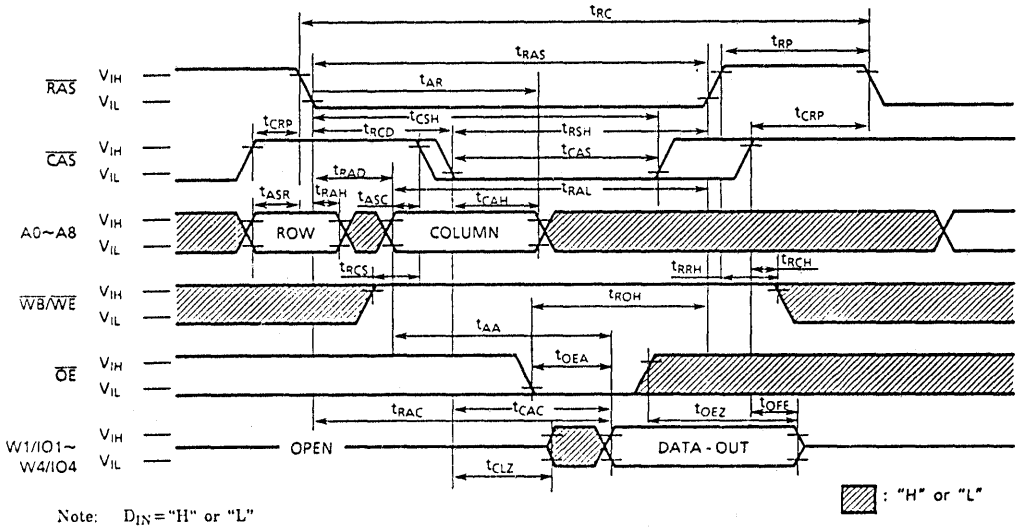
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°c)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/I01~W4/I04)	–	7	pF

NOTES:

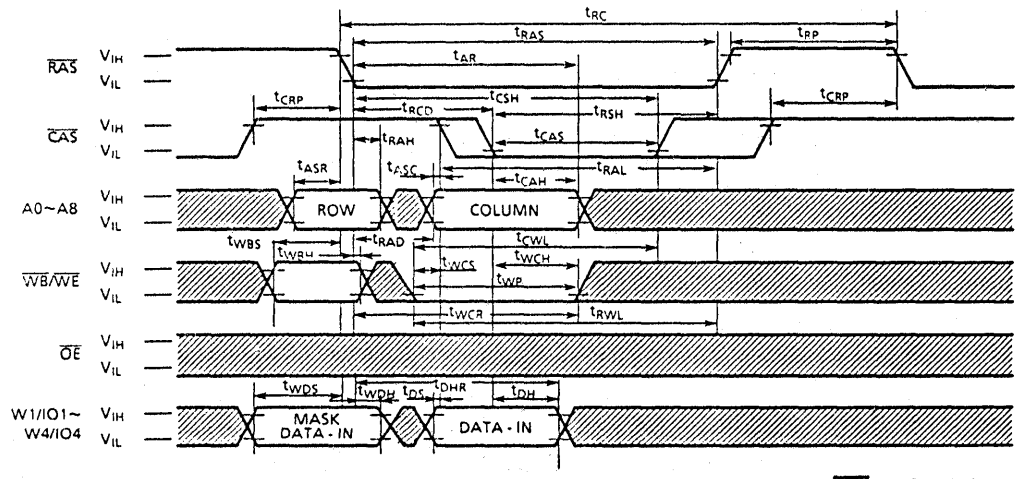
1. Stresses greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WB/WE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE



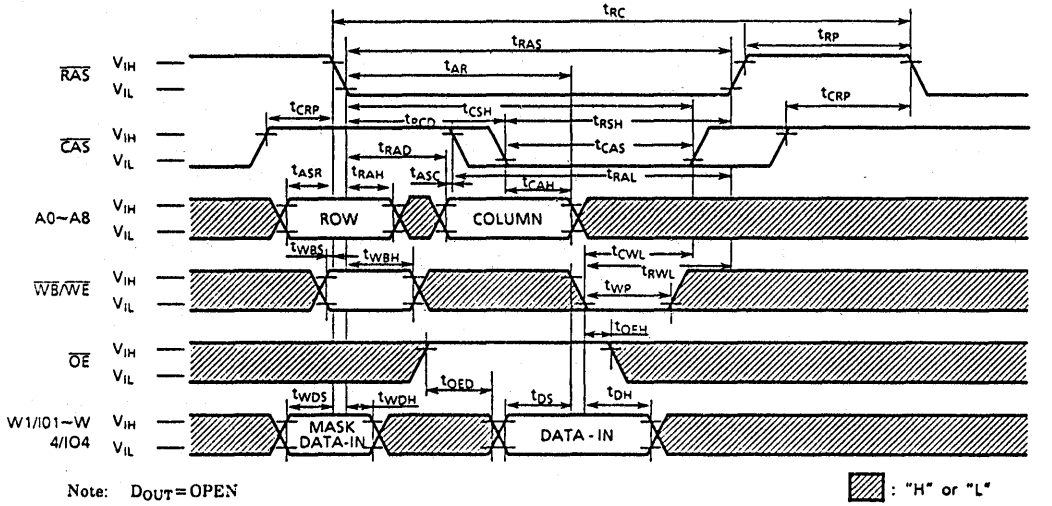
Note: D_{IN} = "H" or "L"

WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

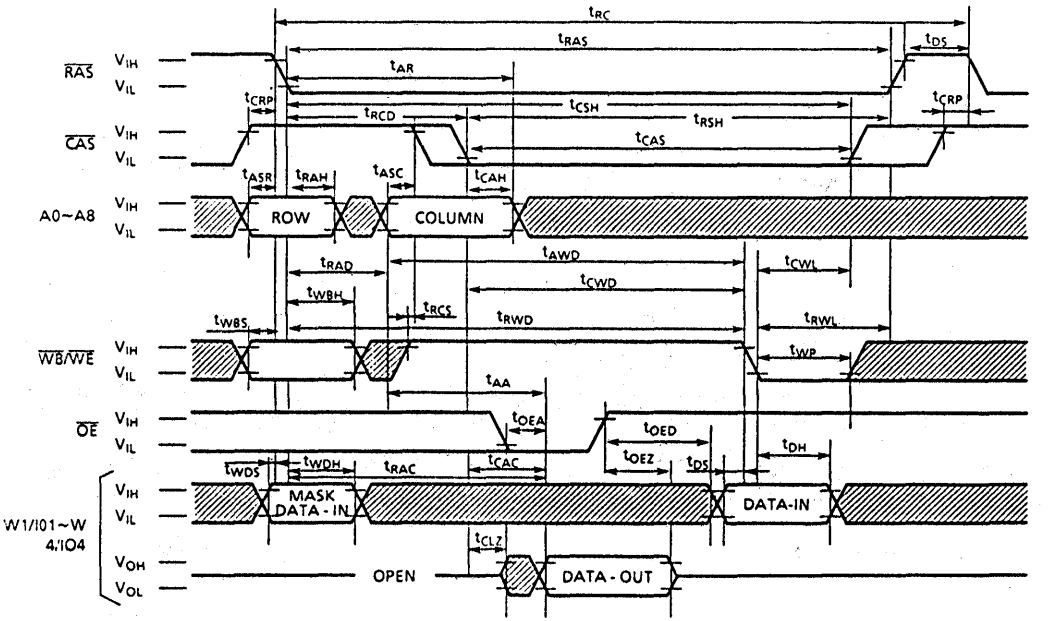
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



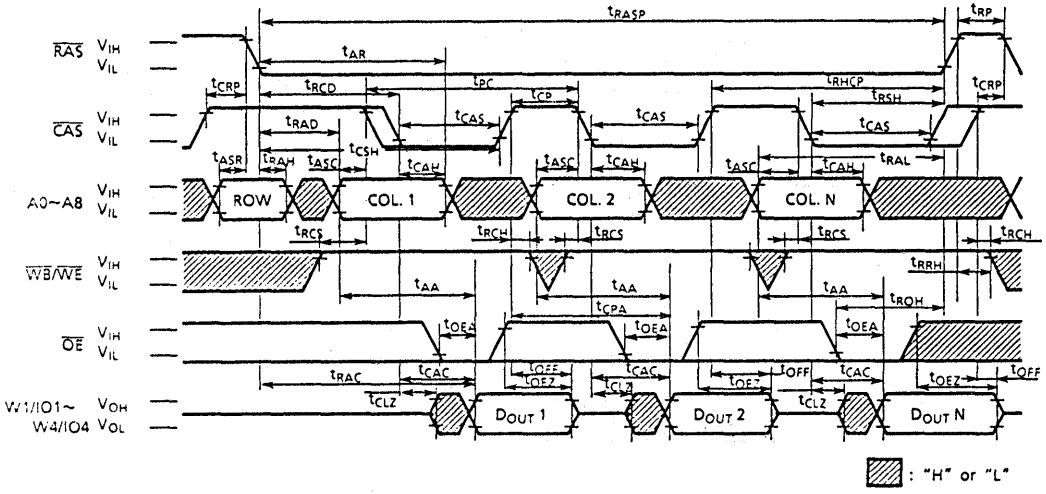
Note: D_{OUT} = OPEN

▨ : "H" or "L"

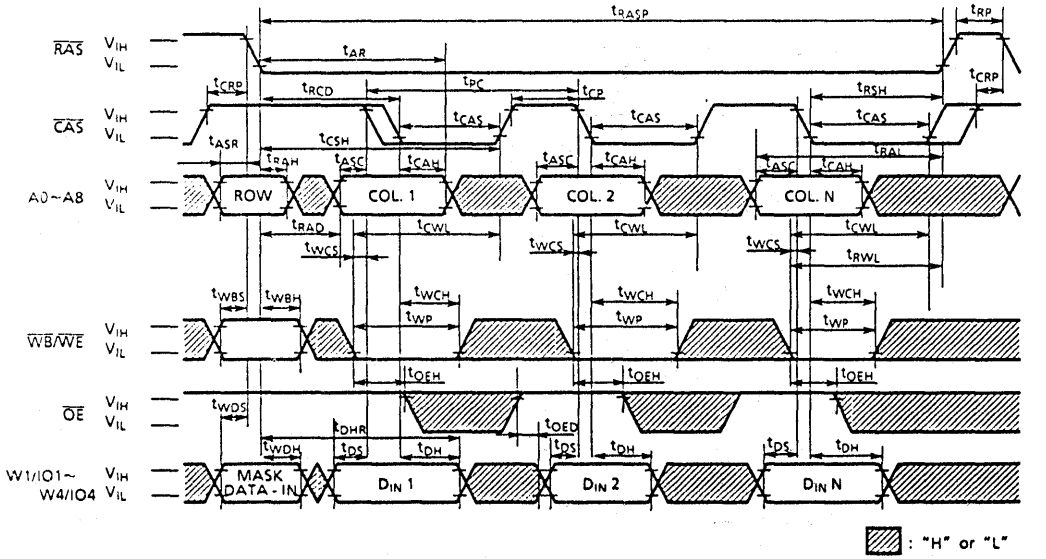
READ-MODIFY-WRITE CYCLE



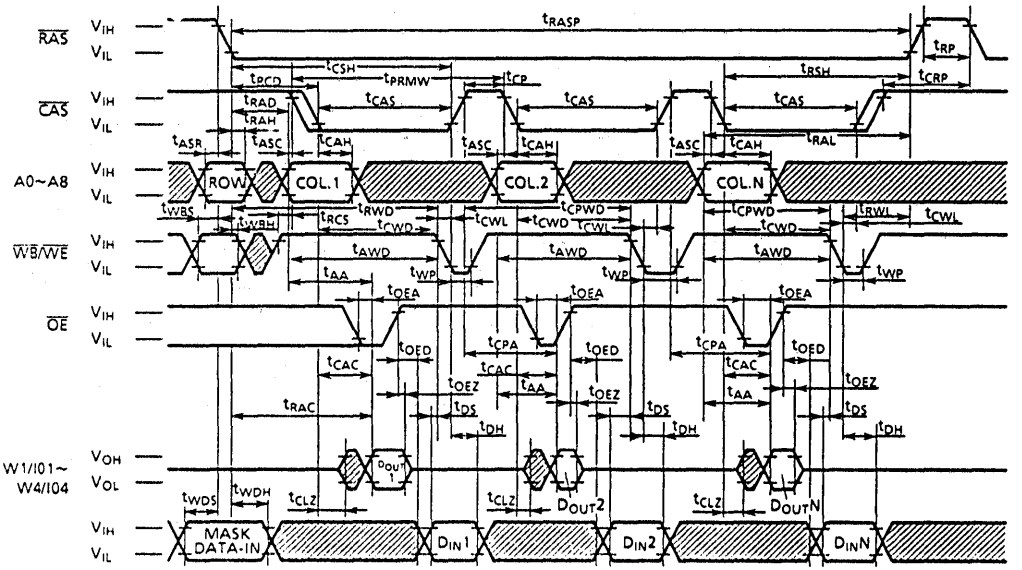
FAST PAGE MODE READ CYCLE



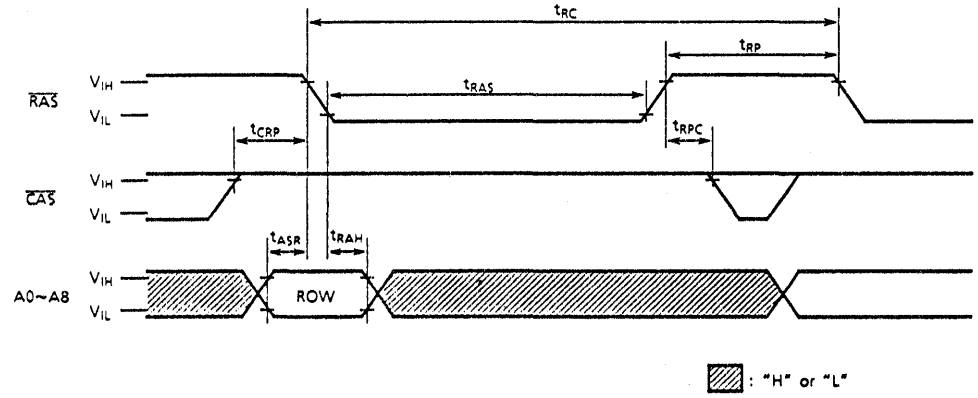
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

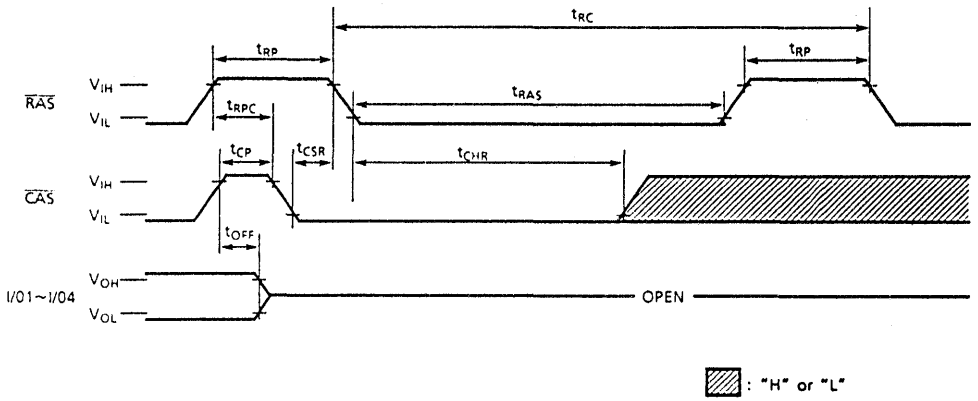


$\overline{RAS}$ ONLY REFRESH CYCLE



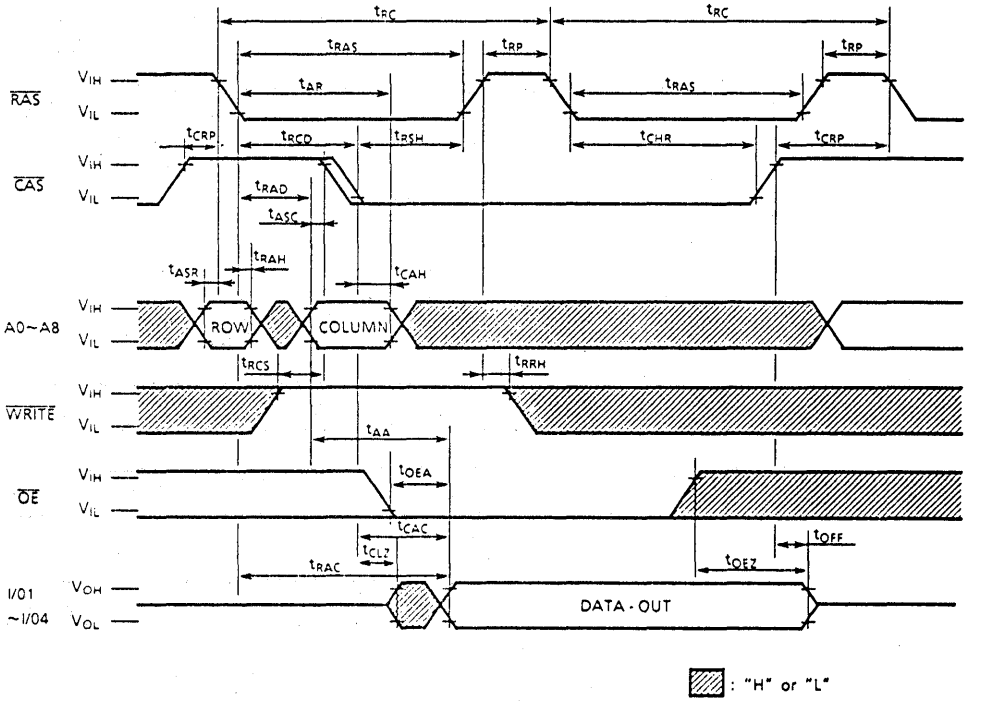
Note: $\overline{WRITE}$, $\overline{OE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

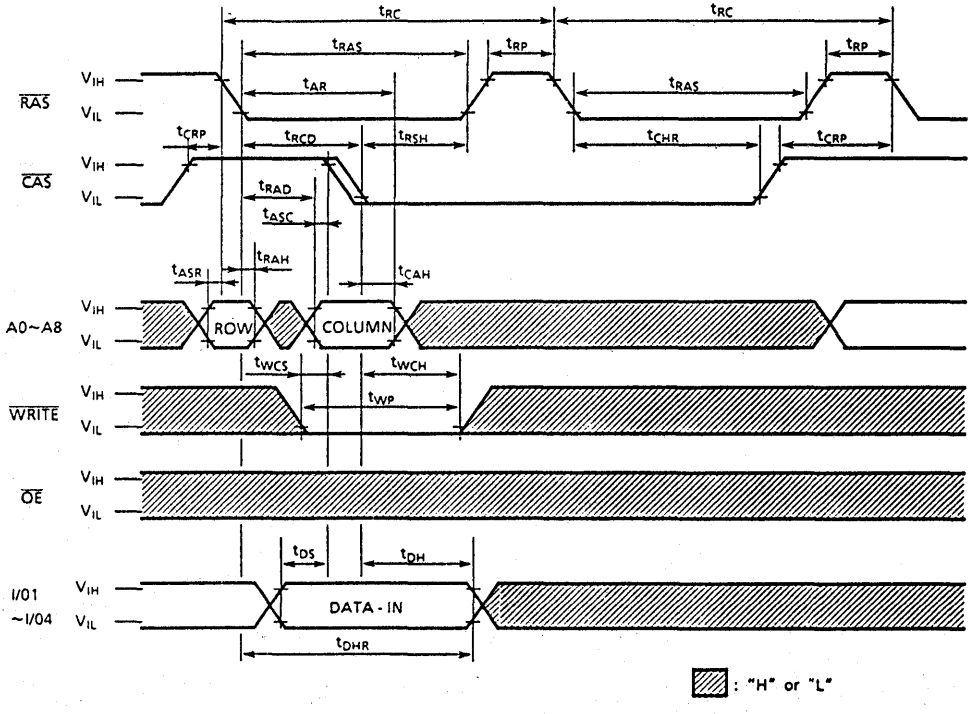


Note: $\overline{WRITE}$, $\overline{OE}$ = A0~A8 = "H" or "L"

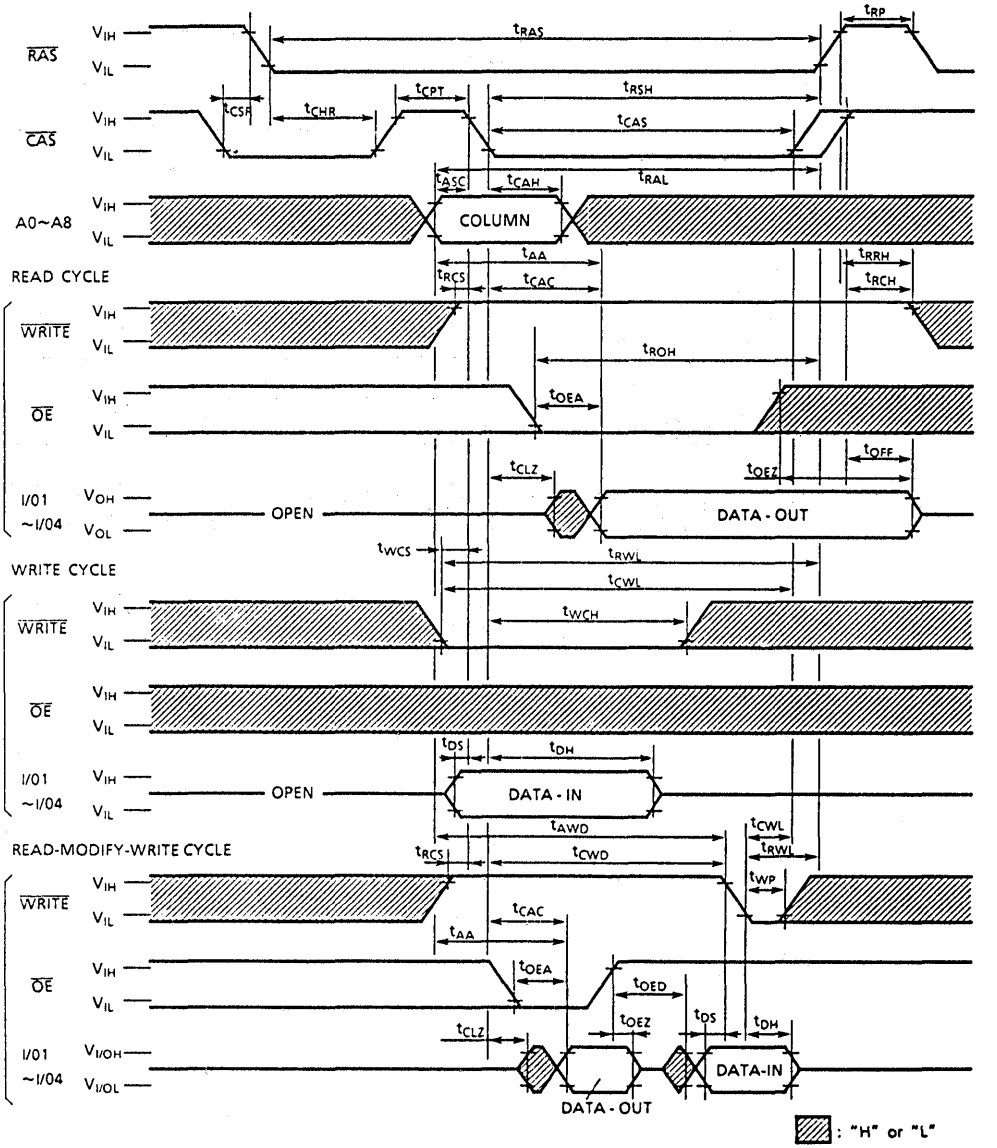
HIDDEN REFRESH CYCLE (READ)



HIDDEN REEFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 18 address bits required to decode 1 of the 262, 144 cell locations within the TC514266AP/AJ/AZare multiplexed onto the 9 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 9 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 9 column address bits into the chip. Each of these signals, $\overline{RAS}$, and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

DATA INPUTS

Write Cycle. A write cycle is performed by bringing ($\overline{WB}$ /)$\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$ /)$\overline{WE}$ strobes data on (Wi) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$(/ $\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/ IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition.

For those data bits of Wi (/ IOi) that are kept low as $\overline{RAS}$ talls the write operation is inhibited on the chip if $\overline{WB}$(/ $\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

DATA OUTPUTS

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valied after the access time has elapsed and remains valied while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffer are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the output. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 512 row address (A0~A8) within each 8 millisecond time interval.

Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

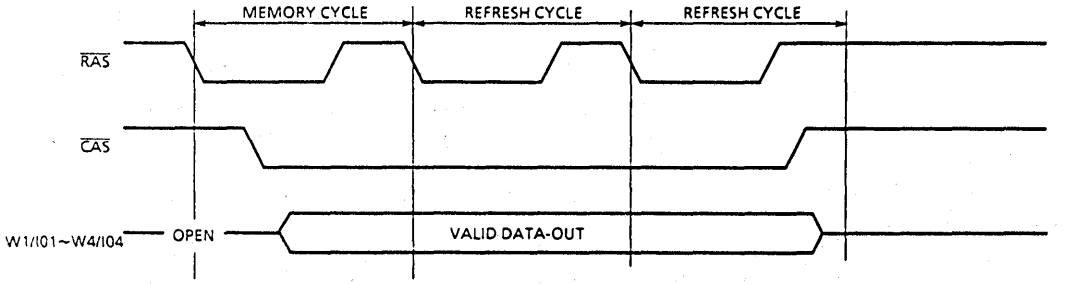
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC514266AP/AJ/AZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

PAGE MODE

The "Page-Mode" feature of the TC514266AP/AJ/AZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Page-Mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC514266AP/AJ/AZ is that refresh cycles may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC514266AP/AJ/AZ can be tested by $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-WRITE CYCLE). Repeat this operation 512 times.

③ Check "1" out of 512 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST. Repeat this operation 512 times.

⑤ Check "0" out of 512 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

65,536 WORD × 16 BIT DYNAMIC RAM

DESCRIPTION

The TC511664J/Z is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511664J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511664J/Z to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

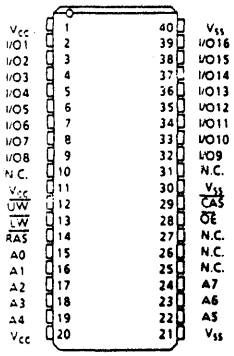
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511664J/Z - 80/ - 10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	40ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

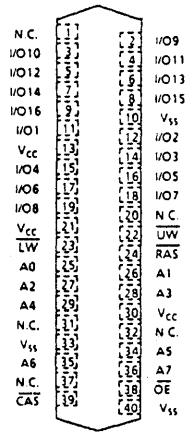
- Single power supply of 5V ± 10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511664J/Z – 80)
  495mW MAX. Operating (TC511664J/Z – 10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Byte-Write and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package Plastic SOJ : TC511664J
  Plastic ZIP : TC511664Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



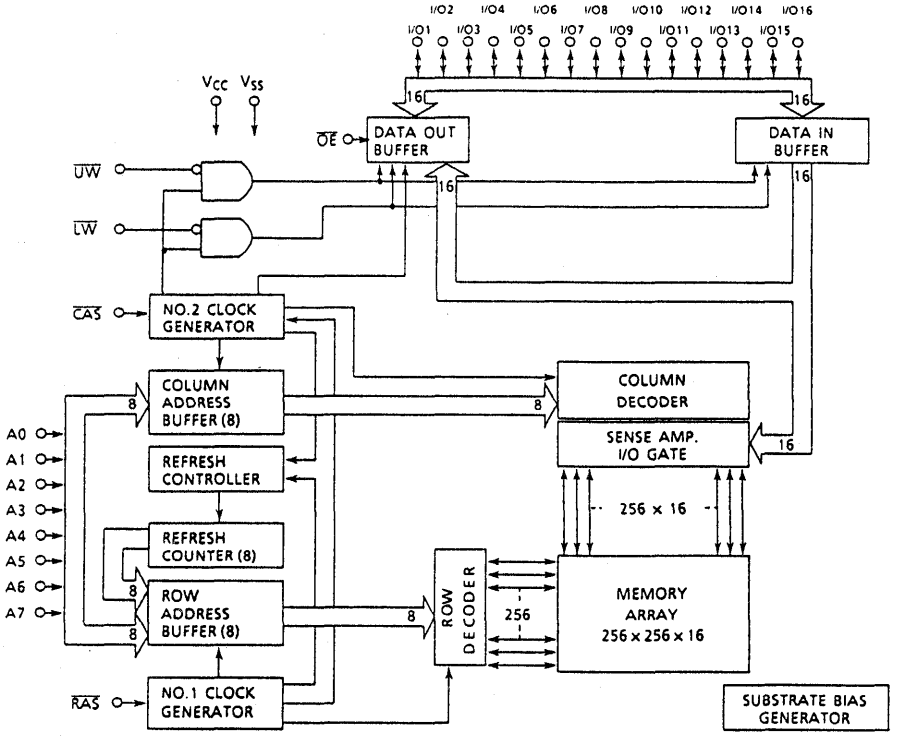
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Colomn Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Ouput Enable
I/O01~I/O16	Data Input/Output
V_{CC}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (I/O1~I/O16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511664J/Z-80	−	115	mA	3, 4, 5
		TC511664J/Z-10	−	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		−	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511664J/Z-80	−	115	mA	3, 5
		TC511664J/Z-10	−	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511664J/Z-80	−	70	mA	3, 4, 5
		TC511664J/Z-10	−	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		−	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511664J/Z-80	−	115	mA	3
		TC511664J/Z-10	−	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −2.5mA)		2.4	−	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		−	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511664J/Z-80		TC511664J/Z-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	35	–	40	ns	9,14
t_{AA}	Access Time from Column Address	–	45	–	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35	–	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511664J/Z-80		TC511664J/Z-10		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	4	–	4	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	70	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Trun Off Delay Time from $\overline{OE}$	0	10	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{MCS}	Masked Write Set-Up Time	0	–	0	–	ns	
t_{MRH}	Masked Write Hold time Referenced to $\overline{RAS}$	0	–	0	–	ns	
t_{MCH}	Masked Write Hold time Referenced to $\overline{CAS}$	0	–	0	–	ns	

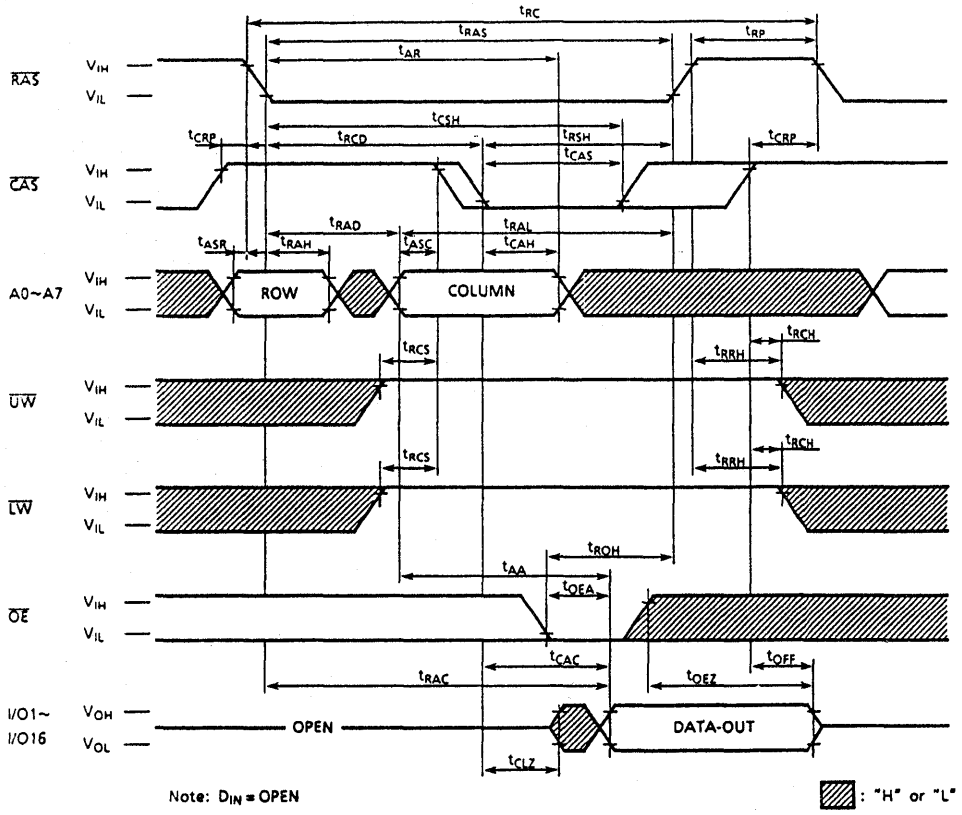
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A7)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	–	7	pF

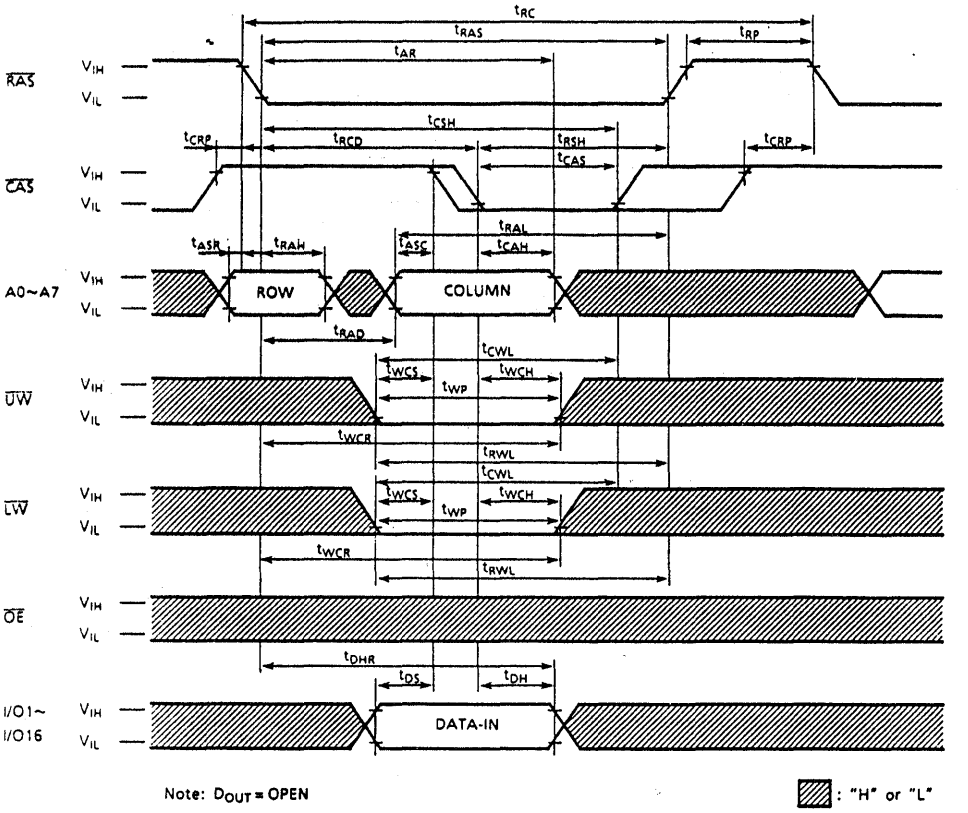
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 1 TTL load and 50pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{UW}$, $\overline{LW}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A7
ROW
COLUMN
tRCS
tRRH
tRCH
UW
LW
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1~
I/O16
VOH
VOL
OPEN
DATA-OUT
tCLZ
Note: DIN = OPEN
: "H" or "L"

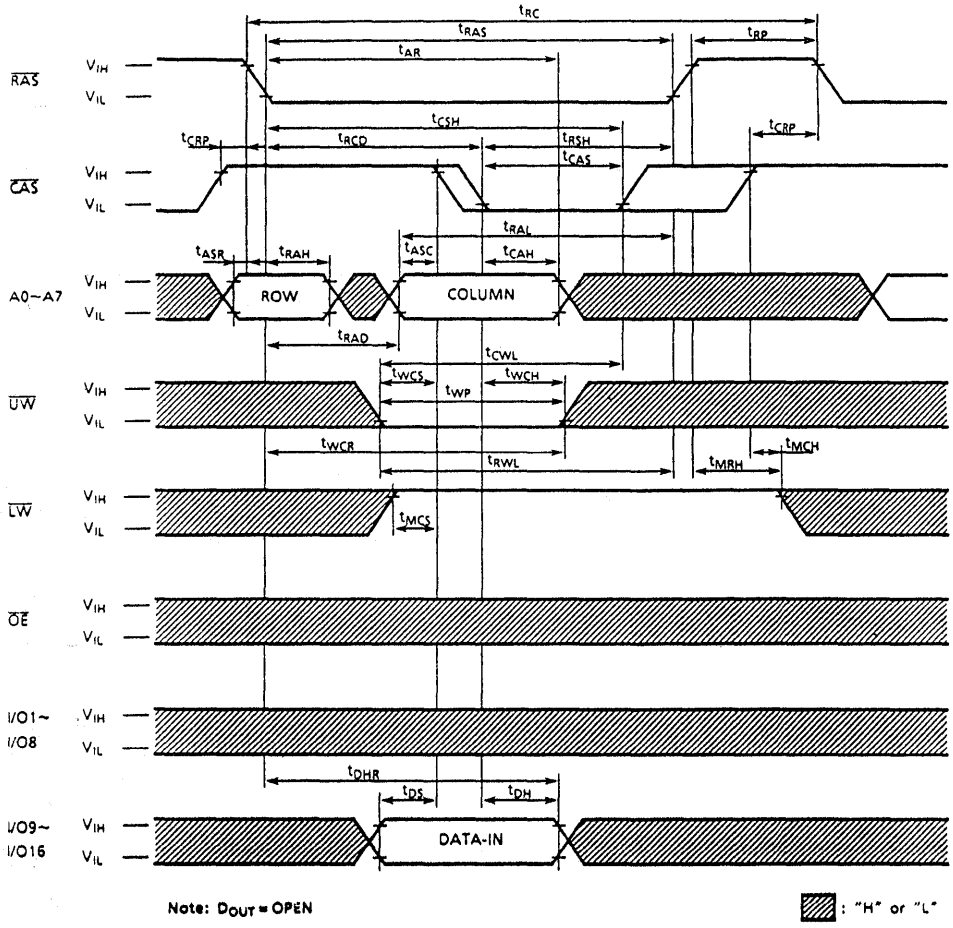
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

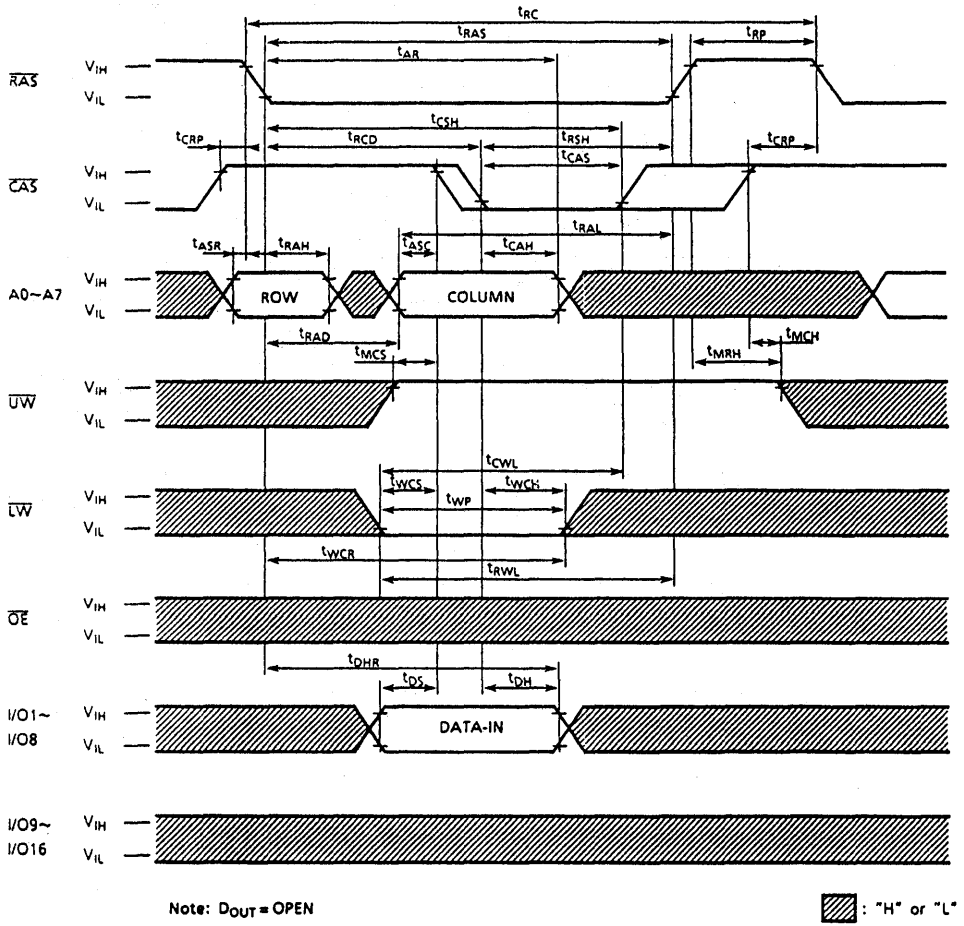
UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

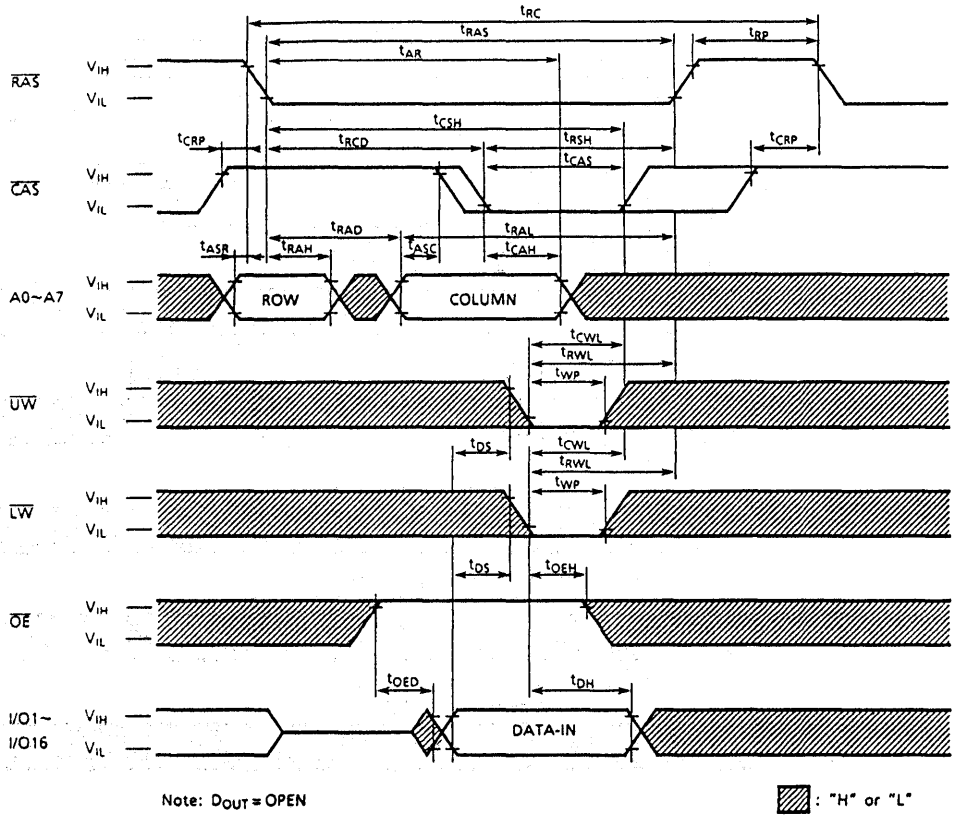
LOWER BYTE WRITE CYCLE (EARLY WRITE)



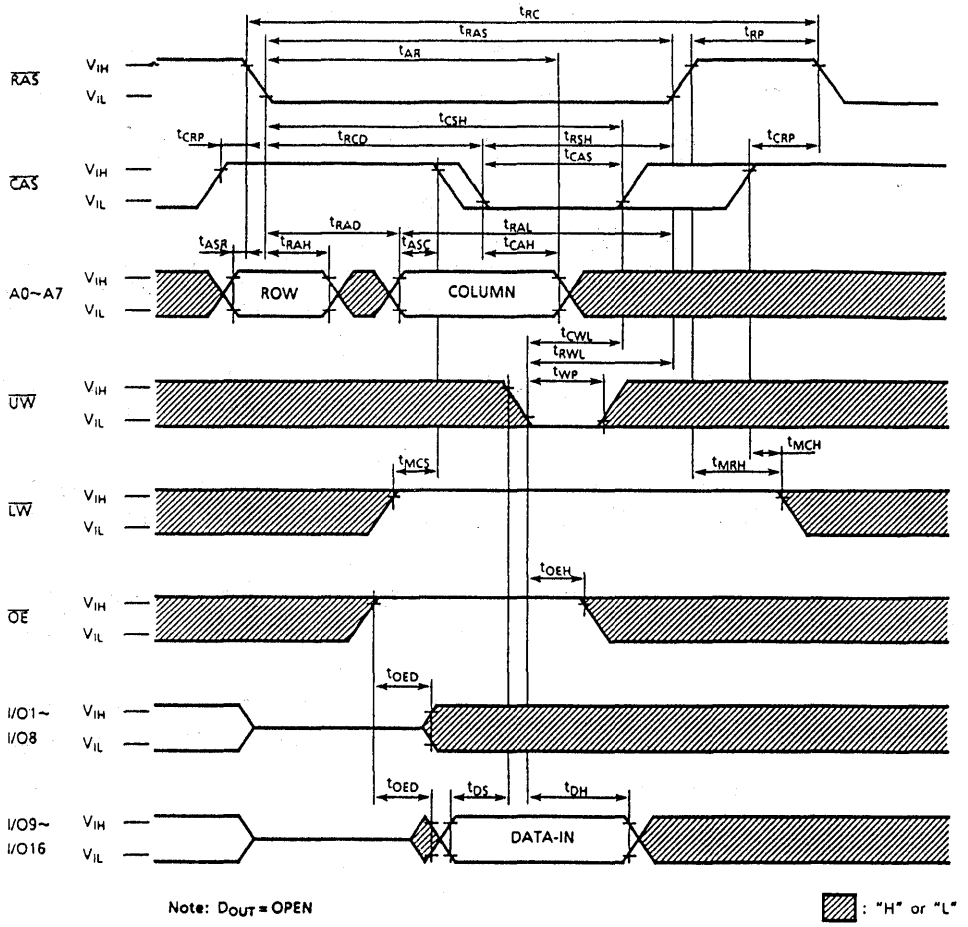
Note: D_{OUT} = OPEN

▨ : "H" or "L"

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



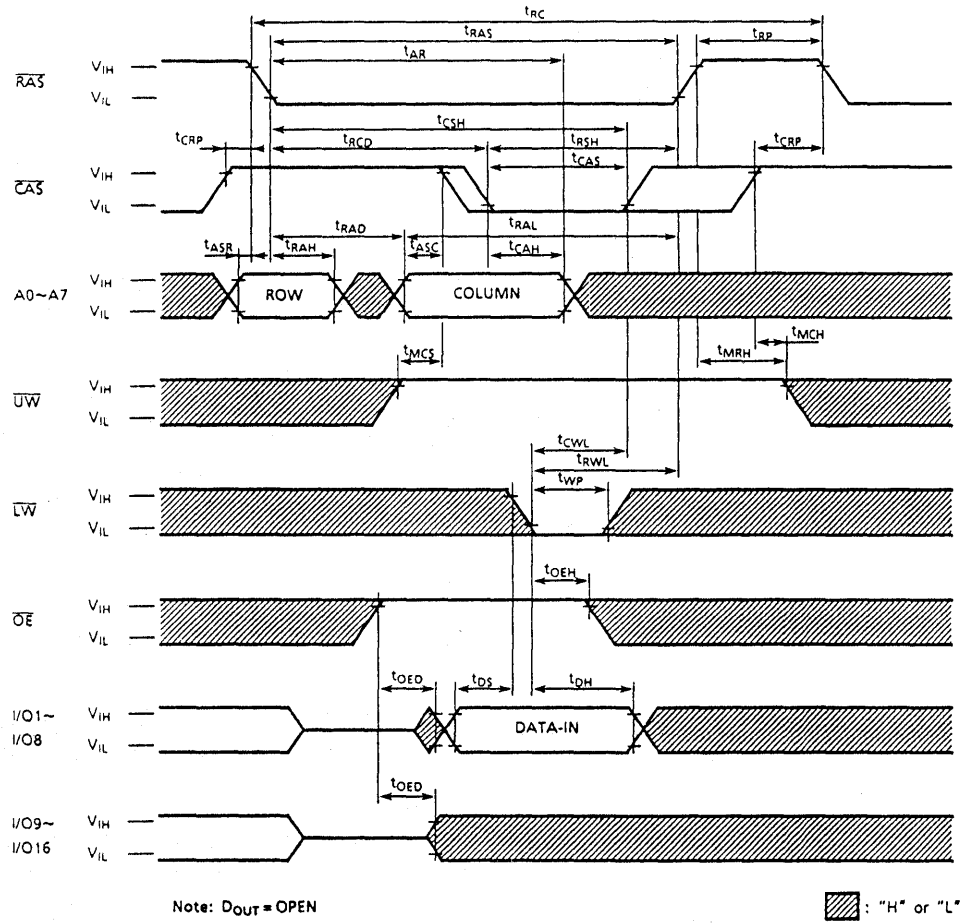
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

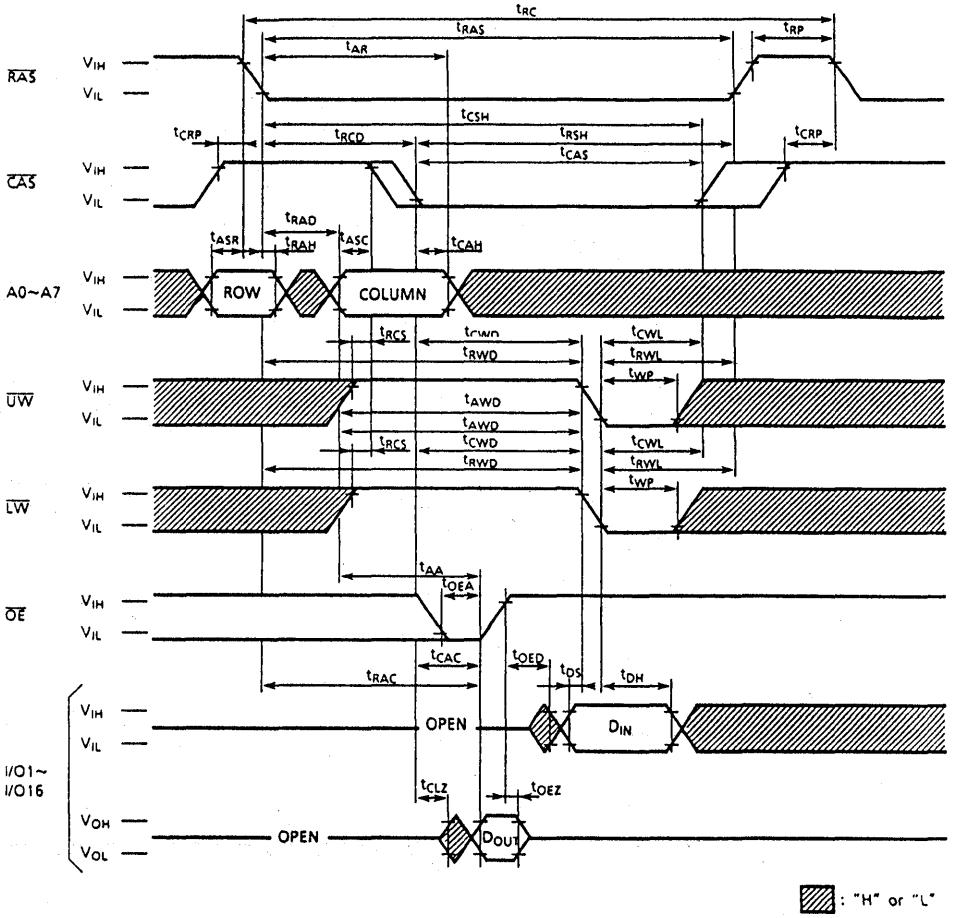
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



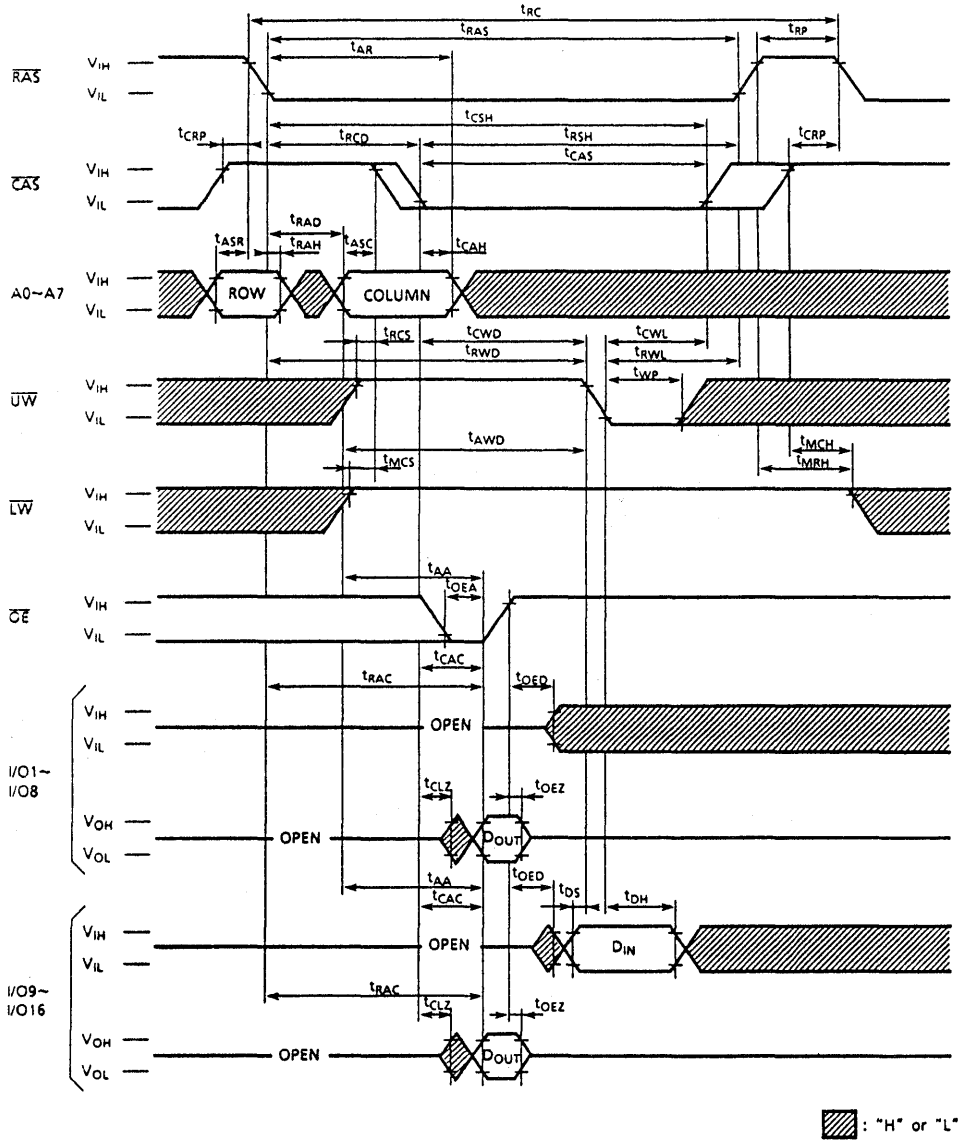
Note: D_{OUT} = OPEN

▨: "H" or "L"

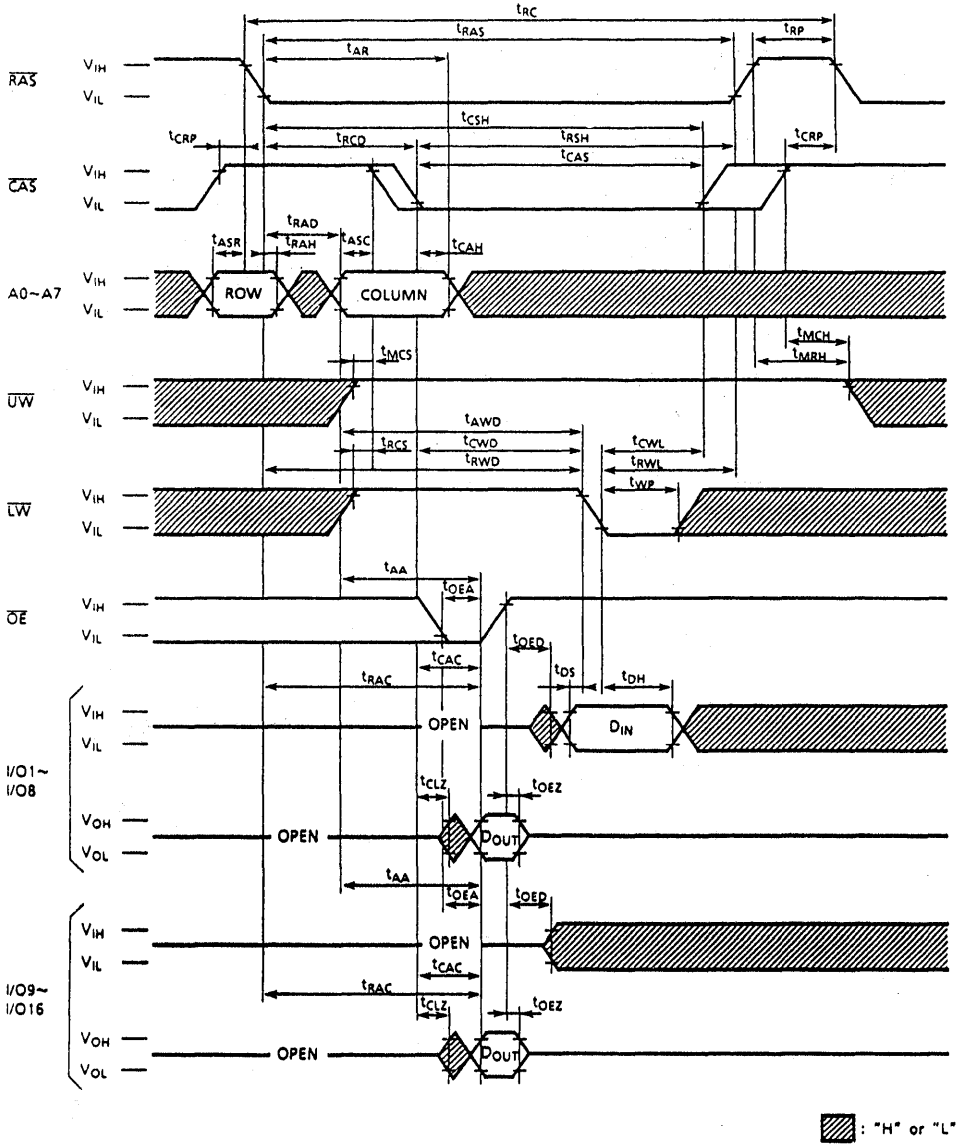
READ-MODIFY-WRITE CYCLE



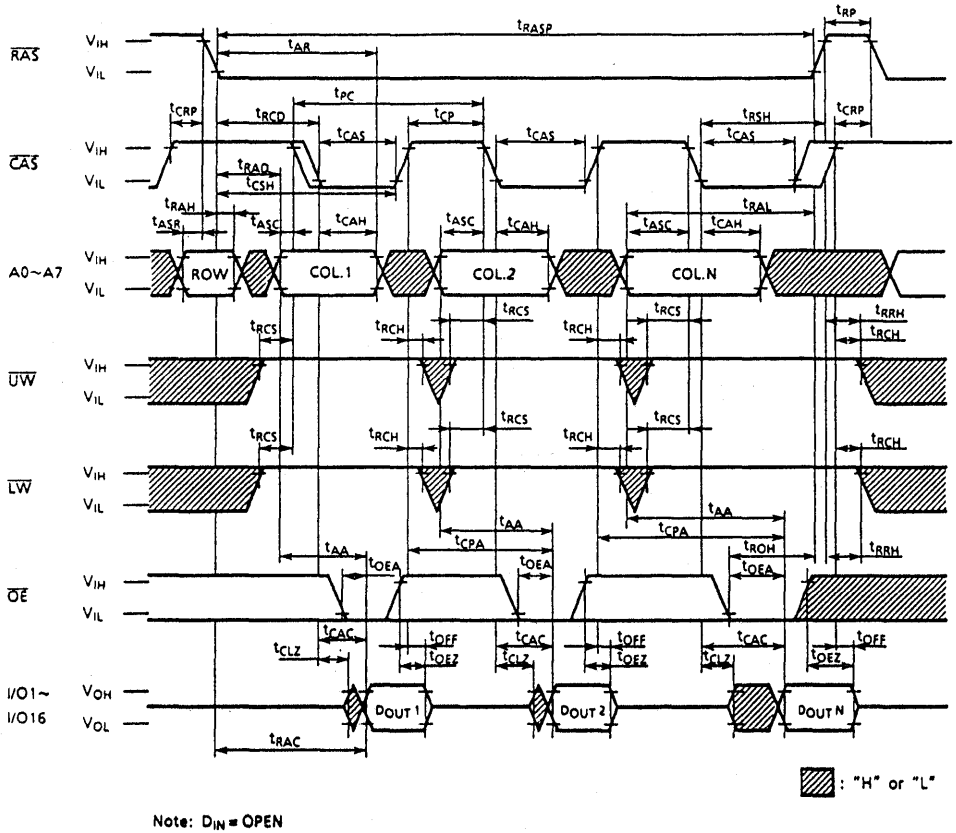
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE

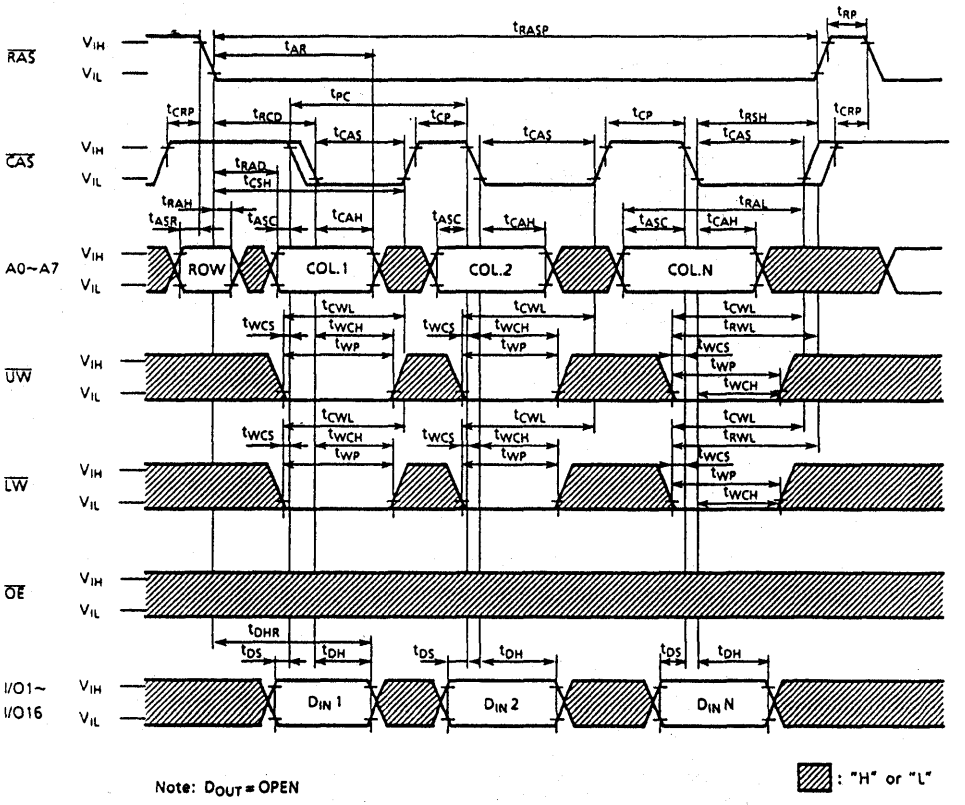


FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

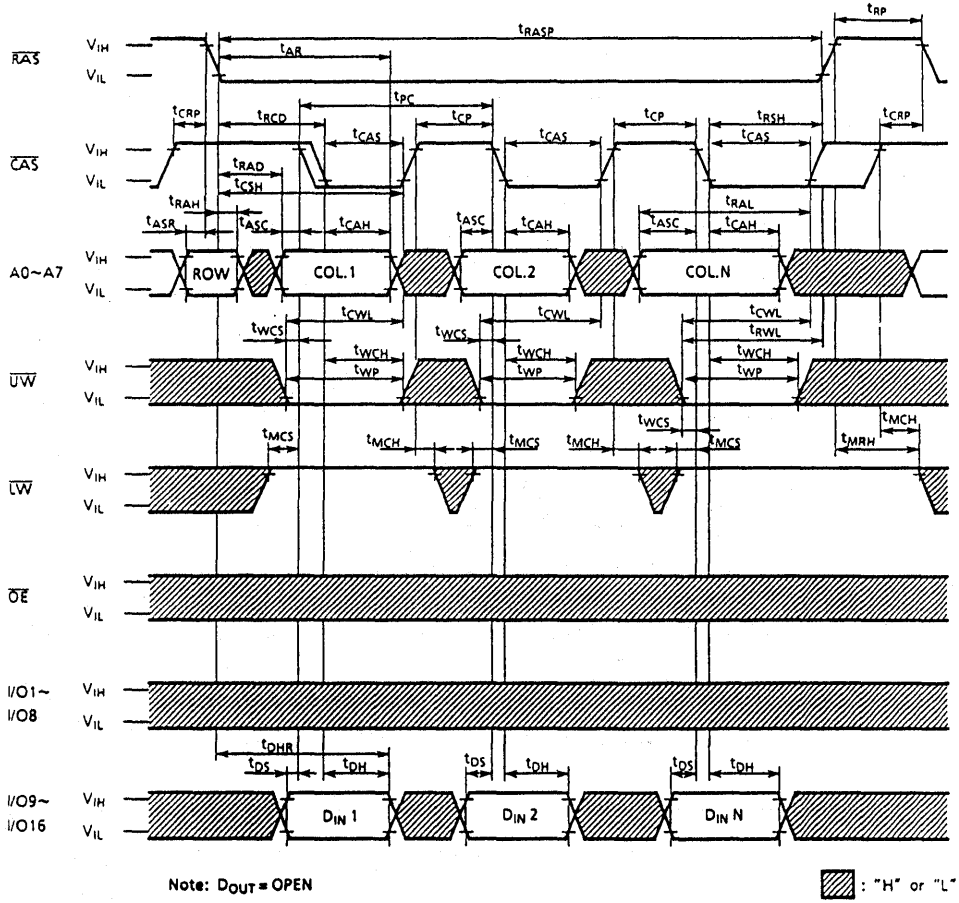
FAST PAGE MODE WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

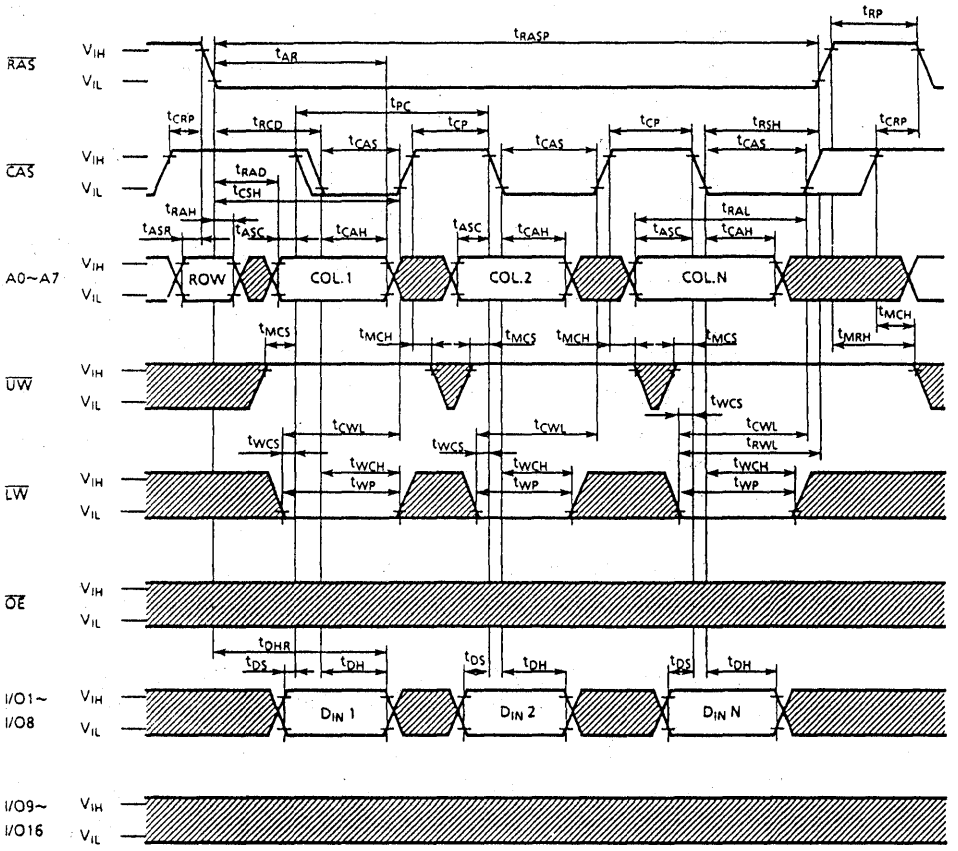
FAST PAGE MODE UPPER BYTE WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

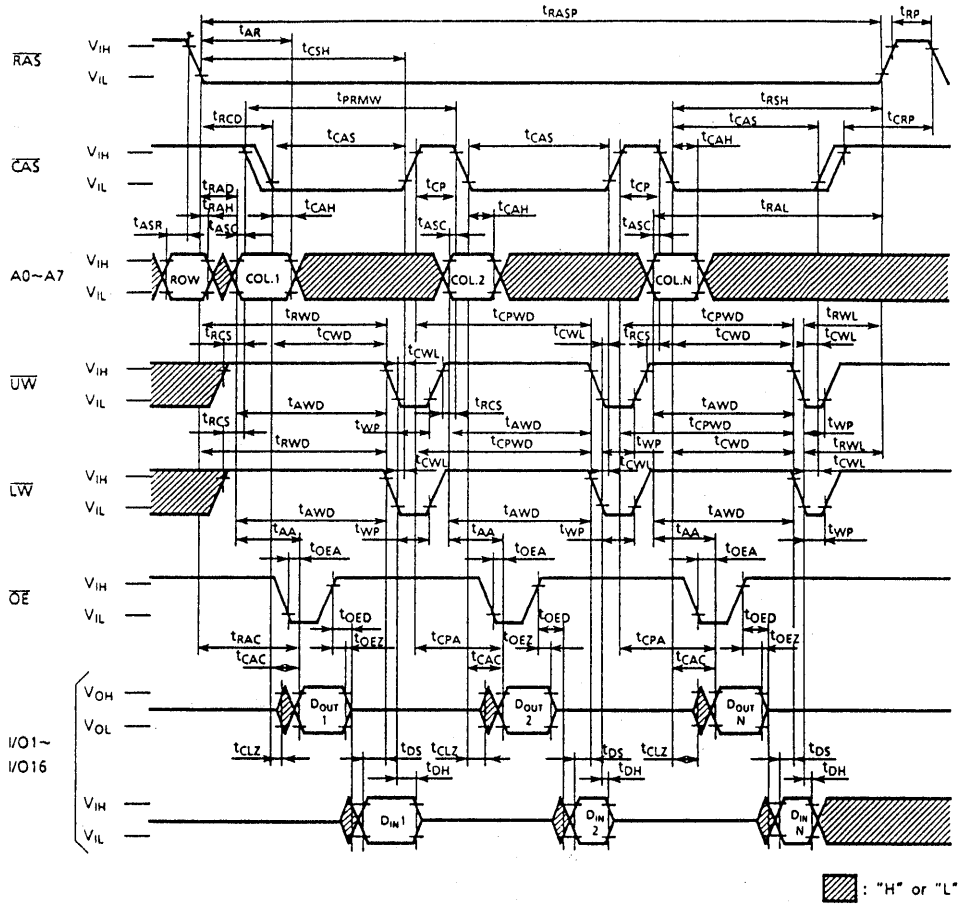
FAST PAGE MODE LOWER BYTE WRITE CYCLE



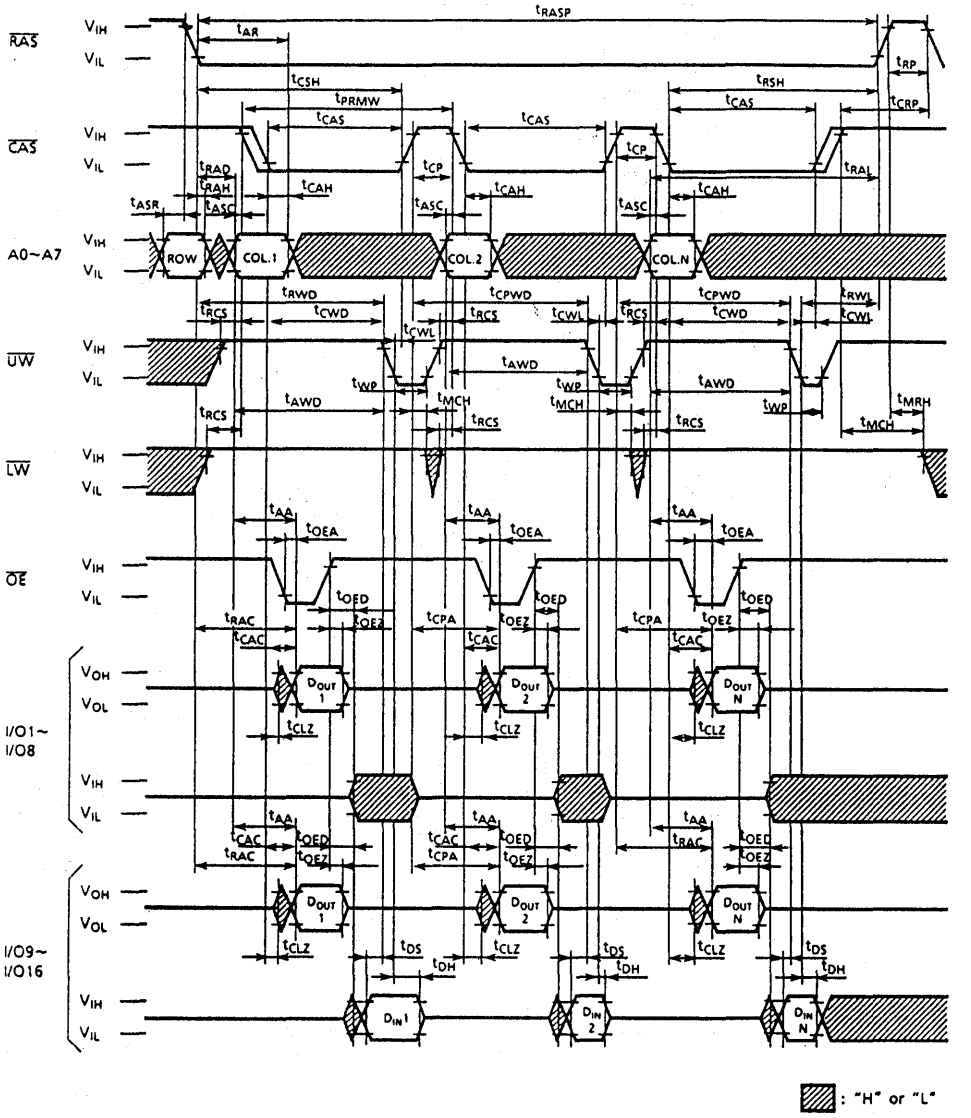
Note: D_{OUT} = OPEN

▨ : "H" or "L"

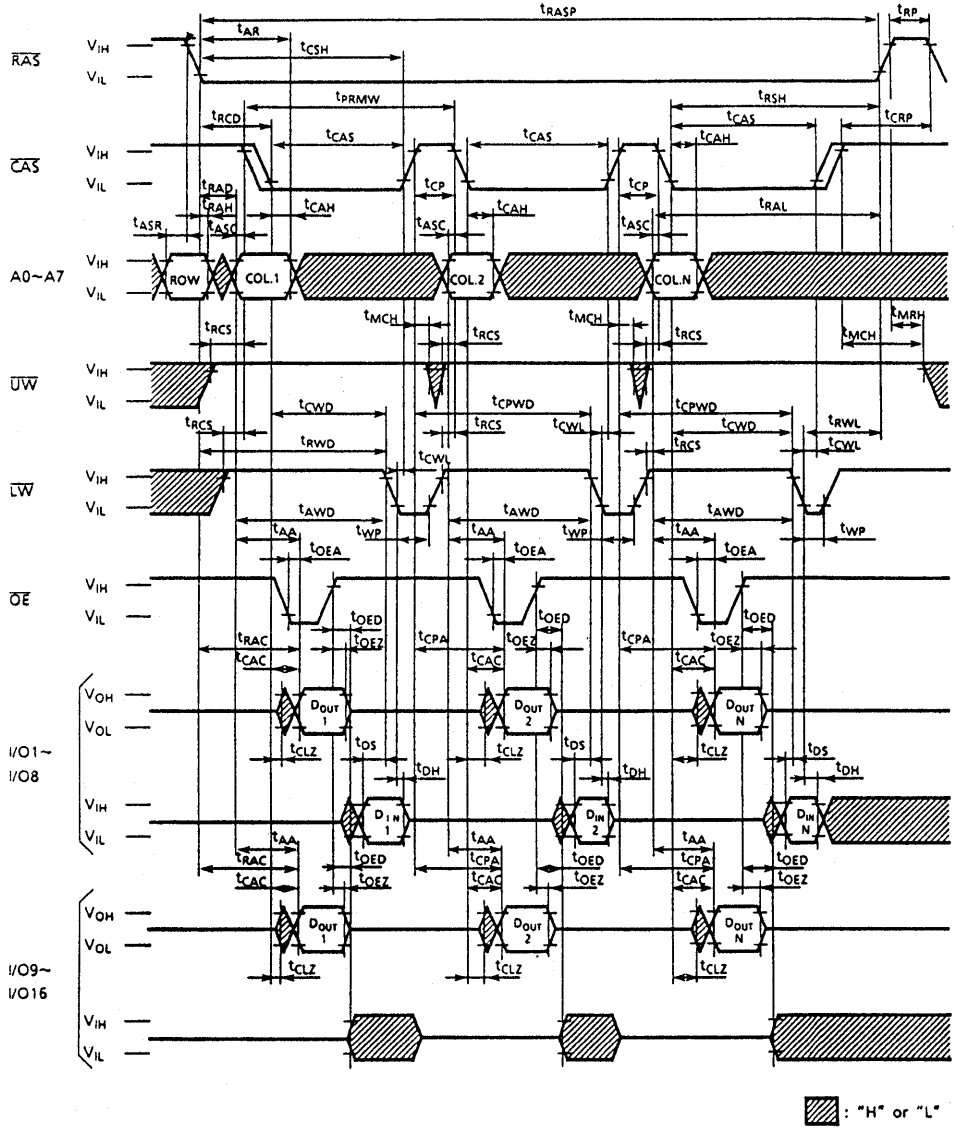
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



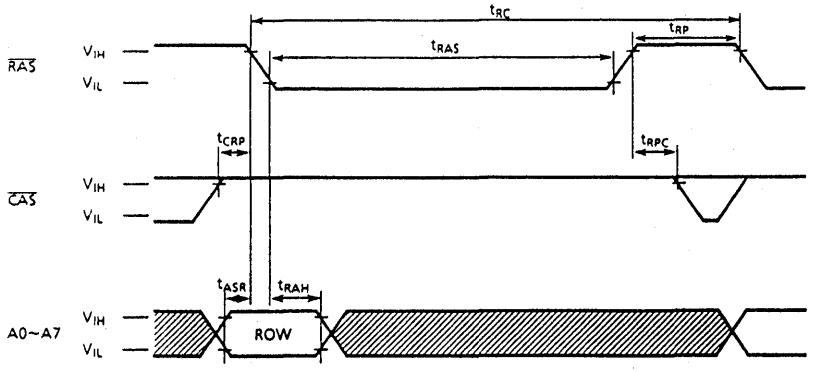
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



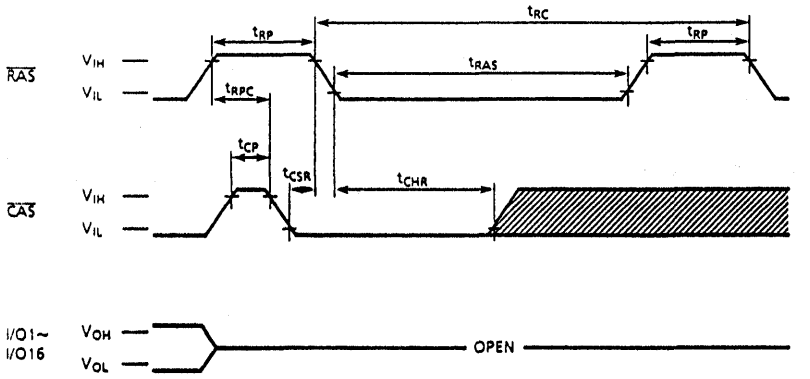
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

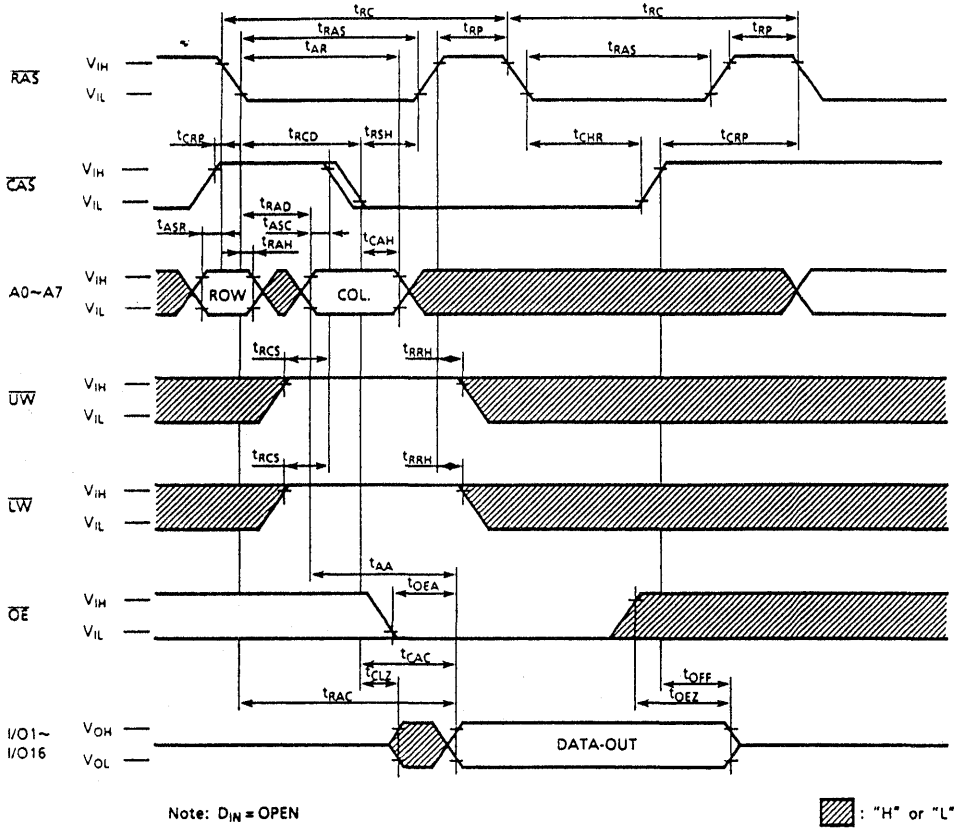
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0~A7 = "H" or "L"

▨ : "H" or "L"

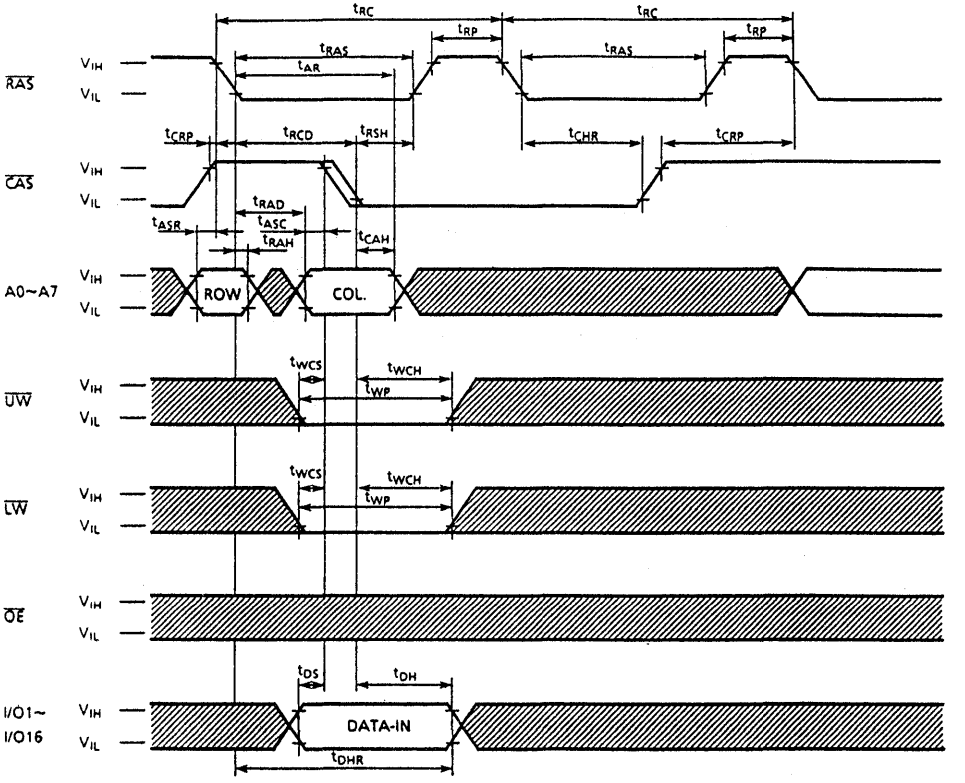
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

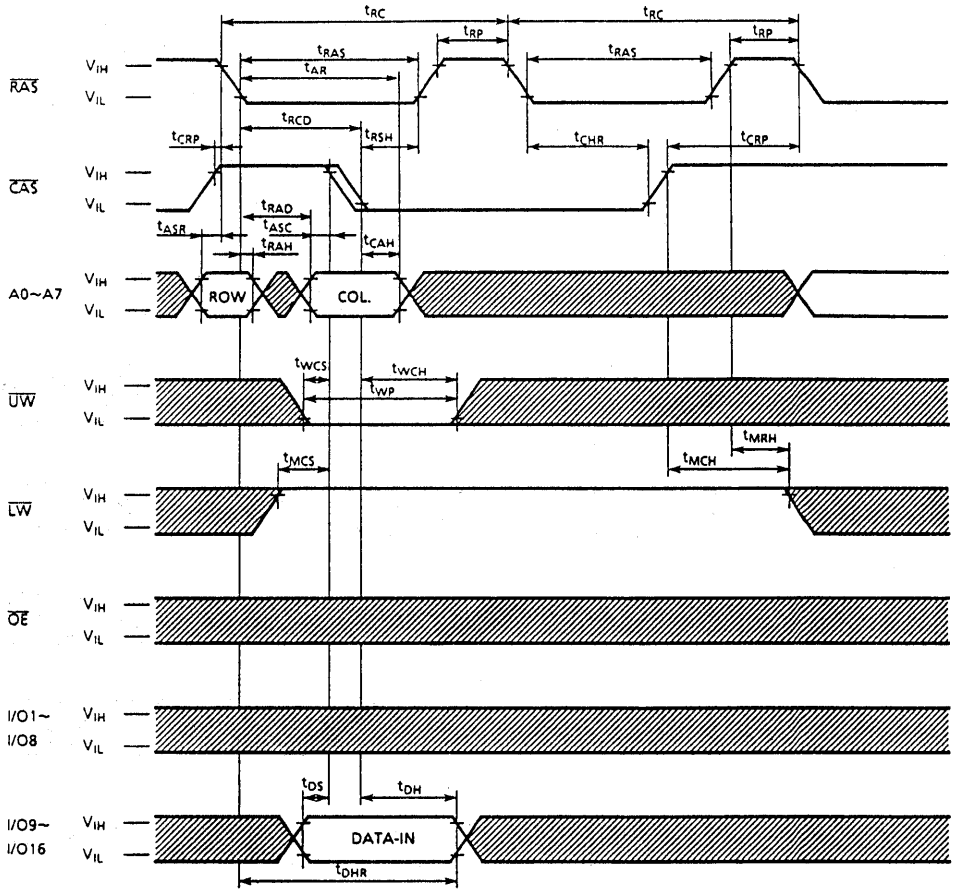
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

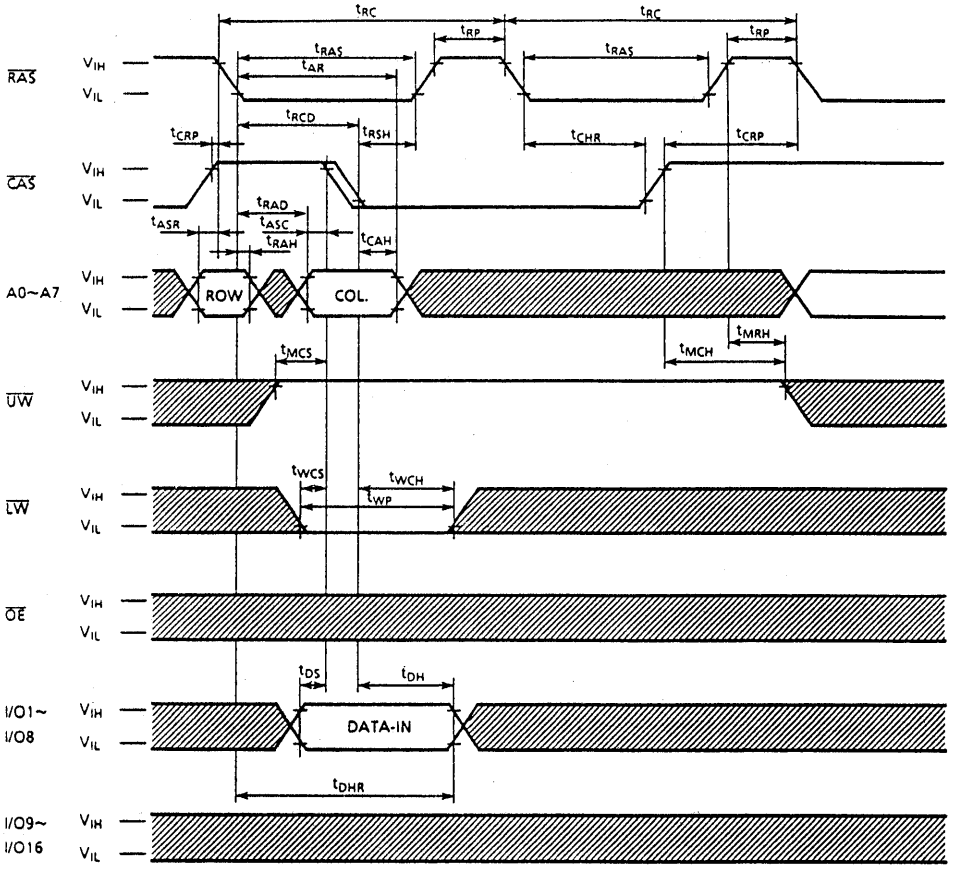
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

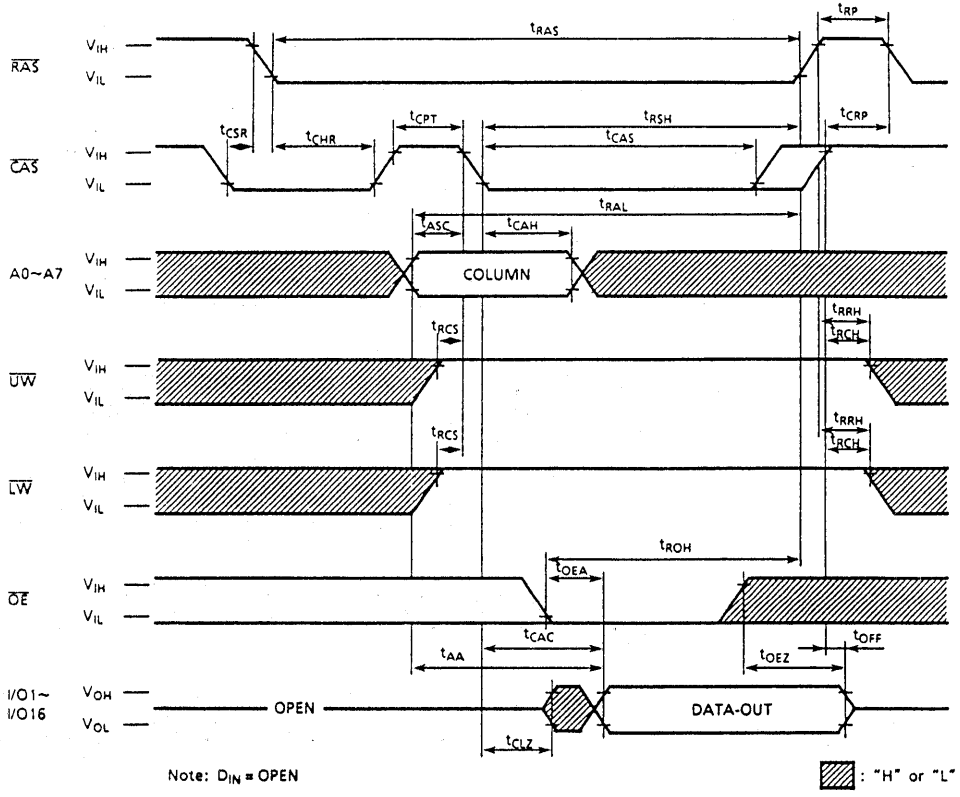
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



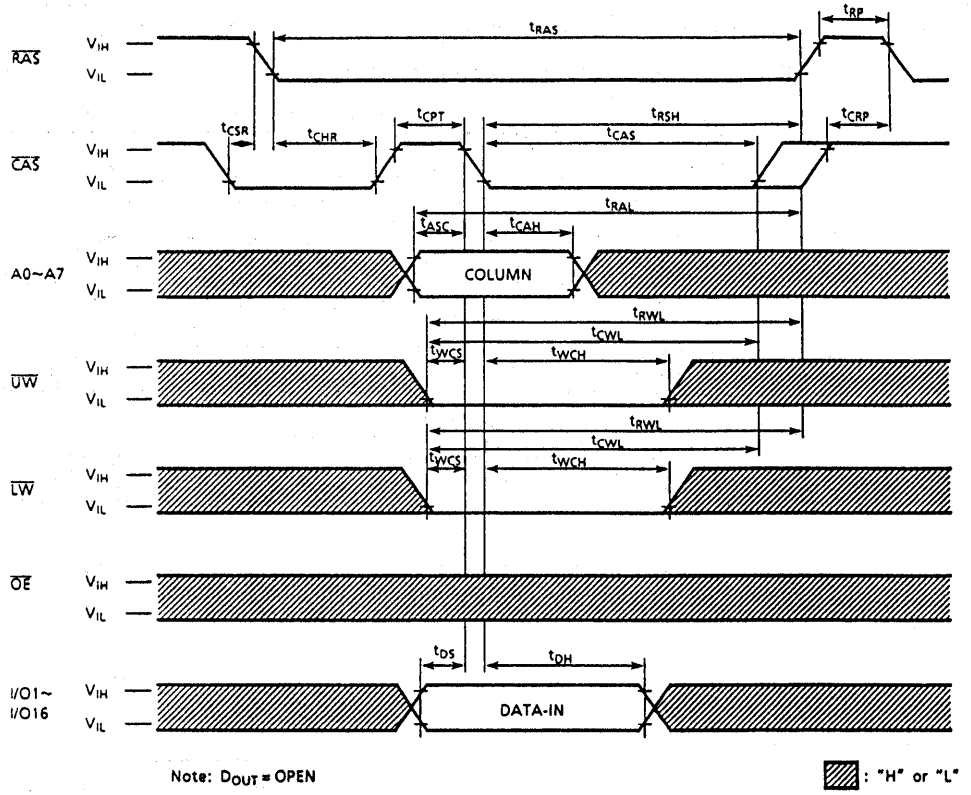
Note: D_{OUT} = OPEN

▨ : "H" or "L"

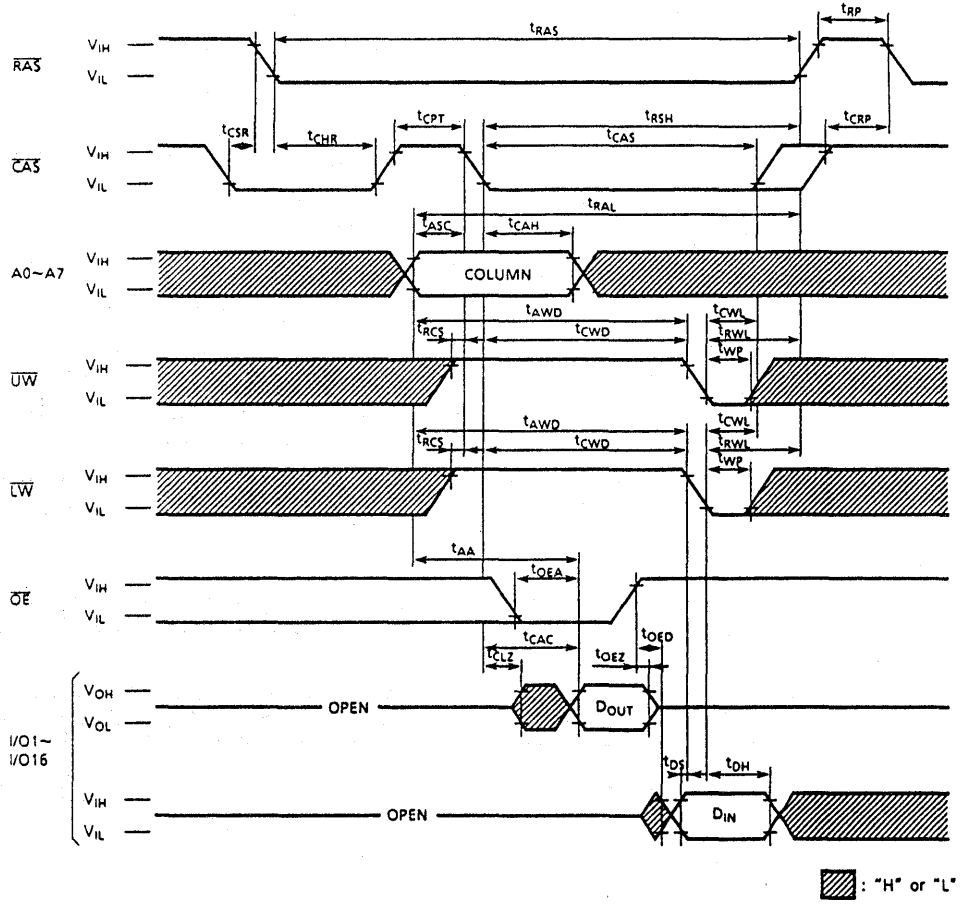
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511664J/Z are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{UW}$ and $\overline{LW}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{LW}$ strobes data on I/O1~I/O8 into the on-chip data latch. And the falling edge of $\overline{CAS}$ or $\overline{UW}$ strobes data on I/O9~I/16 into the on-chip data latch. In an early write cycle, $\overline{LW}$ and $\overline{UW}$ are brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In derayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{LW}$ and $\overline{UW}$ with setup and hold times referenced to these signals.

In derayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high inpedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

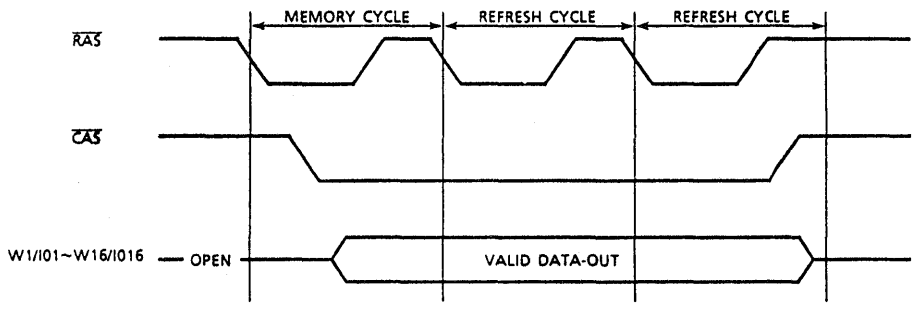
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511664J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511664J/Z allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511664J/Z is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511664J/Z can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

65,536 WORD × 16 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC511664JL/ZL is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511664JL/ZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511664JL/ZL to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

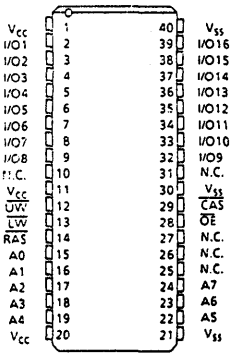
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511664JL/ZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	40ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

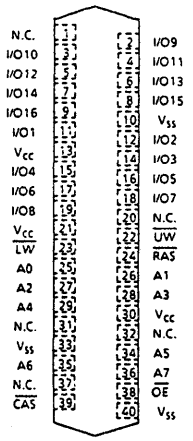
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511664JL/ZL-80)
  495mW MAX. Operating (TC511664JL/ZL-10)
  1.7mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Byte-Write and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/32ms
- Package Plastic SOJ : TC511664JL
  Plastic ZIP : TC511664ZL

PIN CONNECTION (TOP VIEW)

Plastic SOJ



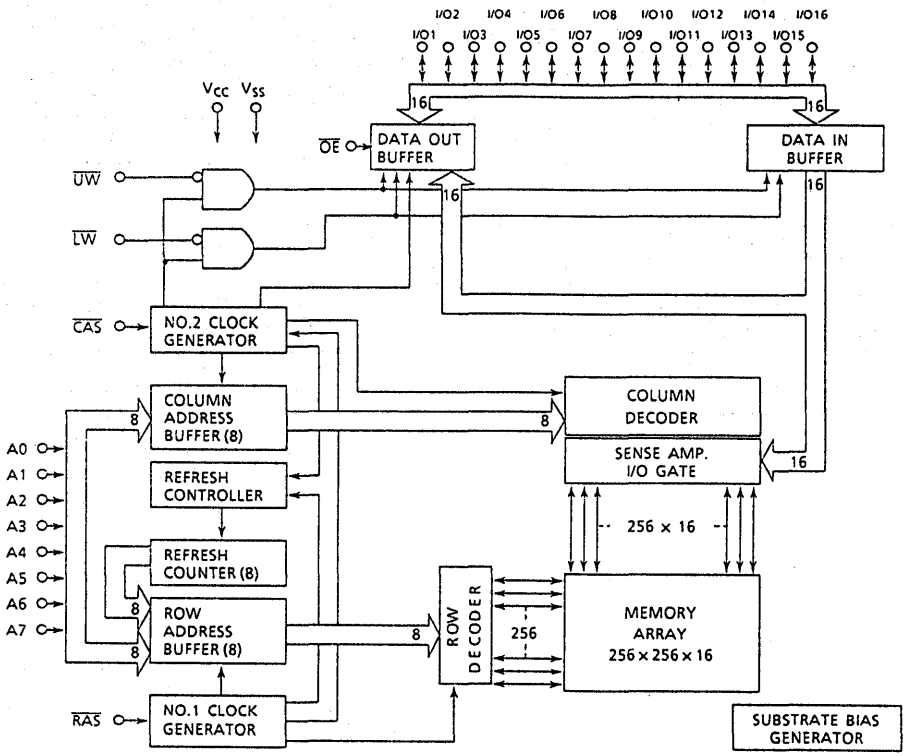
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Colomn Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Ouput Enable
I/O01~I/O16	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage ($A0\sim A7$, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (I/O1~I/O16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511664JL/ZL-80	–	115	mA	3, 4, 5
		TC511664JL/ZL-10	–	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511664JL/ZL-80	–	115	mA	3, 5
		TC511664JL/ZL-10	–	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511664JL/ZL-80	–	70	mA	3, 4, 5
		TC511664JL/ZL-10	–	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	300	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511664JL/ZL-80	–	115	mA	3
		TC511664JL/ZL-10	–	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{UW}$,$\overline{LW}$ = V_{CC} – 0.2V or 0.2V, A0~A7 = V_{CC} – 0.2V or 0.2V, I/O1~16 = V_{CC} – 0.2V,0.2V or OPEN: t_{RC} = 125μs, t_{RAS} = t_{RAS} MIN.~1μs)		–	400	μA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2.5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC511664JL/ZL-80		TC511664JL/ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	–	35	–	40	ns	10,15
t_{AA}	Access Time from Column Address	–	45	–	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35	–	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	ns	13

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511664JL/ZL-80		TC511664JL/ZL-10		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	32	–	32	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	70	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Trun Off Delay Time from $\overline{OE}$	0	10	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{MCS}	Masked Write Set-Up Time	0	–	0	–	ns	
t_{MRH}	Masked Write Hold time Referenced to $\overline{RAS}$	0	–	0	–	ns	
t_{MCH}	Masked Write Hold time Referenced to $\overline{CAS}$	0	–	0	–	ns	

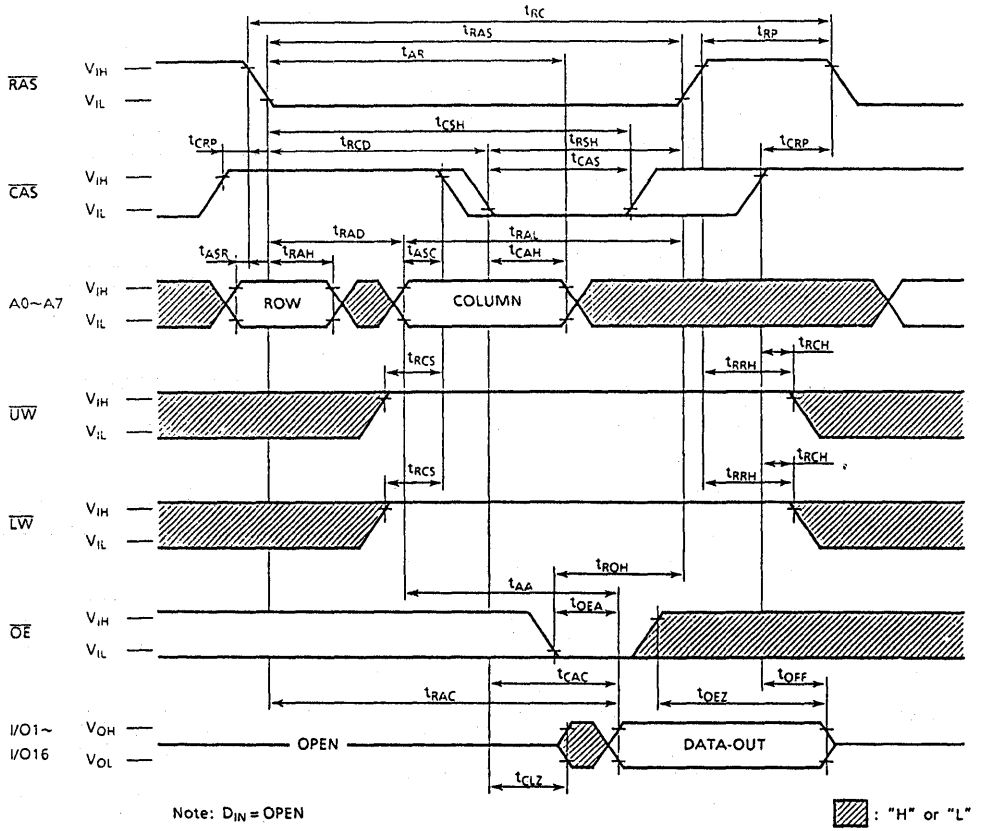
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A7)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	–	7	pF

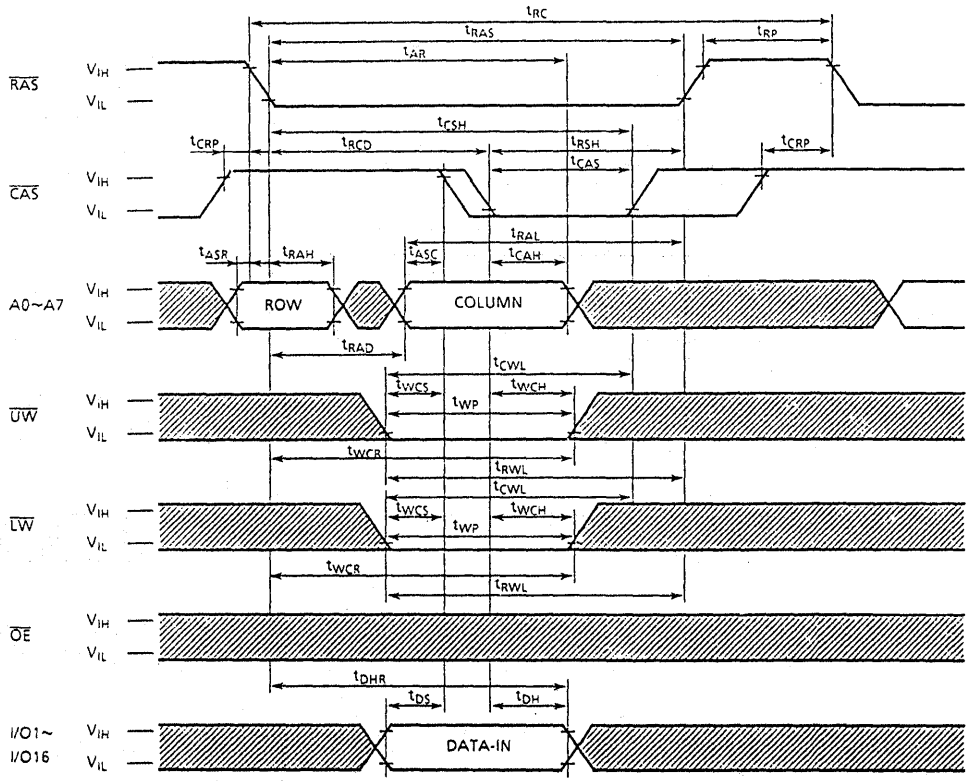
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T=5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 1 TTL load and 50pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{UW}$, $\overline{LW}$ leading edge in read-modify-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCAS
tCRP
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A7
ROW
COLUMN
tRCH
tRCS
tRRH
UW
LW
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1~
I/O16
VOH
VOL
OPEN
DATA-OUT
tCLZ
Note: DIN = OPEN
: "H" or "L"

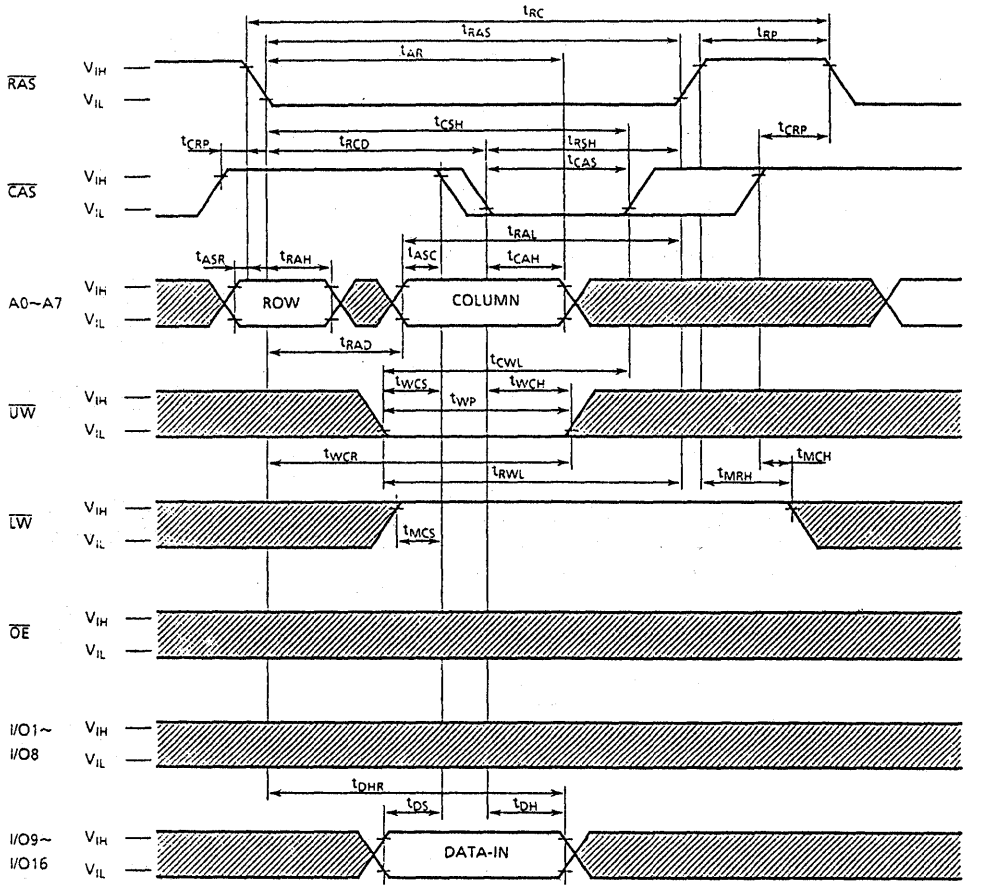
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

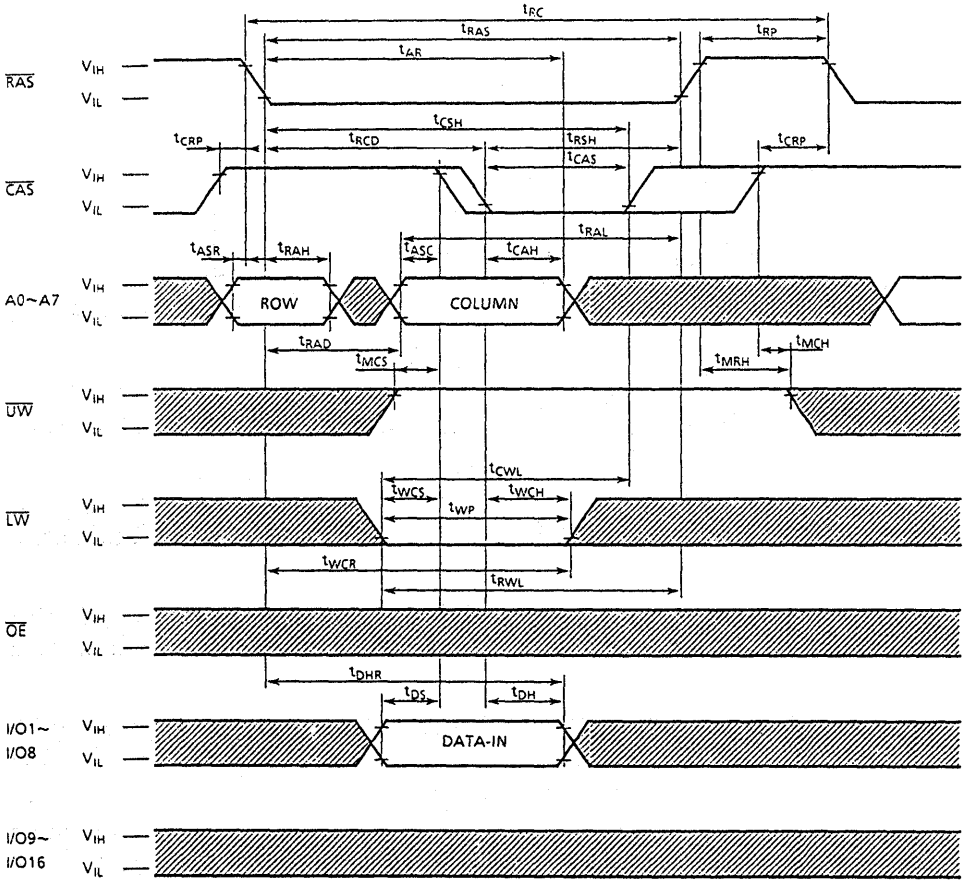
UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

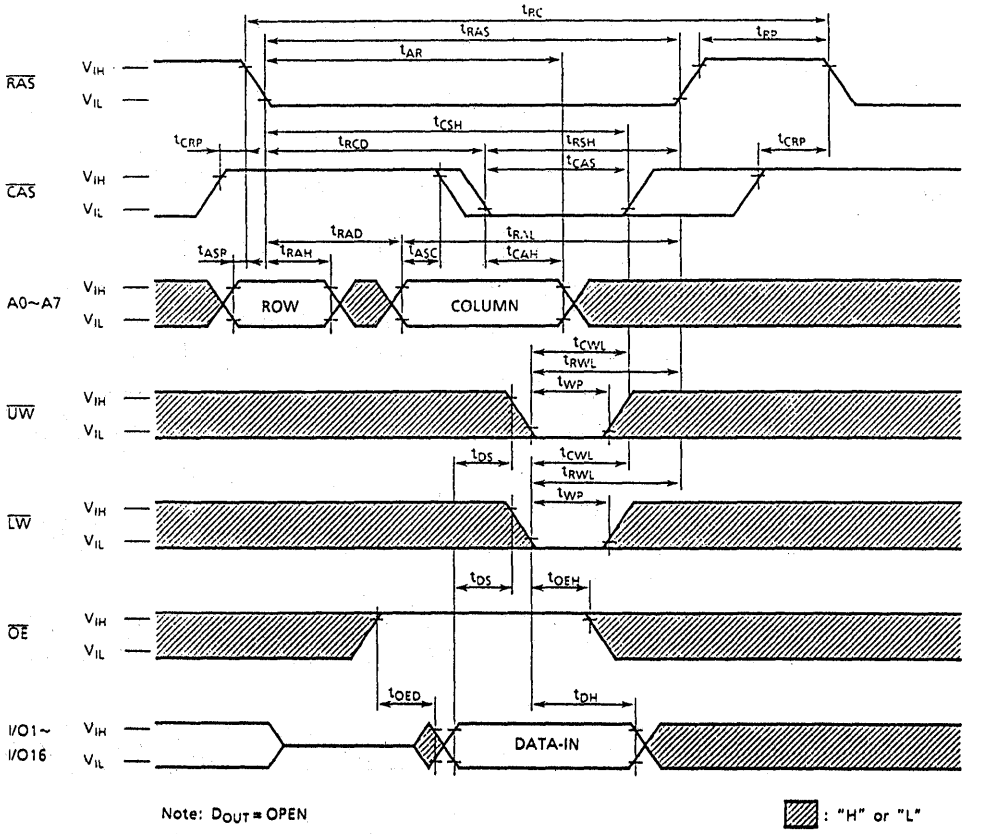
LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

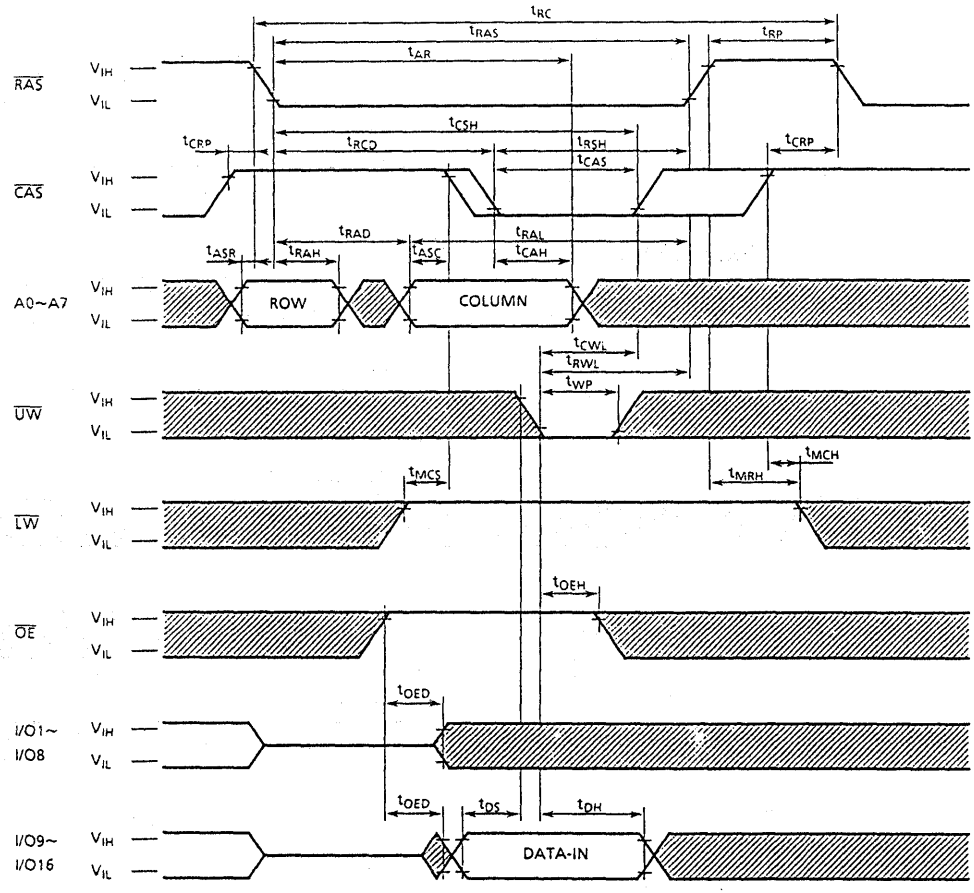
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

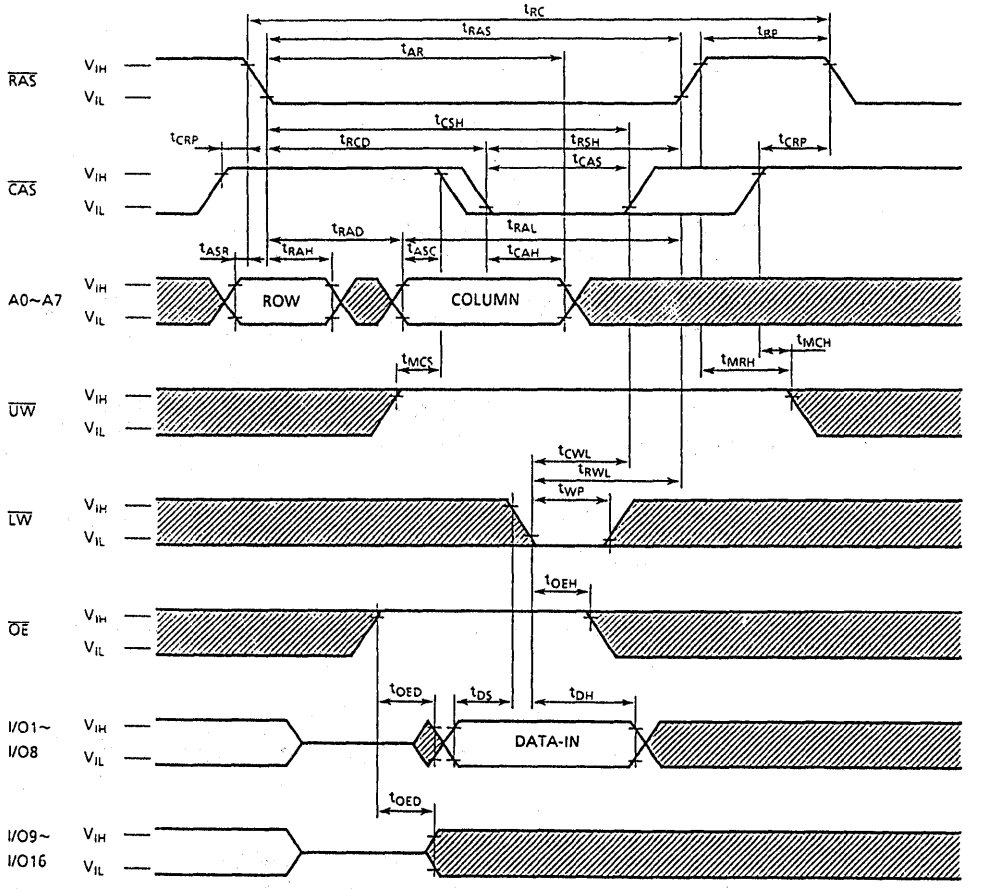
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

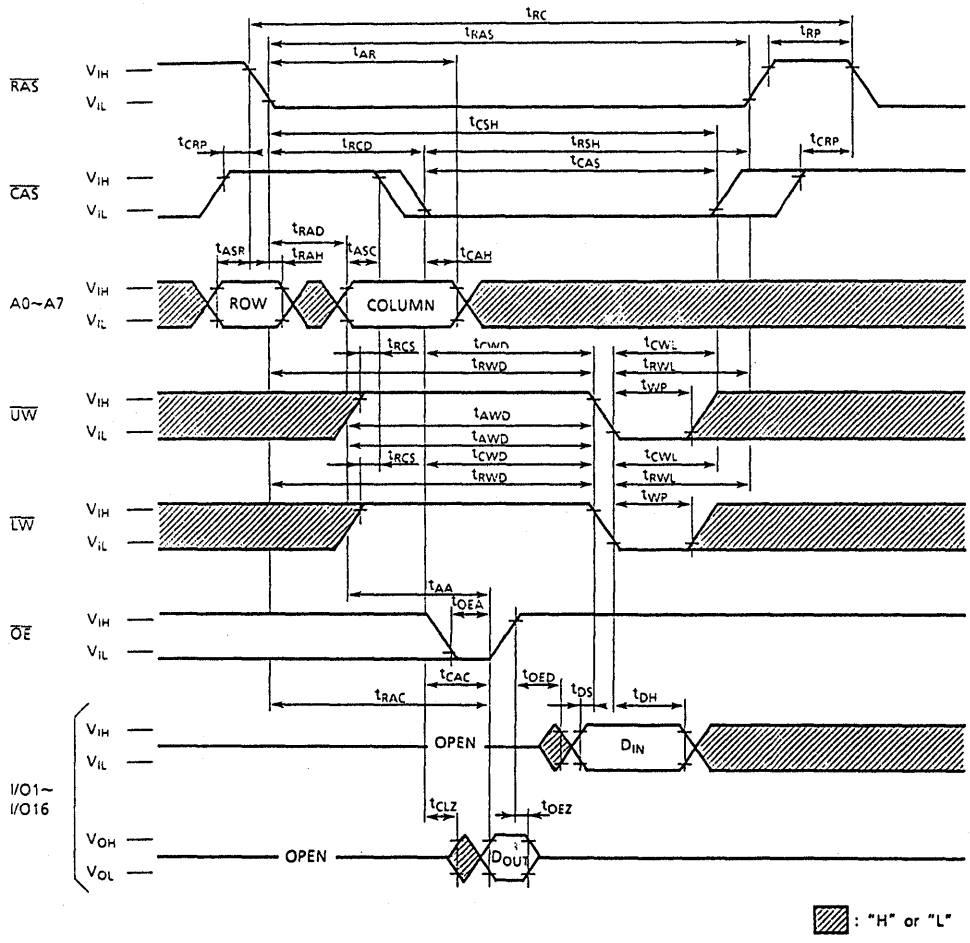
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



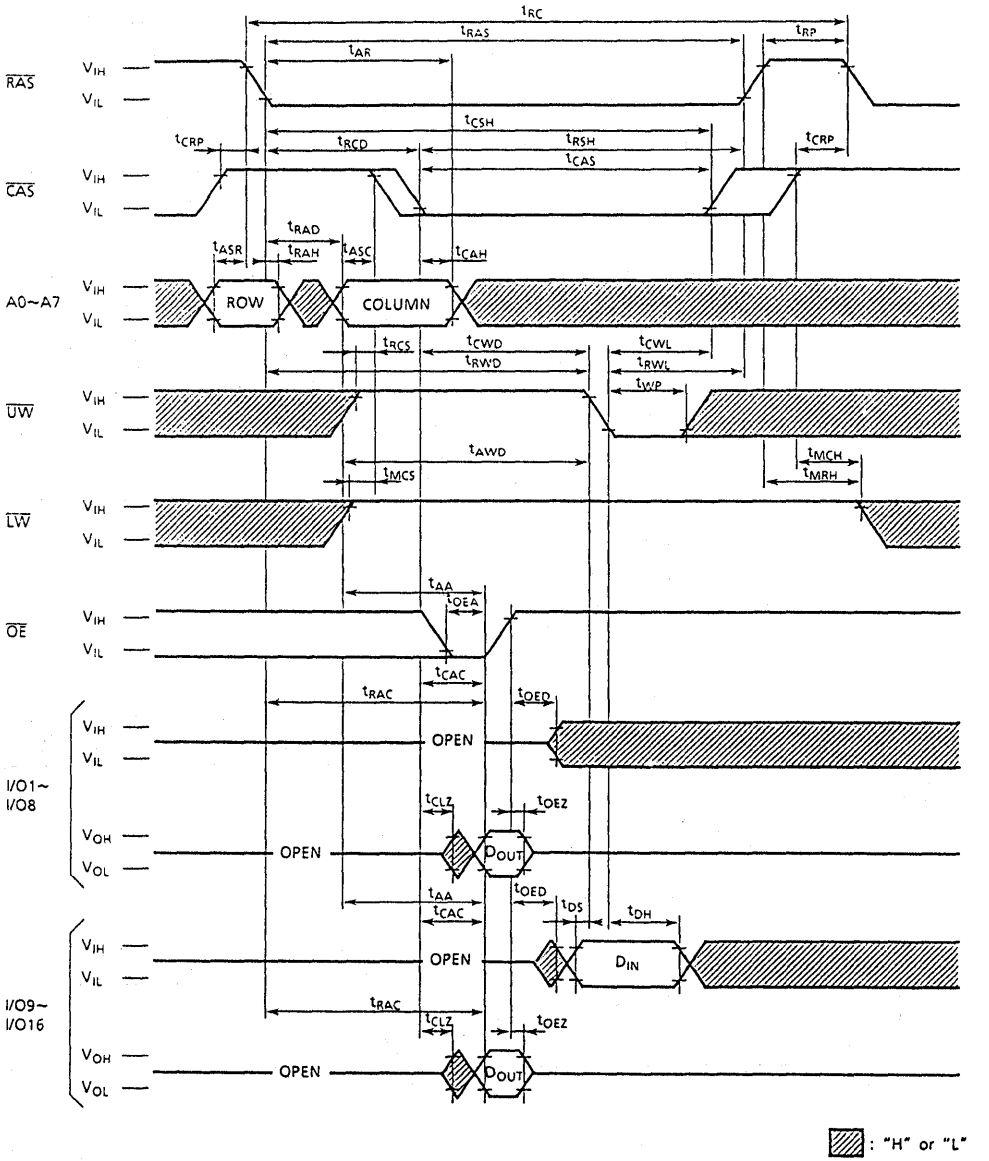
Note: D_{OUT} = OPEN

▨ : "H" or "L"

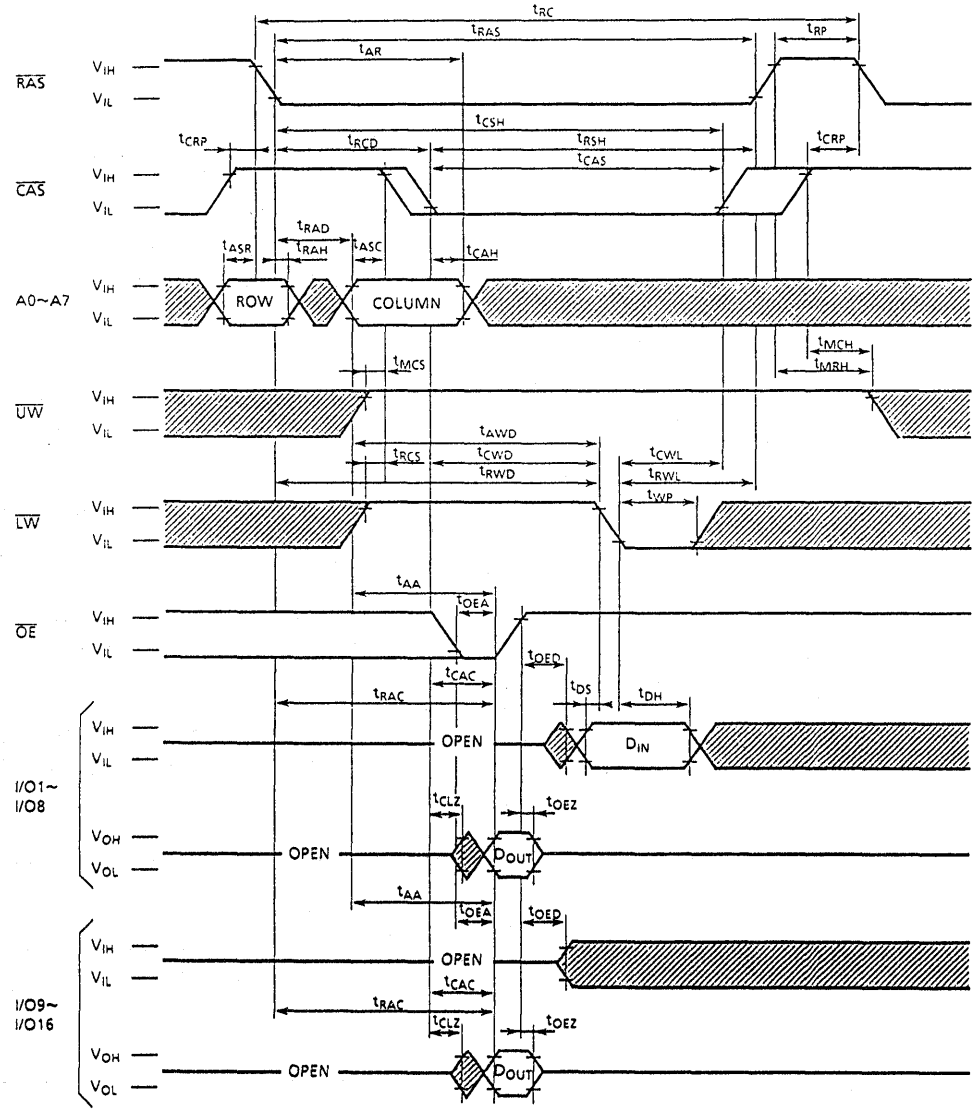
READ-MODIFY-WRITE CYCLE



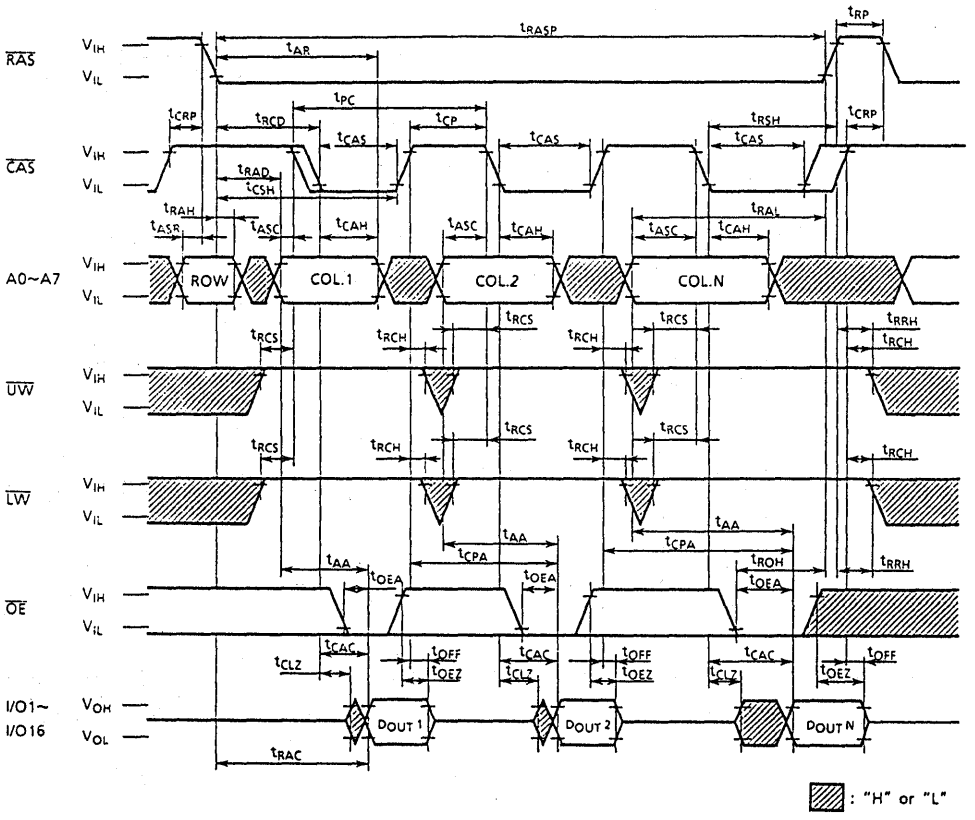
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE

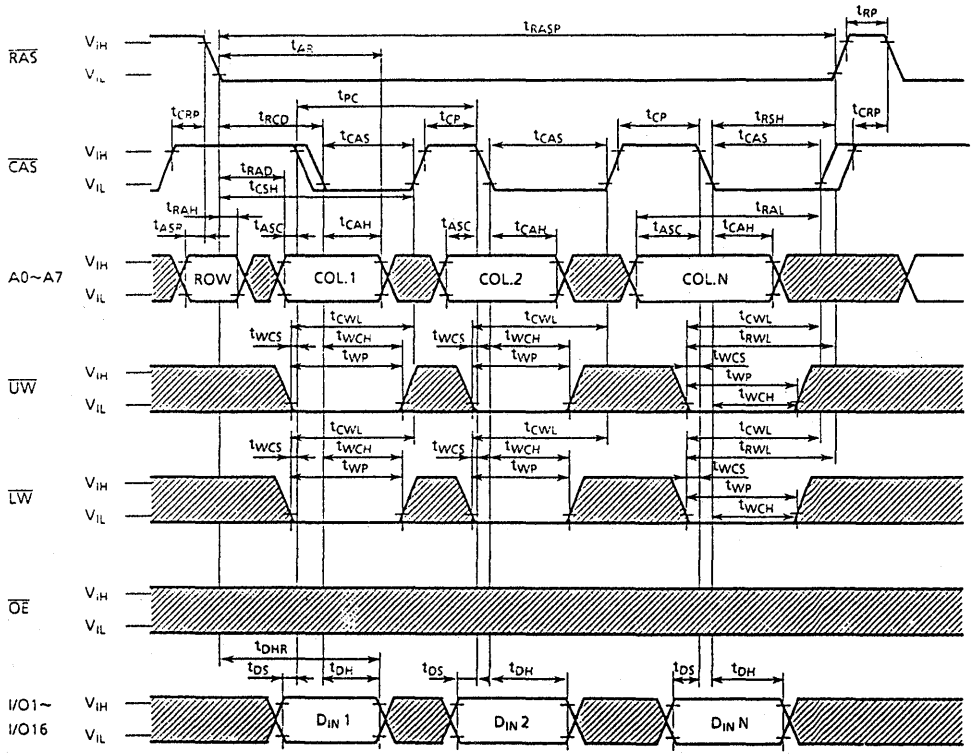


FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

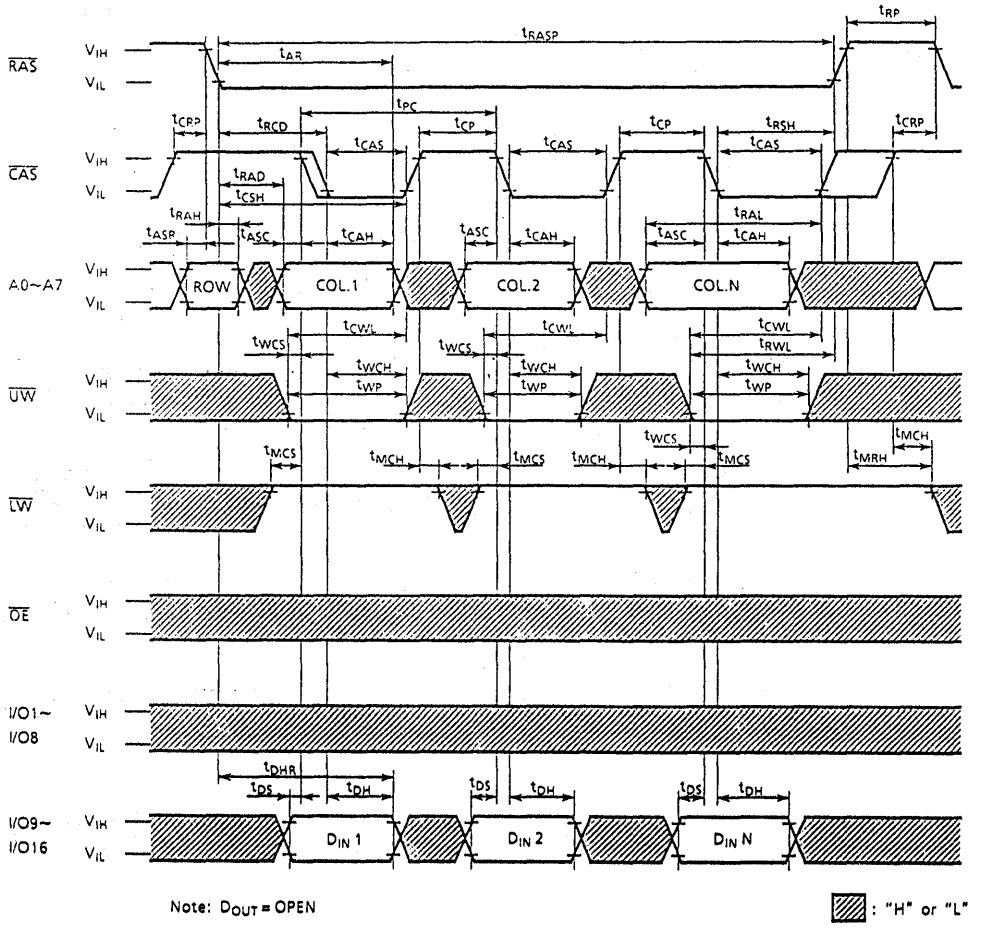
FAST PAGE MODE WRITE CYCLE



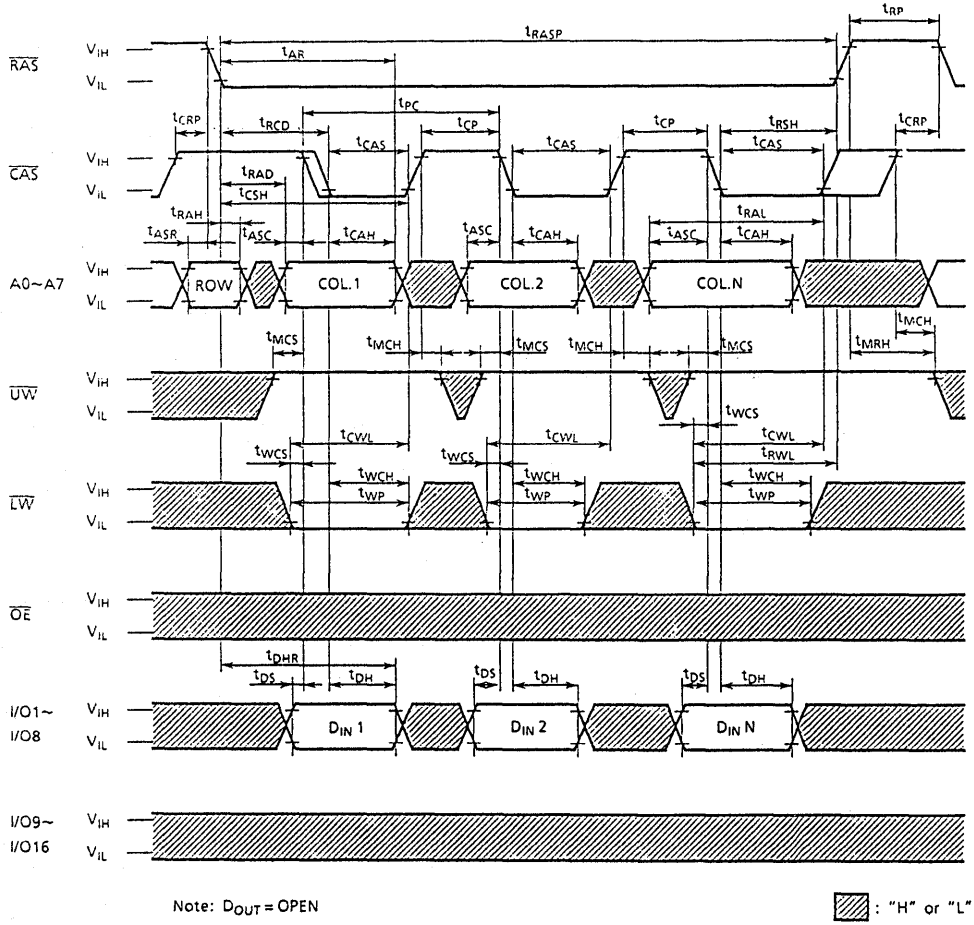
Note: D_{OUT} = OPEN

▨ : "H" or "L"

FAST PAGE MODE UPPER BYTE WRITE CYCLE



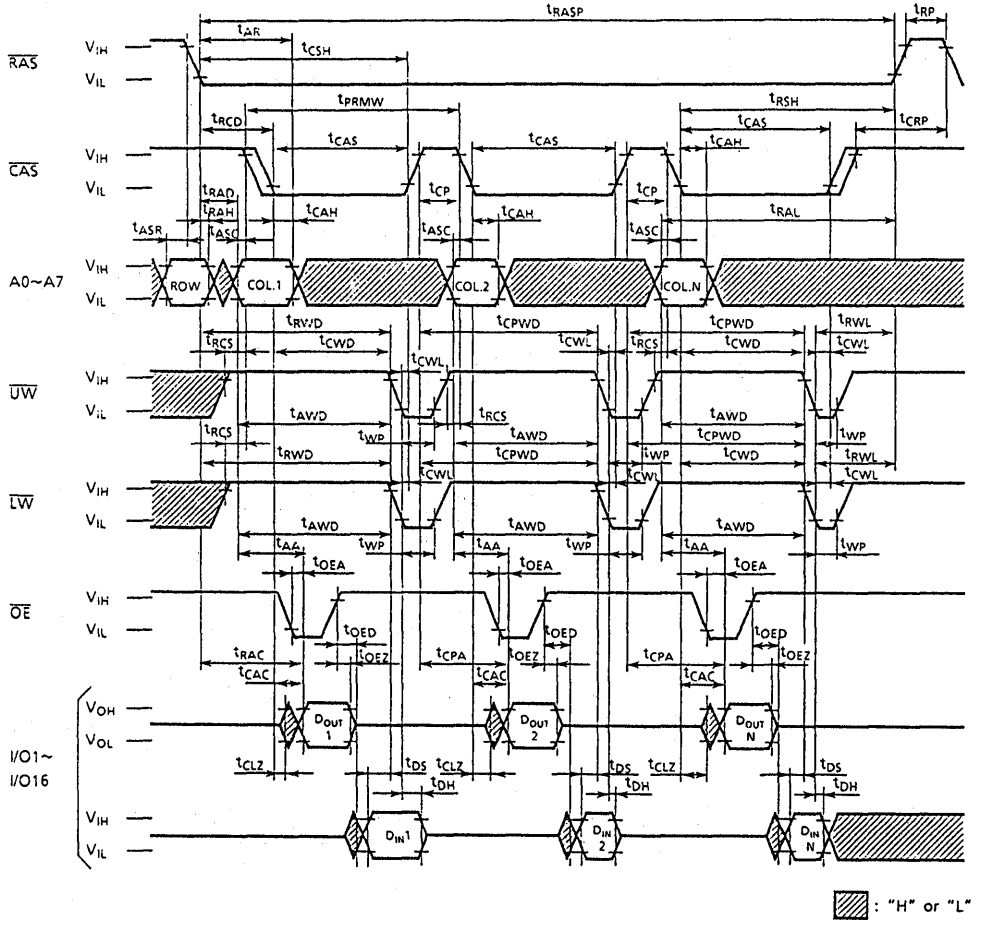
FAST PAGE MODE LOWER BYTE WRITE CYCLE



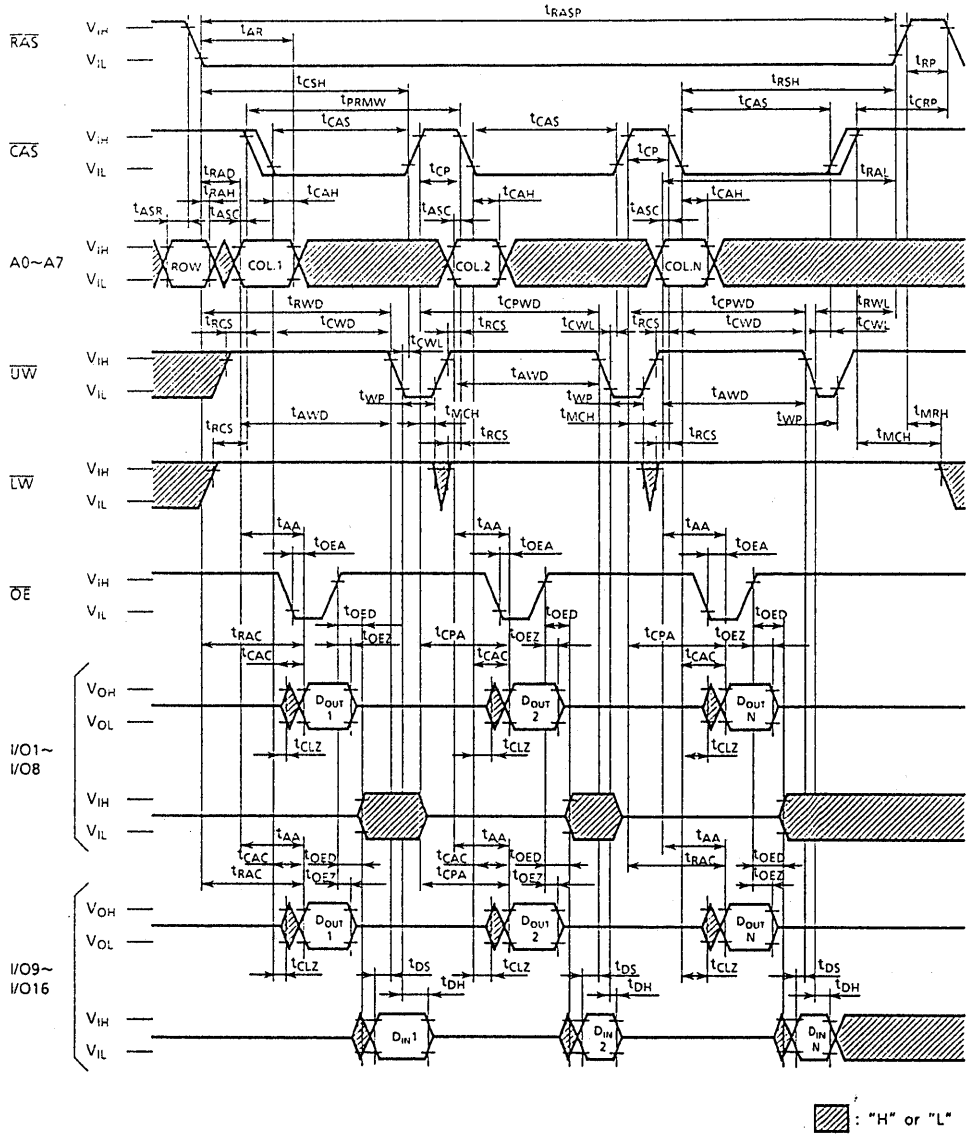
Note: D_{OUT} = OPEN

▨ : "H" or "L"

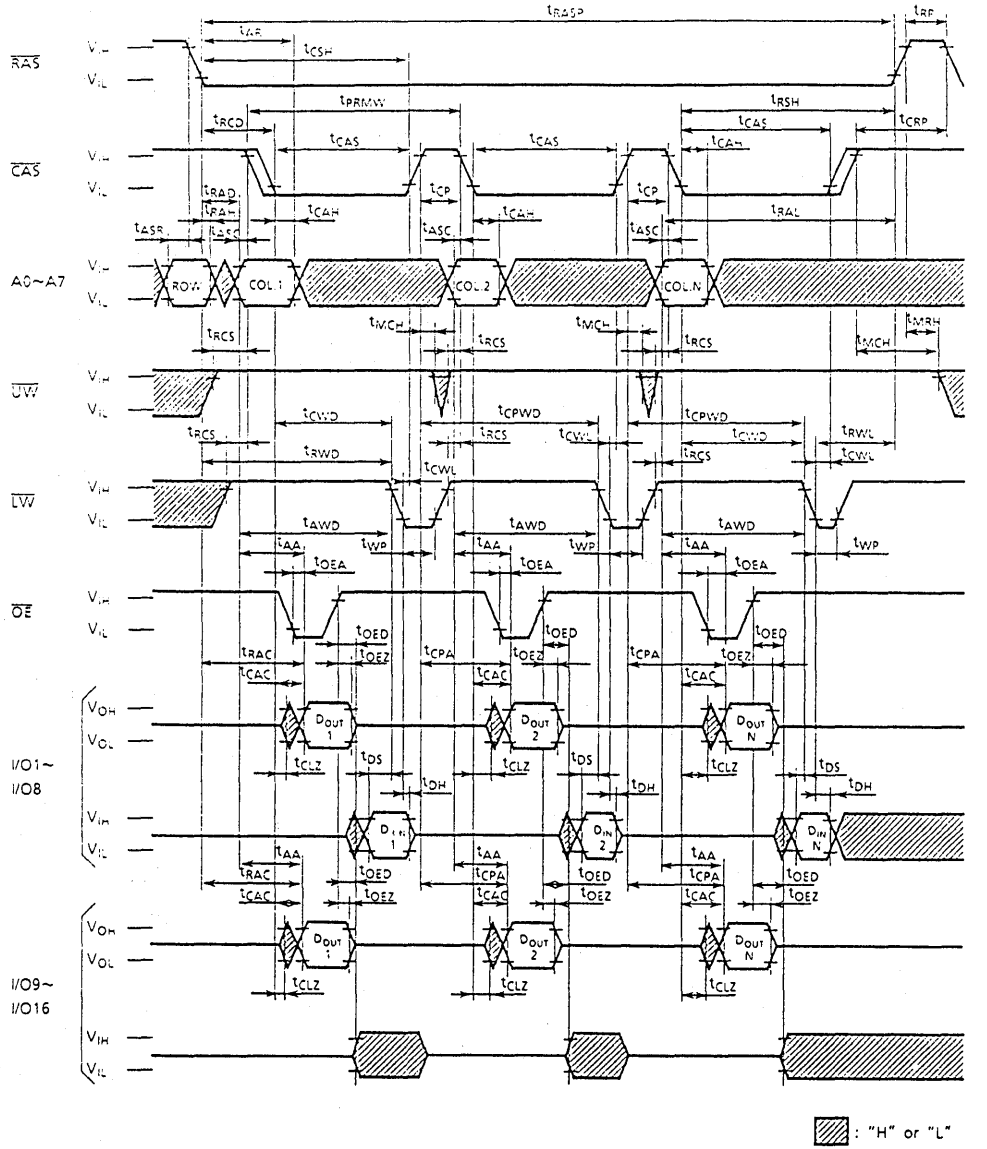
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



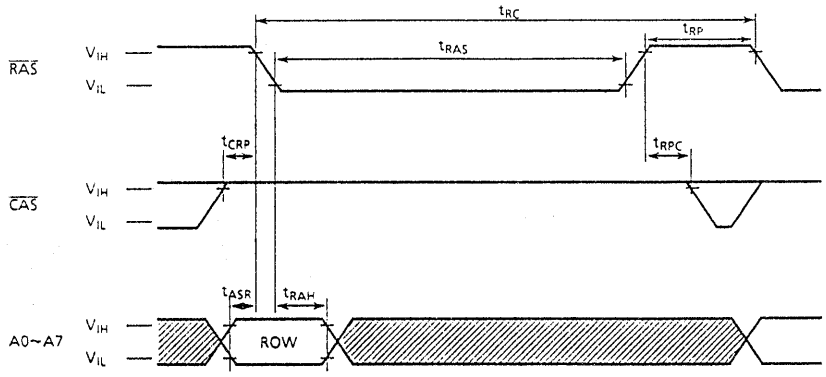
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



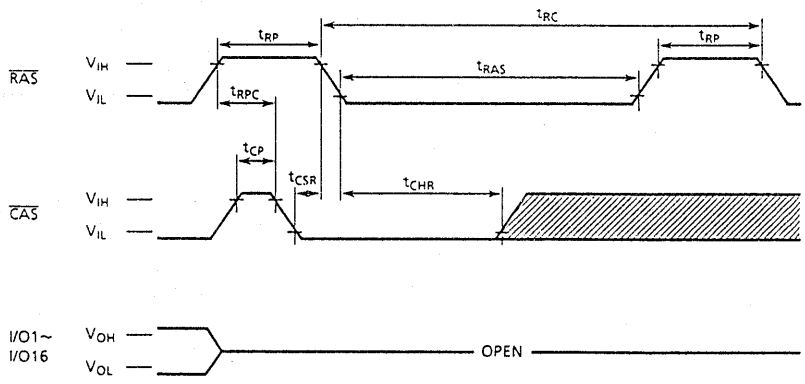
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

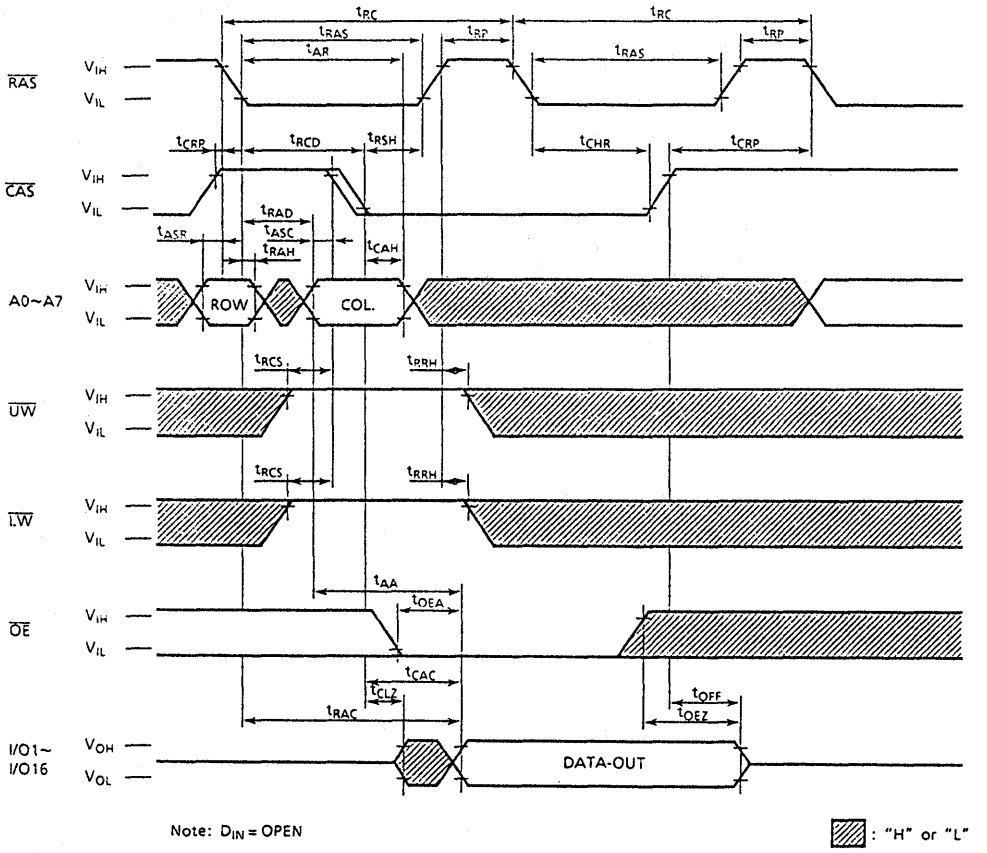
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0~A7 = "H" or "L"

▨ : "H" or "L"

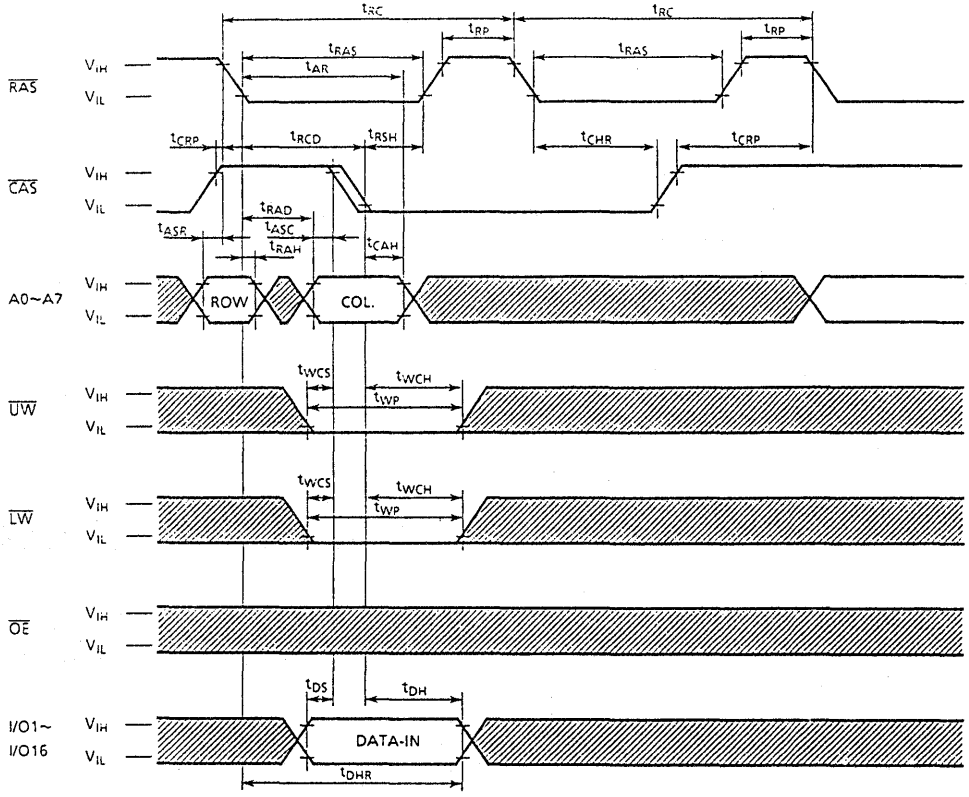
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

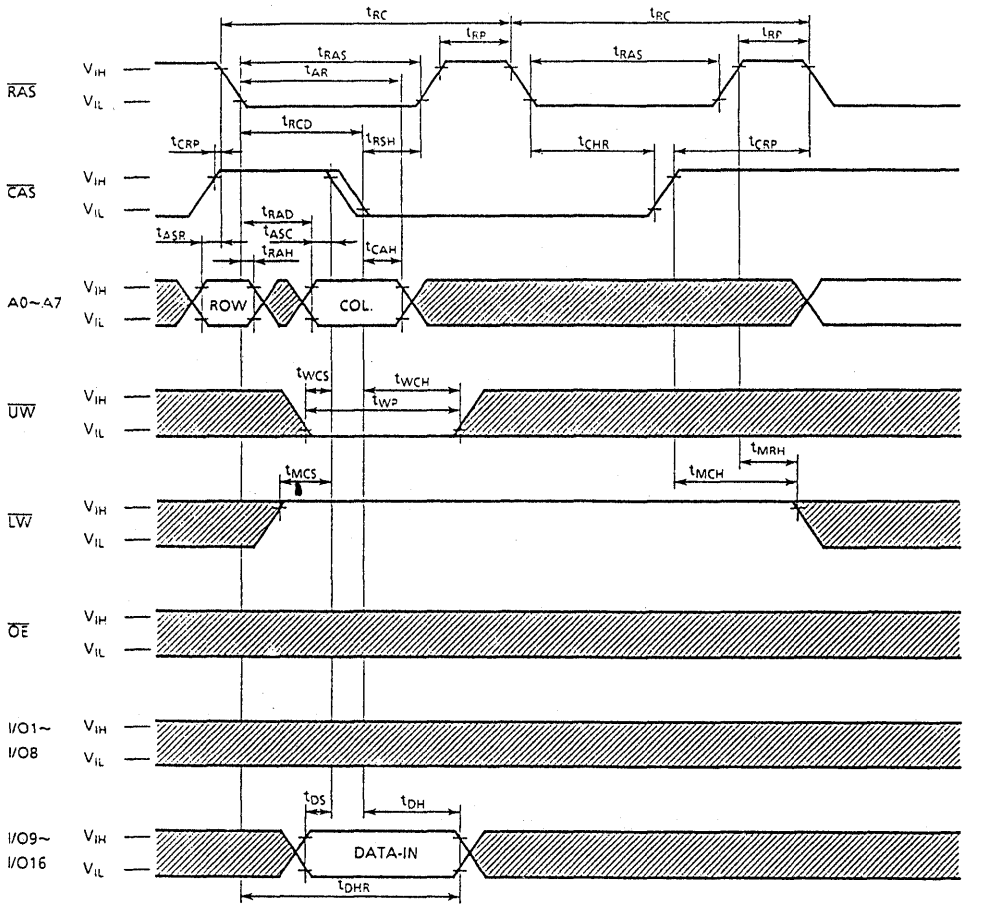
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

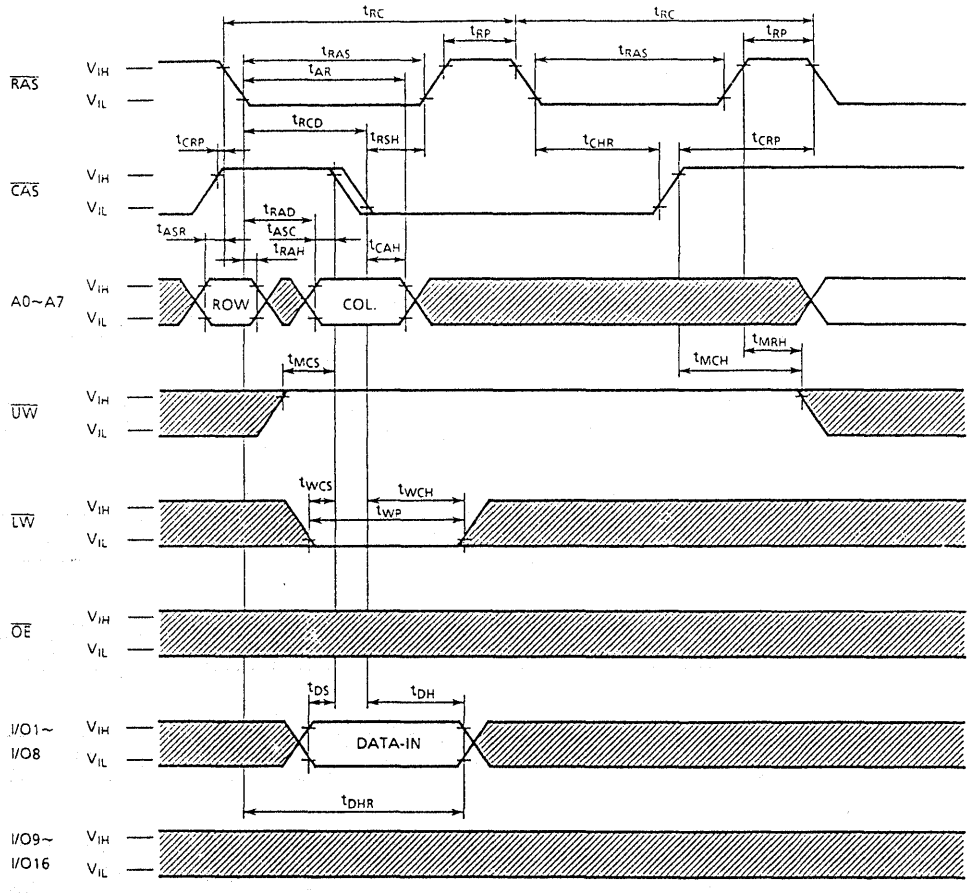
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

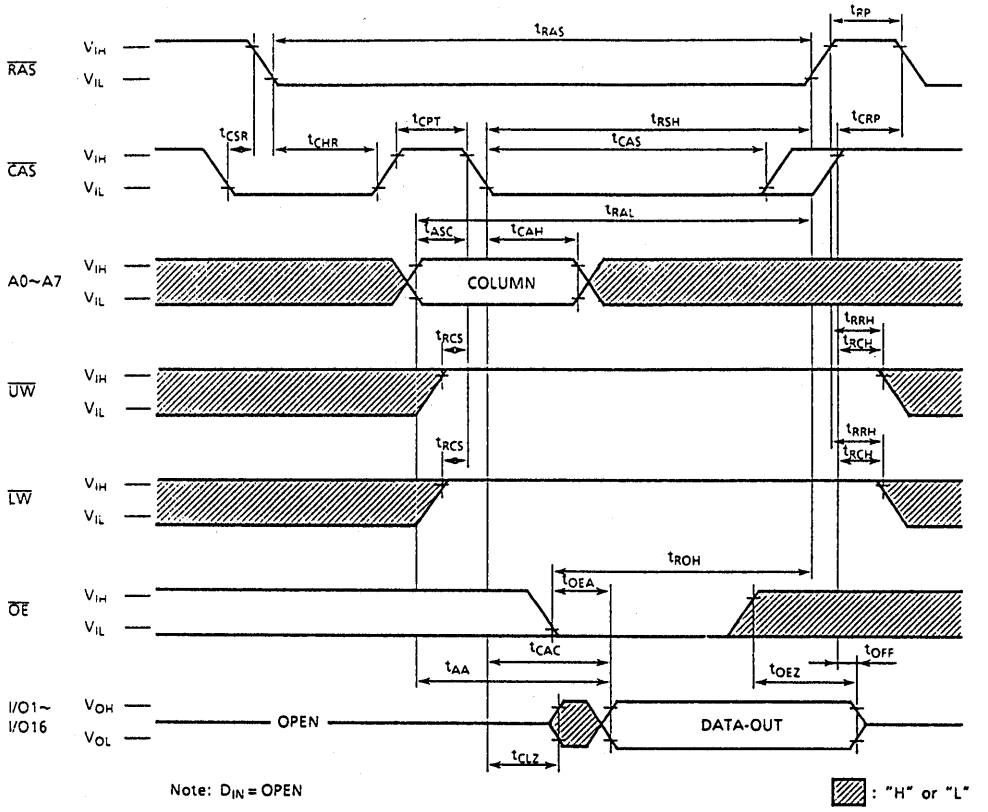
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



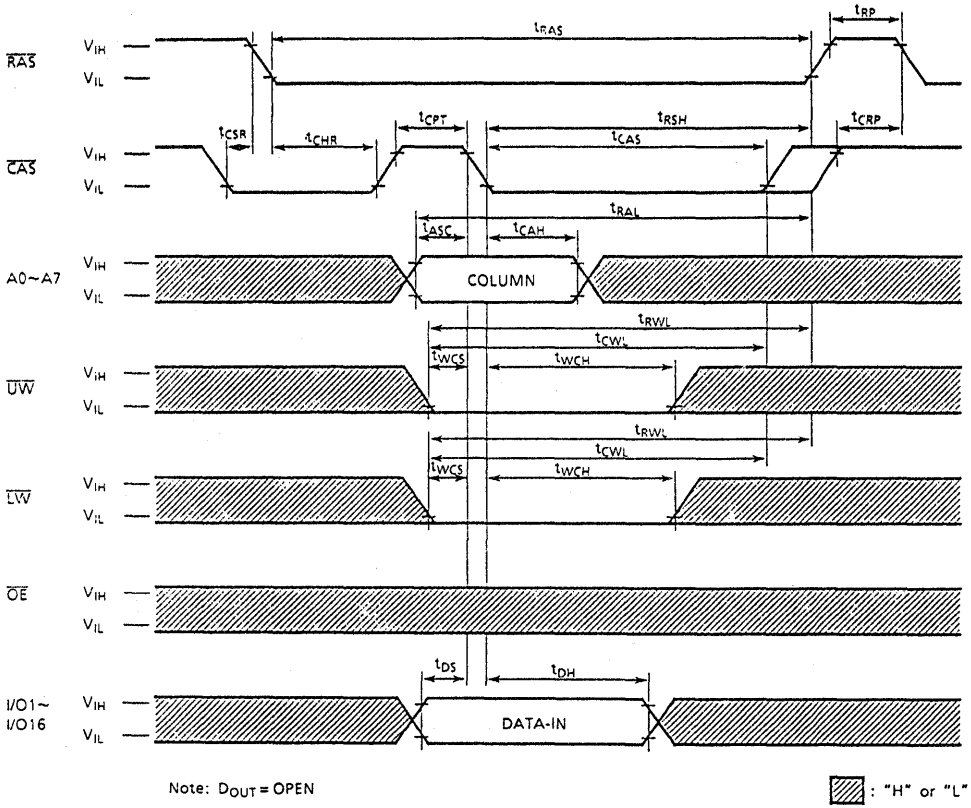
Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



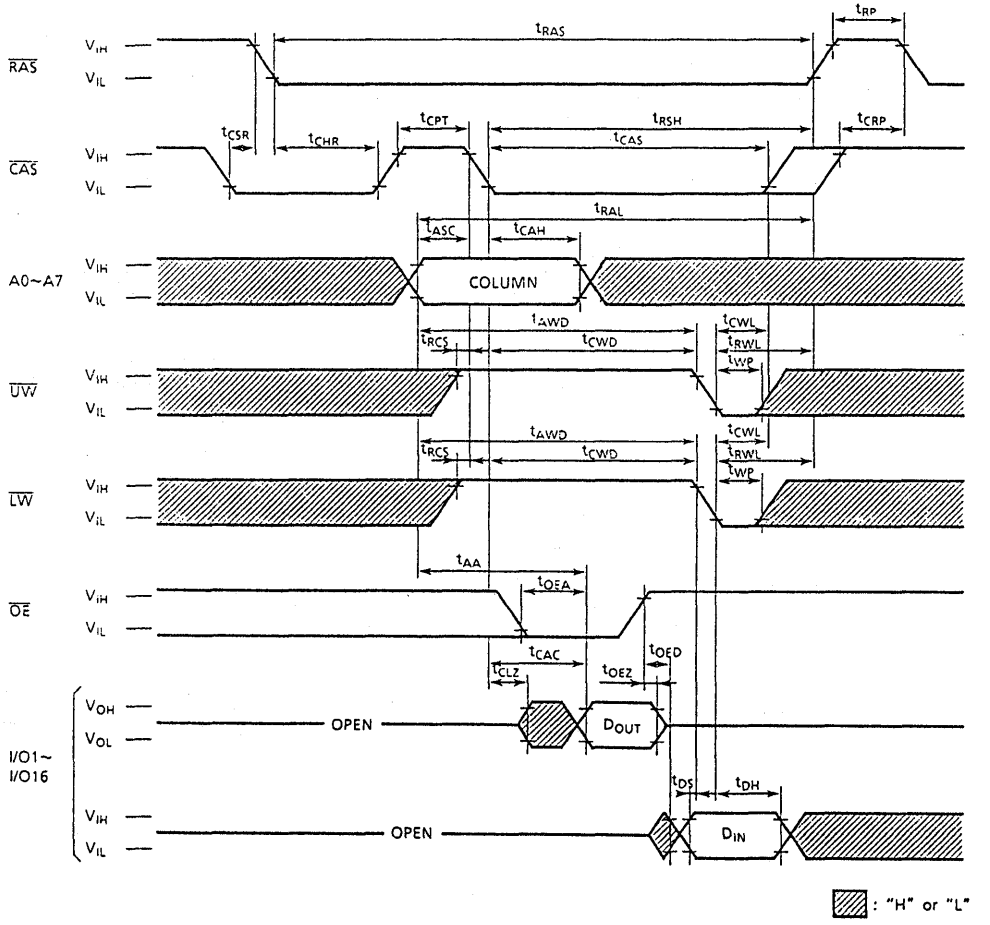
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511664JL/ZL are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{UW}$ and $\overline{LW}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{LW}$ strobes data on I/O1~I/O8 into the on-chip data latch. And the falling edge of $\overline{CAS}$ or $\overline{UW}$ strobes data on I/O9~I/16 into the on-chip data latch. In an early write cycle, $\overline{LW}$ and $\overline{UW}$ are brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In derayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{LW}$ and $\overline{UW}$ with setup and hold times referenced to these signals.

In derayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high inpedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

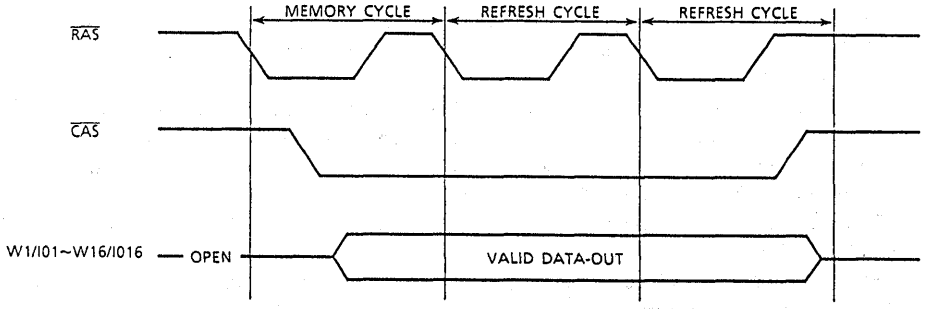
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511664JL/ZL offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511664JL/ZL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511664JL/ZL is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511664JL/ZL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

65,536 WORD × 16 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC511665J/Z is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511665J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511665J/Z to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

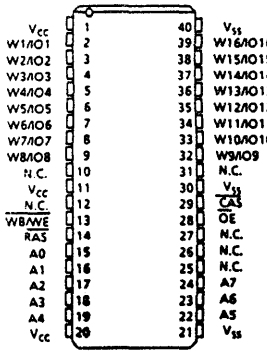
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511665J/Z-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	40ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

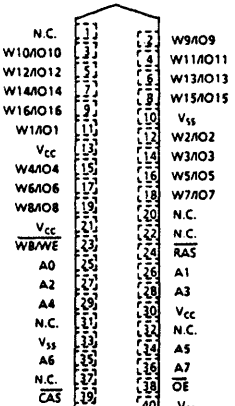
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511665J/Z-80)
  495mW MAX. Operating (TC511665J/Z-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package Plastic SOJ : TC511665J
  Plastic ZIP : TC511665Z

PIN CONNECTION (TOP VIEW)

Plastic SOJ



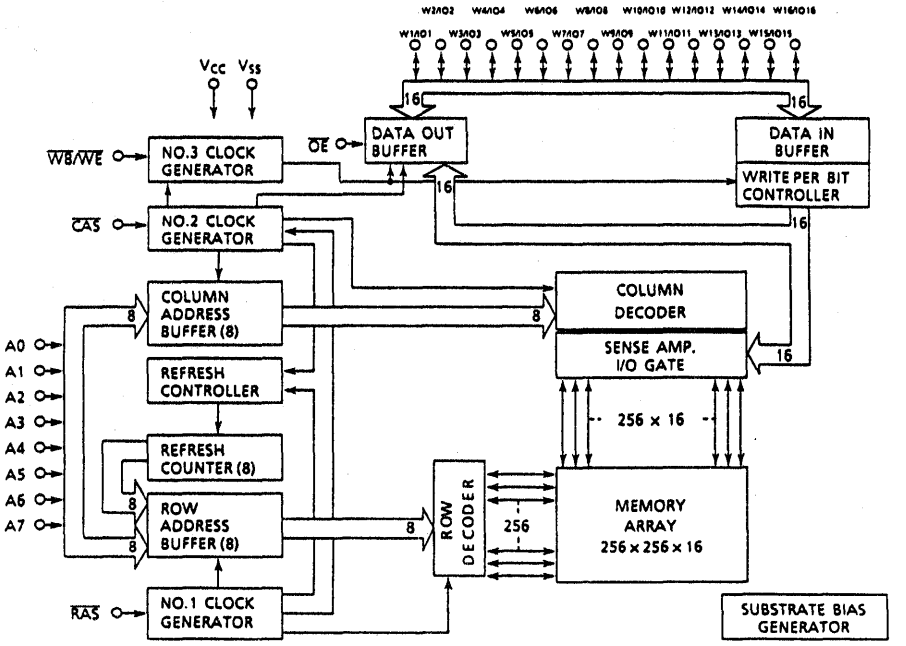
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Colomn Address Strobe
$\overline{WB/WE}$	Write Per Bit/ Read/Write Input
$\overline{OE}$	Ouput Enable
W1/IO1~ W16/IO16	Write Selection/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	−1.0 *1	-	0.8	V	2
V_{IL}	Input Low Voltage (W1/IO1~W16/IO16)	−0.5 *2	-	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns

*2 -2.0V at pulse width ≤ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511665J/Z-80	-	115	mA	3, 4, 5
		TC511665J/Z-10	-	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		-	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511665J/Z-80	-	115	mA	3, 5
		TC511665J/Z-10	-	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511665J/Z-80	-	70	mA	3, 4, 5
		TC511665J/Z-10	-	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		-	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511665J/Z-80	-	115	mA	3
		TC511665J/Z-10	-	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −2.5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511665J/Z-80		TC511665J/Z-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	35	–	40	ns	9,14
t_{AA}	Access Time from Column Address	–	45	–	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35	–	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	60	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511665J/Z-80		TC511665J/Z-10		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	4	–	4	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	70	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Trun Off Delay Time from $\overline{OE}$	0	10	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	ns	

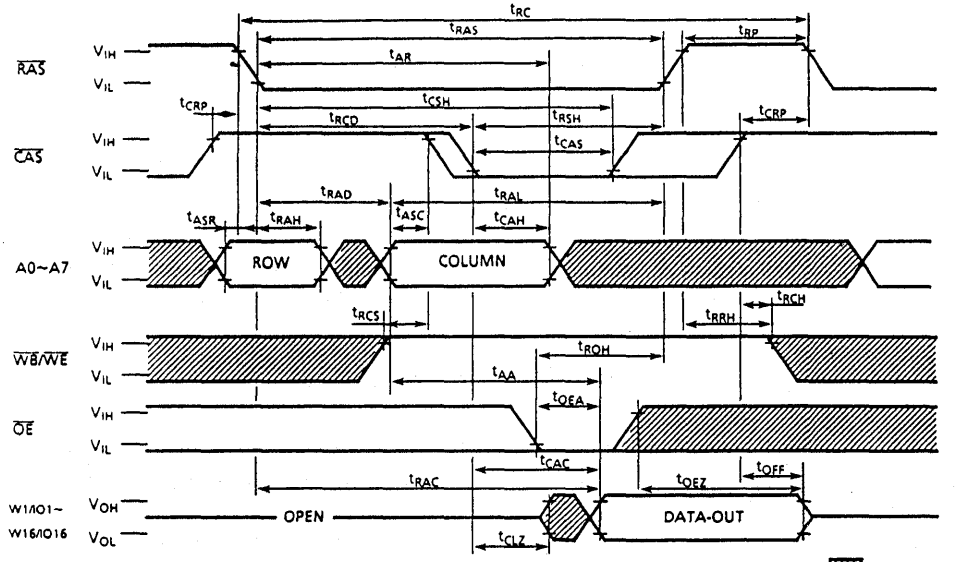
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A7)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/IO1~W16/IO16)	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 1 TTL load and 50pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{WB}$/) $\overline{WE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

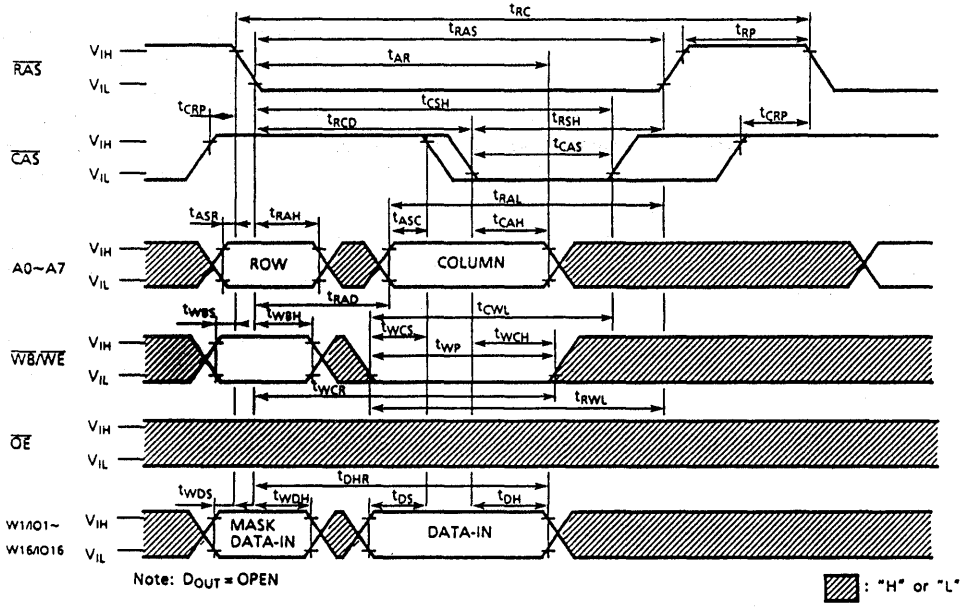
READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

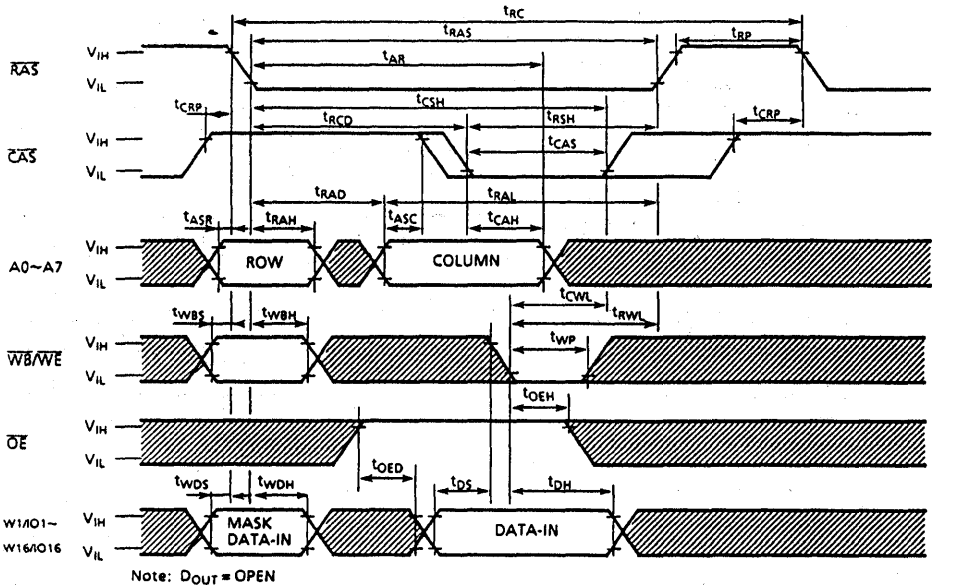
WRITE CYCLE (EARLY WRITE)



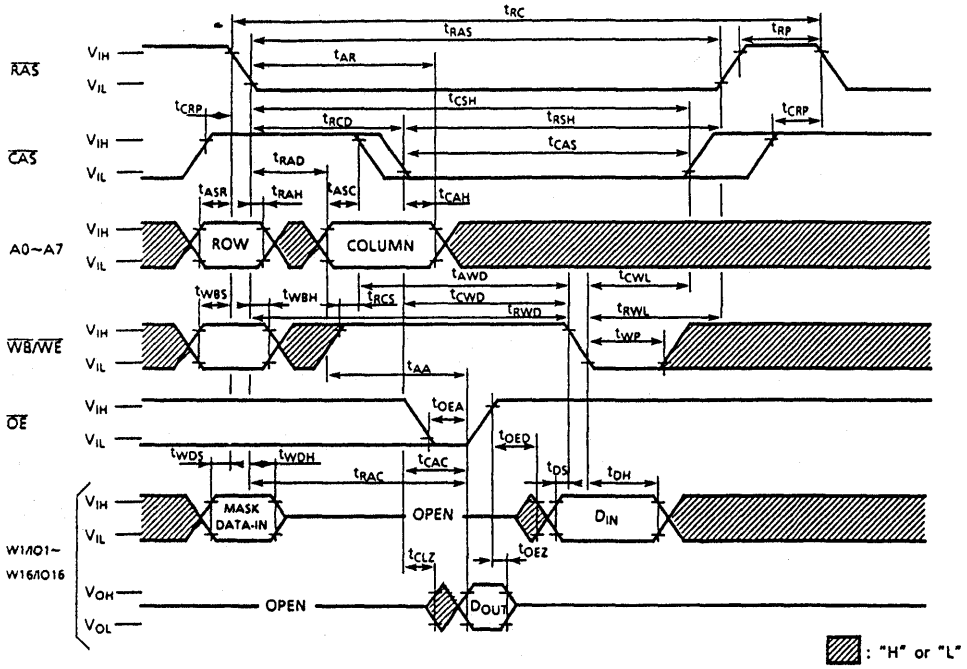
Note: D_{OUT} = OPEN

▨ : "H" or "L"

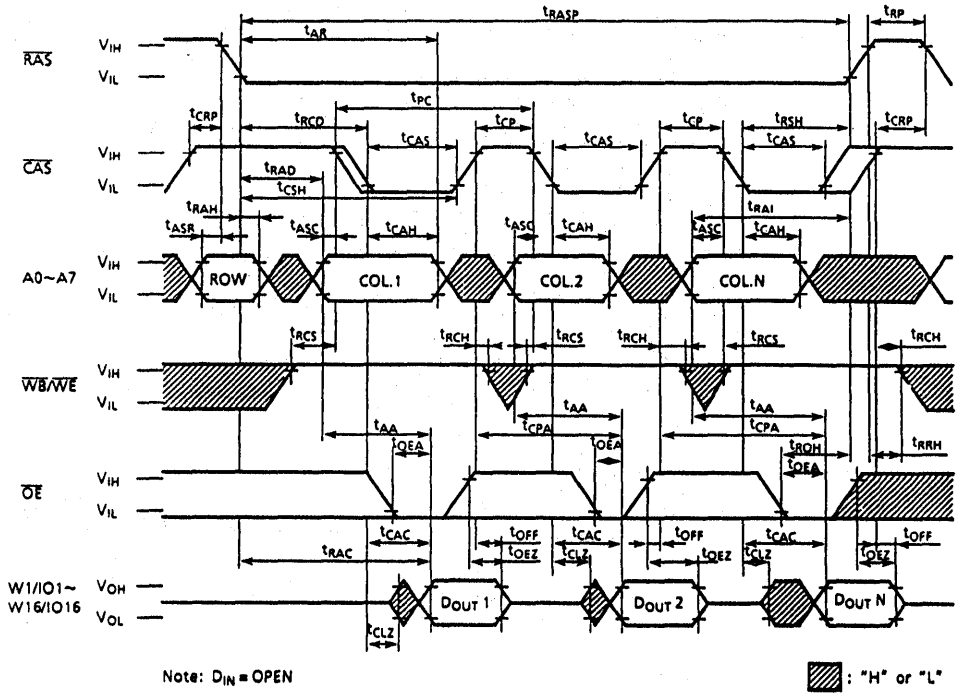
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



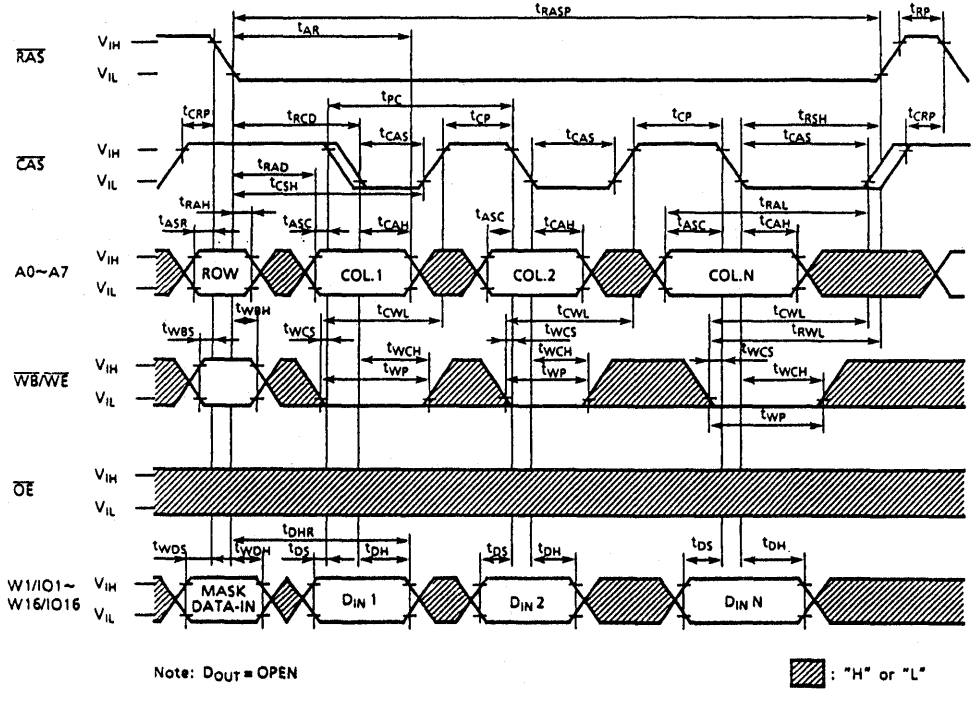
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

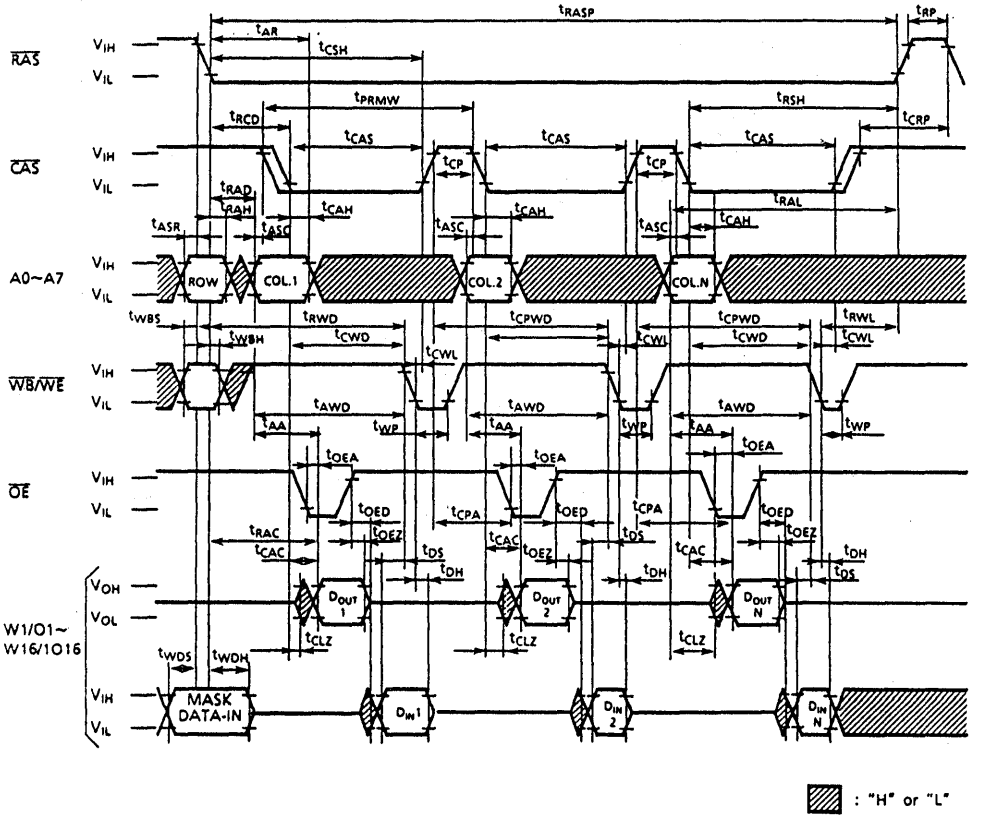
FAST PAGE MODE WRITE CYCLE



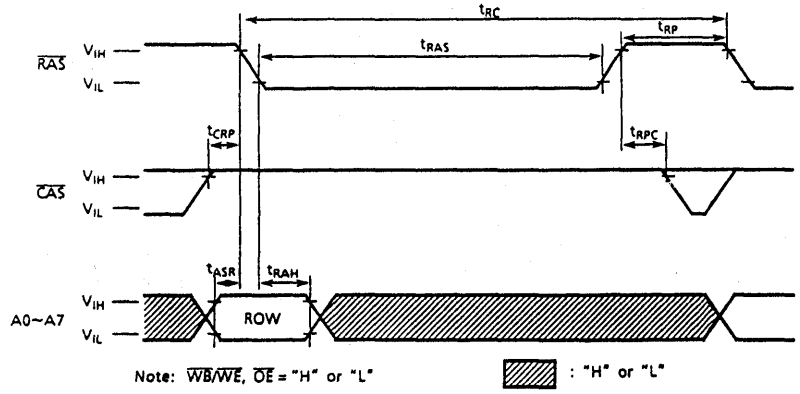
Note: D_{OUT} = OPEN

▨ : "H" or "L"

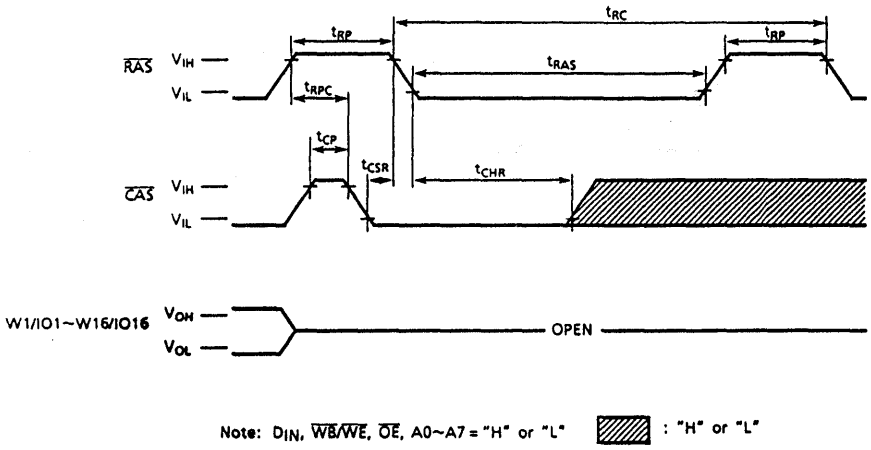
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



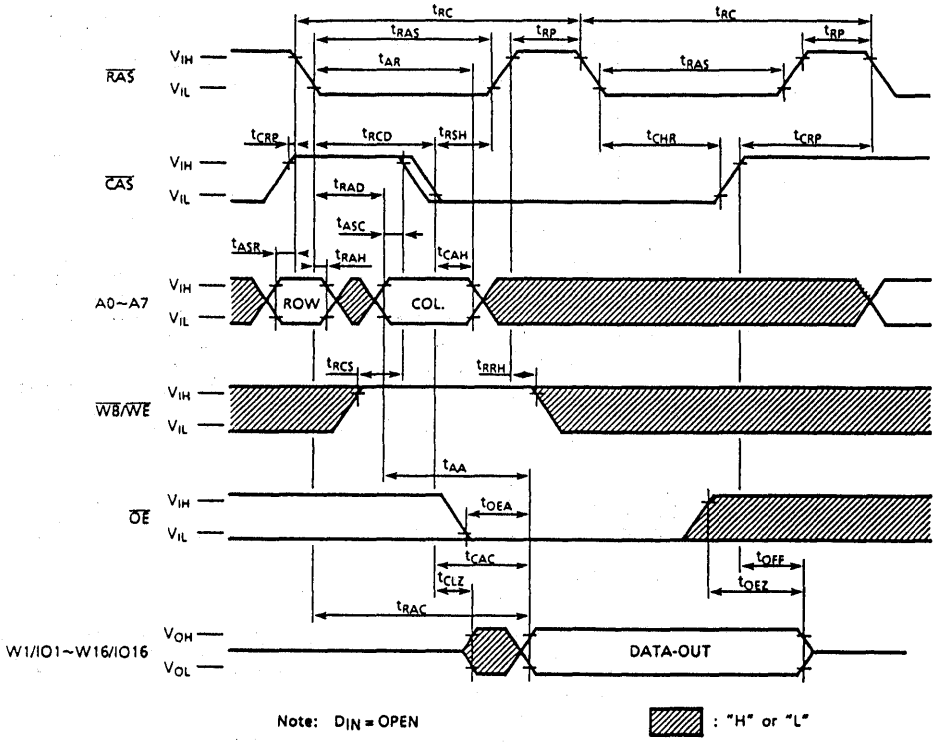
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



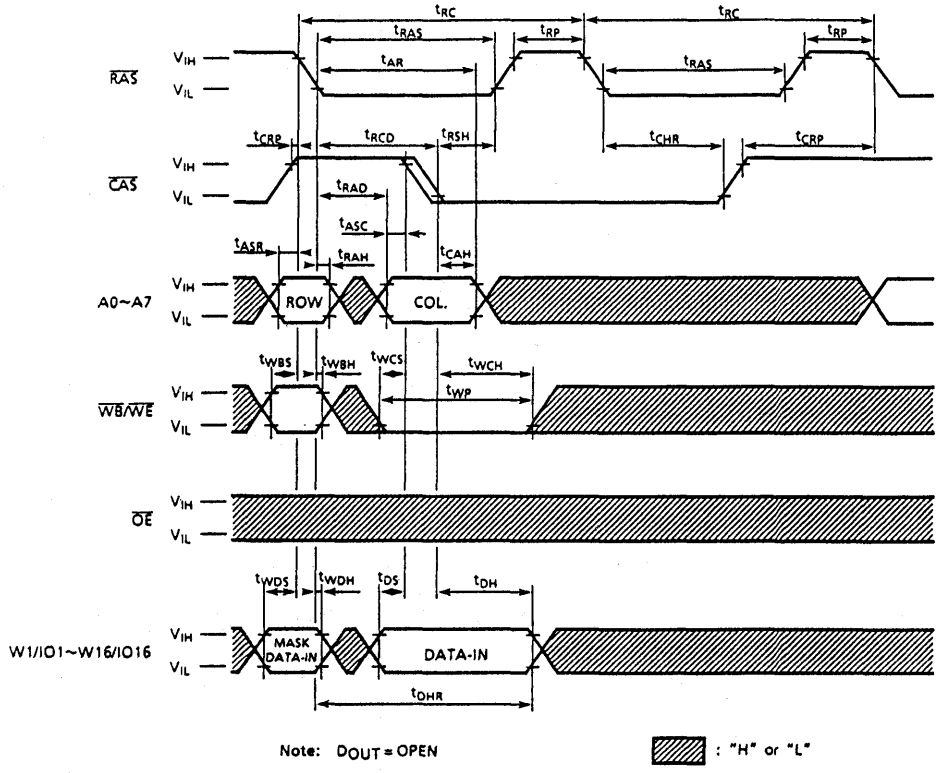
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

: "H" or "L"

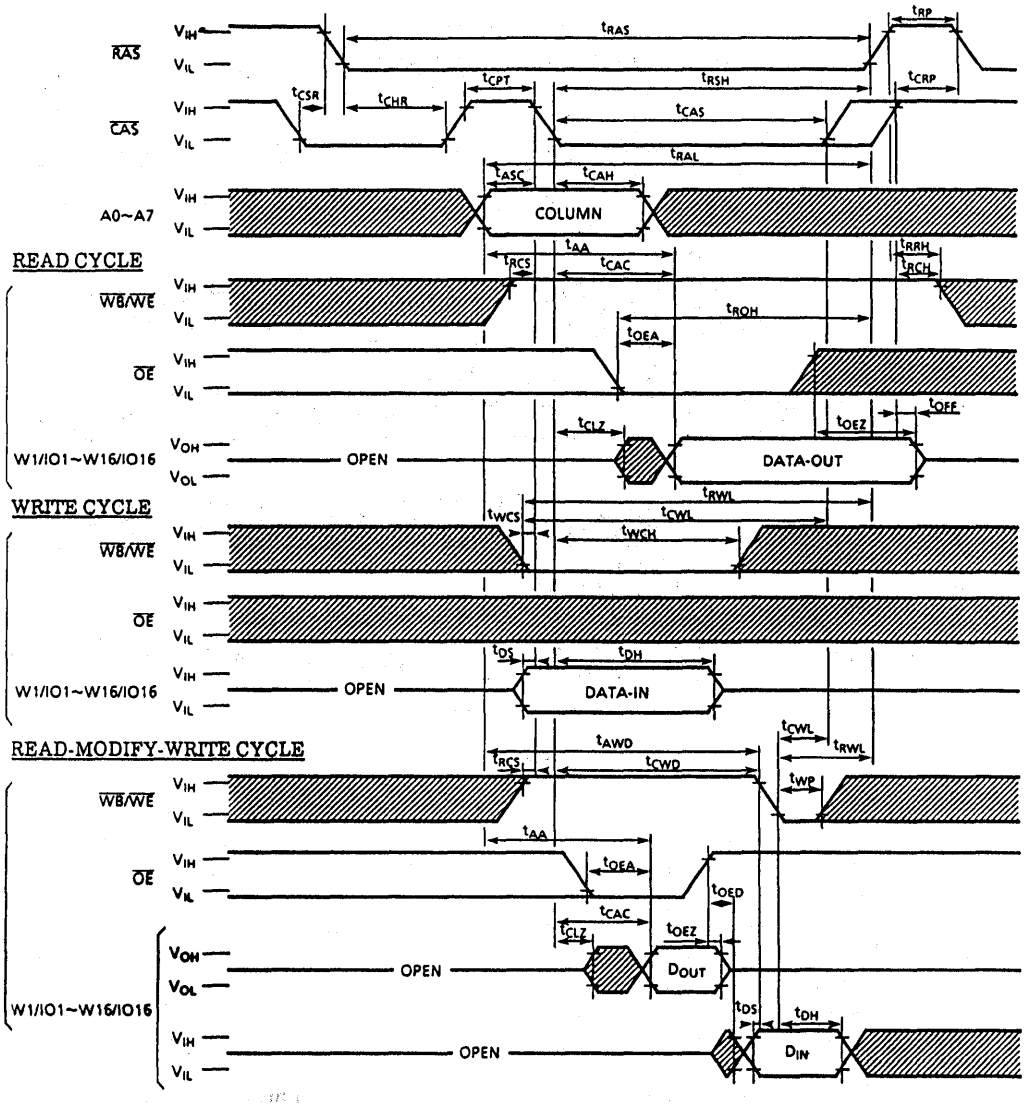
HIDDEN REFRESH CYCLE (WRITE)



Note: DOUT = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511665J/Z are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi/) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$ (/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

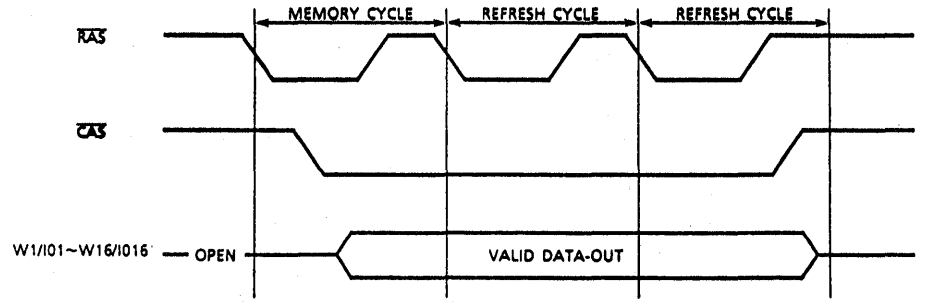
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511665J/Z offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511665J/Z allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511665J/Z is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511665J/Z can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

65,536 WORD × 16 BIT DYNAMIC RAM

* This is advanced information and specifications are subject to change without notice.

DESCRIPTION

The TC511665JL/ZL is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511665J/Z utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511665JL/ZL to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

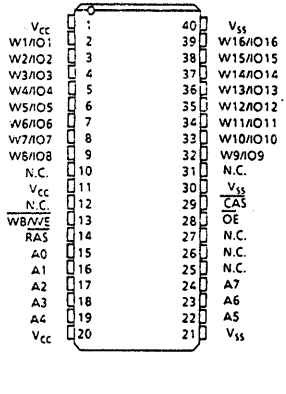
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511665JL/ZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	35ns	40ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

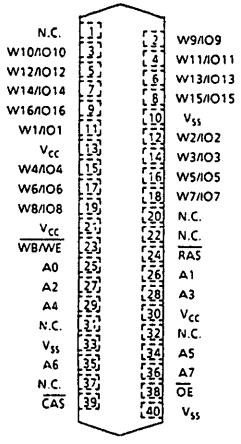
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511665JL/ZL-80)
  495mW MAX. Operating (TC511665JL/ZL-10)
  1.7mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/32ms
- Package Plastic SOJ : TC511665JL
  Plastic ZIP : TC511665ZL

PIN CONNECTION (TOP VIEW)

Plastic SOJ



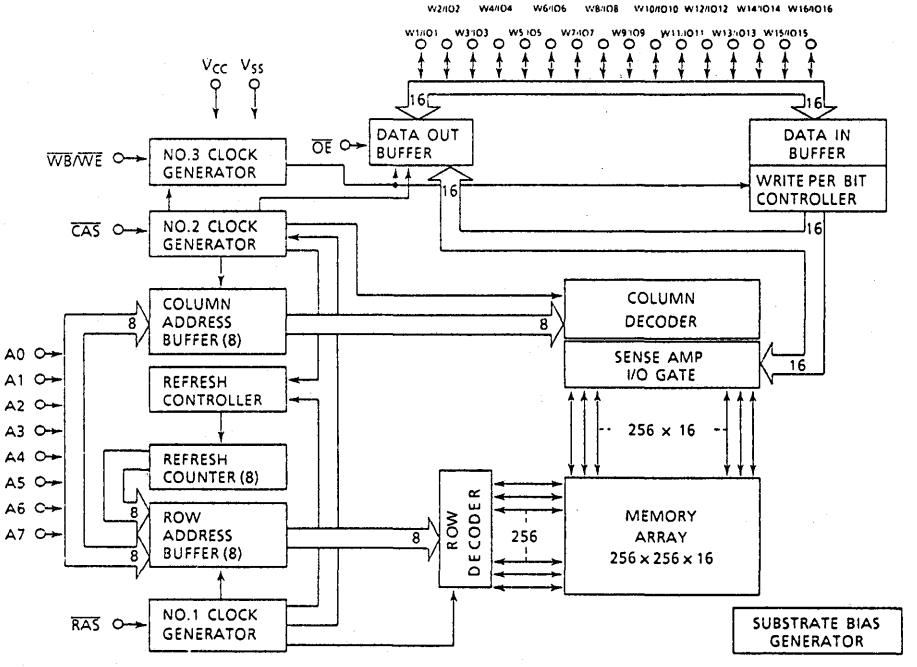
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Colomn Address Strobe
$\overline{WB/WE}$	Write Per Bit/ Read/Write Input
$\overline{OE}$	Ouput Enable
W1/IO1~ W16/IO16	Write Selection/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (W1/IO1~W16/IO16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511665JL/ZL-80	–	115	mA	3, 4, 5
		TC511665JL/ZL-10	–	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	TC511665JL/ZL-80	–	115	mA	3, 5
		TC511665JL/ZL-10	–	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	TC511665JL/ZL-80	–	70	mA	3, 4, 5
		TC511665JL/ZL-10	–	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	300	μA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	TC511665JL/ZL-80	–	115	mA	3
		TC511665JL/ZL-10	–	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE} = V_{CC} - 0.2V$, $\overline{WB/WE} = V_{CC} - 0.2V$ or 0.2V, A0~A7 = $V_{CC} - 0.2V$ or 0.2V, W1/IO1~W16/IO16 = $V_{CC} - 0.2V$, 0.2V or OPEN: $t_{RC} = 125\mu s$, $t_{RAS} = t_{RAS}$ MIN.~1μs)		–	400	μA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2.5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC511665JL/ZL-80		TC511665JL/ZL-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	–	35	–	40	ns	10,15
t_{AA}	Access Time from Column Address	–	45	–	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	35	–	40	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	35	10,000	40	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	60	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	ns	13

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511665JL/ZL-80		TC511665JL/ZL-10		UNITS	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	32	–	32	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	70	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	ns	
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Trun Off Delay Time from $\overline{OE}$	0	10	0	20	ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	ns	

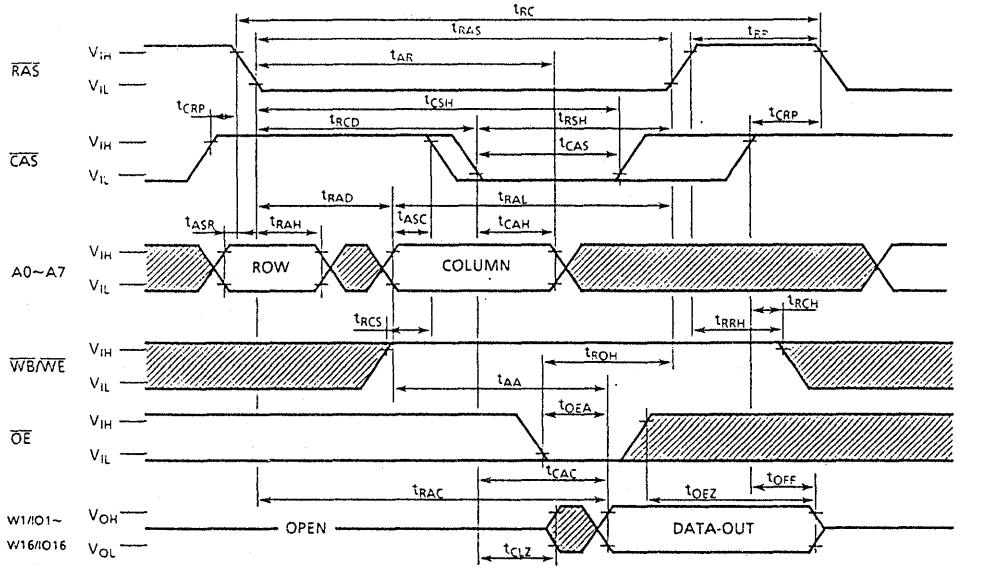
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A7)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/IO1~W16/IO16)	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T = 5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
   Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 1 TTL load and 50pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{WB}$/) $\overline{WE}$ leading edge in read-modify-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

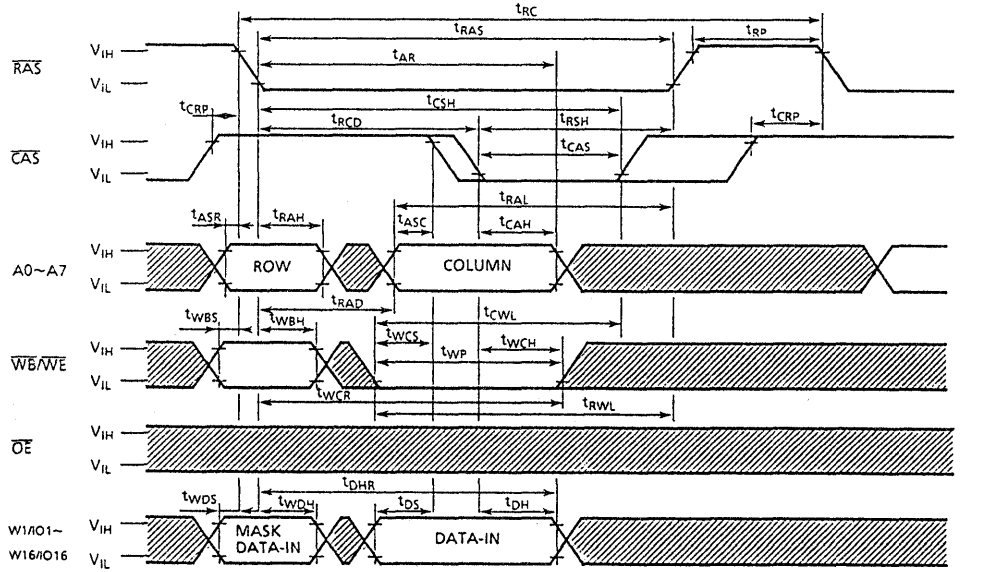
READ CYCLE



Note: D_{IN} = OPEN

: "H" or "L"

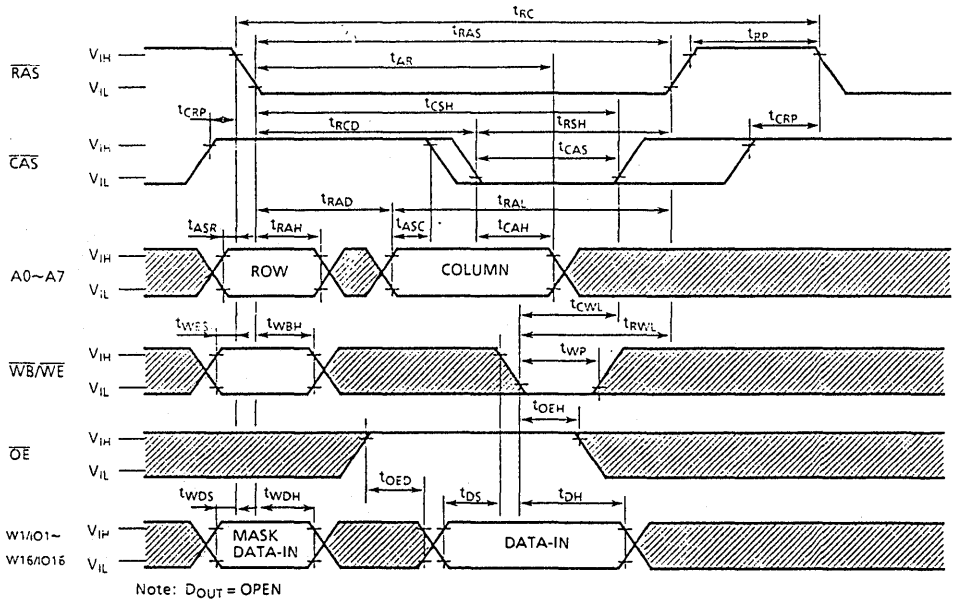
WRITE CYCLE (EARLY WRITE)



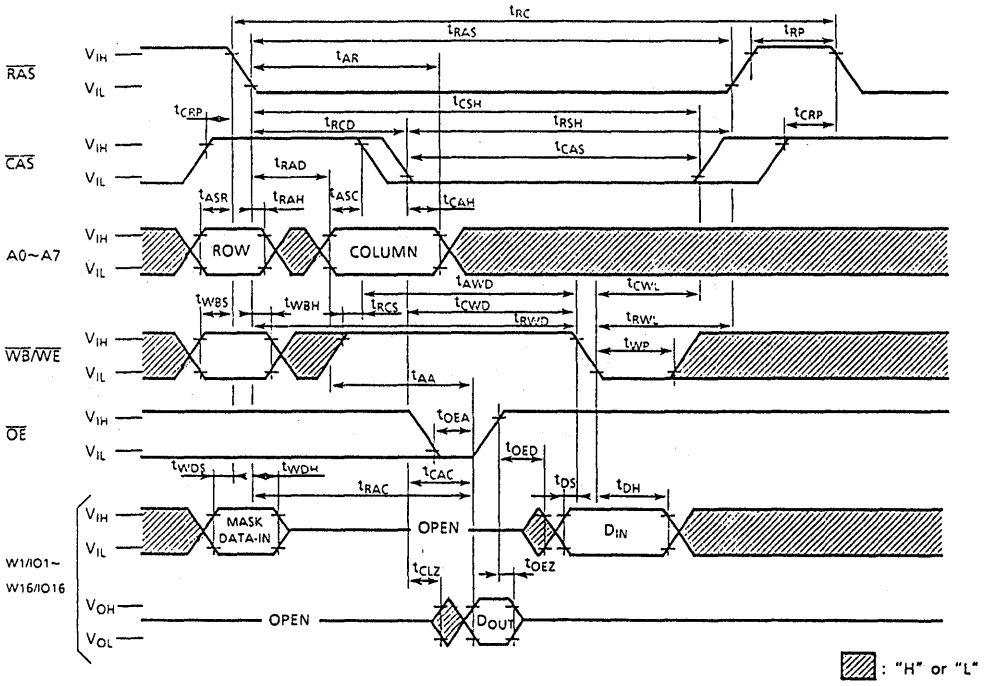
Note: D_{OUT} = OPEN

: "H" or "L"

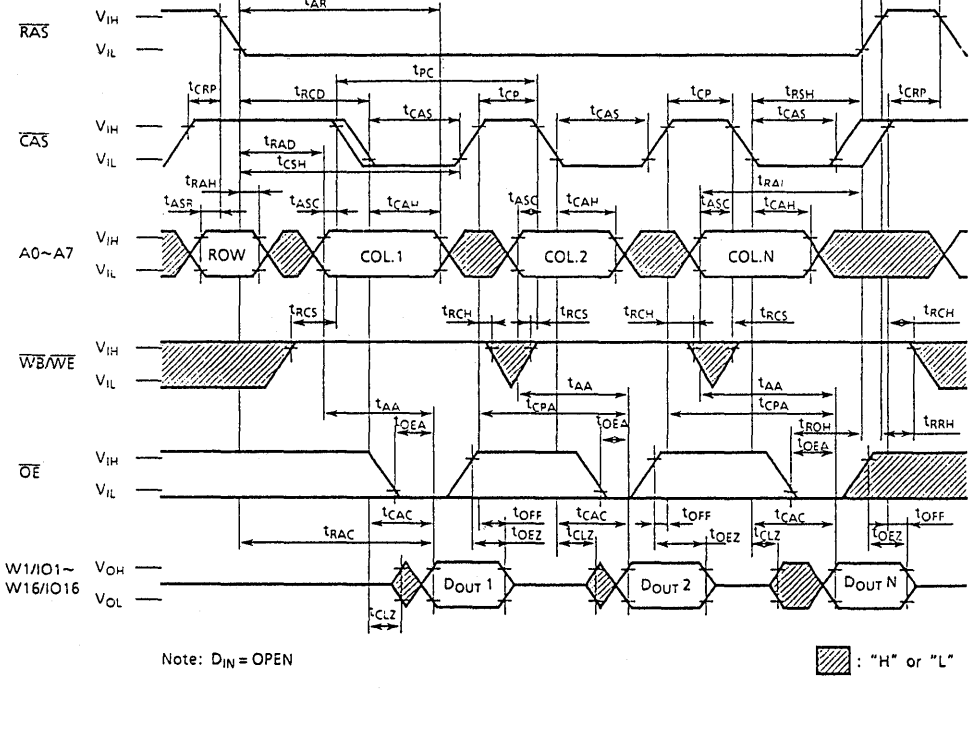
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



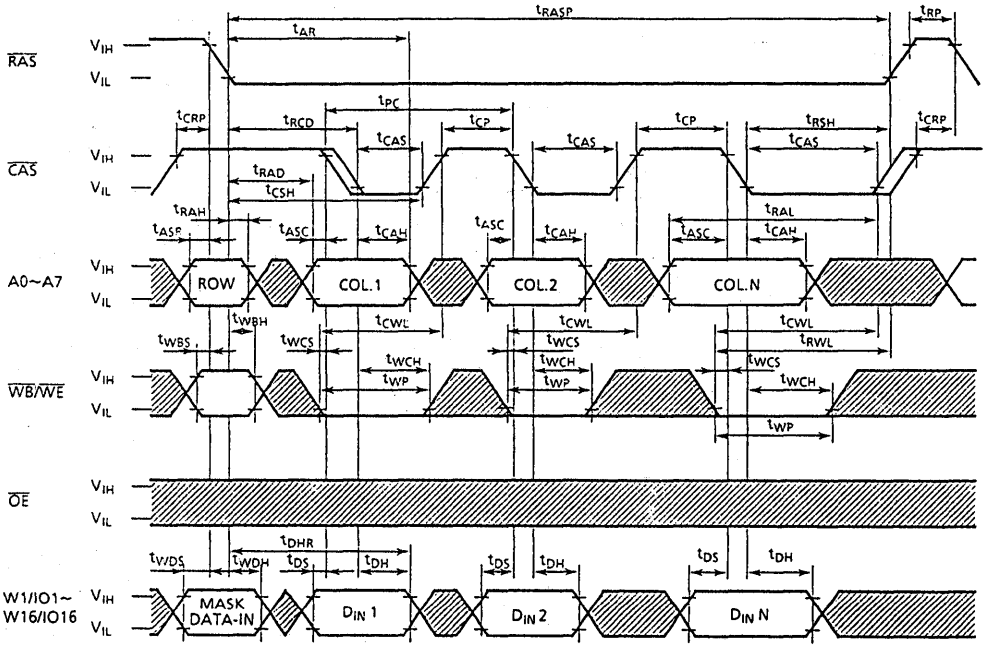
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

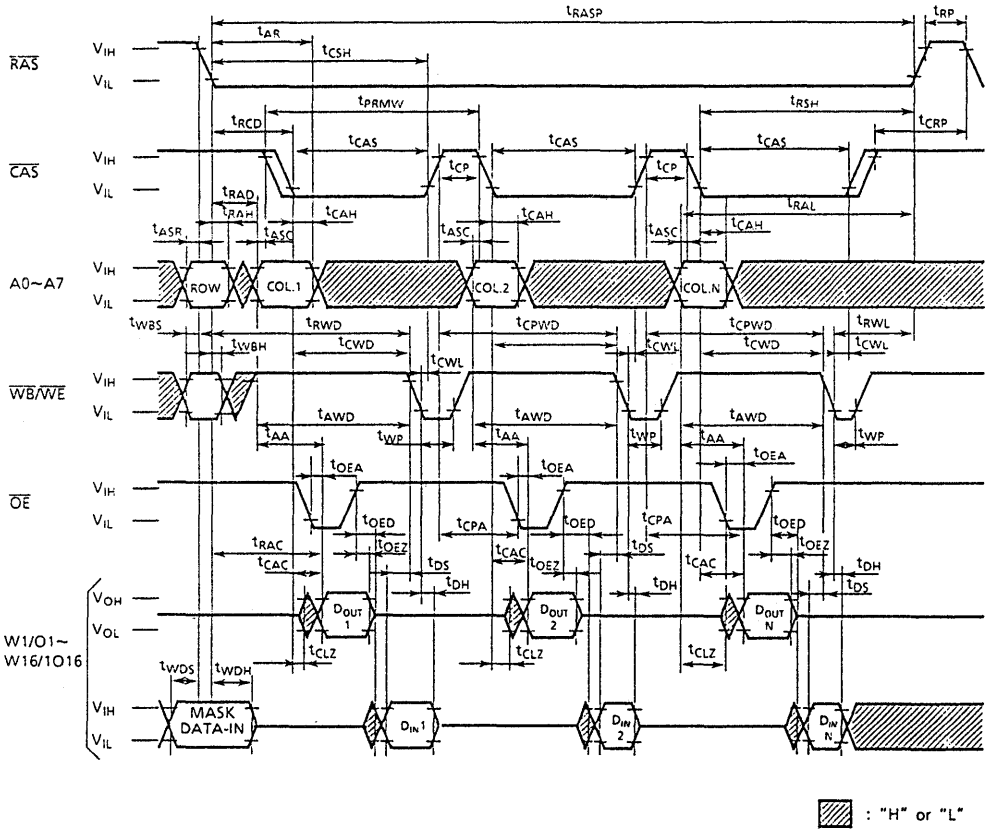
FAST PAGE MODE WRITE CYCLE



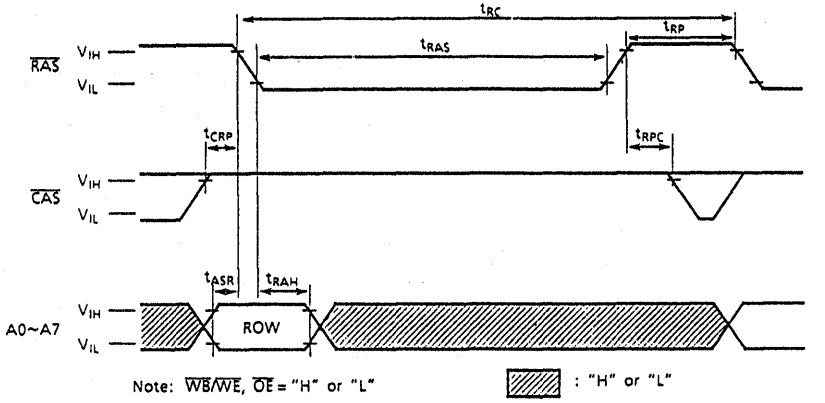
Note: D_{OUT} = OPEN

▨ : "H" or "L"

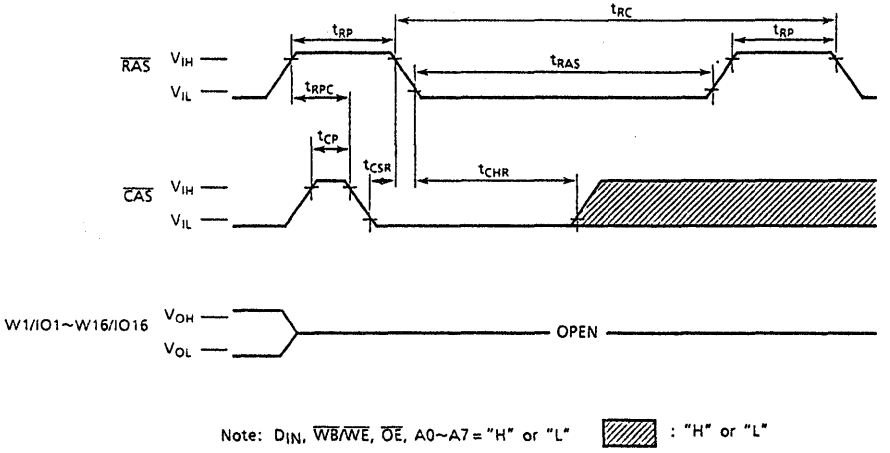
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



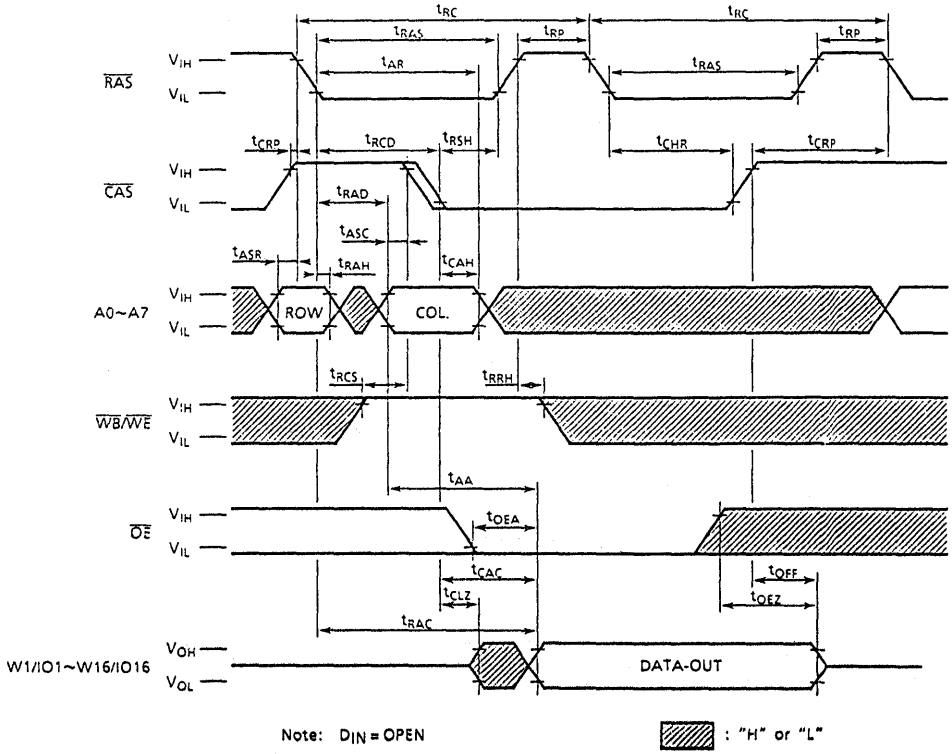
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



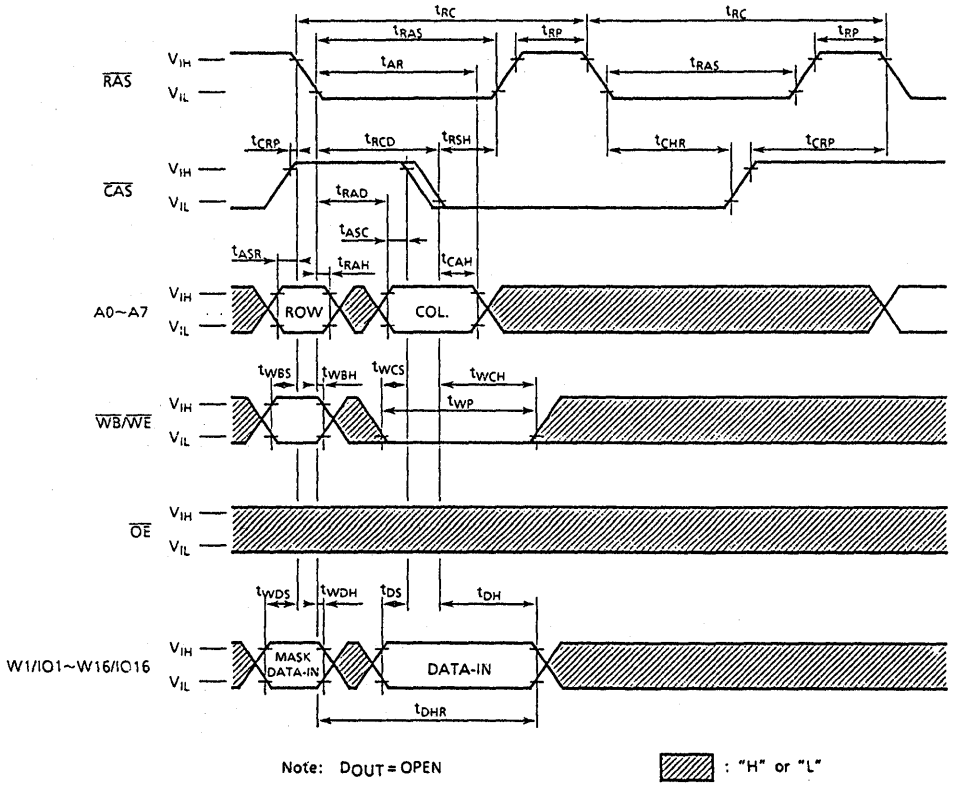
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

: "H" or "L"

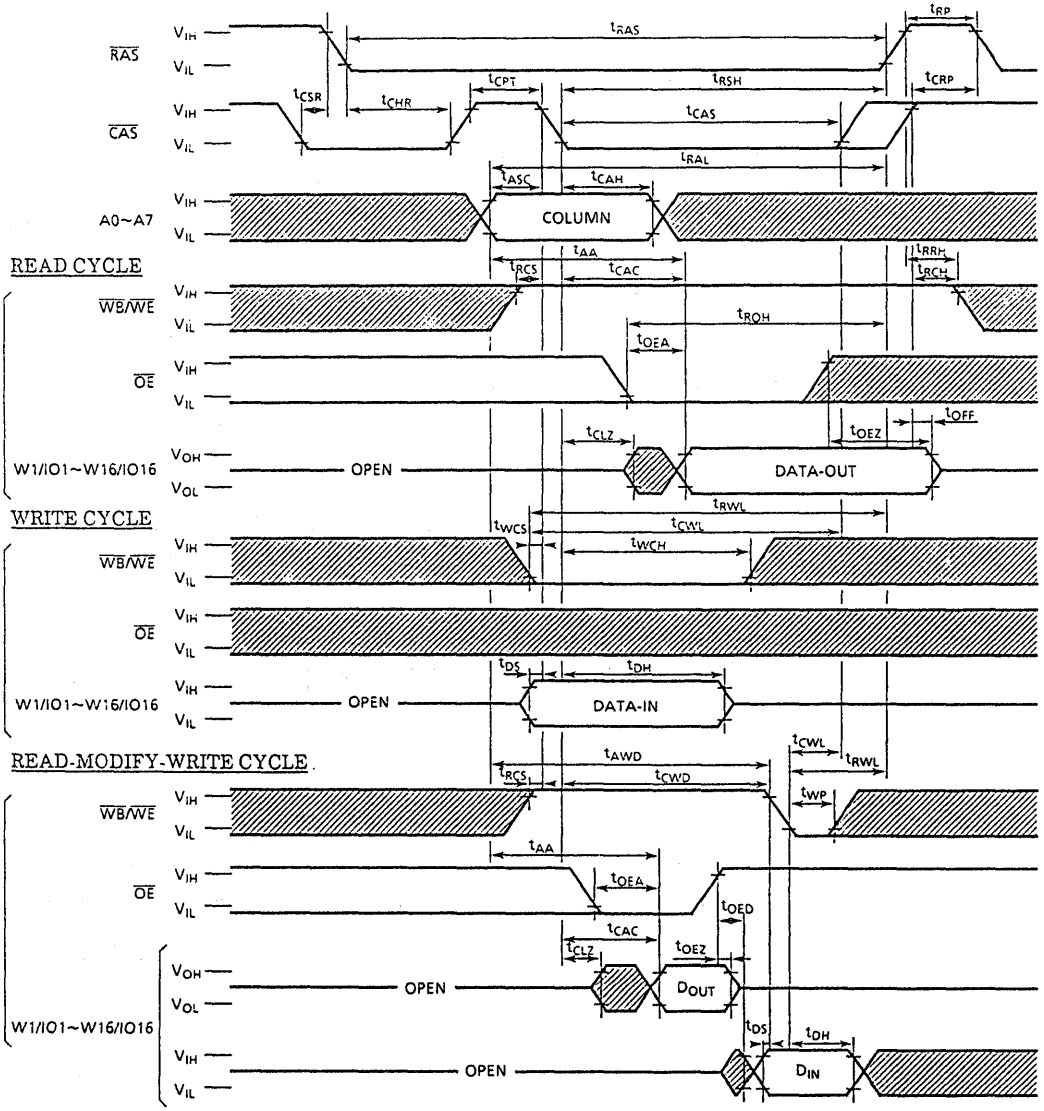
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511665JL/ZL are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi/) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$ (/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

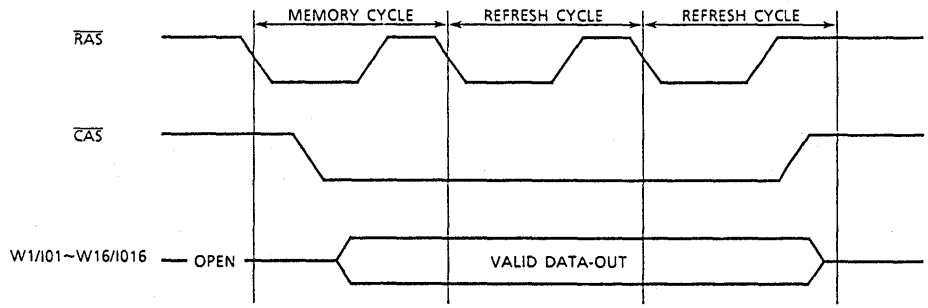
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511665JL/ZL offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511665JL/ZL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511665JL/ZL is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511665JL/ZL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

TENTATIVE DATA
65,536 WORD × 16 BIT DYNAMIC RAM

DESCRIPTION

The TC511664BJ/BZ is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511664BJ/BZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511664BJ/BZ to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

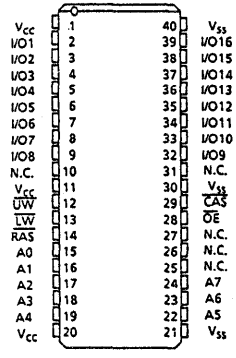
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511664BJ/BZ-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

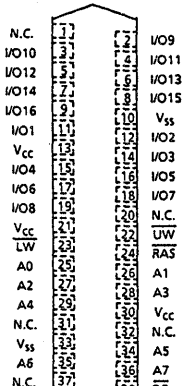
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511664BJ/BZ-80)
  495mW MAX. Operating (TC511664BJ/BZ-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Byte-Write and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package TC511664BJ:SOJ40-P-400
  TC511664BZ:ZIP40-P-475

PIN CONNECTION (TOP VIEW)

Plastic SOJ



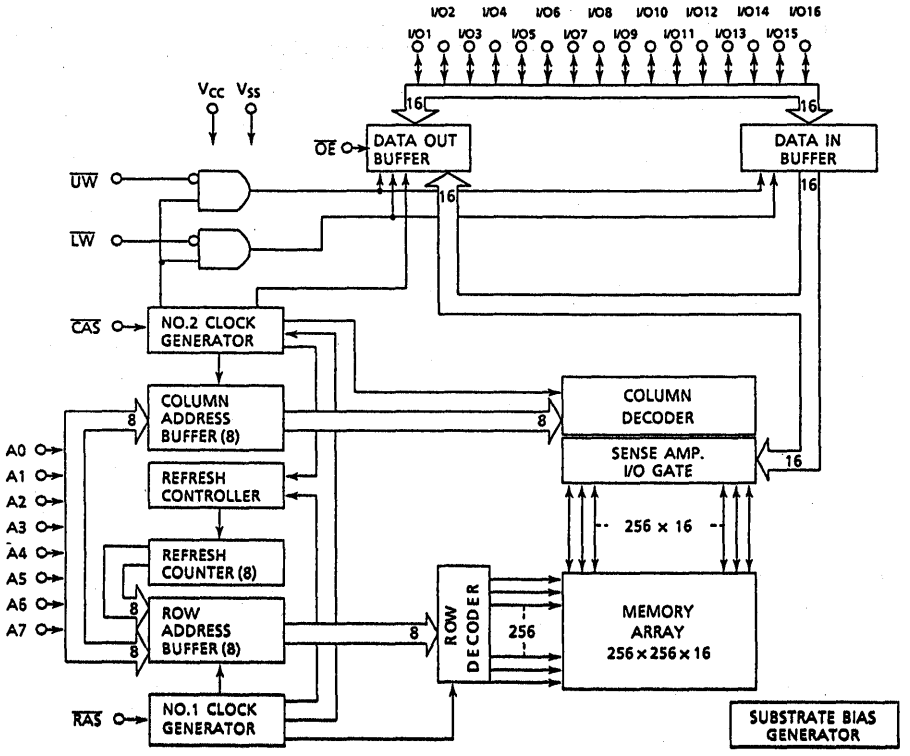
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (T_a = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (I/O1~I/O16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511664BJ/BZ-80	−	115	mA	3, 4, 5
		TC511664BJ/BZ-10	−	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		−	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511664BJ/BZ-80	−	115	mA	3, 5
		TC511664BJ/BZ-10	−	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511664BJ/BZ-80	−	70	mA	3, 4, 5
		TC511664BJ/BZ-10	−	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		−	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511664BJ/BZ-80	−	115	mA	3
		TC511664BJ/BZ-10	−	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −2.5mA)		2.4	−	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		−	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511664BJ/BZ-80		TC511664BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	—	170	—	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	—	225	—	ns	
t_{PC}	Fast Page Mode Cycle Time	55	—	65	—	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	—	120	—	ns	
t_{RAC}	Access Time from $\overline{RAS}$	—	80	—	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	—	30	—	35	ns	9,14
t_{AA}	Access Time from Column Address	—	45	—	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	50	—	60	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	45	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	—	35	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	—	100	—	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	65	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{ASR}	Row Address Set-Up Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Set-Up Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	—	55	—	ns	
t_{RCS}	Read Command Set-Up Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time	0	—	0	—	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	ns	11
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{DS}	Data Set-Up Time	0	—	0	—	ns	12
t_{DH}	Data Hold Time	15	—	15	—	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511664BJ/BZ-80		TC511664BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	4	–	4	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	65	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	10	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{MCS}	Masked Write Set-Up Time	0	–	0	–	ns	
t_{MRH}	Masked Write Hold time Referenced to $\overline{RAS}$	0	–	0	–	ns	
t_{MCH}	Masked Write Hold time Referenced to $\overline{CAS}$	0	–	0	–	ns	

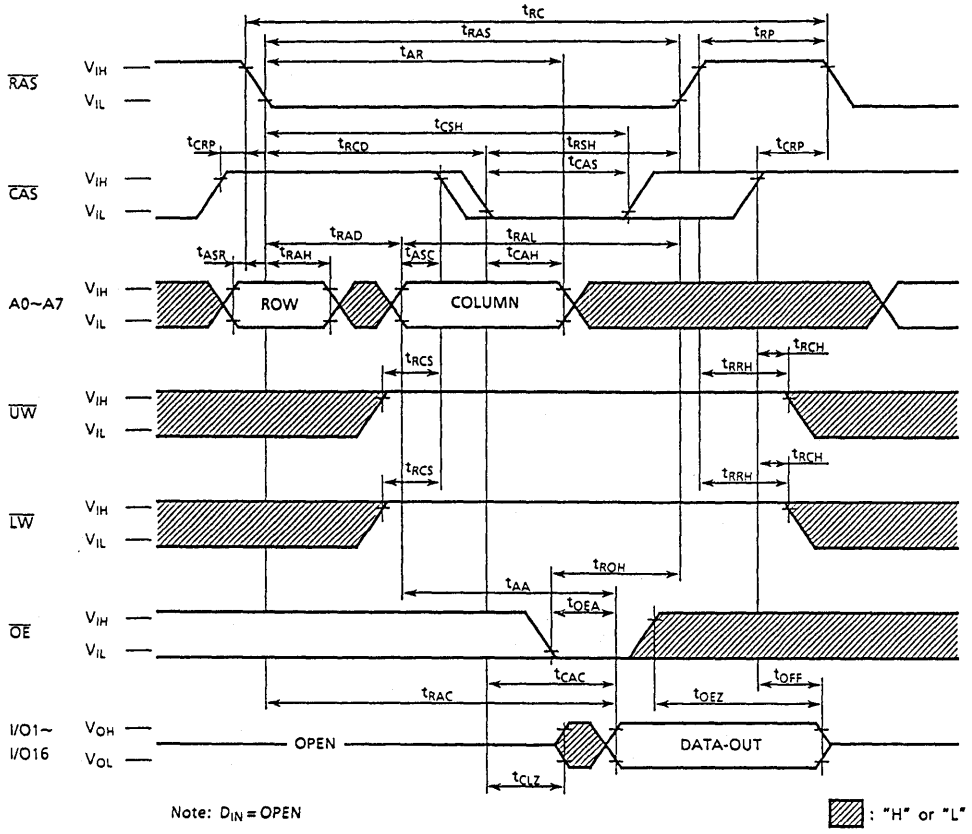
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	-	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	-	7	pF

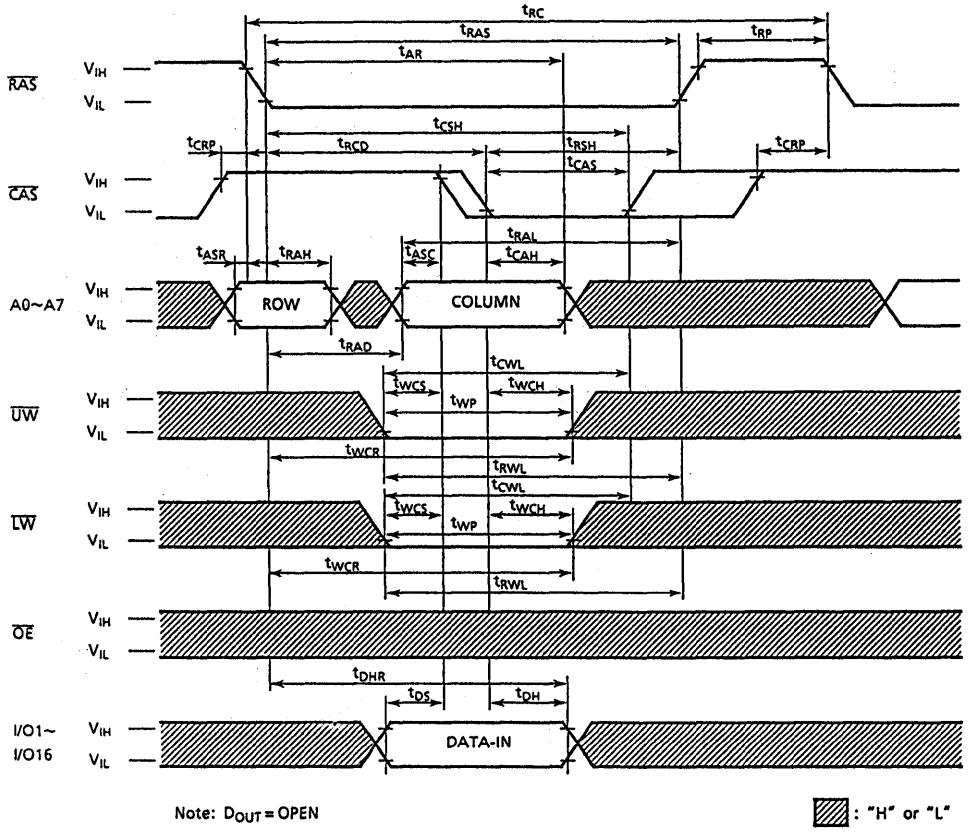
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 1 TTL load and 50pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{UW}$, $\overline{LW}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCAS
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A7
ROW
COLUMN
tRCH
tRCS
tRRH
UW
LW
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1~
I/O16
VOH
VOL
OPEN
DATA-OUT
tCLZ
Note: DIN = OPEN
: "H" or "L"

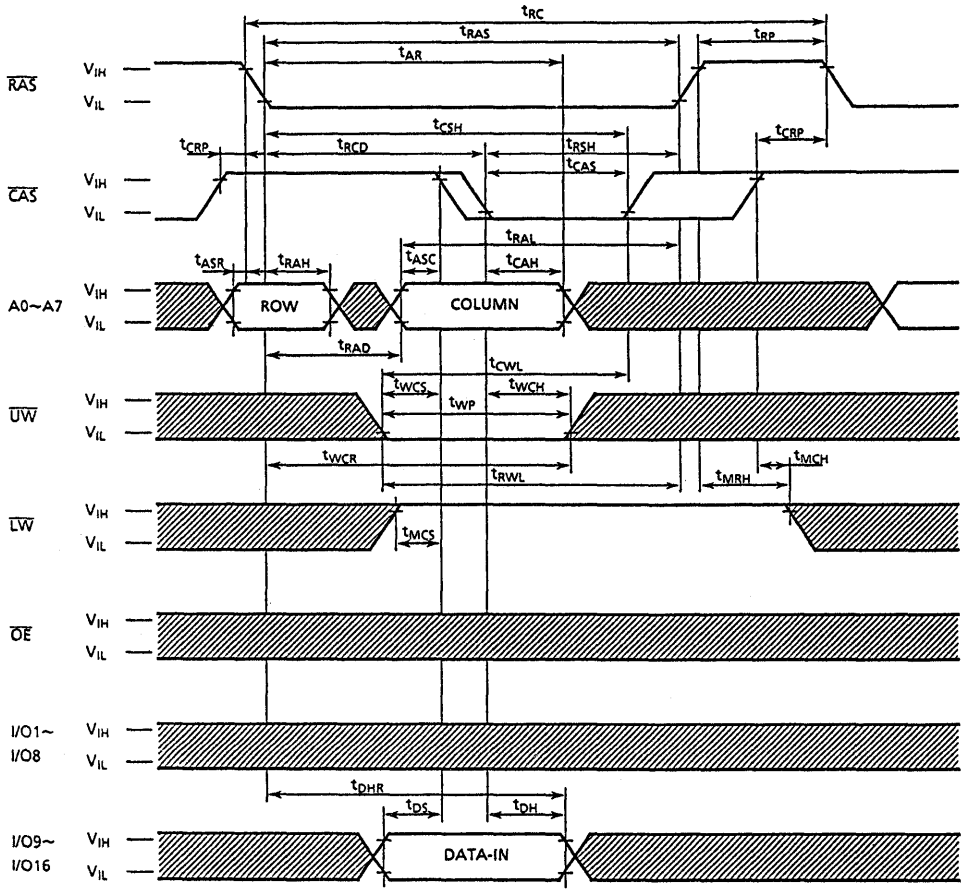
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

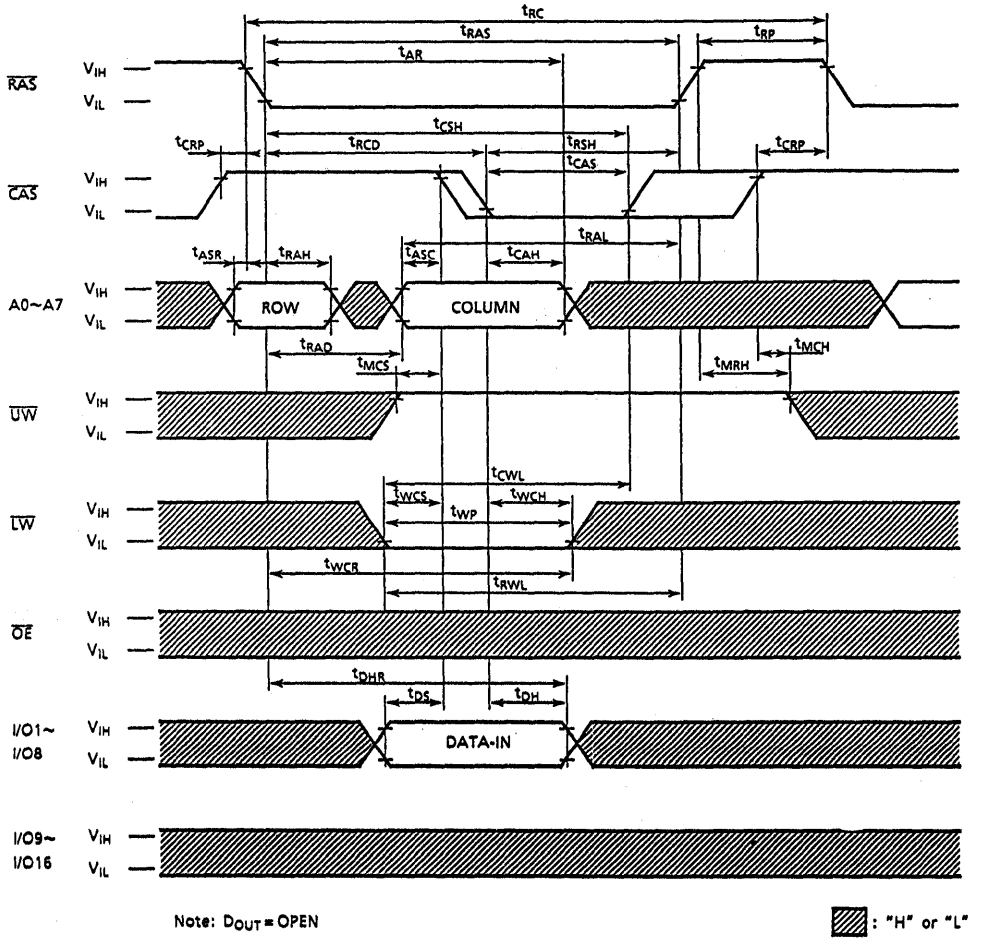
UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

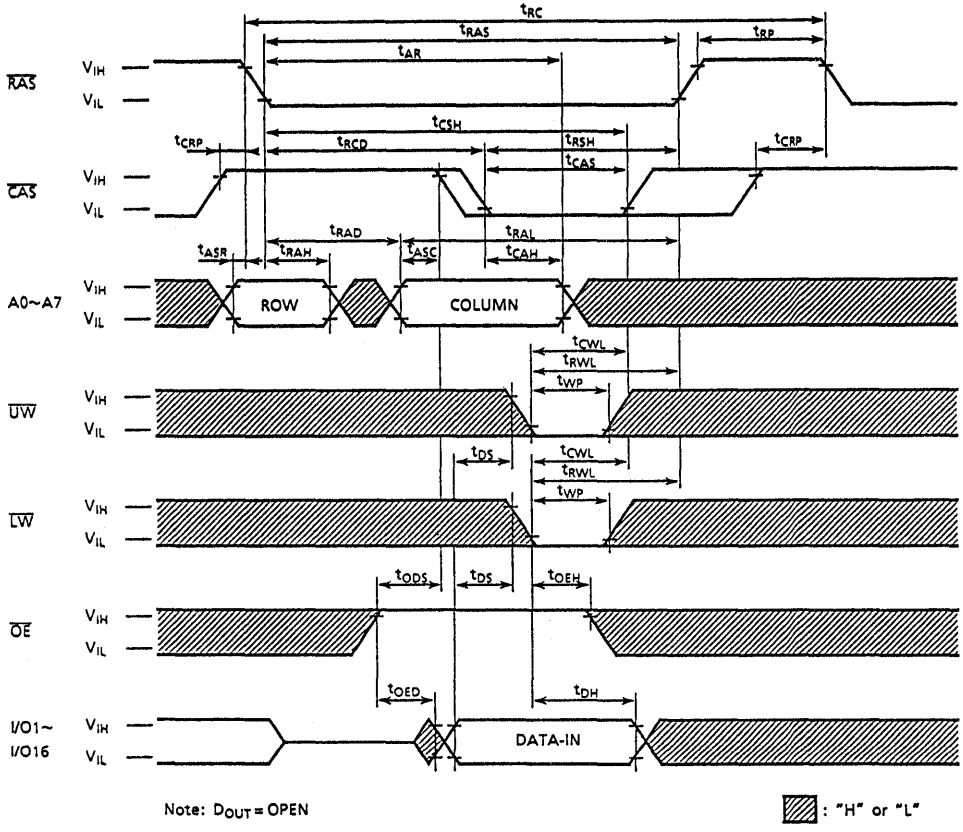
LOWER BYTE WRITE CYCLE (EARLY WRITE)



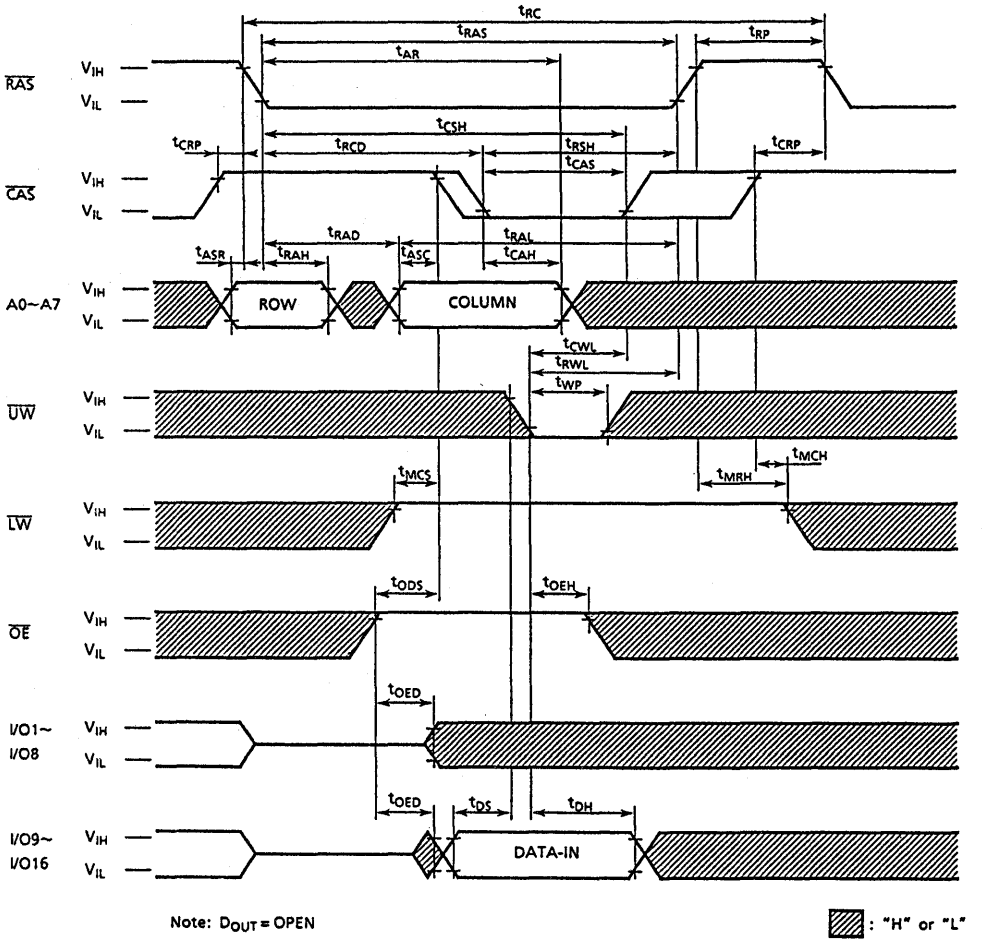
Note: D_{OUT} = OPEN

▨: "H" or "L"

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



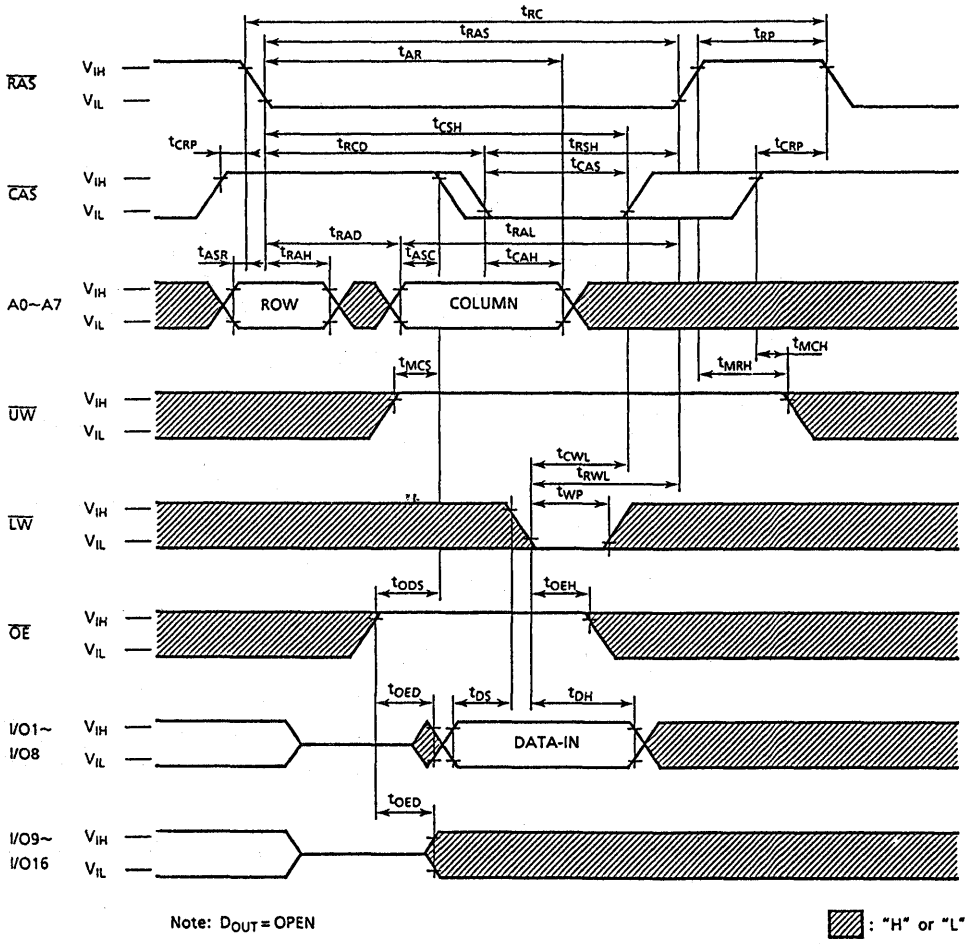
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

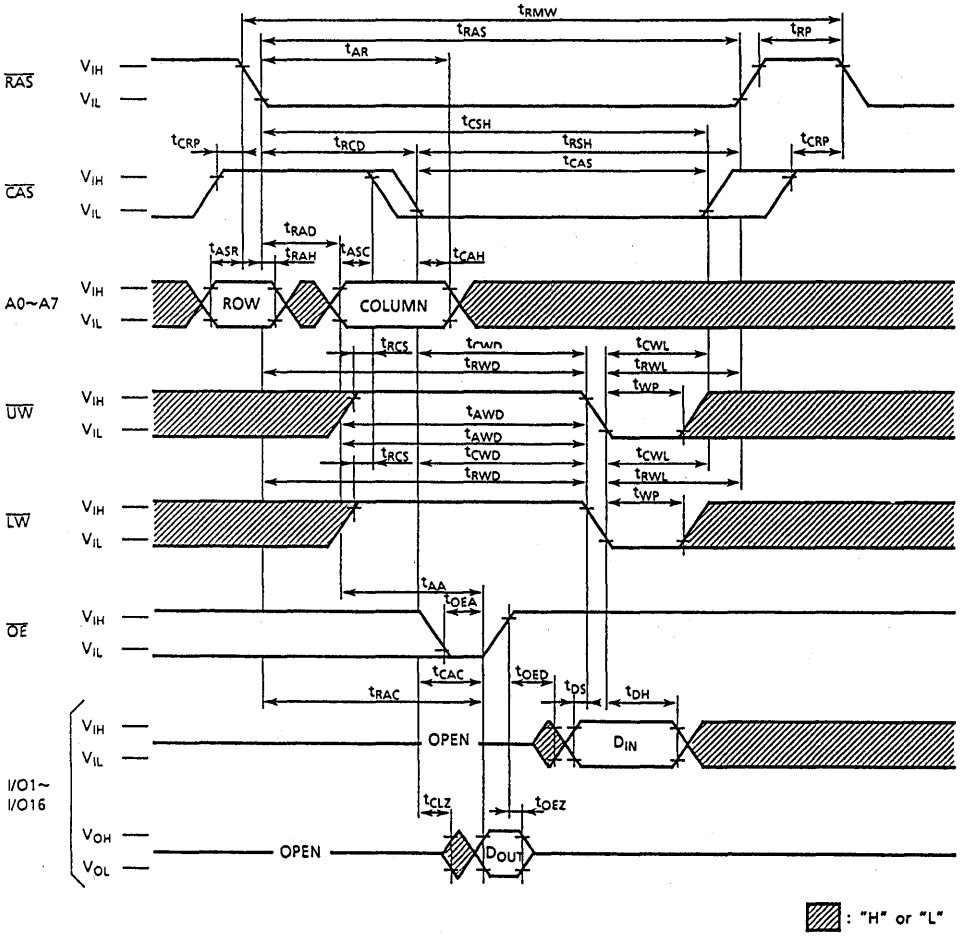
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



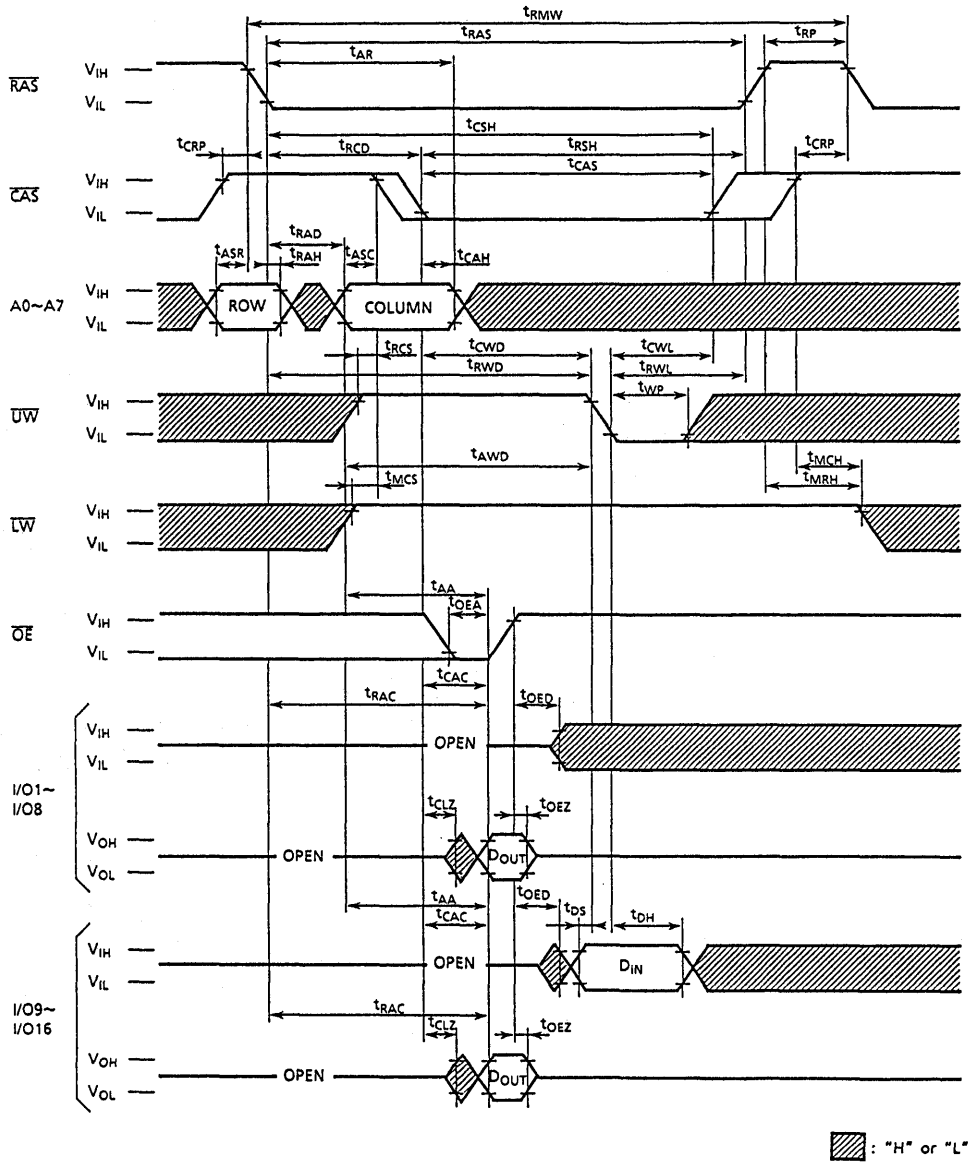
Note: D_{OUT} = OPEN

▨: "H" or "L"

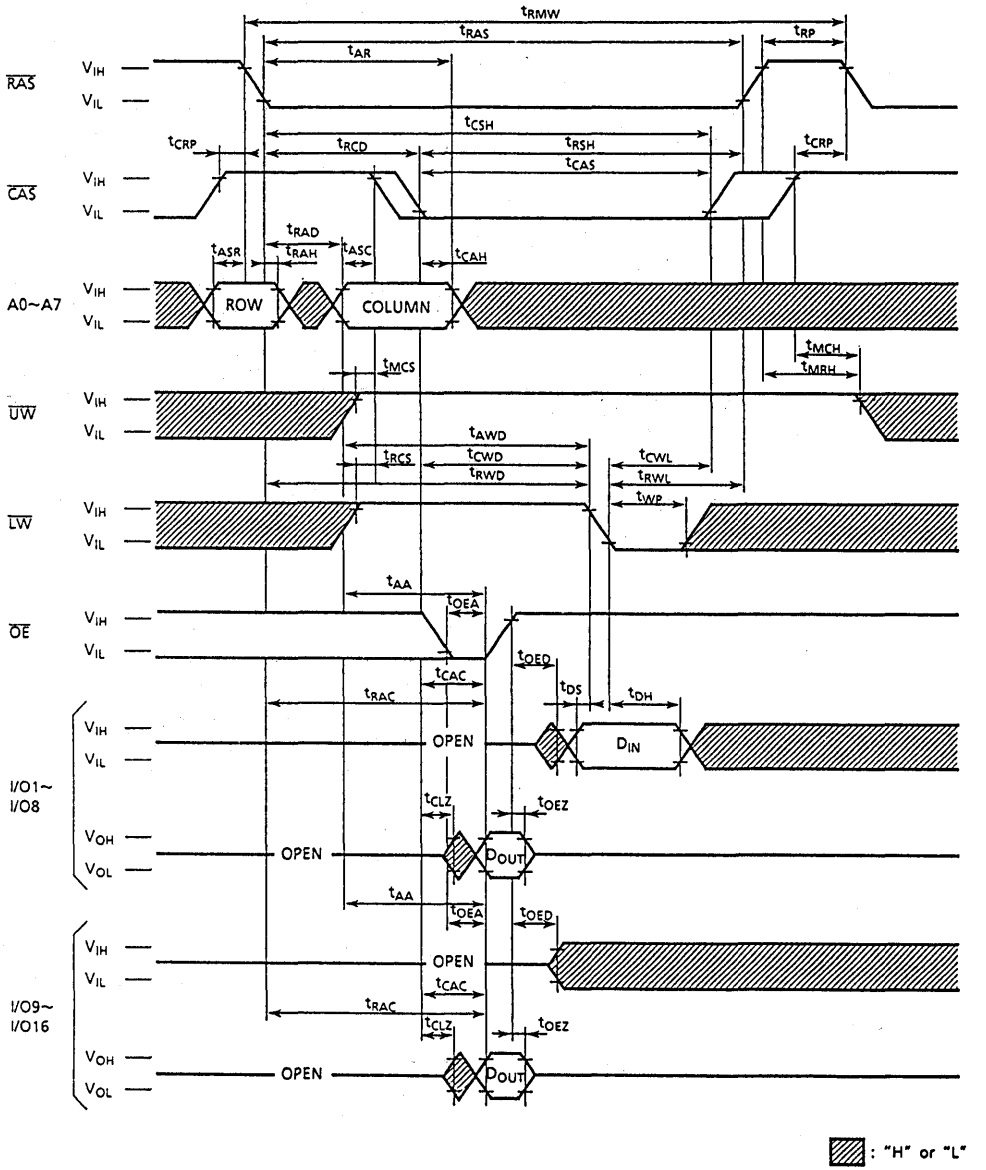
READ-MODIFY-WRITE CYCLE



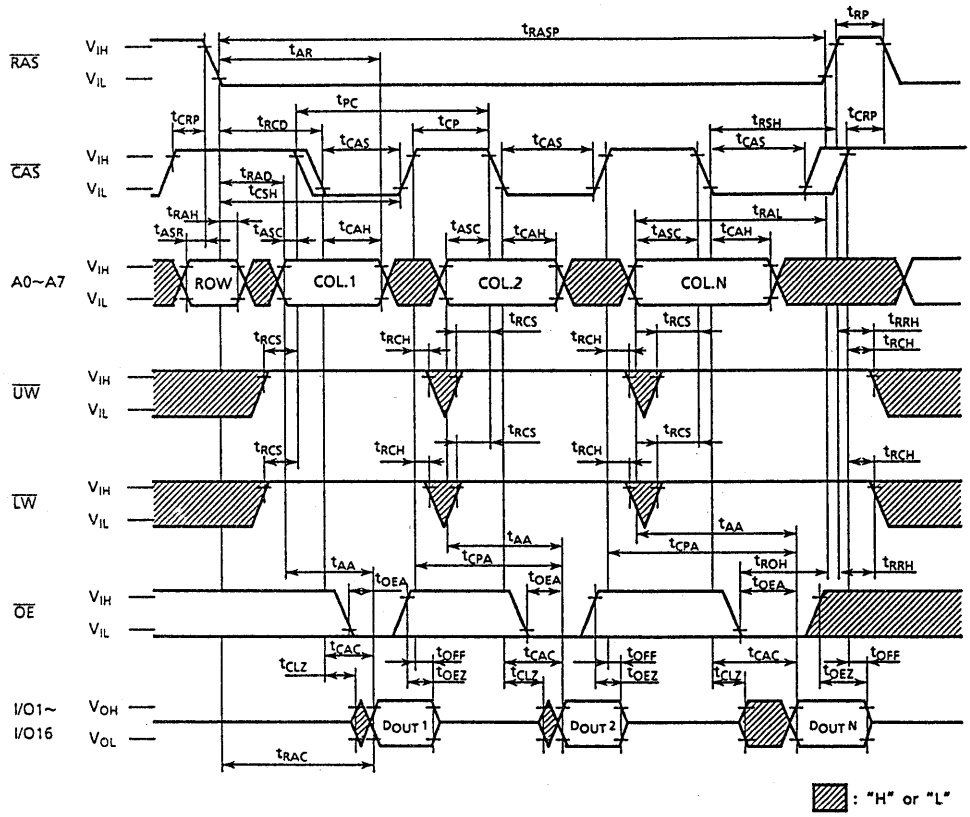
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE

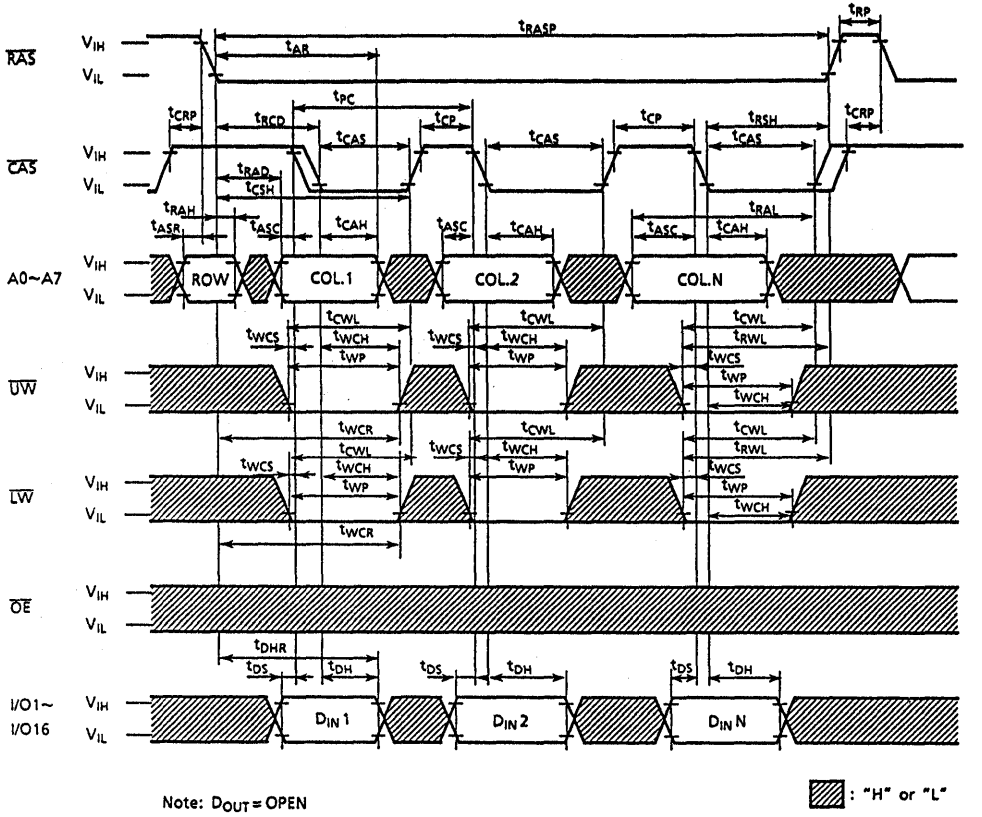


FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

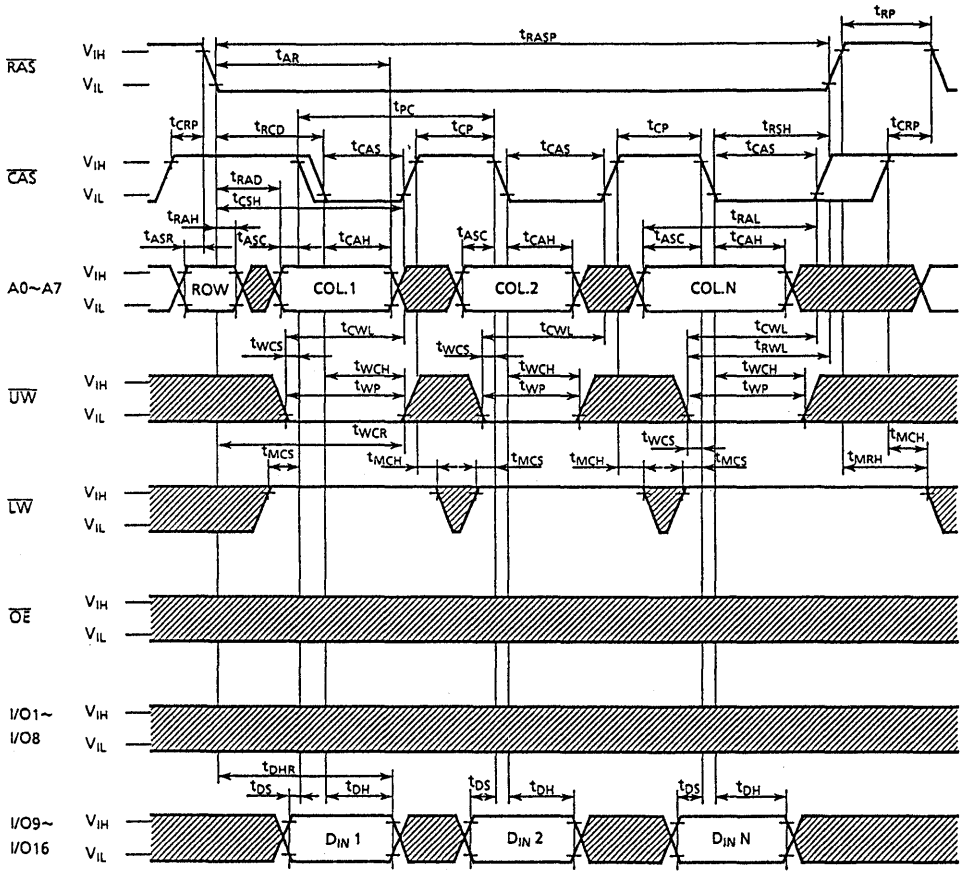
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

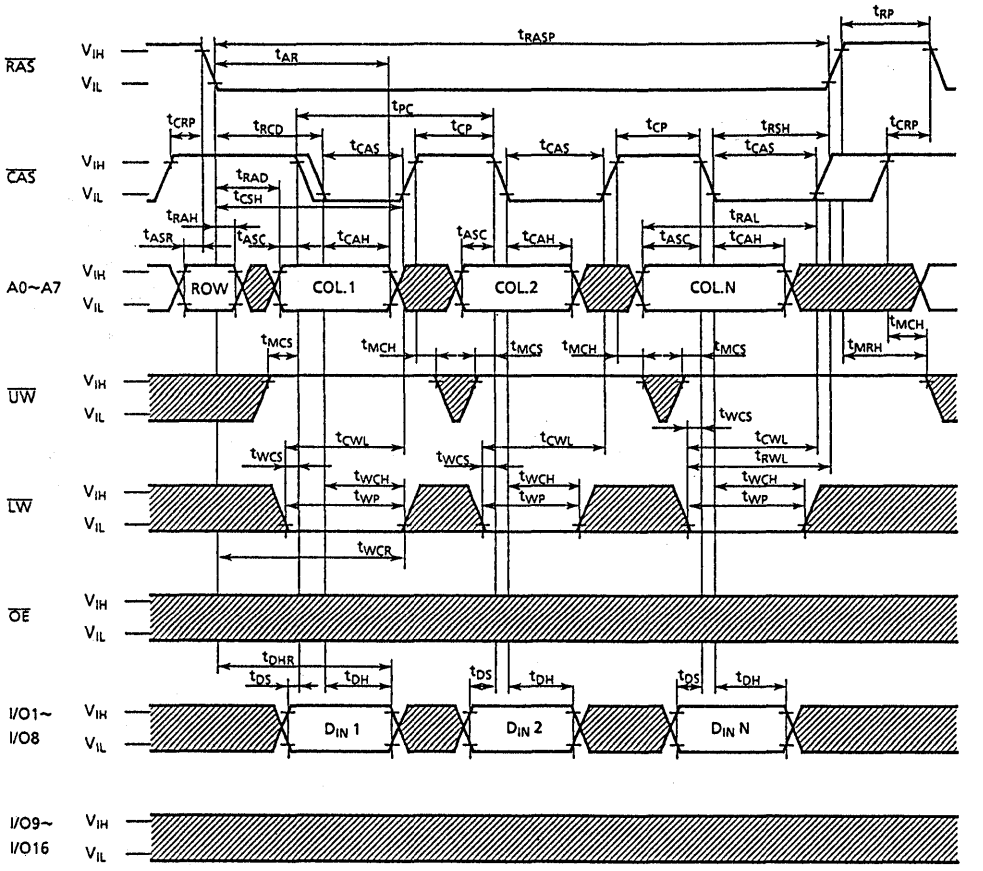
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

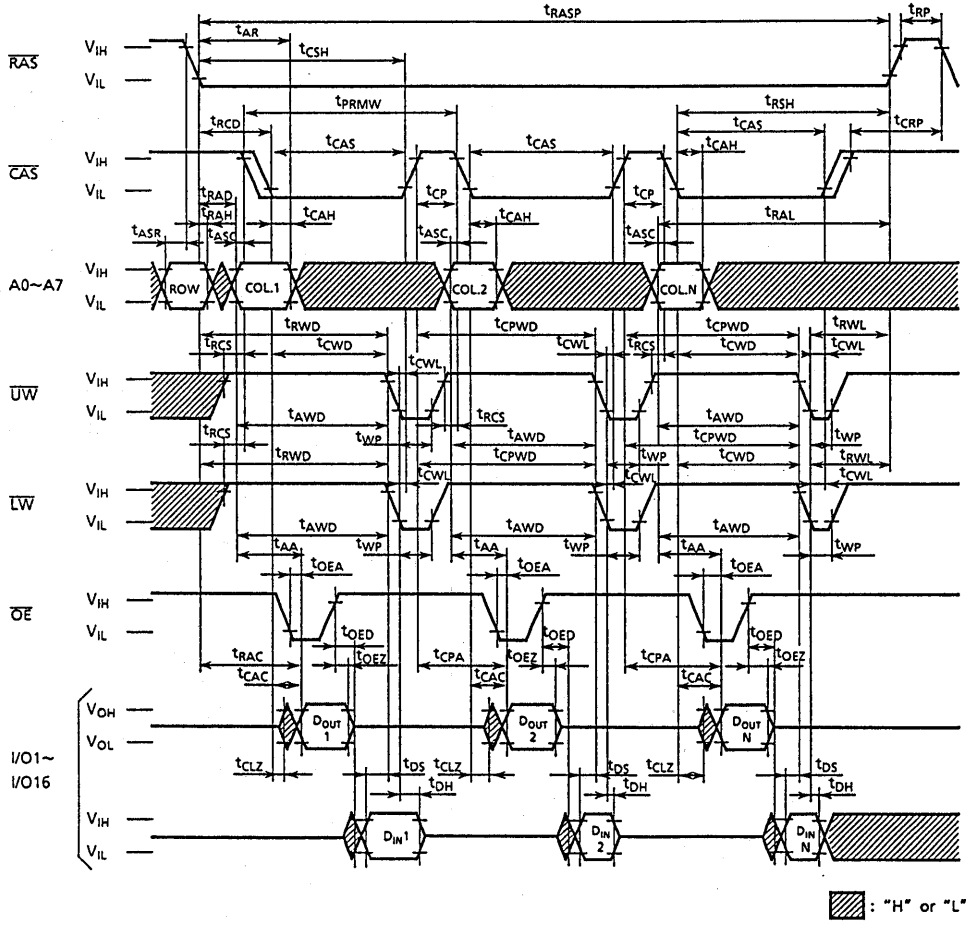
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



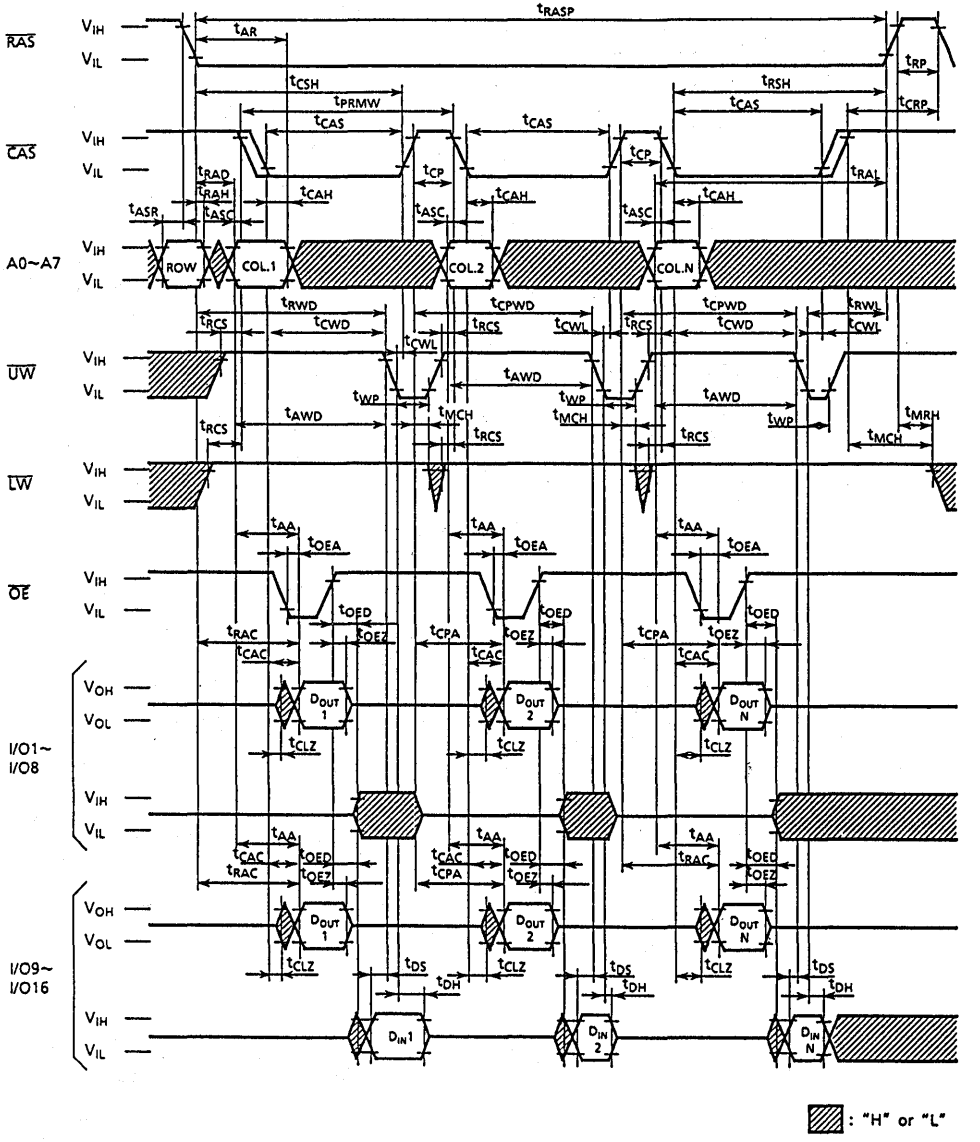
Note: D_{OUT} = OPEN

▨: "H" or "L"

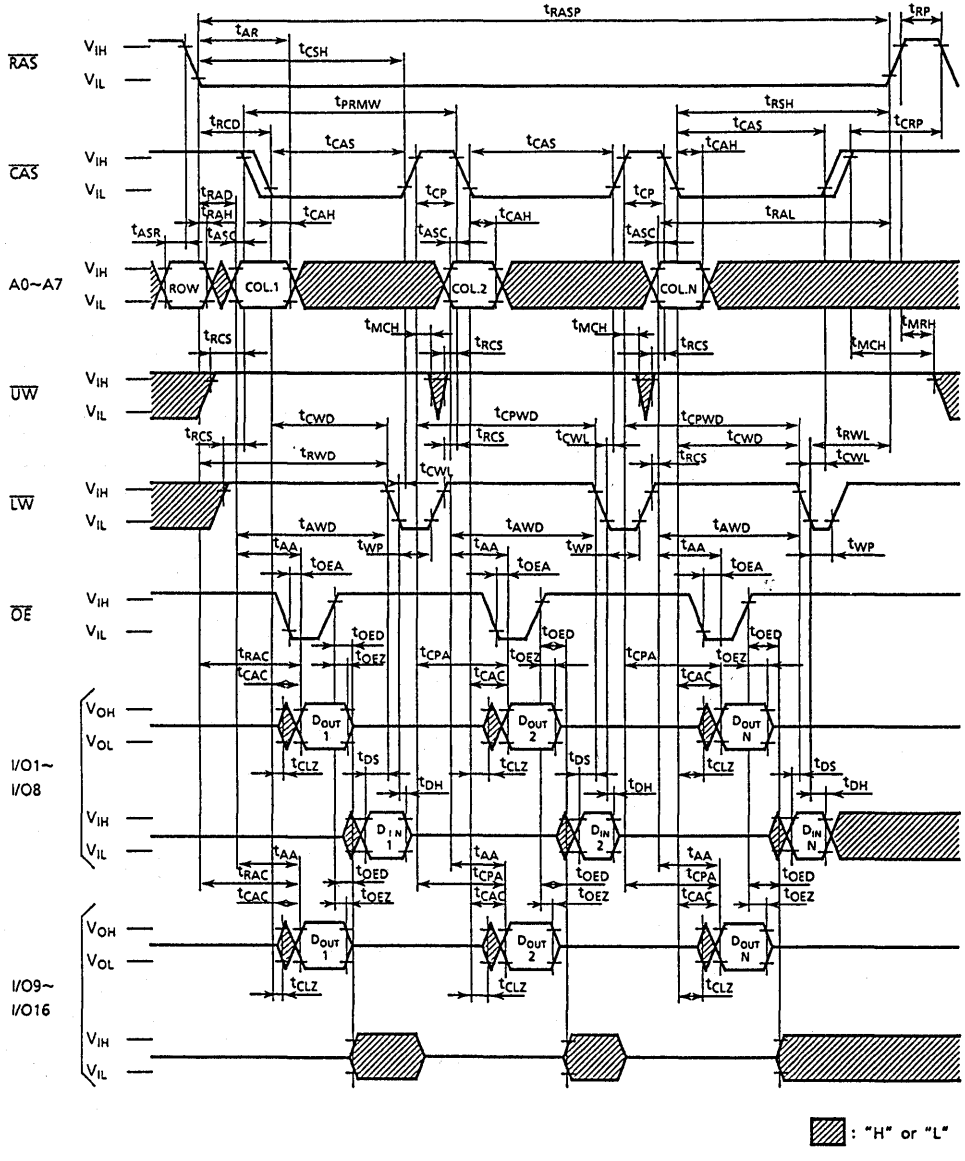
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



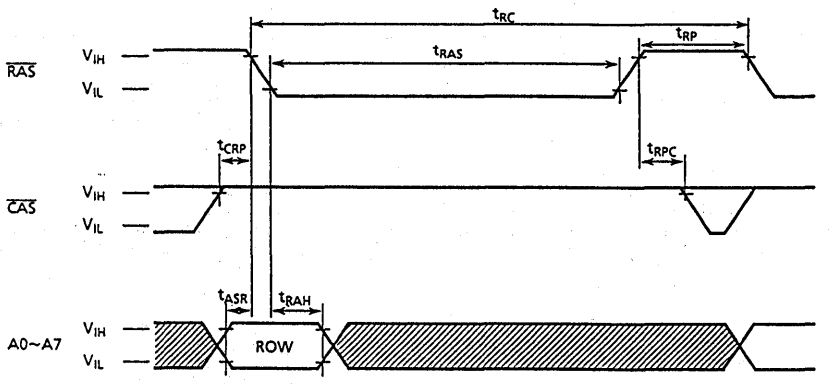
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



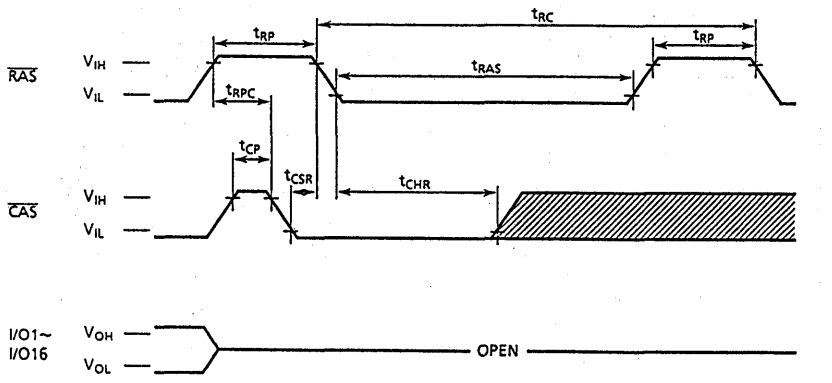
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

▨ : "H" or "L"

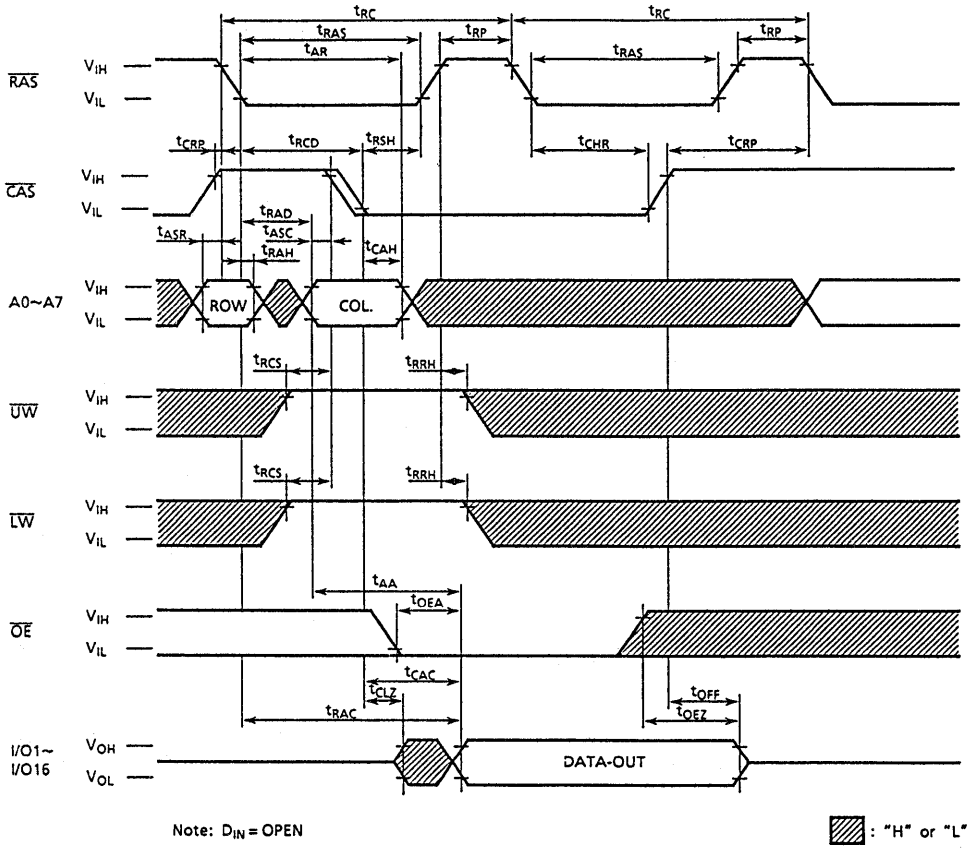
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0~A7 = "H" or "L"

▨ : "H" or "L"

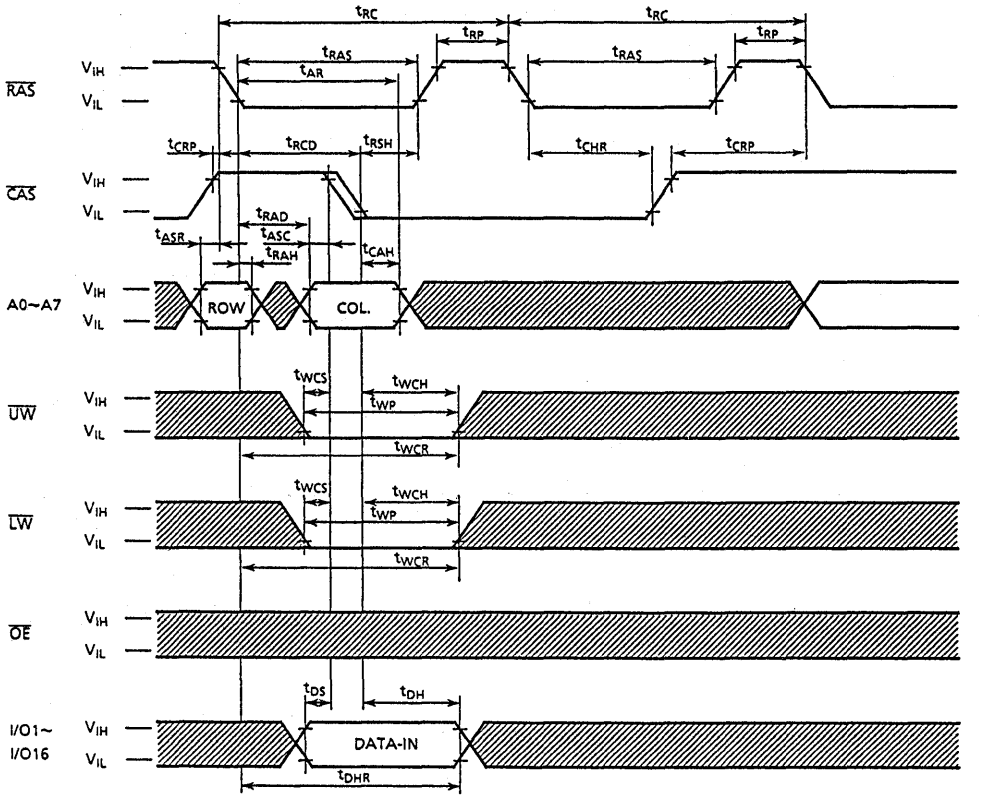
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

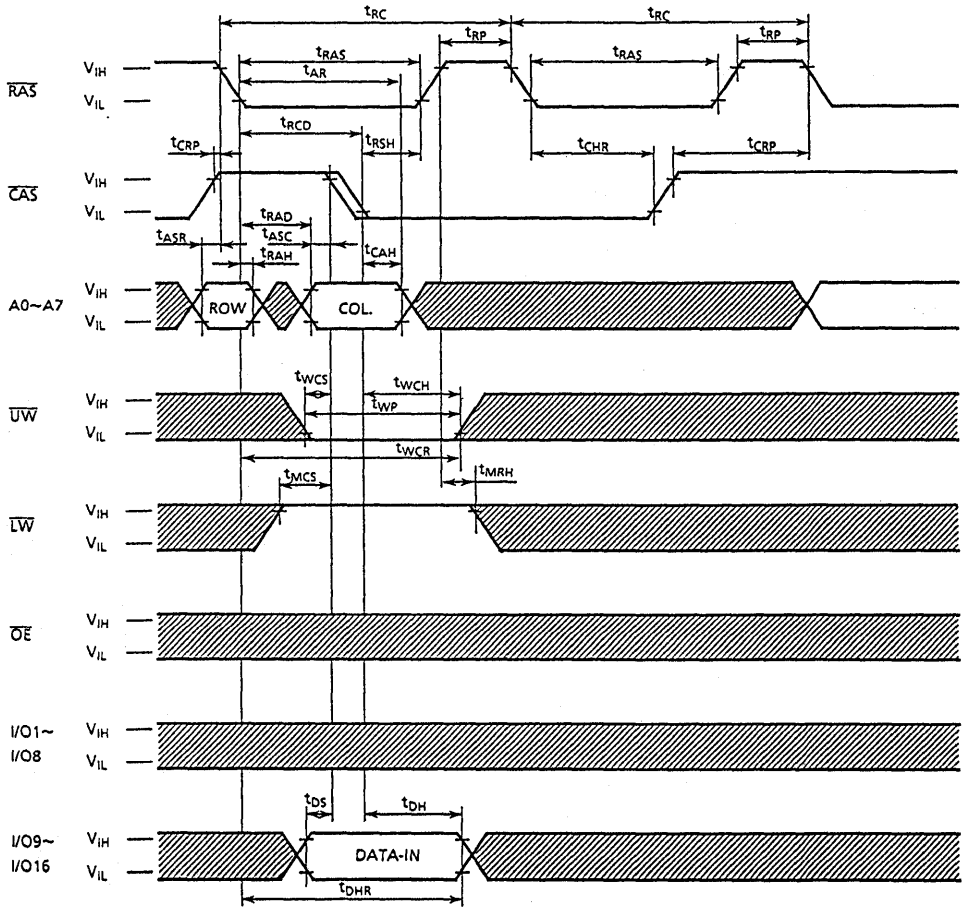
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

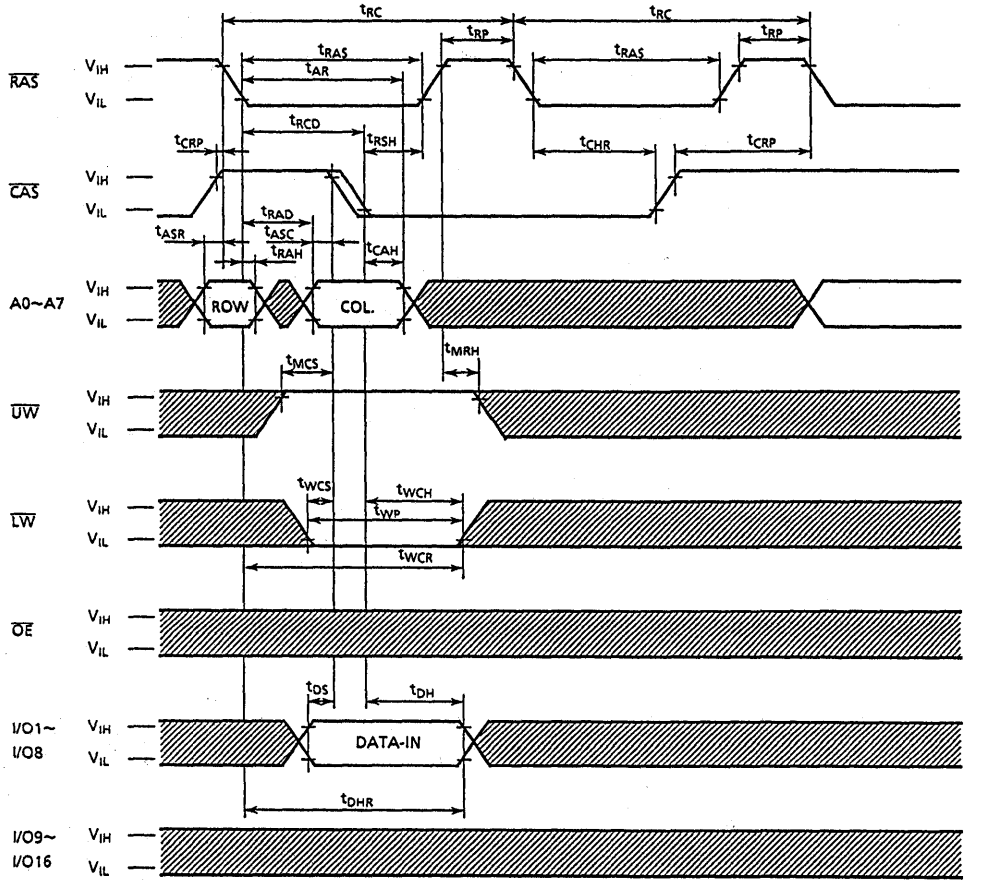
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

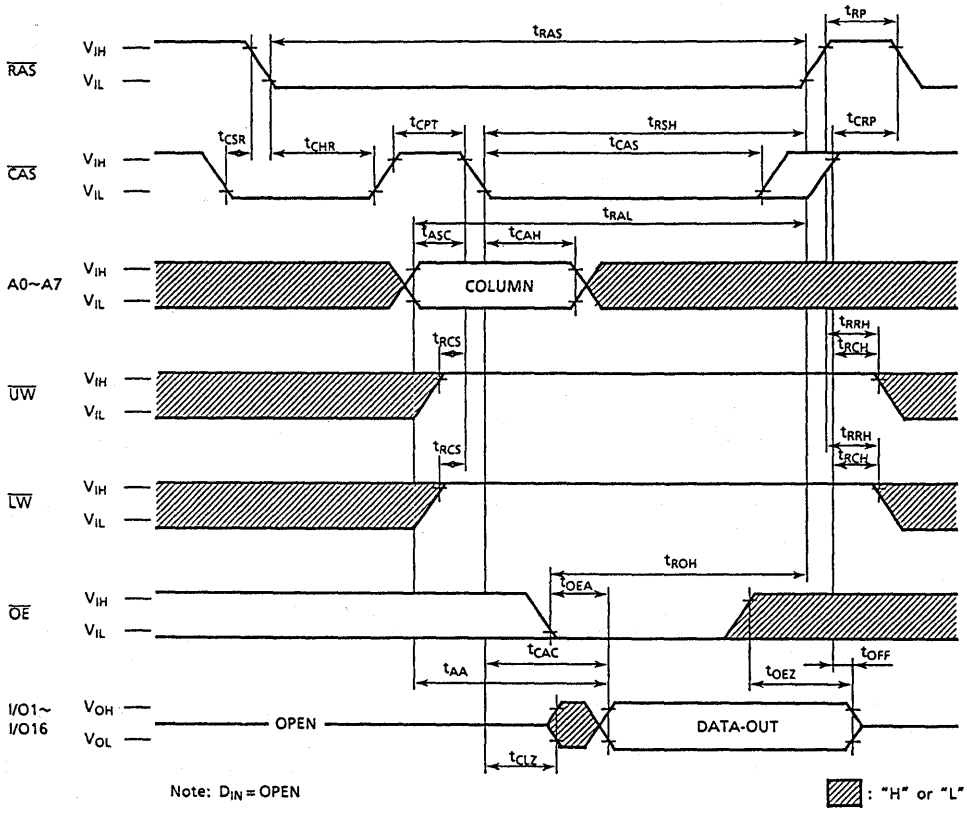
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



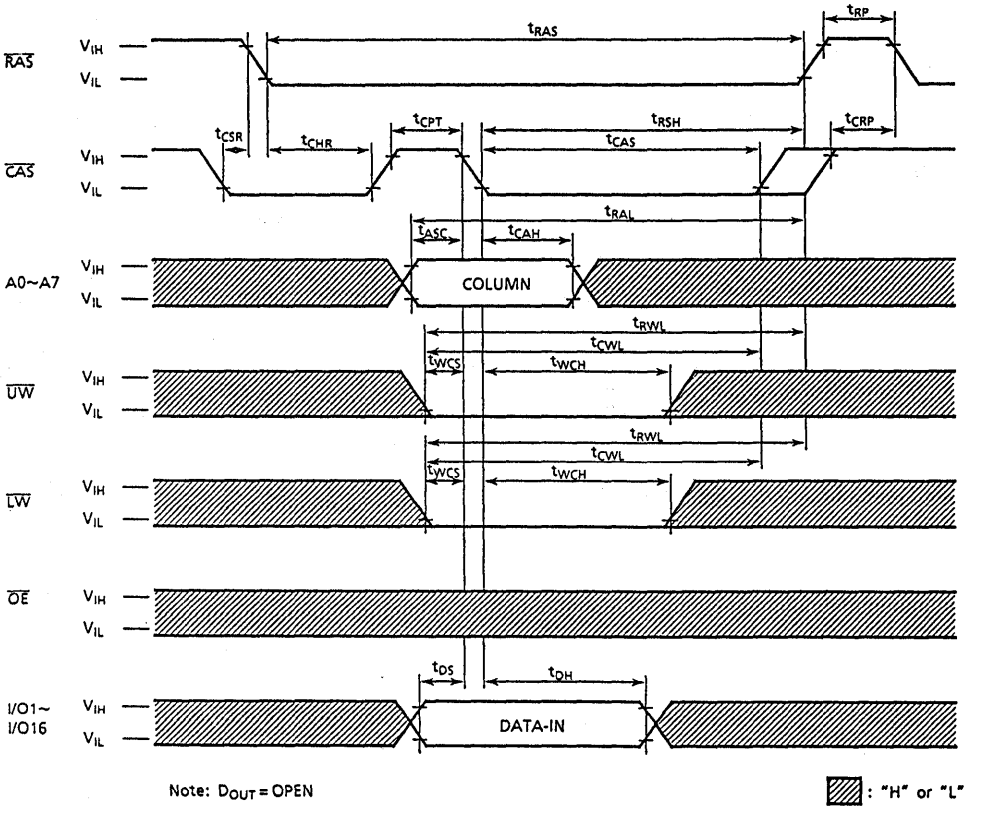
Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



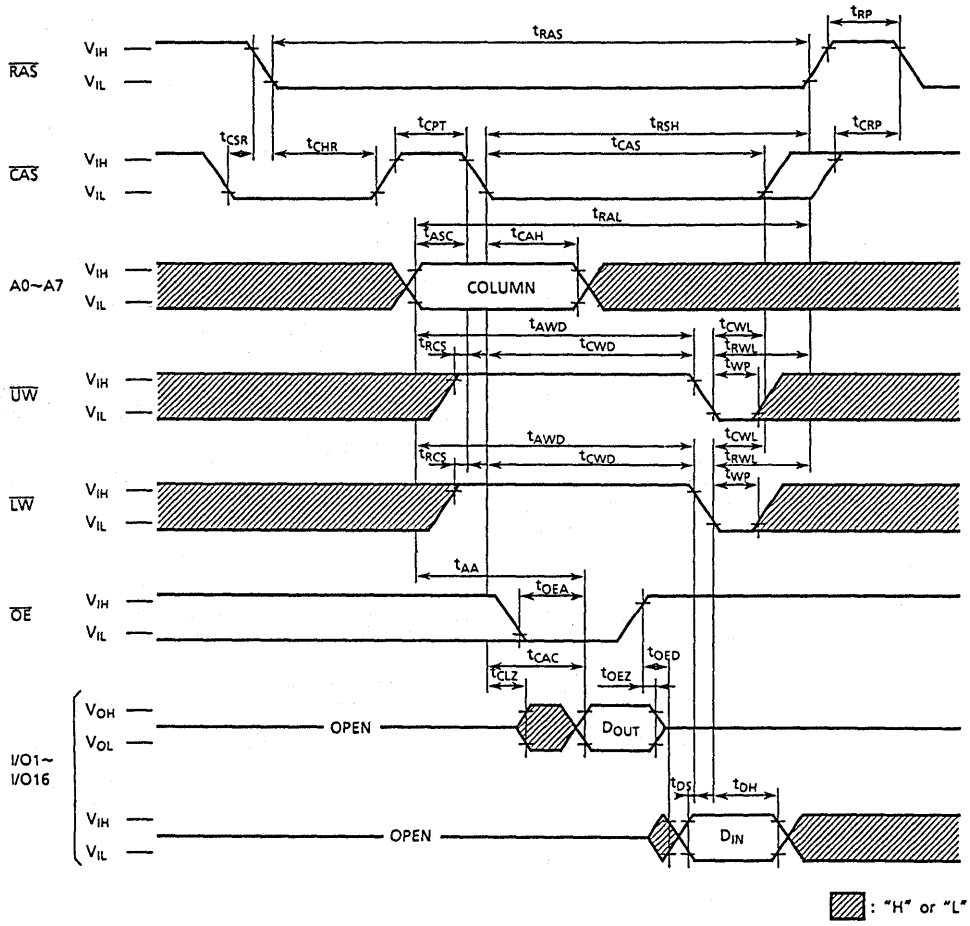
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



Note: D_{OUT} = OPEN

▨ : "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511664BJ/BZ are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{UW}$ and $\overline{LW}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{LW}$ strobes data on I/O1~I/O8 into the on-chip data latch. And the falling edge of $\overline{CAS}$ or $\overline{UW}$ strobes data on I/O9~I/O16 into the on-chip data latch. In an early write cycle, $\overline{LW}$ and $\overline{UW}$ are brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In derayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{LW}$ and $\overline{UW}$ with setup and hold times referenced to these signals.

In derayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high inpedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

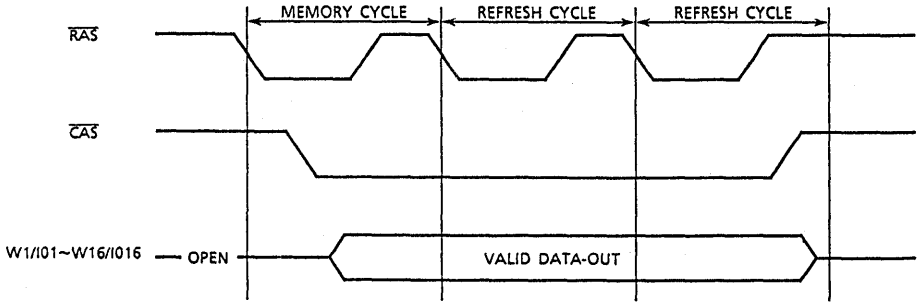
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511664BJ/BZ offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511664BJ/BZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511664BJ/BZ is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511664BJ/BZ can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

TENTATIVE DATA
65,536 WORD × 16 BIT DYNAMIC RAM

DESCRIPTION

The TC511664BJL/BZL is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511664BJL/BZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511664BJL/BZL to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

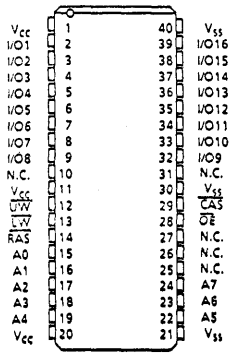
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511664BJL/BZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

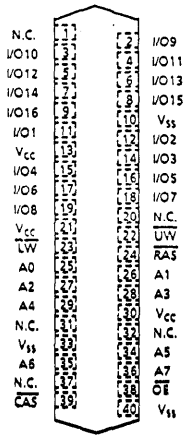
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511664BJL/BZL-80)
  495mW MAX. Operating (TC511664BJL/BZL-10)
  1.7mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Byte-Write and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/32ms
- Package TC511664BJL :SOJ40-P-400
  TC511664BZL :ZIP40-P-475

PIN CONNECTION (TOP VIEW)

Plastic SOJ



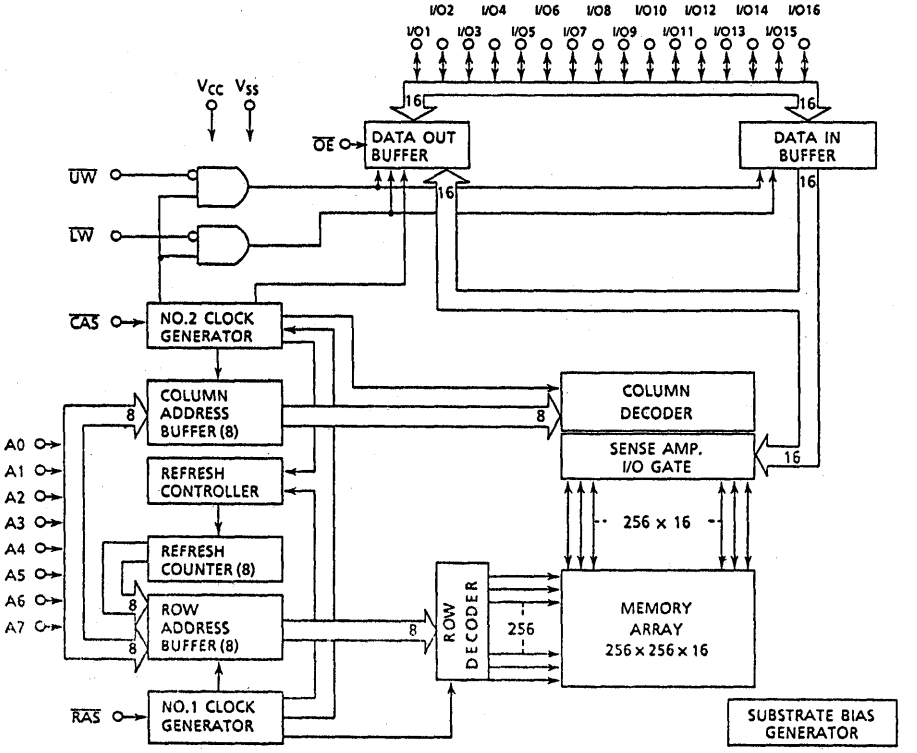
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
I/O1~I/O16	Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (I/O1~I/O16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511664BJL/BZL-80	–	115	mA	3, 4, 5
		TC511664BJL/BZL-10	–	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511664BJL/BZL-80	–	115	mA	3, 5
		TC511664BJL/BZL-10	–	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511664BJL/BZL-80	–	70	mA	3, 4, 5
		TC511664BJL/BZL-10	–	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	300	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511664BJL/BZL-80	–	115	mA	3
		TC511664BJL/BZL-10	–	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{UW}$,$\overline{LW}$ = V_{CC} – 0.2V or 0.2V, A0~A7 = V_{CC} – 0.2V or 0.2V, I/O1~16 = V_{CC} – 0.2V,0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN.~1µs)		–	400	µA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2.5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC511664BJL/BZL-80		TC511664BJL/BZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	35	ns	10,15
t_{AA}	Access Time from Column Address	–	45	–	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	65	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	ns	13

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511664BJL/BZL-80		TC511664BJL/BZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	32	–	32	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	65	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	10	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{MCS}	Masked Write Set-Up Time	0	–	0	–	ns	
t_{MRH}	Masked Write Hold time Referenced to $\overline{RAS}$	0	–	0	–	ns	
t_{MCH}	Masked Write Hold time Referenced to $\overline{CAS}$	0	–	0	–	ns	

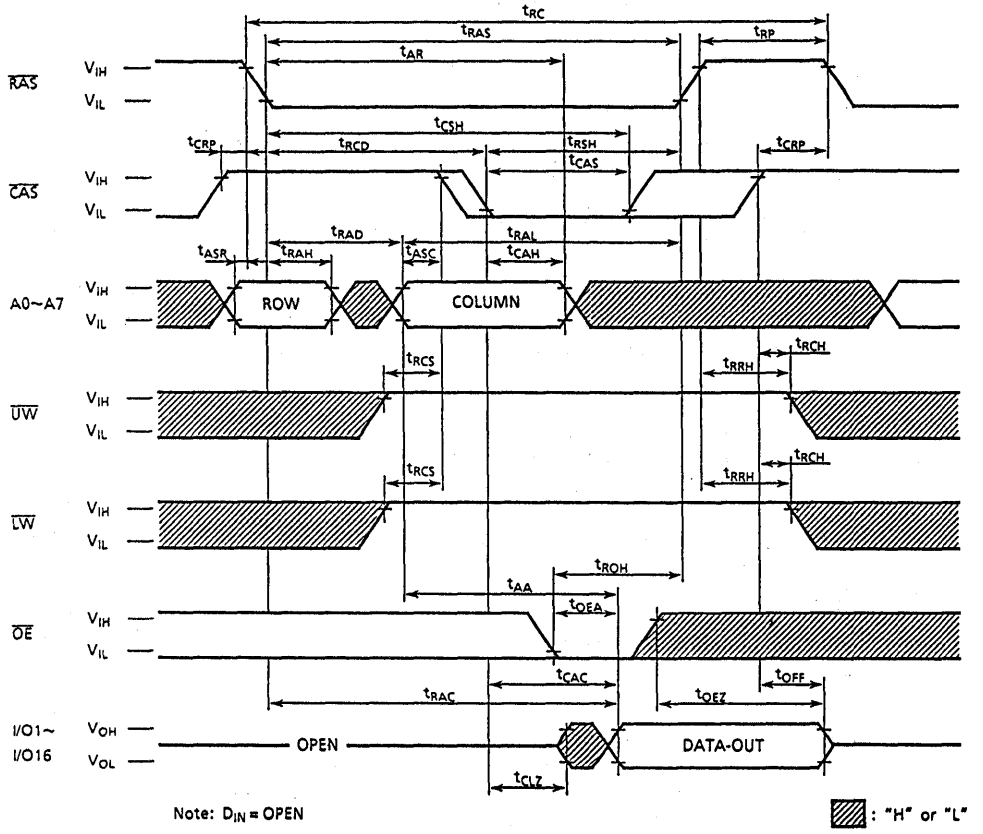
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (I/O1~I/O16)	–	7	pF

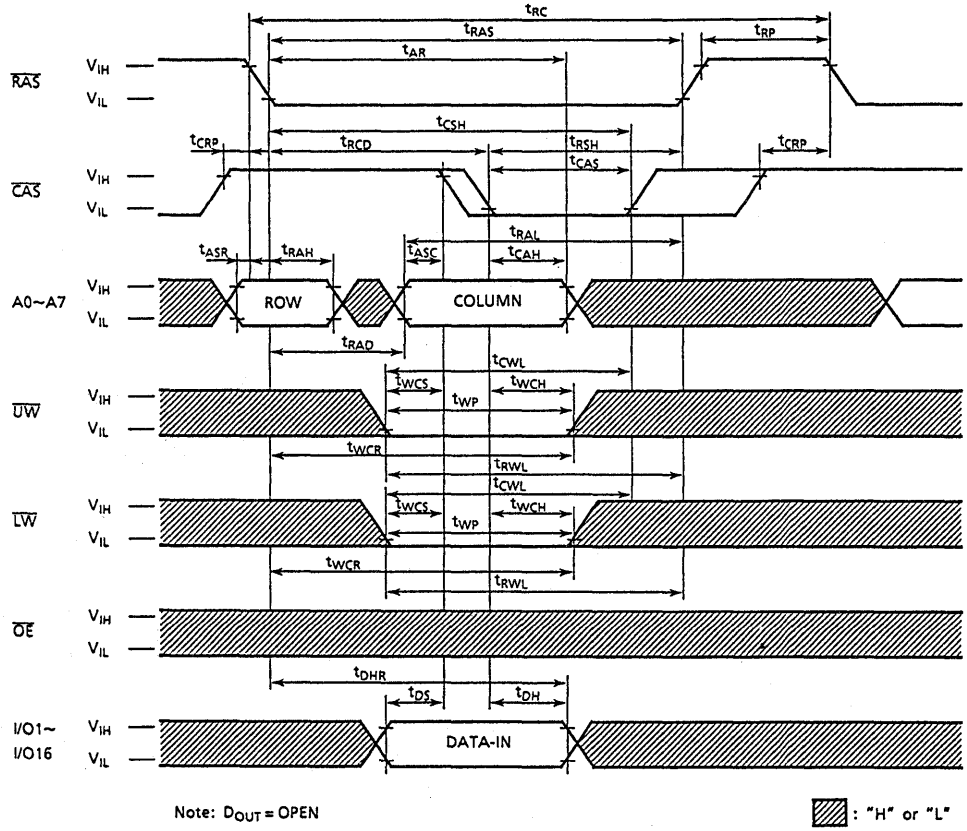
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T=5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
   Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 1 TTL load and 50pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{UW}$, $\overline{LW}$ leading edge in read-modify-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCAS
tCRP
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A7
ROW
COLUMN
tRCS
tRRH
tRCH
UW
LW
tROH
tAA
tOEA
OE
tCAC
tOFF
tRAC
tOEZ
I/O1~
I/O16
VOH
VOL
OPEN
DATA-OUT
tCLZ
Note: DIN = OPEN
: "H" or "L"

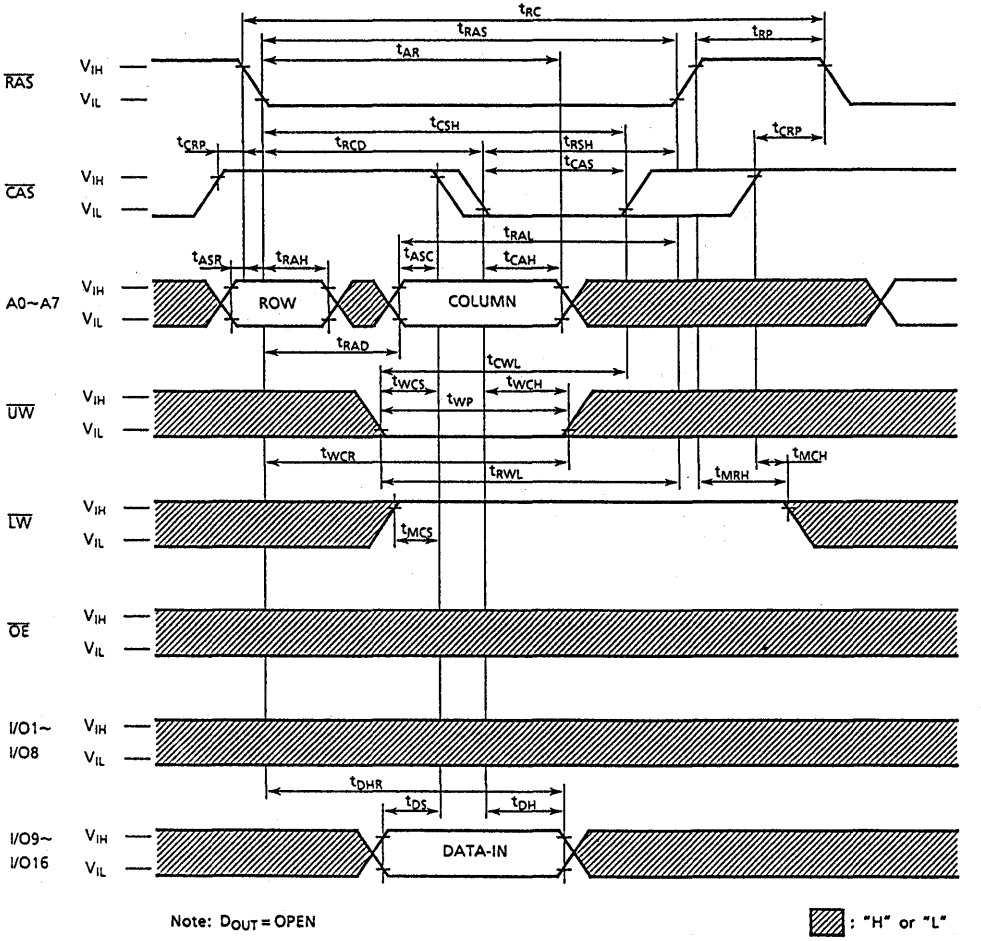
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

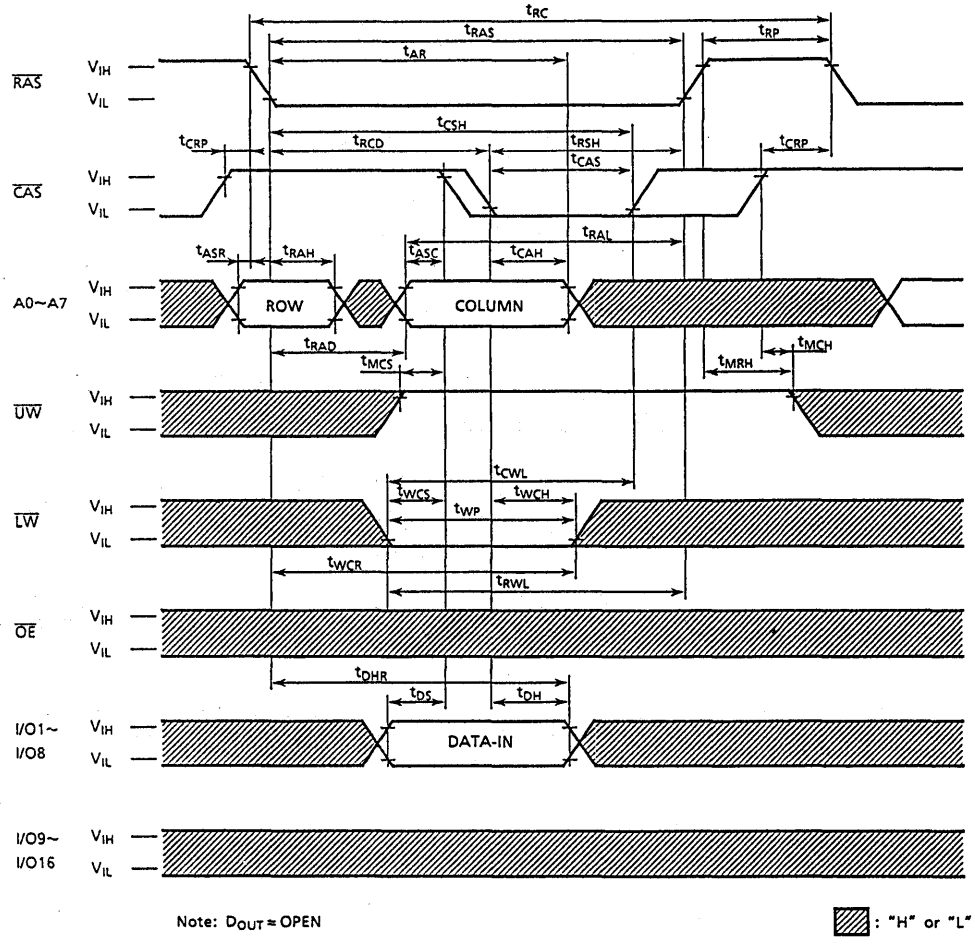
UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

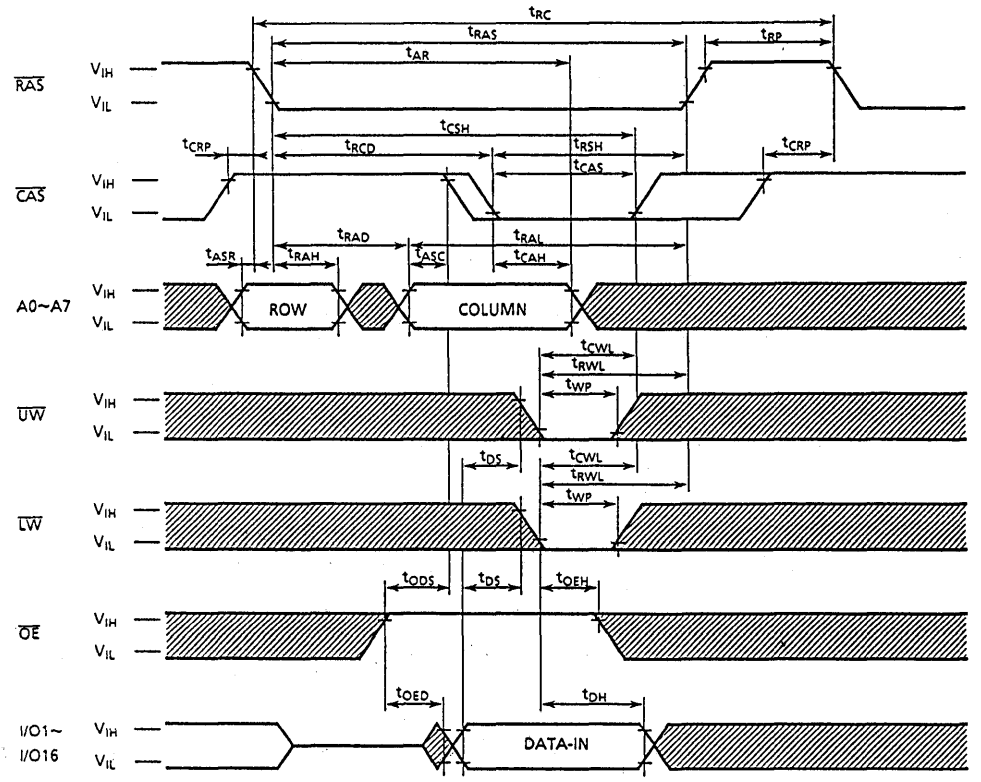
LOWER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

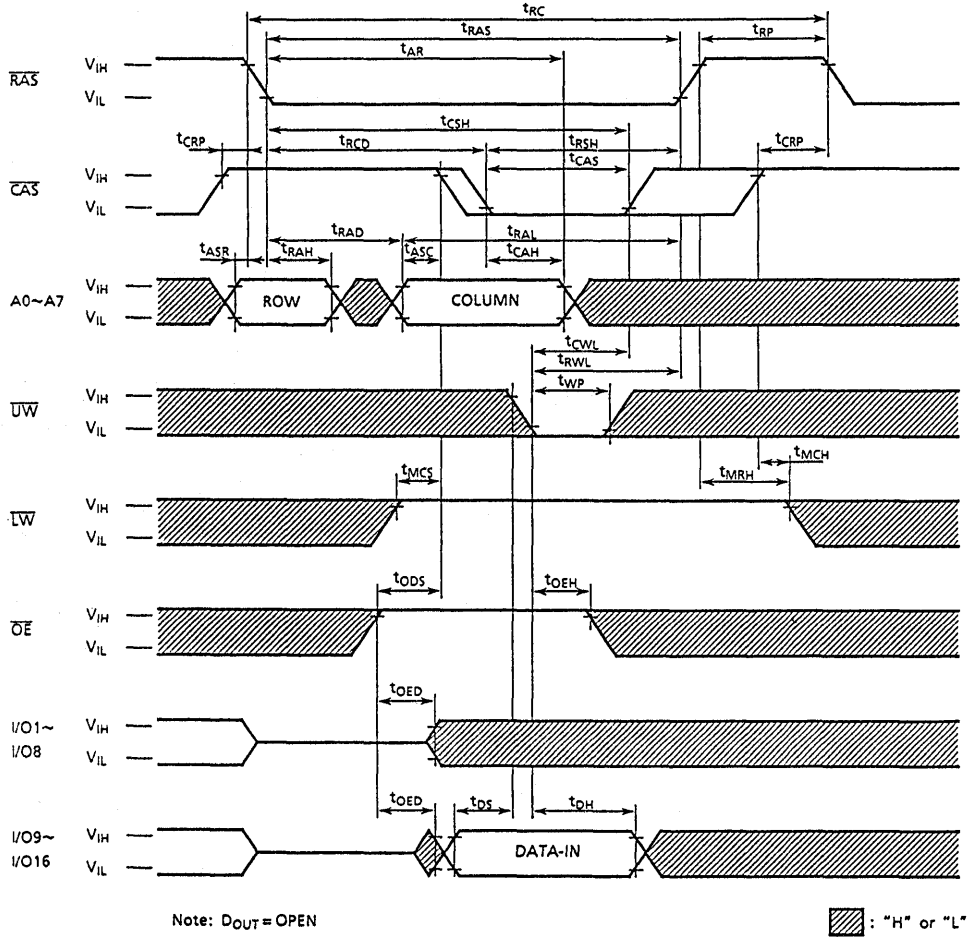
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

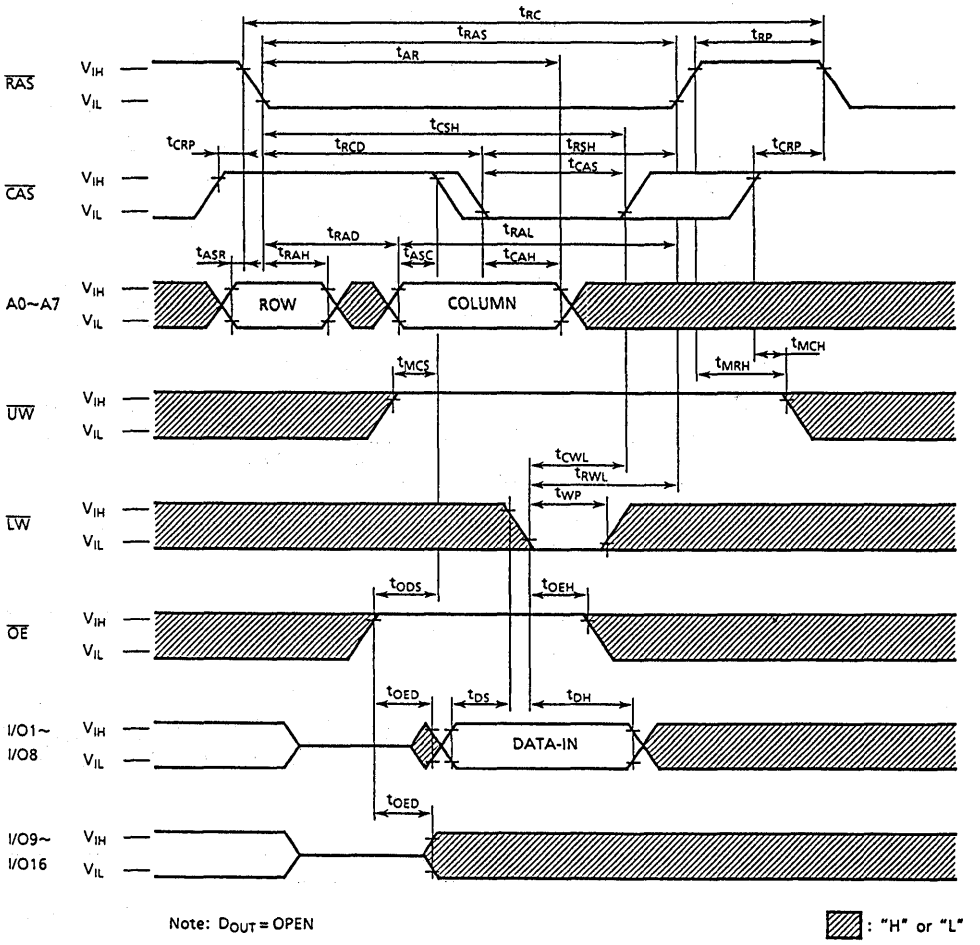
UPPER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

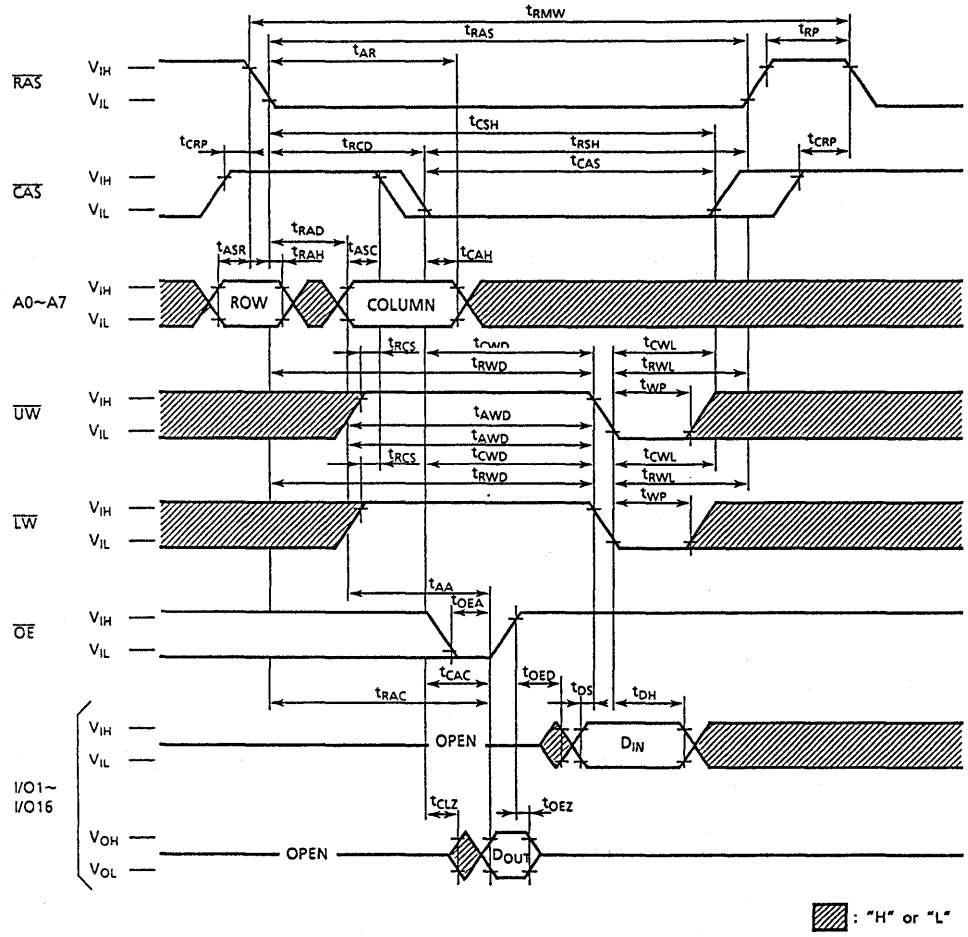
LOWER BYTE WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



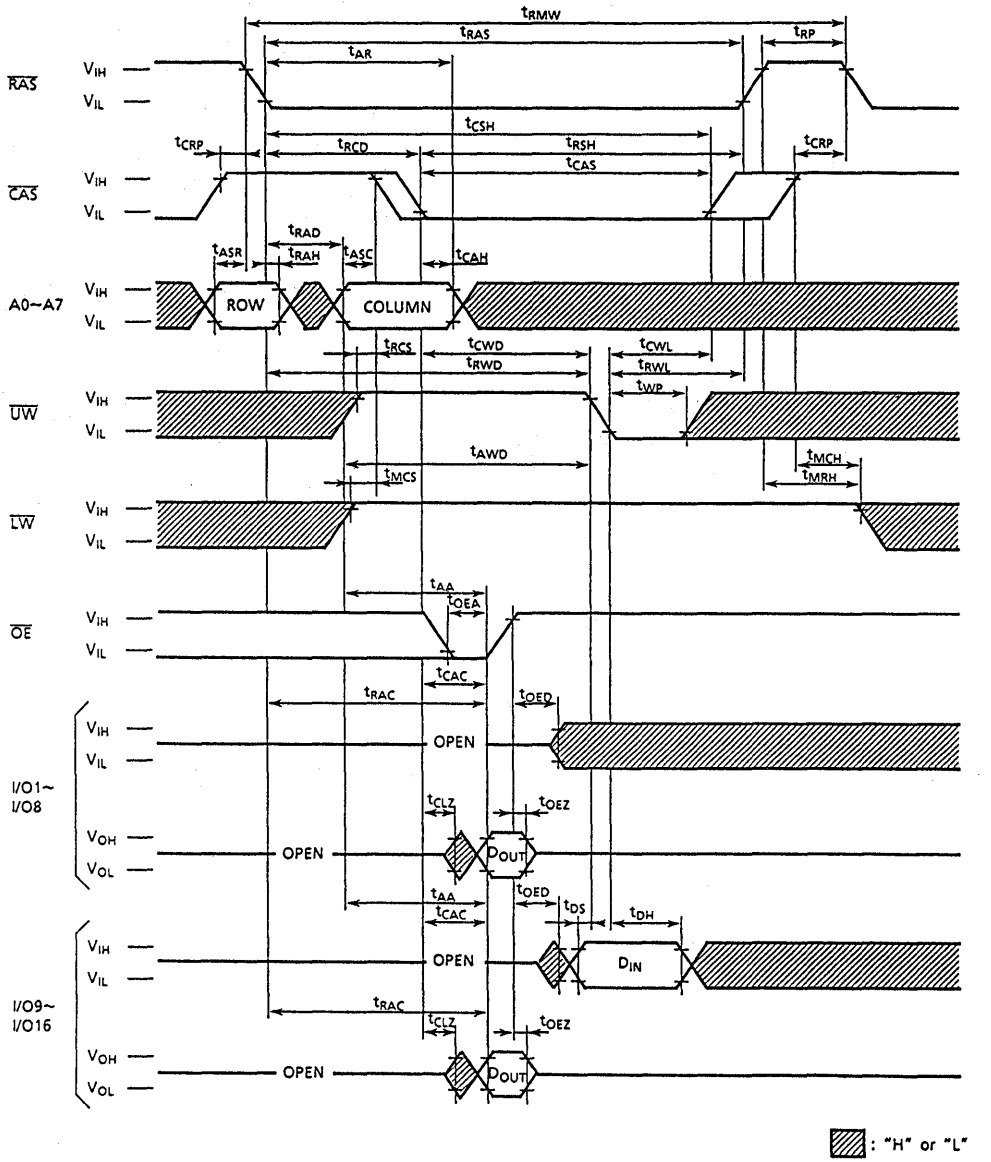
Note: D_{OUT} = OPEN

▨: "H" or "L"

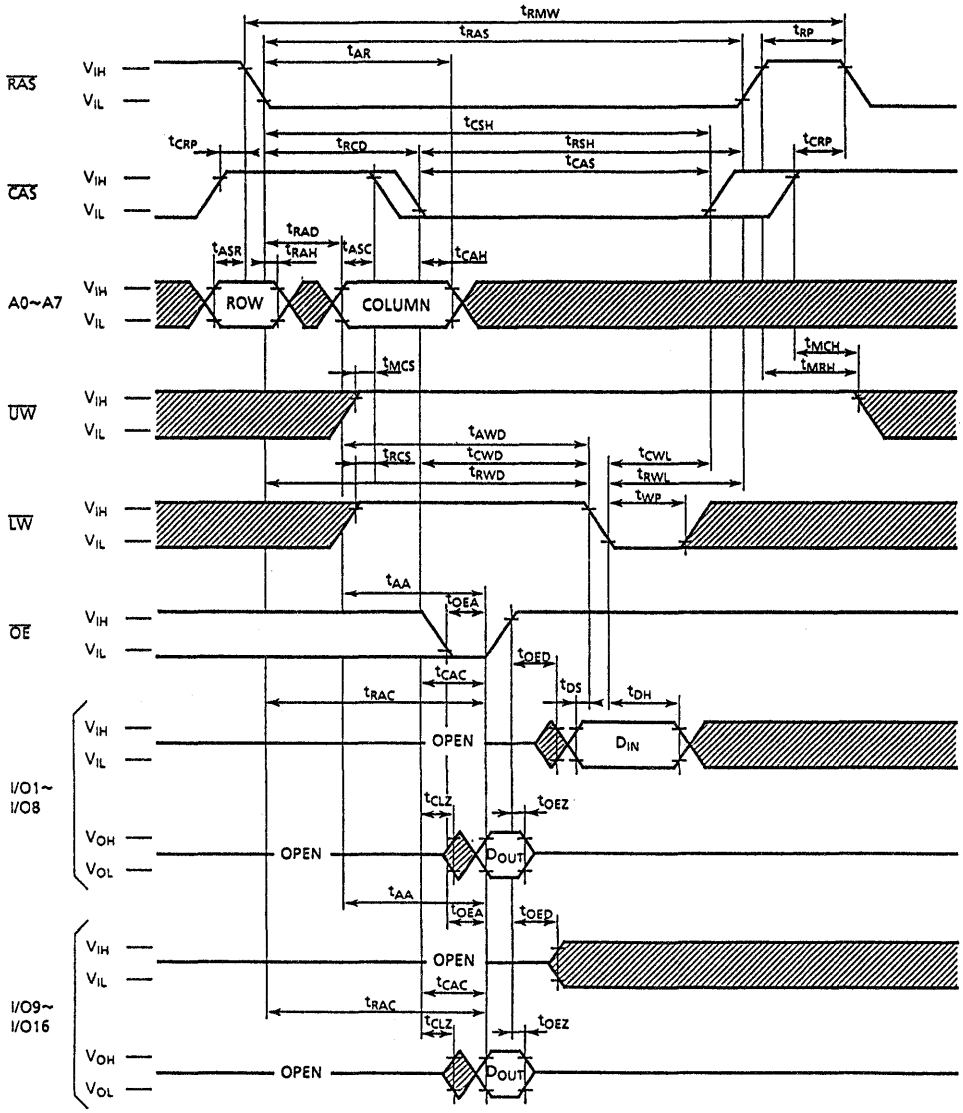
READ-MODIFY-WRITE CYCLE



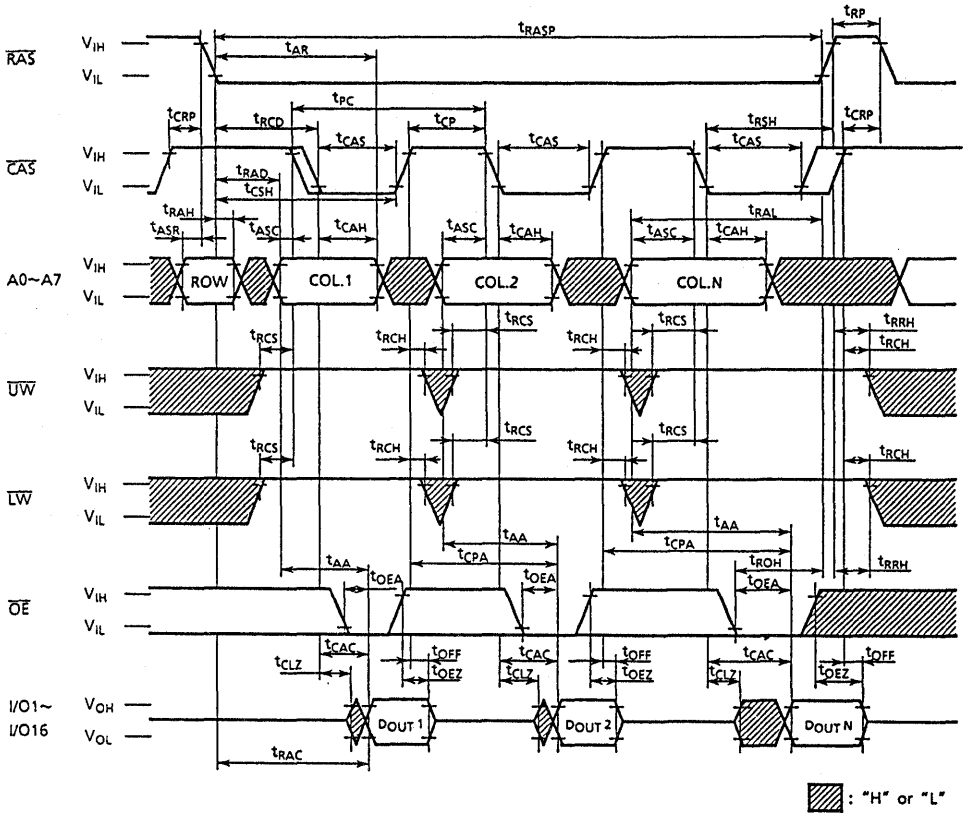
READ-MODIFY-UPPER-BYTE-WRITE CYCLE



READ-MODIFY-LOWER-BYTE-WRITE CYCLE

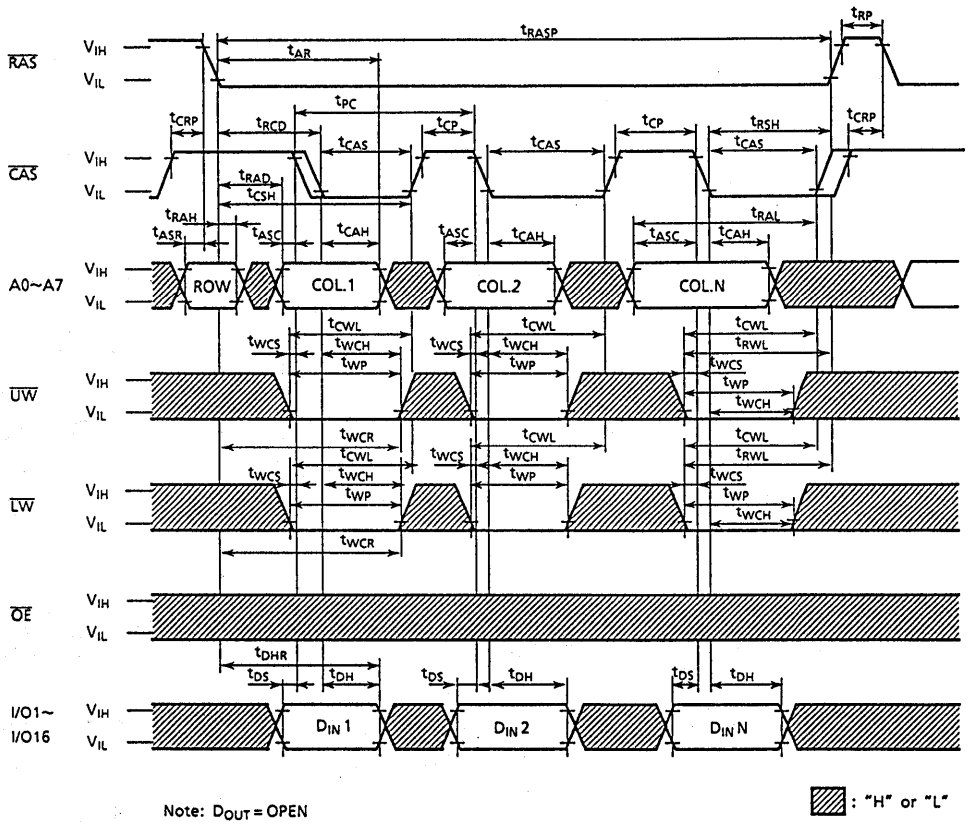


FAST PAGE MODE READ CYCLE

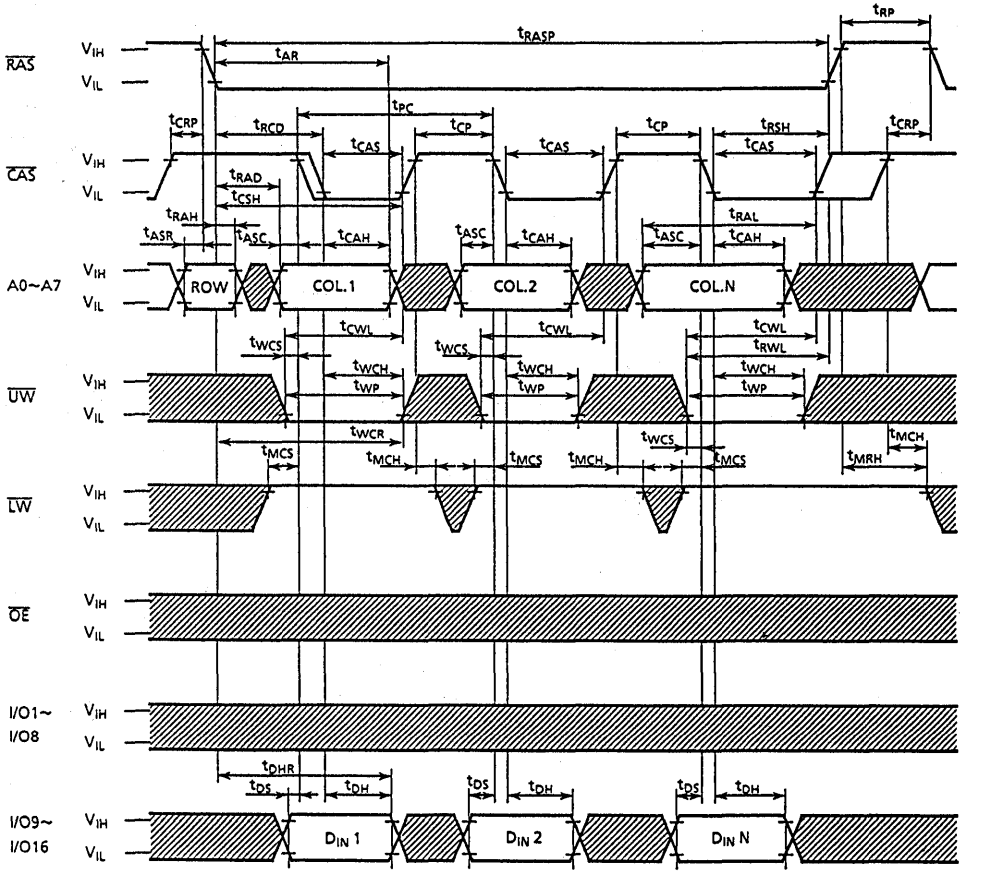


Note: D_{IN} = OPEN

FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



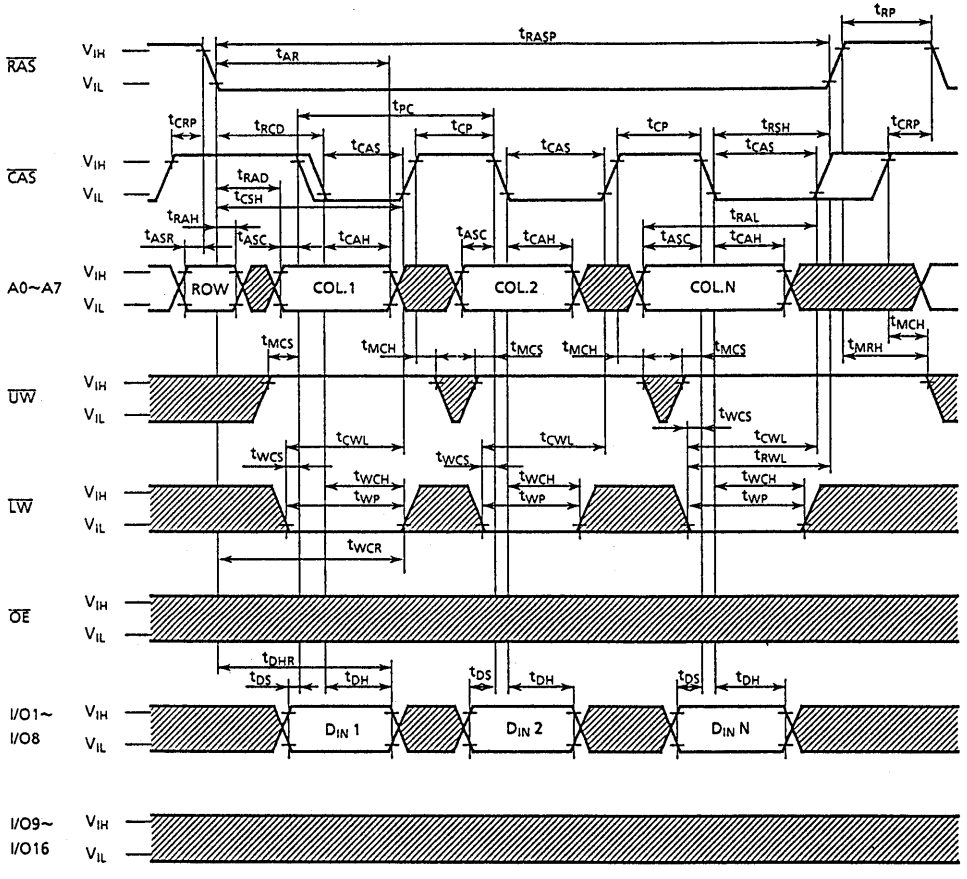
FAST PAGE MODE UPPER BYTE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

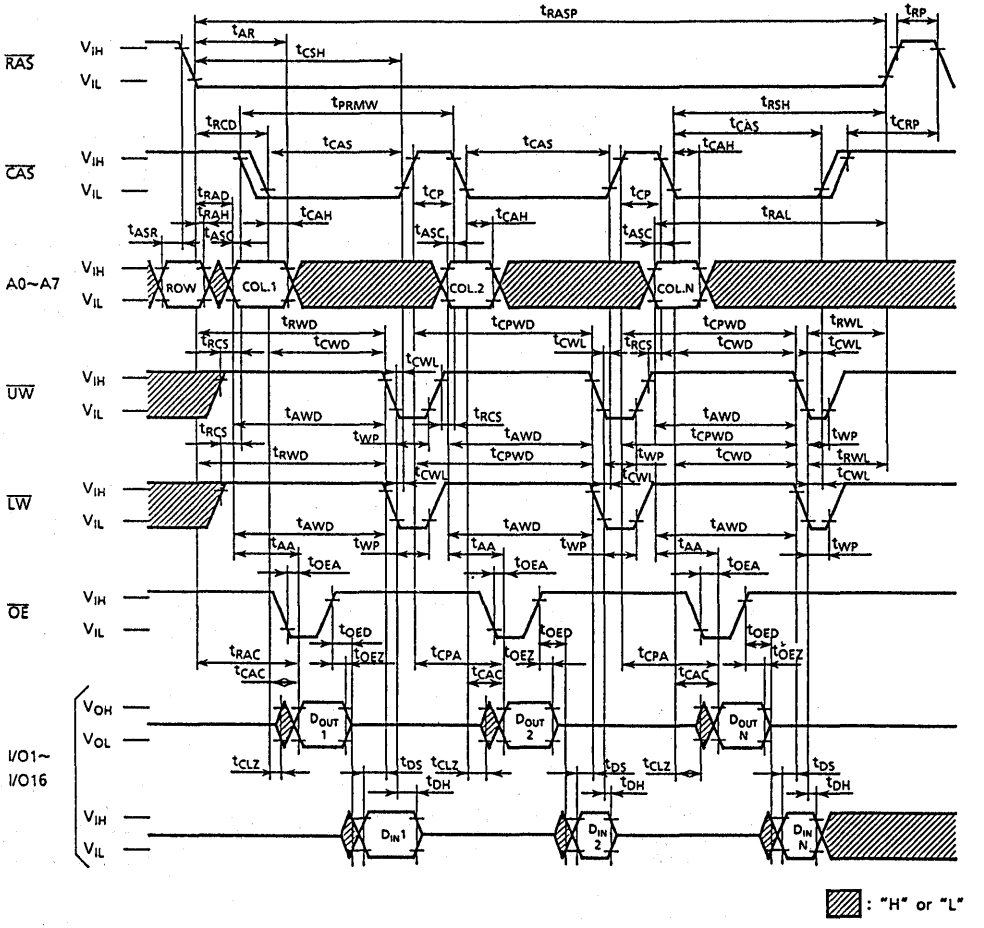
FAST PAGE MODE LOWER BYTE WRITE CYCLE (EARLY WRITE)



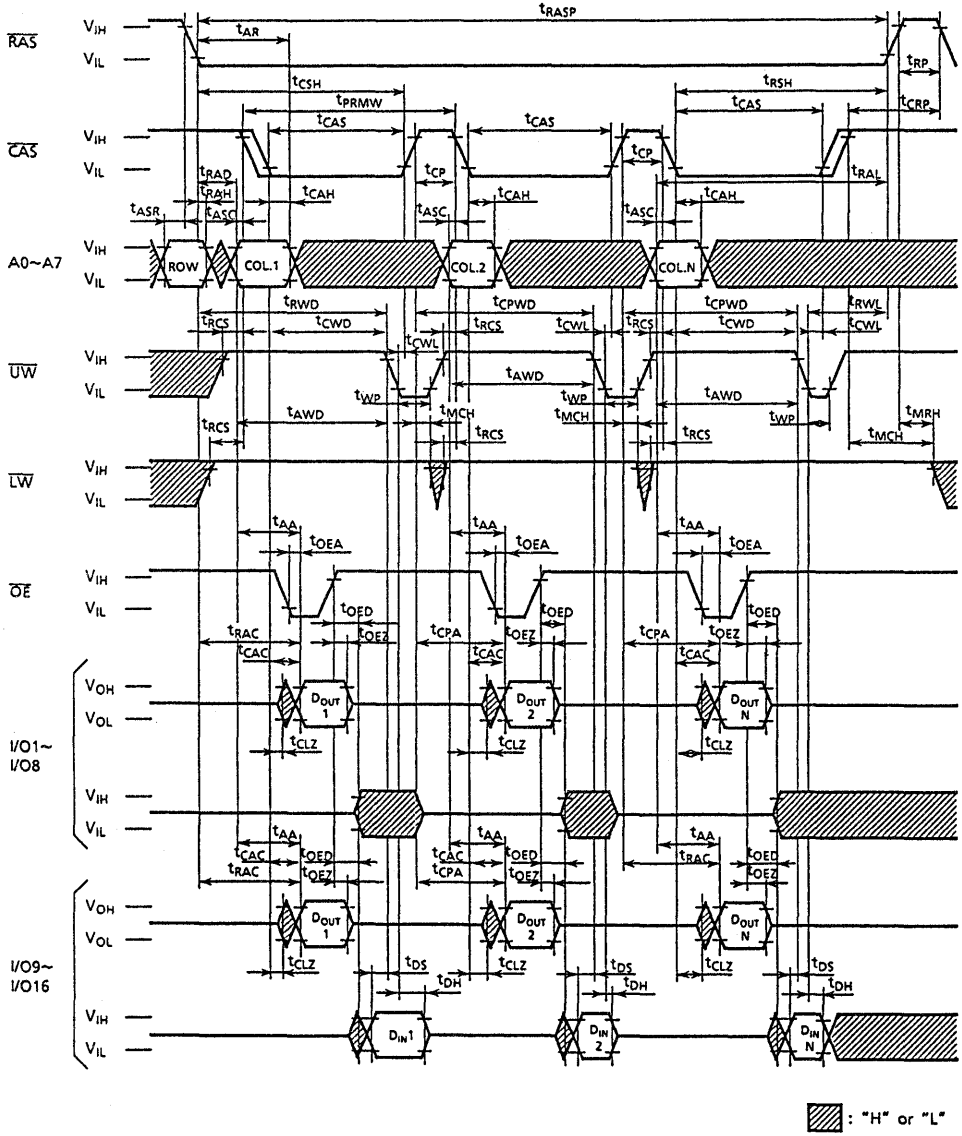
Note: D_{OUT} = OPEN

▨ : "H" or "L"

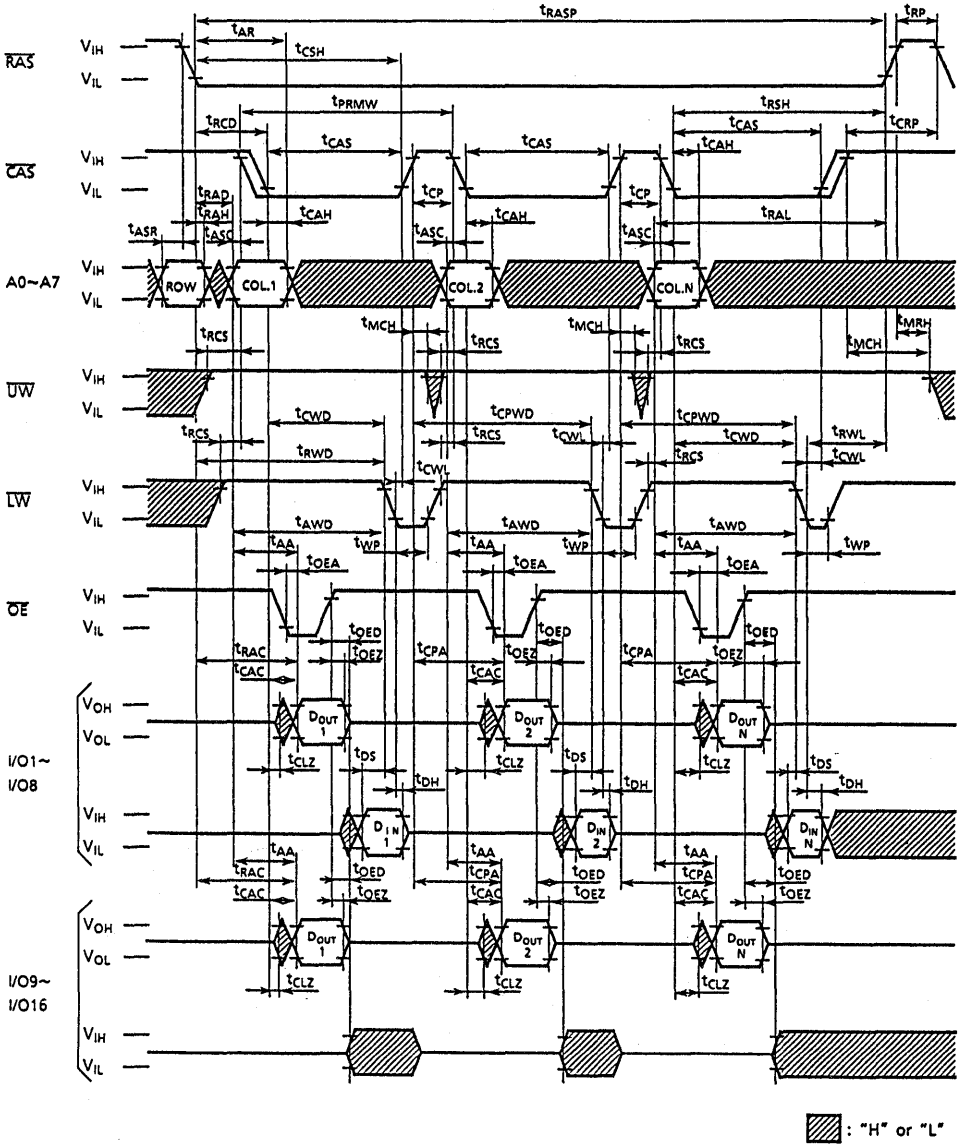
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



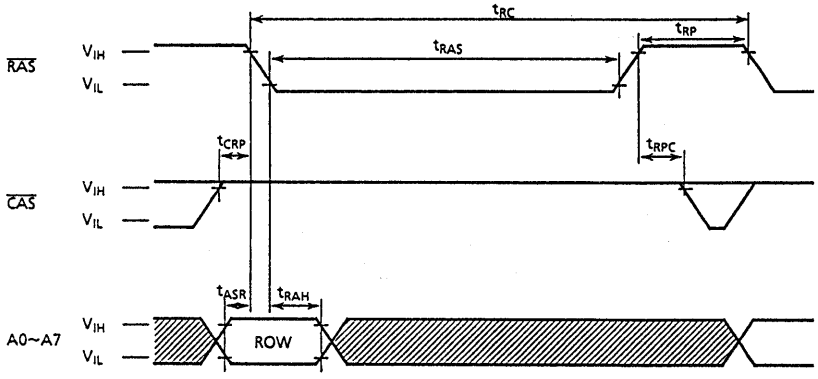
FAST PAGE MODE READ-MODIFY-UPPER-BYTE-WRITE CYCLE



FAST PAGE MODE READ-MODIFY-LOWER-BYTE-WRITE CYCLE



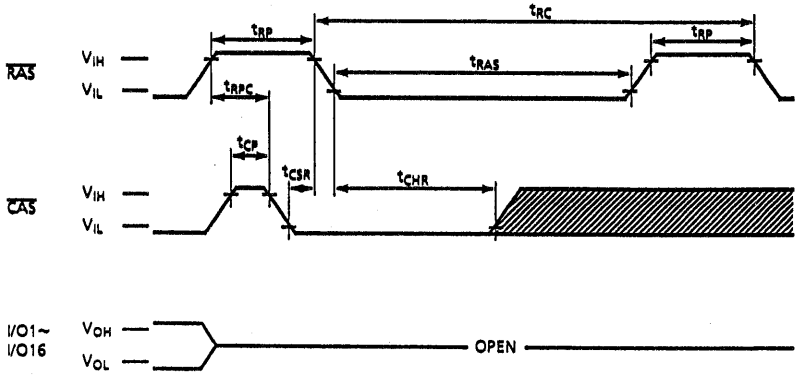
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

▨: "H" or "L"

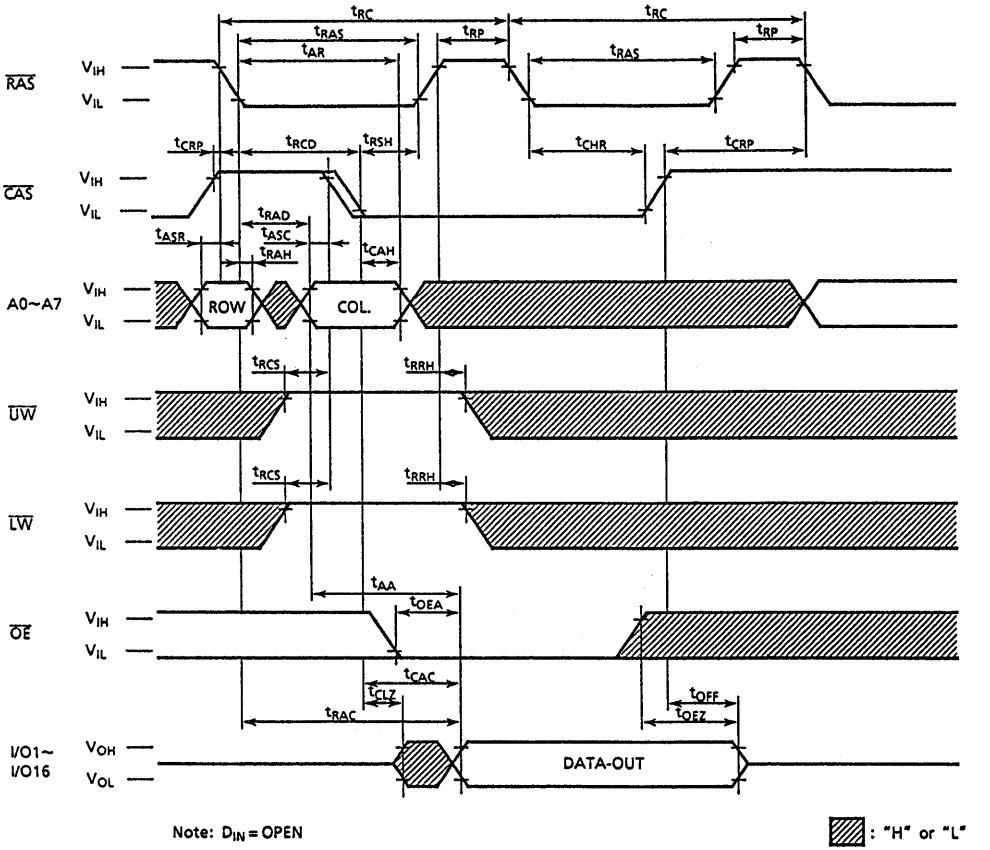
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



Note: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0~A7 = "H" or "L"

▨: "H" or "L"

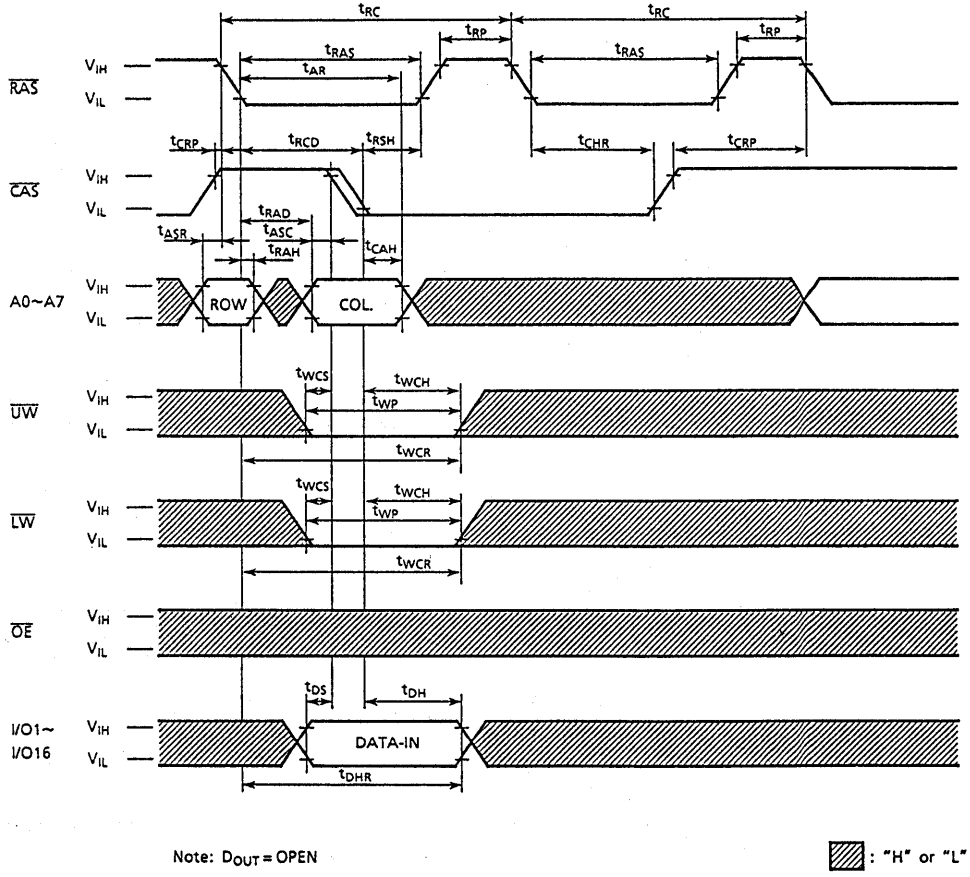
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

▨ : "H" or "L"

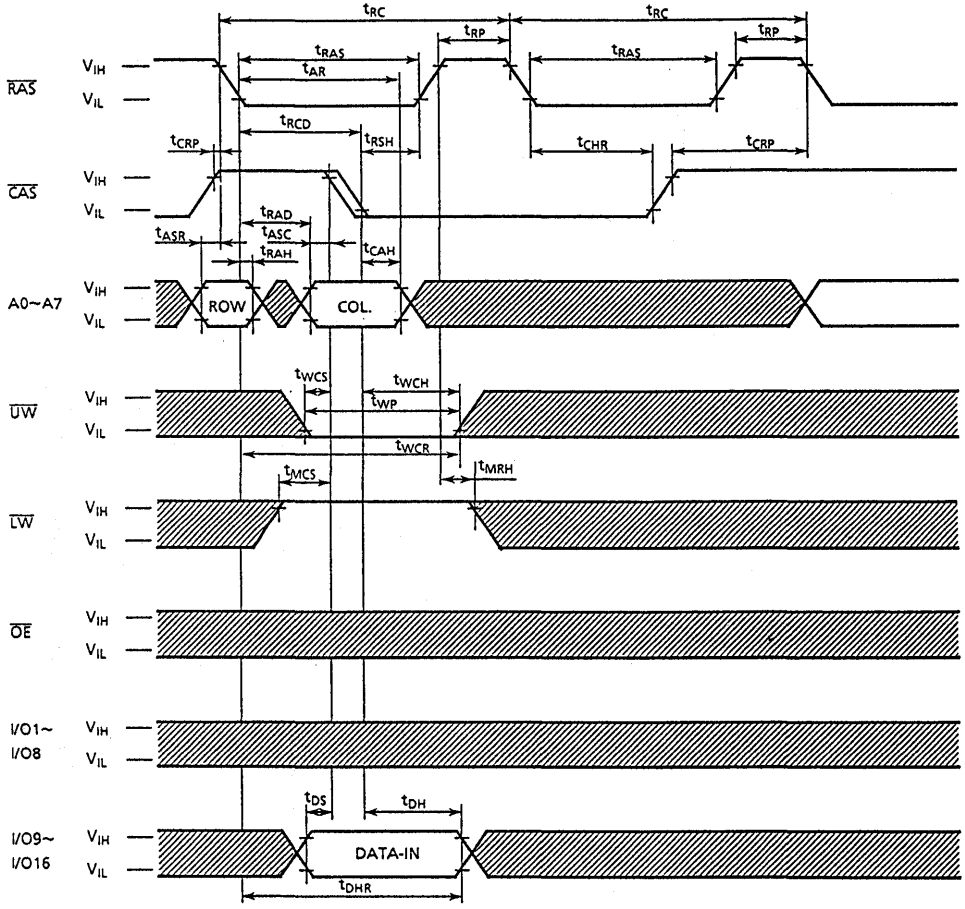
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

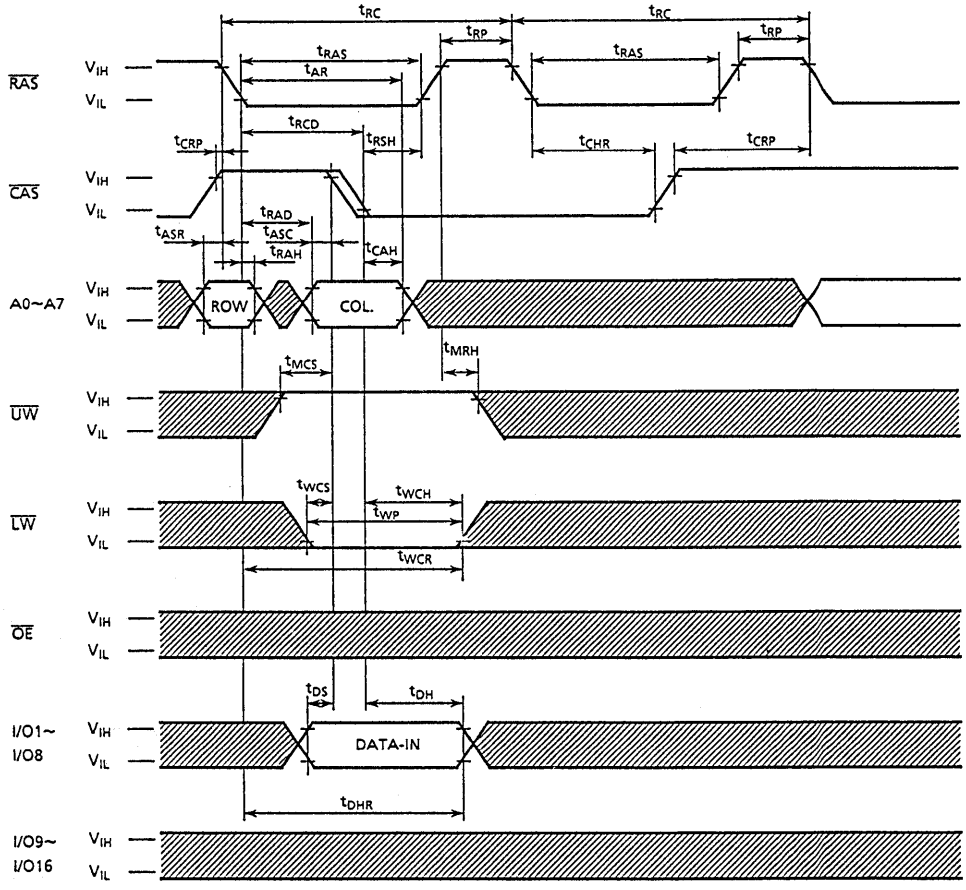
HIDDEN REFRESH CYCLE (UPPER BYTE WRITE)



Note: D_{OUT} = OPEN

▨ : "H" or "L"

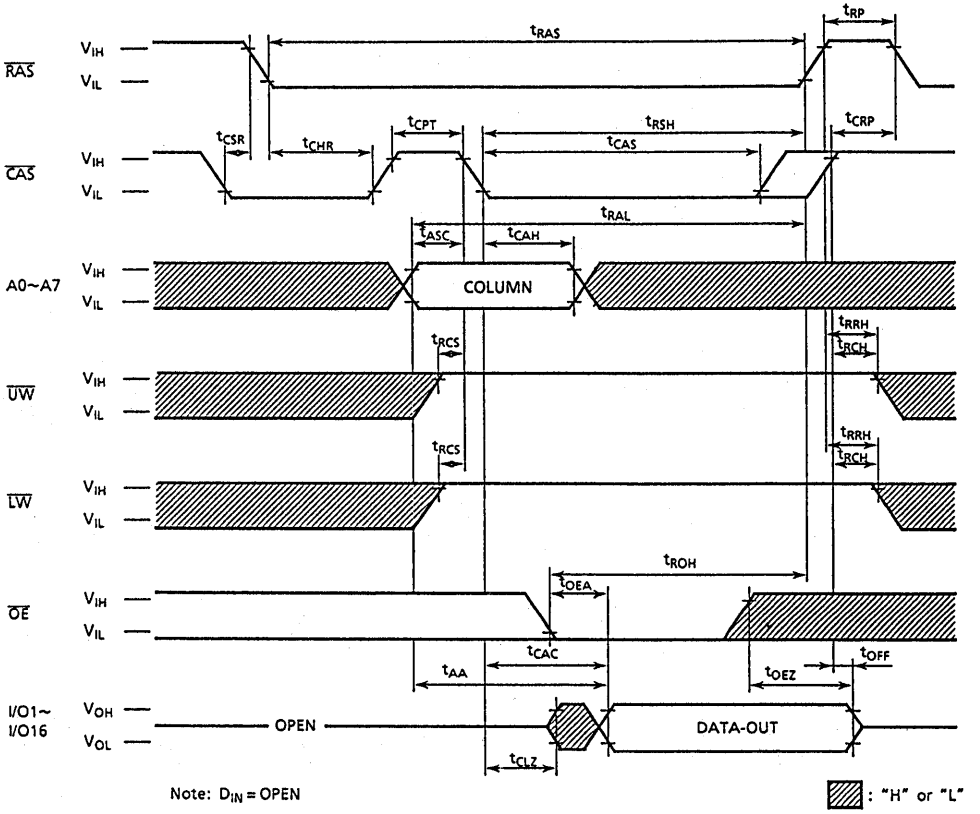
HIDDEN REFRESH CYCLE (LOWER BYTE WRITE)



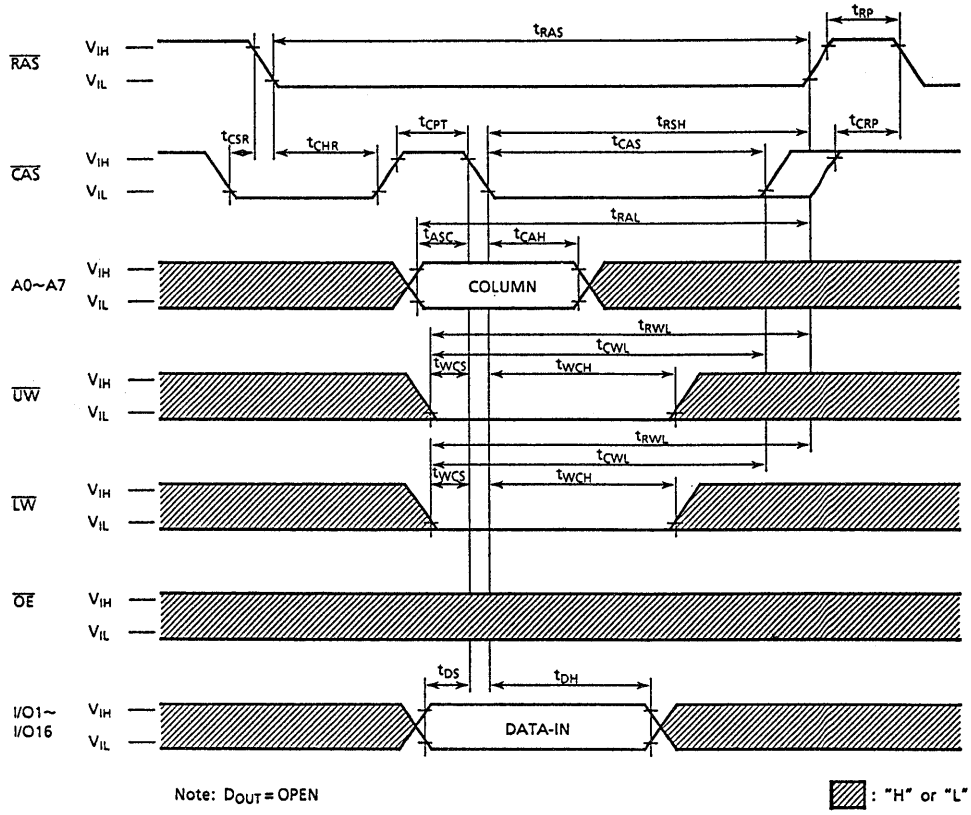
Note: D_{OUT} = OPEN

▨: "H" or "L"

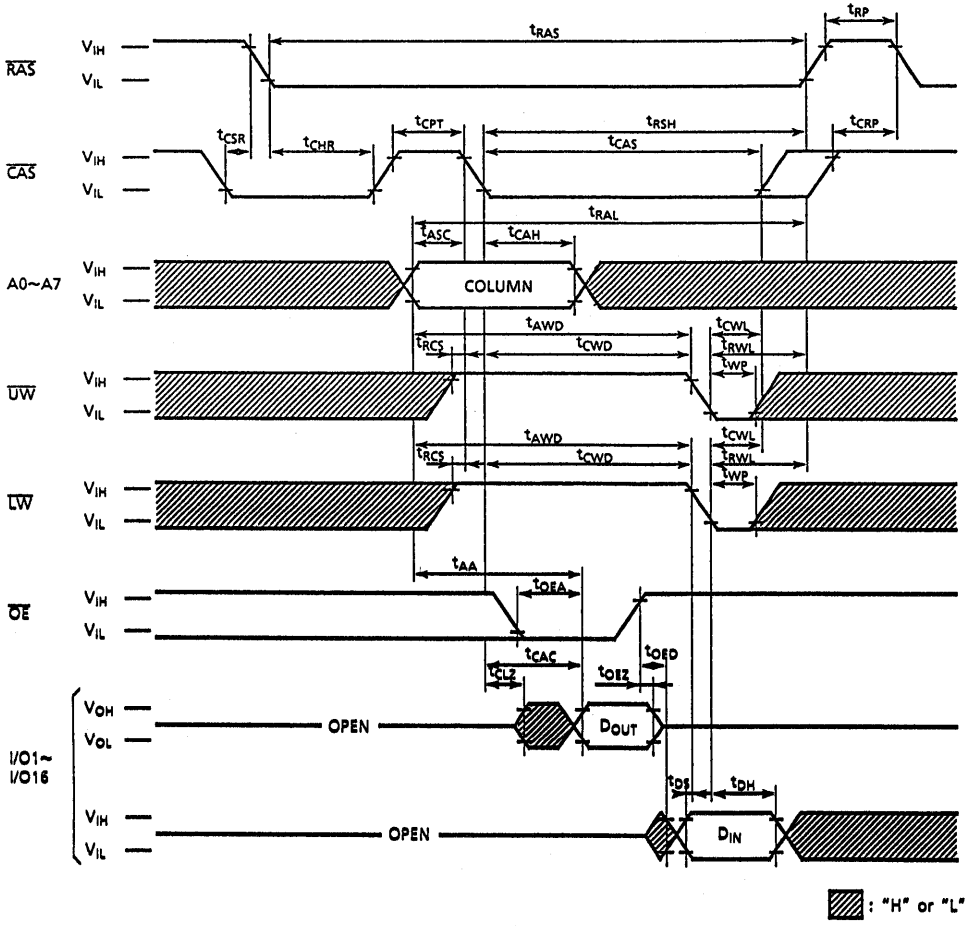
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST READ-MODIFY-WRITE CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511664BJL/BZL are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing $\overline{UW}$ and $\overline{LW}$ low during the $\overline{RAS}/\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or $\overline{LW}$ strobes data on I/O1~I/O8 into the on-chip data latch. And the falling edge of $\overline{CAS}$ or $\overline{UW}$ strobes data on I/O9~I/O16 into the on-chip data latch. In an early write cycle, $\overline{LW}$ and $\overline{UW}$ are brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In derayed write or read modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{LW}$ and $\overline{UW}$ with setup and hold times referenced to these signals.

In derayed or read modify write, $\overline{OE}$ must be high to bring the output buffers to high inpedance prior to impressing data on the I/O lines.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

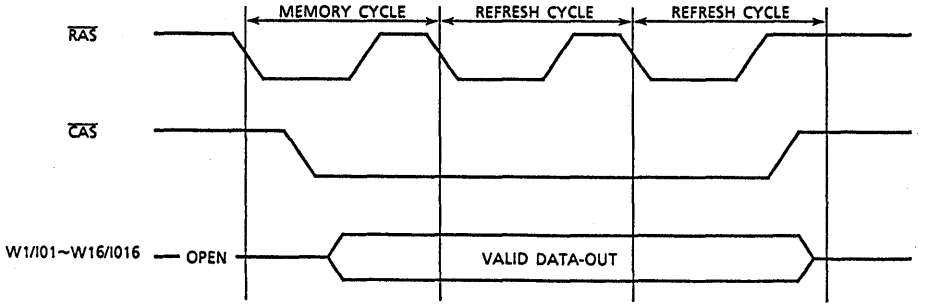
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511664BJL/BZL offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511664BJL/BZL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511664BJL/BZL is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511664BJL/BZL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

TENTATIVE DATA
65,536 WORD × 16 BIT DYNAMIC RAM

DESCRIPTION

The TC511665BJ/BZ is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511665BJ/BZ utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511665BJ/BZ to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

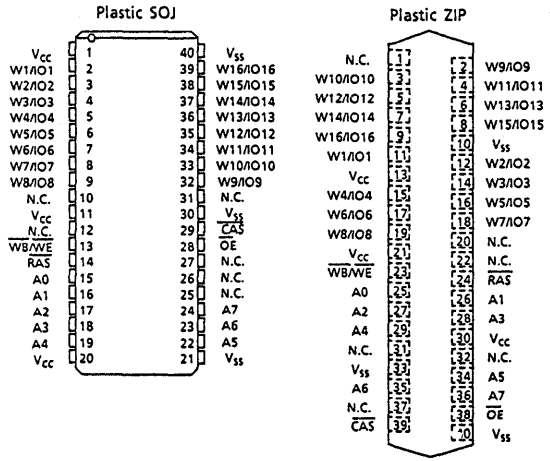
FEATURES

- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511665BJ/BZ-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511665BJ/BZ-80)
  495mW MAX. Operating (TC511665BJ/BZ-10)
  5.5mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/4ms
- Package TC511665BJ:SOJ40-P-400
  TC511665BZ:ZIP40-P-475

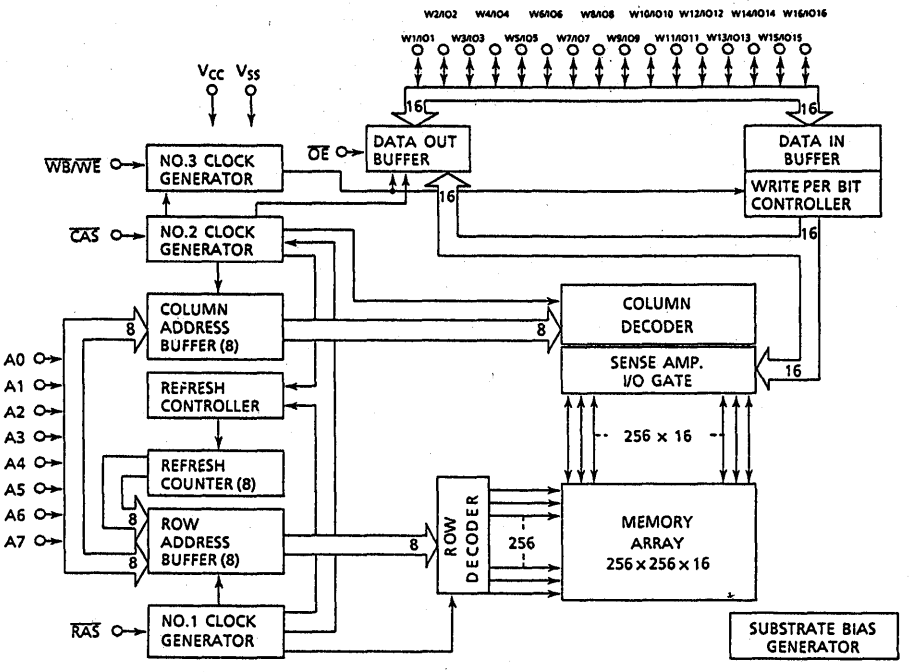
PIN CONNECTION (TOP VIEW)



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/ Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~ W16/IO16	Write Selection/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (W1/IO1~W16/IO16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≦ 20ns

*2 -2.0V at pulse width ≦ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511665BJ/BZ-80	−	*115	mA	3, 4, 5
		TC511665BJ/BZ-10	−	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		−	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511665BJ/BZ-80	−	115	mA	3, 5
		TC511665BJ/BZ-10	−	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511665BJ/BZ-80	−	70	mA	3, 4, 5
		TC511665BJ/BZ-10	−	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		−	1	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511665BJ/BZ-80	−	115	mA	3
		TC511665BJ/BZ-10	−	90		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		−10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −2.5mA)		2.4	−	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		−	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 6, 7, 8)

SYMBOL	PARAMETER	TC511665BJ/BZ-80		TC511665BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	35	ns	9,14
t_{AA}	Access Time from Column Address	–	45	–	55	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	65	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	ns	12

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511665BJ/BZ-80		TC511665BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	4	–	4	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	65	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	ns	9
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	10	0	20	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	ns	

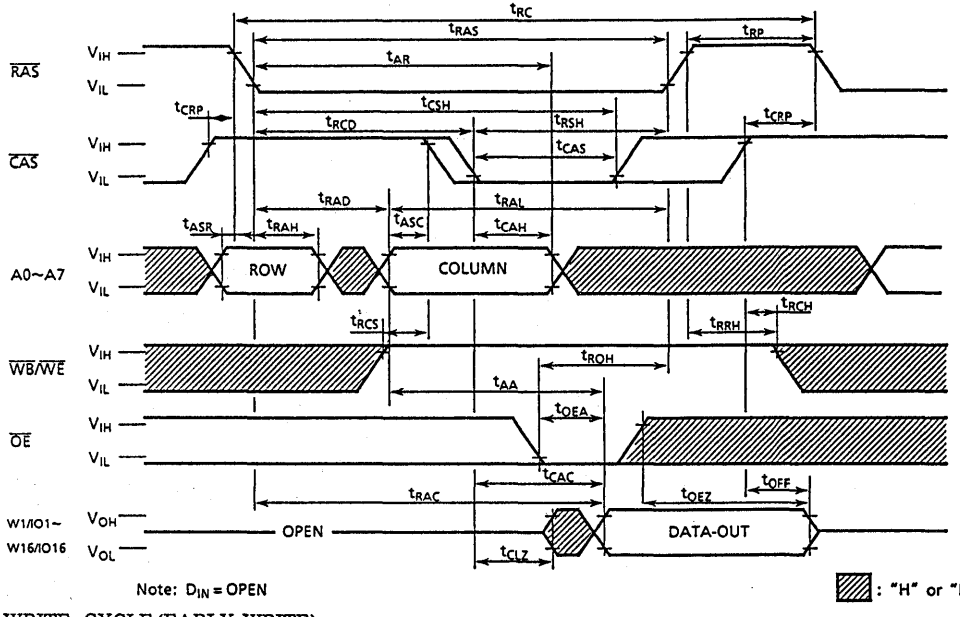
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/IO1~W16/IO16)	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 1 TTL load and 50pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{WB}$/) $\overline{WE}$ leading edge in read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

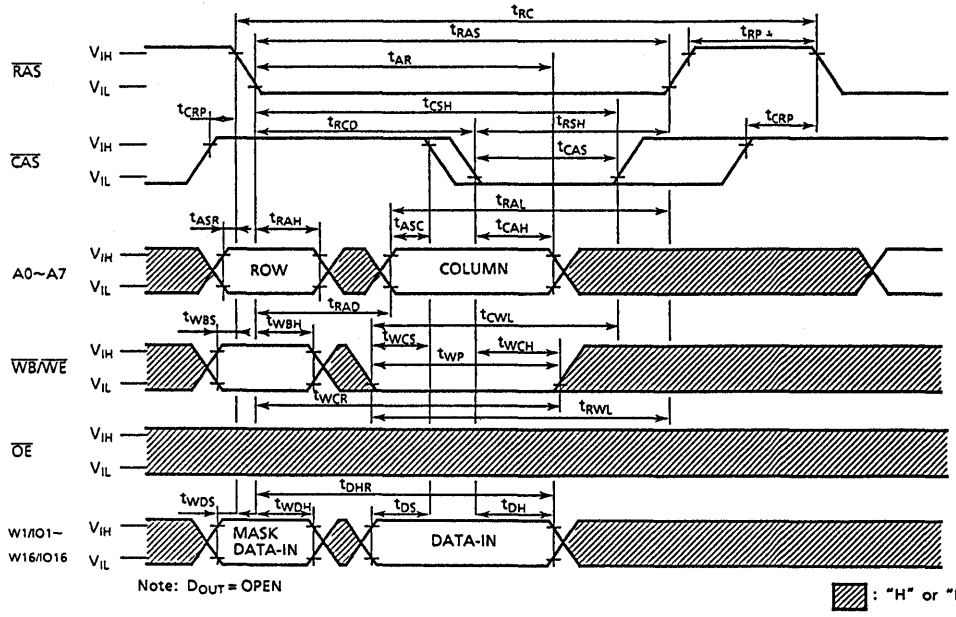
READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

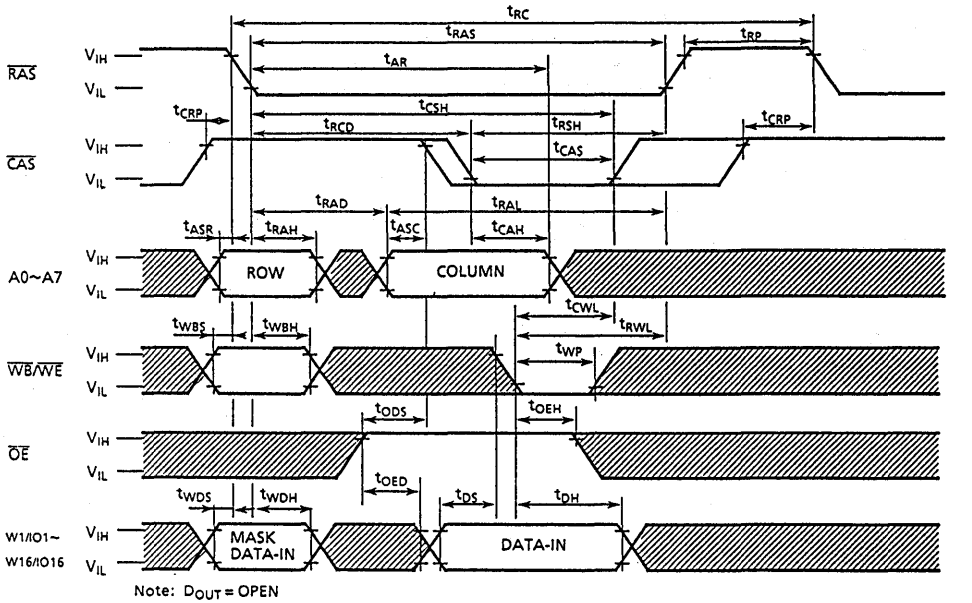
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = OPEN

▨: "H" or "L"

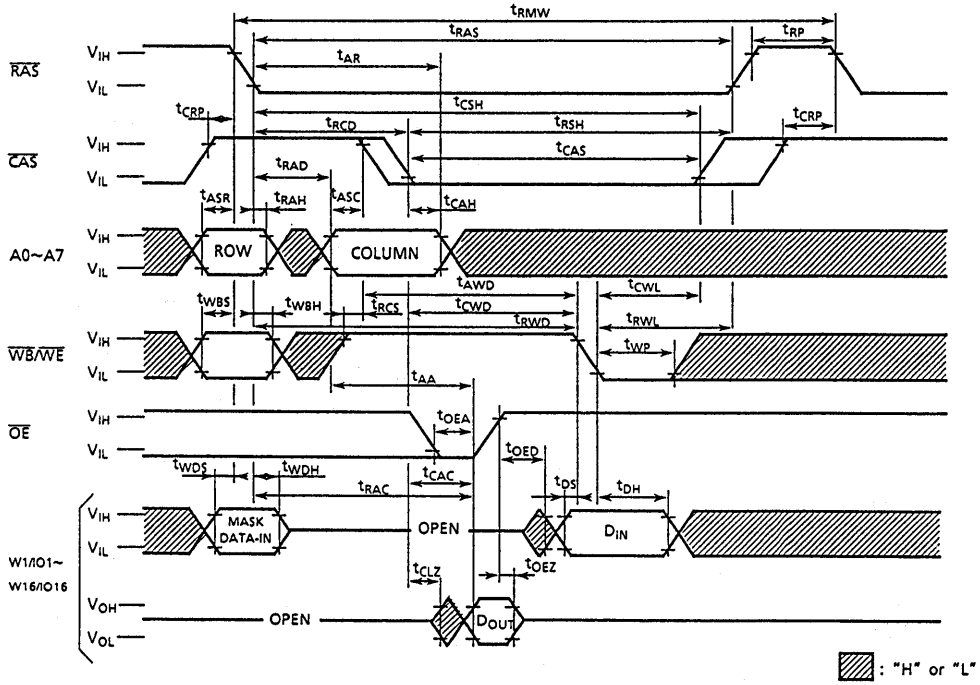
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



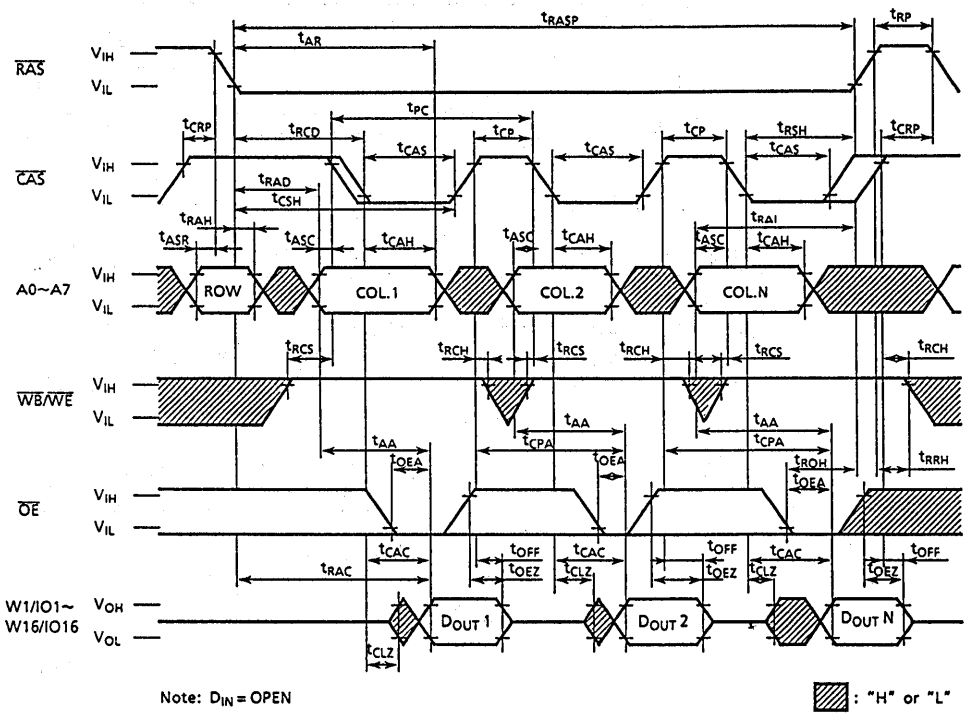
Note: D_{OUT} = OPEN

▨: "H" or "L"

READ-MODIFY-WRITE CYCLE



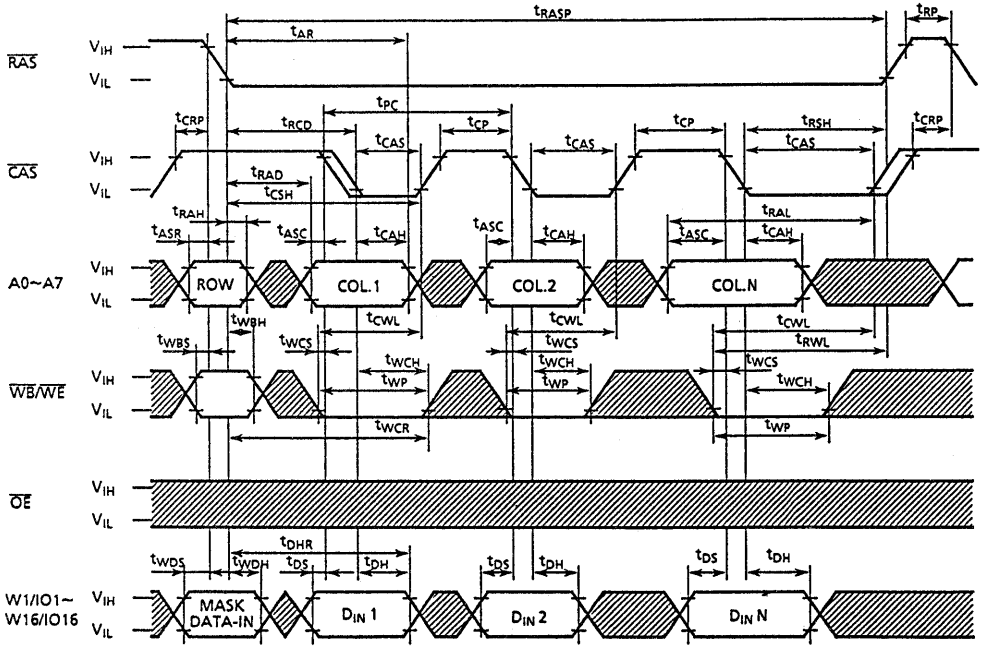
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

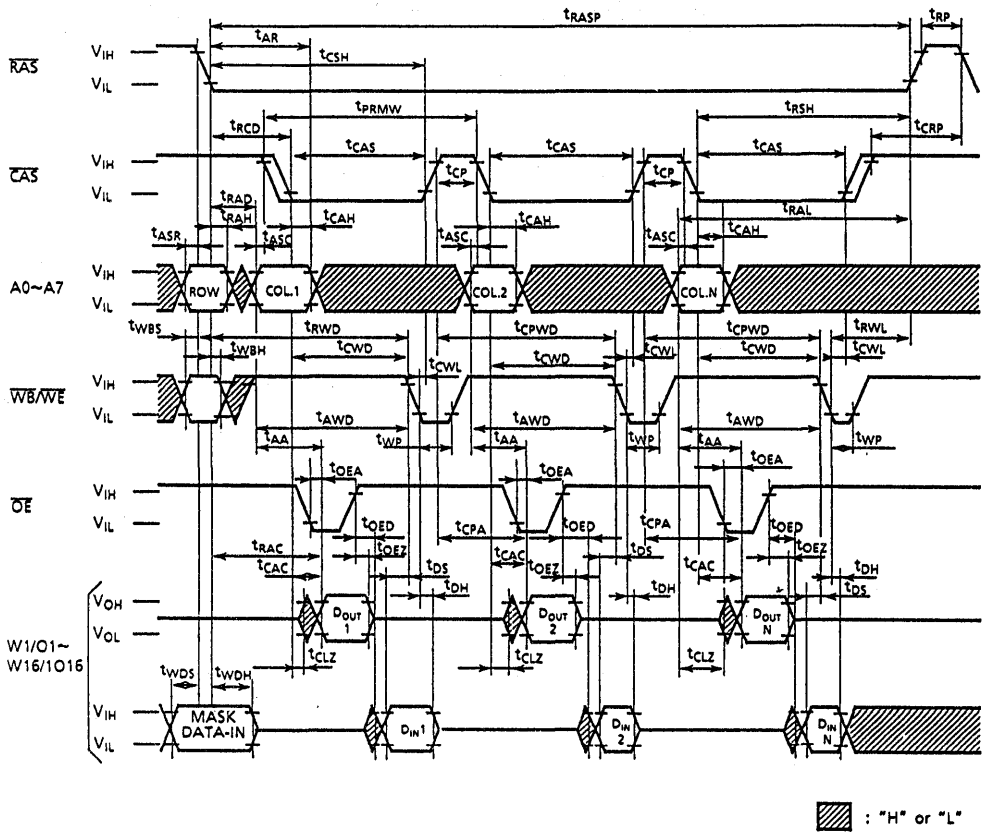
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



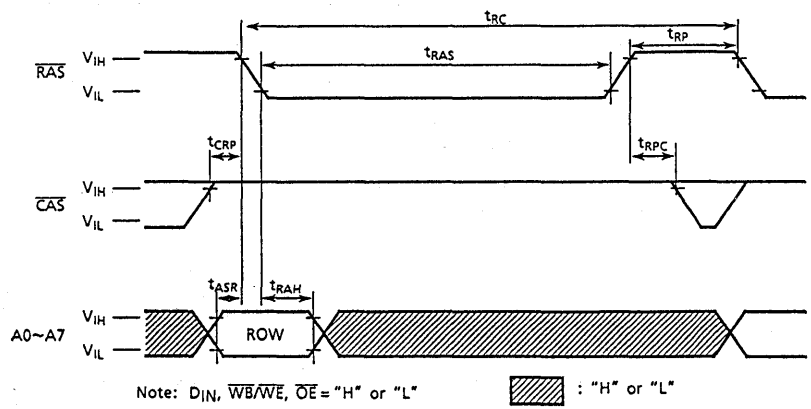
Note: D_{OUT} = OPEN

▨ : "H" or "L"

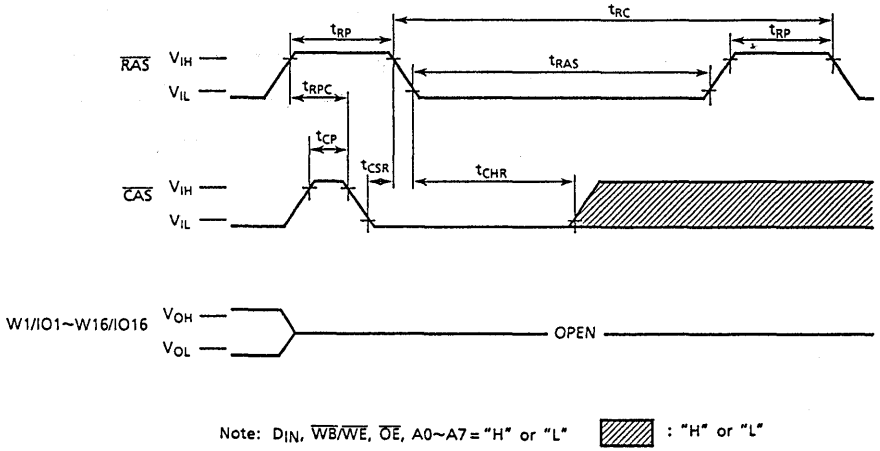
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



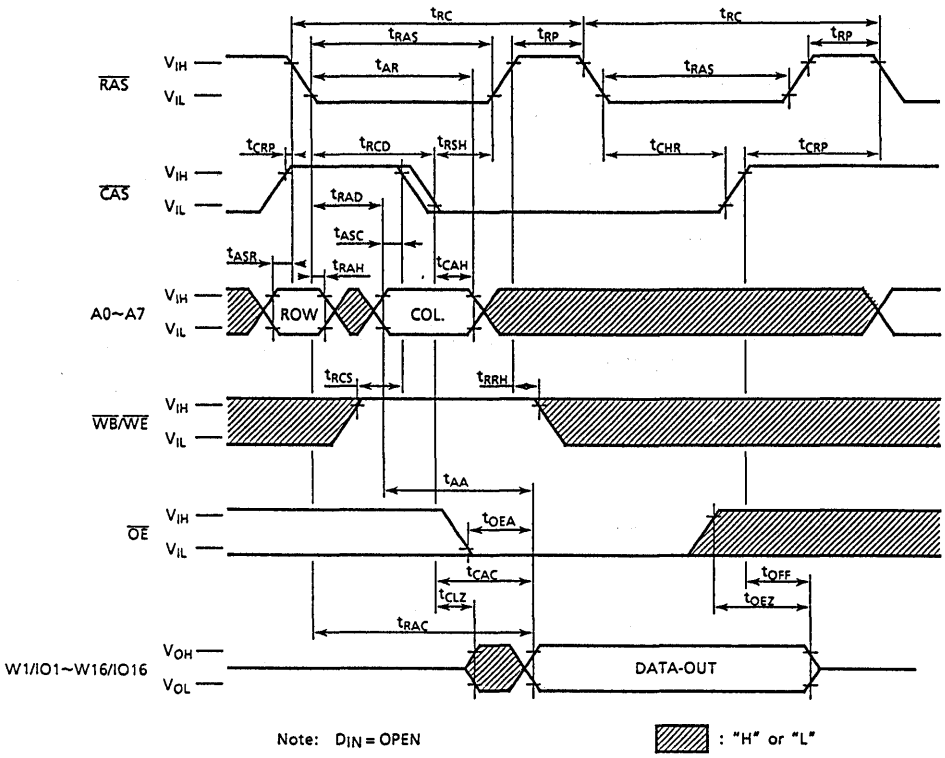
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



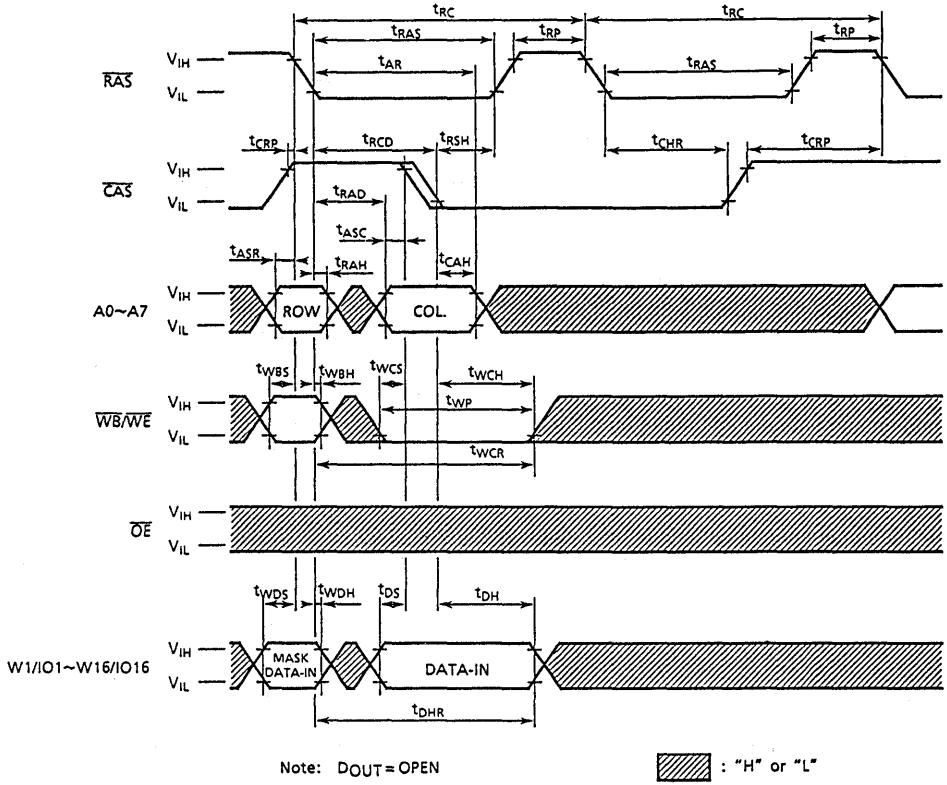
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

: "H" or "L"

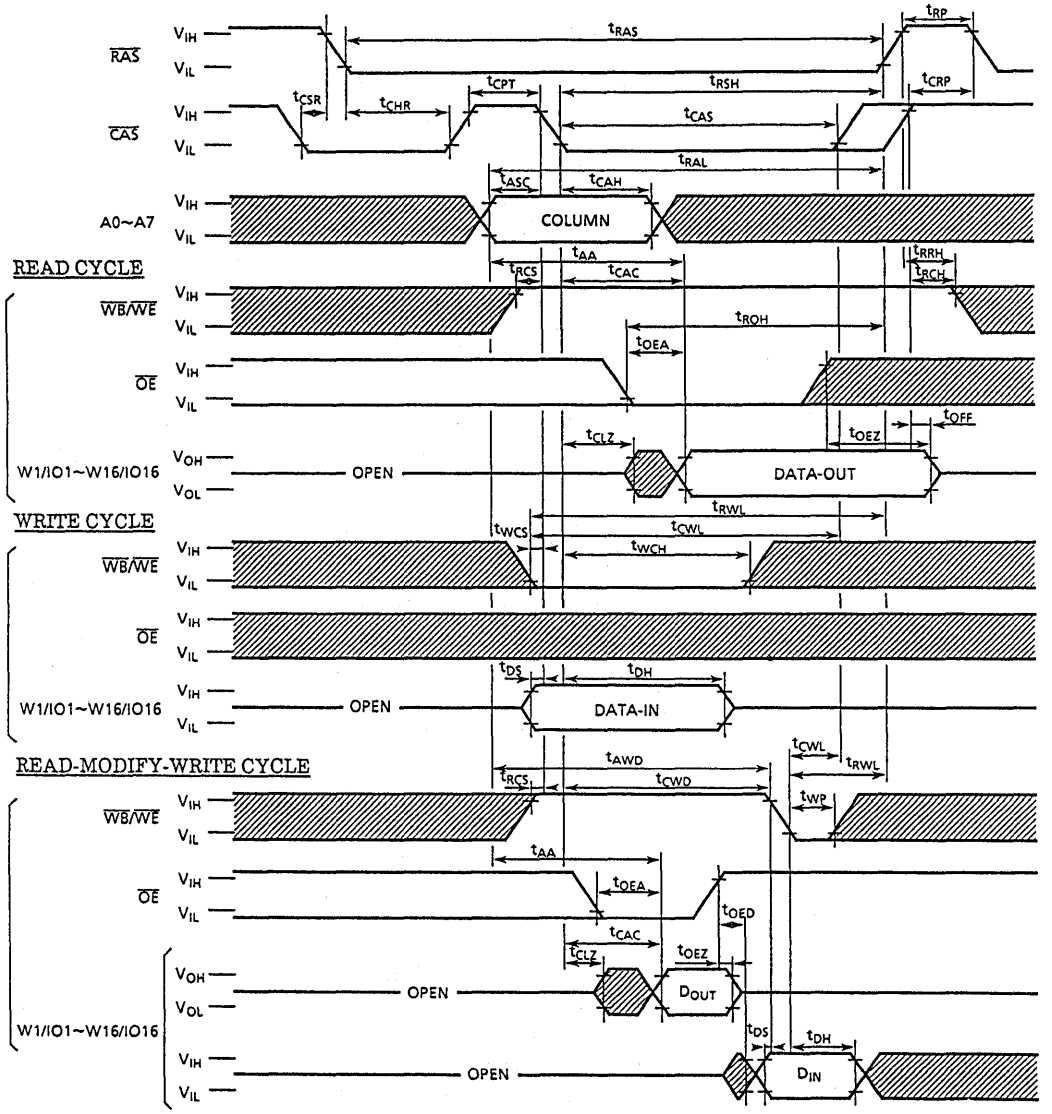
HIDDEN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

: "H" or "L"

CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511665BJ/BZ are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi/) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$ (/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{\text{RAS}}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{\text{RAS}}$-only" cycles, $\overline{\text{RAS}}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH

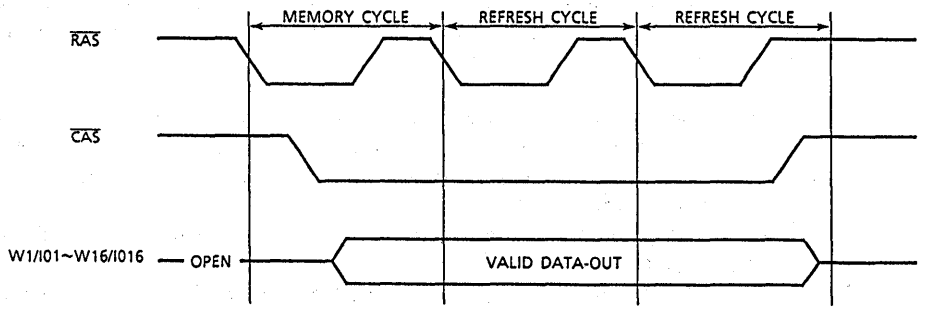
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refreshing available on the TC511665BJ/BZ offers an alternate refresh method. If $\overline{\text{CAS}}$ is held on low for the specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511665BJ/BZ allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{\text{RAS}}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{\text{RAS}}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511665BJ/BZ is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{\text{CAS}}$ at V_{IL} and taking $\overline{\text{RAS}}$ high and after a specified precharge period (t_{RP}), executing a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511665BJ/BZ can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

NOTES

TENTATIVE DATA
65,536 WORD × 16 BIT DYNAMIC RAM

DESCRIPTION

The TC511665BJL/BZL is the new generation dynamic RAM organized 65,536 words by 16 bits. The TC511665BJL/BZL utilizes TOSHIBA's CMOS Silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC511665BJL/BZL to be packaged in a standard 40 pin plastic SOJ and 40 pin plastic ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

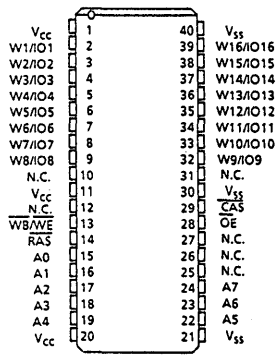
- 65,536 word by 16 bit organization
- Fast access time and cycle time

		TC511665BJL/BZL-80/-10	
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	45ns	55ns
t_{CAC}	$\overline{CAS}$ Access Time	30ns	35ns
t_{RC}	Cycle Time	135ns	170ns
t_{PC}	Fast Page Mode Cycle Time	55ns	65ns

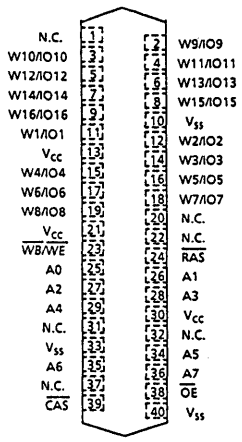
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Low Power
  633mW MAX. Operating (TC511665BJL/BZL-80)
  495mW MAX. Operating (TC511665BJL/BZL-10)
  1.7mW MAX. Standby
- Outputs unlatched at cycle end allows two-dimensional chip seleciton
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, Hidden refresh, Write-Per-Bit and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 256 refresh cycles/32ms
- Package TC511665BJL:SOJ40-P-400
  TC511665BZL:ZIP40-P-475

PIN CONNECTION (TOP VIEW)

Plastic SOJ



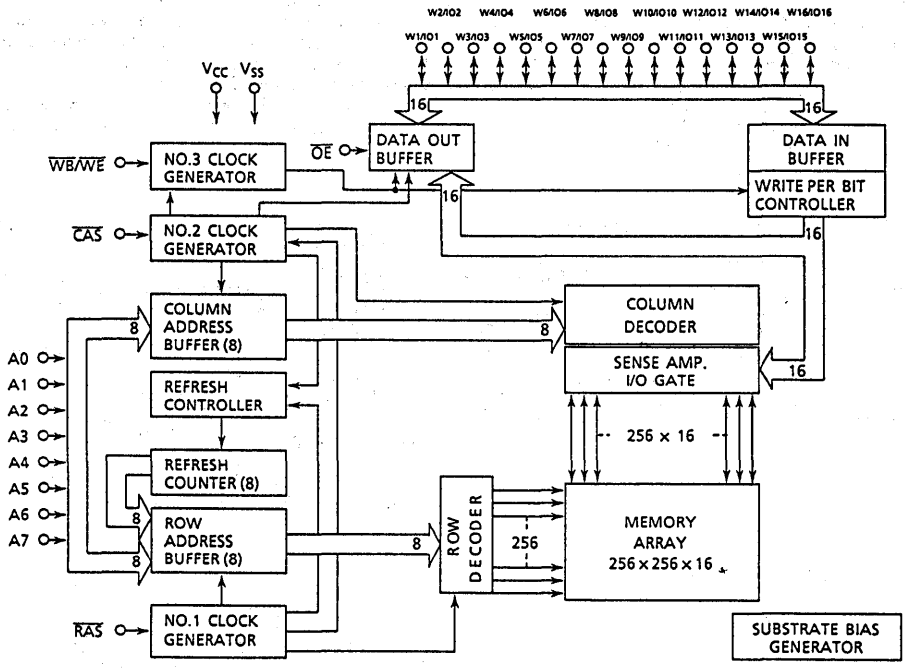
Plastic ZIP



PIN NAMES

SYMBOL	NAME
A0~A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WB/WE}$	Write Per Bit/ Read/Write Input
$\overline{OE}$	Output Enable
W1/IO1~ W16/IO16	Write Selection/ Data Input/Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1~7	V	1
Output Voltage	V_{OUT}	−1~7	V	1
Power Supply Voltage	V_{CC}	−1~7	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~150	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	700	mW	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°c)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	−1.0 *1	−	0.8	V	2
V_{IL}	Input Low Voltage (W1/IO1~W16/IO16)	−0.5 *2	−	0.8	V	2

*1 -2.5V at pulse width ≤ 20ns

*2 -2.0V at pulse width ≤ 20ns

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°c)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	TC511665BJL/BZL-80	–	115	mA	3, 4, 5
		TC511665BJL/BZL-10	–	90		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	TC511665BJL/BZL-80	–	115	mA	3, 5
		TC511665BJL/BZL-10	–	90		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	TC511665BJL/BZL-80	–	70	mA	3, 4, 5
		TC511665BJL/BZL-10	–	60		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	300	µA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	TC511665BJL/BZL-80	–	115	mA	3
		TC511665BJL/BZL-10	–	90		
I_{CC7}	BATTERY BACK UP CURRENT Average Power Supply Current, Battery back up Mode ($\overline{CAS}$ = $\overline{CAS}$ Before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} – 0.2V, $\overline{WB/WE}$ = V_{CC} – 0.2V or 0.2V, A0~A7 = V_{CC} – 0.2V or 0.2V, W1/IO1~W16/IO16 = V_{CC} – 0.2V, 0.2V or OPEN: t_{RC} = 125µs, t_{RAS} = t_{RAS} MIN.~1µs)		–	400	µA	3, 6
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 2.5mA)		2.4	+–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 2.1mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°c)(Notes 7, 8, 9)

SYMBOL	PARAMETER	TC511665BJL/BZL-80		TC511665BJL/BZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	–	170	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	180	–	225	–	ns	
t_{PC}	Fast Page Mode Cycle Time	55	–	65	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	10,15, 16
t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	35	ns	10,15
t_{AA}	Access Time from Column Address	–	45	–	55	ns	10,16
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	60	ns	10
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	10
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	11
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	9
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	30	10,000	35	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	* 65	ns	15
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	16
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45	–	55	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	12
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	12
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	13
t_{DH}	Data Hold Time	15	–	15	–	ns	13

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Continued)

SYMBOL	PARAMETER	TC511665BJL/BZL-80		TC511665BJL/BZL-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	65	–	ns	
t_{REF}	Refresh Period	–	32	–	32	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	65	–	ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	130	–	ns	14
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time (Fast Page Mode)	70	–	90	–	ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	85	–	ns	14
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	25	–	30	ns	10
t_{OED}	$\overline{OE}$ to Data Delay	10	–	20	–	ns	
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	10	0	20	ns	11
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	20	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	ns	
t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	ns	
t_{WBH}	Write Per Bit Hold Time	10	–	10	–	ns	
t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	ns	
t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	ns	

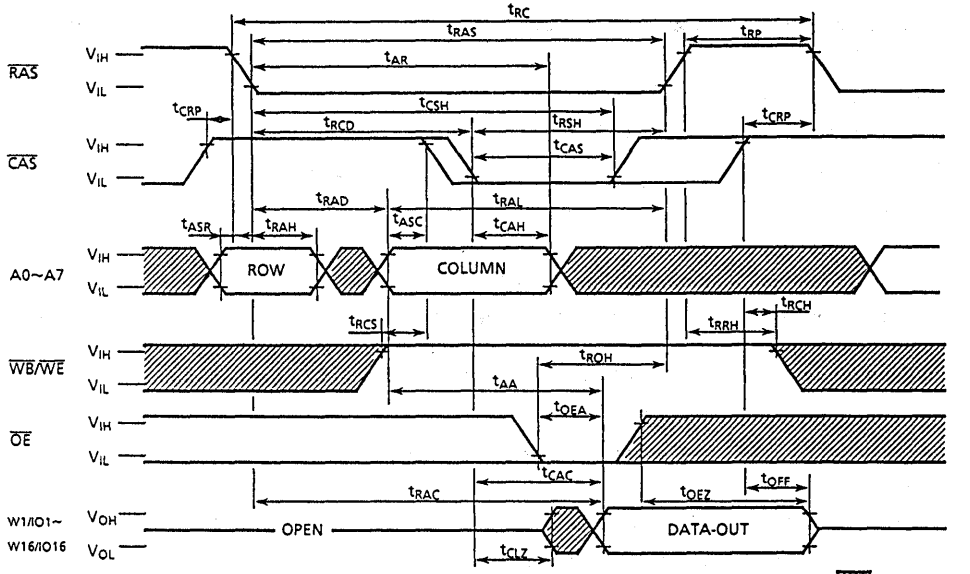
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance (A0~A7, $\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{OE}$)	–	7	pF
C_O	Input/Output Capacitance (W1/IO1~W16/IO16)	–	7	pF

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the outputs open.
5. Column Address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. t_{RAS} (max.) = 1μs is only applied to refresh of battery-back up.
   t_{RAS} (max.) = 10μs is applied to functional operating.
7. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
8. AC measurements assume $t_T=5$ns.
9. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.
   Also, transition times are measured between V_{IH} and V_{IL}.
10. Measured with a load equivalent to 1 TTL load and 50pF.
11. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to ($\overline{WB}$/) $\overline{WE}$ leading edge in read-modify-write cycles.
14. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and data out pins will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
16. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

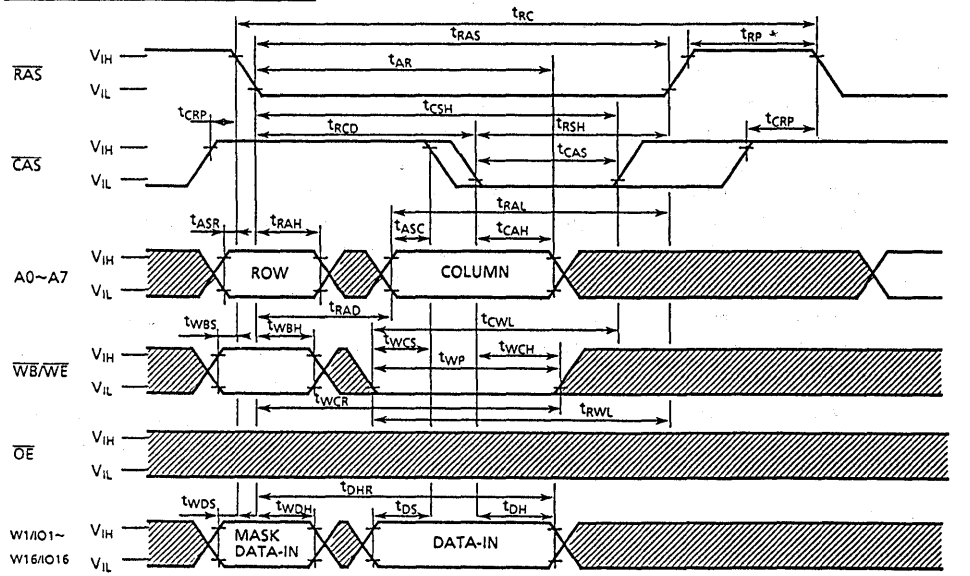
READ CYCLE



Note: D_{IN} = OPEN

▨: "H" or "L"

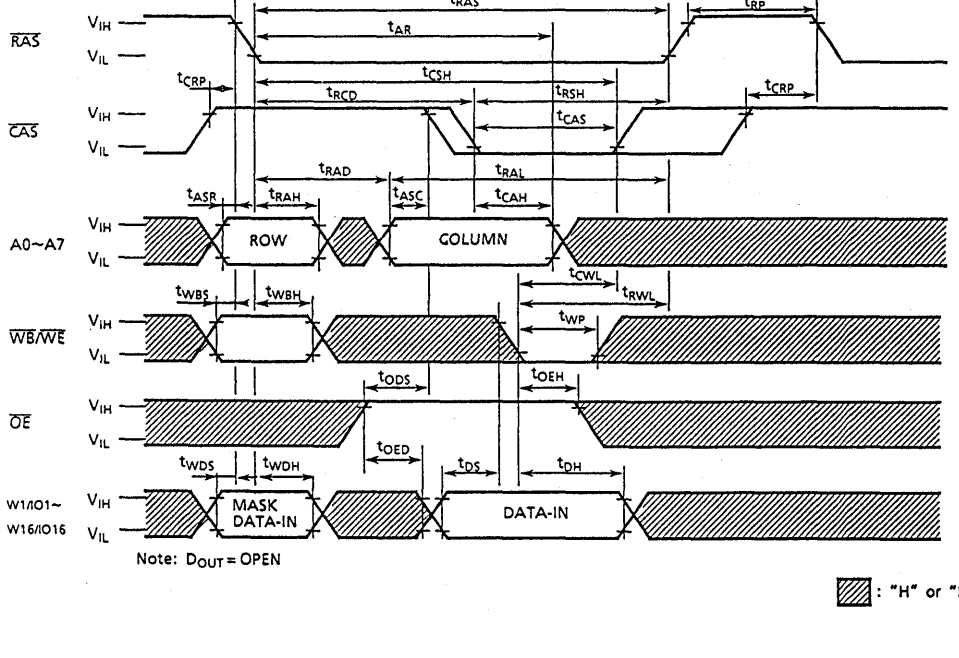
WRITE CYCLE (EARLY WRITE)



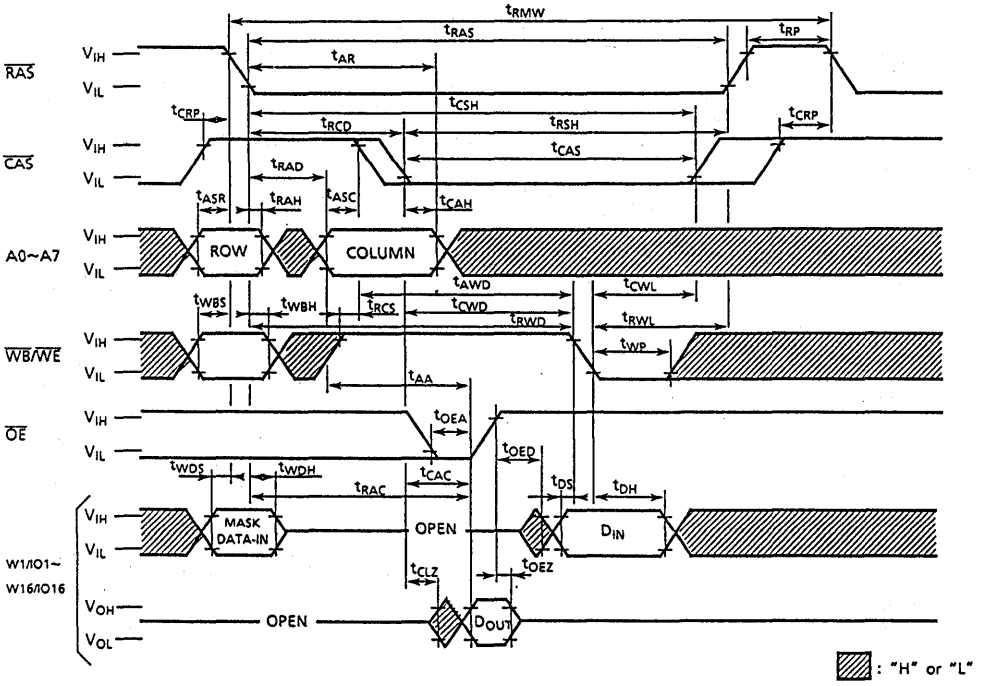
Note: D_{OUT} = OPEN

▨: "H" or "L"

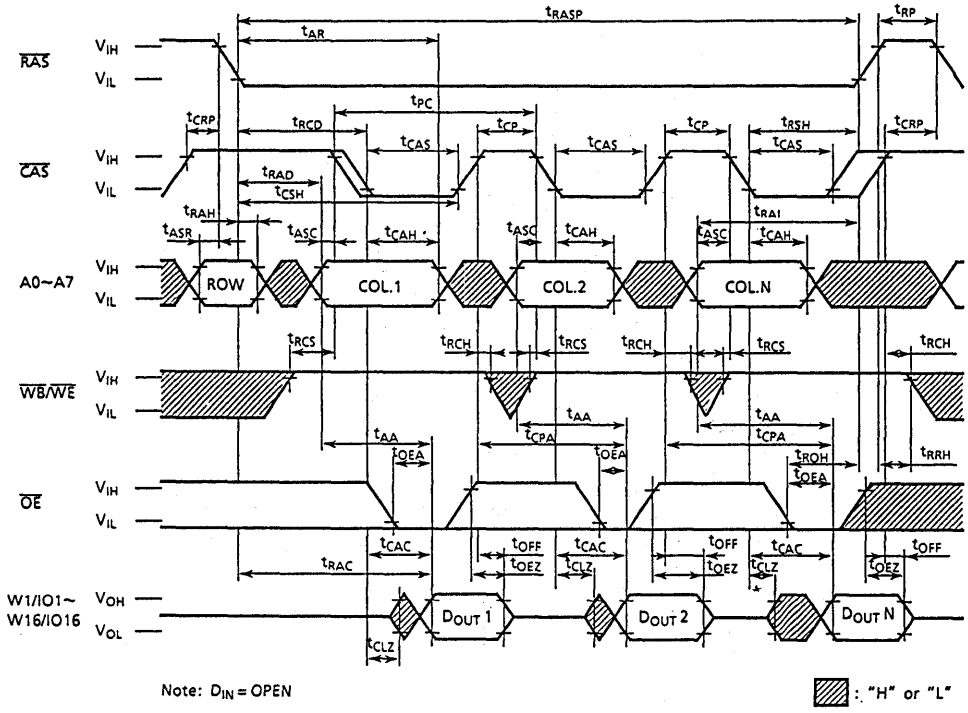
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



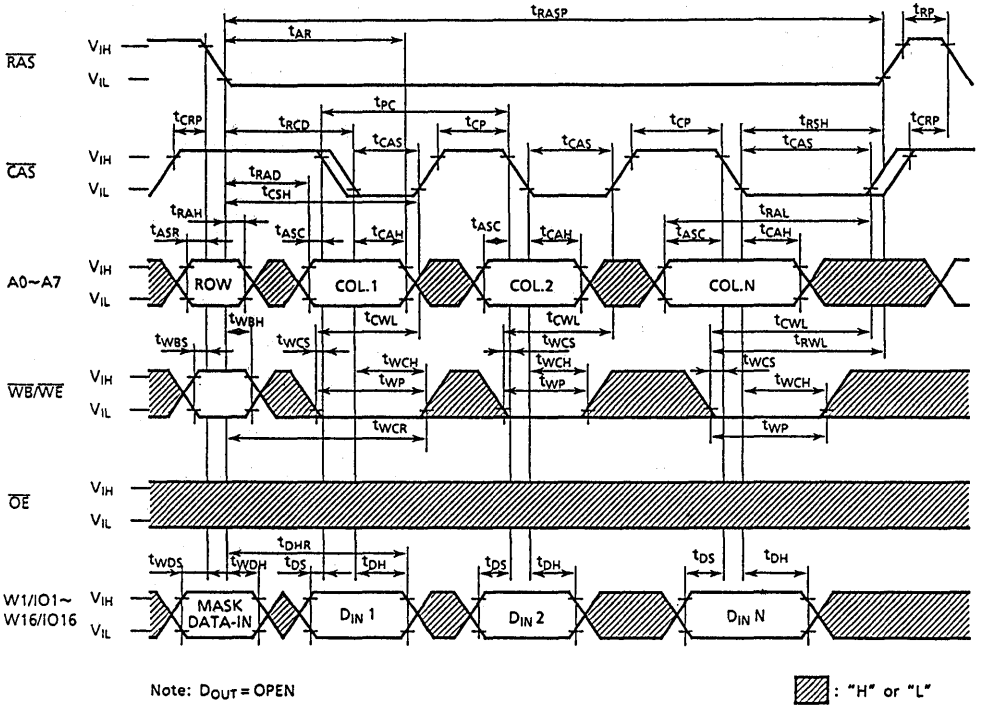
FAST PAGE MODE READ CYCLE



Note: D_{IN} = OPEN

▨ : "H" or "L"

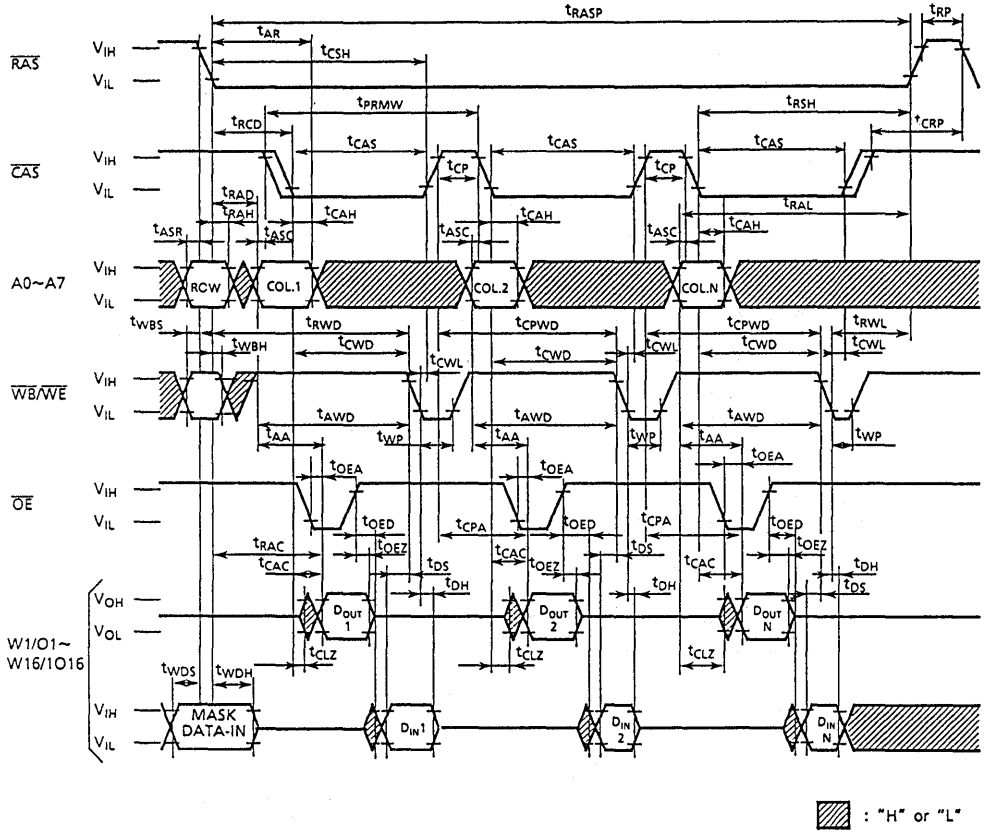
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



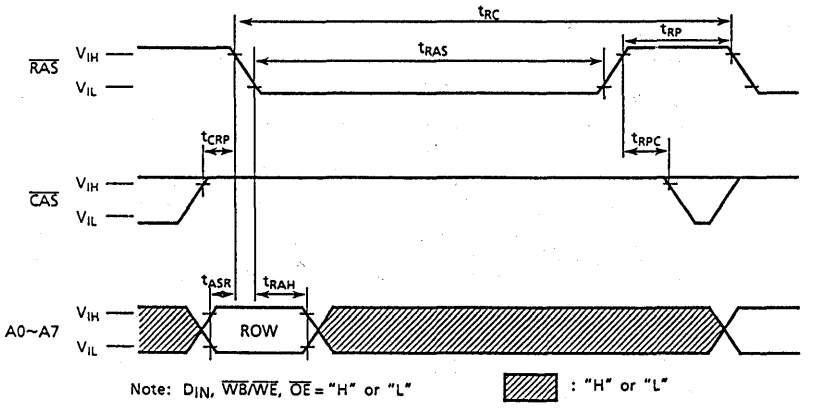
Note: D_{OUT} = OPEN

▨ : "H" or "L"

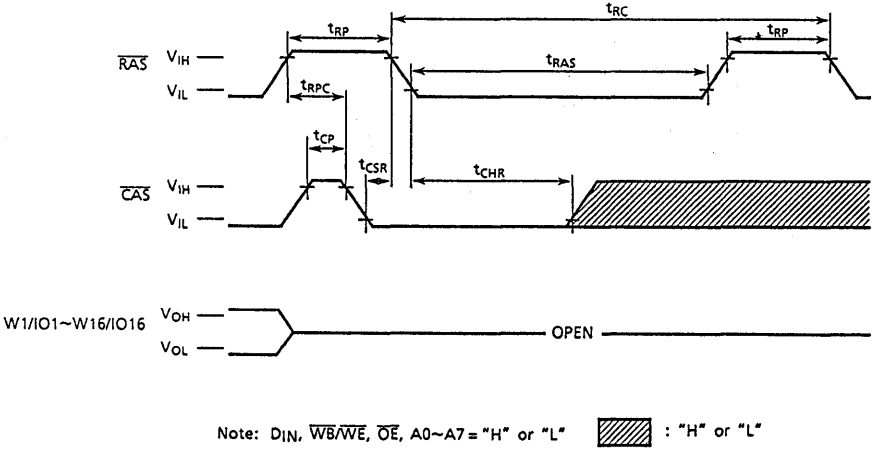
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



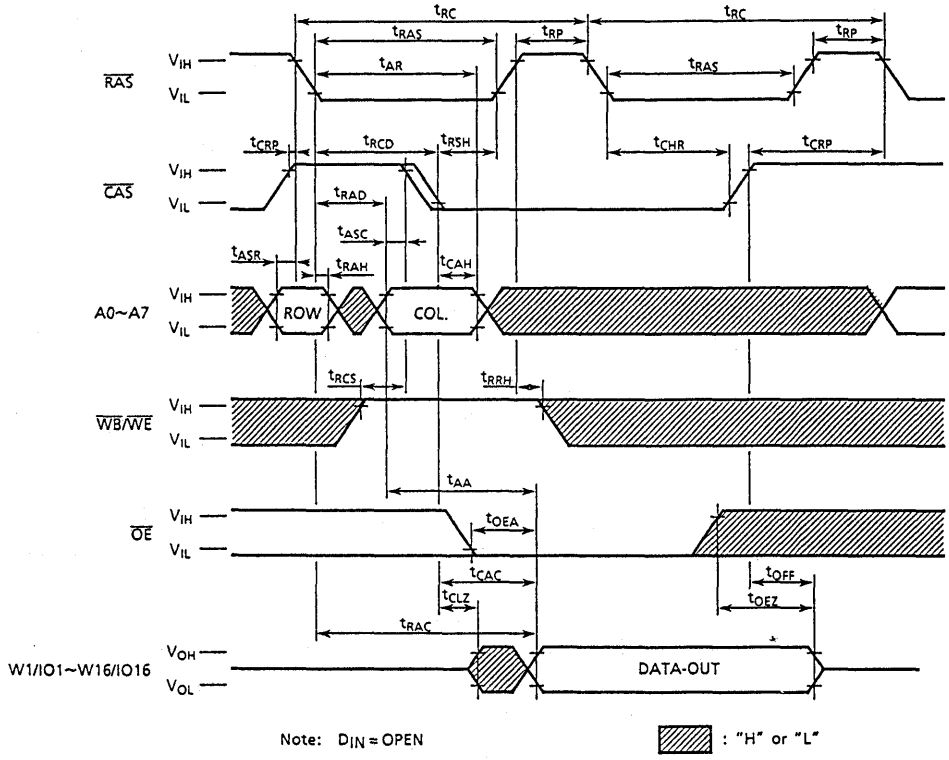
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



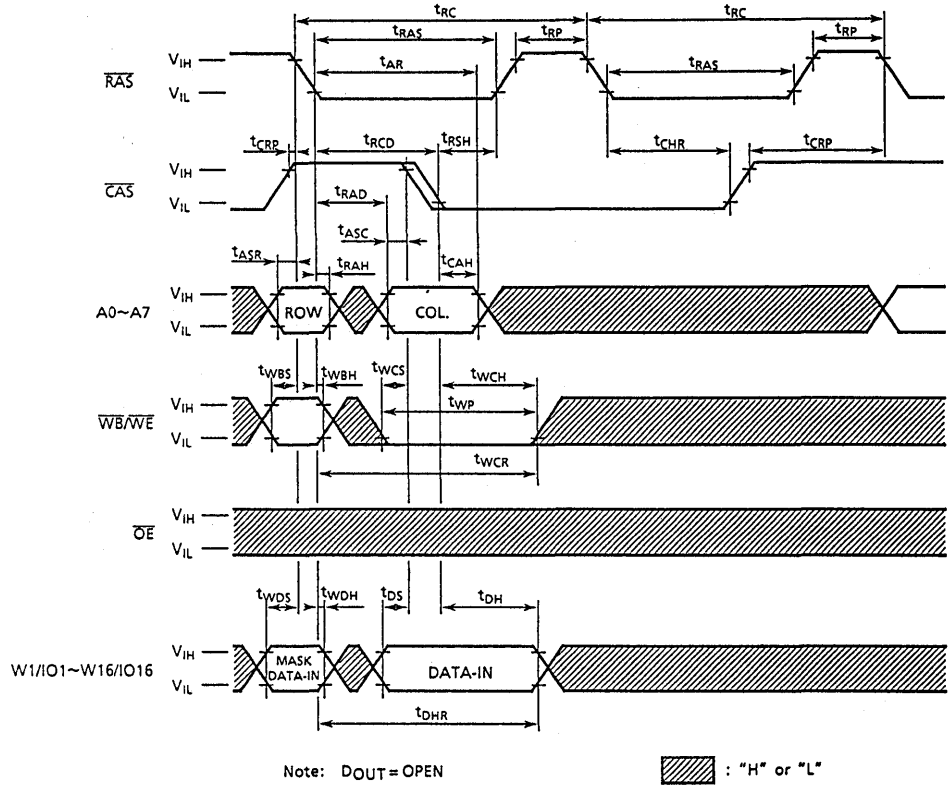
HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = OPEN

: "H" or "L"

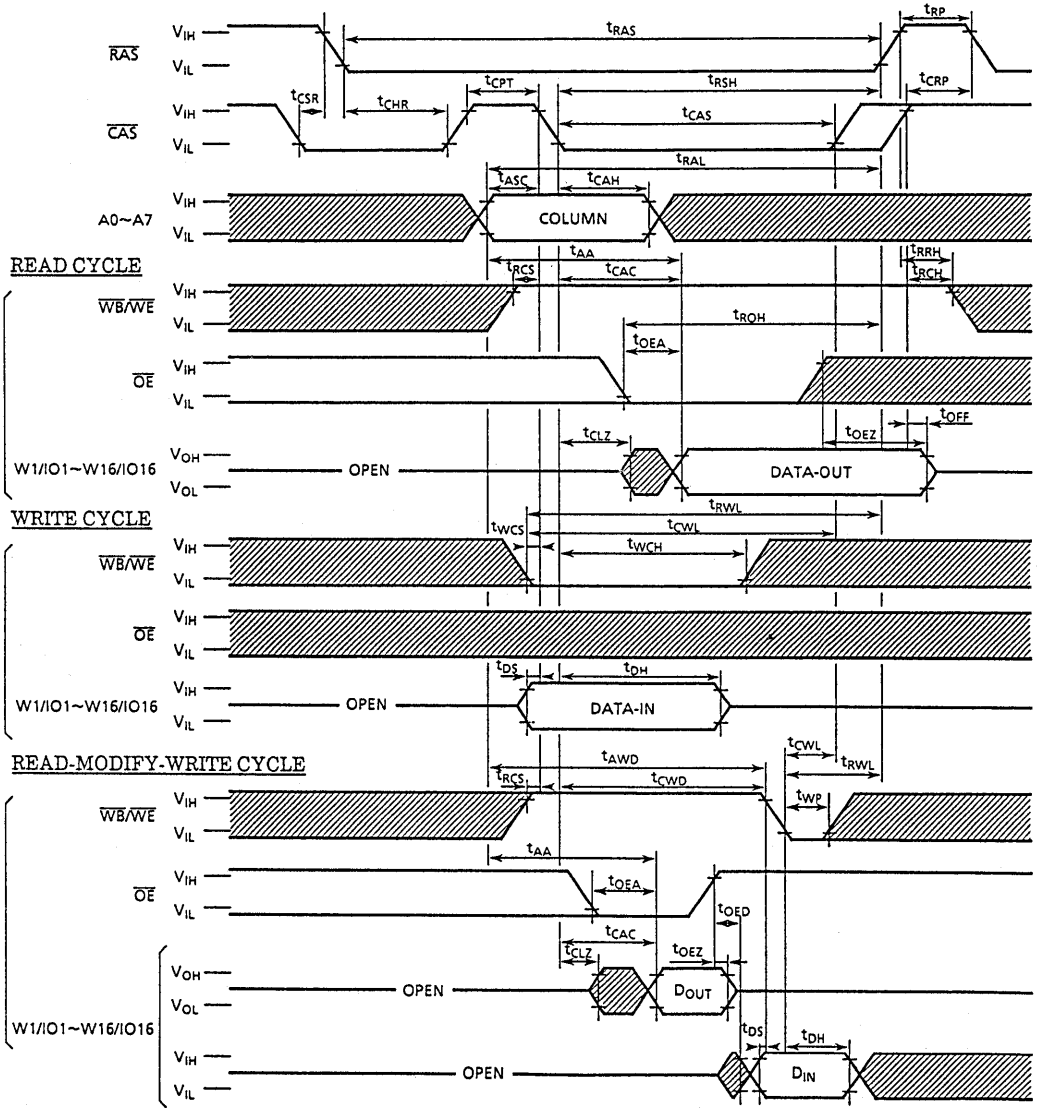
EN REFRESH CYCLE (WRITE)



Note: D_{OUT} = OPEN

: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



APPLICATION INFORMATION

ADDRESSING

The 16 address bits required to decode 1 of the 65,536 cell locations within the TC511665BJL/BZL are multiplexed onto the 8 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks.

The first clock, the Row address Strobe ($\overline{RAS}$), latches the 8 row address bits into the chip, The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 8 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$ triggers a sequence of events which are controlled by different delayed internal clocks.

The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. The "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Data Inputs

A write cycle is performed by bringing ($\overline{WB}$/) $\overline{WE}$ low during the $\overline{RAS}$/$\overline{CAS}$ operation. The falling edge of $\overline{CAS}$ or ($\overline{WB}$/) $\overline{WE}$ strobes data on (Wi/) IOi into the on-chip data latch. To make use of the write-per-bit capability $\overline{WB}$ (/$\overline{WE}$) must be low as $\overline{RAS}$ falls. In this case data bits to which the write operation is applied can be specified by keeping Wi (/IOi) high with set-up and hold times referenced to the $\overline{RAS}$ negative transition. For those data bits of Wi (/IOi) that are kept low as $\overline{RAS}$ falls the write operation is inhibited on the chip. If $\overline{WB}$(/$\overline{WE}$) is high as $\overline{RAS}$ falls, the write-per-bit capability does not work and the write operation is performed for all four data bits.

Data Outputs

The three-state output buffers provide direct TTL compatibility with a fan-out of a standard TTL load. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied.

The outputs become valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the outputs are always in the high-impedance state. In a delayed-write or read-modify-write cycle, the outputs will follow the sequence for the read cycle.

The $\overline{OE}$ controls the impedance of the output buffers. In the logic high position the buffers will remain in a high impedance state.

When the $\overline{OE}$ input is brought to a logical low level, the output buffers are enabled. Both $\overline{CAS}$ and $\overline{OE}$ can control the outputs. Thus in a read operation, either $\overline{OE}$ or $\overline{CAS}$ returning high forces the outputs into the high impedance state.

$\overline{RAS}$ ONLY REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses (A0~A7) within each 4 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles, $\overline{RAS}$ only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{CC3} specification.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH

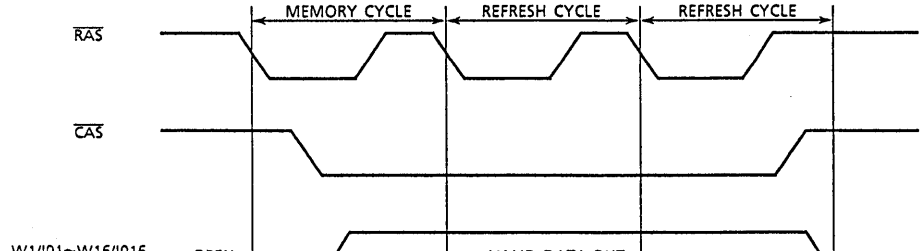
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the TC511665BJL/BZL offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generations and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

FAST PAGE MODE

The "Fast Page Mode" feature of the TC511665BJL/BZL allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "Fast page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new address is eliminated, thereby decreasing the access and cycle times.

HIDDEN REFRESH

An optional feature of the TC511665BJL/BZL is that refresh cycles may be performed while maintaining valid data at the output pins. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure below)



This feature allows a refresh cycle to be "Hidden" among data cycles without affecting the data availability.

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh operation of TC511665BJL/BZL can be tested by "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". This cycle performs READ/WRITE operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycles as initialization cycles. The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Select one certain column address and read "0" out and write "1" in each cell by performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST (READ-MODIFY-WRITE CYCLE)". Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

④ Using the same column as ②, read "1" out and write "0" in each cell performing "$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST". Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ to the complement data.

DYNAMIC RAM MODULES

262,144 WORDS×8 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM82500AS is a 262,144 words by 8 bits dynamic RAM module which assembled 2 pcs of TC514256AJ on the printed circuit board. The THM82500AS is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

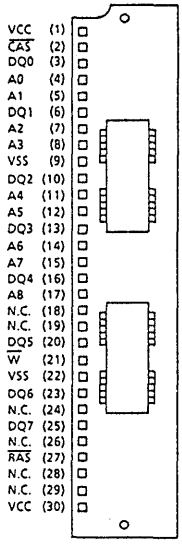
FEATURES

- 262,144words by 8 bits organization
- Fast access time and cycle time

		THM825000 AS-70	THM82500 AS-80	THM82500 AS-10
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10%
- Low power
  880mW MAX. Operating (THMxxxxxx-70)
  770mW MAX. Operating (THMxxxxxx-80)
  660mW MAX. Operating (THMxxxxxx-10)
  11mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 4ms
- Tin-Lead Contact: THM82500AS-70, 80, 10
- Gold Contact: THM82500ASG-70, 80, 10

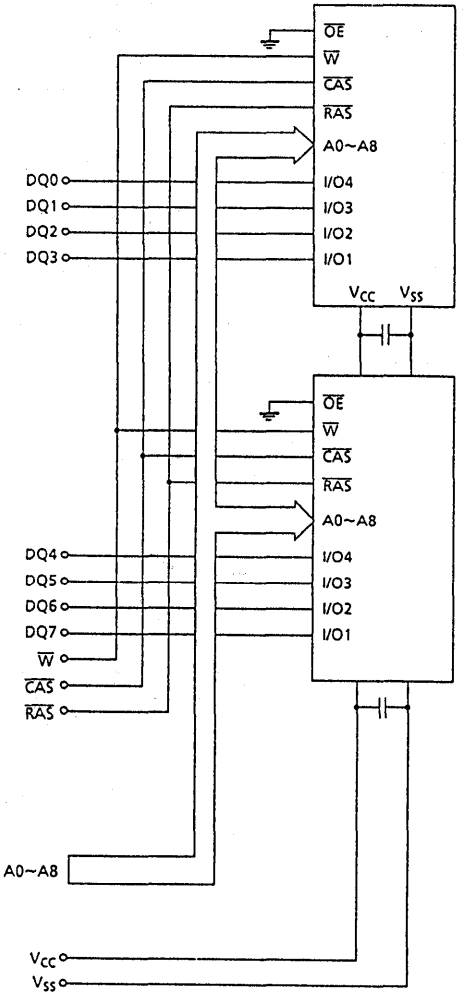
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A8	Address Inputs
DQ0~DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THM82500AS-70	–	160	mA	3, 4
		THM82500AS-80	–	140		
		THM82500AS-10	–	120		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THM82500AS-70	–	160	mA	3
		THM82500AS-80	–	140		
		THM82500AS-10	–	120		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THM82500AS-70	–	120	mA	3, 4
		THM82500AS-80	–	100		
		THM82500AS-10	–	80		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	2	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THM82500AS-70	–	160	mA	3
		THM82500AS-80	–	140		
		THM82500AS-10	–	120		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 20	20	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM82500AS-70		THM82500AS-80		THM82500AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM82500AS-70		THM82500AS-80		THM82500AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	8	-	8	-	8	ms	
t_{WCS}	Write Command Set-UP Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	

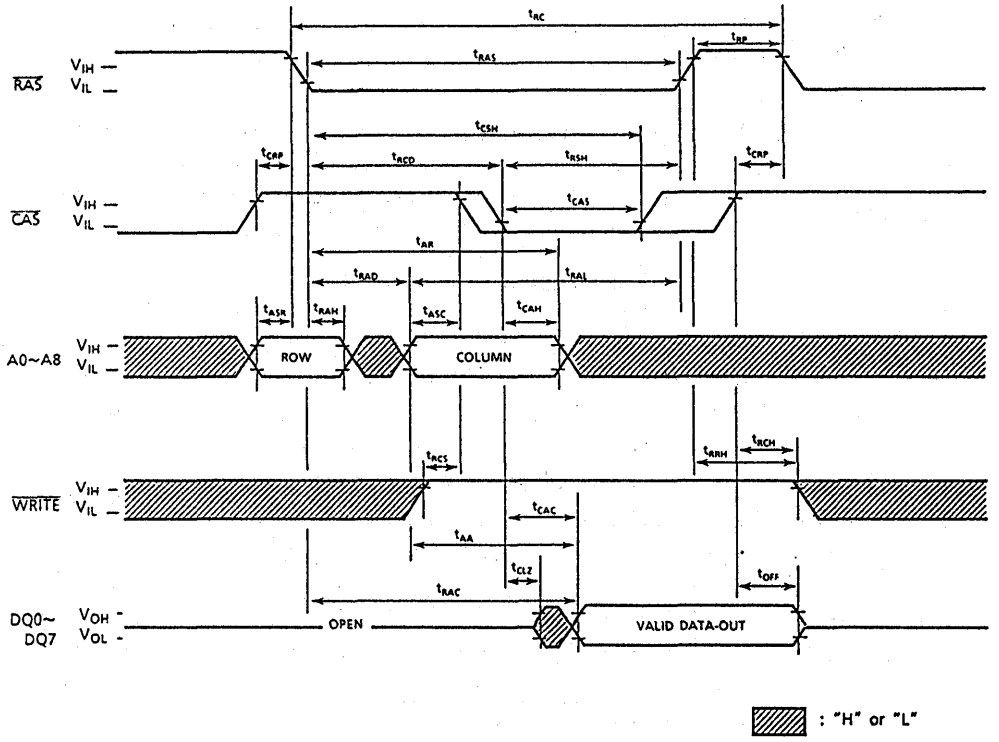
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	-	25	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	-	12	pF

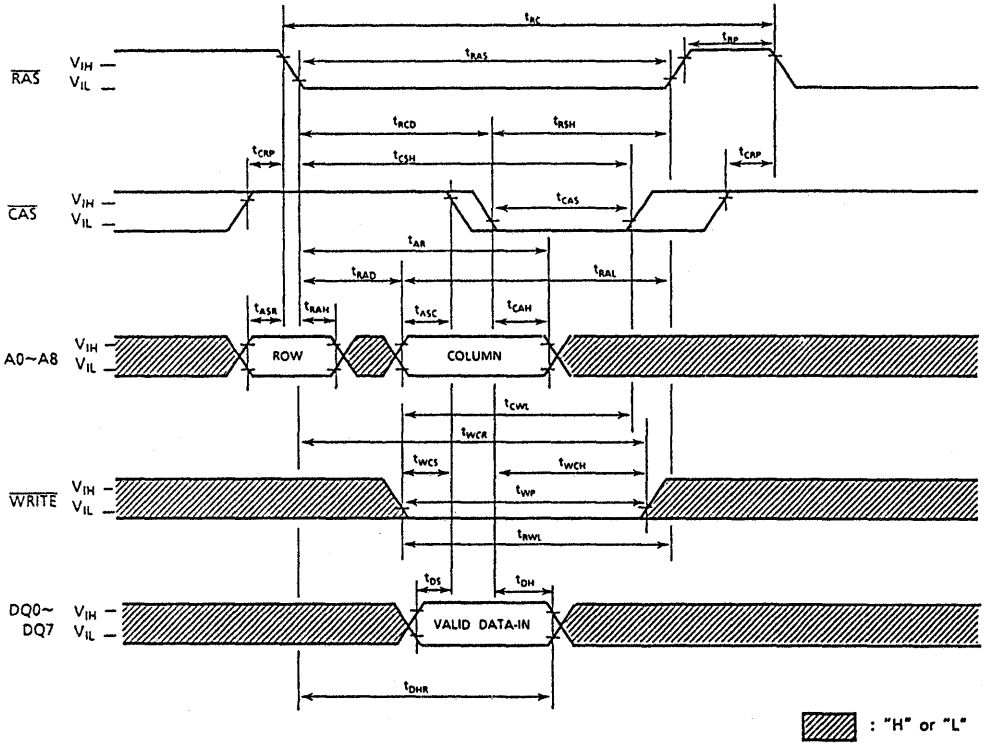
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

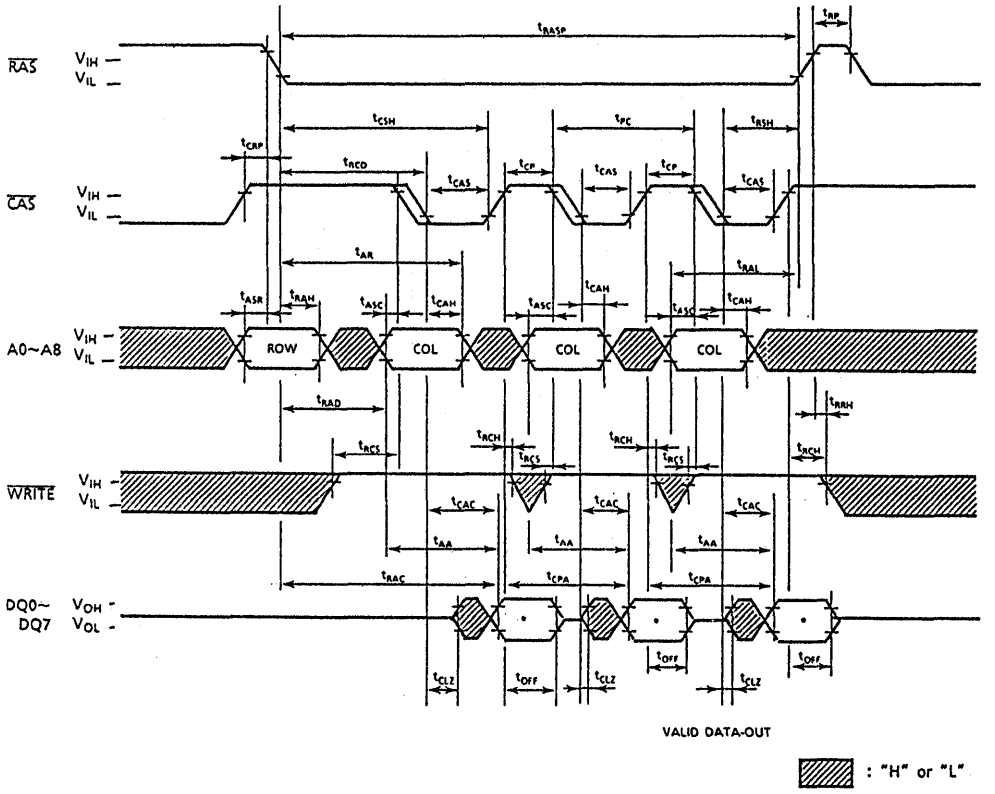
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~
DQ7
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

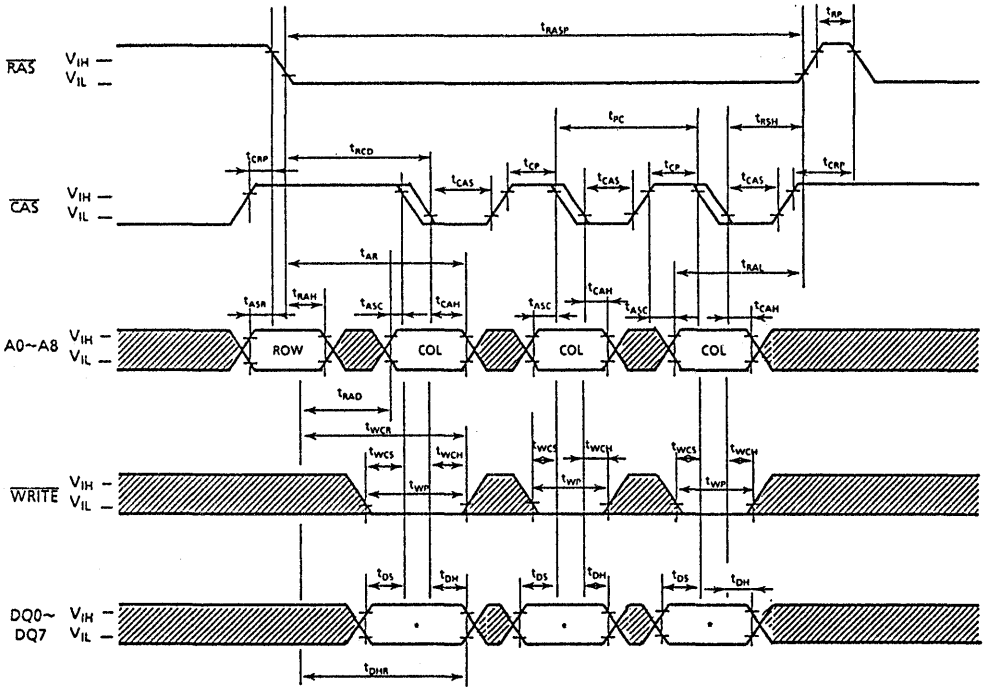
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



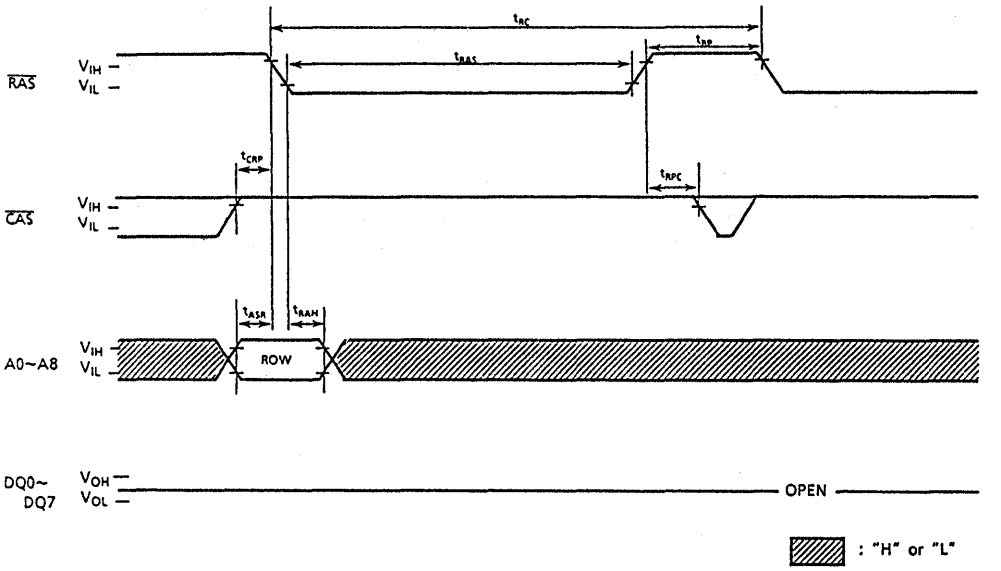
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA-IN

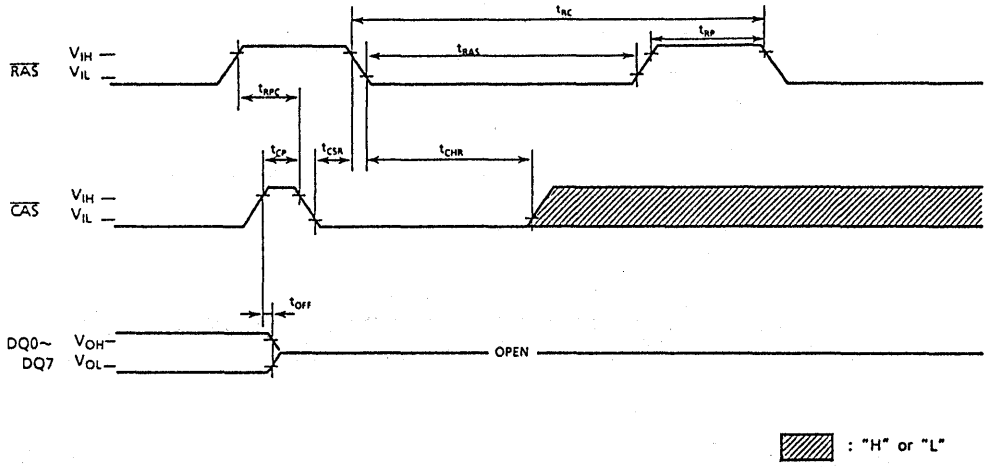
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



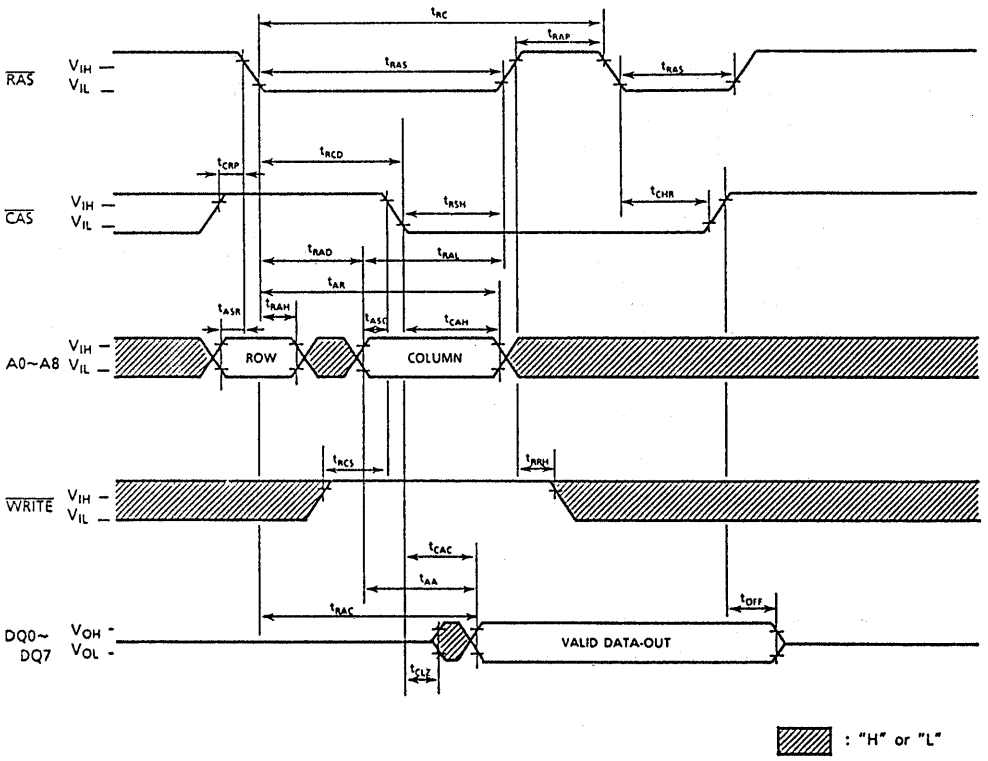
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

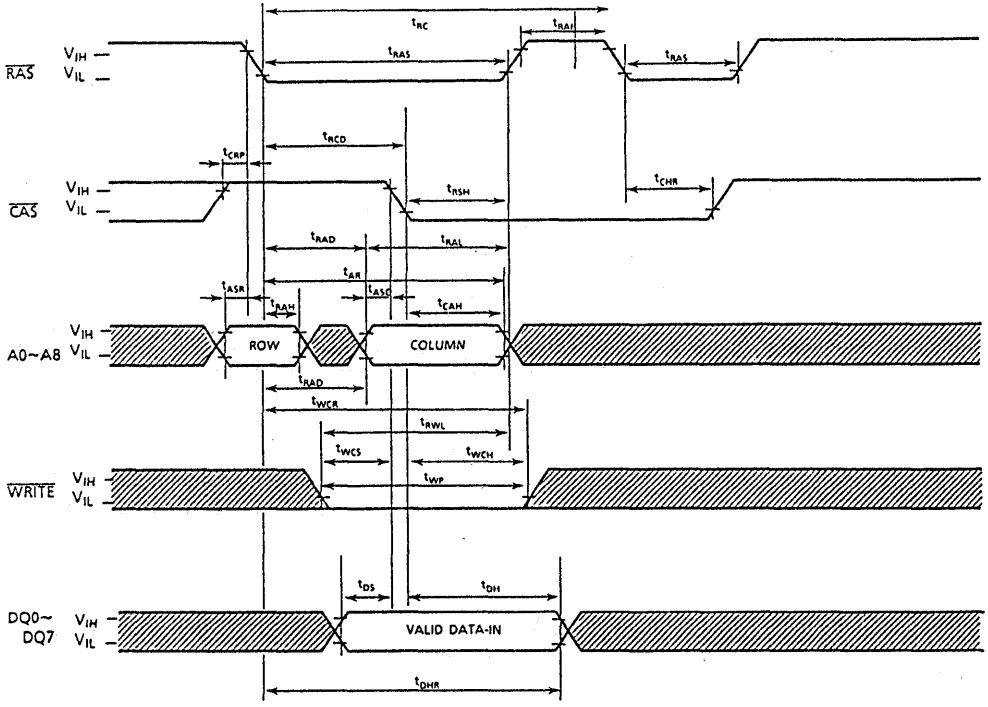


Note: $\overline{WRITE}$ = "H" or "L", A0~A8 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

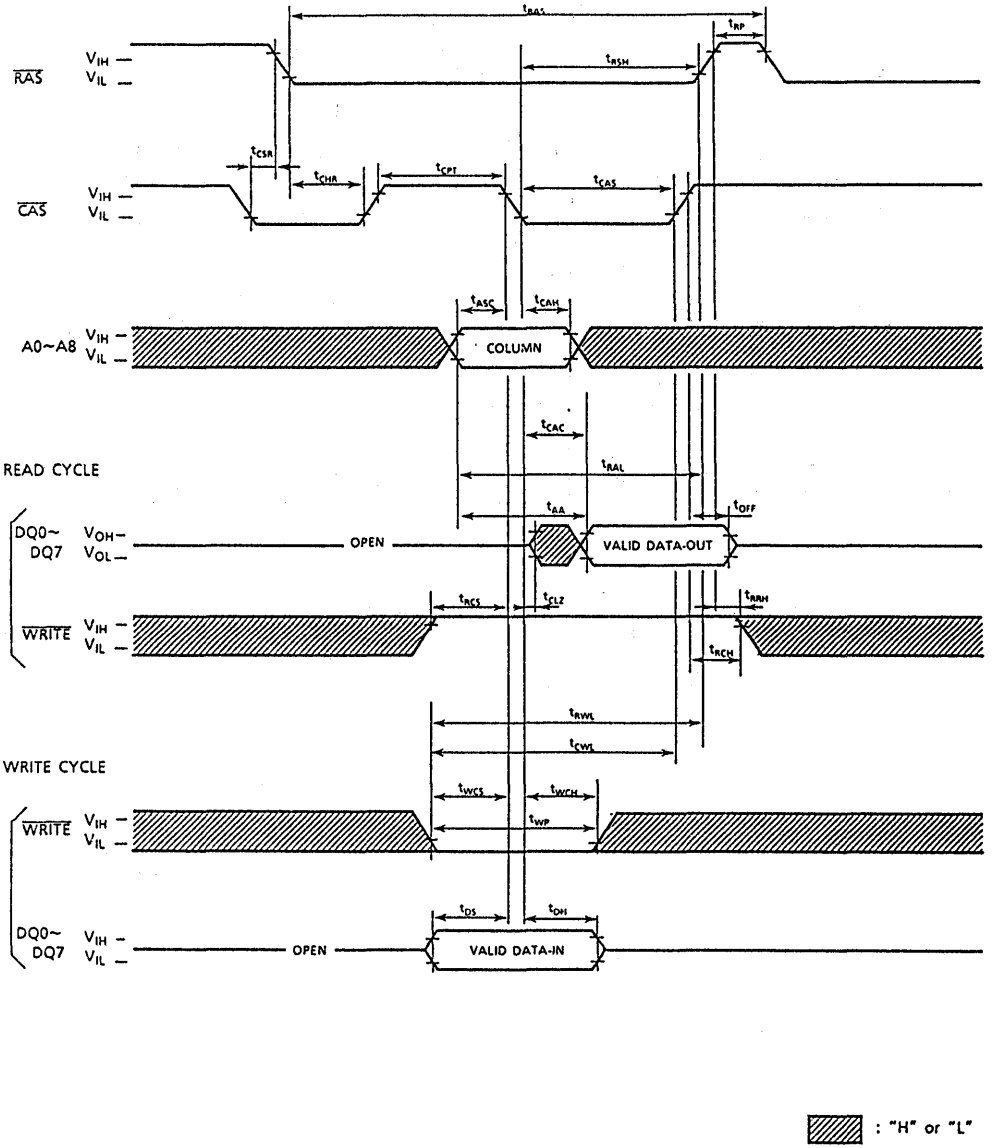


HIDDEN REFRESH CYCLE (WRITE)



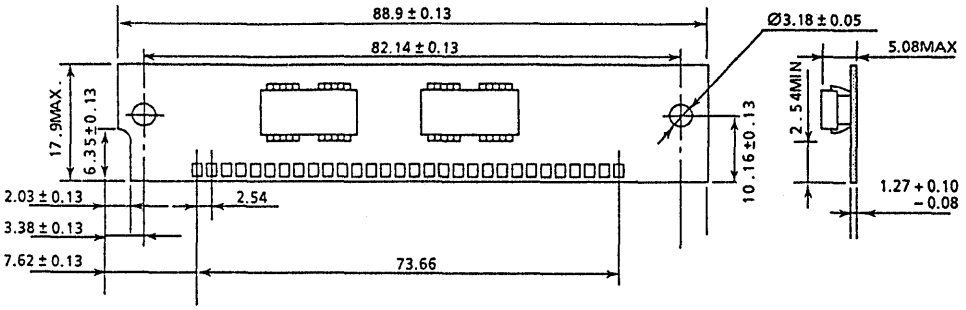
: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CYCLE



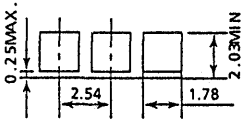
OUTLINE DRAWINGS

Unit : mm



• THM82500AS

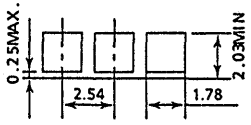
DETAIL OF CONTACTS



Contacts : Tin-Lead

• THM82500ASG

DETAIL OF CONTACTS



Contacts : Gold

NOTES

262,144 WORDS x 9 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM92500AS is a 262,144 words by 9 bits dynamic RAM module which assembled 2 pcs of TC514256AJ and 1 pcs of TMM51256T on the printed circuit board.

The THM92500AS is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

FEATURES

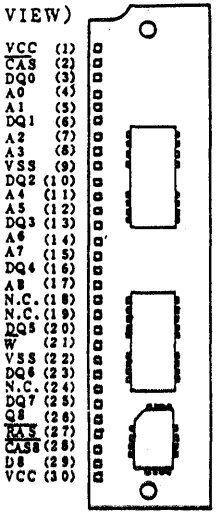
- 262,144 words by 9 bits organization
- Fast access time

		THM92500AS-70	THM92500AS-80	THM92500AS-10
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10%
- Low power
  1320mW MAX. Operating(THM92500AS-70)
  1155mW MAX. Operating(THM92500AS-80)
  990mW MAX. Operating(THM92500AS-10)
  16.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/4ms

PIN CONNECTION

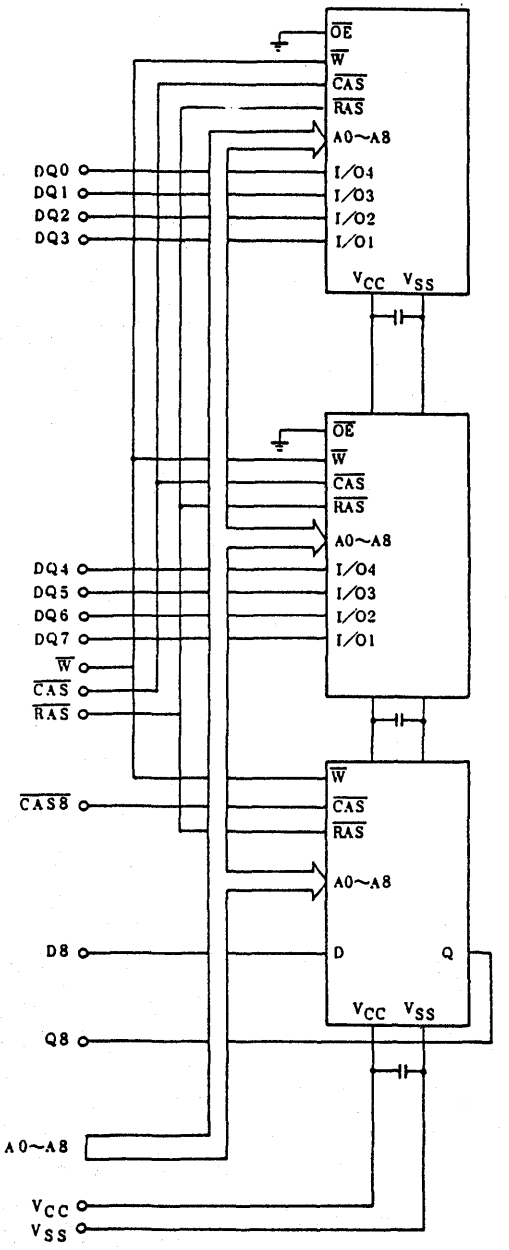
(TOP VIEW)



PIN NAMES

A0 ∿ A8	Address Inputs
DQ0 ∿ DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0∿7.0	V	1
Output Voltage	V_{OUT}	-1.0∿7.0	V	1
Power Supply Voltage	V_{CC}	-1.0∿7.0	V	1
Operating Temperature	T_{OPR}	0∿70	°C	1
Storage Temperature	T_{STG}	-55∿125	°C	1
Soldering Temperature • Time	T_{SOLDER}	260 • 10	°C • sec	1
Power Dissipation	P_D	1.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0∿70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} MIN.)	THM92500AS-70	-	240	mA	3, 4
		THM92500AS-80	-	210		
		THM92500AS-10	-	180		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{IH})		-	6	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	THM92500AS-70	-	240	mA	3
		THM92500AS-80	-	210		
		THM92500AS-10	-	180		
I_{CC4}	FAST PAGE MODE Average Power Supply Current, Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} MIN.)	THM92500AS-70	-	180	mA	3, 4
		THM92500AS-80	-	150		
		THM92500AS-10	-	120		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$=$\overline{CAS}$=V_{CC}-0.2V)		-	3	mA	
I_{CC6}	CAS BEFORE RAS REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	THM92500AS-70	-	240	mA	3
		THM92500AS-80	-	210		
		THM92500AS-10	-	180		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V≦V_{IN}≦6.5V, All Other Pins not under Test=0V)		-30	30	μA	
$I_{O(L)}$	OUTPUT LEAKAGE (D_{OUT} is disabled, 0V≦V_{OUT}≦5.5V)		-10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	-	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT}=4.2mA)		-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM95200AS						UNIT	NOTES
		-70		-80		-10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	-	150	-	180	-	ns	
t_{PC}	Fast Page Mode Cycle Time	40	-	45	-	55	-	ns	
t_{RAC}	Access Time from $\overline{RAS}$	-	70	-	80	-	100	ns	8,13
t_{CAC}	Access Time from $\overline{CAS}$	-	20	-	20	-	25	ns	8,13
t_{AA}	Access Time from Column Address	-	35	-	40	-	50	ns	8,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	50	ns	8,14
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	6
t_{RP}	$\overline{RAS}$ Precharge Time	50	-	60	-	70	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	-	20	-	25	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	-	80	-	100	-	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	-	10	-	10	-	ns	
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	15	-	ns	
t_{ASC}	Column Address Set-Up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	15	-	15	-	20	-	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	-	40	-	50	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	15	-	15	-	20	-	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THM92500AS						UNITS	NOTES
		-70		-80		-10			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{WP}	Write Command Pulse Width	15	-	15	-	20	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	-	20	-	25	-	ns	
t_{DS}	Data Set-Up Time	0	-	0	-	0	-	ns	11
t_{DH}	Data Hold Time	15	-	15	-	20	-	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	-	60	-	75	-	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_{WCS}	Write Command Set-Up Time	0	-	0	-	0	-	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	30	-	30	-	30	-	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	-	0	-	0	-	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	-	40	-	50	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10	-	10	-	15	-	ns	

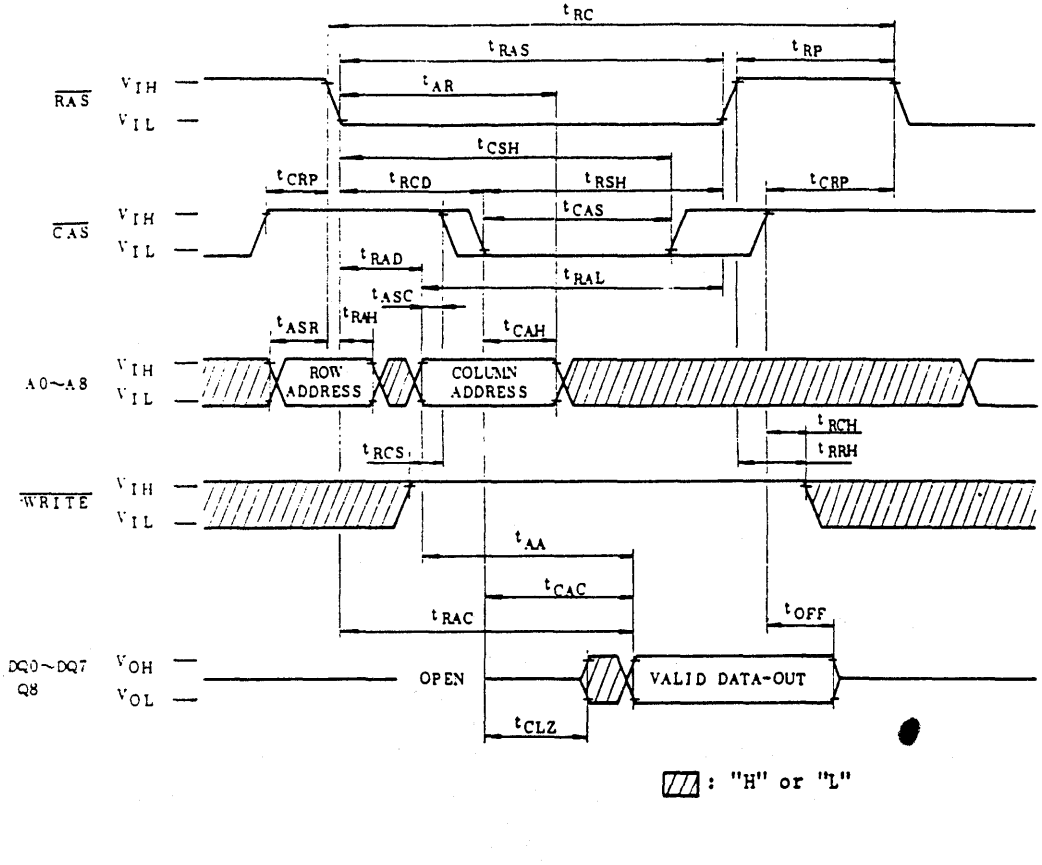
CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$, $\overline{CAS8}$, D8)	-	21	pF
C_{DQ}	I/O Capacitance (DQ0∿DQ7, Q8)	-	7	pF

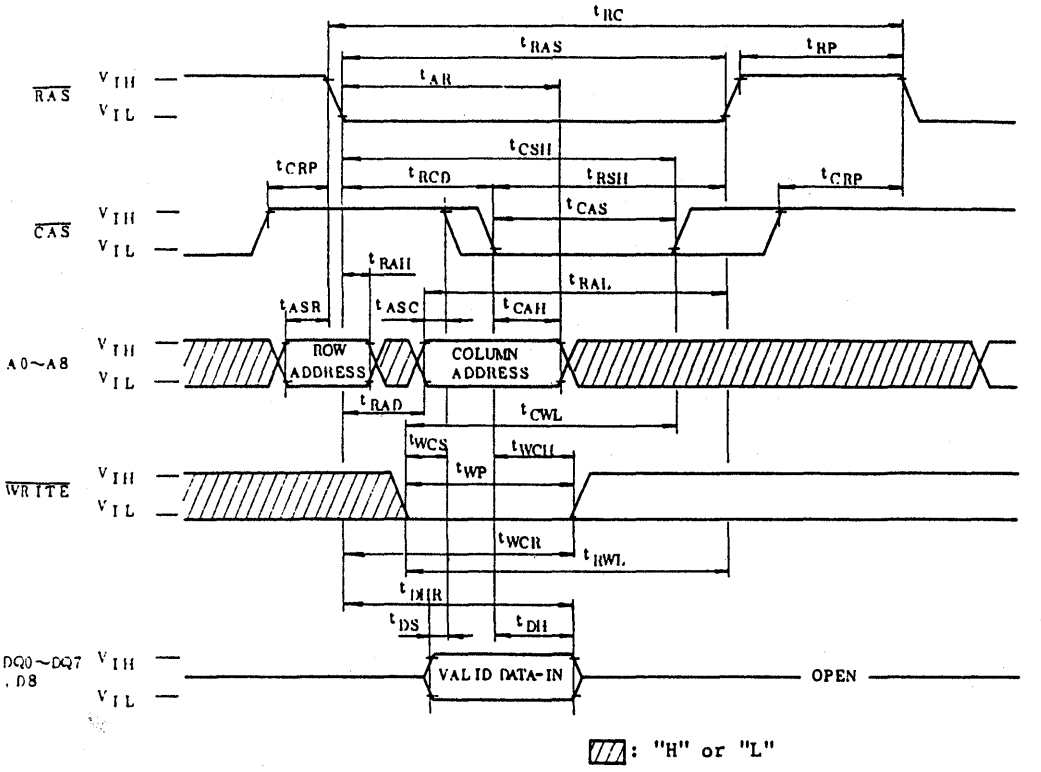
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

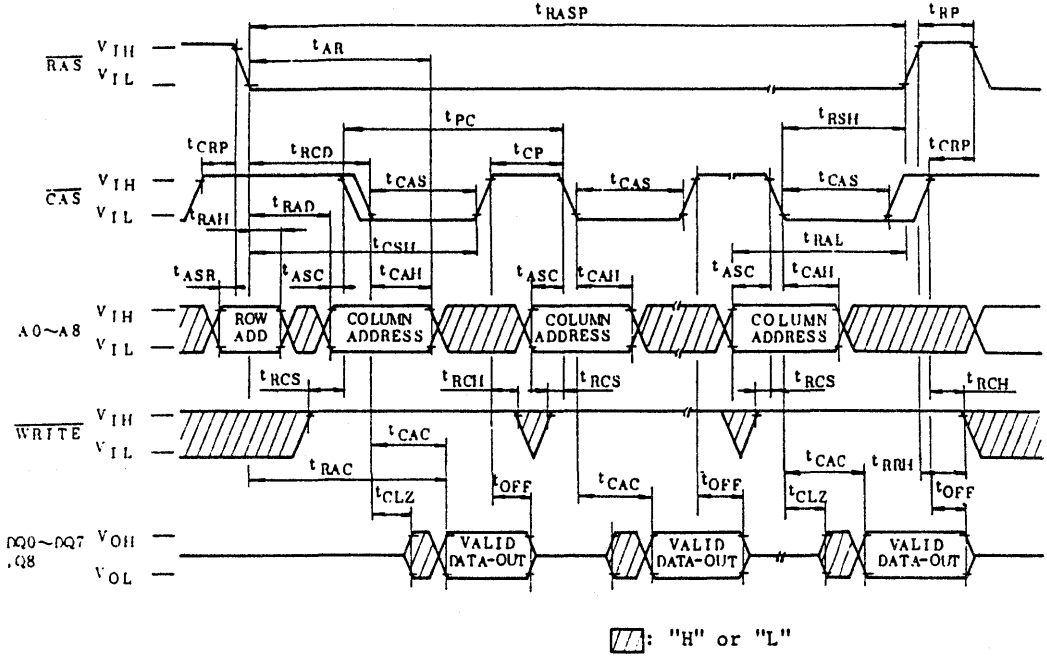
READ CYCLE


tRC
tRAS
tRP
RAS
VIH
VIL
tAR
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH
VIL
tCAS
tRAD
tRAL
tASC
tASR
tRAH
tCAH
A0~A8
VIH
VIL
ROW ADDRESS
COLUMN ADDRESS
tRCH
tRRH
tRCS
WRITE
VIH
VIL
tAA
tCAC
tRAC
tOFF
DQ0~DQ7
Q8
VOH
VOL
OPEN
VALID DATA-OUT
tCLZ
: "H" or "L"

READ WRITE CYCLE

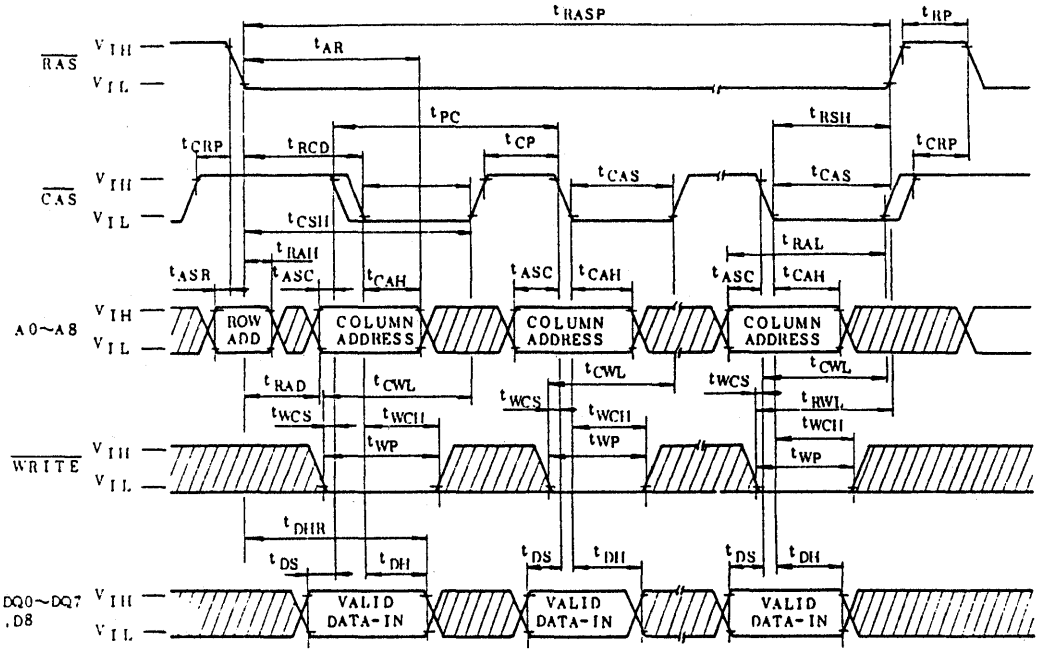


FAST PAGE MODE READ CYCLE



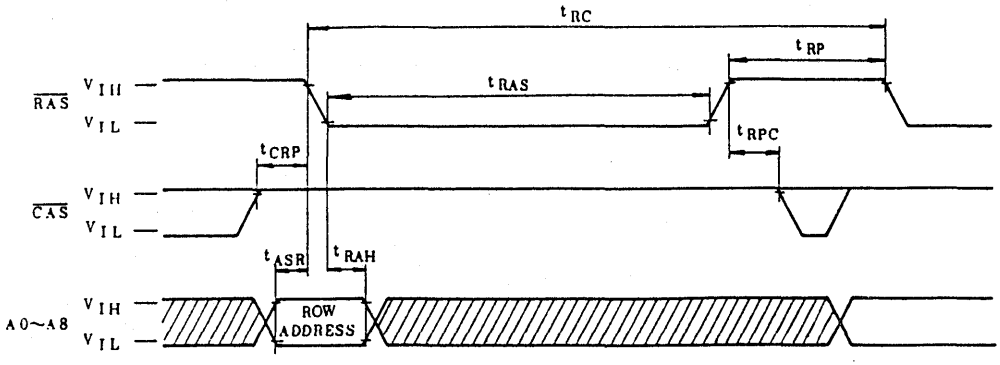
: "H" or "L"

FAST PAGE MODE WRITE CYCLE



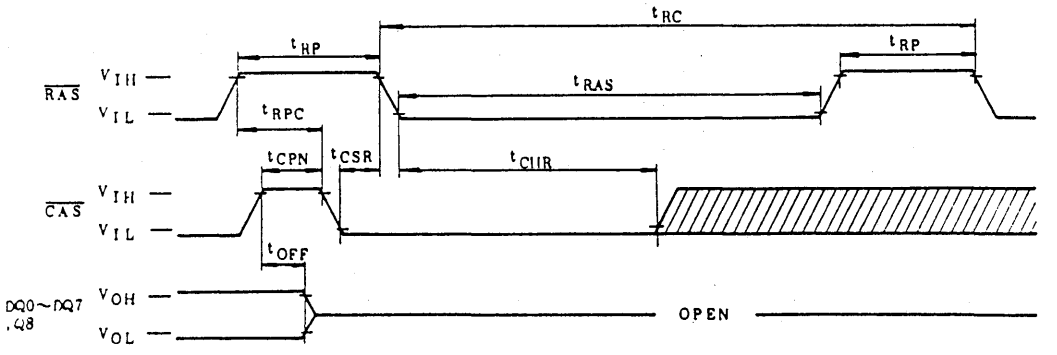
▨: "H" or "L"

RAS ONLY REFRESH CYCLE



Note: WRITE="H" or "L" ▨: "H" or "L"

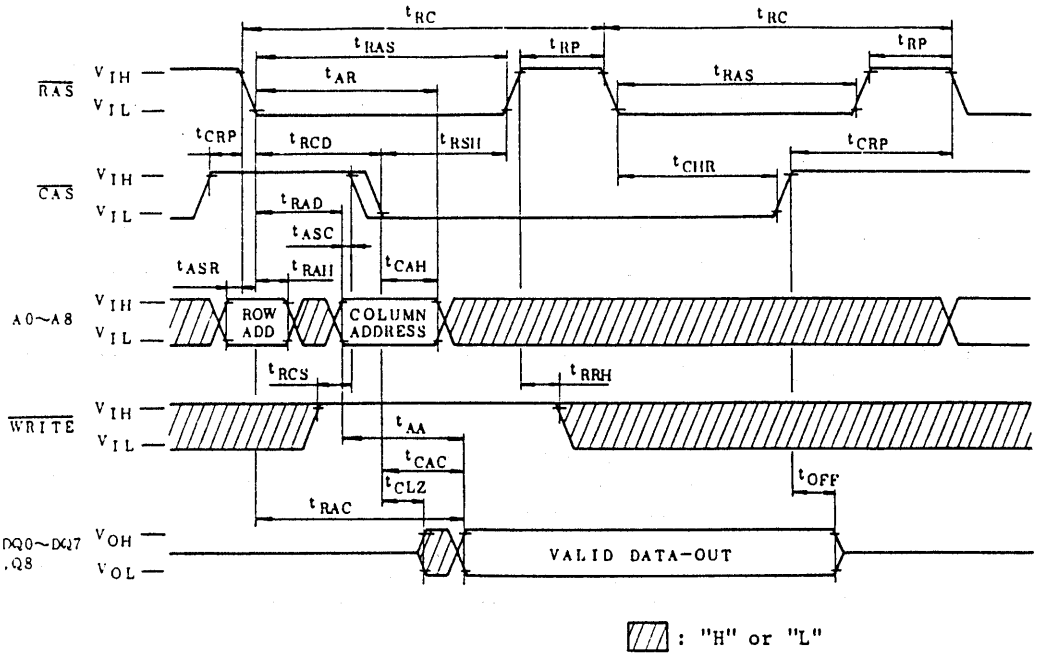
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



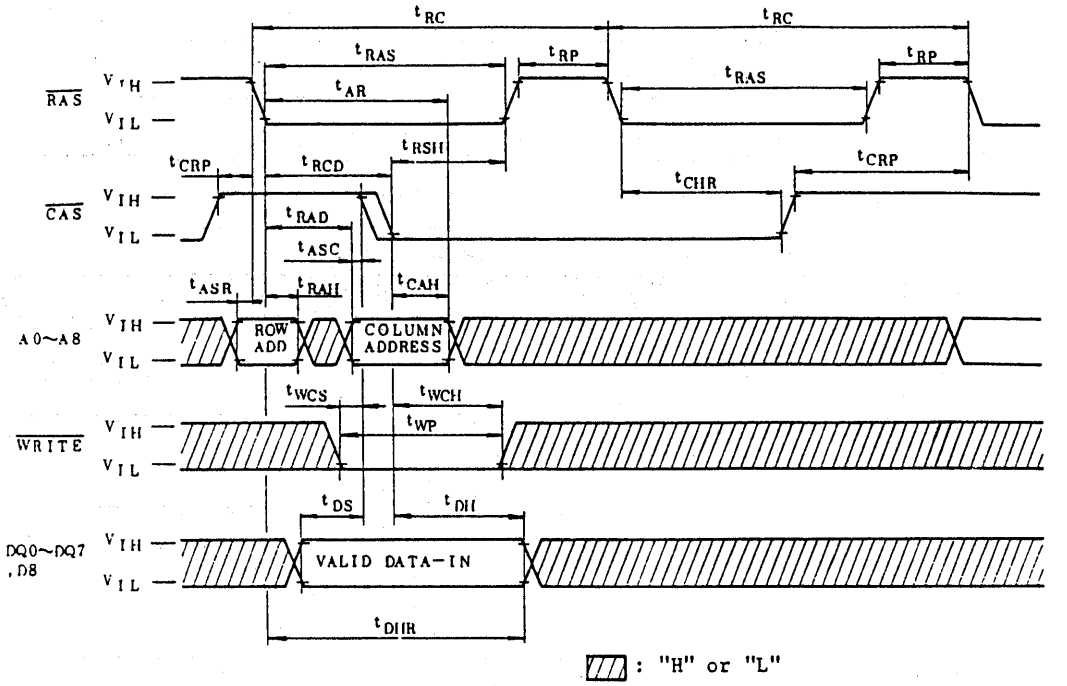
Note: $\overline{WRITE}$, A0 ~ A8="H" or "L"

▨ : "H" or "L"

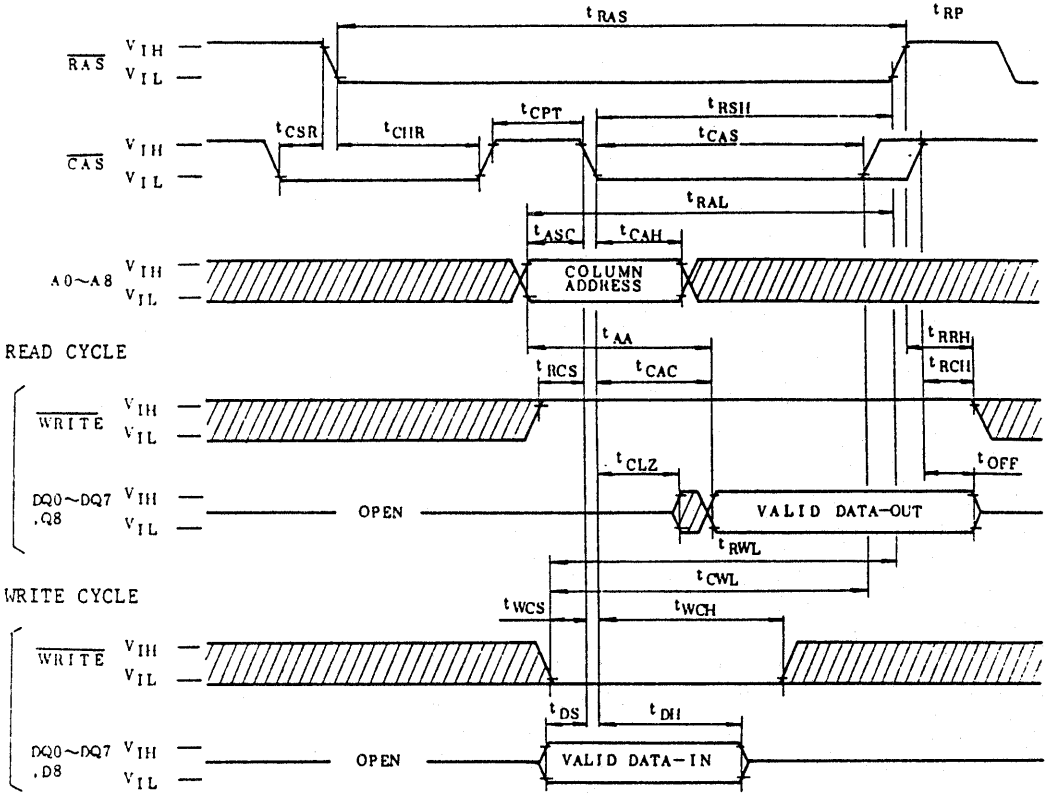
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



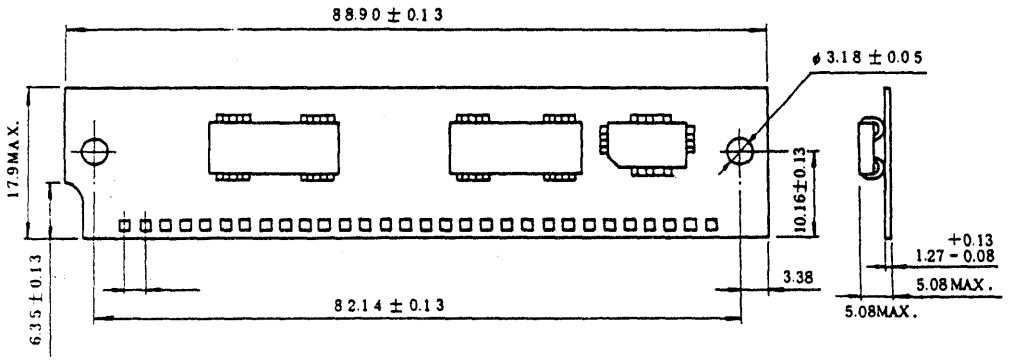
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OUTLINE DRAWINGS

THM92500AS

Unit in mm



262,144 WORDS×9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM92500BS is a 262,144 words by 9 bits dynamic RAM module which assembled 2 pcs of TC514256BJ and 1pcs of TC51256T on the printed circuit board. The THM92500BS is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

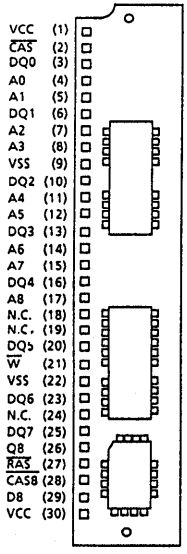
FEATURES

- 262,144words by 9 bits organization
- Fast access time and cycle time

		THM92500BS/BSG-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	115ns
t_{PC}	Fast Page Mode Cycle Time	40ns

- Single power supply of 5V±10%
- Low power
  1,485mW MAX. Operating
  16.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 4ms (Burst Refresh)
- 512 refresh cycles/ 8ms (Distributed Refresh)
- Tin-Lead Contact: THM92500BS-60
- Gold Contact: THM92500BSG-60

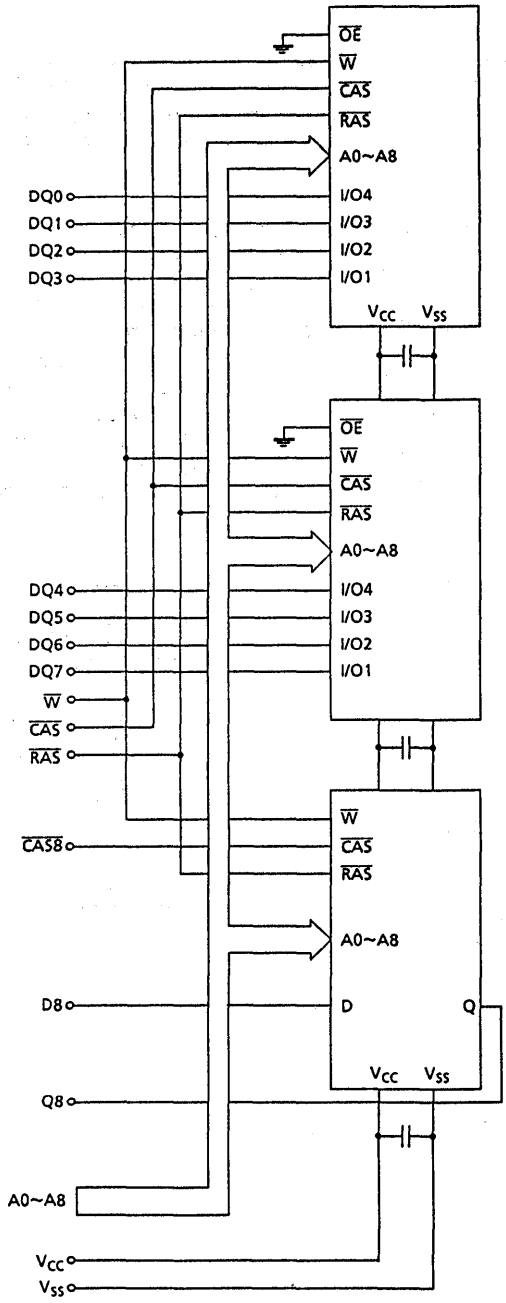
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A8	Address Inputs
DQ0~DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	–	270	mA	3, 4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	6	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	–	270	mA	3
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	–	180	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	3	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	–	270	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)	−30	30	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	−10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = −5mA)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read or Write Cycle Time	115	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	8, 13
t_{AA}	Access Time from Column Address	–	30	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	45	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{WP}	Write Command Pulse Width	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	11
t_{DH}	Data Hold Time	15	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	ns	

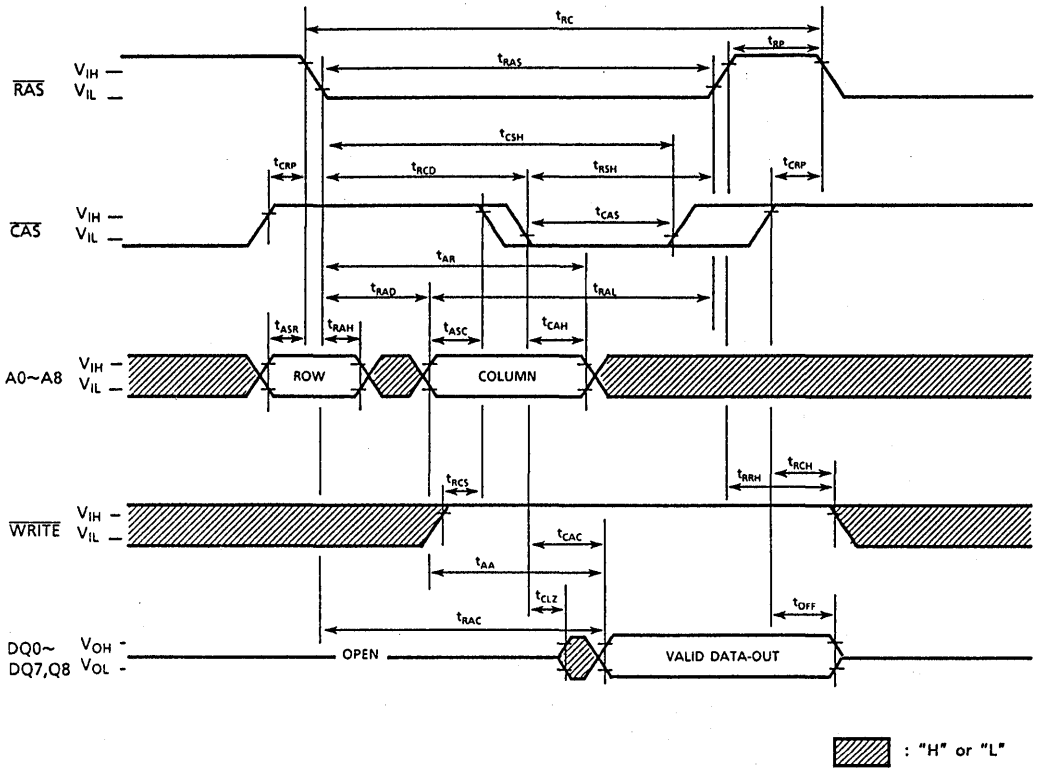
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A8, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	27	pF
C_{I2}	Input Capacitance (D8,$\overline{CAS8}$)	–	10	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	–	15	pF
C_{Q}	Input Capacitance (Q8)	–	10	pF

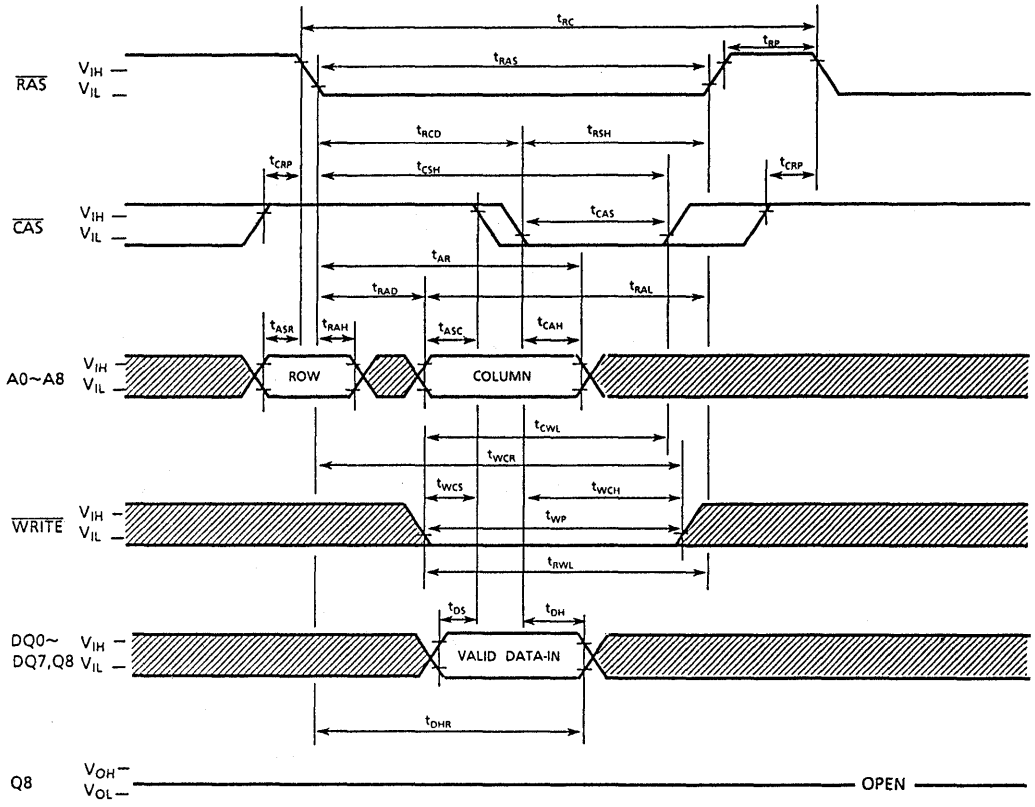
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

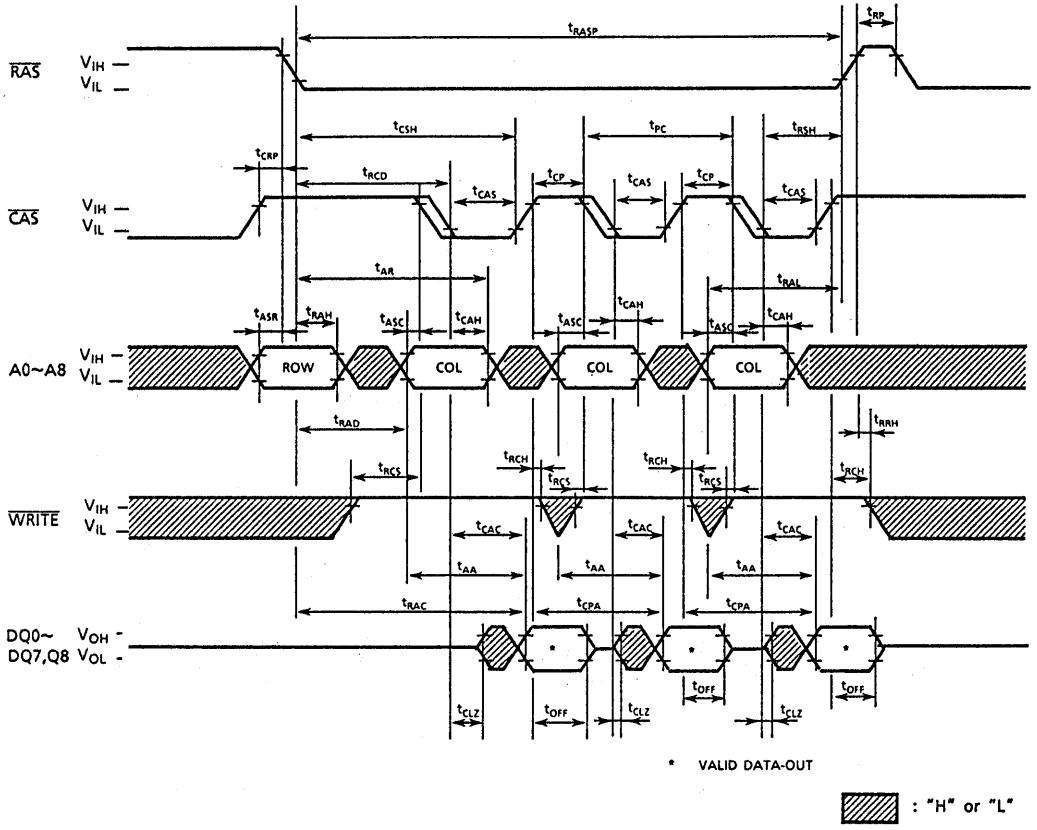

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~
DQ7,Q8
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

EARLY WRITE CYCLE

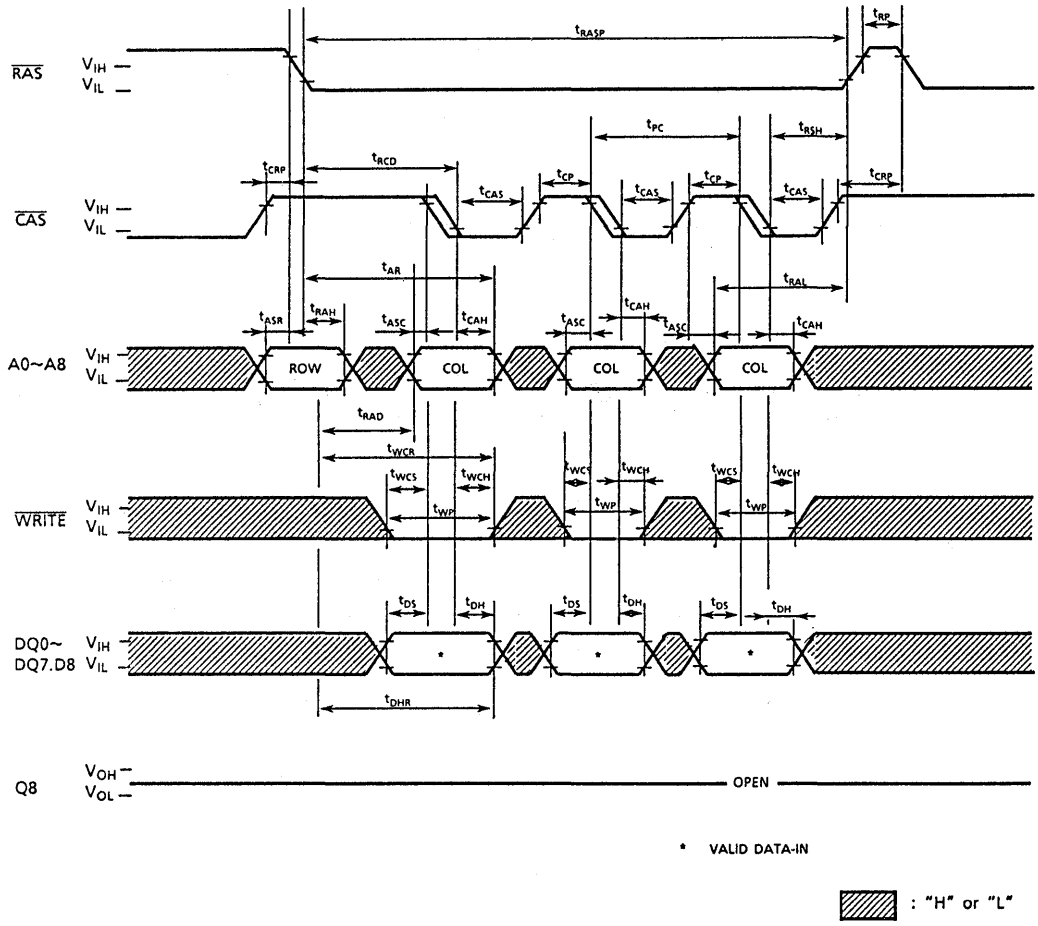


▨ : "H" or "L"

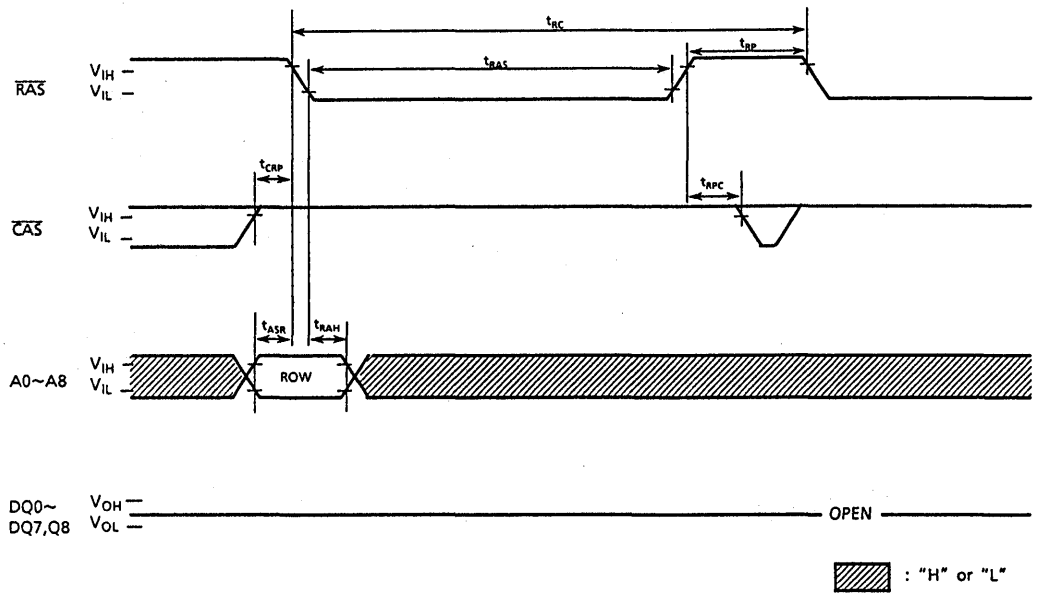
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

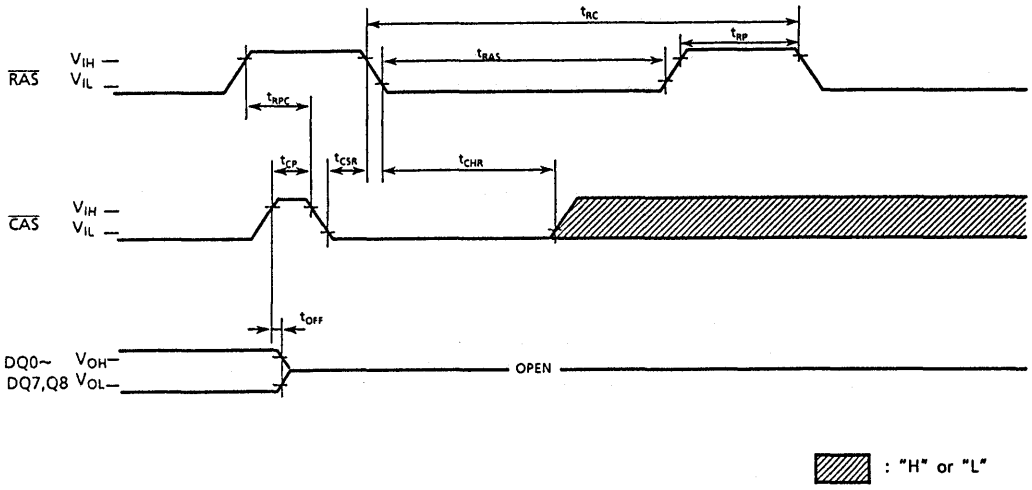


$\overline{RAS}$ ONLY REFRESH CYCLE



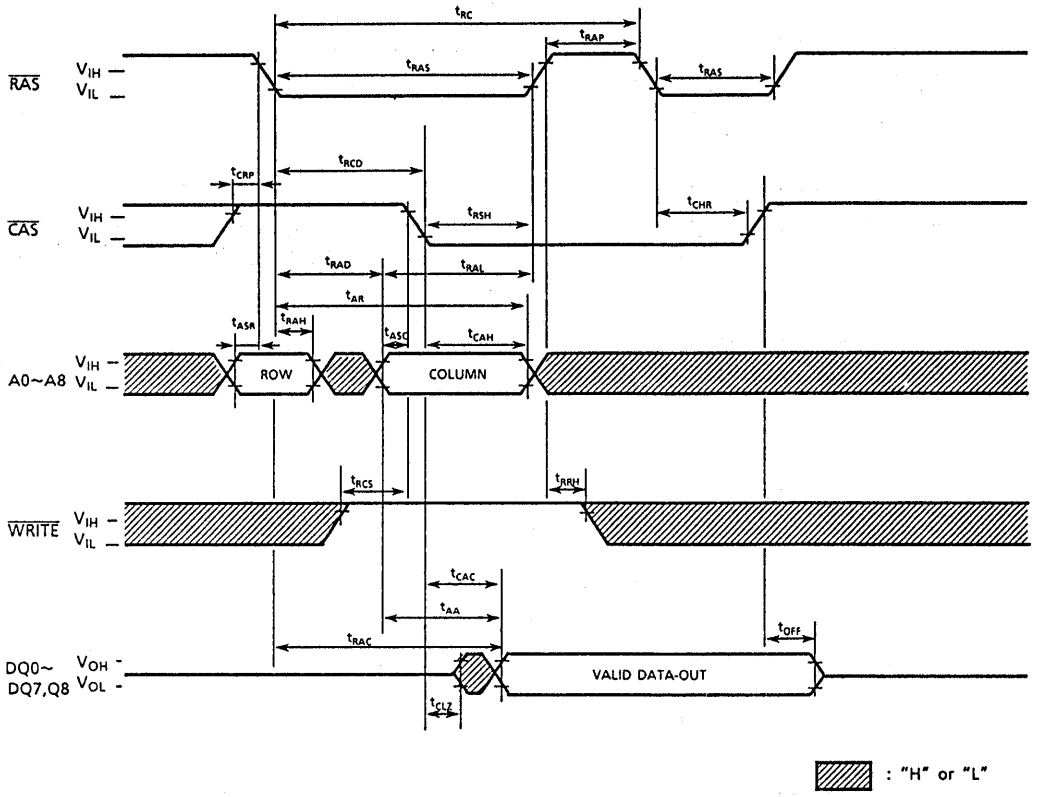
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

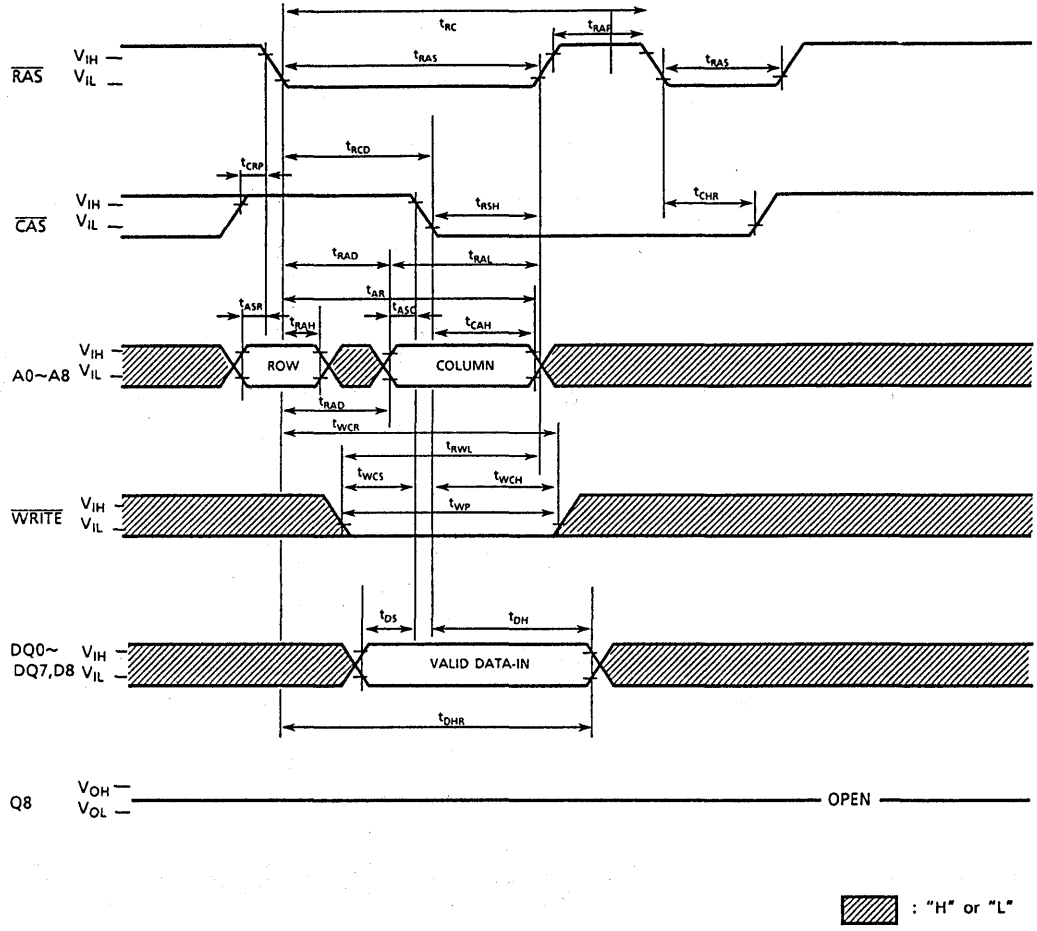


Note: $\overline{WRITE}$ = "H" or "L", A0~A8 = "H" or "L"

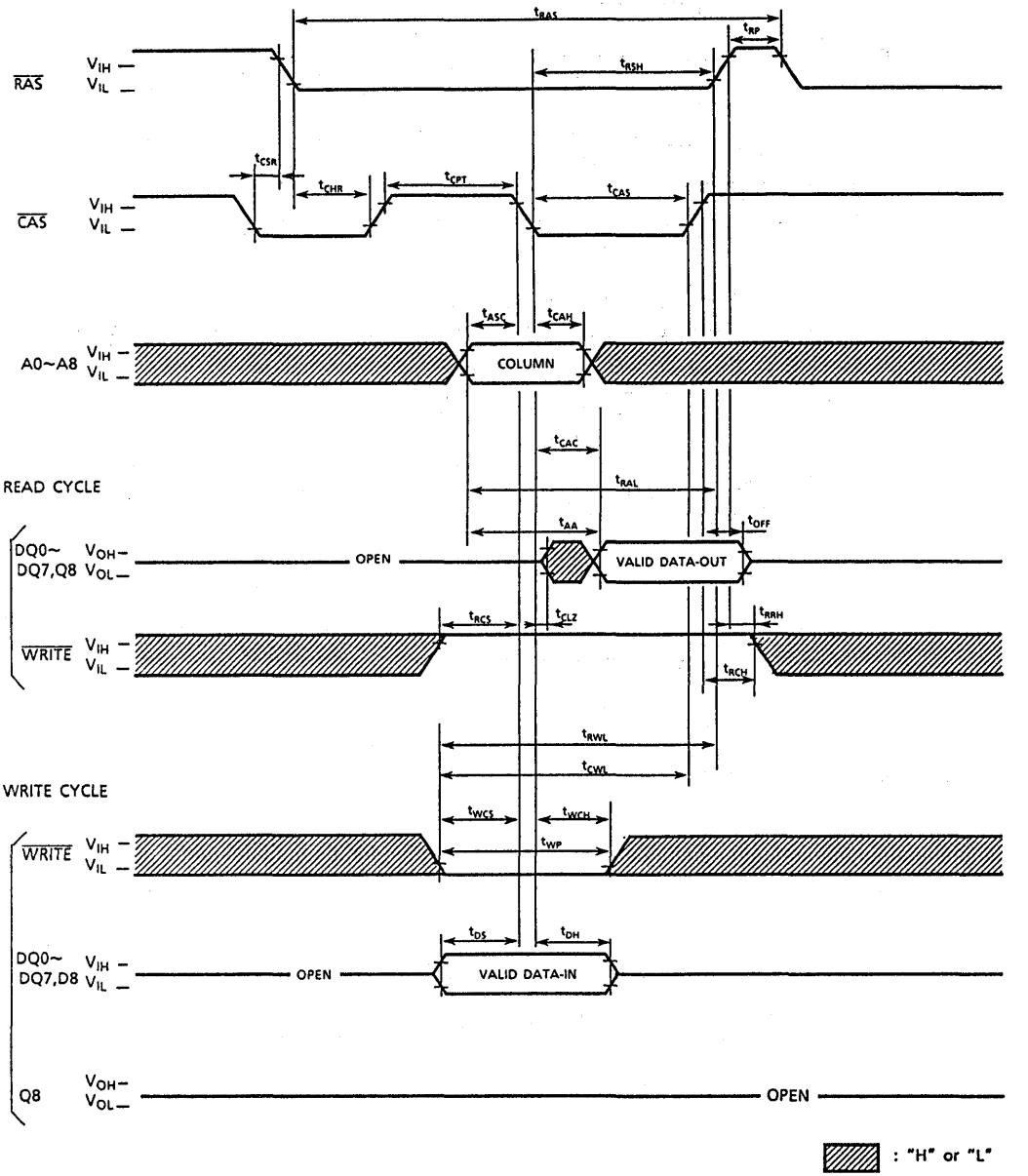
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

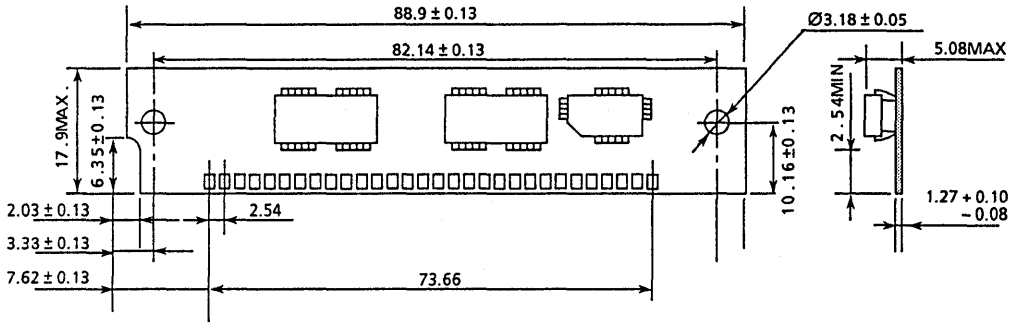


CAS BEFORE RAS REFRESH COUNTER CYCLE



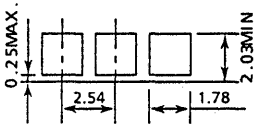
OUTLINE DRAWINGS

Unit : mm



● THM92500BS

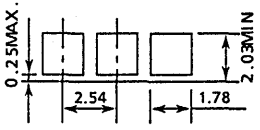
DETAIL OF CONTACTS



Contacts : Tin-Lead

● THM92500BSG

DETAIL OF CONTACTS



Contacts : Gold

NOTES

1,048,576 WORDS × 8 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM81000AS/ASG/AL is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000AJ on the printed circuit board. The THM81000AS/AL is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

FEATURES

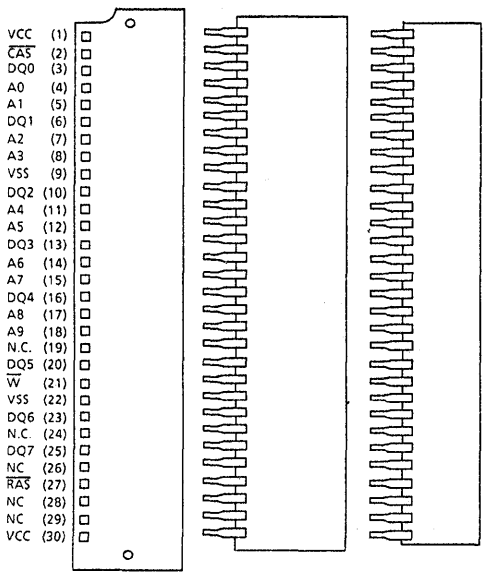
- 1,048,576 words by 8 bits organization
- Fast access time and cycle time

		THM81000 AS-70	THM81000 AS-80	THM81000 AS-10
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10%
- Low power
  3,520mW MAX. Operating (THMxxxxxx-70)
  3,080mW MAX. Operating (THMxxxxxx-80)
  2,640mW MAX. Operating (THMxxxxxx-10)
  44.0mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 8ms
- Tin-Lead Contact : THM81000AS-70, 80, 10

PIN CONNECTION (TOP VIEW)

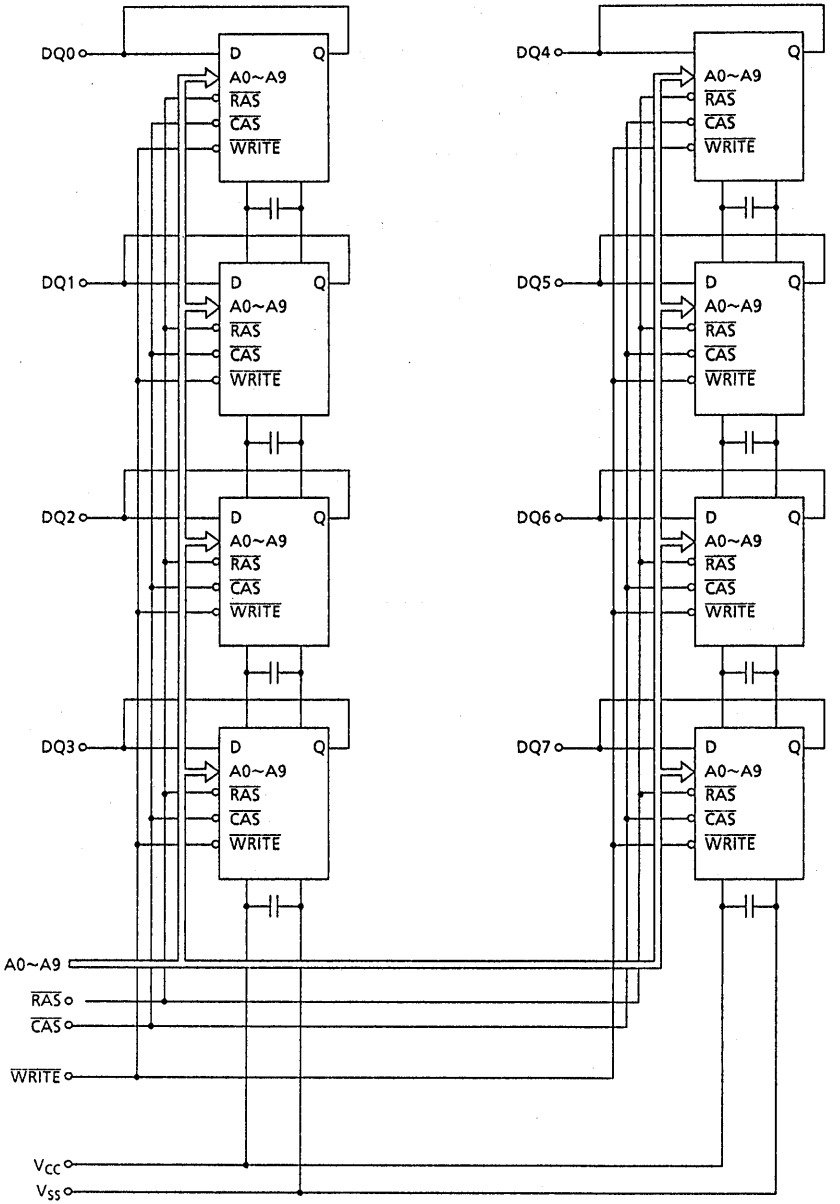
THM81000AS THM81000AL THM81020AL



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THM81000AS-70	–	640	mA	3, 4
		THM81000AS-80	–	560		
		THM81000AS-10	–	480		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THM81000AS-70	–	640	mA	3
		THM81000AS-80	–	560		
		THM81000AS-10	–	480		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THM81000AS-70	–	480	mA	3, 4
		THM81000AS-80	–	400		
		THM81000AS-10	–	320		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THM81000AS-70	–	640	mA	3
		THM81000AS-80	–	560		
		THM81000AS-10	–	480		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		–80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		–20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = –5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM81000AS-70		THM81000AS-80		THM81000AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM81000AS-70		THM81000AS-80		THM81000AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	

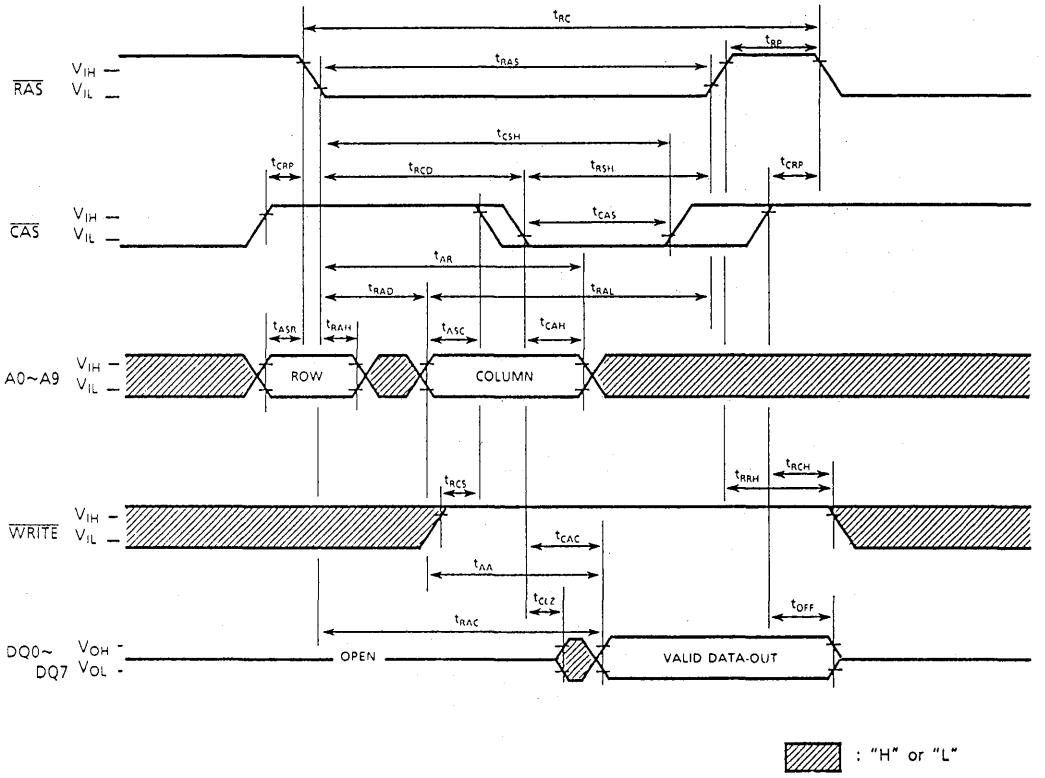
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	–	15	pF

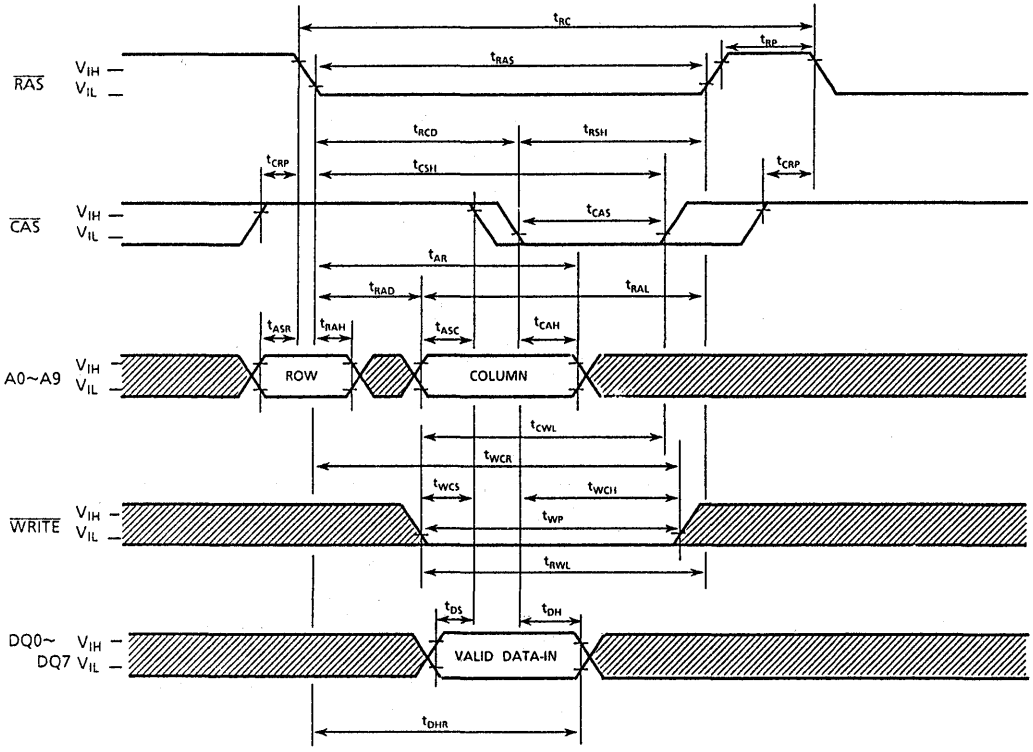
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

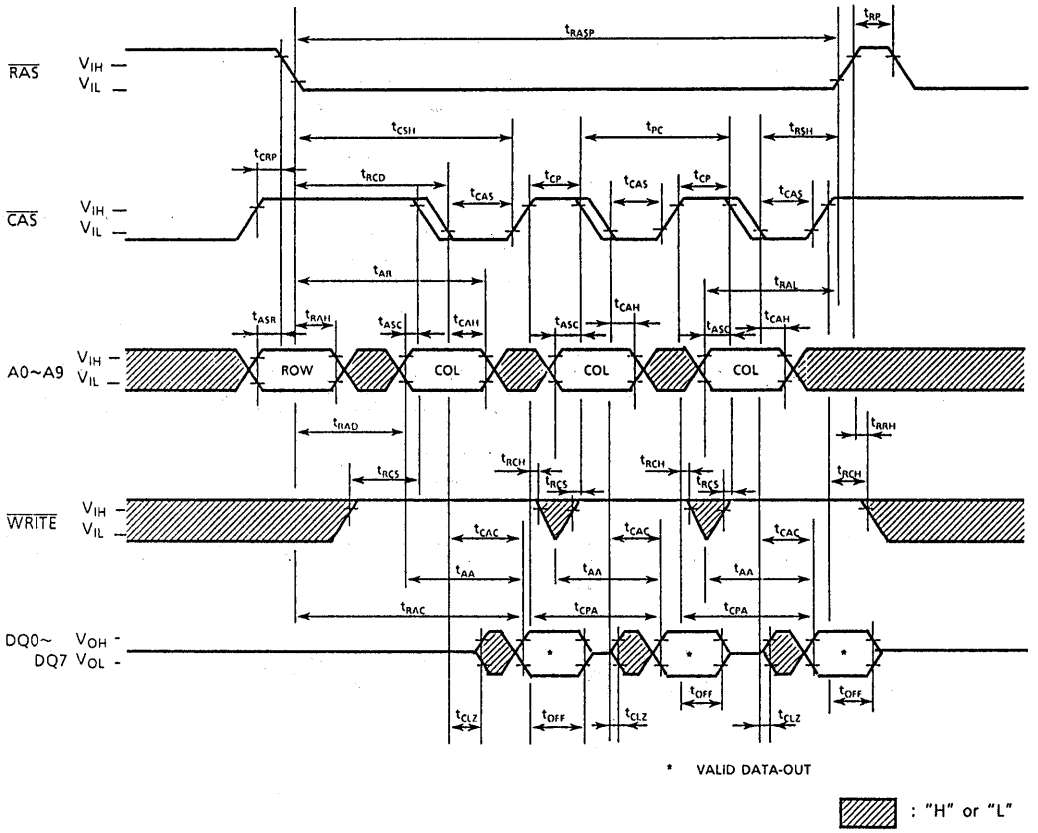

tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~DQ7
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

EARLY WRITE CYCLE

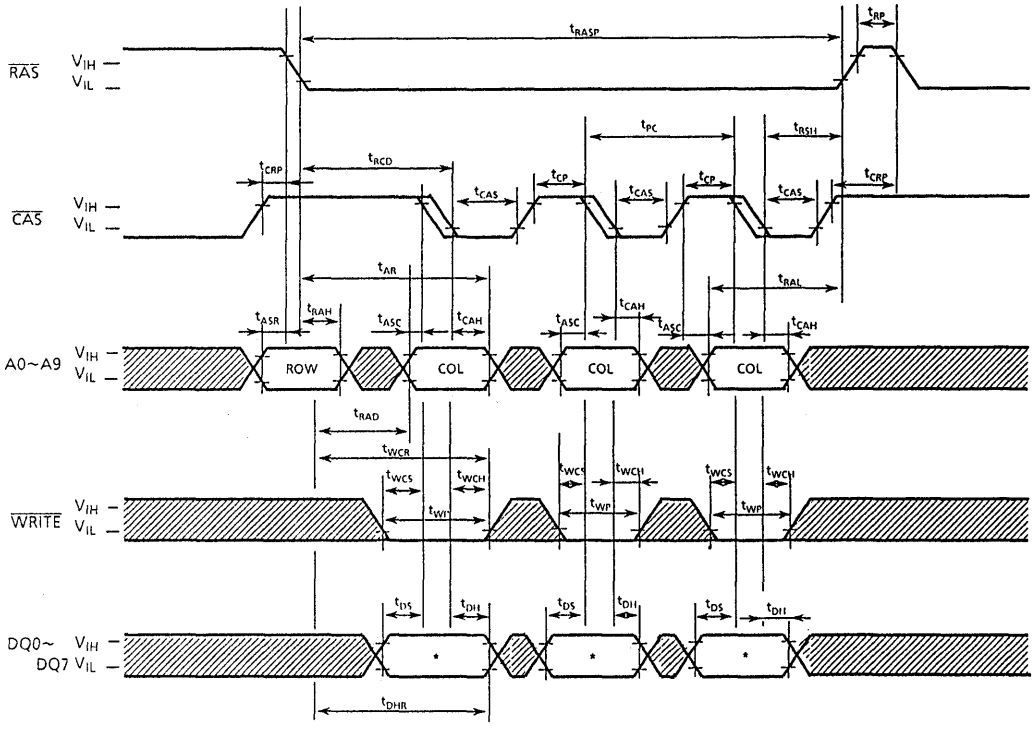


: "H" or "L"

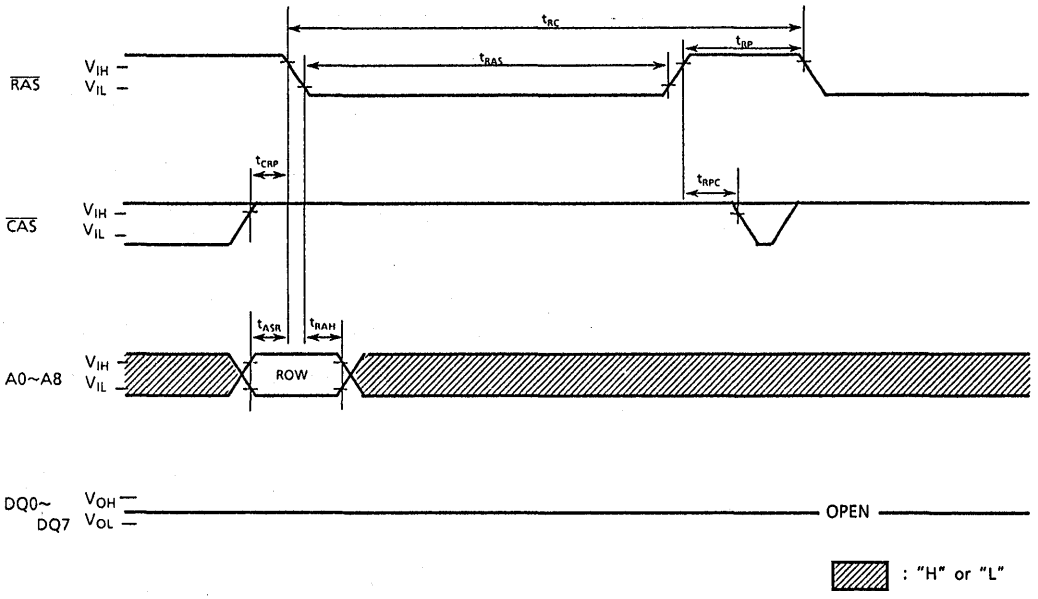
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

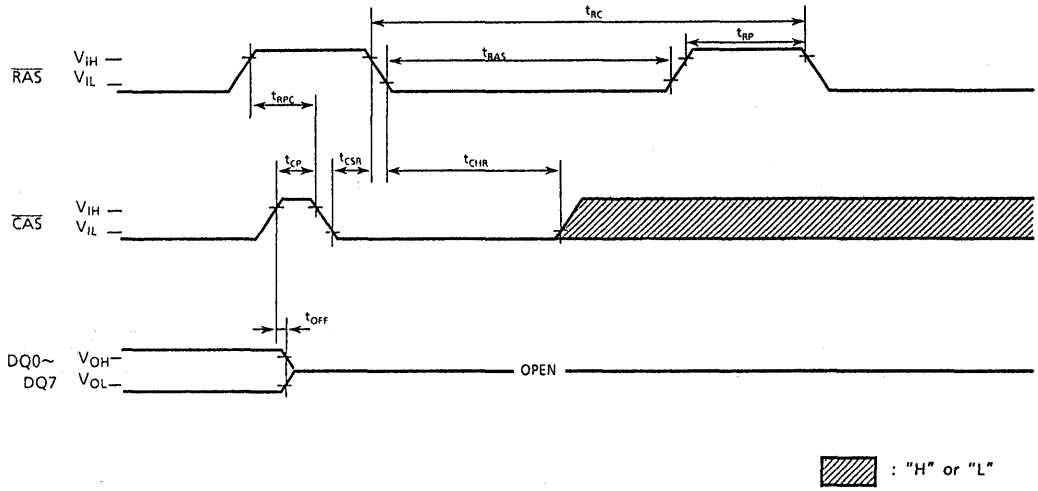


$\overline{RAS}$ ONLY REFRESH CYCLE



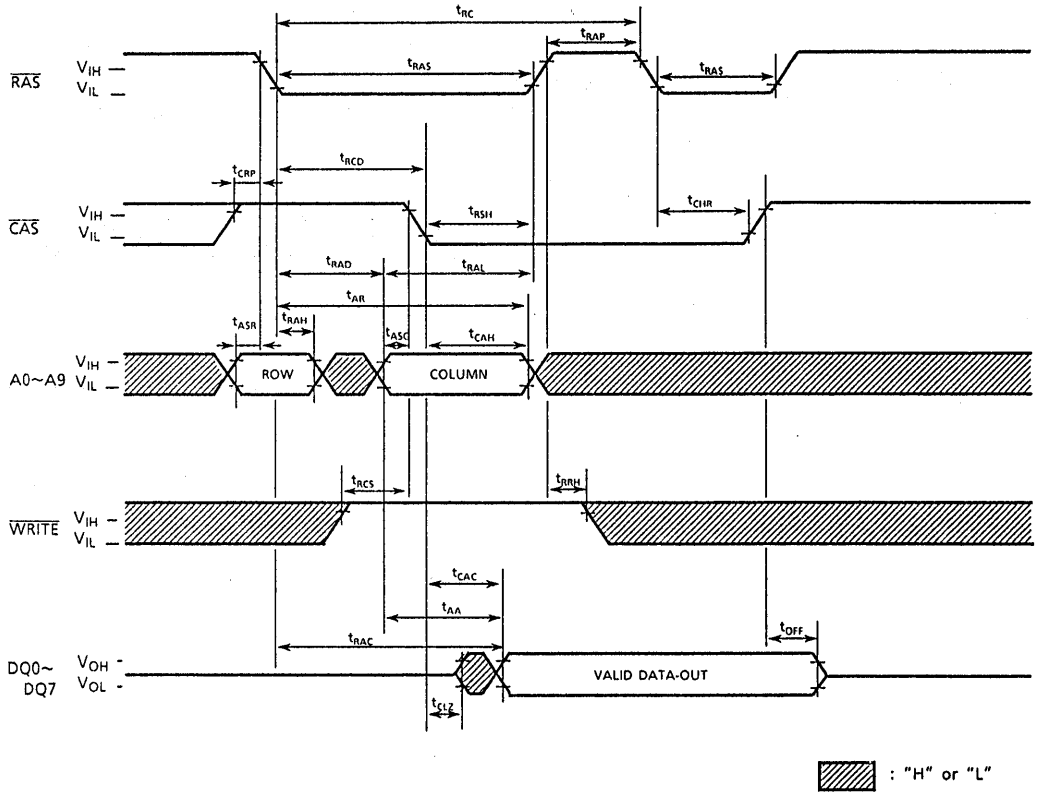
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

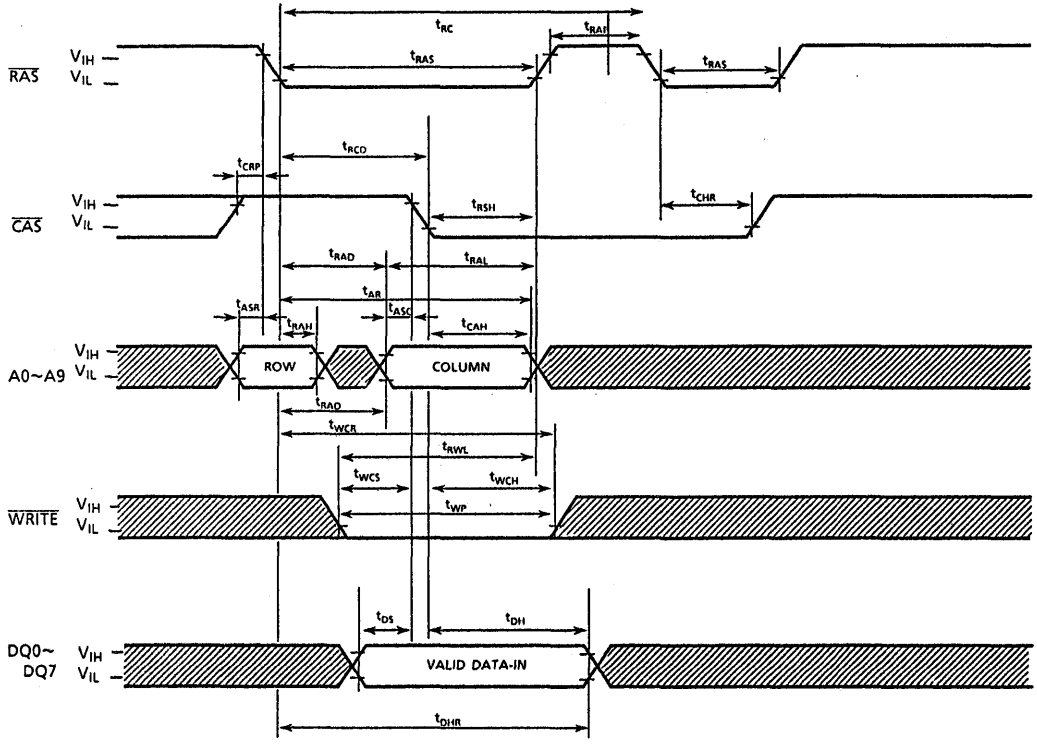


Note: $\overline{WRITE}$ = "H" or "L", A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

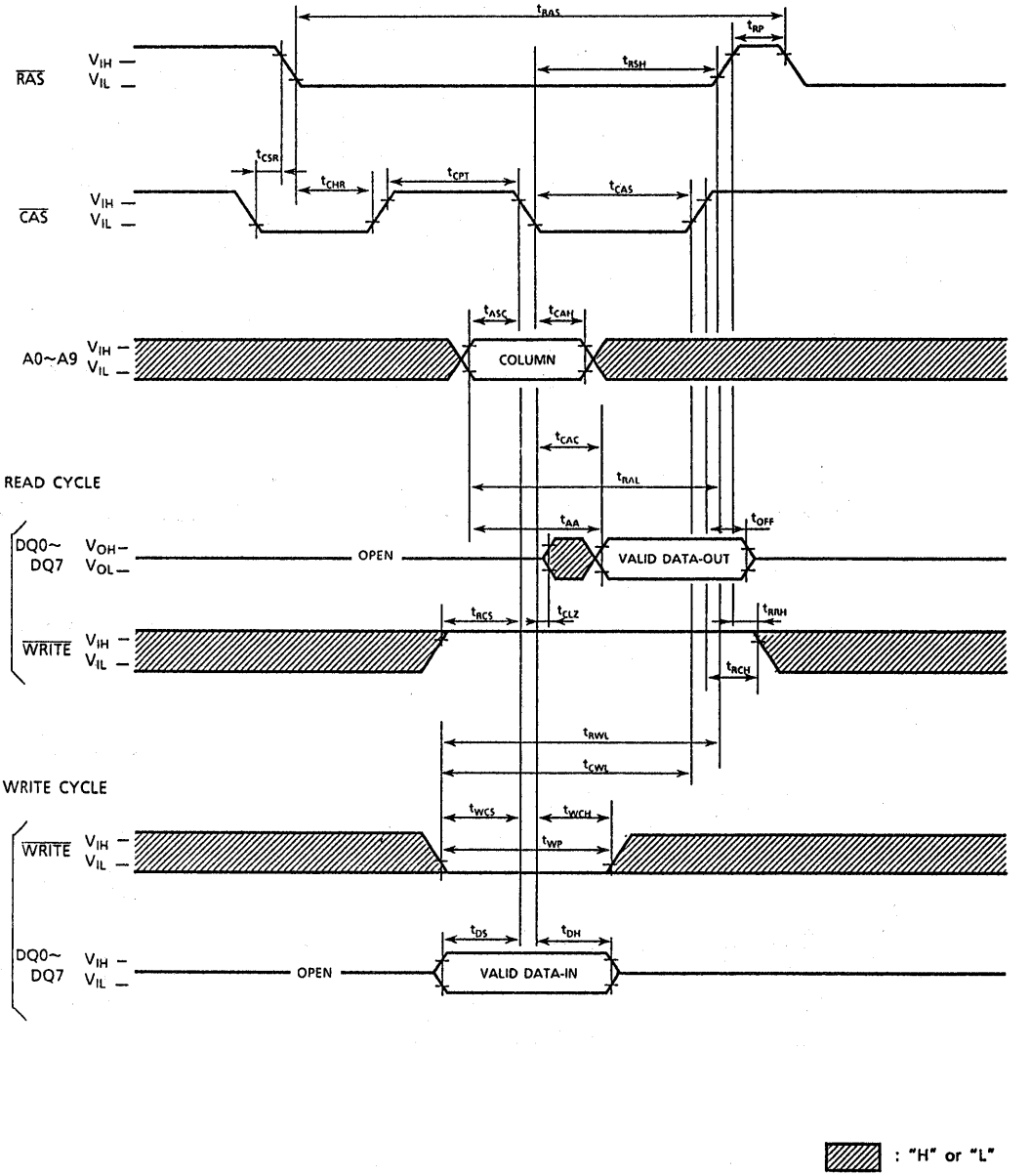


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

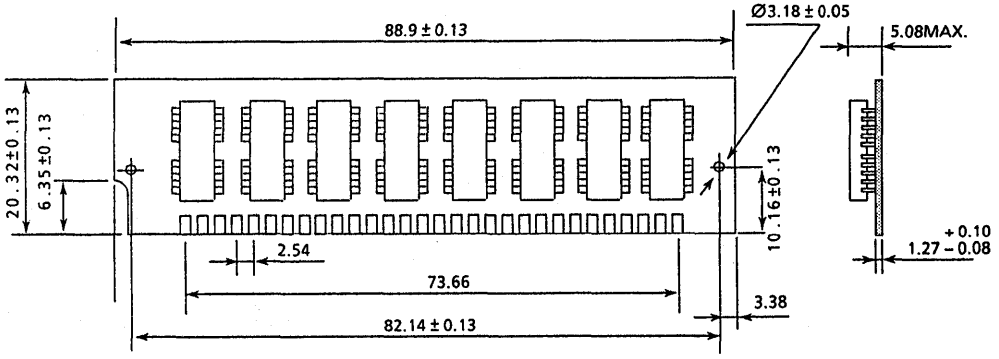
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CYCLE



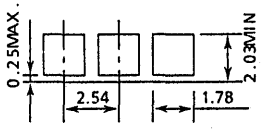
OUTLINE DRAWINGS

Unit: mm

• THM81000AS

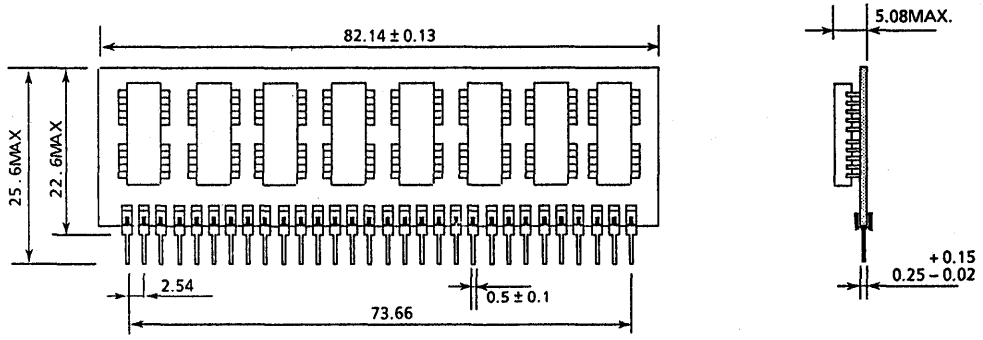


DETAIL OF CONTACTS



Contacts : Tin-Lead

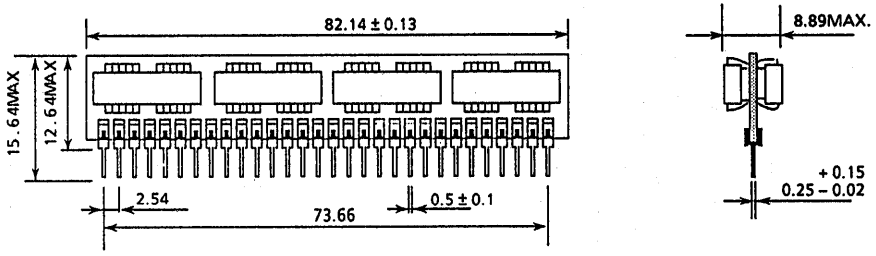
• THM81000AL



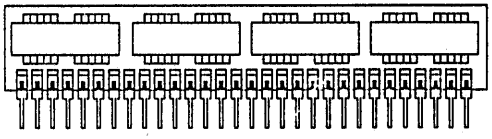
Unit : mm

• THM81020AL

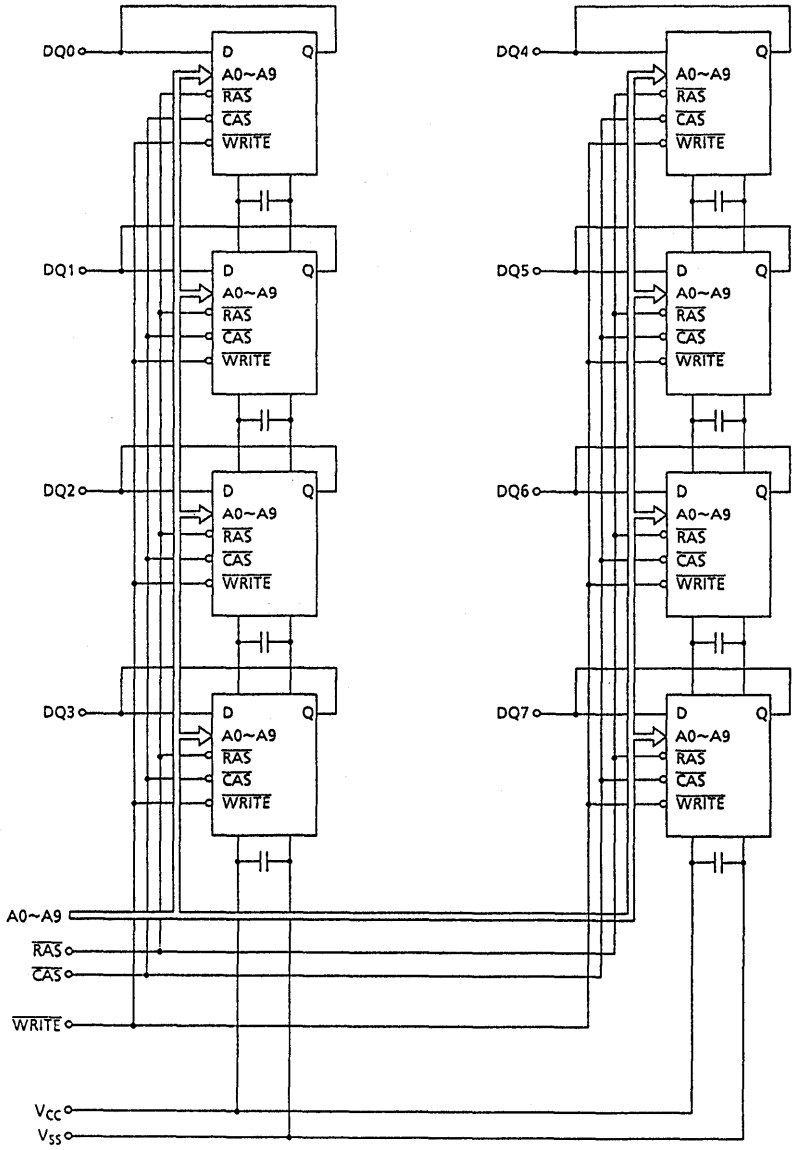
FRONT SIDE



BACK SIDE



BLOCK DIAGRAM



NOTES

1,048,576 WORDS×8 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM81000BS/BSG/BL is a 1,048,576 words by 8 bits dynamic RAM module which assembled 8 pcs of TC511000BJ on the printed circuit board. The THM81000BS / BSG / BL is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

FEATURES

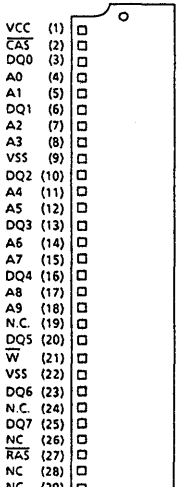
- 1,048,576 words by 8 bits organization
- Fast access time and cycle time

		THM81000BS-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

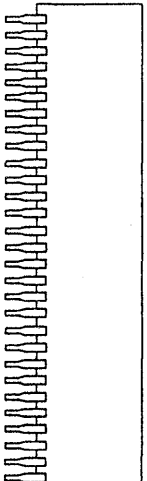
- Single power supply of 5V±10%
- Low power
  3,960mW MAX. Operating
  44mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 8ms
- Tin-Lead Contact: THM81000BS-60
- Gold Contact: THM81000BSG-60

PIN CONNECTION (TOP VIEW)

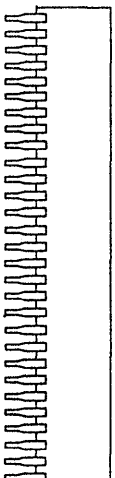
THM81000BS/BSG



THM81000BL



THM81020BL



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Input/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	–	720	mA	3, 4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	–	720	mA	3
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	–	480	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	–	720	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)	–80	80	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	–20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = –5mA)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	8, 13
t_{AA}	Access Time from Column Address	–	30	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	10
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	11
t_{DH}	Data Hold Time	15	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	

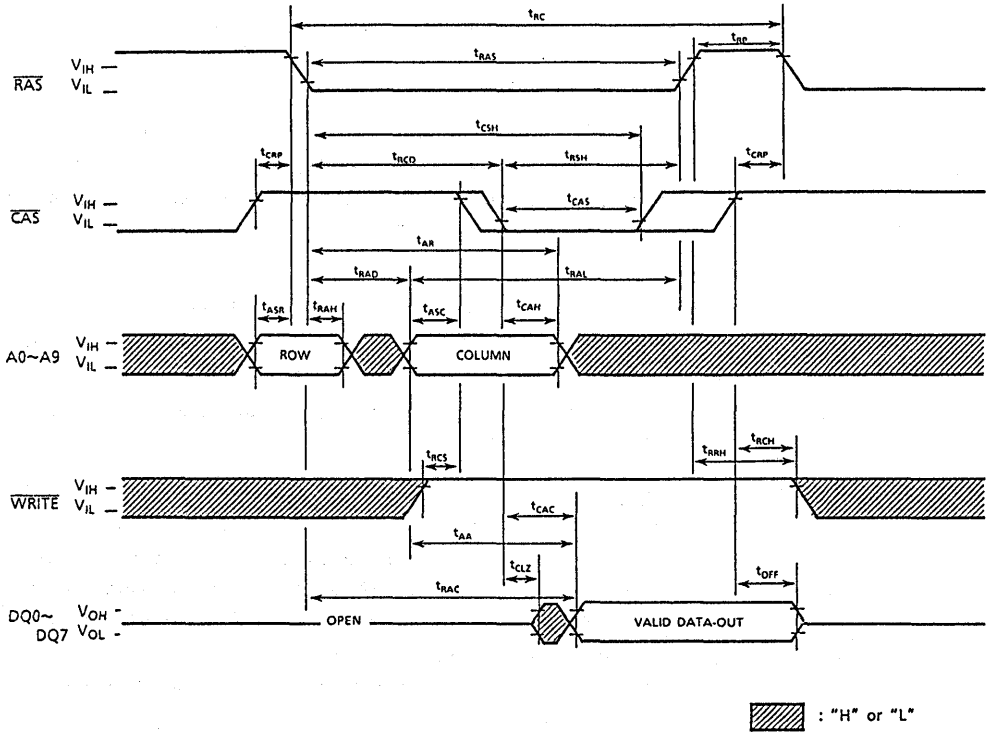
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	–	15	pF

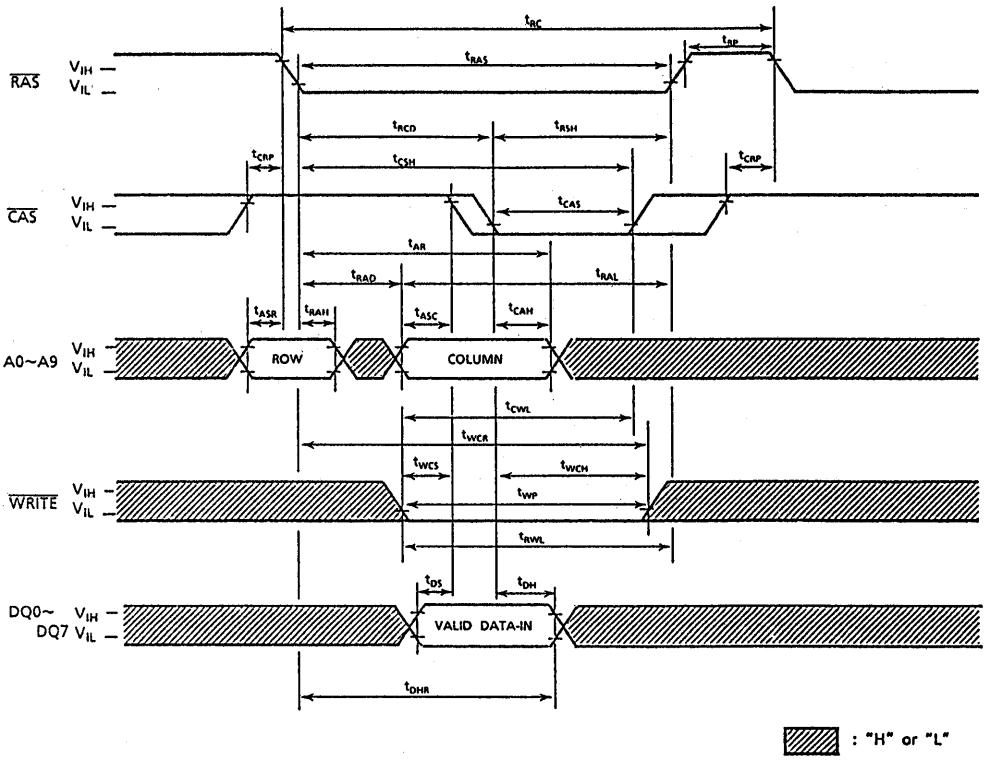
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

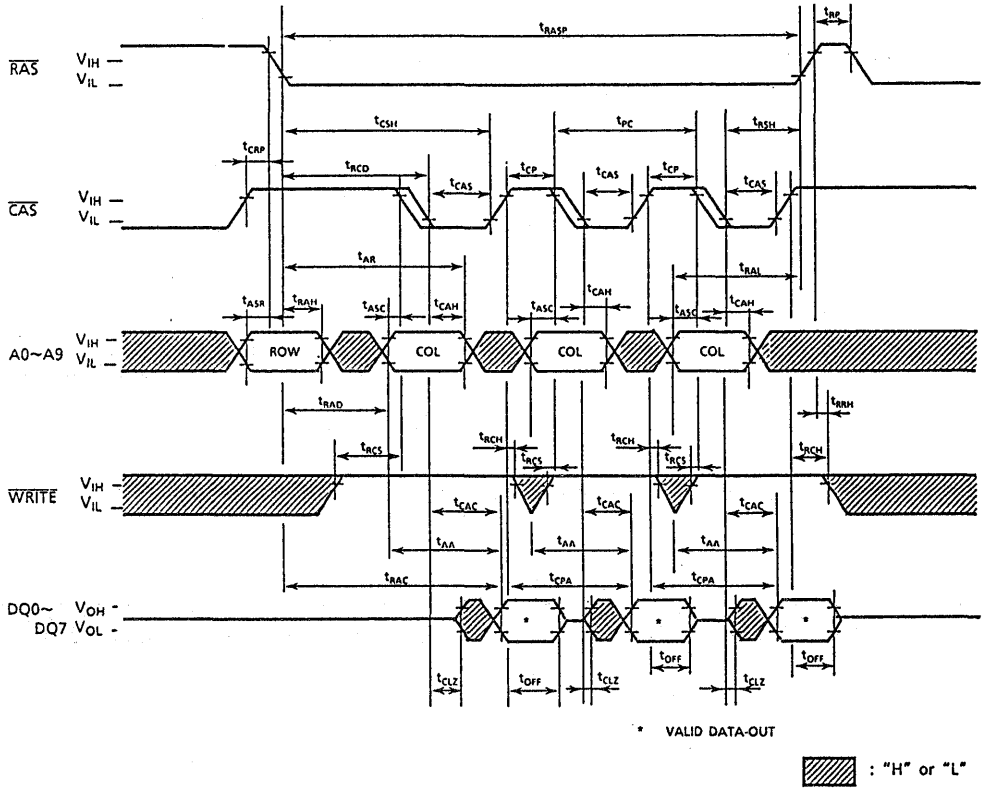
READ CYCLE


tRC
tRP
tRAS
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~
DQ7
VOH
VOL
OPEN
VALID DATA-OUT
: "H" or "L"

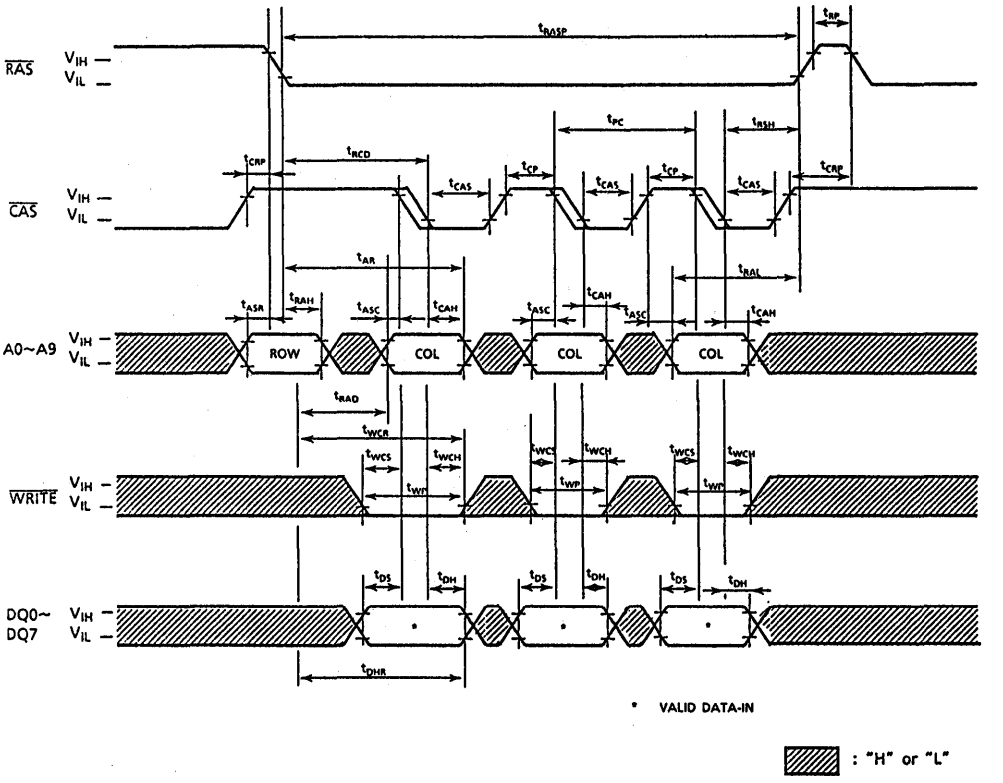
EARLY WRITE CYCLE



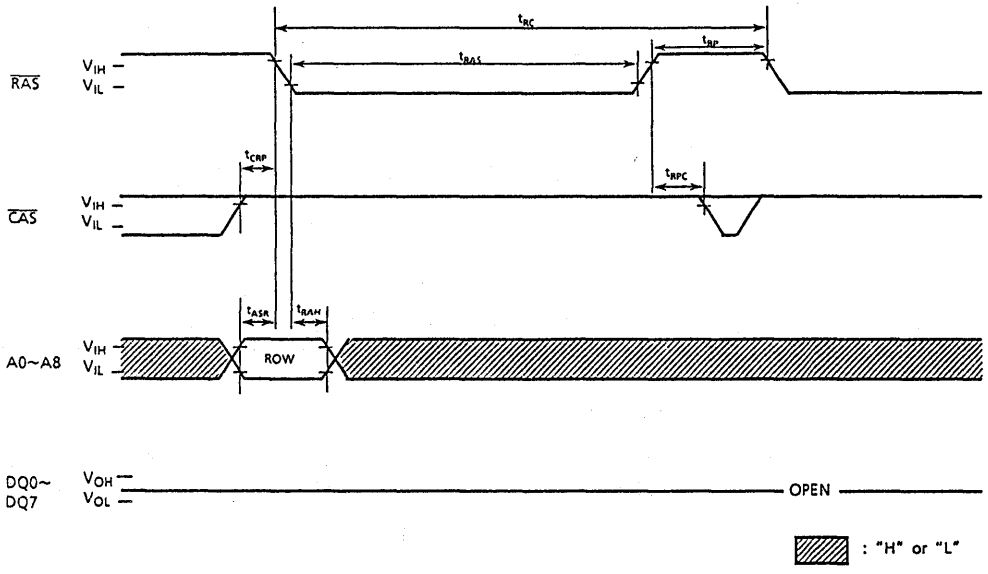
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

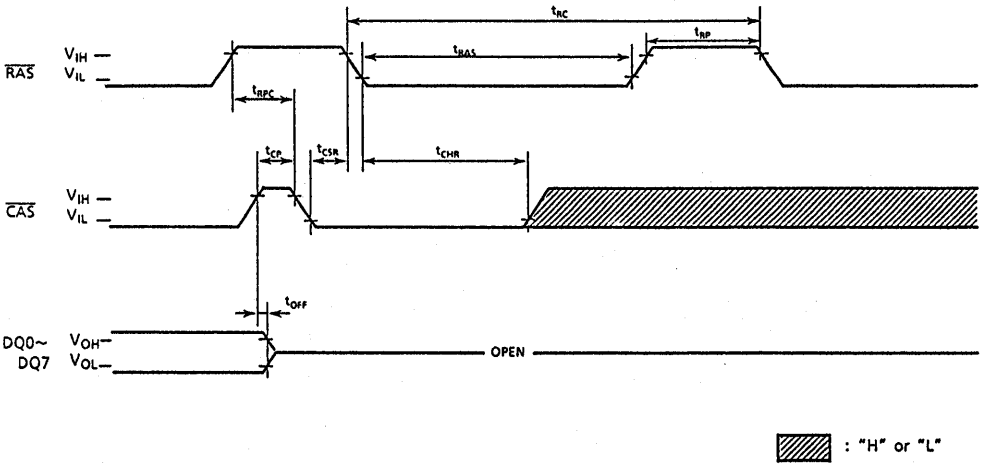


$\overline{RAS}$ ONLY REFRESH CYCLE



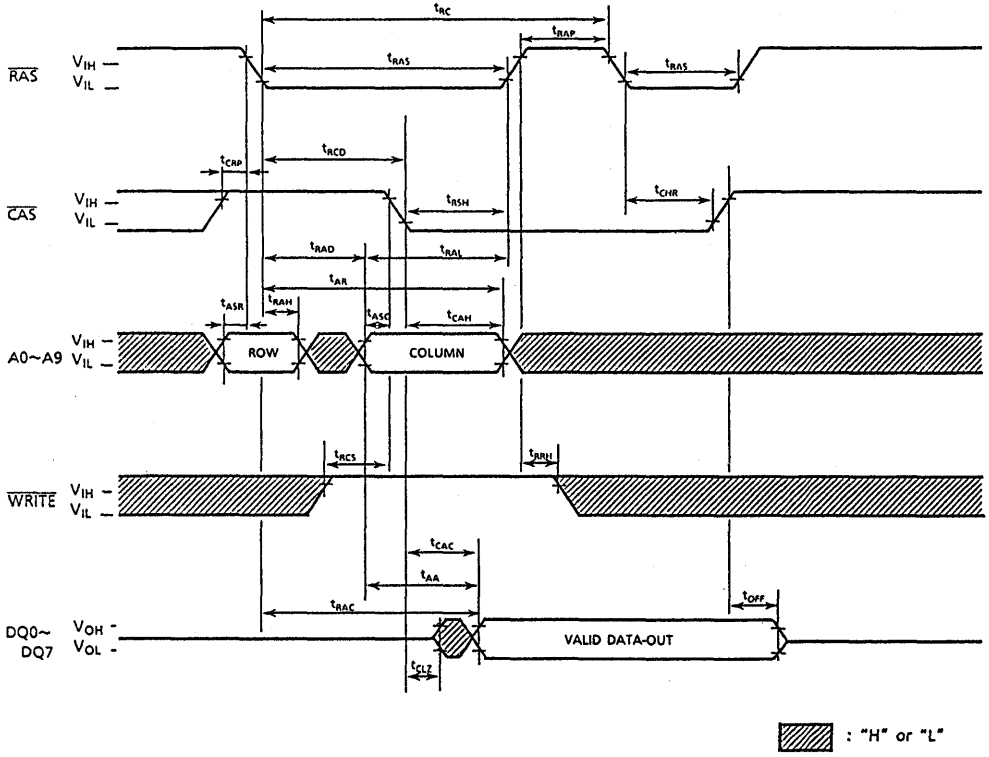
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

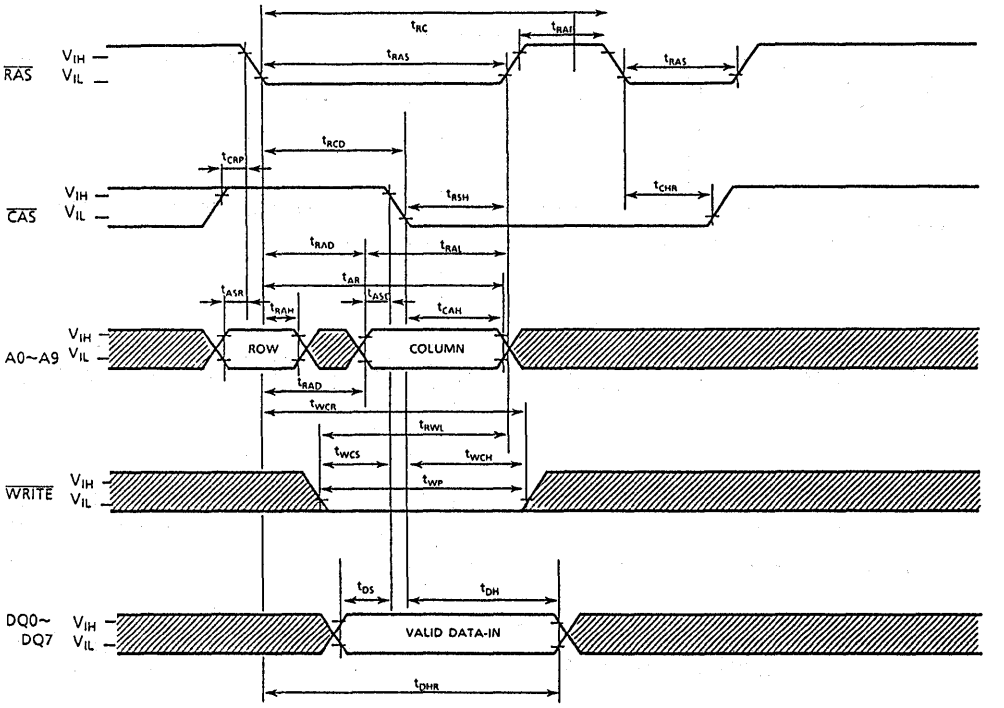


Note: $\overline{WRITE}$ = "H" or "L", A0~A9 = "H" or "L"

HIDDEN REFRESH CYCLE (READ)

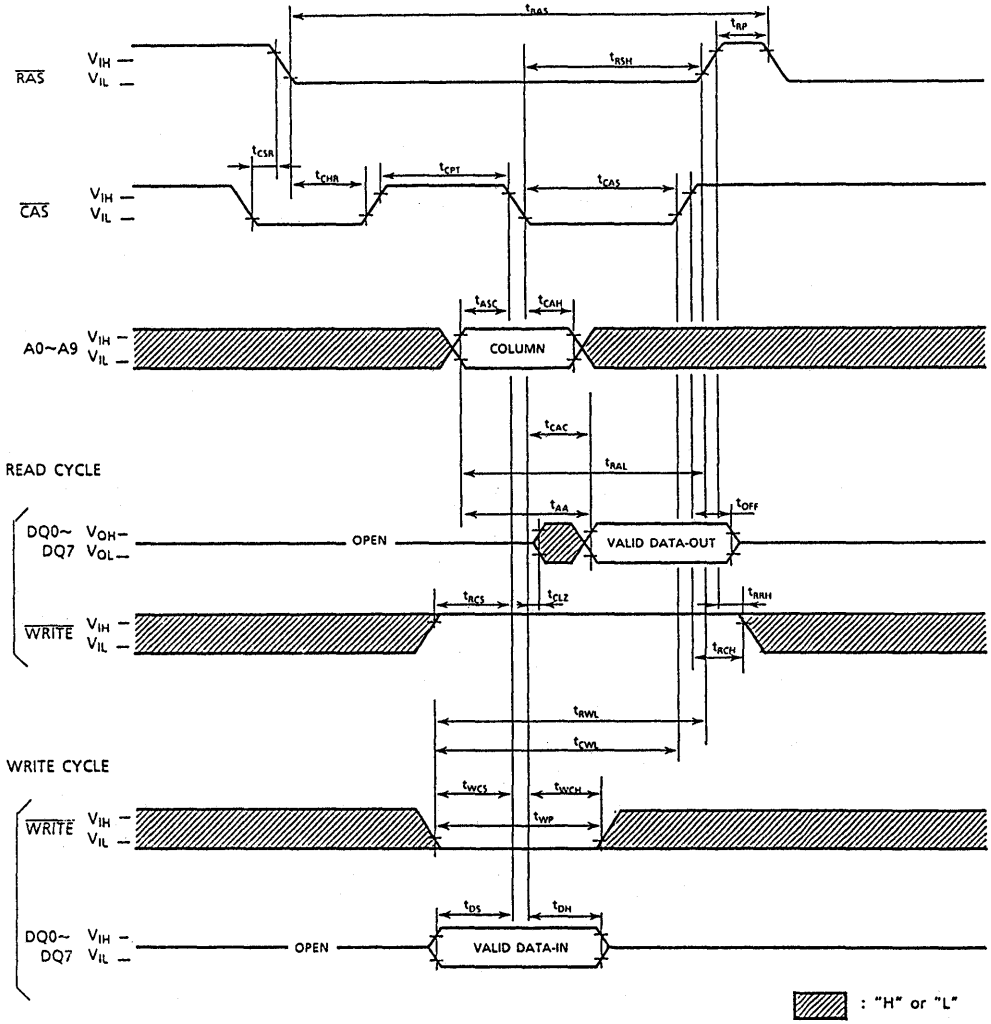


HIDDEN REFRESH CYCLE (WRITE)



: "H" or "L"

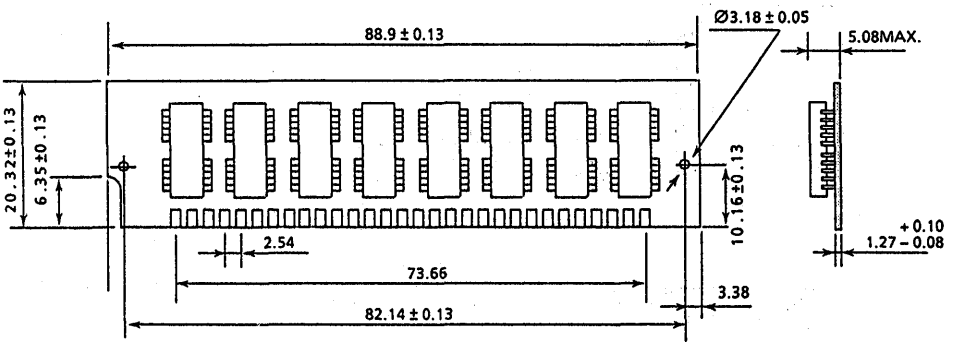
CAS BEFORE RAS REFRESH COUNTER CYCLE



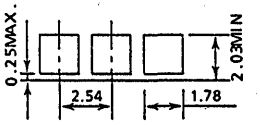
OUTLINE DRAWINGS

Unit: mm

• THM81000BS / BSG

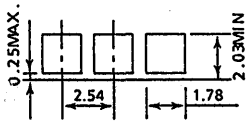


• THM81000BS
DETAIL OF CONTACTS



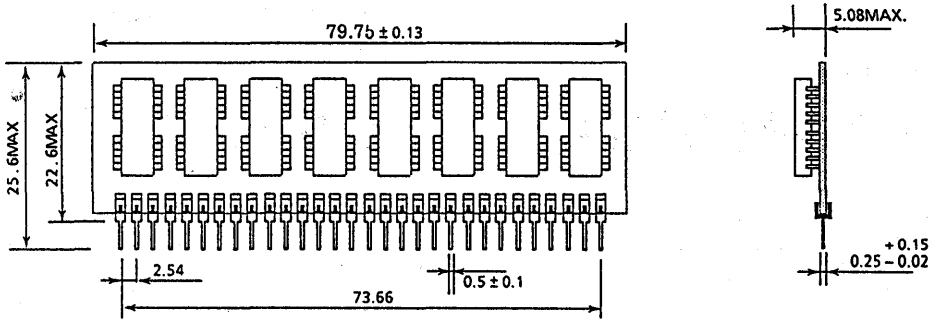
Contacts : Tin-Lead

• THM81000BSG
DETAIL OF CONTACTS



Contacts : Gold

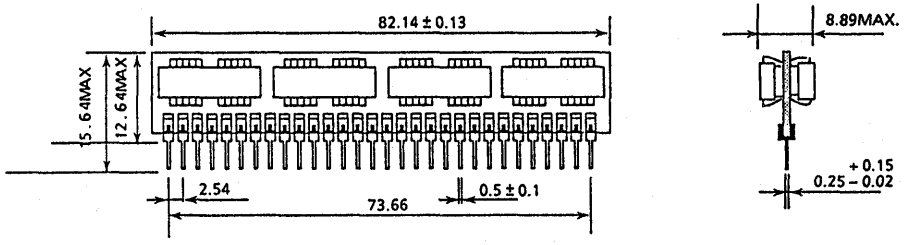
• THM81000BL



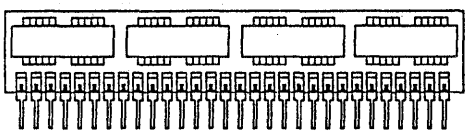
Unit : mm

• THM81020BL

FRONT SIDE



BACK SIDE



NOTES

1,048,576 WORDS×8 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM81070AS/AL and THM81070AS/AL are a 1,048,576 words by 8 bits dynamic RAM module which assembled 2 pcs of TC514400ASJ and 1 pcs of TC511000AJ/BJ on the printed circuit board. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

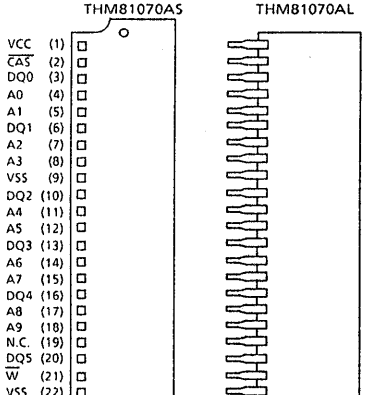
FEATURES

- 1,048,576 words by 8 bits organization
- Fast access time and cycle time

	-60	-70	-80	-10
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC} Cycle Time	110ns	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns	60ns

- Low Power
  1,815mW MAX. Operating (THMxxxxxx−60)
  1,540mW MAX. Operating (THMxxxxxx−70)
  1,320mW MAX. Operating (THMxxxxxx−80)
  1,155mW MAX. Operating (THMxxxxxx−10)
  16.5mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/16ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package THM81070AS-xx : Tin-Lead Contact
  THM81070AL-xx : 30Pin SIP

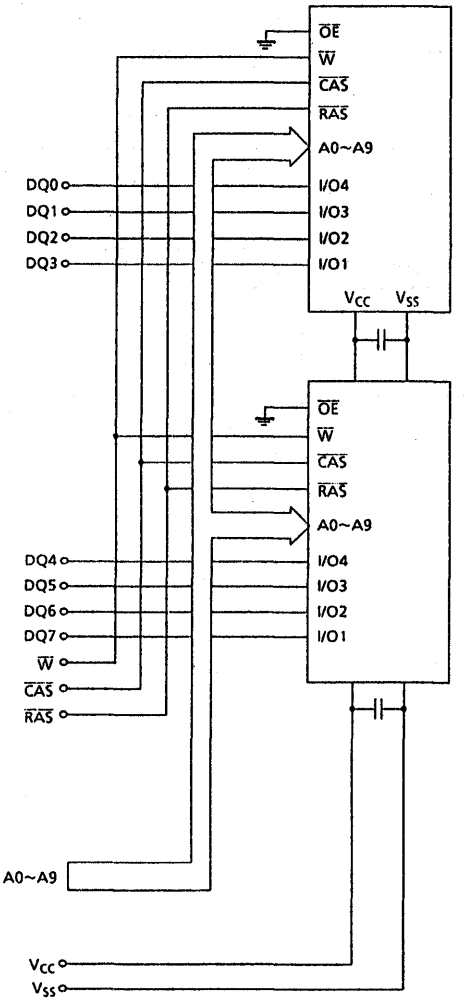
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	240	mA	3, 4 5
		THMxxxxxx-70	–	200		
		THMxxxxxx-80	–	170		
		THMxxxxxx-10	–	150		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	240	mA	3,5
		THMxxxxxx-70	–	200		
		THMxxxxxx-80	–	170		
		THMxxxxxx-10	–	150		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx-60	–	140	mA	3, 4 5
		THMxxxxxx-70	–	140		
		THMxxxxxx-80	–	120		
		THMxxxxxx-10	–	110		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	2	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	240	mA	3,5
		THMxxxxxx-70	–	200		
		THMxxxxxx-80	–	170		
		THMxxxxxx-10	–	150		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 20	20	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,13
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	10	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

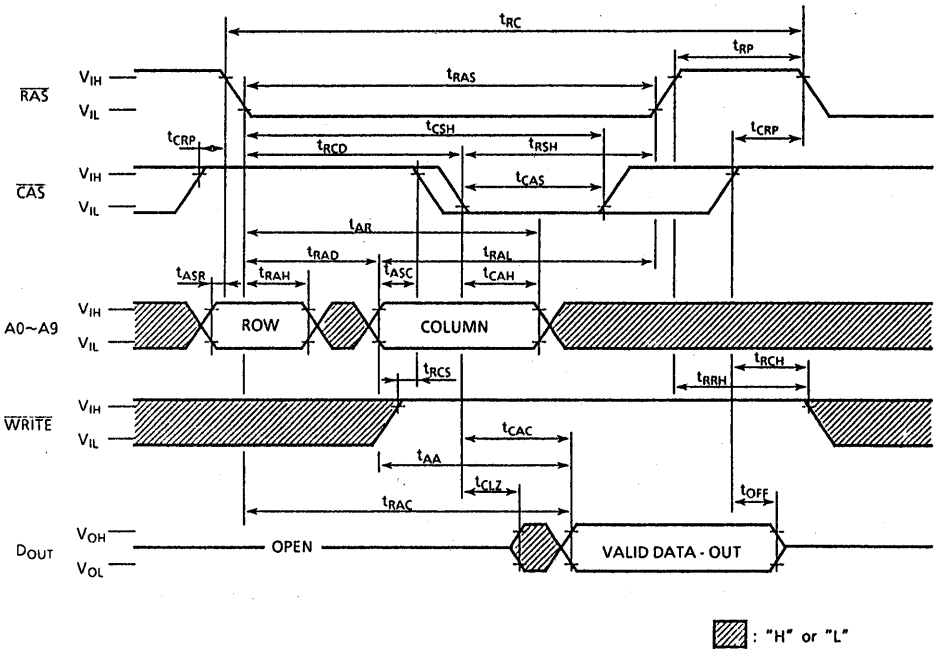
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	30	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF

NOTES:

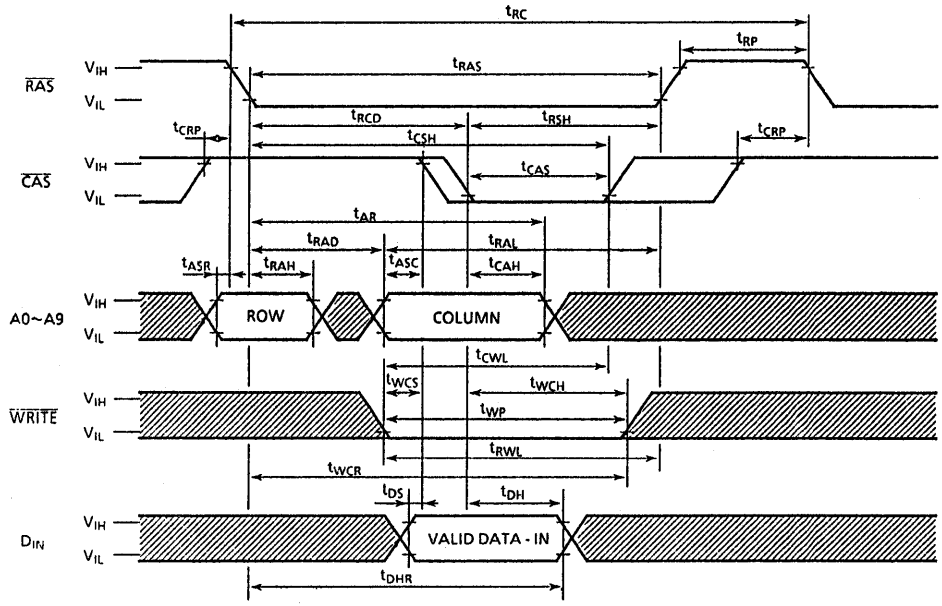
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T = 5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
13. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

READ CYCLE

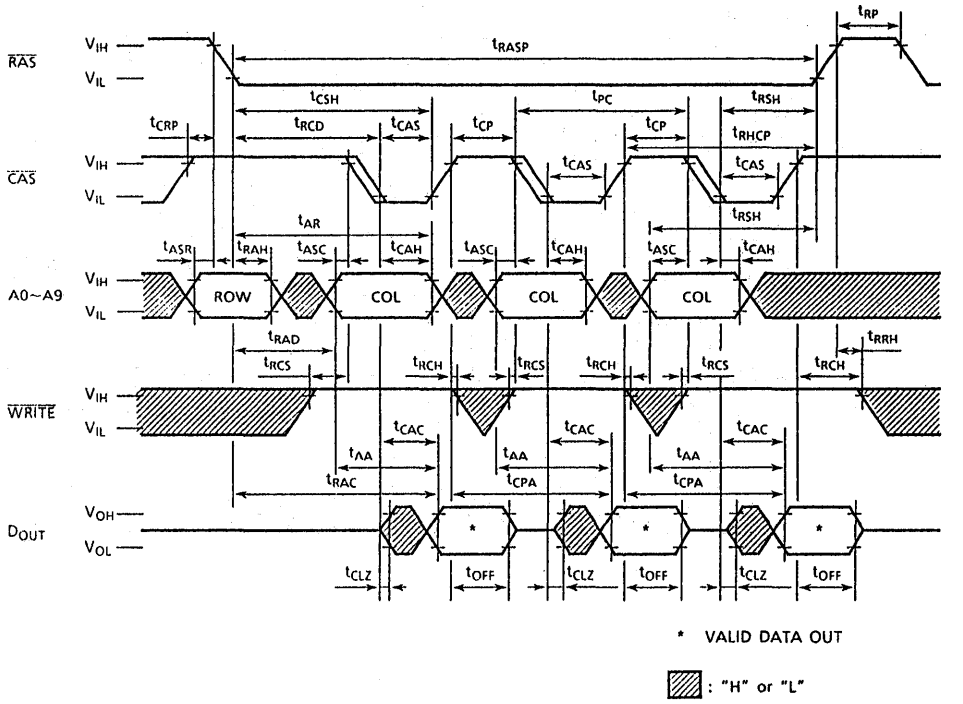


WRITE CYCLE (EARLY WRITE)

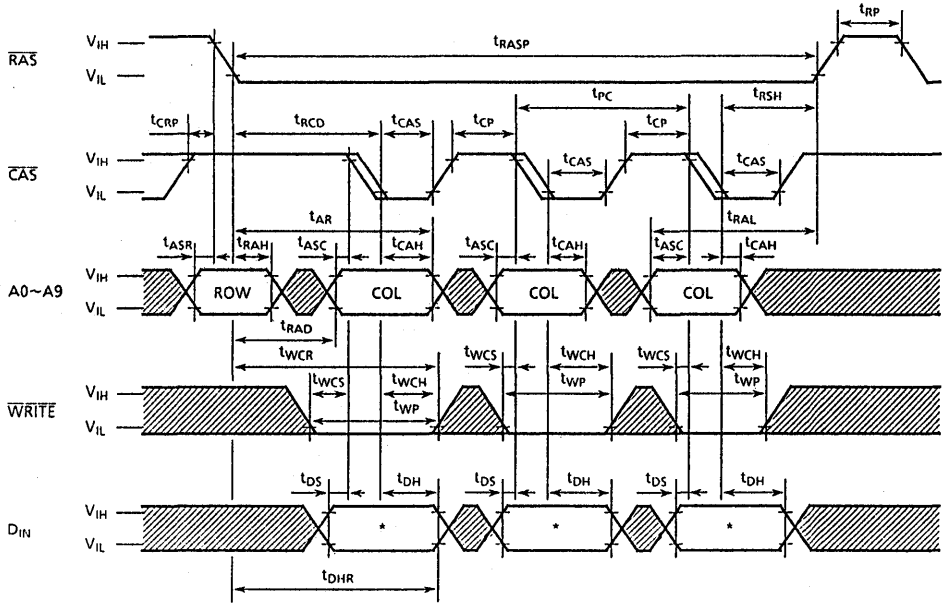


▨ : "H" or "L"

FAST PAGE MODE READ CYCLE



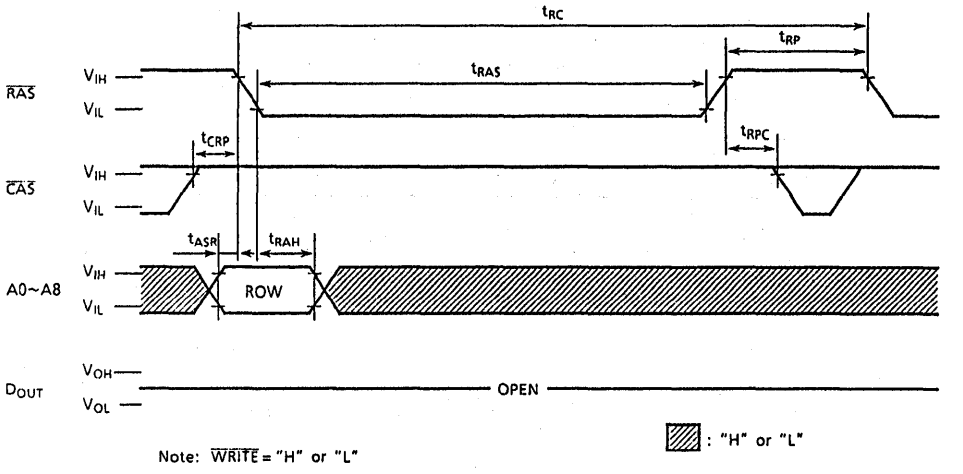
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

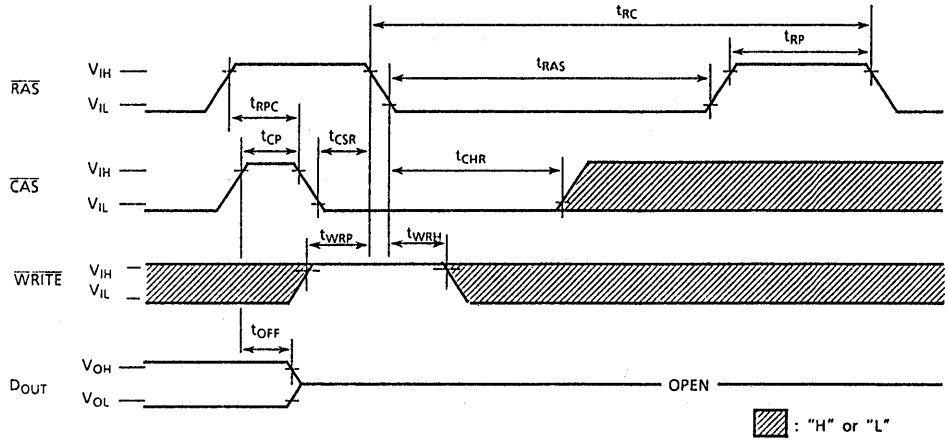
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



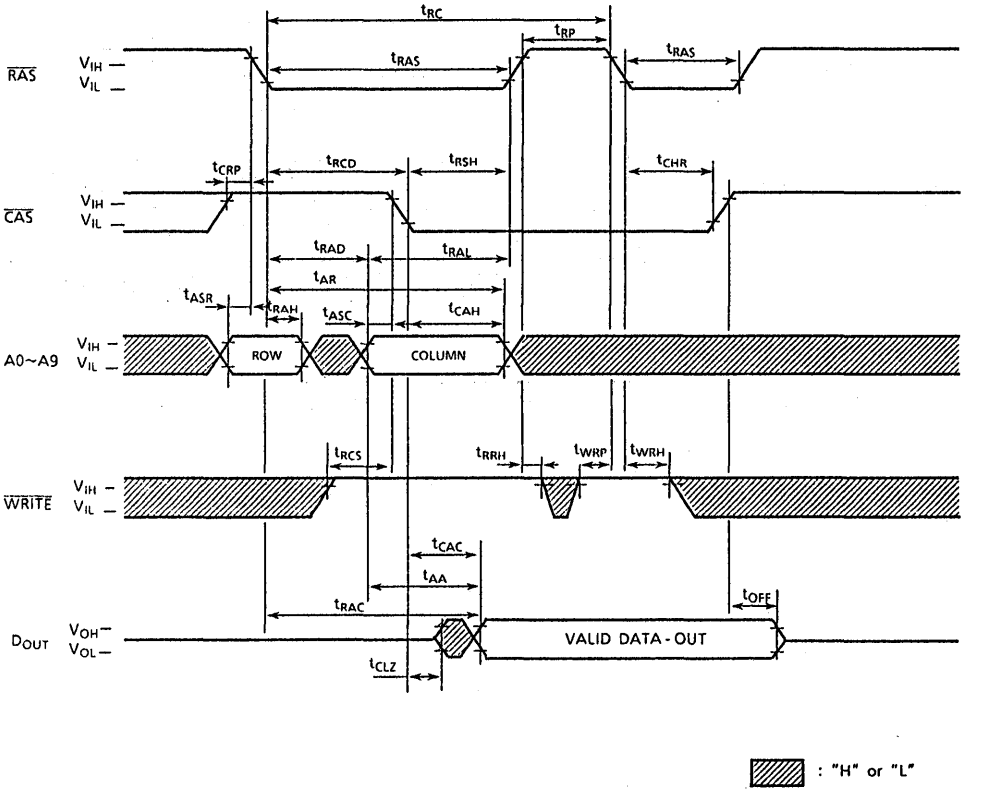
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

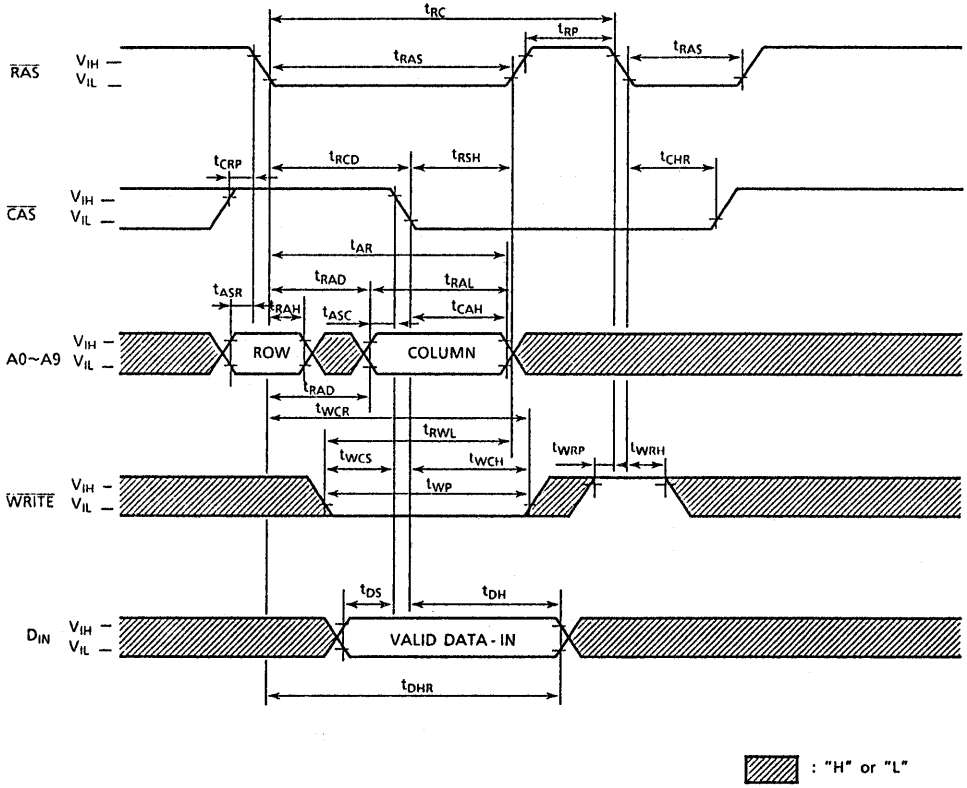


Note: A0~A9 = "H" or "L"

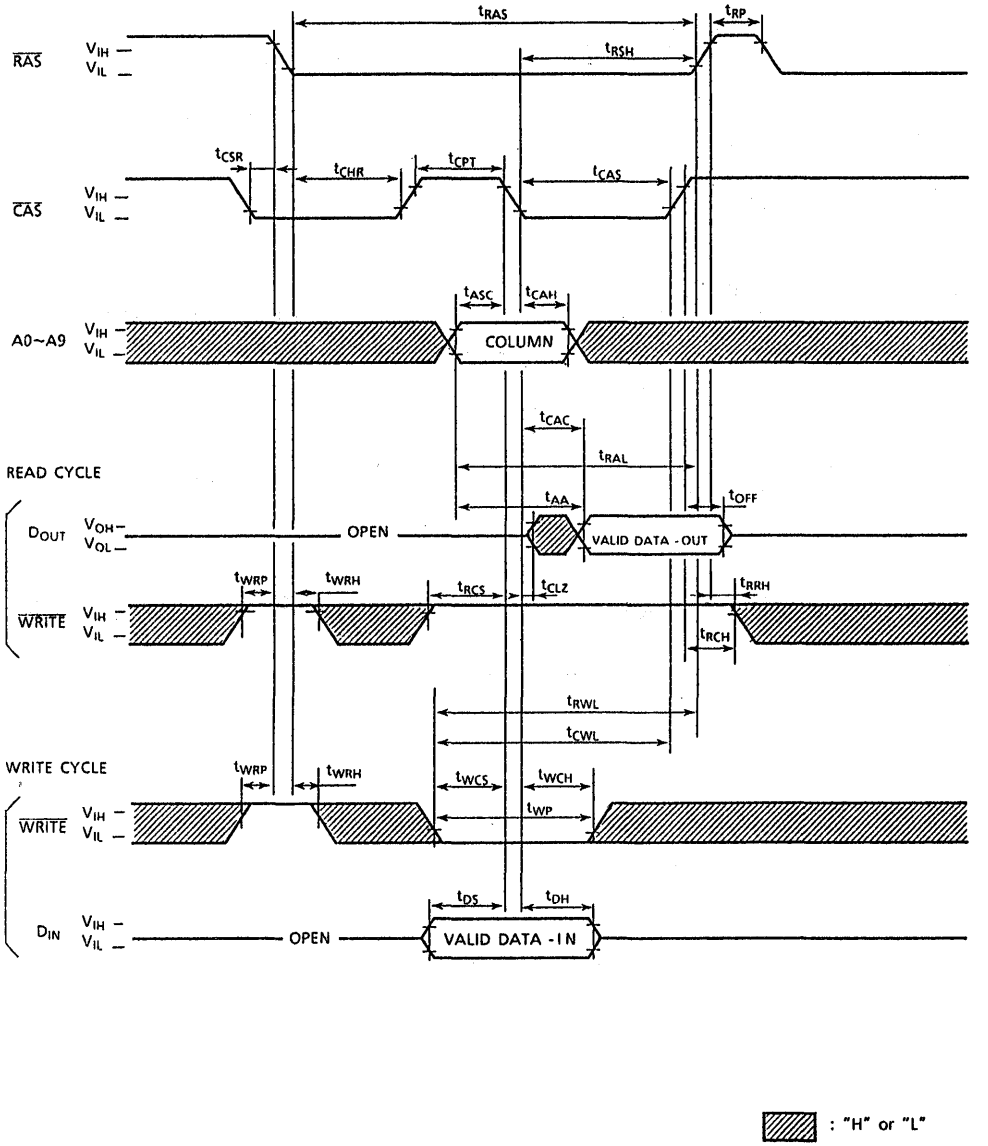
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



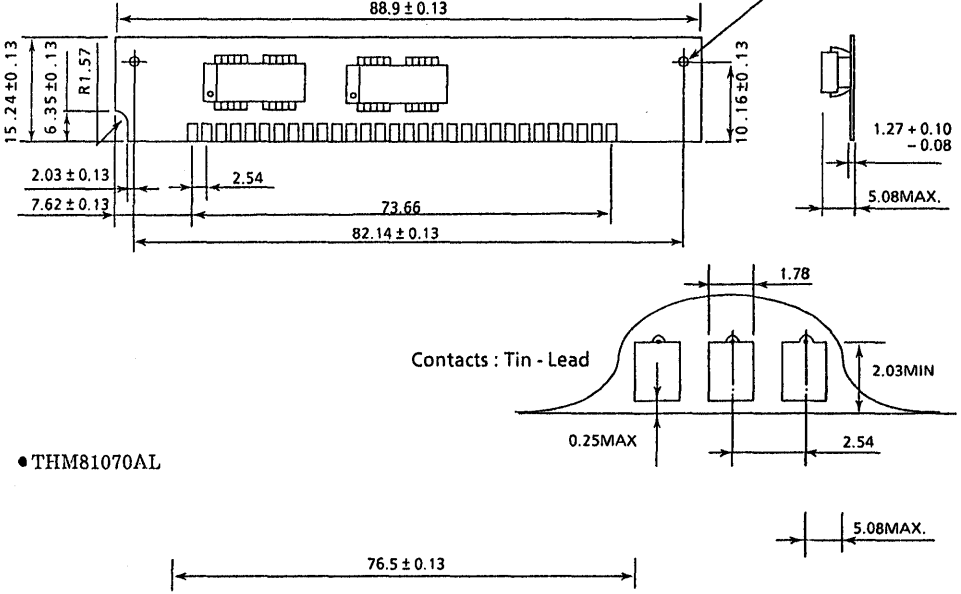
: "H" or "L"

OUTLINE DRAWINGS

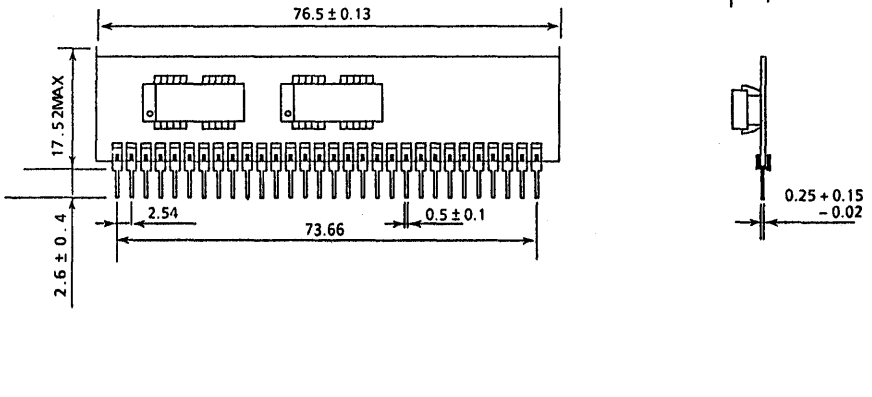
THM81070AS/AL

Unit in mm

• THM81070AS



• THM81070AL



NOTES

262,144 WORDS × 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM322500BS/BSG/AS/ASG is a 524,288 words by 32 bits dynamic RAM module which assembled 8 pcs of TC514256AJ/BJ on the printed circuit board. These modules can be as well used as 524,288 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

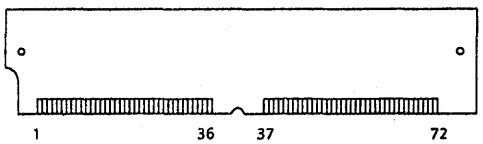
FEATURES

- 262,144 words by 32 bits organization
- Fast access time and cycle time

	-60	-70	-80	-10
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC} Cycle Time	115ns	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	40ns	40ns	45ns	55ns

- Low Power
  3,960mW MAX. Operating (THMxxxxxx−60)
  3,520mW MAX. Operating (THMxxxxxx−70)
  3,080mW MAX. Operating (THMxxxxxx−80)
  2,640mW MAX. Operating (THMxxxxxx−10)
  44mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package
  THM322500BS - 60 : Tin - Lead Contact
  THM322500AS - 70,80,10 : Tin - Lead Contact
  THM322500BSG - 60 : Gold Contact
  THM322500ASG - 70,80,10 : Gold Contact

PIN CONNECTION (TOP VIEW)



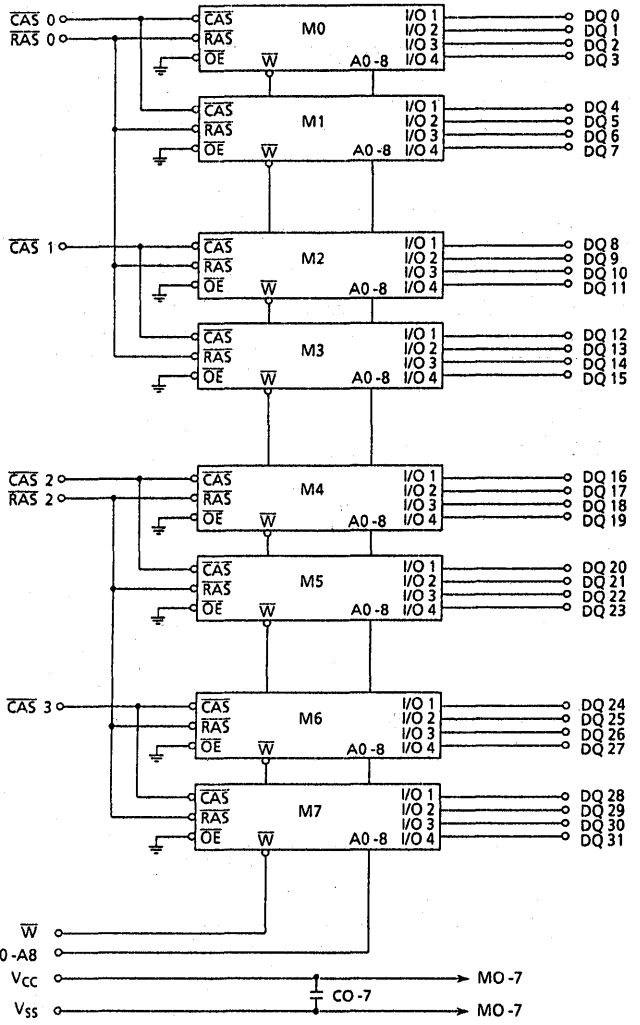
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	NC	45	NC	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

	-60	-70	-80	-10
PD0	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD1	NC	NC	NC	NC
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	4.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	720	mA	3, 4 5
		THMxxxxxx-70	–	640		
		THMxxxxxx-80	–	560		
		THMxxxxxx-10	–	480		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	16	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	720	mA	3,5
		THMxxxxxx-70	–	640		
		THMxxxxxx-80	–	560		
		THMxxxxxx-10	–	480		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxxx-60	–	480	mA	3, 4 5
		THMxxxxxx-70	–	480		
		THMxxxxxx-80	–	400		
		THMxxxxxx-10	–	320		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	8	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	720	mA	3,5
		THMxxxxxx-70	–	640		
		THMxxxxxx-80	–	560		
		THMxxxxxx-10	–	480		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 80	80	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

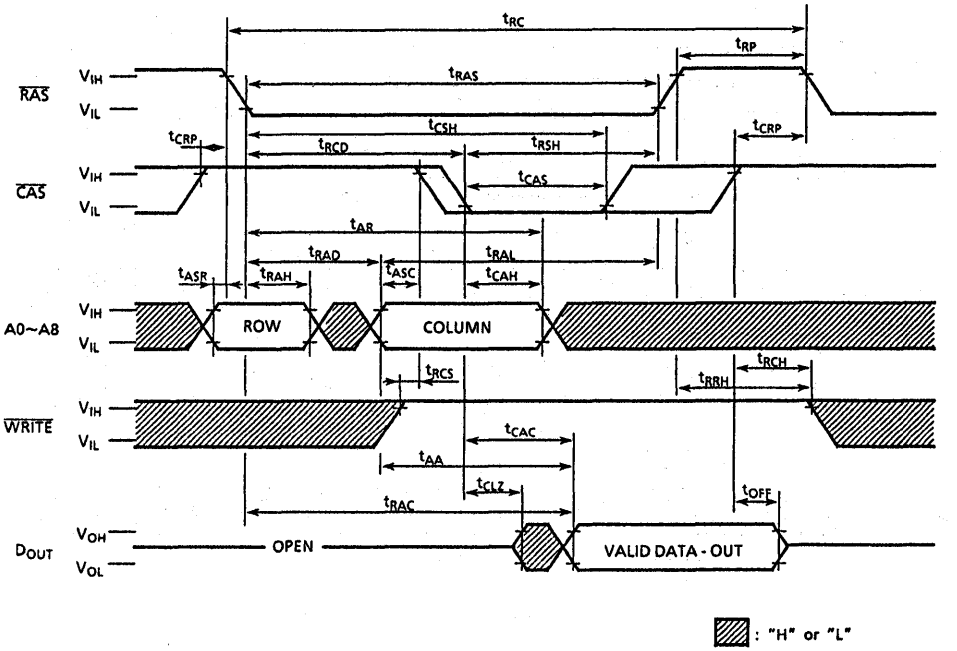
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A8)	–	60	pF
CI2	Input Capacitance ($\overline{W}$)	–	60	pF
CI3	Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	–	35	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	25	pF
CDQ1	I/O Capacitance (DQ0~31)	–	17	pF

NOTES:

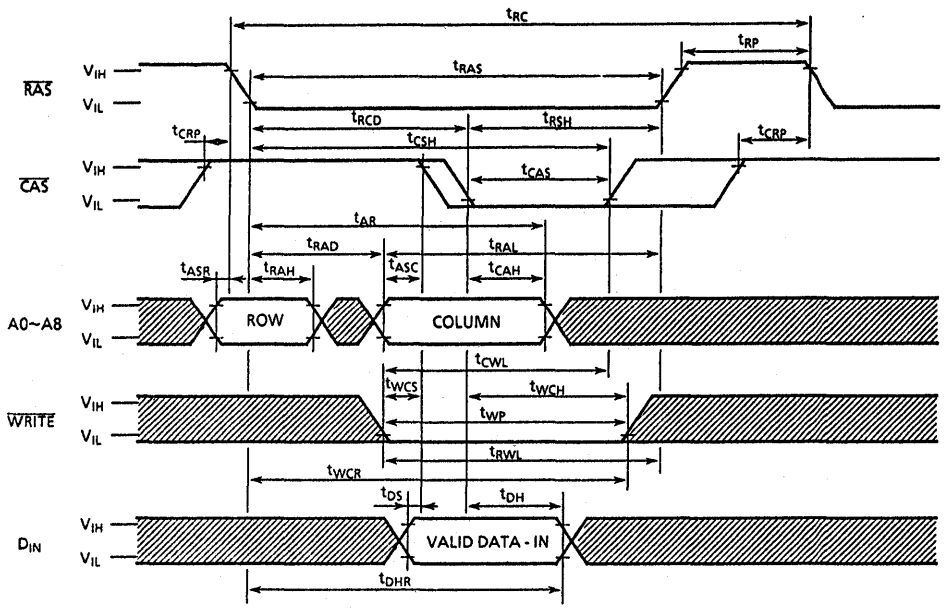
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

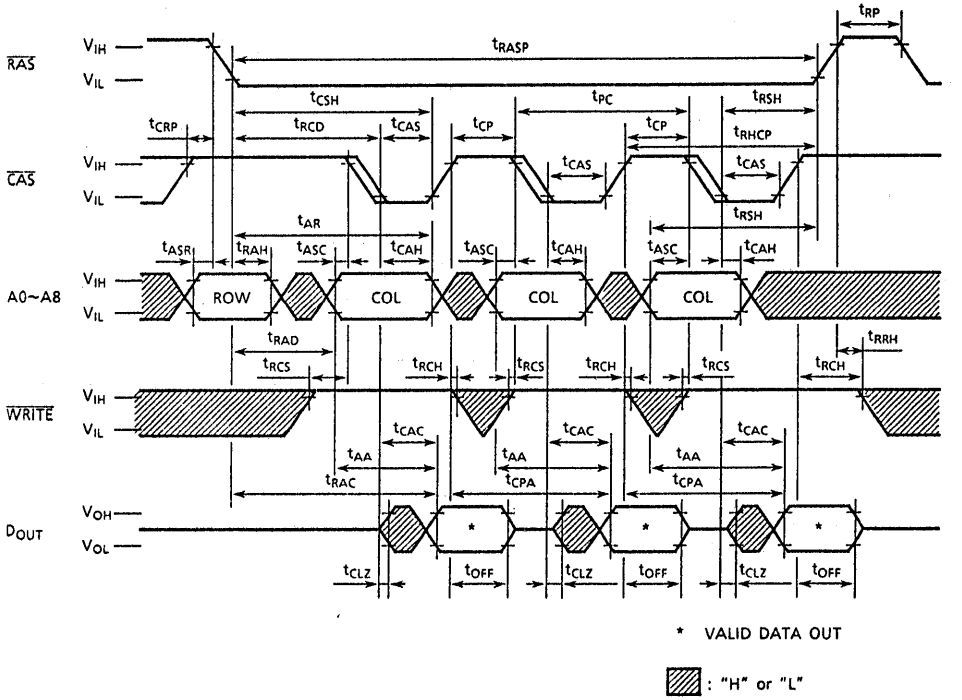
READ CYCLE



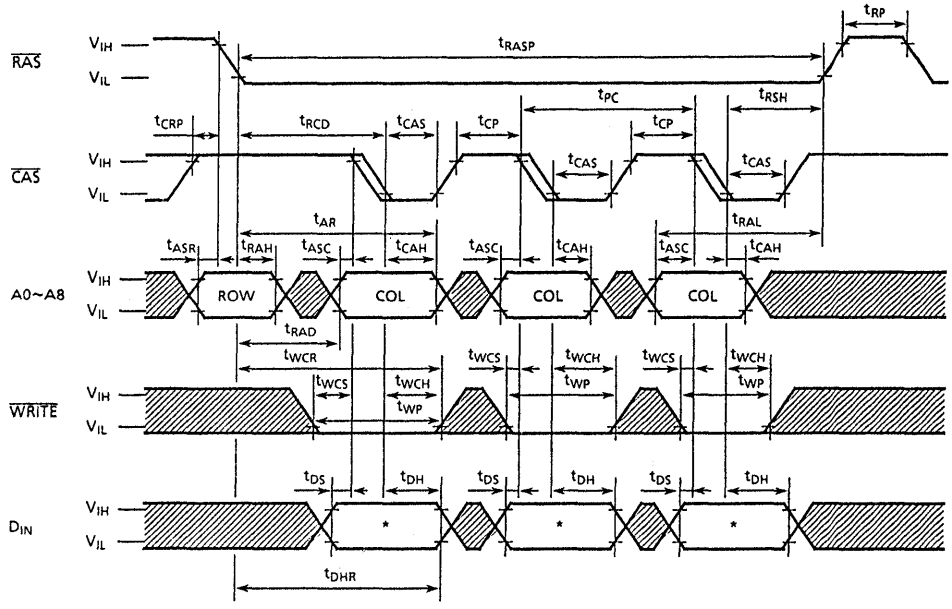
WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ CYCLE



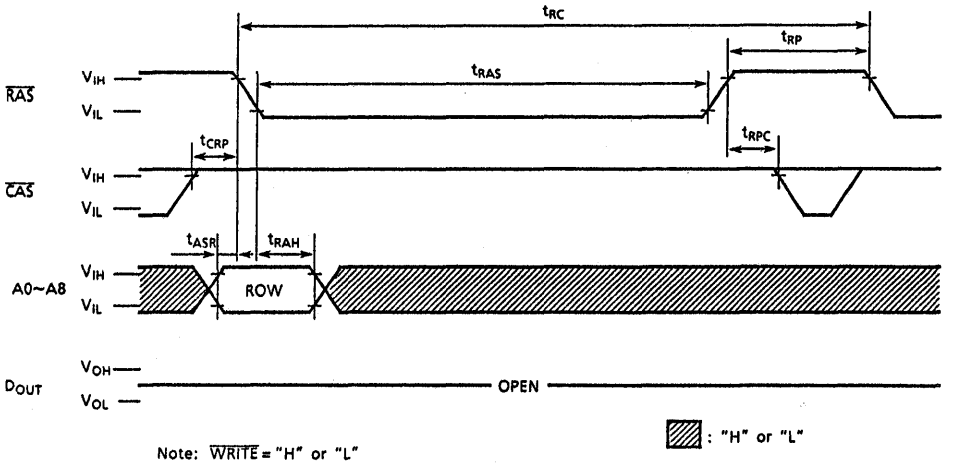
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

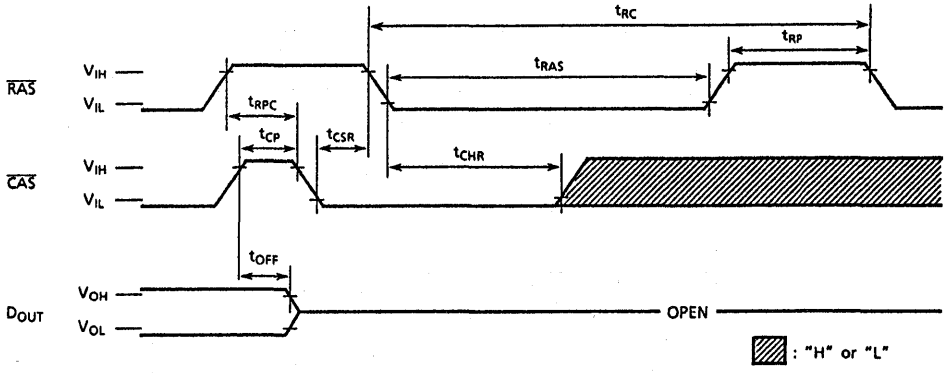
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



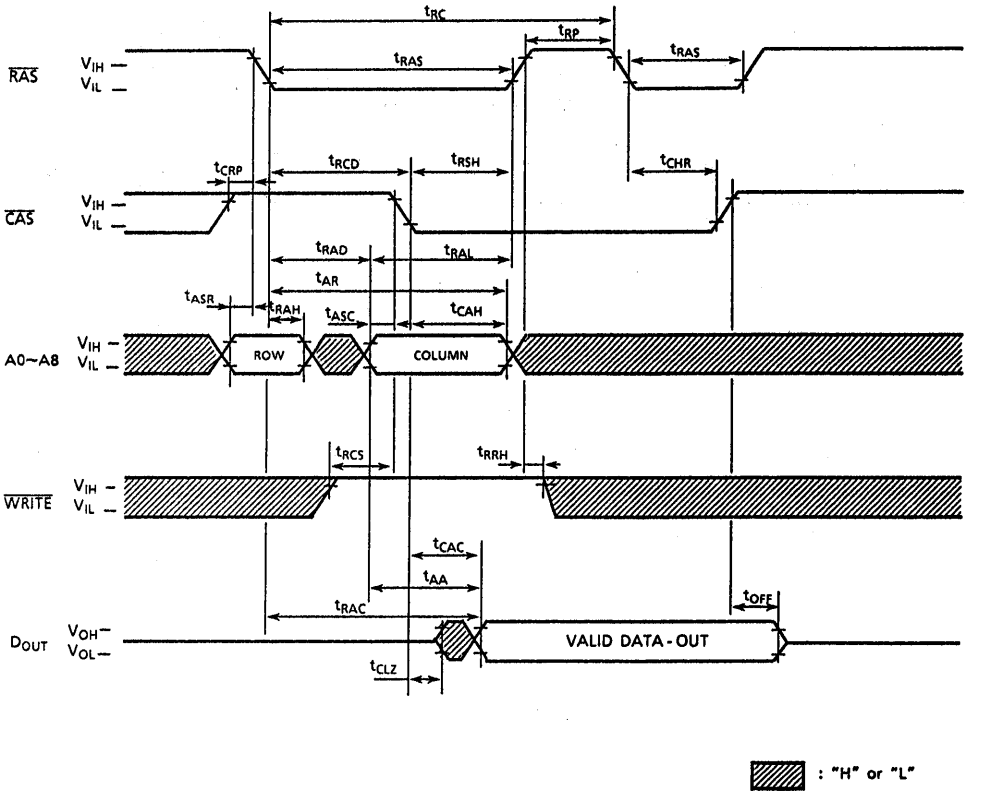
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

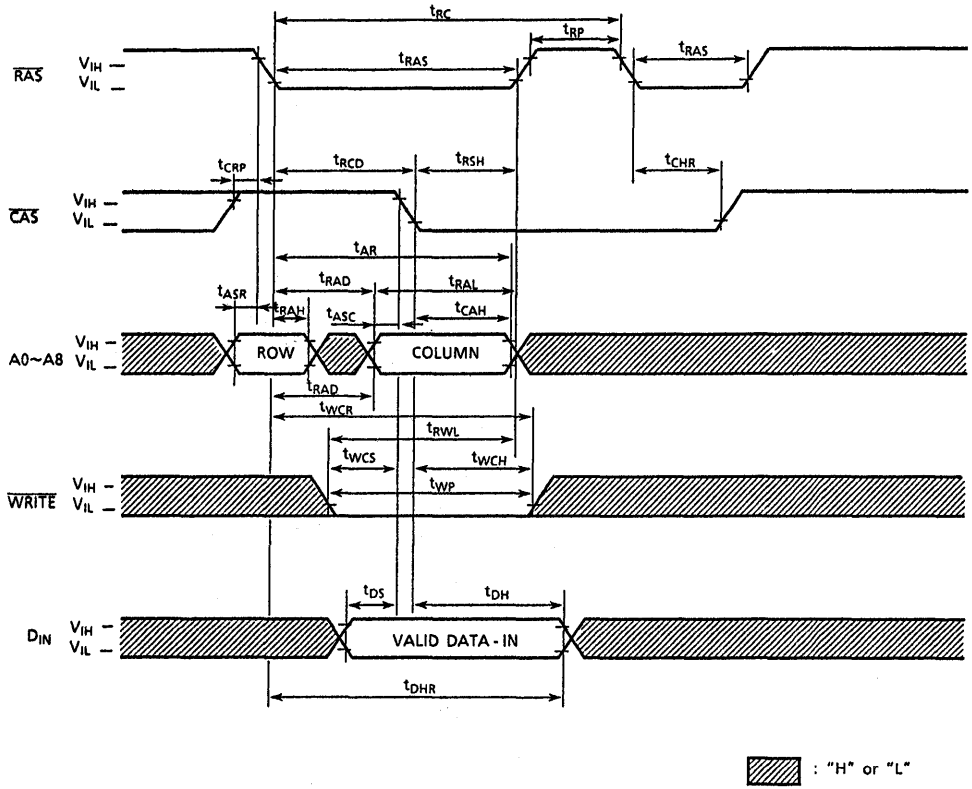


Note: A0~A8, $\overline{WRITE}$ = "H" or "L"

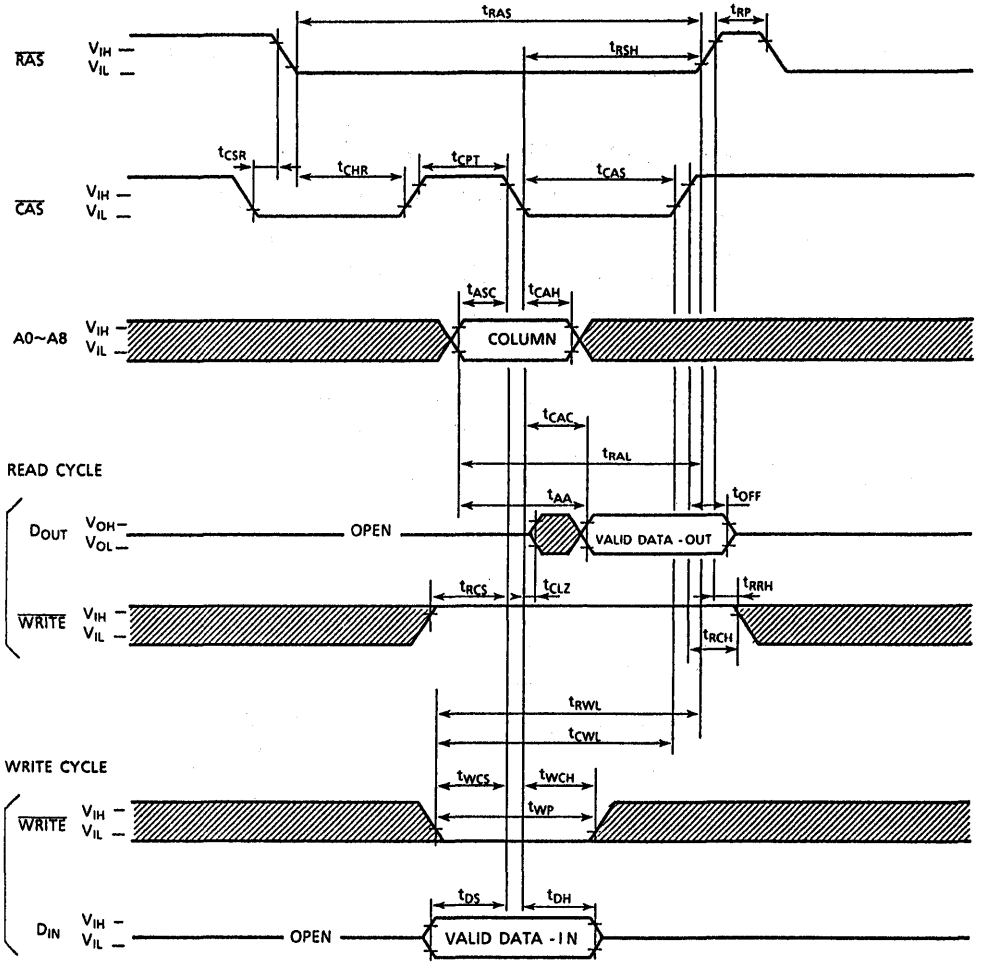
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



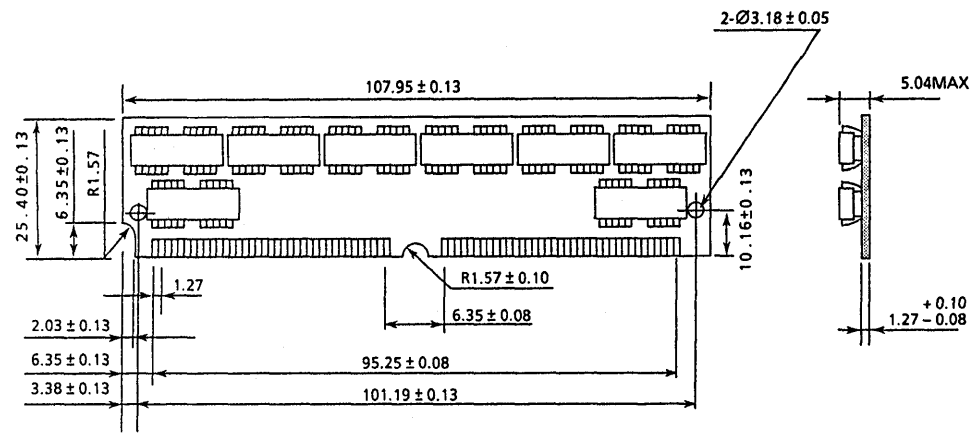
CAS BEFORE RAS REFRESH COUNTER TEST CYCLE

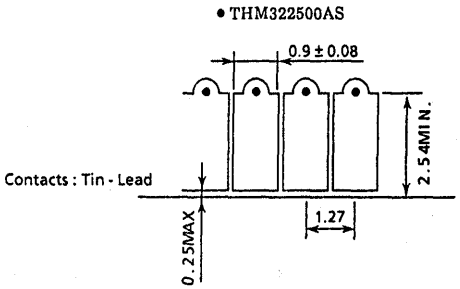


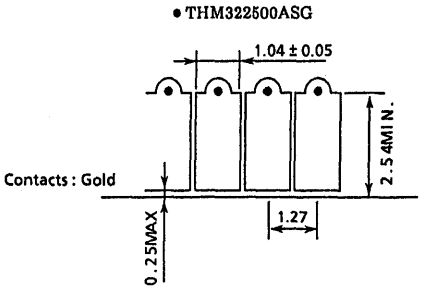
OUTLINE DRAWINGS

THM322500AS/ASG

Unit in mm







NOTES

1,048,576 WORDS×9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM91000AS/ASG/AL is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000AJ on the printed circuit board. The THM91000AS/ASG/AL is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

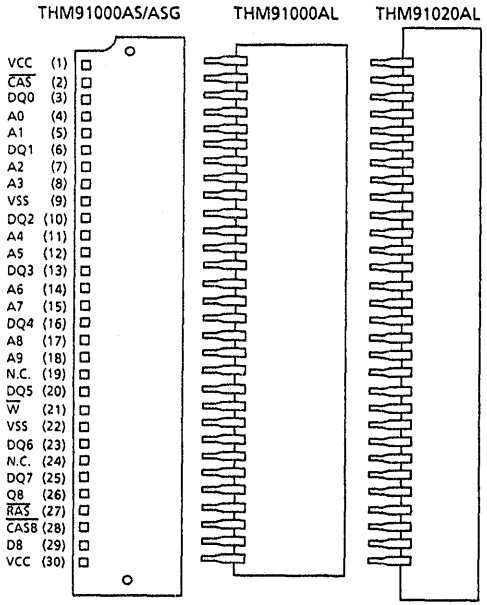
FEATURES

- 1,048,576 words by 9 bits organization
- Fast access time and cycle time

		THM91000 AS-70	THM91000 AS-80	THM91000 AS-10
t_{RAC}	$\overline{RAS}$ Access Time	70ns	80ns	100ns
t_{AA}	Column Address Access Time	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	25ns
t_{RC}	Cycle Time	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns	55ns

- Single power supply of 5V±10%
- Low power
  3,960mW MAX. Operating (THMxxxxxx-70)
  3,465mW MAX. Operating (THMxxxxxx-80)
  2,970mW MAX. Operating (THMxxxxxx-10)
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 8ms
- Tin-Lead Contact : THM91000AS-70, 80, 10
- Gold Contact : THM91000ASG-70, 80, 10

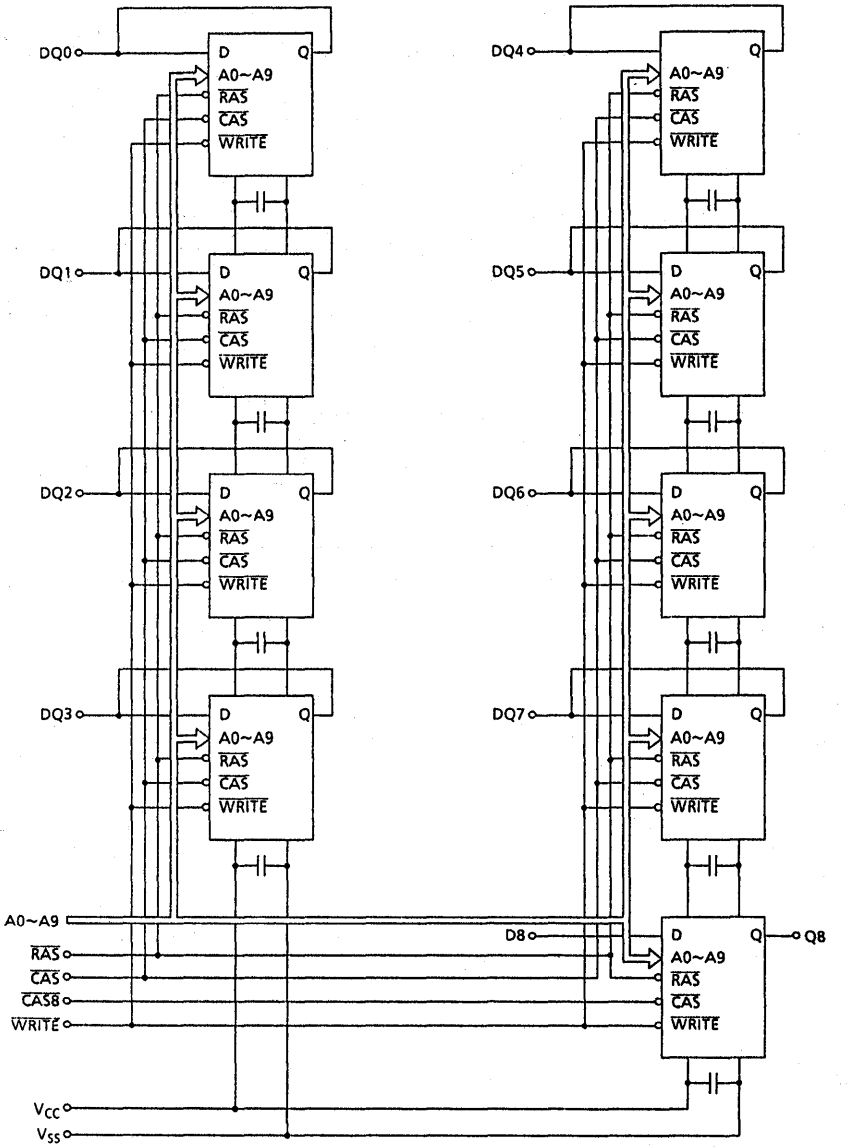
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THM91000AS-70	–	720	mA	3, 4
		THM91000AS-80	–	630		
		THM91000AS-10	–	540		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THM91000AS-70	–	720	mA	3
		THM91000AS-80	–	630		
		THM91000AS-10	–	540		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THM91000AS-70	–	540	mA	3, 4
		THM91000AS-80	–	450		
		THM91000AS-10	–	360		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THM91000AS-70	–	720	mA	3
		THM91000AS-80	–	630		
		THM91000AS-10	–	540		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 90	90	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THM91000AS-70		THM91000AS-80		THM91000AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THM91000AS-70		THM91000AS-80		THM91000AS-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	40	–	50	–	ns	

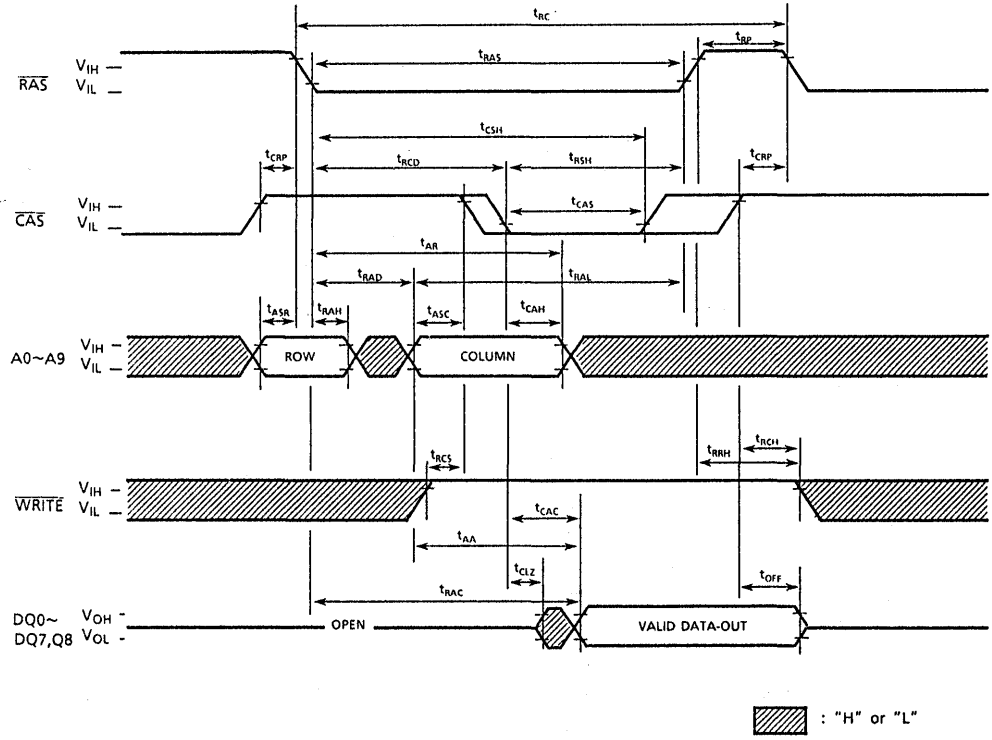
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input Capacitance (D8,$\overline{CAS8}$)	–	7	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	–	15	pF
C_{Q}	Input Capacitance (Q8)	–	10	pF

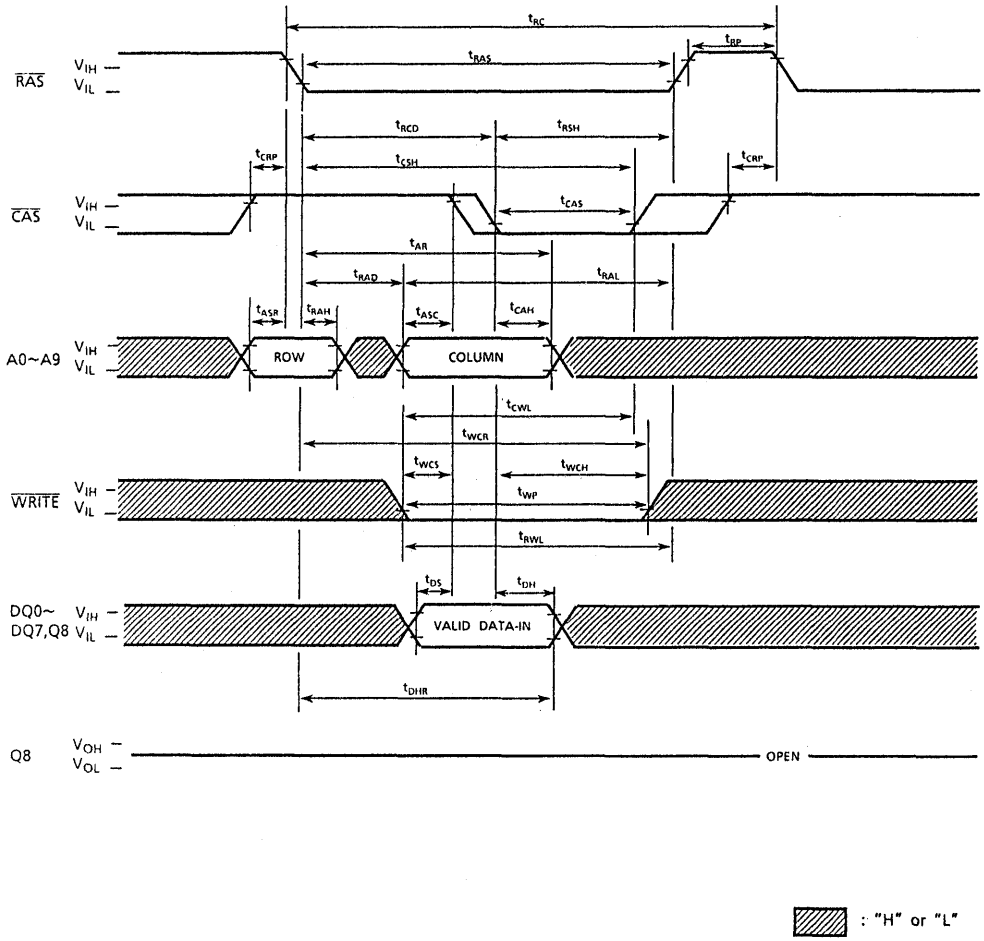
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

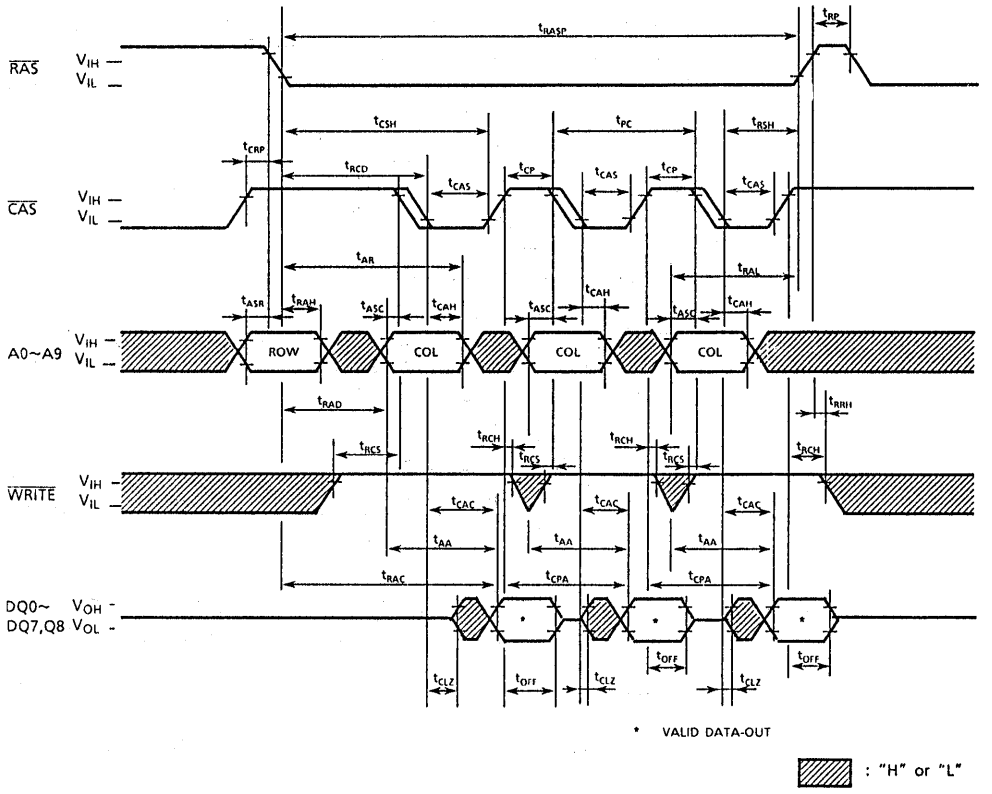
READ CYCLE


tRC
tRP
tRAS
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS VIH VIL
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0~A9 VIH VIL
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE VIH VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~ VOH
DQ7,Q8 VOL
OPEN
VALID DATA-OUT
: "H" or "L"

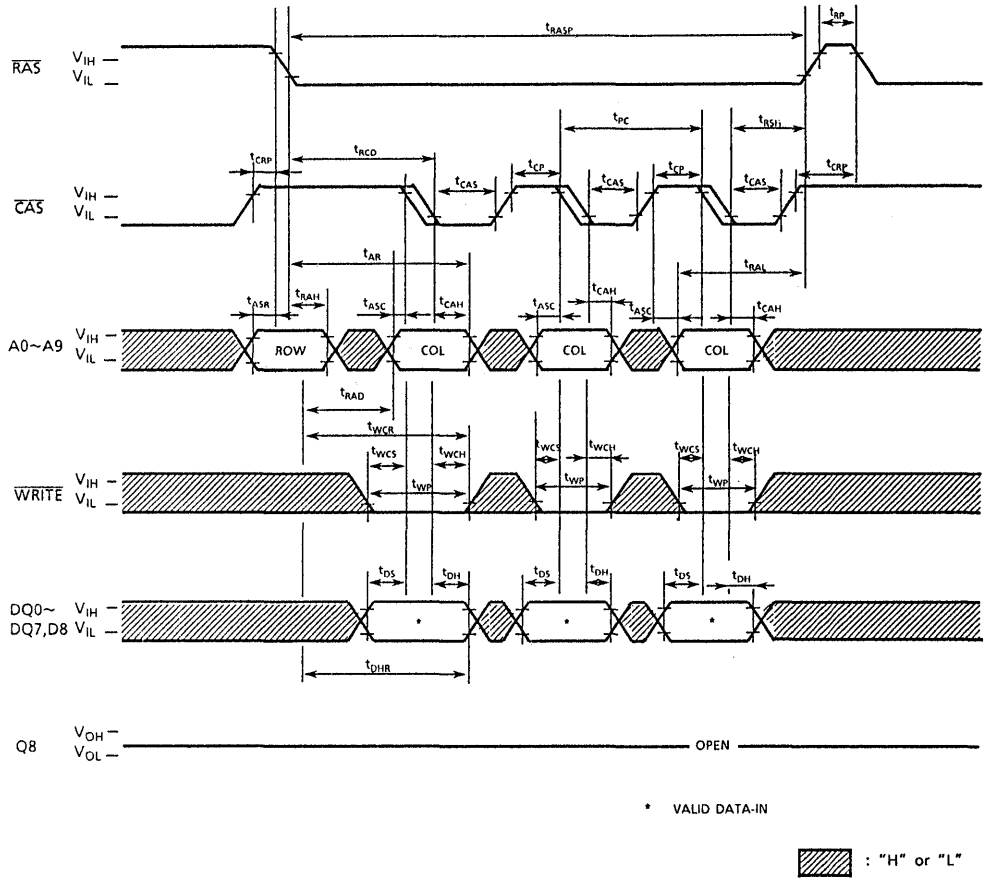
EARLY WRITE CYCLE



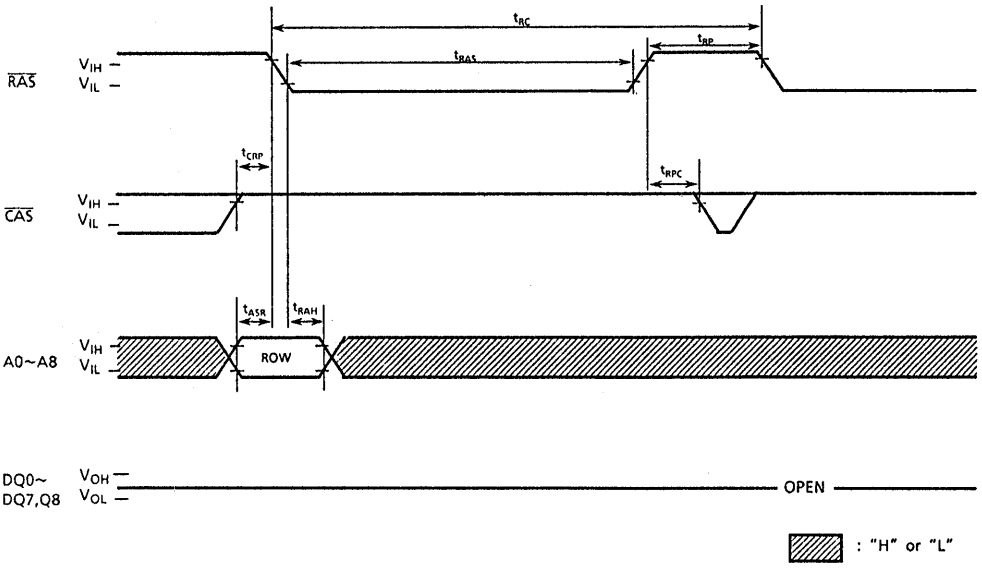
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

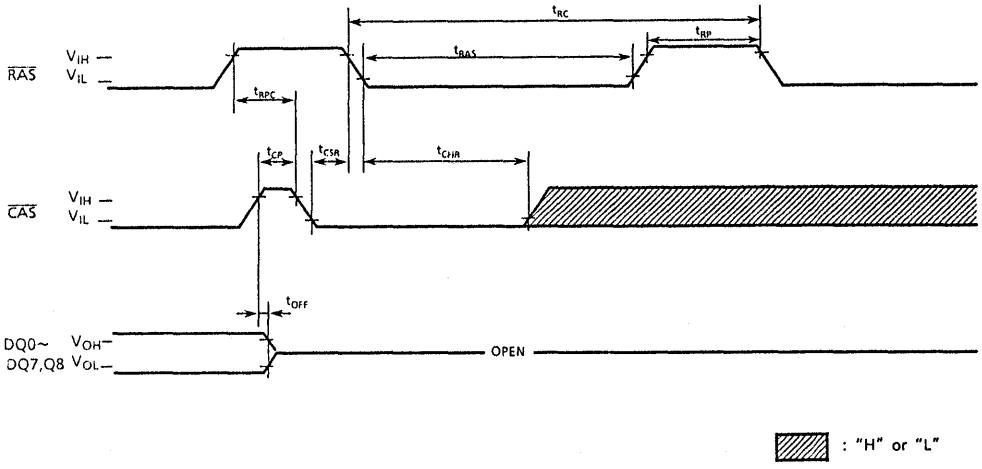


$\overline{RAS}$ ONLY REFRESH CYCLE



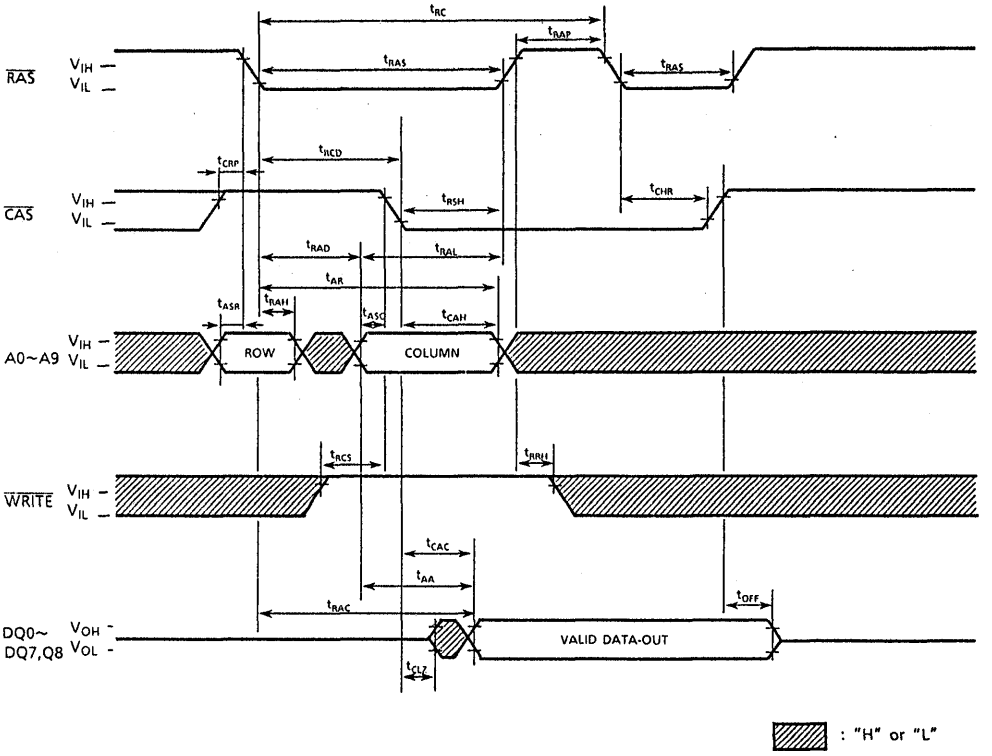
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

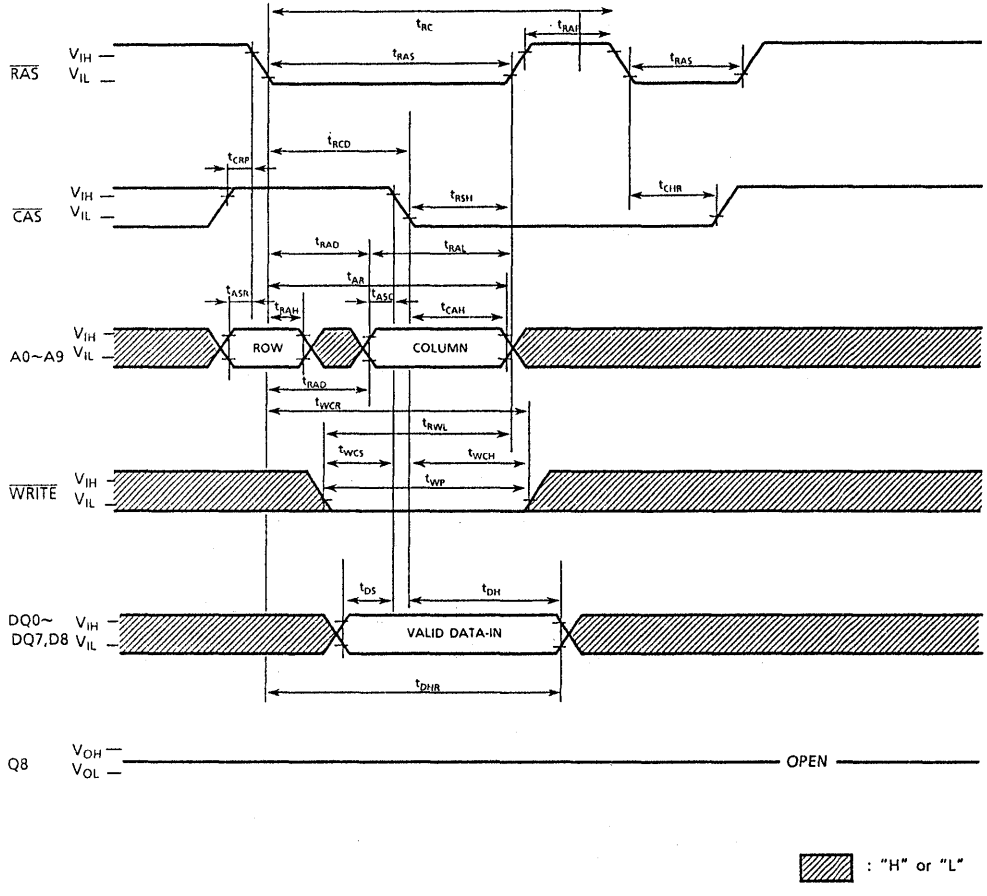


Note: $\overline{WRITE}$ = "H" or "L", A0~A9 = "H" or "L"

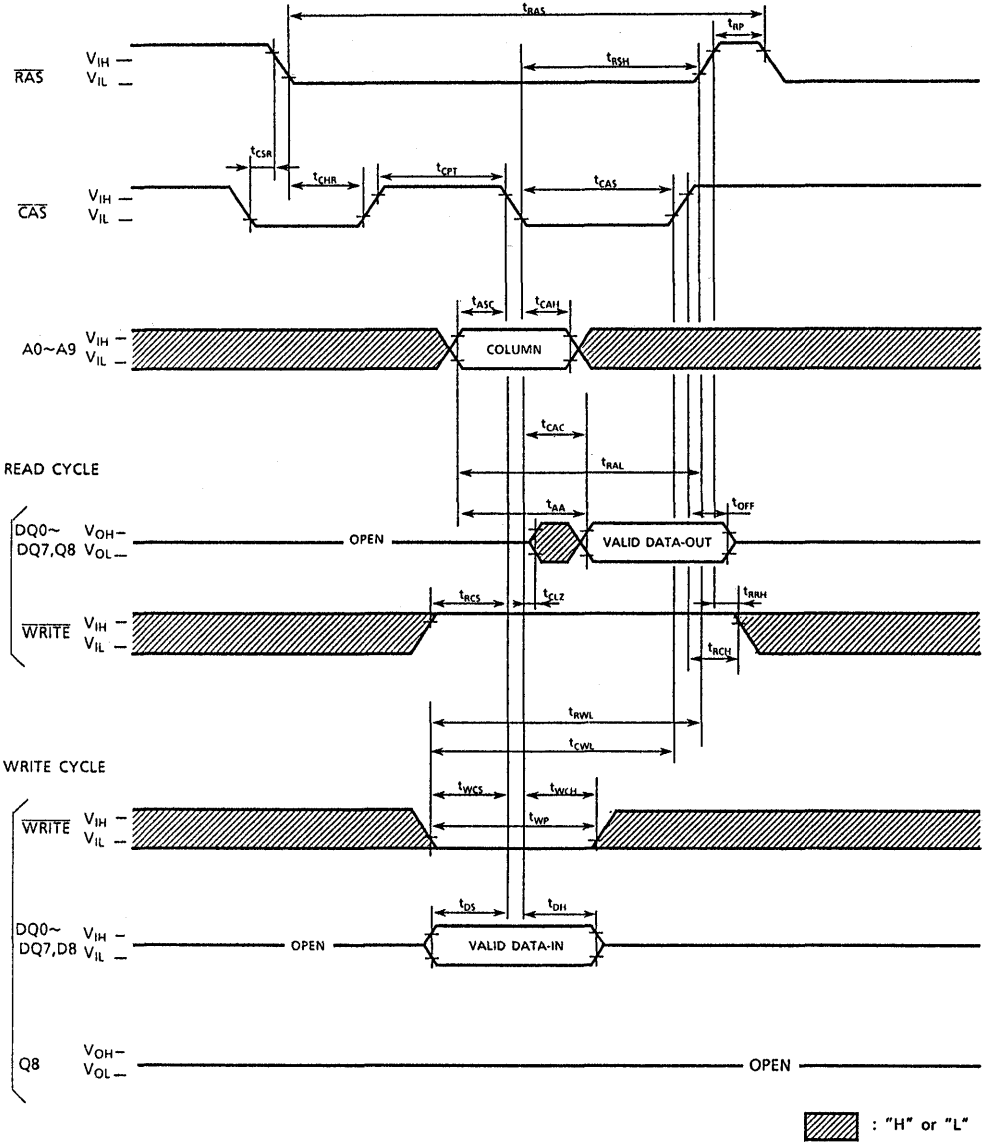
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



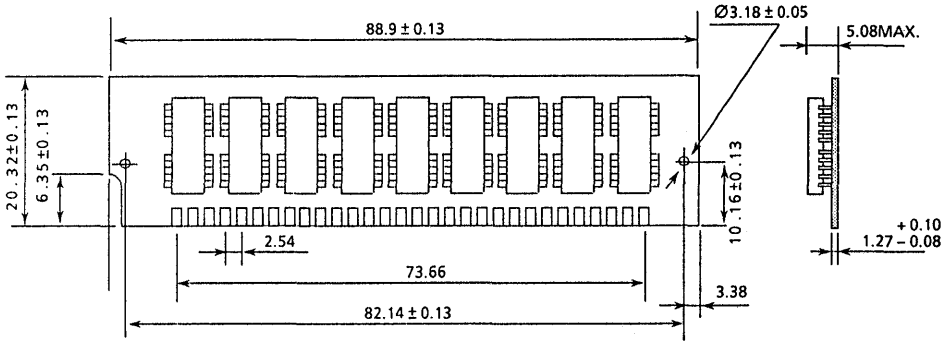
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CYCLE



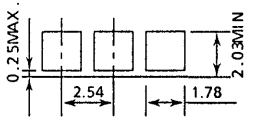
OUTLINE DRAWINGS

Unit: mm

• THM91000AS/ASG

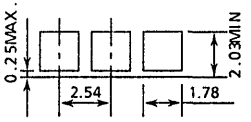


• THM91000AS
DETAIL OF CONTACTS



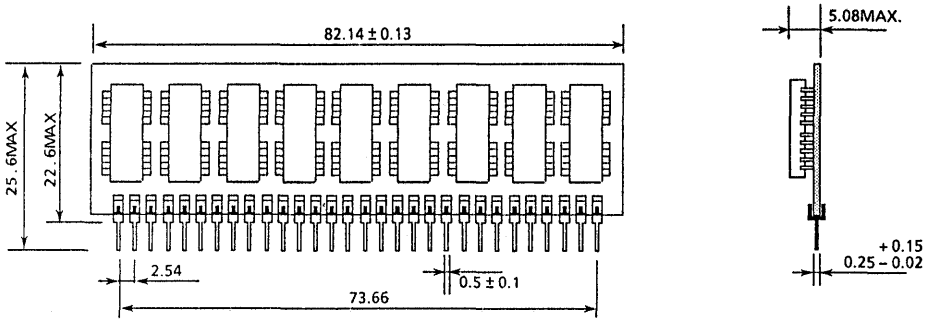
CONTACT : Tin-Lead

• THM91000ASG
DETAIL OF CONTACTS



CONTACT : Gold

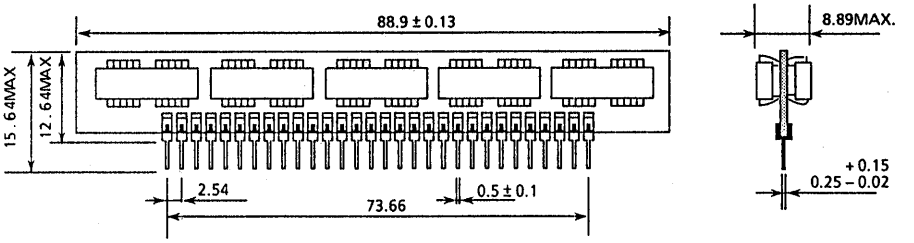
• THM91000AL



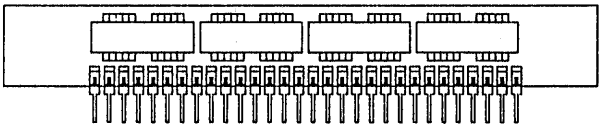
Unit : mm

• THM91020AL

FRONT SIDE



BACK SIDE



1,048,576 WORDS×9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM91000BS/BSG/BL is a 1,048,576 words by 9 bits dynamic RAM module which assembled 9 pcs of TC511000BJ on the printed circuit board. The THM91000BS / BSG / BL is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

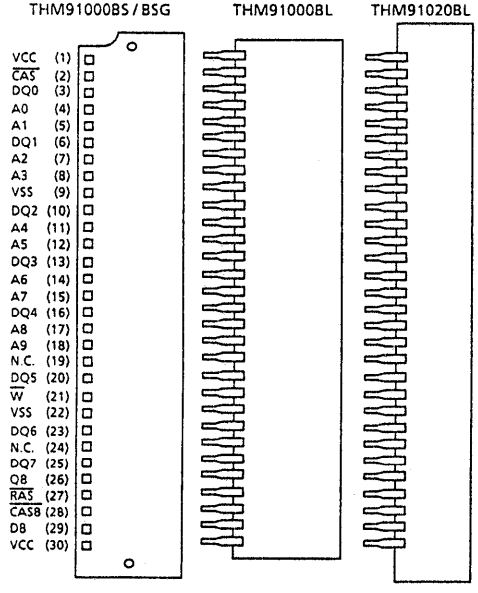
FEATURES

- 1,048,576 words by 9 bits organization
- Fast access time and cycle time

		THM91000BS-60
t_{RAC}	$\overline{RAS}$ Access Time	60ns
t_{AA}	Column Address Access Time	30ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns
t_{RC}	Cycle Time	110ns
t_{PC}	Fast Page Mode Cycle Time	40ns

- Single power supply of 5V±10%
- Low power
  4,455mW MAX. Operating
  49.5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- All inputs and outputs TTL compatible
- 512 refresh cycles/ 8ms
- Tin-Lead Contact : THM91000BS-60
- Gold Contact : THM91000BSG-60

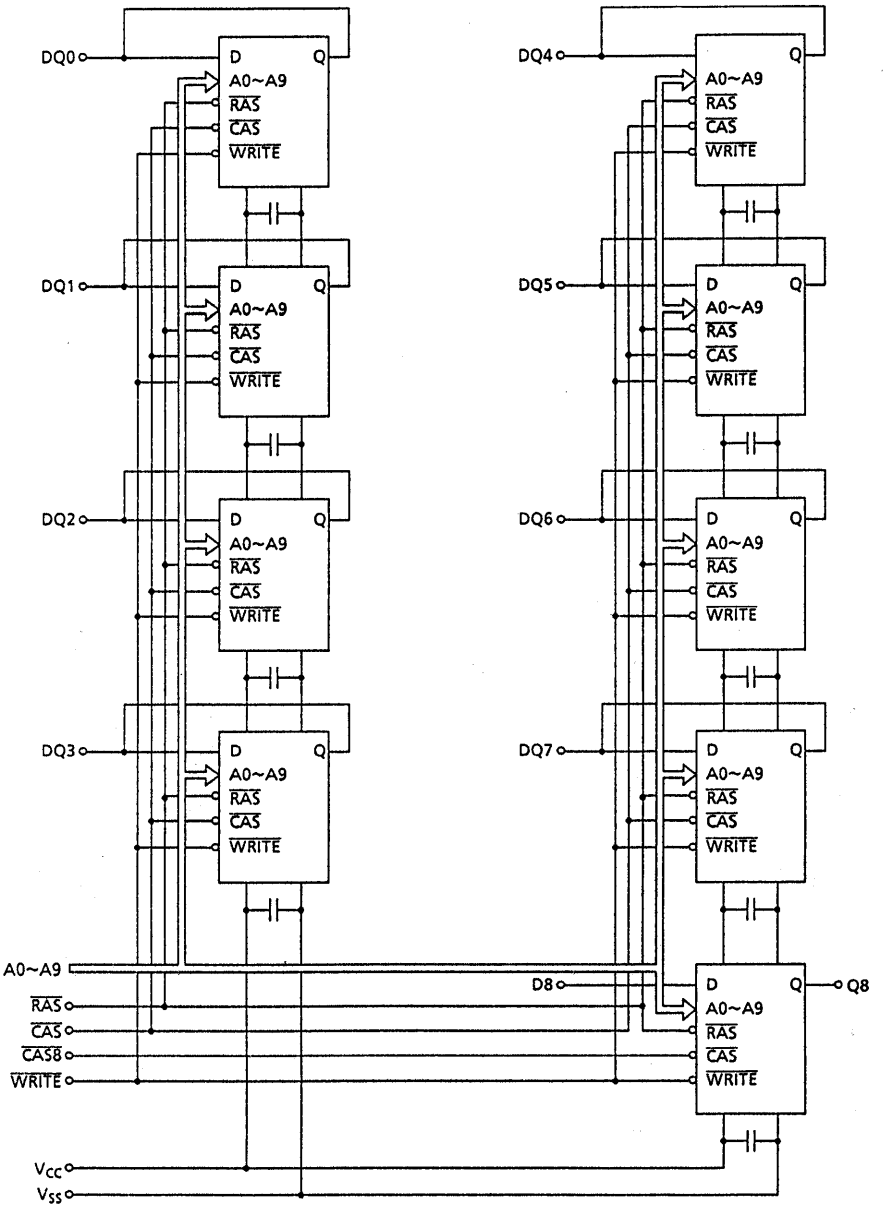
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Input/Outputs
D8	Data Input
Q8	Data Output
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	5.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	–	810	mA	3, 4
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	–	18	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	–	810	mA	3
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Address Cycling: $t_{PC} = t_{PC}$ MIN.)	–	540	mA	3, 4
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)	–	9	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	–	810	mA	3
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)	–90	90	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)	–20	20	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = –5mA)	2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{RC}	Random Read or Write Cycle Time	110	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	ns	8, 13
t_{AA}	Access Time from Column Address	–	30	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	ns	8
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	ns	10
t_{WCH}	Write Command Hold Time	10	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t_{WP}	Write Command Pulse Width	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	ns	
t_{DS}	Data Set-Up Time	0	–	ns	11
t_{DH}	Data Hold Time	15	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	ns	
t_{REF}	Refresh Period	–	8	ms	
t_{WCS}	Write Command Set-UP Time	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	ns	

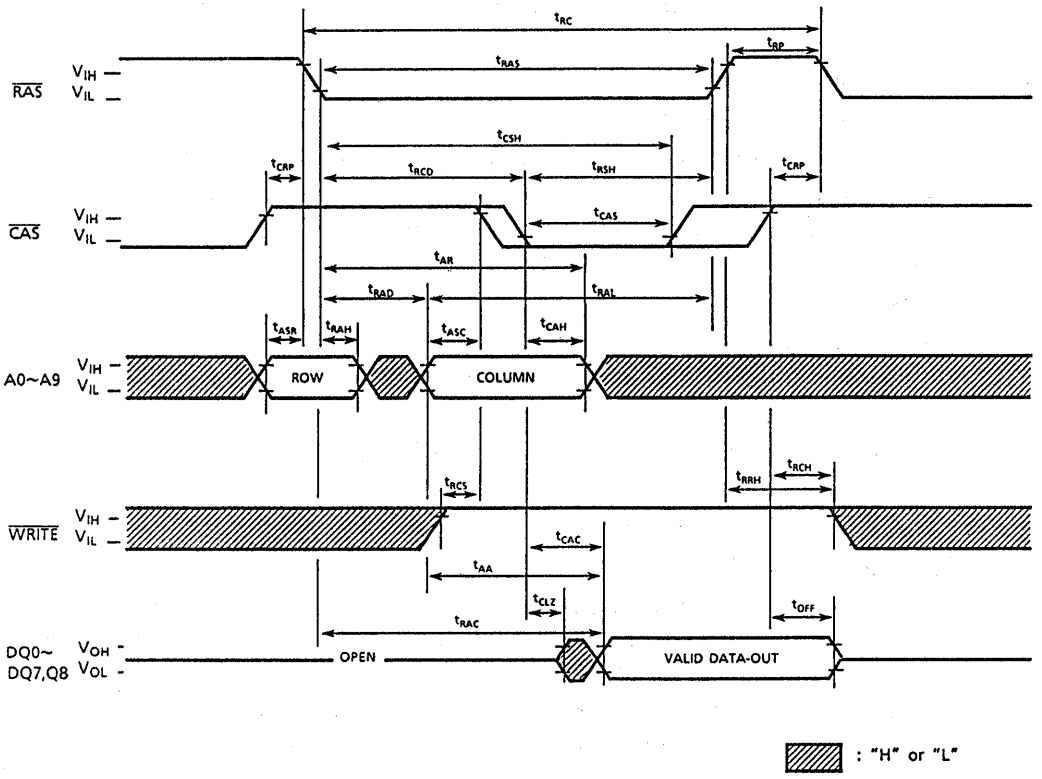
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{I2}	Input Capacitance (D8,$\overline{CAS8}$)	–	7	pF
C_{DQ}	Input Capacitance (DQ0~DQ7)	–	15	pF
C_{Q}	Input Capacitance (Q8)	–	10	pF

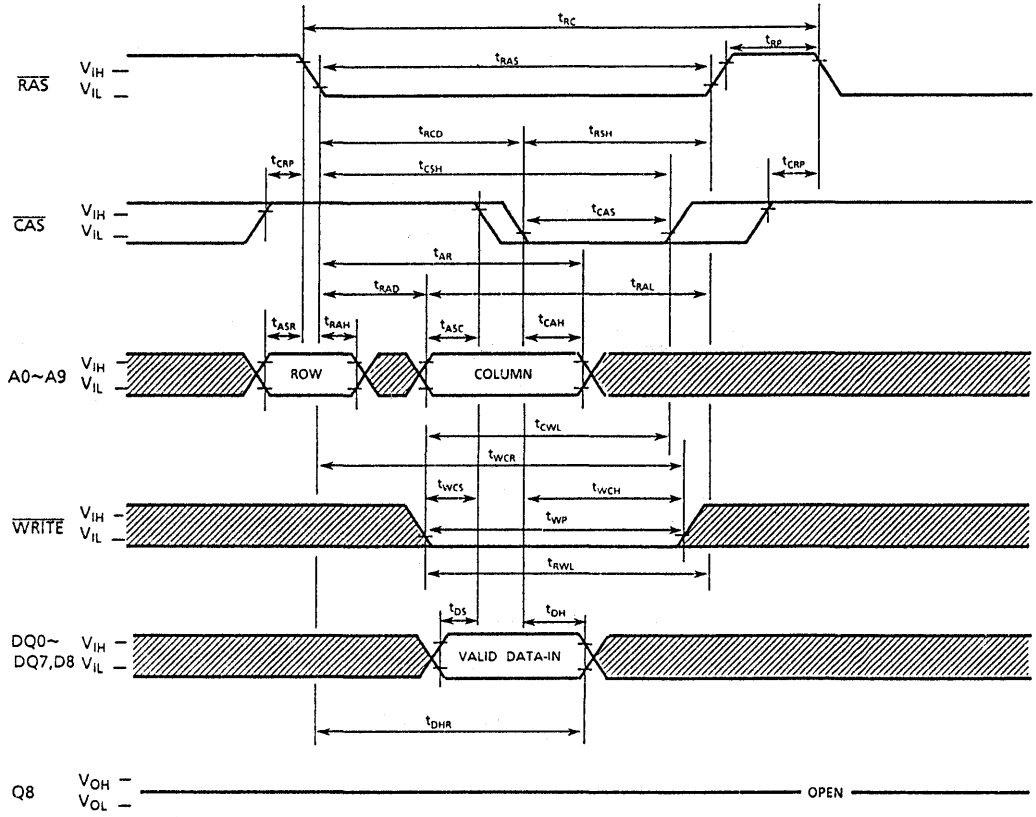
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified value are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met.
    t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit, insures that t_{RAC}(max.) can be met.
    t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

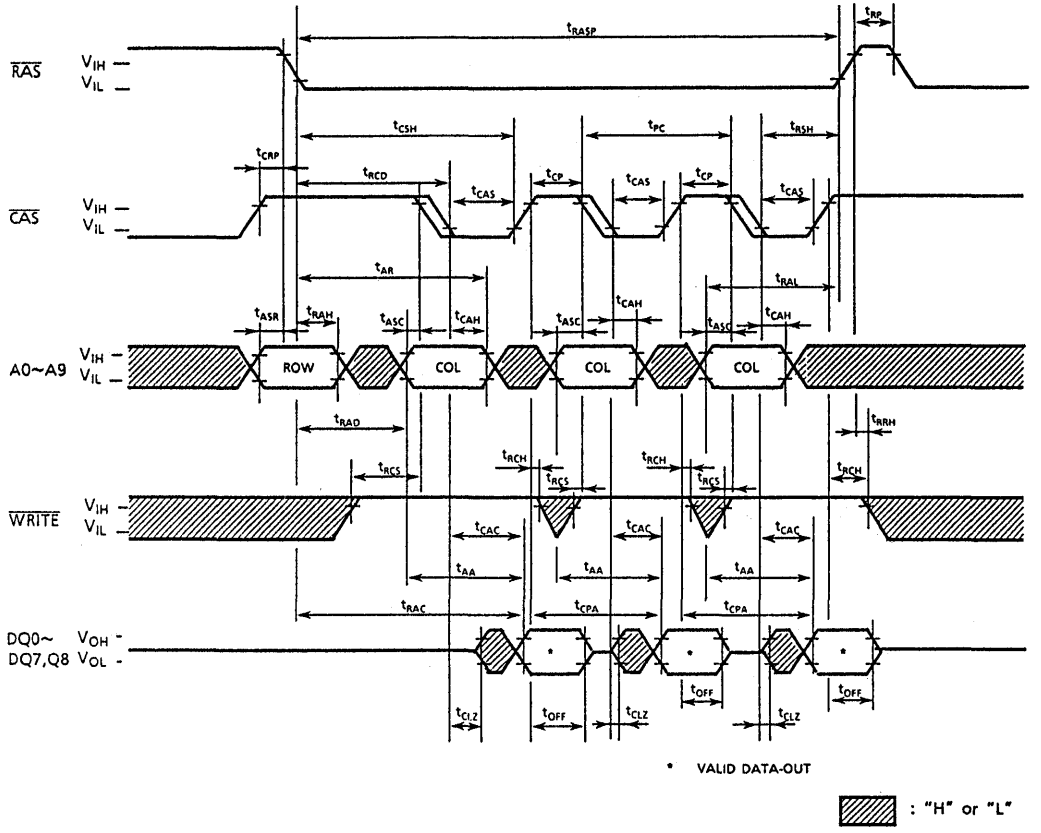

tRC
tRP
tRAS
VIH
RAS VIL
tCSH
tCRP
tRCD
tRSH
tCAP
VIH
CAS VIL
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
VIH
A0~A9 VIL
ROW
COLUMN
tRCS
tRRH
tRCH
VIH
WRITE VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ0~ VOH
DQ7,Q8 VOL
OPEN
VALID DATA-OUT
: "H" or "L"

EARLY WRITE CYCLE

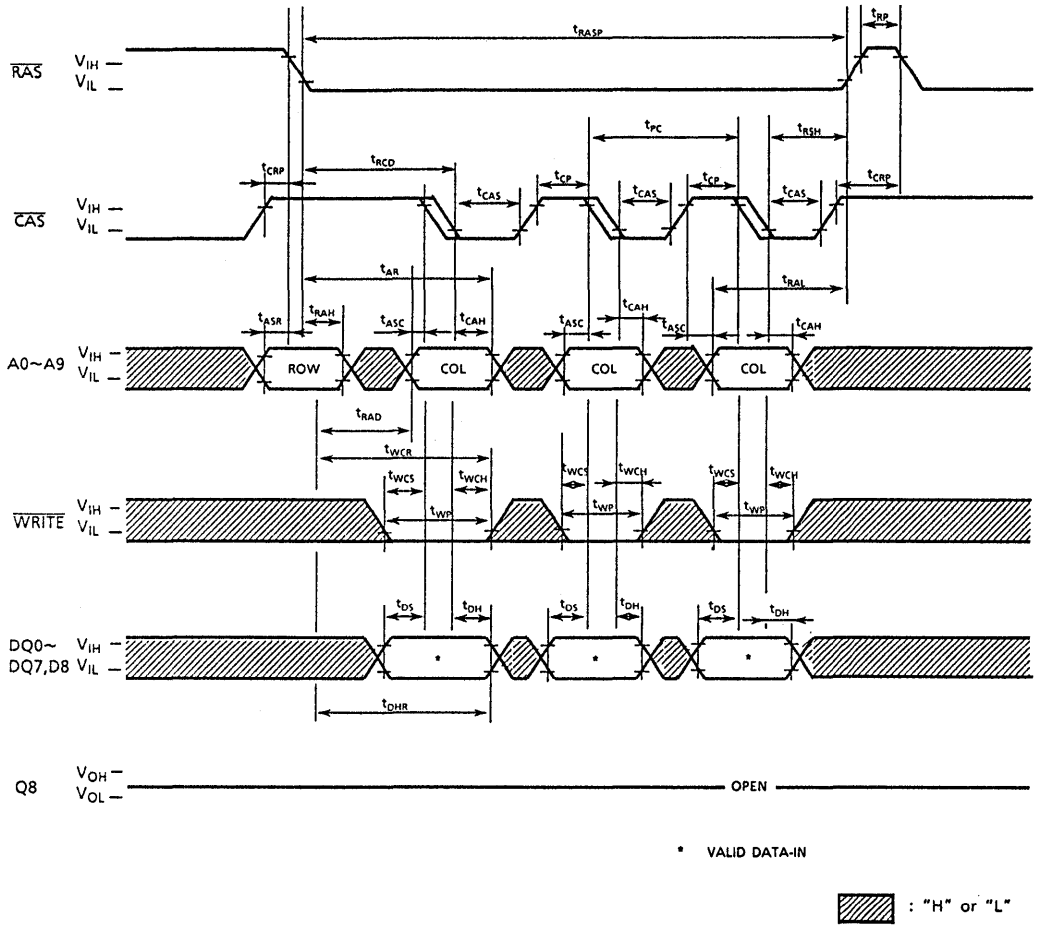


: "H" or "L"

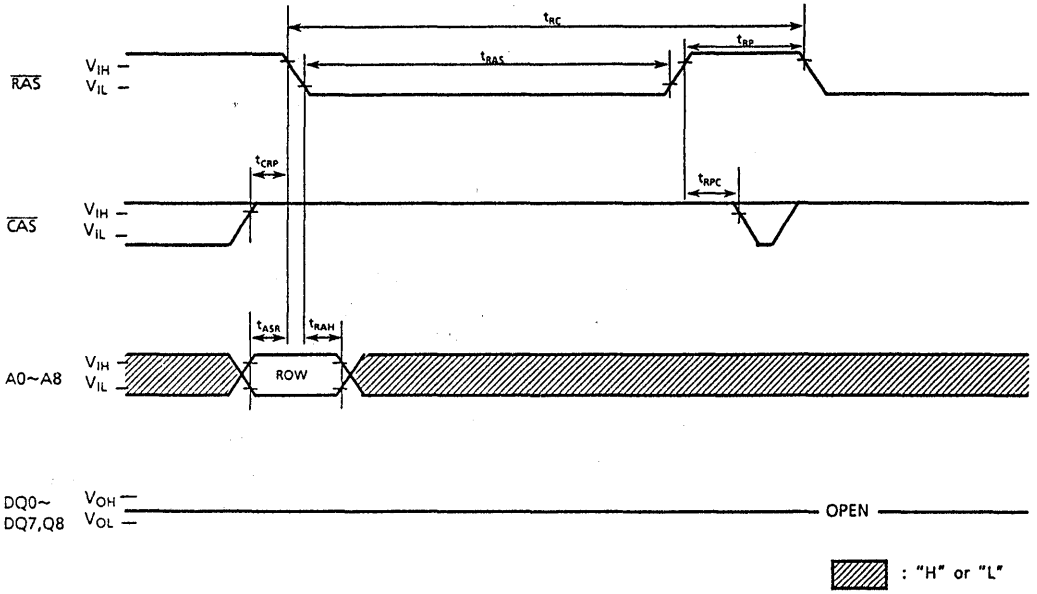
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

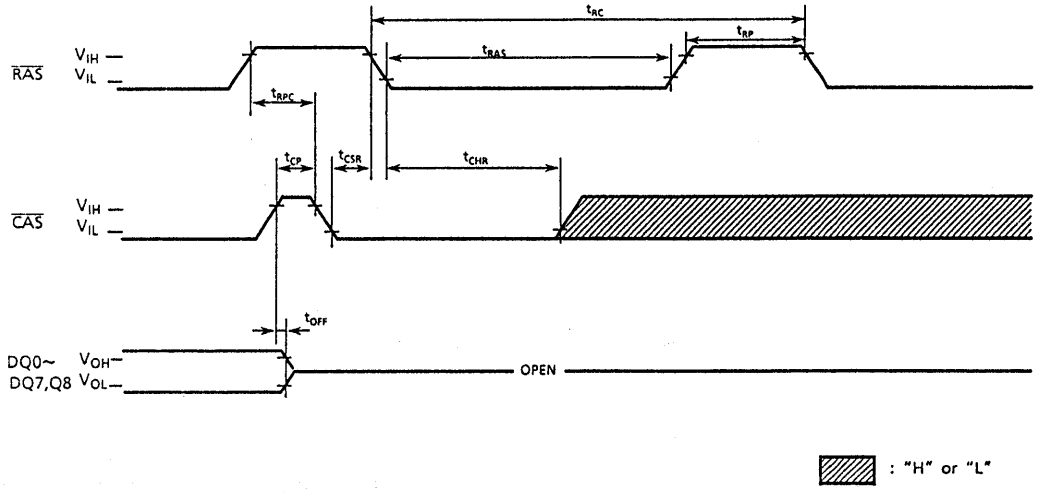


$\overline{RAS}$ ONLY REFRESH CYCLE



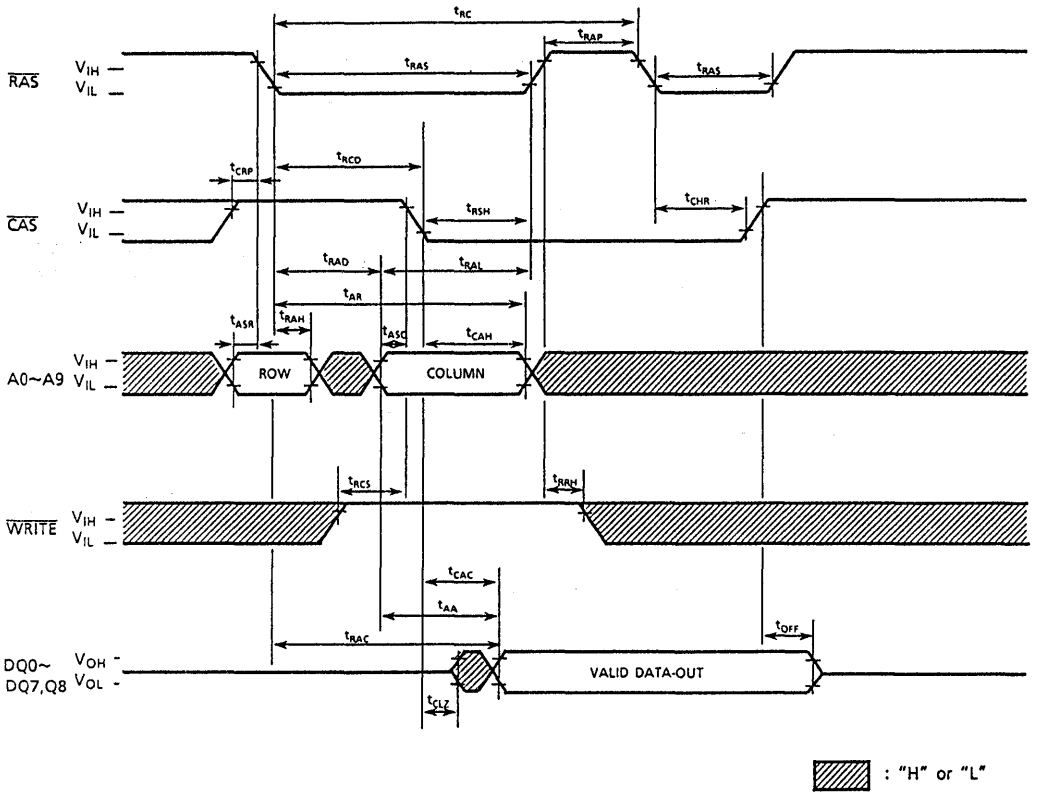
Note: $\overline{WRITE}$ = "H" or "L", A9 = "H" or "L"

$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE

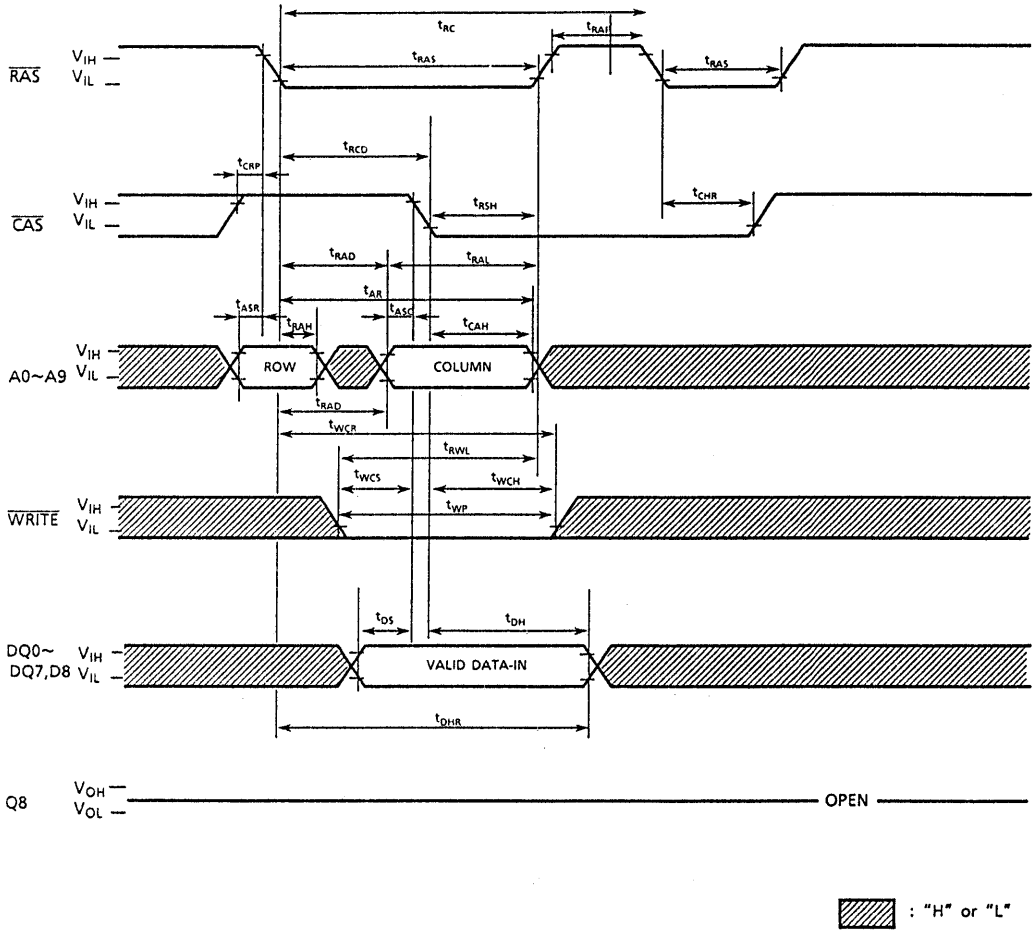


Note: $\overline{\text{WRITE}}$ = "H" or "L", A0~A9 = "H" or "L"

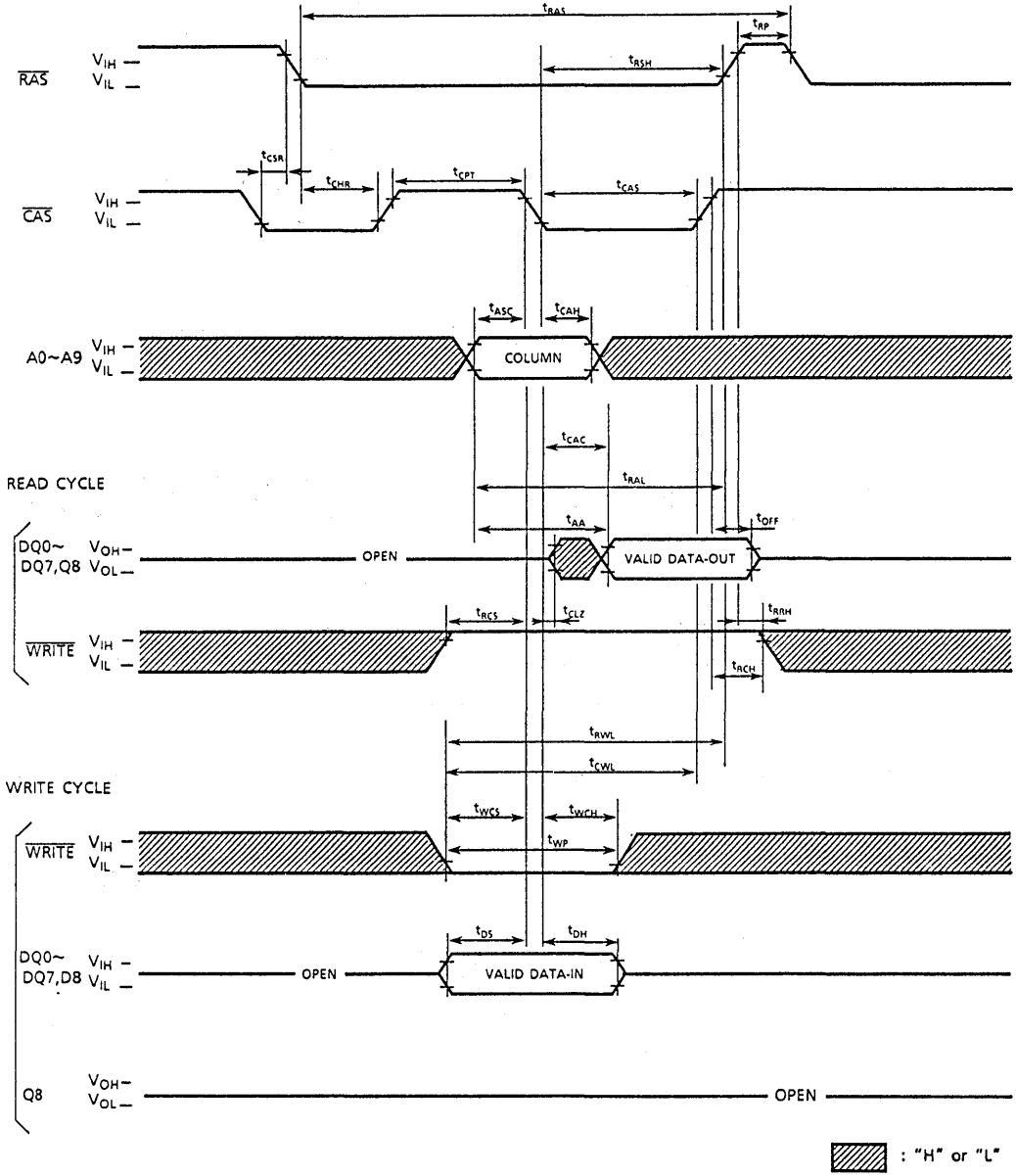
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



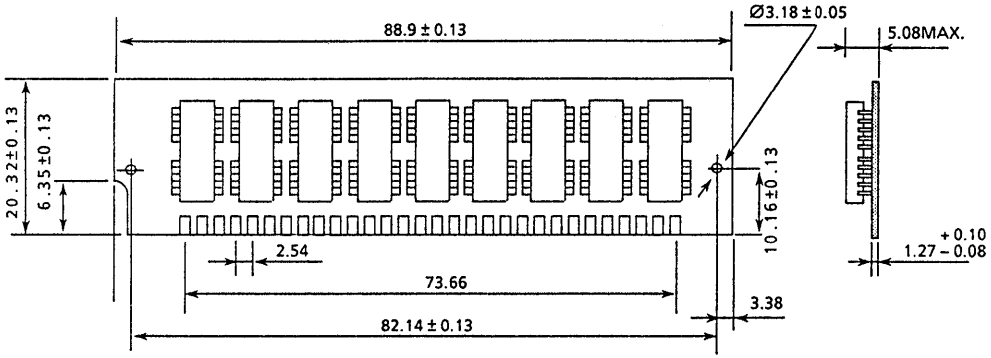
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CYCLE



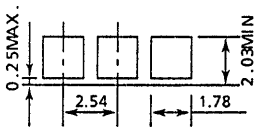
OUTLINE DRAWINGS

Unit: mm

● THM91000BS / BSG

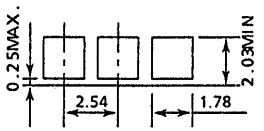


● THM91000BS
DETAIL OF CONTACTS



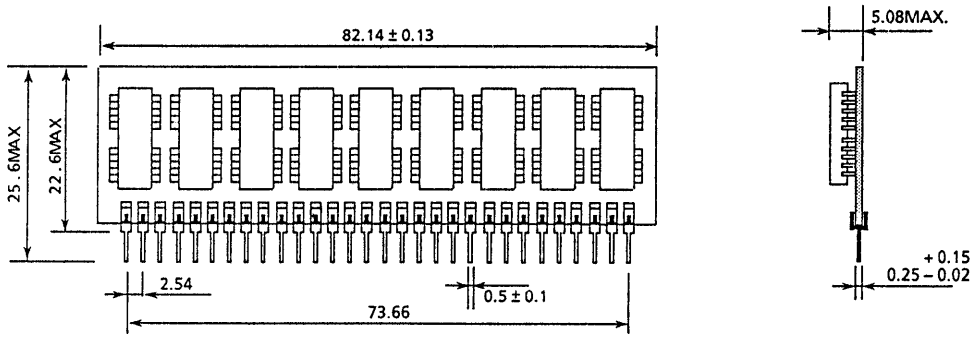
Contacts : Tin-Lead

● THM91000BSG
DETAIL OF CONTACTS



Contacts : Gold

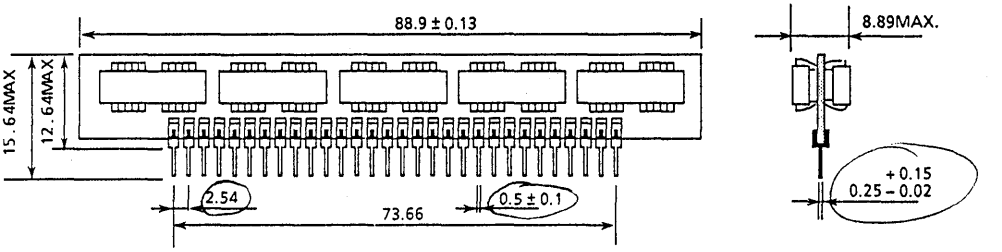
● THM91000BL



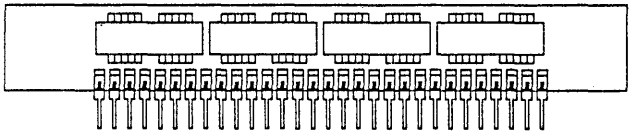
Unit : mm

● THM91020BL

FRONT SIDE



BACK SIDE



1,048,576 WORDS × 9 BIT DYNAMIC RAM MODULE

PRELIMINARY

DESCRIPTION

The THM91070S/L is a 1,048,576 words by 9 bits dynamic RAM module which assembled 2 pcs of TC514400J and 1pc of TC511000AJ on the printed circuit board.

The THM91070S/L is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

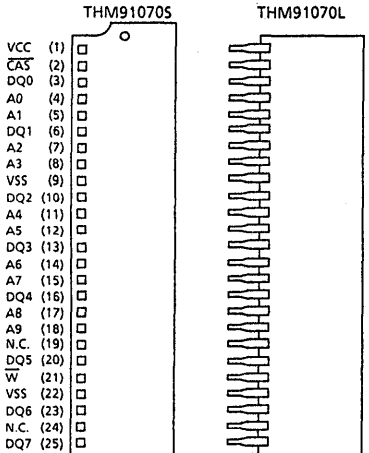
FEATURES

- 1,048,576 words by 9 bits organization
- Fast access time

		-80	-10
t_{RAC}	$\overline{RAS}$ Access Time	80ns	100ns
t_{AA}	Column Address Access Time	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	25ns
t_{RC}	Cycle Time	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	50ns	60ns

- Single power supply of 5V±10%
- Low power 1,540mW MAX. Operating (THMxxxxxx-80)
  1,320mW MAX. Operating (THMxxxxxx-10)
  16,5mW MAX. Standby
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/ 8ms (Burst Refresh)
- 1,024 refresh cycles/16ms (Distributed Refresh)

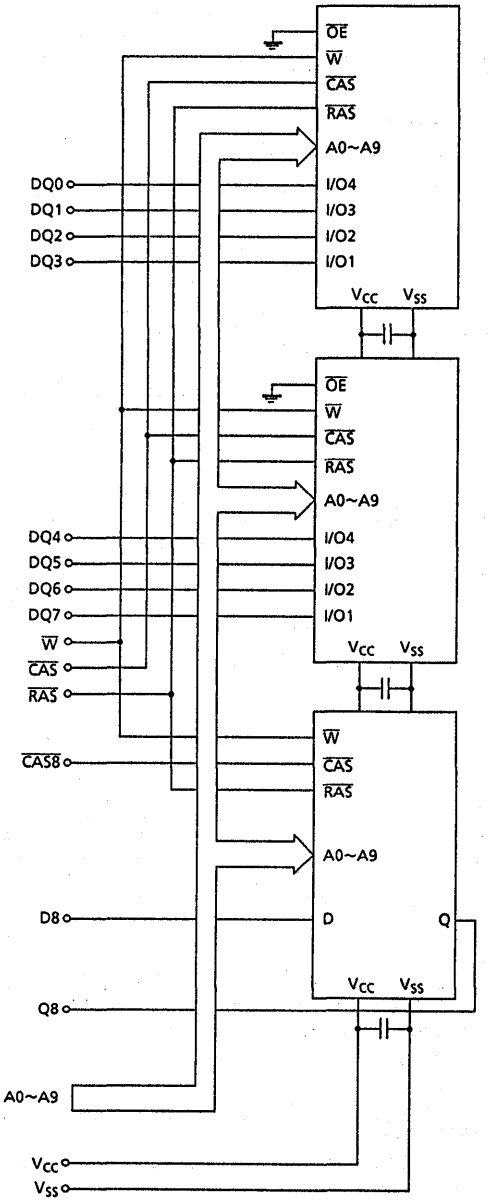
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
D8	Data Inputs
Q8	Data Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	1.8	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	280	mA	3, 4
		THMxxxxxx−10	–	240		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	9	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	280	mA	3
		THMxxxxxx−10	–	240		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxxx−80	–	190	mA	3, 4
		THMxxxxxx−10	–	160		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2V)		–	3	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx−80	–	280	mA	3
		THMxxxxxx−10	–	240		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any Input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins not under Test = 0V)		−30	30	µA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		−10	10	µA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = 5 − mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	ns	8, 13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	ns	8, 13
t_{AA}	Access Time from Column Address	–	40	–	50	ns	8, 14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	55	ns	8
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	ns	8
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	7
t_{RP}	$\overline{RAS}$ Precharge Time	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	80	200,000	100	200,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	10
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	10
t_{WCH}	Write Command Hold Time	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	ns	11
t_{DH}	Data Hold Time	15	–	20	–	ns	11
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	ns	12
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	10	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	ns	

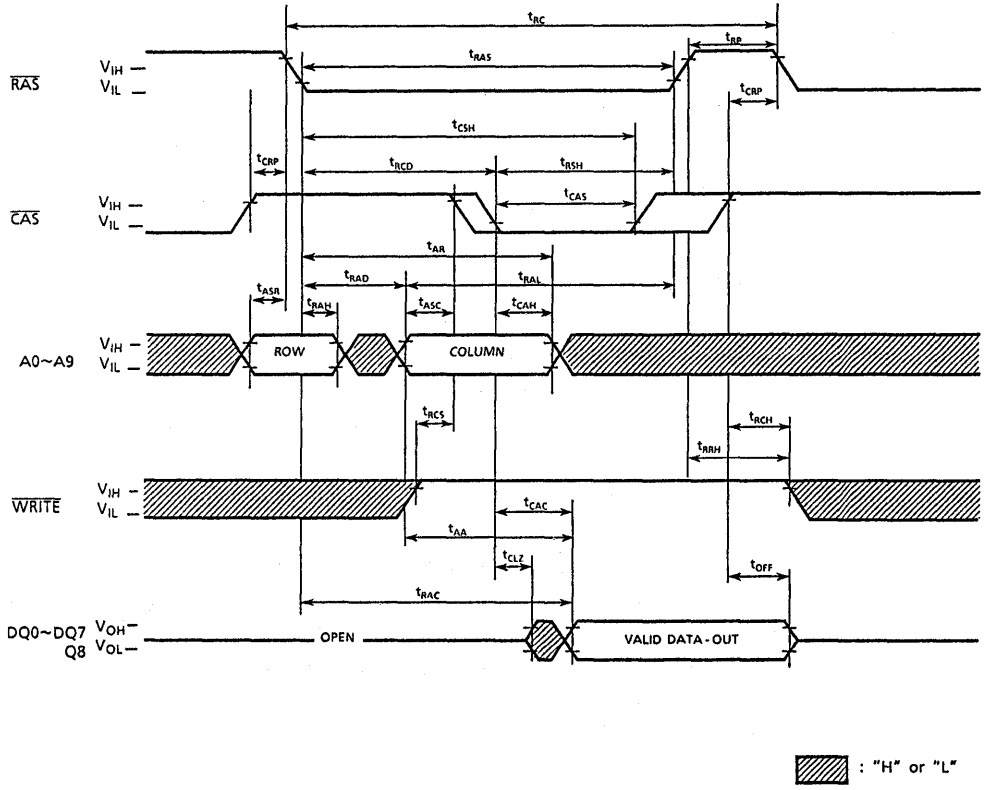
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	30	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF
C_Q	Output Capacitance (Q8)	–	10	pF

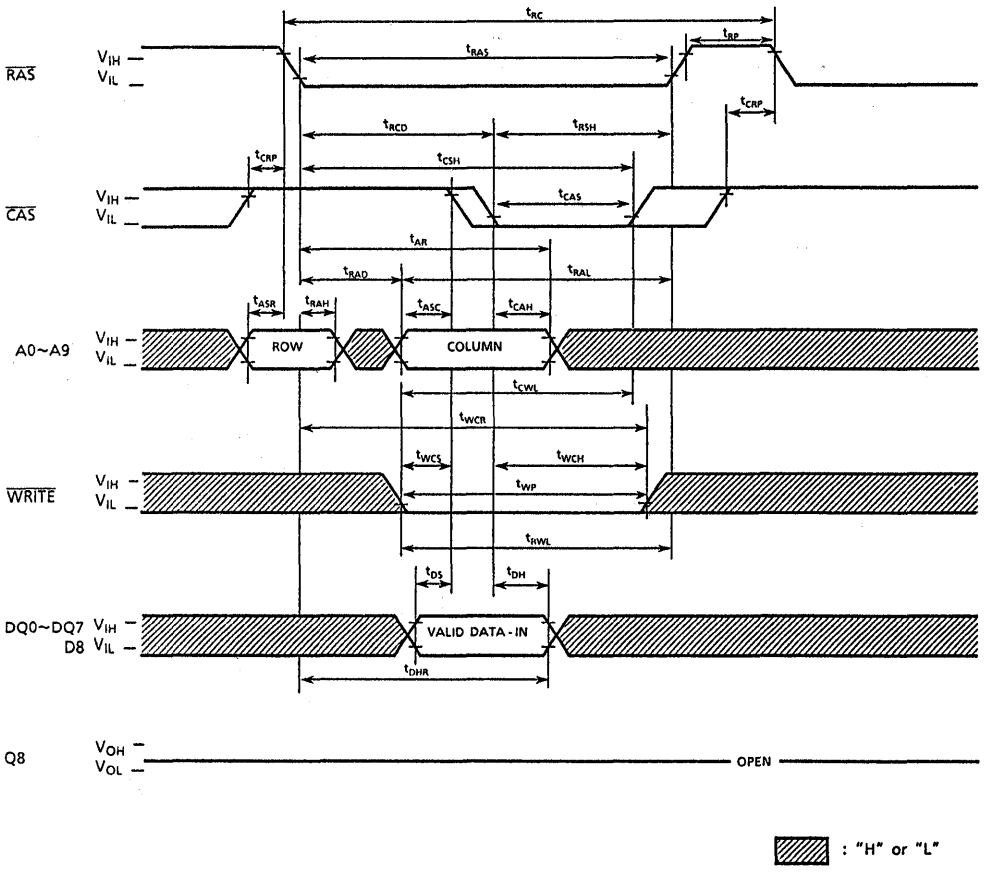
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge.
12. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
13. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

READ CYCLE

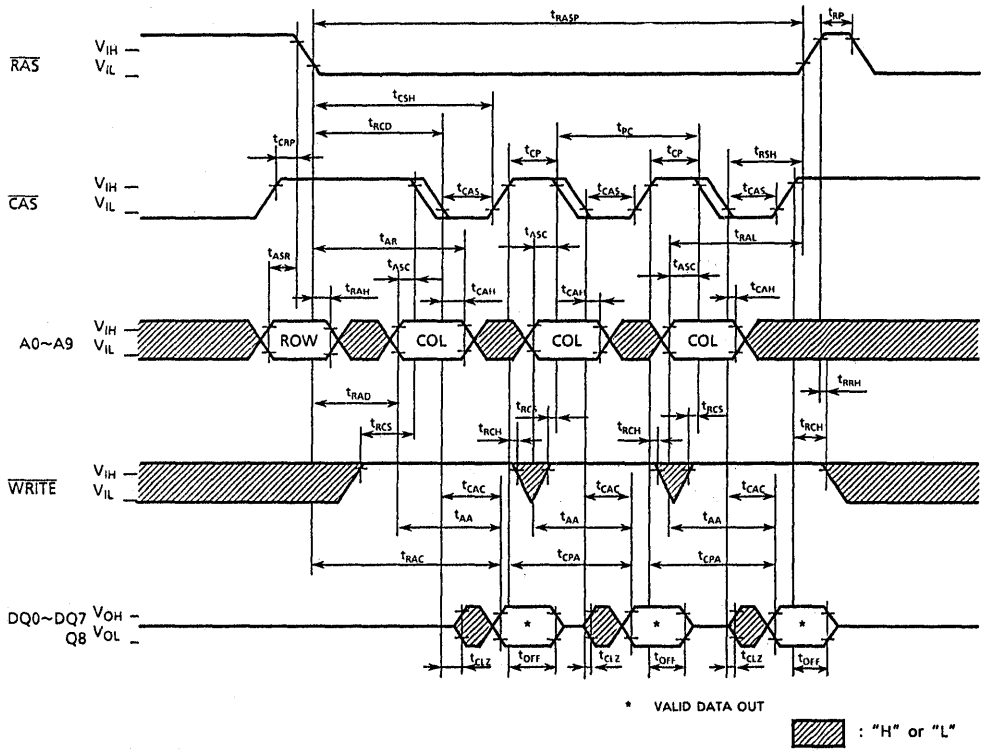

RAS
CAS
A0~A9
WRITE
DQ0~DQ7
Q8
VIH
VIL
VOH
VOL
tRC
tRP
tRAS
tCRP
tCSH
tRCD
tRSH
tCAS
tAR
tRAD
tRAL
tASR
tRAH
tASC
tCAH
ROW
COLUMN
tRCS
tRCH
tRRH
tCAC
tAA
tCLZ
tOFF
tRAC
OPEN
VALID DATA-OUT
: "H" or "L"

EARLY WRITE CYCLE

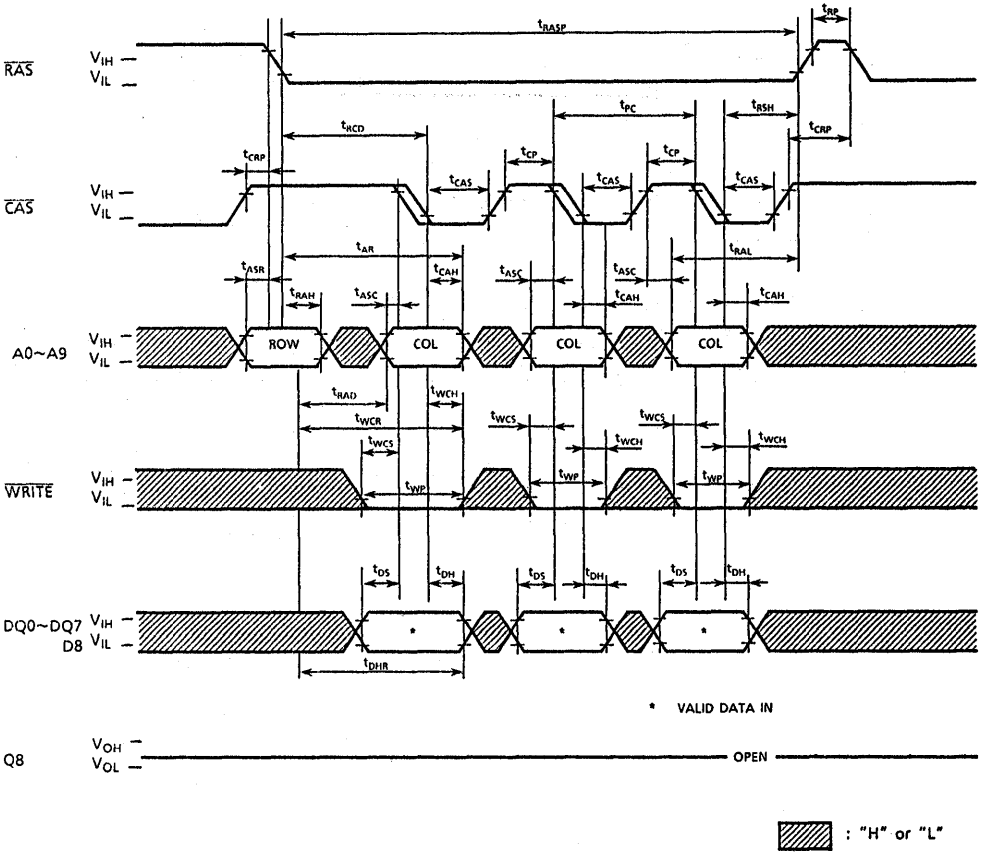


: "H" or "L"

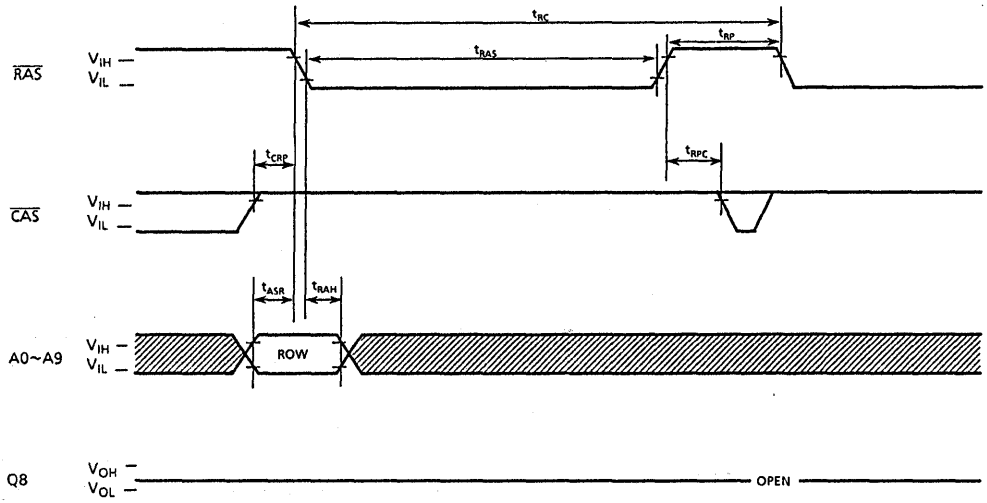
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



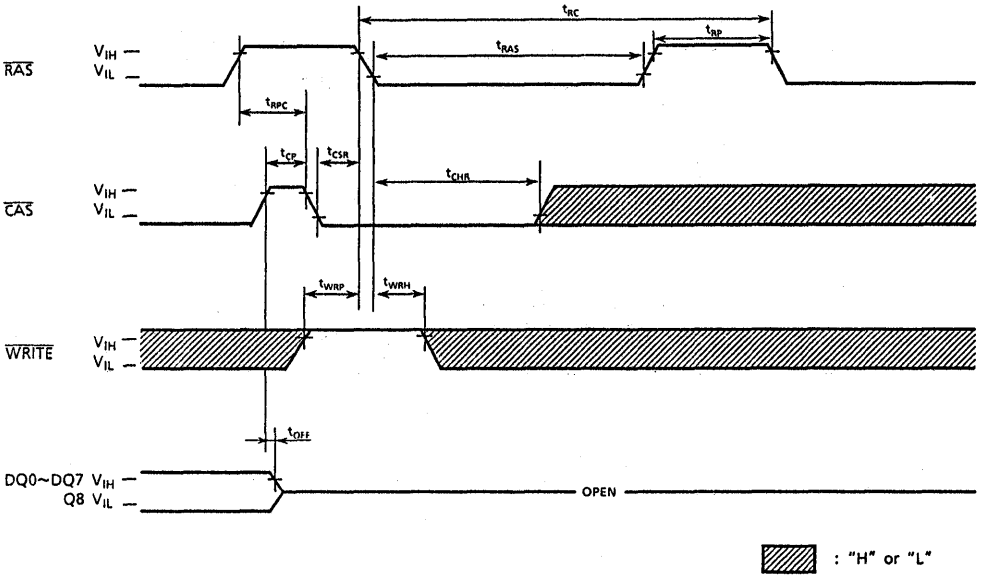
$\overline{RAS}$ ONLY REFRESH CYCLE



Note: $\overline{WRITE}$ = "H" or "L"

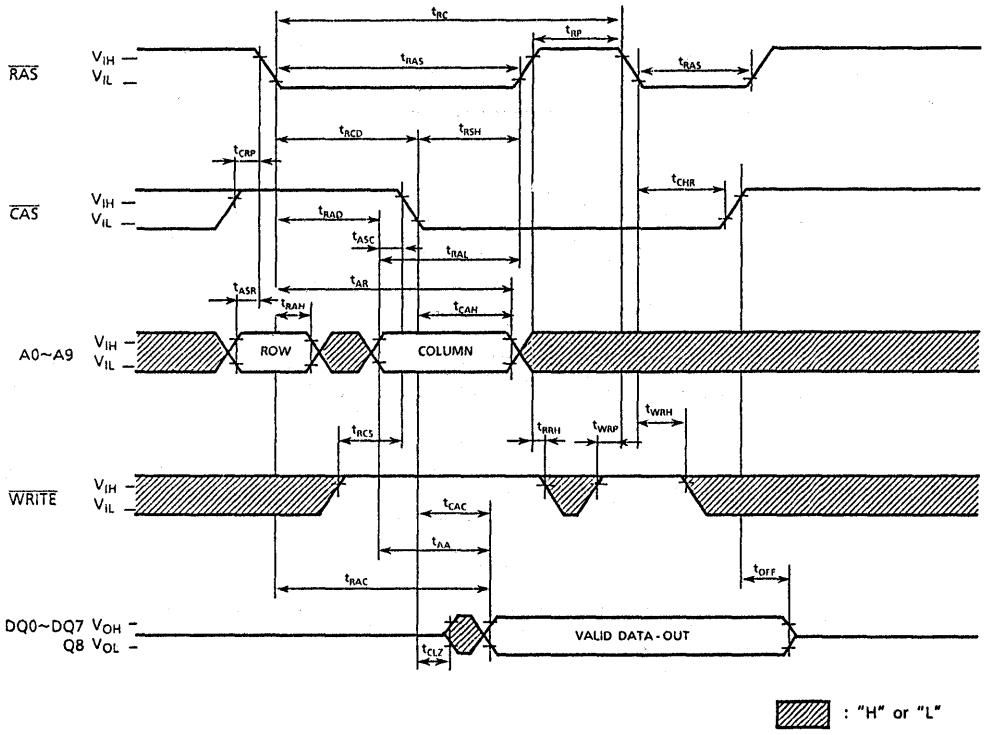
: "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

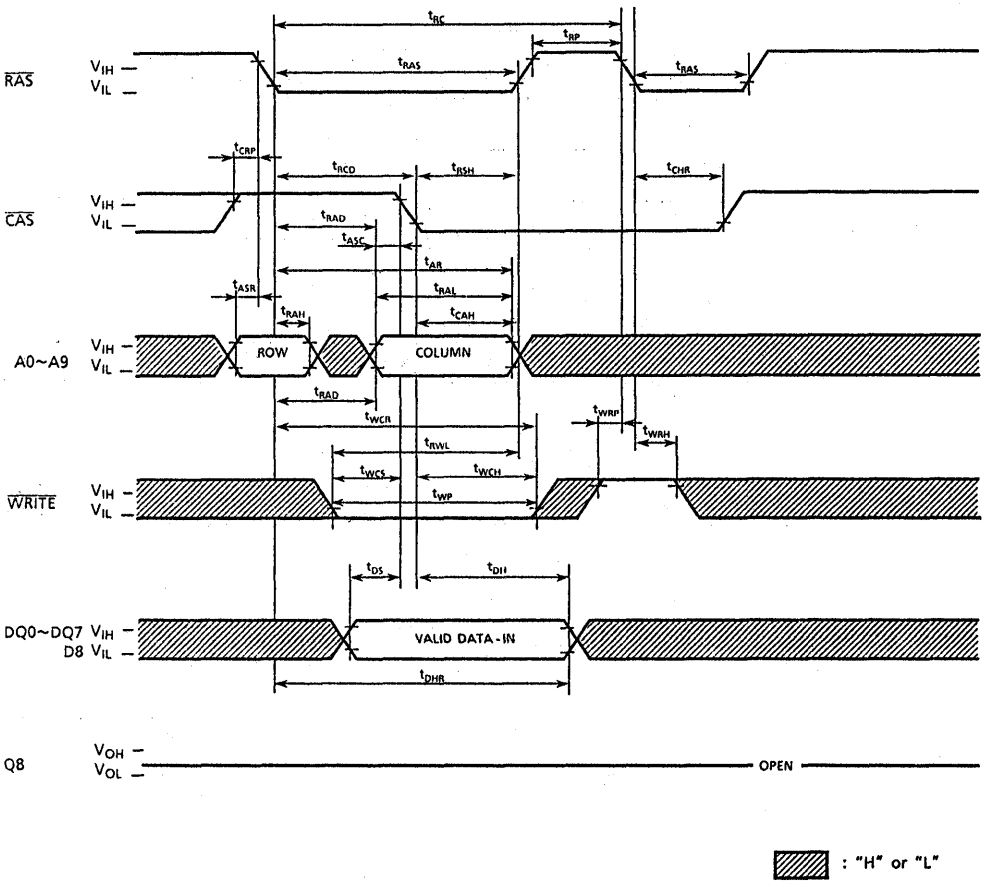


Note: A0~A9 = "H" or "L"

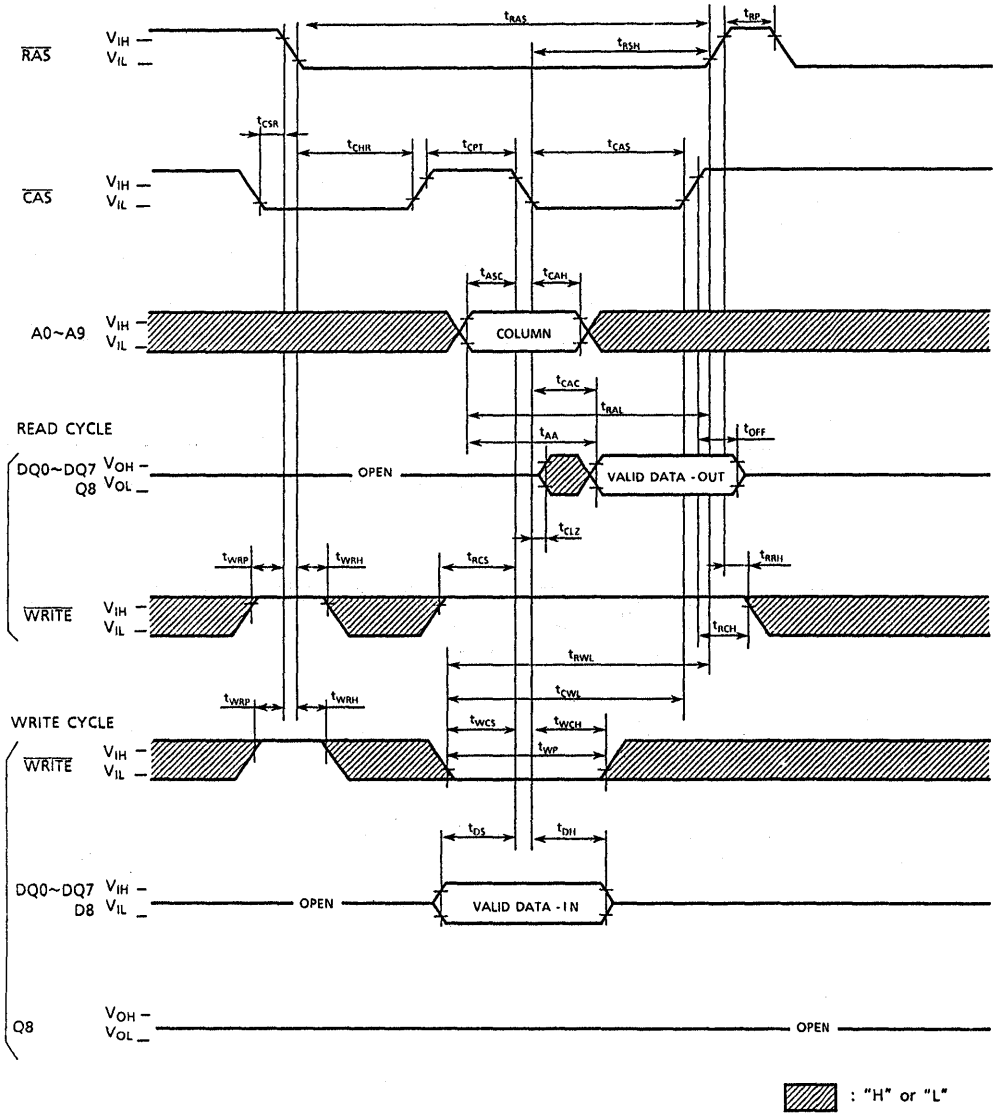
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



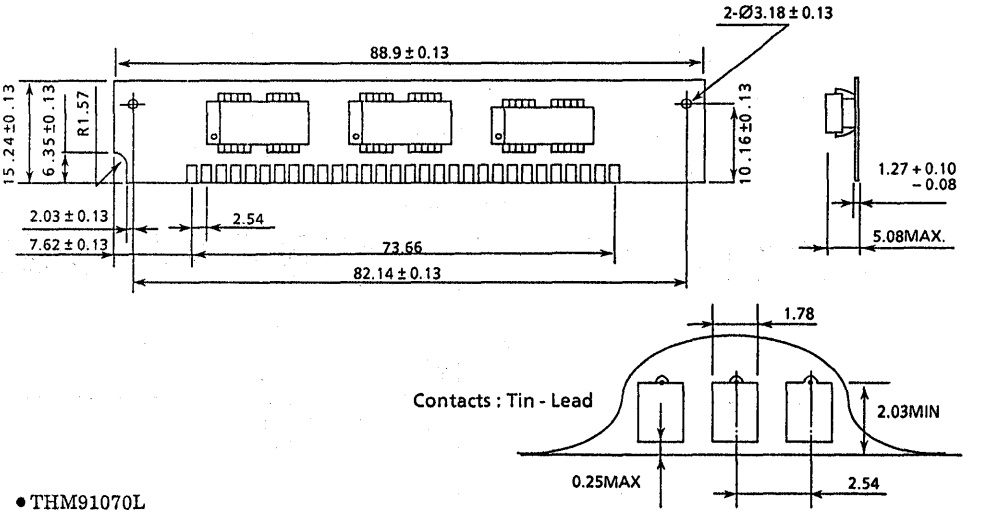
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



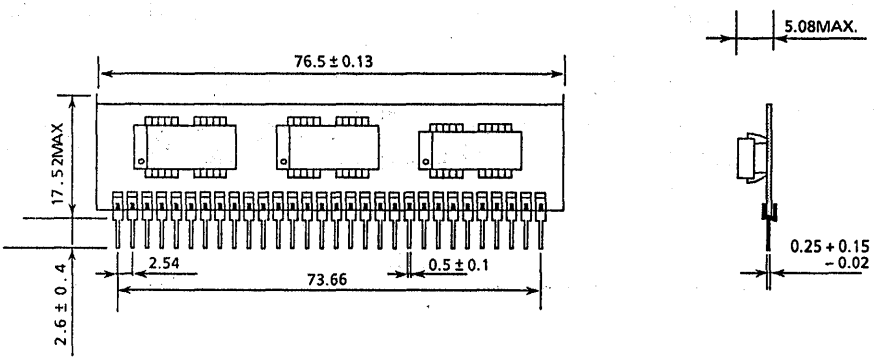
OUTLINE DRAWINGS

Unit in mm

• THM91070S



• THM91070L



1,048,576 WORDS×9 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM91070AS/AL and THM91070AS/AL are a 1,048,576 words by 9 bits dynamic RAM module which assembled 2 pcs of TC514400ASJ and 1 pcs of TC511000AJ/BJ on the printed circuit board. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

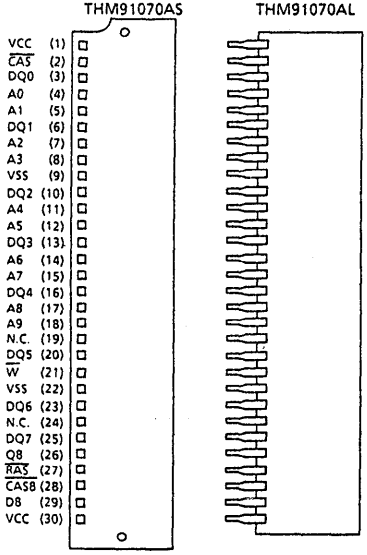
FEATURES

- 1,048,576 words by 9 bits organization
- Fast access time and cycle time

	-60	-70	-80	-10
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC} Cycle Time	110ns	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns	60ns

- Low Power
  1,815mW MAX. Operating (THMxxxxxx−60)
  1,540mW MAX. Operating (THMxxxxxx−70)
  1,320mW MAX. Operating (THMxxxxxx−80)
  1,155mW MAX. Operating (THMxxxxxx−10)
  16.5mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 1,024 refresh cycles/ 8ms(Burst Refresh)
- 1,024 refresh cycles/16ms(DistributedRefresh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package THM91070AS-xx : Tin-Lend Contact
  THM91070AL-xx : 30Pin SIP

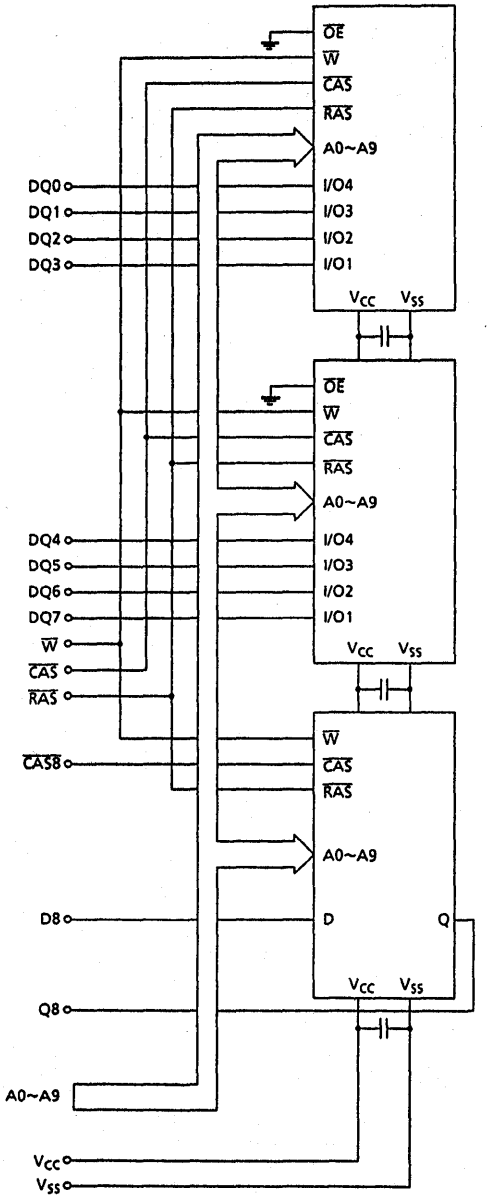
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A9	Address Inputs
DQ0~DQ7	Data Inputs/Outputs
D8	Data Inputs
Q8	Data Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{CAS8}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	2.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	330	mA	3, 4 5
		THMxxxxxx-70	–	280		
		THMxxxxxx-80	–	240		
		THMxxxxxx-10	–	210		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	6	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	330	mA	3,5
		THMxxxxxx-70	–	280		
		THMxxxxxx-80	–	240		
		THMxxxxxx-10	–	210		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx-60	–	200	mA	3, 4 5
		THMxxxxxx-70	–	200		
		THMxxxxxx-80	–	170		
		THMxxxxxx-10	–	150		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	3	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	330	mA	3,5
		THMxxxxxx-70	–	280		
		THMxxxxxx-80	–	240		
		THMxxxxxx-10	–	210		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 30	30	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	45	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,13
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,13
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,14
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	40	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	13
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	14
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	16	–	16	–	16	–	16	ms	
t_{WCS}	Write Command Set-UP Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	
t_{WRP}	$\overline{WRITE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	10	–	ns	
t_{WRH}	$\overline{WRITE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	10	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

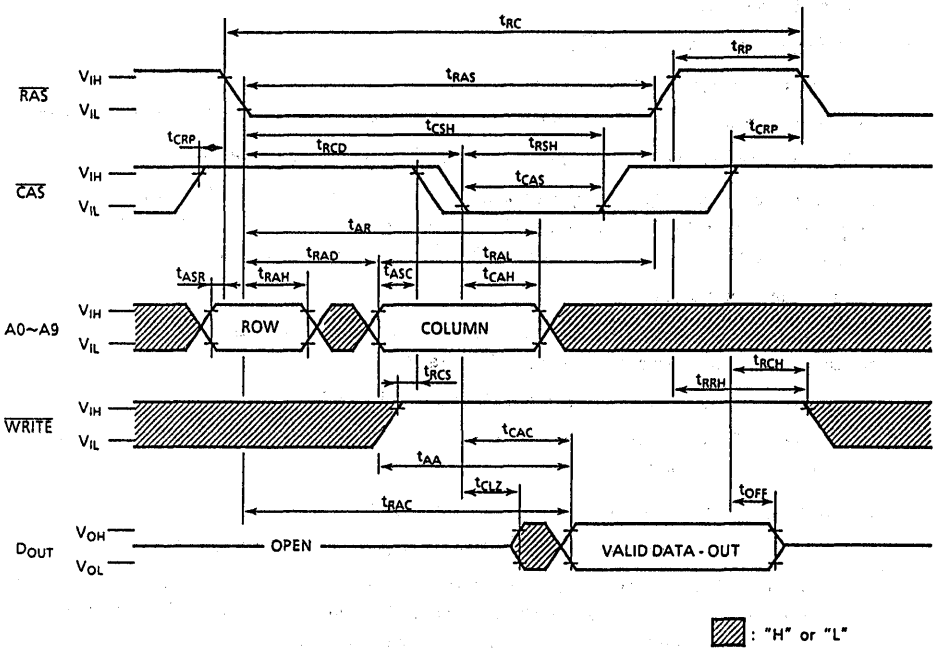
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0~A9, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$)	–	30	pF
C_{I2}	Input Capacitance (D8, $\overline{CAS8}$)	–	10	pF
C_{DQ}	I/O Capacitance (DQ0~DQ7)	–	15	pF
C_Q	Output Capacitance (Q8)	–	10	pF

NOTES:

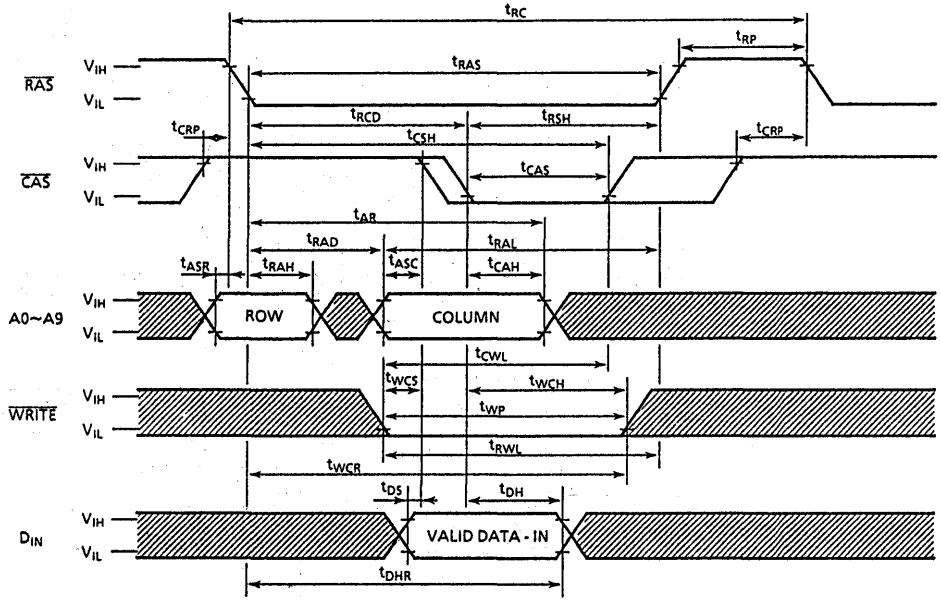
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less While $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
13. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throughout the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

READ CYCLE

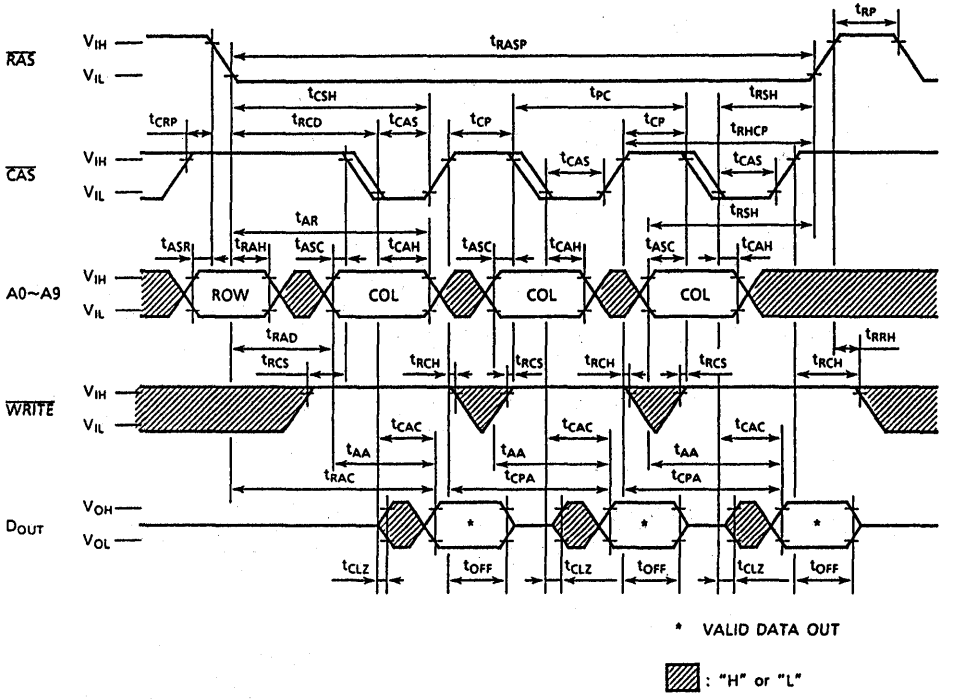


WRITE CYCLE (EARLY WRITE)

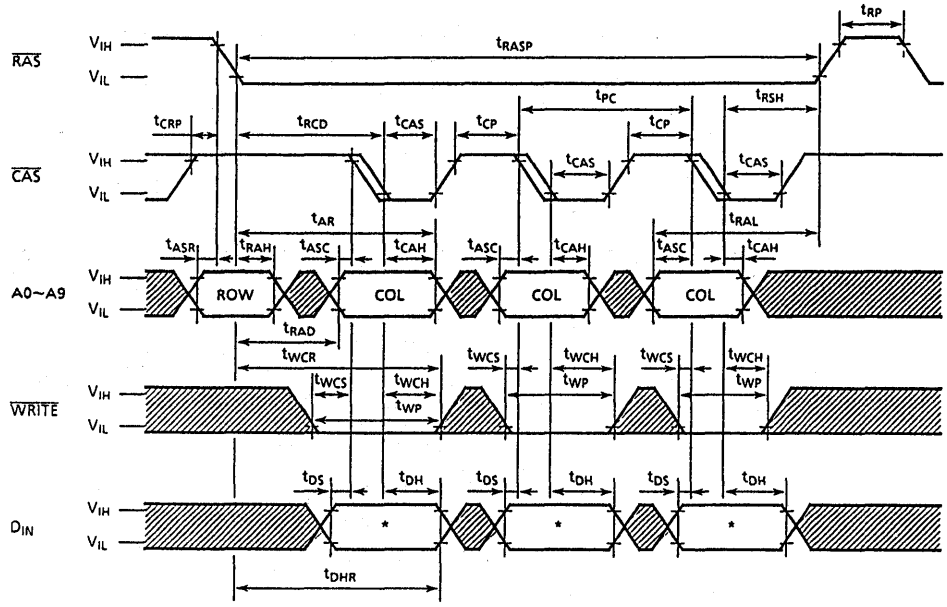


: "H" or "L"

FAST PAGE MODE READ CYCLE



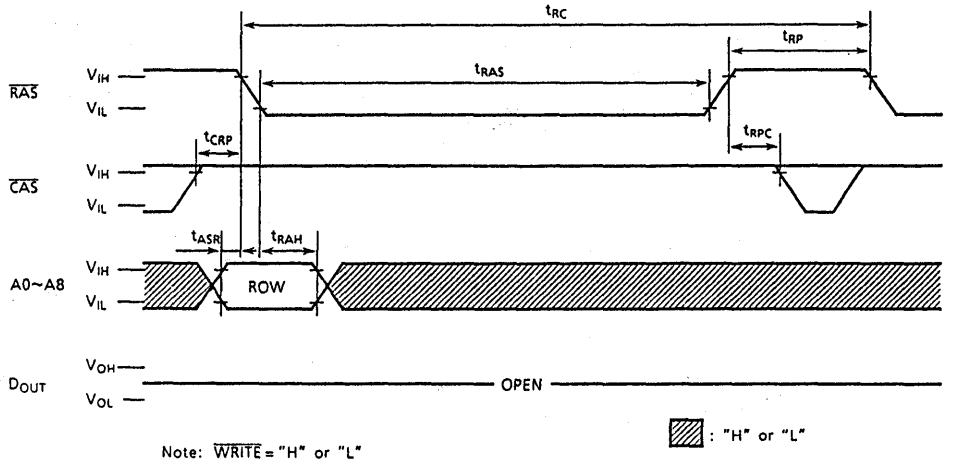
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

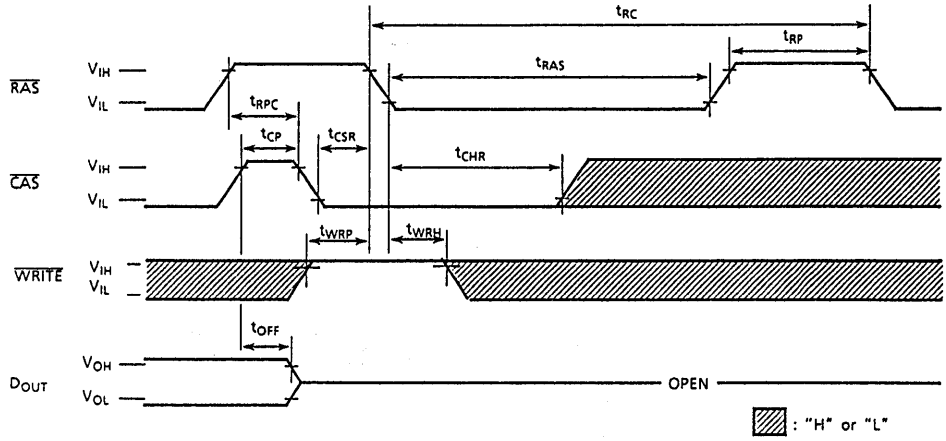
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



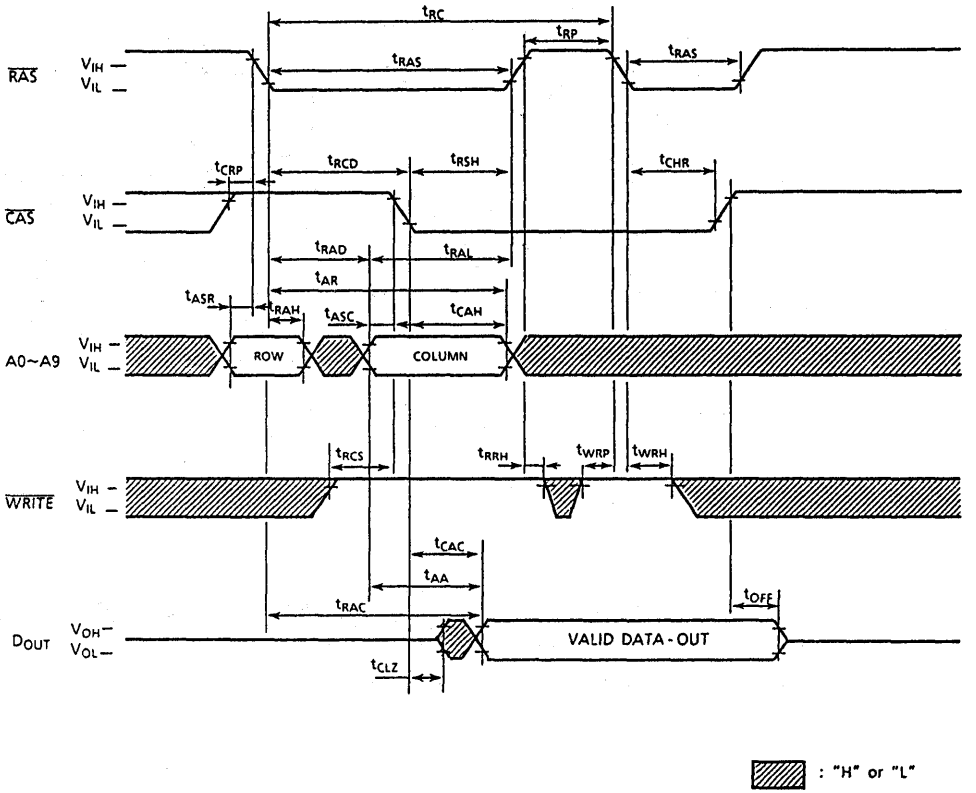
Note: $\overline{WRITE}$ = "H" or "L"

CAS BEFORE RAS REFRESH CYCLE

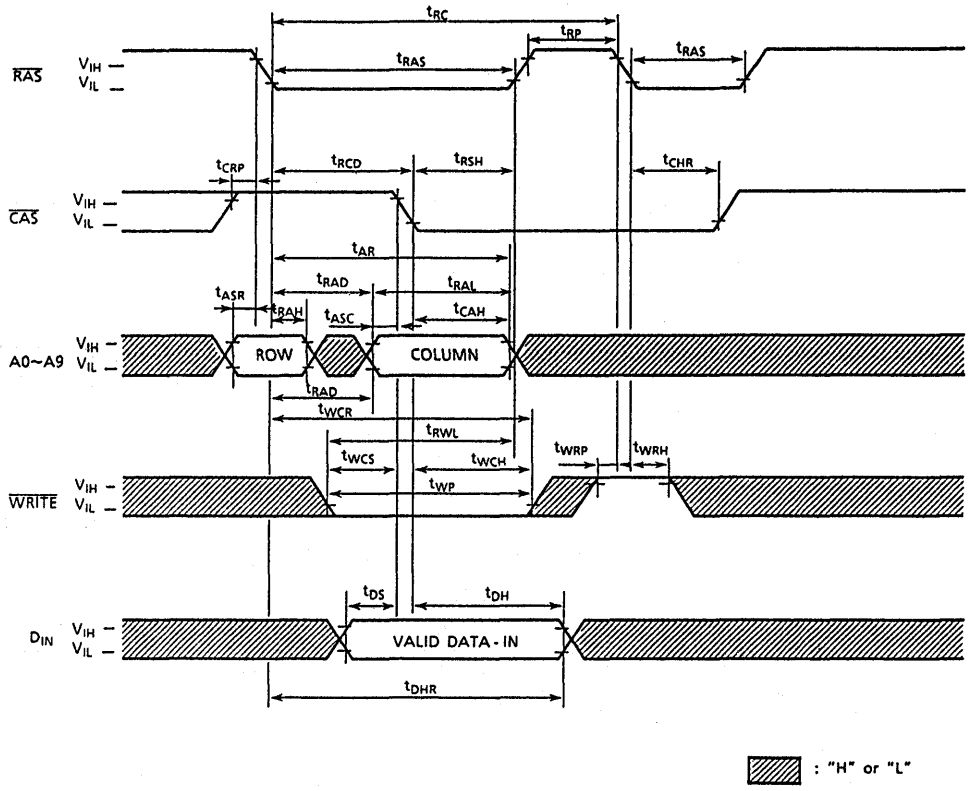


Note: A0~A9 = "H" or "L"

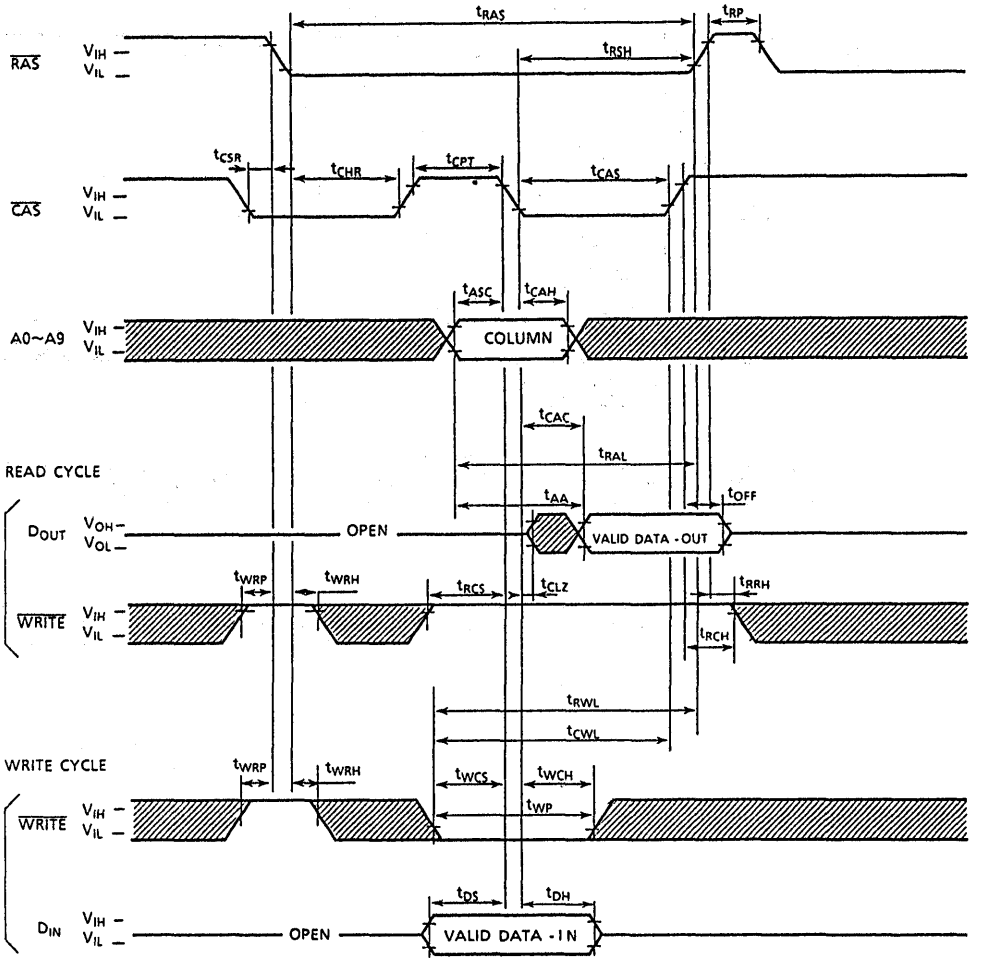
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



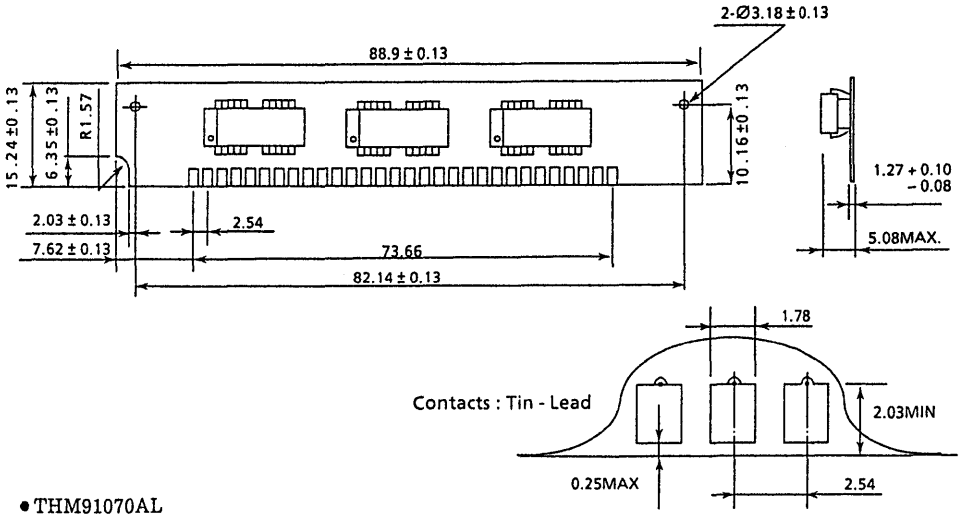
: "H" or "L"

OUTLINE DRAWINGS

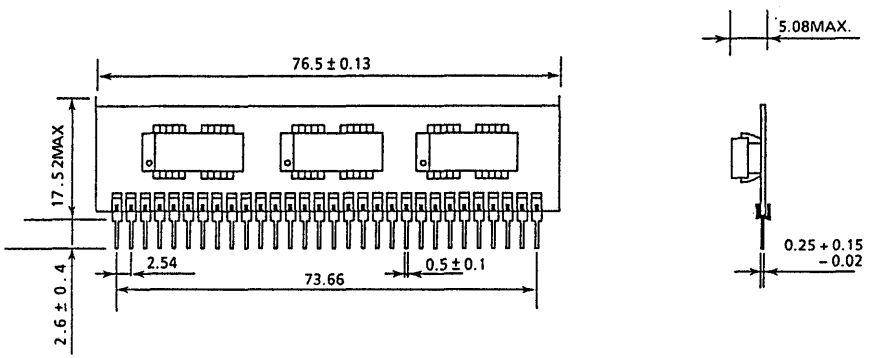
THM91070AS/AL

Unit in mm

• THM91070AS



• THM91070AL



NOTES

262,144 WORDS×36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM362500BS/BSG/AS/ASG is a 262,144 words by 36 bits dynamic RAM module which assembled 8 pcs of TC514256AJ/BJ and 4 pcs of TC51256T on the printed circuit board. These modules can be as well used as 524,288 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

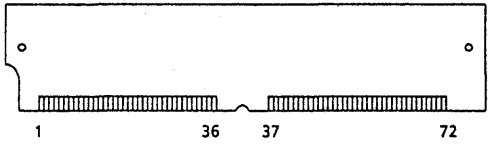
FEATURES

- 262,144 words by 36 bits organization
- Fast access time and cycle time

		-60	-70	-80	-10
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC}	Cycle Time	115ns	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns	45ns	55ns

- Low Power
  5,940mW MAX. Operating (THMxxxxxx-60)
  5,280mW MAX. Operating (THMxxxxxx-70)
  4,620mW MAX. Operating (THMxxxxxx-80)
  3,960mW MAX. Operating (THMxxxxxx-10)
  66mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 512 refresh cycles/4ms(Burst Refresh)
- 512 refresh cycles/8ms(Distributed Refresh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package THM362500BS - 60 : Tin - Lead Contact
  THM362500AS - 70,80,10 : Tin - Lead Contact
  THM362500BSG - 60 : Gold Contact
  THM362500ASG - 70,80,10 : Gold Contact

PIN CONNECTION (TOP VIEW)



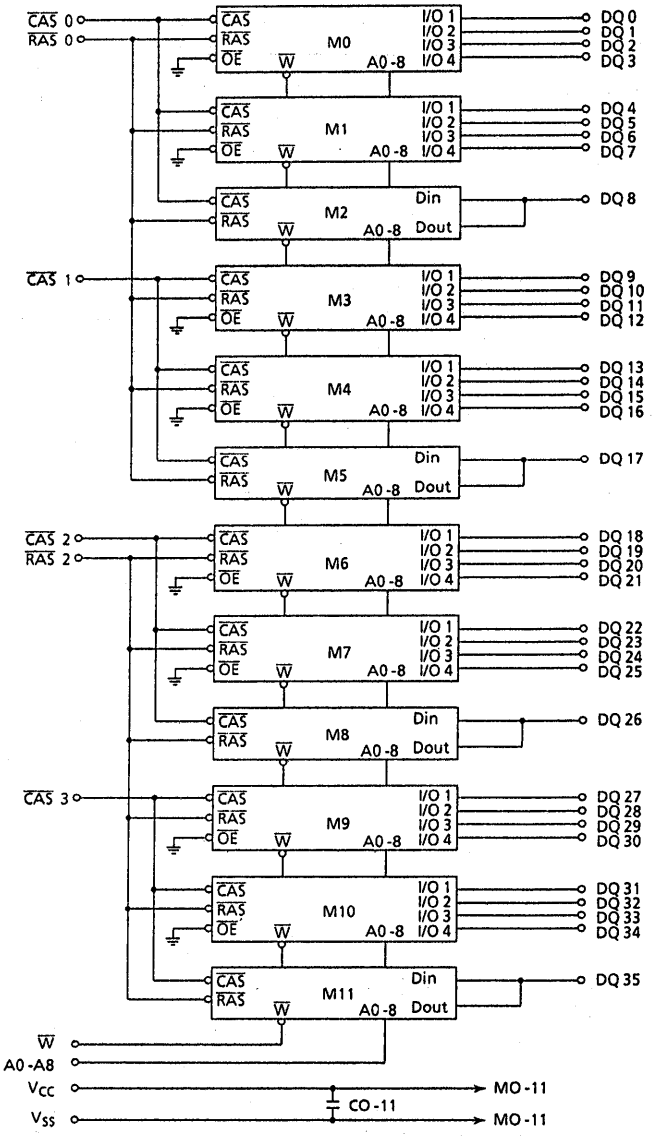
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

	-60	-70	-80	-10
PD0	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD1	NC	NC	NC	NC
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	7.2	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	1080	mA	3, 4 5
		THMxxxxxx-70	–	960		
		THMxxxxxx-80	–	840		
		THMxxxxxx-10	–	720		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	24	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} \geq t_{RC}$ MIN.)	THMxxxxxx-60	–	1080	mA	3,5
		THMxxxxxx-70	–	960		
		THMxxxxxx-80	–	840		
		THMxxxxxx-10	–	720		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx-60	–	720	mA	3, 4 5
		THMxxxxxx-70	–	720		
		THMxxxxxx-80	–	600		
		THMxxxxxx-10	–	480		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	12	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	1080	mA	3,5
		THMxxxxxx-70	–	960		
		THMxxxxxx-80	–	840		
		THMxxxxxx-10	–	720		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 120	120	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

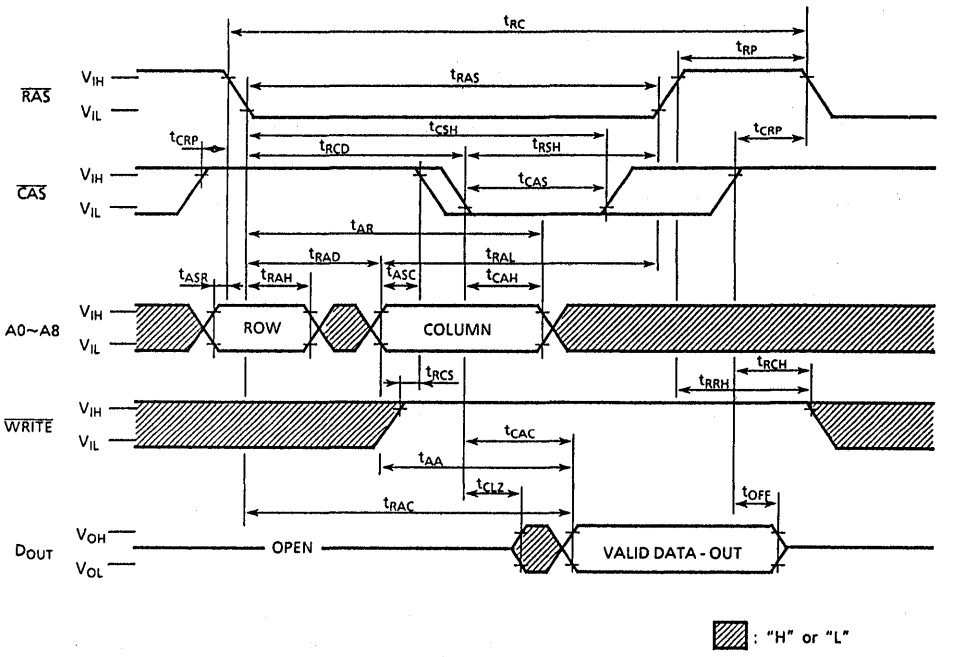
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A8)	–	88	pF
CI2	Input Capacitance ($\overline{W}$)	–	84	pF
CI3	Input Capacitance ($\overline{RAS0}$,$\overline{RAS2}$)	–	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	36	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	–	17	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	–	22	pF

NOTES:

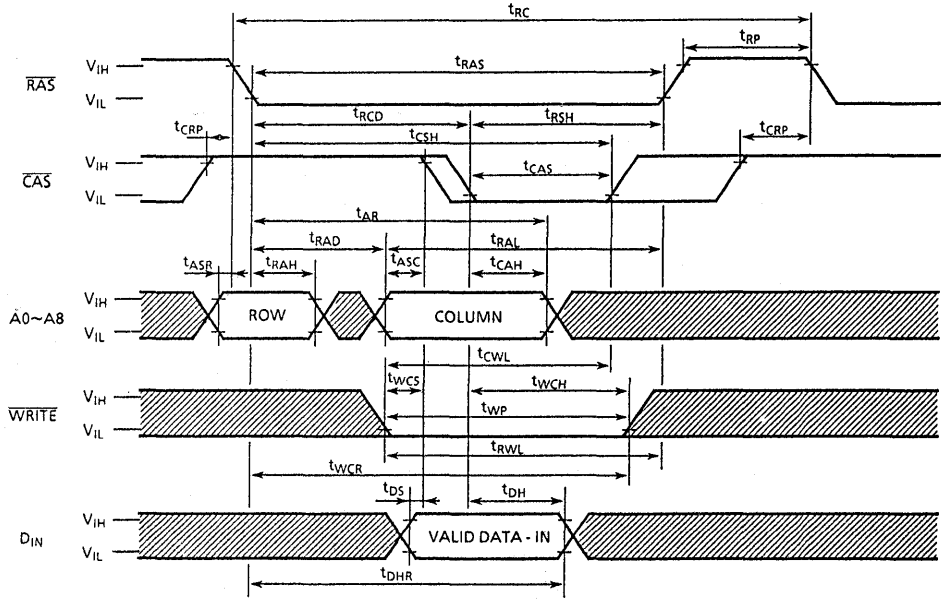
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

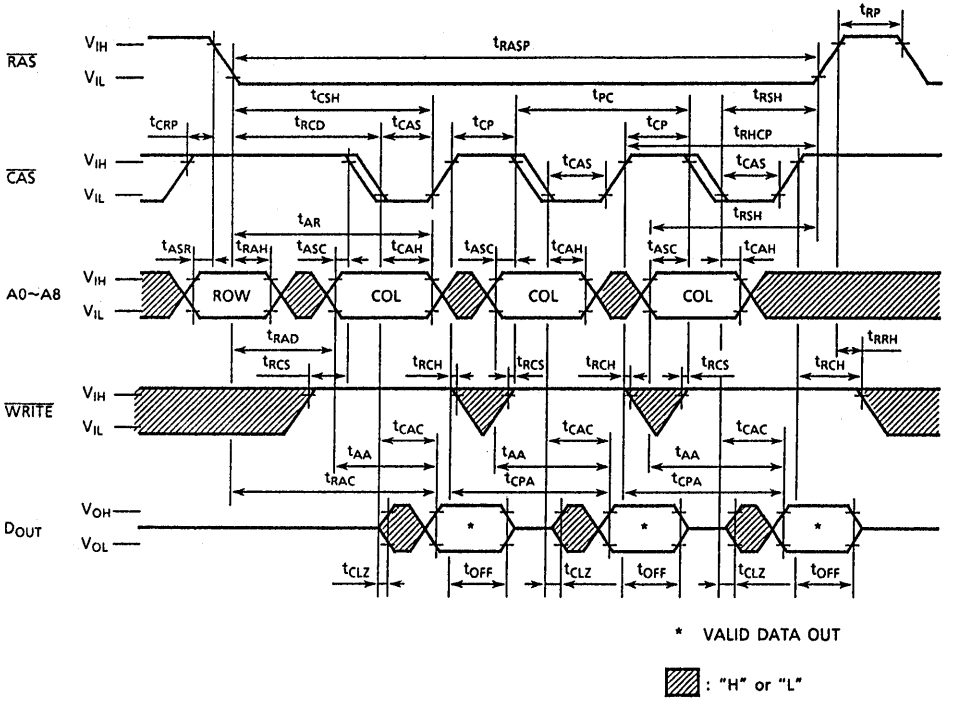
READ CYCLE



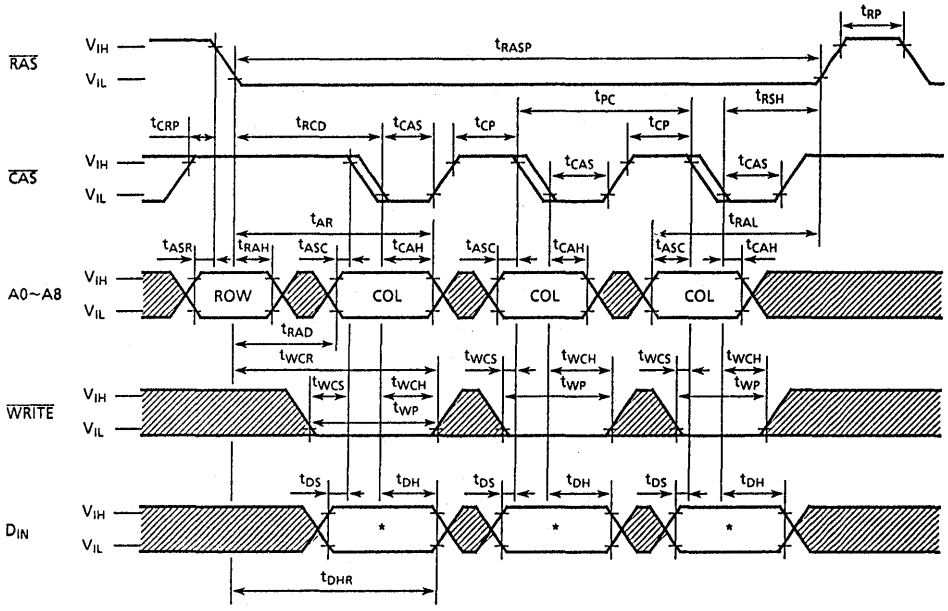
WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ CYCLE



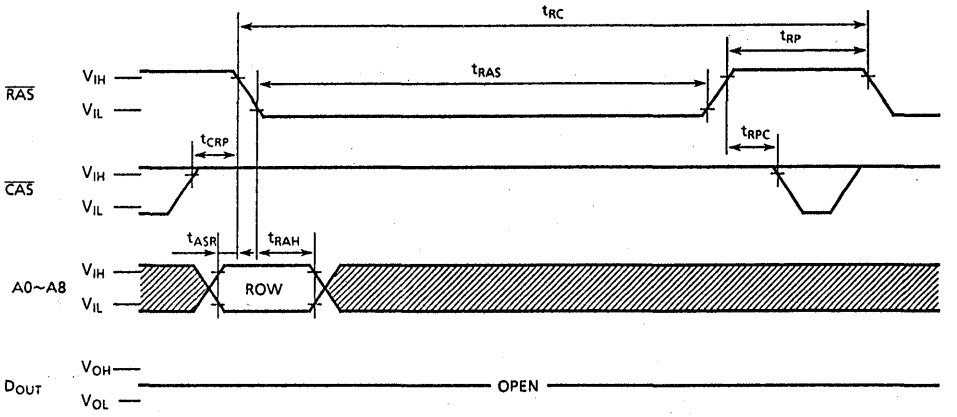
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

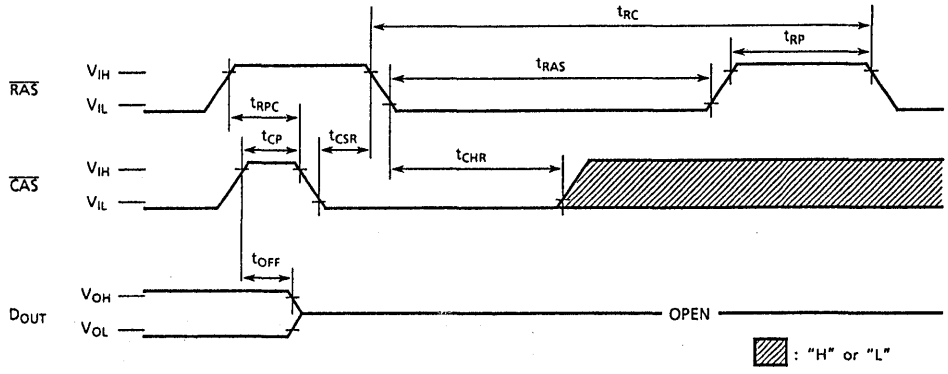
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



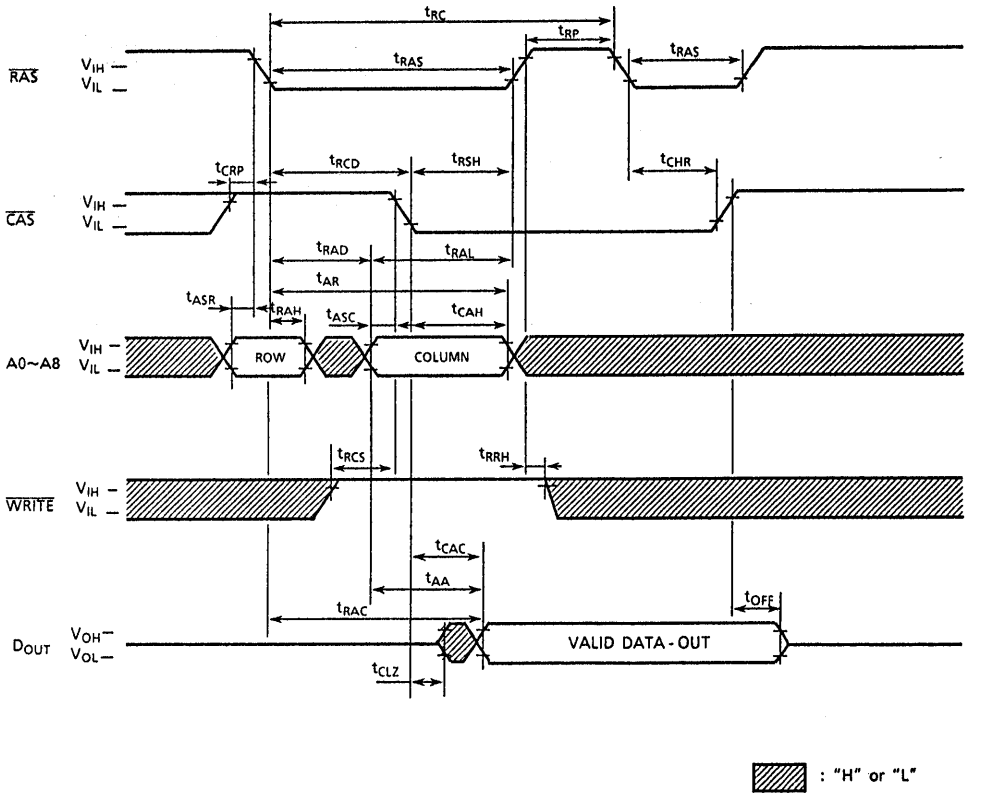
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

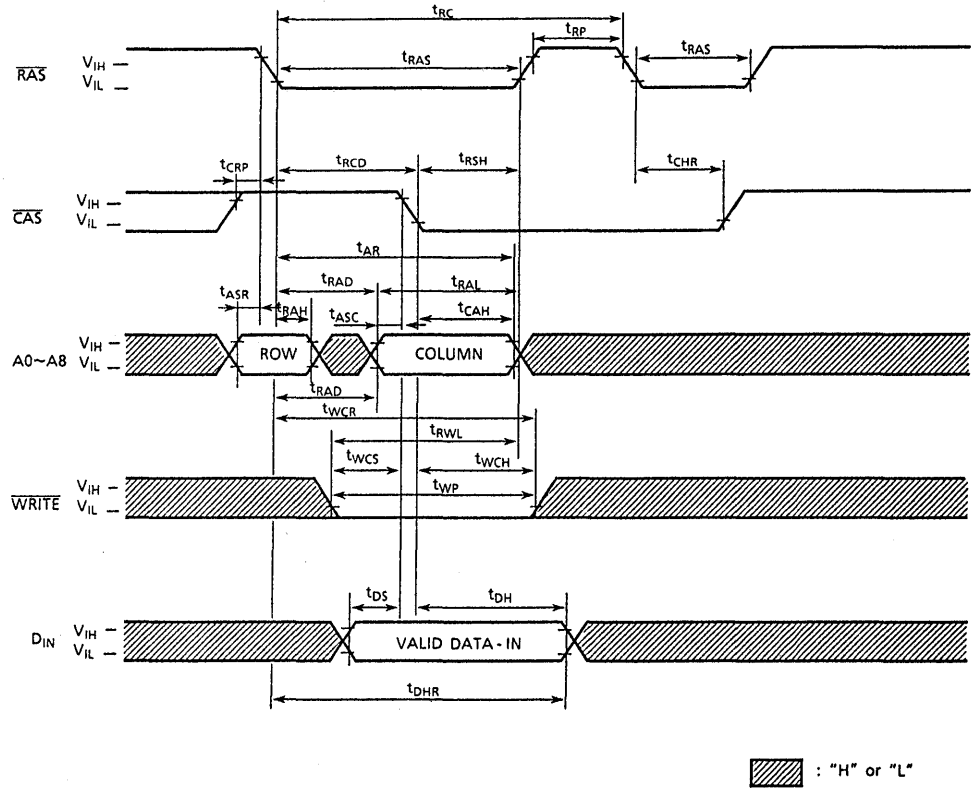


Note: A0~A8, $\overline{WRITE}$ = "H" or "L"

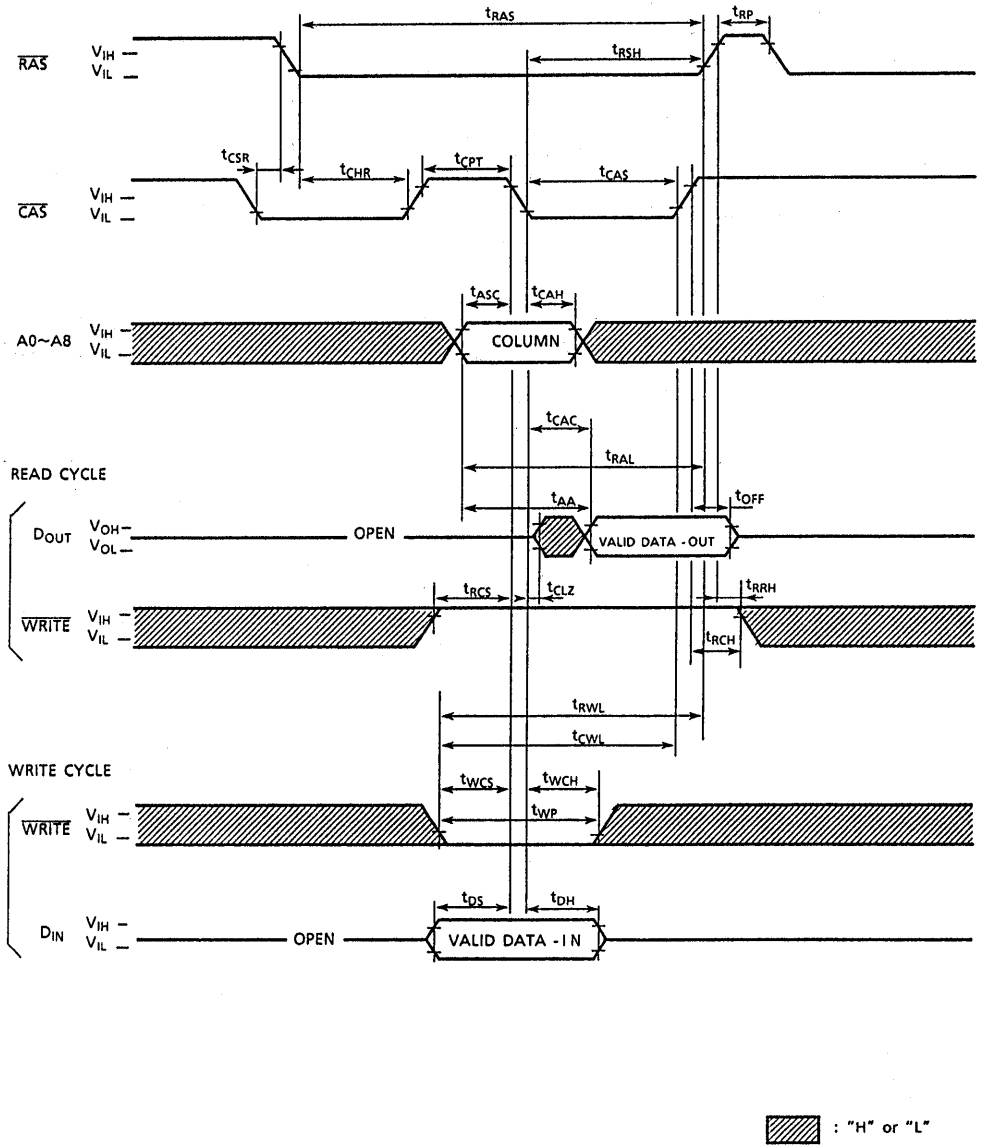
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

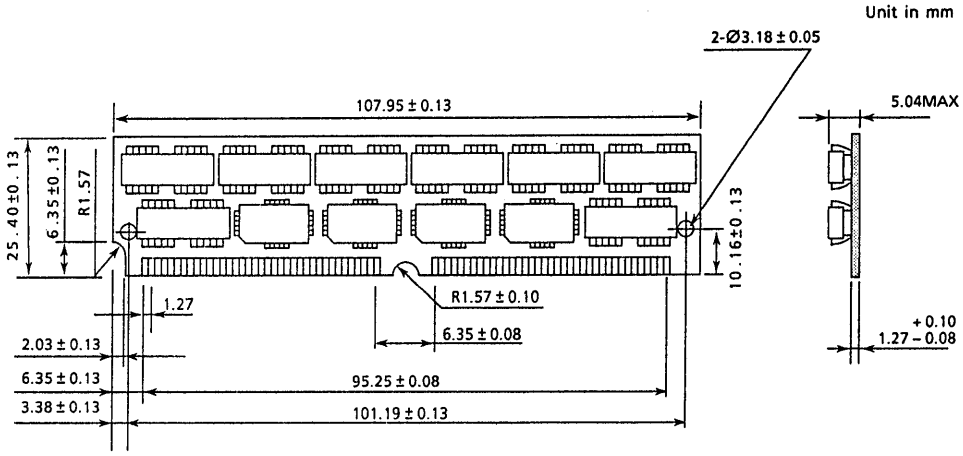


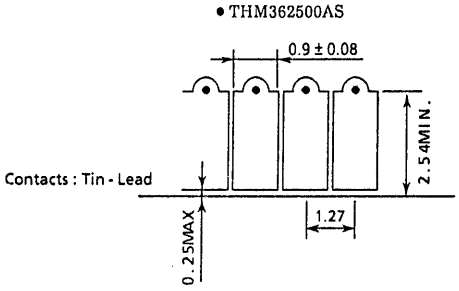
: "H" or "L"

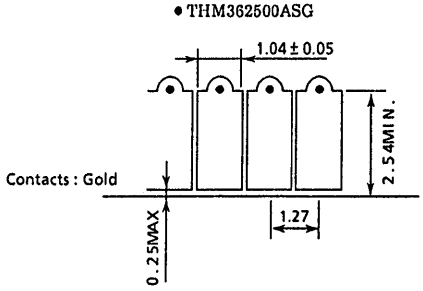
OUTLINE DRAWINGS

THM362500AS/ASG

Unit in mm







NOTES

262,144 WORDS×40 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM402500ASG/BSG isa 262,144 words by 40 bits dynamic RAM module which assembled 10 pcs of TC514256AJ/BJ on the printed circuit board.

The THM402500ASG/BSG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

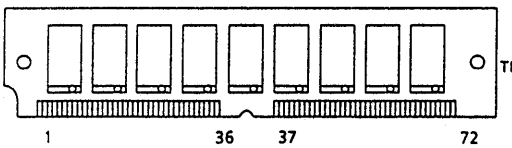
FEATURES

- 262,144 words by 40 bits organization

		-60	-70	-80	-10
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC}	Cycle Time	110ns	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	45ns	45ns	50ns	60ns

- Low power
  - 4,950mW MAX. Operating (THMxxxxxx-60)
  - 4,440mW MAX. Operating (THMxxxxxx-70)
  - 3,850mW MAX. Operating (THMxxxxxx-80)
  - 3,300mW MAX. Operating (THMxxxxxx-10)
  - 55mW MAX. Standby
- Read-Modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- 512 Refresh cycles / 8ms
- Fast access time and cycle time
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Gold Contact
- JEDEC OUTLILNE : THM402500BSG - 60, ASG - 70, 80, 10

PIN CONNECTION (TOP VIEW)



THM402500ASG/BSG

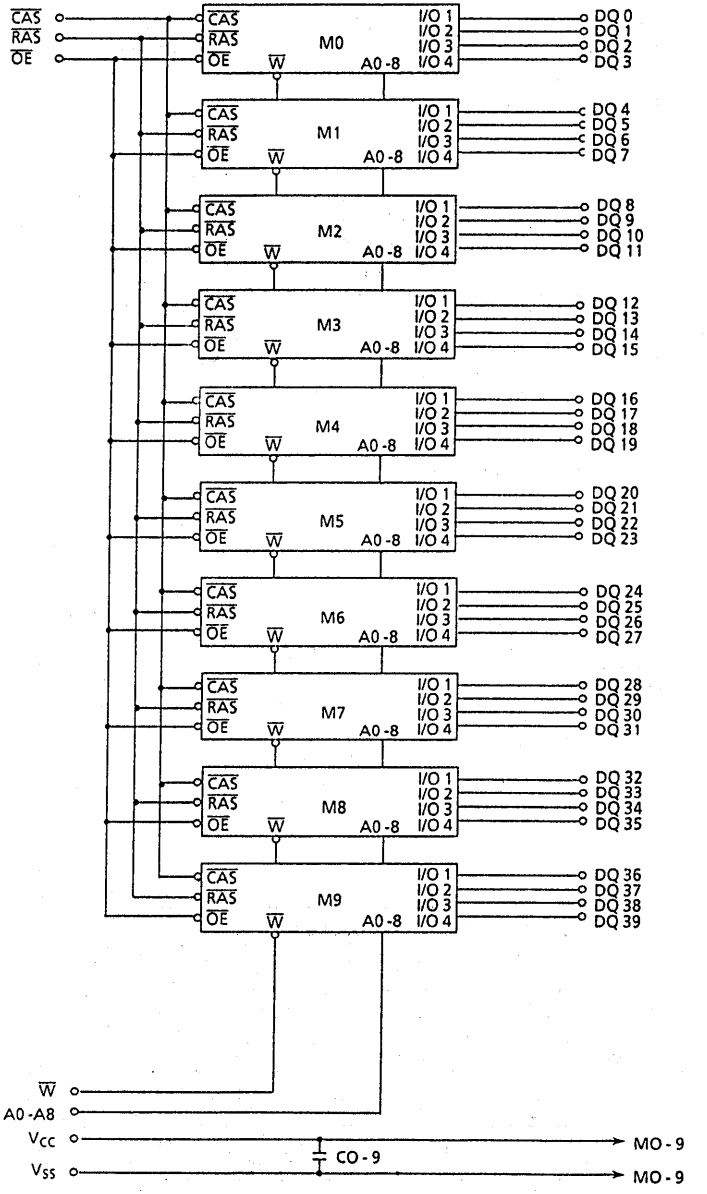
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
$\overline{CAS}$	Column Address Strobe
$\overline{RAS}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	NC	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	NC	44	$\overline{RAS}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	NC	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

	-60	-70	-80	-10
PD0	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD1	NC	NC	NC	NC
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	6.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	900	mA	3, 4 5
		THMxxxxxx-70	–	800		
		THMxxxxxx-80	–	700		
		THMxxxxxx-10	–	600		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	20	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	900	mA	3,5
		THMxxxxxx-70	–	800		
		THMxxxxxx-80	–	700		
		THMxxxxxx-10	–	600		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxxx-60	–	600	mA	3, 4 5
		THMxxxxxx-70	–	600		
		THMxxxxxx-80	–	500		
		THMxxxxxx-10	–	400		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	10	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	900	mA	3,5
		THMxxxxxx-70	–	800		
		THMxxxxxx-80	–	700		
		THMxxxxxx-10	–	600		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≦ V_{IN} ≦ 6.5V, All Other Pins Not Under Test = 0V)		– 100	100	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	95	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	25	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	0	–	0	–	ns	

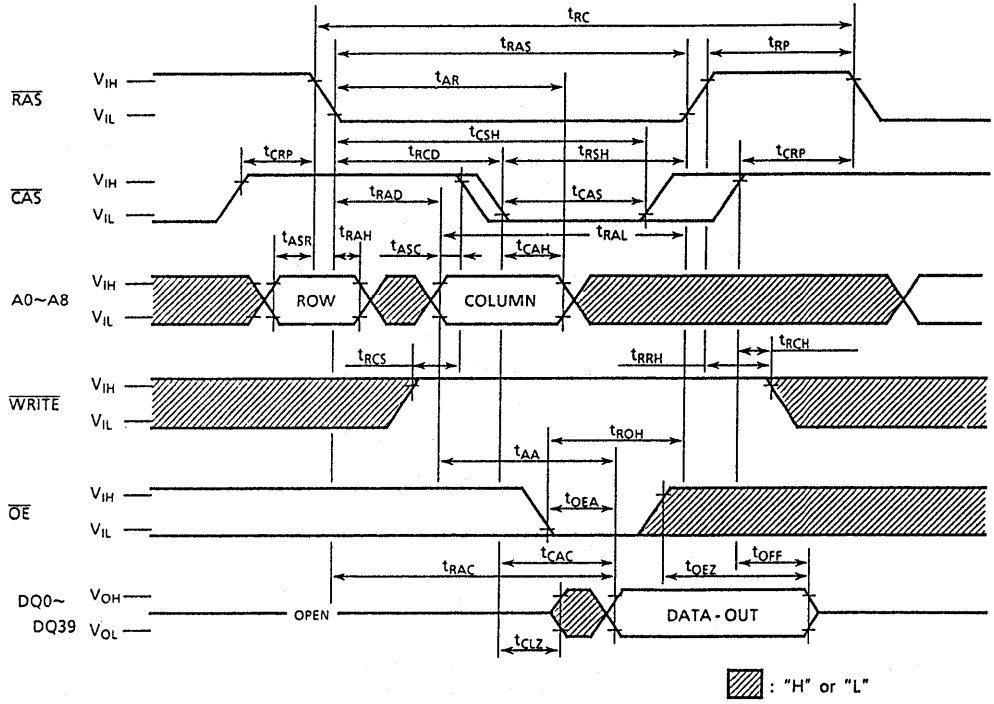
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	80	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	70	pF
CI3	Input Capacitance ($\overline{RAS}$)	-	60	pF
CI4	Input Capacitance ($\overline{CAS}$)	-	50	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	15	pF

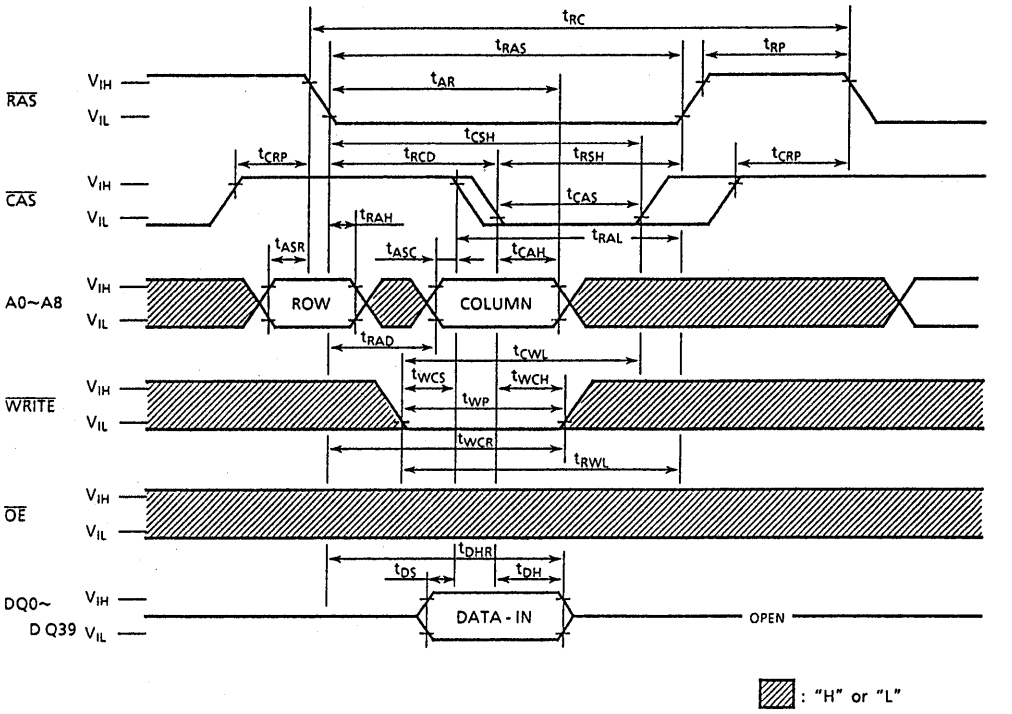
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

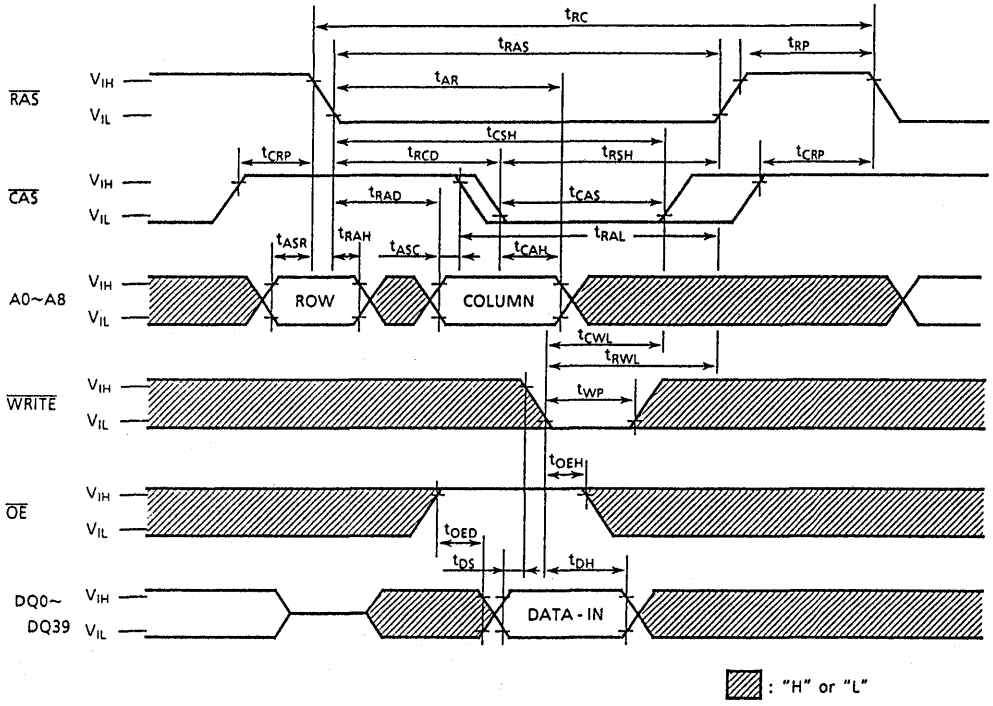
READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tROH
tAA
OE
tOEA
tCAC
tOFF
tRAC
tOEZ
DQ0~
DQ39
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

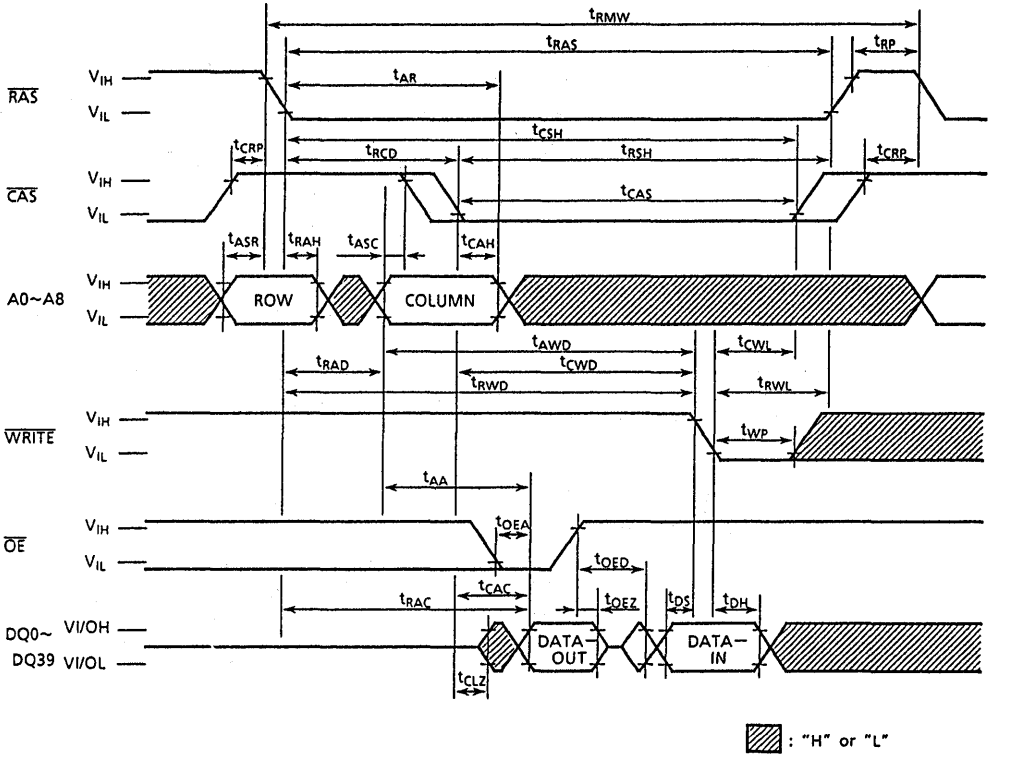
WRITE CYCLE (EARLY WRITE)



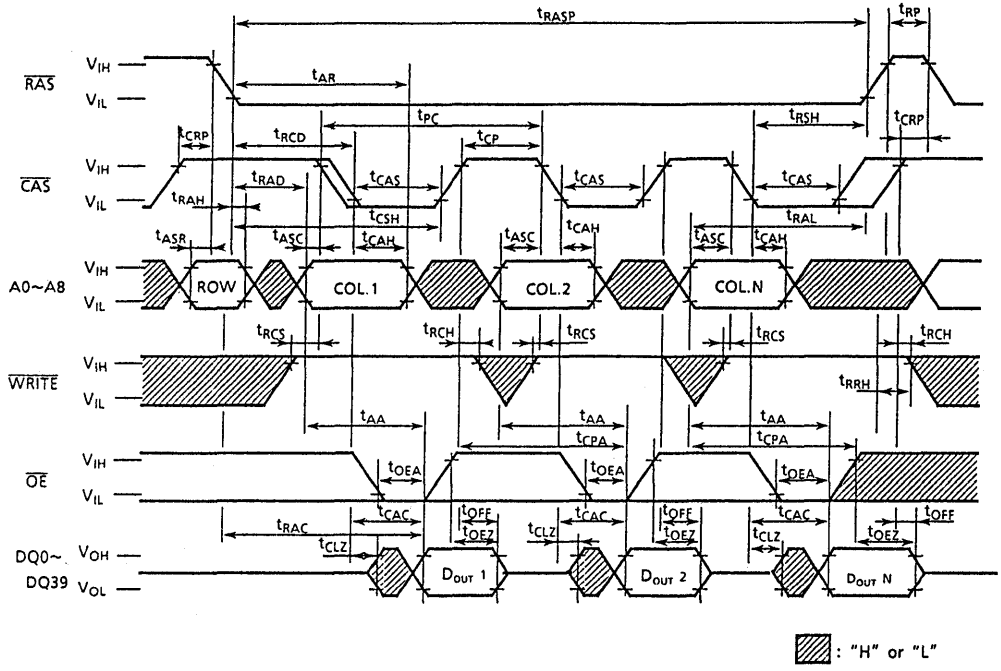
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



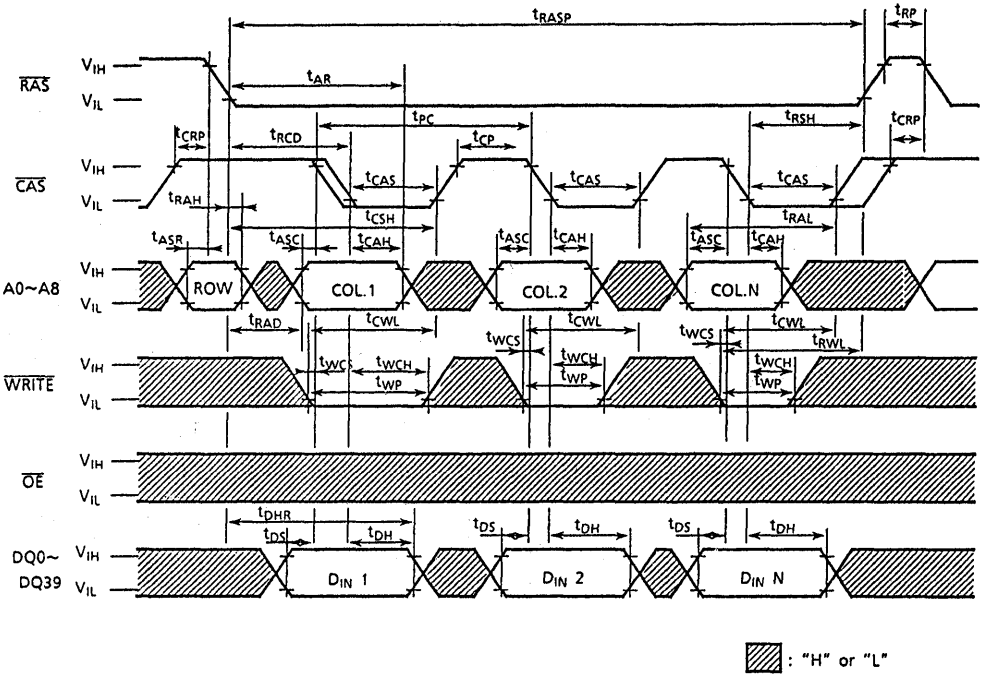
READ-MODIFY-WRITE CYCLE



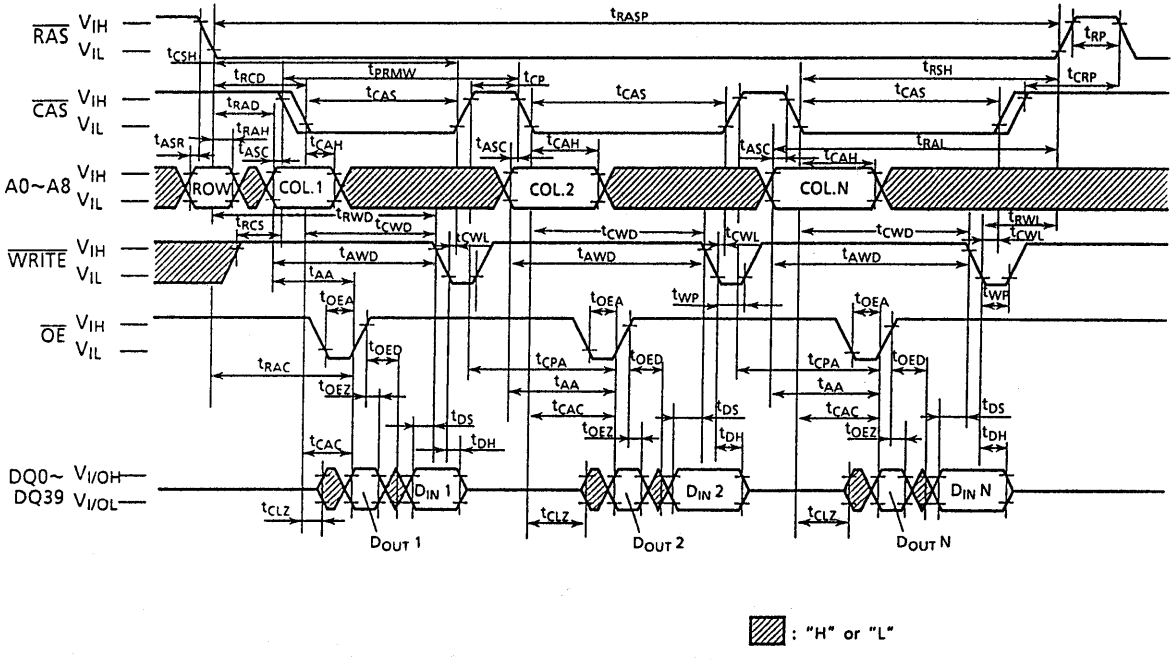
FAST PAGE MODE READ CYCLE



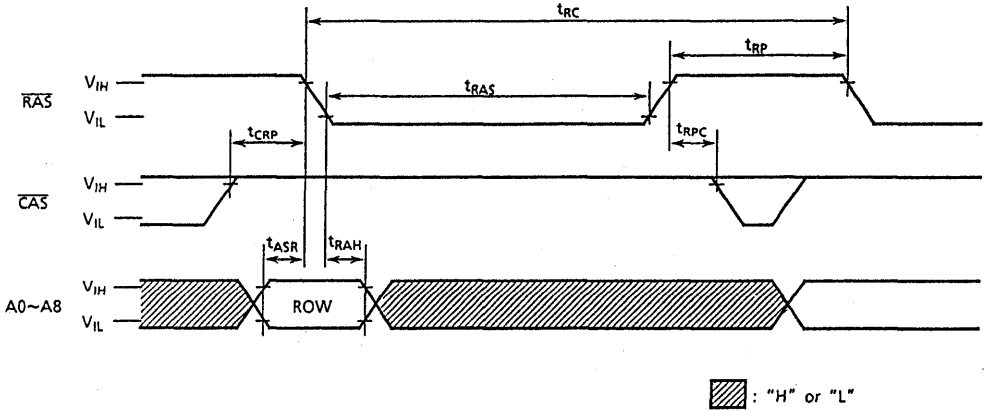
FAST PAGE MODE WRITE CYCLE



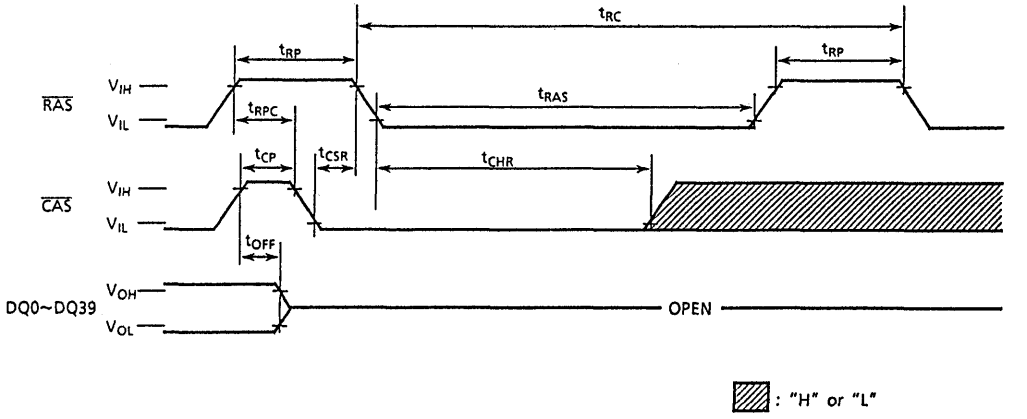
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



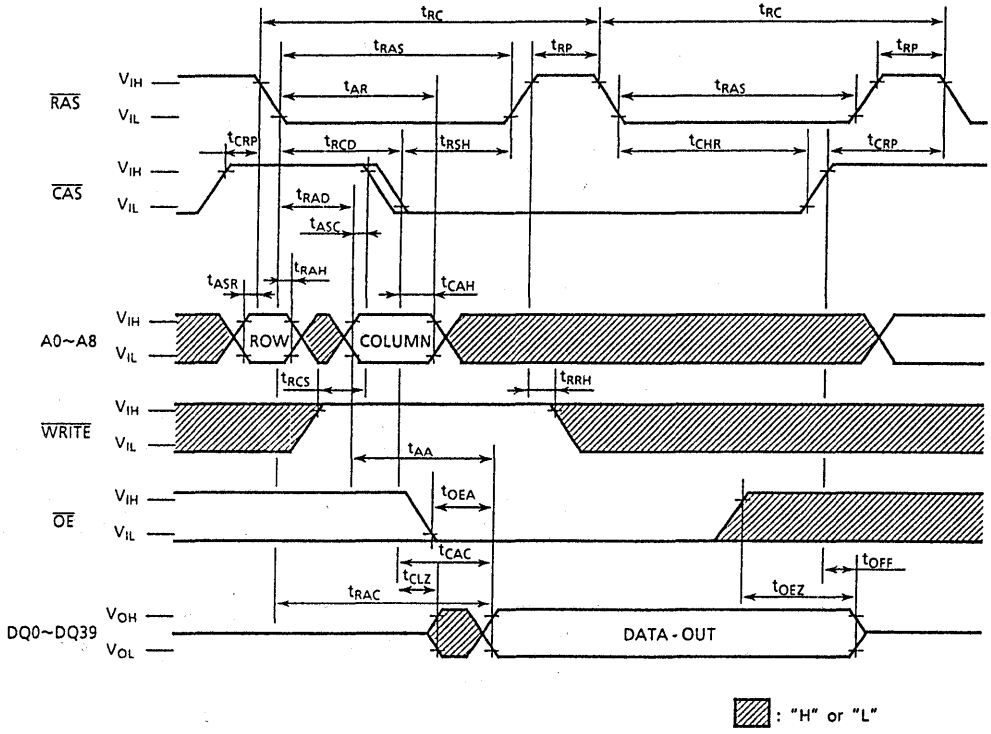
$\overline{RAS}$ ONLY REFRESH CYCLE



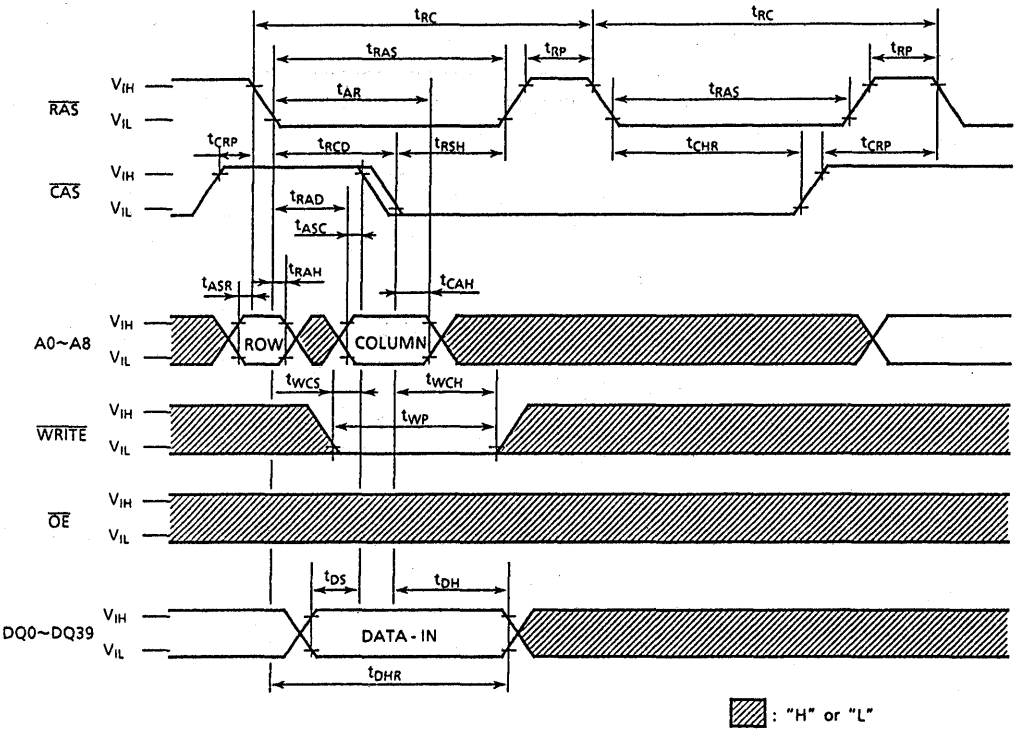
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



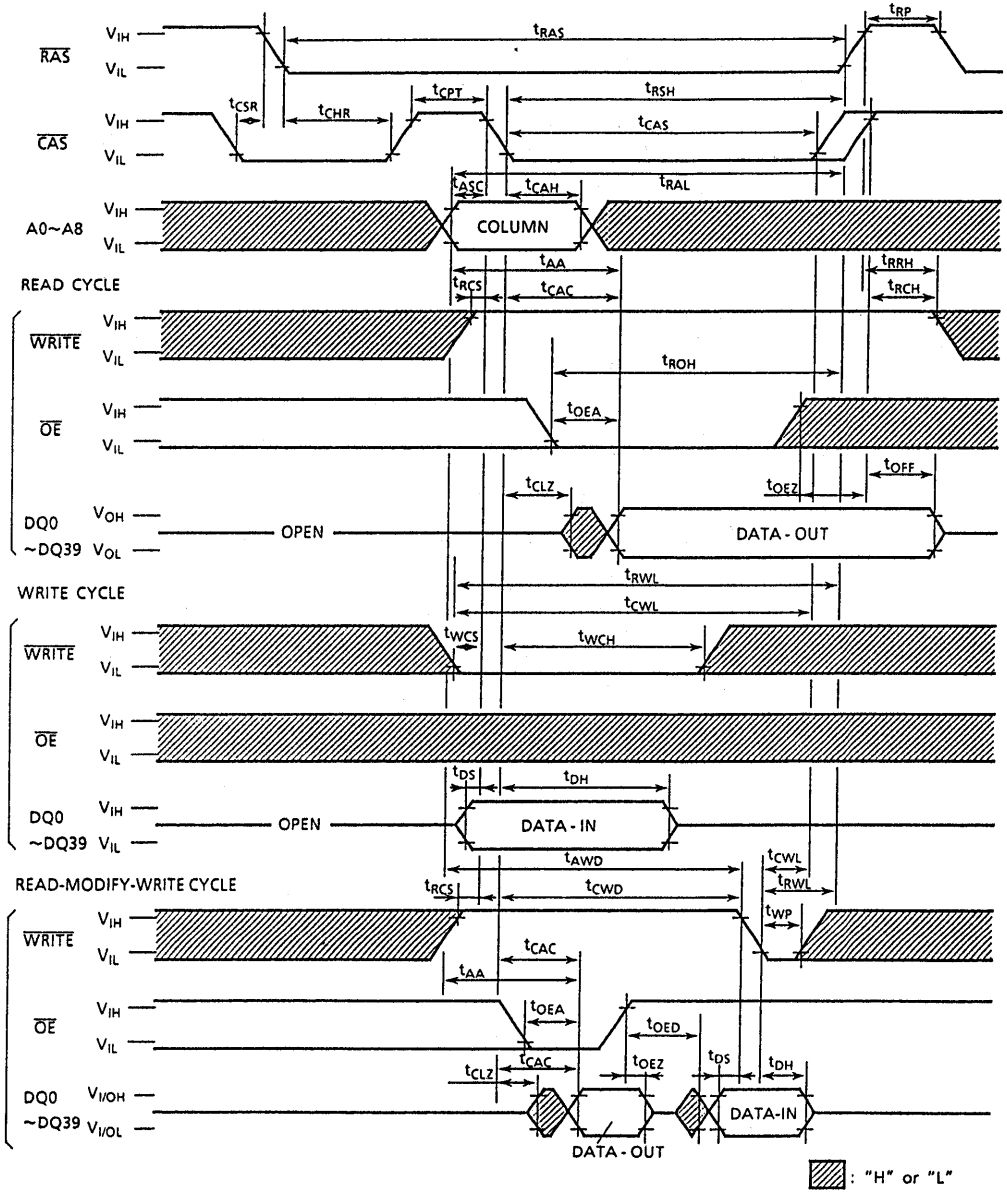
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



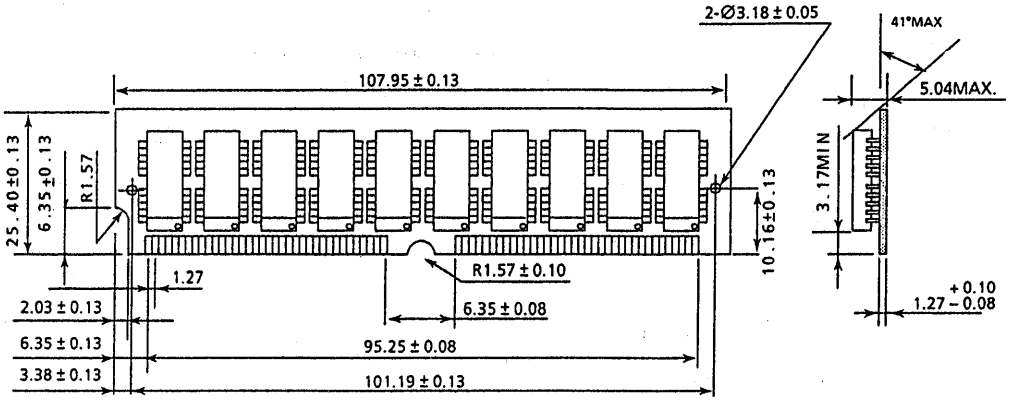
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

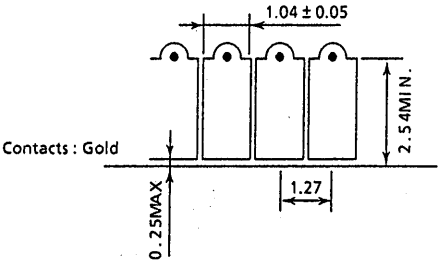


OUTLINE DRAWINGS

• THM402500ASG/BSG (JEDEC OUTLINE)

Unit in mm





524,288 WORDS × 32 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM325120BS/BSG/AS/ASG is a 524,288 words by 32 bits dynamic RAM module which assembled 16 pcs of TC514256AJ/BJ on the printed circuit board. These modules can be as well used as 1,048,576 words by 16 bits dynamic RAM module, by means of connecting DQ0 and DQ16, DQ1 and DQ17, DQ2 and DQ18, ·····, DQ15 and DQ31, respectively. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

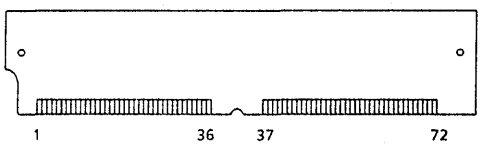
FEATURES

- 524,288 words by 32 bits organization
- Fast access time and cycle time

		-60	-70	-80	-10
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC}	Cycle Time	115ns	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns	45ns	55ns

- Low Power
  4,048mW MAX. Operating (THMxxxxxx−60)
  3,608mW MAX. Operating (THMxxxxxx−70)
  3,168mW MAX. Operating (THMxxxxxx−80)
  2,728mW MAX. Operating (THMxxxxxx−10)
  88mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 512 refresh cycles/8ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package
  THM325120BS - 60 : Tin - Lead Contact
  THM325120AS - 70,80,10 : Tin - Lead Contact
  THM325120BSG - 60 : Gold Contact
  THM325120ASG - 70,80,10 : Gold Contact

PIN CONNECTION (TOP VIEW)



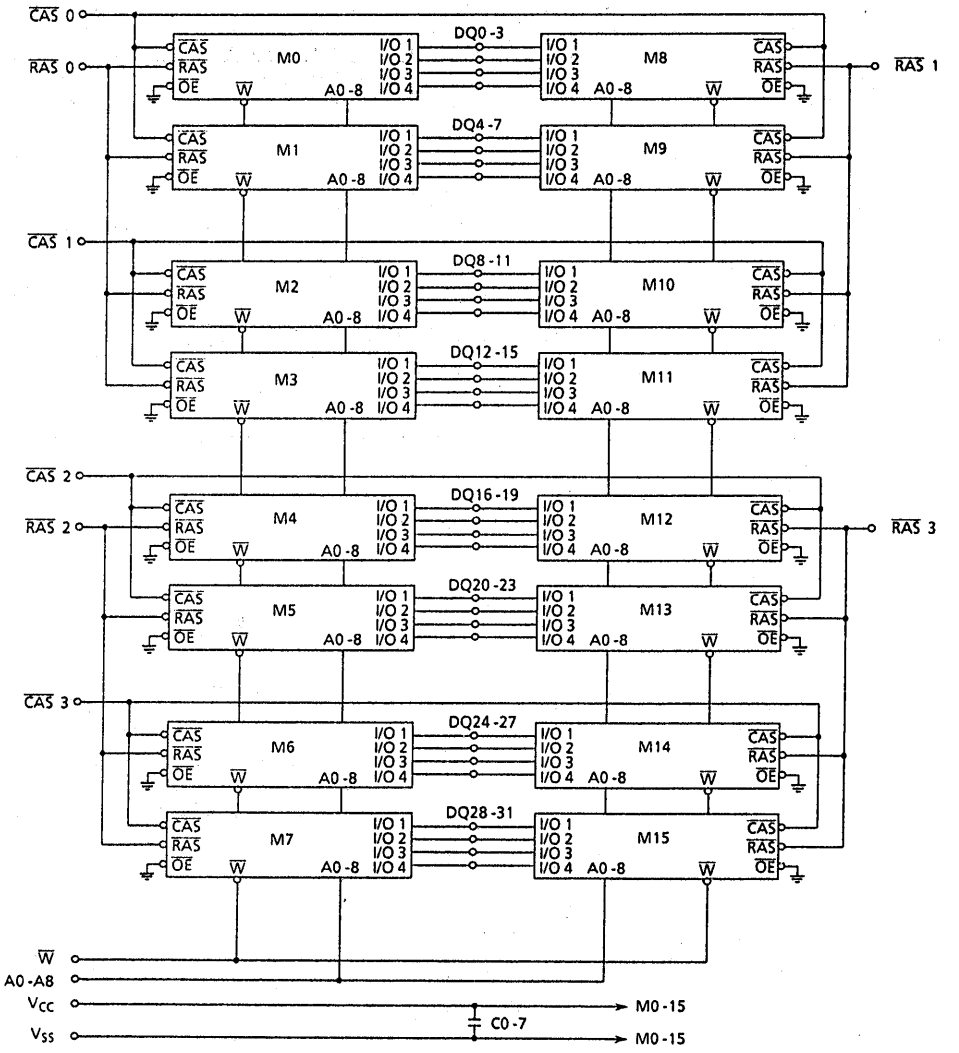
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ31	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ22	37	NC	49	DQ8	61	DQ13
2	DQ0	14	A2	26	DQ7	38	NC	50	DQ24	62	DQ30
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	PD0
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ27	68	PD1
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	PD3
11	NC	23	DQ21	35	NC	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	NC	48	NC	60	DQ29	72	V_{SS}

	-60	-70	-80	-10
PD0	NC	NC	NC	NC
PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	9.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	736	mA	3, 4 5
		THMxxxxxx-70	–	656		
		THMxxxxxx-80	–	576		
		THMxxxxxx-10	–	496		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	32	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	736	mA	3,5
		THMxxxxxx-70	–	656		
		THMxxxxxx-80	–	576		
		THMxxxxxx-10	–	496		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx-60	–	496	mA	3, 4 5
		THMxxxxxx-70	–	496		
		THMxxxxxx-80	–	416		
		THMxxxxxx-10	–	336		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	16	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	736	mA	3,5
		THMxxxxxx-70	–	656		
		THMxxxxxx-80	–	576		
		THMxxxxxx-10	–	496		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leqq V_{IN} \leqq 6.5V$, All Other Pins Not Under Test = 0V)		– 160	160	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leqq V_{OUT} \leqq 5.5V$)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

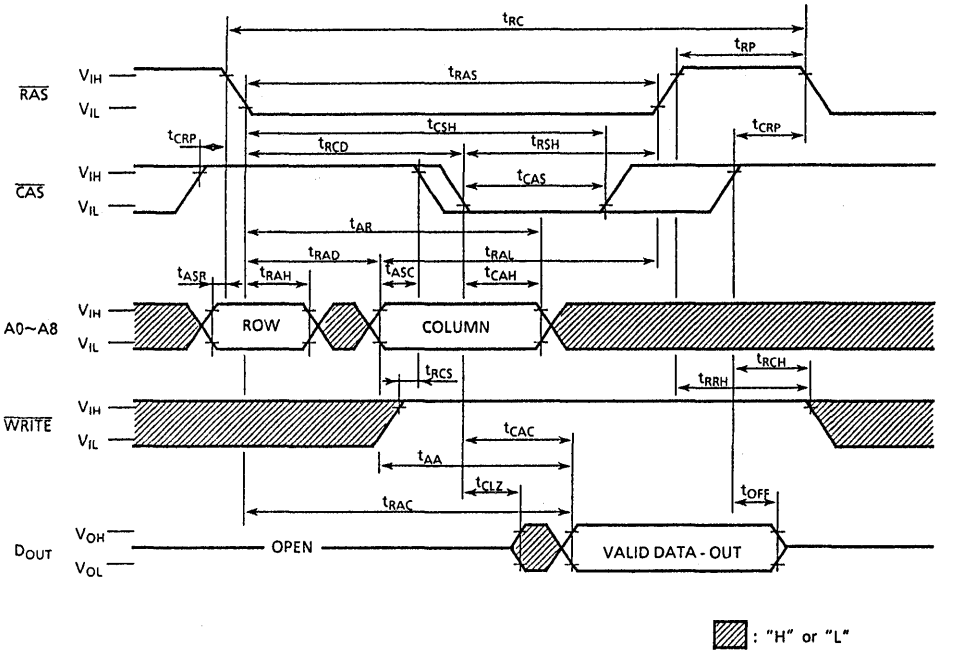
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A8)	–	120	pF
CI2	Input Capacitance ($\overline{W}$)	–	90	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	–	40	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	30	pF
CDQ1	I/O Capacitance (DQ0~31)	–	25	pF

NOTES:

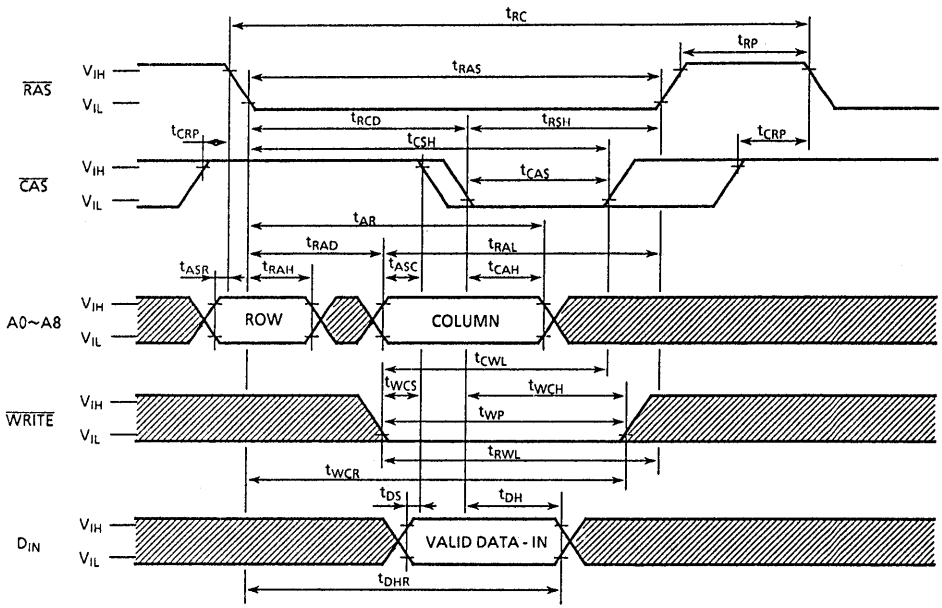
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T = 5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

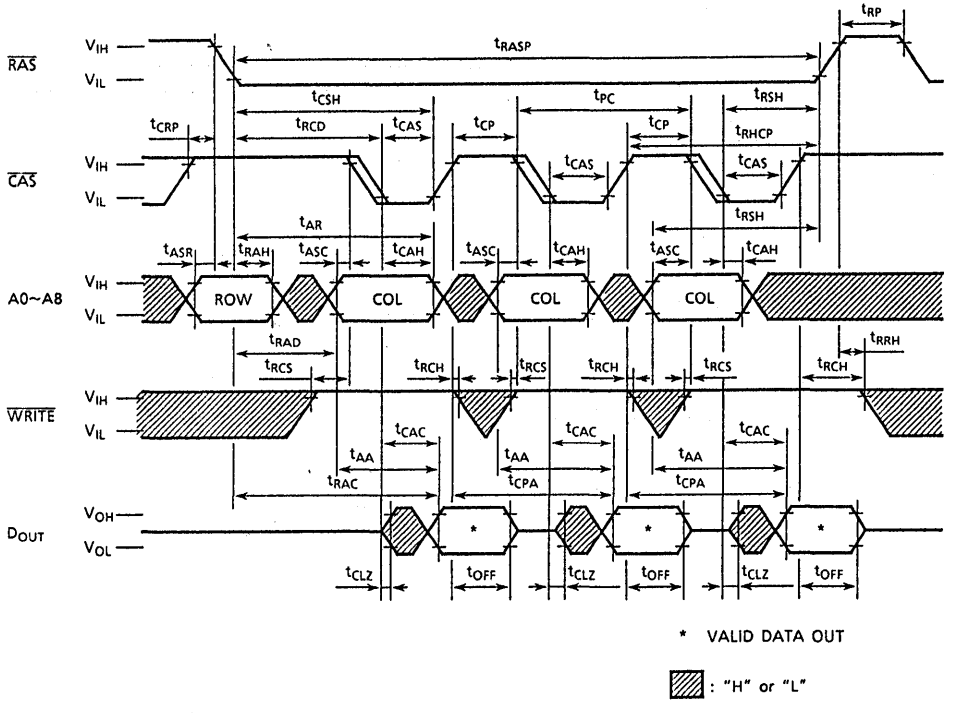
READ CYCLE



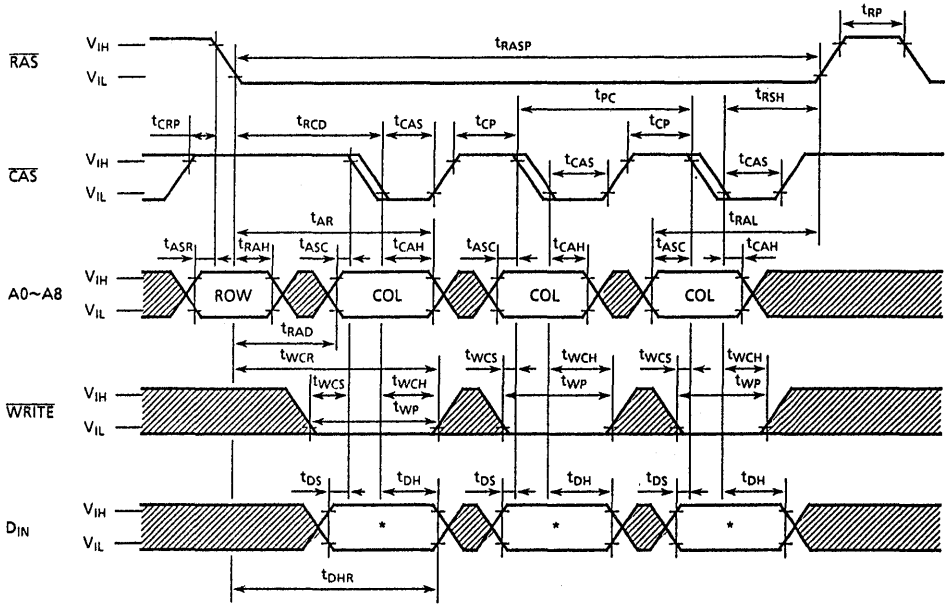
WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ CYCLE



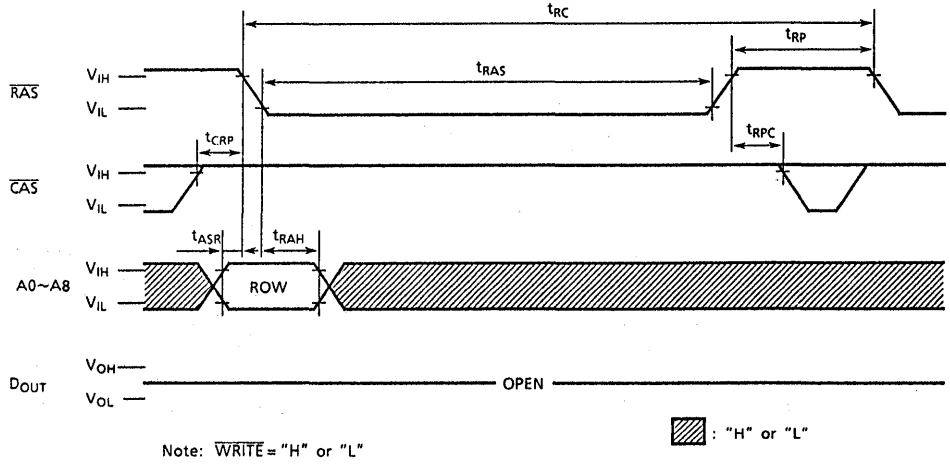
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

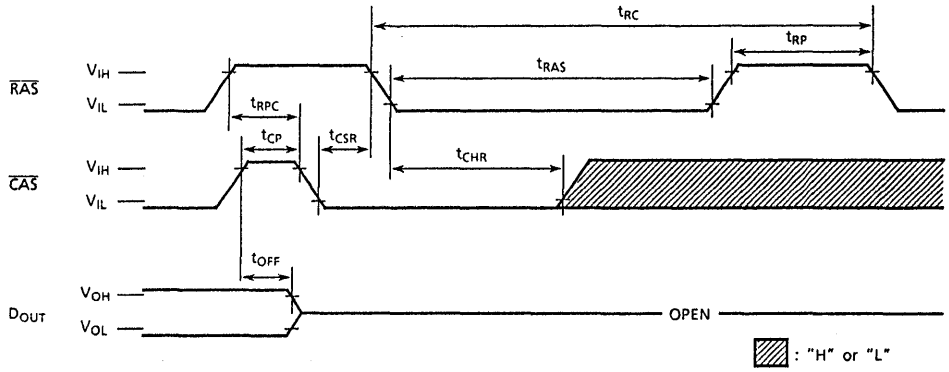
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



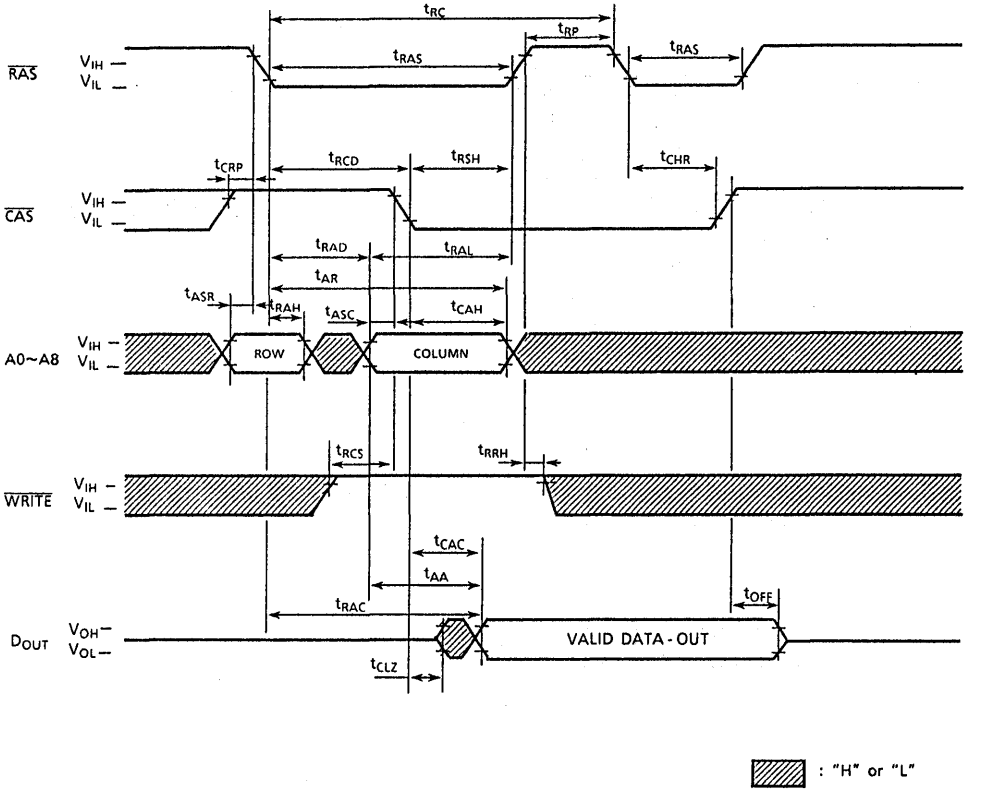
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

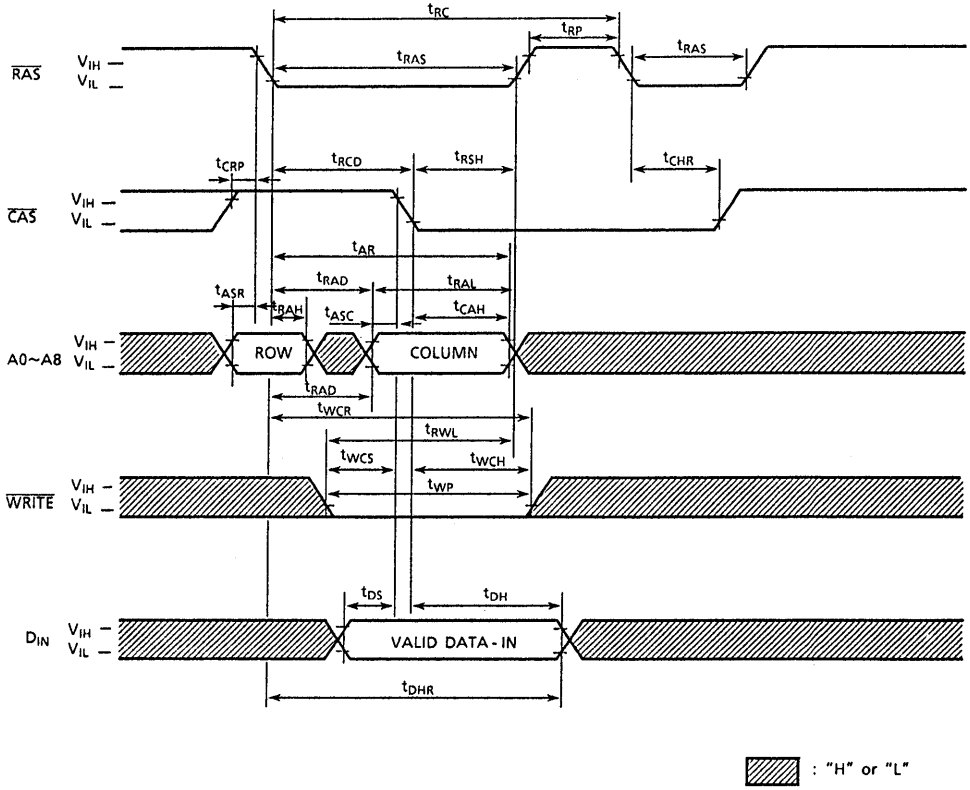


Note: A0~A8, $\overline{WRITE}$ = "H" or "L"

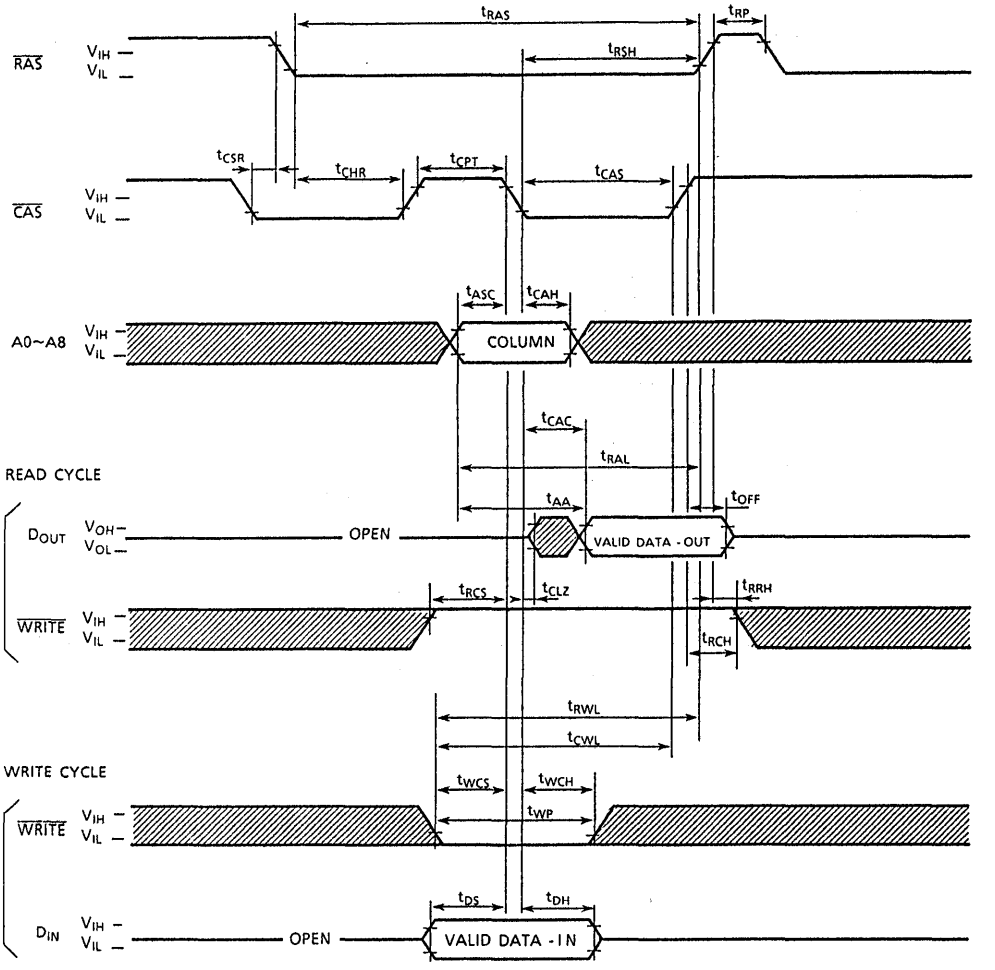
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



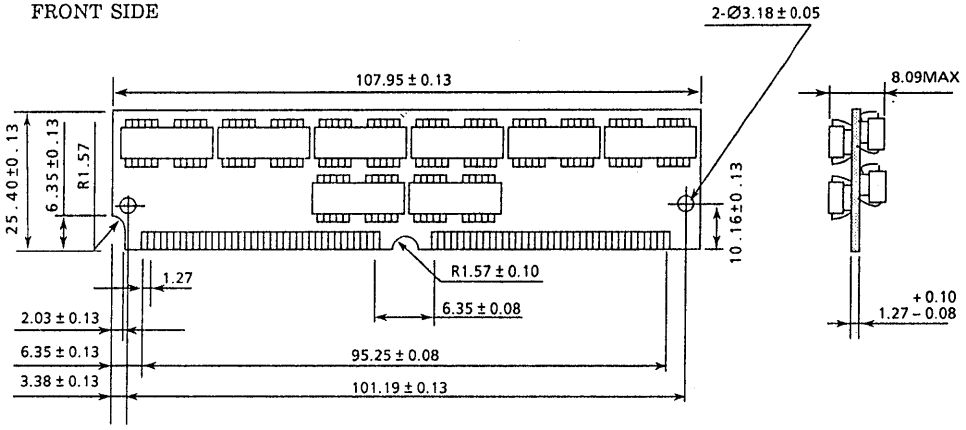
: "H" or "L"

OUTLINE DRAWINGS

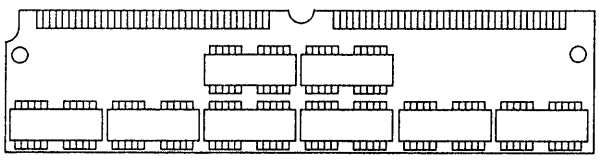
THM325120AS/ASG

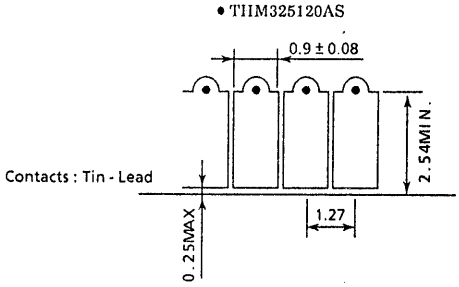
Unit in mm

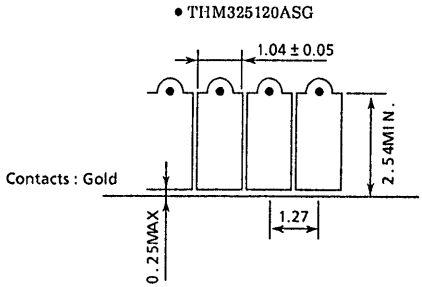
FRONT SIDE



BACK SIDE







NOTES

524,288 WORDS x 36 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM365120BS/BSG/AS/ASG is a 524,288 words by 36 bits dynamic RAM module which assembled 16 pcs of TC514256AJ/BJ and 8 pcs of TC51256T on the printed circuit board. These modules can be as well used as 1,048,576 words by 18 bits dynamic RAM module, by means of connecting DQ0 and DQ18, DQ1 and DQ19, DQ2 and DQ20, ·····, DQ17 and DQ35, respectively. The These modules are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

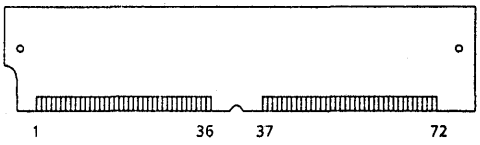
FEATURES

- 524,288 words by 36 bits organization
- Fast access time and cycle time

		-60	-70	-80	-10
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA}	Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC}	Cycle Time	115ns	130ns	150ns	180ns
t_{PC}	Fast Page Mode Cycle Time	40ns	40ns	45ns	55ns

- Low Power
  6,072mW MAX. Operating (THMxxxxxx-60)
  5,412mW MAX. Operating (THMxxxxxx-70)
  4,752mW MAX. Operating (THMxxxxxx-80)
  4,092mW MAX. Operating (THMxxxxxx-10)
  132mW MAX. Standby
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- 512 refresh cycles/4ms(Burst Refresh)
- 512 refresh cycles/8ms(Distributed Refresh)
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh and Fast Page Mode capability
- Package THM365120BS - 60 : Tin - Lead Contact
  THM365120AS - 70,80,10 : Tin - Lead Contact
  THM365120BSG - 60 : Gold Contact
  THM365120ASG - 70,80,10 : Gold Contact

PIN CONNECTION (TOP VIEW)



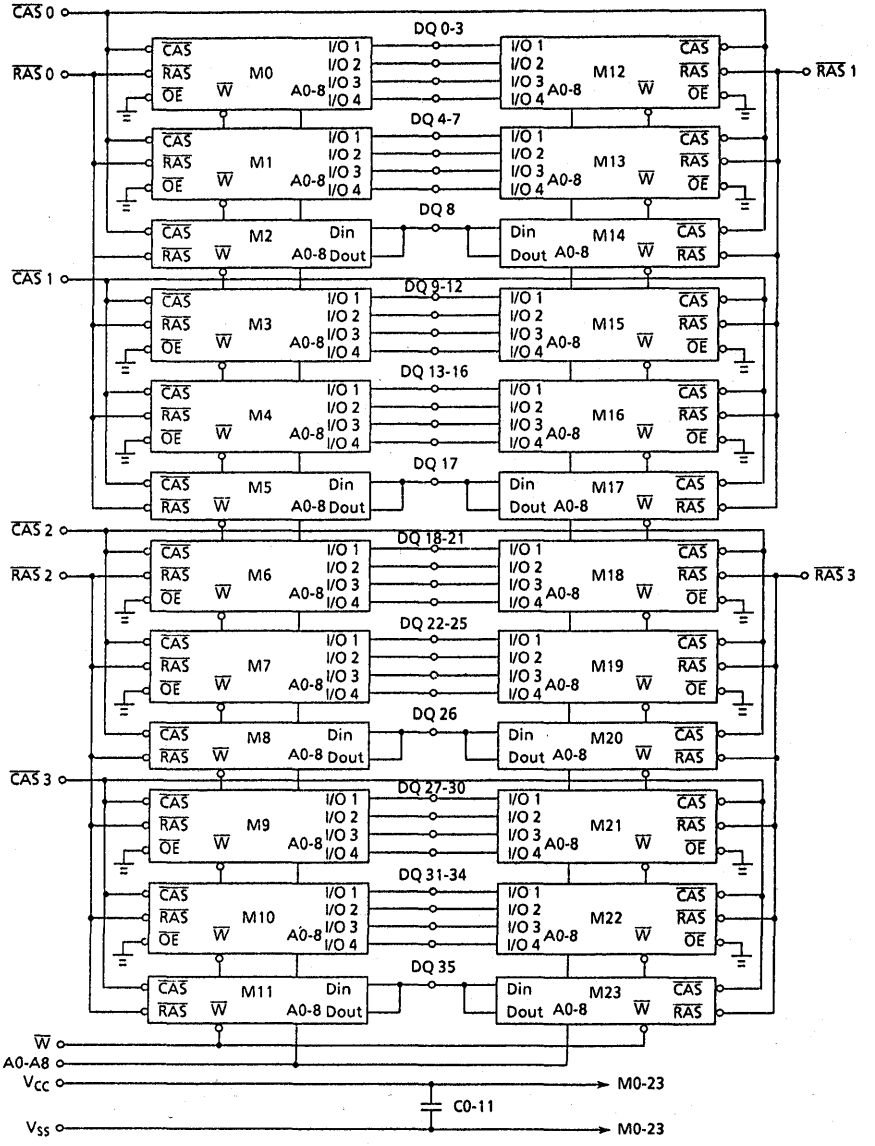
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ35	Data Input/Outputs
$\overline{CAS0}$~$\overline{CAS3}$	Column Address Strobe
$\overline{RAS0}$~$\overline{RAS3}$	Row Address Strobe
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD0
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ30	68	PD1
9	DQ21	21	DQ22	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ13	69	PD2
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD3
11	NC	23	DQ23	35	DQ26	47	$\overline{W}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

	-60	-70	-80	-10
PD0	NC	NC	NC	NC
PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTE
Input Voltage	V_{IN}	−1.0~7.0	V	1
Output Voltage	V_{OUT}	−1.0~7.0	V	1
Power Supply Voltage	V_{CC}	−1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	−55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	14.4	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	–	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	–	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	1104	mA	3, 4 5
		THMxxxxxx-70	–	984		
		THMxxxxxx-80	–	864		
		THMxxxxxx-10	–	744		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		–	48	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	1104	mA	3,5
		THMxxxxxx-70	–	984		
		THMxxxxxx-80	–	864		
		THMxxxxxx-10	–	744		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{PC} = t_{PC}$ MIN.)	THMxxxxxx-60	–	744	mA	3, 4 5
		THMxxxxxx-70	–	744		
		THMxxxxxx-80	–	624		
		THMxxxxxx-10	–	504		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2V$)		–	24	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN.)	THMxxxxxx-60	–	1104	mA	3,5
		THMxxxxxx-70	–	984		
		THMxxxxxx-80	–	864		
		THMxxxxxx-10	–	744		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 6.5V$, All Other Pins Not Under Test = 0V)		– 240	240	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, $0V \leq V_{OUT} \leq 5.5V$)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	*Refresh Period*	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	

CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

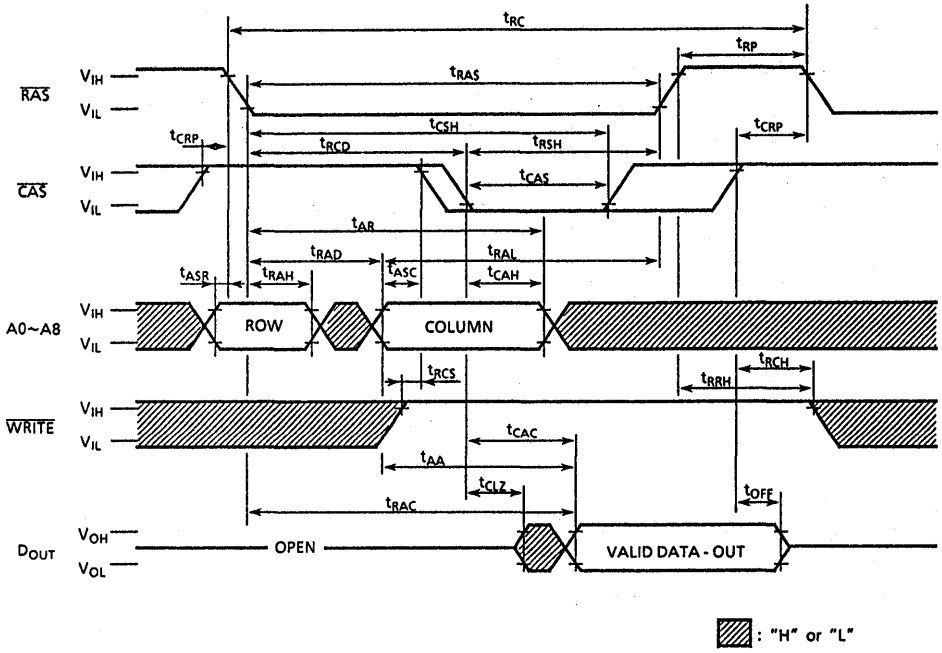
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A8)	–	161	pF
CI2	Input Capacitance ($\overline{W}$)	–	168	pF
CI3	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	–	42	pF
CI4	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	–	42	pF
CDQ1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	–	29	pF
CDQ2	I/O Capacitance (DQ8, 17, 26, 35)	–	39	pF

NOTES:

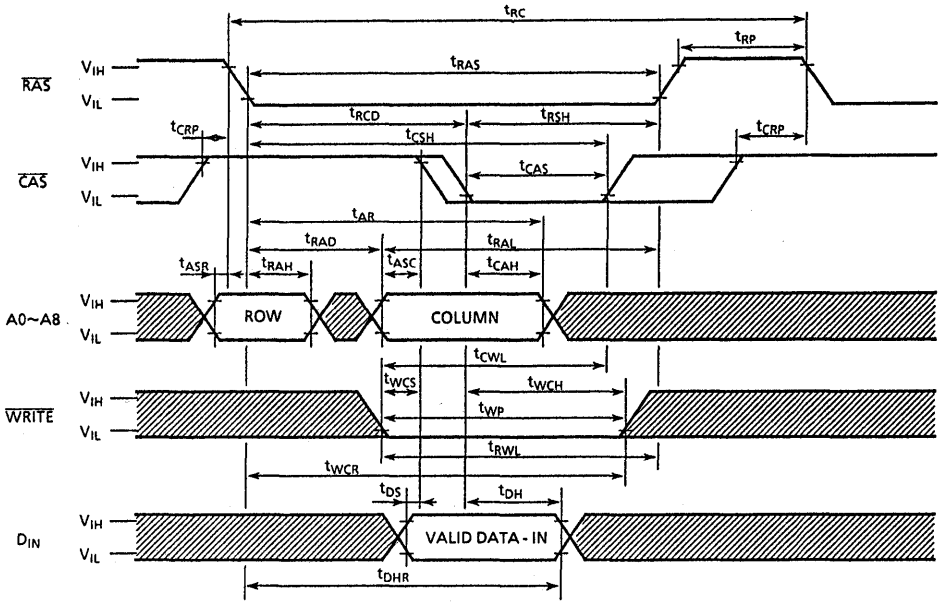
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5ns$.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met.
    t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

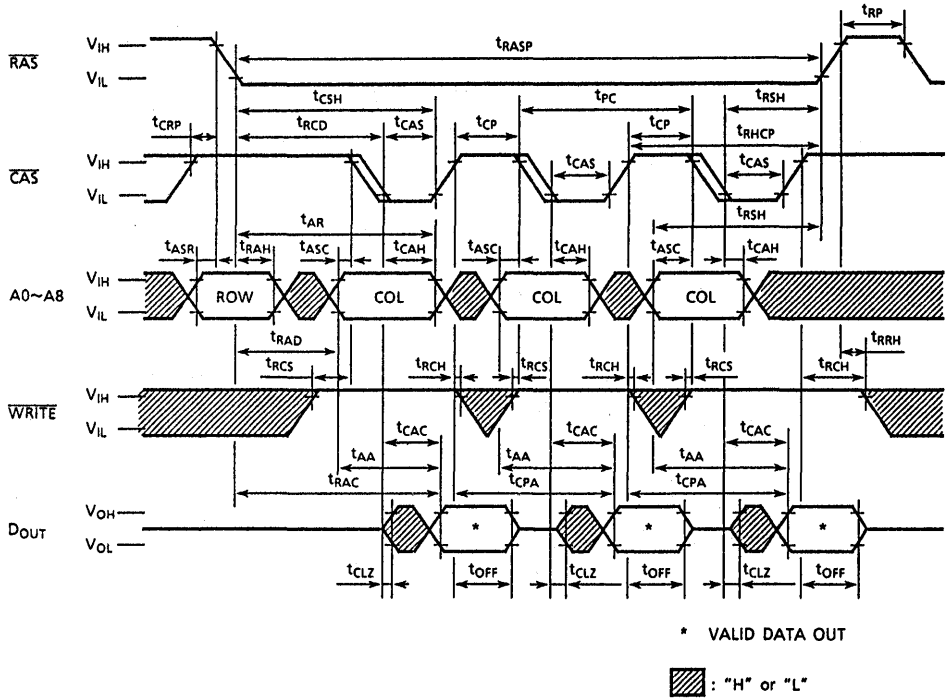
READ CYCLE



WRITE CYCLE (EARLY WRITE)



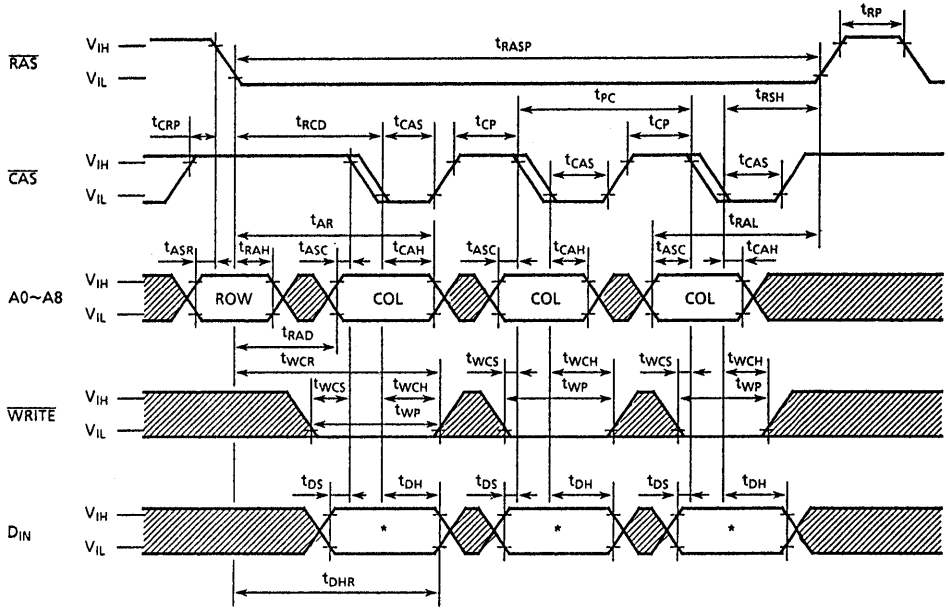
FAST PAGE MODE READ CYCLE



* VALID DATA OUT

▨ : "H" or "L"

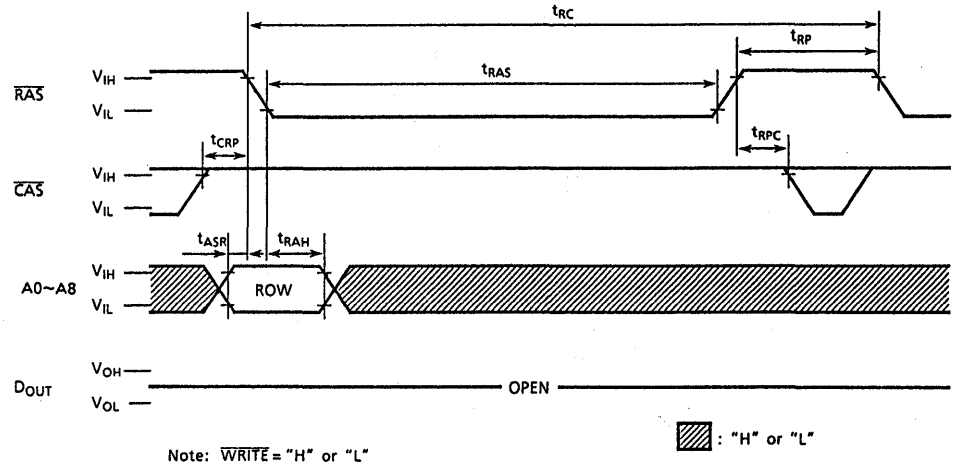
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



* VALID DATA IN

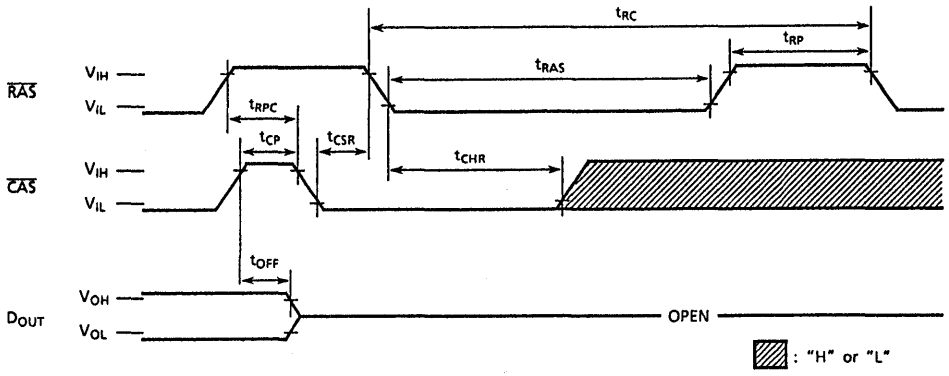
▨ : "H" or "L"

$\overline{RAS}$ ONLY REFRESH CYCLE



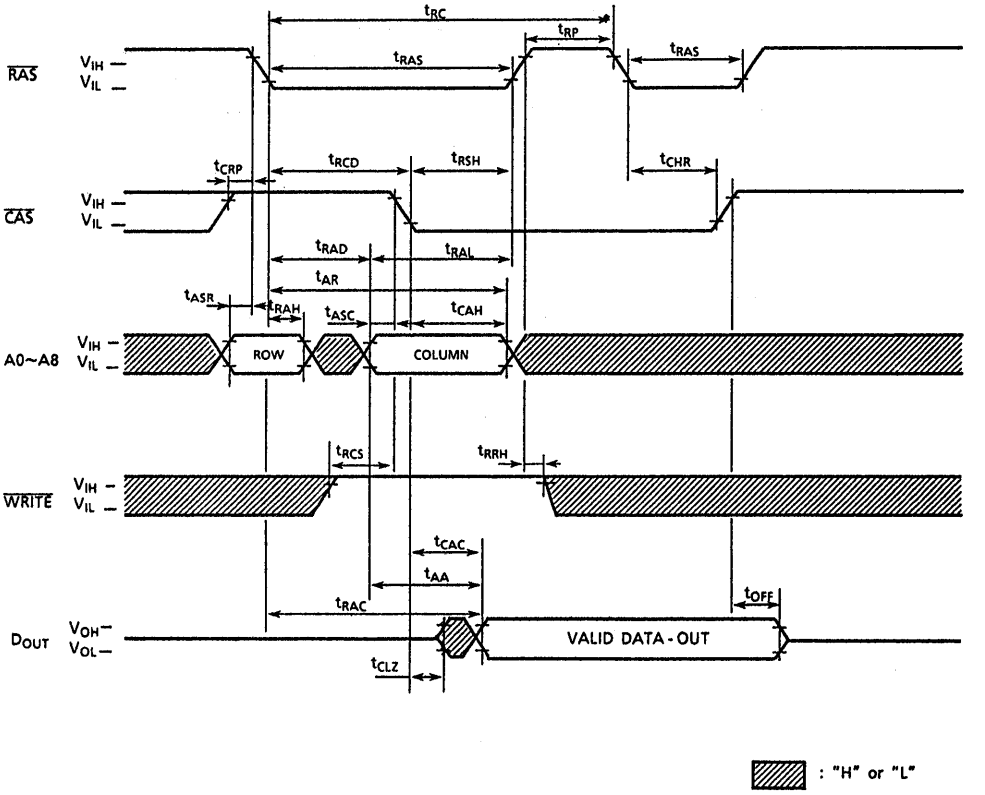
Note: $\overline{WRITE}$ = "H" or "L"

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

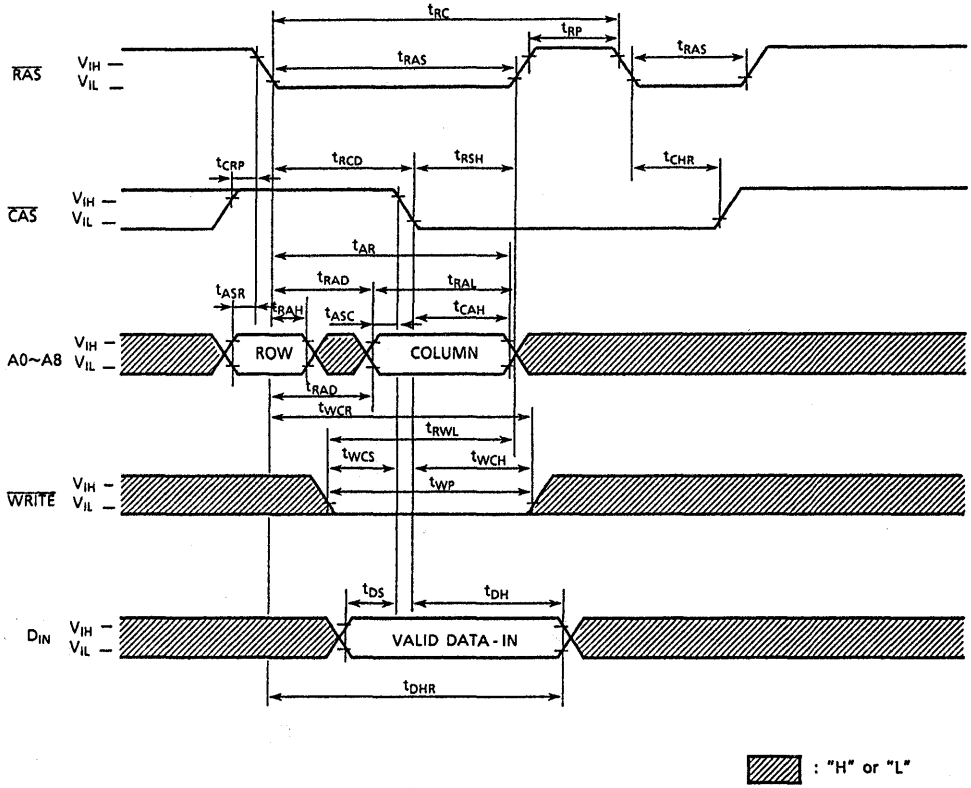


Note: A0~A8, $\overline{WRITE}$ = "H" or "L"

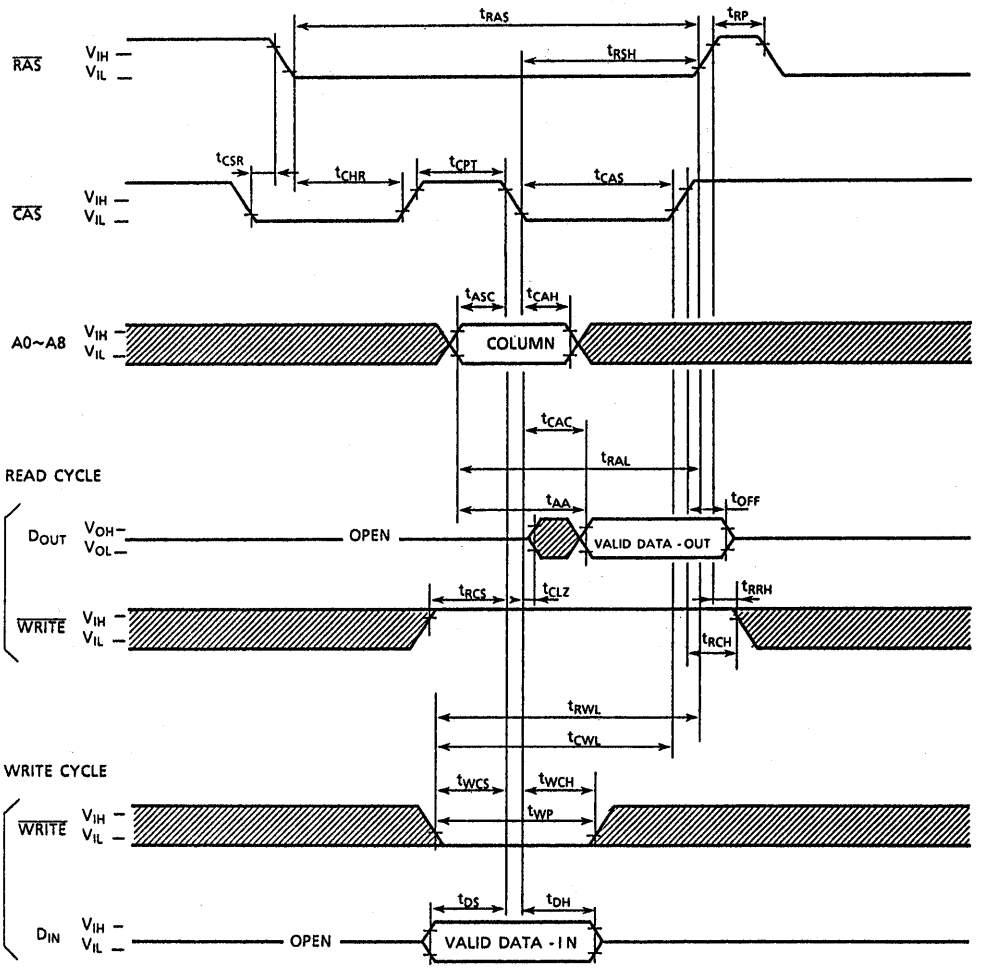
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



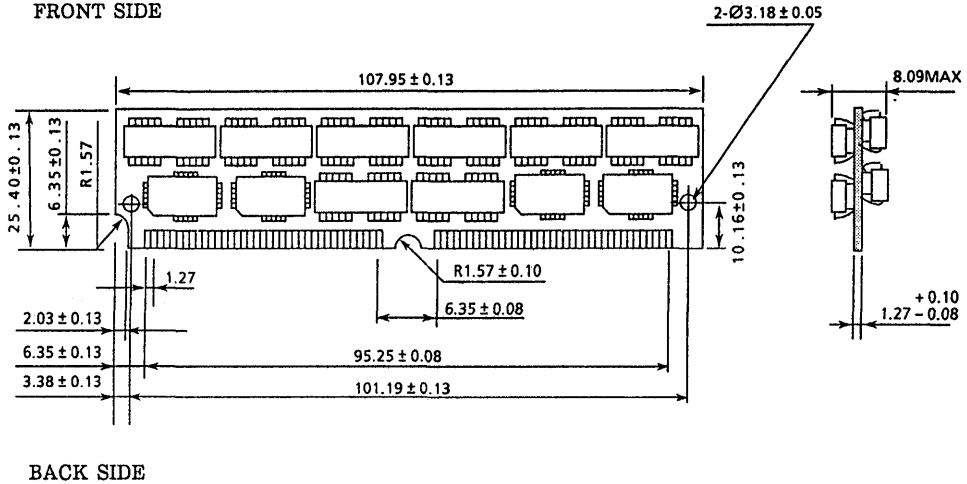
: "H" or "L"

OUTLINE DRAWINGS

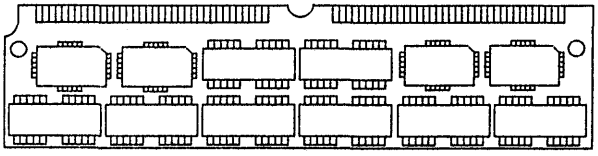
THM365120AS/ASG

Unit in mm

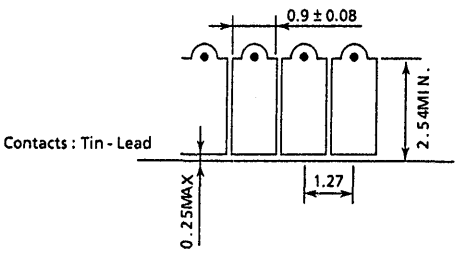
FRONT SIDE



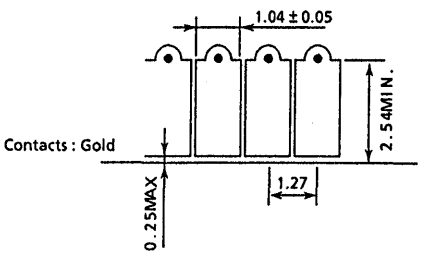
BACK SIDE



• THM365120AS



• THM365120ASG



NOTES

524,288 WORDS×40 BIT DYNAMIC RAM MODULE

DESCRIPTION

The THM405120ASG/BSG is a 524,288 words by 40 bits dynamic RAM module which assembled 20 pcs of TC514256AJ/BJ on the printed circuit board.

The THM405120ASG/BSG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and as image memory systems, and to the others which are requested compact size.

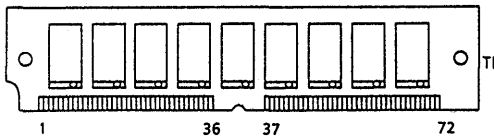
FEATURES

- 524,288 words by 40 bits organization

	-60	-70	-80	-10
t_{RAC} $\overline{RAS}$ Access Time	60ns	70ns	80ns	100ns
t_{AA} Column Address Access Time	30ns	35ns	40ns	50ns
t_{CAC} $\overline{CAS}$ Access Time	20ns	20ns	20ns	25ns
t_{RC} Cycle Time	110ns	130ns	150ns	180ns
t_{PC} Fast Page Mode Cycle Time	45ns	45ns	50ns	60ns

- Fast access time and cycle time
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Gold Contact
- JEDEC OUTLILNE : THM405120BSG - 60, ASG - 70, 80, 10
- Low power
  - 5,060mW MAX. Operating (THMxxxxxx-60)
  - 4,510mW MAX. Operating (THMxxxxxx-70)
  - 3,960mW MAX. Operating (THMxxxxxx-80)
  - 3,410mW MAX. Operating (THMxxxxxx-10)
  - 110mW MAX. Standby
- Read-Modify-write, $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh, and Fast Page Mode capability.
- 512 Refresh cycles / 8ms

PIN CONNECTION (TOP VIEW)



THM405120ASG/BSG

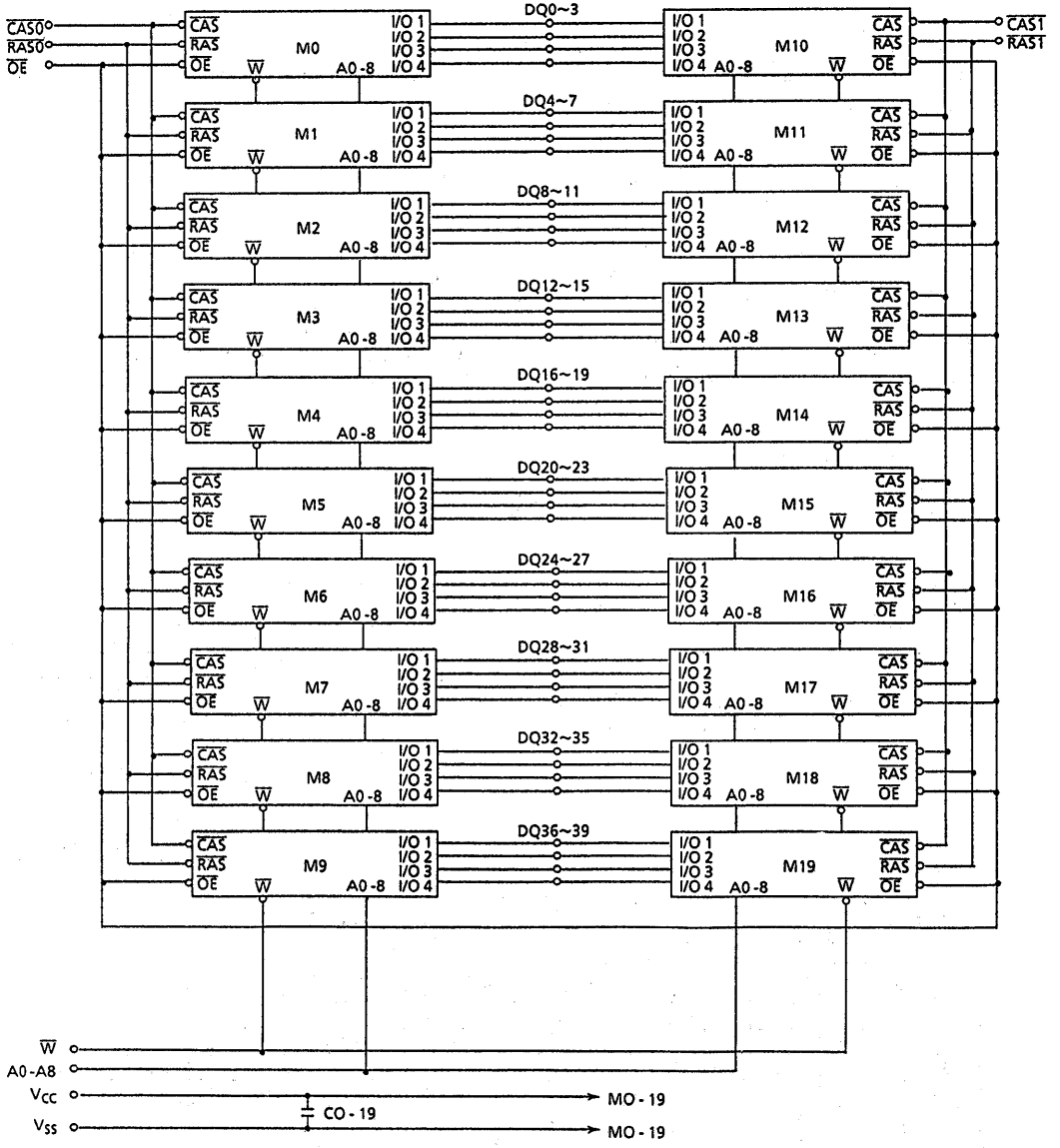
PIN NAMES

A0~A8	Address Inputs
DQ0~DQ39	Data Inputs/Outputs
$\overline{CAS0}$,$\overline{CAS1}$	Column Address Strobe
$\overline{RAS0}$,$\overline{RAS1}$	Row Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
PD	Presence Detect Pin

1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD0
8	DQ6	20	DQ8	32	NC	44	$\overline{RAS0}$	56	DQ29	68	PD1
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD2
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD3
11	NC	23	DQ11	35	DQ17	47	$\overline{W}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	V_{SS}	60	DQ32	72	V_{SS}

	-60	-70	-80	-10
PD0	NC	NC	NC	NC
PD1	V_{SS}	V_{SS}	V_{SS}	V_{SS}
PD2	NC	V_{SS}	NC	V_{SS}
PD3	NC	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNITS	NOTES
Input Voltage	V_{IN}	-1.0~7.0	V	1
Output Voltage	V_{OUT}	-1.0~7.0	V	1
Power Supply Voltage	V_{CC}	-1.0~7.0	V	1
Operating Temperature	T_{OPR}	0~70	°C	1
Storage Temperature	T_{STG}	-55~125	°C	1
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec	1
Power Dissipation	P_D	12.0	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

RECOMMENDED DC OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	MAX.	UNIT	NOTE
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	920	mA	3, 4 5
		THMxxxxxx-70	–	820		
		THMxxxxxx-80	–	720		
		THMxxxxxx-10	–	620		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		–	40	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	920	mA	3,5
		THMxxxxxx-70	–	820		
		THMxxxxxx-80	–	720		
		THMxxxxxx-10	–	620		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} MIN.)	THMxxxxxx-60	–	620	mA	3, 4 5
		THMxxxxxx-70	–	620		
		THMxxxxxx-80	–	520		
		THMxxxxxx-10	–	420		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2V)		–	20	mA	
I_{CC6}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC} = t_{RC} MIN.)	THMxxxxxx-60	–	920	mA	3,5
		THMxxxxxx-70	–	820		
		THMxxxxxx-80	–	720		
		THMxxxxxx-10	–	620		
$I_{I(L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test = 0V)		– 200	200	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		– 20	20	μA	
V_{OH}	OUTPUT LEVEL Output "H" Level Voltage (I_{OUT} = – 5mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output "L" Level Voltage (I_{OUT} = 4.2mA)		–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes 5, 6, 7)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	110	–	130	–	150	–	180	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	165	–	185	–	205	–	245	–	ns	
t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	50	–	60	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	95	–	100	–	120	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	9,14
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	9,14
t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	45	–	55	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	0	20	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	40	–	50	–	60	–	70	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100,000	70	100,000	80	100,000	100	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	35	–	40	–	45	–	55	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	60	25	75	ns	14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	15
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
t_{ASR}	Row Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
t_{ASC}	Column Address Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	0	–	ns	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(Continued)

SYMBOL	PARAMETER	THMxxxxxx-60		THMxxxxxx-70		THMxxxxxx-80		THMxxxxxx-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	10	–	15	–	15	–	20	–	ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	45	–	55	–	60	–	75	–	ns	
t_{WP}	Write Command Pulse Width	10	–	15	–	15	–	20	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
t_{DS}	Data Set-Up Time	0	–	0	–	0	–	0	–	ns	12
t_{DH}	Data Hold Time	15	–	15	–	15	–	20	–	ns	12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
t_{REF}	Refresh Period	–	8	–	8	–	8	–	8	ms	
t_{WCS}	Write Command Set-Up Time	0	–	0	–	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay Time	50	–	50	–	50	–	60	–	ns	13
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay Time	90	–	100	–	110	–	135	–	ns	13
t_{AWD}	Column Address to $\overline{WRITE}$ Delay Time	60	–	65	–	70	–	85	–	ns	13
t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WRITE}$ Delay Time	65	–	65	–	70	–	85	–	ns	13
t_{CSR}	$\overline{CAS}$ Set-Up Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle)	30	–	40	–	40	–	50	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	20	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	–	25	ns	
t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	25	–	ns	
t_{OEZ}	Output buffer turn off Delay Time from $\overline{OE}$	0	20	0	20	0	20	0	25	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	25	–	ns	
t_{ODS}	Output Disable Set-Up Time	0	–	0	–	0	–	0	–	ns	

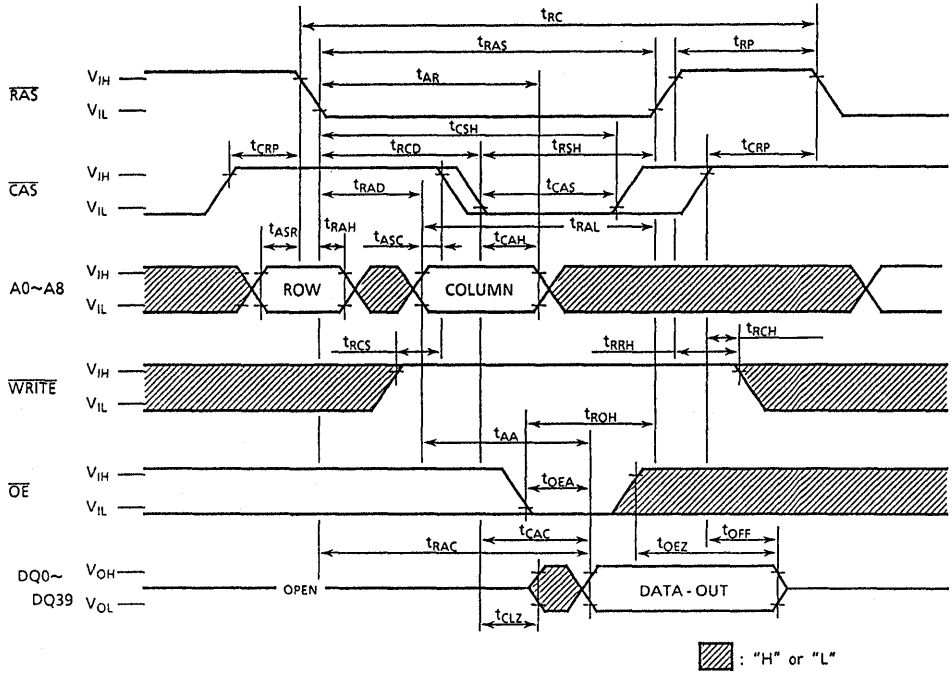
CAPACITANCE (V_{CC} = 5V ± 10%, f = 1MHz, Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
CI1	Input Capacitance (A0~A9)	-	130	pF
CI2	Input Capacitance ($\overline{W}$, $\overline{OE}$)	-	110	pF
CI3	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	-	60	pF
CI4	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	-	50	pF
CDQ	I/O Capacitance (DQ0~DQ39)	-	20	pF

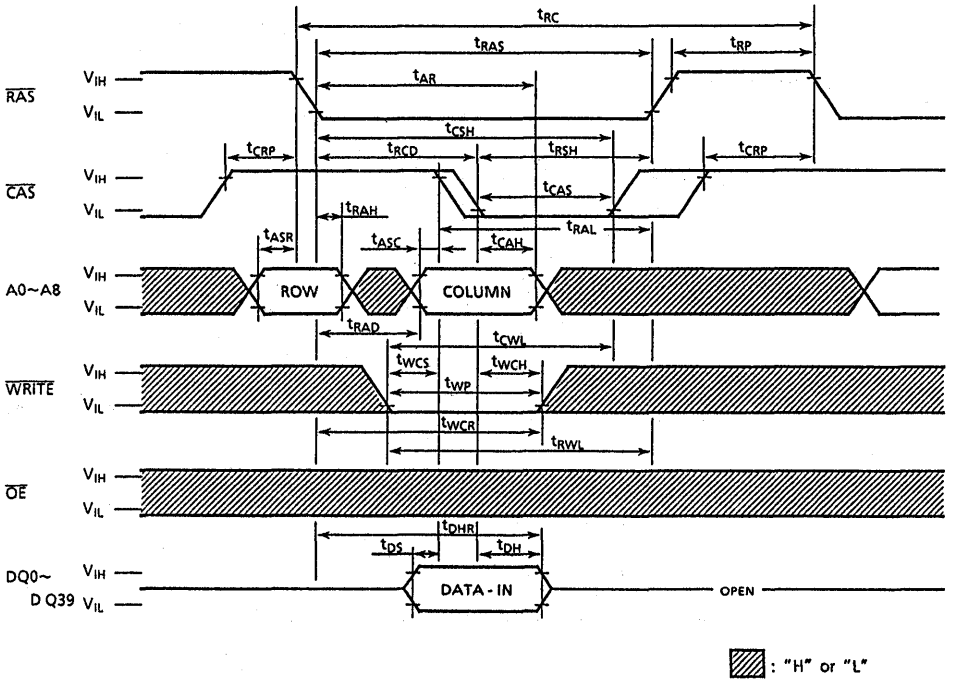
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Column address can be changed once or less while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
6. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
7. AC measurements assume $t_T=5$ns.
8. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. Measured with a load equivalent to 2 TTL loads and 100pF.
10. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min.), $t_{CWD} \geqq t_{CWD}$ (min.), $t_{AWD} \geqq t_{AWD}$ (min.) and $t_{CPWD} \geqq t_{CPWD}$ (min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
15. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

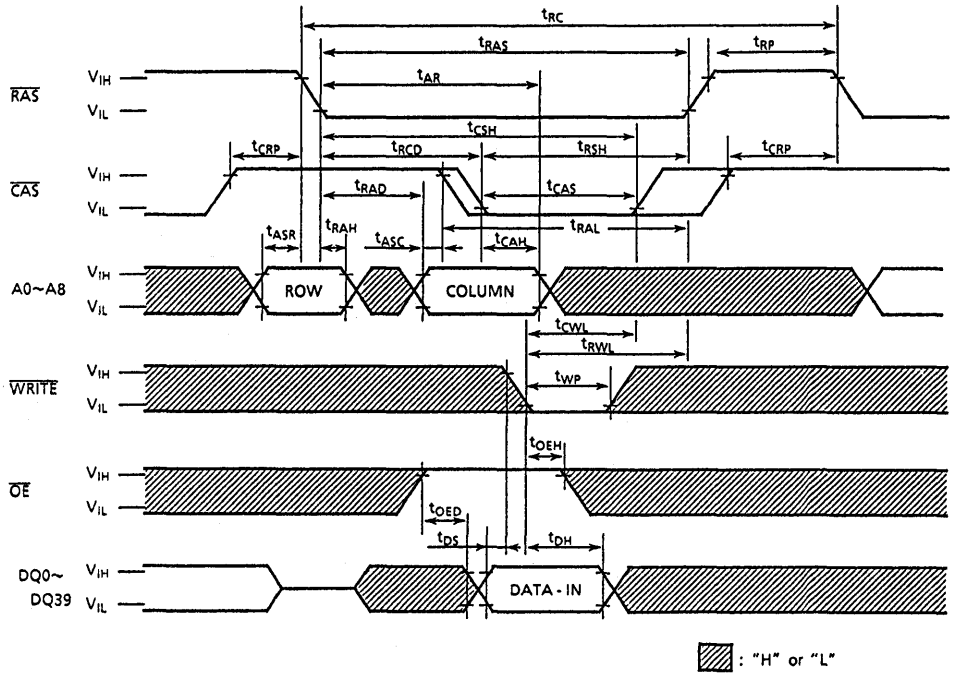
READ CYCLE


tRC
tRAS
tRP
tAR
RAS
VIH
VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
tRAD
tCAS
tASR
tRAH
tASC
tCAH
tRAL
A0~A8
ROW
COLUMN
tRCS
tRRH
tRCH
WRITE
tRQH
tAA
OE
tOEA
tCAC
tRAC
tOEZ
tOFF
DQ0~
DQ39
VOH
VOL
OPEN
DATA-OUT
tCLZ
: "H" or "L"

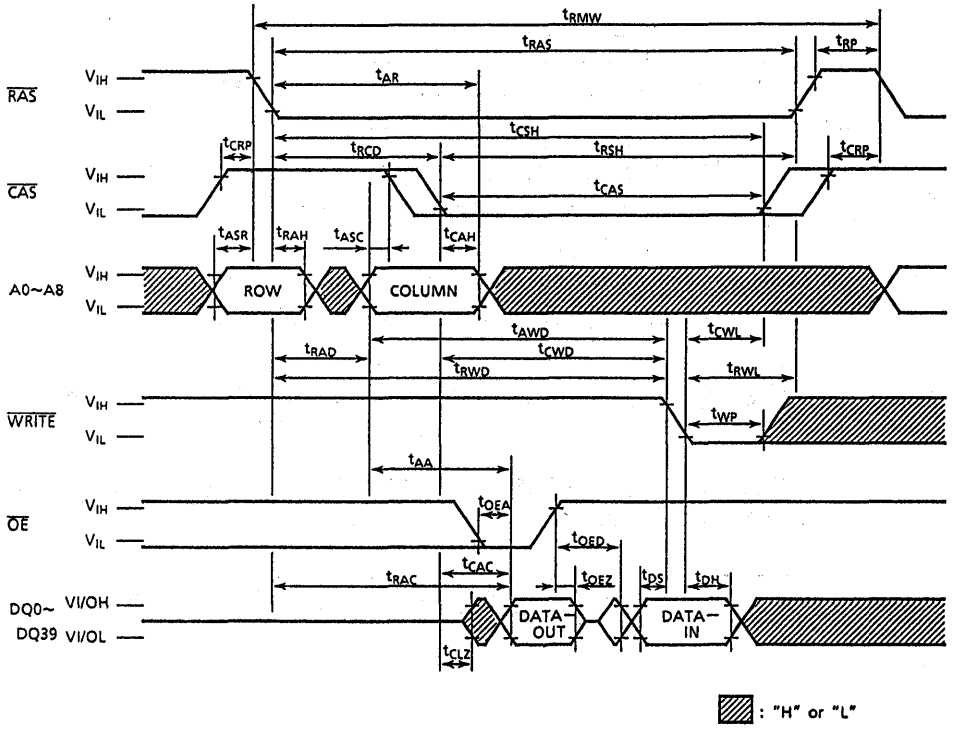
WRITE CYCLE (EARLY WRITE)



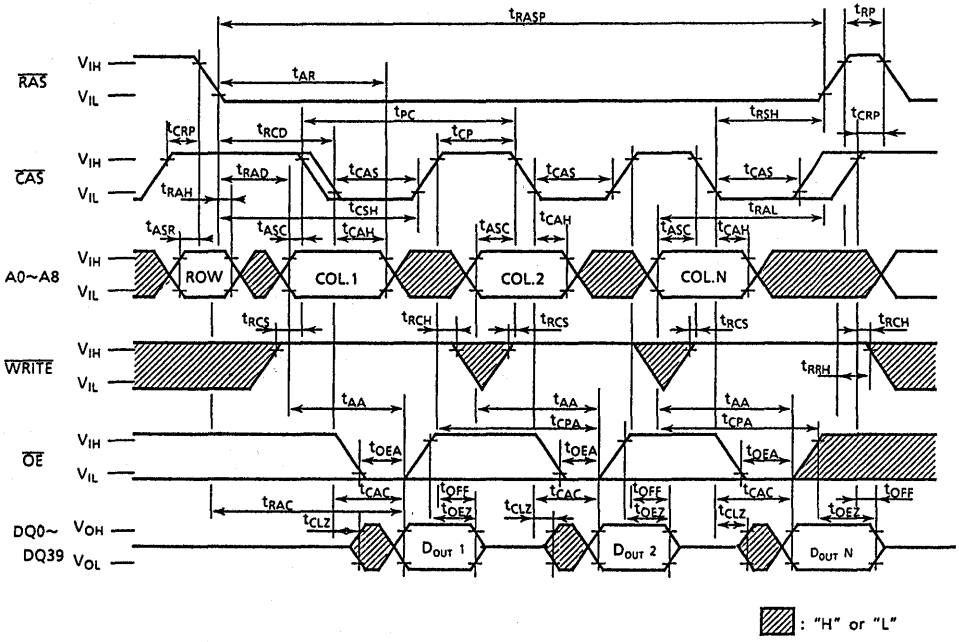
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



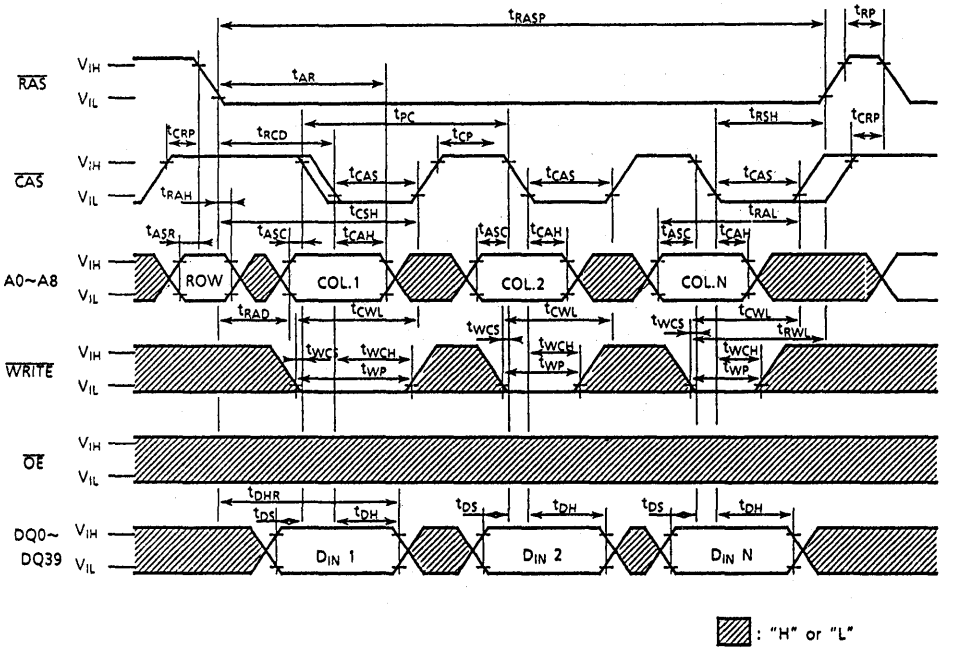
READ-MODIFY-WRITE CYCLE



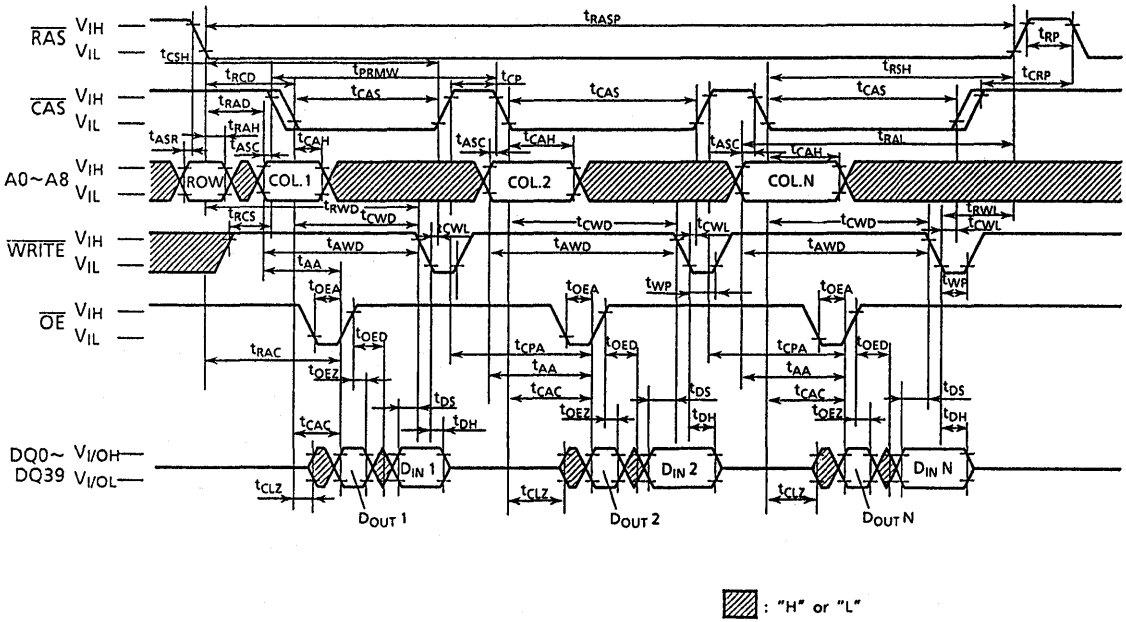
FAST PAGE MODE READ CYCLE



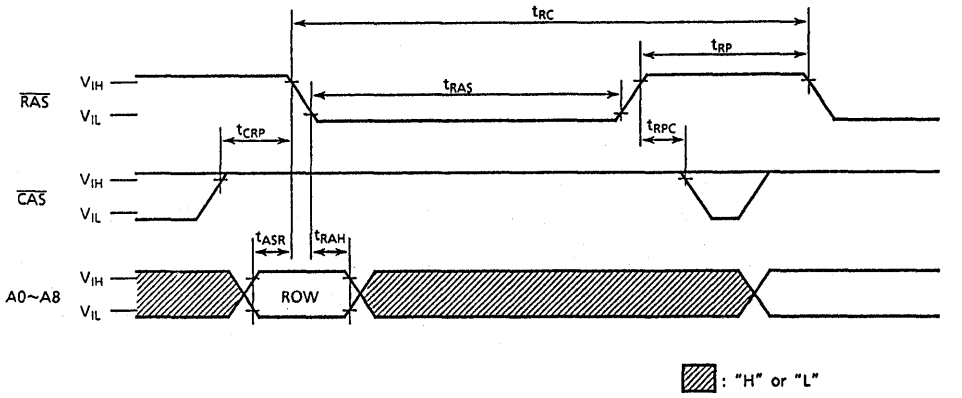
FAST PAGE MODE WRITE CYCLE



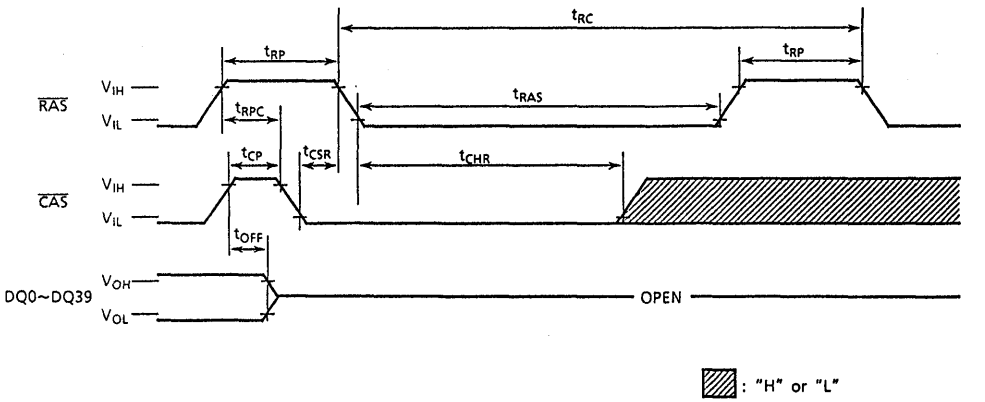
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



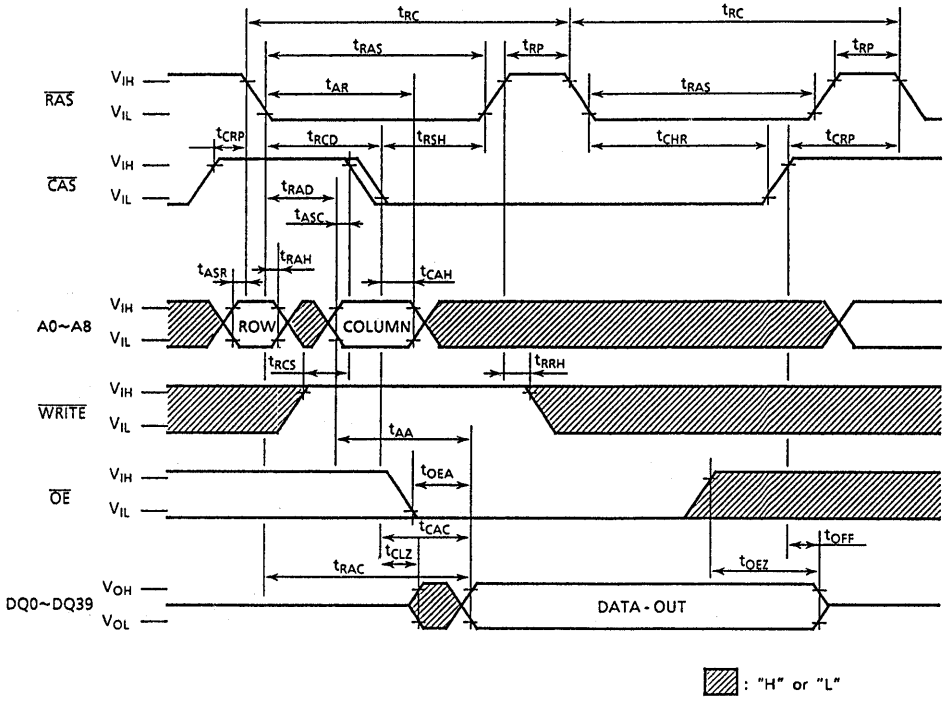
$\overline{RAS}$ ONLY REFRESH CYCLE



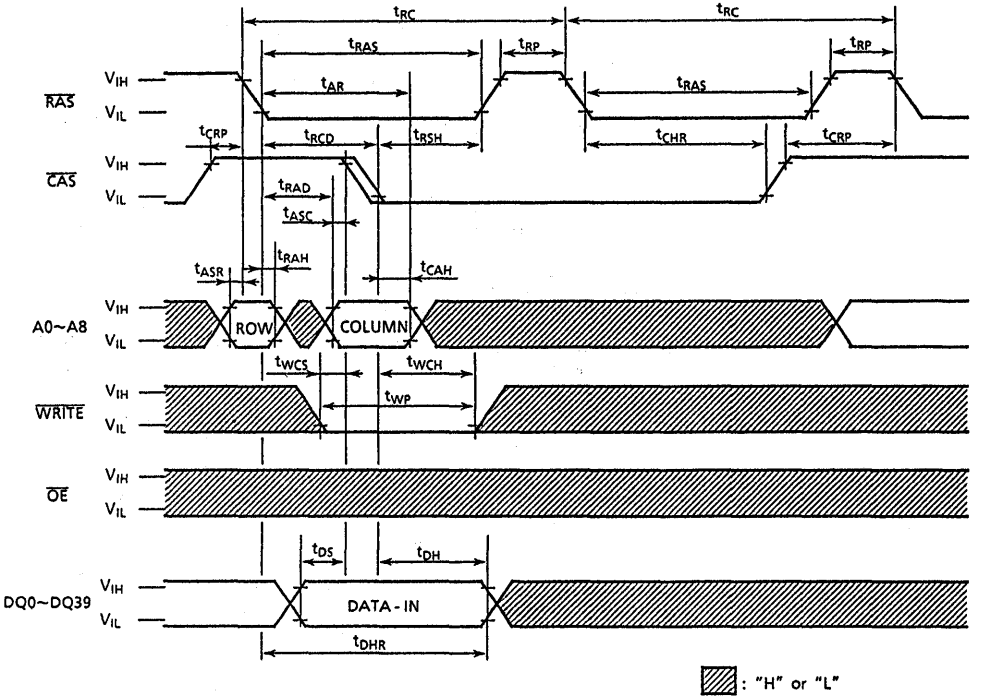
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



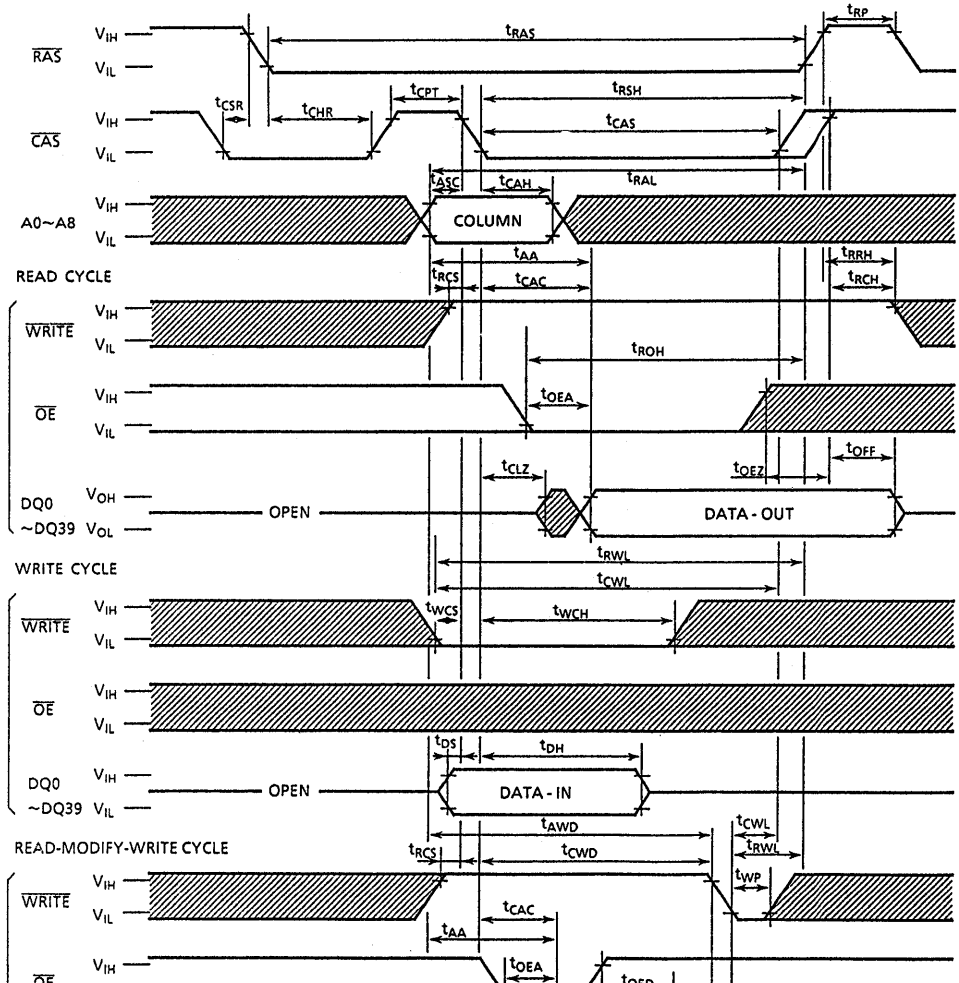
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE

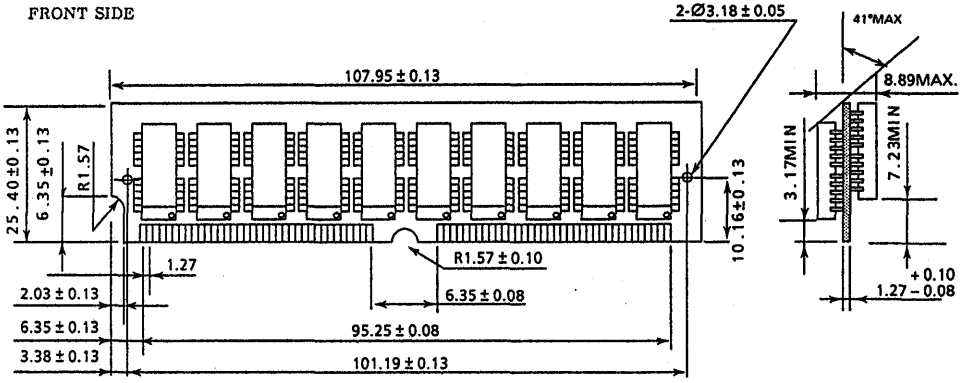


OUTLINE DRAWINGS

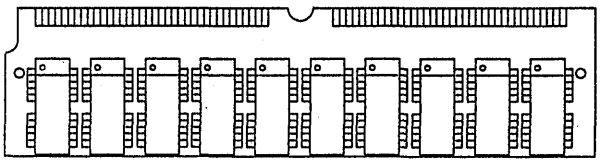
• THM405120ASG/BSG (JEDEC OUTLINE)

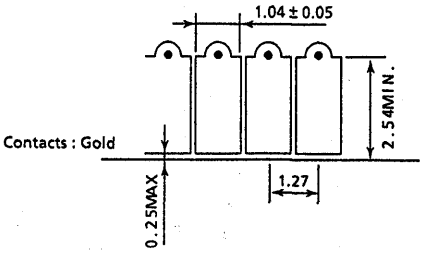
Unit in mm

FRONT SIDE



BACK SIDE





VIDEO RAM

131,072WORDS×8BITS MULTIPORT DRAM

PRELIMINARY

DESCRIPTION

The TC528126BJ/BZ is a CMOS multiport memory equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The TC528126BJ/BZ supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC528126BJ/BZ is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC528126BJ/BZ -80	TC528126BJ/BZ -10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	90mA	75mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

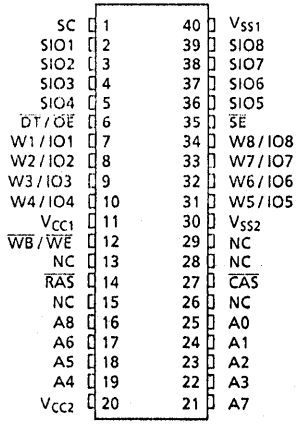
- Organization
  - RAM Port : 131,072words×8bits
  - SAM Port : 256words×8bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - 512 refresh cycles/8ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 256 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
- Package
  - TC528126BJ : SOJ40-P-400
  - TC528126BZ : ZIP40-P-475

PIN NAME

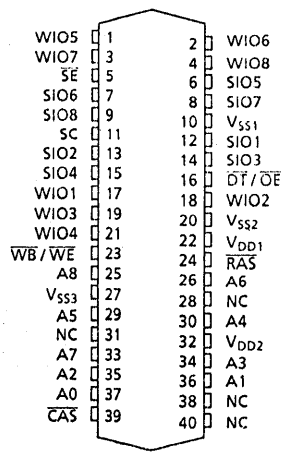
A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
W1/IO1~W8/IO8	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO8	Serial Input/Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

PIN CONNECTION

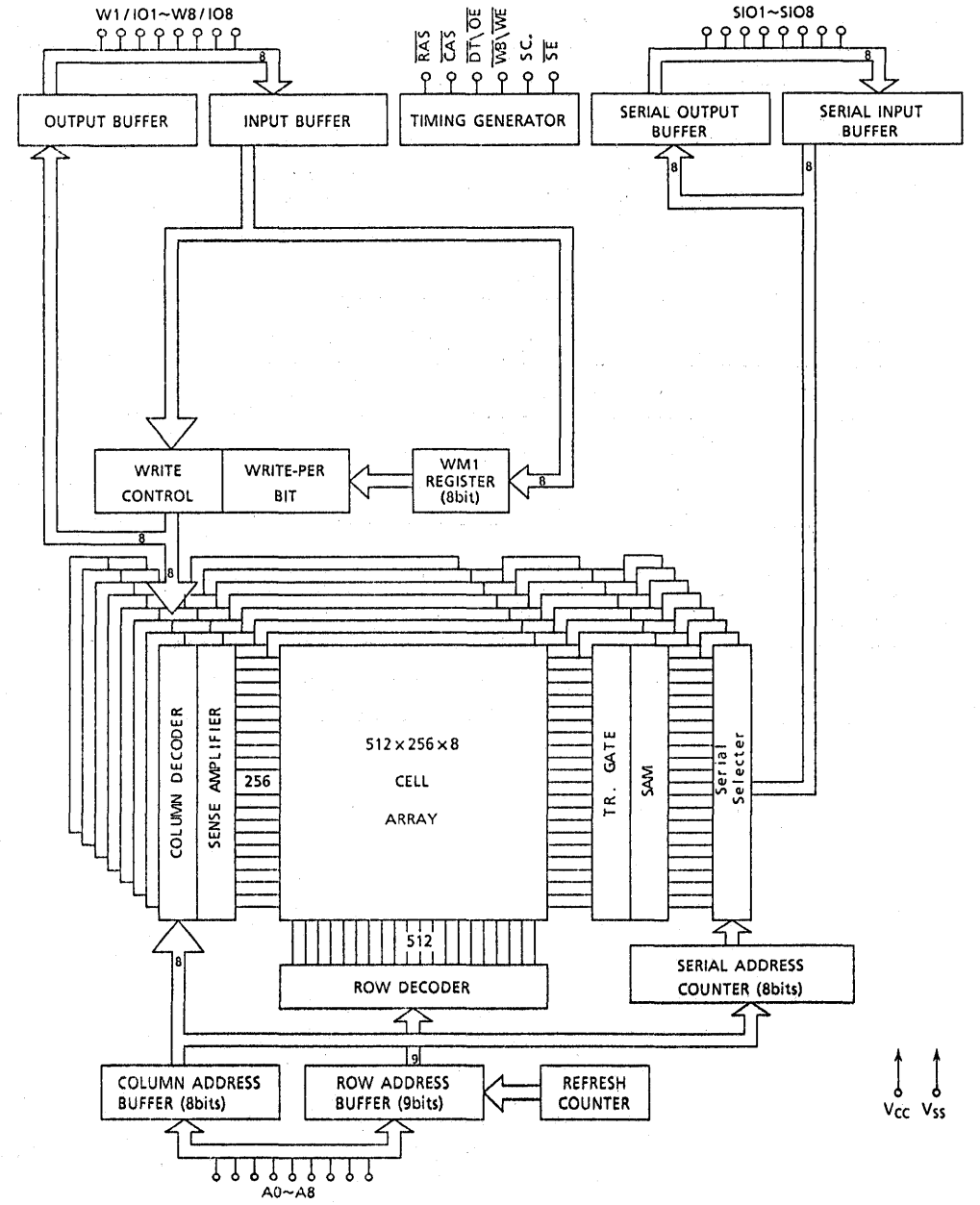
TC528126BJ



TC528126BZ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	−1.0~7.0	V	1
V_{CC}	Power Supply Voltage	−1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	−	7	pF
C_{IO}	Input/Output Capacitance	−	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC528126BJ/BZ-80		TC528126BJ/BZ-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	–	90	–	75	mA	3, 4
	Active	I_{CC1A}	–	130	–	115		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	–	90	–	75		3, 4
	Active	I_{CC3A}	–	130	–	115		3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Standby	I_{CC4}	–	80	–	65		3, 4
	Active	I_{CC4A}	–	120	–	105		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	–	90	–	75		3, 4
	Active	I_{CC5A}	–	130	–	115		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	–	110	–	95		3, 4
	Active	I_{CC6A}	–	150	–	135		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≦ V_{IN} ≦ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≦ V_{OUT} ≦ 5.5V, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = – 2mA	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC528126BJ/BZ-80		TC528126BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC528126BJ/BZ-80		TC528126BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0		ns	12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

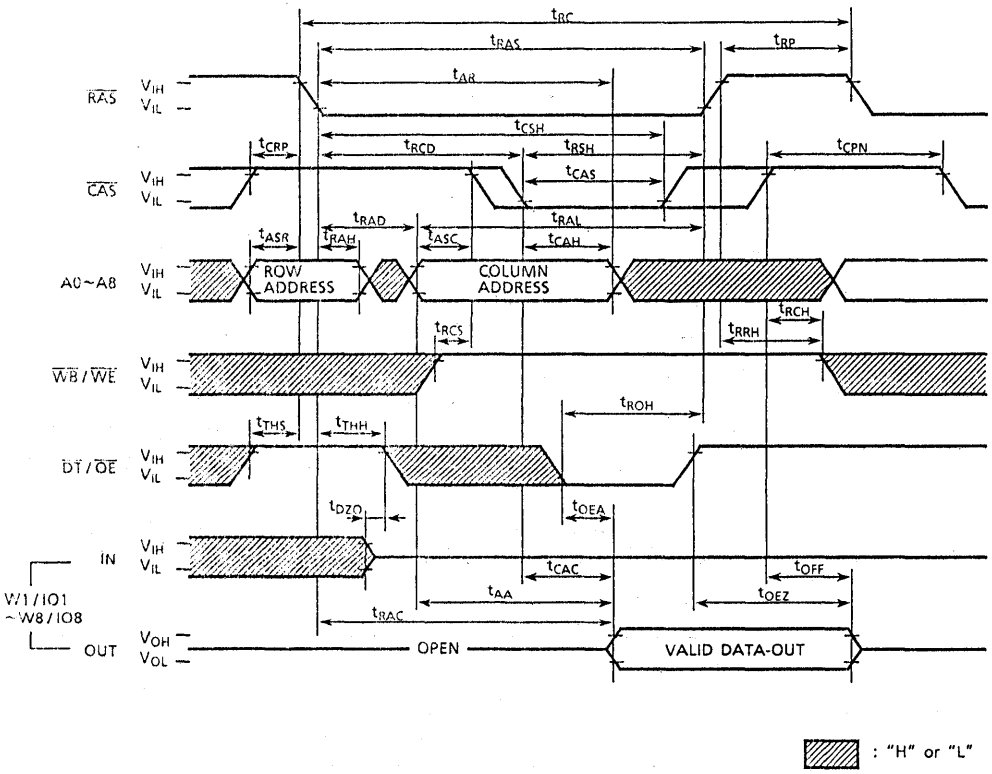
SYMBOL	PARAMETER	TC528126BJ/BZ-80		TC528126BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			

NOTES :

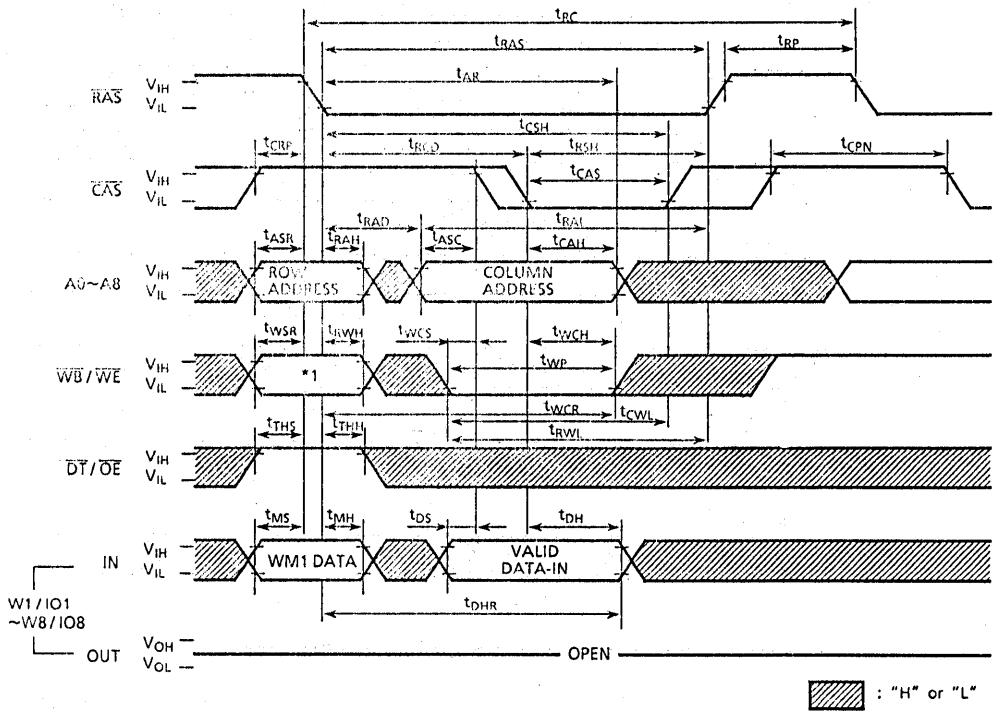
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}$/$\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$/$\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycle and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only : If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



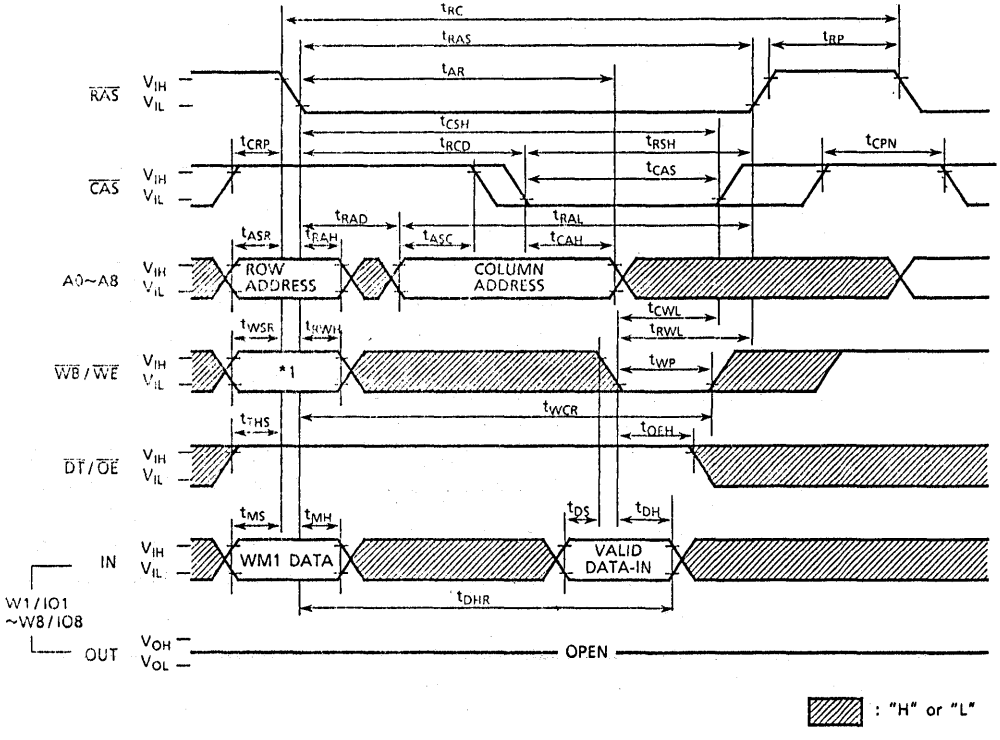
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

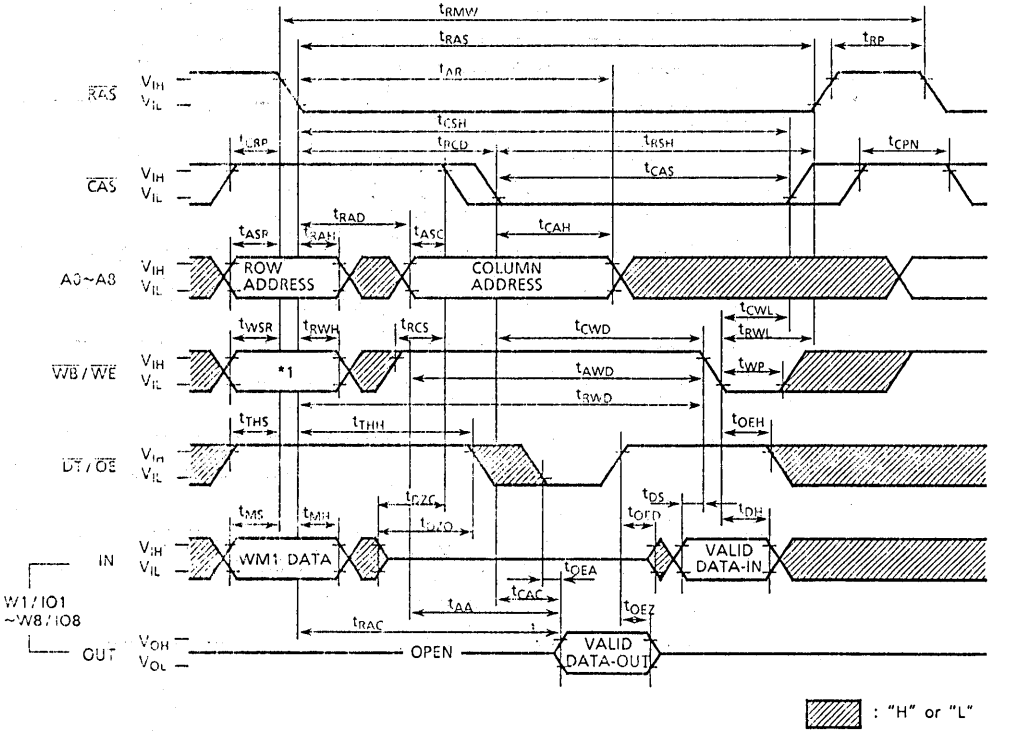
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	*Don't Care*	*Normal Write*

WM1 data : 0 : Write Disable
1 : Write Enable

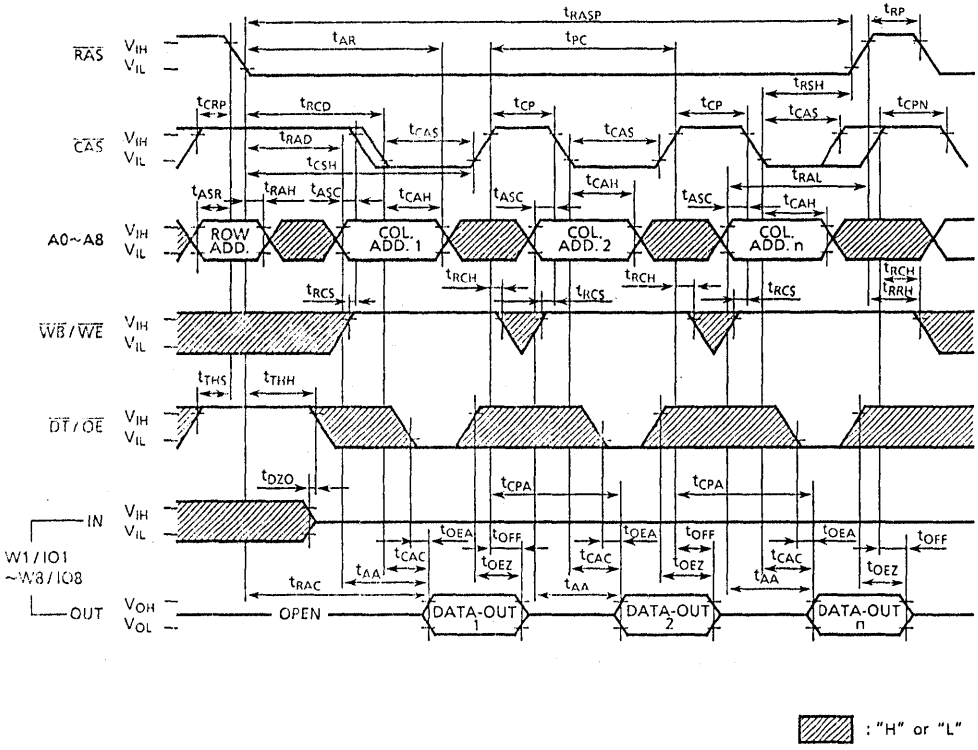
READ - MODIFY - WRITE CYCLE



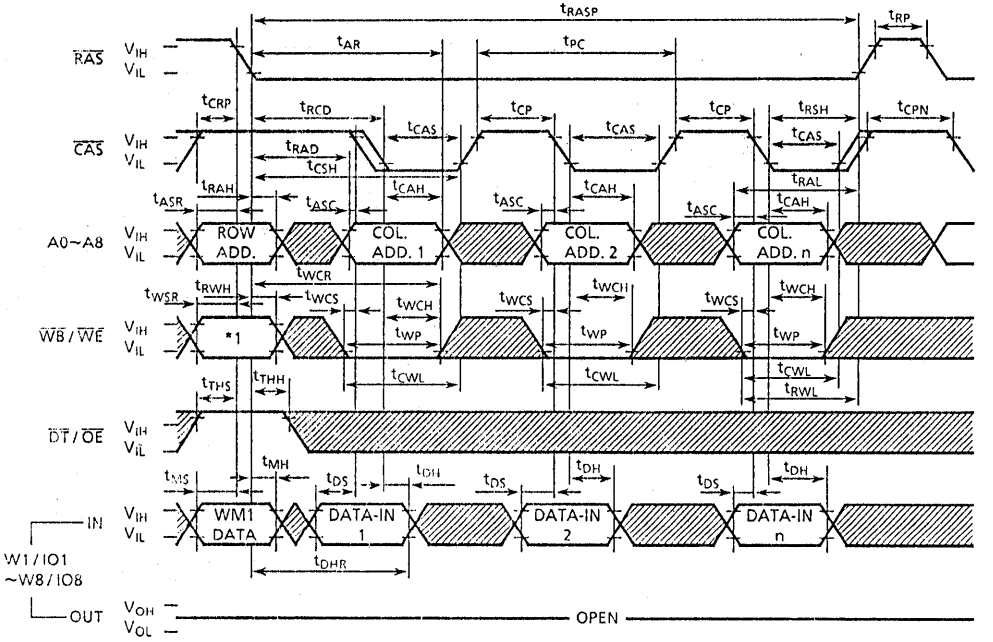
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



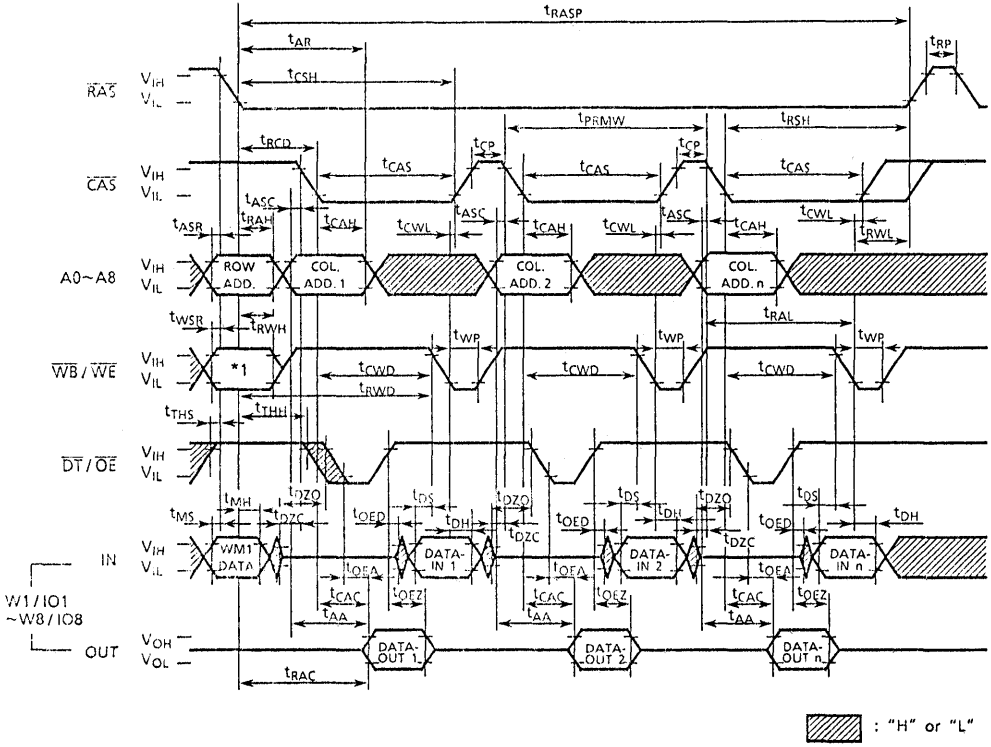
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

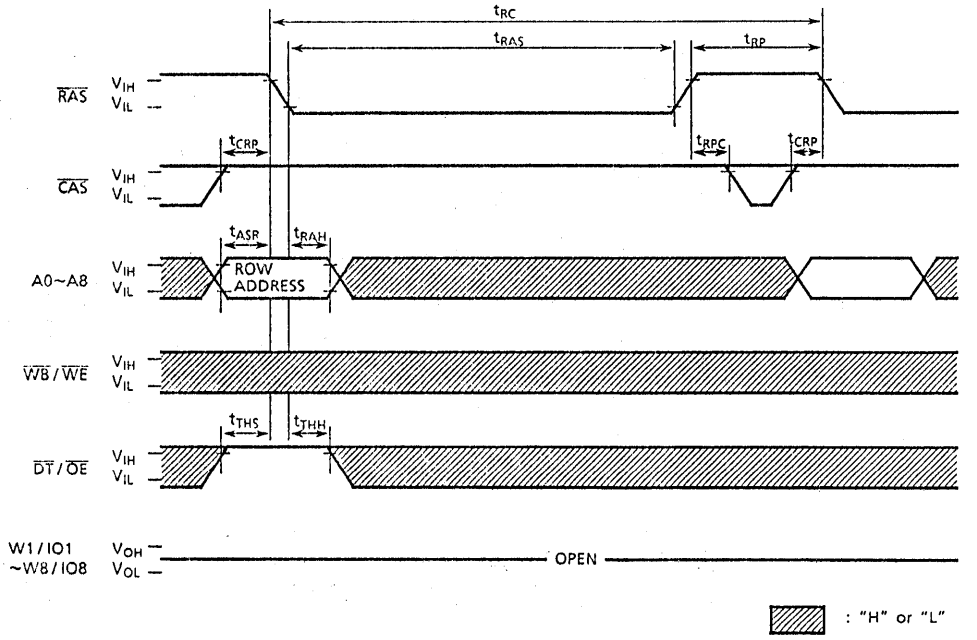
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



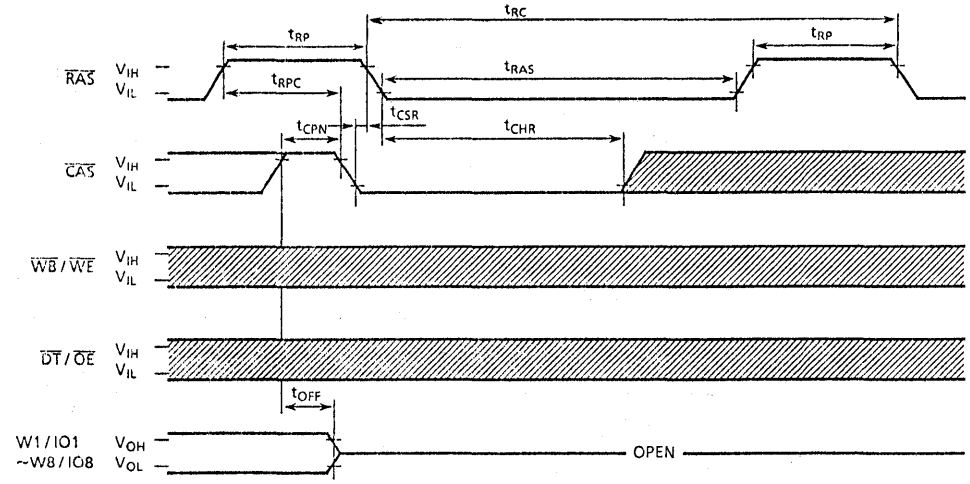
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

$\overline{RAS}$ ONLY REFRESH CYCLE



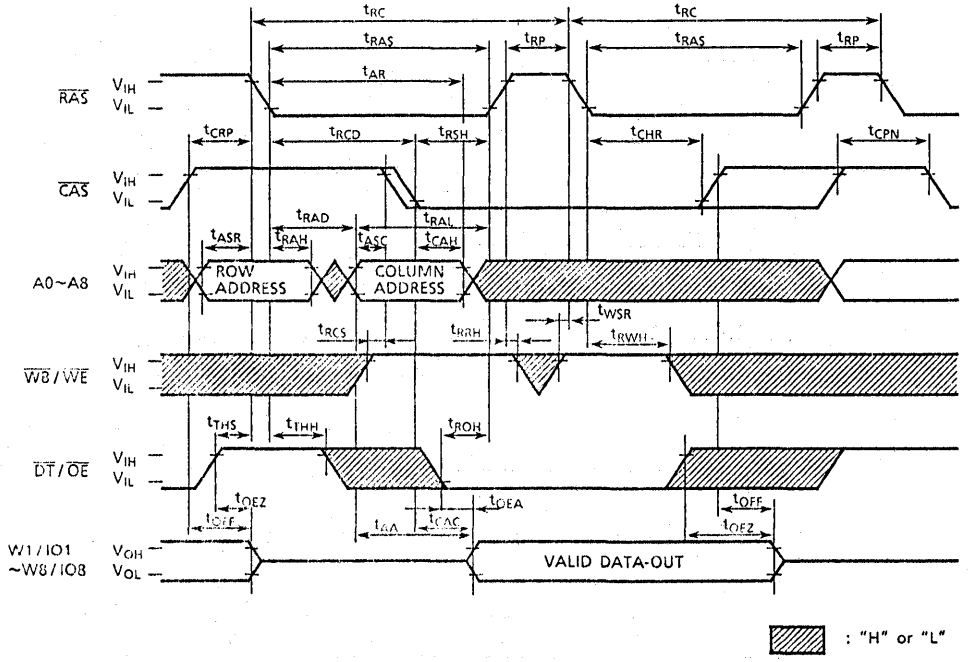
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



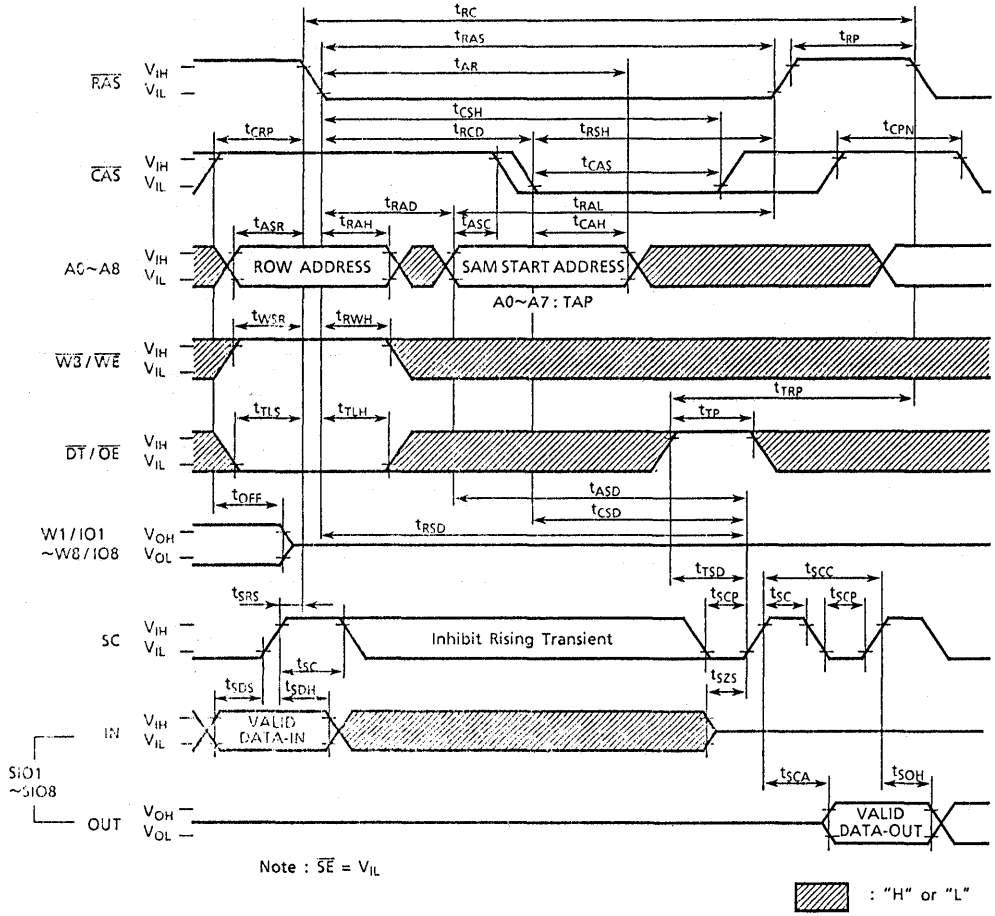
Note : A0 – A8 = Don't Care ("H" or "L")

: "H" or "L"

HIDDEN REFRESH CYCLE



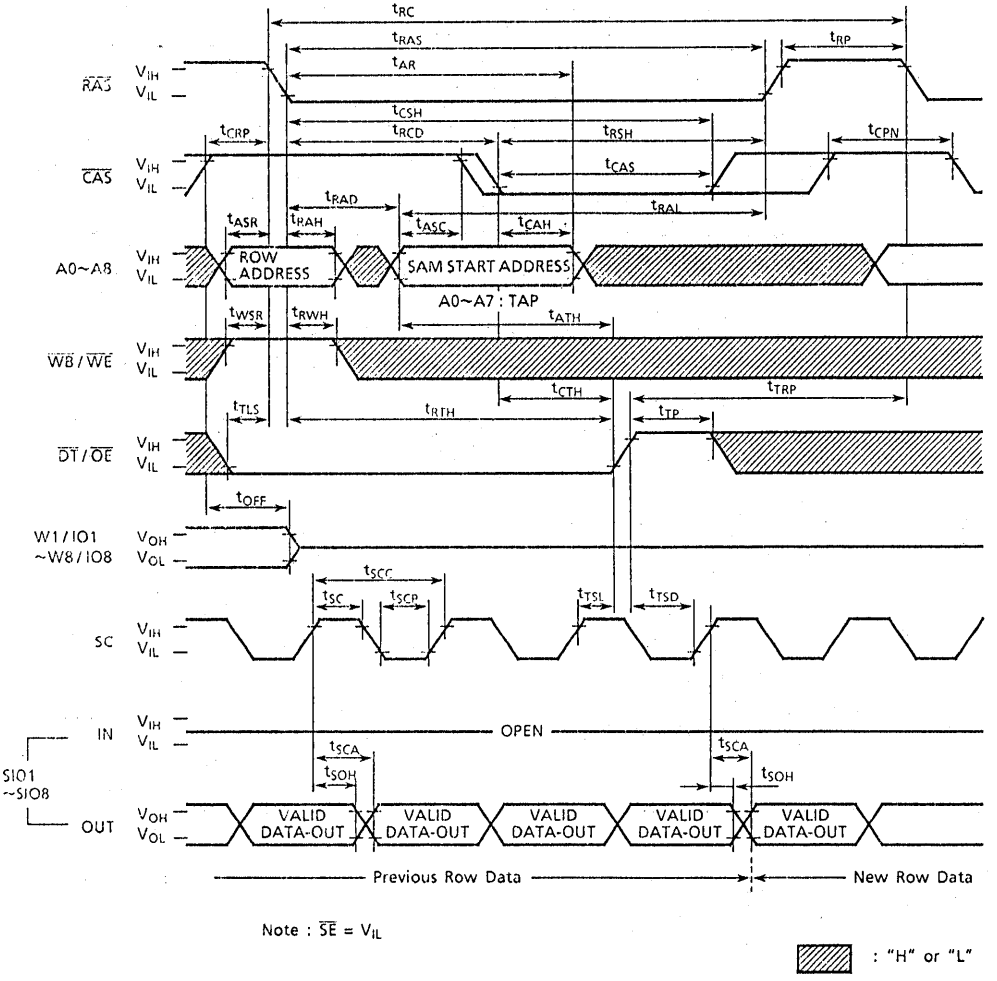
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

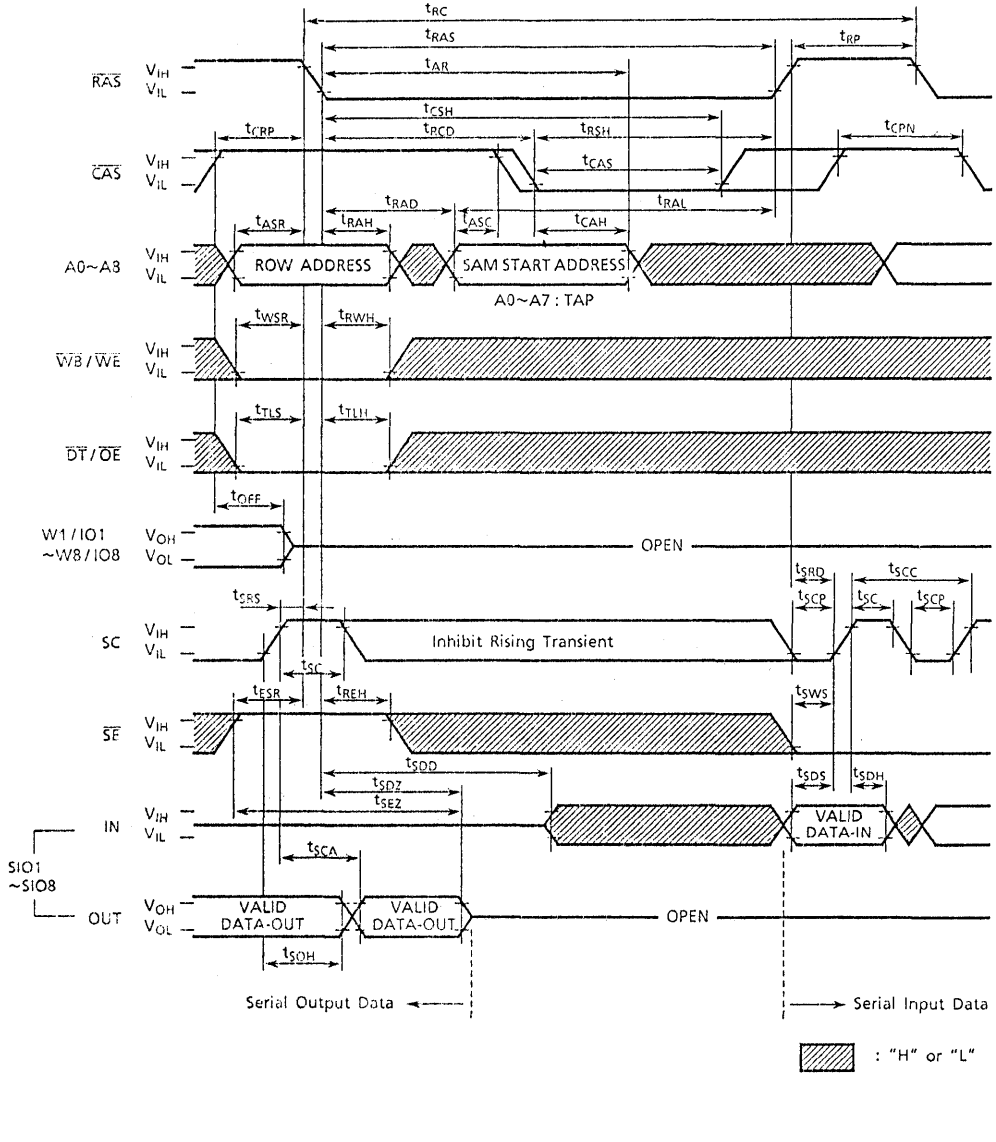
REAL TIME READ TRANSFER CYCLE



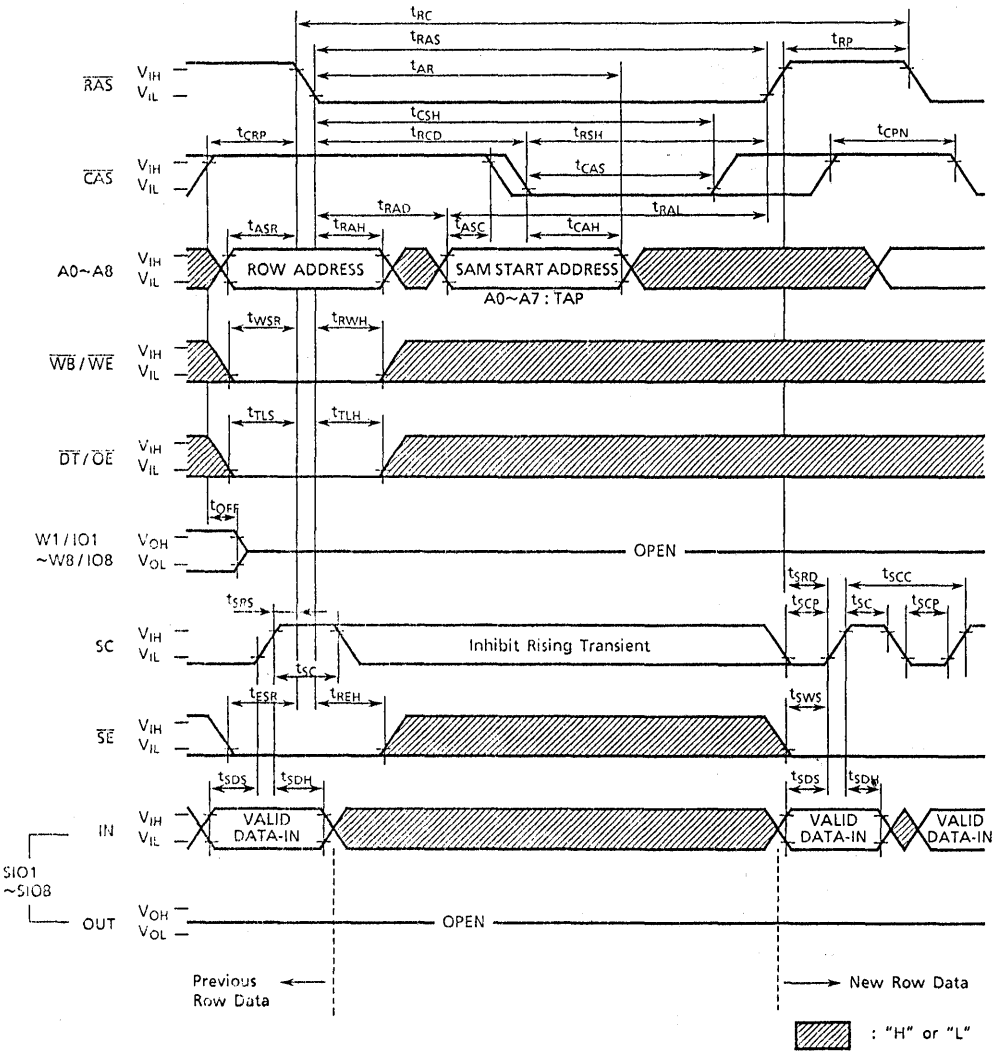
Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

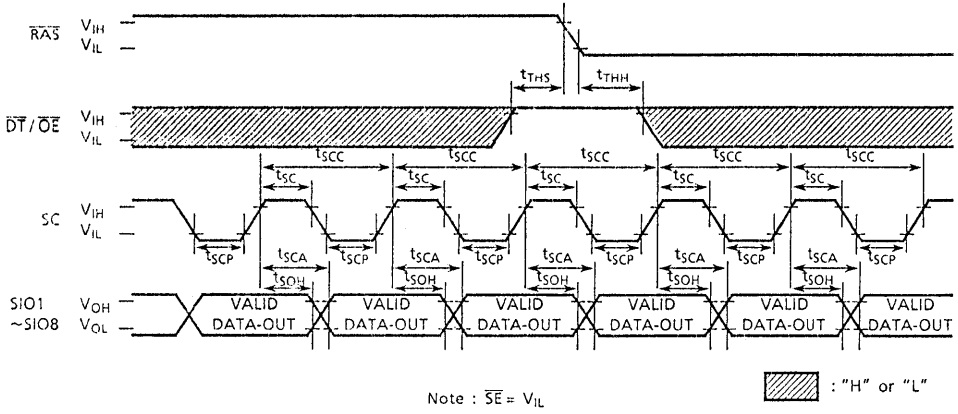
PSEUDO WRITE TRANSFER CYCLE



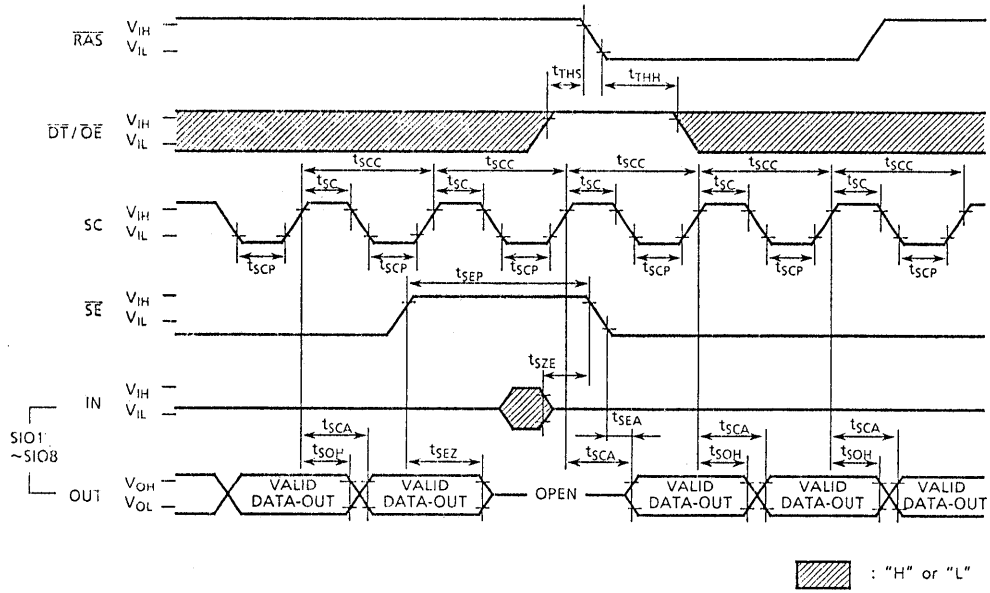
WRITE TRANSFER CYCLE



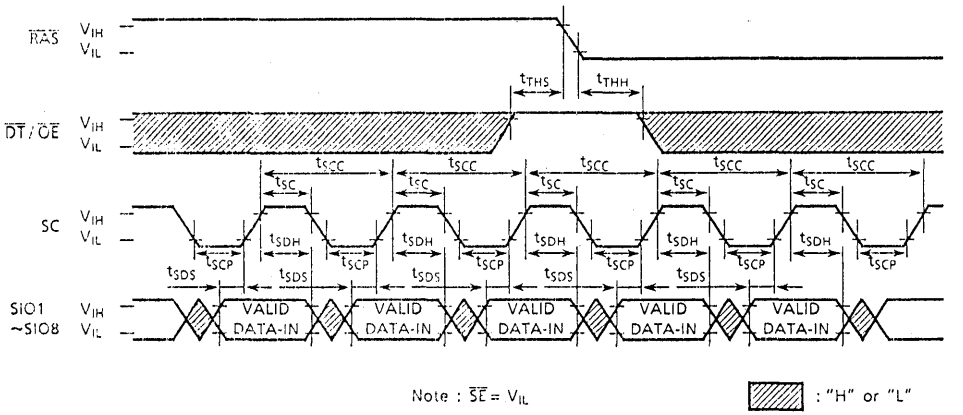
SERIAL READ CYCLE ($\overline{SE}$=V_{IL})



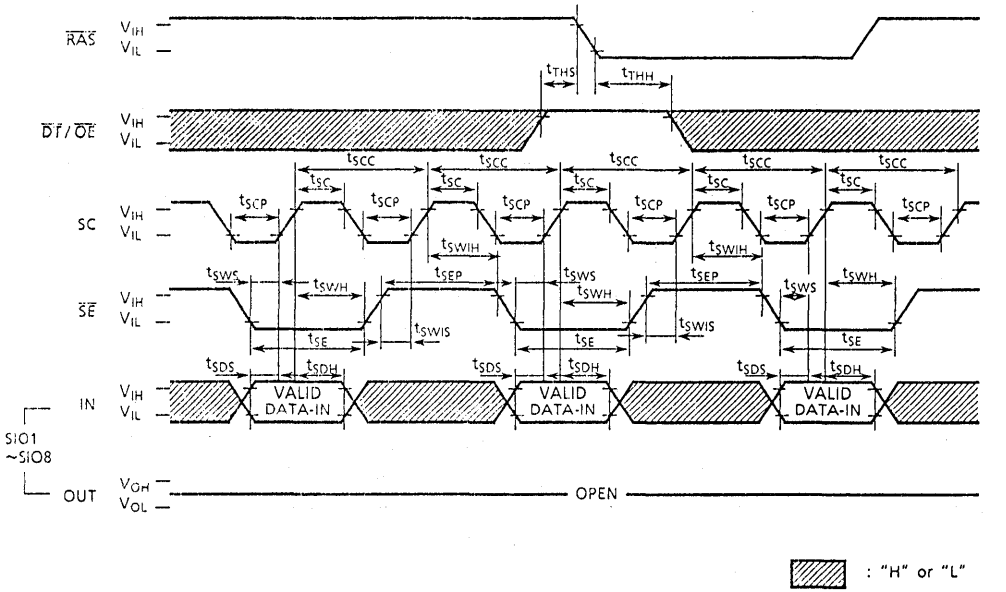
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC528126BJ/EZ are multiplexed onto 9 address input pins ($A_0 \sim A_8$). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ to invoke the various random access and data transfer operating modes shown in Table 2.
$\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

WRITE MASK DATA/DATA INPUT AND OUTPUT : $W_1/IO_1 \sim W_8/IO_8$

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read transfer/pseudo write transfer/write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SERIAL INPUT/OUTPUT : SIO1~SIO8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC528126BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{RAS}$ falling edge ↓				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh
1	0	0	0	Write Transfer
1	0	0	1	Pseudo Write Transfer
1	0	1	*	Read Transfer
1	1	0	*	Read/Write per Bit
1	1	1	*	Read/Write

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓				Address		W/IO		Write Mask
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓	WM1
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	–
Write Transfer	1	0	0	0	Row	TAP	*	*	–
Pseudo Write Transfer	1	0	0	1	Row	TAP	*	*	–
Read Transfer	1	0	1	*	Row	TAP	*	*	–
Write per Bit	1	1	0	*	Row	Column	WM1	DIN	Load use
Read/Write	1	1	1	*	Row	Column	*	DIN	–

* : "0" or "1" , TAP : SAM start address , – : not used

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC528126BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

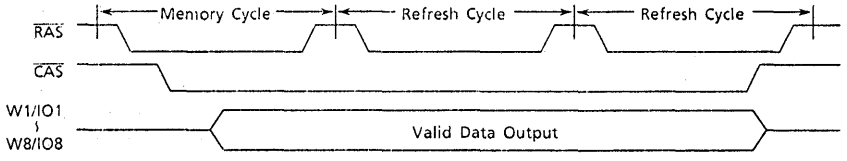


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When a "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i = 1~8)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

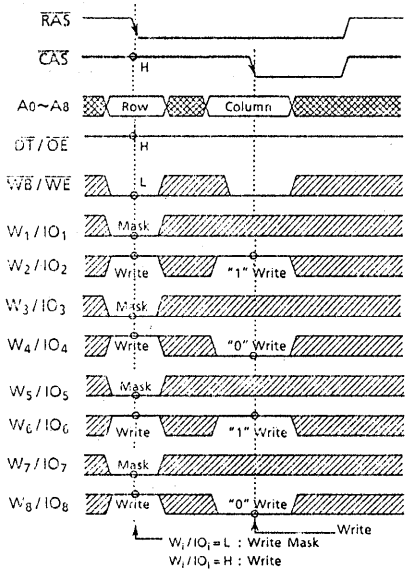


Figure 2. Write-per-bit timing cycle

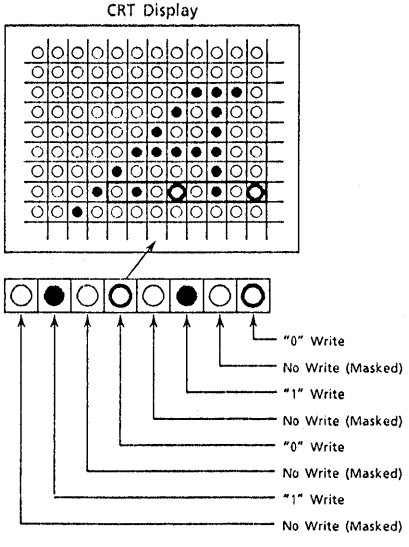
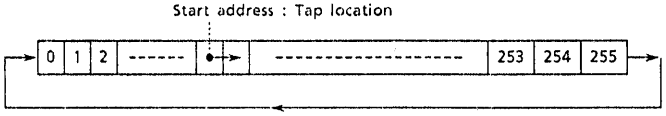


Figure 3. Corresponding bit-map

SAM PORT OPERATION

The TC528126BJ/BZ is provided with a 256 words by 8 bits serial access memory (SAM). High speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read transfer/write transfer/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC528126BJ/BZ features internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 4. During a transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).

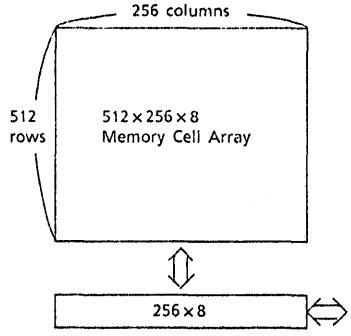


Figure 4. Data Transfer

As shown in Table 5, the TC528126BJ/BZ supports three types of transfer operations: Read transfer, Write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ latched at the falling edge of $\overline{RAS}$. During data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/Pseudo write transfer). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_7 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$				Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$				
H	L	H	*	Read Transfer	RAM → SAM	256×8	Input → Output
H	L	L	L	Write Transfer	SAM → RAM	256×8	Output → Input
H	L	L	H	Pseudo Write Transfer	-	-	Output → Input

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" and $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 5 shows the operation block diagram for read transfer operation.

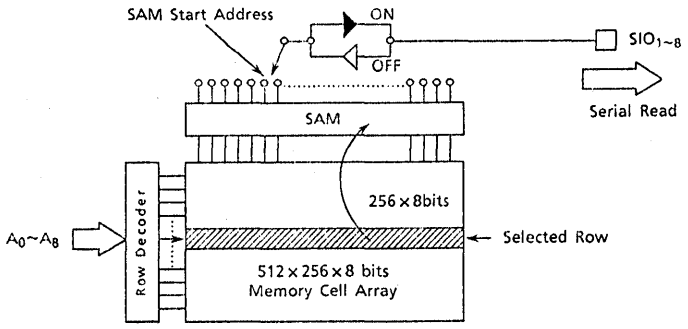


Figure 5. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 6.

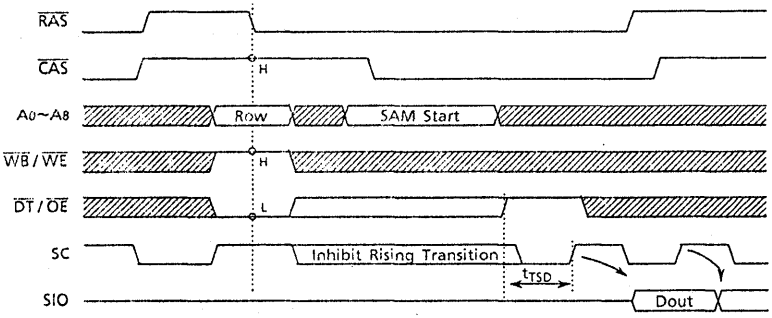


Figure 6. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 7.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min.

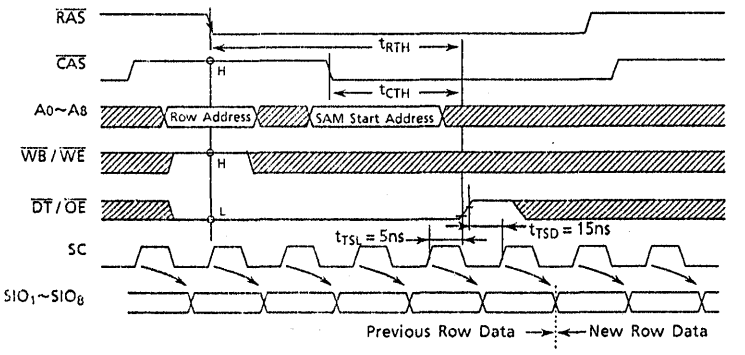


Figure 7. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "low" at the falling edge of $\overline{RAS}$.

Figure 8 and 9 show the timing diagram and block diagram for write transfer operations, respectively.

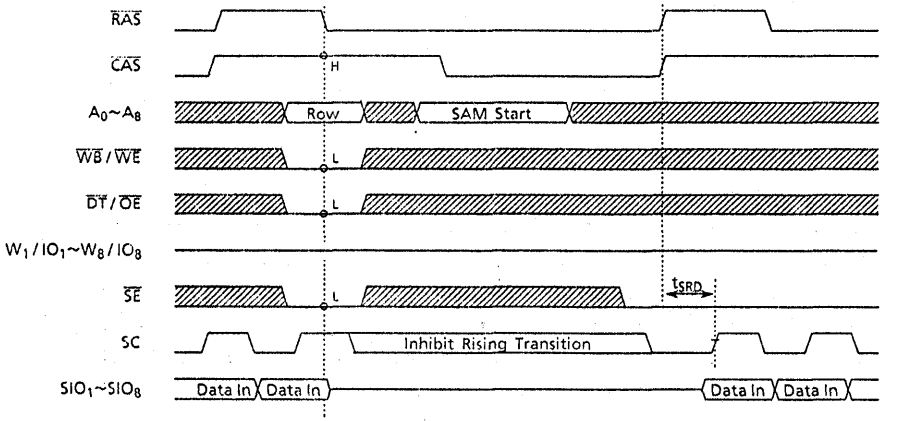


Figure 8. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

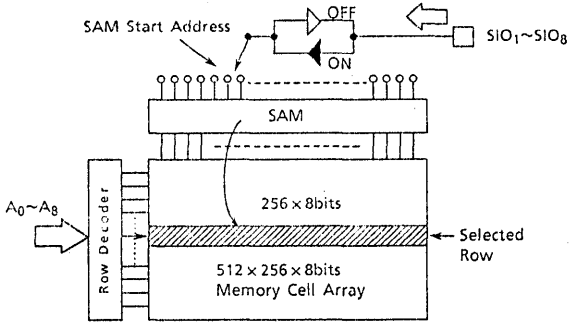


Figure 9. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

REGISTER OPERATION SEQUENCE (EXAMPLE)

Figure 10 illustrates an example of register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255) and wraps around to the least significant address location. The SAM address is incremented as long as SC is clocked.

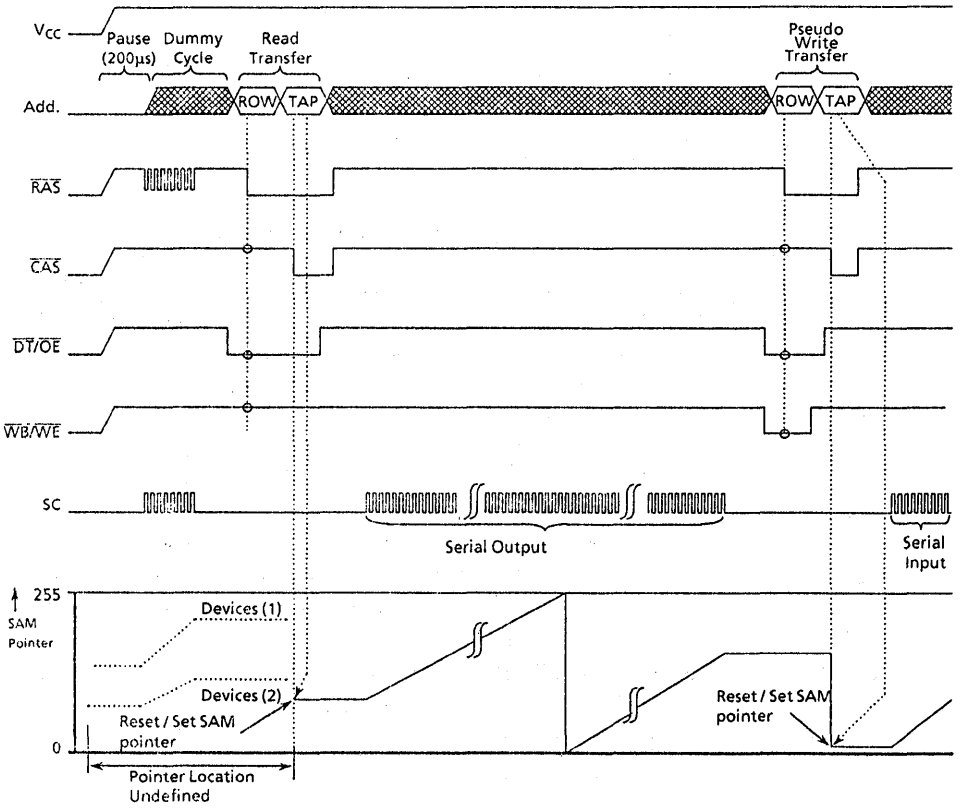
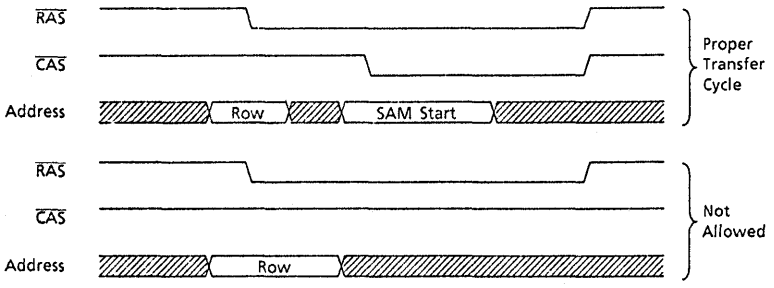


Figure 10. Example of SAM Register Operation Seguence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

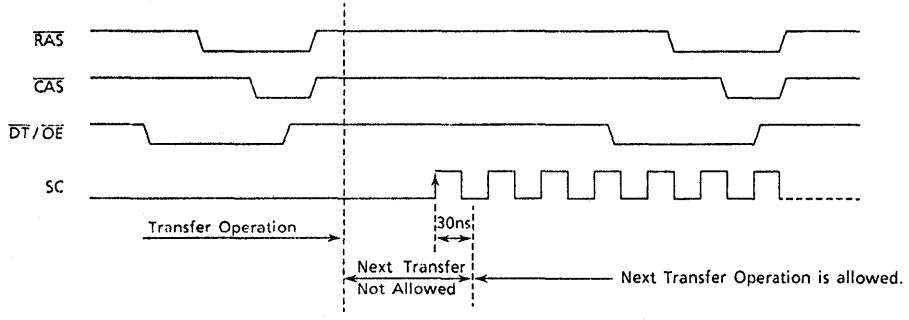
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



READ TRANSFER CYCLE AFTER READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528126BJ/BZ is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
WM1 Register	Write Enable
TAP pointer	Invalid

131,072WORDS×8BITS MULTIPORT DRAM

PRELIMINARY

DESCRIPTION

The TC528128BJ/BZ is a CMOS multiport memory equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The TC528128BJ/BZ supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport video RAM operating modes, the TC528128BJ/BZ features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port. The TC528128BJ/BZ is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC52812 BJ/BZ -80	-10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	90mA	75mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

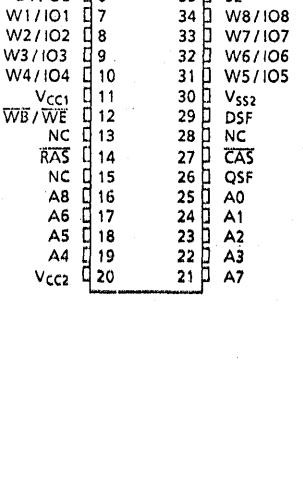
- Organization
  - RAM Port : 131,072words×8bits
  - SAM Port : 256words×8bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - Flash Write, Block Write
  - 512 refresh cycles/8ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 256 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read/Write Transfer
- Package
  - TC528128BJ : SOJ40-P-400
  - TC528128BZ : ZIP40-P-475

PIN NAME

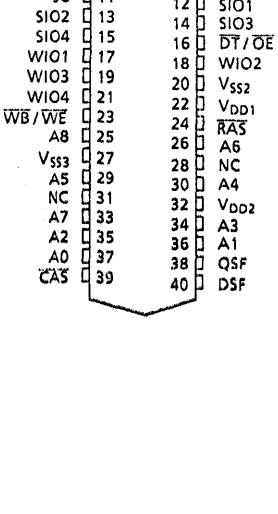
A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1~W8/IO8	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO8	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

PIN CONNECTION

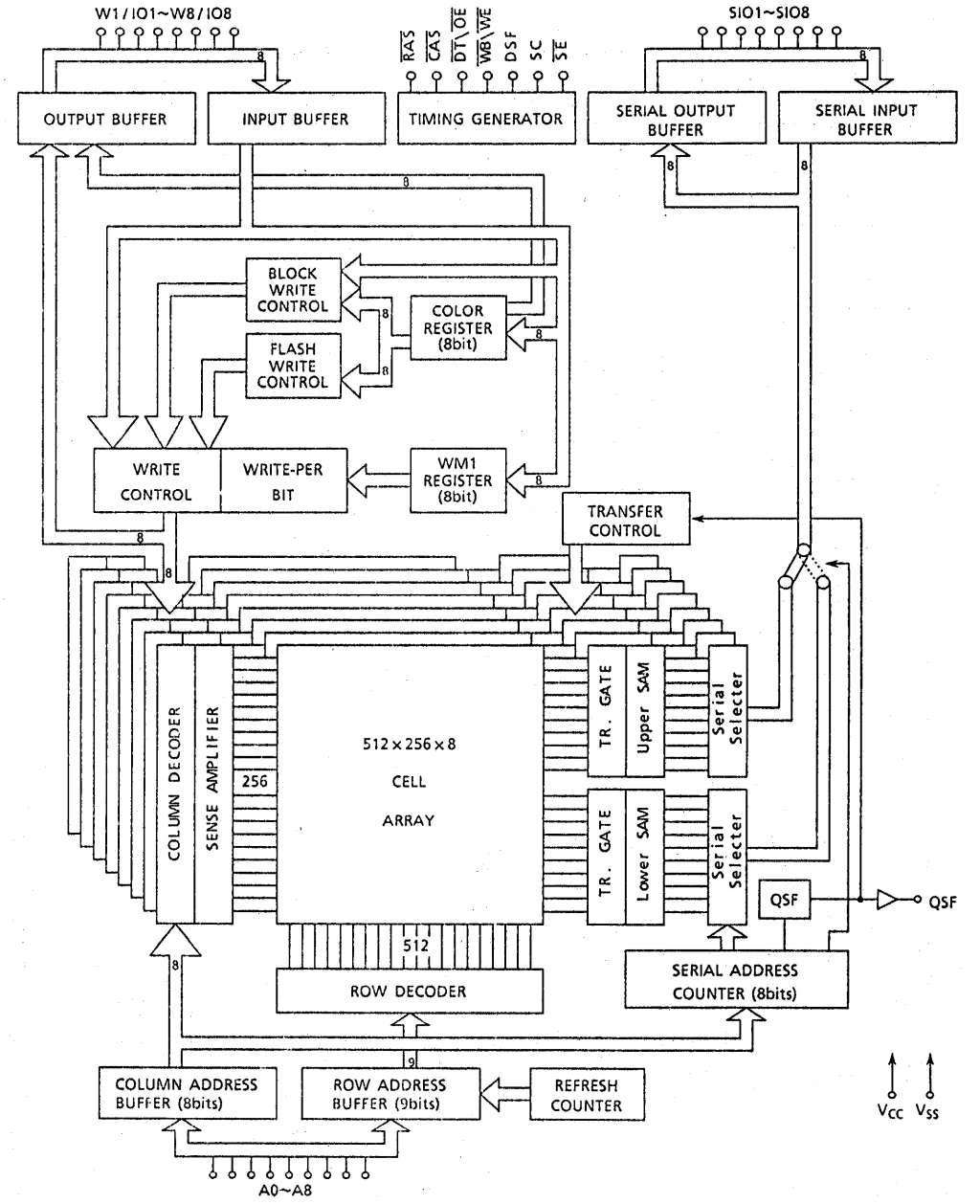
TC528128BJ



TC528128BZ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	−1.0~7.0	V	1
V_{CC}	Power Supply Voltage	−1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	−	7	pF
C_{IO}	Input/Output Capacitance	−	9	
C_O	Output Capacitance (QSF)	−	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC528128BJ/BZ-80		TC528128BJ/BZ-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	–	90	–	75	mA	3, 4
	Active	I_{CC1A}	–	130	–	115		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	–	90	–	75		3, 4
	Active	I_{CC3A}	–	130	–	115		3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Standby	I_{CC4}	–	80	–	65		3, 4
	Active	I_{CC4A}	–	120	–	105		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	–	90	–	75		3, 4
	Active	I_{CC5A}	–	130	–	115		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	–	110	–	95		3, 4
	Active	I_{CC6A}	–	150	–	135		3, 4
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC7}	–	100	–	75		3, 4
	Active	I_{CC7A}	–	130	–	115		3, 4
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC8}	–	100	–	85		3, 4
	Active	I_{CC8A}	–	140	–	125		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≦ V_{IN} ≦ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≦ V_{OUT} ≦ 5.5V, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = – 2mA	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC528128BJ/BZ-80		TC528128BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC528128BJ/BZ-80		TC528128BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130		ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{FSR}	DSF Set-UP Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	55		70			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

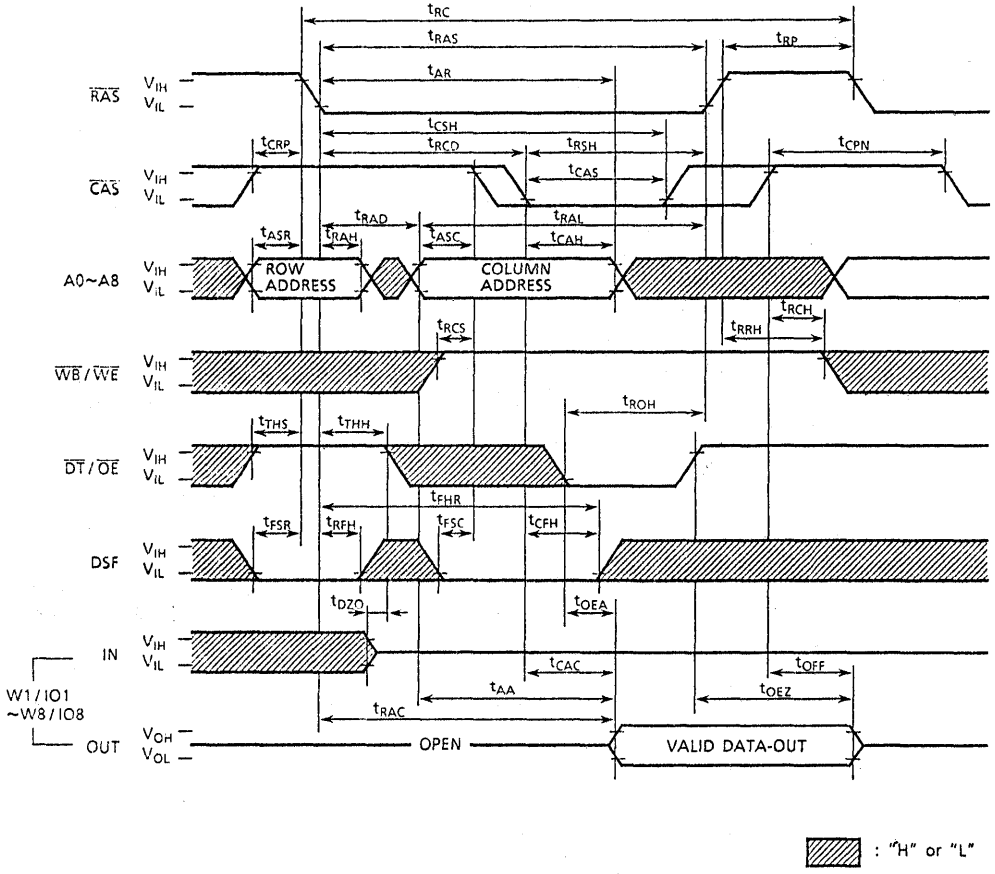
SYMBOL	PARAMETER	TC528128BJ/BZ-80		TC528128BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			
t_{STS}	Split Transfer Set-Up Time	30		30			
t_{STH}	Split Transfer Hold Time	30		30			
t_{SQD}	SC-QSF Delay Time		25		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		25		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		35		35		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		75		90		

NOTES :

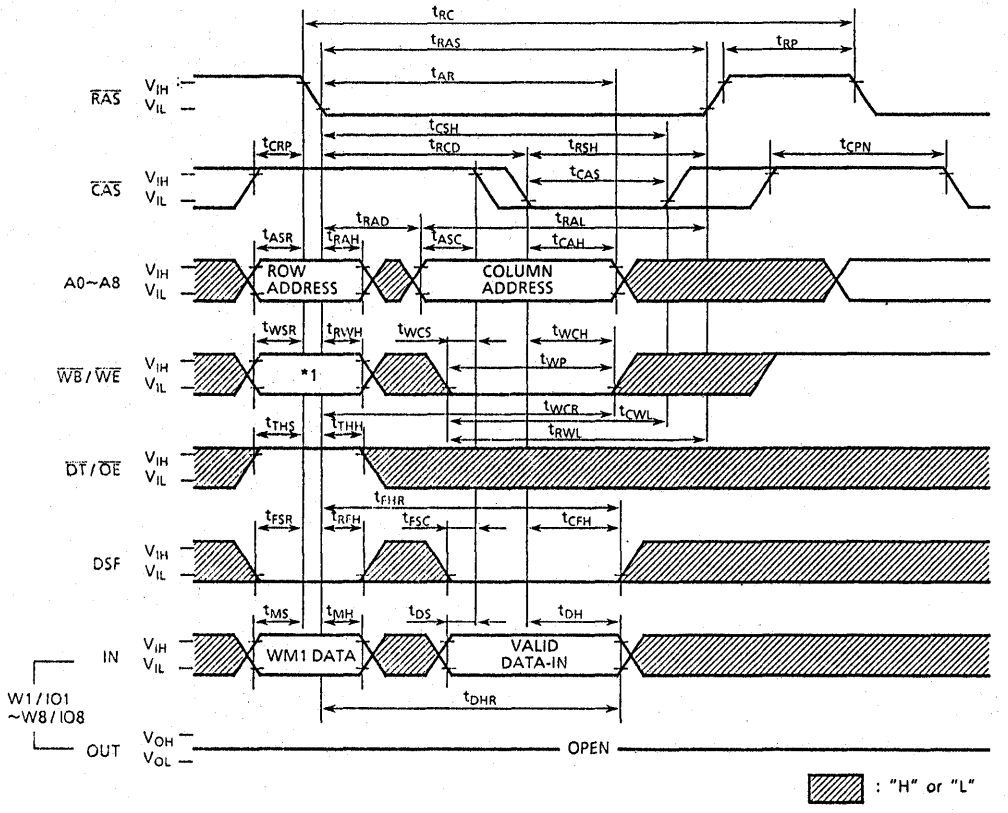
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}$/$\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$/$\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycle and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only : If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



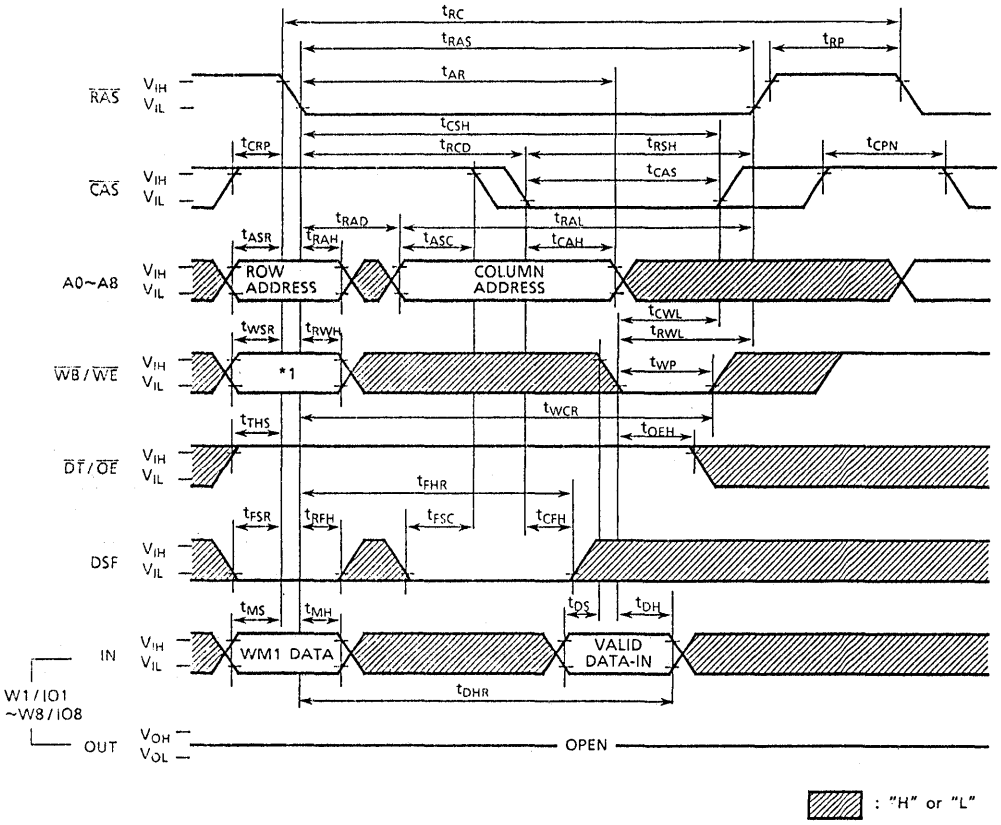
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

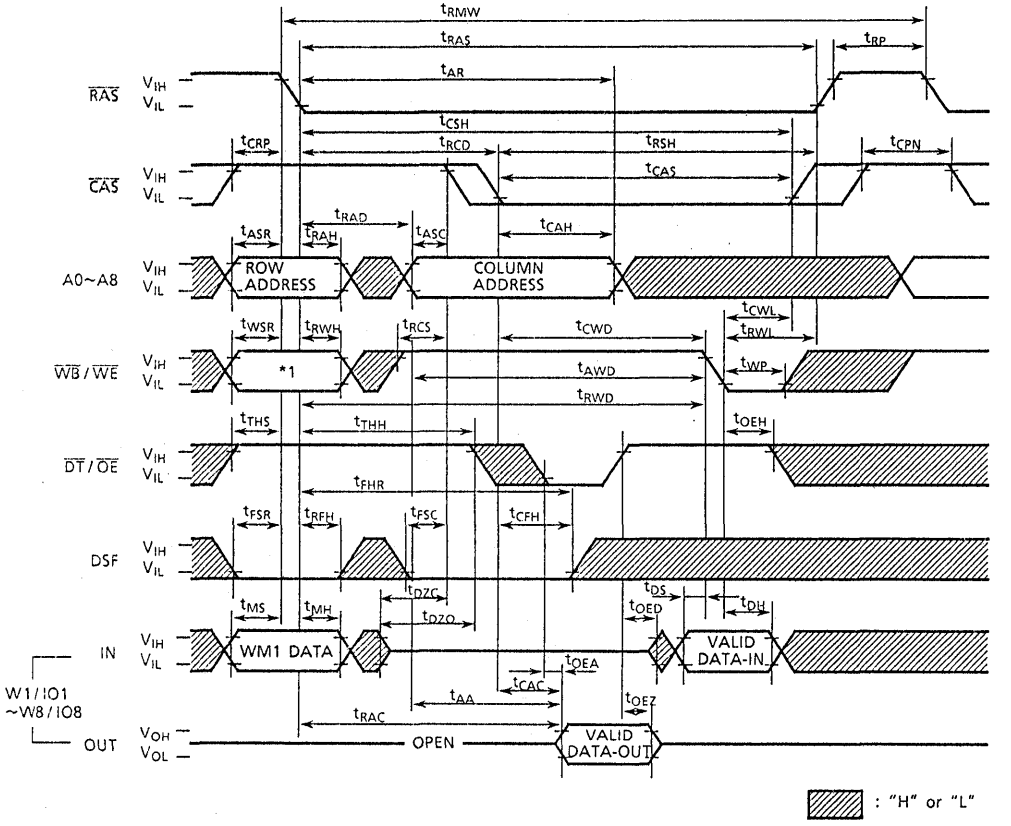
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

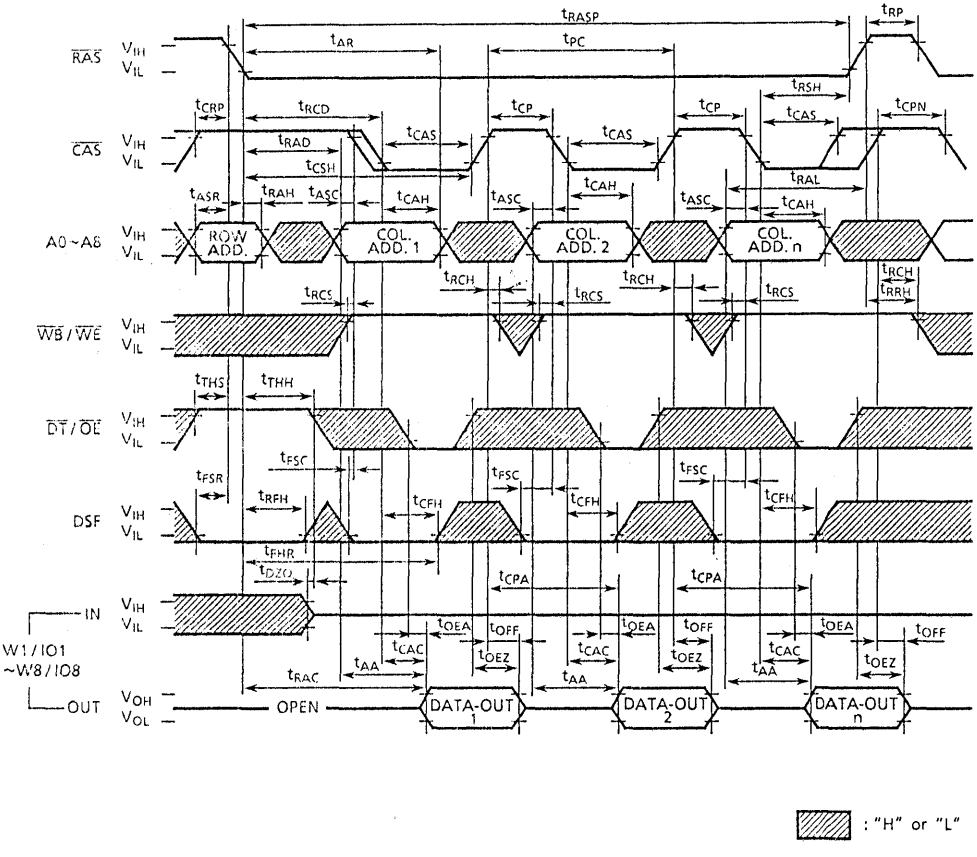
READ - MODIFY - WRITE CYCLE



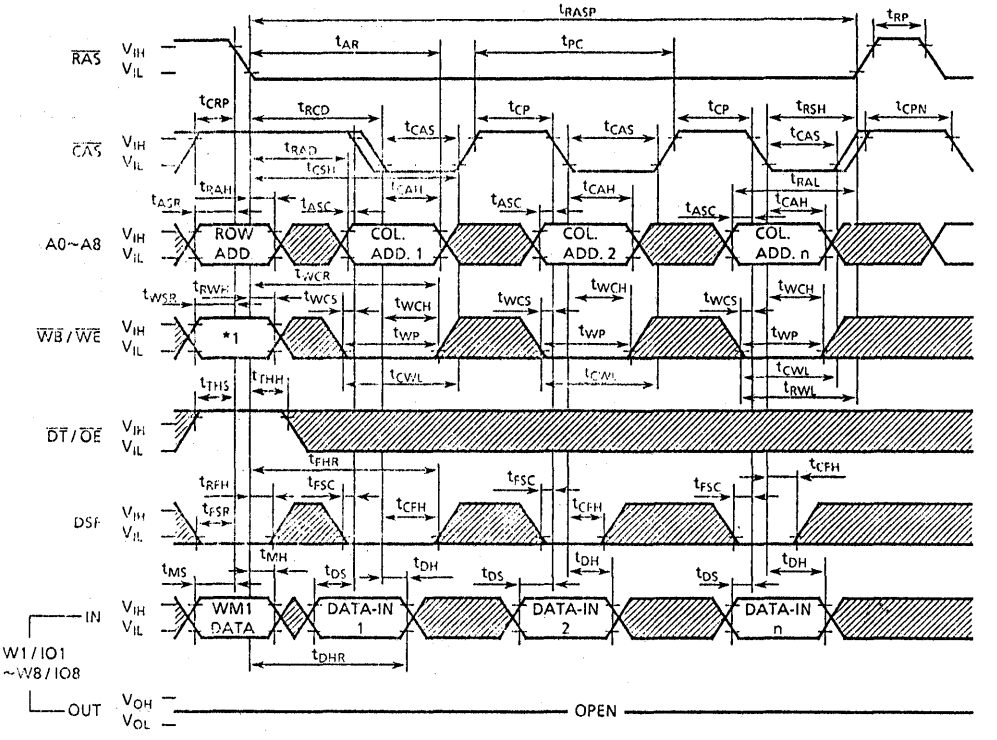
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



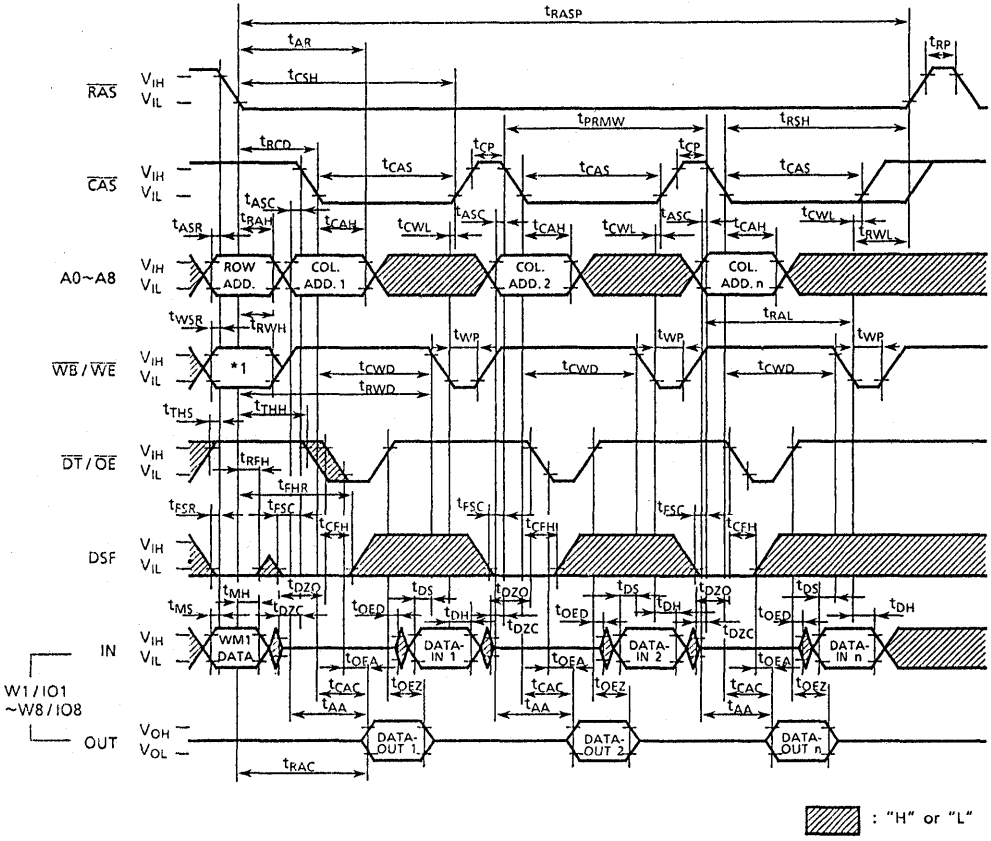
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

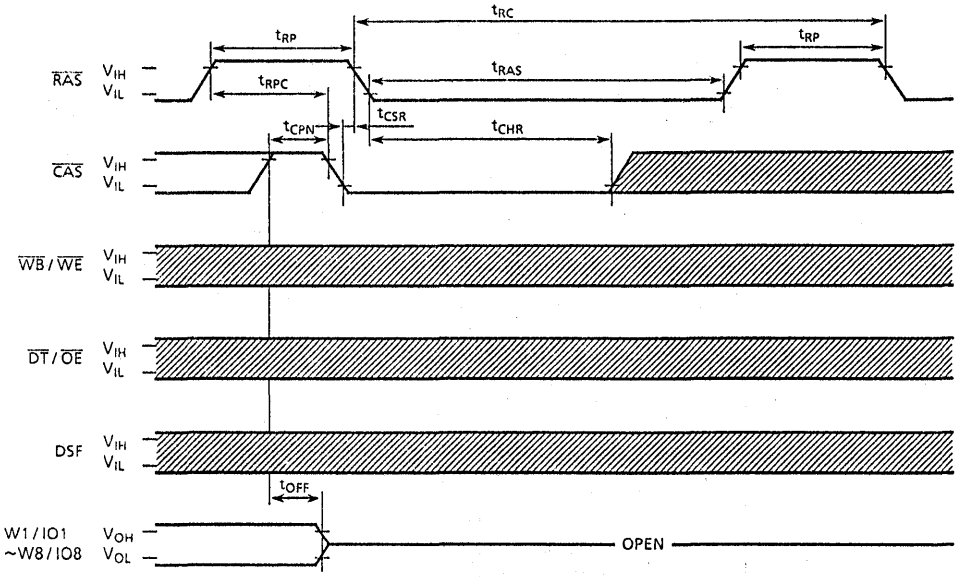
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W8 / IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

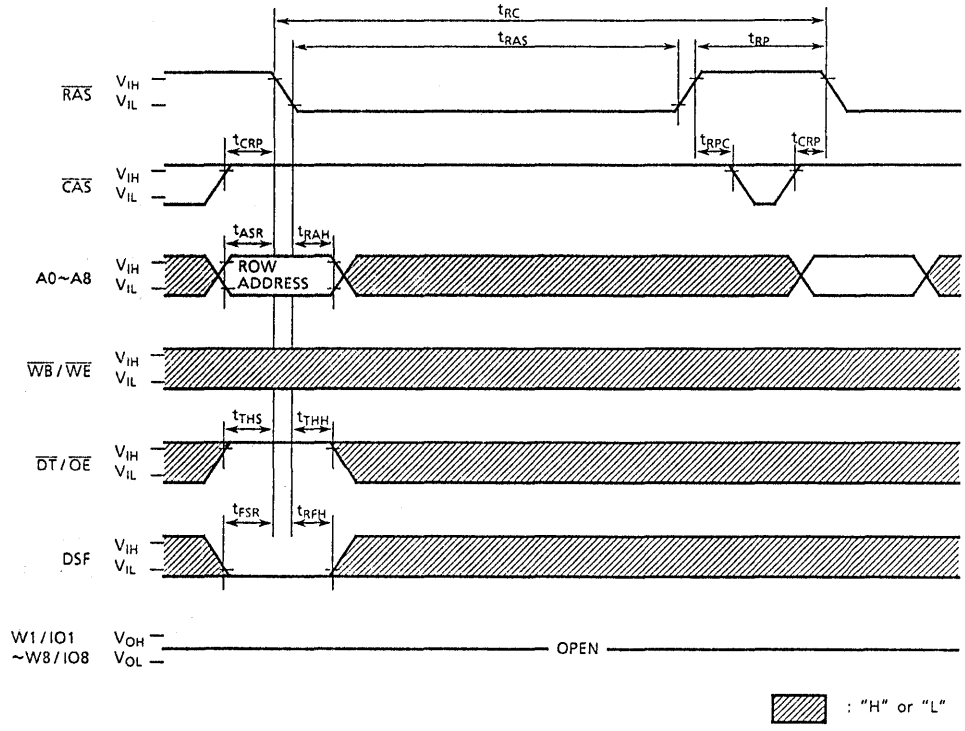
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



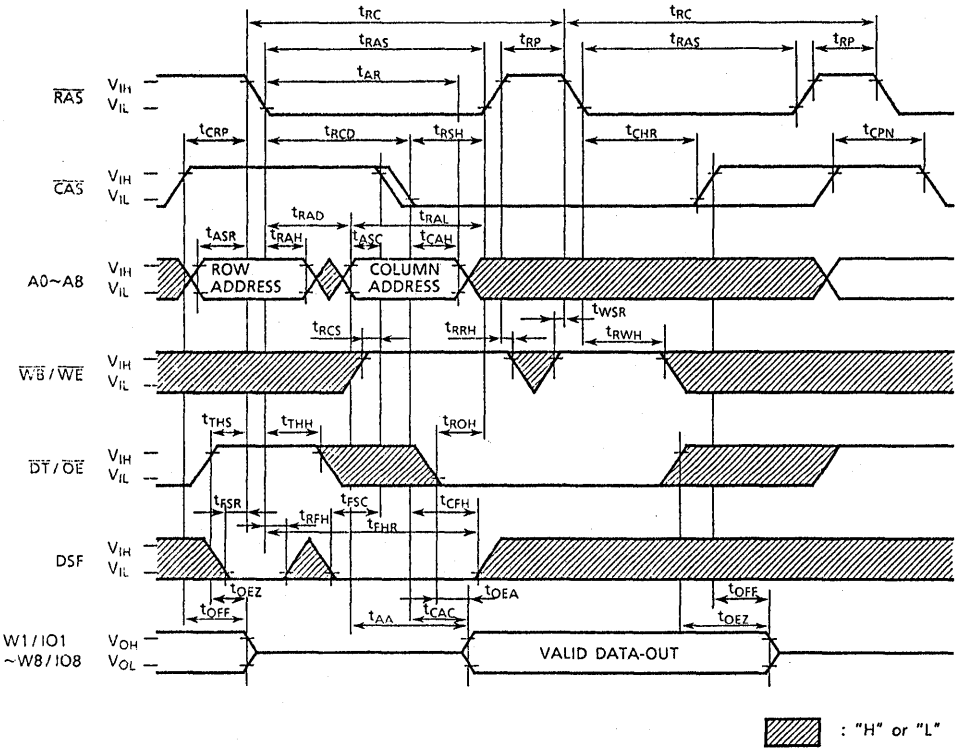
Note : A0 – A8 = Don't Care ("H" or "L")

: "H" or "L"

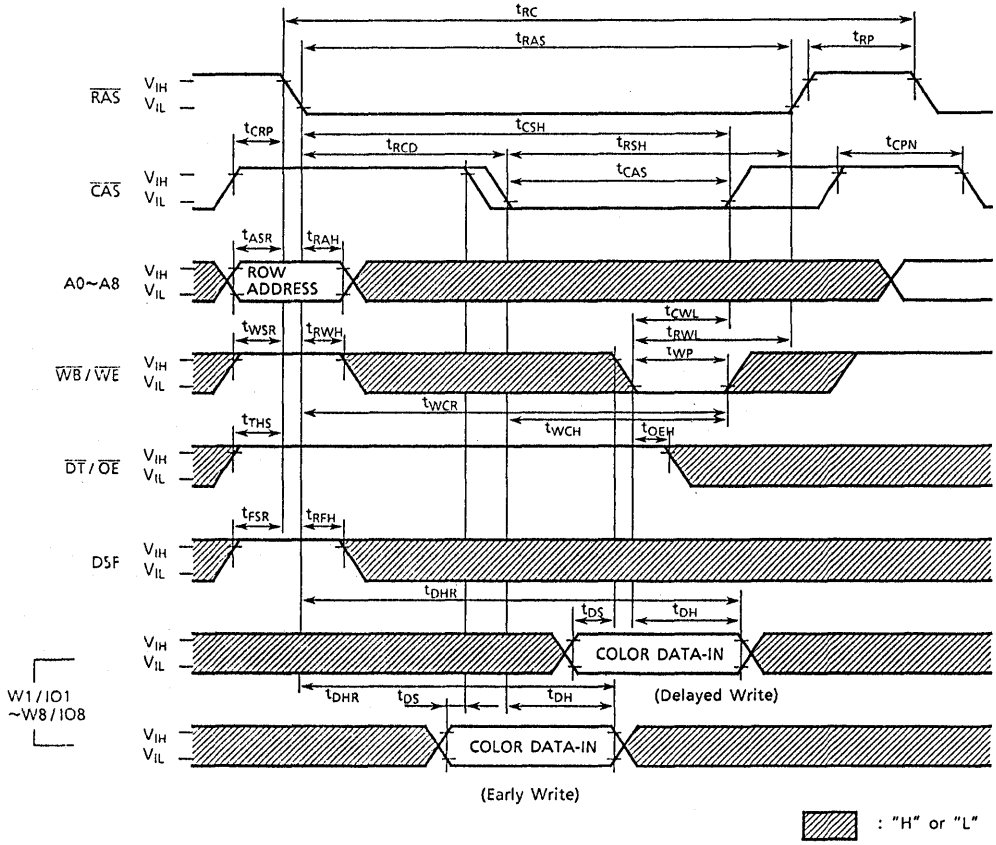
$\overline{RAS}$ ONLY REFRESH CYCLE



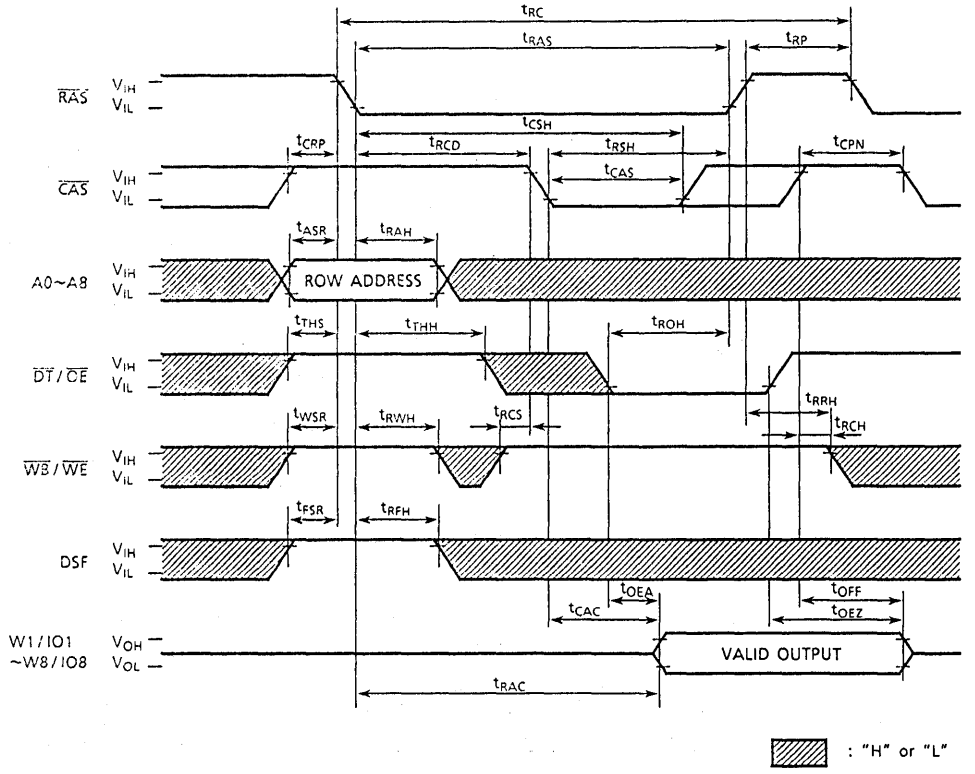
HIDDEN REFRESH CYCLE



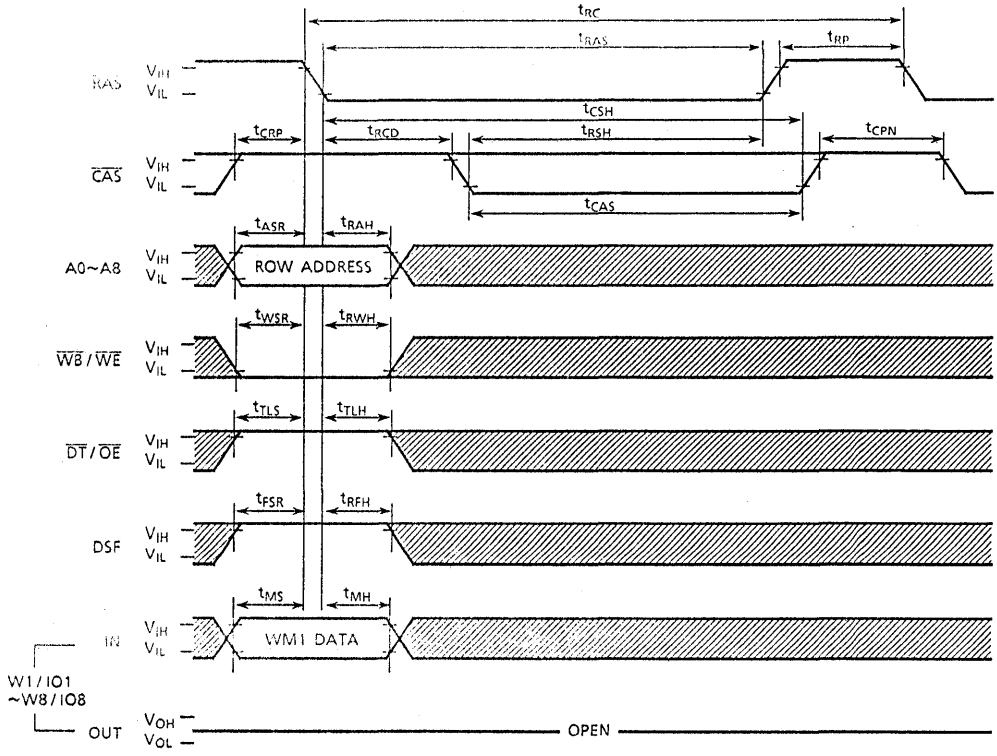
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE

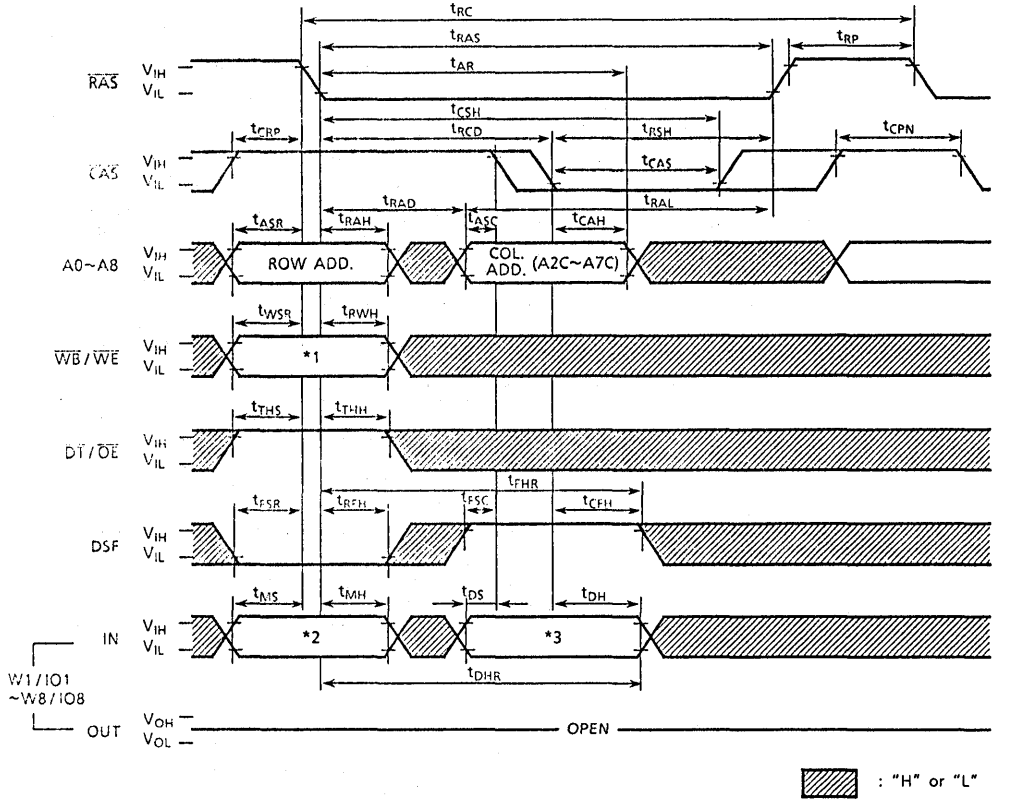


FLASH WRITE CYCLE



WM1 DATA	CYCLE
0	Flash Write Disable
1	Flash Write Enable

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W8/IO8	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

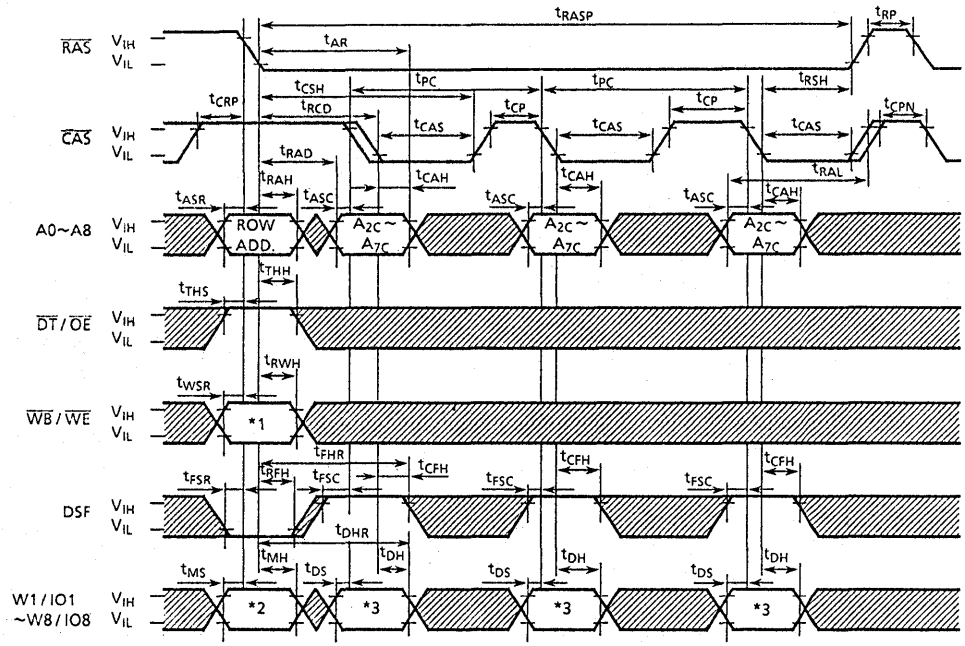
WM1 data: 0: Write Disable
1: Write Enable

*3) COLUMN SELECT

W1/IO1 — Column 0 ($A_{1C}=0$, $A_{0C}=0$)
W2/IO2 — Column 1 ($A_{1C}=0$, $A_{0C}=1$)
W3/IO3 — Column 2 ($A_{1C}=1$, $A_{0C}=0$)
W4/IO4 — Column 3 ($A_{1C}=1$, $A_{0C}=1$)

Wn/IOn
= 0 : Disable
= 1 : Enable

PAGE MODE BLOCK WRITE CYCLE



: "H" or "L"

*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W8/IO8	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

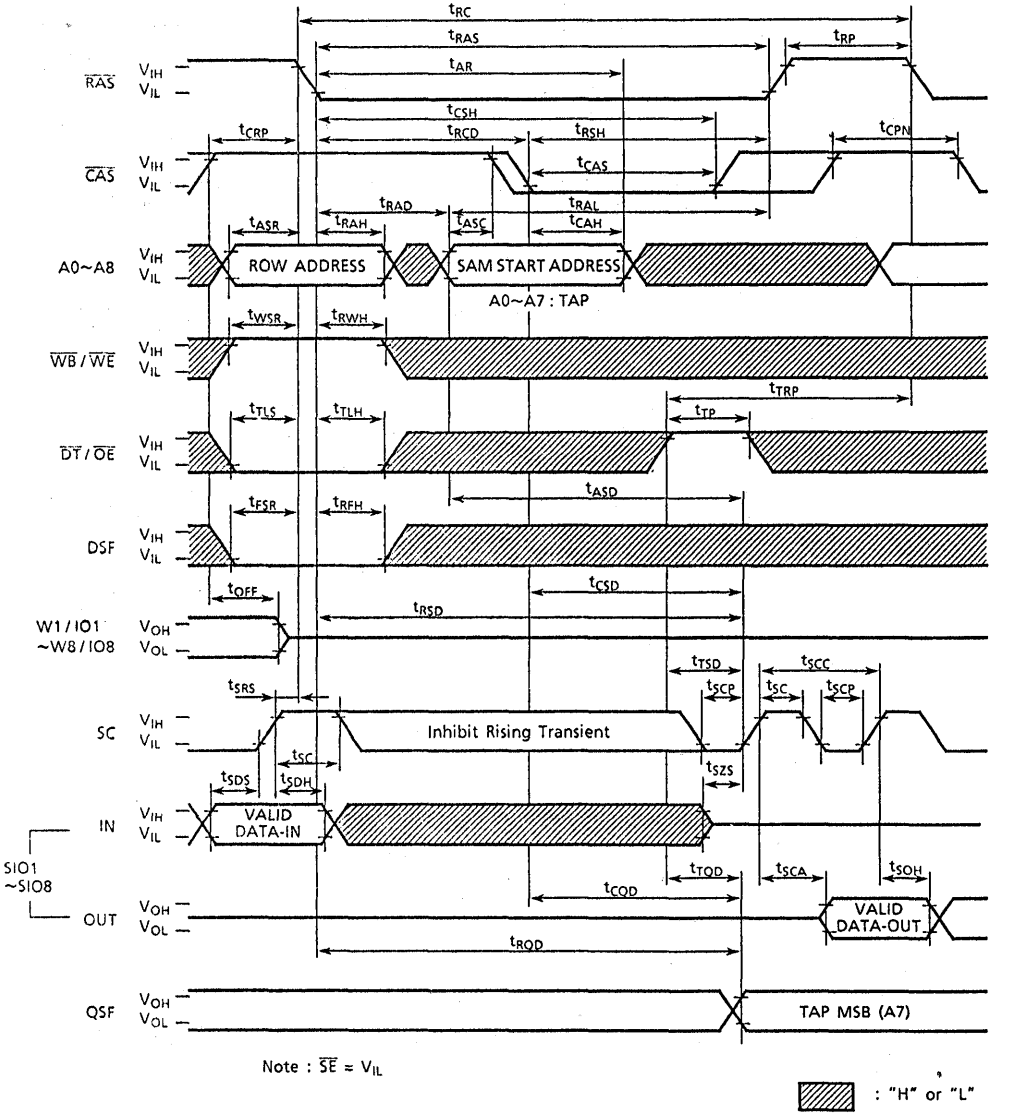
WM1 data : 0 : Write Disable
1 : Write Enable

*3) COLUMN SELECT

W1/IO1 – Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 – Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 – Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 – Column 3 (A_{1C} = 1, A_{0C} = 1)

} Wn/IOn
= 0 : Disable
= 1 : Enable

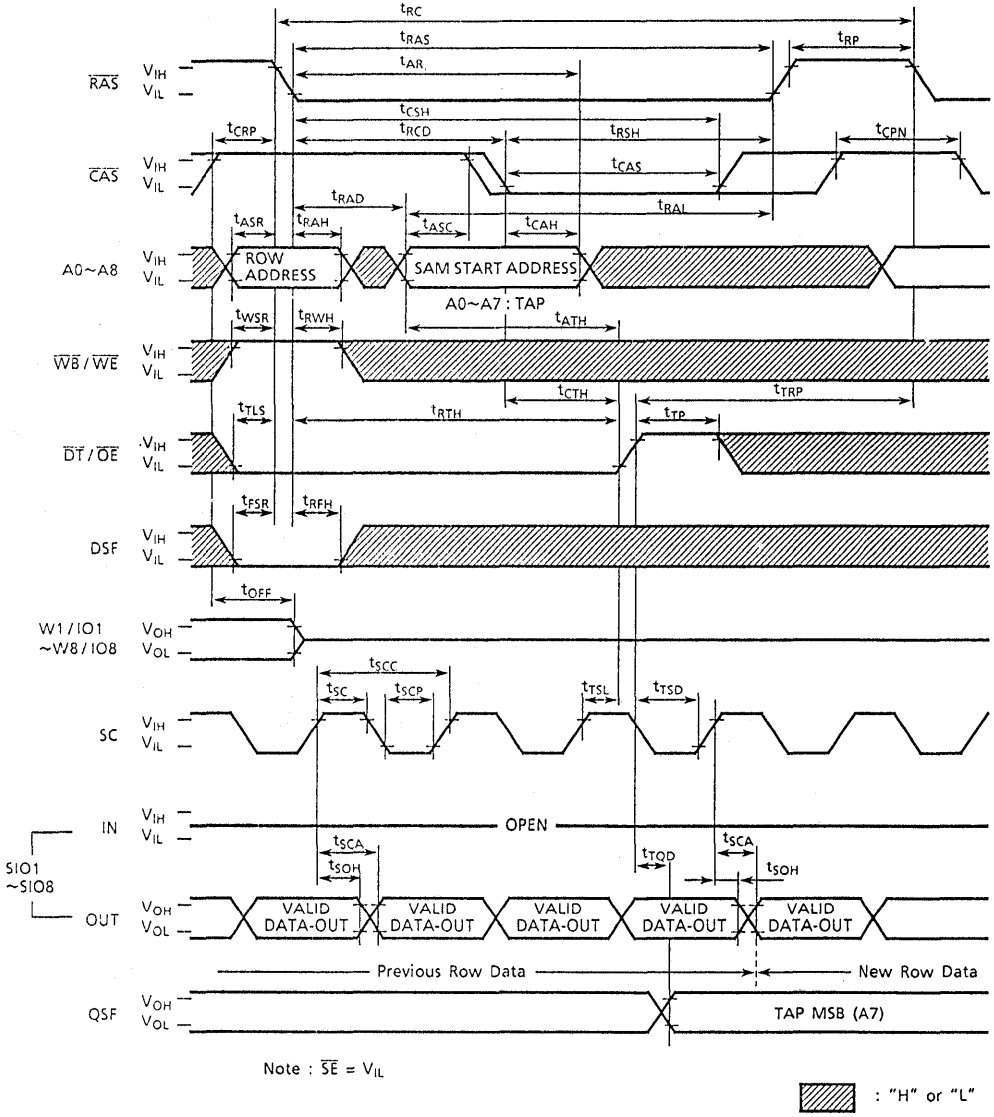
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



Note : $\overline{SE} \geq V_{IL}$

: "H" or "L"

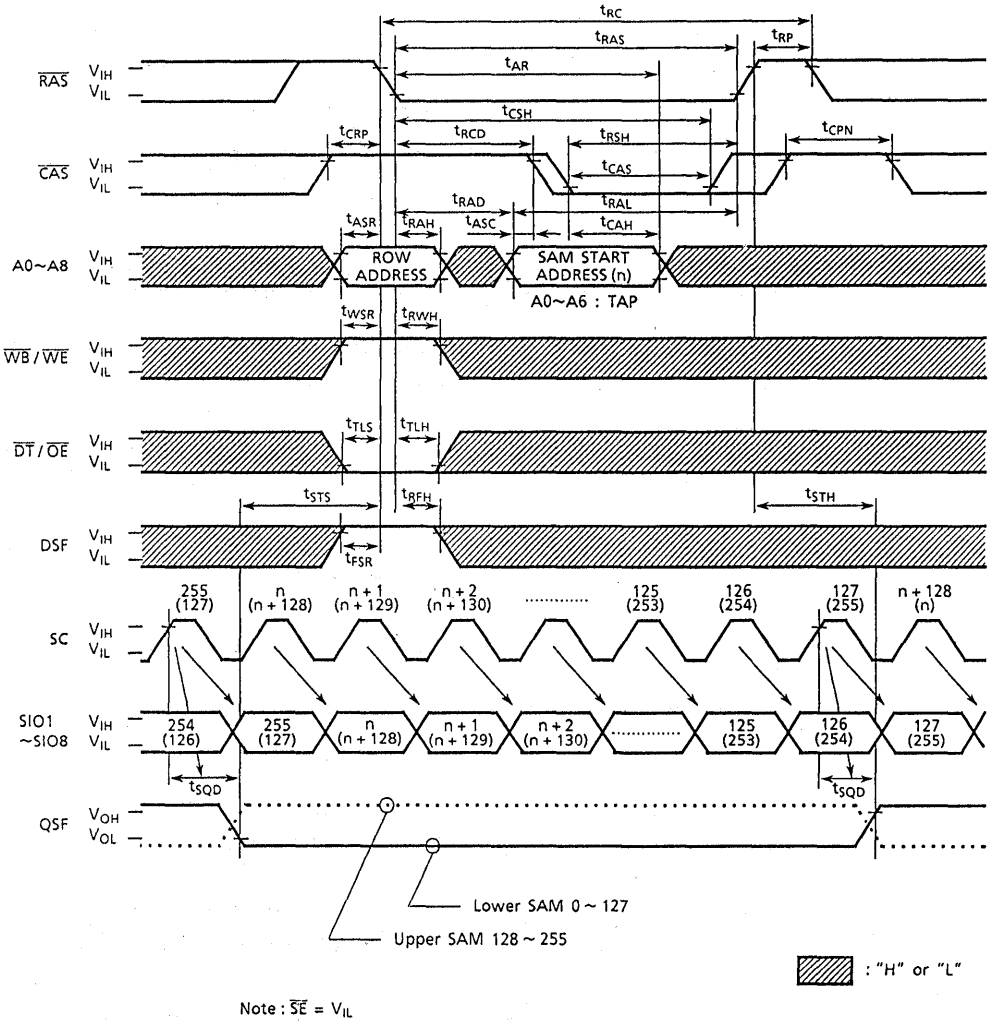
REAL TIME READ TRANSFER CYCLE



Note : $\overline{SE}$ = V_{IL}

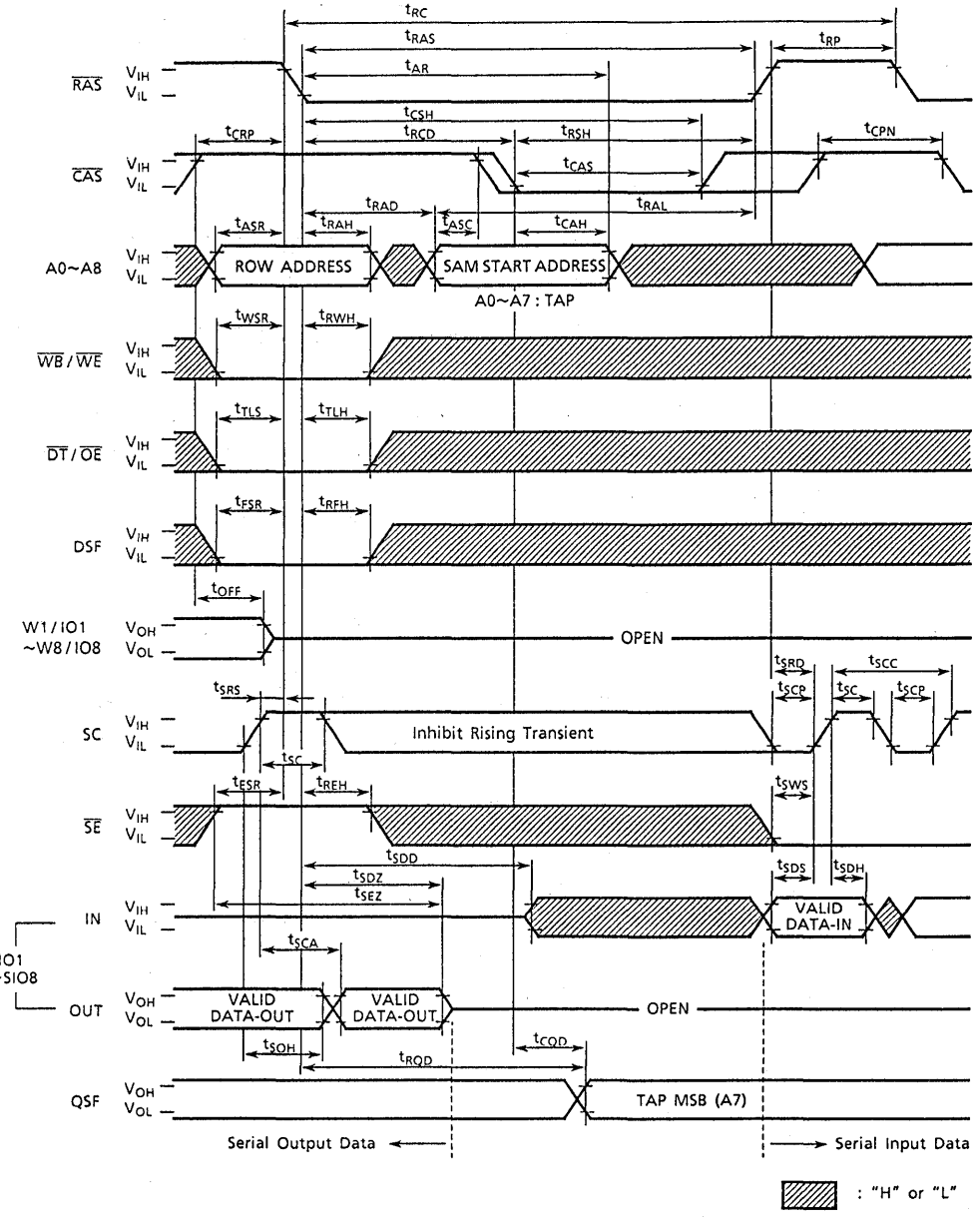
: "H" or "L"

SPLIT READ TRANSFER CYCLE

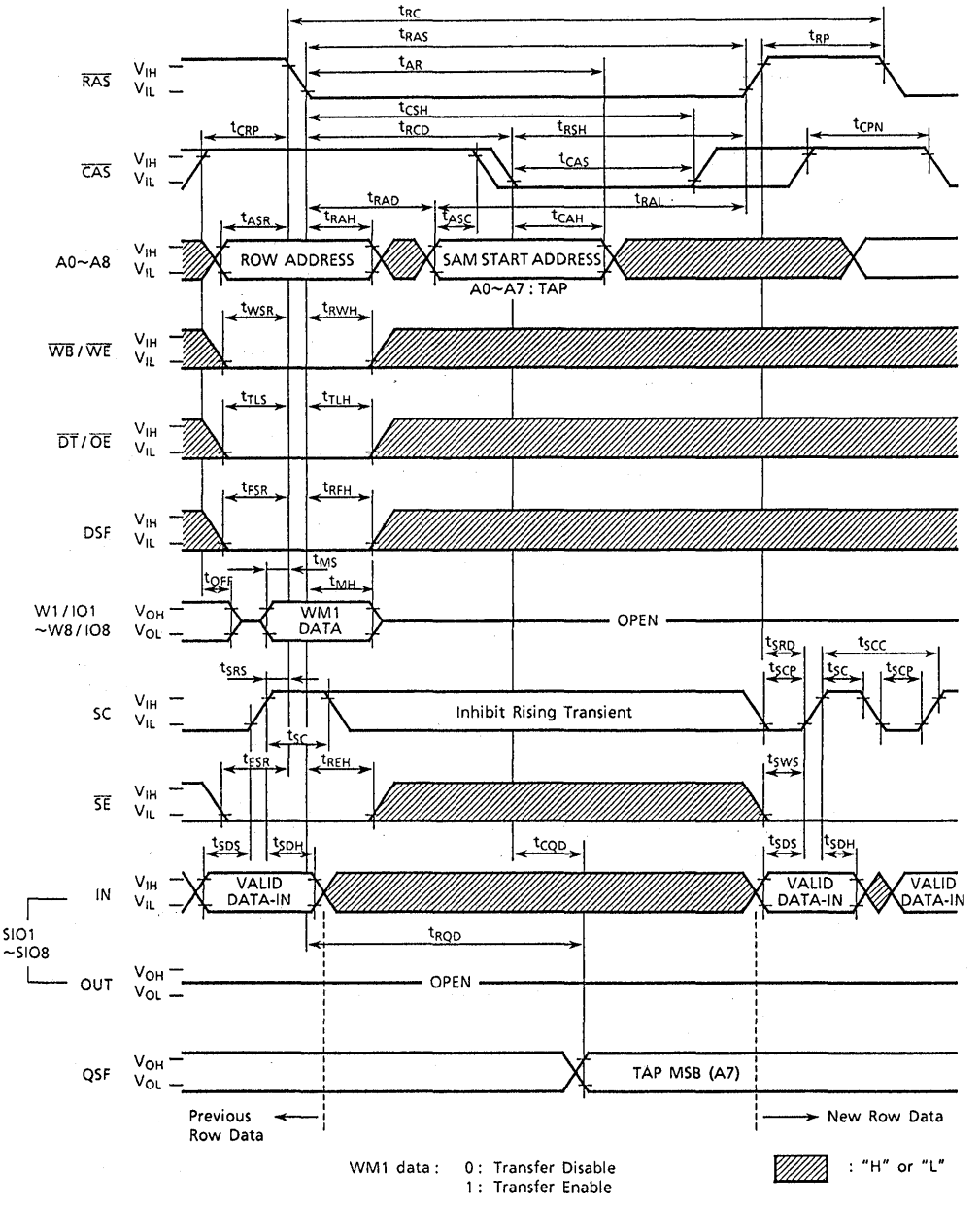


Note : $\overline{SE}$ = V_{IL}

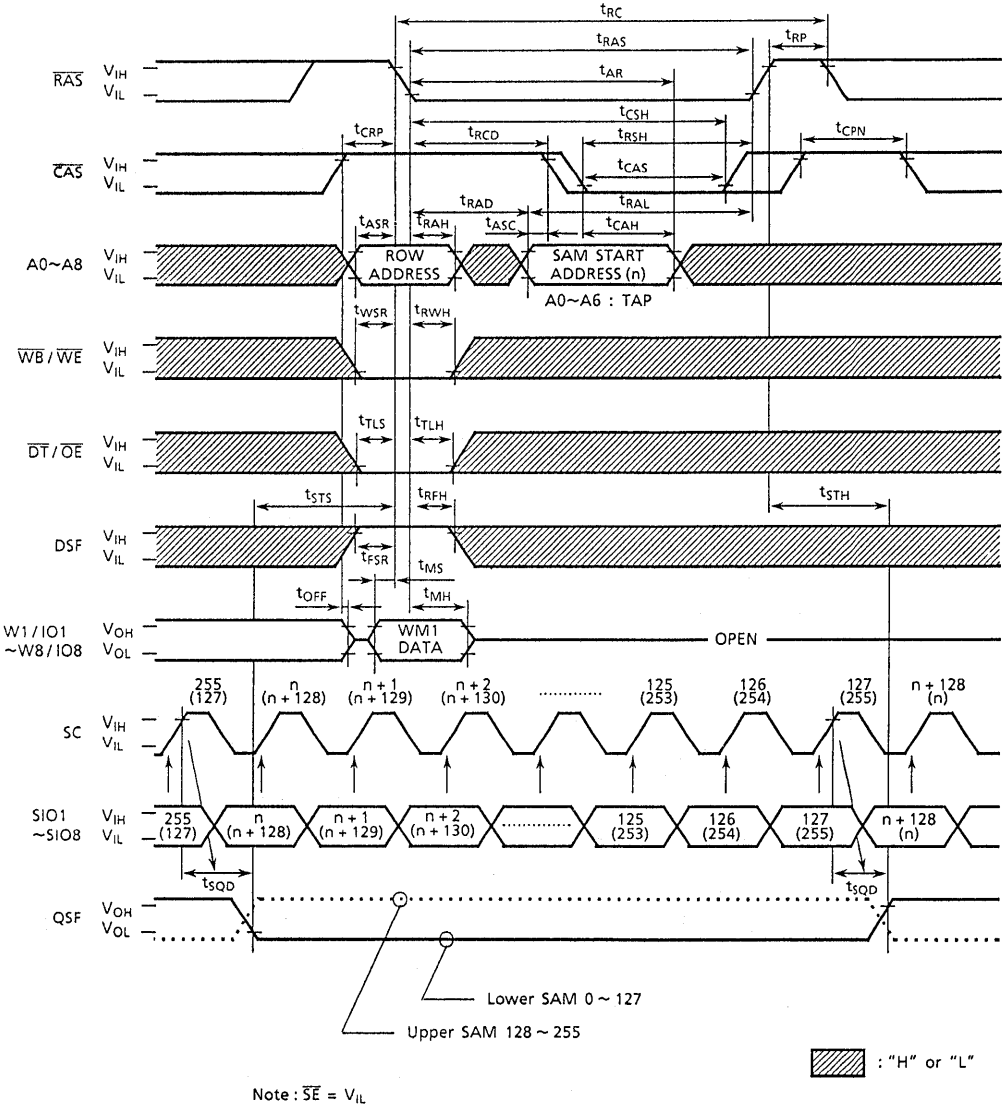
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE

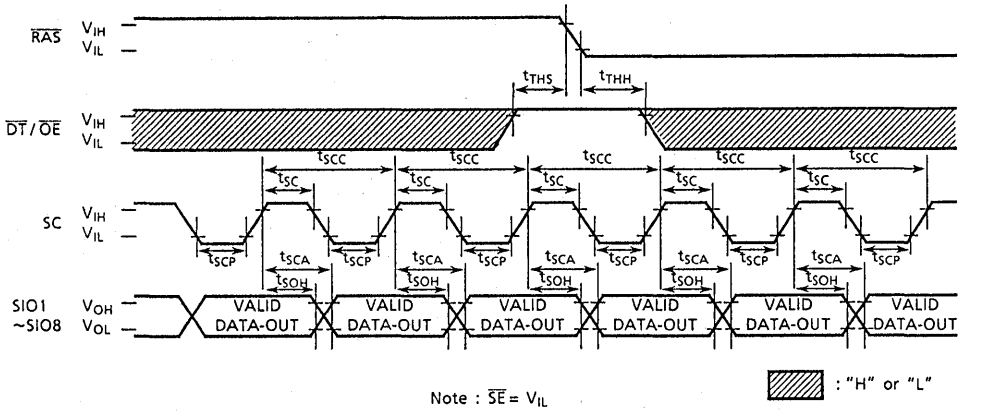


SPLIT WRITE TRANSFER CYCLE



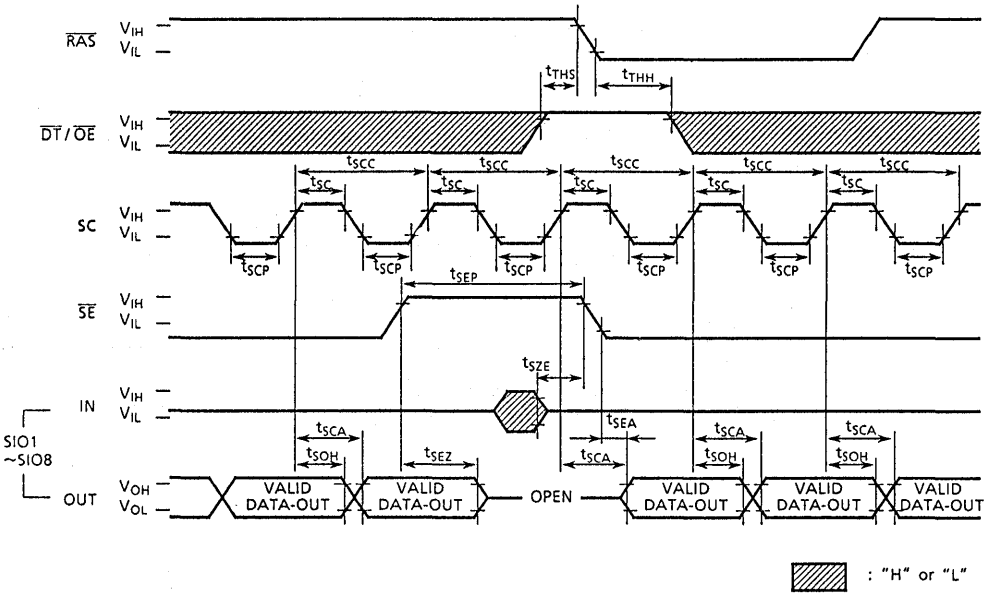
Note : $\overline{SE}$ = V_{IL}

SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

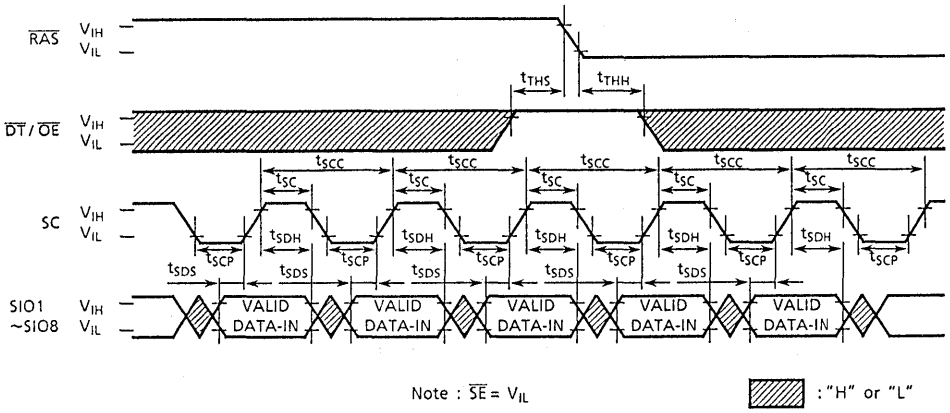


Note : $\overline{SE}$ = V_{IL}

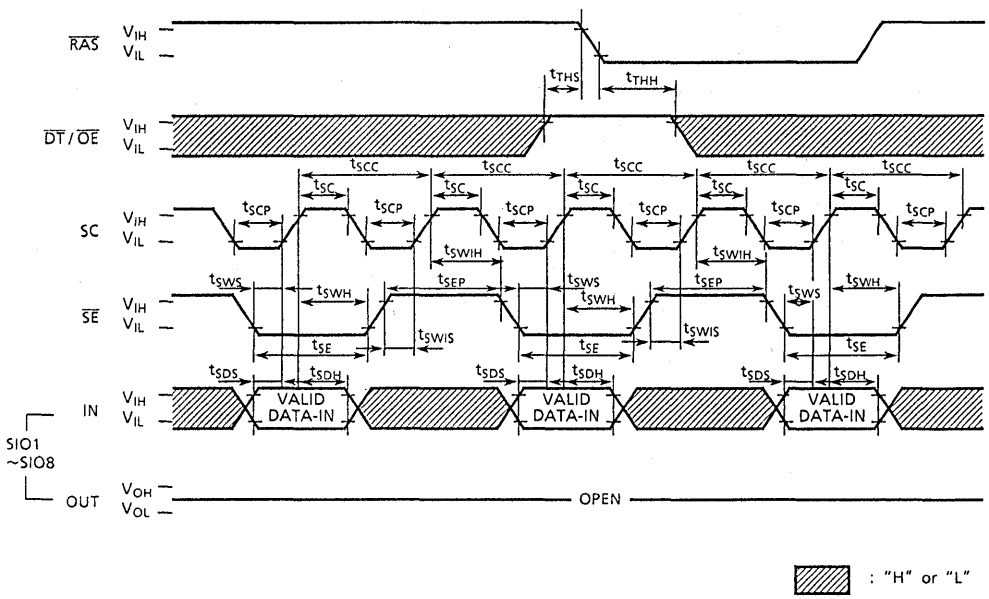
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC528128BJ/BZ are multiplexed onto 9 address input pins ($A_0 \sim A_8$). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{RAS}$ control, either read/write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT / WRITE ENABLE : $\overline{WB}$ / $\overline{WE}$

The $\overline{WB}$ / $\overline{WE}$ input is also a multifunction pin. When $\overline{WB}$ / $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}$ / $\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}$ / $\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}$ / $\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked-write transfer).

WRITE MASK DATA / DATA INPUT AND OUTPUT : W_1 / IO_1~W_8 / IO_8

When the write-per-bit function is enabled, the mask data on the W_i / IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}$ / $\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i / IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}$ / $\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}$ / $\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer (7-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read / pseudo write / write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT : DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of flash write, block write, load color register and split read/write transfer can be invoked.

SPECIAL FUNCTION OUTPUT : QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~127) is being accessed and QSF "high" indicates that the upper split SAM (Bit 128~255) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO1~SIO8

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC528128BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{CAS}$ falling edge				Don't	0	0	1	1
$\overline{RAS}$ falling edge				DSF	0	1	0	1
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$					
0	*	*	*		$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0		Masked Write Transfer	Split Write Transfer with	Masked Write Transfer	Split Write Transfer with
1	0	0	1		Pseudo Write Transfer	Mask	Pseudo Write Transfer	Mask
1	0	1	*		Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*		Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	*		Read/Write	Load Color	Block Write	Load Color

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓		WM1	Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	*	–	–	–	–	–
Masked Write Transfer	1	0	0	0	0	*	Row	TAP	WM1	*	*	WM1	Load use	–
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	–	–	–
Split Write Transfer	1	0	0	1	*	*	Row	TAP	WM1	–	*	WM1	Load use	–
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	–	–	–
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	–	–	–
Write per Bit	1	1	0	0	*	0	Row	Column	WM1	–	DIN	WM1	Load use	–
Masked Block Write	1	1	0	0	*	1	Row	Column A2C-7C	WM1	Column Select	–	WM1	Load use	use
Masked Flash Write	1	1	0	1	*	*	Row	*	WM1	–	*	WM1	Load use	use
Read Write	1	1	1	0	*	0	Row	Column	*	–	DIN	–	–	–
Block Write	1	1	1	0	*	1	Row	Column A2C-7C	*	Column Select	–	–	–	use
Load Color	1	1	1	1	*	*	Row	*	*	–	Color	–	–	Load

* : "0" or "1" , TAP : SAM start address , – : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked : $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split write transfer, split read transfer, flash write and load color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write special feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μsconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC528128BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

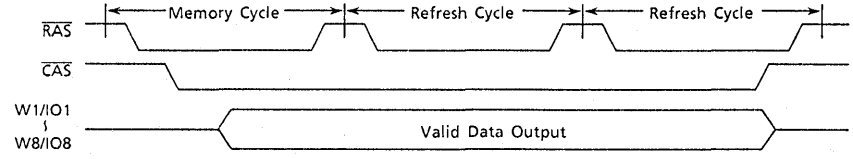


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When a "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i = 1~8)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

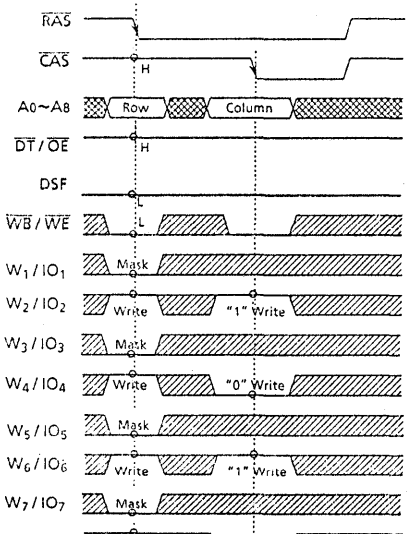


Figure 2. Write-per-bit timing cycle

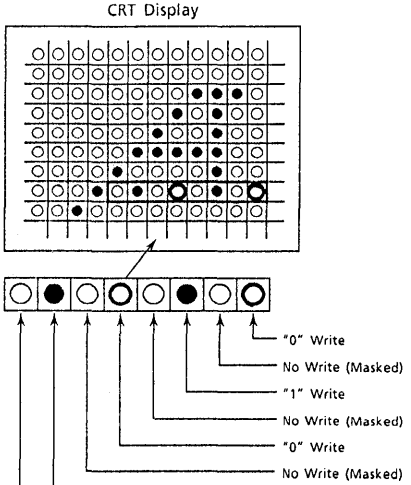


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER/READ COLOR REGISTER

The TC528128BJ/BZ is provided with an on-chip 8-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs last. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ are satisfied. During the load/read color register cycle, valid A_0~A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

FLASH WRITE

Flash write is a special RAM port write operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (Refer to Figure 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle (Refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2 μseconds.

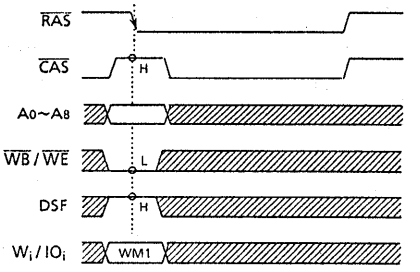


Figure 4. Flash Write Timing

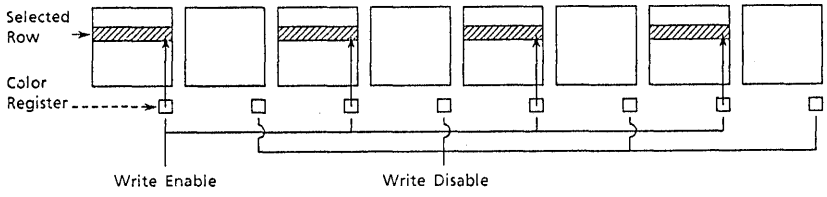


Figure 5. Flash Write

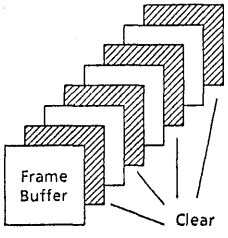


Figure 6. Plane clear application example

BLOCK WRITE

Block write is also a special RAM port write operation which, in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB}/\overline{WE}$ must be "low " to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the six most significant column addresses (A2C~A7C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 7).

An example of the block write function is shown in Figure 8 with a data mask on W_1/IO_1, W_4/IO_4, W_6/IO_6, W_7/IO_7 and column 2. Block write is most effective for window clear and fill operation in frame buffer applications, as shown in the examples in Figure 9.

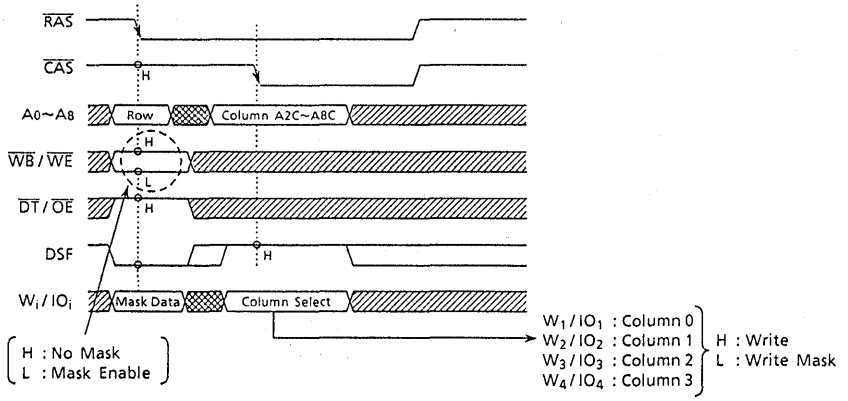


Figure 7. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1 / IO_1	0	1	0
W_2 / IO_2	1	1	0
W_3 / IO_3	1	0	1
W_4 / IO_4	0	1	1
W_5 / IO_5	1	–	1
W_6 / IO_6	0	–	1
W_7 / IO_7	0	–	0
W_8 / IO_8	1	–	0

	Column 0	Column 1	Column 2	Column 3	
W_1 / IO_1					← Mask
W_2 / IO_2	0	0		0	
W_3 / IO_3	1	1		1	
W_4 / IO_4					← Mask
W_5 / IO_5	1	1		1	
W_6 / IO_6					
W_7 / IO_7					
W_8 / IO_8	0	0		0	

Mask

Figure 8. Example of Block Write Operation

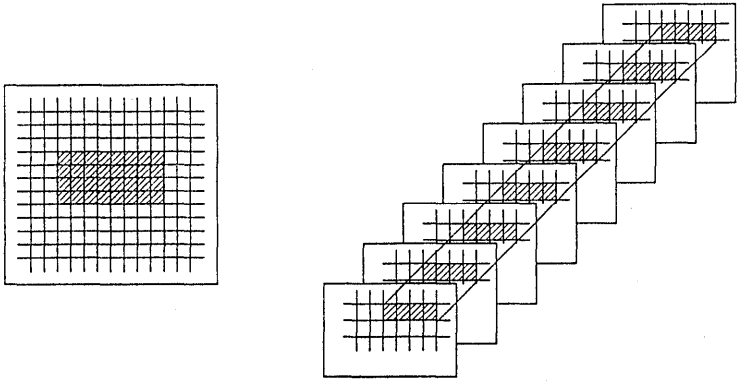


Figure 9. Examples of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read/write operation will occur. Therefore a combination of block write and read/write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

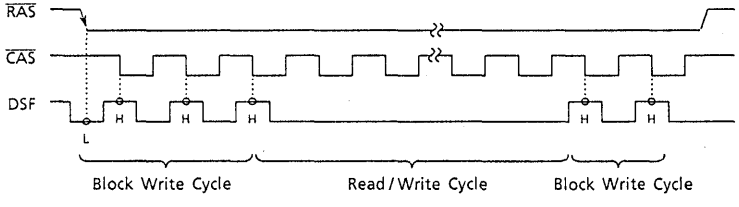


Figure 10. Fast Page Mode Block Write Cycle

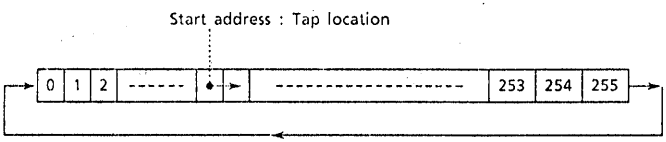
SAM PORT OPERATION

The TC528128BJ/BZ is provided with a 256 words by 8 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



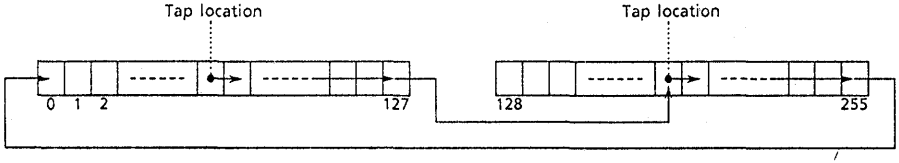
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

SPLIT REGISTER MODE

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (Non-split) read/write/pseudo write transfer operation must precede any split read/write transfer operation. The non-split read, write and pseudo write transfer will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 128 tap locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected tap location to the most significant bit (127 or 255) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data in or out sequentially starting from this tap location to the most significant bit (255 or 127) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC528128BJ/BZ features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal (Non-split) transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 128 words by 8 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal .

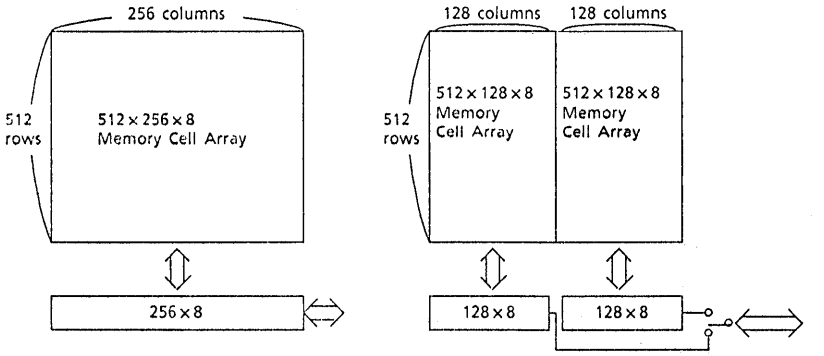


Figure 11. (a) Normal (Non-split) Transfer (b) Split Transfer

As shown in Table 5, the TC528128BJ/BZ supports five types of transfer operations: Read transfer, Split read transfer, Write transfer, Split write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/Pseudo write transfer) whereas it remains unchanged during split transfer operations (Split read or split write transfers). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_7 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A7C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	256×8	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	256×8	Output → Input
H	L	L	H	L	Pseudo Write Transfer	-	-	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	128×8	Not changed
H	L	L	*	H	Split Write Transfer	SAM → RAM	128×8	Not changed

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for read transfer operation.

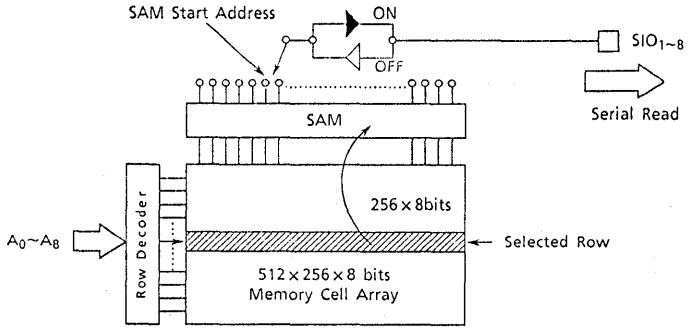


Figure 12. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 13.

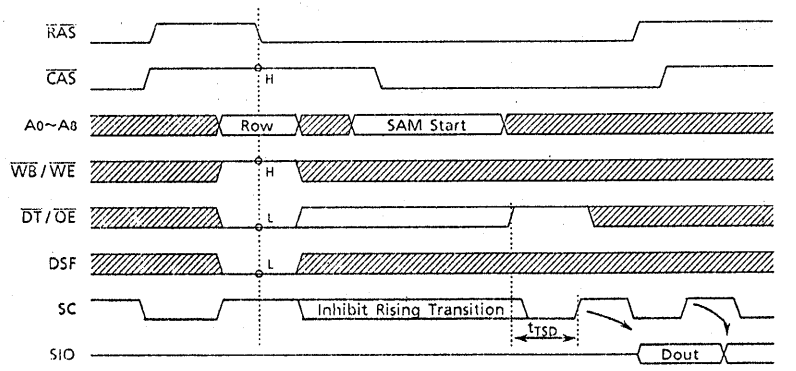


Figure 13. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

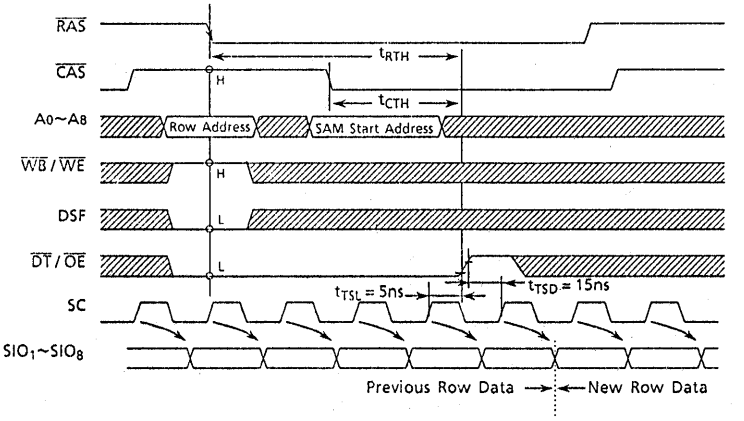


Figure 14. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figure 15 and 16 show the timing diagram and block diagram for write transfer operations, respectively.

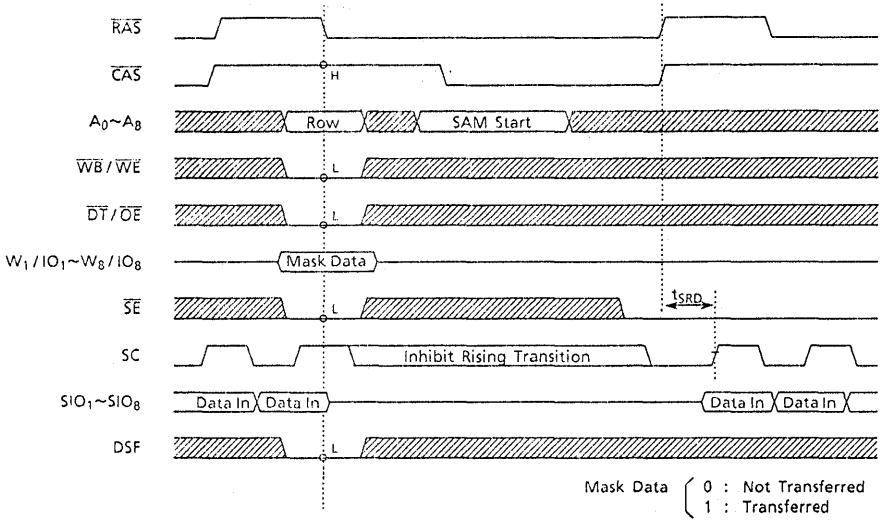


Figure 15. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

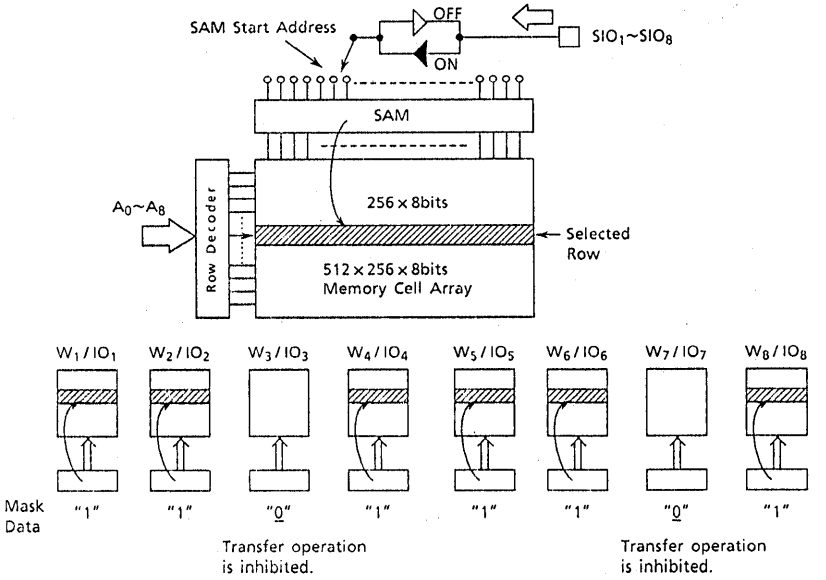


Figure 16. Block Diagram for Write Transfer Operation

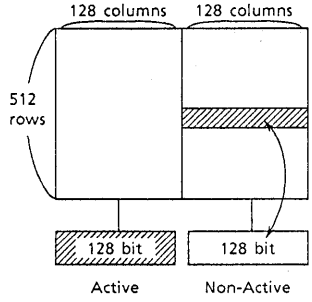
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}$ / $\overline{OE}$ "low", $\overline{WB}$ / $\overline{WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

SPLIT DATA TRANSFER AND QSF

The TC528128BJ/BZ features a bi-directional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A7C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 18.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 17. Split Register Mode

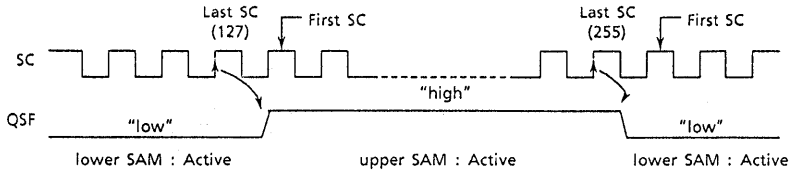


Figure 18. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading 127 words by 8 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

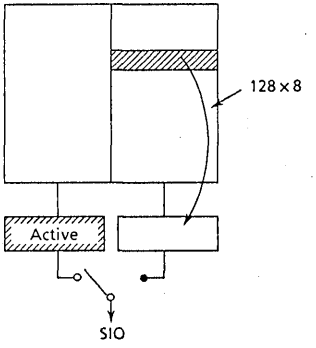


Figure 19. Block Diagram for Split Read Transfer

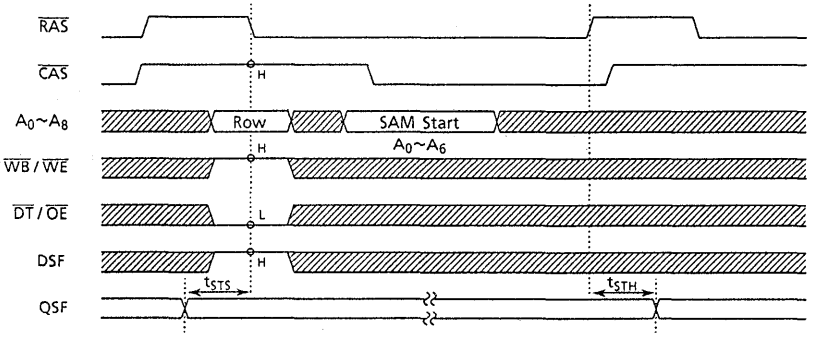


Figure 20. Timing Diagram for Split Read transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 21.

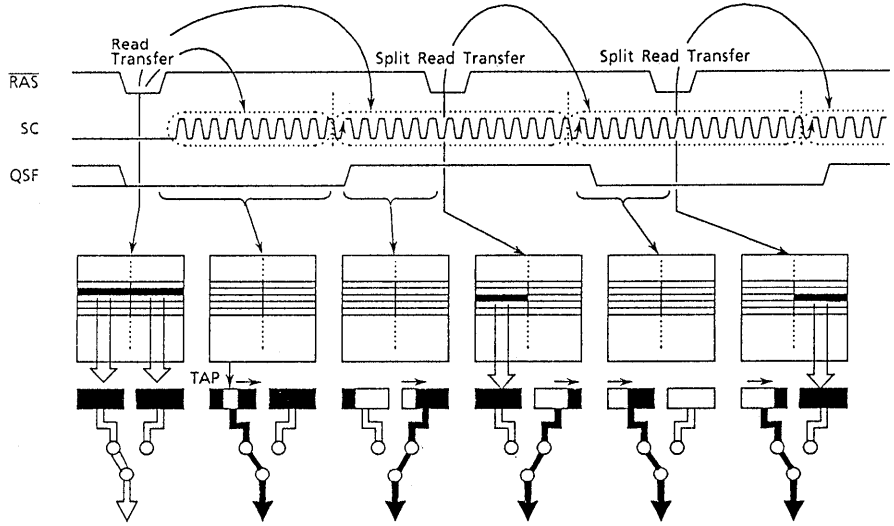


Figure 21. Example of Consecutive Read Transfer Operations

SPLIT WRITE TRANSFER CYCLE

A split write transfer consists of loading 128 words by 8 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figure 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

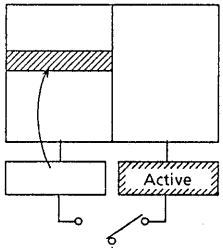


Figure 22. Block Diagram for Split Write Transfer

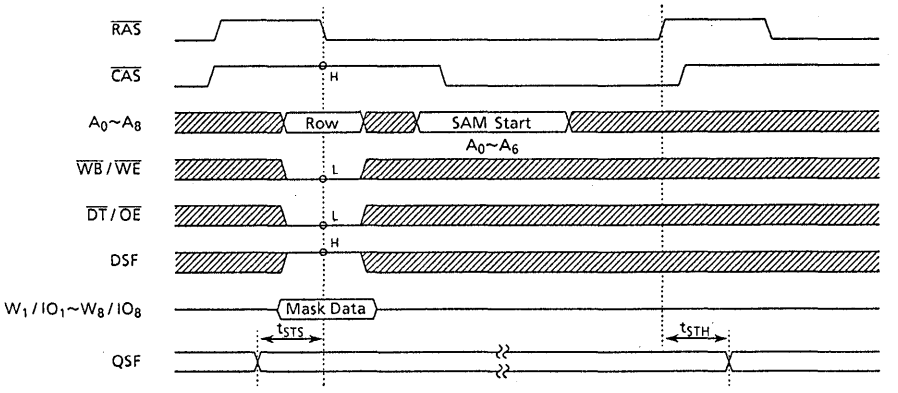


Figure 23. Timing Diagram for Split Write Transfer

A pseudo write transfer operation must precede split transfer cycles as shown in the example in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

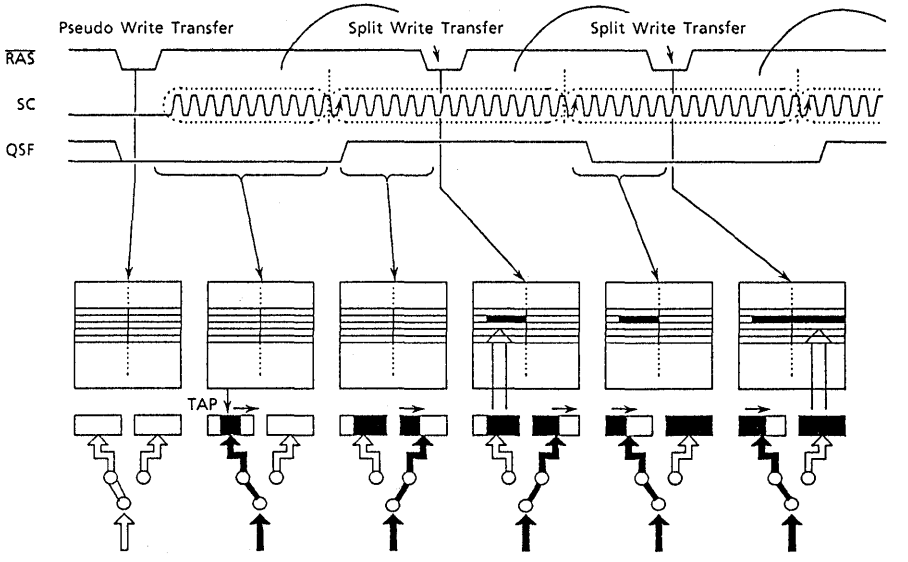


Figure 24. Example of Consecutive Write Transfer Operations

SPLIT-REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read / write transfers must be preceded by a normal (Non-split) transfer such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 127 in this example and the pointer is incremented from this location by cycling the SC clock.

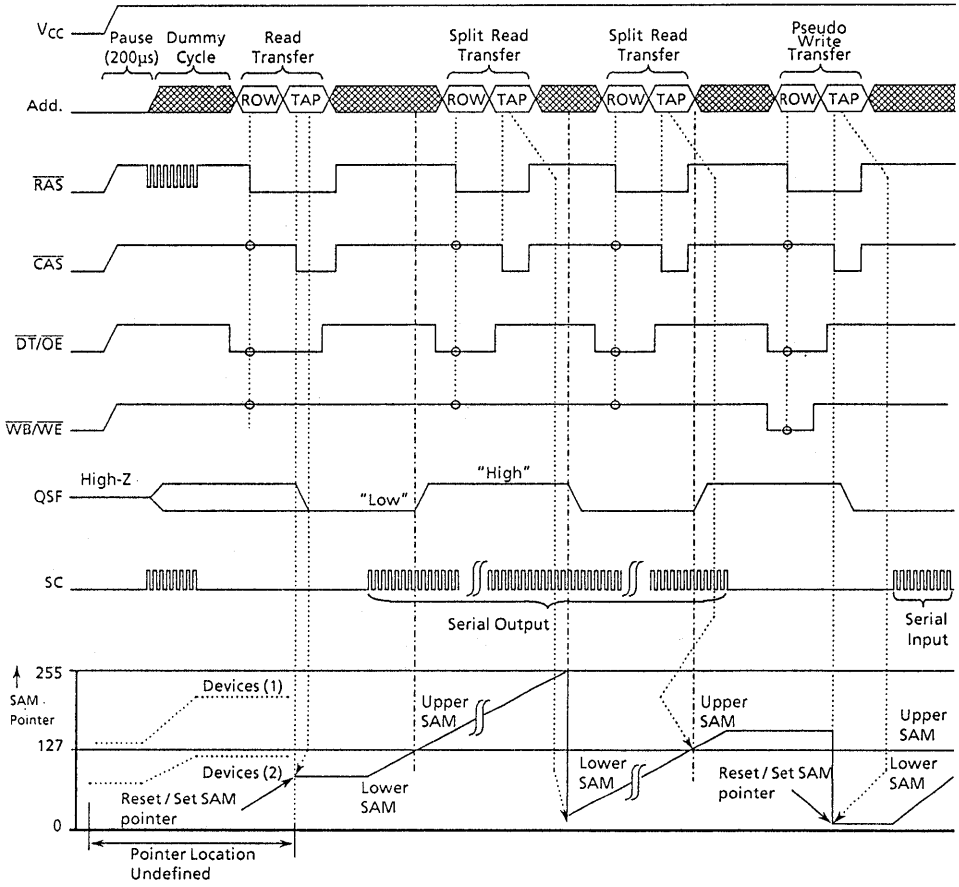
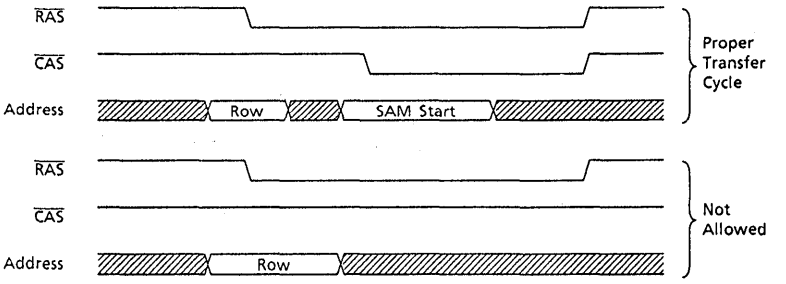


Figure 25. Example of Spilit SAM Register Operation Seguence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

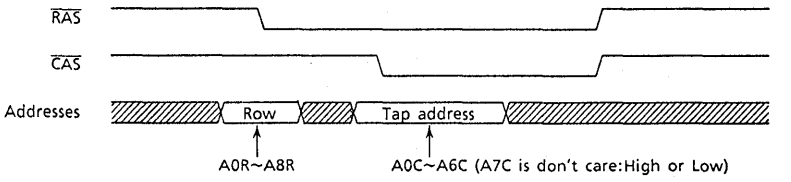
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



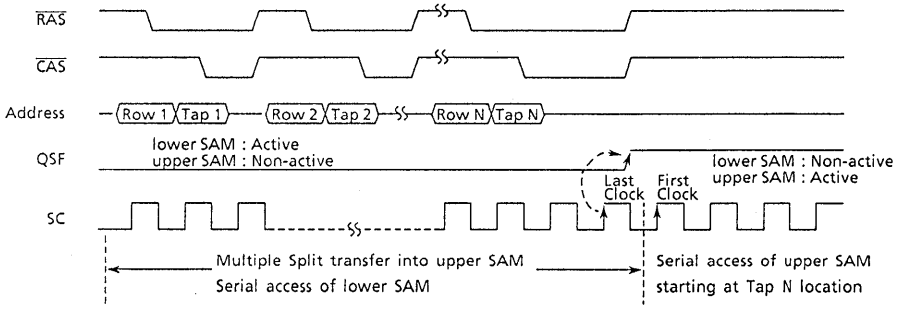
TAP LOCATION SELECTION IN SPLIT TRANSFER OPERATION

(a) In a split transfer operation, column addresses A0C through A6C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split transfer, column address A7C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A6C=7F), in either the lower SAM or the upper SAM, as the tap location.

(b) In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ/WRITE TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read/write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF.

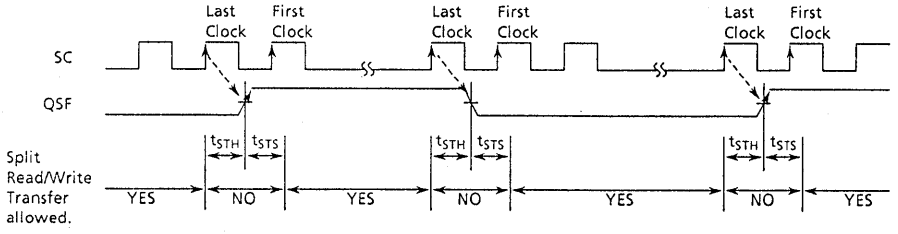
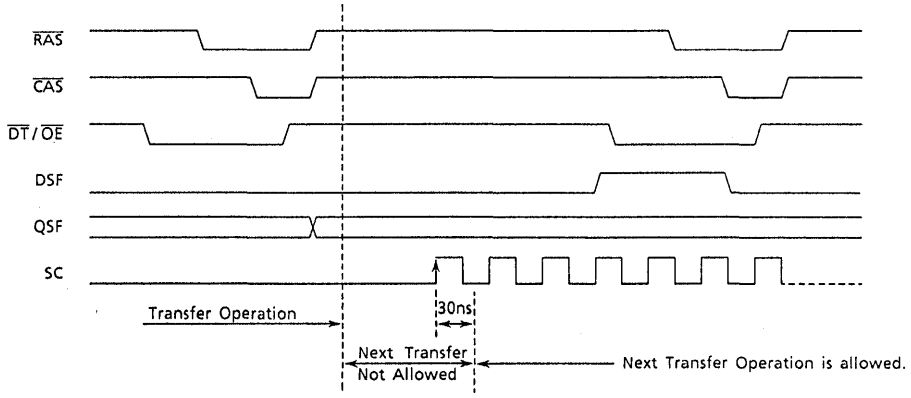


Figure 26. Split Transfer Operation Allowable Periods

As indicated in Figure 26, a split read/write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

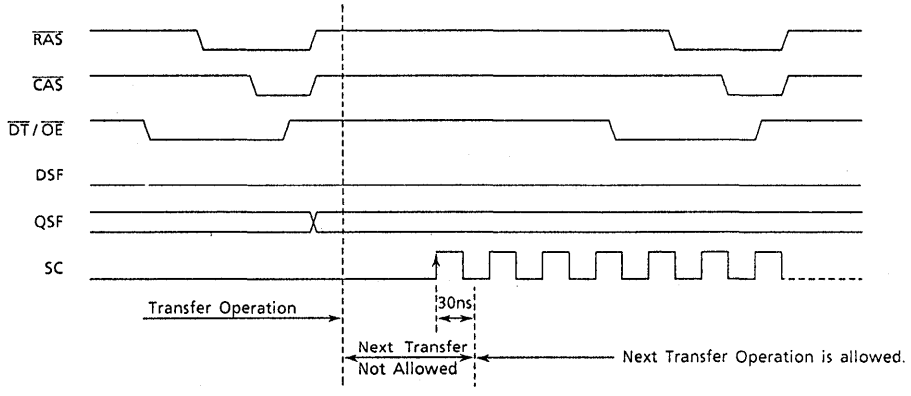
SPLIT TRANSFER CYCLE AFTER NORMAL TRANSFER CYCLE

A split transfer may be performed following a normal transfer (Read / Write / Pseudo-Write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



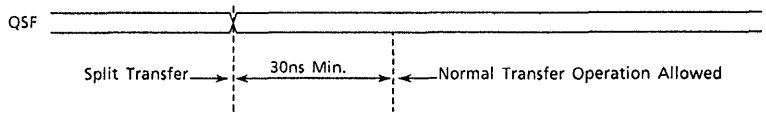
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT TRANSFER

A normal transfer (read / write / pseudo write) may be performed following split transfer operation provided that a 30ns minimun delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC528128BJ / BZ is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

NOTES

262,144WORDS × 4BITS MULTIPORT DRAM

PRELIMINARY

DESCRIPTION

The TC524256BJ/BZ is a CMOS multiport memory equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The TC524256BJ/BZ supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC524256BJ/BZ is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC524256BJ/BZ	
		-80	-10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	85mA	70mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

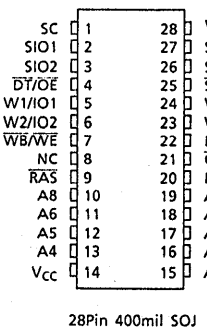
- Organization
  - RAM Port : 262,144words×4bits
  - SAM Port : 512words×4bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - 512 refresh cycles/8ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
- Package
  - TC524256BJ : SOJ28-P-400
  - TC524256BZ : ZIP28-P-400

PIN NAME

A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write per Bit/Write Enable
W1/IO1~W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO4	Serial Input/Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

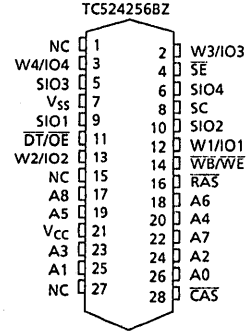
PIN CONNECTION

TC524256BJ



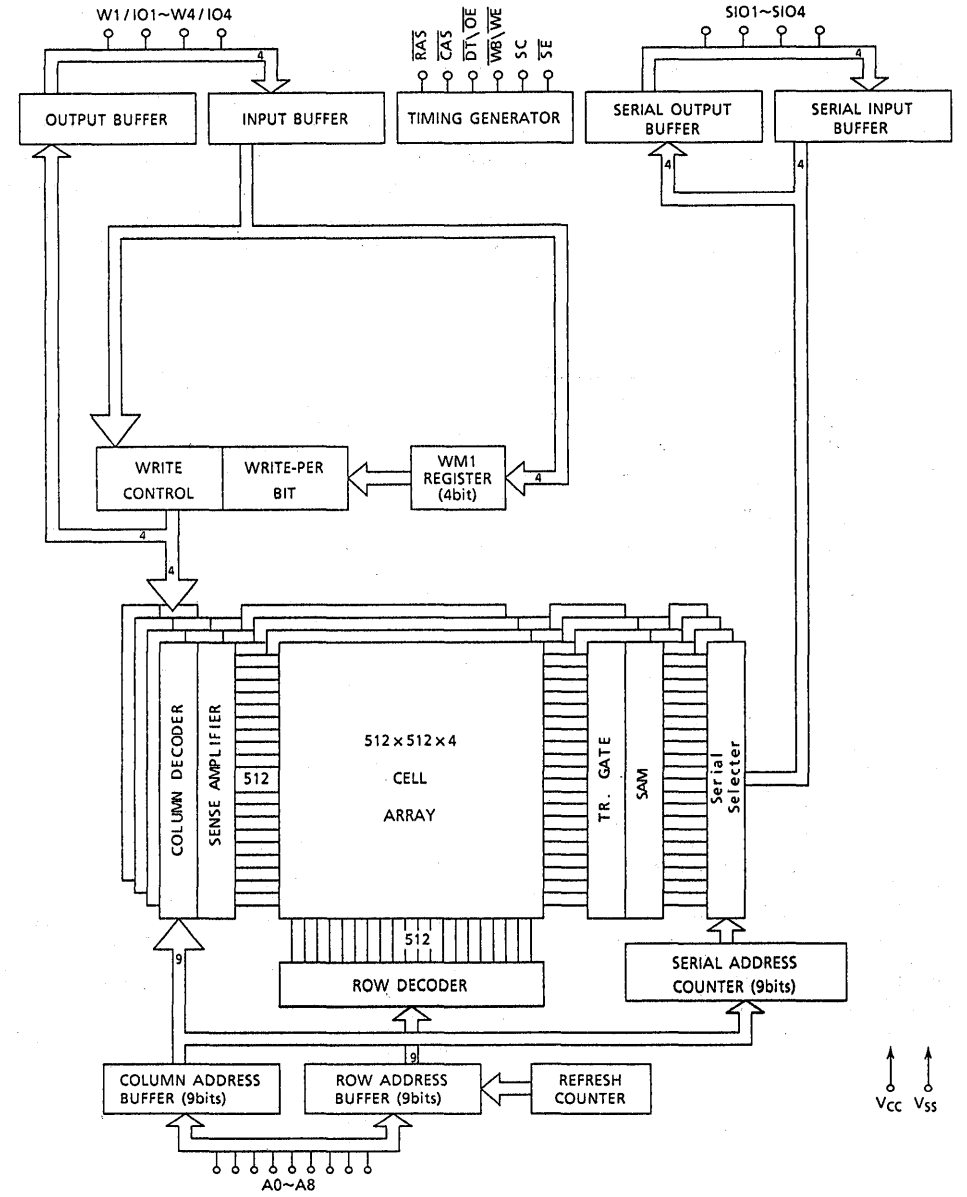
28Pin 400mil SOJ
JEDEC Standard

TC524256BZ



28Pin 400mil height ZIP
JEDEC Standard

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	−1.0~7.0	V	1
V_{CC}	Power Supply Voltage	−1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	−	7	pF
C_{IO}	Input/Output Capacitance	−	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC524256BJ/BZ-80		TC524256BJ/BZ-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	–	85	–	70	mA	3, 4
	Active	I_{CC1A}	–	125	–	110		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	–	85	–	70		3, 4
	Active	I_{CC3A}	–	125	–	110		3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Standby	I_{CC4}	–	75	–	60		3, 4
	Active	I_{CC4A}	–	115	–	100		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	–	85	–	70		3, 4
	Active	I_{CC5A}	–	125	–	110		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	–	105	–	90		3, 4
	Active	I_{CC6A}	–	145	–	130		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≦ V_{IN} ≦ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≦ V_{OUT} ≦ 5.5V, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = – 2mA	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC524256BJ/BZ-80		TC524256BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC524256BJ/BZ-80		TC524256BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130		ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

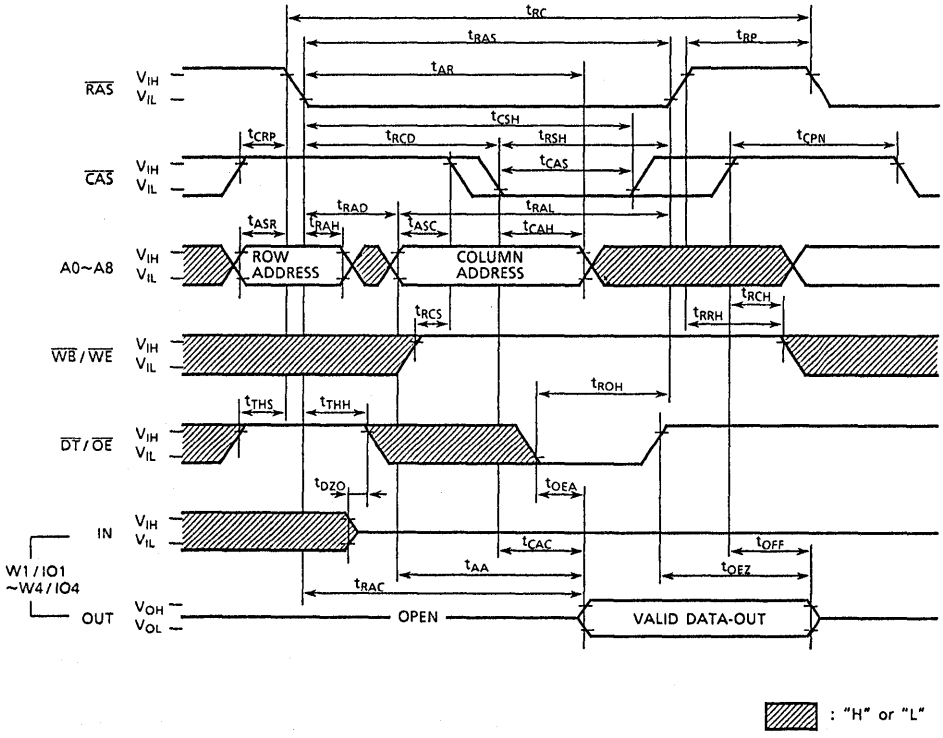
SYMBOL	PARAMETER	TC524256BJ/BZ-80		TC524256BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			

NOTES :

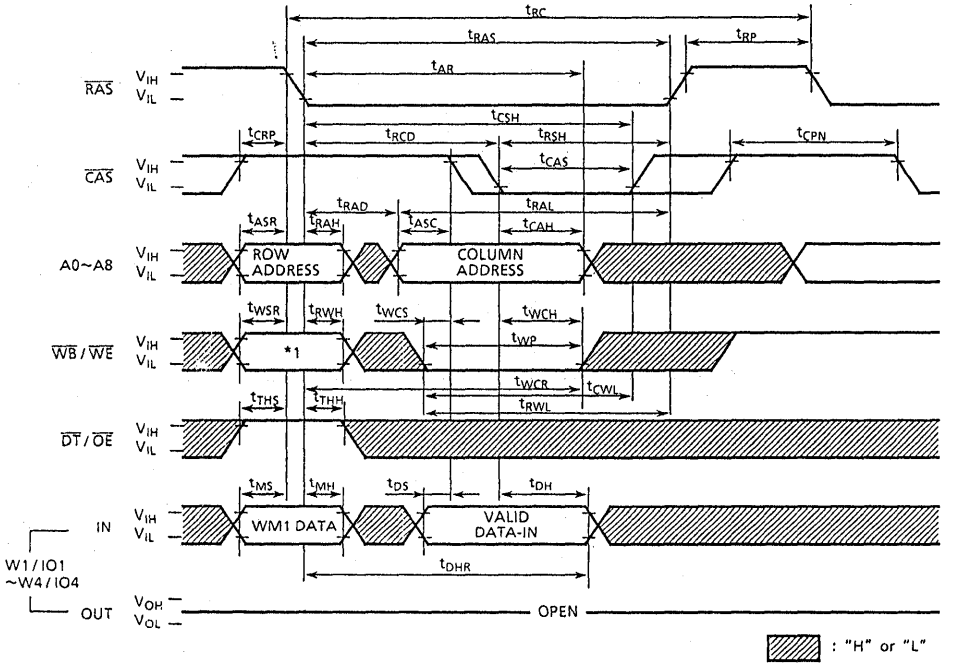
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only : If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



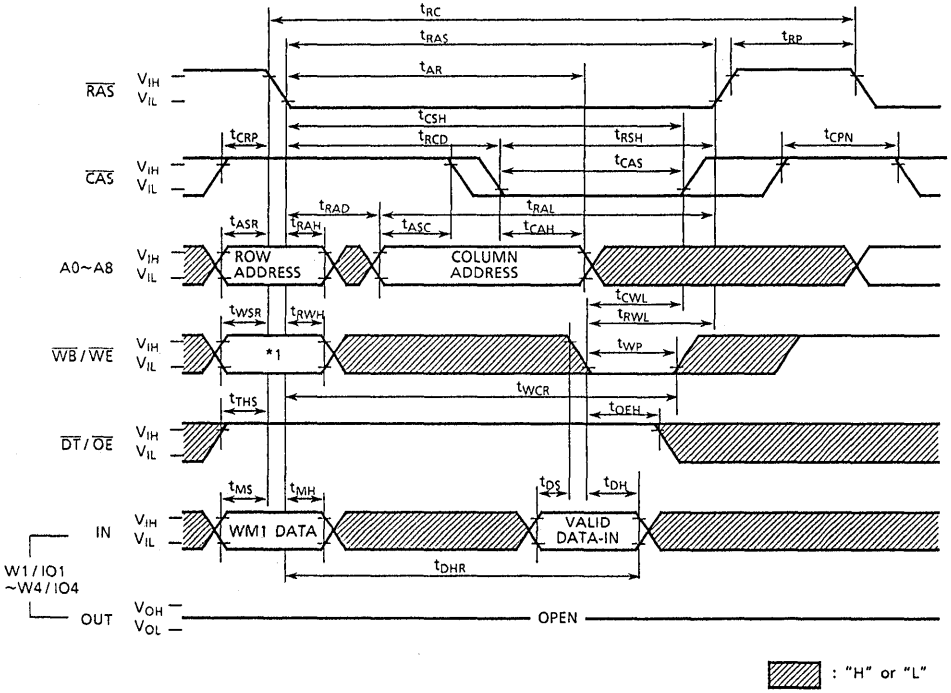
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W4 / IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

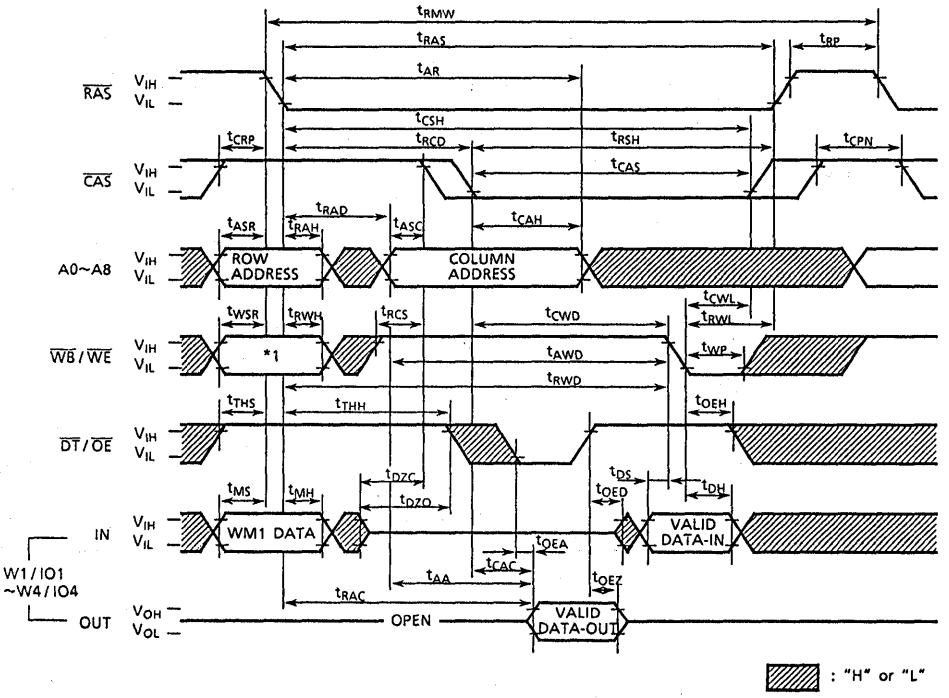
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W4 / IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

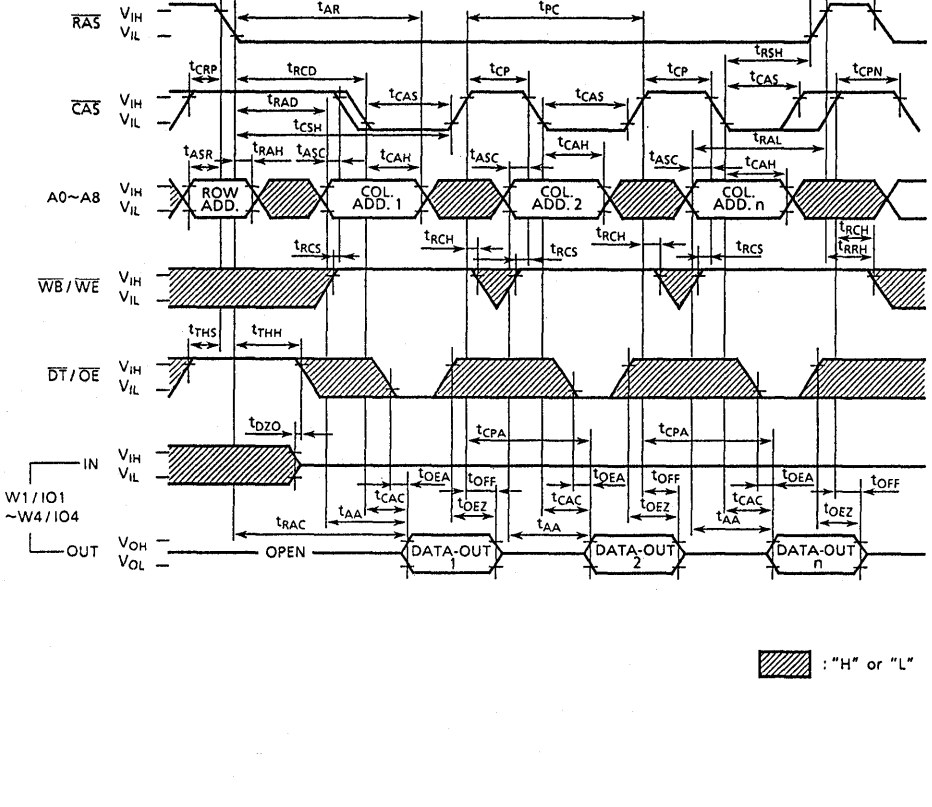
READ - MODIFY - WRITE CYCLE



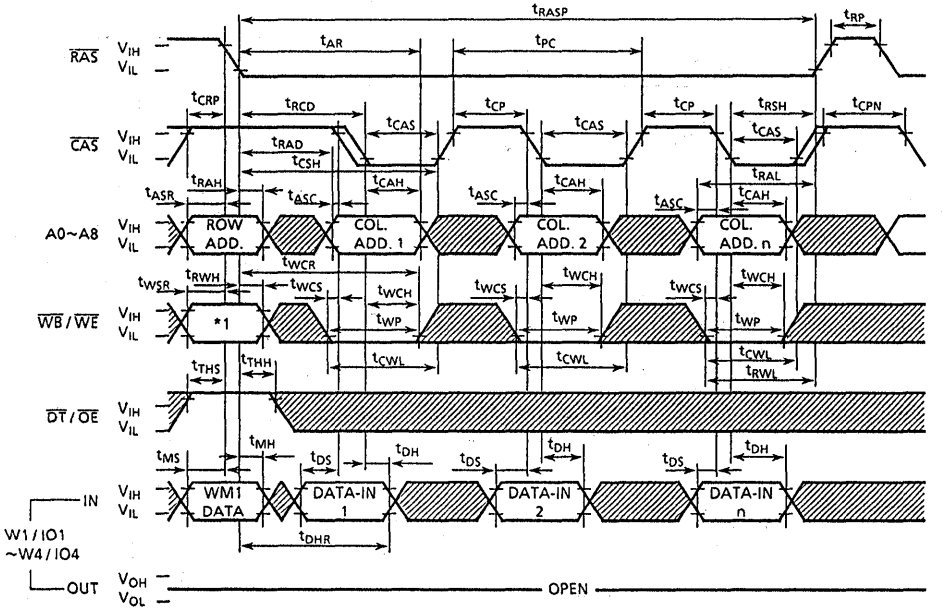
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W4 / IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



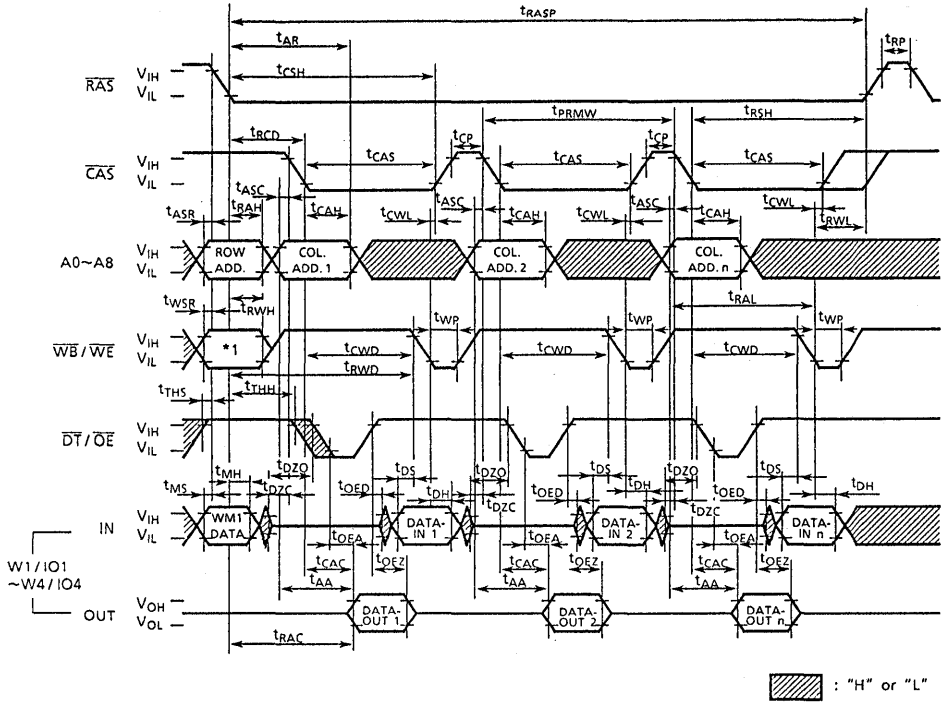
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

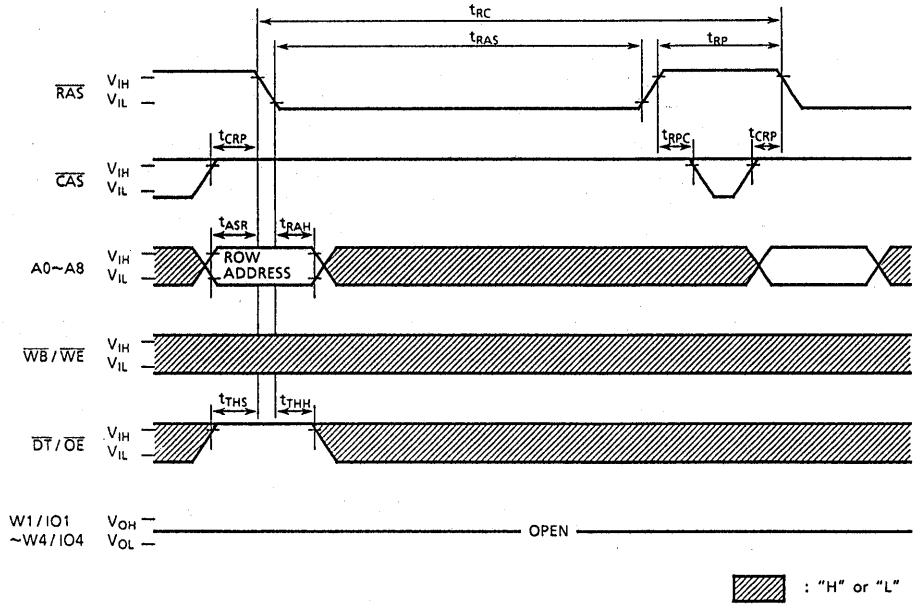
FAST PAGE MODE READ - MODIFY - WRITE CYCLE



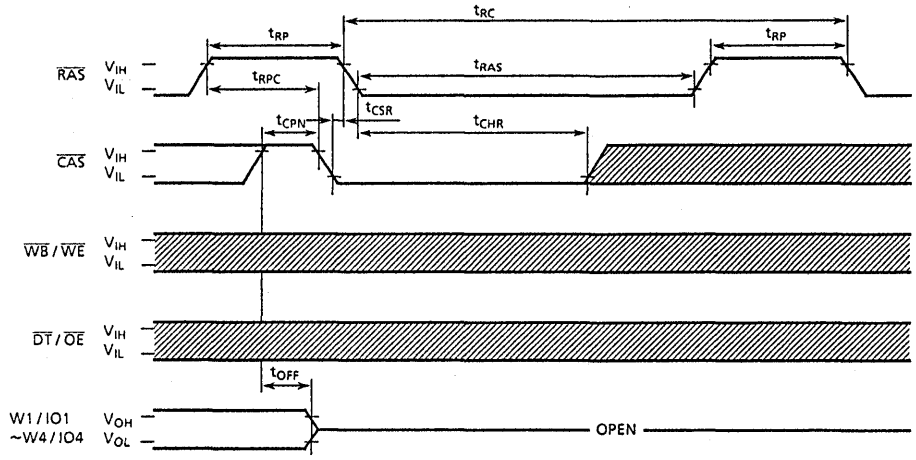
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W4 / IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

$\overline{RAS}$ ONLY REFRESH CYCLE



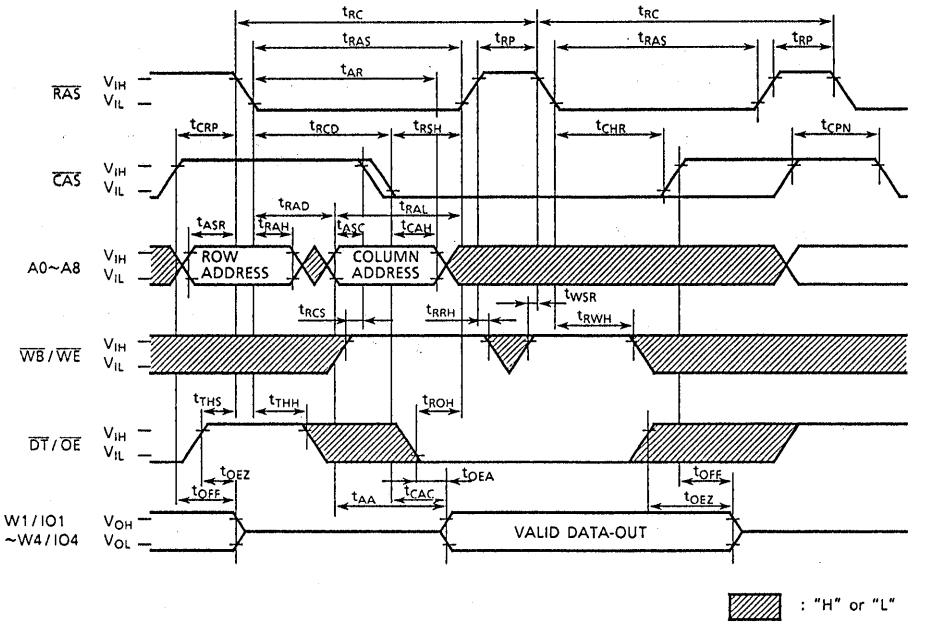
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



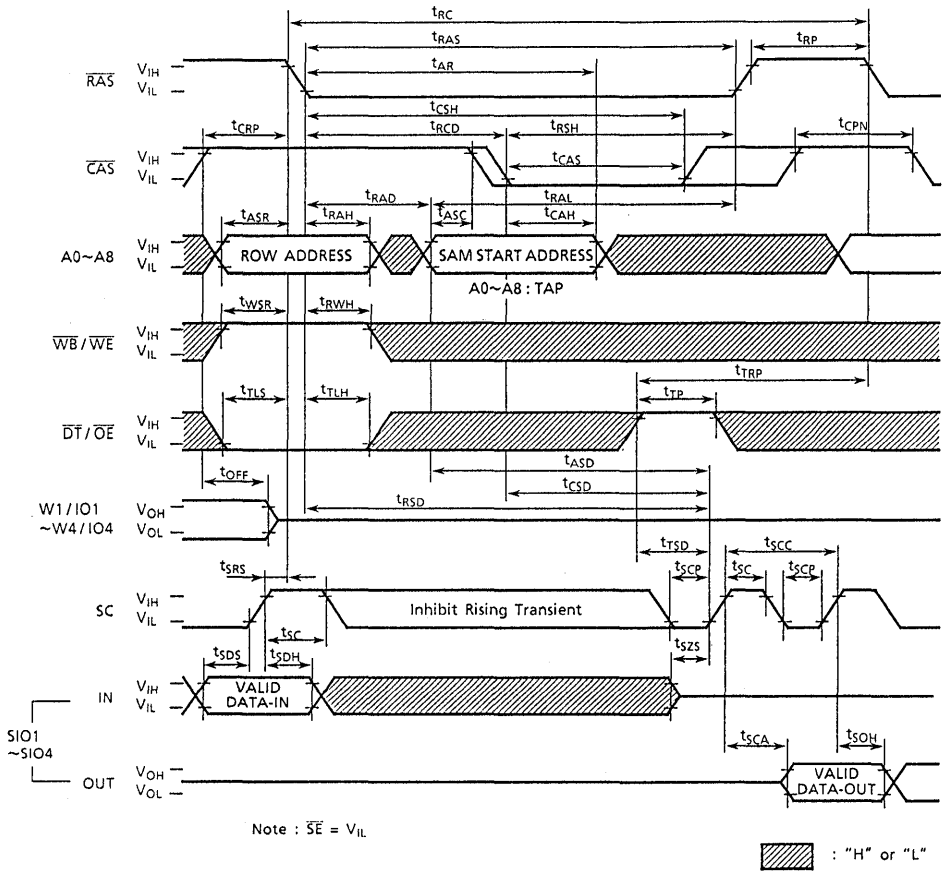
Note : A0 ~ A8 = Don't Care ("H" or "L")

: "H" or "L"

HIDDEN REFRESH CYCLE



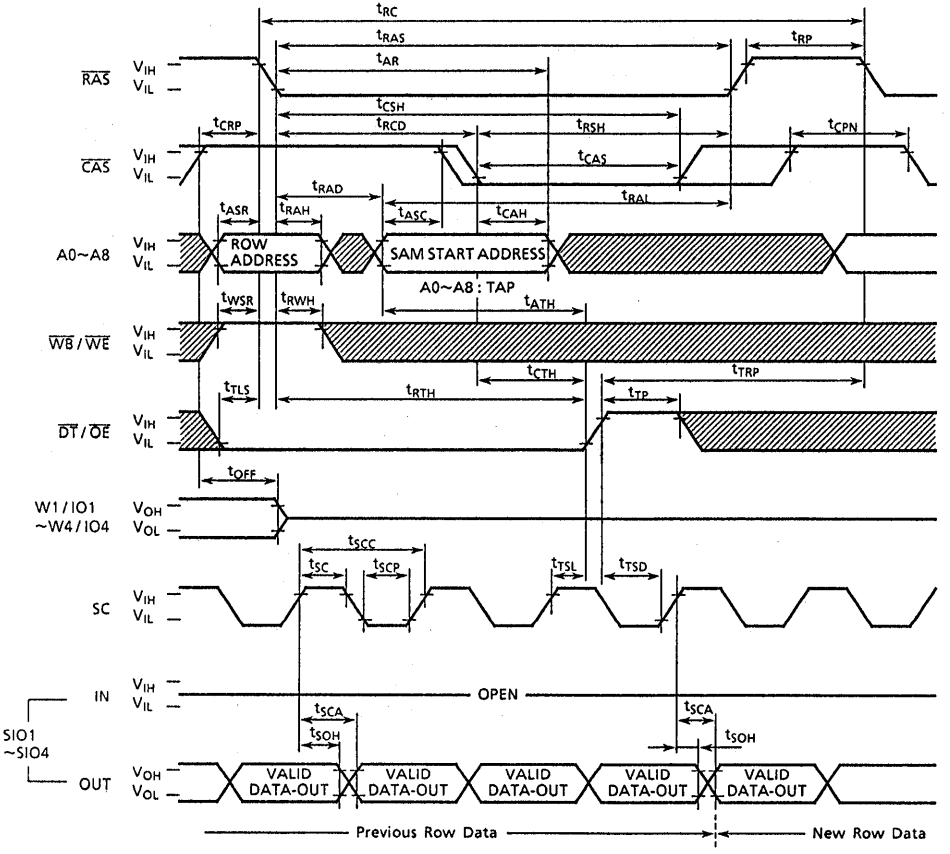
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

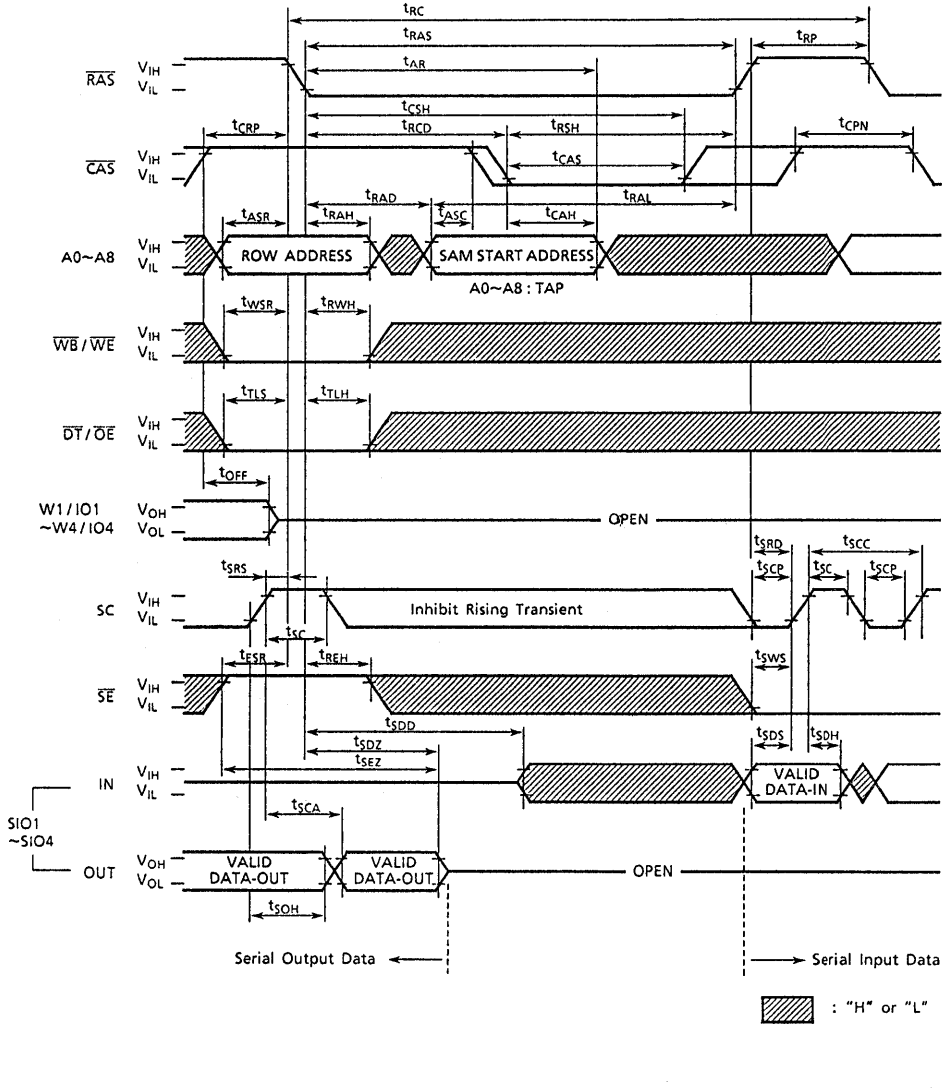
REAL TIME READ TRANSFER CYCLE



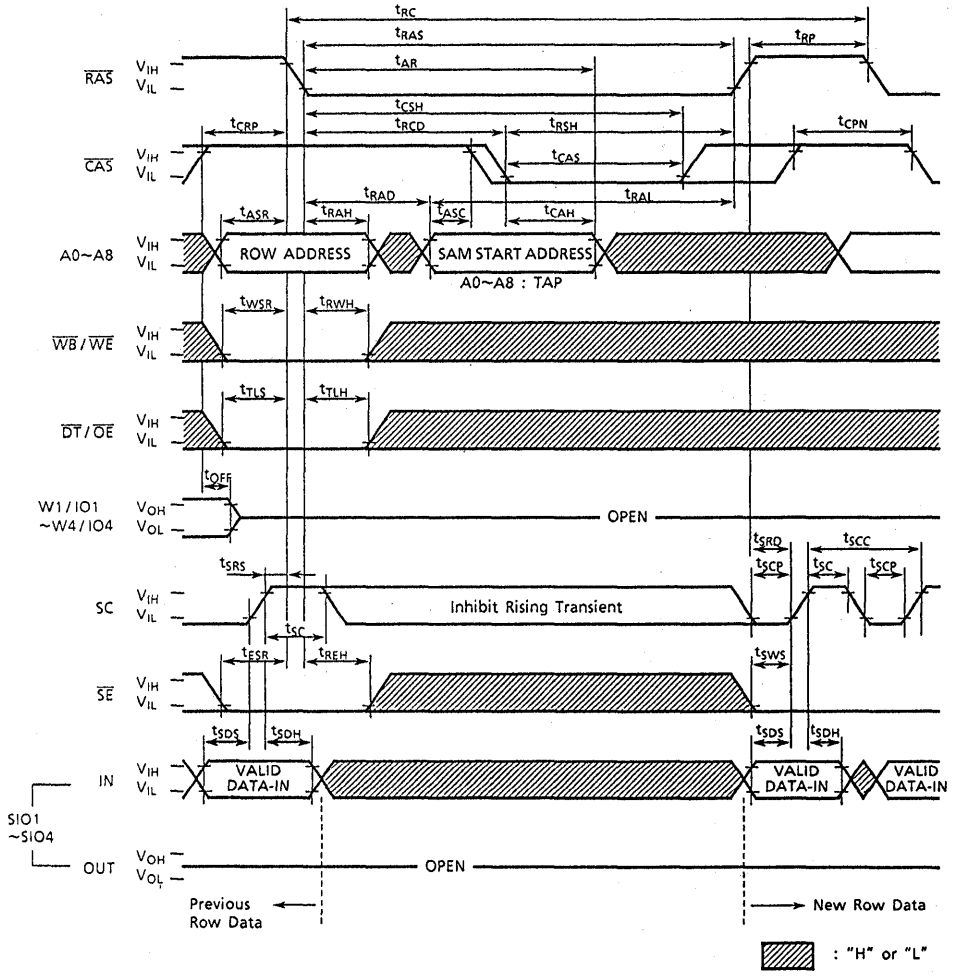
Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

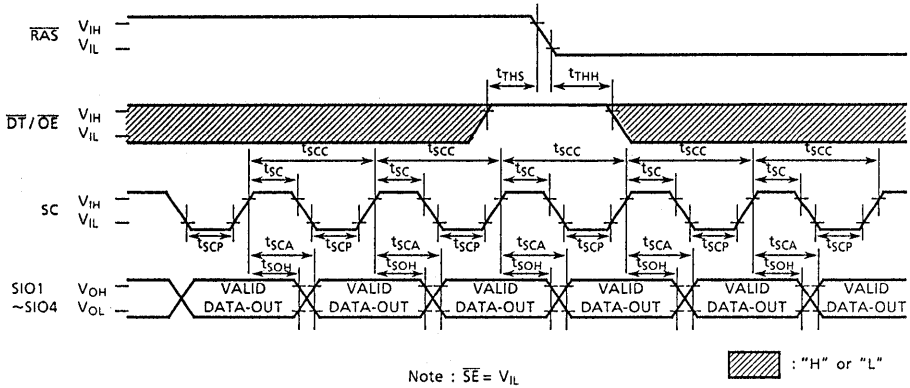
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE

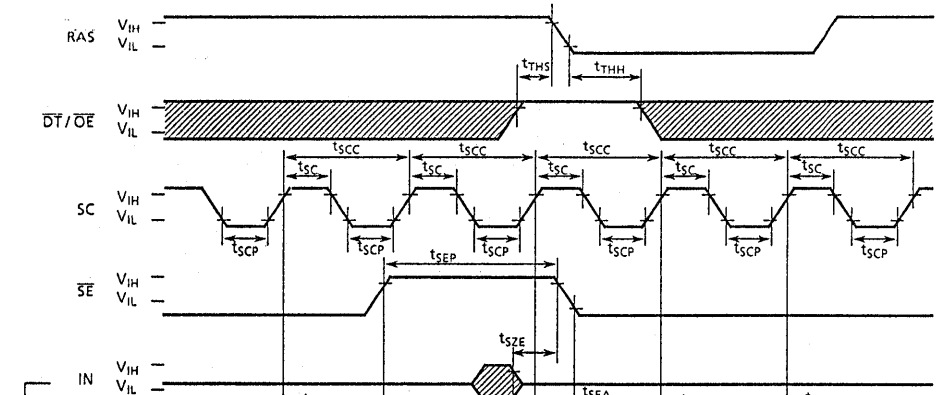


SERIAL READ CYCLE ($\overline{SE}$ = V_{IL})

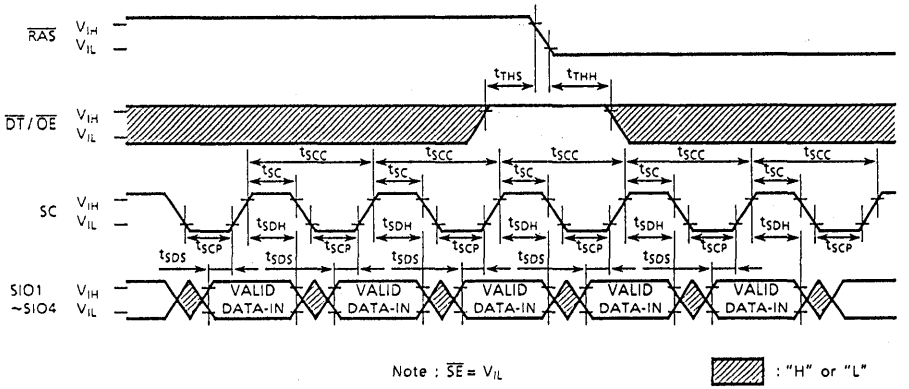


Note : $\overline{SE}$ = V_{IL}

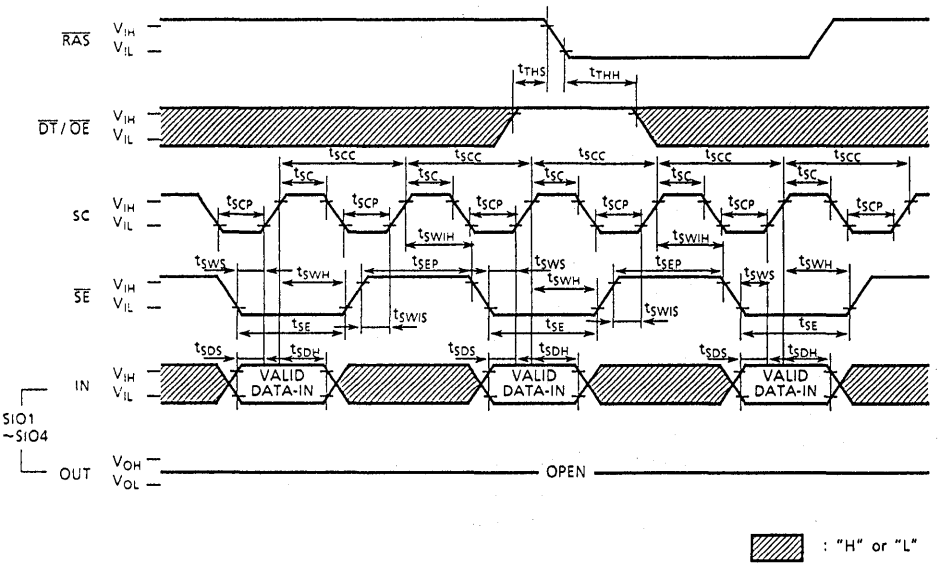
SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



SERIAL WRITE CYCLE ($\overline{SE}=V_{IL}$)



SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC524256BJ/BZ are multiplexed onto 9 address input pins ($A_0 \sim A_8$). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ to invoke the various random access and data transfer operating modes shown in Table 2.
$\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

WRITE MASK DATA / DATA INPUT AND OUTPUT : $W_1/IO_1 \sim W_4/IO_4$

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read transfer / pseudo write transfer / write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SERIAL INPUT / OUTPUT : SIO1~SIO4

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524256BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{RAS}$ falling edge ↓				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh
1	0	0	0	Write Transfer
1	0	0	1	Pseudo Write Transfer
1	0	1	*	Read Transfer
1	1	0	*	Read/Write per Bit
1	1	1	*	Read/Write

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓				Address		W/IO		Write Mask
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓ / $\overline{WE}$ ↓	WM1
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	–
Write Transfer	1	0	0	0	Row	TAP	*	*	–
Pseudo Write Transfer	1	0	0	1	Row	TAP	*	*	–
Read Transfer	1	0	1	*	Row	TAP	*	*	–
Write per Bit	1	1	0	*	Row	Column	WM1	DIN	Load use
Read/Write	1	1	1	*	Row	Column	*	DIN	–

* : "0" or "1" , TAP : SAM start address , – : not used

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC524256BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

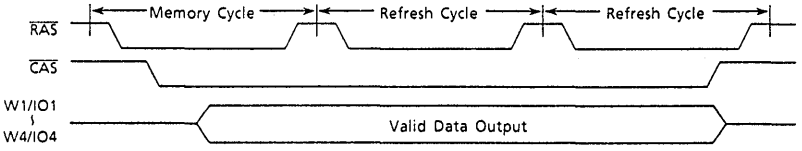


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When a "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i = 1~4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

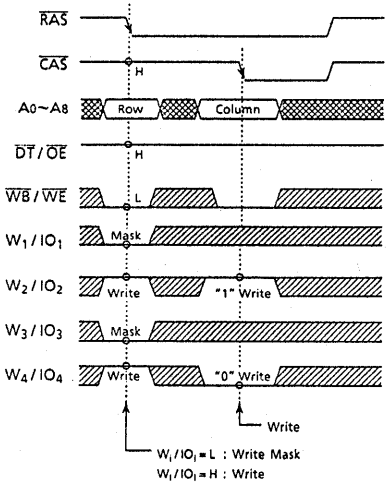


Figure 2. Write-per-bit timing cycle

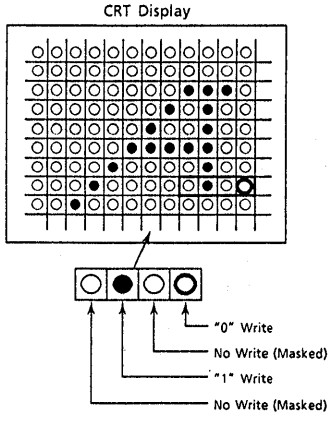
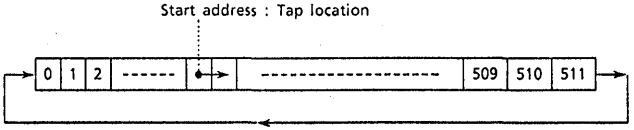


Figure 3. Corresponding bit-map

SAM PORT OPERATION

The TC524256BJ/BZ is provided with a 512 words by 4 bits serial access memory (SAM). High speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read transfer/write transfer/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC524256BJ/BZ features the internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 4. During a transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).

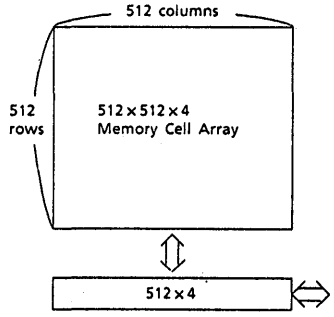


Figure 4. Data Transfer

As shown in Table 5, the TC524256BJ/BZ supports three types of transfer operations: Read transfer, Write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ latched at the falling edge of $\overline{RAS}$. During data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/Pseudo write transfer). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$				Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$				
H	L	H	*	Read Transfer	RAM → SAM	512×4	Input → Output
H	L	L	L	Write Transfer	SAM → RAM	512×4	Output → Input
H	L	L	H	Pseudo Write Transfer	-	-	Output → Input

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" and $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode.

In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 5 shows the operation block diagram for read transfer operation.

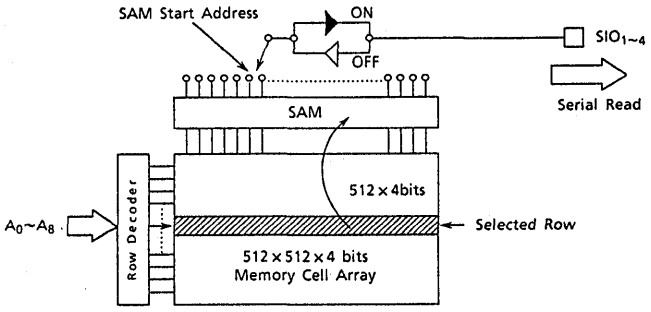


Figure 5. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 6.

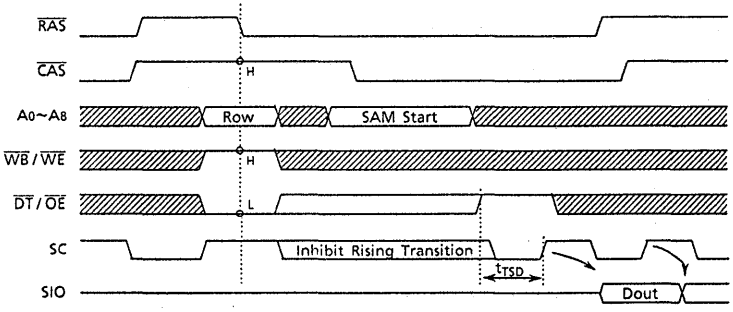


Figure 6. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 7.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min.

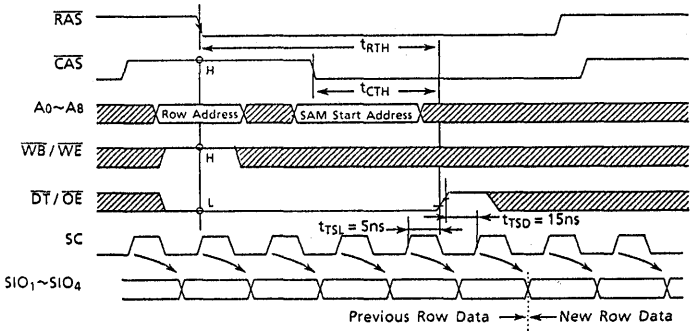


Figure 7. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "low" at the falling edge of $\overline{RAS}$.

Figure 8 and 9 show the timing diagram and block diagram for write transfer operations, respectively.

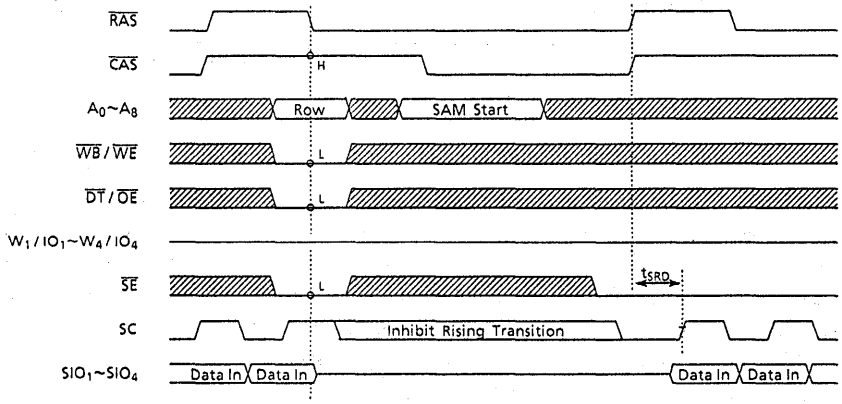


Figure 8. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

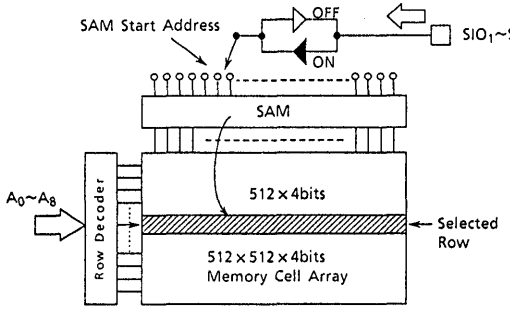


Figure 9. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

REGISTER OPERATION SEQUENCE (EXAMPLE)

Figure 10 illustrates an example of register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511) and wraps around to the least significant address location. The SAM address is incremented as long as SC is clocked.

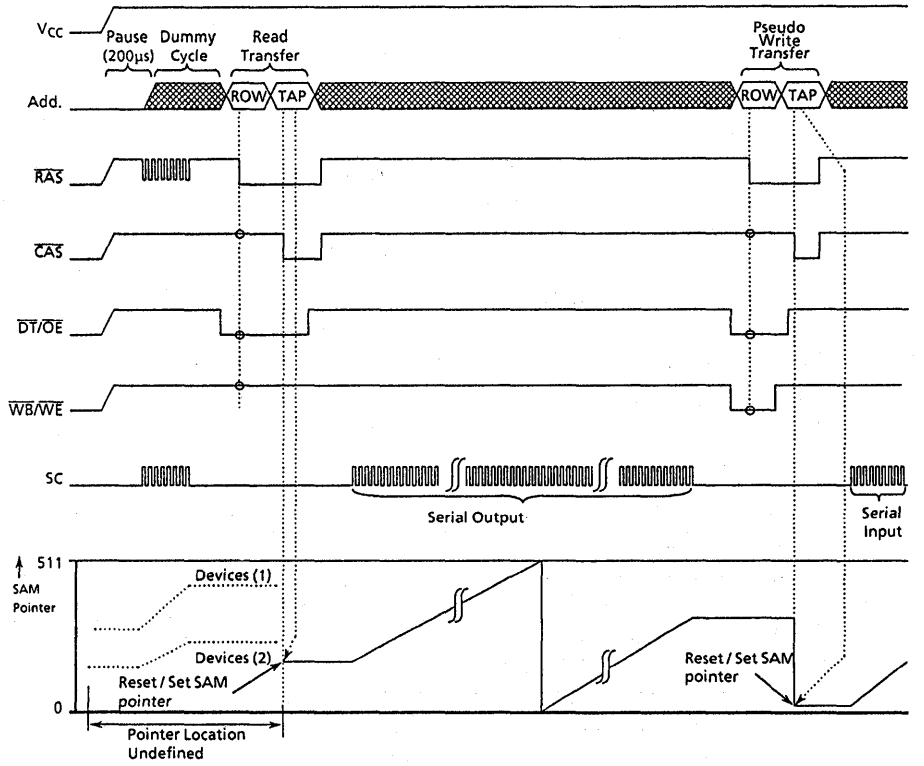
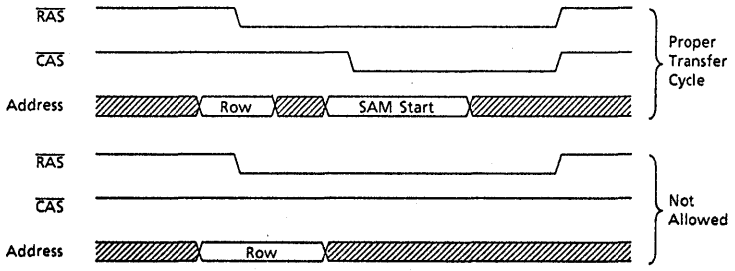


Figure 10. Example of SAM Register Operation Seguence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

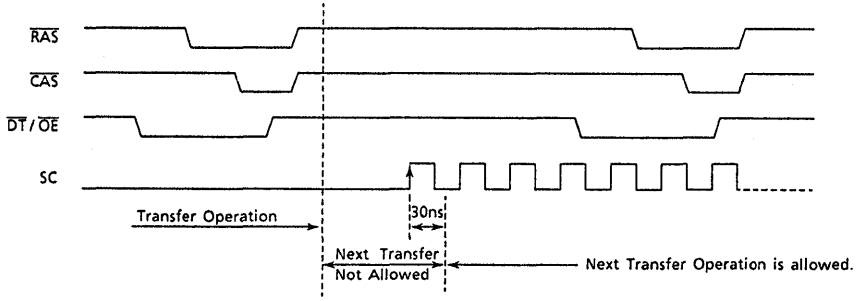
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



READ TRANSFER CYCLE AFTER READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC524256BJ/BZ is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
WM1 Register	Write Enable
TAP pointer	Invalid

262,144WORDS×4BITS MULTIPORT DRAM

PRELIMINARY

DESCRIPTION

The TC524258BJ/BZ is a CMOS multiport memory equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The TC524258BJ/BZ supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport video RAM operating modes, the TC524258BJ/BZ features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port. The TC524258BJ/BZ is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC524258BJ/BZ -80	TC524258BJ/BZ -10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	85mA	70mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

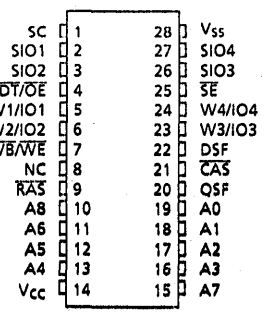
- Organization
  - RAM Port : 262,144words×4bits
  - SAM Port : 512words×4bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit
  - Flash Write, Block Write
  - 512 refresh cycles/8ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read/Write Transfer
- Package
  - TC524258BJ : SOJ28-P-400
  - TC524258BZ : ZIP28-P-400

PIN NAME

A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
CAS	Column Address Strobe
$\overline{DT}$/$\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}$/$\overline{WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1~W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO4	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

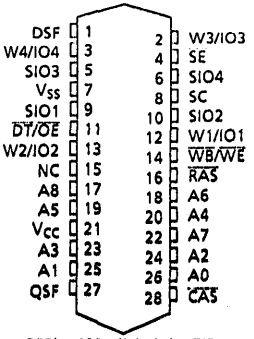
PIN CONNECTION

TC524258BJ



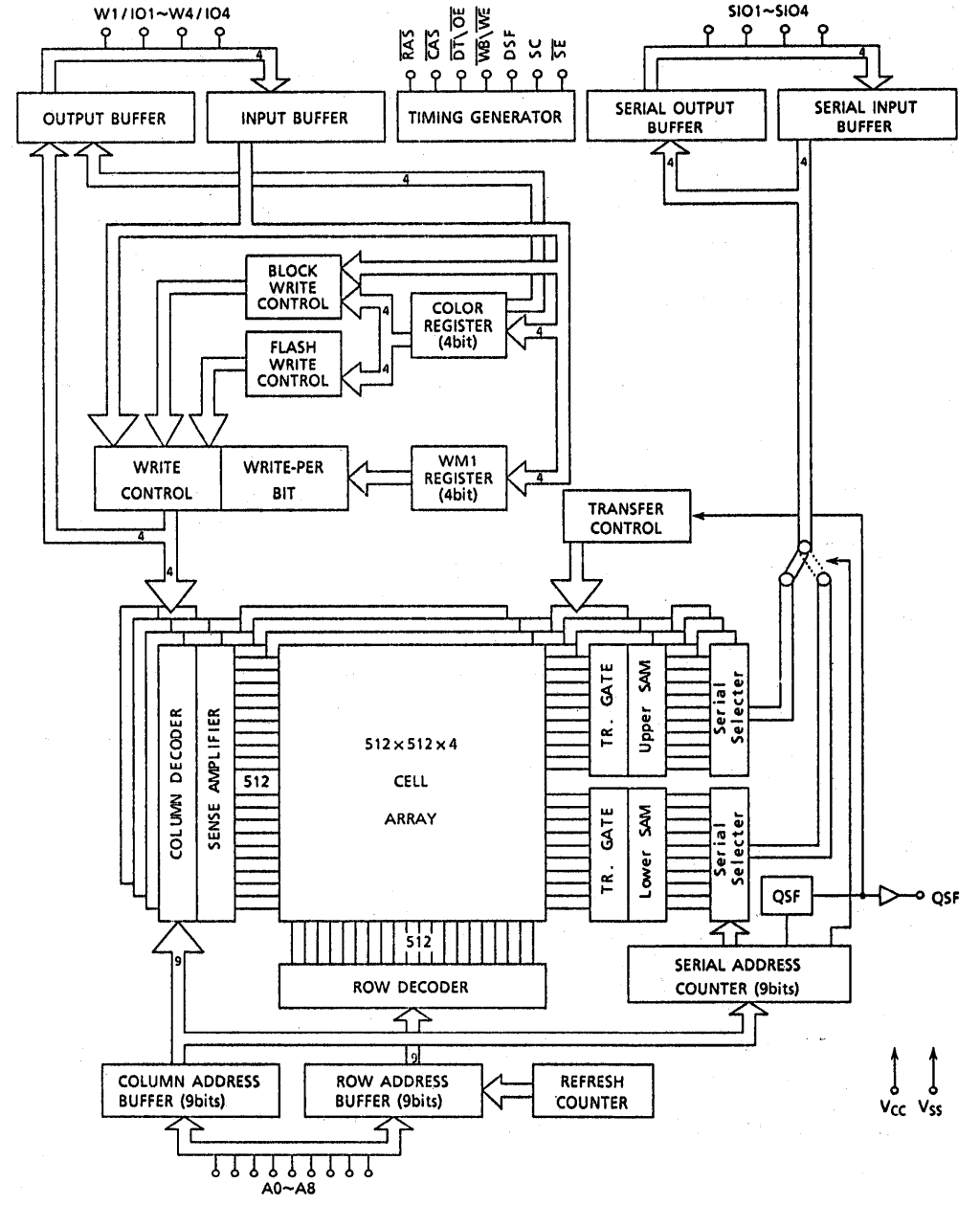
28Pin 400mil SOJ
JEDEC Standard

TC524258BZ



28Pin 400mil height ZIP
JEDEC Standard

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	−1.0~7.0	V	1
V_{CC}	Power Supply Voltage	−1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~150	°C	1
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	−	7	pF
C_{IO}	Input/Output Capacitance	−	9	
C_O	Output Capacitance (QSF)	−	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC524258BJ/BZ-80		TC524258BJ/BZ-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC1}	–	85	–	70	mA	3, 4
	Active	I_{CC1A}	–	125	–	110		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)	Standby	I_{CC3}	–	85	–	70		3, 4
	Active	I_{CC3A}	–	125	–	110		3, 4
PAGE MODE CURRENT ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min.)	Standby	I_{CC4}	–	75	–	60		3, 4
	Active	I_{CC4A}	–	115	–	100		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT ($\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$, t_{RC} = t_{RC} min.)	Standby	I_{CC5}	–	85	–	70		3, 4
	Active	I_{CC5A}	–	125	–	110		3, 4
DATA TRANSFER CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC6}	–	105	–	90		3, 4
	Active	I_{CC6A}	–	145	–	130		3, 4
FLASH WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC7}	–	85	–	70		3, 4
	Active	I_{CC7A}	–	125	–	110		3, 4
BLOCK WRITE CURRENT ($\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} min.)	Standby	I_{CC8}	–	95	–	80		3, 4
	Active	I_{CC8A}	–	135	–	120		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT 0V ≤ V_{IN} ≤ 6.5V, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT 0V ≤ V_{OUT} ≤ 5.5V, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE I_{OUT} = – 2mA	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE I_{OUT} = 2mA	V_{OL}	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC524258BJ/BZ-80		TC524258BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC524258BJ/BZ-80		TC524258BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130		ns	13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0			
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{FSR}	DSF Set-UP Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	55		70			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

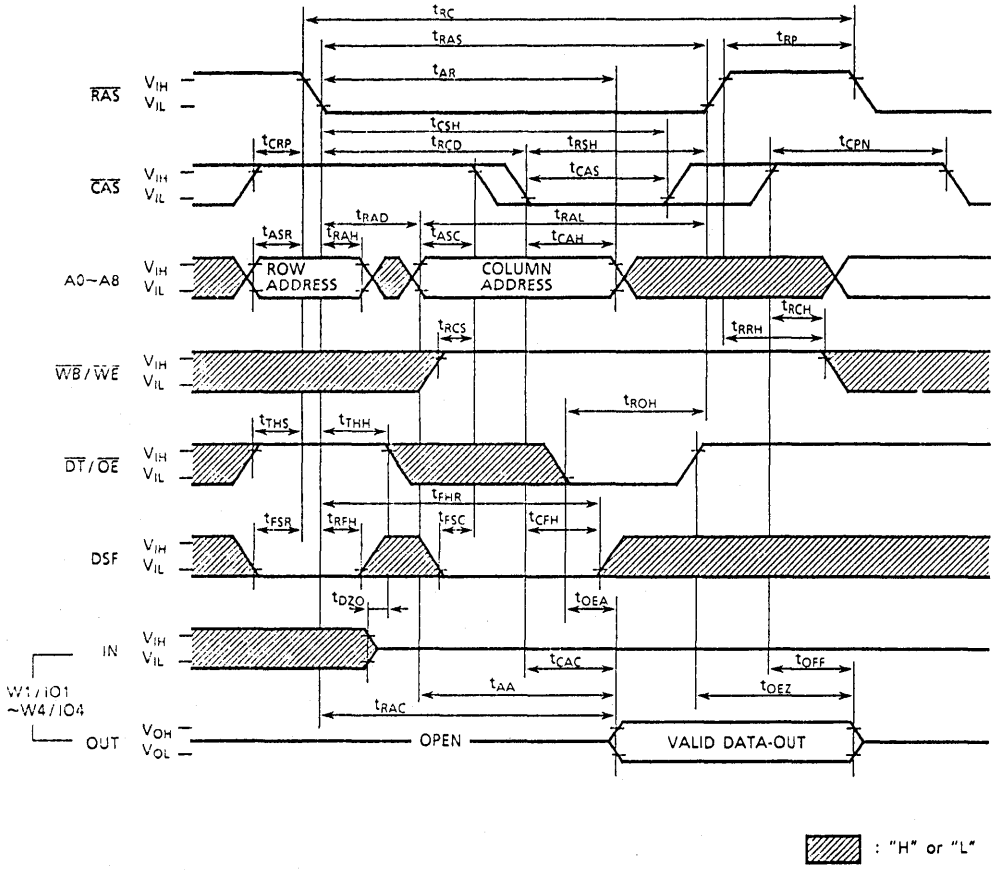
SYMBOL	PARAMETER	TC524258BJ/BZ-80		TC524258BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			
t_{STS}	Split Transfer Set-Up Time	30		30			
t_{STH}	Split Transfer Hold Time	30		30			
t_{SQD}	SC-QSF Delay Time		25		25		
t_{TQD}	$\overline{DT}$-QSF Delay Time		25		25		
t_{CQD}	$\overline{CAS}$-QSF Delay Time		35		35		
t_{RQD}	$\overline{RAS}$-QSF Delay Time		75		90		

NOTES :

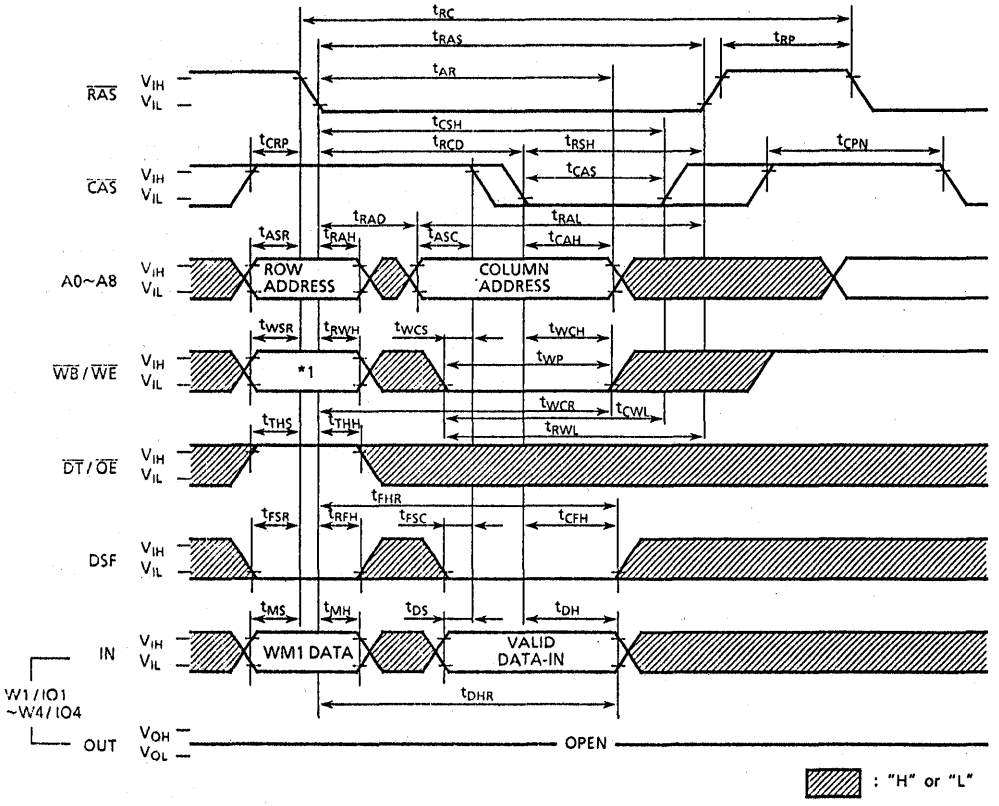
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume $t_T = 5ns$.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF.
   D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   D_{OUT} reference levels : $V_{OH}/V_{OL} = 2.0V/0.8V$.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met.
    $t_{RCD\,(max.)}$ is specified as a reference point only : If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only : If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.

TIMING WAVEFORM

READ CYCLE



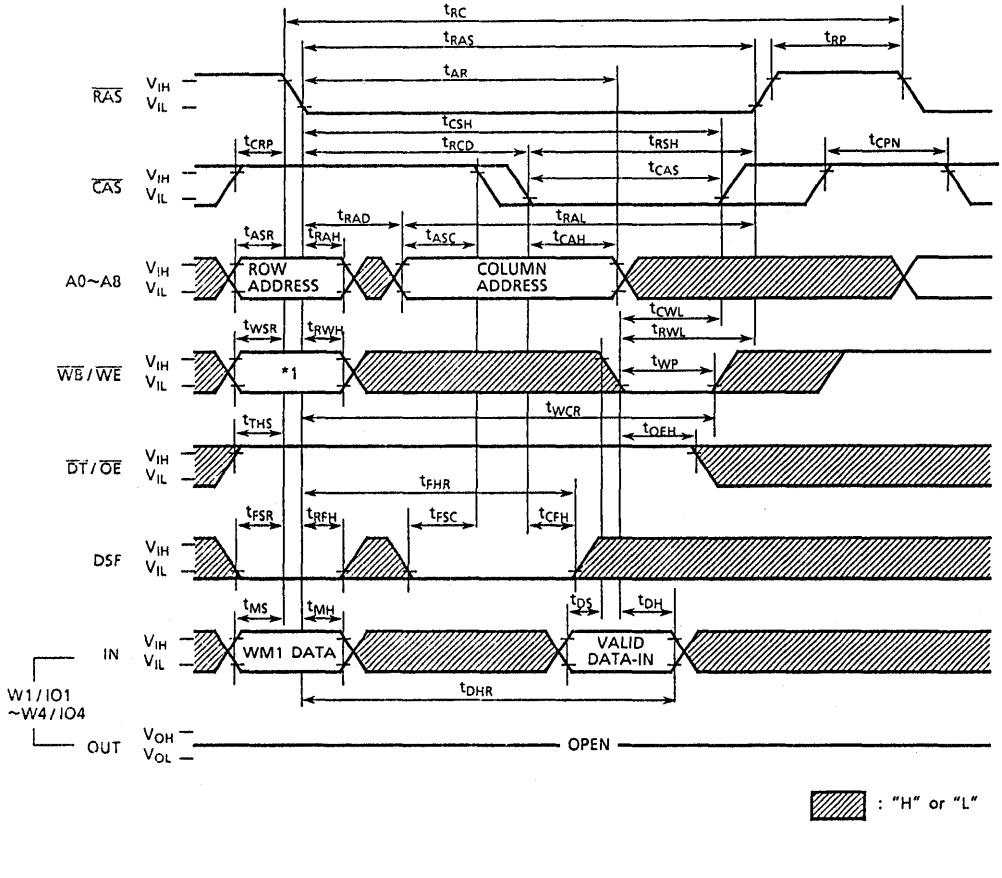
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

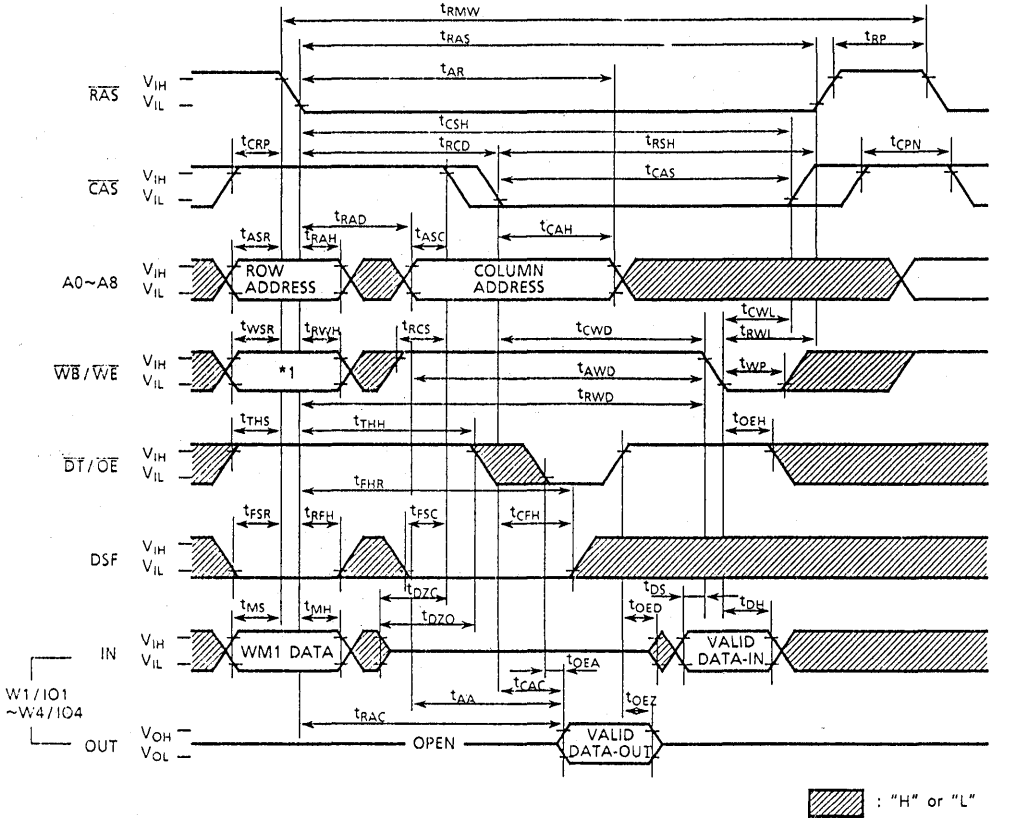
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

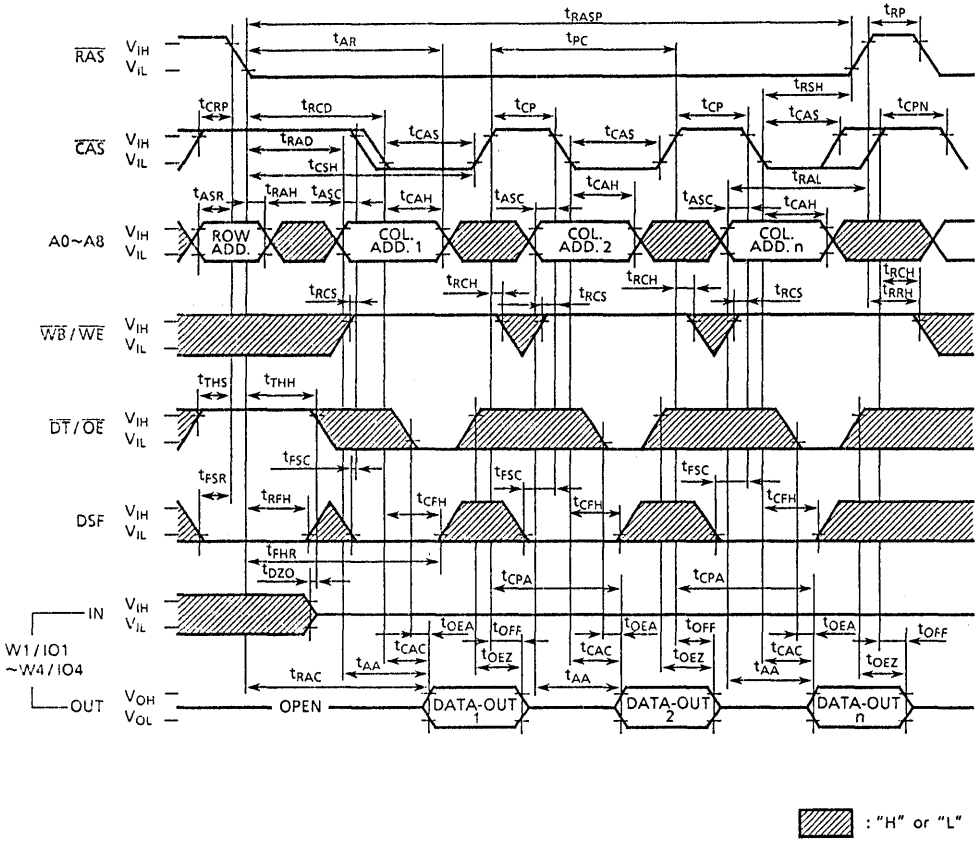
READ - MODIFY - WRITE CYCLE



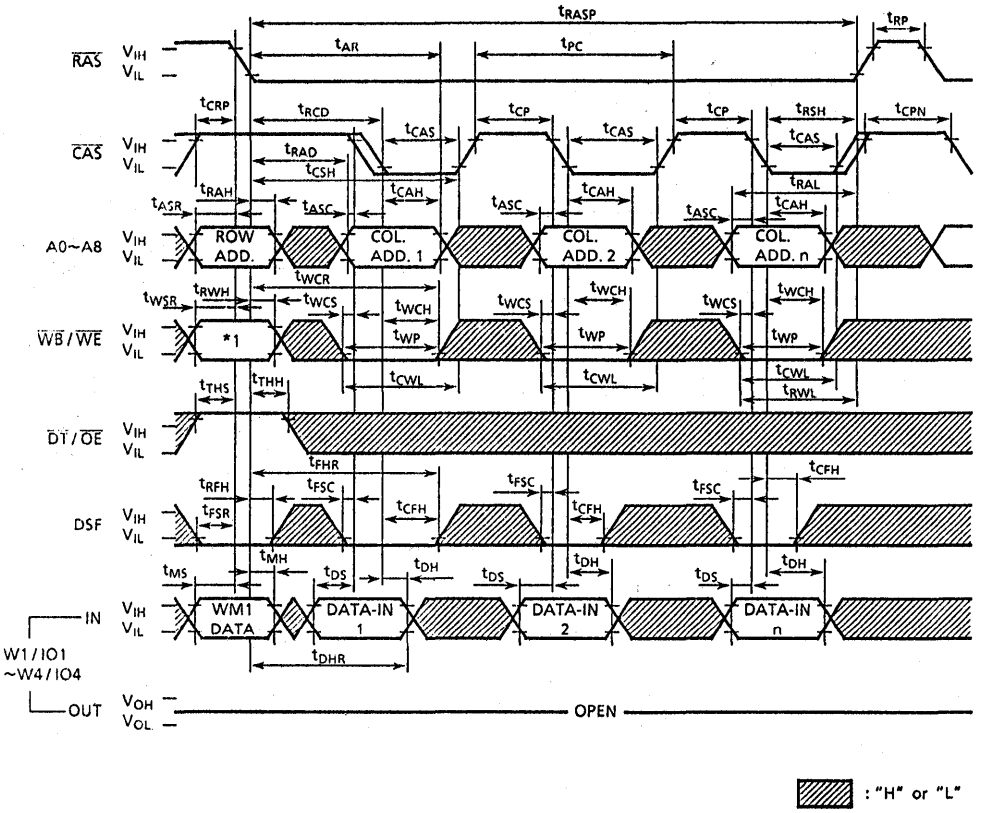
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



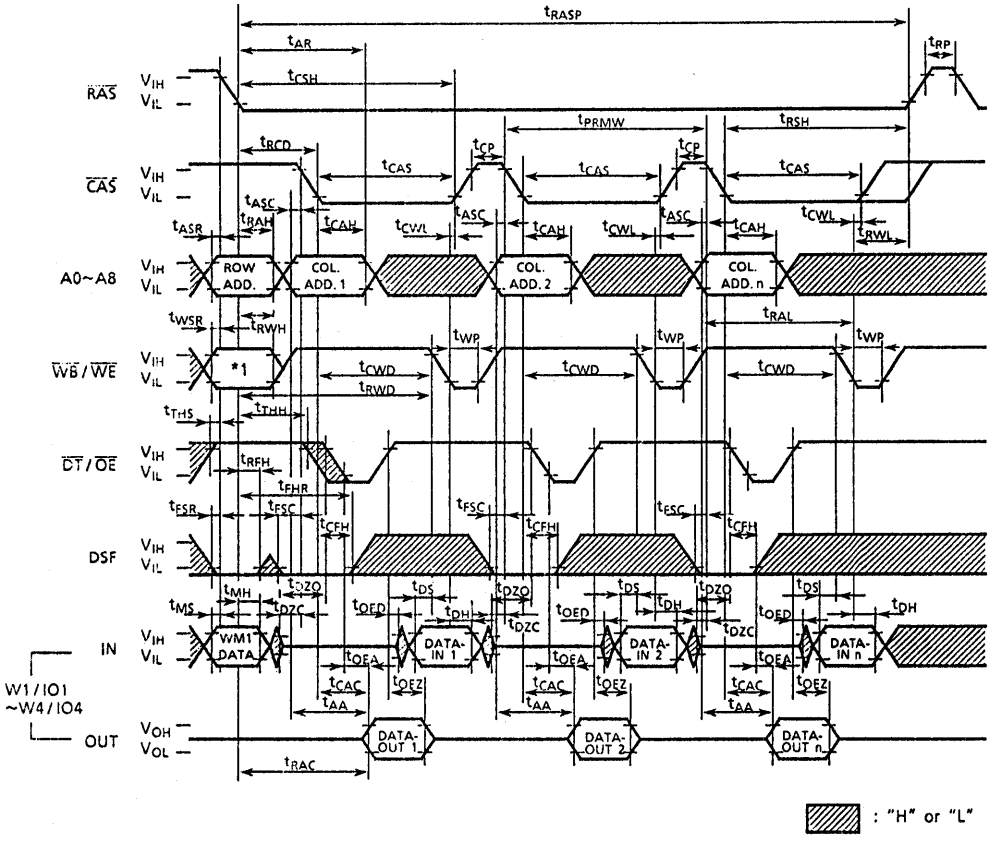
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

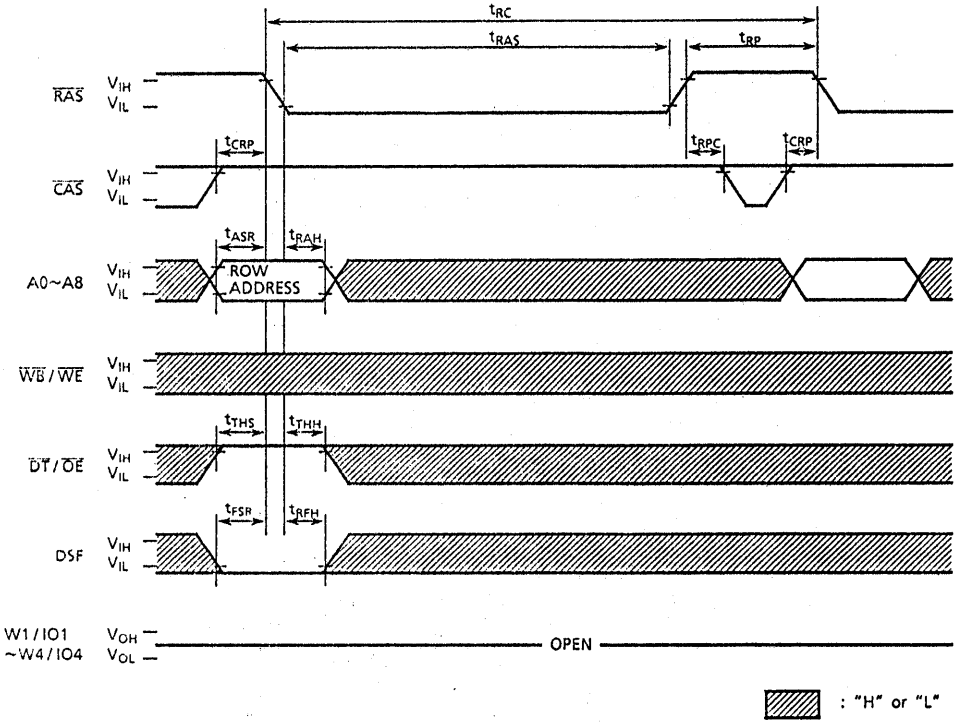
FAST PAGE MODE READ - MODIFY - WRITE CYCLE



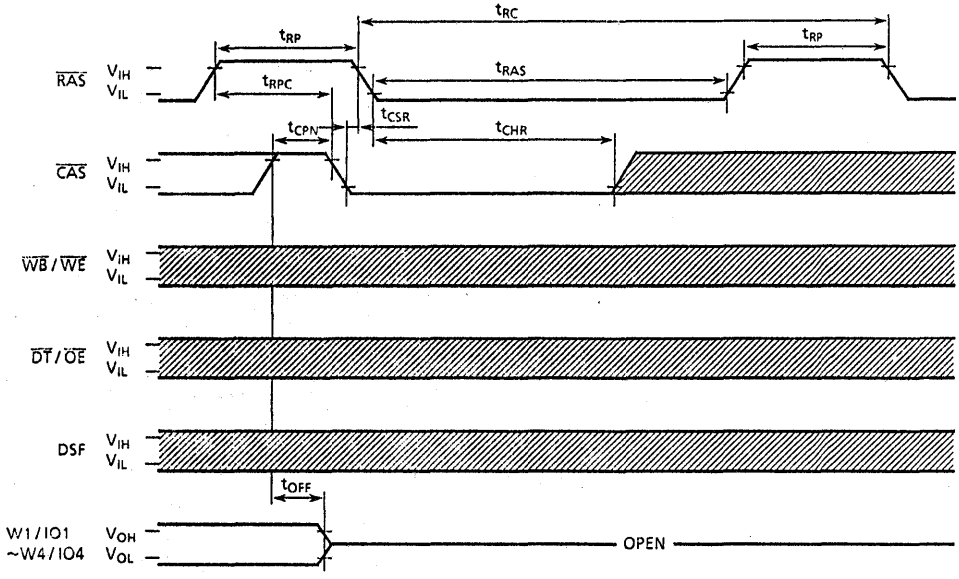
*1 $\overline{WB}$ / $\overline{WE}$	W1 / IO1~W4 / IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data : 0 : Write Disable
1 : Write Enable

$\overline{RAS}$ ONLY REFRESH CYCLE



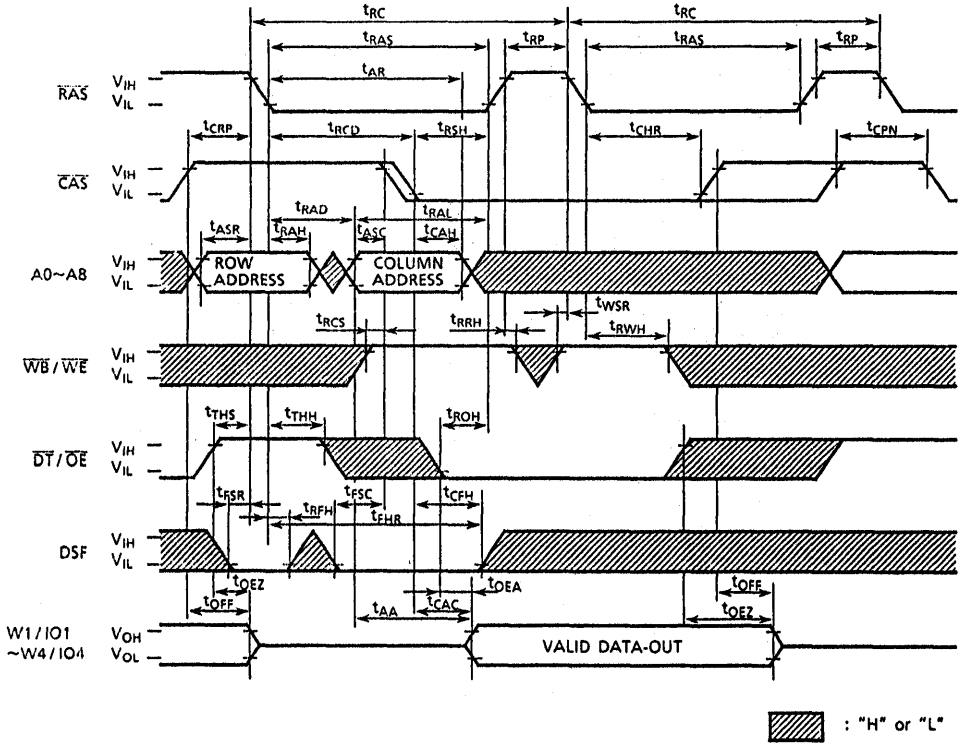
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



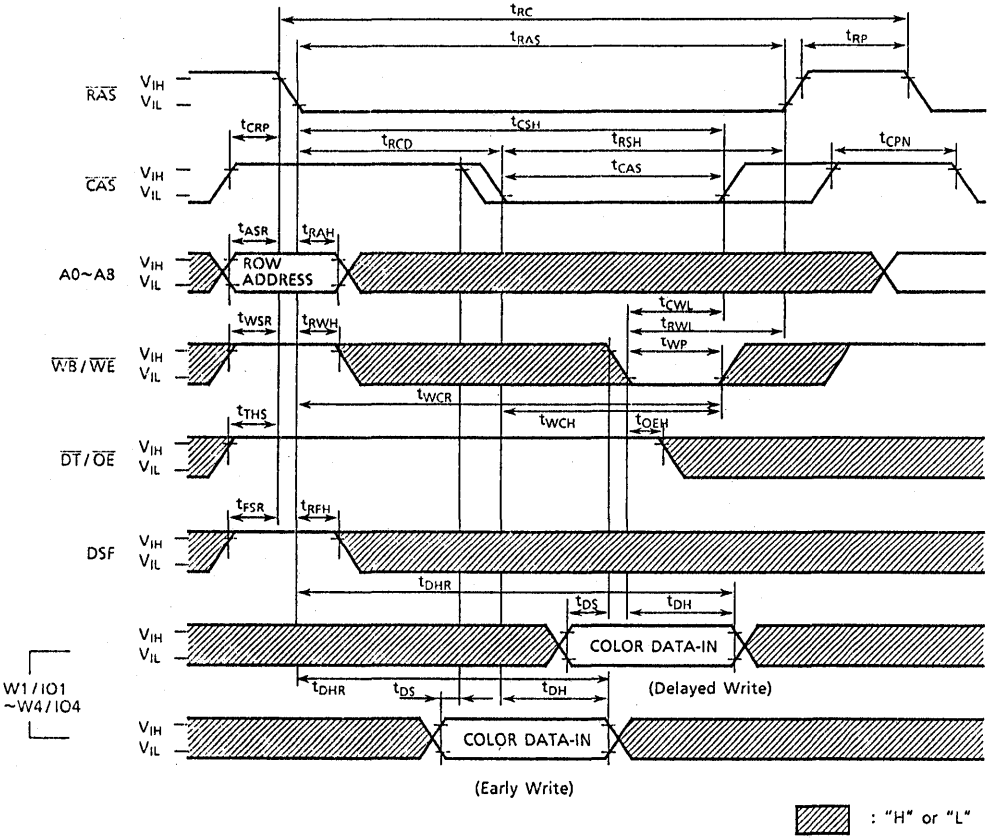
Note : A0 ~ A8 = Don't Care ("H" or "L")

: "H" or "L"

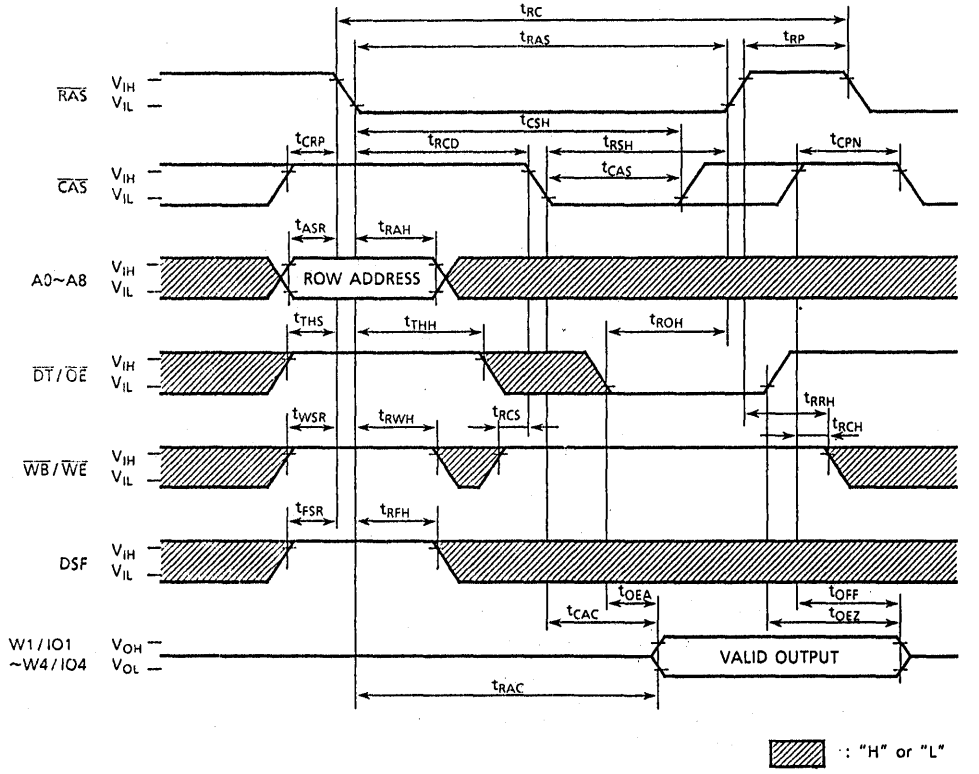
HIDDEN REFRESH CYCLE



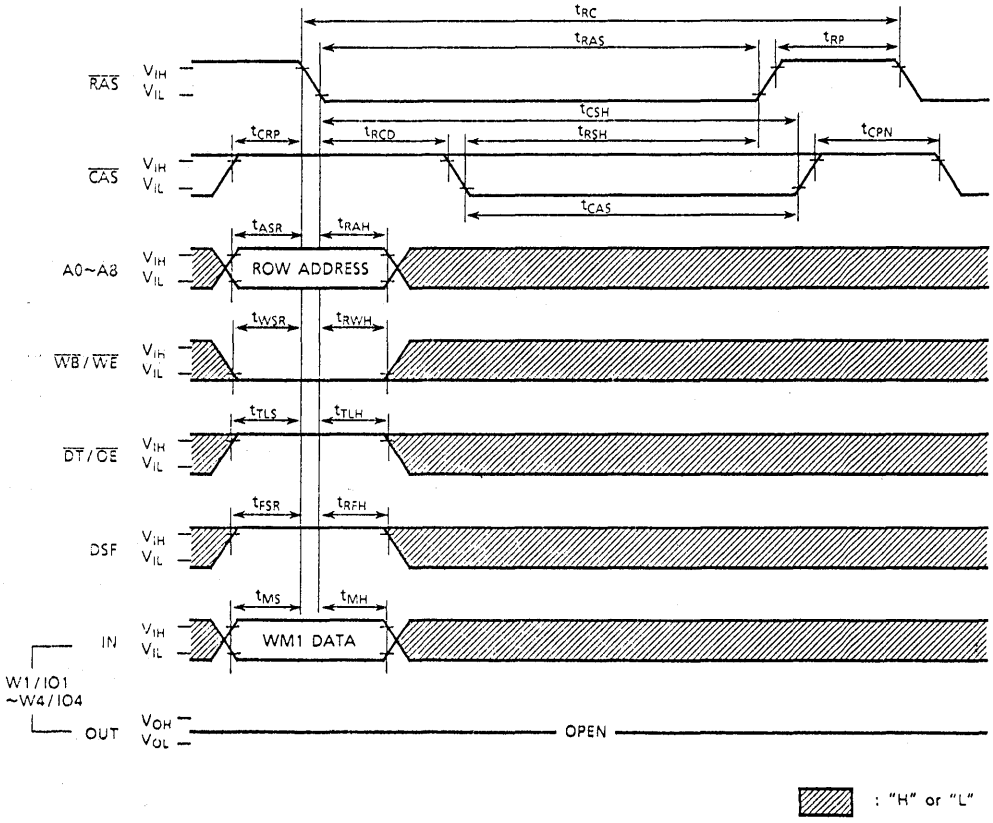
LOAD COLOR REGISTER CYCLE



READ COLOR REGISTER CYCLE

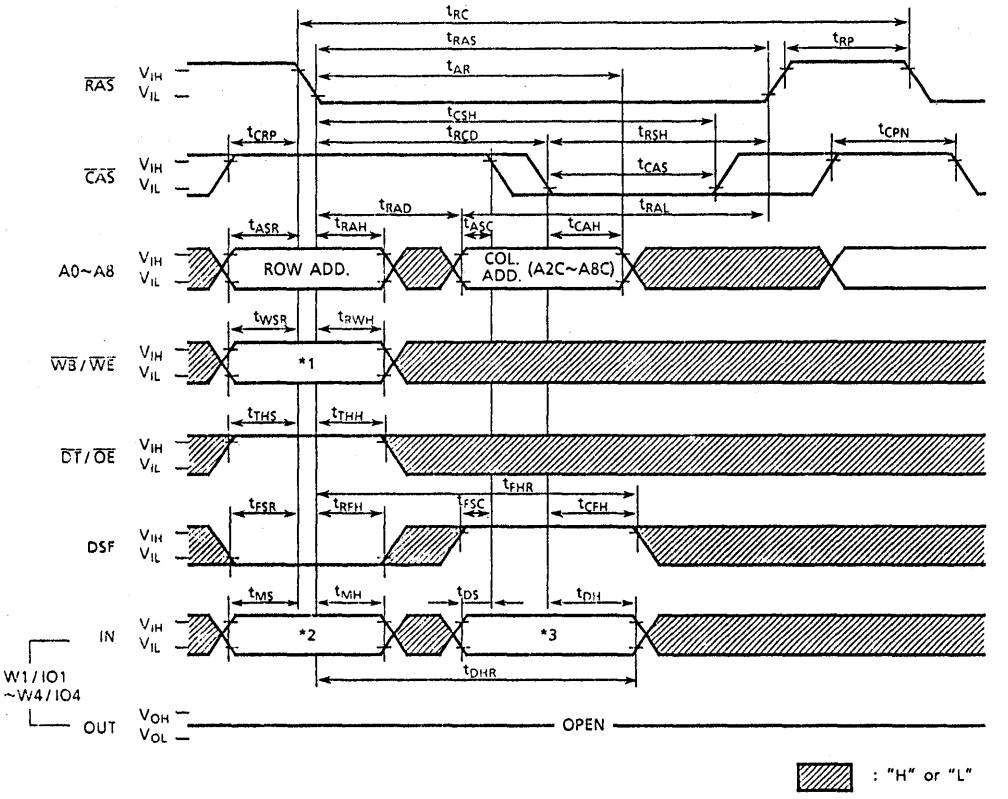


FLASH WRITE CYCLE



WM1 DATA	CYCLE
0	Flash Write Disable
1	Flash Write Enable

BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W4/IO4	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

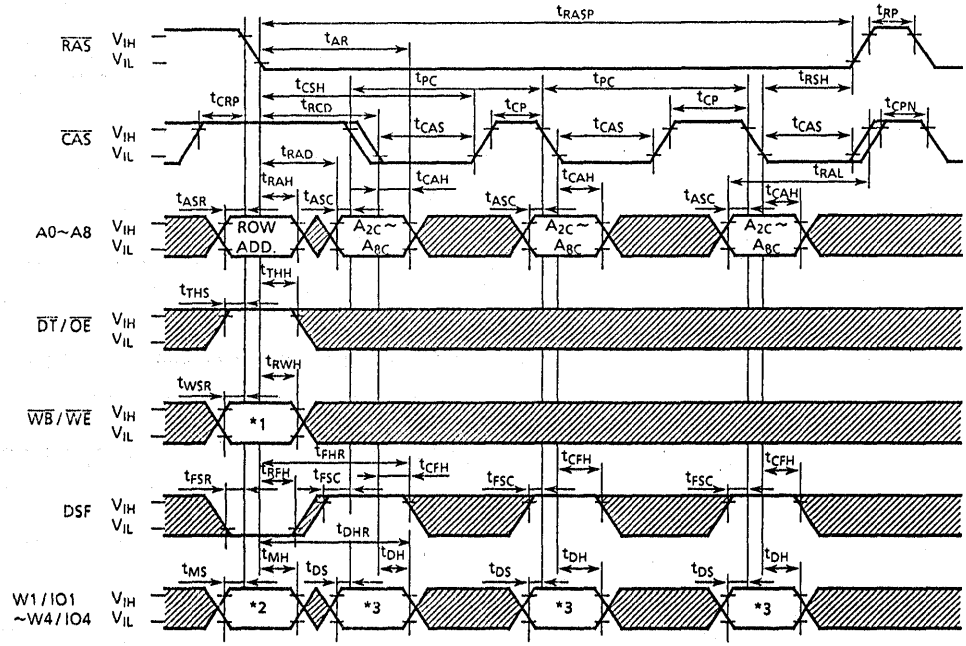
WM1 data : 0 : Write Disable
1 : Write Enable

*3) COLUMN SELECT

W1/IO1 — Column 0 ($A_{1C}=0$, $A_{0C}=0$)
W2/IO2 — Column 1 ($A_{1C}=0$, $A_{0C}=1$)
W3/IO3 — Column 2 ($A_{1C}=1$, $A_{0C}=0$)
W4/IO4 — Column 3 ($A_{1C}=1$, $A_{0C}=1$)

Wn/IOn
= 0 : Disable
= 1 : Enable

PAGE MODE BLOCK WRITE CYCLE



: "H" or "L"

*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W4/IO4	CYCLE
0	WM1 Data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

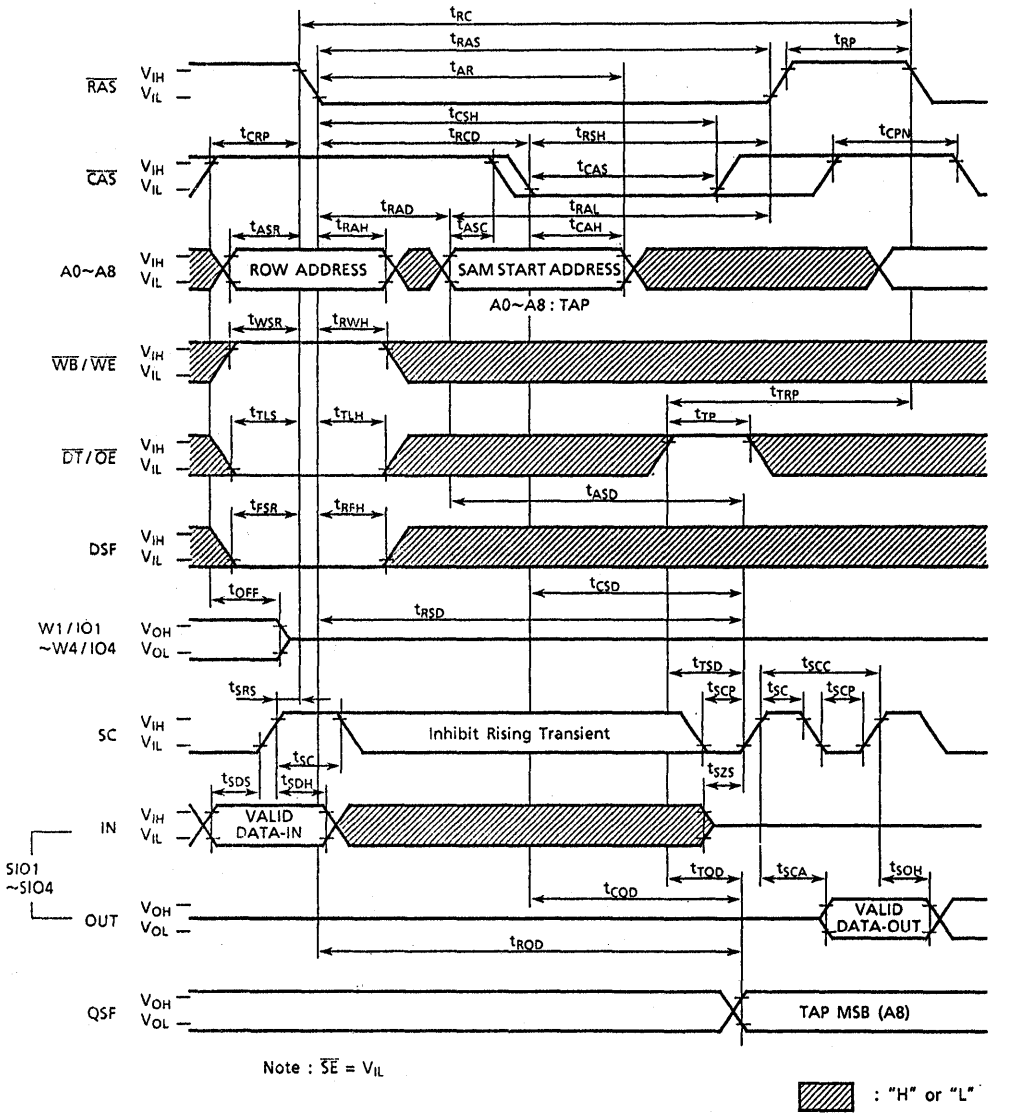
WM1 data : 0 : Write Disable
1 : Write Enable

*3) COLUMN SELECT

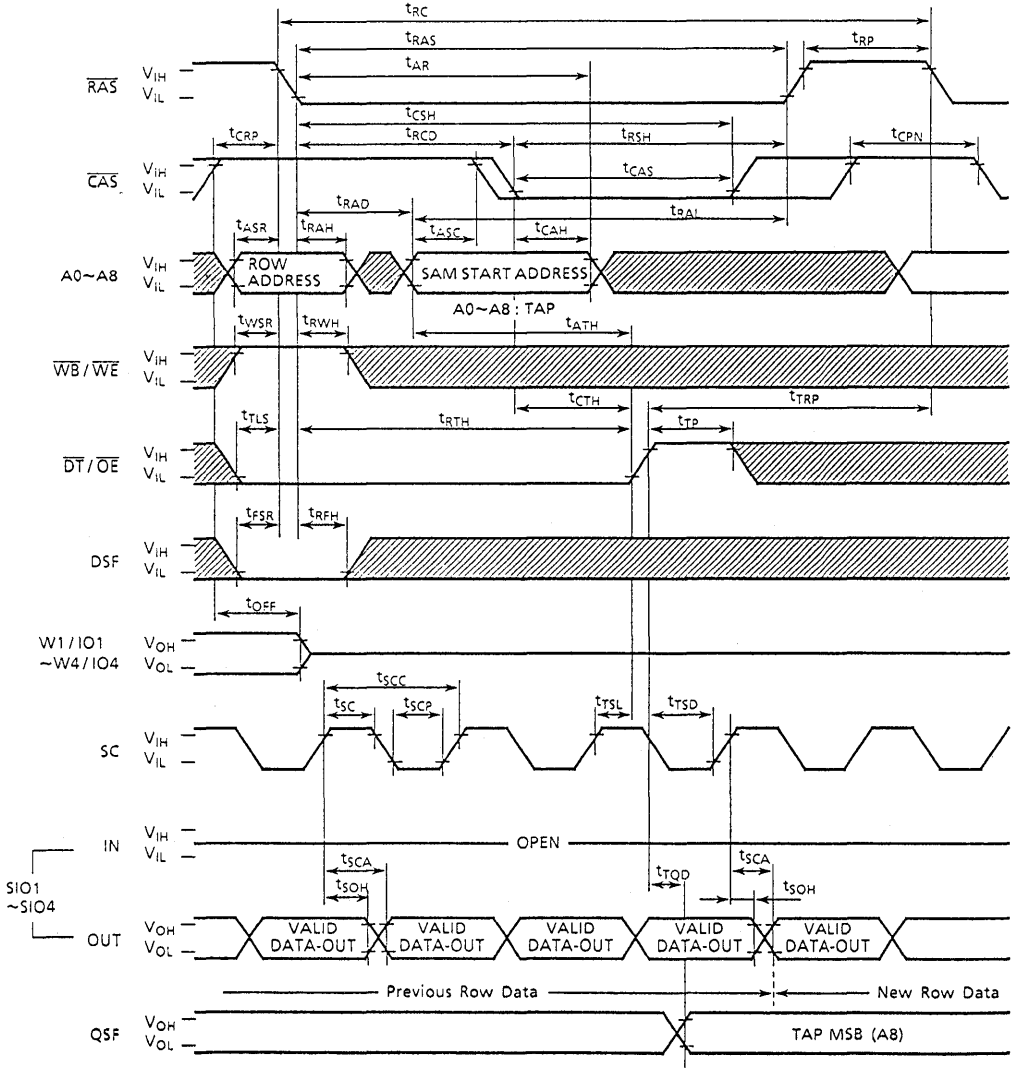
W1/IO1 – Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 – Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 – Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 – Column 3 (A_{1C} = 1, A_{0C} = 1)

} Wn/IOn
= 0 : Disable
= 1 : Enable

READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



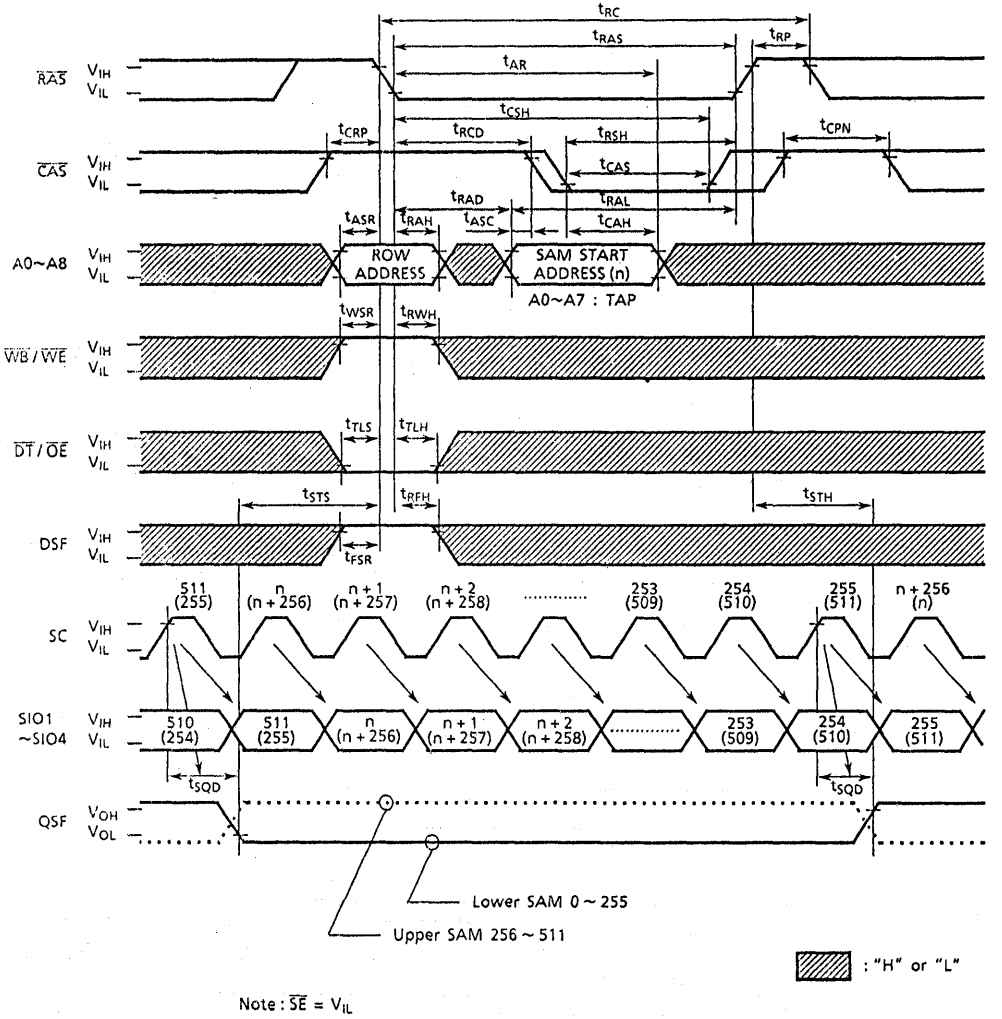
REAL TIME READ TRANSFER CYCLE



Note : $\overline{SE}$ = V_{IL}

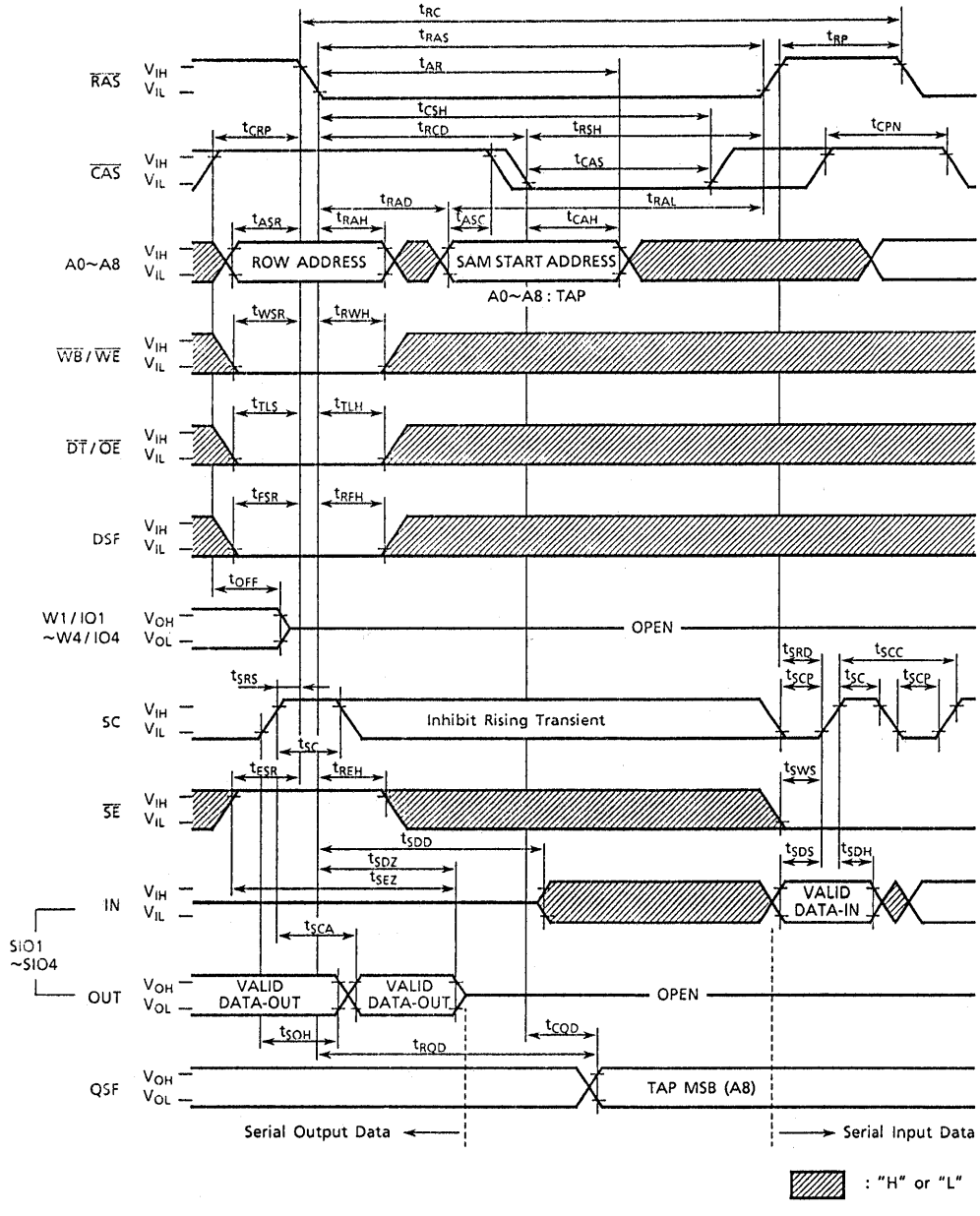
: "H" or "L"

SPLIT READ TRANSFER CYCLE

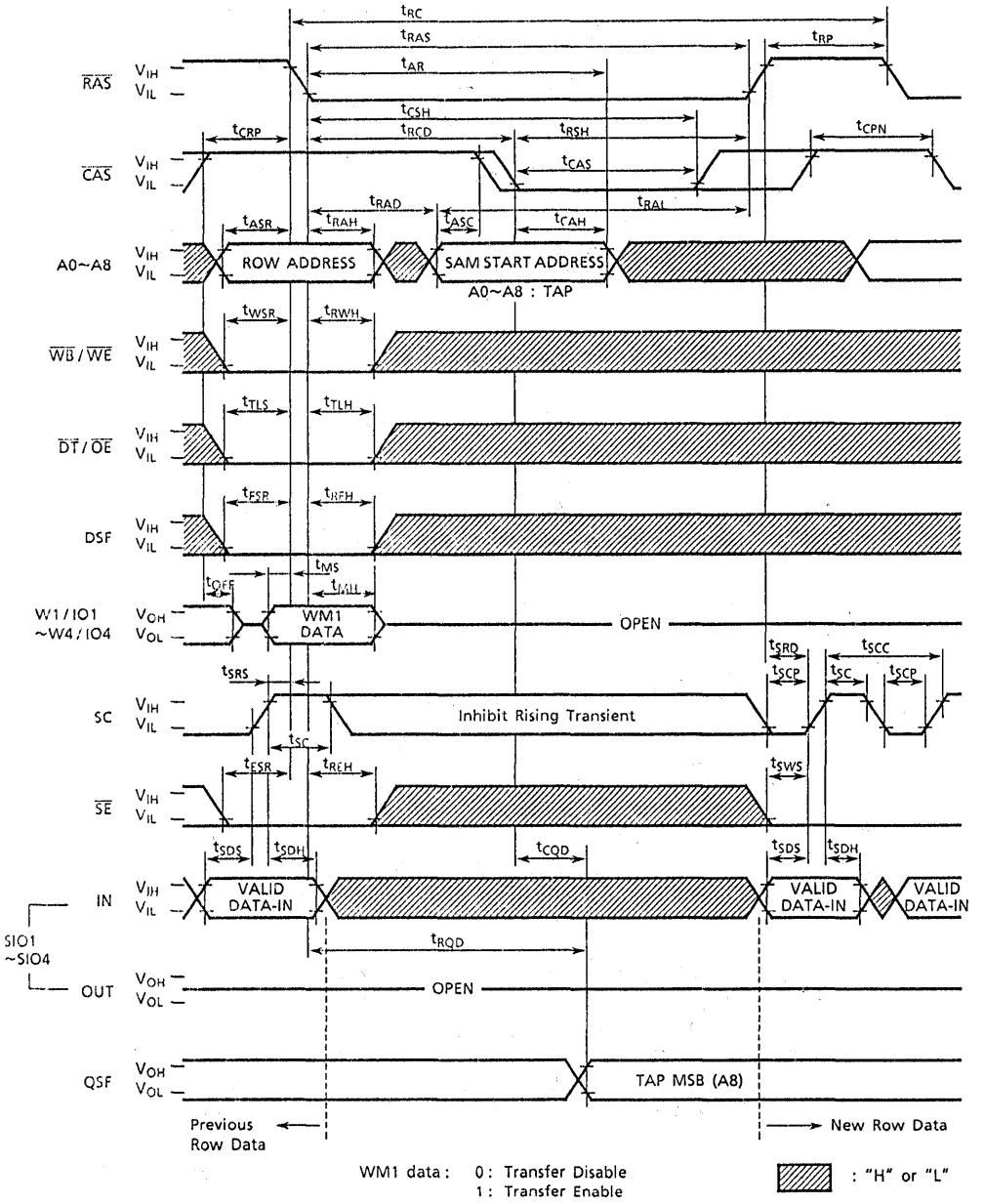


Note : $\overline{SE}$ = V_{IL}

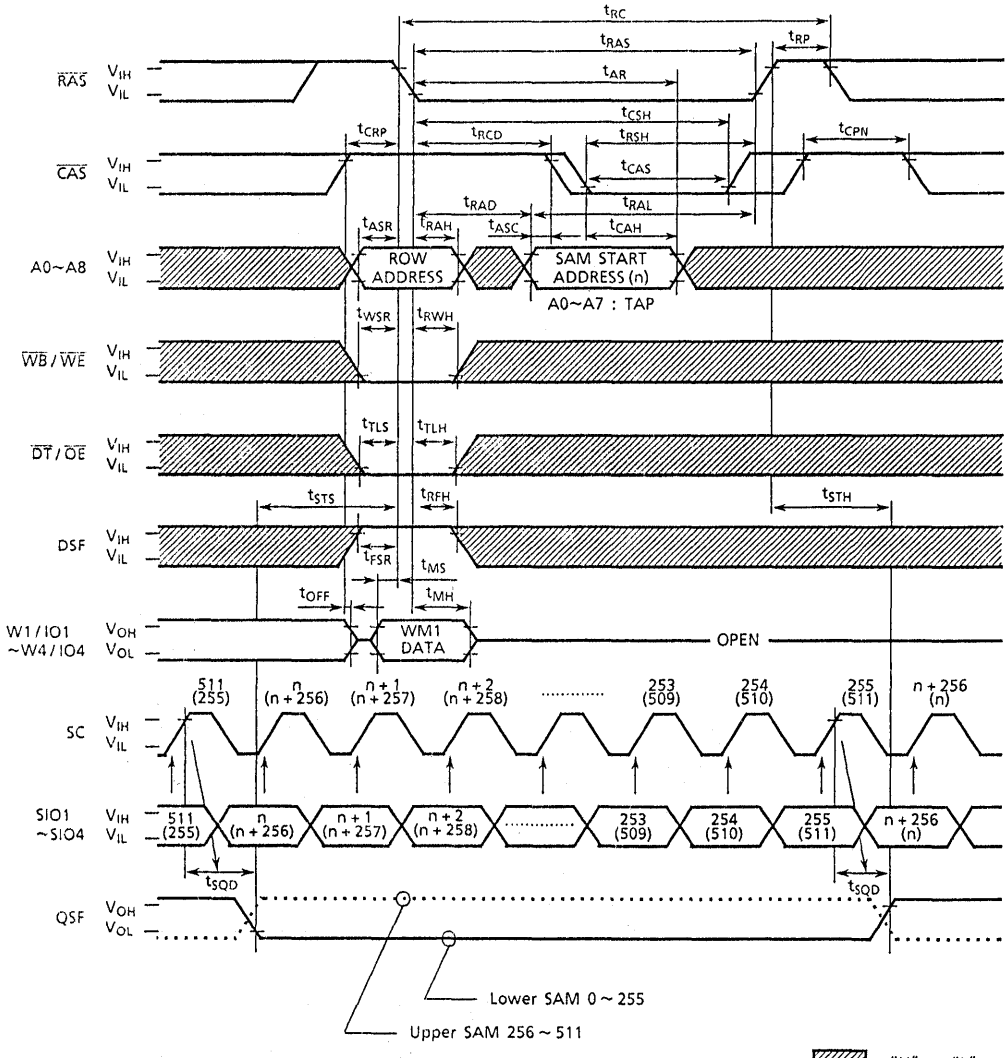
PSEUDO WRITE TRANSFER CYCLE



WRITE TRANSFER CYCLE

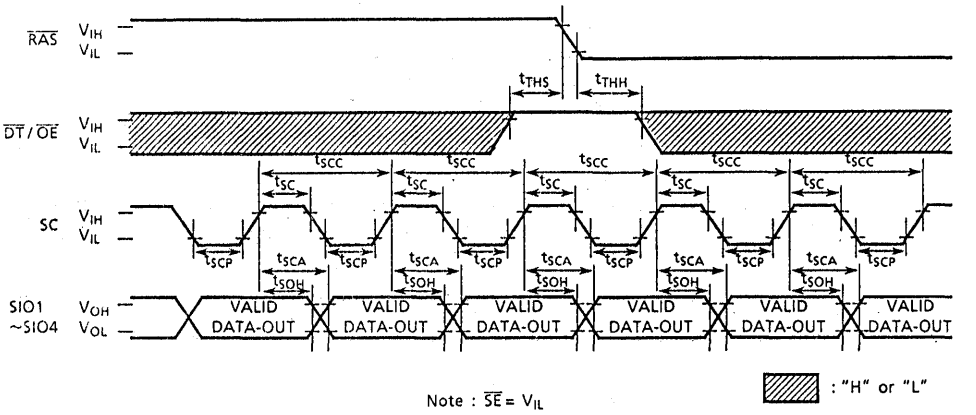


SPLIT WRITE TRANSFER CYCLE



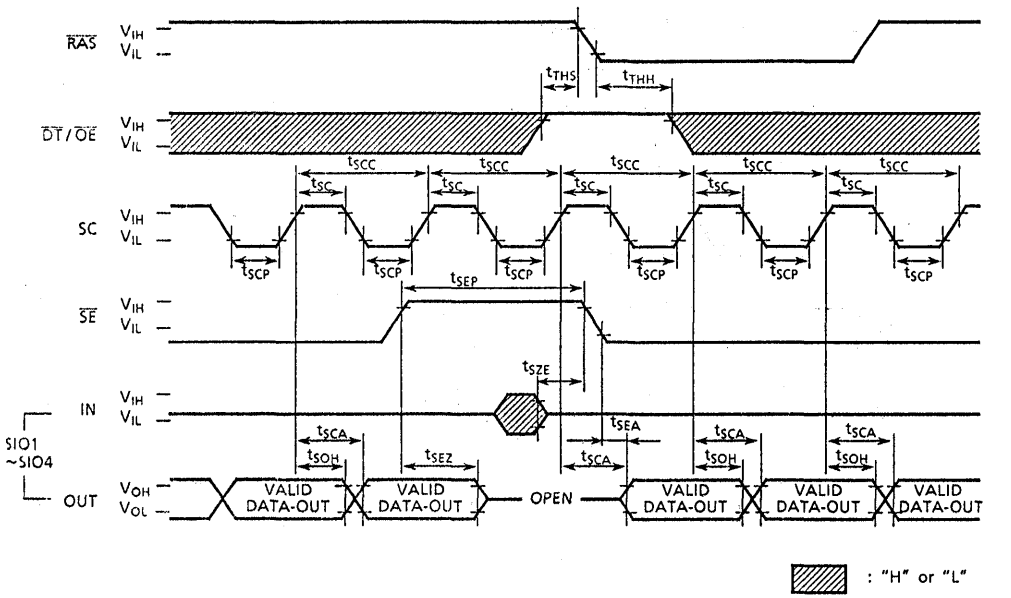
Note : $\overline{SE}$ = V_{IL}

SERIAL READ CYCLE ($\overline{SE}$=V_{IL})

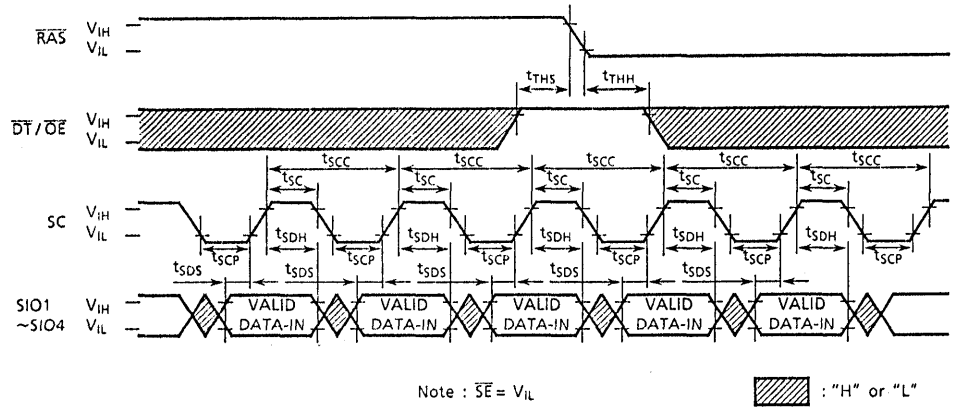


Note : $\overline{SE}$ = V_{IL}

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



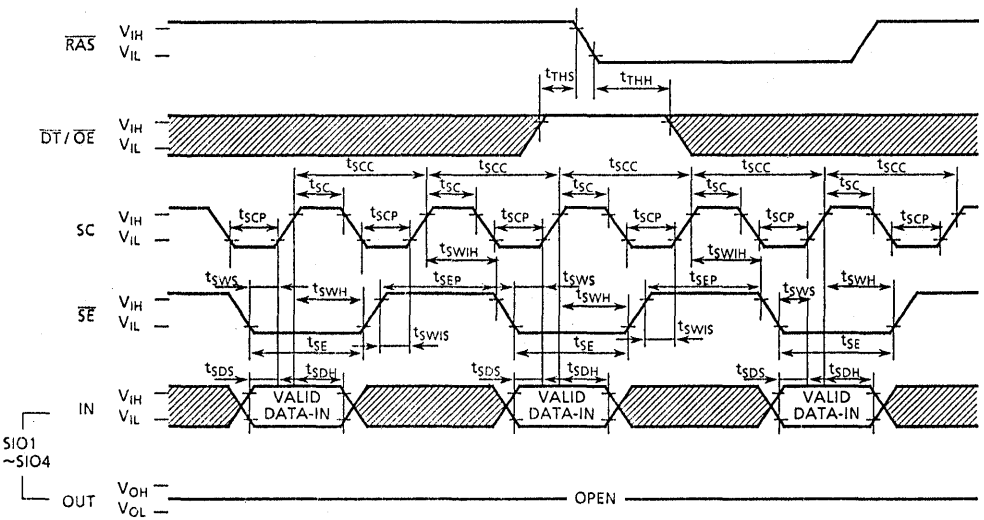
SERIAL WRITE CYCLE ($\overline{SE}$ = V_{IL})



Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



: "H" or "L"

PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC524258BJ/BZ are multiplexed onto 9 address input pins ($A_0 \sim A_8$). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{RAS}$ control, either read/write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT / WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked-write transfer).

WRITE MASK DATA / DATA INPUT AND OUTPUT : $W_1/IO_1 \sim W_4/IO_4$

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer (8-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read / pseudo write / write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT : DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of flash write, block write, load color register and split read/write transfer can be invoked.

SPECIAL FUNCTION OUTPUT : QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0~255) is being accessed and QSF "high" indicates that the upper split SAM (Bit 256~511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

SERIAL INPUT/OUTPUT : SIO1~SIO4

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524258BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{CAS}$ falling edge				DSF	0	0	1	1
$\overline{RAS}$ falling edge				DSF	0	1	0	1
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$					
0	*	*	*		$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0		Masked Write Transfer	Split Write Transfer with	Masked Write Transfer	Split Write Transfer with
1	0	0	1		Pseudo Write Transfer	Mask	Pseudo Write Transfer	Mask
1	0	1	*		Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*		Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	*		Read/Write	Load Color	Block Write	Load Color

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$ ↓		WM1	Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	*	–	–	–	–	–
Masked Write Transfer	1	0	0	0	0	*	Row	TAP	WM1	*	*	WM1	Load use	–
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	–	–	–
Split Write Transfer	1	0	0	1	*	*	Row	TAP	WM1	–	*	WM1	Load use	–
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	–	–	–
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	–	–	–
Write per Bit	1	1	0	0	*	0	Row	Column	WM1	–	DIN	WM1	Load use	–
Masked Block Write	1	1	0	0	*	1	Row	Column A2C-8C	WM1	Column Select	–	WM1	Load use	use
Masked Flash Write	1	1	0	1	*	*	Row	*	WM1	–	*	WM1	Load use	use
Read Write	1	1	1	0	*	0	Row	Column	*	–	DIN	–	–	–
Block Write	1	1	1	0	*	1	Row	Column A2C-8C	*	Column Select	–	–	–	use
Load Color	1	1	1	1	*	*	Row	*	*	–	Color	–	–	Load

* : "0" or "1" , TAP : SAM start address , – : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked : $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split write transfer, split read transfer, flash write and load color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write special feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC524258BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

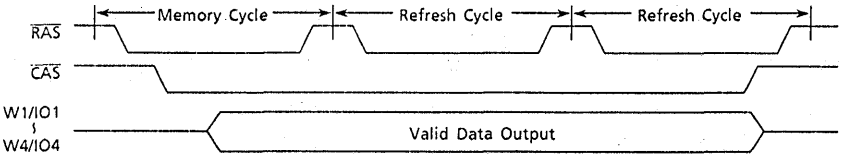


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB}/\overline{WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When a "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

Table 3. Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	W_i/IO_i (i = 1~4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

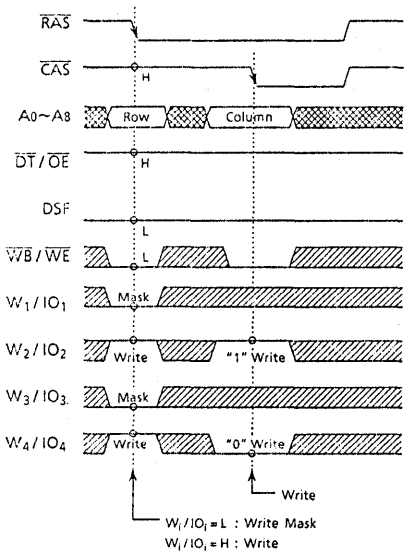


Figure 2. Write-per-bit timing cycle

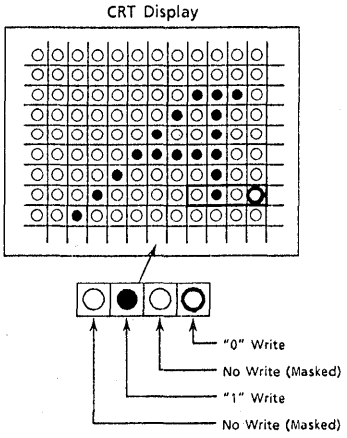


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER/READ COLOR REGISTER

The TC524258BJ/BZ is provided with an on-chip 4-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs last. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB}/\overline{WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ are satisfied. During the load/read color register cycle, valid A_0~A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

FLASH WRITE

Flash write is a special RAM port write operation which in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB}/\overline{WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (Refer to Figure 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycle and by specifying a different row address location during each flash write cycle (Refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2 μseconds.

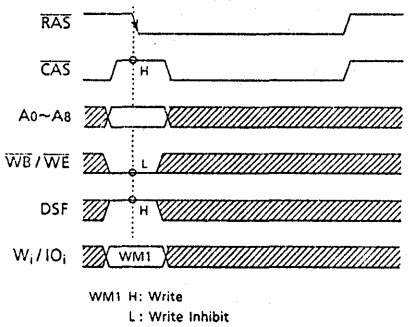


Figure 4. Flash Write Timing

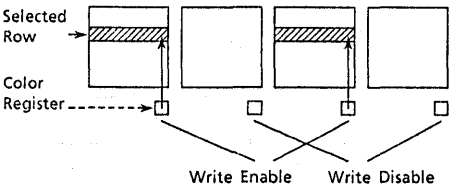


Figure 5. Flash Write

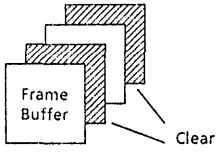


Figure 6. Plane clear application example

BLOCK WRITE

Block write is also a special RAM port write operation which, in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB}/\overline{WE}$ must be "low " to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the seven most significant column addresses (A2C~A8C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 7).

An example of the block write function is shown in Figure 8 with a data mask on W_1/IO_1, W_4/IO_4 and column 2. Block write is most effective for window clear and fill operation in frame buffer applications, as shown in the examples in Figure 9.

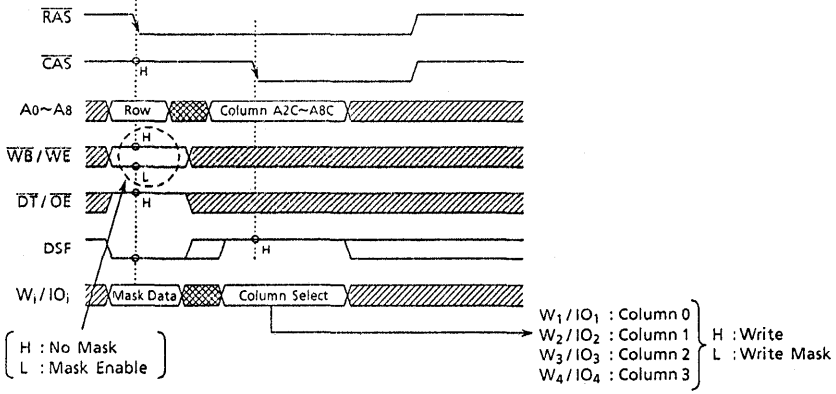


Figure 7. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1

	Column 0	Column 1	Column 2	Column 3	
W_1/IO_1					← Mask
W_2/IO_2	0	0		0	
W_3/IO_3	1	1		1	
W_4/IO_4					← Mask
			↑ Mask		

Figure 8. Example of Block Write Operation

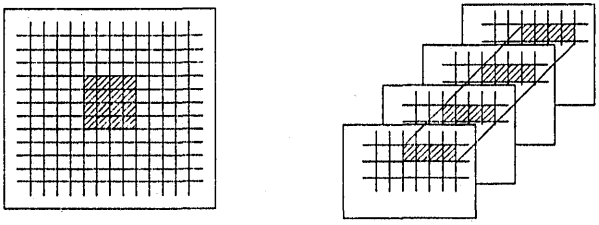


Figure 9. Examples of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read/write operation will occur. Therefore a combination of block write and read/write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

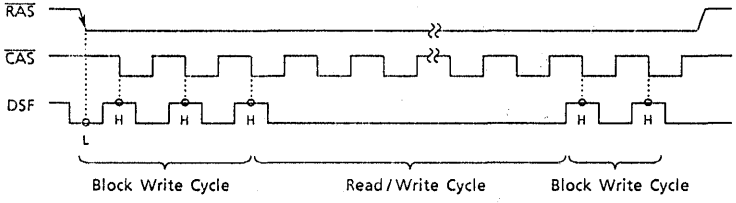


Figure 10. Fast Page Mode Block Write Cycle

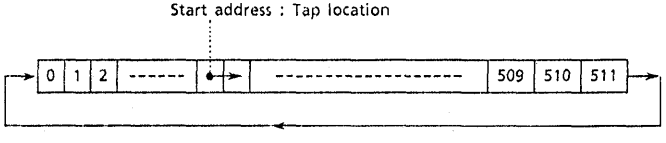
SAM PORT OPERATION

The TC524258BJ/BZ is provided with a 512 words by 4 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



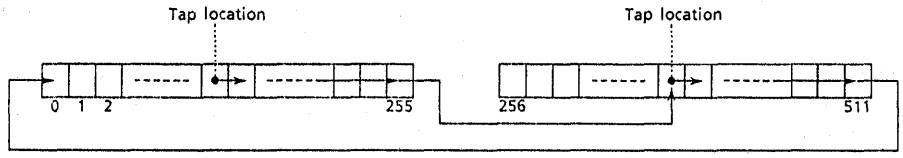
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

Table 4. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

SPLIT REGISTER MODE

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (Non-split) read / write / pseudo write transfer operation must precede any split read / write transfer operation. The non-split read, write and pseudo write transfer will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any at the 256 tap locations, excluding the last address of each split SAM, data is shifted in or out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data in or out sequentially starting from this tap location to the most significant bit (511 or 255) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC524258BJ/BZ features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal (Non-split) transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 256 words by 4 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal .

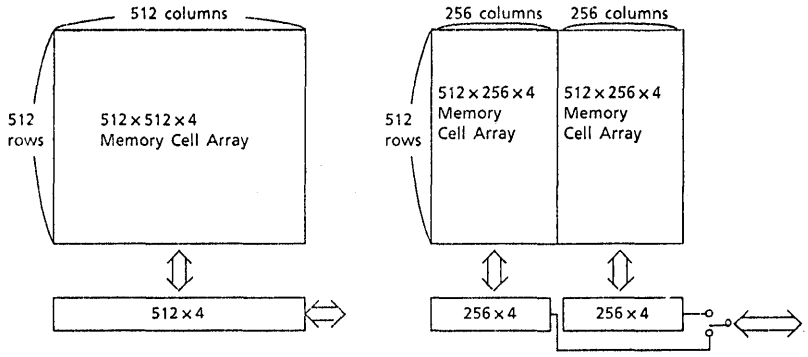


Figure 11. (a) Normal (Non-split) Transfer (b) Split Transfer

As shown in Table 5, the TC524258BJ/BZ supports five types of transfer operations: Read transfer, Split read transfer, Write transfer, Split write transfer and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/Pseudo write transfer) whereas it remains unchanged during split transfer operations (Split read or split write transfers). During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A8C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	512×4	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	512×4	Output → Input
H	L	L	H	L	Pseudo Write Transfer	-	-	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	256×4	Not changed
H	L	L	*	H	Split Write Transfer	SAM → RAM	256×4	Not changed

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for read transfer operation.

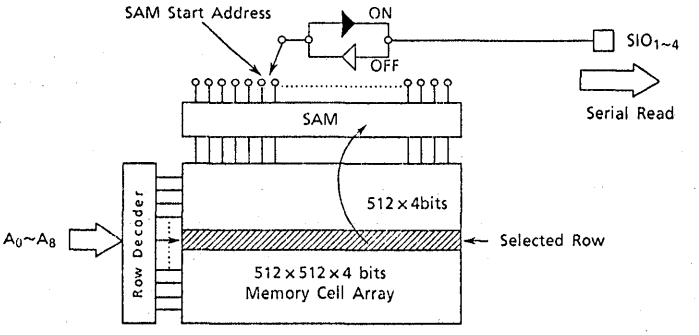


Figure 12. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 13.

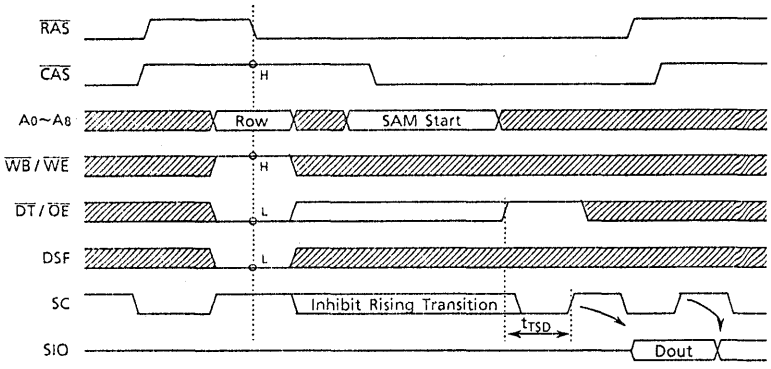


Figure 13. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

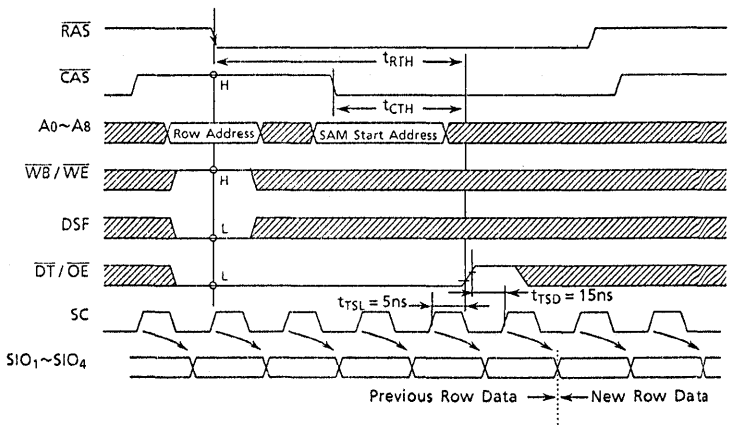


Figure 14. Real Time Read Transfer

WRITE TRANSFER CYCLE

A write transfer cycle consist of loading the content of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figure 15 and 16 show the timing diagram and block diagram for write transfer operations, respectively.

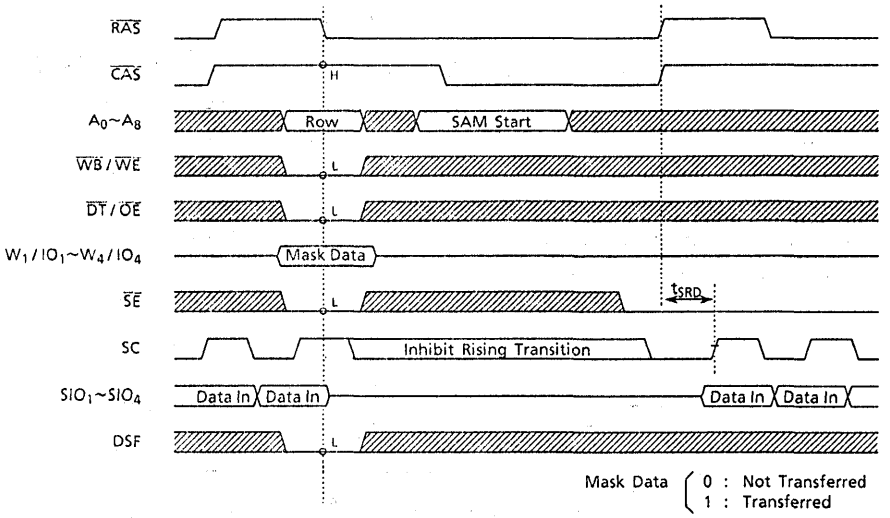


Figure 15. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

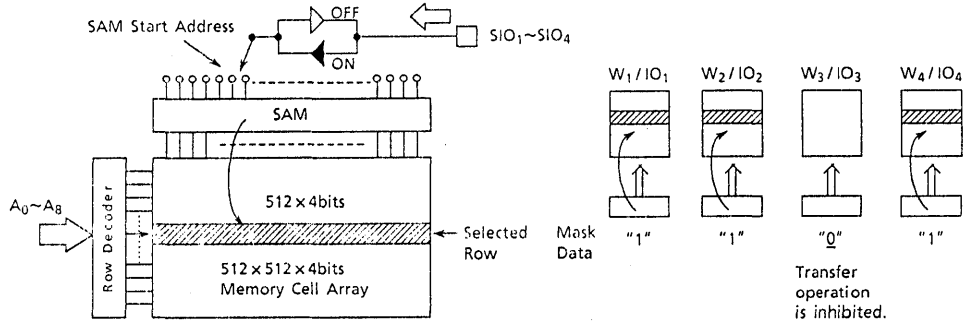


Figure 16. Block Diagram for Write Transfer Operation

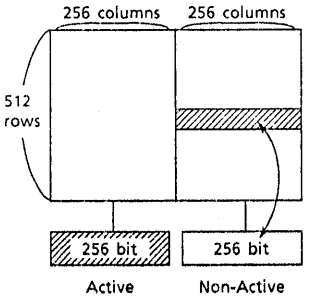
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

SPLIT DATA TRANSFER AND QSF

The TC524258BJ/BZ features a bi-directional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 18.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 17. Split Register Mode

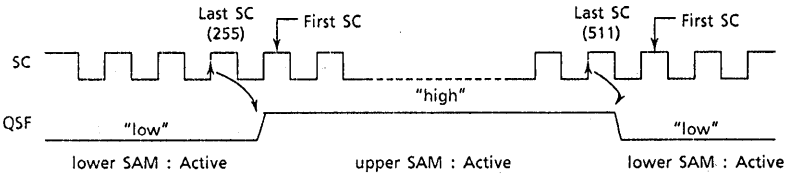


Figure 18. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading 256 words by 4 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

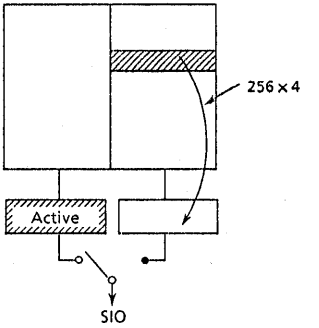


Figure 19. Block Diagram for Split Read Transfer

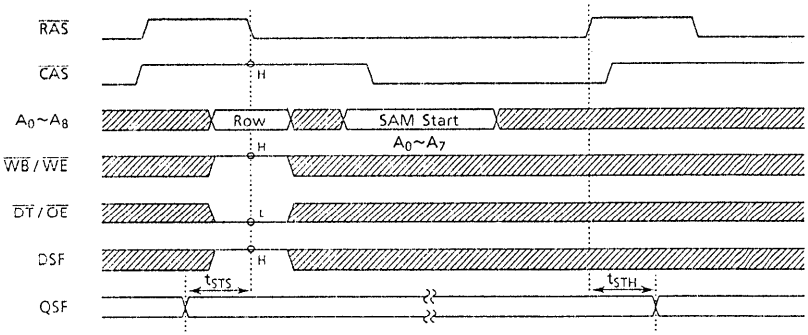


Figure 20. Timing Diagram for Split Read transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 21.

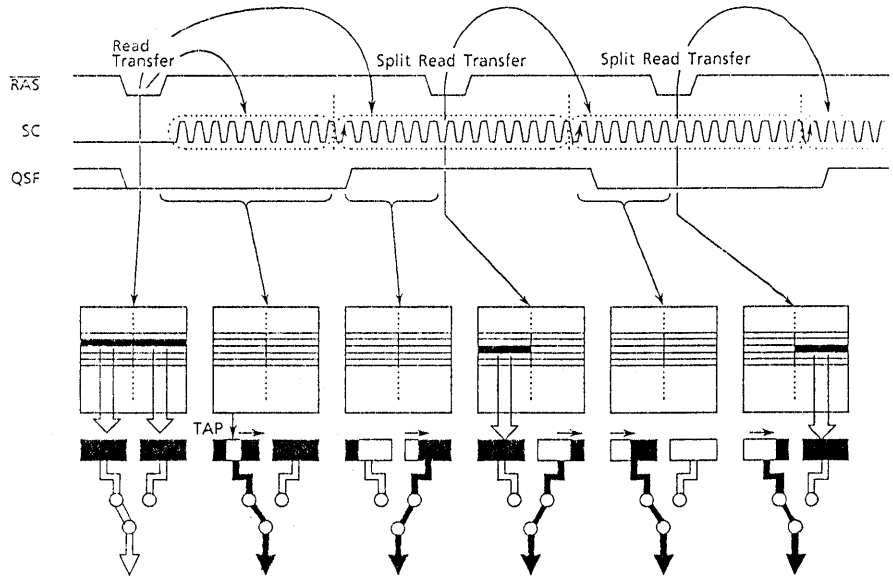


Figure 21. Example of Consecutive Read Transfer Operations

SPLIT WRITE TRANSFER CYCLE

A split write transfer consists of loading 256 words by 4 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figure 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

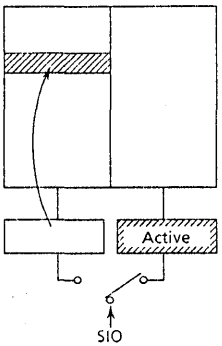


Figure 22. Block Diagram for Split Write Transfer

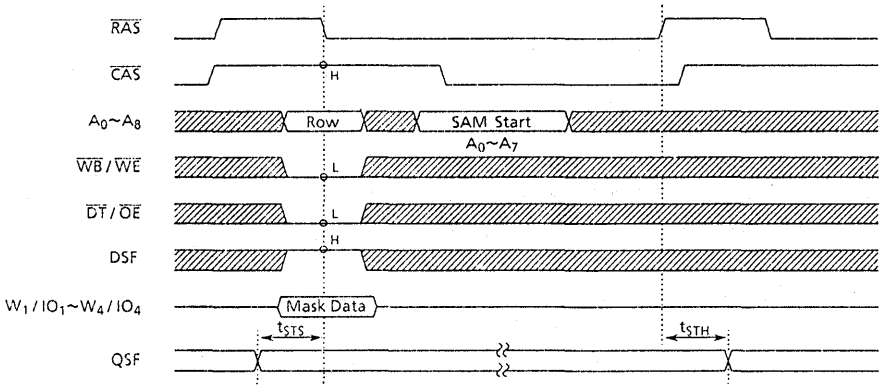


Figure 23. Timing Diagram for Split Write Transfer

A pseudo write transfer operation must precede split transfer cycles as shown in the example in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

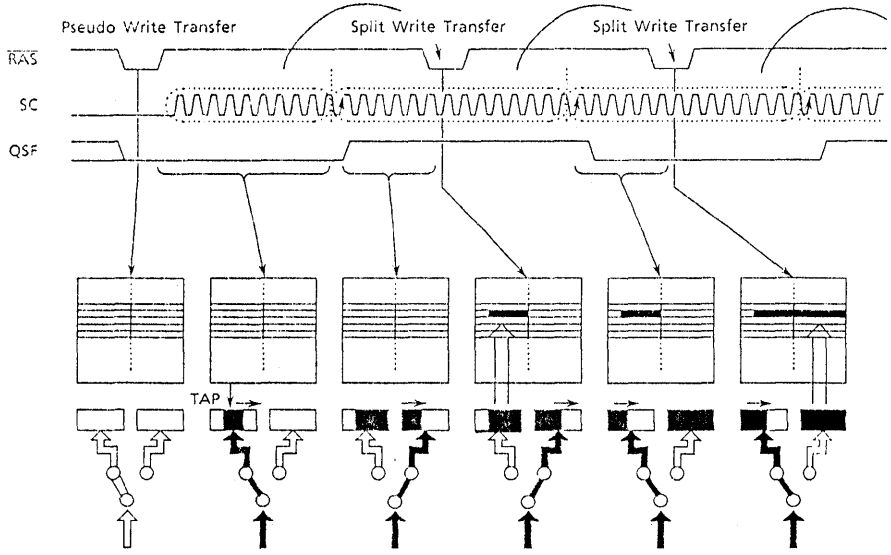


Figure 24. Example of Consecutive Write Transfer Operations

SPLIT-REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read/write transfers must be preceded by a normal (Non-split) transfer such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 256 in this example and the pointer is incremented from this location by cycling the SC clock.

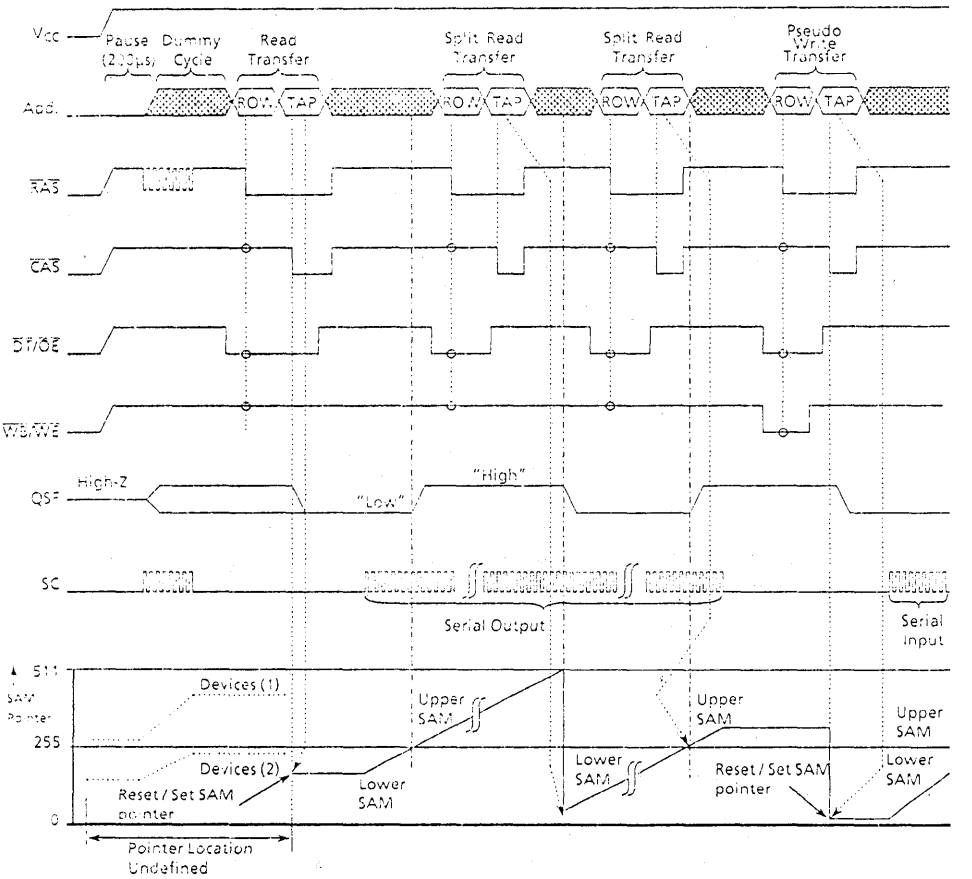
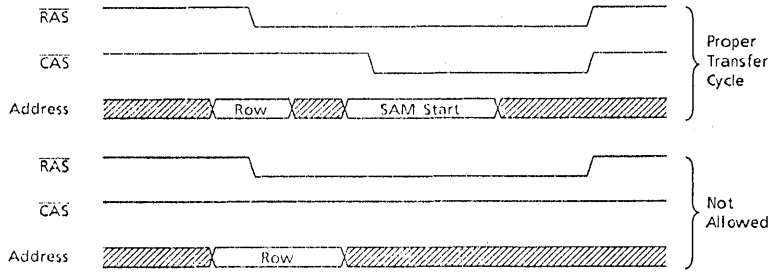


Figure 25. Example of Split SAM Register Operation Seguence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

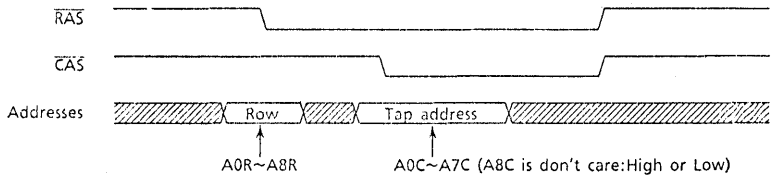
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



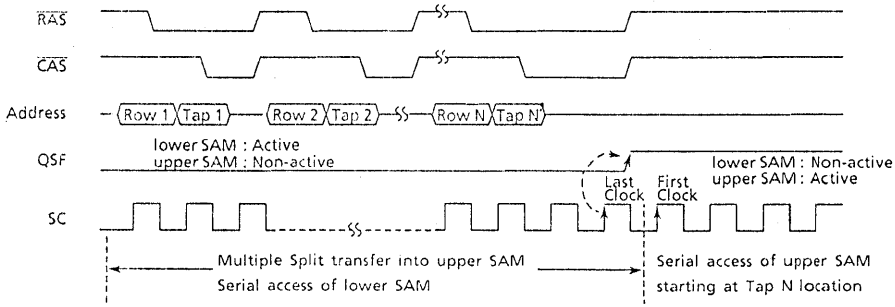
TAP LOCATION SELECTION IN SPLIT TRANSFER OPERATION

(a) In a split transfer operation, column addresses A0C through A7C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split transfer, column address A8C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A7C=FF), in either the lower SAM or the upper SAM, as the tap location.

(b) In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ / WRITE TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read / write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF.

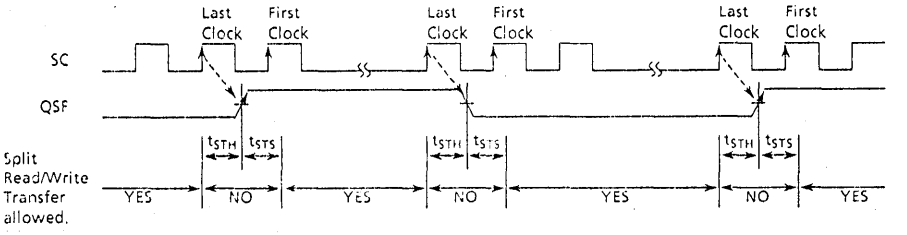
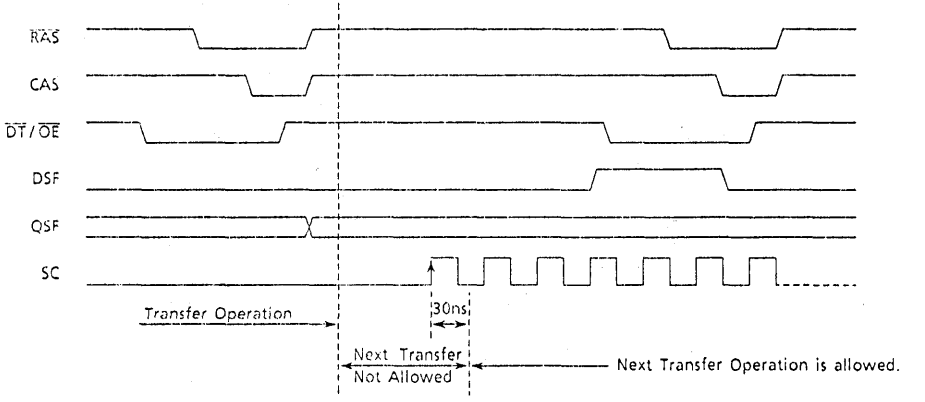


Figure 26. Split Transfer Operation Allowable Periods

As indicated in Figure 26, a split read / write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

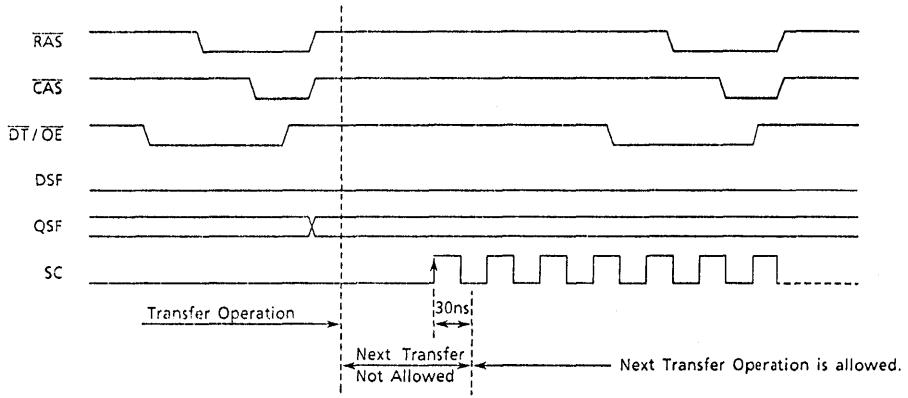
SPLIT TRANSFER CYCLE AFTER NORMAL TRANSFER CYCLE

A split transfer may be performed following a normal transfer (Read / Write / Pseudo-write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



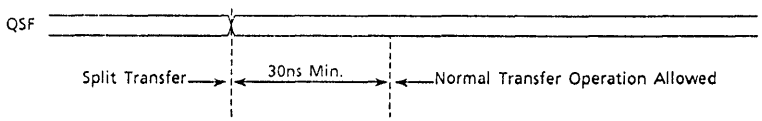
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT TRANSFER

A normal transfer (read/write/pseudo write) may be performed following split transfer operation provided that a 30ns minimun delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC524258BJ/BZ is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

262, 144WORDS×4BITS MULTIPORT DRAM

PRELIMINARY

DESCRIPTION

The TC524259BJ/BZ is a CMOS multiport memory equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The TC524259BJ/BZ supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. In addition to the conventional multiport video RAM operating modes, the TC524259BJ/BZ features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port. The TC524259BJ/BZ is fabricated using Toshiba's CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

FEATURES

ITEM		TC524259BJ/BZ	
		-80	-10
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	80ns	100ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	25ns	25ns
t_{AA}	Column Address Access Time (Max.)	45ns	50ns
t_{RC}	Cycle Time (Min.)	150ns	180ns
t_{PC}	Page Mode Cycle Time (Min.)	50ns	55ns
t_{SCA}	Serial Access Time (Max.)	25ns	25ns
t_{SCC}	Serial Cycle time (Min.)	30ns	30ns
I_{CC1}	RAM Operating Current (SAM : Standby)	85mA	70mA
I_{CC2A}	SAM Operating Current (RAM : Standby)	50mA	50mA
I_{CC2}	Standby Current	10mA	10mA

- Single power supply of 5V±10% with a built-in V_{BB} generator
- All inputs and outputs : TTL Compatible

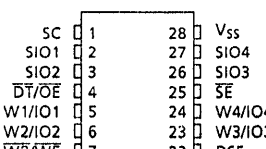
- Organization
  - RAM Port : 262,144words×4bits
  - SAM Port : 512words×4bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh
  - $\overline{RAS}$ only Refresh, Write per Bit 1&2
  - Block Write, Block Write (Mask 1&2)
  - 512 refresh cycles/8ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read Transfer
- Package
  - TC524259BJ : SOJ28-P-400
  - TC524259BZ : ZIP28-P-400

PIN NAME

A0~A8	Address inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}$/$\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}$/$\overline{WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1~W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1~SIO4	Serial Input/Output
QSF	Special Flag Output
V_{CC}/V_{SS}	Power (5V)/Ground
N.C.	No Connection

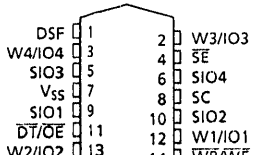
PIN CONNECTION

TC524259BJ



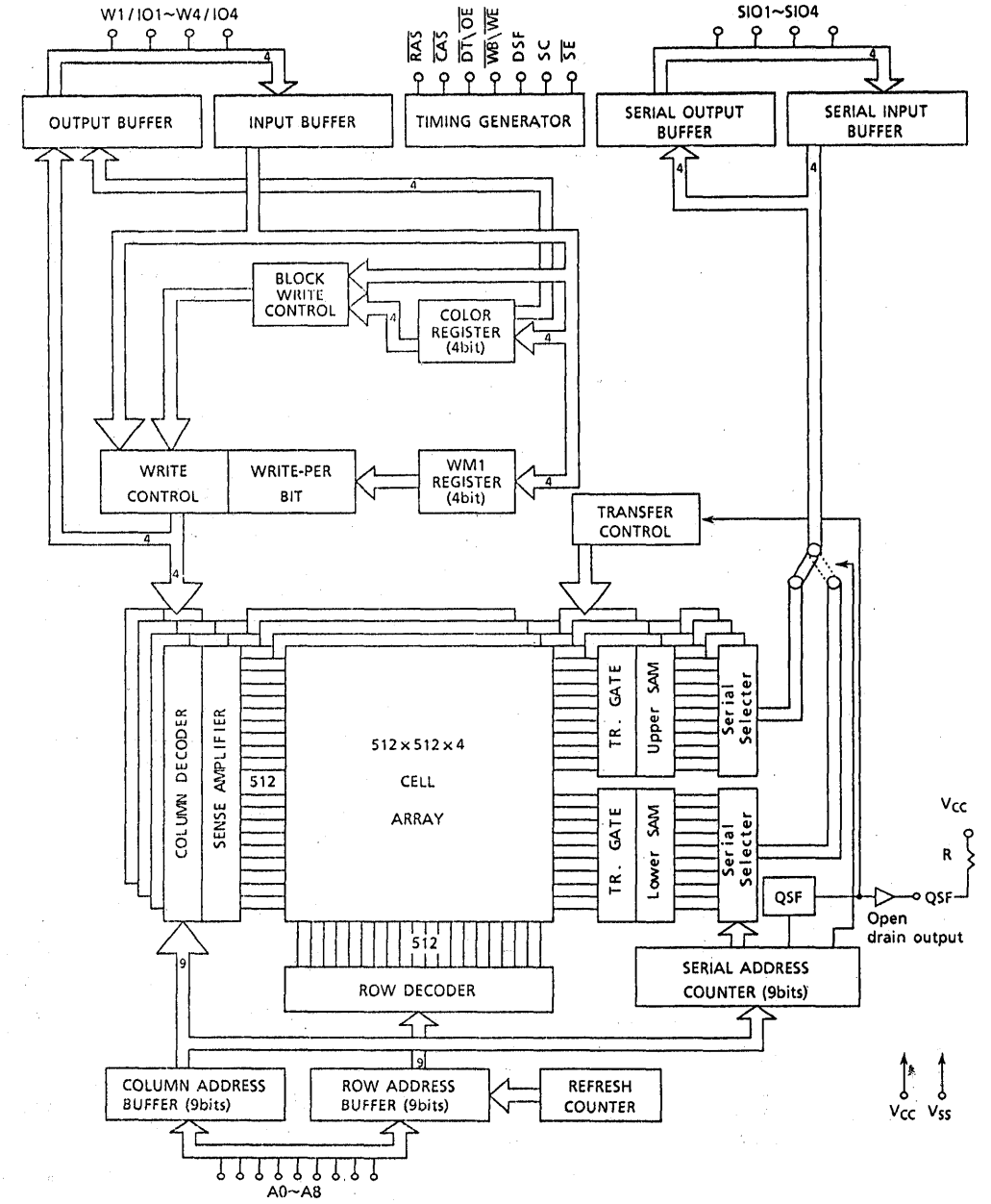
28Pin 400mil SOJ
JEDEC Standard

TC524259BZ



28Pin 400mil height ZIP
JEDEC Standard

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT	NOTE
V_{IN}, V_{OUT}	Input Output Voltage	−1.0~7.0	V	1
V_{CC}	Power Supply Voltage	−1.0~7.0	V	1
T_{OPR}	Operating Temperature	0~70	°C	1
T_{STG}	Storage Temperature	−55~150	°C	1
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED D.C. OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	2
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	2

CAPACITANCE (V_{CC} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_I	Input Capacitance	−	7	pF
C_{IO}	Input / Output Capacitance	−	9	
C_O	Output Capacitance (QSF)	−	9	

Note : This parameter is periodically sampled and is not 100% tested.

D.C. ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, Ta = 0~70°C)

ITEM (RAM PORT)	SAM PORT	SYMBOL	TC524259BJ/BZ-80		TC524259BJ/BZ-10		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.		
OPERATING CURRENT $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.	Standby	I_{CC1}	–	85	–	70	mA	3, 4
	Active	I_{CC1A}	–	125	–	110		3, 4
STANDBY CURRENT ($\overline{RAS}$, $\overline{CAS} = V_{IH}$)	Standby	I_{CC2}	–	10	–	10		
	Active	I_{CC2A}	–	50	–	50		3, 4
$\overline{RAS}$ ONLY REFRESH CURRENT $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$ $t_{RC} = t_{RC}$ min.	Standby	I_{CC3}	–	85	–	70		3, 4
	Active	I_{CC3A}	–	125	–	110		3, 4
PAGE MODE CURRENT $\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling $t_{PC} = t_{PC}$ min.	Standby	I_{CC4}	–	75	–	60		3, 4
	Active	I_{CC4A}	–	115	–	100		3, 4
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT $\overline{RAS}$ Cycling, $\overline{CAS}$ Before $\overline{RAS}$ $t_{RC} = t_{RC}$ min.	Standby	I_{CC5}	–	85	–	70		3, 4
	Active	I_{CC5A}	–	125	–	110		3, 4
DATA TRANSFER CURRENT $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.	Standby	I_{CC6}	–	105	–	90		3, 4
	Active	I_{CC6A}	–	145	–	130		3, 4
BLOCK WRITE CURRENT $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC}$ min.	Standby	I_{CC8}	–	95	–	80		3, 4
	Active	I_{CC8A}	–	135	–	120		3, 4

ITEM	SYMBOL	MIN.	MAX.	UNIT	NOTE
INPUT LEAKAGE CURRENT $0V \leqq V_{IN} \leqq 6.5V$, All other pins not under test = 0V	$I_{I(L)}$	– 10	10	μA	
OUTPUT LEAKAGE CURRENT $0V \leqq V_{OUT} \leqq 5.5V$, Output Disable	$I_{O(L)}$	– 10	10	μA	
OUTPUT "H" LEVEL VOLTAGE $I_{OUT} = -2mA$	V_{OH}	2.4	–	V	
OUTPUT "L" LEVEL VOLTAGE $I_{OUT} = 2mA$	V_{OL}	–	0.4	V	
OUTPUT "L" LEVEL VOLTAGE (QSF) $I_{OUT} = 6mA$	V_{OL} (QSF)	–	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED A.C. OPERATING CONDITIONS

(V_{CC} = 5V ± 10%, Ta = 0~70°C) (Notes : 5, 6, 7)

SYMBOL	PARAMETER	TC524259BJ/BZ-80		TC524259BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		235			
t_{PC}	Fast Page Mode Cycle Time	50		55			
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		100			
t_{RAC}	Access Time from $\overline{RAS}$		80		100		8,14
t_{AA}	Access Time from Column Address		45		50		8,14
t_{CAC}	Access Time from $\overline{CAS}$		25		25		8,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		8,15
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20		10
t_T	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	60		70			
t_{RAS}	$\overline{RAS}$ Pulse Width	80	10000	100	10000		
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode Only)	80	100000	100	100000		
t_{RSH}	$\overline{RAS}$ Hold Time	25		25			
t_{CSH}	$\overline{CAS}$ Hold Time	80		100			
t_{CAS}	$\overline{CAS}$ Pulse Width	25	10000	25	10000		
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	55	20	75		14
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	50		14
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	45		50			
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10			
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		10			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	15		15			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		70			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0			11
t_{WCH}	Write Command Hold Time	15		15			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		70			
t_{WP}	Write Command Pulse Width	15		15			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25			

SYMBOL	PARAMETER	TC524259BJ/BZ-80		TC524259BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{DS}	Data Set-Up Time	0		0		ns	12
t_{DH}	Data Hold Time	15		15			12
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		70			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		130			13
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		80			13
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		55			13
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{OE}$		20		25		8
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	10	0	20		10
t_{OED}	$\overline{OE}$ to Data Delay Time	10		20			
t_{OEH}	$\overline{OE}$ Command Hold Time	10		20			
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15			
t_{CSR}	$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Cycle	10		10			
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{WB}$ Set-Up Time	0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15			
t_{FSR}	DSF Set-UP Time referenced to $\overline{RAS}$	0		0			
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15			
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	55		70			
t_{FSC}	DSF Set-Up Time referenced to $\overline{CAS}$	0		0			
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15			
t_{THS}	$\overline{DT}$ High Set-Up Time	0		0			
t_{THH}	$\overline{DT}$ High Hold Time	15		15			
t_{TLS}	$\overline{DT}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10000	15	10000		
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	65	10000	80	10000		
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	30		30			
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	25		25			

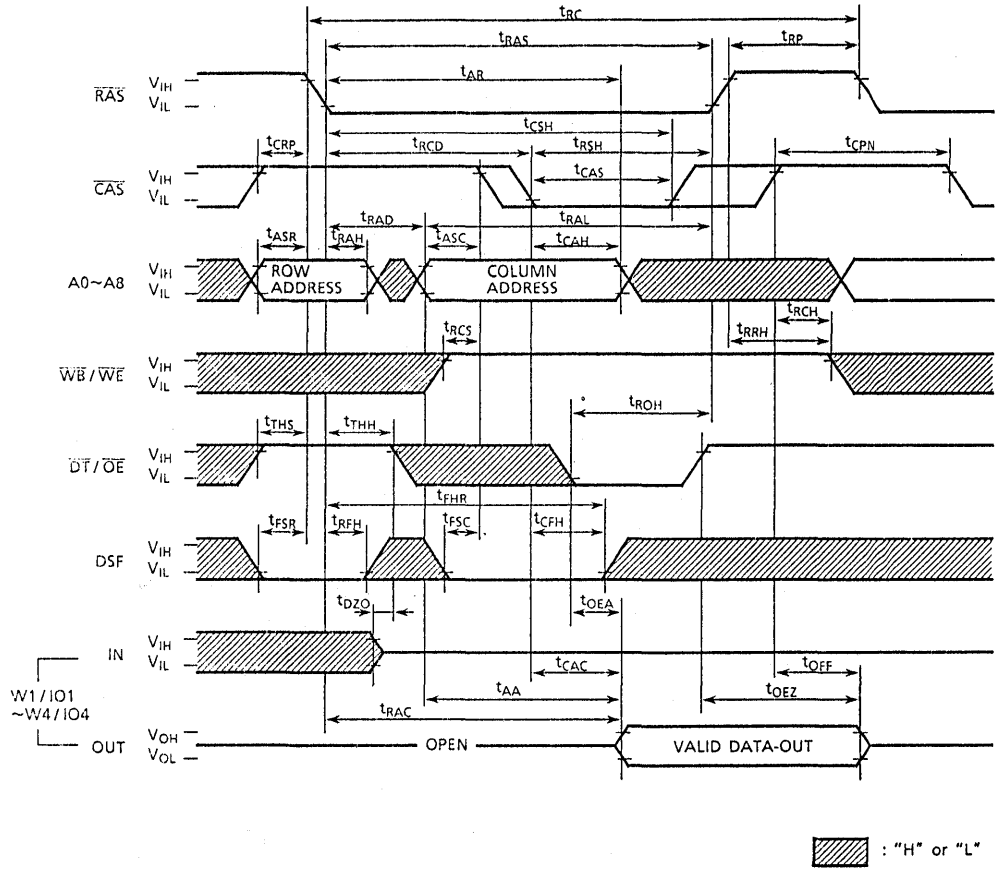
SYMBOL	PARAMETER	TC524259BJ/BZ-80		TC524259BJ/BZ-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
t_{ESR}	$\overline{SE}$ Set-Up Time referenced to $\overline{RAS}$	0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15			
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		70			
t_{TP}	$\overline{DT}$ Precharge Time	20		30			
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	80		100			
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		50			
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	25		25			
t_{ISL}	Last SC to $\overline{DT}$ Load Time (Real Time Read Transfer)	5		5			
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		30			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		25			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		50			
t_{SDZ}	Serial Output Buffer Turn-off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	50		10
t_{SCC}	SC Cycle Time	30		30			
t_{SC}	SC Pulse Width (SC High Time)	10		10			
t_{SCP}	SC Precharge Time (SC Low Time)	10		10			
t_{SCA}	Access Time from SC		25		25		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	15		15			
t_{SEA}	Access Time from $\overline{SE}$		25		25		9
t_{SE}	$\overline{SE}$ Pulse Width	25		25			
t_{SEP}	$\overline{SE}$ Precharge Time	25		25			
t_{SEZ}	Serial Output Buffer Turn-off Delay from $\overline{SE}$	0	20	0	20		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	0		0			
t_{SWH}	Serial Write Enable Hold Time	15		15			
t_{SWIS}	Serial Write Disable Set-Up Time	0		0			
t_{SWIH}	Serial Write Disable Hold Time	15		15			
t_{STS}	Split Transfer Set-Up Time	30		30			
t_{STH}	Split Transfer Hold Time	30		30			
t_{SQD}	SC-QSF Delay Time		60		60		16

NOTES :

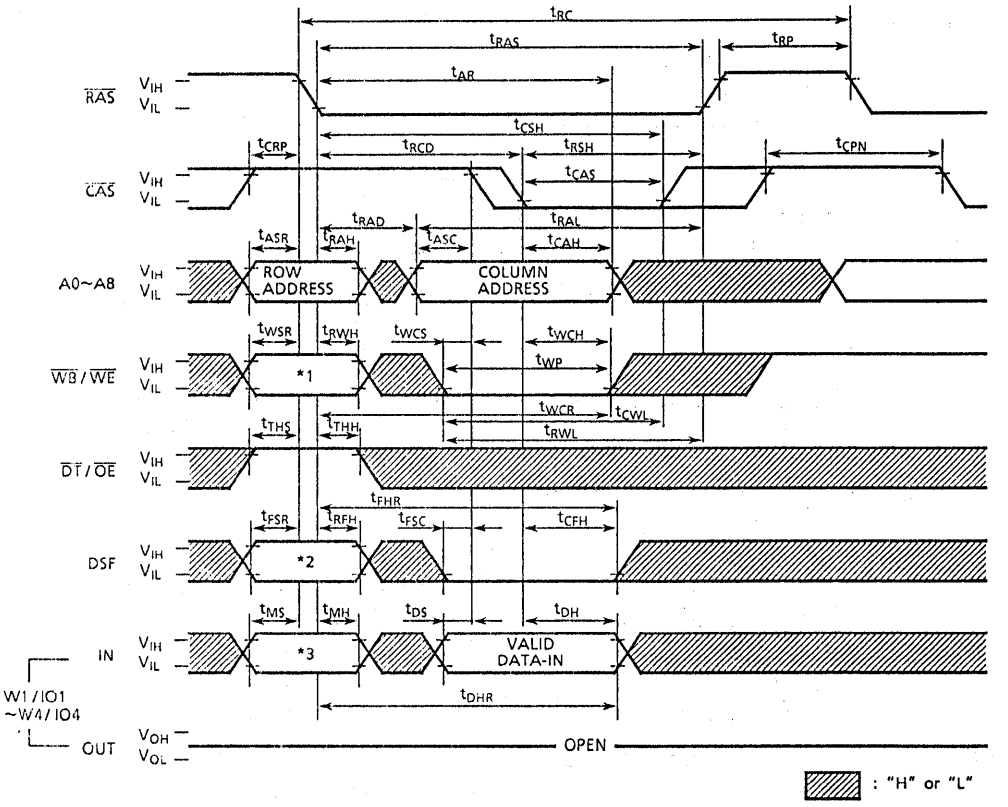
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltage are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}$/$\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
6. AC measurements assume t_T=5ns.
7. $V_{IH\,(min.)}$ and $V_{IL\,(max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 1 TTL load and 100pF. D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
9. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF. D_{OUT} reference levels : V_{OH}/V_{OL}=2.0V/0.8V.
10. $t_{OFF\,(max.)}$, $t_{OEZ\,(max.)}$, $t_{SDZ\,(max.)}$ and $t_{SEZ\,(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}$/$\overline{WE}$ leading edge in $\overline{OE}$-controlled-write cycles and read-modify-write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS\,(min.)}$, the cycle is an early write cycles and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{RWD} \geqq t_{RWD\,(min.)}$, $t_{CWD} \geqq t_{CWD\,(min.)}$ and $t_{AWD} \geqq t_{AWD\,(min.)}$ the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the $t_{RCD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RCD\,(max.)}$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{RCD\,(max.)}$ limit, then access time is controlled by t_{CAC}.
15. Operation within the $t_{RAD\,(max.)}$ limit insures that $t_{RAC\,(max.)}$ can be met. $t_{RAD\,(max.)}$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD\,(max.)}$ limit, then access time is controlled by t_{AA}.
16. This parameter measurement assumes Pull up resister = 820Ω.

TIMING WAVEFORM

READ CYCLE



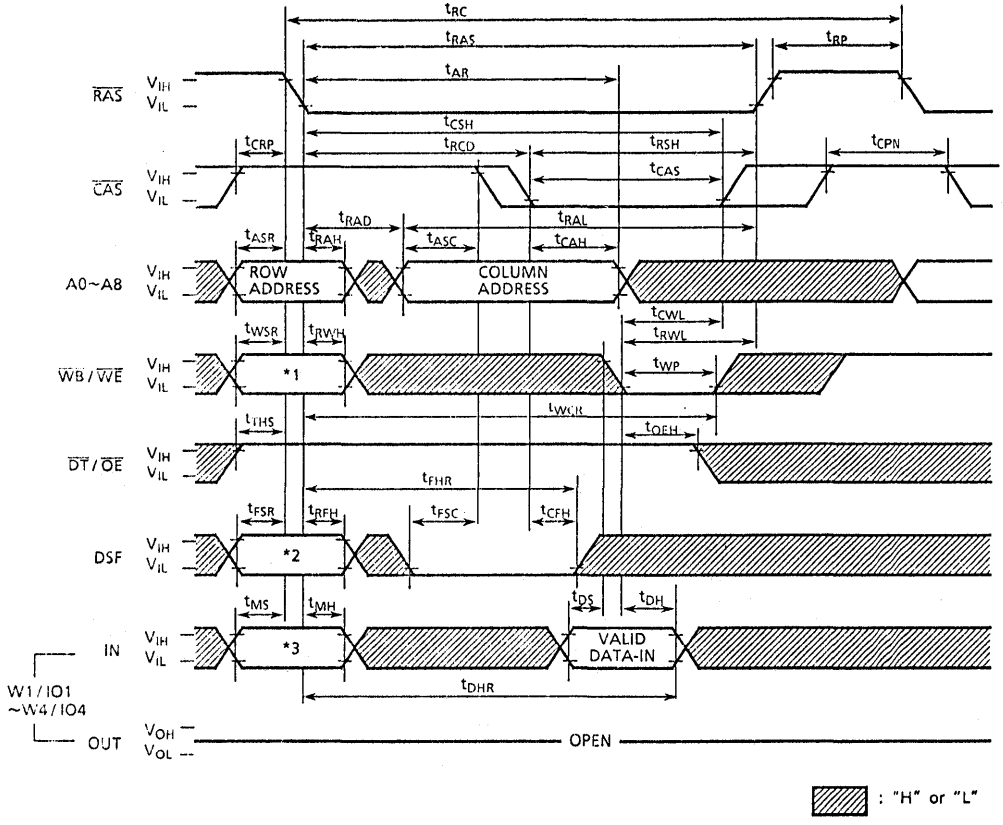
WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data : 0 : Write Disable
1 : Write Enable

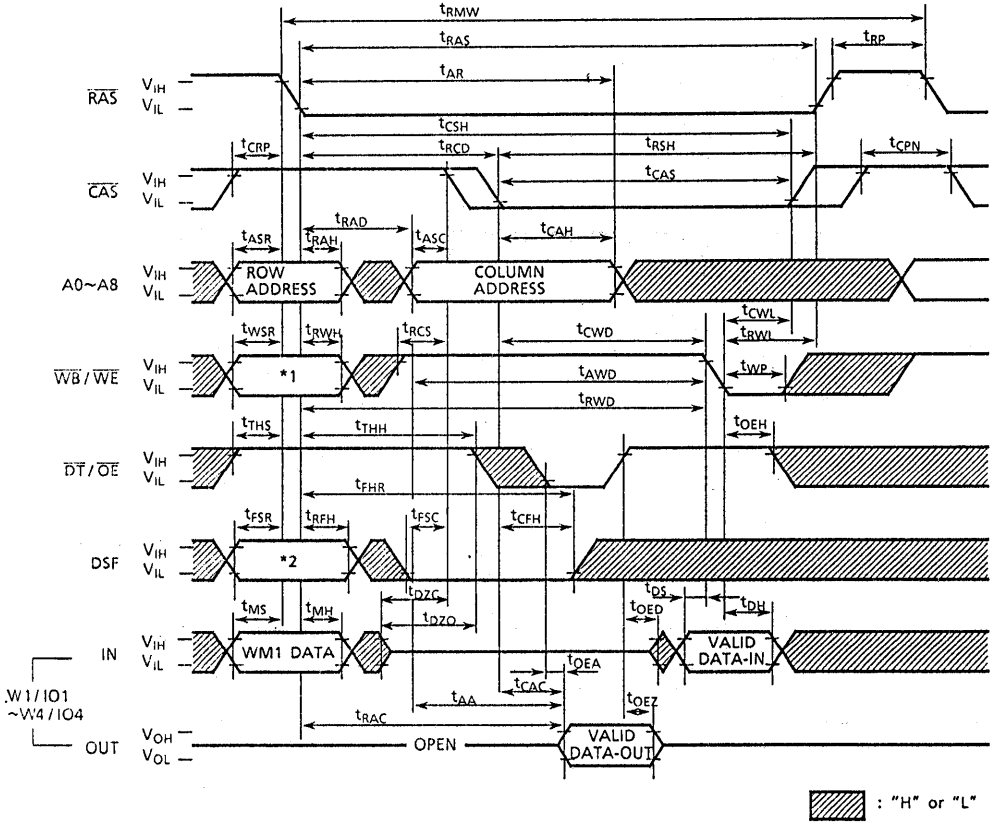
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data : 0 : Write Disable
1 : Write Enable

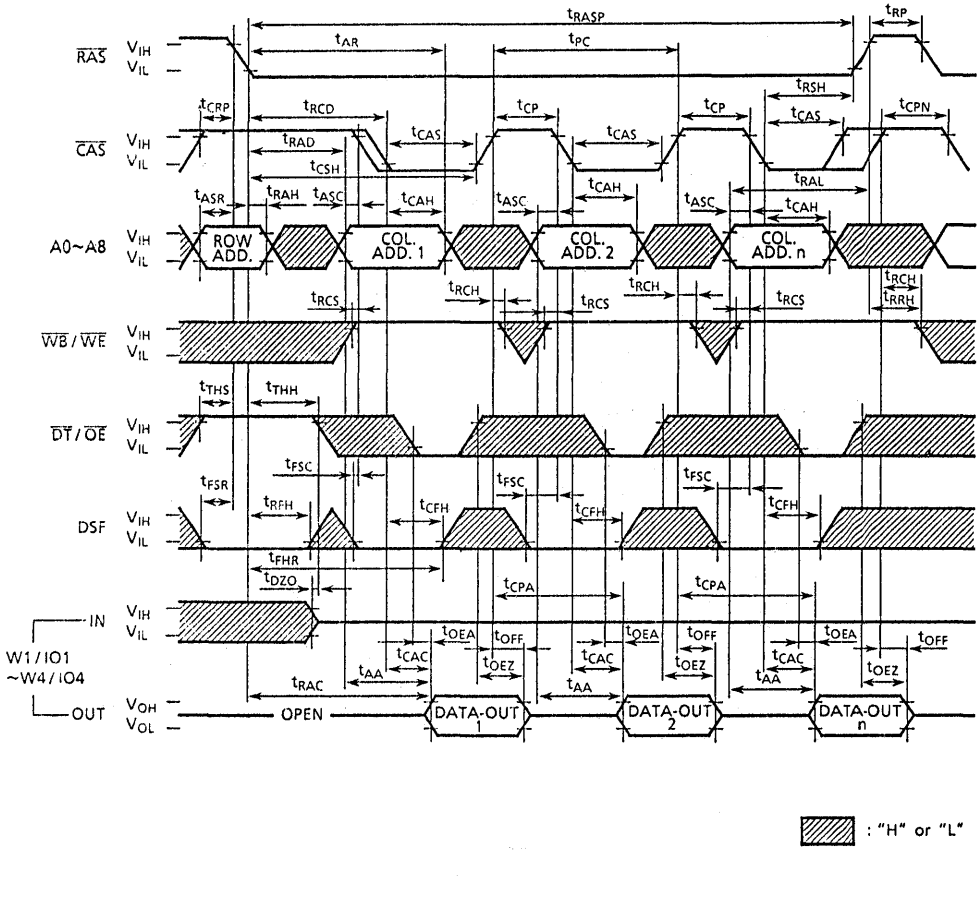
READ - MODIFY - WRITE CYCLE



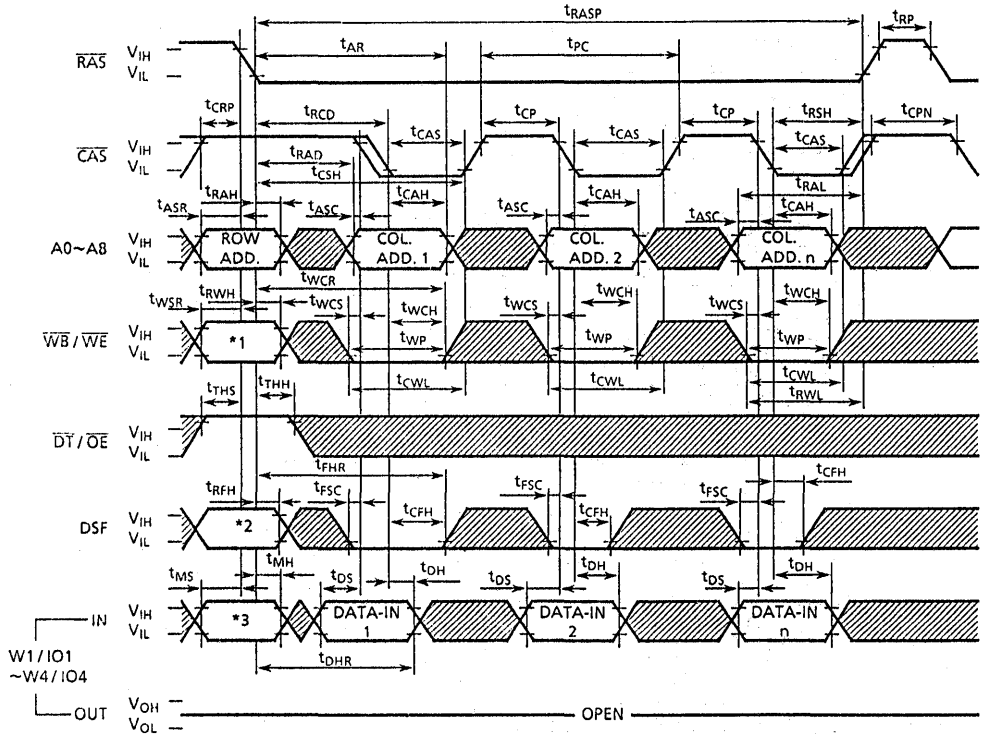
*1 $\overline{WB}$ / $\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data : 0 : Write Disable
1 : Write Enable

FAST PAGE MODE READ CYCLE



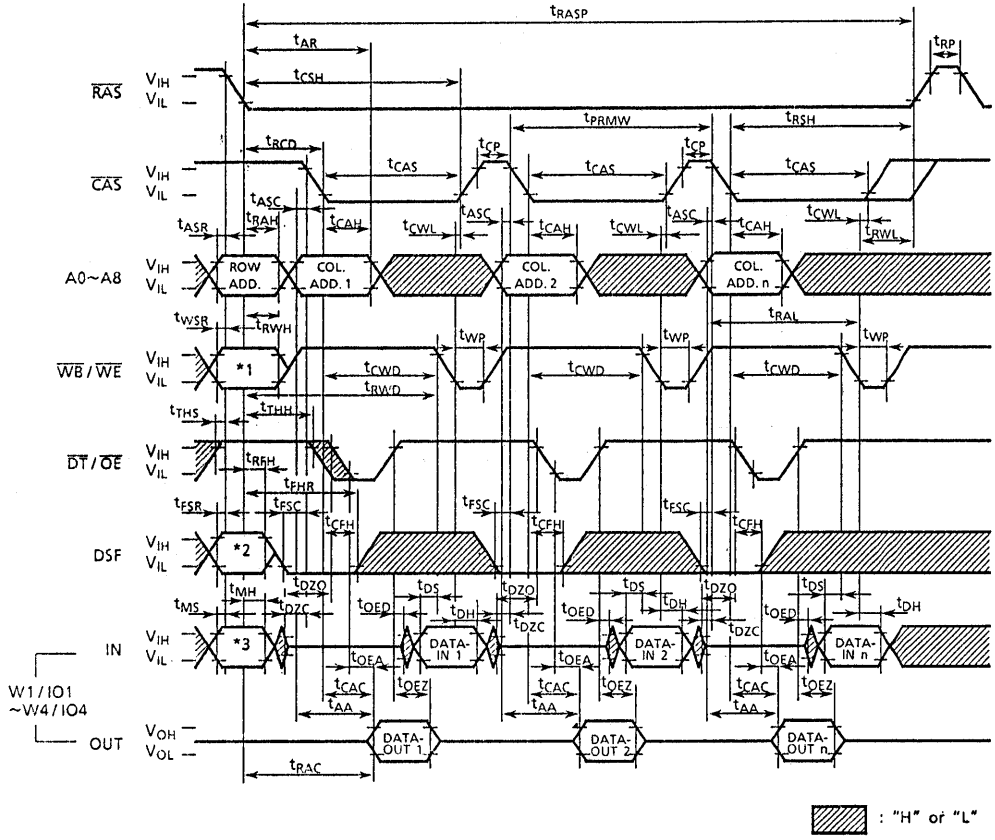
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



*1 $\overline{WB}$ / $\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data : 0 : Write Disable
1 : Write Enable

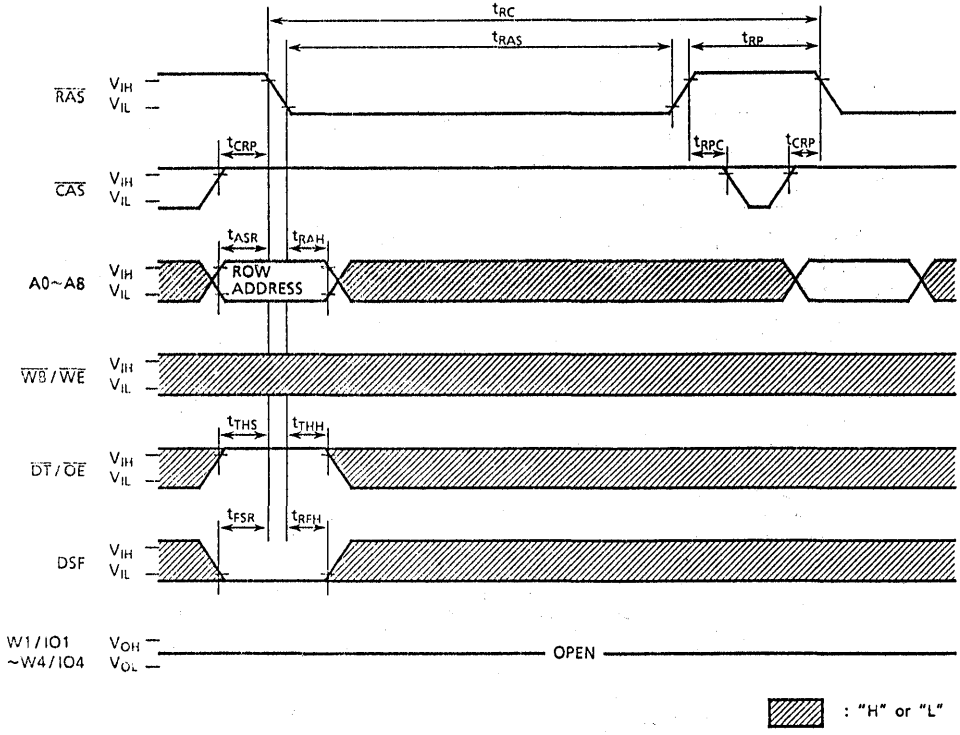
FAST PAGE MODE READ - MODIFY - WRITE CYCLE



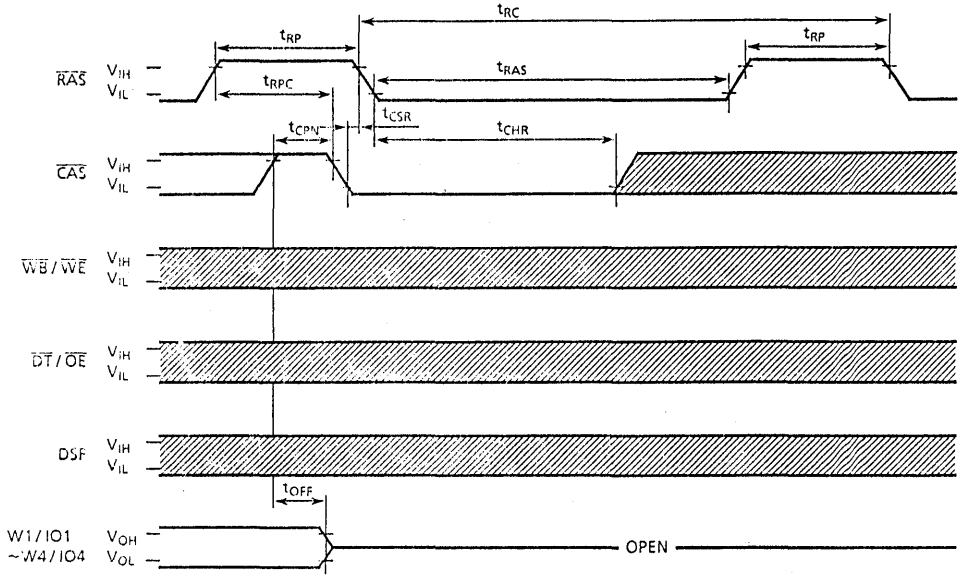
*1 $\overline{WB}$ / $\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Write per bit 1 (New Mask Mode)
	1	Don't Care	Write per bit 2 (Old Mask Mode)
1	0	Don't Care	Normal Write (No Mask Mode)

WM1 data : 0 : Write Disable
1 : Write Enable

$\overline{RAS}$ ONLY REFRESH CYCLE



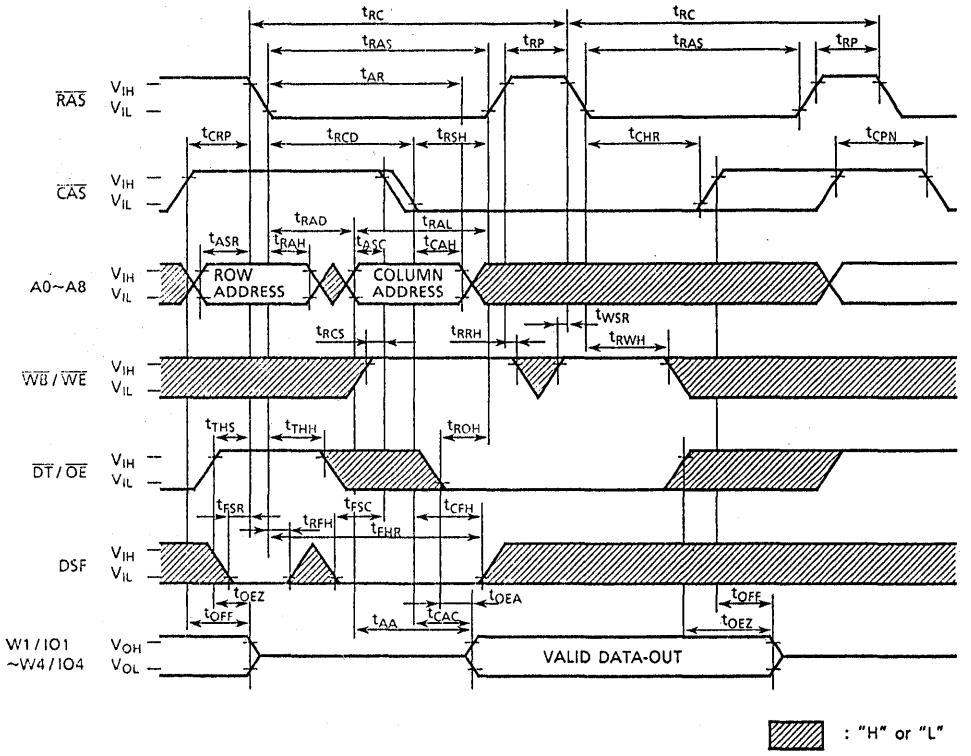
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



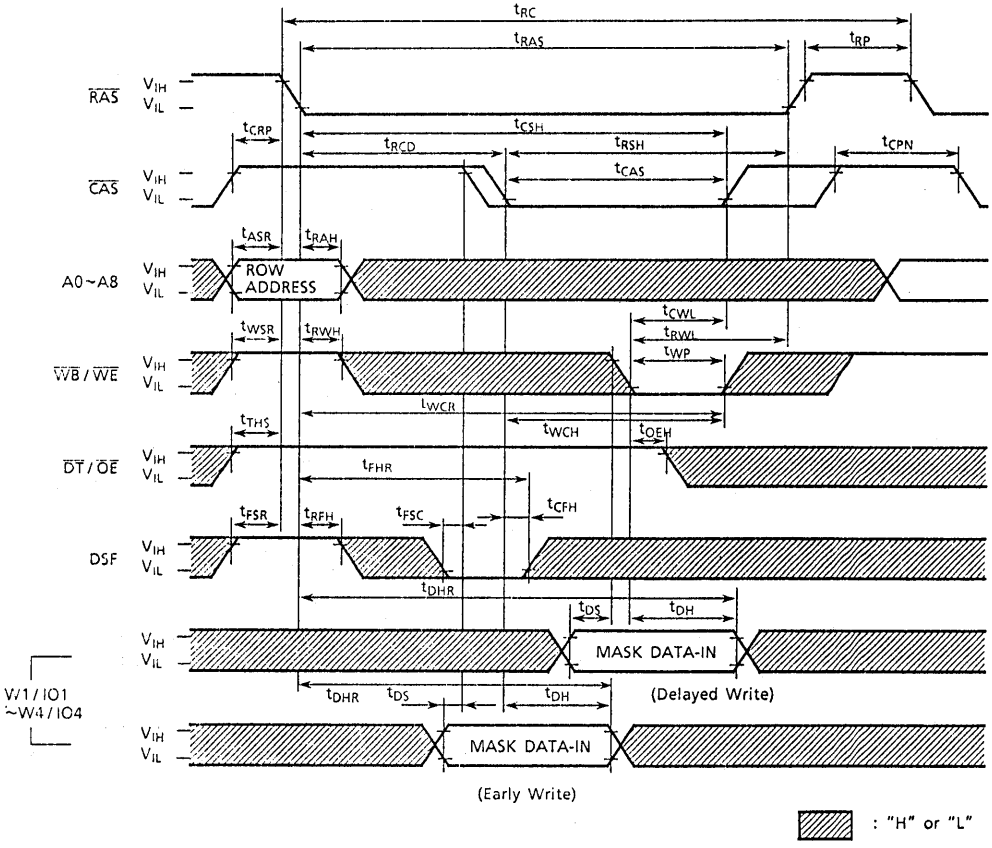
Note : A0 – A8 = Don't Care ("H" or "L")

: "H" or "L"

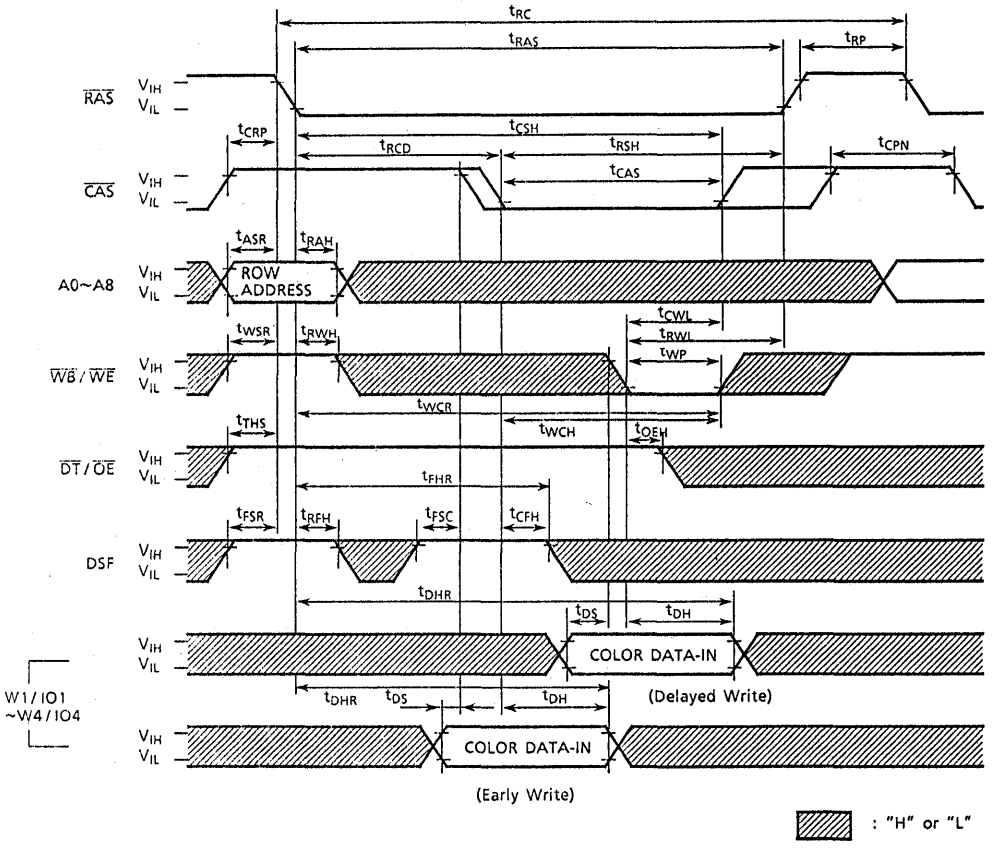
HIDDEN REFRESH CYCLE



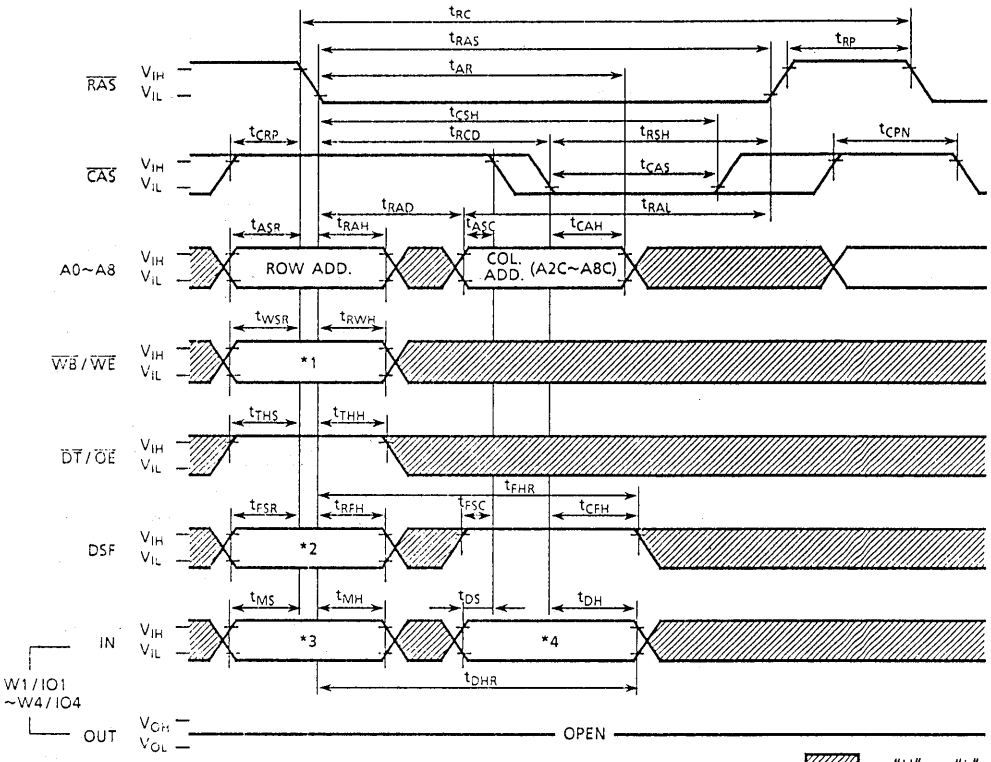
LOAD MASK REGISTER CYCLE



LOAD COLOR REGISTER CYCLE



BLOCK WRITE CYCLE



*1 $\overline{WB}/\overline{WE}$	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Block Write (Mask 1) (New Mask Mode)
	1	Don't Care	Block Write (Mask 2) (Old Mask Mode)
1	0	Don't Care	Block Write (No Mask Mode)

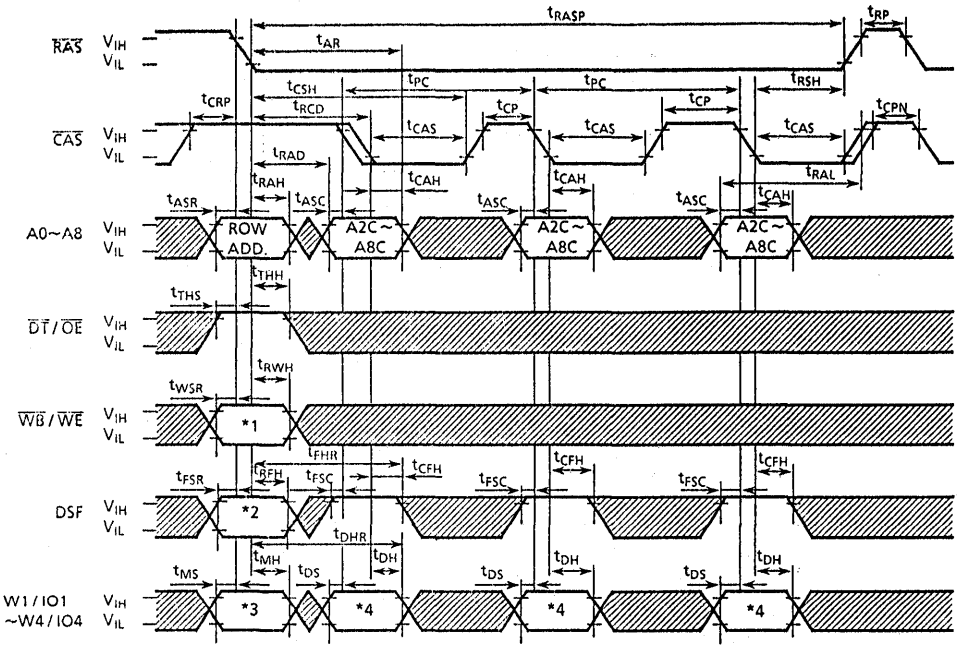
WM1 data : 0 : Write Disable
1 : Write Enable

*4) COLUMN SELECT

W1/IO1 — Column 0 (A1C = 0, A0C = 0)
W2/IO2 — Column 1 (A1C = 0, A0C = 1)
W3/IO3 — Column 2 (A1C = 1, A0C = 0)
W4/IO4 — Column 3 (A1C = 1, A0C = 1)

} Wn/IOn
= 0 : Disable
= 1 : Enable

PAGE MODE BLOCK WRITE CYCLE



*1 WB/WE	*2 DSF	*3 W1/IO1 ~ W4/IO4	Cycle
0	0	WM1 data	Block Write (Mask 1) (New Mask Mode)
	1	Don't Care	Block Write (Mask 2) (Old Mask Mode)
1	0	Don't Care	Block Write (No Mask Mode)

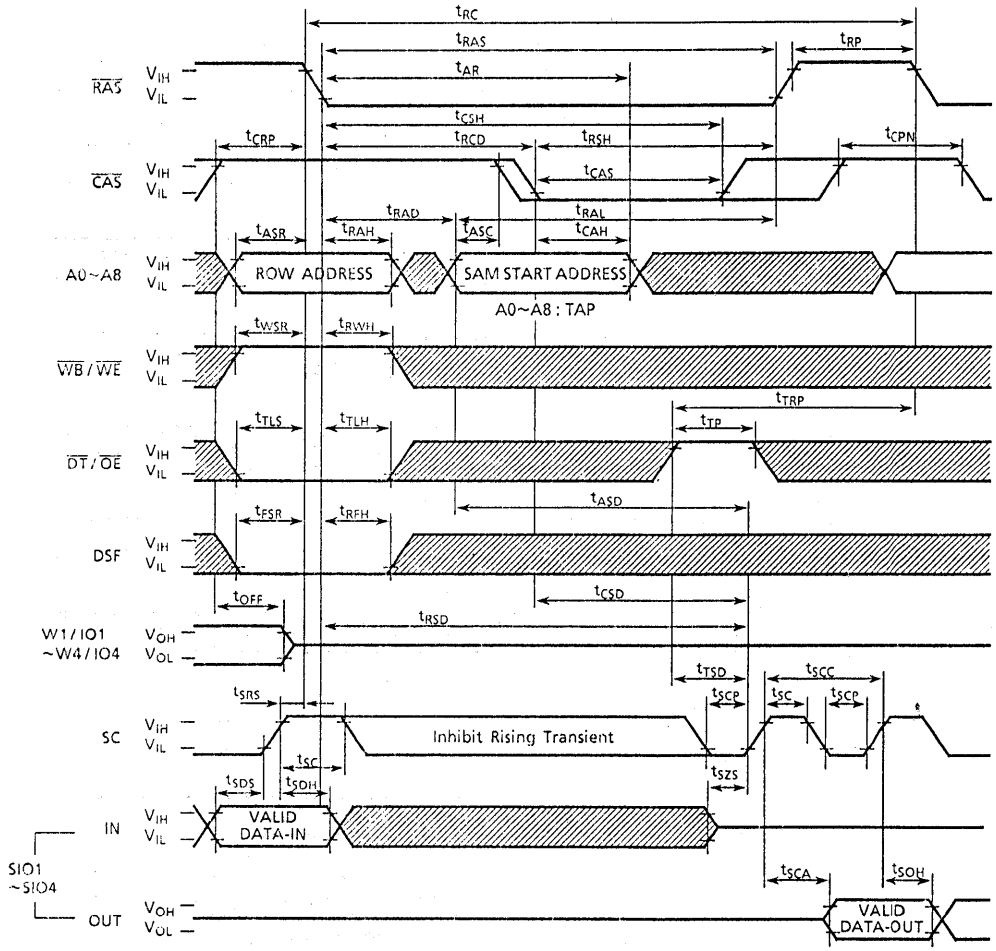
WM1 data : 0 : Write Disable
1 : Write Enable

*4) COLUMN SELECT

W1/IO1 – Column 0 (A1C = 0, A0C = 0)
W2/IO2 – Column 1 (A1C = 0, A0C = 1)
W3/IO3 – Column 2 (A1C = 1, A0C = 0)
W4/IO4 – Column 3 (A1C = 1, A0C = 1)

} Wn/IOn
= 0 : Disable
= 1 : Enable

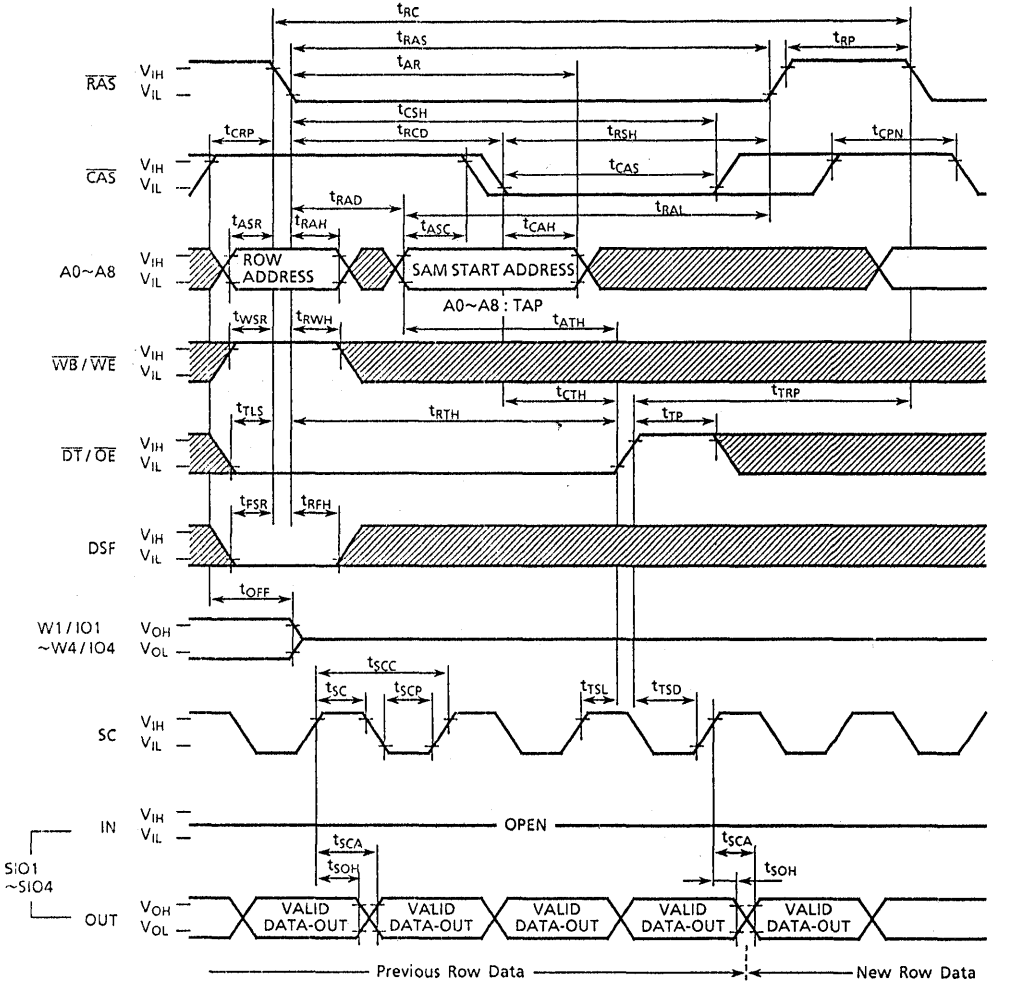
READ TRANSFER CYCLE (Previous Transfer is WRITE TRANSFER CYCLE)



Note : $\overline{SE}$ = V_{IL}

: "H" or "L"

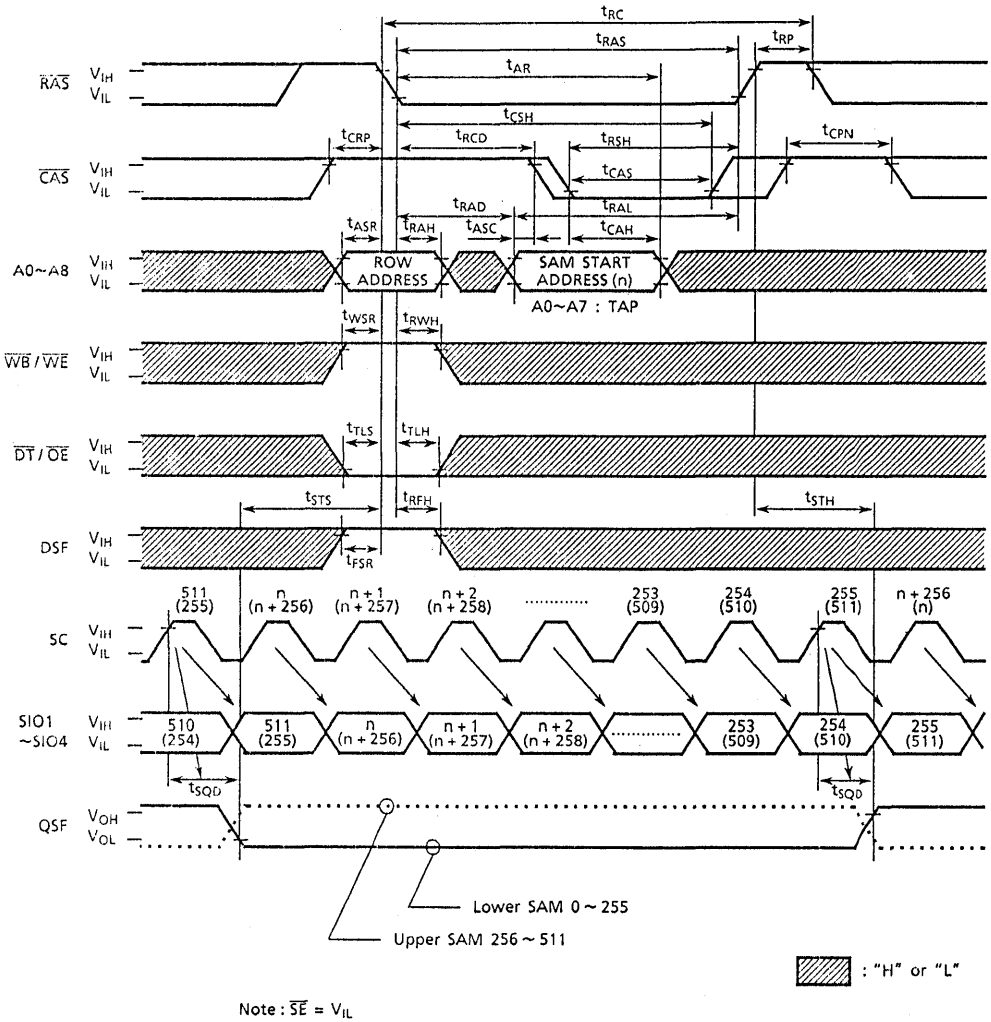
REAL TIME READ TRANSFER CYCLE



Note : $\overline{SE}$ = V_{IL}

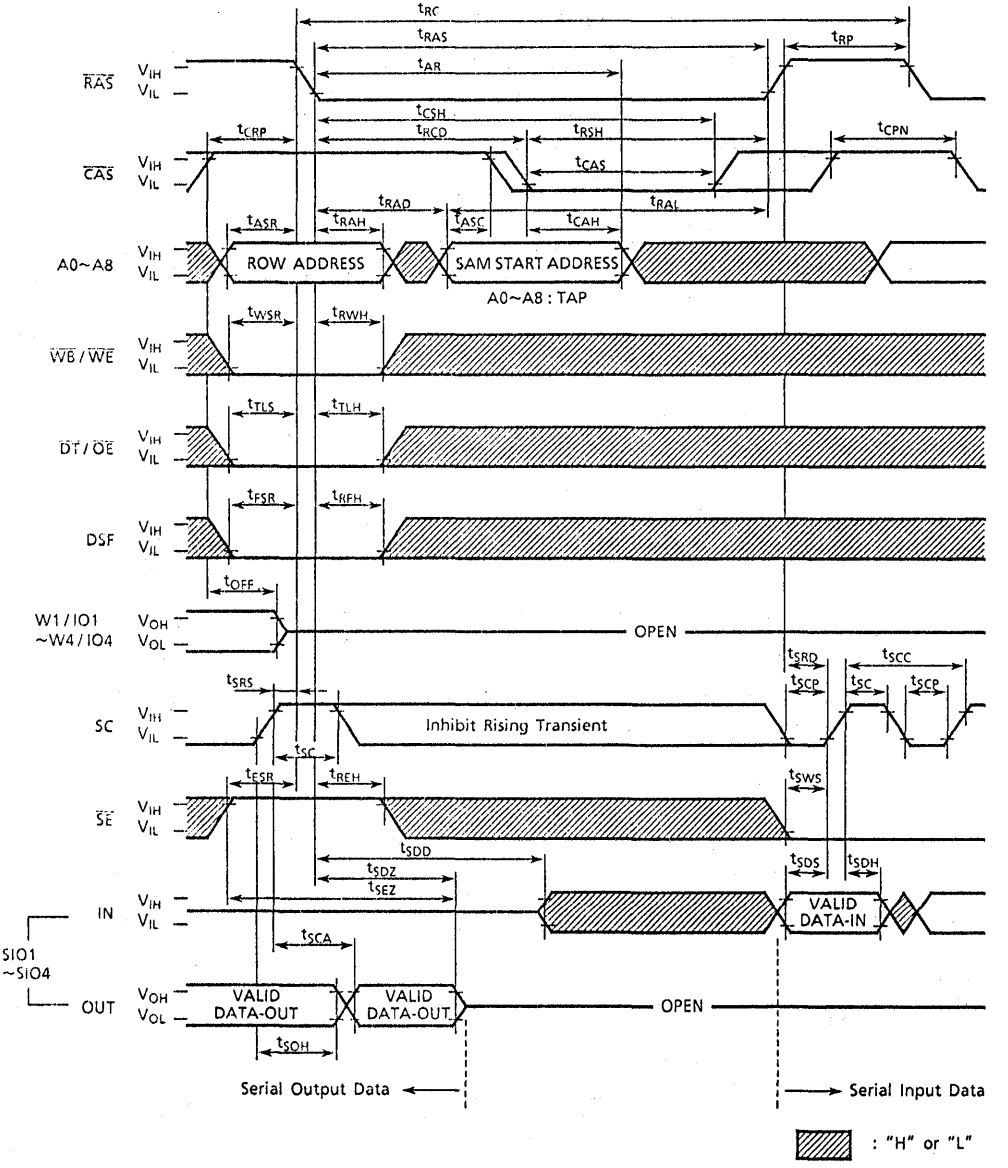
: "H" or "L"

SPLIT READ TRANSFER CYCLE

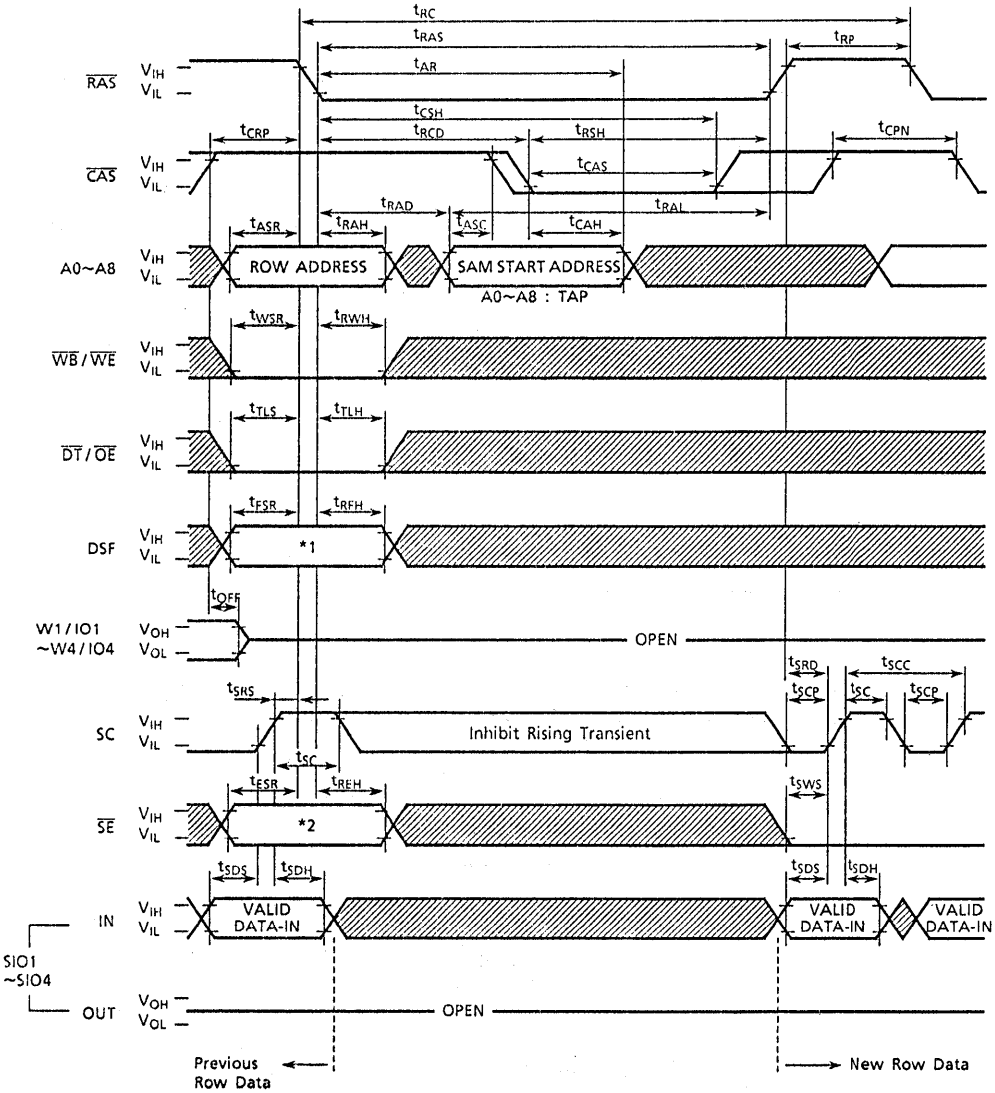


Note : $\overline{SE}$ = V_{IL}

PSEUDO WRITE TRANSFER CYCLE

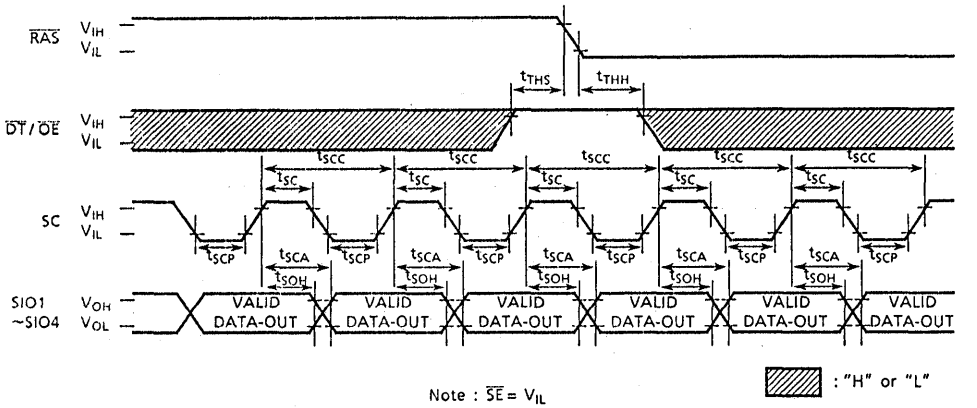


WRITE TRANSFER CYCLE



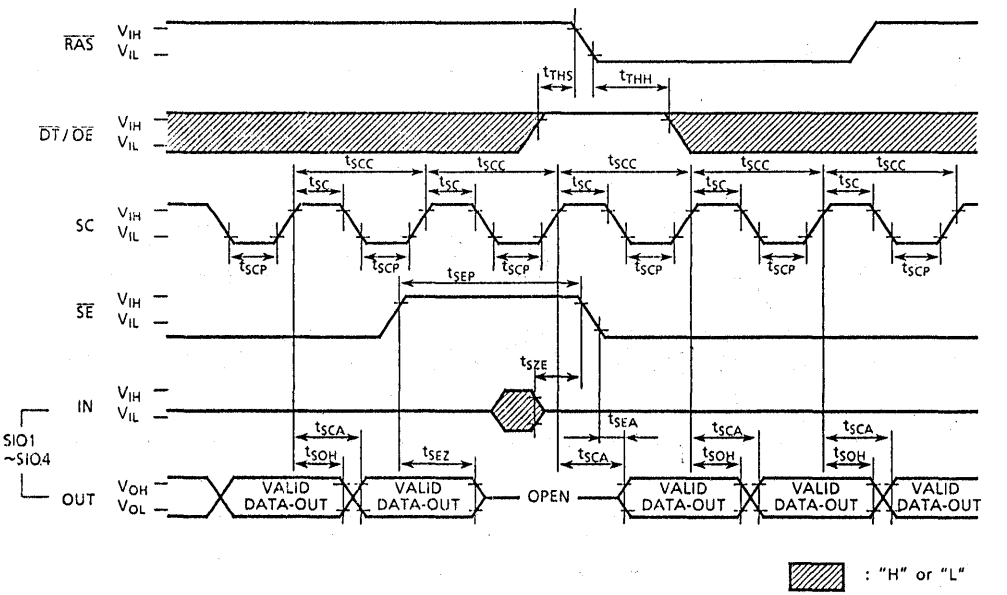
*1 DSF	*2 $\overline{SE}$	Cycle
0	0	Write Transfer
1	*	Write Transfer

SERIAL READ CYCLE ($\overline{SE}=V_{IL}$)

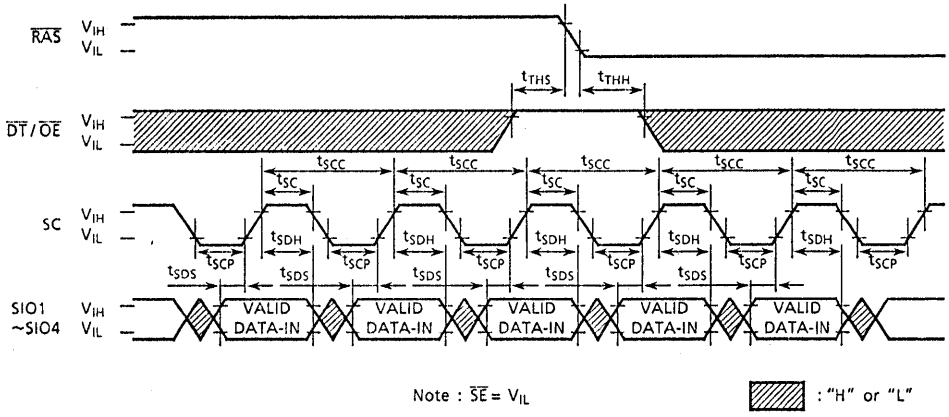


Note : $\overline{SE}=V_{IL}$

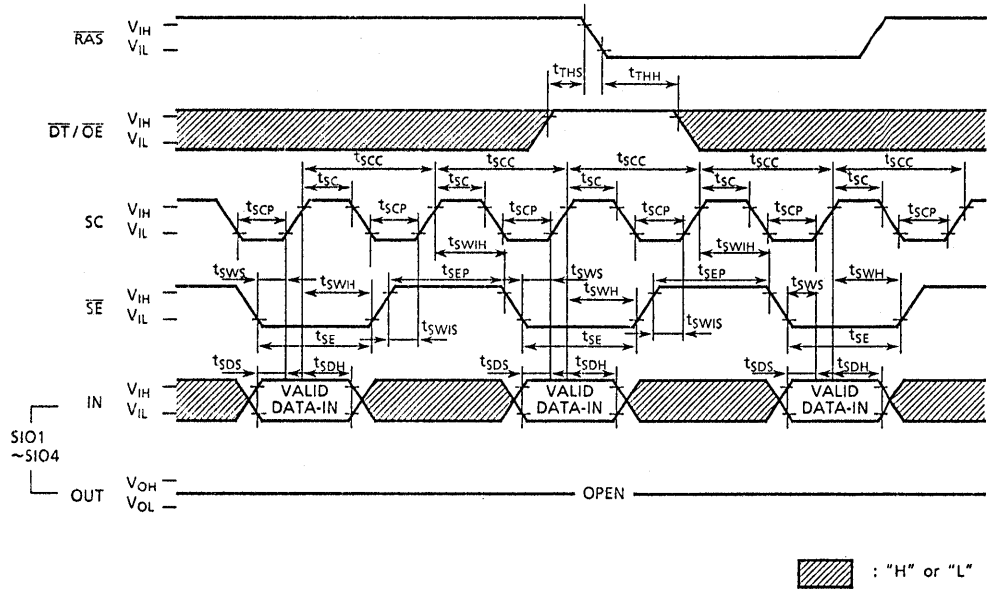
SERIAL READ ($\overline{SE}$ Controll Outputs)



SERIAL WRITE CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE ($\overline{SE}$ Controlled Inputs)



PIN FUNCTION

ADDRESS INPUTS : $A_0 \sim A_8$

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the TC524259BJ/BZ are multiplexed onto 9 address input pins ($A_0 \sim A_8$). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

ROW ADDRESS STROBE : $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

COLUMN ADDRESS STROBE : $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF to select, in conjunction with the $\overline{RAS}$ control, either read/write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

DATA TRANSFER/OUTPUT ENABLE : $\overline{DT}/\overline{OE}$

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT}/\overline{OE}$ is used as an output enable control. When the $\overline{DT}/\overline{OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE PER BIT/WRITE ENABLE : $\overline{WB}/\overline{WE}$

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).
When $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

WRITE MASK DATA/DATA INPUT AND OUTPUT : $W_1/IO_1 \sim W_4/IO_4$

When the write-per-bit (New Mask Mode) function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT}/\overline{OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$, whichever occurs first.

SERIAL CLOCK : SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer (8-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).
The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read/pseudo write/write transfer operations and should not be clocked while the SAM port is in the standby mode to prevent the SAM pointer from being incremented.

SERIAL ENABLE : $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

SPECIAL FUNCTION CONTROL INPUT : DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features consisting of write per bit 2, block write, block write (mask 1 & 2) ,load color / mask register and split read transfer can be invoked.

SPECIAL FUNCTION OUTPUT : QSF

QSF is an open drain output signal which, during split register operation, indicates which half of the split SAM is being accessed. Since QSF is an open drain output, it must be pulled up to V_{CC} with an appropriate pull-up resistor. QSF "on" (low state) indicates that the lower split SAM (Bits 0 thru 255) is being accessed and QSF" off" (open state) indicates that the upper split SAM (Bits 256 thru 511) is begin accessed. After the QSF has toggled to either an open or low state, a delay of t_{STS} must be met before a split read transfer operation can be performed on the non-active half of the split SAM.

SERIAL INPUT / OUTPUT : SIO1~SIO4

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During subsequent write transfer cycle, the SAM remains in the input mode.

OPERATION MODE

The RAM port and data transfer operating of the TC524259BJ/BZ are determined by the state of $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and the Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operation, respectively.

Table 1. Operation Truth Table

$\overline{CAS}$ falling edge			DSF	0	0	1	1
$\overline{RAS}$ falling edge			DSF	0	1	0	1
$\overline{CAS}$	$\overline{DT}/\overline{CE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$				
0	*	*	*	$\overline{CAS}$ before $\overline{RAS}$ Refresh			
1	0	0	0	Write Transfer	Write Transfer	Write Transfer	Write Transfer
1	0	0	1	Pseudo Write Transfer		Pseudo Write Transfer	
1	0	1	*	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	*	Pead/Write per Bit 1	Read/Write per Bit 2	Block Write (Mask 1)	Block Write (Mask 2)
1	1	1	*	Read/Write	Load Mask	Block Write	Load Color

Table 2. Functional Truth Table

Function	$\overline{RAS}$ ↓					$\overline{CAS}$ ↓	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{RAS}$ ↓	$\overline{CAS}$ ↓	$\overline{CAS}$ ↓ $\overline{WE}$		WM1	Color
$\overline{CAS}$ before $\overline{RAS}$ Refresh	0	*	*	*	*	–	*	–	*	–	–	–	–	–
Write Transfer	1	0	0	0	0	*	Row	TAP	*	*	*	–	–	–
Pseudo Write Transfer	1	0	0	0	1	*	Row	TAP	*	*	*	–	–	–
Write Transfer	1	0	0	1	*	*	Row	TAP	*	*	*	–	–	–
Read Transfer	1	0	1	0	*	*	Row	TAP	*	*	*	–	–	–
Split Read Transfer	1	0	1	1	*	*	Row	TAP	*	*	*	–	–	–
Write per Bit 1	1	1	0	0	*	0	Row	Column	WM1	–	DIN	WM1	Load use	–
Block Write (Mask 1)	1	1	0	0	*	1	Row	Column A2C-8C	WM1	Column Select	–	WM1	Load use	use
Write per Bit 2	1	1	0	1	*	0	Row	Column	*	–	DIN	WM1	use	–
Block Write (Mask 2)	1	1	0	1	*	1	Row	Column A2C-8C	*	Column Select	–	WM1	use	use
Read Write	1	1	1	0	*	0	Row	Column	*	–	DIN	–	–	–
Block Write	1	1	1	0	*	1	Row	Column A2C-8C	*	Column Select	–	–	–	use
Load Mask	1	1	1	1	*	0	Row	*	*	–	WM1	–	Load	–
Load Color	1	1	1	1	*	1	Row	*	*	–	Color	–	–	Load

* : "0" or "1" , TAP : SAM start address , – : not used

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked : $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer and read write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split read transfer, load mask, load color register, write per bit 2 and block write (Mask 2), can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write (No Mask, Mask 1) feature can be invoked.

RAM PORT OPERATION

FAST PAGE MODE CYCLE

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycle during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 μseconds. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT}/\overline{OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH

The TC524259BJ/BZ also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (Refer to Figure 1).

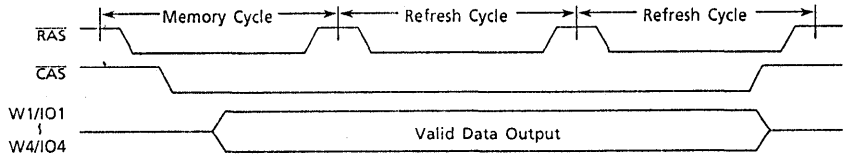


Figure 1. Hidden Refresh Cycle

WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. Two types of write-per-bit may be utilized-"New Mask Mode" or "Old Mask Mode". The state of the signals required to select the modes of write-per-bit are shown in table 3.

The write-per-bit 1 (New Mask Mode) function is enabled when $\overline{WB}/\overline{WE}$ and DSF are held "low" at the falling edge of $\overline{RAS}$ in a random write operation. Also, at the falling edge of $\overline{RAS}$, the mask data on the W_i/IO_i pins are latched into a write mask register (WM1). New write mask data must be presented at the W_i/IO_i pins at every falling edge of $\overline{RAS}$. A "0" on any of the W_i / IO pins will disable the corresponding write circuits and new data will not be written into the RAM. A "1" on any of the W_i/IO_i pins will enable the corresponding write circuits and new data will be written into the RAM.

The write-per-bit 2 (Old Mask Mode) function is enabled when $\overline{WB}/\overline{WE}$ is "low" and DSF is "high" at the falling edge of $\overline{RAS}$ in a random write operation. This function does not use the data present on the W_i/IO_i pins at the falling edge of $\overline{RAS}$ as write mask data. Therefore, data on the W_i/IO_i pins at the falling edge of $\overline{RAS}$ is a don't care ("H" or "L"). The write mask data which is utilized by this function resides in the write mask register (WM1). The mask data is placed into the "WM1" write mask register by using either the "Load Mask Register Cycle", "Write-per-bit 1 (New Mask Mode) Function", or "Block Write 1 (New Mask Mode) Function"

Table 3. Write-per-bit function truth table

At the falling edge of $\overline{RAS}$ ($\overline{RAS}\searrow$)					$\overline{CAS}\searrow$	Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	W/IO	DSF	
H	H	H	L	*	L	Normal Write
H	H	L	L	WM1	L	Write-per-bit 1 (New Mask Mode)
H	H	L	H	*	L	Write-per-bit 2 (Old Mask Mode)

* : don't care (H or L)

An example of the write-per-bit function using a display application is shown in Figures 2 and 3.

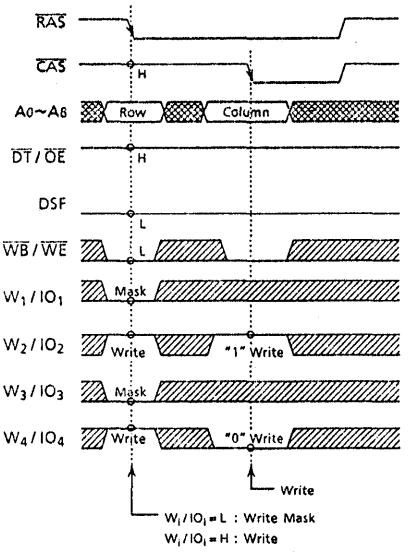


Figure 2. Write-per-bit 1 timing cycle

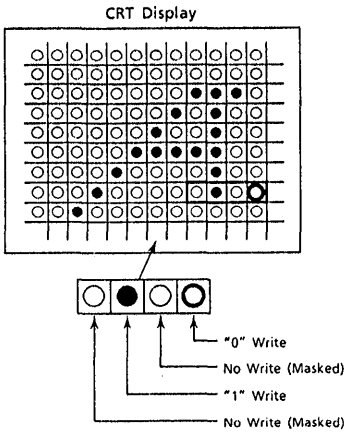


Figure 3. Corresponding bit-map

LOAD COLOR REGISTER

The TC524259BJ/BZ is provided with an on-chip 4-bits register (color register) which is used in the block write function. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{DT}$ / $\overline{OE}$, $\overline{WB}$ / $\overline{WE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding DSF "low" at the falling edge of $\overline{CAS}$. The data presented on the W_i / IO_i lines are subsequently latched into the color register at the falling edge of $\overline{CAS}$ or $\overline{WB}$ / $\overline{WE}$, whichever occurs later. During the load color register cycle, a valid row address (A_0 thru A_8) is not required. However, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ is refreshed.

LOAD MASK REGISTER

The TC524259BJ/BZ has an on-chip 4 bit register (WM1 register) which provides the I/O mask data during the write-per-bit (New and Old Mask Mode) and Block Write (New and Old Mask Mode) functions. Each bit of the mask register corresponds to one of the DRAM I/O blocks. The mask data must be specified in the WM1 register by using the load mask register cycle prior to the execution of "Write-Per-Bit 2" and "Block Write 2" old mask mode functions. The load mask register cycle is initiated by holding $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by DSF "high" at the falling edge of $\overline{CAS}$. The data presented on the W_i/IO_i lines are subsequently latched into the mask register at the falling edge of either $\overline{CAS}$ or $\overline{WB}/\overline{WE}$, whichever occurs later. The mask data which is latched into the WM1 register will also be updated by the write-per-bit 1 (New Mask Mode) or Block Write 1 (New Mask Mode) functions. During the load mask register cycle, a valid row address (A_0 thru A_8) is not required. However, the memory cells of the row address which is latched at the falling edge of $\overline{RAS}$ is refreshed.

BLOCK WRITE

Block write is a special RAM port write operation which, in a single $\overline{RAS}$ cycle, writes the data in the color register into 4 consecutive column address locations starting from a selected column in a selected row. Three modes of block write operation may be selected-No Mask Mode, New Mask Mode, Old Mask Mode. Column mask capability is applicable on all three modes. The seven most significant column addresses (A2C~A8C) are latched at the falling edge of $\overline{CAS}$ to designate the starting column address and the two least significant column addresses (A0C~A1C) are "don't care". The column mask data is also provided on the W_i/IO_i pins at the falling edge of $\overline{CAS}$. This column mask data will enable/disable the write operation on any of the 4 consecutive column address locations.

A block write cycle is selected by holding $\overline{CAS}$, and $\overline{DT}/\overline{OE}$ "high" at the falling edge of $\overline{RAS}$ and DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB}/\overline{WE}$ and DSF inputs at the falling edge of $\overline{RAS}$ will select one of the three modes of block write as shown in the following table 4.

When the DSF input at the falling edge of $\overline{RAS}$ is "low", the state of $\overline{WB}/\overline{WE}$ selects either "No Mask Mode" or "New Mask Mode". If $\overline{WB}/\overline{WE}$ is "high" at the falling edge of $\overline{RAS}$, the block write (No Mask Mode) is selected. If $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, the block write 1 (New Mask Mode) is selected and the mask data on the W_i/IO_i pins are latched and used like the write-per-bit 1 (New Mask Mode) function.

If DSF is "high" and $\overline{WB}/\overline{WE}$ is "low" at the falling edge of $\overline{RAS}$, then the block write 2 (Old Mask Mode) is selected and the mask data stored in the "WM1" register is used. The I/O masking for this function is used in the same manner as the write-per-bit 2 (Old Mask Mode)..

Table 4. Block Write function truth table

At the falling edge of $\overline{RAS}$ ($\overline{RAS}\searrow$)					$\overline{CAS}\searrow$		Function
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	DSF	W_i/IO_i	DSF	W_i/IO_i	
H	H	H	L	*	H	Column Mask	Block Write (No Mask Mode)
H	H	L	L	WM1	H	Column Mask	Block Write (Mask 1) (New Mask Mode)
H	H	L	H	*	H	Column Mask	Block Write (Mask 2) (Old Mask Mode)

* : don't care (H or L)

An example using the block write 1 (New Mask Mode) function with a data mask on W_1/IO_1, W_4/IO_4 and column 2 is shown in Figure 5. Also, an example using a window clear clear and fill application is shown in Figure 6.

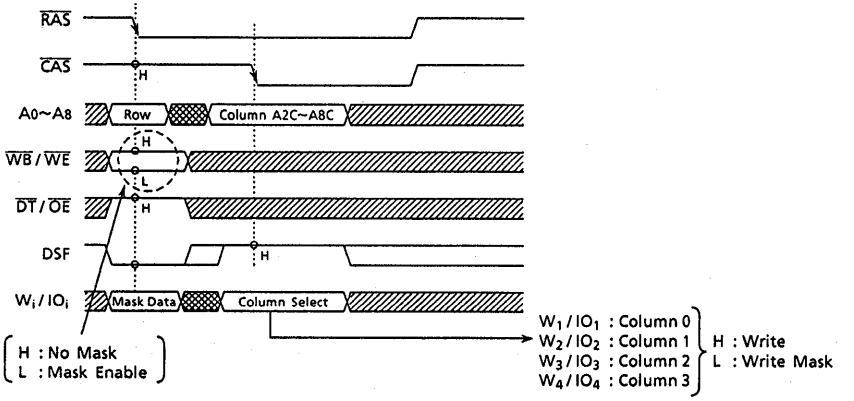


Figure 4. Block Write Timing

	Mask Data	Column Select	Color Resister Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1

	Column 0	Column 1	Column 2	Column 3
W_1/IO_1				
W_2/IO_2	0	0		0
W_3/IO_3	1	1		1
W_4/IO_4				

Mask
Mask
Mask

Figure 5. Example of Block Write Operation

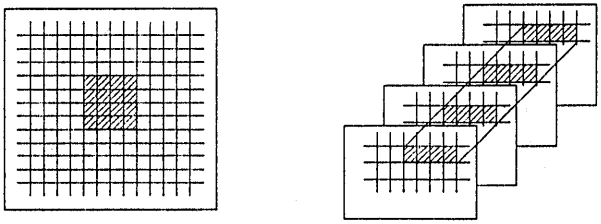


Figure 6. Examples of Block Write Application

FAST PAGE MODE BLOCK WRITE CYCLE

Fast page mode block write can be used to perform high speed clear and fill operations. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read/write operation will occur. Therefore a combination of block write and read/write operations can be performed during a fast page mode block write cycle. Refer to the example shown in Figure 10.

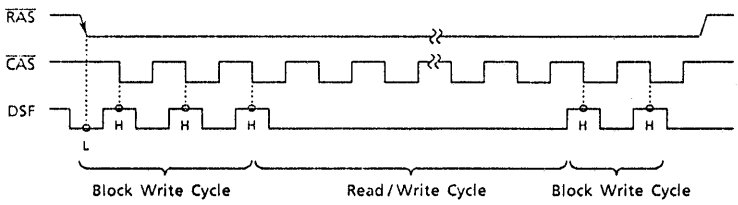


Figure 7. Fast Page Mode Block Write Cycle

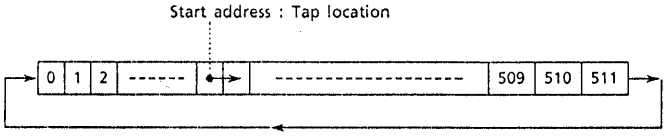
SAM PORT OPERATION

The TC524259BJ/BZ is provided with a 512 words by 4 bits serial access memory (SAM) which can be operated in the single register mode or the split register mode.

SINGLE REGISTER MODE

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; Data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM→SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit, as illustrated below.



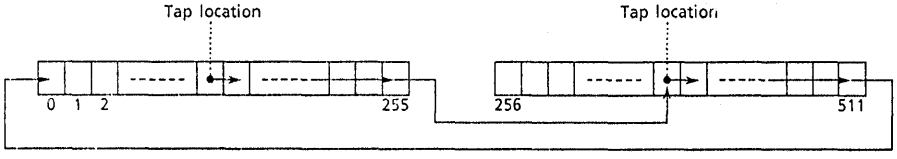
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 5.

Table 5. Truth Table for SAM Port Operation

SAM PORT OPERATION	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	FUNCTION	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode		⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode		⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

SPLIT REGISTER MODE

In split register mode, data can be shifted out of one half of the SAM while a split read transfer is being performed on the other half of the SAM. A normal (Non-split) read transfer operation must precede any split read transfer operation. The non-split read transfer will set the SAM port into output mode. The split read transfers will not change the SAM port mode set by preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted out of one of the split SAM registers starting from any at the 256 tap locations, excluding the last address of each split SAM, data is shifted out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first split SAM and then the SAM pointer moves to the tap location selected for the second split SAM to shift data out sequentially starting from this tap location to the most significant bit (511 or 255) and finally wraps around to the least significant bit, as illustrated in the example below.



REFRESH

The SAM data registers are static flip-flop, therefore a refresh is not required.

DATA TRANSFER OPERATION

The TC524259BJ/BZ features two types of internal data transfer capability between RAM and the SAM, as shown in Figure 8. During a normal (Non-split) transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split read transfer, 256 words by 4 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal .

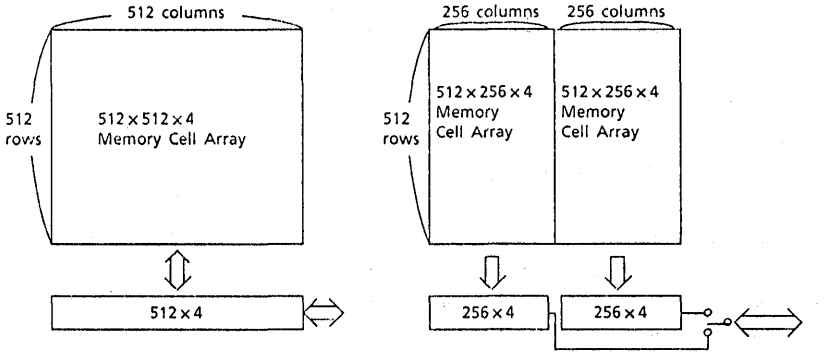


Figure 8. (a) Normal (Non-split) Transfer (b) Split Read Transfer

As shown in Table 6, the TC524259BJ/BZ supports four types of transfer operations: Read transfer, Split read transfer, Write transfer, and Pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF latched at the falling edge of $\overline{RAS}$. During normal (Non-split) data transfer operations, the SAM port is switched from input to output mode (Read transfer) or output to input mode (Write transfer/Pseudo write transfer) whereas it remains unchanged during split read transfer operations. During a data transfer cycle, the row address A_0~A_8 select one of the 512 rows of the memory array to or from which data will be transferred and the column address A_0~A_8 select one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split read transfer cycles, the most significant column address (A8C) is controlled internally to determine which half of the serial register will be reloaded from the RAM array.

Table 5. Transfer Modes

at the falling edge of $\overline{RAS}$					Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	DSF				
H	L	H	*	L	Read Transfer	RAM → SAM	512×4	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	512×4	Output → Input
H	L	L	H	L	Pseudo Write Transfer	-	-	Output → Input
H	L	L	*	H	Write Transfer	SAM → RAM	256×4	Output → Input
H	L	H	*	H	Split Read Transfer	RAM → SAM	256×4	Not changed

* : "H" or "L"

READ TRANSFER CYCLE

A read transfer consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low" $\overline{WB}/\overline{WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and this data becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 9 shows the operation block diagram for read transfer operation.

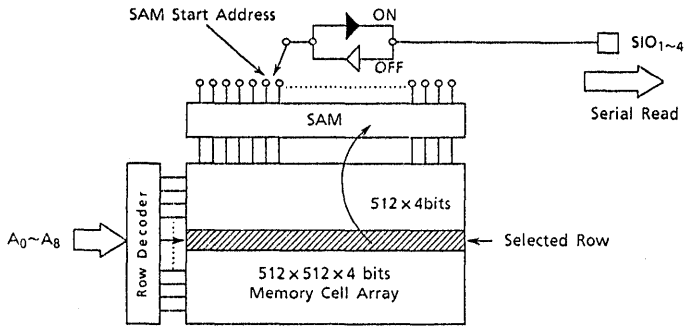


Figure 9. Block Diagram for Read Transfer Operation

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 10.

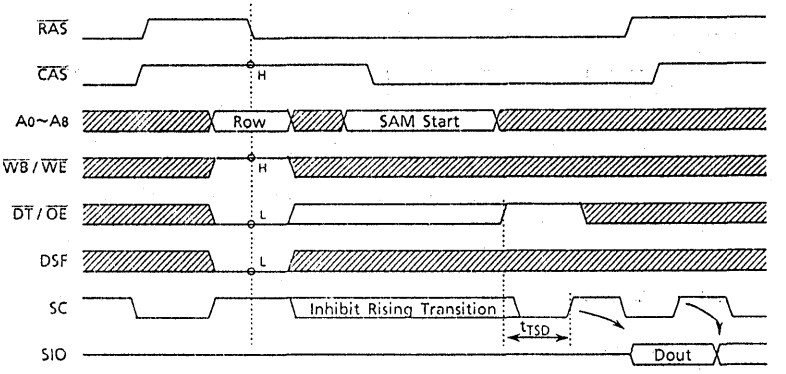


Figure 10. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time t_{SCA} for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 11.

The timing restriction t_{TSL}/t_{TSD} are 5ns min / 15ns min. The split read transfer mode eliminates these timing restrictions.

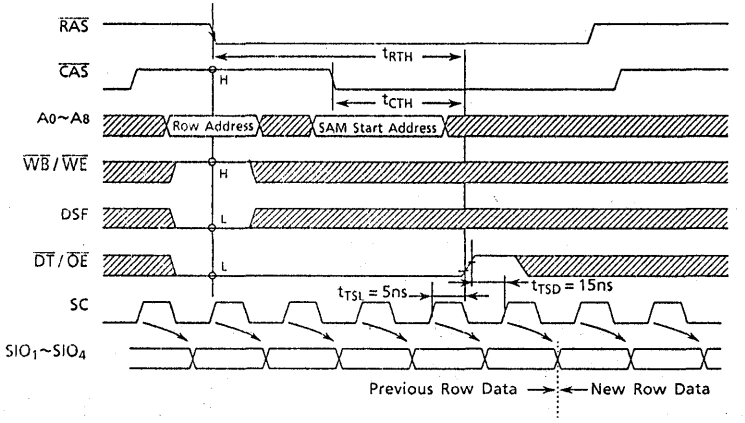
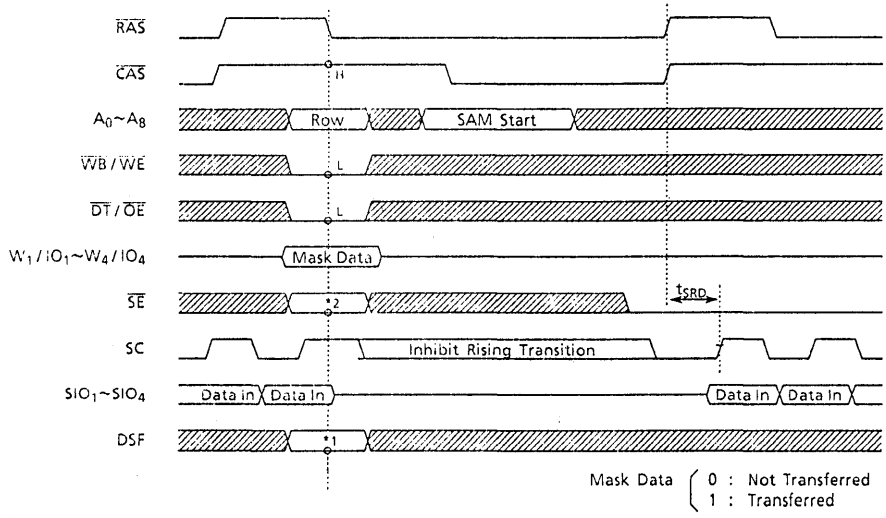


Figure 11. Real Time Read Transfer

WRITE TRANSFER CYCLE

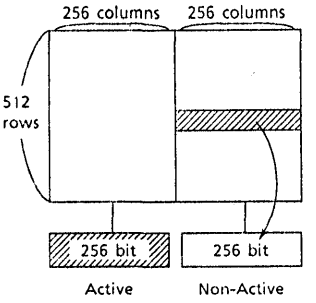
A write transfer cycle transfers the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer cycle. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. Also if DSF is "high" under the condition of a "high" $\overline{CAS}$, "low" $\overline{DT}/\overline{OE}$ and "low", $\overline{WB}/\overline{WE}$ at the falling edge of $\overline{RAS}$, a write transfer is invoked independent of the state of $\overline{SE}$.



*1 DSF	*2 $\overline{SE}$	Operation
L	L	Write Transfer
H	L or H	Write Transfer

Figure 12. Write Transfer Timing

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 14. Split Register Mode

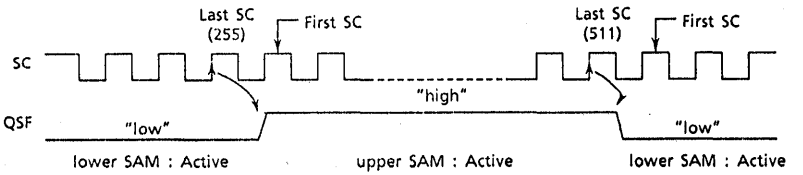


Figure 15. QSF Output State During Split Register Mode

SPLIT READ TRANSFER CYCLE

A split read transfer consists of loading 256 words by 4 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figure 16 and 17, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS}, from the change of state of the QSF output, is satisfied.

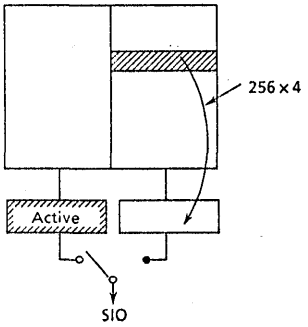


Figure 16. Block Diagram for Split Read Transfer

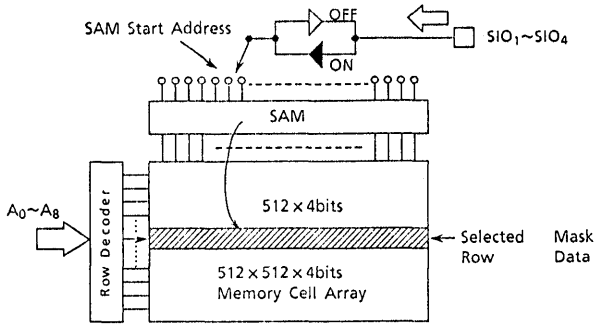


Figure 13. Block Diagram for Write Transfer Operation

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

PSEUDO WRITE TRANSFER CYCLE

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (A data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

SPLIT READ TRANSFER AND QSF

The TC524259BJ/BZ features a split read transfer capability between the RAM and the SAM. During split read transfer operation, the serial register is split into two halves which can be controlled independently. Split read transfer operations can be performed to one half of the serial register while serial data can be shifted out of the other half of the serial register, as shown in Figure 14. The most significant column address location (A8C) is controlled internally to determines which half of the serial register will be reloaded from the RAM array. QSF is an output in which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 15.

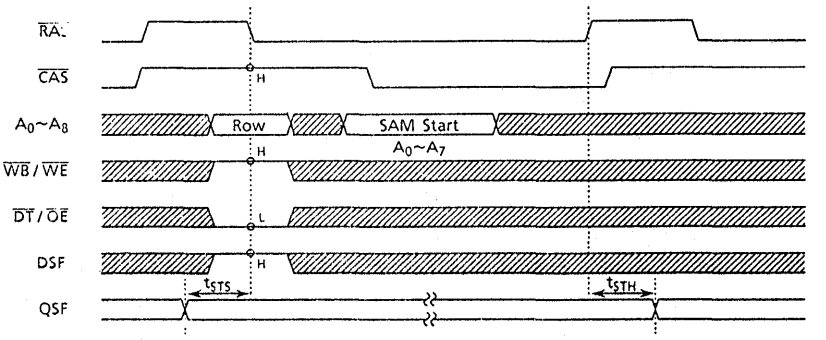


Figure 17. Timing Diagram for Split Read transfer

A normal (Non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 18.

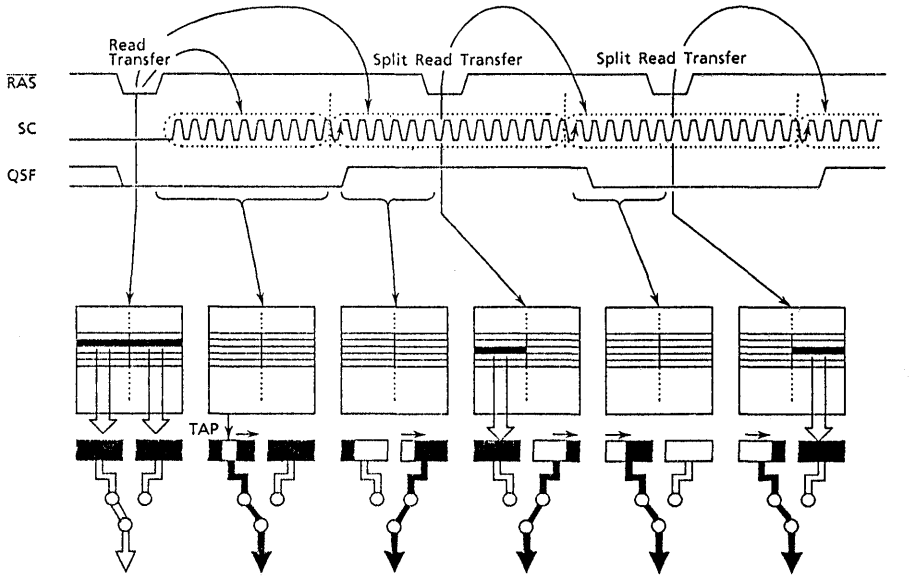


Figure 18. Example of Consecutive Read Transfer Operations

SPLIT-REGISTER OPERATION SEQUENCE (EXAMPLE)

Split read transfers must be preceded by a normal read transfer. Figure 19 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511) and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register address 256 in this example and the pointer is incremented from this location by cycling the SC clock.

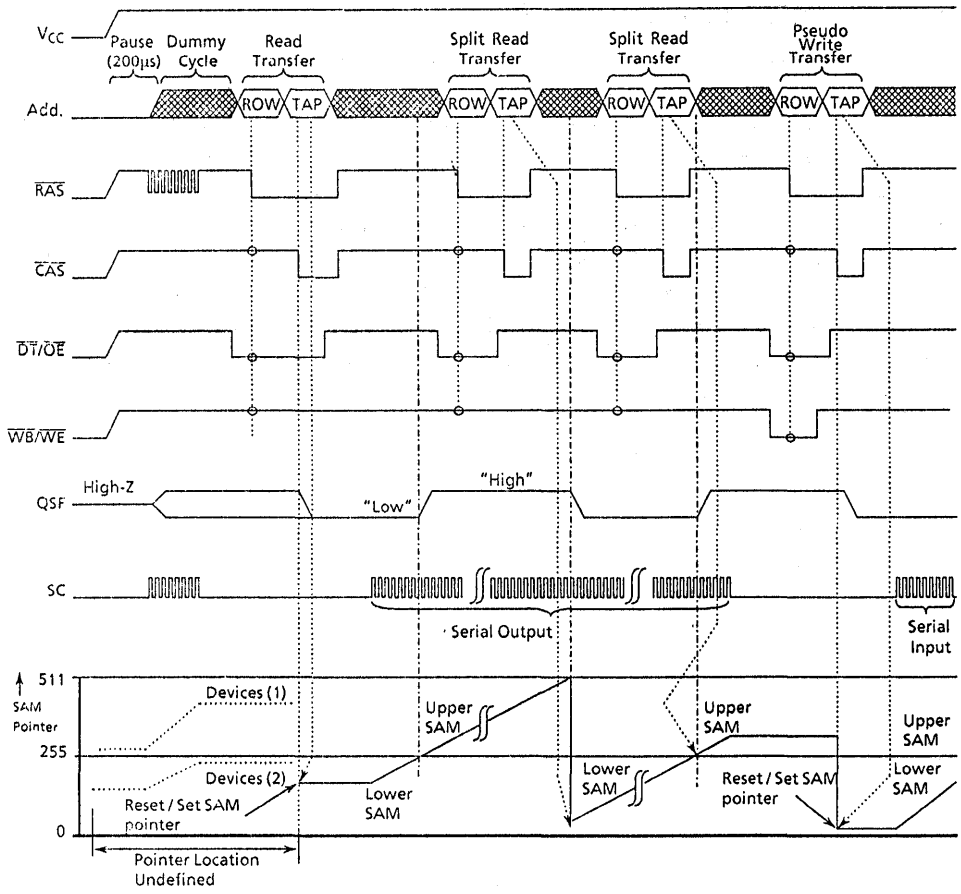
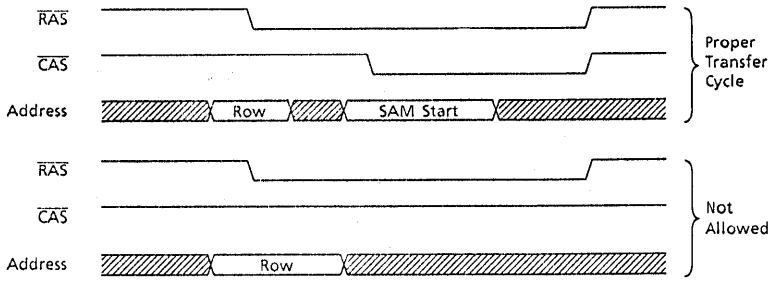


Figure 19. Example of Spilit SAM Register Operation Seguence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

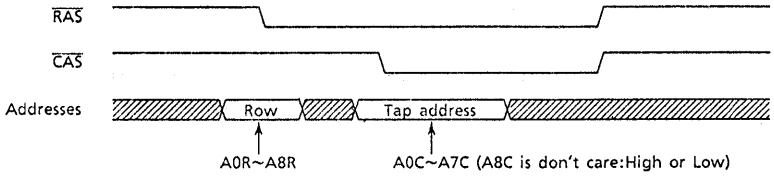
TRANSFER OPERATION WITHOUT $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column address are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore a transfer cycle with $\overline{CAS}$ held "high" is not allowed (Refer to the illustration below).



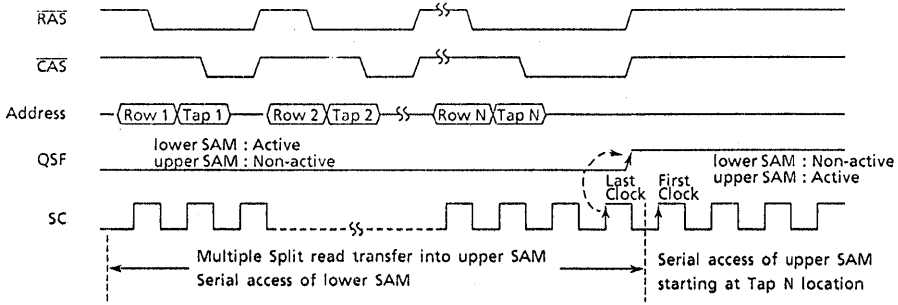
TAP LOCATION SELECTION IN SPLIT READ TRANSFER OPERATION

(a) In a split read transfer operation, column addresses A0C through A7C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split read transfer, column address A8C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$.



During a split transfer, it is not allowed to set the last address location (A0C~A7C=FF), in either the lower SAM or the upper SAM, as the tap location.

(b) In the case of multiple split read transfers performed into the same split SAM register, the tap location specified during the last split read transfer, before QSF toggles, will prevail. In the example shown below, multiple split read transfers are performed into the upper SAM (Non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



SPLIT READ TRANSFER OPERATION ALLOWABLE PERIOD

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read transfers and highlights the time periods where split read transfer are allowed, relative to SC and QSF.

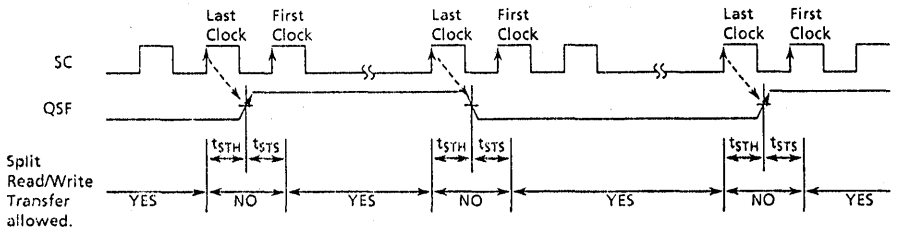
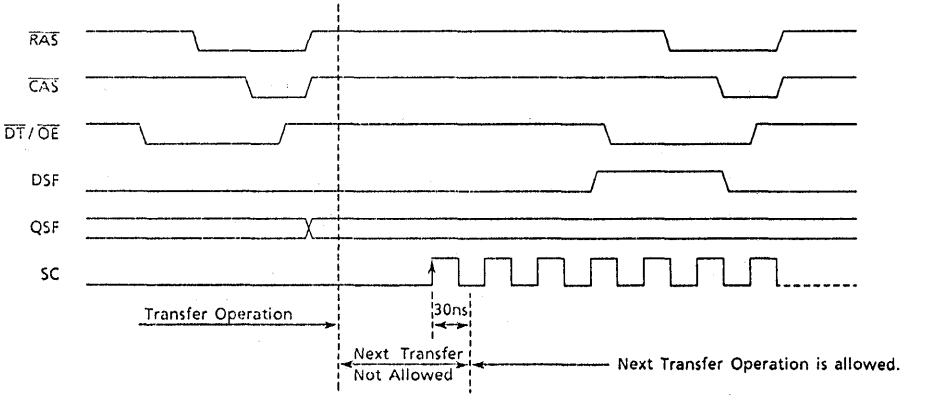


Figure 20. Split Transfer Operation Allowable Periods

As indicated in Figure 20, a split read transfer is not allowed during the period of $t_{STH} + t_{STS}$.

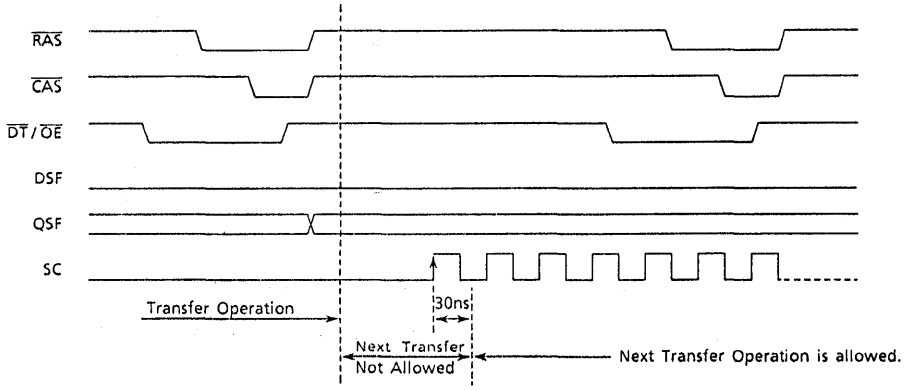
SPLIT READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

A split read transfer may be performed following a normal read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



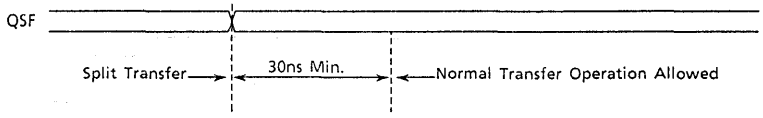
NORMAL READ TRANSFER CYCLE AFTER NORMAL READ TRANSFER CYCLE

Another read transfer may be performed following the read transfer provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (Refer to the illustration shown below).



NORMAL TRANSFER AFTER SPLIT READ TRANSFER

A normal transfer (read / write / pseudo write) may be performed following split read transfer operation provided that a 30ns minimun delay is satisfied after the QSF signal toggles.



POWER-UP

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{CC} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

INITIAL STATE AFTER POWER-UP

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the TC524258BJ/BZ is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μseconds pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

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