Data Sheet

PT880 Pro North Bridge

Revision 1.0
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VIA TECHNOLOGIES, INC.

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REVISION HISTORY

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1.0	9/27/05	Initial external release	CY

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PT880 PRO NORTH BRIDGE

800 / 533 / 400 MHz Intel Pentium 4 Front Side Bus
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1 GB/Sec Ultra V-Link Interface

PRODUCT FEATURES

- **Defines Highly Integrated Solutions for Performance Desktop PC Designs**
  - High performance North Bridge with 800MHz Front Side Bus for Pentium 4 processors plus PCI Express and AGP bus
  - Dual-channel, 128-bit, advanced SDRAM controller supporting DDR2 533 / 400 SDRAM
  - Combines with VIA VT8235M / VT8237R / VT8237R Plus / VT8251 V-Link South Bridge for integrated 10/100 LAN, AC97 Link, ATA133 IDE, LPC, USB 2.0, Serial ATA (VT8237R / VT8237R Plus & VT8251), PCI-Express (VT8251) and High-Definition Audio (VT8251)
  - 1.5V Core and Pentium 4 AGTL+ I/O
  - 37.5 x 37.5mm FCBGA package (Flip Chip Ball Grid Array) with 1054 balls and 1mm ball pitch
- **High Performance CPU Interface**
  - Supports Intel 800 / 533 / 400 MHz FSB Pentium 4 and Pentium M processors
  - Supports Intel Hyper-Threading Technology
  - Supports DBI (Dynamic Bus Inversion) and Data, Address, Response Parity
  - Deep In-Order command Queue (IOQ)
  - Built-in Phase Lock Loop circuitry for optimal skew control within and between clocking regions
- **High Bandwidth 1 GB/Sec "Ultra V-Link" South Bridge Interface Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, Ultra V-Link Host interface with 1 GB/sec total bandwidth
  - Full duplex transfers with separate command / strobe for 4x and 8x mode
  - Request / Data split transaction
  - Transaction assurance for V-Link Host to Client access eliminates V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to minimize data wait-state and throttle transfer latency to avoid data overflow
  - Highly efficient V-Link arbitration with minimum overhead
- **Advanced High Bandwidth PCI Express Interface**
  - Supports PCI Express 1.0a
  - Supports one 4-Lane PCI Express port for high bandwidth peripheral devices (configurable lane width, either 4 or 1)
  - Supports interconnect power management
  - Supports polarity reversal
  - Supports Hot Plug
  - Loop-back testing mode for easy debugging mode for PCI Express

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.0 compliant with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Asynchronous AGP and CPU interface
  - Thirty-two level request queue for read and write
  - One hundred-twenty-eight level (quadwords) of read data FIFO
  - Sixty-four level (quadwords) of write data FIFO
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme
  - VPX-I / VPX-II support (see separate VIA VT8101 and VT8102 data sheets)
- **Advanced High-Performance 128-bit, Dual-Channel, DDR / DDR2 SDRAM Controller**
  - Supports two operating modes:
    - DDR2 Mode
      - Supports DDR2 533 / 400 memory
      - Supports mixed 64Mb / 128Mb / 256Mb / 512Mb / 1024Mb / 2048Mb x 8/16 DDR2 SDRAMs
      - Supports 4 unbuffered double-sided DIMMs and up to 4 GB of physical memory
      - Supports CL 3 / 4 / 5 for DDR2 533 / 400
    - DDR Mode
      - Supports DDR 400 / 333 / 266 / 200 memory
      - Supports mixed 64Mb / 128Mb / 256Mb / 512Mb / 1024Mb x 8/16 DDR SDRAMs
      - Supports 4 unbuffered double-sided DIMMs and up to 4 GB of physical memory
      - Supports CL 2 / 2.5 for DDR 266 / 333, CL 2.5 / 3 for DDR 400
  - Dual 64-bit data paths and two sets of memory address, data and control signals each of which drives up to two DIMMs
  - Supports asymmetric 128-bit, Dual-channel, memory accesses
  - Programmable I/O drive capability for memory address, data and control signals
  - DRAM interface pseudo-synchronous with host CPU for optimal memory performance
  - Concurrent CPU, PCIe, AGP and V-Link access for minimum memory access latency
  - Rank interleave and up to16-bank page interleave (i.e., 16 pages open simultaneously) based on LRU to effectively reduce memory access latency
  - Seamless DRAM command scheduling for maximum DRAM bus utilization (e.g., precharge other banks while accessing the current bank)
  - CPU Read-Around-Write capability for non-stalled operation
  - Speculative DRAM read before snoop result to reduce PCI master memory read latency
  - Supports Burst Read and Write operation with burst length 4 or 8
  - Integrated CPU-to-DRAM post-write buffers and CPU-to-DRAM pre-fetch buffers
  - Supports self-refresh and CAS-before-RAS DRAM refresh with staggered RAS timing
- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports Suspend-to-DRAM (STR) and DRAM self refresh
  - Supports dynamic Clock Gating for optimal chip power management
  - Supports SMI, SMM and STPCLK mechanisms
  - Supports Enhanced Intel SpeedStep Technology
  - Low-leakage I/O pads

PT880 PRO SYSTEM OVERVIEW

The PT880 Pro is a high performance, cost-effective and energy efficient North Bridge used for the implementation of high-end desktop personal computer systems based on 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors.

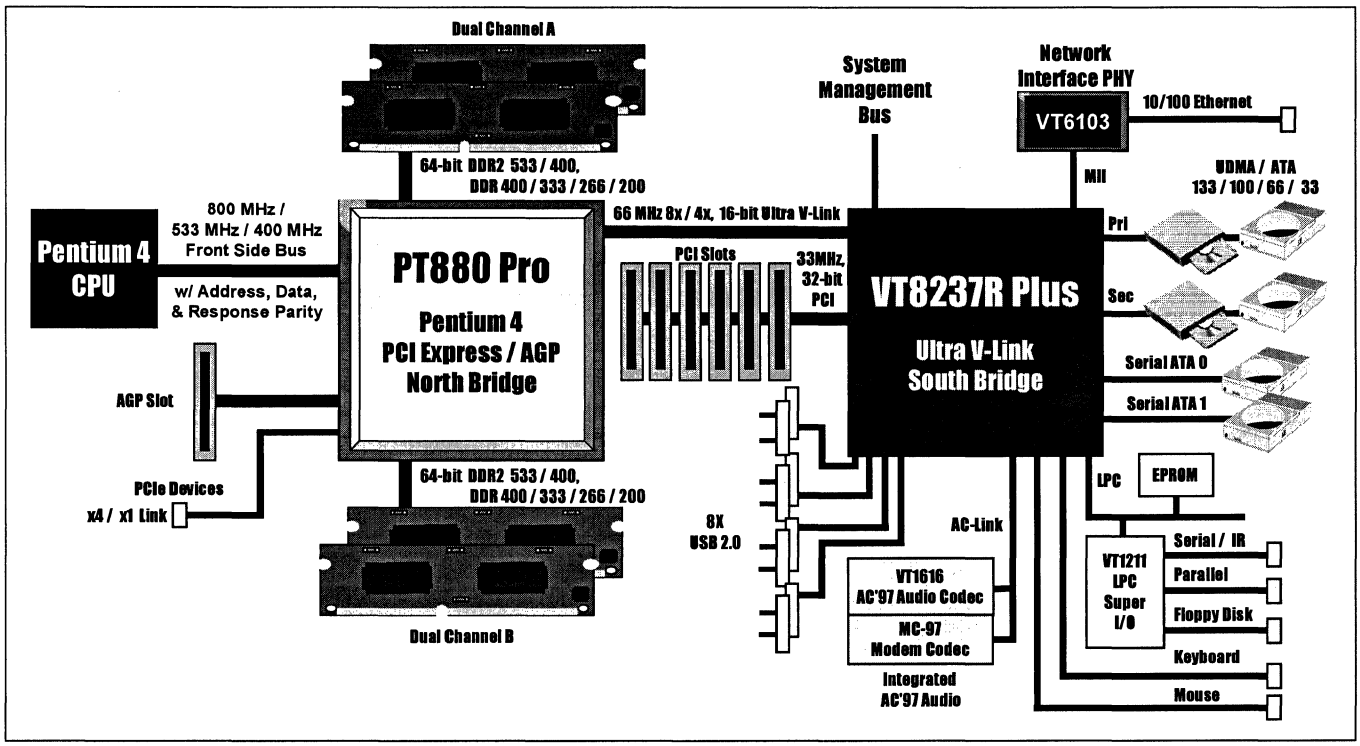


Figure 1. System Block Diagram

The chipset consists of the PT880 Pro North Bridge and the VT8237R Plus V-Link South Bridge. The PT880 Pro "Host System Controller" is an upgrade of VIA's most advanced system controller with dual DDR memory interface and PCI Express support. The PT880 Pro provides superior performance between CPU, DRAM, V-Link bus and PCI Express / AGP bus with pipelined, burst and concurrent operation. The VT8237R Plus is a highly integrated peripheral controller, it includes V-Link-to-PCI / V-Link-to-LPC controllers and integrates Serial ATA and Ultra DMA IDE controllers, USB2.0 host controller, 10/100 Mb networking MAC, AC97 and system power management controllers.

PT880 Pro Overview

The PT880 Pro supports 800 / 533 / 400 MHz FSB Intel Pentium 4 and Pentium M super-scalar processors; it implements deep In-Order Queue and supports Intel Hyper-Threading Technology to maximize system performance for multi-threaded software applications. DBI and Pentium M bus protocol, as well as Enhanced Intel SpeedStep Technology are supported, which effectively reduce overall system power consumption.

The PT880 Pro includes a PCI Express 1.0a compliant PCI Express controller, which supports one high bandwidth PCIe port. This PCIe port can be configured in either 4-Lane or 1-Lane as to serve bandwidth-hungry peripheral devices.

The PT880 Pro implements an AGP v3.0 compliant AGP controller, which supports up to 2.1 GB / second data transfer rate. Asynchronous design between AGP and CPU interface is implemented for flexible system configuration. Deep read (1024 bytes) and write (512 bytes) FIFO are integrated for optimal bus utilization and minimum data transfer latency.

The PT880 Pro supports dual 64-bit memory channels and up to 4 double-sided DIMMs (eight banks) of synchronous DRAMs for 16 GB maximum physical DDR2 memory (8 GB DDR memory). The DRAM controller supports DDR2 533 / 400 or DDR 400 / 333 / 266 / 200 SDRAM. The DDR DRAM interface allows zero wait state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024Mb (up to 2048Mb for DDR2 mode) SDRAM in x8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus.

The PT880 Pro North Bridge interfaces to the South Bridge through a high speed (1 GB/sec) 8x 66 MHz Data Transfer interconnect bus called Ultra V-Link. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. The combined PT880 Pro North Bridge and VT8237R Plus South Bridge system supports enhanced PCI bus commands such as "Memory-Read-Line", "Memory-Read-Multiple" and "Memory-Write-Invalid" commands to minimize snoop overhead. In addition, advanced features are supported such as CPU write-back forward to PCI master and CPU write-back merged with PCI post-write buffers to minimize PCI master read latency and DRAM utilization. Delay transaction and read caching mechanisms are also implemented for further improvement of overall system performance.

System Power Management

For sophisticated power management, the PT880 Pro supports dynamic Clock Gating to optimize the chip power management. A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. Enhanced Intel SpeedStep Technology enables minimization of CPU power consumption while sustaining processing power. Coupled with the VT8237R Plus south bridge chip, a complete power conscious PC main board can be implemented with no external glue-logic.

System Reliability

The PT880 Pro provides features required for high-performance commercial and consumer PCs. These features include parity on CPU, AGP, PCIe and V-Link buses.

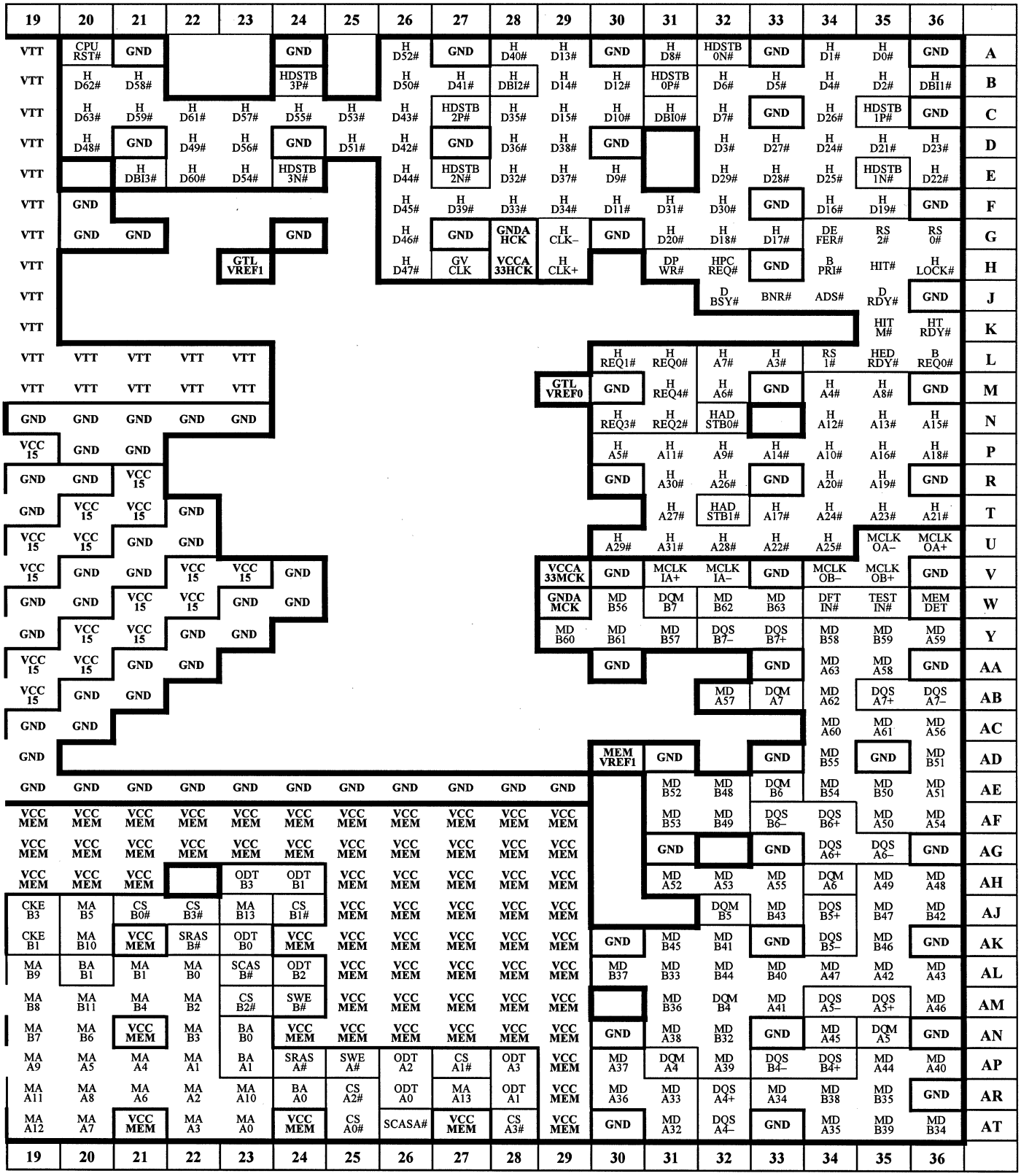
BALLOUT

Ball Diagram

Figure 2. Ball Diagram, Top View

Key	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		G D22	G D21	G D25	G D24	NC	G SBA4#	GSB STBF	GSB STBS	G WBF	G RBF		GND	VTT	VTT	VTT	VTT	VTT
B		GND	G D19	GAD STBS1	GND	GSB A6#	G SBA7#	GND	GND	G SBA0#	GND		GND	VTT	VTT	VTT	VTT	VTT
C	G D17	G D18	G D20	GAD STBF1	G D26	G D28	G SBA3#		G SBA5#	G SBA1#		G ST1	GND	VTT	VTT	VTT	VTT	VTT
D	G IRDY	G D16	G C#BE2	G C#BE3	G D27	G D29	G SBA2#			NC	INTR#	G ST0	GND	VTT	VTT	VTT	VTT	VTT
E	G FRAME	GND	GND	G D23	GND	GND	G D30	GND		GND	GND	G REQ	GND	VTT	VTT	VTT	VTT	VTT
F	GDEV SEL	G TRDY	G D15	G SERR	GND	GND	G D31	G DBIH		NC	G ST2	G GNT	GND	VTT	VTT	VTT	VTT	VTT
G	G D13	G PAR	G STOP	G D14	G C#BE1	GND	GND	G DBIL	GND	NC	NC			GND	VTT	VTT	VTT	VTT
H	G D12	GND	G D9	NC	GND	G D10	G D11	GND	NC		AGP8X DET#				GND	VTT	VTT	VTT
J	G D8	G C#BE0	G D7	G D6	G D2	G D3	GND	GND	AGP VREF1		AGP VREF0					GND	VTT	VTT
K	G D4	G D5	GAD STBF0	GAD STBS0	G D1	G D0	GND	GND								GND	VTT	VTT
L	NC	GND	NC	NC	GND	GND	GND	GND	VCC15 AGP	VCC15 AGP	VCC15 AGP						VTT	VTT
M	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	GND				GND		VTT
N	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	GND					GND	
P	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	VCC15 AGP	GND				GND		VCC 15
R	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND			GND		VCC 15	VCC 15
T	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	GND	GND		VCC 15	VCC 15	GND
U	GND	PE1 RX0–	PE1 RX0+	GND	PE1 TX0–	PE1 TX0+	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	VCC33 PE	GND	GND	GND		VCC 15	GND	GND
V	VSUS 15PE	PE1 COMP	PE1 TX1–	PE1 TX1+	GND	VCCA 33PE	GND	GND	GND	VCC33 PE	VCC33 PE	GND	GND	VCC 15	VCC 15	GND	GND	VCC 15
W	GNDA PE1	GND	PE1 RX1–	PE1 RX1+	GND	GNDA PE	PE CLK–	T CLK	GND	GND	GND	GND	VCC 15	VCC 15	GND	GND	VCC 15	VCC 15
Y	VCCA 33PE1	PE1 REXT	PE1 RX2+	PE1 RX2–	PE1 TX2–	PE1 TX2+	PE CLK+	GND	GND	GND	VCC15 VL	VCC15 VL	VCC 15	GND		VCC 15	VCC 15	GND
AA		V D13	PE1 TX3+	PE1 TX3–	PE1 RX3+	PE1 RX3–	GND	VCC 15	VCC 15	VCC 15	VCC15 VL	VCC15 VL	VCC 15		VCC 15		GND	GND
AB	GND	V D8	V D9	GND	V D12	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15		GND	GND	VCC 15
AC		V D5	V D4	V PAR	V D1	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15		VCC 15	VCC 15	VCC 15
AD		V D0	V BE#	DN STB+	DN STB–	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15		VCC 15	VCC 15	GND
AE	GND	UP STB–	UP STB+	GND	VL VREF	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15		VCC 15	GND	GND
AF		V D2	V D3	DN CMD	V D7	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15		GND	VCC MEM	VCC MEM
AG		V D6	UP CMD	GND	V D10	VL COMPP	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	VCC 15	GND	GND	GND	VCC MEM	VCC MEM
AH	GND	V D11	V D14	V D15	VSUS 15	VCC 15	VCC 15	VCC 15	GND	GND	GND	GND	GND	GND			VCC MEM	VCC MEM
AJ	PWR OK	PE WAKE#	SUS ST#	MD B5	MD B4	GND	GND	GND	GND	MEM VREF0		MD B29					VCC MEM	VCC MEM
AK	RE SET#	DQM B0	MD B1	GND	MD B0	MD B11	GND		MD B20	GND		MD B28	GND	DM COMP			CKE B0	VCC MEM
AL	GND	DQS B0–	DQS B0+	MD B3	MD B14	MD B9		MD B16	MD B21	MD B19	MD A20	MD B24	DQM B3	MD B26	GND		MA B14	CKE B2
AM	MD B6	MD B7	MD B2	MD B8	DQM B1	MD B10	MD A9	MD B17	DQM B2	MD B18	MD A17	MD B25	DQS B3–	MD B27	DQM A3	GND	BA B2	MA B12
AN	MD B13	GND	MD B12	GND	DQS B1–	MD B15	GND	MD A14	DQS B2–	GND	MD A22	DQS B3+	GND	MD B31	GND	MD A27	CKE A2	VCC MEM
AP	MD A4	MD A0	MD A5	MD A7	DQS B1+	MD A12	DQS A1–	MD A15	DQS B2+	MD B23	DQM A2	MD A19	MD B30	MD A29	DQS A3–	MD A26	CKE A0	MA A14
AR	MD A1	DQM A0	DQS A0+	MD A2	MD A3	MD A8	DQS A1+	MD A11	MD B22	MD A16	DQS A2–	MD A23	MD A28	MD A24	GND	MD A30	CKE A3	BA A2
AT	GND	DQS A0–	MD A6	GND	MD A13	DQM A1	GND	MD A10	MD A21	GND	DQS A2+	MD A18	GND	MD A25	DQS A3+	MD A31	CKE A1	VCC MEM
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 3. Ball Diagram, Top View (continued)



Ball Lists

Table 1. Ball List (Listed by Ball Number)

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name
A02	GD22	E07	GD30	L30	HREQ1#	AB05	VD12	AK34	DQSB5–	AP10	MDB23
A03	GD21	E12	GREQ	L31	HREQ0#	AB32	MDA57	AK35	MDB46	AP11	DQMA2
A04	GD25	E21	HDBI3#	L32	HA7#	AB33	DQMA7	AL02	DQSB0–	AP12	MDA19
A05	GD24	E22	HD60#	L33	HA3#	AB34	MDA62	AL03	DQSB0+	AP13	MDB30
A06	NC	E23	HD54#	L34	RS1#	AB35	DQSA7+	AL04	MDB3	AP14	MDA29
A07	GSBA4#	E24	HDSTB3N#	L35	HEDRDY#	AB36	DQSA7–	AL05	MDB14	AP15	DQSA3–
A08	GSBSTBF	E26	HD44#	L36	BREQ0#	AC02	VD5	AL06	MDB9	AP16	MDA26
A09	GSBSTBS	E27	HDSTB2N#	M31	HREQ4#	AC03	VD4	AL08	MDB16	AP17	CKEA0
A10	GWBF	E28	HD32#	M32	HA6#	AC04	VPAR	AL09	MDB21	AP18	MAA14
A11	GRBF	E29	HD37#	M34	HA4#	AC05	VD1	AL10	MDB19	AP19	MAA9
A20	CPURST#	E30	HD9#	M35	HA8#	AC34	MDA60	AL11	MDA20	AP20	MAA5
A26	HD52#	E32	HD29#	N30	HREQ3#	AC35	MDA61	AL12	MDB24	AP21	MAA4
A28	HD40#	E33	HD28#	N31	HREQ2#	AC36	MDA56	AL13	DQMB3	AP22	MAA1
A29	HD13#	E34	HD25#	N32	HADSTB0#	AD02	VD0	AL14	MDB26	AP23	BAA1
A31	HD8#	E35	HDSTB1N#	N34	HA12#	AD03	VBE#	AL17	MAB14	AP24	SRASA#
A32	HDSTB0N#	E36	HD22#	N35	HA13#	AD04	DNSTB+	AL18	CKEB2	AP25	SWEA#
A34	HD1#	F01	GDEVSEL	N36	HA15#	AD05	DNSTB–	AL19	MAB9	AP26	ODTA2
A35	HD0#	F02	GTRDY	P30	HA5#	AD34	MDB55	AL20	BAB1	AP27	CSA1#
B03	GD19	F03	GD15	P31	HA11#	AD36	MDB51	AL21	MAB1	AP28	ODTA3
B04	GADSTBS1	F04	GSERR	P32	HA9#	AE02	UPSTB–	AL22	MAB0	AP30	MDA37
B06	GSBA6#	F07	GD31	P33	HA14#	AE03	UPSTB+	AL23	SCASB#	AP31	DQMA4
B07	GSBA7#	F08	GDBIH	P34	HA10#	AE31	MDB52	AL24	ODTB2	AP32	MDA39
B10	GSBA0#	F10	NC	P35	HA16#	AE32	MDB48	AL30	MDB37	AP33	DQSB4–
B20	HD62#	F11	GST2	P36	HA18#	AE33	DQMB6	AL31	MDB33	AP34	DQSB4+
B21	HD58#	F12	GGNT	R31	HA30#	AE34	MDB54	AL32	MDB44	AP35	MDA44
B24	HDSTB3P#	F26	HD45#	R32	HA26#	AE35	MDB50	AL33	MDB40	AP36	MDA40
B26	HD50#	F27	HD39#	R34	HA20#	AE36	MDA51	AL34	MDA47	AR01	MDA1
B27	HD41#	F28	HD33#	R35	HA19#	AF02	VD2	AL35	MDA42	AR02	DQMA0
B28	HDBI2#	F29	HD34#	T31	HA27#	AF03	VD3	AL36	MDA43	AR03	DQSA0+
B29	HD14#	F30	HD11#	T32	HADSTB1#	AF04	DNCMD	AM01	MDB6	AR04	MDA2
B30	HD12#	F31	HD31#	T33	HA17#	AF05	VD7	AM02	MDB7	AR05	MDA3
B31	HDSTB0P#	F32	HD30#	T34	HA24#	AF31	MDB53	AM03	MDB2	AR06	MDA8
B32	HD6#	F34	HD16#	T35	HA23#	AF32	MDB49	AM04	MDB8	AR07	DQSA1+
B33	HD5#	F35	HD19#	T36	HA21#	AF33	DQSB6–	AM05	DQMB1	AR08	MDA11
B34	HD4#	G01	GD13	U02	PE1RX0–	AF34	DQSB6+	AM06	MDB10	AR09	MDB22
B35	HD2#	G02	GPAR	U03	PE1RX0+	AF35	MDA50	AM07	MDA9	AR10	MDA16
B36	HDBI1#	G03	GSTOP	U05	PE1TX0–	AF36	MDA54	AM08	MDB17	AR11	DQSA2–
C01	GD17	G04	GD14	U06	PE1TX0+	AG02	VD6	AM09	DQMB2	AR12	MDA23
C02	GD18	G05	GC#BE1	U30	HA29#	AG03	UPCMD	AM10	MDB18	AR13	MDA28
C03	GD20	G08	GDBIL	U31	HA31#	AG05	VD10	AM11	MDA17	AR14	MDA24
C04	GADSTBF1	G10	NC	U32	HA28#	AG06	VLCOMPP	AM12	MDB25	AR16	MDA30
C05	GD26	G11	NC	U33	HA22#	AG34	DQSA6+	AM13	DQSB3–	AR17	CKEA3
C06	GD28	G26	HD46#	U34	HA25#	AG35	DQSA6–	AM14	MDB27	AR18	BAA2
C07	GSBA3#	G29	HCLK–	U35	MCLKOA–	AH02	VD11	AM15	DQMA3	AR19	MAA11
C09	GSBA5#	G31	HD20#	U36	MCLKOA+	AH03	VD14	AM17	BAB2	AR20	MAA8
C10	GSBA1#	G32	HD18#	V02	PE1COMP	AH04	VD15	AM18	MAB12	AR21	MAA6
C12	GST1	G33	HD17#	V03	PE1TX1–	AH23	ODTB3	AM19	MAB8	AR22	MAA2
C20	HD63#	G34	DEFER#	V04	PE1TX1+	AH24	ODTB1	AM20	MAB11	AR23	MAA10
C21	HD59#	G35	RS2#	V31	MCLKIA+	AH31	MDA52	AM21	MAB4	AR24	BAA0
C22	HD61#	G36	RS0#	V32	MCLKIA–	AH32	MDA53	AM22	MAB2	AR25	CSA2#
C23	HD57#	H01	GD12	V34	MCLKOB–	AH33	MDA55	AM23	CSB2#	AR26	ODTA0
C24	HD55#	H03	GD9	V35	MCLKOB+	AH34	DQMA6	AM24	SWEB#	AR27	MAA13
C25	HD53#	H04	NC	W03	PE1RX1–	AH35	MDA49	AM31	MDB36	AR28	ODTA1
C26	HD43#	H06	GD10	W04	PE1RX1+	AH36	MDA48	AM32	DQMB4	AR30	MDA36
C27	HDSTB2P#	H07	GD11	W07	PECLK–	AJ01	PWROK	AM33	MDA41	AR31	MDA33
C28	HD35#	H09	NC	W08	TCLK	AJ02	PEWAKE#	AM34	DQSA5–	AR32	DQSA4+
C29	HD15#	H11	AGP8XDET#	W30	MDB56	AJ03	SUSST#	AM35	DQSA5+	AR33	MDA34
C30	HD10#	H26	HD47#	W31	DQMB7	AJ04	MDB5	AM36	MDA46	AR34	MDB38
C31	HDBI0#	H27	GVCLK	W32	MDB62	AJ05	MDB4	AN01	MDB13	AR35	MDB35
C32	HD7#	H29	HCLK+	W33	MDB63	AJ12	MDB29	AN03	MDB12	AT02	DQSA0–
C34	HD26#	H31	DPWR#	W34	DFTIN#	AJ19	CKEB3	AN05	DQSB1–	AT03	MDA6
C35	HDSTB1P#	H32	HPCREQ#	W35	TESTIN#	AJ20	MAB5	AN06	MDB15	AT05	MDA13
D01	GIRDY	H34	BPRI#	W36	MEMDET	AJ21	CSB0#	AN08	MDA14	AT06	DQMA1
D02	GD16	H35	HIT#	Y02	PE1REXT	AJ22	CSB3#	AN09	DQSB2–	AT08	MDA10
D03	GC#BE2	H36	HLOCK#	Y03	PE1RX2+	AJ23	MAB13	AN11	MDA22	AT09	MDA21
D04	GC#BE3	J01	GD8	Y04	PE1RX2–	AJ24	CSB1#	AN12	DQSB3+	AT11	DQSA2+
D05	GD27	J02	GC#BE0	Y05	PE1TX2–	AJ32	DQMB5	AN14	MDB31	AT12	MDA18
D06	GD29	J03	GD7	Y06	PE1TX2+	AJ33	MDB43	AN16	MDA27	AT14	MDA25
D07	GSBA2#	J04	GD6	Y07	PECLK+	AJ34	DQSB5+	AN17	CKEA2	AT15	DQSA3+
D10	NC	J05	GD2	Y29	MDB60	AJ35	MDB47	AN19	MAB7	AT16	MDA31
D11	INTR#	J06	GD3	Y30	MDB61	AJ36	MDB42	AN20	MAB6	AT17	CKEA1
D12	GST0	J32	DBSY#	Y31	MDB57	AK01	RESET#	AN22	MAB3	AT19	MAA12
D20	HD48#	J33	BNR#	Y32	DQSB7–	AK02	DQMB0	AN23	BAB0	AT20	MAA7
D22	HD49#	J34	ADS#	Y33	DQSB7+	AK03	MDB1	AN31	MDA38	AT22	MAA3
D23	HD56#	J35	DRDY#	Y34	MDB58	AK05	MDB0	AN32	MDB32	AT23	MAA0
D25	HD51#	K01	GD4	Y35	MDB59	AK06	MDB11	AN34	MDA45	AT25	CSA0#
D26	HD42#	K02	GD5	Y36	MDA59	AK09	MDB20	AN35	DQMA5	AT26	SCASA#
D28	HD36#	K03	GADSTBF0	AA02	VD13	AK12	MDB28	AP01	MDA4	AT28	CSA3#
D29	HD38#	K04	GADSTBS0	AA03	PE1TX3+	AK14	DMCOMP	AP02	MDA0	AT31	MDA32
D32	HD3#	K05	GD1	AA04	PE1TX3–	AK17	CKEB0	AP03	MDA5	AT32	DQSA4–
D33	HD27#	K06	GD0	AA05	PE1RX3+	AK19	CKEB1	AP04	MDA7	AT34	MDA35
D34	HD24#	K35	HITM#	AA06	PE1RX3–	AK20	MAB10	AP05	DQSB1+	AT35	MDB39
D35	HD21#	K36	HTRDY#	AA34	MDA63	AK22	SRASB#	AP06	MDA12	AT36	MDB34
D36	HD23#	L01	NC	AA35	MDA58	AK23	ODTB0	AP07	DQSA1–		
E01	GFRAME	L03	NC	AB02	VD8	AK31	MDB45	AP08	MDA15		
E04	GD23	L04	NC	AB03	VD9	AK32	MDB41	AP09	DQSB2+		

Table 2. Ball List (Listed by Ball Name)

Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball	Ball Name	Ball #	Ball Name	Ball	Ball Name
J34	ADS#	C04	GADSTBF1	T35	HA23#	C27	HDSTB2P#	AT34	MDA35	Y31	MDB57
H11	AGP8XDET#	K04	GADSTBS0	T34	HA24#	E24	HDSTB3N#	AR30	MDA36	Y34	MDB58
AR24	BAA0	B04	GADSTBS1	U34	HA25#	B24	HDSTB3P#	AP30	MDA37	Y35	MDB59
AP23	BAA1	J02	GC#BE0	R32	HA26#	L35	HEDRDY#	AN31	MDA38	Y29	MDB60
AR18	BAA2	G05	GC#BE1	T31	HA27#	H35	HIT#	AP32	MDA39	Y30	MDB61
AN23	BAB0	D03	GC#BE2	U32	HA28#	K35	HITM#	AP36	MDA40	W32	MDB62
AL20	BAB1	D04	GC#BE3	U30	HA29#	H36	HLOCK#	AM33	MDA41	W33	MDB63
AM17	BAB2	K06	GD0	R31	HA30#	H32	HPCREQ#	AL35	MDA42	W36	MEMDET
J33	BNR#	K05	GD1	U31	HA31#	L31	HREQ0#	AL36	MDA43	A06	NC
H34	BPRI#	J05	GD2	N32	HADSTB0#	L30	HREQ1#	AP35	MDA44	D10	NC
L36	BREQ0#	J06	GD3	T32	HADSTB1#	N31	HREQ2#	AN34	MDA45	F10	NC
AP17	CKEA0	K01	GD4	G29	HCLK–	N30	HREQ3#	AM36	MDA46	G10	NC
AT17	CKEA1	K02	GD5	H29	HCLK+	M31	HREQ4#	AL34	MDA47	G11	NC
AN17	CKEA2	J04	GD6	A35	HD0#	K36	HTRDY#	AH36	MDA48	H04	NC
AR17	CKEA3	J03	GD7	A34	HD1#	D11	INTR#	AH35	MDA49	H09	NC
AK17	CKEB0	J01	GD8	B35	HD2#	AT23	MAA0	AF35	MDA50	L01	NC
AK19	CKEB1	H03	GD9	D32	HD3#	AP22	MAA1	AE36	MDA51	L03	NC
AL18	CKEB2	H06	GD10	B34	HD4#	AR22	MAA2	AH31	MDA52	L04	NC
AJ19	CKEB3	H07	GD11	B33	HD5#	AT22	MAA3	AH32	MDA53	AR26	ODTA0
A20	CPURST#	H01	GD12	B32	HD6#	AP21	MAA4	AF36	MDA54	AR28	ODTA1
AT25	CSA0#	G01	GD13	C32	HD7#	AP20	MAA5	AH33	MDA55	AP26	ODTA2
AP27	CSA1#	G04	GD14	A31	HD8#	AR21	MAA6	AC36	MDA56	AP28	ODTA3
AR25	CSA2#	F03	GD15	E30	HD9#	AT20	MAA7	AB32	MDA57	AK23	ODTB0
AT28	CSA3#	D02	GD16	C30	HD10#	AR20	MAA8	AA35	MDA58	AH24	ODTB1
AJ21	CSB0#	C01	GD17	F30	HD11#	AP19	MAA9	Y36	MDA59	AL24	ODTB2
AJ24	CSB1#	C02	GD18	B30	HD12#	AR23	MAA10	AC34	MDA60	AH23	ODTB3
AM23	CSB2#	B03	GD19	A29	HD13#	AR19	MAA11	AC35	MDA61	V02	PE1COMP
AJ22	CSB3#	C03	GD20	B29	HD14#	AT19	MAA12	AB34	MDA62	Y02	PE1REXT
J32	DBSY#	A03	GD21	C29	HD15#	AR27	MAA13	AA34	MDA63	U02	PE1RX0–
G34	DEFER#	A02	GD22	F34	HD16#	AP18	MAA14	AK05	MDB0	U03	PE1RX0+
W34	DFTIN#	E04	GD23	G33	HD17#	AL22	MAB0	AK03	MDB1	W03	PE1RX1–
AK14	DMCOMP	A05	GD24	G32	HD18#	AL21	MAB1	AM03	MDB2	W04	PE1RX1+
AF04	DNCMD	A04	GD25	F35	HD19#	AM22	MAB2	AL04	MDB3	Y04	PE1RX2–
AD05	DNSTB–	C05	GD26	G31	HD20#	AN22	MAB3	AJ05	MDB4	Y03	PE1RX2+
AD04	DNSTB+	D05	GD27	D35	HD21#	AM21	MAB4	AJ04	MDB5	AA06	PE1RX3–
H31	DPWR#	C06	GD28	E36	HD22#	AJ20	MAB5	AM01	MDB6	AA05	PE1RX3+
AR02	DQMA0	D06	GD29	D36	HD23#	AN20	MAB6	AM02	MDB7	U05	PE1TX0–
AT06	DQMA1	E07	GD30	D34	HD24#	AN19	MAB7	AM04	MDB8	U06	PE1TX0+
AP11	DQMA2	F07	GD31	E34	HD25#	AM19	MAB8	AL06	MDB9	V03	PE1TX1–
AM15	DQMA3	F08	GDBIH	C34	HD26#	AL19	MAB9	AM06	MDB10	V04	PE1TX1+
AP31	DQMA4	G08	GDBIL	D33	HD27#	AK20	MAB10	AK06	MDB11	Y05	PE1TX2–
AN35	DQMA5	F01	GDEVSEL	E33	HD28#	AM20	MAB11	AN03	MDB12	Y06	PE1TX2+
AH34	DQMA6	E01	GFRAME	E32	HD29#	AM18	MAB12	AN01	MDB13	AA04	PE1TX3–
AB33	DQMA7	F12	GGNT	F32	HD30#	AJ23	MAB13	AL05	MDB14	AA03	PE1TX3+
AK02	DQMB0	D01	GIRDY	F31	HD31#	AL17	MAB14	AN06	MDB15	W07	PECLK–
AM05	DQMB1	G02	GPAR	E28	HD32#	V32	MCLKIA–	AL08	MDB16	Y07	PECLK+
AM09	DQMB2	A11	GRBF	F28	HD33#	V31	MCLKIA+	AM08	MDB17	AJ02	PEWAKE#
AL13	DQMB3	E12	GREQ	F29	HD34#	U35	MCLKOA–	AM10	MDB18	AJ01	PWROK
AM32	DQMB4	B10	GSBA0#	C28	HD35#	U36	MCLKOA+	AL10	MDB19	AK01	RESET#
AJ32	DQMB5	C10	GSBA1#	D28	HD36#	V34	MCLKOB–	AK09	MDB20	G36	RS0#
AE33	DQMB6	D07	GSBA2#	E29	HD37#	V35	MCLKOB+	AL09	MDB21	L34	RS1#
W31	DQMB7	C07	GSBA3#	D29	HD38#	AP02	MDA0	AR09	MDB22	G35	RS2#
AT02	DQSA0–	A07	GSBA4#	F27	HD39#	AR01	MDA1	AP10	MDB23	AT26	SCASA#
AR03	DQSA0+	C09	GSBA5#	A28	HD40#	AR04	MDA2	AL12	MDB24	AL23	SCASB#
AP07	DQSA1–	B06	GSBA6#	B27	HD41#	AR05	MDA3	AM12	MDB25	AP24	SRASA#
AR07	DQSA1+	B07	GSBA7#	D26	HD42#	AP01	MDA4	AL14	MDB26	AK22	SRASB#
AR11	DQSA2–	A08	GSBSTBF	C26	HD43#	AP03	MDA5	AM14	MDB27	AJ03	SUSST#
AT11	DQSA2+	A09	GSBSTBS	E26	HD44#	AT03	MDA6	AK12	MDB28	AP25	SWEA#
AP15	DQSA3–	F04	GSERR	F26	HD45#	AP04	MDA7	AJ12	MDB29	AM24	SWEB#
AT15	DQSA3+	D12	GST0	G26	HD46#	AR06	MDA8	AP13	MDB30	W08	TCLK
AT32	DQSA4–	C12	GST1	H26	HD47#	AM07	MDA9	AN14	MDB31	W35	TESTIN#
AR32	DQSA4+	F11	GST2	D20	HD48#	AT08	MDA10	AN32	MDB32	AG03	UPCMD
AM34	DQSA5–	G03	GSTOP	D22	HD49#	AR08	MDA11	AL31	MDB33	AE02	UPSTB–
AM35	DQSA5+	F02	GTRDY	B26	HD50#	AP06	MDA12	AT36	MDB34	AE03	UPSTB+
AG35	DQSA6–	H27	GVCLK	D25	HD51#	AT05	MDA13	AR35	MDB35	AD03	VBE#
AG34	DQSA6+	A10	GWBF	A26	HD52#	AN08	MDA14	AM31	MDB36	AD02	VD0
AB36	DQSA7–	L33	HA3#	C25	HD53#	AP08	MDA15	AL30	MDB37	AC05	VD1
AB35	DQSA7+	M34	HA4#	E23	HD54#	AR10	MDA16	AR34	MDB38	AF02	VD2
AL02	DQSB0–	P30	HA5#	C24	HD55#	AM11	MDA17	AT35	MDB39	AF03	VD3
AL03	DQSB0+	M32	HA6#	D23	HD56#	AT12	MDA18	AL33	MDB40	AC03	VD4
AN05	DQSB1–	L32	HA7#	C23	HD57#	AP12	MDA19	AK32	MDB41	AC02	VD5
AP05	DQSB1+	M35	HA8#	B21	HD58#	AL11	MDA20	AJ36	MDB42	AG02	VD6
AN09	DQSB2–	P32	HA9#	C21	HD59#	AT09	MDA21	AJ33	MDB43	AF05	VD7
AP09	DQSB2+	P34	HA10#	E22	HD60#	AN11	MDA22	AL32	MDB44	AB02	VD8
AM13	DQSB3–	P31	HA11#	C22	HD61#	AR12	MDA23	AK31	MDB45	AB03	VD9
AN12	DQSB3+	N34	HA12#	B20	HD62#	AR14	MDA24	AK35	MDB46	AG05	VD10
AP33	DQSB4–	N35	HA13#	C20	HD63#	AT14	MDA25	AJ35	MDB47	AH02	VD11
AP34	DQSB4+	P33	HA14#	C31	HDBI0#	AP16	MDA26	AE32	MDB48	AB05	VD12
AK34	DQSB5–	N36	HA15#	B36	HDBI1#	AN16	MDA27	AF32	MDB49	AA02	VD13
AJ34	DQSB5+	P35	HA16#	B28	HDBI2#	AR13	MDA28	AE35	MDB50	AH03	VD14
AF33	DQSB6–	T33	HA17#	E21	HDBI3#	AP14	MDA29	AD36	MDB51	AH04	VD15
AF34	DQSB6+	P36	HA18#	A32	HDSTB0N#	AR16	MDA30	AE31	MDB52	AG06	VLCOMPP
Y32	DQSB7–	R35	HA19#	B31	HDSTB0P#	AT16	MDA31	AF31	MDB53	AC04	VPAR
Y33	DQSB7+	R34	HA20#	E35	HDSTB1N#	AT31	MDA32	AE34	MDB54		
J35	DRDY#	T36	HA21#	C35	HDSTB1P#	AR31	MDA33	AD34	MDB55		
K03	GADSTBF0	U33	HA22#	E27	HDSTB2N#	AR33	MDA34	W30	MDB56		

Table 3. Power, Ground and Voltage Reference Ball List

Outer Ring Balls (Intermixed with Signal Balls)

AGPVREF[1:0]	:	J09, J11
GTLVREF[1:0]	:	H23, M29
MEMVREF[1:0]	:	AD30, AJ10
VLVREF	:	AE05
VCCA33HCK	:	H28
GNDAHCK	:	G28
VCCA33MCK	:	V29
GNDAMCK	:	W29
VCCA33PE1	:	Y01
GNDAPE1	:	W01
VCCA33PE	:	V06
GNDAPE	:	W06
VCCMEM	:	AF17, AF18, AF19, AF20, AF21, AF22, AF23, AF24, AF25, AF26, AF27, AF28, AF29, AG17, AG18, AG19, AG20, AG21, AG22, AG23, AG24, AG25, AG26, AG27, AG28, AG29, AH17, AH18, AH19, AH20, AH21, AH25, AH26, AH27, AH28, AH29, AJ17, AJ18, AJ25, AJ26, AJ27, AJ28, AJ29, AK18, AK21, AK24, AK25, AK26, AK27, AK28, AK29, AL25, AL26, AL27, AL28, AL29, AM25, AM26, AM27, AM28, AM29, AN18, AN21, AN24, AN25, AN26, AN27, AN28, AN29, AP29, AR29, AT18, AT21, AT24, AT27, AT29
VCC15	:	P18, P19, R17, R18, R21, T16, T17, T20, T21, U16, U19, U20, V14, V15, V18, V19, V22, V23, W13, W14, W17, W18, W21, W22, Y13, Y16, Y17, Y20, Y21, AA08, AA09, AA10, AA13, AA15, AA19, AA20, AB06, AB07, AB08, AB09, AB10, AB11, AB12, AB13, AB14, AB18, AB19, AC06, AC07, AC08, AC09, AC10, AC11, AC12, AC13, AC14, AC16, AC17, AC18, AD06, AD07, AD08, AD09, AD10, AD11, AD12, AD13, AD14, AD16, AD17, AE06, AE07, AE08, AE09, AE10, AE11, AE12, AE13, AE14, AE16, AF06, AF07, AF08, AF09, AF10, AF11, AF12, AF13, AF14, AG07, AG08, AG09, AG10, AG11, AG12, AG13, AH06, AH07, AH08
VCC15VL	:	Y11, Y12, AA11, AA12
VCC33PE	:	R01, R02, R03, R04, R05, R06, R07, R08, R09, R10, R11, T01, T02, T03, T04, T05, T06, T07, T08, T09, T10, T11, U07, U08, U09, U10, U11, V10, V11
VCC15AGP	:	L09, L10, L11, M01, M02, M03, M04, M05, M06, M07, M08, M09, M10, M11, N01, N02, N03, N04, N05, N06, N07, N08, N09, N10, N11, P01, P02, P03, P04, P05, P06, P07, P08, P09, P10, P11
VSUS15	:	AH05
VSUS15PE	:	V01
VTT	:	A14, A15, A16, A17, A18, A19, B14, B15, B16, B17, B18, B19, C14, C15, C16, C17, C18, C19, D14, D15, D16, D17, D18, D19, E14, E15, E16, E17, E18, E19, F14, F15, F16, F17, F18, F19, G15, G16, G17, G18, G19, H16, H17, H18, H19, J17, J18, J19, K17, K18, K19, L17, L18, L19, L20, L21, L22, L23, M18, M19, M20, M21, M22, M23
GND	:	A13, A21, A24, A27, A30, A33, A36, B02, B05, B08, B09, B11, B13, C13, C33, C36, D13, D21, D24, D27, D30, E02, E03, E05, E06, E08, E10, E11, E13, F05, F06, F13, F20, F33, F36, G06, G07, G09, G14, G20, G21, G24, G27, G30, H02, H05, H08, H15, H33, J07, J08, J16, J36, K07, K08, K16, L02, L05, L06, L07, L08, M12, M16, M30, M33, M36, N12, N17, N19, N20, N21, N22, N23, P12, P16, P20, P21, R12, R15, R19, R20, R30, R33, R36, T12, T13, T14, T18, T19, T22, U01, U04, U12, U13, U14, U17, U18, U21, U22, V05, V07, V08, V09, V12, V13, V16, V17, V20, V21, V24, V30, V33, V36, W02, W05, W09, W10, W11, W12, W15, W16, W19, W20, W23, W24, Y08, Y09, Y10, Y14, Y18, Y19, Y22, Y23, AA07, AA17, AA18, AA21, AA22, AA30, AA33, AA36, AB01, AB04, AB16, AB17, AB20, AB21, AC19, AC20, AD18, AD19, AD31, AD33, AD35, AE01, AE04, AE17, AE18, AE19, AE20, AE21, AE22, AE23, AE24, AE25, AE26, AE27, AE28, AE29, AF16, AG04, AG14, AG15, AG16, AG31, AG33, AG36, AH01, AH09, AH10, AH11, AH12, AH13, AH14, AJ06, AJ07, AJ08, AJ09, AK04, AK07, AK10, AK13, AK30, AK33, AK36, AL01, AL15, AM16, AN02, AN04, AN07, AN10, AN13, AN15, AN30, AN33, AN36, AR15, AR36, AT01, AT04, AT07, AT10, AT13, AT30, AT33

Ball Descriptions

CPU Interface Ball Descriptions

CPU Interface			
Signal Name	**Ball #**	**I/O**	**Signal Description**
HA[31:3]#	(see ball lists)	IO	**Host CPU Address Bus.** Connect to the address bus of the host CPU. Inputs during CPU cycles and driven by the PT880 Pro during cache snooping operations.
HADSTB [1:0]#	T32, N32	IO	**Host CPU Address Strobe.** Source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0]# at a 2x transfer rate. HADSTB1# is the strobe for HA[31:17]# and HADSTB0# is the strobe for HA[16:3] and HREQ[4:0]#.
HD[63:0]#	(see ball lists)	IO	**Host CPU Data.** These signals are connected to the CPU data bus.
DPWR#	H31	O	**Data Bus Power Reduction.** Request to reduce power on the mobile CPU data bus input buffer. Connect to mobile CPU if used.
HDBI[3:0]#	E21, B28, B36, C31	IO	**Host CPU Dynamic Bus Inversion.** Driven along with HD[63:0]# to indicate if the associated signals are inverted or not. Used to limit the number of simultaneously switching signals to 8 for the associated 16-bit data ball group (HDBI3# for HD[63:48]#, HDBI2# for HD[47:32]#, HDBI1# for HD[31:16]#, and HDBI0# for HD[15:0]#). HDBIn# is asserted such that the number of data bits driven low for the corresponding group does not exceed 8.
HDSTB [3:0]P# **HDSTB [3:0]N#**	B24, C27, C35, B31 E24, E27, E35, A32	IO	**Host CPU Differential Data Strobes.** Source synchronous strobes used to transfer HD[63:0]# & HDBI[3:0]# at a 4x transfer rate. HDSTB3P# / HDSTB3N# are the strobes for HD[63:48]# & HDBI3#; HDSTB2P# / HDSTB2N# are the strobes for HD[47:32]# & HDBI2#; HDSTB1P# / HDSTB1N# are the strobes for HD[31:16]# & HDBI1#; and HDSTB0P# / HDSTB0N# are the strobes for HD[15:0]# & HDBI0#.
ADS#	J34	IO	**Address Strobe.** The CPU asserts ADS# in T1 of the CPU bus cycle.
DBSY#	J32	IO	**Data Bus Busy.** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DRDY#	J35	IO	**Data Ready.** Asserted for each cycle that data is transferred.
HEDRDY#	L35	O	**Early Data Ready.** Indicates that data will be returning on the bus exactly two clocks after assertion. Connect to host CPU if it implements this function, otherwise leave unconnected.
HREQ[4:0]#	M31, N30, N31, L30, L31	IO	**Request Command.** Asserted during both clocks of the request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.
HTRDY#	K36	IO	**Host Target Ready.** Indicates that the target of the processor transaction is able to enter the data transfer phase.
RS[2:0]#	G35, L34, G36	IO	**Response Signals.** Indicates the type of response per the table below: RS[2:0]# — Response type 000 — Idle State 001 — Retry Response 010 — Defer Response 011 — Reserved 100 — Hard Failure 101 — Normal Without Data 110 — Implicit Writeback 111 — Normal With Data

Note: Clocking of the CPU interface is performed with HCLK+ and HCLK– (see clock ball description group).

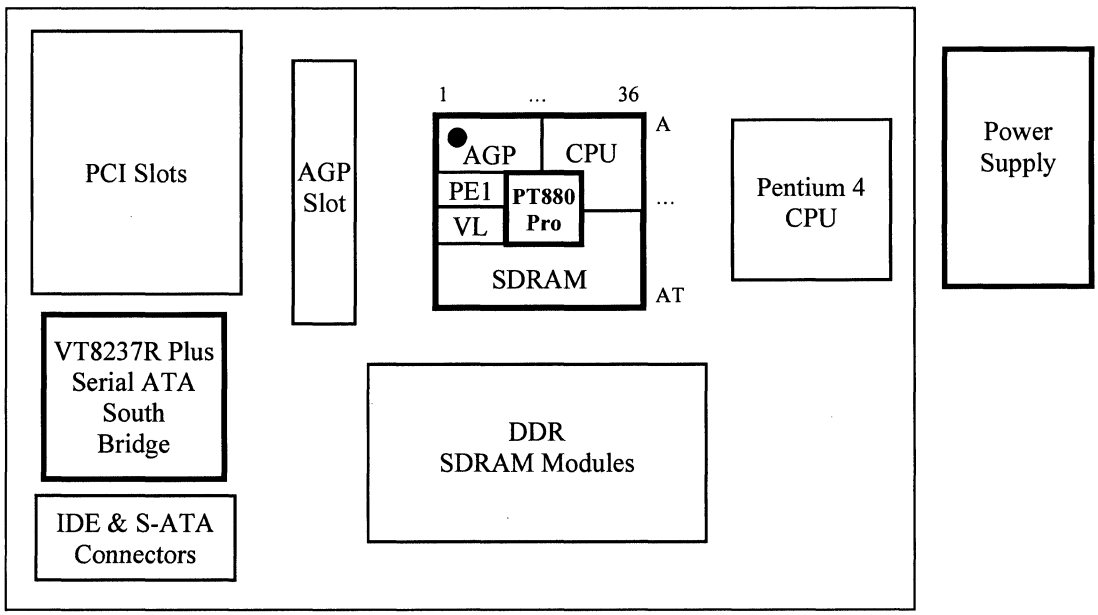
Note: Internal pullup resistors are provided on all AGTL+ interface balls. If the CPU does not have internal pull-ups, these North Bridge internal pull-ups may be enabled to allow the interface to meet AGTL+ bus interface specifications (see VD3 strap).

Note: I/O pads for the above balls are powered by VTT.

CPU Interface (continued)			
Signal Name	**Ball #**	**I/O**	**Signal Description**
HIT#	H35	IO	**Hit.** Indicates that a caching agent holds an unmodified version of the requested line. Also driven in conjunction with HITM# by the target to extend the snoop window.
HITM#	K35	I	**Hit Modified.** Asserted by the CPU to indicate that the address is modified in the L1 cache and needs to be written back.
HLOCK#	H36	I	**Host Lock.** All CPU cycles sampled with the assertion of HLOCK# and ADS# until the negation of HLOCK# must be atomic.
HPCREQ#	H32	I	**PreCharge Request.** The CPU asserts this signal to indicate that the next memory access will be off-page. Connect to ground if the CPU does not implement this function.
BREQ0#	L36	O	**Bus Request.** Bus request output to CPU.
BPRI#	H34	IO	**Priority Agent Bus Request.** The owner of this signal will always be the next bus owner. This signal has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions unless the HLOCK# signal is asserted. The PT880 Pro drives this signal to gain control of the processor bus.
BNR#	J33	IO	**Block Next Request.** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
DEFER#	G34	IO	**Defer.** The PT880 Pro uses a dynamic deferring policy to optimize system performance. The PT880 Pro also uses the DEFER# signal to indicate a processor retry response.
CPURST#	A20	O	**CPU Reset.** Reset output to CPU. External pullup and filter capacitor to ground should be provided per CPU manufacturer's recommendations.

Note: I/O pads for the above balls are powered by VTT.

The ballouts were defined assuming the ATX PCB layout model shown below (and general ball layout shown) as a guide for PCB component placement. Other PCB layouts (AT, LPX, and NLX) were also considered and can typically follow the same general component placement.



Ultra V-Link Ball Descriptions

Ultra V-Link Interface			
Signal Name	**Ball #**	**I/O**	**Signal Description**
VD15,	AH04	IO	**Data Bus.** During system initialization, VD[7:0] are used to transmit strap information from the South Bridge (the straps are not on the VD balls but are on the indicated balls of the South Bridge chip). Check the strap ball table for details.
VD14,	AH03	IO	
VD13,	AA02	IO	
VD12,	AB05	IO	
VD11,	AH02	IO	
VD10,	AG05	IO	
VD9,	AB03	IO	
VD8,	AB02	IO	
VD7,	AF05	IO	
VD6,	AG02	IO	
VD5,	AC02	IO	
VD4,	AC03	IO	
VD3,	AF03	IO	
VD2,	AF02	IO	
VD1,	AC05	IO	
VD0	AD02	IO	
VPAR	AC04	IO	**Parity.**
VBE#	AD03	IO	**Byte Enable.**
UPCMD	AG03	I	**Command from Client (South Bridge) to Host (North Bridge).**
UPSTB+	AE03	I	**Strobe from Client to Host.**
UPSTB–	AE02	I	**Complement Strobe from Client to Host.**
DNCMD	AF04	O	**Command from Host (North Bridge) to Client (South Bridge).**
DNSTB+	AD04	O	**Strobe from Host to Client.**
DNSTB–	AD05	O	**Complement Strobe from Host to Client.**

Note: I/O pads for all balls in the table above are powered by VCC15VL. Input voltage levels are referenced to VLVREF.

DDR / DDER2 SDRAM Memory Controller Ball Descriptions

DDR DRAM Interface – "A" Data			
Signal Name	**Ball #**	**I/O**	**Signal Description**
MDA[63:0]	(see ball lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMA[7:0]	AB33, AH34, AN35, AP31, AM15, AP11, AT06, AR02	O / IO	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSA[7:0]+ **DQSA[7:0]–**	AB35, AG34, AM35, AR32, AT15, AT11, AR07, AR03 AB36, AG35, AM34, AT32, AP15, AR11, AP07, AT02	IO	**DDR / DDR2 Memory Data Strobes.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0. DQSA[7:0]– are used only for DDR2 differential data strobe.
CSA[3:0]#	AT28, AR25, AP27, AT25	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEA[3:0]	AR17, AN17, AT17, AP17	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.
ODTA[3:0]	AP28, AP26, AR28, AR26	O	**On Die Termination.** Enables termination resistance internal to the DDR2 SDRAM. Not used in DDR mode.

DDR DRAM Interface – "B" Data			
Signal Name	**Ball #**	**I/O**	**Signal Description**
MDB[63:0]	(see ball lists)	IO	**Memory Data.** These signals are connected to the DRAM data bus. Output drive strength may be set by Device 0 Function 3 RxE2.
DQMB[7:0]	W31, AE33, AJ32, AM32, AL13, AM09, AM05, AK02	O / IO	**Data Mask.** Data mask of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE2.
DQSB[7:0]+ **DQSB[7:0]–**	Y33, AF34, AJ34, AP34, AN12, AP09, AP05, AL03 Y32, AF33, AK34, AP33, AM13, AN09, AN05, AL02	IO	**DDR / DDR2 Memory Data Strobes.** Data strobe of each byte lane. Output drive strength may be set by Device 0 Function 3 RxE0. DQSB[7:0]– is used only for DDR2 differential data strobe.
CSB[3:0]#	AJ22, AM23, AJ24, AJ21	O	**Chip Select.** Chip select of each bank. Output drive strength may be set by Device 0 Function 3 RxE4.
CKEB[3:0]	AJ19, AL18, AK19, AK17	O	**Clock Enables.** Clock enables for each DRAM bank for powering down the SDRAM or clock control for reducing power usage and for reducing heat / temperature in high-speed memory systems.
ODTB[3:0]	AH23, AL24, AH24, AK23	O	**On Die Termination.** Enables termination resistance internal to the DDR2 SDRAM. Not used in DDR mode.

DDR DRAM Interface – Address			
Signal Name	**Ball #**	**I/O**	**Signal Description**
MAA[14:0], **MAB[14:0]**	(see ball lists)	O	**Memory Address A and B.** Two sets for additional drive. Output drive strength set via Function 3 RxE8 (MAA) and RxEA (MAB).
BAA[2:0], **BAB[2:0]**	AR18, AP23, AR24 AM17, AL20, AN23	O	**Bank Address A and B.** Two sets for additional drive. Output drive strength may be set by Device 0 Function 3 RxE8 (BAA) and RxEA (BAB).
SRASA#, SCASA#, SWEA#, **SRASB#, SCASB#, SWEB#**	AP24, AT26, AP25 AK22, AL23, AM24	O	**Row Address, Column Address and Write Enable Command Indicators A and B.** Two sets for additional drive. Output drive strength set via Function 3 Rx E8(A) & EA(B).

Note: I/O pads for all balls on this page are powered by VCCMEM. MD / DQS input voltage levels are referenced to MEMVREF.

Accelerated Graphics Port Ball Descriptions

AGP Bus Interface			
Signal Name	**Ball #**	**I/O**	**Signal Description**
GD31 **GD30** **GD29** **GD28** **GD27** **GD26** **GD25** **GD24** **GD23** **GD22** **GD21** **GD20** **GD19** **GD18** **GD17** **GD16** **GD15** **GD14** **GD13** **GD12** **GD11** **GD10** **GD9** **GD8** **GD7** **GD6** **GD5** **GD4** **GD3** **GD2** **GD1** **GD0**	F07 E07 D06 C06 D05 C05 A04 A05 E04 A02 A03 C03 B03 C02 C01 D02 F03 G04 G01 H01 H07 H06 H03 J01 J03 J04 K02 K01 J06 J05 K05 K06	IO	**Address / Data Bus.** Address is driven with GADSTB assertion.
GC#BE[3:0]	D04 D03 G05 J02	IO	**Command / Byte Enable.** For AGP cycles these balls provide command information driven by the master (graphics controller). These balls provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to "0000" during the return of AGP read data.
GPAR	G02	IO	**AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0].
GDBIH **GDBIL**	F08 G08	IO	**Dynamic Bus Inversion High / Low.** Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-ball group.
GADSTBF0, **GADSTBS0**	K03 K04	IO	**Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GADSTBF0 is "First" strobe, GADSTBS0 is "Second" strobe.
GADSTBF1, **GADSTBS1**	C04 B04	IO	**Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GADSTBF1 is "First" strobe, GADSTBS1 is "Second" strobe.
GFRAME	E01	IO	**Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
GDEVSEL	F01	IO	**Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles.

Note: I/O pads for all balls on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.

AGP Bus Interface – continued			
Signal Name	**Ball #**	**I/O**	**Signal Description**
GIRDY	D01	IO	**Initiator Ready.** For write cycles, assertion indicates that the master is ready to provide all write data for the current transaction. Once asserted, the master is not allowed to insert wait states. For read cycles, assertion indicates that the master is ready to transfer a subsequent block of read data. The master is never allowed to insert a wait state during the initial block of a read transaction, however it may insert wait states after each block transfers.
GTRDY	F02	IO	**Target Ready.** For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions.
AGP8XDET#	H11	I	**AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode
GRBF	A11	I	**Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When asserted, the North Bridge will not return low priority read data to the graphics controller.
GWBF	A104	I	**Write Buffer Full.**
GSBA7#, **GSBA6#,** **GSBA5#,** **GSBA4#,** **GSBA3#,** **GSBA2#,** **GSBA1#,** **GSBA0#**	B07 B06 C09 A07 C07 D07 C10 B10	I	**Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge).
GSBSTBF, **GSBSTBS**	A08 A09	I	**Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. GSBSTBF is "First" strobe and GSBSTBS is "Second" strobe.
GST2, **GST1,** **GST0**	F11 C12 D12	O	**Status.** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT is asserted. GST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller). (i.□. Indicates that a previously requested low priority read or flush data is being returned to the master (graphics controller). (i.□. Indicates that previously requested high priority read data is being returned to the master. (i.□. Indicates that the master is to provide low priority write data for a previously enqueued write command. (i.□. Indicates that the master is to provide high priority write data for a previously enqueued write command. (i.□. Reserved. (arbiter must not issue, may be defined in the future). (i.□. Reserved. (arbiter must not issue, may be defined in the future). (i.□. Reserved. (arbiter must not issue, may be defined in the future). 111 Indicates that the master (graphics controller) has been given permission to start a bus transaction.
GREQ	E12	I	**Request.** Master (graphics controller) request for use of the AGP bus.
GGNT	F12	O	**Grant.** Permission is given to the master (graphics controller) to use the AGP bus.
GSERR	F04	IO	**System Error.**
GSTOP	G03	IO	**Stop.** Asserted by the target to request the master to stop the current transaction.

Note: I/O pads for all balls on this page are powered by VCC15AGP. Input voltage levels are referenced to AGPVREF.
Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses).

PCI Express Ball Descriptions

PCI Express (PCIe) Port			
Signal Name	**Ball #**	**I/O**	**Signal Description**
PE1RX3+ **PE1RX3–**	AA05 AA06	I	**PCI Express Port Receive Data 3.**
PE1RX2+ **PE1RX2–**	Y03 Y04	I	**PCI Express Port Receive Data 2.**
PE1RX1+ **PE1RX1–**	W04 W03	I	**PCI Express Port Receive Data 1.**
PE1RX0+ **PE1RX0–**	U03 U02	I	**PCI Express Port Receive Data 0.**
PE1TX3+ **PE1TX3–**	AA03 AA04	O	**PCI Express Port Transmit Data 3.**
PE1TX2+ **PE1TX2–**	Y06 Y05	O	**PCI Express Port Transmit Data 2.**
PE1TX1+ **PE1TX1–**	V04 V03	O	**PCI Express Port Transmit Data 1.**
PE1TX0+ **PE1TX0–**	U06 U05	O	**PCI Express Port Transmit Data 0.**

Note: I/O pads for all balls in the table above are powered by VCC33PE.

Clock Ball Descriptions

Clock				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
HCLK+ **HCLK–**	H29 G29	I	**Host Clock.** These balls receive the host CPU clock (100 / 133 / 166 / 200 MHz) used by all PT880 Pro logic that is in the host CPU domain.	**VTT**
PECLK+ **PECLK–**	Y07 W07	I	**PCI Express Clock.** These balls receive the 100 MHz clock used by the internal PCI Express logic. Multiplied up to 2.5 GHz on-chip for use by the integrated PCI Express PHY to transmit / receive data.	**VCC33PE**
VGCLK	H27	I	**AGP Clock.** This ball receives the 66 MHz clock used by the internal AGP logic.	**VCC33PE**
MCLKOA+ **MCLKOA–**	U36 U35	O	**Memory (SDRAM) Clock A.** Output from internal clock generator to the external clock buffer (if needed for fanout) for memory interface "A".	**VCCMEM**
MCLKIA+ **MCLKIA–**	V31 V32	I	**Memory (SDRAM) Clock Feedback A.** Input from MCLKOA.	**VCCMEM**
MCLKOB+ **MCLKOB–**	V35 V34	O	**Memory (SDRAM) Clock B.** Output from internal clock generator to the external clock buffer (if needed for fanout) for memory interface "B".	**VCCMEM**

Reset, Power Control, General Purpose I/O, Interrupt and Test Ball Descriptions

Reset, Power Control, General Purpose I/O, Interrupt and Test				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
RESET#	AK01	I	**Reset.** Input from the South Bridge chip. When asserted, this signal resets the PT880 Pro and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options.	**VSUS15**
PWROK	AJ01	I	**Power OK.** From Power Good circuitry. Also connected to South Bridge.	**VSUS15**
SUSST#	AJ03	I	**Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable.	**VSUS15**
PEWAKE#	AJ02	OD	**PCI Express Wake.** Indicates that a system wake event has occurred on the PCI Express bus. Used to waken the chip from deep sleep mode (S3 / S4 / S5 states). Wire-OR with other system WAKE# signals (including PEWAKE# on the PCI Express bus connector) and connect to the South Bridge PME input. This ball has a weak internal pullup to VSUS15 but the system should also provide an external 10K ohm pullup to VSUS33.	**VSUS15**
INTR#	D11	OD	**PCI Express Interrupt.** Connect to South Bridge interrupt input to indicate that an interrupt condition was detected on PCI Express bus or the internal APIC. This ball has a weak internal pullup in AGP 2.0 mode only (disabled in AGP 3.0 mode).	**VCCAGP**
MEMDET	W36	I	**Memory Detect.** Must be strapped low / high for DDR / DDR2.	**VCCMEM**
TCLK	W08	I	**Test Clock.** This ball is used for testing. It is internally pulled high so may be left unconnected for all board designs.	**VCC33PE**
TESTIN#	W35	I	**Test In.** This ball is used for testing and must be connected to VCCMEM through a 1K-4.7K ohm resistor for all board designs.	**VCCMEM**
DFTIN#	W34	I	**DFT In.** This ball is used for testing and must be connected to VCCMEM through a 1K-4.7K ohm resistor for all board designs.	**VCCMEM**

Compensation and Reference Voltage Ball Descriptions

Compensation				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
DMCOMP	AK14	AI	**SDRAM Compensation.** Connect a 275 Ω 1% resistor to ground.	**VCCMEM**
PE1COMP	V02	AI	**PCI Express Port 0 Compensation.** Connect a 250 Ω 1% resistor to ground to calibrate 50 Ω termination.	**VCC33PE**
PE1REXT	Y02	AI	**PCI Express Port 1. External Resistor.** See Design Guide.	**VCC33PE**
VLCOMPP	AG06	AI	**V-Link Bus Compensation.** Connect a 360 Ω 1% resistor to ground.	**VCC15VL**

Reference Voltages				
Signal Name	**Ball #**	**I/O**	**Signal Description**	**Power Plane**
GTLVREF[1:0]	H23, M29	P	**Host CPU Interface AGTL+ Voltage Reference.** 2/3 VTT ±2% typically derived using a resistive voltage divider. See Design Guide.	**VTT**
MEMVREF[1:0]	AD30, AJ10	P	**Memory Voltage Reference.** 0.5 VCCMEM ±2% typically derived using a resistive voltage divider. See Design Guide.	**VCCMEM**
VLVREF	AE05	P	**V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider. See PT880 Pro Design Guide.	**VCC15VL**
AGPVREF[1:0]	J09, J11	P	**AGP Voltage Reference.** ½ VCC15AGP (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCC15AGP (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.	**VCC15AGP**

Analog Power Ball Descriptions

Analog Power / Ground			
Signal Name	**Ball #**	**I/O**	**Signal Description**
VCCA33HCK	H28	P	**Power for Host CPU Clock PLL** (3.3V ±5%). 400 MHz for CPU / DRAM frequencies of multiples of 100, 133, and 200 MHz.
GNDAHCK	G28	P	**Ground for Host CPU Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33MCK	V29	P	**Power for Memory Clock PLL** (3.3V ±5%)
GNDAMCK	W29	P	**Ground for Memory Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33PE1	Y01	P	**Power for PCI Express Port Clock PLL** (3.3V ±5%). For PE1[3:0].
GNDAPE1	W01	P	**Ground for PCI Express Port Clock PLL.** Connect to main ground plane through a ferrite bead.
VCCA33PE	V06	P	**Power for PCI Express Clock PLL** (3.3V ±5%). For PECLK clock synthesizer.
GNDAPE	W06	P	**Ground for PCI Express Clock PLL.** Connect to main ground plane through a ferrite bead.

Digital Power Ball Descriptions

Digital Power / Ground			
Signal Name	**Ball #**	**I/O**	**Signal Description**
VTT	(see ball lists)	P	**Power** for **CPU I/O Interface Logic.** Typical 1.65V (CPU dependent).
VCCMEM	(see ball lists)	P	**Power** for **Memory I/O Interface Logic.** 1.8 / 2.5V ±5%.
VCC15VL	Y11, Y12, AA11, AA12	P	**Power** for **V-Link I/O Interface Logic.** 1.5V ±5%
VCC15AGP	(see ball lists)	P	**Power** for **AGP Bus I/O Interface Logic.** 1.5V ±5%
VCC33PE	(see ball lists)	P	**Power** for **PCIe I/O Interface Logic.** 3.3V ±5%
VCC15	(see ball lists)	P	**Power** for **Internal Logic.** 1.5V ±5%
VSUS15	AH05	P	**Suspend Power.** 1.5V ±5%. For RESET#, PWROK, SUSST# and PEWAKE# balls and associated internal circuitry.
VSUS15PE	V01	P	**PCI Express Suspend Power.** 1.5V ±5%.
GND	(see ball lists)	P	**Digital Ground.** Connect to main ground plane.

Strap Ball Descriptions

Strap Balls (External pullup / pulldown straps are required to select "H" / "L")				
Signal	**Actual Strap Ball**	**Function**	**Description**	**Status Bit**
VD7	**VT8235M-CD,CE:** SDCS3# **VT8237R Plus:** PDCS3#	V-Link Compensation Select	L: Auto Mode (Use VLCOMP Resistor) H: Manual Mode (Use internal default setting) VD7 is sampled during system initialization; the actual strapping ball is located on the South Bridge chip. Default Setting: Manual Mode	F7 RxB4[0]
VD6	**VT8235M-CD,CE:** SDA2 **VT8237R Plus:** PDA2	Auto-Configure (ROMSIP)	L: Disable H: Enable VD6 is sampled during system initialization; the actual strapping ball is located on the South Bridge chip. Default Setting: Enable	F2 Rx76[2]
VD5	**VT8235M-CDCE:** SDA1 **VT8237R Plus:** PDA1	V-Link 4X Vref Select	L: 0.9V for 0.22u SB Core Power +2.5V (for VT8237R Plus) H: 0.75V for 0.15u SB Core Power +1.5V (for VT8251) VD5 is sampled during system initialization; the actual strapping ball is located on the South Bridge chip.	F7 RxB4[4]
VD3	**VT8235M-CD:** SA19 **VT8235M-CE:** Strap_VD3 **VT8237R Plus:** GPIOD	Internal AGTL+ Pullups	L: Enable H: Disable VD3 is sampled during system initialization; the actual strapping ball is located on the South Bridge chip. Default Setting: Enable	F2 Rx52[5]
VD2	**VT8235M-CD:** SA18 **VT8235M-CE:** Strap_VD2 **VT8237R Plus:** GPIOB	IOQ Depth	L: 12-Level deep H: 1-Level deep VD2 is sampled during system initialization; the actual strapping ball is located on the South Bridge chip. Default Setting: 12-Level deep	F2 Rx50[7]
VD4, VD1, VD0	**VT8235M-CD:** SDA0, SA17, SA16 **VT8235M-CE:** SDA0, Strap_VD1, Strap_VD0 **VT8237R Plus:** PDA0, GPIOA, GPIOC	FSB Frequency	LLL: 100 MHz LLH: 133 MHz LHL: 200 MHz LHH: 166 MHz HLL: -reserved- HLH: -reserved- HHL: -reserved- HHH: Auto VD4, VD1 and VD0 are sampled during system initialization; the actual strapping balls are located on the South Bridge chip.	F2 Rx54[7:5]

REGISTER OVERVIEW

In the register descriptions, column "Default" indicates the default value of register bit(s). While column "Attribute" indicates access type of register bit(s).

Abbreviation

Attribute definitions are

RW:	Read / Write.
RO:	Read Only.
RZ:	Read as Zero.
R1:	Read as 1.
W1:	Write Once then Read Only after that.
W1C:	Write of "1" clears bit to zero.
ROS:	Sticky-Read Only. Registers will not be set or altered by hot reset.
RWS:	Sticky-Read/Write. Registers will not be set or altered by hot reset.
RW1CS:	Sticky-Write-1-to-Clear. Registers will not be set or altered by hot reset.
IW:	Ignore Write.
MW:	Must Write back what is read.
XW:	Backdoor Write.
"—":	Reserved (essentially the same as RO).

Bit default value indicated as "**dip**" means the default value is set by dip switch or strapping.

There are three PCI devices, device 0, device 1, device 2 and up to 10 PCI functions are implemented in this chip. To specifically identify a PCI function, the following abbreviations will be applied in subsequent sections.

D0F0: Device 0, Function0 - AGP and Host Control

D0F1: Device 0, Function1 - Error Reporting

D0F2: Device 0, Function2 - Host Bus Control

D0F3: Device 0, Function3 - DRAM Bus Control

D0F4: Device 0, Function4 - Power Management Control

D0F5: Device 0, Function5 - APIC and Central Traffic Control

D0F6: Device0, Function 6 - Scratch Registers

D0F7: Device 0, Function7 - V-Link Control

D1F0: Device 1, Function0 - PCI-to-PCI Bridge - PCI2

D2F0: Device 2, Function0 - PCI-to-PCI Bridge - PCI Express Root Port (x4 with options of x2 and x1 Line Width)

REGISTER DESCRIPTIONS

Miscellaneous I/O

I/O Port Address: 22h
PCI Arbiter Disable **Default Value: 00h**

Bit(s)	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**PCI2 Arbiter Control** 0: Enable PCI2 Bus Arbiter 1: Disable PCI2 Bus Arbiter
0	RW	0	**PCI Arbiter Control** 0: Enable PCI Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

All north bridge's PCI space registers are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h
PCI Configuration Address **Default Value: 0000 0000h**

Bit(s)	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disabled 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: CFF-CFCh
PCI Configuration Data **Default Value: 0000 0000h**

Bit(s)	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note. Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

Device 0 Function 0 (D0F0): Host Controller

Device 0 Function 0, a host controller, is connected to the PCI bus through AD11 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0.

Header Registers (0-3Fh)

Offset Address: 1-0h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 3-2h (D0F0)

Device ID **Default Value: 0308h**

Bit	Attribute	Default	Description
15:0	RO	0308h	**Device ID Code**

Offset Address: 5-4h (D0F0)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description	Mnemonic
15:10	—	0	**Reserved**	
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Disable)	
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)	
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)	
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors	**RPTYERR**
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)	
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)	
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)	
2	RO	1	**PCI Master Function** Hardwired to 1 (May behave as a bus master)	
1	RO	1	**Memory Space Access** Hardwired to 1 (Responds to memory space access)	
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)	

Offset Address: 7-6h (D0F0)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detect Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR#)**
13	RW1C	0	**Set when terminated with Master-Abort, except special cycle** 0: No abort received 1: Transaction aborted by the master
12	RW1C	0	**Set when received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set when signaled a Target-Abort** NB never signals Target Abort
10:9	RO	01	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Set when set or observed SERR# and Parity Error** (see RPTYERR (Rx04[6]) for details) 0: Disable 1: Enable
7	RO	0	**Capable of Accepting fast back-to-back as a target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1	**Support New Capability List**
3:0	—	0	**Reserved**

Offset Address: 8h (D0F0)
Revision ID **Default Value: 0nh**

Bit	Attribute	Default	Description
7:0	RO	0nh	**North Bridge Chip Revision Code**

Offset Address: 0B-9h (D0F0)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Dh (D0F0)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:3	RW	0	**PCI Bus Time Slice for CPU as a Master (in Unit of PCI clocks)**	**MLT[7:3]**
2:0	RO	0	**Reserved** MLT[2:1] is programmable; however, it's read as 0	**MLT[2:0]**

Offset Address: 0Eh (D0F0)
Header Type **Default Value: —**

Bit	Attribute	Default	Description
7	RO	—	**Multi-Function Device** 0 if MFUNC (Rx4F[0], the multiple function control bit) is set to 0 1 if MFUNC is set to 1
6:0	RO	0	**Reserved**

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 13-10h (D0F0)
Graphic Aperture Base Configuration **Default Value: 0000 0008h**

Bit	Attribute	Default	Description	Mnemonic
31:22	RW	0	**Programmable Base Address** These bits behave as if hardwired to 0 if GTSZ (Rx94[11:0]) is set to 0. See the following table for details. (Note: this range is defined as prefetchable)	GTBSA[31:22]
21:4	—	0	**Reserved—Hardwired to 0**	—
3	RO	1	**Prefetchable** 0: Non-prefetchable (if RGHDR_A (Rx48[0]) is 0) 1: Prefetchable	—
2:1	RO	0	**Type** Indicates that the address range is in the 32-bit address space	—
0	RO	0	**Memory Space** Indicates that the address range is in the memory address space.	—

Table 4. Graphics Aperture Base Address Table

Aperture Base Rx10[31:22]	31	30	29	28			27	26	25	24	23	22	Aperture Size
Aperture Size Rx94[11:0]	11	10	9	8	7	6	5	4	3	2	1	0	
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	RW	4M
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	RW	0	8M
	RW	RW	RW	RW	0	0	RW	RW	RW	RW	0	0	16M
	RW	RW	RW	RW	0	0	RW	RW	RW	0	0	0	32M
	RW	RW	RW	RW	0	0	RW	RW	0	0	0	0	64M
	RW	RW	RW	RW	0	0	RW	0	0	0	0	0	128M
	RW	RW	RW	RW	0	0	0	0	0	0	0	0	256M
	RW	RW	RW	0	0	0	0	0	0	0	0	0	512M
	RW	RW	0	0	0	0	0	0	0	0	0	0	1G
	RW	0	0	0	0	0	0	0	0	0	0	0	2G –Max Size
	0	0	0	0	0	0	0	0	0	0	0	0	4G

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 37-34h (D0F0)
Capability Pointer **Default Value: 0000 0080h**

Bit	Attribute	Default	Description
31:0	RO	80h	**AGP Capability List Pointer** An offset address from the start of the configuration space

If RGHDR_A (Rx48[0]) = 1:

RX34	RX80	RX50	
80	50	NULL	RX34 -> RX80 AGP/AGP8X -> RX50 PMU ->NULL

If RGHDR_A (Rx48[0]) = 0:

RX34	RX50	
50	NULL	RX34 -> RX50 PMU -> NULL

AGP Drive Control (40-48h)

Offset Address: 40h (D0F0)
AGP Pad Compensation Control / Status **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**AGP4X Strobe's Reference Voltage** 0: Strobe signals do not use AGPVREF as input reference voltage (i.e. STB VREF is STB# and vise versa). 1: Strobe signals use AGPVREF as input reference voltage. (Note: This bit is valid only in 4x and 8x mode, otherwise always use AGPVREF as strobe signals)
6	RW	0	**AGP4X Strobe and GD Pad Driving Strength Control** 0: Driving strength is set to compensation circuit defaults 1: Driving strength is controlled by Rx 41[7:0]
5:3	RO	—	**AGP Compensation Circuit N Control Output**
2:0	RO	—	**AGP Compensation Circuit P Control Output**

Offset Address: 41h (D0F0)
AGP Driving Strength Control **Default Value: 63h**

Bit	Attribute	Default	Description
7:4	RW	6h	**AGP Output Buffer Driving Strength N Control**
3:0	RW	3h	**AGP Output Buffer Driving Strength P Control**

Offset Address: 42h (D0F0)
AGP Pad Driving and Delay Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**GD / GADSTBx / GC#BE and GSBSTBx / GSBA# Pad Control** GSBSTBx, GSBA# — GD, GC#BE, GADSTBx 0 — No Cap — No Cap 1 — Cap — Cap
6:5	RW	00	**GD, GC#BE Receive Strobe Delay for the First 16 Bits** 00: Delay by –150 ps — 01: No delay 10: Delay by 150 ps — 11: Delay by 300 ps
4	RW	0	**GD[31:16] Output Staggered Delay (1 ns)** 0: No delay — 1: GD[31:16] is delayed by 1 ns
3	RW	1	**GD, GADSTBx Slew Rate Control** 0: Disable — 1: Enable
2	RW	0	**GSBA Receive Strobe Delay** 0: No Delay — 1: Delay by 1 ns
1:0	RW	00	**GADSTBx Output Delay for the First 16 Bits** 00: No delay — 01: Delay by 150 ps 10: Delay by 300 ps — 11: Delay by 450 ps Note: GADSTB1 and GADSTB1# will be delayed 1 ns more if RGDLY (bit-4) is set to 1..

Offset Address: 43h (D0F0)
AGP Strobe Drive Strength Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Strobe Output Buffer Driving Strength N Control**
3:0	RW	0	**AGP Strobe Output Buffer Driving Strength P Control**

Offset Address: 44h (D0F0)
AGP GSBA Pads Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**GD and GC#BE Strobe Delay for Receiving for the First 16 Bits**
6:4	RW	00	**GSBA Pads Control Signals for Strobe**
3	—	0	**Reserved**
2:0	RW	0	**GSBA Pads Control**

Offset Address: 48h (D0F0)
AGP Header Presentation **Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	
0	RW	1	**AGP Header Presented in Device 0** 0: Disable 1: Enable If this bit is set to 0, Rx13-10 will be fixed at 0, and the Rx80 will be taken off from the capability list directed by Rx34 of device 0.	RGHDR_A

Miscellaneous Control (4A-

Offset Address: 4Ah (D0F0)
AGP Hardware Support I – VPX Mode **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:0	RW	1Fh	**AGP Request Queue Size** The value in this register is valid and effective if RAGPHW (Rx4D[1]) is set to 1.

Offset Address: 4Bh (D0F0)
AGP Hardware Support II – VPX Mode **Default Value: C4h**

This register is used to re-configure the AGP controller. To change the operating mode of the AGP controller, Rx4D[1] must be set to 1.

Bit	Attribute	Default	Description
7	RW	1	**AGP SBA Mode Enable** 0: Disable 1: Enable
6	RW	1	**AGP Enable** 0: Disable 1: Enable
5	RO	0	**Set by Strap Ball AGP8XDET#** 0: AGP2.0 mode (Not support) 1: AGP3.0 mode
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RW	0	**AGP8X Mode Enable** 0: Disable 1: Enable
2	RW	1	**AGP4X Mode Enable** 0: Disable 1: Enable
1	RW	0	**AGP2X Mode Enable** 0: Disable 1: Enable
0	RW	0	**AGP1X Mode Enable** 0: Disable 1: Enable

Offset Address: 4Dh (D0F0)
AGP Capability Header Control **Default Value: 04h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	0	**GSBA Strobe Delay for Receiving**	
5	RW	0	**GART Access Control** 0: GART access enabled by RGTEN (RxBF[7]) 1: GART access enabled by either APEREN_A (Rx90[8]) or APEREN_B (Rx90[8]) (decided by RAGPCAP1 (D1F0 RxBF[0])	**RBKGTEN**
4	—	0	**Reserved**	
3	RW	0	**AGP Major / Minor Number Control** 0: Major / Minor = 35 1: Major / Minor = 30	**RBKMJMN**
2	RW	1	**Select Rx80 as the AGP20 or AGP30 Header** 0: Rx80 is used as the AGP20 capability header even if the chip is powered up in AGP30 mode 1: Rx80 is used as the AGP30 capability header when the chip is powered up in AGP30 mode	**RAGP30CAP**
1	RW	0	**Enable AGP Hardware Registers in Rx4A ~ Rx4B** 0: AGP hardware is configured by register values defined in AGP header (for 3.0) 1: AGP hardware is configured by register values defined in Rx4A ~ Rx4B (for VPX mode)	
0	RW	0	**Enable AGP Header Status Register Write** 0: Disable (Status registers in the AGP header cannot be modified) 1: Enable (Status registers in the AGP header can be modified)	**RSTATW**

Offset Address: 4Fh (D0F0)
Multiple Function Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	—
0	RW	0	**Multi-Function Support** 0: Disable; functions 1, 2, 3, 4, 7 cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed 1: Enable; This bit's setting will be reflected on Rx0E[7]	**MFUNC**

AGP Extended Power Management Control (50–57h)

Offset Address: 50h (D0F0)
Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Capability ID**

Offset Address: 51h (D0F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 52h (D0F0)
Power Management Capabilities **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Power Management Capabilities**

Offset Address: 53h (D0F0)
Power Management Capabilities **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Power Management Capabilities**

Offset Address: 54h (D0F0)
Power Management Control / Status **Default Value: 0nh**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1:0	RW	—	**Power State** 00: D0 11: D3 Hot

Offset Address: 55h (D0F0)
Power Management Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Power Management Status**

Offset Address: 56h (D0F0)
PCI to PCI Bridge Support Extensions **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**PCI to PCI bridge Support Extensions**

Offset Address: 57h (D0F0)
Power Management Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Power Management Data**

AGP 3.0 Configuration (80–Afh)

For registers (e.g. AGP status register) with attribute "XW", it is allowed to write-over the default setting by setting the register RSTATW (status write) at Rx4D[0] to 1.

Offset Address: CAPPTR (D0F0 83-80h)
AGP Capability **Default Value: 00355002h**

Bit	Attribute	Default	Description
31:24	RZ	0	**Always Return 0 (write no effect)**
23:20	R-IW	0011	**Major Revision**
19:16	R-IW	5h	**Minor Revision** The value of MINOR is determined by RBKMJMN (Rx4D[3]). 0000b: if RBKMJMN = 1 0101b: if Rx4D[3] = 0
15:8	R-IW	50h	**Pointer to Next Item**
7:0	R-IW	02h	**Capability ID**

Offset Address: CAPPTR + 04h (D0F0 87-84h)

AGP Status **Default Value: 1F00 0A0nh**

Bit	Attribute	Default	Description	Mnemonic
31:24	R-XW	1fh	**Max # of AGP Command Requests**	
23:18	RZ-IW	0	**Reserved**	
17	R-XW	0	**Isoch Transaction** 0: Isoch transaction is not supported 1: Supports Isoch transaction	**RISOCH_A**
16	RZ-XW	0	**Reserved**	
15:13	R-XW	0	**Optimum Asynchronous Request Size** Suggested setting is 010b or 2^(2+4) = 64 bytes for 8QW access	
12:10	R-XW	010	**Calibrating Cycle** 000 : 4MS 001 : 16MS 010 : 64MS 011 : 256MS Valid when RAGP30 (bit 3) is 1.	
9	R1-IW	1	**SBA support is always ON**	
8	R-XW	0	**Coherent Support** Not implemented	
7	R-XW	0	**64-bit GART Entries** Support 32-bit GART entry only	
6	R-XW	0	**Host GART Translation** 0: Support host GART translation 1: Does not support host GART translation	
5	R-XW	0	**Over 4GB Support – not implemented**	
4	R-XW	0	**Fast Write Support**	
3	R-XW	0	**AGP 3.0 Detected** 0: AGP 2.0 Mode (not supported) 1: AGP 3.0 Mode initial value: set by strap ball AGP8XDET#	**NC_RAGP30**
2:0	R-XW	011 111	**If NC RAGP30 (bit 3) is 1**, the default value is 011: supports 4X and 8X data transfer rate. **If NC RAGP30 (bit 3) is 0**, the default value is 111: supports 1X, 2X and 4X data transfer rate.	

Offset Address: CAPPTR + 08h (D0F0 8B-88h)

AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Max # of AGP Command Requests**
23:16	RZ-IW	0	**Reserved**
15:13	RZ-IW	0	**Reserved for Master Devices**
12:10	RW	0	**Calibrating Cycle**
9	RW	0	**SBA Enable** 0: Disable 1: Enable
8	RW	0	**AGP Enable** 0: Disable 1: Enable
7	RW	0	**64-Bit GART** Not supported
6	RZ-MW	0	**Reserved**
5	RW	0	**Over 4G Support** 0: Disable 1: Enable
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RZ-MW	0	**Reserved**
2:0	RW	0	**AGP Data Transfer Rate** If NC_RAGP30 (Rx84[3]) = 1 001: 4X data transfer rate 010: 8X data transfer rate If MC_RAGP30 = 0, 001: 1X data transfer rate 010: 2X data transfer rate 100: 4X data transfer rate

Offset Address: CAPPTR + 0Ch: (D0F0_8F-8Ch)

AGP Isochronous Status **Default Value: 0000 0028h**

This register can only be accessed if RISOCH (Rx86[2])is set. Otherwise, all registers are RZ.

Bit	Attribute	Default	Description	Mnemonic
31:24	R-XW	0	**Reserved**	
23:16	R-XW	0	**Maximum Bandwidth (in unit of 32 bytes)** Shared by both asynchronous and isochronous transactions	
15:8	R-XW	0	**Maximum Number of Isochronus Transactions in a Single Isochronous Period**	
7:6	R-XW	00	**Isochronous Payload Size Supported** 00: 32,64,128,256 bytes 01: 64,128,256 bytes 10: 128,256 bytes 11: 256 bytes	ISOCH_Y_A
5:3	R-XW	101	**Isochronous Data Transfer Maximum Latency (in unit of 1 us)**	ISOCH_L_A
2	R-XW	0	**Reserved**	
1:0	R-XW	00	**Isochronous Error Code** 00: No error 01: Isoch Request Overflow 1x: Reserved	

Offset Address: CAPPTR + 10h (D0F0_93-90h)

AGP Control **Default Value: 0000 0080h**

Bit	Attribute	Default	Description	Mnemonic
31:10	—	0	**Reserved (writable)**	
9	RW	0	**Disable Calibration Cycle**	
8	RW	0	**Enable AGP Aperture (Enable CPU/PMSTR GART Access)** Set to 1 to enable AGP Aperture. Note: RBKGTEN (Rx4D[5]) must be 1 to enable this function.	APEREN_A
7	RO	1	**GTLB Enable** When set to 0, GART TLB entries are invalidated. All AGP aperture accesses need to fetch translation table first.	
6:0	—	0	**Reserved**	

Offset Address: CAPPTR + 14h (D0F0_97-94h)

AGP Aperture Size **Default Value: 0001 0F00h**

Bit	Attribute	Default	Description	Mnemonic
31:28	RW	0000	**Aperture Page Size Select** The page size is determined by the formula: 2^[n+12] Default, 0000b, 4KB is supported.	
27	—	0	**Reserved**	
26:16	R-IW	01h	**Page Size Supported** If bit N is 1, which indicates support of page size of (2^(N+12)). Currently only 4KB page size is supported.	
15:12	—	0	**Reserved**	
11:0	RW	F00h	**Aperture Size – Default size is 256MB** Refer to Table 2 for detailed setting (Maximum aperture size: 2GB) GTSZ[n]=0 forces APBASE[22+n] to 0 when 0 <= n <= 5 GTSZ[n]=0 forces APBASE[22+n-2] to 0 when 8 <= n <=11 GTSZ[n]=1 allows APBASE[22+n] to be Read/Write-able. GTSZ[11] is hardwired to 1 and GTSZ[7:6] are hardwired to 00. When NC_RAGP30 (Rx84[3]) is 0, only supports 4MB ~ 256MB.	GTSZ_A[11:0]

Table 2. Aperture Size

Aperture Size \ Rx94[11:0] (GTSZ)	11	10	9	8	7	6	5	4	3	2	1	0
4MB	1	1	1	1	0	0	1	1	1	1	1	1
8MB	1	1	1	1	0	0	1	1	1	1	1	0
16MB	1	1	1	1	0	0	1	1	1	1	0	0
32MB	1	1	1	1	0	0	1	1	1	0	0	0
64M	1	1	1	1	0	0	1	1	0	0	0	0
128M	1	1	1	1	0	0	1	0	0	0	0	0
256M	1	1	1	1	0	0	0	0	0	0	0	0
512M	1	1	1	0	0	0	0	0	0	0	0	0
1G	1	1	0	0	0	0	0	0	0	0	0	0
2G (Max Aperture Size)	1	0	0	0	0	0	0	0	0	0	0	0
4G	0	0	0	0	0	0	0	0	0	0	0	0

Offset Address: CAPPTR + 18h (D0F0 9B – 98h)
AGP GART Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**GART Table Base Address [31:12]**
11:0	—	0	**Reserved**

Offset Address: CAPPTR + 1Ch (D0F0 9F- 9Ch)
AGP GART Table Pointer High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Base Address [63:32]** Since OVER4G is not supported, OS should program this register to zero. This register is ignored.

Offset Address: CAPPTR + 20h (D0F0 A3-A0h)
AGP Isochronous Command **Default Value: 00000040h**

Bit	Attribute	Default	Description
31:8	RZ-IW	0	**Reserved**
7:6	RW	01	**Isochronous Payload Size** Default is ISOCH_Y (CAPPTR + 0C [7:6])
5:0	RZ-IW	0	**Reserved**

AGP Enhanced Control (B0–FFh)

Offset Address: B8h (D0F0)
AGP Enhanced Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	—	0	**Reserved**
2	RW	0	**AGP Pad Power Down**
1	—	0	**Reserved (Not used)**
0	—	0	**Reserved (Not used)**

Offset Address: B9h (D0F0)
AGP Mixed Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FIFO Depth Control** 0: Normal FIFO Depth – 64 QW, isochronous FIFO Depth – 32 QW 1: Normal FIFO Depth – 96 QW, isochronous FIFO Depth – 0 QW
6	RW	0	**Hold GD Signal Level After De-assertion of RTXRDY**
5:0	RW	0	**Maximum Number of Isochronous Request Supported** (ISOCH_N (Rx8C[15:8]) * ISOCH_L (Rx8C[5:3]))

Offset Address: Bah (D0F0)
Isochronous Read GPRI Assertion Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPRI Read Counter** GPRI assertion period for Isochronous Read Request

Offset Address: BB (D0F0)
Isochronous Write GPRI Assertion Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPRI Write Counter** GPRI assertion period for Isochronous Write Request

Offset Address: BCh (D0F0)
AGP Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**AGP Disable**	
6	RW	0	**AGP Read Synchronization** 0: Disable 1: Enable	
5	RW	0	**AGP Read Snoop DRAM Post-Write Buffer** 0: Disable 1: Enable	
4	RW	0	**PP2REQ (CPU/PCI1-to-PCI2 REQ) / AGP Read Priority** 0: Disable the function. (PP2REQ's priority become higher when AGPC parking at AGP master) 1: PP2REQ has higher priority if MGFIFO is not over 24 QW for low priority read	
3	RW	0	**GRDY 2T Early Control (Not support)** 0: Disable 1: Enable	
2	RW	0	**Enable FENCE / FLUSH** 0: LPR could be executed in out-of-order mode 1: Enable FENCE / FLUSH. All normal priority AGP operations are executed sequentially.	**RFENCE**
1	RW	0	**GGNT Parking Policy** 0: Non-parking GGNT; GGNT is de-asserted after GFRAME or PIPE assertion 1: Parking GGNT; after the assertion of GFRAME or PIPE, GGNT is kept asserted till GREQ de-asserted or timeout.	**RPKGNT**
0	RW	0	**AGP to PMSTR / C2P Turn Around Cycle** 0: 2 or 3T 1: 1T	**RGDARB**

Notes: 1. When RPKGNT (RxBC[1]) is set to 1, GGNT will remain asserted until either GREQ de-asserts or data phase ready
2. When RGDARB (RxBC[0]) is set to 0, it allows C2P access when the previous PCI master transaction is a delayed transaction.
3: RFENCE (RxBC[2]) when enabled will force all requests executed in-order, which automatically enables FENCE/FLUSH function. When disable, FENCE/FLUSH function is not guaranteed.

Offset Address: BDh (D0F0)
AGP Miscellaneous Control **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**AGP GGNT Timing** 0: Normal 1: 1T earlier
6	RW	0	**PIPE Operating Mode** 0: Normal 1: Fast mode
5	RW	0	**AGP GD and GCBE Input Pads Control** 0: Input disable 1: Input enable
4	RW	0	**AGP Operating Mode** 0: Normal 1: Fast mode
3:0	RW	02h	**AGP Data Phase Latency Timer** (in unit of 4 GCLKs)

Offset Address: BEh (D0F0)
AGP Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Select NMI / AGPBUSY# Function** 0: NMI 1: AGPBUSY#	
6	RW	0	**Enable PP2 Request Timeout (for Isochronous support)**	
5	RW	0	**Isochronous Read Snoop DRAM Post-Write Buffer** 0: Disable 1: Enable	
4	RW	0	**Guard Register for Isochronous Request with Length Inconsistent with the Setting of PISOCH_Y (CAPPTR + 20h [7:6])** 0: ISOCH_Y = PISOCH_Y 1: 1: ISOCH_Y = 2'h3 Where ISOCH_Y is located at CAPPTR + 0Ch [7:6]	
3	RW	0	**AGP Asynchronous FIFO Sharing with Isochronous Read (when no asynchronous read allocated)** 0: Disable 1: Enable	
2	—	0	**Reserved**	
1	RW	0	**Internal Graphics RDY Signal Assertion Policy** 0: Asserts RDY when the whole transaction data received 1: Asserts RDY when one block of data received	
0	RW	0	**CPU GART Read and AGP GART Write Coherency Enable** 0: Disable 1: Enable	

Offset Address: BFh (D0F0)
AGP 3.0 Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Enable CPU/PMSTR GART Access** 0: Disable 1: Enable This control bit is used differently from APEREN of Rx90. Also, Rx4D[5] must be 0 for this control bit to be effective.	**RGTEN**
6	RW	0	**AGP Calibration Enable** 0: Disable 1: Enable	
5	RW	0	**Mix Coherent / Non-coherent Access Enable** 0: Disable 1: Enable	
4	RW	0	**DBI/PIPE Ball Function** 0: DBIH 1: PIPE	
3	RW	0	**DBI Function Enable** 0: Disable 1: Enable Global DBI enable control – If disabled (set to 0), DBI input is masked, and outputs assume DBI=0.	
2	RW	0	**DBI Output for AGP Transaction Enable** 0: Disable 1: Enable	
1	RW	0	**DBI Output for FRAME Transaction Including Fast-Write Enable** 0: Disable 1: Enable	
0	RW	0	**Reserved**	

Offset Address: C0h (D0F0)
AGPC CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Rising-Time Control (R Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps
5:4	RW	00	**CKG Falling-Time Control (R Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps
3:2	RW	00	**CKG Rising-Time Control (S Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps
1:0	RW	00	**CKG Falling-Time Control (S Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps

Offset Address: C1h (D0F0)
AGPC CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:2	RW	00	**CKG Rising-Time Control (D Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps
1:0	RW	00	**CKG Falling-Time Control (D Port)** 00: Default timing 01: Delay by 100ps 10: Delay by 200ps 11: Delay by 300ps

Offset Address: C2h (D0F0)
AGP Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Sync PIPE / SBA Request** 0: Disable 1: Enable
6	RW	0	**Fast RMREQ** 0: Disable 1: Enable Reduce 1T for SBA2X/4X/8X accessing DRAM cycles when this function is enabled
5	RW	0	**Fast GADS Conversion** 0: Disable 1: Enable
4:3	RW	0	**AGP Recorder Distance (Not support)** 00: 16 QW 01: 24 QW 10: 32 QW 11: 48 QW
2	RW	0	**AGPC Recorder Control (Not support)** 0: Disable 1: Enable
1	RW	0	**Grant Isochronous Write When Buffers** Are Available for the Whole Payload 0: Disable 1: Enable
0	RW	0	**GGNT Assertion Control (Always high)** 0: Assert GGNT after the whole requested data is ready 1: Assert GGNT when a block of the requested data is ready

Offset Address: F0h (D0F0)
PSTATECTL Pulse Width Count (LCLK Domain) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Number of LCLK PSTATECTL to LDTC Stay Active**

Offset Address: F1h (D0F0)
GD and GC#BE Strobe Delay **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW	1	**GD and GC#BE Strobe Delay for Receiving for the Second 16 bits**

Offset Address: F2h (D0F0)
AGPC CKG Control – Second 16 Bits **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Rising-Time Control for the Second 16 Bits (R Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Falling-Time Control for the Second 16 Bits (R Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Rising-Time Control for the Second 16 Bits (S Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Falling-Time Control for the Second 16 Bits (S Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: F3h (D0F0)

AGPC CKG Control – Second 16 Bits **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**GD, GC#BE Receive Strobe Delay for the Second 16 Bits** 00: Delay by –150 ps 01: No delay 10: Delay by 150 ps 11: Delay by 300 ps
5:4	RW	00	**GADSTBx Output Delay for the Second 16 Bits** 00: No delay 01: Delay by 150 ps 10: Delay by 300 ps 11: Delay by 450 ps
3:2	RW	00	**CKG Rising-Time Control for the Second 16 Bits (D Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Falling-Time Control for the Second 16 Bits (D Port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Device 0 Function 0 (D0F0) – Extended Space

Virtual Channel Capability (140–14Fh)

Virtual Channel Capability is defined for Egress direction of the device, including TC/VC mapping, VC arbitration and Port arbitration. Hardware Round-Robin arbitration scheme is applied in both Port and VC arbitration. By default, TC0 is mapped to VC0 while TC1, TC2, TC3, TC4, TC5, TC6 and TC7 are mapped to VC1.

Offset Address: 143-140h (D0F0)
Virtual Channel Enhanced Capability Header **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability Offset**
19:16	RO	1	**Capability Version**
15:0	RO	2h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D0F0)
Port VC Capability Register 1 **Default Value: 0000 0400h**

Bit	Attribute	Default	Description
31:12	—	0	**Reserved**
11:10	RO	01	**Port Arbitration Table Entry Size** 01: Arbitration entry size is 2 bits.
9:8	RO	0	**Reference Clock**
7	—	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	—	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D0F0)
Port VC Capability Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
31:24	RO	0	**VC Arbitration Table Offset** Table is not implemented.
23:8	—	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability**

Offset Address: 14D-14Ch (D0F0)
Port VC Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3:1	RO	0	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table**

Offset Address: 14F-14Eh (D0F0)
Port VC Status Register **Default Value: 00h**

Bit	Attribute	Default	Description
15:1	—	0	**Reserved**
0	RO	0	**VC Arbitration Table Status (TL)** Reserved

VC0 Resource Registers (150–15Bh)

Offset Address: 153-150h (D0F0)

VC Resource Capability Register (VC0) **Default Value: 00000001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Table is not implemented.
23	—	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions** Reserved
14	RO	0	**Advanced Packet Switching** Reserved
13:8	—	0	**Reserved**
7:0	RO	01	**Port Arbitration Capability** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme.

Offset Address: 157-154h (D0F0)

VC Resource Control Register (VC0) **Default Value: 800200FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable**
30:27	—	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	001	**Port Arbitration Select** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme
16	RO	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0 (by software). Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D0F0)

VC Resource Status Register (VC0) **Default Value: 00h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status (TL)** Reserved
15:0	—	0	**Reserved**

VC1 Resource Registers (15C–16Fh)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following registers will be read as 0.

Offset Address: 15F-15Ch (D0F0)

VC Resource Capability Register (VC1) **Default Value: 1000001Fh**

Bit	Attribute	Default	Description
31:24	RO	10	**Port Arbitration Table Offset (VC1)**
23	—	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transaction**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	—	0	**Reserved**
7:0	RO	1F	**Port Arbitration Capability** Supported Time-based WRR up to 128 phases

Offset Address: 163-160h (D0F0)

VC Resource Capability Register (VC1) **Default Value: 01020000h**

Bit	Attribute	Default	Description
31	RO	0	**VC Enable**
30:27	—	0	**Reserved**
26:24	RW	1	**VC ID**
23:20	—	0	**Reserved**
19:17	RW	1	**Port Arbitration Select** 01: Non-configurable fixed hardware-fixed Round Robin arbitration scheme
16	RO	0	**Load Port Arbitration Table**
15:8	—	0	**Reserved**
7:0	RW Bit 0: RO	0FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0 (by software). Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D0F0)

VC Resource Status Register (VC1) **Default Value: 00h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status (TL)** Reserved
15:0	—	0	**Reserved**

Virtual Channel Port Arbitration Table for VC1 (180–19Fh)

Offset Address: 19F-180h (D0F0)

VC1 Port Arbitration Table **Default Value: 00h**

Bit	Attribute	Default	Description
255:254	RW	0	**Phase 127** 00: Time slot to Port 0 01: Time slot to Port 0 10: Time slot to Port 1 11: Time slot to Port 2 **Note: The above time slot assignment applies to Phase 0 – Phase 127 of the VCI Port Arbitration Table.**
2N+1 : 2N	RW	0	**Phase N, where 0< N <127**
1:0	RW	0	**Phase 0**

VC Arbitration Timer (200–209h)

PCI Express arbitration scheme is based on the same scheme used in the DRAM Controller. A timer named as Occupancy Timer is used to guarantee the number of time slots one requester will be granted when there is no high priority requesters come in. Another timer named as Promote Timer is used for a requester to upgrade its requests to high priority if it is not served after the Promote Timer times out. However, priority request promoted by the expiration of the Promote Timer will be served once only.

Offset Address: 200h (D0F0)

VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC0 Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 201h (D0F0)

VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC0 Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 202h (D0F0)

VC1 Port Arbitration Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC1 Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 203h (D0F0)

VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**VC1 Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Note: Port arbitration timers defined by registers 202h and 203h are not applicable in current VC1 implementation; currently the VC1 arbitration is in strict priority.

Port Arbitration Timer for VC0 (210–229h)

Offset Address: 212h (D0F0)
Root Port 1 (x4) Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 213h (D0F0)
Root Port 1 (x4) Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 216h (D0F0)
Root Port 2 (x1) Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of 125MHz)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 217h (D0F0)
Root Port 2 (x1) Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of 125MHz)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Host Side Upstream Arbitration Timers (230–23Fh)

A fair arbitration timer is designed for the upstream traffic, which provides a fair arbitration between PCI express devices and other devices like AGP, PCI2 master, IOAPIC and V-Link. The arbitration scheme also used the one currently implemented in the DRAMC.

Offset Address: 230h (D0F0)
PCIe – VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 231h (D0F0)
PCIe – VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 232h (D0F0)
PCIe – VC1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe – VC1 Strict Priority** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 233h (D0F0)
PCIe – VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 234h (D0F0)
V-Link Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GPCI or NVC (PMADS) Request** 0: Disable 1: Enable
6	RW	0	**High Priority to GPCI or NVC (with PMSIO) Request** 0: Disable 1: Enable
5:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 235h (D0F0)
V-Link Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 236h (D0F0)
V-Link – VC1 Arbitration Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**Strict Priority to V-Link – VC1** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 237h (D0F0)
V-Link – VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 238h (D0F0)
AGP Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GADS from AGPC** 0: Disable 1: Enable
6	RW	0	**High Priority to GADS with GISOCH Asserted** 0: Disable 1: Enable
5:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 239h (D0F0)
AGP Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 23Ah (D0F0)
PCI2 / NVC Occupancy Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	0	**NVC Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T
3:2	—	0	**Reserved**
1:0	RW	0	**PCI2 Occupancy Timer (in unit of host frequency)** 00: Timer is off (i.e. 1T Round Robin scheme) 01: 4T 10: 8T 11: 16T

Offset Address: 23Bh (D0F0)
PCI2 / NVC Promote Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	0	**NVC Promote Timer (in unit of host frequency)** 00: Timer is off 01: 4T 10: 8T 11: 16T
3:2	—	0	**Reserved**
1:0	RW	0	**PCI2 Promote Timer (in unit of host frequency)** 00: Timer is off 01: 4T 10: 8T 11: 16T

Offset Address: 23Ch (D0F0)
IOAPIC Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of host frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 23Dh (D0F0)
IOAPIC Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of host frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

DRAM Side Upstream Arbitration Timers (240–24Fh)

This fair arbitration timer is for upstream traffic to do a fair arbitration between all of the VC1 PCI express devices and AGP.

Offset Address: 240h (D0F0)
PCIe-VC1 Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to VC1** 0: Disable 1: Enable
6:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of DRAMC frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 241h (D0F0)
PCIe-VC1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of DRAMC frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Offset Address: 244h (D0F0)
AGP Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Occupancy Timer (in unit of DRAMC frequency)** 0000: Timer is off (Arbitration will be based on a fair RR scheme) 0nh: 4n T, where 1<= n <= 15

Offset Address: 245h (D0F0)
AGP Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	0	**Promote Timer (in unit of DRAMC frequency)** 0000: Timer is off 0nh: 4n T, where 1<= n <= 15

Device 0 Function 1 (D0F1): Error Reporting

Header Registers

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	1308h	**Device ID – Error Reporting**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0200h	**PCI Status**
8h	RO	0	**Revision ID**
0B – 9h	RO	060000h	**Class Code**
0Dh	RO	0	**Latency Timer**
0Eh	RO	00h	**Header Type**
0Fh	RO	0	**BIST**
13 – 10h	—	—	**Reserved**
2D – 2Ch	RW1	0	**Subsystem Vendor ID**
2F – 2Eh	RW1	0	**Subsystem ID**
33 – 30h	—	—	**Reserved**
37 – 34h	RO	0	**Capability Pointer**
3F – 38h	—	—	**Reserved**

V-Link Error Report (50-5Fh)

Offset Address: 50h (D0F1)

V-Link Error Status — **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW1C	0	**V-Link Parity Error Detected** 0: No V-Link Parity Error being detected 1: V-Link Parity Error detected

Offset Address: 58h (D0F1)

V-Link Error Command — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parity Error / SERR# Report Through NMI** 0: Disable 1: Enable
6	RW	0	**Parity Error / SERR# Report Through V-Link to SB** 0: Disable 1: Enable
5:1	—	0	**Reserved**
0	RW	0	**V-Link Parity Check Report** 0: Disable 1: Enable

Host Bus Error Report (60-7Fh)

Offset Address: 60h (D0F1)

Host Parity Status — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Host Address Parity Error Detected** 0: No Address Parity Error being detected 1: Address Parity Error detected
6	RW1C	0	**Host Data Parity Error Detected** 0: No Data Parity Error being detected 1: Data Parity Error detected
5	RW1C	0	**AGP Access Above 4G Detected** 0: No above 4GB AGP cycles being detected 1: AGP Access Above 4GB detected
4	RW1C	0	**Host LOCK Cycle to PCI Detected** 0: No host Lock cycle to PCI being detected 1: Host Lock Cycle to PCI detected
3	RW1C	0	**MC Error Status**
2	RW1C	0	**BINIT Error Status**
1:0	—	0	**Reserved**

Offset Address: 68h (D0F1)
Host Parity Command **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Address Parity Generation and Check (AP[1:0]#)** 0: Disable 1: Enable
6	RW	0	**Host Data Parity Generation and Check (DP[3:0]#)** 0: Disable 1: Enable
5	RW	0	**Host Response Parity Generation (RSP#)** 0: Disable 1: Enable
4	RW	0	**Parity Error SERR# / NMI Assertion (see the settings on Rx58[7:6])** 0: Disable 1: Enable
3	RW	0	**Parity Test Mode** 0: Disable (normal mode) 1: Enable (invert the parity bit)
2:0	—	0	**Reserved**

DRAM Bus Error Report (80-8Fh)

AGP / PCI2 Non Standard Error Reporting (E0-EFh)

Offset Address: E0h (D0F1)
AGP / PCI2 Error Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	W1C	—	**AGP Cycles Data Parity Error Status** 0: No Parity Error being detected 1: Parity Error detected
6	W1C	0	**PCI2 GSERR Error Status** 0: No GSERR being detected 1: GSERR detected
5:0	—	0	**Reserved**

Offset Address: E1h (D0F1)
AGP / PCI2 Error Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1:0	RO	0	**Isochronous Error Code (see D0F0 Rx8C[1:0])**

Offset Address: E8h (D0F1)
AGP / PCI2 Error Report Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Parity Error Report for AGP Data Parity Error** 0: Disable 1: Enable
3:2	—	0	**Reserved**
1	RW	0	**Parity Error Report for PCI2 Data Parity Error** 0: Disable 1: Enable
0	RW	0	**Parity Error Report for PCI2 Address Parity Error** 0: Disable 1: Enable

Device 0 Function 2 (D0F2): Host Bus Control

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	2308h	**Device ID – Host Bus**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0200h	**PCI Status**
8h	RO	00	**Revision ID**
0B – 9h	RO	060000h	**Class Code**
0Dh	RO	00	**Latency Timer**
0Eh	RO	00	**Header Type**
0Fh	RO	00	**BIST**
13-10h	—	0000	**Reserved**
2D – 2Ch	RW1	00	**Subsystem Vendor ID**
2F – 2Eh	RW1	00	**Subsystem ID**
33 – 30h	RO	00	**Reserved**
37 – 34h	RO	00	**Capability Pointer**
3F – 38h	—	—	**Reserved**

Host CPU Control (50-5Fh)

Offset Address: 50h (D0F2)

Request Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RO	dip	**IOQ (In-Order Queue) Depth** 0: 1 level 1: 12 level Default sets from the inverse of the VD2 signal during system initialization. For strap ball information, check the Strap Ball table for details.	
6	RO	dip	**Dual CPU** 0: Single CPU 1: Dual CPU Default sets from the VD7 signal during system initialization. For strap ball information, check the Strap Ball table for details.	
5	RW	0	**Fast ADS Assertion to DRAM Controller** 0: Disable 1: Enable	
4:0	RW	0	**Dynamic Defer Snoop Stall Count** Value for the Defer Snoop Stall Counter. The timer starts counting at the beginning of the snoop phase of C2P cycle; it increases one for every 2 HCLKs. If the C2P cycle is pending when the timer expired, and there are pending ADS, a Defer/Retry response will be replied to the host. For medium decoding PCI slave device; the optimal value for DEFTIM is 8.	**DEFTIM[4:0]**

Table 5. Dynamic Defer Snoop Stall Table

Timer Expired	New Pending ADS	PCI Completion	Action
No	-	No	Snoop stall till PCI complete
No	-	Yes	Normal Data Response
Yes	No	No	Snoop stall till either arrival of new pending ADS or PCI complete
Yes	No	Yes	Normal Data Response
Yes	Yes	No	Defer/Retry Response
Yes	Yes	Yes	Normal Data Response

Offset Address: 51h (D0F2)
CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Fast Ready for CPU Memory Read Cycle** 0: Disable, wait until all 8QWs are received before DRDY assertion 1: Enable, DRDY assertion timing is set up through Rx60-67	
6	RW	0	**Read Around Write** 0: Disable 1: Enable	**RAW**
5	RW	0	**Host Controller DRAM Request Queue Control (DRQCTL)** 0: Disable pipelined DRQCTL 1: Enable pipelined DRQCTL	
4	RW	0	**CPU to PCI Read Defer** 0: Disable 1: Enable	
3	RW	0	**2 Defer/ Retry Entries** 0: Disable 1: Enable	
2	RW	0	**2 Defer / Retry Entries Sharing** 0: One entry for each processor 1: Each entry is shared by the two processors	
1	—	0	**Reserved**	
0	RW	0	**APIC Logic Modification** 0: Enable APIC logic modification for PCI Master 8QW Access (Rx54[2]) mode 1: Do not enable the modification circuit	

Offset Address: 52h (D0F2)
CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**CPU Read / Write DRAM 0WS for Back-to-Back Pipeline Access** 0: Disable 1: Enable	
6	RW	0	**HREQ (Host Continuous DRAM Ownership) / HPRI (Host High Priority DRAM Request) Assertion to DRAM Controller** 0: Disable 1: Enable assertion of HREQ / HPRI to DRAM controller for efficient memory utilization / faster memory data access.	
5	RW	0	**AGTL+ Pullup Enable** 0: Disable 1: Enable Default sets from the inverse of the VD3 signal during system initialization. For strap ball information, check the Strap Ball table for details.	
4	—	0	**Reserved**	
3	RW	0	**Write Retire Policy After 2 Writes** 0: Disable 1: Enable	**RFRAW**
2	RW	0	**2 Level Defer Queue With Lock Cycle** 0: Disable 1: Enable	
1	RW	0	**Consecutive Speculative Read** 0: Disable 1: Enable	
0	RW	0	**Speculative Read** 0: Disable 1: Enable	

Offset Address: 53h (D0F2)
Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Host Occupancy Timer** (in unit of 4 HCLKs) Host Occupancy timer guarantees a time slot of P6TIM * 4 HCLK for pipelined CPU's ADS.	
3:0	RW	0	**Master Occupancy Timer (in unit of 4 HCLKs)** Master Occupancy timer guarantees a time slot of PRITIM*4 HCLK for pending master requests.	**PRITIM[3:0]**

Offset Address: 54h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:5	RO	000	**CPU FSB Frequency (Powell)** 000: 100MHz 001: 133MHz 010: 200MHz 011: 166MHz 100: Reserved Default sets from the VD4, VD1 and VD0 signals during system initialization. For strap ball information, check the Strap Ball table for details.	
4	RO	0	**Burst 8QW Host to Memory Access** 0: Disable 1: Enable This bit must be set to 1 in 128-bit DRAM mode.	
3	RW	0	**Host-Memory DRDY Assertion Adjustment** 0: Normal mode, no adjustment 1: Special mode This bit's setting should follow RDRDYLPH / RDRDYQPH / RDRDYPH_WS (Rx60 – Rx67) settings. Check Rx55[1] for details of DRDY assertion adjustment..	**RFASTH**
2	RW	0	**PCI Master 8QW Memory Access** 0: Disable 1: Enable	
1	RW	0	**Memory-to-Host Conversion Circuit** 0: Transparent mode 1: Sync 1T in certain clock phases Transparent mode (default operating mode) is faster than Sync mode.	
0	RW	0	**PCI2 Operating Mode (for EOI message processing)** 0: AGP mode 1: VPX mode	

Offset Address: 55h (D0F2)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Set NB Host Interface IOQ Size** **CPUIOQSZ** **CPUIOQSZ8** **Host IF IOQ Size** 0 x 1 1 1 8 1 0 12
6	RW	0	**Disable CPU's HT Option** 0: Enabled HT 1: Disable HT
5	—	0	**Reserved**
4	RW		**Early read data ready signal for Host Interface DRDY table.** 0: 2T early 1: 3T early
3	RW	0	**Fast Command When Dynamic Clock is Enabled** 0: Disable 1: Enable
2	RW	0	**Medium Threshold for Write Policy (see ROPTW (RxF9[3:0]) for details)** 0: Disable medium threshold 1: Add a medium threshold, defined by Rx56, in Write Queue to enable earlier memory write. Refers to Rx5D for write policy.
1	RW	0	**Host-Memory DRDY Assertion 2T Adjustment** 0: 2T early 1: 2T late This bit is effective when RFASTH (Rx54[3]) is 1.
0	RW	0	**Request Reorder** 0: Disable 1: Enable

Offset Address: 56h (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Medium Threshold for Write Policy**	**ROPTW[3:0]**
3:0	—	0	**Reserved**	

Offset Address: 59h (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Reserved**
5:4	RW	0	**Warm CPU Reset (CPURST#) Duration Control** 00= 512us 01= 1024us 10= 1532us 11= 2048us
3	RW	0	**Warm CPU Reset (CPURST#) Trigger** Write 0 □ 1 transition will trigger warm CPURST# Firmware will have to reset this bit to "0" before trigger another CPURST#.
2:1	—	0	**Reserved**
0	RW	0	**Lowest-Priority IPI (Inter-Processor Interrupt) Support** 0: Disable 1: Enable

Offset Address: 5Ch (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	0	**Enable patching D11 from reserved to set when logic mode APIC**
3	RW	0	**APIC Redirection Hint Information Obtained From** 0: Address filed 1: Data field (not supported)
2	RW	0	**APIC Destination Mode Information Obtained From** 0: Address field 1: Data field (not supported)
1	RW	0	**APIC Cluster Mode Support** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: 5Dh (D0F2)
Write Policy **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Write Request High Threshold**	**RWLM[3:0]**
3:0	RW	0	**Write Request Low Threshold**	**RWBS[3:0]**

Table 6. CPU Write Request Policy

RAW Rx51[6]	RFRAW Rx52[3]	RWLM Rx5D[7:4]	RWBS Rx5D[3:0]	Write Policy
1	0	x	x	Will not handle write request until FIFO is full
1	1	4	2	Will start processing write request when write request count reaches RWLM, and stop processing write request when write request count drops to RWBS.

Offset Address: 5Eh (D0F2)
Bandwidth Timers **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**Host Bandwidth Timer**	**RHBWTM [3:0]**
3:0	RW	0	**DRAM Bandwidth Timer**	**RDBWTM [3:0]**

Offset Address: 5Fh (D0F2)
CPU Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6	RW	0	**Reorder Retry Queue Enable** 0: Retried CPU transaction always complete in order 1: Allow second entry of retried (IOW/MEMW) transaction to complete before first queued entry
5	RW	0	**Enable HPCREQ# (pre-charge request) input from CPU** 0: HPCREQ# is disabled 1: HPCREQ# is enabled
4	RW	0	**Enable PT894 HEDRDY# (early data ready) output to CPU** 0: HEDRDY# is disabled 1: HEDRDY# is enabled
3	—	0	Reserved
2	RW	0	**Host Bandwidth Restriction** 0: Disable 1: Enable Host Bandwidth Timer is set up by RHBWTM [3:0] (Rx5E[7:4]).
1	RW	0	**DRAM Bandwidth Restriction** 0: Disable 1: Enable DRAM Bandwidth Timer is set up by RDBWTM [3:0] (Rx5E[3:0]).
0	RW	0	**Enable relaxed DBSY# CPU Timing Workaround.** 0: Workaround disabled 1: Workaround enabled

Table 7. Host / DRAM Bandwidth Policy

RHOSTBW Rx5F[2]	RDRAMBW Rx5F[1]	Host / DRAM Bandwidth Setting Policy
0	0	Disable the new DRAM/Host Bandwidth Arbiter
0	1	Use the DRAM Bandwidth Timer only
1	0	Use the HOST Bandwidth Timer only
1	1	Dynamically toggles between the Host and Dram bandwidth timers. Both timers, RHBWTM and RDBWTM are used by the arbitration logic.

Host Interface DRDY Timing Control

Offset Address: 60h (D0F2)
Line DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	0	**Read Line Phase 4 Wait State**	**RDRDYLPH4**
5:4	RW	0	**Read Line Phase 3 Wait State**	**RDRDYLPH3**
3:2	RW	0	**Read Line Phase 2 Wait State**	**RDRDYLPH2**
1:0	RW	0	**Read Line Phase 1 Wait State**	**RDRDYLPH1**

Offset Address: 61h (D0F2)
Line DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	0	**Read Line Phase 8 Wait State**	**RDRDYLPH8**
5:4	RW	0	**Read Line Phase 7 Wait State**	**RDRDYLPH7**
3:2	RW	0	**Read Line Phase 6 Wait State**	**RDRDYLPH6**
1:0	RW	0	**Read Line Phase 5 Wait State**	**RDRDYLPH5**

Offset Address: 62h (D0F2)
Line DRDY Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	—	0	**Reserved**	—
3:2	RW	0	**Read Line Phase 10 Wait State**	**RDRDYLPH10**
1:0	RW	0	**Read Line Phase 9 Wait State**	**RDRDYLPH9**

Offset Address: 63h (D0F2)
QW DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	0	Read QW Phase 4 Wait State	RDRDYQPH4
5:4	RW	0	Read QW Phase 3 Wait State	RDRDYQPH3
3:2	RW	0	Read QW Phase 2 Wait State	RDRDYQPH2
1:0	RW	0	Read QW Phase 1 Wait State	RDRDYQPH1

Offset Address: 64h (D0F2)
QW DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	0	Read QW Phase 8 Wait State	RDRDYQPH8
5:4	RW	0	Read QW Phase 7 Wait State	RDRDYQPH7
3:2	RW	0	Read QW Phase 6 Wait State	RDRDYQPH6
1:0	RW	0	Read QW Phase 5 Wait State	RDRDYQPH5

Offset Address: 65h (D0F2)
QW DRDY Timing Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	—	0	Reserved	—
3:2	RW	0	Read QW Phase 10 Wait State	RDRDYQPH10
1:0	RW	0	Read QW Phase 9 Wait State	RDRDYQPH9

Offset Address: 66h (D0F2)
Read Line Burst DRDY Timing Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	Phase 8 Wait State	RDRDYPH8_WS
6	RW	0	Phase 7 Wait State	RDRDYPH7_WS
5	RW	0	Phase 6 Wait State	RDRDYPH6_WS
4	RW	0	Phase 6 Wait State	RDRDYPH5_WS
3	RW	0	Phase 4 Wait State	RDRDYPH4_WS
2	RW	0	Phase 3 Wait State	RDRDYPH3_WS
1	RW	0	Phase 2 Wait State	RDRDYPH2_WS
0	RW	0	Phase 1 Wait State	RDRDYPH1_WS

Offset Address: 67h (D0F2)
Read Line Burst DRDY Timing Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	Reserved	—
5	RW	0	Phase 10 Wait State	RDRDYPH10_WS
4	RW	0	Phase 9 Wait State	RDRDYPH9_WS
3:0	—	0	Reserved	—

Note: Check BIOS Porting Guide for RDRDY register settings.

Offset Address: 6F-68h (D0F2)
APIC CPU Priority **Default Value: 00h**

Offset Address	Attribute	Default	Description	Mnemonic
6Fh	RO	0	Priority of CPU ID#7	LDR7_[7:0]
6Eh	RO	0	Priority of CPU ID#6	LDR6_[7:0]
6Dh	RO	0	Priority of CPU ID#5	LDR5_[7:0]
6Ch	RO	0	Priority of CPU ID#4	LDR4_[7:0]
6Bh	RO	0	Priority of CPU ID#3	LDR3_[7:0]
6Ah	RO	0	Priority of CPU ID#2	LDR2_[7:0]
69h	RO	0	Priority pf CPU ID#1	LDR1_[7:0]
68h	RO	0	Priority of CPU ID#0	LDR0_[7:0]

Host AGTL+ I/O Circuit (70–7Fh)

Offset Address: 70h (D0F2)
Host Address Pad (2x) Pullup Driving — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	0	2X Address Strobe Pad Pullup Driving – (HADSTB1#, HADSTB0#)
3	—	0	Reserved
2:0	RW	0	2X Address Pad Pullup Driving – (HA[31:3], HREQ[4:0])

Offset Address: 71h (D0F2)
Host Address Pad (2x) Pulldown Driving — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	0	2X Address Strobe Pad Pulldown Driving – (HADSTB1#, HADSTB0#)
3	—	0	Reserved
2:0	RW	0	2X Address Pad Pulldown Driving – (HA[31:3], HREQ[4:0])

Offset Address: 72h (D0F2)
Host Data Pad (4x) Pullup Driving — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	0	4X Data Strobe Pad Pulldup Driving – (HDSTB[3:0]N#, HADSTB[3:0]P#)
3	—	0	Reserved
2:0	RW	0	4X Data Pad Pullup Driving – (D[63:0], DBI[3:0])

Offset Address: 73h (D0F2)
Host Data (4x) Pulldown Driving — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	0	4X Data Strobe Pad Pulldown Driving – (HDSTB[3:0]N#, HADSTB[3:0]P#)
3	—	0	Reserved
2:0	RW	0	4X Data Pad Pulldown Driving – (D[63:0], DBI[3:0])

Offset Address: 74h (D0F2)
Memory Interface Timing Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	Reserved
5	RW	0	HD[63:48], HD[31:16], DBI[3,1]# Output Stagger Delay (1 ns) 0: No delay 1: 1 ns delay
4	RW	0	HA[31:17] Output Stagger Delay 0: No delay 1: 1 ns delay
3:2	RW	00	HDSTB[3:0]N#, HDSTB[3:0]P# Extra Output Delay 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps
1:0	RW	00	HADSTB1#, HADSTB0# Extra Output Delay 00: No delay 01: 150 ps 10: 300 ps 11: 450 ps

Offset Address: 75h (D0F2)

AGTL+ I/O Circuit **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**AGTL+ 4X Input: Add Delay to Filter Noise (TR3 Control)** 0: Disable 1: Enable
6	RW	0	**AGTL+ 2X Input: Add Delay to Filter Noise (TR3 Control)** 0: Disable 1: Enable
5	RW	0	**AGTL+ Slew Rate** 0: Disable 1: Enable
4	RW	0	**C3 and P4 Driving Control** 0: C3 mode, weak driving 1: P4 mode, strong driving
3	RW	0	**Input Always Pullup (PULLUP)** 0: Disable 1: Enable
2	RW	0	**AGTL+ TR Function (always pullup) for STROBE** 0: Disable 1: Enable
1	RW	0	**AGTL+ TR Function (always pullup) for DATA** 0: Disable 1: Enable
0	RW	0	**AGTL+ Dynamic Compensation** 0: Disable 1: Enable

Offset Address: 76h (D0F2)

AGTL+ Compensation Status **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Auto-Compensation Driving** 1: Enable Auto mode	
6:4	RO	0	**AGTL+ Compensation Result**	**RPOSDRV[2:0]**
3	RW	0	**AGTL+ POS Function** 1: Power-down AGTL+ input when idle	
2	RW	0	**Enable ROMSIP Auto Configure (Powell)** 0: Disable 1: Enable Default sets from the VD6 signal during system initialization. For strap ball information, check the Strap Ball table for details.	
1	RW	0	**Disable DBI Function** 0: Enable DBI 1: Disable DBI (DBI always high including DBI double-check)	
0	RW	0	**DBI Functional Mode** 0: Minimize data change count (through data comparison with previous data) 1: Minimize AGTL+ pulldown count	

Offset Address: 77h (D0F2)

AGTL+ Auto Compensation Offset **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**2X AGTL+ IO Pad Driving Offset to Compensation Result (Rx76[6:4])**	**RGTLOST2X[3:0]**
3:0	RW	0	**4X AGTL+ IO Pad Driving Offset to Compensation Result (Rx76[6:4])** The actual driving to GTL pad is RPOSDRV+RGTLOST2X, or RPOSDRV+RGTLOST4X. RGTLOST2X/RGTLOST4X can be either positive or negative offset; negative offset is represented in 2's complement, so the driving offset value ranges from –8 to +7.	**RGTLOST4X[3:0]**

Offset Address: 78h (D0F2)

Output Address / Address Clock Delay Control **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10	**Output Address Delay for Group 0** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18, respectively
5:4	RW	10	**Output Address Clock Delay for Group 0** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18, respectively
3:2	RW	10	**Output Address Delay for Group 1** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18, respectively
1:0	RW	10	**Output Address Clock Delay for Group 1** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 650ps (min), 750ps (typ), 850ps (max) from CK to CKO0~CKO18, respectively

Offset Address: 79h (D0F2)

Input Address Strobe Delay Control **Default Value: 33h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	1	**Input Address Strobe Delay for Group 0**
4	RW	1	**Input Address Strobe Delay for Group 1**
3:2	RW	00	**Input Address Strobe Delay for Group 0** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 240ps (min), 300ps (typ), 360ps (max) from DI0~DI18 to DO0~DO18, respectively
1:0	RW	00	**Input Address Strobe Delay for Group 1** 00: Delay = Td –0.4ns 01: Delay = Td –0.2ns 10: Delay = Td 11: Delay = Td + 0.2ns Delay (Td) = 240ps (min), 300ps (typ), 360ps (max) from DI0~DI18 to DO0~DO18, respectively

Offset Address: 7Ah (D0F2)

Address CKG Rising / Falling Time Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Address Group 0** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Address Group 0** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Address Group 1** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Address Group 1** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Bh (D0F2)

Address CKG Clock Rising / Falling Time Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Address Clock Group 0** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Address Clock Group 0** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Address Clock Group 1** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Address Clock Group 1** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Ch (D0F2)

Host FSB CKG Control Group 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Dh (D0F2)

Host FSB CKG Control Group 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Eh (D0F2)
Host FSB CKG Control Group 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 7Fh (D0F2)
Host FSB CKG Control Group 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CKG Falling-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
5:4	RW	00	**CKG Rising-Time Control for Host Interface (S port)** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
3:2	RW	00	**CKG Falling-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps
1:0	RW	00	**CKG Rising-Time Control for Host Interface** 00: Default timing 01: Delay by 100 ps 10: Delay by 200 ps 11: Delay by 300 ps

Offset Address: 80h (D0F2)
Input Delay for Group 0/1 **Default Value: 44h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	100	**Control Relative Delay Between Data/Strobe Input for Group 1**
3	—	0	**Reserved**
2:0	RW	100	**Control Relative Delay Between Data/Strobe Input for Group 0**

Offset Address: 81h (D0F2)
Input Delay for Group 2/3 **Default Value: 44h**

Bit	Attribute	Default	Description
7	—	0	Reserved
6:4	RW	100	**Control Relative Delay Between Data/Strobe Input for Group 3**
3:2	—	0	Reserved
1:0	RW	100	**Control Relative Delay Between Data/Strobe Input for Group 2**

Device 0 Function 3 (D0F3): DRAM Bus Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	3308h	**Device ID – DRAM Control**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0200h	**PCI Status**
8h	RO	00	**Revision ID**
0B – 9h	RO	060000h	**Class Code**
0Dh	RO	00	**Latency Timer**
0Eh	RO	00	**Header Type**
0Fh	RO	00	**BIST**
13-10h	—	—	**Reserved**
2D – 2Ch	RW1	00	**Subsystem Vendor ID**
2F – 2Eh	RW1	00	**Subsystem ID**
33 – 30h	RO	00	**Reserved**
37 – 34h	RO	00	**Capability Pointer**
3F – 38h	—	—	**Reserved**

Note: All Function 3, DRAM Controller, registers are implemented in Powell.

DRAM Rank (Row) Ending Address (40–4Fh)

Offset Address: 47-40h (D0F3)

DRAM Rank Ending Address **Default Value: 0000 0000 0000 0001h**

Offset Address	Attribute	Default	Description
40h	RW	01h	**Virtual Rank 0 Ending Address (HA[33:26])**
41h	RW	00h	**Virtual Rank 1 Ending Address (HA[33:26])**
42h	RW	00h	**Virtual Rank 2 Ending Address (HA[33:26])**
43h	RW	00h	**Virtual Rank 3 Ending Address (HA[33:26])**
44h	RW	00h	**Virtual Rank 4 Ending Address (HA[33:26])**
45h	RW	00h	**Virtual Rank 5 Ending Address (HA[33:26])**
46h	RW	00h	**Virtual Rank 6 Ending Address (HA[33:26])**
47h	RW	00h	**Virtual Rank 7 Ending Address (HA[33:26])**

Offset Address: 4F-48h (D0F3)

DRAM Rank Beginning Address **Default Value: 0000 0000 0000 0000h**

Offset Address	Attribute	Default	Description
48h	RW	00h	**Virtual Rank 0 Beginning Address (HA[33:26])**
49h	RW	00h	**Virtual Rank 1 Beginning Address (HA[33:26])**
4Ah	RW	00h	**Virtual Rank 2 Beginning Address (HA[33:26])**
4Bh	RW	00h	**Virtual Rank 3 Beginning Address (HA[33:26])**
4Ch	RW	00h	**Virtual Rank 4 Beginning Address (HA[33:26])**
4Dh	RW	00h	**Virtual Rank 5 Beginning Address (HA[33:26])**
4Eh	RW	00h	**Virtual Rank 6 Beginning Address (HA[33:26])**
4Fh	RW	00h	**Virtual Rank 7 Beginning Address (HA[33:26])**

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)

DRAM MA Map Type **Default Value: 2222h**

Bit	Attribute	Default	Description
15:13	RW	001	**Rank 4/5 MA Map Type (see the following table)**
12	RW	0	**Rank 4/5 1T Command Rate** 0: Disable (2T command) 1: 1T command
11:9	RW	001	**Rank 6/7 MA Map Type**
8	RW	0	**Rank 6/7 1T Command Rate** 0: Disable (2T command) 1: 1T command
7:5	RW	001	**Rank 0/1 MA Map Type**
4	RW	0	**Rank 0/1 1T Command Rate** 0: Disable (2T command) 1: 1T command
3:1	RW	001	**Rank 2/3 MA Map Type**
0	RW	0	**Rank 2/3 1T Command Rate** 0: Disable (2T command) 1: 1T command

Table 6. Rank MA Map Type Table

Rank MA Map Type	0	1	2	3	4	5	6	7
Bank Address Bits	2	2	2	2	Rsvd	3	3	3
Row Address Bits	13-12	14-12	15-12	15-13		15-12	15-12	15-13
Column Address Bits	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Offset Address: 52h (D0F3)

Bank Interleave Address Select **Default Value: 11h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	001	**BA0 Address Select**	**RBA0SEL_[2:0]**
3	—	0	**Reserved**	
2:0	RW	001	**BA1 Address Select**	**RBA1SEL_[2:0]**

Note: Refer to Bank Interleave Address Table below.

Offset Address: 53h (D0F3)

Bank / Rank Interleave Address Select **Default Value: 10h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**BA2 Support (turn on if any 8BK-device exists)**	**RB2AEN**
6:4	RW	001	**BA2 Address Select**	**RBA2SEL_[2:0]**
3:2	RW	000	**Rank Interleave Address Bit 1 (RA1) Select**	**RINLV1SEL_[1:0]**
1:0	RW	00	**Rank Interleave Address Bit 0 (RA0) Select**	**RINLV0SEL_[1:0]**

Table 7. DRAM Bank Address Table

RBAxSEL_[2:0] where x=0, 1, 2	0	1	2	3	4	5	6	7
BA2 RBA2SEL_[2:0] (Rx53[6:4])	A14	A15	A18	A19	rsvd	rsvd	rsvd	rsvd
BA1 RBA1SEL_[2:0] (Rx52[2:0])	A12	A14	A16	A18	A20	rsvd	rsvd	rsvd
BA0 RBA0SEL_[2:0] (Rx52[6:4])	rsvd	A13	A15	A17	A19	rsvd	rsvd	rsvd

Table 8. Rank Interleave Address Table

RINLVxSEL_[1:0] where x=0, 1	0	1	2	3
Rank Interleave Address Bit 1 RINLV1SEL_[1:0] (Rx53[3:2])	A14	A16	A18	A20
Rank Interleave Address Bit 0 RINLV0SEL_[1:0] (Rx53[1:0])	A15	A17	A19	A21

Notes. 1. Rank Interleave Address Bit 2 is fixed at A6.
2. BA2, BA1, BA0, INLV1, INLV0 should select 5 different address bits for Rx53[7] =1
3. BA1, BA0, INLV1, INLV0 should select 4 different address bits for Rx53[7] =0

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 54h (D0F3)
Physical-to-Virtual Rank Mapping 1 — **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1	**Enable Physical Rank 0** 0: Disable 1: Enable the rank
6:4	RW	000	**Virtual Rank Number of Physical Rank 0**
3	RW	0	**Enable Physical Rank 1** 0: Disable 1: Enable the rank
2:0	RW	001	**Virtual Rank Number of Physical Rank 1**

Offset Address: 55h (D0F3)
Physical-to-Virtual Rank Mapping 2 — **Default Value: 23h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 2** 0: Disable 1: Enable the rank
6:4	RW	010	**Virtual Rank Number of Physical Rank 2**
3	RW	0	**Enable Physical Rank 3** 0: Disable 1: Enable the rank
2:0	RW	011	**Virtual Rank Number of Physical Rank 3**

Offset Address: 56h (D0F3)
Physical-to-Virtual Rank Mapping 3 — **Default Value: C5h**

Bit	Attribute	Default	Description
7	RW	1	**Enable Physical Rank 4** 0: Disable 1: Enable the rank
6:4	RW	100	**Virtual Rank Number of Physical Rank 4**
3	RW	0	**Enable Physical Rank 5** 0: Disable 1: Enable the rank
2:0	RW	101	**Virtual Rank Number of Physical Rank 5**

Offset Address: 57h (D0F3)
Physical-to-Virtual Rank Mapping 4 — **Default Value: 67h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 6** 0: Disable 1: Enable the rank
6:4	RW	110	**Virtual Rank Number of Physical Rank 6**
3	RW	0	**Enable Physical Rank 7** 0: Disable 1: Enable the rank
2:0	RW	111	**Virtual Rank Number of Physical Rank 7**

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #0 Interleave Address Select (RINLV0AS[2:0])** This 3-bits field determines the Rank Interleave Address of Rank #0. If RINLV0Asn is 1 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit of Rank 0 is 1, and vice versa.	RINLV0AS[2:0]
3	—	0	**Reserved**	
2:0	RW	000	**Rank #0 Interleave Address Enable (RINLV0AEN[2:0])** 0: Mask 1: Enable This 3-bits field determines if the Rank Interleave Address of Rank #0 to be masked (used) or not. If RINLV0AENn is 0 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit will be masked (ignored), and vice versa.	RINLV0AEN[2:0]

Offset Address: 59h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #1 Interleave Address Select** See the description on Rank 0 (Rx58).	RINLV1AS[2:0]
3	—	0	**Reserved**	
2:0	RW	000	**Rank #1 Interleave Address Enable** See the description on Rank 0 (Rx58).	RINLV1AEN[2:0]

Offset Address: 5Ah (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #2 Interleave Address Select** See the description on Rank 0 (Rx58).	RINLV2AS[2:0]
3	—	0	**Reserved**	
2:0	RW	000	**Rank #2 Interleave Address Enable** See the description on Rank 0 (Rx58).	RINLV2AEN[2:0]

Offset Address: 5Bh (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #3 Interleave Address Select** See the description on Rank 0 (Rx58).	RINLV3AS[2:0]
3	—	0	**Reserved**	
2:0	RW	000	**Rank #3 Interleave Address Enable** See the description on Rank 0 (Rx58).	RINLV3AEN[2:0]

Offset Address: 5Ch (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 4 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #4 Interleave Address Select** See the description on Rank 0 (Rx58).	RINLV4AS[2:0]
3	—	0	**Reserved**	
2:0	RW	000	**Rank #4 Interleave Address Enable** See the description on Rank 0 (Rx58).	RINLV4AEN[2:0]

Offset Address: 5Dh (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 5 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #5 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV5AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #5 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV5AEN[2:0]**

Offset Address: 5Eh (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 6 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #6 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV6AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #6 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV6AEN[2:0]**

Offset Address: 5Fh (D0F3)
Virtual Rank Interleave Address Select / Enable – Rank 7 **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	—	0	**Reserved**	
6:4	RW	000	**Rank #7 Interleave Address Select** See the description on Rank 0 (Rx58).	**RINLV7AS[2:0]**
3	—	0	**Reserved**	
2:0	RW	000	**Rank #7 Interleave Address Enable** See the description on Rank 0 (Rx58).	**RINLV7AEN[2:0]**

Following is an example, which shows a possible register settings for a system with 2 double-sided DIMM installed.

(i.□. Rx53[3:2] (RINLV1SEL_[1:0]) = 2 and Rx53[1:0] (RINLV0SEL_[1:0])=2 selects A6, A18, A19 as the Rank Interleave Address for the system.

(2) If the settings on the Rank Interleave Address Selection of Rank 0, 1, 2, 3 (Rx58-5B[6:4]) are
Rx58[6:4] (RINLV0AS) = 001b
Rx59[6:4] (RINLV1AS) = 000b
Rx5A[6:4] (RINLV2AS) = 010b
Rx5B[6:4] (RINLV3AS) = 011b

And if the Rank Interleave Address Enable of Rank 0, 1, 2, 3 (Rx58-5B[2:0]) are
Rx58[2:0] (RINLV0AEN) = 011b
Rx59[2:0] (RINLV1AEN) = 011b
Rx5A[2:0] (RINLV2AEN) = 011b
Rx5B[2:0] (RINLV3AEN) = 011b

With the above register settings, Rank Interleave Address 2, A6, is ignored for the system, and the four ranks of the system are decided by A18 and A19 as shown in the following table.

A18	A19	Selected Rank
0	0	Rank#1
0	1	Rank#0
1	0	Rank#2
1	1	Rank#3

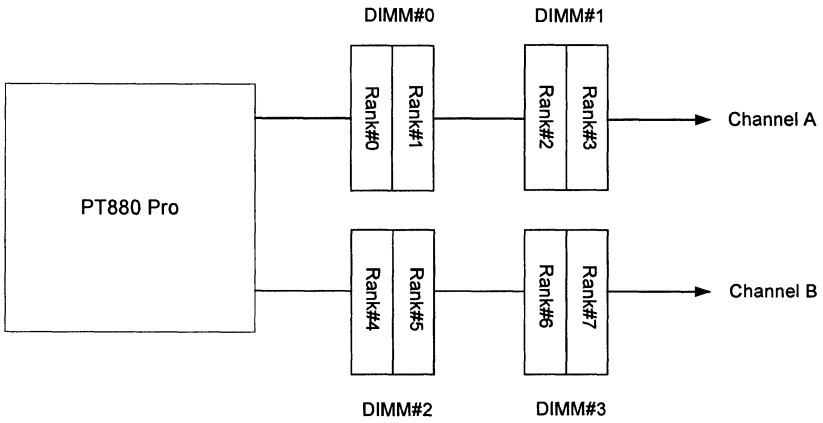


Figure 4. DIMM / Channel Mapping Diagram

DRAM Timing (60–64h)

Offset Address: 60h (D0F3)

DRAM Pipeline Turn-Around Setting **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**0ws Back-to-Back Write to Different DDR Rank** 0: Disable 1: Enable
6	RW	0	**Fast Read-to-Read Turn Around** 0: Disable 1: Enable (DQS post-amble overlap with preamble)
5	RW	0	**Fast Read-to-Write Turn Around** 0: Disable 1: Enable
4	RW	0	**Fast Write-to-Read Turn Around** 0: Disable 1: Enable
3:2	—	00	**Reserved**
1	RW	0	**0ws DRAM Channel Switching Between Read Cycles** 0: Disable 1: Enable This function is valid in 64-Bit mode.
0	RW	0	**0ws DRAM Channel Switching Between Write Cycles** 0: Disable 1: Enable This function is valid in 64-bit mode.

Offset Address: 61h (D0F3)

DRAM Timing for All Ranks **Default Value: 44h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Write Recovery Time (tWR) –** 00: 2T 01: 3T 10: 4T 11: 5T
5:0	RW	04h	**Refresh-to-Active or Refersh-to-Refresh (tRFC)** 00: 8T 01h: 9T … 0nh: (8+n)T 3eh: 70T 3f:h: 71T

Offset Address: 62h (D0F3)
DRAM Timing for All Ranks **Default Value: 21h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**Active-to-Precharge (tRAS)** 0000: 5T 0001: 6T ... 0nh: (5+n)T 1110: 19T 1111: 20T
3	RW	0	**Enable DDR2 8-Bank Device Timing Constraint (tRRD and tRP).**
2:0	RW	001	**CAS Latency** DDR DDR2 000 1.5 2 001 2 3 010 2.5 4 011 3 5 1xx reserved reserved

Offset Address: 63h (D0F3)
DRAM Timer for All Ranks **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Active-to-Active Period (tRRD)** 00: 2T 01: 3T 10: 4T 11: 5T
5:4	—	00	**Reserved**
3	RW	0	**Read-to-Precharge Delay (tRTP)** 0: 2T 1: 3T
2	—	00	**Reserved**
1	RW	0	**Write to Read Command Delay (tWTR)** DDR DDR2 0 1T 2T 1 2T 3T
0	—	0	**Reserved**

Offset Address: 64h (D0F3)
DRAM Timer for All Ranks **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00	**Active to Read or Write Delay (tRCD)** 00: 2T 01: 3T 10: 4T 11: 5T
5	—	00	**Reserved**
4	RW	0	**CKE Minimum Pulse Width** 0: 2T 1: 3T This function is valid when RDYNCKE=1 (Fun4 RxA1[6])
3:2	RW	01	**Precharge Period (tPR)** 00: 2T 01: 3T 10: 4T 11: 5T
1	—	00	**Reserved**
0	RW	0	**Exit Precharge/Active Power Down to Any Command Delay** 0: 1T 1: 2T This function is valid when RDYNCKE=1 (Fun 4 RxA1[6])

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)
DRAM Arbitration Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Timer** (unit of 4 DCLKS) DRAMC time slot allocated for AGP device.
3:0	RW	0	**Host Timer** (unit of 4 DCLKS) DRAMC time slot allocated for Host.

Offset Address: 66h (D0F3)
DRAM Queue / Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**DRAMC Queue Size Greater Than 2** 0: No 1: Yes	
6	RW	0	**DRAMC Queue Size Not Equal To 4** 0: No 1: Yes To setup DRAMC queue size of 2, set Rx66[7:6] to 2'b00; sets Rx66[7:6] to 2'b11 for queue size of 3; sets Rx[7:6] to 2'b10 for queue size of 4.	
5:4	RW	00	**Arbitration Parking Policy** 00: Park at the last bus owner 01: Park at CPU 10: Park at AGP 11: Reserved	
3:0	RW	0000	**Priority Promotion Timer** (in unit of 4 DCLKs) A DRAM request is promoted to become a high priority request when it is pending over PTIM*4 DRAM cycles.	**PTIM[3:0]**

Offset Address: 67h (D0F3)
DIMM Command / Address Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**DIMM 3 Command / Address Selection** 00: SCMD/MA Bus A; 01: SCMD/MA Bus B 10: Reserved 11: Reserved
5:4	RW	0	**DIMM 2 Command / Address Selection**
3:2	RW	0	**DIMM 1 Command / Address Selection**
1:0	RW	0	**DIMM 0 Command / Address Selection**

DRAM Control (68–69h)

Offset Address: 68h (D0F3)
DDR Page Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Page Register Life Timer (in unit of 16 DCLKs)** When timer expired, the expired page will be closed.
3:0	RW	0000	**DRAM Expired Page Threshold** Close expired pages with precharge-all command when the number of expired pages exceeds the value.

Offset Address: 69h (D0F3)
DDR Page Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Bank Interleave** 00: No interleave 01: 2-bank 10: 4-bank 11: 8 bank
5	RW	0	**Enable Bank Address Scramble** When set to 1, BA0=A13^A15^A17^A19, BA1=A12^A14^A16^A18^A20
4	RW	0	**Auto-Precharge for TLB Read and CPU Write-Back** 0: Disable 1: Enable
3:2	—	0	**Reserved**
1	RW	0	**Keep Page Active When Cross Bank** 0: Disable 1: Enable
0	RW	0	**Multiple Page Mode** 0: Disable 1: Enable

Refresh Control (6A–6Bh)

Offset Address: 6Ah (D0F3)
Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter** (in unit of 16 DRAM CLKs) When set to 00, DRAM refresh is disabled

Offset Address: 6Bh (D0F3)
DRAM Miscellaneous Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**DQS Input DLL Adjustment** 0: Disable 1: Enable
6	RW	0	**DQS Output DLL Adjustment** 0: Disable 1: Enable
5	RW	0	**Burst Refresh** 0: Disable 1: Enable
4	RW	1	**DLL Manual Reset** 0: Disable 1: Enable
3	RW	0	**Enable Memory Size Detection, MA 32/16 33/17 Swap** 0: Disable 1: Enable
2:0	RW	0	**SDRAM Operation Mode Select** 000: Normal SDRAM Mode 001: NOP Command Enable 010: All-Banks-Precharge Command Enable. 011: MRS to SCMD 100: CBR, CAS-before-RAS refresh, Cycle Enable 101: Reserved 11x: Reserved

DDR SDRAM Control (6C–6Fh)

Offset Address: 6Ch (D0F3)

DRAM Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 DRAM Support** 0: Disable DDR2 1: Enable DDR2
6	RO	—	**Memory Type Detected (through ball: MEMDET)** 0: DDR 1: DDR2
5	RO	—	**128-Bit DRAM Mode** 0: Disable 128-bit DRAM mode 1: Support 128-bit DRAM mode
4	RW	0	**Disable DQM balls**
3	RW	0	**SDRAM Effective Burst Length** For 128-bit mode ranks, SDRAM MRS 0: Not support 1: BL4 For 64-bit mode ranks, SDRAM MRS 0: BL4 1: BL8
2:1	—	0	**Reserved**
0	RW	0	**Registered DIMM** 0: Disable (i.e. supports unbuffered DIMM) 1: Enable

Offset Address: 6Dh (D0F3)

DQ Channel Select **Default Value: C0h**

Bit	Attribute	Default	Description
7	RW	1	**DQ Channel Select for DIMM#3** 0: Channel A 1: Channel B
6	RW	1	**DQ Channel Select for DIMM#2** 0: Channel A 1: Channel B
5	RW	0	**DQ Channel Select for DIMM#1** 0: Channel A 1: Channel B
4	RW	0	**DQ Channel Select for DIMM#0** 0: Channel A 1: Channel B
3:2	—	00	**Reserved**
1	RW	0	**Enable MA Bus C Inversion (except MAC10)**
0	RW	0	**Enable MA Bus B Inversion (except MAB10)**

Note: If ODT is not supported, the registers can be programmed, i.e. the function of MD/CS mapping can work.

Offset Address: 6Fh (D0F3)

Miscellaneous Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Non-ONBD Protection for GART Table Fetching** 0: Disable 1: Enable
6	RW	1	**DRAM-Side-Input-Pointer Non-Return-Zero Mode** 0: Disable 1: Enable Enable to avoid overwrite data
5	RW	0	**Disallow the 2nd Cycle of a 2T Command Overlapped with Command of Different Type on a Different MA/SCMD Bus** 0: Allow 1: Not allow Sets this bit to 1 when read-modify-write mode is enabled (for example, ECC mode).
4	RW	0	**Read-Modify-Write (RMW) Option** When enabled, RMW is processed in relaxed mode.
3	RW		**Applying Same-Channel IO Turn-Around Constraints between Different Channels**
2	RW	0	**Exclusive SCMD Buses** When enabled, the two SCMD buses are exclusive, do not have commands in the same cycle.
1	—	0	**Reserved**
0	RW	0	**GART Table Access Option** When enabled, GART Table accessing is in relaxed mode. Set this bit to 1 in DDR400 mode.

DRAM Signal Timing Control (70–7Fh)

Offset Address: 73 – 70h (D0F3)
MD / DQS Output Delay Control — **Default Value: 00000000h**

Offset Address	Attribute	Default	Description
73h	RW	0	**Channel B MD Output Delay**
72h	RW	0	**Channel B DQS Output Delay**
71h	RW	0	**Channel A MD Output Delay**
70h	RW	0	**Channel A DQS Output Delay**

Note: these delay registers are in unsigned binary format.

Offset Address: 74h (D0F3)
DQS Output Clock Phase Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	000	**Initial Phase of Internal Clocks for DQS Output on Channel B** Each steps increase a phase of 1/8 T
3	—	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQS Output on Channel A** Each steps increase a phase of 1/8 T

Offset Address: 75h (D0F3)
DQ Output Clock Phase Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	000	**Initial Phase of Internal Clocks for DQ Output on Channel B** Each steps increase a phase of 1/8 T
3	—	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQ Output on Channel A** Each steps increase a phase of 1/8 T

Offset Address: 76h (D0F3)
Write Data Phase Control — **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**1 More Pipeline Stage on Write Data Path**	**RDWPIPE**
6	—	0	**Reserved**	—
5	RW	0	**DQ/DQS Output Clocks Bypass Delay Component**	
4	—	0	**Reserved**	—
3:2	RW	00	**Advance Write Phase Signals to Make Room for the Long Bus Delay** 00: Normal mode 01: Advance 1 cycle 10: Advance 2 cycle 11: Forbidden The 2 bits must be used with Bit [1:0] (RDWPH[1:0]).	**RDWADV[1:0]**
1:0	RW	00	**Write MD/DQS/CAS Output Timing Range Control** Each increased step delays the output range by 1/4 T.	**RDWPH[1:0]**

Offset Address: 77h (D0F3)
DQS Input Delay Calibration — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Manual DQS Input Delay Setting** 0:Auto 1: Manual
6	—	0	**Reserved**
5:0	RW	0	**DDR DQS Input Delay** This is the base delay value of DQS input signal in unsigned binary format. The reading value depends on Rx77[7]. If Rx77[7] = 0 (auto mode), DLL calibration result is returned when read.

Offset Address: 78h (D0F3)
Channel A DQS Input Capture Range Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**Manual DQS Input Capture Range Setting for Channel A** 0: Auto 1: Manual
6	RW	0	**Enable DQS Input Capture Range Detection for Channel A**
5:0	RW	00	**DQS Input Capture Range for Channel A** **Bit [5:4]** 00: 1T prior to 1st DQS rising edge 01: at 1st DQS rising edge 10: 1T after 11: Reserved **Bit [3:1] 1/8T delay** **Bit [0] 0.35ns fine tune delay**

Offset Address: 79h (D0F3)
Channel B DQS Input Capture Range Control **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**Manual DQS Input Capture Range Setting for Channel B** 0: Auto 1: Manual
6	RW	0	**Enable DQS Input Capture Range Detection for Channel B**
5:0	RW	00	**DQS Input Capture Range for Channel B**

Offset Address: 7Ah (D0F3)
DQS Input Capture Range Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Select DQS Input Ball as Input Capture Range Detection Signal** 0: DQSB0 1: DQSB4
6:4	RW	000	**DQS Input Capture Range Offset Value for Channel B** 1/8T per step, 2's complement
3	RW	0	**Select DQS Input Ball as Input Capture Range Detection Signal** 0: DQSA0 1: DQSA4
2:0	RW	000	**DQS Input Capture Range Offset Value for Channel A** 1/8T per step, 2's complement

Offset Address: 7Bh (D0F3)
Read Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	000	**MD Input Data Push Timing Control** 00: Start moving data into internal buffer 1T after the 1st DRAM strobe 01: 1.5T 10: 2T 11: 2.5T
3:1	—	0	**Reserved**
0	RW	0	**Extend DQS Input Capture Range 1/2T Earlier**

Read-Only Control (7C-7Fh)

Offset Address: 7Ch (D0F3)
Channel A DQS Input Delay Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:0	RW	0	**Channel A DQS Input Delay Offset (In two's complement)** This is the offset values (in 2's complement format) from the base delay value (Rx77[5:0]) for Channel A DIMM.

Offset Address: 7Eh (D0F3)
Channel B DQS Input Delay Offset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:0	RW	0	**Channel B DQS Input Delay Offset (In two's-complement).** This is the offset values (in 2's complement format) from the base delay value (Rx77[5:0]) for Channel B DIMM.

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)
Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**C8000-CBFFFh Memory Space Access Control**
3:2	RW	00	**C4000-C7FFFh Memory Space Access Control**
1:0	RW	00	**C0000-C3FFFh Memory Space Access Control**

Offset Address: 81h (D0F3)
Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**D8000-DBFFFh Memory Space Access Control**
3:2	RW	00	**D4000-D7FFFh Memory Space Access Control**
1:0	RW	00	**D0000-D3FFFh Memory Space Access Control**

Offset Address: 82h (D0F3)
Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00	**E8000-EBFFFh Memory Space Access Control**
3:2	RW	00	**E4000-E7FFFh Memory Space Access Control**
1:0	RW	00	**E0000-E3FFFh Memory Space Access Control**

Offset Address: 83h (D0F3)

Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5:4	RW	00	**F0000-FFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable	
3:2	RW	00	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)	
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM Mode** 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: (i.□. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.	**RABKDOFF**
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of RABKDOFF (bit 1), the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.	**RRWABK**

Table 10. CPU-to-SMRAM Cycle Flow

RABKDOFF (Rx83[1])	RRWABK (Rx83[0])	CPU MODE	Target of CODE Access Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

DRAM Above 4G Support (84-8D)

Offset Address: 84h (D0F3)

Low Top Address – Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Low Top Address - A[23:20]**
3:0	—	0000	**Reserved**

Offset Address: 85h (D0F3)

Low Top Address – High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – A[31:24]**

Offset Address: 86h (D0F3)
SMM and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable	
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh – FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh – FEC8_0000h access cycles are passed to PCI2.	RAPIC2
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping	
2	RW	0	**Top 1MB SM Memory Enable** 0: Disable 1: Enable TSMMA[31:20] = {LOWTOPA[31:24],4'h0} – {FBSZ[2:0],1'b0}; OSLOWTOPA[31:20] = TSMMA[31:20] – RTSMMEN	RTSMMEN
1	—	0	**Reserved**	
0	RW	1	**Compatible SMM Enable** 0: Disable 1: Enable	RCSMMEN

Offset Address: 89-88h (D0F3)
Misc. DRAM Address Setting **Default Value:0000h**

Bit	Attribute	Default	Description
15:11	—	0	**Reserved**
10:0	RW	0	**The Address Next to the Last Valid DRAM Address**

Offset Address: 8Ch (D0F3)
DQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:2	—	0	**Reserved**	
1	RW	0	**MD/DQS Earlier Output Enable** MDOE 1/2T earlier DQSOE 1/2T earlier if Bit 0 (RDSOLNGPRE)=0	RDSOLNGPRE2
0	RW	0	**DQS Earlier Output Enable** DQSOE 1/4T earlier if Bit 1 (RDSOLNGPRE2)=1	RDSOLNGPRE

DRAM Clocking Control (90-9F)

Offset Address: 90h (D0F3)
DRAM Clock Operation Mode and Frequency **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**DCLK Switch to Non-Feedback Mode** 0: Feedback mode 1: Non-feedback mode (feed-forward mode). There is no need to feed DCLKO back through MCLKIN port.	RNODCLKIN
6:3	—	0	**Reserved**	
2:0	RW	000	**DRAM Operating Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: Reserved 110/111: Reserved	

Offset Address: 91h (D0F3)
DCLK (MCLK) Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	000	**DCLKOB Phase Select for Rx90[7] (RNODCLKIN) =1 Mode** Each step increases 1/8T
3	—	0	**Reserved**
2:0	RW	000	**DCLKOA Phase Select** Each step increases 1/8T

Offset Address: 92h (D0F3)
CS/CKE Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
6:4	RW	0	**Channel B Sampling Clock Phase Select for CS/CKE** Each step increases a phase of 1/8 T
3	RW	0	**Reserved**
2:0	RW	0	**Channel A Sampling Clock Phase Select for CS/CKE** Each step increases a phase of 1/8 T

Offset Address: 93h (D0F3)
SCMD/MA Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
6:4	RW	0	**Channel B Sampling Clock Phase Select for SCMD/MA** Each step increases a phase of 1/8 T
3	—	0	**Reserved**
2:0	RW	0	**Channel A Sampling Clock Phase Select for SCMD/MA** Each step increases a phase of 1/8 T

Offset Address: 94h (D0F3)
DCLKO Feedback Mode Output Control **Default Value: 01h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6:4	RW	000	**DCLKO Feedback Mode Output Control** For Rx90[6] (RNODCLKIN) = 0 mode, if DCLKOA is fed back to DCLKIA, each increased step delays DCLKOB; if DCLKOB is fed back to DCLKIA, each increased step makes DCLKOA earlier (1/8T per step).
3	—	0	**Reserved**
2:0	RW	001	**DCLKO Feedback Mode Output Control** For Rx90[6] (RNODCLKIN) = 0 mode, if DCLKOA is fed back to DCLKIA, each increased step makes DCLKOB earlier; if DCLKOB is fed back to DCLKIA, each increased step delays DCLKOA (1/8T per step).

DDR2 – I/O Pad Control (D0–D3h)

Offset Address: D0h (D0F3)
DQ / DQS Termination Strength Manual Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQ/DQS Pull-up Termination Strength Manual Setting**
3:0	RW	0	**DQ/DQS Pull-down Termination Strength Manual Setting**

Offset Address: D1h (D0F3)
DQ / DQS Termination Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ/DQS Pull-up Termination Strength Auto-comp Value**
3:0	RO	0	**DQ/DQS Pull-down Termination Strength Auto-comp Value**

Offset Address: D2h (D0F3)
DQ Driving Strength Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ Pull-up Driving Strength Auto-comp Value**
3:0	RO	0	**DQ Pull-down Driving Strength Auto-comp Value**

Offset Address: D3h (D0F3)
Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	0	**Reserved**
1	RW	0	**DDR Compensation Auto Mode** 1: Disable Auto Mode 0: Enable Auto Mode If DDR Compensation and DDR Auto Compensation are both enabled, the ODT settings for all DRAM pads are from auto-comp circuit (RxD1); otherwise, if Auto Compensation is disabled, the ODT settings are from manual setting (RxD0).
0	RW	0	**DDR Compensation** 1: Enable 0: Disable Disable DDR Compensation provides a power saving mode, however, the values of RxD1 and RxD2 should be ignored.

Note: The DQ driving bits of RxD2 is the result of the auto-comp circuit; however, there is no "auto-mode" for the DQ/DQB driving control since it depends on the actual number of ranks in the DRAM data channel

DDR2 – ODT Control (D4–D7h)

Offset Address: D4h (D0F3)
ODT Pullup / Pulldown Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**NB Pad ODT** 1: Enable ODT when reading data 0: Disable ODT unless RxD4[3:0] is not equal to 0
6:4	—	0	**Reserved**
3	RW	0	**ODT Pullup Enable**
2	—	0	**Reserved**
1	RW	0	**ODT Pulldown Enable**
0	—	0	**Reserved**

Offset Address: D5h (D0F3)
ODT Driving and Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Channel-A DQ ODT Driving Select** 0: Weak driving, for DDR or DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
6	RW	0	**Channel-B DQ ODT Driving Select**
5	RW	0	**Channel-A DQS ODT Driving Select**
4	RW	0	**Channel-B DQS ODT Driving Select**
3	RW	0	**Channel-A DQ ODT Range Select** 1: 75 ohm 0: 150 ohm
2	RW	0	**Channel-B DQ ODT Range Select** 1: 75 ohm 0: 150 ohm
1	RW	0	**Channel-A DQS ODT Range Select** 1: 75 ohm 0: 150 ohm
0	RW	0	**Channel-B DQS ODT Range Select** 1: 75 ohm 0: 150 ohm

Offset Address: D6h (D0F3)
ODT Driving and Range Select — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCLKOA ODT Driving Select (DS)**
6	RW	0	**DCLKOB ODT Driving Select (DS)**
5	RW	0	**SCMD/MAA Driving Select**
4	RW	0	**SCMD/MAB Driving Select**
3	RW	0	**CKEA Driving Select**
2	RW	0	**CKEB Driving Select**
1	RW	0	**CKEA ODT Range Select (RS)**
0	RW	0	**CKEB ODT Range Select (RS)**

Offset Address: D8h (D0F3)
ODT Lookup Table for Channel A — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Rank 3 ODT Signal Selection** 00:ODTA0 01: ODTA1 10:ODTA2 11: ODTA3
5:4	RW	0	**Rank 2 ODT Signal Selection**
3:2	RW	0	**Rank 1 ODT Signal Selection**
1:0	RW	0	**Rank 0 ODT Signal Selection**

Offset Address: D9h (D0F3)
ODT Lookup Table for Channel B — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Rank 7 ODT Signal Selection** 00:ODTB0 01: ODTB1 10:ODTB2 11: ODTB3
5:4	RW	0	**Rank 6 ODT Signal Selection**
3:2	RW	0	**Rank 5 ODT Signal Selection**
1:0	RW	0	**Rank 4 ODT Signal Selection**

Offset Address: Dah (D0F3)
SDRAM ODT Control — **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**DDR2 SDRAM ODT Control** 0: Disable 1: Enable	**RODTEN**
6	RW	0	**2T Write Command when Rx50 (RCMDIT) =1** 0: Disable 1: Enable	**RODTCMD2T**
5	RW	0	**Add MD Bus Turn Around Wait State for DDR2 ODT** 0: Disable 1: Enable	**RODTTAR**
4:2	—	0	**Reserved**	
1	RW	0	**Channel B Differential DQS Input** 0: Disable 1: Enable	**RDQSDFB**
0	RW	0	**Channel A Differential DQS Input** 0: Disable 1: Enable	**RDQSDFA**

Offset Address: DCh (D0F3)
Channel A DQ/DQS CKG Output Delay Control — **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group A3** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group A2**
3:2	RW	00	**DQ/DQS Delay Control for Group A1**
1:0	RW	00	**DQ/DQS Delay Control for Group A0**

Offset Address: DDh (D0F3)
Channel A DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group A7** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group A6**
3:2	RW	00	**DQ/DQS Delay Control for Group A5**
1:0	RW	00	**DQ/DQS Delay Control for Group A4**

Offset Address: Deh (D0F3)
Channel B DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group B3** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group B2**
3:2	RW	00	**DQ/DQS Delay Control for Group B1**
1:0	RW	00	**DQ/DQS Delay Control for Group B0**

Offset Address: DFh (D0F3)
Channel B DQ/DQS CKG Output Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQ/DQS Delay Control for Group B7** 00: Default 01: Delays100ps 10: Delays 200ps 11: Delays 300ps
5:4	RW	00	**DQ/DQS Delay Control for Group B6**
3:2	RW	00	**DQ/DQS Delay Control for Group B5**
1:0	RW	00	**DQ/DQS Delay Control for Group B4**

DRAM Driving Control (E0–EFh)

Table 11. Physical Ball to Driving Group Mapping Table

Physical Balls	DCLK[A, B]	CKE[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	MPD/DQM[A, B]
Driving Group	DCLK[A, B]	CS[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	DQ[A, B]

Offset Address: E0h (D0F3)
DRAM Driving – Group DQSA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSA – PMOS Driving**
3:0	RW	0	**DQSA – NMOS Driving**

Offset Address: E1h (D0F3)
DRAM Driving – Group DQSB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSB – PMOS Driving**
3:0	RW	0	**DQSB – NMOS Driving**

Offset Address: E2h (D0F3)
DRAM Driving – Group DQA (MD, MPD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQA – PMOS Driving**
3:0	RW	0	**DQA – NMOS Driving**

Offset Address: E3h (D0F3)
DRAM Driving – Group DQB (MD, MPD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	DQB – PMOS Driving
3:0	RW	0	DQB – NMOS Driving

Offset Address: E4h (D0F3)
DRAM Driving – Group CSA (CS, DQM, MPD) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	CSA – PMOS Driving
3:0	RW	0	CSA – NMOS Driving

Offset Address: E5h (D0F3)
DRAM Driving – Group CSB (CS, DQM, MPD) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	CSB – PMOS Driving
3:0	RW	0	CSB – NMOS Driving

Offset Address: E6h (D0F3)
DRAM Driving – Group DCLKA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	DCLKA – PMOS Driving
3:0	RW	0	DCLKA – NMOS Driving

Offset Address: E7h (D0F3)
DRAM Driving – Group DCLKB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	DCLKB – PMOS Driving
3:0	RW	0	DCLKB – NMOS Driving

Offset Address: E8h (D0F3)
DRAM Driving – Group MAA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	MAA – PMOS Driving
3:0	RW	0	MAA – NMOS Driving

Offset Address: E9h (D0F3)
DRAM Driving – Group MAB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	MAB – PMOS Driving
3:0	RW	0	MAB – NMOS Driving

Offset Address: Ech (D0F3)
Channel-A DQS / DQ CKG Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: Edh (D0F3)
Channel-B DQS / DQ CKG Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: Eeh (D0F3)
DCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Duty Control for DCLKA** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00	**Duty Control for DCLKA** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00	**Duty Control for DCLKB** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00	**Duty Control for DCLKB** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EFh (D0F3)
DQS CKG Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5:4	RW	00	**Duty Control for DQSA** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps
3:2	—	0	**Reserved**
1:0	RW	00	**Duty Control for DQSB** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps

Device 0 Function 4 (D0F4): Power Management Control

Header Registers

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	4308h	**Device ID – Power Management Control**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0200h	**PCI Status**
8h	RO	00	**Revision ID**
0B – 9h	RO	060000h	**Class Code**
0Dh	RO	00	**Latency Timer**
0Eh	RO	00	**Header Type**
0Fh	RO	00	**BIST**
13-10h	—	—	**Reserved**
2D – 2Ch	RW1	00	**Subsystem Vendor ID**
2F – 2Eh	RW1	00	**Subsystem ID**
33 – 30h	RO	00	**Reserved**
37 – 34h	RO	0000	**Capability Pointer**
3F – 38h	—	—	**Reserved**

Power Management Control (A0–EFh)

Offset Address: A0h (D0F4)

Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6	RW	0	**Power Management during HALT / SHUTDOWN** 0: Disable 1: Enable
5	RW	0	**Power Management during STPCLK** 0: Disable 1: Enable
4	RW	0	**Power Management during SUSSTAT** 0: Disable 1: Enable
3:0	—	0	**Reserved**

Offset Address: A1h (D0F4)

DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DRAM Self-Refresh During Power-Management Mode** 0: Disable 1: Enable
6	RW	0	**Dynamic CKE When DRAM Idle** 0: Disable 1: Enable Note: Before entering STR Mode, please turn off this bit
5	RW	0	**Dynamic DRAM I/O Pad Power-Down** (i.e. float) 0: Disable 1: Enable
4:0	—	0	**Reserved**

Note: The DRAM power management mode is defined as HALT / SHUTDOWN, STPCLK and SUSSTAT triggered

Offset Address: A2h (D0F4)
Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Interface Power Management** 0: Disable 1: Enable
5	RW	0	**V-Link Interface Power Management** 0: Disable 1: Enable
4	RW	0	**AGP Interface Power Management** 0: Disable 1: Enable
3	RW	0	**PCI2 Interface Power Management** 0: Disable 1: Enable
2	RW	0	**Graphics Interface (GMINT) Power Management** 0: Disable 1: Enable
1	RW	0	**VKCFG Interface Power Management** 0: Disable 1: Enable
0	RW	0	**Host Fast Power-Management (DADS Fast Timing)** 0: Disable 1: Enable

Offset Address: A3h (D0F4)
MA / SCMD Pad Toggle Reduction **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**MA / SCMD Toggle Reduction** (i.e. do not switch MA / SCMD if not accessed) 0: Disable 1: Enable
6:0	—	0	**Reserved**

Offset Address: A8h (D0F4)
PCIe Dynamic Clock Stop **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Dynamic Clock STOP of PEG Port for PHY**
6	—	0	**Reserved**
5	RW	0	**Central Traffic Controller Dynamic Clock STOP** 0: Disable 1: Enable
4	RW	0	**Enable Dynamic Clock STOP for PEG Port**
3:0	—	0	**Reserved**

Offset Address: DF-D0h (D0F4)
BIOS Extended Scratch Registers D **Default Value: 00h**

Offset Address	Attribute	Default	Description
DF – D0h	RW	0	**BIOS Extended Scratch Registers D**

Offset Address: EF-E0h (D0F4)
BIOS Extended Scratch Registers E **Default Value: 00h**

Offset Address	Attribute	Default	Description
EF – E0h	RW	0	**BIOS Extended Scratch Registers E**

Device 0 Function 5 (D0F5): APIC and Central Traffic Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	5308h	**Device ID – for Power Management Control**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0000h	**PCI Status**
8h	RO	00	**Revision ID**
0B – 9h	RO	080020h	**Class Code**
0Dh	RO	00	**Latency Timer**
0Eh	RO	80	**Header Type**
0Fh	RO	00	**BIST**
13-10h	—	—	**Reserved**
2D – 2Ch	RW1	00	**Subsystem Vendor ID**
2F – 2Eh	RW1	00	**Subsystem ID**
33 – 30h	RO	00	**Reserved**
37 – 34h	RO	00	**Capability Pointer**
3F – 38h	—	—	**Reserved**

Legacy APIC Base I/O Registers (40–5Fh)

Offset Address: 40h (D0F5)

APIC Legacy Configuration — **Default Value: 4Ch**

Bit	Attribute	Default	Description
7	RW	0	**Legacy APIC** 0: Disable 1: Enable; Range FECxyz00 to FECxyzFF, where x,y,z are defined in Rx40[3:0] and Rx41[7:0]
6	RW	1	**Reserved**
5	RW	0	**Issues MSI Cycle for the Interrupt Deassertions** 0: Disable, there will be no corresponding MSI cycle for IRQ deassertion 1: Enable, IRQ assertion and de-assertion will both issue MSI cycle out
4	—	0	**Reserved**
3:0	RW	0Ch	**APIC Legacy Address Range - x**

Offset Address: 41h (D0F5)

APIC Legacy Address Range – y / z — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**APIC Legacy Address Range - y**
3:0	RW	0	**APIC Legacy Address Range - z**

Offset Address: 42h (D0F5)

APIC BT_INTR Control — **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	**Disable INTx Transparent Mode** 0: Enable Transparent mode 1: Disable Transparent mode
2	RW	0	**APIC Nonshare Mode Enable**
1	RW	1	**BTIDIS Function of the APIC Module** 0: Disable 1: Enable
0	RW	1	**BT_INTR Function** 0: Disable 1: Enable

Offset Address: 44h (D0F5)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW	0	**APIC Data Voltage for CPU Voltage Select** 0: 2.5V 1: 1.5V

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)
Extended CFG Address Support **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	—	0	**Reserved**
5	RW	1	**Convert Device2 CF8 Cycles to Device1 while Passing it to the SB (in PCIe Mode)** 0: CF8 access cycles are passed to the SB normally 1: CF8 with data[15:11]=00010 will be changed to data[15:11]=00001
4	RW	0	**CF8 Byte Write Enable** 0: Only supports CF8 write with all BE active 1: Allow CF8 write with partial BE active
3	RW	0	**For Device 2 and Device 3, Configuration Cycles to the Secondary Bus behind the P2P Bridge** 0: Configuration cycles for all the devices will be passed through. 1: Only configuration cycles for device 0 will be passed to the secondary bus.
2	—	0	**Reserved**
1:0	RW	0	**Extended CFG Mode** 00: Extended CFG mode is off 01: Reserved 10: Capability header for extended configuration address support 11: Memory mapped extended CFG address supported (Rx61[7:0] should also be programmed.)

Offset Address: 61h (D0F5)
Memory Mapped Extended CFG Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	—	0	**Extended Configuration Address: A[35:28]** 00h: No extended configuration address Else: Extended configuration address A[35:28] from host side

Offset Address: 62h (D0F5)
Memory Mapped Extended RCRB Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	—	0	**RCRB Base Address** 00h: no RCRB is supported

Offset Address: 64h (D0F5)

Miscellaneous **Default Value: 13h**

Bit	Attribute	Default	Description
7:5	—	0	**Reserved**
4	RW	1	**Downstream C2P Forces Flush of the Upstream P2C Write to the Host Side before Return LRDY to the Host Side** 0: Disable 1: Enable Note: C2P Downstream cycles include MEMR, IOR and IOW
3:2	—	0	**Reserved**
1	RW	1	**Downstream Write Request Timing** 0: Wait for the write data to issue downstream request 1: Issue downstream request once request from the host is received
0	RW	1	**Traffic Controller Downstream Cycles Are Processed in Order** 0: Disable; Downstream post write transaction won't be issued out until the data phase of the previous read transaction is finished 1: Enable; Downstream post write transaction can be issued out before the completion of the data phase of the previous read transaction

Central Traffic - Upstream Control (80h)

Offset Address: 80h (D0F5)

Central Traffic-Upstream Control **Default Value: 18h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**VC1 Upstream Path** 0: VC1 requests are forwarded to the host side (snoop) 1: VC1 requests are forwarded to the DRAMC side. Those required snoops are reported as MalFunction TLPs.
5	RW	0	**CPU-to-Memory FIFO Snoop Policy for Upstream Request to DRAMC** 0: Upstream requests are sent to DRAMC directly 1: Upstream requests to DRAMC have to wait for the snoop result from CPU-to-Memory FIFO. When hit, DRAMC will postpone handling these upstream requests till cycles in the CMFIFO been flushed to the DRAM.
4	RW	1	**AGP Upstream Path** 0: AGP requests are forwarded to the host side (snoop) 1: AGP requests are forwarded to the DRAMC side
3	RW	1	**TPQPush, TPQPop 1T early** 0: Normal latency for upstream request 1: Reduced 1T latency for upstream request
2	RW	0	**Host Side Upstream Write** Transaction end with 1T earlier notice 0: Disable 1: Enable
1	RW	0	**Host Side Upstream Read Data Returning Path** 0: 2 levels of synchronous FIFO 1: 1 level synchronous FIFO.
0	RW	0	**Host Side Upstream Write, Data Return With a 1T Notice** 0: Disable 1: Enable

Offset Address: 82h (D0F5)
Central Traffic-Upstream Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**PCIe VC1 Read/Write Ordering Rule** 0: Obey PCIe VC1 read/write ordering rule 1: PCIe VC1 read cycle can pass VC1write cycle
4	RW	0	**PCIe VC1 Command Rate** 0: PCIe VC1 read/write 2T command rate 1: PCIe VC1 read 2T command rate, but write 1T command rate
3	RW	0	**AGP Read/Write Ordering Rule** 0: Obey AGP read/write ordering rule 1: AGP read cycle can pass AGP write cycle
2	RW	0	**AGP Command Rate** 0: AGP read/write 2T command rate 1: AGP read 2T command rate, but, write 1T command rate
1	RW	0	**Fair arbitration latency for the host side arbitration unit at D0F0 extended register space Rx230 ~ Rx23D.** 0: 2T 1: 1T
0	RW	0	**Port arbitration latency for the port arbitration unit at D0F0 extended register space Rx210 ~ Rx219.** 0: 2T 1: 1T

PCIe Message Controller and Power Management (A0–F0h)

Offset Address: A0h (D0F5)
PCIe PMU Control and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**PEWAKE# Activation Control** 0: PEWAKE# function is disabled. 1: PEWAKE# function is enabled.
6:5	—	0	**Reserved**
4			**PEG, a x4 Root Port, L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RxF0[7] to 1, PEG goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PEG.
3:0	—	0	**Reserved**

Offset Address: A1h (D0F5)
PCIe PMU Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PM_PME Message Status** 0: No PM_PME message 1: At least one PM_PME message was received at the PCIe ports. Note: Wake up the system through either PEWAKE# depends on the settings on RxA0[7].
6:0	—	0	**Reserved**

Offset Address: A2h (D0F5)
PMU Downstream Address [15:8] **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Downstream Address Bits [15:8]** This register is used for monitoring S3/S4/S5 downstream command. Refers to RxA3[7] for address [7].

Offset Address: A3h (D0F5)
PMU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Address Bit [7]** This bit is used for monitoring S3/S4/S5 downstream command. Refers to RxA2 for address [15:8].
6:1	—	0	**Reserved**
0	RW	0	**Monitor S3/S4/S5 Command** 0: Disable 1: Enable When enable, the controller will monitor S3/S4/S5 commands (e.g. IOW 4005, 'h24 or 'h28) in the following procedure: 1. The controller receives the STPGNT cycles from the CPU 2. The controller triggers MSGC to issue PME_TURNOFF message to PCIe devices (D2F0, D2Fx) 3. The controller waits for the acknowledge from all the devices to issue the STPGNT cycle received in step 1 to SB.

Offset Address: F0h (D0F5)
PMU Control **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Device Power Management Control** 0: Disable 1: Enable Programmed this bit to 1 will trigger a PME_TURNOFF message sent to PCIe Root Ports, where devices are activated. This bit has to be programmed to 0 before it can be programmed to 1 again.
6	—	0	**Reserved**
5	RW	1	**DV2 Exist or Not**
4:1	—	0	**Reserved**
0	RW	0	**Capability/Status Write of the P2P Header (D2F0, D3F0 and D3F2)** 0: Disable 1: Enable

Device 0 Function 6 (D0F6): Scratch Registers

Scratch Registers (40–7Fh)

Offset Address	Attribute	Default	Description
40-4Fh	RW	00000000	**BIOS Scratch Register**
50-5Fh	RW	00000000	**BIOS Scratch Register**
60-6Fh	RW	00000000	**BIOS Scratch Register**
70-7Fh	RW	00000000	**BIOS Scratch Register**

Device 0 Function 7 (D0F7): V-Link North Bridge and South Bridge Control

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	7358h	**Device ID – for V-Link Control**
5 – 4h	RO	0006h	**PCI Command**
7 – 6h	RO	0200h	**PCI Status**
8h	RO	00	**Revision ID**
0B – 9h	RO	060000h	**Class Code**
0Dh	RO	00	**Latency Timer**
0Eh	RO	00	**Header Type**
0Fh	RO	00	**BIST**
13-10h	—	—	**Reserved**
2D – 2Ch	RW1	00	**Subsystem Vendor ID**
2F – 2Eh	RW1	00	**Subsystem ID**
33 – 30h	RO	00	**Reserved**
37 – 34h	RO	00	**Capability Pointer**
3F – 38h	—	—	**Reserved**

V-Link Control Interface (40–B1h)

Offset Address: 40h (D0F7)

V-Link Specification ID **Default Value: 51h**

Bit	Attribute	Default	Description
7:4	RO	5h	**North Bridge V-Link Revision ID**
3:0	RO	1h	**South Bridge V-Link Revision ID** 0, 0Fh: 8-bit V-Link, the operating mode is determined by Rx48[0]. 1h: Support V-Link capability up to mode 1. 2h: Support V-Link capability up to mode 2. 3h: Support V-Link capability up to mode 3. 4h: Support V-Link capability up to mode 4. 5h: Support high priority upstream read. 6h: Support high priority upstream read / write.

Offset Address: 41h (D0F7)

NB V-Link Capability **Default Value: 3Bh**

Bit	Attribute	Default	Description	Mnemonic
7:6	—	0	**Reserved**	—
5	RO	1	**16-Bit Bus Width** 0: Not supported 1: Supported	NVK_16bit
4	RO	1	**8-Bit Width** 0: Not supported 1: Supported	NVK_8bit
3	RO	1	**4X Rate** 0: Not supported 1: Supported	NVK_4X
2	RO	0	**2X Rate** 0: Not supported 1: Supported	NVK_2X
1	RO	1	**V-Link Bus Split (native 8X mode)** 0: Not supported 1: Supported	NVK_VDSP
0	RO	1	**8X Rate** 0: Not supported 1: Supported	NVK_8X

Offset Address: 42h (D0F7)
NB Downlink (C2P) Configuration **Default Value: 88h**

Bit	Attribute	Default	Description
7:4	RW	8h	**C2P, DNCMD, Maximum Pending Request Depth** Maximum # of pending DNCMD, C2P, requests. 0000: 1 level ... 1111: 16 levels
3:0	RW	8h	**C2P Maximum Write Buffer Size (from 1 to 16 DW)**

Offset Address: 43h (D0F7)
NB Uplink (P2C) Status I **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C, UPCMD, Maximum Pending Request Depth** 0: 16 levels 1: 1 level ... n: n levels, where 0 < n <= 0Fh
3:2	—	0	**Reserved**
1:0	RO	10	**High Priority P2C Request Depth** 00: 1 level 01: 4 levels 10: 8 levels 11: 16 levels

Offset Address: 44h (D0F7)
NB Uplink (P2C) Status II **Default Value: 82h**

Bit	Attribute	Default	Description
7:4	RO	8h	**P2C Write Buffer Size (max # of lines)** 0000: 16 lines (64QW) 1000: 8 lines(32QW) 0001: 1 lines (4QW) 1111: 15 lines (60QW)
3:0	RO	2h	**P2P Write Buffer Size (max # of lines)**

Offset Address: 45h (D0F7)
NB V-Link Arbiter Timer **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**V-Link Arbiter Timer for Normal Priority Request from SB** 0000: 0 VCLK 1000: 8*4 VCLK 0001: 1*4 VCLK 1001: 16*4 VCLK 0010: 2*4 VCLK 1010: 32*4 VCLK 0011: 3*4 VCLK 1011: 64*4 VCLK 0100: 4*4 VCLK 11--: NB holds the bus as long as there is pending downstream request
3:0	RW	4h	**V-Link Arbiter Timer for High Priority Request from SB** 0000: 0 VCLK 1000: 8*2 VCLK 0001: 1*2 VCLK 1001: 16*2 VCLK 0010: 2*2 VCLK 1010: 32*2 VCLK 0011: 3*2 VCLK 1011: 64*2 VCLK 0100: 4*2 VCLK 11--: NB holds the bus as long as there is pending downstream request Note: see Table for more details

Table 8. NB V-Link Bus Arbitration

RNNTM[3:0] (Rx45[7:4])	RNHTM[3:0] (Rx45[3:0])	SB Request Priority	NB When to Relinquish the Occupied V-Link Bus
0000	xxxx	Normal / high	Immediately
0001,0010,...	0000	High	Immediately
0001,0010,...	0001,0010,...	High	Wait for either Normal or High timer expired
0001,0010,...	00xx	Normal	Wait for Normal timer expired
0001,0010,...	11xx	Normal / high	Wait for Normal timer expired
11xx	0000	High	Immediately
11xx	0000	Normal	Wait until no more pending downstream request
11xx	0001,0010,...	High	Wait for High timer expired
11xx	0001,0010,...	Normal	Wait until no more pending downstream request
11xx	11xx	Normal / high	Wait until no more pending downstream request

Offset Address: 46h (D0F7)

NB V-Link Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Downstream Read Data Return High Priority** 0: NB will not issue preamble command to SB. 1: Enable NB to issue preamble command to inform SB release V-Link for P2C Read-Request data return	**RNHIRQ**
6	RW	0	**C2P Request Priority** 0: NB will not issue preamble command to SB. 1: Enable NB to issue preamble command to inform SB release V-Link for downstream C2P request. Note: To enable this function, RNHIRQ (bit7) must be set to 1.	
5:4	RW	0	**Options of Combining Multiple STPGNT Cycles Into a V-Link Command** 00: Compatible mode: a V-Link command per STPGNT cycle 01: Combines 2 STPGNT cycles into a V-Link command 10: Combines 3 STPGNT cycles into a V-Link command 11: Combines 4 STPGNT cycles into a V-Link command	
3:2	RW	0	**V-Link Master Read/Write Access Ordering Rules** 00: High Priority Read allows to pass Normal Read (but not pass Write) 01: Read (High/Normal) allows to pass Write (High Priority R>Normal Priority R>Write) 1x: Read / Write are executed in order	**RINORDER RHRPW**
1	RW	0	**Read Around Write** 0: Read always pass Write, if RINORDER (bit3) is 0 1: Allows up to 8 Read-Around-Write cycles before flushing the pending write, if RINORDER is 0 **Read Around Write is disabled if Bit 3 (RINODER) is set to 1**	
0	RW	0	**Downstream DAC (Double Address Cycle) Cycle** 0: Disable 1: Enable	

Offset Address: 47h (D0F7)

NB V-Link Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Upstream High-Priority Write Request Stream** 0: No high-priority write request stream. 1: Enable support of high-priority write request stream.. When V-Link is not operated at 8X (and above), the high-priority write request is always disabled no matter what the setting of this bit is.
6	RW	0	**Upstream High-Priority Read Request Stream** 0: No high-priority read request stream. 1: Enable high-priority read request stream.
5	RW	0	**C2P Read ACK Return Priority** 0: V-Link decodes C2P Read ACK command right when it's received 1: C2P Read ACK command will be handled till pending P2C write cycles are all flushed
4	RW	0	**0CF8h Configuration Cycle Address Bit[27:24] Usage** 0: Normal PCI usage 1: Address bit[27:24] are used as extended register address bit[11:8]
3	RW	0	**Dynamic STOP on Down Strobe** 0: Disable 1: Enable
2	RW	0	**Auto-Disconnect** 0: Disable 1: Enable
1	RW	0	**V-Link Disconnect Sequence for STPGNT Cycle** 0: Disable 1: Enable
0	RW	0	**V-Link Disconnect Sequence for HALT cycle** 0: Disable 1: Enable

Offset Address: 48h (D0F7)

V-Link Configuration – NB / SB **Default Value: 18h**

This register is used to configure V-Link bus controller on both North and South bridge chips.

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**Parity Check** 0: Disable 1: Enable	
6	—	0	**Reserved**	
5	RW	0	**16-Bit Width** 0: Disable 1: Enable	**RX16VK**
4	RW	1	**8-Bit Width** 0: Disable 1: Enable	**RX8VK**
3	RW	1	**4X Rate** 0: Disable 1: Enable	
2	RW	0	**2X Rate** 0: Disable 1: Enable	
1	RW	0	**V-Link Split Bus** 0: Disable 1: Enable	**RVKSPLT**
0	RW	0	**8X Rate** 0: Disable 1: Enable	

	X: Multiples of 66MHz cycle	Bus Width	R8XVK – 8X (D0F7 Rx48[0])	RX16VK – 16bit (D0F7 Rx48[5])	RVKSPLT – Split Bus (D0F7 Rx48[1])
Mode0 - 8-bit VD Half Duplex	4X	8-bit □	0	0	0
Mode1 – 8-bit VD Full Duplex	8X	4-bit □□	1	0	1
Mode2 – 8-bit VD Half Duplex	8X	8-bit □	1	0	0
Mode3 – 16-bit VD Half Duplex	4X	16-bit □	0	1	0
Mode4 – 16-bit VD Full Duplex	8X	8-bit □□	1	1	1

Procedure to Enable / Disable V-Link-8X Mode:

1. BIOS sets Rx48[0] to 1
2. Hardware will automatically enter a disconnect sequence, and then both NB/SB will start V-Link 8X mode. Then normal operation is then resumed.
3. To return to V-Link 4X mode, BIOS sets Rx48[0] to 0
4. Step 2 is then repeated.

Offset Address: A0h (D0F7)

NVC Configure **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3	RW	0	**While returning the P2C read ACK to SB, the NVC start to issue the next read request to reduce the P2C read latency** 0: Disable 1: Enable
2:0	—	0	**Reserved**

Offset Address: B0h (D0F7)

V-Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00	**Rising-Time Control for V-Link (R-Port)**
5:4	RW	00	**Falling-Time Control for V-Link (R-Port)**
3:2	RW	00	**Rising-Time Control for V-Link (S-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (S-Port)**

Offset Address: B1h (D0F7)

V- Link CKG Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	—	**Reserved**
3:2	RW	00	**Rising-Time Control for V-Link (D-Port)**
1:0	RW	00	**Falling-Time Control for V-Link (D-Port)**

V-Link North Bridge Driving Control (B3–B7h)

Offset Address: B3h (D0F7)

V-Link Auto Compensation Termination Resistor Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**P Resistor Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation
6	RO	0	**N Resistor Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation
5	RO	0	**P Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
4	RO	0	**N Pull Down Driving Check Flag for the NB Termination Resistor** 0: Abnormal condition occurred 1: Normal operation.
3	—	0	**Reserved**
2:0	RO	0	**NB V-Link Autocomp Termination Resistor Value** 000: Largest Resistor …. 111: Smallest Resistor

Offset Address: B4h (D0F7)

NB V-Link Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**V-Link Auto-compensation PMOS Output Value**
4	RW	0	**Reference Voltage of the VKCOMP in 4X V-Link Mode** 0: VREF4X=0.75V 1: VREF4X=0.9V
3:1	RO	0	**V-Link Auto-compensation NMOS Output Value**
0	RW	0	**Compensation Option** 0: Use Auto Compensation (value is kept in bits 7:5) 1: Use Manual setting (use the values of RxB5 and RxB6)

Offset Address: B5h (D0F7)

NB V-Link Manual Driving Control - Strobe **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Strobe Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Strobe Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B6h (D0F7)

NB V-Link Manual Driving Control - Data **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**Manual Setting - NB V-Link Data Pullup (PMOS)**
4	—	0	**Reserved**
3:1	RW	0	**Manual Setting - NB V-Link Data Pulldown (NMOS)**
0	—	0	**Reserved**

Offset Address: B7h (D0F7)

NB V-Link Receiving Strobe Delay **Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RW	0	**V-Link Manual Termination Resistor Value** 000: Largest Resistor …. 111: smallest Resistor
4:3	—	0	**Reserved**
2	RW	1	**NB V-Link Strobe Delay for Receiving**
1:0	RW	0	**NB V-Link Receiving Strobe Delay** 00: 0.15ns earlier 01: No delay 10: Delay 0.15ns 11: Delay 0.3ns

Device 1 Function 0 (D1F0): PCI to PCI Bridge

This configuration is provided to facilitate the configuration of the second PCI bus (AGP) without requiring new enumeration code. This function is represented as device number 1, function 0.

Header Registers (0–3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	B198h	**Device ID**

Offset Address: 5 - 4h (D1F0)

PCI Command **Default Value: 0007h**

Bit	Attribute	Default	Description
15:10	—	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0.
8	RO	0	**SERR# Enable** Hardwired to 0.
7	RO	0	**Address / Data Stepping** Hardwired to 0.
6	RW	0	**Parity Checking** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0.
4	RO	0	**Memory Write and Invalidate** Hardwired to 0
3	RO	0	**Respond To Special Cycle** Hardwired to 0.
2	RW	1	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	1	**Memory Space Access** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	1	**I/O Space Access** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 7-6h (D1F0)

PCI Status **Default Value: 0230h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13	RO	0	**Set When Terminated with Master-Abort, Except Special Cycle** 0: No abort received 1: Transaction aborted by the master
12	RO	0	**Set When Received a Target-Abort** 0: No abort received 1: Transaction aborted by the target
11	RO	0	**Set When Signaled a Target-Abort** NB never signals Target Abort
10-9	RO	01	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	—	0	**Reserved**
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6	RO	0	**User Definable Features**
5	RO	1	**66 MHz Capable**
4	RO	1	**Support New Capability List**
3:0	—	0	**Reserved**

Offset Address: 0E – 08h (D1F0)
PCI Header Registers

Offset Address	Attribute	Default	Description
08h	RO	00h	**Revision ID**
0B - 09h	RO	060400h	**Class Code**
0D-0Ch	RO	00h	**Reserved**
0Eh	RO	01h	**Header Type** It adheres to the PCI-PCI Bridge Configuration
0F	RO	00h	**Built In Self Test (BIST)**

Offset Address: 13-10h (D1F0)
Graphic Aperture Base Configuration **Default Value: 00000000h**

Bit	Attribute	Default	Description	Mnemonic
31:22	RW	0	**Programmable Base Address** The aperture base address bit acts as if hardwired to 0 if the corresponding (D1F0 Rx94[11:0]) bit is 0. Note: this range is defined as prefetchable	**GTBS1[31:22]**
21:4	—	0	**Reserved** (Hardwire to 0)	—
3	RO	0	**Prefetchable** Read as 1 when D1F0 Rx48[0] is 1	—
2:1	RO	0	**Type** Indicates that the address range is in the 32-bit address space	—
0	RO	0	**Memory Space**	—

Offset Address: 18h (D1F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number** Primary Bus Number is fixed at 0 internally; this register setting is ignored.

Offset Address: 19h (D1F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number** Secondary Bus Number is used when converting Type#1 configuration cycles to TYPE#0 configuration cycles.

Offset Address: 1Ah (D1F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number** PCI2 uses Subordinate Bus Number to decide if Type#1 command is passed to the PCI2 Bus.

Offset Address: 1Ch (D1F0)
IO Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**IO Address Bit[15:12] – inclusive**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1Dh (D1F0)
IO Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**IO Address Bit[15:12] – inclusive**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1F-1Eh (D1F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Secondary Status** If R2NDSTAT = 0 (Rx44[4]) : Read this register has 0 returned If R2NDSTAT = 1: Read this register has contents of Rx7-Rx6 (PCI Status Register) returned

Offset Address: 21-20h (D1F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	0FFFh	**Memory Address Bit[31:20]** - inclusive (address [19:0] is not decoded)
3:0	—	0	**Reserved**

Offset Address: 23-22h (D1F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit[31:20]** – inclusive (address [19:0] is not decoded)
3:0	—	0	**Reserved**

Offset Address: 25-24h (D1F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	0FFFh	**Memory Address Bit[31:20]** - inclusive
3:0	—	0	**Reserved**

Offset Address: 27-26h (D1F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	0	**Memory Address Bit[31:20]** - inclusive
3:0	—	0	**Reserved**

Offset Address: 34h (D1F0)
Capability Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**AGP Capability List Pointer** 70h, if RX48[0] is 0 80h, if RX48[0] is 1

Offset Address: 3F-3Eh (D1F0)
PCI-to-PCI Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	—	0	**Reserved**
6	RW	0	**Secondary Bus Reset**
5	—	0	**Reserved**
4	RW	0	**Enable Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**Enable VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O cycles to PCI2 1: Forward VGA compatible memory and I/O cycles to PCI2
2	RW	0	**Block ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit to PCI2. 1: Do not forward ISA I/O cycles with address in the top 768 bytes of each 1Kbyte block
1	RW	0	**Forward Lower Side PCI SERR# to Upper Side** Status is reported on Rx7[6]
0	RW	0	**Parity Error Response Enable**

Second PCI Bus Control (40–6Fh)

Offset Address: 40h (D1F0)
CPU to PCI Flow Control I **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7	RW	0	**CPU to PCI Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).	
6	RW	0	**CPU to PCI 1-Wait State Burst Write** 0: Disable 1: Enable	
5:4	RW	0	**Read Prefetch Control** x0: Always prefetch x1: Disable prefetch	
3	—	0	**Reserved**	—
2	RW	0	**MDA Resource Location** (Note: the setting on this register bit overwrites the settings on the IO/Memory's Base and Limit of the other devices) 0: AGP/PCI2; forward MDA access cycles to AGP/PCI2 1: PCI1; forward MDA access cycles to PCI1 MDA Resources include: Memory: B0000h-B7FFFFh, I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh. Check the following table for the function of register bits, RVGA2 and RMDA.	**RMDA**
1	RW	0	**PCI2 Master Read Caching** 0: Disable 1: Enable	
0	RW	0	**PCI2 Delay Transaction** 0: Disable 1: Enable	

Address	RVGA2 Rx3E[3]	RMDA Rx40[2]	Cycle Destination
Memory: AFFFFh-A0000h	0	-	PCI1
	1	-	PCI2
Memory: MDA (BFFFFh-B0000h)	1	0	PCI2
	1	1	PCI1
	0	-	PCI1
IO:[3BBh,3B0h] except MDA	0	-	PCI1
	1	-	PCI2
IO: MDA	1	0	PCI2
	0	-	PCI1
	1	1	PCI1
IO: [3DFh,3C0h]	1	-	PCI2
	0	-	PCI1

Notes:

If RISA2 (Rx3E[2]) is set to 1, NB will not forward cycles to AGP if A[9:0] is in the range of 3ffh-100h even if address are within the range defined by the RIOBS and RIOLM.

If both RVGA2 and RMDA are set to 1, VGA is on PCI2 and MDA is put on PCI1. VGA palette snooping is not supported in PCI2.

Offset Address: 41h (D1F0)

CPU to PCI Flow Control II **Default Value: 08h**

Bit	Attribute	Default	Description
7	RO	0	**Retry Status** 0: No retry occurred 1: Retry occurred (write 1 to clear)
6	RW	0	**Action When Retry Timeout** 0: No action taken except recording status 1: Flush buffer (write) or return 0FFFFFFFFh (read)
5:4	RW	0	**Retry Count** 00: Retry 2 times, back off CPU 01: Retry 4 times, back off CPU 10: Retry 16 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1	**C2P Burst Timeout Enable** 0: Disable 1: Enable
2	—	0	**Reserved**
1	RW	0	**Invalidate PCI1/PCI2 Read Buffer Data (read caching data) when C2P Cycle Arrived** 0: Disable 1: Enable
0	—	0	**Reserved**

Offset Address: 42h (D1F0)

PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	—	0	**Reserved**
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**Break Consecutive PCI Master Access** 0: Disable 1: Enable
3	RW	0	**Reserved**
2	RW	0	**PCI2 Claims the IO R/W and Memory Read Cycles** 0: Disable 1: Enable
1	RW	0	**PCI2 Claims the Local APIC FEEx_xxxx Cycles** 0: Disable 1: Enable
0	—	—	**Reserved**

Offset Address: 43h (D1F0)

PCI2 Timer **Default Value: 22h**

Bit	Attribute	Default	Description
7:4	RW	2h	**Host to PCI2 Time Slot** 0: Disable (no timer) 1: 16 GCLKs 2: 32 GCLKs ... 0Fh: 128 GCLKs
3:0	RW	2h	**PCI2 Master Time Slot** 0: Disable (No timer) 1: 16 GCLKs 2: 32 GCLKs ... 0Fh: 128 GCLKs

Offset Address: 44h (D1F0)
PCI2 Miscellaneous Control — **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:5	—	0	**Reserved**	
4	RW	0	**Rx1F-Rx1E Read Returned Value** 0: Rx1F-Rx1E always read as 00 1: Rx1F-Rx1E read will receive the values in Rx07-Rx06	**R2NDSTAT**
3:0	—	0	**Reserved**	

Offset Address: 45h (D1F0)
Fast Write Control — **Default Value: 72h**

Bit	Attribute	Default	Description
7	RW	0	**Force Fast Write Cycle QW Aligned** (if Rx45[6] = 0) 0: Disable (DW aligned) 1: Enable (force QW aligned)
6	RW	1	**Merge Multiple Host Transactions into A Fast Write Transaction (Burst)** 0: Disable 1: Enable (QW aligned)
5:3	—	110	**Reserved**
2	RW	0	**Fast Write Burst Length Limit: 4T** 0: Disable 1: Enable
1	RW	1	**Fast Write: Fast Back to Back** 0: Disable 1: Enable
0	RW	0	**Fast Write Initial Block: 1 Wait State** 0: Disable 1: Enable

Offset Address: 46h (D1F0)
PCI-to-PCI Bridge Device ID (Low Byte) — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge Low Byte (ID[7:0])**

Offset Address: 47h (D1F0)
PCI-to-PCI Bridge Device ID (High Byte) — **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Device ID for P2P Bridge High Byte (ID[15:8])**

Offset Address: 48h (D1F0)
Miscellaneous — **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	—
0	RW	0	**Report AGP Capability in Device 1** 0: Disable(Device 0) 1: Enable (Device 1). D1F0 Rx13-10 will be programmable, and the Rx80 AGP Capability Header will be added into the capability list directed by D1F0 Rx34.	**RGHDR_B**

Power Management Capability (70-77h)

Offset Address: 73-70h (D1F0)
Power Management Registers

Offset Address	Attribute	Default	Description
70h	RO	01h	**Capability ID**
71h	RO	00h	**Next Pointer**
72h	RO	02h	**Power Management Capabilities**
73h	RO	00h	**Power Management Capabilities**

Offset Address: 74h (D1F0)
Power Management Control / Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	—	00	**Reserved**
1:0	RW	00	**Power State** 00: D0 11: D3 hot

Offset Address: 75h (D1F0)
Power Management Registers **Default Value: 00h**

Offset Address	Attribute	Default	Description
75h	RO	00h	**Power Management Status**
76h	RO	00h	**PCI to PCI Bridge Support Extensions**
77h	RO	00h	**Power Management Data**

AGP 3.0 Configuration (80-A3h)

Offset Address: CAPPTR (D1F0 83-80h)
AGP Identifier **Default Value: 0035 000Eh**

Bit	Attribute	Default	Description
31:24	RZ	0	**Always Return 0, write has no effect**
23:20	R-IW	3h	**Major Revision**
19:16	R-IW	5h	**Minor Revision** If RxBD[3] (RBKMJMN1) is 0: 5h If RxBD[3] (RBKMJMN1) is 1: 0h
15:8	R-IW	70h	**Pointer to Next Item**
7:0	R-IW	0Eh	**Capability ID**

Offset Address: CAPPTR + 04h (D1F0 87-84h)
AGP Status **Default Value: 1F00 0A0Bh**

Bit	Attribute	Default	Description	Mnemonic
31:24	R-XW	1Fh	**Max # of AGP Requests**	
23-18	RZ-IW	0	**Reserved**	
17	RZ-XW	0	**Isoch Transaction** 0: Does not support Isoch transaction 1: Support Isoch transaction	
16	—	0	**Reserved**	
15:13	RZ-XW	0	**Optimum Asynchronous Request Size**	
12:10	RZ-XW	010	**Calibration Cycle** Set if RAGP30 (bit3) is 1 000 – 4ms 001 – 16ms 010 – 64ms 011 – 256ms	
9	R1-XW	1	**SBA Support** Always on.	
8	RZ-XW	0	**Reserved**	
7	R-XW	0	**64-bit GART Entry** Support 32-bit GART entry only.	
6	R-XW	0	**Host GART Translation** 0: Support host GART translation 1: No GART translation on host cycles	
5	R-XW	0	**Over 4GB Support** Not Supported	
4	R-XW	0	**Fast Write Support**	
3	R-XW	0	**AGP 8x Detected** Set by strap ball AGP8XDET# 0: AGP 2.0 Mode (not supported) 1: AGP 3.0 Mode	**RAGP30_B**
2:0	R-XW	011 111	**AGP Data Rate** **If Bit 3(RAGP30) is 1**, default is 011: supports 4X and 8X data transfer rate. **If Bit 3 (RAGP30) is 0**, default is 111: supports 1X, 2X and 4X data transfer rate.	—

Offset Address: CAPPTR + 08h (D1F0 8B-88h)

AGP Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RZ-IW	0	**Max # of AGP Command Requests**
23:17	RZ-IW	0	**Reserved**
16	RZ-MW	0	**Reserved**
15:13	RZ-IW	0	**Reserved for Master Device**
12:10	RW	0	**Calibration Cycle**
9	RW	0	**SBA Enable**
8	RW	0	**AGP Enable** 0: Disable 1: Enable
7	RO	0	**64-bit GART** Not supported
6	RZ-MW	0	**Reserved**
5	RW	0	**Over 4G Support** Not Supported
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	—	0	**Reserved**
2:0	RW	0	**Data Rate** If RAGP30 (D1F0 Rx87-84[3])) = 1, 001: 4X data transfer rate 010: 8X data transfer rate If RAGP30 (D1F0 Rx87-84[3])) = 0, 001: 1X data transfer rate 010: 2X data transfer rate 100: 4X data transfer rate

Offset Address: CAPPTR + 0Ch (D1F0 8F-8Ch)

AGP Isochronous Status **Default Value: 0000 0028h**

Bit	Attribute	Default	Description
31:24	—	0	**Reserved**
23:16	R-XW	0	**Maximum Bandwidth** (In unit of 32bytes) Shared by both asynchronous and isochronous.
15:8	R-XW	0	**Maximum Number of Isochronous Transactions in a Single Isochronous Period**
7:6	R-XW	0	**Isochronous Payload Sizes Supported** 00: 32,64,128,256 bytes 01: 64,128,256 bytes 10: 128,256 bytes 11: 256 bytes
5:3	R-XW	5h	**Maximum Isochronous Data Transfer Latency** (In unit of 1 us)
2	—	0	**Reserved**
1:0	R-XW	0	**Isochronous Error Code** 00: No error 01: Isoch Request Overflow 1x: Reserved

Offset Address: CAPPTR + 10h (D1F0 93-90h)

AGP Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	—	0	**Reserved**
9	RW	0	**Disable Calibration Cycle**
8	RW	0	**Enable AGP Aperture** Set to 1 to enable AGP Aperture. Note: Both must be 1 to enable this function.
7	RW	0	**GTLB Enable** When set to 0, GART TLB entries are invalidated. All AGP aperture access needs to fetch the translation table first.
6:0	—	0	**Reserved**

Offset Address: CAPPTR + 14h (D1F0_97-94h)

AGP Aperture Size **Default Value: 0001 0F00h**

Bit	Attribute	Default	Description	Mnemonic
31:28	RW	0	**Aperture Page Size Select** Where n is the value of this register. Only 4KB page size, PAGESZ1=0000h, is supported.	
27	—	0	**Reserved**	
26:16	R-IW	01	**Page Size Supported** Currently only 4KB page size is supported.	
15:12	—	0	**Reserved**	
11:0	RW	0F00h	**Aperture Size** (Default size is 256M) For 0<=n=<5, APSZ1[n]=0 forces Aperture Base Address [22+n] to 0 APSZ1[n]=1 allows Aperture Base Address [22+n] R/W For 8<= n <= 11, APSZ1[n]=0 forces Aperture Base Address [22+n-2] to 0 APSZ1[n]=1 allows Aperture Base Address [22+n-2] R/W	**GTSZ_B [11:0]**

Table 13. Aperture Size

Aperture Size \ APSZ1[11:0]	11	10	9	8	7	6	5	4	3	2	1	0
4MB	1	1	1	1	0	0	1	1	1	1	1	1
8MB	1	1	1	1	0	0	1	1	1	1	1	0
16MB	1	1	1	1	0	0	1	1	1	1	0	0
32MB	1	1	1	1	0	0	1	1	1	0	0	0
64M	1	1	1	1	0	0	1	1	0	0	0	0
128M	1	1	1	1	0	0	1	0	0	0	0	0
256M	1	1	1	1	0	0	0	0	0	0	0	0
512M	1	1	1	0	0	0	0	0	0	0	0	0
1G	1	1	0	0	0	0	0	0	0	0	0	0
2G (Maximum Aperture Size)	1	0	0	0	0	0	0	0	0	0	0	0
4G	0	0	0	0	0	0	0	0	0	0	0	0

Offset Address: CAPPTR + 18h (D1F0_9B-98h)

AGP GART Table Pointer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RW	0	**GART Table Base Address [31:12]**
11:0	—	0	**Reserved**

Offset Address: CAPPTR + 1Ch (D1F0_9F-9Ch)

AGP GART Table Pointer High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**GART Table Base Address [63:32]** Since OVER 4G is not supported, OS should write all zeros to this register. This register is ignored.

Offset Address: CAPPTR + 20h (D1F0_A3-A0h)

AGP Isochronous Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	—	0	**Reserved**
7:6	RW	0	**Isochronous Pay Load Size** Default is set up in register "CAPPTR + 0Ch [7:6]"
5:0	—	0	**Reserved**

AGP 4X / AGP 8X Compensation Circuits (B0-B9h)

Offset Address: B0h (D1F0)

AGP PAD Compensation Control / Status — **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**AGP4X Strobe's Reference Voltage** 0: Strobe signals do not use AGPVREF as input reference voltage (i.e. STB VREF is STB# and vise versa). 1: Strobe signals use AGPVREF as input reference voltage. (Note: this bit is valid only when internal signal, RX4EN or RX8EN, is set to 1; otherwise always use AGPVREF as Strobe signals' reference voltage)
6	RW	0	**AGP4X Strobe and GD Pad Driving Strength Control** 0: Driving strength is set by compensation circuit's defaults 1: Driving strength is controlled by Rx B1[7:0]
5:3	RO	xxx	**AGP Compensation Circuit N Output Strength**
2:0	RO	xxx	**AGP Compensation Circuit P Output Strength**

Offset Address: B1h (D1F0)

AGP Compensation Driving Strength Control — **Default Value: 63h**

Bit	Attribute	Default	Description
7:4	RW	6h	**AGP Output Buffer Driving Strength - N**
3:0	RW	3h	**AGP Output Buffer Driving Strength - P**

Offset Address: B2h (D1F0)

AGP Pad Driving and Delay Control — **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**GD / GADSTBx / GC#BE and GSBSTBx / GSBA# Pad Control** **GSBSTBx, GSBA** — **GD, GC#BE, GADSTBx** **0** No Cap — No Cap **1** Cap — Cap
6:5	RW	0	**GD, GC#BE Receive Strobe Delay** 00: Delay by –150 ps — 01: No delay 10: Delay by 150 ps — 11: Delay by 300 ps
4	RW	0	**GD[31:16] Output Staggered Delay** (1 ns) 0: No delay — 1: GD[31:16] is delayed by 1 ns
3	RW	1	**GD, GADSTBx Slew Rate Control** 0: Disable — 1: Enable
2	RW	0	**GSBA Receive Strobe Delay** 0: No Delay — 1: Delay by 1 ns
1:0	RW	00	**GADSTBx Output Delay** 00: No delay — 01: Delay by 150 ps 10: Delay by 300 ps — 11: Delay by 450 ps Note: GADSTB1 and GADSTB1# will have 1ns extra delayed if bit-4 is set to 1.

Offset Address: B3h (D1F0)

AGP Strobe Driving Strength — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Strobe Output Buffer Driving Strength N**
3:0	RW	0	**AGP Strobe Output Buffer Driving Strength P**

Offset Address: B4h (D1F0)

AGP GSBA Pads Control — **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1	**GD, GCBE Strobe Delay for Receiving**
6:4	RW	0	**SBA Pads Control Signals for Strobe**
3	—	0	**Reserved**
2:0	RO	0	**GSBA Pads Control**

Miscellaneous Control (BA-BFh)

Offset Address: BAh (D1F0)

AGP Hardware Support – VPX Mode **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:0	RW	1Fh	**AGP Request Queue Size** This register is effective if RxBD[1] is set to 1.

Offset Address: BBh (D1F0)

AGP Hardware Support – VPX Mode **Default Value: C4h**

This register is used to re-configure the AGP controller. To reconfigure the AGP controller, RxBD[1] must be set to 1.

Bit	Attribute	Default	Description
7	RW	1	**AGP SBA Mode Enable** 0: Disable 1: Enable
6	RW	1	**AGP Enable** 0: Disable 1: Enable
5	—	0	**Reserved**
4	RW	0	**Fast Write Enable** 0: Disable 1: Enable
3	RW	0	**AGP8X Mode Enable** 0: Disable 1: Enable
2	RW	1	**AGP4X Mode Enable** 0: Disable 1: Enable
1	RW	0	**AGP2X Mode Enable** 0: Disable 1: Enable
0	RW	0	**AGP1X Mode Enable** 0: Disable 1: Enable

Offset Address: BDh (D1F0)

AGP Capability Header Control **Default Value: 84h**

Bit	Attribute	Default	Description	Mnemonic
7:6	RW	10	**SBA Strobe Delay for Receiving**	
5:4	—	0	**Reserved**	
3	RW	0	**AGP Major / Minor Number Control** 0: Major/Minor = 35h 1: Major/Minor = 30h	**RBKMJMN1**
2	RW	1	**Select Rx80 as the AGP20 or AGP30 Header** 0: Rx80 is used as the AGP20 capability header even if the chip is powered up in AGP30 mode 1: Rx80 is used as the AGP30 capability header when the chip is powered up in AGP30 mode	
1	RW	0	**Enable AGP Hardware Registers in RxBA ~ RxBB** 0: AGP hardware is configured by registers of the AGP header (for 3.0) 1: AGP hardware is configured by registers RxBA ~ RxBB (used in VPX mode)	
0	—	0	**Reserved**	

Offset Address: BFh (D1F0)

Miscellaneous **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	—	0	**Reserved**	
0	RW	0	**AGP Capability Header** 0: AGP capability header is in Device0 Function0; D1F0 Rx80 ~ RxA0 are hidden. 1: AGP capability header is as described in D1F0 Rx80 ~ RxA0.	**RAGPCAP1**

APIC Cycles (C0-C3h)

Offset Address: C0h (D1F0)

APIC Legacy **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**APIC Legacy** 0: Disable 1: Enable, Range FECxyz00 to FECxyzFF, x,y,z are defined in {Rx41[7:0], Rx40[3:0]} – {Rx43[7:0], Rx42[3:0]}
6:4	—	0	**Reserved**
3:0	RW	1000	**x bytes in the APIC legacy address Range, base address**

Offset Address: C1h (D1F0)

APIC Legacy **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**y byte in the APIC legacy address Range, base address**
3:0	RW	0000	**z byte in the APIC legacy address Range, base address**

Offset Address: C2h (D1F0)

APIC Legacy **Default Value: 0Bh**

Bit	Attribute	Default	Description
7:4	—	0	**Reserved**
3:0	RW	1011	**x bytes in the APIC legacy address Range, limit**

Offset Address: C3h (D1F0)

APIC Legacy **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	Fh	**y byte in the APIC legacy address Range, limit**
3:0	RW	Fh	**z byte in the APIC legacy address Range, limit**

Device 2 Function 0 (D2F0) – PCI Express Root Port 0 (PCI-to-PCI Virtual Bridge)

Device 2 Function 0, a 4-Lane PCI Express Root Port, is connected to the PCI bus through AD13 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 2 and function number 0.

Header Registers (0-3Fh)

Offset Address	Attribute	Default	Description
1 – 0h	RO	1106h	**Vendor ID**
3 – 2h	RO	A208h	**Device ID**

Offset Address: 5-4h (D2F0)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:11	—	0	**Reserved**	
10	RW	0	**Interrupt Disable** Set when the device is prevented from generating INTx messages	
9	—	0	**Reserved**	
8	RW	0	**SERR# Enable** 0: Disable error report 1: Enable reporting of non-fatal and fatal errors	**RSERR_PEG**
7	—	0	**Reserved**	
6	RW	0	**Parity Error Response** 0: Ignore parity errors & continue 1: Take normal action on detected parity errors	**RPTYERR_PEG**
5:3	—	0	**Reserved**	
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit disables MSI messages.	
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SB 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.	
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SB. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.	

Offset Address: 7-6h (D2F0)
Status Register **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6])
14	RW1C	0	**Signaled System Error** This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message Rx4[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status
10:9	–	0	**Reserved** Always reads 0
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned Requestor poisons a write Request
7:5	–	0	**Reserved**
4	RO	1	**Capabilities List** Indicate the presence of an extended capability list item. Always set to 1 for PCI Express device
3	RO	0	**Interrupt Status** Indicate an INTx message is pending internally
2:0	–	0	**Reserved**

Offset Address: 8h (D2F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Revision Code**

Offset Address: 0B-9h (D2F0)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D2F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Cache Line Size – Reserved (No impact on functionality)**

Offset Address: 0Dh (D2F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Reserved (Hardwired to 0)**

Offset Address: 0Eh (D2F0)
Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type Code** 01: PCI-PCI Bridge

Offset Address: 0Fh (D2F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**BIST Support**

Offset Address: 17-10h (D2F0)
Base Address Register **Default Value: 00h**

Bit	Attribute	Default	Description
63:0	RO	00h	**Base Address**

Offset Address: 18h (D2F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Primary Bus Number**

Offset Address: 19h (D2F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Secondary Bus Number**

Offset Address: 1Ah (D2F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Subordinate Bus Number**

Offset Address: 1Ch (D2F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	1111	**I/O Base (AD[15:12] - inclusive)** This bridge will forward the cycles from primary side to PCI if the IO address AD[15:12] is between IO base and IO limit (Rx1D[7:4])
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.

Offset Address: 1Dh (D2F0)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RW	0	**I/O Limit (AD[15:12] - inclusive)**	**RIOLM_PEG[15:12]**
3:0	RO	0	**I/O Addressing Capability** 0 means IO addressing is 16-bit only.	

Offset Address: 1F-1Eh (D2F0)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6]
14	RW1C	0	**Received System Error** This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	—	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request
7:0	—	0	**Reserved**

Offset Address: 21-20h (D2F0)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – inclusive)** The address bits [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 23-22h (D2F0)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0000	**Reserved** Always reads 0.

Offset Address: 25-24h (D2F0)
Prefetchable Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:0	—	0000	**Reserved** Always reads 0.

Offset Address: 27-26h (D2F0)
Prefetchable Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Prefetchable Memory Limit AD[31:20]**
3:0	—	0000	**Reserved** Always reads 0.

Offset Address: 31-30h (D2F0)
I/O Base Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Base Upper 16 bits Address**

Offset Address: 33-32h (D2F0)
I/O Limit Upper **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	00h	**I/O Limit Upper 16 bits Address**

Offset Address: 34h (D2F0)
Capability Pointer **Default Value: 40h**

This register contains the offset address from the start of the configuration space.

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** Always reads 40h. Capability Pointer link list: Rx34 □ Rx40 □ Rx68 □ Rx70 □ NULL

Offset Address: 3Ch (D2F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D2F0)
Interrupt Ball **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**INT Ball** 01: INTA

Offset Address: 3F-3Eh (D2F0)
Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	–	00h	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Triggers a warm reset on the corresponding PCI Express Port
5	–	0	**Reserved**
4	RW	0	**Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O 1: Forward VGA compatible memory and I/O Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If an MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs 1: Enable the response to poisoned TLPs

PCI Express Capability Registers (40-63h)

Offset Address: 40-41h (D2F0)
PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID**

Offset Address: 43-42h (D2F0)
PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13:9	RO	0	**Interrupt Message Number**
8	RO	1	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled),
7:4	RO	0100	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1	**Capability Version**

Offset Address: 47-44h (D2F0)
Device Capabilities **Default Value: 0000 0nn1h**

Bit	Attribute	Default	Description
31:12	—	0	**Reserved**
11:9	RO	111	**Endpoint L1 Acceptable Latency** 111b: more than 64us
8:6	RO	xxx	**Endpoint L0s Acceptable Latency** This field is set up through PHY negotiation process.
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	—	00	**Reserved**
2:0	RO	001	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D2F0)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	—	0	**Reserved**
14:12	RO	000	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions it initiate that do not require hardware enforced cache coherency.
10	RWS	0	**Auxiliary Power PM Enable** This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO/RW	0	**Extended Tag Field Enable** When Rx47-44[5] ((DAXTAGF_PEG)) is set to 0, Rx44[5] is RO When Rx47-44[5] ((DAXTAGF_PEG)) is set to 1, Rx44[5] is RW
7:5	RW	000	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions it initiate that do not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable**
2	RW	0	**Fatal Error Reporting Enable** For a Root Port, the reporting of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** For a Root Port, the reporting of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D2F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	—	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the Port has issued Non-Posted Requests on its own behalf (using the Port's own Requestor ID) which have not been completed.
4	RO	1	**AUX Power Detected**
3	RW1C	0	**Unsupported Request Detected**
2	RW1C	0	**Fatal Error Detected**
1	RW1C	0	**Non-Fatal Error Detected**
0	RW1C	0	**Correctable Error Detected**

Offset Address: 4F-4Ch (D2F0)

Link Capabilities **Default Value: 0010 0C41h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	—	0	**Reserved**
20	RO	1	**Link Capabilities Register** Data Link Layer Link Active Reporting Capable
19:18	—	0	**Reserved**
17:15	RO	000	**L1 Exit Latency** 000: less than 1us. The value reported indicates the length of time this Port requires to complete transition from L1 to L0.
14:12	RO	000	**L0s Exit Latency** 000: less than 64ns. The value reported indicates the length of time this Port requires to complete transition from L0s to L0.
11:10	RO	11b	**Active State Link PM (ASPM) Support** 11b: L0s and L1 supported. This field indicates the level of ASPM supported on the PCI Express Link.
9:4	RO	04h	**Maximum Link Width** 010000b: x16 Link width
3:0	RO	1h	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D2F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	—	0	**Reserved**	
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us 1: FCU Timer limit is 120us.	LCES_PEG
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with asynchronous reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a distributed common reference clock.	LCCCC_PEG
5	W1C	0	**Retrain Link** A write of 1 to this bit initiates Link retrained by directing the Physical Layer LTSSM to the Recovery state.	
4	RW	0	**Link Disable** This bit disables the Link when set to 1.	
3	RO	0	**Read Completion Boundary** 0: 64 byte	
2	—	0	**Reserved**	
1:0	RW	00	**Link Active State PM (ASPM) Control** 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled	

Offset Address: 53-52h (D2F0)

Link Status **Default Value: 0nn1h**

Bit	Attribute	Default	Description
15:14	—	0	**Reserved**
13	RO	0	**Data Link Layer Link Active**
12	RO	0	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicated that Link training is in progress (Physical Layer LTSSM is in Configuration or Recovery state) or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successfully training of the Link to the L0 Link state.
9:4	RO	HwInitxxxxxx	**Negotiated Link Width** 000001: x1 000010: Reserved 000100: x4 001000: Reserved 010000: Reserved
3:0	RO	0001	**Link Speed** 0001: 2.5Gb/s negotiated Link speed.

Offset Address: 57-54h (D2F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	00h	**Physical Slot Number** Physical slot number attached to the Port.
18:17	—	0	**Reserved**
16:15	RO	0	**Slot Power Limit Scale** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
14:7	RO	00h	**Slot Power Limit Value** Write to the field causes the Port to send the Set_Slot_Power_Limit message.
6	RO	1	**Hot-plug Capable**
5	RO	1	**Hot-plug Surprise**
4	RO	0	**Power Indicator Present**
3	RO	0	**Attention Indicator Present**
2	RO	0	**MRL Sensor Present**
1	RO	0	**Power Controller Present**
0	RO	0	**Attention Button Present**

Offset Address: 59-58h (D2F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	–	0	**Reserved**
12	RW	0	**Slot Control** Data Link Layer State Changed Enable 0:Disable 1: Enable
11	–	0	**Reserved**
9:8	RW	0	**Power Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate POWER_INDICATOR_* Message.
7:6	RW	0	**Attention Indicator Control** 00: Reserved 01: On 10: Blink 11: Off Writes to this field cause the Port to send the appropriate ATTENTION_INDICATOR_* Message.
5	RW	0	**Hot-Plug Interrupt Enable** This bit when set enables generation of Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	**Command Completed Interrupt Enable** This bit when set enables the generation of Hot-Plug interrupt when a command is completed by the Hot-Plug controller.
3	RW	0	**Presence Detect Changed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on a presence detect changed event.
2	RO	0	**MRL Sensor Changed Enable**
1	RO	0	**Power Fault Detected Enable**
0	RW	0	**Attention Button Pressed Enable** This bit when set enables the generation of Hot-Plug interrupt or Wakeup event on an Attention Button pressed event.

Offset Address: 5B-5Ah (D2F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	–	0	**Reserved**
8	RW1C	0	**Slot Status** Data Link Layer State Changed
7	–	0	**Reserved**
6	RO	0	**Presence Detect State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL Sensor State**
4	W1C	0	**Command Completed**
3	W1C	0	**Presence Detect Changed**
2	RO	0	**MRL Sensor Changed**
1	RO	0	**Power Fault Detected**
0	W1C	0	**Attention Button Pressed**

Offset Address: 5D-5Ch (D2F0)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	—	0	**Reserved**
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 63-60h (D2F0)

Root Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	—	0	**Reserved**
17	RO	0	**PME Pending** 0: No pending PME 1: Indicates that another PME is pending when the PME Status (bit 16) is set.
16	W1C	0	**PME Status** Indicates that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D2F0)

Power Management Capabilities **Default Value: C802 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support**
25	RO	0	**D1 Support**
24:22	RO	0	**AUX Current**
21	RO	1	**Device Specific Initialization**
20:19	–	0	**Reserved**
18:16	RO	010	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D2F0)

Power Management Status/Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	–	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm or cold reset.
14:13	RO	0	**Data Scale**
12:9	RW	0	**Data Select**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	0	**Power State**

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D2F0)

MSI Capability Support **Default Value: 0180 0005h**

Bit	Attribute	Default	Description
31:25	–	0	**Reserved**
24	RO	1	**This MSI capability supports pre-vector masking capability**
23	RO	1	**This MSI capability supports 64 bit message address only**
22:20	RW	000	**Multiple Message Enable** 000: 1message allocated 001: 2 message allocated 010: 4 message allocated 011: 8 message allocated 100: 16 message allocated 101: 32 message allocated 11x: Reserved
19:17	RO	000	**Multiple Message Capable** 000: 1message requested 001: 2 message requested 010: 4 message allocated 011: 8 message allocated 100: 16 message requested 101: 32 message requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service 1: This Port is permitted to use MSI to request service.
15:8	RO	0	**Next Capability Pointer**
7:0	RO	05h	**Capability ID**

Offset Address: 77-74h (D2F0)
System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	00h	**System-Specified Message Address Bit [31:2]**
1:0	RO	00	**System-Specified Message Address Bit [1:0]** These bits will always read as 0

Offset Address: 7B-78h (D2F0)
System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**System-Specified Message Address Bit [63:32]**

Offset Address: 7D-7Ch (D2F0)
Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles

Offset Address: 83-80h (D2F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Mask Bit**
0	RW	0	**Mask Bit for Message 0**

Offset Address: 87-84h (D2F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	00h	**Pending Bit**
0	RO	0	**Pending Bit for Message 0**

PCI Express Transaction Layer Registers (A0-A4h)

Offset Address: A0h (D2F0)
Downstream Control I **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disabled 1: Enabled
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disabled 1: Enabled
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disabled 1: Enabled
4	RW	0	**Downstream Lock Cycle Support** 0: Disabled 1: Enabled
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed 1: Allowed
0	RW	1	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: A1h (D2F0)
Downstream Control II **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS (Configuration Request Retry Status) completion.
6	RW	0	**TRANS Assert Wait State at Receiving DownsTream Write Data** 0: Disable 1: Enable
5:4	–	0	**Reserved**
3	RW	0	**C2P Read Completion Timer for Vector Development Mode** When this bit is set to 1, the timer in RxA1[2:0] becomes: 000: 1us 001: 1us 010: 1us 011: 1us 100: 3us 101: 3us 110: 3us 111: 3us
2:0	RW	100	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10ms (Spec. lower bound) 100: 30ms 101: 50ms (Spec. higher bound) 110: 100ms 111: Reserved

Offset Address: A4h (D2F0)
Upstream Control **Default Value: 5Ch**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Address A35~A31 Forced to 0** 0: Disabled 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory
6	–	1	**A Guard bit for Improving Tming to Prevent Upstream write FIFO from Begin Overwritten**
5	RW	0	**Upstream Checking Malformed TLP through "Byte Enable Rule" And "Over 4K Boundary Rule"** 0: Disabled 1: Enabled
4	RW	1	**Downstream Read Wait Till The Upstream Write Data Flushed** 0: Disabled 1: Enabled
3	RW	1	**Infinite Flow Control** 0: Current Design 1: CPLH & CPLD & NPD Become Infinite mode
2	RW	1	**Flow Control Update for Each Header** 0: Current Design (update header credit whenever received two TLPHs 1: Update header credit whenever received TLPH(include PH,NPH and CPLH)
1	RW	0	**VC1 Request Queue Usage (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0)** 0: Disabled 1: Enabled, it allows Transaction Layer map non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note that when this bit is 1, bit-0 has to be 0)
0	RW	0	**Disable Virtual Channel 1 Support** 0: Enable VC1, data FIFO of VC1 is used by VC1. 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

PCI Express Data Link Layer Registers (B0-B8h)

Offset Address: B0h (D2F0)
Ack/Nak Latency Timer Limit **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**Timer Limit for Ack/Nak Latency Timer and Update FC Latency Timer (in unit of 250MHz)** 00: 4 x 1 Clocks 01: 4 x 2 Clocks 02: 4 x 3 Clocks. ... 0n: 4 x (n+1) Clocks FF: 4 x 256 Clocks.

Offset Address: B1h (D2F0)
Replay Timer Limit **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay Timer Limit (In unit of 250MHz)** 00: 8 x 1 Clocks 01: 8 x 2 Clocks 02: 8 x 3 Clocks ... 0n: 8 x (n+1) Clocks FF: 8 x 256 Clocks.

Offset Address: B2h (D2F0)
FCU Control and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCU Timeout Status** 1 Means the FCU timeout has occurred
6	RW	1	**FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCU Receive Timer Limit** 0: Timeout limit of 200us 1: Timeout limit of 300us
4	RW	0	**FCU Receive Timer Reset Control** 0: Timer reset by FCI/FCU only 1: Timer reset by any received DLLPs
3:1	—	0	**Reserved**
0	RW	0	**DL and TL Gard Bit** Reset upstream related logic when retrain is going on.

Offset Address: B3h (D2F0)
Replay Timer Control **Default Value: 80h**

Bit	Attribute	Default	Description
7:6	RW	10	**Replay Timer Control while Rewind** (resend those DLLPs which do not have corresponding ACK/NAK received) 00: Hold Replay Timer during rewind 01: During rewind, if ACK/NAK comes in, reset and hold the Replay Timer 10: During rewind, reset and hold the Replay Timer as long as the Retry Buffer is empty 11: Reserved
5:3	—	0	**Reserved**
2:0	RW	000	**Count of Replay Timer Expired During RXL0s** (Receiving Physical in L0s state) **Before Resend the TLP** **When Rx50[7], LCES_PEG, is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7], LCES_PEG, is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D2F0)

Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3	RW	0	**TLP vs. Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass FCI2 for VC0 1: TLP is allowed to pass FCI2 for VC0
2:0	RW	000	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D2F0)

FCU Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	–	0	**Reserved**
6	RW	0	**FCU (Flow Control Unit) Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired 1: Update flow control credit only when FCU timer expired
5:4	RW	01	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer RACKLTLM (RxB0) expired. 01: Send ACK every 4 correct TLP has been received 10: Send ACK every 8 correct TLP has been received 11: Send ACK every 16 correct TLP has been received
3:2	–	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP/FCU has been received 1: Do not complete FCI process even when TLP/FCU has been received
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP only when FCI timer expired 1: Transmit FCI DLLP continuously as long as the FCI process is not finished

Offset Address: B6h (D2F0)

Transaction / Link Layer Checking Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**VC Negotiate Pending Control for VC1** 0: Assert VC negotiation pending after VC1 is enabled 1: Assert VC negotiation pending after RESET is de-asserted
3	–	0	**Reserved**
2	RW	0	**ECRC Checking Control for the Case of TD equals to1 but no ECRC field in TLP** 0: Ignore the error 1: Report error to Transaction Layer, which will mark the TLP as a Malformed TLP
1	RW	1	**Length Malform Report Control** 0: Do not report length malform to Transaction Layer 1: Report length malform to Transaction Layer
0	RW	1	**LCRC Checking Control** 0: Do not check LCRC 1: Check LCRC

Offset Address: B8h (D2F0)

Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	—	0	**Reserved**
0	RW	0	**Data Link Layer Header Position** 0: SDP (Start DLLP) can be in Lane0/4/8/12 1: SDP (Start DLLP) always at Lane0.

PCI Express Physical Layer Registers (C0-CBh)

Offset Address: C3-C0h (D2F0)

PHY Control **Default Value: 0023 0003h**

Bit	Attribute	Default	Description
31:24	RO	0	**PHYLS State Mapping**
23:22	—	0	**Reserved**
21	RW	1	**Lane Enable** 0: Enable lanes based on LTSSM negotiation results 1: Enable lanes based on receiver detection's results
20	RW	0	**Bypass PHYES Receiver Detect Function** 0: RCVOUT is derived from PHYES 1: Bypass receiver detect: RCVOUT = 1
19:18	—	0	**Reserved**
17	RW	1	**Disparity Check Enable** 0: Disable 1: Enable
16	RW	1	**State Machine LTSSM** 0: Wait for the electrical idle signal from the PHYES or 12ms after RESET# become inactive. 1: Always wait for 12ms after the RESET# become inactive.
15:13	—	0	**Reserved**
12:8	RW	00h	**PHY Lane Configuration Setting** 10000-01000: Reserved 00100: x4 with normal connection 00010: Reserved 00001: x1 with normal connection 01111-10111: Reserved 10111: x8 with reverse connection 11011: x4 with reverse connection 11101: Reserved 11110: x1 with reverse connection 10101: force into L0s state (for testing and measurement used only) 00000: Use phy negotiation Other values are not allowed.
7	RW	0	**Quick Timeout Counter Setting** When set to 1, following timeout counters will be shorter: TIMEOUT_2MS □ TIMEOUT_4US TIMEOUT_12MS □ TIMEOUT_24US TIMEOUT_24MS □ TIMEOUT_48US TIMEOUT_48MS □ TIMEOUT_96US TIMEOUT_1024TS □ TIMEOUT_32TS Receiver Detection: 15x1024ns □ 1x1024ns
6	RW	0	**Disable Data Scrambling/Descrambling** 0: Enable 1: Disable
5:3	RW	000	**Loopback Mode Selection (Applies to All 16 Lanes)** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: Reserved 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved
2:0	RW	011	**COMMA Detection Window** 000, 001: Illegal values Others: Delay number of T to determine correct lane-to-lane deskew value

Offset Address: C7-C4h (D2F0)

Elastic Buffer Base Registers for Lane 0 to 7 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	–	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 7** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	–	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 6** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	–	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 5** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	–	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 4** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	–	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 3** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	–	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 2** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	–	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 1** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	–	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

Offset Address: CB-C8h (D2F0)

Elastic Buffer Base Registers for Lane 8 to 15 **Default Value: 4444 4444h**

Bit	Attribute	Default	Description
31	–	0	**Reserved**
30:28	RW	4h	**Elastic Buffer Base Register for Lane 15** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
27	–	0	**Reserved**
26:24	RW	4h	**Elastic Buffer Base Register for Lane 14** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
23	–	0	**Reserved**
22:20	RW	4h	**Elastic Buffer Base Register for Lane 13** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
19	–	0	**Reserved**
18:16	RW	4h	**Elastic Buffer Base Register for Lane 12** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
15	–	0	**Reserved**
14:12	RW	4h	**Elastic Buffer Base Register for Lane 11** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
11	–	0	**Reserved**
10:8	RW	4h	**Elastic Buffer Base Register for Lane 10** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
7	–	0	**Reserved**
6:4	RW	4h	**Elastic Buffer Base Register for Lane 9** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations
3	–	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 8** 0, 1, 7: Illegal values Others: delay numbers of T for elastic buffer operations

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D3-D0h (D2F0)

PMC Control **Default Value: 0000 0050h**

Bit	Attribute	Default	Description
31:24	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128ns 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
23:16	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (L0SLIM_PEG = 00) 00: 128ns 01: 2x128ns 02: 3x128ns ... FF: 256x128ns
15	W1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[5:4] expired.
14	–	0	**Reserved**
13:12	RW	0	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device). 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
11:10	–	0	**Reserved**
9:8	RW	0	**Downstream Cycles Triggered C2P Cycles**, Period of Staying at L0 Before Returned to L1 for PHY (when PMU is in non-D0 state) 00: Immediately 01: 1 cfgW or message + delay10T 10: 1 32QW +1cfgW or message+ delay10T 11: 2 32QW +1 cfgW or message +delay10T
7	–	0	**Reserved**
6:4	RW	101	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1us 001: 2us 010: 4us 011: 8us 100: 16us 101: 32us 110: 64us 111: 128us
3:2	–	0	**Reserved**
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode, receiving data in the device will be sent to the transmit side
0	RW	0	**LTSSM State During Link Reconfigure Link Width** 0: When reconfigure link width, LTSSM must be in Detect state 1: When reconfigure link width, LTSSM can be in Configuration state

PCI Express Message Controller Related Registers (D8h)

Offset Address: D8h (D2F0)

PMC Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	W1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system
6:0	–	0	**Reserved**

PCI Express Electrical PHY Registers (E0-EAh)

Offset Address: E0h (D2F0)
PHYES Module Control (For x4 Root Ports) **Default Value: 02h**

Bit	Attribute	Default	Description
7:4	–	0	**Reserved**
3:1	RW	1	**Charge Pump Current Control**
0	RW	0	**Charge Pump Style Control**

Offset Address: E1h (D2F0)
PHYES Module Related Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back/received data 1: Have reverse polarity on the loop-back/received data
3:2	RW	10	**Squelch Window Select (64~175mv)**
1	RW	0	**Electrical Idle State Exit Condition: Number of Non Idle Signal Detected Before Exit Idle State** 0: 2 bits 1: 10 bits
0	RW	0	**Electrical Idle State Enter Condition: Number of Idle Signal Detected Before Enter Idle State** 0: 2 bits 1: 10 bits

Offset Address: E2h (D2F0)
First 8 Lanes PHYES Module Control – Rx/Tx I **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	–	0	**Reserved**
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-7** 0: All enable. 1: Power down
4	RW	0	**Lane 4-7 Clock Buffer Power Down** 0: All enable 1: Lane 4-7 power down
3:2	RW	00	**Receiver Input Rise Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps
1:0	RW	00	**Receiver Input Fall Delay (duty cycle adjustment for the first 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps

Offset Address: E3h (D2F0)

First 8 Lanes PHYES Module Control – Rx/Tx II **Default Value: 42h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0]
6:5	RW	10b	**Filter Depth Valid Only When CDR Type is set to 0** 00: filter depth = 1 01: filter depth = 4 10: filter depth = 8 11: filter depth = 12
4	RW	0	**CDR Type** 0: 1/N type 1: Pseudo 6X scheme
3	RW	0	**Reserved / CDR filter Depth** 0: filter depth = 3 1: filter depth = 2
2:0	RW	010b	**First 8 Lanes, Lane 0 –7, Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: E4h (D2F0)

First 8 Lanes PHYES Module Control – Rx/Tx III **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Pre/De-Emphasis Level Selection**
3:0	RW	4h	**Driver Current Source Selection**

Offset Address: E8h (D2F0)

Second 8 Lanes PHYES Module Control – Rx/Tx I **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	–	0	**Reserved**
4	RW	0	**Lane 12-15 Clock Buffer Power** 0: All enable 1: Lane 12~15 power down
3:2	RW	00	**Receiver Input Rise Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80ps
1:0	RW	00	**Receiver Input Fall Delay (duty cycle adjustment for the second 8 lanes)** 00: 0 ps 01: 10 ps 10: 40 ps 11: 80 ps

Offset Address: E9h (D2F0)

Second 8 Lanes PHYES Module Control – Rx/Tx II **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits [2:0]
6	–	0	**Reserved**
5	RW	0	**PHYES Clock Buffer Power Down on Lane 8-15** 0: All enable 1: Power down
4:3	–	0	**Reserved**
2:0	RW	010	**Second 8 Lanes, Lane 8 –15, Termination Resistance Selection** Resistance Range: 62Ω (000b) ~ 43Ω (111b) Default: 50Ω (010b)

Offset Address: EAh (D2F0)

Second 8 Lanes PHYES Module Control – Rx/Tx III **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Pre/De-Emphasis Level Selection**
3:0	RW	4h	**Driver Current Source Selection**

PCI Express Electrical PHY Test Registers (F0-F7h)

Offset Address: F3-F0h (D2F0)

PHY Test **Default Value: 0600 0000h**

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	**Electrical PHY Test Mode Enable** Program this bit to 1 to start Electrical PHY test	EPHYTST_PEG
30:28	—	0	**Reserved**	
27:24	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency/4ns) + 1	
23:20	RW	0	**Select Test Pattern** 0000: SKP order-set 0001: User define, use RxF6[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: D 10.2 test bit sequence 1110: D 24.3 test bit sequence 1111: Compliance test bit sequence	
19:16	RW	0	**Select Lane for Loop Back Test** 0000: Loop back test on lane0 0001: Loop back test on lane1 .... 1111: Loop back test on lane15	
15:8	RW	00h	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) When using loopback mode to test electrical PHY, the following should be satisfied: RXF1 ′ 8 > loopback latency/4ns 00~0Bh: Illegal.value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times ... FFh: Test pattern repeats 255 times	
7:0	—	0	**Reserved**	

Offset Address: F7-F4h (D2F0)

PHY Test Symbol **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Electrical PHY Test Error** 1: An error occurred in loop back test mode receiving side
30	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** That same errors happen or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP
29:26	—	0	**Reserved**
25:16	RW	00h	**Transmitted Symbol when EPHYTST_PEG (RxF0[31]) is set to 1** 00 when EPHYTST_PEG is 0
15:0	—	0	**Reserved**

Offset Address: F9-F8h (D2F0)

PHY BIST Counter Test Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0000	**PHY BIST Period Electrical PHY Test Error**

Device 2 Function 0 (D2F0) – PCI Express Root Port 0 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-137h)

Offset Address: 103-100h (D2F0)

Advance Error Reporting Enhanced Capability Header — **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	Next Capability Offset
19:16	RO	1	Capability Version
15:0	RO	0001h	PCI Express Extended Capability ID

Offset Address: 107-104h (D2F0)

Uncorrectable Error Status — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RW1CS	0	Unsupported Request Error Status (TL)
19	RW1CS	0	ECRC Error Status (TL)
18	RW1CS	0	Malformed TLP Status (TL)
17	RW1CS	0	Receiver Overflow Status (TL)
16	RW1CS	0	Unexpected Completion Status (TL)
15	RW1CS	0	Completer Abort Status (TL)
14	RW1CS	0	Completion Timeout Status (TL)
13	RW1CS	0	Flow Control Protocol Error Status (TL)
12	RW1CS	0	Poisoned TLP Status (TL)
11:5	–	0	Reserved
4	RW1CS	0	Data Link Protocol Error Status (DLL)
3:1	–	0	Reserved
0	RW1CS	0	Training Error Status (PHY)

Offset Address: 10B-108h (D2F0)

Uncorrectable Error Mask — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	–	0	Reserved
20	RWS	0	Unsupported Request Error Mask (TL)
19	RWS	0	ECRC Error Mask (TL)
18	RWS	0	Malformed TLP Mask (TL)
17	RWS	0	Receiver Overflow Mask (TL)
16	RWS	0	Unexpected Completion Mask (TL)
15	RWS	0	Completed Abort Mask (TL)
14	RWS	0	Completion Timeout Mask (TL)
13	RWS	0	Flow Control Protocol Error Mask (TL)
12	RWS	0	Poisoned TLP Mask (TL)
11:5	–	0	Reserved
4	RWS	0	Data Link Protocol Error Mask (DLL)
3:1	–	0	Reserved
0	RWS	0	Training Error Mask (PHY)

Offset Address: 10F-10Ch (D2F0)
Uncorrectable Error Severity **Default Value: 0006 0011h**

Bit	Attribute	Default	Description
31:21	—	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1	Malformed TLP Severity (TL)
17	RWS	1	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	0	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:5	—	0	Reserved
4	RWS	1	Data Link Protocol Error Severity (DLL)
3:1	—	0	Reserved
0	RWS	1	Training Error Severity (PHY)

Offset Address: 113-110h (D2F0)
Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	—	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	—	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D2F0)
Correctable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:13	—	0	Reserved
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	—	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	—	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D2F0)
Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	—	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 12B-11Ch (D2F0)
Header Log (TL)

Offset	Attribute	Default	Description
11F – 11C	ROS	00h	Header Log Register 1st DW
123 – 120	ROS	00h	Header Log Register 2nd DW
127 – 124	ROS	00h	Header Log Register 3rd DW
12B – 128	ROS	00h	Header Log Register 4th DW

Offset Address: 12F-12Ch (D2F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	—	0	Reserved
2	RW	0	Fatal Error Reporting Enable
1	RW	0	Non-Fatal Error Reporting Enable
0	RW	0	Correctable Error Reporting Enable

Offset Address: 133-130Ch (D2F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	Advanced Error Interrupt Message Number (TL)
26:7	—	0	Reserved
6	RW1CS	0	Fatal Error Messages Received (TL)
5	RW1CS	0	Non-Fatal Error Messages Received (TL)
4	RW1CS	0	First Uncorrectable Fatal Error Message Received (TL) Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error
3	RW1CS	0	Multiple ERR_FATAL/NONFATAL Received (TL)
2	RW1CS	0	ERR_FATAL/NONFATAL Received (TL)
1	RW1CS	0	Multiple ERR_COR Received (TL)
0	RW1CS	0	ERR_COR Received (TL)

Offset Address: 137-134Ch (D2F0)
Error Source Identification **Default Value: 0000 0000h**

This register is updated regardless of the settings of Root Control register and the Root Error Command register.

Bit	Attribute	Default	Description
31:16	ROS	0000	ERR_FATAL/NONFATAL Source Identification
15:0	ROS	0000	ERR_COR Source Identification

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined, there is no implementation of VC Arbitration Table and Port Arbitration Table.

Offset Address: 140-143h (D2F0)
Virtual Channel Enhanced Capability **Default Value: 0001 0002h**

Bit	Attribute	Default	Description
31:20	RO	000h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	0002h	PCI Express Extended Capability ID

Offset Address: 147-144h (D2F0)
Port VC Capability I — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:12	–	0	**Reserved**	
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port	
9:8	RO	0	**Reference Clock** Reserved for root port	
7	–	0	**Reserved**	
6:4	RO	0	**Low Priority Extended VC Count**	
3	–	0	**Reserved**	
2:0	RO	0	**Extended VC Count**	VCAEVCC_PEG_[2:0]

Offset Address: 14B-148h (D2F0)
Port VC Capability II — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined
23:8	–	0	**Reserved**
7:0	RO	00h	**VC Arbitration Capability;**

VC0 Resource (150-15Bh)

Offset Address: 150-153h (D2F0)
VC Resource Capability (VC0) — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)** Indicates the maximum number of time slot (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR port arbitration.
15	RO	0	**Reject Snoop Transactions**
14:0	–	0	**Reserved**

Offset Address: 157-154h (D2F0)
VC Resource Control (VC0) — **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1	**VC Enable** Hardwired to 1
30:27	–	0	**Reserved**
26:24	RO	0	**VC ID** Hardwired to 0 for VC0.
23:8	–	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D2F0)
VC Resource Status (VC0) — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going
16:0	–	0	**Reserved**

VC1 Resource (15C-167h)

The following registers exist only when Rx144[0] is programmed to 1. If Rx144[0]=0, all the following content will be read as 0.

Offset Address: 15F-15Ch (D2F0)

VC Resource Capability (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31: 23	–	0	**Reserved**
22:16	RO	00h	**Maximum Time Slots (TL)** Indicates the maximum number of time slot (minus one) that the VC resource is capable of supporting when it is configured for time-based WRR port arbitration.
15	RO	0	**Reject Snoop Transactions**
14:0	–	0	**Reserved**

Offset Address: 163-160h (D2F0)

VC Resource Control (VC1) **Default Value: 0010 0000h**

Bit	Attribute	Default	Description
31	RW	0	**VC Enable**
30:27	–	0	**Reserved**
26:24	RW	1	**VC ID.**
23:8	–	0	**Reserved**
7:0	RW Bit 0: RO	00	**TC/VC Mapping** This field indicates the TCs that are mapped to VC1. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC1 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit0 is hardwired to 0 (i.e. TC0 is always mapped to VC0).

Offset Address: 167-164h (D2F0)

VC Resource Status (VC1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	–	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware) 0: Negotiation is complete 1: Negotiation is on-going.
16:0	–	0	**Reserved**

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_C	Case Operating Temperature	0	85	°C	1
T_S	Storage Temperature	–55	125	°C	1
V_{IN}	Input Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2
V_{OUT}	Output Voltage	–0.5	V_{RAIL} + 10%	Volts	1, 2

Note 1. Stress above the conditions listed may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described under operating conditions.

Note 2. V_{RAIL} is defined as the V_{CC} level of the respective rail. The CPU interface is CPU dependent (CPU V_{CORE} or VTT). Memory is 2.5V or 1.8V. V-Link is 1.5V. AGP can be 1.5V (4x transfer mode) or 0.8V (8x transfer mode).

DC Characteristics

T_C = 0-85°C, V_{RAIL} = V_{CC} ±5%, V_{CORE} = 1.5V ±5%, GND = 0V

Table 10. DC Characteristics

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	–0.50	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage	–	0.55	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4	–	V	I_{OH} = –1.0 mA
I_{IL}	Input Leakage Current	–	±10	uA	0 < V_{IN} < V_{CC}
I_{OZ}	Tristate Leakage Current	–	±20	uA	0.55 <V_{OUT} < V_{CC}

Drive strength for selected output balls is programmable. See Device 0 RxB0[6], B1, B3, B5, B6, B9, BA, D8-DB, E8-EB and straps VD4-5 for details.

MECHANICAL SPECIFICATIONS

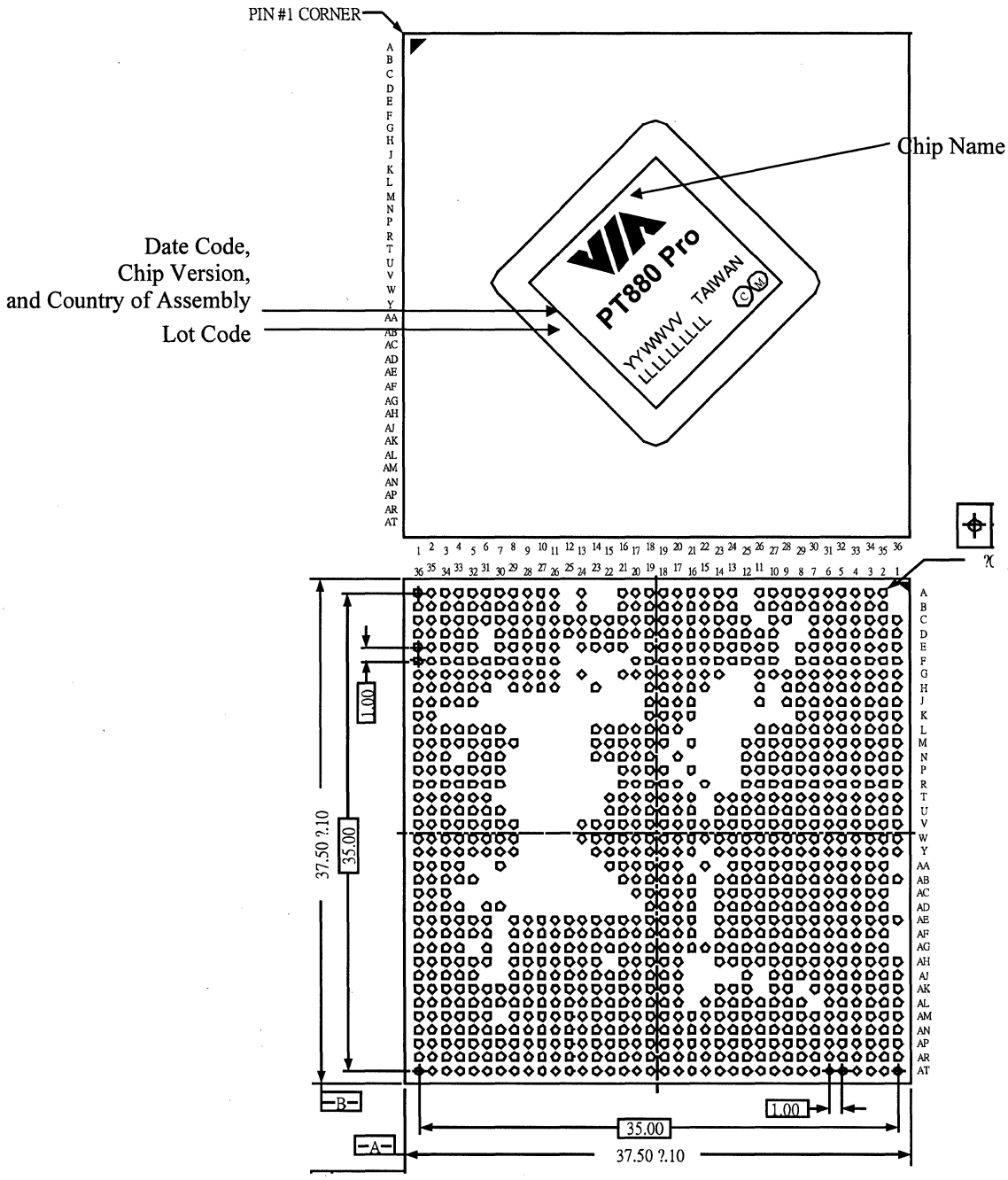


Figure 5. Mechanical Specifications – FCBGA-1054 Flip Chip Ball Grid Array Package

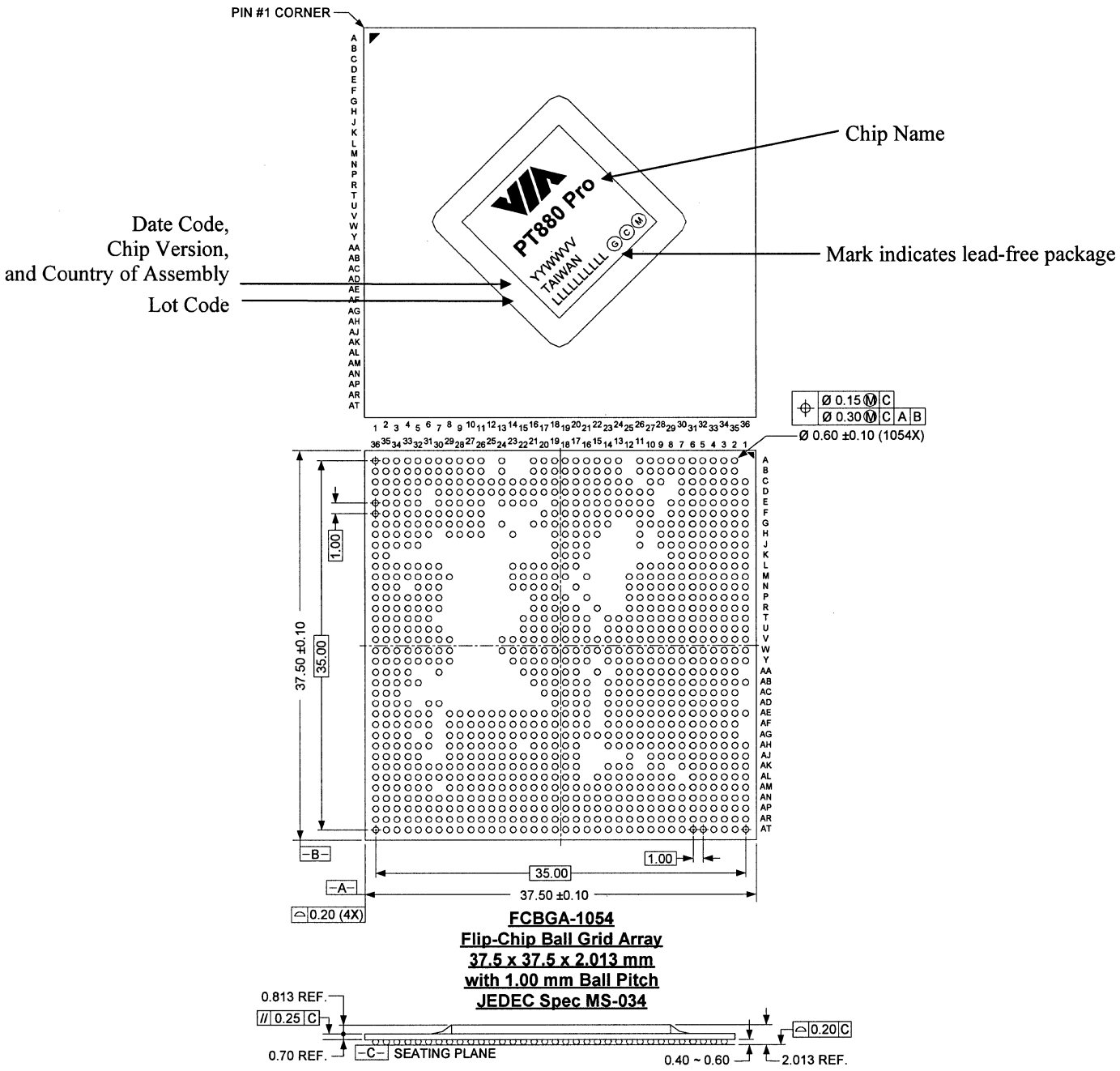


Figure 6. Lead-Free Mechanical Specifications – FCBGA-1054 Flip Chip Ball Grid Array Package