FEATURES

- Generates all Essential Clock Signals for All-In-One Motherboards and Laptops.

- Supports 8086/8088/80286/80386SX/80386DX/80486-based Designs.

- Frequency Options of 100, 80, 66.6, 50, 48, 40, 32, 0 MHz and Others.

- Integrates Floppy Drive, Serial Port and Keyboard Controller Clocks On-chip.

- Single Crystal Expedites FCC Approvals by Reducing EMR.

- Two Independent Clock Generators.

- Fast Rise and Fall Times.

- Glitch Free Switching for Both Clock Generators.

- Extremely Stable Frequencies.

- Switchable Clock Rates, Even After Board Manufacturing.

- 50-50 Duty Cycle With One Percent Tolerance.

- System Outputs Capable of 12 mA Drive.

- All Outputs Switch-Off Testability Option.

- Advanced Low Power CMOS Technology.

- 44 Pin PLCC.

DESCRIPTION SL9093

The SL9093 is a universal System Clock Chip capable of generating all essential clock signals that are used in typical PC and Notebook designs. This device can support 8086, 8088, 80286, 80386SX, 80386DX and 80486 microprocessor based designs, amongst others. The CPUCLK outputs of this clock chip are programmable through the keyboard or by jumper settings. Clock options of 100 MHz, 80 MHz, 66.6 MHz, 50 MHz, 48 MHz, 40 MHz, 32 MHz and DC are available, as well as the resultant frequencies from dividing these signals by 2 or 4, giving optimal flexibility to the user.

CPU frequency selection is done by the three decode inputs FS0-FS2 as shown in Table 1. IOSEL is used to control the system I/O bus clock. During a CPU cycle the IOSEL remains high, and the frequency selection on the outputs is determined by the FS0-FS2 pins. When an I/O cycle is detected, the IOSEL goes low and fixed frequencies of 16 MHz, 8 MHz and 4 MHz are available on output pins F12 (pin 8), F122 (pin 5) and F124 (pin 3). The 8 MHz system I/O clock on Pins F122 and F24 guarantee add-on card compatibility. Designers also have the option to run the system I/O clock at half the CPU clock by connecting the IOSEL pin to the keyboard controller in order to hold this pin high during an I/O cycle. This allows the IOSEL signal to be controlled through the keyboard.

The reference frequency of 14.318 MHz is also supplied to the output through the FREF pin for the I/O slots. The FREF12 pin has an output of 1.19 MHz and is used by Timer 1 (8254) in the peripheral controller for refresh. All outputs are capable of 12mA drive. All inputs are pulled-up or pulled-down on-chip to provide default set-up values.

The SL9093 consists of two independent Voltage Controlled Oscillators (VCOs) integrated with dividers, phase sensitive detectors, charge pumps and buffer amplifiers to provide the desired glitch free frequencies. An externally generated signal of 14.318 MHz is used as the reference frequency for the SL9093. Phase differences between this reference frequency and that generated by the VCOs are tracked by phase sensitive detectors. The phase difference becomes an input to the charge pumps which in turn generate a signal to sink or source the charge. This signal runs through the buffer amplifiers between the charge pumps and the VCOs. The output from the VCOs are divided to generate the appropriate outputs.

The SL9093 is designed using advanced CMOS technology and is available in a 44 pin PLCC. It requires only one crystal (14.318 MHz) and a few RC components to generate all the essential clocks that are required for PC and Notebook designs. As there is only one crystal on the system board, Electro Magnetic Radiation (EMR) is reduced significantly, facilitating FCC approval. This makes the SL9093 an ideal low cost solution with capabilities for universal system applications.

TURBO-IOSEL is 16 MHz normal (on F12) for chip sets using two times the AT Bus clock for asynchronous operation. However, some peripherals may be able to run on BUSCLK's of 16 MHz. This necessitates the chip sets' input frequency to be 32 MHz instead of 16 MHz. TURBO-IOSEL can be switched "on the fly" glitch free. TURBO-IOSEL can also be used to run ATCLK input on chip sets requiring four times BUSCLK input.
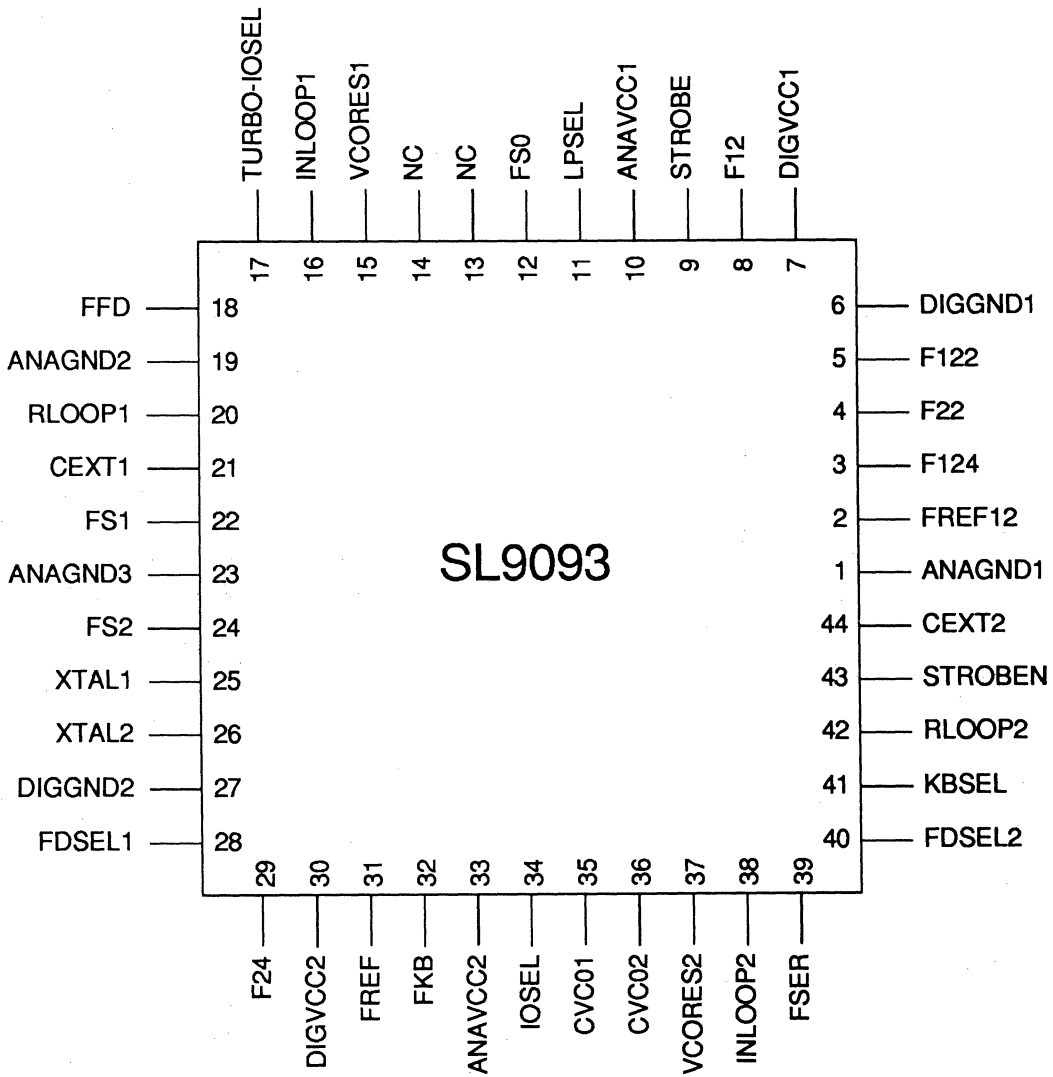
BLOCK DIAGRAM SL9093
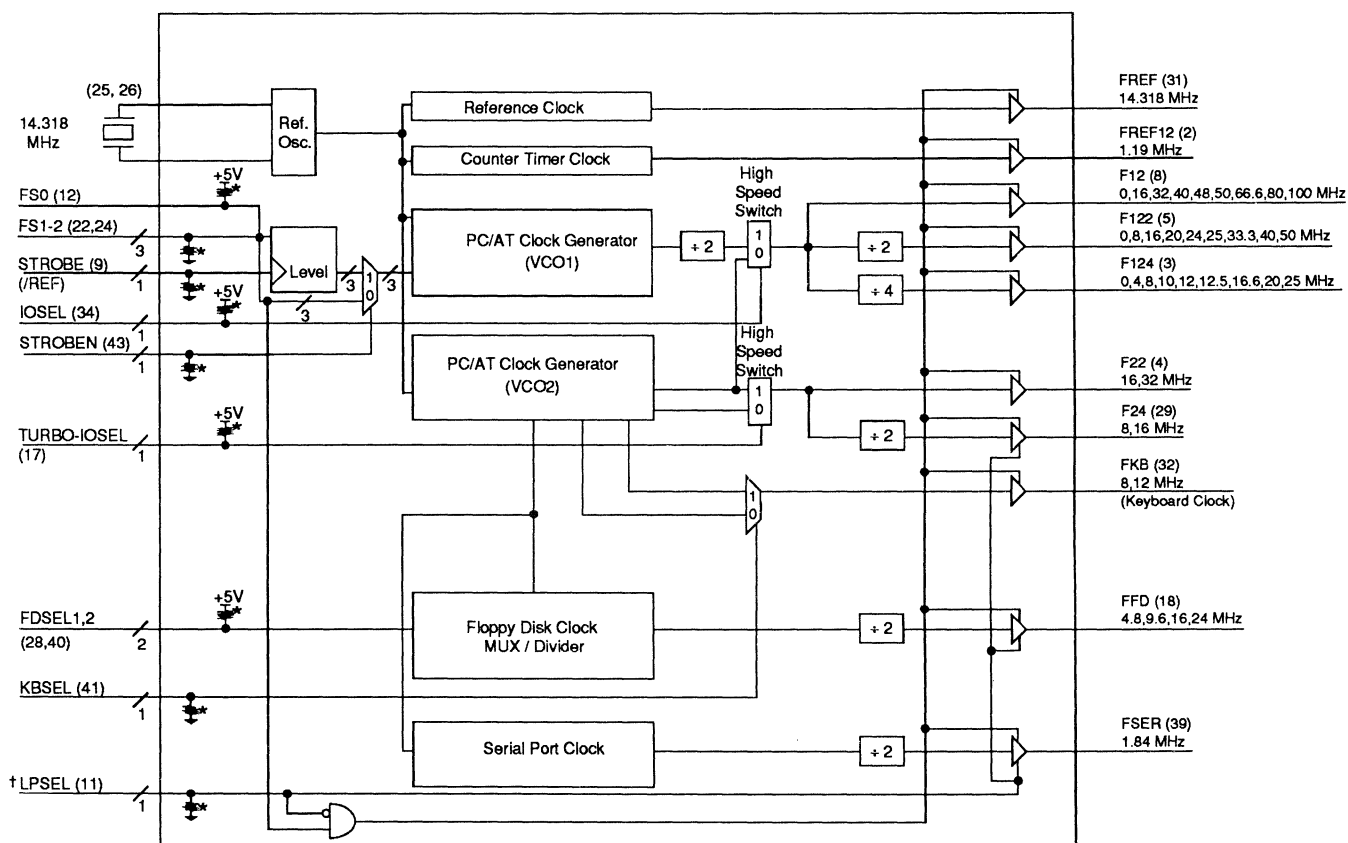
* Pulled Up/Down On-Chip.
† For 100 MHz selection at F12(8) (in non-test mode) LPSEL should be tied high (+5).

PINOUT

Top pins (left to right): 17 TURBO-IOSEL, 16 INLOOP1, 15 VCORES1, 14 NC, 13 NC, 12 FS0, 11 LPSEL, 10 ANAVCC1, 9 STROBE, 8 F12, 7 DIGVCC1

Left pins (top to bottom):
- FFD — 18
- ANAGND2 — 19
- RLOOP1 — 20
- CEXT1 — 21
- FS1 — 22
- ANAGND3 — 23
- FS2 — 24
- XTAL1 — 25
- XTAL2 — 26
- DIGGND2 — 27
- FDSEL1 — 28

Center: **SL9093**

Right pins (top to bottom):
- 6 — DIGGND1
- 5 — F122
- 4 — F22
- 3 — F124
- 2 — FREF12
- 1 — ANAGND1
- 44 — CEXT2
- 43 — STROBEN
- 42 — RLOOP2
- 41 — KBSEL
- 40 — FDSEL2

Bottom pins (left to right): 29 F24, 30 DIGVCC2, 31 FREF, 32 FKB, 33 ANAVCC2, 34 IOSEL, 35 CVC01, 36 CVC02, 37 VCORES2, 38 INLOOP2, 39 FSER

SL9093 PIN DESCRIPTIONS

SYMBOL	PIN	TYPE	DESCRIPTION
ANAGND1,2,3	1,19,23	-	Analog Ground.
ANAVCC1,2	10,33	-	Analog VCC for Clock generator 1, 2.
CEXT1,2	21,44	I	Charge pump pin for Clock generator 1, 2.
CVCO1,2	35,36	I	VCO capacitor pins 1, 2 for Clock generator.
DIGGND1,2	6,27	-	Digital Ground.
DIGVCC1,2	7,30	-	Digital +5V supply.
F12	8	O	F1 (0, 32, 40, 48, 50, 66.6, 80,100 MHz) if IOSEL = 1. F2 (16, 32 MHz) if IOSEL = 0. [12mA drive]
F22	4	O	16 or 32 MHz output. [6mA drive]
F24	29	O	F22 frequency divide by 2. [6mA drive]
F122	5	O	F12 divide by 2. [12mA drive]
F124	3	O	F12 divide by 4. [12mA drive]
FDSEL 1, 2	28, 40	I	Floppy disk frequency select pins.
FFD	18	O	Floppy disk frequencies 4.8, 9.6, 16, or 24 MHz available at this pin depending on FDSEL1 and FDSEL2. [6mA drive]
FKB	32	O	8 or 12 MHz output (Keyboard clock). [6mA drive]
FREF	31	O	14.318 MHz output for AT bus video clock. [12mA drive]
FREF12	2	O	1.19 MHz output (Timer clock). [6mA drive]
FS0-FS2	12,22,24	I	Frequency Select (from Keyboard or Jumpers) as shown in Table 1.
FSER	39	O	Serial Port frequency: 1.8461 MHz. [6mA drive]
INLOOP1,2	16,38	I	Loop filter resistor pin 1 for Clock generator 1, 2. Both pins should also be tied to ground through .001μF capacitors.

SYMBOL	PIN	TYPE	DESCRIPTION
IOSEL	34	I	Frequency Select input used for input/ output operations (Dynamic). When IOSEL is 1, F1 is selected. When it is 0, F2 is selected.
KBSEL	41	I	Keyboard clock frequency select pin. 8 MHz selected when low, 12 MHz when high.
LPSEL	11	I	Low power input. Forces loop 2, Floppy and Serial Clocks to be disabled when low. Should be tied high for 100 MHz selection on F12. For test mode (tri-state all ouput pins) it is pulled low with FS0, FS1=1 and FS2=0.
NC	13,14	–	No Connect.
RLOOP1,2	20,42	I	Loop filter resistor pin 2 for Clock generator 1, 2.
STROBE	9	I	Refresh strobe pin.
STROBEN	43	I	Enable pin for the strobe. Strobe latch in picture when high, bypassed when low.
TURBO-IOSEL	17	I	Selects F22 frequency to be 16 or 32 MHz.
VCORES1,2	15,37	I	Center frequency resistor for Clock generator 1, 2.
XTAL1,2	25,26	X1,X2	Crystal oscillator pin 1, 2.

FS0 (12)	FS1 (22)	FS2 (24)	TURBO -IOSEL (17)	IOSEL (34)	F12 (8)	F122 (5)	F124 (3)
0	0	0	X	1	48 MHz	24 MHz	12 MHz
0	0	1	X	1	50 MHz	25 MHz	12.5 MHz
0	1	0	X	1	80 MHz	40 MHz	20 MHz
0	1	1	X	1	66.6 MHz	33.3 MHz	16.6 MHz
1	0	0	X	1	32 MHz	16 MHz	8 MHz
1	0	1	X	1	40 MHz	20 MHz	10 MHz
1†	1†	0†	X	1	100 MHz	50 MHz	25 MHz
1	1	1	X	1	0 MHz*	0 MHz*	0 MHz*
X	X	X	1	0	32 MHz	16 MHz	8 MHz
X	X	X	0	0	16 MHz	8 MHz	4 MHz

* DC = 0V - (Low)
† LPSEL needs to be tied to +5 for this selection.

Table 1 CPU Clock Outputs/Selection

TURBO-IOSEL (17)	F22 (4)	F24* (29)
1	32 MHz	16 MHz
0	16 MHz	8 MHz

*Output can be disabled using LPSEL input.

Table 2 I/O Clock Frequency Selection

FDSEL1 (28)	FDSEL2 (40)	FFD* (18)
0	0	4.8 MHz
0	1	9.6 MHz
1	0	16 MHz
1	1	24 MHz

*Output can be disabled using LPSEL input.

Table 3 Floppy Disk Frequency Selection

KBSEL (41)	FKB (32)
0	8 MHz
1	12 MHz

Table 4 Keyboard Frequency Selection

FREF (31)	FREF12 (2)	FSER* (39)
14.318 MHz	1.19 MHz	1.8461 MHz

*Output can be disabled using LPSEL input.

Table 5 Reference Frequencies

TEST
LPSEL = LOW
FS0 = 1   FS1 = 1   FS2 = 0

Table 6 Test Mode Selection

DC CHARACTERISTICS   SL9093

(TA = 0 ° C to 70 ° C, VDD = 5V $\pm$ 5%)

Parameters	Symbol	Min.	Max.	Units	Conditions
Low Level Input Voltage	VIL		0.8	V	
Input Current	IIL		±1	μA	
High Level Input Voltage	VIH	2.0		V	
Low Level Output Voltage	VOL1		0.4	V	IDL = 12 mA
High Level Output Voltage	VOH1	2.4			IOH = 12 mA
Low Level Output Voltage (Low power TTL)	VOL2		0.4	V	IDL = 6 mA
High Level Output Voltage (Low power TTL)	VOH2	2.4		V	IDL = 6 mA
Supply Current					
Oper	ICC		1.5	mA	Per MHz
Quiscent			5	μA	Inputs @ Vss or VDD

NOTES

1. Thermal resistance of package = 66° C/W.
2. Calculated worst case tpd factor = 1° 81.
3. Calculated max junction temp = 117° C.

AC CHARACTERISTICS SL9093

(TA = 0 ° C to 70 ° C, VDD = 5V ± 5%)

XTAL1, XTAL2, Crystal frequency..14.318 MHz

Duty Cycle (All Clock Outputs)..50% ± 1%*†
(Load 4 LSTTL inputs)

Settling time from change of FS1, FS2, TURBO-IOSEL...........................1uS to +/- 10% of defined frequency
(1ms to lock)

Rise and Fall times..TBD

* Except F22(4): 70-30 duty cycle for 32MHz option only.
† FREF(32): Follows the duty cycle on the 14.318 MHz crystal at input.
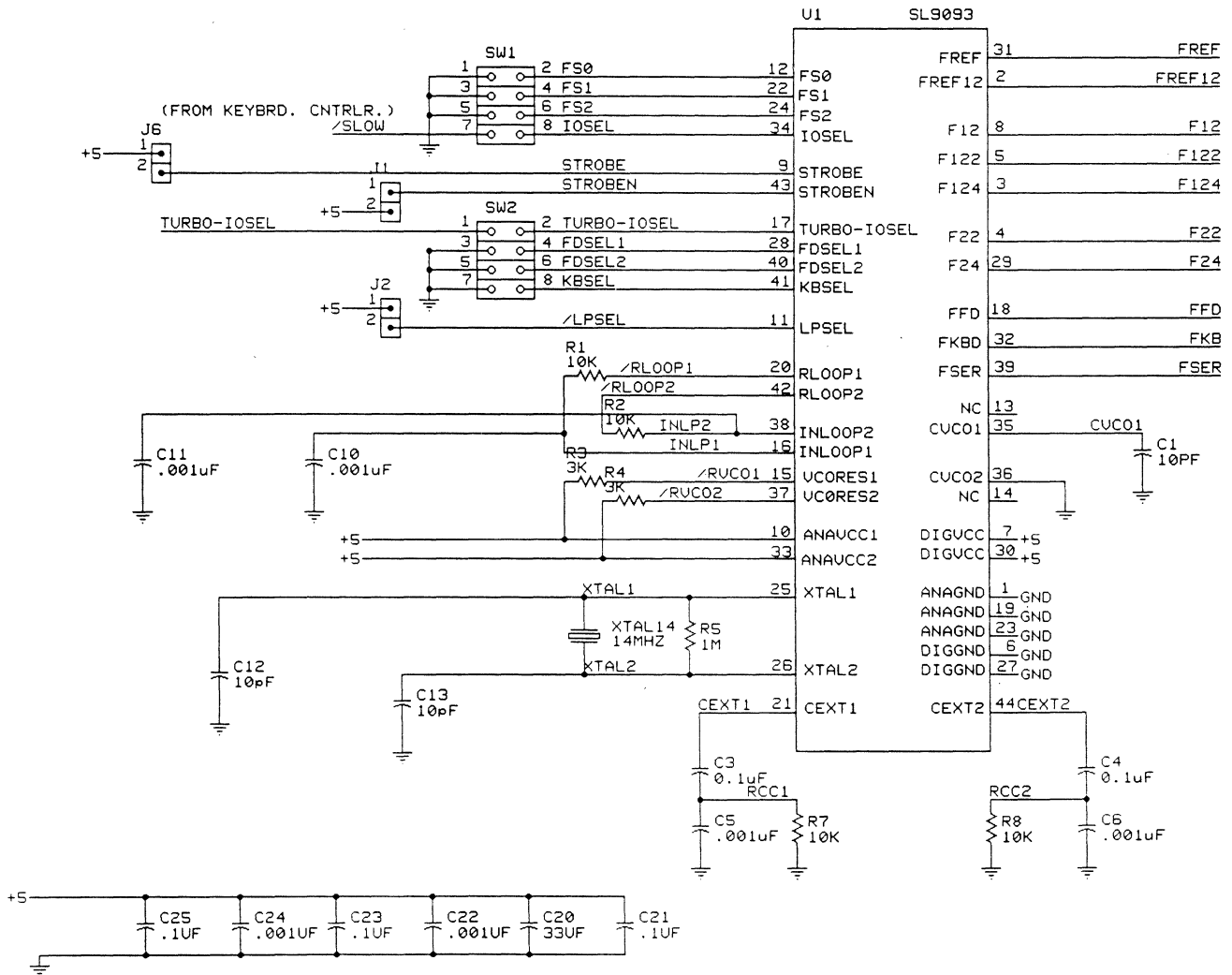
EXTERNAL COMPONENTS

Description	Name	Clock Generator 1	Clock Generator 2
Center Frequency Resistor	(VCORES)	3kΩ	3kΩ
Loop Filter Resistor	(RLOOP - INLOOP)	10kΩ	10kΩ
VCO Capacitor	CVCO1	-	10PF

Charge Pump Components   (CEXT)   Connected as follows:

Pin 21   0.1μf   10KΩ±2%   0.001μf

Pin 44   0.1μf   10KΩ±2%   0.001μf
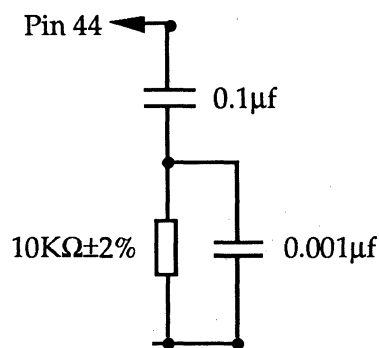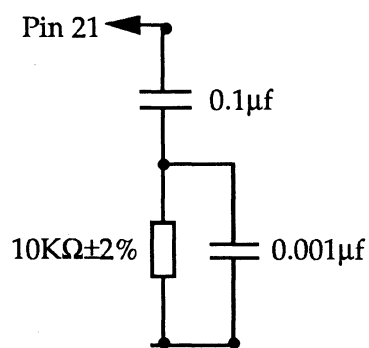
APPLICATION INFORMATION

Clock Circuit Connection Schematic

Package Information

44 Pin Plastic Leadless Chip Carrier

ORDERING INFORMATION

Device Type:
SL9093

Package Type:
PL- Plastic LCC

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

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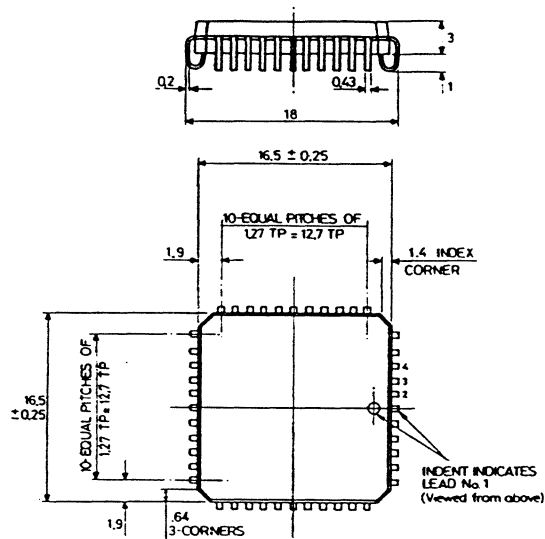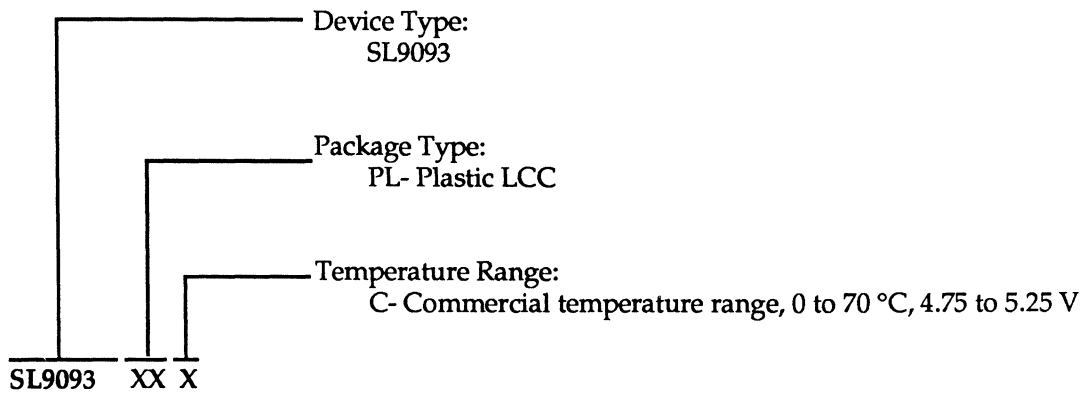
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