VL82C486

SINGLE-CHIP 486 (SC486™) CONTROLLER

FEATURES

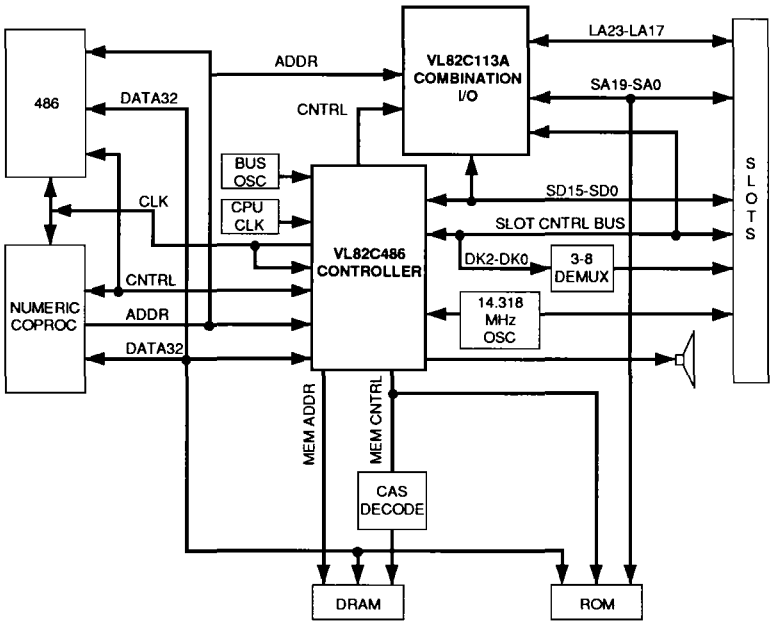
- Fully compatible 486-based PC/AT systems
- Up to 33 MHz CPU operation
- Replaces the following peripheral logic on the motherboard:
  - Two 82C37A DMA controllers
  - 74LS612 memory mapper (extended to support 64 MB)
  - Two 82C59A interrupt controllers
  - 82C54 timer
  - 82284 clock generator and ready interface
  - 82288 bus controller
- Includes:
  - Memory/refresh controller
  - Port A, B, and NMI logic
  - Bus steering logic
  - Parity generation/checking for on-board DRAM
  - Turbo Mode control
  - Hidden off-board, stolen on-board refresh
  - Staggered RAS refresh
  - Three-stateable outputs for board testing
- Memory controller features include:
  - Page Mode DRAM access
  - One to four banks 32 bits wide
  - One or two banks 64 bits wide
  - Two- or four-way interleave support
  - Programmable –RAS/CAS timing
  - Burst support
- Supports:
  - Up to 64 MB system memory
  - 256K, 1M, or 4M DRAM
  - Double-sided SIMMs
  - Secondary cache interface
  - 8- or 16-bit wide BIOS ROM
  - Shadow RAM in the 640K-1M area
  - Flash memory for BIOS ROM
  - Asynchronous ISA bus operation up to 16 MHz
  - Relocation of slot ROMs
- Power saving features include:
  - Sleep Mode
  - Slow DRAM refresh
- Other features:
  - Programmable for 10- or 16-bit internal I/O addressing
  - Programmable drive on DRAM and ISA bus signals
  - Programmable memory access to define "fast-bus", local bus, slot bus, and non-cacheable and write-protect areas
  - Input pin defines access to local bus devices
- 1.0-micron CMOS technology
- 208-lead metric quad flat pack (MQFP)

DESCRIPTION

The VL82C486 is a Single-Chip High Performance Controller for 486- and 486SX/487SX-based PC/AT systems.

The VL82C486 includes the dual 82C37A DMA controllers, dual 82C59A programmable interrupt controllers, 82C54 programmable interval timer, 82284 clock and ready generator, 82288 bus controller and the logic for address/data bus control, memory control, shutdown, refresh generation and refresh/DMA arbitration.

SYSTEM DIAGRAM (VL82C486-BASED PC/AT)



ORDER INFORMATION

Part Number	Package
VL82C486-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to +70°C.

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OVERVIEW

The VL82C486 Controller is designed to perform in 486DX- or 486SX/487SX-based PC/AT-compatible systems running up to 33 MHz. The VL82C486 replaces the following devices on the motherboard:

- Two 82C37A DMA controllers
- Two 82C59A interrupt controllers
- 82C54 timer
- 74LS612 memory mapper
- 82284 clock generator and ready interface
- 82288 bus controller

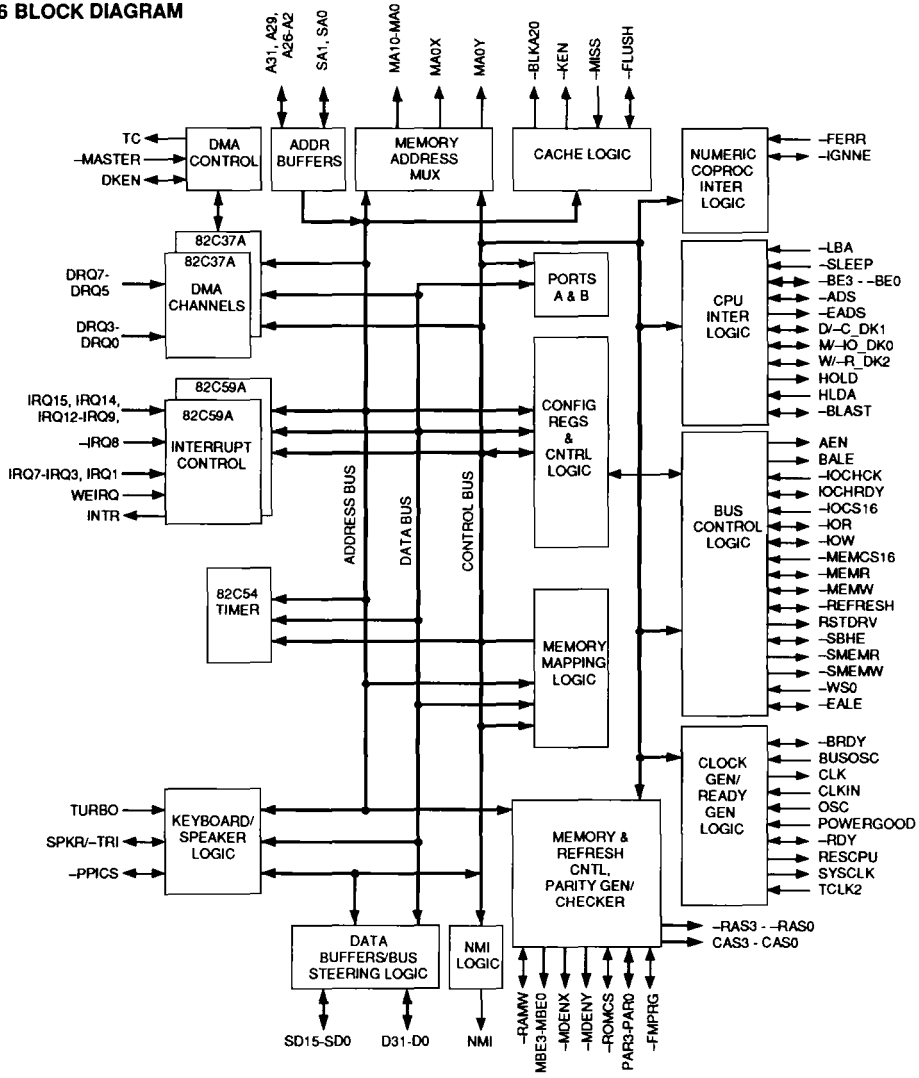
The controller also includes the following:

- Memory/refresh controller
- Port B and NMI logic
- Bus steering logic
- Turbo Mode control logic
- Parity checking logic
- Parity generation logic
- Support for Weitek numeric coprocessors

The memory controller logic is capable of accessing up to 64 MB. There can be up to four banks of 256K, 1M, or 4M DRAMs used in the system. The VL82C486 can drive four banks without external buffering. Built-in Page Mode operation and up to four-way interleaving allow the PC designer to maximize system performance using low cost DRAMs. Programmable DRAM timing is provided for RAS precharge, RAS-to-CAS delay, and CAS pulse width.

Shadowing features are supported on 16K boundaries between A0000h and FFFFFh (640 KB to 1 MB). Simultaneous use of shadowed ROM and direct system board access is possible

VL82C486 BLOCK DIAGRAM



in non-overlapping fashion throughout this memory space. Control over four access options is provided:

1. Access ROM or slot bus for reads and writes.
2. Access system board DRAM for reads and writes.
3. Access system board DRAM for reads and slot bus for writes.
4. Shadow Setup Mode. Read ROM or slot bus, write system board DRAM.

A special mode is supported for erasing and programming flash memories for the case where such devices are used as the BIOS ROMs.

Three special programmable address regions are provided. The fast-bus clock region allows accesses to certain memory regions at a faster ISA clock rate for fast on-board or off-board devices. A non-cacheable region and/or a write-protected region may be defined by a set of six registers that allow memory in the region 640 KB to 1 MB to be marked as non-cacheable and/or write-protected in increments of 16 KB. A further set of registers allows a memory range anywhere in the first 64 MB of memory to be marked as a DRAM region, an ISA bus region, or a local bus region either cacheable or non-cacheable in increments of 2 KB, 64 KB, or 1 MB.

Further support for devices that reside on the 486 local bus is provided through use of the –LBA (local bus access) input, which deselects the VL82C486 during CPU cycles. Also, a memory range anywhere in the first 64 MB of memory can be programmed via the internal Mapping Registers to make the VL82C486 access a local bus device as a 486 bus memory device during DMA or Master Mode transfers.

The VL82C486 handles system board refresh directly and also controls the timing of slot bus refresh. Refresh may be performed in Synchronous, Asynchronous, or Decoupled Mode. In Synchronous Mode, the slot bus and on-board DRAM refresh cycles proceed simultaneously and all memory cycles are held until both have completed. The Asynchronous Mode allows on- and off-board refreshes to be initiated simultaneously, but to complete asynchronously, allowing sooner access to DRAM. In Decoupled Mode, a separate refresh counter is used for slot bus refresh, allowing on-board DRAM and system refreshes to proceed independently, with DRAM refreshes initiated during bus idle cycles. CAS-before-RAS refresh is also supported. Refreshes are staggered to minimize power supply loading and attenuate noise on the VDD and ground pins. The VL82C486 supports the standard PC/AT refresh period of 15.625 µs as well as 125 µs.

Support for write-through cache controllers is provided through the use of a –MISS pin to detect cache-hits and cache-misses.

The interrupt controller logic consists of two 82C59A megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally and two of the interrupt request inputs are connected to internal circuitry allowing a total of 13 external interrupt requests. There is special programmable logic included in the VL82C486 which allows deglitching of inputs on all the interrupt request pins.

The interval timer includes one 82C54 counter/timer megacell. The counter/timer has three independent 16-bit counters and six programmable counter modes.

The DMA controllers are 82C37A compatible. The DMA controllers control data transfers between an I/O channel and on- or off-board memory. DMA can transfer data over the full 64 MB range available. There are internal latches provided for latching the middle address bits output by the 82C37A megacells on the data bus, and the 74LS612 memory mappers are provided to generate the upper address bits.

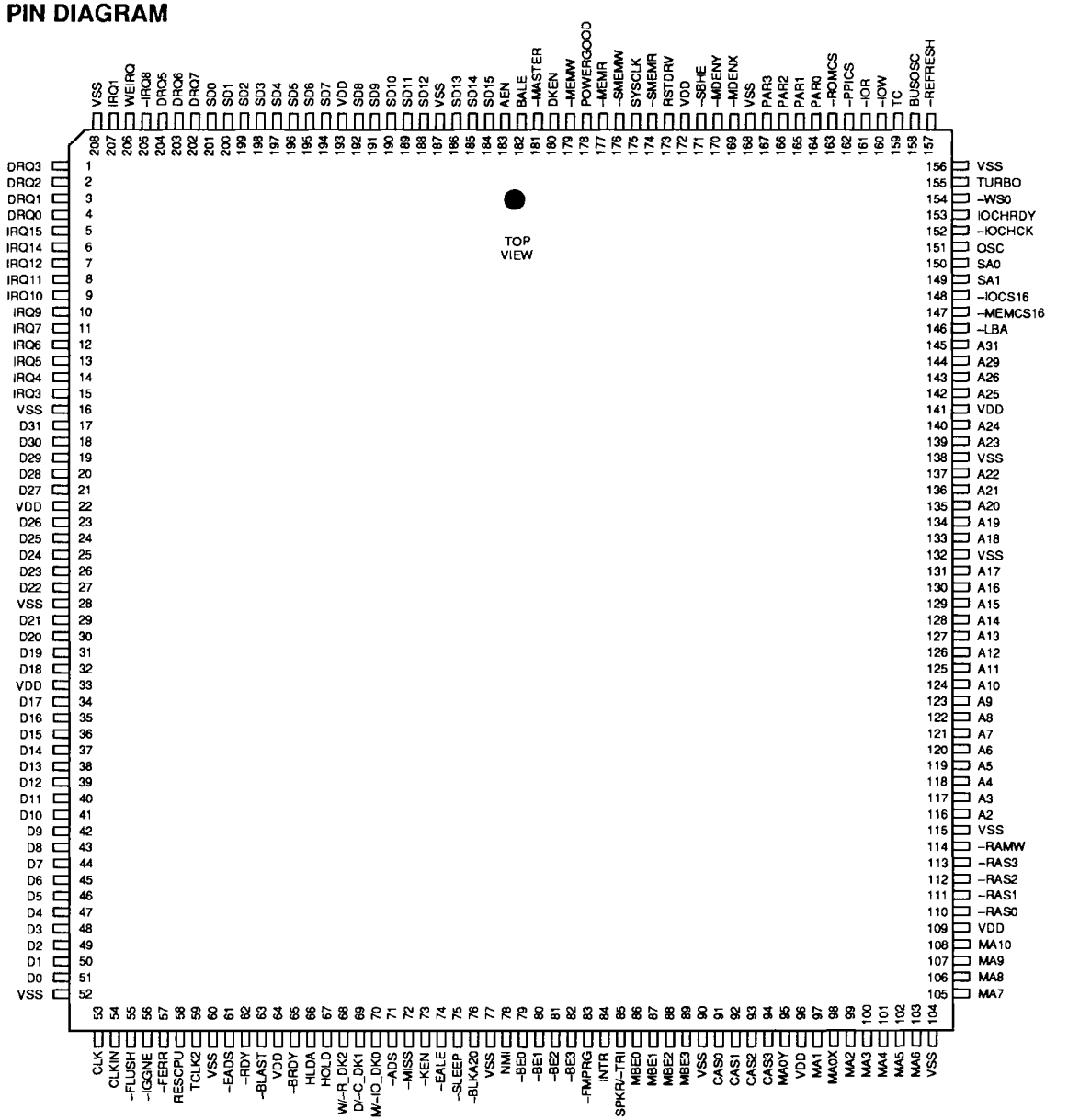
The VL82C486 can be programmed to generate the ISA bus timing from the CPU clock oscillator or a separate asyncronous oscillator.

The VL82C486 also performs all of the data buffer control functions required for a 486XX processor-based PC/AT system. Under the control of the CPU, the VL82C486 routes data to and from the CPU's D bus, the internal XD bus, and the slots (SD bus). During CPU ISA bus reads, the data is latched for synchronization with the CPU. Parity is checked for D bus DRAM read operations. The chip does not generate parity for CPU writes to DRAM.

When the DMA requestor or external bus master is the bus owner, the VL82C486 allows data transfer between the slot SD bus and the CPU local D bus. The chip also performs low-to-high and high-to-low byte swaps on the 16-bit SD bus. Parity is generated by the VL82C486 during DMA or Master writes to on-board DRAM. The chip also provides a single input, –TRI, to disable all of its outputs for board level testability. This is a dual function pin SPKR/–TRI. Care must be taken so that the pin is sampled high at the rising edge of POWERGOOD. A coupling to the speaker circuit is recommended.

The VL82C486 Controller functions are programmable via a set of internal configuration registers. The state of various interface pins on reset is used to determine the default configuration. A dip switch can be used to establish the initial configuration.

PIN DIAGRAM


TOP VIEW
1 DRQ3
2 DRQ2
3 DRQ1
4 DRQ0
5 IRQ15
6 IRQ14
7 IRQ12
8 IRQ11
9 IRQ10
10 IRQ9
11 IRQ7
12 IRQ6
13 IRQ5
14 IRQ4
15 IRQ3
16 VSS
17 D31
18 D30
19 D29
20 D28
21 D27
22 VDD
23 D26
24 D25
25 D24
26 D23
27 D22
28 VSS
29 D21
30 D20
31 D19
32 D18
33 VDD
34 D17
35 D16
36 D15
37 D14
38 D13
39 D12
40 D11
41 D10
42 D9
43 D8
44 D7
45 D6
46 D5
47 D4
48 D3
49 D2
50 D1
51 D0
52 VSS
53 CLK
54 CLKIN
55 -FLUSH
56 -IGNNE
57 -FERR
58 RESCPU
59 TCLK2
60 VSS
61 -EADS
62 -RDY
63 -BLAST
64 VDD
65 -BRDY
66 HLDA
67 HOLD
68 W/-R_DK2
69 D/-C_DK1
70 M/-IO_DK0
71 -ADS
72 -MISS
73 -KEN
74 -EALE
75 -SLEEP
76 -BLKA20
77 VSS
78 NMI
79 -BE0
80 -BE1
81 -BE2
82 -BE3
83 -FMPRG
84 INTR
85 SPKR/-TRI
86 MBE0
87 MBE1
88 MBE2
89 MBE3
90 VSS
91 CAS0
92 CAS1
93 CAS2
94 CAS3
95 MA0Y
96 VDD
97 MA1
98 MA0X
99 MA2
100 MA3
101 MA4
102 MA5
103 MA6
104 VSS
105 MA7
106 MA8
107 MA9
108 MA10
109 VDD
110 -RAS0
111 -RAS1
112 -RAS2
113 -RAS3
114 -RAMW
115 VSS
116 A2
117 A3
118 A4
119 A5
120 A6
121 A7
122 A8
123 A9
124 A10
125 A11
126 A12
127 A13
128 A14
129 A15
130 A16
131 A17
132 VSS
133 A18
134 A19
135 A20
136 A21
137 A22
138 VSS
139 A23
140 A24
141 VDD
142 A25
143 A26
144 A29
145 A31
146 -LBA
147 -MEMCS16
148 -IOCS16
149 SA1
150 SA0
151 OSC
152 -IOCHCK
153 IOCHRDY
154 -WS0
155 TURBO
156 VSS
157 -REFRESH
158 BUSOSC
159 TC
160 -IOW
161 -IOR
162 -PPICS
163 -ROMCS
164 PAR0
165 PAR1
166 PAR2
167 PAR3
168 VSS
169 -MDENX
170 -MDENY
171 -SBHE
172 VDD
173 RSTDRV
174 -SMEMR
175 SYSCLK
176 -SMEMW
177 -MEMR
178 POWERGOOD
179 -MEMW
180 DKEN
181 -MASTER
182 BALE
183 AEN
184 SD15
185 SD14
186 SD13
187 VSS
188 SD12
189 SD11
190 SD10
191 SD9
192 SD8
193 VDD
194 SD7
195 SD6
196 SD5
197 SD4
198 SD3
199 SD2
200 SD1
201 SD0
202 DRQ7
203 DRQ6
204 DRQ5
205 -IRQ8
206 WEIRQ
207 IRQ1
208 VSS

PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	DRQ3	I-PU	TTL-S		33	VDD	PWR		
2	DRQ2	I-PU	TTL-S		34	D17	IO	TTL	8
3	DRQ1	I-PU	TTL-S		35	D16	IO	TTL	8
4	DRQ0	I-PU	TTL-S		36	D15	IO	TTL	8
5	IRQ15	I-PU	TTL-S		37	D14	IO	TTL	8
6	IRQ14	I-PU	TTL-S		38	D13	IO	TTL	8
7	IRQ12	I-PU	TTL-S		39	D12	IO	TTL	8
8	IRQ11	I-PU	TTL-S		40	D11	IO	TTL	8
9	IRQ10	I-PU	TTL-S		41	D10	IO	TTL	8
10	IRQ9	I-PU	TTL-S		42	D9	IO	TTL	8
11	IRQ7	I-PU	TTL-S		43	D8	IO	TTL	8
12	IRQ6	I-PU	TTL-S		44	D7	IO	TTL	8
13	IRQ5	I-PU	TTL-S		45	D6	IO	TTL	8
14	IRQ4	I-PU	TTL-S		46	D5	IO	TTL	8
15	IRQ3	I-PU	TTL-S		47	D4	IO	TTL	8
16	VSS	GND			48	D3	IO	TTL	8
17	D31	IO	TTL	8	49	D2	IO	TTL	8
18	D30	IO	TTL	8	50	D1	IO	TTL	8
19	D29	IO	TTL	8	51	D0	IO	TTL	8
20	D28	IO	TTL	8	52	VSS	GND		
21	D27	IO	TTL	8	53	CLK	O		24
22	VDD	PWR			54	CLKIN	I	CMOS	
23	D26	IO	TTL	8	55	–FLUSH	IO (Note 2)	TTL	8
24	D25	IO	TTL	8	56	–IGNNE	IO (Note 2)	TTL	8
25	D24	IO	TTL	8	57	–FERR	I-PU	TTL	
26	D23	IO	TTL	8	58	RESCPU	O		8
27	D22	IO	TTL	8	59	TCLK2	I	CMOS	
28	VSS	GND			60	VSS	GND		
29	D21	IO	TTL	8	61	–EADS	O		8
30	D20	IO	TTL	8	62	–RDY	IO-PU	TTL	8
31	D19	IO	TTL	8	63	–BLAST	IO	TTL	8
32	D18	IO	TTL	8	64	VDD	PWR		

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
65	–BRDY	IO-PU	TTL	8	97	MA1	O		12/24/36/48
66	HLDA	I	TTL		98	MA0X	O		12/24
67	HOLD	O		8	99	MA2	O		12/24/36/48
68	W/–R_DK2	IO	TTL	8	100	MA3	O		12/24/36/48
69	D/–C_DK1	IO	TTL	8	101	MA4	O		12/24/36/48
70	M/–IO_DK0	IO	TTL	8	102	MA5	O		12/24/36/48
71	–ADS	IO	TTL	8	103	MA6	O		12/24/36/48
72	–MISS	I	TTL		104	VSS	GND		
73	–KEN	O		8	105	MA7	O		12/24/36/48
74	–EALE	IO (Note 2)	TTL	8	106	MA8	O		12/24/36/48
75	–SLEEP	I	TTL		107	MA9	O		12/24/36/48
76	–BLKA20	IO (Note 2)	TTL	8	108	MA10	O		12/24/36/48
77	VSS	GND			109	VDD	PWR		
78	NMI	O		8	110	–RAS0	O		12/24
79	–BE0	IO	TTL	8	111	–RAS1	O		12/24
80	–BE1	IO	TTL	8	112	–RAS2	O		12/24
81	–BE2	IO	TTL	8	113	–RAS3	O		12/24
82	–BE3	IO	TTL	8	114	–RAMW	IO (Note 2)		12/24/36/48
83	–FMPRG	IO (Note 2)	TTL	8	115	VSS	GND		
84	INTR	O		8	116	A2	IO	TTL	8
85	SPKR/–TRI	IO-PU	TTL	24	117	A3	IO	TTL	8
86	MBE0	O		8	118	A4	IO	TTL	8
87	MBE1	O		8	119	A5	IO	TTL	8
88	MBE2	O		8	120	A6	IO	TTL	8
89	MBE3	O		8	121	A7	IO	TTL	8
90	VSS	GND			122	A8	IO	TTL	8
91	CAS0	O		12	123	A9	IO	TTL	8
92	CAS1	O		12	124	A10	IO	TTL	8
93	CAS2	O		12	125	A11	IO	TTL	8
94	CAS3	O		12	126	A12	IO	TTL	8
95	MA0Y	O		12/24	127	A13	IO	TTL	8
96	VDD	PWR			128	A14	IO	TTL	8

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
129	A15	IO	TTL	8	161	–IOR (Note 1)	IO	TTL	12/24
130	A16	IO	TTL	8	162	–PPICS	IO (Note 2)	TTL	8
131	A17	IO	TTL	8	163	–ROMCS	IO (Note 2)	TTL	8
132	VSS	GND			164	PAR0	IO	TTL	8
133	A18	IO	TTL	8	165	PAR1	IO	TTL	8
134	A19	IO	TTL	8	166	PAR2	IO	TTL	8
135	A20	IO	TTL	8	167	PAR3	IO	TTL	8
136	A21	IO	TTL	8	168	VSS	GND		
137	A22	IO	TTL	8	169	–MDENX	O		12
138	VSS	GND			170	–MDENY	O		12
139	A23	IO	TTL	8	171	–SBHE	IO	TTL	12/24
140	A24	IO	TTL	8	172	VDD	PWR		
141	VDD	PWR	TTL		173	RSTDRV	O		8
142	A25	IO	TTL	8	174	–SMEMR (Note 1)	O		12/24
143	A26	IO	TTL	8	175	SYSCLK	O		12/24
144	A29	IO	TTL	8	176	–SMEMW (Note 1)	O		12/24
145	A31	IO	TTL	8	177	–MEMR (Note 1)	IO	TTL	12/24
146	–LBA	I	CMOS		178	POWERGOOD	I-PU	TTL-S	
147	–MEMCS16	I	TTL		179	–MEMW (Note 1)	IO	TTL	12/24
148	–IOCS16	I	TTL		180	DKEN	IO (Note 2)	TTL	12/24
149	SA1	IO	TTL	12/24	181	–MASTER	I	TTL	
150	SA0	IO	TTL	12/24	182	BALE	O	TTL	12/24
151	OSC	I	TTL		183	AEN	O	TTL	12/24
152	–IOCHCK	I	TTL		184	SD15	IO	TTL	12/24
153	IOCHRDY (Note 1)	IO-OD	TTL	12	185	SD14	IO	TTL	12/24
154	–WS0	I	TTL		186	SD13	IO	TTL	12/24
155	TURBO	I	TTL		187	VSS	GND		
156	VSS	GND			188	SD12	IO	TTL	12/24
157	–REFRESH (Note 1)	IO-OD	TTL	24	189	SD11	IO	TTL	12/24
158	BUSOSC	I-PU	TTL		190	SD10	IO	TTL	12/24
159	TC	O		12/24	191	SD9	IO	TTL	12/24
160	–IOW (Note 1)	IO	TTL	12/24	192	SD8	IO	TTL	12/24

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
193	VDD	PWR			201	SD0	IO	TTL	12/24
194	SD7	IO	TTL	12/24	202	DRQ7	I-PU	TTL-S	
195	SD6	IO	TTL	12/24	203	DRQ6	I-PU	TTL-S	
196	SD5	IO	TTL	12/24	204	DRQ5	I-PU	TTL-S	
197	SD4	IO	TTL	12/24	205	–IRQ8	I-PU	TTL-S	
198	SD3	IO	TTL	12/24	206	WEIRQ	I-PD	TTL	
199	SD2	IO	TTL	12/24	207	IRQ1	I-PU	TTL-S	
200	SD1	IO	TTL	12/24	208	VSS	GND		

Notes: 1. These pins require an external pull-up resistor (10 kΩ is recommended).

2. These pins are inputs only during POR (power-on reset).

Legend:

CMOS	CMOS-compatible input
I	Input-only pin
IO	Bidirectional pin
GND	Ground pin
O	Output-only pin
OD	Open drain
PWR	Power supply pin
TTL	TTL-compatible input
-PD	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VSS (internal pull-down resistor on pin).
-PU	Indicates a high-impedance with approximately 10 kΩ minimum resistance to VDD (internal pull-up resistor on pin).
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Pin Type	Signal Description
CPU INTERFACE SIGNALS			
A31, A29, A26-A2	145, 144, 143, 142, 140, 139, 137-133, 131-116	IO	Address bus - This bidirectional address bus is driven by the bus master. It is driven out by the VL82C486 during Non-Master Mode DMA and refresh cycles when HLDA is active and –MASTER is inactive. The signals A25-A2 allow access to 64 MB of system memory. The upper two bits of the bus, A31 and A29, are used for accessing system ROM and the Weitek numeric coprocessor. A26 is used to provide a non-aliased unused address space above 64 MB to assist memory sizing routines.
–ADS	71	IO	Address Status - The active low Address Status (–ADS) signal is driven by the 486 as an indication that the address and control signals currently supplied by the CPU are valid. This signal is used internally to indicate that the data and command are valid and determine the beginning of a memory or I/O cycle. –ADS is driven by the VL82C486 when HLDA is active, and is made low for one CPU clock cycle at the beginning of DMA or Master Mode cycles when a local bus region is selected by the PMR Registers.
–BE3 - –BE0	82-79	IO	Byte Enable bits 3 through 0 - These signals are normally inputs to the VL82C486 and indicate which bytes on D31-D0 are involved in a memory or I/O access. They are ignored during all DRAM reads. –BE3 - –BE0 are driven by the VL82C486 when HLDA is active and indicate which one or two bytes are involved in an 8- or 16-bit DMA or Master Mode transfer between the slot I/O and a local bus device.
–BLAST	63	IO	Burst Last - This signal is used by the VL82C486 as an indicator of when to terminate the current burst cycle, if the length of the burst cycle is less than four double words. It is driven low by the VL82C486 when HLDA is active, since the VL82C486 does not support Burst Mode during DMA or Master Mode cycles.
–BRDY	65	IO-PU	Burst Ready - The active low ready (–BRDY) signal indicates to the 486 that the current burst cycle is complete. It is driven low when valid data has been presented to the CPU in response to a read command or when data has been accepted in response to a write command from the CPU. The VL82C486 drives –BRDY on all local bus DRAM accesses, but never drives it in response to slot bus accesses (see –RDY definition). The VL82C486 enables the –BRDY three-state output only when it needs to drive it low and leaves –BRDY enabled for just one CPU clock cycle after it has driven –BRDY high again. When HLDA is active, –BRDY is an input to the VL82C486 and may be driven by a local bus device to terminate DMA or Master Mode cycles. This pin has an internal pull-up resistor.
CLK	53	O	Clock - This output is a CMOS level signal which is normally one-half the frequency of the TCLK2 signal. It is used by the CPU and other on-board logic.
CLKIN	54	I	Input Clock - This is the fundamental clock input to the VL82C486. It must be the same clock as that supplied to the 486.
M/–IO_DK0	70	IO	Memory Input/Output or DMA Acknowledge bit 0 - When HLDA is low, M/–IO_DK0 is driven by the local bus master and is decoded with D/–C_DK1 and W/–R_DK2 to indicate the type of bus cycle requested When HLDA is high, M/–IO_DK0 is an output signal which along with D/–C_DK1 and W/–R_DK2 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses) this signal is forced high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
D/–C_DK1	69	IO	Data Control or DMA Acknowledge bit 1 - When HLDA is low, D/–C_DK1 is driven by the local bus master and is decoded with M/–IO_DK0 and W/–R_DK2 to indicate the type of bus cycle requested. When HLDA is high, D/–C_DK1 is an output signal which along with M/–IO_DK0 and W/–R_DK2 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses), the D/–C_DK1 signal is forced high.
W/–R_DK2	68	IO	Write/Read or DMA Acknowledge bit 2 - When HLDA is low, W/–R_DK2 is driven by the local bus master and is decoded with D/–C_DK1 and M/–IO_DK0 to indicate the type of bus cycle requested. When HLDA is high, W/–R_DK2 is an output signal which along with D/–C_DK1 and M/–IO_DK0 represents the encoded channel number being serviced at the beginning of DMA acknowledge cycles. If the VL82C486 makes –ADS active during DMA or Master Mode cycles (for local bus accesses), the W/–R_DK2 signal indicates whether a local bus read or write cycle is required.
D31-D0	17-21, 23-27 29-32, 34-51	IO	CPU Data Bus bits 31 through 0 - This is the data bus directly connected to the CPU and other external devices.
–EADS	61	O	External Address - The active low external address signal indicates a primary cache invalidation address is on the address bus. It is driven low by the VL82C486 to perform primary cache invalidations during DMA and Master Mode cycles, and is also driven low for one cycle during the first T2 of a local bus write to a write-protected memory location. It is also modulated for implementation of the Non-Turbo Mode.
–FERR	57	I-PU	Floating Point Error - This signal indicates a floating point error. When active, it generates interrupt IRQ13 internal to the VL82C486. This input pin is active low and has an internal pull-up.
HLDA	66	I	Hold Acknowledge - An active high signal that is issued by the CPU in response to the HOLD signal driven by the VL82C486. It indicates that the CPU is floating its outputs' to the high impedance state so that another master can take control of the bus.
HOLD	67	O	Hold Request - This active high output signal is driven by the VL82C486 to the CPU. It indicates that a bus master (such as a DMA or refresh controller) is requesting control of the bus. It is synchronized to CLKIN.
–IGNNE	56	IO (Note 1)	Ignore Numeric Error Output (or POR Input) - This active low output, when asserted, indicates to the CPU to ignore the present numeric error. This signal is enabled when a dummy write is performed to either Port F0h or F1h with –FERR also active. –IGNNE is an input during power-on reset to set SA1 timing.
INTR	84	O	Interrupt Request - An active high output used to interrupt the CPU. It is generated by the 82C59A megacell any time a valid interrupt request input is received.
–KEN	73	O	Cache Enable - This signal determines whether the current cycle is cacheable. It is normally low, but is driven inactive during the second and subsequent T2 cycles of all CPU memory accesses that are defined non-cacheable, except when local bus CPU cycles are selected by the PMR Registers; in this case, it is made inactive during the first subsequent T2s of the local bus cycle.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
NMI	78	O	Non-Maskable Interrupt - An active high output which indicates to the CPU that an external non-maskable interrupt has been generated. This signal is asserted by either a parity error or an I/O channel error. The NMI output is enabled by resetting the MSB (most significant bit) of I/O Port 70h. NMI is disabled on reset.
–RDY	62	IO-PU	(Non-Burst) Ready - Driven by the VL82C486, this active low signal is an indication that the current memory or I/O slot bus cycle is complete. The VL82C486 enables the –RDY three-state output only when it needs to drive it low and leaves it enabled for just one CPU clock cycle after it has driven –RDY high again. When HLDA is active, –RDY is an input to the VL82C486 and may be driven by local bus devices to terminate DMA and Master Mode cycles. This pin has an internal pull-up resistor.
RESCPU	58	O	Reset CPU - This active high output resets the CPU. It is synchronous to CLKIN and is asserted in response to one of the following: 1. A dummy read from I/O Port EFh. 2. The LSB (least significant bit) of Port A is set to 1 by an active write. 3. The POWERGOOD signal changes state. 4. A Shutdown command.
TCLK2	59	I	This input is connected to a crystal oscillator that has a frequency of twice the system frequency. It is divided and sent to the CLK output.
ON-BOARD MEMORY SYSTEM INTERFACE SIGNALS			
CAS3-CAS0	94-91	O	Column Address Strobe bits 0 through 3 - These signals generate high-going column address strobes for DRAM banks during on-board memory bus cycles. The active period for these signals is determined by the number of wait states and the configuration mode.
MBE3-MBE0	89-86	O	Memory Byte Enable bits 3 through 0 - These signals are used along with the CAS3-CAS0 signals to generate independent column address strobes for each of the four DRAM banks.
MA10-MA1	108-105, 103-99, 97	O	Memory Address bus bits 10 through 1 - These address bits are the row and column addresses sent to on-board memory. They are buffered and multiplexed versions of the local CPU bus address. They allow addressing of up to 64 MB of memory by the VL82C486.
MA0X	98	O	Memory Address bus bit 0, Banks 0 and 2 - This signal is a multiplexed row/column address bit for Banks 0 and 2. It is interleaved with MA0Y to ensure that DRAM setup and hold times are met for A3 during the Fast Burst Interleave Mode.
MA0Y	95	O	Memory Address bus bit 0, Banks 1 and 3 - This signal is a multiplexed row/column address bit for Banks 1 and 3. It is interleaved with MA0X to ensure that DRAM setup and hold times are met for A3 during the Fast Burst Interleave Mode.
–MDENX, –MDENY	169, 170	O	Memory Dword Enable bits X and Y - These active low outputs select the upper and lower 32-bit double word when a 64-bit wide DRAM bank is connected in a system. –MDENX and –MDENY enable the upper and lower 32 bits of the 64-bit DRAM data bus onto the 32-bit CPU data bus. They are never enabled simultaneously during DRAM reads and are always enabled simultaneously during DRAM writes.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
PAR3-PAR0	167-164	IO	Parity bits 3 through 0 - Each parity bit signal is associated with one byte of the data bus. PAR3–PAR0 are written to memory along with their corresponding bytes during DMA and Master Mode memory write operations. During memory read operations, these pins become inputs and are used along with their respective data bytes to determine if a parity error has occurred.
–RAMW	114	IO (Note 1)	RAM Write Output (or POR Input) - This active low output is sent to the DRAM memory to control the direction of data flow of the on-board memory. It is active during on-board memory write cycles and high at all other times. –RAMW is an input during power-on reset to set the BIOS ROM location.
–RAS3- –RAS0	113-110	O	Row Address Strobe bits 3 through 0 - These signals are sent to each of the four DRAM banks to strobe in the row address during on-board memory bus cycles.
CACHE CONTROLLER INTERFACE SIGNALS			
–BLKA20	76	IO (Note 1)	Block A20 Output (or POR Input) - When this signal is low, it indicates that the CPU and cache should mask address bit 20 (A20) for all operations. –BLKA20 is an input during power-on-reset to set the DRAM output drives.
–FLUSH	55	IO (Note 1)	Cache Flush Output (or POR Input) - This signal goes low for one CPU clock cycle in the second T2 of a local bus flush cycle. –FLUSH is an input during power-on reset to set DKEN polarity.
–MISS	72	I	Cache Miss - This active low input is made active by a cache controller at the start of a CPU memory read cycle if the operand is not in the secondary cache. When high in T2 of any CPU memory access, it causes the VL82C486 to cancel the requested cycle. It is tied low when no secondary cache is used. –MISS is ignored during on-board DRAM cycles for DMA/Master Mode cycles unless the –EALE pin is pulled low (for write-back cache option) during power-on reset; in which case it inhibits DMA/Master Mode DRAM read cycles if it is made high when –MEMR is active.
PERIPHERAL INTERFACE SIGNALS			
–EALE	74	IO (Note 1)	Early Address Latch Enable Output (or POR Input) - This signal is normally low. It goes high when BALE is high for all CPU slot bus cycles. During ISA bus refresh cycles –EALE goes high for 0.5 SYSCLKs before going low again. –EALE is an input during power-on reset to set the –MISS operation.
–FMPRG	83	IO (Note 1)	Flash Memory Program Output (or POR Input) - This signal is asserted when the FMPRG bit (bit 2) in the ROMSET Register is set. It may be used to gate the appropriate programming voltage to the flash memory. –FMPRG is an input during power-on reset to set the slot current drive.
–LBA	146	I	Local Bus Access - During CPU accesses, this signal must be made low by a local bus device before one half-way through the first T2 cycle of any CPU bus cycle that normally accesses on-board DRAM, or before the end of first T2 for any other type of cycle, if a CPU access is to a local bus device. It causes the VL82C486 to be deselected.
–PPICS	162	IO (Note 1)	Peripheral Chip Select Output (or POR Input) - This output signal is an active low chip select for the keyboard controller and real-time clock. It is active any time a system bus address is 60h, 64h, 70h, or 71h. –PPICS is an input during power-on reset to set the DRAM output drivers.
POWERGOOD	178	I-PU	System Power-On Reset - An active high input signal indicating that the power to the board is stable. A Schmitt-trigger input is used, thus allowing the input to be connected directly to an RC network.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
-ROMCS	163	IO (Note 1)	ROM Chip Select Output (or POR Input) - This active low signal is asserted during CPU cycles that access on-board system ROM. The on-board system ROM may reside either on the local (D) bus or the ISA (SD) bus. -ROMCS is an input during power-on reset to set the DRAM configuration.
-SLEEP	75	I	Sleep Mode - A high-to-low transition on this pin puts the VL82C486 into the Sleep Mode. The Sleep Mode is when the refresh divider is active, BUSOSC is shut-off from non-essential internal circuitry, and the CPU is halted by HOLD going high.
SPKR/-TRI	85	IO-PU	Speaker or Three-State - This pin functions as the SPKR output signal and as the active low Three-State input signal. The active high SPKR output drives an externally buffered speaker. This signal is an input when the POWERGOOD input is low. If this input is sampled low, it forces the VL82C486 into the Three-State Mode where all outputs and bidirectional pins are driven to a high impedance state. This pin has an internal pull-up resistor.
TURBO	155	I	Turbo Mode - This bit determines the speed at which the CPU operates. When set low, hold signals to the 486 are continuously generated in order to slow its operation. It is also an input to the NTBREF Register from which its state may be read by software.
WEIRQ	206	I-PD	Weitek Numeric Coprocessor Interrupt - The active high WEIRQ signal indicates that an error has occurred within the Weitek numeric coprocessor. It causes an internal IRQ13 to be generated. This pin has an internal pull-down resistor.
BUS INTERFACE SIGNALS			
AEN	183	O	Address Enable - An active high output that indicates a DMA transfer cycle to the I/O resources on the bus. It is asserted only when the DMA controller is the bus owner (HLDA = 1, -MASTER = 1). The I/O resource with an active DMA Acknowledge signal should only respond to the I/O command lines and all the other I/O resources should ignore the commands.
BALE	182	O	Bus Address Latch Enable - This active high pulse is generated at the beginning of any bus cycle initiated by the CPU. It indicates when the SA19-SA0, LA23-LA17, AEN, and -SBHE signals are valid. BALE is forced high any time HLDA is high.
BUSOSC	158	I-PU	System Bus Clock - This signal is supplied by an external oscillator. It has a nominal 50% duty cycle and normally has a frequency of 16 MHz. It is used for ISA bus operations. If an oscillator is connected to this pin, SYSCLK can be programmed to be BUSOSC +2, +4, +6, or +8. If SYSCLK is to be derived from CLKIN, BUSOSC is held high or low and is used in conjunction with the CLKCTL Register to determine the clock divider value.
DKEN	180	IO (Note 1)	DMA Acknowledge Enable Input (or POR Output) - This signal enables an external 3-to-8 decoder for the generation of the DMA acknowledge signals from M/-IO_DK0, D/-C_DK1 and W/-R_DK2 when these signals are valid at the beginning of a DMA cycle. If a local bus cycle is started during a DMA cycle, then DKEN must also be used to latch the DMA acknowledges when active. It is active high when the -FLUSH signal is pulled high during power-on reset and is active low when -FLUSH is pulled low during power-on reset. DKEN is an input during power-on-reset to set the BIOS ROM width.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
DRQ7-DRQ5 DRQ3-DRQ0	202-204 1-4	I-PU	DMA Request bits 7 through 5 and 3 through 0 - These asynchronous inputs are used by external devices to indicate when they need service from the internal DMA controllers. DRQ3-DRQ0 are used for transfers between 8-bit I/O adapters and system memory. DRQ7-DRQ5 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally as it is used to cascade the two DMA controllers together. All DRQ pins have internal pull-ups.
–IOCHCK	152	I	I/O Channel Check - This active low input signal indicates that an error has taken place on the I/O bus. If I/O checking is enabled, an –IOCHCK assertion by a peripheral device generates an NMI to the processor if bit 3 (ENA_IO_CHK) of Port B is set to 0. The state of the –IOCHCK signal is read as data bit 6 (CHAN_CHK) of Port B.
IOCHRDY	153	IO-OD	I/O Channel Ready - This input is pulled low in order to extend the read or write cycles of any bus access when required. The cycle can be initiated by the CPU, DMA controllers or refresh controller. The default number of wait states for cycles initiated by the CPU are four wait states for 8-bit peripherals, one wait state for 16-bit peripherals, and three wait states for ROM cycles. One DMA wait state is inserted as the default for all DMA cycles. Any peripheral that cannot present read data or strobe in write data in this amount of time must use IOCHRDY to extend these cycles. In the DMA Mode, this pin is always driven low by the VL82C486 that generates local bus cycles to allow for local bus latency. The VL82C486 never drives IOCHRDY high, but three-states it when not driven low. This pin requires an external 10 kΩ pull-up resistor.
–IOCS16	148	I	16-bit I/O Chip Select - This input signal determines when a 16-bit to 8-bit conversion is needed for CPU accesses. A conversion is done any time the VL82C486 requests a 16-bit I/O cycle and –IOCS16 is sampled high. A command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long when a conversion is needed. If sampled low, an I/O access is performed in one wait state with one command delay inserted. The –IOCS16 signal is ignored by the DMA and refresh controller for DMA transfer and refresh cycles, respectively.
–IOW –IOR	160 161	IO IO	Input/Output Write Input/Output Read –IOR and –IOW are active low inputs when an external bus master is in control (HLDA = 1, –MASTER = 0). They function as outputs at all other times. When HLDA is low, they are driven by the internal ISA bus controller. During DMA transfer cycles (HLDA = 1, –MASTER = 1), they are driven by the 82C37A DMA controller megacells. They are inactive during a refresh cycle. Both the pins require external 10 kΩ pull-up resistors.
IRQ15, IRQ14 IRQ12-IRQ9 IRQ7-IRQ3 IRQ1, –IRQ8	5, 6 7-10 11-15 207, 205	I-PU	Interrupt Requests - These are the asynchronous interrupt request inputs to the 82C59A megacells. IRQ0, IRQ2, and IRQ13 are not available as external inputs because they are used internally. All IRQ input pins except –IRQ8 are active high and have internal pull-ups. –IRQ8 is an active low input. All IRQ pins have a special programmable logic to reduce noise sensitivity. The logic is controlled by the IRQIN bit (bit 0) in the MISCSET Register. When IRQIN is set, the input to these pins must be stable for at least 105 ns to generate an interrupt.
–MASTER	181	I	Bus Master - An active low input used by an external device to get access to the system bus. When asserted, it indicates that an external bus master has control of the bus.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
–MEMCS16	147	I	16-Bit Memory Chip Select - This active low input is used to determine when a 16-to-8 bit conversion is needed for CPU accesses. A conversion is done any time the VL82C486 requests a 16-bit memory cycle and –MEMCS16 is sampled high. If sampled high, a command delay of one BUSOSC cycle is inserted and the cycle becomes four wait states long. If sampled low, a memory access is performed in one wait state with no command delays inserted. The –MEMCS16 signal is ignored by the DMA and refresh controller for transfer and refresh cycles, respectively.
–MEMR –MEMW	177 179	IO IO	Memory Read Memory Write These active low signals are inputs when an external bus master is in control (HLDA = 1, –MASTER = 0). They are outputs at all other times. When HLDA is low, –MEMW is driven from the ISA bus controller. They are driven by the 82C37A DMA controllers during DMA cycles. Both pins require external 10 kΩ pull-up resistors.
OSC	151	I	Oscillator Input - The buffered input of the 14.31818 MHz oscillator with a duty cycle of 45 to 55%.
–REFRESH	157	IO-OD	Memory Refresh - Whenever a refresh cycle is initiated, this signal is pulled low. An external bus master activates this signal when it requires a refresh cycle from the refresh controller. The internal refresh controller activates this line every 15.6 µs to prevent loss of DRAM data. –REFRESH is an open drain output capable of sinking 24 mA and requires an external pull-up resistor.
RSTDRV	173	O	Reset - This active high output is system reset generated from the POWERGOOD input. RSTDRV is synchronized to the BUSOSC input. On reset, this signal remains high for at least as long as the RESCPU signal. It may therefore be used to drive the 486 AHOLD input to initiate a 486 self-test sequence on power-up reset only.
SA1, SA0	149, 150	IO	System Address bus bits 1 and 0 - These two signals represent the lower two bits of the system address bus. They act as inputs when an external bus master is in control (HLDA = 1, –MASTER = 0) and are outputs at all other times. When HLDA is low, SA1 and SA0 are generated by decoding the CPU byte enables (–BE3 - –BE0). They are driven by the 82C37A DMA controllers during DMA transfer cycles. SA0 is always connected directly to the ISA bus. SA1 is connected to the ISA bus if discrete SA buffers are used. If the VL82C113A I/O Combination chip is used, then SA1 is connected only to the A1 input of the VL82C113A (which then drives the ISA bus SA1 signal). The –IGNNE signal is used to set SA1's timing at power-on reset for use with/without the VL82C113A.
–SBHE	171	IO	System Byte High Enable - An active low signal that indicates valid data is on the upper byte of the system data bus (SD15-SD8). Its functionality is similar to that of the SA1 and SA0 signals. –SBHE is forced low during 16-bit DMA cycles and is the complement of SA0 during 8-bit DMA cycles.
SD15-SD0	184-186, 188-192, 194-201	IO	System Data Bus bits 15 through 0 - These bidirectional signals are directly connected to the slots.
–SMEMR –SMEMW	174 176	O O	System Memory Read System Memory Write These outputs are active during memory read and write cycles, respectively, when the address is below 1 MB. Both pins require an external 10 kΩ pull-up resistor.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Pin Type	Signal Description
SYSCLK	175	O	System Clock - The SYSCLK output is 1/2, 1/3, 1/4, 1/6, or 1/8 the frequency of TCLK2 or BUSOSC depending on the BUSOSC pin's status and the five lower bits in the CLKCTL Register. The bus control signals BALE, –IOR, –IOW, –MEMR and –MEMW are synchronized to SYSCLK.
TC	159	O	Terminal Count - This active high output indicates that one of the DMA channels has transferred all data.
–WS0	154	I	Wait State Terminate - An active low input that indicates a shorter access cycle. It is pulled low by a peripheral on the slot bus to terminate a CPU controlled bus cycle earlier than the default values defined internally on the chip.
POWER AND GROUND PINS			
VSS	16, 28, 52, 60, 77, 90, 104, 115, 132, 138, 156, 168, 187, 208	GND	Ground connection, 0 volts.
VDD	22, 33, 64, 96, 109, 141, 172, 193	PWR	Power connection, nominally +5 volts. These pins should each have 0.1 µF bypass capacitors.

Note 1: These pins are inputs only during POR (power-on reset.)

FUNCTIONAL DESCRIPTION

The VL82C486 can be divided into three main blocks:

- System Controller Block - Includes the clock generation, the CPU interface, the numeric coprocessor interface, the address decoder and the memory controller.
- ISA Bus Controller Block - Includes the dual DMA controllers (82C37A), dual programmable interrupt controllers (82C59A), the programmable interval timer (82C54), the ISA sequencer, and the logic for refresh generation and refresh/DMA arbitration.
- Data Buffer Block - Contains the latching and steering logic necessary to convert 32-bit CPU bus cycles to 8/16-bit ISA bus cycles. This block also contains the parity generation and checking logic.

The sections following cover detailed information for the various logical groupings of the VL82C486's subsystems (see Figure 1). In most cases, the effect of configurable elements that can be controlled via I/O registers is discussed at length.

FIGURE 1. VL82C486 SUBSYSTEMS